HEWLETT PACKARD

ENGINEERING DIAGRAMS SET

HP 3000 SERIES II COMPUTER SYSTEM

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LIST OF EFFECTIVE PAGES

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ILLUSTRATIONS (continued)

TABLES

GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION

1-2. The Engineering Diagrams Set provides component location and schematic diagrams for the HP 3000 Series II Computer System. Also included is an explanation of the logic symbology used to document the system and signal and power distribution information.

1-3. SCOPE

1-4. This manual is intended for use by Customer Engineers who are familiar with the system theory and maintenance procedures.

1-5. Sections II through V contain the following information:

a. Section II, Logic Symbology. Section II describes the logic symbology used in the system. It also provides integrated circuit diagrams and describes the operation of complex logic elements.

b. Section III, PCA Locations. Section III contains diagrams and tables that illustrate the configurations of the standard system models and PCA locations of each model.

c. Section IV, Wiring Information. Section IV contains information on connections between PCA's and equipment bays.

d. Section V, Diagrams. Section V contains schematic, part location, and part number information for printed circuit assemblies (PCA's) used in the system. This section is arranged by product numbers.

LOGIC SYMBOLOGY

SECTION II

2-1. INTRODUCTION

2-2. This section covers basic logic information and symbology as used in this and related manuals. Following the description of symbology is a table of integrated circuits containing diagram symbols for most circuits and descriptions of operation for complex logic functions.

2-3. LOGIC STATES.

2-4. The logic signals are always in one of two possible states, a "1" or a "0." These two states are also referred to as high (H) or low (L). The high and low states reflect the relative voltage levels of the signals; the high state is always relatively more positive than the low state. Note that both states may have actual voltage values that are positive, or both may be absolutely negative; the significance is in the *relative* levels of the two states. In the text of the manuals, logic states are normally described as "high" or "low."

2-5. The "not" bar associated with signal names is used to indicate whether the "active" state of the signal is high or low. For example, if the presence of data on a signal line is represented by a low signal, the signal name for the line might be "not" Data 1; if a signal clears the output register when the signal is low, the signal might be described as "not" Clear Output Register ($\overline{\text{COR}}$). The "not" bar must be considered an integral part of the signal name; this means that there are high states for "not" signals and low states for "not" signals, just as there are high and low states for signals without the "not" bar.

2-6. INVERSION.

2-7. Logic inversion is indicated by an inversion dot at the input or output of a logic symbol. When this dot appears at the input of a logic symbol, the input will be effective when the input signal is low. When the dot appears at the output of a logic symbol the output will be of the opposite state to what would be delivered if the dot were not present.

2-8. LOGIC SYMBOLOGY.

2-9. Three basic symbol shapes distinguish the major classes of logic circuits depicted in this manual. These are gates, regenerative switching elements, and amplifiers. Each symbol and a brief explanation of its operation is given in the following paragraphs.

2-10. In addition to the basic symbols, a general multipurpose symbol is used wherever a standardized logic symbol does not exist. A brief explanation of this multipurpose symbol is included.

2-11. GATES.

2-12. A gate is a circuit that produces a binary output when certain input conditions are met. The gate symbol has input lines connecting to one side of the symbol, and output lines connecting to the other side, as shown in figure 2-1. Since the inputs and outputs are easily identifiable, the symbol can be shown left-facing, right-facing, or facing up or down.

2-13. There are four basic types of gates: "and," "or," "nand," and "nor," each named for the logic function that it performs. Each of these gates is described in the following paragraphs. In addition, a brief explanation of an "expander" gate is given following the descriptions of the basic logic gates.

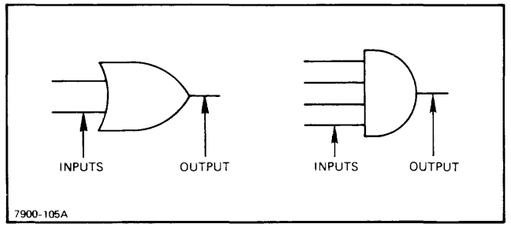
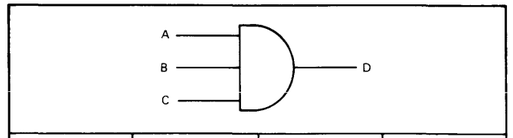


Figure 2-1. Gate Symbols

2-14. "AND" GATE.

2-15. The "and" gate shown in figure 2-2 performs a logical "and" function. It will produce a high output only when all of the input lines are high. Input A *and* input B *and* input C must be high for a high output to be generated.



A	B	C	D
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

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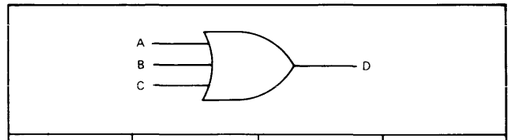
Figure 2-2. Three-Input "And" Gate Logic Symbol and Truth Table

2-16. "OR" GATE.

2-17. The "or" gate performs a logical "or" function. It produces a high output when one *or* more inputs are high. The truth table in figure 2-3 shows the various states of a three-input "or" gate.



A	B	C	D
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

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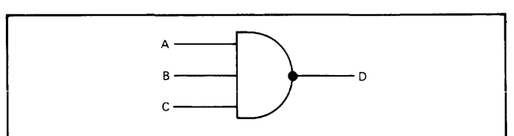
Figure 2-3. Three-Input "Or" Gate Logic Symbol and Truth Table

2-18. "NAND" GATE.

2-19. The "nand" gate is similar to the "and" gate described previously, except that its output is inverted. The gate generates a low output when all inputs are high. The various states of a three-input "nand" gate are shown in the truth table in figure 2-4.



A	B	C	D
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

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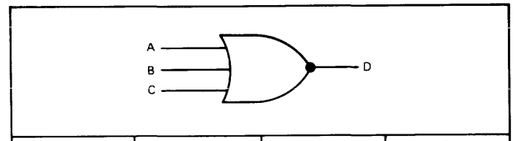
Figure 2-4. Three-Input "Nand" Gate Logic Symbol and Truth Table

2-20. "NOR" GATE.

2-21. The "nor" gate is identical to the "or" gate described previously, except that its output is inverted. The gate generates a low output when one or more inputs are high. The various states of a three-input "nor" gate are shown in the truth table in figure 2-5.



A	B	C	D
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

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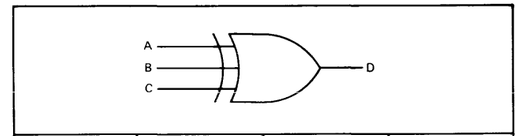
Figure 2-5. Three-Input "Nor" Gate Logic Symbol and Truth Table

2-22. "EXCLUSIVE OR" GATE.

2-23. The "exclusive or" gate is a variation of the basic "or" gate. It has two or more input signals. The output is high when only one input is high. The truth table in figure 2-6 shows the functioning of a three-input exclusive "or" gate.



A	B	C	D
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	L

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Figure 2-6. Three-Input "Exclusive Or" Gate Logic Symbol and Truth Table

2-24. EXPANDER GATE

2-25. Some logic gates have additional input lines which may be used to increase or "expand" the number of input signals. These expanding input lines use different signal levels than the normal gate input. The expander gate provides these special signal levels. The expander gate may provide one or two output lines to drive the expanded gate.

2-26. An expanded input will normally be indicated by the letter "E". Figure 2-7 shows both single and double line expanded inputs. When more than one expander gate is used the expanded inputs are connected together.

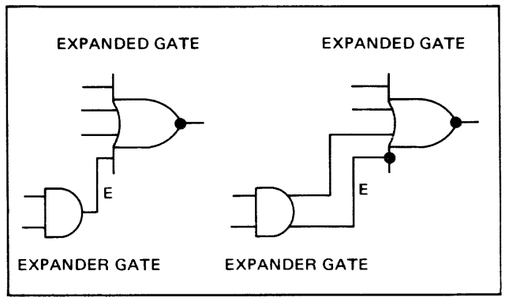


Figure 2-7. Expander Gate Logic Symbol

2-27. STROBE LINES.

2-28. Strobe lines may be used to enable the output lines of tri-state logic elements. The strobe inputs are shown connected at right angles to the normal signal flow. Examples of a strobe controlled gate and amplifier are shown in figure 2-8.

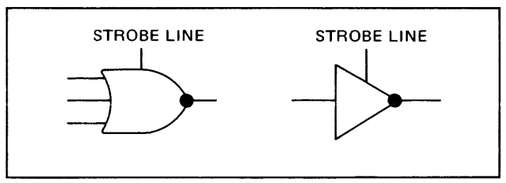


Figure 2-8. Strobe Controlled Gate and Amplifier Symbols

2-29. ENCODING GATE.

2-30. The encoding gate (figure 2-9) has one input and multiple outputs. When the input is high, all outputs (B, C, and D) are high. When the input is low, the outputs are all low.

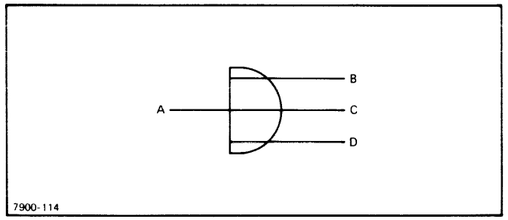


Figure 2-9. Three-Input Encoding Gate, Logic Symbol

2-31. A typical circuit for an encoding gate is shown in figure 2-10. With A high, all diodes conduct and all outputs are clamped high. With A low, each diode is practically an open circuit, and points B, C, and D assume the voltage level of the circuit to which each is connected.

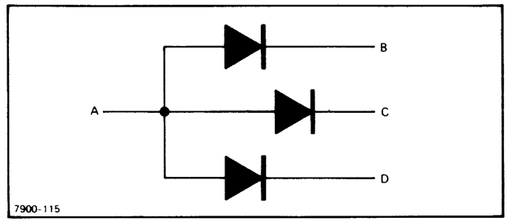


Figure 2-10. Typical Encoding Gate Circuit

2-32. MULTIVIBRATORS.

2-33. The multivibrators described here are of four basic types: flip-flops, Schmitt trigger circuits, one-shot multivibrators, and free-running multivibrators. All furnish a binary output. However, unlike gate circuits, the duration of a multivibrator output signal is not dependent on the duration of an input signal.

2-34. The basic logic symbol for a multivibrator is a rectangle as shown in figure 2-11. Letters in the symbol indicate the type of multivibrator. The rectangle is divided horizontally, with the upper portion representing the "set side" and the lower portion representing the "clear side." The multivibrator is considered set when the output from the set side is high. It is considered cleared when the output from the clear side is high. To avoid confusion, the symbol is always oriented as shown in figure 2-11 inputs on the left, outputs on the right.

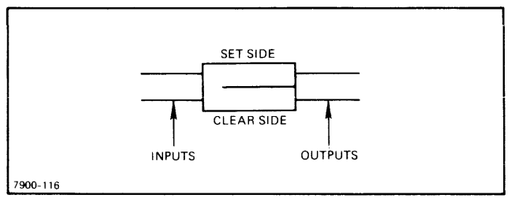


Figure 2-11. Basic Logic Symbol Multivibrator

2-35. FLIP-FLOP.

2-36. The symbol for a flip-flop is shown in figure A-12. The letters "FF" preceded by the name of the flip-flop distinguish this symbol from other types of multivibrators. Additional identification, described later, identifies the particular type of flip-flop.

2-37. A flip-flop is a bistable switching device; an external signal is required to set the flip-flop and another to clear it. The flip-flop remains in its current state until switched to the opposite state by the appropriate external signal. Various forms of flip-flops exist, of which seven are described here: the R-S (reset-set), clocked R-S, J-K, clocked J-K, toggle, latch, and delay flip-flops.

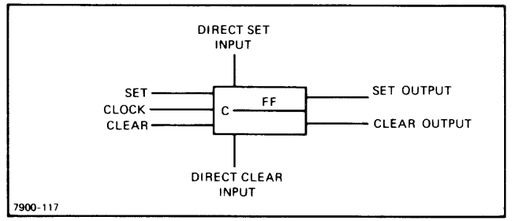
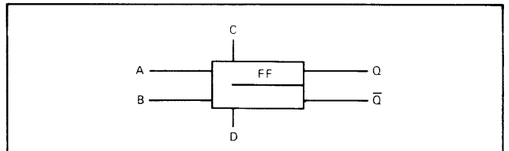


Figure 2-12. General Flip-Flop Logic Symbol

2-38. R-S FLIP-FLOP. The symbol for the R-S flip-flop as shown in figure 2-13 can be recognized by the fact that there is no information in the symbol identifying it as one of the other six types. The R-S flip-flop has a minimum of two input terminals (A and B in figure 2-13) and one or two output terminals Q and $\overline{Q}$. One or two additional input terminals, C and D, may be used.

2-39. The R-S flip-flop is set by a high input at A (assuming no inverting dot at this point). It can also be set by a high input at C, if this input terminal is present. The flip-flop is cleared by a high input at B or D. Figure 2-13 includes a truth table, showing the flip-flop outputs resulting from various input conditions.



INPUT		OUTPUT	
A	B	Q	$\overline{Q}$
L	L	No Change	
H	L	H	L
L	H	L	H
H	H	Indeterminate	

Figure 2-13. R-S Flip-Flop, Logic Symbol, and Truth Table

2-40. After being set or cleared, the R-S flip-flop remains in that condition after termination of the set or clear pulse. If the flip-flop is either set or clear and it receives an input to place it in the existing state no change takes place in the state of the flip-flop.

2-41. Simultaneously high set and clear input signals normally are not permitted, and circuit design usually prevents occurrence of this condition at a time when the flip-flop outputs are used. If simultaneous set and clear inputs are received, both outputs of the flip-flop are high for the duration of the simultaneous inputs. The eventual state of the flip-flop is determined by the input that remains high longest.

2-42. CLOCKED R-S FLIP-FLOP. The clocked R-S flip-flop is similar to the R-S flip-flop, but it has a clock pulse input as shown in figure 2-14. The logic symbol can be recognized by the letter "C" at this input terminal. At the positive-going transition of the clock pulse, the flip-flop becomes set if input A is high, or it becomes clear if input B is high (assuming no inverting dot at the clock pulse input terminal). If inputs A and B are both low during the clock pulse, the flip-flop does not change state. It is not permissible that A and B both be high when the positive-going clock pulse transition takes place.

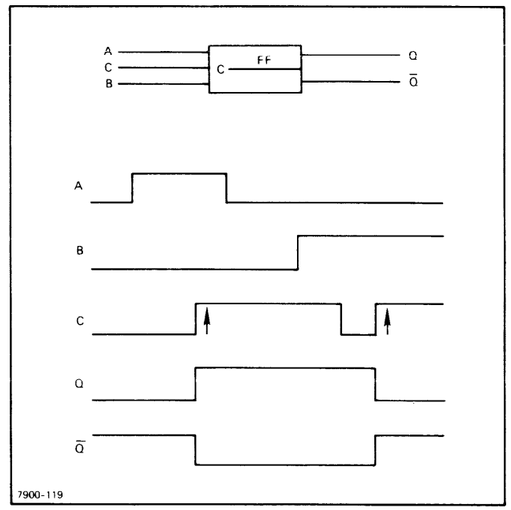


Figure 2-14. Clocked R-S Flip-Flop, Logic Symbol, and Switching Waveforms

2-43. When the clocked R-S flip-flop has an inverting dot at the clock pulse input (figure 2-15), the negative-going transition of the clock pulse is the transition that is effective in setting or clearing the flip-flop.

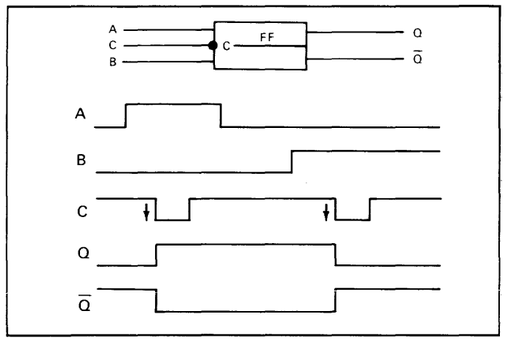


Figure 2-15. R-S Flip-Flop with Inverted Clock Input, Logic Symbol, and Switching Waveforms

2-44. In some cases the clocked R-S flip-flop has a set and clear input at the top and bottom of the logic symbol (inputs D and E, figure 2-16). These inputs are independent of the clock pulse, and are referred to as the direct set and direct clear inputs. They function as a result of a high or low level, rather than a positive- or negative-going transition. An inverting dot at the direct set or clear input indicates that a low level is required to set or clear the flip-flop. No dot indicates that a high level is required. The direct set and clear inputs are also used on other types of flip-flops.

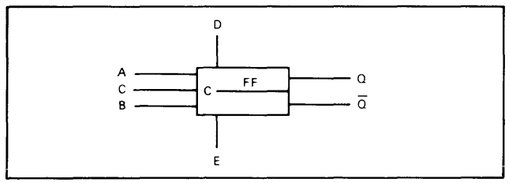


Figure 2-16. Logic Symbol for Clocked R-S Flip-Flop with Direct Set and Direct Clear Inputs

2-45. TOGGLE FLIP-FLOP. The symbol for the toggle flip-flop as shown in figure 2-17 can be recognized by the letter "T" in the symbol. This flip-flop has a single input. If there is no inverting dot at this input, each time the input signal becomes high, outputs Q and $\overline{Q}$ change state. Since two inputs are required to produce one complete cycle of the output, the toggle flip-flop functions as a divide-by-two element, and is commonly used in groups in counting circuits, with the output of one flip-flop driving the next. Figure 2-17 shows the switching waveforms for one flip-flop.

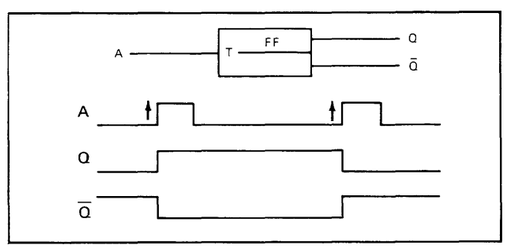


Figure 2-17. Toggle Flip-Flop Logic Symbol and Switching Waveforms

2-46. If a toggle flip-flop symbol has an inverting dot at the input connection, the flip-flop changes state at the negative-going transition of the input. The symbol and waveforms for this type of flip-flop are shown in figure 2-18.

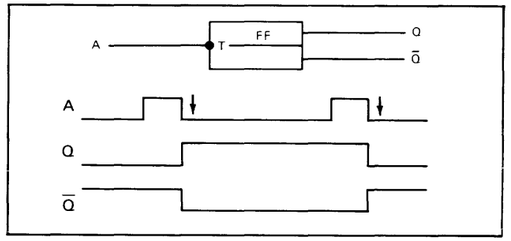


Figure 2-18. Toggle Flip-Flop with Inverted Input, Logic Symbol, and Switching Waveforms

2-47. J-K FLIP-FLOP. In the J-K flip-flop, simultaneous high inputs for both set and clear will reverse the existing state of the flip-flop. This requires some method of storing two conditions, the previous output state and the new output state, until the clock pulse time. The set and clear inputs are labeled J and K respectively. In order to provide the necessary output storage the flip-flops are combined in a dual-rank configuration, together with the necessary gates to form a single logic element. For simplicity the internal dual-rank arrangement of the flip-flop is not usually shown. (See figure 2-19.)

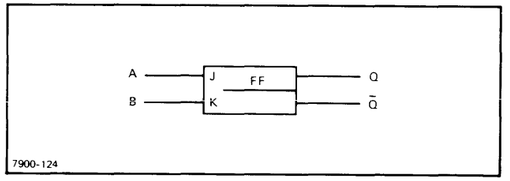


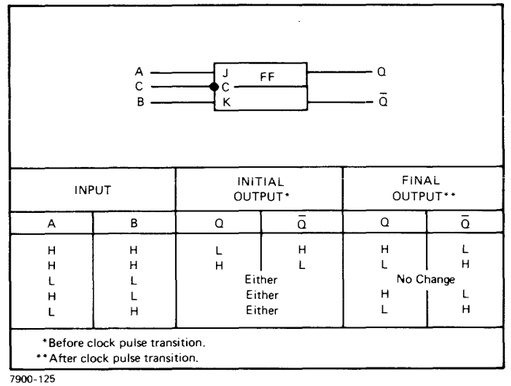
Figure 2-19. J-K Flip-Flop Logic Symbol

2-48. CLOCKED J-K FLIP-FLOP. The clocked J-K flip-flop as shown in figure 2-20 is similar to the clocked R-S flip-flop. However, simultaneous set and clear inputs to the J-K flip-flop are permissible. Under these conditions, the J-K flip-flop changes its state at the occurrence of each positive-going clock pulse transition. With an inverting dot at the clock pulse input, the flip-flop changes state at the negative-going clock pulse transition. If both J and K inputs are high, the flip-flop will toggle when a clock pulse is received.

2-49. The J-K flip-flop can also be operated with one high input and one low input. It then functions in the same manner as the clocked R-S flip-flop.

2-50. Figure 2-20 includes a truth table showing operation of the J-K flip-flop. Note that with both inputs high at the time of clock pulse transition, the final state of the flip-flop (after clock pulse transition) depends on the state before the transition. With only one input high, the initial state of the flip-flop is immaterial.

2-51. In some cases the J-K flip-flop consists of two separate flip-flops, with the output of one applied to the input of the other. Usually, a single flip-flop logic symbol is used to illustrate this circuit. The clock pulse inverting dot, or the lack of it, indicates the clock pulse transition that affects the output flip-flop of the pair.



INPUT		INITIAL OUTPUT*		FINAL OUTPUT**	
A	B	Q	$\overline{Q}$	Q	$\overline{Q}$
H	H	L	H	H	L
H	H	H	L	L	H
L	L	Either		No Change	
H	L	Either		H	L
L	H	Either		L	H

*Before clock pulse transition.
**After clock pulse transition.

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Figure 2-20. Clocked J-K Flip-Flop Logic Symbol and Truth Table

2-52. LATCH FLIP-FLOP. The latch flip-flop shown in figure 2-21 can be recognized by the letter "L" in the symbol. The flip-flop has a clock input and a data input. Although the logic symbol shows one input-signal connection to the flip-flop, this seperates inside the integrated circuit package to form two inputs to the pack. After separation, one input is inverted (indicated by the inverting dot) before application to the flip-flop.

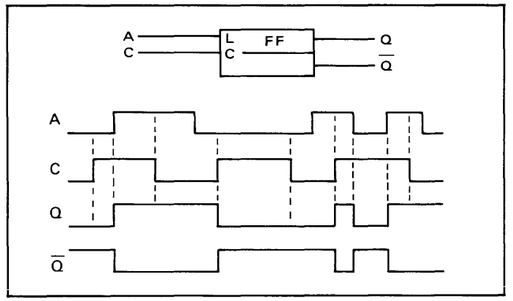


Figure 2-21. Latch Flip-Flop Logic Symbol and Switching Waveforms

2-53. The set-side input is responsive to high signal levels at A in figure 2-22, and the clear input is responsive to low signal levels at A. If there is no inverting dot at the clock input, this response takes place when the clock pulse is high. While the clock pulse remains high, the outputs follow any changes in the logic level at A as these changes take place. When the clock pulse becomes low, the flip-flop retains its current state, and no longer responds to changes of the input signal.

2-54. If the clock input connection of a latch flip-flop has an inverting dot, the flip-flop responds to the input signal while the clock pulse is low.

2-55. DELAY FLIP-FLOP. The delay flip-flop shown in figure 2-22 is identified by a letter "D" inside the flip-flop symbol. This type of flip-flop is similar to the latching flip-flop, except that it responds to the input signal only at the transition of the clock pulse. The delay flip-flop thus does not follow changes in the input signal as these changes take place.

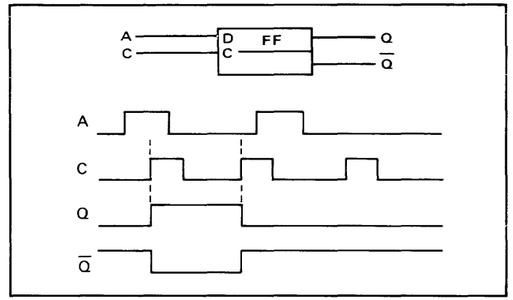


Figure 2-22. Delay Flip-Flop Logic Symbol and Switching Waveforms

2-56. GATE FLIP-FLOP. The gate flip-flop is made up of two logic gates, connected as shown in figure 2-23. The number of inputs to each gate can vary from that shown. The flip-flop can also be made up of two "nor" gates. The circuit may have a set output, a clear output, or both.

2-57. The gate flip-flop functions like an R-S flip-flop, but it has the advantage that it can "or" inputs without the addition of a separate "or" gate. Another reason for use of the gate flip-flop is that if two spare gates are available in integrated circuits on a circuit card, they can be employed as an R-S flip-flop without the need to add another integrated circuit to the card.

2-58. If the flip-flop is made up of two "nand" gates, as in figure 2-23, it is set by a low input at either A or B. Similarly, it is cleared by a low input at C or D. When the flip-flop is in the quiescent state (not undergoing transition), the inputs at A, B, C, and D are all high.

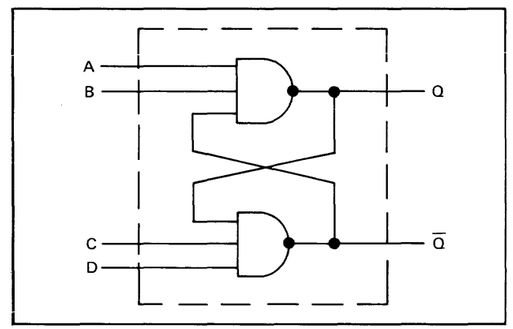


Figure 2-23. "Nand" Gate Flip-Flop, Logic Symbol

2-59. A "nor" gate flip-flop is shown in figure A-24. In this type of flip-flop all inputs are low when the device is in the quiescent state. A high input at A sets the flip-flop, and a high input at B clears it. The outputs cross in the illustration in order to align the set and clear inputs with the set and clears outputs, respectively.

2-60. In most circuits using the "nand" or "nor" gate flip-flop, input signals are such that the flip-flop does not receive high set and clear input signals simultaneously. If circuit design does permit this to occur, both the set- and the clear-side outputs are high for the duration of the condition. The eventual state of the flip-flop is determined by the input that remains longest in the activating condition.

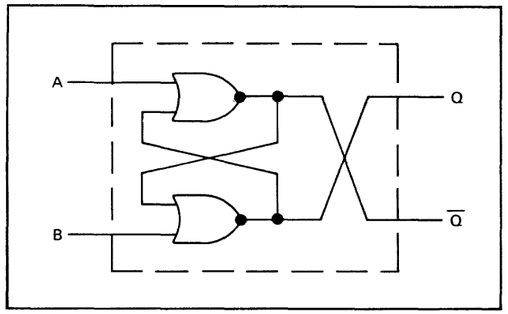


Figure 2-24. "Nor" Gate Flip-Flop Logic Symbol

2-61. SCHMITT TRIGGER.

2-62. The Schmitt trigger circuit shown in figure 2-25 can be identified by the letters "ST" appearing in the logic-diagram symbol. Like the various types of flip-flops this circuit is a two-state device which does not perform a Boolean function. It serves for level sensing or signal squaring. It may have a set-side output, a clear-side output, or both.

2-63. When the input voltage at A is below a certain level, the Schmitt trigger is in the clear state. When the input voltage rises above the reference level, the trigger assumes the set state. Circuit constants establish the reference level.

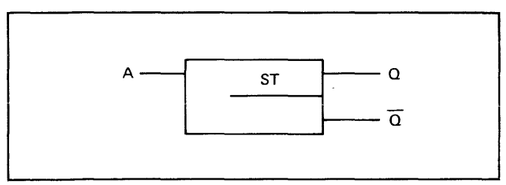


Figure 2-25. Schmitt Trigger Circuit Logic Symbol

2-64. Switching between states takes place rapidly, and the Schmitt trigger is therefore useful for squaring signals that have poor rise and fall times. It can produce a square-wave from a sine wave. Other uses of the Schmitt trigger are voltage level restoration, and detection of the rise of the input signal above a given level.

2-65. ONE-SHOT

2-66. The one-shot multivibrator (figure 2-26) is a monostable switching element, used to produce a pulse of predetermined duration. The device is triggered into its unstable state by an external signal. It returns to the stable state after a time interval determined by circuit constants.

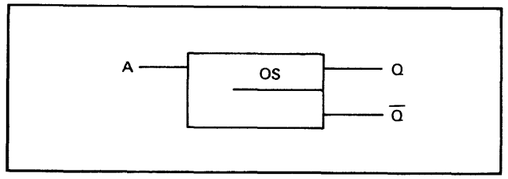


Figure 2-26. One-Shot Multivibrator Logic Symbol

2-67. If there is no inverting dot at the input, triggering is accomplished when input A undergoes a positive-going transition. If there is an inverting dot, a negative-going transition is required. The one-shot multivibrator may have a set-side output, a clear-side output, or both.

2-68. The symbol for the one-shot multivibrator is always drawn with the orientation shown in figure 2-26, with the input at the left and the output or outputs at the right.

2-69. FREE-RUNNING MULTIVIBRATOR.

2-70. The free-running multivibrator shown in figure 2-27 can be distinguished by the letters "MV" appearing in the symbol. This device produces trains of complementary pulses at Q and $\overline{Q}$. Pulse width is determined by circuit constants.

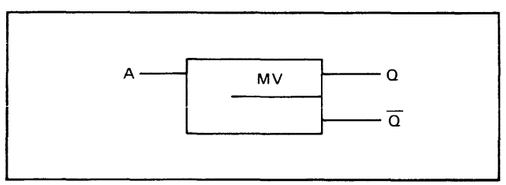


Figure 2-27. Free-Running Multivibrator Logic Symbol

2-71. In some instances a control signal is applied to the free-running multivibrator. If there is no inverting dot at the signal input to the symbol, the multivibrator runs when the control signal is high, and stops when the signal is low. When it is stopped, the multivibrator is in the clear condition. If there is an inverting dot at the control signal input, a low input is required to bring the multivibrator into operation. This type of multivibrator is in the set condition when it is not running.

2-72. Figure 2-28 shows typical waveforms for a controlled free-running multivibrator that runs when the control signal is high. The high and low portions of the output waveforms need not be of equal duration.

2-73. The symbol for the free-running multivibrator is always drawn with the orientation shown in figure 2-28, with the input (if any) at the left, and the output or outputs at the right.

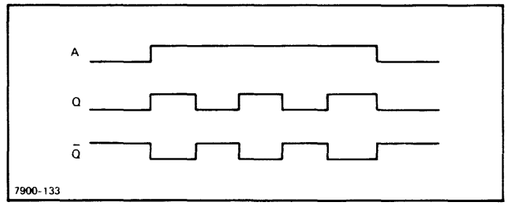


Figure 2-28. Input and Output Waveforms of Controlled Free-Running Multivibrator

2-74. AMPLIFIER.

2-75. The symbol for an amplifier is shown in figure 2-29. A differential amplifier is illustrated in figure 2-30. Like gates, these symbols may be oriented in any of four positions.

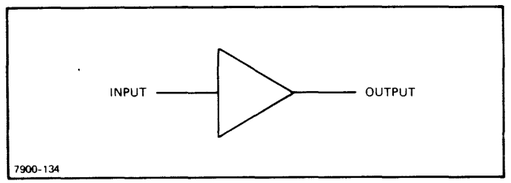


Figure 2-29. Amplifier Logic Symbol

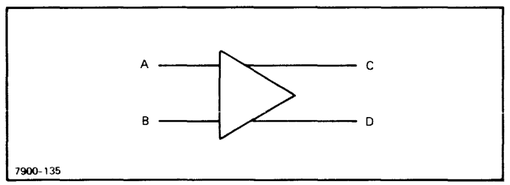


Figure 2-30. Differential Amplifier Logic Symbol

2-76. In most instances, the amplifier symbol has a non-binary input. A circuit which restores the voltage level of a binary input, or which furnishes a low-impedance output from a binary input, is indicated by a one-input "and" gate symbol. An inverting dot at the output of an amplifier symbol indicates that the amplifier inverts the input signal.

2-77. MULTIPURPOSE LOGIC SYMBOL.

2-78. The multipurpose logic symbol is used to indicate a logic function that has not received a standardized logic symbol. The multipurpose symbol is also used to depict multiple logic elements that act together to perform a single overall logic function such as decoding, data storage, or counting. The symbol shown in figure 2-31 may be of varying proportions (mostly commonly 2:1 or 1:2), but rectangular in shape. The symbol includes a descriptive name indicating the overall logic function performed. All active inputs should be labeled to indicate the effect on the overall function. Other descriptive information may be included as needed.

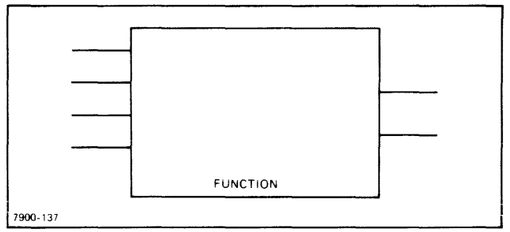


Figure 2-31. Multipurpose Logic Symbol

2-79. Examples of nonstandard symbols are given in figure 2-32. Figure 2-32a shows a binary-to-octal decoder. Figure 2-32b shows a four-bit up/down counter.

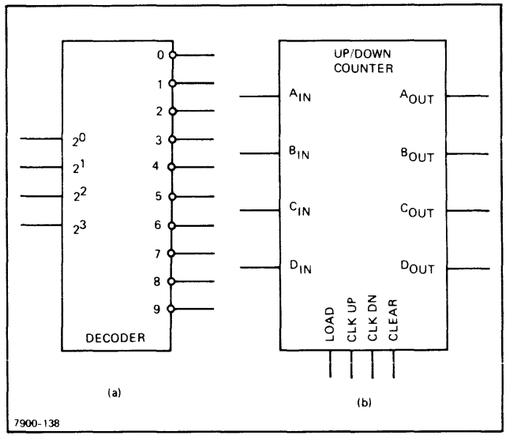
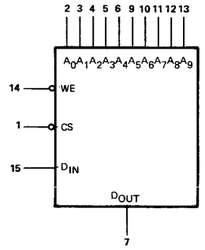
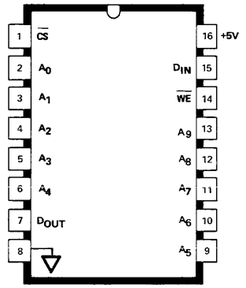


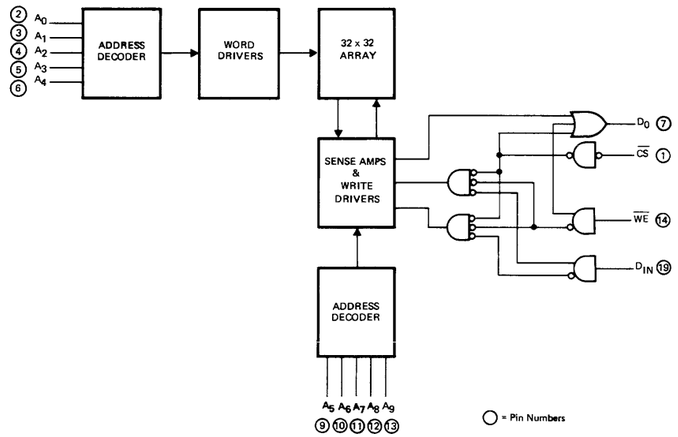
Figure 2-32. Nonstandard Logic Symbols

1816-0914
1024 BIT RAM



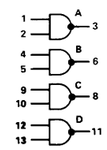


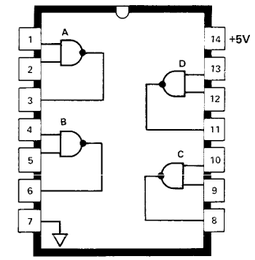
LOGIC DIAGRAM



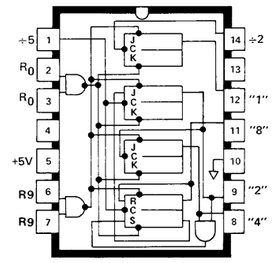
The 1024-bit RAM is organized in 1024 words by 1-bit. Full address decoding is included in the chip. Read and write operations are controlled by the state of the active low Write Enable $\overline{WE}$. With $\overline{WE}$ held low and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

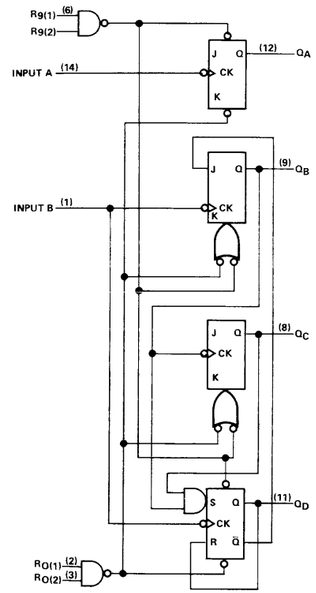
1820-0054
QUAD 2-INPUT NAND GATE



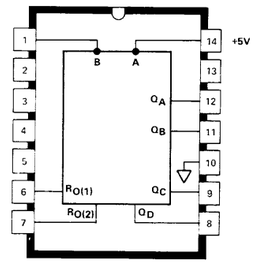


1820-0055
DECADE COUNTER



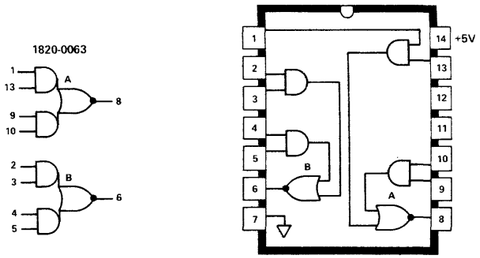


1820-0056
DIVIDE BY 12 COUNTER

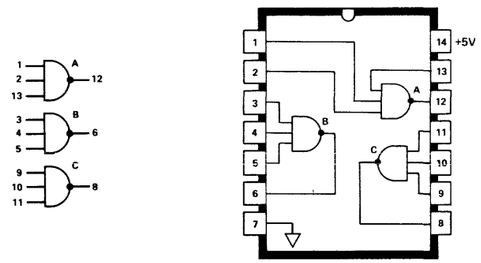


COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

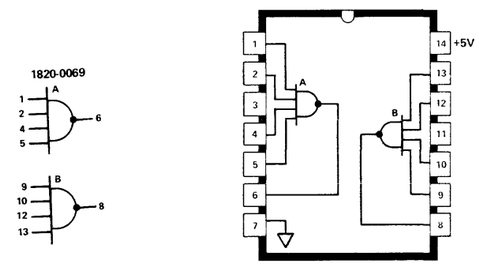
1820-0063
DUAL 2-WIDE 2-INPUT AND-NOR GATE



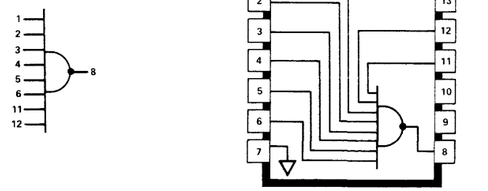
1820-0068
TRIPLE 3-INPUT NAND GATE



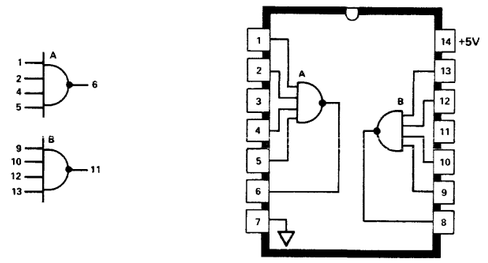
1820-0069
DUAL 4-INPUT NAND GATE



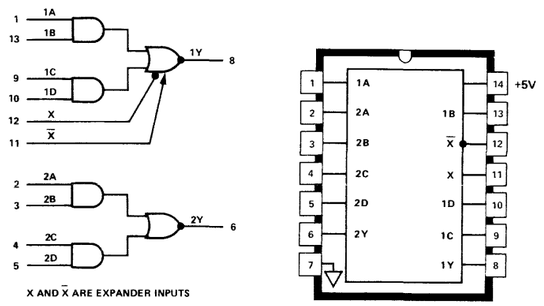
1820-0070
8-INPUT NAND GATE



1820-0071
DUAL 4-INPUT NAND GATE

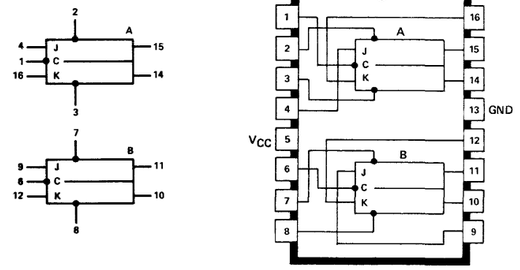


1820-0072
DUAL 2-WIDE 2-INPUT AND-NOR GATE

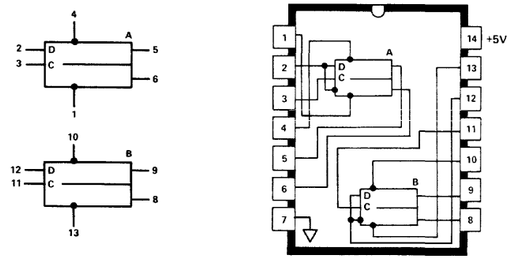


X AND X̄ ARE EXPANDER INPUTS

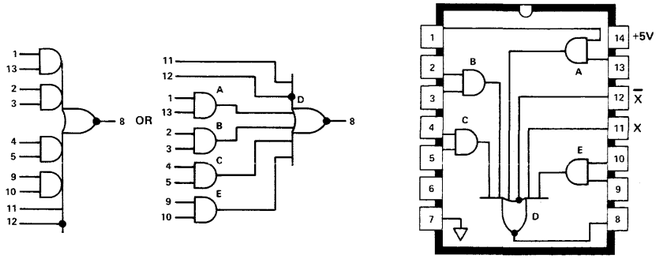
1820-0076
DUAL JK FLIP-FLOP



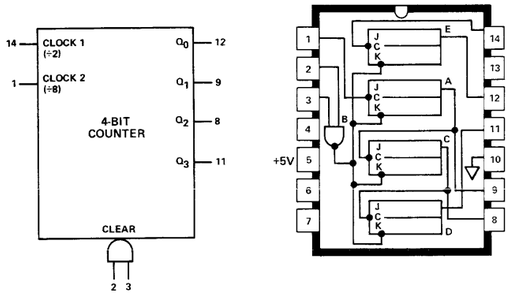
1820-0077
DUAL D FLIP-FLOP



1820-0084
4-WIDE AND-NOR GATE

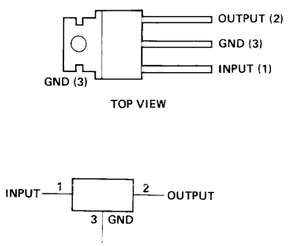


1820-0099
4-BIT BINARY COUNTER



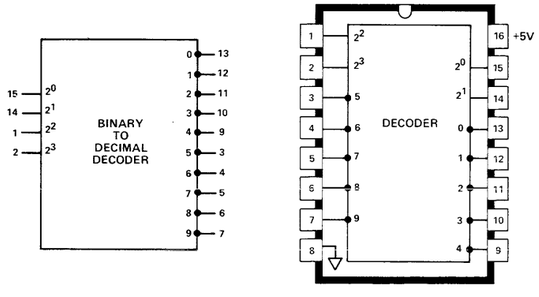
High input signals on the clock 1 line cause the output at Q_0 to toggle. High input signals on the CLOCK 2 line cause outputs Q_1 - Q_3 to count. If the Q_0 output is used as the CLOCK 2 input, then the circuit will act as a simple 4-bit (÷ 16) counter. Simultaneous high signals at pins 2 and 3 will clear the counter.

1820-0106
VOLTAGE REGULATOR



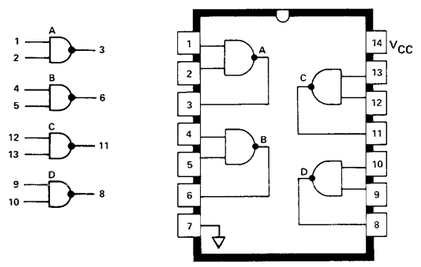
This integrated circuit is a 15 + 0.6 Vdc three terminal positive voltage regulator with current limiting. If internal power dissipation becomes to high thermal shutdown circuit takes over thus preventing the IC from overheating.

1820-0111
BINARY-TO DECIMAL DECODER

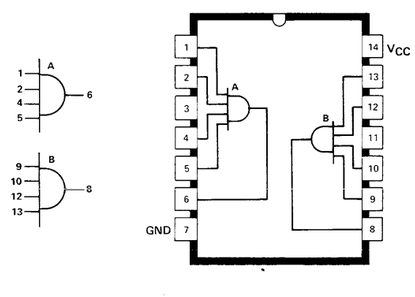


Data on the input lines is interpreted as a binary number. The output line representing the decimal equivalent of the binary input will go low and remain low until the input data is changed. Input data for decimal numbers greater than 9 result in all outputs being high.

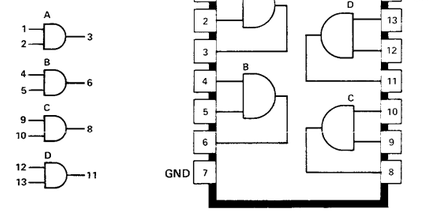
1820-0127
QUAD 2-INPUT NAND GATE



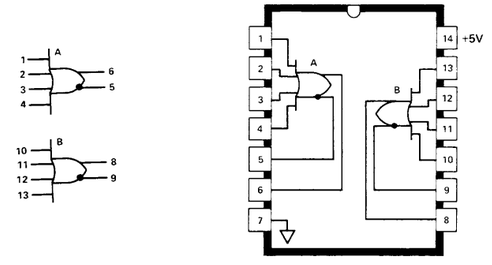
1820-0140
DUAL 4-INPUT AND GATE



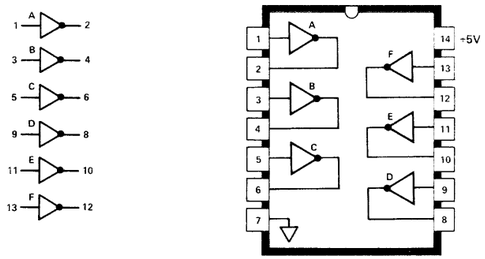
1820-0141
QUAD 2-INPUT AND GATE



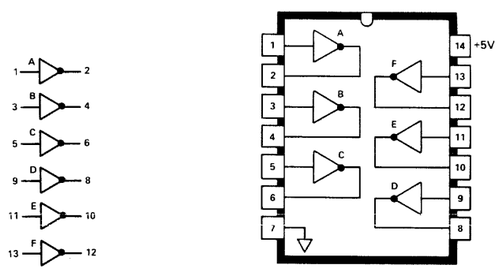
1820-0142
DUAL 4-INPUT OR-NOR GATE



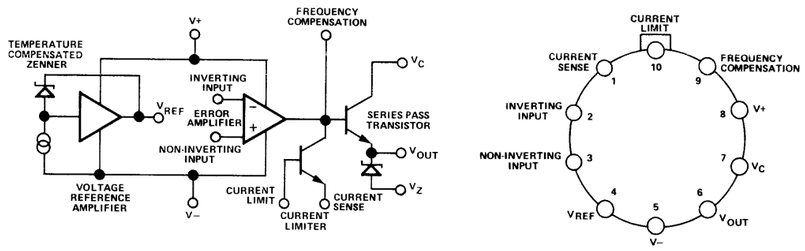
1820-0174
HEX INVERTER



1820-0175
HEX INVERTER

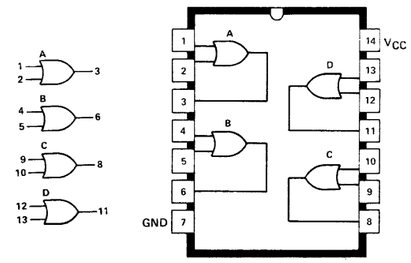


1820-0196
PRECISION VOLTAGE REGULATOR

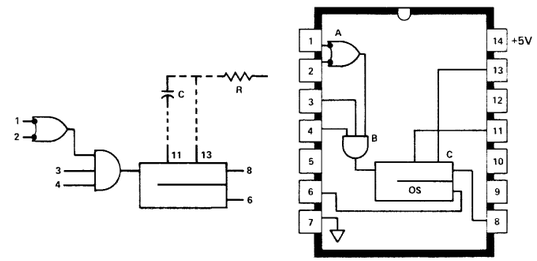


This integrated circuit provides a regulated output voltage and a low-current reference voltage. Provisions are included for voltage shut-down in the event of excessive current in an external circuit. The integrated circuit can be used with external components in a variety of configurations.

1820-0205
QUAD 2-INPUT CR GATE

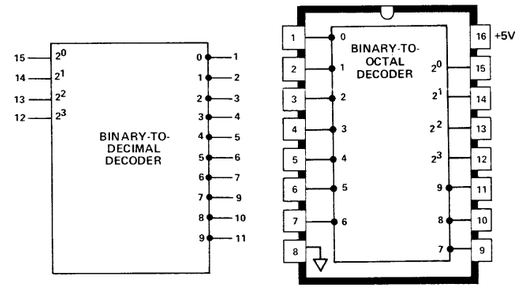


1820-0207
ONE-SHOT



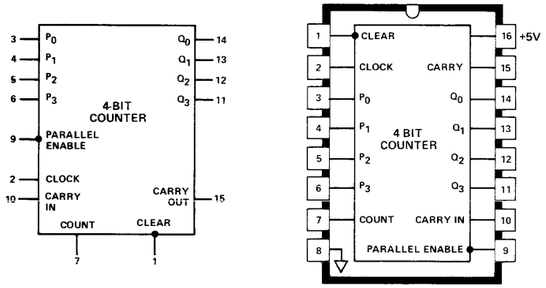
The one-shot is triggred bythe input signal. This produces a pulse with duration determined by the external RC elements.

1820-0214
BCD-TO-DECIMAL DECODER



The binary code on the input lines (2^0-2^3) is decoded and the appropriate output line (0-9) will go low. Codes greater than 9 result in all output lines remaining high.

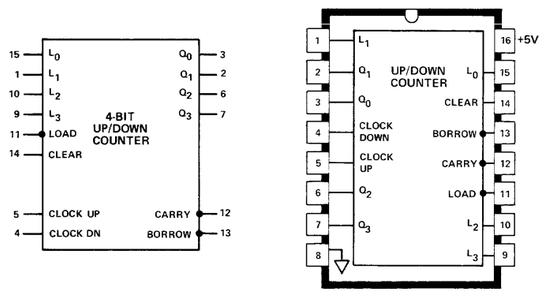
1820-0231
4-BIT COUNTER



The counter is set from the parallel input lines. When the clock input line goes high and a negative input is applied to the PARALLEL ENABLE line, the counter is loaded. When the clock goes high and both the COUNT and CARRY IN lines go high, the counter will be incremented. The new count will be present on the output lines following the low-to-high transition of the clock.

The CARRY OUT line will be high if the CARRY IN line is high and the counter lines are all high.

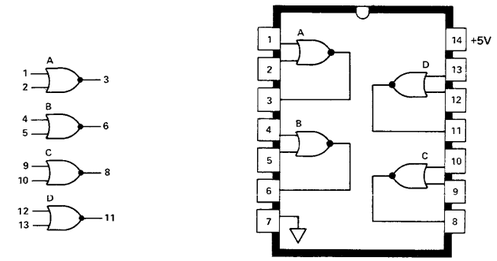
1820-0233
4-BIT UP/DOWN COUNTER



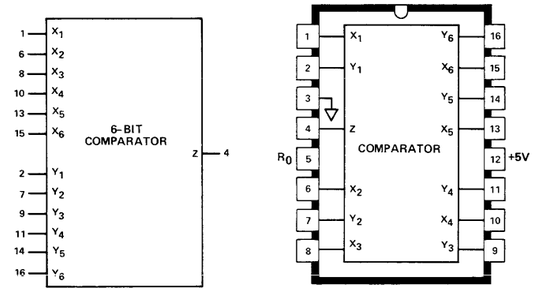
A negative pulse at the LOAD input will set the counter with the data on the input lines. A positive pulse on the CLEAR line will clear the counter. The counter is decremented for each positive-going pulse on the CLOCK DOWN line and incremented for each positive-going pulse on the CLOCK UP line.

A negative pulse occurs on the CARRY line when the outputs of the counter are all high and a negative pulse on the CLOCK UP line occurs. A negative pulse on the BORROW line occurs when the counter outputs are all low and a negative pulse on the CLOCK DOWN line occurs. When a BORROW pulse is generated the counter is set to all "ones".

1820-0239
QUAD 2-INPUT NOR GATE



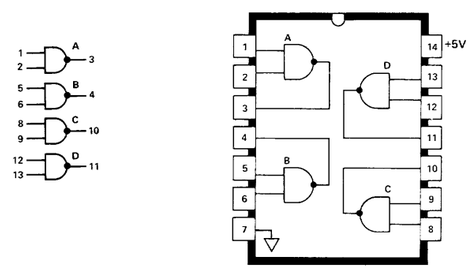
1820-0250
6-BIT COMPARATOR



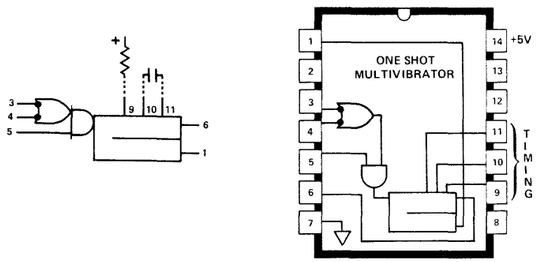
A- Z output is generated when each X input is equal to the respective Y input.

$$Z = \overline{(X_1 \otimes Y_1)} \cdot \overline{(X_2 \otimes Y_2)} \cdot \overline{(X_3 \otimes Y_3)} \cdot \overline{(X_4 \otimes Y_4)} \cdot \overline{(X_5 \otimes Y_5)} \cdot \overline{(X_6 \otimes Y_6)}$$

1820-0256
QUAD 2-INPUT NAND GATE

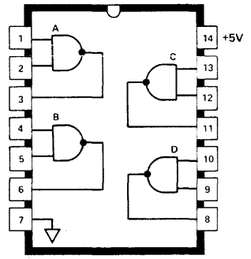


1820-0261
ONE-SHOT MULTIVIBRATOR

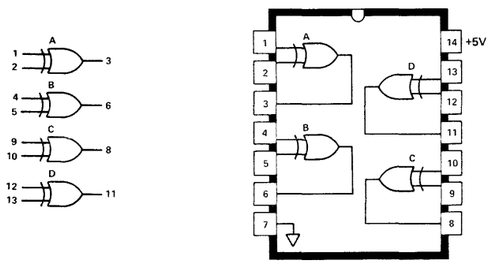


When input conditions are present an output pulse is generated. The pulse width may be determined by external timing circuits.

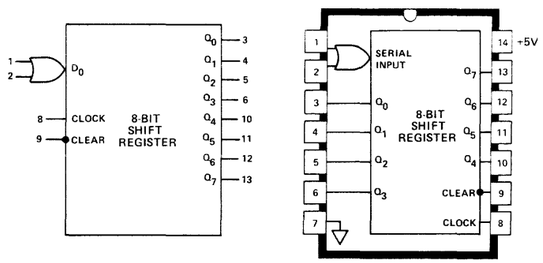
1820-0269
QUAD 2-INPUT POSITIVE NAND GATE



1820-0282
QUAD 2-INPUT EXCLUSIVE OR GATE

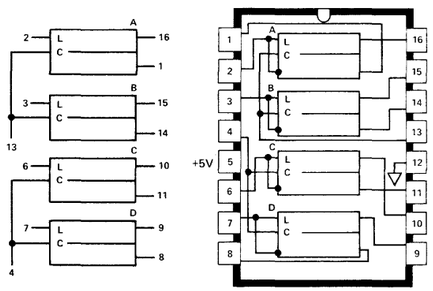


1820-0294
8-BIT SHIFT REGISTER

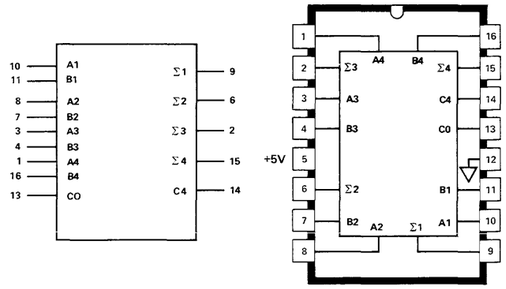


A positive clock pulse shifts the register contents one bit position and loads serial data into position Q_0. A low CLEAR signal clears the register.

1820-0301
4-BIT LATCH



1820-0305
4-BIT BINARY FULL ADDER



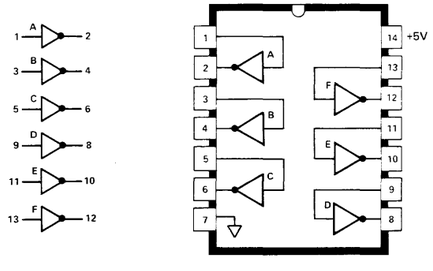
The full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit.

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	L	H	L	H	H
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	H	H	H
H	H	H	H	L	H	H	H	H	H

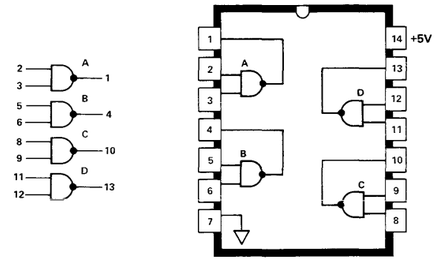
H = high level
L = low level

NOTE: Input conditions at A3, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

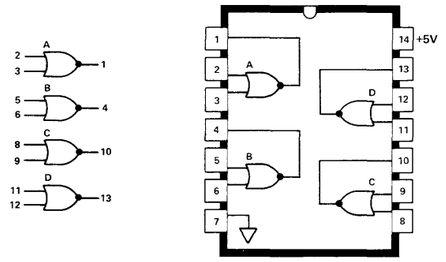
1820-0307
HEX INVERTER



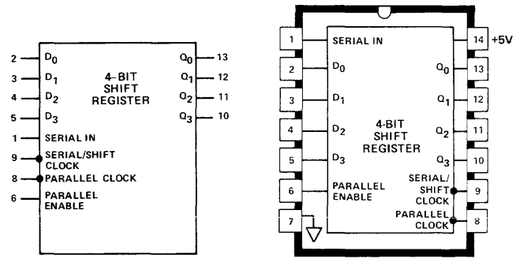
1820-0327
QUAD 2-INPUT NAND GATE



1820-0328
QUAD 2-INPUT NOR GATE

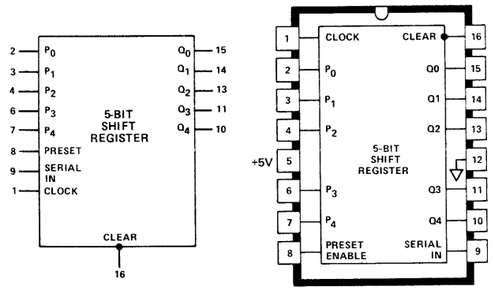


1820-0367
4-BIT SHIFT REGISTER



When the PARALLEL ENABLE line is high and a clock pulse occurs on the PARALLEL CLOCK line, data on parallel input lines (D_0 - D_3) will be stored in the register. Data is transferred to the output lines when the clock signal goes low. A clock pulse on the SERIAL SHIFT CLOCK line and a low on the PARALLEL ENABLE line will cause the contents of the register to be shifted one bit position. Data on the SERIAL IN line will be stored in the Bit 0 position. Data is transferred to the output lines when the clock goes low.

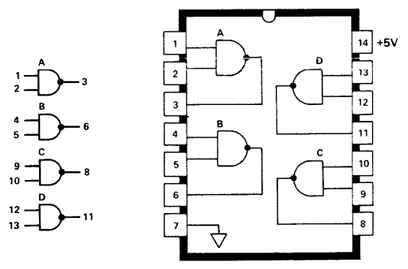
1820-0368
5-BIT SHIFT REGISTER



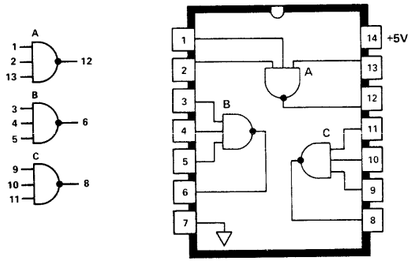
A high input signal on the PRESET line causes the register bits to be set if the corresponding P input line is high.

A clock signal loads the data present on the SERIAL IN line into the first register position and shifts the contents of the register.

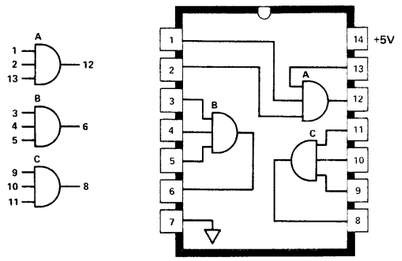
1820-0370
QUAD 2-INPUT NAND GATE



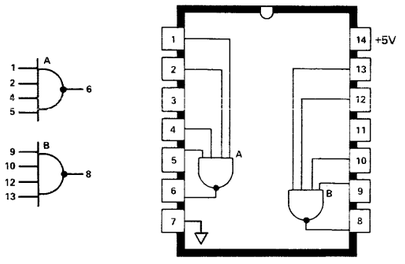
1820-0371
TRIPLE 3-INPUT NAND GATE



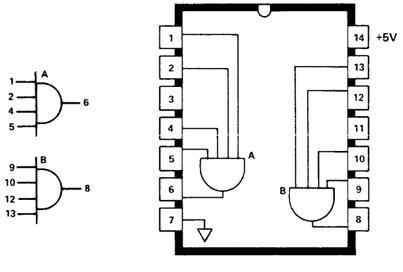
1820-0372
TRIPLE 3-INPUT AND GATE



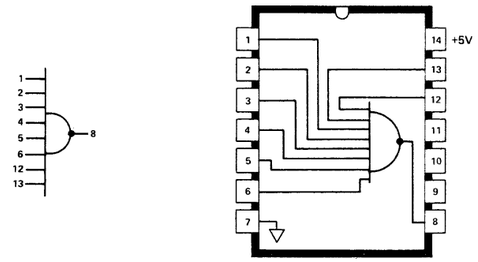
1820-0373
DUAL 4-INPUT NAND GATE



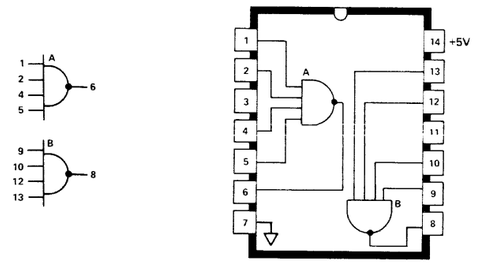
1820-0374
DUAL 4-INPUT AND GATE



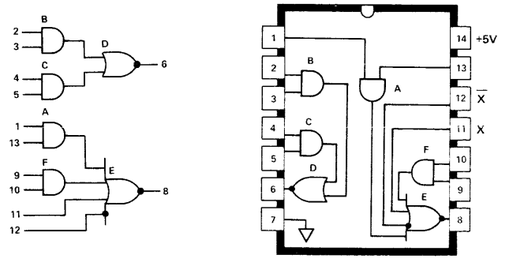
1820-0375
8-INPUT NAND GATE



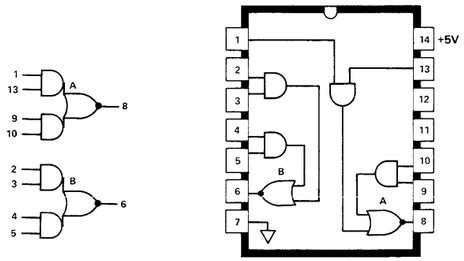
1820-0376
DUAL 4-BIT NAND GATE



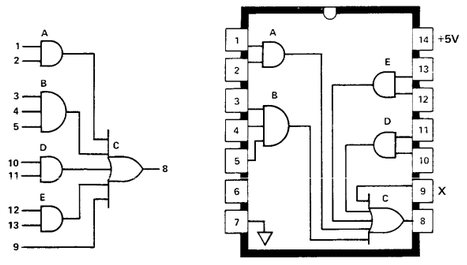
1820-0377
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE



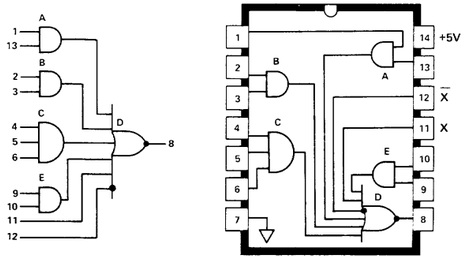
1820-0378
DUAL 2-WIDE 2-INPUT AND-NOR GATE



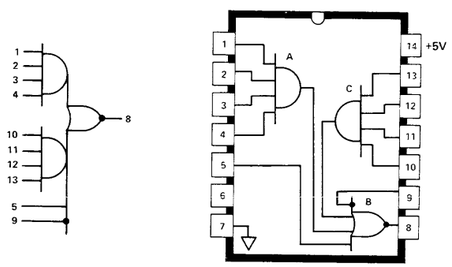
1820-0379
4-WIDE AND-OR GATE



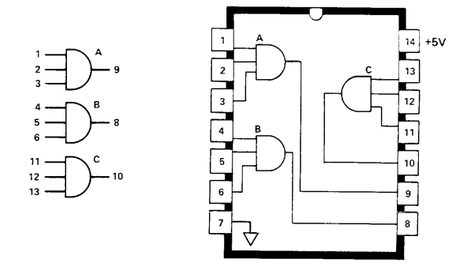
1820-0380
EXPANDABLE 4-WIDE AND-NOR GATE



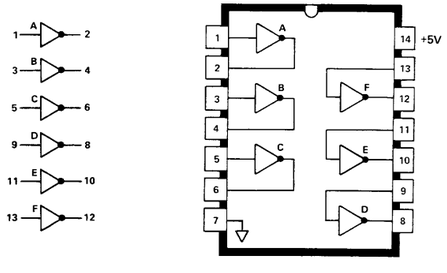
1820-0382
2-WIDE 4-INPUT AND-NOR GATE



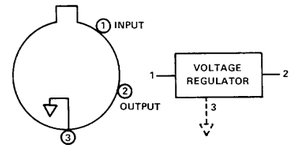
1820-0384
TRIPLE 3-INPUT AND GATE



1820-0424
HEX INVERTER

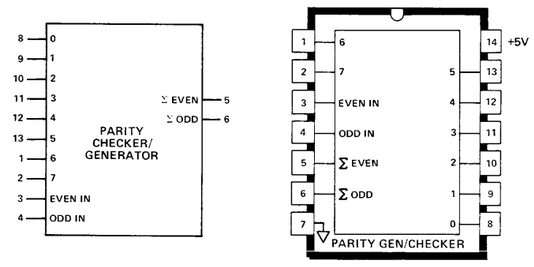


1820-0429
VOLTAGE REGULATOR



The regulator is a self-contained 5V regulator. Current limiting is included to limit the peak output current to a safe value. Thermal shutdown is also included to prevent overheating. Refer to the applicable equipment manual for specific use of the device.

1820-0435
9-BIT ODD/EVEN PARITY GENERATOR/CHECKER



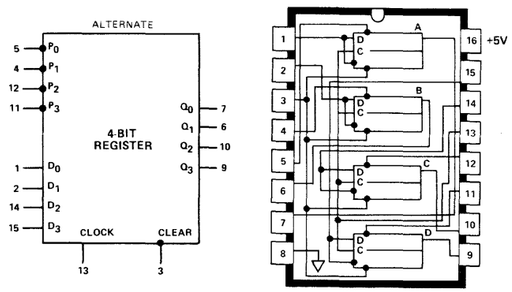
This circuit features odd/even outputs and control inputs to facilitate operation in either odd or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input.

FUNCTION TABLE

INPUTS			OUTPUTS	
Σ OF INPUTS AT 0 THRU 7	EVEN IN	ODD IN	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

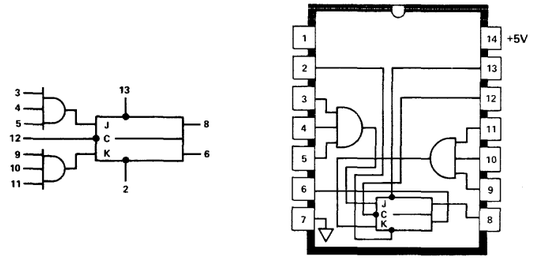
H = High Level, L = Low Level, X = Irrelevant

1820-0437
QUAD D FLIP-FLOP

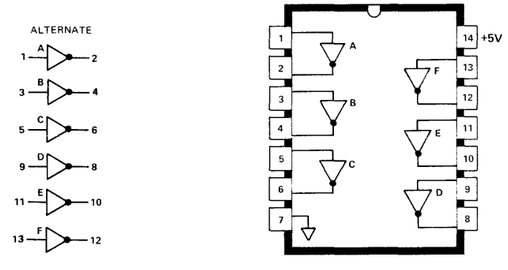


A low signal on any of the preset inputs (P_0-P_3) will cause the corresponding register bit to be set. A high on the clock line will cause the data on the D_0-D_3 lines to be stored. Data is stored on the positive going edge of the clock. A low on the CLEAR line clears the register.

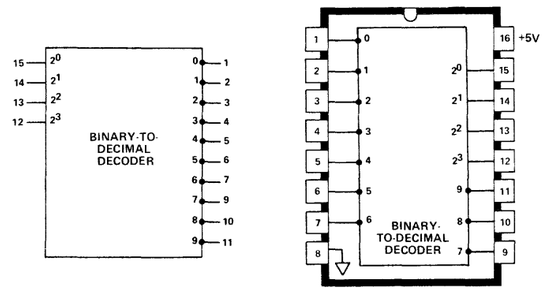
1820-0469
JK FLIP-FLOP WITH AND INPUTS



1820-0471
HEX INVERTER

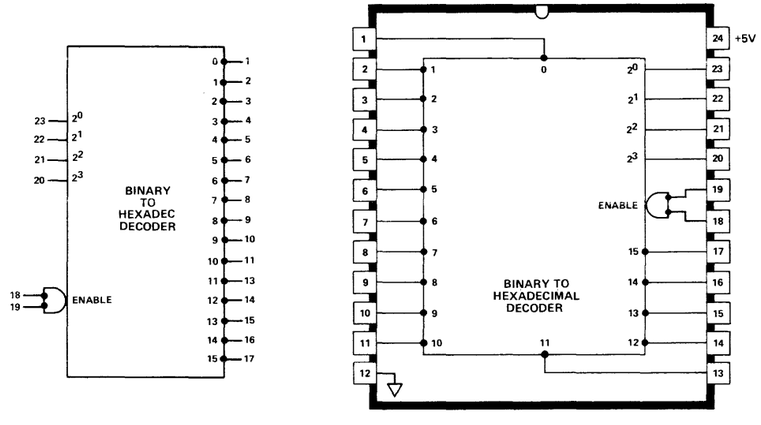


1820-0491
BINARY-TO-DECIMAL DECODER



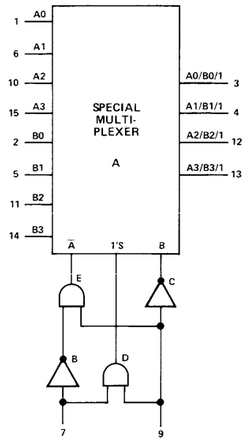
The binary input lines 2^0 through 2^3 appear directly as a decimal equivalent on the output lines 0 through 9 the selected output will be low. For binary inputs equivalent to decimal numbers greater than 9, all output lines will be high.

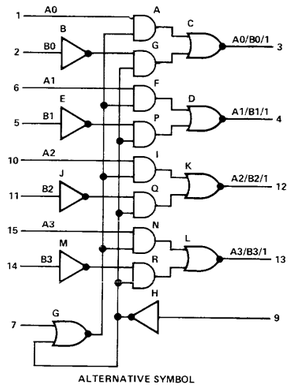
1820-0495
BINARY TO HEXADECIMAL DECODER

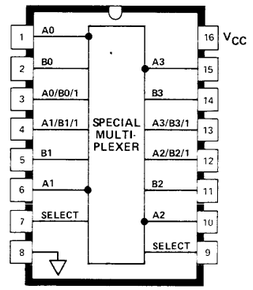


When both ENABLE inputs are low the binary coded input lines (2^0-2^3) are decoded and the equivalent output line (0-15) goes low.

1820-0506
2-INPUT 4-BIT MULTIPLEXER







This integrated circuit performs any of the following functions:

a. Passes (A0:A3) in 1's complement form.

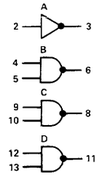
b. Passes (B0:B3) unchanged.

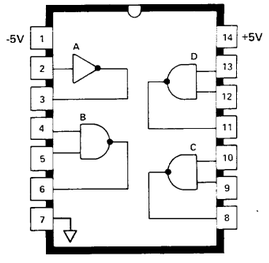
c. When like-numbered A and B inputs are connected, and with pin 7 low, the inputs are passed unchanged when pin 9 is low, or in 1's complement form when pin 9 is high.

d. Provides 1's at the outputs.

SELECT LINES		OUTPUTS			
PIN 7	PIN 9	PIN 3	PIN 4	PIN 12	PIN 13
L	H	A0	A1	A2	A3
X	L	B0	B1	B2	B3
H	H	1	1	1	1

1820-0509
TRIPLE 2-INPUT NAND-INVERT GATE

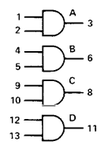


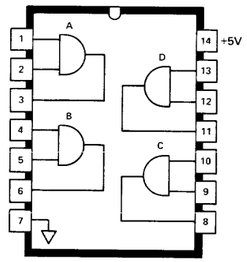


FUNCTION TABLE

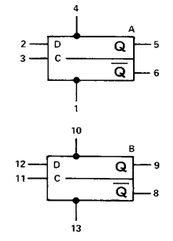
INPUTS			OUTPUTS	
Σ OF INPUTS AT 0 THRU 7	EVEN IN	ODD IN	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

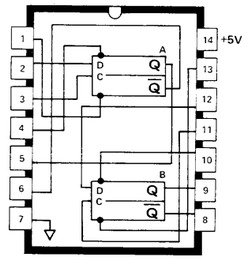
1820-0511
QUAD 2-INPUT AND GATE



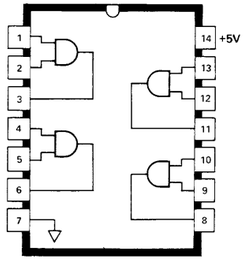


1820-0512
DUAL D FLIP-FLOP

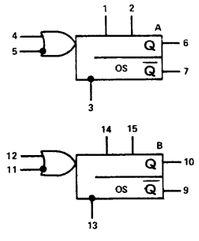


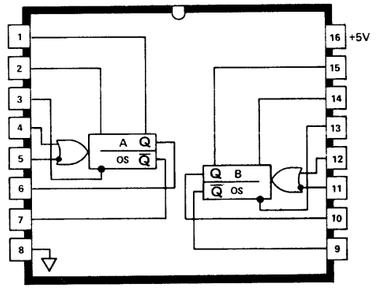


1820-0513
QUADRUPLE 2-INPUT POSITVE-AND GATES



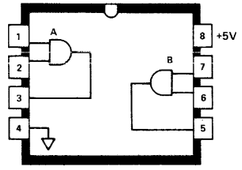
1820-0515
DUAL ONE-SHOT



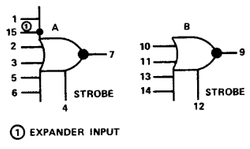


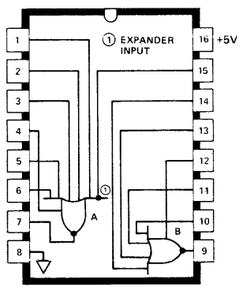
When either input condition is met the one shot will generate an output pulse. The pulse width is determined by an external RC network. The circuit may be initialized by a low clear input.

1820-0535
DUAL 2-INPUT AND GATE



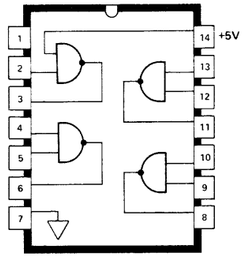
1820-0538
EXPANDABLE DUAL 4-INPUT POSITIVE NOR GATE



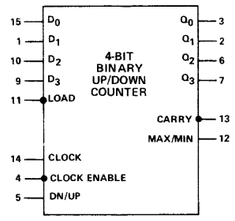


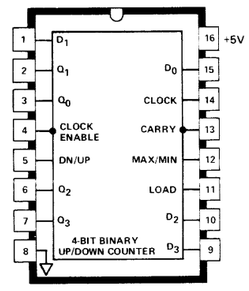
If any of the input lines are high or conditions for the expander input is present when the strobe input goes high, the output will go low.

1820-0539
QUAD 2-INPUT POSITIVE NAND GATE



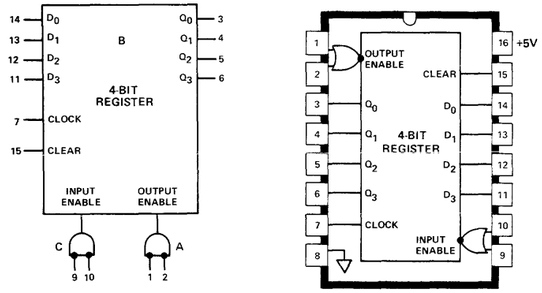
1820-0545
4-BIT BINARY UP/DOWN COUNTER





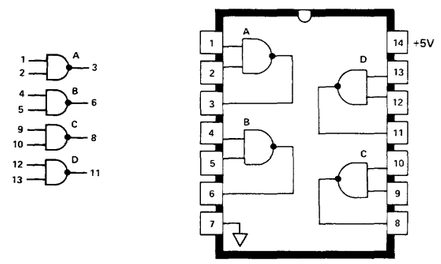
The counter is clocked by a low to high transition of the CLOCK line. The clock is effective only if the CLOCK ENABLE line is low. The CLOCK ENABLE line may only be changed while the CLOCK line is high. The direction of count is determined by the DN/UP line. If the DN/UP line is low the count is up. If the line is high the count is down. The counter may be preset with a low signal on the LOAD line. This will cause the data present on the input lines (D_0-D_3) to be stored. A low output signal is generated on the CARRY line if either a carry or borrow condition occurs. The MAX/MIN line outputs a high signal when the above conditions occur, but for a full clock cycle. This signal is used in "look-ahead carry" applications.

1820-0574
4-BIT REGISTER

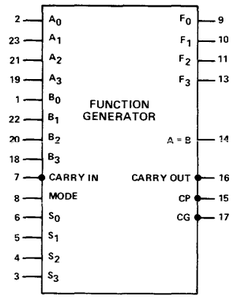


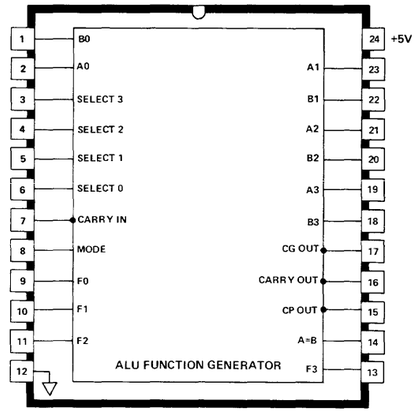
When INPUT ENABLE is true (both signal lines false) a true clock signal will cause data on the input lines to be stored. A true signal on the CLEAR line will clear the register. When OUTPUT ENABLE is true (both signal lines false) the contents of the register are gated to output lines Q_0 through Q_3.

1820-0605
QUAD 2-INPUT NAND GATE



1820-0606
ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR





The MODE line determines whether an arithmetic or logic operation will be performed (A "1" for logic function and a "0" for arithmetic function). The S lines select the function to be performed according to the table given above. If the function code LHHL is used and the A inputs are the same as the B inputs the A=B output line will be true.

The CP (Carry Propagate) and CG (Carry Generate) lines are used for fast addition operations using a "look ahead" carry function. The CP line will go false when the following conditions are met: $CP = F_0 \cdot F_1 \cdot F_2 \cdot F_3$.

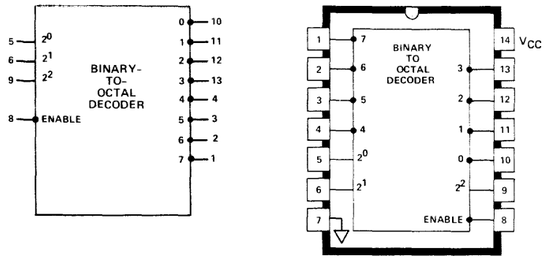
If the CARRY IN line is false and the CP condition is met, then the CARRY OUT line will also go false.

The CG line will go false if the pack addition results in a true CARRY OUT independent of the CARRY IN. The CG signal is defined as follows:

$$CG = A_3 \cdot B_3 + (A_2 \cdot B_2)(A_3 + B_3) + (A_1 \cdot B_1)(A_2 + B_2)(A_3 + B_3) + (A_0 \cdot B_0)(A_1 + B_1)(A_2 + B_2)(A_3 + B_3)$$

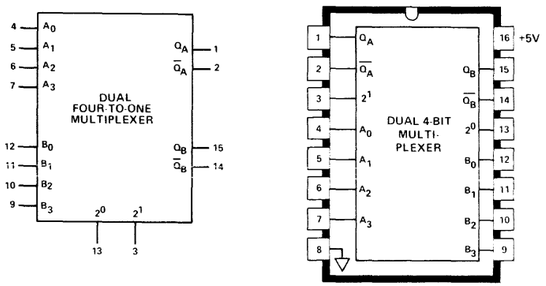
FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOGIC FUNCTIONS	ARITHMETIC OPERATIONS
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A+B}$	F = A+B
L	L	H	L	$F = \overline{A}B$	F = A+B
L	L	H	H	F = Logical 0	F = minus 1 (2's complement)
L	H	L	L	$F = \overline{AB}$	F = A plus $\overline{AB}$
L	H	L	H	$F = \overline{B}$	F = [A+B] plus $\overline{AB}$
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ minus 1
H	L	L	L	$F = \overline{A}+B$	F = A plus AB
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B
H	L	H	L	F = B	F = [A+$\overline{B}$] plus AB
H	L	H	H	F = AB	F = AB minus 1
H	H	L	L	F = Logical 1	F = A plus A 1
H	H	L	H	F = A+$\overline{B}$	F = [A+B] plus A
H	H	H	L	F = A+B	F = [A+$\overline{B}$] plus A
H	H	H	H	F = A	F = A minus 1

1820-0608
BINARY-TO-OCTAL DECODER



Binary data is decoded to octal when the ENABLE input is low. For a given input only one output line will be low.

1820-0610
DUAL 4-INPUT MULTIPLEXER



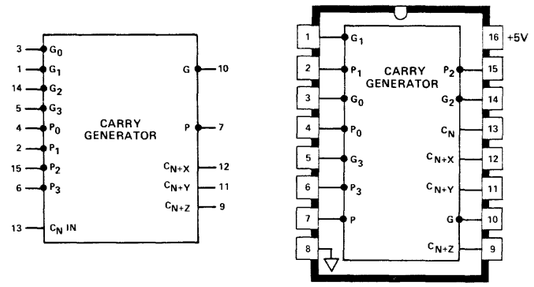
A two bit code selects one out of four bits to be propagated through the multiplexer. The dual output allows both states of the output bit to be used. A truth table of input codes and the resulting bit transfer is given.

TRUTH TABLE

SELECT LINES		INPUTS				OUTPUTS	
2^1	2^0	A_0	A_1	A_2	A_3	Q_A	Q_A
0	0	0	X	X	X	0	1
0	0	1	X	X	X	1	0
0	1	X	0	X	X	0	1
0	1	X	1	X	X	1	0
1	0	X	X	0	X	0	1
1	0	X	X	1	X	1	0
1	1	X	X	X	0	0	1
1	1	X	X	X	1	1	0

X = irrelevant

1820-0611
LOOK AHEAD CARRY GENERATOR



This circuit is used together with 1820-0606 to provide fast addition. The Carry Generator uses CP (Carry Propagate) and CG (Carry Generate) signals from the adder circuits (P_0-P_3 and G_0-G_3) as well as the Carry In signal to the first adder circuit to provide carry in signals to succeeding adder circuits (C_{N+X}, C_{N+Y}, and C_{N+Z}). This is done without waiting for the "ripple carry" to propagate from adder to adder.

The G and P signals provide inputs to additional look ahead circuits if they are used. The output signals are defined as follows:

$$C_{N+X} = G_0 + P_0\, C_N$$

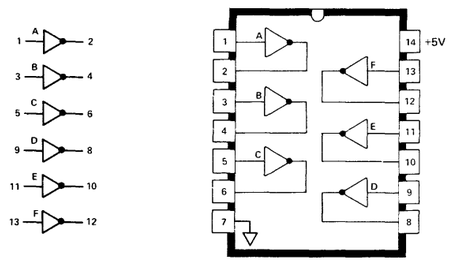
$$C_{N+Y} = G_1 + P_1\, G_0 + P_1\, P_0\, C_N$$

$$C_{N+Z} = G_2 + P_2\, G_1 + P_2\, P_1\, G_0 + P_2\, P_1\, P_0\, C_N$$

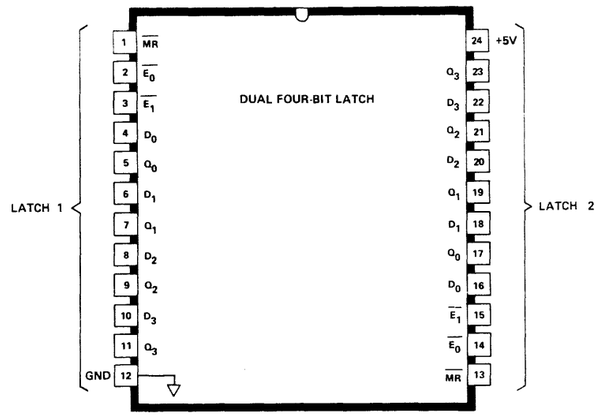
$$G = \overline{G_3 + P_3\, G_2 + P_3\, P_2\, G_1 + P_3\, P_2\, P_1\, G_0}$$

$$P = \overline{P_3\, P_2\, P_1\, P_0}$$

1820-0613
HEX INVERTER



1820-0614
DUAL FOUR-BIT LATCH



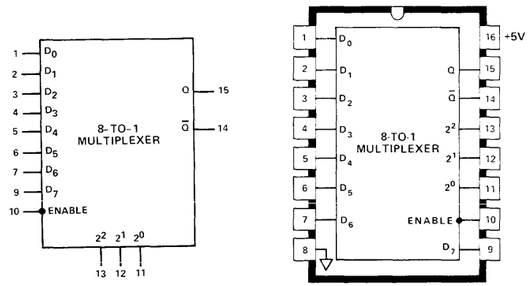
LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input.

The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the master reset input.

X = Irrelevant
L = LOW Logic Level
H = HIGH Logic Level
Q_n-1 = Previous Output State
Q_n = Present Output State

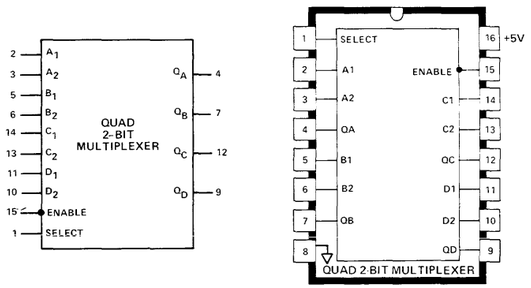
$\overline{MR}$	$\overline{E_0}$	$\overline{E_1}$	D	Q_0	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

1820-0615
8-INPUT MULTIPLEXER



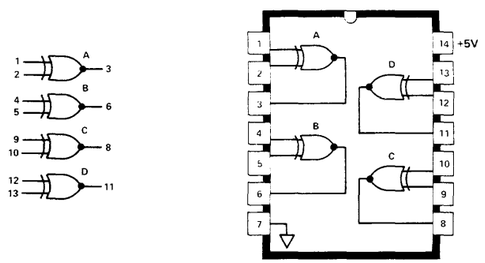
Data on one of the 8 input lines is transferred to the output line when the ENABLE line goes false. The specific input line to be transferred is determined by the three select lines.

1820-0616
QUAD 2-BIT MULTIPLEXER

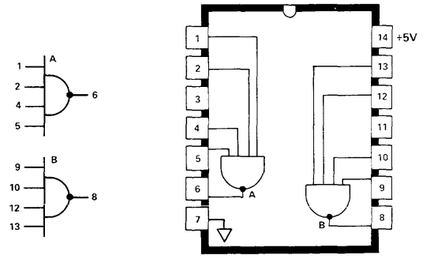


The circuit is used to select one of two four bit data words. The ENABLE must be low to allow the selection. The SELECT line is used to determine which data word will be transmitted. A "0" on the select line will transmit data word 1. A "1" on the select line will transmit data word 2.

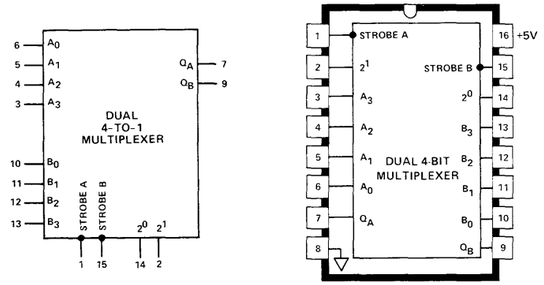
1820-0617
QUAD 2-INPUT EXCLUSIVE NOR GATE



1820-0619
DUAL 4-INPUT NAND GATE



1820-0620
DUAL 4-BIT MULTIPLEXER

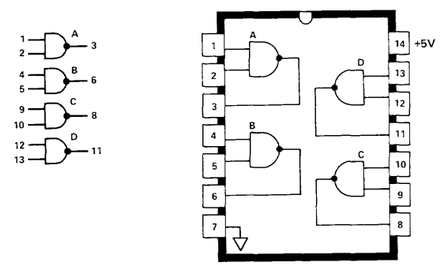


Each part of the multiplexer allows one of four bits to be placed at the output terminal. The data bits are placed on the input lines prior to the multiplexing operation. The code for the desired bit is then placed on the select lines (refer to the table above). The strobe line is used to gate the data bit onto the appropriate output line (A inputs to the Q_A terminal etc.).

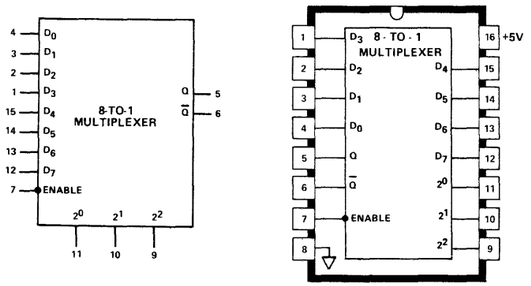
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
2^1	2^0	A0	A1	A2	A3	A	QA
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Select inputs 2^0 and 2^1 are common to both sections.
X = irrelevant

1820-0621
QUAD 2-INPUT EXCLUSIVE NOR GATE

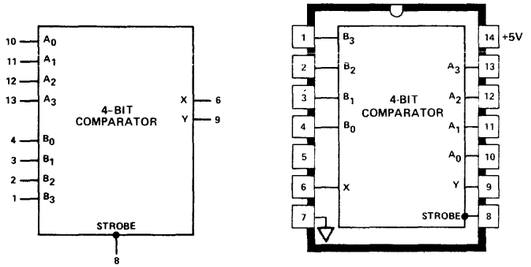


1820-0622
8-INPUT MULTIPLEXER



When the ENABLE line is false, the binary select lines 2^0 through 2^2 are used to select one of the eight inputs, lines D_0 through D_7, and apply it to the output lines Q and $\overline{Q}$.

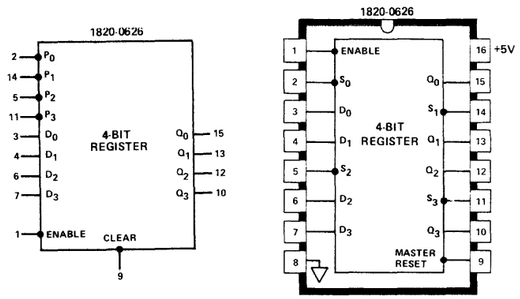
1820-0623
8-BIT COMPARATOR



When the STROBE line goes low the A bits are compared with the B bit. The result of the comparison is present on the output lines for the duration of the strobe. The output is decoded according to the truth table shown.

RELATION	X	Y
A > B	1	0
A < B	0	1
A = B	1	1

1820-0626
4-BIT REGISTER

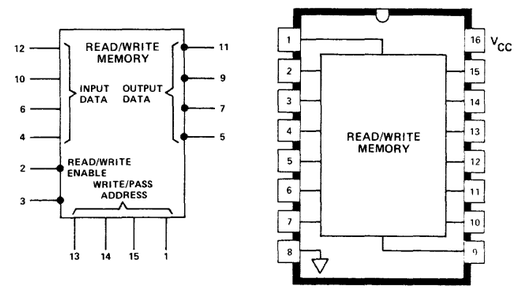


A low input on the ENABLE line allows data on the input lines to set the register. There are two modes of operation, one using the D input lines (most common) and the other using the P input lines.

If the D inputs are used the P inputs are held false. When the ENABLE line is low the register output lines will "follow" the D inputs. When the ENABLE line goes high the register will retain the last set of data inputs.

If the S inputs are used the D inputs are held true. When the ENABLE line is low, a false input on the S line will set the register bit. The register is then cleared by a low signal on the CLEAR line. The CLEAR line serves as a "master" register clear for both the D and S modes of operation.

1820-0628
READ/WRITE MEMORY



This 64-bit read/write memory, consisting of 64 flip-flops, provides 15 words of four bits each. The data outputs can be wire-"anded" to other integrated circuits of the same type to provide a memory of up to 4704 words. With output buffering, additional memory capacity is possible. Access time is typically 33 nanoseconds.

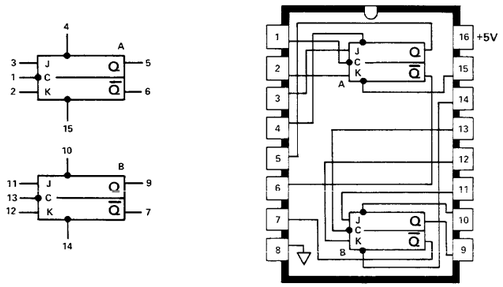
WRITE OPERATION. Information at the data inputs is written into the memory by addressing the desired location and maintaining pins 2 and 3 low. During this operation, the 1's complement of the input data is available at the output.

READ OPERATION (NON-DESTRUCTIVE). The 1's complement of the information written is obtained by addressing the desired location while holding pin 2 low.

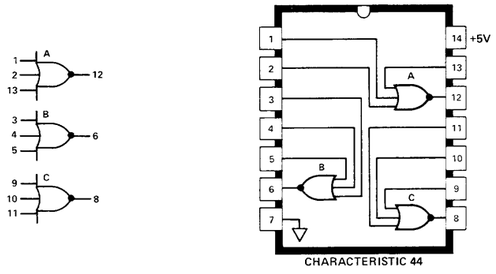
PASS-THROUGH OPERATION. With pin 3 low and pin 2 high, the 1's complement of the information at the data inputs is passed to the data outputs. No change is made to memory contents.

OPERATION	PIN 2	PIN 3	DATA OUTPUTS
Write	L	L	Complement of data inputs.
Read	L	H	Complement of addressed word.
Pass through	H	L	Complement of data inputs.
None	H	H	All high.

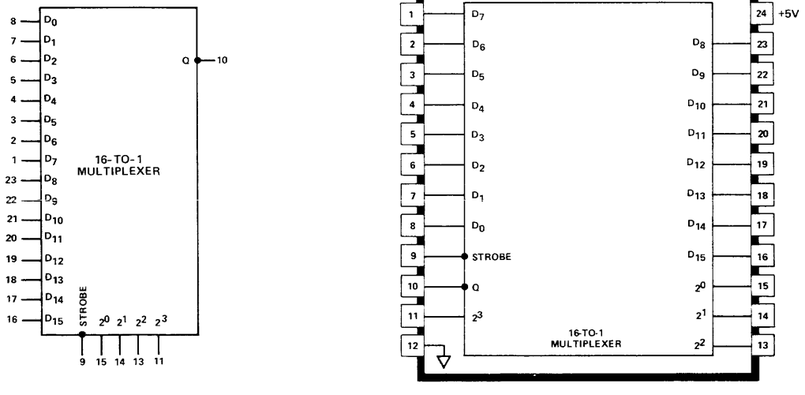
1820-0629
DUAL J-K FLIP FLOP



1820-0637
TRIPLE 3-INPUT NOR GATE

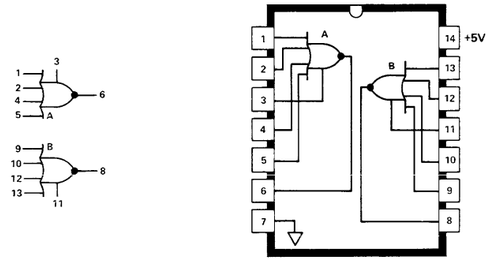


1820-0640
16-TO-1 MULTIPLEXER



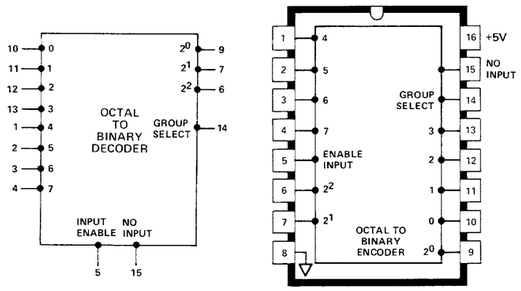
One of the 16 input data lines is selected by the select lines 2^0 - 2^3 . A low signal on the STROBE line causes the selected data line to be inverted and made available on the Q output.

1820-0655
DUAL 4-INPUT GATED NOR GATE



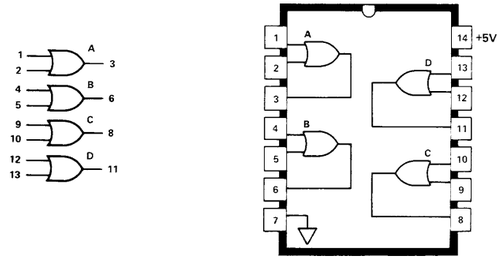
When the gate enable (strobe) is high and any gate input is high the gate output will go low.

1820-0657
OCTAL TO BINARY ENCODER

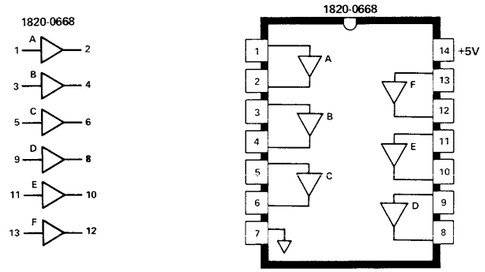


When the ENABLE INPUT line is low and one or more of the input lines 0-7 are low then the output lines making up the binary equivalent of the highest input lines will go low. When this occurs the GROUP SELECT output signals also goes low. If the INPUT ENABLE line is low and none of the input lines are selected (go low) then the NO INPUT line goes low. This allows the next stage of a decoder to be enabled.

1820-0661
QUAD 2-INPUT OR GATE

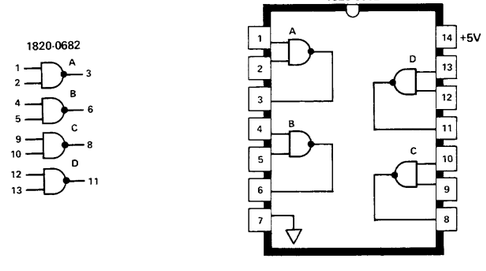


1820-0668
HEX DRIVER

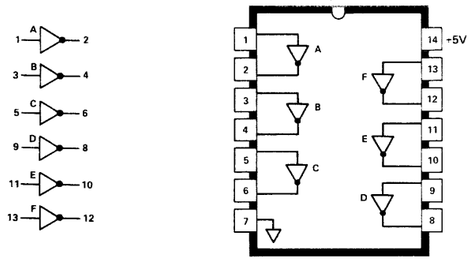


1820-0681
QUAD 2-INPUT NAND GATE

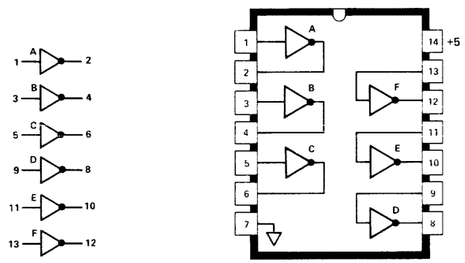
1820-0682
QUAD 2-INPUT NAND GATE



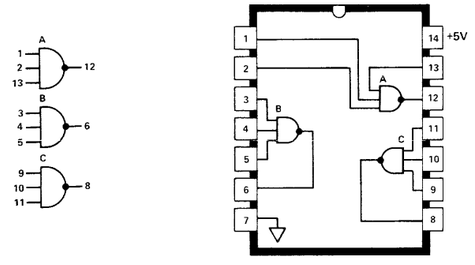
1820-0683
HEX INVERTER



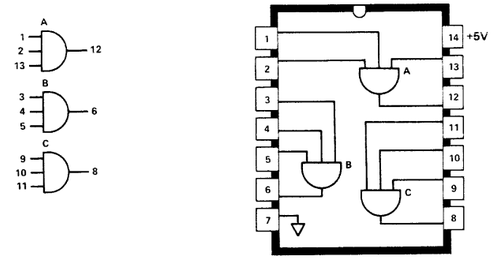
1820-0684
HEX INVERTER



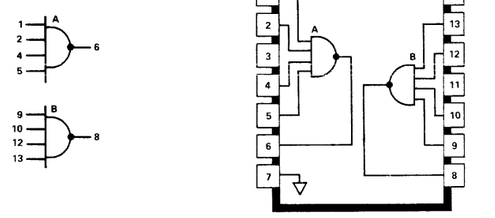
1820-0685
TRIPLE 3-INPUT NAND GATE



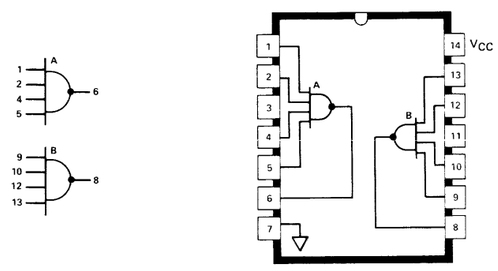
1820-0686
TRIPLE 3-INPUT AND GATE



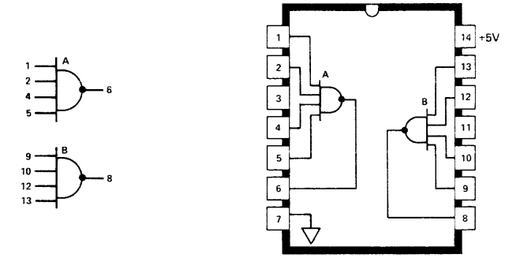
1820-0688
DUAL 4-INPUT NAND GATE



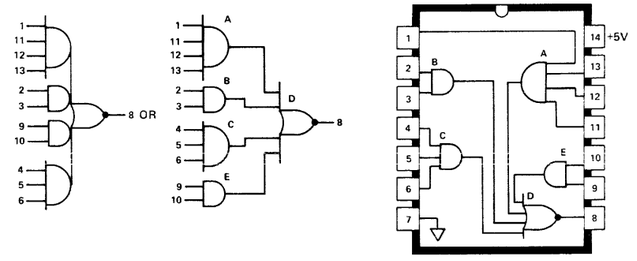
1820-0689
DUAL 4-INPUT NAND GATE



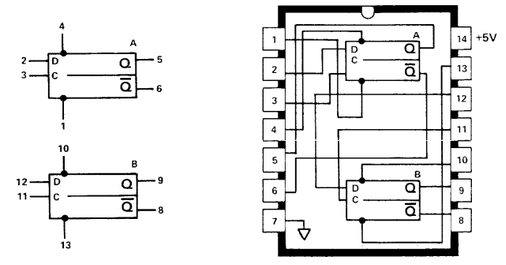
1820-0690
DUAL 4-INPUT NAND GATE



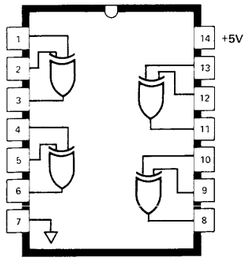
1820-0691
4-2-3-2 INPUT AND-NOR GATE



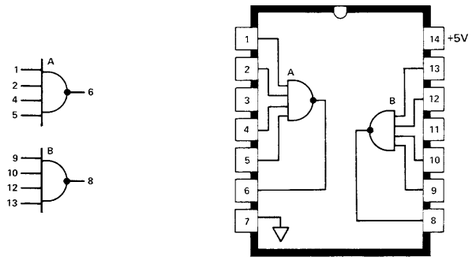
1820-0693
DUAL D FLIP-FLOP



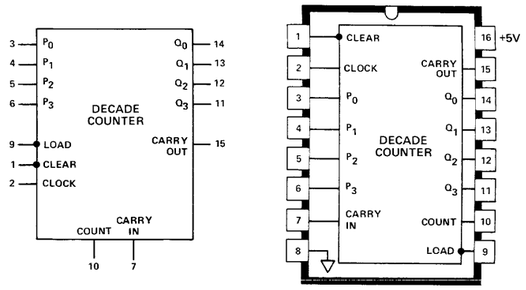
1820-0694
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE



1820-0697
DUAL 4-INPUT NAND GATE



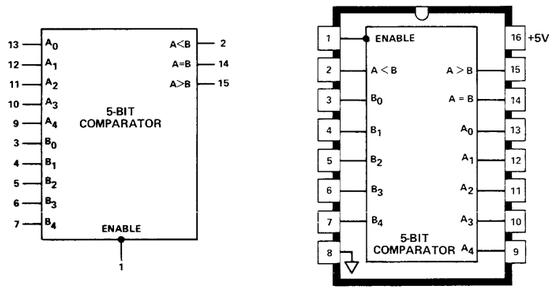
1820-0705
DECADE COUNTER



When the CLOCK input goes high and the LOAD line is low, data on the parallel input lines (P_0-P_3) is stored in the counter. When the CLOCK input goes high and both the COUNT and CARRY IN lines are high, the counter will be incremented. The new count will be present on the output lines (Q_0-Q_3) following the high-to-low transition of the clock.

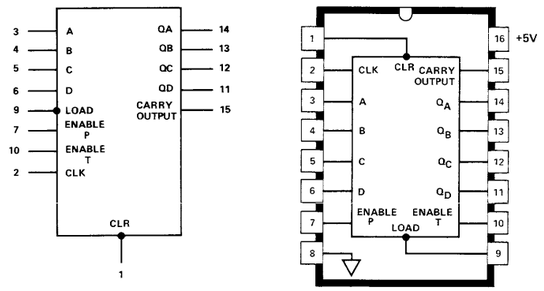
The CARRY OUT line will be high if the output lines Q_0-Q_3 equal nine (1001) and the CARRY IN line is high. The counter will be set to 0000 when the CLOCK line goes low.

1820-0706
5-BIT COMPARATOR



When the ENABLE line is low, input lines A_0 through A_4 are compared with B_0 through B_4. The appropriate output A > B, A = B, or A < B becomes true. The output remains unchanged until the ENABLE signal is removed or the input line signals changed.

1820-0713
4-BIT BINARY COUNTER

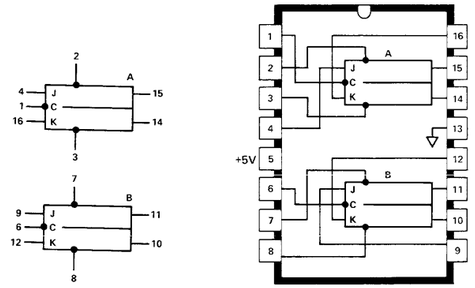


Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable inputs and internal gating. Clock inputs trigger the four flip-flops on the rising (positive-going) edge of the clock input.

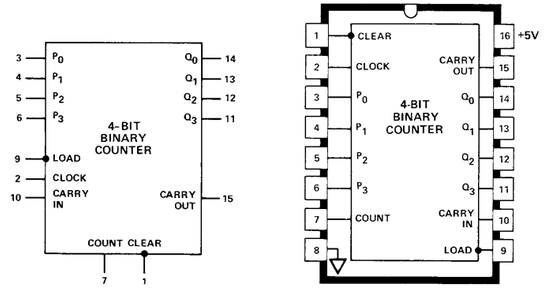
The counter is fully programmable. The outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function is synchronous and a low level at the clear input sets all four flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs.

Both count-enable inputs (P and T) must be high to count, and the T input is fed forward to enable the carry output. The carry output, being enabled, will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output.

1820-0715
DUAL JK FLIP-FLOP



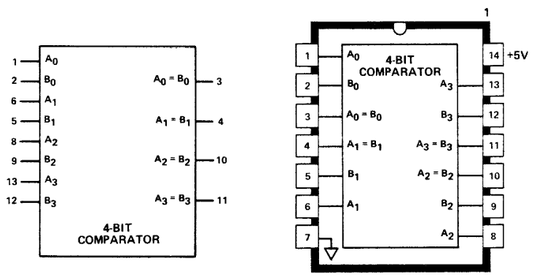
1820-0716
4-BIT BINARY COUNTER



When the CLOCK input goes high and the LOAD line is low, data on the parallel input lines (P_0-P_3) is stored in the counter. When the CLOCK input goes high and both the COUNT and CARRY IN lines are high, the counter will be incremented. The new count will be present on the output lines (Q_0-Q_3) following the high-to-low transition of the clock.

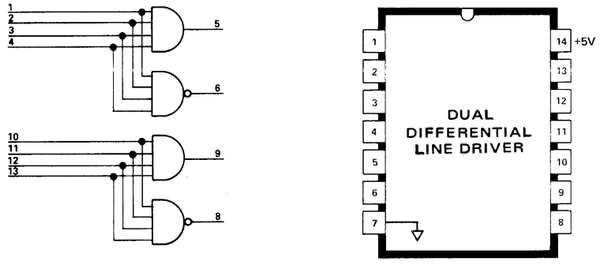
The CARRY OUT line will be high if the output lines Q_0-Q_3 are all high and the CARRY IN line is high.

1820-0719
4-BIT COMPARATOR



Four sets of two bits each are compared. If a set contains equal bits, the respective $A_i = B_i$ output line becomes true. The output line remains true until the input bit pattern is changed.

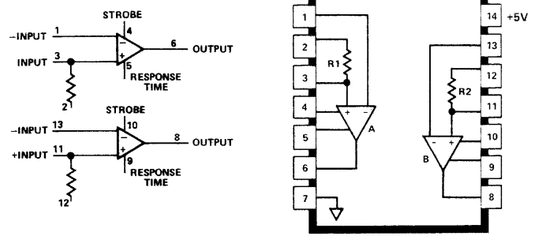
1820-0720
DUAL DIFFERENTIAL LINE DRIVER



The dual differential line driver also performs the dual four-input NAND or dual four-input AND function.

The differential outputs are balanced to drive long lengths of coax with characteristic impedances of 50 to 500 ohms.

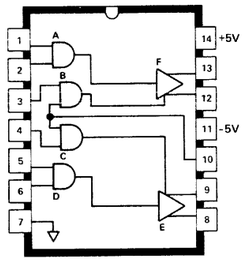
1820-0721
DUAL DIFFERENTIAL LINE RECEIVER



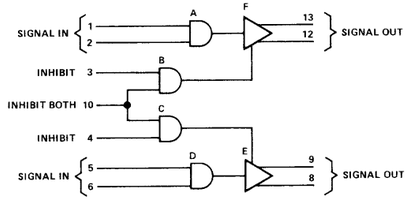
The dual differential line receiver receives inputs from twisted pair lines. The differential input rejects large common mode signals while responding to small differential signals.

Response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic 1 for both inputs open.

1820-0722
DUAL LINE DRIVER



This integrated circuit consists of two line drivers, each driving a line (such as twisted pair) and maintaining a nominal line current of 6 ma when the two wires in the line are at opposite logic levels. Output voltage levels are < 0.8 volts (low) and > 2.0 volts (high). When the line is isolated from ground the voltage across the line is at least 2.8 volts for the high-low or low-high state, and common-mode voltage (line to ground) can range from -3 volts to $+10$ volts. A low input to pin 3 or 4 allows either channel to be inhibited. A low input to pin 10 inhibits both channels.

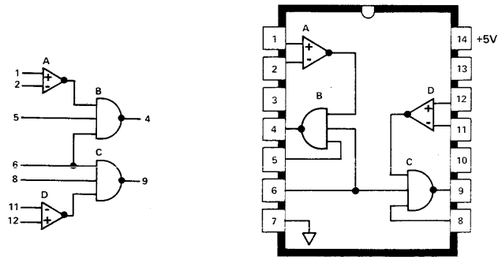


SIGNAL INPUTS		INHIBIT INPUTS		SIGNAL OUTPUTS	
PIN 1	PIN 2	PIN 3	PIN 10	PIN 13	PIN 12
X	X	L	X	H	H
X	X	X	L	H	H
L	Z	H	H	L	H
X	L	H	H	L	H
H	H	H	H	H	L

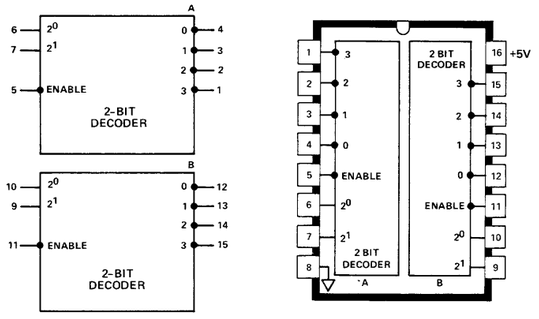
SIGNAL INPUTS		INHIBIT INPUTS		SIGNAL OUTPUTS	
PIN 5	PIN 6	PIN 4	PIN 10	PIN 9	PIN 8
X	X	L	X	H	H
X	X	X	L	H	H
L	X	H	H	L	H
X	L	H	H	L	H
H	H	H	H	H	L

X = irrelevant

1820-0723
DUAL LINE RECEIVER

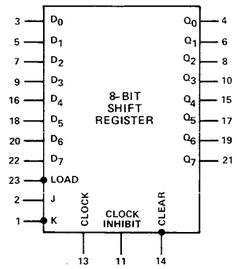


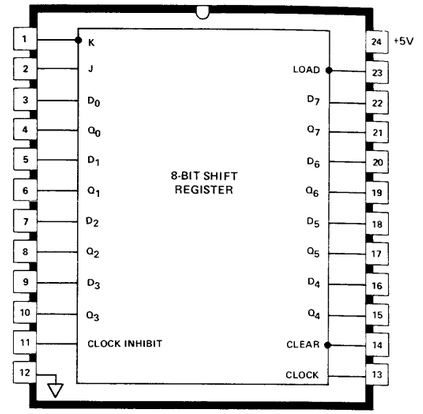
1820-0724
DUAL 2-BIT DECODER



When the ENABLE line is low the input lines 2^0-2^1 select one of four output lines 0-4. The select line goes low.

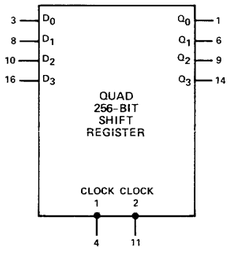
1820-0726
8-BIT SHIFT REGISTER

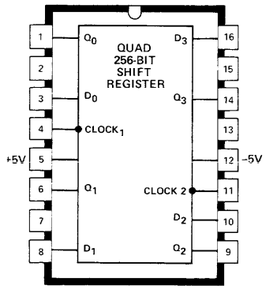




When the LOAD line is low data on the parallel input lines D_0-D_7 is loaded into the register. A low on the CLEAR line clears the register. The contents of the register are shifted one bit position (from D_0 to D_1 etc.) when the CLOCK INHIBIT line is low and a positive clock transition occurs. At this time the J and K inputs will be used to determine the next state of the D_0 bit position.

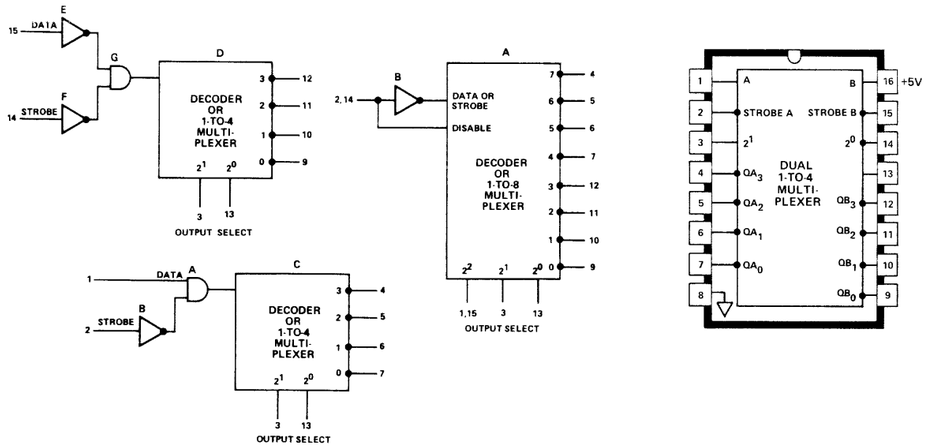
1820-0733
QUAD 256-BIT SHIFT REGISTER





Data on input lines D_0-D_3 is loaded into the register by a high to low transition of either the CLOCK1 or CLOCK2 line. The same clock signal shifts the contents of the register one position and presents the next output bits on the Q_0-Q_3 lines. The register is circular containing 256 4-bit words.

1820-0738
DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER



INPUT PINS				OUTPUT PINS			
3	13	2	1	7	6	5	4
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUT PINS				OUTPUT PINS			
3	13	14	15	9	10	11	12
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

USED AS DUAL 1-TO-4 MULTIPLEXER OR DUAL 2-BIT DECODER

INPUT PINS				OUTPUT PINS							
1,15	3	13	2,14	9	10	11	12	7	6	5	4
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

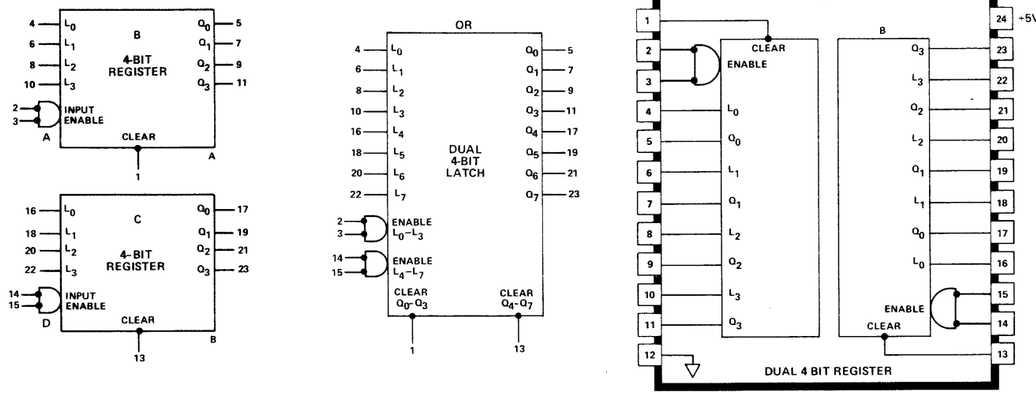
USED AS 1-TO-8 MULTIPLEXER OR 3-BIT DECODER

This integrated circuit can be used as a dual 1-to-4 multiplexer or dual 2-bit decoder. When used as a multiplexer, data supplied to pin 1 is inverted; data supplied to pin 15 is not inverted. The data and strobe inputs to pins 1 and 2 can be interchanged with a reversal of signal sense. The inputs to pins 15 and 14 also can be interchanged, with no change in signal sense. In decoder use, the output of gate A or gate G must be in the high state to enable the decoder.

By connecting pin 1 to pin 15, and pin 2 to 14, the integrated circuit may be used as a 1-to-8 multiplexer or 3-bit decoder.

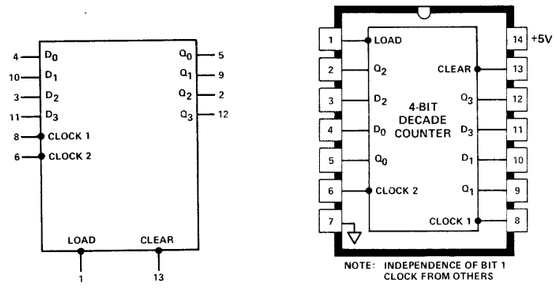
With the exception of the diagram showing physical position of pins, the diagrams above are simplified to show functional operation. An X in the tables indicates that the level is irrelevant.

1820-0742
DUAL 4-BIT LATCH



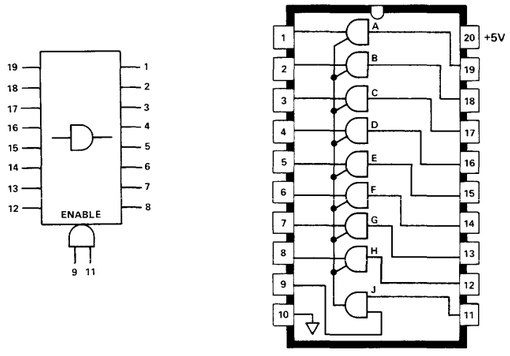
High inputs on both enable lines will cause the input data (L_0-L_3) to be stored in the register. The data is stored on the leading edge of the ENABLE signal. A low signal on the CLEAR line clears the register.

1820-0751
DECADE COUNTER

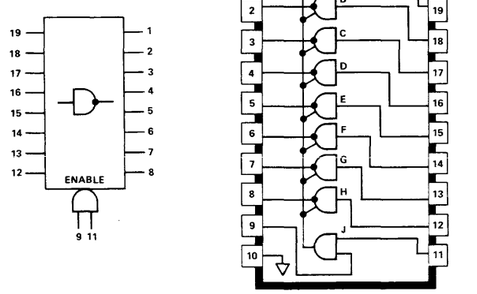


A low signal on the CLOCK1 line toggles the first bit of the counter. A low signal on the CLOCK2 line causes the remainder of the counter to be incremented (counting to 5). If the Q_0 output is used to provide the CLOCK2 input, the counter will act as a decade counter.

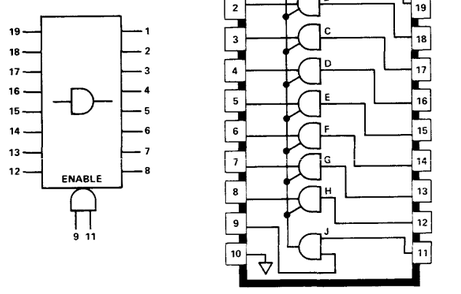
1820-0755
8-BIT DRIVER



1820-0756
8-BIT DRIVER

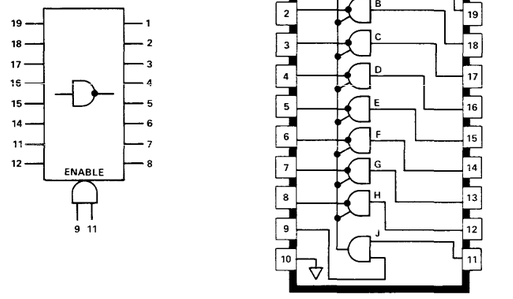


1820-0759
8-BIT RECEIVER

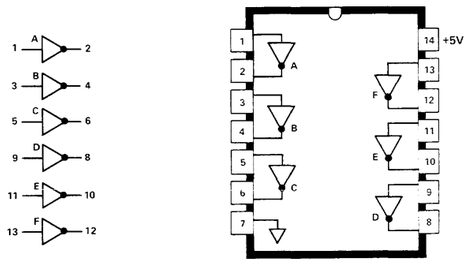


High signals on both enable lines gate the input data. The output data is inverted for 1820-0756 and 1820-0760.

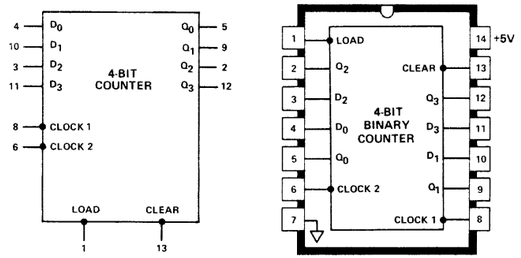
1820-0760
8-BIT RECEIVER



1820-0761
HEX INVERTER

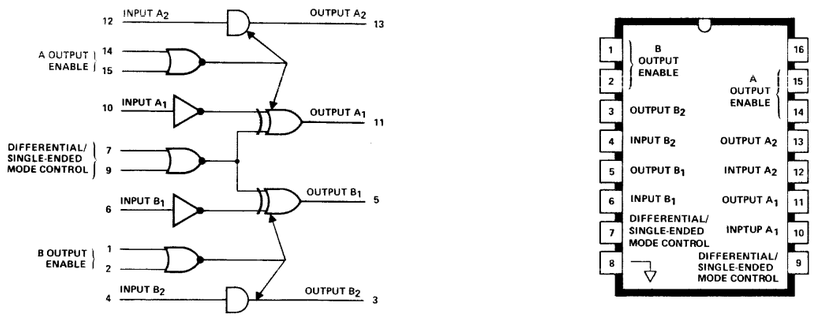


1820-0765
4-BIT COUNTER



A low signal on the LOAD line presets the counter with the data on the input lines D_0 through D_3. A low signal on the CLEAR line clears the counter. A low signal on the CLOCK1 line toggles the first bit of the counter. A low signal on the CLOCK2 line causes the remainder of the register to be incremented by one (counting to 7). If the Q_0 output is used to provide the CLOCK2 signal, the counter will act as a 4-bit binary counter.

1820-0780
QUAD TRI-LEVEL LINE DRIVER

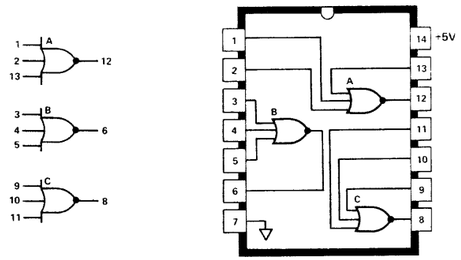


The quad tri-level line driver can be used as either a quad single-ended line driver or as a dual differential line driver.

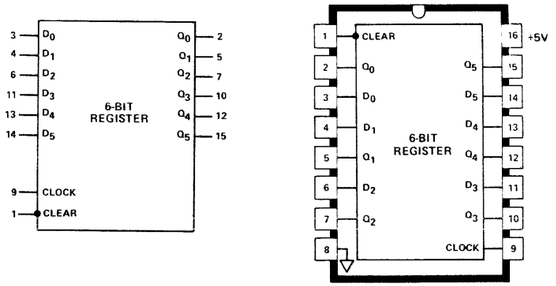
To operate as a quad single-ended line driver, a logic 0 is applied to the Output Enable pins to keep the outputs in the normal low impedance mode, and a logic 0 is applied to both Differential/Single-Ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver, logic 0 is applied to the Output Enable pins, and at least one logic 1 is applied to the Differential/Single-Ended Mode Control inputs. The inputs to the A channel are connected together and the inputs to the B channel are connected together. In this mode, signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs, and inverted on the A_1 and B_1 outputs.

1820-0782
TRIPLE 3-INPUT NOR GATE

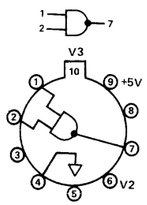


1820-0788
6-BIT REGISTER



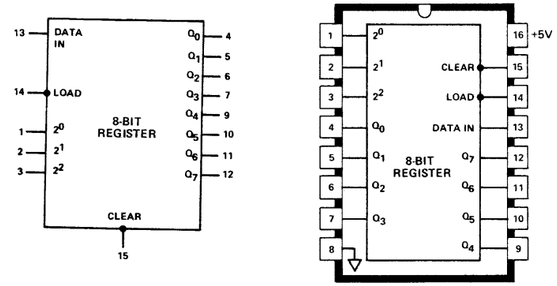
Data on the input lines is entered into the register by a positive going transition of the CLOCK line. The register is cleared by a low input on the CLEAR line.

1820-0832
TTL-TO-MOS TRANSLATOR/CLOCK DRIVER



Voltage references V2 and V3 determine the output signal level.

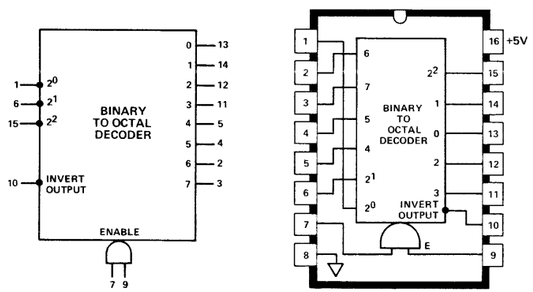
1820-0833
8-BIT REGISTER



When the LOAD line is low the information on the DATA IN line will be stored in the register position selected by the address lines (2^0-2^2). A low CLEAR signal together with a high LOAD signal will cause the register to be cleared.

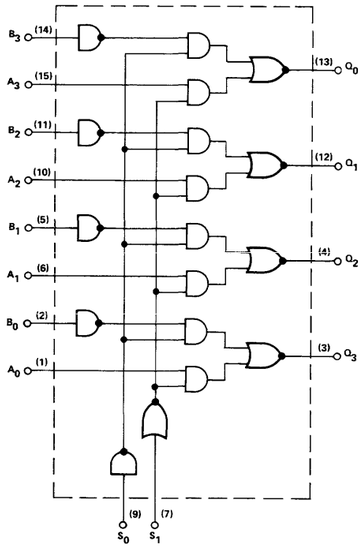
If both LOAD and CLEAR lines are low the register will act as a multiplexer, routing information on the DATA IN line to the output selected by the address lines.

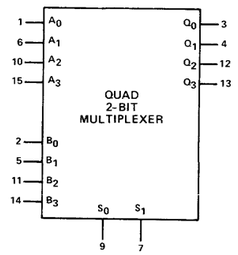
1820-0834
BINARY TO OCTAL DECODER

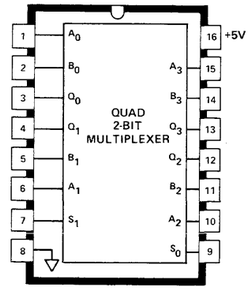


When both enable inputs are high the binary code inputs (2^0-2^2) are decoded. The equivalent octal output (0-7) will go high or low if the INVERT input is high or low respectively.

1820-0835
2-INPUT 4-BIT MULTIPLEXER



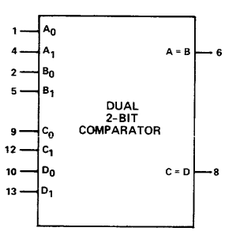




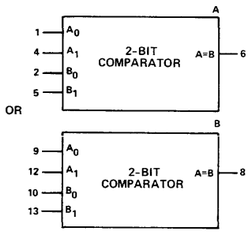
Input data (A_0-A_3 or B_0-B_3) is routed to the output lines (Q_0-Q_3) according to the table given below.

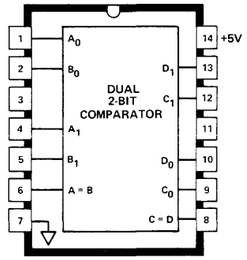
SELECT LINES		OUTPUT
S_0	S_1	Q_N (1,2,3,4)
0	0	B_N
0	1	B_N
1	0	$\overline{A}_N$
1	1	1

1820-0836
DUAL 2-BIT COMPARATOR



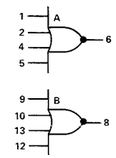
OR

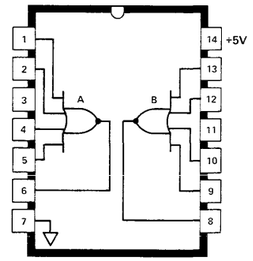




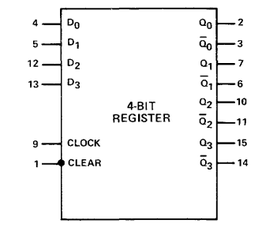
If the input bits A_0 and A_1 compare with the input bits B_0 and B_1 then the output line A= B will go high. Similarly for C and D bits.

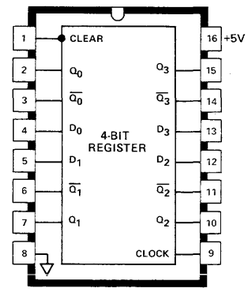
1820-0837
DUAL 4-INPUT NOR GATE





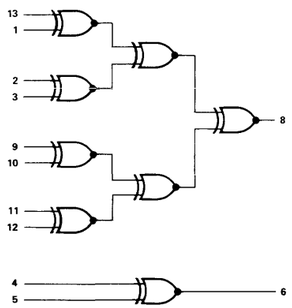
1820-0839
4-BIT REGISTER

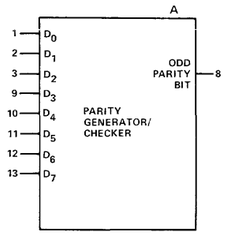


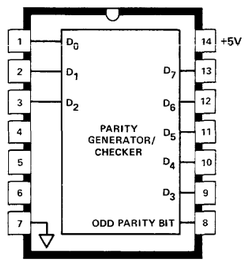


Data on the input lines (D_0-D_3) is stored at the low-to-high transition of the CLOCK line. A low signal on the CLEAR line will clear the register.

1820-0842
PARITY GENERATOR/CHECKER

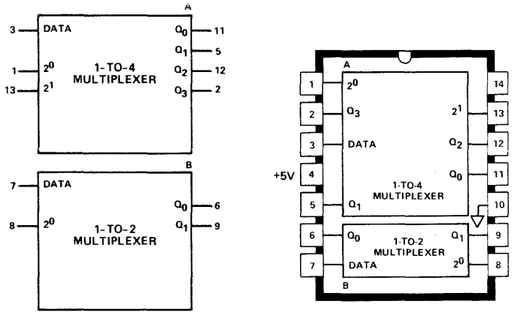






Pin 8 will be high as long as the high state is present on an even number of D inputs.

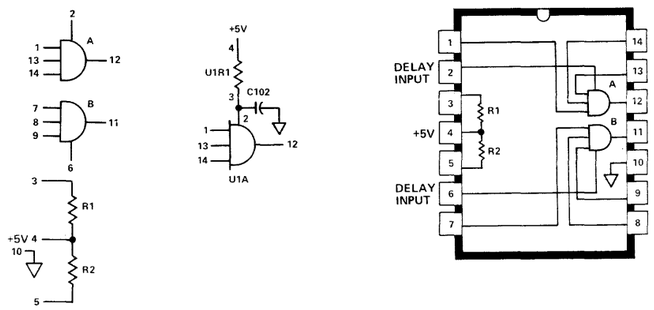
1820-0843
DUAL DATA DISTRIBUTOR



Element A multiplexes data on the DATA line to one of four output lines Q_0-Q_3. The output line is selected by the select lines 2^0 and 2^1.

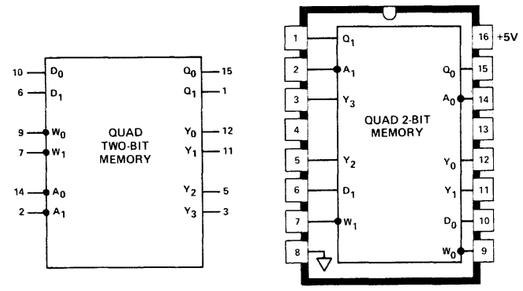
Element B multiplexes the data on the input line to one of the two output lines Q_0-Q_1. The output line is selected by the 2^0 select line.

1820-0844
DUAL 3-INPUT PULSE SHIFT/DELAY AND GATE



The outputs of the gates are delayed by an amount determined by an external RC network.

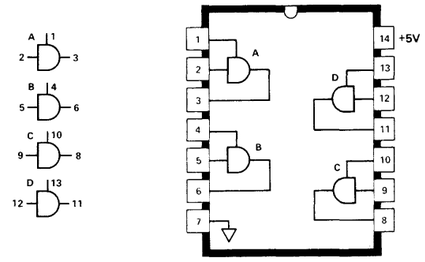
1820-0845
QUAD 2-BIT MEMORY



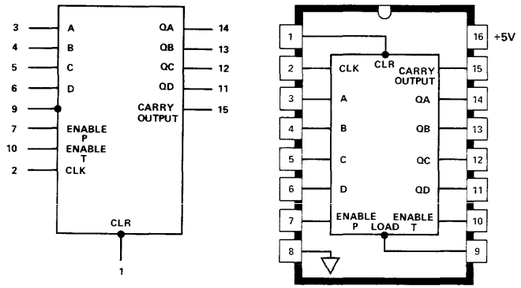
The memory is loaded by selecting the desired address with the W_0 and W_1 lines. Data present on the input lines D_0 and D_1 is then stored in the addressed word.

A word is read from memory by addressing the word with the A_0 and A_1 lines. The word content is then output to the Q_0 and Q_1 lines.

1820-0846
QUAD BUFFER



1820-0899
DECADE COUNTER

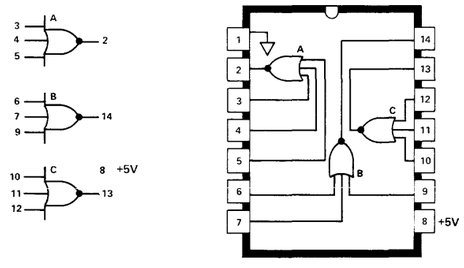


Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable inputs and internal gating. Clock inputs trigger the four flip-flops on the rising (positive-going) edge of the clock input.

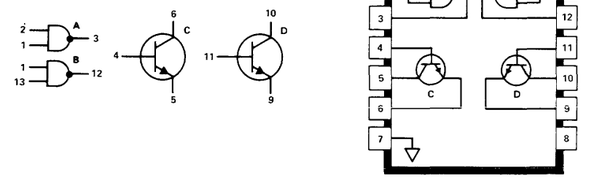
The counter is fully programmable. The outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the enable inputs.

Both count-enable inputs (P and T) must be high to count, and the T input is fed forward to enable the carry output. The carry output, being enabled, will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output.

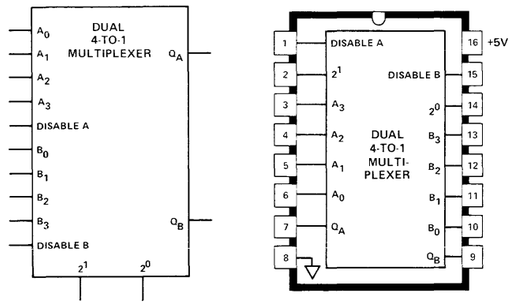
1820-0900
TRIPLE 3-INPUT NOR GATE



1820-0902
DUAL 2-INPUT DRIVER



1820-0906
DUAL 4-INPUT MULTIPLEXER

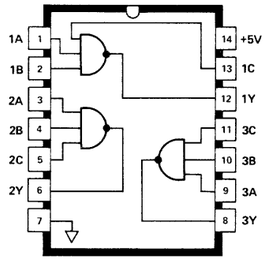


The multiplexer allows one of four bits to be placed at the output terminal. The data bits are placed on the input lines prior to the multiplexing operation. The code for the desired bit is then placed on the select lines (refer to the table above). The strobe line is used to gate the data bit onto the appropriate output line (A inputs to the Q_A terminal etc.).

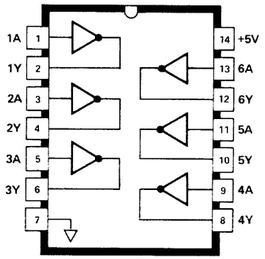
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
2^1	2^0	A0	A1	A2	A3	A	QA
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Select inputs S_0 and S_1 are common to both sections.
X = irrelevant

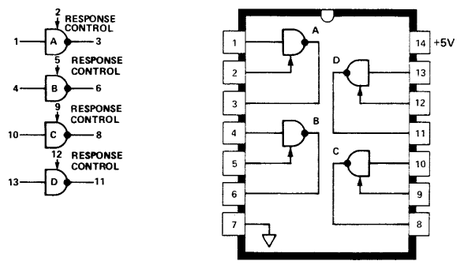
1820-0907
TRIPLE 3-INPUT POSITIVE-NAND GATE



1820-0921
HEX INVERTER

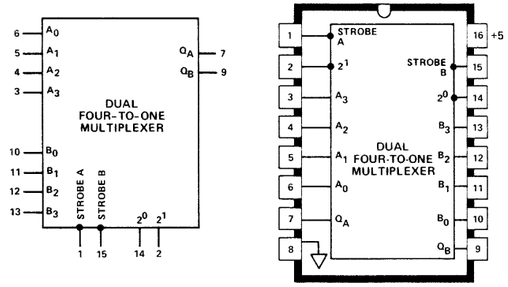


1820-0990
QUAD NAND LINE RECEIVER



Each receiver section has an external response control input that permits the connection of an external resistor to control the threshold voltage level.

1820-0998
DUAL 4-TO-1 MULTIPLEXER

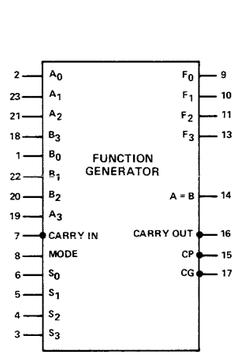


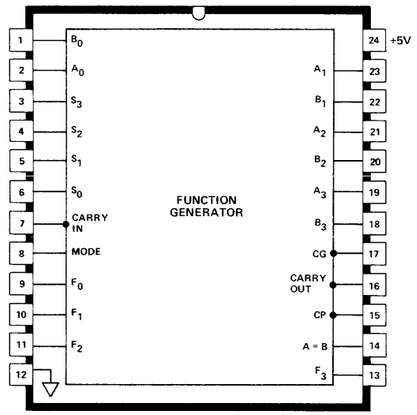
Each part of the 1820-0998 multiplexer allows one of four bits to be placed at the output terminal. The data bits are placed on the input lines prior to the multiplexing operation. The code for the desired bit is then placed on the select lines (refer to the table above). The strobe line is used to gate the data bit onto the appropriate output line (A inputs to the Q_A terminal etc.).

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
2^1	2^0	A0	A1	A2	A3	A	QA
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Select inputs S_0 and S_1 are common to both sections.
X = irrelevant

1820-0999
FUNCTION GENERATOR





The MODE line determines whether an arithmetic or logic operation will be performed (A "1" for logic function and a "0" for arithmetic function). The S lines select the function to be performed according to the table given above. If the function code LHHL is used and the A inputs are the same as the B inputs the A = B output line will be true.

The CP (Carry Propagate) and CG (Carry Generate) lines are used for the fast addition operations using a "look ahead" carry function. The CP line will go false when the following conditions are met:

$$CP = F_0 \cdot F_1 \cdot F_2 \cdot F_3$$

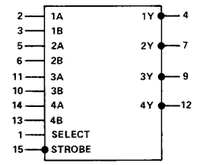
If the CARRY IN line is false and the CP condition is met, then the CARRY OUT line will also go false.

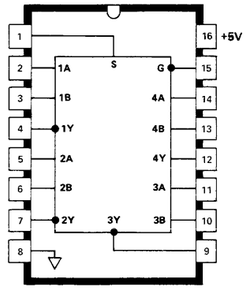
The CG line will go false if the pack addition results in a true CARRY OUT independant of the CARRY IN. The CG signal is defined as follows:

$$CG = A_3 \cdot B_3 + (A_2 \cdot B_2)(A_3 + B_3) + (A_1 \cdot B_1)(A_2 + B_2)(A_3 + B_3) + (A_0 \cdot B_0)(A_1 + B_1)(A_2 + B_2)(A_3 + B_3)$$

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOGIC FUNCTIONS	ARITHMETIC OPERATIONS
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A+B}$	F = A+B
L	L	H	L	$F = \overline{A}B$	F = A+B
L	L	H	H	F = Logical 0	F = minus 1 (2's complement)
L	H	L	L	$F = \overline{AB}$	F = A plus $\overline{AB}$
L	H	L	H	$F = \overline{B}$	F = [A+B] plus $\overline{AB}$
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ minus 1
H	L	L	L	$F = \overline{A}+B$	F = A plus AB
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B
H	L	H	L	F = B	F = [A+$\overline{B}$] plus AB
H	L	H	H	F = AB	F = AB minus 1
H	H	L	L	F = Logical 1	F = A plus A 1
H	H	L	H	$F = A+\overline{B}$	F = [A+B] plus A
H	H	H	L	F = A+B	F = [A+$\overline{B}$] plus A
H	H	H	H	F = A	F = A minus 1

1820-1015
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS



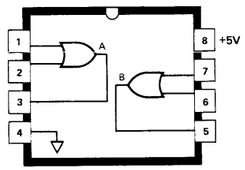


positive logic:
Low level at S selects A inputs
High level at S selects B inputs

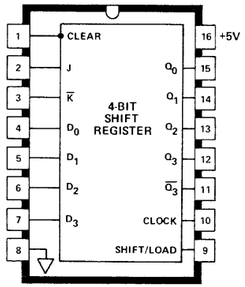
INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

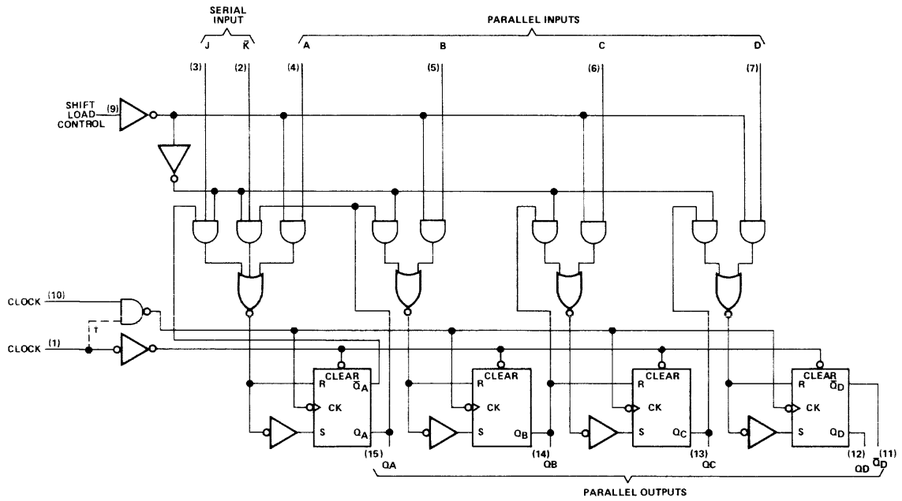
H = high level, L = low level, X = irrelevant

1820-1016
DUAL 2-INPUT OR GATE



1820-1027
4-BIT SHIFT REGISTER





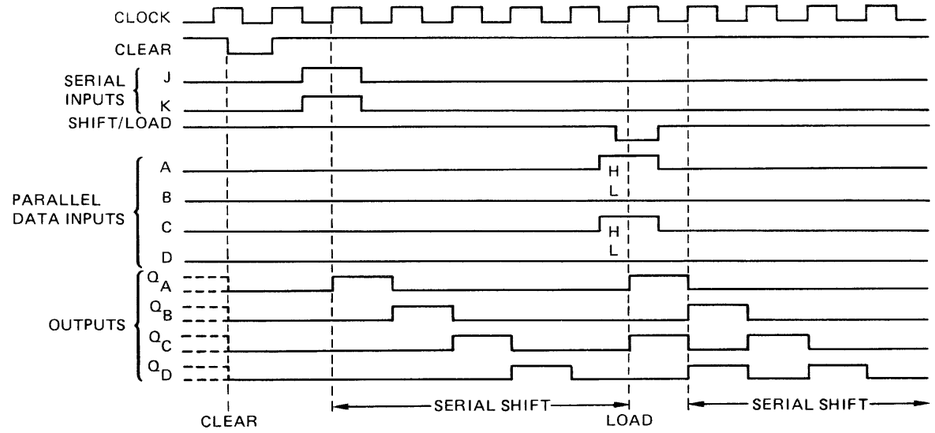
The 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel Load
Serial shift

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. Serial data flow is inhibited during loading.

Shifting is accomplished when the shift/load control input is high. Serial data is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

1820-1027
4 BIT SHIFT REGISTER (CONTINUED)

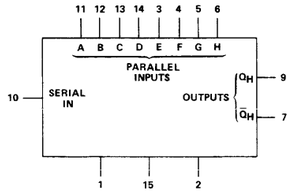


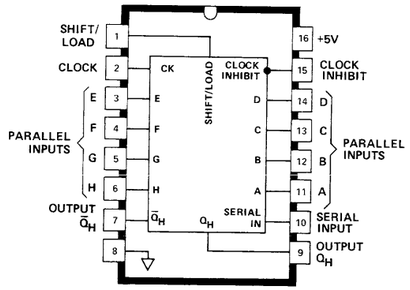
FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	K	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	d
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock

1820-1042
PARALLEL-LOAD 8-BIT SHIFT REGISTER WITH COMPLEMENTARY OUTPUT





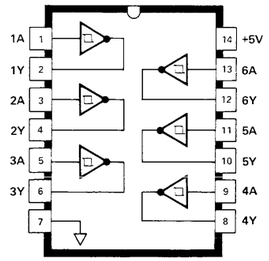
The 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift-load input. The register has gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift-load input independently of the levels of the clock, clock inhibit, or serial inputs.

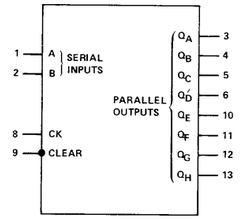
INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	X	H	Q_{AN}	Q_{Gn}
H	L	↑	L	X	L	Q_{AN}	Q_{Gn}
H	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

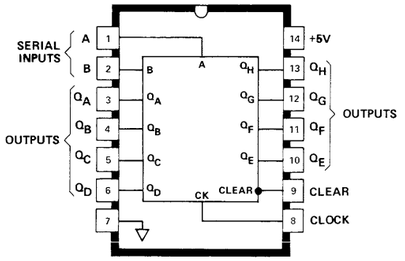
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0},Q_{B0},Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An},Q_{Gn} = the level of Q_A or Q_G, respectively, before the most-recent ↑ transition of the clock.

1820-1053
HEX SCHMITT-TRIGGER INVERTERS (PULSE SHAPING)



1820-1064
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER



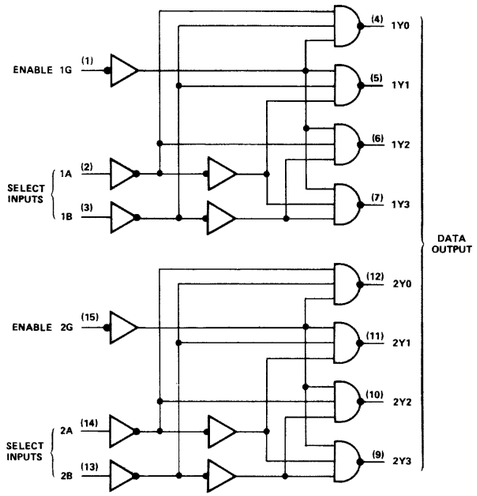


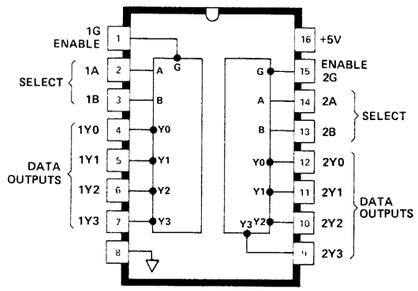
The 8-bit shift register has gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B ...	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{AO}, Q_{BO},Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

1820-1072
DECODER/MULTIPLEXER



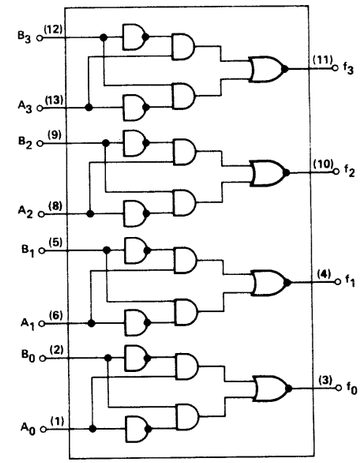


The decoder/demultiplexer consists of two individual two-line to four-line decoders in a single package.

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

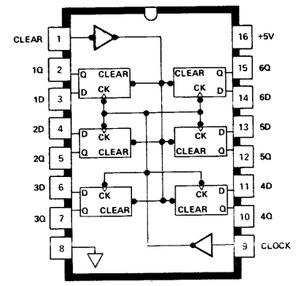
H = high level, L = low level, X = irrelevant

1820-1073
4-BIT QUAD EXCLUSIVE-NOR



+5V = (14), GND = (7), ( ) = Denotes Pin Numbers

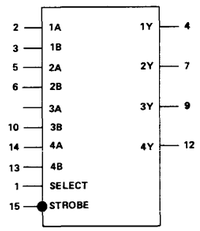
1820-1076
HEX D-TYPE FLIP-FLOPS WITH CLEAR

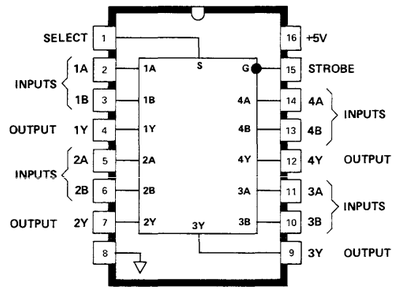


FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

1820-1077
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS



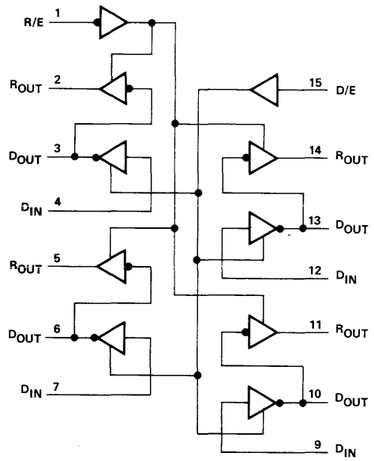


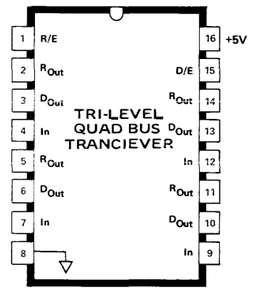
INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High Level, L = Low Level, X = Irrelevant

positive logic:
Low level at S selects A inputs
High level at S selects B inputs

1820-1081
TRI-LEVEL QUAD BUS TRANSCEIVER



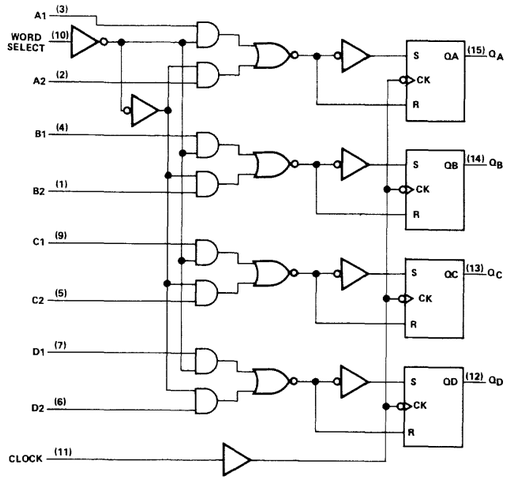


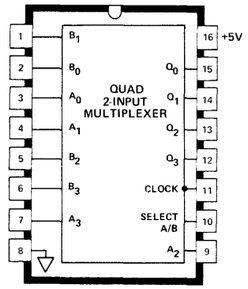
The Tri-Level Quad Bus Receiver consists of four pairs of tri-level logic elements configured as Quad Bus Drivers/ Receivers along with separate buffered receiver enable and driver enable lines.

A logic "1" on the Data Enable (D/E) inut allows input data to be transferred to the outputs of the Drivers while a logic "0" will force the outputs to a high impedance state.

The Receiver gates are enabled by a logic "0" on the Receiver Enable (R/E) pin. A logic "1" forces the Receiver outputs to a high impedance state and disables the inputs.

1820-1100
QUAD 2-INPUT MULTIPLEXER





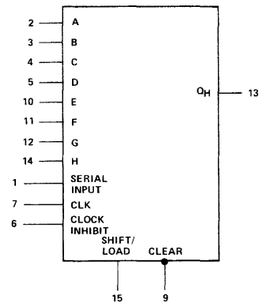
When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

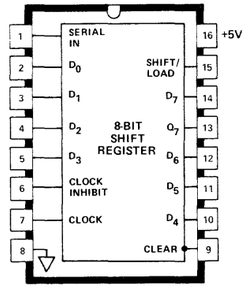
FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

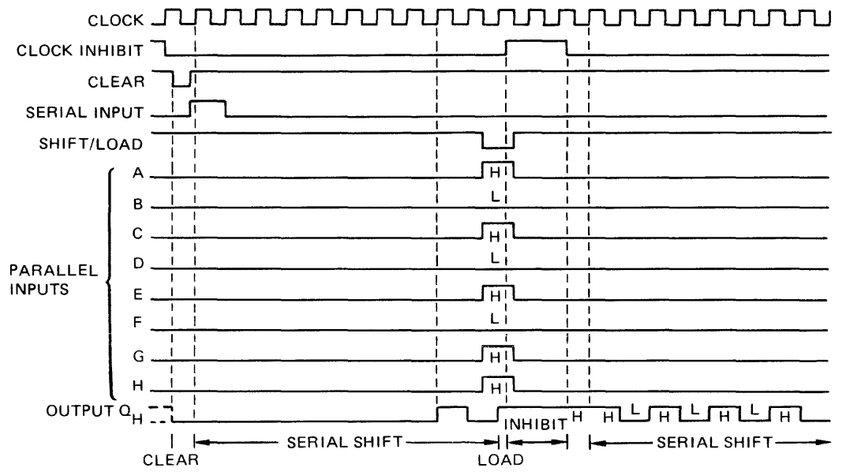
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

1820-1107
8-BIT SHIFT REGISTER





The parallel or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the register for serial shifting with each clock pulse. When low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the clock pulse. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. A direct clear input overrides all other inputs, including the clock, and sets the register to zero.

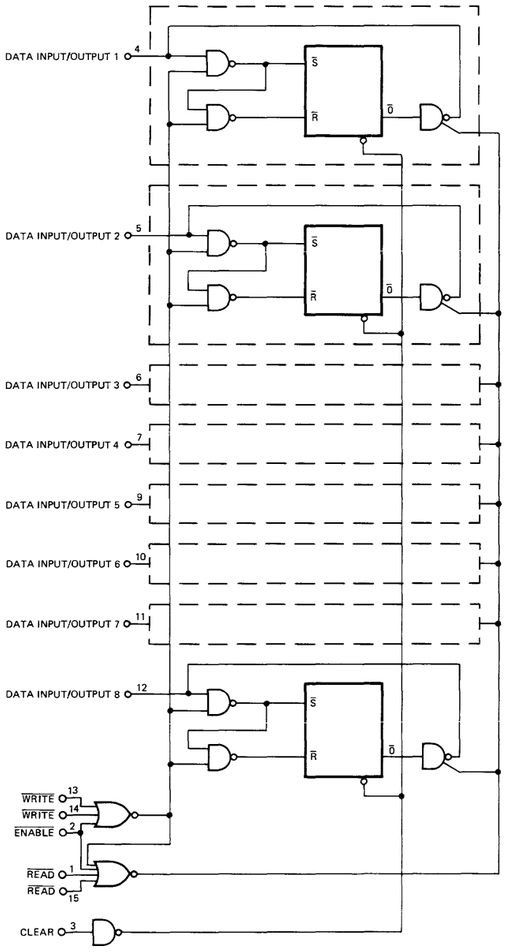


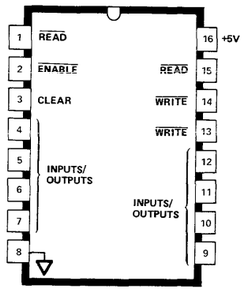
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady-state)
L = low level (steady-state)
X = Irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_3, respectively, before the most-recent ↑ transition of the clock.

1820-1113
TRI-LEVEL 8-BIT LATCH



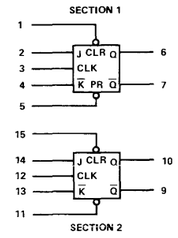


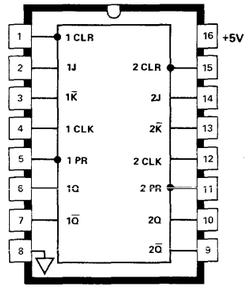
TRUTH TABLE

CLEAR	ENABLE	READ	WRITE	I/O STATE
1	0	0	x	Output = 0
x	x	1	1	Hi-z
0	0	x	0	Write
0	0	0	1	Read

Inputs and outputs are accessed on the same leads of the tri-level 8-bit latch. When in the high impedance state, the outputs and inputs are disabled and no information can be entered. When the outputs are active, the gating associated with each latch prevents information from being entered. Outputs are disabled while information is entered.

1820-1116
DUAL J-K POSITIVE EDGE TRIGGERED FLIP-FLOP

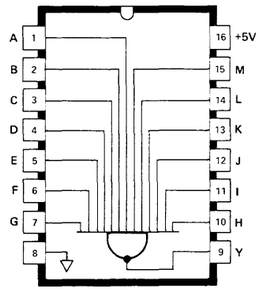




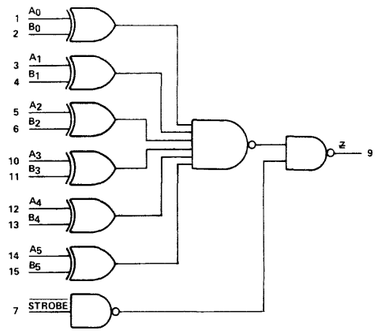
FUNCTION TABLE

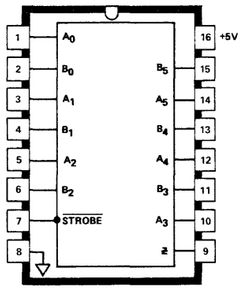
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	Q_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	Q_0

1820-1130
13-INPUT POSITIVE-NAND GATE



1820-1131
6-BIT COMPARATOR

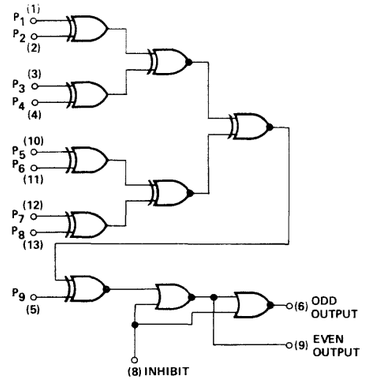


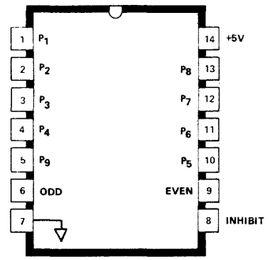


The comparator determines equality or non-equality between two 6-bit words. A strobe over-ride, when a logic 1, will force the output to a logical 1.

CONDITION	$\overline{\text{STROBE}}$ S	Z
A = B, A ≠ B	1	1
A = B	0	0
A ≠ B	0	0

1820-1140
9-BIT PARITY GENERATOR AND CHECKER





LOGIC EQUATIONS:

$$\text{ODD OUTPUT} = P_1 * P_2 * P_3 * P_4 * P_5 * P_6 * P_7 * P_8 * P_9$$

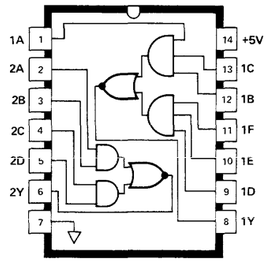
$$\text{EVEN OUTPUT} = \overline{P_1 * P_2 * P_3 * P_4 * P_5 * P_6 * P_7 * P_8 * P_9}$$

The 9-Input Parity Generator/Parity Checker is used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs. (A logic 1 on the INHIBIT input forces both outputs to a logic 0.)

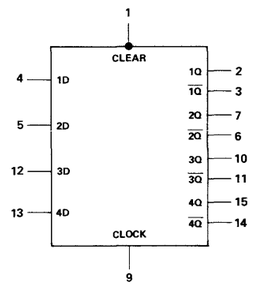
When used as a Parity Generator, the generator supplies a parity bit which is transmitted together with the data word.

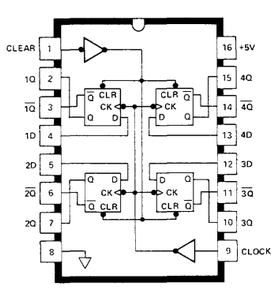
At the receiving end, the device acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

1820-1158
2 WIDE 2-INPUT AND 3-INPUT AND-OR-INVERT GATES



1820-1191
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

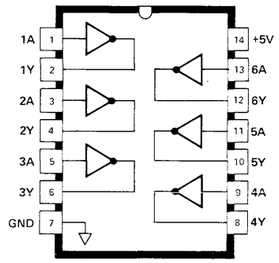




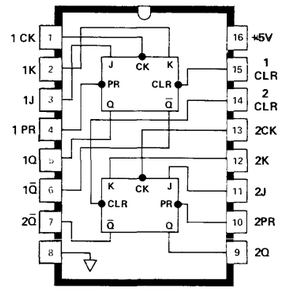
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}\uparrow$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

H = high logic level (steady state)
L = low logic level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established

1820-1199
HEX INVERTER



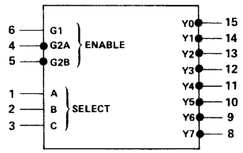
1820-1212
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

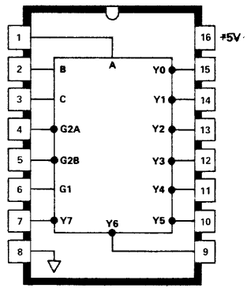


INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state), L = low level (steady state),
X = irrelevant, ↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

1820-1216
DECODER/DEMULTIPLEXER

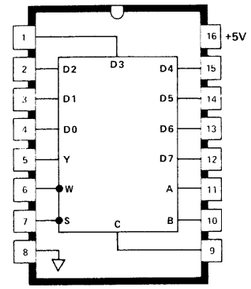


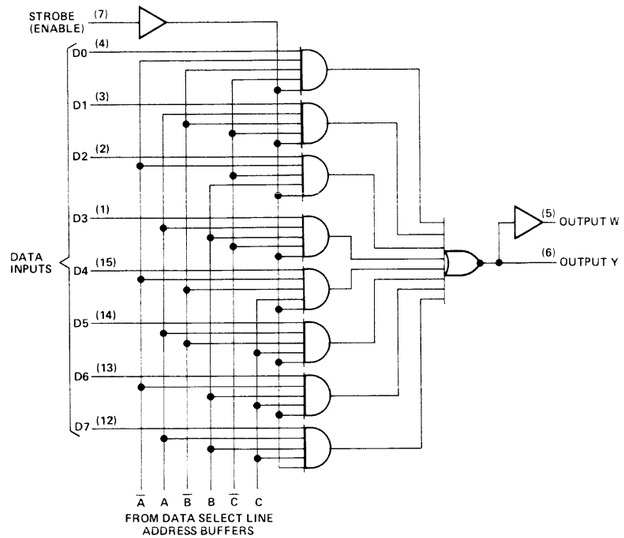


INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

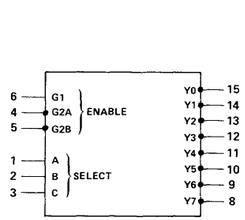
1820-1217
8-INPUT MULTIPLEXER WITH COMPLEMENTARY OUTPUTS

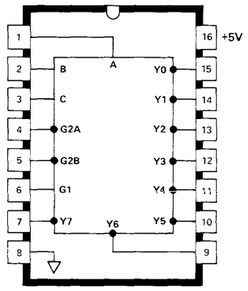




INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

1820-1240
DECODER/DEMULTIPLEXER

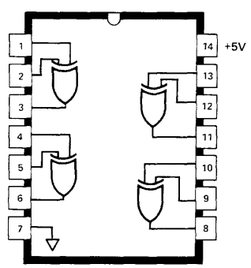




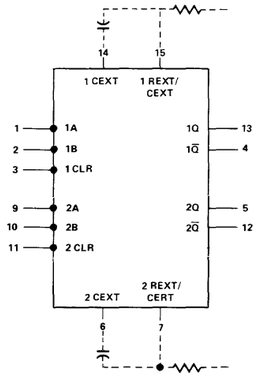
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

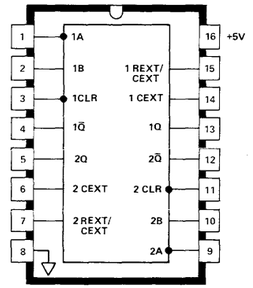
*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

1820-1250
QUAD 2-INPUT EXCLUSIVE OR GATE



1820-1260
DUAL MULTIVIBRATOR





Each multivibrator features a negative transition triggered input and a positive transition triggered input. Either input can be used as an inhibit input.

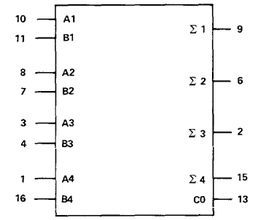
Output pulse width is determined by external component values. Approx. pulse width = 0.7 X RC.

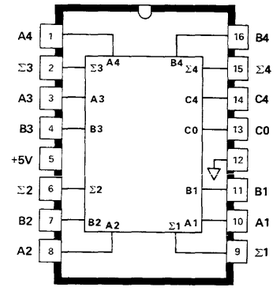
FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
Also see description and switching characteristics				

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high level pulse
⎎ = one low level pulse
X = irrelevant

1820-1261
4-BIT BINARY FULL ADDER

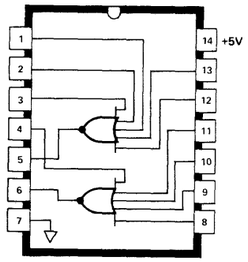




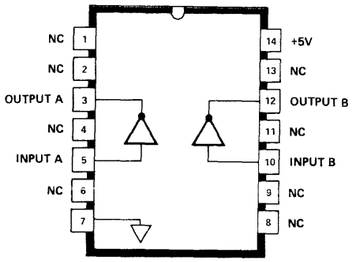
INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level
NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

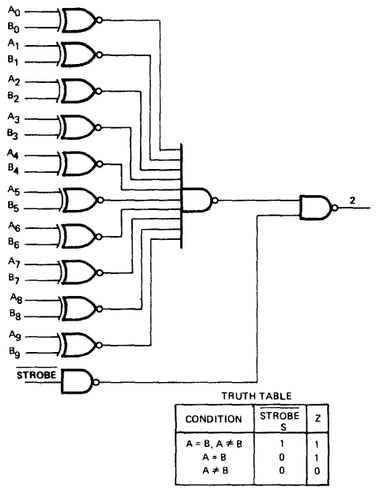
1820-1275
DUAL 5-INPUT POSITIVE-NOR GATES



1820-1288
DUAL CLOCK DRIVER



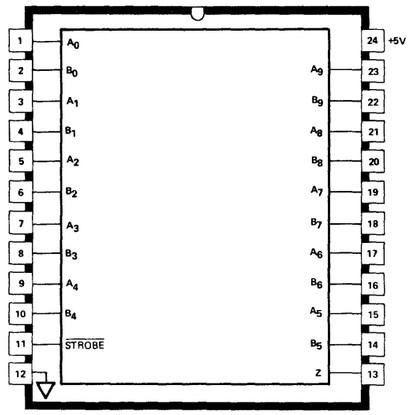
1820-1293
10-BIT COMPARATOR



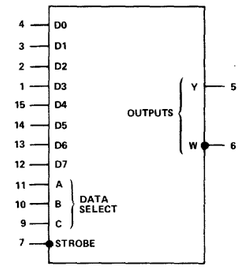
TRUTH TABLE

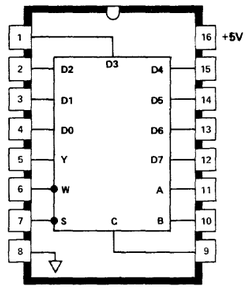
CONDITION	STROBE S	Z
A = B, A ≠ B	1	1
A = B	0	1
A ≠ B	0	0

A = A_0 thru A_9
B = B_0 thru B_9



1820-1302
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



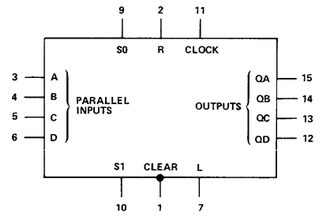


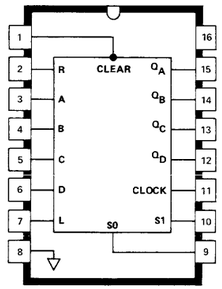
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

The data selector/multiplexer contains full binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

1820-1304
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER





The register has four distinct modes of operation.

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

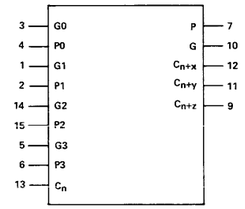
INPUTS										OUTPUTS			
	MODE			SERIAL		PARALLEL							
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

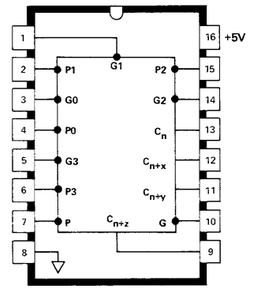
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, Q_D, respectively, before the most recent ↑ transition of the clock.

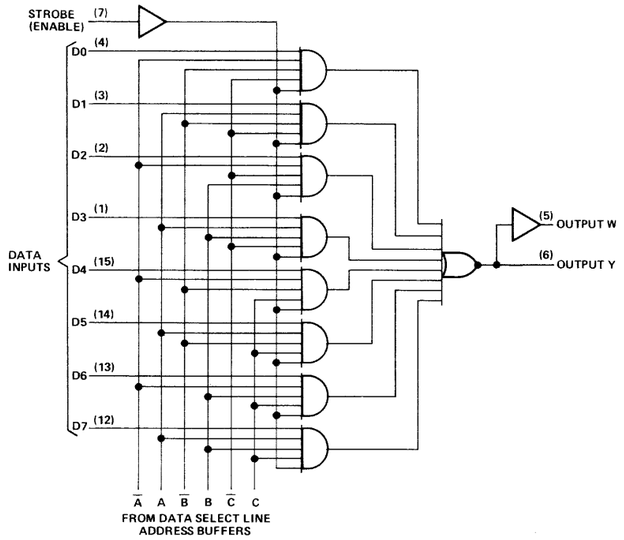
1820-1305
LOOK-AHEAD CARRY GENERATOR

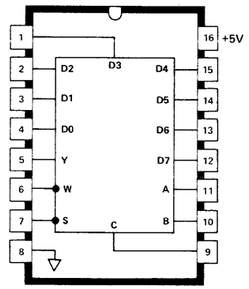




DESIGNATION	PIN NOS.	FUNCTION
G0,G1,G2,G3	3,1,14,5	ACTIVE-LOW CARRY GENERATE INPUTS
P0,P1,P2,P3	4,2,15,6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y} C_{n+z}	12,11,9	CARRY OUTPUTS
G	10	ACTIVE-LOW CARRY GENERATE OUTPUT
P	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
+5V	16	SUPPLY VOLTAGE
GND	8	GROUND

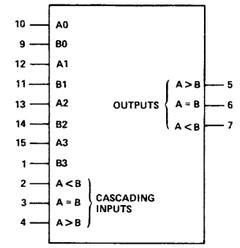
1820-1319
8-INPUT MULTIPLEXER WITH COMPLEMENTARY OUTPUTS

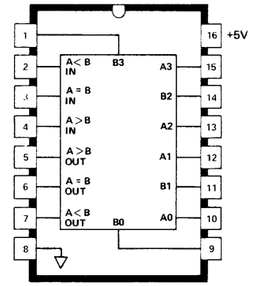




INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

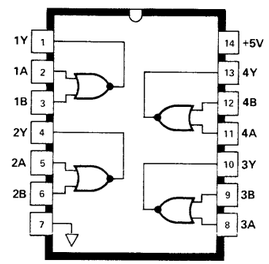
1820-1321
4-BIT MAGNITUDE COMPARATOR





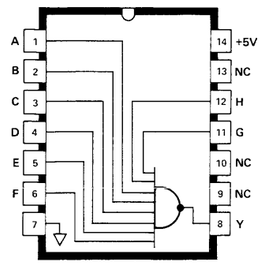
COMPARING UNITS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

1820-1322
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

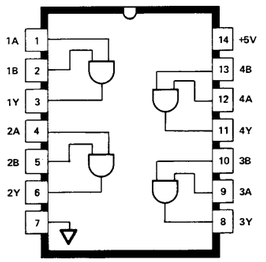


positive logic
$Y = \overline{A + B}$

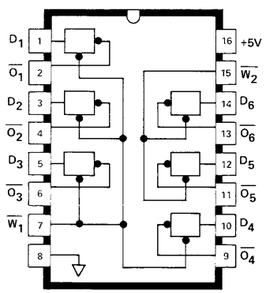
1820-1323
8-INPUT POSITIVE-NAND GATE



1820-1367
QUAD 2-INPUT AND GATE

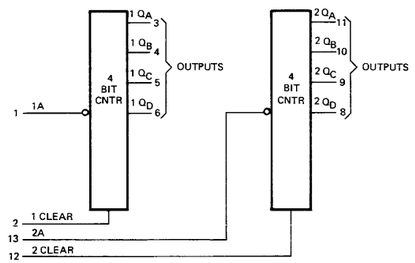


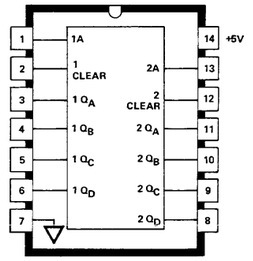
1820-1395
6-BIT LATCH



This integrated circuit contains six high speed latches organized as an independent 4 bit and 2 bit latches. The latches act as high speed inverters when the "write" input is "low".

1820-1464
DUAL 4-BIT BINARY COUNTER

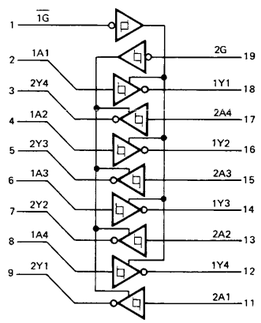


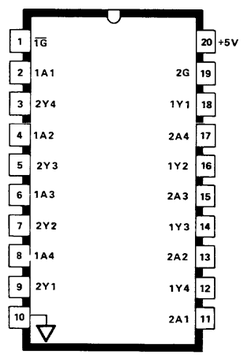


COUNT SEQUENCE (EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

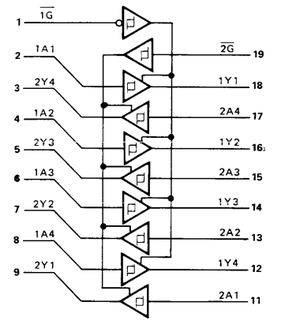
1820-1624
TRI-LEVEL
OCTAL LINE DRIVERS/
LINE RECEIVERS

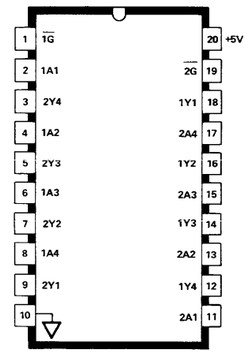




logic: 1Y = 1A when $\overline{1G}$ is low
2Y = 2A when $\overline{2G}$ is low
When $\overline{1G}$ is high 1Y outputs are at a high impedance
When $\overline{2G}$ is high 2Y outputs are at a high impedance

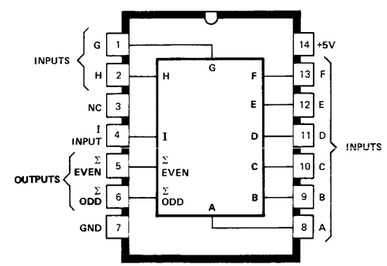
1820-1633
TRI-LEVEL
OCTAL LINE DRIVERS/
LINE RECEIVERS





logic: 1Y = $\overline{1A}$ when $\overline{1G}$ is low
2Y = $\overline{2A}$ when $\overline{2G}$ is low
When $\overline{1G}$ is high 1Y outputs are at a high impedance
When $\overline{2G}$ is high 2Y outputs are at a high impedance

1820-1638
9-BIT ODD/EVEN PARITY
GENERATOR/CHECKER



TRUTH TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

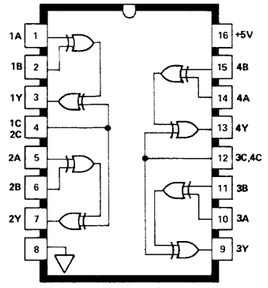
1820-1639
QUAD EXCLUSIVE OR/NOR GATE

TRUTH TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = high level, L = low level

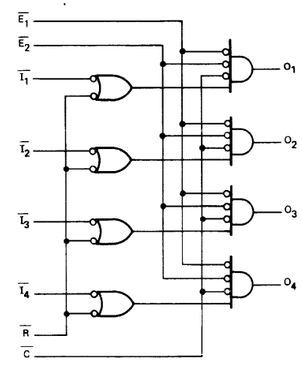
positive logic: $Y = (A \oplus B) \oplus C = A\overline{B}C + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$

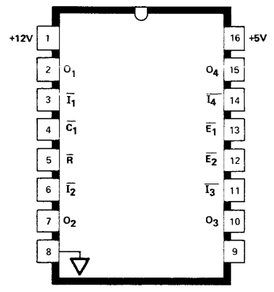


When C input is low, operates as a Exclusive OR gate. When C input is high, operates as a Exclusive NOR gate.

1820-1758
QUAD TTL TO MOS DRIVER

LOGIC DIAGRAM

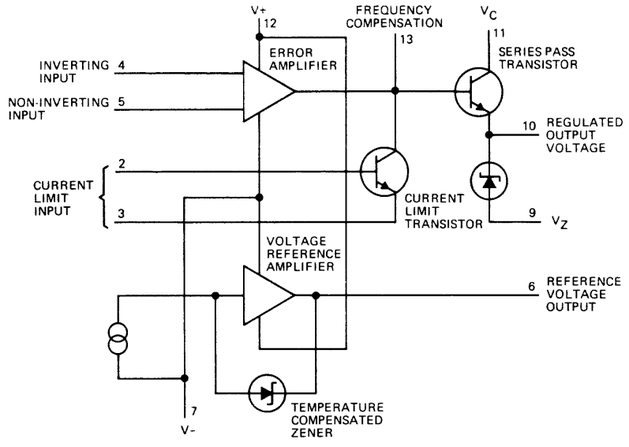


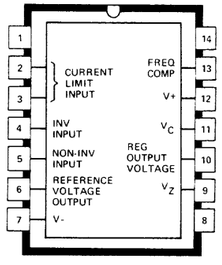


PIN NAMES

$\overline{I_1} \cdot \overline{I_4}$ SELECT INPUTS	$O_1 \cdot O_4$ DRIVER OUTPUTS
$\overline{E_1} \cdot \overline{E_4}$ ENABLE INPUTS	V_{CC} +5V POWER SUPPLY
$\overline{R}$ REFRESH SELECT INPUTS	V_{DD} +12V POWER SUPPLY
$\overline{C}$ CLOCK CONTROL INPUT	

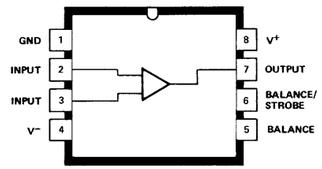
1826-0049
VOLTAGE REGULATOR



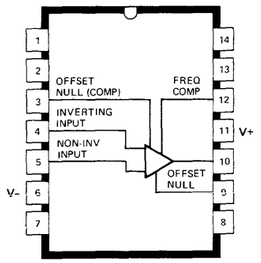


This integrated circuit provides a regulated voltage and a low-current reference voltage. Provisions are included for voltage shut-down in the event of excessive current in an external circuit. The integrated circuit can be used with external components in a variety of configurations. For specific information, refer to the applicable technical manual.

1826-0065
VOLTAGE COMPARATOR

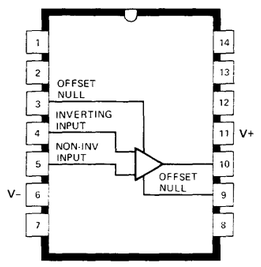


1826-0069
OPERATIONAL AMPLIFIER



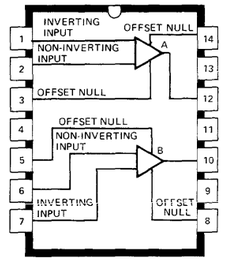
This integrated circuit is an operational amplifier. External components permit its use in a variety of functions, such as a long interval integrator, timer, sample-and-hold circuit square wave generator, or pulse-width modulator. For specific information, refer to the applicable technical manual.

1826-0070
OPERATIONAL AMPLIFIER



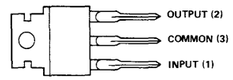
This integrated circuit is an operational amplifier. External components permit its use in a variety of functions. For specific information, refer to the applicable technical manual.

1826-0100
DUAL OPERATIONAL AMPLIFIER



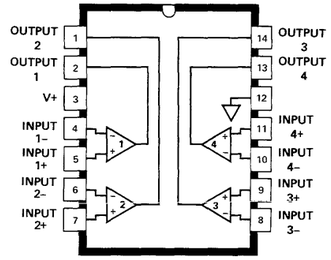
This integrated circuit consists of two separate operational amplifiers. External components permit their use in a variety of separate and combined functions. For specific information, refer to the applicable technical manual.

1826-0106
VOLTAGE REGULATOR



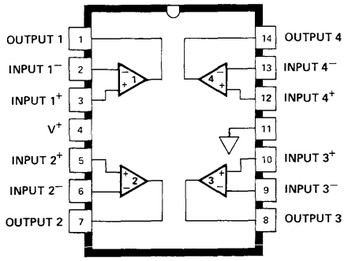
The voltage regulator provides a positive 15 volt output with current limiting, thermal shutdown, and safe area compensation internally incorporated in the device. Refer to the applicable equipment manual for specific use of the device.

1826-0138
QUAD VOLTAGE COMPARATOR



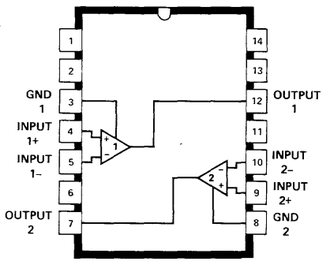
Refer to the applicable equipment manual for specific use of the device.

1826-0161
QUAD OPERATIONAL AMPLIFIER

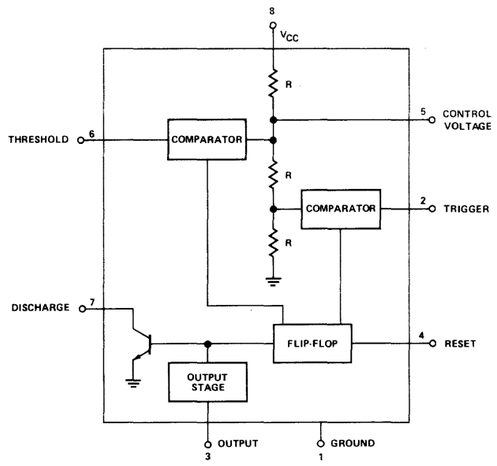


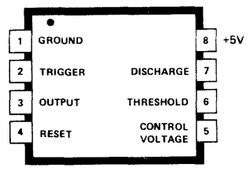
This Integrated circuit consists of four independent, high gain, internally frequency compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Input common mode voltage range includes ground. Differential input voltage range is equal to the power supply voltage, 3 to 30 volts.

1826-0175
DUAL VOLTAGE COMPARATOR



1826-0180
TIMER





The timer is a highly stable controller capable of producing accurate time delays or oscillation by the selected values of external components.

HARDWARE DESCRIPTION

SECTION III

3-1. SERIES II SYSTEMS

This section provides information to orient the reader to the system hardware in order for him to better understand the descriptions of signal and power distribution which follow in Section IV.

3-2. HARDWARE NOMENCLATURE

Cabinets of the HP 3000 Computer Systems derive their names from the hardware complement of the cabinet bays. There are four basic names for cabinets or bays as follows:

CPU Bay

The CPU bay contains the CPU/IOP card cage, three card cages containing memory with some room for I/O hardware, and at the bottom rear of the bay the power control module (PCM). The PCM satisfies the mainframe AC power requirements for all but very large systems.

I/O Bay

The three card cages of the I/O bay are primarily devoted to increasing the I/O capabilities of the system by providing housing for peripheral interface hardware. The I/O bay is used only in Model 8 and 9 Systems. The bottom rear of this bay contains a power control unit (PCU) in systems having an HP 2888A Disc File Subsystem.

PIO Bay

The peripheral I/O (PIO) bay contains a magnetic tape unit and one card cage that provides a limited I/O capability. The bottom rear of this bay may contain a PCU in systems having an HP 2888A Disc File Subsystem. The PIO bay is a component of Model 5, 6, and 7 Systems.

Peripheral Bay

The first peripheral bay of a Model 8 or 9 System houses the magnetic tape unit and is the leftmost bay of a three-bay computer system. In any system, additional peripheral bays may be added to the left of the first peripheral bay of a Model 8 or 9 System or the PIO bay of a Model 5, 6, or 7 System to house additional magnetic tape units and other peripheral hardware. The bottom rear of the first peripheral bay of a system upgraded to a Model 9 by the installation on an HP 30408A Upgrade Kit may contain a PCU.

3-3. SERIES II MODEL 5, 6, AND 7 SYSTEMS

A Series II Model 5, 6, or 7 System is housed in a two-bay equipment cabinet consisting of a CPU bay and a peripheral I/O bay. Figures 3-1 and 3-2 show the racking plan of Model 5, 6, and 7 Systems with notes explaining differences. Shown are the four card cages Nos. 1 through 4 of the CPU bay, the HP 7970E Magnetic Tape Drive occupying card cage positions Nos. 5 and 6 of the PIO bay, and card cage No. 7 of the PIO bay. Also shown are the 16-port HP 30062A Connector Panel and various DC power supplies and AC power modules. System hardware not shown includes the system desk, the HP 7905A Disc Drive of the Model 5 System, the HP 7920A Disc Drive of the Model 6 System, the HP 2888A Disc File of the Model 7 System, and the HP 2640A/B CRT Console. These components were not shown because this manual does not concern itself with hardware external to the equipment bays.

3-4. PCA Complement

Table 3-1 gives the PCA complement of the Model 5 System, table 3-1A gives the PCA complement of the Model 6 System, and table 3-2 gives the PCA complement of the Model 7 System, Their PCA complements compare as follows:

a. The PCA complements of the No. 1 card cages are identical.

b. In card cage No. 2, the Model 5 and 6 Systems have 64K words of fault control memory (2 memory array PCAs); the Model 7 has 96K (3 memory array PCAs).

   The Model 5, 6, and 7 have a Terminal Data Interface PCA in slot A1 of card cage No. 2 making the 15 ports of the HP 30062A Connector Panel available to peripheral devices by direct connection. The Model 6 and 7 also have a Terminal Control Interface PCA in slot A2 making the 15 ports of its HP 30062A Connector Panel alternately available to remote users via type 103A3 modems and telephone facilities. In all models, 15 ports are specified as available since the 16th port (port 0) is reserved for direct hard-wired connection to the system console.

c. In card cage No. 3 of the Model 5, slots A6 through A9 contain the interface PCAs for the HP 7905A Cartridge Discs. The interface must be configured on the selector channel so slots A1 through A4 of this card cage contain the PCAs of the selector channel. In the Model 7, slots A1 through A4 are reserved for adding an optionally available selector channel and slots A6 through A9 are reserved for an optionally available interface to one or more HP 7905A or 7920A Disc Drives. Slot A10 contains the System Clock for the Model 5 or 7.

For the Model 6, slots A1 through A6 of card cage No. 3 are unassigned. Slots A7 through A10 contain the port controller and selector channel for the HP 7920A Disc Drive interface located in card cage No. 4.

d. PCA complements of the No. 4 and 7 card cages are identical for Models 5 and 7 with the multiplexer channel in slot A1, the mag tape interface in slots A2 and A3, and the remainder of this card cage and slots A1 through A9 of card cage No, 7 connected to the IOP bus and multiplexer bus for programmed (SIO) I/O.

   For the Model 6, the multiplexer channel is in slot A1 of card cage No. 7 with the multiplexer bus connected to slots of card cage No. 7 and extended to slots A1 through A5 of card cage No. 4. Slots A6 through A 10 contain the HP 7920A Disc Drive interface

e. In the Model 7 card cage No. 7, slots A8, A9, and A10 hold the interface PCAs to the HP 2888A Disc Files This interface must be configured on the multiplexer channel. In the Model 5, these slots may be used for adding an optionally available interface to HP 2888A Disc Files. Slots A8 and A9 may be used for direct or programmed I/O if not used for the disc file interface. In the Model 6, these slots are available as I/O interfaces to peripheral devices.

3-5. DC Power Supplies

The Model 5, 6, and 7 DC power requirements are identical. An HP 30310A Power Supply, hinge-mounted at the top rear of the CPU bay, furnishes DC power to the CPU/IOP card cage and to an HP 30311A Power Supply mounted in the right half of the rack space above the fan filter. The HP 30311A Power Supply converts the DC power it receives to voltages required by the memory PCAs in card cage No. 2. The HP30312A Power Supply mounted to the left of the HP 30311A Power Supply satisfies the 5-volt power requirements of card cages Nos. 2, 3, and 4. A second HP 30310A Power Supply is hinge-mounted at tne top rear of the PIO bay. It furnishes power for the operation of PCAs in card cage No. 7.

3-6. AC Power Modules

In the Model 5, 6, and 7, the PCM at the bottom rear of the CPU bay distributes AC power to a 9-outlet service strip in the CPU bay and to a power distribution unit in the PIO bay. In the CPU bay, the four card cages, the HP 30310A and HP 30312A Power Supplies, and the cabinet fan all plug into the service strip. In 230-volt, 50 Hz systems, the power distribution unit in the PIO bay feeds a 9-outlet service strip. The magnetic tape drive, the card cage, and the cabinet fan plug into the service strip. In 208-volt, 60 Hz systems, the PIO bay has two service strips; one for the magnetic tape unit and one for the card cage and cabinet fan. AC power may connect from the PIO bay's power distribution unit to power distribution units of additional peripheral bays added to the left until 30 amperes per phase is exceeded.

In the Model 7 System, a Power Control Unit at the bottom rear of the peripheral I/O bay distributes AC power required by the HP 2888A Disc Files.

3-7. SERIES II MODEL 8 OR 9 SYSTEM

A Series II Model 8 or 9 System is housed in a three-bay equipment cabinet consisting of a CPU bay, an I/O bay and a peripheral bay. Figures 3-3 and 3-4 show the racking plan of the Model 8 or 9 System. Shown are the four card cages Nos. 1 through 4 of the CPU bay, the three card cages Nos. 5 through 7 of the I/O bay, and the HP 7970E Magnetic Tape Unit of the peripheral bay. Also shown are the 16-port HP 30062A Connector Panel and various DC power supplies and AC power modules. System hardware not shown includes the system desk, the HP 7920A Disc Drive of the Model 8, tne HP 2888A Disc Files of the Model 9, and the HP 2640A/B CRT Console. These components were not included because this manual does not concern itself with hardware external to the equipment bays.

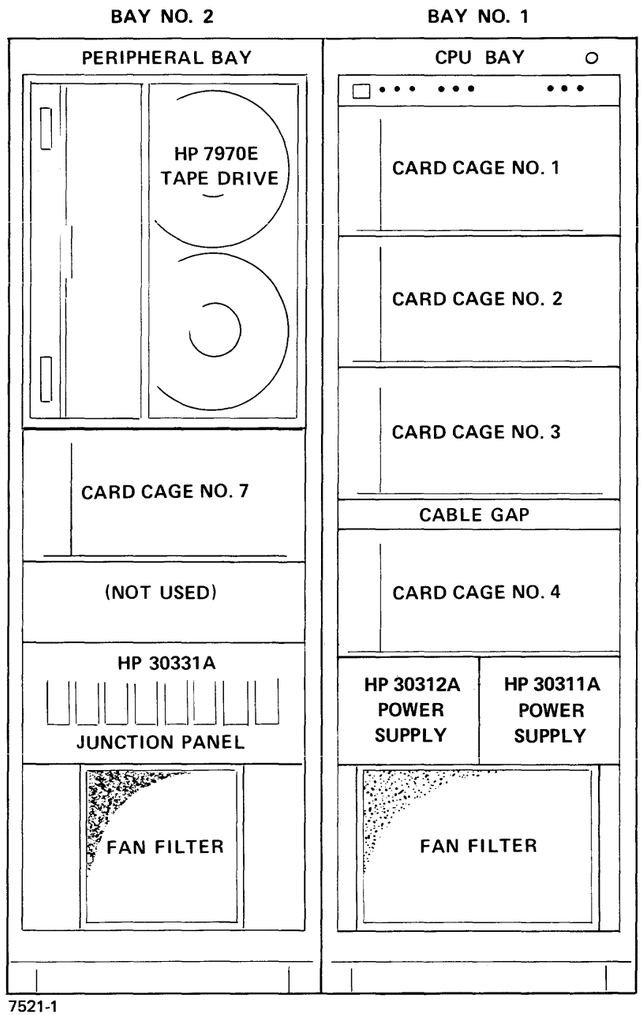
3-8. PCA Complement

Table 3-2A gives the PCA complement of the Model 8 System and Table 3-3 gives the PCA complement of the Model 9 System. A few comments on the PCA complement follow:

a. The PCA complement of card cages No. 1 is identical to that of card cage No. 1 of the Model 5, 6, or 7.

b. Card cages No. 2 contain 128K words (4 memory array PCAs) of fault correction memory. Both have a Terminal Data Interface PCA in slot A1 of card cage No. 2 making the 15 ports of the HP 30062A Connector Panel available to peripheral devices by direct connection. Both also have a Terminal Control Interface PCA in slot A2 making tne 15 ports of tne Connector Panel alternately available to peripheral devices remotely via type 103A3 modems or the equivalent and telephone facilities. An optional Terminal Control Interface PCA installed in slot A3 would make the 15 ports of the HP 30062A Connector Panel remotely available via type 202 modems. Note that in all cases 15 ports of the connector panel are specified as available since the 16th port (port 0) is reserved for direct hard-wired connection to the system console.

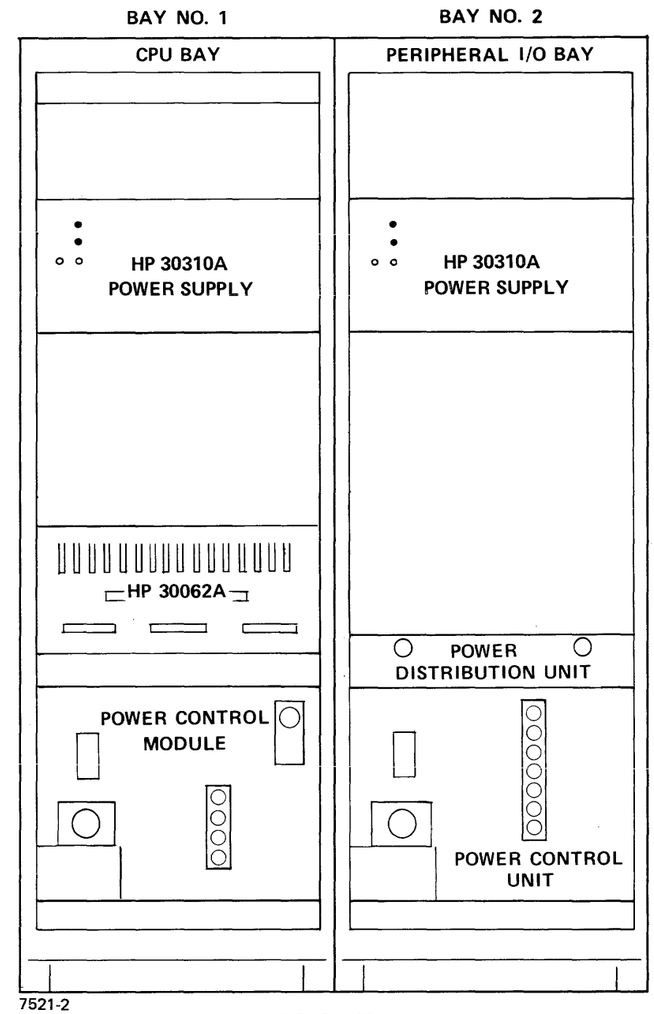
c. Card cage No. 3 contains 32K words of memory with an additional 96K words available at 32K words per memory array PCA. Slots A7 through A10 of the Model 8 contain the port controller and



FRONT VIEW
(DOORS OMITTED FOR CLARITY)

The Model 5 System will not have an HP 30331A Junction Panel unless it contains Option 144 or 146 (one or more HP 2888A Disc Files).

Figure 3-1. Models 5, 6, and 7 - Front View



REAR VIEW
(DOORS REMOVED FOR CLARITY)

The Model 5 System will not have a Power Control Unit unless it contains Option 144 or 146 (one or more HP 2888A Disc Files).

Figure 3-2. Models 5, 6, and 7 - Rear View

Table 3-1. PCA Slot Assignments, Model 5

	SLOT	PRINTED CIRCUIT ASSEMBLY
CARD CAGE NO. 1	A1	Reserved for maintenance panel PCA
	A2	30012-60001 Expanded Read-Only Memory
	A3	30003-60001 Read-Only Memory
	A4	30003-60002 Skip and Special Field
	A5	30003-60003 Arithmetic and Logic Unit
	A6	30003-60004 R Bus
	A7	30003-60005 S Bus
	A8	30003-60006 Current Instruction Register
	A9	30003-60007 Module Control Unit
	A10	30003-60008 Input Output Processor
CARD CAGE NO. 2	A1	30032-60001 Terminal Data Interface
	A2	Available for direct I/O*
	A3	Available for direct I/O*
	A4	30009-60002 Fault Logging Interface
	A5	30009-60001 Fault Correction Array
	A6	Reserved for 32K
	A7	Reserved for 32K
	A8	30008-60002 Memory Array (32K)
	A9	30008-60002 Memory Array (32K)
	A10	30007-60002 Memory Control and Logging
CARD CAGE NO. 3	A1	30030-60016 Selector Channel Port Controller
	A2	30030-60018 Selector Channel Register
	A3	30030-60003 Selector Channel Control
	A4	30030-60011 Selector Channel Sequencer
	A5	Reserved for maintenance
	A6	30229-60001 7905A/7920A Interface
	A7	13037-60002 Disc Controller
	A8	13037-60004 Error Correction Card
	A9	13037-60001 Microprocessor
	A10	30031-60001 System Clock
CARD CAGE NO. 4	A1	30036-60001 Multiplexer Channel
	A2	30215-60002 Magnetic Tape Controller Processor
	A3	30215-60006 Magnetic Tape Controller
	A4	Available for programmed (SIO) or direct I/O
	A5	Available for programmed (SIO) or direct I/O
	A6	Available for programmed (SIO) or direct I/O
	A7	Available for programmed (SIO) or direct I/O
	A8	Available for programmed (SIO) or direct I/O
	A9	Available for programmed (SIO) or direct I/O
	A10	Available for programmed (SIO) or direct I/O
CARD CAGE NO. 7	A1	Available for programmed (SIO) or direct I/O
	A2	Available for programmed (SIO) or direct I/O
	A3	Available for programmed (SIO) or direct I/O
	A4	Available for programmed (SIO) or direct I/O
	A5	Available for programmed (SIO) or direct I/O
	A6	Available for programmed (SIO) or direct I/O
	A7	Available for programmed (SIO) or direct I/O
	A8	Available for programmed (SIO) or direct I/O
	A9	Available for programmed (SIO) or direct I/O
	A10	Reserved for Disc File

*Slot A2 contains a Terminal Control Interface PCA in a system having a 103 Modem capability. Slots A2 and A3 contain Terminal Control Interface PCAs in a system having 103 and 202 Modem capabilities.

Table 3-1A. PCA Slot Assignments, Model 6

	SLOT	PRINTED CIRCUIT ASSEMBLY
CARD CAGE NO. 1	A1	Reserved for maintenance panel PCA
	A2	30012-60001 Expanded Read-Only Memory
	A3	30003-60001 Read-Only Memory
	A4	30003-60002 Skip and Special Field
	A5	30003-60003 Arithmetic and Logic Unit
	A6	30003-60004 R Bus
	A7	30003-60005 S Bus
	A8	30003-60006 Current Instruction Register
	A9	30003-60007 Module Control Unit
	A10	30003-60008 Input Output Processor
CARD CAGE NO. 2	A1	30032-60001 Terminal Data Interface
	A2	Available for direct I/O*
	A3	Available for direct I/O*
	A4	30009-60002 Fault Logging Interface
	A5	30009-60001 Fault Correction Array
	A6	Reserved for 32K
	A7	Reserved for 32K
	A8	30008-60002 Memory Array (32K)
	A9	30008-60002 Memory Array (32K)
	A10	30007-60002 Memory Control and Logging
CARD CAGE NO. 3	A1	Not used
	A2	Not used
	A3	Not used
	A4	Not used
	A5	Not used
	A6	Not used
	A7	30030-60016 Selector Channel Port Controller
	A8	30030-60018 Selector Channel Register
	A9	30030-60003 Selector Channel Control
	A10	30030-60011 Selector Channel Sequencer
CARD CAGE NO. 4	A1	Available for direct I/O
	A2	Available for direct I/O
	A3	Available for direct I/O
	A4	Reserved for Selector Channel Maintenance.
	A5	30031-60001 System Clock
	A6	Reserved for maintenance.
	A7	30229-60001 7905A/7920A Interface
	A8	13037-60002 Disc Controller
	A9	13037-60024 Error Correction Card
	A10	13037-60001 Microprocessor
CARD CAGE NO. 7	A1	30036-60001 Multiplexer Channel
	A2	30215-60002 Magnetic Tape Controller Processor
	A3	30215-60006 Magnetic Tape Controller
	A4	Available for programmed (SIO) or direct I/O
	A5	Available for programmed (SIO) or direct I/O
	A6	Available for programmed (SIO) or direct I/O
	A7	Available for programmed (SIO) or direct I/O
	A8	Available for programmed (SIO) or direct I/O
	A9	Available for programmed (SIO) or direct I/O
	A10	Available for programmed (SIO) or direct I/O

*Slot A2 contains a Terminal Control Interface PCA in a system having a 103 Modem capability. Slots A2 and A3 contain Terminal Control Interface PCAs in a system having 103 and 202 Modem capabilities.

Table 3-2. PCA Slot Assigments, Model 7

	SLOT	PRINTED CIRCUIT ASSEMBLY
CARD CAGE NO. 1	A1	Reserved for maintenance panel PCA
	A2	30012-60001 Expanded Read-Only Memory
	A3	30003-60001 Read-Only Memory
	A4	30003-60002 Skip and Special Field
	A5	30003-60003 Arithmetic and Logic Unit
	A6	30003-60004 R Bus
	A7	30003-60005 S Bus
	A8	30003-60006 Current Instruction Register
	A9	30003-60007 Module Control Unit
	A10	30003-60008 Input Output Processor
CARD CAGE NO. 2	A1	30032-60001 Terminal Data Interface
	A2	30061-60001 Terminal Control Interface
	A3	Available for direct I/O*
	A4	30009-60002 Fault Logging Interface
	A5	30009-60001 Fault Correction Array
	A6	Reserved for 32K
	A7	30008-60002 Memory Array (32K)
	A8	30008-60002 Memory Array (32K)
	A9	30008-60002 Memory Array (32K)
	A10	30007-60002 Memory Control and Logging
CARD CAGE NO. 3	A1	Reserved for Selector Channel (30030-60016)
	A2	Reserved for Selector Channel (30030-60018)
	A3	Reserved for Selector Channel (30030-60003)
	A4	Reserved for Selector Channel (30030-60011)
	A5	Reserved for maintenance
	A6	Reserved for 7905A/7920A Interface (30229-60001)
	A7	Reserved for Disc Controller (13037-60002)
	A8	Reserved for Disc Controller (13037-60004)
	A9	Reserved for Disc Controller (13037-60001)
	A10	30031-60001 System Clock
CARD CAGE NO. 4	A1	30036-60001 Multiplexer Channel
	A2	30215-60002 Magnetic Tape Controller Processor
	A3	30215-60006 Magnetic Tape Controller
	A4	Available for programmed (SIO) or direct I/O
	A5	Available for programmed (SIO) or direct I/O
	A6	Available for programmed (SIO) or direct I/O
	A7	Available for programmed (SIO) or direct I/O
	A8	Available for programmed (SIO) or direct I/O
	A9	Available for programmed (SIO) or direct I/O
	A10	Available for programmed (SIO) or direct I/O
CARD CAGE NO. 7	A1	Available for programmed (SIO) or direct I/O
	A2	Available for programmed (SIO) or direct I/O
	A3	Available for programmed (SIO) or direct I/O
	A4	Available for programmed (SIO) or direct I/O
	A5	Available for programmed (SIO) or direct I/O
	A6	Available for programmed (SIO) or direct I/O
	A7	Available for programmed (SIO) or direct I/O
	A8	30202-60003 Controller Processor (HP 2888A)
	A9	30202-60001 Read/Write (HP 2888A)
	A10	30202-60002 Bus (HP 2888A)

*Slot A2 contains a Terminal Control Interface PCA in a system having a 103 Modem capability. Slots A2 and A3 contain Terminal Control Interface PCAs in a system having 103 and 202 Modem capabilities.

selector channel associated with the HP 7905A/7920A Disc Drive interface in slots A7 through A10 of card cage No. 4. Slots A7 through A10 of the Model 9 are reserved for an optional selector channel which will operate with the optional HP 7905A/7920A Disc Drive interface in card cage No. 4.

d. For the Model 8, slots A6 through A10 of card cage No. 4 contain the HP 7920A Disc Drive interface which is controlled by the port controller and selector channel in card cage No. 3. This port controller is capable of also controlling an optional second selector channel (slots A1 through A3 of card cage No. 4) which operates with an optional HP 7905A/7920A Interface in slot A5 of card cage No. 4. The HP 13037B Disc Controller for this second disc drive interface will reside in slots A8 through A10 of card cage No. 7 which are reserved for this usage.

   For the Model 9, slots A1 through A5 of card cage No, 4 are unassigned and slots A6 through A10 are reserved for an optional HP 7905A/7920A Disc Drive interface.

e. Slot A1 of card cage No. 5 contains a multiplexer channel. The multiplexer bus connects to all slots of the card cages in the I/O bay except slots A8 through A10 of card cage No. 7 for the Model 8 or slot A10 of card cage No. 7 for the Model 9. All PCAs of the I/O bay installed in these slots are able to operate as programmed I/O using the SIO double-word commands with the multiplexer or, since all PCAs are also on the IOP bus, as direct I/O using direct commands from the IOP.

f. For the Model 8, slots A8 through A10 of card cage No. 7 are not connected to the IOP bus or the multiplexer channel bus. These slots are cabled on the backplane to receive the PCAs of the second HP 13037B Disc Controller when the system is configured for having two selector channel/disc drive interfaces.

   For the Model 9, slot A10 of card cage No. 7 is not connected to the IOP bus or the multiplexer channel bus. Connectors P2 and P3 are free to be cabled from the Bus PCA of the HP 2888A Disc File interface to the Disc File junction panel. Slots A8 through A10 of card cage No. 7 are used for the disc file interface in the standard Model 9 system.

g. Slot A10 of card cage No. 7 is not connected to the IOP bus or the multiplexer bus. Connectors P3 and P2 are free to be cabled from the Bus PCA of the HP 2888A Disc File Inter- Interface to the Disc File Junction Panel. Slots A7 through A10 are used for the disc file interface in the standard Model 9 System.

3-9. DC Power Supplies

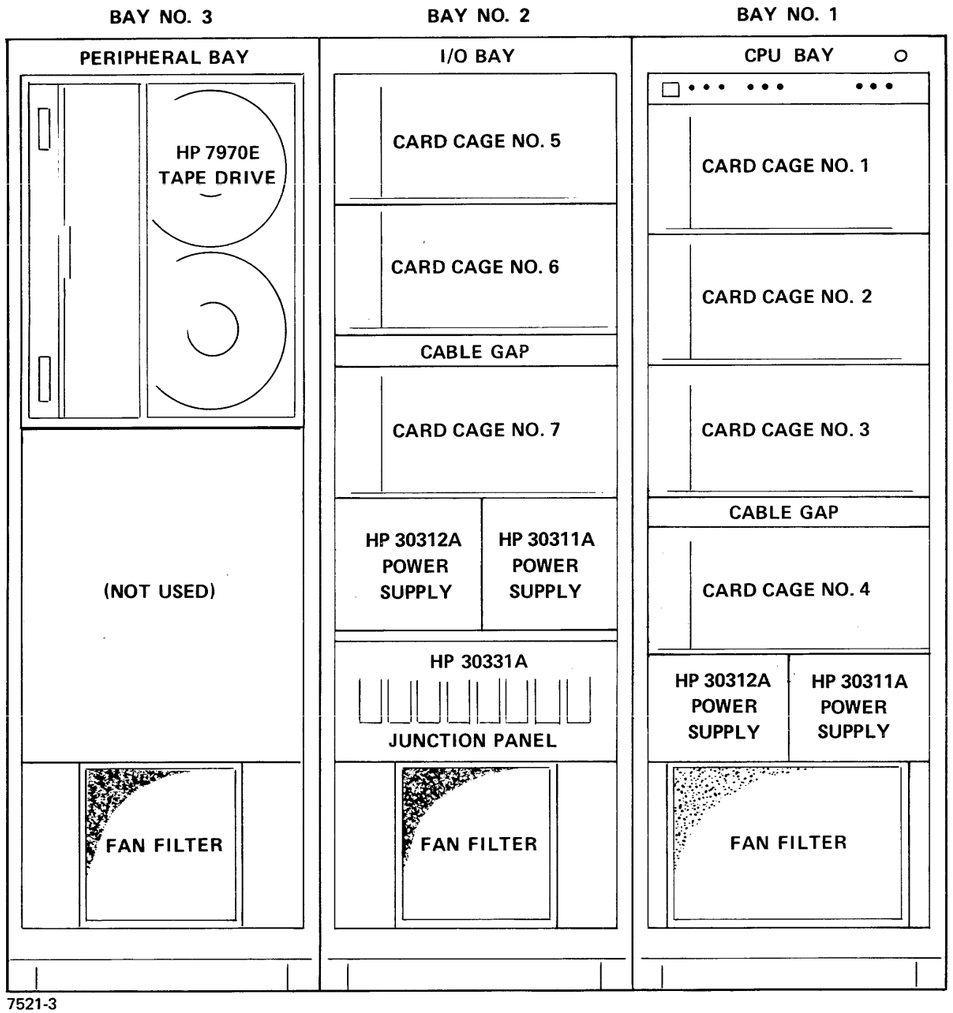
The Model 9 System has two HP 30310A Power Supplies. One is hinge-mounted at the top of the CPU bay; the second is hinge-mounted at the top rear of the I/O bay. The HP 30310A in the CPU bay furnishes DC

power to the CPU/IOP card cage No. 1 and to an HP 30311A Power Supply mounted in the right half of the rack space above the fan filter. The HP 30311A Power Supply converts the DC power it receives to voltages suitable for operating memory PCAs in card cage No. 2. The HP 30310A Power Supply in the I/O bay furnishes DC power to card cage No. 5 and to an HP 30311A Power Supply mounted in the right half of the rack space above the HP 30331A Junction Panel for the HP 2888A Disc File. This HP 30311A Power Supply converts the DC power it receives to voltages suitable for operating memory PCAs in card cage No. 3 of the CPU bay. The HP 30312A Power Supply mounted to the left of the HP 30311A Power Supply in the CPU bay satisfies the 5-volt power requirements of card cages Nos. 2, 3, and 4. The HP 30312A Power Supply mounted to the left of the HP 30311A Power Supply in the I/O bay satisfies the 5-volt power requirements of card cages Nos. 6 and 7.

3-10. AC Power Modules

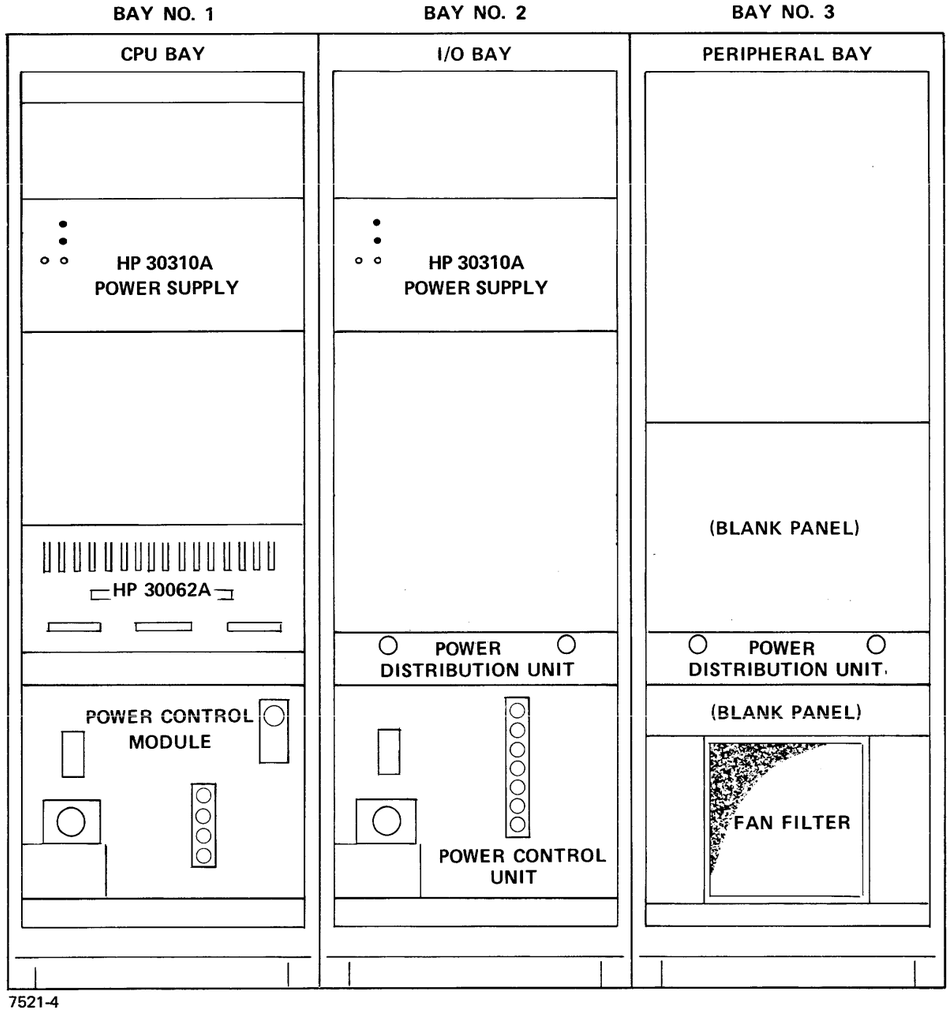
The PCM at the bottom rear of the CPU bay distributes AC power to a 9-outlet service strip in the CPU bay and to a power distribution unit (PDU) in the I/O bay. The four card cages, the HP 30310A and HP 30312A Power Supplies, and the cabinet fan plug into the service strip of the CPU bay. The three card cages, the HP 30310A and HP 30312A Power Supplies, and the cabinet fan of the I/O bay plug into a 9-volt service strip fed by the I/O bay's PDU. From the I/O bay's PDU, AC power is fed in parallel to a PDU in the first peripheral bay and from there to PDUs in any additional peripheral bays until 30 amperes per phase is exceeded. A peripheral bay fed by a three- phase 60 Hertz source has a 208-volt service strip and a 115-volt service strip. The cabinet fan and any rack-mounted peripheral devices that operate on 208 volts plug into the 208-volt service strip. The magnetic tape unit and any other peripheral devices that operate on 115 volts plug into the 115-volt service strip. A peripheral bay fed by a single-phase 50 Hertz source has only a 230-volt service strip. The cabinet fan plugs into this service strip as well as all rack-mounted peripheral devices that are suitably modified to operate on 230 volts.

AC power for the HP 2888A Disc File is brought in from the user's mains via a power control unit at the bottom rear of the I/O bay. The AC power is distributed (along with data and control signals) by the HP 30331A Junction Panel at the lower front of the I/O bay to the HP 2888A Disc File Drives.



FRONT VIEW
(DOORS OMITTED FOR CLARITY)

Figure 3-3. Models 8 and 9 - Front View



REAR VIEW
(DOORS REMOVED FOR CLARITY)

Figure 3-4. Models 8 and 9 - Rear View

Table 3-2A. PCA Slot Assignments, Model 8

	SLOT	PRINTED CIRCUIT ASSEMBLY		SLOT	PRINTED CIRCUIT ASSEMBLY
CARD CAGE NO. 5	A1	30036-60001 Multiplexer Channel	CARD CAGE NO. 1	A1	Reserved for maintenance panel PCA
	A2	30215-60002 Magnetic Tape Controller Processor		A2	30012-60001 Expanded Read-Only Memory
	A3	30215-60006 Magnetic Tape Controller		A3	30003-60001 Read-Only Memory
	A4	30031-60001 System Clock/Console Interface		A4	30003-60002 Skip and Special Field
	A5	Available for programmed (SIO) or direct I/O		A5	30003-60003 Arithmetic and Logic Unit
	A6	Available for programmed (SIO) or direct I/O		A6	30003-60004 R Bus
	A7	Available for programmed (SIO) or direct I/O		A7	30003-60005 S Bus
	A8	Available for programmed (SIO) or direct I/O		A8	30003-60006 Current Instruction Register
	A9	Available for programmed (SIO) or direct I/O		A9	30003-60007 Module Control Unit
	A10	Available for programmed (SIO) or direct I/O		A10	30003-60008 Input Output Processor
CARD CAGE NO. 6	A1	Available for programmed (SIO) or direct I/O	CARD CAGE NO. 2	A1	30032-60001 Terminal Data Interface
	A2	Available for programmed (SIO) or direct I/O		A2	30061-60001 Terminal Control Interface
	A3	Available for programmed (SIO) or direct I/O		A3	Available for direct I/O*
	A4	Available for programmed (SIO) or direct I/O		A4	30009-60002 Fault Logging Interface
	A5	Available for programmed (SIO) or direct I/O		A5	30009-60001 Fault Correction Array
	A6	Available for programmed (SIO) or direct I/O		A6	30008-60002 Memory Array (32K)
	A7	Available for programmed (SIO) or direct I/O		A7	30008-60002 Memory Array (32K)
	A8	Available for programmed (SIO) or direct I/O		A8	30008-60002 Memory Array (32K)
	A9	Available for programmed (SIO) or direct I/O		A9	30008-60002 Memory Array (32K)
	A10	Available for programmed (SIO) or direct I/O		A10	30007-60002 Memory Control and Logging
CARD CAGE NO. 7	A1	Available for programmed (SIO) or direct I/O	CARD CAGE NO. 3	A1	30007-60002 Memory Control and Logging
	A2	Available for programmed (SIO) or direct I/O		A2	30008-60002 Memory Array (32K)
	A3	Available for programmed (SIO) or direct I/O		A3	Reserved for 32K
	A4	Available for programmed (SIO) or direct I/O		A4	Reserved for 32K
	A5	Available for programmed (SIO) or direct I/O		A5	Reserved for 32K
	A6	Available for programmed (SIO) or direct I/O		A6	30009-60001 Fault Correction Array
	A7	Reserved for maintenance PCA		A7	30030-60016 Selector Channel Port Controller
	A8	Reserved for HP 13037B Disc Controller		A8	30030-60018 Selector Channel Register
	A9	Reserved for HP 13037B Disc Controller		A9	30030-60003 Selector Channel Control
	A10	Reserved for HP 13037B Disc Controller		A10	30030-60011 Selector Channel Sequencer
			CARD CAGE NO. 4	A1	Reserved for Selector Channel No. 2 (30030-60018)
				A2	Reserved for Selector Channel No. 2 (30030-60003)
				A3	Reserved for Selector Channel No. 2 (30030-60011)
				A4	Reserved for maintenance
				A5	Reserved for 7905A/7920A Interface No. 2 (30229-60001)
				A6	Reserved for maintenance
				A7	30229-60001 7905A/7920A Interface
				A8	13037-60002 Device Controller
				A9	13037-60024 Error Correction Card
				A10	13037-60001 Microprocessor

*Slot A2 contains a Terminal Control Interface PCA in a system having a 103 Modem capability. Slots A2 and A3 contain Terminal Control Interface PCAs in a system having 103 and 202 Modem capabilities.

Table 3-3, PCA Slot Assignments, Model 9

	SLOT	PRINTED CIRCUIT ASSEMBLY		SLOT	PRINTED CIRCUIT ASSEMBLY
CARD CAGE NO. 5	A1	30036-60001 Multiplexer Channel	CARD CAGE NO. 1	A1	Reserved for maintenance panel PCA
	A2	30215-60002 Magnetic Tape Controller Processor		A2	30012-60001 Expanded Read-Only Memory
	A3	30215-60006 Magnetic Tape Controller		A3	30003-60001 Read-Only Memory
	A4	30031-60001 System Clock		A4	30003-60002 Skip and Special Field
	A5	Available for programmed (SIO) or direct I/O		A5	30003-60003 Arithmetic and Logic Unit
	A6	Available for programmed (SIO) or direct I/O		A6	30003-60004 R Bus
	A7	Available for programmed (SIO) or direct I/O		A7	30003-60005 S Bus
	A8	Available for programmed (SIO) or direct I/O		A8	30003-60006 Current Instruction Register
	A9	Available for programmed (SIO) or direct I/O		A9	30003-60007 Module Control Unit
	A10	Available for programmed (SIO) or direct I/O		A10	30003-60008 Input Output Processor
CARD CAGE NO. 6	A1	Available for programmed (SIO) or direct I/O	CARD CAGE NO. 2	A1	30032-60001 Terminal Data Interface
	A2	Available for programmed (SIO) or direct I/O		A2	30061-60001 Terminal Control Interface
	A3	Available for programmed (SIO) or direct I/O		A3	Available for direct I/O *
	A4	Available for programmed (SIO) or direct I/O		A4	30009-60002 Fault Logging Interface
	A5	Available for programmed (SIO) or direct I/O		A5	30009-60001 Fault Correction Array
	A6	Available for programmed (SIO) or direct I/O		A6	30008-60002 Memory Array (32K)
	A7	Available for programmed (SIO) or direct I/O		A7	30008-60002 Memory Array (32K)
	A8	Available for programmed (SIO) or direct I/O		A8	30008-60002 Memory Array (32K)
	A9	Available for programmed (SIO) or direct I/O		A9	30008-60002 Memory Array (32K)
	A10	Available for programmed (SIO) or direct I/O		A10	30007-60002 Memory Control and Logging
CARD CAGE NO. 7	A1	Available for programmed (SIO) or direct I/O	CARD CAGE NO. 3	A1	30007-60002 Memory Control and Logging
	A2	Available for programmed (SIO) or direct I/O		A2	30008-60002 Memory Array (32K)
	A3	Available for programmed (SIO) or direct I/O		A3	Reserved for 32K
	A4	Available for programmed (SIO) or direct I/O		A4	Reserved for 32K
	A5	Available for programmed (SIO) or direct I/O		A5	Reserved for 32K
	A6	Available for programmed (SIO) or direct I/O		A6	30009-60001 Fault Correction Array
	A7	Reserved for maintenance PCA		A7	Reserved for Selector Channel
	A8	30202-60003 Controller Processor (HP 2888A)		A8	Reserved for Selector Channel
	A9	30202-60001 Read/Write (HP 2888A)		A9	Reserved for Selector Channel
	A10	30202-60002 Bus (HP 2888A)		A10	Reserved for Selector Channel
			CARD CAGE NO. 4	A1	Reserved for Selector Channel No. 2
				A2	Reserved for Selector Channel No. 2
				A3	Reserved for Selector Channel No. 2
				A4	Reserved for maintenance PCA
				A5	Reserved for 7905A Interface
				A6	Reserved for maintenance PCA
				A7	Reserved for Cartridge Disc Interface
				A8	Reserved for Cartridge Disc Interface
				A9	Reserved for Cartridge Disc Interface
				A10	Reserved for Cartridge Disc Interface

*Slot A2 contains a Terminal Control Interface PCA in a system having a 103 Modem capability. Slots A2 and A3 contain Terminal Control Interface PCAs in a system having 103 and 202 Modem capabilities.

WIRING INFORMATION

SECTION VI

4-1. INTRODUCTION

The signal busses of the System interconnect the functional areas of the computer. The central (CTL) data bus is the data and control path which interconnects the memory, CPU/IOP, and the selector channel. The Module Control Unit (MCU) interfaces the CPU/IOP to the CTL data bus. A Port Controller functions as an MCU for the Selector Channel and MCU logic on a memory control PCA performs the interface for the memory modules. The IOP provides control and data handling services for the System Clock, Multiplexer, and device controllers via its IOP bus. The multiplexer (MUX) channel bus connects the MUX to up to 16 device controllers. The combination of Selector Channel and disc drive controller/interface can handle up to 8 disc drives.

4-2. FUNCTIONAL AREAS

The CPU/IOP, Memory, Multiplexer, and Selector Channel are the four principal areas of the system. The groups of signals making up the busses that interconnect these functional areas are listed in tables of this section. Also in functional areas comprised of more than one PCA, the mnemonics of the signals carried by the flat cables interconnecting the PCAs are tabulated.

4-3. CPU/IOP

The CPU/IOP consists of nine PCAs contained in slots A2 through A10 of a ten-slot PCA module (card cage). This is a dedicated module; its backplane is a PCA expressly designed to interconnect the signals of the PCAs it houses. (The other functional areas are located in ten- slot, memory or input/output (MIO) modules designed for universal use.) Slot A1 of the dedicated module may contain a PCA which interfaces to a maintenance panel when the system is being serviced.

When a PCA is seated in a CPU/IOP module slot, its printed circuit connectors mate with two 80-pin connectors on the module backplane. The backplane PCA has 20 such connectors, two for each PCA. Use Table 4-1 when tracing signals at the backplane. In Table 4-1, signal destinations are typically formatted as P1-XX or P2-XX where XX is the pin number of the connector. When an asterisk replaces the dash of the destination format, it denotes a signal source, P1*XX or P2*XX. The BUS column of Table 4-1 shows signals that enter of leave the CPU/IOP module.

Bus connections are:

P1 Power Bus
P2 Central Data Bus
P3 IOP Bus
P4 Not used
P5 Not used

Table 4-2 lists the signals of the power bus. The power bus carries IOP bus related signals and distributes DC power. (Power is distributed on the power bus from the terminal board on the rear of the PCA module to connector P1 of any PCA housed in the PCA module. These power circuits do not connect on a power bus from one module to another.) Table 4-3 lists signals of the CTL data bus and Table 4-4 lists signals of the IOP bus.

Table 4-5 lists the signals at front connector J1 of the Current Instruction Register PCA. These signals are routed by flat cable to provide control and display at the system control panel. The system control panel is located on the front door of the CPU bay.

Table 4-5A lists the signals at front connector J2 of the Current Instruction Register PCA. These signals are routed by flat cable to connector J2 of a maintenance PCA in slot A1 of card cage No. 1 during maintenance periods when the HP 30354A Maintenance Panel is in use.

4-4. Multiplexer Channel

The Multiplexer Channel PCA resides in a slot of memory or input/ output (MIO) PCA module usually near the PCAs of the device controllers that it serves. The MIO modules provide only a PCA connector receptacle for PCA connector P1. Connector P1 carries signals and voltages of the power bus. The module leaves the remaining five edge connectors of the PCA exposed so they may be custom connected by cables as necessary. Connectors P2 and P3 at the rear of the PCA and module are usually used for connection to the system's busses. Connectors J1, J2, and J3 at the front of the PCA are typically used for the interconnection of signals from PCA to PCA within a functional area or, in the case of a device controller, from the PCA to the device. For the Multiplexer Channel, connectors J1, J2, and J3 are not used, connector P2 is cabled to the Multiplexer Channel bus (Table 4-6), and connector P3 connects to the IOP bus (Table 4-4). The Multiplexer Channel executes the I/O programs of up to 16 device controllers on the Multiplexer Channel and IOP busses.

4-5. Selector Channel

The HP 30030B Selector Channel is comprised of three PCAs which occupy three slots of a memory-input/output (MIO) PCA module usually near the PCAs of the device controllers that it serves. A Port Controller PCA is

required to interface the Selector Channel and Memory via the CTL data bus. The MIO module has a single stack of ten PCA receptacles to receive the power bus connectors P1 of each PCA installed in it. The module leaves the remaining five edge connectors of the PCA exposed so they may be custom connected by cables as needed. Connectors P2 and P3 at the rear of the PCA are usually used for connection to the system's busses.

Connectors J1, J2, and J3 at the front of the PCA are typically used for the interconnection of signals from PCA to PCA within a functional area or, in the case of a device controller, from the PCA to the device. For the Selector Channel, a flat cable interconnects the three J1 connectors and another interconnects the three J2 connectors. The three J3 connectors of the Selector Channel and all front connectors of the Port Controller are not cabled. A flat cable interconnects P3 of the Port Controller and P3 of all Selector Channel PCAs forming a Port Controller bus (Table 4-7). The Selector Channel bus, Table 4-8, interconnects P2 of all three cards of a Selector Channel and must be routed to P2 of all high-speed device controllers served by the Selector Channel. Table 4-9 lists the signals of the flat cable interconnecting the J1 connectors of the Selector Channel and Table 4-10 lists the signals of the flat cable interconnecting the J2 connectors of the Selector Channel.

4-6. Memory

A standard Model 5 or 6 System has 64K words of memory and a standard Model 7 System has 96K words but all are easily expandable to 128K words in 32K-word increments. Slots A4 through A10 of card cage No. 2 are dedicated to memory PCAs.

A standard Model 8 or 9 System has 160K words of memory but can easily expanded to 256K words in 32K-word increments. Slots A4 through A10 of card cage No. 2 and slots A1 through A6 of card cage No. 3 are dedicated to memory PCAs.

Signals of the flat cables connecting J1, J2, and J3 at the front of the card cage are given in Tables 4-11, 4-12, and 4-13, respectvely. Table 4-14 lists the IOP/power bus signals as they appear at a memory card cage power bus. Table 4-15 lists the signals carried by the error logging interface cable which connects P3 of the memory control and logging PCA to P2 of the fault logging interface PCA.

4-6A. Input/Output

The input/output area may be considered a fifth functional area. The input/output area consists of the device controller PCAs and the peripheral devices. This area is interfaced to the four principal areas via the IOP bus for direct I/O. For programmed (SIO) I/O, the interface is via the IOP bus and either the Multiplexer Channel bus or the Selector Channel bus. Tables 4-15A through 4-15M list the signals related to this area.

4-6B. SYSTEM FLAT CABLES

Figures 4-3A through 4-3F provide information on the system's flat ribbon cables and their terminators as follows:

a. Figure 4-3A shows the locations of the flat cable terminators for a Model 6 System and 4-3B the flat cables.

b. Figure 4-3C shows the locations of the flat cable terminators for a Model 8 System and 4-3D the flat cables.

c. Figure 4-3E shows the locations of the flat cable terminators for a Model 5 or 7 System and 4-3F the flat cables.

d. Figure 4-3G shows the locations of the flat cable terminators for a Model 9 System and 4-3H the flat cables.

Tables on Figures 4-3B, 4-3D, 4-3F, and 4-3H provide cross reference between cable designators assigned in the figures and signal tables of this section that list pin-by-pin the signals of the cables.

Table 4-1. Backplane Wiring List

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
-APE									P2- 7	P2- 7	P2-47
-BPINT	P1*30							P1-32			
-CARRY	P1-65			P1-65	P1*65						
-CF3				P2*18	P2-18						
-CLK	P1-78	P1-78	P1-78	P1*78	P1-78	P1-78	P1-78	P1-78	P1-78	P1-78	P5- 2
-CLSR				P1*15		P1-15					
-CPUINH									P2-48	P2*48	
-CPULSEL							P1=58		P1*61		
-CPURST	P2-78	P2-78	P2-78	P2-78	P2*78	P2-78	P2-78	P2-78	P2-78		P5-50
-CPURSTS					P2-71			P2*69			
-DATAPE								P1*11	P1-11		
-DCTERZ									P1-47	P1*47	
-DECSR			P1*22			P1-24		P1-24			
-DEVN00										P2*18	P3- 8
-DEVN01										P2*24	P3- 9
-DEVN02										P2*25	P3-11
-DEVN03										P2*26	P3-12
-DEVN04										P2*27	P3-14
-DEVN05										P2*28	P3-15
-DEVN06										P2*29	P3-17
-DEVN07										P2*30	P3-18
-DISPLAY	P1*68		P1-68	P1-68		P1-68			P1-68		
-ENB									P2*18		
-ENFRZEN	P1*12								P1-12	P1-15	
-EXTRP	P1-37										
-FCLK	P1-79	P1-79	P1-79	P1*79	P1-79	P1-79	P1-79	P1-79	P1-79		P5- 4
-FMB				P1*59	P1-59						
-FIELD6					P1*34			P1-15			
-FIELD8					P1*35					P1-35	
-FIELD9					P1*32			P1-31			
-FRCLK			P1-14	P1*10							
-FRUNCLK	P2-35			P2*32							
-FRZ	P1-51			P1-50					P1*46	P1-46	
-HSREQ										P1-37	P1-12
-INCSR			P1*29			P1-27		P1-27			
-INCT				P2*74			P2-77				
-INTACK										P2-71	P3-50
-INTREQ										P2*65	P3-44
-INTRP1				P2-52				P2*58			
-IOCMD0										P2*11	P3- 4
-IOCMD1										P2*17	P3- 6
-IOCMD2										P2*12	P3- 5
-IOD0										P2*31	P3-20
-IOD1										P2*32	P3-21
-IOD10										P2*49	P3-35
-IOD11										P2*59	P3-36
-IOD12										P2*61	P3-38
-IOD13										P2*62	P3-39
-IOD14										P2*63	P3-41
-IOD15										P2*64	P3-42

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
-IOD2										P2*33	P3-23
-IOD3										P2*34	P3-24
-IOD4										P2*41	P3-26
-IOD5										P2*42	P3-27
-IOD6										P2*43	P3-29
-IOD7										P2*44	P3-30
-IOD8										P2*45	P3-32
-IOD9										P2*46	P3-33
-IODPE										P2*10	P3- 2
-IODPRTY										P2* 9	P3- 1
-IOPACT									P1-22	P1-23	
-IORESET					P2*79				P2-79	P2-79	
-IORSTSW					P2-70						
-IOSTEP	P1*45									P1-44	
-IOSTROB									P1*17	P1-12	
-IOTIMER									P1*29	P1-29	
-IOX14										P2-67	P3-47
-IOX15										P2-69	P3-48
-JBNDV				P2-66	P2*66						
-JLUT1			P1*18	P1-12							
-JMPFRZ	P1-54			P1*56						P1-31	
-JMPJSR1		P2*23	P2-28		P2-28						
-JSR1		P1*15	P1-11								
-LDACOR											
-LDDCOR											
-LSRSP0	P2*23			P2-30							
-MCUCL0R				P1*24							
-MCUCL1R				P1*26							
-MCUCL2R				P1*28							
-MCUCL3R				P1*30							
-MCUCL4R				P1*32							
-MCUCL5R				P1*34							
-MCUCL6R				P1*36							
-MCUCL7R				P1*38							
-MCUCLK0				P1*23							
-MCUCLK1				P1*25							
-MCUCLK2				P1*27							
-MCUCLK3				P1*29							
-MCUCLK4				P1*31							
-MCUCLK5				P1*33							
-MCUCLK6				P1*35							
-MCUCLK7				P1*37							
-MCUFR1R				P1* 4							
-MCUFRC0				P1* 1							
-MCUFRC1				P1* 3							
-MCURST										P2* 1	P2-49
-MODINH										P2-41	
-MODINHR										P2-42	
-MPIFRZ	P1*34									P1-33	
-NEXT1		P1* 6	P1- 6								

Table 4-1. Backplane Wiring List (Continued)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
-NOP	P2-38			P2-70				P2*70			
-NOP2				P2*77	P2-77	P2-77			P2-76		
-NXTG			P1-66			P1*67					
-OVFL	P1-53			P1-53	P1*44						
-PADDX						P2-79		P2*79			
-PANLRD	P1-56		P1*56	P1-54							
-PFWARN					P1-24						P1- 2
-PNLS	P2-12		P2-14	P2-14	P2*11						
-POLORSO									P1-26	P1*26	
-RBR1			P1*55	P1-52			P1-28				
-RDIOA							P1*64			P1-64	
-REPN					P2*68		P2-65				
-REVMCUP					P1*43		P1-56				
-ROMFCN1			P2*22			P2-24					
-RORT15			P2*36	P2-36							
-RORT16			P2*38	P2-38							
-RORT21			P2*37		P2-32						
-RSB1			P2* 3	P2- 3							
-SAME				P1-75	P1*77						
-SBR				P2-48		P2*46					
-SETERR					P1*36				P1-36	P1-36	
-SF3				P2*17	P2-17						
-SFQ0						P2-44	P2*44				
-SI									P1*41	P1-41	P1-16
-SIFRZ									P1-34	P1*34	
-SIOCMP									P1-27	P1*28	
-SLOAD	P1*13				P1-13	P1-13		P1-13	P1-13	P1-13	
-SO										P1*43	P1-18
-SPBBANK				P1-57			P1-62		P1*65		
-STEPENB	P1*38									P1-32	
-STTR						P1*38	P1-38				
-SWLDRAR	P2*13			P2-26				P2-11			
-SYSPE									P2*27	P2- 8	P2-48
-T=0				P1-74	P1*74						
-TESTFRZ									P1-32		
-TINT		P2*56						P2-56			P5-48
-TMRUFRZ					P2*59				P1-45		
-TR0						P1*34	P1-34				
-TR1						P1*35	P1-35				
-TR2						P1*36	P1-36				
-TR3						P1*37	P1-37				
-UNC1			P1* 5	P1- 5							
-V0	P2* 9	P2-11	P2*11					P2* 7			P5-10
-V1	P2*10	P2-12	P2*12					P2* 8			P5-12
-V10	P2*31	P2-31	P2*31					P2*31			P5-30
-V11	P2*32	P2-32	P2*32					P2*32			P5-32
-V12	P2*33	P2-33	P2*33					P2*33			P5-34
-V13	P2*34	P2-34	P2*34					P2*34			P5-36
-V14	P2*41	P2-41	P2*41					P2*41			P5-38
-V15	P2*42	P2-42	P2*42					P2*42			P5-40

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
-V2	P2*11	P2-13	P2*13					P2* 9			P5-14
-V3	P2*16	P2-16	P2*16					P2*12			P5-16
-V4	P2*18	P2-18	P2*18					P2*18			P5-18
-V5	P2*17	P2-17	P2*17					P2*17			P5-20
-V6	P2*27	P2-27	P2*27					P2*27			P5-22
-V7	P2*28	P2-28	P2*28					P2*28			P5-24
-V8	P2*29	P2-29	P2*29					P2*29			P5-26
-V9	P2*30	P2-30	P2*30					P2*30			P5-28
A0					P2*29		P2-29				
A1					P2*30		P2-30				
A15					P2*34		P2-34				
ALPHA				P2-12		P2*12					
AT01							P1* 1		P1- 1		
AT02							P1*10		P1-10		
B14	P2- 7			P2* 7			P2- 7				
B15	P2- 8			P2* 8			P2- 8				
BCMP							P2*63	P2-62			
BMCUPRTY								P1-75	P1-75	P1*66	
BMUX								P1* 1			
BNDV	P2-14				P2*27			P2-71			
BPENDING				P2-54				P2*52			
BUSOP1			P1*70						P1-72		
CCPX	P1-16			P1*16	P1-16			P1-16			
CIK12						P1-58		P1*58			
CIK13						P1-57		P1*62			
CIK14						P1-65		P1*64			
CIK15						P1-66		P1*66			
CIK4						P1-49		P1*49			
CIK7					P1-48			P1*50			
CIK8					P1-56			P1*56			
CLK	P1-67			P1*76	P1-76			P1-42	P1-48	P1-48	
CLKENB	P1*61			P1-61							
CMUX	P2-51							P2*64			
CNTRMAX				P2-59			P2*59				
CPUIN								P1-38	P1*38		
CPUSEL							P1-24		P1*24		
CPUTIMER	P1-29				P1*33			P1-29	P1-30		
DATAPOLL										P1* 1	
DISPFLG	P1-46				P1*46			P1-46			
DPUP						P1-72			P1*71		
DS						P2-27		P2*25			
DVSB				P2-56	P2*57						
EMULATOR			P1*30				P1-25		P1-16		
ENABLE									P1-70	P1*62	
ENABLE0									P2-15		P2-40
ENABLE1									P2-19		P2-41
ENABLE2									P2-17		P2-42
ENABLE3									P2-23		P2-43
ENABLE4									P2*21		P2-44
ENABLE5									P2*25		P2-45

Table 4-1. Backplane Wiring List (Continued)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
ENTIMER	P1*31				P1-31				P1-44		P1- 1
EXTCLK				P1-67							
EXTINT								P1-10		P1*10	
FCLK	P2- 1			P2* 1	P2- 1	P2- 1	P2- 1	P2- 1			
FIELD2					P1*27				P1-14		
FIELD4					P1*29				P1-21		
FIELD5					P1*28				P1-19		
FIELD7					P1*26				P1- 8		
FLAG1	P1-58			P1*58	P1-58						
FLAG2	P1-73			P1*73	P1-73						
FLAG3	P2-37			P2-37	P2*33						
FROM0									P2*16		P2-25
FROM1									P2*22		P2-26
FROM2									P2*12		P2-27
GND											
ICSFLG	P1-47				P1*47		P1-27	P1-47			
ILGADR							P1*29		P1-28		
INCNAMER				P1*13		P1-16					
INCP				P2*19			P2-25				
INDIRECT				P2-73				P2*72			
INTCLKM	P1*64			P1-64							
INTG	P2-22			P2*50				P2-51			
INTPOLL										P1*79	
INTRP	P1-63			P2-51				P2*65			
IOERR									P2-50	P2*50	
IOHR									P2-58	P2*58	
IOHREQ									P2*57	P2-57	
IOHSEL									P2*53	P2-53	
IOINP	P2-49								P2*56	P2-56	
IOLR									P2-70	P2*70	
IOLREQ									P2*68	P2-68	
IOLSEL									P2*54	P2-54	
IOMOP0									P2-51	P2*51	
IOMOP1									P2-52	P2*52	
IORESET										P1*33	P1- 8
IOSEL									P2*59		
IOSPF									P2*55	P2-55	
IOTO1									P2-74	P2*74	
IOTO2									P2-72	P2*72	
JLUIM				P2*71				P2-54			
JMP1G	P1-72		P1-77	P1*72							
JMP2G	P1-62		P2-43	P2*45					P2-44		
LDBREG	P1*70			P1-66							
LUTG	P2-79			P2*72				P2-73			
MCUCMP	P1-42							P1*41			
MCUD0							P1*55	P1-55		P1*55	P2- 2
MCUD1							P1*59	P1-59		P1*59	P2- 3
MCUD10							P1*76	P1-76		P1*76	P2-13
MCUD11							P1*70	P1-70		P1*70	P2-15
MCUD12							P1*68	P1-68		P1*68	P2-16

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
MCUD13							P1*73	P1-73		P1*73	P2-17
MCUD14							P1*71	P1-71		P1*71	P2-18
MCUD15							P1*77	P1-77		P1*77	P2-19
MCUD2							P1*57	P1-57		P1*57	P2- 4
MCUD3							P1*63	P1-63		P1*63	P2- 5
MCUD4							P1*61	P1-61		P1*61	P2- 6
MCUD5							P1*65	P1-65		P1*65	P2- 7
MCUD6							P1*69	P1-69		P1*69	P2- 9
MCUD7							P1*67	P1-67		P1*67	P2-10
MCUD8							P1*74	P1-74		P1*74	P2-11
MCUD9							P1*72	P1-72		P1*72	P2-12
MCUDPRTY							P1*75			P1*75	P2-20
MCUERR								P1-25	P1*25		
MCUFRZ						P1-37			P1*18		
MEMREF					P1-48			P1*48			
MODINT								P1- 9	P1* 7		
MOP0									P2*14		P2-28
MOP1									P2*10		P2-29
MPIC0	P2* 5			P2-47							
MPIC1	P2* 6			P2- 6							
NAMER0					P1*25						
NAMER1					P1*26						
NEXT				P2*43	P2-41		P2-42	P2-44			
NIP	P1-43							P1-43	P1*43		
NIPD									P1* 9		
NIPSEL									P1*64		
NIRTOCIR				P1*49				P1-37	P1-37		
NOP2	P2-76			P2*76	P2-76		P2-76				
NOTUSED											P1-10
NUMERIC				P2-16		P2*17					
NXT+1	P2-59			P2*67		P2-64		P2-67			
OFCENB				P2-69	P2*69						
OPINP	P1-35							P1-35	P1*35		
OPNDSEL									P1*63		
OVFLINT				P1*63				P1-26			
P1-14										P1-38	P1-14
P1-20										P1-45	P1-20
P1-3										P1-27	P1- 3
P1-4										P1-25	P1- 4
P3-45										P2-66	P3-45
PADDIN10						P2-57		P2*57			
PADDIN11						P2-59		P2*59			
PADDIN8						P2-53		P2*53			
PADDIN9						P2-55		P2*55			
PADDSUB						P2-61		P2*61			
PADDXS00						P2-63		P2*63			
PADDXS01						P2-65		P2*65			
PAUSE								P1*45			
PONB					P2*74	P2-76		P2-74			
PONUR				P2-41	P2*45						

Table 4-1. Backplane Wiring List (Continued)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BLS
PWRFAIL					P1*30			P1-30			
PWRON					P1-25						P1- 6
QASL					P2*64		P2-64				
QASR					P2*62	P2-62					
QDWN						P1*31	P1-31				
QS				P2-29		P2-29		P2*26			
R0			P1*12		P1-12	P1*12					
R1			P1*11		P1-11	P1*11					
R10			P2* 8		P2- 8	P2* 8					
R11			P2* 7		P2- 7	P2* 7					
R12			P2*47		P2-47	P2*47					
R13			P2*48		P2-48	P2*48					
R14			P2*49		P2-49	P2*49					
R15			P2*51		P2-51	P2*51					
R2			P1* 9		P1- 9	P1* 9					
R3			P1*10		P1-10	P1*10					
R4			P1*61		P1-61	P1*61					
R5			P1*62		P1-62	P1*62					
R6			P1*63		P1-63	P1*63					
R7			P1*64		P1-64	P1*64					
R8			P2*10		P2-10	P2*10					
R9			P2* 9		P2- 9	P2* 9					
RARGA	P2-47		P2-46	P2*46							
RARGB	P2-15		P2-15	P2*15							
RDCIR						P1*28		P1-28			
RDCPX1							P2*43	P2-43	P2-43		
RDCPX2							P2*45	P2-45			
RDIOD							P2*47			P2-47	
RDMOD							P2*46		P2-46		
RDOPND							P2*49	P2-49	P2-49		
RDSWITCH							P2*50	P2-50			
READY0									P2*31		P2-33
READY1									P2*32		P2-34
READY2									P2* 9		P2-35
READY3									P2*29		P2-36
READY4									P2*13		P2-37
READY5									P2*11		P2-38
READY6									P2*30		P2-31
REPEAT	P2-21			P2*21							
REVSYSP					P1*38				P1-73		
RF0	P2*56		P2*56			P2*56					
RF1	P2*54		P2*54			P2*54					
RF2	P2*52		P2*52			P2*52					
RF3	P2*50		P2*50			P2*50					
RFSAME					P2-58	P2*58					
RMOP0	P2- 3								P2*33		
RMOP1	P2- 4								P2*34		
ROM0			P1* 4	P1* 4							P4- 2
ROM1			P1* 3	P1* 3							P4- 3
ROM10			P1*32	P1*32							P4-17

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BLS
ROM11		P1*33	P1*33								P4-18
ROM12		P1*35	P1*35								P4-20
ROM13		P1*34	P1*34								P4-21
ROM14		P1*36	P1*36								P4-23
ROM15		P1*38	P1*38								P4-24
ROM16		P1*41	P1*41								P4-27
ROM17		P1*42	P1*42								P4-28
ROM18		P1*43	P1*43								P4-30
ROM19		P1*44	P1*44								P4-31
ROM2		P1*21	P1*21								P4- 5
ROM20		P1*45	P1*45								P4-33
ROM21		P1*46	P1*46								P4-34
ROM22		P1*47	P1*47								P4-36
ROM23		P1*4A	P1*48								P4-37
ROM24		P1*51	P1*51								P4-39
ROM25		P1*52	P1*52								P4-40
ROM26		P1*53	P1*53								P4-42
ROM27		P1*54	P1*54								P4-43
ROM28		P1*65	P1*65								P4-45
ROM29		P1*67	P1*67								P4-46
ROM3		P1*24	P1*24								P4- 6
ROM30		P1*69	P1*69								P4-48
ROM31		P1*71	P1*71								P4-49
ROM4		P1*23	P1*23								P4- 8
ROM5		P1*25	P1*25								P4- 9
ROM6		P1*27	P1*27								P4-11
ROM7		P1*26	P1*26								P4-12
ROM8		P1*28	P1*28								P4-14
ROM9		P1*31	P1*31								P4-15
ROMENB		P2- 6	P2- 6								P5- 8
ROMFNCT2								P1*67			P1-67
ROR10			P1*72					P1-66			
ROR11			P1*73					P1-68			
ROR12			P1*74					P1-71			
ROR13			P1*75					P1-72			
ROR14			P1*76					P1-75			
ROR23			P2* 5	P2- 5							
ROR24			P2*24	P2-24							
RORT10	P2-44							P2*44			
RORT11	P2-43							P2*43			
RORT12	P2-24							P2*24			
RORT13	P2-25							P2*25			
RORT14	P2-46							P2*46			
RORT15	P2-53		P2*53	P2-53					P2-53		
RORT16	P2-55		P2*55	P2-55					P2-55		
RORT17	P2-58		P2*58	P2-58					P2-58		
RORT18	P2-57		P2*57	P2-57					P2-57		
RORT19	P2-62		P2*62	P2-62					P2-62		
RORT20	P1-57		P1*57					P1-57			
RORT21	P1-49		P1*49					P1-49			

Table 4-1. Backplane Wiring List (Continued)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
RORT22	P1-50		P1*50		P1-50						
RORT23	P2-61		P2*61	P2-61					P2-61		
RORT24	P2-63		P2*63	P2-63					P2-63		
RORT25	P2-64		P2*64	P2-64					P2-64		
RORT26	P2-65		P2*65	P2-65					P2-65		
RORT27	P2-77		P2*77	P2-75					P2-77		
RPTFCN				P2-10	P2*12						
RREG0				P1-51	P1*42						
RUNFF	P1-36						P1-26	P1*34			
S0					P1- 3	P1* 3	P1* 3	P1* 3	P1* 3	P1* 3	
S1					P1- 4	P1* 4	P1* 4	P1* 4	P1* 4	P1* 4	
S10					P2- 5	P2* 5	P2* 5	P2* 5	P2* 5	P2* 5	
S11					P2- 6	P2* 6	P2* 6	P2* 6	P2* 6	P2* 6	
S12					P2-38	P2*38	P2*38	P2*38	P2*38	P2*38	
S13					P2-37	P2*37	P2*37	P2*37	P2*37	P2*37	
S14					P2-36	P2*36	P2*36	P2*36	P2*36	P2*36	
S15					P2-35	P2*35	P2*35	P2*35	P2*35	P2*35	
S2					P1- 5	P1* 5	P1* 5	P1* 5	P1* 5	P1* 5	
S3					P1- 6	P1* 6	P1* 6	P1* 6	P1* 6	P1* 6	
S4					P1-54	P1*54	P1*54	P1*54	P1*54	P1*54	
S5					P1-53	P1*53	P1*53	P1*53	P1*53	P1*53	
S6					P1-52	P1*52	P1*52	P1*52	P1*52	P1*52	
S7					P1-51	P1*51	P1*51	P1*51	P1*51	P1*51	
S8					P2- 3	P2* 3	P2* 3	P2* 3	P2* 3	P2* 3	
S9					P2- 4	P2* 4	P2* 4	P2* 4	P2* 4	P2* 4	
SAVEG	P2-45		P2-44	P2*44							
SCMD	P1-52									P1*50	
SDFG				P1*71	P1-70						
SF0	P2*66		P2*66			P2*66	P2-66				
SF1	P2*68		P2*68			P2*68	P2-68				
SF2	P2*70		P2*70			P2*70	P2-70				
SF3	P2*72		P2*72			P2*72	P2-72				
SF4	P2*74		P2*74			P2*74	P2-74				
SFSAME					P2-28		P2*28				
SHIFTCLK	P1*23				P1-23	P1-23		P1-23	P1-23	P1-24	
SIPG				P1*69	P1-69						
SIODR	P1-48									P1*49	
SIODR	P1-24									P1*30	
SIOMAP	P1-25									P1*31	
SIOP	P1- 9									P1* 9	
SKIP	P2-26		P2-26	P2*27		P2-26					
SKIPMOP1			P1*13	P1- 9							
SMCU	P1-27							P1*33			
SP1 0					P1- 1	P1* 1	P1- 9				
SP115					P2-31	P2*30					
SP1IN					P2*42	P2-42					
SP1SHIFT					P1*45	P1-45					
SP3 0					P2-54		P2*54				
SP315					P2-26	P2-25	P2*26				
SP3IN					P1*15		P1-15				

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
SP3SHIFT					P2*61		P2-61				
SPCLNOP1			P2*25	P2-25							
SPETFM	P1-66								P2*66		
SR0				P2-34		P2*34		P2-47			
SR1				P2-33		P2*33		P2-48			
SR2				P2-31		P2*31		P2-46			
SRBUS	P1-44					P1*44					
SRDYENB	P1-69								P1*69		
SRREG	P1-71				P2*52						
SSBUS	P1-41					P1*41					
SSREG	P1-76				P2*50						
ST0	P2*67		P2*67			P2-67	P2-67				
ST1	P2*69		P2*69			P2-69	P2-69				
ST2	P2*71		P2*71			P2-71	P2-71				
ST3	P2*73		P2*73			P2-73	P2-73				
ST4	P2*75		P2*75			P2-75	P2-75				
STATUS0				P1*41	P1-41		P1-41				
STATUS1				P1*42			P1-42		P1-42	P1-42	
STATUS2				P1*43			P1-43				
STATUS3				P1*44			P1-44	P1-44			
STATUS4				P1*45			P1-45				
STATUS5				P1*46			P1-46				
STATUS6				P1*47			P1-47				
STATUS7				P1*48			P1-48				
STBUSOP				P1-62				P1*62			
STIOA							P1*11			P1-11	
STIOD							P1*16			P1-16	
STORAR				P1-70		P1*70					
STSTATUS				P2-79			P2*79	P2-77			
SUBF	P2-48			P2*49							
SUBUS	P1-55					P1*55					
SYSPTN							P1-49		P1-49		
SYSPRTY							P2* 9		P2- 8		P2-32
T0				P1-55	P1*55						
TNAME00	P1-32					P1*32	P1-32				
TNAME01	P1-33					P1*33	P1-33				
T00									P2*28		P2-22
T01									P2*24		P2-23
T02									P2*26		P2-24
U0	P1- 8			P1- 8	P1* 8	P1- 8	P1- 8	P1- 8		P1- 8	
U1	P1-14			P1-14	P1*14	P1-14	P1-14	P1-14		P1-14	
U10					P2*15	P2-15	P2-15	P2-15	P1-55	P2-15	
U11					P2*16	P2-16	P2-16	P2-16	P1-56	P2-16	
U12					P2*19	P2-19	P2-19	P2-19		P2-19	
U13					P2*21	P2-21	P2-21	P2-21	P1-57	P2-21	
U14	P2-19			P2-22	P2*22	P2-22	P2-22	P2-22	P1-58	P2-22	
U15				P2-23	P2*23	P2-23	P2-23	P2-23	P1-59	P2-23	
U2				P1- 7	P1* 7	P1- 7	P1- 7	P1- 7		P1- 7	
U3				P1-17	P1*17	P1-17	P1-17	P1-17		P1-17	
U4				P1-18	P1*18	P1-18	P1-18	P1-18		P1-18	

Table 4-1. Backplane Wiring List (Continued)

SIGNAL	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1A10	BUS
U5				P1-19	P1*19	P1-19	P1-19	P1-19		P1-19	
U6				P1-21	P1*21	P1-21	P1-21	P1-21		P1-21	
U7				P1-22	P1*22	P1-22	P1-22	P1-22		P1-22	
U8				P2-13	P2*13	P2-13	P2-13	P2-13		P2-13	
U9					P2*14	P2-14	P2-14	P2-14		P2-14	
UGATE	P2-36			P2*35				P2-24			
VBUSENB	P1-74	P2- 4	P2- 4	P2- 4				P2-10			P5- 6
W								P2*76			
XSW14	P1*75			P2-11			P2-11				
XSW15	P1*77			P1-77			P2-10				

Table 4-2. IOP/Power Bus (Non-Memory Card Cage)

PIN NO.		SIGNAL	PIN NO.		SIGNAL
56-PIN	20-PIN		56-PIN	20-PIN	
1		+5V	30		▽
2		+5V	31		Not used
3		+5V	32		Not used
4		+5V	33		Not used
5	2	$\overline{\text{PF WARN}}$	34		Not used
6	1	ENTIMER	35		Not used
7	4	SPARE	36		Not used
8	3	SPARE	37		Not used
9	6	PWR ON	38		Not used
10	5	PWR ON ▽	39		Not used
11	8	IORESET	40		Not used
12	7	IORESET ▽	41	12	$\overline{\text{HSREQ}}$
13	10	$\overline{\text{MCUCLKS}}$ (Note 2)	42	11	▽
14	9	$\overline{\text{MCUCLKS}}$ ▽	43		See note 1
15		▽	44		See note 1
16		▽	45	14	SPARE
17		-5V	46	13	SPARE ▽
18		-5V	47		See note 1
19		▽	48		See note 1
20		▽	49	16	$\overline{\text{SI}}$
21		▽	50	15	$\overline{\text{SI}}$ ▽
22		▽	51		See note 1
23		Not used	52		See note 1
24		Not used	53	18	$\overline{\text{SO}}$
25		Not used	54	17	$\overline{\text{SO}}$ ▽
26		Not used	55		See note 1
27		Not used	56		See note 1
28		Not used		20	Not used
29		▽		19	Not used

Note 1: Reserved for interrupt and data poll connections at backplane.
2: On pin 13 of 56-pin connectors only. Pin 10 of 20-pin is isolated.

Table 4-3. Central Data Bus

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	FROM 1
2	MCUD 0	27	FROM 2
3	MCUD 1	28	MOP 0
4	MCUD 2	29	MOP 1
5	MCUD 3	30	▽
6	MCUD 4	31	READY 6
7	MCUD 5	32	SYSPRTY
8	▽	33	READY 0
9	MCUD 6	34	READY 1
10	MCUD 7	35	READY 2
11	MCUD 8	36	READY 3
12	MCUD 9	37	READY 4
13	MCUD 10	38	READY 5
14	▽	39	▽
15	MCUD 11	40	ENABLE 0
16	MCUD 12	41	ENABLE 1
17	MCUD 13	42	ENABLE 2
18	MCUD 14	43	ENABLE 3
19	MCUD 15	44	ENABLE 4
20	MCUDPRTY	45	ENABLE 5
21	▽	46	▽
22	TO 0	47	$\overline{\text{APE}}$
23	TO 1	48	$\overline{\text{SYSPE}}$
24	TO 2	49	$\overline{\text{MCURST}}$
25	FROM 0	50	▽

Note: CPU/IOP connector P2

Table 4-4. IOP Bus

PIN	SIGNAL	PIN	SIGNAL
1	IODPRTY	26	IOD 4
2	IODPE	27	IOD 5
3	▽	28	▽
4	IOCMD 00	29	IOD 6
5	IOCMD 02	30	IOD 7
6	IOCMD 01	31	▽
7	▽	32	IOD 8
8	DEVNO 0	33	IOD 9
9	DEVNO 1	34	▽
10	▽	35	IOD 10
11	DEVNO 2	36	IOD 11
12	DEVNO 3	37	▽
13	▽	38	IOD 12
14	DEVNO 4	39	IOD 13
15	DEVNO 5	40	▽
16	▽	41	IOD 14
17	DEVNO 6	42	IOD 15
18	DEVNO 7	43	▽
19	▽	44	INTREQ
20	IOD 0	45	Spare
21	IOD 1	46	▽
22	▽	47	IOX 14
23	IOD 2	48	IOX 15
24	IOD 3	49	▽
25	▽	50	INTACK

Note: CPU/IOP connector P3

Table 4-5. Current Instruction Register Connector A8J1

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	CIR 6 Buffered
2	SYSTEM SW REG 0	27	CIR 7 Buffered
3	SYSTEM SW REG 1	28	PON BUF
4	SYSTEM SW REG 2	29	CIR 8 Buffered
5	SYSTEM SW REG 3	30	CIR 9 Buffered
6	SYSTEM SW REG 4	31	CIR 10 Buffered
7	SYSTEM SW REG 5	32	CIR 11 Buffered
8	SYSTEM SW REG 6	33	CIR 12 Buffered
9	SYSTEM SW REG 7	34	CIR 13 Buffered
10	▽	35	CIR 14 Buffered
11	SYSTEM SW REG 8	36	CIR 15 Buffered
12	SYSTEM SW REG 9	37	▽
13	SYSTEM SW REG 10	38	INHAR
14	SYSTEM SW REG 11	39	SYSHFF
15	SYSTEM SW REG 12	40	RUNFF
16	SYSTEM SW REG 13	41	▽
17	SYSTEM SW REG 14	42	RUNSW
18	SYSTEM SW REG 15	43	▽
19	▽	44	LDSW
20	CIR 0 Buffered	45	▽
21	CIR 1 Buffered	46	DUMPSW
22	CIR 2 Buffered	47	▽
23	CIR 3 Buffered	48	IORSTSW
24	CIR 4 Buffered	49	▽
25	CIR 5 Buffered	50	CPURST

Note: Connector A8J1 is cabled to operator's panel on front door.

Table 4-5A. Current Instruction Register Connector A8J2

PIN	SIGNAL	PIN	SIGNAL
1	⏚	26	LDREG
2	PANEL SW REG 0	27	LDADDR
3	PANEL SW REG 1	28	⏚
4	PANEL SW REG 2	29	DISPMEM
5	PANEL SW REG 3	30	LDMEM
6	PANEL SW REG 4	31	⏚
7	PANEL SW REG 5	32	EXECUTE
8	PANEL SW REG 6	33	SINGLE
9	PANEL SW REG 7	34	⏚
10	⏚	35	INCRADDR
11	PANEL SW REG 8	36	DECADDR
12	PANEL SW REG 9	37	⏚
13	PANEL SW REG 10	38	Not used
14	PANEL SW REG 11	39	SYS HALT FF
15	PANEL SW REG 12	40	RUNFF
16	PANEL SW REG 13	41	⏚
17	PANEL SW REG 14	42	RUNSW
18	PANEL SW REG 15	43	⏚
19	⏚	44	LDSW
20	Not used	45	⏚
21	Not used	46	DUMPSW
22	⏚	47	⏚
23	PSRENB	48	IORSTSW
24	INHRINT	49	⏚
25	⏚	50	CPURST

NOTE: Cabled to A1J2 of the CPU card cage when using the maintenance panel.

Table 4-6. Multiplexer Channel Bus

PIN	SIGNAL	PIN	SIGNAL
1	CHANSO	26	SR 10
2	⏚	27	SR 11
3	SRCLOCK	28	SR 12
4	⏚	29	SR 13
5	DEVEND	30	⏚
6	⏚	31	SR 14
7	ACKSR	32	SR 15
8	⏚	33	SR 0
9	CHANACK	34	SR 1
10	⏚	35	SR 2
11	DEVNODB	36	⏚
12	SIO ENABLE	37	SR 3
13	EOT	38	SR 4
14	JMPMET	39	SR 5
15	⏚	40	SR 6
16	TOGGLE INXFER	41	SR 7
17	TOGGLE SR	42	⏚
18	TOGGLE OUTXFER	43	PCMD1
19	TOGGLE SIO OK	44	SETJMP
20	⏚	45	PSTATSTB
21	XFER ERROR	46	PCONTSTB
22	REQ	47	READ NEXT WD
23	⏚	48	PWRITESTB
24	SR 8	49	SETINT
25	SR 9	50	PREADSTB

Note: Multiplexer channel connector P2

Figure 4-1. HP 30036A Multiplexer Channel Cabling is deleted. System cabling is shown elsewhere as follows:
Figure 4-3B. System Flat Cables, Model 6
Figure 4-3D. System Flat Cables, Model 8
Figure 4-3F. System Flat Cables, Model 5 or 7
Figure 4-3H. System Flat Cables, Model 9

Figure 4-2. HP 30030B Selector Channel Cabling is deleted. System cabling is shown as follows:
Figure 4-3B. System Flat Cables, Model 6
Figure 4-3D. System Flat Cables, Model 8
Figure 4-3F. System Flat Cables, Model 5 or 7
Figure 4-3H. System Flat Cables, Model 9

Table 4-7. Port Controller Bus

PIN	SIGNAL	PIN	SIGNAL
1	$\overline{\text{ERR1}}$	26	PCD 0
2	LSEL1	27	PCD 1
3	▽	28	▽
4	HSEL1	29	PCD 2
5	STRB1	30	PCD 3
6	$\overline{\text{CWREQ1}}$	31	▽
7	▽	32	PCD 4
8	$\overline{\text{RRREQ1}}$	33	PCD 5
9	TO1-1	34	▽
10	▽	35	PCD 6
11	TO1-2	36	PCD 7
12	$\overline{\text{ERR2}}$	37	▽
13	▽	38	PCD 8
14	LSEL2	39	PCD 9
15	HSEL2	40	▽
16	▽	41	PCD 10
17	$\overline{\text{STRB2}}$	42	PCD 11
18	$\overline{\text{CWREQ2}}$	43	▽
19	▽	44	PCD 12
20	RRREQ2	45	PCD 13
21	TO2-1	46	▽
22	▽	47	PCD 14
23	TO2-2	48	PCD 15
24	Not used	49	▽
25	▽	50	PCDPRTY

Note: Port Controller Connector P3

Table 4-8. Selector Channel Bus

PIN	SIGNAL	A	B	C	PIN	SIGNAL	A	B	C
1	$\overline{\text{CHAN SO}}$			O	26	SR 13	I		
2	▽				27	SR 12	I		
3	$\overline{\text{SR CLOCK}}$			O	28	SR 11	I		
4	▽				29	SR 10	I		
5	$\overline{\text{DEVEND}}$			I	30	▽			
6	▽				31	SR 9	I		
7	$\overline{\text{ACK SR}}$			O	32	SR 8	I		
8	▽				33	SR 7	I		
9	$\overline{\text{CHANACK}}$			I	34	SR 6	I		
10	▽				35	SR 5	I		
11	$\overline{\text{DEVNO DB}}$			O	36	▽			
12	$\overline{\text{SIO ENABLE}}$		O		37	SR 4	I		
13	$\overline{\text{EOT}}$			O	38	SR 3	I		
14	$\overline{\text{JMP MET}}$			I	39	SR 2	I		
15	▽				40	SR 1	I		
16	TOGGLE INXFER			O	41	SR 0	I		
17	CHAN SR			I	42	▽			
18	TOGGLE OUTXFER			O	43	$\overline{\text{PCMD 1}}$			O
19	TOGGLE SIO OK			O	44	$\overline{\text{SET JMP}}$			O
20	▽				45	$\overline{\text{PSTATUSSTB}}$			O
21	$\overline{\text{XFER ERROR}}$			O	46	$\overline{\text{PCONTSTB}}$			O
22	$\overline{\text{REQ}}$		I		47	$\overline{\text{RDNEXTWD}}$			O
23	▽				48	$\overline{\text{PWRITESTB}}$			O
24	SR 15	I			49	$\overline{\text{SET INT}}$			O
25	SR 14	I			50	$\overline{\text{PREADSTB}}$			O

Note: Selector Channel connectors P2.
I = Input
O = Output
A = Register PCA
B = Sequencer PCA
C = Control PCA

Table 4-9. Selector Channel Connectors J1

PIN	SIGNAL	A	B	C	PIN	SIGNAL	A	B	C
1	$\overline{\text{FREEZE}}$	I	I	O	26	$\overline{\text{LD BANK}}$	I	I	I
2	$\overline{\text{RESET}}$		O	I	27	▽			
3	▽				28	$\overline{\text{RRREQ}}$	I	O	
4	WPB	I	O		29	$\overline{\text{WBA1}}$	I	O	I
5	WBB2	I	O	I	30	▽			
6	▽				31	WAIT	O		
7	WBA2	I	O	I	32	$\overline{\text{XERR}}$		I	O
8	$\overline{\text{SENSEACK}}$		I	O	33	▽			
9	▽				34	$\overline{\text{WBB1}}$	I	O	
10	$\overline{\text{CW1}}$	I		O	35	$\overline{\text{CWREQ}}$	I	O	
11	$\overline{\text{TRB1FF}}$	I	O		36	▽			
12	▽				37	$\overline{\text{IOP CNT DATA}}$	I	O	I
13	$\overline{\text{JUMPFF}}$	I		O	38	$\overline{\text{DATA IN ACK}}$		I	O
14	$\overline{\text{CH ACTIVE}}$				39	▽			
15	▽				40	$\overline{\text{RRDATA}}$	I	O	
16	$\overline{\text{TRB2FF}}$	I	O	I	41	$\overline{\text{PCRST}}$	I	O	
17	$\overline{\text{AWB WAIT}}$	I	O		42	▽			
18	▽				43	$\overline{\text{IOP CNT WAIT}}$	I	O	
19	$\overline{\text{CWB WAIT}}$	I	O		44	$\overline{\text{PFS ENB}}$		I	O
20	$\overline{\text{WT}}$		I	O	45	▽			
21	▽				46	INCWC	I		O
22	$\overline{\text{DATA OUT}}$	I		O	47	ADR	O		
23	$\overline{\text{IOCW WAIT}}$	I	O		48	▽			
24	▽				49	$\overline{\text{DATA OUT ACK}}$		I	O
25	$\overline{\text{IOAW WAIT}}$	I	O		50	$\overline{\text{GO ACTIVE}}$		O	I

Note: I = Input
O = Output
A = Register PCA
B = Sequencer PCA
C = Control PCA

Table 4-10. Selector Channel Connectors J2

PIN	SIGNAL	A	B	C	PIN	SIGNAL	A	B	C
1	$\overline{\text{FS ENB}}$		I	O	26	RBB 2	I	O	I
2	$\overline{\text{TRB ENB}}$		I	O	27	▽			
3	▽				28	$\overline{\text{RBB1}}$	I	O	I
4	LA	O	I		29	$\overline{\text{ENDB}}$		I	O
5	$\overline{\text{IOP CNT DN}}$	I	O		30	▽			
6	▽				31	$\overline{\text{DEVNO ADR}}$	I	O	
7	DPE	O		I	32	$\overline{\text{IOAW ADR}}$	I	O	
8	DATA	O	I		33	▽			
9	▽				34	RBA2	I	O	I
10	WCTC	O	I	I	35	CW2	I		O
11	IOCW 4	O		I	36	▽			
12	▽				37	RBP	I	O	
13	IOCW 0	O		I	38	$\overline{\text{HSEL}}$	O	I	
14	IOCW 1	O		I	39	▽			
15	▽				40	$\overline{\text{LDRR}}$	I		O
16	IOCW 2	O		I	41	STRB	O	I	
17	IOCW 3	O		I	42	▽			
18	▽				43	$\overline{\text{LSEL}}$	O	I	
19	$\overline{\text{WFRTC}}$		I	O	44	$\overline{\text{WCRO}}$	I	I	O
20	$\overline{\text{INTCLRIL}}$		I	O	45	▽			
21	▽				46	PC ERR	O		I
22	$\overline{\text{RBA 1}}$	I	O	I	47	ILL ADR	O	I	O
23	$\overline{\text{LD DEVNO}}$	I	O		48	▽			
24	▽				49	$\overline{\text{RESREQ}}$		I	O
25	$\overline{\text{IOP CNT ADR}}$	I	O		50	$\overline{\text{KEND}}$		O	I

Note: I = Input
O = Output
A = Register PCA
B = Sequencer PCA
C = Control PCA

Figure 4-3. Memory Cabling is deleted. System cabling is shown elsewhere as follows:
Figure 4-3B. System Flat Cables, Model 6
Figure 4-3D. System Flat Cables, Model 8
Figure 4-3F. System Flat Cables, Model 5 or 7
Figure 4-3H. System Flat Cables, Model 9

Table 4-11. Memory Connectors J1

PIN	SIGNAL	PIN	SIGNAL
1		26	MDI 04
2	MDO 00	27	
3		28	MDI 05
4	MDO 01	29	
5		30	MDI 06
6	MDO 02	31	
7		32	MDI 07
8	MDO 03	33	
9		34	$\overline{\text{ENAEC}}$
10	MDO 04	35	
11		36	CKA
12	MDO 05	37	
13		38	CKB
14	MDO 06	39	
15		40	CKC
16	MDO 07	41	
17		42	CKD
18	MDI 00	43	
19		44	$\overline{\text{CKD}}$
20	MDI 01	45	
21		46	CKE
22	MDI 02	47	
23		48	$\overline{\text{CKE}}$
24	MDI 03	49	
25		50	$\overline{\text{ENACK}}$

Table 4-12. Memory Connectors J2

PIN	SIGNAL	PIN	SIGNAL
1		26	$\overline{\text{AD 08}}$
2	R/$\overline{\text{W}}$ CNTRL TIMING	27	
3		28	$\overline{\text{AD 09}}$
4	$\overline{\text{DATA OUT ENB}}$	29	
5		30	AD 10
6	TP1	31	
7		32	AD 11
8	TP2	33	
9		34	AD 12
10	TP3	35	
11		36	AD 13
12	TP4	37	
13		38	AD 14
14	$\overline{\text{MEM PROTECT}}$	39	
15		40	AD 15
16	$\overline{\text{REFRESH CLK}}$	41	
17		42	TP5
18	$\overline{\text{AD 04}}$	43	
19		44	$\overline{\text{PAR}}$
20	$\overline{\text{AD 05}}$	45	
21		46	$\overline{\text{DISACK}}$
22	$\overline{\text{AD 06}}$	47	
23		48	Not Used
24	$\overline{\text{AD 07}}$	49	
25		50	$\overline{\text{READCLK}}$

Table 4-13. Memory Connectors J3

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	MDO 13
2	WRITE CLK	27	▽
3	▽	28	MDO 14
4	WRITE ENB	29	▽
5	▽	30	MDO 15
6	AR1	31	▽
7	▽	32	MDO PRTY
8	AD 01	33	▽
9	▽	34	MDI 08
10	AD 02	35	▽
11	▽	36	MDI 09
12	AD 03	37	▽
13	▽	38	MDI 10
14	AR0	39	▽
15	▽	40	MDI 11
16	MDO 08	41	▽
17	▽	42	MDI 12
18	MDO 09	43	▽
19	▽	44	MDI 13
20	MDO 10	45	▽
21	▽	46	MDI 14
22	MDO 11	47	▽
23	▽	48	MDI 15
24	MDO 12	49	▽
25	▽	50	MDI PRTY

Table 4-14. IOP/Power Bus (Memory Module)

PIN NO.		SIGNAL	PIN NO.		SIGNAL
56-PIN	20-PIN		56-PIN	20-PIN	
1		+5V	30		▽
2		+5V	31		-5VB
3		+5V	32		-5VB
4		+5V	33		◁ Feedthru
5	2	PF WARN	34		◁
6	1	ENTIMER	35		+5VB
7	4	SPARE	36		+5VB
8	3	SPARE	37		+12VB
9	6	PWR ON	38		+12VB
10	5	PWR ON ▽	39		+12.7VB
11	8	IORESET	40		+12.7VB
12	7	IORESET ▽	41	12	Not used
13	10	Not used	42	11	Not used
14	9	Not used	43		Not used
15		▽	44		Not used
16		▽	45	14	Not used
17		Not used	46	13	Not used
18		Not used	47		Not used
19		▽	48		Not used
20		▽	49	16	SI
21		▽	50	15	SI ▽
22		▽	51		MCUFRCOUT
23		Not used	52		▽
24		Not used	53	18	SO
25		Not used	54	17	SO ▽
26		Not used	55		MCUFRCIN
27		Not used	56		▽
28		Not used		20	Not used
29		▽		19	Not used

Table 4-15. Error Logging Interface Cable

PIN	SIGNAL	PIN	SIGNAL
1	$\overline{\text{DISWEC}}$	26	▽
2	▽	27	ELAD7
3	Spare	28	▽
4	▽	29	ELAD6
5	$\overline{\text{SELECT}}$	30	▽
6	▽	31	ELAD5
7	$\overline{\text{U128K}}$	32	▽
8	▽	33	ELAD4
9	Not used	34	▽
10	▽	35	ELAD0
11	Not used	36	▽
12	▽	37	ELAD1
13	$\overline{\text{ELDS}}$	38	▽
14	▽	39	ELAD2
15	$\overline{\text{ELAV}}$	40	▽
16	▽	41	ELAD3
17	$\overline{\text{SELECTED}}$	42	▽
18	▽	43	$\overline{\text{DATA IN}}$
19	$\overline{\text{ELAW}}$	44	▽
20	▽	45	Not used
21	ELAD8	46	▽
22	▽	47	Not used
23	ELAD9	48	▽
24	▽	49	Not used
25	$\overline{\text{DATA OUT}}$	50	▽

Table 4-15A. Mag Tape Interface Connectors J2

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	Not used
2	▽	27	ROM 16
3	ROM 4	28	ROM 0
4	Not used	29	ROM 17
5	ROM 5	30	ROM 1
6	Not used	31	ROM 18
7	ROM 6	32	ROM 2
8	Not used	33	ROM 19
9	ROM 7	34	ROM 3
10	Not used	35	Not used
11	ROM 8	36	Not used
12	Not used	37	RAR 0
13	ROM 9	38	RAR 1
14	Not used	39	RAR 2
15	ROM 10	40	RAR 3
16	Not used	41	RAR 4
17	ROM 11	42	RAR 5
18	Not used	43	RAR 6
19	ROM 12	44	RAR 7
20	Not used	45	RAR 8
21	ROM 13	46	RAR 9
22	Not used	47	RAR 10
23	ROM 14	48	RAR 11
24	Not used	49	▽
25	ROM 15	50	▽

NOTE: Connects J2s at Magnetic Tape Interface.

Table 4-15B. Mag Tape Interface Connectors J3

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	FLG 5
2	$\overline{\text{CLEAR}}$	27	FLG 2
3	$\overline{\text{TO}}$	28	FLG 3
4	$\overline{\text{T3}}$	29	FLG 0
5	$\overline{\text{T2}}$	30	FLG 1
6	ROR 9	31	Not used
7	UDS	32	EXT SEL
8	INPUT STROBE	33	Not used
9	FLG 10	34	Not used
10	LOS	35	Not used
11	FLG 14	36	Not used
12	FLG 12	37	Not used
13	FLG 16	38	Not used
14	FLG 15	39	$\overline{\text{T1}}$
15	ROR 8	40	Not used
16	FLG 17	41	Not used
17	ROR 11	42	Not used
18	ROR 7	43	Not used
19	WT1	44	Not used
20	ROR 10	45	Not used
21	FLG 13	46	Not used
22	FLG 11	47	Not used
23	FLG 6	48	Not used
24	FLG 7	49	Not used
25	FLG 4	50	▽

NOTE: Connects J3s at Magnetic Tape Interface

Table 4-15C. Mag Tape Interface to Tape Unit

PIN	SIGNAL	PIN	SIGNAL
1	Not used	26	Not used
2	$\overline{\text{SINGLE TRACK ERROR}}$	27	Not used
3	$\overline{\text{SELECT COMMAND 0}}$	28	Not used
4	$\overline{\text{SELECT COMMAND 1}}$	29	$\overline{\text{ID BURST}}$
5	$\overline{\text{SELECT COMMAND 2}}$	30	$\overline{\text{WRCLK}}$
6	$\overline{\text{SELECT COMMAND 3}}$	31	$\overline{\text{MULTIPLE TRACK ERROR}}$
7	$\overline{\text{END OF BLOCK}}$	32	$\overline{\text{TAPE MARK}}$
8	$\overline{\text{READ CLOCK}}$	33	$\overline{\text{WRITE DATA 0}}$
9	$\overline{\text{READ DATA PARITY}}$	34	$\overline{\text{WRITE DATA 1}}$
10	$\overline{\text{WRITE DATA PARITY}}$	35	$\overline{\text{WRITE DATA 6}}$
11	$\overline{\text{WRITE RESET}}$	36	$\overline{\text{WRITE DATA 7}}$
12	$\overline{\text{STATUS}}$ (800/1600)	37	$\overline{\text{WRITE DATA 4}}$
13	$\overline{\text{LOAD POINT}}$	38	$\overline{\text{WRITE DATA 5}}$
14	$\overline{\text{READY}}$	39	$\overline{\text{WRITE DATA 2}}$
15	$\overline{\text{FILE PROTECT}}$	40	$\overline{\text{WRITE DATA 3}}$
16	$\overline{\text{END OF TAPE}}$	41	$\overline{\text{READ DATA 6}}$
17	$\overline{\text{FORWARD}}$	42	$\overline{\text{READ DATA 7}}$
18	$\overline{\text{REVERSE}}$	43	$\overline{\text{READ DATA 4}}$
19	$\overline{\text{WRITE}}$	44	$\overline{\text{READ DATA 5}}$
20	$\overline{\text{OFF LINE}}$	45	$\overline{\text{READ DATA 2}}$
21	$\overline{\text{REWIND}}$	46	$\overline{\text{READ DATA 3}}$
22	WRRST	47	$\overline{\text{READ DATA 0}}$
23	Not used	48	$\overline{\text{READ DATA 1}}$
24	Not used	49	Not used
25	Not used	50	Not used

NOTE: Connects J1 of Magnetic Tape Controller Processor to Magnetic Tape Unit.

Table 4-15D. 7905A/7920A Disc Interface to Device Controller

PIN	SIGNAL	PIN	SIGNAL
1	+5V	26	Not used
2	+5V	27	$\overline{\text{IBUS 3}}$
3	$\overline{\text{IFN 0}}$	28	$\overline{\text{CLEAR}}$
4	$\overline{\text{IFN 2}}$	29	$\overline{\text{EN ID}}$
5	$\overline{\text{IFN 1}}$	30	Not used
6	$\overline{\text{IFN 3}}$	31	$\overline{\text{IFCLK}}$
7	FLG 3	32	Not used
8	$\overline{\text{IBUS 4}}$	33	▽
9	FLG 0	34	▽
10	$\overline{\text{IBUS 5}}$	35	+5V
11	FLG 6	36	+5V
12	$\overline{\text{IBUS 6}}$	37	$\overline{\text{IBUS 8}}$
13	$\overline{\text{IFN VALID}}$	38	$\overline{\text{IBUS 12}}$
14	$\overline{\text{IBUS 7}}$	39	$\overline{\text{IBUS 9}}$
15	▽	40	$\overline{\text{IBUS 13}}$
16	▽	41	$\overline{\text{IBUS 10}}$
17	Not used	42	$\overline{\text{IBUS 14}}$
18	POWER FAIL	43	$\overline{\text{IBUS 11}}$
19	▽	44	$\overline{\text{IBUS 15}}$
20	▽	45	Not used
21	$\overline{\text{IBUS 0}}$	46	FLG 7
22	+5V	47	FLG 1
23	$\overline{\text{IBUS 1}}$	48	FLG 8
24	Not used	49	▽
25	$\overline{\text{IBUS 2}}$	50	▽

NOTE: Connects J1 of 7905A Interface to J1 of Device Controller

Table 4-15E. 7905A/7920A Disc Interface Connectors J2

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	ROM 0
2	▽	27	ROM 1
3	ROM 19	28	Not used
4	ROM 18	29	RAR 2
5	ROM 7	30	Not used
6	ROM 6	31	RAR 1
7	ROM 5	32	Not used
8	ROM 4	33	RAR 0
9	ROM 17	34	Not used
10	ROM 16	35	ROM 15
11	ROM 8	36	Not used
12	ROM 9	37	ROM 14
13	ROM 10	38	Not used
14	Not used	39	ROM 13
15	ROM 11	40	Not used
16	Not used	41	ROM 12
17	RAR 7	42	ROM 23
18	Not used	43	ROM 22
19	RAR 6	44	Not used
20	Not used	45	ROM 21
21	RAR 5	46	Not used
22	RAR 4	47	ROM 20
23	RAR 3	48	Not used
24	ROM 2	49	▽
25	ROM 3	50	▽

NOTE: Connects J2 of Error Correction Card to J2 of Microprocessor.

Table 4-15F. 7905A/7920A Disc Interface Connectors P2

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	EXT FLG 5
2	CLEAR	27	EXT FLG 2 (EOW)
3	CYCLE CLOCK	28	EXT FLG 3 (I/O P ERR)
4	Not used	29	EXT FLG 0 (CMDRDY)
5	EXT FLG 16 (UNCORR DATA ERROR)	30	EXT FLG 1 (DT RDY)
6	XADDR2	31	M12
7	UB OUT	32	EXT SEL
8	INPUT	33	M13
9	EXT FLG 8 (INTOK)	34	M11
10	LB OUT	35	M14
11	EXT FLG 12	36	M10
12	EXT FLG 10	37	M15
13	EXT FLG 14	38	M9
14	EXT FLG 13	39	TST CLK
15	XADDR 3	40	M8
16	EX FLG 15	41	M3
17	XADDR 0	42	M4
18	XADDR 4	43	M2
19	CLK DISABLE	44	M5
20	XADDR1	45	M1
21	EX FLG 11 (ANY DATA ERROR)	46	M6
22	EXT FLG 9	47	M0
23	EXT FLG 6 (EOP)	48	M7
24	EXT FLG 7 (OVRLIN)	49	Not used
25	EXT FLG 4	50	▽

NOTE: Interconnects P2 of Cartridge Disc Controller.

Table 4-15G. 7905A/7920A Disc Interface Connectors P3

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	READ NRZ DATA
2	30 MHZ	27	▽
3	▽	28	Not used
4	+5V	29	▽
5	▽	30	Not used
6	INH CRC CLK	31	▽
7	▽	32	DATA CLOCK
8	Not used	33	▽
9	▽	34	TEST CLR
10	WRITE DATA TEST	35	▽
11	▽	36	SYNC
12	WRITE CLK	37	▽
13	▽	38	TEST OUTPUT
14	WRITE TEST	39	▽
15	▽	40	Not used
16	+5V	41	▽
17	▽	42	Not used
18	+5V	43	▽
19	▽	44	SERIAL DATA FROM ECC
20	Not used	45	▽
21	▽	46	Not used
22	READ TEST	47	▽
23	▽	48	Not used
24	READ CLK	49	▽
25	▽	50	CLOCK INHIBIT

NOTE: Interconnects P3s of Cartridge Disc Controller

Table 4-15H. Device Controller to HP 7905A/7920A Disc Drive

PIN	SIGNAL	PIN	SIGNAL
1	+5V	26	Not used
2	+5V	27	$\overline{\text{CBUS 7}}$
3	$\overline{\text{CBUS 0}}$	28	Not used
4	$\overline{\text{CBUS 11}}$	29	▽
5	$\overline{\text{CBUS 1}}$	30	Not used
6	$\overline{\text{CBUS 10}}$	31	▽
7	$\overline{\text{CBUS 2}}$	32	Not used
8	$\overline{\text{CBUS 9}}$	33	▽
9	$\overline{\text{CBUS 3}}$	34	▽
10	$\overline{\text{CBUS 8}}$	35	+5V
11	▽	36	+5V
12	▽	37	Not used
13	Not used	38	$\overline{\text{CBUS 12}}$
14	▽	39	Not used
15	▽	40	$\overline{\text{CBUS 13}}$
16	▽	41	Not used
17	Not used	42	$\overline{\text{CBUS 14}}$
18	Not used	43	Not used
19	▽	44	$\overline{\text{CBUS 15}}$
20	▽	45	▽
21	$\overline{\text{CBUS 4}}$	46	▽
22	+5V	47	▽
23	$\overline{\text{CBUS 5}}$	48	▽
24	Not used	49	▽
25	$\overline{\text{CBUS 6}}$	50	▽

NOTE: Device Controller J3 to Cartridge Disc Drive.

Table 4-15I. Disc File Interface Connectors J1

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	▽
2	UNIR (1)	27	SER DATA
3	▽	28	▽
4	UNIR (2)	29	WD 70
5	▽	30	▽
6	UNIR (4)	31	SMP
7	CEN	32	▽
8	CEE	33	TD
9	▽	34	▽
10	$\overline{\text{FCE}}$	35	FSMK
11	▽	36	CLK MSB
12	CCLR	37	▽
13	▽	38	$\overline{\text{D10}}$
14	▽	39	TA
15	$\overline{\text{DRIVE BUSY}}$	40	▽
16	+READ	41	$\overline{\text{D11}}$
17	$\overline{\text{SEEKING}}$	42	$\overline{\text{D12}}$
18	▽	43	WSM
19	$\overline{\text{UNSAFE}}$	44	$\overline{\text{D15}}$
20	CCIN	45	TC
21	$\overline{\text{ONLINE}}$	46	▽
22	▽	47	$\overline{\text{D14}}$
23	$\overline{\text{PACK CHANGE}}$	48	$\overline{\text{D13}}$
24	$\overline{\text{200 TPI}}$	49	CCW
25	TB	50	▽

NOTE: Connects J1 of Bus PCA to J1 of Read/Write PCA.

Table 4-15J. Disc File Interface Connectors J2

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	Not used
2	▽	27	$\overline{\text{ROM 16}}$
3	$\overline{\text{ROM 04}}$	28	$\overline{\text{ROM 00}}$ (MSB)
4	Not used	29	$\overline{\text{ROM 17}}$
5	$\overline{\text{ROM 05}}$	30	$\overline{\text{ROM 01}}$
6	Not used	31	$\overline{\text{ROM 18}}$
7	$\overline{\text{ROM 06}}$	32	$\overline{\text{ROM 02}}$
8	Not used	33	$\overline{\text{ROM 19}}$ (LSB)
9	$\overline{\text{ROM 07}}$	34	$\overline{\text{ROM 03}}$
10	Not used	35	Not used
11	$\overline{\text{ROM 08}}$	36	ROM ENABLE
12	Not used	37	RAR 00 (SPARE)
13	$\overline{\text{ROM 09}}$	38	RAR 01 (SPARE)
14	Not used	39	RAR 02 (SPARE)
15	$\overline{\text{ROM 10}}$	40	RAR 03
16	Not used	41	RAR 04
17	$\overline{\text{ROM 11}}$	42	RAR 05
18	Not used	43	RAR 06
19	$\overline{\text{ROM 12}}$	44	RAR 07
20	Not used	45	RAR 08
21	$\overline{\text{ROM 13}}$	46	RAR 09
22	Not used	47	RAR 10
23	$\overline{\text{ROM 14}}$	48	RAR 11 (LSB)
24	Not used	49	▽
25	$\overline{\text{ROM 15}}$	50	▽

NOTE: Connects J2 of Read/Write PCA to J2 of Controller Processor PCA.

Table 4-15K. Disc File Interface Connectors J3

PIN	SIGNAL	PIN	SIGNAL
1	▽	26	DRQ (FLG 5)
2	$\overline{\text{CLR}}$, ($\overline{\text{MST RESET}}$)	27	CE (FLG 2)
3	$\overline{\text{T0}}$	28	CSMK (FLG 3)
4	$\overline{\text{T3}}$	29	$\overline{\text{CRWX}}$ (FLG 0)
5	$\overline{\text{T2}}$	30	FLG 7
6	ROR 09	31	M12
7	UOS	32	$\overline{\text{EXT SEL}}$
8	INPUT STROBE	33	$\overline{\text{M13}}$
9	EOTL (FLG 10)	34	$\overline{\text{M11}}$
10	LOS	35	$\overline{\text{M14}}$
11	$\overline{\text{OUTXFER}}$ (FLG 14)	36	$\overline{\text{M10}}$
12	$\overline{\text{DAT}}$ (FLG 12)	37	$\overline{\text{M15}}$ (LSB)
13	INTACT (FLG 16)	38	$\overline{\text{M09}}$
14	$\overline{\text{INXFER}}$ (FLG 15)	39	$\overline{\text{T1}}$
15	ROR 08 (MSB)	40	$\overline{\text{M08}}$
16	FLG 17	41	$\overline{\text{M03}}$
17	ROR 11 (LSB)	42	$\overline{\text{M04}}$
18	ROR 07	43	$\overline{\text{M02}}$
19	WT 1	44	$\overline{\text{M05}}$
20	ROR 10	45	$\overline{\text{M01}}$
21	CMD (FLG 13)	46	$\overline{\text{M06}}$
22	TU (FLG 11)	47	$\overline{\text{M00}}$ (MSB)
23	FLG 6	48	$\overline{\text{M07}}$
24	$\overline{\text{INDEX}}$ (FLG 7)	49	RUN/HALT
25	$\overline{\text{DIS}}$ (FLG 4)	50	▽

NOTE: Connects J3 of Disc File Interface.

Table 4-15L. P2 of Disc File Bus Card PCA

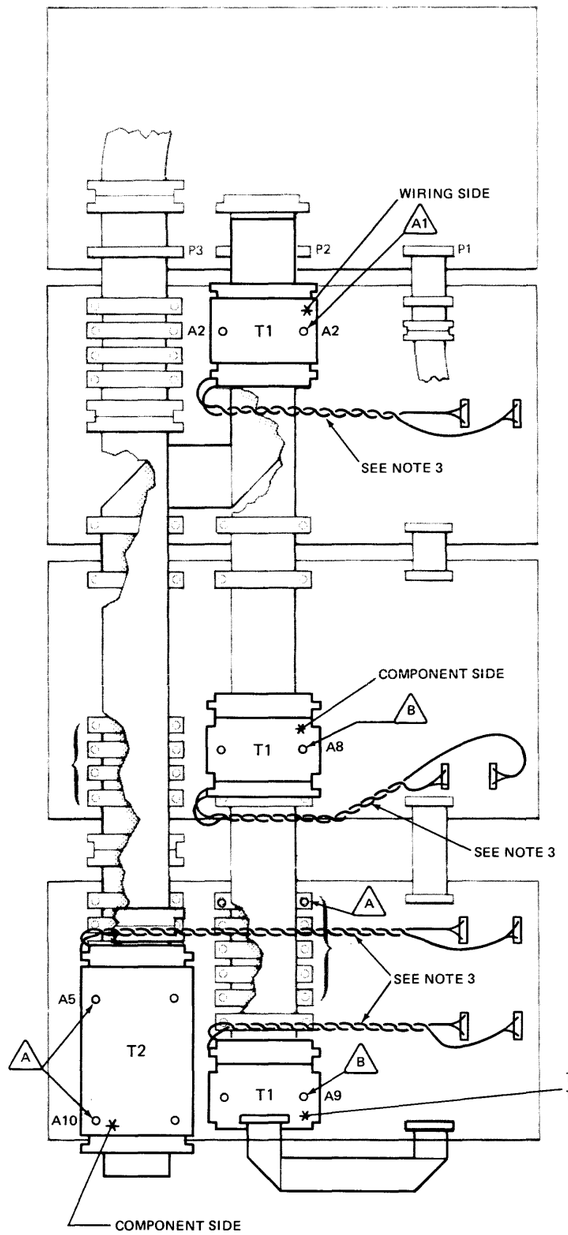
PIN	SIGNAL	PIN	SIGNAL
1	MOD SEL (SPARE)	26	▽
2	▽	27	$\overline{\text{BUS 256}}$
3	MOD SEL 7	28	▽
4	▽	29	$\overline{\text{BUS 1}}$
5	MOD SEL 6	30	▽
6	▽	31	$\overline{\text{BUS 2}}$
7	MOD SEL 4	32	▽
8	▽	33	$\overline{\text{BUS 8}}$
9	MOD SEL 5	34	▽
10	▽	35	$\overline{\text{BUS 4}}$
11	MOD SEL 3	36	▽
12	▽	37	$\overline{\text{BUS 16}}$
13	MOD SEL 2	38	▽
14	▽	39	$\overline{\text{BUS 128}}$
15	MOD SEL 0	40	▽
16	▽	41	$\overline{\text{BUS 32}}$
17	MOD SEL 1	42	▽
18	▽	43	$\overline{\text{BUS 64}}$
19	$\overline{\text{SET HD/DIR}}$	44	▽
20	▽	45	Not used
21	$\overline{\text{SET DIFF}}$	46	▽
22	▽	47	$\overline{\text{SEQ PICK}}$
23	$\overline{\text{SET CYL}}$	48	$\overline{\text{CLK OUT}}$
24	▽	49	$\overline{\text{TRACE SEQ PICK}}$
25	$\overline{\text{CONTR}}$	50	$\overline{\text{CPU HLT}}$

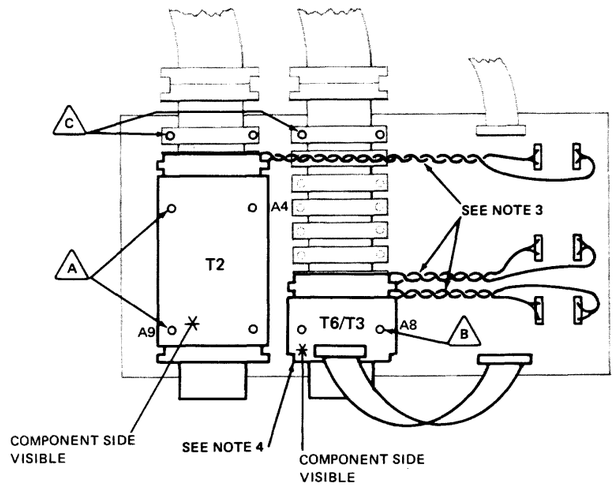
NOTE: Connects P2 of Bus PCA to HP 30331A Junction Panel

Table 4-15M. P3 of Disc File Bus Card PCA

PIN	SIGNAL	PIN	SIGNAL
1	$\overline{\text{GAT 7}}$	26	▽
2	$\overline{\text{GAT}}$ (SPARE)	27	$\overline{\text{FILE UNSAFE}}$
3	▽	28	▽
4	$\overline{\text{GAT 6}}$	29	$\overline{\text{ONLINE}}$
5	$\overline{\text{GAT 5}}$	30	▽
6	▽	31	$\overline{\text{BUSY}}$
7	▽	32	▽
8	$\overline{\text{GAT 4}}$	33	$\overline{\text{INDEX}}$
9	$\overline{\text{GAT 3}}$	34	▽
10	▽	35	$\overline{\text{CAR 1}}$
11	$\overline{\text{GAT 2}}$	36	▽
12	▽	37	$\overline{\text{CAR 2}}$
13	$\overline{\text{GAT 1}}$	38	▽
14	▽	39	$\overline{\text{CAR 4}}$
15	$\overline{\text{GAT 0}}$	40	▽
16	▽	41	$\overline{\text{CAR 8}}$
17	200 TPI	42	▽
18	▽	43	$\overline{\text{CAR 16}}$
19	$\overline{\text{WRCR SENSE}}$	44	▽
20	▽	45	$\overline{\text{CAR 32}}$
21	$\overline{\text{PACK CHANGE}}$	46	▽
22	▽	47	$\overline{\text{CAR 64}}$
23	$\overline{\text{END OF CYL}}$	48	▽
24	▽	49	$\overline{\text{CAR 128}}$
25	$\overline{\text{SEEK INCOMPLETE}}$	50	$\overline{\text{CAR 256}}$

NOTE: Connects P3 of Bus PCA to HP 30331A Junction Panel.





A = DETAIL A, ITEMS 5, 6, 8

A1 = DETAIL A, ITEMS 2, 3, 5, 6, 8

B = DETAIL B

C = DETAIL C

D = FLAT CABLE CONNECTORS JOINED WITH EXTENDER BOARDS

NOTES:

1. TERMINATORS ARE IDENTIFIED AS FOLLOWS:

TERMINATOR	QUANTITY	PART NUMBER
T1	2	30001-60009
T2	2	30001-60016
T3	2	30001-60021
T4	1*	30030-60015
T6	1	30035-60003

2. PRINTED CIRCUIT EDGE CONNECTOR J1 OF A TERMINATOR PLUGS INTO A FLAT CABLE CONNECTOR TO TERMINATE THE CABLE RUN. CORRECT TERMINATOR ORIENTATION IS ASSURED IF YOU KEEP PINS 49 AND 50 OF THE EDGE CONNECTOR TO THE LEFT WHEN TERMINATING THE FLAT CABLE.

3. EACH TERMINATOR (EXCEPT T5) HAS A RED TWISTED PAIR CABLE WHICH CONNECTS FROM EDGE P1 OF THE TERMINATOR PCA TO PINS 2 AND 1 (+5 VOLTS) ON ANY POWER BUS CONNECTOR P1. A BLACK TWISTED PAIR CABLE CONNECTS FROM THE PCA TO PINS 16 AND 15 OF THE SAME POWER BUS CONNECTOR.

4. T3/T4 = T1 IS BENEATH; T4 IS VISIBLE.
   T6/T3 = T6 IS BENEATH; T3 IS VISIBLE.

TERMINATOR MOUNTING HARDWARE

1. 1 INCH ROUND SPACER
2. .125 NYLON SPACER
3. SPLIT LOCK WASHER
4. SCREW
5. SCREW WITH LOCK WASHER
6. FLAT WASHER
7. EXTENDER BOARD
8. HEX STANDOFF

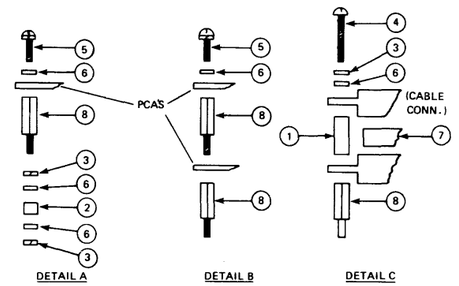
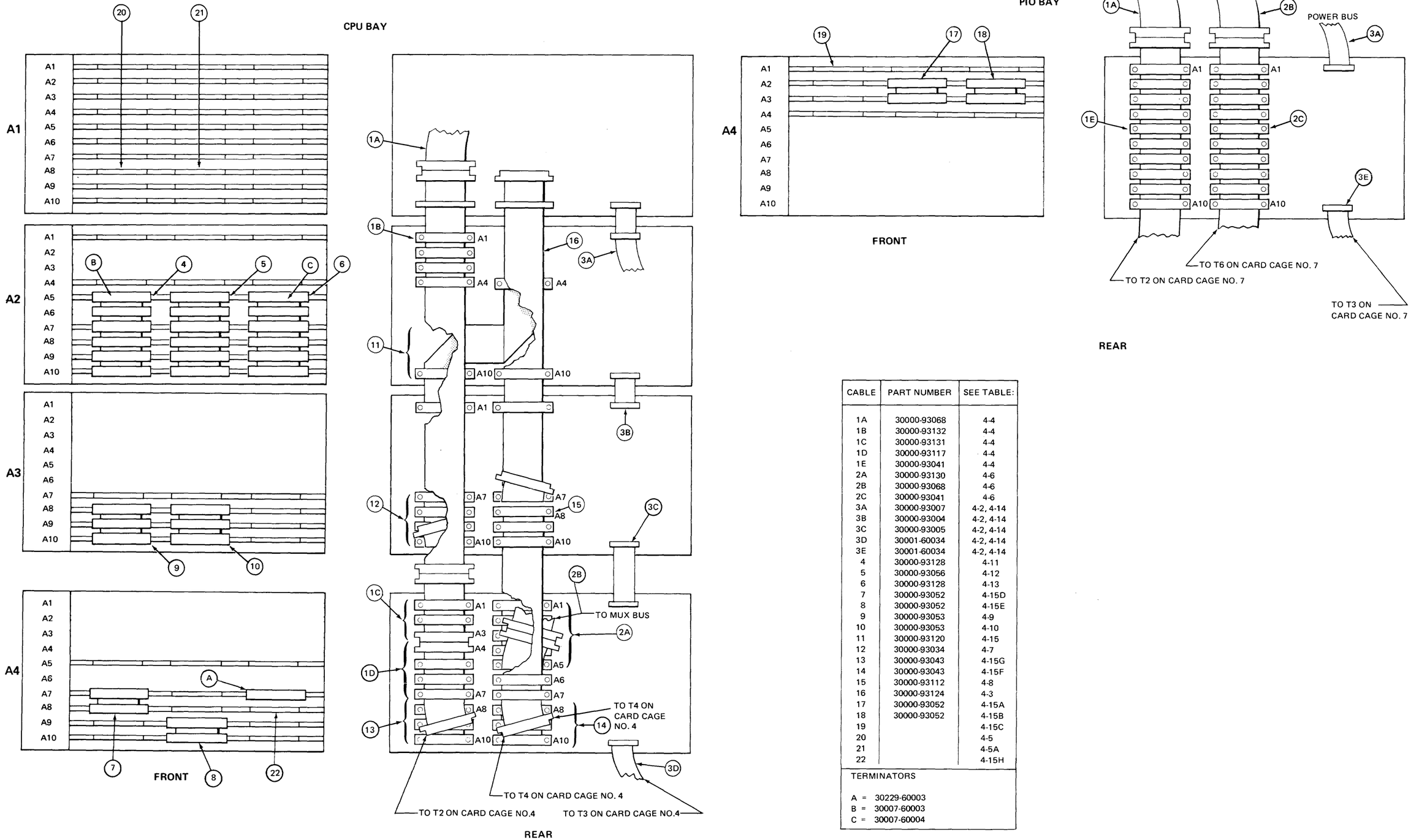


Figure 4-3A. Flat Cable Terminators, Model 6

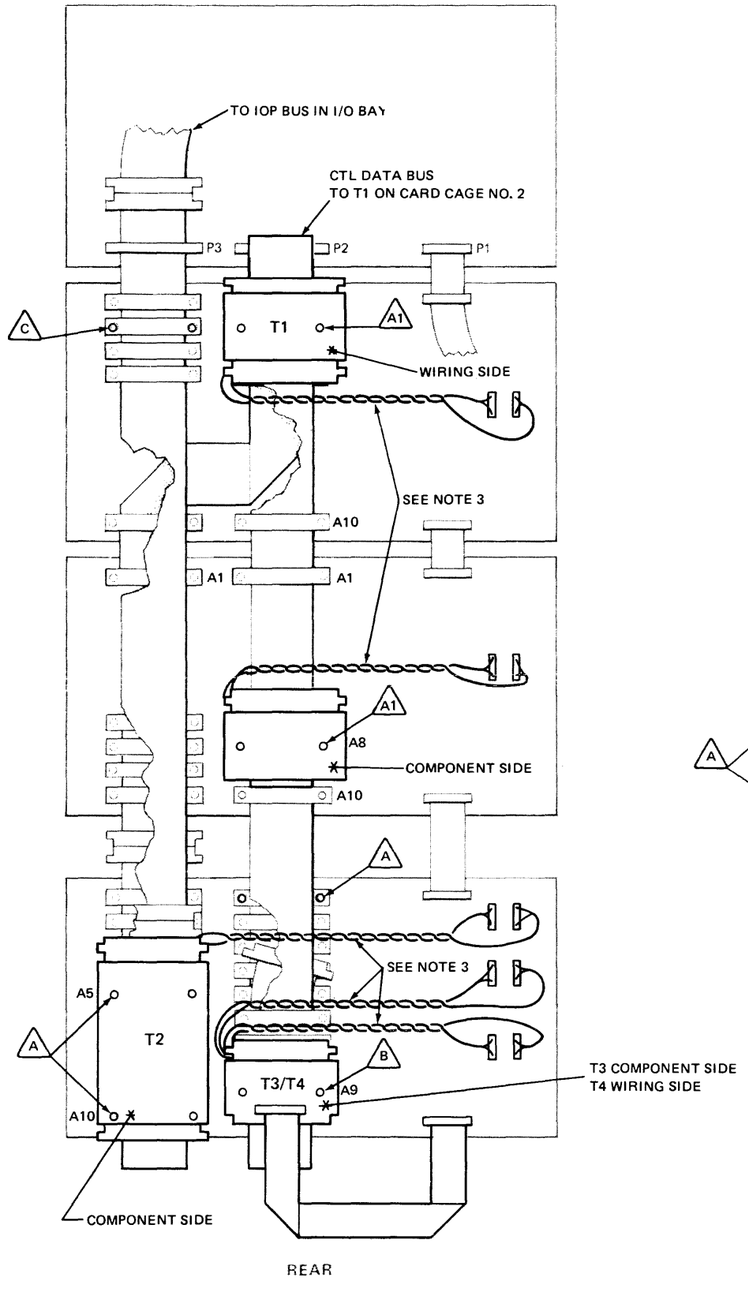


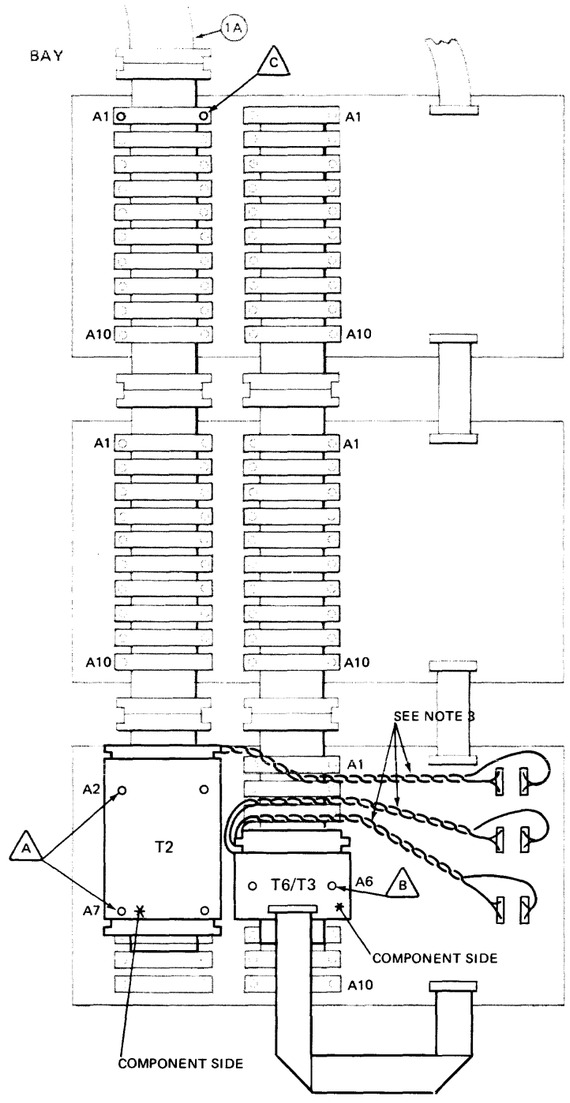
CABLE	PART NUMBER	SEE TABLE:
1A	30000-93068	4-4
1B	30000-93132	4-4
1C	30000-93131	4-4
1D	30000-93117	4-4
1E	30000-93041	4-4
2A	30000-93130	4-6
2B	30000-93068	4-6
2C	30000-93041	4-6
3A	30000-93007	4-2, 4-14
3B	30000-93004	4-2, 4-14
3C	30000-93005	4-2, 4-14
3D	30001-60034	4-2, 4-14
3E	30001-60034	4-2, 4-14
4	30000-93128	4-11
5	30000-93056	4-12
6	30000-93128	4-13
7	30000-93052	4-15D
8	30000-93052	4-15E
9	30000-93053	4-9
10	30000-93053	4-10
11	30000-93120	4-15
12	30000-93034	4-7
13	30000-93043	4-15G
14	30000-93043	4-15F
15	30000-93112	4-8
16	30000-93124	4-3
17	30000-93052	4-15A
18	30000-93052	4-15B
19		4-15C
20		4-5
21		4-5A
22		4-15H

TERMINATORS

A = 30229-60003
B = 30007-60003
C = 30007-60004

Figure 4-3B. System Flat Cables, Model 6





NOTES:

1. TERMINATORS ARE IDENTIFIED AS FOLLOWS:

TERMINATOR	QUANTITY	PART NUMBER
T1	2	30001-60009
T2	2	30001-60016
T3	2	30001-60021
T4	1*	30030-60015
T6	1	30035-60003

2. PRINTED CIRCUIT EDGE CONNECTOR J1 OF A TERMINATOR PLUGS INTO A FLAT CABLE CONNECTOR TO TERMINATE THE CABLE RUN. CORRECT TERMINATOR ORIENTATION IS ASSURED IF YOU KEEP PINS 49 AND 50 OF THE EDGE CONNECTOR TO THE LEFT WHEN TERMINATING THE FLAT CABLE.

3. EACH TERMINATOR HAS A RED TWISTED PAIR CABLE WHICH CONNECTS FROM EDGE P1 OF THE TERMINATOR PCA TO PINS 2 AND 1 (+5 VOLTS) ON ANY POWER BUS CONNECTOR P1. A BLACK TWISTED PAIR CABLE CONNECTS FROM THE PCA TO PINS 16 AND 15 OF THE SAME POWER BUS CONNECTOR.

4. T1/T4 = T1 IS BENEATH; T4 IS VISIBLE.
   T6/T3 = T6 IS BENEATH; T3 IS VISIBLE.

(A) = DETAIL A, ITEMS 5, 6, 8

(A1) = DETAIL A, ITEMS 2, 3, 5, 6, 8

(B) = DETAIL B

(C) = DETAIL C

(D) = FLAT CABLE CONNECTORS JOINED WITH EXTENDER BOARDS

TERMINATOR MOUNTING HARDWARE

1. 1 INCH ROUND SPACER
2. .125 NYLON SPACER
3. SPLIT LOCK WASHER
4. SCREW
5. SCREW WITH LOCK WASHER
6. FLAT WASHER
7. EXTENDER BOARD
8. HEX STANDOFF

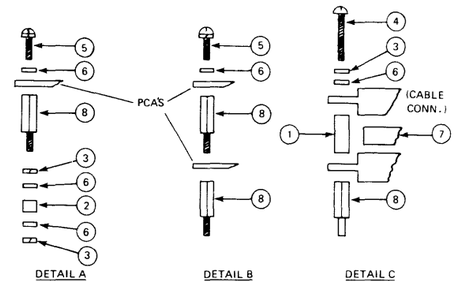
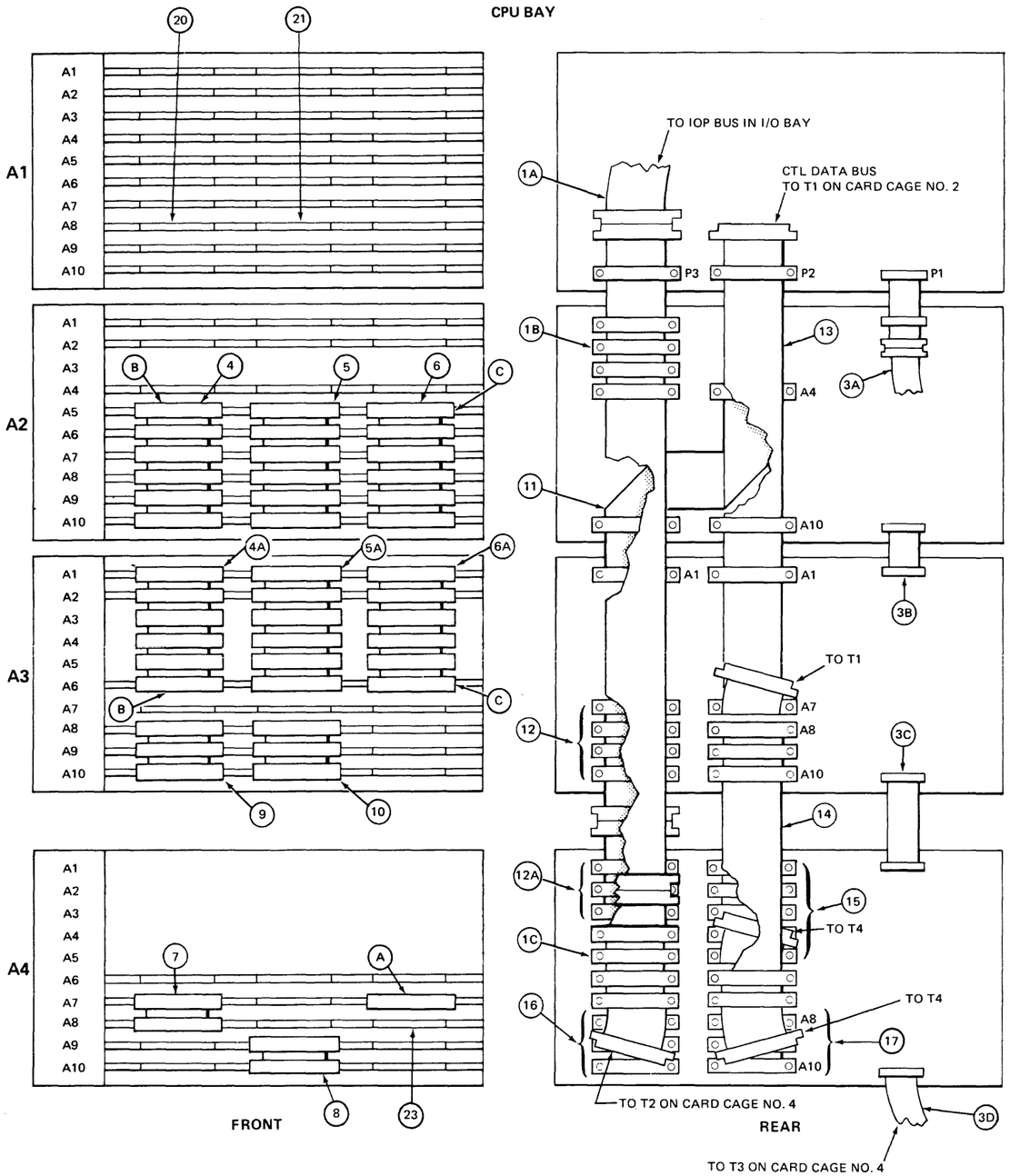
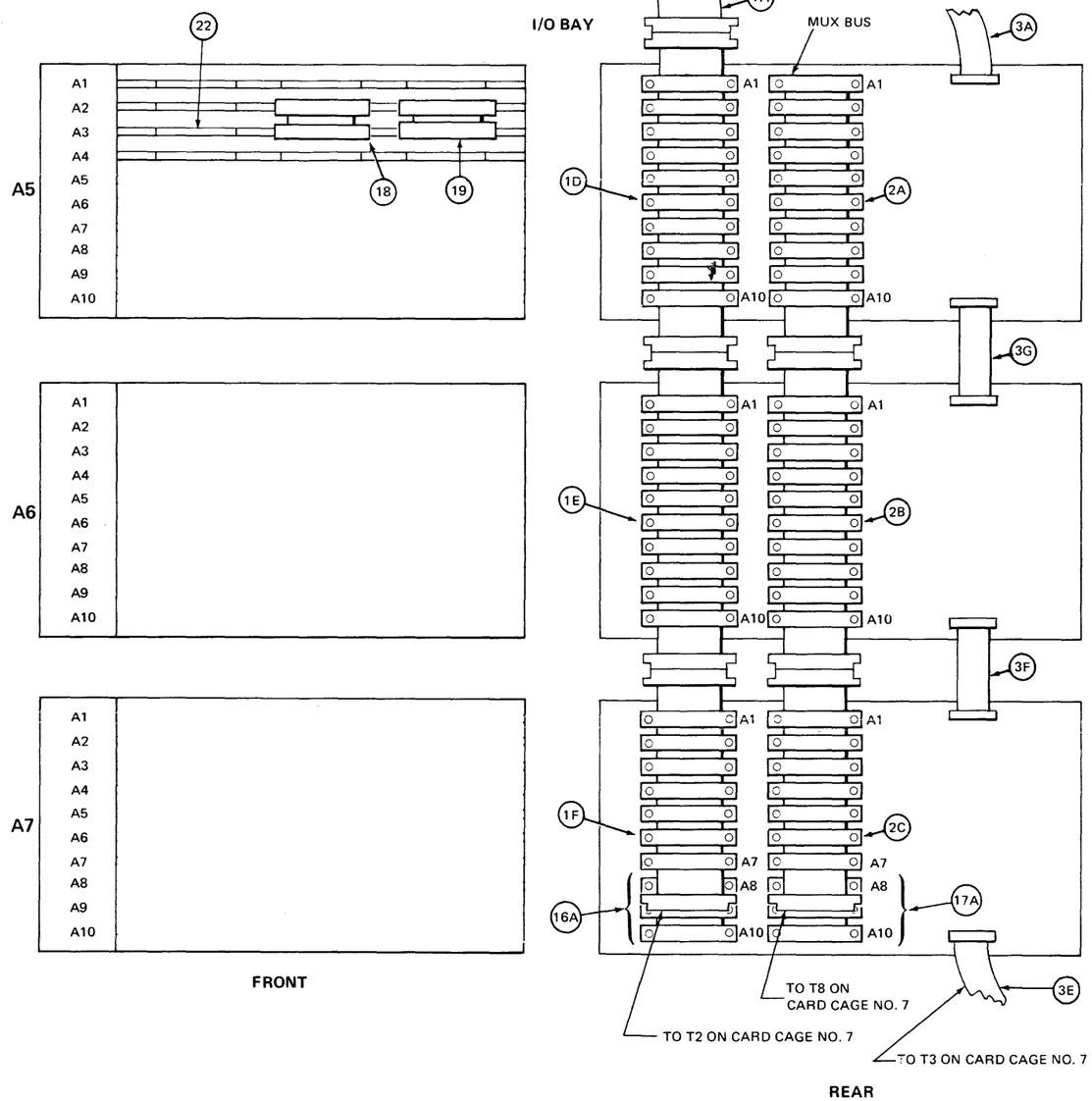


Figure 4-3C. Flat Cable Terminators, Model 8

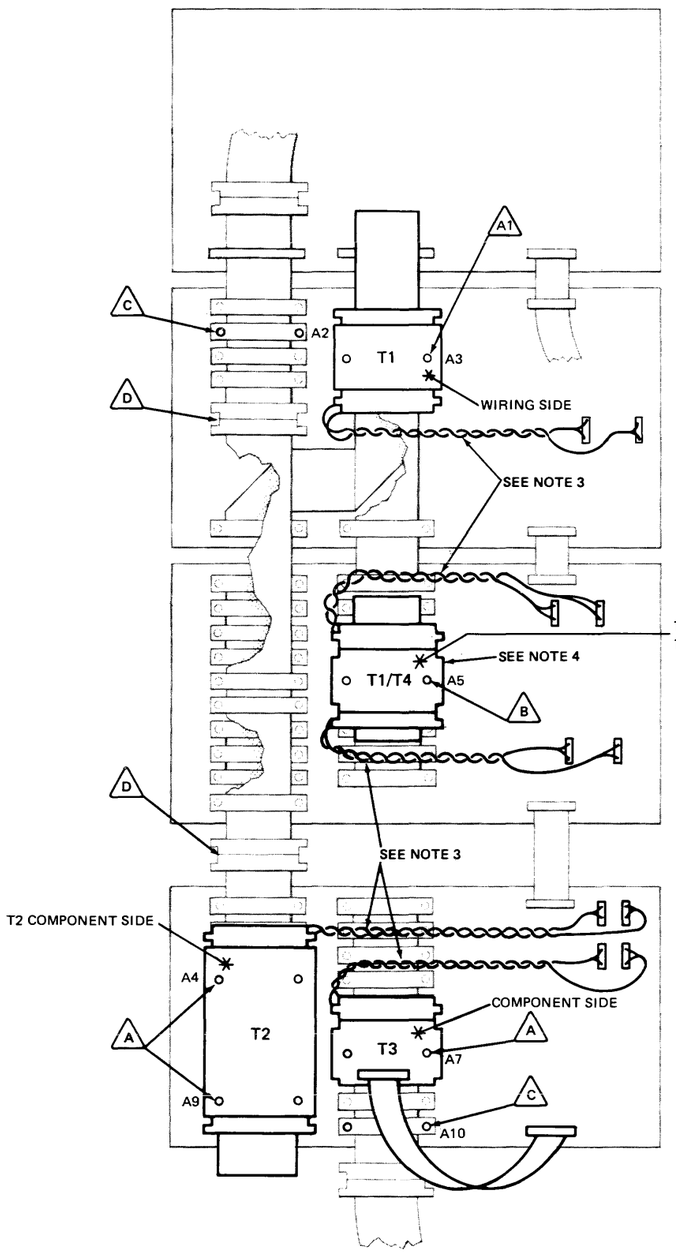


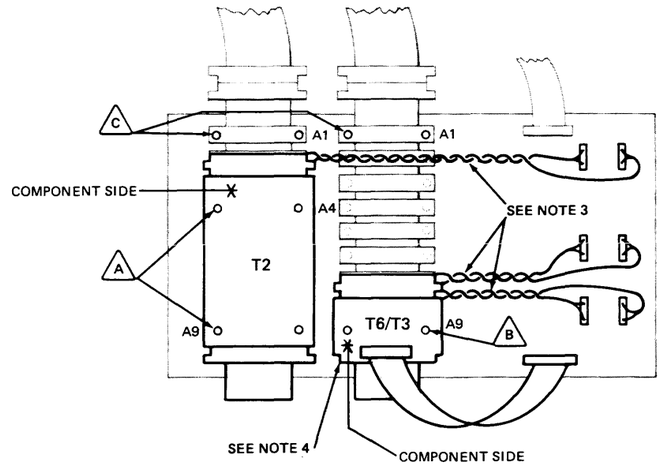


CABLE	PART NUMBER	SEE TABLE	CABLE	PART NUMBER	SEE TABLE	CABLE	PART NUMBER	SEE TABLE
1A	30000-93068	4-4	3F	30000-93005	4-2, 4-14	12A	30000-93131	4-7
1B	30000-93132	4-4	3G	30000-93004	4-2, 4-14	13	30000-93124	4-3
1C	30000-93117	4-4	4	30000-93128	4-11	14	30000-93112	4-8
1D	30000-93041	4-4	4A	30000-93128	4-11	15	30000-93130	4-8
1E	30000-93041	4-4	5	30000-93056	4-12	16	30000-93043	4-15G
1F	30000-93106	4-4	5A	30000-93056	4-12	16A	30000-93043	4-15G
2A	30000-93040	4-6	6	30000-93128	4-13	17	30000-93043	4-15F
2B	30000-93041	4-6	6A	30000-93128	4-13	17A	30000-93043	4-15F
2C	30000-93106	4-6	7	30000-93052	4-15D	18	30000-93052	4-15A
3A	30000-93007	4-2, 4-14	8	30000-93052	4-15E	19	30000-93052	4-15B
3B	30000-93004	4-2, 4-14	9	30000-93053	4-9	20		4-5
3C	30000-93005	4-2, 4-14	10	30000-93053	4-10	21		4-5A
3D	30001-60034	4-2, 4-14	11	30000-93120	4-15	22		4-15C
3E	30001-60034	4-2, 4-14	12	30000-93034	4-7	23		4-15H

TERMINATORS
A = 30229-60003
B = 30007-60003
C = 30007-60004

Figure 4-3D. System Flat Cables, Model 8





A = DETAIL A, ITEMS 5, 6, 8

A1 = DETAIL A, ITEMS 2, 3, 5, 6, 8

B = DETAIL B

C = DETAIL C

D = FLAT CABLE CONNECTORS JOINED WITH EXTENDER BOARDS

NOTES:

1. TERMINATORS ARE IDENTIFIED AS FOLLOWS:

TERMINATOR	QUANTITY	PART NUMBER
T1	2	30001-60009
T2	2	30001-60016
T3	2	30001-60021
T4	1*	30030-60015
T6	1	30035-60003

*Standard for Model 5; optional for Model 7.

2. PRINTED CIRCUIT EDGE CONNECTOR J1 OF A TERMINATOR PLUGS INTO A FLAT CABLE CONNECTOR TO TERMINATE THE CABLE RUN. CORRECT TERMINATOR ORIENTATION IS ASSURED IF YOU KEEP PINS 49 AND 50 OF THE EDGE CONNECTOR TO THE LEFT WHEN TERMINATING THE FLAT CABLE.

3. EACH TERMINATOR (EXCEPT T5) HAS A RED TWISTED PAIR CABLE WHICH CONNECTS FROM EDGE P1 OF THE TERMINATOR PCA TO PINS 2 AND 1 (+5 VOLTS) ON ANY POWER BUS CONNECTOR P1. A BLACK TWISTED PAIR CABLE CONNECTS FROM THE PCA TO PINS 16 AND 15 OF THE SAME POWER BUS CONNECTOR.

4. T1/T4 = T1 IS BENEATH; T4 IS VISIBLE.
   T6/T3 = T6 IS BENEATH; T3 IS VISIBLE.

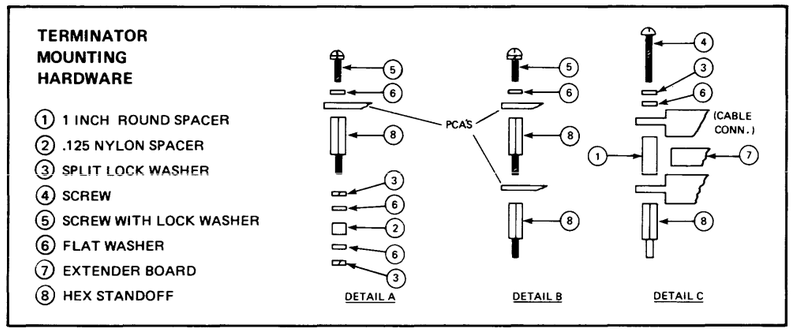
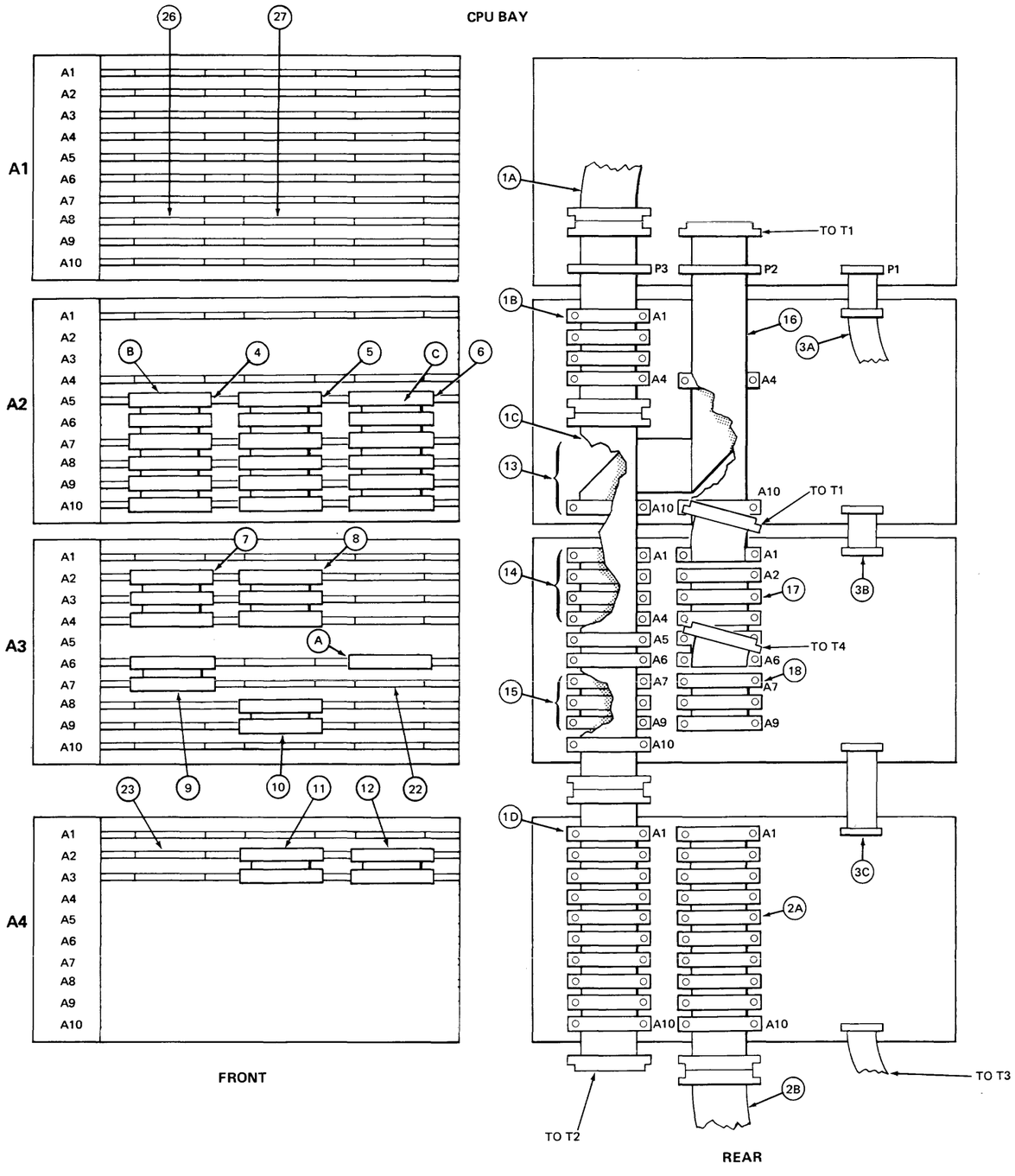
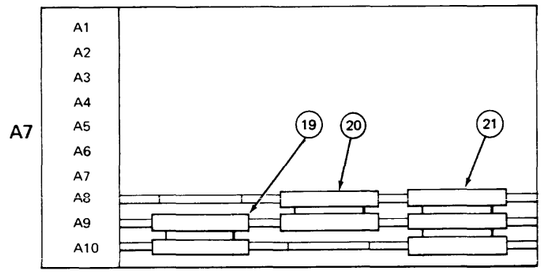
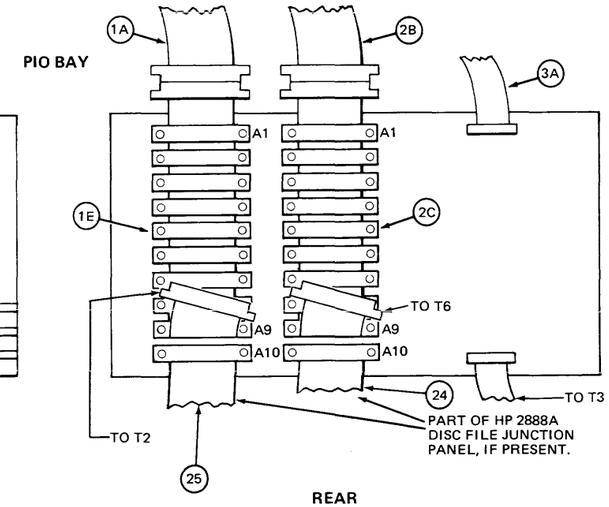


Figure 4-3E. Flat Cable Terminators, Model 5 or 7



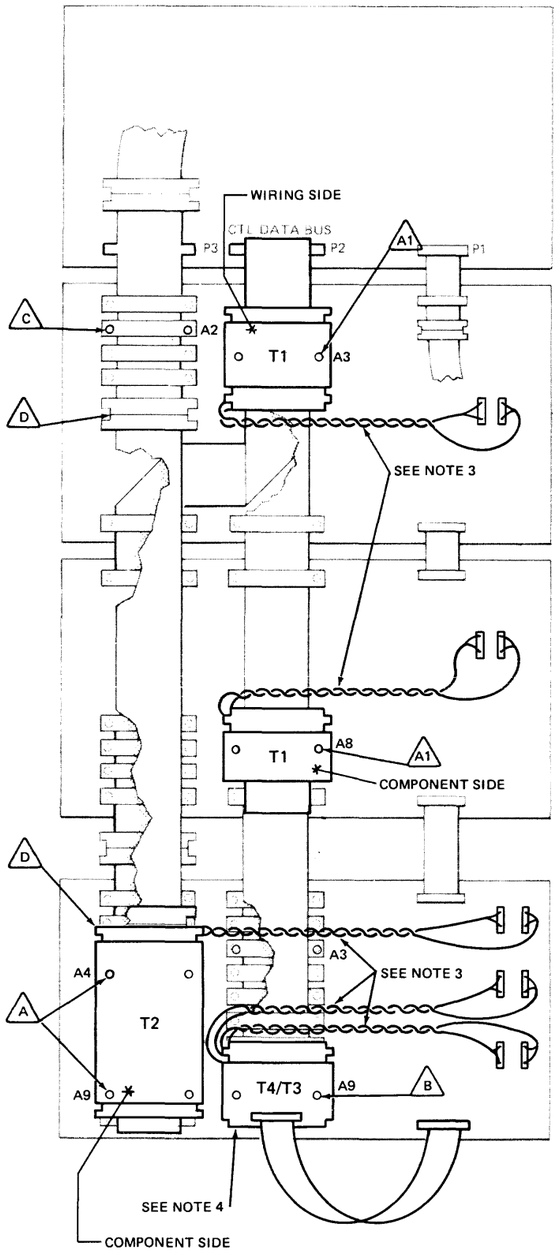


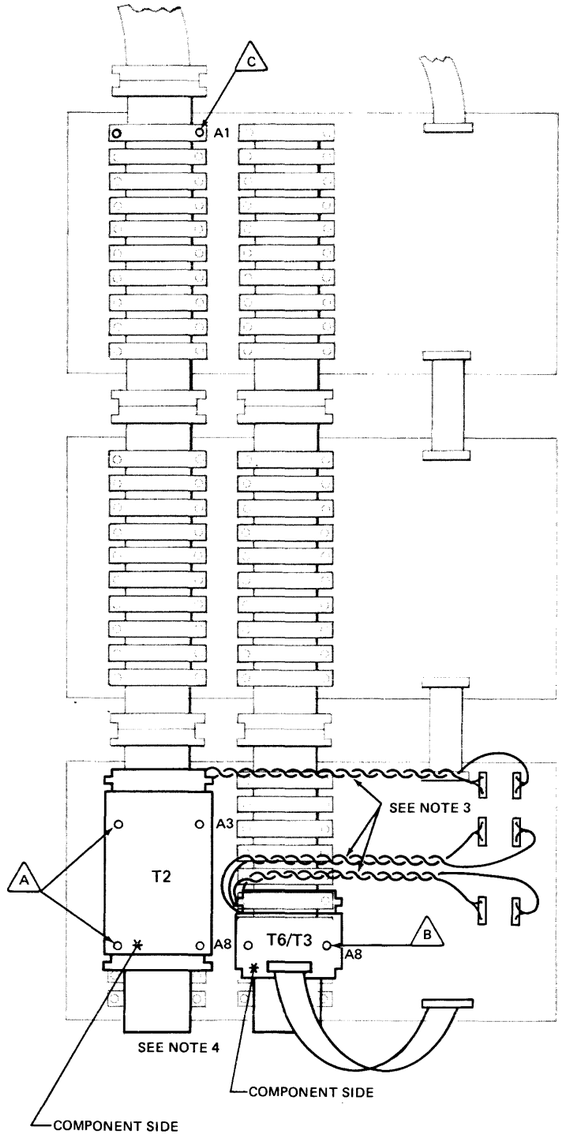


CABLE	PART NUMBER	SEE TABLE:
1A	30000-93068	4-4
1B	30000-93121	
1C	30000-93125	
1D	30000-93041	
1E	30000-93020	
2A	30000-93040	4-6
2B	30000-93068	
2C	30000-93020	
3A	30000-93007	4-2, 4-14
3B	30000-93004	
3C	30000-93005	
4	30000-93128	4-11
5	30000-93056	4-12
6	30000-93128	4-13
7	30000-93053	4-9
8	30000-93053	4-10
9	30000-93052	4-15D
10	30000-93052	4-15E
11	30000-93052	4-15A
12	30000-93052	4-15B
13	30000-93119	4-15
14	30000-93044	4-7
15	30000-93043	4-15G
16	30000-93123	4-3
17	30000-93035	4-8
18	30000-93043	4-15F
19	30000-93052	4-15I
20	30000-93052	4-15J
21	30000-93053	4-15K
22		4-15A
23		4-15C
24		4-15L
25		4-15M
26		4-5
27		4-5A

TERMINATOR	PART NUMBER
A	30229-60003
B	30000-93128
C	30000-93128

Figure 4-3F. System Flat Cables, Model 5 or 7





NOTES:

1. TERMINATORS ARE IDENTIFIED AS FOLLOWS:

TERMINATOR	QUANTITY	PART NUMBER
T1	2	30001-60009
T2	2	30001-60016
T3	2	30001-60021
T4	1*	30030-60015
T6	1	30035-60003

2. PRINTED CIRCUIT EDGE CONNECTOR J1 OF A TERMINATOR PLUGS INTO A FLAT CABLE CONNECTOR TO TERMINATE THE CABLE RUN. CORRECT TERMINATOR ORIENTATION IS ASSURED IF YOU KEEP PINS 49 AND 50 OF THE EDGE CONNECTOR TO THE LEFT WHEN TERMINATING THE FLAT CABLE.

3. EACH TERMINATOR (EXCEPT T5) HAS A RED TWISTED PAIR CABLE WHICH CONNECTS FROM EDGE P1 OF THE TERMINATOR PCA TO PINS 2 AND 1 (+5 VOLTS) ON ANY POWER BUS CONNECTOR P1. A BLACK TWISTED PAIR CABLE CONNECTS FROM THE PCA TO PINS 16 AND 15 OF THE SAME POWER BUS CONNECTOR.

4. T1/T4 = T1 IS BENEATH; T4 IS VISIBLE.
   T6/T3 = T6 IS BENEATH; T3 IS VISIBLE.

A = DETAIL A, ITEMS 5, 6, 8

A1 = DETAIL A, ITEMS 2, 3, 5, 6, 8

B = DETAIL B

C = DETAIL C

D = FLAT CABLE CONNECTORS JOINED WITH EXTENDER BOARDS

TERMINATOR MOUNTING HARDWARE

1. 1 INCH ROUND SPACER
2. .125 NYLON SPACER
3. SPLIT LOCK WASHER
4. SCREW
5. SCREW WITH LOCK WASHER
6. FLAT WASHER
7. EXTENDER BOARD
8. HEX STANDOFF

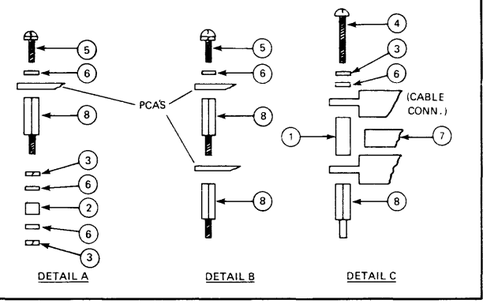
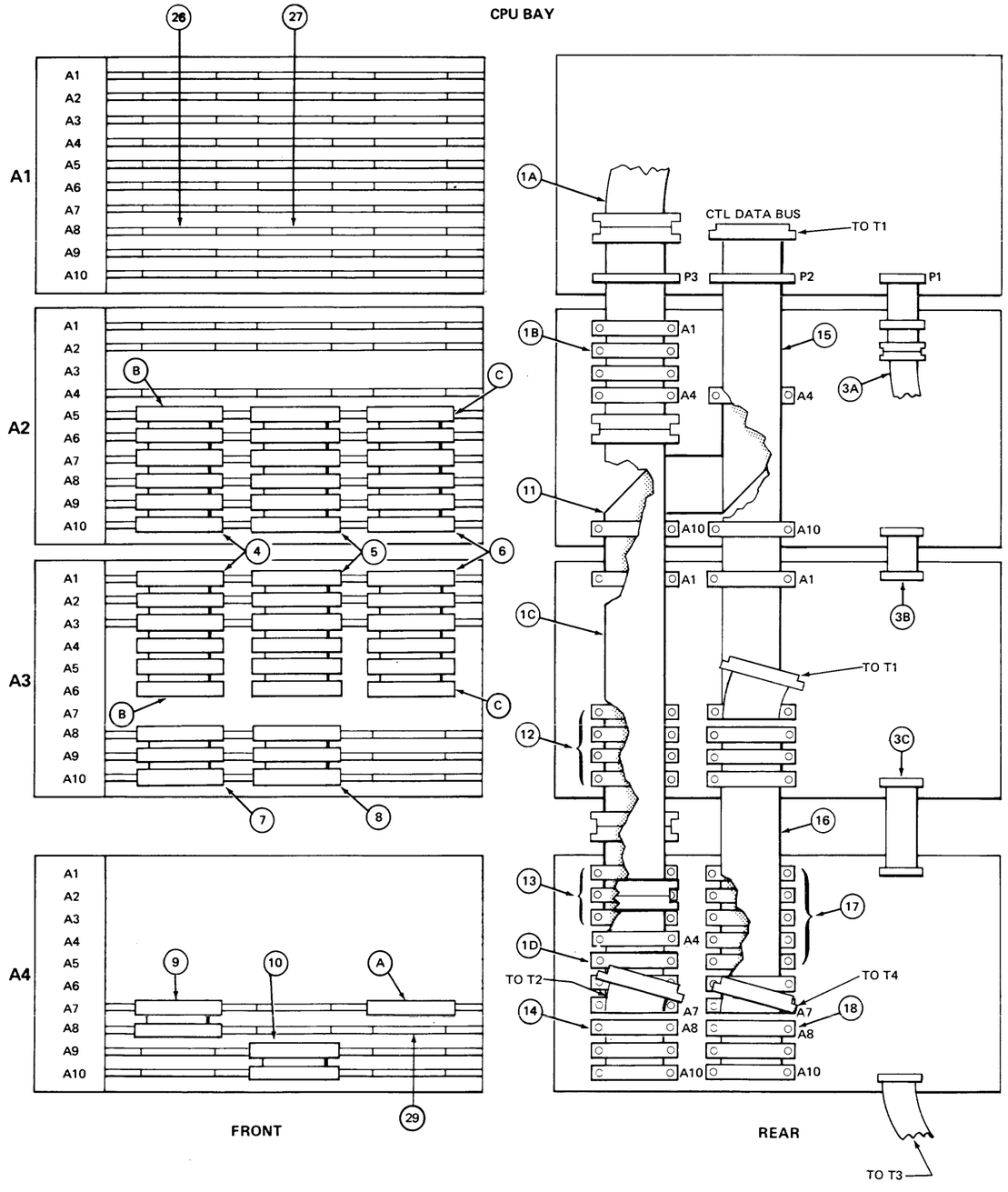
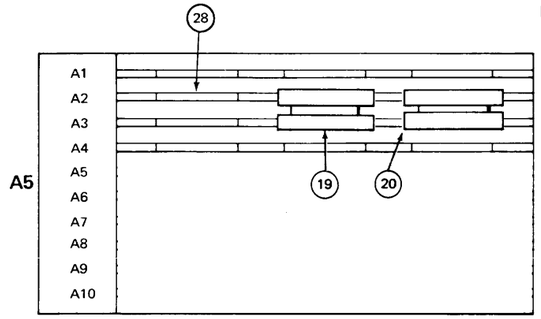
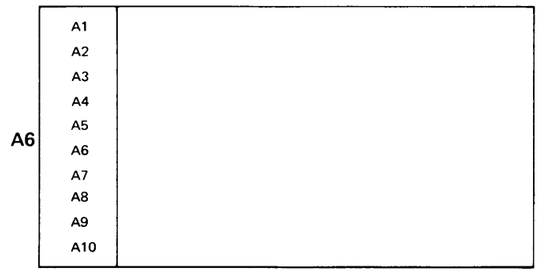
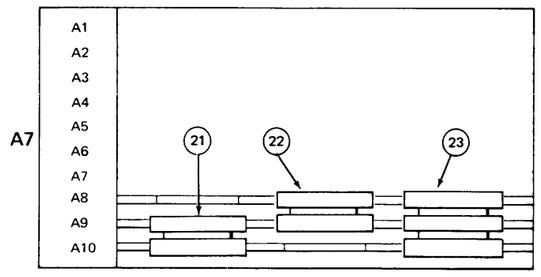


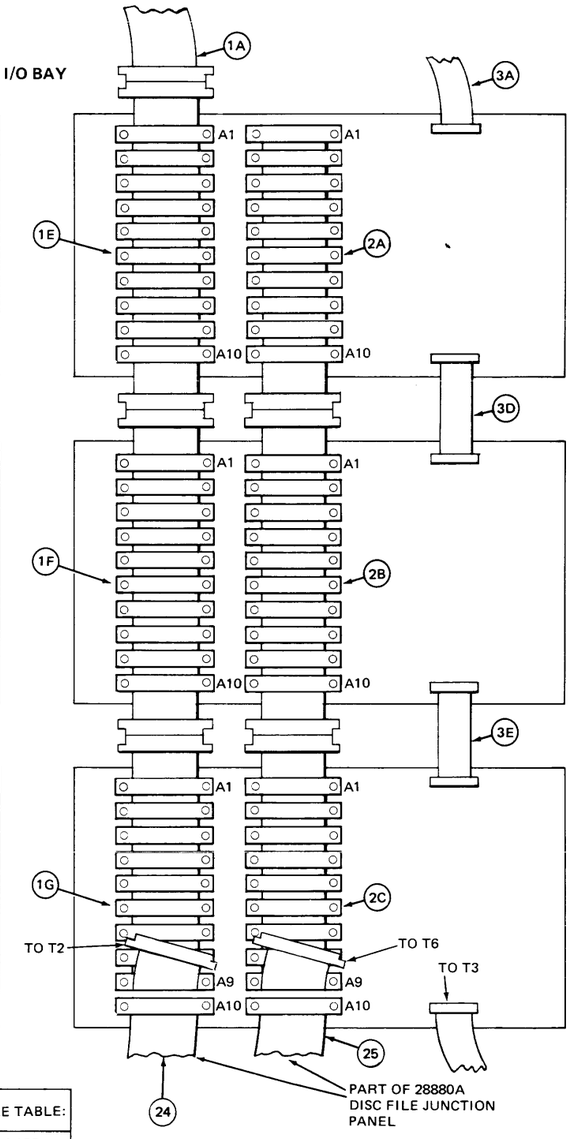
Figure 4-3G. Flat Cable Terminators, Model 9











CABLE	PART NUMBER	SEE TABLE:	CABLE	PART NUMBER	SEE TABLE:
1A	30000-93068	4-4	9	30000-93052	4-15D
1B	30000-93121		10	30000-93052	4-15E
1C	30000-93113		11	30000-93120	4-15
1D	30000-93117		12	93034-93034	4-7
1E	30000-93041		13	30000-93092	4-7
1F	30000-93041		14	30000-93043	4-15G
1G	30000-93020		15	30000-93124	4-3
2A	30000-93040	4-6	16	30000-93112	4-8
2B	30000-93041		17	30000-93035	4-8
2C	30000-93020		18	30000-93043	4-15F
3A	30000-93007	4-2, 4-14	19	30000-93052	4-15A
3B	30000-93004		20	30000-93052	4-15B
3C	30000-93005		21	30000-93052	4-15I
3D	30000-93004		22	30000-93052	4-15J
3E	30000-93005		23	30000-93053	4-15K
4	30000-93128(2)	4-11	24		4-15M
5	30000-93056(2)	4-12	25		4-15L
6	30000-93128(2)	4-13	26		4-5
7	30000-93053	4-9	27		4-5A
8	30000-93053	4-10	28		4-15C
			29		4-15H

TERMINATOR	PART NUMBER
A	30229-60003
B	30000-93128
C	30000-93128

Figure 4-3H. System Flat Cables, Model 9

4-7. INTERRUPT POLLING

In this system, the interrupt priority of a device is completely independent of the device number or physical location. It is determined by the device's logical proximity to the IOP on a jumpered interrupt poll line. The interrupt poll line is wired at system configuration from the IOP to whatever device is assigned first priority and then from device to device according to assigned priority. The interrupt poll line terminates at the device of lowest priority. Table 4-16 provides a suggested guideline for the interrupt polling sequence of some devices. Examination of the interrupt poll line of any system (Figure 4-4) will find it starting at pins 79 (INTPOLL) and 80 (GND) of connector 10P1 of the CPU/IOP backplane which is the IOP connector P1. The connections are made using a twisted pair of wires; one wire is blue and the other is white. These twisted pair cables are equipped at each end with a two-pin spring-clip connector that clips onto pairs of vertically aligned pins. At the CPU/IOP backplane, the twisted pair must be connected with the white wire on the top pin of the pair of pins; at the device controller interfaces, the connections are made with the white wire on the bottom pin.

The INTPOLL signal from the IOP is routed to connector P1 of the device interface PCA with the next highest priority where with the name INTPOLL IN it enters the interface PCA of the device controller on the fifth pair of pins from the left, pins 48 (signal) and 47 (ground). The signal will exit te PCA with the name INTPOLL OUT on the seventh pair of pins from the left, pins 44 (signal) and 43 (ground) for routing to the next highest priority device controller.

4-7A. DATA POLLING

The data poll twisted pair cable is routed from the IOP to the system's Multiplexer Channel PCA as shown typically in Figure 4-4. At the CPU/IOP backplane, the twisted pair must be connected with the white wire on the top pin of the pair of pins; at the Multiplexers, the connections are made with the white wire on the bottom pin.

4-8. MCU CLOCK DISTRIBUTION

Figure 4-5 shows how the coaxial cables are patched on the backplane of the CPU bay to carry the MCUFRC0 to the memory module and the MCUCLK5, MCUCLK6, and MCUCLK7 signals to modules A2, A3, and A4, respectively. (The cabling shown is for a Model 5, 6, 7, 8, or 9 System.) As shown, a 61.9-ohm resistor terminates each of these clock signals with the resistor for module 4 located on the power bus terminator card. Jumpers W1 on the backplane of modules A2, A3, and A4 are opened to isolate the MCUCLK signal to one module.

Figure 4-6 shows the additional cable and terminator used by the two-bay Model 5, 6, or 7 System.

Figure 4-7 shows the additional cables and terminators used by the three-bay Model 8 or 9 System.

4-9. MULTIPLEXER CHANNEL SERVICE REQUEST

The Multiplexer Channel has priority encoder logic which monitors the service request (SR) lines from up to 16 device controllers. Each device controller is assigned data service priority by being assigned one of these SR lines. The assignment is made by the installation of a jumper in one of 16 possible positions at the device controller's interface. Position 0 assigns the highest priority; position 15 the lowest. Table 4-17 shows the sequence by which priority assignment should be made for the device controllers of the HP 3000 Series II Computer System.

4-10. DC POWER CONTROL CIRCUITS

The computer system contains at least one each HP 30310A Power Supply, HP 30311A Power Supply, and HP 30312A Power Supply to power the system's CPU/IOP, Memory, and Input/Output PCA assemblies. A second HP 30310A Power Supply is included to power up to ten additional PCA slots in the second bay and, if memory exceeds 128K words, a second HP 30311A Power Supply installed in the second bay. Model 8 and 9 Systems have a second HP 30312A Power Supply in the second bay to power the increased I/O capability the systems afford. Figure 4-8 shows controls and indicators of the power supplies and of the DC Control Panel which provides master control of DC power for the system. Table 4-18 lists the functions of the controls and indicators.

4-11. General

Figure 4-9 shows the interconnection of the DC Control Panel and the power supplies via their control lines. The DC power control circuits shown are for a system having a memory capacity of over 128K words since two HP 30311A Power Supplies are included. Manual control of system DC power is provided by three series connected ON/STANDBY switches on the DC Control Panel. Setting any of these switches to STANDBY opens the DC Enable line to all HP 30310A and 30312A Power Supplies to disable their output voltage.

In a system with 128K or less memory, setting the SYSTEM switch to STANDBY causes the HP 30310A Power Supply, which furnishes DC power for operation of the HP 30311A Power Supply for lower memory, to remove the

operating power. The HP 30311A Power Supply goes into "battery backup" mode continuing to provide operating voltages to the memory from its internal storage battery. In systems with memories larger than 128K, both HP 30311A Power Supplies go to the "battery backup" mode because both HP 30310A supplies are off.

Setting the LOWER 128K MEMORY switch to STANDBY causes the HP 30310A Power Supply, which furnishes the DC power for operation of the HP 30311A Power Supply for lower memory, to remove the HP 30310A DC power. A second section of the switch opens the DCE line to the HP 340311A thus inhibiting even battery backup outputs to lower memory. The UPPER 128K MEMORY switch removes power from upper memory the same way in systems with a memory larger than 128K.

The HP 30310A Power Supplies provide control signals for use when multiple supplies are "control paralleled". These signals are DC Enable (DCE), Power Supply Up (PSU), Line Power Up (LPU), and control common 4 .

PSU indicates that all DC output voltages in the system are above specified limits. LPU indicates that the AC line voltage is above a specified limit. When the PSU, LPU, DCE, and control common 4 signals of multiple HP 30310A Power Supplies are wired in parallel, any one supply can provide the PON and PFW signals to the system, and all HP 30310A Supply outputs can be controlled by a single DCE signal. The DCE signal also controls the HP 30312A Power Supply output.

4-12. Operating Modes

The MOS semiconductor memory used by this computer system requires that operating power be constantly available. If system power fails memory is lost. Therefore, a backup battery is supplied which continues to supply power to memory during short periods of system shut down or loss of power. The battery is located in the HP 30311A Power Supply which normally furnishes the power used by memory. A second function of the power supply is to keep the battery charged.

When considering operations involving the memory power supply, there are two general practices to avoid. These are:

a. Avoid those procedures and practices which involve shut down of an HP 30311A Power Supply turning off all power, normal and battery backup, to memory. Shut down occurs for lower memory if the LOWER 128K MEMORY switch on the DC Control Panel is set to STANDBY or if the HP 30311A Power Supply No. 1 is turned off at its front panel. Shut down occurs for upper memory if the UPPER 128K MEMORY switch on the DC Control Panel is set to STANDBY or if the HP 30311A Power Supply No. 2 is turned off at its front panel. If a shut down occurs, the corresponding lower or upper segment of memory will be destroyed and the operating system must be restored to its assigned locations in memory.

b. Avoid prolonged unnecessary operation on battery backup power. Memory is using battery backup power to refresh itself when the SYSTEM ON/STANDBY switch on the DC Control Panel is set to STANDBY (during maintenance procedures on non-memory modules) or during periods of AC power failure. Statements implying that the battery can supply refresh power to the memory for approximately 40 to 90 minutes (depending on the size and power demands of memory) are valid only if the battery is fully charged and in excellent condition. (The system service manual provides information on the care of batteries.) The design intent of the battery backup feature is to carry the system through AC line power failures and short (approximately 15-minute) preventive maintenance operations.

The system operates in various modes imposed by the characteristics of the semiconductor memory and the influence these characteristics had on the design of the HP 30311A Power Supply. These operating modes or equipment states are listed along the top of Tables 4-19 and 4-20. They are:

a. Normal Operation

b. Non-Memory Module PCA Replacement

c. Memory Module PCA Replacement

d. Extended Shutdown

e. Battery Test

f. System AC Power Failure

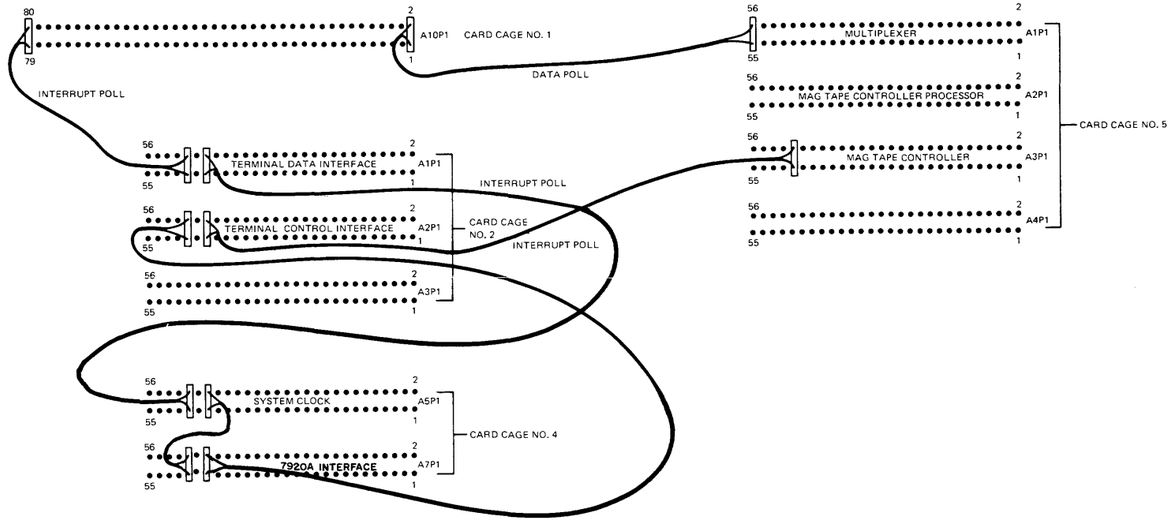
4-13. NORMAL OPERATION. Normal operation is when a battery is installed in a power suppy and the power supply is producing all output voltages to specifications. The BATTERY STATUS indicators may show either a charging (flashing at a 0.5Hz rate) or fully charged (continuously on) condition. The HP 30310A Power Supply furnishing power to the HP 30311A Power Supply must also be operating normally. Even though a system may be configured with 128K words of memory or less, both the LOWER 128K MEMORY and UPPER 128K MEMORY toggle switches on the DC Control Panel must be in the ON position to enable all power supplies in the system.

NOTE

Prior to performing any maintenance or shut down procedures, have the System Operator verify that all jobs/sessions have been terminated before setting an operating mode other than Normal Operation.

Table 4-16. Controller Interrupt Polling

CONTROLLERS BY RANK	
First	Terminal Data Interface
	System Clock/Console
	Paper Tape Reader
	Synchronous Single Line Controller
	7905A Cartridge Disc
	2660A Disc Drive
	7900A Cartridge Disc
	2888A Disc File
	Terminal Control Interface
	Hardwired Serial Interface
	Calcomp Plotter
	Programmable Controller
	Digital Magnetic Tape Unit
	Line Printer
	Card Reader
	Card Reader/Punch
	Card Punch
Last	Paper Tape Punch
Note:	Where there are duplicate controllers, they should be polled as a group in the sequence.



NOTES: WHITE OF INTERRUPT POLL AND DATA POLL TWISTED PAIRS IS UP (EVEN PIN) AT A10P1 AND DOWN (ODD PIN) AT I/O INTERFACES.

Figure 4-4. Typical Interrupt Poll Cabling

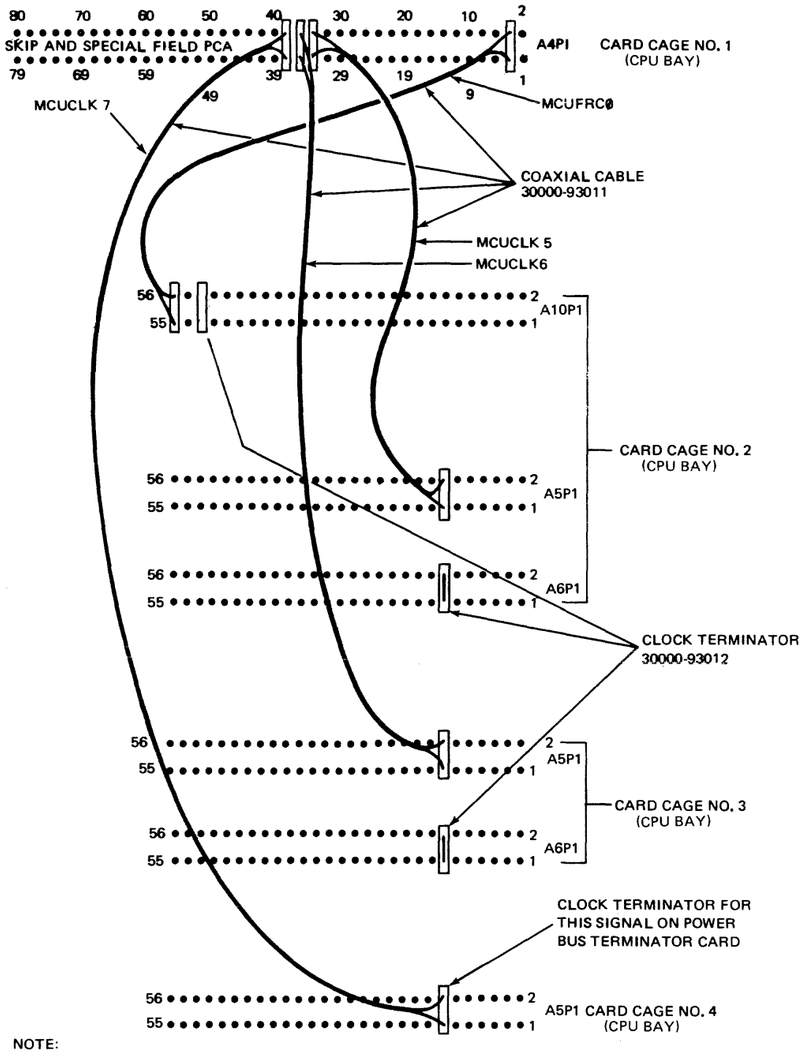


Figure 4-5. Clock Jumpers and Terminators for CPU Bay (All Models)

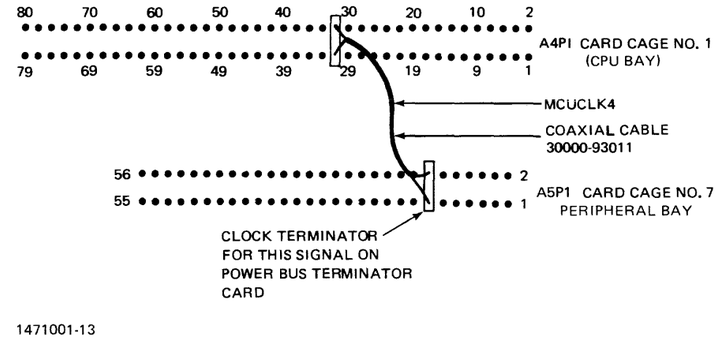


Figure 4-6. Clock Jumpers and Terminators for PIO Bay (Models 5, 6, and 7)

Table 4-17. Data Service Request

SR#	Device Name	Product Number	Transmission Mode
0	Reserved-Selector Channel Test PCA	30033A	S,C
-	7905A Cartridge Disc	30129A	C
1	2888A Disc File	30102A	S,C(1)
2	7900A Cartridge Disc	30110A	S
3	7970B/E Magnetic Tape	30115A	S
4	Hardwired Serial Interface	30360A	S
5	Hardwired Serial Interface	30360A	S
6	Card Reader	30106A/7A	S
7	Synchronous Single Line Controller	30055A	S
8	Synchronous Single Line Controller	30055A	S
9	CalComp Plotter	30126A	S
10	Paper Tape Punch	30105A	A
11	Programmable Controller	30300A/1A	A
12	Line Printer	A11	A
13	Line Printer	A11	A
14	Paper Tape Reader	30104A	D
15	Reader/Punch	30119A	D

Transmission Mode

C = Selector Channel
S = Multiplexer Channel (Synchronous)
A = Multiplexer Channel (Asynchronous)
D = Direct I/O Mode Only
(1) = Configure on multiplexer channel only.

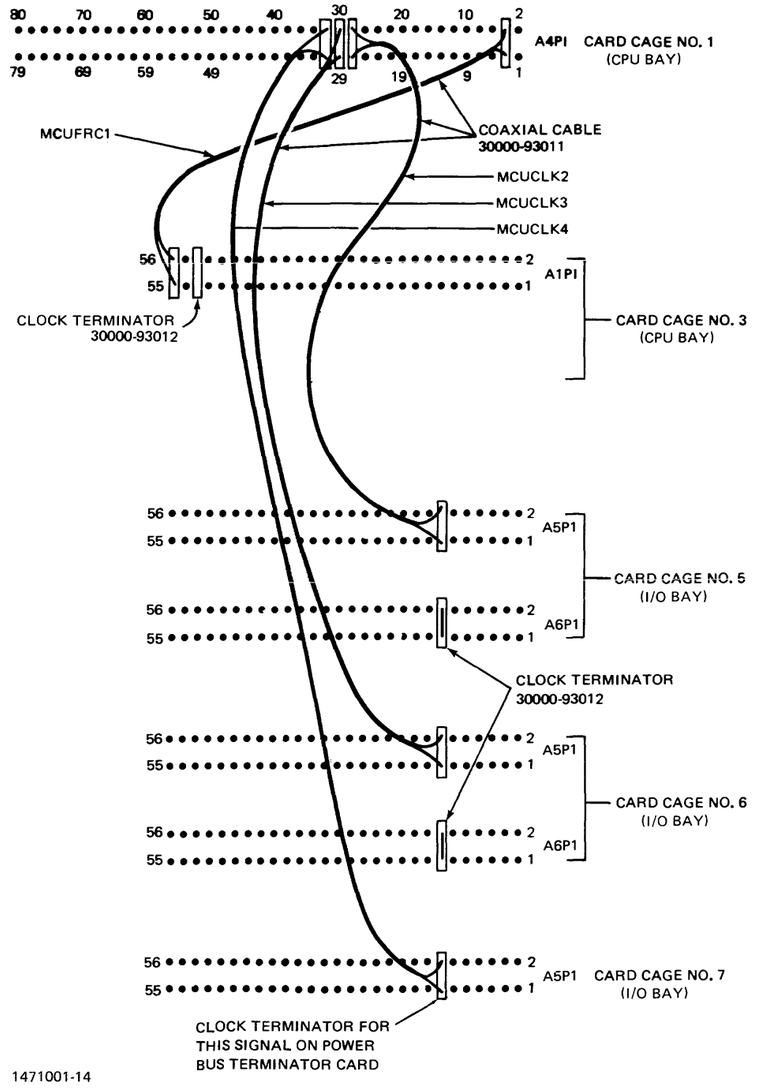
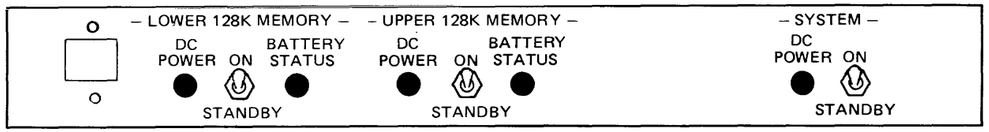
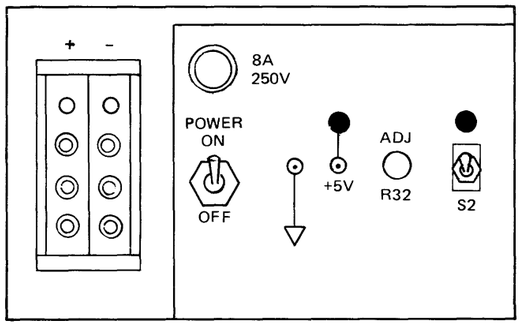


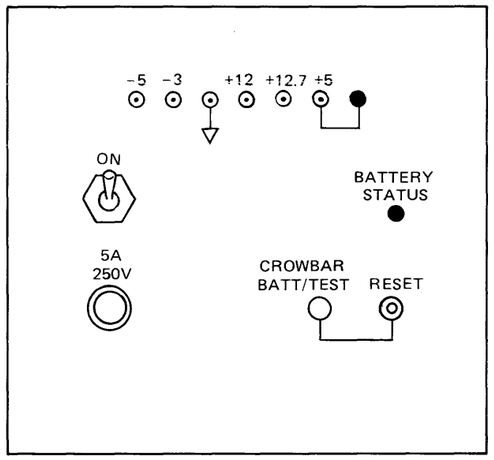
Figure 4-7. Clock Jumpers and Terminators for I/O Bay (Models 8 and 9)



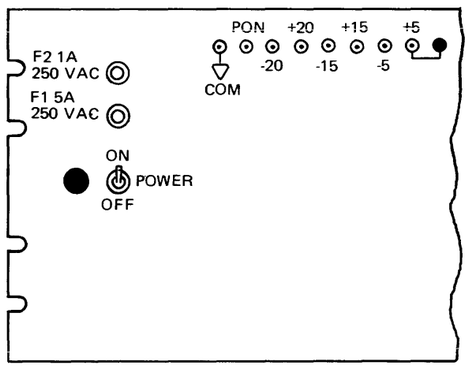
A. DC CONTROL PANEL



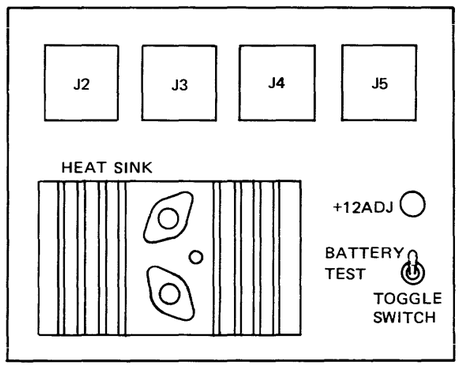
B. HP 30312A POWER SUPPLY



C. HP 30311A POWER SUPPLY



D. HP 30310A POWER SUPPLY



E. HP 30311A POWER SUPPLY (REAR VIEW)

⊙ = TEST POINT
● = INDICATOR

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Figure 4-8. Power Controls and Indicators

Table 4-18.Power Control and Indicator Functions

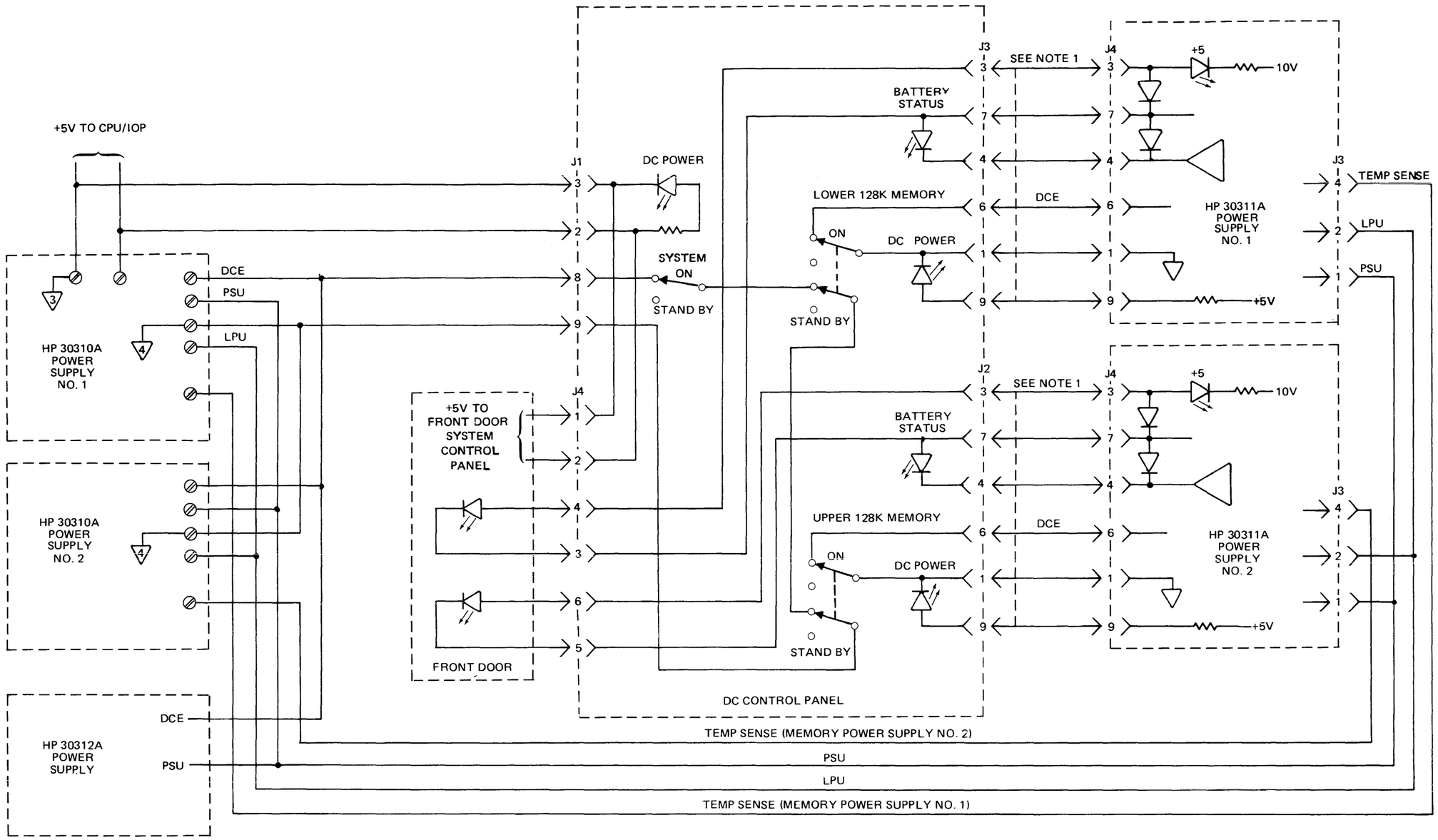
DC Control Panel	Function
SYSTEM ON/STANDBY toggle switch.	In the ON position, enables DC voltage outputs of the HP 30310A and 30312A Power Supplies. In STANDBY, all DC power supply outputs are disabled. Batteries are then sustaining memory.
SYSTEM DC POWER indicator	Implies that system DC power is on by using +5 volts from the HP 30310A Power Supply to light its LED.
UPPER 128K MEMORY ON/STANDBY 2-pole toggle switch	In the ON position, one pole generates a DC Enable signal to its HP 30311A Power Supply. If the power supply is turned on, and if the SYSTEM ON/STANDBY and LOWER 128K MEMORY ON/STANDBY switches are ON, the power supply will power memory and maintain the charge on its battery. If either or both of these other switches are set to STANDBY, the HP 30311A powers memory by its battery backup power to the memory "refresh" circuits.. The second pole maintains continuity of the system DC Enable line which enables the HP 30310A and HP 30312A Power Supply outputs. In the STANDBY position, the system DC Enable line is opened and all DC power supply outputs, except battery backuppower to the lower 128K of memory, are disabled.
UPPER 128K MEMORY DC POWER indicator	Indicates that upper memory power is on by using +5 volts from HP 30311A Power Supply No. 2 to light this LED.
UPPER 128K MEMORY BATTERY STATUS indicator	Indicates battery status of HP 30311A Power Supply No. 2 by being on, flashing, or off.
LOWER 128K MEMORY ON/STANDBY toggle switch	In the ON position, one pole generates a DC Enable signal to its HP 30311A Power Supply. If the power supply is turned on, and if the SYSTEM ON/STANDBY and UPPER 128K MEMORY ON/STANDBY switches on ON, the power supply will power memory and maintain the charge on its battery. If either or both of these other switches are set to STANDBY, the HP 30311A powers memory by its battery backup power to the memory "refresh" circuits. The second pole maintains continuity of the system DC Enable line which enables the HP 30310A and HP 30312A Power Supply

Table 4-18. Power Control and Indicator Functions (Continued)

	outputs. In the STANDBY position, the system DC Enable line is opened and all DC power supply outputs, except battery backuppower to the upper 128K of memory are disabled.
LOWER 128K MEMORY DC POWER indicator	Indicates that lower memory power is on by using +5 volts from HP 30311A Power Supply No. 1 to light this LED.
LOWER 128K MEMORY BATTERY STATUS indicator	Indicates battery status of HP 30311A Power Supply No. 1 by being on, flashing or off.
HP 30310A Power Supply	Function
POWER ON/OFF toggle switch and indicator	Indicator lights when toggle switch is ON connecting AC power to power supply circuits. OFF position disables the HP HP 30310A.
HP 30311A Power Supply	Function
Power ON/OFF toggle switch	In ON position, connects "+20 volts" terminal from the HP 30310A Power Supply to the HP 30311A circuits to maintain the charge on the battery and to develop the required memory operating voltages. Off (down) position disables the HP 30311A and disconnects the battery to prevent discharging.
BATTERY TEST momentary toggle switch	Places power supply in a battery discharge mode for test purposes (simulates a power failure). Lights the battery test indicator.
RESET pushbutton	Resets the battery discharge mode returning the power supply to normal operation. Turns off the battery test indicator.
+5 indicator	When lighted, indicates that +5 volts is being produced by the HP 30311A Power Supply.

Table 4-18. Power Control and Indicator Functions (Continued)

CROWBAR/BATT TEST indicator	Used in conjunction with the BATTERY STATUS indicator to determine if the crowbar circuit has fired and shut down the power supply.
BATTERY STATUS indicator	Indicates battery condition by: a. Being on continuously for fully-charged condition. A bad (open) battery will also produce this condition. b. Flashing at 2 Hz when discharging c. Flashing at 0.5 Hz when charging d. Being off if battery is low or not installed.
HP 30312A Power Supply	Function
POWER ON/OFF toggle switch	The ON position connects AC power to the power supply circuits. The OFF position removes AC power.
ADJ R32 potentiometer, S2 momentary toggle switch, and LED	The potentiometer is adjusted while the toggle switch is pressed until the LED in the upper right of the front panel lights and just goes out. When the toggle switch is released, the threshold level is incremented by 10 amperes.



NOTES:
1. ONE 9-CONDUCTOR 30311-60007 CABLE PER 30311A SUPPLY. PINS 2-2, 5-5, AND 8-8 ARE SPARES.
2. ANY ADDITIONAL HP 30311A POWER SUPPLIES INCLUDED IN THE SYSTEM HAVE CONTROL LINES (EXCEPT TEMP SENSE) PARALLELED.

7521-19

Figure 4-9. DC Power Control Circuits

4-14. NON-MEMORY MODULE REPLACEMENT. This operating mode is useful when it becomes necessary to remove or replace a PCA in a functional area of the computer other than memory. The mode is set by setting the SYSTEM toggle switch on the DC Control Panel to STANDBY thereby shutting down all system power supplies. Since the LOWER 128K MEMORY and UPPER 128K MEMORY switches remain ON, the memory is receiving battery backup power for memory refreshing. If the system is to remain in this mode considerably longer than 15 minutes, it is recommended that the Extended Shut Down mode be implemented. To return the system to Normal Operation, set the SYSTEM switch to ON. The BATTERY STATUS indicators may start flashing at a 0.5Hz rate to indicate a battery charging state if the memory consumed enough battery power during the shut down.

4-15. MEMORY MODULE PCA REPLACEMENT. When it becomes necessary to remove or replace a memory control and logging PCA or a memory array PCA in a PCA module containing either the lower segment of memory or the upper segment of memory, all power including backup power to the module must be interrupted by placing either the LOWER 128K MEMORY or UPPER 128K MEMORY switch to STANDBY. If memory has a lower and an upper segment, the BATTERY STATUS indicators of the segment other than that in which the PCA replacement took place will flash at a 2Hz rate while discharging. Therefore, if the system is to remain in this mode considerably longer than 15 minutes, it is recommended that the Extended Shut Down mode be implemented. To return to Normal Operation, return as appropriate either the LOWER 128K MEMORY or UPPER 128K MEMORY switch to ON. The BATTERY STATUS indicator in which the PCA replacement did not take place may start flashing at a 0.5Hz rate to indicate a battery charging state if the memory consumed enough battery power during the shut down. The operating system must now be restored because the memory data was destroyed in the memory segment in which the PCA was replaced.

4-16. EXTENDED SHUT DOWN. The Extended Shut Down mode should be used whenever it is anticipated that the system will be shut down appreciably longer than 15 minutes. When in this mode, memory is not using battery power over an extensive period and causing an excessive drain on the battery, however, the contents of memory is lost and the operating system must be restored when the system is again turned on. This mode is entered by setting both the LOWER 128K MEMORY and UPPER 128K MEMORY switches to STANDBY. If the shut down is to continue longer than 4 hours, set the POWER switches on the HP 30311A Power Supplies to off (down) to more fully isolate the battery from the power supply circuits. The return to normal operation is made by setting the LOWER 128K MEMORY and UPPER 128K MEMORY switches to ON and, if necessary, set the POWER switches on the HP 30311A Power Supplies to ON.

4-17. BATTERY TEST. A battery test feature is incorporated in the HP 30311A Power Supply which is performed with the system halted. Press down on the BATTERY TEST switch on the rear panel of the power supply and observe the LED display on the front panel indicating discharge by flashing at a 2Hz rate. This battery test indication shows that the battery is backing up the normal memory power source. To return to Normal Operation, momentarily press the RESET pushbutton on the front panel of the power supply.

4-18. SYSTEM AC POWER FAILURE. When the system incurs an AC power failure, circuits in the HP 30311A Power Supply automatically switch to battery backup and supply backup power to memory for a duration which depends on battery condition, battery charge, and memory size. A fully charged battery can supply power to 128K words of memory up to 40 to 90 minutes, however, discharging the battery over such extensive periods should be avoided and considered only under unusual circumstances. When AC power is restored, battery backup ceases, the battery starts charging, and the battery status should eventually return to normal.

4-19. DC WIRING CONFIGURATIONS

There are three basic wiring configurations for the distribution of DC power and each is associated with a particular type of cabinet. The cabinet which contains the central processor unit is called the CPU cabinet and has its own wiring configuration. The cabinet which contains the peripheral device (magnetic tape unit) and one card cage for I/O device controllers is named the Peripheral I/O (or PIO) cabinet. The PIO cabinet has its own wiring configuration. A cabinet added to a system to greatly increase the I/O capabilities of the system is called the I/O cabinet. An I/O cabinet is also added to a system having over 128K words of memory to house the power supply for the increased memory. The I/O cabinet has its own configuration.

4-20. CPU Cabinet

The DC voltage distribution is shown in Figure 4-10. The left side of the figure shows the distribution of the outputs of the HP 30310A and HP 30311A Power Supplies. The distribution of 5-volt outputs of the HP 30312A Power Supply is shown on the right side of the figure. If the wiring and connections shown on the right were taken and superimposed on the wiring and connections shown to the left (like an overlay), the resultant combination would be representative of the actual wiring configuration.

Table 4-19. Switch Positions and Light Indications (Up to 128K Memory)

CONTROLS AND INDICATORS			OPERATING MODES					
			Normal Operation	Non-Memory Module PCA Replacement	Memory Module PCA Replacement	Extended Shutdown	Battery Test	System AC Power Failure
SYSTEM DC CONTROL PANEL	SYSTEM	ON/STANDBY (switch)	ON	STANDBY	ON (1)	STANDBY	ON	ON
		DC POWER (indicator)	ON	OFF	OFF	OFF	ON	OFF
	LOWER 128K MEMORY	ON/STANDBY (switch)	ON	ON	STANDBY	STANDBY	ON	ON
		DC POWER (indicator)	ON	ON	OFF	OFF	ON	ON
		BATTERY STATUS (indicator)	ON (2)	Flashing 2Hz rate	OFF	OFF	Flashing 2Hz rate	Flashing 2Hz rate
	UPPER 128K MEMORY	ON/STANDBY (switch)	ON	ON	ON	ON	ON	ON
		DC POWER (indicator)	OFF	OFF	OFF	OFF	OFF	OFF
		BATTERY STATUS (indicator)	OFF	OFF	OFF	OFF	OFF	OFF
LOWER MEMORY HP 30311A POWER SUPPLY		ON/off (switch)	ON	ON	ON	OFF	ON	ON
		+5 (indicator)	ON	ON	OFF	OFF	ON	ON
		BATTERY STATUS (indicator)	ON (2)	Flashing 2Hz rate	OFF	OFF	Flashing 2Hz rate	Flashing 2Hz rate
		CROWBAR/BATT TEST (indicator)	OFF	OFF	OFF	OFF	ON	OFF

1 Switch may be in either position during PCA replacement, however, it must be set to ON when returning to normal operation.

2 If battery is charging indicator may be flashing at 0.5 Hz rate.

Table 4-20. Switch Positions and Light Indications (Over 128K Memory)

CONTROLS AND INDICATIONS			OPERATING MODES					
			Normal Operation	Non-Memory Module PCA Replacement	Memory Module PCA Replacement	Extended Shutdown	Battery Test	System AC Power Failure
SYSTEM DC CONTROL PANEL	SYSTEM	ON/STANDBY (switch)	ON	STANDBY	ON (1)	STANDBY	ON	ON
		DC POWER (indicator)	ON	OFF	OFF	OFF	ON	OFF
	LOWER 128K MEMORY	ON/STANDBY (switch)	ON	ON	ON	STANDBY	ON	ON
		DC POWER (indicator)	ON	ON	ON	OFF	ON	ON
		BATTERY STATUS (indicator)	ON (3)	Flashing 2Hz rate	Flashing 2Hz rate	OFF	ON	Flashing 2Hz rate
	UPPER 128K MEMORY	ON/STANDBY (switch)	ON	ON	STANDBY (2)	STANDBY	ON	ON
		DC POWER (indicator)	ON	ON	OFF (2)	OFF	ON	ON
		BATTERY STATUS (indicator	ON (3)	Flashing 2Hz rate	OFF (2)	OFF	Flashing 2Hz rate	Flashing 2Hz rate
LOWER MEMORY HP 30311A POWER SUPPLY		ON/off (switch)	ON	ON	ON	OFF	ON	ON
		+5 (indicator)	ON	ON	ON	OFF	ON	ON
		BATTERY STATUS (indicator)	ON (3)	Flashing 2Hz rate	Flashing 2Hz rate	OFF	ON	Flashing 2Hz rate
		CROWBAR/BATT TEST (indicator)	OFF	OFF	OFF	OFF	OFF	OFF
UPPER MEMORY HP 30311A POWER SUPPLY		ON/off (switch)	ON	ON	ON	OFF	ON	ON
		+5 (indicator)	ON	ON	OFF	OFF	ON	ON
		BATTERY STATUS (indicator)	ON (3)	Flashing 2Hz rate	OFF	OFF	Flashing 2Hz rate	Flashing 2Hz rate
		CROWBAR/BATT TEST (indicator)	OFF	OFF	OFF	OFF	ON	OFF

1 Switch may be in either position during PCA replacement, however, it must be set to ON when returning to normal operation.

2 Indications are for change of PCA in upper 128K of memory. If change takes place in lower 128K of memory, ON/STANDBY will be in ON and the indicators will be ON.

3 If battery is charging indicator may be flashing at 0.5 Hz rate.

Output of the HP 30310A Power Supply is distributed as follows:

a. The three +5 "volt" terminals and the three associated ground terminals of terminal strip TB1 are connected to six of the eight terminals on the back of the CPU card cage. Positive 5 volts and ground are routed from the CPU terminal strip to connector J1 on the DC Control Panel to provide an indication of DC power on and for further routing from the front of the DC Control Panel via cable 30003-60014 to the front door logic (System Control Panel). See the upper right of Figure 4-10. Cable 30003-60014 also carries BATTERY STATUS indications to the indicators on the front door.

b. The -5 "volt" terminal is routed to card cage No. 2, jumpers from there to card cage No. 3, and jumpers again to card cage No. 4.

c. The terminals related to +20 and -20 "volts" are routed to jack J3 of the HP 30311A Power Supply as follows:

    +20 to Pins 8 and 9
    -20 to pin 7
    GND to backplane ground and then to pins 3 and 5

d. The terminals of TB3 related to +15 and -15 "volts" are routed to card cage No. 2, jumper from there to card cage No. 3, and jumper again to card cage No. 4. The +15 "volts" also goes to J3-6 of the HP 30311A Power Supply.

e. The Power ON (PON) and Power Fail Warning (PFW) signals at TB3 terminate at card cage No. 2. The remaining signals of this terminal strip were accounted for in paragraph 4-11 and Figure 4-9.

Outputs of the HP 30311A Power Supply are routes from its connector J2 to card cage No. 2 as follows:

+12.7B	from pin 8	-3B	from pin 4
+12B	from pin 9	-5B	from pin 7
+5B	from pins 3 and 6	GND	from pins 1. 2, and 5

An HP 30311A Power Supply in an adjacent I/O cabinet supplies voltages for memory in card cage No. 3 as described for card cage No. 2 in the previous paragraph if the system has more than 128K words of memory.

The HP 30312A Power Supply satisfies the 5-volt power requirements of card cages Nos. 2, 3, and 4. Card cage No.3 has two high current terminal extenders at the top of its rear panel terminal strip that connect to a set of +5 "volt" and ground terminals and another pair of terminal extenders at the bottom of the terminal strip to connect to a second set of +5 "volt" and ground terminals. The 5-volt output of the HP 30312A Power Supply connect to these terminal extenders as shown in Figure 4-10 to power card cage No. 3. The top terminal extenders serve as jumpering points to carry 5 volts and ground to card cage No. 2 and the bottom terminal extenders serve as jumpering points to furnish 5 volts and ground to card cage No. 4.

4-21. I/O Cabinet (Models 8 and 9)

The DC distribution within the I/O cabinet is shown in Figure 4-11. The left side of the figure shows the power distribution of the HP 30310A and 30311A Power Supplies. The HP 30311A Power Supply is present only in systems having more than 128K words of memory. The power distribution of the outputs of the HP 30312A Power Supply is shown on the right portion of the figure. If wiring and connections shown to the right were taken and superimposed on the wiring and connections shown to the left (like an overlay), the resultant combination would be representative of the actual wiring.

Output from the HP 30310A Power Supply is distributed as follows:

a. The three +5-volt terminals and the three associated ground terminals of TB1 are connected to card cage No. 5.

b. The -5-volt terminal is connected to card cage No. 5, jumpered from there to card cage No. 6, and again jumpered to card cage No. 7.

c. In systems having more than 128K words of memory, the terminals related to 20 volts are connected to jack J3 of the HP 30311A Power Supply as follows:

    +20 to pins 8 and 9
    -20 to pin 7
    GND to backplane then to pins 3 and 5

d. The +15 and -15 voltages at TB3 are connected to card cage No.5, jumpered from ther to card cage No. 6, and again jumpered to card cage No. 7. From card cage No. 7, a wire carries the +15 volts to the HP 30311A Power Supply in systems having over 128K words of memory.

e. The PON and PFW signals if TB3 are not used in this cabinet. The remaining signals of TB3 were accounted for in paragraph 4-11 and Figure 4-9.

The HP 30312A Power Supply satisfies the +5 volt requirements of card cages Nos. 6 and 7. Card cage No. 7 of the I/O cabinet has two metal terminal extenders connected at the top of its rear panel terminal strip and another pair of terminal extenders at the bottom. The 5-volt outputs of the HP 30312A Power Supply connect to these terminal extenders as shown in Figure 4-11, thereby furnishing +5-volt power to card cage No. 7. Jumpers extend this power to card cage No. 6.

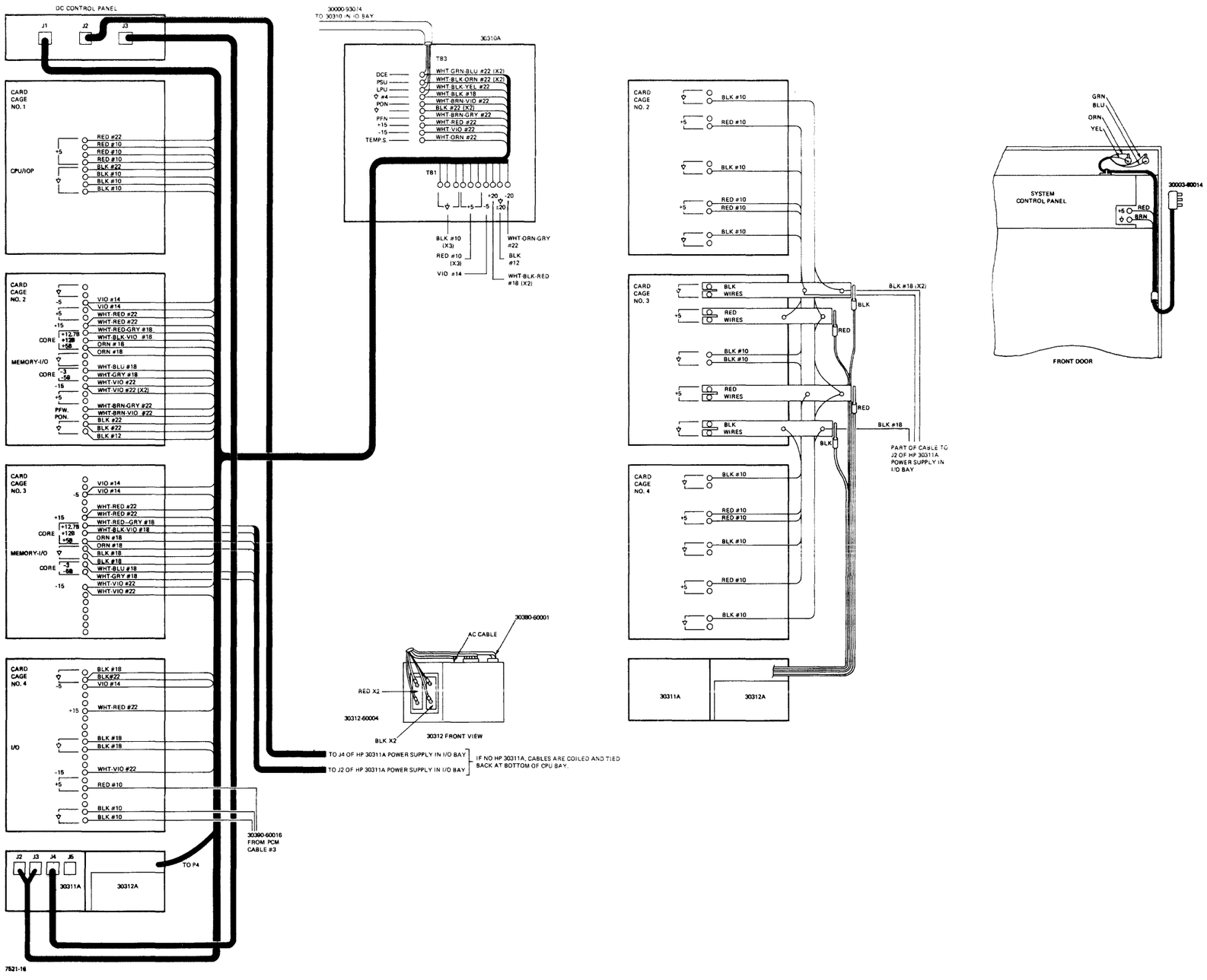


Figure 4-10. Contral Processor Unit Cabinet, DC Wiring

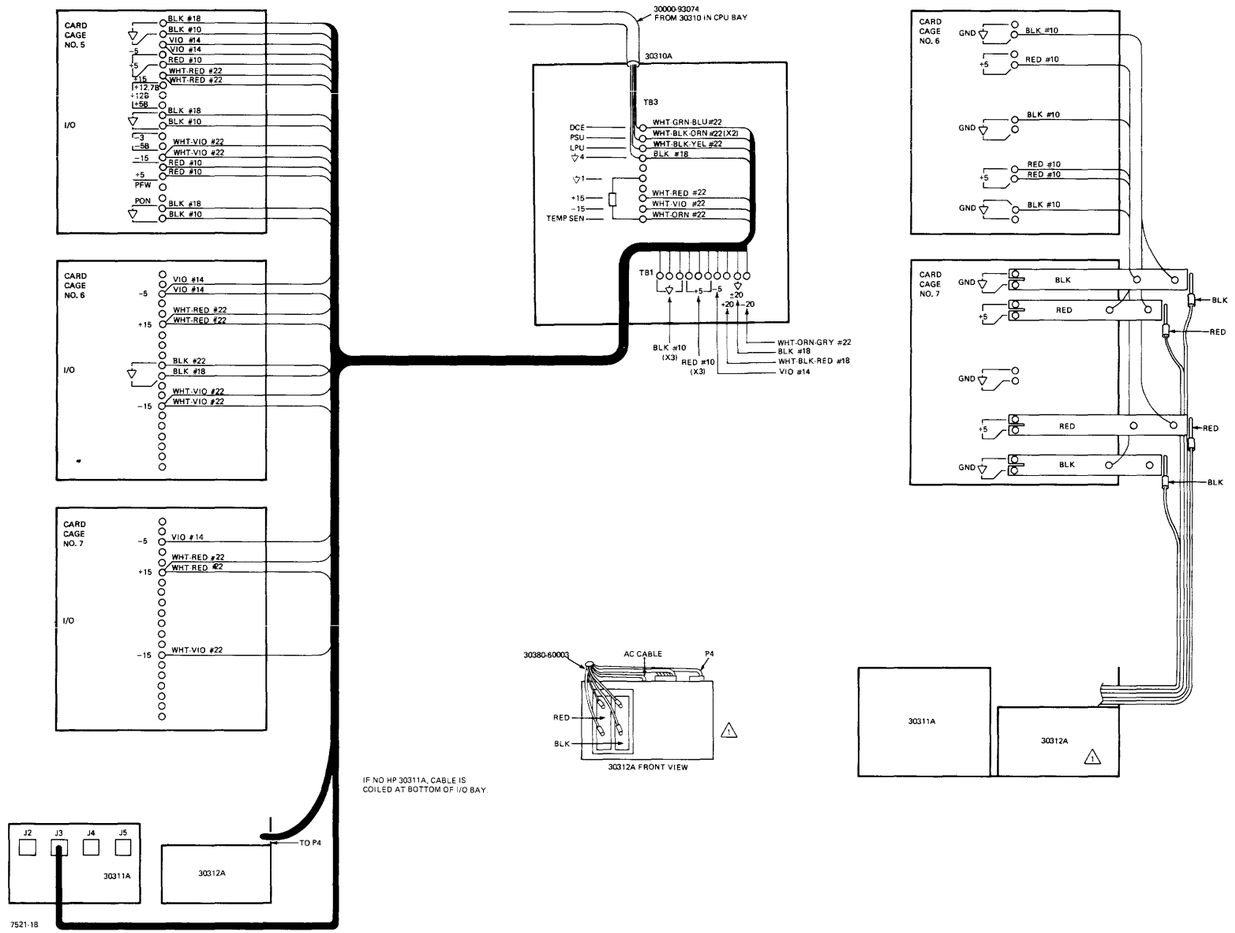


Figure 4-11. Input/Output Cabinet, DC Wiring

4-22. PIO Cabinet

The DC distribution within the PIO cabinet is shown in Figure 4-12. An HP 30310A Power Supply furnishes the DC voltages required by the interface PCAs and device controller PCAs which may be housed in card cage NO. 7. (The magnetic tape unit occupies the rack locations for card cages Nos. 5 and 6.) The DCE, PSU, LPU, and common 4 lines at TB3 connect in parallel to the same terminals of TB3 of the HP 30310A Power Supply in the CPU bay. See Figure 4-9.

4-23. AC POWER DISTRIBUTION

This part of Section IV contains information on the AC power circuits inside the cabinets of the computer system. Connections from the user's user's power mains to the computer system should be performed by the user's electrical contractor in accordance with instructions in the Site Preparation Manual. The computer system can be powered using one of the following power sources.

a. 120/208 volts, 60 hz, 3 phase, 4 wire plus earth wire

b. 230 volts, 50 Hz, 1 phase, 2 wire plus earth wire

As defined in Section III, there are four basic types of cabinets (bays); the CPU bay, the I/O bay, the peripheral I/O (PIO) bay, and the peripheral bay.

4-24. CPU Bay

The CPU bay contains the CPU/IOP card cage, three card cages containing memory and with some room for I/O hardware, and at the bottom rear of the bay the power control module (PCM). The PCM satisfies the mainframe AC power requirements for all but very large systems.

Main power is brought through a line filter into a circuit breaker. (Detailed internal circuits of the PCM are not shown in Figure 4-13.) With the circuit breaker ON, power is routed to the service strip, made available at pins 6 through 9 of TB3 for other bays, applied to a 24-volt power supply in the PCM. The service strip has nine CEE-22 230-volt receptacles and is fuse protected. It furnishes power to the HP 30310A and 30312A Power Supplies and to fans in the four card cages besides the blower shown in Figure 4-13.

The DC power supply in the PCM furnishes DC power to the emergency off circuits which remove all system power when the EMERGENCY OFF pushbutton at the upper right of the CPU cabinet is pressed. (When the front door of the CPU cabinet is closed, the EMERGENCY OFF push- button can be operated by a pushbutton extension at the upper right of the door.) Connector J1 routes the DC power to the EMERGENCY OFF switch an indicator and returns the switched DC to the trip coil of the circuit breaker. Connector J2 is terminated with plug P2 to complete the lamp return of the emergency off circuit to ground. Connector J2 may also

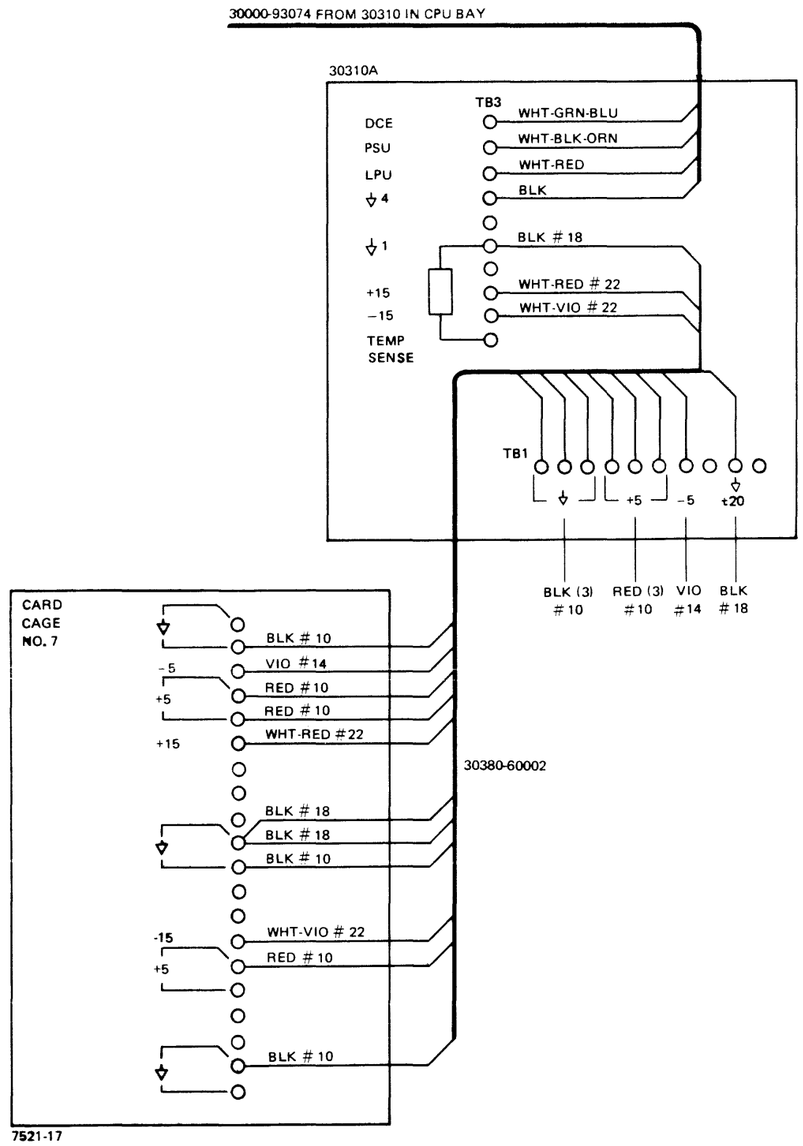


Figure 4-12. Peripheral and Input/Output Cabinet, DC Wiring

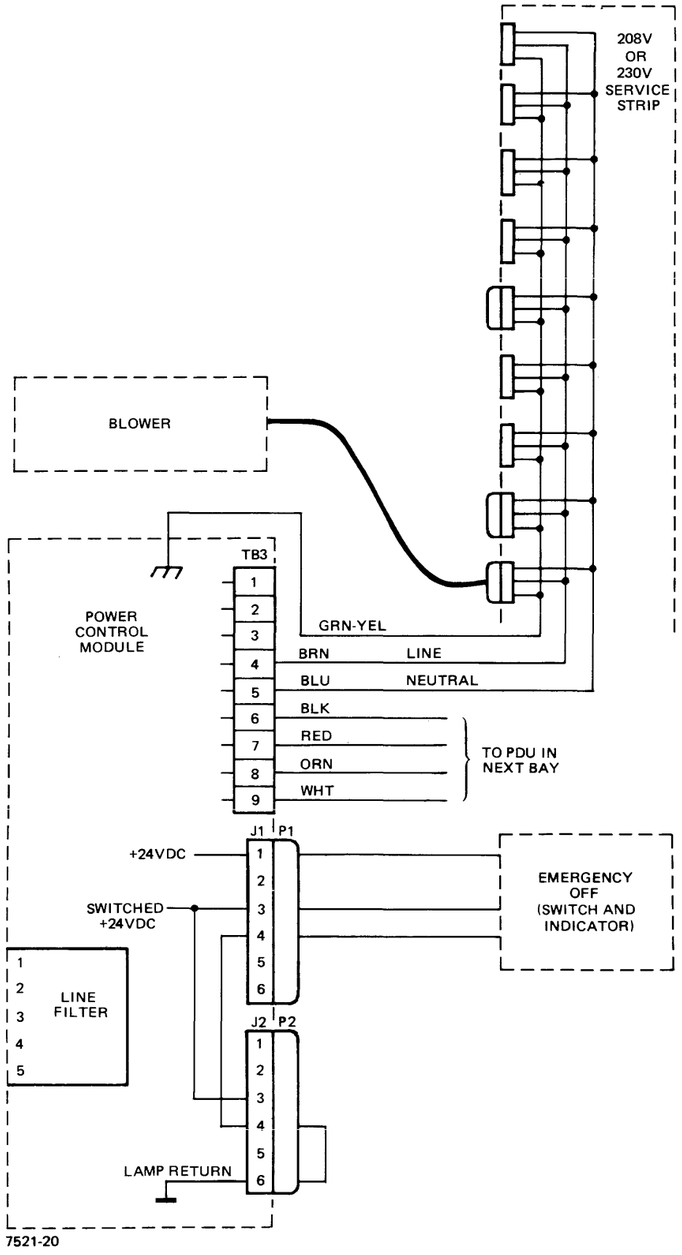


Figure 4-13. AC Distribution CPU Cabinet

extend the emergency off feature to an HP 30330A Power Control Unit in an auxiliary bay. The panel cover of the PCM must be removed to access connectors J1 and J2. A three-pin connector can be accessed without removing the cover. This connector makes logic power from the CPU bay available to power the logic of the maintenance panel you use to evaluate system performance.

Terminal boards TB1 and TB2 (not shown) are strapped according to the customer's type of input power source. See the following table.

PCM Strapping Connections

	(120/208V, 3 PH, 60 Hz)	(230V, 1 PH, 50 Hz)
TB1	1 to 2 3 to 4 4 to 5	2 to 3 5 to 6 ------
TB2	4 to 5	5 to 6

4-26. AUXILIARY CABINETS

Auxiliary cabinets are non-CPU cabinets used for housing the components of the I/O bays, PIO bays, and peripheral bays. The wiring from TB3 of the PCM to the power distribution unit (PDU) of any auxiliary cabinet and then from PDU to PDU is identical regardless of user power source type. This may be seen in Figures 4-14 and 4-15. It is the strapping of TB1 in the PDU that adapts the cabinet to operate on the customer's power. See the following table.

PDU Strapping Connections

	120/208 VAC 3 PH 60 Hz			230 VAC 50 Hz
Bay position relative to PCM if PCM = 1	2, 5, 8, 11, etc.	3, 6, 9, 12, etc.	4, 7, 10, 13, etc.	2, 3, 4, 5, etc.
Strapping at TB1	2-3 4-5 4-7 8-9 9-10	1-2 4-5 7-8 8-9 10-11	1-2 3-4 6-7 8-9 9-10	1-2 5-6 9-10

The strapping plan of the 3 phase balances the load with the CPU bay using one phase, the next bay a second phase, the next bay a third phase, etc. while adding cabinets until the limit of 30 amperes per phase is about to be exceeded. An I/O cabinet does not have the 115-volt service strip.

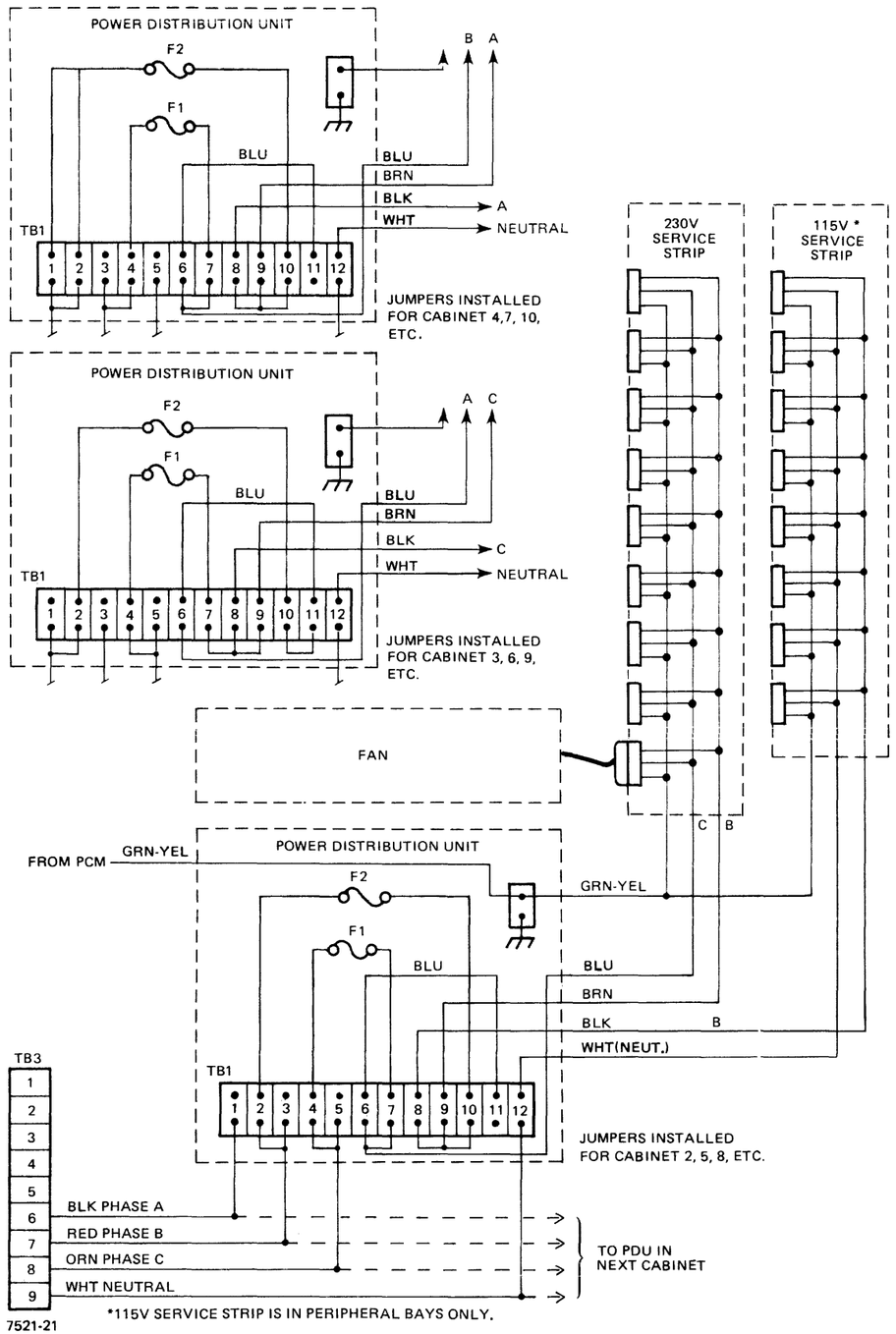


Figure 4-14. AC Distribution, Auxiliary Cabinets (120/280V, 3 PH, 60 Hz)

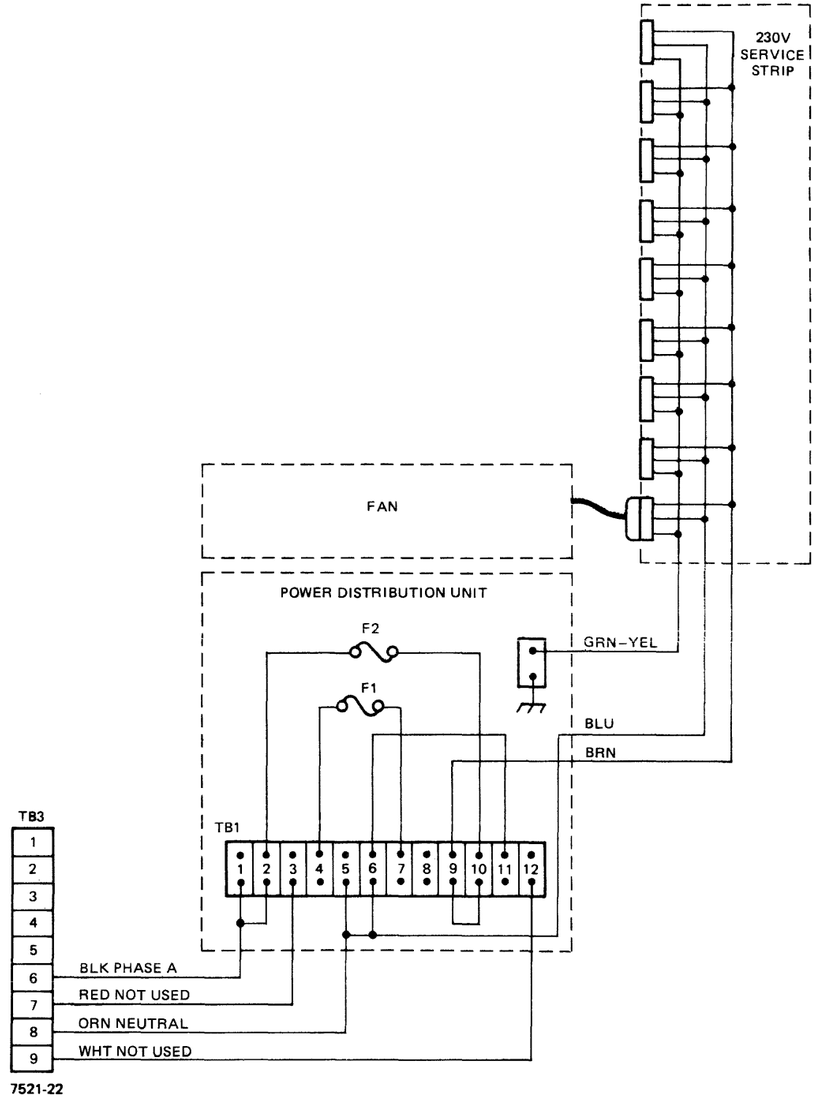


Figure 4-15. AC Distribution, Auxiliary Cabinets (230V, 1 PH, 50 Hz)

DIAGRAMS

SECTION V

5-1. INTRODUCTION

This section contains engineering diagrams for the printed circuit assemblies (PCA's) used in the system.

Each diagram set contains a schematic diagram, part location diagram, and IC index for each assembly. The diagram sets are arranged by numerical product numbers listed in Table 5-1.

5-2. SCHEMATIC DIAGRAMS

The schematic diagram contents are exact duplicates of engineering masters with no alterations to the information contained on each diagram.

5-3. PART LOCATION DIAGRAMS

Each diagram set contains a part location diagram. The part location diagram is provided as an aid in physically locating integrated circuits on the PCA.

5-4. INTEGRATED CIRCUIT INDEX

Each diagram set contains an integrated circuit index for the PCA. The integrated circuit index provides a cross reference between the integrated circuit references used on the schematic diagrams and the HP part number of the circuit. The part numbers may be used to reference a circuit description in section II.

Table 5-1. Diagrams Index

HP Product #	Title	Part Number
30003A	CPU	
	ROM PCA	30003-60001
	SSF PCA	30003-60002
	ALU PCA	30003-60003
	R-Bus PCA	30003-60004
	S-Bus PCA	30003-60005
	CIR PCA	30003-60006
	MCU PCA	30003-60007
	IOP PCA	30003-60008
	System Control Panel	30003-60012
30007B/8A/9A	ERROR CORRECTING MEMORY	
	MCL PCA	30007-60002
	SMA PCA	30008-60002
	FCA PCA	30009-60001
	FLI PCA	30009-60002
30012A	EXTENDED INSTRUCTION SET	
	EIS PCA	30012-60001
30030B	SELECTOR CHANNEL	
	Selector Channel Control PCA	30030-60003
	Selector Channel Sequencer PCA	30030-60011
	Port Controller PCA	30030-60016
	Selector Channel Register PCA	30030-60018
30031A	SYSTEM CLOCK	
	System Clock/Console Interface PCA	30031-60001
30032B	ASYNCHRONOUS TERMINAL CONTROLLER	
	TDI PCA	30032-60001
	TCI PCA	30061-60001
30033A	SELECTOR CHANNEL MAINTENANCE BOARD	
	SCMB PCA	30033-60001
30036A	MULTIPLEXER CHANNEL	
	MUX Channel PCA	30036-60001
30049C	DIAGNOSTIC HARDWARE ASSEMBLY	
	Diagnostic Hardware Assembly	30049-60003
30050A	UNIVERSAL INTERFACE	
	Universal Interface (TTL) PCA	30050-60001
30051A	UNIVERSAL INTERFACE	
	Universal Interface (Diff.) PCA	30051-60001
30055A	SYNCHRONOUS SINGLE LINE CONTROLLER	
	SSLC PCA	30055-60001
30061A	TERMINAL CONTROLLER	
	(See product 30032B)	
30102A	DISC DRIVE (HP2888A) CONTROLLER INTERFACE	
	Read/Write PCA	30202-60001
	Bus PCA	30202-60002
	Controller Processor PCA	30202-60003
30129A	CARTRIDGE DISC (HP7905A) CONTROLLER INTERFACE	
	Interface Unit PCA	30229-60001
30203A	DISC MEMORY (HP2660A) INTERFACE	
	Controller PCA	30203-60001
	Data PCA	30203-60002
30206A	CARD READER (HP2893A) INTERFACE	
	Card Reader Interface PCA	30206-60001
30210A	CARTRIDGE DISC (HP7900) INTERFACE	
	Controller Processor PCA	30202-60003
	Disc Controller PCA	30210-60001
30215A	MAG TAPE INTERFACE	
	Mag Tape (9 Track) Controller PCA	30215-60006
	Mag Tape Controller Processor PCA	30215-60002
30219A	CARD READER/PUNCH INTERFACE	
	Card Reader/Punch Interface PCA	30050-60008
30226A	PLOTTER INTERFACE	
	Plotter Interface PCA	30226-60001
30310A	POWER SUPPLY	
	HP 30310A Power Supply	30310-60024
30311A	SEMICONDUCTOR MEMORY POWER SUPPLY	
	Semiconductor Memory Power Supply	30311-60001
30312A	POWER SUPPLY	
	Power Supply	30312-60001
	Interface Board Assembly	30312-60002
30354A	MAINTENANCE PANEL	
	HP 30354A Maintenance Panel	30354-60001
	Maintenance Panel Interface PCA	30354-60003
30360A	HARDWIRED SERIAL INTERFACE	
	Hardwired Serial Interface PCA	30360-60001

30003A
CPU

ROM PCA	30003-60001	4 SHEETS
SSF PCA	30003-60002	5 SHEETS
ALU PCA	30003-60003	4 SHEETS
R-BUS PCA	30003-60004	4 SHEETS
S-BUS PCA	30003-60005	5 SHEETS
CIR PCA	30003-60006	4 SHEETS
MCU PCA	30003-60007	4 SHEETS
IOP PCA	30003-60008	4 SHEETS
SYSTEM CONTROL PANEL	30003-60012	3 SHEETS

ENGINEERING RESPONSIBILITY / SEPIA

SYM	REVISIONS	SZ	APPROVED	DATE
A	AS ISSUED 1512	A	DT / DR	3/25/75
B	DELETE S1 PAC F 1512		GSB	11/11/13
C	ADDED M1 & R12		GSB	3.12.76
D	REMOVED U/S GRADE 1, 2, & U/S 3.		GSB	4.5.76

ROM 0 1 2 3 — P1-4 3 21 24 — ROM 4 5 6 7 — P1-28 26 27 26 — ROM 8 9 10 11 — P1-28 31 32 33 — ROM 12 13 14 15 — P1-35 34 36 38 — ROM 16 17 18 19 — P1-41 42 43 44 — ROM 20 21 22 23 — P1-45 46 47 48 — ROM 24 25 26 27 — P1-51 52 53 54 — ROM 28 29 30 31 — P1-65 67 69 71

R11 — U179 — U207 — U177 — U176 — U175 — U176

R1 / R2 / R3 / R5 — +5 — 500

U25 — U26 — U27 — U28

15	45	35	65	55	85	75	105	95	125	115	145	135	165	155	SECTOR 7,6
16	46	36	66	56	86	76	106	96	126	116	146	136	166	156	SECTOR 5,4
17 -0513	47 -0522	37 -0514	67 -0903	57 -0515	87 -0904	77 -0516	107 -0905	97 -0517	127 -0906	117 -0518	147 -0907	137 -0519	167 -0908	157 -0520	SECTOR 3,2
18 -0497	48 -0506	38 -0498	68 -0507	58 -0499	88 -0508	78 -0500	108 -0509	98 -0501	128 -0510	118 -0502	148 -0511	138 -0503	168 -0512	158 -0504	SECTOR 1,0

U198 — U208 — U188 — U174 — U187 — U187

U186 — P2-6 ROMENB — R6 1K — +5

SOCKET 1200-0973 — (2K) PROM PLUG — (1K)

U206 — U164 — U216 — U206 — U204 — U174 — R8 1K — R7 — U161

V0-7 (G15) — V8-15 (G15)

P2- 11 12 13 14 18 17 27 28 — 0 1 2 3 4 5 6 7 — V

P2- 29 30 31 32 33 34 41 42 — 8 9 10 11 12 13 14 15 — V

P1-14 FRCLK — P1-79 FCLK — P1-30 EMULATOR

U14 — RCLK (G12) — R9 — R4 — CLOCK

U24 — U44 — U54 — U64 — U74 — U84 — U94 — U104 — U114

(A17) ROR 0-3 — (A17) ROR 4-7 — (A17) ROR 8-11 — (A17) ROR 12-15 — (A17) ROR 16-19 — (A17) ROR 20-23 — (A17) RORT 24-27 — (D30,D16) RORT 28-31

(D30,A18) ROR 0-3 — (D30,A18) ROR 4-7 — (A18) ROR 8-11 — (A18) ROR 12-15 — (D30,A18) ROR 16-19 — (D16,A18) ROR 20-23 — (D16,A18) RORT 24-27

U43 — U53 — U63 — U73 — U83 — U93 — U103 — U113

(A17) RORT 5-9 — RORT 20-23 (G16) — RORT 24-27 (G16) — RORT 28-31 (G16)

P2- 36,53 RORT 12 15 — P1-72 73 74 75 76 ROR 10 11 12 13 14 — P2- 38,55, 58 RORT 16 17 — P2- 57 62 RORT 18 19 — P1-57 49 50 P2-61 RORT 20 21 22 23 — P2-5,24 ROR 23 24 — P2- 63 64 65 77 RORT 24 25 26 27 — P2-37 RORT 21

+5 — R12 7.8M — M1

ROM PCA
30003-60001
Sheet 1 of 4

STOCK NO. 8280-0004 PRINTED ON DIEPO NO. 1030-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15 / 16 17 18 19 20 21 22 90 / 63 93 / 33 34 38 42 43	

SYM	REVISIONS	APPROVED	DATE
A	[illegible]	GJ / DR	3/27/75

RARGA RARGB 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 JMPIG

P2-46 P2-15 J3-19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49 P1-77

J3 20-48 (EVEN)

RBRI P1-55 | ROMFCN1 P2-22 | JMPJSB1 P2-23 | SPCLNOP1 P2-25 | SKIPNOP1 P1-13 | JSBI P1-15 | BUSOP1 P1-70

(E3) ROR 0-3 (E4) ROR 4-7 (E5) ROR 8-11 (E6) ROR 12-15 (E7) ROR 16-19 (E8) ROR 20-23 (E9) ROR 24-27

(E2) RCLK

(D12) RAR 0-3

(D11,E11) RAR 0-3

(B10) JSBI, SKIP, CLOCK

+5 R10 1K

U181 U191 U201 U211 U171 R9

U212 U182 U192 U202

U217 U183 U193 U203

U205 U204 U215 U214

U185 U184 U195 U194

RAR RAR RAR RAR ROR ROR ROR ROR RORT RORT RORT RORT

(F8) ROR 0-3 (F9) ROR 20-23 (F11) ROR 24-27

P2-44 SAVEG (F3) V0-7 (F2) V8-15 P2-43 JMP2G P2-4 VBUSENB

U61 U174 U216 U176 U126

SPARES

U123 U122 U121 U142 U141 U152 U151 U171 U191 U192 U102 U101 U112 U111 U162 U172

RBRI ROMFCN1 PUSH1 JMPJSB1 ROMFCN1 PANLRD ZEPNT RSBT JCUI1 NEXT1 UNC1 INSR1 PORT+ PORT- DECSR1 DROPT

U62 U61 U162 U174

U131 U134 U144 U164 U133 U124 U173

ROR 12-15 (E4) ROR 16-19 (E7) ROR 0-3 (F3) ROR 4-7 (F4) ROR 28-31 (F11) RORT 5-9 (E4)

JSBI (E13)

P1-12 R0 11 R1 9 R2 10 R3 61 R4 62 R5 63 R6 64 R7

P2-10 R8 9 R9 8 R10 7 R11 47 R12 48 R13 49 R14 51 R15

P2-26 SKIP

P1-56 PANLRD

P2-66 SF0 68 SF1 70 SF2 72 SF3 74 SF4

P2-56 RF0 54 RF1 52 RF2 50 RF3

P1-66 NXTG

P1-68 DISPLAY

P2-14 PNLS

P2-67 ST0 69 ST1 71 ST2 73 ST3 75 ST4

P1-5 UNC1 P1-6 NEXT1 P1-18 JCUI1 P2-3 RSBT

P2-78 CAURST P1-22 DECSR P1-29 INCSR

R4

EVPASS P1 AND P2 WITH A 39 μF TANTALUM AT EACH END.

PULLUPS

R4 330 R9 330 R11 330

E1 E2 E3 E4

32 ea. .01 μF CERAMIC C1, 3, 4, 6-25, 27, 28, 34, 36-38, 43, 44, 49

14 ea. .1 μF CERAMIC C2, 29, 31, 33, 35, 39-42, 45-47, 50

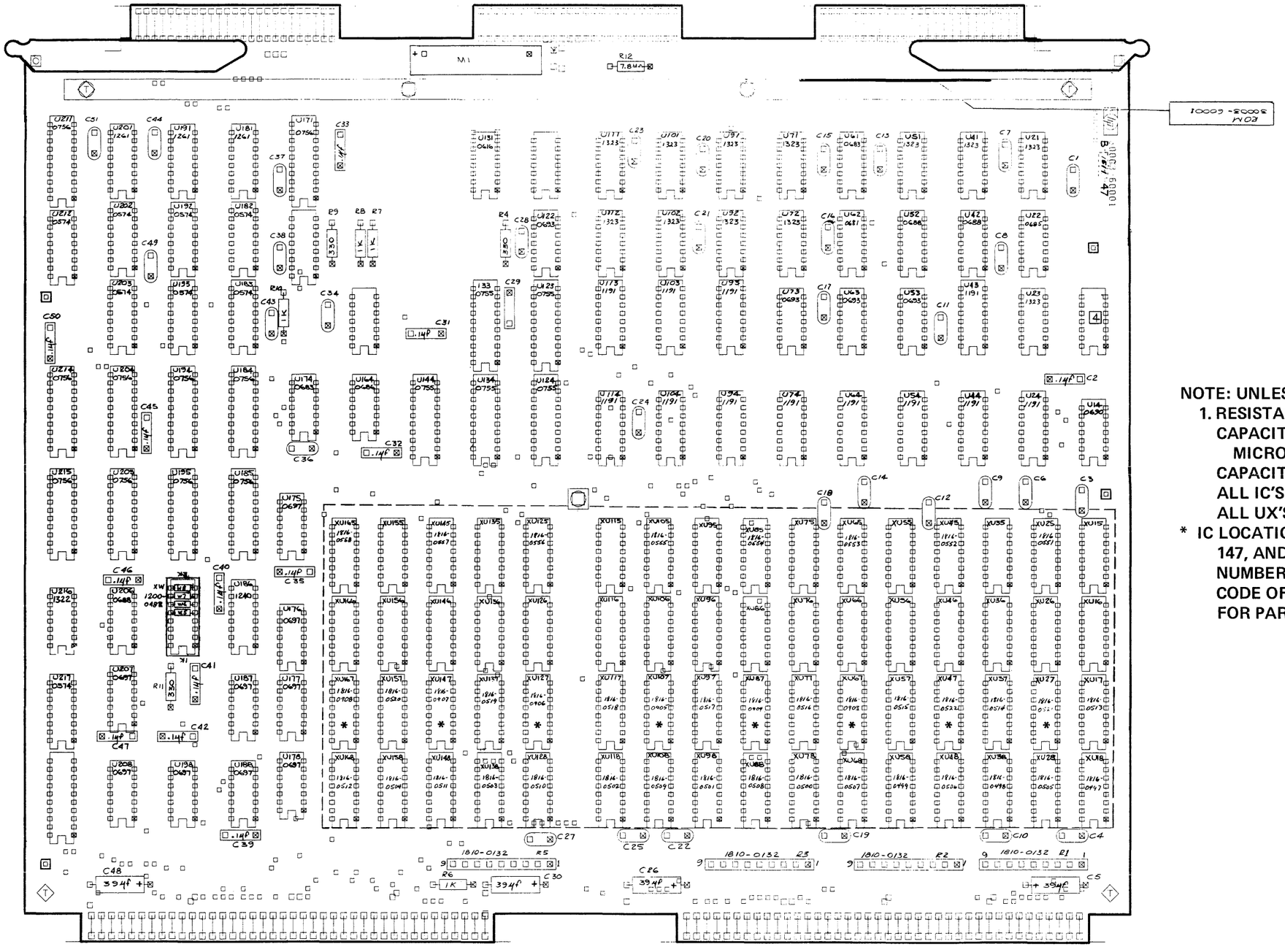
4 ea. 39 μF TANTALUM C5, 26, 30, 48

P1-19, 20, 59, 60 P2-19, 20, 59, 60

P1-1, 2, 39, 40, 80 P2-1, 2, 39, 40, 79, 80

ROM PCA
30003-60001
Sheet 2 of 4

STOCK NO 8380-0004 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT



NOTE: UNLESS OTHERWISE SPECIFIED

1. RESISTANCE IN OHMS ±5% .25W
   CAPACITANCE VALUES ARE IN MICROFARADS
   CAPACITORS ARE .01 CERAMIC DISC
   ALL IC'S ARE 1820-
   ALL UX'S ARE 1200-0482

* IC LOCATIONS U27, 47, 67, 87, 107, 127, 147, AND 167 HAVE DIFFERENT PART NUMBERS FOR PCA'S HAVING DATE CODE OF 1630. REFER TO IC INDEX FOR PART NUMBERS.

ROM PCA
30003-60001
Sheet 3 of 4

ROM PCA

30003-60001

IC Index

U	18XX-	U	18XX-	U	18XX-
14	1820-0690	XU68	1816-0507	XU135,136	1200-0482
XU15,16	1200-0482	71,72	1820-1323	XU137	1816-0519
XU17	1816-0513	73	0693	XU138	1816-0503
XU18	0497	74	1191	144	1820-0755
21	1820-1323	XU75,76	1200-0482	XU145	1816-0557
22	0685	XU77	1816-0516	XU146	1200-0482
23	1323	XU78	0500	XU147	1816-0907 *
24	1191	XU85	0554	XU148	0511
XU25	1816-0551	XU86	1200-0482	XU155,156	1200-0482
XU26	1200-0482	XU87	1816-0904 *	XU157	1816-0520
XU27	1816-0521 *	XU88	0508	XU158	0504
XU28	0505	91,92	1820-1323	164	1820-0686
XU35,36	1200-0482	93,94	1191	XU165	1816-0558
XU37	1816-0514	XU95,96	1200-0482	XU166	1200-0482
XU38	0498	XU97	1816-0517	XU167	1816-0908 *
41	1820-1323	XU98	0501	XU168	0512
42	0688	101,102	1820-1323	171	1820-0756
43,44	1191	103,104	1191	174	0683
XU45	1816-0552	XU105	1816-0555	175-178	0697
XU46	1200-0482	XU106	1200-0482	181	1261
XU47	1816-0522 *	XU107	1816-0905 *	182,183	0574
XU48	0506	XU108	0509	184,185	0756
51	1820-1323	111,112	1820-1323	186	1240
52	0686	113,114	1191	187,188	0697
53	0693	XU115,116	1200-0482	191	1261
54	1191	XU117	1816-0518	192,193	0574
XU55,56	1200-0482	XU118	0502	194,195	0756
XU57	1816-0515	122	1820-0693	198	0697
XU58	0499	123,124	0755	201	1261
61	1820-0681	XU125	1816-0556	202,203	0574
62	0681	XU126	1200-0482	204,205	0756
64	1191	XU127	1816-0906 *	206	0688
XU65	1816-0553	XU128	0510	207,208	0697
XU66	1200-0482	131	1820-0616	211	0756
XU67	1816-0903 *	133,134	0755	212	0574
				214,215	0756
				216	1322
				217	0574

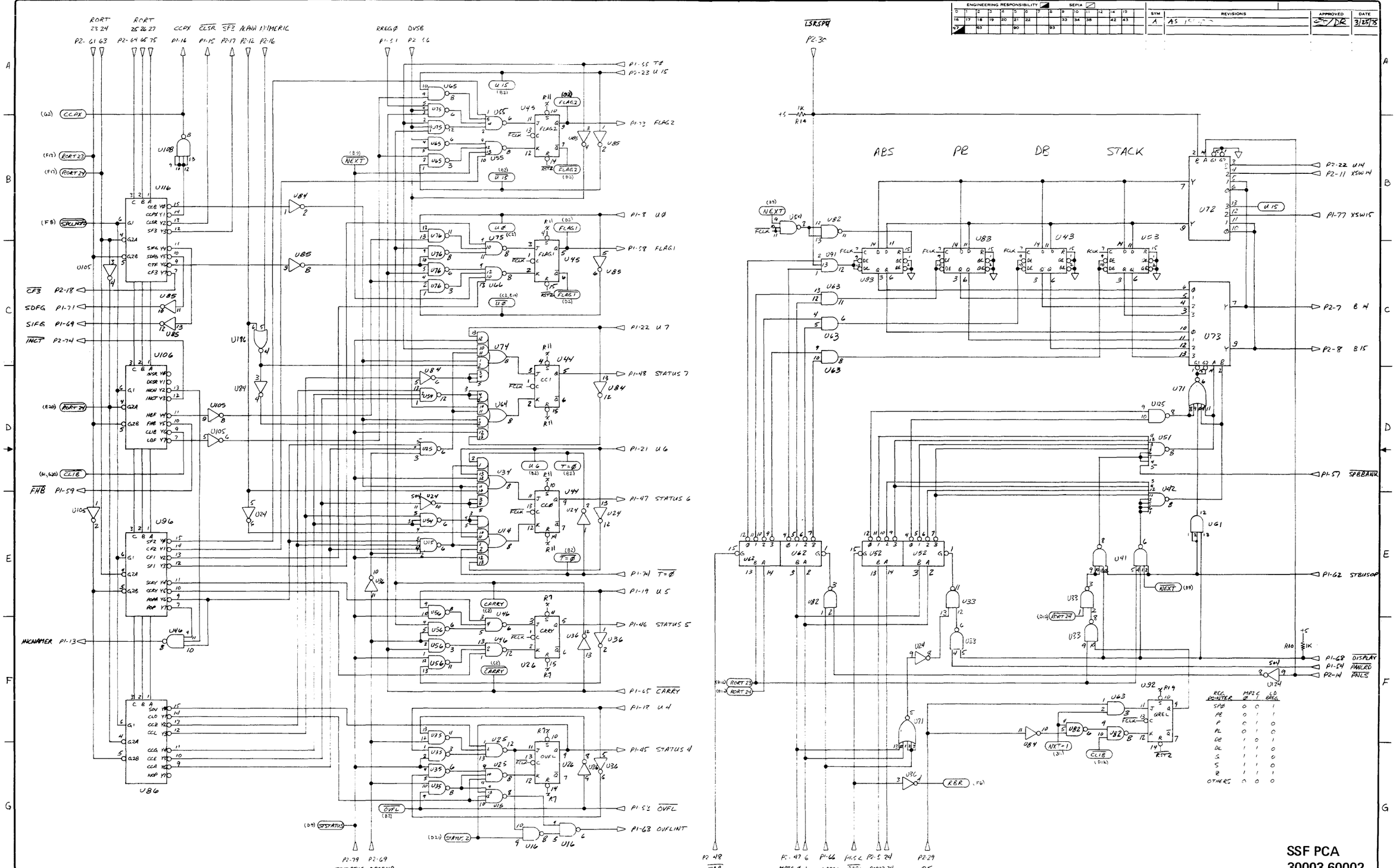
* PCA's with a date code of 1630 use the following part numbers:

U27	1816-0968
U47	1816-0969
U67	1816-0970
U87	1816-0971
U107	1816-0972
U127	1816-0973
U147	1816-0974
U167	1816-0975

ENGINEERING RESPONSIBILITY																SEPIA															
0	1	2	3	4	5	6	7	8	9	10	11	12	14	15																	
16	17	18	19	20	21	22			33	34	38		42	43																	
63				90			93																								

SYM.	REVISIONS	52	53	APPROVED	DATE
A	AS ISSUED 1512	A	A	BK/DR	3/25/75
B	ADDED 111 & R24			BK/GSB	3-25-76

SSF PCA
30003-60002
Sheet 1 of 5


ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
SYM
APPROVED
DATE
ABS
PR
DB
STACK
SSF PCA
30003-60002
Sheet 2 of 5

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS PER ECO [illegible]	[illegible] / DR	3/25/75

TEST2 TEST1 INTCLKM EXTCLK

J1-19 20 23 24 P1-64 P1-67

2XCLKOUT 2XCLK IN SYNC IN SYNC OUT

J1-27 28 31 32 J1-35 36 39 40

P2-41 PONUB

P1-20, 60
P2-20, 60

P1-2, 39, 40, 80
P2-2, 39, 40, 80

C9, 13, 22, 24 — 4 x 39 μf TANTALUM
C10, 12, 14, 17 — 4 x .1 μf CERAMIC
19 ea. .01 μf CERAMIC — C1-3, 6-8, 11, 15, 16, 18-21, 23, 25-29

NOTE: C5 = .01 μf ALSO. (IN CIRCUIT ABOVE)

INTCLKM = 1 (INTERNAL CLOCK MODE)
INTCLKM = 0
INTCLKM = 1
INTCLKM = 0
INTCLKM = 1
INTCLKM = 0
(EXTERNAL CLOCK MODE)

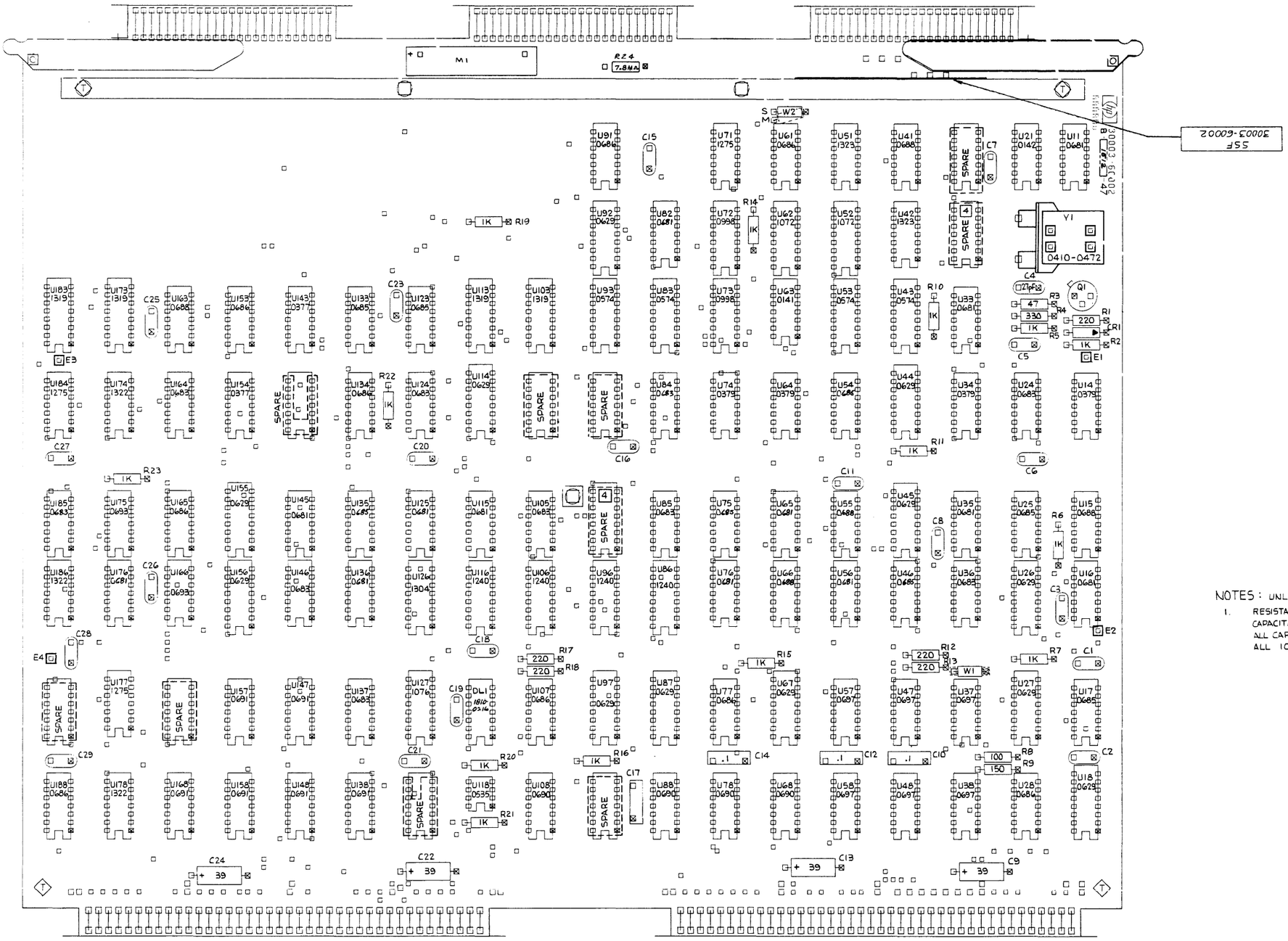
P1-61 CLKENB

P2-32 FRUNCLK
P1-1 MCUFRC0
P1-3 MCUFRC1
P1-4
P1-23 MCUCLK0
P1-24
P1-25 MCUCLK1
P1-26
P1-27 MCUCLK2
P1-28
P1-29 MCUCLK3
P1-30
P1-31 MCUCLK4
P1-32
P1-33 MCUCLK5
P1-34
P1-35 MCUCLK6
P1-36
P1-37 MCUCLK7
P1-38
P1-78 CLK
P1-76 CLK
P1-10 FRCLK
P1-79 FCLK
P2-1 FCLK

(G10) RPTFRZ
(G7) FRZ

P2-78 CP.IRST
P1-50 FRZ

SSF PCA
30003-60002
Sheet 3 of 5



SSF PCA
30003-60002
Sheet 4 of 5

SSF PCA

30003-60002

IC Index

U	1820-	U	1820-	U	1820-
11	0681	65	0681	124	0683
14	0397	66	0688	125	0681
15	0688	67	0629	126	1304
16	0681	68	0690	127	1076
17	0685	71	1275	133	0685
18	0629	72,73	0998	134	0686
21	0142	74	0379	135	0685
24	0683	75	0685	136	0681
25	0685	76	0681	137	0683
26,27	0629	77	0686	138	0691
28	0686	78	0690	153	0686
33	0681	82	0681	154	0377
34	0397	83	0574	155	0629
35	0681	84,85	0683	156	0629
36	0683	86	1240	157,158	0691
37,38	0697	87	0629	163	0688
41	0688	88	0690	164	0683
42	1323	91	0686	165	0686
43	0574	92	0629	166	0693
44,45	0629	93	0574	168	0691
46	0685	96	1240	173	1319
47,48	0697	97	0629	174	1322
51	1323	103	1319	175	0693
52	1072	105	0683	176	0681
53	0574	106	1240	177	1275
54	0685	107	0686	178	1322
55	0688	108	0690	183	1319
56	0681	113	1319	184	1275
57,58	0697	114	0629	185	0683
61	0686	115	0681	186	1322
62	1072	116	1240	188	0686
63	0141	118	0535		
64	0379	123	0685		

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15	
16 17 18 19 20 21 22 33 34 38 42 43	
63 90 93	

SYM	REVISIONS	SZ	APPROVED	DATE
A	AS ISSUED 1512	A	ES/DIR	9-25-75
B	ADDED P11 = K12		ES/GSD	3-19-76

SRREG A2-52 · SSREG P2-50 · RREG2 P1-42 · CVFL P1-44 · TØ P1-55 · T=Ø P1-74 · SAME P1-77 · ARRY P1-65 · SP3-15 P2-26 · FLAG1 P1-58

$SLOAD$ P1-12 · SHIFTCLK P1-22

U67 · U65 · U117 · U125 · U82 · U102 · U92 · U93 · U103 · U72 · U94 · U66 · U34 · U62 · U43 · U83 · U73 · U63 · U53 · U113 · U123 · U133 · U143 · U99

SILG · RILG · DCAD · XORT10 · CARRY · SP3-15 · SP1-Ø · G1-7 · G0 · A0 · Z0 · C0 · G8-15 · A1-14 · B1-14 · C15 · B15 · A15

B9 270 +5

U54 · U144 · BYPASS .1µf CERAMIC

U64 · U134 · U4-7 · U10 · U11 · U12

FCLK · U87 · U85 · U127 · U105 · U137 · U115 · R10 · R11 · R18

U76 · U86 · U106 · U126 · U95 · ALUSØ-3 · ALUM · ALUFC · FLAG3

U36 · U35 · U74 · U84 · U104 · U124 · U55 · U114 · U56 · T15

SPARES: U66 · U44 · U41 · U51 · U25 · U144 · U101 · U161 · U156 · U12 · U6 · U35 · U171 · U24 · U162

FCLK FCLK U97 X R8 · CLK CLK U107 X R8 · +5 R12 7.87 M1

R1 · R8 · R10 · R11 · C14, 27 · 25m · 2.2m · .1µf CER · 39µf TANT · C1, 2, 11, 20, 24, 31 · .01µf CER · C4, 6-10, 12, 13, 15-19, 21-23, 25, 26

P1-20, 60 · P2-20, 60 · P1-2, 39, 40, 80 · P2-2, 39, 40, 80

P2-34 A15 · P2-30 A1 · P2-29 AØ

P1-8 UØ · 14 U1 · 7 U2 · 17 U3 · P1-18 U4 · 19 U5 · 21 U6 · 22 U7 · P2-13 U8 · 11 U9 · 15 U10 · 16 U11 · P2-19 U12 · 21 U13 · 22 U14 · 23 U15

ALU PCA
30003-60003
Sheet 1 of 4

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	A= ISSUED	[illegible] DR	3/25/76

SFSAME P2-28 · ROMFRNZ P1-67 · NOP2 P1-76 · RORT 20 21 22 P1-57 49 50 · CIR7 P1-48 · FLAG2 P1-73 · CIR8 P1-56 · SP1-15 P2-31 · QASR P2-62 · QASL P2-64 · DVSB P2-57 · FH8 P1-59 · SP1IN P2-42 · SP3IN P1-15 · ENTIMER P1-31

SIFG P1-69 · 30FG P1-70 · CCPX P1-16 · P1-41 STATUS Ø

SHIFT FIELD DECODER

FUNC. FIELD DECODER

CCPX FIELD DECODER

P1-27 FIELD 2 · P1-29 FIELD 4 · P1-28 FIELD 5 · P1-34 FIELD 6 · P1-26 FIELD 7 · P1-35 FIELD 8 · P1-32 FIELD 9 · P1-38 REVSYSP · P1-43 REVMCUP · P1-46 DISP FLAG · P1-47 ICS FLAG · P1-36 SETERR · P2-27 BNDV · P2-66 JBNDV · P1-33 CNTIMER · P2-69 TRTIMFRZ · P1-37 MCUFRZ · P1-30 PWRFAIL · P2-79 IORESET · P2-78 CPURST · P2-74 PONB · P2-45 PONB

ALU PCA
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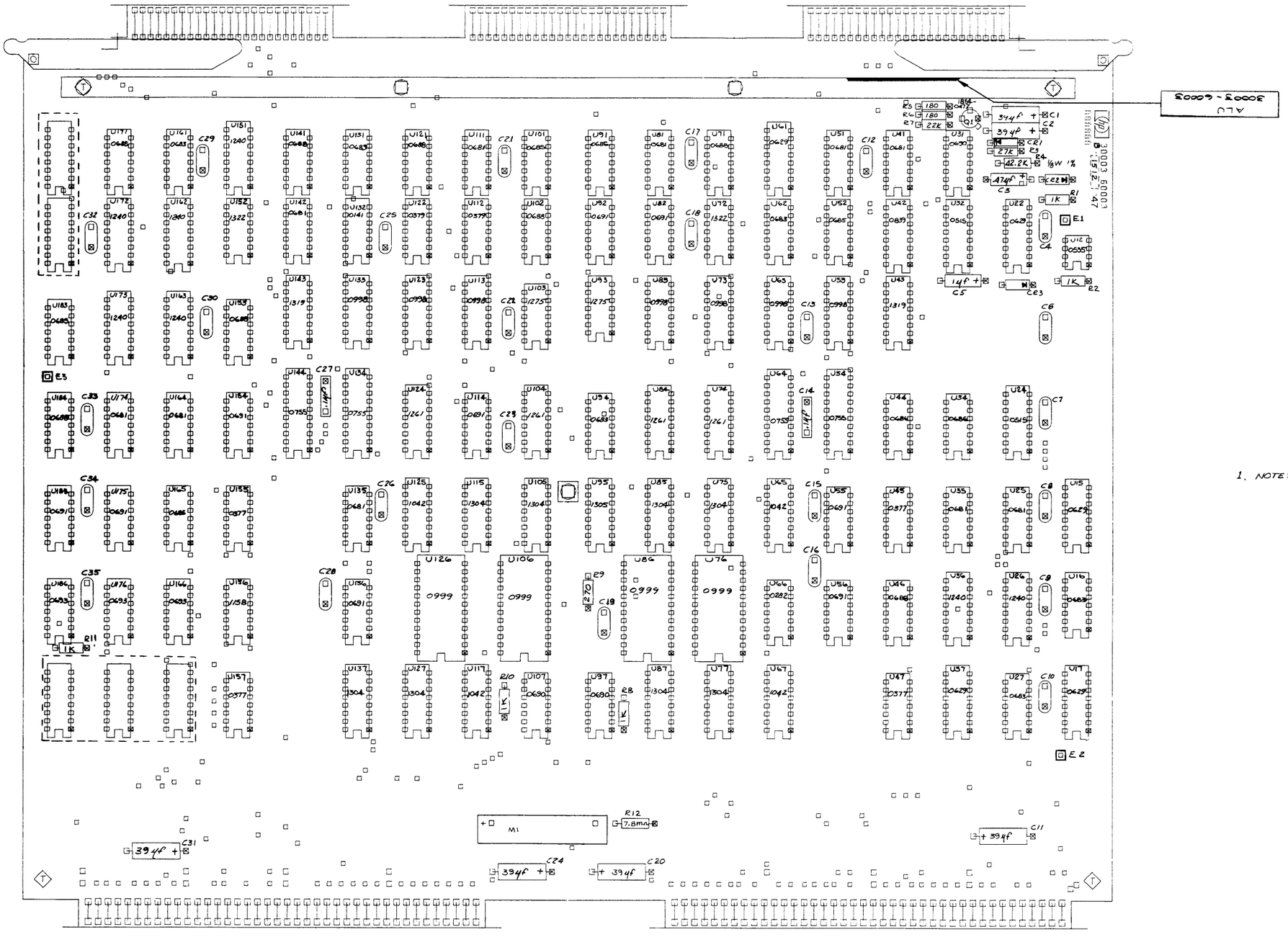
Sheet 2 of 4



1. NOTE: UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE IN OHMS ± 5%, ¼W
   ALL CAPACITANCE IN MICRO FARADS
   ALL .01 CAPACITORS ARE CERAMIC DISC.
   ALL DIODES ARE 1901-0040
   ALL IC'S ARE 1820-

ALU PCA
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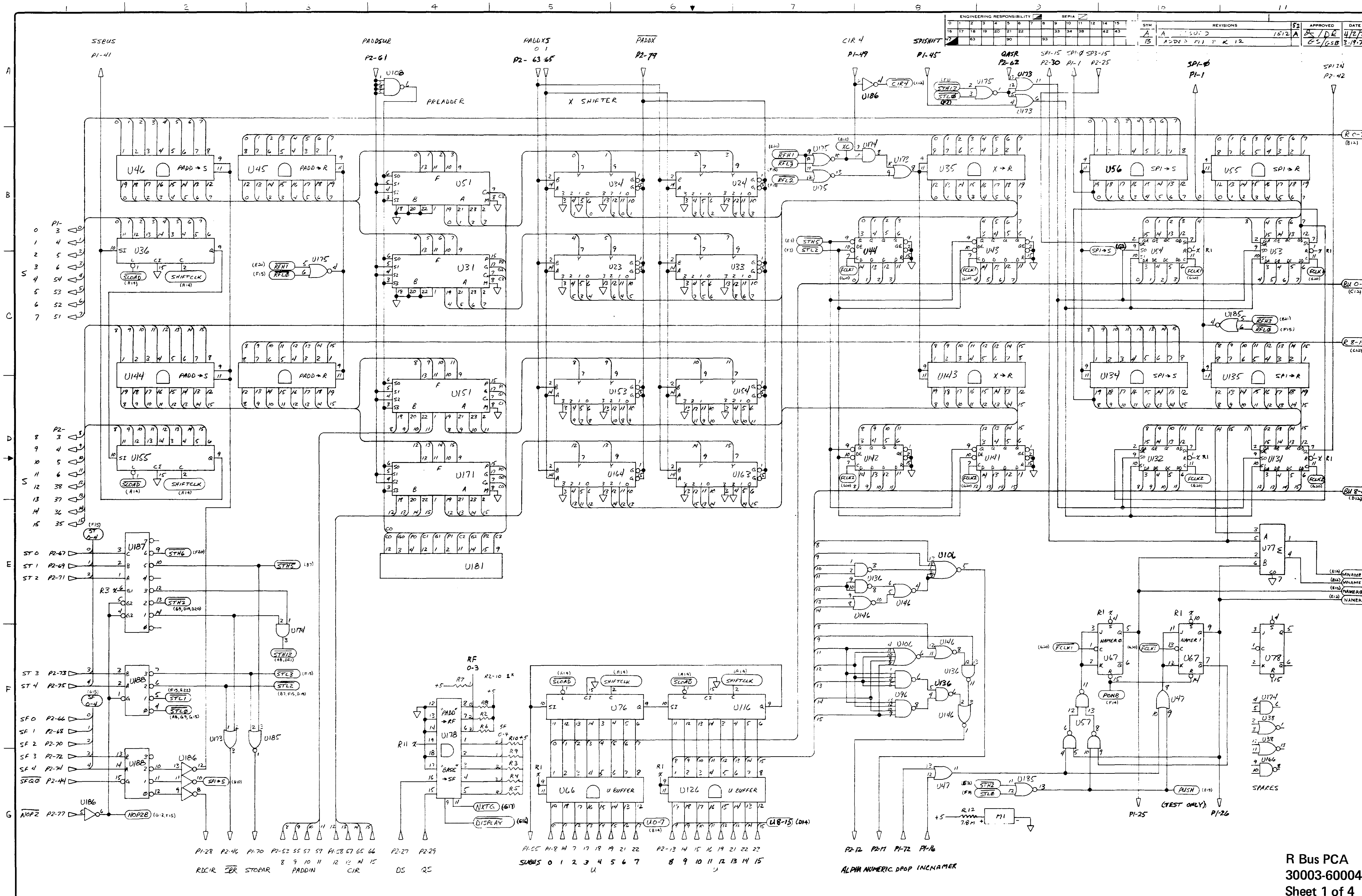
ALU PCA

30003-60003

IC Index

U	1820-	U	1820-	U	1820-
12	0535	74	1261	131	0683
15	0629	75	1304	132	0141
16	0683	76	0999	133	0998
17	0629	77	1304	134	0755
22	0629	81	0681	135	0681
24	0515	82	0691	136	0691
25	0681	83	0998	137	1304
26	1240	84	1261	141	0688
27	0683	85	1304	142	0681
31	0690	86	0999	143	1319
32	0515	87	1304	144	0755
34	0686	91	0686	151	1240
35	0681	92	0691	152	1322
36	1240	93	1275	153	0688
37	0629	94	0683	154	0691
41	0681	95	1305	155	0377
42	0839	97	0690	156	1158
43	1319	101	0685	157	0377
44	0686	102	0688	161	0683
45	0377	103	1275	162,163	1240
46	0688	104	1261	164	0681
47	0377	105	1304	165	0685
51	0681	106	0999	166	0693
52	0685	107	0690	171	0685
53	0998	111	0681	172,173	1240
54	0755	112	0397	174	0681
55,56	0691	113	0998	175	0691
61	0629	114	0691	176	0693
62	0683	115	1304	183	0685
63	0998	117	1042	184	0688
64	0755	121	0688	185	0691
65	1042	122	0397	186	0693
66	0282	123	0998		
67	1042	124	1261		
71	0688	125	1042		
72	1322	126	0999		
73	0998	127	1304		



R Bus PCA
30003-60004
Sheet 1 of 4

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS RELEASED	BEIDK	4/2/75

SRBUS P1-44 · SKIP P2-26 · SHIFTCLK P1-23 · SLOAD P1-13 · STTR P1-38 · TR0 P1-34 · TR1 P1-35 · TR2 P1-36 · TR3 P1-37

TR0 · TR1 · TR2 · TR3 · Z · PL · SPB

R 0-7 (B11) · BU 0-7 (C11) · R 8-15 (C11) · BU 8-15 (D11)

SHIFTCLK (D2,C2,F6,F7,D13,H13) · SLOAD (D2,F2,F5,F6,B12,D12)

U85 U75 U65 U95 U105 U115 U125 U135 U124 U114 U104 U94 U84 U74 U64 U123 U113 U103 U93 U83 U73 U63 U122 U112 U102 U92 U82 U72 U62 U121 U111 U101 U91 U81 U71 U61

ZERO, SR→R · UBUS→R · SI · L · CI · C · Q

U145 U146 U147 U156 U167 U165 U185 U118

RFMOP (G17) · ROMFCN (G17) · XC (G17) · CJRN (G18) · RFH3 (E23) · RFL3 (F15) · RFH2 (G23) · RFL2 (F15) · RFH0 (F23) · RFL0 (F13)

FCLK1 (G20) · FCLK2 (G20)

U87 U97 U107 U117 U127 U88 U98 U108 U78 U68 U48 U58 U38 U177 U167 U158 U147 U168 U148 U178 U168 U157 U147

MINAMER0 (E9) · MINAMER1 (E11) · NAMER0 (E9) · NAMER1 (E11)

SR0 · SR1 · SR2 · U174 · U147 · FCLK2

U176 U156 U167 U186 · RDMREG (G16) · RA-RB · PUSH (G18) · QUP (F19) · STMREG (F18) · STNG (E8)

U178 U168 U148 · DISPLAY (G5) · NXTG (G4)

U157 · RFH3 (C11,C14,D13) · RFH1 (C3,B7) · RFH0 (D13) · RFNOP (G17) · P2-58 RFSAME

1K R1 · 1K R11 · (5 VOLTS, TOTAL) · +5 (P1, P2) · 25 CM. 0.1uF CER · 9 CM. 1uF CER · 4 CM. 33uF TANT

P1-20,60 P2-20,60 · P1-2,39,40,80 P2-2,39,40,80

C1,2,5,6,9, 11-16,19-23, 26,28,30-36 · C4,7,8,10, 17,24,25, 27,29 · C3,18, 21,28

P1-27 IMCSR · P1-24 DECSR · P2-34 SR0 · P2-33 SR1 · P2-31 SR2 · P1-15 CLSR · P2-76 PONB · P1-31 QDWN · P2-24 ROMFCN1 · P2-28 JMPISB1 · P1-68 DISPLAY · P2-64 NXT+1 · P1-48 MEMREF · P1-67 NXTG · P1-32 33 6 1 TNAMER · P2-1 FCLK · P1-79 FCLK

P1-0 12 0 · P1-1 11 1 R · P1-2 9 2 · P1-3 10 3
P1-4 61 4 · P1-5 62 5 R · P1-6 63 6 · P1-7 64 7
P2-10 8 · P2-9 9 · P2-8 10 R · P2-7 11
P2-47 12 · P2-48 13 · P2-49 14 R · P2-51 15
P2-56 RF 0 · P2-54 RF 1 · P2-52 RF 2 · P2-50 RF 3

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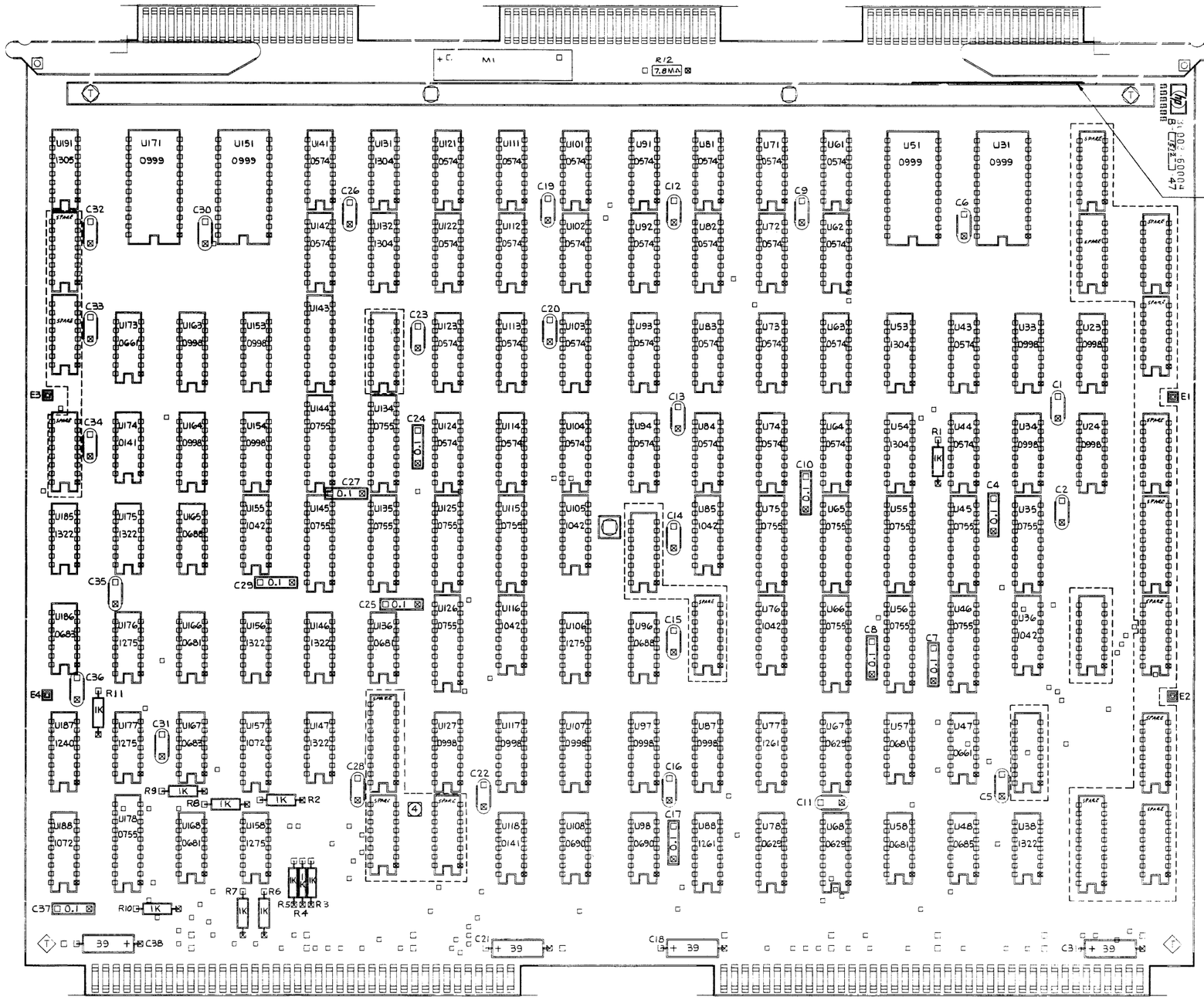
ENGINEERING RESPONSIBILITY	DEPT.

SYM	REVISIONS
A	1st ISSUE

F-30003-60004
APPROVED
25 Jan 83



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS IN OHMS.
   ALL RESISTORS 1/4W, 5%.
   ALL CAPACITANCE IN MICROFARADS.
   ALL CAPACITORS .01μF CERAMIC DISC.
   ALL IC'S ARE 1820-____.

R Bus PCA
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R BUS PCA

30003-60004

IC Index

U	1820-	U	1820-	U	1820-
23,24	0998	87	0998	146,147	1322
31	0999	88	1261	151	0999
33,34	0998	91-94	0574	153,154	0998
35	0755	96	0688	155	1042
36	1042	97	0998	156	1322
38	1322	98	0690	157	1072
43,44	0574	101-104	0574	158	1275
45,46	0755	105	1042	163-165	0998
47	0661	106	1275	166	0681
48	0685	107	0998	167	0683
51	0999	108	0690	168	0681
53,54	1304	111-114	0574	171	0999
55,56	0755	115	0755	173	0661
57,58	0681	116	1042	174	0141
61-64	0574	117	0998	175	1322
65,66	0755	118	0141	176,177	1275
67,68	0629	121-124	0574	178	0755
71-74	0574	125-126	0755	181	1305
75	0755	127	0998	185	1322
76	1042	131,132	1304	186	0683
77	1261	134,135	0755	187	1240
78	0629	136	0681	188	1072
81-84	0574	141,142	0574		
85	1042	144,145	0755		

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15	
16 17 18 19 20 21 22 33 34 38 42 43	
47 63 90 93	

SYM	REVISIONS	S2	S3	APPROVED	DATE
A	AS ISSUED 1512	A	A	BF / DR	4/8/75
B	ADD U171 + RLS			BF / GDB	3 16 76

A0 A1 A15

SYSPRTY MCUDPRTY

MCUD 0 1 2 3 4 5 6 7

MCUD 8 9 10 11 12 13 14 15

BCMP LDDCOR LDACOR

XSGN 14 15

CPUSEL

P2-29 30 34

P2-9 P1-75

P1-55 59 57 63 61 65 69 67

74 72 76 70 68 73 71 77

P2-63 P1-50 66

P2-11 10

P1-58

CPUSEL P1-24

SYSPIN P1-49

U171 U172 U172 U164 U191

U38 UBUS→S

U28 U→BU

U15 U17 U27 U16 U45 U25

U37 P→S

U47 U36

S 0-7

BU 0-7

S 8-15

BU 8-15

(G27) RDUBUS

(G27) RDP

U18 INH EVEN

U25 INH EVEN

U46 U26 A B Y

U138 UBUS→S

U128 U→BU

DCOR

U117 U127 U145 U125

ACOR

P

U137 P→S

U147 U136

U118 INH EVEN

U135 INH EVEN

U146 U126 A B Y

U158

ST 0 P2-67

ST 1 69

ST 2 71

ST 3 73

ST 4 75

NDP2 P2-76

STH3 (B26)

STH4 (B24)

STH5 (E18)

STL3 (B23)

STL2 (B22)

STL1 (B21)

STL0 (B20, E40)

U187 U188

STPCLK (E13)

STCTRL (E17)

STCTRH (F13)

STP (F11)

STSP3 (B-5)

P1-11 P1-16

STIDA STIOD

U181 U13 U14 U131 U132 U89 U129 U149 U130 U148 U182

SPARE GATES

P1-56

REVMCIP

P2-7 8

EH EIS

EH (E19)

EIS (E19)

S1 S2

SW MODULE INTER-
POS SIZE LEAVING
1 16K NONE
2 32K NONE
3 64K NONE
4 32K 2-WAY
5 (NOT USED)

P1-1

ATC 1

P1-10

ATC 2

U155 A>B A=B A<B

P1-29

ILL ADR

S3

SW MEM COMP
POS SIZE CODE
1 48K 0 0 1 0
2 64K 0 0 1 1
3 80K 0 1 0 0
4 96K 0 1 0 1
5 112K 0 1 1 0
6 128K 0 1 1 1
7 160K 1 0 0 1
8 192K 1 0 1 1
9 224K 1 1 0 1
0 256K 1 1 1 1

U186 STP (G4)

P1-62 SPBBANK

P2-25 INCP

+5 R5 7.8M M1

S Bus PCA
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Sheet 1 of 5

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	8-2-82	4-19-83

SP3-Ø (P2-54) SP3IN (P1-15) SP3SHIFT (P2-61) QASL (P2-64) SP1-Ø (P1-9) SP345 (P2-26) STSTATUS (P2-79)

STATUS 0 1 2 3 4 5 6 7 (P1- 41 42 43 44 45 46 47 48)

STATUS 8 9 10 11 12 13 14 15 (J3- 43 41 27 39 45 25 23 21)

RDIOA (P1-64) CTRM (P2-59)

PCLK SP3 STATUS MISC CTRH CTRL

S 0-7 (B23)

BU 0-7 (B23)

S 8-15 (D23)

BU 8-15 (E23)

U65 PCLK→S · U66 SP3→S · U48 STATUS→S · U131 RBR, ICA, CTRL, CC, NOP→S · U121 CTRH→S

U75 U55 U76 U56 U105 U85 U106 U86 U87 U77 U67 U57 U95 U96 U153 U143 U133 U123 U173 U183

U108 U98 U162 U161 U163 U152 U151 U142 U141 U181 U186

RDPCLK (G26) RDSP3 (G28) RDSTA (G28) RDIOA (G25) RDCTRL (G26) RDIOF (G29) RDCC (G29) STCTRL (G3) STCTRH (G3) STS (F4) STLD (G2) STARCLK (G2)

RSTI (G13) RST2 (G13) FCLK3 (G15) FCLK1 (D24) FCLK2 (B24) CLK (G15)

(C7, C8, C9, D8, D9, C10 C11, E10, E11, C15, C16, E15, E16, E17, E18, F10, F19, F20, F21, F22)

(C1-6, 8-14, 12-14, 19-21, 22, 24-27, 29, 31, 32-36, 40, 41, 42-48, 124.1 SEP, 147A) 4×.39μf AT P1, P2 DISTRIBUTE +5 1K R2 E1 – E4 TERMINALS

(C12, C13, E12, E13, F18, F19) (F20, F21, F21, F22) (C4, C5, C6, D5, D6, C12, C13, E13, E12, F12, F13, F11, F15)

P1-26 P1-27 P1-25 P2-78 RUNFF ICEFLK EMULATOR CPURST

P1-79 FCLK

P1-78 CLK

P1-20,60 P2-20,60 P1-2,39,40,80 P2-2,39,40,80

P2-65 REPN

P2-17 P1-28 INKT RERI

P2-53 55 58 57 62 15 16 17 19 19 RDRT

P2-42 NEXT

S Bus PCA
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Sheet 2 of 5

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	DE/DR	4/16/75

$\overline{STTR}$ P1-38 $\overline{TR\emptyset}$ P1-34 $\overline{TR1}$ P1-35 $\overline{TR2}$ P1-36 $\overline{TR3}$ P1-37

Q DB SM DL SP2 PB TRØ TR1 TR2 TR3

S 0-7 (B12) 4-7 — U111 U101 U91 U81 U71 U61 U51 U41 U31 U21 — P1- 3 0, 4 1, 5 2, 6 3 S

U112 U102 U92 U82 U72 U62 U52 U42 U32 U22 — P1- 54 4, 53 5, 52 6, 51 7 S

BU 0-7 (D12) 0-3 — (G14) FCLK1

S 8-15 (B12) 12-15 — U113 U103 U93 U83 U73 U63 U53 U43 U33 U23 — P2- 3 8, 4 9, 5 10, 6 11 S

U114 U104 U94 U84 U74 U64 U54 U44 U34 U24 — P2- 38 12, 37 13, 36 14, 35 15 S

BU 8-15 (D12) 8-11 — (G14) FCLK2

U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 U26 U27 U28 U29 U30 U31 U32 U33 U34 U35 U36 U37 U38 U39 U40 U41 U42 U43 U44 U45 U46 U47 U48 U49 U50 U51 U52 U53 U54 U55 U56 U57 U58 U59 U60 U61 U62 U63 U64 U65 U66 U67 U68 U69 U70 U71 U72 U73 U74 U75 U76 U77 U78 U79 U80 U81 U82 U83 U84 U85 U86 U87 U88 U89 U90 U91 U92 U93 U94 U95 U96 U97 U98 U99 U100 U101 U102 U103 U104 U105 U106 U107 U108 U109 U110 U111 U112 U113 U114 U115 U116

U168 — R2 X — U178

P1- 32 TNAME 0, 33 TNAME 1

P2: 66 68 70 72 74 — 0 1 2 3 4 — SF

P2-44 P2-43 46 45 50 — $\overline{SF\emptyset}$ RDCPX1 RDMOD RDCPX2 RDSWCH

RDIOA (C20) RDIOCK (C13) — P2-47 — RDIOD

RDCTRL (C20) RDCTRN (C21) RDWEUS (C1) — P2-28 — SFSAME

RDP (C10)

RDSTA (C17) RDSP2 (C15) RDCC (C18) — P2-49 — RDOPND

RDNOP (D19) — P1-31 — QUWN

S Bus PCA
30003-60005
Sheet 3 of 5

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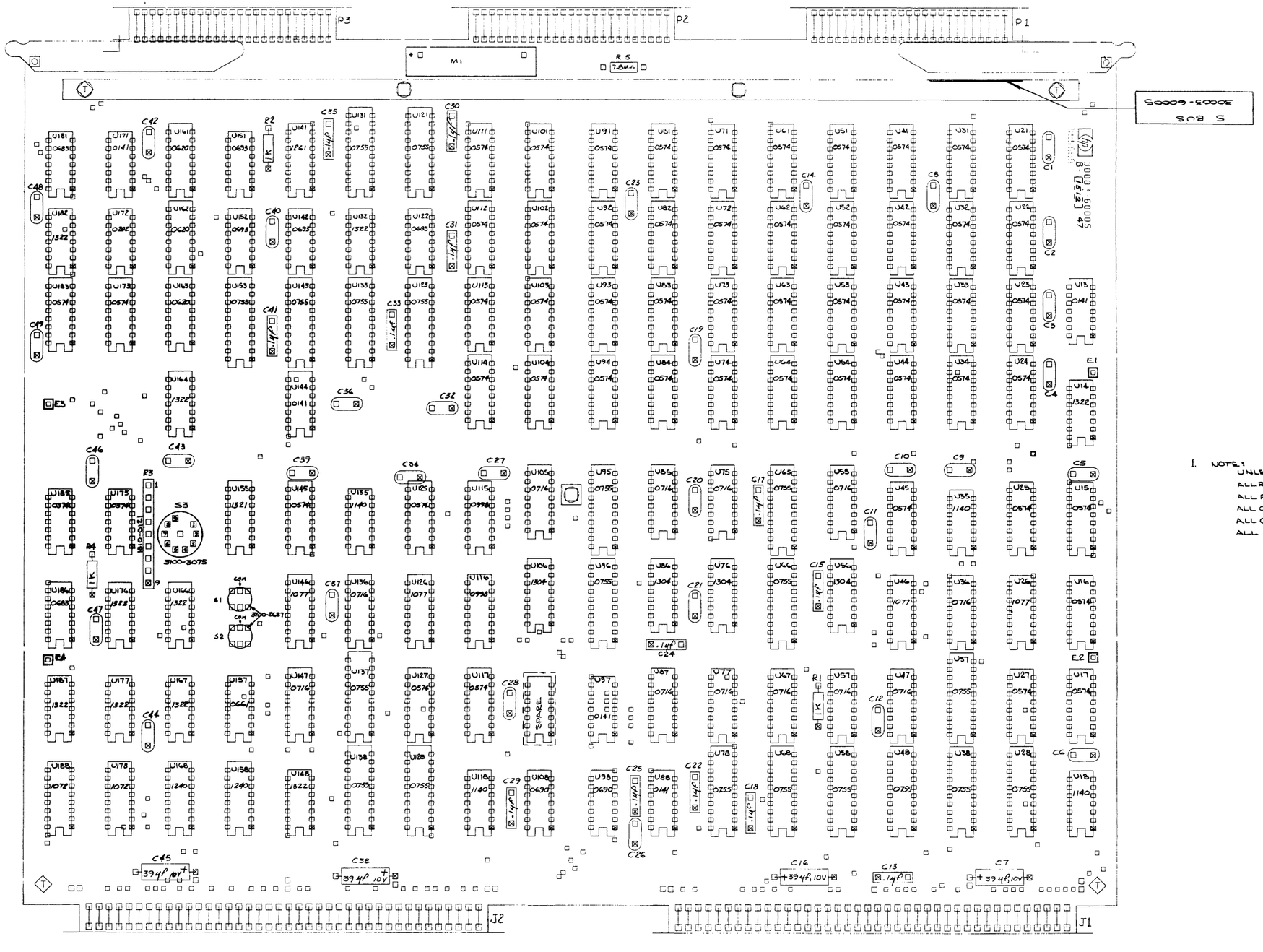


1. NOTE:
   UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS
   ALL RESISTORS ARE 1/8W 1%
   ALL CAPACITANCE IN MICRO FARADS
   ALL CAPACITORS ARE .01 μF CER. DISC. 0160-2055
   ALL IC'S ARE 1820-

S Bus PCA
30003-60005
Sheet 4 of 5

S BUS PCA

30003-60005

IC Index

U	1820-	U	1820-	U	1820-
13	0141	81-84	0574	141	1261
14	1322	85	0716	142	0693
15-17	0574	86	1304	143	0755
18	1140	87	0716	144	0141
21-25	0574	88	0141	145	0574
26	1077	91-94	0574	146	1077
27	0574	95,96	0755	147	0716
28	0755	97	0141	148	1322
31-34	0574	98	0690	151,152	0693
35	1140	101-104	0574	153	0755
36	0716	105	0716	155	1321
37,38	0755	106	1304	157	0661
41-45	0574	108	0690	158	1240
46	1077	111-114	0574	161-163	0620
47	0716	115,116	0998	164	1322
48	0755	117	0574	166,167	1322
51-54	0574	118	1140	168	1240
55	0716	121	0755	171	0141
56	1304	122	0685	172	0282
57	0716	123	0755	173	0574
58	0755	125	0574	175	0374
61-64	0574	126	1077	176,177	1322
65,66	0755	127	0574	178	1072
67	0716	128	0755	181	0683
68	0755	131	0755	182	1322
71-74	0574	132	1322	183	0574
75	0716	133	0755	185	0374
76	1304	135	1140	186	0683
77	0716	136	0716	187	1322
78	0755	137,138	0755	188	1072

ENGINEERING RESPONSIBILITY	SEPIA
U 1 12 8 14 15 16 9 17 18 10 11 19 / 16 17 18 19 20 21 22 33 34 38 42 43 / 47 63 90 93	

SYM	REVISIONS	52	APPROVED	DATE
A	AS ISSUED 1512	A	ES/DR	2.1.75
B	ADDED P31 R18		ES/DR	3.10.76

CIR PCA
30003-60006
Sheet 1 of 4

J1 - 1, 10, 19, 37, 41, 43, 45, 47, 49
J2 - 1, 10, 19, 22, 25, 28, 31, 34, 37, 41, 43, 45, 47, 49

SYSTEM SW REG — PANEL SW REG — RDOPND OPINP FIELD Φ RUNFF

RINSW DUMPSW LDSW LDREG LDADDR LDMEM DISPMEM SINGLE EXECUTE INCRADDR DECRADDR INHRMT SYSHLTFF RUNFF

PULLUPS 1K EA — RDCPX2 — INTHR SYSHFF RUNFF RUNSW DUMPSW LDSW — S (Φ-15) — CPURST'S IORSTSW

CIR → SBUS — SW → SBUS — PNLSW → SBUS — MCU CTRL/MXL — SHORT TRACE — FAST CPND — OPND

RDCIR P1-28 — PSRENB J2-23 — RDSWITCH P2-50

PULLUPS 1K, EACH, (1811) — GP. 0 1 2 3 4 5 6 COMM. — IN = ABSENT OUT = PRESENT — OP. PRESENT (E22)

0683-2715

CIR(0-15) (E3) — BMCU(0-15) (E2)

NIRTOCIR (G3) — BPENDING (G4) — JLUI PENDING (F8) — INTRPI (G21) — NEXT — JLUIM P2-54 — STA3 (D19) — INTRPI (F21)

STSTATUS P2-77 — STATUS3 P1-44

BMUXFF (G6) — XEQ (D20) — PAUSE (D21) — CMUXFF (E4)

P1-1 B MUX — P2-64 CMUX

Z (E7) — MR (F5) — MR (F4) — MR W (F7)

P2-25 DS — P2-26 QS — P2-61 PADDSDB — P2-63 PADDXSØ/Ø — P2-65 PADDXSØ1 — P2-53 PADDIN 8 — P2-55 9 — P2-57 10 — P2-59 11

P1-45 PAUSE — P2-79 PADDX

(E13,G13,C1, D11,E17) FCLK — (E2,F8,D16) CLK — (F2) CLK — (B2,E2,E7,G21) FCLK

P2-1 FCLK — P1-78 CLK — P1-42 CLK — P1-79 FCLK

RUN FF — SYS HLT — PWR INH

U1 — U0 — U2 — XEQ (F14) — NEXT (G11) — PAUSE (F14) — START (A7)

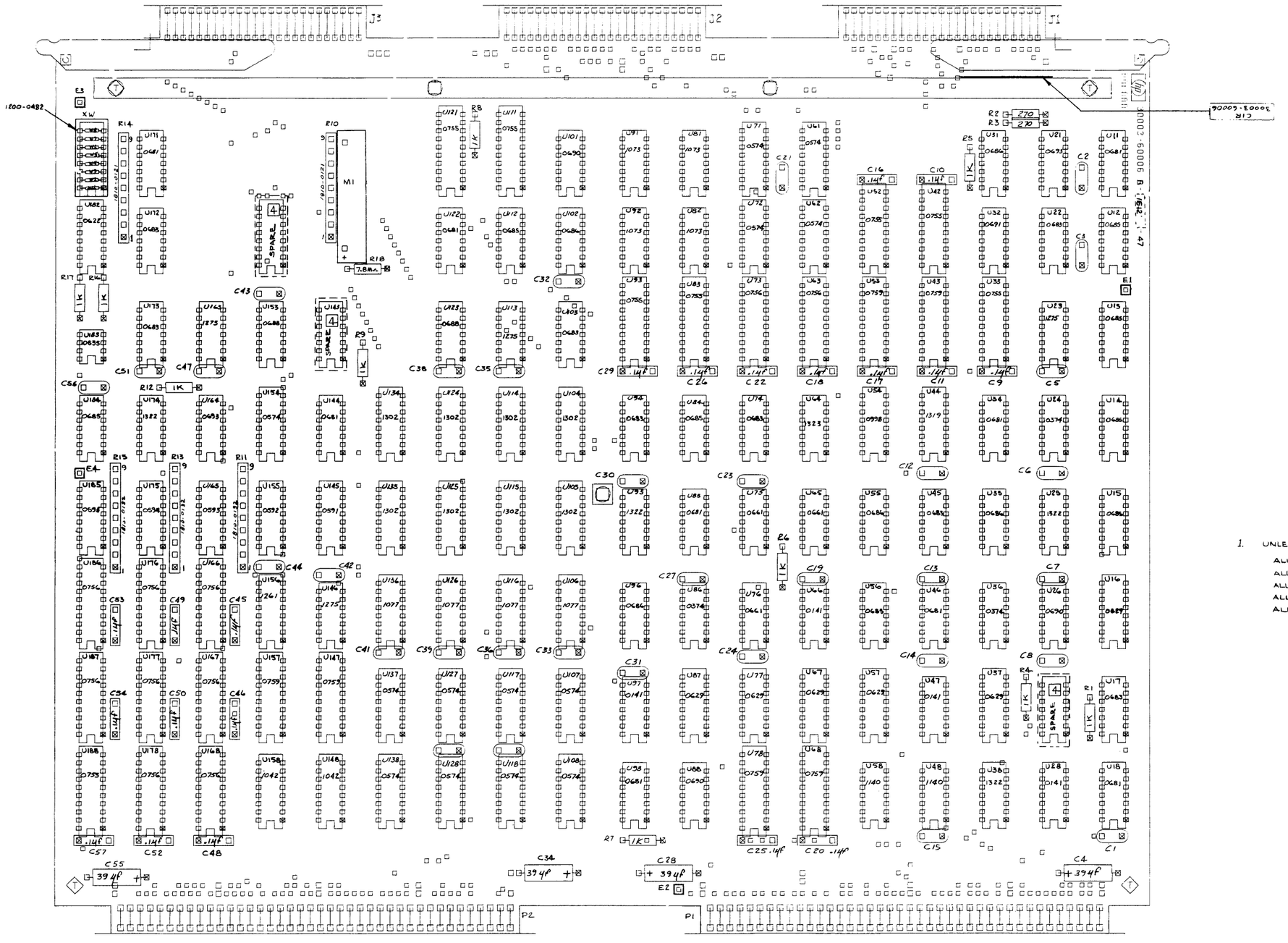
STA3 (H12) — PC 1 (E7) — PC Ø (E7)

FOR ALL SWITCH FUNCTIONS
SWITCH 00 NOP
UIS·CCPX 10 INTERRUPT
11 WAIT
SWITCH RELEASED 01
00 NOP

FOR LOAD, SINGLE, EXECUTE
SWITCH 00 NOP
NEXT 10 WAIT (GI INTRP)
HLT+NEXT 11 INTERRUPT
SWITCH RELEASED 01 WAIT
00 NOP

P2-67 NXT+1 — P2-43 RDCPXI — OP. PRESENT (D18) — P1-46 DISPFLG — P1-47 IOSFLG — P1-26 OVFLINT — P2-71 BNDV — P1-29 CPUTIMER — P1-10 EXTINT — P1-30 PWRFAIL — P1-25 MCUERR — P1-9 MODINT — P1-32 BPINT — P2-36 TINT — P2-58 INTRPI — P2-66 INTRP

CIR PCA
30003-60006
Sheet 2 of 4



1. UNLESS OTHERWISE NOTED;
   ALL RESISTANCE IN OHMS
   ALL RESISTORS ± 5% .25W
   ALL CAPACITANCE IN MICRO FARADS
   ALL CAPACITORS .01μF CER. DISC.
   ALL IC'S ARE 1820-

CIR PCA
30003-60006
Sheet 3 of 4

CIR PCA

30003-60006

IC Index

U	1820-	U	1820-	U	1820-
11	0681	63	0756	116	1077
12-15	0685	64	1323	117,118	0574
16	0629	65	0661	121	0755
17	0683	66	0141	122	0681
18	0681	67	0629	123	0688
21	0693	68	0759	124,125	1302
22	0683	71,72	0574	126	1077
23	1275	73	0756	127,128	0574
24	0374	74	0683	134,135	1302
25	1322	75,76	0661	136	1077
26	0690	77	0629	137,138	0574
28	0141	78	0759	144	0681
31	0686	81,82	1073	145	0591
32	0691	83	0755	146	1275
33	0755	84	0685	147	0759
34	0681	85	0681	148	1042
35	0686	86	0374	153	0688
36	0374	87	0629	154	0574
37	0629	88	0690	155	0592
38	1322	91,92	1073	156	1261
42	0755	93	0756	157	0759
43	0759	94	0683	158	1042
44	1319	95	1322	163	1275
45	0683	96	0686	164	0693
46	0681	97	0141	165	0593
47	0141	98	0681	166-168	0756
48	1140	101	0690	171	0681
52	0755	102	0686	172,173	0683
53	0759	103	0683	174	1322
54	0998	104,105	1302	175	0594
55	0686	106	1077	176-178	0756
56	0685	107,108	0574	182	0622
57	0629	111	0755	183	0535
58	1140	112	0685	184	0685
61	0574	113	1275	185	0594
62	0574	114,115	1302	186,187	0756
				188	0755

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	SZ	APPROVED	DATE
A	A & 16SUE > 1512	A	CS/DR	4/17/75
B	ADDED M1 & R19		DS /GSB	3.10.76

MCU PCA
30003-60007
Sheet 1 of 4

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	DR	4/17/78

S Φ 1 2 3 — P1- 3 4 5 6 — S2 (D11)

S4 5 6 7 — P1-54 53 52 51 — (B11) S4, (L10) S5, S7 (D11)

S8 9 10 11 12 13 14 15 — P2- 3 4 5 6 38 37 36 35

RDMOD P2-46

U34 (DQ, CLK, R, RST (C16), RMOPΦ (A6), RMOP1 (A6))

U24 (CLR (C21), RST (C16))

UM5

U178

RFRM 0 1 2

R5 4.7K +5 — R4 4.7K +5

CPU #1 — CPU #2

U133 U155 U153 U155

RDCPX1 (B11)

(C7) ME

(E10) LDMOD

CPUTIMER P1-30

EMULATOR P1-16

(C1) RRDYΦ, (C1) RRDY1, (C1) RRDY2, (C1) RRDY3 — U155 — IOLRDY (C1)

P2-42

MODINH P2-41

CPUINH P2-48

RB 4.7K +5

U113 — LSELINH (B5)

(D1) RDYΦ, (E1) RDY1, (E1) RDY2, (E1) RDY3 — U173, U183, U163, U143

U143 — HSELINH (B5)

(B2) ENB

U132

IOLREQ P2-68

(B3) IOLREQ

(C8) CPUHREQ

IOLR P2-70

(A3) IOHREQ

IOHREQ P2-57

IOHR P2-58

U182 (IOLREQ), U172 (IOHREQ), U162 (IOSEL), U152 (IOMSEL)

62-13

(C20) CLK1, (C21) CLK

(C19) IRST

IOHREQ (C1)

U142 — IOSEL (A3)

U152

U163 HOT 62-13 — IOIND U172 — (C9) IOINP

U113

P2-50 IOERR

P2-53 P2-54 P2-59 IOHSEL IOLSEL IOSEL

P2-56 IOINP — P2-74 IOTO1 — P2-72 IOTO2 — P2-51 P2-52 IOMOP φ 1

(TO BACKPLANE PINS, SHEET1)

TO 0 1 2 — FRM 0 1 2 — MOP 0 1 — TO/FRM/MOP (A7)

U186 — U181 — U185 ODD — U164

(A8) SYSPRTY

P1-17 IOSTROB

R12 270 +5 — U175, U176, U136

ME (C9)

RFRM02 (B3)

(D7) MEMWO-2

U113 — IORTN (D8)

U33

0160-2208 C24 330pf — 0683-3335 R7 33K +5

U102 — 3μSEC — 62-13

U54

P1-44 ENTIMER

P1-26 POLORSO

P1-22 IOPACT

62-14 IO TIMER

U105 — U83 — U73 — U55 — U43

RDCPX1 — FRZ (G10)

(C10) CLK1 — IRST (C19)

P1-29 IOTIMER

P1-41 SI

P1-70 ENABLE

(C10) SIOCMP — U92 — P1-27 SIOCMP

.01 mf 2'S'IC, per 4 non-'S' C1,5,7,10,11,13,15,17-20,22,23,27,28,30-35,40-42

1 per 106,107,540

C2,3,6,8,9,12,14,16,24,29,36-38

39 μf/10V

C4 C21 C25 C39

+5 P1,P2 20,60

P1,P2 2,39,40,80

X = 1K PULLUP TO +5 (UP TO 20 INPUTS PER 1K PULLUP)

PINS P1-75, P1-76 ARE RESERVED. DO NOT USE.

MCURST P2-1 — CPURST P2-78 — IORESET P2-79

(NEXT TO CPU# JMPR) WB

+5 — 62-13 1K — U81, U82, U72, U77 — R15

S04 62-12

RST (B8,B11) — RST1 (B4,C9,B6,C4,E9,F9,D3,D4,D5,P5) — RST2 (G1,F4,E8,E8,F8,F9,C8,B10,C10,D10,E10) — IRST (C10,F13,G13,F14,G14,G15,F19,F21)

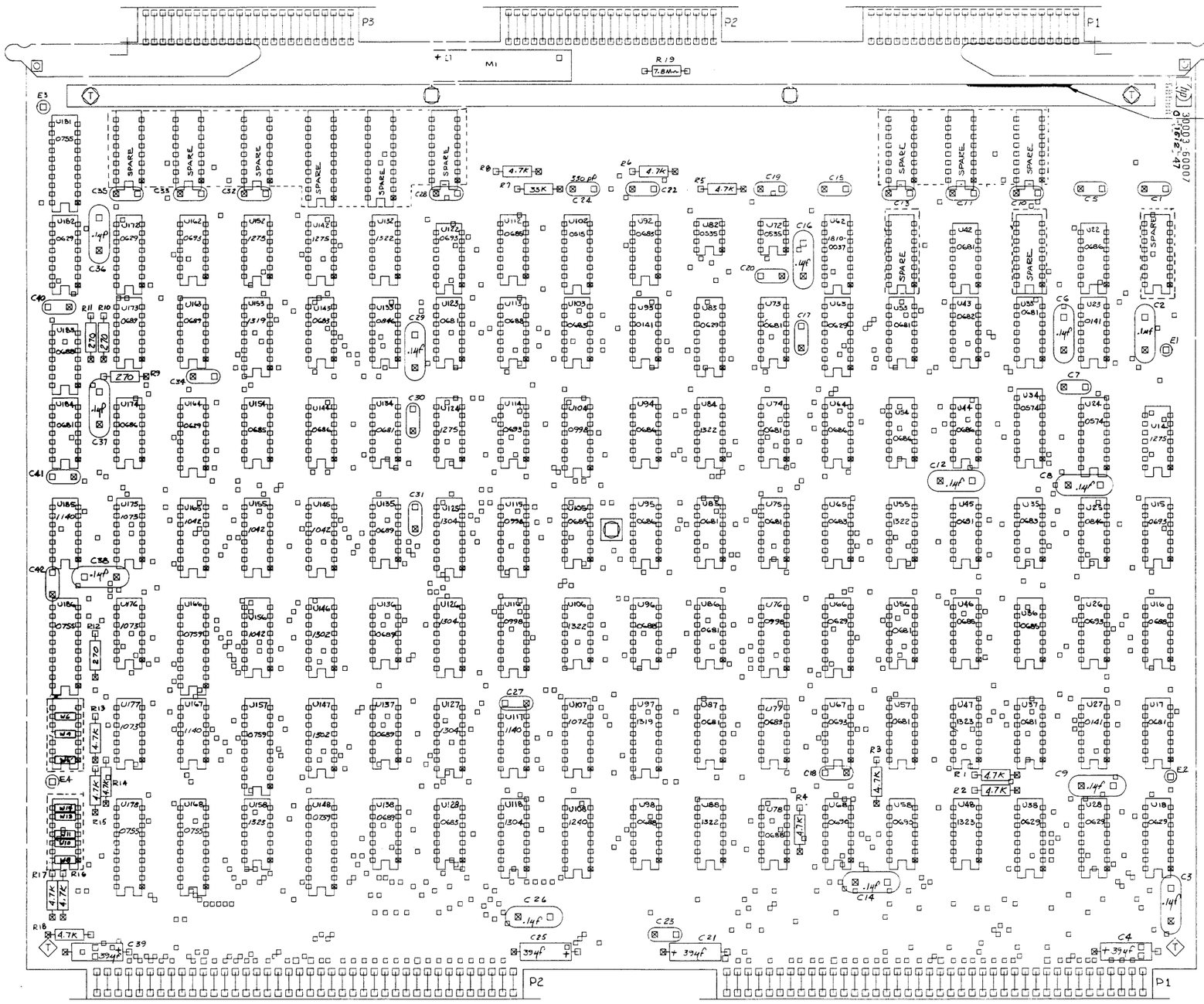
CLK P1-48 — CLK P1-78 — FCLK P1-79

R3 4.7K — R4 4.7K

U58 U68 U67 U87

CLK1 (B4,C9,E8,E8,G12,F12,G15,F20) — CLK2 (E8,E8,B10,B10,C10,D10,D10) — CLK (F4,B5,C5,C8,D9,D5,D5,F9,G14,F14,G14,B12,B13) — FCLK (G1,F7,D3)

MCU PCA
30003-60007
Sheet 2 of 4



1. NOTE :
   UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS .
   ALL RESISTORS ARE 1/4 W 5%
   ALL CAPACITANCE IN MICRO FARADS
   ALL CAPACITORS ARE .01. 0160-2055
   IC'S ARE 1820-

MCU PCA
30003-60007
Sheet 3 of 4

MCU PCA

30003-60007

IC Index

U	1820-	U	1820-	U	1820-
14	1275	67	0693	128	0683
15	0693	68	0690	132	1275
16	0688	72	0535	133	0846
17	0681	73-75	0681	134	0681
18	0629	76	0998	135-138	0689
22	0686	77	0683	142	1275
23	0141	78	0688	143	0683
24	0574	82	0535	144	0686
25	0846	84	1322	145	1042
26	0693	85-87	0681	146,147	1302
27	0141	88	1322	148	0759
28	0629	92	0685	152	1275
33	0681	93	0141	153	1319
34	0574	94,95	0686	154	0685
35	0683	96	0688	155,156	1042
36	0685	97	1319	157	0759
37	0681	98	0688	158	1323
38	0629	102	0515	162	0693
42	0681	103	0685	163	0689
43	0682	104	0998	164	0629
44	0686	105	0685	165	1042
45	0691	106	1322	166	0759
46	0685	107	1072	167	1140
47,48	1323	108	1240	168	0755
53	0681	112	0685	172	0629
54	0686	113	0688	173	0689
55	1322	114	0693	174	0686
56,57	0681	115,116	0998	175-177	1073
58	0690	117	1140	178	0755
62	1810-0037	118	1304	181	0755
63	1820-0629	122	0693	182	0629
64	0686	123	0681	183	0688
65	0683	124	1275	184	0681
66	0629	125-127	1304	185	1140
				186	0755

P1-25,27,38,45 AND P2-66 ARE RESERVED PINS

P1-56, 58 AND P2-73,75,76,77,78 ARE SPARES

ENGINEERING RESPONSIBILITY																SEAL
0	1	2	3	4	5	6	7	8	9	10	11	12	14	15	16	
17	18	19	20	21	22				33	34	38		42	43		
97		83			90			93								

SYM	REVISIONS	52	APPROVED	DATE
A	AS ISSUED 1312 A		CS/DR	7-20-75
B	ADDED MI & R16		83/658	2.23.76

IOP PCA
30003-60008
Sheet 1 of 4

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED .	DE/DE	3-20-75

MCODPRTY ← MCOD0-15 → IOHSEL

P1 75 | P1 55 59 57 63 61 65 69 67 — P1 74 72 76 70 68 73 71 77 — P1 P2 53

LOCATE MCODPRTY AND MCOD DRIVERS AND RECEIVERS NEAR P1 CONNECTOR - MINIMIZE NET SIZE.

(C12) SHIFTCLK
(C4) SLOAD
(E9) INCENB

SIOMAP P1 31 | IOSEL P2 54 | IOSTEP P1 44

(D22) IOTO1
(E24) IOTO2

STEPENB P1 32 (G5) SIOCMD (F4) POLLCMP (A6) OCTCMP

APE P2 7 | SYSPE P2 R

APEFF J3-2 | SYSPEFF J3-4 | ILGADDRFF J3-6

BMCOPRTY P1-66
SIOOR P1-30
SLOAD P1-13
SHIFTCLK P1-24

IOP DATA IN REG.

IOD INPUT REG.

(D11, A16, E18) SLOAD
(C14, A16, D18) SHIFTCLK

(D10) I.OMDATA
(F7) DRTS

(F8) LDIOBUF

IOP DATA OUT REG.

IOD DATA OUT REG.

IOINP P2-56

(E2) ENABLE
(C10) IOPGATE
(C5) SIOACT

IODPETY P2 9

IOD0-15 P2 31 32 33 34 41 42 43 44 — P2 45 46 47 59 61 62 63 64 — P2 67 69

IOX14 IOX15

(B10) DDGATE
(A8) STIOD

SA SB

STEPFRZ (C2)

ATC (B1)
IOERR (A8)
P2-55 IOSPE
IOLREQ (A8)

ERRCYC

SIODB
P1-49 SIODB
P1-50 SCMD
SCMD

IOTO1 (A16) → P2-74 IOTO1
IOTO2 (A16) → P2-72 IOTO2

MODULE CONFIGURATION
S1 IOTO1
S2 IOTO2
0 16K MODULES
8|5 32K MODULES
8|4 64K MODULES
8|5 32K-2WAY
1 16K MODULES
0 32K MODULES
8|5 64K MODULES
5 32K-2WAY

P2-47 RDIOD
LDIOA (G5)
P1-64 RDIOA

IOA

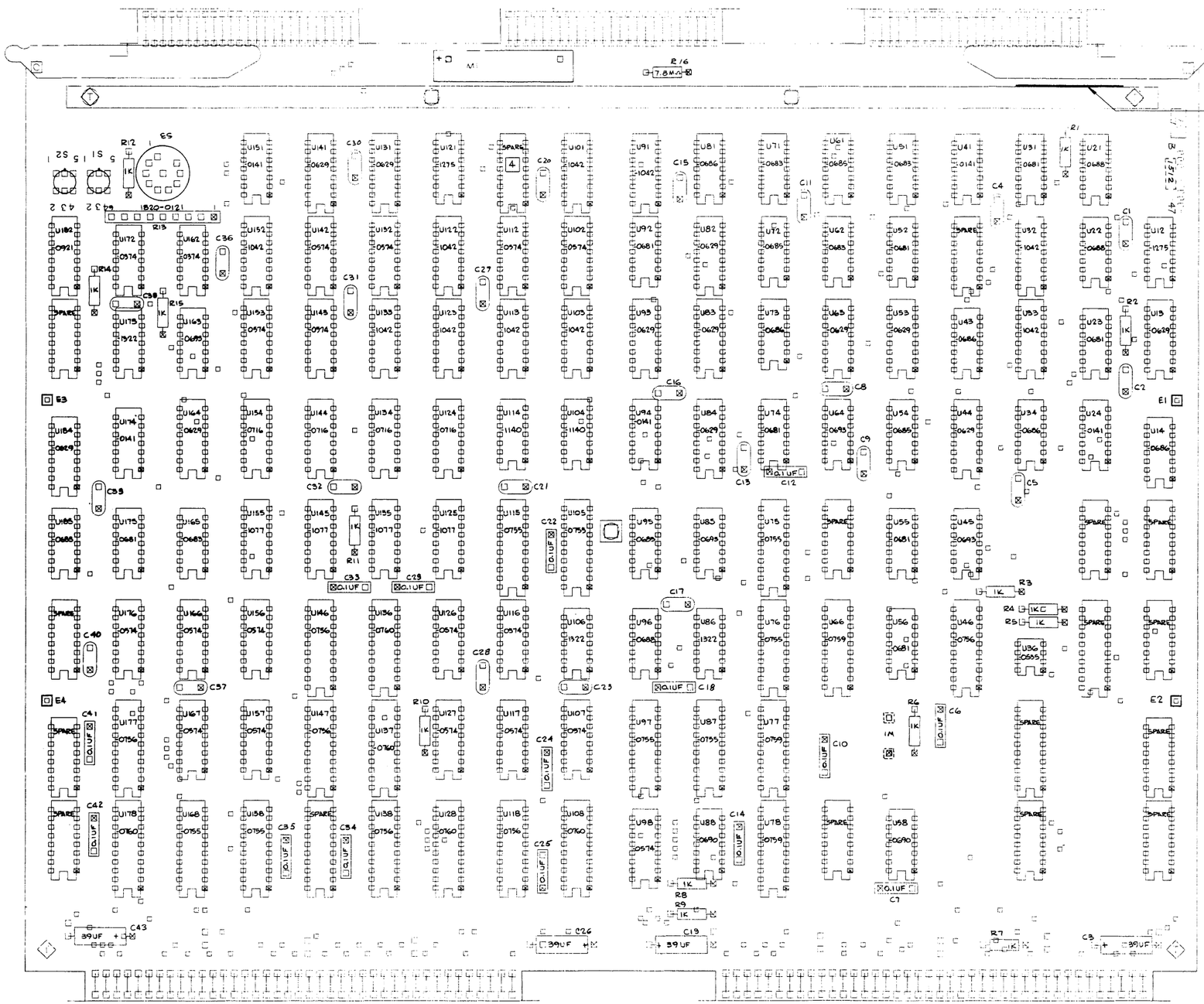
MEMORY SIZE S3
(0 ⇒ 256K)
PULLUP RESISTORS 1K EACH
+5

MASKRTN (C1)
ENABLE (E2)
DAGENB (E10)
NONZERO (J2)

IOCMD0 1 2
DEVNO 0 1 2 3 4 5 6 7

P1 P2 3 4 5 6 54 53 52 51 3 4 5 6 38 37 36 35 — S0-15
P1 P2 8 14 7 17 18 19 21 22 13 14 15 16 19 21 22 23 — U0-15

IOP PCA
30003-60008
Sheet 2 of 4



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS.
   ALL RESISTORS 1/4 W, 5%
   ALL CAPACITANCE IN MICROFARADS
   ALL CAPACITORS .01 UF CERAMIC DISC
   ALL IC'S ARE 1820-

IOP PCA
30003-60008
Sheet 3 of 4

IOP PCA

30003-60008

IC Index

U	1820-	U	1820-	U	1820-
12	1275	85	0693	132	0574
13	0629	86	1322	133	1042
14	0686	87	0755	134	0716
21,22	0688	88	0690	135	1077
23	0681	91	1042	136,137	0760
24	0141	92	0681	138	0756
31	0681	93	0629	141	0629
32,33	1042	94	0141	142,143	0574
34	0686	95	0685	144	0716
36	0535	96	0688	145	1077
41	0141	97	0755	146,147	0756
43	0686	98	0574	151	0141
44	0629	101	1042	152	0142
45	0693	102	0574	153	0574
46	0756	103	1042	154	0716
51	0683	104	1140	155	1077
52	0681	105	0755	156,157	0574
53	0629	106	1322	158	0755
54	0685	107	0574	162	0374
55,56	0681	108	0760	163	0693
58	0690	112	0574	164	0629
61,62	0685	113	1042	165	0683
63	0629	114	1140	166,167	0574
64	0693	115	0755	168	0755
66	0759	116,117	0574	172	0574
71	0683	118	0756	173	1322
72	0685	121	1275	174	0141
73	0686	122,123	1042	175	0681
74	0681	124	0716	176	0574
75,76	0755	125	1077	177	0756
77,78	0759	126,127	0574	178	0760
81	0686	128	0760	182	0921
82-84	0629	131	0629	184	0629
				185	0685

ENGINEERING RESPONSIBILITY															SEPIA
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22			33	34	38		42	43	
47		83			90			93							

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	CES/DK	4/11/75

CURRENT INSTRUCTION REGISTER

+5V

R6 1K

J1-

CIR Ø	20
CIR 1	21
CIR 2	22
CIR 3	23
CIR 4	24
CIR 5	25
CIR 6	26
CIR 7	27
CIR 8	29
CIR 9	30
CIR 10	31
CIR 11	32
CIR 12	33
CIR 13	34
CIR 14	35
CIR 15	36
SYSHAR	39
RUNFF	40

U4, U3

R3-1 133 Ø CR1 · R3-2 133 1 CR2 · R3-3 133 2 CR3 · R3-4 133 3 CR4 · R3-5 133 4 CR5 · R3-6 133 5 CR6 · R3-7 133 6 CR7 · R7-1 133 7 CR8 · R7-2 133 8 CR9 · R7-3 133 9 CR10 · R7-4 133 10 CR11 · R7-5 133 11 CR12 · R7-6 133 12 CR13 · R7-7 133 13 CR14 · R8-1 133 14 CR15 · R8-2 133 15 CR16

SYSTEM SWITCH REGISTER

+5V

R16-1 133 Ø CR19 · R15-2 133 1 CR20 · R15-3 133 2 CR21 · R15-4 133 3 CR22 · R15-5 133 4 CR23 · R15-6 133 5 CR24 · R15-7 133 6 CR25 · R16-3 133 7 CR26 · R16-2 133 8 CR27 · R16-1 133 9 CR28 · R16-4 133 10 CR29 · R16-5 133 11 CR30 · R16-6 133 12 CR31 · R16-7 133 13 CR32 · R8-5 133 14 CR33 · R8-6 133 15 CR34

PONB J1-28

S19 S20 S21 S22 S23 S24 S25 S26 S27 S28 S29 S30 S31 S32 S33 S34

U6 U7 U8 U9 (D/E, R/E)

S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13 S14 S15 S16

J1-

SW Ø	2
SW 1	3
SW 2	4
SW 3	5
SW 4	6
SW 5	7
SW 6	8
SW 7	9
SW 8	11
SW 9	12
SW 10	13
SW 11	14
SW 12	15
SW 13	16
SW 14	17
SW 15	18
INHAR	38
LDSW	44
DUMPSW	41
RUNSW	42
IORSTSW	J1-48
CPURSTSW	J1-50

R8-3 133Ω CR17 SYSTEM HALT · R8-4 133Ω CR18 RUN

U12

R16-4 4.7K · R9-2 4.7K

U11 U10

MSB XW2 XW1 LSB

R13 1K R12 1K R10 1K R11 1K

U5

R9-3 4.7K DIS ENAB

S38 3101-1213 PANEL

R22 470Ω R21 470Ω LOAD S35 C13 6.8 mf

R23 470Ω R24 470Ω RUN/HALT S36 C14 6.8 mf

R18 470Ω R17 470Ω DUMP S37 C11 6.8 mf

R20 470Ω R19 470Ω ENABLE S40 C12 6.8 mf

R1-2 1K · R1-3 1K · R1-1 1K

R4 27K C1 mf · R5 27K C2 mf · R2 1K

LOAD GS DUMP GS

R9-4 4.7K

S39 3101-1673 ZBO PRESET

R9-6 4.7K

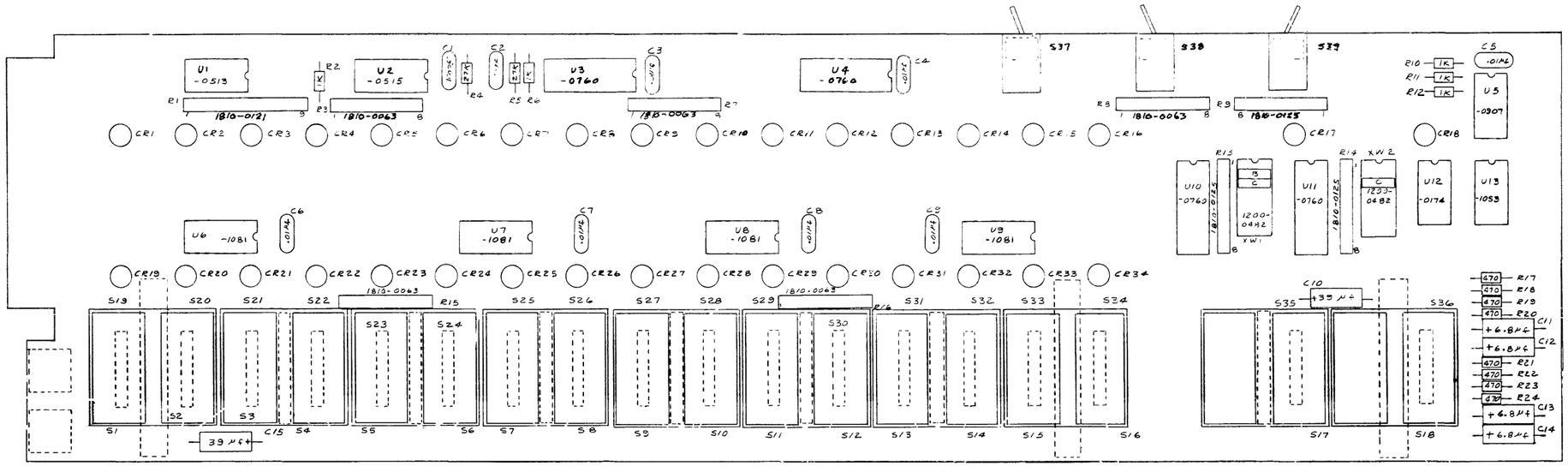
DISABLE ENABLE 3101-1213 S37 PF/ARS

J1- 6,10,19,37 41,43,45,47,49

+5V GROUND

C10,15 39 mf · C1-9 .01 mf

System Control Panel
30003-60011
Sheet 1 of 3



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS
   ALL RESISTORS 1/4W, 5%
   ALL DIODES 1990-0325

System Control Panel
30003-60011
Sheet 2 of 3

SYSTEM CONTROL PANEL

30003-60011

IC Index

U	1820-
1	0513
2	0515
3,4	0760
5	0907
6-9	1081
10,11	0760
12	0174
13	1053

30007B/8A/9A
ERROR CORRECTING MEMORY

MCL PCA	30007-60002	5 SHEETS
SMA PCA	30008-60002	3 SHEETS
FCA PCA	30009-60001	3 SHEETS
FLI PCA	30009-60002	3 SHEETS

ALL LEADS NOT INDICATED GO TO SHEET 52

SYM	REVISIONS	52	53	APPROVED	DATE
A	AS ISSUED 1616	A	A	DS/PC	11/4/77

ENGINEERING RESPONSIBILITY — SILPHA

P2-2 MCUD Ø0 A0
P2-3 MCUD Ø1 A1
P2-4 MCUD Ø2 A2
P2-5 MCUD Ø3 A3
P2-6 MCUD Ø4 A4
P2-7 MCUD Ø5 A5
P2-9 MCUD Ø6 A6
P2-10 MCUD Ø7 A7
P2-11 MCUD Ø8 A8
P2-12 MCUD Ø9 A9
P2-13 MCUD 10 A10
P2-15 MCUD 11 A11
P2 16 MCUD 12 A12
P2-17 MCUD 13 A13
P2-18 MCUD 14 A14
P2-19 MCUD 15 A15
P2-20 MCUD PRTY A16

U491 -1629 · U4101 -1624 · U142 -1624 · U1633 · U492 · U1633 · U1102

U114 0683

U51 1638 · U141 1638 ODD

U151 · U52 · U71 1395 ADR. REG. · 1395 U81 ADR. REG · 1395 U131

U61 1395 DATA REG. · U111 1395 · U121 1395

J3-32 MDO PRTY

1820-1639 · U1E07 · U2E13 · U3E23 · U4E63 · U5E15 · U6E25 · U7E11 · U8E21 · U9E16 · UAE26 · UBE32 · UCE22 · UDE34 · UEE24 · UFE14 · UGE30 · R11 1K

UHE00 · UJE20 · UKE10 · ULE4 · UME2 · UNE1 · 1742 1130

A16 T S

J1-36 CK A
J1-38 CK B
J1-40 CK C
J1-42 CK D
J1-44 CK D
J1-46 CK E
J1-48 CK E

U41 1113 CK REG

U31 1240 · U21 1240 · U32 1240 · U22 1240 ERR DECODER

P1-1,2,3,4 · P1-35,36 · +5V · +5VB

P3, J1, J2, J3 - ODD PINS
P2 - 1, 8, 14, 21, 30, 39, 46, 50
P1 - 10, 14, 15, 16, 19 20, 29, 30, 52, 56

R42 S1 · C57 S1 pf · R34 10K · R33 10K · 14.4K · U42Ø · U192 · C56 110pf · 34.8K R41

R31 1K · R22 46.4K · R23 3.16K · R26 10K · R25 10K · 34.8K · C55 910pf · C63 910pf · RT1 · C58 .22µf · 6.81K R29 · U183

R28 23.7K · C46 .047 µf · R32 26.1K · C45 .39µf · CR1 0033 · CR2 0033 · U162 · U172 · U182 · U192 · 1854-0019 Q1 · R21 178 · R27 100 · R20 178 · R19 100

U125 · U113 · U123 · U124 · U114 · RESET CIRCUIT

U161 1015 · U171 1015 · U181 1015 · U191 1015 · U201 1464 · U202 1464

U152 · U132 · U162 · R6 · R7 · R16 · R12 · R35 1K

TEST PT 1 J2-C
TEST PT 2 J2-B
MCU RESET P2-49
POWER ON P1-9
FOR SHEET 3 SEE SHT 2
MEM PROTECT
PF WARNING P1-5
MDO

MCL PCA
30007-60002
Sheet 1 of 5

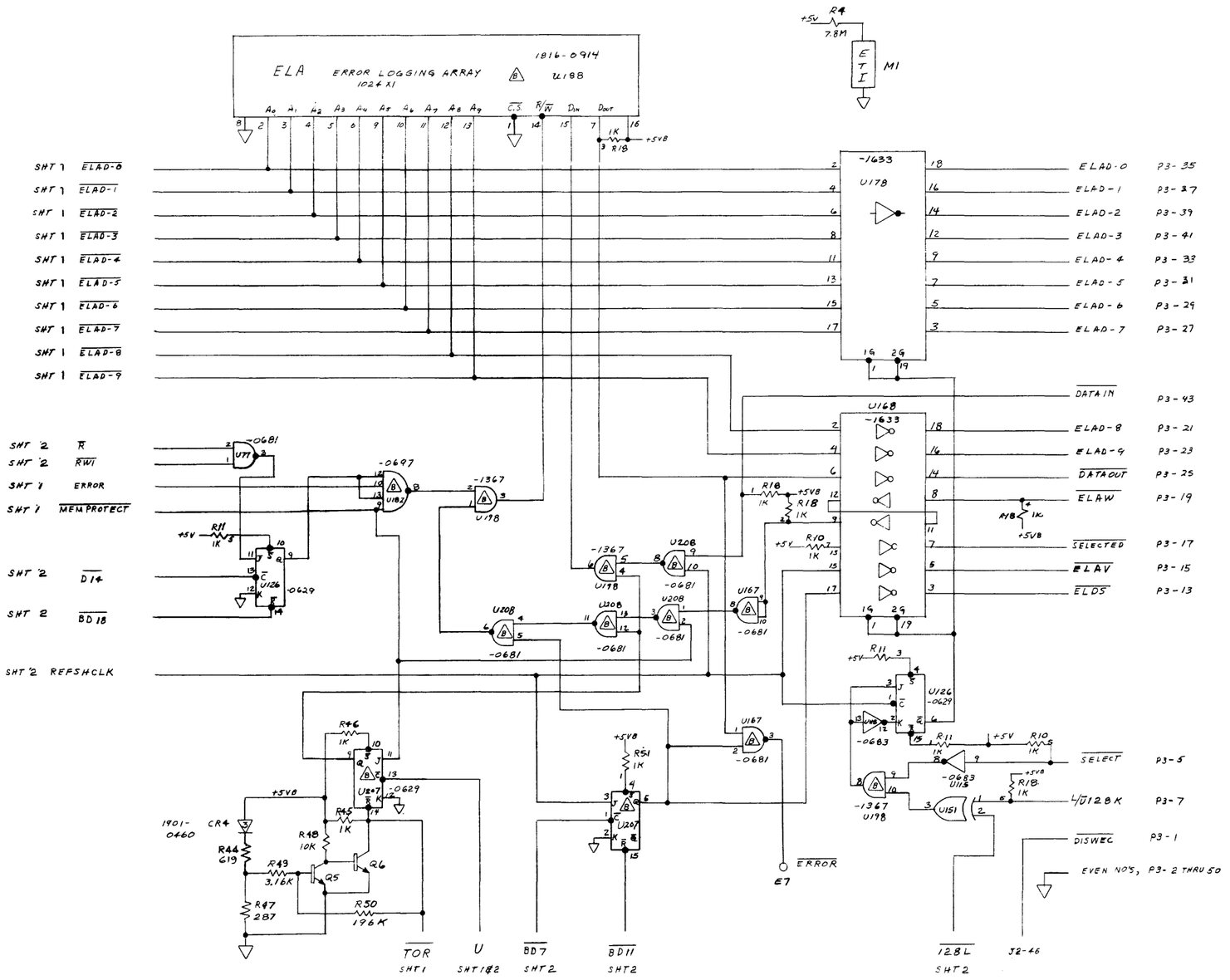
ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15 16 17 18 19 20 21 22 23 90 93	33 34 38 42 43

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED 1616	[illegible]	7/7/76

MCL PCA
30007-60002
Sheet 2 of 5

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15	
16 17 18 19 20 21 22 33 34 36 42 43	
47 63 90 93	

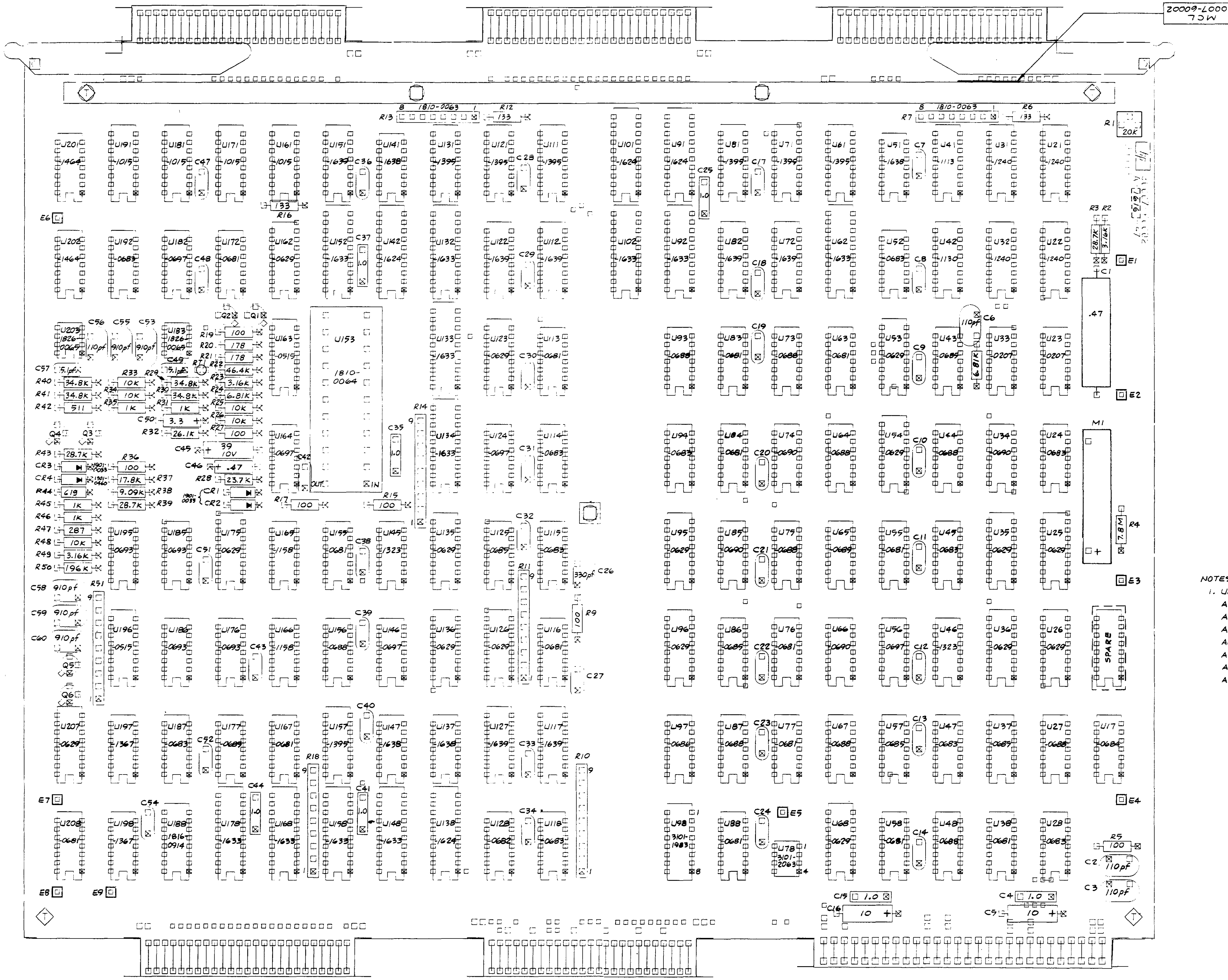
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED 1616	DS/PC	5/6/76



NOTES:
1. TRANSISTORS ARE 1854-0019
2. DISCRETE RES = 1/4 W M.F. 1%

MCL PCA
30007-60002
Sheet 3 of 5

A AS ISSUED



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS
   ALL RESISTORS 1/8W, 1%
   ALL CAPACITANCE IN MICROFARADS
   ALL CAPACITORS .01 µf CERAMIC DISC
   ALL TRANSISTORS 1854-0019
   ALL RESISTOR NETWORKS 1K, 1810-0121
   ALL IC'S ARE 1820-

MCL PCA
30007-60002
Sheet 4 of 5

MCL PCA

30007-60002

IC Index

U	1820-	U	1820-	U	1820-
17	0684	74	0690	148	1633
21,22	1240	75	0688	151	1639
23	0207	76,77	0681	152	1633
24	0683	81	1399	153	1810-0064
25,26	0629	83,84	0681	155	1820-0681
27	0688	85	0690	156	0688
28	0683	86	0685	157	1395
31,32	1240	87	0688	158	1633
33	0207	88	0681	161	1015
34	0690	91	1624	162	0629
35,36	0629	92	1633	163	0515
37	0689	93	0688	164	0697
38	0681	94	0683	165,166	1158
41	1113	95,96	0629	167	0681
42	1130	97	0686	168	1633
43	0689	111	1395	171	1015
44	0688	112	1639	172	0681
45	0683	113	0681	175	0629
46	1323	114,115	0683	176	0693
47	0683	116	0681	177	0689
48	0688	117	1639	178	1633
51	1638	118	0683	181	1015
52	0683	121	1395	182	0697
53	0629	122	1639	185,186	0693
54	0629	123	0629	187	0683
55	0681	124	0697	188	1816-0914
56	0697	125	0685	191	1820-1015
57	0685	126	0629	192	0683
58	0681	127	1639	195	0693
61	1395	128	0682	196	0515
62	1633	131	1395	197,198	1367
63	0681	132-134	1633	201,202	1464
64	0688	135,136	0629	207	0629
65	0689	137	1638	208	0681
66	0690	138	1638		
67	0688	141	1638		
68	0629	142	1624		
71	1399	145	1323		
72	1639	146	0697		
73	0688	147	1638		

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED (B1615)	BSTC	4.7.76

JUMPER TABLE

W	1	2	3	4	5	6
W/O ERROR CORRECTING						
LOWER 32K	X					X
UPPER 32K		X				X
WITH ERROR CORRECTING						
LOWER BANK-LOWER 32K	X	X			X	
LOWER BANK-UPPER 32K	X		X		X	
UPPER BANK-LOWER 32K	X			X	X	
UPPER BANK-UPPER 32K	X			X	X	

DATA OUT J1-2 J1-4 J1-6 J1-8 J1-10 J1-12 J1-14 J1-16 J3-16 J3-18 J3-20 J3-22 J3-24 J3-26 J3-28 J3-30 J3-32

U512 U515 U518

B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 PARITY

J2-4 DATA OUT ENABLE — U58 1322

J2-2 R/W CNTRL. TMG

J2-14 MEMORY PROTECT

U53 0760

R41 46.4 R42 46.4 R43 46.4 R44 46.4

R24 6.81K R25 6.81K R26 6.81K R27 6.81K +5 Vcc B

4 PLACES R = 147Ω 8 PLACES R = 1K C = 680 pf

U61 1240

J3-12 AD Ø3
J3-10 AD Ø2
J3-8 AD Ø1
J3-6 AR 1
J3-14 AR Ø

J2-50 CLK (READ)
J3-2 CLK (WRITE)
J2-16 REFRESH

U58 1322 U51 0685

J2-18 AD Ø4
J2-20 AD Ø5
J2-22 AD Ø6
J2-24 AD Ø7
J2-26 AD Ø8
J2-28 AD Ø9
J2-30 AD 10
J2-32 AD 11
J2-34 AD 12
J2-36 AD 13
J2-38 AD 14
J2-40 AD 15

J3-4 WRITE ENABLE

P1-35 NOTE 13
P1-36 NOTE 14
NOTE 15

J1 ODD PINS
J2 ODD PINS
J3 ODD PINS
P1-15
P1-16
P1-29
P1-30
P1-19
P1-20

DATA IN

U513 U516 U519 0760

J1-18 J1-20 J1-22 J1-24 J1-26 J1-28 J1-30 J1-32 J3-34 J3-36 J3-38 J3-40 J3-42 J3-44 J3-46 J3-48 J3-50

R16 6.81K R15 6.81K R14 6.81K R13 6.81K +5 Vcc B

46.4 R45 46.4 R46 46.4 R47 46.4 R48

-5V1 +12V

U56 U57 U54 U55 0736 0755

ALL PACKS S4-S7 ALL PACKS S0-S3

R22 2.2K R23 2.2K R20 2.2K R21 2.2K

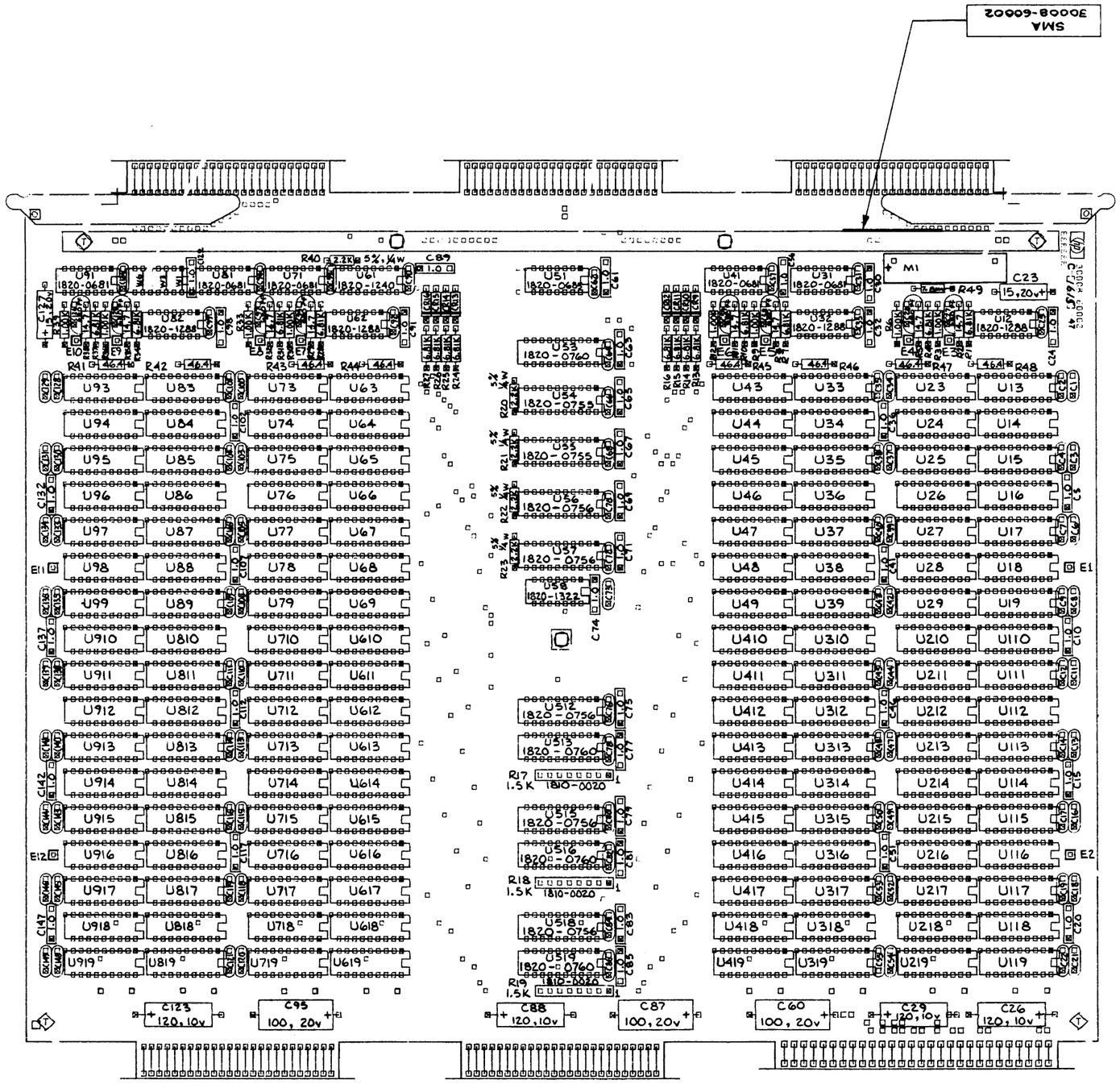
E10 E9 E8 E7 E6 E5 E4 E3

S0 S1 S2 S3 S4 S5 S6 S7

SMA PCA
30008-60002
Sheet 1 of 3

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]/RC	4.2.76



NOTES –

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE VALUES ARE IN OHMS ± 1%, AND ARE 1/8 W.
   ALL CAPACITANCE VALUES ARE IN MICROFARADS.
   ALL CAPACITORS ARE .01 μf CERAMIC DISC.
   ALL DIODES ARE 1910-0016.
   ALL I.C.'S ARE 5080-4560 (136 PLACES).

SMA PCA
30008-60002
Sheet 2 of 3

SMA PCA

30008-60002

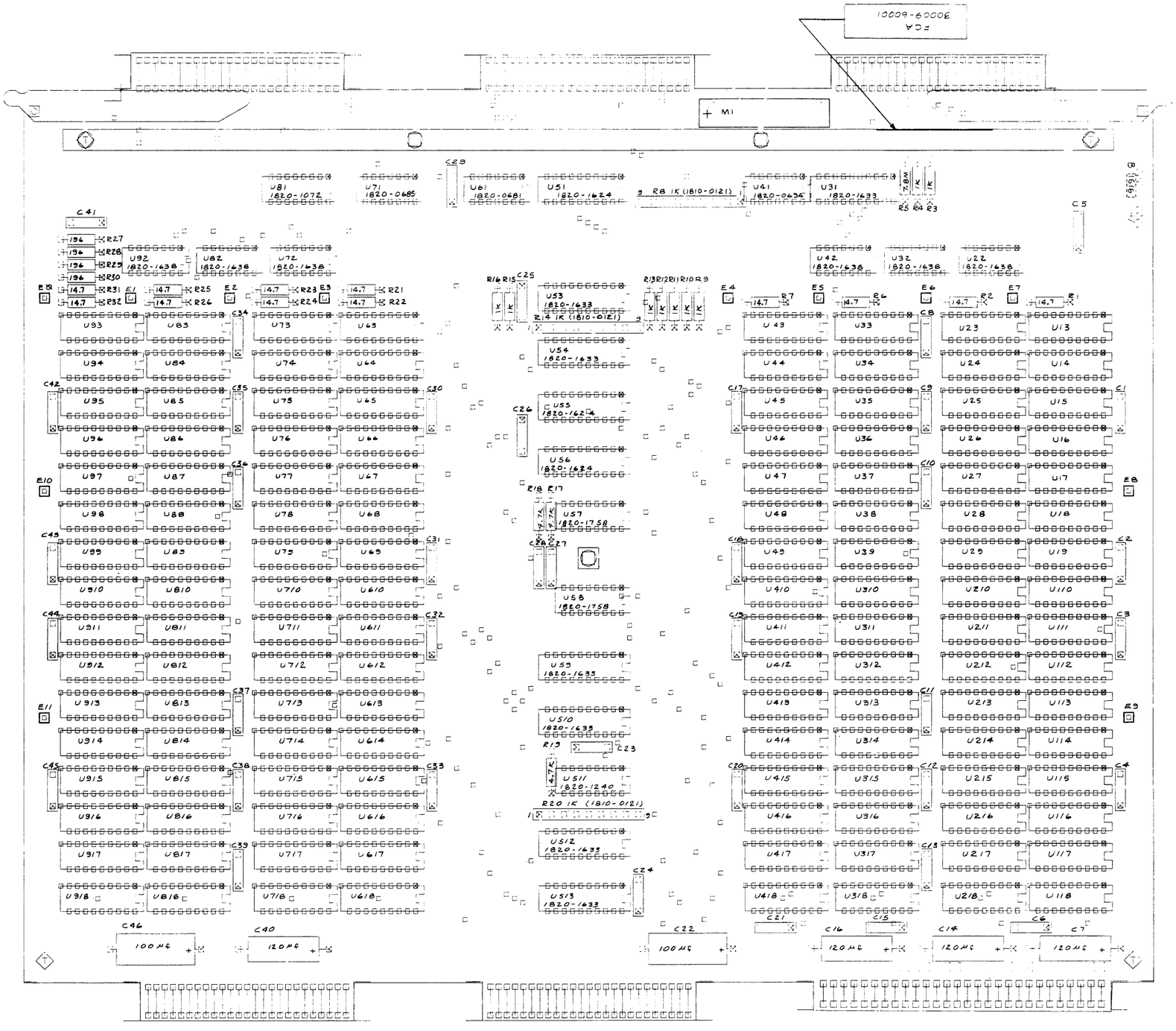
IC Index

U	18XX-	U	18XX-
12	1820-1288	513	1820-0760
13-19	5080-4560	515	0756
110-119	4560	516	0760
23-29	4560	518	0756
210-219	4560	519	0760
31	1820-0681	61	1240
32	1288	62	1288
33-39	5080-4560	63-69	5080-4560
310-319	4560	610-619	4560
41	1820-0681	71	1820-0681
43-49	5080-4560	73-79	5080-4560
410-419	4560	710-719	4560
51	1820-0689	81	1820-0681
53	0760	82	1288
54,55	0755	83-89	5080-4560
56,57	0756	810-819	4560
58	1322	91	1820-0681
512	0756	93-99	5080-4560
		910-919	4560

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15 16 17 18 19 20 21 22 33 34 38 42 43 47 53 90 93	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED 1616	05/11	816176

FCA PCA
30009-60001
Sheet 1 of 3



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE IN OHMS
   ALL RESISTORS 1/8W ±5%
   ALL CAPACITANCE IN MICROFARADS
   ALL CAPACITORS MF CERAMIC DISC
   ALL IC'S ARE 5080-4560 (128 PLACES

FCA PCA
30009-60001
Sheet 2 of 3

FCA PCA

30009-60001

IC Index

U	18xx-	U	18xx-
13-19	5080-4560	510	1820-1633
110-118	-4560	511	-1240
22	1820-1638	512,513	-1633
23-29	5080-4560	61	-0681
210-218	-4560	63-69	5080-4560
31	1820-1633	610-618	-4560
32	-1638	71	1820-0685
33-39	5080-4560	72	-1638
310-318	-4560	73-79	5080-4560
41	1820-0694	710-718	-4560
43-49	5080-4560	81	1820-1072
410-418	-4560	82	-1638
51	1820-1624	83-89	5080-4560
53,54	-1633	810-818	-4560
55,56	-1624	92	1820-1638
57,58	-1758	93-99	5080-4560
59	-1633	910-918	-4560

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 7 8 9 10 11 12 14 15 / 16 17 18 19 20 21 22 33 34 38 42 43 / 83 90 93	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED 1616		4-28-76

P2-23 ELAD-9
P2-21 ELAD-8
P2-27 ELAD-7
P2-29 ELAD-6
P2-31 ELAD-5
P2-33 ELAD-4
P2-41 ELAD-3
P2-39 ELAD-2
P2-37 ELAD-1
P2-35 ELAD-0
P2-25 $\overline{DOUT}$
P2-17 SELECTED
P2-15 $\overline{ELAV}$
P2-13 $\overline{ELDS}$
P2-1 $\overline{DISWEC}$
P2-7 LG128K
P2-43 $\overline{DIN}$
P2-19 $\overline{ELAW}$
P2-5 $\overline{SELECT}$

-1624 U87
-1293 U97 ADDRESS COMPARE
U77 -1633
U155 I/O LOGGING ARRAY 1024X1 73415 1816-0914
U156 -0716
U166 -0716
U165 -0716
U157 -0760
U137 -0760
U167 -0756
U147 -0756
U146 -1077
U126 -0683
U127 -0760
U117 -1293
U107 DEV. # SWITCH
U46 -1240 CMD DECODER
U47 -0760
U57 -0761
U37 -1367
U27 -0688
U36 -0681
U35 -0683
U45 -1367
U106 -0686
U145 -0686
U75 -0681
U76 -0683
U65 -0685
U66 -0688
U95 -0693
U96 -0693
U125 -0693
U135 -0693
U56 -0693
U136 -0693
U109 -0515
U128K
U97 -0697
U67 -0697
U57 -0761
U45 -1367
U126 -0683
U27 -0688
U37 -1367
U35 -0683
U36 -0681
U46 -1240
U47 -0760
U57 -0761
U37 -1367
U35 -0683
U36 -0681
U127 -0760
U117 -1293
U107

R13 +5V 1K
R6-6 +5V 1K
R6-1 10K
R6-5 +5V 1K
R6-8 +5V 1K
R8 +5V 1K
R10 +5V 1K
R12 1K +5V
R11 8X1K
R9 100K
R1 1K
R2 100
R3 196
R4 100
R5 196
C1A 1000 PF
C1B .01
C2 47PF-0761
C1,4,8, 20,30,31 .01uf
C3,5,6,9-11,12,13, 19-17,21,22,24,26,28 .01uf
C7,14,23 29,27 .01uf
T1 .0uf .01uf
M1 ELAPSED TIME INDICATOR
R7 7.8M 1%
300045
T10-1
245

P1 - 15,16,19,20,29,30
P2 - EVEN NOS 2 THRU 50
P3 - 3,7,10,13,16,19,22,25,28, 31,34,37,40,43,46,49
J2 - 1,3,5,45,47,49

P3 -42 -41 -39 -38 -36 -35 -33 -32 DATA -30 -29 -27 -26 -24 -23 -21 P3-20

$\overline{ST}$ P1-49
CR P1-50

CMD IN OUT
2 P3-5
1 P3-6
0 P3-4
CR P1-54
$\overline{SO}$ P1-53
IO RESET P1-11
$\overline{CLK}$ P1-13
CR P1-14

$\overline{DEV\ ADR}$
7 P3-18
6 P3-17
5 P3-15
4 P3-14
3 P3-12
2 P3-11
1 P3-9
0 P3-8

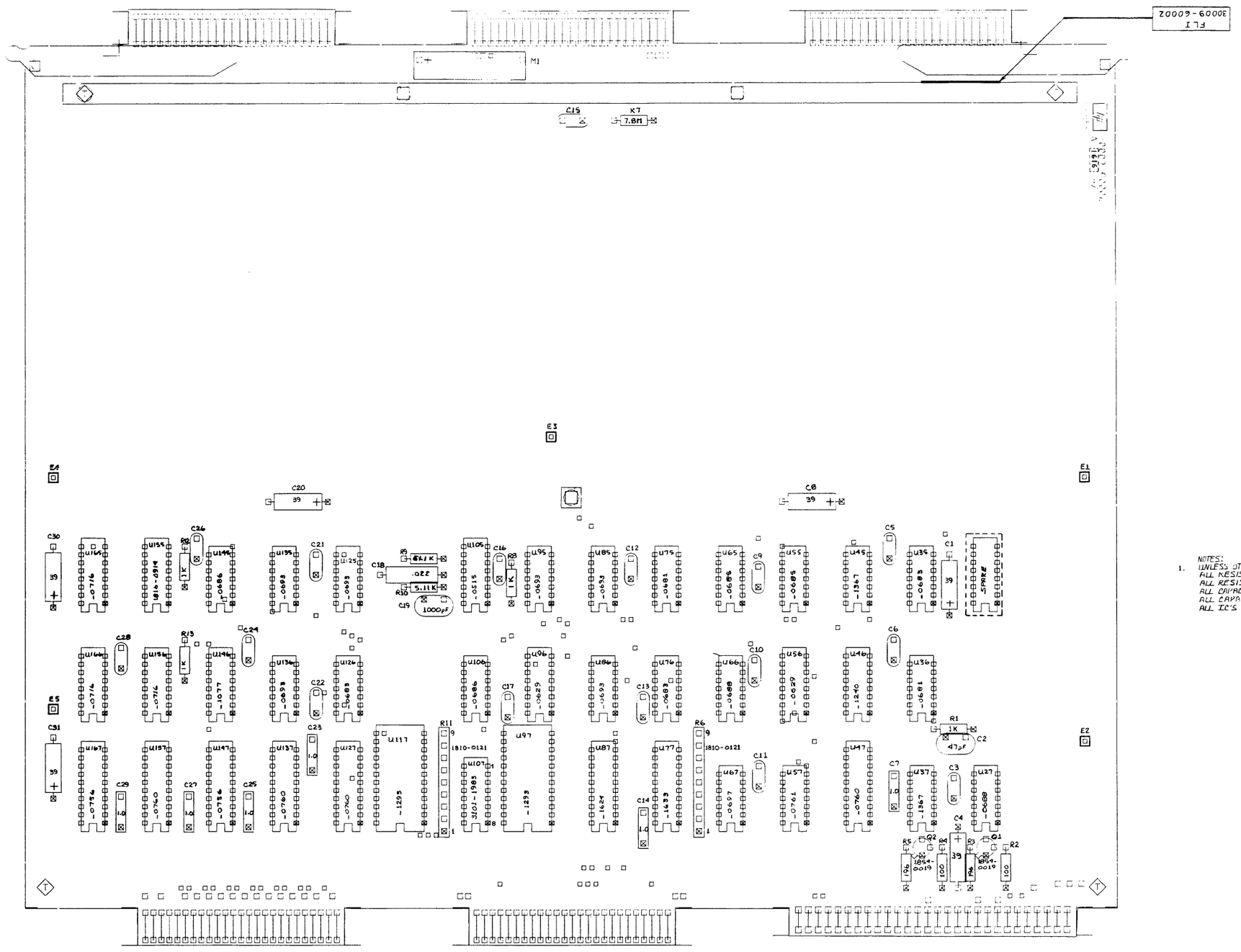
INT POLL IN P1-48
CR P1-47
INT POLL OUT P1-44
CR P1-43

P1-10 $\overline{PFW}$ P1-5 PON P1-9

READ COPY ERROR
READ SCAN
LOAD BLOCK
WRITE SINGLE
WRITE DATA
WRITE COPY
R/W COPY
DIS WEC
CLK
FOR 2060:55
J2-46

FLI PCA
30009-60002
Sheet 1 of 3

A AS ISSUED



1. NOTES:
   UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS
   ALL RESISTORS 1/4 W 1%
   ALL CAPACITANCE IN MICROFARADS
   ALL CAPACITORS .01 UF CER. DISC.
   ALL IC'S 1820-XXXX

FLI PCA
30009-60002
Sheet 2 of 3

FLI PCA

30009-60002

IC Index

U	1820-	U	1820-	U	1820-
27	0688	66	0688	106	0686
35	0683	67	0697	117	1293
36	0681	75	0681	125	0693
37	1367	76	0683	126	0683
45	1367	77	1633	127	0760
46	1240	85,86	0693	135,136	0693
47	0760	87	1624	137	0760
55	0685	95	0693	145	0686
56	0629	96	0629	147	0756
57	0761	97	1293	155	1816-0914
65	0685	105	0515	156	1820-0716
				157	0760
				165,166	0716
				167	0756

30012A
EXTENDED INSTRUCTION SET

EIS PCA 30012-60001 3 SHEETS

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	A3 ISSUED A 7607	ES/BB	2-11-76

CONNECTIONS TYP (96 PLCS)

330 +5 R1

U193 ENB1

U192 U158 ENB2

U194 U195

U187 2K

U197 1K /XW

U196

U198

ROM SELECTOR

P2-6 ROMENB 0 1 2 3 4 5 6 7

P2-29 30 31 32 33 34 41 42 8 9 10 11 12 13 14 15

SPARE U196

U2 ADDRESS 8 7 6 5 4 3 2 1 0 OUTPUT

U11 U21 U31 U41 U51 U61 U71 U81 U91 U101 U111 U121 U131 U141 U151 U161

U12 U22 U32 U42 U52 U62 U72 U82 U92 U102 U112 U122 U132 U142 U152 U162

U13 U23 U33 U43 U53 U63 U73 U83 U93 U103 U113 U123 U133 U143 U153 U163

U14 U24 U34 U44 U54 U64 U74 U84 U94 U104 U114 U124 U134 U144 U154 U164

U15 U25 U35 U45 U55 U65 U75 U85 U95 U105 U115 U125 U135 U145 U155 U165

U16 U26 U36 U46 U56 U66 U76 U86 U96 U106 U116 U126 U136 U146 U156 U166

U141 %17777 ↑ %11000 U131 %10777 ↑ %10000 U161 %10777 ↑ %10400 U151 %10377 ↑ %10000

U142 %13777 ↑ %13000 U132 %12777 ↑ %12000 U162 %11777 ↑ %11400 U152 %11377 ↑ %11000

U143 %15777 ↑ %15000 U133 %14777 ↑ %14000 U163 %12777 ↑ %12400 U153 %12377 ↑ %12000

U144 %17777 ↑ %17000 U134 %16777 ↑ %16000 U164 %13777 ↑ %13400 U154 %13377 ↑ %13000

U145 %21777 ↑ %21000 U135 %20777 ↑ %20000 U165 %14777 ↑ %14400 U155 %14377 ↑ %14000

U146 %23777 ↑ %23000 U136 %22777 ↑ %22000 U166 %15777 ↑ %15400 U156 %15377 ↑ %15000

ADDRESSES USING 2K PROMS

ADDRESSES USING 1K PROMS

ENB1 ENB2

U47 U67 U87 U107 U127 U147 U167

P1- 4 3 21 24 0 1 2 3 ROM

P1- 23 25 27 26 4 5 6 7

P1- 28 31 32 33 8 9 10 11

P1- 35 39 36 38 12 13 14 15

P1- 41 42 43 44 16 17 18 19

P1- 45 47 48 20 21 22 23

P1- 51 52 53 54 24 25 26 27

P1- 55 57 59 71 28 29 30 31

+5 1K R2 P1- 5,6,15,18,22,29,49,50, 55,56,57,72,73,79,75,76

+5 1K R3 P2- 3,5,22,23,24,53,55,57, 58,61,62,63,64,65,77

C1-3,6-8,10-12,14-16 19-21,23-25,27-29, 32,33

+5 C5C/C8 C31/C33

23 x .01μf ARRAY

12 x .1μf AT SNOS, 5241's

4 x 39μf AT P1,P2

E1 — E4

C4,9,13,17,22, 26,30,34-38

P1-19,20,59,60

P2-19,20,59,60

P1-1,2,39,40,80

P2-1,2,39,40,79,80

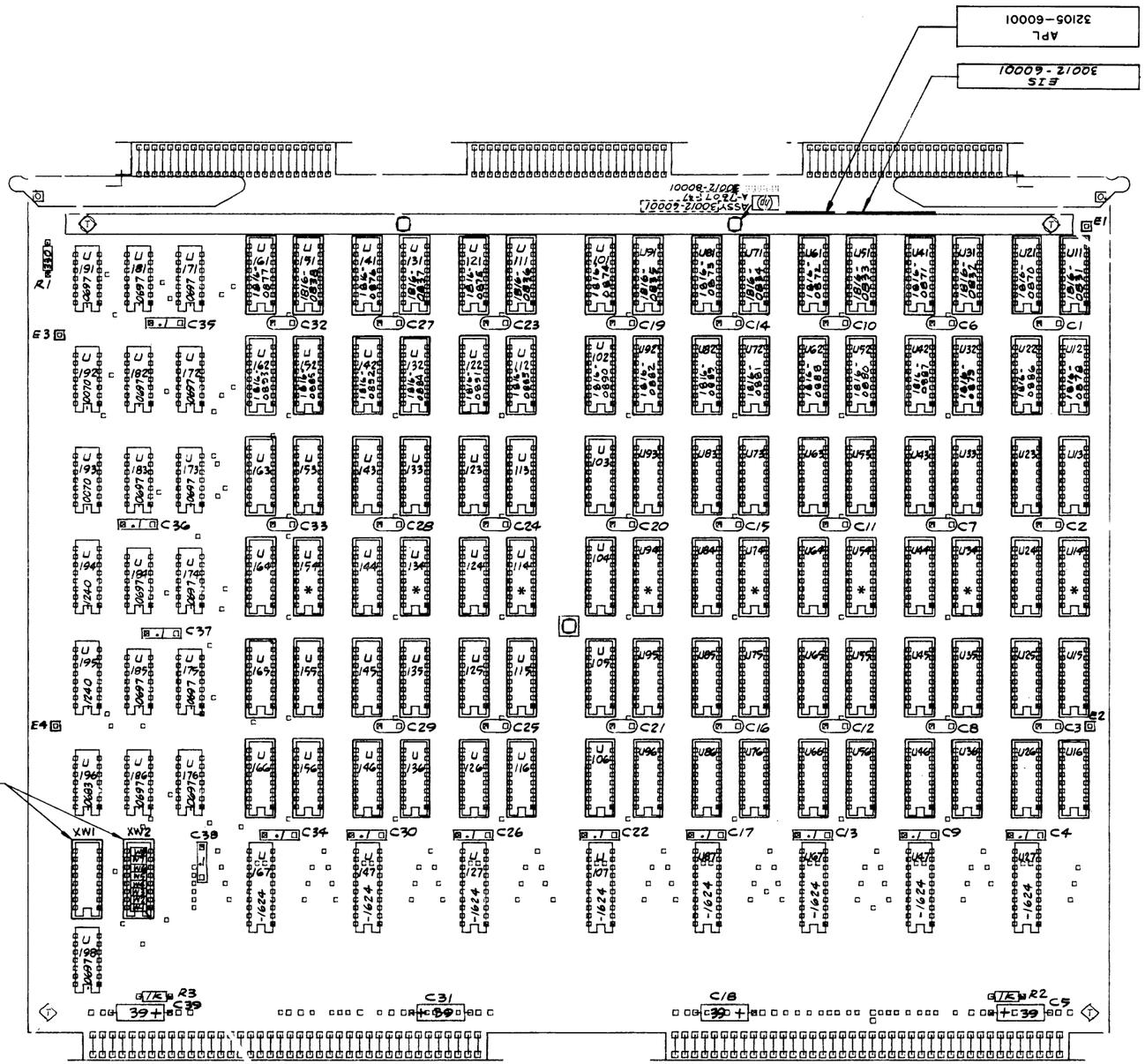
P1-13,70

P2-25,36,37,38

EIS PCA
30012-60001
Sheet 1 of 3

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS
   ALL CAPACITANCE IN MICROFARADS
   ALL CAPACITORS .01 CERAMIC DISC
   ALL IC'S ARE 1820

* THESE ITEMS ADDED TO THE PCA WHEN APL IS INSTALLED. REFER TO IC INDEX FOR IC PART NUMBERS.

EIS PCA
30012-60001
Sheet 2 of 3

EIS PCA

30012-60001

IC Index

U	1820-	U	1820-	U	1820-
11	1816-0831	81	1816-0873	147	1816-1624
12	0878	82	0889	151	0838
21	0870	87	1820-1624	152	0885
22	0866	91	1816-0835	161	0877
27	1820-1624	92	0882	162	0893
31	1816-0832	101	0874	167	1820-1624
32	0879	102	0890	171-176	1820-0697
41	0871	107	1820-1624	181-186	0697
42	0887	111	0836	191	0697
47	1820-1624	112	0883	192,193	0070
51	1816-0833	121	0875	194,195	1240
52	0880	122	0891	196	0683
61	0872	127	1624	198	0697
62	0888	131	1816-0837		
67	1820-1624	132	0884		
71	1816-0834	141	0876		
72	0881	142	0892		

The following IC's are present if the PCA has APL capability.

U14	1816-0976
U34	1816-0977
U54	1816-0978
U74	1816-0979
U94	1816-0980
U114	1816-0981
U134	1816-0982
U154	1816-0983