OPERATING AND SERVICE MANUAL

12610B

DRUM MEMORY INTERFACE KIT

Note

This manual should be retained with Volume Three
of the HP Computer System Documentation.

12610-9001

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides installation, operating, programming, and service information for the Hewlett-Packard (HP) 12610B Drum Memory Interface Kit.

1-3. DESCRIPTION.

1-4. GENERAL.

1-5. The equipment portion of the kit furnishes the control circuits and cable for connecting an HP 2773A, 2774A, or 2775A Drum Memory to an HP 2114B, 2115A, 2116A, or 2116B Computer. The control circuits are on two plug-in cards which install in the computer card cage. The cable supplied with the kit connects the cards to the drum memory.

1-6. The cards must not be installed in the HP 2150A or 2150B Input/Output and Memory Extender, or in the 2151A Input/Output Extender. These extender units do not have the direct memory access facility necessary for operation of the drum system.

1-7. INTERFACE KIT CONTENTS.

1-8. The drum memory interface kit consists of the following:

   a. Data channel interface card (part no. 12610-6001).

   b. Command channel interface card (part no. 12610-6002).

   c. Interface cable, 10 feet (part no. 12610-6004).

   d. Drum diagnostic tape (part no. 20340C).

NOTE

The part number of the program tape includes a suffix letter which identifies a particular revision of the tape. The first issue of a tape is identified by the letter A. Subsequent revisions are identified in alphabetical sequence as B, C, D, etc. If revision of a tape requires changes to associated documentation, an updating supplement for the documentation is supplied when the new tape is furnished. Always use the latest revision of a program tape, even if different from that specified in this manual, together with all updating documentation.

   e. Operating and service manual with supplement covering diagnostic program procedures (part no. 12610-9001).

1-9. IDENTIFICATION.

1-10. Hewlett-Packard uses five digits and a letter (00000A) to identify standard interface kits. If the designation of the kit received does not agree with the designation on the title page of this manual, there are differences between the kit received and the kit described in this manual. These differences are explained in change sheets and manual supplements available at HP Sales and Service Offices. (Addresses of these offices are listed at the back of this manual.)

1-11. In addition to a part number, each plug-in printed-circuit card is identified by a letter, a date code, and a division code (e.g. A-921-22). These are marked on the card beneath the part number. The letter identifies the version of the etched circuit on the card. The date code (three digits) refers to the electrical characteristics of the board with components mounted. The division code (two digits) identifies the Hewlett-Packard division which manufactured the card. If the date code on a printed-circuit card does not agree with the date code shown on the corresponding logic diagram in this manual, the card differs from the one described in this manual. These differences are explained in change sheets or a manual supplement available at HP Sales and Service Offices.

1-12. The interface cable is identified by its part number, marked on one of the plugs attached to the cable.

1-13. The diagnostic program tape is identified by name and part number, marked on a label affixed to the beginning of the tape.

1-14. The manual and manual supplement are identified by title, part number, and publication date, marked on the title page of the document. The supplement is bound to the back of the manual.

1-15. ADDITIONAL ITEMS REQUIRED.

1-16. EQUIPMENT.

1-17. In addition to the computer, drum memory, and drum memory power supply, use of the drum memory interface kit requires that the computer include the direct memory access (DMA) option. This option consists of the HP 12578A or 12578A-001 Accessory Kit (for the HP 2115A, 2116A, or 2116B Computers), or the HP 12607A Accessory Kit (for the HP 2114B Computer).

1-18.   Use of the drum diagnostic tape requires that the computer system include a paper-tape reader and a teleprinter.

1-19.   DOCUMENTS.

1-20.   In addition to the manual and manual supplement supplied with the drum memory interface kit, the following documents furnish information pertinent to the use of the interface kit:

a.   Operating and service manual for the HP 2773A, 2774A, or 2775A Drum Memory (part no. 2773-90003, 2774-90001, and 2775-90001, respectively).

b.   Operating and service manual for the direct memory access system. The part number of the manual is as follows:

(1) Part no. 12578-9001 for the 12578A and 12578A-001 Direct Memory Access Kit (used with the 2115A, 2116A, or 2116B Computer).

(2) Part no. 12607-90002 for the 12607A Direct Memory Access Kit (used with 2114B Computer).

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2.   This section provides information for unpacking, initial inspection, installation, and checkout of the drum memory interface kit. The computer, drum memory, drum memory power supply, and other required equipment, should be installed and prepared for operation before installing the interface kit.

2-3. UNPACKING AND INITIAL INSPECTION.

2-4.   If the drum memory interface kit is received separated from the computer, inspect the carton containing the kit before opening. If there is external evidence of damage, or if the box rattles, request that the carrier's agent be present when the carton is opened.

2-5.   Inspect each component of the kit as the parts are unpacked. Look for such evidence of damage as cracks, dents, broken components, detached parts, corrosion, water damage, etc. If any part of the kit is damaged, retain the carton, packing material, and shipping papers, and immediately notify the carrier and the nearest Hewlett-Packard Sales and Service Office. The Sales and Service Office will arrange for repair or replacement of damaged parts without waiting for settlement of claims against the carrier.

2-6.   After inspecting all components, refer to paragraph 1-7 of this manual and ensure that the kit is complete. Also check the part numbers given in paragraph 1-7 against the part numbers on the kit components. If the kit is incomplete, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

2-7. PREPARATION FOR INSTALLATION.

2-8. COMPUTATION OF CURRENT REQUIREMENTS.

2-9.   The cards in the interface kit obtain their operating voltages from the computer power supply. Before installing the cards, it is necessary to determine whether they will impose an excessive added load on the power supply. Together, these cards require 2.40 amperes from the +4.5 volt source, and 0.24 amperes from the -2 volt source. If these amounts will overload the computer power supply, an HP 2160A Power Supply Extender must be used.

2-10.   The drum memory has its own power supply, which furnishes all ac and dc operating voltages required by the drum memory.

2-11. PROTECTION OF TRACKS.

2-12.   A track protect switch on the data channel interface card permits a read-only status to be selected for some or all drum tracks. This protect feature is in effect when the switch is in the up position. As shipped from the factory, the card can protect track 0000 only. By removing diodes from the card before it is installed in the computer, additional groups of tracks can be protected when the switch is in the up position.

2-13.   If protection is not desired for any track, no removal of diodes is required. The track protect switch is simply set to the down position when the computer is in operation. Similarly, if only track 0000 is to be protected, no diodes are removed, and the track protect switch is set to the up position when track protection is desired.

2-14.   When more than one track is to be protected, diodes are removed from the data channel interface card in accordance with table 2-1. If the drum has fewer than 1400 (octal) tracks, the table applies to the extent of the number of tracks on the drum.

Table 2-1. Track Protect Diodes

TRACKS PROTECTED WITH TRACK PROTECT SWITCH UP (OCTAL TRACK ADDRESS)	DIODES REMOVED	QUANTITY OF PROTECTED TRACKS (DECIMAL)
0000	None	1
0000 and 0001	CR1	2
0000 thru 0003	CR1,2	4
0000 thru 0007	CR1,2,3	8
0000 thru 0017	CR1,2,3,4	16
0000 thru 0037	CR1,2,3,4,5	32
0000 thru 0077	CR1,2,3,4, 5,6	64
0000 thru 0177	CR1,2,3,4,5, 6,7	128
0000 thru 0377	CR1,2,3,4,5, 6,7,8	256
0000 thru 0777	CR1,2,3,4,5, 6,7,8,9	512
0000 thru 1377	CR1,2,3,4,5, 6,7,8,9,10	768

2-15.   The locations of track protect diodes are shown in figure 5-2. Diodes which have been removed can later be replaced to reduce the number of tracks protected. When removing or replacing diodes, observe the normal precautions for avoiding damage to components and circuit cards.

2-16.   INSTALLATION.

2-17.   Installation of the drum memory interface kit is performed as follows:

a.   Set the AC POWER switch on the drum memory power supply to the down (off) position.

b.   Remove power from the computer by means of the computer POWER switch.

c.   Gain access to the computer card cage, and insert the data channel interface card (part no. 12610-6001) in the card-slot corresponding to the desired I/O address and select code.

d.   Insert the command channel interface card (part no. 12610-6002) in the card slot immediately to the right of the slot used for the data channel interface card.

e.   Connect the double connector on the end of the interface cable (part no. 12610-6004) to the two interface cards. The portion of the connector marked DATA must fit

on the data channel interface card, and the portion marked COMMAND must fit on the command channel interface card.

CAUTION

In the next step, do not accidentally make connection to connector J2 on the drum memory. Connector J2 is the center connector of three which are situated beneath the drum memory.

f.   Connect the 50-pin plug on the interface cable to connector J1 beneath the drum memory. (When facing the DRUM READY lamp on the drum memory, J1 is the leftmost of the three connectors beneath the drum.) Leave sufficient slack in the cable to prevent strain.

2-18.   INSTALLATION CHECKOUT.

2-19.   After installation, turn on the computer and drum memory power supply. Allow four minutes for the drum rotor to reach operating speed. Then check the operation of the drum memory, drum memory power supply, and drum memory interface kit by running the drum memory diagnostic program described in the supplement to this manual. In the read/write portion of the program, check all tracks and sectors on the drum, making at least three passes of the test using the worst-case test word: 1100110011001100CC. The worst-case word should be rotated one bit-position each successive pass.

SECTION III

PROGRAMMING

3-1.   INTRODUCTION.

3-2.   This section contains information for programming the drum memory interface. The following topics are discussed:

    a. Drum characteristics.
    b. Sector and track addresses.
    c. Channel addresses.
    d. Timing.
    e. Parity.
    f. Drum status word.
    g. Read/write transfer.
    h. Track address incrementing.
    i. Multiple drum programming.
    j. Track protection.
    k. Write or read abort.
    l. DMA lockup.
    m. Power-off periods.
    n. Interrupts.
    o. Programming procedure.

3-3.   Refer to the operating and service manual for the DMA option for additional programming information.

3-4.   DRUM CHARACTERISTICS.

3-5.   Data is organized on the surface of the drum in tracks, sectors, words, and bits. Each track extends around the entire circumference of the drum, and contains 32 sectors. Each sector consists of 64 17-bit words. Included in the 17 bits is a parity bit. There are 2048 words in each track. As the drum rotates, each track passes under a read/write head, which records or acquires data when directed by the program. One point in each track, preceding the first word in the first sector, is called the track origin.

3-6.   Table 3-1 shows the principal programming characteristics for the three types of drum.

3-7.   As the table shows, the HP 2775A Drum Memory has 768 tracks. The 2773A Drum Memory has basically 192 tracks, which can be increased to 512 tracks. The 2774A has a basic capacity of 384 tracks, which can be expanded to 512 tracks. The expansion in track capacity is brought about in 90-track increments, and can be made either in the factory or in the field. When a 2773A has 384 or more tracks it is physically and electrically identical with the 2774A, and when such a model is shipped from the factory, it is designated the 2774A.

3-8.   SECTOR AND TRACK ADDRESSES.

3-9.   The smallest addressable unit of data in the drum memory is one sector (64 words). In each track, the sectors

Table 3-1. Drum Memory Characteristics

DRUM TYPE	QUANTITY OF TRACKS	TRACK ADDRESS RANGE (OCTAL)	TOTAL NO. OF WORDS
2773A	192	0000 thru 0277	393,216
2773A	256	0000 thru 0377	524,288
2773A	320	0000 thru 0477	655,360
2773A/ 2774A	384	0000 thru 0577	786,432
2773A/ 2774A	448	0000 thru 0677	917,504
2773A/ 2774A	512	0000 thru 0777	1,048,576
2775A	768	0000 thru 1377	1,572,864

NOTE: Numbers in this table are in decimal form unless otherwise specified.

are identified by the octal numbers 00 through 37, proceeding in numerical sequence from the track origin.

3-10.   Tracks are identified in octal notation, starting with track number 0000 and proceeding in numerical sequence to the highest numbered track.

3-11.   CHANNEL ADDRESSES.

3-12.   The drum system has a data channel and a command channel, each of which can be addressed by the computer program. The data channel is associated with the data channel interface card, and is addressed by using the I/O select code for that card. The command channel is associated with the command channel interface card, and is addressed by the I/O select code for the command channel card.

3-13.   COMMAND CHANNEL I/O SELECT CODE.

3-14.   The command channel I/O select code can be used in the OTA/B and LIA/B instructions. The OTA/B instruction sends to the drum system a control word which specifies the starting track and starting sector for a drum data transfer operation. The control word also indicates whether reading or writing will take place. The LIA/B instruction acquires a drum status word from the drum system.

3-15.   DATA CHANNEL I/O SELECT CODE.

3-16.   Two instructions use the data channel I/O select code; these are the STC and CLC instructions. The STC

instruction initiates the transfer of data to or from the drum after preliminary instructions have established the drum and core-memory locations to be used. The STC instruction must come after the OTA/B instruction that furnishes the control word containing the drum starting address. However, the time between the OTA/B and STC instructions can be any time that is convenient. The CLC instruction is used to abort a drum read or write operation by cutting off data transfer during the course of the operation.

3-17. TIMING.

3-18.   Timing characteristics of the drum are as follows (all figures are approximate because drum speed may vary slightly from the nominal amount).

a. Speed: 3450 RPM for a drum operating from a 60-Hz power line, 2880 RPM for a 50-Hz power line.

b. Maximum access time (time for one drum revolution): 17.4 milliseconds for the 60-Hz drum, 20.8 milliseconds for the 50-Hz drum.

c. Average access time: 8.7 milliseconds for the 60-Hz drum, 10.4 milliseconds for the 50-Hz drum.

d. Word transfer rate to or from the drum:

(1) For the 60-Hz drum, 8.5 microseconds per word, 550 microseconds per sector, 17.4 milliseconds per complete track (2048 words), 118,000 words per second.

(2) For the 50-Hz drum, 10.0 microseconds per word, 645 microseconds per sector, 20.0 milliseconds per complete track (2048 words), 98,000 words per second.

3-19.   The address of the next sector to pass under the read/write head forms part of the drum status word. By examining the next-sector address, the program can most efficiently utilize time. For instance, if drum data are to be read from two groups of sectors, the sectors that will be first to pass under the read/write head can be read first. Another use of the next-sector address is to determine the next sector or sectors available for writing.

3-20.   The address indicated for the next sector could immediately precede an address in which reading or writing is desired. However, the time required for execution of read or write instructions may make it impossible to access the desired sector until the following drum revolution. A flag in the drum status word is set to logic 1 when it is impossible to access the next sector in the current drum revolution. When the flag is logic 0, access to the next sector may be possible, depending on how many read or write instructions are required and on how close the sector is to the read/write head. Since there is no indication of the distance of the sector from the read/write head, obtaining access to the sector in the same drum revolution can be expressed only as

a probability. Figure 3-1 shows this probability. The horizontal axis of the graph is the time from the end of the LIA/B instruction which acquires the drum status word, to the end of the STC instruction which initiates a transfer of data to or from the drum. Included in figure 3-1 is a line showing the probability of accessing sector N+1, where N is the next sector. As the illustration shows, the access times are dependent on the power line frequency for which the drum is designed.
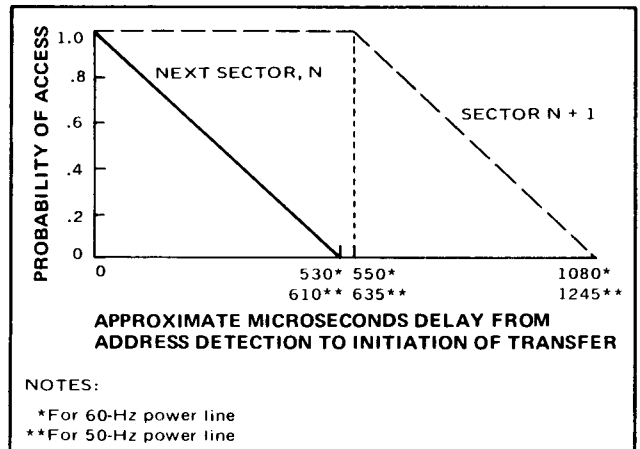
Figure 3-1. Probability of Sector Access in Current Drum Revolution

3-21. PARITY.

3-22.   Each word written on the drum consists of 16 data bits and one parity bit. The parity bit is generated when the word is written, and parity is automatically checked each time the word is read. Occurrence of a parity error is indicated by a flag in the drum status word.

3-23. DRUM STATUS WORD.

3-24.   The drum status word is a 16-bit word which can be acquired from the drum system by the LIA/B instruction. The instruction must use the drum command channel I/O select code.

3-25.   The format and content of the drum status word are shown in table 3-2. The various parts of the word are updated at different times.

3-26.   Bits 3 and 1 of the drum status word are reset to logic 0 by an STC instruction with the drum data channel I/O select code. Since this instruction starts a transfer of data to or from the drum, a check of bits 3 and 1 after completion of the data transfer provides an indication of certain types of data transfer failure.

3-27. READ/WRITE TRANSFER.

3-28.   At least one sector must be allowed to elapse between the end of a read or write operation and the start of another read or write operation. This precaution must be observed because there is insufficient time between sectors

Table 3-2. Drum Status Word

BITS	DESCRIPTION
15	Sector Flag. Logic 1 indicates that the sector designated by bits 12-8 of the drum status word is not accessible in the current drum revolution.
14 thru 13	Not used.
12 thru 8	Next-Sector Address. Indicates address of sector which will follow the sector currently under the read/write heads. Bit 8 is the low-order bit.
7	Drum Ready Flag. Logic 1 indicates that the drum is ready for use or is in use. Logic 0 indicates that the drum is currently not ready for use for one of the following reasons: a. Low drum speed. b. HEADS switch not at the IN position. c. Certain drum circuits are defective. d. Drum memory not connected to the computer. e. Drum memory not connected to the drum power supply. f. Low line voltage or no line voltage applied to the drum power supply. g. Drum power supply defective or not turned on.
6	Not used.
5	Sector Address Coincidence Flag. Logic 1 indicates that sector address coincidence has occurred since the last STC instruction addressed the drum data channel. Logic 0 indicates that sector address coincidence has not occurred. This bit is used only for equipment troubleshooting purposes.
4	Not used.
3	Abort Flag. Logic 1 indicates that bit 7 of the drum status word has been logic 0 at least once since performance of the last STC instruction that addressed the drum data channel. Consequently, the data transfer concerned may not have been successfully completed. Logic 0 indicates that bit 7 has been logic 1 since the last STC instruction which addressed the drum data channel. Bit 3 is reset by an STC instruction that addresses the drum data channel.
2	Writing Enabled Flag. Logic 1 indicates that the currently selected drum track is not protected by the track protect switch. Logic 0 indicates the track is protected. This bit has significance only after a drum track has been specified for writing by an OTA/B instruction. If the track address is incremented because end-of-track has been reached while reading or writing, bit 2 indicates the protect status of the new track.
1	Parity Error Flag. Logic 1 indicates read parity error has occurred. Logic 0 indicates no read parity error has occurred. Bit 1 is reset by an STC instruction that addresses the drum data channel.
0	Drum Busy Flag. Logic 1 indicates that a drum read or write operation is being initiated, is in progress, or is being terminated. Logic 0 indicates that none of these conditions exists. If writing or reading ends before the end of a sector, the busy flag remains logic 1 until the end of the sector is reached.

to program the second operation. If an attempt is made to perform such an operation, the first operation will either be aborted before the transfer of all data, or the second operation will wait until rotation of the drum brings the desired sector around for the second time.

3-29. TRACK ADDRESS INCREMENTING.

3-30.   When the last sector in a track is reached, and additional sectors remain to be written or read, the current track address is automatically incremented by 1. Writing or reading then continues from sector 00 of the next-higher-numbered track, and continues in subsequent sectors of the new track. Track incrementing continues until the specified quantity of words has been written or read. However, after the highest numbered track writing or reading ceases; imaginary tracks are then written or read until track 1777 octal (imaginary), after which actual writing or reading begins again in track 0000. Caution must be exercised that this effect does not erase desired data in track 0000 and subsequent tracks. The actual or imaginary writing or reading ends when DMA has transferred the specified quantity of words from or to core storage.

3-31. MULTIPLE DRUM PROGRAMMING.

3-32.   When a computer utilizes two or more drums, programming procedures require only that the appropriate command channel and data channel I/O select codes be used for each drum.

3-33. TRACK PROTECTION.

3-34.   To write on a protected track, the track protect switch is set to the down (nonprotect) position. The switch is returned to the up (protect) position to re-establish the protect status.

3-35. WRITE OR READ ABORT.

3-36.   A drum write or read abort can be initiated by programmed means, or it can be the result of certain types of equipment fault. When an abort occurs, no further data is transferred to or from the drum. If the abort takes place after initiation of a drum operation, but before the first desired sector is reached on the drum, no data is transferred. If fewer than 64 words are programmed to be written or read in the last sector, and an abort of either type occurs after the last desired word has been transferred to or from the drum, the data write or read operation is completed successfully.

3-37.   An equipment-fault abort occurs when certain types of fault occur in the drum system. In some cases, when an abort of this type takes place bit 3 of the drum status word is set to logic 1. (Refer to table 3-2.)

3-38.   Note that bit 3 of the status word can become logic 1 if an equipment fault occurs after completion of the data transfer operation. Therefore, the bit should be checked as soon as possible after completion of data transfer to or from the drum. Completion of transfer can be determined by an examination of the drum busy bit (bit 0) of the status word. If the drum is still busy, the LIA/B instruction which acquires the status word does not interfere with the transfer of data to or from the drum.

3-39.   A programmed abort is brought about by a CLC instruction that addresses the data channel, or which has an I/O select code of zero. A programmed abort also occurs if an OTA/B instruction addresses the command channel. (Such an OTA/B instruction usually is performed in order to start another drum read or write operation.)

3-40. DMA LOCKUP.

3-41.   If a drum write or read operation is aborted as a result of an equipment fault, the DMA system will lock up. When this situation occurs, DMA waits to transfer more words to or from the drum, but the drum system does not send a signal to DMA to indicate that another word is required (when writing) or is ready (when reading).

3-42.   It should be noted that a programmed abort, using a CLC instruction with the drum data channel I/O select code or with a zero I/O select code, does not cause DMA lockup.

3-43.   When DMA lockup has occurred, a programmed check of the DMA channel, using an SFS or SFC instruction with the DMA channel I/O select code, will indicate that the DMA channel is busy. Furthermore, a check of the drum busy bit (bit 0) of the drum status word will indicate that the drum is busy.

3-44.   The lockup condition continues until one of the following actions is performed:

a.   Clear the entire I/O system by programming a CLC instruction with a zero I/O select code.

b.   Start a new drum write or read operation on the same DMA channel, using the normal drum and DMA initiation instructions. (The 2114B Computer has only a single DMA channel.)

c.   Perform a CLF instruction with the DMA channel I/O select code, and a CLC instruction with the drum data channel I/O select code. These two instructions can be programmed in any sequence.

d.   Stop the program, then press the PRESET switch.

e.   Turn off computer power, then restore power.

3-45.   Existence of DMA lockup is indicated by bit 3 of the drum status word. (Refer to table 3-2.) If this bit is logic 1 after sufficient time for completion of the data transfer, an equipment-fault abort has occurred. Another method of checking for an equipment fault abort is to perform an LIA/B instruction with the DMA channal I/O select code. If sufficient time has been allowed for completion of the transfer, the word count should be zero.

3-46.   Checking for an abort condition as described in the preceding paragraph will not interfere with the data transfer operation, if it is still in progress. The check should be made as soon as possible after completion of the transfer of data. This will avoid the possibility of an equipment fault setting the abort flag after completion of the data transfer, thereby erroneously indicating that the transfer was not completed.

3-47.   If the computer has two DMA channels, the channel not used for the drum write or read operation is not affected by a DMA channel lockup.

3-48. POWER—OFF PERIODS.

3-49.   If ac power is removed from the computer or the drum memory power supply and then restored, data recorded on the drum is retained. However, if drum writing is taking place at the time of power removal, erroneous data may be recorded in the sector in which writing is taking place. If power is removed from the drum memory power supply but not from the computer, the drum ready flag (bit 7 of the drum status word) is logic 0 during the power-off period. Also, the abort flag (bit 3 of the status word) becomes logic 1, and it remains 1 after restoration of drum power. When power is restored to the drum after a power failure, it will restart without manual intervention.

3-50. INTERRUPTS.

3-51.   The drum system does not furnish or receive program interrupts.

3-52. PROGRAMMING PROCEDURE.

3-53.   Transfers of data to and from the drum memory are controlled by the DMA system of the computer. The DMA system transfers the drum data to or from the core memory in the computer, suspending the computer program one machine cycle for every 16-bit word transferred. (One machine cycle requires 2.0 microseconds for the 2114B or 2115A Computer, 1.6 microseconds for 2116A or 2116B Computer.) The rate of transfer is determined by the rate at which the drum memory can furnish or receive data.

3-54.   The DMA system can transfer up to 16,384 words with one initializing subroutine. One sector is the minimum addressable data unit in the drum memory; however, as few as 2 words can be written in the sector. These words will appear in the first two word locations of the sector addressed. The remainder of the sector will contain the same word that was written in the second word location. Similarly, if more than one sector is written, the last sector can contain from 2 to 64 words. If the last sector contains fewer than 64 words, the last word written is repeated in the track for the remainder of the sector. Thus any number of words up to 16,384 can be written or read with a single initialization, with the exception of 1 modulo 64 words. (That is, any number of words up to 16,384 can be written,

with the exception of 1 plus any multiple of 64.) if writing or reading of one word is programmed, the word will not be transferred to or from the drum. Similarly, if 1 modulo 64 words is programmed, the last word will not be transferred to or from the drum.

3-55.   In a read or write subroutine the particular use made of the drum status word is determined by the type of operation being performed, the program time available, and the amount of core storage that can be allocated to the subroutine. Therefore, no concrete rules can be laid down regarding use of the drum status word.

3-56.   Normally, the first step in a drum read or write subroutine is to acquire the current drum status word with an LIA/B instruction addressed to the command card. Bits 7 and 0 are then checked to ensure that the drum can be used (refer to table 3-2). Bits 15 and 12 through 8 are also checked if the address of the next sector is pertinent to the operation being programmed.

3-57.   After appropriate portions of the drum status word have been checked, initialization of a drum operation follows the procedures used with DMA data transfers. (Refer to the operating and service manual for the DMA option.) In the initialization procedure, four 16-bit control words are used. These are referred to as CW1, CW2, CW3, and CW4. Through the use of the OTA/B instruction the first three of these are forwarded to the DMA system, and the last is furnished to the drum command channel. Table 3-3 describes each of the control words.

3-58.   If a drum write operation is to be performed, the drum status word can be read a second time after the drum track is specified by a CW4 word, and bit 2 of the status

Table 3-3. Data-Transfer Control Words

CONTROL WORD	DESCRIPTION
CW1	CW1 is the DMA program control word. Format and content are as follows: Bit 15. If logic 1, turn on the drum control bit flip-flop (perform the function of an STC instruction) after each word is transferred to or from the drum. If logic 0, do not turn on the drum control flip-flop after each word. Bit 14. This bit specifies whether DMA will handle 8-bit bytes or 16-bit words. Since the drum memory stores 16-bit words, bit 14 must be logic 0 for drum data transfers. Bit 13. If logic 1, turn off the drum control bit flip-flop (perform the function of a CLC instruction) after the last drum word has been transferred. If logic 0, do not turn off the drum control bit flip-flop after the last word. Bits 12 thru 6. Not used. Bits 5 thru 0. Drum data channel I/O select code. Bit 0 is the low-order bit.
CW2	CW2 is the DMA memory address register word. Format and content are as follows: Bit 15. Logic 1 specifies core memory write. Logic 0 specifies core memory read. Bits 14 thru 0. Core memory starting address. Bit 0 is the low-order bit.

Table 3-3. Data-Transfer Control Words (Continued)

CONTROL WORD	DESCRIPTION
CW3	CW3 is the DMA block length word. Format and content are as follows: Bits 15 and 14. Not used. Bits 13 thru 0. The 2's complement of the number of words to be transferred to or from the drum. Bit 0 is the low-order bit.
CW4	CW4 is the drum function and drum address word. Format and content are as follows: Bit 15. Logic 1 specifies drum write. Logic 0 specifies drum read. Bits 14 thru 5. Drum starting track. Bit 5 is the low-order bit. Bits 4 thru 0. Drum starting sector. Bit 0 is the low-order bit.

word can then be checked to ensure that the track is not protected. It is particularly desirable to check bit 2 when the track-protect switch must be set to the nonprotect position in order to write in the selected track. After completion of the data transfer to or from the drum, the drum status word can be read once more to check bit 3. If this bit is logic 1, the data transfer was probably not completed successfully. After a read operation bit 1 can also be checked to determine whether a parity error occurred.

3-59.   To illustrate the use of the control words, and to demonstrate the principles of drum programming, table 3-4 presents a typical drum subroutine. For simplicity, the subroutine makes no checks of the drum status word. The subroutine reads a block of 4096 (decimal) words from the drum, starting at sector 25 (octal) of track 10 (octal), and stores the words in core memory starting with address 10,000 (octal). DMA channel 1 is used, and the drum interface cards are in slots having an I/O select code of 10 (data channel card) and 11 (command channel card). The control words are as follows:

   a. CW1: 020010 (octal). This control word turns off the drum control bit flip-flop after the last word has been transferred (bit 13 is logic 1), and specifies the I/O select code of the drum data channel (bits 5 through 0 are 10, octal).

   b. CW2: 110000 (octal). This control word specifies a core memory write operation (bit 15 is logic 1) and designates the starting address in core memory (bits 14 through 0 are 10000, octal).

   c. CW3: -4096 (decimal). This control word, after program assembly, specifies the 2's complement of the number of words to be transferred.

   d. CW4: 000425 (octal). This control word specifies drum read (bit 15 is logic 0), track 10 (bits 14 through 5 are 0010, octal) beginning with sector 25 (bits 4 through 0 are 25, octal).

Table 3-4. Typical Drum Subroutine

OP CODE	OPERAND	REMARKS
		INITIALIZE DMA CHANNEL 1
LDA	CW1	Fetch CW1 from core memory and load in the A-register.
OTA	6	Output CW1 to DMA channel 1.
CLC	2	Prepare DMA channel 1 memory address register to receive CW2.
LDA	CW2	Fetch CW2 from core memory and load in the A-register.
OTA	2	Output CW2 to DMA channel 1.
STC	2	Prepare DMA channel 1 word-count register to receive CW3.
LDA	CW3	Fetch CW3 from core memory and load in the A-register.
OTA	2	Output CW3 to DMA channel 1.
		INITIALIZE DRUM MEMORY
LDA	CW4	Fetch CW4 from core memory and load in the A-register.
OTA	11	Output CW4 to drum command channel.
		START TRANSFER OF DATA
STC	6,C	Activate DMA channel 1.
STC	10	Initiate drum data transfer.

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION.

4-2.   This section explains the circuit theory of the data channel interface card and the command channel interface card. Operations of the drum memory and computer are described only to the extent required for explaining the functioning of the two interface cards.

4-3.   For brevity, the names of equipment items mentioned in this section have been shortened as follows:

   a. The HP 12610-6001 Data Channel Interface card is referred to as the "data card".

   b. The HP 12610-6002 Command Channel Interface card is referred to as the "command card".

   c. The HP 2773A, 2774A, or 2775A Drum Memory is referred to as the "drum memory" or "drum".

   d. The HP 2776A or 2777A Drum Memory Power Supply is referred to as the "drum power supply".

   e. The HP 2114B, 2115A, 2116A, or 2116B Computer is referred to as the "computer".

   f. The HP 12578A, 12578A-001, or 12607A Direct Memory Access is referred to as "DMA" or the "DMA system".

4-4. OVERALL FUNCTIONAL DESCRIPTION.

4-5.   The data card and command card, under control of the computer, perform the following functions:

   a. Determine when the first drum sector of a read or write operation reaches the drum read/write head.

   b. When writing on the drum, receive 16-bit parallel words from the computer, generate a parity bit (odd parity is used), and forward the resulting 17-bit word, serially and in 1's complement form, to the drum.

   c. When reading from the drum, receive 17-bit 1's complement serial words from the drum, recomplement each word, check parity, and forward the 16 data bits in parallel to the computer.

   d. Prevent writing on protected tracks.

   e. Forward a drum status word to the computer.

   f. Continue writing or reading from sector 00 of the next-higher-numbered track when the end of a track is reached.

4-6.   Interface circuits for controlling the transfer of data to and from the drum are situated principally on the command card. Additional control circuits are located on the data card, together with circuits for handling the data transferred.

4-7.   The DMA system transfers to or from the computer all words written on the drum or read from the drum. DMA and the drum memory conduct these operations without the performance of computer instructions, other than those required to initiate the operation.

4-8. DETAILED THEORY.

4-9.   REFERENCE INFORMATION.

4-10.   The following paragraphs present general information which is required for understanding the detailed theory discussion that follows.

4-11.   BINARY VOLTAGE LEVELS. The binary signal levels on both interface cards are approximately +3.5 volts and +0.2 volts. The levels may vary from these approximate amounts, depending on the type of integrated circuit providing the signal. The input and output voltage levels for each type of integrated circuit are specified in section V of this manual.

4-12.   LOGIC CIRCUITS. The logic circuits on both interface cards principally employ positive logic. That is to say, all inputs to an "and" or "nand" gate must be +3.5 volts for coincidence to occur. Similarly, if any input to an "or" or "nor" gate is +3.5 volts, the output is +3.5 volts for an "or" gate or +0.2 volts for a "nor" gate. The output from the "set" side of a flip-flop is approximately +3.5 volts when the flip-flop is set, and +0.2 volts when the flip-flop is reset. As an exception to the use of positive logic, diodes CR1 through CR10 on the data card, together with the circuits to which they connect on the command card, form a negative "and" gate. Also, "nand" gate MC12B on the data card, and "nand" gates MC35A, MC35C, and MC55B on the command card, are used as negative-logic "nor" gates.

4-13.   In accordance with established usage for positive-true logic circuits, the term "true" in this manual refers to a nominal signal level of +3.5 volts, and "false" refers to a nominal level of +0.2 volts.

4-14.   ABBREVIATIONS. Signal-name abbreviations are listed in tables 5-3 and 5-5, together with the meanings of the abbreviated designations. For the meanings of abbreviations and letter symbols which are not signal names, refer to tables 4-2, 4-3, and 6-2.

4-15.   SIGNAL NAMES. Signals which enter or leave the two interface cards are named in one of the following ways:

    a. As a condition which either exists or does not exist.

    b. As a command or order, expressed in the imperative grammatical mode.

    c. In accordance with the name of a flip-flop which is the source of the signal.

    d. In accordance with the name of the bus which carries the signal.

4-16.   Since most of the circuits on the two interface cards employ positive logic, signal names are positive-true. The following paragraphs describe the expression "positive-true name" as applied to each of the four types of signal names.

4-17.   When a signal is named in accordance with a condition, the signal level is +3.5 volts when the condition exists, and +0.2 volts when the condition does not exist. For instance, the TO (track origin) signal is +3.5 volts when the drum track origin is passing the read/write heads, and +0.2 volts when the track origin is not passing the read/write heads. Similarly, the "not" RY signal is +3.5 volts when the drum is not ready, and +0.2 volts when it is ready.

4-18.   In further accordance with the principle of positive-true signal names, a signal which is named in the imperative mode becomes +3.5 volts to bring about the action commanded. For instance, the Flag FF is cleared when the CLF (clear flag) signal changes from +0.2 volts to +3.5 volts.

4-19.   When a signal is named in accordance with the flip-flop which is its source, the signal taken from the set side of the flip-flop is +3.5 volts when the flip-flop is in the set condition, and +0.2 volts when the flip-flop is in the reset condition. For instance, when the Control Bit FF is set, the CB signal is +3.5 volts.

4-20.   When a signal is named in accordance with the bus which carries it, the signal is +3.5 volts when the bus carries a logic 1, and +0.2 volts when it carries a logic 0.

4-21.   DRUM SIGNALS. All control signals and data signals that enter or leave the drum pass through the two interface cards. The control signals are illustrated in figure 4-1. The operating and service manual for the drum memory provides information on the timing of signals originating in the drum.

4-22.   MULTIPLE DRUMS. If more than one drum is connected to the computer, each drum has its own interface kit.

4-23.   LOCATION OF CONTROLS. Table 4-1 gives the location of controls mentioned in the detailed theory discussion in this section.

Table 4-1. Location of Controls

CONTROL	LOCATION
AC POWER switch	Drum memory power supply
DC POWER switch	Drum memory power supply
HEADS switch	Drum memory
PRESET switch	Computer
POWER switch	Computer

4-24.   ADDITIONAL INFORMATION. Logic diagrams for the two interface cards are furnished in figures 5-3 and 5-5, in section V of this manual. Interconnections between the two cards, and between each card and the drum memory, are listed in tables 5-3 and 5-5. In the logic diagrams and tables, pins marked with an asterisk plug into the 48-contact interface connector. Pins without an asterisk plug into the 86-contact backplane connector.

NOTES:
1. NOT TO SCALE HORIZONTALLY
2. THE $\overline{W}$ OR $\overline{R}$ SIGNAL SHOWS WRITING OR READING IN THE FIRST TWO SECTORS
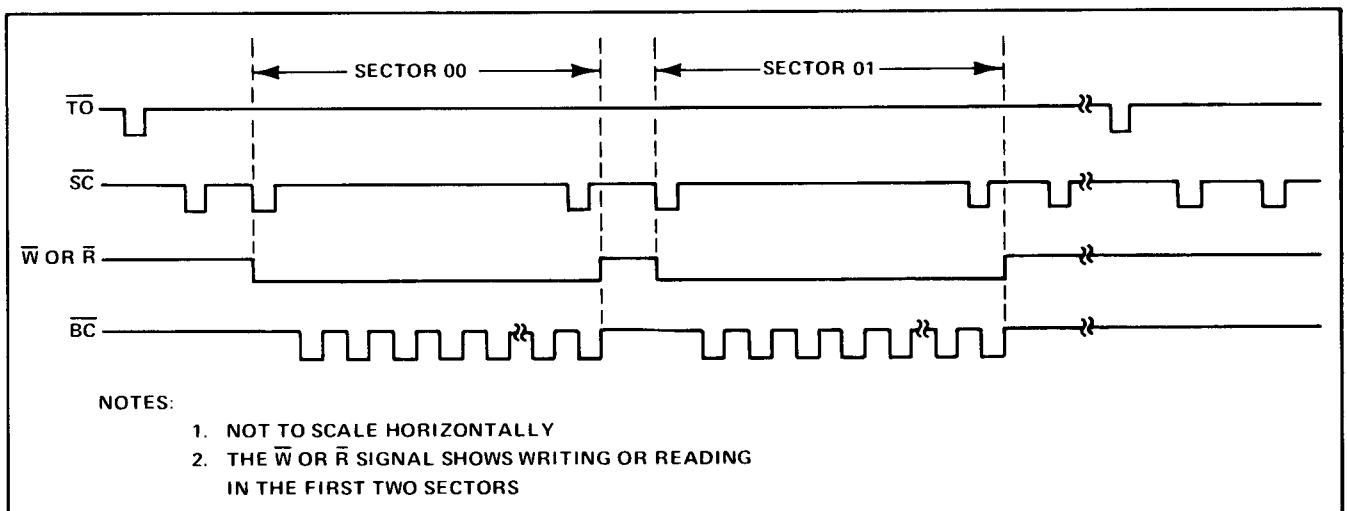
Figure 4-1. Control Signals Transferred to and from Drum Memory, Timing Chart

4-25. Connections from the cards to the computer are listed in the backplane wiring list for the computer.

4-26. Tables 4-2 and 4-3 list the flip-flops and registers on the two interface cards, and briefly describe the functions they perform.

4-27. The figures and tables mentioned above should be referred to as necessary while reading the detailed theory discussion which follows.

4-28. POWER—ON INITIALIZATION.

4-29. When power is applied to the computer by the POWER switch, a CRS signal is supplied to the data card for approximately 40 milliseconds. The signal, consisting of a series of T5 pulses, is inverted on the data card, and clears the Control Bit FF and Flag FF. The inverted signal also clears the Run FF on the command card. When the Run FF is in the reset condition, the "not" R and "not" W signals are true, preventing drum reading or writing that could result from the unpredictable state of flip-flops during and after power turn-on. When the computer is not running, pressing the PRESET switch also generates the CRS signal, producing the same results as at power turn-on.

4-30. To further ensure that drum writing does not take place during the transient conditions of the power turn-on period, the PON signal from the power fail interrupt card is applied to the base of transistor Q1 on the command card. The PON signal is false for about 40 milliseconds during and after power turn-on. For this period of time it keeps transistor Q1 cut-off, providing protection against drum writing. In addition, the PON signal is false during the power turn-off period, providing protection at that time also.

Table 4-2. Data Card Flip-Flops and Registers

FLIP-FLOP OR REGISTER	FUNCTION
Control Bit FF	Set by an STC instruction that uses the I/O select code of the data card. Reset by a CLC signal generated by the DMA system. Can also be reset by a CLC instruction performed by the computer, using the I/O select code of the data card. When set, initiates transfer of data to or from the drum. Remains set during and between drum sectors. When reset, terminates drum operation at the end of the current drum sector.
Data Shift Register	When writing, furnishes data to the drum in serial form. When reading, receives data from the drum in serial form. Flip-flop D0 contains the low-order bit before shifting starts (when writing) or after shifting ends (when reading).
Flag FF	Set when a new word is needed for transfer to the drum (when writing), or set when a new word has been acquired from the drum (when reading). Initiates action by DMA to furnish another word (when writing), or to acquire the new drum word (when reading). Cleared by a CLF signal received from DMA. Can also be cleared by a CLF instruction that uses the data card I/O select code.
Input Register	Used only when writing on drum. Receives from DMA each word to be written, and holds it for loading into the data shift register. Flip-flop I0 contains the low-order bit.
Track Address Register	Contains the 1's complement of the address of the track in which writing or reading will take place or is taking place. Flip-flop "not" TA0 contains the low-order bit. The register is loaded by the 1's complement of bits 14 thru 5 of a word transferred from the computer by an OTA/B instruction addressed to the command card. When the end of a track is reached during writing or reading, the contents of the track register are incremented by 1 to cause writing or reading to continue in the next track. The register retains its final contents after completion of the write or read operation until another OTA/B instruction loads a new address in the register.
Output Register	Used only when reading from the drum. Receives from the data shift register each word read from the drum, and holds the word until DMA acquires it. Flip-flop O0 contains the low-order bit. Contents are changed each time a new word read from the drum is furnished by the data shift register.
Write Parity (WP) FF	Used to furnish the parity bit when writing on the drum. Set before start of writing each word, then toggled by each logic 1 sent to the drum. After 16 data bits have been transferred to the drum, the WP FF is in the condition for furnishing the parity bit. Odd parity is used.

Table 4-3. Command Card Flip-Flops and Registers

FLIP-FLOP OR REGISTER	FUNCTION
Abort Store FF	Cleared when an STC instruction addresses the data card. Set when the "not" RY signal becomes true, or when the drum is disconnected from the command card. The state of the Abort Store FF can be determined by examining bit 3 of the drum status word. (Refer to table 3-2.)
Bit Counter	Counts "not" BC pulses received from the drum when writing or reading takes place. Flip-flop B0 contains the low-order bit. When 15 pulses have been received, the counter contains a binary 1 in each position, and an associated "nand" gate indicates the approach of the end of a word being transferred serially to or from the drum. The 16th "not" BC pulse clears the counter, and the 17th attempts to advance the counter to 1. However, the WRD FF is then in the reset condition, and the counter is held in the cleared state. The counter thus contains zero at the start of the next word. The bit counter is also cleared at the start of each sector by the second "not" SC pulse of the sector. The bit counter runs only when drum writing or reading takes place.
Direction (DI) FF	Indicates whether drum writing or reading is taking place. Set for writing, reset for reading, by an OTA/B instruction that addresses the command card.
End-of-Sector (EOS) FF	Indicates when the end of a sector is reached on the drum. Set at the end of the 64th word in the sector, and reset by the leading edge of the second "not" SC pulse of the next sector.
Read Parity (RP) FF	Performs a meaningful function during drum reading only. Set at the start of each sector, then toggled by each logic 0 read from the drum. If clear at the end of a 17-bit word, a parity error existed in the word. After the first parity error of a sector is detected, the RP FF no longer performs a meaningful function.
Read-Parity Error (RPE) FF	Performs a meaningful function during drum reading only. Checks the state of the RP FF at the end of reading each word. If the RP FF found an odd number of logic 0's in the word (a parity error condition), the RPE FF is set. The RPE FF remains set, regardless of additional parity errors, until an STC instruction addresses the data card. The state of the RPE FF can be examined by checking bit 1 of the drum status word.
Run FF	Set at the leading edge of the second "not" SC pulse for a sector in which drum reading or writing will take place. Reset at the end of each sector.
Sector Address Coincidence FF	Indicates that the sector specified for drum reading or writing has been reached. Set by the first "not" SC pulse of the specified sector. Reset when drum operation is completed or aborted.
Sector Address Register	Receives the address of the sector in which drum writing or reading will start. Flip-flop S0 contains the low-order bit. The register is loaded by bits 4 thru 0 of a word transferred from the computer by an OTA/B instruction addressed to the command card. The register retains its contents until a new sector address is loaded.
Sector Clock Phase (SCP) FF	In the set condition between the trailing edges of each pair of "not" SC pulses. Serves as a divide-by-two counter for the sector counter input, and is also used to differentiate between the first and second "not" SC pulses.
Sector Counter	Contains a binary number that is one greater than the address of the drum sector passing the read/write heads. Flip-flop SC0 contains the low-order bit. The counter contains zeros when the current sector is 37 (octal). The counter is advanced by the second "not" SC pulse of each sector, and is cleared each time track origin passes the read/write heads.
Sector Select Register	Contains a binary number one greater than the address of the drum sector passing the read/write heads. Flip-flop SC0 contains the low-order bit. The register is updated by the first T3(B) pulse occurring after the sector counter is updated. The output of the sector select register forms bits 12 thru 8 of the drum status word.

Table 4-3. Command Card Flip-Flops and Registers (Continued)

FLIP-FLOP OR REGISTER	FUNCTION
Store Sector Phase (SSP) FF	Set or cleared by the first T3(B) pulse after the SCP flip-flop is set or cleared, respectively. Furnishes an indication, synchronized with computer timing, of the state of the SCP flip-flop. The output of the SSP flip-flop is bit 15 of the drum status word.
Strobe (STR) FF	Set at the start of each word read or written. Reset at the end of each word read or written. Controls the transfer of data from the data shift register to the output register (when reading), or from the input register to the data shift register (when writing) on the data card. Also controls setting of the WP FF on the data card (when writing), and the application of SRQ requests to the DMA system.
Word Counter	Counts words transferred to or from the drum. Flip-flop WD0 contains the low-order bit. The counter is reset by the second "not" SC pulse of each sector. The counter runs only during transfer of data to or from the drum.
Word (WRD) FF	When transferring words to or from drum, indicates when the end of each word is reached. Set at the start of each word transferred, reset near the end of each word.

4-31. When the AC POWER and DC POWER switches on the drum power supply are set to the ON position, the drum starts to rotate and the drum memory supplies a true "not" RY signal to the command card. The "not" RY signal is inverted on the command card, and it clears the Sector Address Coincidence FF and sets the Abort Store FF.

4-32. If the drum is not connected to the computer, the "not" RY input pin to the command card faces an open circuit, and resistors R7 and R8 on the command card apply a true input to inverter MC53A. This produces the same result as if the "not" RY signal were true. Other faults which will keep the "not" RY signal true are the following:

    a. HEADS switch not at the IN position.

    b. The circuit in the drum memory which supplies the "not" RY signal is defective.

    c. The drum memory is not connected to the drum power supply.

    d. No line voltage is applied to the drum power supply.

    e. The drum power supply is defective or not turned on.

4-33. When the drum is ready for use, the "not" RY signal becomes false. Through "and" gate MC66A on the command card, the inverted "not" RY signal can be gated onto the IOB17 line. This occurs when an LIA/B instruction addresses the command card. The instruction places all IOBI bits from the command card into the A or B register in the computer. These bits constitute the drum status word, and bit 7 will indicate whether the drum is ready for use. (Refer to table 3-2.)

4-34. After the power turn-on period the sector counter, on the command card, assumes an unpredictable condition. The first "not" TO pulse received from the drum resets the counter to zero, after which it functions in synchronism with the "not" SC pulses received from the drum. Figure 4-2 is a timing chart showing the operation of the counter and its associated SCP FF.

4-35. It should be noted that the SCP and SC4 through SC0 FFs are of the dual-rank JK type. The positive-going clock input to each flip-flop gates the signal input into the first rank of the flip-flop. The negative-going clock input transfers the original signal input to the output rank of the flip-flop.

4-36. Each pair of "not" SC pulses advances the sector counter by 1, with the SCP FF functioning as a divide-by-two counter preceding the sector counter. The change of the output rank flip-flops in the sector counter takes place at the trailing edge of the second "not" SC pulse of each pair.

4-37. The first pair of "not" SC pulses after the "not" TO pulse advances the counter to 00001, binary. This number is one greater than the address of the sector that is about to come under the read-write heads. The counter continues to function in this manner for each sector in the track. When the last sector (sector 11111) is reached, the counter is advanced to zero at the beginning of the sector.

4-38. A voltage transient or momentary equipment failure could result in incorrect contents in the sector counter and the SCP FF. If this occurs, the next "not" TO pulse will return the counter and SCP FF to their proper state, restoring normal operation.

4-39. Except when "not" TO is false, each T3(B) pulse applied to the command card gates the contents of the sector counter into the sector select register. From the sector select register the address of the next drum sector can be gated onto the IOBI12 through 8 lines, and placed in the A or B register in the Computer, by an LIA/B instruction that addresses the command card. (Refer to table 3-2, bits 12 through 8.) The T3(B) pulse synchronizes the updating of the sector select register with the computer timing, thereby preventing sampling of the sector address while a carry bit is rippling along the counter.
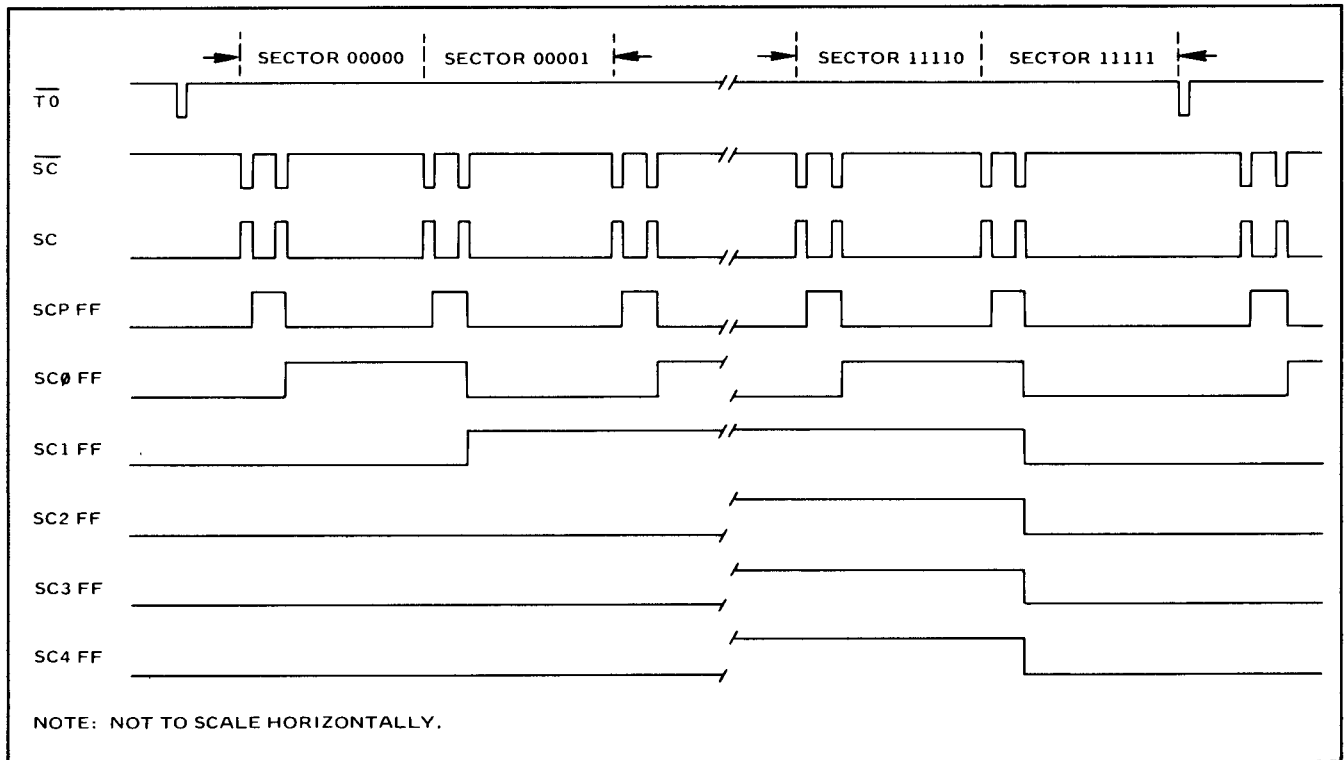
Figure 4-2. Sector Counter Timing Chart

4-40.   After the SCP FF is set, the next T3(B) pulse from the computer timing system places the SSP FF in the same state (set) as the SCP FF. Later, when the SCP FF is reset, its state will again be transferred to the SSP FF by the next T3(B) pulse. The set state of the SSP FF indicates that the sector counter is about to be advanced. This advance occurs when the SCP FF is reset. The condition of the SSP FF can be sampled by an LIA/B instruction which addresses the command card. When this instruction is executed, the IOBI outputs from the command card are loaded into the computer A or B register as the drum status word. Bit 15 of the status word can then be examined by the program to determine the state of the SSP FF. (Refer to table 3-2.) If the SSP FF is set (bit 15 of the status word is logic 1), the next sector is about to pass under the read/write heads. Consequently, it is too late in the current drum revolution to start a write or read operation in the sector indicated by the sector select register (bits 12 through 8 of the status word). If an attempt is made to start such an operation, it will not begin until one drum revolution later. During this revolution of the drum the Run FF remains set. The reset-side output of the Run FF is furnished to "nand" gate MC35A, which functions as a negative-logic "nor" gate. If, during the 1-revolution waiting period, an LIA/B instruction acquires the drum status word, "and" gate MC46B forwards the output of MC35A as bit 0 of the status word. Since the Run FF is set at this time, bit 0 of the status word will be logic 1, indicating that the drum is busy. (Refer to table 3-2.)

4-41.   It has been seen that after power is applied to the computer and drum, the trailing edge of the first "not" SC

pulse after the first "not" TO pulse sets the SCP FF. With this flip-flop set, the second "not" SC pulse (inverted) clears the word counter and EOS FF on the command card through "nand" gates MC34E and MC33E. Also, "nand" gate MC35C sets the STR, WRD, and RP FFs, and clears the Read Inhibit FF. (Gate MC55B, used in clearing the bit counter, functions as a negative-logic "nor" gate.)

4-42.   To summarize the initial condition of the data card and command card after power is applied to the computer and the drum, flip-flops and registers are in the following condition:

a.   The Control Bit FF is reset.

b.   The Flag FF is reset.

c.   The Run FF is reset.

d.   The Sector Address Coincidence FF is reset.

e.   The Abort Store FF is set.

f.   The sector counter contains the address of the next drum sector, and is running.

g.   The sector select register contains the address of the current drum sector, and is running.

h.   The word counter is reset and not running.

i.   The EOS FF is reset.

j. The bit counter is reset and not running.

k. The STR FF is set.

l. The WRD FF is set.

m. The RP FF is set.

n. The Read Inhibit FF is set.

4-43. Other flip-flops and registers on the interface cards could be either set or reset.

4-44. When the command card is addressed by an LIA/B instruction, no change is made in the state of flip-flops on the interface cards. However, when drum reading or writing is initiated, flip-flops are set or cleared as required to start the operation, and the word counter and bit counter start running.

4-45. WRITE OPERATIONS.

4-46. GENERAL. Drum writing requires that the computer initialize the DMA system, then furnish a CW4 word to the drum system by means of an OTA/B instruction addressed to the command card. (The CW4 word is described in section III of this manual.) The computer then initiates writing by executing an STC instruction addressed to the data card.

4-47. OTA/B INSTRUCTION. The CW4 word specifies whether a read or write operation will be performed, and specifies the track and sector in which reading or writing will start. (Refer to table 3-3.) When the OTA/B instruction which supplies this word is executed, the T-register in the computer is reset in the last half of computer time period T0 (see figure 4-3). Then, during T2, the instruction is read from the core storage unit in the computer, and placed in the T-register. The OTA/B instruction is decoded, and the appropriate SCM and SCL signals become true. (There are eight each of the SCM and SCL signals, corresponding to the eight high-order and eight low-order octal digits of the range of I/O select codes that can be used. The signals which become true are those that specify the I/O select code of the command card.)

4-48. At T3 the IOGE(B) and IOO signals become true. With SCM, SCL, IOGE(B), and IOO all true, "nand" gate MC55A on the command card furnishes a false "not" CCB output which ensures that the Read Inhibit FF and Run FF are in the reset condition. (Resetting the Read Inhibit FF is meaningful only when drum reading is to be performed.) Also, pin *19 of the command card furnishes a false "not" CCB signal to pin *19 of the data card to ensure that the Control Bit FF is reset. The resulting false CB signal furnished to pin *W of the command card ensures, in turn, that the Sector Address Coincidence FF is reset.

4-49. If the Control Bit FF was in the set condition, a prior drum read or write operation was in progress. Resetting the Control Bit FF will immediately terminate the former operation. The Run, Read Inhibit, and Sector
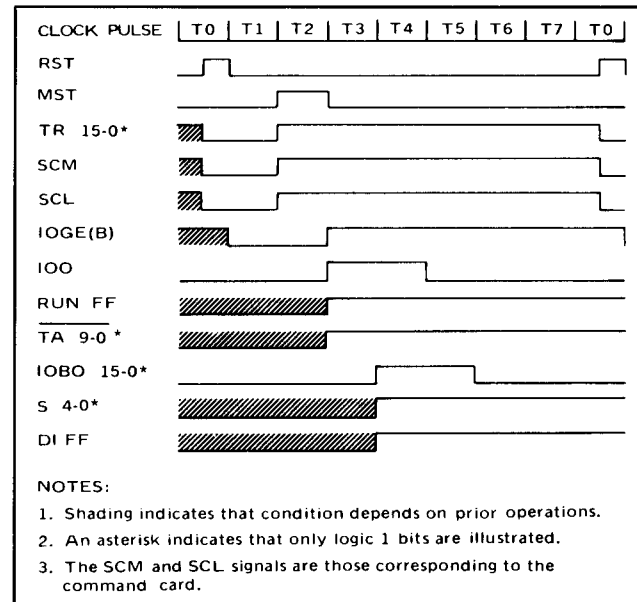
Figure 4-3. OTA/B Instruction and Resulting Drum System Operations, Timing Chart

Address Coincidence FFs might also have been set, hence the necessity for ensuring they are in the reset condition before a new operation is started.

4-50. The output of MC55A on the command card is forwarded to "nand" gate MC43A. The STA signal at the output of MC43A is routed through pin *X to "nand" gate MC53D on the data card. When enabled by the coincidence of signals STA and T3(B), the output of MC53D sets all positions of the track address register to binary 1.

4-51. At T4, the computer places CW4 on IOBO lines 15 through 0. The bit positions of CW4 retain their identification when CW4 is placed on the lines. That is, the bit in position 15 of the A- or B-register is gated onto IOBO line 15, the bit in position 14 of the register is gated onto IOBO line 14, etc.

4-52. On the command card, starting at T3, signal STA enabled the clock inputs to the S4 through S0 FFs of the sector address register. At T4, CW4 is gated onto the IOBO lines. Since the S4 through S0 FFs are of the latch type, they accept any input applied while their clock input is true. By this means the sector address on IOBO lines 4 through 0 is loaded into the sector address register flip-flops. Also at T4, the DI FF on the command card is set by the logic 1 on IOBO line 15. As with the S4 through S0 FFs, the DI FF is of the latch type, which accepts the bit supplied to it at any time while its clock input is true. The logic 1 on IOBO line 15 corresponds to the 1 in bit position 15 of the CW4 word. This 1 indicates that drum writing, rather than reading, will be performed. When the DI FF is set, its reset output is forwarded to the data card, where the false signal resets the D16 FF of the data shift register.

4-53. On the data card, any binary 1's on IOBO lines 14 through 5 are gated into the track address register at T4. The data on the IOBO lines is inverted during this gating, and the track address register will therefore contain a

binary 0 for every binary 1 on the IOBO lines. If there are binary 0's on the IOBO lines, they will not cause "nand" gate coincidence, and the corresponding position of the track address register will retain the binary 1 that was placed in it when the entire register was set at T3. The result will be that the track address register is set to the 1's complement of the starting track address.

4-54.   Although the OTA/B instruction is addressed to the command card, the data on IOBO lines 14 through 5 is loaded into the track address register on the data card. This is made possible by the true STA input applied to pin *X of the data card.

4-55.   S T C   INSTRUCTION. When the computer decodes the STC instruction which initiates drum writing, SCM and SCL signals that address the data card become true at the start of T2. (See figure 4-4.) Signal IOGE(B) becomes true at T3, and the STC signal is true during T4. The STC signal is furnished to the data card, where it sets the Flag FF through "nand" gate MC14B. The output of this gate also resets the data shift register, with the exception of position 16. Position 16 of the register was reset by the preceding OTA/B instruction, which, by setting the DI FF on the command card to indicate a write operation, cleared the D16 FF.
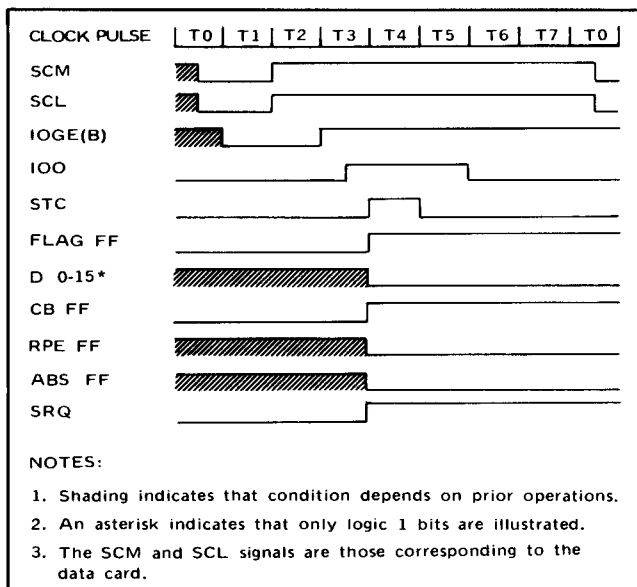

Figure 4-4.   STC Instruction and Resulting Drum
System Operations, Timing Chart

4-56.   The STC signal is inverted and gated by "nand" gate MC15B. The resulting output sets the Control Bit FF, and is forwarded as the "not" CRA signal to the command card. There it resets the RPE and Abort Store FFs. (The RPE reset is meaningful only when drum reading is initiated.)

4-57.   With the Flag FF in the set state, a true SRQ signal is sent to the DMA system by the data card.

4-58.   Upon receipt of the SRQ signal, the DMA system acquires from the computer memory the first word to be written on the drum, and places the word on IOBO lines 15 through 0. Then the DMA system furnishes the following signals to the data card: SCM, SCL, IOGE(B), and IOO. Upon receiving these signals, "nand" gate MC14A on the data card furnishes a clock input to the I15 through I0 FF's of the input register, and the word on the IOBO lines is loaded into the register. DMA also furnishes a CLF signal, resetting the Flag FF on the data card.

4-59.   No further operations take place until the correct sector is reached on the drum. During this interval the Control Bit FF on the data card remains set, and if an LIA/B instruction acquires the drum status word, bit 0 of the status word (the busy bit) will be logic 1.

4-60.   If a CLC instruction addresses the data card while the starting sector is being awaited, the Control Bit FF on the data card will be cleared by a CLC signal, and the drum operation will be aborted before any data is transferred. This programmed abort does not set the Abort Store FF.

4-61.   DRUM WRITING. Drum writing is described in paragraphs 4-62 through 4-107.

4-62.   Sector Coincidence. Writing begins when the starting sector is reached on the drum. It has been seen that the address of this sector is placed in the sector address register by an OTA/B instruction. It has also been seen that the current next-section address is in the sector counter. The contents of the register and counter are compared by "and" gates MC74C, MC74A, MC84D, MC84B, MC84C, MC84A, MC94D, MC94B, MC94C, and MC94A on the command card. These gates compare the set-side outputs of the counter flip-flops with the reset-side outputs of the register flip-flops. They also compare the reset-side outputs with the set-side outputs of the register. When the numbers in the counter and the register are unlike, one or more of the "and" gates encounters coincidence, and furnishes a true signal to one of the "nor" gates MC74E, MC84E, or MC94E. The outputs of the three "nor" gates are "or" tied. Thus if the numbers in the counter and the register are unlike, a false output is provided by the "nor" gates.

4-63.   When the numbers in the counter and register are alike, none of the "and" gates encounters coincidence, all inputs to the three "nor" gates are false, and the output of these three gates becomes true.

4-64.   It will be noted that "nor" gate MC74E receives inputs from "and" gates MC74D and MC74B. These two "and" gates are permanently connected to MC74E within the integrated circuit that contains all the MC74 gates. To prevent MC74D and MC74B from furnishing true signals to MC74E, the inputs to the two "and" gates are connected to ground.

4-65.   It will also be noted that pin 11 inputs to MC74E, MC84E, and MC94E are connected together, as also are pin 12 inputs. By connecting the pins in this way, with no signal or enable input applied to them, the outputs of the three "nor" gates are caused to "or" together.

4-66.   Sector Coincidence FF. When address coincidence is encountered, the output of the three "nor" gates becomes true. This true signal is applied to "nand" gate MC25A. The two other inputs to this gate are the reset-side output of the SCP FF, and the SC (inverted "not" SC) pulse. Figure 4-5 illustrates the signals applied to the gate. In the illustration, "nand" gate input and output signals are identified by the pin numbers of the gate.
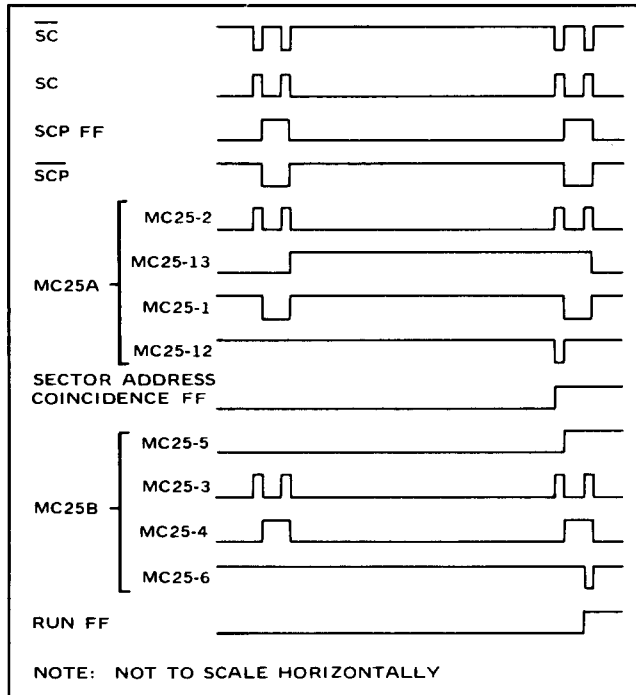

Figure 4-5. Sector Coincidence, Timing Chart

4-67.   As the illustration shows, coincidence for "nand" gate MC25A does not occur until one drum sector after address coincidence takes place. The circuits are designed to operate in this fashion because the number in the sector counter is one greater than the address of the sector under the read/write heads.

4-68.   The output of the Sector Address Coincidence FF is applied to "and" gate MC66B. This gate is enabled when the computer acquires the drum status word with an LIA/B instruction. The instruction gates the IOBI lines into the A or B register of the computer, and by examining the state of the IOBI 5 bit, the program can determine whether the Sector Address Coincidence FF is set.

4-69.   The output of the Sector Address Coincidence FF is also applied to "nand" gate MC53D. The output of this gate, signal "not" ATR, is false when the Sector Address Coincidence FF is set and the drum track origin is beneath the read/write heads. The false "not" ATR signal is forwarded to the "not" TAO FF on the data card, where it advances the track address register. As a result, writing will continue in the next track when the last sector in a track has been written on and an additional sector or sectors remain to be written. It will be noted that the reset output

of each of the "not" TA9 through TA0 FFs is connected to the set and reset inputs of the same flip-flop. As a result, when the clock input to a flip-flop goes false, the flip-flop changes its state. The register will thereby be advanced in such a fashion that the 1's complement number it contains will progress in the correct manner.

4-70.   Run FF. As figure 4-5 shows, the Sector Address Coincidence FF is set by the first "not" SC pulse of the desired sector. The output of this flip-flop is furnished to "nand" gate MC25B, which allows the Run FF to be set by the second "not" SC pulse. MC25B also furnishes a false signal to inverter MC24D, which forwards a true RFW signal to pin *U on the data card. At this time, pins *T and *S on the data card are also receiving true inputs. (The "not" EWW input to pin *S is true because the STR FF on the command card is set.) When the RFW input to pin *U becomes true, "nand" gate MC22A on the data card experiences coincidence, and its output becomes false. As a result, the output of "nand" gate MC12B on the data card becomes true. (MC12B functions as a negative logic "nor" gate.) The true output of MC12B causes the contents of the input register on the data card to be gated into the data shift register. This word, previously received from the DMA system, will be the first word written on the drum. Also, the WP and Flag FFs are set.

4-71.   When the Flag FF is set, it forwards a true SRQ signal to the DMA system. DMA responds by placing the next word on the IOBO lines, and by generating CLF, IOO, IOGE(B), SCM, and SCL signals. The SCM and SCL signals address the data card. The CLF signal, gated by "nand" gate MC15A, resets the Flag FF. The IOO signal, gated by "nand" gate MC15D, transfers the new word from the IOBO lines into the input register on the data card.

4-72.   Returning to the Run FF, when it becomes set it furnishes a true input to "nand" gate MC13C. One of the other inputs to the gate is received from the set-side output of the DI FF. This flip-flop is in the set condition when writing takes place. The other input to MC13C is the "not" TP signal received from the data card. If track protection does not exist, "not" TP is true, and MC13C furnishes a false output. As a result, transistor Q1 conducts, and the "not" W signal changes from approximately +2.5 volts to approximately +0.3 volts. Writing on the drum then starts.

4-73.   The reset output of the Run FF is furnished to "nand" gate MC35A. As noted earlier, an LIA/B instruction which acquires the drum status word enables "nand" gate MC46B on the command card. This gate furnishes bit 0 of the status word. If the Run FF or Control Bit FF (or both) is set, bit 0 of the drum status word will be 1, indicating that the drum is busy.

4-74.   Write Control Operations. Figure 4-6 illustrates the signals which control drum writing and reading. Included in the illustration are bit values for typical data words. At the beginning of each sector, the word counter and bit counter are cleared by the second "not" SC pulse. When a "not" W signal from the command card initiates a
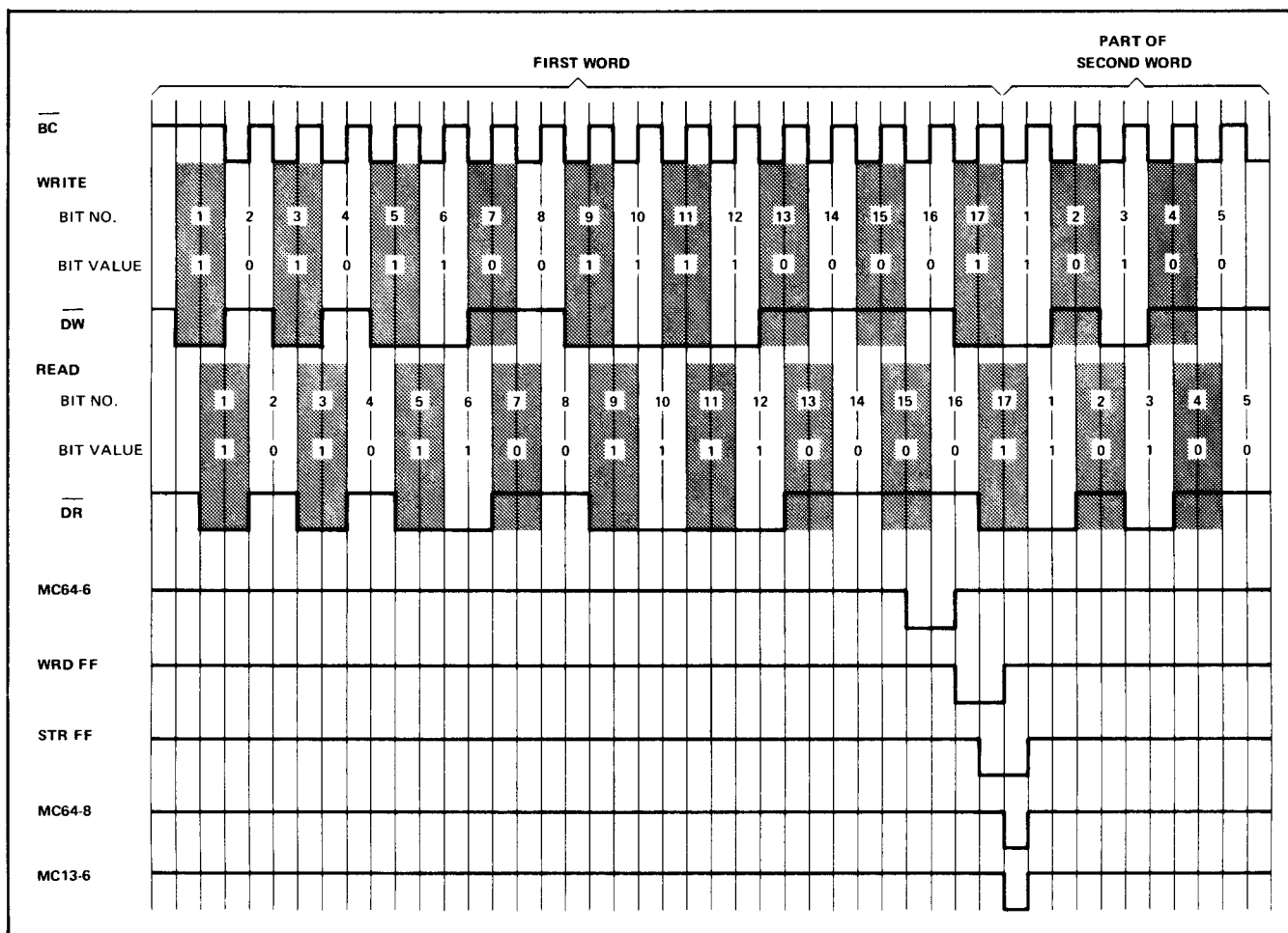
Figure 4-6. Write and Read Control, Timing Chart

drum write operation, "not" BC pulses start. The leading (negative-going) edge of each of these steps the bit counter on the command card, indicating that a bit has been written on the drum. At the leading edge of the 15th pulse all positions at the bit counter contain logic 1, and "nand" gate MC64A is enabled. (The "nand" gate output is identified in figure 4-6 by its output pin, MC64-6.) With the "nand" gate output negative, the leading edge of the next (16th) "not" BC pulse (inverted) resets the WRD FF, indicating that 16 data bits have been transferred. Also, the 16th "not" BC pulse clears the bit counter. With the WRD FF reset, the STR FF is reset by the trailing (positive-going) edge of the 16th "not" BC pulse. Then, at the leading edge of the 17th "not" BC pulse, the WRD FF is again set.

4-75.   The leading edge of the 17th pulse also attempts to set FF B0 of the bit counter. However, because of the circuit delay in setting the WRD FF, and delay in MC55B and MC54E, the reset condition of the WRD FF holds B0 in the reset state. (MC55B functions as a negative-logic "not" gate.) With the WRD FF set and the STR FF reset, coincidence occurs for "nand" gate MC64B on the command card. (The output of this gate is identified in figure 4-6 as MC64-8. Also shown in the illustration is MC13-6, the corresponding gate-output for read operations.) The false output of MC64B is forwarded to pin

*S on the data card as the "not" EWW signal. At this time, the input to pin *T on the data card is true because the DI flip-flop is set, and the input to pin *U on the data card is false because "nand" gate MC25B on the command card is not enabled due to the reset condition of the SCP FF. (Refer to figure 4-2.) On the data card, "nand" gate MC22A is disabled by the false input to pin *U of the card. The input to pins 12 and 13 of "nand" gate MC12B on the data card therefore is true.

4-76.   Returning to "nand" gate MC64B on the command card, its output, furnished to pin *S of the data card, is true until the WRD FF is set at the end of a word. Then, while the STR FF remains in the reset condition, the input to pin *S of the data card is false.

4-77.   Coincidence no longer exists for "nand" gate MC12B on the data card, and its output becomes true. This true output gates the contents of the input register into the data shift register. At the same time, the WP and Flag FFs on the data card are set. The Flag FF sends an SRQ signal to the DMA system indicating that the second word is required for the input register on the data card. When the word is supplied, SCM, SCL, IOGE(B), and IOO signals from the DMA system gate the word into the input register on the data card, and a CLF signal from DMA resets the Flag FF.

4-78. Note that prior to the first word stored in each sector the actions described in the preceding paragraph are brought about by a true input to pin *U on the data card. For subsequent words in the sector, the same actions are brought about by a false input to pin *S.

4-79. When the WRD FF is set near the end of the first word, the positive-going edge of the 17th "not" BC pulse sets the STR FF. At this time, the word counter is advanced by binary 1, to indicate that the first word of the sector has been recorded on the drum.

4-80. The procedures described for the second word are repeated for each subsequent word in the sector. After the 64th word of the sector has been written, FF WD5 on the command card is cleared, setting the EOS FF. Inverter MC24A on the command card then prevents the enabling of "nand" gate MC64B, and thereby prevents the Flag FF from requesting a word from the DMA system.

4-81. When the WRD FF is set at the end of the 64th word, "nand" gate MC13A is enabled, and the Run FF is reset. With the Run FF cleared, the "not" W output furnished to the drum becomes true, and writing ceases. (See "not" W signal in figure 4-1.)

4-82. Operations now await the second "not" SC pulse of the new sector. This pulse strobes "nand" gates MC34E and MC33E on the command card, resetting the EOS flip-flop and ensuring that the WD5-0 flip-flops are also in the reset condition. "Nand" gate MC35C ensures that the STR and WRD FFs are in the set condition, and "nand" gate MC55B ensures that the bit counter is in the reset condition. (MC55B functions as a negative-logic "nor" gate.)

4-83. If writing is to be continued in the next sector, the Sector Address Coincidence FF remains set between the two sectors. As a result, when the second "not" SC pulse of the new sector occurs, "nand" gate MC25B sets the Run FF. Operations then proceed as with the previous sector, and are continued until the operation is completed in the normal manner or aborted. Termination proceedings are described later in this section.

4-84. Data Transfer to Drum. When writing takes place, each 16-bit word in the data shift register is transferred in serial form to the drum, low-order bit first. After the 16 data bits have been transferred, a parity bit is furnished as the 17th bit. The track in which writing takes place is specified by the TA9-0 bits from the data card; these bits select the appropriate read/write head.

4-85. As stated earlier, when the writing of each word takes place the drum furnishes to the command card 17 "not" BC pulses, each indicating that a bit has been written on drum and a new bit is required. After 17 pulses have been furnished, an additional 17 are furnished for the second word, and so on. The pulses are provided in a continuous train without pauses between words. However, the pulses are not furnished between sectors. Thus 1088 pulses are generated for every sector written (17 pulses for each of 64 words).

4-86. At the start of every drum sector while writing, before the first "not" BC pulse, the "not" DW output from the data card is sampled by the drum. This output is taken from the reset side of FF D0. Since the WRD FF is in the set condition during the writing of the 16 data bits, "nand" gate MC13C on the data card is disabled, its output is true, and "nand" gate MC16C is enabled, allowing the reset output of FF D0 to be forwarded to the drum.

4-87. After sampling the bit on the "not" DW line, the drum writes the bit in the first bit position of the sector, then starts furnishing the "not" BC pulses to the data card. The negative-going edge of each pulse is inverted, and shifts the word in the data shift register one position toward the low-order end of the register. Thus, after each shift a new bit is supplied to the "not" DW line. This bit is written on the drum, and another register shift takes place. Because data is taken from the reset side of FF D0, it is furnished to the drum in 1's complement form. The process continues until all 16 data bits have been transferred to the drum. Figure 4-6 shows the timing relationships.

4-88. As each data bit is shifted out of the D0 FF, the output rank of the WP FF is toggled if the bit is a binary 1. At the start of each word the WP FF is in the set condition. After 16 data bits have been transferred to the drum, the WP FF will be in the set state if there was an even number of 1's in the 16-bit word, or in the reset state if there was an odd number of 1's. Consequently, the output of this flip-flop will be in the required state for furnishing the parity bit. (Odd parity is used.)

4-89. On the command card, the WRD FF is reset by the negative-going edge of the 16th "not" BC pulse. As a result, "nand" gate MC13C on the data card is enabled, and the parity bit in the WP FF is forwarded to "and" gate MC16C. At this time, the D0 FF contains a binary 0, and its reset output serves as an enable for MC16C. (The binary 0 in D0 was shifted down the register from FF D16, which was reset before shifting started.) MC13C inverts the parity bit to change it to the required 1's complement form, and MC16C forwards the bit to the drum.

4-90. While the parity bit is being sent to the drum, a new word is gated into the data shift register from the input register. Then, when the negative-going edge of the 17th "not" BC pulse indicates that the parity bit has been written, the WRD FF is set. As a result, "and" gate MC16C on the data card is again ready to forward data from FF D0 to the drum. The write operation continues without interruption, with the first bit of the new word being recorded on the drum immediately after the parity bit of the preceding word.

4-91. Words continue to be transferred to the drum until the end of the first sector is reached. If additional sectors are to be written, the procedure described is repeated for

each sector. The Run FF is set and reset, respectively, at the beginning and end of each sector. However, the Sector Address Coincidence FF remains set until the operation is completed or aborted.

4-92.   Incomplete Sector. If the number of words to be written is not a multiple of 64, the last sector will not be completely filled. When an operation of this type takes place, the DMA system supplies the data card with a CLC signal after it has furnished the last word. This signal resets the Control Bit FF, which in turn resets the Sector Address Coincidence FF. However, the Run FF remains set until the end of the sector. As a result, the "not" W signal remains false and writing continues. However, the data card no longer receives SCM, SCL, IOGE(B), or IOO signals from DMA. Therefore, the contents of the input register remain unchanged. These contents will be the last word written on the drum. Each word-time for the remainder of the last sector, the contents of the input register will be gated into the data shift register and transferred to the drum as the word to be written. Thus, the last word will be repeated on the drum until the end of the sector is reached. The Run FF is then reset, the "not" W signal becomes true, and the operation ceases. Until the Run FF is reset at the end of the sector, bit 0 of the drum status word is logic 1. (As noted earlier, if either the Control Bit FF or the Run FF is set, bit 0 of the status word is logic 1.)

4-93.   Track Protection. When track protect switch S1 on the data card is closed (in the down position), no tracks are protected against writing. In this nonprotect situation the "not" TP signal is true, and "nand" gate MC13C on the command card is enabled. If the track protect switch is open, the "not" TP signal is false if the track address register contains the 1's complement of an address for a protected track.

4-94.   To clarify the functioning of the track protect circuits, assume first that all tracks are protected. To bring this about, diodes CR1 through CR10 are all removed from the data card. (Refer to table 2-1.) Now, when the track protect switch is open, the "not" TP input pin on the command card (pin *16) faces an open input. Since resistor MC66R2 is connected to – 2 volts, "nand" gate MC13C on the command card is disabled. Consequently no writing can take place. If the track protect switch is then closed, the gate is enabled, writing can take place on any track, and no track protection exists.

4-95.   Assume, now, that diodes CR1 through CR10 are all in place on the data card. As shown in table 2-1, track 00 (octal) is then protected when switch S1 is open. The 10 diodes, together with resistor MC66R2 on the command card, constitute a negative-logic "and" gate. Diode CR11 constitutes an 11th input to the gate when S1 is closed. If all inputs to the gate are false, the output of the gate is false. With S1 open, the "not" TP signal is false only when all flip-flops in the track address register are set. Since the register contains the 1's complement of the track address, track 00 (octal) is protected. However, if one or more of the flip-flops is in the reset condition, "and" gate coincidence does not exist, the "not" TP signal is true, and writing can be conducted. This condition exists when the track address is other than 00.

4-96.   To further illustrate the functioning of the track protect circuits, assume that diode CR1 has been removed. The "and" gate now has nine inputs (not counting CR11), and the low-order flip-flop of the track address register is not examined when determining track protect status. Track protection exists when the "not" TA9 through "not" TA1 FFs are all in the set state; "not" TA0 can be either reset or set. This condition occurs when the track address is 00 or 01 (octal).

4-97.   As additional diodes are removed, additional tracks are brought into protect status when S1 is open. The track addresses corresponding to the diodes removed are not examined when the circuits determine protect status. These tracks are simply given protect status at all times, provided switch S1 is open.

4-98.   Abort Store FF. The STC instruction which initiates a write operation resets the Abort Store FF on the command card. Then, if certain fault conditions exist during all or part of the write operation, the "not" RY signal from the drum becomes true and the flip-flop is placed in the set condition. After the completion of writing, the state of the flip-flop can be checked by an LIA/B instruction. If the flip-flop is set, bit 3 of the drum status word will be logic 1, indicating that the write operation possibly was not performed successfully. The conditions which result in setting the Abort Store FF are the following:

a. Low drum speed.

b. HEADS switch not at the IN position.

c. The drum circuits which supply the "not" RY signal are defective.

d. Drum memory not connected to the computer.

e. Drum memory not connected to the drum memory power supply.

f. Low line voltage or no line voltage applied to the drum memory power supply.

g. Drum memory power supply defective or not turned on.

4-99.   TERMINATION OF WRITING.

4-100.   General. Drum writing can be terminated in two ways: by permitting all words to be transferred to the drum, or by an abort of the write operation before its completion. In the first method, the operation is terminated by the DMA system without intervention by the computer program. In the second method the operation is terminated by a programmed abort or by an automatic abort brought about by equipment failure.

4-101. Termination by DMA System. When the DMA system terminates drum writing, it issues a CLC signal to the data card after forwarding the last word to the input register on the card. The signal resets the Flag FF (if the CLF signal failed to reset it) and the Control Bit FF. The Sector Address Coincidence FF on the command card is cleared by the false CB signal produced when the Control Bit FF is reset. The Run FF is reset at the end of the current sector, when the EOS FF on the command card is set. If the number of words supplied by the DMA system is not sufficient to fill the last sector, the last word furnished is repeated in each word location in the track until the end of the sector is reached. After being reset, the Run FF is not set again at the start of the new sector, as is done when writing continues. Therefore, the "not" W signal remains true and the bit on the "not" DW line is not written on the drum at the start of the next sector.

4-102. When the "not" W signal becomes true, the "not" BC signal is no longer furnished by the drum, and the bit counter and word counter cease running. These counters are cleared at the end of the last sector written, and remain cleared until another drum write or read operation is initiated. Also, after the end of the last sector written, the WRD and STR FFs remain in the set condition. Because STR remains set, "nand" gate MC64B on the command card does not experience coincidence, and "nand" gate MC12B on the data card experiences continued coincidence. Consequently, the Flag FF on the data card remains reset and SRQ signals are no longer sent to the DMA system.

4-103. Termination by Abort. It has been noted that a write operation can be aborted in two ways: either by a programmed instruction or by the occurrence of certain faults in the drum memory or drum memory power supply.

4-104. When a programmed abort occurs, the computer performs a CLC instruction with the I/O select code of the data card. The computer furnishes a true CLC signal to pin 21 of the data card, producing the same results as the CLC signal supplied by the DMA system for normal termination.

4-105. The equipment-fault termination is brought about by the "not" RY signal becoming positive during the drum write operation. This resets the Sector Address Coincidence FF on the command card and sets the Abort Store FF. At the end of the sector, the Run FF is reset in the normal manner, but because the Sector Address Coincidence FF is reset, the Run FF is not set again at the start of the next sector. As a result, the "not" W signal remains true, and at the start of the next sector the bit on the "not" DW line is not written on the drum and the "not" BC signal is not supplied. Without "not" BC pulses, the bit counter and word counter remain in the clear condition and the WRD and STR FFs remain in the set condition. Because the STR FF remains set, the Flag FF on the data card remains reset and SRQ signals are no longer sent to the DMA system.

4-106. If a write operation is aborted because the "not" RY signal becomes true, the DMA channel concerned becomes locked up. The word count maintained by the DMA system indicates that additional words must be supplied to the drum, but because DMA no longer receives true SRQ signals from the drum data card, it does not furnish the required words. A programmed check of the DMA channel, using an SFS or SFC instruction with the DMA channel I/O select code, will indicate that the DMA channel is busy. Furthermore, a check of the drum busy bit (bit 0 of the drum status word) will indicate that the drum is busy. The situation continues until the Flag FF on the DMA control card, and the Control Bit FF on the drum data channel interface card, are reset. These two flip-flops can be cleared by performing one of the following:

a. Start a new drum read or write operation on the DMA channel concerned, using the normal drum initiation instructions.

b. Clear the DMA Flag FF by performing a CLF instruction with the DMA channel I/O select code. Also, clear the drum Control Bit FF by performing a CLC instruction with the drum data card I/O select code.

c. Reset the entire I/O system by generating a CRS signal in any of the following ways:

(1) With the computer stopped, press the PRESET switch.

(2) Turn off computer power by means of the POWER switch, then restore power.

(3) Program a CLC instruction, using zero as the I/O select code.

4-107. Existence of DMA lockup resulting from a fault in the drum memory or drum memory power supply is indicated by bit 3 of the drum status word. If this bit is 1 after sufficient time has been allowed for completion of the data transfer, the "not" RY signal was true during the transfer, the data transfer was probably not completed and the DMA channel and drum must be cleared by one of the methods listed in the preceding paragraph. Another method of checking for the existence of the lockup condition is to perform an LIA/B instruction using the DMA channel I/O select code. This instruction places in positions 13-0 of the computer A or B register the number in the DMA word count register. (This register is on the DMA register card.) Bit 0 in the computer A or B register will contain the low-order bit of the word count. If sufficient time has been allowed for completion of the transfer, the word count should be zero.

4-108. POST—WRITE STATE. After termination of writing, either by DMA or by a programmed CLC instruction, flip-flops and registers on the drum interface cards will be in the condition listed below. The state of flip-flops and registers not listed depends on prior operations. (If an operation is terminated before the end of a sector, the bit counter and word counter remain running

and the Run FF remains set until the end of the sector is reached. Also, the RP FF is reset then set, at the end of each remaining word in the sector.)

a. The Control Bit FF is reset.

b. The Flag FF is reset.

c. The Run FF is reset.

d. The Sector Address Coincidence FF is reset.

e. The sector counter contains the address of the next drum sector, and is running.

f. The sector select register contains the address of the next sector, and is running.

g. The word counter is reset and not running.

h. The EOS FF is reset.

i. The bit counter is reset and not running.

j. The STR FF is set.

k. The WRD FF is set.

l. The RP FF is set.

m. The DI FF is set.

4-109.   READ OPERATIONS.

4-110.   Drum read operations are very similar to drum write operations. Therefore, only the principal functions of reading are presented, together with detailed discussion of the operations unique to the read process.

4-111.   When reading is to be performed, the DMA system and drum memory are initialized in the same manner as the writing. First, an OTA/B instruction with the command card I/O select code forwards a CW4 word to the command card and data card. This word indicates that reading will take place, and designates the starting track and sector. The track address register and sector address register are loaded in the same manner as for writing. However, bit 15 of CW4 is logic 0 when reading is to be performed, resulting in the DI flip-flop being placed in the reset condition.

4-112.   After the OTA/B instruction, an STC instruction starts the drum read operation.

4-113.   Sector coincidence occurs in the same manner as for writing. However, the Read Inhibit FF ensures that at least a full sector elapses between the occurrence of sector coincidence and the setting of the Sector Address Coincidence FF. Referring to figure 4-5, the MC25-13 input to the MC25A "nand" gate is shown as becoming true at the trailing edge of the second "not" SC pulse. This will occur if coincidence did not exist when the sector address register was loaded. However, if coincidence does exist when the register is loaded, MC25A will furnish a false

output as soon as the next "not" SC pulse occurs. This could happen almost immediately if the sector address register is loaded near the end of a sector. The situation is not a problem with writing, but it creates a difficulty when reading because circuits in the drum require greater settling time for reading. Therefore, the Read Inhibit FF prevents the setting of the Sector Address Coincidence FF until the Read Inhibit FF is reset. While it is set, the Read Inhibit FF furnishes a true input to pin 5 of "nand" gate MC35B. The resulting false input to pin 4 of "nand" gate MC23A keeps pin 6 of MC23A false. Then, if an attempt is made to set the Sector Address Coincidence FF by the first "not" SC pulse after the sector address register is loaded, the Sector Address Coincidence FF furnishes true outputs from both the set and reset sides. Then, when the output of "nand" gate MC25A again becomes true, the Sector Address Coincidence FF remains reset. Consequently, at the second "not" SC pulse after address coincidence, the Run FF cannot be set. However, the second "not" SC pulse encountered does reset the Read Inhibit FF. After this point, sector coincidence will be effective in setting the Sector Address Coincidence FF.

4-114.   When the run flip-flop is set, the command card sends a false "not" R signal to the drum, rather than a "not" W signal as is done for writing. This difference is brought about by the reset condition of the DI flip-flop.

4-115.   Upon receipt of the false "not" R signal, the drum commences to read data from the track indicated by the TA9-0 outputs from the data card. Also, "not" BC pulses are furnished to the data card (refer to figure 4-6).

4-116.   The data read from the drum is furnished to the data card as the "not" DR signal. This signal is inverted by inverter MC42B, converting the 1's complement data which was furnished to the drum back to uncomplemented form. In each word the data is received low-order bit first, and the parity bit is received last.

4-117.   As it arrives from the drum, each bit is inserted to change it to uncomplemented form. The negative-going edge of the pulse applied to pin 3 of the D16 FF then clocks the bit into the input rank of the D16 FF. The bit thus is acquired from the drum at the trailing (positive-going) edge of a "not" BC pulse. At the leading edge of the next "not" BC pulse, the bit is transferred to the output rank of the D16 FF. Then, the trailing edge of the "not" BC pulse transfers the bit to the input rank of the D15 FF, while at the same time a new bit is clocked into the input rank of the D16 FF. This process continues for each bit of the word.

4-118.   When the bit counter indicates that 16 bits have been received, the WRD FF is reset, then set again at the start of the 17th bit. When the 17th (parity) bit has been placed in the D16 FF on the data card, the STR FF is reset, and "nand" gate MC13B on the command card experiences coincidence. The output of this gate is forwarded to the data card as the "not" EWR signal, where it sets the Flag FF and gates the contents of FFs D15-0 into the output register.

4-119.   Setting the Flag FF sends a true SRQ signal to the DMA system, indicating that a word is waiting in the output register. When it is ready to acquire the word, the DMA system furnishes IOI, IOGE(B), SCM, and SCL signals to the data card. These gate the contents of the output register onto the IOBI 15-0 lines, and the word is acquired by the DMA system.

4-120.   Subsequent words read from the drum are treated in the same manner as the first word. Between each sector the Run FF is clear, the "not" R signal is true, and "not" BC pulses are no longer furnished by the drum. Then, at the start of each new sector, the Run FF is set, the "not" R signal becomes false, and "not" BC pulses are furnished. In each sector 1088 bits are written (64 17-bit words), and the drum furnishes 1088 "not" BC pulses.

4-121.   As the bits in each word are received, they are inverted by inverter MC42B on the data card and forwarded to the command card. There, if a bit is a binary 0, the RP FF is toggled by the leading edge of the associated "not" BC pulse. The RP FF is set at the start of each sector by a false input to pin 13 of MC44A. Then, if the parity of each word is correct, the RP FF is toggled an even number of times during the word. (Since parity is odd, there is an even number of binary 0's in each 17-bit word.) At the start of a read operation, the STC instruction which initiates the transfer of data clears the RPE FF. Then, at the end of each word read, the RPE FF samples the reset-side output of the RP FF. If a parity error occurred in the word, the RP FF will be in the reset state at the end of the word, and the RPE FF becomes set. Thereafter, the RPE FF remains set and the RP FF plays no further part in the operation. If a parity error occurs in a second word, the RPE FF is not reset because it is held in the set condition by the false input furnished to its pin 10 by its own pin 8. When reading is completed, an LIA/B instruction can acquire the drum status word, and bit 1 of the word can be examined to determine whether a parity error occurred. (See table 3-2.)

4-122.   The RPE FF is reset the next time an STC instruction initiates a drum operation. When this occurs, a false input is applied to pin 13 of the RPE FF, making the output from pin 8 true. With pin 8 true, the input to pin 10 is no longer effective in holding the flip-flop set, and it becomes reset.

4-123.   The drum read operation can be terminated either by reading all words scheduled, or the operation can be aborted. Termination procedures are the same as for drum writing. After termination, flip-flops and registers on the drum interface cards will be in the same condition as when writing is terminated, except that the DI FF is in the reset state.

4-124.   As in drum writing, a true condition of the "not" RY signal sets the Abort Store FF. After completion of the read operation, an LIA/B instruction allows examination of the state of the flip-flop.

4-125.   LIA/B INSTRUCTION.

4-126.   Functions of the LIA/B instruction have been dealt with in appropriate places when discussing drum writing and reading. Operation of the instruction as a whole, as it pertains to the drum interface cards, will now be presented.

4-127.   When an LIA/B instruction using the command card I/O select code is decoded, the appropriate SCM and SCL signals become true at T2. (See figure 4-7.) Then, when IOGE(B) and IOI become true, "and" gate MC36A on the command card experiences coincidence. The output of this gate is furnished to other "and" gates which forward the various bits of the drum status word to the IOBI lines. At T5TS, these bits are placed in the computer A or B register.
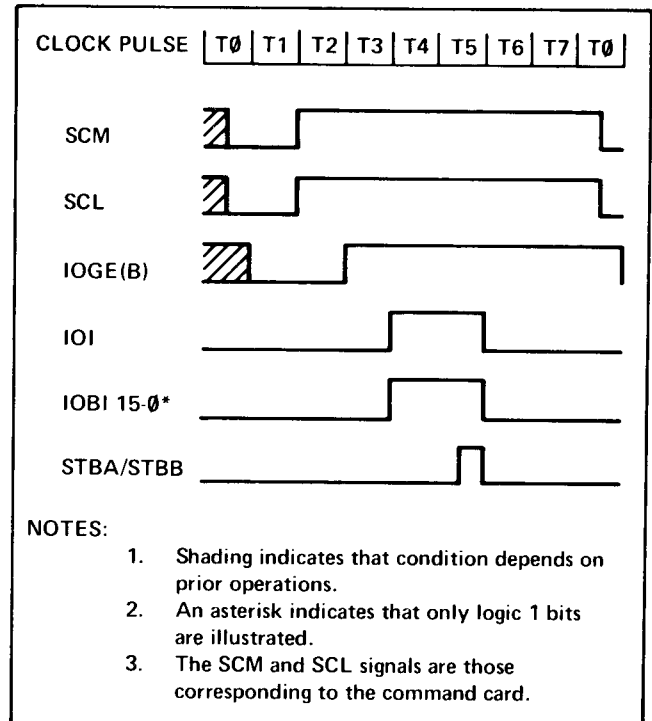

Figure 4-7.   LIA/B Instruction and Resulting Drum
System Operations, Timing Chart

4-128.   Table 3-2 describes the significance of the various parts of the status word.

SECTION V

MAINTENANCE

5-1.   INTRODUCTION.

5-2.   This section contains maintenance information for the 12610B Drum Memory Interface Kit. Included are preventive maintenance instructions, corrective maintenance instructions, and maintenance data consisting of a table of interface card connections, information pertaining to integrated circuit characteristics and connections, reference designation indexes, part location views, and schematic diagrams.

5-3.   PREVENTIVE MAINTENANCE.

5-4.   Preventive maintenance for the drum memory interface kit is conducted by running the entire drum diagnostic program once each month. At least three passes through the read/write portion of the program must be made, using the worst-case test word: 1100110011001100CC.

5-5.   As well as testing the drum memory interface, the diagnostic program also checks the operation of the drum memory and the drum memory power supply. Instructions for running the diagnostic program are contained in the manual supplement attached to the back of this manual.

5-6.   CORRECTIVE MAINTENANCE.

5-7.   GENERAL.

5-8.   When performing troubleshooting, refer to figures 5-1 through 5-5 and tables 5-1 through 5-5 in this section, and to figures 4-1 through 4-7 in section IV.

5-9.   INTERCONNECTIONS.

5-10.   For connections to the 86-pin connector on each interface card, refer to the computer backplane wiring list. For connections to the 48-pin connector on each card, refer to the schematic.

5-11.   SIGNAL VOLTAGES.

5-12.   The voltage levels of signals received from the drum are as follows: logic 1 is +5.1 to +2.4V (+3.5V nominal), logic 0 is +0.4 to +0.0V (+0.2V nominal).

5-13.   For voltage levels of signals received from the computer, refer to computer documentation.

5-14.   To determine the input voltages, output voltages, and circuit delay of integrated circuits on the drum interface cards, first locate the integrated circuit in figure 5-1 then refer to the appropriate characteristic in table 5-1. The nominal levels for all integrated circuit inputs and outputs are +3.5V and +0.2V.
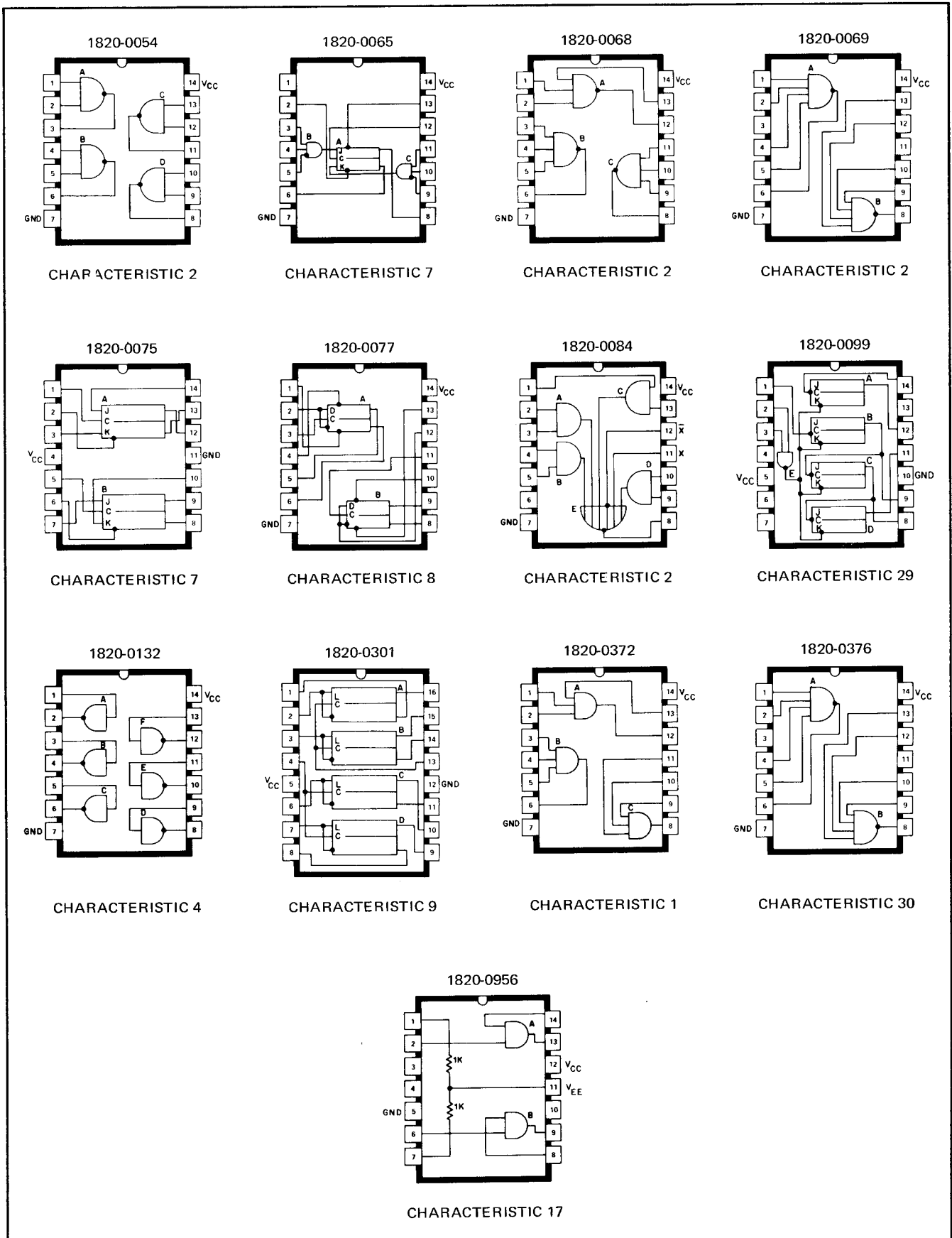
Figure 5-1. Integrated Circuit Pin Connections

Table 5-1. Integrated Circuit Input Levels, Output Levels, and Delay Times

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO 1 (NANOSEC)	TO 0 (NANOSEC)
1	+2.0	+0.8	+2.4	+0.4	Logic 1	15	15
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
4	+1.9	+0.8	+2.4	+0.45	Logic 1	15	13
7	+2.0	+0.8	+2.4	+0.4	Logic 1	50	50
8	+2.0	+0.8	+2.4	+0.4	Logic 1	35	50
9	+2.0	+0.8	+2.4	+0.4	Logic 1	40	25
17	+1.25	+0.5	+2.25	-0.36	Logic 0	18	18
29	+2.0*	+0.8†	+2.4	+0.4	Logic 1	135	135
30	+2.0	+0.8	+2.4	+0.4	Logic 1	10	10

NOTES:

* +2.2V for pin 1

† +0.6V for pin 1

Table 5-2.   Data Channel Interface Card (12610-6001), Reference Designation Index

| REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru C50	0160-2055	Capacitor, Fxd, Cer, 0.01 uf, +80 –20%, 100 VDCW	28480	0160-2055
CR1 thru CR10	1901-0040	Diode, Si, 30 mA	07263	FDG1088
CR11	1901-0460	Diode, Si, 3-Junction Stabistor	03508	STB523
MC12,14	1820-0376	Integrated Circuit, TTL	01295	SN4484
MC13	1820-0068	Integrated Circuit, TTL	56289	USN7410A
MC15,22,33,53,63,73,83,93,103	1820-0054	Integrated Circuit, TTL	01295	SN4342
MC16	1820-0372	Integrated Circuit, TTL	01295	SN4342
MC23,25	1820-0069	Integrated Circuit, TTL	56289	USN7420A
MC24	1820-0065	Integrated Circuit, TTL	01295	SN4352
MC26,36,46,56,66,76,86,96,106	1820-0956	Integrated Circuit, CTL	07263	SL3459
MC34,43,44,54,62,64,72,74,82, 84,92,94,102,104	1820-0077	Integrated Circuit, TTL	01295	SN4354
MC35,45,55,65,75,85,95,105	1820-0301	Integrated Circuit, TTL	01295	SN4463
MC42,52	1820-0132	Integrated Circuit, TTL	07263	U6A901659X
R1 thru R4,7	0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w	01121	CB1025
R5,6	0683-2715	Resistor, Fxd, Comp, 270 ohms, 5%, 1/4w	01121	CB2715
S1	3101-0932	Switch, Slide, DPDT, 0.5A, 125V, AC/DC	79727	GG350-0001
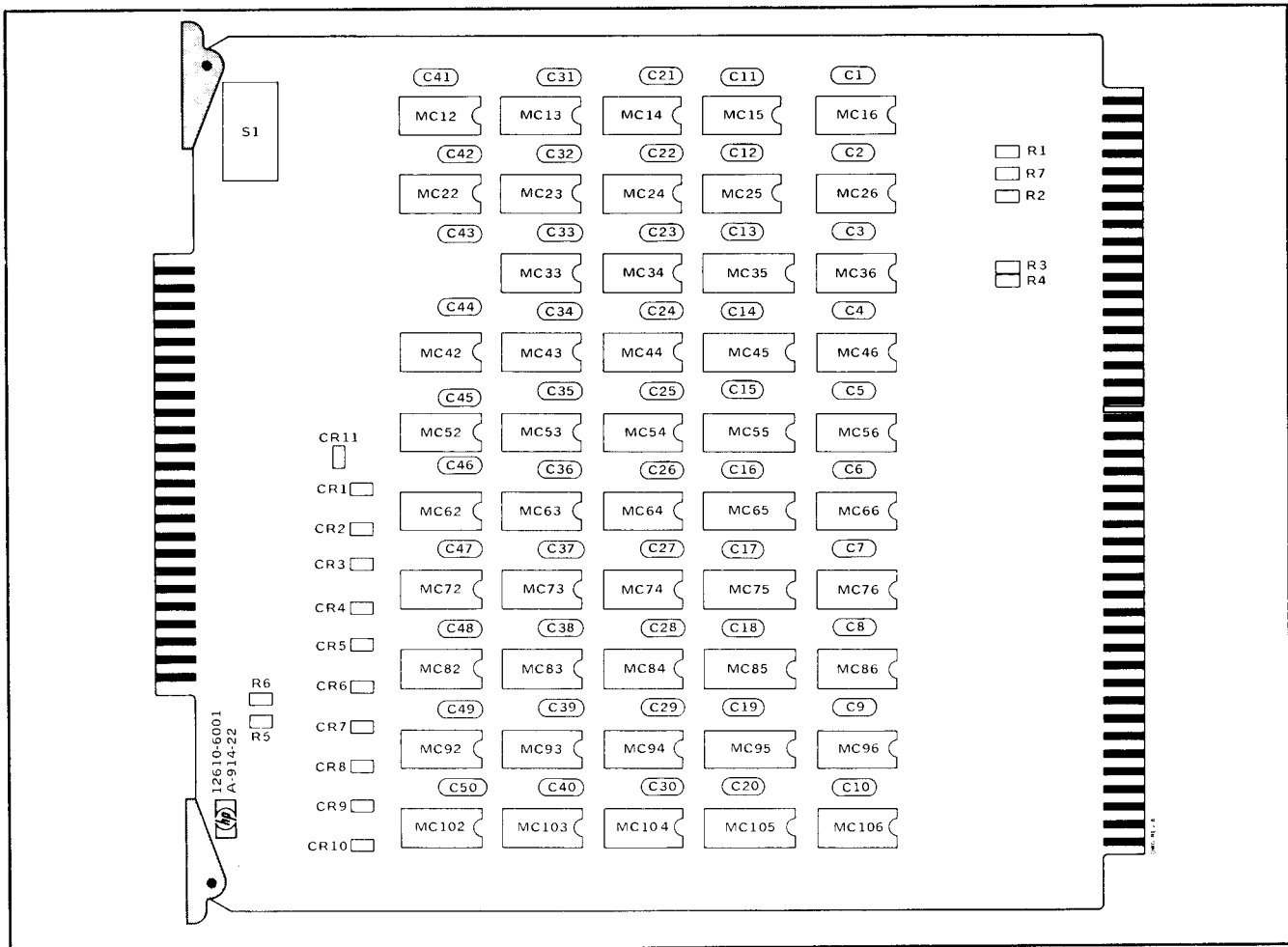
Figure 5-2.   Data Channel Interface Card (12610-6001), Part Location Diagram

Table 5-3. Data Channel Interface Card, 48-Pin Connector Signals

SIGNAL	DATA CARD PIN		CONNECTED TO:	
	SIGNAL	GROUND	SIGNAL	GROUND
$\overline{\text{ATR}}$ ("not" advance track register)	DAT-*V	—	CMD-*V	—
BC (bit clock)	DAT-*R	—	CMD-*R	—
CB (Control Bit FF)	DAT-*W	—	CMD-*W	—
$\overline{\text{CCB}}$ ("not" clear Control Bit FF)	DAT-*19	—	CMD-*19	—
$\overline{\text{CRA}}$ ("not" clear RPE and ABS FFs)	DAT-*13	—	CMD-*13	—
$\overline{\text{CRS}}$ ("not" control reset)	DAT-*Z	—	CMD-*Z	—
DI (Direction FF)	DAT-*T	—	CMD-*T	—
$\overline{\text{DI}}$ ("not" Direction FF)	DAT-*20	—	CMD-*20	—
DR (data read)	DAT-*21	—	CMD-*21	—
$\overline{\text{DR}}$ ("not" data read)	DAT-*23	DAT-*24	J1-N	J1-L
$\overline{\text{DW}}$ ("not" data write)	DAT-*AA	DAT-*BB	J1-D	J1-B
$\overline{\text{EWR}}$ ("not" end-of-word, read)	DAT-*15	—	CMD-*15	—
$\overline{\text{EWW}}$ ("not" end-of-word, write)	DAT-*S	—	CMD-*S	—
RFW (ready for first word)	DAT-*U	—	CMD-*U	—
STA (strobe track address)	DAT-*X	—	CMD-*X	—
TA0 (track address bit 0)	DAT-*1	DAT-*2	J1-v	J1-t
TA1 (track address bit 1)	DAT-*3	DAT-*2	J1-r	J1-n
TA2 (track address bit 2)	DAT-*4	DAT-*5	J1-k	J1-h
TA3 (track address bit 3)	DAT-*6	DAT-*5	J1-e	J1-c
TA4 (track address bit 4)	DAT-*7	DAT-*8	J1-a	J1-Y
TA5 (track address bit 5)	DAT-*A	DAT-*B	J1-W	J1-U
TA6 (track address bit 6)	DAT-*C	DAT-*B	J1-S	J1-P
TA7 (track address bit 7)	DAT-*D	DAT-*E	J1-M	J1-K
TA8 (track address bit 8)	DAT-*F	DAT-*E	J1-H	J1-E
TA9 (track address bit 9)	DAT-*H	DAT-*J	J1-C	J1-A
$\overline{\text{TP}}$ ("not" track protect)	DAT-*16	—	CMD-*16	—
$\overline{\text{WRD}}$ ("not" Word FF)	DAT-*P	—	CMD-*P	—

NOTES:

"DAT-*" identifies a pin in the 48-pin connector for the data channel interface card.

"CMD-*" identifies a pin in the 48-pin connector for the command channel interface card.

"J1-" identifies a pin in connector J1 on the drum memory.

A dash for a ground return indicates that the common ground return between cards is used (pins 1, 2, 85, and 86 of the 86-pin card connector). All signals transferred between the two interface cards use the common ground return. All signals transferred to or from drum use a separate ground return, with the ground lead and signal lead forming a twisted pair.

DATA CHANNEL INTERFACE CARD (12610-6001, REV 914)

Figure 5-3. Data Channel Interface Card (12610-6001), Schematic Diagram

Table 5-5. Command Channel Interface Card, 48-Pin Connector Signals

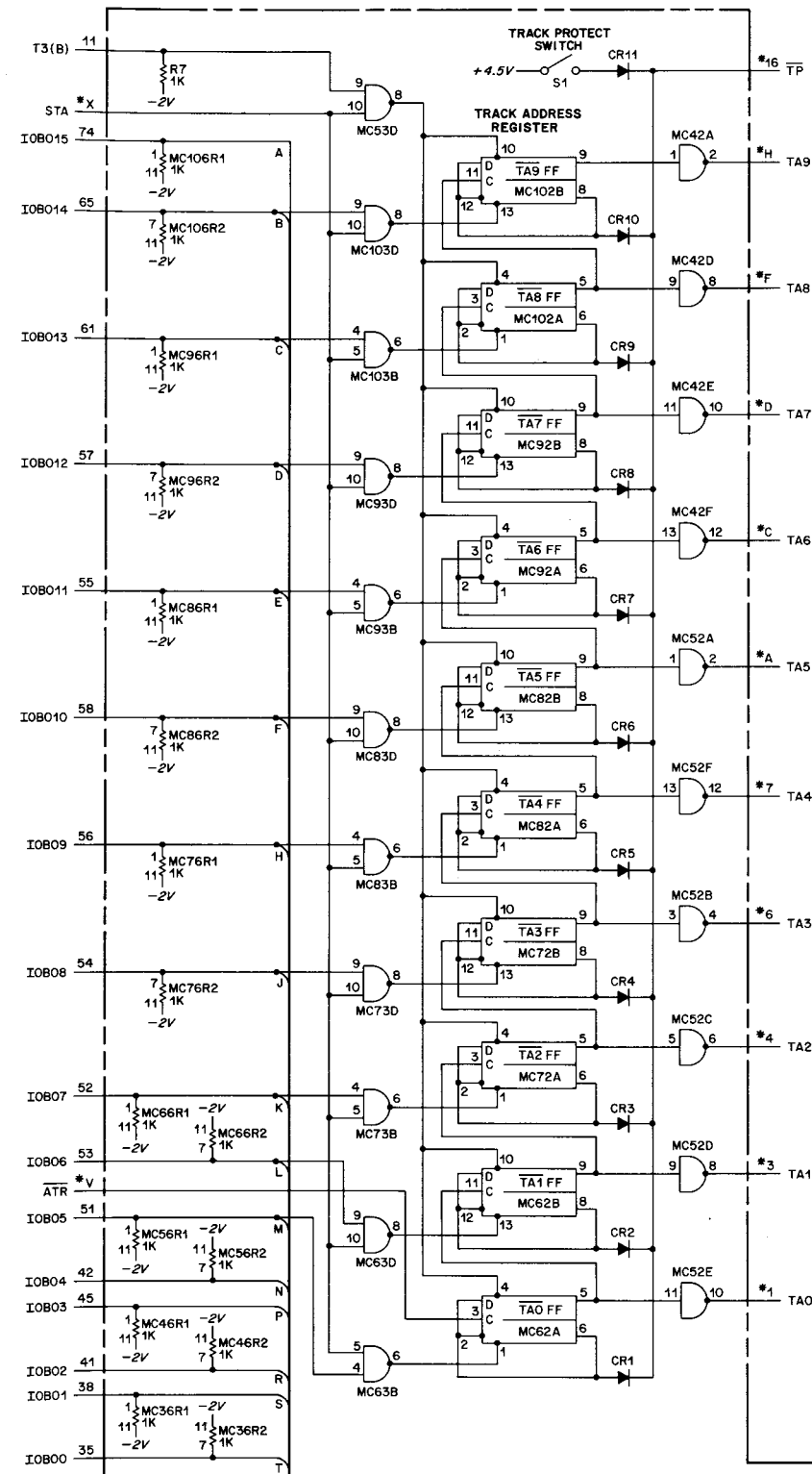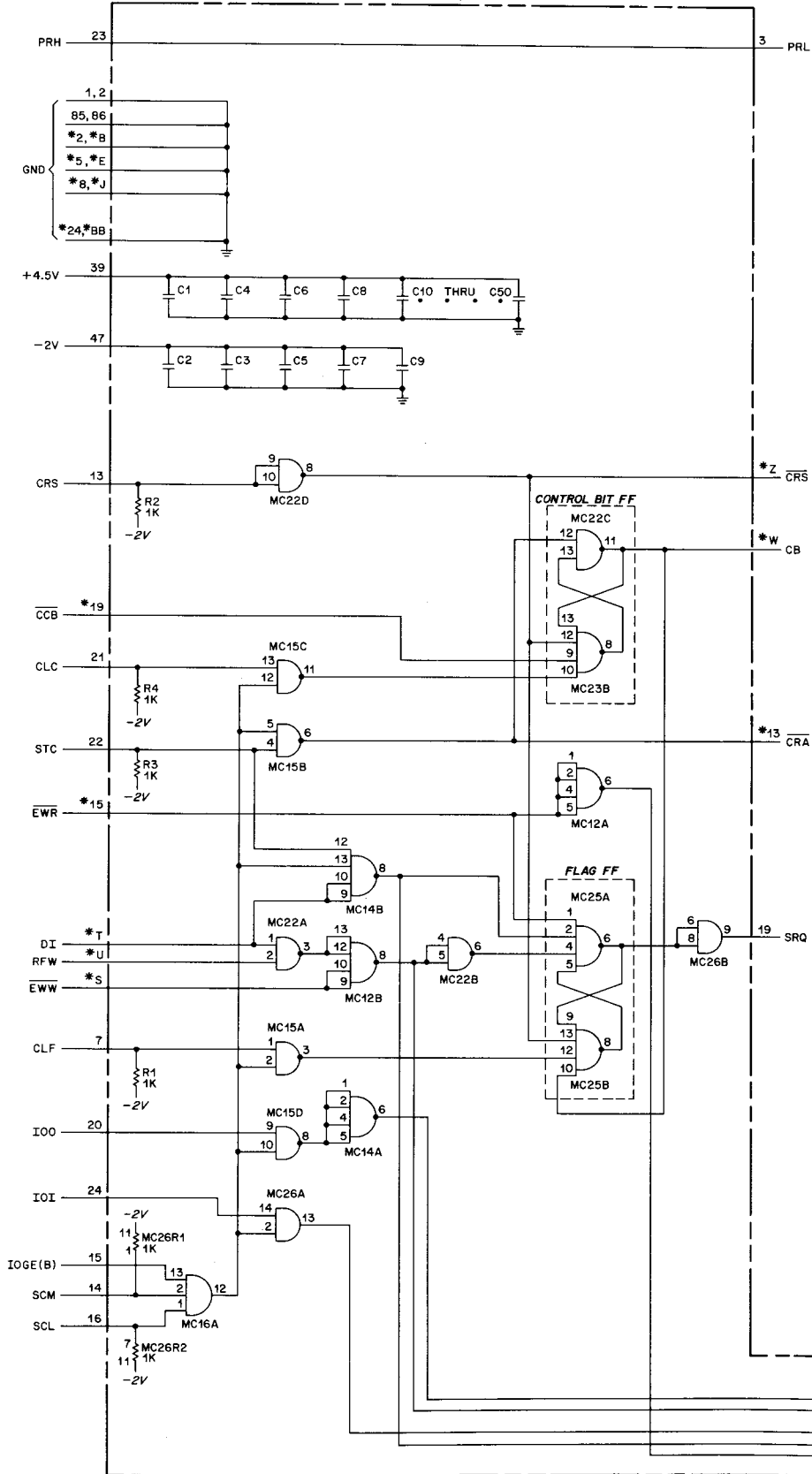| SIGNAL	COMMAND CARD PIN		CONNECTED TO:	
	SIGNAL	GROUND	SIGNAL	GROUND
$\overline{ATR}$ ("not" advance track register)	CMD-*V	—	DAT-*V	—
BC (bit clock)	CMD-*R	—	DAT-*R	—
$\overline{BC}$ ("not" bit clock)	CMD-*C	CMD-*B	J1-s	J1-p
CB (Control Bit FF)	CMD-*W	—	DAT-*W	—
$\overline{CCB}$ ("not" clear Control Bit FF)	CMD-*19	—	DAT-*19	—
$\overline{CRA}$ ("not" clear RPE and ABS FFs)	CMD-*13	—	DAT-*13	—
$\overline{CRS}$ ("not" control reset)	CMD-*Z	—	DAT-*Z	—
DI (Direction FF)	CMD-*T	—	DAT-*T	—
$\overline{DI}$ ("not" Direction FF)	CMD-*20	—	DAT-*20	—
DR (data read)	CMD-*21	—	DAT-*21	—
$\overline{EWR}$ ("not" end-of-word, read)	CMD-*15	—	DAT-*15	—
$\overline{EWW}$ ("not" end-of-word, write)	CMD-*S	—	DAT-*S	—
$\overline{R}$ ("not" read)	CMD-*4	CMD-*5	J1-EE	J1-HH
RFW (ready for first word)	CMD-*U	—	DAT-*U	—
$\overline{RY}$ ("not" drum ready)	CMD-*3	CMD-*2	J1-AA	J1-y
$\overline{SC}$ ("not" sector clock pulse)	CMD-*A	CMD-*B	J1-X	J1-V
STA (strobe track address)	CMD-*X	—	DAT-*X	—
$\overline{TO}$ ("not" track origin)	CMD-*1	CMD-*2	J1-f	J1-d
$\overline{TP}$ ("not" track protect)	CMD-*16	—	DAT-*16	—
$\overline{W}$ ("not" write)	CMD-*D	CMD-*E	J1-DD	J1-BB
$\overline{WRD}$ ("not" Word FF)	CMD-*P	—	DAT-*P	—

NOTES:

"DAT-*" identifies a pin in the 48-pin connector for the data channel interface card.

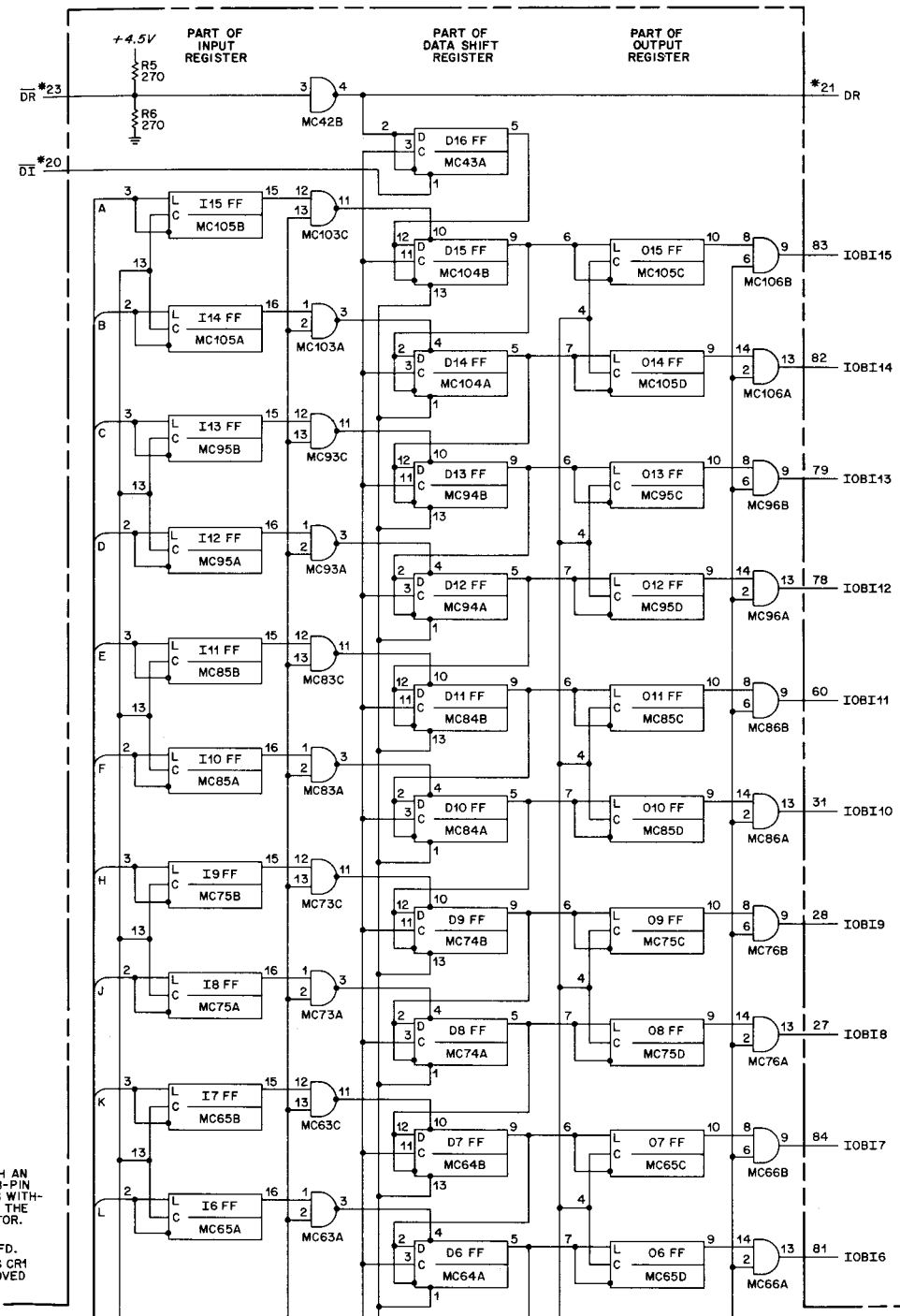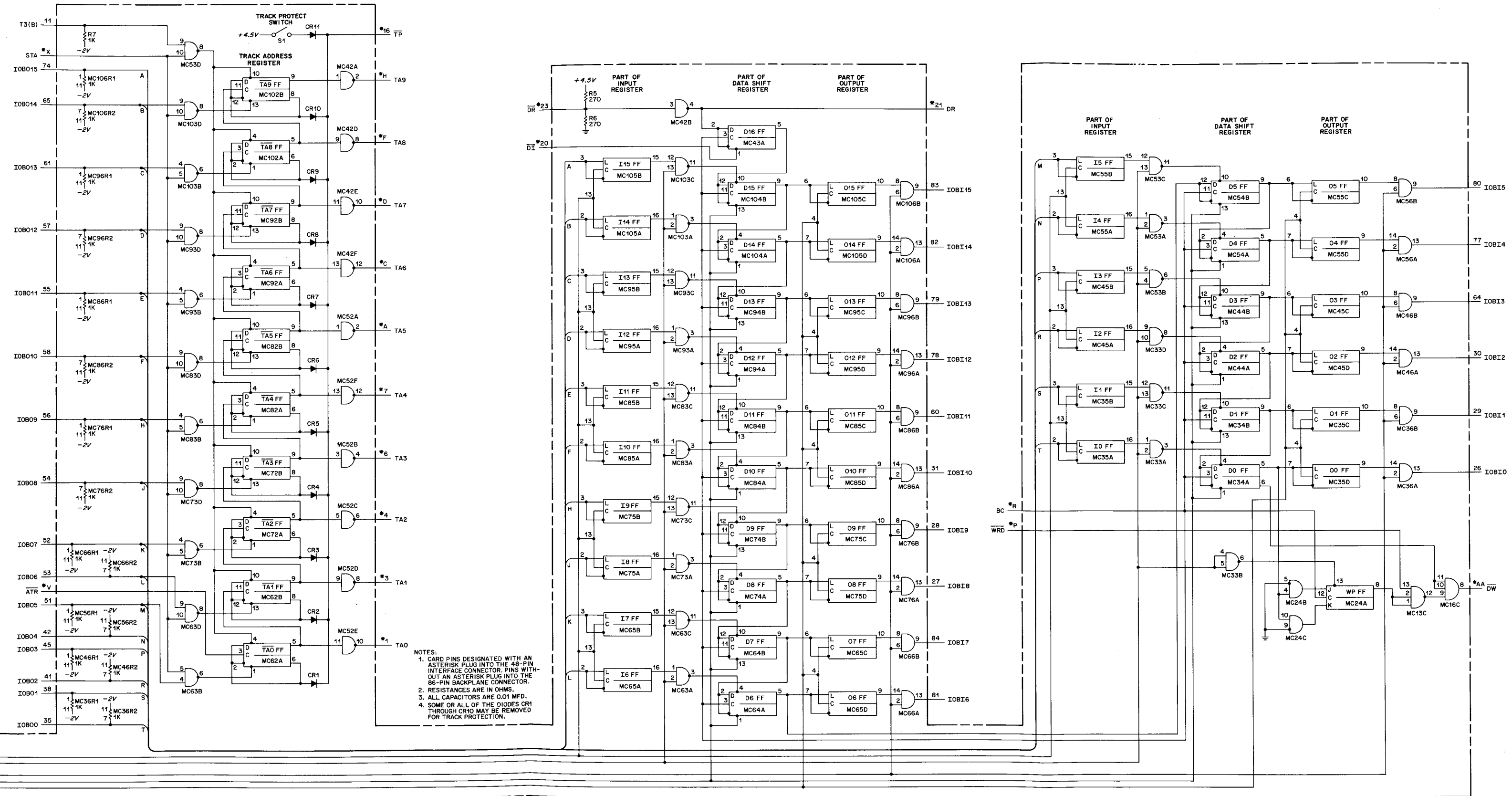"CMD-*" identifies a pin in the 48-pin connector for the command channel interface card.

"J1-" identifies a pin in connector J1 on the drum memory.

A dash for a ground return indicates that the common ground return between cards is used (pins 1, 2, 85, and 86 of the 86-pin connector). All signals transferred between the two interface cards use the common ground return. All signals transferred to or from the drum use a separate ground return, with the ground lead and signal lead forming a twisted pair.

COMMAND CHANNEL INTERFACE CARD (12610-6002, REV 914)

NOTES:
1. CARD PINS DESIGNATED WITH AN ASTERISK PLUG INTO THE 48-PIN INTERFACE CONNECTOR. PINS WITHOUT AN ASTERISK PLUG INTO THE 86-PIN BACKPLANE CONNECTOR.
2. RESISTANCES ARE IN OHMS.
3. ALL CAPACITORS ARE 0.01 MFD.

DWG REV B

Figure 5-5. Command Channel Interface Card
(12610-6002), Schematic Diagram

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2.   This section provides information for ordering replacement parts for the 12610B Drum Memory Interface Kit. Table 6-1 is a total-quantity listing of all replaceable parts in the kit.

6-3.   Reference designation indexes (tables 5-2 and 5-4) and parts location diagrams (figures 5-2 and 5-4) for the data channel interface card and the command channel interface card are provided in section V of this manual adjacent to the logic diagram for each card.

6-4.   Tables 5-2, 5-4, and 6-1 list the following information for each replaceable part:

a.   Reference designation of the part (tables 5-2 and 5-4 only). Refer to table 6-2 for an explanation of abbreviations used in the REFERENCE DESIGNATION column.

b.   Hewlett-Packard part number.

c.   Description of the part. Refer to table 6-2 for an explanation of abbreviations used in the DESCRIPTION column.

d.   A five digit code that corresponds to the manufacturer of the part. Refer to table 6-3 for a listing of the manufacturers that correspond to the codes.

e.   Manufacturer's part number.

f.   Total quantity (TQ) of each part used in the kit or assembly (table 6-1 only).

6-5. ORDERING INFORMATION.

6-6.   To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a.   Identification of the instrument, kit, or assembly containing the part (refer to paragraph 1-9).

b.   Hewlett-Packard part number for each part.

c.   Description of each part.

d.   Circuit reference designation (if applicable).

Table 6-1. Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0150-0093	Capacitor, Fxd, Cer, 0.01 uf, +80 −20%, 100 VDCW	18480	0150-0093	88
0683-1025	Resistor, Fxd, Comp, 1000 ohms, 5%, 1/4w	01121	CB1025	5
0683-2715	Resistor, Fxd, Comp, 270 ohms, 5%, 1/4w	01121	CB2715	10
0683-4715	Resistor, Fxd, Comp, 470 ohms, 5%, 1/4w	01121	CB4715	1
1820-0054	Integrated Circuit, TTL	01295	SN4342	14
1820-0065	Integrated Circuit, TTL	01295	SN4352	2
1820-0068	Integrated Circuit, TTL	56289	USN7410A	4
1820-0069	Integrated Circuit, TTL	56289	USN7420A	4
1820-0075	Integrated Circuit, TTL	01295	SN4353	3
1820-0077	Integrated Circuit, TTL	01295	SN4354	16
1820-0084	Integrated Circuit, TTL	01295	SN7453N	3
1820-0099	Integrated Circuit, TTL	01295	SN4462	3
1820-0132	Integrated Circuit, TTL	07263	U6A901659X	3
1820-0301	Integrated Circuit, TTL	01295	SN4463	11
1820-0372	Integrated Circuit, TTL	01295	SN4342	2
1820-0376	Integrated Circuit, TTL	01295	SN4484	3
1820-0956	Integrated Circuit, CTL	07263	SL3459	16
1854-0215	Transistor, Si, NPN	04713	SPS3611	1
1901-0040	Diode, Si, 30 mA	07263	FDG1088	10
1901-0460	Diode, Si, 3-Junction Stabistor	03508	STB523	1
3101-0932	Switch, Slide, DPDT, 0.5A, 125V AC/DC	79727	GG350-0001	1
12610-6001	Data Channel Interface Card	28480	12610-6001	1
12610-6002	Command Channel Interface Card	28480	12610-6002	1
12610-6004	Interface Cable (10 feet)	28480	12610-6004	1
12610-9001	Drum Memory Interface Kit Manual	28480	12610-9001	1
20340B	Drum Diagnostic Tape	28480	20340B	1

MANUAL SUPPLEMENT
DIAGNOSTIC PROGRAM PROCEDURES

for

12610B

DRUM MEMORY INTERFACE KIT

Note

This manual is considered part of and should be
attached to the 12610B Drum Memory Interface
Kit Operating and Service Manual.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2.   This manual supplement describes the Hewlett-Packard 20340C Drum Memory Diagnostic Program. The program tests the operation of the following:

    a.   HP 2773A Drum Memory in combination with the HP 12610B Interface Kit and HP 2776A Drum Memory Power Supply.

    b.   HP 2774A Drum Memory in combination with the HP 12610B Interface Kit and HP 2776A Drum Memory Power Supply.

    c.   HP 2775A Drum Memory in combination with the HP 12610B Interface Kit and HP 2777A Drum Memory Power Supply.

1-3. EQUIPMENT REQUIRED.

1-4.   The equipment items listed below, connected to form a computer system, are required for running the drum diagnostic program. One of each item is required.

    a.   Computer: HP 2114B, 2115A, or 2116A/B.

    b.   Direct Memory Access: HP 12578A or 12578A-01 (for HP 2115A or 2116A/B Computer), or HP 12607A (for HP 2114B Computer).

    c.   Teleprinter: HP 2752A or equivalent.

    d.   Teleprinter Interface Kit: HP 12531B.

    e.   Punched Tape Reader: HP 2737A or equivalent.

    f.   Punched Tape Reader Interface Kit: HP 12532A.

    g.   Drum Memory: HP 2773A, 2774A, or 2775A.

    h.   Drum Memory Interface Kit: HP 12610B.

    i.   Drum Memory Power Supply: HP 2776A (for HP 2773A or 2774A Drum Memory), or HP 2777A (for HP 2775A Drum Memory).

1-5.   If the computer system does not include a punched tape reader, the tape reading unit in the teleprinter can be used for reading the paper tapes used by the program. With this method of operation, however, tape reading speed is only 10 characters per second, as compared to 300 characters per second with the HP 2737A Punched Tape Reader.

1-6.   If two or more drums are used, each of them can be tested by running the diagnostic program separately for each drum, specifying the appropriate I/O select code each time the program is run.

1-7. PUNCHED TAPES REQUIRED.

1-8.   To run the drum diagnostic program, two punched paper program tapes are required. One contains the diagnostic program, the other contains a teleprinter driver routine. If the computer system includes a photoelectric paper tape reader, a tape-reader driver tape is also used.

1-9.   The tapes are selected in accordance with the size of the computer memory, as specified in table 1-1.

Note

The part number of each HP program tape is followed by a letter which identifies a particular revision of the tape. The first issue of a tape is identified by the letter A. Subsequent revisions are identified in sequence as B, C, D, etc. If a revision of a tape requires changes to associated documentation, an updating supplement for the documentation is supplied when the new tape is furnished. Always use the latest revision of a program tape, even if different from that specified in this manual, together with all updating documentation.

Table 1-1. Tapes Required

CORE MEMORY SIZE	DRUM MEMORY DIAGNOSTIC PROGRAM TAPE	SYSTEM INPUT/OUTPUT (SIO) BUFFERED DRIVER TAPE (TELEPRINTER)	SYSTEM INPUT/OUTPUT (SIO) BUFFERED DRIVER TAPE (TAPE READER)
4K	HP 20340C	HP 20322A	HP 20303A
8K thru 12K	HP 20340C	HP 20323A	HP 20306A
16K thru 32K	HP 20340C	HP 20330B	HP 20319A

1-10. An optional data tape may also be used with the diagnostic program. This tape, which is prepared in the field, avoids the necessity for manually inserting test words and drum addresses during the diagnostic program. Instructions for preparing this tape are given in paragraph 2-157. This tape can be used either in the photoelectric tape reader or in the tape reading unit which is part of the teleprinter.

1-11. NOTATION.

1-12. NUMBER BASE.

1-13. Throughout this manual, numbers are in decimal form unless otherwise specified. Drum track and drum sector numbers are always in octal form. Numbers typed by the teleprinter during the program, and numbers entered into the teleprinter, are in octal or binary form.

1-14. USE OF QUOTATION MARKS.

1-15. In this manual, examples of teleprinter printouts are presented verbatim and in quotation marks. In the printouts themselves the quotation marks do not appear.

1-16. The displayed contents of registers are also shown in quotation marks, and are stated in octal notation.

1-17. DRUM CAPABILITIES.

1-18. Before starting the drum diagnostic program, the operator must know the number of tracks on the drum. Table 1-2 lists this information for each type of drum. The 2773A has a basic number of tracks that can be increased in the factory or in the field by the addition of modification kits which increase the number of tracks in increments of 64.

Table 1-2. Drum Track Capacity

DRUM MEMORY	CAPACITY
HP 2773A	192 (300_8) tracks minimum; 512 (800_8) tracks maximum
HP 2774A	384 (600_8) tracks minimum; 512 (800_8) tracks maximum
HP 2775A	768 (1400_8) tracks

1-19. Each track has 32 (40_8) sectors, and each sector can store 64 (100_8) words consisting of 17 bits (including parity bit).

1-20. Some or all tracks can be protected against writing by the use of a track protect switch. The number of tracks protected is established by installing or removing diodes

from Data Channel Interface Card 12610-6001, as described in the Drum Memory Interface Kit Manual (Part no. 12610-9001).

1-21. SIZE OF DATA-TRANSFER BLOCK.

1-22. Before starting the drum diagnostic program, the operator must know the maximum number of sectors that can be transferred to or from the drum in a single group. This is dependent on the size of core memory in the computer, as indicated in table 1-3.

Table 1-3. Maximum Data-Transfer Block

CORE MEMORY SIZE	MAXIMUM DATA-TRANSFER BLOCK
4k	14 (16_8) Drum sectors
8K	63 (77_8) Drum sectors
Greater than 8K	64 (100_8) Drum sectors

1-23. CORE MEMORY REQUIREMENTS.

1-24 Table 1-4 lists the core memory locations required by the drum memory diagnostic program.

Table 1-4. Core Memory Requirements

CORE MEMORY SIZE	LOCATIONS REQUIRED (OCTAL)
All sizes	000100—001702
All sizes	002000—005204
PLUS ONE OF THE FOLLOWING:	
4K	007235—007677*
8K	017235—017677*
Greater than 8K	037235—037677*
*Required for SIO teleprinter and tape reader drivers.	

1-25. CONTROLS AND INDICATORS.

1-26. Table 1-5 gives the locations of controls and indicators used in running the drum diagnostic program.

Table 1-5. Locations of Controls and Indicators

CONTROL OR INDICATOR	LOCATION
AC POWER switch	Drum memory power supply
DC POWER switch	Drum memory power supply
DRUM READY lamp	Drum control panel
HALT switch	Computer
HEADS switch	Drum control panel
LINE FEED key	Teleprinter
LOAD ADDRESS switch	Computer
LOAD MEMORY switch	Computer
ON LINE, OFF, LOC. switch	Teleprinter
POWER switch	Computer
P-register display	Computer (not on 2114B)
PRESET switch	Computer
RETURN key	Teleprinter
SWITCH REGISTER switches	Computer
Track protect switch	Data Channel Interface Card 12610-6001*
T-register display	Computer (not on 2114B)

*Card 12610-6001 is an I/O interface card in the computer card cage. The card slot in which it is situated determines the drum I/O select code.

SECTION II

PROGRAM DESCRIPTION

2-1.   INTRODUCTION.

2-2.   The drum diagnostic program uses three diagnostic subroutines and one control subroutine to execute the following tests:

    a.   Track protect test.

    b.   Track address test.

    c.   Read/write test.

    d.   Sector timing test.

    e.   Power failure test.

2-3.   The tests are conducted in the sequence listed, and they perform the following functions:

    a.   The track protect test checks that the track protect feature is functioning normally.

    b.   The track address test checks that the correct track is selected when a drum track is addressed for reading or writing.

    c.   The read/write test checks that data stored on the drum can be read back without error.

    d.   The sector timing test checks that the sector timing pulse pairs are correctly counted. This test uses the same subroutine as the read/write test.

    e.   The power failure test checks the ability of the drum to retain data through a temporary failure of the power line voltage. The test also checks that when a power failure occurs during drum writing, no tracks and sectors lose data except those involved in the write operation. The power failure test uses the same subroutine as the read/write test.

2-4.   OPTIONAL FUNCTIONS.

2-5.   The drum diagnostic program has several optional functions, which can be selected by setting SWITCH REGISTER switches as shown in table 2-1. A switch is set to the up position for logic 1, and to the down position for logic 0.

2-6.   ENTRY OF INFORMATION ON THE TELEPRINTER.

2-7.   At various points in the program, the operator is required to enter information on the teleprinter. When this .

type of data entry is needed, the program first prints on the teleprinter a request for the information; the program then enters a waiting loop until the operator responds. The operator manually types the information requested, then presses the RETURN key to return the type head to the left margin of the paper. Next, the operator presses the LINE FEED key. This action transfers to the computer the last line of information typed and brings the program out of its waiting loop. (On some teleprinters the RETURN key is labeled CARRIAGE RETURN.)

2-8.   PRELIMINARY PROGRAM FUNCTIONS.

2-9.   After the drum diagnostic program is started, certain preliminary information must be supplied to the program. This is done by manual input on the teleprinter.

2-10.   The first information required is the direct memory access (DMA) channel number used by the drum. The channel number can be 6 or 7 (only 6 in the case of the 2114B Computer). When this information is needed, the program prints "DMA OCTAL CHANNEL # ?", then enters a waiting loop. The operator types in the channel number, presses the RETURN key, and then presses the LINE FEED key. Pressing the LINE FEED key takes the program out of its waiting loop.

2-11.   The next information required by the program is the I/O select code of the drum. When this is needed, the program types "HIGH PRIORITY OCTAL DRUM ADDRESS?", then enters a waiting loop. The operator responds by typing on the teleprinter the I/O select code associated with the card slot in which data channel ‛card 12610-6001 is located. (Two I/O interface cards are used for each drum employed. The cards are in adjacent card slots, with the data channel card situated in the slot with the higher I/O priority.)

2-12.   After typing the I/O select code for the drum to be tested, the operator presses the RETURN and LINE FEED keys. The LINE FEED key takes the program out of its waiting loop, and the program then starts the track protect test without further operator intervention.

2-13.   TRACK PROTECT TEST.

2-14.   TEST DESCRIPTION.

2-15.   The track protect test checks the ability of the track protect switch to prevent writing on protected drum tracks. During the test no drum writing or reading takes place. Therefore, material previously stored on the drum is not destroyed by this part of the diagnostic program. The track protect test cannot be looped; one pass at the test is an adequate check of the protect circuits, unless an inter-_nittent fault exists.

Table 2-1. Selection of Program Functions

SWITCH REGISTER SWITCH	LOGIC SETTING	PROGRAM ACTION
15	1	Use data tape in photoelectric tape reader for parameter input, and omit request printouts.
	0	Use teleprinter for parameter input, and execute request printouts. Parameters can be supplied to the teleprinter either on the keyboard or from a data tape read by the teleprinter tape reading unit.
14	1	Use SWITCH REGISTER switches for test word input, and omit "BINARY TEST PATTERN?" printout.
	0	Use tape reader or teleprinter for test word input.
11	1	Loop on track address test.
	0	Omit or exit track address test.
3	1	Omit error printouts. The "DRUM NOT READY" printout and operator error printouts are still provided.
	0	Execute error printouts and error stops.
2	1	Loop on read test.
	0	Do not loop on read test.
1	1	Loop on write test.
	0	Do not loop on write test.
0	1	Loop on read/write test.
	0	Perform single execution of read/write test.

NOTES:

Switches 15, 14, 3, 2, 1, and 0 affect the read/write subroutine. Switches 11 and 3 affect the track address test.

When read, write, or read/write looping is being performed, the program does not examine switches 15, 14, and 11.

Except when transferring from one type of looping to another, only one of the switches 2, 1, and 0 should be at logic 1.

2-16.   TEST METHOD.

2-17.   Before the start of the diagnostic program, the track protect switch is set to the "protect" position, if not already at that position. This switch must be set before the program preliminary functions are completed, since there is no stop or waiting loop after the DMA channel number and drum I/O select code have been entered into the program.

2-18.   When the track protect test is performed, the program checks the number of drum tracks being protected by the track protect switch. When the check is complete, the program prints "NO. OF PROTECTED TRACKS —", followed by a 4-digit octal number stating the number of tracks found to be protected. This number should correspond to the number of tracks for which protect status has been established.

2-19.   After printing out the number of protected tracks, the program proceeds to the next test without operator intervention.

2-20.   TRACK ADDRESS TEST.

2-21.   TEST DESCRIPTION.

2-22.   The track address test checks to ensure that when a particular track on the drum is addressed, the correct track is selected. All tracks are subjected to this test. The track address test also performs a preliminary check of the drum read and write circuits.

2-23.   The program writes the address of each track in the first sector of the track. All 64 word-locations in the sector receive this data. Then, the program reads back all words in the first sector of each track, and checks the 64 words to ensure that each is the same as the track number that was addressed for reading. If no error is found, a printout indicates that the test was passed successfully. If one or more words in a sector are not the same as the track address, an error printout is furnished.

2-24.   The track protect switch must be in the non-protect (down) position before the track address test is started, otherwise false error printouts will occur. Faulty read or write circuits may also cause false error printouts, which will indicate a track addressing error rather than faulty read or write circuits.

2-25.   The track address test destroys any data previously stored in the first sector of every track on the drum.

2-26.   The track address test can be omitted by setting SWITCH REGISTER switch 11 to logic 0 before the track protect test is reached (refer to table 2-1). When switch 11 is at logic 1, the track address test is performed, and it will be repeated continuously until switch 11 is set to logic 0. Unless an intermittent fault exists, only one pass through the track address test is required. Looping is used for troubleshooting purposes when a fault is detected.

2-27.   TEST METHOD.

2-28.   After the completion of the track protect test, the track address test starts without operator intervention. Because there is no program stop at the end of the track protect test, SWITCH REGISTER switch 11 must be set to execute or bypass the track address test before the drum diagnostic program is started.

2-29.   When the track address test starts, the program prints "NO. OF TRACKS?" on the teleprinter, then enters a waiting loop. The operator sets the track protect switch to the off (down) position, then types on the teleprinter a 4-digit octal number stating the total number of tracks on the drum. This number is one greater than the highest track address. The operator then presses the RETURN and LINE FEED keys, and the program leaves its waiting loop.

2-30.   The program now executes the check of track addressing circuits in the manner previously described. Error printouts are furnished if faults are detected.

2-31.   When the test is looped (SWITCH REGISTER switch 11 is at logic 1 at the end of a pass), the printout requesting information is not repeated after the first pass.

2-32.   When SWITCH REGISTER switch 11 is set to logic 0, the track address test completes its current pass, after which the program proceeds to the read/write test.

2-33.   PRINTOUTS.

2-34.   TYPES OF PRINTOUT. During the track address test, three types of printout can occur. These are as follows:

   a.   Request printout.

   b.   If no error is detected, a printout stating that the test has been successfully completed.

   c.   Error printouts.

2-35.   REQUEST PRINTOUT. One type of request printout is furnished during the track address test. The printout, which has been explained previously, is "NO. OF TRACKS ?".

2-36.   COMPLETION PRINTOUT. When the track address test is completed without detection of an error, "TRACK ADDRESS CHECK COMPLETE" is printed. When looping, the printout is furnished only after completion of the last pass.

2-37.   ERROR PRINTOUTS. If a fault is detected during the track address test, one of the following printouts is furnished:

   a.   "TRACK ADDRESS ERROR
"EXPECTED TRACK XXXX, ACTUAL TRACK XXXX" (where X is an octal digit).

   b.   "DRUM NOT READY".

2-38. The first type of error printout indicates that when a certain track was addressed for reading, one or more words in the first sector did not contain the track number. The printout is furnished for each such error, and thus may occur 64 times for a single sector. The program does not stop after furnishing this printout. It should be borne in mind that faulty write or read circuits can cause this printout.

2-39. The "DRUM NOT READY" printout occurs when the drum ready flag bit is logic 0. The printout indicates that the wrong I/O select code was entered for the drum earlier in the program, the drum is not plugged in, the drum memory power supply is defective or not switched on, the drum is not up to operational speed, or the drum ready flag bit circuits are faulty. The program stops after this printout is furnished. When the situation is corrected, the diagnostic program can be resumed by pressing the RUN switch.

2-40. READ/WRITE TEST.

2-41. TEST DESCRIPTION.

2-42. The read/write test stores 16-bit words on the drum, then reads them back and checks them to ensure that they are the same as the words written. The tracks and sectors on which the test words are written, and the test words themselves, can be specified by a data tape or entered manually by the operator. Usually, a data tape is used for an initial and complete check of the drum read and write capabilities. This data tape tests all tracks and sectors on the drum, checking each word-location by storing both "1's" and "0's" in each bit position. Then, if a fault is detected by the program, the operator performs the read/ write test again, this time using manually entered drum addresses to exercise only the failing tracks and sectors. The test word also is entered manually after error detection, and it too can be selected to suit the fault symptoms.

2-43. Using either a data tape or manually entered data, any 16-bit word can be stored in any sector or sectors of any track or tracks. The 64 word-locations in all sectors specified for test can be filled with the same word, or a variety of test patterns can be used consisting of the test word and its one's complement. A third method, using manual data entry, writes a different word in each word-location of a sector, with each specified sector containing the same 64 words.

2-44. If an error is detected, the program types an appropriate error printout on the teleprinter. If the error results from a mistake by the operator, or is due to a faulty data tape, the program stops to permit correction of the error.

2-45. The time required to run the read/write test depends on the number of tracks and sectors in which writing and reading takes place, and on the type of computer used. An error printout delays the program for the time required for printing.

2-46. Successful completion of the test is indicated by the absence of error printouts. At the end of the test the program enters a waiting loop in readiness for new test words and drum addresses. As an alternative, the test program can be looped to repeat the test as many times as desired.

2-47. Control of test functions is exercised by SWITCH REGISTER switches 15, 14, 3, 2, 1, and 0 (refer to table 2-1). Switch 15 permits the operator to select the way in which tracks and sectors are designated for test. If switch 15 is at logic 1, track and sector designation is made by the data tape, which is prepared beforehand to test any desired tracks and sectors with any desired test word. The tape is read by the computer automatically at the appropriate times. When switch 15 is at logic 0, it causes the program to print requests on the teleprinter for track and sector designations. The operator responds to these requests by manually typing the requested information. With manual data entry, a printed record is furnished of the tracks and sectors selected.

2-48. SWITCH REGISTER switch 14 selects the way in which test words will be entered into the program. When the switch is at logic 0, a single test word is used, and it is entered in the same manner as track and sector addresses — that is, either from the data tape or by manual entry on the teleprinter, as determined by SWITCH REGISTER switch 15. When manual entry is used, the test word is requested on the teleprinter. The operator responds by typing the test word, thereby furnishing a written record of the word used. When switch 14 is at logic 1 at the start of the test, 64 test words are used, and they are entered in sequence into the SWITCH REGISTER switches. The 64 test words can all be different, some can be alike, or all can be alike. This method of supplying test words is used when a fault is responsive to groups of two or more words having bit configurations which are different and not complementary. No written record is furnished of the 64 words.

2-49. SWITCH REGISTER switch 3, when set to logic 1, eliminates error printouts and error stops.

2-50. SWITCH REGISTER switches 2, 1, and 0 permit the test to be looped in three different ways. In any of these types of looping, test parameters (the test word, track designation, and sector designation) are inserted during the first loop only. Thereafter, these parameters are used for each pass until looping is terminated.

2-51. SWITCH REGISTER switch 2, when set to logic 1, permits looping of the read part of the test. Test words are written on the drum in the first program pass, but in subsequent passes the write portion of the test is bypassed. In each read pass the words read are compared with the words that were initially written, and error printouts are furnished if a discrepancy is detected.

2-52. SWITCH REGISTER switch 1 permits looping of the write operation, while omitting the read and comparing functions of the test. Write looping is rarely used in the read/write test, since most types of errors are detected only

during the read cycle. However, write looping serves an important function in the power failure test, which is performed later in the drum diagnostic program using the read/write test subroutine.

2-53. SWITCH REGISTER switch 0 permits the entire read/write test to be looped.

2-54. No useful function is achieved by attempting to conduct more than one type of looping at a time. Therefore, only one of the three switches which control looping should normally be at the logic 1 position. However, to avoid termination of looping when changing from one type of looping to another, it is necessary to set to logic 1 the switch for the looping to be started, before setting to logic 0 the switch for the looping to be stopped.

2-55. When switch 2, 1, or 0 is returned to logic 0 to stop all looping, the program completes the current pass. The program can then be rerun, if desired, with a new test word and with new track and sector addresses.

2-56. TEST METHOD.

2-57. INTRODUCTION. The read/write test starts without operator intervention as soon as the preceding test is exited. Therefore, SWITCH REGISTER switches which control the read/write test must be positioned before the drum diagnostic program is started.

2-58. As noted earlier, switches 15 and 14 can establish any of three ways in which test parameters will be furnished. (Test parameters are test words, track designations, and sector designations.) Depending on the way in which these parameters are to be supplied, the program functions in one of the following ways when it starts:

 a. The program prints "BINARY TEST PATTERN ?" on the teleprinter, then enters a waiting loop. (SWITCH REGISTER switches 15 and 14 at logic 0.)

 b. The program stops. (SWITCH REGISTER switch 14 at logic 1 and switch 15 at logic 0).

 c. The program reads a set of test parameters from the data tape, and proceeds with the test. (SWITCH REGISTER switch 15 at logic 1 and switch 14 at logic 0).

2-59. In the first of the above operating methods (SWITCH REGISTER switches 15 and 14 are at logic 0), all test parameters will be furnished by manual entry into the teleprinter. In the second method (switch 14 at logic 1), test words will be entered manually into the switch register and drum addresses will be entered manually into the teleprinter. In the third method (switch 15 at logic 1), all test parameters will be acquired from a data tape. Each of these methods is described separately in the paragraphs which follow.

2-60. MANUAL ENTRY INTO TELEPRINTER. This type of operation begins with the program printing

"BINARY TEST PATTERN?", and entering a waiting loop. First, the operator ensures that the track protect switch is in the off (down) position if writing is to be performed in protected tracks. In response to the printed request, the operator then types a 16-bit test word, followed by two control-code characters which indicate the complementing pattern to be employed. (The control-code characters are described in paragraphs 2-90, 2-91, and 2-92.)

2-61. After typing the test word and control-code characters, the operator presses the RETURN and LINE FEED keys, and the program leaves the waiting loop.

2-62. As the next operation, the program prints "WRITE TRACKS ?", and enters a waiting loop. The operator responds by typing an identification of the track or tracks to be written upon, using the track designation system described in paragraphs 2-95 through 2-98.

2-63. After typing the track designation or designations, the operator presses the RETURN and LINE FEED keys, and the program leaves its waiting loop.

2-64. Next, the program prints "WRITE SECTORS ?", and enters a waiting loop. The operator responds by typing an identification of the sector or sectors to be written upon, using the sector designation system described in paragraphs 2-99 through 2-103. The same sector or sectors will be written on in each of the tracks previously designated.

2-65. After typing the sector designation or designations, the operator presses the RETURN and LINE FEED keys, and the program leaves its waiting loop.

2-66. The program next writes the test word on the designated tracks and sectors, using complement patterns if these were designated when the test word was typed. If write looping was selected at the start of the diagnostic program (SWITCH REGISTER switch 1 at logic 1), the program continues to write and rewrite on the designated tracks and sectors until switch 1 is returned to logic 0. The program then types "BINARY TEST PATTERN ?", and enters a waiting loop. The test can then be rerun using new test parameters and any of the three types of looping.

2-67. If write looping was not selected initially, the program writes once in the designated drum addresses after the write sectors are identified, then prints "READ TRACKS ?", and enters a waiting loop.

2-68. The operator responds by typing the designation of the track or tracks to be read. These will normally be the same as the tracks for which writing was specified, and the same method of designation is used.

2-69. The operator presses the RETURN and LINE FEED keys, and the program leaves its waiting loop.

2-70. The program types "READ SECTORS?", and enters a waiting loop. The operator responds by typing an identification of the sector or sectors to be read.

2-71. The operator presses the RETURN and LINE FEED keys, and the program leaves its waiting loop. Operations now depend on the setting of SWITCH REGISTER switches 0 and 2. If both are at logic 0, the program reads the designated tracks and sectors once, compares each word read with the test word or words, and furnishes error printouts to identify any discrepancies. (Error printouts are described in paragraph 2-117.) After completing the comparison of words read with words written, the program prints "BINARY TEST PATTERN ?", and enters a waiting loop. The test can now be repeated with different test words, drum addresses, and looping method.

2-72. If SWITCH REGISTER switch 0 is at logic 1 when the read designations are entered, the program performs read/write looping. It writes, reads, and compares in each pass of the test. Again, error printouts are furnished if discrepancies are detected. The procedure continues until looping is stopped by returning switch 0 to logic 0. The test then completes its current pass, prints "BINARY TEST PATTERN ?", and enters a waiting loop in readiness for new test parameters.

2-73. Finally, if SWITCH REGISTER switch 2 is at logic 1 when the read drum addresses are typed, the program enters a read loop. It reads all designated tracks and sectors, compares the words read with those originally written, and provides error printouts if discrepancies are detected. The procedure continues until looping is stopped by returning switch 2 to logic 0. The test then completes its current pass, prints "BINARY TEST PATTERN ?" and enters a waiting loop in readiness for new test parameters.

2-74. MANUAL ENTRY OF TEST WORD IN SWITCH REGISTER. When manual entry of test words into the SWITCH REGISTER switches has been selected (SWITCH REGISTER switch 14 at logic 1 at the start of the read/write test), the program stops at the beginning of the test. The operator ensures that the track protect switch is in the off (down) position if writing is to be performed in protected tracks. The operator then enters 64 words in sequence into the SWITCH REGISTER switches, pressing the LOAD MEMORY switch after setting up each word. SWITCH REGISTER switch 0 is the low-order bit of the 16-bit words.

2-75. After the 64 words have been entered, SWITCH REGISTER switch 0, 1, or 2 is set for looping, if desired. Then the RUN switch is pressed twice to start the program. The first time the switch is pressed, the program encounters a halt instruction. This instruction prevents damage to the program if 65, rather than 64, test words were entered. If a 65th word is accidently inserted, it takes the place of the halt instruction, and the program starts the first time the RUN switch is pressed. The 65th word then has no further affect on the program.

2-76. After the program starts, it prints "WRITE TRACKS ?". From this point, the program functions in the same manner as when test words are manually entered into the teleprinter.

2-77. DATA TAPE AS SOURCE OF TEST PARAMETERS. When a data tape is used as the source of test parameters (SWITCH REGISTER switch 15 at logic 1), the program reads a set of test parameters off the data tape when the test starts. The test is then performed with these parameters. If looping is not being conducted, the program returns to the data tape for a new set of parameters at the end of each pass, and repeats the procedure as long as parameters are available on the tape. When looping is conducted, SWITCH REGISTER switch 2, 1, or 0 is set to logic 1 before the test, and looping takes place with the first set of parameters read from the tape. To acquire a second set of parameters from the tape, the looping control switch is set to logic 0. The program then completes its current pass, reads a set of parameters from tape, and starts the test with the new parameters. The looping control switch is set to logic 1 during the first pass in order to maintain looping with the second set of parameters. The process may be continued with as many sets of parameters as are available on the tape.

2-78. If the SWITCH REGISTER switch that is controlling looping is set to logic 0, the current pass is completed, the program prints "BINARY TEST PATTERN ?", and enters a waiting loop. Operations can then continue with test parameters manually entered into the teleprinter.

2-79. When operating with a data tape no requests for test parameters are printed by the program. However, error printouts are furnished if faults are encountered.

2-80. WRITE BYPASSING.

2-81. In the read/write test it is possible to bypass the write cycle in two ways. The first method, setting SWITCH REGISTER switch 2 to logic 1, has been explained earlier. This method has the disadvantage that writing still takes place during the first pass through the test, possibly destroying data that must be retained.

2-82. To retain previously written data, it is possible to bypass the write cycle entirely. In this type of operation a test word is entered into the program, but is not written on the drum. Then, when reading takes place, the test word is used for comparison purposes. To conduct this type of testing, the words in the tracks and sectors specified for reading must be known. Read looping and other functions of the read/write test can be performed in the normal manner.

2-83 To bypass writing, the operator presses the teleprinter space bar once in response to the request "WRITE TRACKS ?". Then, the RETURN and LINE FEED keys are pressed in the normal manner. The program omits the "WRITE SECTORS ?" printout, and proceeds to the "READ TRACKS ?" printout regardless of the setting of SWITCH REGISTER switch 1.

2-84. If a data tape is being used as the source of test parameters, a space symbol is punched on the tape in place

of the write track designation, followed by a carriage return and line feed symbol. No write sector designation is punched on the tape.

2-85.   READ BYPASSING.

2-86.   The read function can be bypassed in the same manner as the write function, by providing a space symbol in place of the read track designation and omitting the section designation.

2-87.   TEST WORD PATTERNS.

2-88.   In the drum tracks and sectors specified for writing, test words can be written in any of the following ways during a given pass of the read/write test:

a.   Any desired 64 words can be written in the 64 word-locations of each specified sector. The 64 words can all be different, but all sectors will contain the same 64 words in the same sequence. Complement patterns cannot be used.

b.   In all specified sectors, the same word can be repeated in the 64 word-locations of each sector.

c.   In all specified sectors, a word and its one's complement can be written in alternate word-locations.

d.   A word and its one's complement can be written in alternate sectors, until all specified sectors have been written upon. In a given sector all 64 word-locations will then contain the same data (either the word typed or its complement).

e.   Methods "c" and "d" above can be combined. That is, in each specified sector a word and its one's complement are written in alternate word-locations, and each sector contains the complement of the sector previously written.

2-89.   In method "a" above, the 64 16-bit words are entered in sequence into the SWITCH REGISTER switches by the operator.

2-90.   For the four methods of writing a test word described in "b", "c", "d", and "e" above, a single 16-bit word is manually entered on the teleprinter by the operator. Alternatively, the 16-bit word can be supplied by a data tape. To indicate the particular complement pattern desired, two control-code characters are furnished by the operator or the data tape after the 16-bit word. Each control-code character is either a letter "C" or a space.

2-91.   To illustrate the method of specifying complement patterns, the following is a typical 16-bit word that might be entered on the teleprinter or punched on a data tape:

1100110011001100CC

The first 16 characters are the binary word to be written on the drum. The first "C" specifies that alternate-word complementing is to be performed. The second "C" specifies alternate-sector complementing. When either or both types of complementing take place, complementing is alternated in each write pass of the program. That is the "1's" and "0's" in each word on the drum are reversed each pass.

2-92.   If alternate-word or alternate-sector complementing is not to be performed, a blank (space bar operation) is entered into the teleprinter or punched on the data tape in place of the appropriate "C".

2-93.   TRACK AND SECTOR SELECTION.

2-94.   INTRODUCTION. During the read/write test, the operator or a data tape specifies drum tracks and sectors on which writing or reading will take place. Both manual and data-tape entry employ the same format.

2-95.   TRACK DESIGNATION FORMAT. When the program prints "WRITE TRACKS ?" or "READ TRACKS ?", one or more track numbers must be entered, and the number of consecutive tracks must be specified. (As an exception, when writing is to be suppressed only the space bar is pressed, or the data tape supplies only a space symbol.) When actual tracks are designated, the following format is used:

T0000—0001

The letter "T" indicates that a track identification is being entered. The four digits following the "T" identify, in octal notation, the address of the first track to be written or read. The four digits after the hyphen specify, in octal notation, the number of tracks to be sequentially written or read. In the example shown, writing or reading will take place in track 0000, and one track will be written or read. There must always be four digits after the "T" and four digits after the hyphen.

2-96.   The next example shows how successive tracks are specified:

T0005—0004

In this example, writing or reading will take place on tracks 0005, 0006, 0007, and 0010.

2-97.   Nonsuccessive tracks are specified by using the following format.

T0006—0001, T0011—0001, T0444—0001

In this example, writing or reading will take place on tracks 0006, 0011, and 0444. A comma follows each track designation except the last one; there is no space after the comma. The track addresses must be arranged in ascending numerical sequence. (The sector timing test departs from this rule in order to perform its particular functions.)

2-98. Groups of successive tracks can also be specified, as in the following example:

T0000—0002, T0020—0007, T0040—0004

In this example, writing or reading will take place in tracks 0000, 0001, 0020 through 0026, and 0040 through 0043. The track addresses must be arranged in ascending numerical sequence. (The sector timing test departs from this rule.)

2-99. SECTOR DESIGNATION. FORMAT. After track identification has been entered, the program types on the teleprinter: "WRITE SECTORS?" or "READ SECTORS?". Identification of sectors is then made in a manner similar to that used for tracks. A sector designation begins with the letter "S". The first-sector address and the number of sectors are each specified by two digits, using octal numbers. To illustrate, the following might be entered as sector identification.

S11—01, S20—04, S33—03

In this example, writing or reading will take place in sectors 11, 20 through 23, and 33 through 35. These sectors will be addressed in all tracks that were specified when the track request was made.

2-100. The sector addresses must be arranged in ascending numerical sequence. (The sector timing test departs from this rule in order to perform its particular functions.)

2-101. If the quantity of consecutive sectors specified is greater than the number of sectors remaining in a track, incrementing of the current track address takes place after the last sector in the track, and the operation is continued from sector 00 of the next track. When two or more groups of sectors are specified, care must be exercised that this function does not result in overlap of the groups of sectors. Also, if there is data on the drum which must be retained, care must be observed that track address incrementing does not result in writing on tracks that must be protected.

2-102. The number of consecutive sectors specified must not exceed the maximum data-block capabilities of the core memory in the computer. (Refer to table 1-3.) For instance, the designation S00-17 must not be used when the computer has a 4K core memory. Instead, the following can take its place, and will perform the operation desired:

S00—16, S16—01

2-103. Another precaution that must be observed is that the total number of sector groups must not exceed 128 (200_8), regardless of the size of core memory. To illustrate, the example in the preceding paragraph has two groups of sectors; up to 128 such groups can be specified.

2-104. END-OF-LINE PROCEDURE. When tracks and sectors are being specified, and the teleprinter reaches the end of the typing line, a virgule (/) is typed as the last character in the line to indicate continuation on the next line. The virgule must not break a track or sector designation; that is, it must take the place of the comma that normally follows a track or sector designation. The virgule must appear in, or prior to column 72 on the teleprinter.

2-105. After the virgule is typed, the operator presses the RETURN key and the LINE FEED key. When a data tape is used, symbols are punched on the tape to reproduce the virgule, carriage return, and line feed functions.

2-106. ELIMINATION OF ERROR STOPS AND ERROR PRINTOUTS.

2-107. It has been seen that in the event of operator error or a defective data tape, the read/write test stops after providing an error printout. To prevent these program stops, SWITCH REGISTER switch 3 is set to the logic 1 position. As well as preventing error stops, this setting of the switch prevents the occurrence of error printouts, regardless of the cause of the error. As an exception, the "DRUM NOT READY" printout still can occur, and still is accompanied by an error halt.

2-108. ERROR COUNT.

2-109. A count is maintained of the number of word-comparison errors detected in the read/write test. This count continues regardless of whether SWITCH REGISTER switch 3 is set to stop error printouts.

2-110. The error count is maintained in memory locations 001700 and 001701. At the start of the read/write test these locations are cleared to zero by the program. Then, during the test, location 001700 is incremented by 1 each time a word read from the drum is not the same as the test word. The program allows for complement patterns, and for 64 different test words if these are used. After $65,536_{10}$ errors, location 001700 overflows and clears to zero. When this occurs, location 001701 is incremented by 1. Location 001700 then recommences its count, incrementing 001701 each time it overflows.

2-111. To display the count, the program is stopped, and the contents of locations 001700 and 001701 are displayed. Then, to resume the program, the operator loads 002402 into the P-register, and the program resumes with the "BINARY TEST PATTERN ?" printout. After a new test word is entered, the two count locations are cleared to zero by the program in preparation for further testing.

2-112. The principal use of the error counter is to determine whether occasional errors are occurring. The read/write test can be allowed to loop for several hours, and the count will be automatically maintained. The error counter also has sufficient capacity to count errors that occur at a rapid rate. When errors occur rapidly, it is usually best to step error printouts and halts by setting SWITCH REGISTER switch 3 to logic 1.

2-113. PRINTOUTS.

2-114. TYPES OF PRINTOUT. During the read/write test, two types of printout may occur. These are as follows:

a. Requests for test words, track designations, and sector designations.

b. Error printouts identifying operator error, faulty data tape, or an equipment fault in the drum memory, drum memory interface kit, or drum memory power supply. Faults in the computer central processing unit or in the DMA system can also cause error printouts. Therefore, the computer and DMA system should be checked with an appropriate diagnostic program if this difficulty is suspected.

2-115. When looping is performed, the request printouts occur during the first pass only. Error printouts are always furnished when an error is detected, unless SWITCH REGISTER switch 3 is at logic 1.

2-116. REQUEST PRINTOUTS, READ/WRITE TEST. Five types of request printout occur during the read/write test. These have been explained previously, and are listed below in the sequence in which they are printed.

a. "BINARY TEST PATTERN ?".

b. "WRITE TRACKS ?".

c. "WRITE SECTORS ?".

d. "READ TRACKS ?".

e. "READ SECTORS ?".

2-117. ERROR PRINTOUTS, READ/WRITE TEST.

2-118. Introduction. When an error is detected during the read/write test, one of the following printouts is furnished by the teleprinter:

a. "BINARY PATTERN EXCEEDS 72 CHARACTERS".

b. "CHARACTER IN OCTAL PARAMETER ILLEGAL".

c. "DRUM NOT READY".

d. "ERROR BUSY STATUS BIT DURING WR/RD".

e. "ILLEGAL CHARACTER IN TEST PATTERN PARAMETER".

f. "IMPROPER CHARACTER IN WR/RD PARAMETER".

g. "READ ABORT — TRACK" (followed by an octal number).

h. "READ INTERRUPT MISSING "DMA WORD COUNT=" (followed by an octal number).

i. "READ PARAMETER INCOMPLETE".

j. "READ PARITY ERROR".

k. "READ SECTOR BUFFER OVERFLOWED".

l. "TRACK XXXX SECTOR XX WORD NO. XX "OUTPUT XXXXXX INPUT XXXXXX" (where X represents any octal digit).

m. "WRITE ABORT - TRACK" (followed by an octal number).

n. "WRITE INTERRUPT MISSING "DMA WORD COUNT=" (followed by an octal number).

o. "WRITE PARAMETER INCOMPLETE".

p. "WRITE SECTOR BUFFER OVERFLOWED".

q. "WR/RD PARAMETER EXCEEDS 72 CHARACTERS".

r. "WR/RD WORD COUNT EXCESSIVE".

2-119. Explanation of Error Printouts. The error printouts, in alphabetical order, are explained in the following paragraphs. It has been noted that most printouts which are a result of operator error or a defective data tape cause error stops. In the explanation for each printout of this type, program recovery procedures are included. These printouts are items a, b, c, e, f, i, k, o, p, q, and r in the preceding list. The "DRUM NOT READY", "READ ABORT—TRACK", and "WRITE ABORT—TRACK" printouts can be due either to operator error, defective data tape, or an equipment fault. The "DRUM NOT READY" printout causes an error stop. The other two printouts do not cause a stop.

2-120. "BINARY PARAMETER EXCEEDS 72 CHARACTERS". This printout occurs after an attempt is made to read a binary test pattern from the data tape. The printout indicates that the test pattern on the tape is preceded by more than 72 blanks. To correct the situation, press the RUN switch repeatedly until the binary test pattern is reached on the tape. The printout will be repeated for every 72 blanks encountered on the tape.

2-121. "CHARACTER IN OCTAL PARAMETER ILLEGAL". This printout occurs after a faulty track or sector designation is furnished to the teleprinter or by a data tape. The printout indicates that the numerical portion of the designation contained one or more characters other than the digits 0 through 7. The printout is preceded by the first faulty character. To correct the error and restart the program, press the RUN switch, retype the faulty parameter, then press the RETURN and LINE FEED keys. If the incorrect designation was read from tape, set SWITCH REGISTER switch 15 to logic 0, press the RUN switch,

then type the correct parameter, set switch 15 to logic 1, and press the RETURN and LINE FEED keys. Correct the data tape, if this was the source of error.

2-122. "DRUM NOT READY". This printout indicates that the drum memory power supply is defective or not switched on, the drum is not up to operational speed, the wrong I/O select code was entered for the drum earlier in the program, or the drum ready status bit circuits are faulty. The program stops after the printout is furnished. When the situation is corrected, the diagnostic program can be resumed by pressing the RUN switch.

2-123. "ERROR BUSY STATUS BIT DURING WR/RD". This printout is furnished when the busy status bit is found to be "0" when it should be "1", or vice-versa.

2-124. "ILLEGAL CHARACTER IN TEST PATTERN PARAMETER." This printout occurs after a faulty binary test pattern is furnished, either manually or from the data tape. The printout indicates that one or more of the first 16 characters of the test pattern was a character other than "1" or "0", or that the 17th and/or 18th characters were not the letter "C" or a blank space. To correct the error and restart the program, follow the recovery procedure described in paragraph 2-121.

2-125. "IMPROPER CHARACTER IN WR/RD PARAM-ETER". This printout occurs after a faulty track or sector designation is furnished, either manually or from punched tape. The printout indicates that the "T", "S", "—", or "," portion of the designation was incorrect. To rectify the error and restart the program, follow the recovery procedure described in paragraph 2-121.

2-126. "READ ABORT — TRACK". This printout includes a 4-digit octal track number after the word "TRACK". The printout is furnished when the computer attempts to read from the drum and one of the following faults exists: overheated drum memory, drum memory power supply defective or not turned on, HEAD switch at the OUT position, or an attempt is made to read from a protected or nonexistent track. If the fault is the result of specifying a protected track, set the track protect switch to the down (nonprotect) position, provided the data in the track need not be saved. Then restart the program either from address 002000 (start of the entire program), or from 002042 ("BINARY TEST PATTERN ?" waiting loop). If the error was the result of specifying a nonexistent track, restart the program from 002000 or 002042, and specify only existing tracks. (Correct the data tape if this was the source of error.) If the drum memory power supply is overheated, off, or defective or if the HEADS switch is at the OUT position, make the necessary correction, and restart the program from 02000 or 02042.

2-127. "READ INTERRUPT MISSING DMA WORD COUNT = ". This printout includes a 6-digit octal number after the "=" sign. The printout indicates that after a read operation was initiated, no interrupt occurred within approximately 100 milliseconds. If a single group of consecutive sectors was being read, or if several groups of

sectors of the same size were being read, inspection of the DMA word count will indicate the number of words transferred into core memory before the failure occurred. The DMA word count in the printout is the 8's complement of the actual word count. If two or more groups of sectors of differing size were specified for reading, it is not possible to determine the number of words transferred into core memory because the group of sectors in which the failure occurred is not reported. As an exception, if the complement number indicates a sector group so large that it can only be the largest group specified, the determination can be made. If the failing sector group cannot be determined, rerun the read/write test several times, specifying each time only one of the sector groups.

2-128. "READ PARAMETER INCOMPLETE". This printout occurs after a faulty track or sector designation is furnished, either manually or from a data tape. The printout indicates that the numerical portion of the designation contained the wrong number of digits. To correct the error and restart the program, follow the recovery procedure described in paragraph 2-121.

2-129. "READ PARITY ERROR". This printout indicates that a drum parity error was detected while reading a word from the drum. With regard to this type of failure, it should be noted that a parity error can occur as a result of power-line noise. (Safety measures relating to the amount of electrical noise that can be bypassed to ground prevents complete filtering of line noise.) Most programs use a read loop to avoid difficulty from parity errors of this type. In the read loop, the word is read several times if a parity error occurs, in an attempt to obtain a good reading. In the read/write test, however, a word is read only once.

2-130. "READ SECTOR BUFFER OVERFLOWED". This printout occurs after a faulty sector designation is furnished, either manually or from the data tape. The printout indicates that more than 128 (200₈) sector groups were specified. To correct the error restart the program from address 002000 (start of the entire program), or from 002042 ("BINARY TEST PATTERN ?" waiting loop), and specify fewer sectors. Correct the data tape, if this was the source of the error.

2-131. "TRACK XXXX SECTOR XX WORD NO. XX OUTPUT XXXXXX INPUT XXXXXX" (where X is an octal digit). This printout is furnished when a comparison error occurs. That is, when a word read from the drum is not the same as the word that was stored on the drum. The track, sector, and word number are stated. The word written ("OUTPUT") and the word read ("INPUT") also are specified, using octal notation.

2-132. "WRITE ABORT — TRACK". This printout includes a 4-digit octal track number after the word "TRACK". The printout has the same significance as the "READ ABORT — TRACK" printout, except that it occurs as the result of a write operation. Recovery procedures are the same as for the read operation.

2-133. "WRITE INTERRUPT MISSING DMA WORD COUNT = ". This printout includes a 6-digit octal number after the "=" sign. The printout has the same significance as the "READ INTERRUPT MISSING DMA WORD COUNT = " printout, except that it occurs as the result of a write operation. The DMA word count printed is the 8's complement of the number of words that have been read from core memory and stored on the drum.

2-134. "WRITE PARAMETER INCOMPLETE". This printout has the same significance as the "READ PARAMETER INCOMPLETE" printout, except that it occurs as the result of a write operation. Recovery procedures are the same as for the read operation.

2-135. "WRITE SECTOR BUFFER OVERFLOWED". This printout has the same significance as the "READ SECTOR BUFFER OVERFLOWED" printout, except that it occurs as the result of a write operation. Recovery procedures are the same as for the read operation.

2-136. "WR/RD WORD COUNT EXCESSIVE". This printout occurs after a faulty sector designation is furnished, either manually or from the data tape. The printout indicates that a data transfer block specified was in excess of the maximum size permitted (refer to table 1-3). Recover procedures are the same as those specified in paragraph 2-130.

2-137. "WR/RD PARAMETER EXCEEDS 72 CHARACTERS". This printout occurs after a test parameter has been typed past column 72 of the teleprinter. For program recovery, refer to paragraph 2-104, then press the RUN switch, and type the test parameter in the correct manner. Correct the data tape if this was the source of error.

2-138.   SECTOR TIMING TEST.

2-139.   TEST DESCRIPTION.

2-140. The sector timing test determines whether sector timing pulses are being counted correctly. These pulses occur in pairs, and if one or both pulses in a pair are not counted, the selection of tracks and sectors will not be made correctly.

2-141.   TEST METHOD

2-142. The sector timing test uses the same subroutine as the read/write test. However, drum addresses are specified in a different way. In the write or read track and sector designations, the tracks and sectors are specified in an overlapping manner. To illustrate, tracks and sectors might be specified in the following manner:

    a.   For writing, T0000—0040 and S00—40.

    b.   For reading, T0000—0040, T0000—0020, T0020—0020, T0007—0023 and S00—10, S04—30, S20—20.

2-143. If a sector timing error occurs, a word read from the drum will not be the same as the word supposed to be written at that address. Other kinds of error may also be detected since the read/write subroutine checks for various types of errors. The error printout will show the kind of error found. The absence of error printouts indicates that the test has been successfully passed.

2-144. In the sector timing test, the reading of all specified sectors in a track does not always take place in the same program pass in which the sectors were written. Therefore, since complement patterns are reversed each pass, the complement function must not be used when conducting the sector timing test.

2-145.   PRINTOUTS.

2-146. Printouts for the sector timing test are the same as for the read/write test. A sector timing error will give a printout of the type described in paragraph 2-131.

2-147.   POWER FAILURE TEST.

2-148.   TEST DESCRIPTION.

2-149. If the ac power furnished to the drum memory power supply fails (drops to zero volts), information previously written on the drum should be intact after power is restored. If writing is taking place at the time of the power failure, only the tracks and sectors involved in the write operation should lose data.

2-150. The power failure test checks for the aforementioned results. The test consists of two portions — a read test and a write test. The read test ensures that after a power failure occurs, data previously written on the drum can be read back without error. The write test checks that when a power failure takes places during writing, only the tracks and sectors involved in the write operation are affected.

2-151.   TEST METHOD.

2-152. The power failure test uses the same subroutine as the read/write test. For the read portion of the power failure test, the read/write subroutine is used to store data in all tracks and sectors on the drum. Then the read/write test is looped in its read cycle. To produce a power failure, the drum memory power supply is turned off for a short time. Then, after the restoration of power, the read loop is restarted to determine whether read errors take place. At the moment power is removed, read errors may occur. This is normal.

2-153. For the write portion of the test, a write loop is established in which one sector of one track is written on. The test word is the same as that used in the preceding read portion of the test; consequently, all tracks and sectors other than that being written on will contain the same word that is being written. While the write loop is operating,

power is removed and restored. Then, a read/write test is initiated in which writing is suppressed and all tracks and sectors are specified for reading. The test word is the same as before. Because of the suppressed writing, no change is made to the data on the drum in the write cycle, and during the read cycle the test word is compared with the words in all tracks and sectors. If comparison errors occur, they should be for only the track and sector in which writing was taking place at the time of power removal. At the moment power is removed, write errors may be indicated. This is normal.

2-154.   PRINTOUTS.

2-155.   Printouts for the power failure test are of the same type as occur during the read/write test. During either the read or write portions of the power failure test, error printouts may occur when power is removed. These are not an indication that corrective measures are needed. The printouts will be one or more of the following:

a.   "READ ABORT — TRACK" (followed by a track number).

b.   "READ INTERRUPT MISSING".

c.   "WRITE ABORT — TRACK" (followed by a track number).

d.   "WRITE INTERRUPT MISSING".

e.   "PARITY ERROR".

f.   "DRUM NOT READY".

2-156.   Printouts which are an indication of equipment fault occur only after the restoration of power. For both the read and the write portions of the test, these printouts are of the type described in paragraph 2-131. In the case of the power failure write test, this printout is not an indication of equipment fault if it specifies the track and sector being written on when power was removed.

2-157.   PREPARATION OF DATA TAPE.

2-158.   A data tape for the drum diagnostic program contains test pattern words, track designations, and sector designations in ASCII code. A complete check of the drum read and write capabilities requires test parameters for the read/write test, the sector timing test, and the power failure test. For the complete check, the read/write test should use two or more test words, and these must be written and read in all tracks and sectors. A total of at least three read/write cycles should be conducted with these test words. The last test word used should be the worst-case word, which is 1100110011001100CC.

2-159.   For the complete check, two or more additional sets of test parameters should be provided for the sector timing test, each set specifying different overlapping tracks

and sectors. One pass with each set of parameters is an adequate test of sector timing. Complement patterns must not be used.

2-160.   For the power failure test, three sets of parameters are required. The first set must write and read a test word, such as 1100110011001100, in all tracks and sectors. Complement patterns must not be used. The second set must write the same test word in one sector of one track; reading can be suppressed in this parameter, although this is not essential. The third set of parameters for the power failure test must use the same test word as before, must suppress writing, and must read all tracks and sectors.

2-161.   Test parameters are punched on the tape in the same sequence used for manual teleprinter entry of data. That is, a test word is furnished, followed by a write track designation or designations, write sector designation or designations, read track designation or designations, and read sector designation or designations.

2-162.   When the tape is made, a carriage return symbol and line feed symbol must follow the test pattern and each set of track or sector designations, just as with manual teleprinter entry of data.

2-163.   When specifying sectors to be written or read, the maximum data transfer block must not be exceeded. (Refer to tables 1-3 and 3-1.) For a 4K memory, all sectors in a track can be specified as follows: S00—16, S16—16, S34—04.

2-164.   Three to four inches of leader should be allowed on the data tape. This will provide a program stop before the first set of data on the tape is used, allowing an opportunity to set the track protect switch to the non-protect position in the event that the track address test was bypassed. However, it is recommended that the track address test not be omitted when a data tape is used.

2-165.   Figure 2-1 is a printout of a typical data tape. The tape is prepared for a 1400—track drum and a core memory of 8K or greater capacity. The blank lines, 3rd and 5th from the bottom, result from pressing the space bar, RETURN key, and LINE FEED key, for suppressing reading and writing in the power failure test.

2-166.   Each set of five lines in the printout (figure 2-1) provides one set of parameters for the read/write test. The five lines contain the following information:

a.   The first line specifies the test pattern. This consists of a 16-bit test word, followed by "C's" and spaces, to make a total of 18 characters. The first C, if used, specifies alternate-word complementing. The second C, if used, specifies alternate sector complementing.
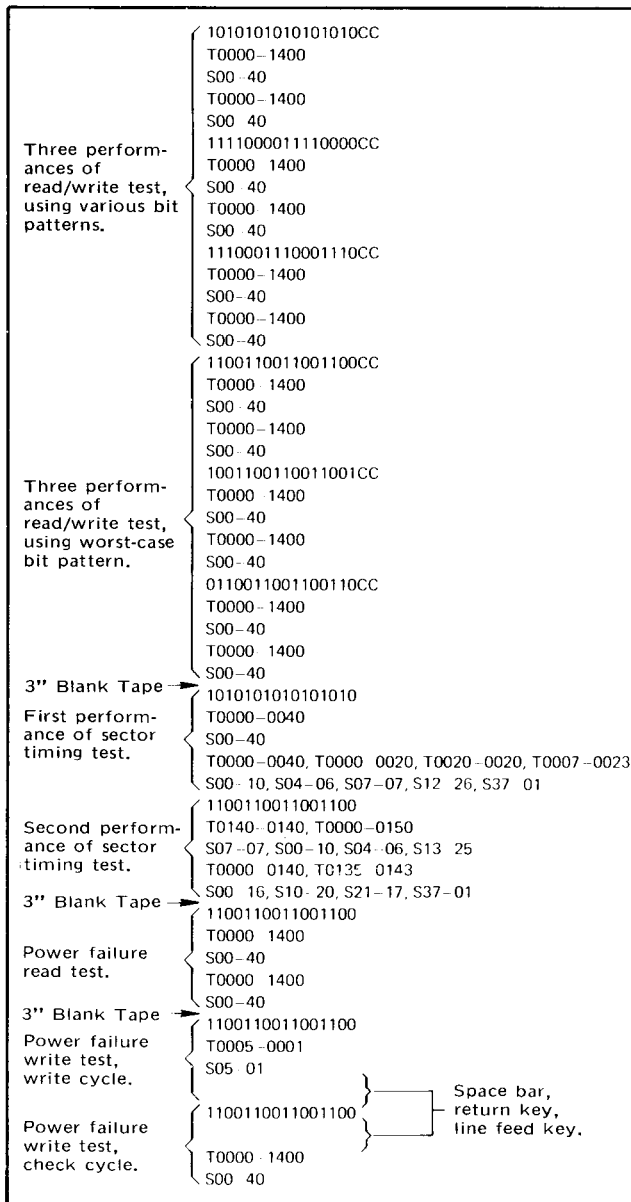
	1010101010101010CC
	T0000 – 1400
	S00 40
	T0000 – 1400
	S00 40
Three perform-	111100001 1 10000CC
ances of	T0000 1400
read/write test,	S00 40
using various bit	T0000 1400
patterns.	S00 40
	1110001 110001 110CC
	T0000 – 1400
	S00 – 40
	T0000 – 1400
	S00 – 40
	1100110011001100CC
	T0000 1400
	S00 40
	T0000 – 1400
	S00 40
Three perform-	10011001 10011001CC
ances of	T0000 1400
read/write test,	S00 – 40
using worst-case	T0000 – 1400
bit pattern.	S00 – 40
	01100110011001 10CC
	T0000 – 1400
	S00 – 40
	T0000 1400
	S00 – 40
3" Blank Tape →	1010101010101010
First perform-	T0000 – 0040
ance of sector	S00 – 40
timing test.	T0000 – 0040, T0000 0020, T0020 – 0020, T0007 – 0023
	S00 10, S04 – 06, S07 – 07, S12 26, S37 01
Second perform-	1100110011001100
ance of sector	T0140 0140, T0000 – 0150
timing test.	S07 – 07, S00 – 10, S04 – 06, S13 25
	T0000 0140, T013C 0143
3" Blank Tape →	S00 16, S10 20, S21 – 17, S37 – 01
	1100110011001100
Power failure	T0000 1400
read test.	S00 – 40
	T0000 1400
3" Blank Tape →	S00 – 40
Power failure	1100110011001100
write test,	T0005 – 0001
write cycle.	S05 01
Power failure	1100110011001100
write test,	
check cycle.	T0000 1400
	S00 40

Space bar, return key, line feed key.

Figure 2-1. Printout of Typical Data Tape

b. The second line identifies, in octal notation, the first drum track and the quantity of drum tracks on which writing will take place.

c. The third line identifies, in octal notation, the first sector and the quantity of sectors on which writing will take place. These sectors will be written on in all tracks designated in line 2.

d. The fourth line identifies, in octal notation, the first drum track and the quantity of drum tracks which will be read.

e. The fifth line identifies, in octal notation, the first sector and the quantity of sectors which will be read.

2-167. About three inches of blank tape is left at three places on the data tape. These portions of the tape may be either unpunched, or can contain space bar symbols. Each of the three blank areas causes a program halt when the computer attempts to acquire the next set of test parameters from the tape. The program is restarted by pressing the PRESET switch, then pressing the RUN switch repeatedly until the next set of parameters is reached on the tape. The first of the program stops serves to indicate that the read/write tests are finished and the sector timing tests are about to start. The second halt indicates that the power failure read test is about to start, and provides an opportunity for setting SWITCH REGISTER switch 2 to logic 1 for read looping. The third stop indicates that the power failure test is about to start.

2-168. In the example tape, the read/write test is performed three times with the worst-case bit pattern. To obtain maximum effectiveness, the bit pattern is rotated each time it is punched on the tape.

SECTION III

TEST PROCEDURES

3-1. INTRODUCTION.

3-2.   This section describes operating procedures for the drum diagnostic program. Before running the program, the operator should be familiar with sections I and II of this manual supplement.

3-3.   The diagnostic program has considerable flexibility, and can be run in various ways. The procedures described in this section are the simplest and most straightforward method of running the program. After the user has become familiar with the methods described, variations can be introducted to shorten the time required to achieve a particular test.

3-4. REFERENCE INFORMATION.

3-5.   OPERATING DATA.

3-6.   For running the diagnostic program, information concerning the computer system is required. This information should be listed in table 3-1, where it will be readily accessible to all users of the diagnostic program. Use pencil when filling in the reference table, as this will allow changes to be easily made if the computer system is modified.

3-7.   The time per pass listed in table 3-1 depends on the number of tracks on the drum and the type of computer used. For the read/write test, the maximum time is the time required for writing and reading all sectors of all tracks. If fewer tracks and sectors are involved, the running time is reduced proportionately. The running times will be increased by the time required to insert test parameters and by delays due to printouts and error stops.

3-8.   In the read/write test the execution of read passes and write passes can be determined from the P-register indicator lamps. The lamps flicker more brightly during a read cycle than during a write cycle. In the case of the 2114B Computer, which has no P-register display, the effect can be observed in the M-register display.

3-9.   CONTROLS AND INDICATORS.

3-10.   Table 1-5 gives the locations of controls and indicators used in running the drum diagnostic program.

3-11.   The functions of SWITCH REGISTER switches are described in table 2-1.

Table 3-1. Reference Data

DATA	1ST DRUM	2ND DRUM (IF ANY)	3RD DRUM (IF ANY)
Size of computer memory*			
SIO teleprinter driver tape no.*			
Teleprinter I/O select code*			
SIO punched-tape reader driver tape no.*			
Punched-tape reader I/O select code*			
Track-protect switch card slot			
DMA channel used by drum			
Drum I/O select code (octal)			
Number of protected tracks (octal)			
Total number of drum tracks (octal)			
Maximum data transfer block (sectors, octal)*			
Time per pass, track protect test			
Time per pass, track address test			
Maximum time per pass, read/write			
Maximum time per pass, write only			
Maximum time per pass, read only			
*Same for all drums used			

3-12.   DATA TAPE.

3-13.   The operating procedures presented in this section include operation both with a data tape and with manual entry of test parameters. The data tape is assumed to have been prepared in accordance with the example tape described in paragraph 2-157. This tape is intended for a 1400-track drum and a core memory of 8K or greater capacity.

3-14.   ERROR PROCEDURES.

3-15.   Operator error in entering test parameters on the teleprinter may result in a program stop. To recover from this type of stop, proceed as follows:

    a.   Press the PRESET switch.

    b.   Press the RUN switch.

    c.   The program repeats on the teleprinter its request for a test parameter.

    d.   Type the requested parameter.

    e.   Press the RETURN key.

    f.   Press the LINE FEED key.

    g.   The program resumes from the point at which it stopped.

3-16.   A defective data tape (a tape with illegal test parameters) will cause a program stop. To recover from this type of stop, proceed as follows:

    a.   Set SWITCH REGISTER switch 15 to logic 0.

    b.   Press the PRESET switch.

    c.   Press the RUN switch.

    d.   Type the required test parameter on the teleprinter.

    e.   Set SWITCH REGISTER switch 15 to logic 1.

    f.   Press the RETURN key.

    g.   Press the LINE FEED key.

    h.   The program resumes from the point at which it stopped.

3-17.   When an error printout is the result of an equipment fault detected by the diagnostic program, no program stop occurs. Action taken by the operator depends on the type of fault detected.

3-18.   Three types of error printout can be a result of either operator error or equipment fault. The first of these printouts is "DRUM NOT READY". This printout is always accompanied by a program stop. The two other printouts are "READ ABORT — TRACK" and "WRITE ABORT — TRACK". These are not accompanied by program stops. In the case of the "DRUM NOT READY" stop, the program can be resumed after the drum is ready by simply pressing the PRESET and RUN switches.

3-19.   Error printouts and error stops resulting from any cause can be eliminated by setting SWITCH REGISTER switch 3 to logic 1. As an exception, the "DRUM NOT READY" printout and its program stop are always executed.

3-20.   READ/WRITE SUBROUTINE.

3-21.   The read/write subroutine is used for the read/write test, the sector timing test, and the power failure test. In the read/write test at least three passes of the read and write portions of the subroutine must be performed in order to make a thorough test of the read and write circuits. All tracks and sectors must be written and read. Preferably, several test words should be used, including the worst-case bit pattern, which is 1100110011001100CC.

3-22.   For a check of sector timing, the sector timing test should be performed twice, each time with different test parameters.

3-23.   In the power failure test, each part of the test need be performed only once.

3-24.   A data tape normally is used for a complete check of the drum, furnishing data for the above tests for the required number of passes. Then, to assist in fault localization if an error occurs, the failing test can be repeated with manual data entry. The test can be repeated with read or write looping only, as indicated by the error printout symptoms, and using only the failing tracks and sectors.

3-25.   The read/write subroutine can be restarted from any point in the test by the following procedure:

    a.   If the program is running, press the HALT switch.

    b.   Set 002042 into the SWITCH REGISTER switches.

    c.   Press the LOAD ADDRESS switch.

    d.   Set all SWITCH REGISTER switches to logic 0.

    e.   Set SWITCH REGISTER switches for the test functions desired.

    f.   Press the PRESET switch.

    g.   Press the RUN switch.

    h.   The program prints "BINARY TEST PATTERN ?", and enters a waiting loop. Operations can then proceed with teleprinter entry of data, as described in paragraph 3-35.

3-26.   An alternative restart method is to return to the beginning of the track protect test. This is done by stopping the program, setting 002000 into the SWITCH REGISTER switches, and proceeding from step j of paragraph 3-28.

3-27.   PREPARATION AND LOADING.

3-28.   Preparation and loading of the diagnostic program is performed as follows:

a. If the computer is running, stop the program by pressing the HALT switch.

b. If the computer is off, turn it on by means of the POWER switch.

c. If the drum memory power supply is off, set the AC POWER switch to the ON (up) position, then set the DC POWER switch to the ON position. Wait for the drum to come up to speed. (The drum is at operational speed when the DRUM READY lamp goes out.)

d. Set the HEADS switch to IN.

e. With the basic binary loader, load the SIO teleprinter driver program. (Refer to table 3-1 for the teleprinter driver tape no.)

f. Configure the teleprinter driver program by entering the teleprinter I/O select code into the driver program.

g. If a data tape will be used, load the SIO punched tape reader driver program, using the basic binary loader. Then configure the tape reader driver.

h. With the basic binary loader, load the drum diagnostic program (tape no. 20340C). When the tape is loaded, the T-register should display "102077". If the T-register does not contain this number, reload the diagnostic tape and check the display again. Do not proceed until the T-register displays "102077".

i. If a data tape will be used, install it on the punched tape reader. Leave three to four inches of leader to the left of the read head.

j. Set 002000 into the SWITCH REGISTER switches.

k. Press the LOAD ADDRESS switch.

l. Set all SWITCH REGISTER switches to logic 0.

m. If the track address test is to be performed, set SWITCH REGISTER switch 11 to logic 1.

n. If looping is to be performed in the read/write test, set SWITCH REGISTER switch 0, 1, or 2 to logic 1, in accordance with the type of looping desired. (Refer to table 2-1 for switch functions.)

o. If switch register input of test words in the read/write test is desired, set SWITCH REGISTER switch 14 to logic 1.

p. If a data tape is to be used in the read/write test, set SWITCH REGISTER switch 15 to logic 1.

q. Set the track protect switch to the up (protect) position.

r. Set the ON LINE, OFF, LOC. switch to ON LINE. (On some models of teleprinter this switch is labeled LINE, OFF, LOC.)

s. Press the PRESET switch.

t. Press the RUN switch.

u. The program prints "DMA OCTAL CHANNEL # ?".

v. Manually type on the teleprinter the DMA channel number used by the drum. (Refer to table 3-1 for the channel number.)

w. Press the RETURN key. (On some models of teleprinter this key is labeled CARRIAGE RETURN.)

x. Press the LINE FEED key.

y. The program prints "HIGH PRIORITY OCTAL DRUM ADDRESS ?".

z. Manually type on the teleprinter the drum I/O select code. (Refer to table 3-1 for the select code.)

aa. Press the RETURN key.

ab. Press the LINE FEED key.

ac. The program enters the track protect test.

3-29.   TRACK PROTECT TEST.

3-30.   After the last item (line feed) is entered into the teleprinter for the preliminary procedures, the track protect test is conducted, as follows:

a. The program performs the test, and prints "NO. OF PROTECTED TRACKS — ", followed by a 4-digit octal number.

b. If the printout states the correct number of tracks, the track protect circuits are functioning normally. (Refer to table 3-1 for the correct number of protected tracks.) If the stated number of tracks is incorrect, an equipment fault exists. One pass through the test is an adequate check of the track protect circuits, unless an intermittent fault exists. Looping cannot be performed.

c. After printing the number of protected tracks, the program continues into the next test.

    (1) If the next test is the track address test (SWITCH REGISTER switch 11 is at logic 1), the program prints "NO. OF TRACKS ?", and enters a waiting loop.

    (2) If the next test is the read/write test using manual teleprinter entry of test parameters, the program prints "BINARY TEST PATTERN ?", then enters a waiting loop.

    (3) If the next test is the read/write test using switch register entry of test words, the program halts with "000271" in the P-register.

    (4) If the next test is the read/write test with data tape entry of test parameters, the program reads the blank leader on the data tape, prints "BINARY PARAMETER EXCEEDS 72 CHARACTERS", and halts with "002103" in the P-register.

3-31. TRACK ADDRESS TEST.

3-32. The following instructions explain how to perform the track address test. A single pass through the test is sufficient to reveal whether the drum addressing circuits are functioning properly, unless there is an intermittent fault. If an error is detected, looping can be used to assist in fault localization.

a. At the start of the test the program prints "NO. OF TRACKS ?", then enters a waiting loop.

b. Set the track protect switch to the down (non-protect) position.

c. If a single pass through the test is desired, set SWITCH REGISTER switch 11 to logic 0.

d. Manually type on the teleprinter the total number (octal) of tracks on the drum. (Refer to table 3-1 for the number of tracks.)

e. Press the RETURN key.

f. Press the LINE FEED key.

g. The program executes the track address test. If faults are detected, the program prints the appropriate error printout.

h. If looping was selected, the test can be ended by setting SWITCH REGISTER switch 11 to logic 0. The program then completes its current pass, and prints "TRACK ADDRESS CHECK COMPLETE" if no error was detected in any pass. The program then enters the read/write test. If looping was not selected, the program completes one pass through the test, prints "TRACK

ADDRESS CHECK COMPLETE" if no errors were detected, and enters the read/write test.

    (1) If the read/write test will use manual teleprinter entry of test parameters, the program prints "BINARY TEST PATTERN ?", then enters a waiting loop.

    (2) If the read/write test will use switch register entry of test words, the program halts with "000271" in the P-register.

    (3) If the read/write test will use data tape entry of test parameters, the program reads the blank leader on the data tape, prints "BINARY PARAMETER EXCEEDS 72 CHARACTERS", and halts with "002103" in the P-register.

3-33. READ/WRITE TEST, SECTOR TIMING TEST, AND POWER FAILURE TEST, USING DATA TAPE.

3-34. The procedure which follows employs a data tape similar to the tape shown in figure 2-1. The tape must suit the size of core memory in the computer and the number of tracks on the drum.

a. At the start of the read/write test, the program reads blank tape, prints "BINARY PARAMETER EXCEEDS 72 CHARACTERS", then halts.

b. Check that all SWITCH REGISTER switches except switch 15 are at logic 0.

c. If the track address test was bypassed, and writing is to be performed in protected tracks, set the track protect switch to the down (nonprotect) position.

d. Press the PRESET switch.

e. Press the RUN switch repeatedly until the first set of data on the tape is reached.

f. Acquiring six sets of test parameters from the data tape, the program performs six passes of the read/write test, one with each set of data. The last three sets of data use the worst-case bit pattern. All tracks and sectors are written and read in each of the six passes. If no error printouts occur, the read/write test is successfully passed.

g. The program attempts to acquire the next set of parameters from the data tape. encounters blank tape, prints "BINARY PARAMETER EXCEEDS 72 CHARACTERS", and halts.

h. Press the PRESET switch.

i. Press the RUN switch repeatedly until the next set of data on tape is reached.

j. Acquiring test parameters from the data tape, the program performs two passes of the sector timing test, each with different parameters. If no error printouts occur, the sector timing test is successfully passed.

k. The program attempts to acquire the next set of parameters from the data tape, encounters blank tape, prints "BINARY PARAMETER EXCEEDS 72 CHAR-ACTERS", and halts.

l.. Set SWITCH REGISTER switch 2 to logic 1.

m. Press the PRESET switch.

n. Press the RUN switch repeatedly until the next set of data on tape is reached.

o. The program acquires the power failure read parameters from tape, and after writing on all tracks and sectors, commences read looping.

p. When the P-register or M-register lamps indicate that read looping has started, set the AC POWER switch to the OFF (down) position.

q. The program prints "DRUM NOT READY", and halts. Other error printouts may precede "DRUM NOT READY".

r. Set the AC POWER switch to the ON (up) position.

s. Wait for the DRUM READY lamp to light and go out.

t. Press the PRESET switch.

u. Press the RUN switch.

v. Allow the test to cycle for at least one read pass. If word-comparison error printouts occur after the restoration of power, the read portion of the test has failed.

w. Set SWITCH REGISTER switch 2 to logic 0.

x. The program completes the current read pass, attempts to acquire the next set of parameters from the data tape, encounters blank tape, prints "BINARY TEST PARAMETER EXCEEDS 72 CHARACTERS", and halts.

y. Set SWITCH REGISTER switch 1 to logic 1.

z. Press the PRESET switch.

aa. Press the RUN switch repeatedly until the next set of data on the tape is reached.

ab. The program acquires the power failure write parameters from tape, and starts write looping. Since only one track and sector are being written, each loop requires only a fraction of a second.

ac. Set the AC POWER switch to the OFF (down) position.

ad. The program prints "DRUM NOT READY", and halts.

ae. Set the AC POWER switch to the ON (up) position.

af. Set SWITCH REGISTER switch 1 to logic 0.

ag. Wait for the DRUM READY lamp to light and go out.

ah. Press the PRESET switch.

ai. Press the RUN switch.

aj. The program acquires the power failure write test check parameters from tape. Allow time for the program to read all tracks and sectors at least once. Word-comparison errors should occur only for the track and sector being written on at the time of power removal. For the example test tape, these are track 0005, sector 05. If no other word-comparison errors occur, the power failure write test is successfully passed.

3-35. READ/WRITE TEST USING MANUALLY ENTERED DATA.

a. At the start of the test, the program either stops with "000271" in the P-register (if test words will be entered into the SWITCH REGISTER switches), or the program prints "BINARY TEST PATTERN ?" and enters a waiting loop (if test words will be entered manually into the teleprinter).

b. If writing is to be performed in tracks that can receive protect status, ensure that the track protect switch is in the off (down) position.

c. If the switch register will be used for input of test words, enter into the SWITCH REGISTER switches 64 test words in the sequence in which they are to be written in the drum sector or sectors. After setting up each word, press the LOAD MEMORY switch. When all words have been entered, the P-register will display "000371". Next, set all SWITCH REGISTER switches to logic 0 except as required for looping. Then, press the RUN switch twice.

d. If teleprinter input of the test word is to be used, manually type a 16-bit test word followed by two characters ("C's" and/or spaces) to indicate the kind of complementing to be performed. The first "C" is for alternate-word complementing, the second for alternate-sector complementing. Check that the SWITCH REGISTER switches are set for the type of looping to be performed, press the RETURN key, then press the LINE FEED key.

e. For either type of test word entry method, the program next prints "WRITE TRACKS ?", then enters a waiting loop.

f. Manually type one or more track designations. If no writing is to be performed, press the teleprinter space bar once.

g. Press the RETURN key.

h. Press the LINE FEED key. If writing was suppressed in step "e", operations continue at step "l" below.

i. The program prints "WRITE SECTORS?", then enters a waiting loop.

j. Manually type one or more sector designations.

k. Press the RETURN key.

l. Press the LINE FEED key. The program writes in the designation tracks and sectors.

m. The program prints "READ TRACKS?", then enters a waiting loop.

n. Manually type the same track designations that were typed in step "f" above. If only the space bar was pressed in step "f", enter the track designations to be read. If reading is to be suppressed, press the space bar.

o. Press the RETURN key.

p. Press the LINE FEED key. If reading was suppressed in step "n", operations continue at step "u" (no looping) or "v" (looping).

q. The program types "READ SECTORS?", then enters a waiting loop.

r. Manually type the same sector designations that were typed in step "j" above. If writing was suppressed in step "f", enter the sector designations to be read.

s. Press the RETURN key.

t. Press the LINE FEED key.

u. If looping was selected, operations proceed as described in step "v". If looping was not selected, the program performs a single pass through the read/write test. If faults are detected, error printouts are provided. If no faults are detected, no printout is furnished. If SWITCH REGISTER switch 14 is at logic 0, after completing the pass the program returns to the beginning of the sub-routine, prints "BINARY TEST PATTERN?", and enters a waiting loop. If switch 14 is at logic 1, the program stops. To repeat the read/write test with another set of parameters, the operator returns to step "c" or "d" above. To perform the sector timing test, the operator proceeds to the procedure described in paragraph 3-36.

v. If looping was selected, the program performs the type of looping specified. If faults are detected, error printouts are provided. If no faults are detected, no printout is

furnished. To transfer to a different type of looping, first set to logic 1 the SWITCH REGISTER switch for the type of looping desired. Then set to logic 0 the SWITCH REGISTER switch for the type of looping to be ended. To end all types of looping, set to logic 0 the SWITCH REGISTER switch for the type of looping being performed; the program then completes its current pass, returns to the beginning of the subroutine, and either stops (if SWITCH REGISTER switch 14 is at logic 1) or prints "BINARY TEST PATTERN ?" and enters a waiting loop (if switch 14 is at logic 0). To repeat the read/write test with a different set of test parameters, the operator returns to step "c" or "d" above. To perform the sector timing test, the operator proceeds to the procedure described in paragraph 3-36.

3-36. SECTOR TIMING TEST USING MANUALLY ENTERED DATA.

3-37. The sector timing test with manually entered test patterns and drum addresses is conducted in the same general manner as the manual read/write test. However, overlapping track and sector numbers are used. This results in a greater time per pass than otherwise would be the case. Complement test patterns must not be used. The test cannot be performed with write-only cycling.

3-38. When performing the sector timing test, suitable test parameters are as follows:

a. Binary test pattern 1010101010101010 (no complementing).

b. Write tracks T0000—0040.

c. Write sectors S00—40.

d. Read tracks T0000—0040, T0000—0020, T0020—0020, T0007—0023.

e. Read sectors S00—10, S04—06, S07—07, S12—26, S37—01.

3-39. A second set of parameters suitable for the sector timing test is the following:

a. Binary test pattern 1100110011001100 (no complementing).

b. Write tracks T0140—0140, T0000—0150.

c. Write sectors S07—07, S03—07, S00—07, S13—25.

d. Read tracks T0000—0300.

e. Read sectors S00—16, S10—20, S21—17, S37—01.

3-40. The absence of word-comparison error printouts indicates that the sector timing test has been successfully completed.

3-41.   POWER FAILURE TEST USING MANUALLY ENTERED DATA.

3-42.   The following instructions explain how to perform the power failure test using manually entered test words and drum addresses. Complement test patterns must not be used, and the same test word must be employed for the read and the write portions of the test. Typical test parameters are included with the instructions.

3-43.   Since the power failure test uses the read/write subroutine, basic operating procedures and error printouts are the same as for the read/write test. The test is performed as follows:

a.   Using the procedures employed for the read/write test, start read looping. Use 1100110011001100 as the test word, and read all tracks and sectors on the drum.

b.   When read looping is being conducted, set the AC POWER switch to the OFF (down) position.

c.   The program prints "DRUM NOT READY", then stops. Other error printouts may precede "DRUM NOT READY".

d.   Set the AC POWER switch to the ON (up) position.

e.   Wait for the DRUM READY lamp to light and go out.

f.   Press the PRESET switch.

g.   Press the RUN switch.

h.   Allow the test to cycle for at least one read pass.

i.   If word-comparison errors occur after the restoration of power, the read portion of the test has failed. If the read test is successfully passed, proceed with the write portion, as follows.

j.   Using the procedures employed for the read/write test, start write looping. Use the same test word as in the read portion of the test, and write on sector 5 in track 5.

k.   Set the AC POWER switch to the OFF (down) position.

l.   The program prints "DRUM NOT READY", then stops. Other error printouts may precede "DRUM NOT READY".

m.   Set the AC POWER switch to the ON (up) position.

n.   Set 002042 into the SWITCH REGISTER switches.

o.   Press the LOAD ADDRESS switch.

p.   Set all SWITCH REGISTER switches to logic 0.

q.   Wait for the DRUM READY lamp to go out.

r.   Press the PRESET switch.

s.   Press the RUN switch.

t.   The program prints "BINARY TEST PATTERN ?", and enters a waiting loop.

u.   Using the procedures employed for the read/write test, start a single read/write cycle with suppressed writing. Use the same test word as earlier in the power failure test, and read all tracks and sectors on the drum.

v.   If word-comparison error printouts occur after the restoration of power, they should specify only the track and sector in which writing was being conducted at the time of power removal. If other tracks and sectors have acquired erroneous data, the write portion of the test has failed.

3-44.   TEST TERMINATION PROCEDURE.

3-45.   After completion of the drum diagnostic program, proceed as follows:

a.   Set the track protect switch to the up (protect) position.

b.   Set the ON LINE, OFF, LOC. switch to OFF.