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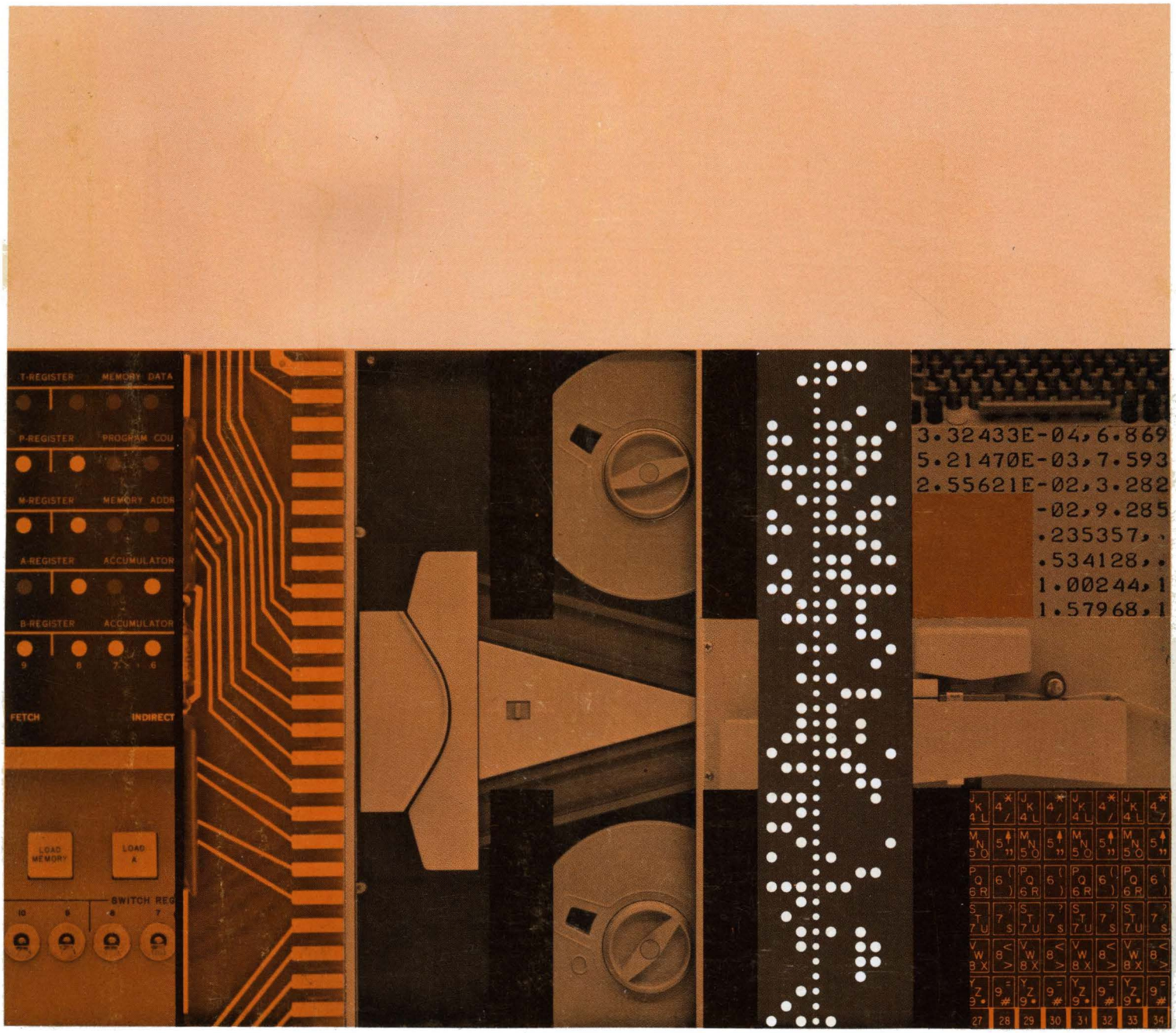
COMPUTER MAINTENANCE COURSE



VOLUME XVII

HP2114B CENTRAL PROCESSOR UNIT

HEWLETT-PACKARD

COMPUTER MAINTENANCE COURSE

VOLUME XVII

STUDENTS MANUAL

HP2114B CENTRAL PROCESSOR UNIT

(HP STOCK NO. 5951-1311)

-NOTICE-

The information contained in this manual is for training purposes only. Consult the Hewlett-Packard documentation supplied with the computer for current information concerning the specific computer system furnished.

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PREFACE

This training manual has been prepared to acquaint a service technician with the rudiments of maintaining the Hewlett-Packard 2114B. It is assumed that the user possesses a basic understanding of programming and of digital computer service.

The document is intended to supplement the Operating and Service Manuals supplied with the computer. These manuals should be consulted for schematics and other technical information appropriate to the particular unit being maintained.

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SECTION I
INTRODUCTION

1-1. PURPOSE OF 2114B COMPUTER.

1-2. The Hewlett-Packard Model 2114B Computer is a small general purpose digital computer which combines performance and economy with small size. The HP 2114B has full compatibility with HP data measuring and recording instruments as well as a wide range of input/output devices. The HP 2114B is subject to rigid operational and environmental specifications. The logic design and software follow conventional standards of computer usage and notation so that the HP 2114B may also be used as a free-standing device in other types of systems, such as process control, media conversion, data reduction or communication systems. The hardware and software are specifically designed to permit interfacing of real-time devices (i.e., devices running asynchronously with respect to a program being run). The word length is 16 bits. The basic HP 2114B computer includes the processor unit (main frame) with 4,096-word memory.

1-3. PHYSICAL DESCRIPTION OF HP 2114B COMPUTER.

1-4. In detailing a physical description of the HP 2114B, the major assemblies that make up the computer are shown in Figure 1-1. The following assemblies will be emphasized as the course progresses.

a. PLUG-IN CARD ASSEMBLY — which contains Card assemblies A1 through A23 that make up the main portion of the Computer's Logic circuits. Each assembly is located on a separate printed circuit card which fits into the Computer's Card Cage.

b. DISPLAY ASSEMBLIES — The Display Board is directly connected to the back of the Front Panel Assembly. The display board contains driver circuits for the front panel lamps, and the sensing assemblies for the Switch Register. The display cable links the Display Board with the Computer's logic cards.

c. BACKPLANE ASSEMBLY — The Computer's Back Plane Assembly is located beneath the card cage and is directly accessed by removing the bottom protective cover. The Back Plane contains power supply buses and interconnecting circuitry for the plug-in cards in the card cage.

d. POWER SUPPLY — The Computer power supply provides regulated DC voltages to the logic circuits, indicator lamps and other computer circuitry.

e. 4K CORE MEMORY ASSEMBLY — The Core Memory Assembly is located behind the card cage on the left hand side of the computer. The core stack makes up the computer's memory storage.

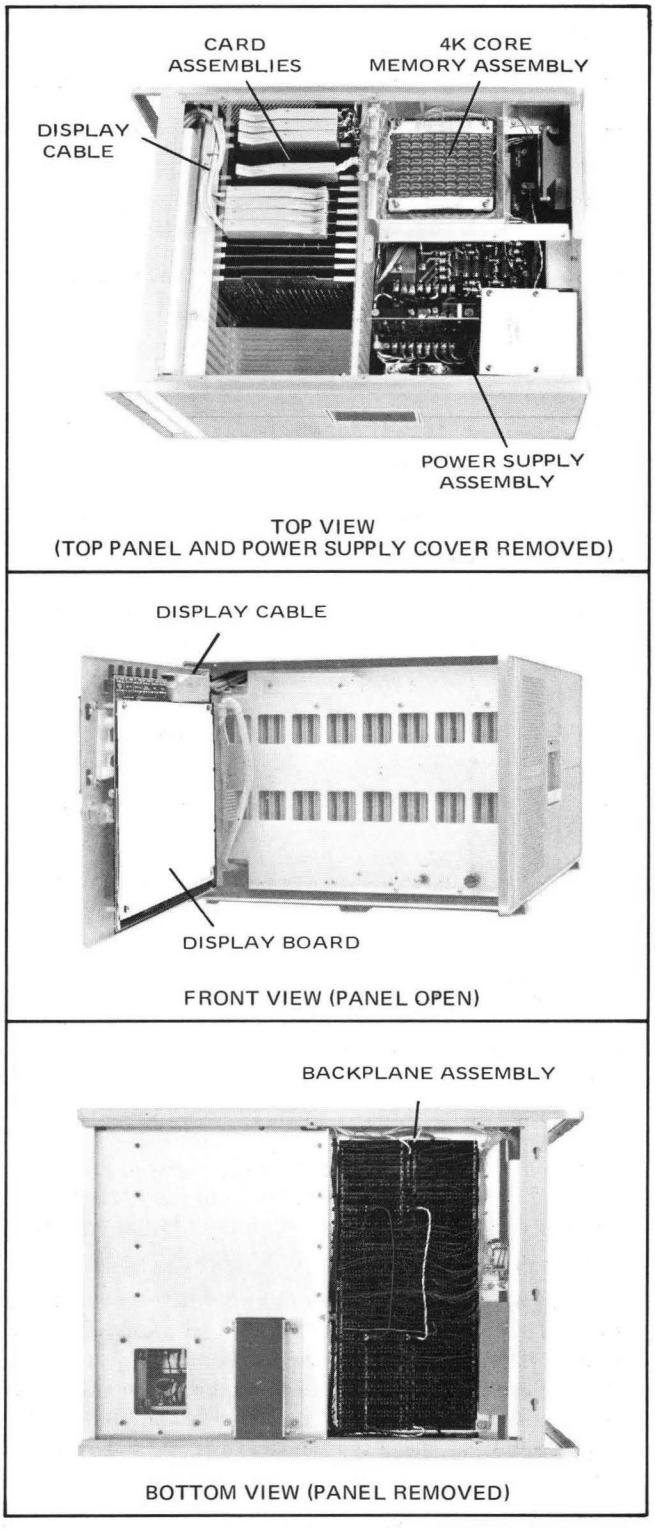


Figure 1-1. HP2114B

f. FRONT PANEL ASSEMBLY — Contains the display registers, Switch Register and Control Switches for the HP 2114B.

Table 1-1. Major Computer Assemblies

REFERENCE	ASSEMBLY	QUANTITY	NOMENCLATURE
A1,A2	02114-60427	2	Driver Switch Card
A3	02114-60429	1	Inhibit Driver Card
A6	02114-6005	1	Sense Amplifier Card
A8,A9,A10,A11	02114-60424	4	Arithmetic Logic Card
A12	02114-60426	1	Timing Generator Card
A13	02114-60425	1	Instruction Decoder Card
A14	02114-6003	1	Shift Logic Control Card
A15	02114-6007	1	I/O Control Card
A24	02114-6009	1	Display Board
A25	02114-6016	1	Display Cable
A400	02115-6042	1	4K Core Memory Assembly
—	02114-60391	1	Backplane Assembly
—	02114-6020	1	Power Supply Assembly
A300	—	1	Capacitor Board Assembly
A301	02114-6013	1	Heat Sink Assembly

1-5. OPTIONS.

1-6. Options for the HP 2114B Computer are of two general types:

a. Processor Options or options that allow for an increase in memory or in computation capabilities of the basic unit. Examples of such options are the additional 4K of memory or the Direct Memory Access Option now available with the HP 2114B.

b. Input/Output Options which add input and/or output facilities to the basic HP 2114B Computer. The options, identified by Interface Kit Numbers, provide the circuitry, cabling, and software to enable the computer to operate with a specific input or output instrument (measuring reading, or recording device), or with a series of instruments.

1-7. A total of seven (7) available I/O Slots are present in the main frame of the HP 2114B, but this can be extended by seventeen (17) more available slots through the use of the HP 2151A I/O Extender Option. A greater increase in the input/output capability of the HP 2114B can also be attained through the HP 12595A Multiplexed I/O option which provides for a possible fifty-six (56) extra I/O devices of customer design.

1-8. SOFTWARE.

1-9. Software is the totality of programs, routines, manuals, diagrams and operating insturctions. In the case of the HP 2114B, the software consists of the routines and materials supplied by the Hewlett-Packard Company which enables the computer to operate. The owner of a computer has three principal sources of runable programs:

a. The Manufacturer

b. User's Group Library

c. Proprietary, written by his own company.

1-10. When troubleshooting or repairing the HP 2114B all hardware problems should be solved first. Once the hardware confidence of the computer is high through hardware diagnostic testing and problems still exist in the computer a software check should be made. An attempt at the program conditions which initially failed to operate properly should be made, which, in turn, may prove to be the problem area. Unfortunately, it may prove to be the most difficult part for the technician because of the intimate marriage between the software and hardware. Trying to understand a strange program, which is probably not documented with flow charts and description, is difficult even for top notch technicians with wide experience. Solving a software problem like this is one of the highest compliments to a technician's expertise.

1-11. There are two methods of entering information into the HP 2114B Computer that the technician should know. Information can be entered into the computer either by toggling the routine into the computer with the use of the Switch Register and Control Switches on the Front Panel or through the use of peripheral Input devices such as the HP 2748A Tape Reader or the HP 2752A Teleprinter. The standard method for entering information into the HP 2114B is through the use of punched tapes since all standard HP Program Software is produced on punched tape for convenience to the customer.

1-12. LOGICAL TROUBLESHOOTING.

1-13. The operating computer system is rather complicated. There are certain techniques that the technician can use to simplify the troubleshooting problem. These techniques are covered in Section VII, Troubleshooting Procedures. These techniques allow the isolation of possible faults to smaller functional blocks.

1-14. Try to determine the nature of the difficulty from the person reporting a malfunction. Try to outline briefly the software program being used. How was it expected to

function? What were the actual results? Hopefully, problems associated with the misuse of hardware or simple operating errors can be detected at this point.

1-15. INTEGRATED CIRCUIT DESCRIPTION.

1-16. The logic type selected for use in the 2114B Computer is the TTL family. It requires only a +5.0 volt power supply and ground. The HP 1820-0956 CTL (Complementary Transistor Logic AND gate is used to buffer input and output levels for compatibility with the HP family of I/O interface devices. Refer to Table 1-2 for stock number and description.

1-17. The TTL family is a high speed saturating logic. Characteristics for the normal family follow. Typical pro-

Table 1-2. 2114B Integrated Circuit Components

HP STOCK NUMBER	DESCRIPTION	MFG. TYPE
1820-0054	*TTL Quad 2-input NAND	7400N
1820-0063	Dual 2-wide 2-input AND-OR-INV	7451N
1820-0065	J-K FF	7470N
1820-0068	Triple 3-input NAND	7410N
1820-0070	8-input NAND	7430N
1820-0071	Dual 4-input NAND	7440N
1820-0074	4-wide 2-input AND-OR-INV	7454N
1820-0075	Dual J-K Master/Slave FF	7473N
1820-0077	Dual D FF	7474N
1820-0084	4-wide 2-input AND-OR-INV Exp	7453N
1820-0085	Dual 4-input Exp	7460N
1820-0105	Linear Ckt Voltage Reg	SL6160
1820-0111	1 out of 10 Decoder	930159X
1820-0127	Quad 2-input NAND	900259X
1820-0129	Triple 3-input NAND	900359X
1820-0130	Dual 4-input NAND	900459X
1820-0132	Hex Inverter	901659X
1820-0183	Differential Amplifier	CA3028
1820-0233	Up/Down Counter	SN10625
1820-0301	Quad Latch Buffer (D FF)	7475N
1820-0305	Full Adder	7483N
1820-0310	DTL Triple 3-input NAND	15862N
1820-0327	Quad 2-input NAND	7401N
1820-0328	Quad 2-input NOR	7402N
1820-0370	HS Quad 2-input NAND	74H00N
1820-0371	HS Triple 3-input NAND	74H10N
1820-0372	HS Triple 3-input AND	74H11N
1820-0374	HS Dual 4-input AND	74H21N
1820-0377	HS Dual 2-input AND-OR-INV Exp.	74H50N
1820-0378	HS Dual 2-wide 2-input AND-OR-INV	74H51N
1820-0379	HS 4-wide 2-2-2-3-input AND-OR Exp.	74H52N
1820-0380	HS 4-wide 2-2-2-3-input AND-OR-INV Exp.	74H53N
1820-0381	HS 4-wide 2-2-2-3-input AND-OR-INV	74H54N
1820-0382	HS 2-wide 4-input AND-OR-INV Exp.	74H55N
1820-0383	HS Dual 4-input Expander	74H60N
1820-0384	Triple Dual 4-input Expander	74H61N
1820-0956	CTL Dual 2-input AND Buffer	SL3459

* Except DTL and CTL as noted.

pagation delay is 13nsec per gate and 40nsec per flip flop. Power dissipation is 10 MW per gate and 60 MW per flip flop. Operating temperature range is 0°C to 70°C which is more than adequate for the 2114B.

1-18. The logic is built around the NAND gate. Figure 1-2 is a sample of the circuit with approximate resistor values shown.

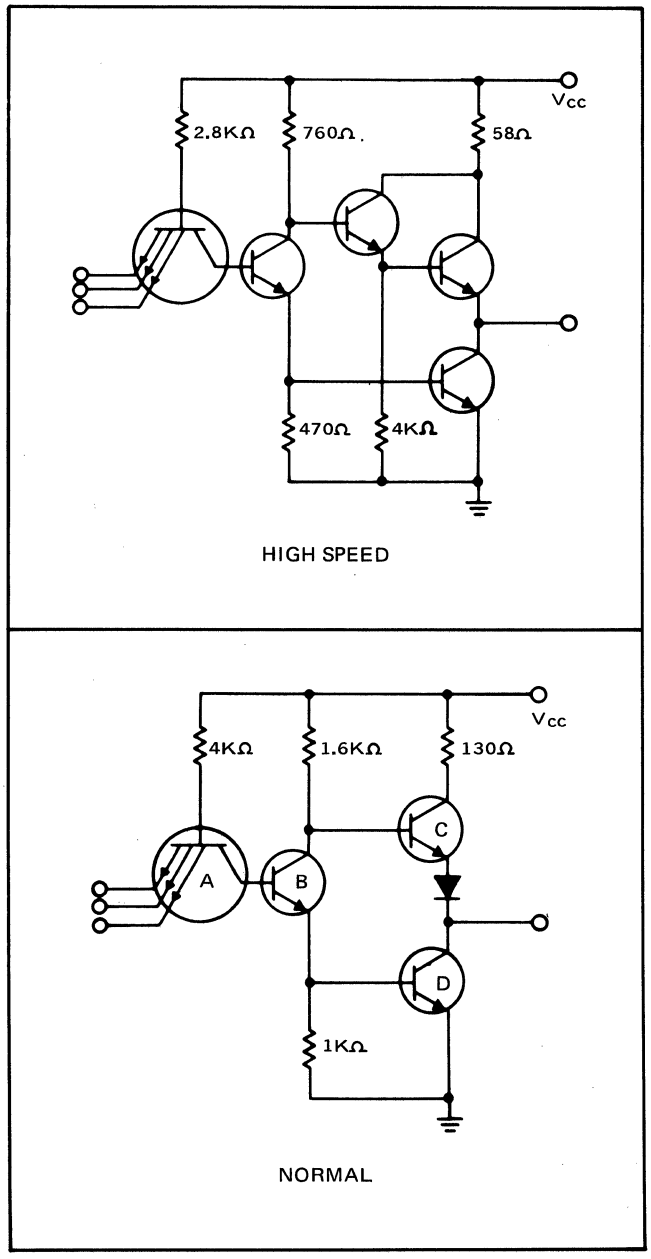


Figure 1-2. TTL "NAND" Basic Building Block

1-19. A high speed version is used in some applications where higher fan out or improved speed is necessary. The power requirement doubles and the propagation delay halves compared to the normal unit.

1-20. OUTPUT.

1-21. The totem pole output in the normal device gives a "one" output impedance of about 70 ohms. This helps provide good noise immunity. The logical "one" output has a guaranteed value of 2.4 volts minimum. Fan out, and drive criteria are based on a minimum of 2.0 volts which provides a noise immunity safety band.

1-22. The logical "zero" level is guaranteed at 0.4V maximum. Fan out and drive requirements are determined at 0.8V which provides a noise immunity safety band. An individual gate will normally change state as the input increases to about 1.4 volts.

1-23. CIRCUIT OPERATION.

1-24. The TTL family is designed around the basic NAND circuit. Any number of emitters can be provided in the input transistor. Any one of the emitters pulled down to a logical "zero" will saturate transistor A pulling the collector voltage down. This holds off transistor B. The output is pulled high by the 1.6K resistor pulling up on the base of transistor C.

1-25. When all emitters are at the logical "one" level transistor B base to collector junction acts like a diode. It pulls up the base of transistor B, and both B and D are conducting. The output goes low through saturated transistor D.

1-26. FAILURE.

1-27. The common failure modes include shorting in the output transistors which can hold the output either high or low. Failure in the input typically shorts emitter to emitter. This can pull an inter-connection bus high by virtue of the shorted emitters.

1-28. OR TYING.

1-29. The totem-pole output precludes OR tying gates together because of the current limitations corresponding to each integrated circuit. Each TTL integrated circuit added through OR tying the outputs together produces an additional load in parallel to the other TTL integrated circuits. This additional load which is in parallel with the other loads provided by other integrated circuits reduces the total load of the circuit thus allowing an increase in current draw. This increase in current will exceed the limitations of each TTL integrated circuit and will begin to "blow" I.C. packs. Figure 1-3 shows the open collector output (alongside the normal output). One quad 2-input NAND gate is made this way — HP Stock No. 1820-0327. It allows OR tying for negative true signals. It is used extensively in the 2114B logic design, refer to the Bus structure design on the Arithmetic Logic assembly.

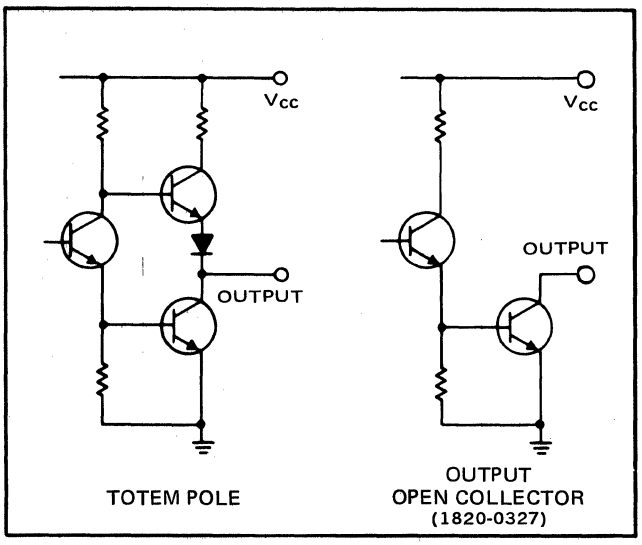


Figure 1-3. Open Collector

1-30. CTL COMPARISON.

1-31. The CTL family used extensively in Hewlett-Packard computers differs somewhat in characteristics from the TTL logic. It requires a +4.5V supply and a -2.0V supply. The input circuit is a transistor base with the tie down resistors to -2.0V or ground. The output is an emitter follower and can be OR tied in positive true direction. A logical "zero" output is -0.3 volts. A logical "one" output is +2.3 volts. (Refer to Figure 1-4.)

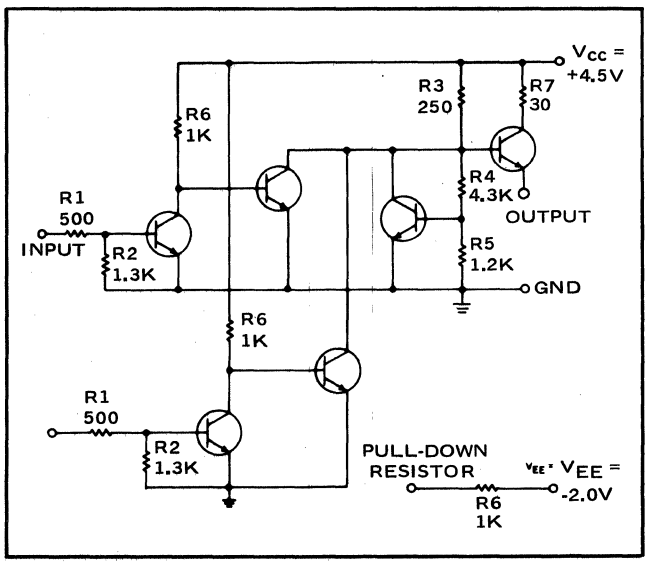


Figure 1-4. CTL Typical Circuit (1820-0956)

1-32. The use of the CTL integrated circuits in the HP 2114B is to allow "OR" tying in the positive true sense and to amplify signals that are sent to other sections in the computer.

1-33. TYPE D FF.

1-34. A commonly used TTL circuit is the 1820-0077 Dual D type positive edge triggered flip flop. The FF is made up of NAND gates as shown in Figure 1-5. The preset and clear signal inputs are both negative true. Either (or both) negative will inhibit the FF operation.

1-35. When preset and clear are both high the state of the D input establishes certain conditions. The change in the clock input from low to high state will complete the establishment of the FF state. A subsequent change of D input level (even with the clock remaining high) will not affect the FF output. Figure 1-5 shows the functional block diagram.

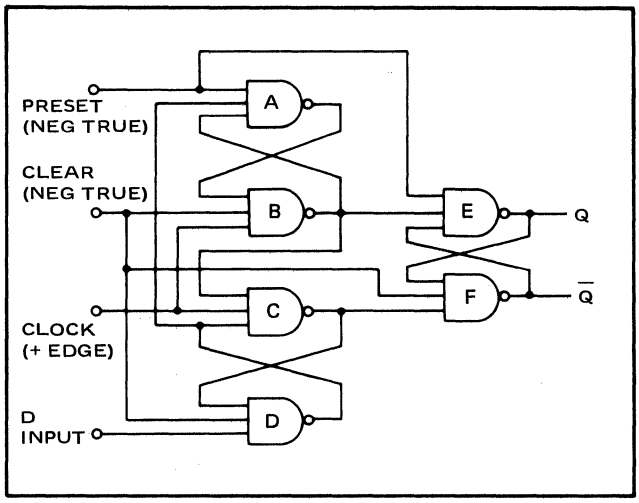


Figure 1-5. D Type Flip Flop (+ Edge Trigger)

1-36. AND-OR EXPANDERS.

1-37. Because of the OR tie limitations inherent in the totem pole output stage a family of expandable OR circuits was developed. The basic circuit is an AND-OR structure. The output may be true or inverting. The OR or NOR output stage may accept additional inputs. These are of two types. In one a single true input permits an additional OR, the other requires both true and complementary inputs for the additional OR input.

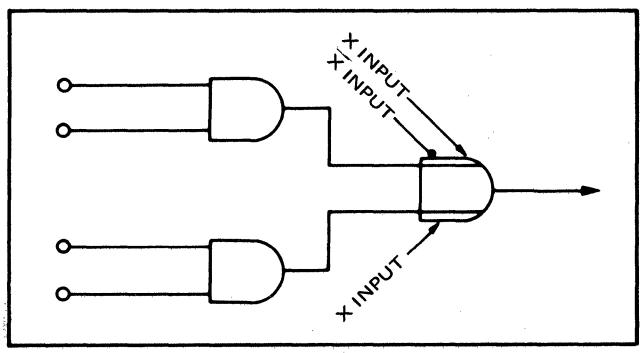


Figure 1-6. AND-OR Expander

1-38. BINARY FULL ADDER.

1-39. The Full Adder is used on the arithmetic logic assembly for arithmetic adding operations. The R and S buses and the carry in are compared two by two. If at least two are high a carry out (negative true) is generated.

1-40. If no carry out is generated either R, S, or Carry in can provide a T bus output. The presence of R, S, and Carry in will also generate a T bus output.

1-41. A glance at the adder circuit on the Arithmetic schematic will disclose that the R and S inputs are inverted in the second and fourth circuits, and the T bus output is inverted in the first and third. The polarity of the Carry out changes between each stage.

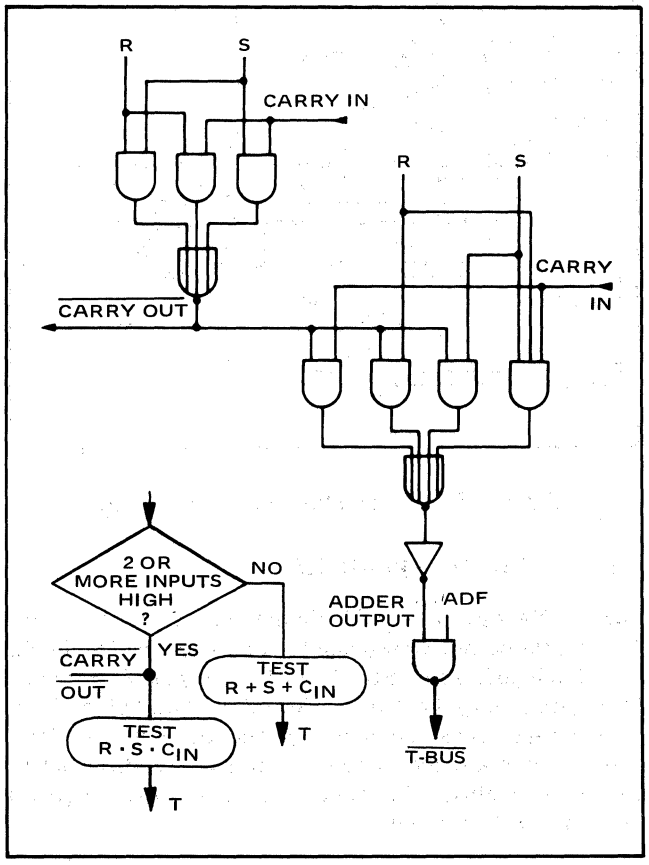


Figure 1-7. Binary Full Adder

1-42. The parallel add - serial carry requires a typical delay of 8 nsec per stage. Whenever the 2114B uses the full adder two timing cycles are used (500 nsec) to insure adequate time for completion.

1-43. "D" LATCH.

1-44. The flip flop follows the D input so long as the clock input is positive. The current FF condition is retained as the clock goes negative. HP Stock No. 1820-0301. Refer to Figure 1-8.

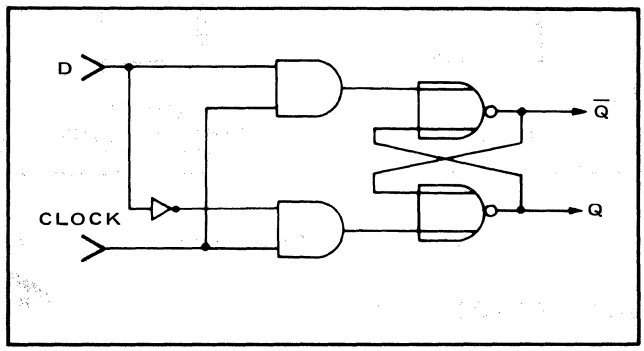


Figure 1-8. D Latch (1820-0301)

1-45. IC REPLACEMENT.

1-46. The replacement of Integrated Circuit packs on the Printed Circuit board requires care. Too much heat can "measle" the board ruining its appearance. Too much heat or aggressive mechanical manipulation can damage the plating around holes.

1-47. An effective way to replace an IC pack follows: Cut the body out. A sharp diagonal cutting pliers will allow cutting each leg individually. Remove each leg individually. Care must be exercised so that undue stress is not produced which might damage the plated hole. Use a light soldering iron with a tiny tip to remove each leg (from the component side). Each hole can be cleaned out with a round tapered toothpick (its size may have to be reduced to fit in the hole) or a vacuum device.

1-48. The new IC pack can be inserted, and carefully soldered. The rosin flux can be removed with Alpha cleaner (or other commercial product).

THE POWER SUPPLY

SECTION II
THE POWER SUPPLY

2-1. INTRODUCTION.

2-2. PHYSICAL CONSTRUCTION.

2-3. The physical parts of the power supply assembly consist of the rear panel of the instrument which houses the line filter, the fans and the voltage bus test points. The heat sink assembly contains those elements which dissipate significant amounts of power. The transformer, capacitor board and the capacitor assembly are mounted to the deck. The regulator board is a plug-in board containing the small components associated with the primary regulator, +20 volt regulator, and power fail detect circuitry. The outputs of the power supply are the voltage buses with wiring attached to the computer back plane. All cabling associated with the primary regulator and AC line is physically separated from the DC voltage bus cabling. This is a precaution for personnel safety.

2-4. The 2114B power supply is a 50-60 Hz, 115 volt AC input only. A step down transformer is required for operation from a 230 volt line. It is a dissipative type power supply. Any line voltage in excess of the minimum required is dissipated in the form of heat. This heat is dissipated primarily by those components situated on the heat sink.

2-5. The power supply consists of four basic sections:

a. The primary regulator establishes an input voltage of 83 volts to the primary of this transformer (T1).

b. The DC voltage buses are simply full wave rectifier, capacitor filter buses, and depend on the transformer turns ratio to determine the actual voltage.

c. The +20 volt regulator is a stable regulator with temperature compensation for the memory circuits.

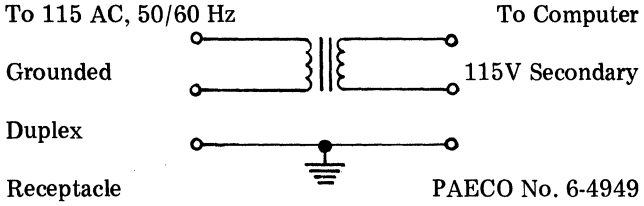
d. A power fail circuit senses power failure and also provides a turn-on delay.

2-6. The purpose of this lesson on the power supply will be to study the circuits and gain a familiarity with how they operate. It will discuss the safety precautions. A laboratory session will deal with wave shapes, troubleshooting and actual fault analysis.

2-7. EQUIPMENT FOR MAINTENANCE.

2-8. The equipment needed for the maintenance of the HP 2114B Power Supply is as follows:

a. Isolation Transformer
115V:115V 800 volt-amp capacity
(For 60 Hz operation only, 550 volt-amp will be adequate)



b. Variable AC Autotransformer 50/60 Hz, 7 amp.

c. Oscilloscope HP 180A or equivalent
HP 1801A Vert Amplifier
HP 1720 Time Base
HP 10004A Probes

d. Multimeter HP 427A
For +20V bus improved accuracy is desired such as HP 412A or HP 3430A.

WARNING

Dangerous voltages are present in the computer even when the Power Switch S1 is in the OFF position. Do not attempt to remove the protective cover of the Power Supply, or attempt maintenance of any kind in area of the Power Supply, unless the power cord has first been removed from the power source. Do not energize the Power Supply during servicing unless an isolation transformer is connected between the main power source and J1 at the rear of the Computer. Use caution when making test measurements. Failure to heed this warning could result in death or injury.

2-9. SAFETY PRECAUTIONS.

2-10. There are safety hazards associated with troubleshooting and maintaining this power supply which differ from typical power supplies. The primary regulator determines the AC level to the primary winding on the transformer. All of the circuitry associated with the AC line thus is hot (i.e., connected electrically to the AC line). The series regulators, the regulator board, and the voltage and overload current protection circuits are all superimposed on the AC line voltage. Utmost care must be used in troubleshooting. Fault analysis and repair should not be performed without using an isolation transformer which allows this primary regulator circuit to float. Thus any single point can be grounded and become a reference node. Without this isolation transformer it is extremely difficult to troubleshoot the primary regulator circuit.

2-11. Periodic inspection of the insulation and cabling, especially following the replacement of components will establish that the insulation is still intact. Faulty insulation may result in serious danger to personnel, and to equipment. The routing of the cables must not be disturbed which may lead to contact between AC regulator circuitry and DC buses.

2-12. CIRCUIT DESCRIPTION.

2-13. PRIMARY REGULATOR.

2-14. Figure 2-1, the block diagram of the Line Regulator, shows the 115 volt AC line supplying the transformer T1 winding and the series regulator circuitry. The winding design voltage is 83V AC. The series regulators absorb the excess voltage. Because it is not convenient to work with AC voltage in semi-conductor circuits a full wave bridge converts to pulsating DC. This allows the series regulators to be DC circuits instead of bi-polar.

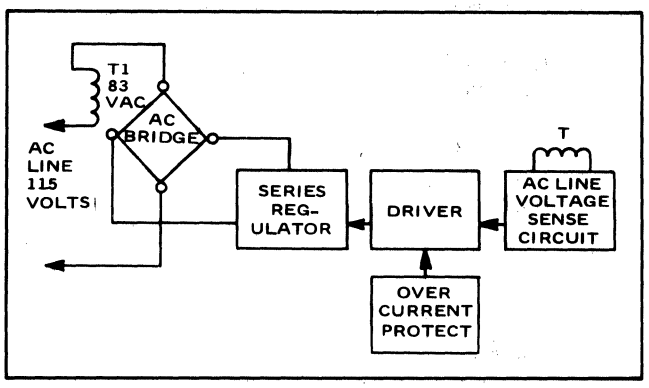


Figure 2-1. Line Regulator Block Diagram.

2-15. The series regulators require a driver for current amplification. The driver is controlled by two circuits: The AC line voltage circuit which establishes the 83 volts on the primary of the transformer, and the over-current protection circuit which prevents short circuits or other malfunctions from drawing excessive current through the series regulators.

2-16. A partial schematic of the primary regulator is shown in Figure 2-2. Capacitors C1 and C2 together with line filter FL1 provide noise filtering. Resistor R1 and capacitor C3, located in the Power Switch Turn-on Circuit, are used as an arc suppressor to prevent arcing caused by inductive kick-back from this primary of T1. This inductive kick-back from the primary windings will occur during turn-off and could possibly cause the Power Switch to burn up. R1 and C3 will protect against this burn up. Diodes CR1, CR2, CR3 and CR4 make up a full wave rectifier to convert the AC voltage to pulsating DC. The pulsating DC is applied to the series regulators made up of transistor Q1, Q2, Q3 and Q4. By controlling the current flow through the series regulator the voltage drop across the primary winding of transformer T1 is limited to a maximum of 83 volts. The series regulators are driven by Q5 which provides the required base current for regulation. The driver Q5 is in turn controlled by two circuits, the AC voltage sense circuit and the over current protection circuit.

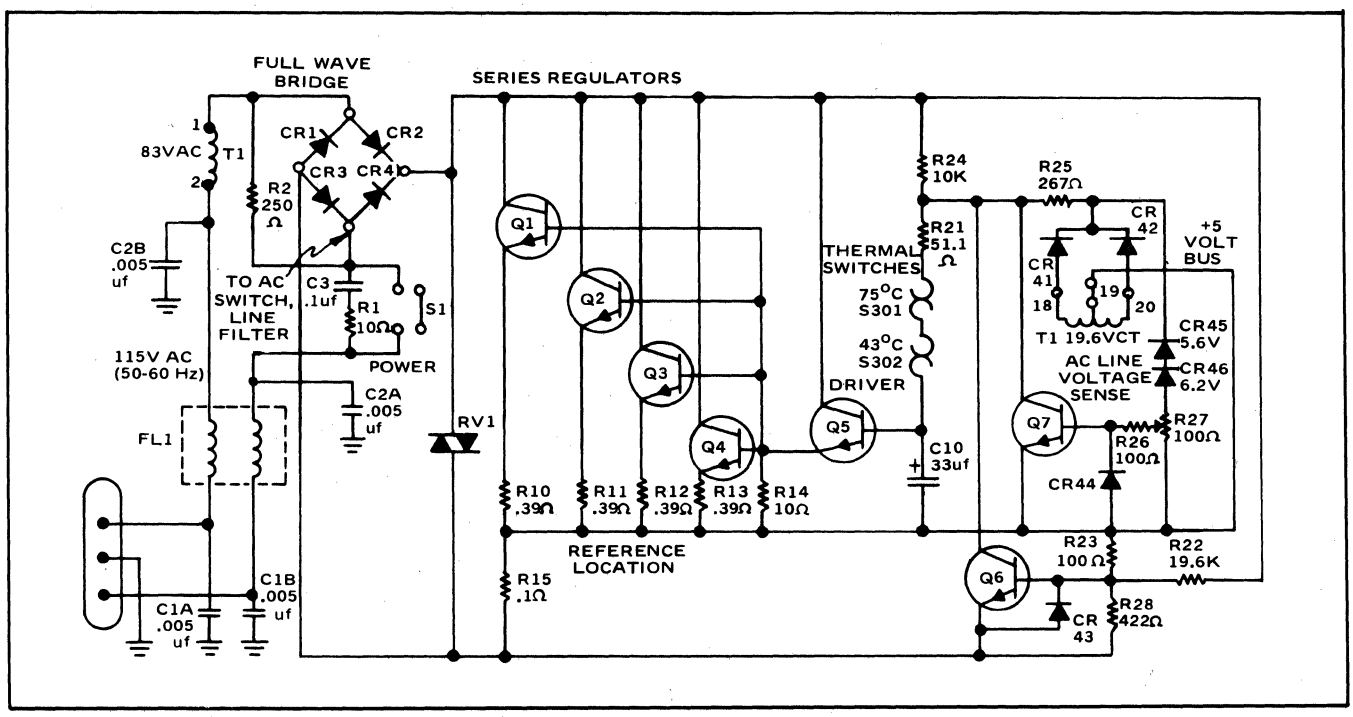


Figure 2-2. Primary Regulator

2-17. The varistor RV1 across the full-wave rectifier, CR1, CR4, protects against high voltage spikes. At voltages in excess of 140V RMS the varistor breaks down, providing a low impedance to high noise spikes or an essential short to the high noise spikes. With respect to high frequency spikes, capacitor C10 is used in conjunction with R21 to filter out high frequency noise that may occur into the base of the driving transistor Q5. This will prevent the primary regulator circuit from operating in a sporadic fashion upon the occurence of these high frequency spikes.

2-18. THE AC VOLTAGE SENSE CIRCUIT.

2-19. The AC Voltage Sense Circuit uses a separate transformer winding and diodes CR41 and CR42 provide full wave rectification for the sense voltage which is applied to the zener breakdown diodes CR45 and CR46.

2-20. The Zener diodes CR45 and CR46 will break down when 11.8V is sensed from the sense secondary. Transistor Q7 will begin to conduct at 12.4V causing a drop in the collector voltage. The voltage on the base of Q5 is reduced, reducing the base drive to the series regulators. The increased resistance of the series regulators causes the voltage applied to the primary to drop, maintaining the required 83 volts.

Note

The series regulators dissipate all power due to excess line voltage to the supply. This requires that the heat sink assembly and fan filters should be kept clean in order to allow propwer heat dissipation.

2-21. OVERCURRENT PROTECTION.

2-22. The operation of the overcurrent protection circuit is as follows: All of the line current must flow through resistor R15. When the voltage drop across R15 increases sufficiently, transistor Q6 is turned on and the collector voltage drop reduces the base drive to Q5 so as to limit current at this level. It requires approximately 10 amps peak (4.1 RMS) to initiate this overcurrent action. Resistor R22 provides base current to Q6 depending on the AC line voltage. This reduces some what the critical current through R15 at elevated line voltages, and helps limit the peak dissipation of the regulators.

2-23. PRIMARY REGULATOR – TROUBLESHOOTING.

2-24. ISOLATION TRANSFORMER.

2-25. It is necessary in troubleshooting the primary regulator that this circuit be isolated from the AC line. This is accomplished by using an isolation transformer. The isolation transformer should have a one to one ratio and be capable of handling 600 to 800 volt-amps. Such a large capacity is necessary because of the large peak to average currents in this supply. A transformer and variable AC autotransformer with less capacity may cause poor operation.

2-26. REGULATOR AND DRIVER SHORTS.

2-27. A convenient troubleshooting aid is to remove the primary regulator board. When this board is removed Q5 does not provide drive current and the line regulators remain off. There will be some voltage applied to the primary of the transformer because of the current path through resistor R2 (250 ohms). This provides sufficient primary current so that there will be 1.5 or 2 volts present on the 5 volt bus and proportional amounts on the other voltage buses.

2-28. There should be no current through the series elements Q1 to Q4. This can be determined by measuring the voltage drop across emitter resistors R10, 11, 12, and 13. (These are physically located on the Kingman board to the rear of the heat sink assembly.)

2-29. REGULATOR AND DRIVER OPEN CIRCUIT.

2-30. Operation of the Regulator transistors can be checked without the regulator board by providing base drive. Use the isolation transformer and variable AC autotransformer in the line. Start with the AC autotransformer turned all the way down. Turn on Driver Q5 by connecting its base (+ terminal of C10 on Kingman Board) to the collector of Q1 or Q2 (on top side of heat sink) through a 1K resistor (1/4W ok). Use common node of R10-R15 for scope ground.

WARNING

This provides full line voltage to T1 primary. The line voltage should not exceed 85 to 90 volts. Now it is necessary to protect the power supply manually. You no longer have voltage or overcurrent protection. This requires that the input AC line slowly be increased with the variable AC autotransformer while carefully monitoring both voltage and current of the line. This procedure will establish that the regulators, driver, and AC bridge are capable of proper operation. Operation of the 5V bus should be an adequate indication. The above procedure will provide 5 volts DC with 0.3V P to P ripple at 85V AC Line.

2-31. WAVESHAPES.

2-32. With the regulator board installed viewing waveshapes in the AC voltage sense and overcurrent circuits is a powerful troubleshooting aid. Specific changes take place as a function of line voltage. Use variable AC autotransformer and isolation transformers.

2-33. The regulator voltage (collector Q1 to R15) will have spikes as the AC line crosses zero voltage (figure 2-3). They are caused by the transformer flux decay as the diode bridge ceases to conduct. The voltage level is stable and they re-

peat each 8.3 milliseconds. As the voltage is increased to 85V the regulators will begin to show a voltage peak. This collector voltage increases to 60V peak-to-peak at high line.

2-34. The collector waveshape of Q7 increases until at 83V line voltage it develops a dip. (Refer to Figure 2-4.) The increased base drive to Q7 (with increasing line voltage) results in the collector dropping to a level which maintains the 83V input to T1.

2-35. THERMAL SWITCHES.

2-36. The computer power supply could be damaged by an increase in ambient temperature. Thermal Switches S301 and S302 provide protection by shutting off the base drive to the series regulators and effectively turning the power supply off. Thermal Switch S302 is set to open at 43° centigrade and is located in the air stream directly behind fan B1. Thermal Switch S301 is set to open at 75° centigrade and is located on the heat sink assembly.

2-37. HEAT DISSIPATION.

2-38. It is important that the filters on the fan assemblies be checked and cleaned as necessary at frequent intervals.

2-39. At high line and maximum current each transistor must dissipate over 100 watts peak. To accomplish this,

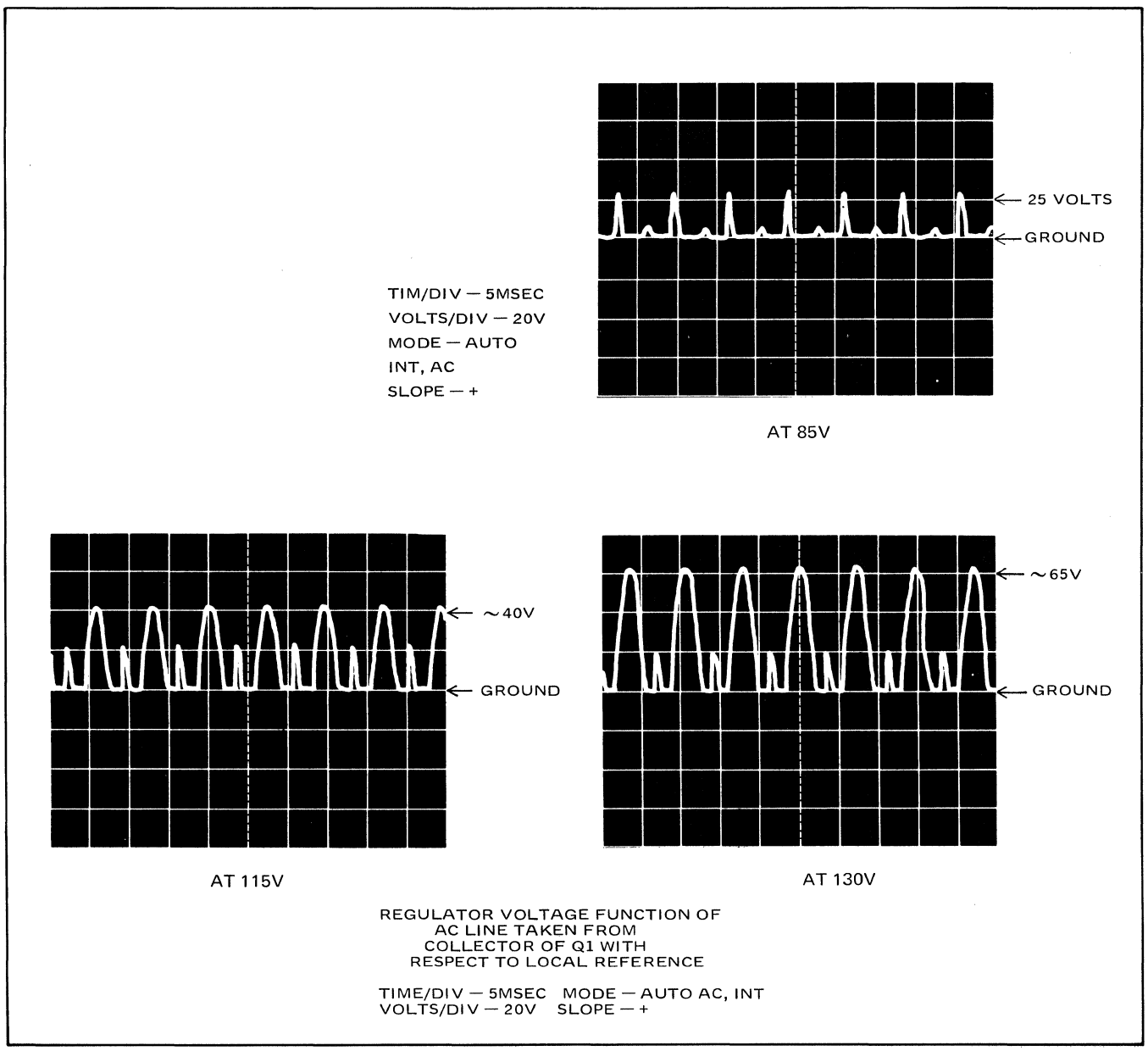


Figure 2-3. Q1 Collector Waveshapes

these transistors are mounted individually on each of the four vanes on the heat sink assembly. In addition to the four series regulators, the Q5 driver transistor, two regulators in the +20 volt circuit, and the 4 diodes in the AC bridge are also located on the heat sink assembly. It is not wise to leave the computer in the overload current mode for extended periods of time.

2-40. TRANSISTOR INSULATORS.

2-41. Care must be exercised in working around the Heat Sink Assembly. The mica insulators for Q1 to Q5 are special insulators of larger physical size (HP 0340-0458). The high voltage noise spikes that may be on the AC line require insulators which will safely handly 1000 to 1500 volts. The mica protrudes over the edge of the heat sink. The mica edge must not be cracked, bent, or broken.

2-42. A thin uniform layer of silicon grease must be used on both surfaces of the insulator to insure adequate thermal conductivity.

2-43. When replacing the diodes do not allow them to rotate. Rotation will score and damage the mica insulators.

2-44. UNREGULATED SUPPLIES.

2-45. The power supply contains several unregulated DC voltage supplies for the computer's logic circuits and in-

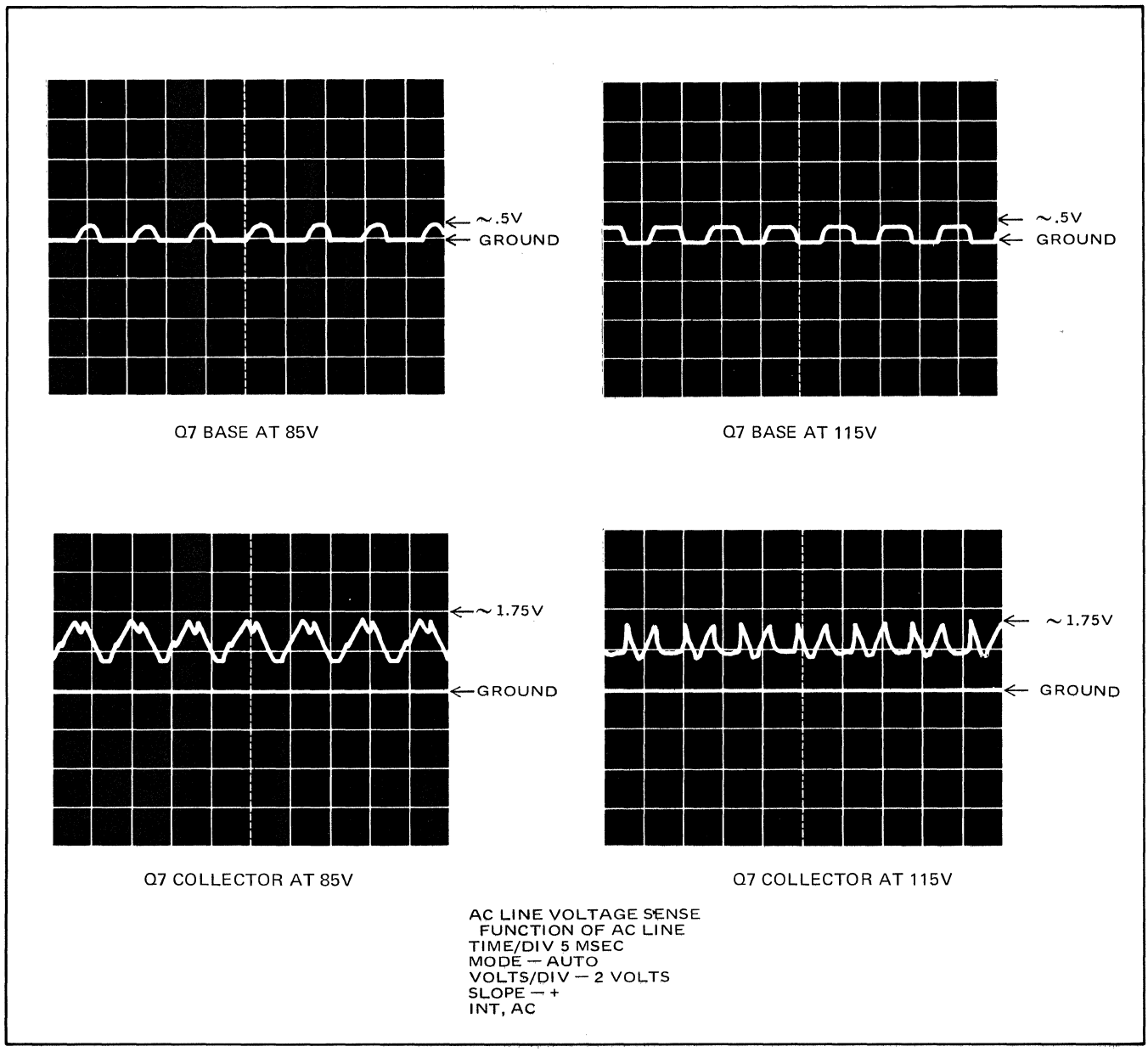


Figure 2-4. Q7 Base and Collector Waveshapes

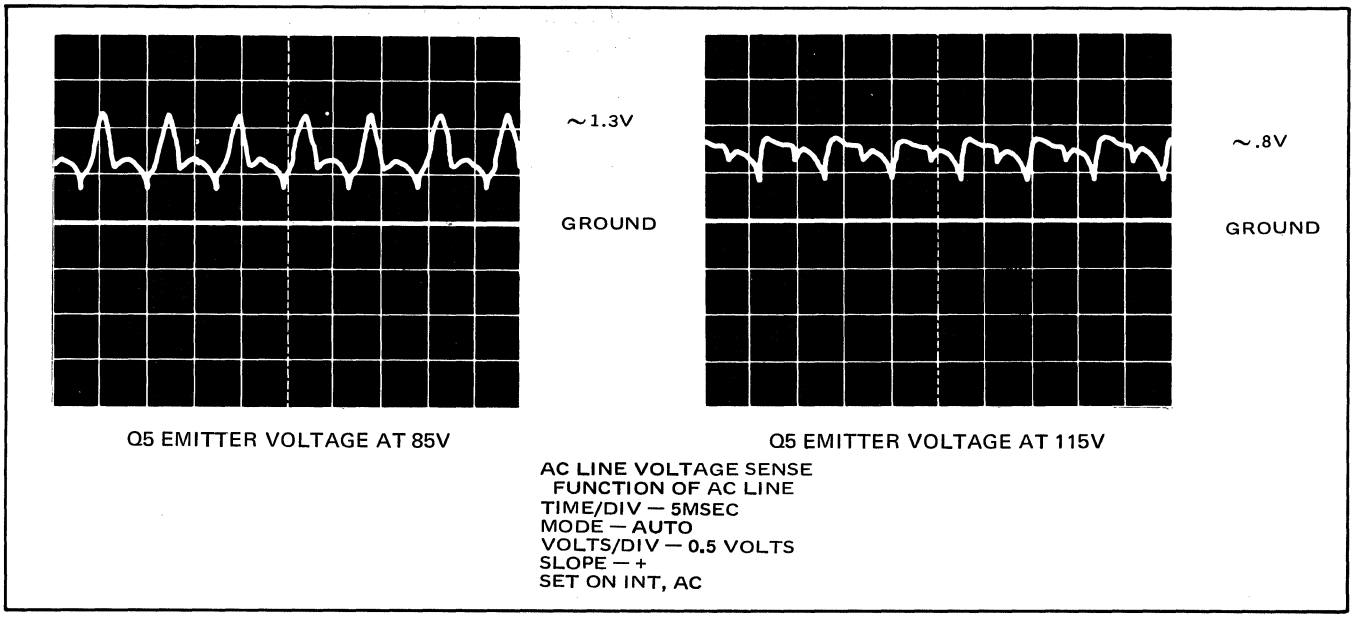


Figure 2-5. Q5 Emitter Waveshapes

dicators. The supplies, +30V, +30 volt lamp supply, ±12V, +5V and -2V are shown in Figure 2-6.

2-46. The voltage buses of the power supply are brute force (no voltage control or current limit), full wave rectifier, capacitor input lines. All cicruicts have fuse protection with the exeption of the +5 volt bus. The high current protection of the +5 volt bus is provided by the primary regulator overcurrent protection. The actual DC voltage of these buses is established by the turns ratio of

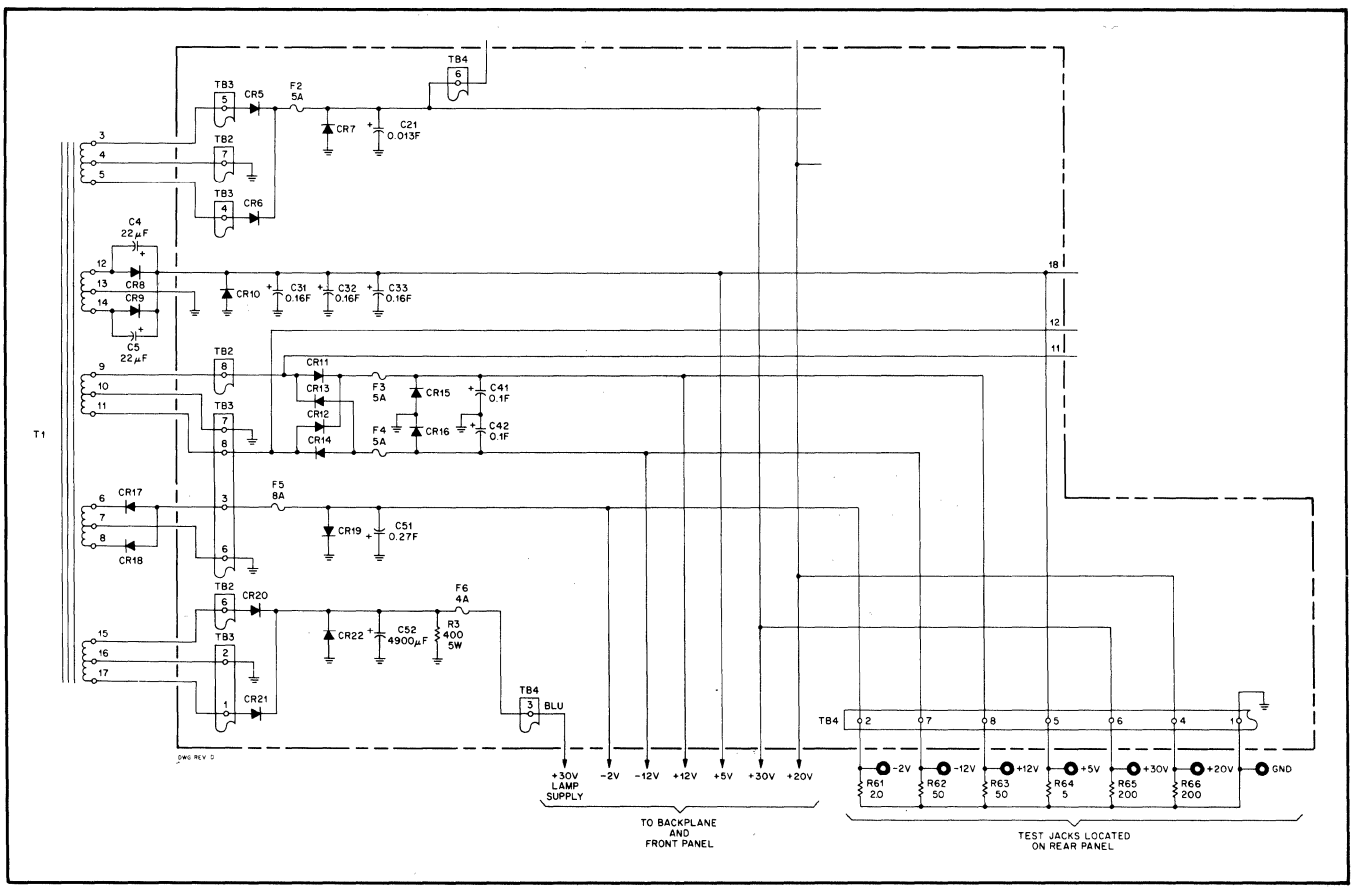


Figure 2-6. The Unregulated Buses

the transformer windings. Proper adjustment of the line regulator establishes the +5 volt bus. The other buses fall where they will.

2-47. An important troubleshooting aid on these voltage buses is the DC voltage as well as the AC ripple on each bus. It will be noted that each large capacitor has a protection diode across it which reduces the danger due to inadvertent reverse voltage connection. The plus 30 volt lamp supply is independent of the normal +30 volt supply. Its filtering requirements are minimal so the acceptable ripple is sub stantially higher. Otherwise, the supplies are similar. Refer to Table 2-1 for normal operating voltage levels.

Table 2-1. Computer Voltage Bus

VOLTAGE BUS	MAXIMUM *	MINIMUM **	AC RIPPLE PEAK-TO-PEAK
+ 5V	5.5V	4.3V	0.5V
+12V	13.0V	11.8V	0.3V
-12V	-13.0V	-11.9V	0.3V
- 2V	- 2.8V	- 1.9V	0.4V
+30V	32.0V	29.0V	0.5V
+30V Lamp	32.5V	28.0V	3.0V
+20V	19.5V***	19.5V	0.01V

* High AC Line, minimum computer load.
** Low AC Line, maximum computer load.
*** Depends upon ambient temperature.
19.5V dc nominal for 72°F to 80°F.

2-48. THE +30V SUPPLY.

2-49. The voltage for the +30 volt logic supply is determined by the turns ratio of the transformer. Diodes CR5 and CR6 provide fullwave rectification. Diode CR7 protects the filter capacitor C21 from damage due to reverse voltages. The +30 volt supply also provides a lightly filtered input to the regulated +20 volt memory supply.

2-50. +5V SUPPLY.

2-51. The voltage for the +5 volt logic supply is determined by the turns ratio of the transformer. Diodes CR8 and CR9 provide full wave rectification. Diode CR10 protects filter capacitors C31, C32, and C33 from damage due to reverse voltages.

2-52. -2V SUPPLY.

2-53. The voltage for the -2 volt supply is determined by the turns ratio of the transformer. Diodes CR17 and CR18 provide full wave rectification. Diode CR19 protects filter capacitor C51 from damage due to reverse voltages.

2-54. ±12V SUPPLY.

2-55. The voltage for the ±12 volt supply is determined by the turn ratio of the transformer. Diodes CR11, CR12, CR13, and CR14 provide fullwave rectification. Diodes CR15 and CR16 protect filter capacitors C41 and C42 from damage due to reverse voltages. The power failure detection circuits monitor the ±12 volt supply windings.

2-56. +30V LAMP SUPPLY.

257. The voltage for the +30 volt lamp supply is determined by the turns ratio of the transformer. Diodes CR20 and CR21 provide fullwave rectification. Diode CR22 protects filter capacitor C52 from damage due to reverse voltages. The +30 volt lamp supply is only lightly filtered.

2-58. TROUBLESHOOTING THE UNREGULATED SUPPLIES.

2-59. It is imperative that the high current carrying lines have good connections because of the extremely high peak currents. All of the mechanical connections in the 5V bus must be checked to determine that they make good contact. A poor connection in the 5 volt circuit compensated by raising the input regulator obviously will make all other voltage buses excessive. If error or fault occurs in only one or two of these nonregulated voltage buses the chances are good that it will be associated with either the rectifiers or transformer windings. Check that the diodes are installed and operating correctly and that the transformer center tap and voltage windings are properly connected.

2-60. 60 CYCLE RIPPLE.

2-61. If analysis of all voltage buses indicates the presence of 60 cycle ripple rather than 120 cycle ripple it may indicate that one of the diodes in the AC diode bridge or that one of the diodes or transformer windings in the voltage sense circuit is open so that voltage regulation is accomplished each half cycle.

2-62. FUSES.

2-63. It will be noted that the fuses are connected between the rectifier and capacitor in some cases. This means the fuses are subjected to RMS currents which are higher than the average DC output of the respective buses. This may account for fuse failure apparently below its rating. 60 cycle ripple present in one or two buses would indicate trouble in the transformer winding or rectifier associated with the specific voltage bus.

2-64. +20 VOLT REGULATOR.

2-65. A glance at the block diagram (Figure 2-7) shows that this +20 volt regulator consists of series regulating elements with an appropriate driver, a complex integrated circuit, and the voltage adjustment potentiometer with several temperature compensation resistors. The sophisticated IC reduces the number of discrete components that are required.

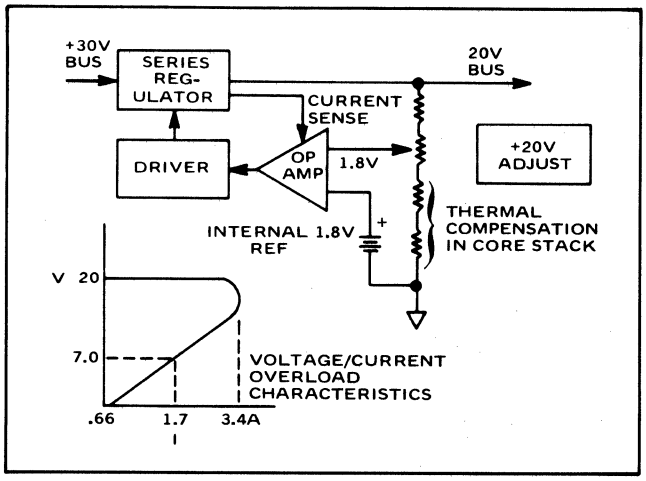


Figure 2-7. 20 Volt Regulator Block Diagram

2-66. CURRENT PROTECTION.

2-67. A look at the voltage overload graph shows that the output voltage is very stable up to its maximum established current (which in this case is about 3.5 amps). Above this level any further attempt to increase the current reduces the current delivering capability. This current fold back characteristic affords protection by reducing worse case dissipation.

2-68. Standard circuit operation delivers about 2.5 amps continuously. It is not necessary to measure the overload curve unless circuit failure has damaged components. To spot check the short current operation short out the +20 volt bus before power is applied to the computer. Then bring up AC voltage slowly. The regulator shall stay in the reduced current mode drawing about 0.8 amp with negligible output voltage.

2-69. +20 VOLT REGULATOR ADJUSTMENT.

2-70. The proper DC level is 19.5V at 25° ± 2°C. [The adjustment for other temperatures is 19.5V -0.088/°C (Ambient Temp -25°C.]

2-71. Referring to Figure 2-8, the +30 volt bus (consisting of a full wave rectifier and capacitor filter) is the unregulated power input. The series regulators are transistors Q10 and Q11. These transistors must be able to dissipate the power required at 2-1/2 amps. These transistors are located on the upper rear of the heat sink. The two emitter resistors R16, R17 are located directly behind on the left end of the Kingman card assembly. The bases are driven by the driver transistor Q12 located on the 2114-6010 Regulator assembly. Q12 gets its drive from the IC pin 2 booster output.

2-72. The +20 volt output bus is connected to pin 8. Output current goes through the series elements and the emitter resistors. The emitter resistors provide current balancing so that each transistor dissipates approximately half the load. If either of the transistors is destroyed or becomes inoperative the other is apt to become destroyed also. Check to insure both transistors are conducting. This can be done by measuring the voltage drop across the two emitter resistors.

2-73. The other inputs include: pin 4 ground, pin 3 unregulated input voltage, pin 5 by-pass for internal

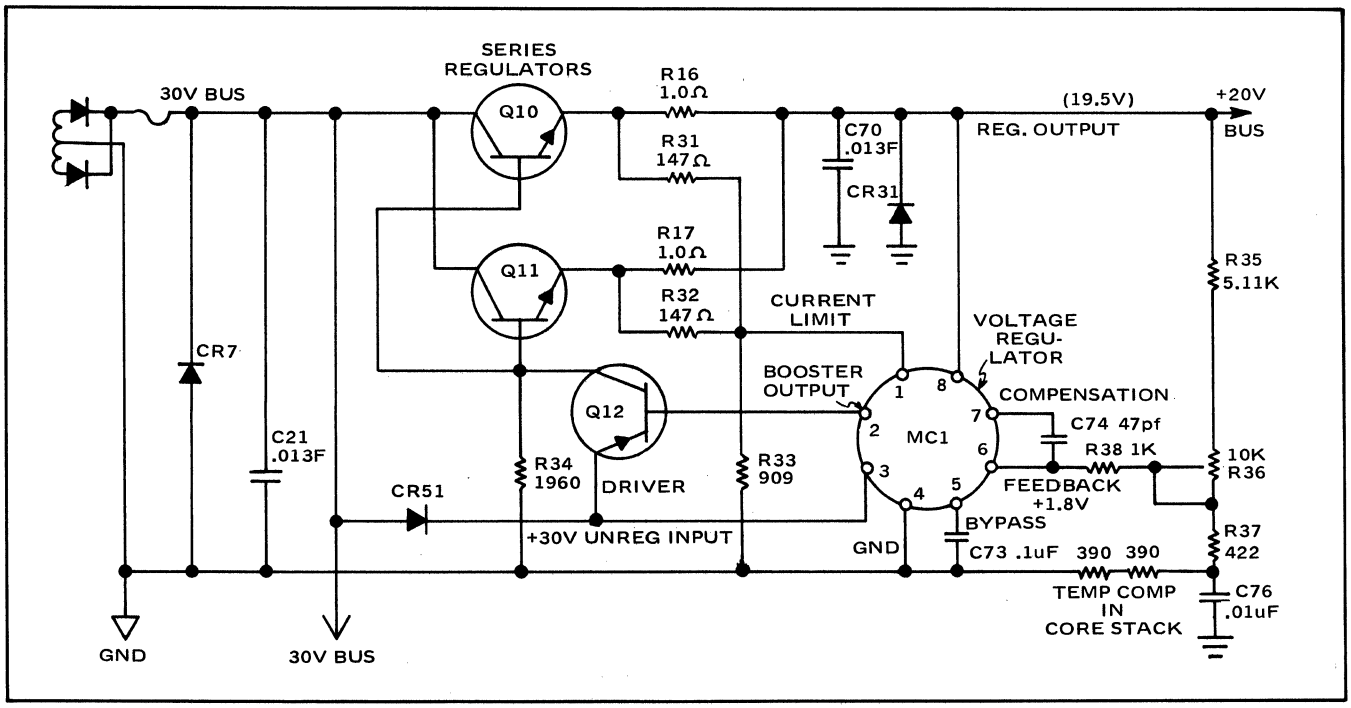


Figure 2-8. 20 Volt Regulator

circuitry, pin 6 is the feedback point for voltage control, pin 7 allows frequency compensation to prevent oscillation.

2-74. Pin 6 is a voltage feedback node and compares the circuit voltage with an internal reference. The resistor sting consists of R35, R36, R37 and two temperature compensating resistors which are physically located in the core stack. The normal DC operating level for Pin 6 is about 1.8 volts.

2-75. Pin 1 senses the current being drawn through the regulating circuit and allows the overload characteristic for protection of the series elements. When the voltage between pins 1 and 8 exceeds about 0.7 volts it reduces the current pin 2 can provide.

2-76. +20 VOLT REGULATED BUS – TROUBLESHOOTING.

2-77. An analysis of the DC levels is the most expedient way to troubleshoot the circuit. Check first that the +30 volt unregulated bus is normal. The input voltage level to pin 6 integrated circuit the feedback point should be approximately 1.8 volts when it is operating. As the +20 volt adjustment is made with potentiometer R36 the voltage change at pin 6 is negligible. The adjustment range of this circuit is from 2 volts to 30 volts.

2-78. The voltage relationship of pins 2 and 3 are stable regardless of actual adjustment of the 20 volt bus. Pin 3 is approximately 0.7V below the +30 volt unregulated bus. Pin 2 is about 0.7V below pin 3. Pin 1 to pin 8 voltage is a measure of the current being supplied by the regulator (voltage drop on emitter resistors of the regulators). When pin 1 exceeds pin 8 by 0.7 volts the booster output of pin 2 is reduced and the regulator enters the current fold back protection mode.

2-79. TEMPERATURE COMPENSATION.

2-80. The temperature compensating resistors are located in the core stack. An allowance should be made of approximately 88 millivolts/degree C for voltage adjustment at temperatures other than 23-27°C (72-80°F) ambient. The voltage bus should be decreased by 88 millivolts per degree C. A *decrease* in temperature below normal ambient will require a voltage *increase* of 88mv/°C.

2-81. COMPENSATION RESISTORS.

2-82. The only check of the temperature compensating resistors is a simple resistance measurement. A value of 675 to 900 ohms is an acceptable value. The component has a +7400 PPM/°C temperature coefficient. In case of component failure the computer can be brought up by substituting the closest resistor value available. Run Memory Checkerboard Program while slowly increasing voltage and note voltage at failure. Then restart the test and decrease the voltage to failure point. Set voltage at the middle of the range. This will result in a reduced temperature operating range, but will suffice until the correct replacement can be obtained and installed.

2-83. The TC resistors are vendor supplied, and are not available through Hewlett-Packard. They are Texas Instruments sensistor TM 1/8W, 390 ohm ± 10%, +0.7% per °C. The closest substitute available through HP stock is 0811-2031 815 ohm, +5900 PPM/°C. Mount substitute on feedthrough insulators on memory bracket.

2-84. POWER FAIL DETECT CIRCUIT.

2-85. The purpose of this power fail detect circuit is to allow orderly turn on of power in the computer, and in case of power failure to allow proper turn off. A view of the block diagram indicated an AC detector which senses the voltage from the transformer winding. It utilizes the plus and minus 12 volt transformer windings although it is independent of the actual voltage buses. The circuit consists of an AC detector with a turn off delay, the threshold detector zener diode, the pulse shaping gates, and an effective AND gate with the 5 volt bus (Q24), a DC section with a turn-on delay network followed by a pulse shaping network.

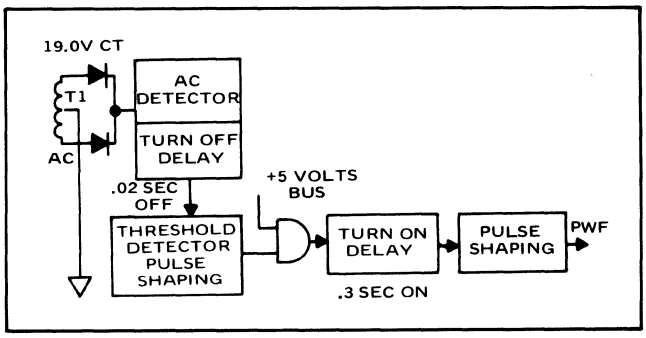


Figure 2-9. Power Fail Block Diagram

2-86. AC INPUT.

2-87. Referencing Figure 2-7, as the AC power comes up the full wave rectifiers CR52 and CR53 develop the voltage on C72. When the voltage has built up on this capacitor sufficiently high the zener diode CR54 begins to conduct at 6.2 volts and pulls up the input to the NAND gate MC2C. This voltage is pulled up through the forward biased diode CR55. Diodes CR55 and CR56 provide a hysteresis voltage level to the NAND gate inputs so that even if the voltage is somewhat near the turn on - turn off point for the NAND gates the output will not stutter. This provides an approximate 1.4 volt hysteresis range so that the operation will be stable even with minor variations in AC line.

2-88. TURN ON OPERATION.

2-89. Now, let us follow the normal sequence as the AC power comes up. The voltage builds up on C72 until the voltage exceeds the level of CR54. This voltage build up on

C72 is based upon the RC time constant R40 and C72 during turn on. The voltage on the input gate MC2C rises until it switches the NAND gate MC2C. The output of the first section goes down so the output on the second section comes up. Resistors R45 and R43 provide a feedback network for speed up, and hold on purposes.

2-90. The true output from MC2D saturates Q23 and holds off Q24.

2-91. TURN ON DELAY

2-92. The collector of Q24 goes high allowing C75 to charge up toward the +5V bus. The charging path is through R47 and R48. The time constant is about 300 milliseconds. When this voltage exceeds the threshold level on MC2B pin 5, MC2A and 2B switch providing a PWF high level output. The output of MC2D pin 8 is high and enables MC2B pin 4. R51 is a speed up resistor for pulse shaping.

2-93. TURN OFF MODE.

2-94. When power failure reduces the AC line voltage the DC level on C72 discharges toward ground through R41 and R42. The time constant is about 20 milliseconds. Diode CR56 pulls the input to MC2C down until it falls below the turn on threshold. The output of MC2D drops disabling MC2B pin 4 which changes PWF to its negative true state.

2-95. Q24 turns on providing a discharge path for C75 to re-establish proper turn on time constant.

2-96. TROUBLESHOOTING THE POWER FAIL DETECT CIRCUIT.

2-97. A variable AC autotransformer on the computer AC line provides the best method for troubleshooting the circuit. The voltage on C72 will vary between approximately 7.7 to 8.3 volts DC (from 98 to 130 VAC line). The AC ripple will be 120 CPS with a 1.4V P.P. amplitude.

2-98. The input to MC2C will be 1.9 volts DC nominal. The AC waveshape at MC2C pin 12 will have a positive hump and a negative dip as CR55 and CR56 conduct. The relative size of the two will depend on the AC line voltage. When R42 is adjusted correctly the negative dip enlarges as the line voltage drops toward 98 VAC. At 98 to 100 VAC (96V minimum) the waveshape changes suddenly indicating that the states of MC2C and D have changed. (Refer to Figure 2-10). At this point the PWF output will go low initiating the power failure sequence.

2-99. TURN ON DELAY.

2-100. The delay function during turn on can be checked in a rough way by observing the waveshape on C75 and the PWF output simultaneously. Set horizontal sweep to 100 msec/div, sync on AC line. Turn on the computer AC switch when the trace just begins a new sweep. The waveshapes can be seen after a couple of attempts. Leave switch off for a few seconds to insure all voltage buses have discharged fully before repeating. A delay of 300 to 500 milliseconds is typical (including reaction time in turning on the switch).

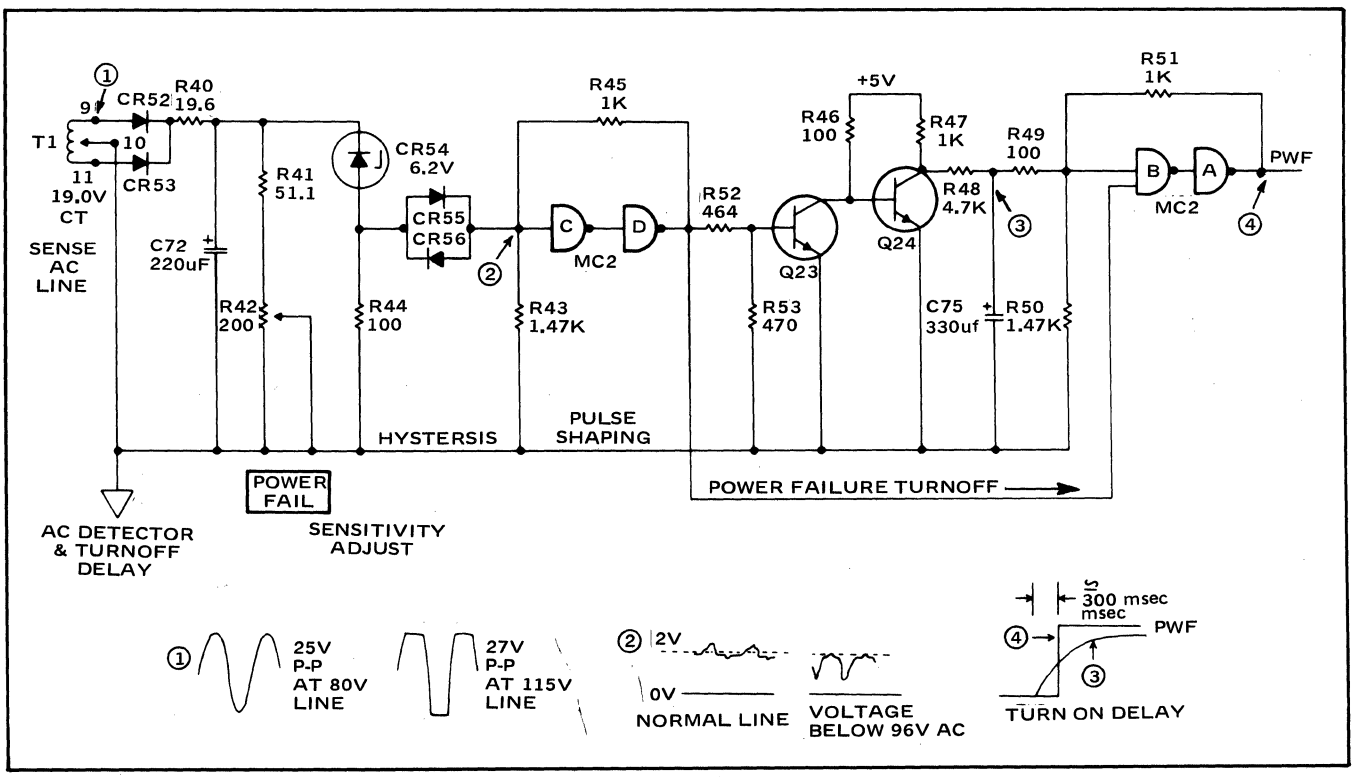


Figure 2-10. Power Fail

2-101. The PWF signal to the computer allows determining the status of the AC input voltage. This allows proper turn off for power failure. When Option 008 is installed the power failure option provides automatic restart when the power comes back on by interrupting to the software subroutine.

2-102. MAINTENANCE PROCEDURES.

2-103. The HP 2114B Computer Power Supply requires a minimum of routine maintenance to ensure proper Computer operation. The routine maintenance, usually performed on a monthly basis, consists of cleaning, inspection and testing.

2-104. CLEANING.

2-105. FILTERS. The Computer's two air filters, located on the Computer rear panel, should be cleaned as part of the routine maintenance procedure, or in extreme environments (high dust or oil content in the air), as needed. To clean filters perform the following:

a. Remove the filters from the computer.

b. Blow the filters clean with compressed air.

c. If compressed air is not available, hot soapy water may be used as a substitute.

d. Be sure the filters are completely dry and free of grease.

e. Replace the filters.

2-106. DUSTING. Small particles may pass through filters and build up in the computer. Use a small vacuum or compressed air hose to remove excess dust. Pay particular attention to heat dissipating areas.

2-107. INSPECTION.

2-108. Routine maintenance of the computer should include visual inspection of the mechanical parts of the computer. Dents, scratches, or poorly operating controls may indicate damage to the computer. Frayed, broken or burned insulation should be checked and corrected if necessary.

2-109. SUPPLY VOLTAGES.

2-110. Check the computer's supply voltages at the test jacks on the computer's rear panel. The various supplies and the acceptable ranges for each are given in Table 2-1.

2-111. If any of the computer's supply voltages are not within tolerance, refer to paragraph 2-112 for the appropriate adjustment procedure. Note that all logic supplies are adjusted by the +5 volt adjustment. When the +5 volt supply is properly adjusted the other supplies should be within their stated tolerances; if not, follow appropriate troubleshooting procedures. The +20 volt memory supply may be separately adjusted to compensate for variations in operating temperature.

2-112. PRIMARY REGULATOR ADJUSTMENT.

2-113. If the +5 volt supply is out of tolerance, proceed as follows:

a. Connect a voltmeter (refer to paragraph 2-7 for test equipment specifications) between the GND and +5V test jacks on the computer's rear panel.

b. Remove the computer's top cover.

c. Using a nonmetallic tuning wand, adjust the "PRIMARY REGULATOR" variable resistor (R27 on the Regulator Card) to obtain a reading of +5 ± 0.03 volts.

d. If the supply fails to adjust to tolerance, follow appropriate troubleshooting procedures.

e. Recheck the other supplies.

2-114. +20 VOLT MEMORY SUPPLY ADJUSTMENT

2-115. The correct voltage level for the +20 volt supply is dependent on the ambient temperature. The correct setting for a normal environment (72° to 80°) is 19.5 volts. The correct setting for temperatures outside this range can be determined from the following formula:

$$E = 19.5 - .05 (T - 76)$$; where T is the ambient temperature in degrees Farenheit.

If the +20-volt supply is outside of its specified tolerance, proceed as follows:

a. Connect a voltmeter between the GND and +20V test jacks on the computer's rear panel.

b. Remove the computer's top cover.

c. Using a nonmetallic tuning wand, adjust the "+20V MEMORY SUPPLY" variable resistor (R36 on the Regulator Card) to obtain a reading within the tolerance range specified by Table 4-1.

d. If the supply fails to adjust to tolerance, follow appropriate troubleshooting procedures.

2-116. POWER FAILURE THRESHOLD ADJUSTMENT.

2-117. The Power Failure Threshold adjustment sets the level at which a drop in the computer's supply voltage will trigger the computer's power failure detection circuits and cause the computer halts.

2-118. This adjustment is made by Hewlett-Packard before shipment of the computer and no further adjustment should be required. If adjustment becomes necessary proceed as follows:

a. Turn the computer off by pressing the HALT switch and turning off the POWER switch located on the chassis behind the computer front panel.

b. Disconnect the computer power cord from the AC line source and connect it to a variable autotransformer.

c. Remove the computer's top cover.

d. Set the computer POWER switch to "ON".

e. Insert a test loop in the computer as follows:

(1) Set the computer LOOP INSTRUCTION switch, located behind the front panel, to LOOP.
(2) Set the Switch Register to zero.
(3) Press the LOAD ADDRESS switch.
(4) Press LOAD MEMORY and LOAD ADDRESS again.
(5) Press the RUN switch. The computer should begin executing the test loop.

f. Using a nonmettalic tuning wand, rotate the "POWER FAIL THRESHOLD" variable resistor (R42 on the Regulator Card) fully counterclockwise.

g. Set the variable AC source to 98 volts.

h. Rotate R42 slowly clockwise until the computer halts.

i. Increase the voltage of the variable AC source to approximately 102 volts.

j. Press the computer RUN switch. The computer should begin executing the test loop. Slowly reduce the voltage from the AC source. The computer should halt when the source voltage approaches 98 volts. If the computer fails to halt, repeat the adjustment procedure. If repeated adjustment fails to correct the problem, follow appropriate troubleshooting procedures.

FRONT PANEL

SECTION III
FRONT PANEL

3-1. INTRODUCTION.

3-2. The Front Panel contains the various switches necessary to operate the 2114B Computer. The memory data register ("T" Register) and memory address ("M" Register) are both displayed on the front panel. The Switch Register is displayed with lamps under the actual proximity switch assembly. This permits display of the Switch Register for manual inputs, and output display under program control by outputing to select code 01.

3-3. The power switch and line fuse are accessible behind the panel. The rear of the front panel contains various switches for troubleshooting and service. The Front Panel Assembly can be locked to prevent access to the power switch or the diagnostic switches. The entire panel can be easily removed by the detachable hinges, and removal of the nut holding the ground braid.

3-4. EQUIPMENT FOR SERVICE.

a. Oscilloscope HP 180A or equivalent
   Vertical amplifier HP 1801A
   Time base HP 1820A
   Probes HP 10004A

b. Voltmeter HP 427A
   If Null adjustment is attempted with a digital voltmeter an HP 3430A or HP 2401A/2A is required.

c. Insulated tuning screwdriver for NULL adjustment.

3-5. ACCESS FOR SERVICE.

3-6. The front panel can be removed from the front door to make the components visible for easier identification. Care should be exercised to prevent shorting any circuit to the instrument.

3-7. CIRCUIT DESCRIPTION.

3-8. MASTER OSCILLATOR.

3-9. The amplitude of the frequency determining portion of the oscillator is established by the nonlinearities of the transistors Q30 and Q32, (i.e., saturation). The signal is AC coupled to the power amplifier. The power amplifier has a voltage gain of one. In the positive direction the collector voltage of Q35 is about equal to the base of Q33. The output current through R126 reduces the current flow through Q34 thus reducing current through Q36. In this manner the output stage provides a low output impedance with small steady state dissipation. The output impedance is about 25 ohms, and the load is 25 proximity switch circuits in parallel (800 ohms effective impedance).

3-10. PROXIMITY SWITCH CIRCUIT.

3-11. The two inputs to the proximity switch circuit are a DC Bias voltage, and an AC sinusoidal signal. The circuit

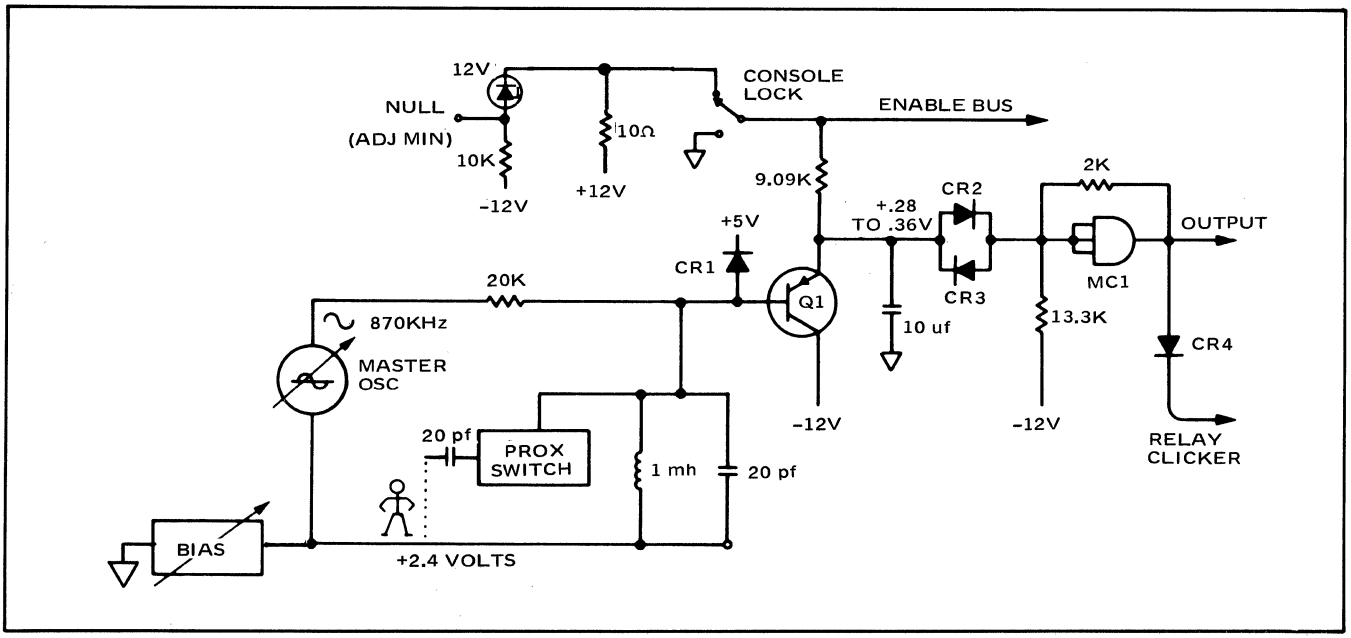


Figure 3-1. Proximity Switch Circuit

also requires the ENABLE voltage in order to operate. Each circuit provides an output to the computer backplane, and drives the relay clicker circuit.

3-12. The master oscillator generates a sine wave signal. The frequency can be adjusted over the range 0.7 to 1.3 MHz by adjusting the NULL variable capacitor. This signal drives the parallel tuned circuit on the base of each emitter follower transistor. The DC return is through the inductor to the BIAS voltage bus which should be adjusted to +2.40V ± 0.1 volts. The emitter capacitor charges to the negative peaks, normally +0.28 to +0.36 volts. This voltage holds the input to the AND gate in zero state.

3-13. The action of touching the proximity switch sensor is to increase the capacitance by about 20 pf in the parallel tuned circuit. This detunes the circuit resulting in a smaller signal envelope. The emitter capacitor voltage rises with the negative peaks. The diode pulls the AND gate input up until the AND gate switches to the one state. The 2K feedback resistor keeps the AND gate on until pulled down by the other diode, and also speeds up the output signal.

3-14. The AND gate switching to the one state energizes the relay clicker circuit, and provides a positive clock to the Switch Register FF on the Arithmetic Logic assembly. The diodes between the emitter capacitor and the AND gate provide a safety margin gap for turn on and turn off of the AND gate due to the hysteresis effect produced by the diodes. This ensures that the output of the AND gate will not stutter as the emitter voltage fluctuates.

3-15. The diode between the base and the +5 volt bus is a clamp on the positive peak to protect the transistor and to limit the tuned circuit amplitude.

3-16. The NULL test point measures the voltage drop across the 10 ohm resistor between the ENABLE bus and the +12 volt bus (translated down by the zener diode to make measurement easier). As the master oscillator frequency is adjusted the transistor current increases to its maximum value (minimum voltage) at the average parallel resonance of the base circuits. This indication is subtle and must be observed carefully.

3-17. The ENABLE bus can be disabled by using the CONSOLE LOCK switch on the front panel assembly, or by removing the jumpers W1 and W2 on the board. The console lock can be defeated by replacing the jumpers W1 and W2 in the lower alternate positions.

3-18. ADJUSTMENTS.

3-19. Set BIAS voltage to 2.4V ± 0.1V DC. Adjust NULL to minimum (observe and adjust carefully); it requires 3 or 4 place accuracy for DVM measurement. An alternate NULL method is to observe emitter DC voltage (DC input, 0.05V/cm with 10:1 probe). Adjust NULL for minimum voltage — +0.28 to +0.36 volts typical. Repeat for 5 to 10 switches and set NULL capacitor at the best average position. Oscillator frequency is 870 kHz typical.

3-20. Do not troubleshoot by looking at the base circuit with a scope probe (except for sensor failure noted below). The probe will detune the base enough to prevent proper operation.

3-21. The failure of the proximity switch sensor material may cause an intermittent connection. It can be checked by observing the signal envelope on the base circuit (at 20 msec/cm). Touching the sensor or moving it sideways should result in smooth envelope changes (not abrupt or jagged envelope).

3-22. The voltage on the emitter is the best indication of proper proximity operation. The normal level is +0.28 to +0.36 volts. It increases as the switch is touched. The AND gate switches and the clicker clicks at about 1.5 volts dc.

3-23. The light indicator is driven from circuitry on the Arithmetic Logic board. A clean envelope on the base and operation of the clicker at an emitter voltage of 1.5 volts usually indicates correct operation of the proximity circuit.

3-24. No adjustment of the values of the base circuit components exist. If the capacitor or inductor is changed it may be necessary to select this component to provide comparable switch sensitivity with the other switches. Slight change in oscillator frequency or Bias voltage may be helpful in establishing uniform switch sensitivity.

3-25. The clock input to the Switch Register FF is filtered with a 100 ohm, .01 μf RC filter. This reduces improper triggering due to coupling in the cable. Replacement of the AND gate on the front panel may result in poor overall switch operation due to insufficient amplitude or rise time. It may be necessary to select an AND gate which will work properly.

3-26. LOAD CIRCUIT.

3-27. The proximity switch circuit for the automatic use of the Basic Binary Loader is fundamentally the same. It has two additional features, however, which limit (or control) the circumstances under which it can be operated. The Enable voltage for the emitter follower is disabled by the low PRS preset line. When the preset control is touched first this PRS line goes high which then allows normal operation of the Enable voltage to the emitter follower.

3-28. The RFB signal is low whenever the computer is running. Q4 will be non-conducting and MC7 pin 1 will be open due to the open collector of Q4. This will act as a high signal into MC7 pin 1 but PRS will be low due to the fact that the Preset Switch is dependent upon the RFB signal also. This will pull the Enable Voltage low and disable the LOAD switch during RUN. When the computer is in the halt mode RFB goes high allowing Q4 to conduct. This will put pin 1 of MC7 at a low voltage and cause the circuit to be dependent upon the PRS signal.

3-29. When PRS is generated by pressing the Preset Switch it forces Q4 off by bringing its emitter to a high voltage. This forces Pin 1 of MC7 open or high and enables the Enable voltage to the LOAD switch circuitry. When LOAD is pressed an LDL signal is generated and sent to the Timing Generator Card. This, in turn, allows the Basic Binary Loader to take command over any Absolute Binary tape being entered.

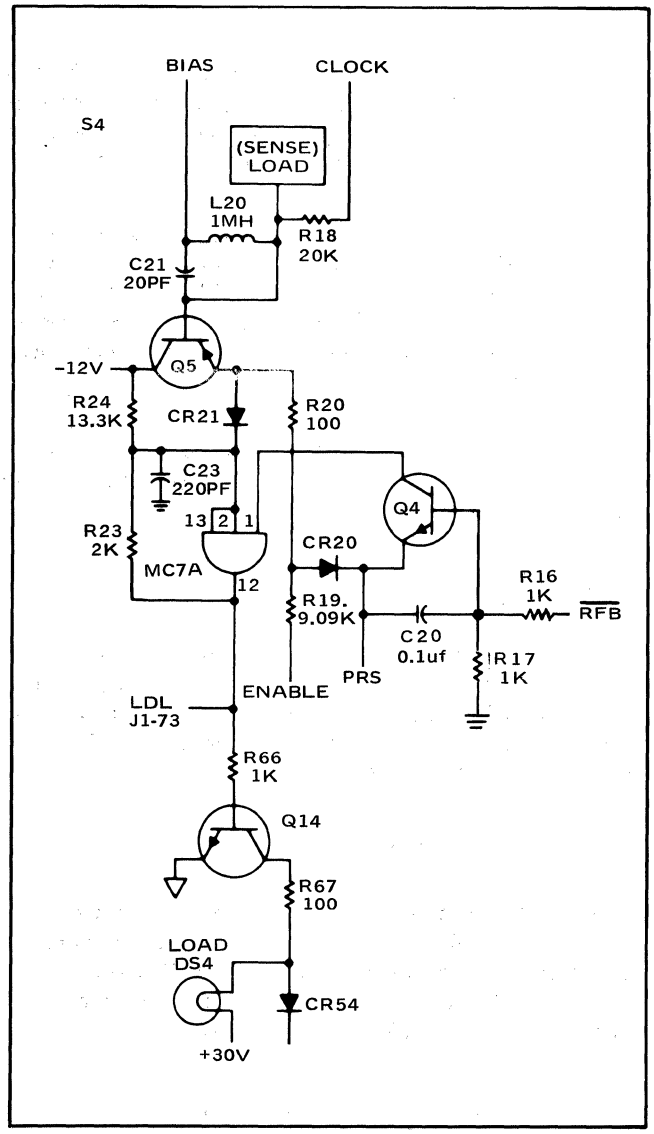


Figure 3-2. LOAD Proximity Switch

3-30. SWITCH REGISTER LAMPS.

3-31. The drive transistors for the Switch Register lamps are located on the Arithmetic Logic assembly. The proximity switch toggles the Switch Register flip-flop each time it is pushed. The contents of the Switch Register can be read into the S bus by the load memory or load address switch, or by an Input A or B instruction at select code 01.

3-32. The contents of the Switch Register can be set by an output (OT A/B) to select code 01. The register is cleared by CSR at T3, then the bits which are "one" are set at T4 by SSR and R bus. This allows using the lamps in the Switch Register to display information under program control.

3-33. The integrity of the lamp filaments can be checked by the LAMP TEST switch. (Refer to Figure 3-3.)

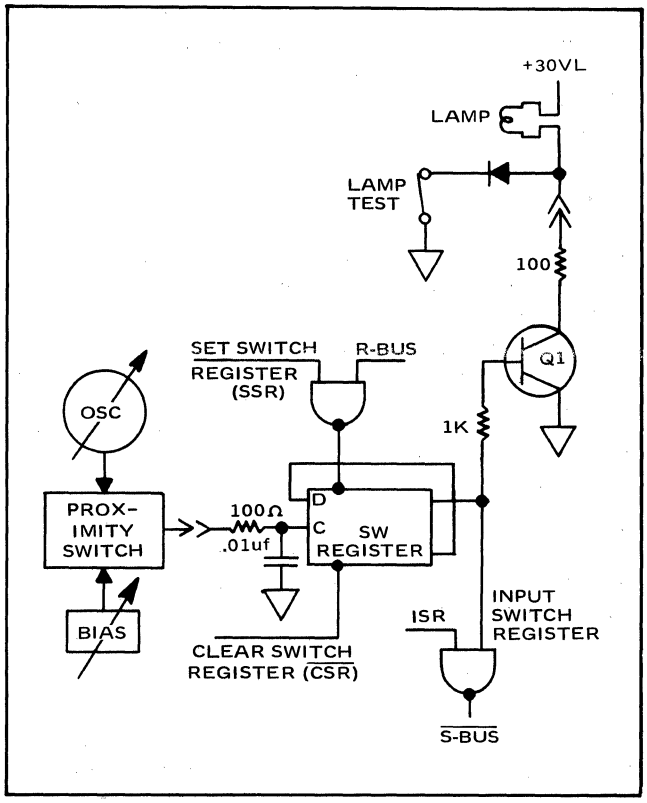


Figure 3-3. Switch Register Logic

3-34. RUN FF BUFFER.

3-35. The RF2 is buffered on the front panel and the output RFB is used to control the LOAD, and to inhibit the LOAD MEMORY, LOAD ADDRESS, DISPLAY MEMORY, and SINGLE CYCLE switches.

3-36. A couple of isolated cases have arisen in which the value of C101 was too small and this allowed a malfunction in which the computer stepped 10 or 15 cycles or more. This can be quite confusing depending on what is in the affected memory locations.

3-37. FRONT PANEL TEST SWITCHES.

3-38. The six switches accessible from the rear of the Front Panel assembly are useful for troubleshooting and diagnostic purposes. It is wise to check their condition before starting to work on the machine.

3-39. CONSOLE LOCK.

3-40. The Console Lock switch allows the operation of the Front Panel proximity switches to be inhibited. It removes the +12 volt Enable voltage from the proximity switch circuits.

3-41. Jumpers W1 and W2 are located in the upper right hand corner of the board (facing the components). They allow overriding the Console Lock by hardwiring the Enable lines to the +12 volt bus. W1 provides Enable voltage to the Switch Register. W2 provides Enable voltage to the Front Panel Control functions. This switch is used in applications where inadvertent operation of the Front Panel Controls or the Switch Register is undesirable.

3-42. LAMP TEST.

3-43. The lamps used on the front panel are driven in many different ways. The use of this single switch applies voltage to the filaments of all front panel lamps. Some lamps will be brighter in Lamp Test. This results from the full 30 volt lamp supply voltage in test position. In normal operation the lamp driver has a current limiting resistor for lamp turn on and to establish a satisfactory illumination level.

3-44. The lamps associated with the Memory Register bits 14 and 15 are tested by the Lamp Test, but are not used by the computer in any operational sense. They can be used as spare lamps.

3-45. LOADER ENABLE.

3-46. This loader Enable switch provides a means to protect the top 64 core locations, but still to have access under certain conditions. It must be ON for core access. This allows using the bootstrap loader, or by direct toggling to enter the Basic Binary Loader instructions. The switch is then protected in NORMAL position.

3-47. The front panel PRESET-LOAD allows automatic access to the Basic Binary Loader without the necessity of manipulating this Loader Enable (protect) switch.

3-48. Occasions arise in which access is desired. If malfunctions occur in the PRESET-LOAD circuits operation in the manual mode might still be possible (enable the protected area Loader Enable to ON, set switch register to 0X7700, Load Address, Preset, Run).

3-49. The switch is also helpful to display contents of the protected area, and to allow Single Cycle operation for debugging.

3-50. SINGLE INSTRUCTION LOOP.

3-51. The output of the Single Instruction switch in LOOP position is the signal SIN. This signal has one function. It holds the SB0 high at time T67. This prevents the $\overline{P + 1 \rightarrow P,M}$. Thus, no incrementing of the P and M Registers occurs in the normal operations (Run, Single Cycle, Display Memory, Load Memory, etc.).

3-52. This allows performing the same instruction repetitively. It is usually easier than trying to write a short loop program. Refer to Phase Loop below.

3-53. PHASE LOOP.

3-54. The output of the Phase Loop switch is the LNS negative true. This signal (negative) prevents clocking the Phase flip-flops. It thus retains the phase condition established at the time it is placed in the LOOP position.

3-55. It is useful for initializing core. An instruction like Store A is single cycled to execute phase. The Phase switch is then placed in LOOP condition. This allows the P and M Registers to increment. The contents of the A-Register are stored throughout core. This is one method used for checking the Sense Amplifiers.

3-56. A useful combination of Phase and Single Instruction Loop allows repetitive data store in a single memory location.

3-57. MEMORY OFF SWITCH.

3-58. The Memory Switch in Off position produces the MON negative signal. The positive MON is required to generate the MTE which in turn controls the memory timing generator. This OFF position essentially makes all core locations NOP instructions.

3-59. HALT BUTTON.

3-60. The Halt switch provides two useful functions. If the HALT switch is touched during a LOAD MEMORY the P and M Registers are not incremented. It allows loading the A Register and executing the instruction without the necessity of loading address 0 in between.

3-61. The other use is in conjunction with the Interrupt Phase 4. The Run 1 flip-flop is a required input to set Phase 4. Run 1 FF is not set while using the Single Cycle button. Therefore, the computer can not execute a Phase 4 Interrupt through use of the Single Cycle button. Holding HALT while pushing RUN wil result in executing a single machine cycle (like Single Cycle). Since the Run 1 FF is set in this mode of operation the setting of Phase 4 is allowed.

3-62. FRONT PANEL OPERATING CONTROLS.

3-63. Table 3-1 describes the logical functions used in the Front Panel Operating Controls. Refer to Figure 4-6 for the circuit diagram for the controls.

Table 3-1. Front Panel Operating Controls

BUTTON	MNEMONIC	FUNCTION
RUN	RNL	Forces Step FF1, 2; providing conditions on Run FF 1 (set input) to continue in Run mode.
HALT	HLL	Sets the K input to Run FF 1, causes halt after current machine cycle.
PRESET	PRS	Provides POPIO @ T5. Clears Step FF 1,2. Clears Phase FF 1-4.
CLEAR REGISTER	CLR	Generates $\overline{\text{CSR}}$ which directly clears the Switch Register FF's.
LOAD ADDRESS	LAL	Produces SSPM which generates all STM and STP strobes. Produces SEO → EOF and ISR. Holds off MST and sets MWL to overlook Parity condition. Set Phase 1. Operation does not require Single Cycle. Holds off Preset and Load.
LOAD MEMORY	LML	Produces $\overline{\text{SWST}}$ (SWSA if addr 0, SWSB if addr 1) Strobe signals. Set Phase 3. Force Single Cycle operation. Set $\overline{\text{EIR}}$ to inhibit Instruction Register. Produces SEO → EOF and ISR. Holds off MST and sets MWL to overlook Parity condition. Holds off Preset and Load
LOAD	LDL	Overrides Memory Protect giving MTE. Forces Single Cycle and Run. Sets Phase 1. Generates SAL and SSPM to set Loader address. $\overline{\text{RF2}}$ retains the sense of LDL as long as Run mode continues.
DISPLAY MEMORY	DML	Set Phase 3. Initiate Single Cycle Set $\overline{\text{EIR}}$ to inhibit Instruction Register normal Phase 3 operation: Clear T @ T0, Memory Timing for Read and Write, P + 1 → P.M.
SINGLE CYCLE	SCL	Operates Step FF 1,2 to achieve one machine cycle. Single Cycle and Halt can be used together to prevent incrementing P and M Registers (holds off $\overline{\text{SB0}}$).

3-64. BASIC BINARY LOADER.

CAUTION

To load any absolute binary tape using the basic binary loader CLEAR the SWITCH REGISTER.

3-65. The Basic Binary Loader has two optional features in addition to the primary loading capability. The features are selected by bits 0 and 15. They include comparing the tape against core (without loading) and Check Sum (without loading). To insure proper load it is necessary to clear the Switch Register before loading the tape.

3-66. TROUBLESHOOTING.

3-67. The second step in troubleshooting the HP 2114B is to check the operating conditions of the Front Panel (the first step is to check the Power Supply voltages). The technician will use the Front Panel Switches for all initial tests of the HP 2114B before actually running diagnostic test tapes. He will be testing the Central Processor Boards and Memory Boards within the machine for any obvious problems that can be detected directly from the display registers on the Front Panel (this is referring to the Pretest Checkout Procedure described in Chapter 7 on Troubleshooting the HP 2114B). But first he must ensure himself that the operation of all the Front Panel Controls are correct.

3-68. To test the Front Panel simply perform the Pretest Checkout Test. This Pretest Checkout Test not only gives an initial check of the CPU Boards and Memory Boards but it ensures correct operation of the Front Panel Switches, Controls and Display Registers as well. If a problem is detected while executing the Pretest Checkout, the technician should try to logically reduce his problem to a certain section of the computer. Is the problem in the Central Processor Unit Section of the computer? Is the problem generated in Memory Section of the computer; Or, is the Front Panel Assembly giving the problem;

3-69. The Front Panel Assembly consists of two basic parts, the actual metal casing and the printed circuit board attached to the back of the metal casing. The metal casing is used as a display board and as a protection shield for the Front Panel printed circuit board (A24), the printed circuit board contains all circuitry related to the Front Panel Controls, Switches and Display Registers. If any problem exists in the Front Panel Assembly it will exist on the printed circuit board.

3-70. Because of the large size of this printed circuit board and because all of the components on the board are located between the metal casing and the printed board, it becomes a task to try to troubleshoot the Front Panel. This is one good reason why all other possibilities relating to the problem occuring should be checked out before trying to troubleshoot the Front Panel. Troubleshooting techniques such as board swapping identical boards within the computer to determine whether the problem follows the switch should be performed. This will reduce the problem to one of the identical boards or rule them out of the problem completely.

3-71. The technician is completely satisfied that the problem does exist on the Front Panel, he can begin troubleshooting the Front Panel printed circuit board. Once the technician has actually begun troubleshooting the board with an oscilloscope or logic probe, etc., it will be up to him to develop his own troubleshooting technique. But, a few hints are in order at this time. Try to reduce the problem even further; the technician needs a starting place to begin troubleshooting. Ask yourself "Is the problem common to more than one switch?". As an example, all the lights are out on the Switch Register and will not come on. "Is the problem unique to one specific switch?" Possible the switch for bit 6 in the Switch Register is the only switch that is giving problems. These type of questions can reduce the problem to specific circuits on the board and produce a good starting point for the technician.

3-72. Common problems that do occur on the Front Panel Assembly are:

a. The adjustments are out of alignment.

b. The light bulbs blow out.

c. Possible circuit problems with each proximity switch; i.e., problems can occur with a single proximity switch rather than all switches. A few troubleshooting hints dealing with these problems will follow.

3-73. Anytime the Front Panel Controls or Switches begin to give sporadic problems such as random lights beginning to come on when the switches are not pressed, the clicker does not click or the Front Panel is inoperative it may be caused by a maladjustment of the two Front Panel adjustments. A good troubleshooting hint when problems do occur on the Front Panel is to immediately check the two adjustments on the Front Panel. A specific hardware problem on the Front Panel can cause the two adjustments (the BIAS adjustment and the NULL adjustment) to become out of specifications. Once the adjustments have been corrected the problem is usually reduced to one specific switch on the Front Panel.

3-74. Every once in a while one of the light bulbs on the Front Panel will fail. This is detected very easily by simply switching the Lamp Test Switch to TEST which is located on the back of the Front Panel Assembly in the upper left-hand corner. *ALL* lamps should light. If they do not then the most likely problem would be a bulb failure. Exchange the bulb and test the lamps again.

3-75. It is a simple procedure to change a bulb on the HP 2114B Front Panel but the procedure should be mentioned at this time because the technician can cause serious problems on the Front Panel by forgetting parts of the procedure. To change a bulb on the Front Panel simply open the Front Panel Door and remove the protective cover on the back of the door. The bulbs can now be visibly seen on the back of the door and are held in place by sliding contacts which hold the bulbs in place by tension on the back of the bulb. These sliding contacts supply a +30V to the base of each lamp to allow turn on of each lamp when its corresponding driver transistor is turned on. To remove each bulb slide its corresponding contact to the right or to the left and pull the bulb out. Replace the bulb and the *sliding contact* to the bulb and perform the LAMP TEST again. Again, don't forget to replace the +30V contact to the back of the bulb.

3-76. The +30V sliding contact has no real position to be moved when changing a bulb; therefore, once the sliding contact has been moved it will most likely come into contact with other parts of the Switch circuit. If the contact is not replaced and power is turned on, the +30V will be put directly into contact with other components of the circuit and will blow all or part of the associated circuit to that proximity switch circuit. Since the +30V contacts do slide it is good practice to check all contacts to each bulb after the Front Panel has been worked on. An accidental push of one of these contacts can cause the same problem as described above.

3-77. Circuit failure of a proximity switch can be considered the next common type problem. A common type problem can be defined as a problem, if it occurs, that can be reduced to a certain section of the Front Panel, not a problem that occurs frequently. The characteristics of this type problem could be that a proximity switch will always be on or it will never turn on. Also, the clicker may always be energized due to a faulty switch. This can be detected by touching the proximity switch and determining whether

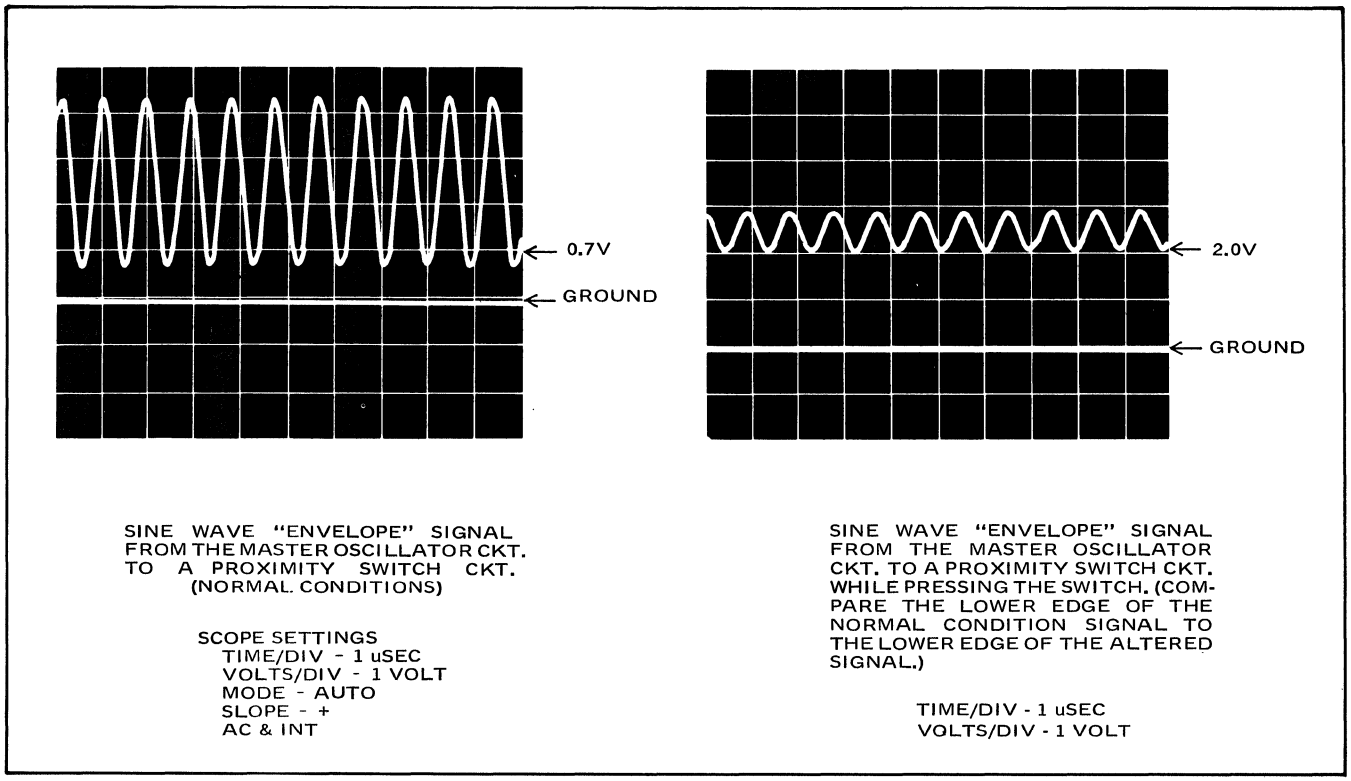


Figure 3-4. Envelope Signal to Base of Proximity Switch Transistor

correct operation occurs. Again, a problem on the Front Panel can be a fault of associated sections of the computer. Ensure the problem is on the Front Panel by checking associated sections first.

3-78. When troubleshooting the proximity switch circuit (refer to Figure 3-1) a good starting position is at the base of Q1. (Each proximity switch circuit has a corresponding transistor as shown in Figure 3-1.) An "envelope" signal as shown in Figure 3-4 (with respect to ground) is placed on the base of transistor Q1. Any other signal at this point will indicate an error. As an example, referring to the previous description of changing the light bulb, if the +30V contact was not replaced and it was making contact with one of the extended prongs from the proximity switch, when power was turned on the first component to fail would be the clamping diode on the base of the transistor. Most of the time this diode shorts out and allows the full +5V to the base of the transistor with no "envelope" signal present. From this point on, it is just a matter of going through the switch circuit and ensuring correct operation from component to component. The integrated circuit is the most reliable component of the circuit and need not be checked until last.

3-79. Similar problems can also occur within a proximity switch circuit due to aging of the circuit. The transistor, Q1, and the integrated circuit MC1 can become heat sensitive due to age. This problem tends to increase the propagation delay from intput to output of the integrated circuit causing problems with the Switch Register FF associated with that proximity switch circuit. A heat sensitive transistor, Q1, tends to load down the tuned circuit on the input to the base of the transistor. This will decrease the amplitude of the "envelope" signal, decreasing the condition of the transistor which would turn MC1 on all the time causing the Switch Register FF to remain in one state at all times. This problem can be detected by comparing signals to the bases of other transistors in other proximity switch circuits. The signals should all be equal.

3-80. These are a few helpful hints on troubleshooting the Front Panel Circuitry. Don't forget to put the protective cover back on the Front Panel Assembly.

CENTRAL PROCESSOR UNIT

IV

SECTION IV
CENTRAL PROCESSOR UNIT

4-1. INTRODUCTION.

4-2. The central processor unit of the 2114B Computer consists of 7 printed circuit assemblies: 4 identical arithmetic logic assemblies, 1 timing generator, 1 instruction decoder, and 1 shift logic assembly. In conjunction with the front panel the central processor unit can accomplish certain arithmetic operations. It is possible to determine the operation of certain functions without any memory installed. The content of this chapter will be limited circuit description on the arithmetic logic and timing generator boards and fairly extensive analysis of the computer operation codes including the signals that they utilize. It is assumed that the service technician understands the operation of the simple TTL logic components utilized in the central processor design.

4-3. BUS STRUCTURE.

4-4. Figure 4-1 shows a brief logic diagram of the 2114B Bus Structure. This consists of certain logical functions which can be separated by function. At the top of this figure the memory module, the address decoding and driver switches, the sense amplifier, and inhibit driver are shown. The M-Register contains the memory address information for the core. This information is used by the driver switch assemblies to address the proper X and Y wires that traverse the core. The bit planes are interrogated by addressing currents. The sense amplifier is used to set the T-Register, and the T-Register is used in turn to drive the inhibit drivers to determine the proper writing data information.

4-5. This memory section consists of the 2 driver/switch boards and the memory module which can contain a 4K or and 8K unit. One each of the sense amp and inhibit driver assemblies are required for each 4K module. The minimum memory board count is 4 boards, the maximum would be 6 boards. The parity error is an additional board when this option is used. It is not shown on the bus structure diagram.

4-6. REGISTERS AND BUSES.

4-7. The registers contained in the 2114B Computer are the T, P, M, A, B, and Switch Registers. These registers are contained on the arithmetic logic card (4 bits per board). It requires 4 Arithmetic Logic cards to provide all 16 bits. (Refer to Figure 4-1.) The information from these registers can be read onto the S bus or R bus. The information on the R and S buses is manipulated with certain logical functions and the resultant appears on the T bus. The T bus can be stored in each of the 5 registers. The outputs from the registers are gated to the negative true S bus, and negative true R bus. Both of these buses are inverted, which provides the positive true S bus and R bus. It is the positive true S and R buses on which the logical functions are accomplished. The output goes to the T bus which is negative true. This negative true T bus provides inputs to the 5 registers. The limitations of the TTL logic prescribes the polarities of this bus structure since the only gate which can be OR tied must be OR tied in the negative true direction. The T bus negative true provides the D inputs to the 5 registers. The positive true output from these 5 registers is taken from the $\overline{Q}$ side of the flip flops.

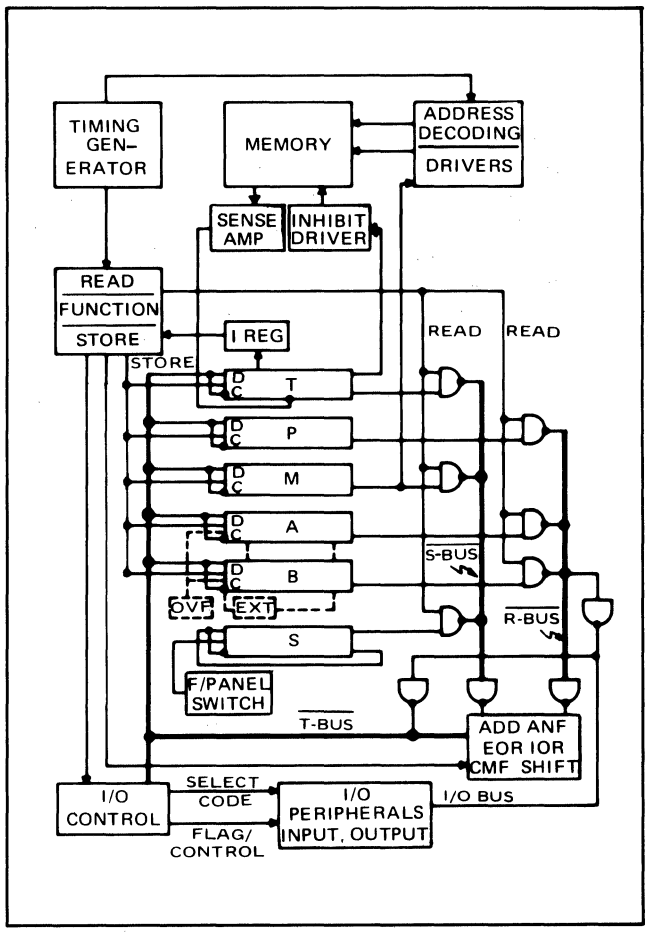


Figure 4-1. Bus Structure

4-8. SWITCH REGISTER.

4-9. The input to the Switch Register is the output of the proximity switch circuit on the front panel. Each time this proximity switch is operated the Switch Register toggles. Note that the output of the Switch Register comes from the Q side of the flip flop.

4-10. OVERFLOW AND EXTEND.

4-11. The Overflow Register provides a one bit register to determine when an arithmetic operation causes the A-Register or B-Register to overflow. The Extend Register couples the A-Register and B-Register for rotation to the left or to the right. It also indicates arithmetic carry from bit 15.

4-12. READ - STORE - FUNCTION.

4-13. The other signals required by the design of the central processor unit are the reading and storing signals and other logical functions. These are generated on the Instruction Decoder assembly and the Shift Logic assembly. The I-Register is located on the Instruction Decoder assembly and decodes bits 10 through 15 of the T-Register to determine what instruction or instruction group is being performed.

4-14. I/O INTERFACE.

4-15. The I/O Control assembly provides the flag, control, and interrupt circuitry for servicing the I/O peripheral devices. It encodes the select code information which is hard wired to each individual I/O slot. The I/O interface cards provide input/output registers. These registers utilize the input/output bus for transferring data from the device to the computer to the device. The I/O bus is read into the T-Bus for input information. The I/O bus recieves information from the R bus for output operations.

4-16. The I/O Control assembly also provides select code and interrupt information for servicing I/O extender and I/O multiplex options.

4-17. ARITHMETIC LOGIC ASSEMBLY.

4-18. The circuitry of the Arithmetic Logic assembly consists of 4 bits with the registers, bus structure logic, arithmetic, and shift mechanisms. Figure 4-2 shows the information on the arithmetic logic card for bit 11. There are certain inputs and outputs that differ for specific bits on the arithmetic logic card. You will note that the signals are the specific inputs associated with bit 11.

4-19. HARDWARE REGISTERS.

4-20. The arithmetic logic assembly contains 6 hardware registers, the T, P, M, A, and B-Registers and the Switch Register. It will be noted that the inputs to the T, P, M, A, and B-Registers is the T bus negative true to the input of this D type positive edge triggering flip flop. In order to utilize the information contained in these registers it is necessary to read information out of the registers onto the bus structure. After manipulation it is stored back in the appropriate register. The clock inputs to the T, P, M, A, and B-Registers allows storing the appropriate information from the T bus negative true. The 5 specific store instructions are the STBB, STBA, STBT, STM, and STP. The latter two being for bits 10-15. On the other arithmetic logic board provisions are made for storing in the M- and P-Registers bits 0 through 9. Information is read from the 6 registers into the S and R bus with the following 6 instructions: ISR, RMSB, RTSB, RBRB, RARB, and RPRB.

4-21. S-R BUS.

4-22. The contents of the hardware registers are read onto the S bus negative true, and R bus negative true. Each of these buses is inverted generating the R bus and S bus positive true as well. The output from the logical and shift operations is on the T bus negative true. This T bus negative true provides the D inputs to the T, P, M, A, and B-Registers.

4-23. LOGIC OPERATIONS.

4-24. The contents of the R and S buses are manipulated using 5 logic instructions Exclusive Or Function (EOF), And Function (ANF), Complement Function (CMF), Inclusive Or Function (IOF), and Add Function (ADF). The full adder for bit 11 is one quarter of the pack. The pack provides internal carry in from lower bits and external carry out at the end of each 4th bit. Interior carries (between bits on the card) are not required outside of the pack.

4-25. SHIFT — ROTATE.

4-26. The shift and rotate functions on the arithmetic logic card are provided by 5 signals. These are: Shift Left Magnitude (SLM), Shift Right Magnitude (SRM), Rotate Left 4 (RL4), Least significant bit Right to Sign bit (LRS), and Shift Left bit 14 (SL14). Since this figure is drawn representing bit 11 the specific inputs R bus bit 12 for a rotate or shift right, R bus bit 10 for shift or rotate left, and R bus 7 for rotate left 4 are shown. The Set Address Loader (SAL) gate is in the same general area on the assembly.

4-27. I/O BUS.

4-28. The I/O bus is brought to the arithmetic logic board. It is read into the $\overline{\text{T bus}}$ with the IOI input signal. It is possible to output from the R bus using IOCO, the input/output control signal. The Switch Register is also handled in the I/O system. The input to the Switch Register is a clock signal produced by the proximity switches on the front panel. The output Q is cross coupled providing the D input to the flip flop. This allows the flip flop contents to toggle each time the proximity switch is touched. The contents of the switch register are enabled to the bus structure with the Input Switch Register (ISR). The contents of the A-Register or B-Register can be output to the Switch Register in order to illuminate the Switch Register lamps. This is accomplished by clearing the contents of the Switch Register with the Clear Switch Register ($\overline{\text{CSR}}$) and then setting the Switch Register with the SSR signal which sets the Switch Register with the contents of the R bus.

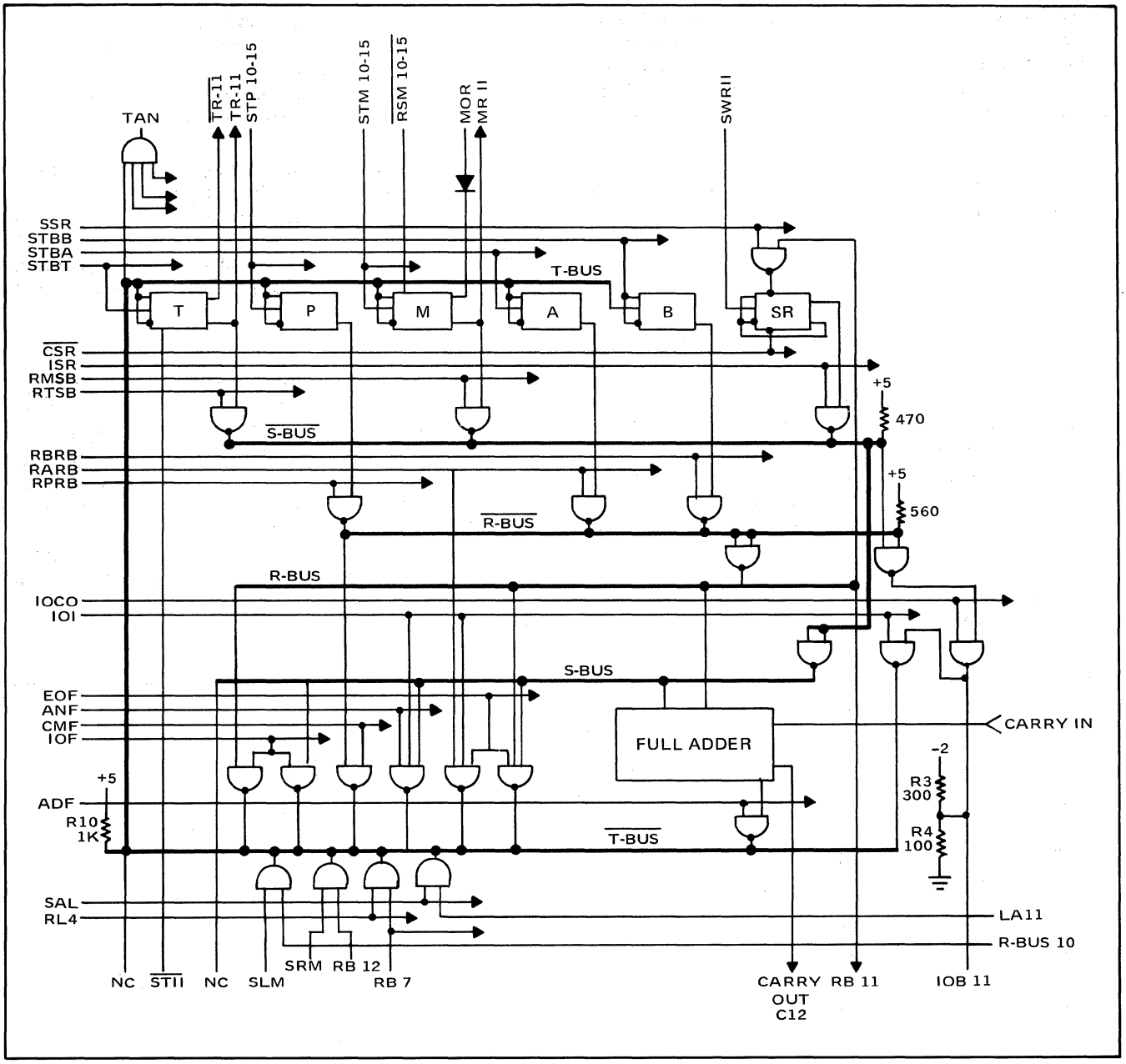


Figure 4-2. Arithmetic Logic

4-29. REGISTER DISPLAYS.

4-30. The contents of the hardware registers are available for driving lamp displays. The T-Register and M-Register are displayed on the 2114B front panel. The Switch Register is displayed on the front panel by lamps physically located under the proximity switch associated with the bit. The contents of the P-Register, A-Register, and B-Register do not have transistor drivers. The contents of those respective registers are available through isolation resistors on the 48 pin connector of the Arithmetic Logic board. External devices such as the Register Display Fixture utilize these outputs with their own transistor drivers to illuminate all of the hardware registers.

4-31. SYSTEM TIMING GENERATOR.

4-32. The system timing generator assembly contains five significant circuits.

4-33. OSCILLATOR AND DIVIDER.

4-34. Figure 4-3 shows the schematic for the oscillator and divider circuits. The oscillator is an integrated circuit design utilizing an 8 Mhz crystal. The output of this oscillator has sufficient rise time to operate the clock input of the 125ns flip flop. The 125ns flip flop is a divide by 2 circuit. The clock input is 8 Mhz, the output is 4 Mhz. Thus its output period is 250 nsec. The 4 Mhz signal drives the

clock inputs for the timing flip flops. The $\overline{Q}$ output drives the memory timing MST circuit. Figure 4-3 also shows the timing circuits used for generating the TS timing strobe signal. The output from integrated circuit pack MC71 pin 11 provides an approximate 60 nsec delay, and is used in the memory timing circuits.

4-35. Jumper W1 and the test points are used for in plant board testing.

4-36. TIMING SIGNALS.

4-37. Figure 2-4 shows the flip flops and buffering circuits for generating the computer timing signals. This circuit is reasonably straightforward. It consists of 8 flip flops for normal operation, plus two additional flip flops for time stretching required by the ISZ instruction. The output of the frequency divider 125ns flip flop in Figure 4-3 provides positive clock signals every 250 nsec. These clock signals are applied to each timing flip flop in parallel. It allows a timing pulse to propagate through the timing flip flops. The $\overline{Q}$ output of each timing flip flop drives a diode to the D input of flip flop T0. Thus, any other timing flip flop being set lowers the D input to flip flop T0 preventing the introduction of another timing pulse. When a timing pulse has propagated to flip flop T6 the D input to flip flop T0 is still held low. The next clock signal transfers the pulse from flip flop T6 to flip flop T7. At this point the D input to flip flop T0 goes high by making the input to the T0 flip flop look open since all the diodes are now reverse biased. The next clock signal introduces the next timing pulse into flip flop T0.

4-38. The outputs of the timing flip flops are buffered and provide timing signals to the computer. In addition to a normal T0, T1, and so on, there are certain composite signals. These include T12, T34, T45, and T67. The signals T2 called the ENF signal, T5 called the SIR signal, and T3 called the T3I/O, are available to the I/O section of the computer.

4-39. The operation of the pulse stretching circuits is as follows. In normal operation the ISZ signal is not present so that the NAND gate MC33 output pins 6 and 3 will normally go low when flip flop F5 is high. This negative true signal directly sets flip flops T6E and T7E. The high output from T7E allows the pulse train to propagate directly from T5 to T6. For operation with ISZ instruction during phase 3 the NAND gates 33 are not enabled so that the flip flops T6E and T7E are not set. The pulse train from flip flop T5 must then propagate through the two additional flip flops. This allows the additional 500 nsec timing stretch for the ISZ instruction.

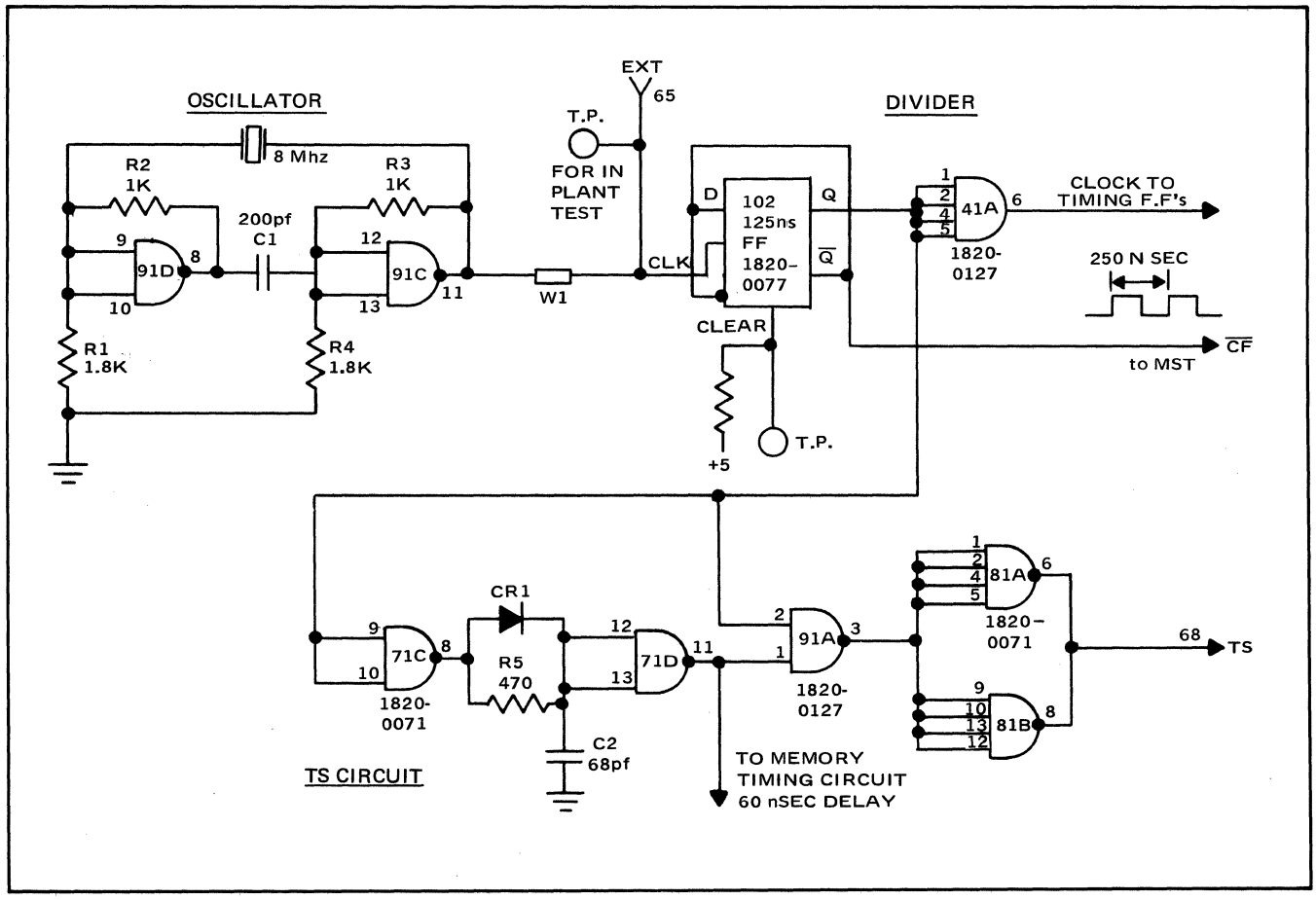


Figure 4-3. Oscillator and Divider

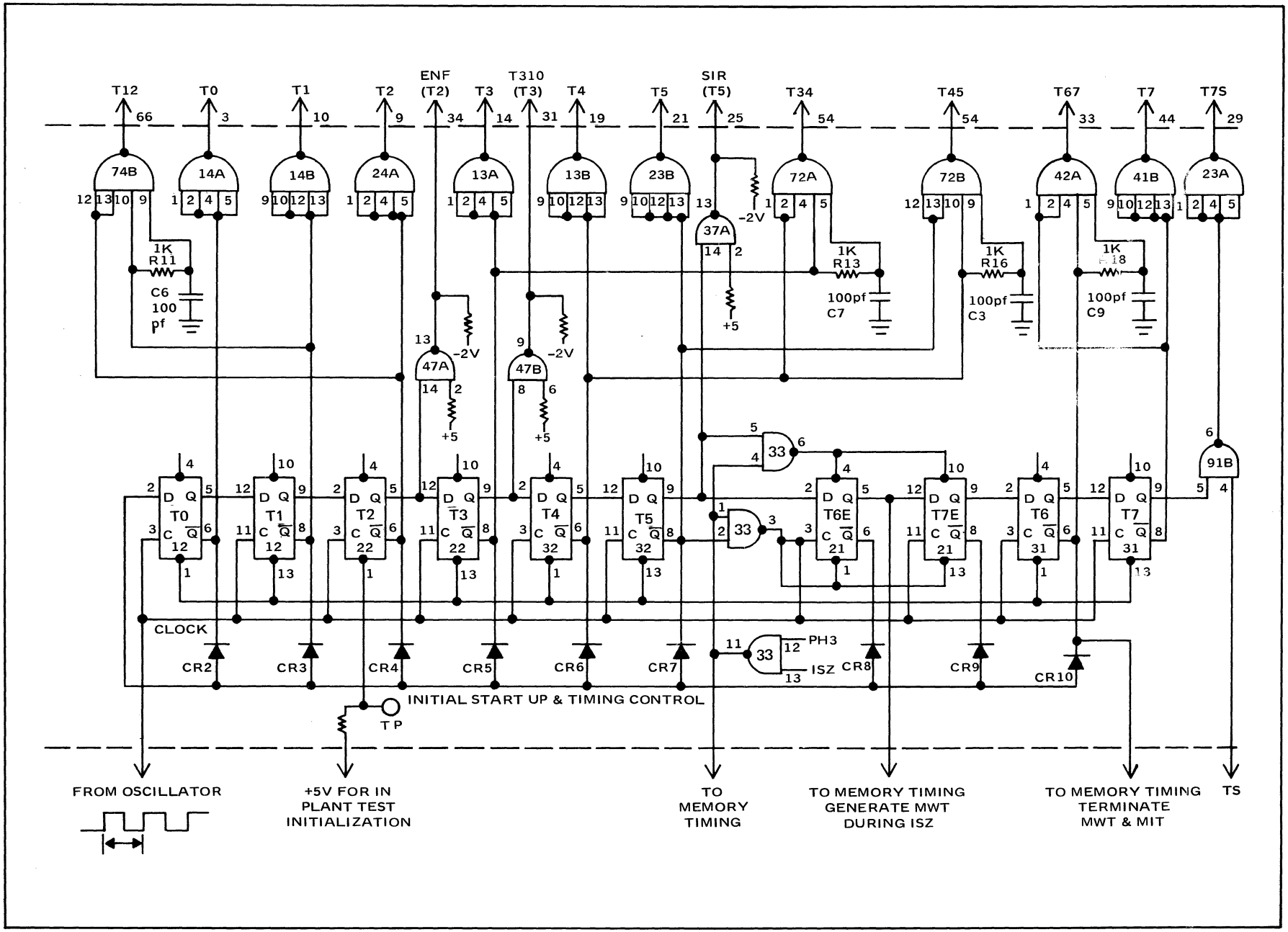


Figure 4-4. Timing Circuits

4-40. At Computer turn on the FF status is random. During the initial seven timing periods the status of the timing generator is correctly established. On each positive clock signal every pulse propagates through the flip flops, so that after a maximum of seven clock signals the proper operating conditions will have been established with one and only one pulse propagating. The computer PON signal is delayed by 300 milliseconds, thus no faulty computer operation can result during this required initialization.

4-41. MEMORY TIMING SIGNALS.

4-42. Figure 4-5 presents the schematic for the memory timing circuit. The presence of the MTE Memory Timing Enable signal indicates that the computer is in phase 1-2-3, Memory On switch is set, and we are not addressing the protected area. The presence of MTE signal permits operation of the memory timing generator. The MRT0 signal is generated at time T0. The MRT signal is delayed approximately 120 nsec. The MST signal is generated at time T1 · TS ANDed with the divider output from flip flop $\overline{125ns}$. The MST signal can be inhibited by the presence of certain signals such as addressing the A and B-Register, JSB, ISG, and so on. The function of jumper W2 in the MST circuit allows varying the time of MST for the 4 or 8K modules. The additional capacity in the 8K module requires that the MST signal be delayed. In the 4K installation jumper W2 is removed allowing MST signal to occur 30 or 40 nsec earlier.

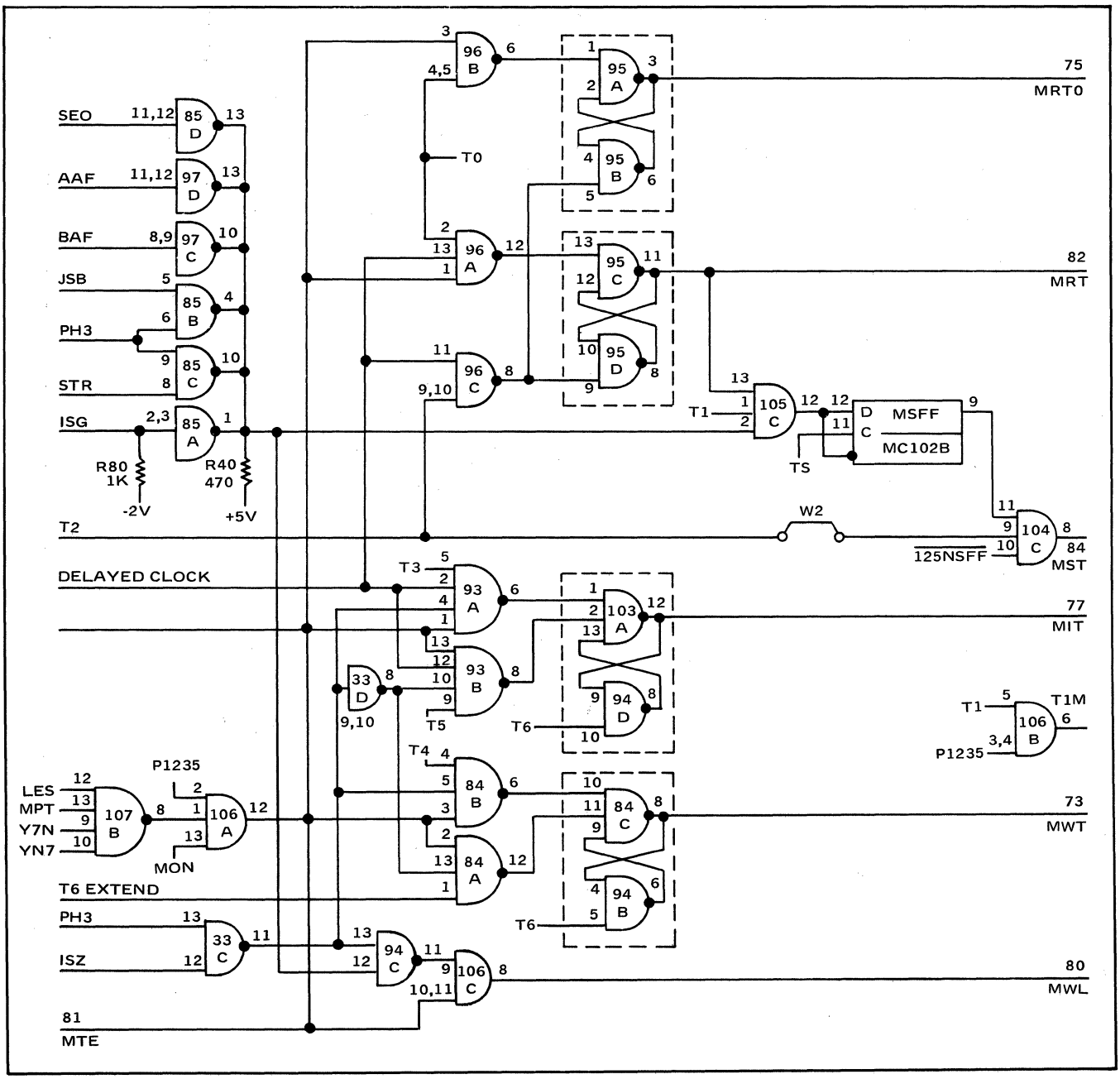


Figure 4-5. Memory Timing Signals

4-43. Inspection of the MIT, and MWT signals indicate inputs from the ISZ and PH3 signals. This permits delaying the MIT and MWT signals during the ISZ · PH3 operation.

4-44. RUN — STEP FF.

4-45. Figure 4-6 indicates the logic for the RUN and STEP Flip Flops. The purpose of the STEP flip flop is to allow single cycle operation. It also allows the computer to operate once when the RUN button is pushed until a halt is encountered. If it were not for this feature when the RUN button was pushed, the computer might encounter a halt instruction and restart before the RUN button could be released. The STEP flip flops provide logical control so that the RUN button must be released and then touched again to initiate another Computer Run cycle.

4-46. The operation of the STEP FF1 and STEP FF2 under single cycle operation is as follows. The D input to STEP FF1 is normally low by virtue of pack MC107. When RUN is initiated by any one of the following: LOAD MEMORY, DISPLAY MEMORY, or SINGLE CYCLE, the D input to STEP FF1 goes high. At the next T2 the clear output of STEP FF1 goes down. The Q output of STEP FF2 is still down therefore, a high J input is available on RUN FF2 but not on RUN FF1. At time T7S RUN FF2 is set enabling the phase gates for operation. At time T1 following, STEP FF2 is set which now removes the high input to RUN FF2. At time T7S RUN flip flop two is cleared and the operation ceases. Removing finger from the front panel control enables STEP FF 1 and STEP FF 2 to return to normal conditions.

4-47. The manner in which the computer begins to run is as follows. When the RUN button is pushed the STEP FF1 and STEP FF2 operation is as described above. Now, however, a high J input to RUN FF1 is also present. Thus, at time T5 prior to enabling RUN FF2 the Q output of FF1 goes low. The J input to RUN FF2 goes high for one cycle as before, however, now as it goes low the K input is also low so that the state of RUN FF2 remains unchanged. The RSP pulse initiates STEP and RUN Flip Flop operation the same as RUN. The LOAD button for Automatic Load also operates the same way.

4-48. There are three ways to terminate computer operation. The status of RUN FF1 must be changed. This is accomplished by one of the three signals to the K input. They are $\overline{\text{PEH}}$, $\overline{\text{HIN}}$, and HLL.

4-49. PHASE OPERATION.

4-50. Figure 4-7 shows the logic schematic for the phase circuits. The Phase operation follows a descending priority from phase 4 down to phase 1. A higher Phase request will inhibit any lower Phase request. The Phase 4 operation has the highest priority. It can be achieved under any computer conditions except a JSB or JMP simultaneous with an indirect IR15. Under any other circumstances Phase 4 can be requested.

4-51. Phase 3 can be requested by a DISPLAY MEMORY or LOAD MEMORY signal from the front panel, the completion of Phase 2 indirect, or the completion of Phase 1 which is not specifically a one phase only.

4-52. Phase 2 can be requested by a Phase 2 indirect instruction, or a Phase 1 indirect instruction.

4-53. It will be noted that the phase requests are on the J inputs of flip flops for Phase 2, Phase 3, and Phase 4. The Phase 1 request is on the K input of Phase 1 flip flop.

4-54. Phase 1 operation is normally provided by the absence of a request for Phase 2, Phase 3, or Phase 4 operation. Specific requests for Phase 1 include the completion of a JMP Phase 2, a load LAL, or the completion of a Phase 3.

Table 4-1. Set Phase Conditions

PHASE	SET	PREVENT
PHASE 1	1) LOAD ADDRESS, Automatic LOAD 2) Following PH4 3) Following PH3 (no PH4 req) 4) Following JMP · PH2 if I not set (no PH4 req)	1) PH2 req 2) PH3 req 3) PH4 req
PHASE 2	1) Following PH1, not OPO with I set (Bit 15) 2) Following PH2, I set	1) PH1 req 2) PH3 req 3) PH4 req
PHASE 3	1) DISPLAY MEM (Step FF) 2) LOAD MEM (Step FF) 3) Following PH2, no I set, not JMP, and no PH4 req 4) Following PH1, I not set, not JMP, not single phase instruction, no PH4 req	1) PH1 req 2) PH4 req
PHASE 4	1) INT req, computer running, no indirect 2) INT req, computer running, not JMP or JSB 3) INT req, computer running, and RSP	1) PH1 req

4-55. The outputs of the four Phase flip flops is NANDed with the $\overline{\text{PH5}}$ signal generated from DMA. It is then inverted to provide Phase 1, Phase 2, Phase 3, and Phase 4 signals to the computer. The output of the Phase flip flops also drives the Phase 1, 2, and 3 indicators on the front panel. Phase 4 lamp is located on the Timing Generator assembly. Setting of the PHASE loop switch on the front panel prevents clocking the Phase flip flops, so phase cannot be changed.

4-56. INSTRUCTION DECODER.

4-57. Referring to Figure 4-8, (page 21/22) the simplified block diagram, the instruction Decoder assembly contains the Instruction Register bits 10 through 15. It contains encoding to generate the Memory Reference Instructions.

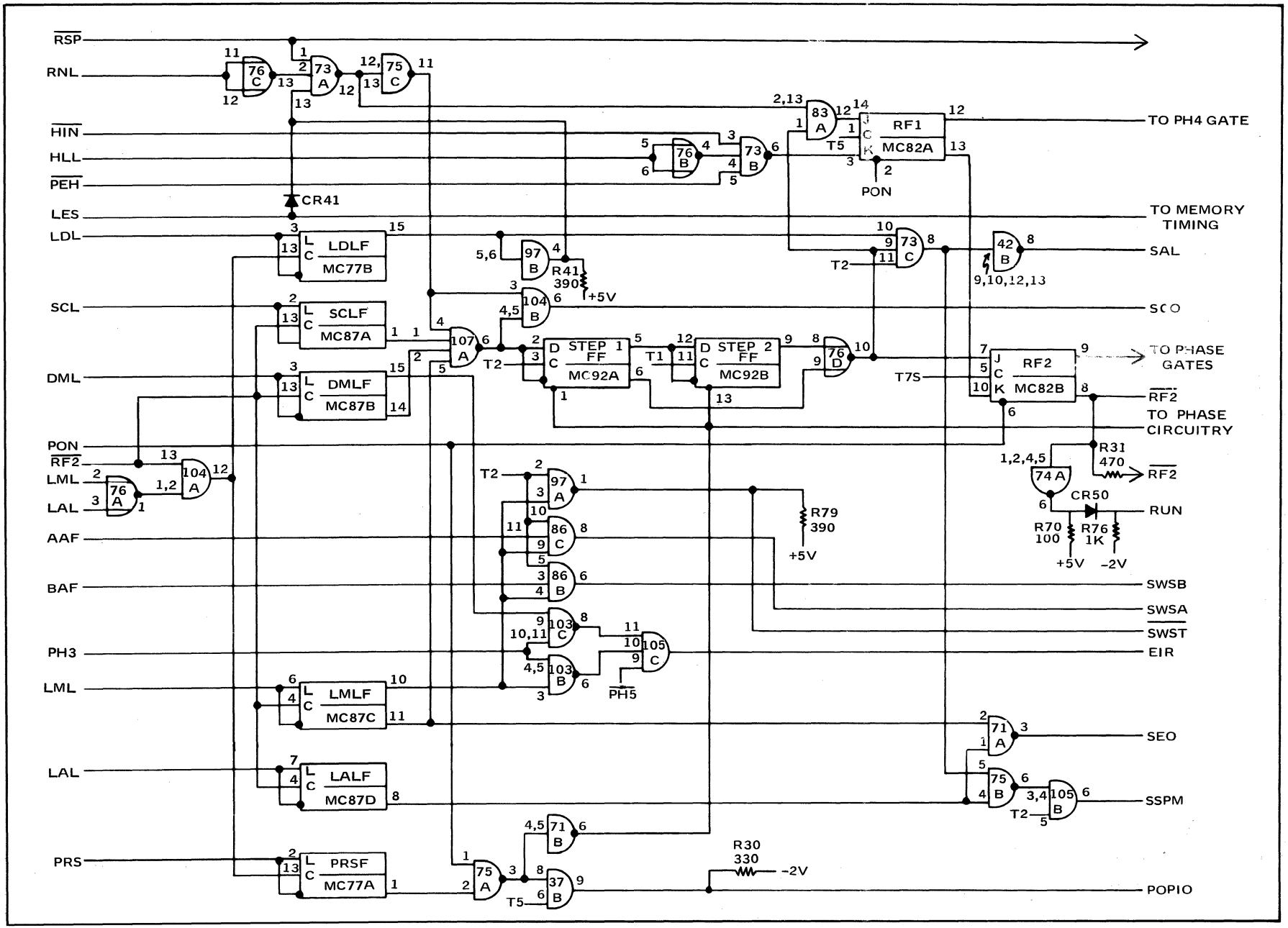


Figure 4-6. Run - Step FF's and Panel Controls

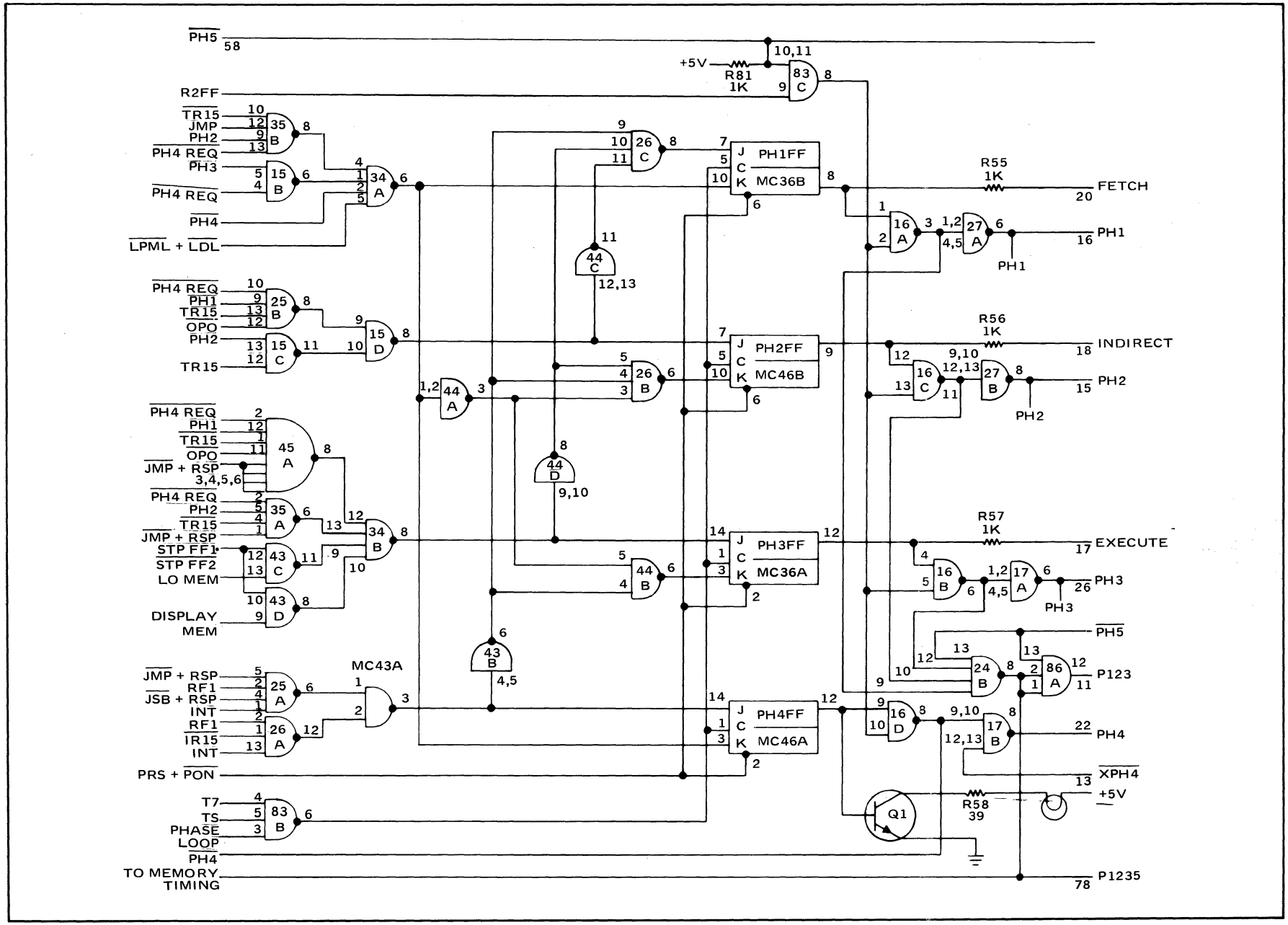


Figure 4-7. Phase Operation

These include JMP, IOA, CPA, JSB, and so on. They also provide the SRG, IOG, ASG, and OPO signals. The rest of the logic on the Instruction Decoder Assembly includes the various store, read and logical signals necessary for computer operation.

4-58. SHIFT LOGIC ASSEMBLY.

4-59. The Shift Logic Assembly contains numerous signals associated with shifting, rotating, I/O control, and the Overflow and Extend Flip Flops. In the upper right hand corner of the schematic diagram the various signals associated with shifting and rotating are generated.

4-60. The upper middle of the schematic diagram shows the various signals associated with I/O control, such as, IOO, IOCO, CLC, STF, and so on. The upper right margin of the schematic indicates the addressable A and B flip-flops.

4-61. The right margin of the schematic diagram indicates the Extend and Carry 0 flip flops. The logic for generating the Carry 0 is present in the lower margin of the schematic diagram. The Overflow Register is located in the lower left of the schematic diagram. The Overflow Register provides a numerical overflow from the A and B-Registers. It also provides a flag at select code 01. It can be interrogated to provide skip signals.

4-62. Shifts and Rotates use TB0 and TB15 for establishing conditions for bits 0 and 15. These circuits are on the left side of the schematic diagram.

4-63. OVERFLOW REGISTER.

4-64. The Overflow Register is a one bit register. It can be manipulated by various instructions in the I/O group. These include STF (S.C.01), CLF (S.C.01), SFC (S.C.01), and SFS (S.C.01). These instructions also have special op code (STO, CLO, SOC, SOS).

4-65. The Overflow Register also is set by numerical overflow conditions when using the ADA, ADB, INA, and INB instructions. (Although overflow may result from the use of ISZ this will not set the Overflow bit.) The necessary conditions depend on the sign of the data. RB15 · SB15 · $\overline{TB15}$ is the condition experienced when adding large negative numbers. Bit 15 is set but bit 14 is zero for a large number. Thus no carry is generated by the bits 14 to give a TB15.

4-66. In large positive numbers bit 15 is zero but bit 14 is set. This provides a condition $\overline{RB15}$ · $\overline{SB15}$ · TB15 for large positive numerical overflow (ADA/B or INA/B).

4-67. In either case the Overflow bit should be cleared prior to the addition, and checked right afterwards.

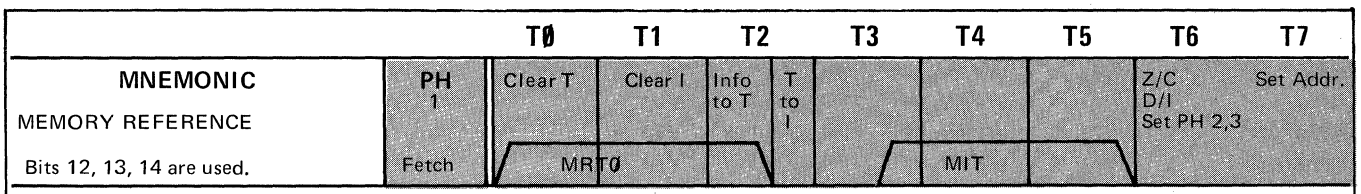
4-68. Its status can also be determined by the front panel lamp. The lamp is on when the register is set.

4-69. EXTEND REGISTER.

4-70. The Extend Register is a one bit register. It is used to detect a carry C16 from the ADA, ADB, INA, INB instruction. This would normally be encountered whenever adding two negative numbers (of any magnitude). The addition of a large positive number and a small negative number would also result in setting the Extend bit.

4-71. The Extend Register is very useful as an aid in linking the A and B-Registers while using multi-precision arithmetic. The EL A/B will clear or set the extend bit depending on the status of bit RB15. The ER A/B will clear or set depending on RB0. Both instructions can be enabled in both time periods. This results in a rather complex logic circuit to permit all combinations. The Direct instructions include CLE (Shift-Rotate, or Alterskip), CME, and CCE. The status interrogation includes SEZ and SEZ, RSS.

Table 4-2. Machine Instruction and Signals
MEMORY REFERENCE INSTRUCTIONS



TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
TØ	A13-26	P123 · TØ · TS →	MC25A	STBT	Clear T Reg.
T1	A13	PH1 · T1 →	MC71A	–	Clear I Reg.
T2	A12-84	MST	MC104C	MST	Info to T Reg.
	A13	PH1 · T2 · TS	MC52A	–	TR 10-15 → I Reg.
T67	A13-27	PH1 · EIR · $\overline{OPO}$ · T67 →	MC55B	RTSB	For Address Strobe to M
	A13-25	P123 · T67 →	MC54A	ADF	For ADDR to T bus
	A13-58	PH1 · EIR · $\overline{OPO}$ · T7S →	MC57B	STM Ø - 5	Strobe in Address
	A13-63	PH1 · EIR · $\overline{OPO}$ · T7S →	MC57B	STM 6 - 9	Strobe in Address
	A13-35	PH1 · IR1Ø · $\overline{OPO}$ · T7S →	MC57A	RSM 1Ø-15	Clear M Reg. 1Ø-15 force zero page (Z) Remain in Current page (C)
	A12-26	$\overline{PH4\ req.}$ · PH1 · $\overline{TR15}$ · $\overline{OPO}$ · $\overline{JMP}$ · T7 · TS →	MC45A · MC83B	PH3	Direct address (D)
	A12-15	$\overline{PH4\ req.}$ · PH1 · TR15 · $\overline{OPO}$ →	MC25B	PH2	Indirect Address (I)

Table 4-2. Machine Instruction and Signals (cont'd)
MEMORY REFERENCE INSTRUCTIONS (CONT'D)

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE JSB	PH 3 Ex	Clear T	P + 1 → T	M → P			P + 1 → P, M Set PH 1 ***	
X 001 IX			*	WRITE	**			

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T12	A13-65	PH3 · T12 · JSB →	NC21B	RPRB	Increment P-Reg and store in T-Reg.
	A13-19	PH3 · T12 · JSB →	MC32B	SB0	
	A13-25	PH3 · T12 · JSB →	MC53A	ADF	
	A13-26	PH3 · T2 · TS · JSB →	MC35A	STBT	
T3	A13-62	PH3 · T34 · JSB →	MC45B	RMSB	Store M-Register into P-Register
	A13-24	PH3 · T34 · EIR · JSB →	MC15B	EOF	
	A13-67, 68	PH3 · T4 · TS · JSB →	MC86B	STP0-9, 10-15	
*T2	A12-84	PH3 · JSB →	MC85B	$\overline{\text{MST}}$	Inhibit Memory Strobe

** T34 WRITE contents of M-Register is core ADDR for WRITE cycle. T-Register caontains the current program location plus 1 — This provides Inhibit Driver info to write the return address.

*** T67 P contains starting address for subroutine (NOP). Increment P-Register and store into P- and M-Registers.

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE AND	PH 3 Ex	Clear T		Info to T	AND		P + 1 → P, M set PH1	
X 001 0X		READ	MST		WRITE			

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T0	A13-26	P123 · T0 · TS →	MC25A	STBT	Clear T Reg.
		$\overline{\text{IR11}}$ · IR12 · $\overline{\text{IR13}}$ · $\overline{\text{IR14}}$ →	MC91A	ANA	AND Encoded
T34	A13-72	PH3 · T34 · $\overline{\text{IR11}}$ · $\overline{\text{IR14}}$ →	MC32A	RARB	Allow A-Reg to R-Bus
	A13-27	PH3 · T34 · EIR · $\overline{\text{JSB}}$ →	MC55A	RTSB	Allow T-Reg to S-Bus
	A13-23	ANA · PH3 · T34 →	MC25B	ANF	AND R-bus & S-bus to T-bus
	A13-73	PH3 · T5 · IR12 · $\overline{\text{CPA}}$ · AAF · TS → (MC25)	MC25C	STBA	Store T-bus into T-Reg
T67	A13-65	PH3· T67 →	MC22	RPRB	Allow P-Reg to R-bus
	A13-19	PH3 · T67 →	MC23	SB0	Increment P-Register
	A13-25	P123 · T67 →	MC54	ADF	
		PH3 · T7S→	MC11-MC77C	STP,M (ALL)	Store T-bus into P- & M-Reg.

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE LDA/LDB	PH 3 Ex	Clear T		Data to T	LOAD		P + 1 — P, M Set PH1	
X 110 A/B X		READ	MST		WRITE			

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T34	A13	$\overline{\text{IR12}}$ · IR13 · IR14 · EIR →	MC81B	$\overline{\text{LOD}}$	LOD encoded
	A13-27	PH2 · T34 · EIR · $\overline{\text{JSB}}$ →	MC55A	RTSB	
	A13-24	PH3 · T34 · EIR · LOD →	MC15B	EOF	
T4	A13-73, 74	PH3 · T4 · LOD · TS · {IR11 / $\overline{\text{IR11}}$} →	MC94C	STB A/B	

Table 4-2. Machine Instruction and Signals (cont'd)

MEMORY REFERENCE INSTRUCTIONS (CONT'D)

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE STA/STB	PH 3 EX	Clear T	A/B to T Reg			T to Driver	Inhibit	P + 1 → P,M Set PH 1
X 11Ø A/B X		READ			WRITE			

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
	A13-64	IR12 · IR13 · IR14 · EIR →	MC102A	STR	Store Encoded
T1	A13-72	P123 · T1 · {AAF / BAF} →	MC95	R (A/B) RB	
	A13-24	P123 · T1 →	MC14C	EOF	
	A13-26	P123 · T1 · TS · {AAF / BAF} →	MC34B	STBT	ref MC85 pin 10 Inhibits Memory
T2 T45	A12-84	PH3 · STR → $\overline{\text{T REG}}$	MC85C	$\overline{\text{MST}}$ IDØ-16	Controls writing infor To Inhibit Drivers

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE ISZ	PH 3 EX	Clear T	Data to T	TR + 1 → T		Cycle T6E	Stretch T7E	P + 1 + C0 → P, M Set PH 1
X Ø11 1 X		READ	MST			WRITE		

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
		IR11 · IR12 · IR13 · $\overline{\text{IR14}}$ · E1R →	MC82B	ISZ	
T34	A13-27	PH3 · T34 · E1R · $\overline{\text{JSB}}$ →	MC55A	RTSB	
	A13-20	ISZ · PH3 · T34 →	MC33A	RBØ	
	A13-25	ISZ · PH3 · T34 →	MC44A	ADF	
	A13-26	PH3 · ISZ · T4 · TS →	MC35B	STBT	
	A14-57	PH3 · ISZ · T4 · C16 →	MC56A	CØ	used at T67
T34 (Mem Inhibit)		$\overline{\text{PH3 · ISZ}}$ →	MC33C		(prevents MIT @ T3 · TS MWT @ T4)
T5		PH3 · ISZ →		T5 to T-6E to T-7E to T6	(MC33C pin 11) (Extra 500 nsec)
T5 (T6E & T7E)		PH3 · ISZ · MTE · T5 · TS delay → PH3 · ISZ · MTE · T-6E→	MC93B MC84A	MIT MWT	(MC98 pin 8) (MC84 pin 12)

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE ADA/ADB	PH 3 Ex	Clear T		Data to T	ADD			P + 1 → P, M Set PH 1
X 1ØØ A/B X		READ		MST		WRITE		

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T34	A13-71 72	PH3 · T34 · ADD · {$\overline{\text{IR11}}$ / IR11} →	MC94B	R (A/B) RB	Allow A/B-Register to the R-b
	A13-27	PH3 · T34 · EIR · $\overline{\text{JSB}}$ →	MC55A	RTSB	Allow T-Reg. to S-bus
	A13-25	PH3 · T34 · ADD →	MC44A	ADF	Add A/B and T-Reg to T-bus
	A13-73, 74	PH3 · T4 · ADD · TS · {$\overline{\text{IR11}}$ / IR11}	MC94C	STB (A/B)	Store T-bus into A/B-Reg
	A14-62	PH3 · T4 · ADD · C16 · TS →	MC21D	E	numerical carry
	A14-8	PH3 · T4 · ADD (RB15 : SB15 · $\overline{\text{TB15}}$ + $\overline{\text{RB15}}$ · $\overline{\text{SB15}}$ · TB15)	MC105B (MC12C + MC12B)	OVF	numerical overflow

Table 4-2. Machine Instruction and Signals (cont'd)
MEMORY REFERENCE INSTRUCTIONS (CONT'D)

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE XOR – IOR	PH 3 Ex	Clear T		Info to T	XOR — IOR			P + 1 → P, M Set PH 1
X Ø1(Ø/1) ØX		READ	MST					

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T34	A13-71, 72	PH3 · T34 · $\overline{IR14}$ · $\{\overline{IR11}, IR11\}$ →	MC32A	R A/B RB	Allow A/B Reg to R-bus
	A13-27	PH3 · T34 · EIR · JSB →	MC55A	RTSB	Allow T-Reg to S-bus
	A13-24	PH3 · T34 · EIR · $\overline{XOA}$ →		EOF	XOR
	A13-21	PH3 · T34 · IOA →		IOF	IOR
	A13-73, 74	PH3 · T5 · IR12 · $\overline{CPA}$ · TS · $\{AAF, BAF\}$ → (PH3 · T5 · IR12 · $\overline{CPA}$ = MC25)		STB A/B	Store T-bus into A/B registers

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE CPA/CPB	PH 3 Ex	Clear T		Data to T	CP	A/B		P + 1 + C0 → P, M Set PH 2
Compare, SKIP if UNEQUAL X 101 A/B X		READ	MST			WRITE		

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T34	A13-72	PH3 · T34 · CPA · $\{\overline{IR11}, IR11\}$ →	NC94B	R (A/B) RB	
	A13-27	PH3 · EIR · T34 · $\overline{JSB}$ →	MC55A	RTSB	
	A13-24	PH3 · T34 · EIR · CPA →	MC15B	EOF	
	A14-57	PH3 · T4 · CPA · TS → (TAN1 + TAN2 + TAN3 + TAN4) (T4 · CPA · TS = TAN 1,2,3,4)	MC15B	CØ	used at T67
T67	A13-65	PH3 · T67 →	MC22	RPRB	
	A13-19	PH3 · T67 →	MC23	SBØ	
	A13-25	P123 · T67 →	MC54	ADF	SBØ plus CØ
	A13-58, 63, 66, 67, 68	P3 · T7S →	MC77C	STM, P (all)	

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE	PH 2 Indirect	Clear T-Reg	Addr to T-Reg				T-Reg → M-Reg D set PH3 I set PH2	

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
TØ	A13-26	P123 · TØ · TS →	MC25A	STBT	Clear T-Reg.
T67	A13-27	PH2 · T67 · EIR →	MC45C	RTSB	New Address
	A13-25	PH123 · T67 →	MC54A	ADF	Allow address to T-bus
	A13-58	PH2 · T7S →	MC11	STM Ø - 5	Store Address
	A13-63	PH2 · T7S→	MC11	STM 6 - 9	
	A13-66	PH2 · T7S →	MC11	STM 10-15	
	A12-15	PH2 · TR15 · T7 · TS → (If no PH4 req.)	MC15C · MC83B	PH2	Indirect (I)
	A12-26	PH2 · $\overline{TR15}$ · T7 · TS → (If no PH4 req.)	MC35A	PH3	Direct (D)

Table 4-2. Machine Instruction and Signals (cont'd)

MEMORY REFERENCE INSTRUCTIONS (CONT'D)

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE JMP	PH 1	Clear T	Clear I	TR10-15 to I			Z 0 → M 10-15 D T → P, M (0-9) Set PH 1 I T → M (Set PH 2)	
D/I 010 1 Z/C		READ	MST		WRITE			

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T67	A13-27	PH1 · T67 · $\overline{OPO}$ · EIR →	MC55B	RTSB	
	A13-25	PH123 · T67 →	MC54	ADF	
	A13-63, 58	PH1 · T7S · OPO · EIR →	MC11B	STM 0-5, 6-9	Current Page (C)
	A13-69	PH1 · T7S · JMP · $\overline{IR15}$ →	MC86A	STP 0-9	Direct Address (D)
		(Set PH1 by no – PH2, 3, 4, req)			
	A13-58, 63	PH1 · T7S · $\overline{OPO}$ · EIR →	MC57B	STM 0-5, 6-9	Current Page (C)
	A12-15	PH1 · IR15 · $\overline{OPO}$ · $\overline{PH4\ REQ}$ →	MC25B	SET PH2	Indirect Address (I)
	A13-35	PH1 · T7S · $\overline{OPO}$ · $\overline{IR10}$ →	MC57A	RSM 10-15	Zero Page (Z)

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC MEMORY REFERENCE JMP	PH 2 Ind	Clear T	Addr to T				D TR → P, M SET PH 1 I TR → M SET PH 2	
		READ	MST		WRITE			

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T67	A13-27	PH2 · T67 · E1R →	MC45C	RTSB	
	A13-25	P123 · T67 →	MC54	ADF	
	A13-58, 63 66	PH2 · T7S →	MC11	STM 0-9, 10-15	
	A13-67, 68	PH2 · $\overline{TR15}$ · T7S · JMP →	MC75	STP 0-9, 10-15	Direct Address (D)
	A12-16	PH2 · $\overline{TR15}$ · JMP · $\overline{PH4\ req}$ →	MC25B	SET PH1	
	A12-15	PH2 · IR15 →	MC15C	SET PH2	Indirect Address (I)

SHIFT ROTATE

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC SHIFT-ROTATE ALTER SKIP	PH 1 Fetch	Clear T Reg STBT	Clear I Reg	T Reg → I Reg		T Reg to Inhibit Driver		P + 1 + C0 → P, M Set PH1
		READ	Strobe MST		WRITE			

TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
T0	A13-26	P123 · T0 · TS →	MC25A	STBT	Clear T-Register
T1	A13	PH1 · T1	MC71A		Clear I -Register
T2	A13	PH1 · T2 ; TS	MC52A,		TR 10-15 → I-Register
T67	A13-65	OPO · T67 →	MC22	RPRB	
	A13-25	P123 · T67 →	MC54	ADF	Includes SB0 and C0
	A13-63,58 66,67,68	OPO · T7S →	MC11, MC77B	STM, P	

NOP SHIFT-ROTATE WITH NOTHING ENABLED. (i.e., Bits 9, 4 all zero)

Table 4-2. Machine Instruction and Signals (cont'd)

SHIFT ROTATE (CONT'D)

				T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC				PH 1							
ALL SHIFT-ROTATE				Fetch			Bits 6-9	Bits 3, 5	Bits 0-2,4		
TIME	SOURCE	EQUATION			GATE		MNEMONIC		PURPOSE		
T3	A13-71, 72	SRG · T3 →			MC84B		R (A/B) RB				
	A14-80	SRG · TR6, 7, 8 · T3 →			MC51B		RL4		*LF		
	A14-78	SRG · TR6 · T3 $(\overline{TR7} + \overline{TR8})$ →			MC104B		SRM		*RS, R*R, ER*, *LF		
	A14-75	SRG · $\overline{TR6}$ · T3 →			MC105C		SLM		*LS, R*L, *LR, EL*		
	A14-72	SRG · T3 · TR6 · TR7 · $\overline{TR8}$ →			MC91		LRS		R*R		
	A14-69	SRG · T3 · $\overline{TR6}$ · TR7 · $\overline{TR8}$ →			MC101		SLØ		R*L		
	A14-71	SRG · T3 · $\overline{TR6}$ · TR7 →			MC86B		SL14		R*L, EL*		
	A14-82	SRG · E · T3 · $\overline{TR6}$ · TR7 · TR8 →			MC87B		$\overline{TBØ}$		EL*		
	A14-24	SRG · E · T3 · TR6 · $\overline{TR7}$ · TR8 →			MC102		$\overline{TB15}$		ER*, *LR		
	A13-73, 74	SRG · T3 · TS · TR9 · $\left\{\begin{matrix}\overline{TR11}\\TR11\end{matrix}\right\}$ →			MC93C		STB (A/B)				
T4	A14	SRG · T4 · TR5			MC62C				Clear Extend CLE		
	A13-73	SRG · T45 · $\left\{\begin{matrix}\overline{IR11}\\IR11\end{matrix}\right\}$ →			MC 85		R (A/B) RB		SL (A/B)		
	A14-57	SRG · $\overline{RBØ}$ · TR3 · T4 →			MC75A		CØ		Skip Condition		
T5	Refer T3 above T3 → T5; TR8 → TR2; TR7 → TR1; TR6 → TRØ										

				T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC				PH 1							
ALTER SKIP				Fetch			Bits 5-7,0				
EXTEND REGISTER INSTRUCTIONS											
INSTRUCTION	SOURCE	EQUATION			GATE		MNEMONIC		PURPOSE		
CLE	A14	ASG · TR6 · $\overline{TR7}$ · T3 →			MC61A		K INPUT				
CME	A14	ASG · $\overline{TR6}$ · TR7 · T3 →			MC42		K INPUT				
		ASG · TR7 · T3 →			MC103		J INPUT				
CCE	A14	ASG · TR7 · T3 →			MC103		J INPUT				
SEZ	A14-57	ASG · TR5 · T3 · $\overline{E}$ · $\overline{TRØ}$ →			MC76		CØ		at T67		
		ASG · TR5 · T3 · E · TRØ →			MC76		CØ		at T67		

				T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC				PH 1							
ALTER SKIP				Fetch			Bits 8, 9				
CLEAR & COMPLEMENT INSTRUCTIONS											
INSTRUCTION	SOURCE	EQUATION			GATE		MNEMONIC		PURPOSE		
		S BUS, R BUS are Ø									
CL A/B	A13-24	ASG · T3 · $\overline{TR9}$ →			MC13A		EOF				
	A13-73, 74	ASG · $\left\{\begin{matrix}IR11\\\overline{IR11}\end{matrix}\right\}$ · T3 · TS →			MC105 A/B		STB (A/B)				
CM A/B	A13-71, 72	ASG · $\overline{TR8}$ · T3 →			MC96B		R A/B RB				
	A13-22	ASG · TR9 · T3 →			MC17		CMF				
	A13-73, 74	ASG · $\left\{\begin{matrix}IR11\\\overline{IR11}\end{matrix}\right\}$ · T3 · TS →			MC105A/B		STB (A/B)				
		S BUS AND R BUS ARE Ø									
CC A/B	A13-22	ASG · TR9 · T3 →			MC17		CMF				
	A13-73, 74	ASG · $\left\{\begin{matrix}IR11\\\overline{IR11}\end{matrix}\right\}$ · T3 · TS			MC105A/B		STB (A/B)				

Table 4-2. Machine Instruction and Signals (cont'd)

SHIFT ROTATE (CONT'D)

		T∅	T1	T2	T3	T4	T5	T6	T7
MNEMONIC ALTER SKIP	PH 1 Fetch						Bits 0, 1 ↑		

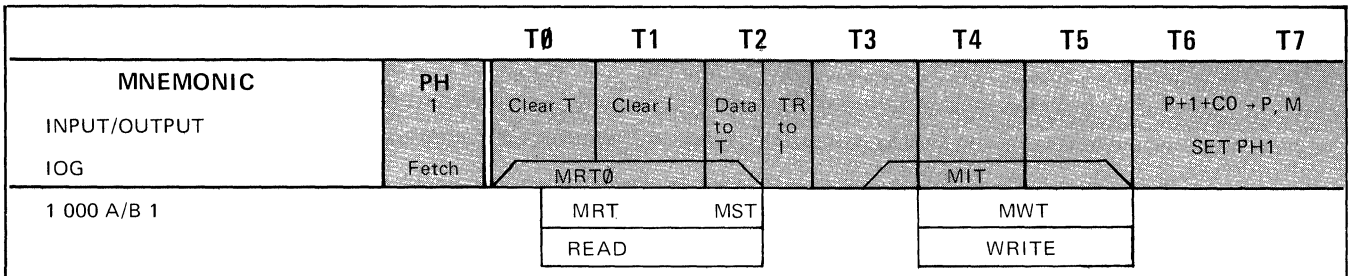
INSTRUCTION	SOURCE	EQUATION	GATE	MNEMONIC
SZ A/B	A13-72	ASG · T45 · $\{\overline{IR11}, IR11\}$ →	MC85	R (A/B) RB
	A13-25	ASG · T45 →	MC54	ADF
	A14-57	ASG · T5 · TR1 · $\overline{TR∅}$ · ($\overline{TAN1}$ + $\overline{TAN2}$ + $\overline{TAN3}$ + $\overline{TAN4}$) →	MC64A	C∅
	A14-57	ASG · T5 · TR1 · TR∅ · TAN 1, 2, 3, 4 →	MC63A	C∅

		T∅	T1	T2	T3	T4	T5	T6	T7
MNEMONIC ALTER SKIP	PH 1 Fetch						Bits ∅, 2-4 ↑ SKIP SIGN BIT, ZERO BIT, & INCREMENT		

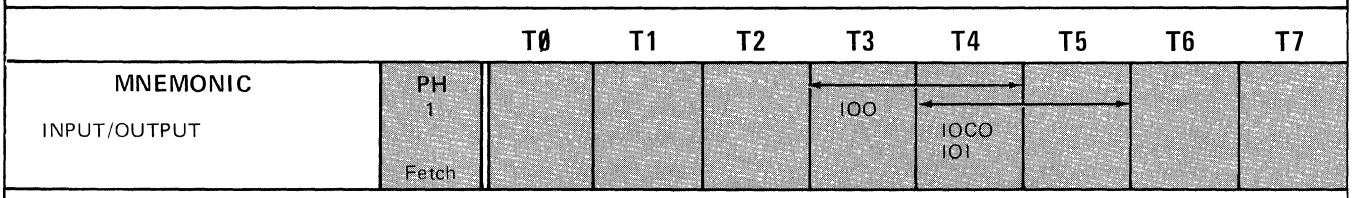
INSTRUCTION	SOURCE	EQUATION	GATE	MNEMONIC
SS A/B	A13-72	ASG · T45 · $\{\overline{IR11}, IR11\}$ →	MC85	R (A/B) RB
	A14-57	ASG · T4 · TR4 · $\overline{RB15}$ · $\overline{TR∅}$ →	MC56B	C∅
	A14-57	ASG · T4 · TR4 · RB15 · TR∅ · $\overline{TR3}$ →	MC15A	C∅
	A14-57	ASG · T4 · TR4 · RB15 · TR∅ · $\underbrace{TR3 \cdot RB∅}$ → (SL*)	MC63	C∅
SL A/B	A13-71, 72	ASG · T45 · $\{\overline{IR11}, IR11\}$ →	MC85	R (A/B) RB
	A14-57	ASG · T4 · TR3 · $\overline{RB∅}$ · $\overline{TR∅}$ →	MC75B	C∅
	A14-57	ASG · T4 · TR3 · RB∅ · TR∅ · $\overline{TR4}$ →	MC64B	C∅
	A14-57	ASG · T4 · TR3 · RB∅ · TR∅ · $\underbrace{TR4 \cdot RB15}$ → (SS*)	MC63	C∅
IN A/B	A13-71, 72	ASG · T45 · $\{\overline{IR11}, IR11\}$ →	MC85	R (A/B) RB
(T4 & T5)	A13-19	ASG · TR2 · T45 →	MC23	SB∅
	A13-25	ASG · T45 →	MC54	ADF
	A13-73, 74	ASG · TR2 · T5 · $\{\overline{IR11}, IR11\}$ · TS →	MC93B	STB (A/B)
	A14-62	ASG · TR2 · C16 · T4 · TS →	MC21A	EXTEND

Table 4-2. Machine Instruction and Signals

INPUT/OUTPUT



TIME	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
	A13-53	$\overline{TR12} \cdot \overline{TR13} \cdot \overline{TR14} \cdot PH1 \rightarrow$	MC73B	OPO	
	A13-52	OPO · IR10 · IR15 →	MC52C	IOG	
TØ	A13-26	P123 · TØ · TS→	MC25A	STBT	Clear T-Register
T1	A13	PH1 · T1 →	MC71A	–	Clear I -Register
T2	A13	PH1 · T2 · TS →	MC52A	–	TR1Ø-15 to I-Register
T67	A13-65	OPO · T67→	MC22	RPRB	
	A13-15	P123 · T67→	MC54	ADF	SBØ plus CØ
	A13-58,63,66	OPO · T7S →	MC11	STM (all)	
	A13-67,68	OPO · T7S →	MC77B	STP (all)	



INSTRUCTION	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
MI (A/B)	A13-71, 72	IOG · $\overline{TR6}$ →	MC74B	RARB	
	A13-52	IOG · $\overline{TR7}$ · TR8 · T45 →	MC71A	IOI	
		IOI · IOG · (SC) →		Data to IOB (BUS)	ON INTERFACE
	A8→A11	IOI STROBES IOB	MC104	T-BUS	
	A13-21	IOG · T45 →	MC14A	IOF	
	A13-73, 74	IOG · $\overline{TR7}$ · TR8 · T5 · TS · $\{\overline{IR11}, IR11\}$ →	MC83A	STB (A/B)	
	A14-17	TR9 · T4 →	MC36B	CLF	
LI (A/B)	A13-52	IOG · $\overline{TR7}$ · TR8 · T45 →	MC71A	IOI	
		IOI · IOG · (SC) →		Data to IOB (BUS)	INTERFACE
	A8→A11	IOI STROBES IOB →	MC104	T-BUS	
	A13-21	IOG · T45 →	MC14A	IOF	
	A13-73, 74	IOG · $\overline{TR7}$ · TR8 · T5 · TS · $\{\overline{IR11}, IR11\}$ →	MC83B	STB (A/B)	
	A14-17	TR9 · T4 →	MC36B	CLF	
OT(A/B)	A13-71, 72	IOG · $\overline{TR6}$ · $\{\overline{IR11}, IR11\}$ →	MC74B	RARB	
	A14-19	IOG · $\overline{TR6}$ · TR7 · TR8 · T45 →	MC36A	IOCO	
	A8 → A11	IOCO STROBES R BUS TO IOB (BUS)	MC62,MC101		
	A14-13	$\overline{TR6}$ · TR7 · TR8 · T34 · IOG →	MC37A	IOO	
		IOO · (SC) · STROBES IOB INTO BUFFER			INTERFACE
	A14-17	TR9 · T4 →	MC36B	CLF	

Table 4-2. Machine Instruction and Signals (cont'd)

INPUT/OUTPUT (CONT'D)

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC INPUT/OUTPUT	PH 1 Fetch						P + 1 + C0 → P, M SET PH1	

INSTRUCTION	SOURCE	EQUATION	GATE	MNEMONIC	PURPOSE
STF	A14-15	IOG · T3 · TR6 · $\overline{TR7}$ · $\overline{TR8}$	MC37B	STF	STF sets Flag FF @ S.C. STF → Clears Int. Control FF T-Reg infor present for S.C. STF (S.C. ØØ) sets IEN
CLF	A14-17	IOG · TR9 · T4	MC36B	CLF	CLF → Reset Flag FF @ S.C. CLF → Clear Int. Control FF T-Reg info present for Select Code
SFC	A14-21	IOG · $\overline{TR6}$ · TR7 · $\overline{TR8}$	MC47B	SFC	Test condition of Flag FF on interface cards SFC (S.C. Ø1) tests condition of OVF FF SFC (S.C. ØØ) tests condition of Int. Enable FF
SFS	A14-27	IOG · TR6 · TR7 · $\overline{TR8}$		SFS	Tests condition of Flag FF on interface card SFS (S.C. Ø1) tests condition of OVF FF SFS (S.C. ØØ) tests condition of Interrupt Enable FF

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC INPUT/OUTPUT	PH 1 Ex			STO CLO SOC				

INSTRUCTION	SOURCE	EQUATION	GATE	MNEMONIC
STC	A14-25	TR6 · TR7 · TR8 · $\overline{TR11}$ · T4 → STC · (SC) →	MC46B	STC SETS FF
CLC	AI4-23	TR6 · TR7 · TR8 · TR11 · T4 → CLC · (SC) →	MC47A	CLC CLEARS FF
STO	A14-15	TR6 · $\overline{TR7}$ · $\overline{TR8}$ · T3 → STF · (SCØ1) · IOG · TS →	MC11A	STF Set OVF
CLO	A14-17	TR9 · T4 → CLF · IOG · (SCØ1) →	MC35B	CLF Clear OVF
SOC	A14-21	$\overline{TR6}$ · TR7 · $\overline{TR8}$ → SFC · (SCØ1) · IOG · T4 · $\overline{OVF}$ →	MC82B	SFC CØ at T67
	A14-17	C - TR9 · T4 →		CLF
SOS	A14-27	TR6 · TR7 · $\overline{TR8}$ → SFS · OVF · IOG · (SCØ1) · T4 →	MC82A	SFS CØ at T67
	A14-17	C - TR9 · T4 →		CLF

	T0	T1	T2	T3	T4	T5	T6	T7
MNEMONIC INPUT/OUTPUT HLT	PH 1 Fetch	Clear T	MST	Info to I		Reset RF1	P →	P, M Reset RF2
		READ			WRITE			

SOURCE	EQUATION	GATE	MNEMONIC
A14-64	IOG · $\overline{TR6}$ · $\overline{TR7}$ · $\overline{TR8}$ HIN · T5	MC87A MC73B	HIN RESET RF1
A13-65	OPO · T67	MC22	RPRB
A13-25	P123 · T67	MC54	ADF
A13-58, 63,66	OPO · T7S	MC11	STM Ø-5, 6-9, 1Ø-15
A13-67,68	OPO · T7S	MC77B	STP Ø-9; 1Ø-15
A12	$\overline{RF1}$ · T7S		RESET RF2

Table 4-2. Machine Instruction and Signals (cont'd)

PHASE 4

	T∅	T1	T2	T3	T4	T5	T6	T7
MNEMONIC INTERRUPT *	PH 4	CM P → P		INC P → P		CMP → P		CLM6-15 STM∅-5 SET PH1

*Refer to Figure 6-1.

TIME	SOURCE	EQUATION	GATE	MNEMONIC
T12	A13-65	PH4 · T12→	MC22	RPRB
	A13-22	PH4 · T12→	M17	CMF
	A13-67, 68	PH4 · T2 · TS→	MC76C	STP ∅-9, 1∅-15
T34	A13-65	PH4 · T34→	MC21A	RPRB
	A13-19	PH4 · T34→	MC23	SB∅
	A13-25	PH4 · T34→	MC54	ADF
	A13-67, 68	PH4 · T45 · TS→	MC76B	STP ∅-9, 1∅-15
	A15	PH4 · T3IO→	MC13B	Clears Interrupt Control FF
T5	A13-65	PH4 · T5 →	MC22	RPRB
	A13-22	PH4 · T5 →	MC17	CMF
	A13-67, 68	PH4 · T45 · TS→	MC76B	STP ∅-9, 1∅-15
T7	A13-32, 35	PH4 · T7 →	MC56B,MC74C	$\overline{\text{RSM 6-9}}$, $\overline{\text{1∅-15}}$
	A15	$\overline{\text{RSM 6-9}}$ →	MC94F	Select Code to Central Int. Reg.
	A15	$\overline{\text{RSM 6-9}}$ →	MC85C	Central Interrupt Reg → $\overline{\text{T-Bus}}$
	A13-58	PH4 · T7S→	MC12D	STM ∅-5
	A12	PH4→		PH1

	T∅	T1	T2	T3	T4	T5	T6	T7
MNEMONIC 1st machine cycle following interupt PHASE 4	PH 1 Fetch	IAK Clear Flag Buffer	Clear IRQ FF				STM Set Inhibit	6-9 Interrupt FF

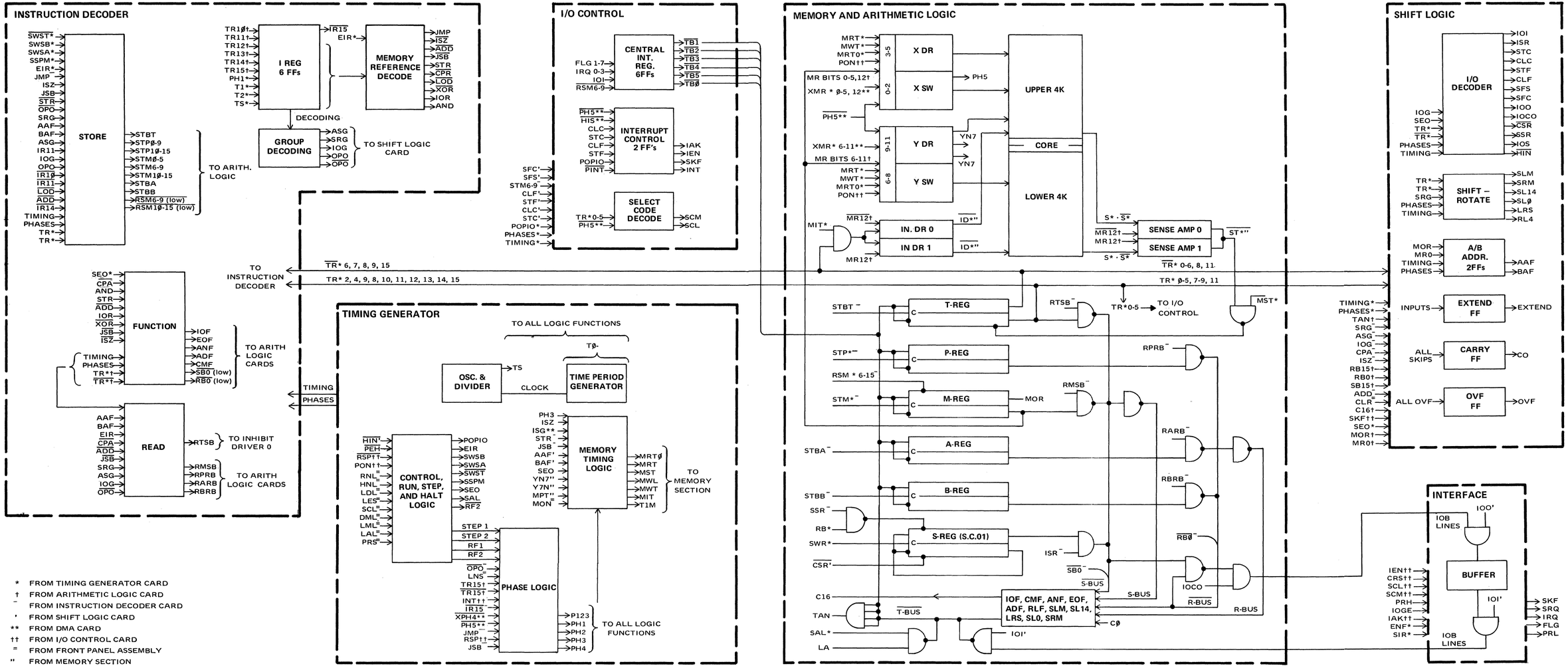
PERFORMS INSTRUCTION IN TRAP CELL.
This trap cell instruction is usually a JSB or JSB,I which stores the P-Register contents to allow a return to the Program in Process.

TIME	SOURCE	EQUATION	GATE	MNEMONIC
T1	A15-10	PH1 · T1 $\overline{\text{INTERRUPT CONTROL}}$→	MC36C on Interface card	IAK
		IAK · IRQ FF (Device) →		Clears Flag Buffer
T2		T2		Clears IRQ FF (device)
T7	A13-63	PH1 · T7S · ($\overline{\text{OPO}}$ · EIR + OPO)→	MC57B, MC11	STM 6-9
	A15-16	STM 6-9 →		Sets Interrupt Inhibit FF

	T∅	T1	T2	T3	T4	T5	T6	T7
MNEMONIC 2nd Machine Cycle Following Interrupt Phase 4	PH 1, 2, 3	T∅ · TS						

PURPOSE

T∅ · TS clears Interrupt Inhibit. This sets Interrupt Control FF. After T∅ Higher Priority Interrupts can be serviced (ESR High again). Subroutine must clear Flag (device) to allow PRL line to function.



* FROM TIMING GENERATOR CARD
† FROM ARITHMETIC LOGIC CARD
¯ FROM INSTRUCTION DECODER CARD
' FROM SHIFT LOGIC CARD
** FROM DMA CARD
†† FROM I/O CONTROL CARD
= FROM FRONT PANEL ASSEMBLY
'' FROM MEMORY SECTION

Figure 4-8. Simplified Block Diagram

MEMORY

V

SECTION V
MEMORY

5-1. INTRODUCTION.

5-2. The 2114B computer contains a ferrite toroidal memory module. The cores are arranged in an array with appropriate address mechanisms. Driver-Switch boards provide the means to convert address information into actual core reading and writing currents. The Sense Amplifier detects the state of the core during read operation. The Inhibit Driver permits setting the state of the core during write cycles.

5-3. The core module design permits providing either 4096 addresses (called 4 "K") or 8192 (called 8 "K") within the package. The actual reading or writing requires power, but the passive core condition doesn't require any power consumption to retain the core information.

5-4. MEMORY TIMING.

5-5. The basic computer memory timing remains the same during each cycle (except for ISZ). Early in the cycle the information is read out of the core. This process destroys the information content. It is necessary to rewrite the information back into core later in the cycle.

5-6. The approximate time required for the read or write operation is 500 nsec. The computer architecture was designed around the read time occurring during time periods T0 to T2, and write time T3 to T5. More specific timing information will be given in paragraph 5-9.

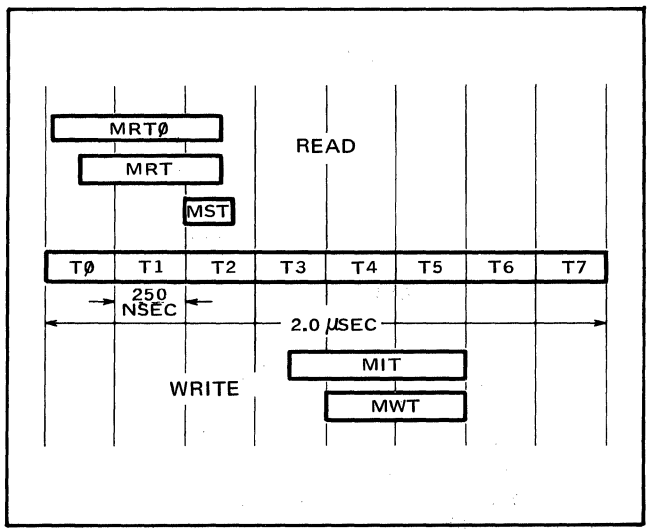


Figure 5-1. Memory Timing.

5-7. FERRITE CORE CHARACTERISTICS.

5-8. The utilization of ferrite materials for computer memories depended on the development of rectangular hysteresis loop material. Refer to Figure 5-2. The toroid provides a flux linkage between the primary winding and the secondary winding of a transformer. The flux will be oriented essentially one of two possible directions, referred to as being a "zero" or a "one".

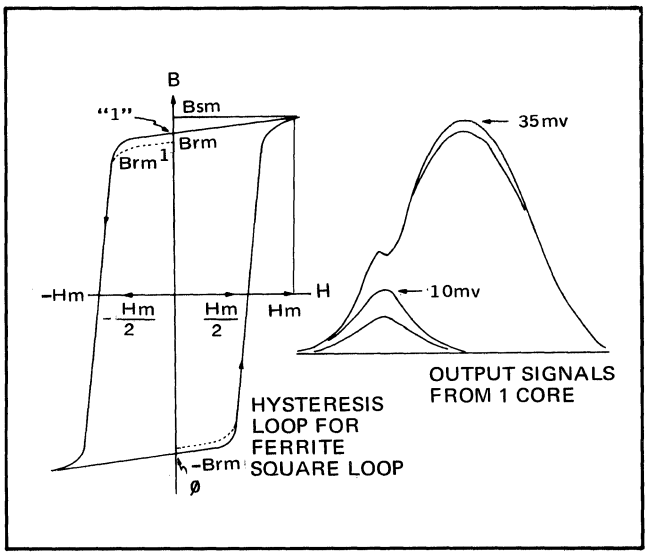


Figure 5-2. Core Characteristics

5-9. The physical nature of the ferrite material retains the flux condition (polarity) until a certain current magnitude is applied to the primary winding. When the current increases to the proper level the flux reversal takes place rather abruptly and completely. Currents less than the critical amount are insufficient to cause flux changes.

5-10. The computer hardware design will provide a mechanism to establish full read-write currents causing flux reversal, or one half value currents with no flux changes. The induced voltage on the secondary winding will be 32 millivolts for a flux reversal, but less than 10 millivolts if no flux reversal takes place.

5-11. TOROID

5-12. The actual toroidal core is a tiny ring 30 thousands of an inch in diameter. The primary windings are X, Y, and Inhibit wires which merely go through the hole. The sense winding is the secondary and is coupled by the flux linkages.

5-13. The array of cores is traversed by both "X" and "Y" wires. The M register bits are encoded to select one X wire, and one Y wire. Each of these wires provides one half of the total necessary current for flux reversal. Current flows through both wires in the correct direction so that during read cycle the flux establishes the "zero" state. During write cycle the currents establish the "one" state. Each toroid contains four wires. The sense wire is a secondary which provides interrogation during the read cycle to determine the previous state of the flux direction. The inhibit winding is the mechanism to prevent writing a one when the desired write state is a zero. This core system is commonly referred to as being a four wire - three dimensional system. The three dimension refers to the X-Y array on each bit plane, plus the "Z" dimension for 17 bits. Refer to Figure 5-5.

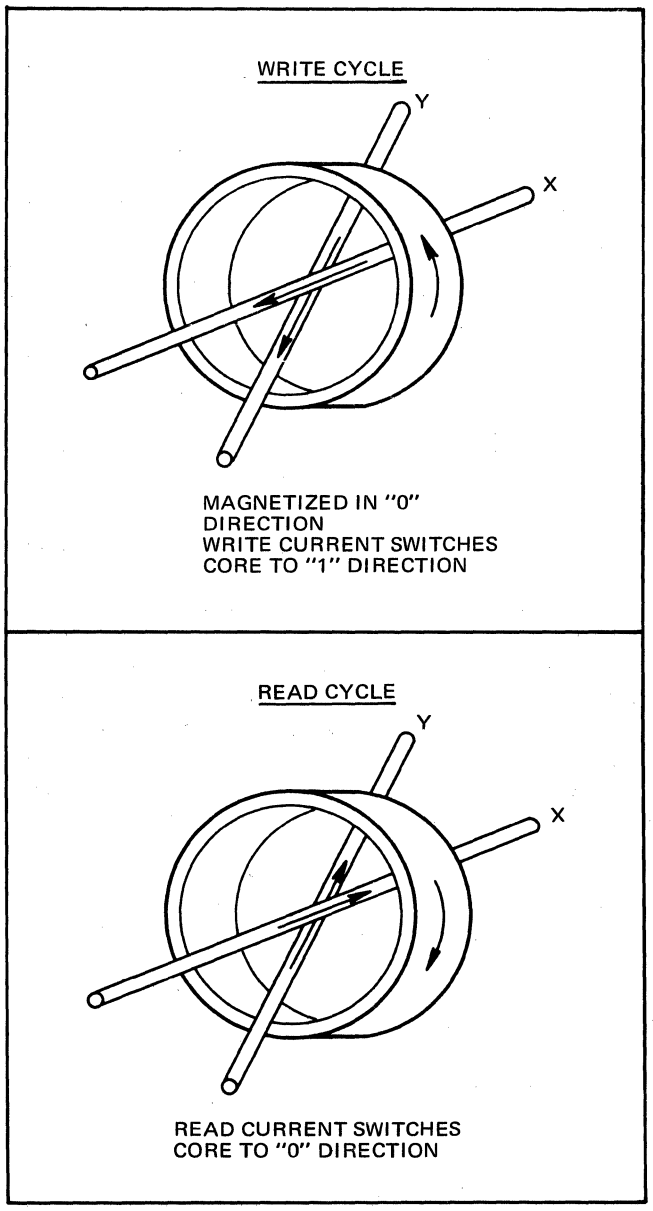


Figure 5-3. Read Write Currents vs. Core Status

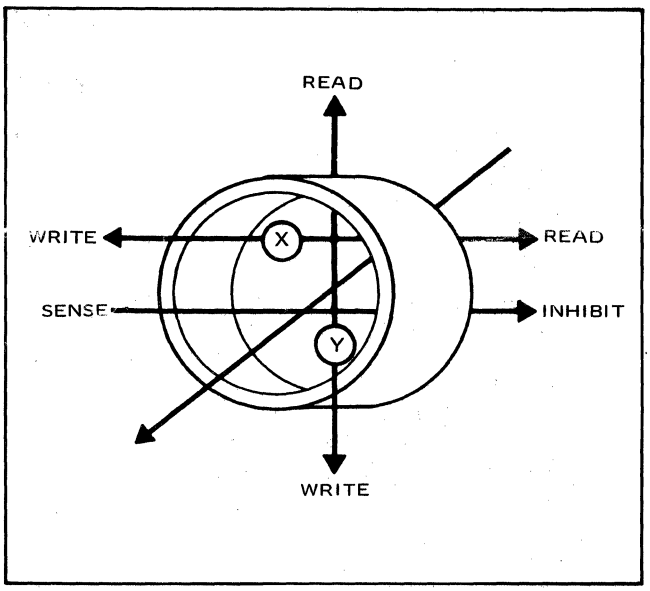


Figure 5-4. The 4-Wire System

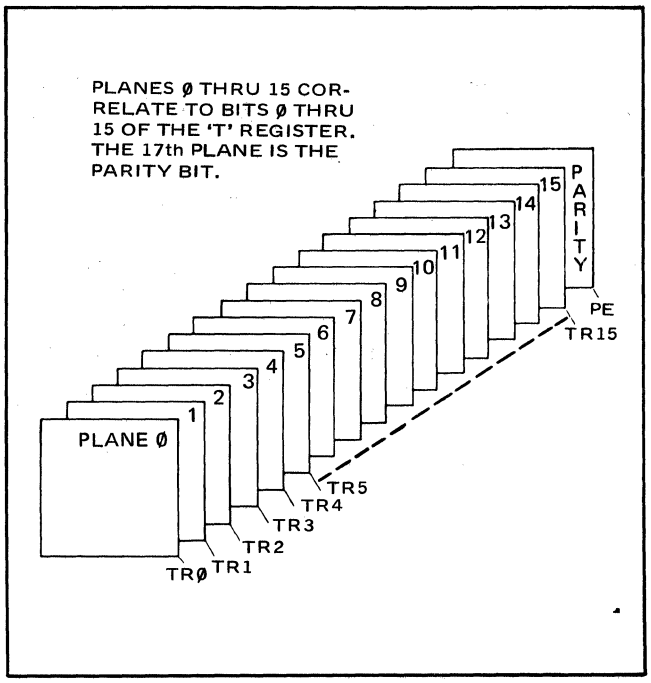


Figure 5-5. Each 4K Core Module has 17 Core Planes

5-14. CORE ARRAYS.

5-15. The toroids are arranged in a 64 by 64 array. (Refer to figure 5-6.) Each plane then has 4096 cores. Each plane is associated with one specific bit in the computer word. A 4K module has 17 such planes. One for each bit from 0 to 15, plus the Parity bit. Associated with each bit plane is a Sense Amp winding and an Inhibit winding.

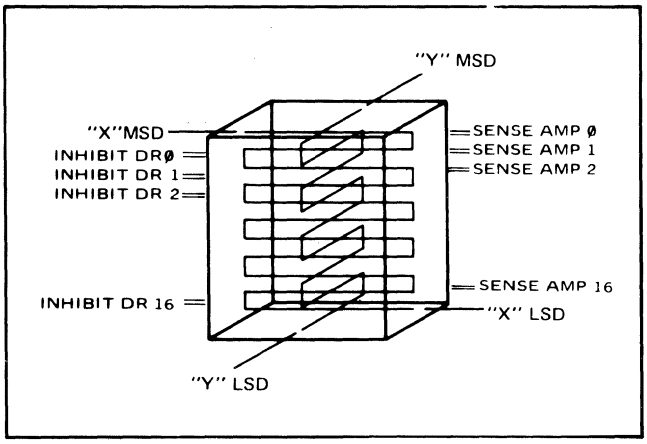


Figure 5-6. Core Module Addressing and Data

5-16. In the X direction the core has 64 wires which traverse all 17 planes. In the Y direction 64 wires also traverse the entire plane structure. The X address defines a plane through the entire core structure. The Y address defines a similar plane. The intersection of these two planes is a straight line defining 17 cores, one on each plane. (Refer to Figure 5-7.)

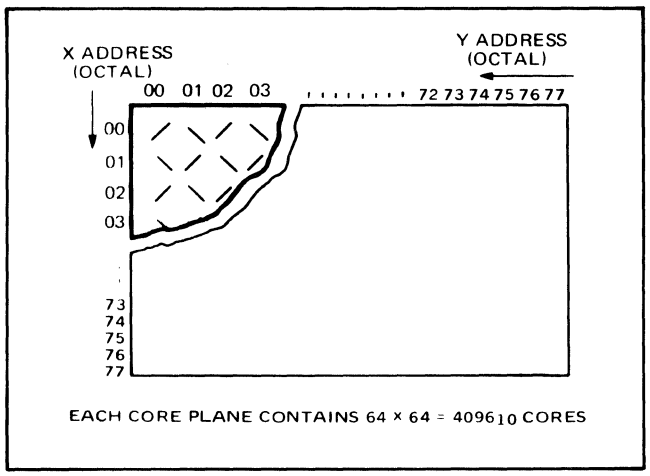


Figure 5-7. The Core Plane

5-17. It should be pointed out that this description is figurative and not literal. The actual core array in the 2114B has four bit planes on each frame.

5-18. ADDRESSING

5-19. The Memory Register contains the computer memory address. The information in the register is in binary form. The 64 address wires in each direction are designated in octal notation and range from 00 to 77. The computer word address ranges from 0000 to 7777 providing the 4096 decimal locations. This requires 12 binary bits. These 4096 addresses are arranged in four pages. Paging will be discussed later. The maximum number of 4K modules provided for in the 2114B is two. Another binary bit is required to indicate the lower or upper 4K module. The entire 2114B memory can be addressed with 13 binary bits (0 to 12).

5-20. The X and Y wires through core are arranged in groups of eight. At the common end they are connected together in address groups of 00 to 07, 10 to 17, 20 to 27, etc. The most significant octal digit corresponds to M reg. bits 3-5 for the X and 9-11 for the Y address.

5-21. The least significant end of these wires are connected together (using a diode matrix) in groups of eight. In the case of least significant octal digit corresponding to one, the addresses would be 01, 11, 21, 31, 41 and so on. The purpose of the driver switch circuit is to connect the common end (most significant digit) to the proper power supply voltage and to connect the diode end (lease significant digit) to its proper supply voltage. The current polarity through these addressing wires is bi-polar. For read and write operation current must be capable of flowing in either direction. This is provided for on the least significant end by the diode matrix. Each individual wire is connected to two diodes, one anode and one cathode. The drivers and switches drive these diodes in groups of eight. Each wire thus has two possible diodes, either the common anode end or common cathode end. This provides current flow in the proper address wire and isolation by the back biased diode to the other 7 lines.

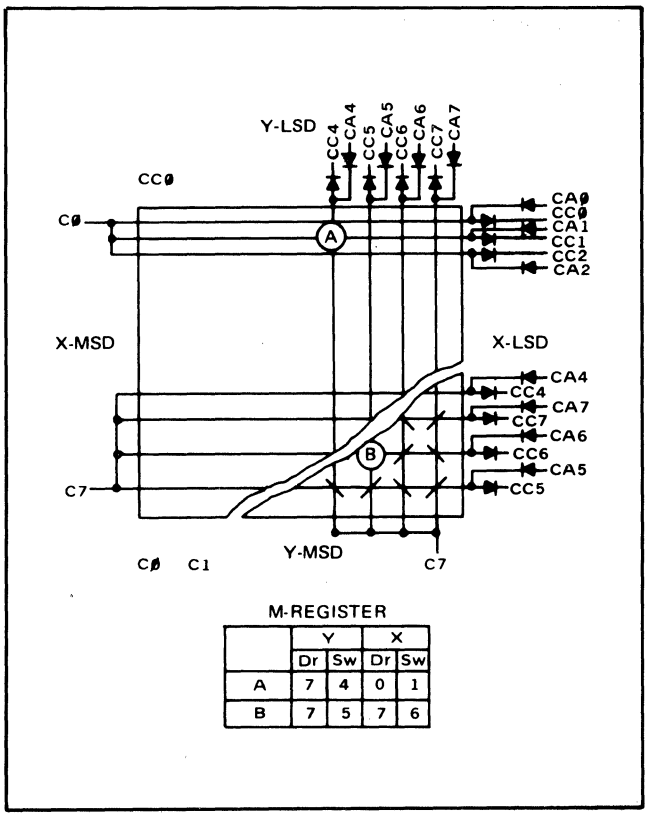


Figure 5-8. Memory Address Identification

5-22. DIODE MATRIX.

5-23. The core module has two diode matrix boards. The purpose of these diode matrix boards is to allow the driver switch assembly to select the least significant bit, using the common anode or the common cathode for correct polarity current. Those address wires which are not in use will be eliminated from the circuit consideration by virtue of their back biased diodes. The least significant octal inputs to the diode matrix board are the eight common cathode leads associated with bits 0 through 7, and the eight leads associated with the common anode bits 0 through 7. The most significant octal bits are provided by the 8 common leads 0X to 7X.

5-24. Figure 5-9 shows the diode matrix circuit. The eight common inputs associated with most significant bits are shown on the right margin. The common cathode and common anode diode inputs associated with bits X0 through X7 are located on the lower margin. Figure 5-10 shows an enlarged portion of the diode decoders associated with common bits 3 and 6 and common cathode and common anode bits 3 and 4. The address wire (X or Y) which traverses core is shown in the figurative sense between the diode junction and the common lead. Each of these wires traverses the 17 bit planes associated with each 4K of memory.

5-25. Figure 5-11 shows figuratively how the driver switch assembly makes the appropriate connections to allow current to flow through these address wires. For example; if the common bit 3 is switched to the plus supply that means the current must flow through the common cathode bit 4 to the minus supply (ground). This establishes current flow through the "X" wire octal 34. If this had

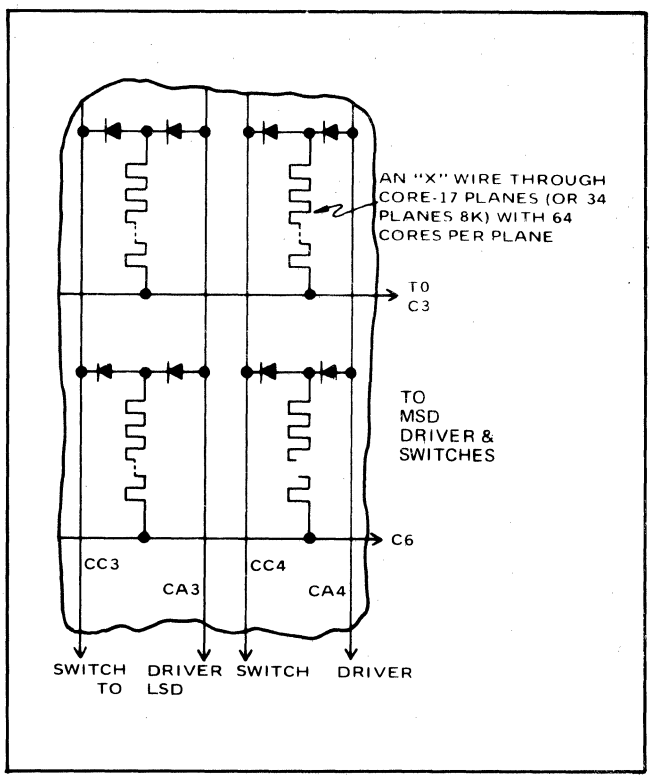


Figure 5-10. Octal Input Lines to Core

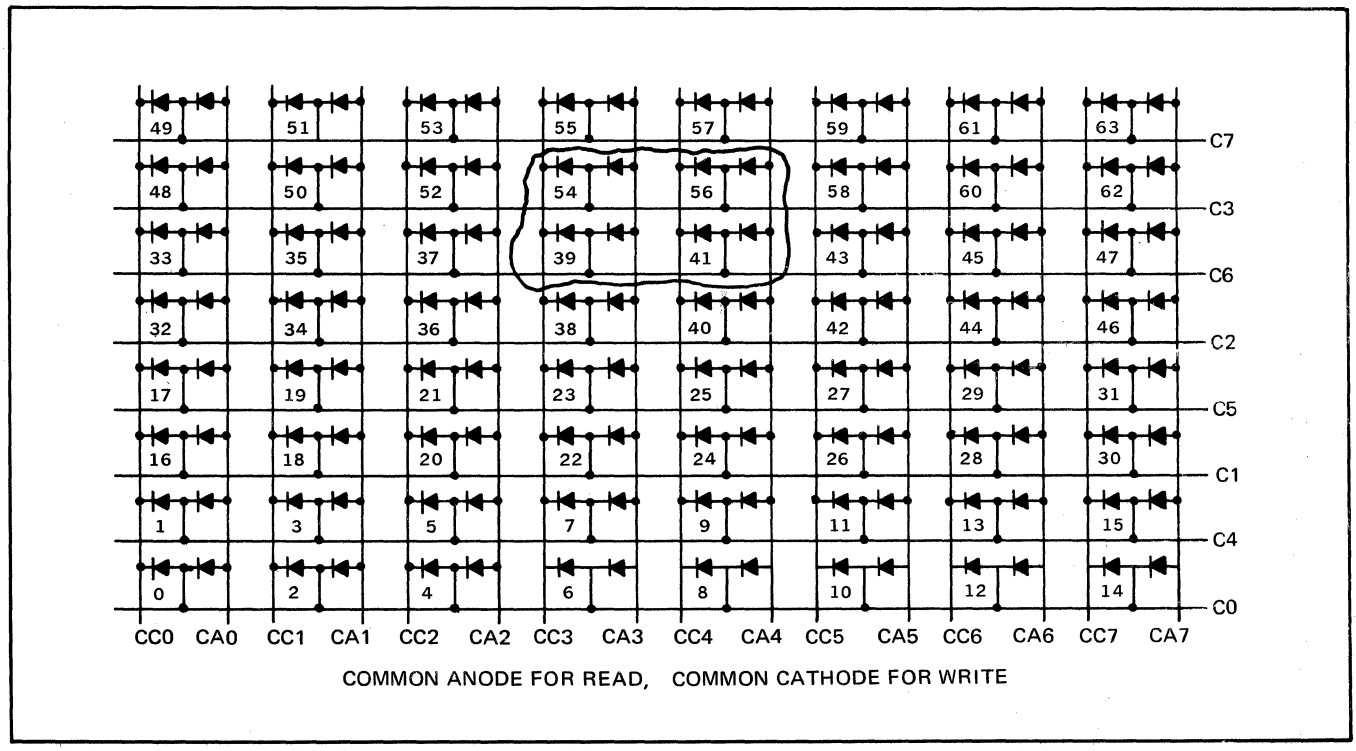


Figure 5-9. X-Y Diode Decoders

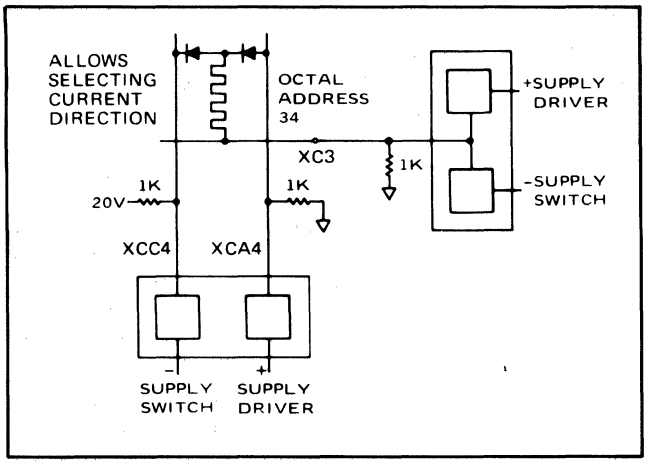


Figure 5-11. Driver Switch Voltage Buses

been necessary during the read portion of the cycle, then during the write portion of the cycle the currents are reversed and the common lead 3X would have to go to the minus supply and the common anode lead on bit X4 would be connected to the +20 volt bus.

5-26. DRIVER-SWITCH ASSEMBLY.

5-27. Figure 5-12 shows a selected pair of "X" driver-switch circuits. The common line corresponds to address X2. The function performed by this assembly will be to apply 20 volts through Q30 to the common lead 6 during write operations, and ground the common cathode end with Q16, 17. During write the common end is grounded through Q28, 29 and the common anode is connected to 20 volts through Q18. The operation above corresponds to addresses in the lower 4K module. The words read and

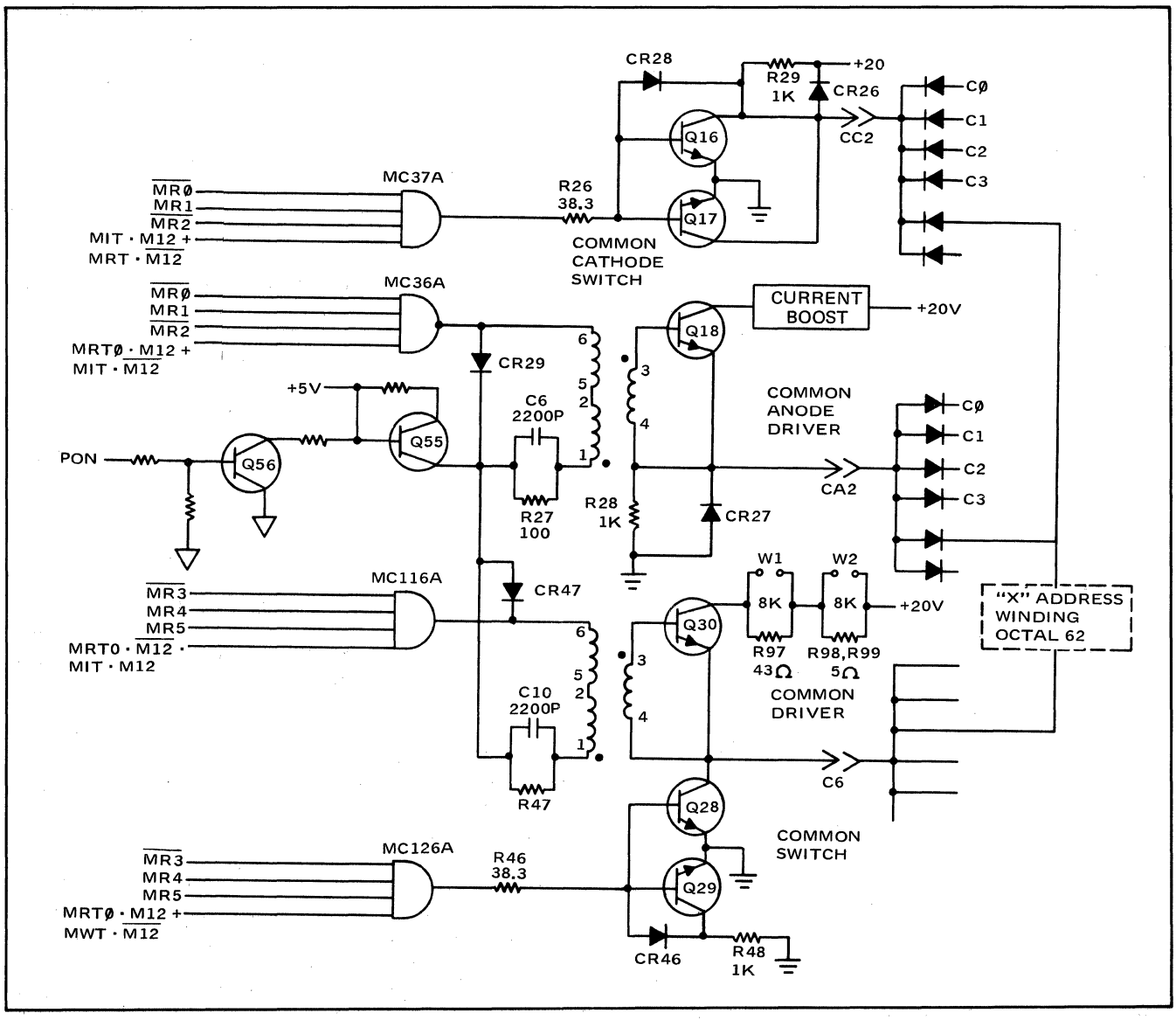


Figure 5-12. Driver/Switch

write should be interchanged for operation in the upper core module. Refer to section 3-10.

5-28. The ends which are switched to ground are directly coupled by transistor switches. The TTL logic level provides a convenient drive level to the transistor base. Transistors Q16 and Q17 on the common cathode, and Q28 and Q29 on the common line constitute the switch circuits.

5-29. The ends of the address line which must be connected to the +20 volt bus are done so by a single transistor - the DRIVER circuit. The DC design considerations for direct base drive would be difficult. A transformer provides the necessary DC isolation. The DC return for the transformer primary is provided to the +5 volt bus (when PON signal is present).

5-30. The NAND gate low output allows transformer primary current which forward biases the base to emitter junctions to transistors Q18 and Q30.

5-31. The RC network allows high turn on current to speed up the transformer output and overcome the transistor input capacity. The drive then reduces to an adequate hold on level.

5-32. DRIVER SWITCH TIMING.

5-33. A review of Figure 5-1 will indicate the timing relationship between MRT0 and MRT, and between MIT and MWT. The Driver circuits are always switched on during the earlier memory timing pulse. This ensures that the driver transistor (Q18 or Q30) is saturated before significant current must flow.

5-34. The power dissipation in the transistor switches is low during saturated conditions. The power dissipation is significant during turn on and turn off switching. Two transistors are provided to ensure an adequate safety margin (even in the case of poor saturation voltage characteristics or slow transistors).

5-35. The transistor switches are also used to cut off the current flow at the end of the conduction pulse. Diodes CR28 and CR46 are germanium diodes to allow rapid switch off. A saturated transistor contains excess stored charge in the active transition region. The turn off delay depends greatly on the transistor doping and temperature.

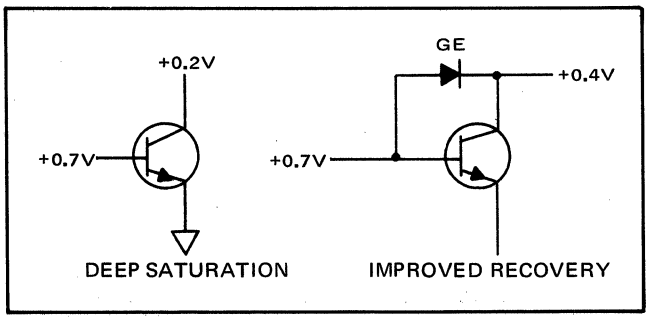


Figure 5-13. Transistor Saturation

5-36. The Germanium diodes CR28 and CR46 are used on the base to collector junctions to prevent such deep saturation. This controls the current waveshape and makes it less sensitive to individual component parameters.

5-37. COINCIDENCE — ANTI-COINCIDENCE.

5-38. The core stack is designed so that the Coincidence of the X current of one half value plus the Y current of one half value is sufficient to change the flux polarity in the core for both read and write operation. A mechanism providing anti-coincidence current is used which enables the same X and Y wires to address the entire 8K. This is accomplished by reversing the polarity of the X current between the 4K modules. In the lower 4K (when we are addressing the lower 4K) both currents add up and allow flux changes. In the upper 4K (that is from 4K to 8K) module both currents are present but because of the phasing of the X wire the currents cancel. The net current in the Non-addressed module is zero. It is possible thus, to use one set of driver switch boards to provide the X and Y currents for the entire core module. The current of the X wire is reversed in the upper module by physical construction. The current of the Y wire remains the same through the entire 8K. Thus both X and Y wires traverse the 17 bit planes associated with the lower 4K and continue then through the 17 bit planes associated with the upper 8K. It is necessary to provide separate Sense Amp assembly and Inhibit Driver assemblies since these are necessary bit by bit. Bit 12 in the M-Register determines which core module is addressed. $\overline{M12}$ indicates the lower 4K module and M12 indicates the upper 4K module.

5-39. ADDRESS EXAMPLE.

5-40. Consider an example in the lower 4K module with address XX62. Using Figure 5-12 we will trace through the sequence of events. Since we are assuming the lower module only those circuits in which $\overline{M12}$ occurs will be used. Those circuits using M12 will not be used.

5-41. The M-Register contents are available to the board. Binary bits 0, 2, 3, and 12 are low, bits 1, 4, and 5 are high (EXAMPLE: ○ ○○○ $\underline{○○○}$ $\underline{○○○}$ ●●○ ○●○). Bits 6-11 associated with the Y address can be any condition in the example. The M-Register complimentary signals are also generated on the driver switch assembly.

5-42. Bits 0-2 are associated with the common anode and common cathode memory lines. Only the driver and switch associated with octal address X2 can be energized. Similarly the bits 3-5 are encoded permitting operation of octal address 6X.

5-43. At T0 as MRT0 goes high NAND gate MC116A is enabled, saturating transistor Q30, pulling the common end to +20 volts. 120nsec later as MRT signal goes true MC37A is enabled turning on transistors Q16 and Q17. Read current now flows through X address wire 62. At T2 plus 120 nsec the MRT and MRT0 signals fall. The switches cease to conduct, current stops, and address line 62 returns to its normal quiescent state.

5-44. At T3 plus 120 nsec MIT goes high turning the driver transistor Q18 on. At T4 MWT turns on Q28 and Q29 and write current flows through address wire 62. At the end of T5 the MIT and MWT signals go low, the switches cease to conduct, current stops, and address line 62 returns to its quiescent state.

5-45. PROTECTION DIODES.

5-46. Certain protection devices are present to safeguard the components. In the common cathode switch circuit diode CR26 prevents the flux decay in the cores from pulling the common cathode line more positive than 20 volts thus protecting the collector junctions of transistors Q16 and Q17. The inductive kick as the X addressing current ceases would endanger the transistors without this protective diode. The common anode circuit transistor Q18 is protected by CR27. This prevents the inductive kick when the address current ceases from damaging transistor Q18 by pulling its emitter more negative than ground. In the transformer circuits diode CR29 in the bit 2 and diode CR47 in the common bit 6 are provided to protect the integrated circuit packs against the inductive kick due to the flux decay in the transformer. The design of the transformer circuit provides a current limiting resistor of 100 ohms and a speed-up capacitor of 2200pf which gives fairly high initial currents to overcome the stored charge in the transistor for quick turn on.

5-47. CURRENT BOOST.

5-48. Current boost circuits are provided which allow shaping of the current pulses. The circuit associated with common bit 6 has a current boost associated with it. Observe the 43 ohm resistor between the +20 volt bus and the transistor collector. This 43 ohm resistor provides an exact current in the address wire. It will be noted that a jumper exists to use the bypass capacitor (520pf) for the 8K core stack but is unused in the 4K core stack. This jumper is W1. A 5 ohm resistor is also present. Jumper W2 is used to short out this 5 ohm resistor for an 8K installation. In both cases the different characteristics of the 4K and 8K core module requires the changes. The 5 ohm resistor added in the 4K module allows the total resistive component of the address wires to remain the same in both cases. The resistance difference between 4K and 8K is approximately 5 ohms. The inductive and capacitive loading of the address wire is also different between 4 and 8K. The purpose of the parallel 520pf capacitor in the 8K unit is to allow current shaping which helps overcome the additional capacitance of the core stack.

5-49. The characteristics of the common lead 6 or common anode diode lead 2 in the core is different. The impedance as seen by the common lead 6 is essentially the inductance and capacitance associated with the 8 wires. On the common anode driver 2, however, the 8 wires are connected through the diodes, each in turn go through to the other end of the core and are electrically connected to 7 other wires which come back through core. The impedance seen through the common anode lead is essentially the capacitance of all 64 wires throughout core. Because of this greatly increased capacity it is necessary in utilizing the common anode driver to give an additional current boost. Figure 5-14 shows the current boost circuit

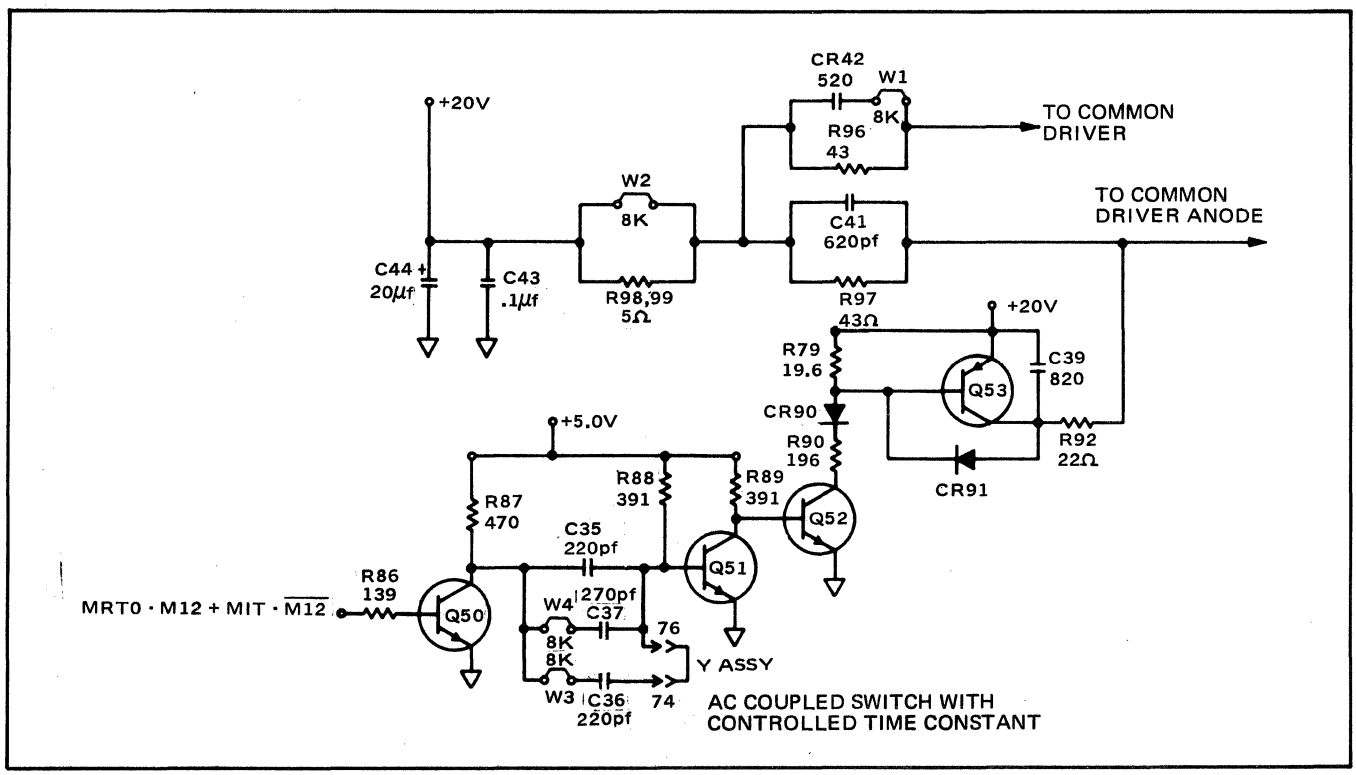


Figure 5-14. Memory Read Current Boost

utilized with the common anode driver. This circuit provides an additional 22 ohms to the +20 volt bus in parallel with 43 ohm or 48 ohm normally used.

5-50. As we follow the circuit operation we will see that the logical input is the MRT0 · M12 or MIT · $\overline{M12}$. When either of these signals is present transistor Q50 is saturated and the signal is AC coupled to transistor Q51 which is turned off allowing Q52 to conduct. Q52 turns on transistor Q53 which connects the 22 ohm resistor to the +20 volt bus. The amount of time that this boost circuit is required depends on the configuration whether 4K or 8K. The AC coupling between transistors Q50 and Q51 consist normally of the 330pf capacitor. For 8K operation an additional 270pf capacitor is added. On the Y address driver, using pins 74 and 76, a jumper on the back plane enables an additional 220pf capacitor to be added. So we have a boost circuit, the time characteristics of which depend on the jumper configuration. Diodes CR9 and CR91 provide for a timely termination of this current pulse. Transistor Q53, if allowed to enter a deep saturation, would be difficult to turn off. Diode CR91 between collector and base prevents deep saturation in transistor Q53. The utilization of this boost circuit with the external jumper allows both driver switch boards to be identical but still provide different characteristics for the X and Y drivers.

5-51. POWER ON.

5-52. The Driver-Switch circuits are not enabled until the Power On signal is present. This prevents operating memory until PON is present. The voltage return for the transformer primaries for both of the driver circuits is returned to 5 volts through transistor Q55. Transistor Q55 is turned on and saturated whenever the PON signal is present. When computer power first comes on the PON signal is not present and it prevents the memory circuits from operating. When the PON signal does come up then the voltage to these driver circuits is enabled allowing normal memory operation.

5-53. PAGE ADDRESSING.

5-54. The concept of page addressing and the utilization of T-Register bit 10 to designate the current page or the zero page sometimes needs clarification. The computer architecture utilizing 15 bits for memory addressing and the 16th bit for direct or indirect addressing, enables the addressing of 32K of memory. The memory capacity of the 2114B computer is 8K which means that bits 0 through 12 are sufficient for addressing all of core. This addressing information is contained in the M-Register.

5-55. In Memory Reference Instructions the bits which have been dedicated to the address are bits 0 through 9. Bit 10 enables us to remain in the current page or to force ourselves to the zero page. The 2114B computer has 8 pages of memory, the lower 4K module has pages 0, 1, 2, and 3, the upper 4K module has pages 4, 5, 6, and 7. The bits associated with these pages are bits 9, 10, and 11 plus bit 12 which designates the lower 4K or the upper 4K. In a Memory Reference type instruction the memory address contained in T-Register bits 0 through 9 contain the memory information within the current page. Bits 10, 11, and 12 are retained in the M-Register and do not normally change with each individual instruction. It is possible to clear out bits 10, 11, and 12 in the M-Register. This is accomplished by forcing bit 10 of the instruction to 0 which clears out M-Register bits 10, 11, and 12. The use of an indirect address utilizing bits 0 through 14 for the address and bit 15 for the direct-indirect allows setting all bits of the M-Register to a new value. Bit 10 thus serves the function of enabling a direct clear of the memory register bits 10, 11, and 12 forcing the address into the base page. Figure 5-15 indicates the bit status and address limits of the memory pages.

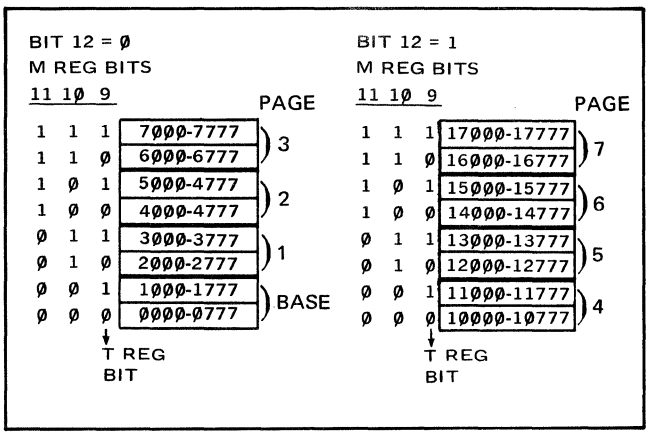


Figure 5-15. 8K Core Page Addressing

5-56. MEMORY BIT INFORMATION.

5-57. Information to this point has been dealing primarily with memory addressing. The utilization of X currents and Y currents enable addressing those 17 bits (Toroidal cores) associated with that address. The rest of the memory function will deal with the determination of the status of those 17 bits. Figure 5-16 shows a simplified

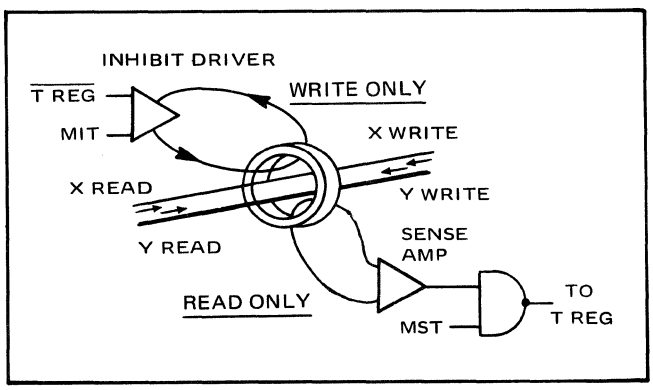


Figure 5-16. Four Wires

example in which the X and Y currents enable reading or writing. These currents traverse the opening in the toroidal core. A secondary winding (the Sense Winding) also traverses the core and the changing flux orientation within the core enables the sense amp to determine the previous flux state. The information from the sense amp is then strobed with the Memory Strobe Timing (MST) pulse. It allows the sense amp information to set the T-Register.

5-58. During the Write part of the cycle the Inhibit Driver is controlled by the information contained in the T-Register. It allows inhibiting the address current so that the core can remain in zero state. If the inhibit current is not enabled the core is forced to the "one" condition by the X and Y write currents.

5-59. Figure 5-17 shows schematically the relationships of the Sense Amp and Inhibit Driver with the core stack and the T-Register Flip-Flop. This is drawn to represent data bit 9. The Sense Amp winding includes all 4096 cores on this bit 9 core plane. This winding provides an input to the sense amplifier. The output of the Sense Amplifier will be a one or a zero depending on what the previous state of the core was. The X and Y current drives the core toward the zero state and if the core changes state (which means that it has been a "one") then the sense amplifier will have an output. This output from the Sense Amp is enabled by the Memory Strobe Timing pulse. This output drives the direct clear side of the T-Register bit 9 and forces the T-Register to the one state. During the Write cycle the T-Register Q output is ANDed with the Inhibit Timing Pulse (MIT). If both signals are present the Inhibit winding allows current to flow which prevents the core from writing the "one" and allows the state to remain "zero".

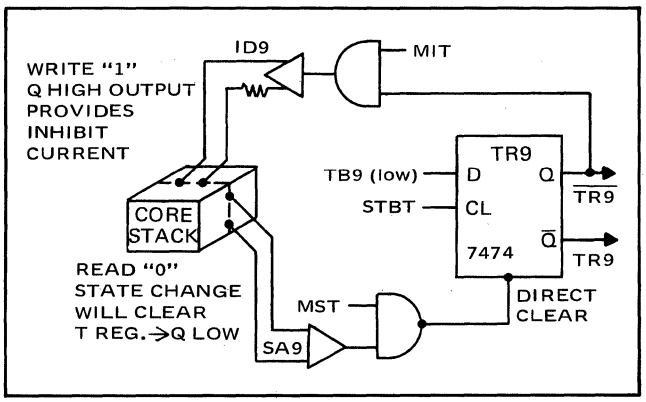


Figure 5-17. Data Sense And Inhibit

5-60. It should be noted that the polarities of the signals are not obvious. The T-Register D input is the TB9 (negative true signal), so the T-Register true output must come from the Q side of the flip flop. The sense amp goes to the direct clear (negative true). The presence of a flux change will give a sense amp output which is enabled by the Memory Strobe Timing. This negative true signal clears the T-Register flip flop which forces the Q high indicating a one in the T-Register. The Memory Inhibit Timing signal along with the Q output from the T-Register flip flop are combined to control the Inhibit Driver output. If this is high it indicates that the T-Register contains a zero and we must inhibit the X and Y current from writing a one. The Inhibit Driver is enabled allowing current to flow through the Inhibit winding. This Inhibit winding traverses all 4096 cores in the bit 9 plane.

5-61. SENSE AMPLIFIER.

5-62. The winding associated with the Sense Amplifier includes all 4096 cores on its respective bit plane. The output voltages indicated on Figure 5-2 represent the switching voltages for one core. As the Sense Amplifier winding passes through many cores the voltages are additive. To prevent the large number of cores which have one half current flowing from adding zero signal voltages giving a large apparent signal the sense winding must be wound in a special manner. The X addressing current flows through 64 cores of which one is the desired core being addressed. The Y current also flows through 64 cores of which only one is desired. The sense winding must enter these 127 cores one half in the positive sense, and one half in the negative sense. In this way the noise contribution (zero voltages) cancels. The anticipated signal thus is discerned from the noise by amplitude and by timing. The Sense Amplifier is strobed during the first 120 nsec of time T2. It also prescribes the requirement that the sense amplifier be able to handle both polarity signals.

5-63. Figure 5-18 shows a typical Sense Amplifier stage. The components are shown for bit 0. This Sense Amplifier

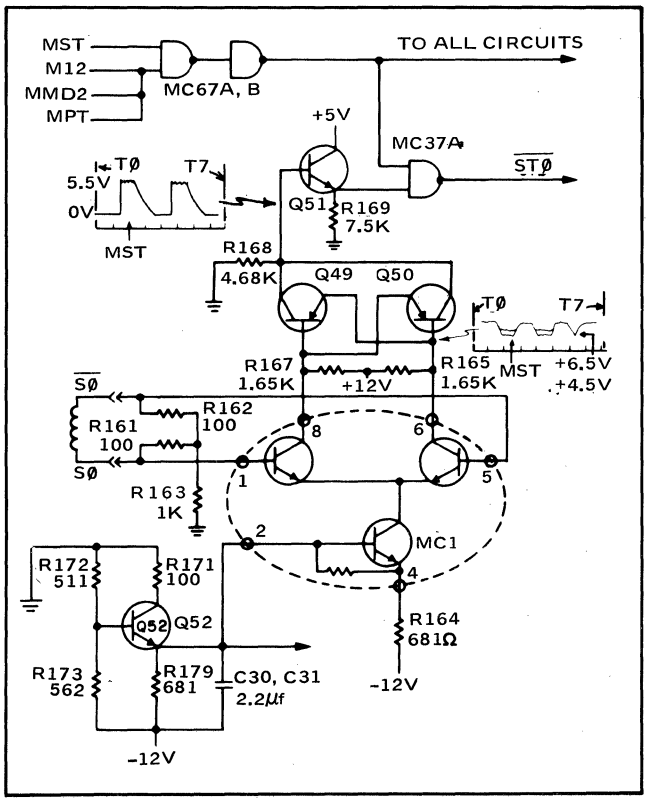


Figure 5-18. Sense Amplifier

consists of a differential transistor pair, an accurate current source, a transistor amplifier and output gate. The integrated circuit pack contains the differential pair and a transistor to serve as an accurate current source. The base of this current source transistor goes to an emitter follower, transistor Q52. This transistor provides a stable voltage supply, and feeds all sense amplifier circuits. The current source transistor provides a stable current to the differential pair. This total current remains the same, so depending on sense winding inputs as one transistor current increases the other must decrease.

5-64. The voltage on the sense winding is applied to the bases of the differential pair. The current flow is approximately 7 milliamps total through the two differential transistors. This establishes steady state collector voltages of approximately +6.5 volts. As the low level sense winding voltage is applied to the bases one transistor increases current flow and the other transistor decreases current flow. The voltage changes on the collector resistors thus developing a differential voltage. This voltage across the collectors of the differential pair is applied to transistors Q49 and Q50. One of these transistors will be forward biased and will conduct. The collector voltage of the conducting transistor goes positive, pulling the emitter of the emitter follower Q51 positive, providing a high input to NAND gate MC37A. The Memory Strobe Timing (MST) signal, and the memory module information MR12 being present also enables NAND gate MC37A. This provides a negative true signal $\overline{\text{ST0}}$, which clears the T-Register.

5-65. The operation of this circuit is symmetrical so that either polarity signal on the sense winding operates the circuit in an identical fashion. In previous Sense Amplifier designs for the 2115A and 2116A computers a balancing potentiometer was necessary in the collector return. In this 2114B design a special integrated circuit pack is being used with tight specifications on the transistor balance eliminating the balancing potentiometer.

5-66. The voltages present on the Sense Amp winding are difficult to interpret. The voltages on the differential pair collectors and at the emitter follower output are better places to observe for troubleshooting purposes. The collector voltages on the differential pair are normally approximately +6.5 volts. Under signal conditions wave shapes will be visible with outputs at +4.5 volts and +5.8 volts. The wave shape on emitter follower Q51 will indicate large voltages at time T1 and T2, and T5 and T6. Only the signal present at time T2 is used by the MST signal.

5-67. INHIBIT DRIVER.

5-68. The Inhibit Winding parallels the X current address winding on an entire bit plane. On the succeeding bit plane it follows the Y address winding. It thus alternates on alternating bit planes. The purpose of the inhibit driver circuit is to provide one half current through the inhibit winding which effectively cancels one half of the addressing current through the addressed core. This prevents the core flux to be written to the "one" state. One end of the inhibit winding is connected to the 20 volt bus through a 43 ohm resistor. A 1000pf capacitor provides current shaping to overcome the distributed capacitance of the core stack. The inhibit driver transistors, when conducting, ground the other end of the inhibit winding thus allowing current to flow.

5-69. The T-Register output, Q output, is wired directly to the Inhibit driver circuit. The presence of the T-Register output along with the MIT signal permits operation of the Inhibit driver circuit. An individual Inhibit driver assembly is provided for the lower 4K, and for the upper 4K if installed. The MIT, MIL, and $\overline{\text{MR12}}$ signal is delayed between packs MC76B and MC76A NAND gates. This RC filter delays the start of the driver switch current. The transistor switches Q27 and Q28 have a germanium diode CR27 to prevent deep saturation. This allows expeditious termination of the Inhibit drive current pulse. Diode CR28 protects the transistor switches from the inductive spike when the inhibit driver current is terminated.

5-70. It will be noted that both the Inhibit Driver and Sense Amplifier assemblies have 17 circuits. Both provide the necessary bit for parity error operation.

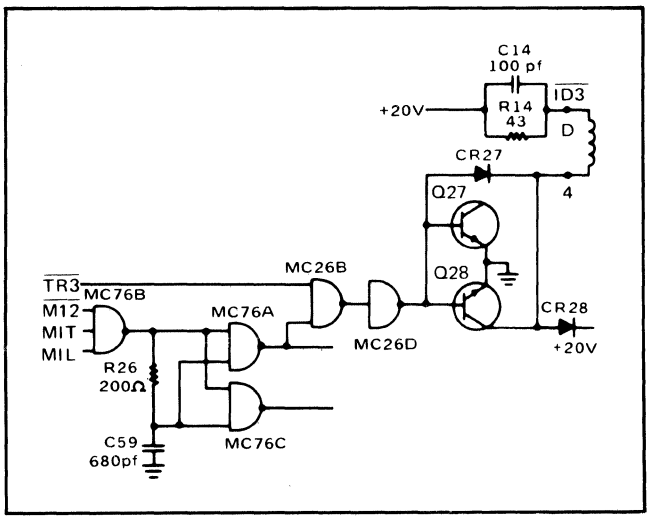


Figure 5-19. Inhibit Driver

5-71. MEMORY CORE MODULE CHARACTERISTICS.

5-72. The 1/2 read and write currents are 320 milliamperes. The Rise and Fall times are 300 nsec, read and write pulse duration 400 nsec, inhibit pulse 500 nsec. The "one" voltage shall be at least 32 mv during the time period 400 to 500 nsec. The "zero" shall not exceed 10MV during the same period. The X and Y resistance is 5 and 8 ohms for 4K and 8K modules. The sense windings are about 16 ohms, the inhibit windings are 12 ohms.

5-73. The X and Y common address lines tie together sets of 8 adjacent lines. These lines alternate, 4 each on

opposite sides. The inhibit windings alternately parallel the X and Y address lines on sequential planes through the stack.

5-74. 8K CORE INSTALLATION.

5-75. The installation of 8K memory in a 2114B Computer requires changing the memory core module, and the addition of a Sense Amplifier assembly, and an Inhibit Driver assembly. The two Driver Switch assemblies remain sufficient, however, jumper changes must be made. On each Driver Switch assembly 4 jumpers must be added for 8K installation. On the System Timing Generator jumper W2 must be removed. The purpose of W2 is to delay the MST signal in an 8K installation. When jumper W2 is removed in a 4K installation it allows the MST signal to come earlier by 30 or 40 nsec. In the 8K installation jumper W2 is installed delaying the MST signal to take care of the increased distributed capacitance between the 4 and 8K memory module.

5-76. PARITY ERROR.

5-77. The Parity Error option for the 2114 Computer is Accessory Model 12598A. This option provides parity interrupt to location 5, or computer halt when parity errors are encountered. The Parity Error assembly consists of control and flag circuitry for generating the interrupt, the bit comparison tree for determining odd or even number of bits in the computer word, and memory address flip flops.

5-78. The output of the bit comparison tree is compared with the parity bit. If this combination is odd no parity error exists. If this combination is even, indicating an apparent parity error, the interrupt circuitry is enabled. The memory address flip flops are set to the memory address at which the parity error occurred. Provisions on the 48 pin connector allows selection of parity error halt or parity error interrupt to a service subroutine.

5-79. BIT COMPARISON TREE.

5-80. The bit comparison tree is made up of TTL, AND-OR-INV logic units. Each of these logic units compares 2 bits and determines whether the combination is odd or even. Thus the 16 bits in the computer word are compared two by two. The eight outputs of the first rank are compared two by two, the four outputs from the second rank are compared two by two. The two outputs of the third rank are compared. The single odd or even output representing the 16 bits is then compared with the parity bit flip flop. This final combination must be odd to prevent a parity error indication. The bit comparison must be odd to prevent a parity error indication. The bit comparison tree always compares the contents of the T-Register. This information is strobed only during time T3 when the MTE signal is present.

5-81. The output of the bit comparison tree is the $\overline{\text{TR16}}$ bit, which drives the inhibit driver. A negative signal on $\overline{\text{TR16}}$ will not enable the inhibit driver, thus writing a "one" in core. The parity bit flip flop is cleared during each T1M when memory is enabled. It is set by the Sense Amplifier Output $\overline{\text{ST16}}$.

5-82. The TTL logic packs in the bit comparison tree are high speed units. The typical delays in the AND-OR-INV is 7 nsec. The delay in the high speed NAND gates is 6 nsec. Typical delays through the entire bit comparison tree is in the order 70 nsec.

5-83. The use of the parity error assembly makes a powerful troubleshooting aid. It is necessary when installing the Parity Error assembly to reload all programs in order to generate the parity bit. Information on the use of the Parity Error option is contained in the Operating and Service Manual for the Accessory 12598A, and in the Diagnostic Supplement.

5-84. MEMORY ERROR ADDRESS REGISTER.

5-85. The Parity Error assembly contains 13 flip flops which are used to store the error producing memory location. The flip flops for bits 0 to 11 are D type latch flip flops. When the clock signal is positive the contents of the M-Register is allowed to set the flip flop. When the latch signal is negative the register contents will not change. Bit 12 ($\overline{\text{M12}}$) uses a D type edge triggering flip flop. Its operation is equivalent. The operation of the error address flip flops is inhibited by AAF and BAF signals (since the A and B-Registers do not contain parity bits), and the other conditions (LOAD MEMORY, ISG, STR and JSB) which provide MWL positive except PH3 · ISZ. The operation under ISZ-PH3 operation is checked even though MWL is positive. When the comparison of the bit comparison tree and the Parity Bit Flip Flop is high (indicating no error) the latch inputs are negative preventing the contents from changing. When the comparison is low the latch inputs are held positive allowing the current contents of the M busses to set the address register. The contents of the address register are strobed to the IOB buses with an Input select code 05 instruction. Bit 15 is high during the same operation. (Bit 15 is used in the 2115A to differentiate between Parity Error and Memory Protect. This printed circuit assembly is used in both options with minor loading changes.)

5-86. FLAG AND INTERRUPT CIRCUITRY.

5-87. The flag and interrupt circuitry on the Parity Error assembly are similar in operation to other flag and interrupt design. The computer Power On and PRESET control provide POPIO signal which sets up proper operating conditions for the Parity Error operation. The Parity Error operation can be inhibited with a CLF signal to select code 5. The functions of the Control Flip Flop, Flag Flip Flop, Flag Buffer Flip Flop, and IRQ Flip Flop is described in the I/O system operation volume 3. The interrupt outputs from this assembly are the IRQ5 address line and $\overline{\text{PINT}}$ signals or $\overline{\text{PEH}}$ depending on the hood orientation.

5-88. TROUBLESHOOTING THE MEMORY SECTION.

5-89. Detecting simple problems within the Memory Section (the Dr/Sw Cards, the Sense Amp Cards, the Inhibit Drivers, the Diode Matrices or the Core Stack) can easily be accomplished through the execution of the Pretest Checkout Procedure explained in Chapter 7 on Troubleshooting the HP 2114B. Problems such as dropping bits of information or gaining bits of information when storing information into memory are immediately detected from the Pretest Checkout Procedure. Less obvious problems within the Memory Section of the computer may not be easily recognized by the inexperienced technician from the Pretest Checkout Procedure but the problem will be displayed upon execution of the test.

5-90. Being able to detect these errors from diagnostic tests is one of the objectives of this training manual, as well as, providing a few hints on troubleshooting each section of the computer. Chapter 7 which covers troubleshooting procedures of the HP 2114B tells the technician exactly what to look for when executing a test. Any other indication other than the correct result implies that an error is present and that the technician should repair the problem before proceeding. This section of the training manual will deal with actual troubleshooting hints to the repair of detected problems. Refer to Chapter 7 for correct indications when checking out the memory section by executing test procedures.

5-91. In troubleshooting the memory section of the HP 2114B, the technician must first reduce his problem to a specific board within the memory section. To reduce a problem within memory to a certain board, the technician should analyze his problem, reduce his problem to a certain part of the Memory Section and (if 8K is present) use the board switching technique to reduce the problem to one specific board. This technique is described in Chapter 7 in the Pretest Checkout Procedure when testing the Memory Section of the computer.

5-92. Once the technician has reduced his problem to one specific board in memory he has to reduce his problem even further to provide a good starting point for troubleshooting. Obvious problems, as examples; picking up bit 6 in all information coming out of the lower 4K of memory should tell the technician to begin at the circuit corresponding to bit 6 on the board that is giving problems or every address corresponding to $XXXXX6_8$ produces a problem in memory should indicate to the technician to begin his troubleshooting with the circuit corresponding to address $XXXXX6_8$.

5-93. GENERAL TROUBLESHOOTING TECHNIQUES.

5-94. The best way to begin troubleshooting any one of the memory boards is to compare waveshapes of the assumed bad circuit with one of the other good circuits on the same board. Each board has its corresponding "good" waveshapes relating to each bit of information or to each "good" address. The Sense Amplifier(s) and Inhibit Driver(s) correspond to information transfer in and out of memory. The Driver/Switch Cards are associated with each address in memory. The waveshapes for each board are taken directly from the output transistor for each specific circuit.

5-95. To generate the waveshapes for each specific board the computer must be in the RUN mode. It is left to the technician to generate his own looping program, or single instruction loop, or single phase loop to allow memory timing to operate. Memory Timing Signals (MRT0, MRT, etc.) are the signals that allow the memory section to operate. When the memory timing is turned off all of the memory section will be turned off.

5-96. The technician should analyze his problem before he does any troubleshooting. If his problem is dropping bit 6 from all information coming out of the lower 4K of memory, he obviously would not want to use an instruction that did not make use of bit 6 in memory. If his problem is common to a specific address configuration, the technician should ensure that he uses that address configuration in troubleshooting. This simply ensures operation of the faulty circuit to allow easy operation in troubleshooting the circuit.

5-97. TROUBLESHOOTING HINTS.

5-98. There are a few hints on troubleshooting the memory section that can guide the technician to a reasonable starting point, if not a quick repair. Within the Pretest Checkout Procedure there is a specific test that stores all one's into memory and allows the technician to read them back out of memory. This checks for correct operation of all of memory and allows the technician to determine whether any bits of information is being lost due to faulty circuits within memory. The second part of this specific test of memory stores all zeros into memory allowing the technician to determine whether any bits of information is being picked up due to faulty circuitry within memory. These two specific tests are key diagnostic tests of memory and should become the technicians handiest procedures for checking memory.

5-99. The troubleshooting hints for the technician are based upon the tests described above and in the Pretest Checkout Procedure. When problems occur in memory and 8K is present, determine whether the problem is common to both upper and lower 4K modules of core. If so, the problem will usually be a result of a faulty Dr/Sw Card. If the problem is unique to one specific 4K module, the fault will usually lie within the Sense Amplifier or Inhibit Driver associated with that 4K module.

5-100. There is no real way for the technician to tell if his problem is on the Sense Amplifier Card or Inhibit Driver Card. If 8K of core is present, the technician can switch identical cards and determine if the problem follows. But which set of boards should he exchange first or what if only 4K of core is present? From here it is left up to the

technician to decide but a common procedure can be followed. If the computer is picking up a bit of information begin with the Inhibit Driver, if the computer is dropping a bit of information begin with the Sense Amplifier.

5-101. This procedure is followed simply because the Inhibit Driver, when turned on, should prevent a "1" from being written into core. If the Driver does not turn on the computer will pick a bit of information up. The Sense Amplifier senses all 1's out of memory, if it does not turn on the computer will drop that bit of information.

5-102. These hints should give the technician a logical starting point. He can now determine whether his problem is on the specific board he chose or, if 8K of core is present, switch the two identical cards and determine if the problem followed the switch.

5-103. Once the problem has been reduced to one specific board the technician has usually accomplished his job. He can now exchange the board with a good one and send the bad board back to the factory on the exchange program. But what if he had no "good" board to exchange and he had to repair the board immediately? Where does the technician begin?

5-104. TROUBLESHOOTING THE DR/SW CARDS.

5-105. Referring back to earlier comments in this troubleshooting procedure for the memory section. Compare waveshapes from the faulty circuit with waveshapes from corresponding good circuits. Memory problems associated with the Dr/Sw Cards are very hard to reduce to one specific circuit. If the Parity Error Option is not present, which would readily detect any memory problems, the technician would have to reduce his problem manually. The Parity Error Option with respect to the Dr/Sw Card would reduce any hardware problems specifically to one circuit on the board.

5-106. To determine what circuit is causing the problem on the Dr/Sw Card, with Parity Error or without, run the little diagnostic test that stores all 1's into memory. Parity Error will halt at the error address plus one. Without Parity Error the computer will continue to run storing all 1's into memory. Using an oscilloscope, check the waveshapes coming off of the common collector of the driver transistors in each circuit (all the collectors of each driver transistor in the lower bank of circuits on the schematic are common and should have a common waveshape. The same reasoning occurs for the upper bank of circuits on the Schematic.). Since all memory addresses will be turned on during this test a constant waveshape as shown in Figure 5-20 should be displayed. When the computer is not running the collector to each driver transistor is at approximately +20v. During the RUN mode when the transistor turns on the collector voltage reduces to approximately +4v. If the Loader Enable Switch is in the NORM position (protect position) a faint line across the top of the waveshape at the +20v level can be seen. This is caused by the instantaneous turn off of the drivers when the computer loops through the upper 64_{10} protected locations of memory and memory turns off. The Loader Enable Switch should be put in the ON position to eliminate this line.

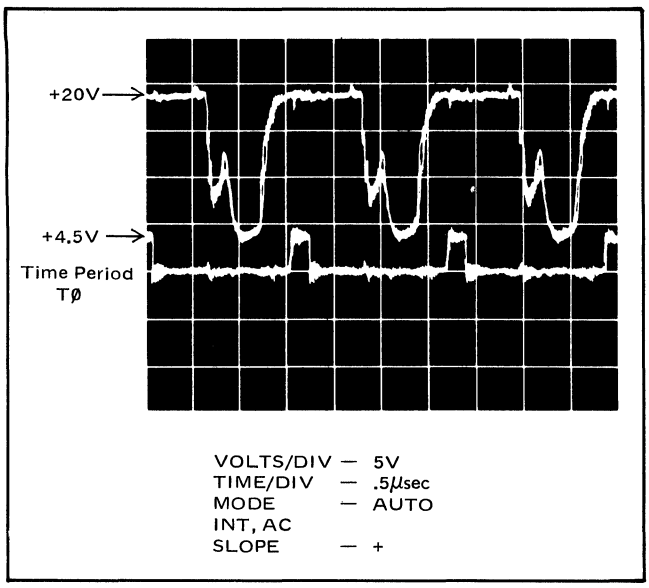


Figure 5-20. Driver/Switch Waveshape

5-107. The displayed waveshape in Figure 5-20 is shown with respect to time period T0 and ground. The oscilloscope is using time period T0 as a synchronizing signal.

5-108. A faulty Driver/Switch Circuit would cause the waveshape in Figure 5-20 for the Dr/Sw circuit to differ from the normal waveshape everytime that circuit was turned on. The machine cycle is so fast that the good Dr/Sw circuits and the faulty Dr/Sw circuit will look like they are turning on constantly. The faulty circuits waveshape will look as though it is overlapping the good waveshape, thus can be readily compared and detected easily.

5-109. A faulty waveshape as compared to the good waveshape of the Dr/Sw circuit can have a decrease in amplitude, an increase in amplitude or it can be completely distorted. In other words, any faulty waveshape, no matter how small can possibly cause problems to the computer and should be repaired.

5-110. Once a faulty Dr/Sw circuit has been detected, it is left to the technician to determine which circuit it is. The Parity Error Option would indicate what address was giving the problem by halting at the location following the error. The technician should write the error address down and allow the computer to RUN again until the next Parity halt. Keep writing the error address down and continue the process until a common section of all the error address have been detected. As an example:

Error halts occurred at

1. 000172_8
2. 001155_8
3. 010144_8
4. 012163_8

5-111. A common Y-Sw (Least Significant Digit with respect to the Y DR/SW Card) in the 100_8's seems to be giving the problem. The technician can now switch DR/SW Cards and determine if the problem follows the change from the XXX100_8's addresses to the XXXXX1_8's addresses by following the same procedure as above. When the technician is confident he has reduced his problem to one specific circuit, he can loop an instruction using the INSTRUCTION LOOP Switch on the back of the Front Panel in one of the error addresses to allow the faulty DR/SW circuit to turn on. This will allow easy troubleshooting of the faulty circuit while it is operating.

5-112. If Parity Error is not present, the technician has to find the faulty DR/SW circuit by using the diagnostic test switches on the back of the Front Panel. Store all 1's into memory following the procedure given in the Pretest Checkout Procedure. Continue looping and looking at the waveshapes of the DR/SW Card. Now, take the INSTRUCTION LOOP Switch and switch it to the LOOP position while watching the waveshapes. If the bad waveshape remains displayed the technician has found a bad address. Continue looping and begin troubleshooting with respect to that DR/SW address.

5-113. If the bad waveshape does not remain continue switching the INSTRUCTION LOOP Switch until one does remain. The computer will remain running with the PHASE LOOP Switch in the LOOP position. The INSTRUCTION LOOP switch simply disallows any incrementation of the P and M-Register which makes the computer loop on one specific address. This troubleshooting technique is a hit and miss type of technique but is effective for the technician.

5-114. The Dr/Sw Cards are the two hardest boards to troubleshoot in the memory section. The Sense Amplifier Cards (A6 & A7) and the Inhibit Driver Cards (A3 & A4) are easier to troubleshoot simply because they have seventeen exact circuits on each board with one circuit corresponding to one bit of information going in and out of memory. Once the technician has reduced his problem to one specific board, he has to reduce his problem even further on the board to one particular circuit. Once this is achieved, generate another looping diagnostic that forces the suspected bad circuit to operate.

5-115. TROUBLESHOOTING THE INHIBIT DRIVER CARDS

5-116. A handy loop diagnostic to check the Inhibit Drivers is to store all zeros into memory following the procedure in the Pretest Checkout then PRESS RUN. This essentially runs the NOP test in the computer where the computer reads all zeros out of memory and executes a NOP (000000_8) instruction. This should ensure that all inhibit drivers turn on during each machine cycle and that the computer will constantly run by looping through NOP instructions. While the computer is running the technician can go to the specific inhibit driver circuit and compare the waveshape of the suspected bad circuit with other waveshapes from good inhibit driver circuits on the same board. An example of a good waveshape of an Inhibit Driver is shown in Figure 5-21. The waveshape of the inhibit driver is taken from the collector of the output transistors in each circuit. An Inhibit Driver that is turned off does not turn the output transistors on; therefore, the collector is setting at +20V. When an Inhibit Driver is turned on the output signal goes to ground as shown in Figure 5-21.

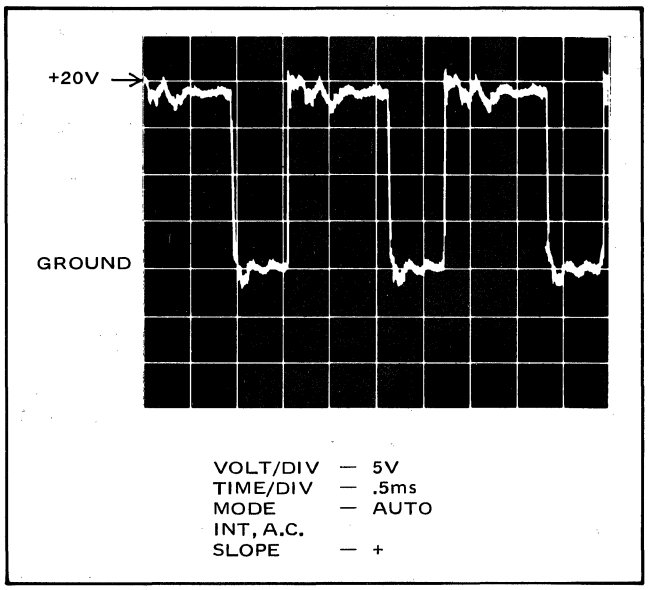


Figure 5-21. Inhibit Driver Waveshape

5-117. TROUBLESHOOTING THE SENSE AMP CARDS

5-118. When troubleshooting the Sense Amplifiers use basically the same technique as troubleshooting the Inhibit Driver. But, instead of storing all 0's store all 1's and read them back by using a LDA instruction and the PHASE LOOP switch in the same manner as the STA instruction was used.

1. LOAD ADDRESS 000000_8

2. LOAD MEMORY with 060000_8 (press HALT and LOAD MEMORY at the same time).

3. Press SINGLE CYCLE

4. Set PHASE LOOP Switch to LOOP Position

5. Press RUN.

5-119. This procedure will make the computer think it is loading the A-Register with the contents of every memory location. Since all 1's are written into memory, all 1's should be read out of memory. This will turn all sense amplifier circuits on, allowing the technician to check and compare waveshapes on the faulty sense amp card. The waveshapes are taken directly from the emitter of the output transistor of each circuit. A normal waveshape of a good sense amplifier is shown in Figure 5-22 with respect to T0. Notice at what times the waveshapes occur.

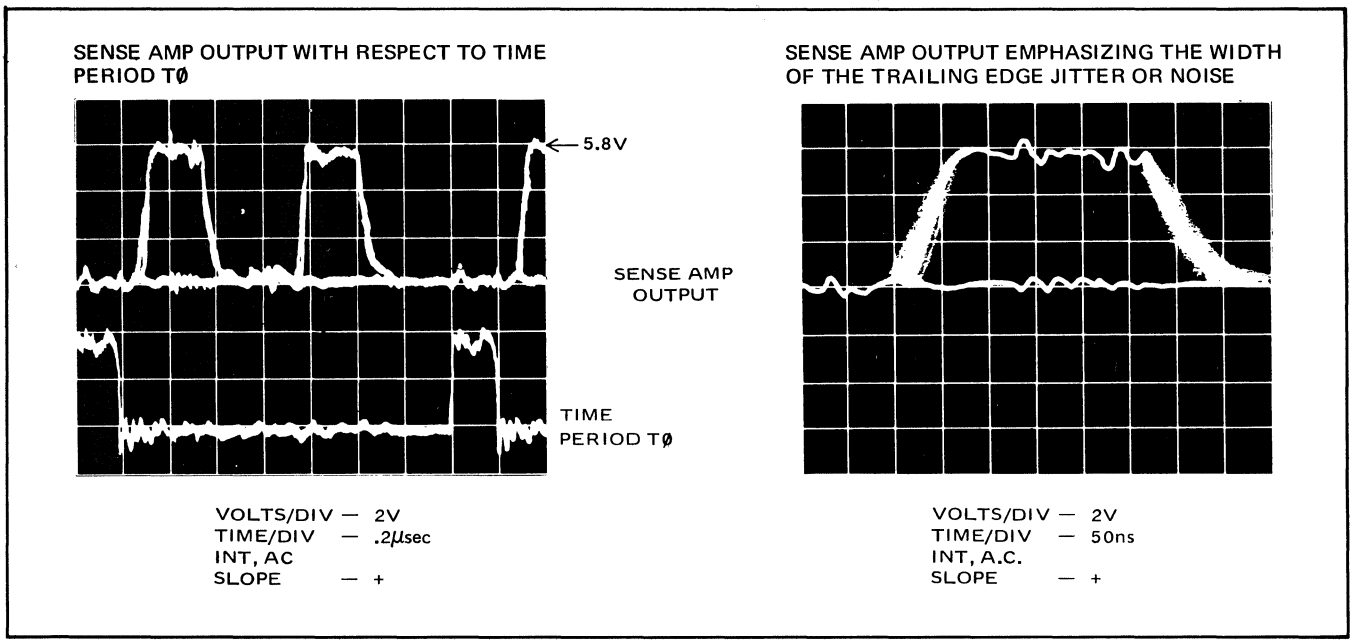


Figure 5-22. Sense AMP Output

5-120. The Sense Amplifier produces a double pulse signal every machine cycle when it senses a 1 from memory. The double pulse occurs both during the READ time (T0—T2) and during the WRITE time (T3—T5) because the actual core being addressed will change state twice during one machine cycle. This is caused by the X and Y currents through core being in one direction during the READ cycle which initiates a change of state of that addressed core to a 0 and then a current reversal on the X and Y lines during the WRITE cycle which changes the state of the address core back to a 1. The Sense Amplifier does not differentiate each change of state into a READ cycle change or a WRITE cycle change, so it will sense both changes of state. The pulse that the technician is worried about is the first signal from memory occurring during the READ cycle.

5-121. The technician should compare the suspected faulty circuit waveshape with other good waveshapes from associated circuits on the same board. He should compare amplitudes, check the timing of each signal (Determine whether the signal is being turned on at the correct time with respect to the machine cycle) and check the trailing edge of the first waveshape from the sense amplifier for jitter width.

5-122. The amplitude of the Sense Amplifier signals should approximately equal 5.8v ± 0.3v. It is left to the technician to determine whether a problem is being produced by a Sense Amplifiers with specifications under or over those that are given.

5-123. When checking the timing of each signal simply ensure that the signal is high at the beginning of time period T2 until the middle of time period T2 of the first waveshape. This ensures that the sense amp output correlates to the MST timing signal which allows information to be strobed into the T-Register.

5-124. The specifications for the trailing edge jitter or noise should not exceed 50ns in width. Jitter or noise width greater than 50ns can cause the sense amplifier to output a constant high voltage which would always look like a 1 coming out of memory. This problem is not very common but can possibly occur. It is not obvious what would cause this problem when all signals seem to be operating correctly, therefore, the technician should be aware of this possible problem.

INPUT/OUTPUT SYSTEM

VI

SECTION VI
INPUT/OUTPUT SYSTEM

6-1. INTRODUCTION.

6-2. A review of Figure 4-1, the bus structure of the HP 2114B Computer, shows the overall input/output relationship. The data is outputed on the IOB lines from the A or B registers by the effect of an OTA/B instruction which puts the data into the $\overline{\text{R-bus}}$ and is gated to the IOB lines. Data being inputed from the IOB lines is put directly onto the $\overline{\text{T-BUS}}$. The I/O Control assembly encodes the select code information, and provides flag, control and interrupt capabilities. The HP 2114B Computer provides seven I/O slots plus provides for the capability of Direct Memory Access (DMA). An I/O Extender option HP 2151A provides additional I/O slots maintaining interrupt priority. An I/O Multiplex option allows the availability of the computer signals for equipment the customer may design.

6-3. I/O CONTROL ASSEMBLY.

6-4. The I/O Control assembly contains the circuitry for power fail interrupt, I/O device interrupt flip-flops, central interrupt address register, select code encoding, and select code output signals. The Volume 3 Input/Output System Operation Manual contains descriptions of the circuit operation for flag, control and interrupt. It also contains power requirements for I/O peripheral interfaces. It shows the signal pin assignments for the computer to interface connections, and for the I/O Control card to computer pin connections.

6-5. INTERRUPT PHASE 4.

6-6. The Computer Phase 4 Interrupt operation provides for decrementing the P-Register, clearing the M-Register bits 6 to 15, setting the M-Register bits 0 to 5, and setting Phase 1. This forces the next computer machine cycle to the memory address associated with the select code (called trap cell).

6-7. The trap cell will normally contain a JSB or JSB,I instruction which allows the P-Register to be stored providing a return address to the computer program location prior to interrupt.

6-8. INTERRUPT OPERATION FOLLOWING PHASE 4.

6-9. A sequence of operations must follow the Interrupt Phase 4. The first machine cycle following a phase 4 will fetch the contents of the trap cell. This instruction is normally a JSB or JSB,I which stores the return address of the main program in the subroutine NOP location. During time T1 the IAK signal is generated.

6-10. This signal clears the interface (device) Flag Buffer flip flop. During time T7S the Store T bus in the M-Register (bits 6 to 9) signal sets the Interrupt Inhibit flip-flop located on the I/O Control Card.

6-11. During the next machine cycle, which can be Phase 1, 2, or 3 the TOTS clears the Interrupt Inhibit flip-flop, and sets the Interrupt Control flip-flop. This completes the hardware routine following interrupt Phase 4. A software routine must clear the device flag to allow the PRL line to function. Without this operation no lower priority device can interrupt.

6-12. CONDITIONS WHICH ALLOW PHASE 4.

6-13. Figure 6-1 is a flow chart indicating the conditions which must be met to allow Phase 4 Interrupt operation. It

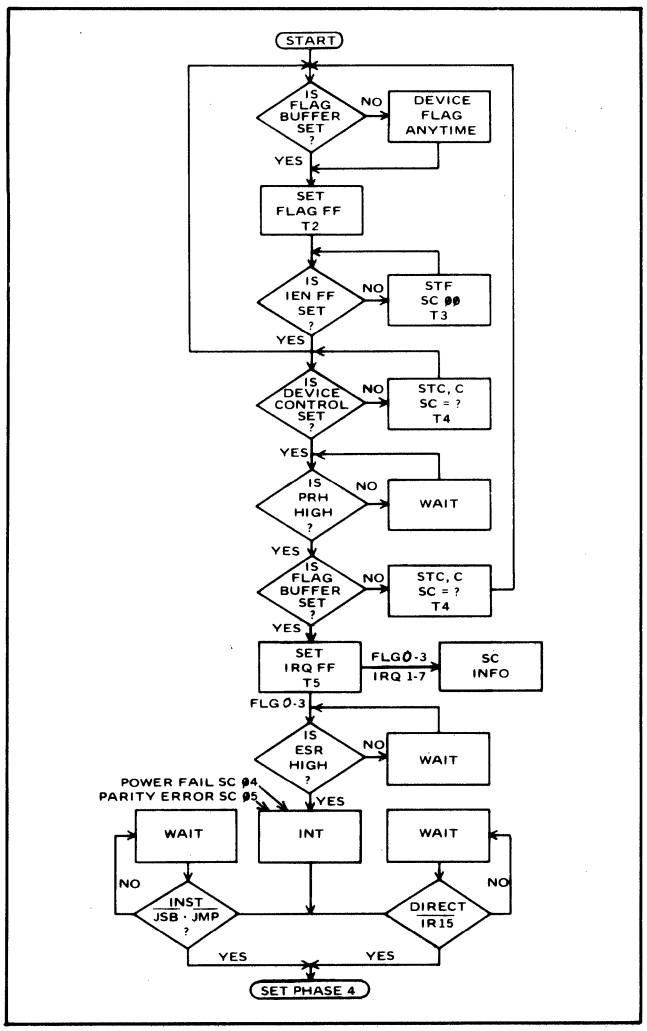


Figure 6-1. Interrupt Flow Chart

will be noted that the Power Fail interrupt at select code 04, and the Parity Error interrupt at select code 05 can directly set Phase 4. Phase 4 operation takes precedence over all lower phase operations. Once the INT signal is generated the only conditions which will hold off Phase 4 are the coincidence of the JSB or JMP along with the indirect IR15. The flow chart summarizes the control flag and interrupt conditions.

6-14. When the external device has completed its operation, it generates a device flag signal to the interface card flag generator which sets the flag buffer flip-flop (see figure 6-2). The output of the flag buffer flip-flop in conjunction with the ENF (enable flag) signal from the Timing Generator card at time T2 causes "and" gate A to set the flag flip-flop. The flag flip-flop output is "anded" at gate B with the output of "and" gate C. The gate C output is true when the control flip-flop is set and when the IEN (interrupt enable) signal is received from the I/O control card. Unless the control flip-flop is set by a set control (STC) instruction, an interrupt request cannot occur.

6-15. The control flip-flop is set under program control and therefore, may be set at any T4 time of a machine cycle, depending on the type of operation being performed.

6-16. The STC instruction is enabled to the control flip-flop by the SCM (select code most significant digit) and SCL (select code least significant digit) signals and the IOG (I/O group instruction) signal from the I/O control card. The SCM and SCL signals are enabled on the individual interface card by the IOG signal which occurs when the instruction to be performed is an I/O group instruction. When the control flip-flop sets, a true input is applied to "and" gate C. The inputs to "and" gates B and C are then true and gate B applies a true output to inverting "or" gate D. The false output of gate D disables "and" gate E, making the priority network bus to the lower-priority devices false. This prevents any device of lower priority from requesting an interrupt.

6-17. At the same time that gate B applied a true output to gate D, it also applied a true output to "and" gate F. The priority network signal to gate F will be true if an interface card (device) of higher priority than the one represented in figure 6-2 is not requesting an interrupt. In this case, the true output of gate F is combined with the SIR (Set Interrupt Request) signal from the I/O control card at time T5 and the output of the set flag buffer flip-flop to provide a true output from "and" gate G. The gate G output sets the IRQ (interrupt request) flip-flop.

6-18. The IRQ flip-flop outputs provide the flag signal and the IRQ signal to the I/O address circuits. (The IRQ signal is obtained by the inversion of the false clear side output of the IRQ flip-flop by inverting "or" gate H.) The flag signal is "anded" in the I/O address circuits with the enable service request (ESR) signal from the I/O control circuits to form an interrupt signal. However, the ESR signal is false for the remainder of the machine cycle during which an instruction occurs that effects device priorities as determined by the I/O control circuits. At time T2, the

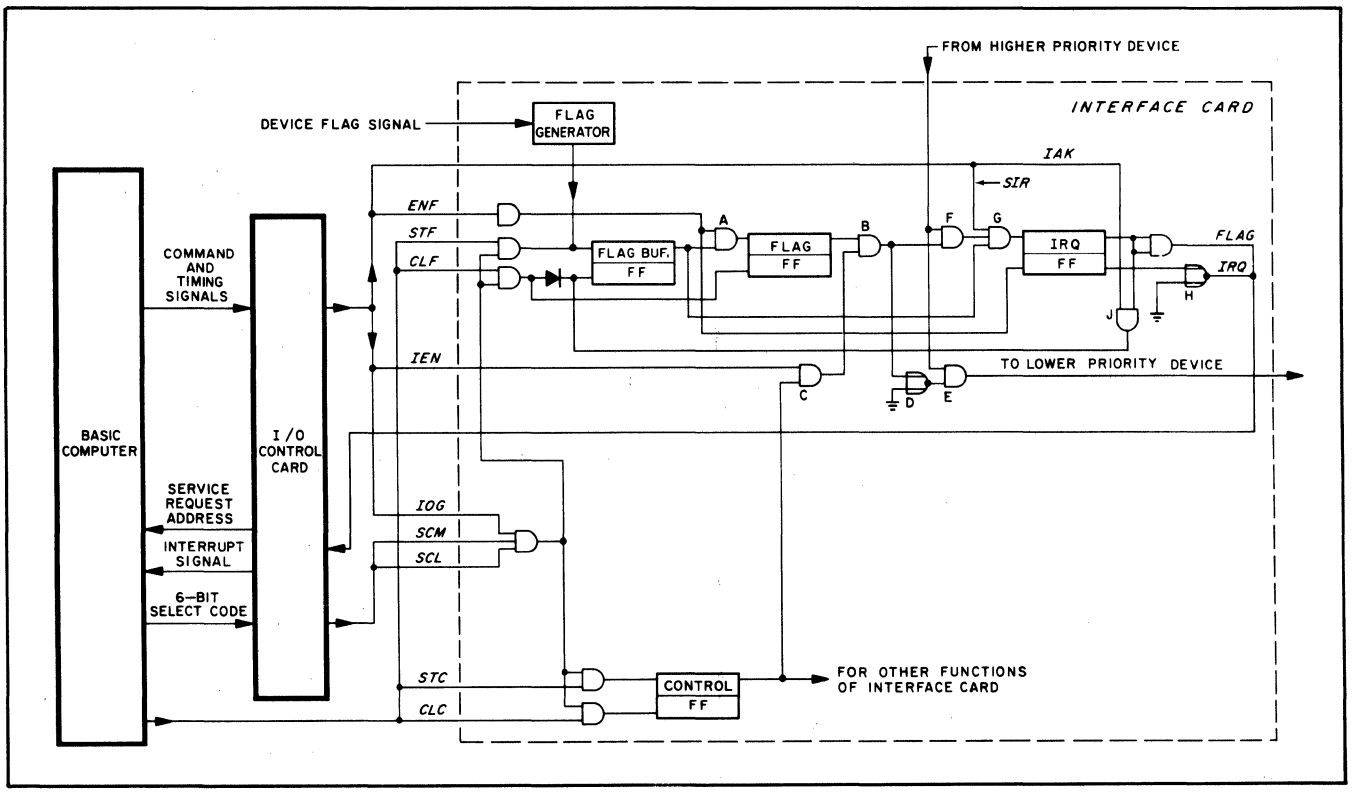


Figure 6-2. Typical Interrupt Logic

higher-priority device to request an interrupt. If the control flip-flop is still set and no higher-priority devices have requested an interrupt, the IRQ flip-flop will again be set at time T5 (SIR). The flag and IRQ signals are again sent to the I/O address circuits. The signals are used to form a 6-bit service request address to be sent to the computer at time T7 of the interrupt phase 4. The flag signal and the now true ESR signal form the interrupt signal which is sent to the computer. This signal causes an interrupt at the end of the current machine phase, switching the computer into the interrupt phase, except when any of the following conditions occur:

a. The computer is in the halt mode.

b. A jump indirect (JMP,I) or a jump to subroutine indirect (JSB,I) instruction is not fully executed. (These instructions inhibit all interrupts until fully executed for any number of indirect levels of addressing. An interrupt request will be granted at the beginning of the machine phase immediately following the complete execution of the JMP,I or JSB,I instruction.)

6-19. SELECT CODE GENERATION.

6-20. The I/O Control assembly has the one out of ten decoders to encode the binary information in octal form. This select code octal information is available through the 86-pin connector to the backplane, and through the 48-pin connector for external use. The input TR0 to TR2 generates the least significant select code information SCL0 to SCL7. T-Register bits TR3 to TR5 generate the most significant select code bits SCM1 to SCM3.

6-21. CENTRAL INTERRUPT REGISTER.

6-22. The interrupt request signals from the interrupting address are in octal form. The signals IRQ0 to IRQ7 are the least significant select code digits. The signals FLG1 to FLG3 are the most significant digits (and already are in binary form). These inputs are encoded into binary form. They are strobed into the Central Interrupt Register during Phase 4 operation at time T7. This Central Interrupt Register retains the select code address of the last interrupting location. This information is available to the computer via an input from select code 04, and is strobed onto the T bus bits 0 through 5.

6-23. I/O EXTENDER 2151A.

6-24. The HP 2151A I/O Extender provides additional I/O addresses for the 2114B Computer. I/O address 16 contains the I/O Extender interface board. The interface board consists of traces to provide the necessary output signals for the extender module. Two cables are necessary, one on the I/O Control assembly, and one of the Extender Interface board. The I/O Extender picks up address 16 and adds addresses 20 to 27, and addresses 30 to 37. It retains the priority interrupt structure. The HP 2151A module is similar in design to the 2114B module, including power supply.

6-25. I/O MULTIPLEX.

6-26. The 2114B Computer can also provide I/O Multiplex commonly called Party Line operation. The I/O Multiplex interface board can be inserted in any address slot address 10 to 16. The interrupt priority of the customer's designed system retains the priority of the address slot utilized. The multiplexed I/O Data assembly consists of buffers. The IOB input/output buses are buffered and provide OR-tying capabilities on the 48-pin connector (ground true signals). This allows data outputs to the external device, and inputs from the external device to the computer on these common buses. The computer control signals such as STC, SFS, CLF, and so on are buffered. Their outputs on the 48-pin connector are ground true. The cabling to this external I/O Multiplex device has two cable assemblies one from the Data board and one from the I/O Control board. The select code information on the I/O Control board must be ground true also.

6-27. The ground true signals from the I/O Control assembly are produced by minor modifications to the I/O Control assembly. The jumpers W1 to W11 provide positive true select code outputs and are used in the I/O Extender. For the I/O Multiplex these jumpers are physically removed. Eight additional integrated circuit buffers are plugged in the appropriate integrated circuit sockets. They invert the polarity of the select code lines providing ground true signals. It is necessary to remove the jumpers to prevent coupling between these signals which would be detrimental to rise time.

6-28. POWER FAILURE - AUTOMATIC RESTART.

6-29. The Power Failure circuit with automatic restart provides an interrupt to select code 04. The trap cell 04 should contain either a halt, or the JSB to subroutine which services this power failure interrupt. The components associated with this power failure circuit provide the PON (Power Turn On) signal to the Computer, and the necessary control, flag, and IRQ flip-flops associated with the interrupt.

6-30. POWER FAILURE HALT.

6-31. When the Power Failure Interrupt option is not provided, the power failure indication (PWF) from the power supply or the external power fail (XPF) from the external device provides a hardware halt through PEH bus. Both of these signals are ground true.

6-32. POWER ON CIRCUIT (PON).

6-33. The Power On circuit provides a turn on procedure insuring that the +5 volt computer power supply is high enough. During power failure it provides a timed delay power down condition. Refer to Figure 6-3. When PWF signal indicates the computer power is on transistor Q2 conducts. The input voltage to MC43C is low holding off transistor Q3. The collector of transistor Q3 is pulled high by zener diode CR1 to the +5 volt bus. The base of

transistor Q4 is pulled up saturating Q4. Q5 is nonconducting, providing a high base signal to transistor Q6. This provides the computer power on signal (PON).

6-34. The purpose of zener diode CR1 is to ensure that the PON signal is not present unless the voltage on the +5 volt bus exceeds approximately +4.7 volts.

6-35. When PWF signal goes low, indicating power failure, transistor Q2 is nonconducting. The collector of Q2 allows a charge path for capacitor C52. The positive voltage on C52 changes the state of MC43C, resulting in the PON signal going toward ground. The time constant through resistor R32 and R33 into C52 is approximately 4 milliseconds. The sales specification is 1.5 milliseconds minimum. This provides a guaranteed minimum time for the computer to operate after power failure has been detected with guaranteed proper computer operation.

6-36. POWER DOWN OPERATION SEQUENCE.

6-37. During power turn on the power fail circuitry undergoes certain prescribed changes. (Refer to Figure 6-4.) After the initial request for Power Fail interrupt has been processed the Power Fail circuitry sits in a ready condition. That condition is as follows: The ARM flip-flop and Direction flip-flop are both set. The PWF signal from the power supply along with timing clock signals ensures the condition of these two flip-flops. The D input to the Flag flip-flop is high. Power failure will initiate a clock signal to the Flag flip-flop which will set the Flag flip-flop and the IRQ flip-flop resulting in the interrupt request. The Control flip-flop prevents subsequent power failure interrupts until cleared under program control. The status of the Direction flip-flop can be interrogated to determine whether computer power is coming up or going down.

6-38. The power failure sequence is as follows. The PWF signal goes negative indicating the sensing of failure on the AC line supply. This lowers the D input to the ARM flip-flop. At time T1 the clock signal clears the ARM flip-flop. The high output from the ARM flip flop pin 6 is "nanded" with the set output pin 9 of the Direction flip-flop. These two signals lower the clock signal to the Flag flip-flop. At time T2 the clock signal to the Direction flip-flop goes positive strobing the low input into the Direction flip-flop. Conditions on MC33C are now such that the clock signal to the Flag flip-flop goes positive. This sets the Flag flip-flop, and brings output pin 5 high. The Service Interrupt Request at time T5 sets the IRQ flip-flop. The output of the IRQ flip-flop requests an interrupt to select code 4, which forces interrupt operation Phase 4. The setting of the Flag flip-flop clears the Control flip-flop preventing another power fail interrupt until the Control flip-flop is serviced under program control. The interrupt to trap cell 4 performs a JSB or JSB,I to the service subroutine (which will be discussed in Paragraph 4-15), or a halt.

6-39. INITIAL POWER ON.

6-40. On initial power turn on the low PON signal directly clears the ARM flip-flop, Direction flip-flop, and Flag flip-flop. The low PON signal in conjunction with the high clear output from the Flag flip-flop sets the Control flip-flop and establishes the high PRL4 signal. The high input to the IRQ flip-flop pin 9 allows the ENF signal (T2) to clear the IRQ flip-flop.

6-41. After 0.3 second the PWF signal goes positive. Then the PON signal goes positive. This allows the power failure circuitry to function. The time T1 signal "nanded" with PRL4 clocks the ARM flip-flop setting it. This provides the proper signals to MC33B to lower the clock input to

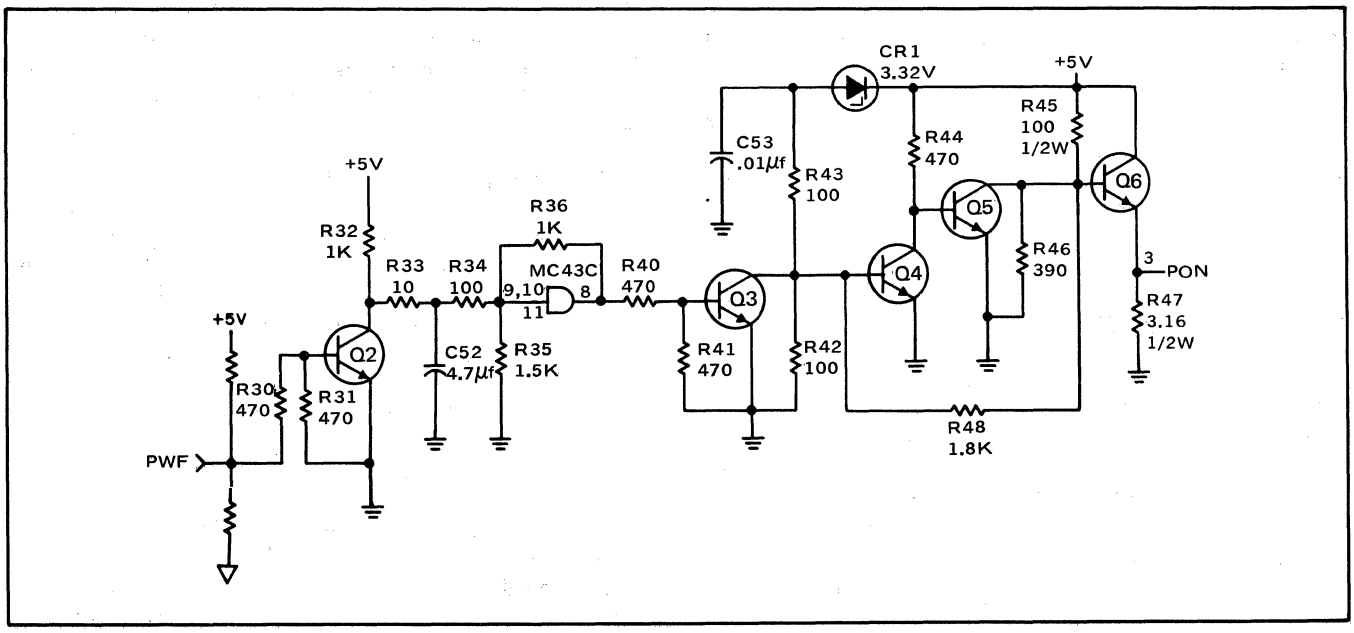


Figure 6-3. PON Circuit

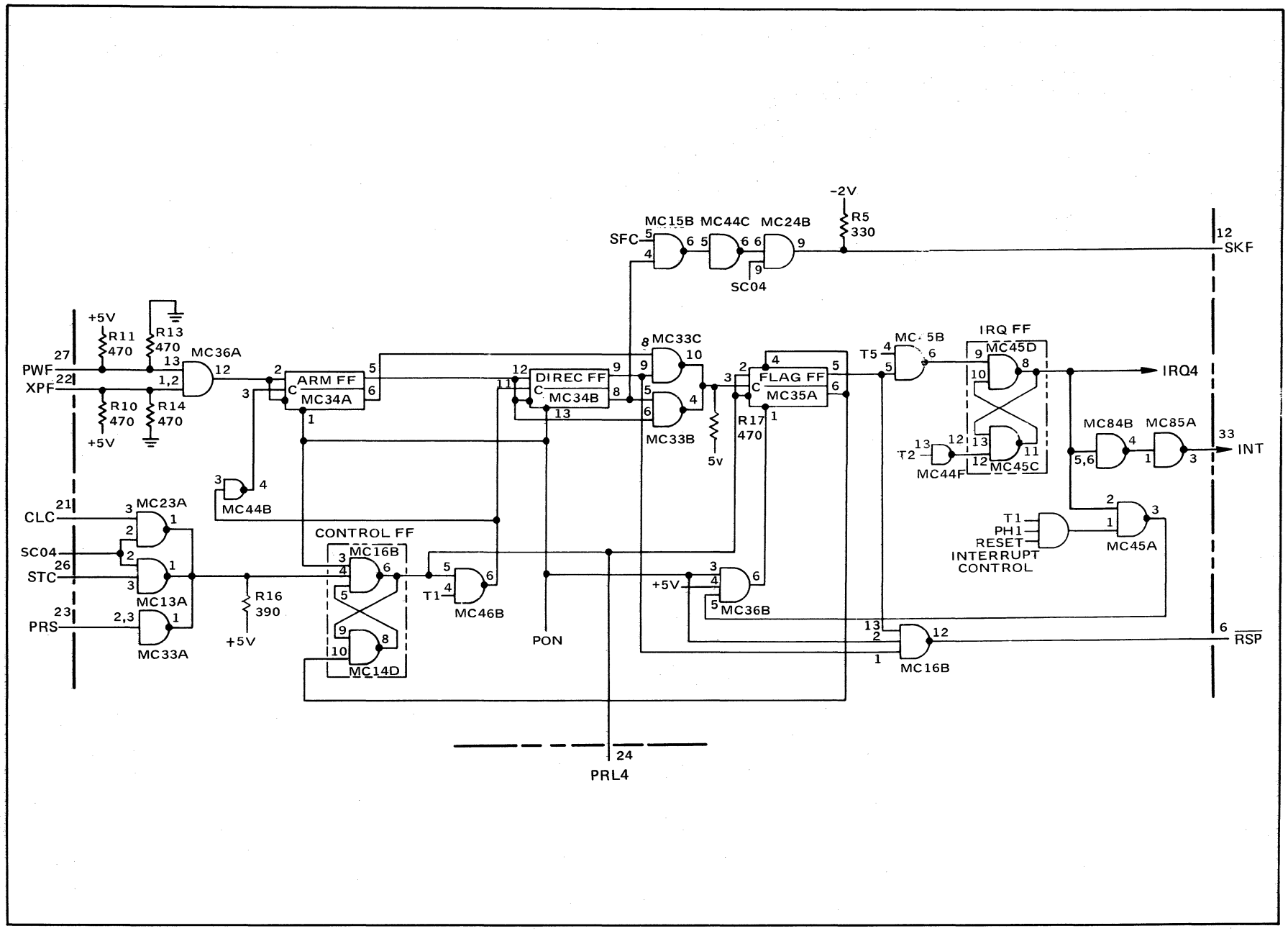


Figure 6-4. Simplified Power Fail Interrupt Circuit

the Flag flip-flop. At the end of time T1 the high D input to the Direction flip-flop is clocked in. The conditions on MC33B force the positive clock signal to the Flag flip-flop, setting it. The following time T5 signal sets the IRQ flip-flop. The IRQ flip-flop forces select code 04, and INT signal.

6-42. The three inputs to gate MC16A are positive. The Direction flip-flop is high indicating power is on, PON signal high indicates sufficient +5 volt bus for computer operation including adequate timing delay, and the Flag flip-flop output forces the gate. This provides the $\overline{\text{RSP}}$ restart pulse which initiates computer run condition.

6-43. The initial computer operation is Phase 4 Interrupt forcing memory address 4. The next operation performs the contents of memory address 04, which will normally be a JSB to the subroutine, or a halt signal.

644. The high IRQ flip-flop output clears the Flag flip-flop. Enable flag ENF at time T2 clears the IRQ flip-flop. The Control flip-flop must be cleared under program control. The completion of these operations leaves the computer in steady state run condition.

6-45. SERVICE SUBROUTINE.

6-46. (This program is prepared by the customer, and is not supplied by HP). The power fail subroutine normally includes a test to determine whether power is coming up or failing. For power failure the subroutine will provide instructions to save the state of the interrupt system, A, B, E, O, and Switch registers. If required it will also provide saving the status of the output register such as general purpose registers, relay registers, and so on. Where motor control or process control is included it should also perform the orderly shutdown on these process control functions.

6-47. The power on subroutine should provide turn on procedures for process control. It should re-establish proper output conditions on general purpose registers, relay registers, and so on. It should restore the status of the interrupt system, A, B, E, O, and Switch registers. The final instruction prior to the JSB through the stored address will be to set the Control flip-flop. This will allow another power failure interrupt.

6-48. The worst case condition will be on initial computer power turn on. After the interrupt request the re-establishment and initialization of all registers and functions is performed. If power failure has occurred during this time an interrupt is generated which interrupts immediately following the JSB indirect instruction. The service routine for power failure must then be performed prior to actual computer failure. This worst case condition requires that both store, and restore programs be completed within the 1.5 millisecond specification.

6-49. Hewlett-Packard diagnostic tests normally will not include either the Power Fail service routine, or the halt in location 4. It is very useful when servicing a computer to ensure the halt is in location 04.

6-50. TROUBLESHOOTING THE I/O SYSTEM.

6-51. The most common problem within the I/O system is the picking up or dropping of bits of information while transferring this information between the computer and I/O device. The problem can be caused directly from the I/O device, by the interface card associated to the I/O device, by the Arithmetic Logic boards, by the Parity Error board (if present) or by the DMA board (if present). Each of these hardware parts are interconnected by common IOB lines for inputting and outputting information and can possibly be the cause of the problem.

6-52. The technician now has to determine exactly what section is causing the problem. The quickest way to reduce the problem is to remove boards that can be removed or switch boards that can be switched. But first, the IOB lines have to be initialized with data by setting up a small diagnostic program that allows inputting and outputting data.

6-53. The 16-Bit Duplex Register Interface card with a special hood attachment (the hood simply shorts all pins of the connector to the corresponding pins on the opposite side of the connector) is the best interface card to use in conjunction with troubleshooting the I/O system. This is the best board to use simply because it provides a 16-Bit Input Register and a 16-Bit Output Register with which the technician can enable all the IOB lines at one time to ensure correct operation of all the IOB lines. If the 16-Bit Duplex Register Interface card is not available then a standard Buffered TTY Interface card can be used. The only limitation with a TTY Interface board is that it will only check the 8 least significant IOB lines rather than all 16 IOB lines. This section will be written with the thought that the 16-Bit Duplex Register Interface Card is available but specific points will be brought out with respect to the TTY Interface card.

6-54. A quick check of the IOB lines, the Arithmetic Logic Card circuitry associated with the IOB lines, and a specific interface slot using the 16-Bit Duplex Register Interface Card can be performed from the following short looping program:

```
LIA 01      102501
OTA 10      102610
STC 10      102710
LIB 10      106510
JMP*-4      026---
```

6-55. This program inputs information from the Switch Register to the A-Register, outputs this information to the select code being tested and reads the same information back to the B-Register. If any bits of information are being lost or if extra information is being picked up it will be displayed in the B-Register.

6-56. If the TTY interface card is being used, this instruction is not needed. The STC instruction used with the 16-Bit Duplex Register Interface Card and the special hood

provides a clock signal to the output register on the board. This allows the information just inputted to the input register from the computer to be put into the output register on the same card.

6-57. This small diagnostic program allows the technician to enable any or all of the IOB lines by simply loading the A-Register from the Switch Register. To begin the program the technician should load all one's into the A-Register, halt the machine and display the contents of the B-Register. The HP 2114B does not have a display for the A-Register or B-Register so the technician will have to loop his program, halt the machine and manually check the contents of the B-Register. The B-Register should contain the contents of the A-Register which, in turn, should contain the contents of the Switch Register.

6-58. Once the all one's condition has been checked, load in all zero's and check the A-Register and B-Register for correct data. Once the technician is confident that the machine is working properly by loading all one's and zero's, he should load in bit patterns as he did for one's and zero's. These bit patterns can possibly detect a problem that loading all one's or loading all zero's did not detect.

6-59. If any error is detected the technician should reduce his problem to one specific card. Remove any card that is associated with the IOB lines that may be causing the problem and can be removed without affecting the machine in other ways. That is, remove the DMA card (if present), remove the Parity Error Card (if present), and remove all other interface boards other than the 16-Bit Duplex Register board or TTY Board being used in the program. If any of these boards or their respective I/O devices were causing the problem it would clear up upon removal of the board. REMOVE ONE AT A TIME and check the problem each time. (Interface boards can be removed while power is ON but never insert a board while power is ON.)

6-60. If the problem still remains, switch the Arithmetic Logic Card associated with the bad data. Switch the card with one of the other identical Arithmetic Logic Card and perform the test again. If the problem was associated with the Arithmetic Logic Card it should have followed the switch. This technique comes in very handy when only the TTY board is available. Although only the 8 least significant IOB lines can be checked with the TTY board by switching Arithmetic Logic Cards, this rules out any possibility of the Arithmetic Logic Cards causing the problem.

6-61. Once the technician has switched the Arithmetic Logic Cards he has reduced his problem to either the back plane wiring or the 16-Bit Duplex Register Board. A back plane wiring problem should not exist therefore should be the last area to check. Pull the 16-Bit Duplex Register Card out and loop the OTA 10 instruction. Check the IOB lines on any I/O slot. They should indicate the contents of the A-Register. If the fault is picking up bits, load the A-Register with all zeros: if the fault is dropping bits, load the A-Register with all ones. If the problem is still apparent, check the back plane wiring. If the problem has gone, the fault must be due to the interface board in the slot associated with Select Code 10.

6-62. All the I/O instructions are decoded on the Shift Logic Card. If any failure of the I/O instructions occur troubleshooting should begin on the Shift Logic Card.

6-63. To check the interrupt system for each I/O slot, use the following test program:

```
STF 0       102100
STC 10,C    103710
STF 10      102110
NOP         000000
JMP*-4      026---
```

6-64. Load each select code address (the trap cell) with HLT instructions and number the halts with its respective location. For example, the interrupt select code 00 address should contain 102000 and so on through select code 40.

6-65. If the computer is not interrupting to the correct location, this short program should tell the technician to what select code the computer is going. Put a JMP instruction back to the beginning of the short diagnostic program into the location that the computer is interrupting so the program will loop continuously. Now the technician can begin troubleshooting the I/O system to try and determine why the computer is not interrupting to the correct location. The technician should begin on the I/O Control Card where the select code is being decoded. He should also keep in mind that all I/O instructions are decoded on the Shift Logic Card and that Phase 4 is set on the Timing Generator Card.

6-66. Most of the hardware problems associated with the I/O System are due to the I/O devices. The technician should always be aware that approximately 90% of all hardware problems will be due to a faulty I/O device.

6-67. DMA.

6-68. GENERAL DESCRIPTION.

6-69. The DMA option is used with the HP 2114B general purpose computer. The DMA option consists of a single plug-in card, which plugs into a prewired slot in the computer. DMA is single-channelled and is program-assignable to addresses 10 through 16. The HP 12607A DMA Accessory Kit includes the following items:

a. 12607-6001 Single-Channel DMA card.

b. 12607-90002 DMA Operating and Service Manual and Diagnostic Supplement.

c. HP 20524A (or later) DMA Binary Diagnostic Tape.

d. HP 20525A (or later) DMA Binary Rate and Transfer Diagnostic Tape.

6-70. DMA enables the computer to transfer data directly between memory and external devices at a maximum rate of 500,000 16-bit words per second in block lengths of 1 to 8192 words. Word transfer time is 2.0 microseconds for each 16-bit word. No character packing hardware is provided on the card; when using byte (eight bit) oriented devices, character packing and unpacking may be accomplished with software, before or after data transfer.

6-71. To be placed in operation, the DMA system must first be initialized for a specific operating mode by instructions and control words in the main program. Data interchange then occurs automatically when a service request signal is received from an I/O channel programmed to DMA.

6-72. The DMA option then takes control of the central processor and I/O system, suspends the running program at the end of the current phase, and during the following machine cycle, generates a special phase 5 memory cycle to read or write a word directly into or out of a predetermined memory location. At the end of the phase 5 memory cycle (one complete machine cycle), control is returned to the central processor and I/O system, and the main program is automatically resumed at the point where it was suspended, without loss of continuity. A new phase 5 cycle is initiated each time the I/O device signals DMA that it is ready to input or output another word. When all data in a predetermined block length have been transferred, DMA initiates a normal interrupt to a service subroutine.

6-73. MAJOR ADVANTAGES.

6-74. The advantages to incorporating the DMA option in a computer system are:

a. Fast Data Transfer: Under DMA control, data may be transferred between the computer memory and external devices at the rate of up to 500,000 (16-bit) words per second, which means the range of computer capabilities may be extended to include applications where data is generated at rapid rates and in large quantities. Also, data may be transferred in block lengths from one word to 8,192 words.

b. Program Independent: Data interchange occurs automatically as DMA "steals" memory cycles from the running program to read or write data directly from memory. By merely delaying regular program execution for the number of memory cycles "stolen," we can have regular program control with the fast access feature of the DMA option.

6-75. INSTALLATION.

6-76. No special installation procedures are required to install the DMA option. However, make certain that power is off at the computer before plugging the DMA card into connector XA16 in the computer mainframe. After the DMA card has been installed, perform diagnostic test procedures contained in the diagnostic supplement to this manual to ensure proper operation of the DMA card.

6-77. PROGRAMMING.

6-78. PROGRAM WORD FORMATS.

6-79. The DMA option is programmed using HP assembler language. (This language is explained in Volume 1, HP Computer Maintenance Course.) The instruction, control, and data word formats used in the operation of DMA are shown in figure 6-5 and are defined below.

a. Input/output instruction words: I/O group instructions addressed to select code 2 or 6 that permit the central processor to control the following DMA functions through the I/O select codes specified:

(1) Select code 2 permits initialization channel control flip-flop on DMA card to be addressed by CLC and STC instructions.

(2) Select code 2 preceded by a CLC instruction permits DMA memory address register to be addressed by an OTA instruction.

(3) Select code 2 preceded by a STC instruction permits DMA word count register to be addressed by OTA and LIA instructions.

(4) Select code 6 permits DMA switching functions to be addressed by OTA, CLC, STC, CLF, STF, SFC, and SFS instructions.

b. DMA program control words: Program constants that can be programmed to DMA to specify the following information:

(1) The I/O channel select code address of the device to be serviced by DMA (bits 0 through 2 select devices 10 through 16).

(2) Clear (turn off) control on device after last word in data block has been transferred (bit 13 = 1).

(3) Do not clear control on device after data transfer (bit 13 = 0).

(4) Set (turn on) control on device after each word in data block has been transferred (bit 15 = 1).

(5) Do not set control on device after each transfer (bit 15 = 0).

c. DMA address words: Program constants that can be programmed to DMA to specify the following information:

(1) Starting memory address for first word of input/output data block (bits 0 through 14).

(2) Memory input from device I/O channel (bit 15 = 1).

(3) Memory output to device I/O channel (bit 15 = 0).

d. DMA block length words: Program constants that can be programmed to DMA to specify the number of words in the data block. Word count is a number expressed as the two's complement of the positive binary equivalent of the number.

e. Data input/output words: Format used to transfer data directly between the device I/O channel and memory.

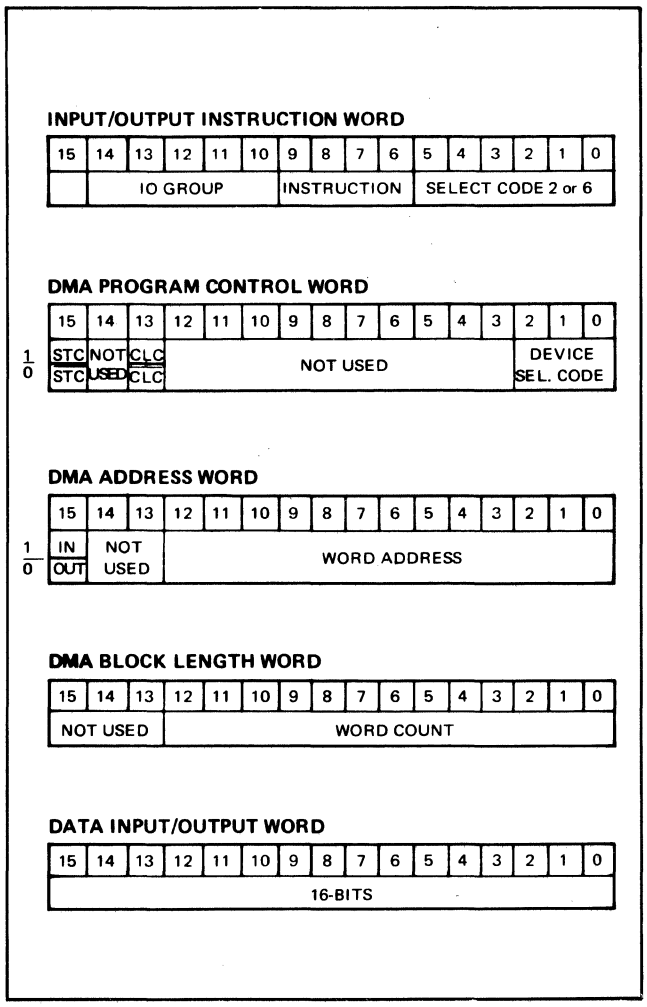


Figure 6-5. DMA Instruction and Control Word Formats

6-80. TYPICAL DMA PROGRAM.

6-81. An example of a typical program that uses the DMA option is listed in table 6-1. In this program, a memory input operation is carried out where a block of 50_{10} words is read from a tape read (I/O channel select code address 10_8) into computer memory locations 200_8 through 261_8.

Note

The program in table 6-1 assumes that the interrupt system is enabled (STF0 instruction) and that DMA will initiate an interrupt to a service subroutine when all words in the assigned data block have been transferred.

6-82. THEORY OF OPERATION.

6-83. FUNCTIONAL DESCRIPTION.

6-84. The DMA option adds a fifth phase to the four-phase capability of the basic computer. Phase 5 is a special memory cycle that requires one machine timing cycle (T0 through T7). Once initiated by service request signals received from I/O channels programmed to DMA, phase 5 operation is automatic and independent of program control. Each phase 5 cycle permits one input or output word to be exchanged between an external device (tape reader, disc memory, magnetic tape unit, etc.) and computer memory.

6-85. When a service request is received by DMA the main program is suspended for one machine cycle to achieve data transfer (one 16-bit word per cycle), rather than achieving data transfer by interrupting to a service subroutine. While the program is suspended, the computer is in phase 5 and data is transferred to or from the external device. At the end of the phase 5 cycle, the main program (now delayed by one machine cyle) continues from the point that it was suspended since the counting registers in the central processor are not stepped during a phase 5 cycle. A DMA interrupt occurs only after the word count function signals that all words in a data block have been transferred.

6-86. Figure 6-6 is a functional block diagram showing the relationship between the HP 2114B logic circuitry and the DMA logic. Table 6-2 lists the step-by-step sequence for DMA operation. When referencing figure 6-6 and table 6-2, assume that the typical DMA program in table 6-1 is being run. Since this program is for a memory input operation, table 6-2 does not cover the sequence for a memory output operation. However, the two operations are the same except for the signals generated to transfer data between the IOB lines and memory. These signals are shown for both operations in figure 6-6.

6-87. DETAILED CIRCUIT DESCRIPTION.

6-88. The following paragraphs contain a detailed circuit description for the DMA options. The description covers initialization, generation of a phase 5 signal, data input and output operations, DMA register stepping and device turn-off, and DMA completion interrupt.

Table 6-1. Typical DMA Program

LABEL	OP CODE	OPERAND	REMARKS
			INITIALIZE DMA FOR INPUT
ASGN	LDA	CW1	Fetches control word 1 (CW1) from memory and loads it in A-register.
	OTA	6	Outputs CW1 to DMA.
MAR	CLC	2	Prepares DMA memory address register to receive and store control word 2 (CW2).
	LDA	CW2	Fetches CW2 from memory and loads in in A-register.
	OTA	2	Outputs CW2 to DMA.
WCR	STC	2	Prepares DMA word count register to receive and store control word 3 (CW3).
	LDA	CW3	Fetches CW3 from memory and loads it in A-register.
	OTA	2	Outputs CW3 to DMA.
			START DEVICE AND DMA
STRT	STC	10B,C	Initiate tape reader data transfer.
	STC	6B,C	Activate DMA.
			DMA DATA TRANSFER
	. . .	. . .	Continue program while data transfer takes place.
			DMA CONTROL WORDS
CW1	OCT	120010	Assignment for DMA; specifies I/O channel select code address (10_8), STC after each word is transferred, and CLC after final word is transferred.
CW2	OCT	100200	Memory address register control for DMA; specifies memory input operation and starting memory address (200_8).
CW3	DEC	-50	Word count register control for DMA; specifies the two's complement of the number of words in the block to be transferred.

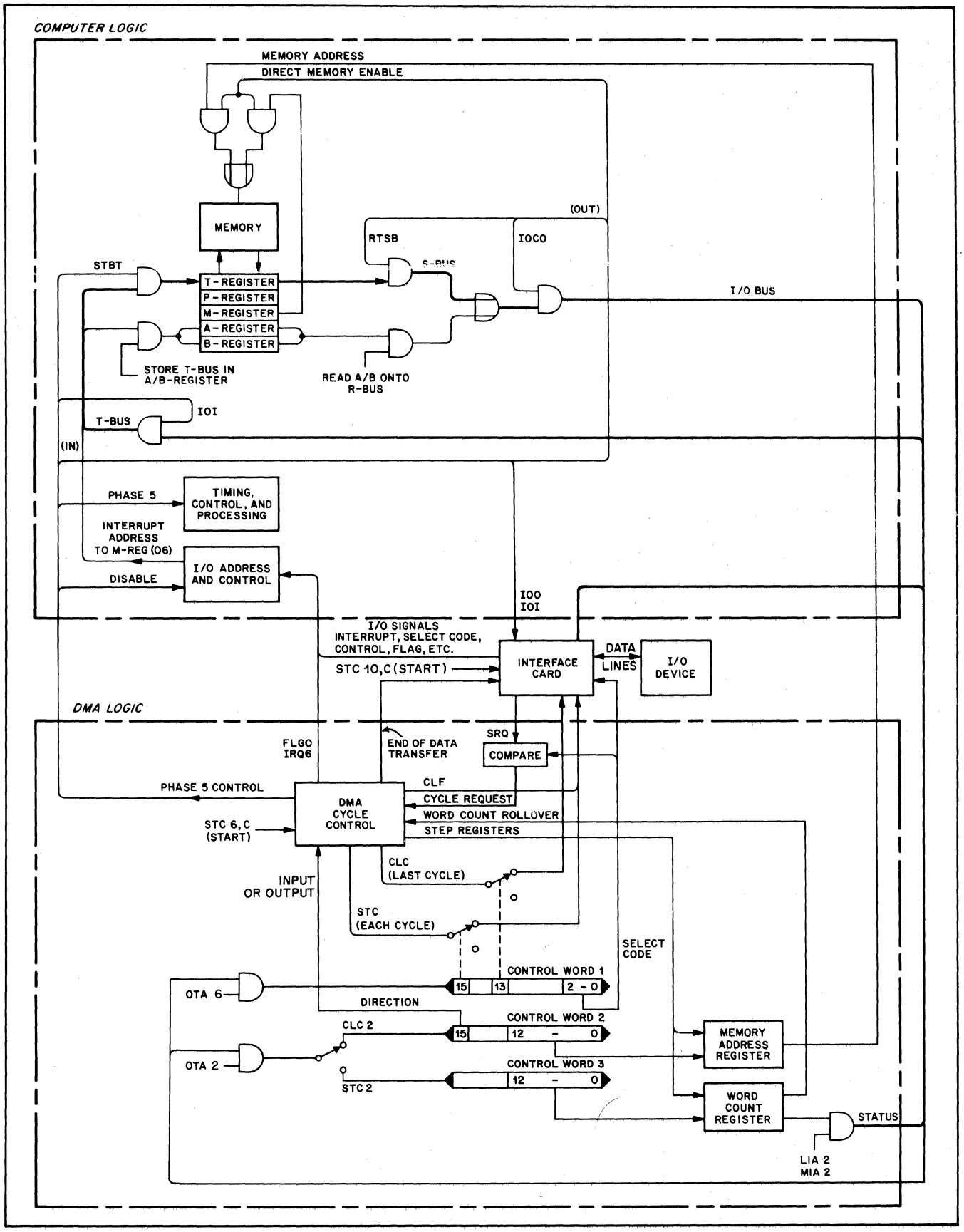


Figure 6-6. DMA Functional Block Diagram

Table 6-2. Basic Sequence for DMA Data Transfer

INITIALIZE DMA FOR AN INPUT OPERATION
a. Control word 1 (CW1) is transferred to the DMA card from the A-register on the IOB lines by an OTA 6 instruction. b. Bits 0 thru 3, 13, and 15 of CW1 are stored on the DMA card. Bits 0 thru 3 specify the select code of the device involved in the data transfer. Bit 13 (if true) specifies CLC of the device after the final word is transferred. Bit 15 (if true) specifies STC of the device after each word is transferred. c. A CLC 2 instruction prepares DMA to receive control word 2 (CW2), and OTA 2 transfers CW2 to the DMA card. d. Bits 0 thru 12 and 15 of CW2 are stored on the DMA card. Bits 0 thru 12 specify the starting address in memory of the data transfer and are stored in the memory address register. Bit 15 specifies whether the transfer is a memory input or an output operation (bit 15 = logic 1 = memory input operation). e. A STC 2 instruction prepares DMA to receive control word 3 (CW3), and OTA 2 transfers CW3 to the DMA card. f. Bits 0 thru 12 of CW3 are stored in the word count register of the DMA card and specify the 2's complement of the number of words (octal) in the block length of data to be transferred. g. I/O signals turn on DMA (STC 6,C) and the I/O device (STC 10,C).
DMA DATA TRANSFER
a. Device sets interface flag when ready to transfer data, generating an SRQ signal. b. On the DMA card, an SRQ signal is compared with the stored select code of the device and, if the select code of the device that originated the SRQ signal is the same as the select code that is stored on the DMA card, a cycle request signal is originated. c. The cycle request signal causes a PH5 signal to be generated at the end of the current cycle, which: (1) Puts the computer into the phase 5 mode, disabling all other phases and the instruction register. An ISG signal inhibits the reading of memory into the T-register. (2) Disables normal I/O operation by inhibiting select code logic. (3) Reads the interface card data onto the I/O bus lines using DMA generated select code and IOI signals. (4) Gates the data from the IOB lines onto the T-bus with an IOI signal. (5) Stores the T-bus bits in the T-register using a DMA STBT signal. (6) Enables the memory address register to select the desired memory location for input. d. The computer now continues into a memory cycle. Since memory reading is inhibited, the T-register retains the input word through the read portion of the memory cycle, and the word is written into memory on the write portion of the cycle. e. At the end of the phase 5 cycle, a CLF signal and a STC signal (if selected) are issued to the interface card, releasing the device to obtain the next input word.
DATA TRANSFER COMPLETION
a. At the beginning of each phase 5 cycle, the WORD COUNT register is advanced by one count allowing the register to advance one count closer to zero from the initial negative value. b. At the end of each phase 5 cycle, the memory address register is advanced by one count. This allows the memory address register to address the next higher memory location. c. When the word count register reaches zero, word count rollover occurs and the phase 5 cycle control is disabled. d. If the interrupt system is on, an interrupt to location 06 will occur through the interrupt system. e. Anytime during or after data transfer, the status of the word count register may be checked by LIA 2 or MIA 2 instruction, which loads the word count register into the A-register. f. A SFS 6 instruction may be used to test for transfer completion since the DMA flag is set at word count rollover. g. If selected during initialization, a CLC signal is issued to the interface card to turn off the device.

6-89. INITIALIZATION.

6-90. When the DMA option is initialized, the first control word is output to the DMA card on the IOB lines with an OTA 6 instruction in the main program. Referring to figure 6-7, at T3T4 when the OTA instruction has been decoded, bits 0, 1, and 2 are locked into the service select register FF's MC55A, MC55B, and MC55C. The bits are encoded by MC76 to provide the least significant octal digits of the select code of the external device involved in the data transfer. This information will remain on the Service Select (SS) lines until the data transfer is complete and a succeeding data transfer is initiated.

6-91. Also from control word 1, as shown in figure 6-8, if bit 13 is high the clear control FF will be set. This indicates that a CLC signal should be generated at the end of the data transfer in order to turn off the I/O device being

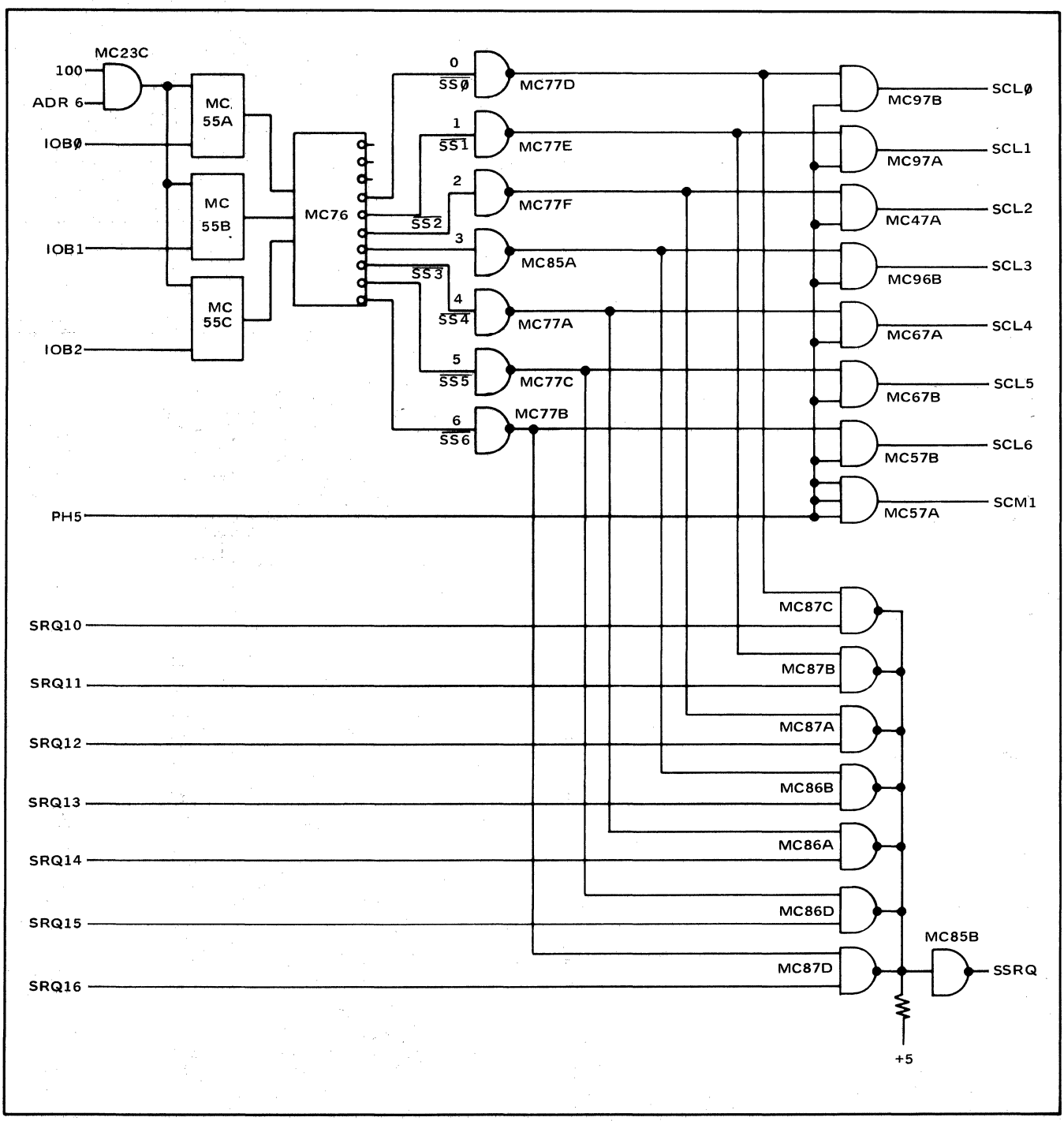


Figure 6-7. Device Channel Select Logic At Initialization

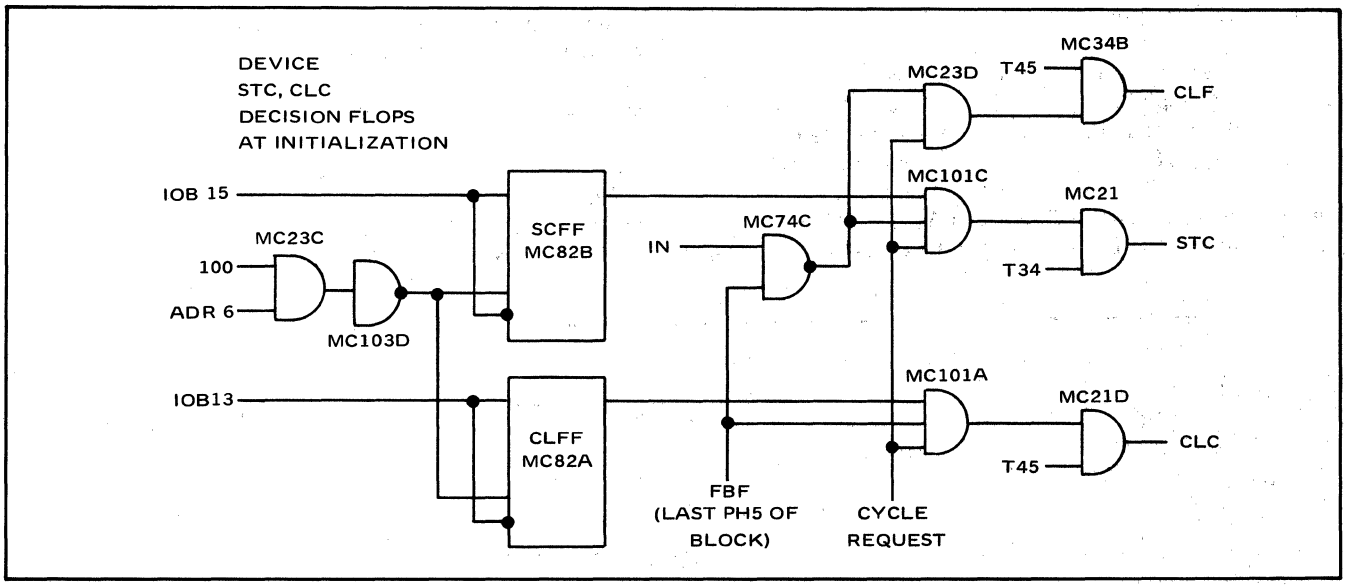


Figure 6-8. Initialization of Set Control and Clear Control FF's

serviced by DMA. The second option in control word 1 is to determine whether a STC signal should be generated after every data word transfer from DMA. This is done by setting bit 15 high which, in turn, will set the SET CONTROL FF on the DMA card. These FF's are clocked at T3T4 when the SC6 signal and the IOO signal are both true.

6-92. The second step in initialization DMA is to output a CLC 2 instruction which resets the Initialization Channel Control FF (see figure 6-9). The second control word may then be loaded into the A-Register and output to DMA over the IOB lines by a OTA 2 instruction. Bits 0 through 12 of control word 2 specify the starting address of the block of data to be transferred, and bit 15 specifies whether the data transfer is an input or an output operation (bit 15 = logic 1 - input operation). At T3T4 the IOO signal is true, making all inputs to MC14C true, and a false $\overline{\text{LMAR}}$ signal is generated. The false $\overline{\text{LMAR}}$ signal allows the starting address on the IOB lines to be clocked into the memory address register, and the address appears on lines XMR0 through XMR12. At the same time, bit 15 is clocked into the memory address register and pin 7 of MC75 goes true for a data input operation or false for an output operation.

6-93. Next, a STC 2 instruction is output to DMA which sets the Initialization Channel Control FF (figure 6-10). Control word 3 is then loaded into the A-Register and output to DMA on the IOB lines, again by an OTA 2 instruction. Bits 0 through 12 of control word 3 specify the 2's complement of the number of words in the data block to be transferred. At T3T4, all inputs to MC14B are true and a false LWCR signal clocks bits 0 through 12 of control word 3 into the word count register. The word count register output lines (WCR0 through WCR12) now reflect the 2's complement of the number of words in the data block.

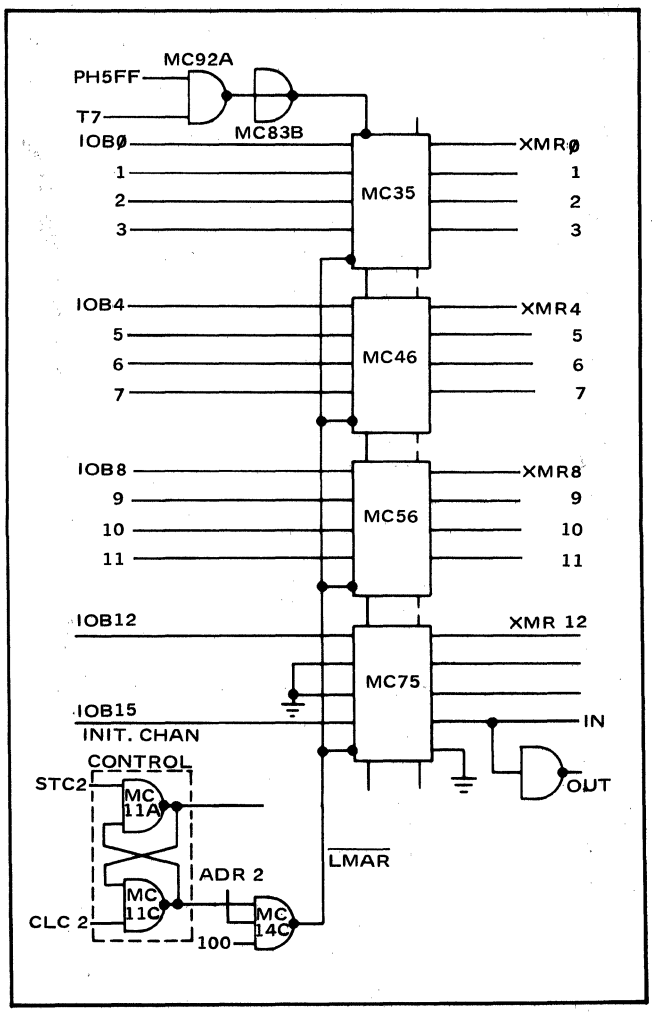


Figure 6-9. Memory Address Register

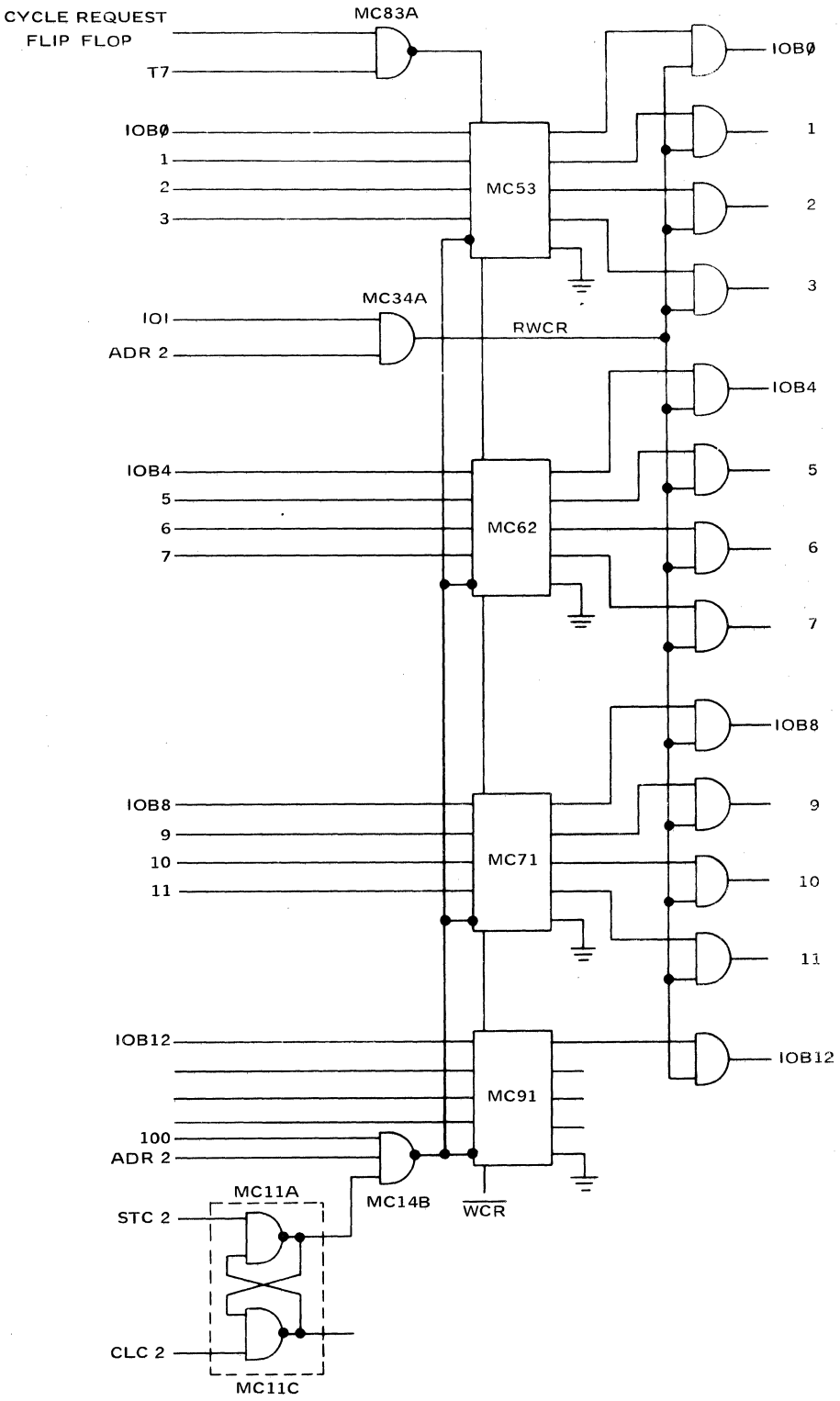


Figure 6-10. Word Count Register

6-94. An IOI signal (resulting from an LIA, LIB, MIA, or MIB instruction) will cause the WCR bits to be read onto the IOB lines if the respective instruction is addressed to code 2. This allows the status of the data transfer to be checked as desired.

6-95. The last step in the initialization process consists of setting control and clearing flag FF's on the DMA card and the device interface card to or from which data is to be transferred. Referring to figure 6-11, this is done by STC,C instructions in the program to the select code of the device and to select code 6 (the DMA select code). On the DMA card, the STC instruction sets the Interrupt Channel Control FF and the Transfer Enable FF. The CLF instruction resets the Flag Buffer FF and the Flag FF. Data transfer can now begin.

6-96. GENERATION OF A PHASE 5 SIGNAL.

6-97. When the device is ready to transfer a word, figure 6-12, an SRQ signal is generated on the appropriate SRQ line. The SRQ signal and the corresponding service select register bit are combined in a nand-gate. The resulting output is inverted by MC85B to provide the SSRQ signal. The true set output of the transfer enable FF and the SSRQ signal are combined in MC83C. The resulting false output of MC83C resets the cycle request FF at T4T5. At T7 of the same cycle, the phase 5 FF is set, generating the PH5 signal.

6-98. When the PH5 signal is generated, central processor operation is suspended for one machine cycle by the signals generated on the DMA card. The $\overline{PH5}$ signal at pin 83 is generated by inverting the PH5 signal in MC106A. During the phase 5, the signal inhibits the enable phase gate on the timing generator card and prevents the computer from going into phase 1, 2, 3, or 4 until phase 5 is complete. An $\overline{HIS}$ (Hold Interrupt System) low signal is also generated from the set side of the Cycle Request FF and the reset side of the PH5FF and is sent to the I/O Control Card to hold the interrupt system off during a phase 5. To accomplish data transfer, DMA must generate its own control signals that would normally be generated within the central processor unit.

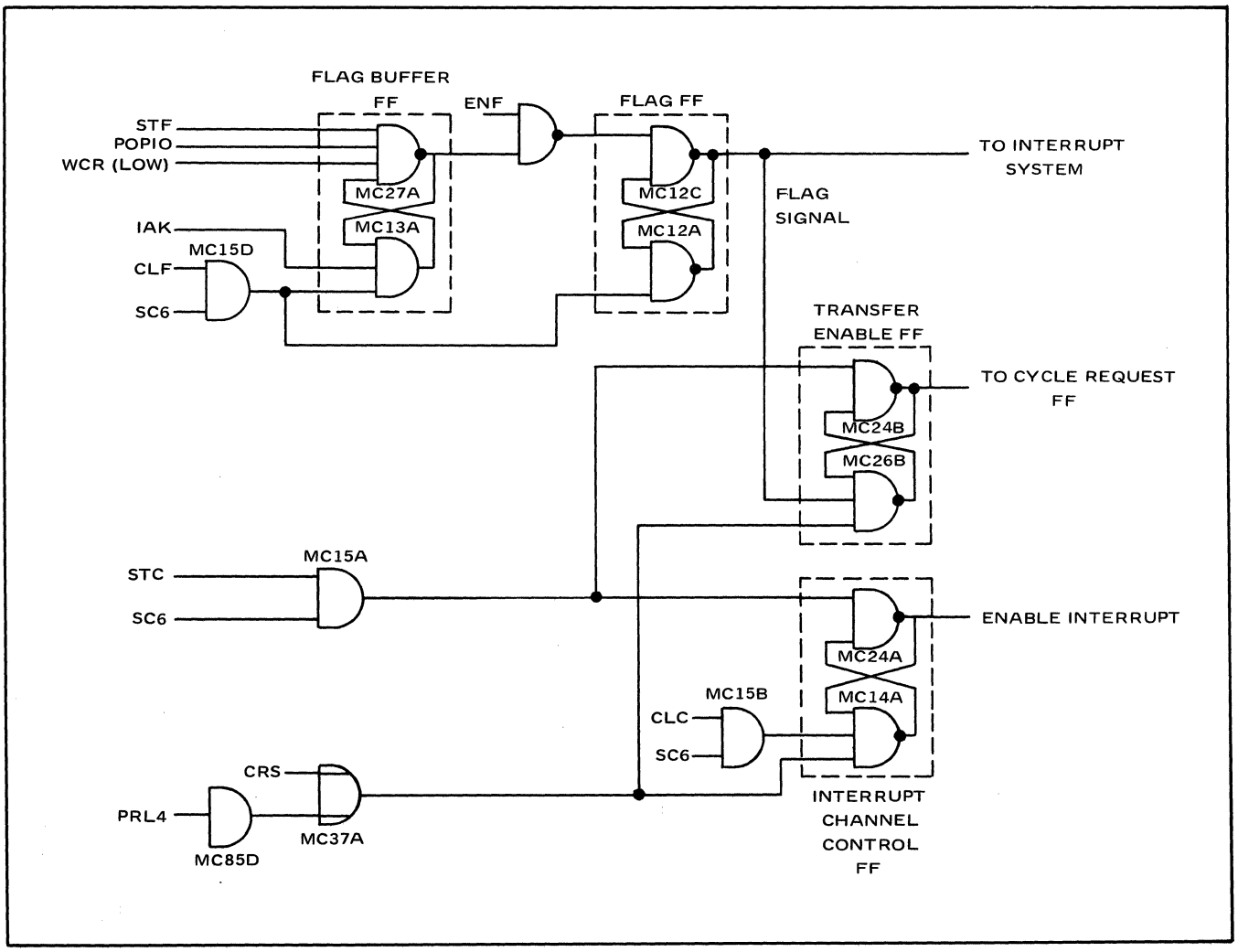


Figure 6-11. Turnig DMA On

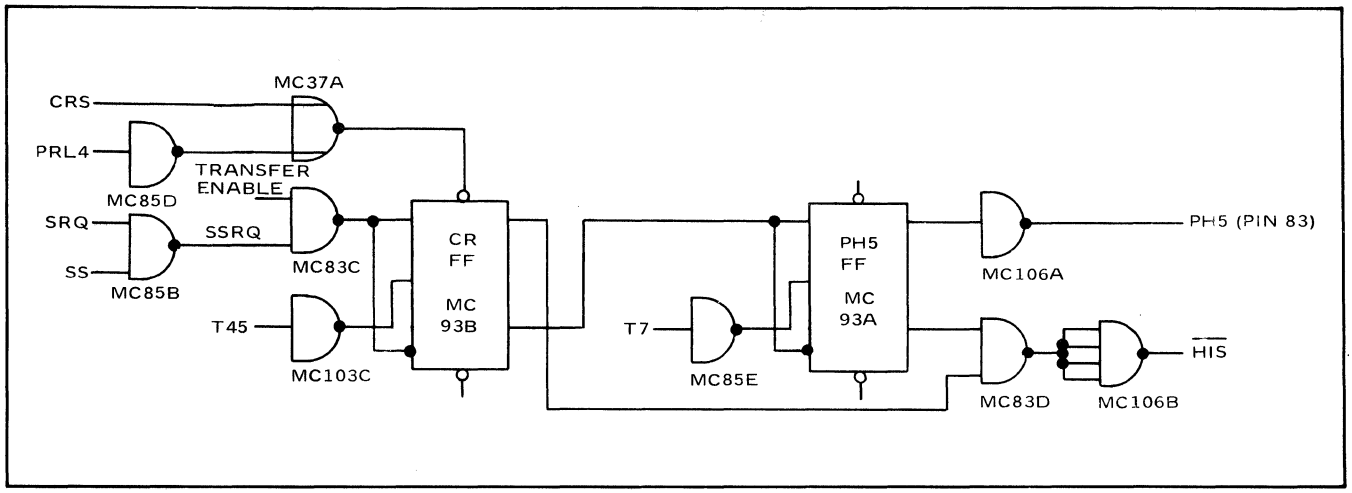


Figure 6-12. Cycle Request & PH5 Logic

6-99. DATA INPUT OPERATION (Figure 6-13).

6-100. When the phase 5 FF is set, the service select register bits are gated onto the select code lines along with the SCM1 signal. This allows DMA to address the device on the appropriate select code lines (10 through 16). At the device interface card, SCL and SCM signals from DMA are combined with an IOG signal and the resulting output is combined with an IOI signal to gate data from the interface card onto the IOB lines.

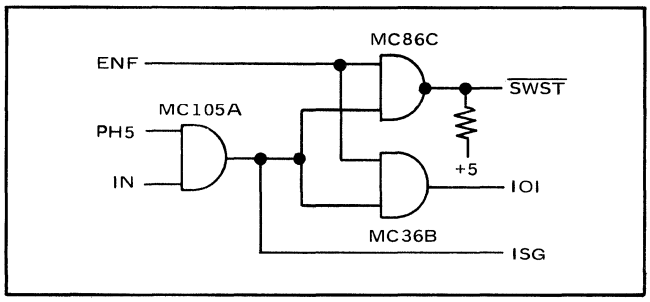


Figure 6-13. Circuits Unique to Input

6-101. On the DMA card, the PH5 and IN signals are combined in MC105A. The output of MC105A generates an ISG (Inhibit Strobe Generator) signal (pin 73) which will inhibit the memory strobe time (MST) signal from being generated on the computer timing generator card. The combination of the PH5 signal and the IN signal along with the ENF signal also generates the SWST and IOI signals. Referring to figure 6-14, the block diagram for transferring data from an external device to memory, the IOI signal gates the IOB bits onto the T-bus in the central processor.

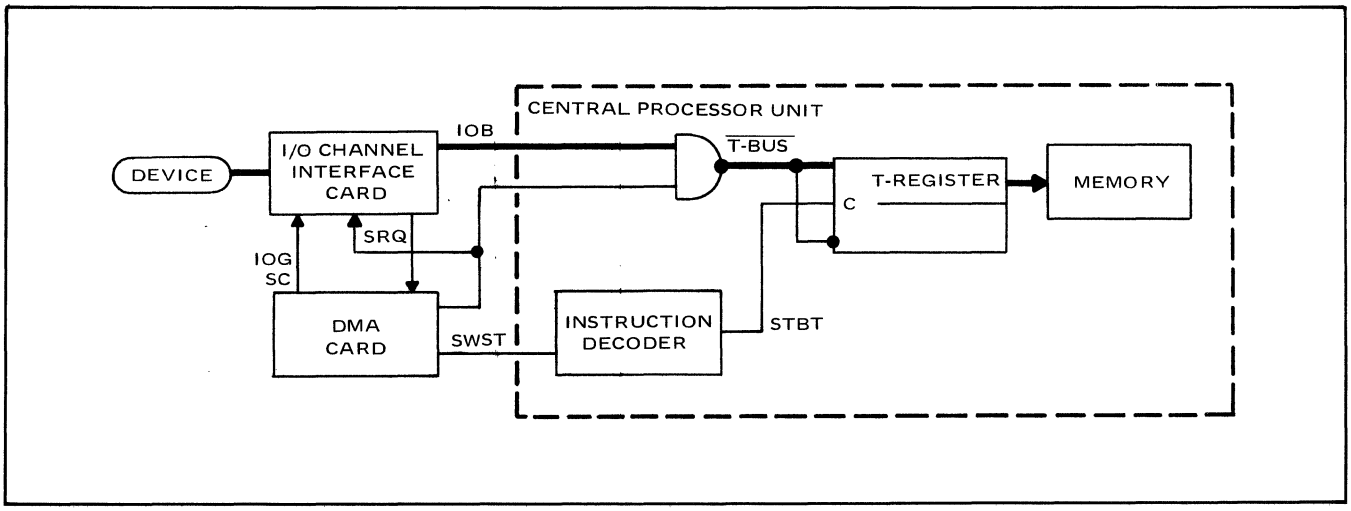


Figure 6-14. Transferring Data from an External Device to Memory

The $\overline{\text{SWST}}$ signal is decoded by the instruction decoder in the computer. The STBT signal, which results from the $\overline{\text{SWST}}$ signal being decoded, clocks the T-bus bits into the T-Register. The T-Register output is then routed directly into the computer memory and the data transfer for the first word is complete. This process is repeated for each word to be transferred into memory.

6-102. DATA OUTPUT OPERATION (Figures 6-15 and 6-16.)

6-103. When the phase 5 FF is set, the service select register bits are gated onto the select code lines along with the SCM1 signal, allowing DMA to address I/O select codes 10 through 16. At the device interface card, SCL, SCM, IOG, and IOO signals from DMA are used to gate data from the IOB lines into the interface card registers. To transfer data out of computer memory and onto the IOB lines, DMA generates $\overline{\text{XRTS}}$ and IOCO control signals (see figure 6-16). The $\overline{\text{XRTS}}$ signal and the RTS signal from the computer instruction decoder card combine to generate the RTSB signal. The RTSB signal gates the T-Register bits onto the $\overline{\text{S-bus}}$. The $\overline{\text{S-bus}}$ bits are inverted and are gated onto the IOB lines by the IOCO signal. The IOB bits are then transferred into the interface card and the device, as mentioned previously, and a single word transfer is complete. This process is repeated until all words in the data block have been transferred.

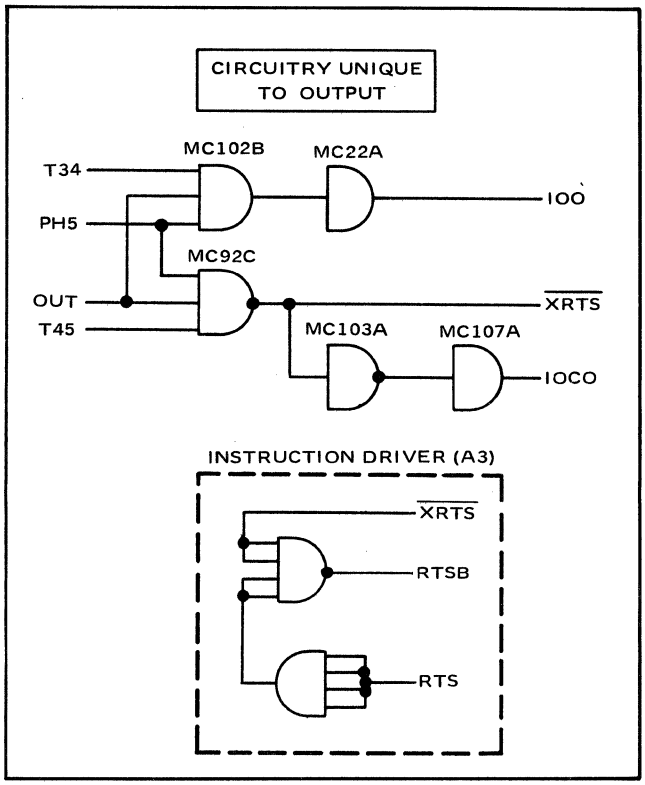


Figure 6-15. Circuitry Unique to Output

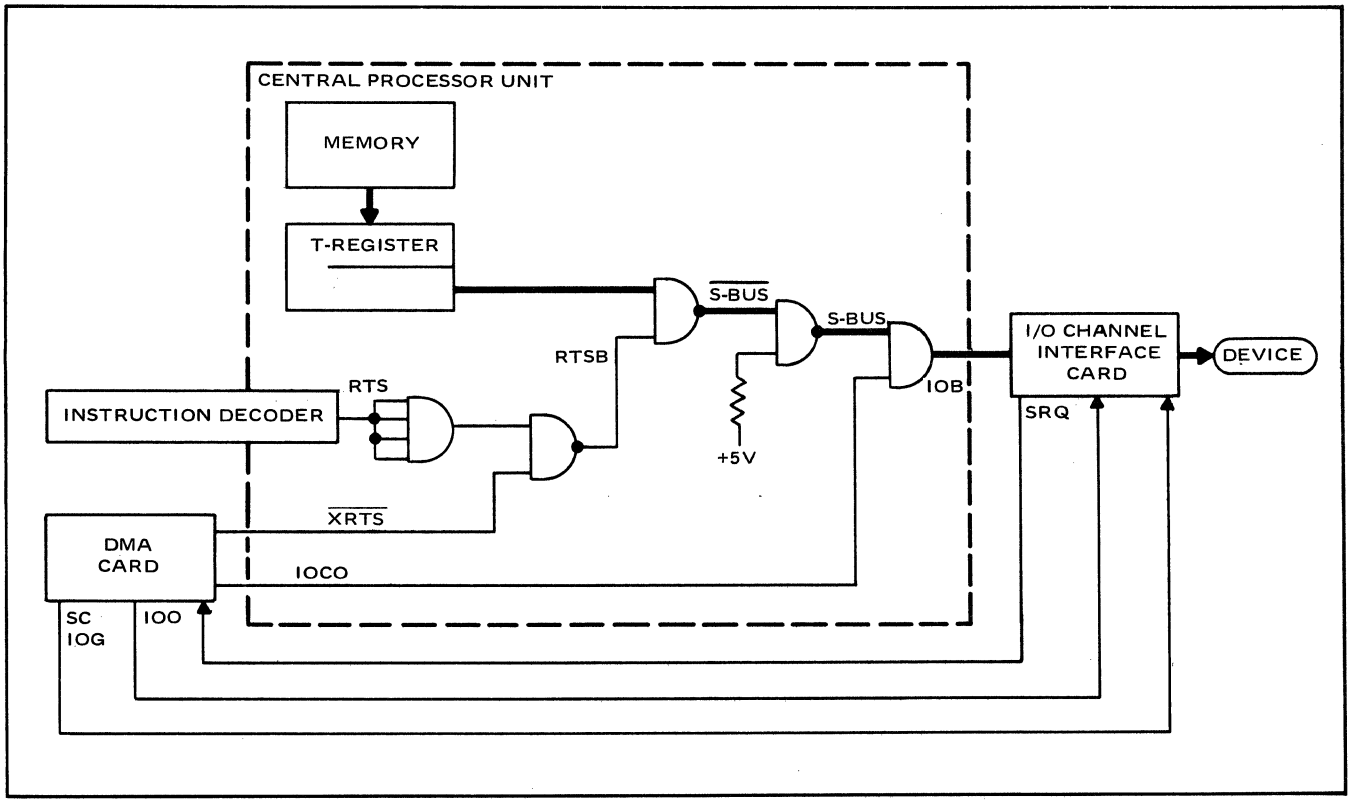


Figure 6-16. Transferring Data from Memory to an External Device

6-104. DMA REGISTER STEPPING AND DEVICE TURN-OFF.

6-105. Referring back to figure 6-9, at the beginning of T7 of PH5, the output of MC83B goes true, and the memory address register is advanced one count by the true SMAR signal. This updates the memory address register to the memory location involved in the next word transfer. At the end of T7 of the previous machine cycle to a phase 5, after the Cycle Request FF has been set, the output of MC83A goes true and the true $\overline{\text{SWCR}}$ signal advances the word count register one count (figure 6-10). The characteristics of the Register Counters is to step or count on the leading edge of each stepping signal; therefore, the stepping signal to each register has to go low and then be brought back to a high condition in order to step each counter.

6-106. The above process is repeated for each phase 5 cycle until all words in the data block have been transferred. Since the word count register is initially loaded with the two's complement of the number of words in the data block, the word count register will contain all zero's when all words have been transferred. The final $\overline{\text{SWCR}}$ signal sets all WCR bits to zero and causes pin 12 of MC91 (the carry output) to go false. The false WCR signal makes the output of MC101B false, setting the flag buffer FF. At T2, the ENF signal and the true FBFF signal set the flag FF.

6-107. Setting the STC and CLC FFs during initialization causes a STC signal to be generated after each word transfer and a CLC signal to be generated after the final word transfer. Figure 6-8 shows that the STC FF output is applied to MC101C along with the reset output of the cycle request FF and the output of MC74C. The MC74C output will be true until the last word transfer when the flag buffer FF is set. The cycle request FF is reset by every SRQ signal. Therefore, a STC signal will be generated at pin 22 of the DMA card for every word transfer except the last when the flag buffer FF is set. Also, the true output of MC74C causes a CLF signal to be generated at pin 7 every T4T5 to clear the device flag after every word transfer, except the last. The CLC FF output is applied to MC101A along with the reset output of the cycle request FF and the set output of the flag buffer FF. The false flag buffer FF output signal inhibits MC101A until after the final word transfer. The flag buffer FF signal then goes true and a CLC signal is generated at pin 21 of the DMA card to turn off the external device. This inhibits any SRQ signals from being generated by the device until DMA is reinitialized.

6-108. DMA COMPLETION INTERRUPT.

6-109. Figure 6-17 gives a circuit description of the Flag and Interrupt circuits. The true FBFF signals enable the generation of flag and interrupt signals at the end of the

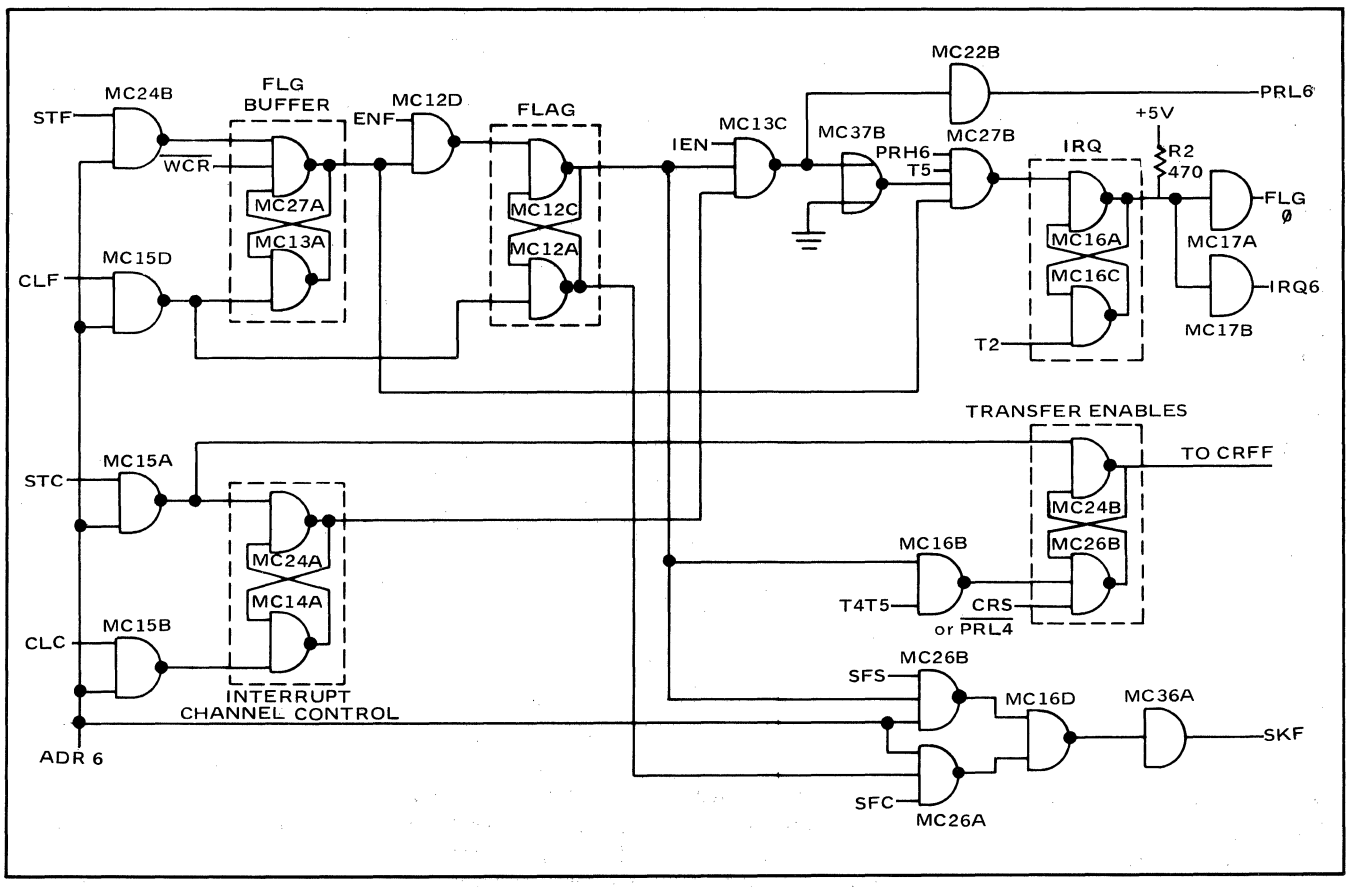


Figure 6-17. Flag & Interrupt Circuits

final word transfer. The true FLFF signal along with true ICCFF and IEN signals make MC13C output a false signal to MC37B. True signals from MC37B, FBFF, and PRH6 make MC27B output a false signal at T5 to set the interrupt request FF and generate FLG0 and IRQ6 signals. The FBFF signal also enables the generation of an EDT signal at the DMA card which is used by some of the I/O devices to signal the end of data transfer.

6-110. At the I/O control card, the FLG0 and IRQ6 signals try to generate an interrupt, but the interrupt system is disabled for at least one phase to allow a main program instruction to be executed following a phase 5 operation. At the end of this cycle, DMA interrupts, causing the generation of a phase 4 cycle and forcing the DMA trap cell location into the M-Register. The next fetched instruction will be the call instruction for the DMA completion subroutine.

6-111. DMA is turned off through hardware means on the DMA interface card. Upon the generation of the $\overline{WCR}$ from the Word Count Register, the Flag Buffer FF will be set. The low $\overline{WCR}$ signal is sent to pin 5 of MC27A, the set side of the Flag Buffer FF. The high signal from the output of the Flag Buffer FF, pin 6 of MC27A, gated with ENF through MC12D will set the Flag FF. The high set signal from MC12C, pin 11, is then gated with T4T5 as an input to the reset side of the Transfer Enable FF which turns DMA off.

6-112. The operator can also decide upon using the "Wait for Flag Method" of data transfer rather than the "Interrupt Method" of data transfer. This allows a fast data transfer using DMA without other computer operations. The interrupt system is disabled by a CLF00 instruction which resets the Flag Buffer and Flag Flip-Flops. After the DMA transfer of data, the $\overline{WCR}$ signal will set the Flag Buffer Flip-Flop which, in turn, will set the Flag Flip-Flop. Then the SFS instruction (Skip if Flag Set) allows the next instruction, a JMP, to be skipped by enabling the SKF signal to the computer. Therefore, the computer cannot perform any other operations until the flag is set which allows the total block of data to be transferred before the computer can continue its original program.

6-113. THE UPDATE INTERRUPT SYSTEM.

6-114. There is one more circuit on the DMA schematic, figure 6-18, that should be explained in detail. Figure 6-18 represents an isolation of the Update Interrupt Circuit on the DMA schematic. This consists specifically of the Update Interrupt Address Flip-Flop, MC104A and MC104C, with its external signals that control the flip-flop.

6-115. The Update Interrupt System is turned on only when a phase 4 is in operation and a phase 5 is enabled directly after the present phase 4 cycle. The problem that arises from this situation is the possibility of an interrupt from a higher priority device while the phase 5 cycle is in operation. This is why an update to the interrupt system at the end of the phase 5 cycle is needed. The Update Interrupt System is used to create an XPH4 signal at time T7 of a phase 5 in order to acknowledge the higher priority device interrupt and delay the lower priority device interrupt until the higher priority device has been serviced. To further explain this operation, an enabling of a phase 5 occurs when a SSRQ signal from the Compare CKT of the DMA card is sent to the DMA Cycle Control CKT. This SSRQ signal causes a phase 5 to occur directly after the present cycle.

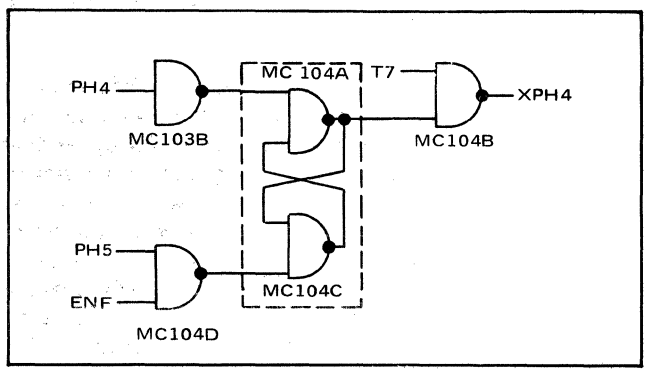


Figure 6-18. Update PH4 Circuitry

6-116. The Update Interrupt System consists of a combination of "nand" gates MC103, MC104 and the "Update Interrupt Address" Flip-Flop MC104 located on the DMA card. The "Update Interrupt Address" Flip-Flop is set from a phase 4 cycle signal and is reset at time T2 (ENF) along with a $\overline{PH5}$ signal. The PH5 signal controls the enabling of the Update Interrupt System.

6-117. During a usual procedure when a Phase 5 is not enabled ($\overline{PH5}$) and a phase 4 is in operation the "Update Interrupt Address" Flip-Flop is set at time T0 of the phase 4 cycle, but is reset at time T2·$\overline{PH5}$ of the next timing cycle to inhibit the Update Interrupt System. Thus, the usual procedure of a phase 1 will occur after a phase 4.

6-118. When a phase 5 is set up during the operation of a phase 4, the phase 5 cycle will occur directly after the completion of the phase 4 cycle. This allows a high PH5 signal and at time T2 (ENF) along with the $\overline{PH5}$ low the "Update Interrupt Address" Flip-Flop remains set enabling the Update Interrupt System during the phase 5 cycle. Therefore, at time T7 during the phase 5 cycle the XPH4 signal is generated allowing an update of the interrupt system.

6-119. The low XPH4 signal is sent to the Timing Generator Card (pin 13) and enables a high PH4 signal (pin 22) through MC17B. This PH4 signal (pin 22) is then routed to the Instruction Decoder Board (pin 50) generating a RSM6-9 signal which is sent to the I/O Control Board to allow the Select Code in the Central Interrupt Register to be strobed onto the T-bus and generating a STM0-5 signal to allow the storing of the select code into the M-Register. The reason there is a need for an update to the M-Register during a phase 5, coming into effect directly after a phase

4, is to make sure that no higher priority device has sent its interrupt signal during that time. If there was not an update interrupt system CKT in the circuitry of the DMA Card and, during a phase 5, there was a higher priority interrupt signal initiated, at the end of a phase 5 the M-Register bits 0-5 would not be updated to the Select Code of the higher priority device. Therefore, the interrupt system would be acknowledging the higher priority device but servicing the lower priority device forcing a loss of our higher interrupt. The update interrupt system prevents this mix up by correcting the M-Register bits 0-5, the select code bits, to the higher priority select code. This would allow the interrupt system to acknowledge as well as service the higher priority device.

6-120. DMA TROUBLESHOOTING.

6-121. Troubleshooting the DMA option is accomplished by performing the diagnostic tests that are contained within the HP 12607A DMA Accessory Kit. The HP 20524A (or later) DMA Binary Diagnostic Tape and the HP 20525A (or later) DMA Binary Rate and Transfer Diagnostic Tape are the two tapes that thoroughly check the operation of the DMA option in the HP 2114B.

6-122. The DMA Diagnostic Program checks the operation of the interrupt logic on the DMA card, tests the Word Count Register for all numbers, checks the Word Count Rollover, tests the Memory Address Register operation, tests the STC and CLC decision Flip-Flops, tests the DMA data output capability, tests the DMA data input capability and tests the DMA output/input capability via the teleprinter. The DMA Rate Test Program checks to see if the DMA steals every cycle and transfers data to all of memory. The operating instructions for each of the diagnostic test tapes are given in the Operating and Service 12607A Direct Memory Access Manual.

6-123. Other troubleshooting hints are:

a. The use of short "toggle in" programs that will transfer data into or out of memory.

b. Tape looping - this allows a constant transfer of tape and interrupts at the end of each block transfer.

6-124. Loop a piece of tape with as much information on it as the technician desires with a piece of clear tape (all one's on tape). Set the looped tape into the tape reader of the teletype or the High Speed Tape Reader. Toggle in the short program that initializes the DMA transfer of data from the reader and turn on the interrupt system (STF00). In the interrupt address (trap cell) there should be a JSB instruction back to the start of the main program that initializes the DMA transfer. This will produce another block transfer and will allow a continuous looping of the tape as data is transferred. Signals from DMA can now be checked since they come up frequently.

6-125. HIGH-SPEED DATA CHANNEL.

6-126. The high speed data channel option has the same capability as the DMA option. The difference between the two is that the high-speed channel card is used with the HP 12595A Multiplexed Input/Output Computer Accessory Kit and a user-designed controller. The multiplexed input/output computer accessory kit allows the computer to interface with the user's controller and to directly address up to 56 different devices from the computer. The addition of the high-speed channel accessory kit makes it possible to have direct high-speed data transfer between the computer and the high-speed devices in the system. Data transfer between the computer and the slower devices can then be accomplished under program control.

6-127. The high-speed channel accessory kit enables the computer to transfer data directly brtween memory and external devices at a rate of 500,000 16-bit words per second in block lengths of 1 to 8192 words. Word transfer time is 2.0 microseconds for a 16-bit word. No character packing hardware is provided on the card; when using byte (eight-bit) oriented devices, character packing and unpacking may be accomplished with software, before or after data transfer.

6-128. The high-speed channel accessory kit can be used for either random or block data transfers. For random data transfers, a memory address must be provided for each 16-bit word transfer. For block data transfers, a starting address in memory must be provided as well as a word count block length. The memory address register on the high-speed channel card is then incremented automatically after each word transfer. The word count register is incremented with each word transfer and supplies an interrupt when the complete block of data has been transferred.

6-129. As in DMA, the high-speed channel card generates a special phase-5 memory cycle to read or write a word directly into or out of the predetermined memory location. During this phase 5 cycle, the high-speed channel card has control of the central processor unit and input/output section of the computer. The card generates the necessary control signals to accomplish the data transfer. A new phase 5 cycle is generated each time a cycle is requested by the user's controller.

6-130. PROGRAMMING THE HIGH-SPEED DATA CHANNEL.

6-131. In order for the high speed data channel card to operate, certain control signals from the user's controller must be present in addition to the program words. In fact, all initialization of the card will be done by the external controller except for actual turn-on which is accomplished by a STC 06,C. The following is a listing of program instructions to which the high-speed channel card will respond:

a. STC 06: Set the control bit to enable interrupts and sets the Transfer Enable flip-flop, which effectively turns on the card.

b. CLC 06: Clears the control bit, which inhibits interrupts. A CLC 06 instruction does not reset the Transfer Enable flip-flop on the card and thus does not inhibit data transfers.

c. STF 06: Sets the flag bit on the card.

d. CLF 06: Clears the flag bit on the card.

e. SFS 06: Causes the next program instruction to be skipped if the flag bit on the card is set.

f. SFC 06: Causes the next program instruction to be skipped if the flag bit on the card is clear.

g. LIA 02 (or LIB 02): Loads the contents of the word count register on the card into the A-register (or B-register) of the computer.

h. MIA 02 (or MIB 02): Merges ("inclusive or") the contents of the word count register on the card with the contents of the A-register (or B-register) of the computer.

i. CLC 00: Resets the Interrupt Channel Control flip-flop and the Transfer Enable flip-flop on the card to prevent the card from generating either an interrupt or a phase 5 cycle.

6-132. FUNCTIONAL DESCRIPTION.

6-133. The high-speed channel accessory kit requires a fifth phase in addition to the basic four-phase capability of the computer. Phase 5 is a special memory cycle that requires one machine timing cycle (T0 through T7). Once initiated by a Request signal from the controller, phase 5 operation is automatic and independent of program control. Each phase 5 cycle permits one input or output word to be exchanged between an external device (tape reader, disc memory, magnetic tape unit, etc.) and computer memory. See figure 6-19.

6-134. Before data transfer begins, the high-speed channel card is initialized for a particular transfer by inputs from the controller. The block length of data to be transferred is loaded into the word count register, and the starting address in computer memory is loaded into the memory address register on the high-speed channel card. The card is also set up for either an input transfer or an output transfer, and the memory address register is set to either count up or count down.

6-135. The high-speed channel card now waits for a Request signal from the controller. The Request signal causes a phase 5 cycle to be generated, suspending the main computer program for at least one machine cycle to achieve data transfer (one 16-bit word per phase 5 cycle). While the program is suspended, the high-speed channel card generates the necessary control signals to achieve data transfer. The select code addressing to the device involved in the transfer must be done by the controller. If the Request signal from the controller is held in a true state, consecutive phase 5 cycles will occur until the complete block of data has been transferred. At the end of the transfer, the word count register generates a Word Count Rollover signal and a normal interrupt to a service subroutine occurs.

6-136. The high-speed channel card may also be used to implement random data transfers between computer memory and input/output devices. For these single-word transfers, an Inhibit Step Word Count Register signal is used to prevent the word count register from counting and generating a Word Count Rollover signal. This prevents the high-speed channel completion interrupt from being generated after each of these random transfers. After all of the random transfers have been accomplished, an interrupt can be requested by the controller and the computer will interrupt to the normal completion subroutine.

6-137. The HP 12595A Multiplexed Input/Output Computer Accessory Kit allows the computer to directly address up to 56 different I/O devices. The addition of the high-speed channel accessory kit makes it possible to have a direct high-speed data transfer between the computer and the high-speed devices in the system. Data transfer between the computer and the slower devices can then be accomplished under program control.

6-138. A detailed circuit description will not be discussed in this manual but can be found in the Operating and Service Manual for the 12616A High-Speed Input/Output Channel Accessory Kit. A general circuit description can be obtained by studying the DMA detailed circuit logic since they are both similar.

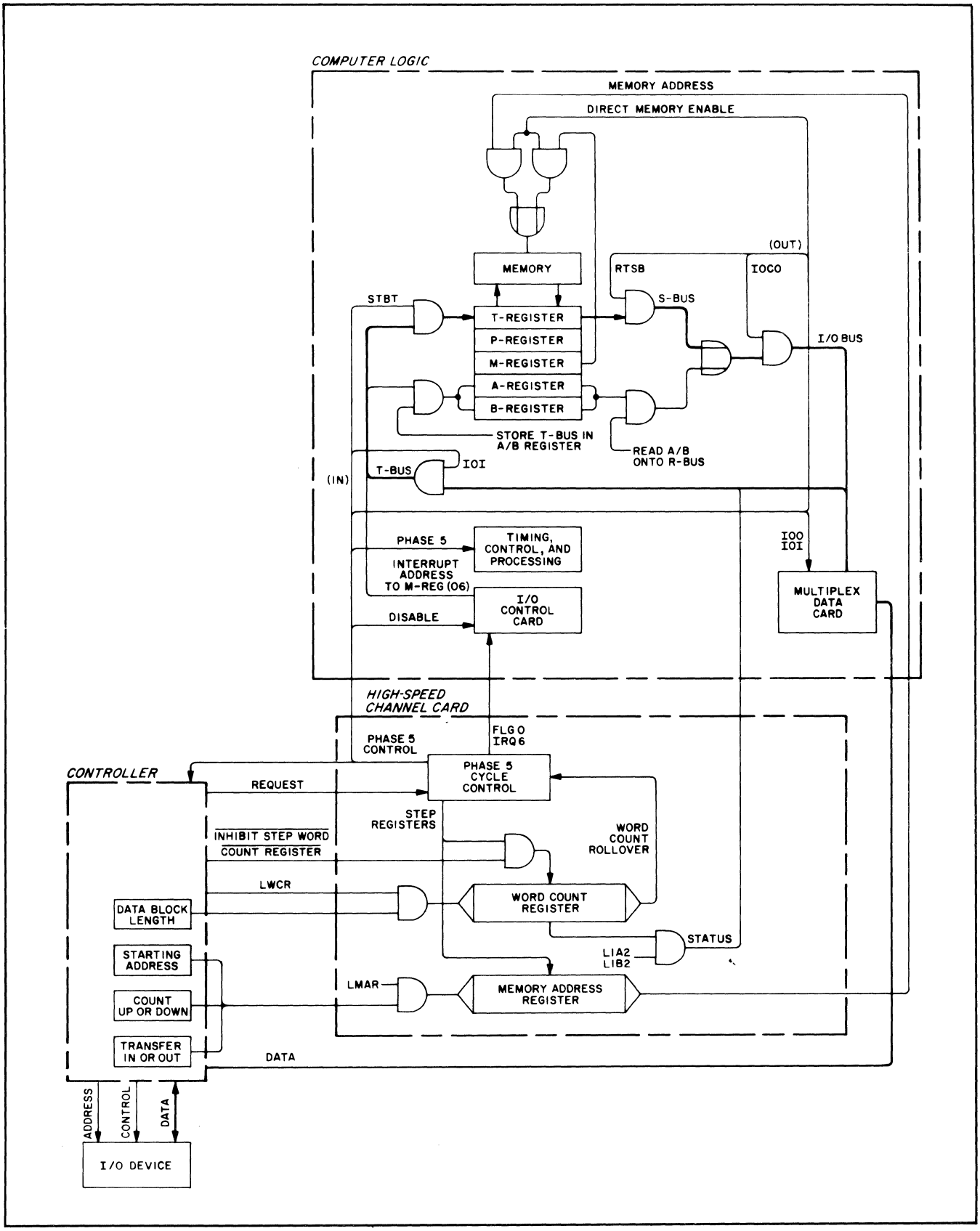


Figure 6-19. High-Speed Channel Card Functional Block Diagram

TROUBLE SHOOTING PROCEDURES

SECTION VII
TROUBLE SHOOTING PROCEDURES

7-1. INTRODUCTION.

7-2. This chapter contains detailed procedures for troubleshooting the HP 2114B. The tools and test equipment recommended for the maintenance, testing, troubleshooting and repair are listed in Table 7-1. Unless otherwise noted, tools or test equipment equivalent to that specified (see critical specifications in Table 7-1) may be substituted. Refer to the special servicing notes below before proceeding.

7-3. SPECIAL SERVICING NOTES.

WARNING

Dangerous voltages are present in the computer even when the Power Switch is in the "OFF" position. Do not attempt to remove the protective cover of the power supply, unless the power cord has first been removed from the power source. Do not energize the Power Supply during servicing unless an isolation transformer is connected between the main power source and J1 at the rear of the Computer. Use caution when making test measurements. Failure to heed this warning could result in death or injury!

7-4. TROUBLESHOOTING AIDS.

7-5. The Operating and Service Manual for the HP 2114B contains diagrams and tables that provide essential data for troubleshooting, maintenance and repair. Included are signal indexes, wiring information, logic equations and schematic diagrams. The scope and purpose of this data is discussed in the paragraphs which follow.

7-6. ABBREVIATIONS AND MNEMONICS.

7-7. The abbreviated terms used in expressing reference designations and electrical values are included in the Operating and Maintenance Manual for the HP 2114B. Signal abbreviations, commonly referred to as mnemonics, are listed and defined in the signal index presented in the Operating Manual. This index lists all signals and supply voltages routed through the connector pins on the plug-in cards installed in the Card Cage Assembly, and the Display Board located behind the Front Panel Assembly. Pertinent reference data for each signal is also included.

7-8. Reference numbers are listed for those signals routed through the sockets on the Backplane Assembly. These numbers (typically 015 associated with signal AAF) provide a cross-reference of numerical order of each mnemonic as it is found in the Backplane Wiring List. By referring to the reference number of each mnemonic in the

Table 7-1. Recommended Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Dual Trace Oscilloscope	Rise time $\leq$ 10 nsec.	HP 180A (HP 1801 vert amp, HP 1820A Time base, HP 10004A probes)
Voltmeter	Accuracy: ± 1% of full scale Input Impedance: 10 Megohms minimum Ranges: ± 1 volt to ± 50 volts	HP 412A, HP 3430A
Multimeter	Accuracy: ± 3% of full scale Range: ± 1 volt to ± 50 volts	HP 427A
Logic Probe*	Indication: logic high $>$ +1.4 volts	HP 10525A
Isolation Transformer	115:115 volt, 800 volt-amp capacity (for 60 Hz operation only, 550 volt-amp capacity will be adequate)	
Variable Autotransformer	50/60 Hz. 7 amp capacity, 115-80 volts metered.	

*Optional.

Backplane Wiring List, complete wiring and interconnection information can be found for each mnemonic.

7-9. Those signals that are routed through interconnecting cables from one section of the computer to another rather than being connected through the Backplane Wiring are designated by asterisks in the reference number column of the Backplane Wiring List. Signals routed between the I/O Control Card A15 and an external device are designated by a single asterisk (*); signals routed between the Core Memory Stack Assembly and associated plug-in cards are designated by a double asterisk (**); signals routed through the Display Board Cable Assembly are designated by a triple asterisk (***).

7-10. The Source Column in the Signal Index Table provides the technician with information as to where this signal is generated and at which pin number this signal can be found on the source. This source is useful as a test point reference, or as a reference to the assembly schematic diagram that provides circuit level coverage for the signal.

7-11. EQUATIONS.

7-12. Logic equations are provided for all signals listed in the Signal Index. Each logic equation is written to indicate input conditions required to produce a given output signal. The equations have been arranged with a minimum of "OR" conditions to facilitate troubleshooting. When a signal is shown with several "OR"ed equations, any one of the given equations can produce the desired signal. The equations are in reduced form and do not necessarily reflect the logic hardware.

7-13. When generating a logic equation for each mnemonic, two operators are used. A "+" is used to indicate a logical "OR" condition. For example C = A + B simply means C is true whenever A or B is true. (The exclusive "OR" condition is not used.) A "*" is used to indicate a logical "AND" condition. For example C = A * B simply means that in order for C to be true both A and B have to be true. Consequently, if either A or B were false, C would also be false. When parentheses are used the quantity within the parentheses is treated as a single term. A bar over a quantity is used to represent a logical inverse or negative quantity.

7-14. WIRING DATA.

7-15. Interconnection Diagram — the overall interconnection diagram presented in the Operating Manual shows the relationship and primary interconnections between major computer assemblies. Detailed interconnection and wiring data presented within this section is described below.

7-16. Backplane Wiring List — Wiring data for the plug-in card slots located on the Backplane Assembly are given in Table 6-2 of the Operating and Maintenance Manual for the HP 2114B Computer. This information must be used in conjunction with the schematic drawings to determine signal and power interconnections for the plug-in cards installed in the Card Cage Assembly and the Display Board located behind the Front Panel Assembly.

7-17. The quickest way of tracing a signal either physically or schematically is to determine its reference number either from the pin number indexes (if included on the schematic diagram), or by referring to the Signal Index. Once the reference number has been established, the signal can be found in the Backplane Wiring List by directly going to the reference column on the Backplane Wiring List, which is in numerical order, and finding the reference number corresponding to that mnemonic. For example, assume that the interconnecting or wiring data was needed for the signal AAF. By referring to the mnemonics listing and finding the mnemonic AAF (the mnemonics listing is in alphabetical order) it can be established that 015 is the reference number for the signal AAF. This number says that the signal AAF and all the wiring data pertaining to this signal can be found on line 015 of the Backplane Wiring List.

7-18. From the Backplane Wiring List, Line 015, for the signal AAF the following data is presented:

a. The source of the mnemonic AAF is A14, the Shift Logic Board. This means that the signal AAF is generated on the Shift Logic Board and that the Shift Logic Board is located in slot 14 of the Card Cage Assembly.

b. As specified by numerical entry "14" at the intersection of line 015 and Column A14, the signal AAF is routed through pin 14 of the Shift Logic Board to pin 14 of socket XA14 on the Backplane Assembly.

c. As specified by the numerical entries at the intersection of line 015 with columns A5, A12, and A13, signal AAF is routed from pin 14 of the Shift Logic Card to the pins specified for the Instruction Decoder, Timing Generator Card and the optional Parity Error Card.

d. The signal AAF can be checked on the Backplane at any one of the four socket pins listed on the Backplane Wiring List (XA14-14, XA13-14, XA12-56, or XA5-55), or at a corresponding pin number on any of the four associated plug-in cards (A14-14, A13-14, A12-56, or A5-55). (The Extender Board must be employed to gain access to pins on the plug-in cards.)

e. By referring to the schematic diagram in the Operating and Service Manual for assemblies A5, A12, A13 and A14, signal AAF can be traced to all associated circuit components.

7-19. It should be noted that the Backplane Wiring list is set up in such a manner as to resemble the physical layout of the Backplane and Card Cage. However, signal mnemonics and associated pin numbers are not listed alphanumerically. For this reason, reference numbers are used for locating data, rather than attempting to locate mnemonics or pin numbers at random.

7-20. SCHEMATIC DIAGRAMS.

7-21. Schematic Diagrams are supplied for all electrical assemblies comprising the basic computer, in the HP 2114B Operating and Service Manual. Electrical assemblies or cards such as the Arithmetic Logic Card, A8-A11, or the Sense Amplifiers, A6-A7, are all identical to each other. In other words, the HP 2114B has four identical Arithmetic Logic Cards. If the HP 2114B has 8K of memory the two Sense Amplifier Cards required will be identical. In the given schematics, only one schematic for each set of identical cards is supplied.

7-22. Identical sets of cards in the HP 2114B consist of the following:

a. Two DR/Sw cards

b. Two Inhibit Driver cards (8K memory)

c. Two Sense Amp Cards (8K memory)

d. Four Arithmetic Logic Cards

Note

When using the schematic diagrams, be sure to observe all notes pertaining to the schematic.

7-23. MAINTENANCE AND REPAIR PROCEDURES.

7-24. The maintenance of the HP 2114B is very minimal to ensure proper computer operation. A monthly maintenance is all that is required, consisting of cleaning, inspection, and testing.

7-25. When cleaning the HP 2114B Computer, cleaning the air filters and dusting is all that is required. To clean the air filters (which are located on the rear panel of the computer) simply remove the filters by pulling in on one side of each of the filters to release the plastic hooks which hold them in place. Clean each filter with either an air hose and compressed air, or soapy water. When using soapy water, be sure the filters are completely dry and free of grease before replacing each filter.

7-26. To finish the job of cleaning the HP 2114B Computer, simply dust. Small dust particles may pass through the air filters, and build up inside the computer. Use a small vacuum or a compressed air hose to remove excess dust.

7-27. Inspection of the HP 2114B is very simple also. Visually inspect the mechanical parts of the computer. Dents, scratches or poorly operating controls may indicate damage to the computer. Insulation should be checked for frayed, broken or burnt sections, and should be immediately repaired.

7-28. REPAIR PROCEDURES.

7-29. This section in the chapter on Troubleshooting Procedures provides the technician with testing and repairing information for the HP 2114B. A detailed description of the testing procedures will follow.

7-30. In testing the HP 2114B Computer, a Pretest Checkout and diagnostic test programs should be performed. The pretest checkout should be executed before the diagnostic test programs are performed. This ensures that all operating controls and indicators are functioning properly, that an apparent trouble is not the result of an improper switch setting, and that the computer is capable of storing and executing the diagnostic test programs.

7-31. PRETEST CHECKOUT.

7-32. The Pretest Checkout is a very basic test of the computer operation. This test is performed manually through the operation of the control switches and indicators. Again, this test should be performed before executing the diagnostic test program. Once normal operation has been established from the Pretest Checkout, proceed with the diagnostic testing. The Pretest Checkout procedure is as follows:

7-33. TEST SWITCHES. To begin, there are six switches located on the rear of the front panel assembly on the upper left hand corner. These switches are used to protect memory, simplify diagnostic testing and disable the front panel console. The switches should be set as follows:

MEMORY	– NORM
PHASE	– NORM
INSTRUCTIONS	– NORM
LOADER	– NORM
LAMP TEST	– NORM
LOCK CONSOLE	– NORM

7-34. If these switches are not set in the normal condition, the pretest checkout may give false problem indication to the operator.

7-35. POWER ON. Turn on the power switch which is located on the computer inside the Front Panel Assembly near the lower right hand corner. Press the halt switch if computer comes up in the RUN mode (indicates Power Failure Interrupt with Automatic Restart, OPTION 008, is present). Check the two fans, located on the Rear Panel Assembly, to be sure they are operating normally. Then close the Front Panel door and check for air flow through the exhaust vents located on either side of the HP 2114B cabinet. Once this is checked out normal, proceed to the next step.

7-36. POWER SUPPLY VOLTAGES. On the Rear Panel Assembly of the HP 2114B, there are six supply voltage test jacks readily available to check the condition of each supply voltage generated from the HP 2114B Power Supply. Check these supply voltages and perform adjustments specified in the section on Maintenance Procedures in the Power Supply Chapter. The various supplies and the acceptable ranges for each supply voltage are given in Table 2-1 of the Power Supply section. Any discrepancies between any of the voltages should be repaired at this time.

Refer to the section on the Power Supply for troubleshooting procedures.

7-37. LAMP TEST. Reopen the Front Panel and Set the LAMP TEST switch to TEST. Check that all front panel indicators are lit. If they are, set the LAMP TEST switch to NORMAL, set POWER switch to OFF, and proceed with the next step. If any of the lights do not light, check the bulb location for that light on the back of the Front Panel Assembly for a bad connection. If the connection is good, then change the bulb.

7-38. INDICATOR TEST. Set the power switch to ON, press the HALT switch if the comptuer comes up in the RUN mode. Check that the indicators listed in Table 7-2 are in the state specified. (Indicators other than those listed may either be "ON" or "OFF".) Repeat this step several times, ensuring that the FETCH light is lit everytime. If all indications are normal, proceed to next step. If any problems exist, begin troubleshooting with respect to the HALT CONTROL SWITCH circuit.

Table 7-2. State of Front Panel Indicators After Power Turn-On

INDICATOR	STATE
RUN	Off
HALT	On
FETCH	On
INDIRECT	Off
EXECUTE	Off

7-39. CONSOLE LOCK TEST. Again refer to the test switches on the rear of the Front Panel Assembly and set the Console Lock switch to LOCK position. Go to the Front Panel Control Switches and check each one by pressing it to ensure that each switch is inoperative. The Console Lock switch disengages the +12V bias voltage bus to all control switches and the switch register switches, locking each switch into the state it was in before the Console switch was turned "ON". If any of the switches are not in operating condition, an error is indicated and should be repaired at this time. Begin troubleshooting with respect to the proximity switch that is in operating condition. If more than one switch is operating begin troubleshooting at the CONSOLE LOCK CKT. Both circuits are located on the Front Panel Assembly. Once indication is normal, set the Console Lock switch to NORMAL and proceed to the next step.

7-40. SWITCH REGISTER TEST. Press each Switch Register (also referred to as the S-Register) proximity switch and bring the Register to the condition that all switches are indicating a "true" level or a "1" (all switches are lit). If any indication of error exists, such as the indicators intermittently going "OFF" or "ON" or the Clicker not operating properly, refer to the section on troubleshooting the Front Panel Assembly. If indication is normal press CLEAR REGISTER switch. This should clear the S-Register to all "zero" (all indicators OFF). Check the S-Register display for the indication of 000000_8. If any of the Proximity Switch lights remain lit (one or two lights) an error is indicated. Begin troubleshooting with respect to that Switch Register flip-flop located on the Arithmetic Logic Card. If all lights remain on, begin troubleshooting with respect to the CSR signal generated on the Shift Logic Board (A14). A good troubleshooting procedure for the technician is to exchange identical boards within the computer and determine whether the problem existing follows the exchange. This procedure immediately reduces the problem to one specific card or prevents the technician from being "fooled" by false indications from other sections of the computer. If indication is normal, proceed with the next step.

7-41. LOAD ADDRESS "ZEROS" TEST. Maintain the S-Register with all "zeros" and press LOAD ADDRESS switch. This should load the contents of the Switch Register, all zeros, into the M-Register which is displayed on the Front Panel. The most common failure at this point would be a bit remaining high (in the one condition) in the M-Register or the P-Register. The error in the M-Register can be readily detected from the display of the M-Register on the Front Panel. This error can be directly related to the M-Register Flip-Flop and its associated circuitry. It is located on the Arithmetic Logic Card which correlates to the M-Register bit that is in error. Exchange Arithmetic Logic Cards and repeat this test to ensure that the problem follows the change. The error in the P-Register will not be detected at this point if no REMOTE DISPLAY REGISTER is present because the P-Register bits are not directly displayed on the Front Panel of the HP 2114B. This error will be detected later upon continuation of the Pre-Test Checkout. If indication is normal, proceed to the next step.

7-42. LOAD MEMORY "ONES" TEST. Enter all "ones" into the Switch Register. Press LOAD MEMORY switch. The contents of the Switch Register should have been transferred to the MEMORY DATA REGISTER (T-REGISTER) which is displayed on the Front Panel. The MEMORY ADDRESS Register (M-Register) should have been incremented by one. At this point, if the P-Register had had a bit that was high from the previous test and no REMOTE DISPLAY REGISTER was available to detect the error, it will be detected at this point simply by checking the M-Register display. Under normal conditions, the M-Register is incremented by adding one to the P-Register and storing the contents into both the P- and M-Registers. If the P-Register had one of its bits always high then the M-Register would indicate this error simply by displaying the erroneous bit of data upon transfer of the P-Register +1 to the M-Register. Another error that may occur at this point is the dropping of one of the data bits being transferred from the Switch Register to the T-Register. This will be displayed on the Front Panel in the T-Register display. The technician should begin troubleshooting at the T-Register flip flop corresponding to the erroneous bit located on the Arithmetic Logic Board. (Don't forget to interchange identical boards to ensure that the problem exists on the suspected board.) Repeat the test

several times; if indication is normal, proceed to the next step.

7-43. LOAD ADDRESS "ONES" TEST. Again press the LOAD ADDRESS switch. The M-Register should display all "ones" from bit 0 through bit 13 (037777_8). (Indicators for bits 14 and 15 of the M-Register display are not connected and will remain "off" even when binary "ones" are stored in those positions.) A handy usage for the use of these inoperative bits in the M-Register is to use the lights associated with these bits as replacements to the other lights on the Front Panel. Any other bits in the M-Register that are not lit indicate an error and should be repaired at this time. Begin troubleshooting at the M-Register bit flip-flop located on the Arithmetic Logic Cards. Again, any errors within the P-Register will be present at this time (if the P-Register is dropping a bit), but will not be detected until later on in the Pretest Checkout. The following three steps will detect whether the P-Register is dropping a bit of information, since this error disallows any incrementation of the M-Register past the erroneous bit in the P-Register; i.e., if bit 4 of the P-Register is always low, the M-Register will never be able to increment past bit 4 of the M-Register. If all indications are normal, proceed to the next step.

7-44. LOAD MEMORY "ZEROS" TEST. Press the CLEAR REGISTER, LOAD ADDRESS and LOAD MEMORY switches. This should clear the Switch Register, load all "zeros" into the M-Register (clear the M-Register), load all "zeros" into the T-Register and increment the M-Register by one. If any of the displayed bits on the Front Panel are lit besides bit 0 of the M-Register, an error exists. Repair as explained in paragraph 7-41. If all indications are normal, proceed to the next step.

7-45. LOAD MEMORY SWITCH TEST. Again press LOAD ADDRESS switch. This should CLEAR the M-Register. Press the LOAD MEMORY switch several times. This should increment the M-Register by one each time LOAD MEMORY is depressed. If all indications are normal, proceed to the next step.

7-46. DISPLAY MEMORY TEST. While observing the M-Register display, depress the DISPLAY MEMORY switch. The M-Register should increment by one with each depression of the DISPLAY MEMORY switch. The T-Register will give a random display of information, since the information in each address core is displayed every time the DISPLAY MEMORY switch is depressed. If an error exists, begin troubleshooting at the DML signal generated from the DISPLAY MEMORY switch on the Front Panel. If all indications are normal, proceed to the next step.

7-47. SINGLE CYCLE SWITCH TEST. Going to the test switches on the rear of the front panel, turn the MEMORY switch to "off". Depress SINGLE CYCLE several times and observe the M-Register display on the front panel. The M-Register should increment each time the SINGLE CYCLE switch is depressed. If an error exists, begin troubleshooting at the SCL signal generated from the SINGLE CYCLE switch on the Front Panel. If all indications are normal, proceed to the next step.

7-48. NOP TEST. Set the MEMORY switch on the back of the Front Panel to "off". Clear the S-Register and press LOAD ADDRESS, then press LOAD MEMORY twice in order to clear the A- and B-Registers (the A-Register = memory location 0 and the B-Register = memory location 1).

7-49. Press the RUN switch and check to see if the RUN indicator is on. Then check the T-Register display for an indication of 000000_8, and observe the M-Register display indicators. Each succeeding indicator of this display, viewed from bit 13 to bit 0, should appear progressively brighter. Bit 13 should be changing state at a visible rate and have a flickering appearance; bits 14 and 15 are not used and are always off. At this point, if the P-Register is dropping a bit (refer to paragraph 3-43), and this was not detected in the previous steps, it will be caught at this time. Look at the incrementing of the M-Register. If the M-Register does not increment through the full 13 bits (i.e., increments only through bit 10) then the technician could assume that the P-Register bit 10 is always low. *Exchange the Arithmetic Logic Card* correlating to bit 10 of the M-Register with one of the other three identical boards and determine whether the problem continues following the exchange. Then depress the HALT switch. Ensure that the HALT indicator is on, that the RUN indicator is off, and that all operation on the front panel has terminated. (Each indicator in the M-Register is in a static state, either on or off.) The numeric value of the M-Register display is a random value, but all lights that are on should have the same amount of brightness. If all indications are normal, proceed to the next step.

7-50. ADDRESSABLE A AND B TEST. Load address 000000_8 and set the Switch Register to 000377_8. Depress LOAD MEMORY (location 000000_8 as a memory address actually represents the A-Register; therefore the A-Register will contain 000377_8). The M-Register display should be incremented by one (i.e., M = 000001_8).

7-51. Now set the Switch Register to 177400_8 and depress LOAD MEMORY. The contents of the T-Register should now read 177400_8 (the B-Register is represented by memory address 000001_8; therefore, the B-Register in the HP 2114B will contain 177400_8). The M-Register should increment by one (M = 000002_8).

7-52. Load Address 000000_8 and depress DISPLAY MEMORY; the T-Register should read 000377_8. Depress DISPLAY MEMORY again. The T-Register should display 177400_8.

7-53. Load 102000_8 into the A- and B-Registers (locations 000000_8 and 000001_8 in memory) by clearing the Switch Register and pressing LOAD ADDRESS. Set the switch register to 102000_8 and press LOAD MEMORY twice. Depress RUN. The computer will HALT with the T-Register equalling 102000_8 (the A- and B-Registers will equal 102000_8 also). The M-Register will equal 000001_8. Continue depressing RUN. Each time, the computer will halt with the M-Register displaying the folloiwng sequence:

000002_8
100001_8 } only if remote
100002_8 } display is
000001_8 } available

7-54. If any error exists, the technician should reduce the problem to either the A- or B-Register and begin troubleshooting at the AAF or BAF signal generated on the Shift Logic Board (A14).

7-55. STA TEST. Setting the MEMORY TEST SWITCH in the "off" position, set all registers to 000000 (Clear Switch Register, load ADDRESS, load MEMORY (twice), and load ADDRESS). Then load 070001 into the A-Register (location 000000). To do this, hold the HALT switch down and press LOAD MEMORY (this procedure will load the information, but will not increment the M-Register). Note the status of the EXTEND and OVERFLOW registers. The FETCH light should be on.

7-56. Depress SINGLE CYCLE and the indicators shall be:

T 070001
M 000001
EXTEND . . . . . UNCHANGED
OVERFLOW . . . . . UNCHANGED
FETCH . . . . . .OFF
INDIRECT . . . . . .OFF
EXECUTE . . . . . ON
PARITY . . . . . .OFF

7-57. Depress SINGLE CYCLE once again. The Indicators shall be:

T 070001
M 000001
EXTEND . . . . . UNCHANGED
OVERFLOW . . . . . UNCHANGED
FETCH . . . . . ON
INDIRECT . . . . . .OFF
EXECUTE . . . . . .OFF
PARITY . . . . . .OFF

7-58. EXTEND AND INDIRECT INDICATOR TEST. Set the M-Register to 000000_8 (clear Switch Register and press LOAD ADDRESS). Load 002200_8 into location 000000_8 (the A-Register) by pressing HALT down and the LOAD MEMORY Switch simultaneously. Then set the INSTRUCTION TEST Switch to LOOP (on the rear of the front panel) and depress SINGLE CYCLE several times. The EXTEND indicator shall alternately light and extinguish. If it does not light and extinguish, there is a problem within the computer which should be repaired at this time. Once indication is normal, proceed with the next step.

7-59. Set the INSTRUCTION switch to NORMAL and load 164000_8 into location 000000_8 (the A-Register) by putting 164000_8 into the Switch Register, holding HALT down and pressing LOAD MEMORY. Then depress SINGLE CYCLE once and check the INDIRECT indicator. The INDIRECT indicator should be on.

7-60. MEMORY TEST. Return the MEMORY TEST switch back to normal and check the +5V (Primary Regulator) to +5V ± 0.10V and the +20V (Memory Supply) to 19.5V ± 0.2V. The adjustments are covered in the section on Troubleshooting the Power Supply. Once the supply voltages are satisfactorily adjusted, the actual testing of memory can take place.

7-61. Set the LOAD switch to ENABLE and set all Registers to 000000_8. Load 070000_8 into location 000000_8 (Switch Register to 070000_8). Hold HALT down so the M-Register will not increment. Press LOAD MEMORY. Depress SINGLE CYCLE in order to begin execution of this STORE instruction. Depressing the SINGLE CYCLE switch will cause the EXECUTE indicator to go on, and move the computer into its next phase of operation, the EXECUTE PHASE.

7-62. Set the PHASE TEST switch to LOOP and load 177777_8 into the Switch Register. Press LOAD MEMORY to load the A-Register and then RUN. The HP 2114B will continue to run with all lamps on in the T-Register, indicating that the 177777_8 is being stored in all memory locations. Press HALT.

7-63. Check each 4K module in memory to ensure all "one"s have been stored in each location in memory. First, load address 000000_8 (set the switch register to 000000_8 and press LOAD ADDRESS) and press DISPLAY MEMORY several times. Now, randomly load address throughout the lower 4K module and press DISPLAY MEMORY; start at address 000100_8 (bit 6 = 1) and check the "hundreds" locations (100_8, 200_8, etc.) by displaying a few locations in each set, then progress to the "thousands" locations (1000_8, 2000_8, etc.) and so on throughout the lower 4K module. This procedure will check the lower 4K module in memory and memory cards corresponding to the lower 4K module. All "ones" should be displayed in the T-Register each time DISPLAY MEMORY is pressed; any other indication implies an error and should be corrected immediately. The usual error indication is one of the lights on the T-Register going out. This is due to a bit of information being dropped from each displayed address.

7-64. The memory cards corresponding to the lower 4K module of core are the two Driver/Switch cards, (located in slots A1 and A2), one sense Amplifier (located in slot A6), and one Inhibit Driver (located in Slot A3). An error detected upon execution of this test usually indicates a hardware problem corresponding to one of these cards. If 8K of memory is present there will be a total of six memory cards, an additional Sense Amplifier (located in Slot A7) and an additional Inhibit Driver (located in Slot A4). The upper 4K module should be checked in the same fashion as the lower 4K module. (Load address 001000_8 and press DISPLAY MEMORY several times, etc.) If any type of error is detected it can be reduced to the memory cards corresponding to the upper 4K module, the two Driver Switch Boards (located in Slot A1 and Slot A2), the additional Sense Amplifier (located in Slot A7), and the additional Inhibit Driver (located in slot A4).

7-65. If the HP 2114B has 8K of memory the problem can be reduced to a certain card within the memory section by analyzing the problem first and then actually switching the identical cards associated with the 8K module. These are:

two identical Dr/Sw Boards
two identical Inhibit Dr. Boards
two identical Sense Amp Boards

Determine whether the problem is common to both the upper and lower 4K module or is isolated to one specific 4K module. A problem to both the upper and lower 4K modules indicates the problem corresponds to one of the two Driver/Switch Boards since they are the only memory boards that are common to both modules. A problem that corresponds specifically to the lower 4K module indicates a hardware problem with either the I.D. 0 (in slot A3) or the S.A. 0 (in slot A6). A problem that corresponds specifically to the upper 4K module indicates a hardware problem with either the I.D. 1 (in slot A4) or the S.A. 1 (in slot A7).

7-66. Once the technician has analyzed and reduced the problem to a specific section of memory the actual troubleshooting procedure can begin. If the technician has reduced the problem to the Dr/Sw Boards, he may be able to reduce it even further to the actual board. The X DR/SW Board represents bits 0-5 of the M-Register and the Y DR/SW Board represents bits 6-11 of the M-Register. If problems arise with actual memory addressing, it should be determined whether the difficulty corresponds to addressing bits 6-11 or addressing bits 0-5, thereby narrowing the problem to one of the two DR/SW Boards. Once the technician has assumed he has reduced his problem to one specific DR/SW card, exchange the two cards and ensure that the problem follows with the change. If the technician does not exchange the cards and relies upon his assumptions he may find himself chasing false indications caused from other sections of the computer.

7-67. If the hardware problem is reduced to one specific 4K module the technician has then reduced the problem to one of the Sense Amplifiers or one of the Inhibit Drivers. The most common failures that will be detected with respect to each 4K module will be a dropping of a bit of information or a picking up of a bit of information which can be detected by storing all "ones" into memory or by storing all "zeros" into memory. The technician has no real way of determining whether the problem is due to the Inhibit Driver or the Sense Amplifier, but there are a couple of hints the technician can follow. If the problem within memory is picking up a bit, the technician can begin his troubleshooting procedures with the Inhibit Drivers (switch the two Inhibit Drivers and determine if the problem followed the switch from upper to lower 4K or vice-versa). If the problem within memory is dropping a bit, the technician can begin his troubleshooting procedures with the Sense Amplifiers (again switching the Sense Amplifier boards and determining if the problem follows the switch from upper to lower 4K or vice-versa).

7-68. Store all "zeros" into memory by following the same procedure as to store all "ones" into memory except after setting the PHASE SWITCH to LOOP load 000000_8 into the Switch Register, press LOAD MEMORY and RUN. The HP 2114B continues to RUN with all lamps in the T-Register display indicating that 000000_8 is being stored in all memory locations. Press HALT and continue the checking procedure of memory as indicated when the storing of "ones" into memory was executed.

7-69. Set the PHASE switch to NORMAL and the MEMORY Switch to OFF (on rear of Front Panel). Set all the Registers to 000000_8 and press DISPLAY MEMORY. The M-Register will increment by one each time DISPLAY MEMORY is pressed. The T-Register shall remain 000000_8 since the MEMORY switch was turned off. (If the A- and B-Registers were not cleared, the T-Register would display "ones" for these two locations.) If indication was normal, proceed with the next step.

7-70. Set all the Registers to 000000_8 (press LOAD ADDRESS) and set the MEMORY switch to NORM and the INSTRUCTION switch to LOOP. Load 064002 into location 000000_8 (A-Register) and press RUN. The HP 2114B shall continue to RUN with both the FETCH and EXECUTE lit dimly.

7-71. If the Parity Error option is present, pull the hood connector from the Sense Amplifier A6. The HP 2114B will halt with the PARITY indicator lit. Press the PRESET switch and the PARITY light should go out. Once this is accomplished, replace the hood to the Sense Amplifier and set the INSTRUCTION switch back to NORM.

7-72. MEMORY ADDRESS TEST. The last test of the Pre-Test Checkout procedure is the Memory Address Test. This test consists of eighteen instructions that test each location in memory for correct operation. These eighteen instructions simply load each core location in memory with its own address, reads the information back out and compares the "Read-Out" information with the original information stored. If the information does not compare, the computer will halt and will indicate an address error. This memory address test gives a thorough check-out of the Memory cards, as well as the actual core stack:

2 — Dr/Sw Cards
1 — Sense Amplifier
1 — Inhibit Driver

Note

There are one sense amp and one Inhibit Driver for each 4K machine; therefore, if the HP 2114B was an 8K machine, there would be two Sense Amps and two Inhibit Driver cards.

7-73. The Memory Address Test is as follows (set Loader Switch to Enable):

	LOCATION	OCTAL CODE	ASSEMBLY LANGUAGE
	00002	006204	INB, CME
	00003	060023	LDA FRST
CMPAR	00004	150000	CPA 0,I
	00005	002001	RSS
	00006	102000	HLT
	00007	052022	CPA LAST
	00010	024014	JMP START
	00011	002004	INA
	00012	024004	JMP CMPAR
	00013	000000	NOP
START	00014	060023	LDA FRST
STORE	00015	170000	STA 0,I
	00016	050022	JMP CMPAR-2
	00017	024002	CPA LAST
	00020	002004	INA
	00021	024015	JMP STORE
LAST	*00022	007777	OCT 7777
FRST	00023	000024	OCT 00024

Starting Address is 00014

*Note

For 8K machines (22) 017777 press Preset and RUN. The HP 2114B will run. If it halts, there is an address error. The Extend bit should blink on and off. Once this test has been performed to satisfaction, the Pre-Test Checkout of the HP 2114B has been completed and the computer can now be loaded with the HP Diagnostic Test Tapes. The loading of these test tapes will be covered in the following paragraphs of this section.

7-74. THE BASIC BINARY LOADER.

7-75. When introducing newcomers to the HP Computer Family (which consists of the HP 2116B, HP 2115A, and HP 2114B) the question of entering information into each computer arises. There are two means of entering information into the computer: through the switch register, or through input/output devices.

7-76. The first method (entering information into the computer from the Switch Register) is handy because it allows entering small diagnostic programs directly into the computer (5 to 10 instructions). Once the programs begin to expand to a longer length, the disadvantage of entering data through the switch register becomes evident. This method becomes long and tedious and causes the probability of error to increase. Therefore, the method of entering information into the computer through high speed data input devices was developed.

7-77. It will be assumed that the student who is reading this material has had the 3-1/2 days of Introductory Programming associated with this class or another class that is comparable. There are two types of programs associated with standard Hewlett-Packard software. These programs are classified as either absolute programs (which have a specified starting address) or relocatable programs (which are loaded into memory at a random starting address established through specified software). (No further explanation of HP software will be stressed at this time since it is assumed that the reader has a basic idea of its make-up.) The standard software that the technician will be mainly concerned with are the HP standard diagnostic test tapes which are *absolute* tapes that allow for testing of the hardware in an HP Computer.

7-78. The loading of any absolute binary tape is done through programming means; there is a certain programmed tape that is loaded into the computer by means of a short "toggle in" program that allows the loading specifically of absolute tapes. This HP standard tape is called the BASIC BINARY LOADER.

7-79. The Basic Binary Loader loads absolute programs produced by the Assembler or the Basic Control System absolute output option. It is also used to load standard software systems that are in absolute form (e.g., FORTRAN, ALGOL, Assembler, Basic Control System, and Symbolic Editor). Familiarity with the Basic Binary Loader operating procedures is assumed in the operating procedure for all other software systems.

7-80. The Basic Binary Loader is stored in the protected area of memory (the highest 64_{10} locations). This manual is concerned with the actual loading of the BASIC BINARY LOADER into the HP 2114B Computer. This concern is pointed directly toward the technician and should be used as a guiding feature in the loading of the BASIC BINARY LOADER (also called ABSOLUTE BINARY LOADER (ABL)).

7-81. If the diagnostic test program will not load and you do not get an orderly halt at 102077 it is possible that the Absolute Binary Loader is not loaded properly. This section describes the procedures to reload the Absolute Block Loader in 4K or 8K machines. The procedures for loading the ABL in an 8K machine with the photoreader at select code XX will be given first. This procedure may be modified slightly for 4K machines. XX represents the select code of the input device (tape reader) being used to input the Basic Binary Loader.

7-82. Toggle in the Loader-Loader into memory using the Front Panel Controls:

LOCATION	OCTAL CODE	ASSEMBLY LANGUAGE
00020	1037xx	STC 10, C
00021	1023xx	SFS 10
00022	026021	JMP, 21
00023	1025xx	LIA 10
00024	001727	ALF, ALF
00025	1037xx	STC 10, C
00026	1023xx	SFS 10
00027	026026	JMP 26
00030	1024xx	MIA 10
00031	170001	STA 1, I
00032	006004	INB
00033	026020	JMP 20

a. Load address to 1. Set Switch Register to 077700 and press LOAD MEMORY.

b. Load address to 20.

c. Place 8K Absolute Block Loader tape, 02116-9731, into 2748A. Set 2114B LOADER switch to the ENABLED position.

d. Press RUN. 2114B will read tape and continue running. Press HALT.

e. Protect the LOADER.

Note

The above procedure loads an 8K ABL. For a 4K machine, change the contents of memory location 7772 to 170100.

7-83. A complete listing of the BASIC BINARY LOADER is given in Table 7-3. The "m" and "n" variables that correspond to the following memory size:

m = 0 for 4K memory
= 1 for 8K memory
= 2 for 12K memory
= 3 for 16K memory
n = 7 for 4K memory
= 6 for 8K memory
= 5 for 12K memory
= 4 for 16K memory

Absolute instructions for use with the 2752A Teleprinter (Parallel), or 2748A Punched Tape Reader.

Table 7-3. Basic Binary Loader Listing

ADDRESS	0	1	2	3	4	5	6	7
0m7700:	107700	063770	06501	004010	002400	006020	063771	073736
0m7710:	006401	067773	006006	027717	107700	102077	027700	017762
0m7720:	002003	027712	003104	073774	017762	017753	070001	073775
0m7730:	063775	043772	002040	027751	017753	004400	000000	002101
0m7740:	102000	037775	037774	027730	017753	054000	027711	102011
0m7750:	027700	102055	027700	000000	017762	001727	073776	017762
0m7760:	033776	127753	000000	1037cc	1023cc	027764	1025cc	127762
0m7770:	173775	153775	1n0100	177765	000000	000000	000000	000000

cc = channel number of Punched Tape Reader

7-84. The BASIC BINARY LOADER has to be configured to each computer with respect to the memory size and with respect to the select code location of the input device (either a High Speed Punched Tape Reader or the Teleprinter). The address location should be configured for the upper 64_{10} locations of memory ($0m7700_8$ → $0m7777_8$). Location $0m7772_8$ should be configured with respect to the memory size ($1n0100_8$). Locations 17763_8, 17764_8 and 17766_8 should be configured for the select code of the PHOTO READER or TELEPRINTER ($1037cc_8$, $1023cc_8$ and $1025cc_8$).

7-85. ENTERING CHANGES INTO THE BASIC BINARY LOADER.

7-86. To enter changes into the protected area of memory (the upper 64_{10} locations of memory) proceed as follows:

a. Set LOADER ENABLE switch to ENABLE.

b. Enter address of desired change into S-Register.

c. Press LOAD ADDRESS switch.

d. Press CLEAR REGISTER switch.

e. Enter change into S-Register.

f. Press LOAD MEMORY switch.

g. Repeat steps "b" through "f" for each instruction entered. Then set LOADER ENABLE switch to PROTECT.

7-87. To verify the instructions stored in the protected area of memory, proceed as follows:

a. Enter address of instruction to be verified into S-Register.

b. Press LOAD ADDRESS switch.

c. Set LOADER ENABLE switch to ENABLE.

d. Press DISPLAY MEMORY switch. The contents of the memory location selected in step "a" above is now indicated by the T-Register display. Each time the DISPLAY MEMORY switch is pressed, the contents of the next consecutive memory location are displayed. (Because the M-Register is incremented by one each time the DISPLAY MEMORY switch is pressed, the address indicated by the M-Register display is always one address higher than the address of the data currently displayed by the T-Register indicators.)

e. Set LOADER ENABLE switch to PROTECT after all desired locations in the protected area of memory have been displayed.

7-88. LOADING ABSOLUTE TAPES.

7-89. The HP 2748A Tape Reader and the 2752A Teleprinter are typical input devices that can be used to read program data from the test tapes and transfer it into memory. If the Punched Tape Reader is used, three loading options can be selected. These options, and the entries required in bits 0 and 15 of the Switch Register to select them, are specified in Table 7-4. Procedures for using each input device are presented in the following paragraphs.

7-90. PUNCHED TAPE READER.

7-91. If using the HP 2748A Tape Reader to load the diagnostic program tapes, proceed as follows:

a. At the Tape Reader, set POWER switch to ON.

b. Press LOAD to allow loading of tape.

c. Carefully position program tape to be loaded in the tape reading mechanism and press the READ lever to prepare the Tape Reader to read.

d. At the computer front panel, press CLEAR REGISTER switch.

e. Refer to Table 7-4 and enter the appropriate settings for bits 0 and 15 into the S-Register.

Table 7-4. Punched Tape Reader Loading Options

OPTION	SWITCH REGISTER SETTINGS	
	BIT 15	BIT 0
Load tape	0	0
Verify Checksum without loading	0	1
Compare the contents of the tape with the contents of memory without loading.	1	0/1

f. Press and hold PRESET and LOAD switches, then release both switches. The computer should go into the run mode (RUN indicator on) and the program tape should process through the tape reading mechanism of the Punched Tape Reader. When the computer halts (RUN indicator off, HALT indicator on), check the T-Register indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program loading, refer to Table 7-5.) If indication is normal, proceed with applicable instructions for running the diagnostic test program now in memory. If indication is abnormal, refer to Table 7-5 and proceed as directed.

g. After loading, rewind the tape and return it to the appropriate storage box.

7-92. TELEPRINTER.

7-93. If using the Teleprinter to load the diagnostic program tape, proceed as follows:

a. At the Teleprinter, set LINE/OFF/LOCAL switch to LINE position.

b. Carefully position program tape to be loaded in the Teleprinter tape reader.

c. Set START/STOP/FREE switch to START position.

d. At the Computer front panel, press CLEAR REGISTER switch, then press and hold PRESET and LOAD switches. Release both switches. The computer should go into the run mode (RUN indicator on) and the program tape should process through the tape reader of the Teleprinter. When the computer halts (RUN indicator off; HALT indicator on), check the T-Register indicators. If the test program was correctly loaded into memory, halt instruction 102077 should be displayed. (For an explanation of this and other halts encountered during program

Table 7-5. Loading Halts

MEMORY DATA (T-REGISTER) DISPLAY	EXPLANATION	ACTION
102077	An end-of-tape condition has been detected. Ten consecutive feed frames are interpreted as end-of-tape.	This indication is normal. Proceed with applicable diagnostic test procedure.
102011	Checksum error. The A-Register contains the checksum from the tape; the B-Register contains the computed checksum.	To restart, replace tape in input device and simultaneously press PRESET and LOAD.
102055	Address error. An attempt has been made to destroy the loader or to load outside the memory limits.	To restart, replace tape in input device and simultaneously press PRESET and LOAD.
102000	The Punched Tape Reader compare option has been specified. The tape being read does not compare with memory. The A-Register contains the word from tape which did not agree.	To find the location of the corresponding word in memory, press SINGLE CYCLE twice. The contents of the T-Register minus one is the address of the desired word. To restart after displaying the contents of the address, replace tape in input device, and simultaneously press PRESET and LOAD.

loading, refer to Table 7-5.) If indication is normal proceed with applicable instructions for running the diagnostic test program now in memory. If indication is abnormal, refer to Table 7-5 and proceed as directed.

e. Set the Teleprinter START/STOP/FREE switch to STOP, remove tape, rewind, and return it to the appropriate storage box.

7-94. LOADING HALTS.

7-95. After all program data is read from a test tape and transferred into memory, the associated tape reader and the Computer will halt with a normal indication of 102077_8 (end-of-tape condition) indicated by the T-Register display. This signals the operator to continue with the applicable test instructions for the diagnostic test now stored in memory. If a halt occurs and an indication other than 102077_8 is present in the T-Register display, refer to Table 7-5 and proceed as directed.

7-96. THE LONG DIAGNOSTIC.

7-97. The Long Diagnostic Test Tape is simply a combined tape of 5 basic tests that are used to test the computer hardware.

Note

This tape is used for training purposes only; therefore it is not a part of the standard Hewlett-Packard software and is not available for purchase by the customer.

7-98. The tests that are executed are as follows, where tests 4, 5 and 6 are executed on both upper and lower portions of memory:

NUMBER	TEST	TIMES RUN
1	ASG Test	1000
2	MRG Test	2
3	SRG Test	10,000
4a	Low Memory Address Test	500
5a	Low word bit Checkerboard Ampex Stack	1000
6a	Low word bit Checkerboard Ferroxcube Stack	1000

7-99. If a diagnostic test fails the T-Register contains 1020xx, and the diagnostic that failed can be isolated simply by checking the printout on the Teleprinter. The location of the halt instruction in that diagnostic test will be M-1, where M is the address contained in the M-Register. The instruction that failed is then at address M-2.

7-100. LOADING THE LONG DIAGNOSTIC IN THE HP 2114B.

7-101. To load the Long Diagnostic in the HP 2114B computer, proceed as follows:

a. Load the LONG DIAGNOSTIC control program into the memory of the HP 2114B by placing the tape into the photoreader and pressing the PRESET and LOAD control switches simultaneously. The first portion of the tape will be loaded and the computer will HALT with 102077_8 in the T-Register (do not remove tape from reader).

b. Set contents of A-Register to select code of photoreader and bits 8-11 should be set to select the type of core stack in the machine being tested: Bit 8 = 1 for Ampex 4K stack for HP 2116A; bit 9 = 1 for Cupertino 4K or 8K stack; bit 10 = 1 for Ferroxcube or ISL 4K or 8K stacks; bit 11 = 1 for Ampex 4K or 8K stack. (Clear SWITCH REGISTER. Press LOAD ADDRESS. Set SWITCH REGISTER to select code of PHOTOREADER and the type of core stack. Press LOAD MEMORY.)

c. Set contents of B-Register to teleprinter select code. Set SWITCH REGISTER to the Select Code of the Teleprinter. (If Teletype is a buffered interface card, set the Switch Register bit 15 to 1.) Press LOAD MEMORY.

Note

If there is no teleprinter in the system, set the B-Register to zero and the teleprinter output will be suppressed.

d. Set LOAD ADDRESS to location 15_8. (Set Switch Register to 15_8. Press LOAD ADDRESS.)

e. Press RUN. The computer will enter the data in the A-Register and B-Register and halt at address 20_8 with 102001_8 in the T-Register.

f. Set the contents of the A-Register to the upper boundary of available core (i.e., 007677_8 for 4K or 017677_8 for 8K).

g. Load Address to 20_8.

h. Set the Switch Register to 077777_8.

i. Press RUN. The computer will load and execute each diagnostic in turn. At the end of the programs, the 2114B will type END OF TAPE and HALT.

Note

Any HALT before END OF TAPE is an error except as noted below.

7-102. A brief description of each test that is being executed in the LONG DIAGNOSTIC follows:

7-103. ALTER-SKIP GROUP DIAGNOSTIC. This program is a reliability test of all legitimate code combinations in the Alter-Skip Group. The codes are tested using both the A and B-Registers, rendering a total of 2048 legitimate combinations. This test should be used as the initial reliability test to be executed. If successful, more advanced reliability and diagnostic programs should be attempted. This test does not use any memory reference instructions during the first execution pass.

7-104. MEMORY REFERENCE GROUP DIAGNOSTIC. This program is a reliability test of the 14 Memory Reference instructions. The instructions are tested utilizing both the A and B-Registers and the E-Register when appropriate. This test should be used only after the Alter-Skip Group test has been successfully executed. This test uses Alter-Skip type instructions during the testing of memory reference instruction codes.

7-105. SHIFT/ROTATE GROUP TEST. This is a test of all legitimate code combinations in the Shift/Rotate Group, and the instructions used to control and sense the overflow logic. The codes are tested utilizing both the A and B-Registers, rendering a total of 612 legitimate and meaningful combinations. This test should be used only after the Alter-Skip group tests and the Memory Reference instruction tests have been successfully executed. This test uses Alter-Skip type and Memory Reference type instructions to execute the SRG combination.

7-106. MEMORY ADDRESS TEST. The Memory Address Test will allow a test to be conducted of the Memory Address register and a specified section of the core. The program is divided into two main sections. The first section loads the core and the second section reads back what has been deposited in memory and tested for errors. If an error is detected, the program will halt with the error in the B-Register and the correct data will be in the A-Register.

7-107. MEMORY CHECKERBOARD TEST. The Memory Checkerboard Program tests the core memory for failures while loading an alternating pattern of all ones or zeros, and then reading it back and checking for errors. If an error occurs, the computer will halt on the address of the error.

7-108. SPECIFIC PROBLEMS DEALING WITH THE BASIC BINARY LOADER AND THE LOADING OF ABSOLUTE TAPES.

7-109. During initial contact with hardware problems in the HP 2114B the technician may find that the loading of the Basic Binary Loader or the loading of an Absolute Binary Tape through the loader can not be performed. In many cases the new technician will go through a period of time where he will be lost as to what to do next. Stop and THINK!

7-110. "Why can't I load the Basic Binary Loader?" or "Why can't I load an Absolute Tape?" states the technician. He should determine whether the computer is not loading the Basic Binary Loader because of a failure in his LOADER-LOADER PROGRAM or the computer is not loading the absolute tape through the loader because of a failure in the Basic Binary Loader.

7-111. If the problem at hand prohibits the Loading of the Basic Binary Loader (refer to the section on the Basic Binary Loader), the technician should recheck the contents of the LOADER-LOADER program. If the contents of the LOADER-LOADER program is correct begin to single cycle through the program and determine what part of the program or what instruction is failing and repair the failure.

7-112. The same type of procedure should be followed when an absolute tape will not load with respect to the Basic Binary Loader. Reload the ABL and try to load the tape again. If this fails then begin Single Cycling through the Basic Binary Loader and determine where the failure occurs in the program and repair the failure. This type of troubleshooting procedure becomes very beneficial to the technician since "most of the time" it will reduce the problem to one specific problem to repair. Therefore, if the technician will become familiar with the operation of the LOADER-LOADER and the BASIC BINARY LOADER the problems pertaining to these programs can be reduced promptly.

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