HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

2114A/2114B COMPUTER OPTION 008

POWER FAILURE INTERRUPT
WITH
AUTOMATIC RESTART

Note

This manual should be retained with Volume Two of the Hewlett-Packard computer system documentation.

02114-90394

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Printed: OCT 1970

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GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual contains basic operation and service information for the Power Failure Interrupt With Automatic Restart Option 008 for the HP 2114A or 2114B Computer. Theory of operation information for the option is given in section II, programming information is given in section III, and maintenance information is given in section IV. This manual should be retained with Volume Two of the HP 2114A/B Computer system documentation.

1-3. GENERAL DESCRIPTION.

1-4. The power failure interrupt with automatic restart option allows the computer to interrupt to a power failure subroutine in the event of a power failure. The subroutine enables the user to save the contents of all computer registers; the contents of these registers would normally be lost during a power failure. The restart capability of the option allows the computer to continue executing the user's program as soon as power is restored.

Note

If this option is used without a power failure subroutine, refer to paragraph 3-7 before operating the computer.

SECTION II
THEORY OF OPERATION

2-1. GENERAL.

2-2. When a power failure occurs, the PWF (Power Fail) signal generated by the power fail detect circuits in the computer power supply, goes false. This causes the power failure interrupt circuitry, located on the I/O control card of the computer, to interrupt to location 04 where the entry point to a power failure subroutine is stored. The power failure interrupt uses the highest priority interrupt channel and while it is being serviced may not be interrupted by any other channel. The subroutine performs an orderly shutdown, saving the contents of all computer registers. The PON (Power On) signal goes false after a delay long enough to allow completion of the power failure subroutine. When the PON signal becomes false, it completes the computer shutdown by effectively turning off memory and resetting the Run FFs on the timing generator (STG) card.

2-3. When power is restored, the PON signal is delayed in going true. The initially false PON signal causes the computer to again interrupt to the power failure subroutine. This time a restart procedure is executed and all registers are restored to the state they were in at the time of the initial power failure interrupt. During the restart procedure, the power failure subroutine also returns control to the instruction in the user program that was to be executed at the time of the power failure interrupt.

2-4. POWER FAILURE DETECTION.

2-5. Power failure detection for the option is performed by the power fail detect circuit on the regulator card, part no. 02114-6010, in the computer power supply. (Refer to the power supply assembly schematic diagram in Volume Two.) The detection circuit monitors the ac voltage on the 12-volt secondary winding of power transformer T1. When the rectified ac voltage level across capacitor C72 drops below about 8.2 volts, the resistance of diode CR54 increases, causing the voltage across resistor R43 to drop. The output of "nand" gate MC2C goes true and the output of "nand" gate MC2D goes false, making the input to "nand" gate MC2B false. Gate MC2B gives a true input to "nand" gate MC2A, causing the PWF signal to go false. The false PWF signal causes the I/O control card to generate the initial power failure interrupt. (A similar process could be used to generate a false XPF (External Power Fail) signal from an external or extender power supply. The use of the XPF signal would allow the user to utilize the power failure subroutine in the event of a power failure in an external power source.)

2-6. POWER RESTORATION. When the power supply voltage returns to a normal level, the voltage across capacitor C72 increases until it is again above 8.2 volts. The process described in Paragraph 2-5 is thus reversed. Transistors Q23 and Q24, and the RC circuit (R47 and C75) provide a turn-on delay in the PWF signal. The input to pin 5 of MC2B is held false for about 300 milliseconds after power is restored. After this delay the PWF signal is allowed to go true. The true PWF signal causes a second interrupt to be generated by the I/O control card to begin the restart function of the power failure subroutine and the resumption of the main program at the point of power failure interrupt.

2-7. POWER FAILURE THRESHOLD. Variable resistor R42 provides adjustment of the threshold level for power failure detection. This adjustment is made at the factory prior to shipment of the computer and no further adjustment should be required. If adjustment becomes necessary refer to the adjustment procedures in paragraph 4-3.

2-8. PON SIGNAL. Refer to the I/O control card logic diagram in Volume Three. The PON (Power On) signal is generated on the I/O control card by the PWF signal. When the PWF signal becomes false, indicating a power failure, the PON signal remains true for about two milliseconds. This delay is provided by capacitor C52, resistor R32, and the associated delay network. This delay allows the computer time to execute the power fail subroutine and perform an orderly shutdown. When the PWF signal goes false, transistor Q2 stops conducting; Q3 conducts, causing the voltage on the base of Q4 to drop. Transistor Q4 stops conducting, turning on Q5. The voltage on the base of Q6 drops and Q6 stops conducting. The emitter voltage of Q6 drops, causing a false PON signal. When PON goes false, computer memory is turned off by the driver switch card circuits. The Run FFs on the timing generator card are then reset. As long as the PON signal is false, the Run FFs remain in the reset state.

2-9. When power is restored, the PON signal remains false long enough to reset the Arm, Direction, and Flag FFs, and to set the Control FF in the power fail interrupt circuit on the I/O control card. This initializes the interrupt circuits so that a second interrupt to the power failure subroutine may be made. The PON signal, together with the set Flag and Direction FFs, causes the RSP signal to go false (resulting in a true Restart Pulse signal), restarting the computer.

2-10. INTERRUPT GENERATION.

2-11. INTERRUPT. The Control FF on the I/O control card (figure 2-1) is initially set by the false PON signal when the computer is turned on. When a power failure occurs, the Arm FF resets at the beginning of time T1 following the true-to-false transition of the PWF signal (or XPF signal). At the end of time T1, the false set-side output of the Arm FF is clocked into the Direction FF, causing it to reset. (The output of the Direction FF indicates the direction of the power change; a true set-side output indicates a proper power level, while a true reset-side output indicates an improper power level.) The true output of the Control FF, together with the inverted set-side output of the Direction FF, sets the Flag FF. (The Flag FF receives a clock pulse only when the Arm and Direction FFs are in opposite states.) The reset-side output of the Flag FF then resets the Control FF causing the PRL 4 (Priority Low 4) signal to go false, preventing any other channels from interrupting the computer.

2-12. IRQ SIGNAL. At time T5, the set Flag FF sets the IRQ FF, generating an interrupt request. The IRQ 4 signal generates an Interrupt (INT) signal and provides the I/O address circuits on the I/O control card with the interrupt address of the power failure subroutine. The interrupt is then processed in the same manner as a normal I/O interrupt.

2-13. SKF SIGNAL. The power failure subroutine is now executed. The first test performed should determine the state of the Direction FF. This is performed with an SFC (Skip if Flag Clear) instruction with a select code of 04. In this case the Direction FF is in the reset state after the initial power failure interrupt. The Direction FF causes an SKF (Skip on Flag) signal to be sent back to the computer. The subroutine then begins its shutdown routine. If power had returned to normal, the Direction FF would be in the set state and an SKF signal would not have been generated. The subroutine would then begin its restart routine (paragraph 2-15).

2-14. SHUTDOWN. If the Direction FF is in the reset state, indicating a power failure, the contents of the various registers should be stored in memory before the computer halts (see paragraph 3-5). At the end of the subroutine a CLC (Clear Control) instruction with a select code of 04 should be used. This causes the Control FF to again be set, allowing the Arm FF to be clocked at each time T1 to monitor the PWF signal. This enables the option's restart capability in the event that power is restored before the PON (Power On) signal goes false (momentary failure).

2-15. RESTART. When a proper power level is restored, the PWF signal again becomes true. This places a true input on the Arm FF. If power is restored before the PON signal goes false, the Arm FF is set at the next time T1. The output of the Arm FF sets the Direction FF at the end of time T1, the interrupt sequence is repeated, and the subroutine again determines the state of the Direction FF. This time the Direction FF sets, indicating that power is returning to a normal level. The subroutine then executes the restart routine. At the end of the subroutine an STC (Set Control) instruction with a select code of 04 should be used to set the Control FF. This allows the option to interrupt if power fails again.

Note

Either an STC 04 or a CLC 04 instruction will set the Control FF. For software compatibility it is suggested that the STC instruction be used only in the restart routine and the CLC instruction be used only in the shutdown routine.

2-16. If power is restored after the PON signal goes false a similar process takes place. The false PON signal sets the Control FF (instead of the programmed CLC or STC 04 instruction) and an interrupt is produced as before.

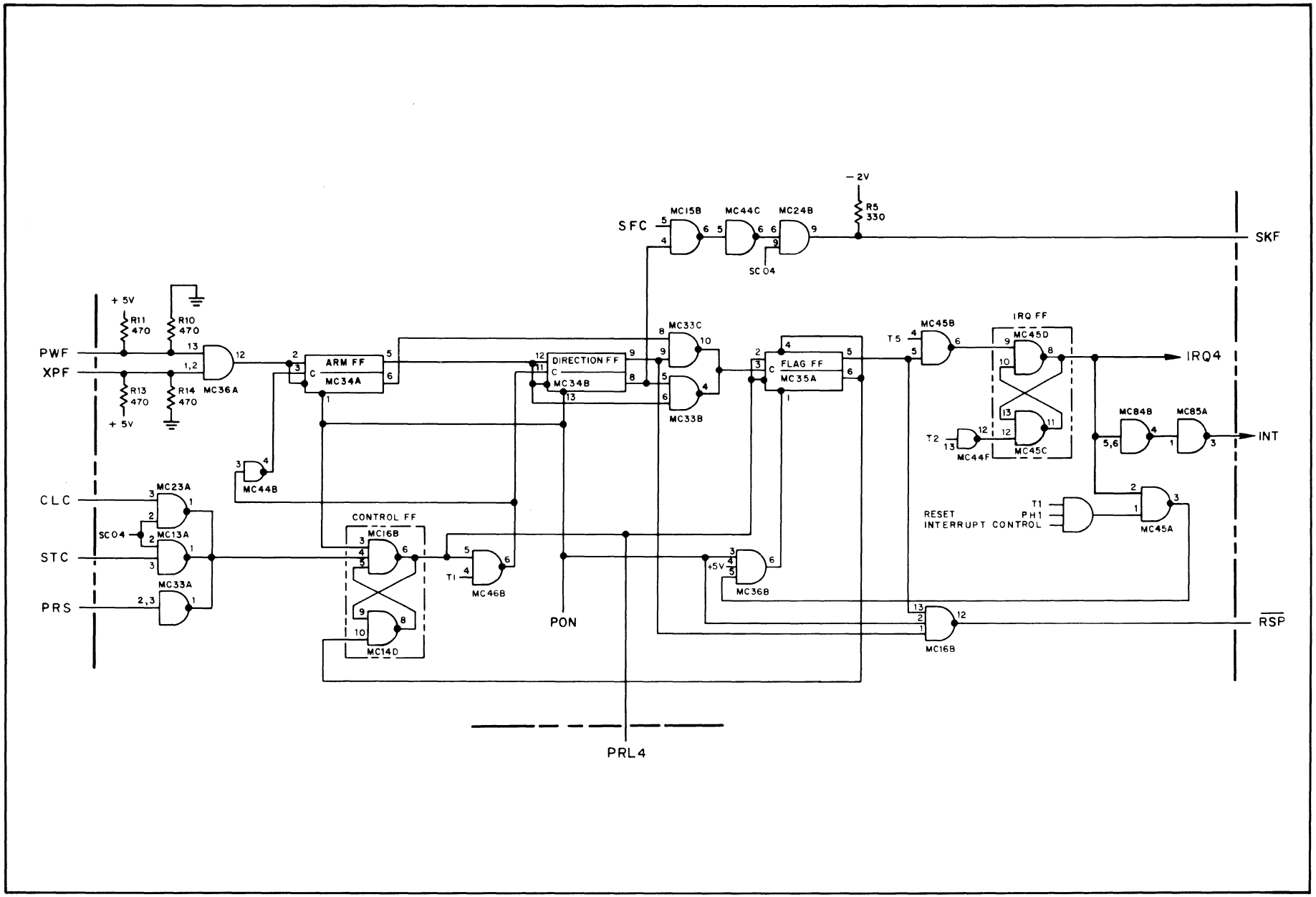

Figure 2-1. Simplified Power Fail Interrupt Circuit

SECTION III
PROGRAMMING

3-1. INTRODUCTION.

3-2. This section contains programming information for option 008. A sample power failure subroutine is provided and described in paragraph 3-3. A minimum power fail program is also provided for use with the option when a subroutine is not used.

3-3. POWER FAILURE SUBROUTINE.

3-4. When an interrupt to location 04 occurs as the result of a power failure the computer executes a JSB (or JSB,I) instruction to a power failure subroutine. If the computer was running when power failed, the subroutine performs an orderly shutdown procedure, saving the contents of the working registers. If the computer was halted at the time the power failed, there is no interrupt. When power returns to a normal operating level the computer interrupts to the power failure subroutine. The subroutine then tests to determine if the computer was running when power failed. If it was, the computer restores the working registers and restarts at the program location at which the first power failure interrupt occurred. If a program was not being executed at the time of power failure, the subroutine returns the computer to the halt condition. Table 3-1 provides a sample power failure subroutine; paragraphs 3-5 and 3-6 provide a description of the sample program.

3-5. SHUTDOWN. The power failure subroutine first checks the status of the Direction FF on the I/O control card. If the FF is set, the subroutine branches to the restart routine. If the FF is reset the subroutine begins the shutdown routine. The contents of the A-register are first stored in memory, making this register available for use by the subroutine. The A-register is next reset and complemented, placing all "ones" in the A-register, and the A-register contents are then stored in memory (SAVR). (The "ones" indicate that the computer was running when the power failure caused an interrupt. This information is used later in the restart section of the subroutine.) The contents of the B-register, the address of the program being executed when the power failure occurred, and the contents of the switch register are also stored in memory. The contents of the overflow, extend, and central interrupt registers may also be stored in memory at this time, as determined by the user. When the desired working information has been stored in memory, the power fail interrupt circuits are set with a CLC 04 instruction to allow an interrupt to occur and restart if power is restored within a short time. The subroutine then halts the computer. It will remain in this state until either the power is restored or the PON signal becomes false, completing shutdown.

3-6. RESTART. When proper power levels are restored, a second interrupt to the power failure subroutine is generated. This time the Direction FF on the I/O control card is set. The SFC 04 test causes the subroutine to begin the restart procedure. The contents of memory location SAVR are tested to determine if the computer was running at the time of the power failure Interrupt. If not, the subroutine places the computer in the halt state. If the computer was executing a program at the time the power failure interrupt occurred, then the contents of SAVR should contain all "ones". The subroutine restores the contents of all registers. When this is completed, the subroutine transfers control through a JMP SAVP,I instruction to the location in the main program where the initial power failure interrupt occurred.

3-7. If a subroutine is not used with the option, a minimum power failure program must include CLC 04 and HLT instructions as follows:

```
0004    JMP    PWF
PWF     CLC    04
        HLT
```

3-8. If the option is used without this minimum program or a power failure subroutine, a power failure could alter information stored in memory.

Table 3-1. Sample Power Failure Interrupt Subroutine

LABEL	OPCODE	OPERAND	COMMENTS
	ORG	4B	
	JSB	PFSR	
PFSR	NOP		POWER FAIL SUBROUTINE.
	SFC	4B	Skip if power is dropping.
	JMP	UP	
DOWN	STA	SAVA	Save contents of A-register.
	CCA		
	STA	SAVR	Signal that computer was running when power failed.
	STB	SAVB	Save contents of B-register.
	LDA	PFSR	
	STA	SAVP	Save contents of P-register.
	LIA	1	
	STA	SAVS	Save contents of S-register.
	.	.	(Execute other desired functions.)
	CLC	4B	
	HLT		Shutdown.
UP	LDA	SAVR	
	CLB		
	STB	SAVR	Indicate that computer is in restart mode.
	SZA	RSS	Test if computer was running when power failed.
	JMP	STOP	
	LDA	SAVS	
	OTA	01	Restore contents of S-register.
	LDA	SAVA	Restore contents of A-register.
	LDB	SAVB	Restore contents of B-register.
	STC	4B	Set up power fail logic for next power failure.
	JMP	SAVP,I	Restore contents of P-register.
STOP	STC	4B	Set up power fail logic for next power failure.
	HLT		Turn off restart mode. The computer was not running when power failed.
SAVA	OCT	0	
SAVB	OCT	0	
SAVP	OCT	0	
SAVR	OCT	0	
	END		

SECTION IV
MAINTENANCE

4-1. ROUTINE MAINTENANCE.

4-2. No routine maintenance of this option is required.

4-3. ADJUSTMENTS.

4-4. EQUIPMENT REQUIRED. The adjustment of the power failure threshold will require the following minimum equipment:

a. A variable, metered ac source (Variac 115 volt, 10 amp or equivalent).

b. A thin-bladed, insulated alignment tool or tuning wand.

4-5. PRELIMINARY SET-UP. Proceed as follows:

a. Turn the computer off by pressing the HALT switch, and then turning off the POWER switch behind the computer front panel.

b. Disconnect the power cord from the ac line source and connect it to a variable, metered ac source.

c. Remove the top cover of the computer by removing the four (4) screws holding it in place.

d. Locate the adjustment hole labeled "POWER FAIL THRESHOLD" on the cover plate of the computer power supply. DO NOT REMOVE THIS PROTECTIVE PLATE.

4-6. ADJUSTMENT PROCEDURE. Proceed as follows.

a. Set the variable ac source to 115 volts and then turn the computer POWER switch on.

b. Load the power failure interrupt with automatic restart diagnostic program. Refer to Diagnostic Program Procedures, part no. 02116-91769, in the Manual of Diagnostics.

c. With an alignment tool slowly rotate variable resistor R42 fully counterclockwise.

d. Load the starting address of the diagnostic program into the switch register. Press the LOAD ADDRESS switch. Press the RUN switch. The test program should begin counting at about two counts per second. The count, starting at zero, is displayed in the switch register.

e. Adjust the variable ac source to 98 volts ± 1%. Rotate variable resistor R42 slowly clockwise until the computer halts. The T-register should contain 102004.

f. Increase the voltage of the ac source until the computer beings executing the test program count. (It should continue the count from the point of interruption.) This should occur before 102 volts is reached. If the computer fails to run, repeat the adjustment procedure. If repeated adjustment fails to correct the problem, follow normal troubleshooting procedures.

4-7. TESTING AND TROUBLESHOOTING.

4-8. To test and troubleshoot this option, perform the Diagnostic Program Procedures, part no. 02116-91769, in the Manual of Diagnostics. To further isolate trouble, refer to the logic diagram of the I/O control card in Volume Three, I/O System Operation.

4-9. REPLACEABLE PARTS.

4-10. Replaceable parts for the I/O control card including the power fail interrupt circuitry are shown with reference designations in Volume Three, I/O System Operation. The part location diagram for the I/O control card including power fail circuitry is also included in Volume Three. Replaceable parts, a parts location view and a power supply logic diagram are contained in Volume Two. Update Volume Two of the 2114A or 2114B Computer system documentation for use with this option by performing the following:

a. In the Signal Index, Table 4-1 or 6-1, respectively: delete A15-83 as a source for the PEH signal.

b. In the Backplane Wiring List, Table 4-2 or 6-2, respectively, for reference numbers 218 and 350: delete the connection to the I/O control card.

4-11. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. Include the HP part number and description.

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