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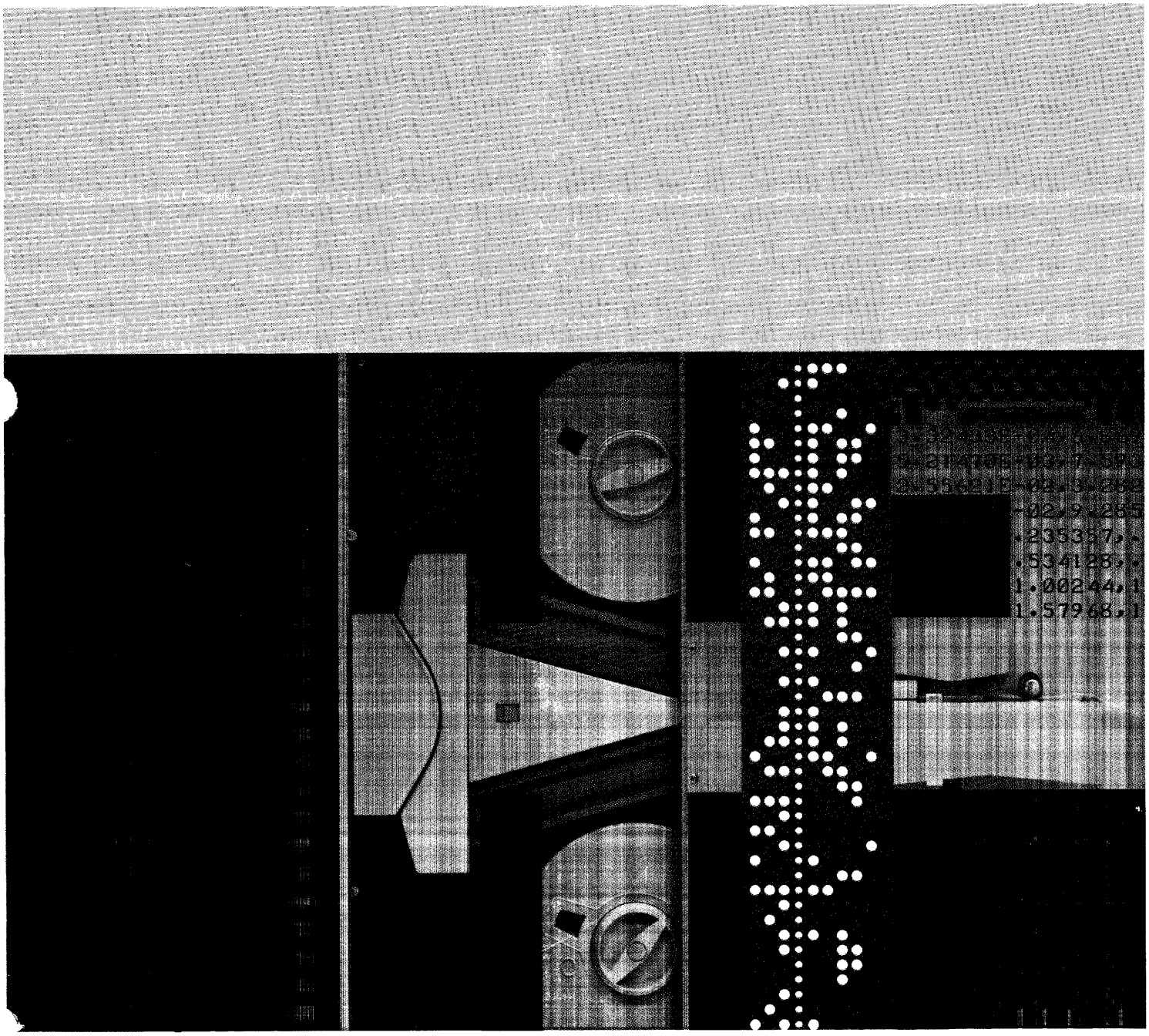

VOLUME XIX

HP TIMESHARE MULTI-PROCESSOR ENVIRONMENT

HEWLETT-PACKARD

COMPUTER MAINTENANCE COURSE

VOLUME XIX

STUDENTS MANUAL

HP TIME SHARE MULTI-PROCESSOR ENVIRONMENT

(HP STOCK NO. 5951-1400)

-NOTICE-

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FOREWORD

The Hewlett Packard family of Time Share Systems includes the 2000A, 2000B and 2000C. The previous manual in this series covered the HP 2000A Time Share System (stock number 5951-1346). It dealt with the philosophy of the Time Share system. Its emphasis was intensively hardware oriented. It dealt particularly with the Scheduler, Multiplexor, and operating environment.

This present volume deals with the multi-processor environment used with the 2000B and 2000C. The addition of the second processor allows a substantial increase in the number of users along with other system improvements.

The purpose of this manual is to describe the operating environment, especially the inter-processor communications and power fail considerations. It gives specific information on the tables and pointers for the 2000B.

There are further changes in the 2000C. These include the drivers and tables required to implement the Moving Head Disc capability. The loading and sleeping technique required significant changes (between 2000B and 2000C). The communications between the system processor and the Communications Processor program is virtually identical. It is hoped that this manual will be helpful for both 2000B and 2000C systems.

It is recommended that the HP 2000A Time Share System manual be available because of the fundamental similarity. References are made to it.

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Multi-Processor Time Share

CHAPTER 1

MULTI-PROCESSOR TIMESHARE

1-1 Multi-Processor Environment

The advantages of dividing the system activities between two processors will be more apparent with a clear understanding of the 2000A system. This training manual relies heavily on the basic system philosophy contained in the HP 2000A Time Share System manual (stock number 5951-1346). References will be made from time-to-time to that volume in the format: HP 2000A TSS Figure # , Page # .

Before proceeding please review the following HP 2000A TSS sections: 1-4 Time Sharing, 1-7 Response Time, 3-1 Multiplexor, 3-2 Multiplexor Software, and Chapter 4 Multiplexor System.

Let us consider the 2000A system from the standpoint of its limitations or weaknesses. The incremental cost of adding more ports (i.e. more than 16) is low from the cost of the hardware required. However, due to core limitations (in the present configuration) it is impossible to exceed the 16 port limit. It would require additional memory space for TTY buffers and TTY tables which is unavailable. Also important is the fundamental change required in status words and flags. The 16 bit machine placed an effective limit at 16 ports without restructuring.

The output buffer was limited to 50 words. Whenever the 100 character output storage was exceeded the Basic Interpreter would initiate an output suspend. This requires a wasted core to drum swap followed by a drum to core swap. Although in the 2000A this limitation was not critical, as one increases the number of ports the wasted time becomes increasingly important. An increase in buffer size would be desirable as the number of ports is increased. The time spent servicing the routine Multiplexor interrupts was significant whenever the number of active ports was high or the quantity of input/output traffic was high.

Finally, although certain desirable user and system features were possible the core limitation absolutely prevented their consideration. The use of a second computer makes possible effective solutions to the system limitations listed above. It also allows the addition of rather important new features.

Two problems arise as a result of the multi-processor environment. One is the power failure techniques and procedures. Another is the communications required to gain access to data available only in the other processor and the initiation of action by the other processor. We will consider these in detail in Sections 3-2 and 3-6.

1-2 2000B Time Share System

Compare Figure 1 2000B Time Share System with the HP 2000A TSS Figure 4 (2000A Time Share System), page 3-3. The comparison will show that the same basic functions exist. They are now merely distributed between the two processors. If the System Processor and Communications Processor computers along with the processor interconnect kits and the communication modules were drawn within a system "black box" these two drawings would be virtually identical.

For the 2000C the main addition to this diagram would be the Moving Head Disc hardware and drivers associated with the System Processor.

The system improvements are now easy to visualize. The 8K memory (in the communications Processor) allows a very substantial increase in TTY buffer size. Each port now has 150 words. This is helpful particularly in output mode in reducing the swapping for output suspensions, and for input while in tape mode. Simultaneous tape input from a large number of ports places a stringent requirement on buffer size. It is satisfied by the 300 character buffer. A glance at the core map (figure 5) indicates the substantial core dedication to these buffers.

In the 2000A a clear functional division existed between the multiplexor and scheduler. The multiplexor indicated a port was ready for service by setting the respective bit in MPCOM. Now this is done through the processor communications by setting a status bit in the System Processor TTY tables. The finished line (in the buffer) was immediately available to the Scheduler or Basic Interpreter. Now the characters are passed as a result of a character request or character output command. A clearer understanding of the TTY tables will result as we see how they were split between the processors with additions and duplications. This manual is based on the listings for the 2000B Revision B. The stock numbers are:

2000B	TSB System	(Rev B)	24239-60001	Part One
			24239-60002	Part Two
2000B	TSB Loader	(Rev B)	24238-60001	
2000B/C	TSB Communications Processor		(Rev A)	24231-60001

Notice the same Communications Processor program is used with both the 2000B and 2000C. A user with the 2000B (Revision A) will find minor difference, especially the new commands IBF and IPF as well as the changes to KAO.

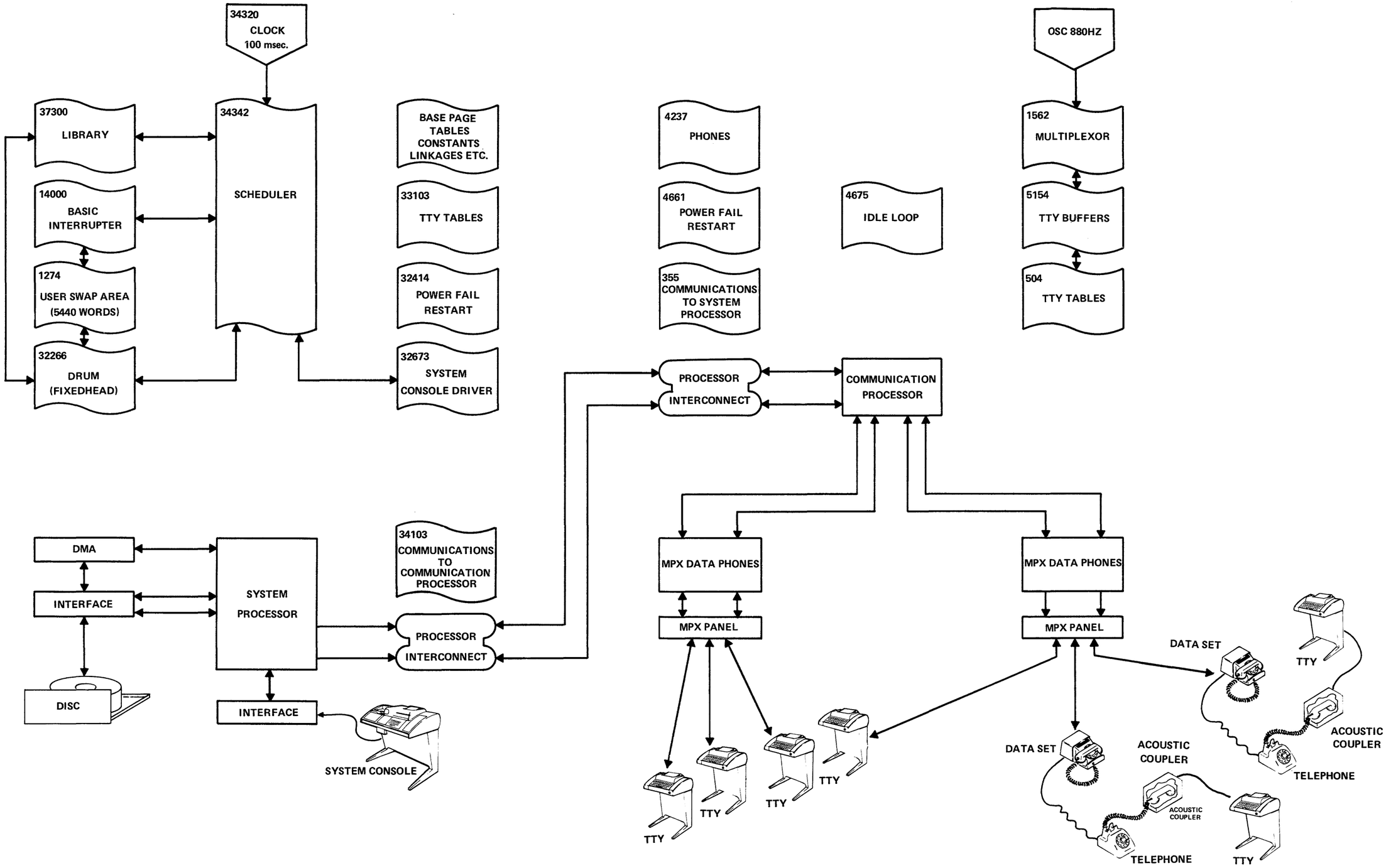


FIGURE 1. 2000B TIME SHARE SYSTEM

Communications Processor Functions

CHAPTER 2

COMMUNICATIONS PROCESSOR FUNCTIONS

The use of the second processor to service the Multiplexor requires certain pointers, tables and software routines. This chapter will consider these requirements. It would be desirable to review chapters 5 and 6 from the HP 2000A TSS Manual.

2-1 Multiplexor Hardware

The Communications Processor provides greatly expanded multiplexor capability. Figure 2 shows the multiplexor data and phone arrangement. Compare with HP 2000A TSS Figure 5 on Page 4-3.

The maximum user capability allows 32 users. These may be hard wired (direct cable) or coupled through data phones.

The minimum system consists of a data board in Select Code 10. This allows up to 16 direct users. If the Data board in Select Code 11 is unnecessary a Priority Jumper must be substituted. Since the processor communications operates under Interrupt, the priority string must be intact.

As the system is expanded to include Phones the Ring Carrier Interface and Phones board must be installed. Notice the relationship between the Data and Phones board. The Phones board in select code 14 is required for users 0 to 15 in conjunction with the data board in select code 10. The Phones board in select code 15 is required for users 16 to 31 in conjunction with the data board in select code 11. Any compatible installation is possible between the minimum or maximum configuration.

Notice that only the first Data board interrupt circuitry is utilized. This one interrupt controls the servicing of all Data and Phones.

A change in the PHOnes command was implemented. The select code is no longer specified. The only parameter required is the log on time limit. Thus PHO-14,180 would be misinterpreted, and would result in a log on time of 14 seconds. An additional change precludes the use of PHO-Ø to turn off the phones. The two possibilities now allow PHO-1 which would ring then disconnect in one second, or manual intervention to turn off the data phone set.

2-2 Multiplexor Software

The 2000A was an example of extremely tight and efficient coding. Core was so valuable that virtually every trade off was resolved with the solution requiring less core. Now with a separate computer dedicated to the user processing and communication tasks, core is more abundant. The trade offs between speed or efficiency vs core requirements can now be resolved at the expense of program size.

If we consider the implications of 32 users we see the availability of 32 bits by using 2 computer words. Now our flag words require 2 addresses. Glance ahead at the locations described in section 2-5. These describe 6 flag functions requiring 12 memory addresses. Review the definitions.

Figure 3 shows the greatly simplified block diagram for the multiplexor routine. The multiplexor routine operates under the interrupt mode. The oscillator on the data board in select code 10 interrupts every 1.134 millisecond. Since this has the highest I/O priority it will override the processor communications if flag Ø is enabled. The multiplexor then ascertains whether any new user input requires servicing. These are set up one at a time. Then the LADDR routine determines whether bit processing is required by any active user. Any such requirement is handled by the MPXIO routine.

The phones routine is entered ten times each second. This is determined by counting 88 multiplexor interrupts.

The multiplexor flag holds off the interrupt from lower priority devices. It also holds a subsequent multiplexor oscillator interrupt in the "storage FF". Thus it will not be lost due to an unusually large amount of multiplexor business during any specific interrupt. The multiplexor flag is cleared as the routine is exited.

It will now be beneficial to review the HP 2000A TSS Chapter 4 Multiplexor System. The Communications Processor Multiplexor technique is quite similar. The apparent differences include the method of signalling user business to the scheduler and the implications of the FAST port command.

For FAST port command a count of -2 is placed in the BTIM table entry instead of the -4 for normal 10 cps terminals. This is shown on HP 2000A TSS Figure 6 on page 4-7 near the right margin. This occurs as the ISZ entry is placed in the LADDR routine. The count between bit processing is also cut in half for the FAST port from -8 to -4. This is shown on HP 2000A TSS Figure 6, page 4-8 near the top. Whenever a bit time out occurs the new value (-8 or -4) is placed in the BTIM entry.

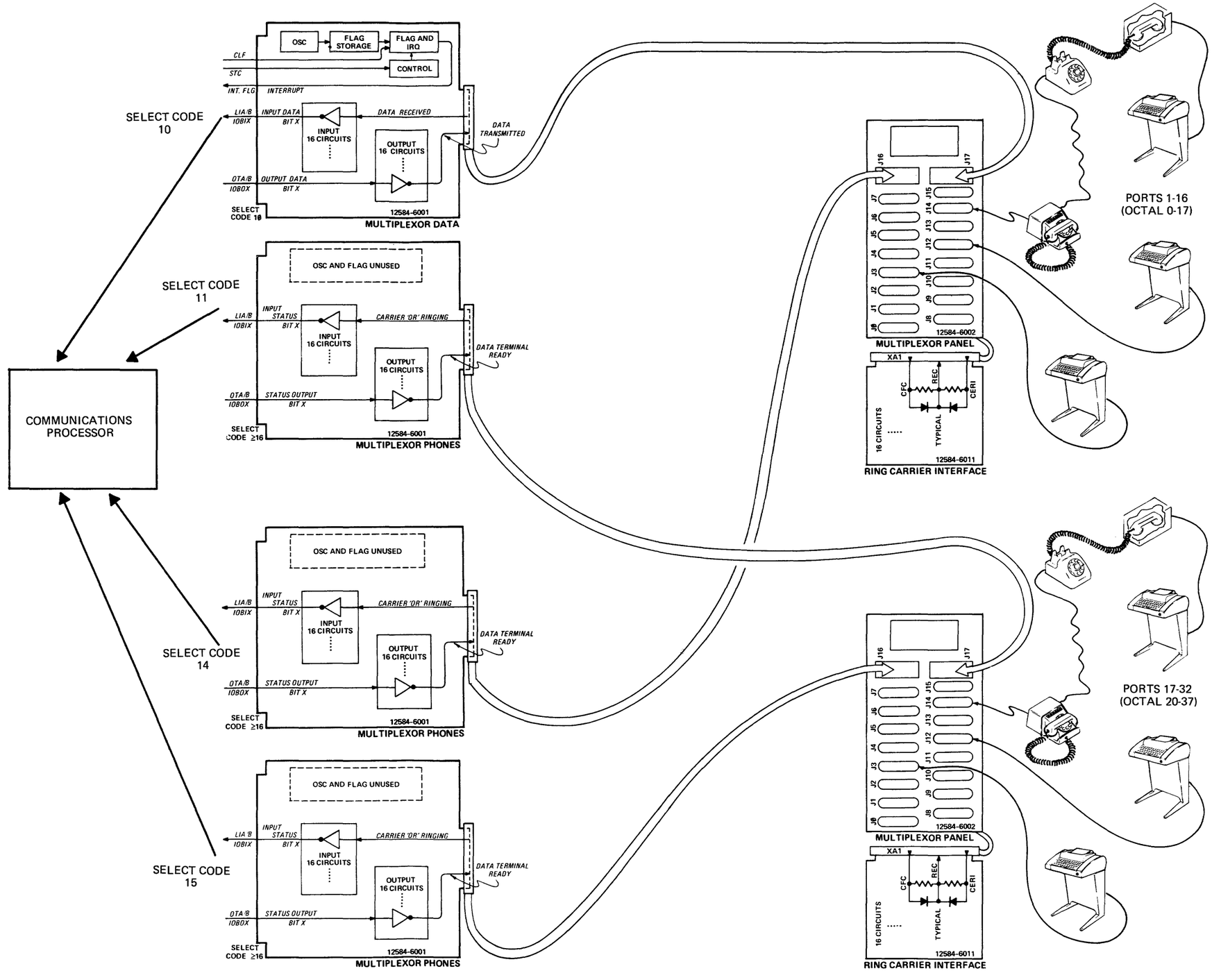


FIGURE 2. MULTIPLEXOR DATA AND PHONES

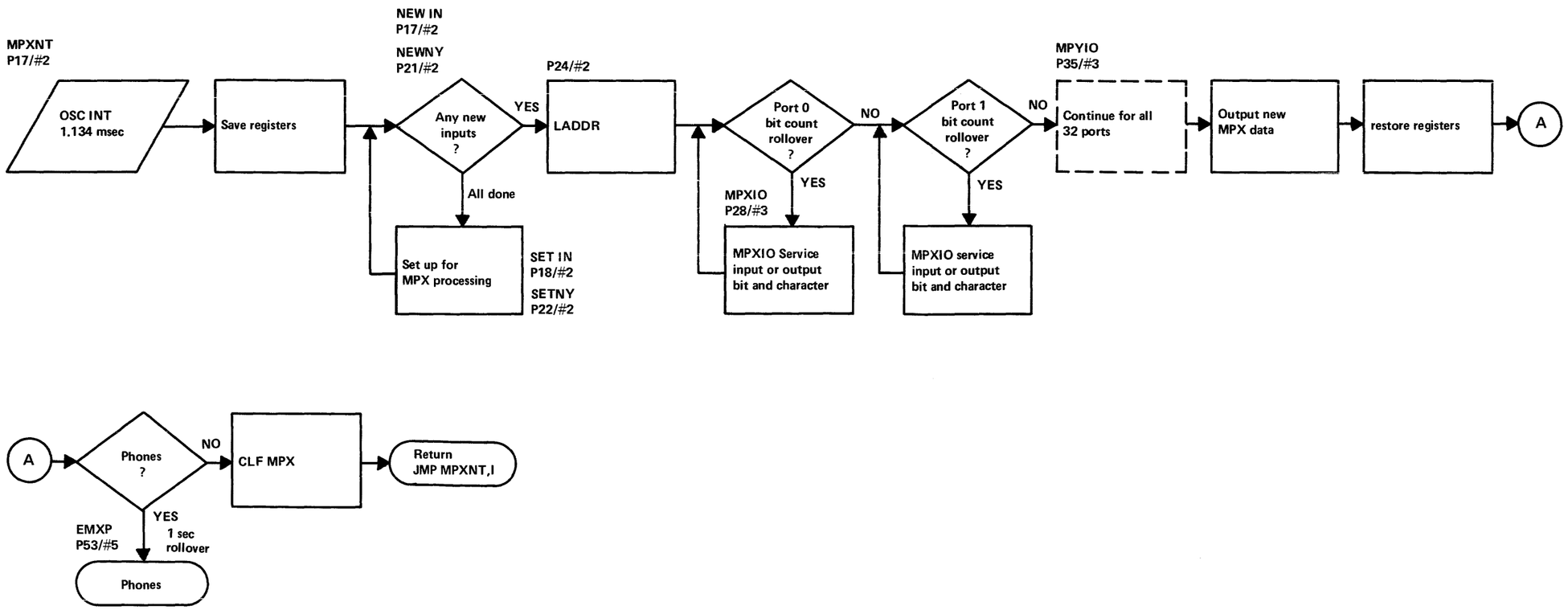


FIGURE 3. MULTIPLEXOR ROUTINE BLOCK DIAGRAM

When a full input line is available, or the output buffer is reduced to 10 characters, the System Processor must be told. Instead of setting a MPCOM bit as was done in the 2000A, now a status change is initiated through the processor communications drivers. This affects the HP 2000A TSS Figure 6 sheet 2 of 3 and 3 of 3 at the end of each respective flow chart.

With this general background we can be more specific with the technique adapted for the 2000B. There is no difficulty getting to the TTY tables or buffer once the user is known. We still use the base page to copy certain TTY entry addresses for the user during SETIN or MPXIO processing. Because of the 32 user capability it is necessary to have 2 words each for the flags such as Fast Port (FAF), Ignore Port (IG), Input/Output pointer (IOTOG), etc. Rather than preparing a technique for multiple entrance to these multiplexor segments it was more expedient to provide duplicate code segments. Each refers directly to its multiplexor Data or Phone board and the corresponding base page flag words. In the trade off simpler housekeeping and faster execution is achieved at the expense of additional core. A glance at the core map will indicate the rather minimal core duplication.

The feature of allowing the console operator to specify the number of ports means that certain unused hardware ports are not provided with a swap track. To insure against inadvertant noise glitches or operator hardware error that would prove unhealthy to the system the IG and IG1 flags are provided. The System Processor sets these bits upon awake from sleep and during initial system configuration. These bits instruct the multiplexor to ignore the user even though an apparant space might be received.

The incoming multiplexor data is masked by the IG bits and becomes the INBIT data. This is further checked against the INPTF words which indicate the users which are currently being serviced by the multiplexor routine. The residue are those new inputs requiring new set up.

The FAST command clears the corresponding bits in the FAF flag word (for 220 baud rate). This data is used during set up to determine the number of interrupts to the middle of the start bit. During bit count rollover in the MPXIO routine it is used again to determine the number of interrupts to the middle of the next bit.

IOTOG is used within the MPXIO to determine whether an input or output character is being processed.

The ABTST flag indicates the users who are being checked for an abort. The abort allows terminating an operation such as RUN or LIST by the Basic Interpreter. There are certain functions that cannot be allowed to terminate prematurely. These include the process of compiling or semi-compiling, renumbering, or appending. Any of these would leave the internal program representation in disarray. A user in potential abort must be checked each interrupt for a data change, whereas an active user is only processed on bit count rollover.

2-3 Communications Processor TTY Tables

The functions of the Teletype table entries can be organized by their relationship to Multiplexor, Scheduler, Basic Interpreter, or general system information. In the 2000A they were all located together in a common TTY table. Now for the 2000B and 2000C we see a splitting by functions and only the necessary TTY table entries are provided in each processor.

The entries which were retained in the System Processor Coding but are not required in the Communication Processor Coding, include the swap area related entries, the scheduler queue related entries, and some general entries. The swap area entries are: DISC and PROG. The scheduler entries are: LINK, PLEV, RSTR, and CLOC. The general entries are ID, NAME, and TIME. These are all discussed in Section 4-3.

Three new entries are used in the Communications Processor. The ATIM and TIMO are required by the Enter command. The third one BSAV replaced an entry in the users swap area (BADDR), and provides reset capability. The Basic Interpreter has certain branch conditions in evaluating the syntax line. The buffer pointer BHED is advanced through the character sequence in the line. BSAV now is required in the Communications Processor to allow resetting to the beginning of the current line (or to the beginning of the branch condition).

One duplication exists in the TTY Tables for both the System Processor and Communication Processor. This is the STAT entry. You will notice a great deal of difference between these two entries. The status of the user has different implications for the multiplexor in the Communications Processor than for the scheduler or Basic Interpreter in the System Processor. The description of the status bits in the TTY definitions will help to clarify the manner in which these status entries are used.

The following list of TTY Table entry definitions is arranged in the sequence in which they appear within the TTY table.

The Teletype tables in the Communications Processor consist of 17 entries for each of the 32 possible users. Four entries are fixed depending only on the users port number (MASK, BGIN, BEND, & LADR).

BTIM Is a counter location which counts the multiplexor interrupts corresponding to the individual bits. It is incremented by the ISZ instruction in the LADDR coding. BTIM rollover indicates required servicing by the MPXIO routine for bit processing.

CHAR Is a location containing the current character being processed. The character is input or output a bit at a time and the packing or unpacking is done in this location.

BCNT Counts the number of bits within a character for both input and output mode.

MASK A "one" in the bit corresponding to the port number allows AND and XOR type instructions to update pointers. The value is a constant for each port number.

The next five entries are associated with the character buffer for input and output manipulation. Refer Section 2-4.

CCNT* Contains the number of characters to be output including the current one. The value is in minus form.

BPNT* Points to the location in which the next input character will be placed. In output it points to the character currently being transmitted.

BSTR* Points to the first character of the current line.

BHED* Points to the head of the input or output character sequence.

BSAV* Points to the beginning of the current line in the buffer, or sometimes to an intermediate branching point, and allows BHED to be reset if necessary.

The next three entries are pointer addresses depending on the user port number.

BGIN* Associated with each port is a 150 word buffer. BGIN contains the address of the first word.

BEND* BEND is the address of the next word following the end of the physical buffer.

LADR The multiplexor contains a ladder subprogram. LADR is the address of an instruction corresponding to the user port. This allows this instruction to be changed from a JMP to an ISZ during character processing. The ISZ performs the bit timing. It is replaced by a JMP when the character is complete.

Two entries are used for general timing.

PHON Is used for timing required by the Phones Logic, including log on and disconnect timing. The location is a timeout counter when in use.

ABCN This is a counter used by the multiplexor to handle possible abort timing. Break key must be depressed for 114 msec to achieve abort. When abort timing is taking place user data is compared every interrupt.

*Refer to Section 2-4 for address convention.

STAT This contains the status of the user. The System Processor also has a stat entry but the codes are different.

TPBT bit Ø	User in tape mode
STBT bit 1	Stop bit due to full output buffer
ESBT bit 2	Escape was hit, or input buffer full in tape mode
NIBT bit 3	No input allowed
LDBT bit 4	Line dropout occurred
LTBT bit 5	Log on timing
ENBT bit 6	Enter timing
HUBT bit 7	Hang user up
RNBT bit 8	User is running

The next two entries are new with the 2000B and provide timing capability for the ENTER statement.

ATIM Contains allowed time for ENTER statement execution. Time value in tenths of a second. Initiated by System Processor STE. Time limit value in seconds is converted to tenths before storing in ATIM.

TIMO Loaded with the 2's complement value of ATIM. Following the output message for the ENTER statement this value is incremented once per phone servicing. The process is terminated either by an input carriage return or by TIMO rollover. The response time in seconds is determined by adding ATIM to TIMO and dividing by 10.

Table 1 lists the memory addresses for each of the Communications Processor TTY table entries. Notice that the contents of those entries with fixed data is shown. Only the first 16 ports are included. The pattern is evident. It is expected that the reader will have a Listing and could easily generate specific table entries for a user with port number 20 to 37.

2-4 Teletype Buffer Pointers

Six TTY table entries contain address information associated with the buffer. An interesting technique is used to specify (or designate) the left or right character position. The actual address is multiplied by 2. Bit zero indicates left position with a "Ø" and right position with a "1". When the address information is to be extracted the pseudo address entry is rotated ERA or ERB. This divides by two leaving the actual address in the register. It also provides the left or right positional information in the E register.

TABLE 1
COMMUNICATIONS PROCESSOR TTY TABLE

	Ø (ØB)	1 (1B)	2 (2B)	3 (3B)	4 (4B)	5 (5B)	6 (6B)	7 (7B)	8 (10B)	9 (11B)	10 (12B)	11 (13B)	12 (14B)	13 (15B)	14 (16B)	15 (17B)
BTIM	504	525	546	567	610	631	652	673	714	735	756	777	1020	1041	1062	1103
CHAR	505	526	547	570	611	632	653	674	715	736	757	1000	1021	1042	1063	1104
BCNT	506	527	550	571	612	633	654	675	716	737	760	1001	1022	1043	1064	1105
MASK	507 (1)	530 (2)	551 (4)	572 (10)	613 (20)	634 (40)	655 (100)	676 (200)	717 (400)	740 (1000)	761 (2000)	1002 (4000)	1023 (10000)	1044 (20000)	1065 (40000)	1106 (100000)
CCNT	510	531	552	573	614	635	656	677	720	741	762	1003	1024	1045	1066	1107
BPNT	511	532	553	574	615	636	657	700	721	742	763	1004	1025	1046	1067	1110
BSTR	512	533	554	575	616	637	660	701	722	743	764	1005	1026	1047	1070	1111
BHED	513	534	555	576	617	640	661	702	723	744	765	1006	1027	1050	1071	1112
BSAV	514	535	556	577	620	641	662	703	724	745	766	1007	1030	1051	1072	1113
BGIN	515 (12330)	536 (13004)	557 (13460)	600 (14134)	621 (14610)	642 (15264)	663 (15740)	704 (16414)	725 (17070)	746 (17544)	767 (20220)	1010 (20674)	1031 (21350)	1052 (22024)	1073 (22500)	1114 (23154)
BEND	516 (13004)	537 (13460)	560 (14134)	601 (14610)	622 (15264)	643 (15740)	664 (16414)	705 (17070)	726 (17544)	747 (20220)	770 (20674)	1011 (21350)	1032 (22024)	1053 (22500)	1074 (23154)	1115 (23630)
LADR	517 (2207)	540 (2213)	561 (2217)	602 (2223)	623 (2227)	644 (2233)	665 (2237)	706 (2243)	727 (2247)	750 (2253)	771 (2257)	1012 (2263)	1033 (2267)	1054 (2273)	1075 (2277)	1116 (2303)
PHON	520	541	562	603	624	645	666	707	730	751	772	1013	1034	1055	1076	1117
ABCN	521	542	563	604	625	646	667	710	731	752	773	1014	1035	1056	1077	1120
STAT	522	543	564	605	626	647	670	711	732	753	774	1015	1036	1057	1100	1121
ATIM	523	544	565	606	627	650	671	712	733	754	775	1016	1037	1060	1101	1122
TIMO	524	545	566	607	630	651	672	713	734	755	776	1017	1040	1061	1102	1123

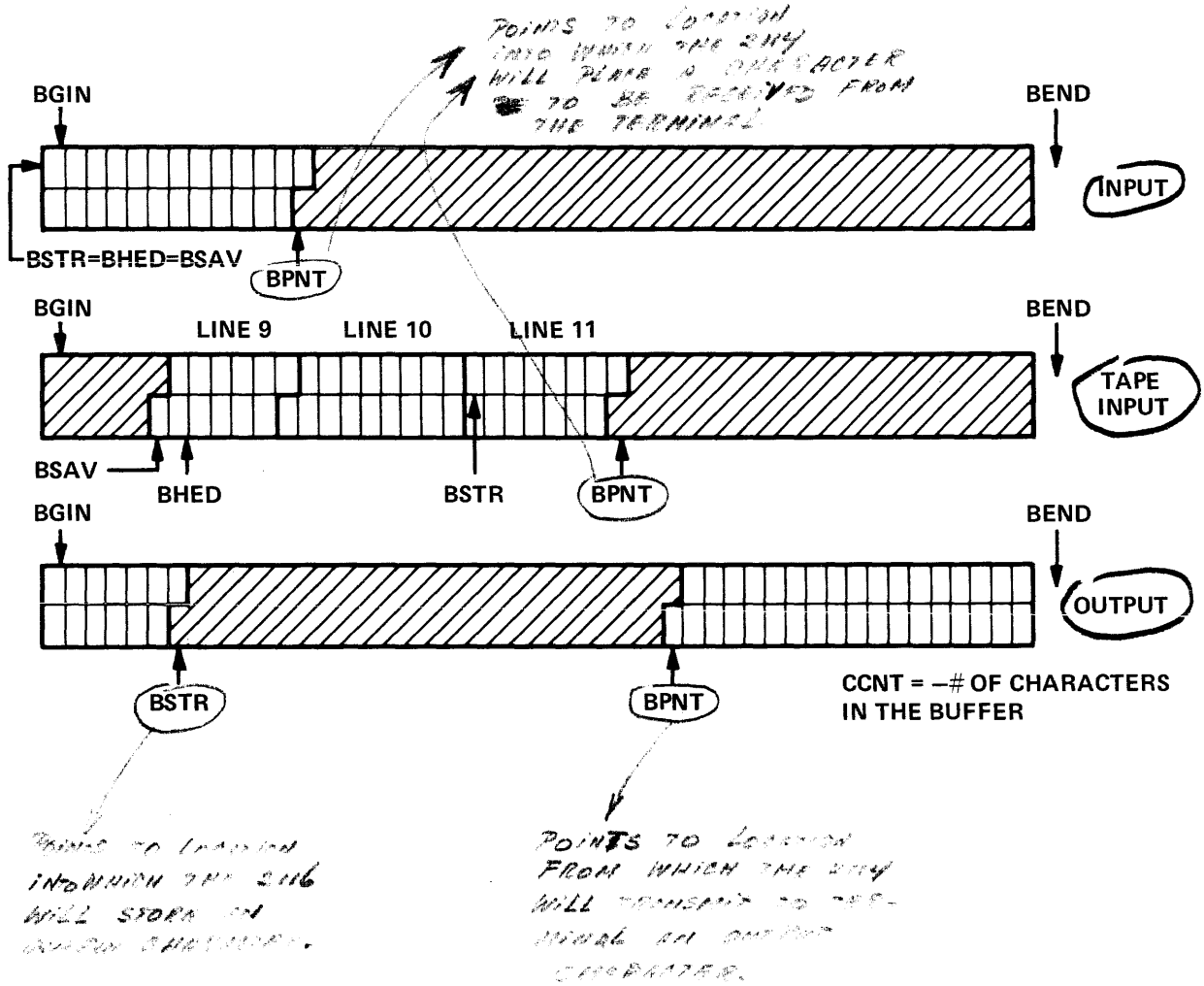


FIGURE 4. INPUT/OUTPUT BUFFERING

Figure 4 shows the use of buffer pointers. BGIN always points to the first character position in the buffer. It allows easy resetting of other buffer pointers. BEND points to the first character beyond the users buffer. It is used primarily to test for wrap around in TAPE mode or OUTPUT. In normal input all characters in excess of the full buffer length are lost.

For input BSTR = BHED = BSAV and all are equal to the physical beginning of the buffer. BPNT points to the next sequential position into which a character may be placed. At the end of the input line the system processes the line. It then outputs a carriage return. The end of the output resets the buffer pointers.

For output the buffer is merely a sequential buffer for up to 300 ASCII characters. Lines have no significance. BSTR points to the next available location for an output character. BPNT points to the location from which the multiplexor will get the next character to be serviced. It is pure wrap around buffer. When BPNT catches up to BSTR the output buffer is empty, and all 4 pointers are reset to BGIN. When system output rate exceeds the terminal capacity BSTR advances toward BPNT (buffer is filling up). When the character count CCNT reaches -299 the Communications Processor initiates an output suspend request to the System Processor.

The operation in Tape mode is somewhat more complex. The user types TAPE and then begins to read tape. Initially all buffer pointers = BGIN. As characters are appended to the buffer BPNT is advanced. When each carriage return is found (by the multiplexor) BSTR is advanced to the beginning of the next line. The Communications Processor sends the HVL command while characters still continue to be appended. BPNT and BSTR continue to advance as above.

When the System Processor starts to process the input line BHED moves a character at a time. BSAV marks the beginning of the line. It also indicates the temporary limits of the buffer. When a complete line is processed BHED has advanced to the first character of the next line. The System Processor asks if more input exists with the ALI which in turn advances BSAV. At the ALI request if BHED ≠ BSTR it indicates one or more full lines exist in the buffer and the Communications Processor responds HVL.

In input the response to a backspace is to decrement BPNT by one. If BPNT = BSTR the line is null and the backspace is ignored.

2-5 Base Page Locations Communications Processor

ABTST 110 ABTSY 111	Abort flag bit = Ø for abort in progress. This bit is set as a result of input when the status word says no input is allowed (NIBT). The input is checked every multiplexor interrupt to determine that it remains a space (zero) for 100 interrupts.

FAF 131
FAF1 132

The bit is cleared for 220 baud rate. It is cleared as a result of the console command FAST - Port. It is used by SETIN to set 2 or 4 interrupts to the middle of the start bit, and by the MPXIO to set 4 or 8 interrupts to the next bit.

IG 133
IG 134

If bit = 1 ignore that port. During configuration the bits are set for all ports which are not opened. The multiplexor then ignores all input data from these ports.

INBIT 135
INBIY 136

This bit is low whenever a start signal is detected (i.e., the first indication of a character from the TTY). The Ignore (IG) bits are OR'd to throw out data from all ports not opened at configuration time. This composite word now forms the new multiplexor data for each interrupt.

INPTF 137
INPTY 140

This bit is set upon a new input (i.e., TTY start bit). The port is set up for servicing. Thereafter the incoming data is only serviced as a result of bit count (BCNT) rollover, or end of character. The INPTF bit is cleared during end of character processing.

IOTOG 141
IOTG1 142

Bit is cleared for output. It is used by MPXIO at bit count rollover to determine whether to remain in the input section, or to go to the output section. This bit is set again at the "End of the Output" (i.e., when the TTY buffer becomes empty).

2-6 Core Map Communications Processor

Figure 5 shows the core map for the Communications Processor. It is drawn approximately to scale. The small percentage (of core) required by the actual multiplexor software is rather interesting. It is apparent on this figure what a large part of the available 8K memory is dedicated to the TTY Buffers. A significant unused portion exists under the loader. It can be used for software additions or additional features (through the contributed library).

2-7 Phones Routine

The phones routine was placed in the Communications Processor to service the phones boards and also to save core in the System Processor. In the 2000A, the phones routine was located in the Scheduler and thus, was entered 10 times per second. In the Communications Processor only the multiplexor provides a timed interrupt. It requires 88 interrupts to provide the 0.1 second interval.

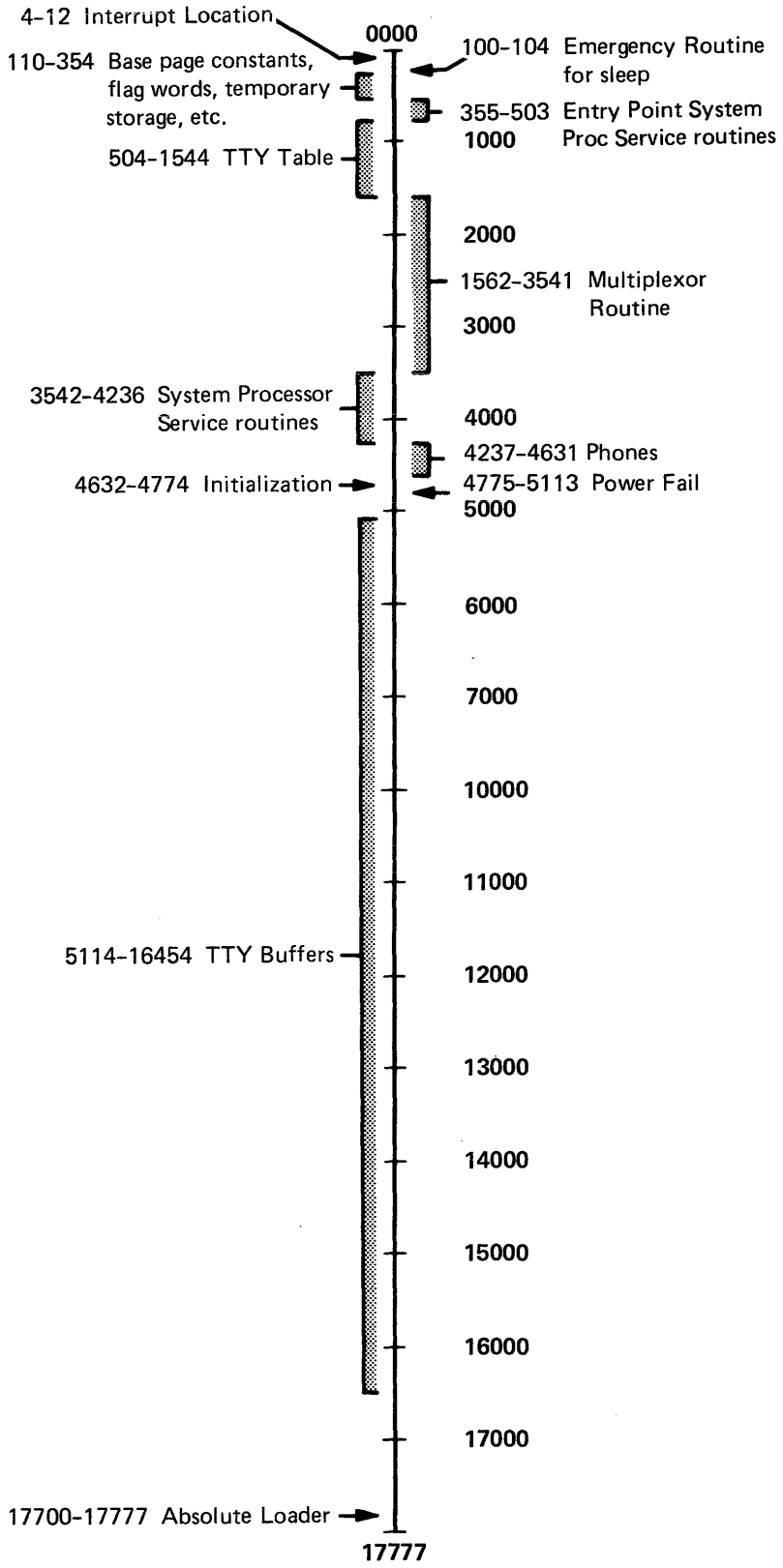


FIGURE 5. CORE MAP

The routine still provides the servicing for a new call in, a user hang up, and an unsuccessful log on. A new function required in the 2000B and C is the timing for the ENTER statement. The actual timing for this routine is non-critical.

Most of the Phones servicing is done with the interrupt system enabled. This allows the multiplexor and System Processor communications to interrupt. In effect, this routine makes use of the chinks of time that would otherwise be spent waiting in the idle loop.

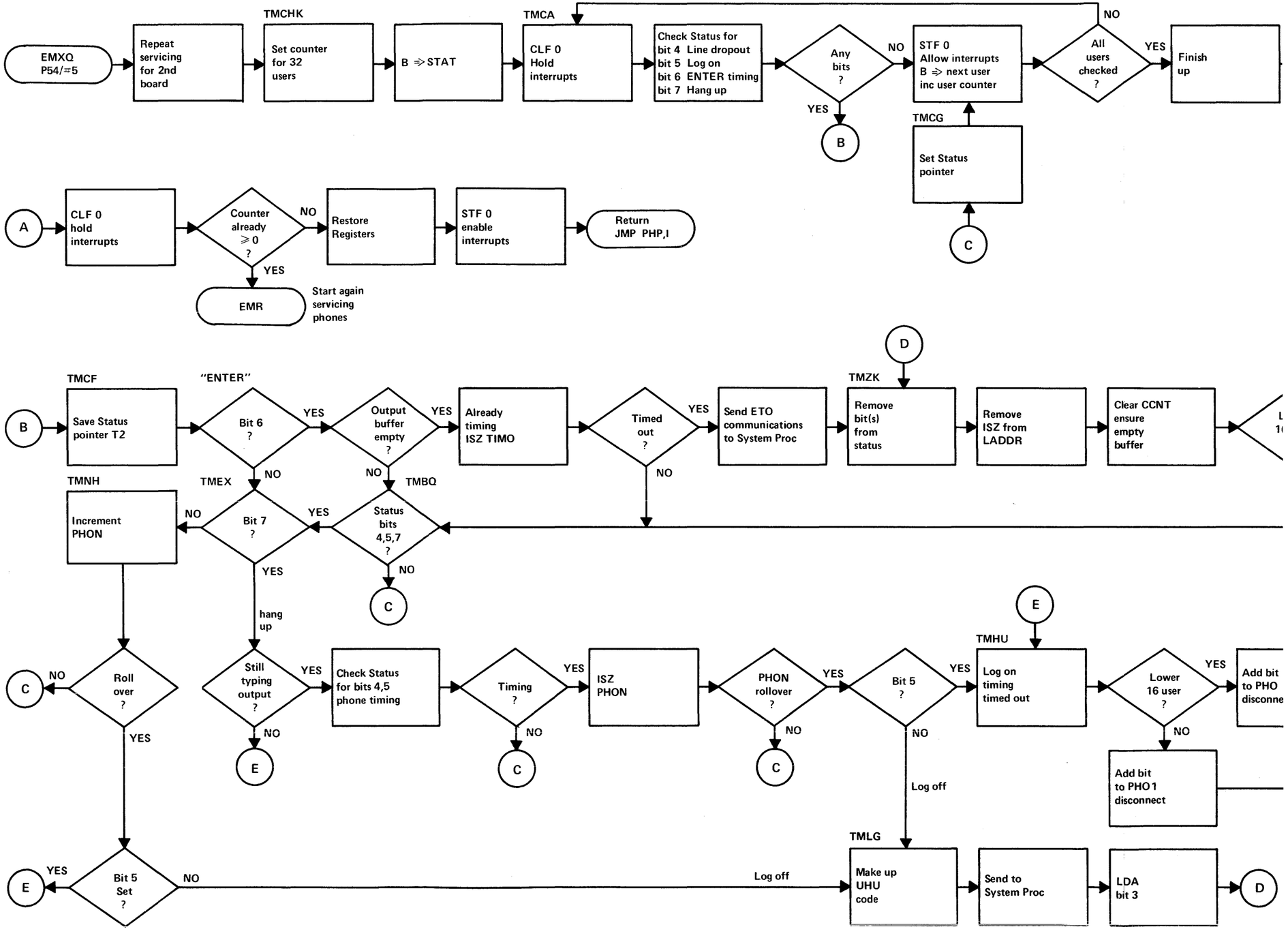
It should be apparent to the reader that the time required to service the phones for log on and hang up is quite small. Consider all 32 users being serviced by the phones routine on a 3 minute basis. Statistically this would require handling one call in and one hang up (or time out) per interrupt. This is a low duty cycle. A more common environment might be CAI in which many users were being timed for ENTER statements.

Refer to Figure 6 for the detailed Phones Block Diagram. The first page gets the new data from the phone board. It compares it with the previous data and determines changes. The changes imply either a new call up (or end of line dropout) or a hang up (or line dropout). The routine then processes the status word and sets the timer value for timing.

When all changes are processed the procedure is repeated for the second phones board.

The second part of the routine services each of the 32 users. It looks at the status word for four conditions: Line Dropout, Log On, ENTER timing, and Hang Up. It initiates communications to the System Processor for ENTER time out. It interprets a line drop out which exceeds 2 seconds as a hang up and initiates communications to the System Processor. The System Processor responds with the Hang Up command when the output message is completed.

The final task updates the data and interrupt counter. The return location is the interrupt address for the multiplexor interrupt when the phones counter rolled over. Typically it will be the idle loop.


EMXQ
P54/=5
Repeat servicing for 2nd board
TMCHK
Set counter for 32 users
B ⇒ STAT
TMCA
CLF 0 Hold interrupts
Check Status for bit 4 Line dropout bit 5 Log on bit 6 ENTER timing bit 7 Hang up
Any bits ?
NO
YES
B
STF 0 Allow interrupts B ⇒ next user inc user counter
All users checked ?
NO
YES
Finish up
TMCG
Set Status pointer
C
A
CLF 0 hold interrupts
Counter already ⩾0 ?
NO
YES
Restore Registers
STF 0 enable interrupts
Return JMP PHP,I
EMR
Start again servicing phones
B
TMCF
Save Status pointer T2
"ENTER"
Bit 6 ?
YES
NO
TMEX
Output buffer empty ?
YES
NO
TMBQ
Already timing ISZ TIMO
Timed out ?
YES
NO
Send ETO communications to System Proc
D
TMZK
Remove bit(s) from status
Remove ISZ from LADDR
Clear CCNT ensure empty buffer
TMNH
Increment PHON
NO
Bit 7 ?
YES
hang up
Status bits 4,5,7 ?
NO
C
E
TMHU
Log on timing timed out
Lower 16 user ?
YES
NO
Add bit to PHO disconne
Add bit to PHO1 disconnect
C
NO
Roll over ?
YES
Still typing output ?
YES
NO
E
Check Status for bits 4,5 phone timing
Timing ?
YES
NO
C
ISZ PHON
PHON rollover ?
YES
NO
C
Bit 5 ?
YES
NO
Log off
E
YES
Bit 5 Set ?
NO
Log off
TMLG
Make up UHU code
Send to System Proc
LDA bit 3
D

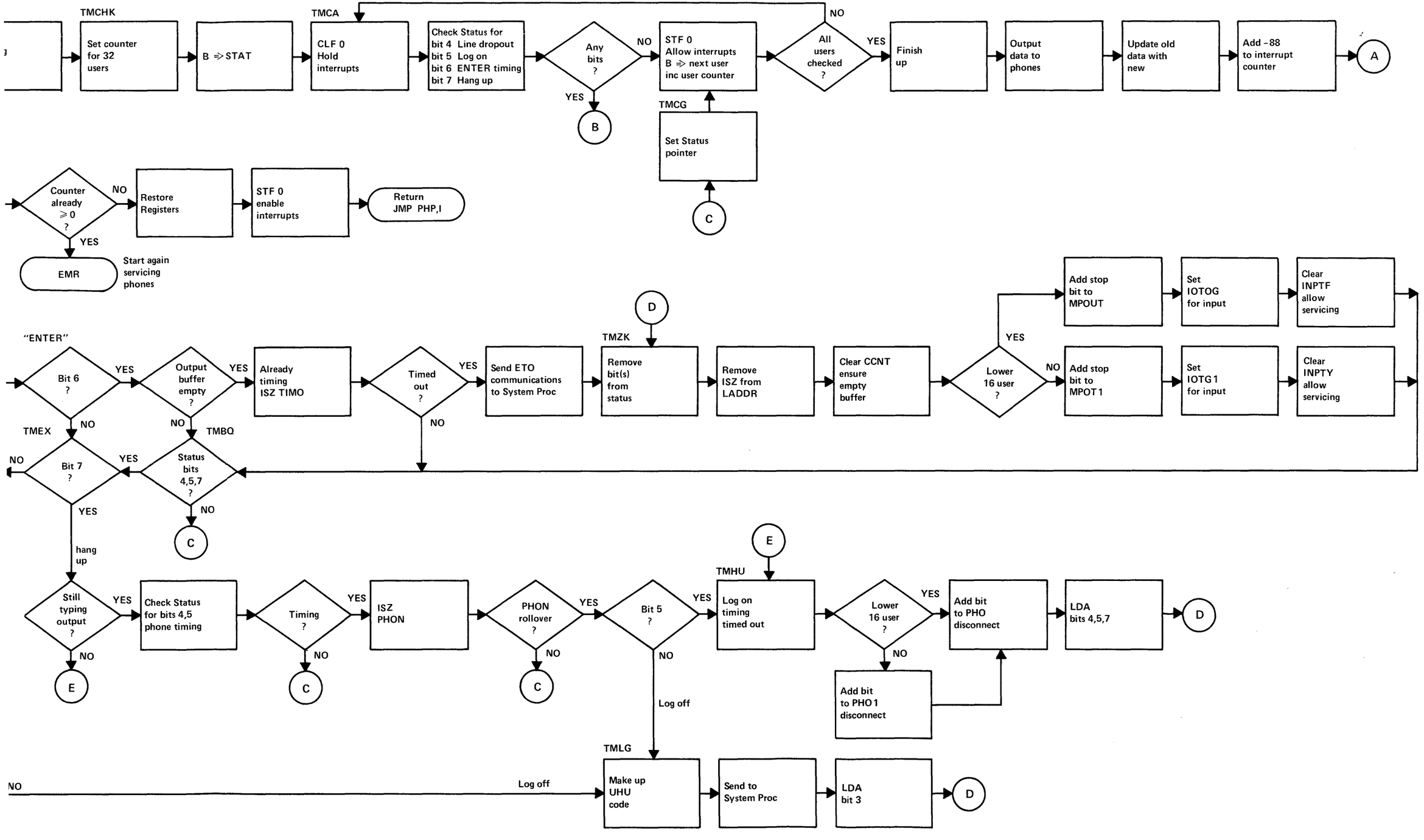


FIGURE 6. PHONES BLOCK DIAGRAM SHEET 1 OF 2

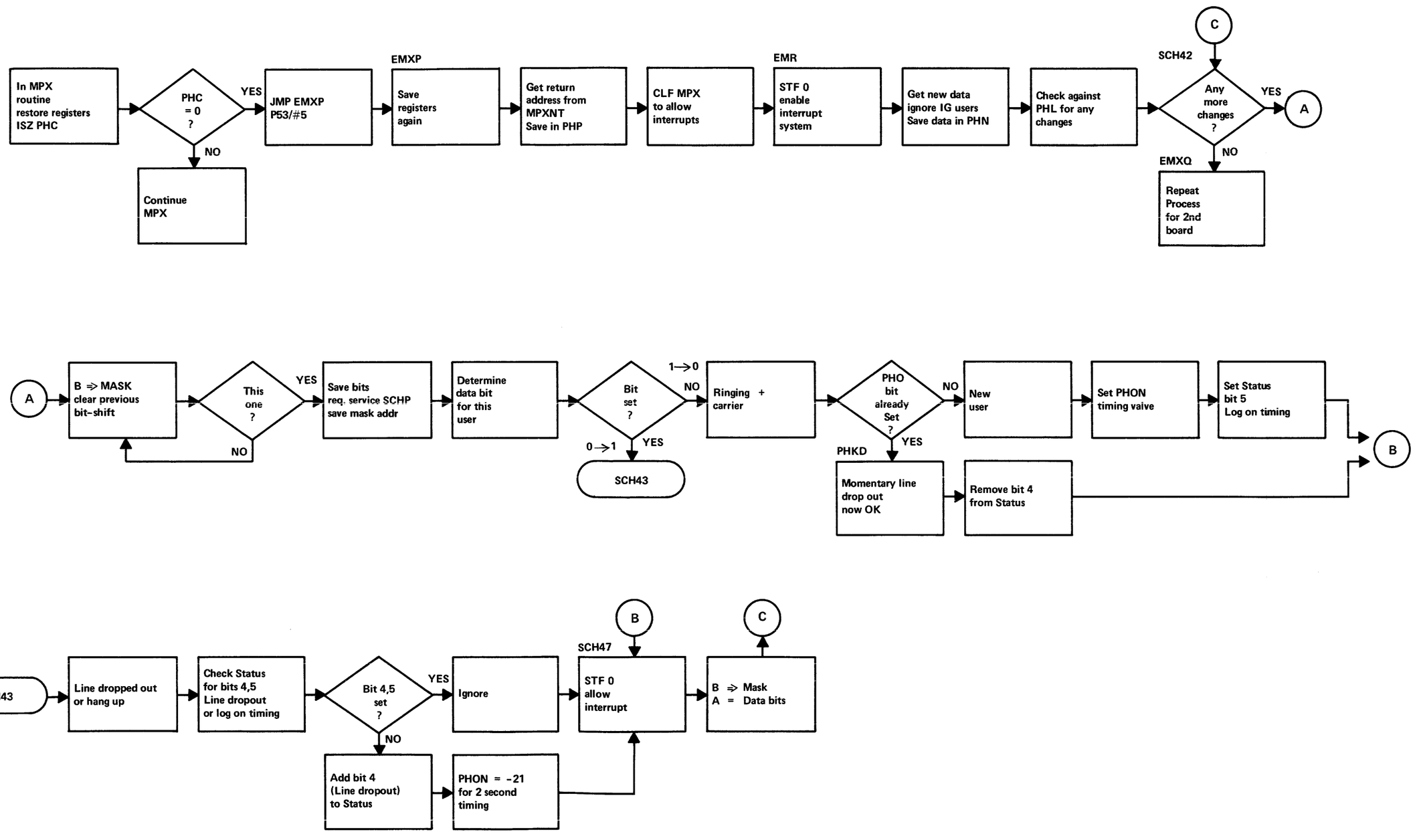


FIGURE 6. PHONES BLOCK DIAGRAM SHEET 2 OF 2

Processor Communications

CHAPTER 3

PROCESSOR COMMUNICATIONS

3-1 Processor Interconnect Kit

Figure 7 shows the block diagram for the System Processor initiate communications channel. The Communications Processor initiate channel is identical except that its select code is 13 and the System Processors select code is 1Ø.

Figure 8 shows the Logic Diagram in which the optional circuitry and unused jumpers have been removed. All four of these 12566-6001 assemblies are identical.

We can trace through the circuit operation of the interconnect kits. The first operation is to place the request code word in the output buffer. This is done with an OTA SC = 11. This places the data word on the IOBO lines. The IOO computer signal is gated with T4 and latches the data in the output flip flops.

The actual transfer is accomplished with a STC 11,C. Dotted lines on the logic diagram show these signals. The STC sets the Encode signal which becomes the Device Flag to the Communications Processor. This in turn causes the data to be placed in its input register, and produces the interrupt.

When the Communications Processor acknowledges with its OTA and STC 12,C this generates the Device Flag signal. The device flag is a positive to negative transition. This is inverted and filtered by MC 87A, R61 and C3. The rise time is improved with MC 87C,D. This positive transition then actuates two "window" type circuits. These circuits produce a negative pulse of short duration. Notice the MC 86C input on pin 13 goes positive right away. The signal on pin 12 is positive but going negative at the rate determined by the R66-C5 time constant. This produces a narrow negative pulse from MC 86C and also MC 85B. MC 86C clears the Encode FF allowing the Device Flag circuitry in the Communications Processor to stabilize before the next command.

The MC 85B signal latches the input data in the flip flops, and also sets the Flag Buffer. Notice however the Flag FF must be cleared or else the Device Flag signal is ignored.

The System Processor cleared the Control right after sending the request. This prevents an automatic interrupt. The System Processor will test the Communications Processor acknowledgement with a SFS signal instead.

3-2 Communications (System to Communications Processor)

The System Processor can initiate requests and commands for the Communications Processors. Two of these are of general nature (i.e., not limited to an individual user). They include PHO to establish the phone log on time limit, and INI to initialize the new system. The other commands are user oriented (the TTY number is specified).

The user commands are associated with the buffer, with hardware control, and for general status. The hardware control includes ECO and ECF for Echo control, and FAS and SLO for terminal speed. Buffer control includes OCR, output a character, and GTC, get next character, for actual data transfer. It uses SBP to place the buffer pointer, RBP to restore the buffer to the start, and BKS to backspace a single character.

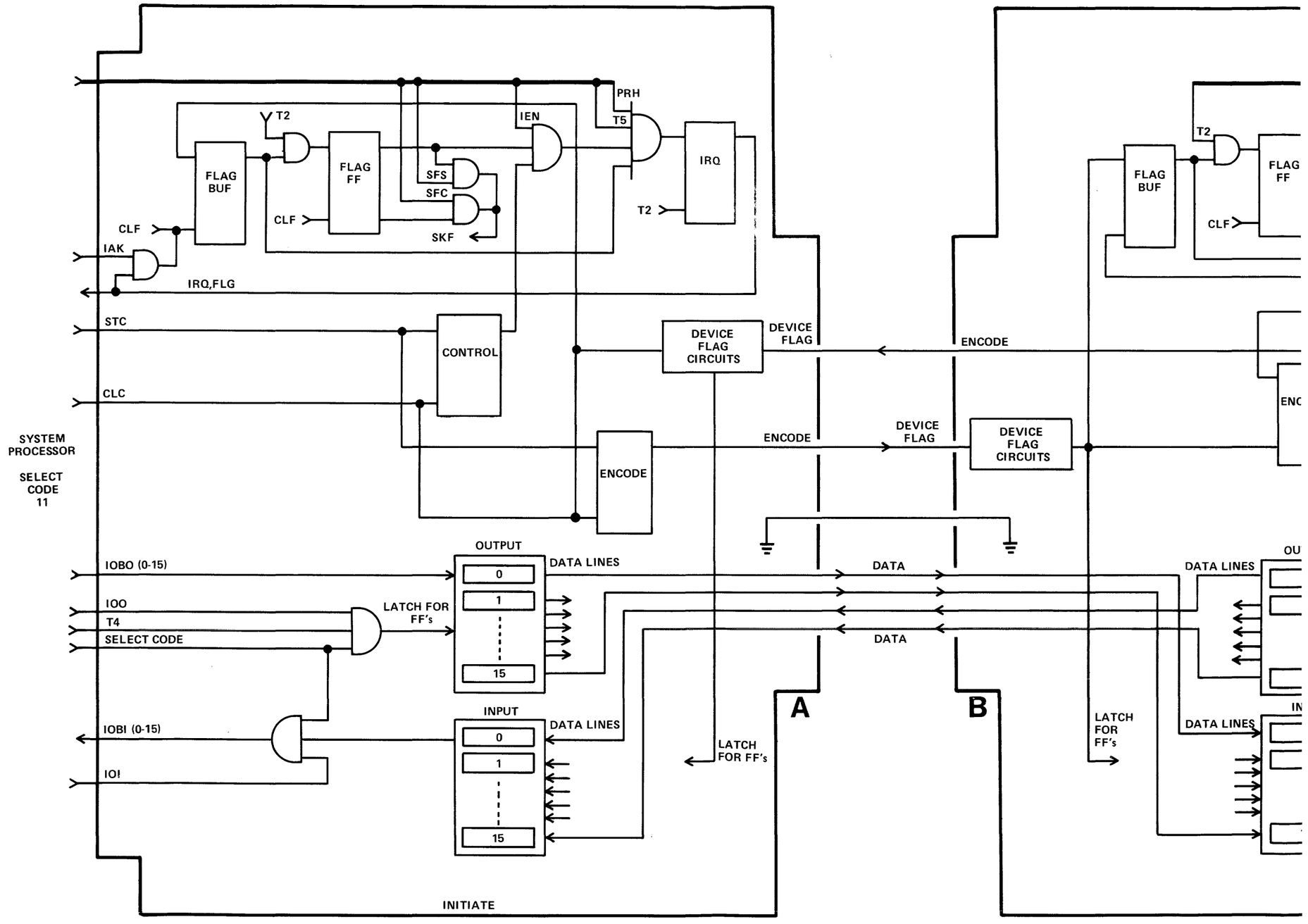
The general status includes NUC, a new user called up, ULO, user got logged on, and HUU, hang user up. The user system status includes UIR, user is running, UNR, user not running, IWT, Input wait, OWT, output wait, and STE, start timing for an ENTER statement execution. KAO allows killing a user for Break or Sleep execution. IBF checks if the buffer is full for the Announce command. IPF allows the System Processor to determine whether the user is in fast mode. The final three include TPO, tape mode, ILI, a check for a command entered during tape mode being valid, and ALI to request more input if available.

Table 2 shows the list of available commands. The actual location in listing from where the command is initiated is shown. This will help in tracking down the actual coding and processing involved.

Each command is described both with words and with a flowchart. These will be helpful in gaining an intuitive feel for the system operation and especially for the use of the TTY tables and buffer.

3-3 Code Format

The code word requires 5 bits in order to specify each of the 32 user ports. Bits 8–12 are used. Some commands require a data character. The eight bits Ø–7 are reserved for data. This leaves bits 13–15 for the code, allowing 8 possibilities. Seven are used for individual codes ØØØ to 11Ø. The eighth code (111) specifies a further micro code in bits Ø to 7. Eighteen are adequate for the commands shown. The sub-code ranges from octal ØØ to 21.


SYSTEM PROCESSOR
SELECT CODE 11
PRH
T5
T2
IEN
IRQ
FLAG BUF
FLAG FF
SFS
SFC
SKF
CLF
IAK
IRQ,FLG
STC
CLC
CONTROL
DEVICE FLAG CIRCUITS
DEVICE FLAG
ENCODE
IOBO (0-15)
IOO
T4
SELECT CODE
LATCH FOR FF's
OUTPUT
DATA LINES
0
1
15
DATA
IOBI (0-15)
IOI
INPUT
A
B
INITIATE

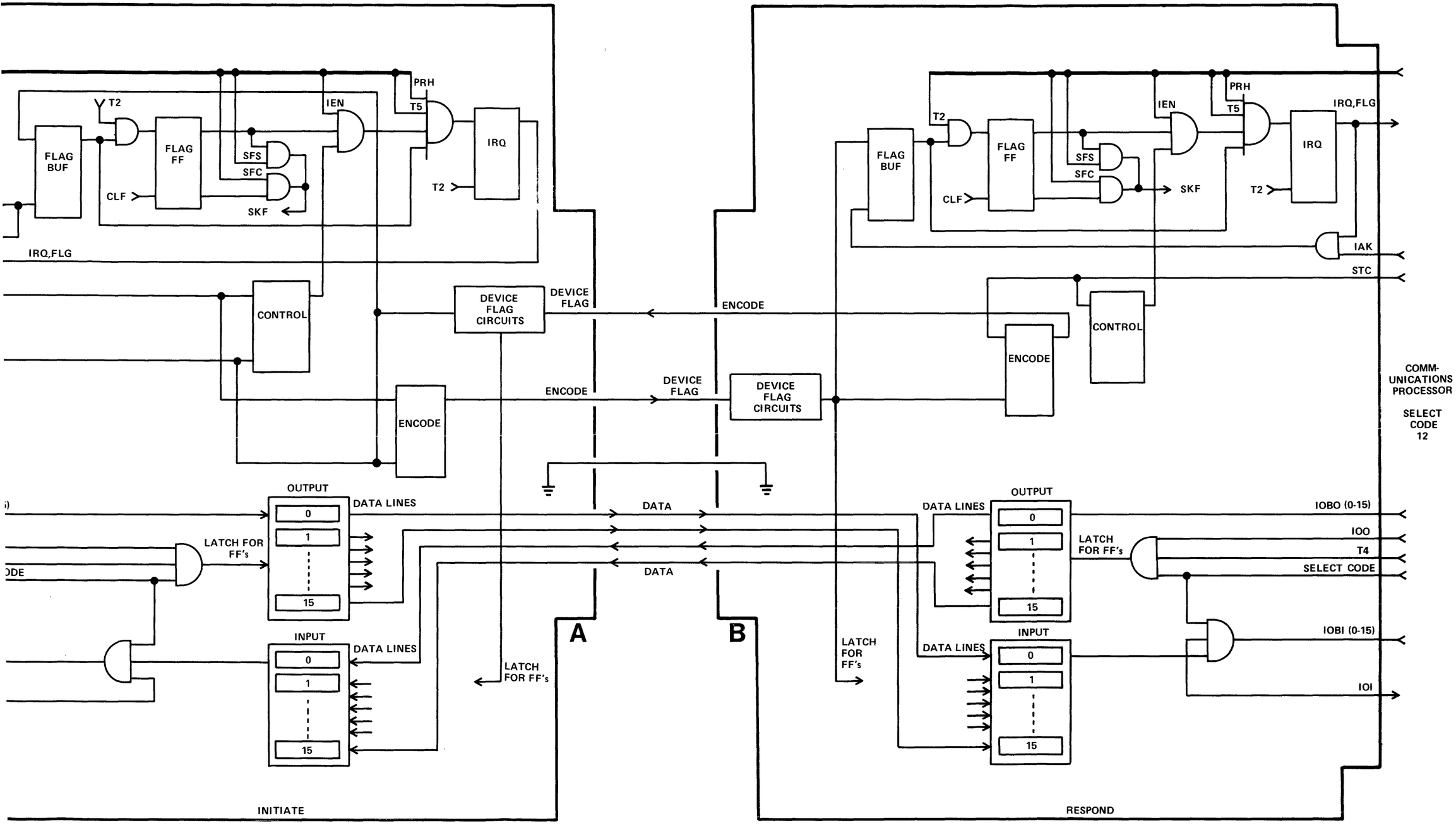


FIGURE 7. BLOCK DIAGRAM, INTER-PROCESSOR COMMUNICATIONS

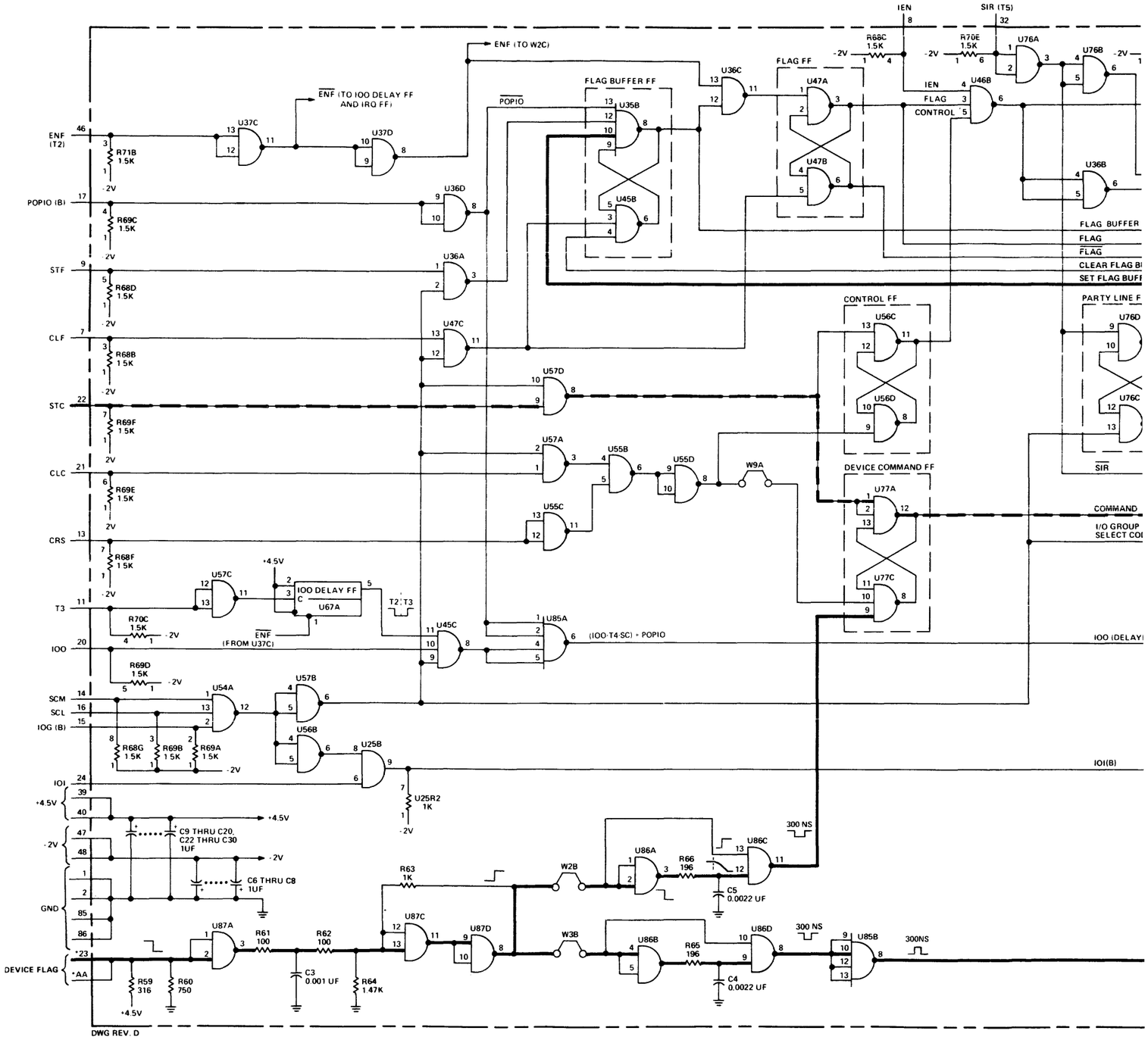


FIGURE 8. SIMPLIFIED PROCESSOR INTERCONNECT LOGIC DIAGRAM (12566-6001)

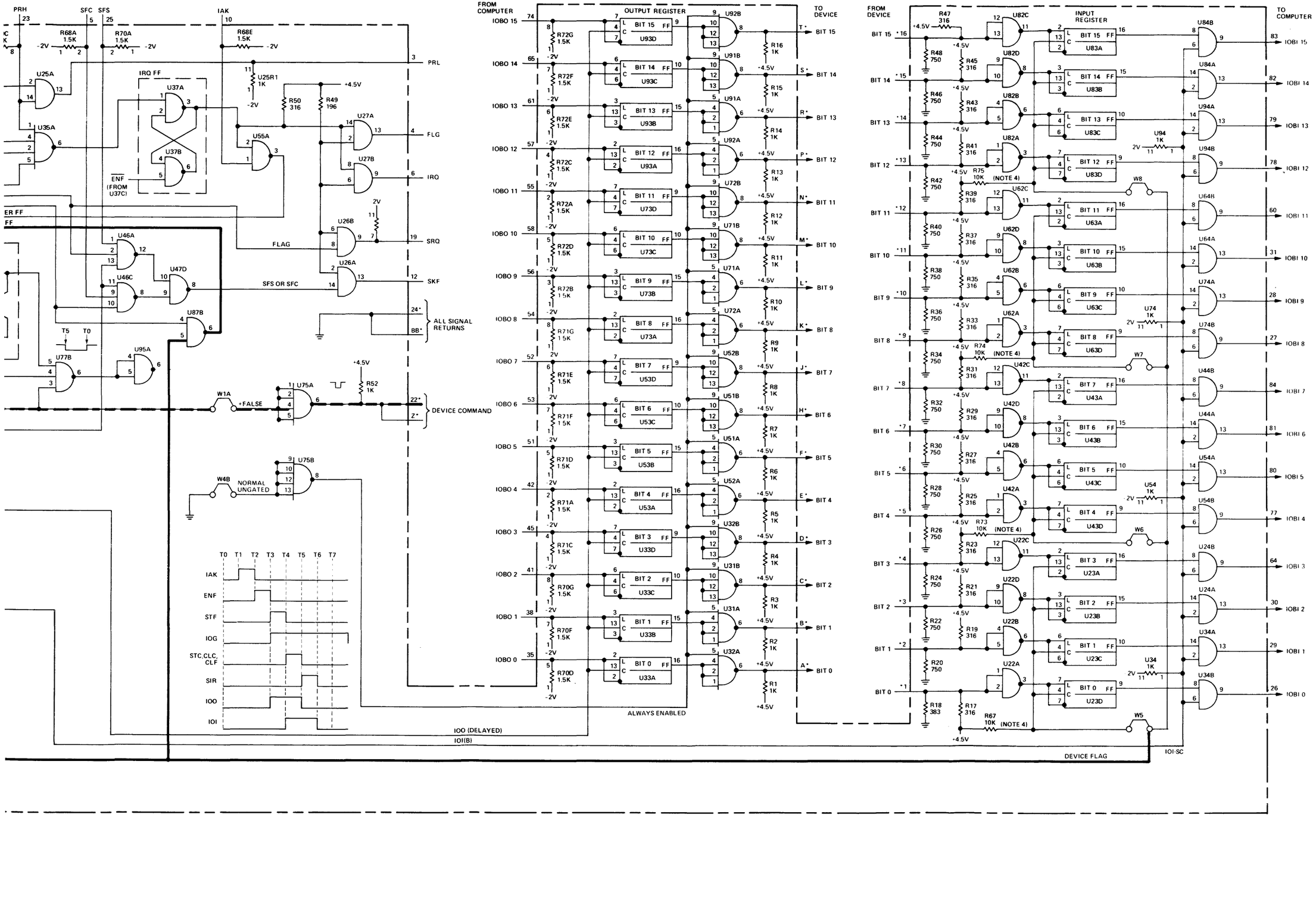

PRH
SFC
SFS
IAK
R68A 1.5K
R70A 1.5K
R68E 1.5K
-2V
IRQ FF
U37A
U37B
U25A
U35A
U25R1 1K
R50 316
R49 196
+4.5V
U55A
U27A
U27B
U26B
U26A
2V
ENF (FROM U37C)
FLAG
SFS OR SFC
U46A
U46C
U47D
U87B
U77B
U95A
T5
T0
+4.5V
R52 1K
W1A
+FALSE
U75A
U75B
W4B
NORMAL
UNGATED
PRL
FLG
IRQ
SRQ
SKF
ALL SIGNAL RETURNS
DEVICE COMMAND
T0 T1 T2 T3 T4 T5 T6 T7
IAK
ENF
STF
IOG
STC,CLC, CLF
SIR
IOO
IOI
IOO (DELAYED)
IOI(B)
FROM COMPUTER
OUTPUT REGISTER
TO DEVICE
IOBO 15
IOBO 14
IOBO 13
IOBO 12
IOBO 11
IOBO 10
IOBO 9
IOBO 8
IOBO 7
IOBO 6
IOBO 5
IOBO 4
IOBO 3
IOBO 2
IOBO 1
IOBO 0
R72G 1.5K
R72F 1.5K
R72E 1.5K
R72C 1.5K
R72A 1.5K
R72D 1.5K
R72B 1.5K
R71G 1.5K
R71E 1.5K
R71F 1.5K
R71D 1.5K
R71A 1.5K
R71C 1.5K
R70G 1.5K
R70F 1.5K
R70D 1.5K
BIT 15 FF U93D
BIT 14 FF U93C
BIT 13 FF U93B
BIT 12 FF U93A
BIT 11 FF U73D
BIT 10 FF U73C
BIT 9 FF U73B
BIT 8 FF U73A
BIT 7 FF U53D
BIT 6 FF U53C
BIT 5 FF U53B
BIT 4 FF U53A
BIT 3 FF U33D
BIT 2 FF U33C
BIT 1 FF U33B
BIT 0 FF U33A
U92B
U91B
U91A
U92A
U72B
U71B
U71A
U72A
U52B
U51B
U51A
U52A
U32B
U31B
U31A
U32A
R16 1K
R15 1K
R14 1K
R13 1K
R12 1K
R11 1K
R10 1K
R9 1K
R8 1K
R7 1K
R6 1K
R5 1K
R4 1K
R3 1K
R2 1K
R1 1K
T* BIT 15
S* BIT 14
R* BIT 13
P* BIT 12
N* BIT 11
M* BIT 10
L* BIT 9
K* BIT 8
J* BIT 7
H* BIT 6
F* BIT 5
E* BIT 4
D* BIT 3
C* BIT 2
B* BIT 1
A* BIT 0
ALWAYS ENABLED
FROM DEVICE
INPUT REGISTER
TO COMPUTER
BIT 15 *16
BIT 14 *15
BIT 13 *14
BIT 12 *13
BIT 11 *12
BIT 10 *11
BIT 9 *10
BIT 8 *9
BIT 7 *8
BIT 6 *7
BIT 5 *6
BIT 4 *5
BIT 3 *4
BIT 2 *3
BIT 1 *2
BIT 0 *1
R47 316
R48 750
R45 316
R46 750
R43 316
R44 750
R41 316
R42 750
R39 316
R40 750
R37 316
R38 750
R35 316
R36 750
R33 316
R34 750
R31 316
R32 750
R29 316
R30 750
R27 316
R28 750
R25 316
R26 750
R23 316
R24 750
R21 316
R22 750
R19 316
R20 750
R18 383
R17 316
R75 10K (NOTE 4)
R74 10K (NOTE 4)
R73 10K (NOTE 4)
R67 10K (NOTE 4)
U94 1K
U74 1K
U54 1K
U34 1K
W8
W7
W6
W5
U82C
U82D
U82B
U82A
U62C
U62D
U62B
U62A
U42C
U42D
U42B
U42A
U22C
U22D
U22B
U22A
BIT 15 FF U83A
BIT 14 FF U83B
BIT 13 FF U83C
BIT 12 FF U83D
BIT 11 FF U63A
BIT 10 FF U63B
BIT 9 FF U63C
BIT 8 FF U63D
BIT 7 FF U43A
BIT 6 FF U43B
BIT 5 FF U43C
BIT 4 FF U43D
BIT 3 FF U23A
BIT 2 FF U23B
BIT 1 FF U23C
BIT 0 FF U23D
U84B
U84A
U94A
U94B
U64B
U64A
U74A
U74B
U44B
U44A
U54A
U54B
U24B
U24A
U34A
U34B
IOBI 15
IOBI 14
IOBI 13
IOBI 12
IOBI 11
IOBI 10
IOBI 9
IOBI 8
IOBI 7
IOBI 6
IOBI 5
IOBI 4
IOBI 3
IOBI 2
IOBI 1
IOBI 0
DEVICE FLAG
IOI-SC

Figure 9 shows the use of bits in the command code word.

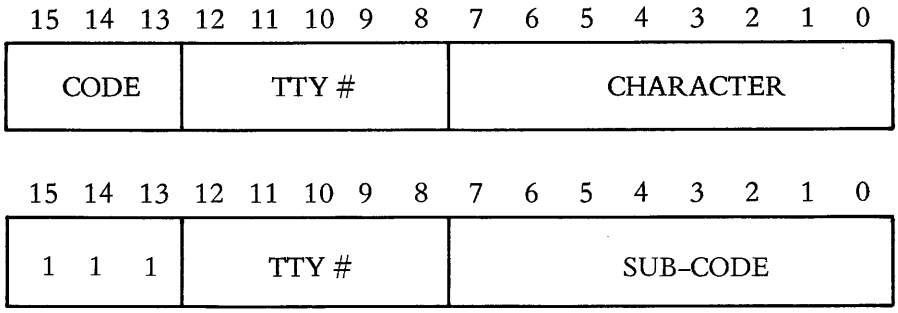


FIGURE 9. COMMAND CODE FORMAT

3-4 Command Initiation

The commands in this section are initiated by the System Processor. We would like to develop an awareness of the philosophy as well as an understanding of the actual hardware. Figure 7 shows the hardware block diagram for Inter Communications. The 4 processor interconnect boards are identical (only 2 shown). Each has standard Flag and Interrupt circuitry. Each has 16 input and 16 output lines.

The output data is latched in the FF's with an OTA or OTB instruction. The input data is available through the cable from the other processor. The Device Flag signal latches the data FF's as well as setting the Flag and IRQ circuits. The input data is available through a LIA or LIB instruction. Notice these boards are cross coupled. The output of one becomes the input of the other, and the Encode out becomes the Device Flag input to the other.

Let's back up now to get an over view of the system. The System Processor initiates these communication requests from various places: Scheduler, basic syntax check, syntax execution and library coding. The TTY number is combined with the request code. In the four cases in which data is required (OCR, STE, PHO, and INI) it is added to the request word. The data is output to the I/O card. The actual transfer takes place when the STC11,C is executed.

Only two commands require an answer in the 2000B (IBF and IPF also require an answer, but they are used only in the 2000C system). INI is easier to wait for than to provide coding to test its completion. It also determines that the Communications Processor is operating. GTC gets the next buffer character. The System Processor must wait until the character is available. It does so with a SFS11, JMP*-1. Now for all other commands the system can continue its processing. But it may be essential that the previous command be executed before continuing.

The Communications Processor sits in its idle loop except when servicing multiplexor (or phones). The communications interrupt may be held off by the multiplexor processing due to its lower priority.

TABLE 2

SYSTEM PROCESSOR TO COMMUNICATIONS PROCESSOR REQUESTS

MNEMONIC		CODE	DEFINITION	LISTING REFERENCE
System Processor	Communications Processor			
*OCR	(HTT)	000000	Output Character	P247/#20 L 146
*STE		020000	Start ENTER Timing	P101/#8 L 38
GTC	(GMA)	040000	Get Next Character	P185/#14 L 652
				P237/#19 L 338
				P246/#20 L 87
*PHO	(PHS)	060000	Phones Timing	P416/#33 L 389
BKS		100000	Backspace in Buffer	P184/#14 L 641
				P241/#19 L 557
				P246/#20 L 104
SBP		120000	Save Buffer Pointer	P26/#3 L 248
				P57/#5 L 22
			[(FBP) an alternate mnemonic for SBP]	P26/#3 L 248
				P58/#6 L 77
RBP		140000	Restore Buffer Pointer	P26/#3 L 263
				P58/#6 L 89
MIKRO		160000	Additional requests encoded using bits 0-4 as follows	
**INI	(INIF)	160000	Initialize System	P234/#19 L 162
UIR		160001	User Is Running	P62/#6 L 249
UNR		160002	User Not Running	P105/#9 L 210
IWT		160003	Input Wait	P110/#9 L 419
HUU		160004	Hang User Up	P303/#24 L 445
				P360/#29 L 64
ULO		160005	User Logged On – stop auto disconnect timing	P297/#24 L 154
ECO		160006	Echo On	P303/#24 L 442
				P337/#27 L 80
ECF		160007	Echo Off	P337/#27 L 78
TPO		160010	Tape Mode On	P240/#19 L 493

* bits Ø-7 contain an output character

** bits Ø –4 contain subcode

TABLE 2 (Cont)

SYSTEM PROCESSOR TO COMMUNICATIONS PROCESSOR REQUESTS

MNEMONIC		CODE	DEFINITION	LISTING REFERENCE
System Processor	Communications Processor			
ILI		160011	Any Illegal Input	P238/#19 L 378
NUC		160012	New User Called	P295/#24 L 45
KAO		160013	Kill All Output	P359/#29 L 30
ALI		160014	Allow Input (LF) syntax tape mode	P54/#5 L 381 P237/#19 L 341
OWT		160015	Output Wait	P248/#20 L 188
FAS		160016	Fast Terminal	P417/#33 L 440
SLO		160017	Slow Terminal	P419/#33 L 458
IBF		160020	Is Buffer Full	***
IPF		160021	Is Port Fast	***

*** These two commands are used in the 2000C only.

We can now understand the command initiation block diagram in Figure 10. The request word is made up of the code, the teletype number and the data character if necessary. This is all accomplished within the initiating routine. It then transfers to the S14SH routine for the actual communications.

It may be necessary to wait for the acknowledgement of the previous request. There is a little house keeping necessary to allow for this wait. Flag ∅ is cleared to hold off interrupts. The A and B registers are saved. The Scheduler is blocked allowing time up-date but no new entry to the scheduler from the Time Base Generator. Now the prior acknowledge is checked. The system waits until this acknowledgement arrives. The Flag ∅ is set to allow interrupts during this potential wait. The Communications Processor responds with a STC 13,C. This Encode signal acts like a device flag to the board in SC 11. The System Processor tests with a SFS 11, JMP*-1.

When the acknowledgement is available the System Processor sends the current code with an OTA 11, STC 11,C. The OTA places the data in the output register. It is immediately available to the Communications Processor board. The STC gives the Encode. This Device flag to the Communications Processor latches the data in the Input register, and initiates an interrupt to select code 12. The System Processor then clears the Control on select code 12. This is done to prevent an interrupt. The only command requiring an immediate answer is the GTC. This is awaited with an SFS 11, JMP*-1. The others are not critical so long as they are accomplished before the next System Processor request.

The B register is restored. The entrance to the scheduler is restored. The program returns to the initiating program.

The Communications Processor responds to the communications request interrupt and saves its registers. It determines the TTY number. It determines the request and the starting address of the actual request servicing routine. It acknowledges the completion of the System Processor and restores the registers. It then returns to the point of execution at the time of interrupt. This will typically be the idle loop or phones routine. The multiplexor is usually executed with the Interrupt flag cleared to prevent interrupts.

The next section provides written descriptions and flow charts for each of the System Processor requests.

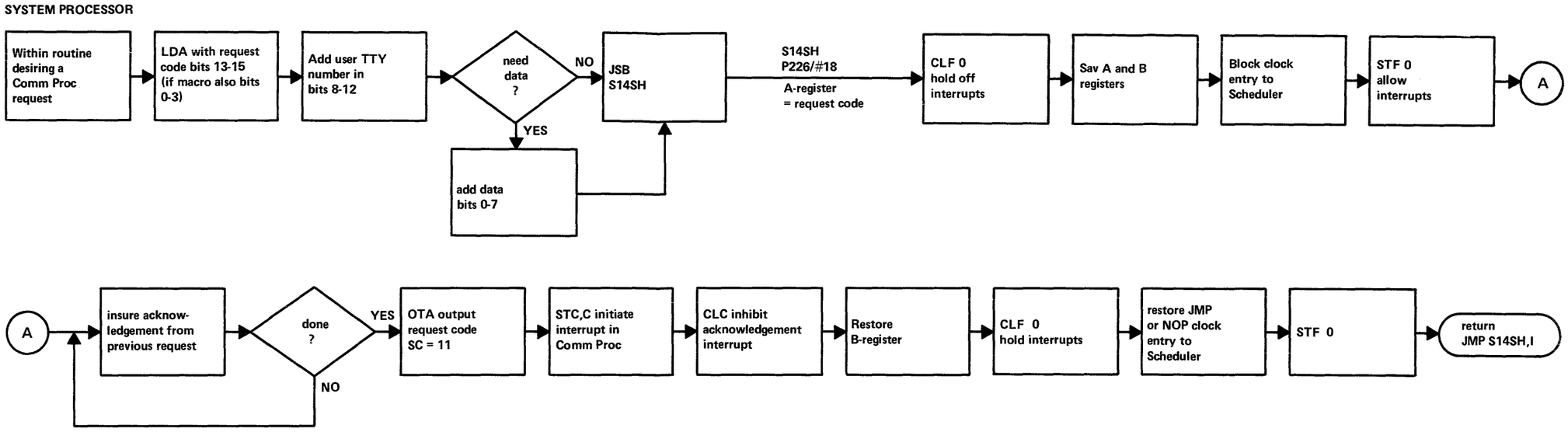


FIGURE 10. COMMAND INITIATION (SYSTEM PROC. TO COMM. PROC.)

3-5 Command Definitions System Processor to Communications Processor

OCR – Output a Character

This command is initiated from numerous locations in the System Processor software. It is necessary for all output to the user including Basic program execution, error messages and command execution. The actual character to be transmitted is placed in bits 0–7 of the request code word.

The Communications Processor service routine determines whether the user is already set up in output mode by the bit in IOTOG. If so it checks for buffer full condition. It initiates the BFL for a full buffer condition. This results in an output suspension by the System Processor. It then updates the CCNT by adding a negative 1. It checks for buffer wrap around condition. It then places the character in the TTY buffer and updates the BSTR pointer. For an initial output character it must insure no input is currently underway. It does this by looking at the LADDR entry for an ISZ entry. It allows either 20 or 100 interrupts to insure adequate sync time for the TTY. (The rotor must be in stop position before starting the next data character). The various TTY table entries are initialized and the character is appended to the buffer.

STE – Start ENTER Timing

When an ENTER command is being executed the maximum response time is specified. This specified value is transmitted through the request code bits 0–7. It is placed in the TTY table entry ATIM. Its 2's complement form is placed in TIMO. The value of TIMO entry is incremented during phones routine. A comparison of TIMO and ATIM at the input carriage return gives the response time. A rollover of TIMO before the response carriage return indicates time out condition.

This request also sets the ENTER timing bit and removes the No Input Allowed bit from the user Status entry.

GTC – Get the Next Character

The System Processor initiates a request whenever it requires the next character from the TTY buffer. After initiating the request the System Processor waits on a SFS Select Code 11.

The Communications Processor services the request by getting the next character and outputs the data through the processor interconnect boards. The Communications Processor then updates the BHED pointer, including buffer wrap around if necessary. In the CMRTN routine the Communications Processor issues the STC, 12B,C. This encode signal latches the new System Processor input character and sets the flag the System Processor has awaited.

PHO – Phones Timing

The phones servicing is handled by the Communications Processor. The log on time limit is established by the system operator. This new value is converted to one-tenth seconds and stored in the 2's complement form. The phones routine is entered ten times per second (88 multiplexor interrupts).

BKS – Backspace the Buffer Pointer

The System Processor sometimes requires that the buffer pointer BHED be backspaced. The Communications Processor decrements the pointer after taking care of possible buffer wrap around.

A good example of the backspace command occurs in the scheduler. The input line is checked for a null line, syntax, invalid command or valid command. If the line is syntax this is determined by the first character lying between ASCII 60 and ASCII 71. Now the user is scheduled for Syntax and the buffer pointer is backspaced to the beginning of the full line.

SBP – Save Buffer Pointer

The BSAV entry points to the beginning of the current input line being processed. The BHED is advanced through the character string pointing to the current character being processed. On occasions it is necessary to reset BHED to the beginning of the line (refer RBP request).

The function of BSAV was performed by a location in the Swap area for the 2000A. Now it is more convenient to provide in the Communications Processor.

RBP – Restore Buffer Pointer

This request allows the Communications Processor to reset the value of BHED to BSAV. The Basic Syntax coding requires a different technique in evaluating a GO TO absolute value compared to a computed GO TO formula. The Syntaxer approaches this as a branching problem. After determining the type it restores the buffer pointer and continues with the statement processing. The other times the Restore Pointer is used occur in GO SUB and multicharacter symbol table search.

INI – Initialize System

When the Communications Processor program is loaded and initiated at starting address = 2 certain conditions are established. The program then reaches the idle loop and remains there except when interrupted out for multiplexor servicing, communications from the System Processor or power fail.

When the System Processor is initiated from paper tape load or reloaded from disc or mag tape sleep it commands the INI Initialize Communications Processor system.

The initialize program when started at starting address = 2 resets all users to 10 cps, and resets the phone log on time constant to 2 minutes. It then proceeds at INIT P61/#5. When the System Processor sends the request the fast ports are not changed and the phone log on timing is not changed, but the actual number of allowable ports are set up in the corresponding Ignore IG and IG1 words. At this point both initialization programs continue at INIT.

The INIT program sets up Control FF's on the multiplexor boards and send channel. It clears Control on the receive channel. It establishes base page words for input flag, multiplex output stop bits, and phone data. It allows power fail interrupt.

The teletype table entries are established. These include the entries associated with the TTY buffer pointers, and status.

When a Time-Share system is up and running and the Communications Processor program is restarted at starting address 2 additional overhead may be introduced into the system.

This occurs when not all 32 users are in use. It is especially noticeable when only one multiplexor board is installed. This is due to clearing all the Ignore bits. The multiplexor board inverts so that all inputs are high when no mpx panel is connected, or no user terminals are connected. But when no mpx board is installed all inputs are low. These look like start bits and require mpx processing.

UIR – User is Running

This command is sent when the program is being compiled for program execution. It prevents all user input except abort.

UNR – User Not Running

At the completion or termination of program execution the run bit in the status word is cleared and No Input Allowed bit is cleared allowing any input (not just abort).

IWT – Input Wait

The execution of an INPUT or ENTER statement requires a very substantial amount of time. A single character and carriage return requires 0.2 seconds (at the 10 cps rate). This time is so large compared with the overhead required to swap out and in again that the system always suspends. The status word is changed to allow the necessary user input. The carriage return initiates the rescheduling on the queue.

HUU – Hang User Up

This request removes the user from Run status, and sets bit 7 indicating a hang up is desired. The hang up is performed by the phones logic. The command is initiated by the user with the BYE command, or by the system operator with the SLEEP command.

ULO – User Logged On

This command is initiated by the HELLO library routine which indicates the user satisfactorily logged on and has time available.

If this were not cleared in time it would result in a disconnect signal to the phones board. It does not affect hard wired terminals.

ECO – Echo On

The Echo bit PLEX is used by the multiplexor to determine whether the output multiplexor data is updated for this user. This command resets the corresponding bit. This results in all incoming data bits being sent back to the users terminal. The 2749A Teleprinter requires this data for the character to be printed locally, thus the Full Duplex mode is normally required.

ECF – Echo Off

This command removes the users bit from the PLEX word. This bit is used by the multiplexor to determine whether the incoming data bits must be sent back to the terminal.

The TBX equipment (teleprinter and telephone networks) conserves phone band-width by printing the character locally and thus avoiding the requirement for the returned signal. Echo Off is primarily used with this class of terminal.

TPO – Tape Mode On

This command sets the status bit indicating tape mode. Tape mode is a special multiplexor operating condition. It is used to load Basic source programs through the TTY reader.

This allows the character inputs to continue while the system schedules and processes the input lines. The TTY buffer is used as a wrap around buffer. This allows multiple input lines in the buffer at any time. A primary difference is that all error messages are suppressed until the Tape mode is exited (by KEY or some other command).

ILI – Illegal Input

This request is sent whenever the scheduler determines the user is in tape mode and a valid command is encountered. The Communications Processor determines whether the buffer still contains data or the reader is still inputing data. If either of these conditions are true the I/O processor computer responds with a "1" to the System Processor. The System Processor then must call its error routine.

If, however, the Communications Processor finds nothing in the buffer and no current input it clears the tape mode status bit and returns a "Ø" to the System Processor. The System Processor then clears its tape mode bit, tests for tape errors and continues. This condition normally occurs when the tape reader is off and the user types KEY.

NUC – New User Called

This request is initiated by the HELLO library routine. It is used to insure the log on timing with a dataphone. No such maximum time is necessary with a hard wired terminal. This feature prevents a "housewife call" from tying up the dataphone lines. The coding sets the log on status bit, and places the log on time limit value in the TTY table PHON entry.

KAO – Kill All Output

This request originates in the SLEEP routine, and for Break servicing. Its purpose is to discontinue the normal output of an individual user. For SLEEP execution the System Processor outputs the Sleep message, then sequentially KAO's each user.

ALI – Allow Input

This request is called from the scheduler whenever the user is in tape mode and a carriage return is encountered. It is also called from syntax when an input statement processing is done. This provision is useful in providing more efficient servicing to the user in tape mode. Because of the potential delays in servicing user multiplexor input the TTY buffer may contain multiple input lines.

Multiple lines (i.e., at least one full line remaining) are evident because BSTR which points to the beginning of the current line and BHED which points to the beginning of the earliest unprocessed line will be different.

The Communications Processor initiates a HVL command to the System Processor which will have started routine scheduler processing. This will enable the System Processor to continue processing subsequent lines.

OWT – Output Wait

The System Processor output character routine handles the communications to the Communications Processor for each character appended to the output TTY buffer. When the buffer fills up, the Communications Processor responds with BFL, buffer full command. This sets the buffer full bit in the users FLAG TTY entry. The next time the output character routine is called it determines that the flag bit was set. It now requests the OWT to the Communications Processor. If the output buffer still has 10 or more characters the user is suspended, and the Communications Processor status word sets bit 1 indicating a suspension took place. The user is rescheduled when the buffer reaches exactly 10 remaining characters. OWT also is used by CAT, DIR and other library programs to suspend with a pseudo output wait.

FAS – Fast Terminal

The FAF and FAF1 words are used in the multiplexor to select -2 or -4 to the middle of the start bit, and -4 or -8 for the bit to bit time. This request is initiated by the FAST library routine (console operator command). Note that all ports are changed to slow when the Communications Processor program is begun at starting address = 2.

SLO – Slow Terminal

This command is initiated by the system operators SLOW command. It sets the corresponding users bit in the FAF or FAF1 words. This establishes the timing constants for 10 cps terminals.

IPF – Is Port Fast

This request instructs the Communications Processor to check the corresponding users bit in FAF or FAF1. A zero implies a fast port (220 baud); a non-zero indicates a normal terminal speed (110 baud). The result is returned to the System Processor. This command is used in the 2000C.

IBF – Is Buffer Full

This request is used by the System Processor for Announce command execution to determine whether the output buffer is full. Refer to figure 4 for the use of buffer pointers for output mode. The CCNT contains the number of characters in 2's complement form. The buffer length in characters (300) is added to the value of CCNT. The actual multiplexor routine considers 299 as a full buffer just in case another character is being processed which must be appended. The IBF routine then subtracts 2. If the result is negative the buffer is, indeed, full. The zero (not full) or one (full) is sent back to the System Processor. This command is used in the 2000C.

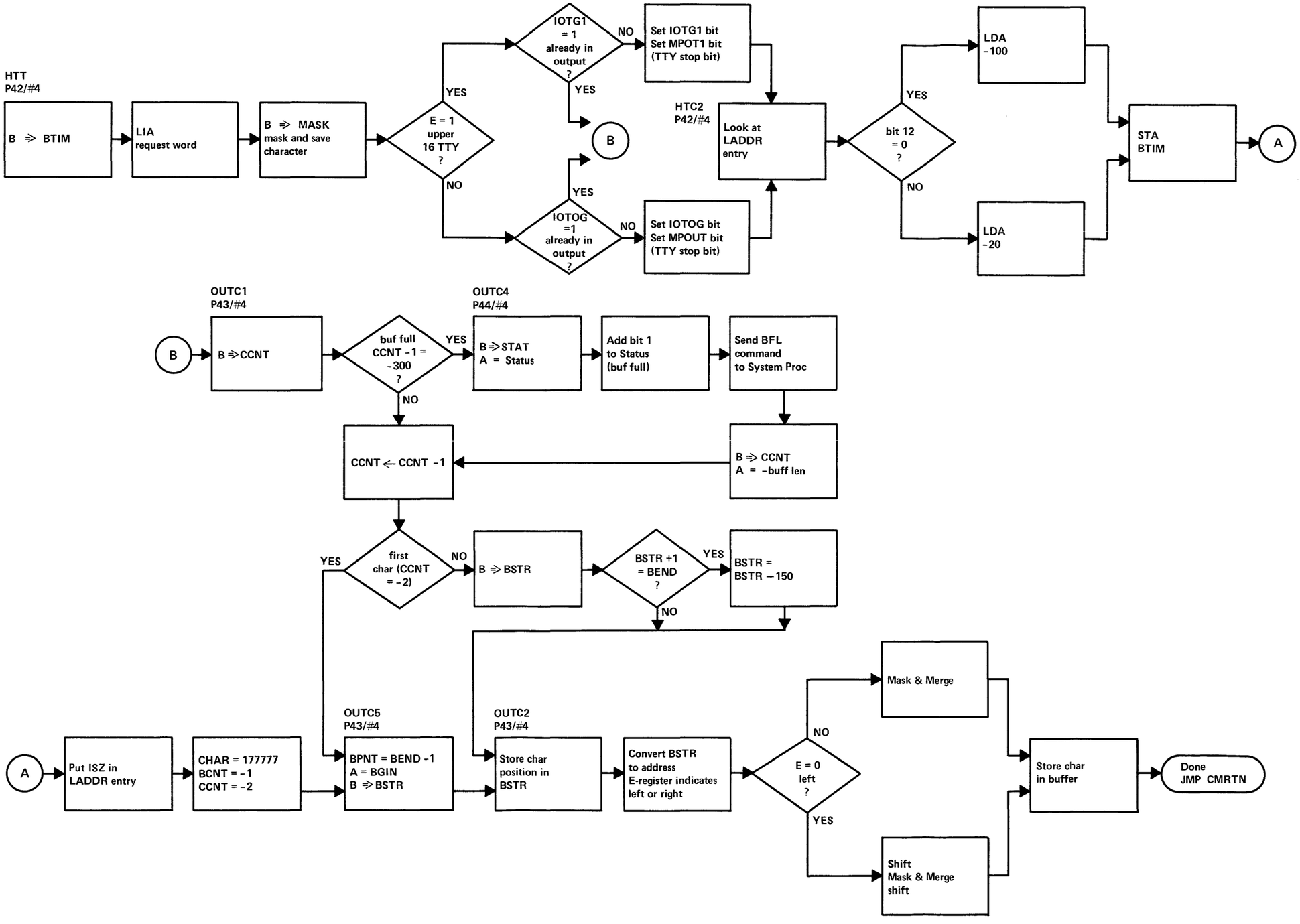


FIGURE 11. OCR OUTPUT A CHARACTER

P45/#4

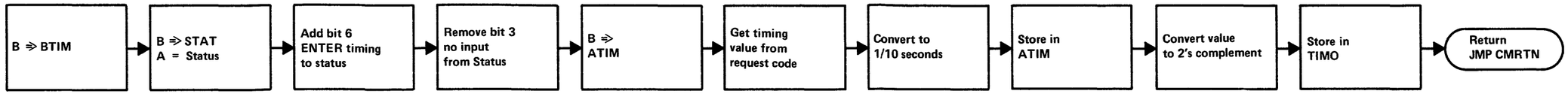


FIGURE 12. STE START ENTER TIMING

P46/#4

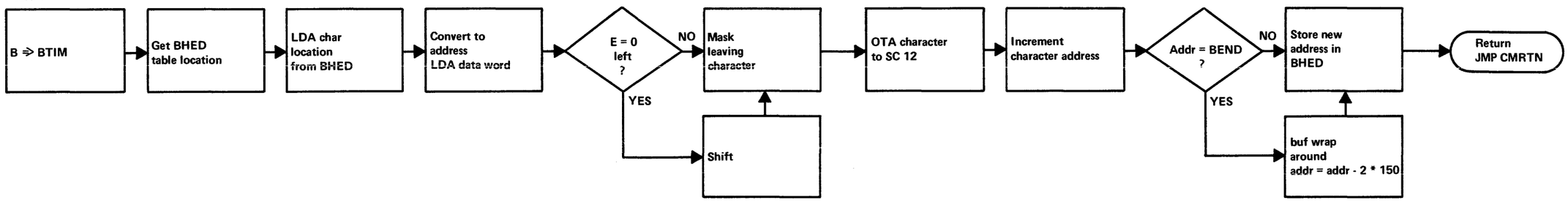


FIGURE 13. GTC GET NEXT CHARACTER

PHS
P46/#4

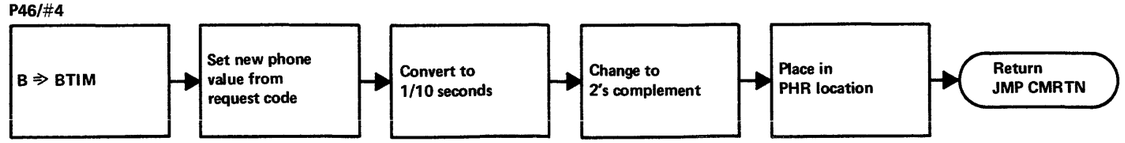


FIGURE 14. PHO PHONES TIMING

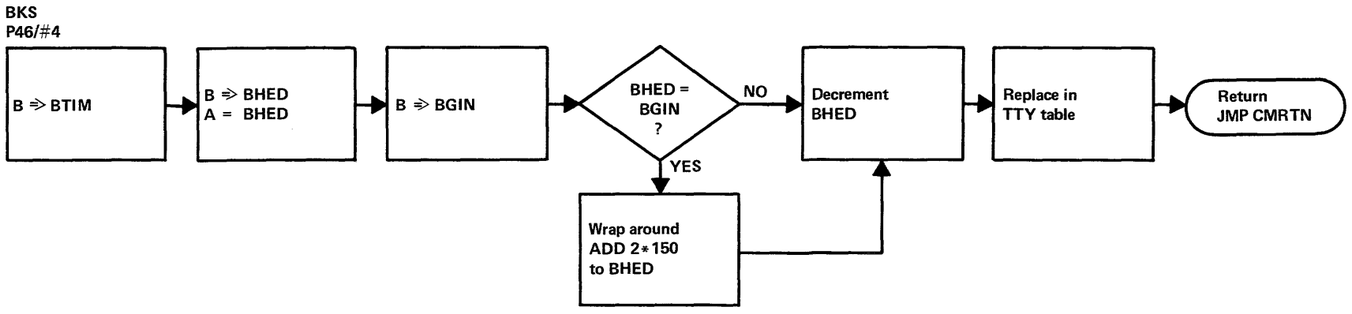


FIGURE 15. BKS BACKSPACE BUFFER POINTER

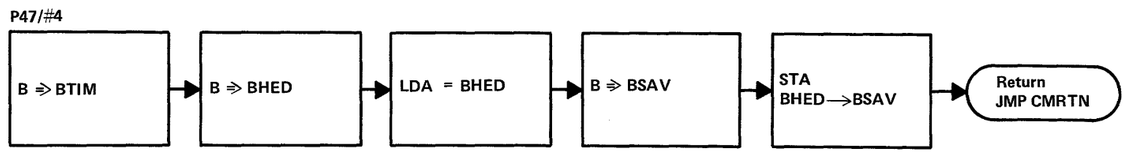


FIGURE 16. SBP SAVE BUFFER POINTER

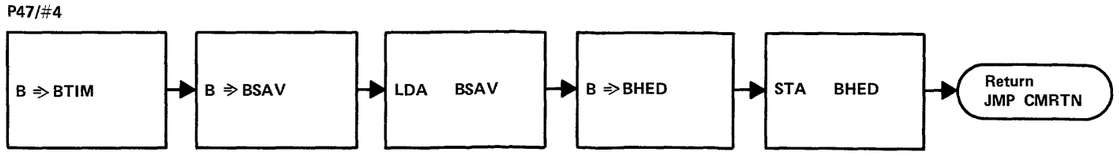


FIGURE 17. RBP RESTORE BUFFER POINTER

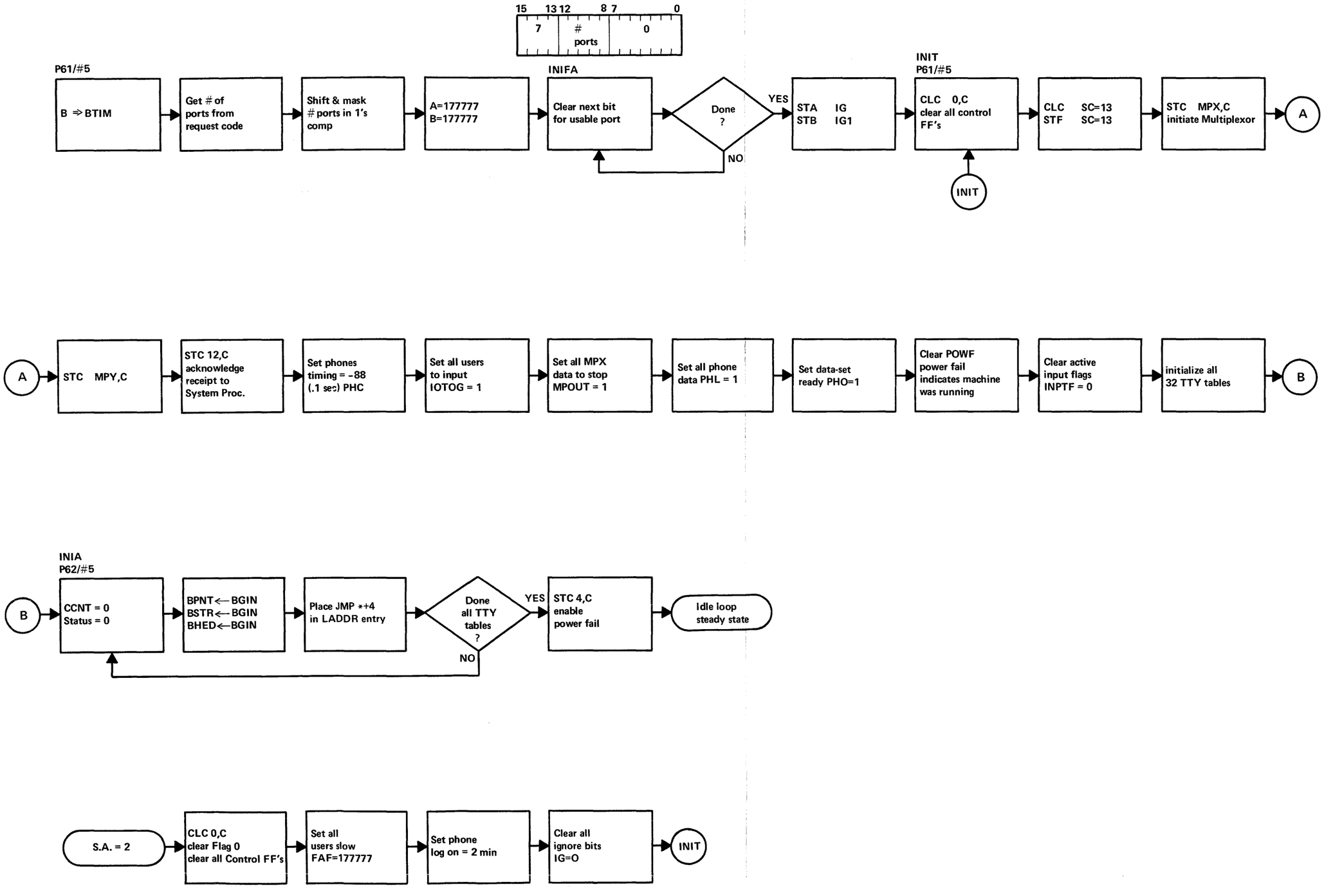


FIGURE 18. INI INITIATE SYSTEM

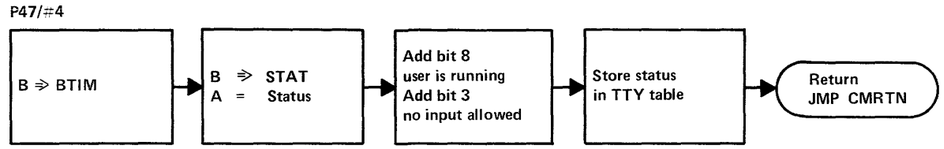


FIGURE 19. UIR USER IS RUNNING

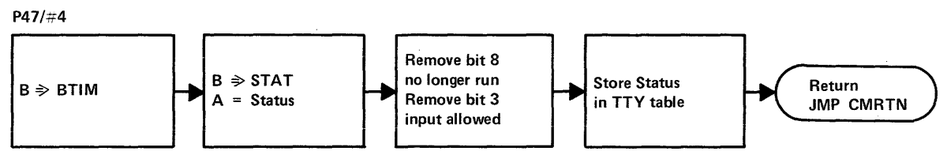


FIGURE 20. UNR USER NOT RUNNING

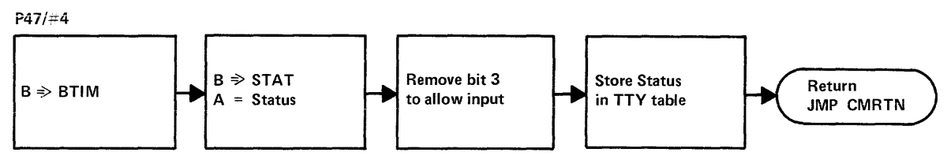


FIGURE 21. IWT INPUT WAIT

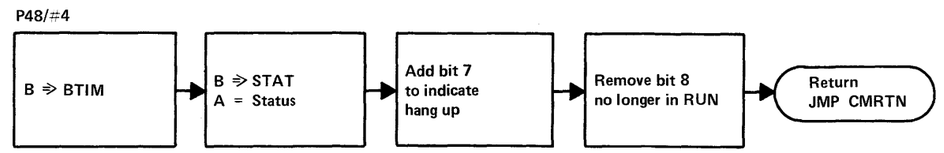


FIGURE 22. HUU HANG USER UP

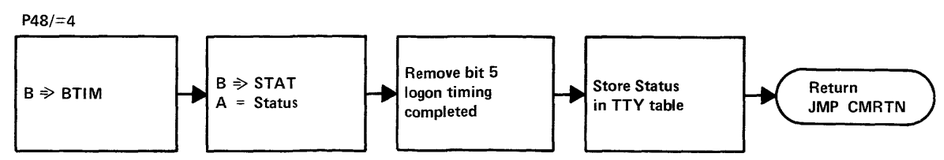


FIGURE 23. ULO USER LOGGED ON

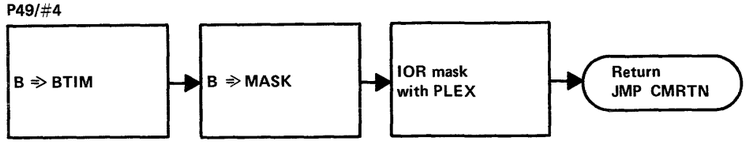


FIGURE 24. ECO ECHO ON

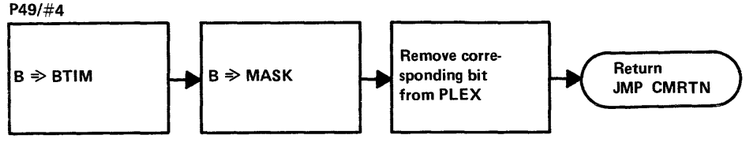


FIGURE 25. ECF ECHO OFF

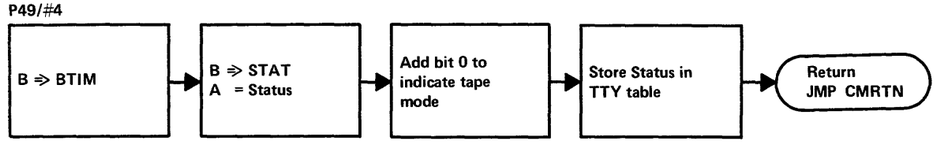


FIGURE 26. TPO TAPE MODE ON

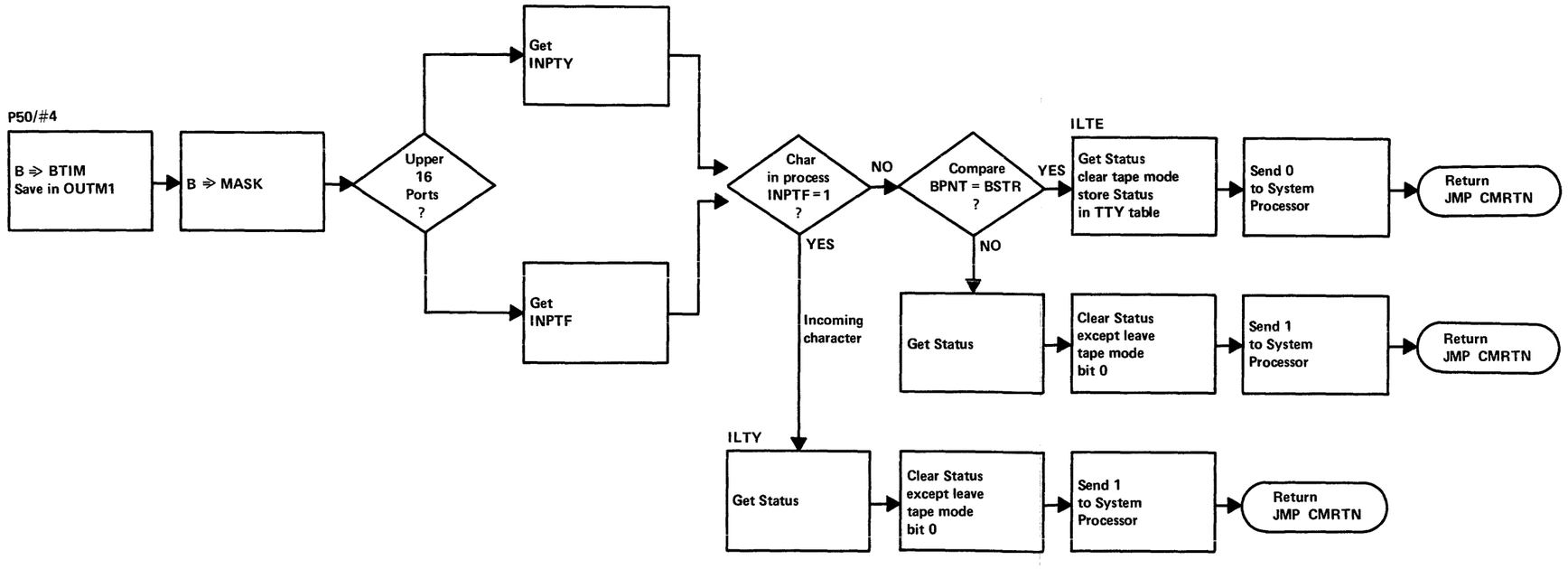


FIGURE 27. ILT ANY ILLEGAL INPUT

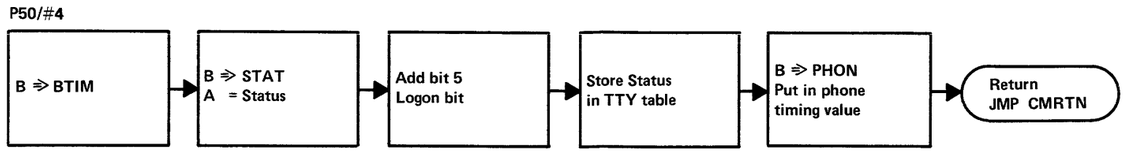


FIGURE 28. NUC NEW USER CALLED

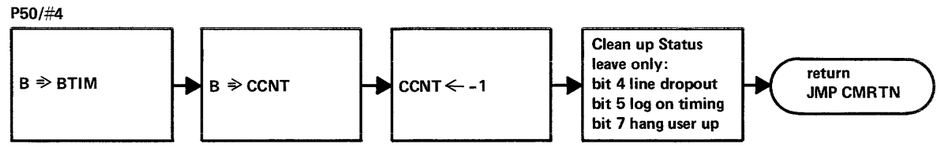


FIGURE 29. KAO KILL ALL OUTPUT

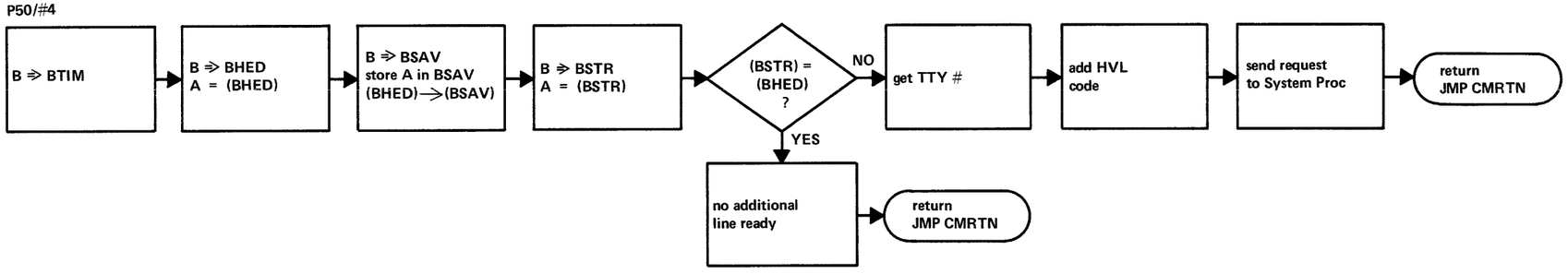


FIGURE 30. ALI ALLOW INPUT

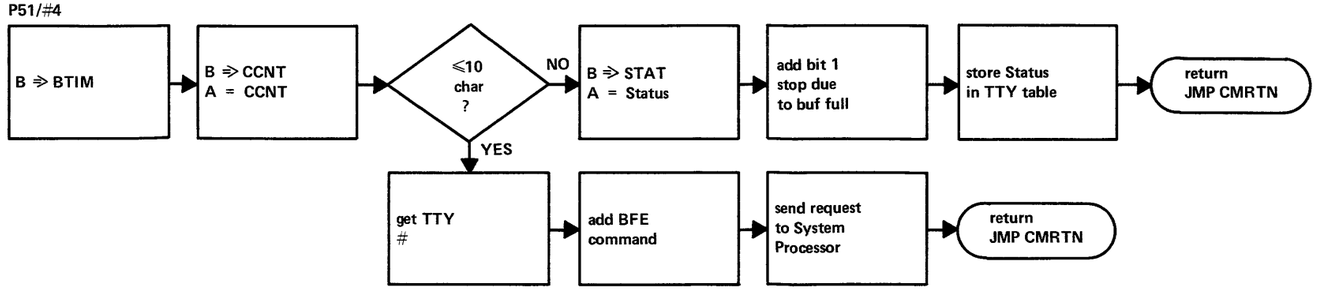


FIGURE 31. OWT OUTPUT WAIT

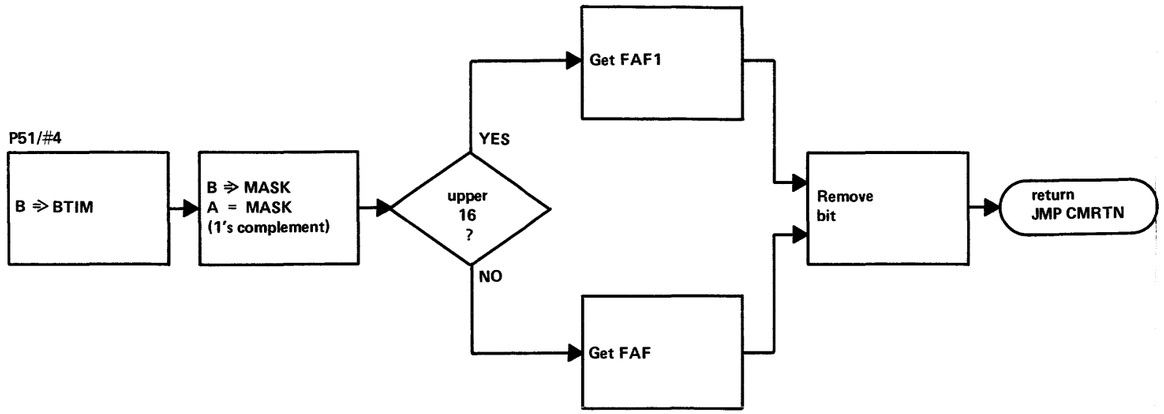


FIGURE 32. FAS FAST TERMINAL

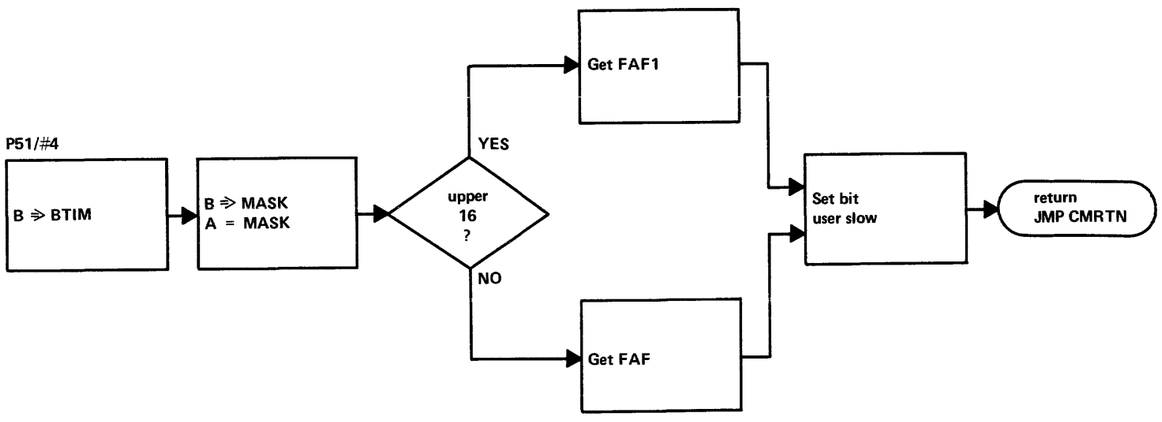


FIGURE 33. SLO SLOW TERMINAL

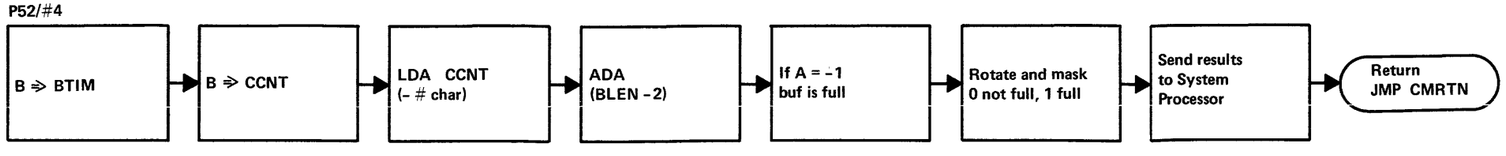


FIGURE 34. IBF IS BUFFER FULL

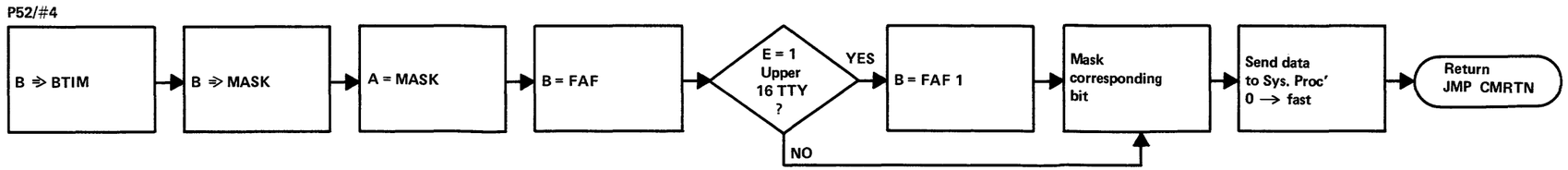
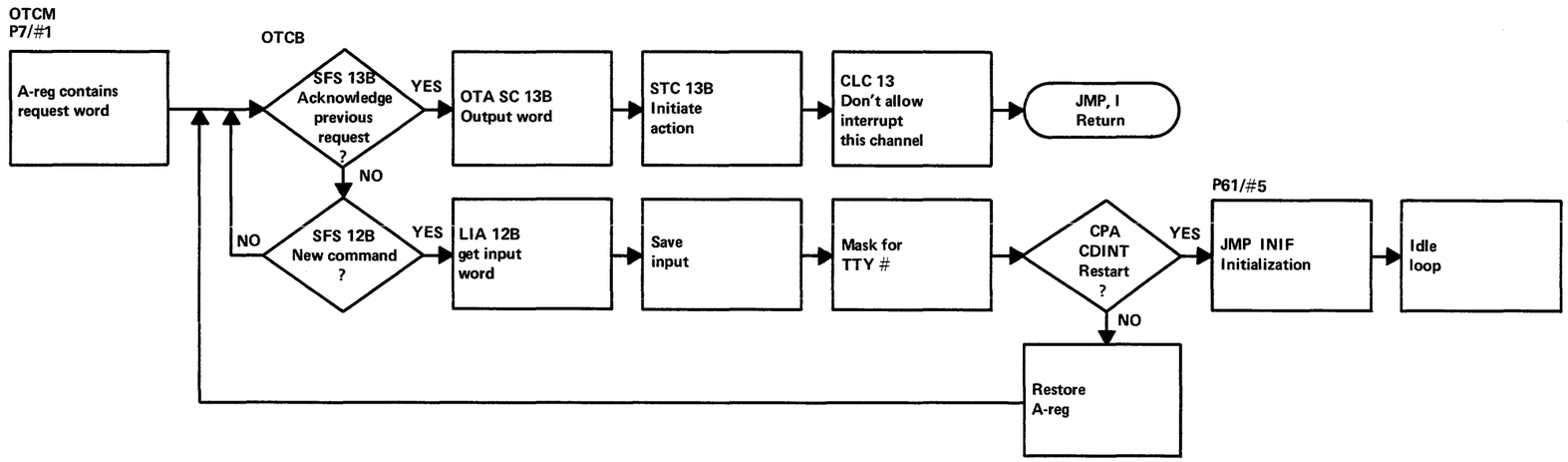


FIGURE 35. IPF IS PORT FAST



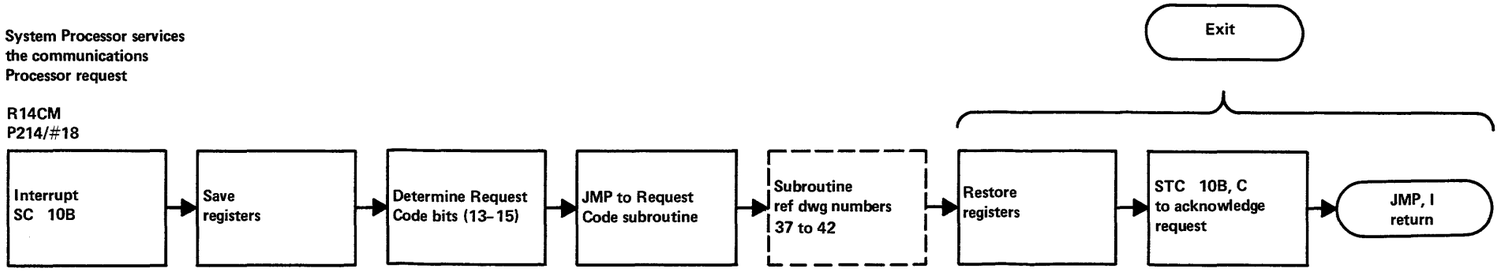


FIGURE 36. COMMUNICATIONS PROCESSOR REQUESTS TO SYSTEM PROCESSOR

3-6 Communications Processor to System Processor Command Initiation

The communications request initiated by the Communications Processor is handled as in the System Processor requests. Refer to figure 36. The request word contains the request code and the teletype port number. Only HVL contains a data character (in answer to an ENTER statement) and none requires a data response.

The Communications Processor checks that the previous request had been serviced (by checking the flag); it awaits the flag if not already acknowledged. It outputs the request to select code, and sets the Control and Encode FF's. It then clears the Control to prevent an acknowledgment interrupt.

The System Processor gets the interrupt on select code 1Ø. It determines the user TTY number. The request code determines the starting address of the service subroutine. In most cases a flag bit is changed in FLAG word and sometimes a status change is involved. Upon completion of servicing the System Processor acknowledges by STC 1ØB,C. This sets the flag on 13 in the Communications Processor.

The requests are summarized in Table 3. The individual flow chart and description follow.

3-7 Command Definitions Communications Processor to System Processor

HVL I have a line

This request indicates that a user has typed an input line terminated with a carriage return. This indicates to the System Processor that servicing is required. The System Processor has information in the user's FLAG and STAT words to determine the nature of the input line.

When the input is in response to an ENTER statement the request word contains the appropriate response time.

For normal input the Communications Processor ceases to respond to the user until the System Processor handles the line and sends the line feed.

This request may also be generated in tape mode in response to the System Processor ALI. The ALI signifies completion of a syntax line and asks if additional input lines exist in the TTY buffer.

TABLE 3

COMMUNICATIONS PROCESSOR TO
SYSTEM PROCESSOR REQUESTS

MNEMONIC	CODE	DEFINITION	LISTING REFERENCE
HVL	000000	I Have A Line	P32/#3 L 224 P39/#3 L 600 P51/#4 L 370
ABR	020000	User Aborted	P19/#2 L 154 P23/#2 L 322
BFL	040000	Buffer Is Full	P44/#4 L 122
BFE	060000	Buffer Is (Almost) Empty	P34/#3 L 374 P41/#3 L 750 P51/#4 L 382
ETO	100000	ENTER Statement Timed Out	P/58/#5 L 242
UHU	120000	User Hung Up	P60/#5 L 356

ABR User Aborted

Abort is a change of mind. After the user has started some action he then discontinues its execution by holding the Break key for >0.11 second (88 interrupts). Abort from a Run or List is easy so long as syntax compiling or decompiling is not taking place. The system must prevent leaving a track of debris along the way.

Certain operations may not be discontinued because they would result in unacceptable internal form. The System Processor sets FLAG bit 4 (called UNABT) when abort is not allowed.

When the UNABT is clear and status indicates syntax is not taking place and the executing condition is not a library program the abort can be accomplished. The Communications Processor communication bit is set and the status is changed to indicate the start of abort.

The only library programs which can be aborted are Library and Catalog. Notice neither of these change the internal system or representation. When abort is not possible an abort try bit is added to the FLAG word. When the non-abort condition is cleared the abort is processed.

BFL Buffer is Full

The Communications Processor processes the output characters from the System Processor. When the buffer fills up then BSTR = BPNT-1. At this point the Communications Processor sends the BFL request. It results in setting the FLAG bit 3 indicating an output wait is required.

The System Processor continues to process the user. If another output character is required then the user is immediately suspended.

Note that by stopping at BSTR = BPNT-1 an additional character in process can still be handled.

BFE Buffer (almost) Empty

The Communications Processor keeps check on the number of output characters in the buffer. When the number reaches -10 and the user has been placed in output suspension the Communications Processor initiates this request. The System Processor requeues the user to resume the program execution.

ETO ENTER Statement Timed Out

The timing for the ENTER statement is handled by the phones routine. When the Communications Processor answers the normal ENTER line with HVL it includes the response time as calculated from ATIM and TIMO. In the case where the allowed time is exceeded the TIMO value rollover occurs. The System Processor requeues the user for service and sets the status to -3 to indicate the response time failure.

UHU User Hung Up

The active phone user initiates the connection with a ringing signal from the data phone. The data terminal signal retains the connection. The data phone responds with carrier signal. This carrier signal remains as long as the connection remains. It disappears if the user hangs up, gets an inadvertent disconnect, or due to noise glitches on the phone line.

The phone routine senses the failure in the phone input data and begins a 2 second counter to test for hang up. Rollover of this counter is interpreted as a hang up and the system treats it like a BYE command. The System Processor requeues him for service and sets his status to -2 for disconnect.

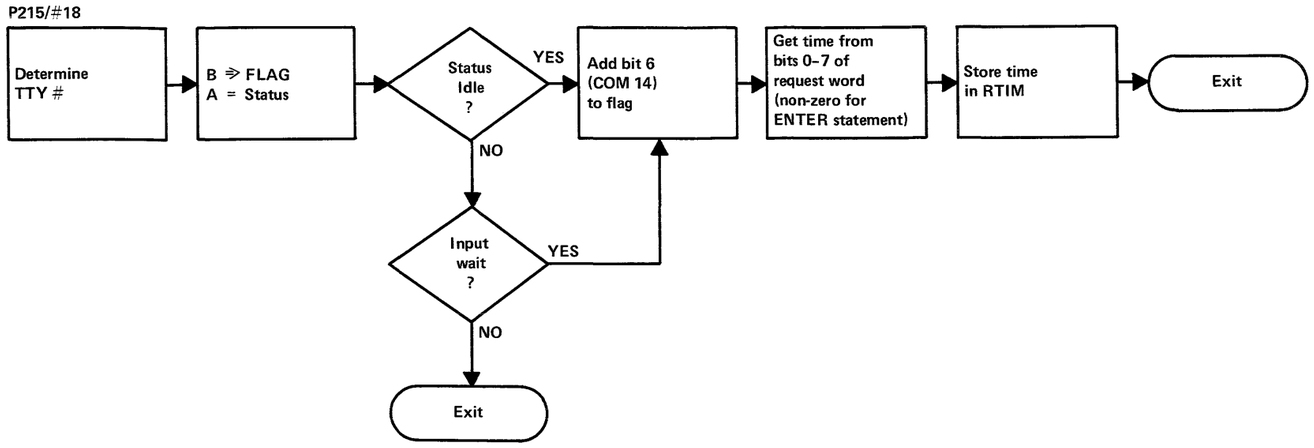


FIGURE 37. HVL I HAVE A LINE

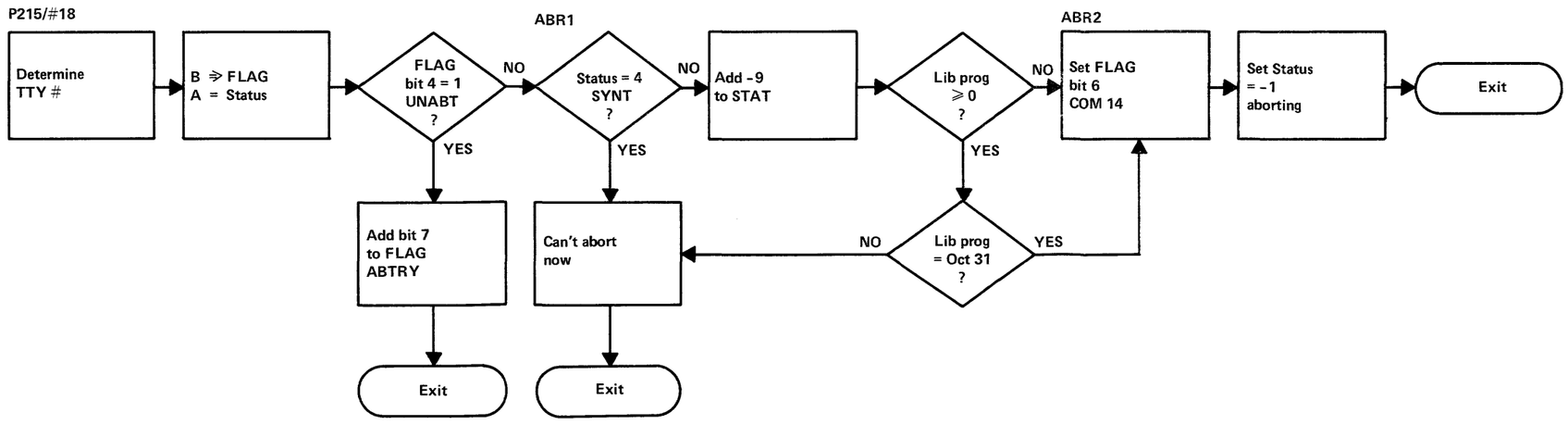


FIGURE 38. ABR USER ABORTED

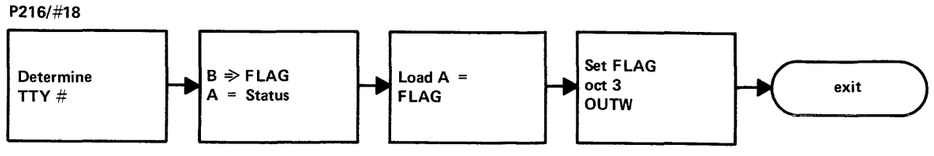


FIGURE 39. BFL BUFFER IS FULL

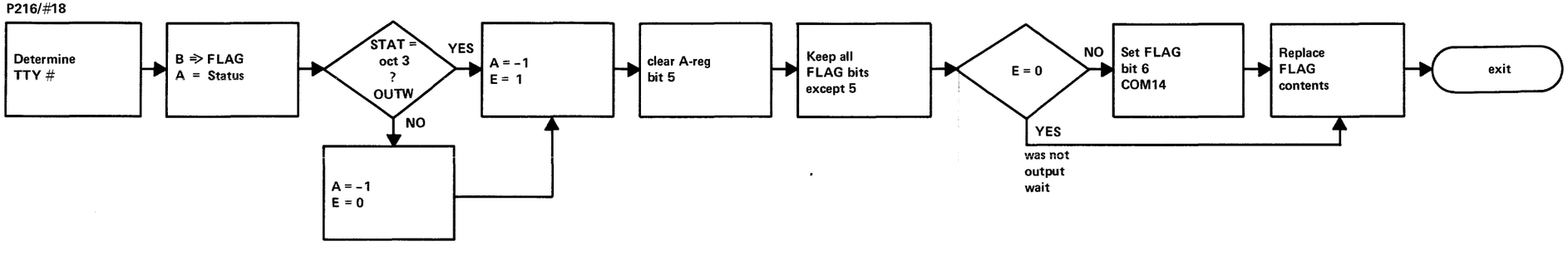


FIGURE 40. BFE BUFFER IS (ALMOST) EMPTY

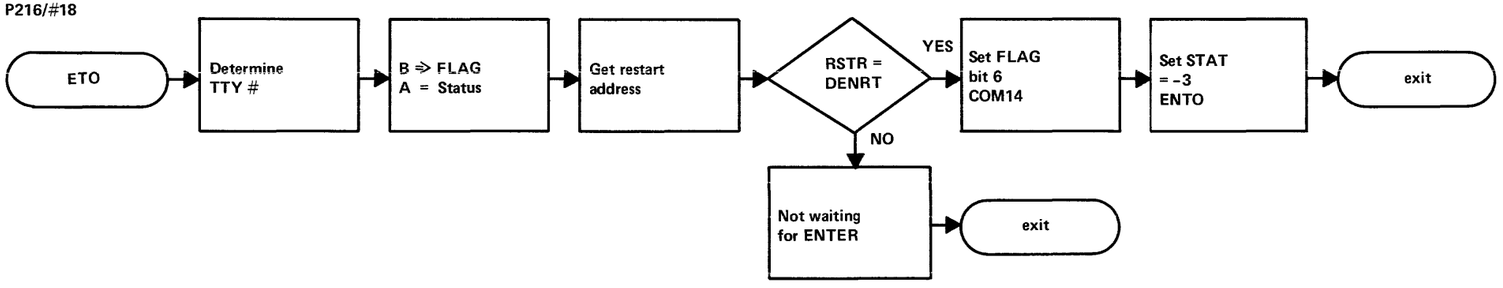


FIGURE 41. ETO ENTER TIMED OUT

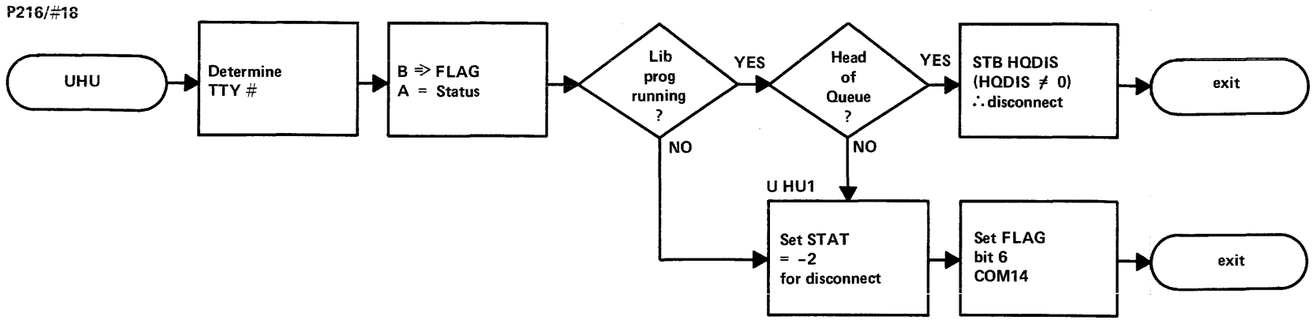


FIGURE 42. UHU USER HUNG UP

System Processor Functions

IV

CHAPTER 4

SYSTEM PROCESSOR FUNCTIONS

4-1 Hardware Configuration (2000B)

Table 4 lists the minimum hardware required for the HP 2000B. The specific board locations are shown for the 2116B/C for the System Processor, and the 2114B for the Communications Processor. The 2766A Disc is listed although the 2773 or 2774 would also be suitable. Normally at least 700,000 words of memory is required for a minimum system.

The Phone boards and Multiplexor Data boards are all shown. Their position is fixed if installed. If the Multiplexor in select code 11 is not used a priority jumper must be installed in its place. The Phones board in SC 14 (if installed) works with the Data board in SC 10. The Phones board in SC 15 (if installed) works with the Data board in SC 11.

Figures 43 and 44 show the board locations for the 2116B and 2116C computers. Notice not all boards are required.

The condition of the various switches are the same as described in HP 2000A TSS Sections 2-2, 2-3, and 2-4: Power Fail Switch up for restart, Parity switch up for halt, and Disc Data switch down for unprotect.

Certain optional hardware devices are available. These include various magnetic tape units, the Telephone Auto Disconnect and the CRT Display Terminal. These devices are listed in Table 5.

In addition to the optional hardware in Table 5 a wide variety of Disc/Drum units are available. They are useful for the addition of Drum capacity, or as an alternate choice for the intial system. Table 6 gives reference data for the various Fixed Head Discs which may be used on the system.

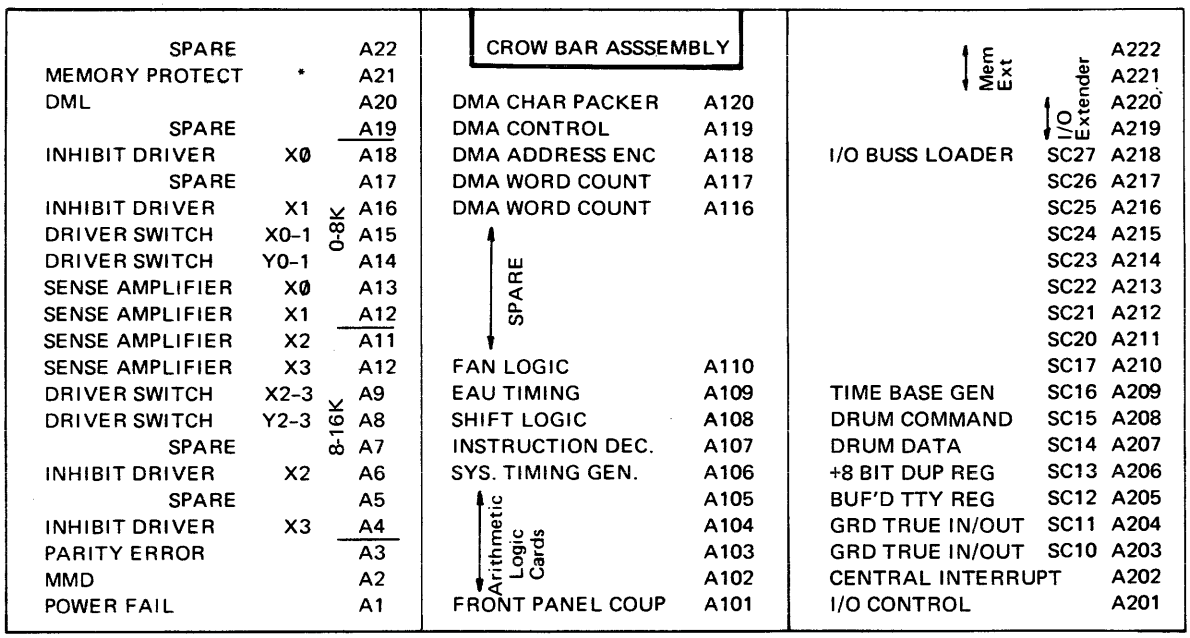
The characteristics of the 2766A Disc and 2773A, 2774A and 2775A Drums are identical from the system standpoint. These include available capacities, data transfer rate and addressing.

It is sometimes helpful to observe data on the Fixed Head Disc or Drum. This may be desirable when troubleshooting the system, for studying the internal representation, or for batch access to the files.

TABLE 4.

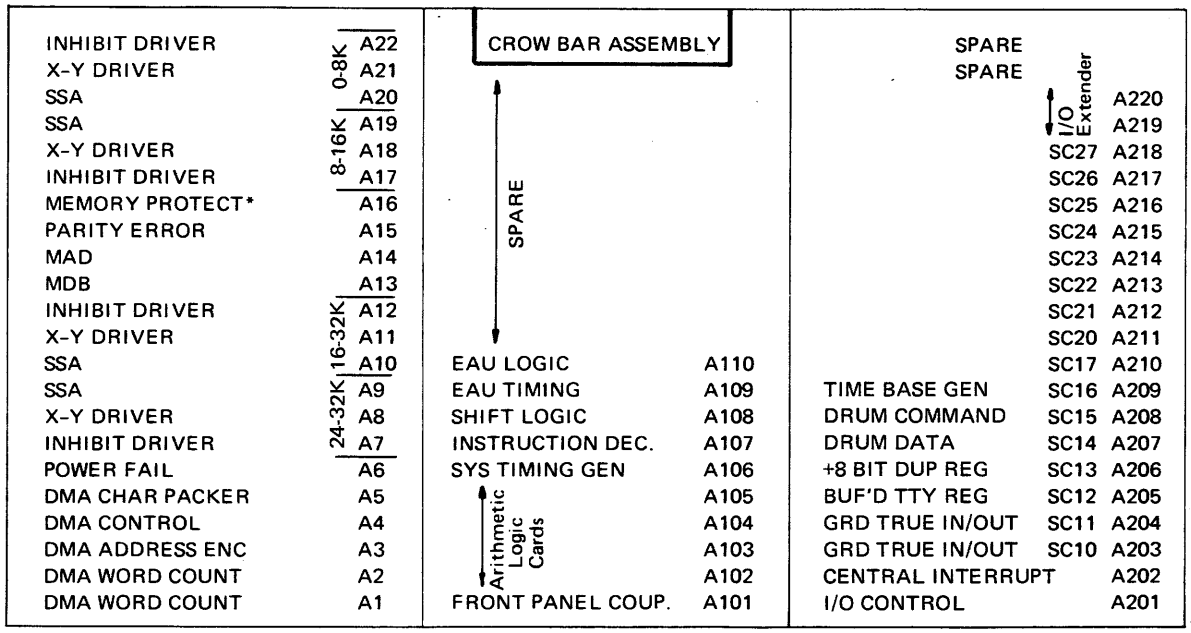
2000B MINIMUM HARDWARE CONFIGURATION

HARDWARE GROUP	MODEL NUMBER	NAME	BOARD STK NO.	COMMENTS	LOCATION
SYSTEM PROCESSOR					
COMPUTER	2116B/C-005	16K MEMORY			
PROCESSOR OPTIONS	12578A	DMA	02116-6206	DMA REG.	
			02116-6205	ADDR ENC.	
			02116-6204	DMA CONTROL	
			02116-6203	CHAR PACKER	
	12579A	EAU	02116-6196	TIMING	
			02116-6202	LOGIC	
	12588A	POWER FAIL	12588-6001	(SW UP-RESTART)	
	12591A	PARITY CHECK	12591-6001	(SW UP-HALT)	
PERIPHERAL OPTIONS	12875A	PROCESSOR –	12566-6001		SC10 A203
		INTERCONNECT	12566-6001		SC11 A204
	2754B	TTY CONSOLE	–	–	
	12531B	TTY INTERFACE	12531-6001	2754B	SC12 A205
	2748A	READER			
	12532A	READER INTERFACE	12597-6001	2748A	SC13 A206
	2766A	DISC (FIXED HEAD)			
	12610C	DISC INTERFACE	12610-6001	DATA (SW DOWN)	SC14 A207
			12610-6002	COMMAND	SC15 A208
	12539A	TIME BASE GEN	02116-6119		SC16 A209
OTHER	2772A	DISC PWR. SUP.			
	2160A	PWR. SUP. EXT.			
	2992Z	2 BAY CABINET			
	2866A	SINGLE BAY CAB			
COMMUNICATIONS PROCESSOR					
COMPUTER	2114A/B-004	8K MEMORY			
	-008	POWER FAIL			
PROCESSOR OPTIONS	12598A	PARITY CHECK	12598-6001	HOOD = HALT	A5
PERIPHERAL OPTIONS	12584A	MULTIPLEXOR	12584-6001	FIRST 16 PORTS	SC10 A23
			12584-6001	OPTIONAL	SC11 A22
	12875A	PROCESSOR –	12566-6001		SC12 A21
		INTERCONNECT	12566-6001		SC13 A20
	12584A-02	PHONES	12584-6001	OPTIONAL	SC14 A19
			12584-6001	OPTIONAL	SC15 A18



*Optional, not required.

FIGURE 43. 2000B BOARD LOCATIONS (2116B COMPUTER)



*Optional, not required.

FIGURE 44. 2000B BOARD LOCATIONS (2116C COMPUTER)

TABLE 5

2000B OPTIONAL HARDWARE

DESCRIPTION	MODEL	INTERFACE	
Mag Tape	HP 3030G	12559A	75 ips
	HP 7970A-200	13181A-001	25 ips
	HP 7970A-202	13181A	37.5 ips
	7970C		45 ips
Telephone Auto Disconnect		12584B-001	
Keyboard-Display Terminal	2600A	None required	

TABLE 6

DISC/DRUM REFERENCE TABLE

Model	Logical Tracks (Decimal)	Physical Tracks (Octal)	Physical Tracks (Decimal)	Storage (words)
2766A-003	96	0-577	384	786,432
2766A-004	128	0-777	512	1,048,576
2773A	48	0-277	192	393,216
12553A-001 adds:	48	–	192	393,216
12533A-002 adds:	16	–	64	131,072
12553A adds:	32	–	128	262,144
2774A	96	0-577	384	786,432
2775A	192	0-1377	768	1,572,864

Both Units Have: 128 Sectors/Logical Track
32 Sectors/Physical Track

TABLE 7

LOGICAL-TO-PHYSICAL TRACK CONVERSION

Physical Track Range (Octal)	0-3	4-7	10-13	14-17	20-23	24-27	30-33	34-37	40-43	44-47	50-53	54-47	60-63	64-67	70-73	74-77
	1st LOGICAL DISC (TRACKS)															
0-77	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
100-177	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
200-277	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
300-377	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64
	2nd LOGICAL DISC (TRACKS)															
400-477	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
500-577	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
600-677	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
700-777	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64

TABLE 8

LOGICAL-TO-PHYSICAL SECTOR CONVERSION

PHYSICAL SECTORS (OCTAL)		LOGICAL SECTORS (DECIMAL)							
0	20	1	17	33	49	65	81	97	113
1	21	2	18	34	50	66	82	98	114
2	22	3	19	35	51	67	83	99	115
3	23	4	20	36	52	68	84	100	116
4	24	5	21	37	53	69	85	101	117
5	25	6	22	38	54	70	86	102	118
6	26	7	23	39	55	71	87	103	119
7	27	8	24	40	56	72	88	104	120
10	30	9	25	41	57	73	89	105	121
11	31	10	26	42	58	74	90	106	122
12	32	11	27	43	59	75	91	107	123
13	33	12	28	44	60	76	92	108	124
14	34	13	29	45	61	77	93	109	125
15	35	14	30	46	62	78	94	110	126
16	36	15	31	47	63	79	95	111	127
17	37	16	32	48	64	80	96	112	128
		Physical Track +Ø		Physical Track +1		Physical Track +2		Physical Track +3	

To accomplish this it may be necessary to convert from the logical time-share system address to the physical track and sector address within the disc/drum. The disc/drum has 32 physical sectors per track. Four physical tracks are required for each logical system track. Table 7 shows the conversion between logical and physical track numbers. The table is shown for an assumed size of 1,048,576 word capacity. Notice that the logical tracks are shown in decimal, whereas the physical tracks are shown in octal notation.

Table 8 provides a conversion from the sectors on a logical system track to the physical tracks and sectors within the Drum.

The 2000A Time-Share System was compatible with the HP 2770A and 2771A Disc units. These are not recommended for the 2000B. They have only 90 sectors/track, which makes them incompatible with the length of certain required files for the CAI package.

The 2000C uses a large swap area requiring 160 sectors. It requires Disc/Drum units which can increment across track boundaries. Since the 2770A and 2771A do not have this capability their use on the 2000B would degrade the system update capability. The 2770A and 2771A units will work on the 2000B, and their capacity is described in HP 2000A TSS Table 3 on page 2-4.

4-2 Base Page Constants

Table 9 provides the Equipment Table (compare HP 2000A TSS Table 4, pages 6-8, 9). All entries are identical except locations 165 and 166. These dealt with the phones and are no longer needed. An additional entry is the number of ports (swap tracks required) NPORT addr 165.

The important core locations have changed only slightly from the 2000A. They are listed in Table 10.

Table 11 provides a cross reference for the disc address pointers and the library programs.

4-3 TTY Tables (System Processor)

The System Processor has 13 TTY table entries for each of the 32 users. Three entries are new (i.e., not required by the 2000A). They include FLAG, TNUM and RTIM. The STAT entry duplicates a STAT entry in the Communications Processor. The contents of these two STAT entries is different. DISC and PROG are associated with the swap track. ID, NAME and TIME are of general nature. STAT, LINK and PLEV are associated with the queue. CLOC is a time-out clock when the user is on top of the queue, RSTR is the restart address when removed from the queue due to time slot expended.

TABLE 9.
EQUIPMENT TABLE (2000B)
SHEET 1

DIREC

FIRST DIRECTORY TRACK

00100	_____	LENGTH OF THIS TRACK
00101	_____	First 5 words of this Directory Track (Pseudo Entry)
00102	_____	
00103	_____	
00104	_____	
00105	_____	
00106	_____	DISC ADDRESS

SECOND DIRECTORY TRACK

00107	_____	LENGTH OF THIS TRACK
00110	_____	First 5 words of this Directory Track
00111	_____	
00112	_____	
00113	_____	
00114	_____	
00115	_____	DISC ADDRESS

THIRD DIRECTORY TRACK

00116	_____	LENGTH OF THIS TRACK
00117	_____	First 5 words of this Directory Track
00120	_____	
00121	_____	
00122	_____	
00123	_____	
00124	_____	DISC ADDRESS

FOURTH DIRECTORY TRACK

00125	_____	LENGTH OF THIS TRACK
00126	_____	First 5 words of this Directory Track
00127	_____	
00130	_____	
00131	_____	
00132	_____	
00133	_____	DISC ADDRESS

TABLE 9.
EQUIPMENT TABLE (2000B)
SHEET 2

IDLOC	00134 _____	DISC ADDRESS OF IDT	
IDLEN	00135 _____	NEGATIVE LENGTH OF ID TABLE	
ADLOC	00136 _____	DISC ADDRESS OF ADT	
ADLEN	00137 _____	NEGATIVE LENGTH OF AD TABLE	
		LOGICAL DISC ZERO	
TRAX	00140 _____	0-15	Track Lock/Unlock Bits
	00141 _____	16-31	0 = Unlocked
	00142 _____	32-47	1 = Locked
	00143 _____	48-63	
		LOGICAL DISC ONE	
	00144 _____	0-15	
	00145 _____	16-31	
	00146 _____	32-47	
	00147 _____	48-63	
		LOGICAL DISC TWO	
	00150 _____	0-15	
	00151 _____	16-31	
	00152 _____	32-47	
	00153 _____	48-63	
		LOGICAL DISC THREE	
	00154 _____	0-15	
	00155 _____	16-31	
	00156 _____	32-47	
	00157 _____	48-63	
?TBL	00160 _____	Logical Disc Zero	0-5 = SC
	00161 _____	Logical Disc One	6-7 = Disc #
	00162 _____	Logical Disc Two	8-15 = #Sect
	00163 _____	Logical Disc Three	per Track
MAGSC	00164 _____	SC for Magtape, 0 if None	
NPORT	00165 _____	Number swap tracks reserved	

TABLE 10

IMPORTANT CORE LOCATIONS

MAIN	262:	_____	Address of TTY Flag word for user in core, Ø if none.
LIB	263:	_____	= Disc address of current library program loaded at location 37300.
ENDSK	264:	_____	= 1 when disc busy, = Ø no transfer underway.
HQDIS	265:	_____	Normally 1, = Ø for top of queue disconnect.
TIMEF	266:	_____	= 1 for current program timed.
X	267:	_____	Normally -2, -1 indicates scheduler is blocked for TBG interrupts.*
MLINK	336:	377	
MLINK +1	337:	_____	Points to top of queue.
MLINK +2	340:	77777	Pseudo PLEV entry for bottom of queue.
LDISC	32266:	_____	Return address for last call to disc driver.
DINT	32321:	_____	Return address disc driver completion interrupt.
POW	32414:	_____	Power fail return address.
?TT35	32673:	_____	System console output return address
?TT2	32712:	_____	System console interrupt return address.
TTYØØ	33103:	_____	First TTY table entry.
S14SH	34103:	_____	Send driver.
R14CM	34130:	_____	Receive driver interrupt routine.
CLKIN	34320:	_____	TBG interrupt return address.
CLC1	34335:	_____	= NOP scheduler blocked = JMP service scheduler.

*X allows the scheduler to ignore every other TBG interrupt. In certain CAI applications servicing every 100 milliseconds results in excessive overhead. By allowing 200 milliseconds the return from I/O wait is usually completely serviced saving two potential disc swaps.

TABLE 11

Contents of LIB (263)

Contents of LIB	Program Name	Page in Listing
36050	LIBRARY SIZES	262/#21
36051	FUSS	264/#21
36052	FUSS (cont)	264/#21
36053	FILES	265/#21
36054	CHAIN	271/#22
36055	SAVE	276/#22
36056	CSAVE	281/#22
36057	SUPERSAVE	283/#23
36060	GET	289/#23
36061	APPEND	292/#23
36062	HELLO	295/#24
36063	BYE	301/#24
36064	KILL	305/#24
36065	RENUMBER	310/#25
36066	NAME	316/#25
36067	CATALOG	318/#25
36070	LIBRARY	322/#25
36071	DELETE	323/#26
36072	TIME	325/#26
36073	PROTECT	327/#26
36074	UNPROTECT	329/#26
36075	OPEN	330/#26
36076	LENGTH	336/#27
36077	ECHO	337/#27
36100	REPORT	338/#27
36101	DIRECTORY	341/#27
36102	STATUS	345/#27
36103	ROSTER	351/#28
36104	RESET	353/#28
36105	CHANGE ID	356/#28
36106	SLEEP	359/#29
36107	SLE OVERLAY	364/#29
36110	NEWID	370/#30
36111	KILLID	374/#30
36112	KIL Overlay	378/#30
36113	UNLOCK	384/#31
36114	LOCK	389/#31
36115	LOC Overlay	395/#31
36116	PURGE	399/#32
36117	PUR Overlay	405/#32
36120	DISC	409/#33
36121	MAGTAPE	415/#33
36122	PHO	416/#33
36123	FAST	417/#33
36124	SLOW	419/#33
36125 – 36132	ERROR MESSAGES	420/#33

FLAG contains various condition bits for each user. In the 2000A certain words were used for the same function where each individual user corresponds to the bit position. The condition of bit 6 is checked by the Scheduler routine to determine whether new activity must be scheduled (i.e., user queued or dequeued).

Bit Ø Error detected during tape mode

Bit 1 Compiled mode in swap area

Bit 2 $HELLO log on message running

Bit 3 User in Tape mode

Bit 4 Unable to abort due to:

a. FILES statement being processed
b. CHAIN statement being processed
c. Compilation or Decompilation underway
d. Library program being executed (except CAT or LIB)

Bit 5 Output wait buffer full

Bit 6 Communications from Communications Processor

Bit 7 Abort attempted but not allowed due to bit 4

Bit 8 Unable to accept input

Bit 9 CHAIN command running

TNUM This location contains the TTY number of the user. These range from 0 to octal 37. They occupy bits 8 to 11. The apparent octal values range from 000000 to 017400. The value is fixed for each TTY table. The value is useful for determining the user and building up the communication request code.

DISC This entry contains the disc address of the first sector of the swap area. To facilitate swapping it is not required that the first sector correspond to the track origin.

PROG This entry monitors the amount of core required by the program while on the Disc swap track. When in core the PBPTR entry specifies the last swap area location used.

ID Whenever a user successfully logs on this entry is updated to contain his ID code. The entry is zero when no user is currently logged on.

NAME The name of the current program is contained in this three word entry. When the name is less than 6 characters blanks are used to fill out the three words.

TIME This two word entry contains the time of day at logon. It is used to update the accounting information at logoff.

CLOC This entry contains the time of day value when the 2 second time slice will run out (was 1 second in 2000A).

RSTR Contains the starting address of the program when initially placed on the queue, and the restart address when the program is suspended.

STAT When this user is on the queue the status word indicates the program type. When the user is not on the queue, it indicates the reason why.

-3	%ENTO	Enter statement timed out
-2	%DISC	Disconnect desired because user hung up, not logged on, BYE
-1		Initiate abort
0		Idle
+1	%ABOR	Abort being processed
+2	%INPT	Input suspend
+3	%OUTW	Output suspend
+4	%SYNT	Processing syntax line
5-61B		Command routine 5 = RUN, 6 = LIST, etc (reference Command Table, page 249/#20)

LINK This entry contains the address of the next lower user on the queue. The contents have significance only if the user is on the queue.

PLEV This word is used in conjunction with LINK and contains the priority of the user when he is entered on the queue.

0	Syntax system library routines once started, return from I/O suspend
1	RUN, LIST, PUNCH
2	System library routines before they reach the top of the queue
4	Computer bound (RUN) programs

RTIM A new entry for ENTER command. It contains the response time for the ENTER input.

Table 12 gives the addresses for the teletype table entries. The contents of TNUM is fixed for each user and the value is shown.

TABLE 12

SYSTEM PROCESSOR TTY TABLE

	0(0B)	1(1B)	2(2B)	3(3B)	4(4B)	5(5B)	6(6B)	7(7B)	8(10B)	9(11B)	10(12B)	11(13B)	12(14B)	13(15B)	14(16B)	15(17B)
FLAG	33103	33123	33143	33163	33203	33223	33243	33263	33303	33323	33343	33363	33403	33423	33443	33463
TNUM	33104 (0)	33124 (400)	33144 (1000)	33164 (1400)	33204 (2000)	33224 (2400)	33244 (3000)	33264 (3400)	33304 (4000)	33324 (4400)	33344 (5000)	33364 (5400)	33404 (6000)	33424 (6400)	33444 (7000)	33464 (7400)
DISC	33105	33125	33145	33165	33205	33225	33245	33265	33305	33325	33345	33365	33405	33425	33445	33465
PROG	33106	33126	33146	33166	33206	33226	33246	33266	33306	33326	33346	33366	33406	33426	33446	33466
ID	33107	33127	33147	33167	33207	33227	33247	33267	33307	33327	33347	33367	33407	33427	33447	33467
NAME(3)	33110	33130	33150	33170	33210	33230	33250	33270	33310	33330	33350	33370	33410	33430	33450	33470
TIME(2)	33113	33133	33153	33173	33213	33233	33253	33273	33313	33333	33353	33373	33413	33433	33453	33473
CLOC	33115	33135	33155	33175	33215	33235	33255	33275	33315	33335	33355	33375	33415	33435	33455	33475
RSTR	33116	33136	33156	33176	33216	33236	33256	33276	33316	33336	33356	33376	33416	33436	33456	33476
STAT	33117	33137	33157	33177	33217	33237	33257	33277	33317	33337	33357	33377	33417	33437	33457	33477
LINK	33120	33140	33160	33200	33220	33240	33260	33300	33320	33340	33360	33400	33420	33440	33460	33500
PLEV	33121	33141	33161	33201	33221	33241	33261	33301	33321	33341	33361	33401	33421	33441	33461	33501
RTIM	33122	33142	33162	33202	33222	33242	33262	33302	33322	33342	33362	33402	33422	33442	33462	33502

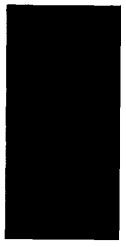
4-4 Loader

The loader in the 2000B is quite similar to the 2000A. However, the Communications Processor program is loaded first through the System Processor Photo Reader and its program is started at address 2.

The rest of the core based system and library programs are similar. The Equipment Table has the phone entries deleted but the number of ports added.

The greatest difference now is the ability to open a selected number of swap tracks. It makes more efficient use of the disc for systems smaller than 32 users.

System Power Fail



CHAPTER 5

SYSTEM POWER FAIL

5-1 AC Power Considerations

Material on the AC power considerations is covered in detail in the Site Preparation Manual. Because of its importance, and because of the subtle nature of these system crashes, the AC power considerations are mentioned here.

The provision for power fail in the time share system is important. The nature of the AC power line is a key system parameter. Ideally, the primary power distribution from utility companies is constant both in frequency and in amplitude. In actual practice the AC lines may have significant noise superimposed on them. This is particularly true in industrial environments containing large motors and air conditioning equipment. In these cases, switching transients may produce very low or high input voltage for long periods (tens of milliseconds).

The power supplies store some energy in the filtering capacitors. The power low line circuitry must sense the failure in the AC line soon enough to signal the power fail condition and still allow the computer to continue operating normally for a few milliseconds. The actual specified minimum time is 2 milliseconds although 4 to 6 milliseconds is more typical.

Good installation procedure requires an adequate power rating on a common circuit (single phase or 3 phase) which powers all the system equipment. In cases where long power lines are required or separate primary circuits are used, it may be difficult to adequately provide for power fail conditions. This is due to noise and system ground loops. The Discs and Drums are rather susceptible to this system noise.

The system power fail provides an independent power fail routine for each processor. The processors are not crosscoupled with Power On or Power Fail hardware status signals.

5-2 Communications Processor Power Down

Figure 45 shows the block diagram of the Power Fail routine. Since characters being input or output to a terminal require 50 or 100 milliseconds a power failure will usually result in a garbled transmission.

The hardware interrupts to location 4 for both power up and power down. This requires the software routine to test the hardware Flag FF to determine the direction. The program then goes to the proper segment to service the interrupt. For power failure the Flag will be clear. The A, B, E, and O registers are saved. The interrupting address is saved. The System Processor acknowledgement of the last request is determined. The POWC2 communications flag is cleared to indicate the machine was running at the time of interrupt. The Communications Processor then clears the Control FF at S.C. = 4 to allow restart when the power is restored. It then executes a halt 4 @ P = 4754.

5-3 Communications Processor Power Up

When the power is restored an interrupt to S.C. = 4 takes place. The routine determines power is coming up because Flag 4 is set. It determines that the machine was running at the time of power failure. If the machine was not running it commences at the INIT routine as on a relaod in the System Processor.

If the computer had been operating at the time of power fail it is now necessary to restore conditions and resume the program. This code starts at POWUP. To protect itself it clears the POWF and clears Flag Ø thus inhibiting interrupts. If the last command had not been acknowledged by the System Processor it sends this command again. It initiates the hardware conditions for the Multiplexor Data boards. The Multiplexor Output data bits are all set. These are TTY stop bits, and insure synchronism. The program then restores the A, B, E, and O registers. It then sets the Control FF at select code 4 to allow a subsequent interrupt. It then returns to the program location which was executing at the time of the power fail interrupt.

5-4 System Processor Power Failure

Refer to figure 46 for the System Processor power failure routine. The power fail interrupt occurs both for power failure and for power restore. Thus whenever the interrupt to select code 4 occurs the software must check the hardware Flag at select code 4 to determine the directional sense (i.e. power up or power down) of the interrupt. This allows the jump to POWI for power up/restart.

If the directional sense is down the program continues execution at POW for the shut down sequence. The routine first temporarily saves the A, B, E, and O registers.

Because the routine is non-reentrant an interrupt for failure from the restart portion is not serviced. The computer executes a halt 4 @ P = 32466. This will allow the execution of the entire power up sequence when power is restored.

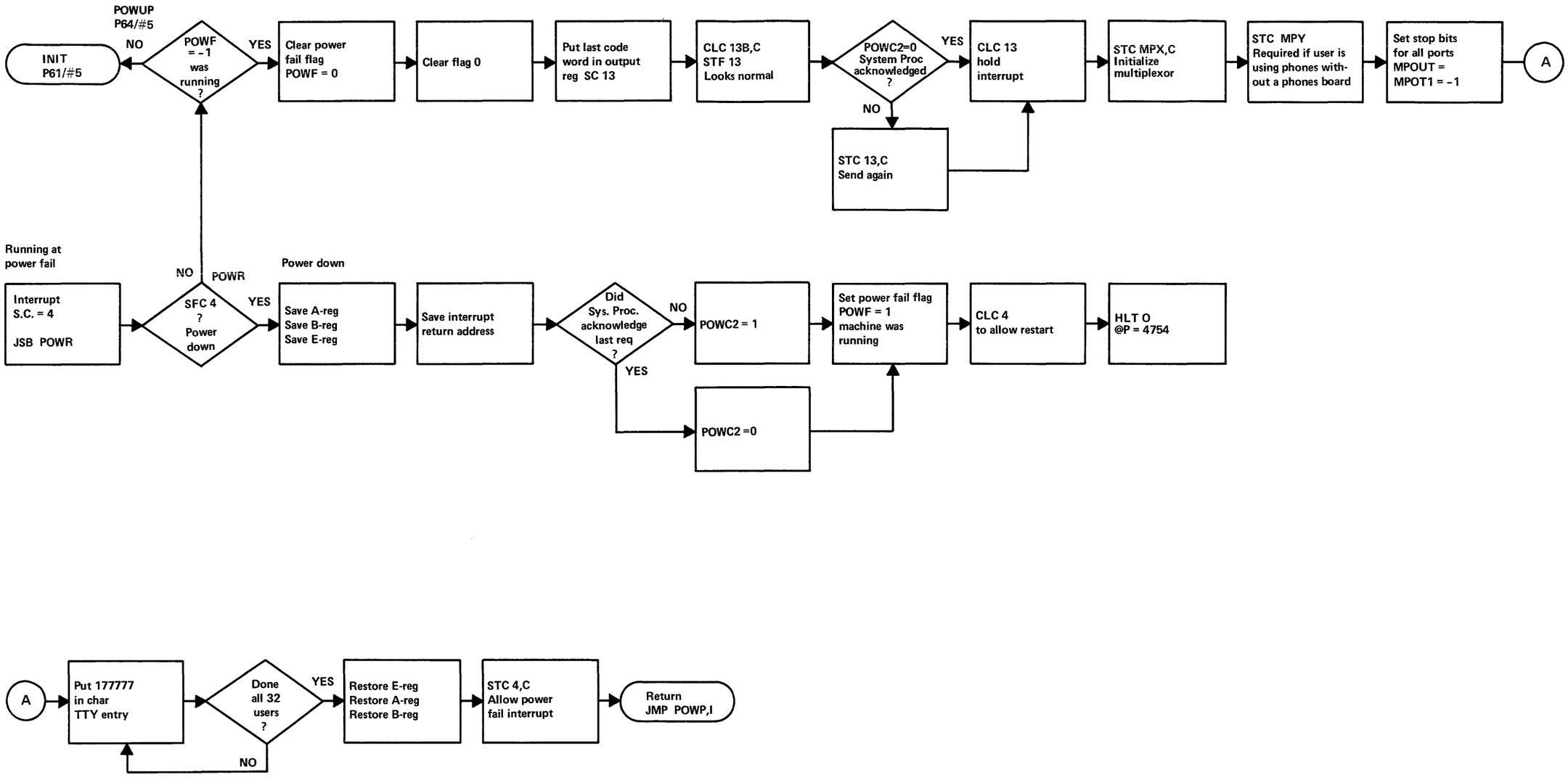
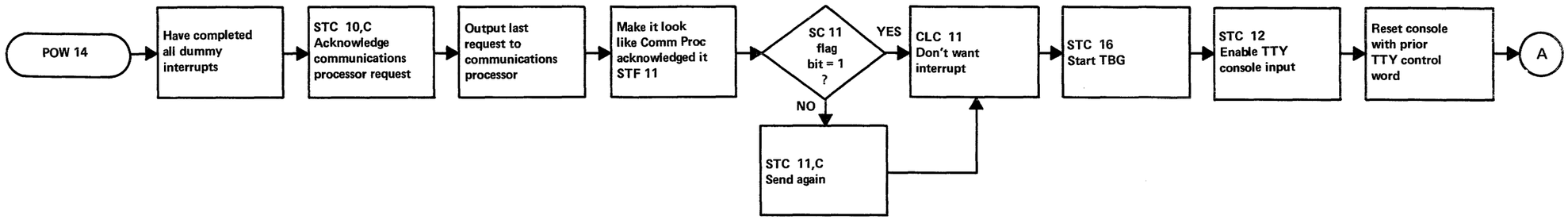


FIGURE 45. COMMUNICATIONS PROCESSOR POWER FAIL BLOCK DIAGRAM



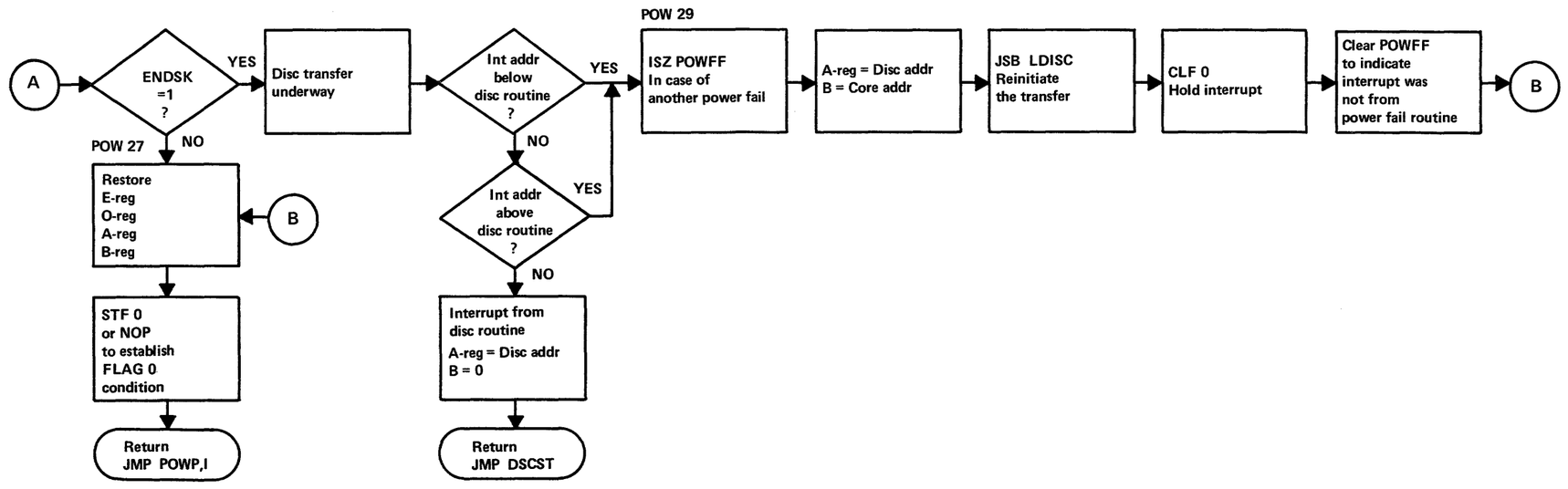


FIGURE 47. SYSTEM PROCESSOR POWER FAIL BLOCK DIAGRAM SHEET 2 OF 2

If the power failure did not originate while executing the power fail routine code area then it is considered a normal power down interrupt. The A, B, E, and O register contents are transferred from the temporary locations to their normal locations. The return address is saved. It is necessary to save the status of certain hardware flip flops. Corresponding bits in a flag word are set to indicate the hardware Flag FF is set. Each of the I/O Flag FF's can be tested with the SFS instruction. The status is saved in POWFL.

The condition when the flag is set may mean that an interrupt is imminent, that one is in the process of being serviced, or that an acknowledgement had taken place but did not require an interrupt. During restart each of these possibilities is pursued with the proper action taken each time.

The status of the interrupt system is determined and saved. Note it was not necessary to clear Flag ∅ because the interrupt at select code = 4 effectively inhibits all other interrupts. The Control FF at select code 4 is set allowing an interrupt if the power is restored before going completely down. The machine then executes a halt ∅ @ P = 32466.

It is interesting to note that any disc transfer underway at power failure continues until the PON (power on) signal drops. This normally occurs 2 to 4 milliseconds after failure is determined.

5-5 System Processor Restart

When an interrupt to select Code 4 is received and the Direction FF indicates power is coming up the power fail routine begins execution at POW1. If power comes up and immediately fails again it is not desirable to continue the power up processing. The Control FF at select code 4 is set which allows an immediate interrupt for power failure. The pointers POWI and POWJ are set up and will be used to service the I/O Flags. The Time Base Generator is initialized with the proper time period. The system console is reset to the Input/Output, and Punch and/or Print conditions encountered at the time of interrupt.

A software loop determines which of the I/O devices require servicing. The status of the I/O Flag FF is available from the POWFL Word. The Flag FF is set by the Device Flag and cleared by the I/O service subroutine just prior to exit. If the Flag FF for a particular I/O device is set and the interrupt return address caused by power failure lies within the bounds of the I/O service routine clearly the I/O interrupt had been received and was being serviced.

In this case we will return to the I/O service subroutine upon completion of the power fail restart currently being executed. An interesting hardware trick is used to establish the proper hardware conditions. An aside is in order to point out the normal hardware conditions. The Device Flag signal sets the Flag Buffer FF. At T2 the Flag FF is set. At T5 (assuming certain other hardware conditions are true) the IRQ FF is set. This IRQ FF toggles until its interrupt (phase 4) is granted. Then the Interrupt Acknowledgement is sent which clears the Flag Buffer, keeps the IRQ FF cleared, and the I/O service routine is actually started. This is the condition we find ourself in for our I/O servicing power fail loop.

The trick used to set up this hardware condition is to allow an interrupt, but to change the contents of the trap cell so no JSB is executed. This sets all of the hardware conditions we need. The trap cell is then restored. When the power fail restart is completed the program execution will resume where it was suspended.

In the case where the Flag FF was set but the Interrupt return address did not lie within the boundaries of the I/O service routine the interrupt was imminent. It is sufficient to set the Flag on this device and the interrupt will take place normally.

When all of the I/O hardware Flags have been serviced the restart program continues at POW14. A STC 10,C sends an acknowledgement to the Communications Processor (whether needed or not). If power goes down on a single machine one communications request to that machine may be lost. This system has no way to tell whether this condition has occurred. This is the reason a common primary power circuit to the entire system is preferable to separate circuits.

It is normally better to ignore the potentially missed request than to repeat it and possible duplicate its execution. An example of this occurs when the System Processor fails. Meanwhile the Communications Processor continues to operate. If the HVL or BFL request were sent while the System Processor power was off the command would be ignored. On power restart an acknowledgement would be sent when in fact no servicing had taken place. This particular sequence would result in the user being in limbo. He could abort with the Break key. All other keyboard inputs would be ignored.

The System Processor repeats its last request if the Communications Processor had not acknowledged it (Flag 11 will be set indicating the acknowledgement). The Time Base Generator is started. The system console is enabled and restored to the prior hardware mode. At this point we are about done. If ENDSK = Ø it indicates no Disc transfer was underway. The A, B, E and O registers are restored. The Interrupt system is re-established and the program control returns to the P register location at the time of power fail.

If ENDSK is set it indicates a transfer was being processed. A Disc transfer cannot be restarted midway. If the interrupt took place within the actual Disc routine coding the entire initialization is repeated. The return is to DSCST. If the interrupt does not take place within the Disc routine it indicates the initialization was completed. It is not necessary to repeat this so just the actual transfer is repeated. The routine is started at LDISC.

5-6 Power Fail Symptoms

After studying the detailed block diagram of the power fail routines we can better understand the symptoms of the operating system.

If only one machine halts, meanwhile a communications request originates in the second processor, and then the first machine comes up again, the request will be lost. Thus, it is highly desirable to power both machines from a common AC power line. When both processor go down together the possibility of an individual user being tied up is greatly reduced.

The nature of the problems which can occur is rather straightforward when the power fail routine and communications requests are understood. Because the time to send or receive a TTY character is long all characters in process at the time of the Communications Processor power fail are likely to be garbled. Since most of the communications requests originating in the System Processor are unique to an individual user a momentary failure in the Communications Processor will probable affect only a single user. The first request from the System Processor will be lost and the lack of an acknowledgement will hold the System Processor in the SFS 11, JMP*-1 loop.

In the case of power fail in the System Processor interesting things happen to the terminals. The frequency of requests by the Communications Requests is low, but each one normally requires action by the System Processor. The first request is initiated normally. The second request causes the Communications Processor to hang up in the OTCB and OTCS routine waiting for the acknowledgement. At this point it can no longer service the terminals. They may run open or cease to function. User control may normally be established by pushing the Break key, but only after power is brought up again on both computers. The Break key works by causing an abort. The abort is serviced irrespective of the various status and flag words pertaining for that particular user.

Sleeping the system is another way to clear up possible trouble following power fail. It is not desirable however, because this also wipes out all current users programs in the swap areas. Power Failure in the Communications Processor normally results in cutting off all dataphones. This is a result of the "fail safe" nature of the dataphones. The absence of the positive Data Terminal Ready signal for more than one second is an automatic disconnect.

5-7 Sleeping With Communications Processor Malfunction

When sleeping the system certain requests are sent to the Communications Processor. It responds in the normal manner (i.e., by executing the request and the acknowledgement). If the Communications Processor is no longer working it fails to send the acknowledgement. This causes the System Processor to loop with a SFS 11, JMP *-1 (102311 = SFS, 024XXX = JMP * -1). If this is encountered verify it by pushing HALT, then SINGLE CYCLE.

If the Communications Processor is still able to run a short emergency program at starting address 100 is used to allow system sleep. It toggles the Flag for command acknowledgement. There exists a condition during syntax checking when the System Processor requires a carriage return. The emergency sleep program also sends this carriage return. If the Communications Processor is unable to execute this emergency sleep program a more powerful sleep technique is required.

An alternate method clears each JMP *-1 instruction in each SFS, JMP *-1 loop encountered. To do this Halt the machine when the loop is encountered. Single cycle to verify the loop. When the T-register contains the 102311 the M-register accesses the JMP location. Clear the switch-register and LOAD MEMORY. Push RUN to continue. This process will be repeated a few times allowing the complete sleep to take place.

When the Communications Processor is returned to service the system may be brought up from Disc or Mag Tape in the normal manner.

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