DPS 6

MSU9617/9618/9619/9620
Fixed-Disk Units Operation

Honeywell

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MSU9617/9618/9619/9620
Fixed-Disk Units Operation

SUBJECT
General Description, Operation, and Maintenance Information for the MSU9617/9618/9619/9620 Fixed-Disk Units

SPECIAL INSTRUCTIONS
This manual supersedes GS10-00, dated March 1986 and Addendum A dated April 1986. Change bars in the margin indicate technical changes and additions, asterisks denote deletions.

The following notice is provided in accordance with the United States Federal Communications Commission's (FCC) regulations.

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. The equipment manufactured after October 1, 1983 has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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About This Manual

This operation manual provides descriptions and instructions for users of the MSU9617/9618/9619/9620 fixed-disk units.

Section 1 introduces the disk units and contains information concerning the devices' capabilities. It also includes a functional description of how the units actually work. Section 2 describes the controls and indicators with which the user should be familiar before using a disk unit. Section 3 provides information used to operate the disk unit. Included in this section are the power-on and power-off procedures as well as maintenance information about the disk unit filter. Appendix A provides programming information. Appendix B provides disk unit specifications.

Readers are invited to use the Technical Publications Remarks form at the end of the manual to note any publication errors or to offer any suggestions for improvement.

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Contents

Figures

Tables

Section 1
Introduction

Two large-capacity fixed-disk units are available on DPS 6 and Level 6 systems. Both units are environmentally sealed for high reliability.

The MSU9617/9618 is a 132-MB (formatted) fixed-disk unit that contains 6 nine-inch discs, each disc having 821 recordable cylinders and 10 heads (161,280 bytes per cylinder). Average seek time (time it takes to position the read/write head over a desired cylinder track to enter or retrieve data) is 30 milliseconds. Data can be transferred at a rate of 1.2 MB per second. Automatic error detection and correction help to protect data integrity. The MSU9617 includes a cabinet with mounting hardware and cables. MSU9618 is an add-on disk drive with cables.

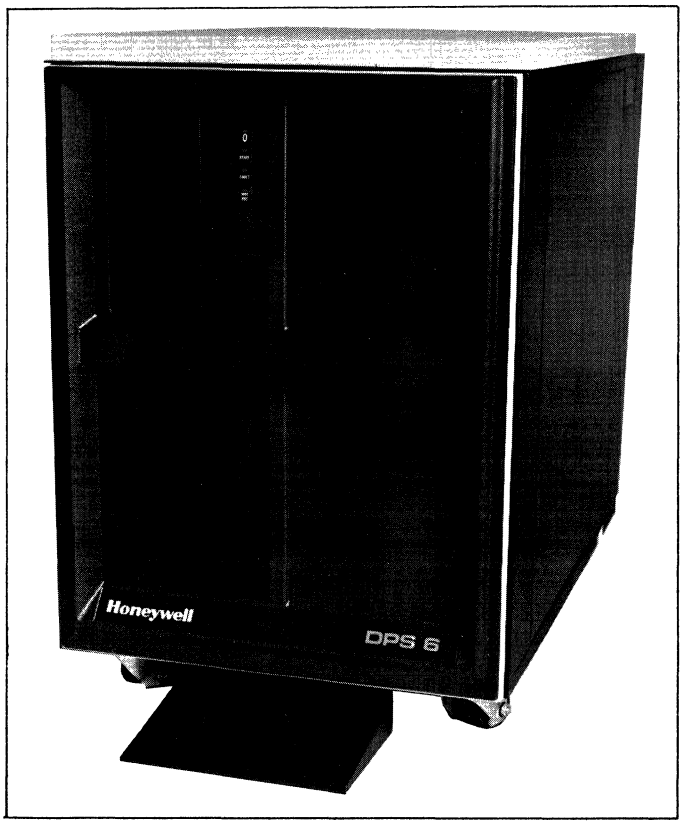

Figure 1-1. MSU9617/9618/9619/9620

The MSU9619/9620 is a 413-MB (formatted) fixed-disk unit that contains 7 nine-inch discs, each disc having 709 recordable cylinders (2 heads per data surface) and 24 heads (583,680 bytes per cylinder). Average seek time is 20 milliseconds. Data can be transferred at a rate of 1.83M bytes per second. Automatic error detection and correction help to protect data integrity. The MSU9619 includes a cabinet with mounting hardware and cables. The MSU9620 is an add-on disk drive with cables.

Up to three units can be housed in a single cabinet and up to four units can be connected to one Disk Controller (MSU9615). The 132-MB and 413-MB disk units can be housed in the same cabinet. Fixed-disk units and cabinets can be added to a configuration at any time to increase overall storage capacity. The disk cabinet can be placed up to 20 ft from the system/controller cabinet.

The MSU9617/9618/9619/9620 fixed-disk units feature:

- Choice of 132-MB (formatted) and/or 413-MB (formatted) fixed-disk units
- Ability to house 132-MB and 413-MB fixed-disk units in same cabinet (up to 3 units)
- Built-in features to help ensure the integrity and protection of data
- Ability, during data transfer on one unit, to perform a simultaneous seek operation on up to three other units
- Multiple-sector read/write capability with automatic track and cylinder switching
- Average access time of 28.3 ms (413-MB unit); 38.3 ms (132-MB unit)
- Transfer rate of 1.82M bytes per second (413-MB unit); 1.2M bytes per second (132-MB unit) from unit to controller
- Transfer rate of 833K bytes per second between the system and controller
- Automatic self test
- Automatic retry and error correction
- Automatic management of media defects
- Full data path error checking
- High reliability

Marketing Identifiers[1,2]

MSU9617 — Single 132-MB fixed-disk unit and cabinet with mounting hardware and cables for one unit for DPS 6 and Level 6 systems

MSU9618 — 132-MB fixed-disk unit with add-on mounting hardware and cables for DPS 6 and Level 6 systems

MSU9619 — Single 413-MB fixed-disk unit and cabinet with mounting hardware and cables for one unit for DPS 6 and Level 6 systems

MSU9620 — 413-MB fixed-disk unit with add-on mounting hardware and cables for DPS 6 and Level 6 systems

CBL9619 — Two 10-foot cables for disk intercabinet connections for DPS 6 and Level 6 systems

Prerequisites

MSC9615 — High-Speed Disk Controller with 4 ports and required cable for attachment to DPS 6 and Level 6 systems

Functional Description

The disk units contain all the circuits and mechanical devices necessary to record and recover data from the discs. The necessary power for this is provided by an integral power supply, which receives its input power from the cabinet power distribution unit.

All functions performed by the unit are done under direction of the controller. The controller communicates with the unit via the interface. This consists of a number of I/O lines carrying the necessary signals to and from the unit.

Some interface lines, including those that carry commands to the unit, are not enabled unless the unit is selected by the controller. Unit selection allows the controller, which can be connected to more than one unit, to initiate and direct an operation on a specific unit.

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[1]Fixed-disk units require a high capacity removable media device for software loading (i.e., streamer, GCR/PE tape, NRZI/PE tape, Cartridge Module or Mass Storage Disk Unit).

[2]An update to the central processor firmware may be required when adding a fixed-disk unit as the systems disk to an installed DPS 6 or Level 6 system (the disc containing booting procedures for the operating system). Consult your Honeywell Representative for details.

All operations performed by the unit are related to data storage and recovery (normally referred to as writing and reading). The actual reading is performed by electromagnetic devices called heads that are positioned over the recording surfaces of the rotating discs. There are two heads for each disc surface on the 413-MB unit and one head for each disc surface on the 132-MB unit. The heads are positioned in such a way that data is written in concentric tracks around the disc surfaces.

Before any read or write operation can be performed, the controller must instruct the unit to position the heads over the desired track (seek) and also to use the head located over the surface (head selection) where the operation is to be performed.

After selecting a head and arriving at the data track, the controller still must locate that portion of the track on which the data is to be written or read. This action (track orientation) is done by using the Index and Sector signals generated by the unit. The Index signal indicates the logical beginning of each track, and the Sector signals are used by the controller to determine the position of the head on the track with respect to Index.

When the desired location is reached, the controller commands the unit to read or write the data. During a read operation, the unit recovers data from the discs and transmits it to the controller. During a write operation, the unit receives data from the controller, processes it and writes it on the discs.

The unit is also capable of recognizing certain errors that may occur during its operation. When an error is detected, it is indicated either by a signal to the controller or by a maintenance indicator on the unit itself.

Section 2
Controls and Indicators

This section describes the various controls and indicators necessary for operating the disk units.

Operation Control Panel

The operation control panel for each disk unit in the subsystem configuration contains four light indicators, three push buttons, and a Logic Address Plug (Figure 2-1).

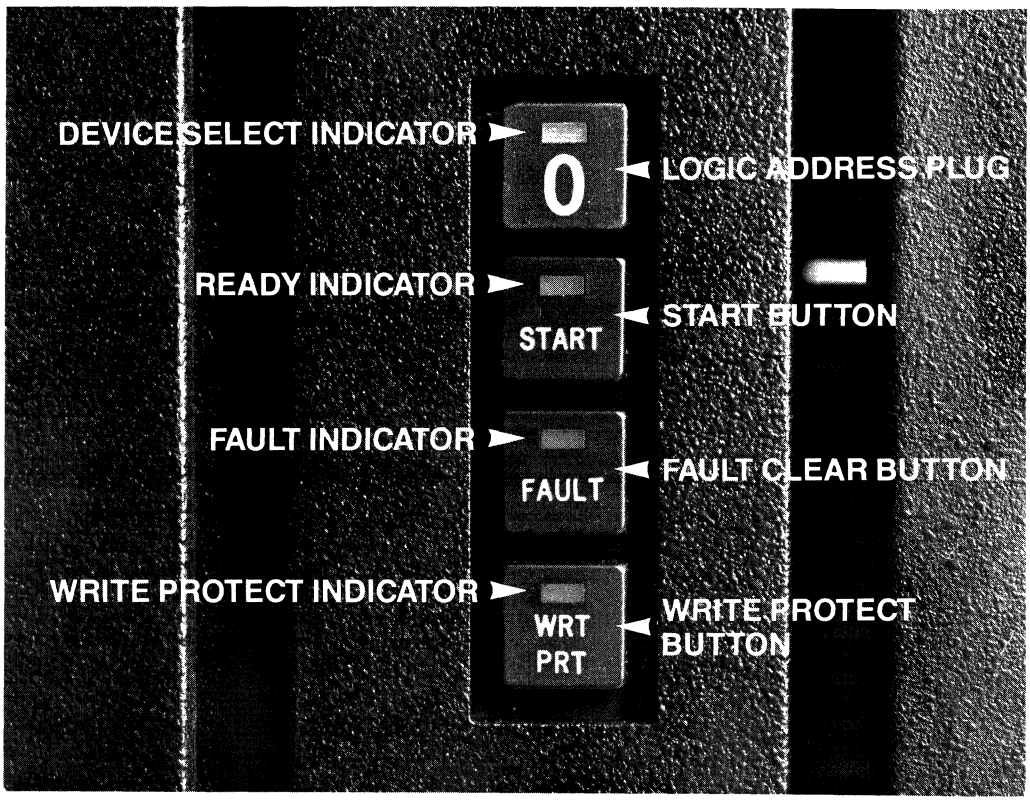


Figure 2-1. Operation Panel

Logic Address Plug/Select Indicator

The Logic Address Plug activates switches that establish the logical address of the device. When the select light on the address plug is lit (yellow), it indicates activity from the controller. Logic Address Plugs are available with numbers 0 through 3 and are supplied with the unit. (They are also available as accessories.) Each device must have a different plug number. A single drive subsystem must use Plug 0 only.

START Button/READY Indicator

Depressing the START button powers-on the unit. The READY indicator (green) flashes until the discs are up to speed, the heads are loaded, and no fault condition exists (power-on sequence). The READY indicator lights steadily when the power-on sequence is complete. Pressing the START button again powers-off the unit; the READY indicator flashes until disc rotation has stopped, then goes out.

FAULT Clear Button/FAULT Indicator

The FAULT indicator lights (red) if a fault exists within the disk unit. It is turned off by momentarily pressing the FAULT clear button, by a fault clear command sent by the controller, or by a disk drive power-on operation.

WRITE PROTECT Button/ WRITE PROTECT Indicator

Depressing the WRITE PROTECT button (labeled WRT PRT) places the disk unit in the write protect mode which prevents writing operations; the WRITE PROTECT indicator lights (red). Pressing the button again deactivates the protection and the indicator goes out.

AC Power Distribution Unit (PDU)

Once the unit is plugged into an active AC outlet, AC power is controlled by the main circuit breaker, located behind the lower right front of the cabinet door (Figure 2-2). For normal operation, the breaker is ON to continue supplying AC power to the drives. This circuit breaker may be used to turn off all power to the drive cabinet.

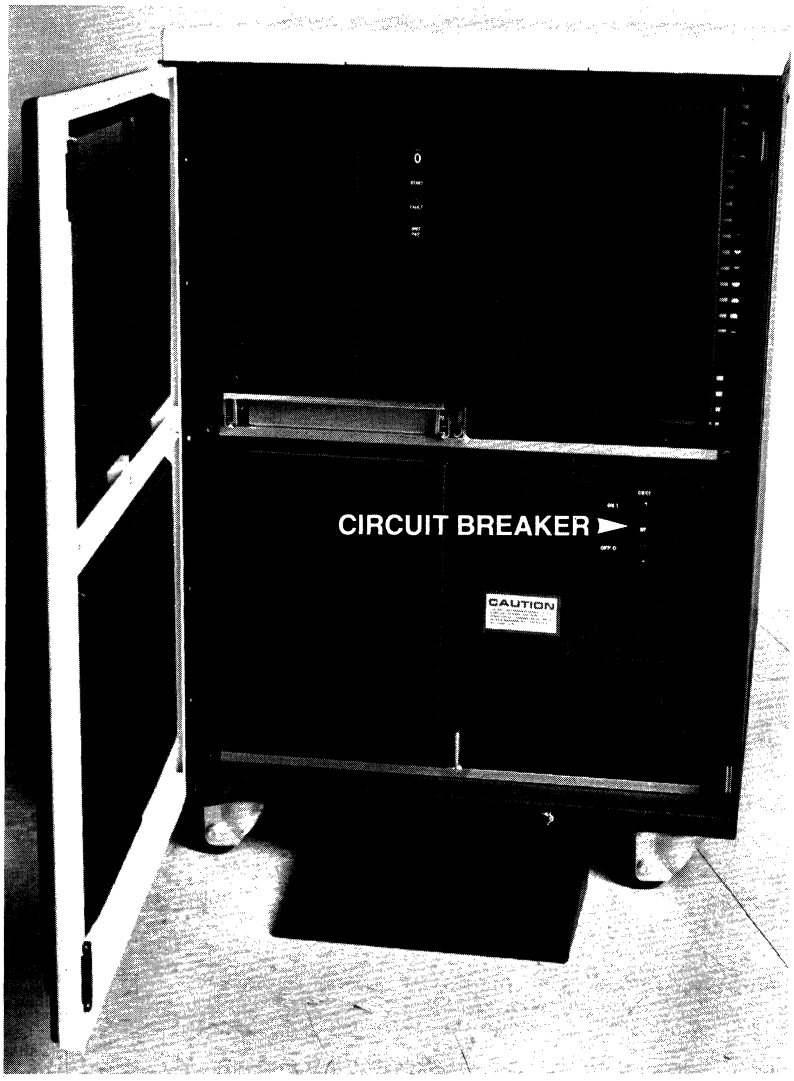


Figure 2-2. Location of Main Cabinet Circuit Breaker

Section 3
Operation

This section describes the operating and maintenance procedures for the MSU9617/9618/9619/9620 fixed-disk units.

CAUTION

Damage to the disk drives may result if the MSU subsystem is relocated.

The MSU cabinet and drives when fully assembled are not designed for mobility.

- Movement of the MSU cabinet with drives installed is allowed for CSD servicing only.
- When relocation is required, the drives must be removed from the cabinet and transported in their shipping container.

Power-On Procedure

In the following procedure, it is assumed that all cables have been properly connected.

1. Open the door on the front of the unit and make sure the MAIN AC circuit breaker is in the ON position (Figure 3-1).
2. Press the START button (Figure 3-2). If the unit is working properly, the READY indicator (located on the START button) will flash, indicating that the power-on sequence is in progress.
3. Observe that the READY indicator lights steadily within 45 seconds, indicating that the power-on sequence has been completed. (The MSU9619 and 9620 will automatically perform a self-diagnostic test that lasts about ten seconds and causes a buzzing sound on each power-on sequence.)
4. Observe that the FAULT indicator is not lit.
5. Make sure WRITE PROTECT is not set, if writing is to be performed.
6. The unit is now ready to read or write data.

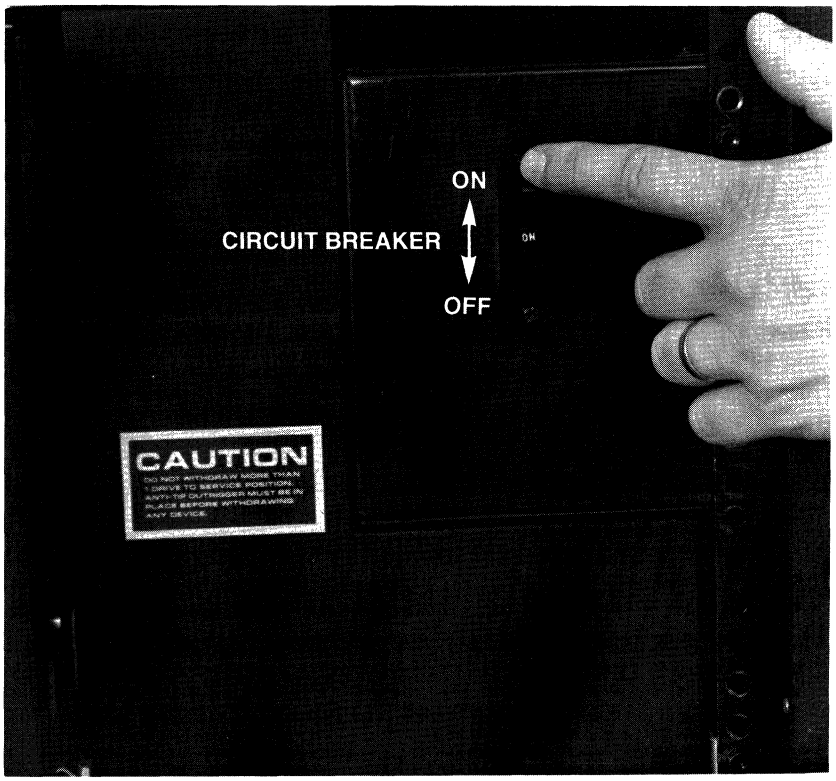


Figure 3-1. Circuit Breaker

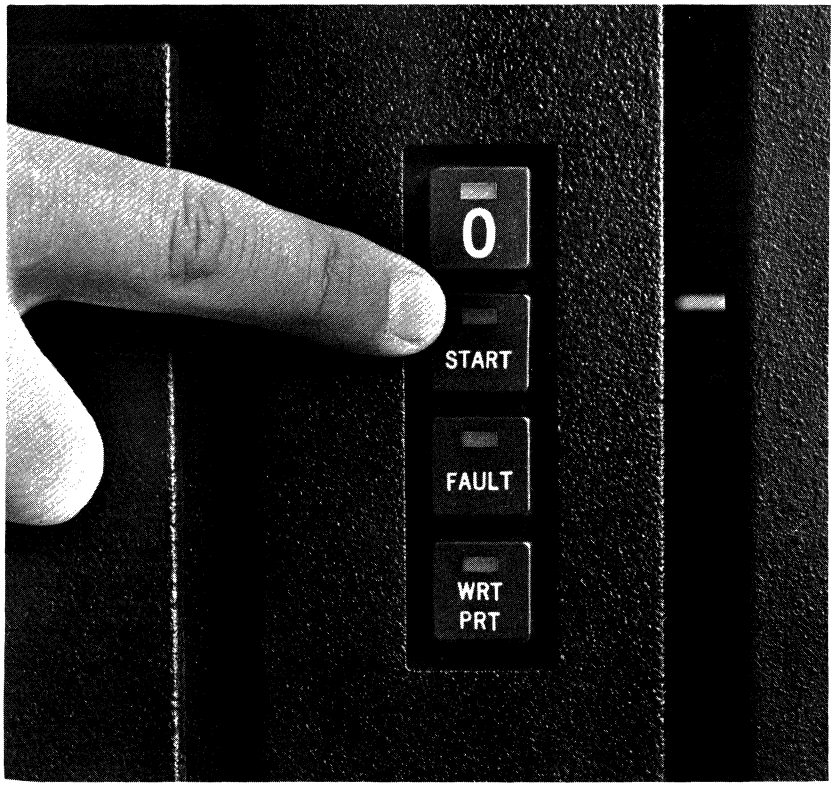


Figure 3-2. Initiating Power-On

Power-Off Procedure

1. Press the START button (releasing it from the ON position). The READY indicator will flash, indicating that power-off is in progress.
2. Observe that the READY indicator goes off within 45 seconds, indicating that power-off is complete. Normally, the main circuit breaker is left ON.

Changing the Logic Address Plug

A Logic Address Plug may be changed easily by grasping the plug firmly and pulling out towards you (as you face the unit). Plugs may be interchanged between units. This is useful if a unit should become inoperative. However, no two units connected to the same controller can have the same logical address (number).

Filter Replacement and Cleaning

The air filter for each drive must be clean to ensure proper air circulation through the drive. The filter is located behind the filter cover shown in Figure 3-3. You should inspect the filter of each drive periodically and either replace or clean it when it is dirty. Cleaning the filter is recommended only if replacement filters are not available. The interval for filter maintenance depends on the operating environment. In computer room conditions, a 6-month interval is suggested. In other conditions, the filter should be checked more frequently. Replacement filters (Catalog No.: M1463 – box of ten) can be obtained through Honeywell using the *National Distribution Operations Sales Catalog Supplies and Accessories* (Order No. GF60).

Filter Replacement

1. Remove the filter cover that is inserted in the front panel by pulling firmly towards you (as you face the drive) to disengage the cover catches (Figure 3-3).
2. Remove the old filter (Figure 3-4). Notice how the filter fits into place so that the new one can be installed in the same position.
3. Install the new filter.

IMPORTANT

Be sure not to disturb the maintenance toggle switch. It must be down (OFF).

4. Replace the filter cover by aligning the catches on the cover with the slots on the panel and pushing until the catches snap into place (Figure 3-5).

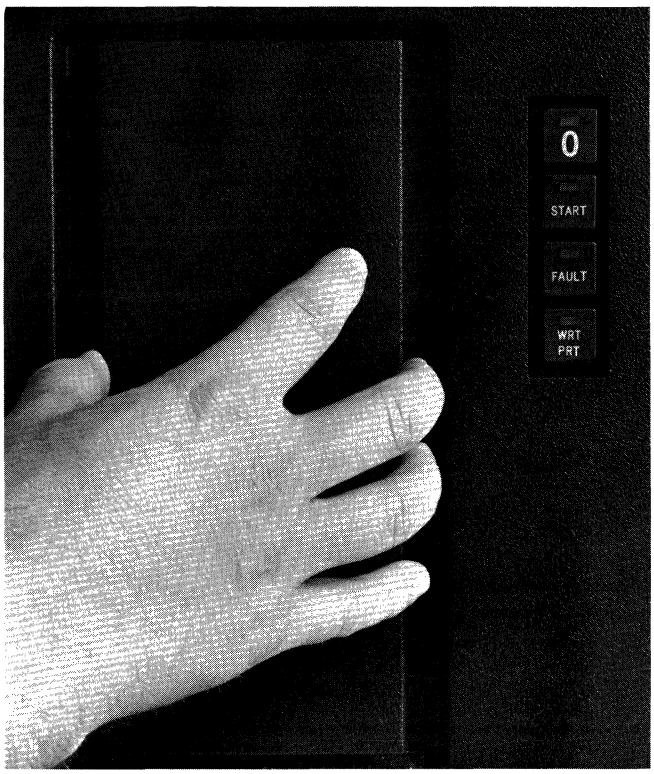


Figure 3-3. Removing Filter Cover

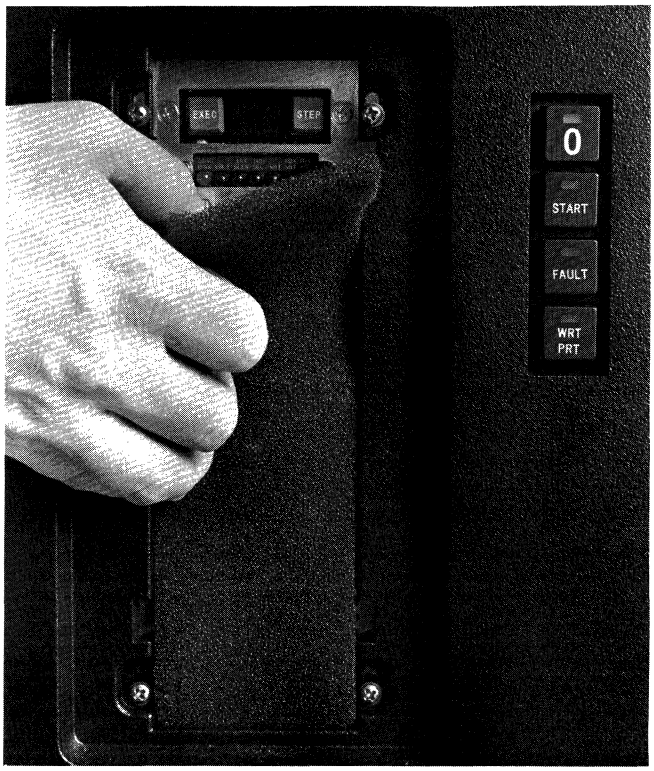


Figure 3-4. Removing Old Filter

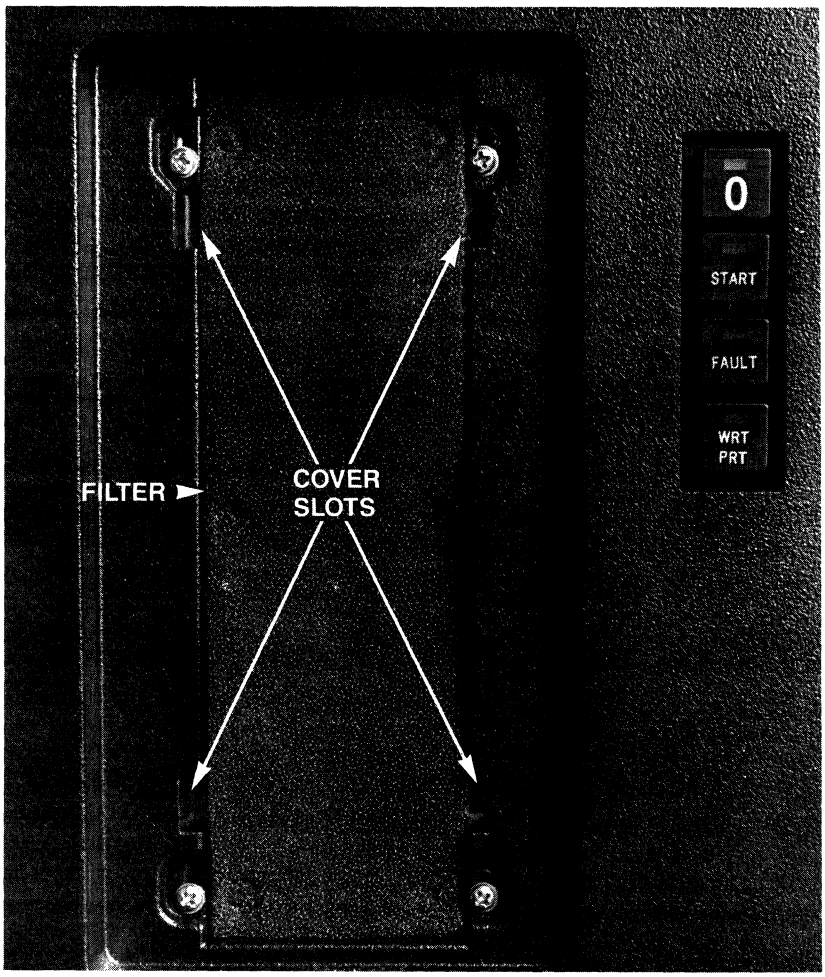


Figure 3-5. Filter Cover Catches

Filter Cleaning

The filter should not be cleaned if replacement filters are available.

1. Remove the filter cover that is inserted in the front panel by pulling firmly towards you (as you face the drive) to disengage the cover catches (see Figure 3-3).
2. Remove the filter (see Figure 3-4).
3. Clean the filter by agitating it in a solution of water and mild detergent.
4. Rinse the filter thoroughly with clean running water and allow it to dry completely.
5. Install the filter.

IMPORTANT

Be sure not to disturb the maintenance toggle switch. It must be down (OFF).

6. Replace the filter cover by aligning the catches on the cover with the slots on the panel and pushing until the catches snap into place (see Figure 3-5).

Software Loading and Saving Procedures

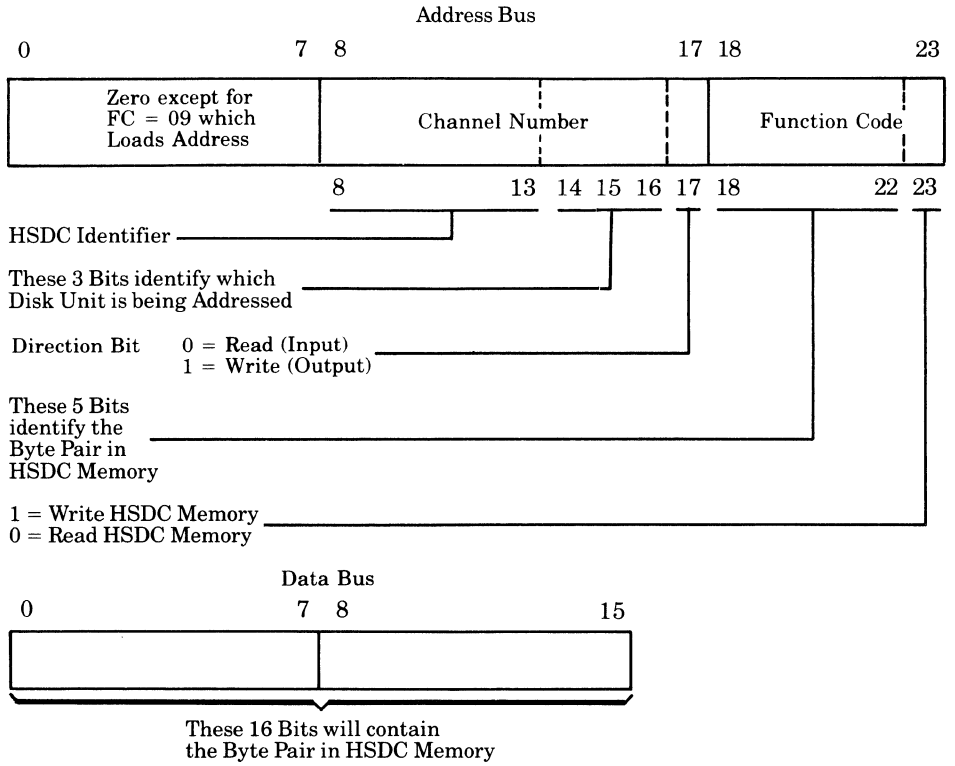
The LOAD/SAVE procedures used to load data from a tape (1/4-inch cartridge or 1/2-inch GCR) to a fixed-disk (MSU9617/9618/9619/9620 Units) or save data from a fixed-disk to a tape are found in *DPS 6 Central Processor Operation* (CT43) or in the *GCOS 6 MOD 400 Software Installation Guide* (CZ11). These procedures are also used for initial software installation of MOD 400 from a tape (acquired from Honeywell).

Appendix A
Programming

HSDC and HPDC[1] Memory and Command Interpretation

Both the High Speed Disk Controller (HSDC), a 16-bit controller, and the High Performance Disk Controller (HPDC), a 32-bit controller, have a 128-word Read/Write memory that is divided into 32 registers (16 bits per register) for each of the four HSDC channels (or ports). The address of each of the various registers in the HSDC is a combination of three bits of the channel number and the five high-order bits of the function code used to write into or read from a particular register.

The CP can read or write any register as long as the specific channel is not busy. To write into a register, an I/O *output* command is used; reading is done with an I/O *input* command. Addressing of the various registers relates to the I/O command as follows:



[1]Although the HPDC acronym has been omitted, the information in this appendix pertains to both the HSDC and the HPDC; they are similar in software function.

The format shown is for a Write cycle on the bus. For a Read cycle, the memory data will be returned from the HSDC on a second bus transfer.

To perform a specific operation, software first loads the address, range, and configuration registers. The task register is loaded last and specifies the operation to be performed. The HSDC begins command execution when it receives the task word.

Channel Number

Units attached to the HSDC are software addressable via channel numbers. Each disk unit has two such channel numbers assigned, differing only in their low-order bit position called the direction bit.

The channel number for the HSDC is separated into three fields:

- HSDC Identifier (bits 8-13) — switch selectable and assigned at system installation time.
- HSDC Port (bits 14-16) — identifies which of the four disk units is being addressed. Port assigment to a particular disk unit is made when the operator inserts an interchangeable Logic Address Plug into it.
- Direction Bit (bit 17) — specifies in the IOLD command whether it is an input or output data transfer. For all other commands, the direction bit is ignored by the hardware.

Simultaneity

The HSDC provides a single level of simultaneity (only one data transfer can be active in the subsytem). However, the HSDC will accept a data transfer command to unit B while unit A is performing a data transfer, but will not start the data transfer on B until A's data transfer is completed. Following completion of a data transfer operation, any seek orders received should be initiated prior to the initiation of any data transfer operations. Channels are serviced on a rotating priority basis so that no one channel or channels can dominate HSDC usage.

Interrupts

An interrupt will be attempted whenever a channel interrupt level is not zero, and an operation initiated by an Output Task Word or Output Control Word instruction is completed or the Attention bit is set in the Status Word. If a negative response is received during an interrupt cycle, the HSDC will store the inter-

rupt until it can be retried. In the meantime, the HSDC can receive commands and/or conduct data transfers on any of the other channels. The channel with the pending interrupt will remain busy and the HSDC will not accept any commands issued to that channel except an Output Control Word.

If the interrupt level of a channel is zero (either via intialization or loaded to zero) no interrupts will be attempted for that channel. If a condition or event occurs that would normally cause an interrupt, the appropriate bits in the Status Words will be set, but no interrupt will be attempted or accepted.

If the interrupt level is set to zero when an interrupt is pending via an Output Control Word (Initialize) or a Master Clear, the pending interrupt will be discarded.

Data Format

Fixed sector format is used by the HSDC, which defines 96 equal sectors per track. However, because a list of defects occupies the space reserved for the first sector (home address), only 95 (or 63 sectors, depending on the unit) are available for user space. See Figure A-1 below.

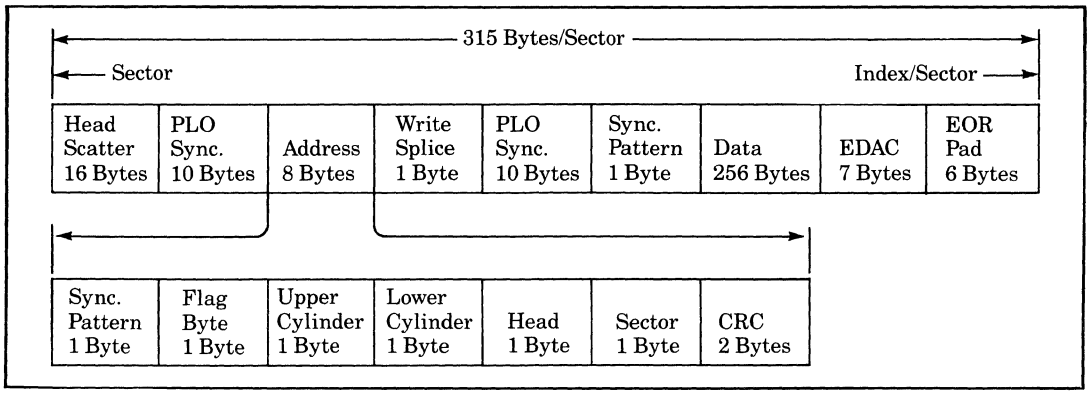


Figure A-1. Data Format

EDAC Functionality

The seven-byte EDAC field appended to the data field provides for the correction of error bursts of up to 11 bits and detection of an error burst of up to 22 bits. Any bit errors separated by more than 10 bits are not correctable.

During update read and write operations, the detection of any read error in an ID field will cause bit 4 of Status Word 1 to be set. The search (update read or write) will continue. If a successful search is not made prior to detection of two Index Marks, the operation is terminated with bit 4 set. Two retries are attempted

before the operation is finally terminated. If a successful search is made prior to detection of two Index Marks, bit 4 is reset and the operation continues in a normal fashion. In neither case will any error correction be performed on the ID field.

If a read error is detected following the transfer of a sector data field to main memory, one of two situations is possible:

1. If the error is not correctable, a retry will be initiated (see Read Error Retry).
2. If the error is correctable via EDAC, the HSDC will automatically perform the required correction in main memory, set bit 9 of Status Word 1, and bit 0 of Status Word 2, and continue the data transfer operation. Note that the loss of a revolution of the media will occur during the correction period.

Read Error Retry

If an uncorrectable read error is detected following transfer of a sector data field to buffer memory, the following retry procedure will be invoked automatically by the HSDC.

1. Three retries
2. Three retries with clock retarded
3. Three retries with clock advanced
4. Three retries with offset in
5. Three retries with offset in, clock retarded
6. Three retries with offset in, clock advanced
7. Three retries with offset out
8. Three retries with offset out, clock retarded
9. Three retries with offset out, clock advanced

Note that:

- EDAC is attempted only once at the end of 27 retries.
- The read error retry is applied only to uncorrectable data field errors during Read Data commands (does not apply to format or diagnostic commands; bit 4 of Status Word 1 is set in these cases as applicable).
- A latency period is entered between retries, i.e., other channels on the HSDC will be serviced if there is any activity on them.
- A loss of at least one revolution will occur for each retry.

- Any offset or clock change condition will be automatically restored after retry (successful or unsuccessful).

The read error retry has one of two results:

- If the error is not recoverable, bit 4 of Status Word 1 is set and the operation is terminated.
- If the error is recoverable, bit 9 of Status Word 1 and bit 1 of Status Word 2 are set and the data transfer operation is continued.

Instructions

Table A-1 lists the I/O commands to which the integrated controller and disk units respond. A detailed description of each instruction follows this table.

Table A-1. I/O Bus Commands

Type	Function Code (Hex)	Description
Output		
	09[a]	Output Address
	0D	Output Range
	0F	Output Offset Range (not used)
	11	Output Configuration Word A
	13	Output Configuration Word B
	15	Output Configuration Word C
	03	Output Interrupt Control
	07	Output Task Word
	01	Output Control Word
Input		
	00	Initial Controller ID
	08	Input Memory Byte Address
	0A	Input Memory Module Address/QLTI
	0C	Input Range
	0E	Input Offset Range
	10	Input Configuration Word A
	12	Input Configuration Word B
	14	Input Configuration Word C
	02	Input Interrupt Control
	26	Input Identification Code
	06	Input Task word
	18	Input Status Word 1
	1A	Input Status Word 2
	3C	Firmware Revision
	20	Retry Counter
Diagnostic		
	Any Even Code	Read HSDC Registers
	Any Odd Code	Write HSDC Registers

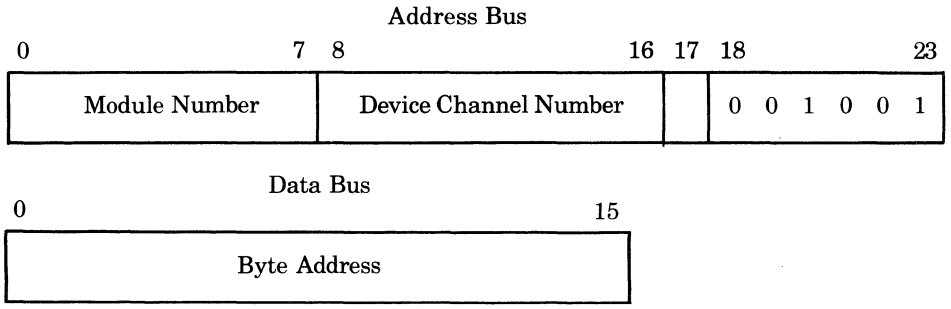
[a]Function Code 09 as executed by the CP results in execution of functions 09 and 0D.

Output Commands

Command Output Address

Function Code 09

Format



Function

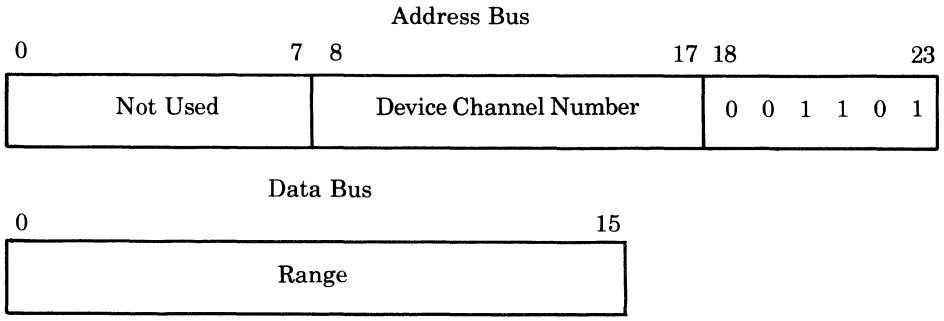
This instruction loads a 24-bit address into the address register associated with the referenced channel device. The address refers to the starting (byte) location in main memory where the HSDC will start input or output data transfers. Bits 0-7 of the Address Bus (Module Number) are the most significant bits of the address. Data transfers to or from memory will normally be on a word basis, but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer (identified by this instruction) begins or ends on an odd byte boundary.

Bit 17 of the Address Bus (direction bit of the channel number) determines the direction of any subsequent data transfer operation. A logical one specifies an output operation (writing on media), while a logical zero specifies an input operation (reading from media).

Command Output Range

Function Code 0D

Format



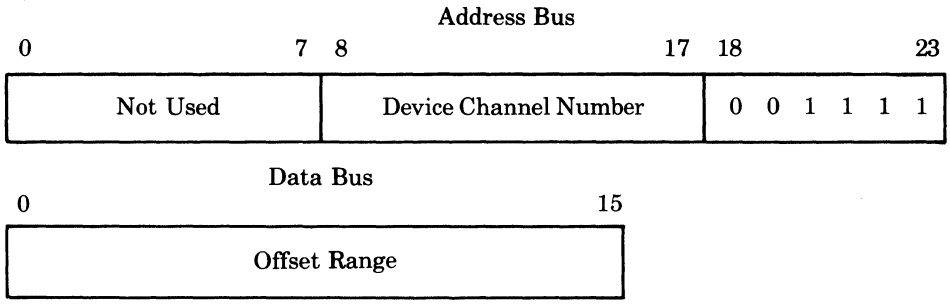
Function

This instruction loads the range register associated with the referenced channel. The (16-bit) quantity loaded (data bus) is the number of bytes to be transferred during the data transfer that is being set up. The number is a positive binary quantity and is decremented by the HSDC after each memory transfer. A range of zero will result in a premature end-of-operation termination for any Read or Write command that may be subsequently issued (refer to Output Task Word command). Any range register residue will be applied to the next command unless reset by another IOLD instruction.

Command Output Offset Range

Function Code 0F

Format



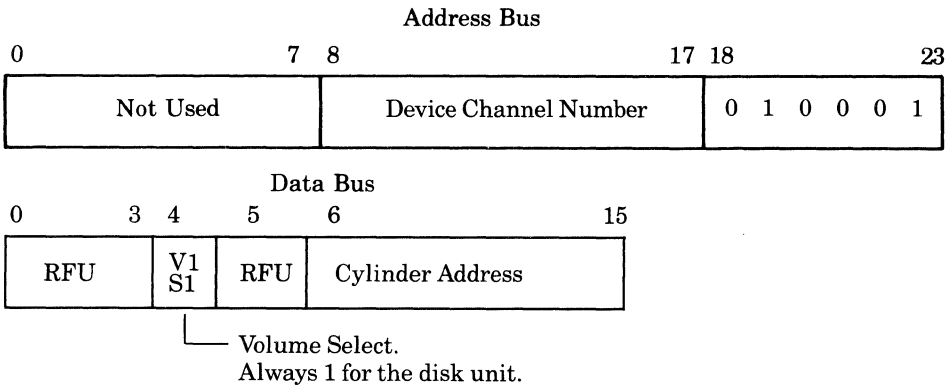
Function

This instruction, implemented for compatibility reasons, loads the output offset range register associated with the referenced channel. No other action takes place, except the normal instruction termination.

Command Output Configuration Word A

Function Code 11

Format



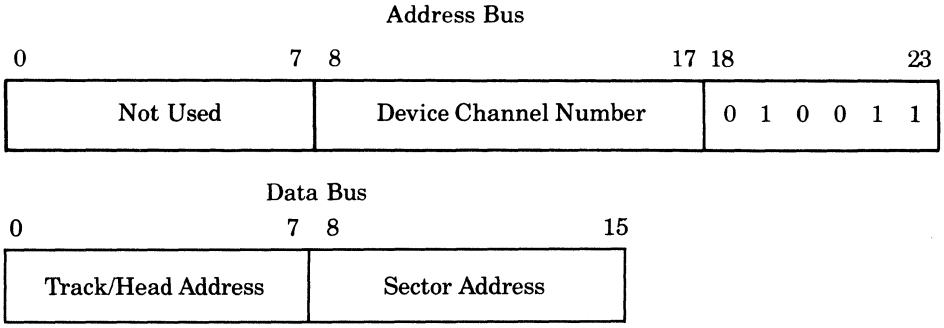
Function

This instruction loads Configuration Word A for the device corresponding to the referenced channel. The cylinder address (bits 6-15) is used as the seek argument during Seek operations. The complete word is used as the two high-order bytes of a sector ID field to be searched for during a data field Read or Write operation. Bits 0-3, and bit 5 are reserved for future use (RFU). The maximum cylinder address permissible is 710 for MSU9619/9620 and 822 for MSU9617/9618. Bit 4, the volume select bit, is defined as: 0 = removable volume; 1 = fixed volume.

Command Output Configuration Word B

Function Code 13

Format



Function

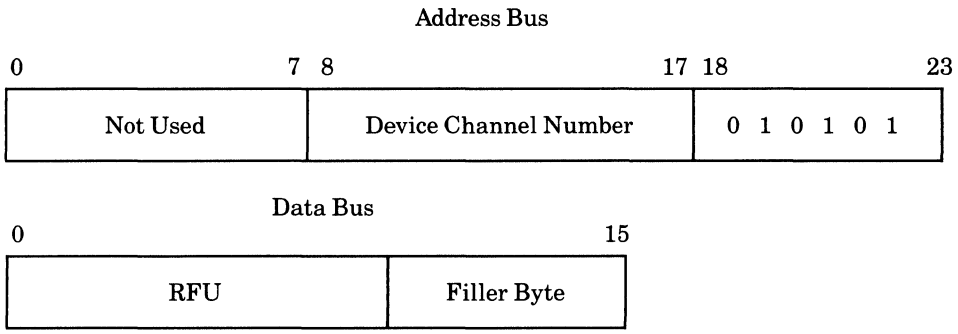
This instruction loads Configuration Word B for the device corresponding to the referenced channel. This word is used as the two low-order bytes of a sector ID field to be searched for during a data field Read or Write operation. Bits 0-7 provide the track address for any Read or Write operations: Even = upper surface address; Odd = lower surface address.

The subsystem will treat bits 8 through 15 of Configuration Word B as a sector number. This number will be incremented after operating on a data field during a data field Read or Write operation (refer to Output Task Word command).

Command Output Configuration Word C

Function Code 15

Format



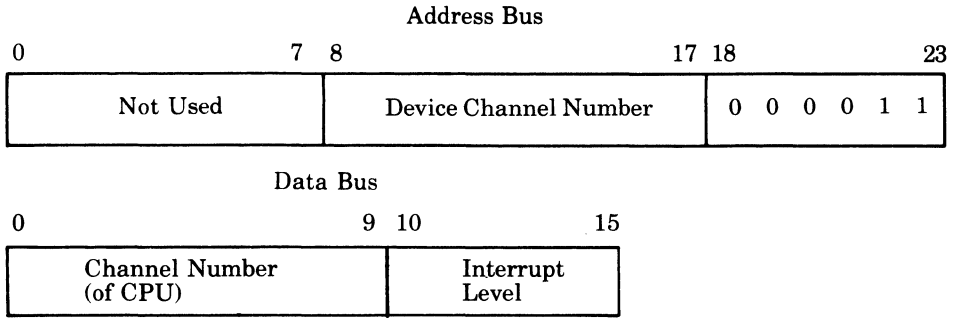
Function

This instruction loads Configuration Word C to the referenced channel. The low-order byte of Configuration Word C is used for filling the data field during the execution of a Format Write instruction. The filler byte is initialized to 6D.

Command Output Interrupt Control

Function Code 03

Format



Function

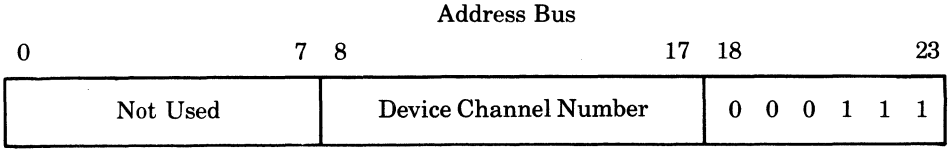
This instruction loads, for the referenced channel, the interrupt level, and the channel number of the CPU. The level number is a 6-bit quantity and is positioned on the data bus as shown. Bits 0-9 of the data bus contain the CPU channel number to which subsequent interrupts are to be directed.

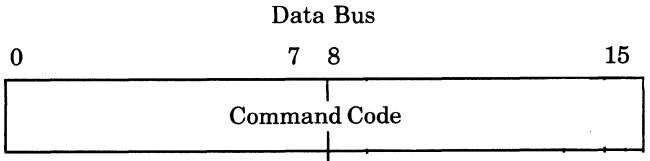
If an interrupt level of zero is loaded, the subsystem will not generate or save interrupts for any events that occur while the interrupt level is zero. The interrupt level is set to zero whenever the subsystem is initialized.

Command Output Task Word

Function Code 07

Format





0 0 0 0 0 0 0 0	MBZ	Recalibrate
0 0 0 0 0 0 0 1	MBZ	Seek
1 0 A R R 0 0 0	MBZ	Format Write
1 0 A R R 0 0 1	MBZ	Read/Write Data
1 0 A R R 0 1 0	MBZ	Diagnostic Format Read/Write
1 0 A R R 0 1 1	MBZ	Diagnostic Read/Write Data
1 0 A R R 1 0 0	MBZ	Format Read/Write ID
1 1 0 0 0 0 0 0	MBZ	Wraparound Read/Write Buffer
1 1 0 0 0 0 1 0	MBZ	Read SPM

where:

A =Automatic Seek Bit
R =Reserved for Future Use (RFU). These must be "don't care" bits when not implemented.
MBZ =Must Be Zero

Function

This instruction outputs a Task Word to the referenced channel. The coding of bits 0-7 represent the operations that are to be performed. When this instruction is accepted, the channel enters the busy state and the indicated task is initiated or stacked. All address, range, and configuration information must be loaded prior to execution of this instruction. The direction of data transfer is indicated in the low-order bit of the most recent output address instruction. For example, if the data field encoding of the Task Word is received when a "Read" channel number is indicated, then a Read Data command will be executed. Note that track selection is performed for each media data transfer command prior to the initiation of the data transfer and is based on the current contents of Configuration Word B.

Bits 2-4 of the command code have specific meaning for all media data transfers as follows:

Bit 2 — Automatic Seek

If this bit is a logical zero, the data transfer will be initiated based on the current cylinder position of the drive.

If this bit is a logical one, a Seek Cylinder operation, based on the current contents of Configuration Word A, will be initiated to the drive. Other channels may be serviced by the HSDC during the seek latency period. At seek completion, no seek complete interrupt will be generated to the bus channel, and the specified data transfer operation will be initiated.

Bits 3 and 4 — Reserved for future use (RFU).

Recalibrate

The Recalibrate command causes the channel to move the device's positioner to cylinder zero, select track zero, and send a Fault Clear command to the disk unit. This instruction is intended as in Initialization command to guarantee that the position location information in the HSDC is correct and that all device faults are cleared. Completion of the Return to Zero operation by the device will result in an On Cylinder status and Seek End.

Seek

The Seek command in the Task Word causes the channel to move the device's positioner to the cylinder indicated in Configuration Word A. If the cylinder specified is greater than the innermost cylinder or an error occurs during positioner movement, then an error bit will be set in the Status Word. Completion of a positioning operation (whether or not any physical movement occurred) by the device will result in the generation of an interrupt. Note that seek completion as a result of an automatic seek will not result in an interrupt.

Format Read ID

The Format Read ID command causes the channel to read all Identifiers (IDs) on a track beginning with the first user sector after Index and in the order in which they are recorded. IDs are transferred to memory beginning at the memory location specified in the subsystem's memory address register. This address is the address loaded by the most recent Output Address (IOLD) instruction if no data transfer has occurred since that instruction was executed. If one or more data transfers have been executed since the last Output Address IOLD instruction, then the starting memory address used for this operation is the byte address immediately following the end of the most recent data transfer executed for this device (either read or write).

If bit 8 (B) of the Command code is a one, then the CRC bytes of any sector identifier read are ignored. If bit 8 of the Command code is a zero, then the CRC bytes of any sector identifier read are checked.

Data is transferred until an uncorrectable read error occurs (except as noted for bit 8), the range is satisfied, or the entire track is read (Index is detected).

Normal range for this command (to read one complete track) is

(R = 4 x 95) 380 bytes for the MSU9619/9620
and (R = 4 x 63) 252 bytes for the MSU9617/9618

where:

4	=	number of bytes in any ID
95 or 63	=	number of user sectors per track

If this command is terminated due to end of track before the range is satisfied, the residual range is available via the Input Range command. An uncorrectable read error in any field (except as previously noted for bit 8 of the Command code equal to one) causes the operation to be terminated with the read error bit set in the Status Word (bit 4). The field in error can be determined through examination of the residual range. If a read error is detected in an ID field, the range is decremented for the ID field only.

If the range register is zero when this command is received, the task is immediately terminated. No data is read or transferred. Track selection of the operation is based on the current contents of the track address of Configuration Word B.

If bit E of the Task Word Command is set to one, the 21 bytes of the Home Address are read starting with the Cylinder Address bytes and ending with the F0 byte. The Defect Log bytes are used by the firmware in reallocating bad sectors to the Error Log Cylinder. This command is used for diagnostic purposes only.

Format Write

The Format Write command causes the channel to format the track which is positioned under the Read/Write head specified by Configuration Words A and B when this command is received. Dependent on the model, 63 or 95 equal length sectors will be written starting at Index (excluding the 96th section). The sector ID fields will be read from memory beginning with the memory location specified in the subsystem's memory address register. Bit 8 is zero for this command.

The data fields are filled by the HSDC with the 6D filler byte. The range to format one complete track is 380 or 252 bytes for MSU9619/9620 or MSU9617/9618, respectively.

Notes:

1. Format Write ID and Format Write codes have the same function.
2. Read errors can occur on reallocated sectors which were found to contain uncorrectable errors.
3. Error sector reallocation is performed at this time. Identified error sector ID field CRC bytes are written incorrectly, i.e., complemented CRC.

If a range other than 380/252 is specified, Program Error bit 5 is set to one in Status Word 1. If the range register is zero when this command is received, the task is immediately terminated (end-of-operation) and no data is written.

If bit E of the Task Word Command is set to one, the 21 bytes of the Home Address are written starting with the Cylinder Address bytes and ending with the F0 byte; the Defect Log bytes are used by the firmware in reallocating bad sectors to the Error Log Cylinder. This command is used for diagnostic purposes only. In addition, if bit D is set to one, the Home Address extended gap is written.

Read Data

The Read Data command causes the channel to locate the sector defined by the sector ID image loaded in Configuration Words A and B and to begin transfer of the data field of (at least) that sector to buffer memory. Data will be transferred to main memory from the HSDC buffer memory when the range is satisfied or the buffer is full, beginning with the memory location specified in the subsystem's memory address register. When the buffer is full and the range is not zero, the next data transfer to main memory occurs when the buffer is full again or the range decrements to zero.

When the transfer, from the disk to the buffer memory, of the first specified sector data field is completed (without error), the sector number field of Configuration Word B will be incremented. If the initial range is greater than 256, the sector on that track represented by the updated contents of Configuration Words A and B will be located and data tranfer will continue with the new sector's data field. This operation will continue until the range is satisfied, an uncorrectable read error occurs, or the record specified by Configuration Words A and B cannot be located on the track or the reallocated track (as indicated by the detection of two Index Marks without a successful compare). If the specified record cannot be located, an unsuccessful search will be posted in the Status Word (bit 7). Note that track and cylinder switching may occur.

Track selection for the operation is based on the current contents of the track address of Configuration Word B.

If an uncorrectable read error is encountered in a data field, the operation will be terminated and the read error bit in the Status Word will be set (bit 4). The sector number field of Configuration Word B will contain the address of the record in error. If a read error is encountered in an ID field, a mis-compare result will be assumed and the search will continue. In this case, the read error bit will be posted in the Status Word so that if the desired record is never located, the operation will be terminated with both the unsuccessful search bit and read error bit posted in the Status Word indicating that the reason for the mis-compare could be read error in the sector ID. If the search is eventually successful, the read error bit in the Status Word will be reset.

If this command is terminated before the range is satisfied, the residual range will be available via the Input Range command. If the range register is zero when this command is received, the task will be immediately terminated (end-of-operation). No data will be read or transferred.

Bit C (bit 14 of the Task Word), when set, inhibits read retries; conversely, retries are enabled when reset. This bit is intended to be used by diagnostics only for identification of bad spots on the media.

Write Data

The Write Data command causes the channel to locate the sector defined by the sector ID image loaded in Configuration Words A and B and to rewrite the data field of at least that sector. The data will be read from main memory, beginning with the memory location specified in the subsystem's memory address register. Data will be read into the HSDC's buffer memory until either the buffer is full or the range becomes zero; then the data is written on the disk one sector at a time. Rewritten data fields will be preceded by PLO sync bytes and data field sync bytes. When the buffer is full and the range is not zero, data transfer to the buffer memory resumes when the buffer is empty again.

If the range is less than 256, the remainder of the data field will be zero-filled. If the range was greater than 256, the sector represented by the updated contents of Configuration Words A and B will be located and the data field rewritten. This operation will continue until either the range is satisfied or the record specified by Configuration Words A and B cannot be located on the track or the reallocated track (as indicated by the detection of two Index Marks without a successful ID field compare). If the latter event occurs, unsuccessful search will be posted in the Status Word (bit 7). Note that track and cylinder switching may occur.

If a read error is encountered in an ID field, the ID contents will be ignored and the search will continue. In this case, the read error bit will be posted in the

Status Word so that if the desired record is not located, the operation will be terminated with both the unsuccessful search bit and the read error bit posted in the Status Word indicating that the reason for the mis-compare could be a read error in the sector ID. If the search is eventually successful, the read error bit in the Status Word will be reset.

If this command is terminated before the range is satisfied, the residual range will be available via the Input Range command. If the tag register is zero when this command is received, the task will be immediately terminated (end-of-operation). No data will be written.

Diagnostic Write Data

The Diagnostic Write Data command causes the channel to perform as if the Write Data command were specified except that EDAC characters will be written at the end of the data field updated as read from memory (not hardware generated). Only one sector can be updated by this command so that the range must equal 263 (256 + 7) bytes.

Track selection for the operation is based on the current contents of the track address of Configuration Words A and B.

Diagnostic Read Data

The Diagnostic Read Data command causes the channel to perform as if the Read Data command were specified except that the seven-byte EDAC field attached to the data field will also be transferred to memory (error detection/correction of the data field is not performed). Only one sector can be read by this command so that the range must equal 263 (256 + 7) bytes.

Diagnostic Format Write

The Diagnostic Format Write command causes the channel to perform as if the Format Write command were specified except that invalid CRC characters (true CRC one's complemented) will be written at the end of each ID field. Note that the data written in the data field is a pattern of bytes derived from the filler byte of Configuration Word C.

Diagnostic Format Read

The Diagnostic Format Read command is not implemented but the same functionality can be obtained by the Format Read ID with bit 8 set.

Wraparound Read/Write

Only one Wraparound level of command is available on the HSDC. When a Wraparound Write command is received the channel writes into the specified buffer starting from the main memory address indicated by the memory address register. Care must be taken not to exceed the buffer memory size.

When a Wraparound Read command is received (immediately following a Wraparound Write), the bytes previously loaded into the specified buffer by the previous Wraparound Write command are returned to the main memory at the address specified in the subsystem's memory address register. The bytes returned during this operation are the same as the bytes supplied by software in the preceding Wraparound Write command. The range supplied for the Wraparound Write must be the same as the range supplied for the Wraparound Read or the results are unpredictable.

A range smaller than or equal to 128 bytes should be specified for these commands. If a range of zero is specified, the command is immediately terminated (without being executed and without any status indications). If a range greater than a buffer size is specified, the results are uncertain and the Program Error bit (bit 5) of the Status Word 1 is set and the command is terminated immediately. In any case, the Wraparound Write and its associated Wraparound Read must start and end from the same memory boundary (byte or word). Execution of a Task instruction on another channel during a Wraparound sequence is unpredictable.

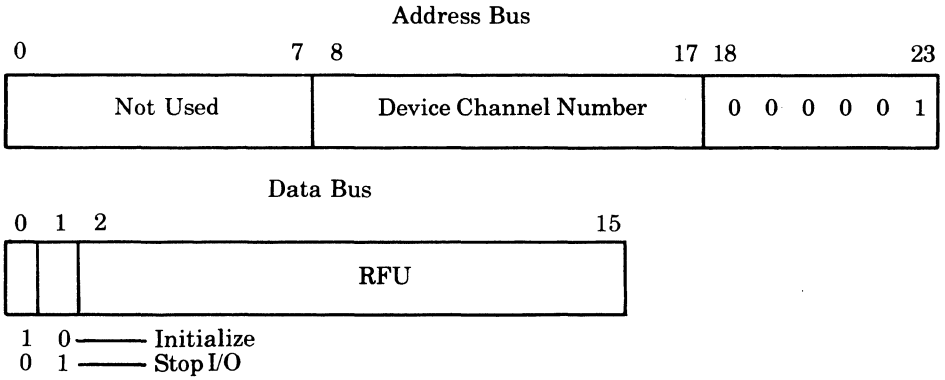
Read Scratch Pad Memory (SPM)

This command is used for diagnostic purposes only; 256 bytes of random access memory (SPM) are sent to the main memory. Contents are meaningful to the firmware only with the first 64 bytes corresponding to the Function Codes; consult the firmware listing for more details.

Command Output Control Word

Function Code 01

Format



Function

This instruction loads a control word into the referenced channel. This command will be unconditionally accepted by the channel regardless of its busy status.

Initialize

This command will cause the HSDC to reset to the same state that it enters after power up. When an initialize command is received by the HSDC, all of its channels are initialized (regardless of over which channel the command was received). A recalibrate will be executed on all disk units.

Operations that are in progress in the HSDC at the time of the initialization will be abruptly terminated and all software addressable registers will be initialized. No information about the terminated operations will be retained and no interrupts for the operations will be generated. The interrupt level for all channels will be set to zero (interrupts blocked). Note that execution of this command may result in invalid data on the media (if a Write command was in progress) or a device fault (if a Seek was in progress at the drive).

Stop I/O

This command causes any operation currently active on the specified channel to be abruptly terminated. If a data transfer operation is in progress, it will not be completed nor will any error checking be done. An interrupt will be generated for the operation terminated by this command as if the operation had come to a

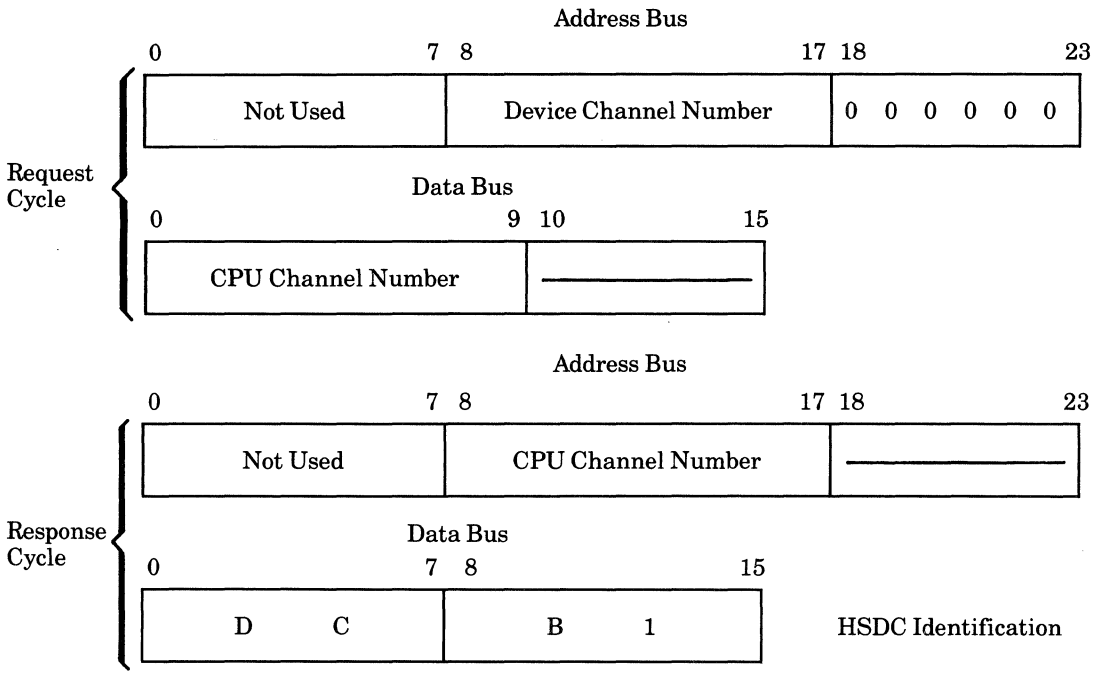
normal ending point. Status, address and range information, present in the HSDC when this command is received, will be retained. Note that execution of this command may result in invalid data on the media (if a Write operation was in progress) or a device fault (if a Seek operation had been initiated and not completed prior to a subsequent operation).

Input Commands

Command Input Initial Controller ID

Function Code 00

Format



Function

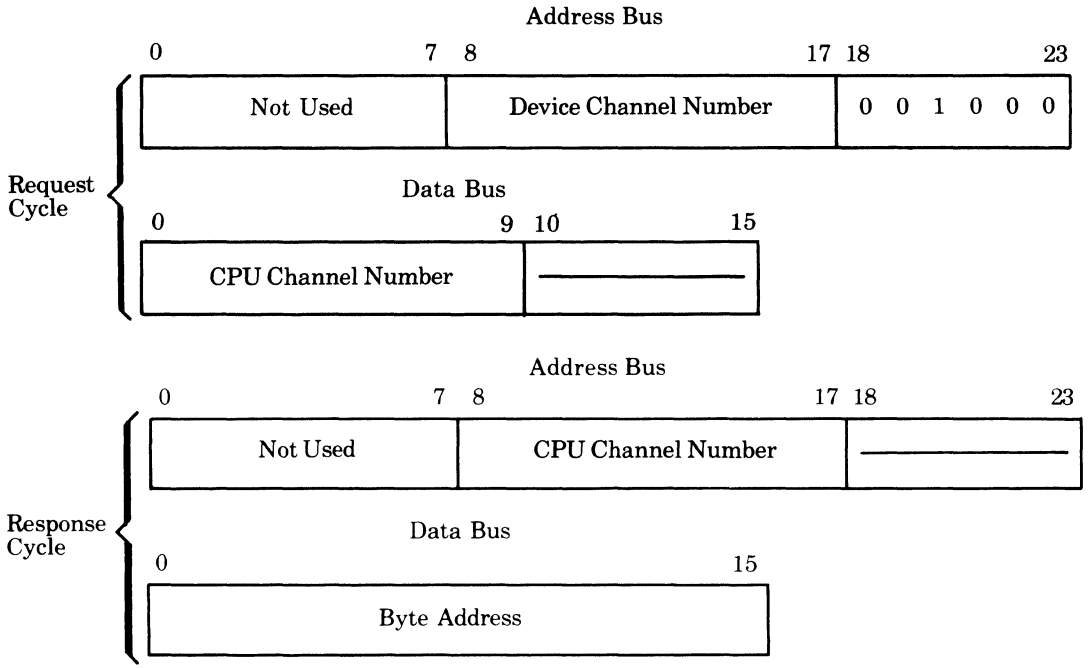
This instruction causes the current contents of the referenced channel's Initial Controller ID to be transferred to the requesting CPU channel.

(During the response cycle (second-half read), the HSDC returns, in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.) The data bus contains the unique numeric (HEX) identifier which is only true after the initialization command or after powering on. This command is intended to be used by diagnostics for controller or adapter identification.

Command Input Memory Byte Address

Function Code 08

Format



Function

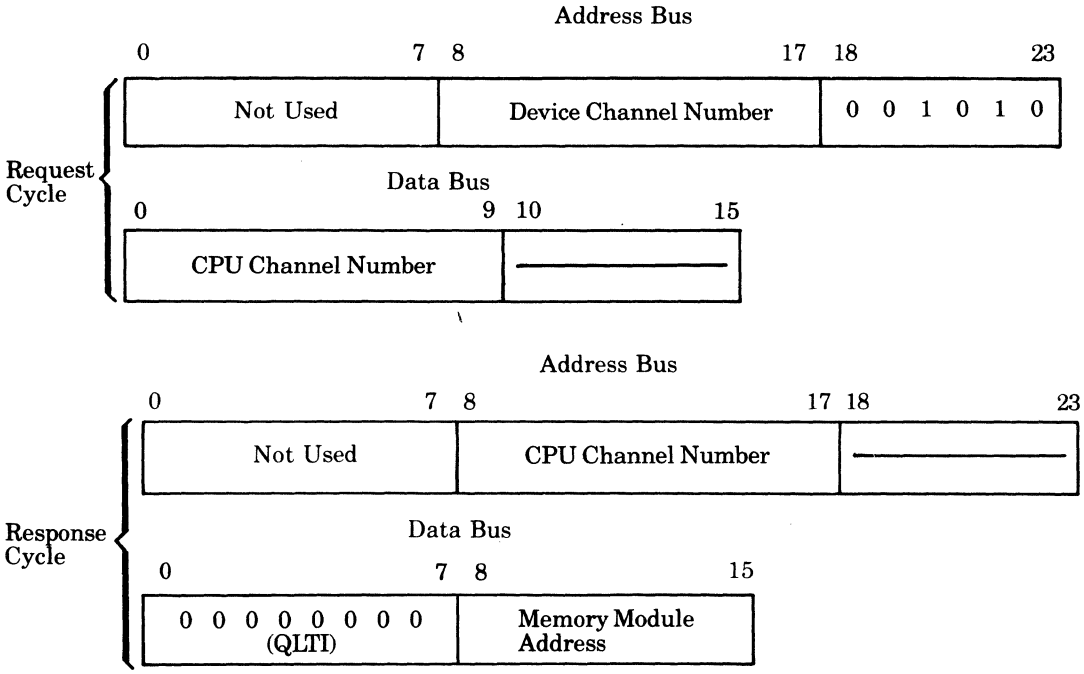
This instruction causes the current contents of the referenced channel's memory byte address to be transferred to the requesting CPU channel.

During the response cycle (second-half read), the HSDC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle. The data bus will contain the 16 low-order bits of the memory byte address currently stored for the specified channel in the HSDC. Note that if a Write command ended at a byte boundary (8 high-order bits of word), the memory address will reflect the next word (not the 8 low-order bits of the previous word). This command is used for diagnostic purposes only.

Command Input Memory Module Address/QLTI

Function Code 0A

Format



Function

This instruction causes the current contents of the referenced channel's memory module address to be transferred to the requesting CPU channel.

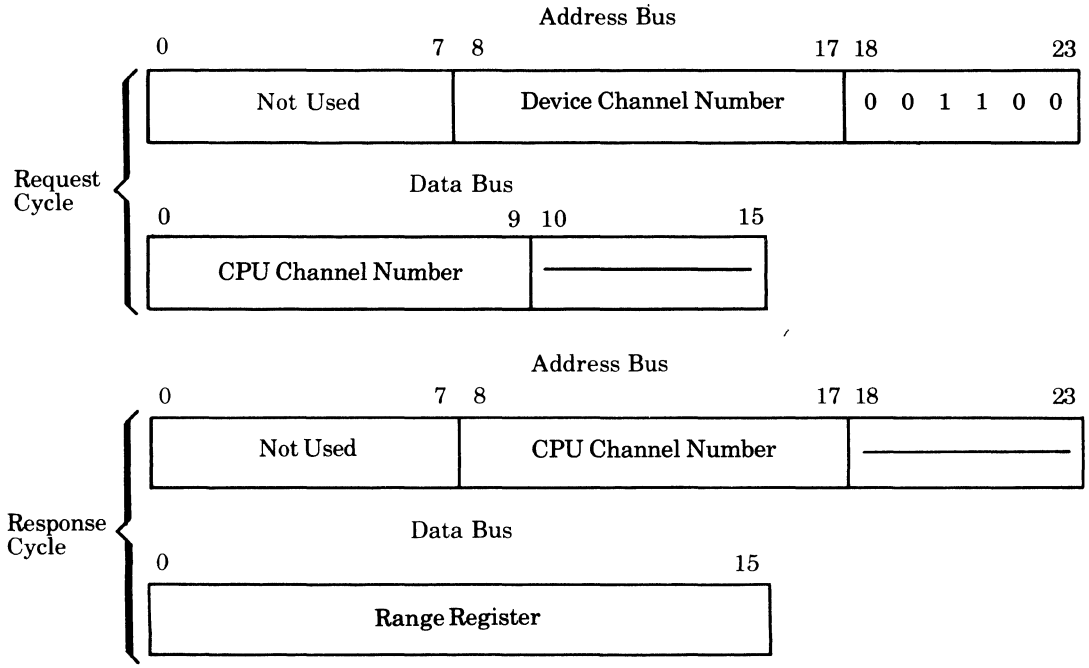
During the response cycle (second-half read), the HSDC will return in bits 8-23 of the address bus the same data that was received in bits 0-15 of the data bus during the request cycle. The data bus will contain the 8 high-order bits of the memory word address currently stored for the specified channel in the HSDC. This command is used for diagnostic purposes only.

The QLTIs are stored in the Scratch Pad Memory (SPM) buffer during the QLT. If the edge indicator remains lit, the QLTI buffer contains the code of a test which had failed on either the HSDC or on an adapter.

Command Input Range

Function Code 0C

Format



Function

This instruction causes the current contents of the referenced channel's range register to be transferred to the requesting CPU channel.

During the response cycle (second-half read), the HSDC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

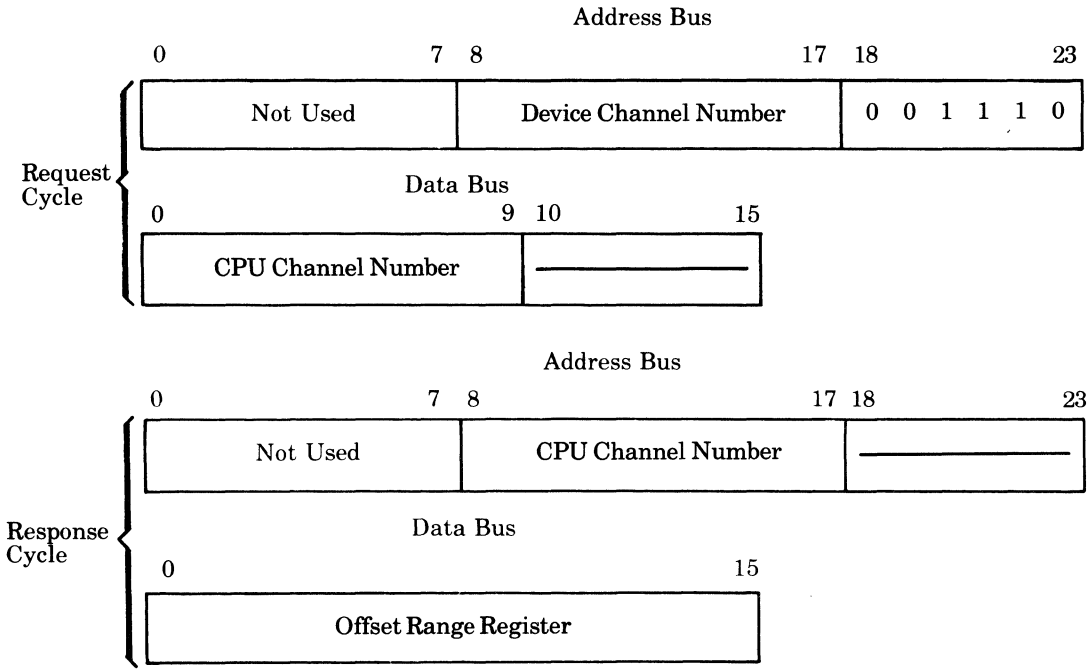
After the completion of a data transfer operation, the contents of the range register reflect the byte count of the data transferred:

- If the content value is greater than zero, the length of the physical sector(s) was less than the original range.
- If the content is zero, the length of the physical sector(s) was equal to or greater than the original range.

Command Input Offset Range

Function Code 0E

Format



Function

This instruction causes the current contents of the referenced channel's offset range register to be tranferred to the requesting CPU channel.

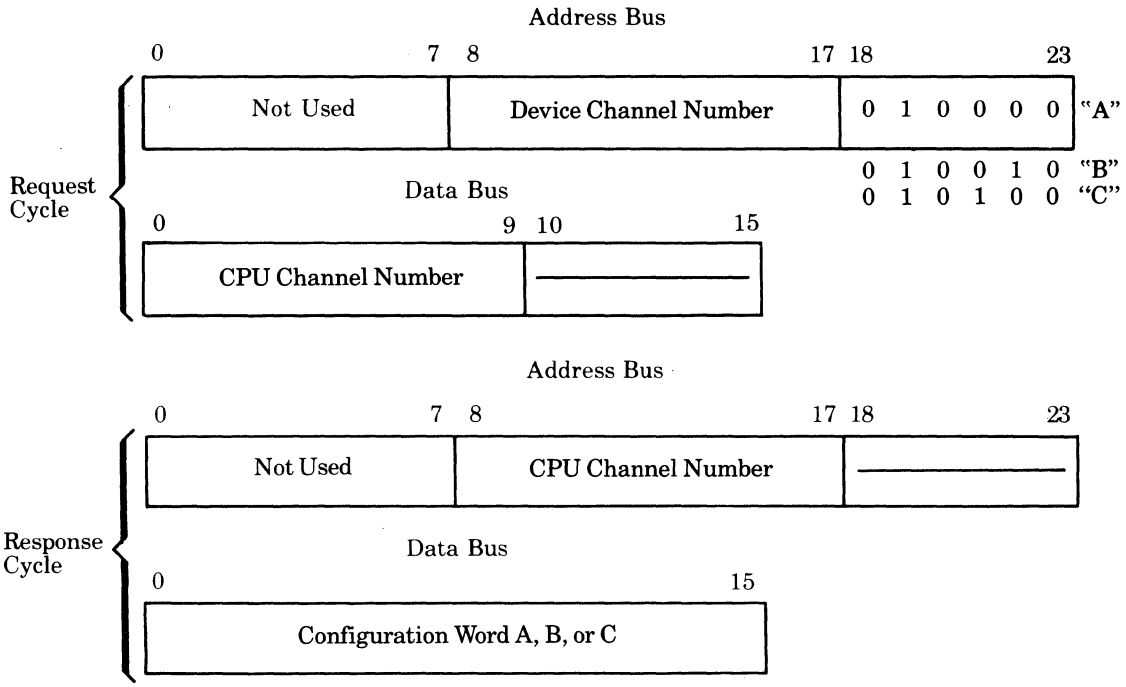
During the response cycle (second-half read), the HSDC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

This instruction, implemented for compatibility reasons, reads the contents of the offset range register which was previously loaded by the Output Offset Range command. No other action takes place except the normal instruction termination.

Command Input Configuration Word A, B, or C

Function Code 10, 12, or 14

Format



Function

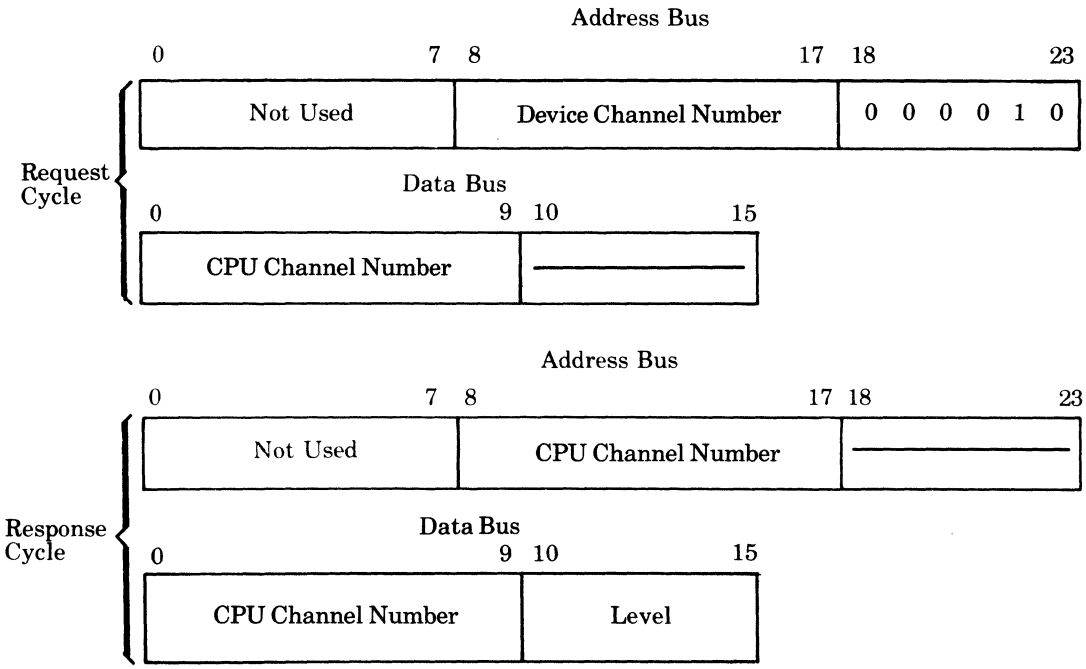
This instruction causes the current contents of the channel's Configuration Word A, B, or C to be transferred to the requesting CPU channel.

During the response cycle (second-half read), the HSDC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

Command Input Interrupt Control

Function Code 02

Format



Function

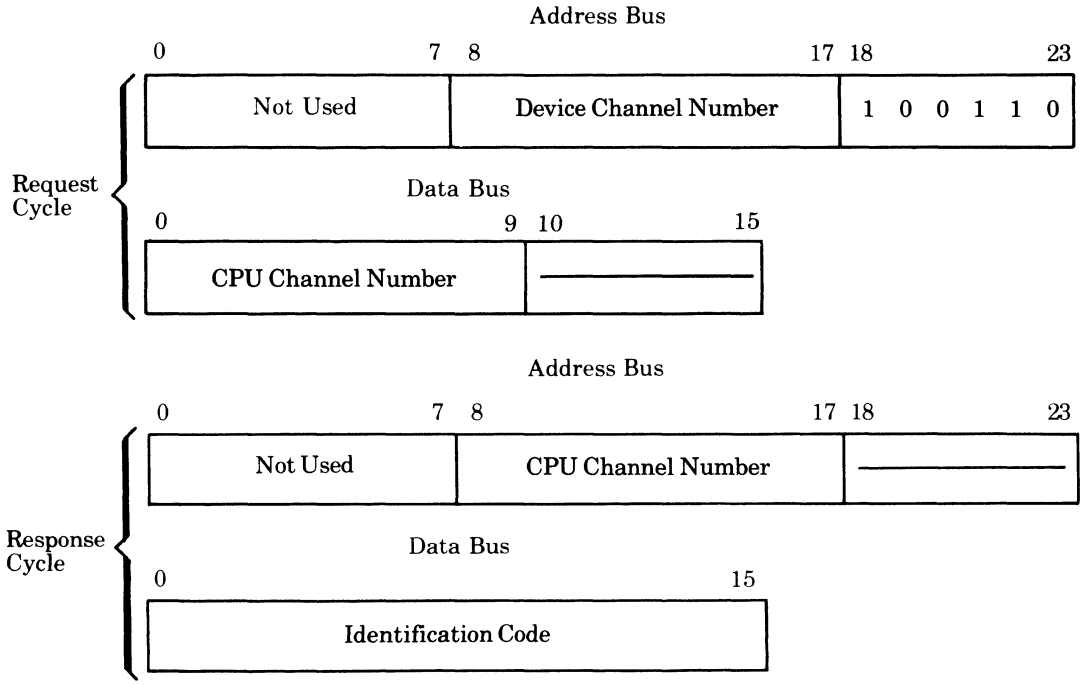
This instruction causes the channel's interrupt level to be transferred to the requesting channel. The level will be placed on data bus bits 10 through 15 (see above) with bit 15 as the least significant bit. This quantity is the value previously received in an Output Interrupt Control instruction, or a default value of 00. The default value is the interrupt level assumed by the channel when initialized. Note that the channel number returned in bits 0-9 of the data bus might be different from the channel number of the CPU executing this instruction if more than one CPU is attached to the megabus.

During the response cycle (second-half read), the HSDC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

Command Input Identification Code

Function Code 26

Format



Function

This instruction will cause the referenced channel to transfer its identification code to the requesting CPU channel. Depending on the unit accessed, one of the following codes will be returned:

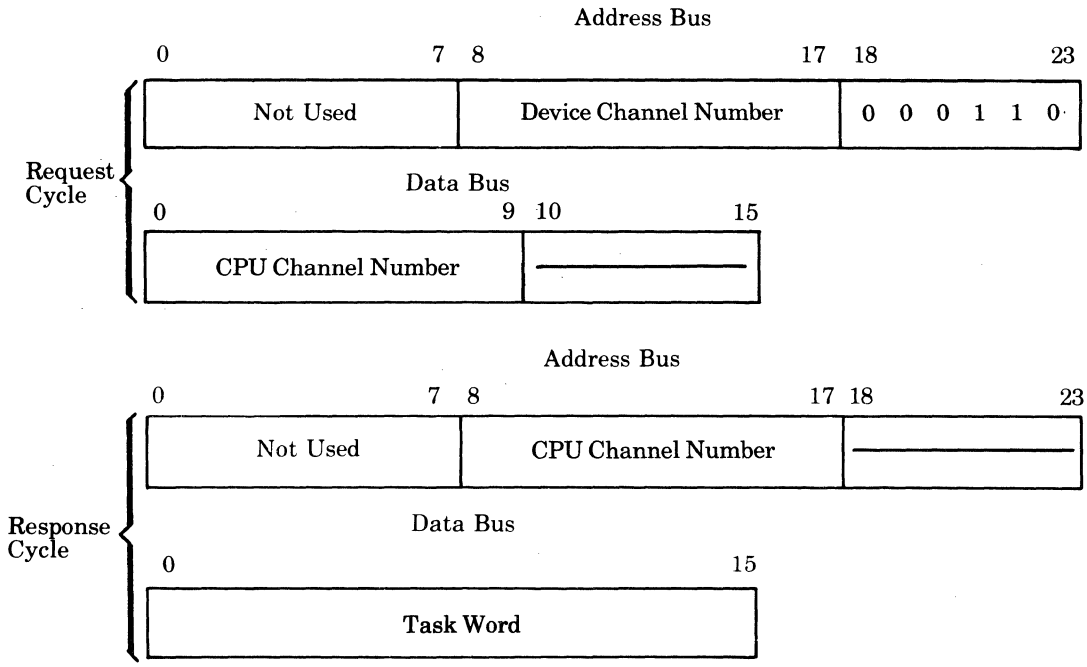
Code (Hex)	Model
2301	MSU9617/9618 Disk Unit
2303	RFU-MBZ
2305	MSU9619/9620 Disk Unit
3311	1/4-in. Cartridge Tape
331F	Tape not Accessible
2017	5 1/4-in. Diskette
201F	Diskette not Accessible
230F	This code represents the ID code received when a unit is physically attached, but is not accessible to the system because it was not powered up. The HSDC will generate the correct ID when the unit becomes available (i.e., when it is cycled up). This updated ID code is visible to software as the result of the execution of another Input Identification Code instruction.

During the response cycle (second-half read) the HSDC will return in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

Command Input Task Word

Function Code 06

Format



Function

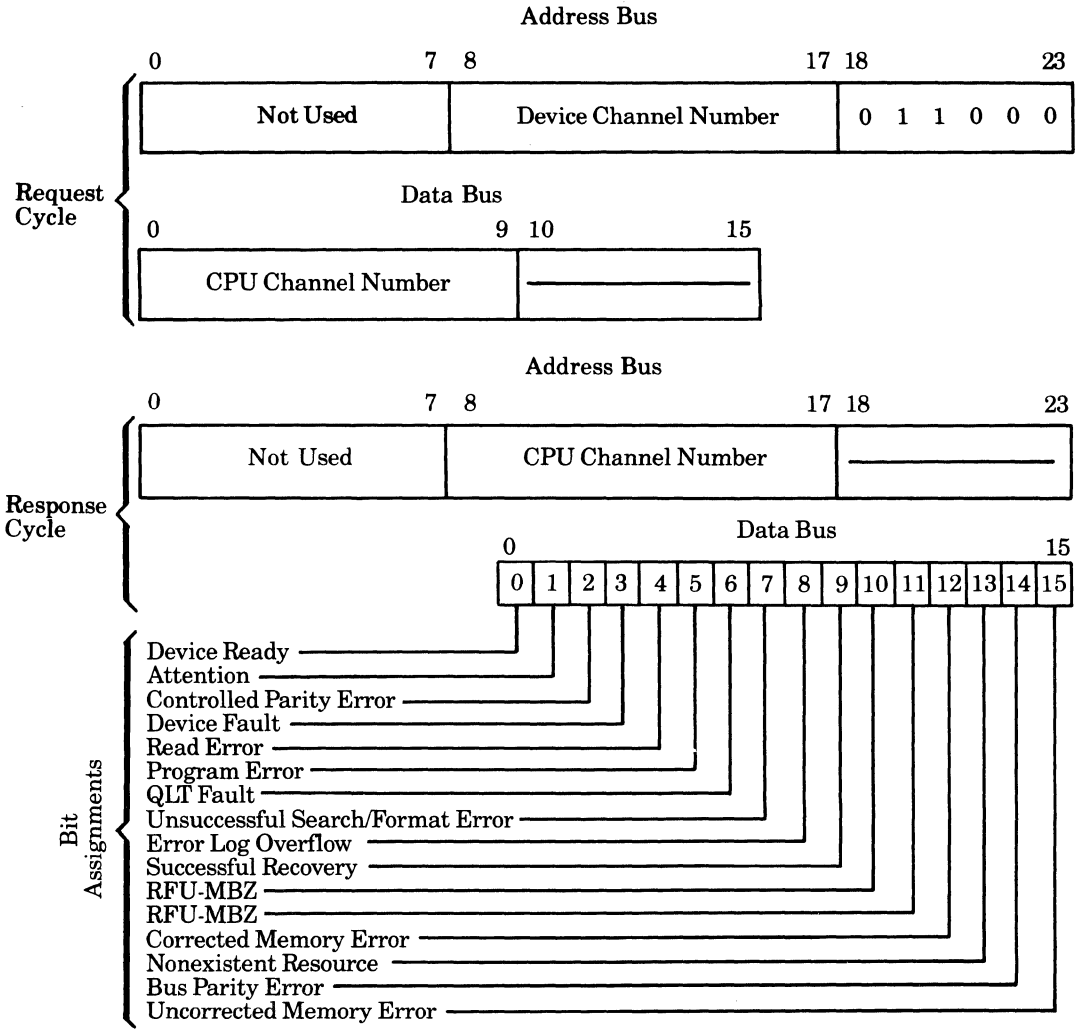
This instruction causes the Task Word of the referenced channel to be transferred to the requesting CPU channel. The Task Word transferred will contain the code for the last operation executed by the channel (unless an Initialize has occurred).

During the response cycle (second-half read) the HSDC will return in bits 8-23 the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle.

Command Input Status Word 1

Function Code 18

Format



Function

This instruction causes the referenced channel's Status Word 1 to be transferred to the requesting CPU channel.

During the response cycle (second-half read) the HSDC returns in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle. See Table A-2.

Table A-2. Status Bit Definitions – Input Status Word 1

Status Condition	Bit	Definition
Device Ready	0	The unit is online with the media loaded and no further manual intervention is required to place it under program control. Note that a change of state of this bit will cause the attention bit (bit 1) to be set resulting in an interrupt (if the interrupt level is nonzero). This bit reflects the current condition of the device.
Attention	1	Set whenever the device ready bit (bit 0 of the Status Word) changes state. Indicates to software any change of operational status of the device (e.g., load/unload of media). Whenever set, an interrupt is attempted (if the interrupt level is nonzero). If a previously initiated operation is in progress when a device state change is sensed, the resultant interrupt (with the attention bit set) serves as notification of both the end of the operation and the device state change. This bit is reset by an Initialize command, an Output Task Word command, an Input Status Word command or Master Clear on the Megabus.
Controller Parity Error	2	When transferring data through the controller, parity is verified and if found in error, this bit is set. This bit is reset by an Initialize command, an output Task Word command, an input Status Word Command or a Master Clear on the Megabus.
Device Fault	3	Set if the HSDC status bit zero is set indicating a device fault. Bits 8-15 of Status Word 2 reflect the specific fault. Operator intervention is required to reset the Write Protect condition of the unit. Note that this bit is reset if the condition causing it to set is removed by the unit.
Read Error	4	Set during any Read operation if either the EDAC word at the end of a field indicates that an uncorrectable data error has occurred within the field or the CRC Error bit appears within the ID field provided it is a new error not logged in the New Error Log on the highest number cylinder. This bit is also set when a mis-compare error is detected during the Read After Write and Compare command. This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.
Program Error	5	This bit is set if any of the available Megabus commands are executed erroneously, e.g.: • Seek to a nonexistent cylinder • Format Write range is not = 380 (or 252 bytes, dependent on the unit type) • Wraparound buffer range is incorrect • Attempt to select a non-existent head This bit is reset by an Initialize command, an Output Task Word command, or a Master Clear on the Megabus.

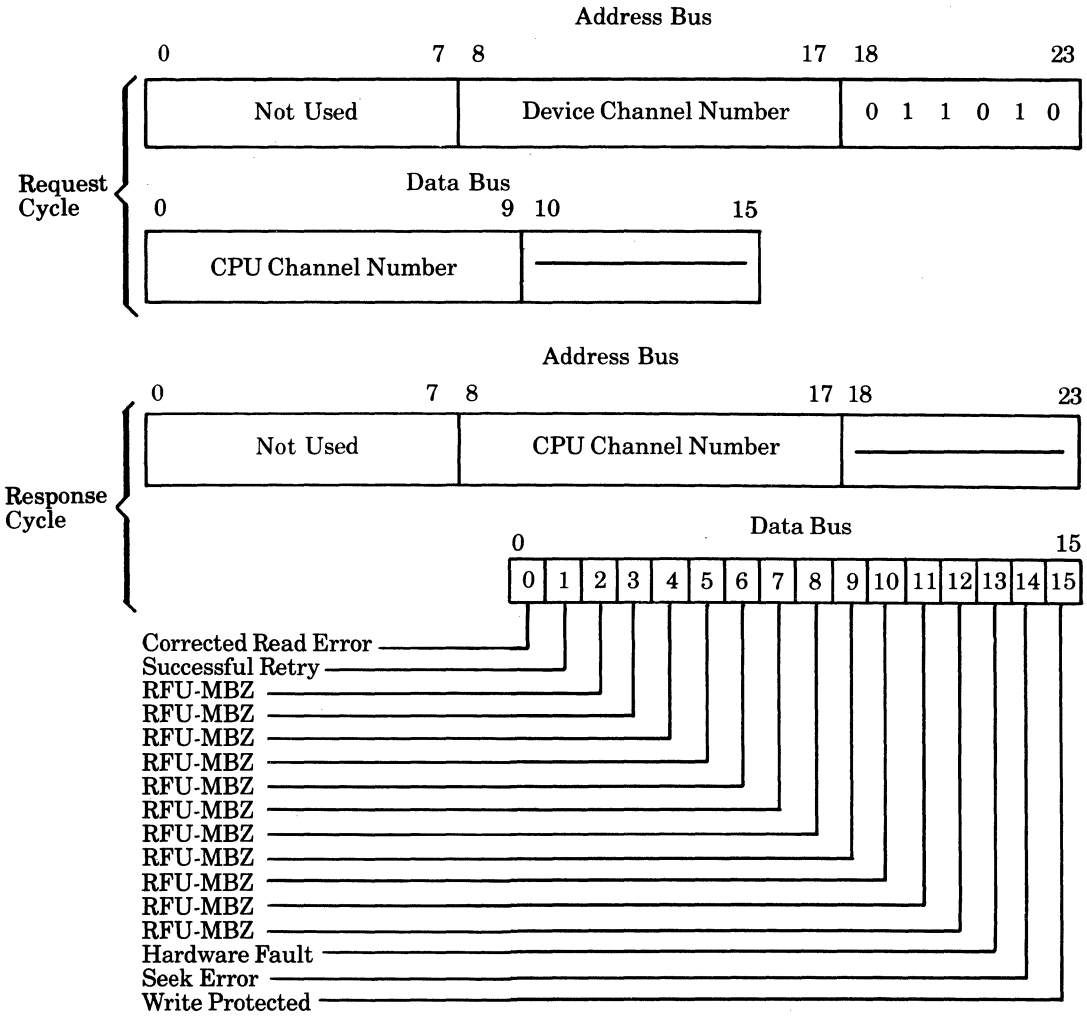
Table A-2 (Cont). Status Bit Definitions – Input Status Word 1

Status Condition	Bit	Definition
QLT Fault	6	This bit indicates that the controller or an adapter QLT has failed and that the QLT status buffer contains the fault identification. The Device Ready bit is also reset in Status Word 1. This bit is reset by an Initialize command or a Master Clear on the Megabus.
Unsuccessful Search/Format Error	7	Set during a nonformat Read or Write operation for which the sector ID specified in Configuration Words A and B cannot be located on the track or on the innermost cylinder. Also set if an Index Mark is detected during a Format Read/Write operation and in this case, memory address register is invalid.
Error Log Overflow	8	This bit is set whenever the HSDC detects that the New Error Log (on the innermost cylinder sectors 1 through 4) on the unit has exceeded 255 error sectors count. If reformatting does not reduce the error count, the media or the device needs further attention.
Successful Recovery	9	Set when an error condition was successfully recovered during the previous operation. Status Word 2 specifies the error condition which has occurred. This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.
Not Used	10	
Not Used	11	
Corrected Memory Error	12	Indicates that during execution of the previous disk write operation main memory detected and corrected a memory read error. Data delivered to the HSDC was assumed to be correct. This bit is reset by an Initialize command, Output Task Word Command, or Master Clear on the Megabus.
Nonexistent Resource	13	Set whenever the HSDC attempts a bus cycle (except interrupt) and receives a NAK response from memory. This bit is reset by an Initialize command, an Output Task Word command, an Input Status Word 1 command, or Master Clear on the Megabus.
Bus Parity Error	14	Set whenever the HSDC detects a parity error on either byte of the data bus during any bus cycle, or when a parity error is detected in bits 0-7 of the address bus. This bit is reset by an Input Status Word command or an Initialize (via Master Clear or an Output Control Word command).
Noncorrectable Memory Error	15	Indicates that during execution of the previous disk write operation, main memory detected a memory read error which the EDAC algorithm could not correct. Data delivered to the HSDC was incorrect. It will not cause termination of the operation in progress (may result in bad data written on the media). This bit is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.

Command Input Status Word 2

Function Code 1A

Format



Function

This instruction causes the referenced channel's Status Word 2 to be transferred to the requesting CPU channel.

During the response cycle (second-half read) the HSDC returns in bits 8-23 of the address bus, the same data that was received in bits 0-15 of the data bus during the request cycle. See Table A-3.

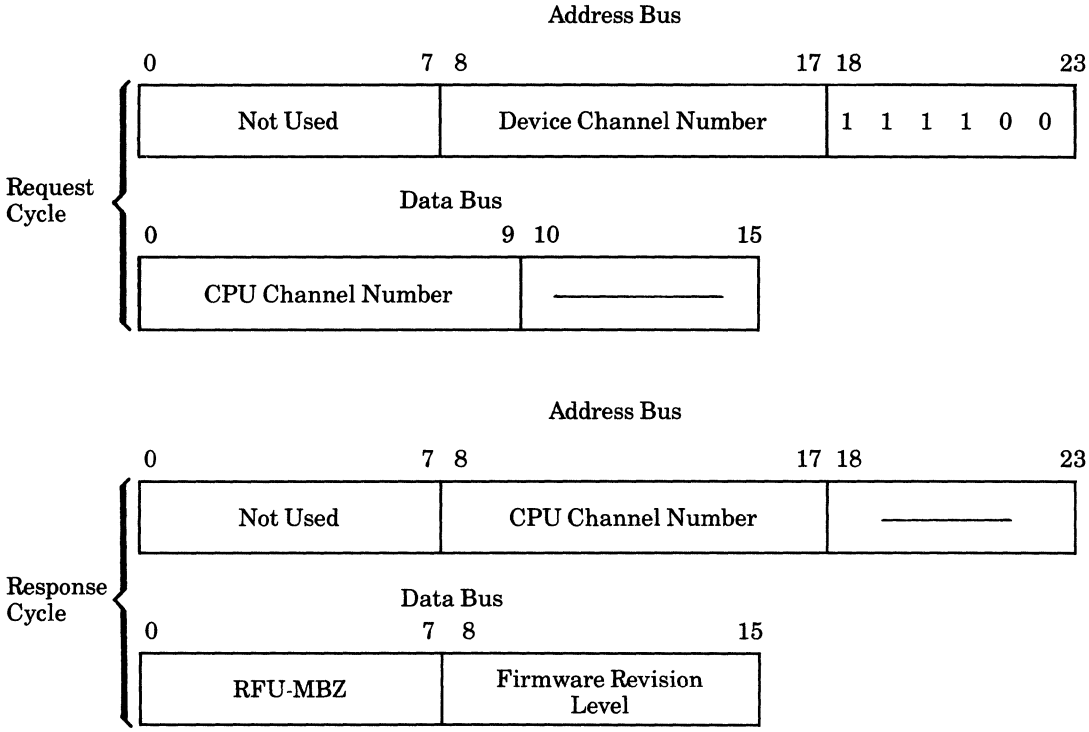
Table A-3. Status Bit Definitions – Input Status Word 2

Status Condition	Bit	Definition
Corrected Read Error	0	Set when a correctable read error occurred during the previous read operation. Correction was performed by the HSDC in buffer memory. When this bit is set, it also will cause bit 9 of Status Word 1 to be set. This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.
Successful Retry	1	Set when a data read error has been successfully retried during the previous operation. Data stored in main memory is correct. When this bit is set, it will also cause bit 9 of Status Word 1 to be set. This indicator is reset by an Initialize command, an Output Task Word command, or Master Clear on the Megabus.
RFU-MBZ	2-12	These bits are reserved for future use and must be zero.
Hardware Fault	13	A device fault has occurred when this bit is set.
Seek Error	14	Set when a seek error has occurred. This signal indicates that the unit was unable to complete a move or that the carriage has moved to a position outside the recording area, or that an address greater than the maximum number of tracks available has been selected. Read error is also set in Status Word 1, bit 4. The Return-to-Zero command is required to clear this error and return the heads to track zero with the On Cylinder and Seek End true.
Write Protected	15	When this bit is set it indicates that the unit is protected from being written on by a front panel switch which inhibits the writer circuit, illuminates the front panel indicator and sets the Write Protect signal true. Attempting to write while in this state results in the set Fault signal from the device. This condition can be reset by depressing the front panel Write Protect switch again which extinguishes the indicator.

Command Input Firmware Revision

Function Code 3C

Format



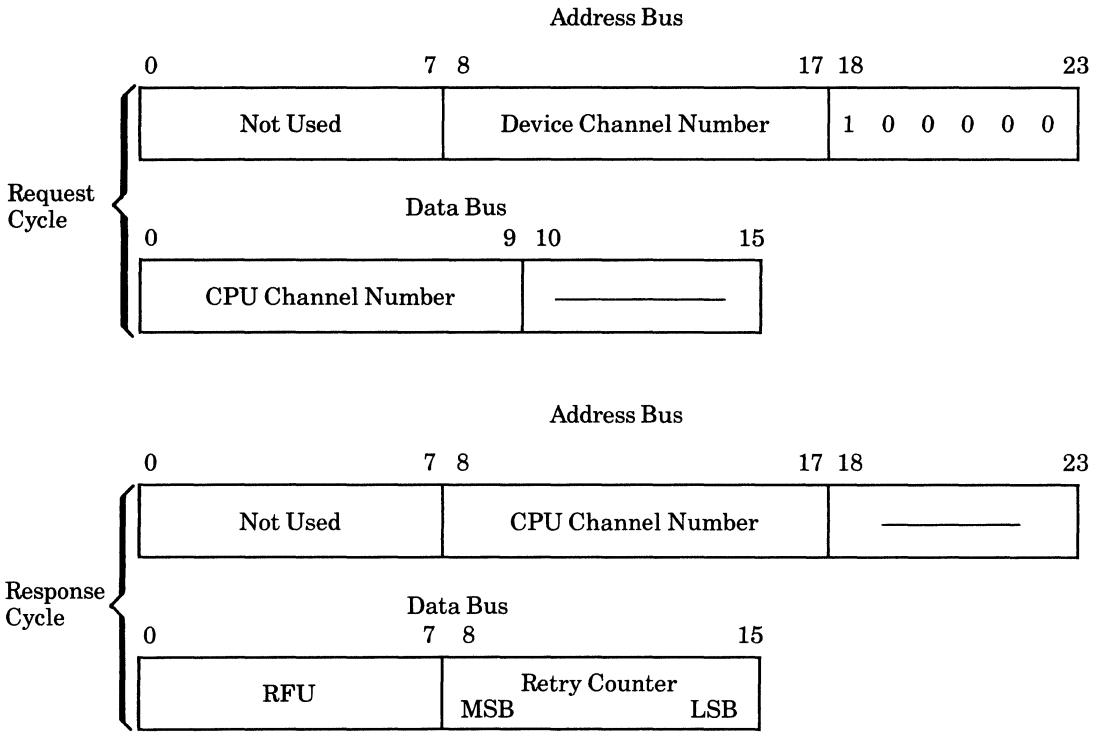
Function

The firmware revision level is represented by a hex number (i.e., 23) which is the sequential control number.

Command Input Retry Counter

Function Code 20

Format



Function

This instruction causes the referenced channel's Retry Counter to be transferred to the requesting CPU channel.

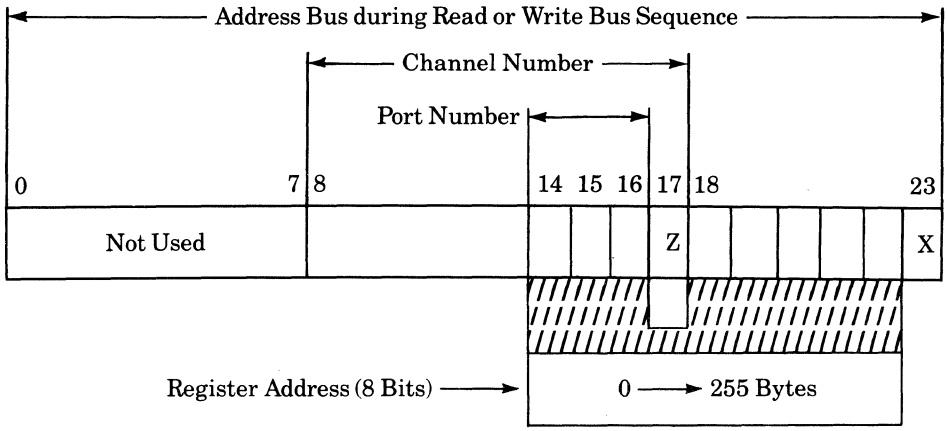
The Retry Counter contains the count of the number of time Read Error Retries were performed. This count is provided for error logging purposes.

The Retry Counter is reset by an Output Task Word, Initialize, or a Master Clear on the Megabus.

Command Read/Write HSDC Registers

Function Code Any Even Code – Read
Any Odd Code – Write

Format



Function

The HSDC maintains 32 registers (16 bits per register) for each channel. The address of each of the various registers in the HSDC is a combination of two bits of the Channel Number and the five high-order bits of the Function Code used to write into or read from a particular register (see above). For example, Configuration Word A for HSDC channel 2 is HSDC register 48 (hex):

- Function code for Configuration Word A = 01000X (X = read/write bit)
- Channel Number = 010Z (Z = direction bit)
- Register Number = 0100, 1000 = 48 (hex)

Complete software visibility to the HSDC registers is provided for diagnostic purposes. An output bus sequence addressed to one of the devices causes the information on the data bus (16 bits) to be loaded into the device-specific register specified by the device port number and the five high-order bits of the function code.

The Output Address command is a special case. When an Output Address command is executed (on port 0, for example), the HSDC register 04 (hex) is loaded with the 16 low-order bits of the address. The eight high-order bits of the HSDC register 04 (hex) is loaded with the 16 low-order bits of the address. The eight high-order bits of the HSDC register 05 are loaded with the eight high-order bits of the address.

Any input bus sequence addressed to a device causes the register specified by the port number and the five high-order bits of the Function Code to be returned via the data bus (during the second-half read cycle). A detailed register map for each device type is available in the HSDC manual.

Appendix B
Specifications

MSU9617/9618 Performance Characteristics

Data Capacity:
Storage capacity (formatted) — 132M bytes
Fixed-discs/unit — 6
Disc diameter — 9 in.
Cylinders/unit — 821
Tracks/cylinder — 10
Sectors/track — 63
Bytes/sector — 256

Average Latency: 8.3 ms

Average Access Time: 38.3 ms

Seek Time:
Minimum — 7 ms
Average — 30 ms
Maximum — 55 ms

Transfer Rate: 1.2M bytes/second

Spindle Speed: 3600 rpm

MSU9619/9620 Performance Characteristics

Data Capacity:
Storage Capacity (formatted) — 413M bytes
Fixed-discs/unit — 7
Disc diameter — 9 in.
Cylinders/unit — 709
Tracks/cylinder — 24
Sectors/track — 96
Bytes/sector — 256

Average Latency: 8.3 ms

Average Access Time: 28.3 ms

Seek Time:
Minimum — 5 ms
Average — 20 ms
Maximum — 40 ms

Transfer Rate: 1.82M bytes/second

Spindle Speed: 3600 rpm

Physical Characteristics (MSU9617 and MSU9619)

Cabinet Height: 30.0 in. (75.0 cm)

Cabinet Width: 20.5 in. (52.0 cm)

Cabinet Depth: 33.0 in. (84.0 cm)

Weight:
MSU9617 (cabinet and one drive) — 214 lb (96.3 kg)
MSU9619 (cabinet and one drive) — 230 lb (104.3 kg)
MSU9618 (drive only) — 66 lb (30 kg)
MSU9620 (drive only) — 82 lb (38 kg)

Electrical Characteristics

Frequency: 60 Hz, ±0.6 Hz

Voltage: 120 Vac, +10%, −15%; single phase

Power Consumption:
MSU9617/9618 — .36 kVA
MSU9619/9620 — .40 kVA

Heat Generation:
MSU9617/9618 — 832 Btu/hr
MSU9619/9620 — 886 Btu/hr

Environmental Characteristics

Operating Temperature: 50°F to 100.4°F (10°C to 38°C)

Relative Humidity: 20% to 80% (noncondensing)

Cables

Power cord: 6.0 ft (1.83 m)

Disk controller cabinet to first cabinet: 25.0 ft (7.62 m) maximum

Cabinet to cabinet: 10.0 ft (3.0 m)

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[1]Fixed-disk units require a high capacity removable media device for software loading (i.e., ¼-in. Cartridge Tape, GCR/PE tape, NRZI/PE tape, Cartridge Module or Mass Storage Disk Unit).

[2]An update to the central processor firmware may be required when adding a fixed-disk unit to an installed DPS 6 or Level 6 system as the systems disc (the disc containing booting procedures for the operating system). Consult your Honeywell Representative for details.

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