Honeywell

SERIES 60 LEVEL 6

TYPE DCM9103 DUAL SYNCHRONOUS COMMUNICATIONS LINE ADAPTER MANUAL

Doc. No. 71010231-200 Order No. FL49, Rev. 1

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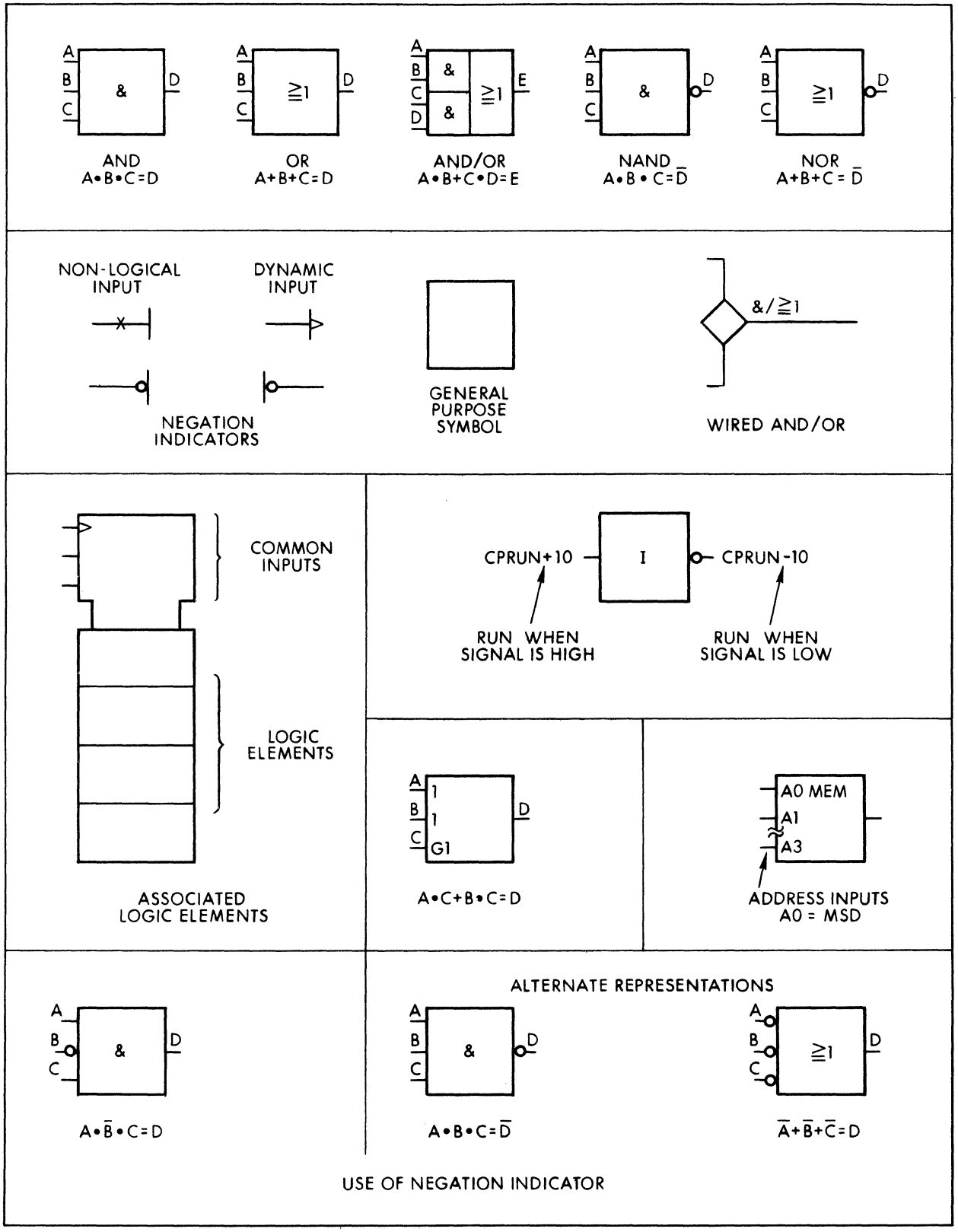

1 INTRODUCTION

1.1 GENERAL DESCRIPTION

The Type DCM9103 Dual Synchronous Communications Line Adapter is one of a series of solid-state Communications-Pacs used with the Multiline Communications Processor (MLCP) of the Honeywell Series 60 Level 6 computer. As shown in Figure 1-1, up to four compatible line adapters can be used with an MLCP, and from one to four of these adapters can be a dual SCLA. Each dual SCLA can support two full-duplex lines, and each direction (receive and transmit) of a line is a separate channel into the MLCP. (Note that in this manual, SCLA refers to a dual Synchronous Communications Line Adapter.)

An SCLA contains the logic for data handling, control and interface between the MLCP and Data Communications Equipment (DCE). Essentially, the SCLA contains a group of line registers which the MLCP continually sets to effect required operational functions. Note that all formatted control procedures used in communicating with the DCE are performed in the MLCP.

The SCLA can be used with, but is not restricted to, the following DCE:

- Dataphone Data Set 201 or equivalent, or direct connect
- Dataphone Data Set 203 or equivalent, or direct connect
- Dataphone Data Set 208 or equivalent, or direct connect.

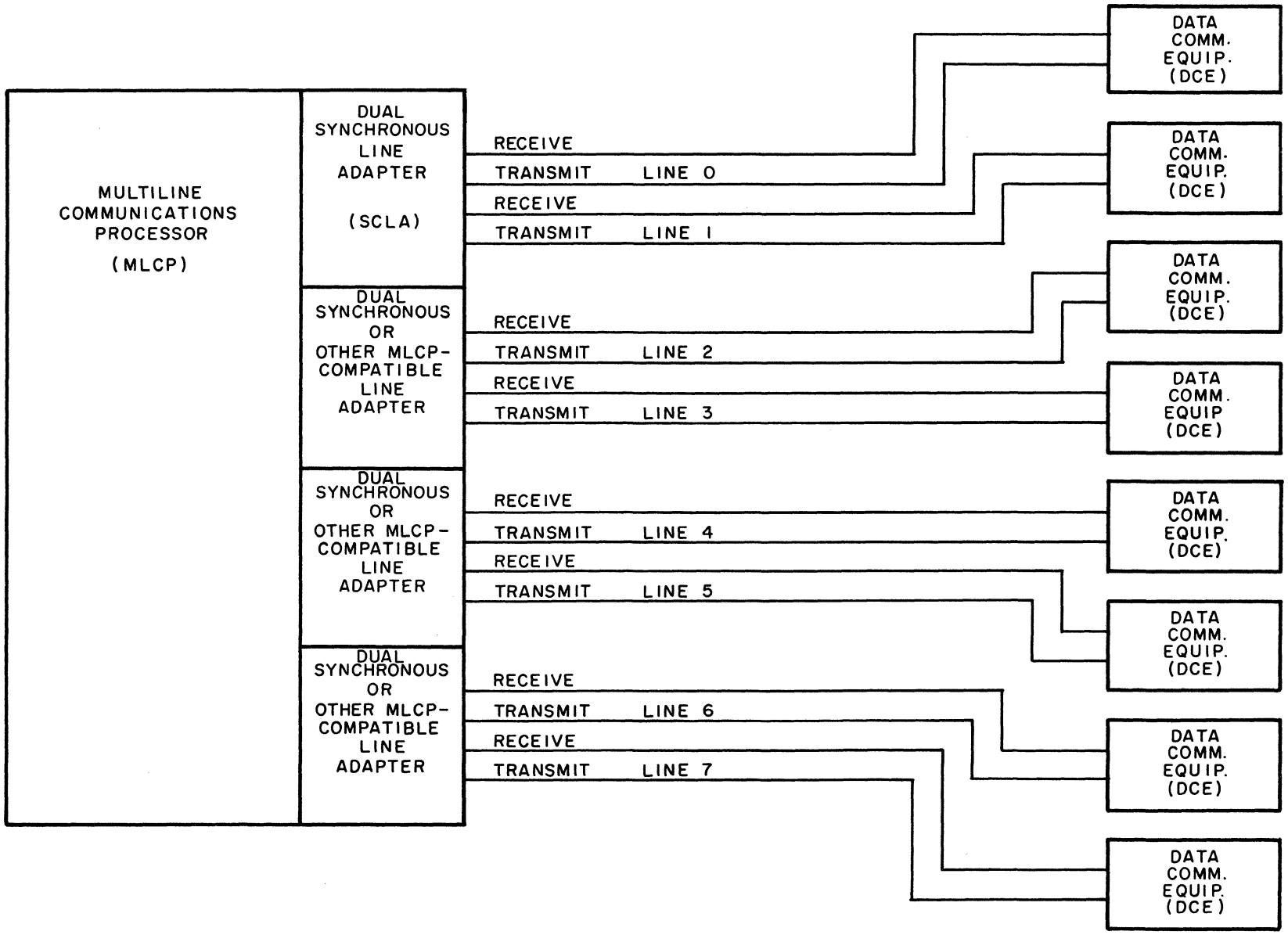

Figure 1-1 Configuration Diagram, Dual Synchronous Communications Line Adapter

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1.2 INTERFACE

The data interface between the SCLA and the DCE is full-duplex for each line. All input and output data information is in a serial stream consisting of communication-type characters. Either 5-, 6-, 7-, or 8-bit characters are used, depending upon software instructions.

In addition to the data interface between the SCLA and the DCE, there are also ten control line interconnections between the SCLA and DCE for each line. See Table 2-2 for an explanation of the use of these lines.

All transmission between the SCLA and the DCE is at a level specified by Specification RS232C of the Electronic Industries Association (EIA). To conform with this specification, 0V and 5V signals generated in the SCLA are changed to +12V and -12V respectively if they are transmitted to the DCE. Conversely, +3 to +25V and -3 to -25V levels generated in the DCE are changed to 0V and 5V respectively when they are received in the SCLA.

The interface between the SCLA and MLCP is half duplex. All input data, output data, and control signals are carried on lines which use connectors on the bottom of the SCLA to connect to the MLCP. All data is transferred in parallel (byte form) between the SCLA and MLCP.

The transmission rate between the SCLA and the DCE is determined by either the transmit clock or receive clock signal generated in the DCE and sent into the SCLA.

1.3 PHYSICAL CHARACTERISTICS

The SCLA (BD2LAS) can be attached to any Communications-Pac position on the MLCP (BF4MLC). The physical dimensions of the MLCP and the Communications-Pacs are shown in Figure 1-2.

The BD2LAS board has two 25-pin connectors (Z01 and Z02) which are used for the physical and electrical connection of the Communications-Pac to the MLCP. A 28-pin connector, Y01, is used to connect the DCE cable to the BD2LAS board.

For information pertaining to cabling, refer to Appendix B.

1.4 OPTIONS

The Synchronous Communications Line Adapter (SCLA) can be used in a direct connect application. This application allows the MLCP to interface with another computer without the use of Data Communications Equipment (DCE). Details on the direct connect option are covered in subsection 2.2.9.

1.5 REFERENCE DOCUMENTS

The following documents supplement the information contained in this manual.

Title	Document No.	Order No.
Model 34/36 Systems Manual	71010200-200	FL35
Type MLC9103 Multiline Communications Processor Manual	71010230-200	FL48
Type DCM9103 Communications Line Adapter Reference Manual	71010381-200	FL52
Level 6 Minicomputer Handbook	--	AS22
MLCP Programmer's Reference Manual	--	AT97
Level 6 System Checkout and Operator's Guide	--	AW94

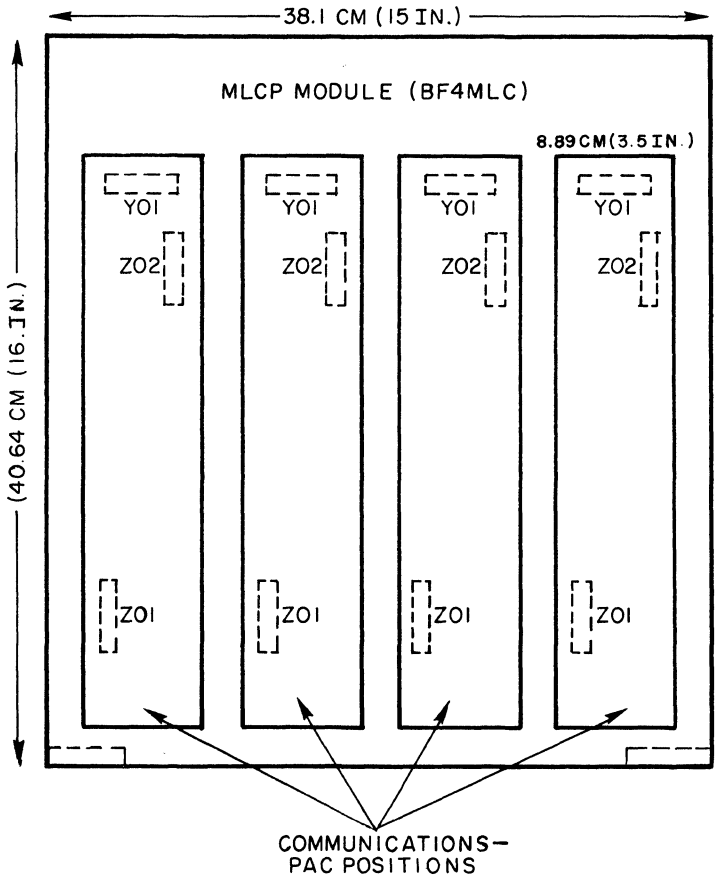

Figure 1-2 Dual SCLA Layout and Dimensions

II THEORY OF OPERATION

2.1 BLOCK DIAGRAM DESCRIPTION

The Synchronous Communications Line Adapter (SCLA) provides the Multiline Communications Processor (MLCP) with two independent interfaces with standard synchronous communications lines. Figure 2-1 is a block diagram of the logic used in interface A (between the MLCP and line 0). Interface B (between the MLCP and line 1), which has similar logic, is not shown. Note, however, that the line adapter control block and the test multiplexer shown in Figure 2-1 are common to interface A and interface B.

The basic function of the SCLA is to control the data flow between the MLCP and the lines. Data bytes received in parallel from the MLCP are transformed into standard communication-type characters and transferred to the lines in a serial stream. Communication-type characters received from the lines in a serial stream are converted to data bytes and sent to the MLCP in parallel-byte form. A secondary function of the SCLA is to interchange control information between the MLCP and the DCE.

All interconnections between the adapter and the MLCP are via hardware connectors on the bottom of the SCLA. There are four control lines and three address lines between the MLCP and the SCLA. The line adapter control logic uses these lines to generate signals for control of the SCLA hardware. (See subsection 2.2.3 for details on the decoding of the control and address lines and the use of the generated control signals.) The eight data input lines are used to transfer either data bytes from the receiver or an input byte from the input status multiplexer into the MLCP. The data output lines are used to transfer;

1. Configuration bytes to the transmitter/receiver (XMTR/RCVR) configuration register.
2. Sync configuration bytes to the receiver.
3. Sync configuration bytes to the transmitter.
4. Configuration information to the data set control register.
5. Data bytes to the transmitter.

Prior to receiving data from the line, the MLCP channel program loads three SCLA registers. First, the XMTR/RCVR configuration register is loaded to handle 5-, 6-, 7-, or 8-bit characters. Next, a sync character is loaded into the XMTR/RCVR sync character register. Finally, the MLCP loads the data set control register to control the operation of the SCLA lines. Note that parity checking of received characters is not accomplished in the SCLA. Then the sync character is used to make a bit-by-bit comparison of the data stream received from the DCE. When a sync character is detected in the incoming stream, the receiver changes from the bit-by-bit mode into a byte mode of operation and notifies the MLCP via the ready flip-flop. In the byte mode, the sync character and all the following characters in the input message are transferred to the MLCP from the DCE. (See subsection 2.2.6 for more details on an input operation.) If the receiver has two characters ready for transfer to the MLCP before one is taken, the receiver generates an overrun error signal.

Prior to transmitting data to the line, the MLCP channel program loads three SCLA registers. First, the XMTR/RCVR configuration register is loaded to handle 5-, 6-, 7-, or 8-bit characters. Next, a transmit fill character is loaded into the XMTR/RCVR transmit fill character register. Finally the MLCP loads the data set control register to control the operation of the SCLA lines. Note that no parity bit generation is accomplished by the transmitter. The configured transmit fill character is sent out to the line during an output operation whenever the MLCP fails to maintain required data output rate. The transmitter also generates an underrun error signal when this condition develops. (See subsection 2.2.5 for more details on a transmit operation.)

The input status multiplexer inputs SCLA error and line status information into the MLCP from either interface A or interface B as selected. (See subsection 2.2.7 for specific information carried by the input signals.)

The test multiplexer provides a wraparound mode for use by diagnostic software. This wraparound mode allows the serial data stream out of the transmitter to be sent directly back to the MLCP via the receiver in data-byte form. The test multiplexer also shifts the source of the clock signal to the MLCP when the wraparound mode is being used. The diagnostic software checks the operation of the SCLA in the wraparound mode by comparing transmitted to received characters. (See subsection 2.2.8 and Appendix A for further details.)

The data set control logic consists of an 8-bit register which stores control information from the MLCP. This information is then used by the SCLA for controlling the interface with its associated DCE. (See subsection 2.2.4 for details on the use of the stored information.)

The EIA interface logic enables the SCLA to use transmitters and receivers designed to specification RS-232C of the Electronic Industries Association (EIA). This interface changes the level of the signals out of the SCLA from the TTL 0V and +5V to +12V and -12V respectively for use by the DCE. Conversely, the EIA interface logic changes signals received at +3 to +25V and -3 to -25V levels from the DCE to 0V and +5V respectively for use by the SCLA. (See Figure 2-7.)

The ready flip-flops which are used in a receive or transmit operation are discussed in detail in subsections 2.2.5 and 2.2.6.

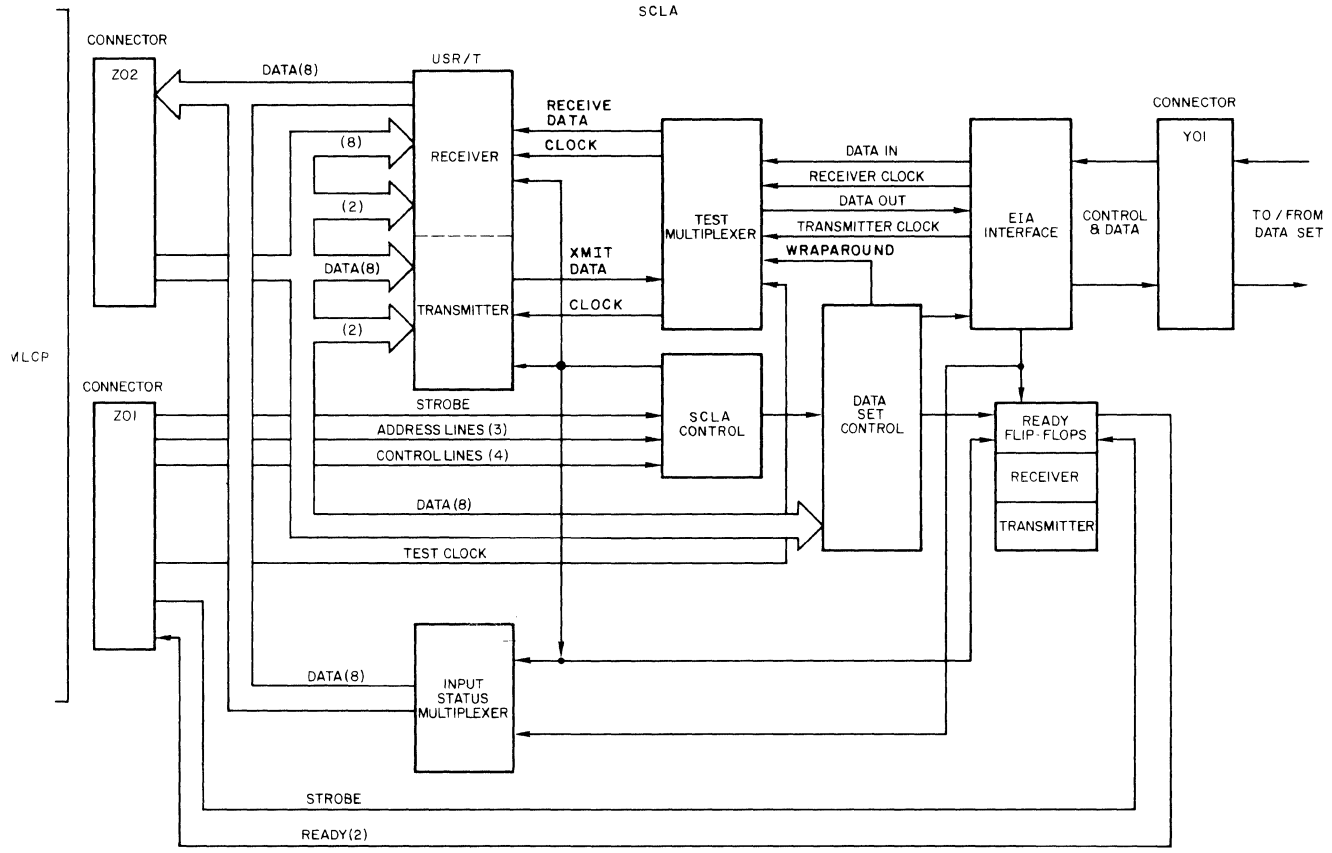

Figure 2-1 Dual Synchronous Communications Line Adapter (SCLA), Block Diagram

2.2 FUNDAMENTAL HARDWARE DESCRIPTION

2.2.1 Interconnections

Figure 2-2 shows the interconnections between the Multiline Communications Processor (MLCP) and the SCLA. Table 2-1 describes the function of the signals carried by these interconnections.

Figure 2-3 shows the interconnections between the SCLA and the lines. Table 2-2 describes the function of the signals carried by these interconnections.

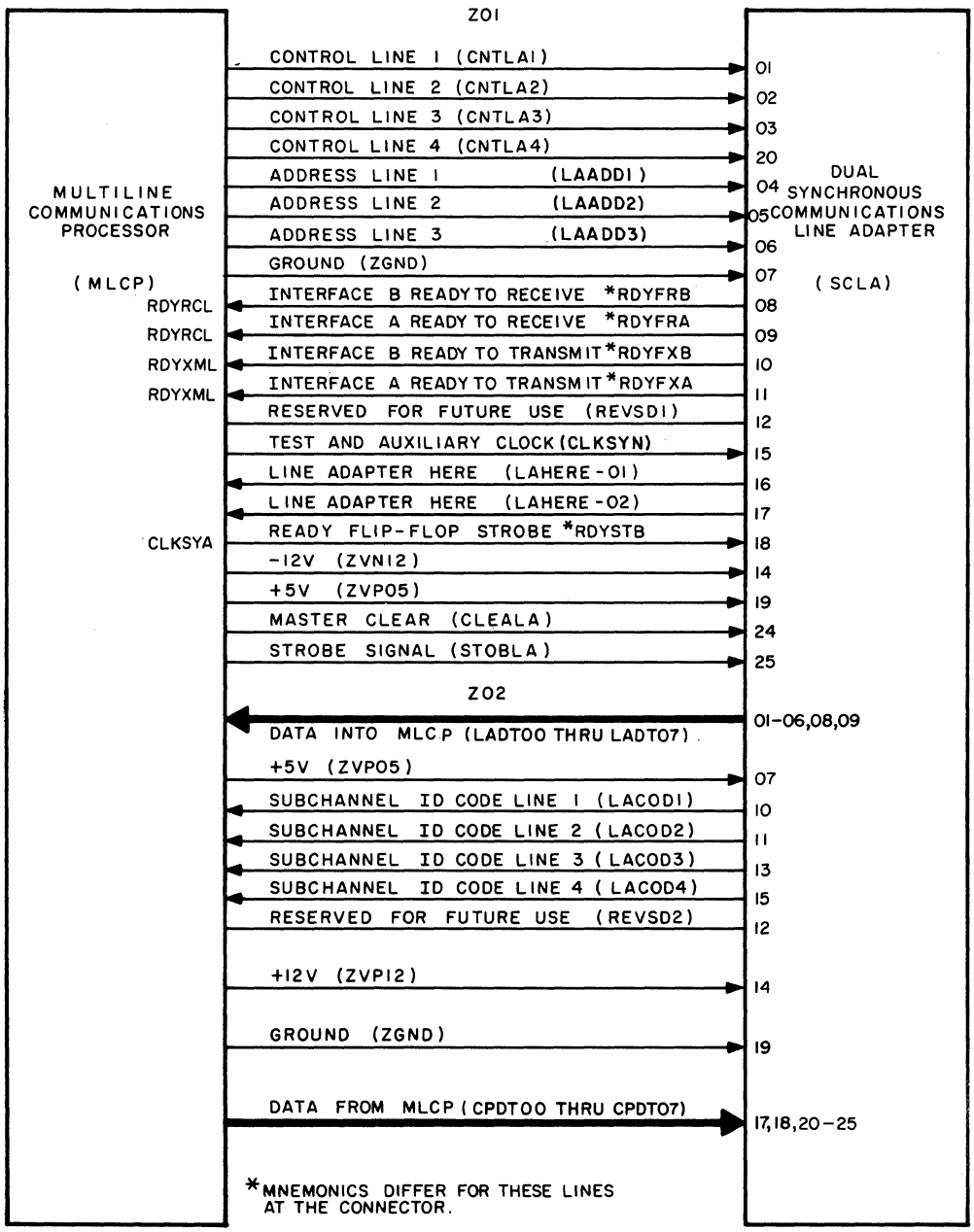

Figure 2-2 Interconnections Between MLCP and Dual SCLA

Table 2-1 Interconnections-SCLA To/From MLCP

MNEMONIC	NAME OF LINE	FUNCTION
CLEALA	Master Clear	Clears hardware in the SCLA when ordered by the MLCP.
CLKSYN	Test and Auxiliary Clock	Clock signal from MLCP used in the test mode and direct connect mode.
CNTLA1 thru CNTLA4	Control	Selects functions to be performed by SCLA hardware.
CPDT00 thru CPDT07	Data Output Byte	Data output byte from the MLCP. Used to transfer both data and control information.
LAADD1 thru LAADD3	Address	Selects line and channel to be serviced.
LACOD1 thru LACOD4	Subchannel ID Code	Lines by which the MLCP identifies the specific type of SCLA attached to it.
LADT00 thru LADT07	Input Byte	Data input byte into the MLCP. Depending upon the operating condition of the SCLA, this byte can be either data or status from either interface A or interface B.
LAHERE-01 LAHERE-02	SCLA Here	Notifies the MLCP that a SCLA is installed.
RDYFRA	Interface A Ready to Receive	Indicates that interface A is ready to transfer a data character into the MLCP.
RDYFRB	Interface B Ready to Receive	Indicates that interface B is ready to transfer a data character into the MLCP.
RDYFXA	Interface A Ready to Transmit	Indicates that interface A is ready to receive a new data character from the MLCP for transmission to the line.
RDYFXB	Interface B Ready to Transmit	Indicates that interface B is ready to receive a new character from the MLCP for transmission to the line.
RDYSTB	Ready Flip-Flop Strobe	Used to synchronize the ready flip-flops in interface A and B (of the SCLA) with the MLCP.
STOBLA	Strobe Signal	Strobe from the MLCP to the SCLA for generating various control signals. Indicates that data from MLCP is valid.
REVSD1 REVSD2	Reserved	Reserved for future use.
ZGND	Ground	Ground
ZVP05	+5V	+5V
ZVN12	-12V	-12V
ZVP12	+12V	+12V

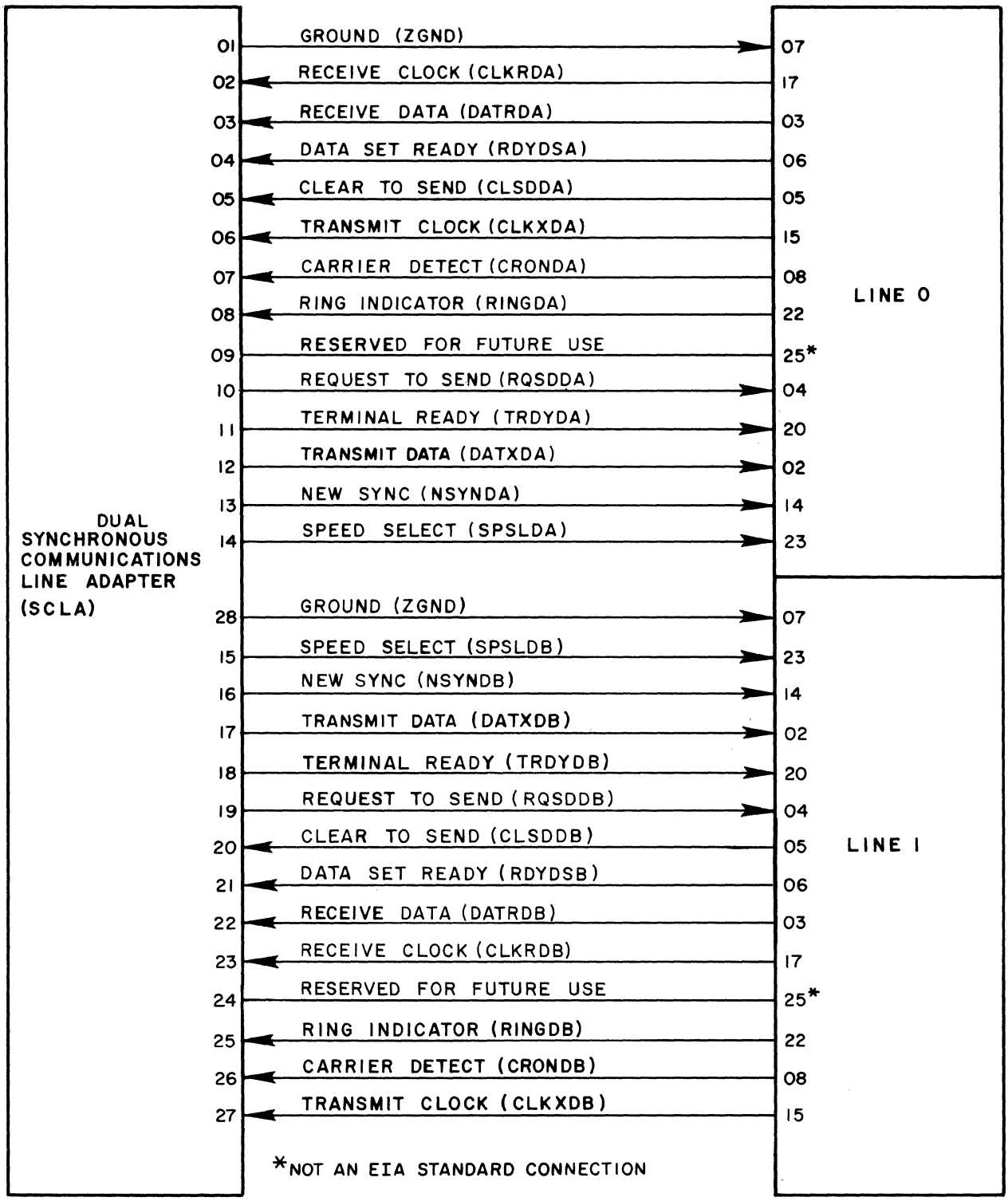

Figure 2-3 Interconnections Between Dual SCLA and Lines

Table 2-2 Interconnections-SCLA To/From Lines

MNEMONIC	NAME	FUNCTION
NOTE The signals listed are for line 0. Line 1 has an identical set of signals, but the last letter of the mnemonic is B instead of A.		
CLKRDA	Receive Clock	Clock signal from the DCE to the SCLA while it is receiving data from the DCE.
CLKXDA	Transmit Clock	Clock signal from the DCE to the SCLA when it is transmitting data to the DCE.
CLSDDA	Clear to Send	A response by the DCE to a Request to Send signal from the SCLA.
CRONDA	Carrier Detect	Indicates to the SCLA that the basic carrier frequency of the communication is present.
DATRDA	Receive Data	The serial data line from the DCE to the SCLA.
DATXDA	Transmit Data	The serial data line from the SCLA to the DCE.
NSYNDA	New Sync (Clock)	A request from the SCLA to the DCE for a new sync signal. In a Direct Connect application this signal is used as a clock for the receiver. See subsection 2.2.9.
RDYDSA	Data Set Ready	A signal from the DCE to the SCLA indicating it is ready to operate.
RINGDA	Ring Indicator	Indicates that the line is in the ringing condition and is trying to get the attention of the SCLA.
RQSDDA	Request to Send	A request to transmit from the SCLA to the DCE.
SPSLDA	Speed Select (Clock)	A signal from the SCLA to the DCE modem to select a specified rate of transfer. In a Direct Connect application this signal is used as a clock for the transmitter. See subsection 2.2.9.
TRDYDA	Terminal Ready	A signal from the SCLA to the DCE indicating that the SCLA is ready for operation.
ZGND	Ground	Ground.

2.2.2 Subchannel Identification Code Lines

The subchannel identification code lines (see Figure 2-2) are used by the MLCP to identify the type of SCLA attached. The MLCP then uses this information to form a software identification word. The specific word assigned to the SCLA is hexadecimal 2158.

The SCLA utilizes interface lines LACOD1 through LACOD4 to input its portion of the subchannel identification code to the MLCP. Table 2-3 identifies the MLCP data bus bit positions to which the SCLA ID code is eventually transferred, the binary and hexadecimal configuration of the subchannel ID code, and the voltage levels to which the LACODx lines are hardwired in the SCLA to produce its portion of the ID (i.e., xx58). The 21xx is generated in the MLCP, and the entire ID word (2158) is transferred to the Megabus* network when requested by software.

Table 2-3 SCLA ID Code Generation

MLCP Data Bus	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SCLA ID (LACOD1-4)										1	2	3	4			
ID Word (Binary)	0	0	1	0	0	0	0	1	0	1	0	1	1	0	0	0
ID Word (Hex)			2				1				5				8	
LACOD1-4 Hardwired Connections In SCLA										+5V	GND	+5V	+5V			

2.2.3 SCLA Control

As shown in Figure 2-4, the SCLA control logic consists of five 2-line to 4-line decoders and numerous gates and inverters. The function of this logic is to develop control signals for performing operations in the hardware of the SCLA. All of these control signals are developed from the three address lines, four control lines, and the strobe signal sent out by the MLCP.

Table 2-4 is a quick reference table showing the general decoding of the address and control lines from the MLCP. Table 2-5 lists the specific use of the address and control information received from the MLCP in developing SCLA control signals.

*Trademark of Honeywell Information Systems Inc.

The programming interface to the SCLA is achieved through line registers located in the SCLA. These registers are illustrated in Figure 2-5.

Each communications line is serviced by a different set of line registers. Each channel (transmit or receive) of a line has a dedicated set of registers and also shares three registers with the other channel of the same line.

As shown in Figure 2-5, line registers 0, 3, and 7 are not used. Line registers 1, 4, and 6 are located in the Universal Synchronous Transmitter/Receiver (Figures 2-8 and 2-9) and are accessed through the specified input gates. Line register 2 contains data set control information and is shown in Figure 2-6. Line register 5 is the status register and is shown in Figure 2-10.

For a detailed description of the line register contents, refer to the MLCP Programmer's Reference Manual (Order Number AT97).

2.2.4 Data Set Control

As shown in Figure 2-6 the data set control logic primarily consists of the data set control register, which is comprised of eight D-type flip-flops. The flip-flops are loaded by the data set strobe with information conveyed by the data information lines from the MLCP. Figure 2-6 shows the destination and the general usage of the output of each flip-flop. The NSYNDA and SPSLDA outputs have different functions in a normal line interface than in a direct connect interface, which is discussed in subsection 2.2.9. The function of the output signal from each flip-flop is as follows.

1. TRDYDA - SCLA ready to the DCE. This is commonly called Terminal Ready in communications systems.
2. RQSDDA - Request to send from the SCLA to the DCE.
3. NSYNDA - When used with a line connector, this signal from the SCLA to the DCE requests a new sync signal from the DCE. When used in a direct connect application, this signal is used for the receiver clock. (See subsection 2.2.9.)
4. SPSLDA - Sends a signal from the SCLA to the modem to select a specified rate of transfer. In a direct connect application, this signal is used for the transmitter clock. (See subsection 2.2.9.)
5. DIRCNA - This signal is used to set the direct connect operational mode (See subsection 2.2.9.)
6. TESMDA - Set test mode in the SCLA. (See subsection 2.2.8 for details.) Although interface B does not generate this signal, interface B is placed in the test mode by the hardware of interface A.
7. RECONA - Enables the receiver in the SCLA. (See subsection 2.2.6 for details on use.)
8. XMTONA - Enables the transmitter in the SCLA. (See subsection 2.2.5 for details on use.)

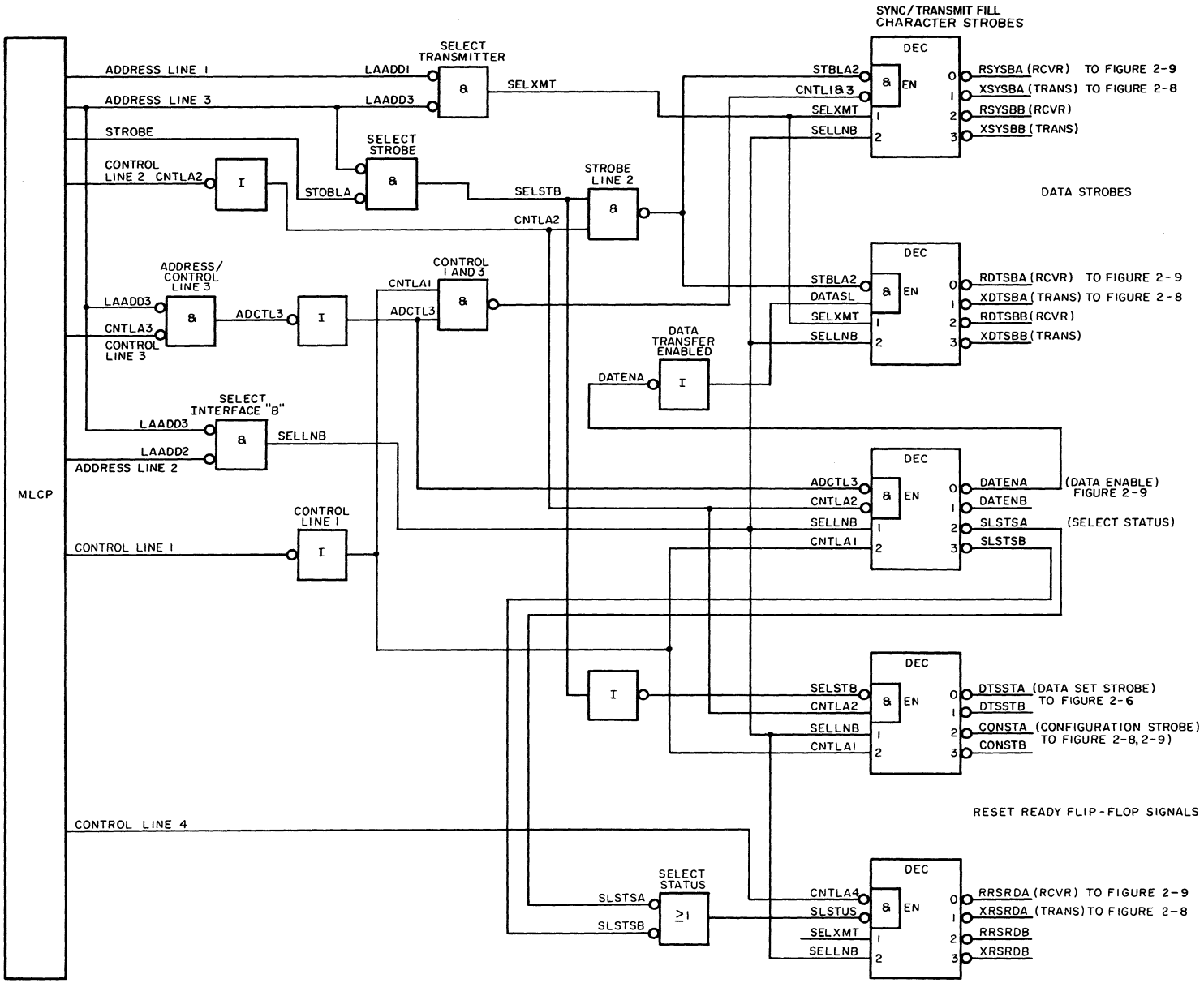

Figure 2-4 Dual SCLA Control, Address and Control Line Decoding

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Table 2-4 Address and Control Lines - General Decoding

ADDRESS LINE			GENERAL FUNCTION AND COMMENT
1	2	3	
1	0	1	Select transmitter
0	0	1	Select receiver
X	1	1	Select interface B
X	0	1	Select interface A
X	X	1	Indicates to the SCLA that is has been selected by the MLCP. The MLCP can control up to four SCLAs but enables only the SCLA with address line 3 set.
X	X	0	Indicates to the SCLA that it has not been selected by the MLCP. Address line decoding is not performed by the SCLA when address line 3 is reset.

NOTE

X = Decoding logic not affected by status of this bit when determining indicated control function.

LINE REGISTER SELECT	CONTROL LINE 1	2	3	4	GENERAL FUNCTION AND COMMENT
4	1	0	0	X	Load sync character
2	0	1	0	X	Load data set register
6	1	1	0	X	Load receiver/transmitter with configuration information
1	0	0	1	X	Output/input data to/from transmitter or receiver
5	1	0	1	X	Input status
5	1	0	1	1	Reset data request ready flip-flop

NOTE

X = Decoding logic not affected by status of this bit when determining indicated control function.

Table 2-5 Decoding-Control and Address Lines

LINE REGISTER SELECT	CONTROL LINES 1 2 3 4	ADDRESS LINES 1 2 3	OUTPUT OF DECODER	ADAPTER INTERFACE	FUNCTION OF DECODED CONTROL SIGNAL
6	1 1 0 X	X 0 1	CONSTA	A	Load/receiver/transmitter with configuration information
6	1 1 0 X	X 1 1	CONSTB	B	Load/receiver/transmitter with configuration information
1	0 0 1 X	1 0 1	XDTSBA	A	Load transmitter data buffer
	0 0 1 X	1 1 1	XDTSBB	B	Load transmitter data buffer
	0 0 1 X	0 0 1	DATENA	A	Enable input from receiver to MLCP
	0 0 1 X	0 0 1	RDTSBA	A	Input receiver data to MLCP
	0 0 1 X	0 1 1	DATENB	B	Enable input from receiver to MLCP
1	0 0 1 X	0 1 1	RDTSBB	B	Input receiver data to MLCP
4	1 0 0 X	0 0 1	RSYSBA	A	Load receiver sync character
4	1 0 0 X	0 1 1	RSYSBB	B	Load receiver sync character
2	0 1 0 X	X 0 1	DTSSTA	A	Load data set control register
2	0 1 0 X	X 1 1	DTSSTB	B	Load data set control register
5	1 0 1 X	X 0 1	SLSTSA	A	Enable and select status multiplexer for this interface
	1 0 1 X	X 1 1	SLSTSB	B	Enable and select status multiplexer for this interface
	1 0 1 1	0 0 1	RRSRDA	A	Reset receiver ready flip-flop
	1 0 1 1	1 0 1	XRSRDA	A	Reset transmitter ready flip-flop
	1 0 1 1	0 1 1	RRSRDB	B	Reset receiver ready flip-flop
5	1 0 1 1	1 1 1	XRSRDB	B	Reset transmitter ready flip-flop
4	1 0 0 X	1 0 1	XSYSBA	A	Load transmitter fill character
4	1 0 0 X	1 1 1	XSYSBB	B	Load transmitter fill character

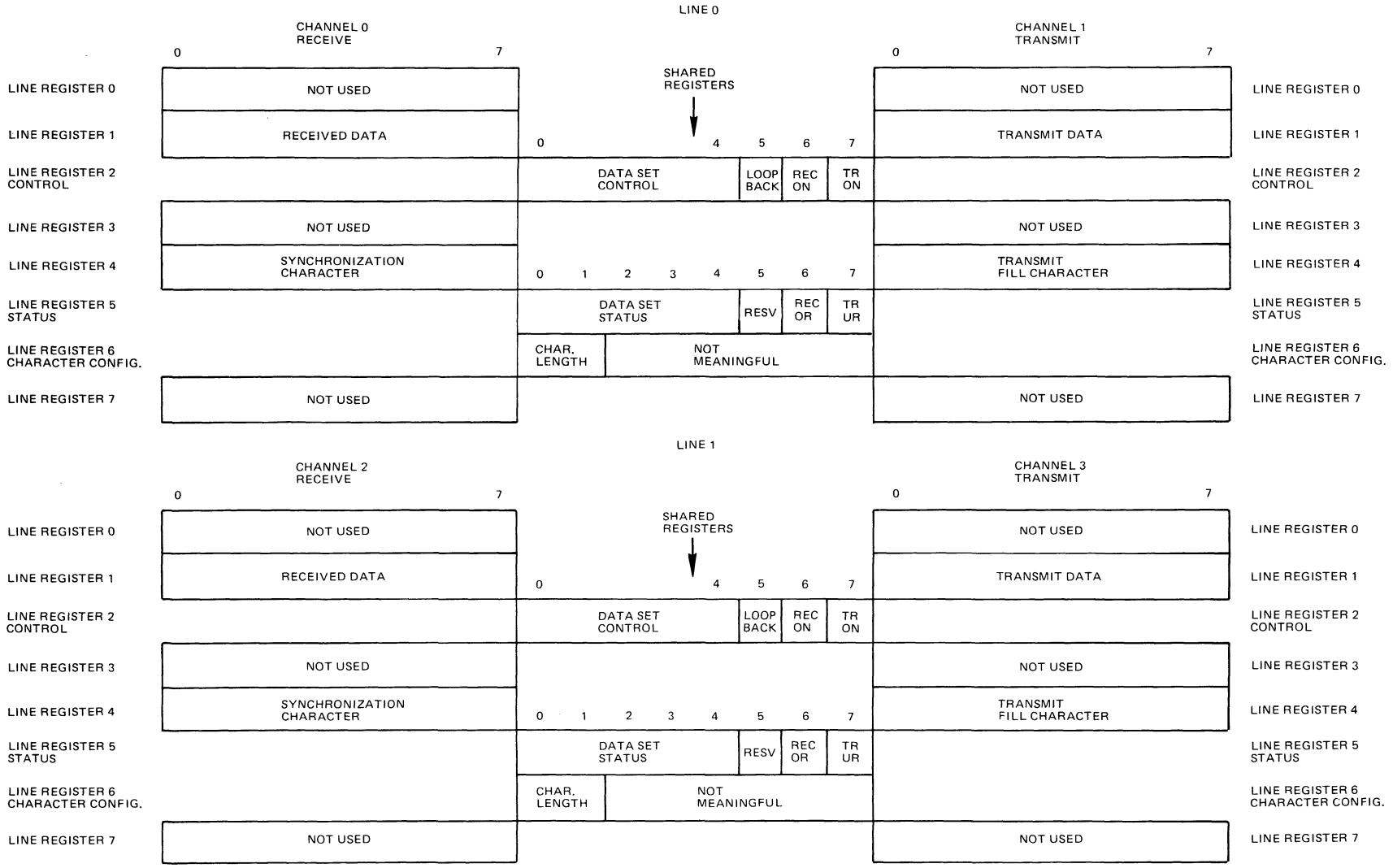

Figure 2-5 Dual SCLA Line Registers

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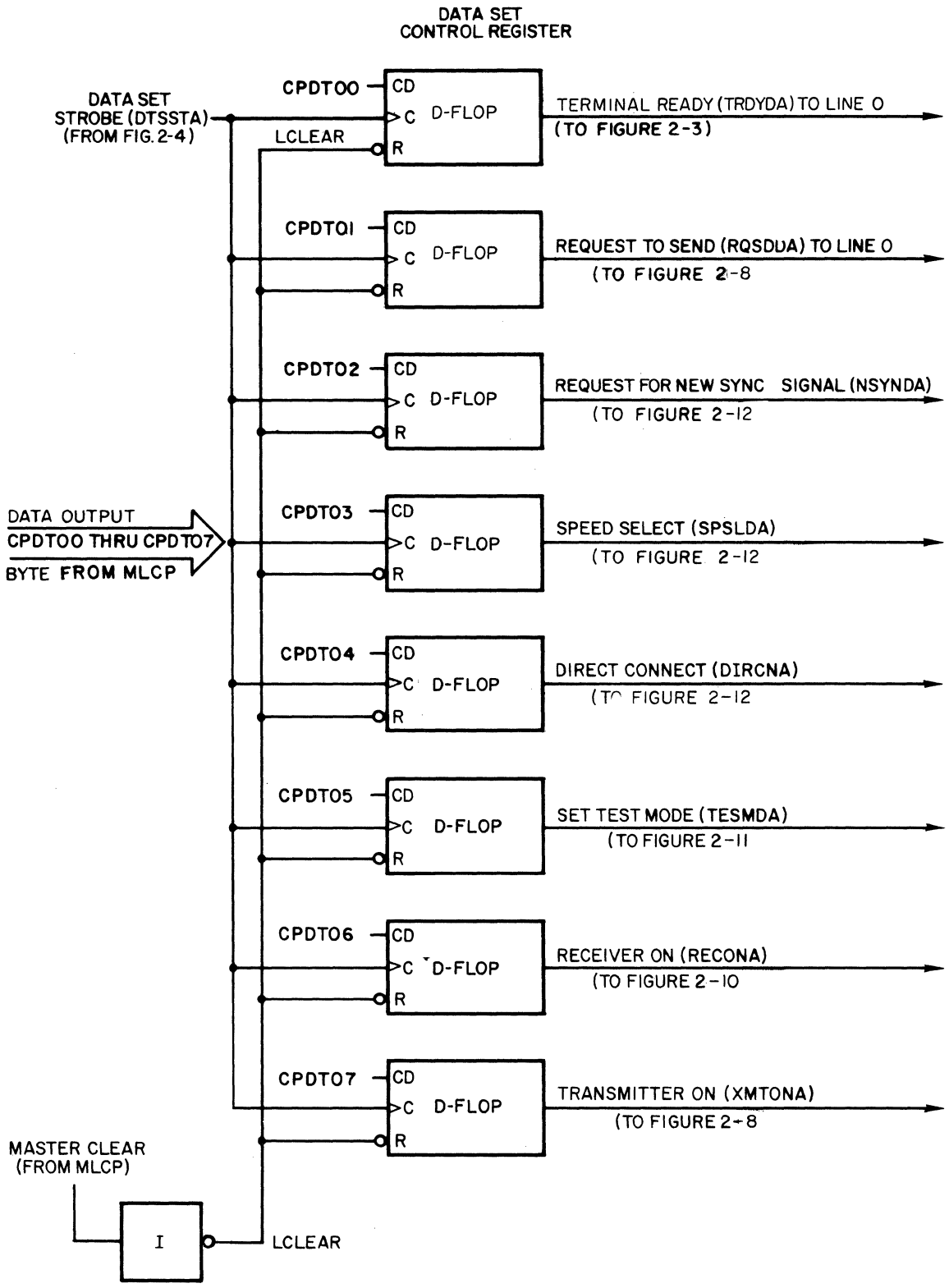

Figure 2-6 Data Set Control Logic

2.2.5 Data Output

The SCLA sends out information to the DCE in a stream of 5-, 6-, 7-, or 8-bit communication-type characters in a continuous block. (See Figure 2-7 for an example of a stream of 6-bit characters.) A character in the stream can be a transmit fill character or a data character. Transmit fill characters are primarily used to notify the receiving equipment of the start of a block of data characters. Transmit fill characters are also used to maintain a continuous stream when data characters are not available during the output operation. Parity generation is inhibited in the SCLA transmitter, but transmitted characters may include a parity bit which is embedded in the byte received from the MLCP.

As shown in Figure 2-8, when the MLCP starts an output operation, it first configures the XMTR/RCVR configuration register to handle either 5-, 6-, 7-, or 8-bit characters. To effect the desired configuration, CPDT00 and CPDT01 are set as shown in Table 2-6 and then strobed into the XMTR/RCVR configuration register by signal CONSTA (see Table 2-5 and Figure 2-4). Note that a 5V input inhibits parity generation by the transmitter.

Next, a transmit fill configuration character must be entered into the transmitter. This is accomplished by the channel program when it sets data lines CPDT00 through CPDT07 with the designated transmit fill character and strobes it into the transmitter with signal XSYSBA (see Table 2-5 and Figure 2-4).

After the configuration information and the configuration transmit fill character are entered into the transmitter, an output operation is started when the channel program turns on the transmitter (XMTONA) and sets Request to Send (RQSDDA). This allows serial data to be sent out to the line as shown in Figure 2-7. The transmitter then requests a data byte to load its data register (RDYXMA). Then if both the Clear to Send and Request to Send are true, the CJ input to the transmitter ready flip-flop is enabled. Then at the next ready flip-flop strobe from the MLCP, the flip-flop sets and sends a ready for a Transmit Data Byte (RDYFXA) to the MLCP. The MLCP then responds by an output or send instruction which strobes a data byte into the transmitter data register (XDTSBA) and resets the transmitter Request (RDYXMA). If the transmitter does not receive a byte from the MLCP in time to maintain the continuous output data stream, it sends out a transmit fill character. An underrun error signal is also generated at this time which is sent to the input multiplexer as a status input (see subsection 2.2.7). When the MLCP has completed its channel program (Wait instruction), it causes an XRSRDA signal to be issued, which resets the transmitter ready flip-flop (RDYFXA).

The voltage level of the bits between the SCLA transmitter and the DCE interface is changed from the TTL level of 0V and +5V to +12V and -12V by the EIA logic. (See Figure 2-7.)

During an output operation with a line, the clock signal (CLKXMA) required to operate the transmitter is received directly from the DCE. However, in the test mode or when using the direct connect feature, the required clock signal originates in the MLCP. The data line to the DCE is placed in a marking condition when in the test mode.

When the channel program in the MLCP desires to conclude the operation, it turns the transmitter off ($\overline{\text{XMTONA}}$). This causes the data line to the DCE to go into the Mark state (see Figure 2-7).

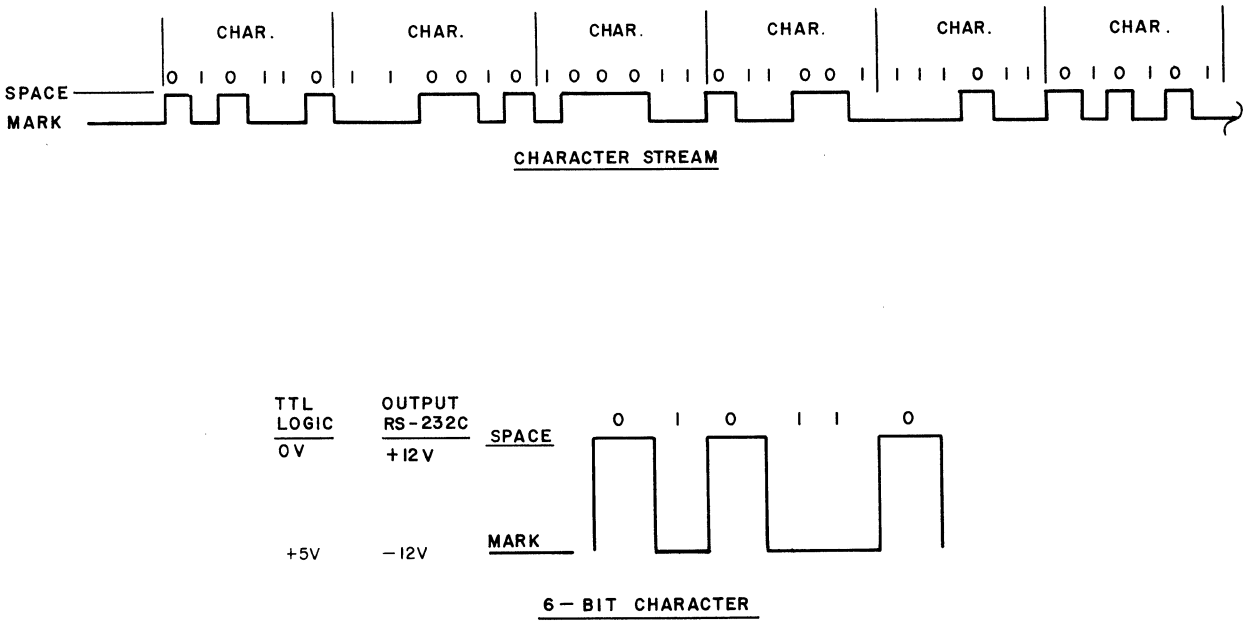

Figure 2-7 Character Transmission

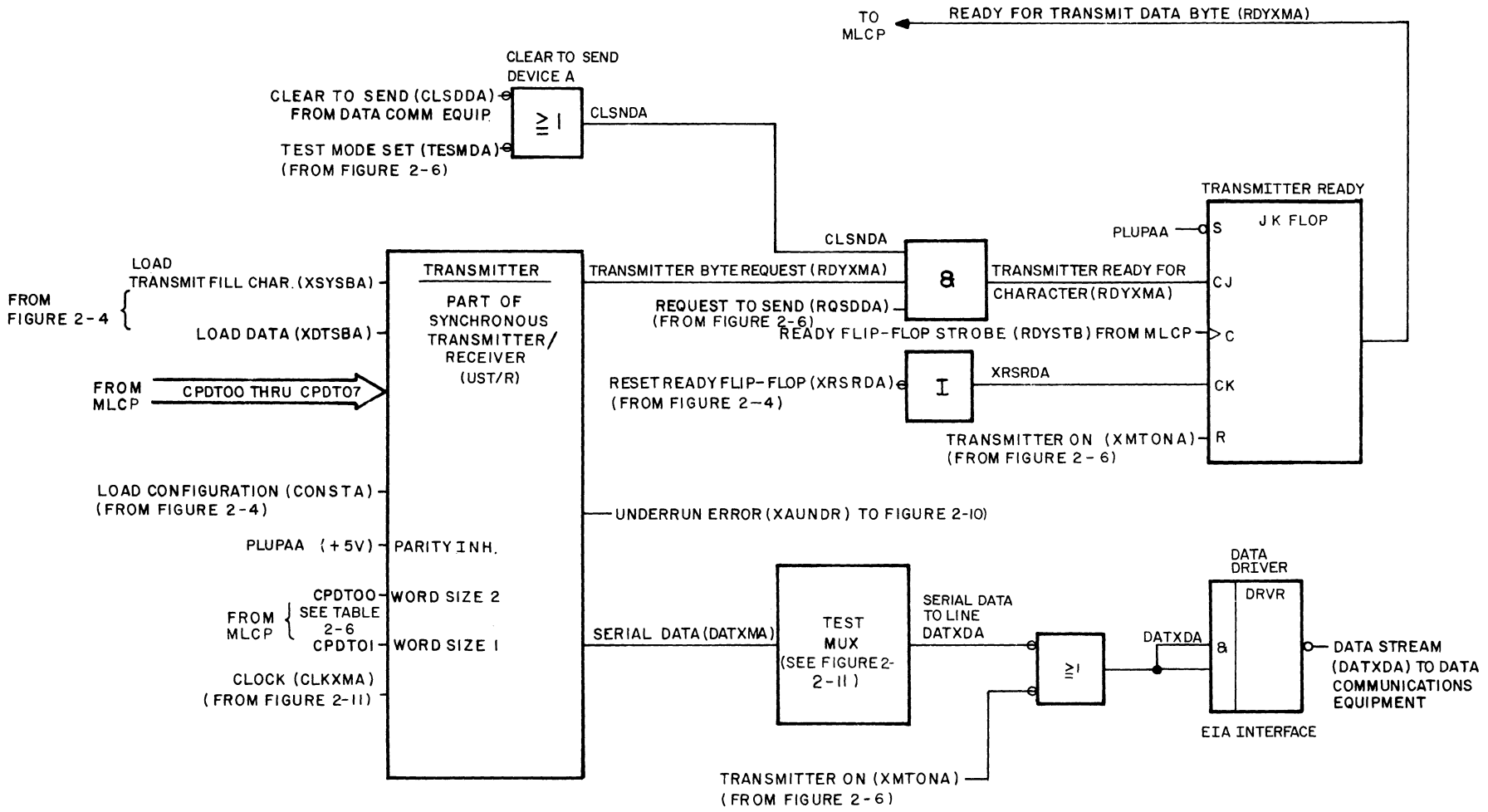

Figure 2-8 Data Output to Data Communications Equipment

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Table 2-6 Transmitter/Receiver Word Size Configuration

Setting		Word Size
CPDT00	CPDT01	(Bits)
0	0	5
0	1	6
1	0	7
1	1	8

2.2.6 Data Input

The adapter receives information from the DCE in a stream of 5-, 6-, 7-, or 8-bit communication-type characters in a continuous stream. (See Figure 2-7 for an example of a stream of 6-bit characters.) The stream may consist of sync characters or data characters. After the receiver in the SCLA recognizes a sync character in an incoming message, it treats that character and all the following characters in the message as data characters. The receiver makes no parity checks on incoming information; however, characters may have parity bits which are transparent to the receiver but are checked in the MLCP. The receiver generates an error (overrun) signal if it has two data bytes ready before one is transferred into the MLCP.

As shown in Figure 2-9, when the channel program starts an input operation it first configures the XMTR/RCVR configuration register to handle either 5-, 6-, 7-, or 8-bit characters in the incoming message. To effect the desired configuration, CPDT00 and CPDT01 are set as shown in Table 2-6 and strobed into the XMTR/RCVR configuration register by CONSTA. (See Table 2-5 and Figure 2-4.) Note that a +5V input always inhibits parity checking by the receiver.

Next, a sync character must be entered into the transmitter/receiver. This is accomplished by the channel program when it sets data lines CPDT00 through CPDT07 with the designated sync character and strobes it into the receiver with signal RSYSBA. (See Table 2-5 and Figure 2-4.)

After the configuration information and the sync character are entered into the receiver, an input operation is started when the MLCP turns on the receiver (RECONA). This sets the receiver in a search mode. In this mode the incoming data bit stream is examined bit by bit until a sync character is found. When the sync character is found, the receiver sends the sync character to a data-holding register within the transmitter/receiver for transfer to the MLCP. At this time the receiver also enables the CJ input to the receiver ready flip-flop (RDYRCA). Then at the next ready flip-flop strobe (RDYSTB) from the MLCP, signal RDYFRA notifies the MLCP that the receiver has a byte ready for transfer. When the receiver identifies the first sync character in the data stream, it sets the receiver in the character mode. In this mode the bits of the incoming data stream are assembled into characters, of the size specified by the configuration register, and sent to the MLCP.

To input a byte from the receiver, the MLCP first connects the data-holding register of the receiver to the MLCP by causing a data enable (DATENA) signal to be issued (see Figure 2-4 and Table 2-5). Then the MLCP transfers the byte with a Received Data Strobe (RDTSBA), input or receive instruction which resets Receiver Request (RDYRCA). Then the receiver ready flip-flop is reset by the MLCP (Wait instruction), causing an RRSRDA signal to be issued. Successive bytes are then transferred as described above from the DCE to the MLCP until the input operation is completed.

During a data input operation, if the receiver has two bytes ready for transfer before one is taken by the MLCP, an overrun (RAOVRN) signal is generated. This error signal is sent to the input status multiplexer and remains on until the next character is received from the DCE.

Between the DCE interface and the SCLA receiver, the level of the bits in the data stream is changed from the EIA level of +3 to +25V, and -3 to -25 to the adapter level of 0V to +5V by the EIA logic.

The channel program stops an input operation by resetting the receiver on (RECONA) signal. This holds the receiver ready flip-flop reset. Note that during an input operation with a line, the clock signal (CLKREA) required to operate the receiver is received directly from the DCE. However, in the test mode or when using the direct connect feature, the required clock signal originates in the MLCP.

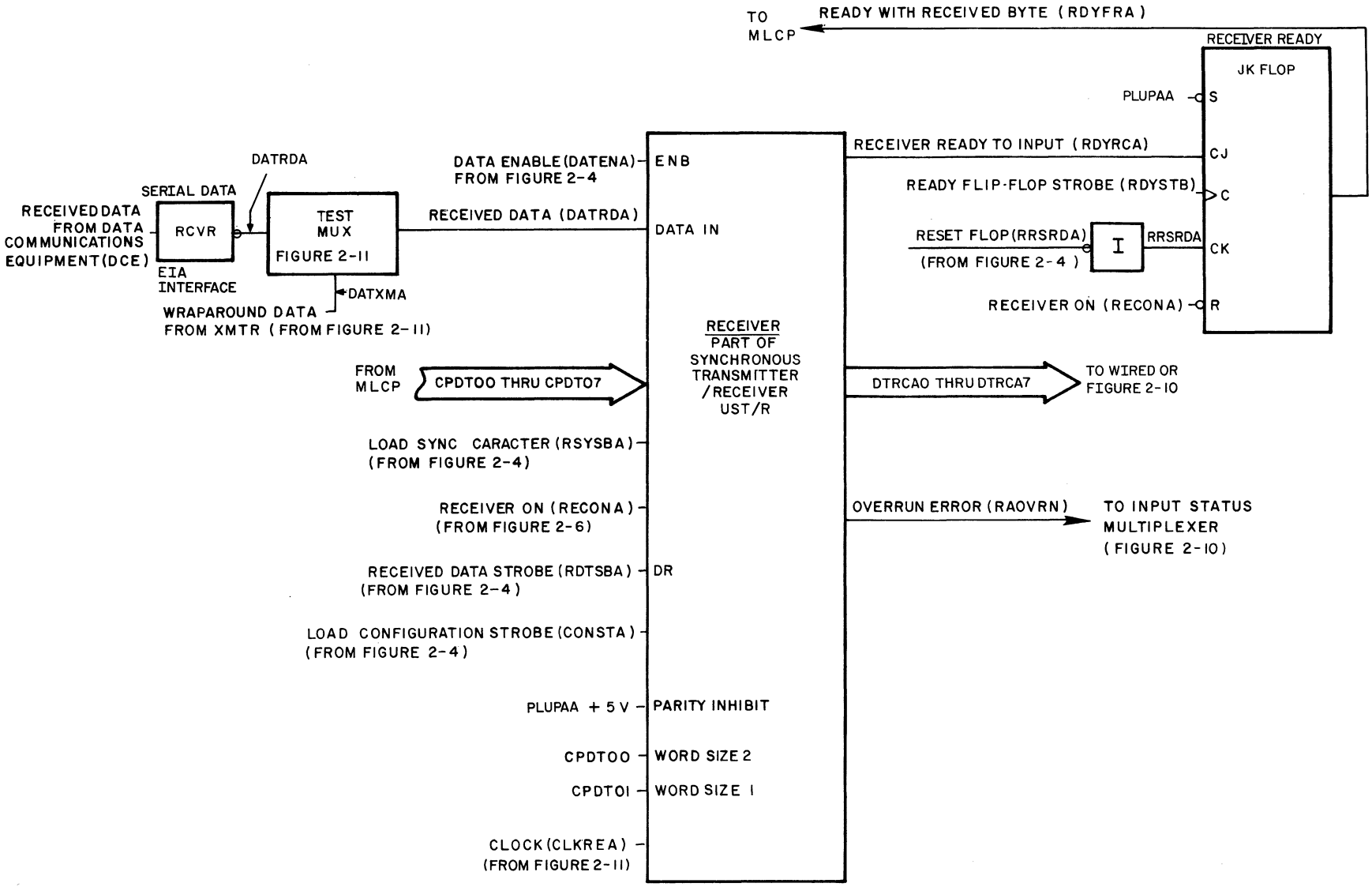

Figure 2-9 Data Input to MLCP from Data Communications Equipment

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2.2.7 Input Status Multiplexer

The input status multiplexer (Figure 2-10) provides a means of sending both error status in the SCLA and status and control information from the DCE to the MLCP. The information sent from the multiplexer to the MLCP may originate in either interface A or interface B or in their respective DCE, depending upon the decoding of the control and address lines from the MLCP. When interface B has not been selected ($\overline{\text{SLSTSB}}$), the multiplexer assumes that interface A and its associated DCE has been selected.

The multiplexer requires an enable signal because it is a tri-state device. When not enabled, all the outputs of the multiplexer are at infinite impedance (floating), thereby disconnecting all logical inputs from the multiplexer into the MLCP. As shown in Figure 2-10, the multiplexer is enabled when the Select Status signal for interface A or B is true.

Each output bit of the multiplexer is hard-wired to the corresponding data input bit from both interface A and interface B prior to being sent to the MLCP. All data input and status bytes are sent to the MLCP via the LADT00 through LADT07 connections. Table 2-7 lists the source and function of all inputs into the status input multiplexer.

2.2.8 Test Multiplexer

A test multiplexer (Figure 2-11) in each interface provides the interface of the SCLA with a wraparound feature. This feature allows serial data out of the transmitter to be sent directly back to the receiver. Diagnostic software uses the wraparound feature to check the operation of the transmitter and receiver by comparing a data byte sent out by the MLCP to the byte received back. Operation with the DCE is precluded when the wraparound logic is enabled. Refer to Appendix A for supplemental information pertaining to wraparound.

As shown in Figure 2-11, a Zero (ground) is placed on the enabling input of the multiplexer. This, in effect, negates the tri-state feature of the multiplexer so that the outputs are always logically connected to either the selected Zero or One input. (Note that Figure 2-11 shows the multiplexer for interface A. The multiplexer for interface B is connected in a similar manner, but the Set Test Mode signal (TESMDA) is generated in the logic of interface A only.)

When operating on-line (test mode not set), the logic One inputs to the multiplexer are connected to the corresponding output. This makes the following normal operating connections within the multiplexers.

INPUT	OUTPUT
MULTIPLEXER - INTERFACE A	
Receive clock from DCE Transmit clock from DCE Line - Interface A Transmitter - Interface A	Clock signal to Rcvr - Interface A Clock signal to Xmtr - Interface A Rcvr - Interface A Line - Interface A
MULTIPLEXER - INTERFACE B	
Receive clock from DCE Transmit clock from DCE Line - Interface B Transmitter - Interface B	Clock signal to Rcvr - Interface B Clock signal to Xmtr - Interface B Rcvr - Interface B Line - Interface B

When the test mode is set, the Zero inputs to the multiplexers are connected to the corresponding output. This makes the following connections within the multiplexers.

INPUT	OUTPUT
MULTIPLEXER - INTERFACE A	
Test clock from MLCP Test clock from MLCP Data stream from Xmtr - Interface A PLUPPA (+5V)	Clock signal to Rcvr - Interface A Clock signal to Xmtr - Interface A Data stream to Rcvr - Interface A Line - Interface A
MULTIPLEXER - INTERFACE B	
Test clock from MLCP Test clock from MLCP Data stream from Xmtr - Interface B PLUPPA (+5V)	Clock signal to Rcvr - Interface B Clock signal to Xmtr - Interface B Data stream to Rcvr - Interface B Line - Interface B

As shown in Figure 2-11, a Mark signal is always sent out to the line if the transmitter is not on ($\overline{\text{XMTONA}}$) or the test mode is set. In the test mode the PLUPPA (+5V) input to the multiplexer causes DATXDA to go low, which in turn causes a low (Mark) signal to go out to the DCE.

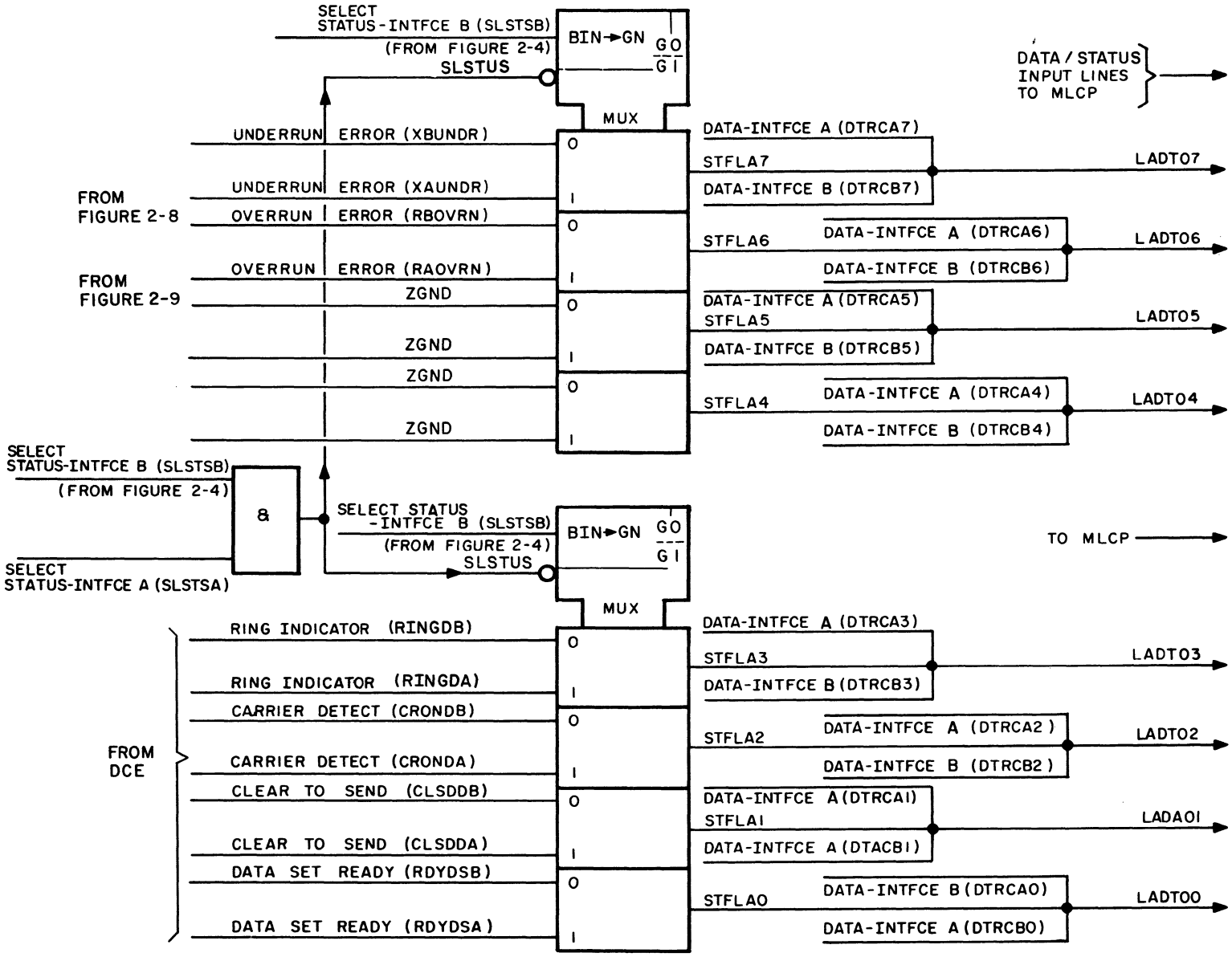

Figure 2-10 Input Status Multiplexer Logic

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Table 2-7 Inputs to Input Status Multiplexer

INPUT SIGNAL	SOURCE	COMMENT
XBUNDR XAUNDR	Adapter transmitter-interface B Adapter transmitter-interface A	Indicates that the transmitter has not received data bytes from the MLCP fast enough to maintain data stream (underrun error). The transmitter has sent a transmit fill character to maintain the data output stream.
RBOVRN RAOVRN	Adapter receiver-interface B Adapter receiver-interface A	Indicates that the receiver had two data bytes ready before one was transferred to the MLCP (overrun error).
RINGDB RINGDA	DCE of interface B DCE of interface A	The associated line is ringing and is trying to get the attention of the MLCP.
CRONDB CRONDA	DCE of interface B DCE of interface A	Indicates that the basic carrier frequency of the associated communication line is present.
CLSDDB CLSDDA	DCE of interface B DCE of interface A	A response by the associated DCE to a request-to-send signal from the SCLA.
RDYDSB RDYDSA	DCE of interface B DCE of interface A	A signal from the associated DCE indicating that it is ready to operate.

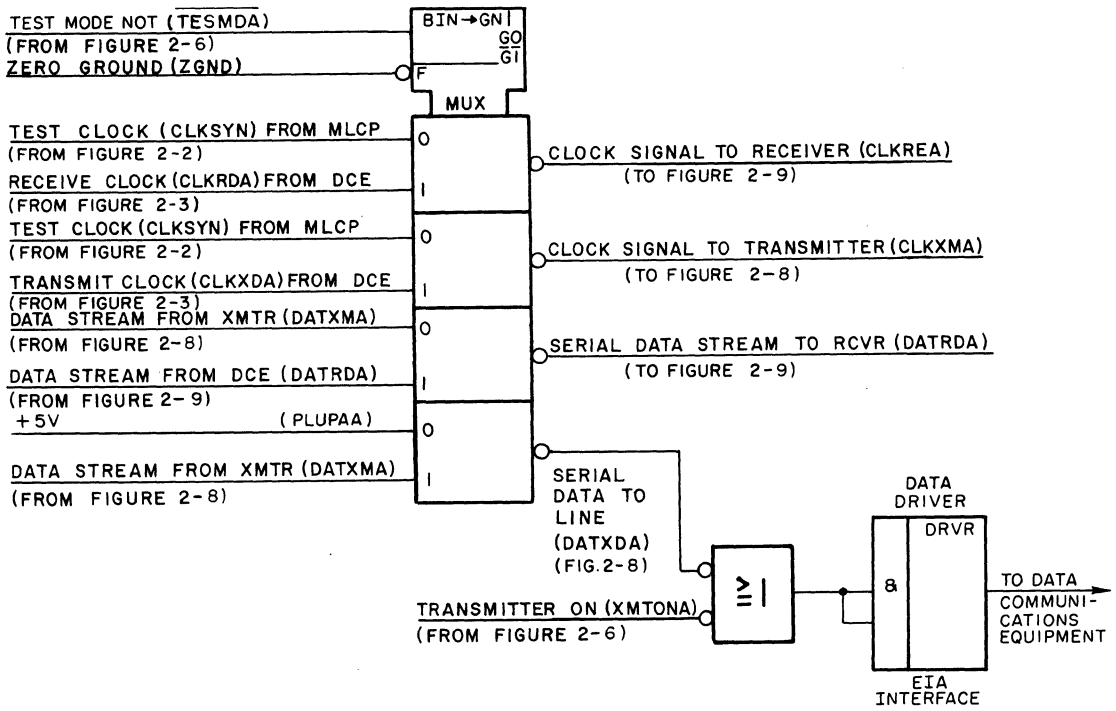


Figure 2-11 Test Multiplexer Logic

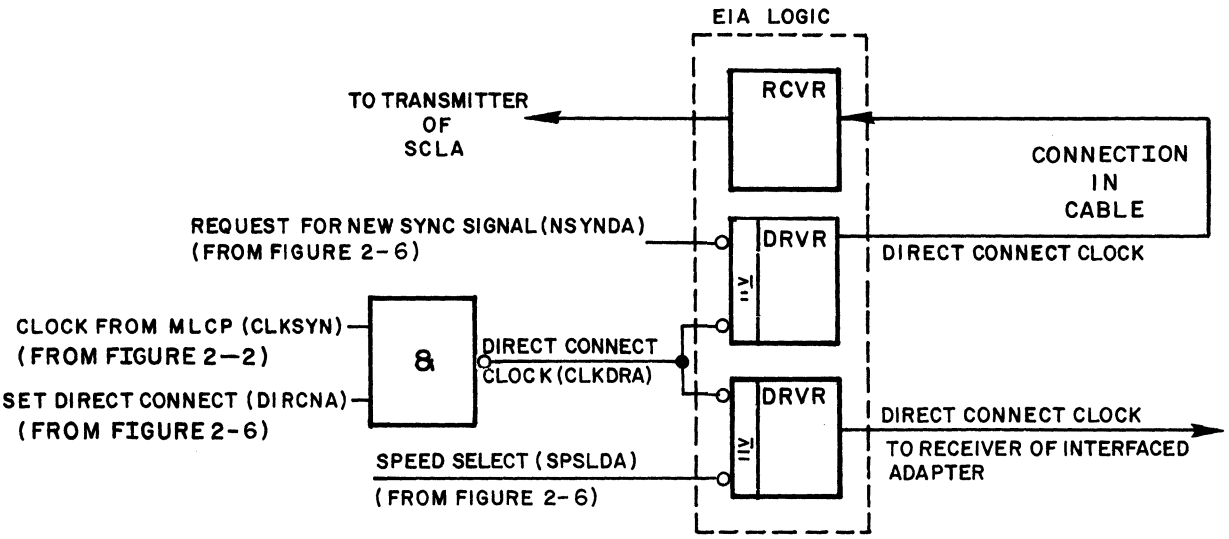
2.2.9 Direct Connect Logic

The additional logic associated with the direct connect feature is shown in Figure 2-12 (A). This logic is installed in both interface A and interface B of the SCLA at the time of delivery. However, a different cable out of the SCLA is required when using a direct connection rather than a line connection.

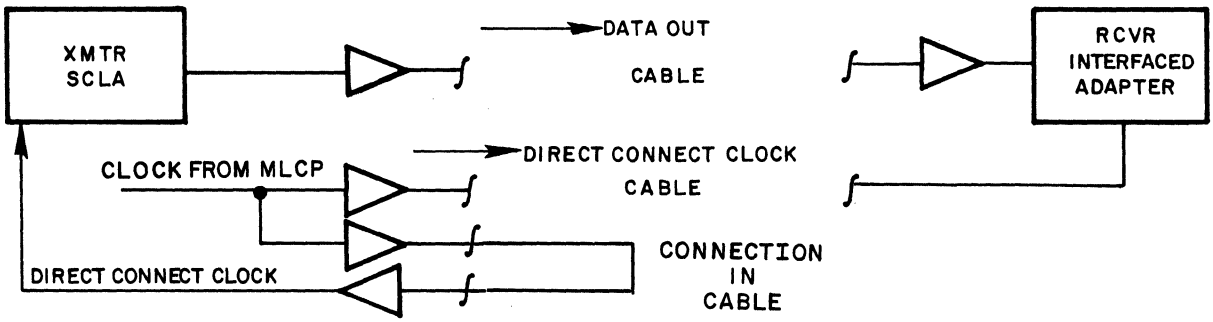
As shown in Figure 2-12 (A), when the direct connect mode (DIRCNA) is set, each clock pulse from the MLCP (CLKSYN) sets the direct connect clock signal (CLKDRA) which is sent to both the transmitter of the SCLA and the receiver of the interfaced adapter. The Direct Connect clock (CLKDRA) is used when the SCLA is transmitting in the direct connect mode. (See Figure 2-12, B.) As shown in Figure 2-12 (C), when the SCLA is receiving data in the direct connect mode, a clock signal from the interfaced equipment is sent to both the receiver of the SCLA and the transmitter of the interfaced adapter. In the direct connect mode, data-out and data-in operations are performed as previously described in this manual.

Note that neither the NSYNDA nor the SPSLDA flip-flop should be used when a direct connect operation is being performed. Also note that when a line connection interface is used, the direct connect (DIRCNA) signal should be false. This forces the CLKDRA signal high, thereby allowing the NSYNDA and SPSLDA flip-flops to perform their normal line connection control function. (See subsection 2.2.4.)

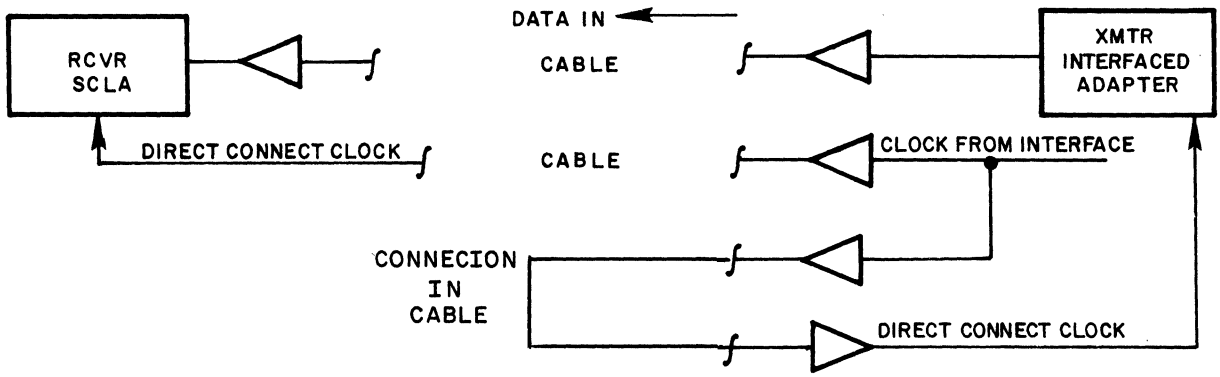
The cable requirements for the direct connect option are listed in Appendix B.



DIRECT CONNECT LOGIC IN SCLA
(A)



SCLA TRANSMITTING - DIRECT CONNECT
(B)



SCLA RECEIVING— DIRECT CONNECT
(C)

Figure 2-12 Direct Connect Logic

III
THEORY OF OPERATION - CYCLE FLOW

The firmware associated with the Synchronous Communications Line Adapter (SCLA) is physically located in the Multiline Communications Processor (MLCP). Because the overall operation of the MLCP firmware is indivisible, it is impractical to describe the functions pertaining to the SCLA separately. Accordingly, the MLCP manual (Document No. 71010230-200) should be used to obtain specific information on firmware related to the SCLA.

Appendix A

Wraparound Test

Through the use of a Test and Verification Program, two wraparound tests can be performed on the SCLA.

The first test, DCMT1-mode A, performs an internal wraparound of the SCLA, checking the integrity of the SCLA to transmit and receive data properly. Serial data is sent out of the transmitter and returned directly back to the receiver. The received data must match the transmitted data to verify integrity.

The second test, DCMT1-mode C, performs an external wraparound of the DCE interface and the DCE cable. This test verifies the integrity of the DCE interface and cable. To perform the external wraparound test, the DCE connectors D and F, at the DCE end of the DCE cable, are terminated by two EIA jumper connectors. These connectors are wired as shown in Table A-1.

For information pertaining to the sequence of steps required to run these programs, refer to the Level 6 System Checkout and Operator's Guide. For cabling information refer to the Model 34/36 Systems Manual.

Table A-1 EIA Connector Jumpers for DCMT1 Loop Test (C Mode)

EIA CONNECTOR PIN NUMBERS TO BE JUMPERED	INTERFACE SIGNAL NAMES
02 to 03	Transmit data to receive data
06 to 20	Data set ready to terminal ready
04 to 05 to 08	Request to send to clear to send to carrier detect
14 to 15	New sync to transmit clock
17 to 22 to 23 to 25	Receive clock to ring indicator to speed select to reserved line (jumper to pin 25 is optional in SCLA)

Appendix B
Cabling

The Type DCM9103 dual Synchronous Communications Line Adapter (SCLA) is cabled in accordance with the system configuration which dictates three possible environments.

Most system configurations connect the Communications-Pac to data communications equipment (DCE) or a remote Communications-Pac via modems and a phone line. Figure B-1 illustrates a typical communications configuration and identifies the type of cable used and the connector type, i.e., male (M).

The system can also be configured to either of two direct connect applications. If the two pieces of equipment are in close proximity to each other (less than 61 feet apart for RS232C applications) a short jumper cable (direct connect female to female) replaces the modem/phone line combination. Figure B-2 shows the cabling requirements for this configuration, i.e., two dataset cables with male (M) connectors and one direct connect cable with female (F) connectors.

For direct connect applications, whereby the Communications-Pac is connected directly to another Communications-Pac or data terminal equipment without the use of data communications equipment, the use of a direct connect cable (male to female) and a dataset cable is required. One cable cannot be used for this application due to signal inconsistencies at the connector pinouts. Figure B-3 shows the cable requirements for this configuration, i.e., one dataset cable with male connectors (M) and one direct connect cable with a male (M) and a female (F) connector. The total combined length of the two cables cannot exceed 50 feet.

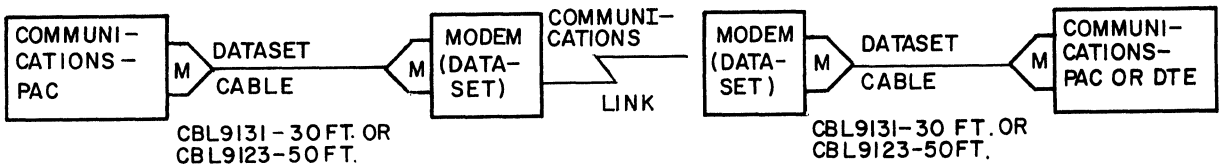


Figure B-1 Typical Modem Configuration

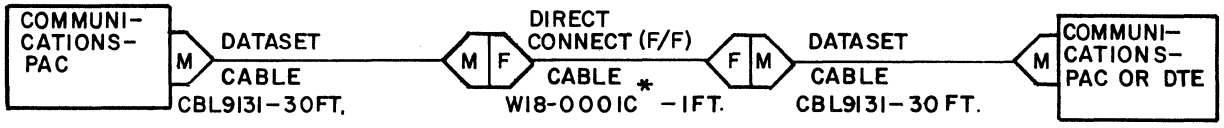


Figure B-2 Direct Connect Female/Female

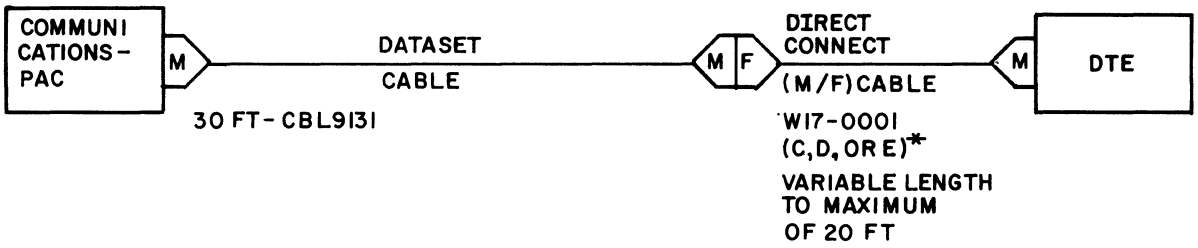


Figure B-3 Direct Connect Male/Female

* C - Connectors assembled to both ends.

D - Disassembled with two connectors shipped unattached.

E - One connector assembled to cable (paddle board side); other connector shipped but not attached.

USERS' REMARKS FORM

TITLE:

DOC. PART NO. _____

DATED _____

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

Fold

DATE _____

FROM: NAME _____

COMPANY _____ M/S _____

TITLE _____

ADDRESS _____

_____ ZIP _____

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DOC. PART NO. _____

DATED _____

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

Fold

DATE _____

FROM: NAME _____

COMPANY _____ M/S _____

TITLE _____

ADDRESS _____

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