Honeywell

LEVEL 6

HARDWARE

TYPE PRM9101 PRINTER ADAPTER MANUAL

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PRM9101

PRINTER ADAPTER MANUAL

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FL18

2.3 FUNDAMENTAL HARDWARE DESCRIPTION

The following discussion presents detailed logic descriptions of the four major elements of the printer adapter as shown in Figure 2-1.

2.3.1 Control Logic

Figure 2-3 is an intermediate block diagram of the major control logic elements and controlling interconnecting signals. These logic elements include:

- End-of-form logic
- End-of-form delay logic
- Strobe logic
- Vertical format unit sequence logic
- Data service request logic
- Nondata service request logic

2.3.1.1 End of Form

As shown in Figure 2-3 (A), whenever the printer spaces up to or beyond the end of form, a flip-flop is set, and a status signal is sent to the input multiplexer (see subsection 2.3.3). This End-of-Form flip-flop is then reset when the firmware issues an ALUOT3 signal after it receives the next IOLD instruction. A clear signal also resets the flip-flop. For diagnostic purposes, the flip-flop can also be set by an ALUOT3 signal when Control Line 1 of the adapter is high.

2.3.1.2 End of Form Delay

When the MDC sends a spacing command to the printer, it must allow time for mechanical positioning before checking the end of form status. Consequently, as shown in Figure 2-3 (B), after each spacing command the firmware starts an end-of-form delay by causing Control Line 2 and ALUOT4 to be true. The end-of-form delay timing, which determines the printer speed in lines per minute, is selected by the setting of a hex rotary switch (See Figure 2-3B for switch setting). After the delay, the end-of-operation flip-flop is set, causing both a nondata service request signal to be sent to the MDC and a status signal to the input multiplexer. The end-of-operation flip-flop is then reset by the firmware by means of the ALUOT0 and Control Line 2 prior to sending out further data to the printer. A clear signal also resets the flip-flop. For diagnostic purposes the flip-flop can also be set by an ALUOT7 signal when Control Line 2 of the adapter is true.

2.3.1.3 Strobe Logic

A strobe signal is sent to the printer to notify it that the data on the line drivers is valid (see Figure 2-3, C). The printer then takes the character from the lines and takes appropriate action. To generate the strobe, the MDC firmware enables the Printer Strobe flip-flop by enabling the adapter and then issues an adapter pulse.

The next clock strobe from the MDC then sets the flip-flop and a strobe signal is sent out to the printer. To ensure that the strobe signal to the printer is at least 500 nanoseconds long, the firmware issues two consecutive Adapter pulse signals, thereby forcing the flip-flop to maintain the output strobe for the required 500 nanoseconds. The flip-flop is reset on the clock strobe after the Enable Strobe signal goes low, or when the adapter is cleared.

2.3.1.4 Vertical Format Unit (VFU) Sequence

The VFU option controls vertical spacing in the printer. The logic for performing this function is shown in Figure 2-3(D).

When vertical spacing is required, firmware enables the adapter and raises Control Line 1 and ALUOT4. This enables the VFU sequence flip-flop, which is set on the next clock strobe from the MDC. The output of the flip-flop is then slope-controlled and sent to the printer via a line driver. The VFU sequence flip-flop is reset when the data buffer of the adapter is loaded for printing the next line.

2.3.1.5 Data Service Requests

Whenever the printer requires data for printing, it signals the adapter via the Printer Demand (LPDEMD) interface line. As shown in Figure 2-3 (E), this signal sets the data service request flip-flop, which sends a signal to the MDC. The flip-flop is then reset when the firmware strobes the printer, or issues a Control Line 2 signal with ALUOT2 high. Note that the flip-flop is also reset by a clear signal. For diagnostic purposes, the firmware may also set the data service request flip-flop by issuing a control Line 2 signal with ALUOT5 high.

2.3.1.6 Nondata Service Request

Whenever the printer goes off line, a nondata service request is sent from the adapter to the MDC. The logic that generates this service request is shown in Figure 2-3(F). Note that the flip-flop can also be set by an End-of-Operation signal after the end of form one-shot times out. (See Subsection 2.3.1.2.) The nondata service request flip-flop is reset when the firmware issues a Control Line 2 signal with ALUTOT1 high.

2.3.2 Data Buffer Register

Figure 2-4 shows the data buffer logic for the printer adapter. The buffer actually consists of two 4-bit synchronous load registers which are parallel loaded and output a parallel byte to the line drivers. The MYDATA input to the register causes the register to be a parallel input/output device rather than a shift register. Firmware loads the register by placing the data on the ALUOT lines and then causing a register strobe (REGSTB) signal to be generated. When the data is loaded into the register, it is simultaneously sent to the line driver logic. Data remains stored in the buffer until the next load operation or when the firmware clears the adapter.

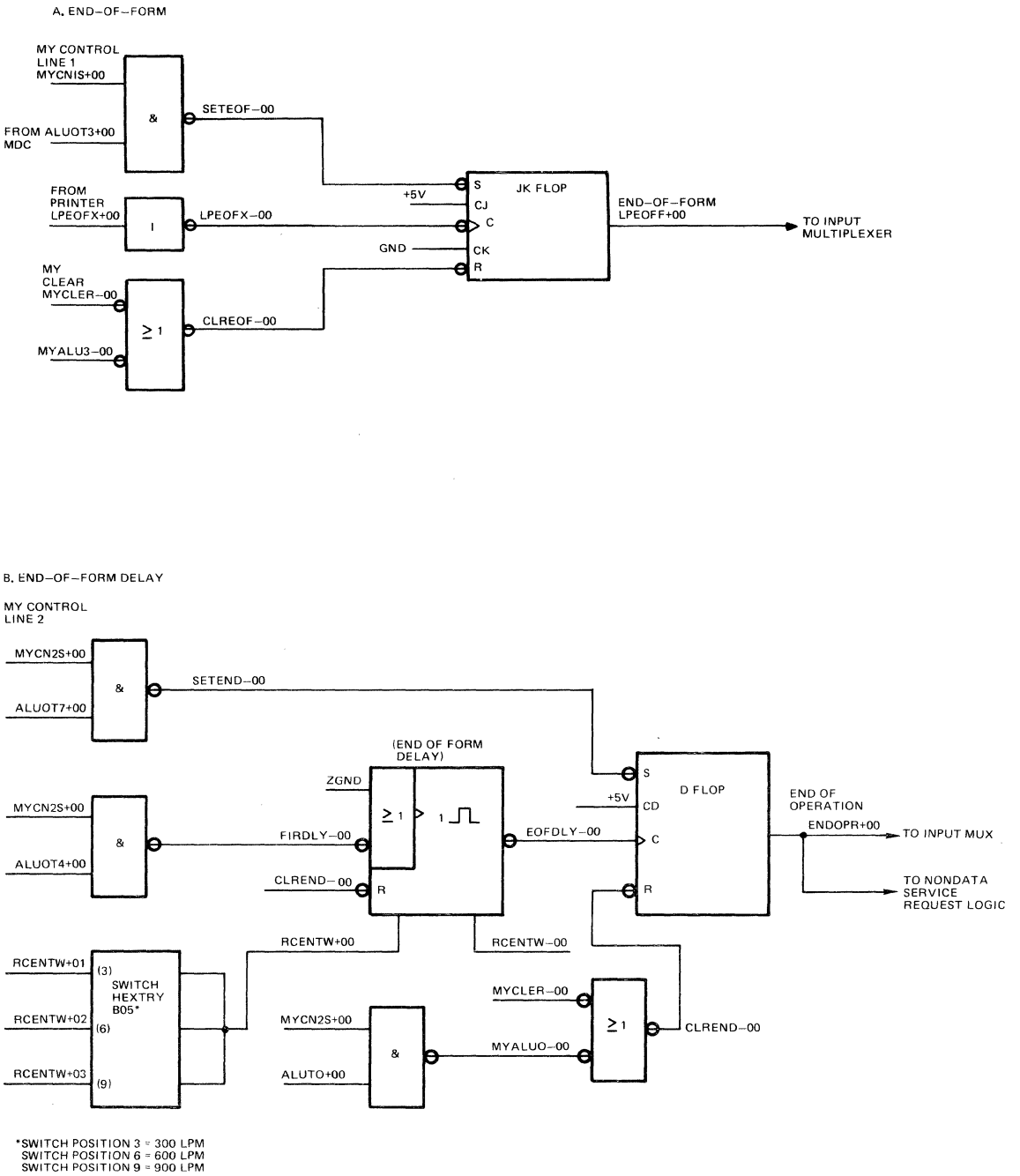

Figure 2-3 Control Logic (Sheet 1 of 2)

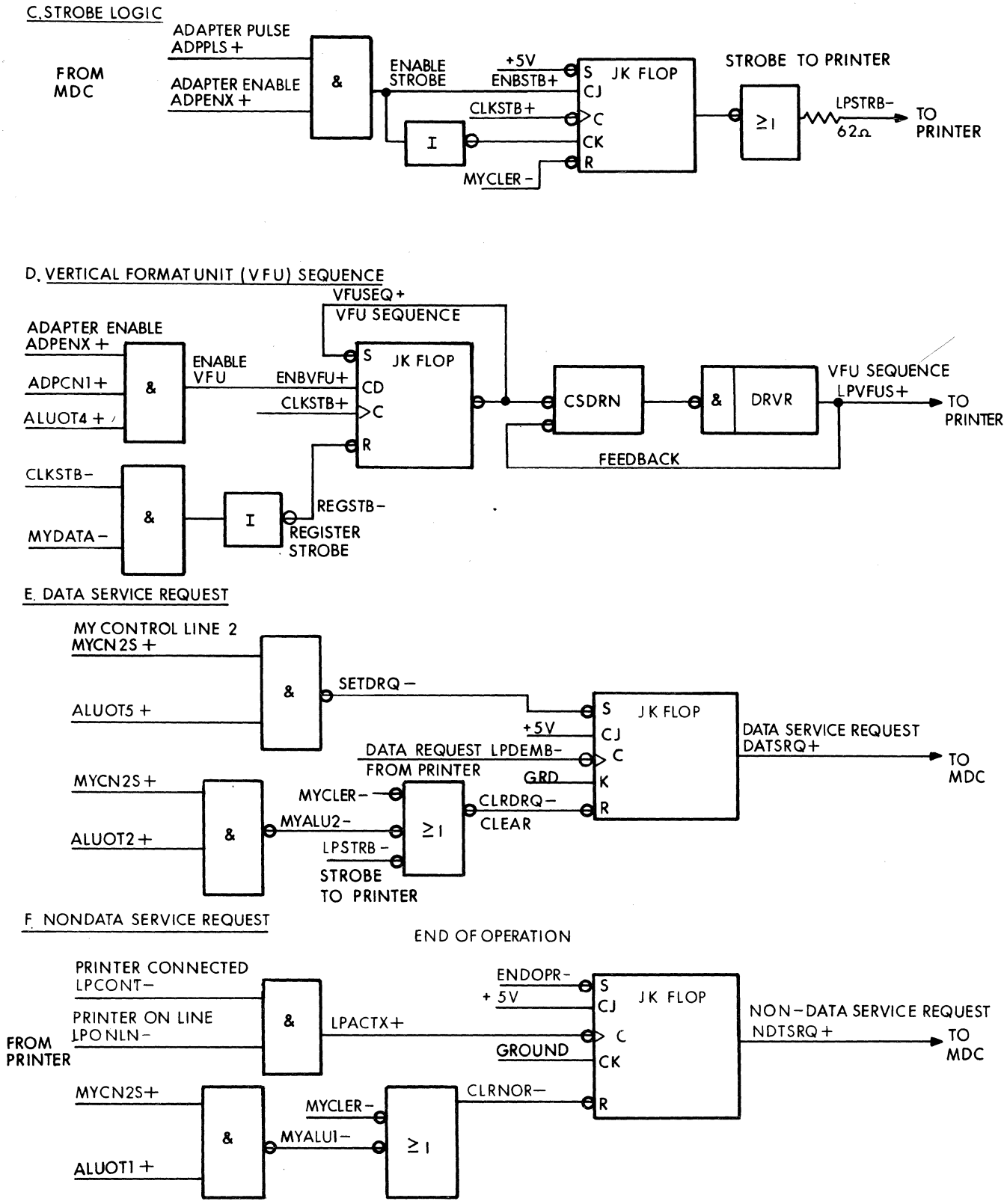

Figure 2-3 Control Logic (Sheet 2 of 2)

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