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NOTE

This EPS-1, if not revised within one year, should be considered obsolete and therefore reference should be made to the appropriate product manual.

HONEYWELL INFORMATION SYSTEMS

SYSTEMS ENGINEERING - BOSTON

ENGINEERING PRODUCT SPECIFICATION (EPS - 1)

SUBSYSTEM LEVEL

TITLE: NMLC HDLC/SDLC ADAPTER

VERSION: APPROVED DATE: _____

PRODUCT CALENDAR REFERENCE: _____

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INTRODUCTION

1.1 SCOPE

This document defines the functions, operations, performance, interfaces, and design requirements of the NMLC HDLC/SDLC Adapter (NHSA) which attaches to the Level 6 New Multiline Controller (NMLC).

1.2 REFERENCE DOCUMENTS

1. 60126448, Level 6 System EPS-1.
2. 60126298, Level 6 Bus EPS-1.
3. CC71, Level 6 Mini Computer Handbook.
4. 60126885, Multiline Communications Processor (MLCP) EPS-1.
5. 60141665, New Multiline Controller (NMLC) EPS-1.
6. 60144425, NMLC Synchronous/Asynchronous Adapter (NSAA) EPS-1.
7. 60144541, Broadband HDLC/SYNC Adapter EPS-1.
8. Honeywell Standard B06.04, Serial Interface Between DTE/DCE.
9. Honeywell Standard B06.03, Character Structure.
10. Honeywell Standard B06.02, Transmission Code.
11. Honeywell Standard B06.01, Signaling Rates.
12. Honeywell Standard B06.00, Data Communications.
13. Honeywell Standard B01.08, Electromagnetic Noise.
14. Honeywell Standard B01.09, Physical Noise.
15. D.002.01, PWB/PWA Testability Design Rules.
16. MTG2, PWA Test Documentation Requirements.

18. MTG3, PWA Microdiagnostic Creation.

19. MTG5, QLT Creation.

20. MTG6, T&V Creation.

21. 58035052, Worldwide Maintenance Requirements.

22. EIA Standard RS-232C, Interface Between data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange.

1.3 DEFINITIONS

ASCII	-	American Standard Code for Information Interchange.
Channel	-	A Simplex communications path with associated control. Two channels are required for each HDX or FDX line.
CLM	-	Configuration Load Manager.
CPU	-	Central Processor Unit.
DCE	-	Data Communications Equipment.
DMA	-	Direct Memory Access.
DTE	-	Data Terminal Equipment.
FDX	-	Full Duplex.
FR	-	FLAP Register.
HDLC	-	High Level Data Link Control.
HDX	-	Half Duplex.
ID	-	Identification.
I/O	-	Input/Output.
L6	-	Level 6 Minicomputer System.
LR	-	Line Register.
MBZ	-	Must be Zero.
MLCP	-	Multiline Communications Processor.
NBHSA	-	NMLC Broadband HDLC/Sync Adapter.
NMLC	-	New Multiline Controller.
ORU	-	Optimum Replaceable Unit.
QLT	-	Quality Logic Test.
RFU	-	Reserved for Future Use.
RHU	-	Reserved for Hardware Use.
SDLC	-	Synchronous Data Link Control.
TBD	-	To be Defined.
T&V	-	Test and Verification.
USRT	-	Universal Synchronous Receiver/Transmitter.

II OVERVIEW

2.1 GENERAL

The NMLC HDLC/SDLC Adapter (NHSA) is packaged on a quarter-sized daughter board which attaches to the New Multiline Controller (NMLC/MLC-16). The NHSA supports two communication lines operating in full or half duplex communications using HDLC/SDLC bit-oriented protocols. Maximum line speed is 19.2 Kbps.

The adapter provides a basic RS232C/V.24 interface on each line which permits connection to DCEs or direct connection to RS232C DTEs which support HDLC/SDLC protocol.

2.2 SOFTWARE COMPATIBILITY

A key requirement is that HDLC/SDLC CCPs written for the NBHSA Broadband adapter shall run without change on the NHSA.

The prime visibility of the NBHSA adapter to the CCP for control, data access and status-sensing purposes is that of a set of Line Registers (LRs) and FLAP Registers (FRs). In the NHSA, this same visibility and assignment of LRs and FRs will be maintained. Firmware will map the LR/FR content into/from the appropriate spots in the NHSA.

The NHSA simulates the FLAP registers (FRs) associated with a RS232C/V.24 FLAP associated with the line. These registers implement data set control and data set status functions associated with the DCE.

Two other registers are also visible: an Adapter Control register and an Adapter Status register. These contain the adapter-related bits of LR2 and LR5 respectively. There are performance advantages to accessing either these registers or FR2 and FR5 instead of LR2 and LR5.

In the NMLC/NHSA configurations, firmware will automatically map LR bits to FR register bits on OUT type CCP instructions, and will assemble FR bits on IN type CCP instructions as appropriate.

Associated with each line's USRT in the NHSA is a set of registers for control and status indication of the USRT itself. Firmware automatically provides mapping of LR bits into and from the appropriate USRT registers. In order that existing CCPs may be used with the NHSA, necessary access to USRT registers not represented in the LRs must not require CCP instructions; this also allows future replacement of the USRT component with a newer type without impacting the viability of existing CCPs. USRT control error sensing, error reset, etc.) will be performed automatically by firmware. Thus, replacement of the USRT with a newer type would impact firmware but would not affect the CCP.

Figure 2-1 shows the register sets associated with each line of the NHSA and their means of access by software.

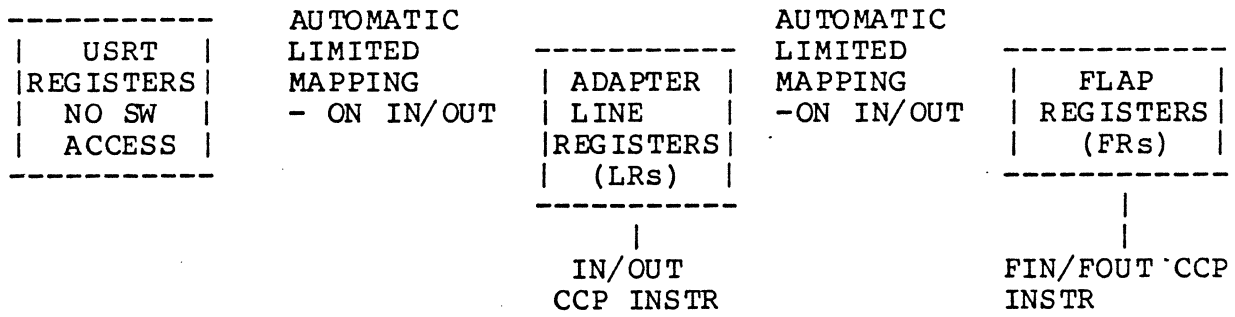


Figure 2-1 NHSA Register Access

2.3 DATA FORMAT

The format of data transferred between the NHSA and the communication equipment conforms to the High Level Data Link Control standards. The fields of the frame and other HDLC attributes are described here for information purposes along with the relationship of hardware and software regarding implementation responsibility. Further details may be found in the referenced HIS standards.

2.3.1 General Format of HDLC/SDLC Frame

In the HDLC/SDLC communications link control procedure, all transmissions are in "frames". The format of a typical frame is shown in Figure 2-2

DIRECTION OF TRANSMISSION

\- - - - - - - - - - - >

| F | FCS | I | C | A | F |

Where the Fields are:

F - Flag Sequence (01111110)
A - Address Field (8 bits; optionally n x 8 bits)
C - Control Field (8 bits; optionally 16 bits)
I - Information Field (any number of characters, optional)

FCS - Frame Check Sequence (16 bits)

Figure 2-2 General Format of HDLC/SDLC Frame

The Flag sequence and the A, C, I, and FCS fields each consist of a multiple of eight bits. For contiguous frames, a single flag sequence may serve as the closing flag for the first frame and the opening flag for the next.

After transmission of a frame is complete, if the next frame is not ready, the NHSA transmitter will send interframe time fill until data for the next frame is available. The receiver will discard interframe time fill. Interframe time fill consists of continuous Flags. When interframe fill is being transmitted, the link is still considered to be in an active state, i.e., the transmitter still has the right to recommence transmission of frames.

There is no provision for intraframe time fill; when such a situation arises, Frame Abort procedure is followed. Abort is the procedure by which a transmitter may terminate the current frame in an unusual manner such that the receiver will ignore the frame. Abort sequences are generated by the transmitter on an output error condition (underrun). A Frame Abort consists of the transmission of at least seven but less than fifteen contiguous Ones. When the receiver detects an Abort Sequence, it notifies the receiving CCP program through status. Transmission of fifteen or more Ones is defined to put the link into an IDLE state; this may occur following an Abort or following a completed frame. When entry into Idle state is detected the receiver reports it to the receiving program via status.

The minimum number of bits between the Flags in a valid frame is 32 (consisting of 8 Address, 8 Control, and 16 FCS). A frame of less than 32 bits should be discarded by the receiving CCP.

In order to prevent accidental and unwanted Flag or Abort sequences from occurring between opening and closing Flags, a "zero bit insertion" procedure is implemented by the NHSA whereby a Zero is added after every five contiguous One bits during transmit. Inserted Zero bits are removed by the receiver.

While sending a frame, the transmitter examines the bit stream between the beginning and ending Flags. Whenever a sequence of five contiguous Ones is detected, a Zero is inserted into the data stream after the fifth One. Note that this procedure applies to the contents of all fields between Flags, which includes the last five bits of the FCS.

The receiver continuously monitors the received bit stream between Flags. When five contiguous Ones are detected followed by a Zero, the Zero is removed. (If a One follows the five contiguous Ones, then the receiver is in the process of receiving either a Flag or Abort sequence, but which of these it is cannot be determined until the next bit is received.)

2.3.2 Fields of The Frame

2.3.2.1 Flag Sequence

The Flag sequence is an eight-bit sequence (01111110) which delimits the beginning and end of each frame, and is used as a synchronization character. When contiguous frames are transmitted, a single Flag may serve as both the closing Flag for the first frame and the opening Flag for the second. Flags may also be used as Inter-frame time fill.

The transmitter generates opening and closing flags at the appropriate time. During idle periods between frames, Flag, Idle or Abort sequences (as determined by the TIFM bit in the NHSA configuration register) are generated and transmitted. The receiver recognizes Flag sequences as opening or closing Flags or as interframe time fill, but does not transfer them to the NMLC.

2.3.2.2 Address Field

The Address field (containing the secondary station link address) directly follows the opening Flag and normally consists of one eight-bit byte. Optionally for extended addressing, this field may contain multiple octets. In this case all octets in the field except the last will have a Zero in their Continuation bit position.

The specification as to whether or not extended mode applies is under program control and must be set up by prior agreement between the transmitting and receiving stations.

Transmitted Address field bytes must be program generated and transferred like data to the NHSA for transmission. Received Address field bytes may be input to the main frame's memory as part of the data block or may be discarded by the receiver CCP.

2.3.2.3 Control Field

The Control field (containing commands or responses, and sequence numbers) directly follows the A field, and normally consists of one octet. In the optional extended Control field mode, a second octet follows the first. The first bit of the octet (i.e., the low order bit, bit 7) (first octet if in extended mode) provides information about the format of the remainder of the frame. When a Zero, it indicates the frame is in Information Transfer format. When a One, it indicates the frame is in Supervisory format or Non-Sequenced format.

The specification as to whether or not extended mode applies is under program control and must be set up by prior agreement between the transmitting and receiving stations.

Output Control field bytes must be program generated and transferred as data to the NHSA for transmission. Received Control bytes may be input to the main frame memory as part of the data block or may be handled by the receiver CCP.

2.3.2.4 Information Field

The optional Information field directly follows the C field. This field may contain any number of text characters (including none at all). The Information field ends with the start of the FCS field which occupies the 16 or 32 bits prior to the next flag. All data in the Information field is in 8-bit bytes.

None of the data in this field is of significance to the NHSA. Under control of the CCP all of the data in this field is transferred between the NHSA and main memory.

Output text data must be program generated and transferred to the NHSA for transmission. When the CCB range is exhausted, the CCP sets an indication in the NHSA which causes it (after transmitting the last data character and the CRC residue) to generate and transmit the closing Flag.

Input text data is input to the main frame memory as part of the data block. Recognition of the closing Flag by the NHSA causes it, after handling the last data character and the CRC residue, to signal the completion of the frame to the CCP. The FCS and closing Flag are not transferred to the main frame memory.

2.3.2.5 Frame Check Sequence

All frames include, for error detection purposes, a 16 or 32 bit frame check sequence just prior to the closing flag. An algebraic procedure based on a modulo 2 division process using a generation polynomial is used to generate and check the FCS.

At the transmitter, the initial remainder of the division is set to all Ones. This initial remainder is then modified by division by the generator polynomial. This division is performed on the contents of the Address, Control, and Information fields, excluding Zero bits inserted for transparency. When these fields have completed the division process, the One's-complement of the resulting remainder is transmitted (high order bit first) as the FCS.

At the receiver the initial remainder is preset to all Ones, and the same division process takes place on the serial incoming bits. All bits between the opening and closing flag are included, except Zero bits inserted for transparency. In the absence of transmission errors, the final remainder for the CCITT FCS is 1111000010111000 LSB to MSB in reading from left to right.

The CCITT generation polynomial is $X^{16} + X^{12} + X^5 + 1$. The adapter has the capability to generate and check this FCS. A 32-bit FCS may also be used; however, this FCS must be generated and checked by the NMLC using the CCH instruction.

The CCITT checking polynomial for output (transmit) frames may be automatically generated during transmission of the A, C and I fields. When transmission of these fields is complete, the FCS is appended to the end of the frame before the closing flag is transmitted.

Similarly, when receiving a frame, the necessary operations may be automatically performed on the incoming data stream. When the ending Flag is received, the generated remainder is compared with the correct remainder for an errorless transmission. The result of this comparison is made available to the programmer as part of the interrupt status.

2.3.3 Order of Bit Transmission

The Flag, Address, Control, and Information fields are transmitted Least Significant Bit (LSB) first. The FCS is transmitted Most Significant Bit (MSB) first.

2.3.4 Abort

Abort is the procedure by which a station in the process of sending a frame ends the frame in an unusual manner such that the receiving station will ignore the frame.

On transmit, the NHSA will automatically send an abort of eight Ones on underrun. On receive, a sequence of seven Ones will be detected as an abort.

2.3.5 Transparency

HDLC/SDLC provides transparency for data coded in the information field. The occurrence of the flag sequence within the frame is prevented via a "Zero bit insertion" technique.

The transmitter inserts a Zero bit following five contiguous One bits anywhere between the beginning and ending flag of a frame. The receiver continuously monitors the received bit stream. Upon receiving a Zero bit followed by five contiguous One bits, the receiver inspects the following bit. If a Zero, the five One bits are passed and the Zero bit is deleted. If the sixth bit is a One, the receiver inspects the seventh bit. If the seventh bit is a Zero, a flag has been received; if a One, an abort sequence has been received.

2.3.6 Interframe Time Fill

The NHSA is capable of sending either flag sequences or continuous Ones between frames under control of the CCP.

2.3.7 Intraframe Time Fill

The HDLC/SDLC protocol does not provide for intraframe time fill. All bytes within a frame are contiguous.

2.3.8 Idle Link State

The transmission of fifteen or more contiguous One bits on a link constitutes an Idle Link State on the link. Idle Link State may be used in Normal Response Mode (NRM) and in SDLC operation to indicate a need for line turnaround. The NHSA provides for both transmission and detection of Idle Link State.

III FUNCTIONAL DESCRIPTION

3.1 BASIC FUNCTIONS

The HDLC/SDLC Line Adapter (NHSA) supports two bit-synchronous clocked data communication lines. Each line supports either half or full duplex data transmission.

The NHSA accommodates bit-synchronous protocols up to 19.2K bits per second via a bit serial DTE/DCE interface.

All characters are 8 bits only.

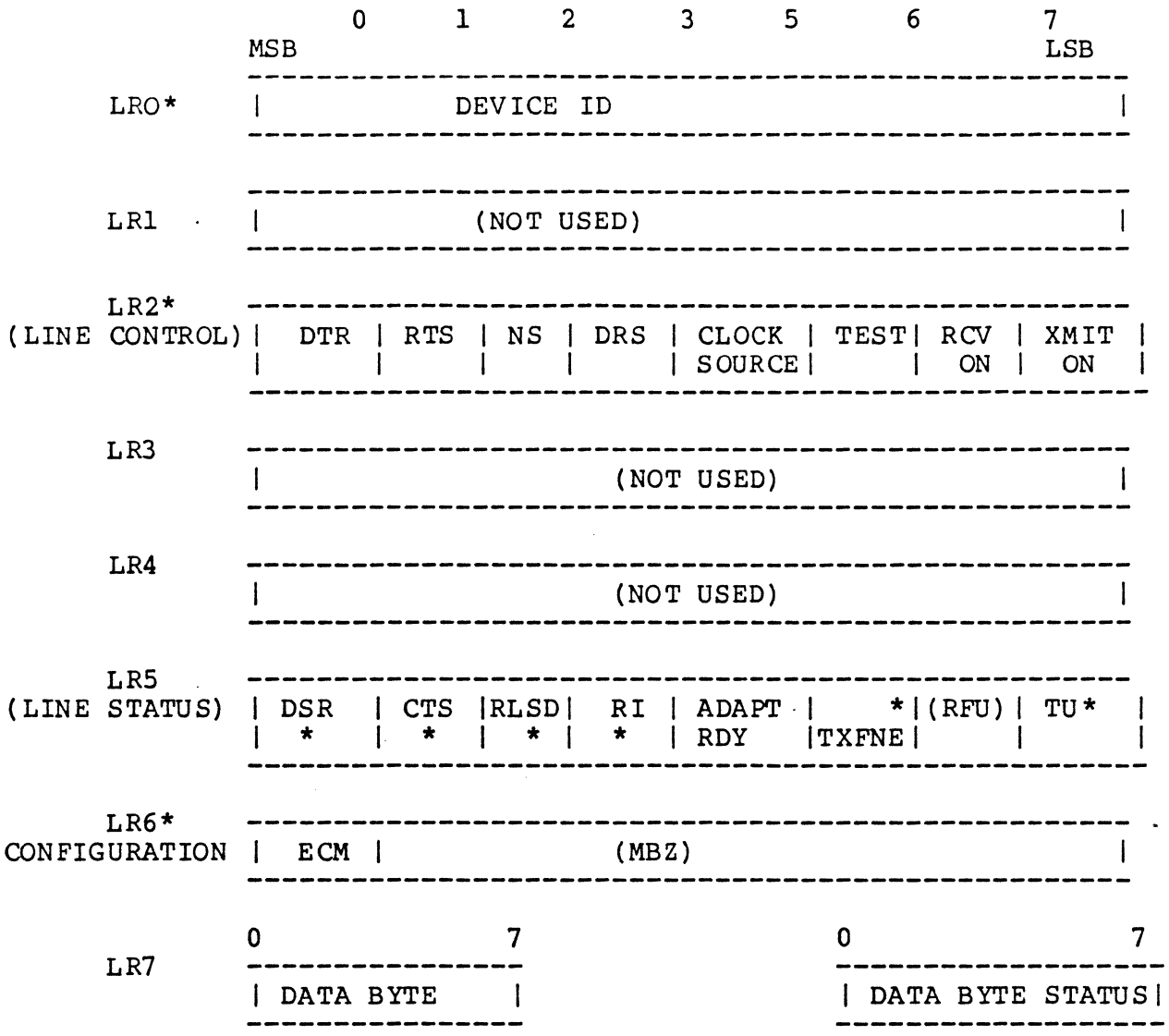
All configuration fields are programmable via the NMLC.

3.2 REGISTERS

Each channel of the two supported lines of the NHSA is controlled and programmed via a set of Registers.

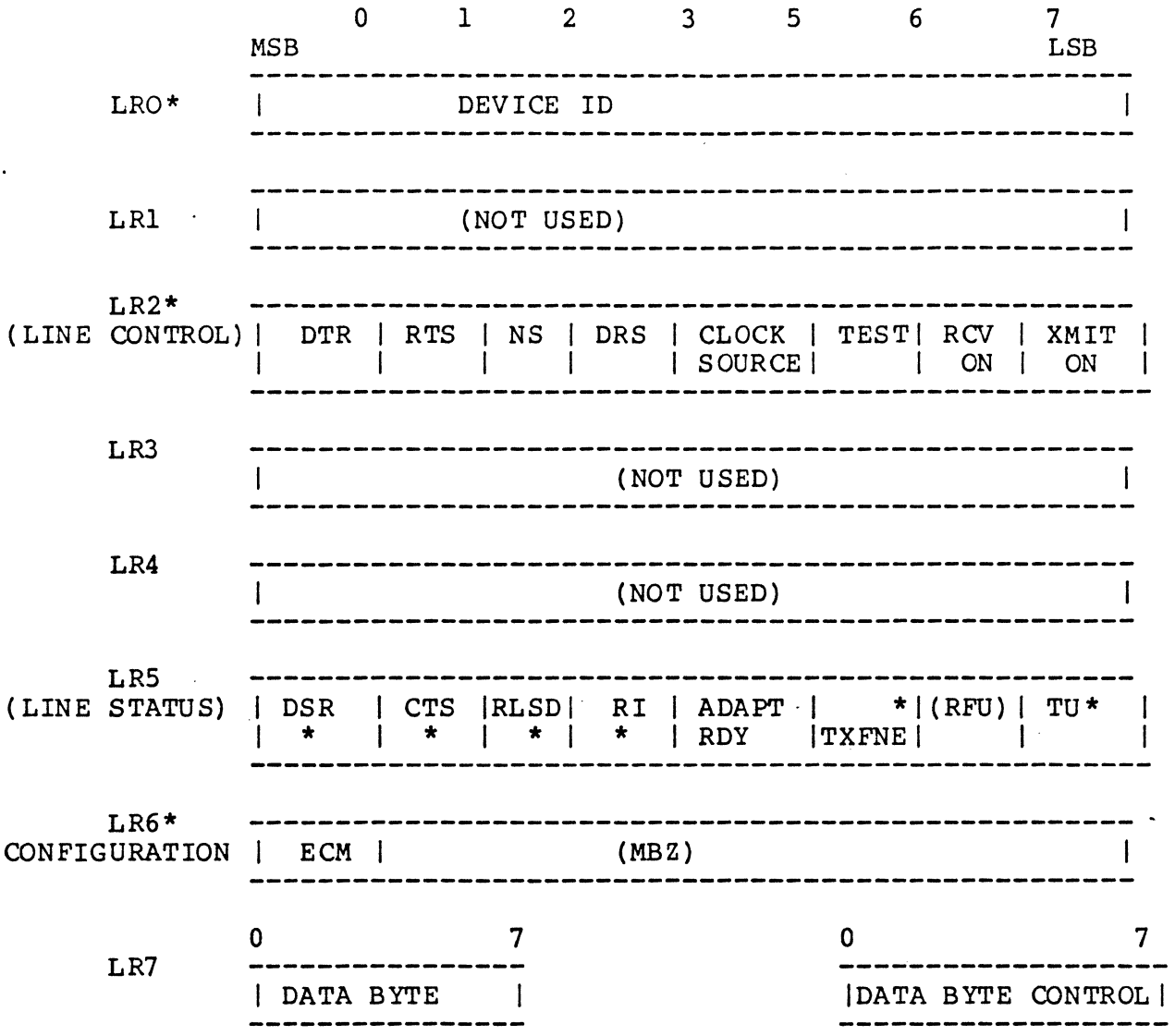
The format of these registers is shown in Figures 3-1 through 3-4.

Note that RECV and SEND instructions may not be used with the NHSA.



* COMMON TO BOTH CHANNELS OF THE SAME LINE.

Figure 3-1 NHSA LR Registers (Receive Channel)



* COMMON TO BOTH CHANNELS OF THE SAME LINE.

Figure 3-2 NHSA LR Registers (Transmit Channel)

3.2.1 Receive Channel LR Register Definitions

All formats shown below follow the same data format and bit positions as the NBHSA.

a) LRO. For LRO usage, see subsection 3.16.

b) LR2. Line Control - This register can only be written by the NMLC. LR2 for the even (receive) channel is the same physical register used by the odd (transmit) channel. Thus a transmit LR2 change also changes the receive LR2 and vice versa.

LR2

0	1	2	3	4	5	6	7
DTR	RTS	NS	DRS	CLOCK SOURCE	TEST	RCV ON	XMIT ON

DTR = Data Terminal Ready, CCITT circuit 108.
RTS = Request to Send, CCITT circuit 105.
NS = New Signal, CCITT circuit 136.
DRS = Data Rate Selector, CCITT circuit 111.

CLOCK SOURCE = This bit is used to select whether an external (Modem) clock or an Internal (NMLC provided) clock is to be used for the line's serial interface. (In the NBHSA EPS-1 this bit is referred to as a Direct Connect bit).

- 0 = External Clock
- 1 = Internal Clock

TEST = Test line on NHSA by enabling test clock and looping transmit data back to the receive side.

- 0 = No Action.
- 1 = Loop-back at test clock frequency.

RCV On = Receive On for this line:

- 0 = Receiver Off and inactive
- 1 = Receiver On. Channel Request Interrupts will be sent to the NMLC.

XMIT ON = Transmitter On for this line:

- 0 = Transmitter Off and inactive
- 1 = Transmitter On. Channel Request Interrupts will be sent to the NMLC.

c) LR5. Line Status - LR5 is used for status purposes by both channels and should only be read.

LR5

0	1	2	3	4	5	6	7
DSR	CTS	RLSD	RI	ADAPT RDY	TXFNE	(RFU)	TU

DSR = Data Set Ready
RLSD= Receive Line Signal Detector
RI = Ring Indicator

ADAPT RDY = Adapter Ready. When this bit is a ONE, it indicates that the Receiver is not empty (i.e., contains information for the NMLC).

CTS = Clear to Send. Allows the transmit USRT to serialize and transmit data which is delivered to it.

TU = Transmit Underrun. See transmit channel LR5.

TXFNE = Transmit FIFO Not Empty, see Transmit channel LR5.

d) LR6. Configuration - This LR can only be written into by the NMLC.

LR6

0	1	7
ECM	(MBZ)	

ECM = Error Control Mode. Specifies if the CRC checking facilities of the adapter are to be used.

1 = OFF
0 = CCITT 16 bit CRC

e) LR7. Data and Data Status - Reading LR7 accesses the receive data and the associated data status information. The IN LR7 instruction causes the Data Status byte to be placed in LCT11 and the Data byte to be delivered to R. The NMLC indicators are set according to the contents of the Data Status. The format of the Data Status byte is as follows:

LR7

0	1	2	3	4	5	6	7
FCSE	RILS	0	0	RO	RAB	REOM	0

RAB = Receive Abort. When this bit is a One and REOM is a One it indicates that the frame was terminated with an Abort Sequence of seven or more Ones.

RO = Receive Overrun. When this bit is a One it indicates that the NHSA was not serviced fast enough and one or more characters or frames in the NHSA data path have been overwritten and lost. The frame will have been terminated by the NHSA and REOM will also be set.

RILS = Receive Idle Link State. When this bit is a One, it indicates that fifteen or more Ones have been received and the input line is in an Idle Link state.

FCSE = Receive Frame Check Sequence Error. When this bit is a One it indicates that the frame was received in error (CRC check failed). This bit is normally Zero and has a valid meaning only when REOM, is also set.

REOM = Receive End of Message. When this bit is a One it indicates that the frame was terminated. The associated data byte in R is the last byte of the frame.

3.2.2 Transmit Channel LR Register Definitions

a) LRO. For LRO usage, see subsection 3.16.

b) LR2. Line Control - This register can only be written into by the NMLC. This is the same physical register as used by the receive channel of the same line.

LR2

0	1	2	3	4	5	6	7
DTR	RTS	NS	DRS	CLOCK SOURCE	TEST	RCV ON	XMIT ON

Definitions are the same as LR2 Receive.

c) LR5. Line Status - This LR can be read by but not written into by the NMLC. The same register is accessed by both channels.

LR5

0	1	2	3	4	5	6	7
DSR	CTS	RLSD	RI	ADAPT RDY	TXFNE	(RFU)	TU

DSR, CTS, RLSD AND RI Definitions are the same as in LR5 Receive.

ADAPT RDY = Adapter Ready. When this bit is a One it indicates that the transmitter can accept information from the NMLC) and there is no Transmit Underrun condition present.

TU = Transmitter Underrun. When this bit is a One, it indicates that the CCP did not service the transmitter fast enough and the NHSA aborted the frame. The bit is reset by setting TSOM in LR7.

TXFNE = Transmit FIFO Not Empty. When this bit is a Zero the Transmit buffer has been emptied. See subsection 3.4.

d) LR6. Configuration - This LR can be written into by the NMLC. The same register is accessed by both channels of the line.

	0	1	7
LR6	ECM	(MBZ)	

ECM = Error Control Mode. Specifies if the CRC generation facilities of the adapter are to be used.

1 = OFF
0 = CCITT 16-bit CRC

e) LR7. Data and Data Control - Writing LR7 delivers the transmit data and data control information to the adapter.

The OUT LR7 instruction causes the Data byte in R and the Data Control byte in LCT43 to be delivered to the adapter.

The format of the Data Control byte is as follows (note that only one bit at a time can be set in this byte):

	0 1 2	3	4	5	6	7
LR7	0 0 0	TILS	TFLG	TAB	TEOM	TSOM

TSOM = Transmit Start of Message . This bit is to be set to One in LCT43 by the CCP before it outputs the first character of the frame to the adapter. The Data Byte which is the first character of the frame (an address character) will thus have this bit set in the associated control byte. When sensed by the adapter, this bit causes the TU bit in LR5 to be reset and the CRC generation facilities in the adapter are initialized for generation of a new CRC.

TEOM = Transmit End of Message. This bit will be set to One in LCT43 by the CCP before it outputs the last data character of the frame to the adapter. When sensed by the adapter, this bit causes the transmitter to begin end of Frame sequence as described in subsection 3.7.10.

TAB = Transmit Abort. When this bit is a One it indicates that the frame is to be terminated with an Abort sequence and the remaining data bytes and FCS are not transmitted.

TFLG = Transmit Flag. This bit may be set in message control bytes following one in which TEOM was set. Message control bytes in which this bit is set must each be preceded by a data byte (R register); the particular character code used in these data bytes is immaterial. Each occurrence of a TFLG control byte will cause the adapter to generate and transmit one Flag character. This function may be used to provide a specific number of Flags between messages or as a means of insuring that the USRT has completed transmission of a message before the transmitter is turned off.

TILS = Transmit Idle Link State. When this bit is set to a One the line is placed in an Idle Link state by transmission of at least 15 Ones.

3.2.3 Adapter Control & Status Registers

	0 4	5	6	7
Adapter Control Register	(MBZ)	TEST	RCV ON	XMIT ON

This register is written into via the ACTL instruction. Bit definitions are the same as for LR2.

	0 3	4	5	6	7
Adapter Status Register	(RFU)	ADAPT RDY	TXFNE	(RFU)	TU

This register is read via the AST instruction. Bit definitions are the same as for LR5.

Figure 3-3 NHSA Adapter Control & Status Registers

3.2.4 NHSA FR Register Definitions

	0	1	2	3	4	5	6	7
FR0	ALL ZEROS							
FR1	NOT USED							
FR2	DTR	RTS	NS	DRS	NOT USED			
FR3	NOT USED							
FR4	NOT USED	CLOCK SOURCE	NOT USED		LL		RL	NOT USED
FR5	DSR	CTS	RLSD	RI	NOT USED		TM	NOT USED
FR6	NOT USED							
FR7	NOT USED							

Figure 3-4 NHSA FR Registers

LL = Local Loop. Provides loopback at the local DCE.
RL = Remote Loop. Provides loopback at the remote DCE.
TM = Test Mode. Indicates that the local DCE is involved in loop testing.

All other bits are the same as similarly-named bits in the LRs.

3.3 REGISTER TRANSFER

The NHSA and the NMLC exchange program visible data, configuration, and status via reference to the registers (see subsection 3.2). The registers are accessed through the NHSA/NMLC interface (see subsection 3.14).

The LR numbers correspond with the LR numbers of the NMLC instruction set.

3.4 DATA TRANSFER

The NHSA and the NMLC exchange parallel data elements on a channel basis through register LR7. The NHSA converts parallel data to bit serial data for transmission, and converts bit serial data to parallel data on receive. Each channel must contain data buffers in addition to a serial input or serial output buffer. The Adapter Ready Bit (LR5, bit 4) indicates the state of the channel parallel buffer. The receive buffer is cleared on transition from REC OFF to REC ON (LR2, bit 6).

On transmit, the NHSA will begin transmission with the first character output to the transmit buffer if the Xmit on bit (LR2, bit 7) is set. If Xmit On is not set, the NHSA will allow character to be output and stored in the output buffer until Adapter Ready is reset.

In order to assure that all characters delivered to the adapter have been transmitted on the line before turning off the transmitter, the CCP should allow for at least three character transmission times after TXFNE becomes a Zero.

The channel request interrupt (see subsection 3.10) provided for each channel is used to co-ordinate with the NMLC when a character may be passed to or from the NMLC controller.

3.5 DATA ELEMENTS

Data elements are always 8 bits in size.

3.6 REDUNDANCY AND PARITY

Cyclic redundancy checks (the Frame Check Sequence) may be generated and checked by the NHSA for each channel.

3.7 OPERATION

3.7.1 Receive Startup and Frame Synchronization

When receive operation from the DCE is desired, the CCP will load LR2 or the Adapter Control register with appropriate information. This connects the DCE to the receive CLA and the receiver begins shifting in serial data bits from the DCE at a rate determined by the DCE receive clock.

As each bit is shifted in, the receiver examines that bit and the seven preceding bits in search of a Flag sequence (01111110). Once a Flag is detected, the receiver has achieved frame synchronization; thereafter the receiver inspects each received octet for a non-Flag or non-Abort sequence. If additional Flags are received, synchronization is maintained; if an Abort (a sequence of seven contiguous Ones) is found, synchronization is lost and must be reestablished.

When, in synchronization, a non-Flag, non-Abort octet is received it is shifted further into the receiver as a byte.

3.7.2 Receive Data Transfers and Receive Overrun

Each data byte received after the Flag is loaded in LR7 by the Adapter. It also sets associated receive status information into LR7. The act of loading into LR7 causes the adapter to send a Channel Request Interrupt (CRI) to the NMLC. The ADAPT RDY would then also become a One at this time, indicating the presence of information.

The receive loop CCP performed by the NMLC removes each character by reading LR7. ADAPT RDY will switch to Zero state when this is done.

Receive overrun will occur if the adapter overflows due to failure of the CCP to unload characters soon enough. If overrun in a frame occurs, RO and REOM are set in LR7 and the remainder of the frame is discarded in the adapter. The RO bit results in the CCP becoming aware of the overrun at the point in the message stream at which it occurred. The condition is reported to software which takes further action. The CCP will then read LR7 thus allowing the next frame to be read by the NMLC.

3.7.3 Receive End of Frame

The data shifting, assembling, and LR7 load and unload process continues until a Flag or Abort sequence is detected by the adapter, denoting end of frame.

In the case of an Abort, the adapter sets ABORT and REOM in LR7. No further loading occurs until synchronization is reestablished and a new frame begins to be received; it will then be loaded into LR7 in the usual manner. The Abort bit results in the CCP becoming aware of the Abort at the point in the message stream at which it occurred. The condition is reported to software which takes further action. The CCP will then read LR7 allowing the next frame to be read by the NMLC.

In the case of a normal frame termination by a Flag sequence, the adapter sets REOM in LR7. It also sets the result of the FCS residue check into FCSE. The last character of the frame is then loaded in LR7. If another frame follows after the Flag, the adapter will proceed to load this. The REOM bit results in the CCP becoming aware of the end of frame at the proper point. The CCP tests the FCSE bit of LR7, passing this information on to software; it then reads R to obtain the last character of the frame, thus preparing to receive the next frame.

3.7.4 Receive Idle Link State

The input line is defined to be in the Idle state when a sequence of fifteen or more Ones are received. This event causes the adapter to report RILS into LR7. Succeeding action is similar to the Abort case except that, since there is no more data, the adapter will become empty, ADAPT RDY will remain Zero and the CCP will remain in a Wait condition.

3.7.5 Receive Missing Frame State

A Missing Frame State occurs if the overrun situation becomes so severe that entire frames are discarded in the adapter. This situation is detected by software as it performs sequence number checks on received frames.

3.7.6 Minimum Receive CCP Structure

A minimum receive loop CCP is shown in the Broadband HDLC adaper EPS-1 (60144541).

3.7.7 Transmit Initialization

Transmit operation is initialized by a CLA Master Clear from the NMLC. Bits in LR2 are set to an OFF state effectively disconnecting the DCE interface.

3.7.8 Transmit Startup

When transmit operation to the DCE is desired, the NMLC CCP will load LR2 or Adapter Control registers with appropriate information. This connects the DCE to the transmit CLA and the transmitter begins sending Flag sequences.

Assuming that XMIT ON is set, the transmitter generates a Channel Request Interrrupt and sets Adapter Ready to True state. As soon as the adapter contains data, the transmitter generates and transmits a Flag and then begins transmitting data.

3.7.9 Transmit Data Transfer and Transmit Underrun

Each data byte sent by the NMLC is loaded into R and an associated Message Control byte is placed in LCT43.

The transmit loop CCP performed by the NMLC load characters (including message control) into LR7 as long as Adapter Ready is True. The adapter will send a CRI to the NMLC whenever Adapter Ready switches from False to True.

Transmit Underrun will occur if the adapter underflows due to failure of the CCP to load it soon enough. If underrun occurs the transmitter generates and sends an Abort sequence followed by Flags. It continues to request data from the NMLC but does not transmit it to the line. When the TEOM bit is set, the CCP should read LR5 or Adapter Status and test TU and, finding it True, branch to its underrun handling routine. On completion of this routine, the CCP starts the next frame and sets TSOM; the adapter senses this and clears its internal stored underrun condition. If XMIT ON is still True, normal startup of the next frame ensues.

Underrun is a fatal error to the frame from a procedural aspect.

3.7.10 Transmit End of Frame

The data load and unload, disassembly, serial shifting and CRC calculation continues until a Last Character (and Last Block) condition is detected by the CCP. The CCP then loads a One into the TEOM bit of LCT43. It does this before sending the last character to the adapter. When the TEOM bit is sensed, the adapter transmits the last character, the CRC residue (FCS sequence), and then transmits a Flag. If the CCP wishes to proceed with the next frame, it loads LR7 with the appropriate frame specification, gets the next block and proceeds to deliver data to the adapter. Until this data is ready and TRANSMIT ON allows its transmission, the adapter will send interframe fill characters.

3.7.11 Minimum Transmit CCP Structure

A minimum transmit loop CCP is shown in the Broadband HDLC Adapter EPS-1 (60144541).

3.8 STATUS

The status for channels is provided in LR5 and Data Status in LR7. Status includes Data Set status, Closing flag, Abort, Receive Overrun, Transmit Underrun, Receive FCS Error, Receive Idle Link and Adapter Ready.

3.9 DATA CLOCK

In most applications for the NHSA, the Data Clock is provided through the DTE/DCE interface from the DCE. This is called the external clock. Each channel has independent clock control such that it may transfer data at a different rate than the other channel, as determined by the DCE.

In the case where a Direct Connect to a terminal or to another NHSA is desired (no DCE and no external clock), a Direct Connect capability can be provided. The clock in this case is provided through the NMLC/NHSA interface. The selection between external or internal clocking is made according to the Clock Source bit in LR2.

3.10 CHANNEL REQUEST INTERRUPT PRIORITY

Each channel is individually capable of generating a Channel Request Interrupt (CRI) which signals a requirement to the NMLC that the channel be serviced. In the NHSA, all CRIs are caused by a need for service.

Once it has begun servicing the adapter as a result of a CRI, the CCP senses the state of Adapter Ready and continues to send/accept characters as long as Adapter Ready is True.

In the receive case, Adapter Ready means that the adapter has data and/or status not yet taken by the NMLC.

CRIs are also controlled on a line basis through the RCV ON and XMIT ON bits in LR2. If RCV ON is reset, the receiver will not generate CRIs. If XMIT ON is reset, the transmitter will not generate CRIs.

The NHSA signals a need for receive or transmit data service to the NMLC as a high priority CRI for its adapter location. Within the adapter, the receive channel is given service preference over the transmit channel.

3.11 CHANNEL NUMBER ASSIGNMENT

The NHSA supports use of the two highest order line numbers of the group associated with its adapter board location:

	ADAPTER BOARD LOCATION			
	0	1	2	3
Receive Channel	4, 6	12, 14	20, 22	28, 30
Transmit Channel	5, 7	13, 15	21, 23	29, 31

The two lowest order line numbers of the group associated with its adapter board location are not useable (NULL).

3.12 CONFIGURATION

The configuration of the NHSA is established through the LRs and are both visible to and controllable from the NMLC. An initial configuration setup must precede actual operation.

3.13 TEST

Each line in the NHSA has a software controlled internal test mode which internally loops back data from the transmit channel to the receive channel. This test is possible regardless of whether a DCE device or device cable is attached.

Internal test mode is invoked by setting the TEST bit in LR2. The Clock Source used for internal test mode is determined by the Clock Source bit in LR2. In internal test mode a continuous string of ones is sent on the DCE interface.

Local or remote loopback through the local or remote DCE can also be performed (if the DCEs support this capability) by setting the appropriate bit in FR4.

3.14 NMLC/NHSA INTERFACE

The interface is defined in the NMLC EPS-1.

3.15 DIRECT CONNECT

An internal clock for Direct Connect applications is provided for the NHSA by the NMLC. The clock may also be used during internal Test mode. Clock speeds are given in the NMLC EPS-1.

3.16 DEVICE IDENTIFICATION NUMBER

The basic identification number is furnished by the NMLC without reference to the presence or type of adapter attached to it. This identification number is given in the NMLC EPS-1.

On line numbers which support data transfer, the extended device identification number provided by the NHSA is (5900)16. If the adapter is inoperable on these lines, the highest order bit of the Extended Device ID will be forced to a One, resulting in an ID of (D900)16.

On NULL line numbers, the extended device identification provided by the NHSA is $(0300)_{16}$.

The contents of LRO correspond to the two high order digits of the Extended Device ID.

IV INTERFACES

4.1 NMLC/NHSA INTERFACE

The NMLC/NHSA provides for the control of data transfer between the NMLC and the NHSA. See NMLC EPS-1 60131665 for explicit definition of the signals involved.

4.2 DCE INTERFACE

The pin assignments on the 25 pin connector to the DCE are as shown in Figure 4-1.

PIN NO.	TYPE	ITCHG CKT	CCITT EQUIV	CIRCUIT DESCRIPTION NAME	DIRECTION
1	COMMON	AA	101	SHIELD GROUND	--
2	DATA	BA	103	TRANSMITTED DATA	TO DCE
3	DATA	BB	104	RECEIVED DATA	FROM DCE
4	CONTROL	CA	105	REQUEST TO SEND	TO DCE
5	CONTROL	CB	106	CLEAR TO SEND	FROM DCE
6	CONTROL	CC	107	DATA SET READY	FROM DCE
7	COMMON	AB	102	SIGNAL GROUND/COMMON RETURN	--
8	CONTROL	CF	109	RECEIVED LINE SIGNAL DETECTOR	FROM DCE
9					
10					
11					
12					
13					
14	CONTROL	NS	136	NEW SIGNAL	TO DCE
15	TIMING	DB	114	TRANSMITTER SIGNAL ELEMENT TIMING (DCE)	FROM DCE
16					
17	TIMING	DD	115	RECEIVER SIGNAL ELEMENT TIMING	FROM DCE
18	CONTROL	LL	141	LOCAL LOOPBACK	TO DCE
19					
20	CONTROL	CD	108	DATA TERMINAL READY	TO DCE
21	CONTROL	RL	140	REMOTE LOOPBACK	TO DCE
22	CONTROL	CE	125	RING INDICATOR	FROM DCE
23	CONTROL	CH	111	DATA SIGNAL RATE SELECTOR	TO DCE
24					
25	CONTROL	TM	142	TEST MODE	FROM DCE

Figure 4-1 DCE Connector Pin Assignments

V PERFORMANCE

5.1 HARDWARE CAPABILITY

Each channel of the NHSA is capable of operation at up to 19,200 bits per second.

The NHSA is capable of simultaneous operation on all of its channels.

5.2 LIMITATIONS IMPOSED BY THE NMLC

The timing requirements of the Channel Control Program (CCP) loops, used in the NMLC to service each character for the NHSA, impose limits upon performance. Thus, the second item of subsection 5.1 above may be constrained by NMLC performance. See NMLC EPS-1 60141665 for further details.

VI PHYSICAL STRUCTURE

6.1 MECHANICAL SPECIFICATIONS

The NHSA is packaged on a quarter-sized daughter board.

The NHSA will connect to its DCE via either Honeywell supplied cables or customer supplied cables which conform to the electrical characteristics of the Honeywell cable. The Honeywell cable will be documented in length as determined by Marketing and the BCO Program Office. RS232C interfaces are limited to 50 feet maximum distance.

6.2 ENVIRONMENT

The NHSA will be capable of operating in the normal environment experienced inside the Level 6 cabinetry as specified in the EPS-1 for NML System, 60126448.

6.3 POWER

The NHSA requires the following power which it draws through the NMLC to which it is attached:

- 0.892 amp at +5 vdc
- 0.059 amp at +12 vdc
- 0.073 amp at -12 vdc

6.4 SAFETY

The NHSA itself meets the Underwriter Laboratories and Canadian Standards Association requirements.

6.5 AMBIENT CONDITIONS

- Temperature: 10° to 50°C
- Humidity: 5% to 90%.

6.6 HIS STANDARDS

The NHSA will meet all applicable referenced HIS standards.

6.7 TESTABILITY

The NHSA will conform to the testability requirements listed in subsection 1.2.

6.8 RFI ELIMINATION

The NHSA will comply with the requirements of Part 15 of Federal Communications Commission Rules for Class A computing device when mounted in a standard L6 chassis.

VII RELIABILITY AND MAINTAINABILITY

7.1 GENERAL REQUIREMENTS

1. Mean Time Between Failures (MTBF): 404,000 hours.
2. Mean Time to Repair (MTTR): 20 minutes maximum for NHSA; one hour for overall system repair.
3. The NHSA is an ORU.
4. HIS Communications Standards must be observed.
5. The NMLC ORU Isolation Test Routine must support failure diagnosis and replacement of the NHSA.

7.2 MAINTENANCE FEATURES

7.2.1 Loopback Methods Possible

The NHSA has several loopback capabilities, both manual and under program control. These are listed in order of increasing amount of hardware checked. By utilization of these loopback capabilities, the isolation of failed components is enhanced.

- Internal Loop - The NHSA has a software controlled internal test mode which internally loops back data from the transmit channel to the receive channel.

Setting the TEST bit on the transmit or receive channel LR2 will invoke the test mode. During test mode, the data rate will be determined by the NMLC. (Assuming that the Clock Source bit in LR2 is also set to Internal Clocking).

- Loopback check of all hardware including adapter transmitter and receiver by the manual connection of a wraparound plug to the DCE bulkhead connector.
- Loopback of all hardware including the DTE/DCE cable by the manual connection of a wraparound plug to the DCE end of the DTE/DCE cable.
- Local loopback through the local DCE under software control using the LL bit in FR4. (Assuming that the DCE supports this).
- Remote loopback through the remote DCE under software control using the RL bit in FR4. (Assuming that the DCE supports this).

7.3 SOFTWARE VERIFICATION OF HARDWARE CHECKS

By use of suitable CCPs and using a loopback mode, it is possible to deliberately create underrun or overrun, thereby verifying correct operation of the NHSA hardware detection circuits.

7.4 ERROR CHECKING

Checks are made in the NHSA for underrun and overrun, Parity error, etc., and are reported to the NMLC's CCP for appropriate action.

7.5 MAINTAINABILITY

It is a design goal that, through a combination of the tests below and use of the maintenance features of the NHSA, 93% of failures of the NMLC system can be isolated to the motherboard-adapter ORU pair.

- QLT
- T&V routines

VIII INTERNATIONAL MARKET REQUIREMENTS

8.1 POWER

The NHSA uses dc power only and is therefore not affected by main power frequency and voltage requirements.

8,.2 INTERNATIONAL STANDARDS

The NHSA provides the necessary hardware support, for conformance with the following CCITT recommendations as they apply to bit oriented synchronous data formats:

V.24, X.1, X.2, X.21 bis, X.25

Note that full support of certain of these recommendations is contingent upon appropriate software.

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