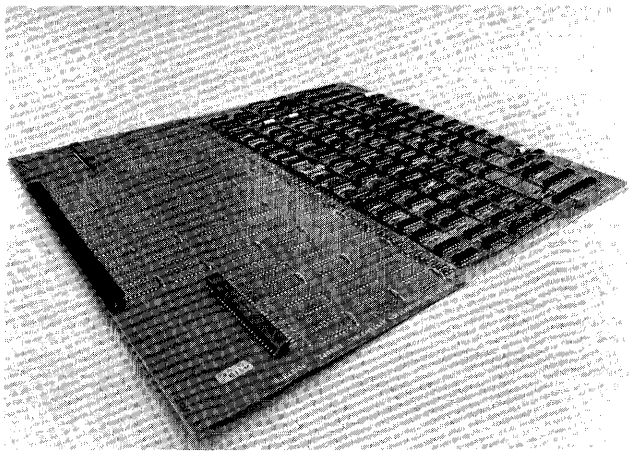
Honeywell

SERIES 60 (LEVEL 6)

GIS9001 General Purpose Direct Memory Access (DMA) Interface

The General Purpose Direct Memory Access (DMA) Interface (GIS9001) offers users of the 6/30 Models the added capability and flexibility of interfacing special devices to Level 6. Completely contained on one board is all the necessary interface circuitry, storage, and control logic required to maintain functionality with the system Megabus. It is designed for the user who wants to extend the capabilities of his Level 6 system or tailor it to special applications.

The General Purpose DMA Interface (GPI) is divided into two distinct areas: an area containing fixed logic providing bus and user interfacing and an area reserved for user-supplied logic. The GPI operates in Direct Memory Access (DMA) mode and supports a single bidirectional channel. Data to/from the user area is transferred in 16-bit parallel form, controlled by a simple, asynchronous handshake operation. Data transfer between the GPI and the Megabus is also in 16-bit parallel form via DMA control. The data transfer rate from memory to user device (or in the opposite direction) is 500K words per second/1000K bytes per second.



FEATURES

- Single, compact 15" x 16" board contains GPI-logic area and user-logic area
- Operates in DMA mode supporting a single bi-directional channel
- Provides intermediate data buffering for both input and output operations
- 66 DIP sites for user-specified logic and two 56-pin connector receptacles for attaching cables to user devices
- Twelve 16-bit user-specific registers available
- 70 wirewrap pins provide GPI logic area to user logic area interface signals
- Provides CP interrupt capability
- Software isolation test routines enable quick, effective fault diagnosis

COMPONENTS

The General Purpose DMA Interface is comprised of the following:

- *Megabus I/F Circuits* – provide the necessary electrical characteristics (level, impedance, noise immunity) required of all units connected to the Megabus.
- *Scratchpad Memory* – a 16-bit by 16-word bipolar memory serving (1) as a temporary data buffer between the Megabus and the user hardware, (2) as a storage area for essential system parameters or control information, and (3) as a reserved area for user implementation.
- *Data Control Logic* – provides control, timing, and monitor signals to the user for the "handshake" operation for data transfers, and also initiates Megabus cycle requests.
- *Interrupt Control Logic* – provides control and monitor signals to the user for generating an interrupt service request.
- *Megabus Cycle Request and Control Logic* – contains all the function decoding for control and access of the scratchpad memory (Megabus side) and response logic for acknowledging, denying, or delaying a response from the General Purpose DMA Interface to the Megabus.
- *Megabus Tiebreak Logic* – resolves simultaneous requests and grants Megabus cycles on the basis of a positional priority system.
- *DMA Address and Range Register* – uses a 24-bit DMA address register to hold the starting address in main memory from which a block of data (contiguous memory locations) will be input or output under DMA control. The address register

is unrestricted, and a block of data may be assigned anywhere in available memory. The range register defines the size (number of words) of data in the block. The maximum value of the range in the GPI is 2^{14} - 1 words.

- *Parity Generation/Check Logic* – generates and checks parity for both data and address information going over the Megabus. Detection of a parity error on incoming data to the GPI from the Megabus sets a parity flag bit in the GPI status word. Similarly, detection of a parity error going in the other direction sets a caution flag that can be examined by the GPI.
- *Loop Test Logic* – allows the GPI to be confidence-tested by performance of DMA transfers in either direction. It also serves to test the interrupt function and task word recognition.
- *User Interface* – consists of 50 signals: 23 from the GPI-logic area to the user-logic area and 27 from the user logic area to the GPI logic area. All interface signals are TTL and available to the user via wirewrap connection.
- *Channel No./Device ID* – validates the unique 10-bit channel number assigned to a GPI. Eight bits are variable via a rotary switch, providing up to 256 possible channel number assignments for a GPI and enabling the configuring of multiple GPIs. It also verifies the unique 16-bit device ID assigned to each device connectable to the Megabus, of which four bits are variable via a rotary switch.

USER LOGIC AREA

The user logic area on the GPI board is populated with 66 DIP sites for mounting 14- or 16-pin DIPs and up to two large (24-pin or 40-pin) DIPs, each of which uses two of the 66 sites available for the smaller DIPs. Two connectors are located in the user area at the front edge of the board to enable the user to connect to remote options if required. Each connector provides 56 pins.

The user logic area communicates with the Megabus via the GPI logic area to user logic area interface. Connection to this interface is via 70 staked wire-wrap pins.

IMPROVED SYSTEM RELIABILITY

A combination of visual indicators and stand-alone isolation test routines is provided to verify all operational aspects of the GPI. Power for attachable user devices is independent of system power, thus enabling the powering down and replacement of failed user devices without affecting system operation in most cases.

SPECIFICATIONS

COOLING: Forced unfiltered air at 125°F maximum ambient at 110 cfm.
POSITION: Can be placed between other Level 6 boards in the chassis on one-inch centers.
USER AREA POWER: +5V @ 3 amps dc
±12V @ 0.2 amps dc
USER AREA DIP SITES: 66
USER AREA INTERFACE SIGNALS: GPI to user area – 23; User area to GPI – 27
INSTRUCTIONS: Input – 15 (9 user-specified); Output – 16 (9 user-specified)
REGISTERS: 16 (12 user-specified, data buffer, task word, interrupt control and status)
MAXIMUM DATA RATE: From memory to user device (or in the opposite direction) 500 KW (1 MB) per sec

Specifications may change as design improvements are introduced.

Honeywell

Honeywell Information Systems
In the U.S.A.: 200 Smith Street, MS 486, Waltham, Massachusetts 02154
In Canada: 2025 Sheppard Avenue East, Willowdale, Ontario M2J 1W5
In Mexico: Avenida Nuevo Leon 250, Mexico 11, D.F.

15264, 7.5376, Printed in U.S.A.