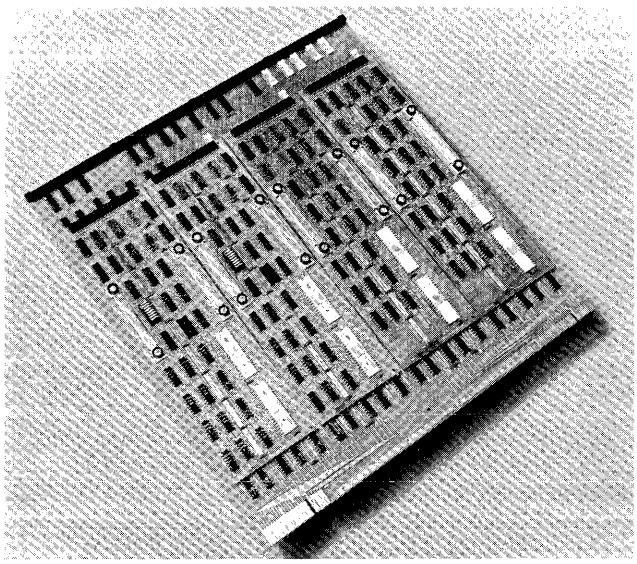
Honeywell

SERIES 60 (LEVEL 6)

MLC9103 Multiline Communications Processor

The MLC9103 Multiline Communications Processor interfaces multiple asynchronous and/or synchronous data communications lines enabling 6/30 Model users to easily plan and implement a powerful data communications system at a reasonable cost. The primary functions of the MLCP are to provide message delimiting, check-character detection and generation, and editing functions to offload the central processor by reducing the amount of processing required.

The MLCP has a maximum throughput rate of approximately 20,000 characters per second and is capable of attaching up to eight, full-duplex low-speed (300 bps or less) and medium-speed (600 to 10,800 bps) lines on a single board using only one bus interface slot. Alternatively, four broadband lines can be attached; within the overall throughput limit, each such line may operate at speeds of up to 72,000 bps.



FEATURES

- Maximum subsystem throughput of 20K characters per second
- User-programmable to provide for message delimiting, message editing, checking of algorithms, etc.
- 3000 bytes of read/write memory for user programming procedures
- Instruction set designed specifically for communications processing (28 instructions)
- Program load of data stream control and configuration data
- Synchronous/Asynchronous Communications-Pacs (1 or 2 lines/Pac)
- Synchronous Broadband Communications-Pac (1 line/Pac)
- Assignment of program interrupt levels dynamically
- Hardware checking (e.g., Cyclic Redundancy Check)
- Individual Direct Memory Access (DMA) for each line and transmission direction
- Channel Control and Status Information (e.g., Underrun/Overrun Protection
- Built-in maintenance aids (e.g., line looping)

OPERATION

The MLCP is responsible for the transfer via the Megabus of data between main memory and the communications lines. The data may be described as a sequential data stream with the MLCP providing the necessary control and transformation of that main memory data into and out of the data formats of the connected lines and terminals.

At the memory side, data is arranged in DMA blocks, and the MLCP supports full DMA data transfers. To minimize block transition timing constraints which may occur because of a busy CP or Megabus, multiple DMA blocks controlled through CCBs (communications control blocks) are provided by the MLCP. These CCBs are user software defined and used by the MLCP to describe address, range, control and status for each block transfer between the MLCP and memory.

At the communications line side, the Communications-Pac (DCM9101/02/03/04/05) provides both

the line interface and parallel/serial conversion of the byte data stream into bit serial form. The MLCP provides control of the line interface, and processes communications data between the Communications-Pac and main memory as required.

As data passes through the MLCP, the MLCP exercises control over the contents and format of the data stream, generating appropriate status, interrupts, and control information. The MLCP also provides, via user-specified software and parameters, message delimiting and editing functions that act upon the data stream.

FLEXIBILITY AND EXPANDABILITY

The MLCP is unusually flexible regarding line types, speeds, communications disciplines, etc. For example, it can simultaneously handle up to eight full-duplex lines at speeds to 7200 bits per second, or it can drive one full-duplex line at 72,000 bits per second without exceeding the maximum throughput rate of 20K characters per second. Its 4096 bytes of Random Access Memory (RAM) – 3000 available to the user and used for its procedure code – permit it to execute complex line handling procedures with no involvement of the central processor.

The microprocessor-based architecture of the MLCP, coupled with the configurability of the Communications-Pacs, provides a highly modular and configurable subsystem. The differences between line protocols and the specific requirements of each Communications-Pac/line combination are handled via small software routines. Each routine is reentrant, can be shared by all lines, and is loaded from an image in main memory by the system operating software. With this system, it is possible to reconfigure lines from one protocol to another by simply changing a parameter or loading a new routine within the MLCP.

IMPROVED RELIABILITY

A portion of the MLCP firmware is reserved for a hardware verification routine called Basic Logic Test (BLT), which supplies a go/no-go visual indication of an MLCP hardware failure. Its purpose is to verify basic data paths so that appropriate software isolation test routines can be loaded and run.

The BLT is invoked in the MLCP in response to a Master Clear on the Megabus or an initialize command (issued by software). Results of the BLT appear as a visual indication on the control panel. An indicator illuminates during execution of the BLT and extinguishes only if the BLT is successfully completed.

Software isolation test routines are provided to verify all operational aspects of the MLCP and to isolate failures. The operator interfaces with these routines via the CP control panel or the CRT display. In addition, each of the eight lines has a programmed loopback of data transmit to data receive which facilitates diagnosis.

OPTIONS

- DCM9101 – Asynchronous Communications-Pac, two lines with 25-foot data set cables (9.6K bps max)
- DCM9102 – Asynchronous Communications-Pac, one line with 25-foot data set cable (9.6K bps max)
- DCM9103 – Synchronous Communications-Pac, two lines with 25-foot data set cables (10.8K bps max)
- DCM9104 – Synchronous Communications-Pac, one line with 25-foot data set cable (10.8K bps max)
- DCM9105 – Synchronous Broadband Communications-Pac, one line with 25-foot data set cable (10.8K bps to 72K bps max)

PACKAGED CONFIGURATIONS

The MLC9103 is also available as the basis of two specially configured subsystems:

- MLC9101 – Packaged Multiline Communications Subsystem with eight asynchronous lines and including one MLC9103 and four DCM9101 Communications-Pacs.
- MLC9102 – Packaged Multiline Communications Subsystem with eight synchronous lines and including one MLC9103 and four DCM9103 Communications-Pacs.

SPECIFICATIONS

CAPACITY: From 1-8 lines; expandable by one or two.

TRANSMISSION TYPE: Half- or full-duplex over switched or private lines, as well as direct connect.

TRANSMISSION MODE: Asynchronous – Speeds from 50 to 9600 bps. Speeds programmable from set of fifteen: 9600, 7200, 4800, 2400, 1800, 1200, 1050, 600, 300, 200, 150, 134.5, 110, 75, 50 bps.

Synchronous – Speeds from 2,000 to 72,000 bps.

DATA FORMAT: Code length, program selectable: 5, 6, 7, or 8 bits per line. Stop bits (asynchronous lines), program selectable: 1, 1.5[1] or 2, per line.

CHARACTER PARITY: Checked on incoming data lines and generated for outgoing data lines, per software command. Sense: even, odd, or none; program-selectable per line.

CYCLIC REDUNDANCY CHECKS: Four program-selectable CRCs – CRC-16, CCITT-16, CRC-12, LRC-8.

MODEM INTERFACE: Conforms with domestic EIA RS232C and foreign CCITT specifications.

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[1] Five-level code only.

Specifications may change as design improvements are introduced.

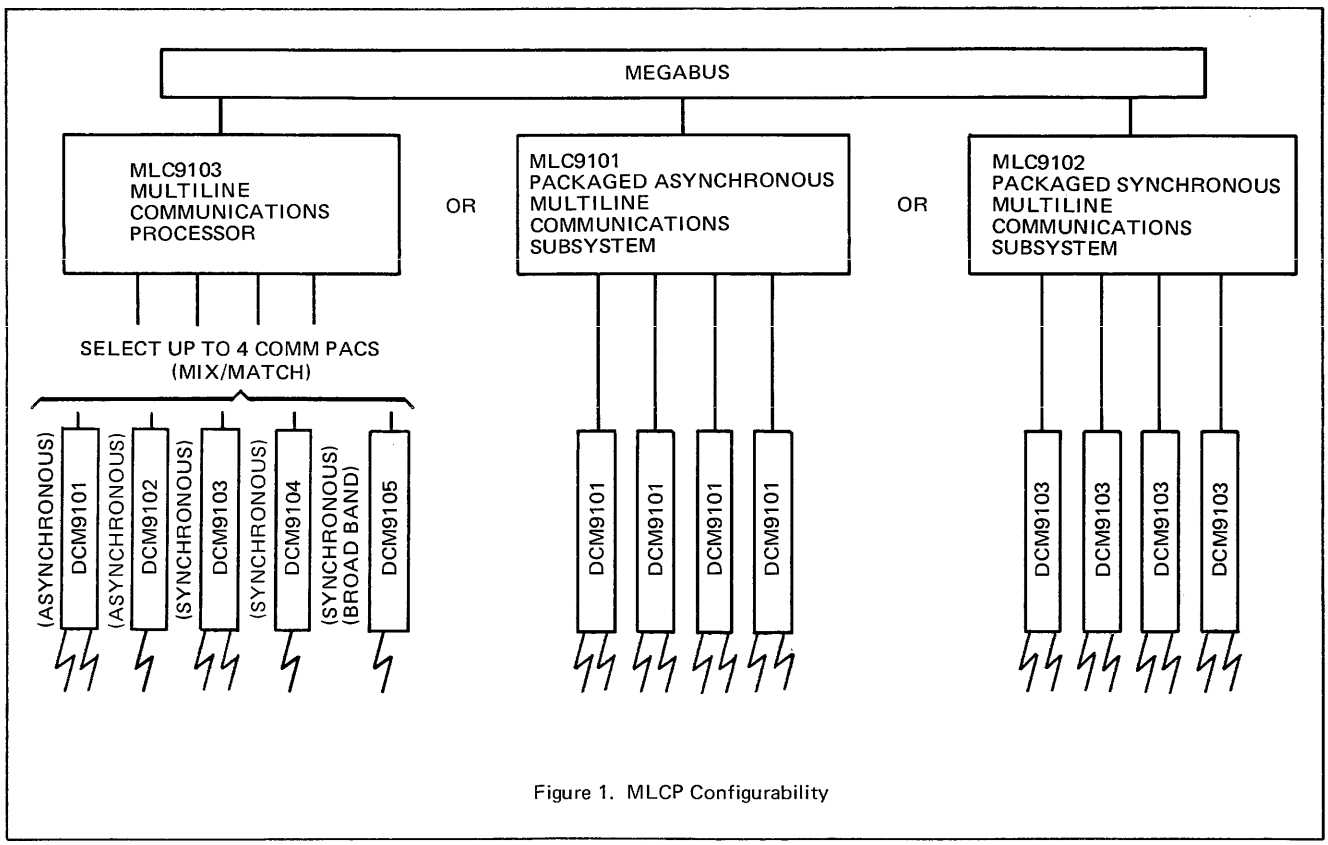

Figure 1. MLCP Configurability

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