II

SYSTEM DESCRIPTION

The Series 60 Level 6 Model 43 and Model 53 systems are available in a number of different configurations. Typical system configurations and the individual components that make up the system are described in this section. Also contained in this section is a description of the Megabus network and its operations. The items that are unique to these systems and increase system performance are functionally described in this section. The last subsection describes the optional components available for the system.

2.1 SYSTEM CONFIGURATIONS

The Model 43 and Model 53 systems are modular in design and flexible in configuration which allows the user to tailor the system to his specific needs. The basic system includes a central processor unit, Megabus Chassis with associated power supply, and a control panel. A minimum of 16KW of main memory must be configured in the system and the Model 53 system contains a cache memory (i.e., 4KW buffer memory between the CPU and main memory). Other components, including all peripheral devices are option dependent and selected by the user to complete the system. Figure 2-1 illustrates the two basic systems.

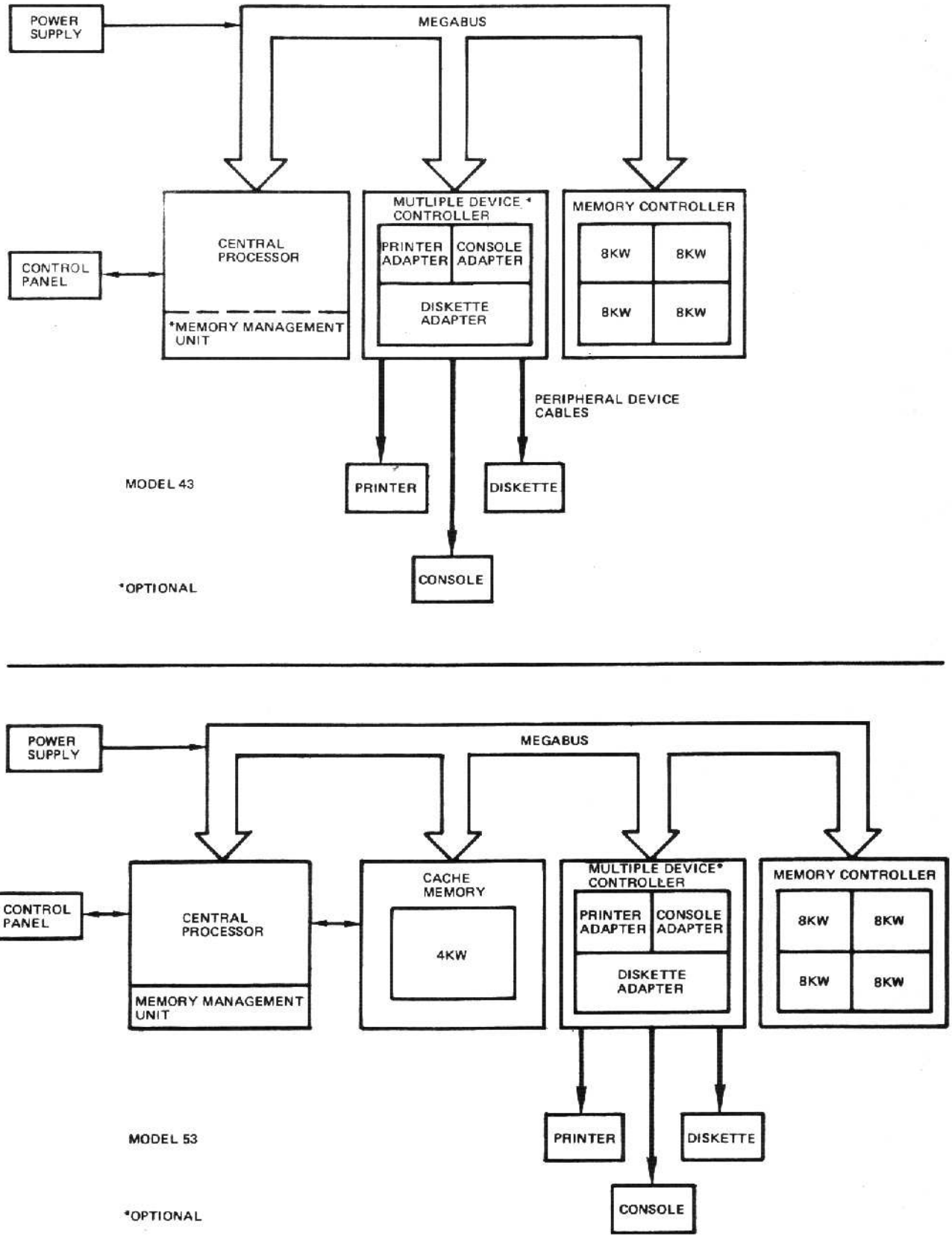


Figure 2-1 Model 43 and Model 53 Basic System

A variety of options (refer to subsection 2.3) can be added to the basic system. Each option requires the replacement or addition of an adapter board and possibly a full-size controller board to the system. Specific adapter boards mount on specific controller boards according to configuration rules specified in the Model 3X, 4X, 5X Installation Manual, Order Number CB68. No controller board can support more than four adapter boards. The maximum number of options that can be added to a system is restricted by the number of Megabus chassis slots available. The basic rack-mountable or office furniture package system can be expanded to a maximum of 23 chassis slots (i.e., two 10-board chassis plus one five-board chassis). Note, as each expansion chassis is added to the system, one chassis slot is taken for Megabus jumper cables. Figure 2-2 illustrates the functional configuration of a typical five-board Model 43 system and a typical nine-board Model 53 system.

2.2 SYSTEM ELEMENTS

This subsection provides the reader with a description of the primary components that make up the system. Discussed is the central processor and its features, Model 53 distinctions including cache memory, the different types of main memory and the Megabus network and its operations. A list of peripheral devices that can be attached to the system and a brief description of the system power components are also provided.

2.2.1 Central Processor

The Central Processor Unit (CPU) is a general purpose firmware controlled digital computer. It is designed to process Level 6 software instructions from main memory and to process information from associated system devices. The CPU uses firmware programs permanently stored in a read only memory to direct and control the step-by-step tasks necessary to execute each software instruction or to process data. The read only memory contains 2K locations of firmware programs. Each location contains 64 bits of information which when decoded enable specific hardware functions. Firmware is cycled out of read only memory in a predetermined order, according to the current system conditions, so that the specific hardware functions are enabled in the necessary sequence to carry out each software instruction or CPU process. Figure 2-3 is a block diagram of the CPU.

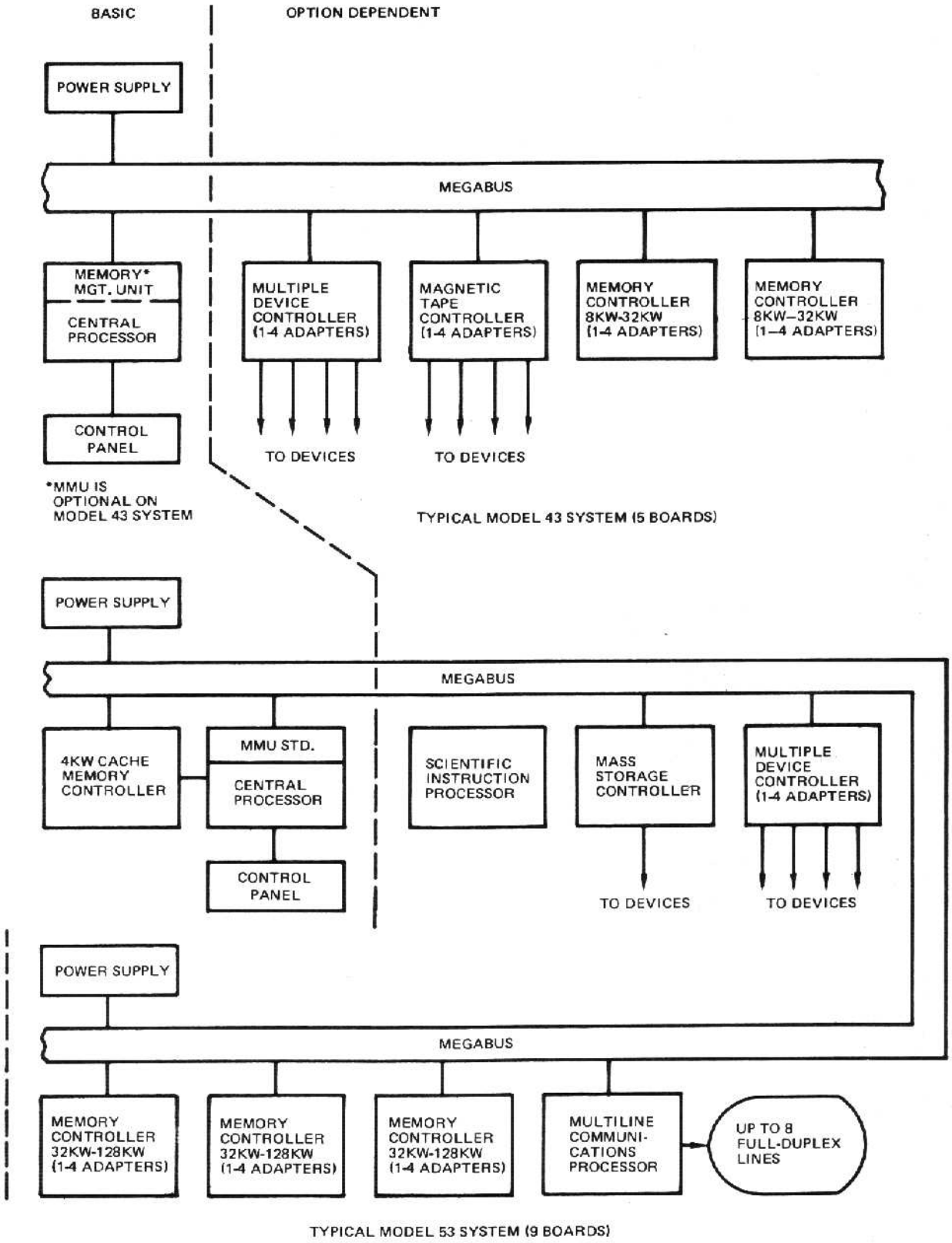


Figure 2-2 Typical System Configurations

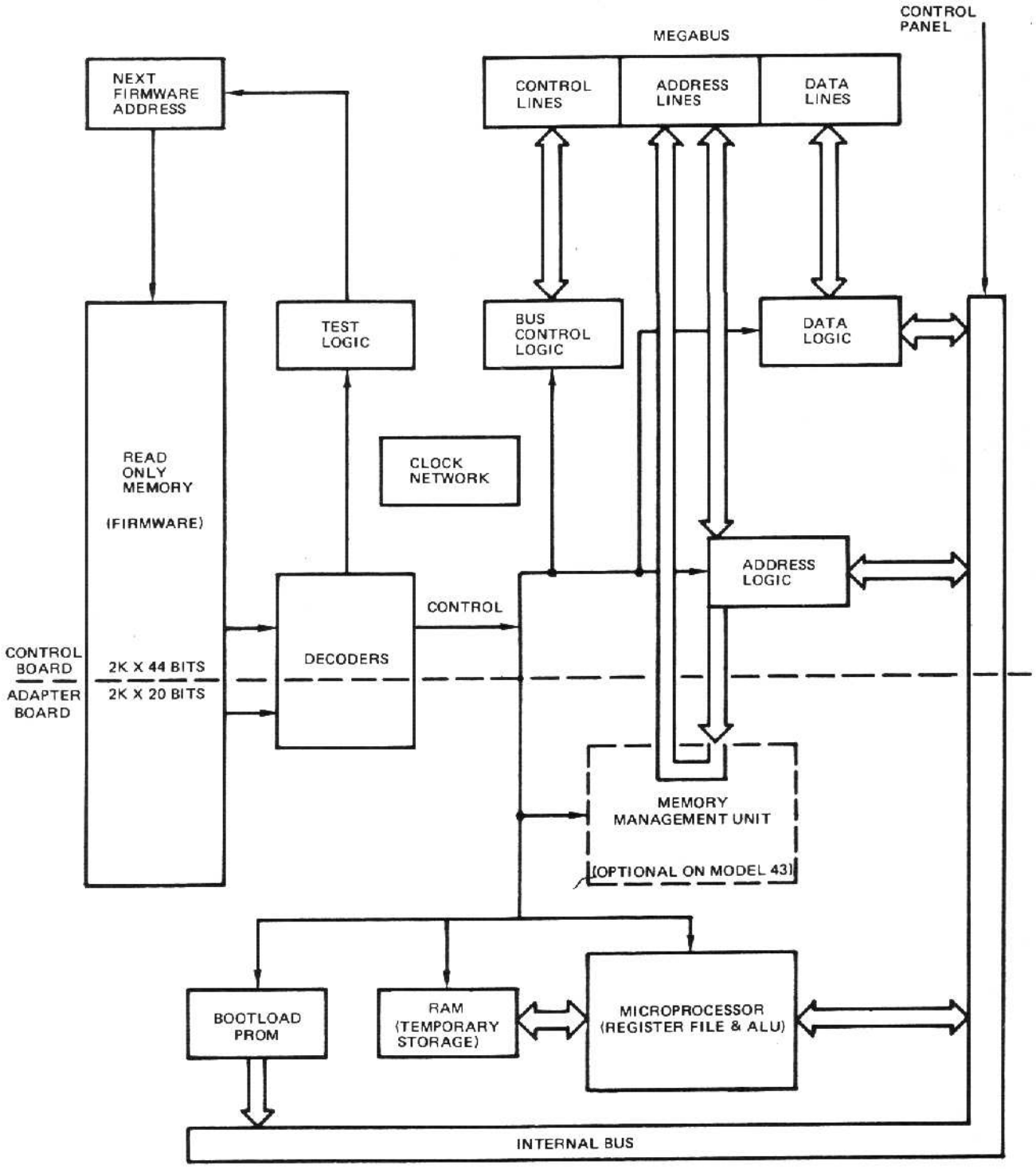


Figure 2-3 CPU Major Block Diagram

The central processor is physically contained on a full-size controller board and one full-size adapter board (see Figure 1-11). The processor board plugs directly into the Megabus chassis and contains storage for 44 bits of read only memory and associated control logic to sequence through firmware programs, the clock network, the Megabus interface logic, and other hardware. The adapter contains functional components such as storage for the remaining bits of read only memory, a Random Access Memory (RAM) for temporary storage, a bootstrap Programmable Read Only Memory (PROM), a microprocessor containing a register file and an arithmetic logic unit. In addition the adapter board contains the optional Memory Management Unit (MMU) if it is configured in the system. In the Model 53 system the adapter board also contains the interface logic necessary for cache memory communications.

The central processor communicates with the other components of the system (memory/controllers) through the Megabus network. Software programs control the selection of which instructions are executed and therefore the resulting communications over the Megabus. The software programs reside in main memory. Some of the general characteristics of the CPU which allows a number of different software programs to be executed are as follows:

- Short Address Formats (SAF) and Long Address Formats (LAF)
- 1,024-location ROS memory (64 bits per location)
- 16-bit word size
- 2M bytes of directly addressable main memory (1M word)
- 28 program visible general registers, including multiple accumulators, multiple address, index, and control registers
- Bit, byte, word, double and quadruple word operands
- Bit test, set and mask capability
- Immediate register-to-register and register-to-memory operation
- 64 interrupt levels
- Multiple vectored trap structure
- Trap support of interpretive implementation of features such as floating point functionality
- Stack/queue handling
- Hardware supported context save and restore

- Multiple addressing modes, including indexing, indirect base plus displacement, program counter relative autoincrement/autodecrement
- Permanent bootstrap
- Power fail detection
- Real-time clock and watchdog timer
- Automatic restart.

Double-word fetching, SAF/LAF addressing, and stack/queue handling are CPU features which increase system performance. These features are described in subsections 2.2.1.1 through 2.2.1.4.

2.2.1.1 Double Word Fetch Feature

The CPU has a double-word fetch capability. This feature allows the CPU to receive two consecutive memory words with one request when issued to a double-word fetch memory controller. This action effectively reduces memory access time and allows the CPU to achieve a greater throughput.

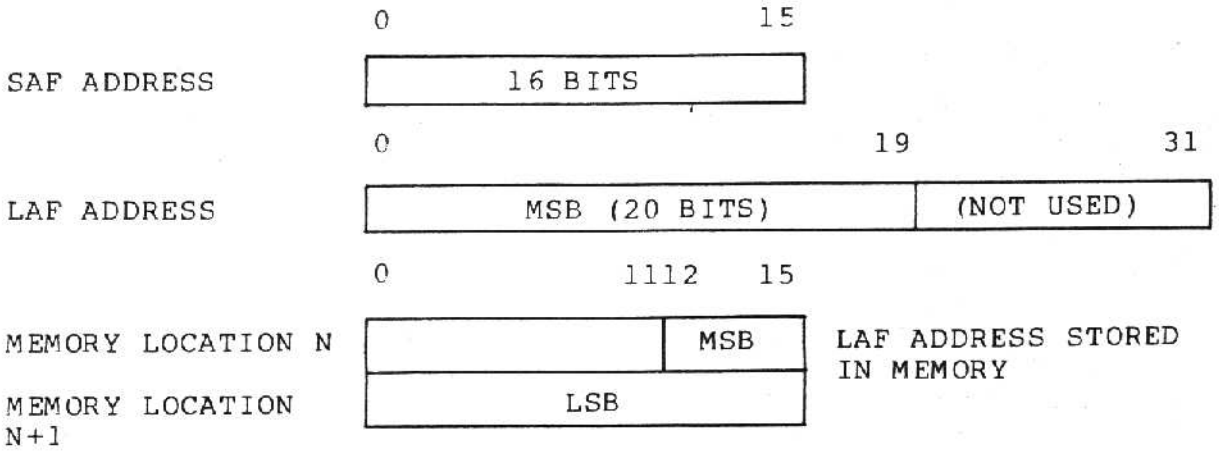
Whenever the CPU requires two consecutive words from main memory, it issues a double pull memory read request over the Megabus. If a double-fetch memory controller is addressed, it responds by sending the requested data with two response cycles. During the first response cycle, the memory controller informs the CPU that a second data word is coming by forcing a dedicated Megabus signal true. If a nondouble fetch memory controller is addressed, the double fetch line is false during the initial response cycle informing the CPU it must issue a second read request cycle to obtain the second data word.

2.2.1.2 SAF and LAF Addressing

To efficiently operate in both a small and large main memory environment, the CPU supports two addressing modes: (1) Short Address Format (SAF) and (2) Long Address Format (LAF). When in SAF mode, all memory addresses are limited to 16 bits and therefore maximum addressable memory is 65KW. This feature allows a complete address to be stored in a single memory location or CPU register and ensures no extra processing time is expended manipulating addresses beyond 16 bits. In LAF mode, all addresses are a 32-bit value and actual physical addresses are limited to 20 bits. Therefore a maximum of one megaword of memory space can be directly addressed.

The selection of which address mode the CPU operates in is determined by a hardware SAF/LAF configuration switch, physically located within the control panel. When this switch is in the LAF position, LAF addressing is effective and the LAF indicator on the control panel illuminates.

It requires two locations in memory to store a LAF address, see the following formats.



MSB - 4 MOST SIGNIFICANT BITS
LSB - 16 LEAST SIGNIFICANT BITS

2.2.1.3 Stack Management

The CPU supports stack structures in main memory. Stack structures are software defined memory areas consisting of a stack header and storage space for a stack of variable length data frames (stack frames). Each stack frame has its data length defined by the first location within the frame (see Figure 2-4). A single stack structure can be set up for each interrupt level. The currently active stack structure is pointed to by the contents of the CPU stack regsiter. Software initially defines the maximum stack structure size when the header is created. Variable stack frames can then be added or deleted from the stack with the CPU maintaining the current number of locations consumed in the stack. If a stack overflow or underflow occurs, the CPU generates a trap to inform the software of the event.

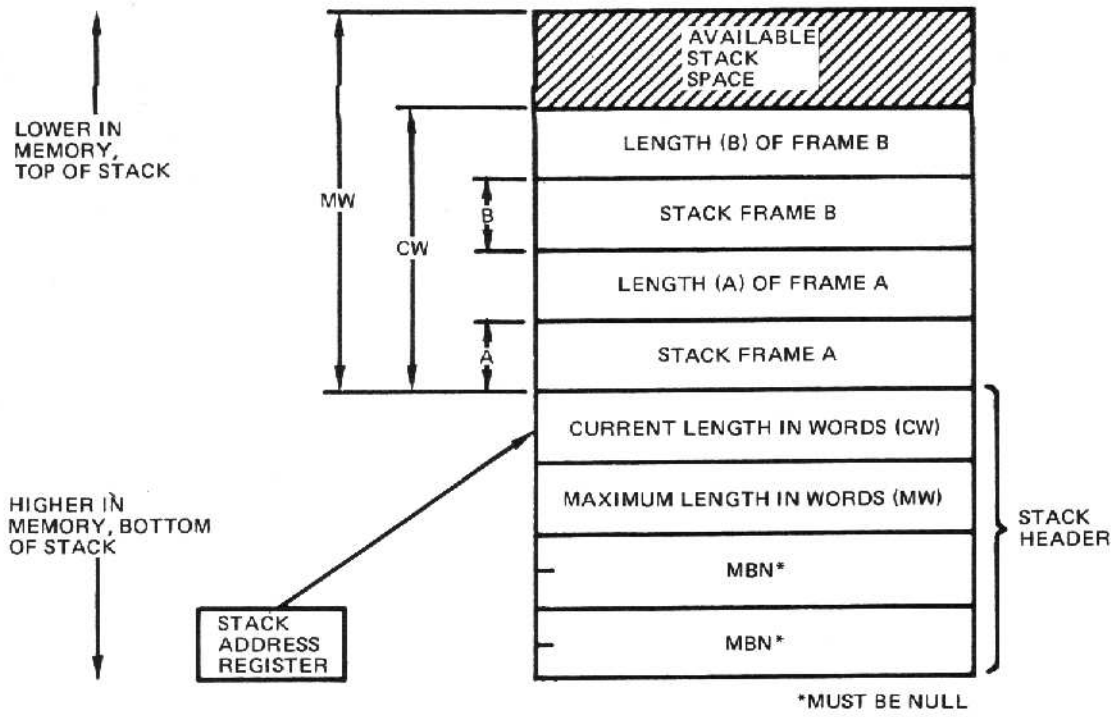
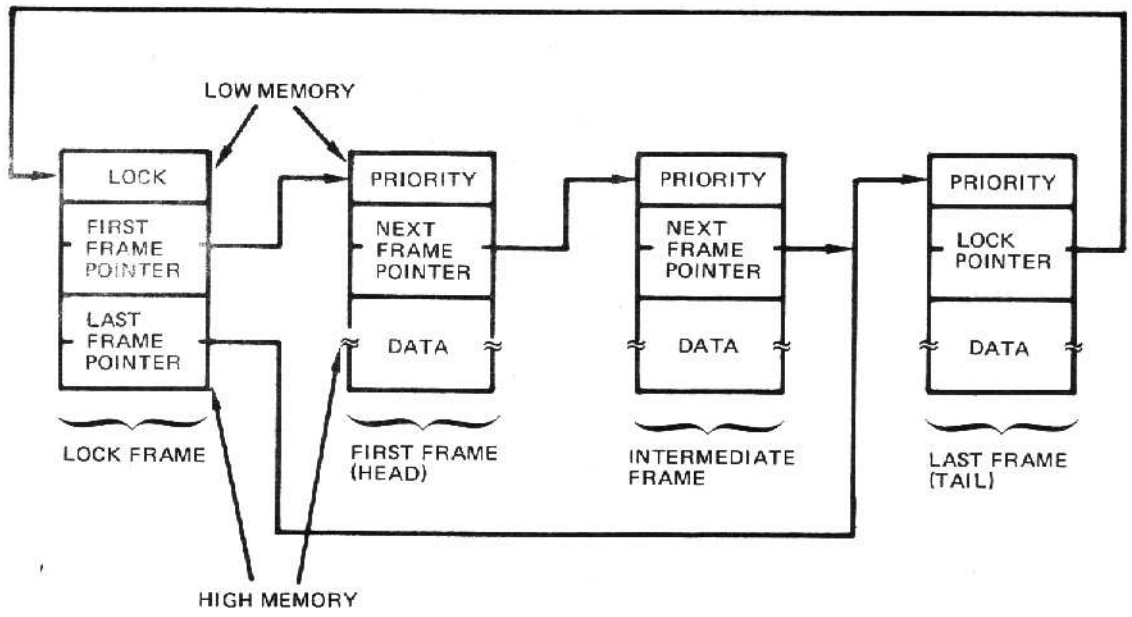


Figure 2-4 Stack Structure

2.2.1.4 Queue Management

The CPU has advanced queue handling capabilities which allow easy maintenance of queue areas in main memory. These areas are set up and controlled by software and are used to implement and control software operating systems. Each queue area consists of a list of ordered frames and is identified by a LOCK frame containing a LOCK word and head and tail pointers of the queue. The other frames contain a priority number, next frame pointer, and associated data (see Figure 2-5).



NOTES:

1. SCANNING (IF ANY) IS ALWAYS PERFORMED FROM FIRST FRAME (HEAD) TO LAST FRAME (TAIL).
2. PRIORITY IS AN UNSIGNED 16-BIT INTEGER.
3. FRAME POINTERS ARE TWO WORDS FOR LAF MODE, ONE WORD FOR SAF MODE.

Figure 2-5 Queue Management

Special generic instructions are used to access queue data. The LOCK frame is used to ensure only one CPU is accessing a particular queue at a time. Each of these instructions will cause the LOCK word to be fetched with a Read-Modify-Write (RMW) cycle. If the LOCK is set, the RMW cycle will execute without modifying the LOCK word contents, the data will not be accessed and the next instruction will be executed. If the LOCK word is reset, the CPU will set the LOCK with the RMW cycle and initiate the execution of the generic instruction. Each queue/dequeue instruction causes a scan of the frames from the head to the tail of the data. The scan continues until the conditions of the particular instruction are met, or the last frame is reached, or an interrupt occurs. If a frame is found with the desired conditions, it is either linked into or out of the list as specified in the instruction. In all cases, at the end of the scan the CPU issues another RMW cycle to reset the LOCK and make the queue available to other CPUs in a multiple CPU environment.

2.2.1.5 Interrupts and Traps

The CPU supports 46 trap events and 64 priority levels of interrupts. Traps are distinguished from interrupts by being synchronous with and in some sense caused by the currently executed instruction. On the other hand, interrupts are generally unrelated or at least asynchronous to the current instruction.

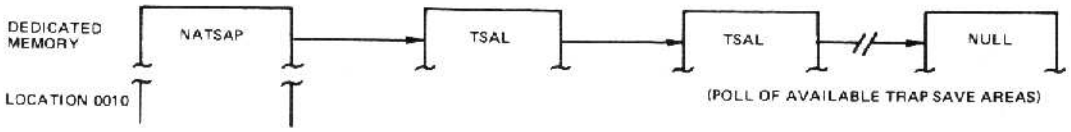
Interrupts

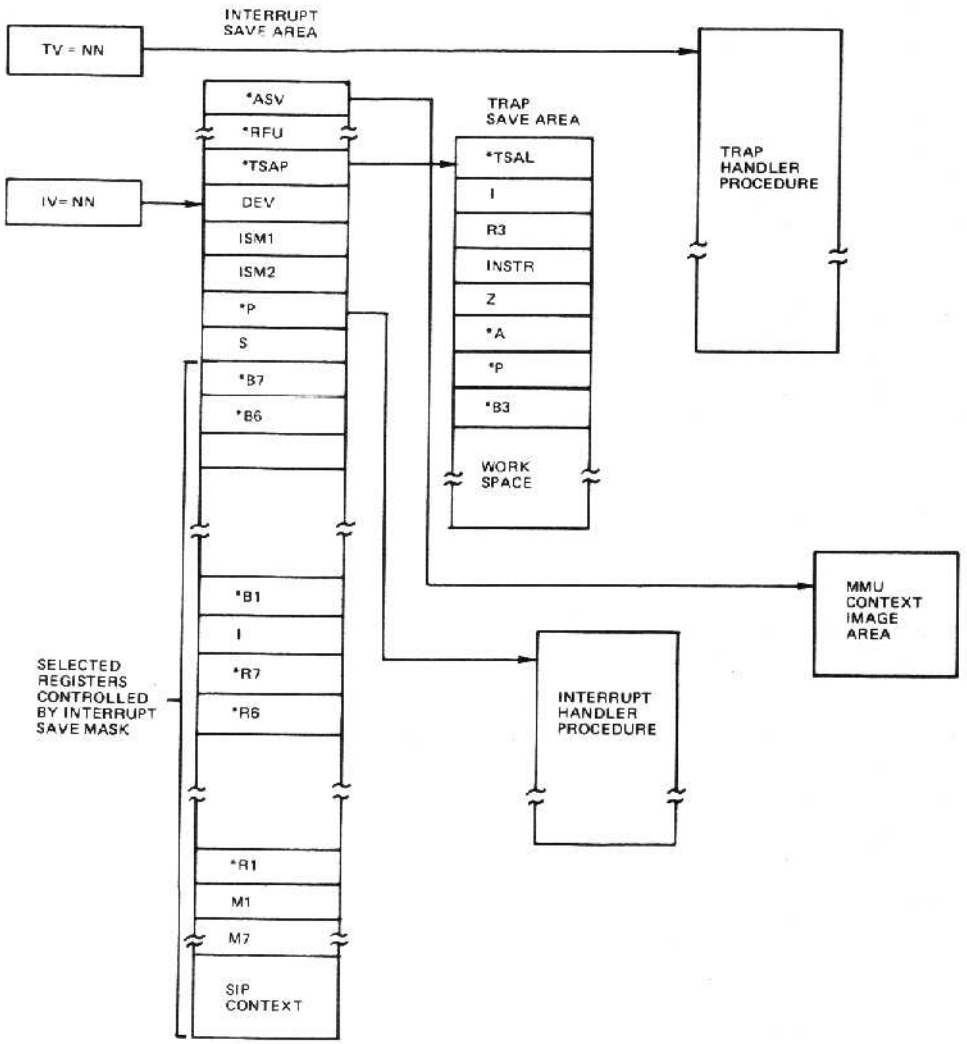
Interrupts occur at the end of the current instruction. Each program is assigned an interrupt level. Associated with each level is a corresponding Interrupt Vector (IV) which is stored in dedicated main memory locations. The IV is a pointer to an Interrupt Saving Area (ISA). When an executing program is interrupted, its context is stored in its corresponding ISA. The context of the interrupting process is retrieved from the ISA associated with the interrupt level. Then processing starts executing at the new assigned level.

When an interrupt occurs the corresponding IV is extracted and provides access to its ISA, into which certain registers and related information is stored. The ISA contains six location (TSAP, DEV, ISM1, ISM2, P, S) plus a variable number of locations dependent on the contents of the Interrupt Save Masks (ISM1, ISM2). TSAP points to any trap information associated with the level of interrupt and P contains the program counter with S reporting system status (see Figure 2-6). ASV is a pointer to context of the memory management unit and is only present if specified by ISM2. This information is used to process the interrupt.

Key interrupt features are:

- 64 priority levels (0-highest priority through 63-lowest priority)
- Active/inactive flag in dedicated memory for each priority level. Flags are set by the interrupt event and set/cleared by software instruction.
- Interrupt save area pointer in dedicated memory for each priority level (interrupt vector).
- The firmware supported dispatch (save/restore) ensures that the highest priority active task becomes the running task during software interrupt (e.g., if an interrupt event occurs with a level number lower (higher priority) than the current running level, the current task is saved and the interrupting task is restored and executed.
- Variable size context save area (ISA) as determined by the interrupt save mask.
- Supports multiple trap events at each priority level.





(TYPICAL)
*OCCUPIES TWO LOCATIONS IF LAF MODE

ASV	=	ADDRESS SAVING VECTOR
DEV	=	IDENTITY OF INTERRUPTING DEVICE
I'	=	CONTENTS OF I REGISTER AND NO. OF TRAP ASSOCIATED WITH THE TSA
ISM1 ISM2	=	INTERRUPT SAVE MASK
IV NO.	=	INTERRUPT VECTOR FOR LEVEL NO.
NATSAP	=	NEXT AVAILABLE TSA POINTER
RHU	=	RESERVED FOR HARDWARE USE
TSA	=	TRAP SAVE AREA
TSAL	=	TRAP SAVE AREA LINK
TSAP	=	TRAP SAVE AREA POINTER
TV NO.	=	TRAP VECTOR FOR CLASS NO.
Z	=	MISCELLANEOUS INFORMATION ABOUT INSTRUCTION

Figure 2-6 Trap/Interrupt Linkage

Traps

A number of events can cause traps (refer to Table 2-1). Each event is associated with a Trap Vector (TV). Trap vectors are stored in dedicated memory locations and are used as pointers to software handling procedures for each of the trap causing events.

Multiple trap conditions at any interrupt level are supported by a pool of Trap Save Areas (TSA) and dedicated Next Available Trap Save Area Pointer (NATSAP). The TSAs store information relating to the trap event and are pointed to by a location (TSAP) in the interrupt save area. Multiple trap save areas are linked together by trap link pointers (TSAL) in the TSA area. Figure 2-6 illustrates the relationship between trap and interrupt save areas.

Table 2-1 Trap Vectors and Events (Sheet 1 of 2)

VECTOR NUMBER	EVENT
Vector 1	Monitor call (MCL instruction)
Vector 2	Trace* (debug) or BRK instruction
Vector 3	Scientific operation not in hardware
Vector 4	RSU
Vector 5	Other operation not in hardware (or undefined)
Vector 6	Integer register overflow*
Vector 7	Scientific divide by zero
Vector 8	Scientific exponent overflow
Vector 9	Stack underflow
Vector 10	Stack overflow
Vector 11	Reserved for future use
Vector 12	Reserved for future use
Vector 13	Unprivileged use of privileged operation
Vector 14	Unauthorized reference to protected memory (with optional protection)
Vector 15	Reference to unavailable resources
Vector 16	Program error

Table 2-1 Trap Vectors and Events (Sheet 2 of 2)

VECTOR NUMBER	EVENT
Vector 17	Memory or bus error (parity or noncorrectable ECC) detected
Vector 18	RFU
Vector 19	Scientific exponent underflow*
Vector 20	Scientific program error
Vector 21	Scientific significance error*
Vector 22	Scientific precision error*
Vector 23	Reference to unavailable resources by external processor
Vector 24	Memory or Bus error detected by external processor
Vector 25	RFU
Vector 26	
Vector 27	
Vector 28	
Vector 29	
Vector 30 through Vector 46	

*If enabled.

2.2.1.6 Dedicated Memory

In order to support trap and interrupt handling and other hardware, 256 locations of main memory are dedicated to hardware use. Some locations are common for both LAF and SAF mode operations. However, locations that store pointers are different dependent on the active address mode. See Figure 2-7. If multiple CPUs are installed in the system a separate 256 location block of memory is set aside for each CPU configured in the system.

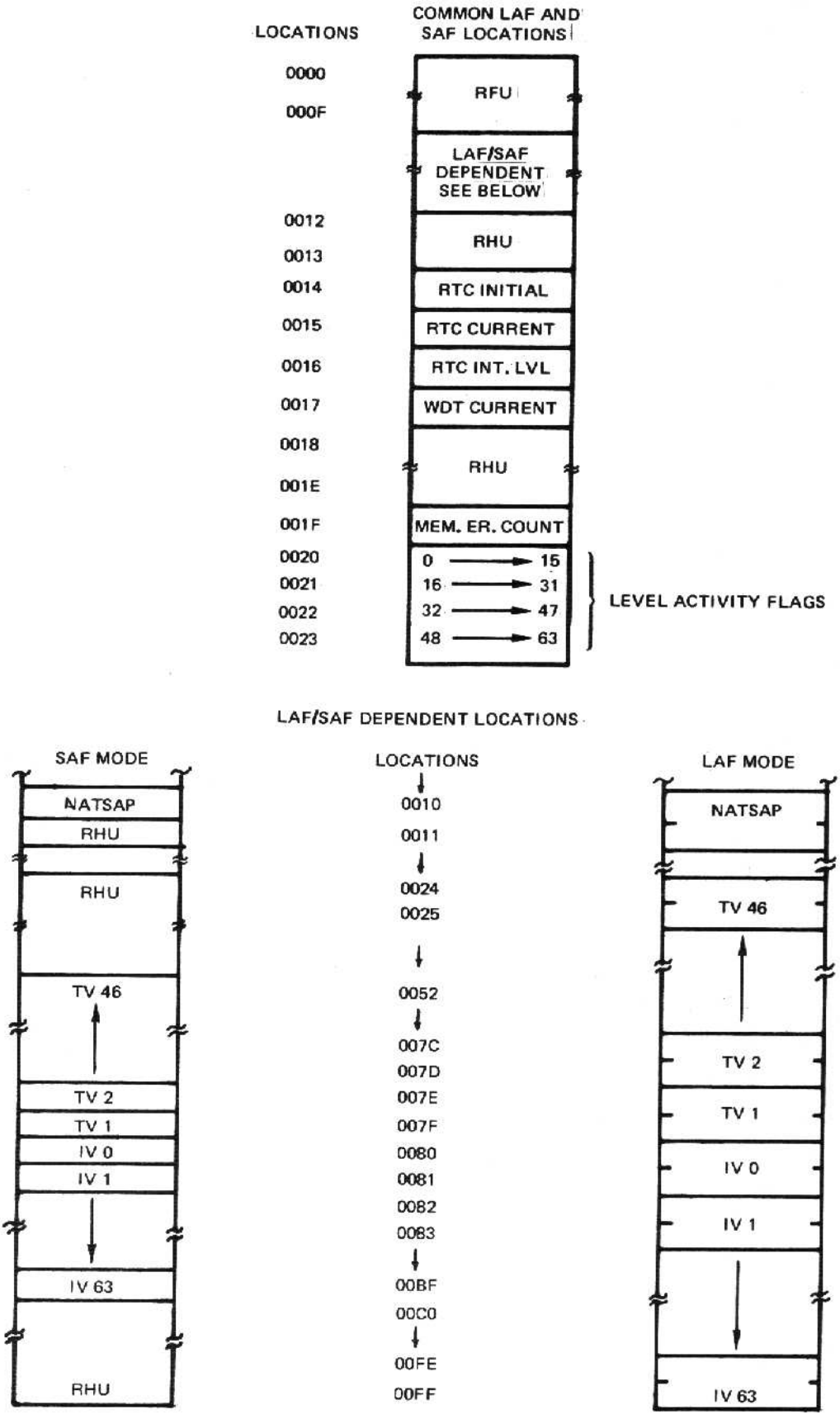


Figure 2-7 Dedicated Memory Locations

2.2.1.7 Quality Logic Test

The system supports built-in Quality Logic Tests (QLTs) which verify hardware integrity during system initialization. Each controller contains its own QLT logic which is activated when a master clear signal is sensed on the Megabus. The QLT tests are initiated when power is applied to the system or the initialize pushbutton on the control panel is depressed. Successful completion of the tests is visually indicated by the CHECK indicator on the control panel and by individual QLT lamps located on the outside edge of the CPU, MDC, MTC, and MLC controller boards. These indicators are illuminated when the QLT tests are activated and they extinguish when the QLT for that particular board is completed without detecting an error. The CHECK indicator on the panel is controlled by CPU logic and is extinguished only if all the units complete their QLT test successfully.

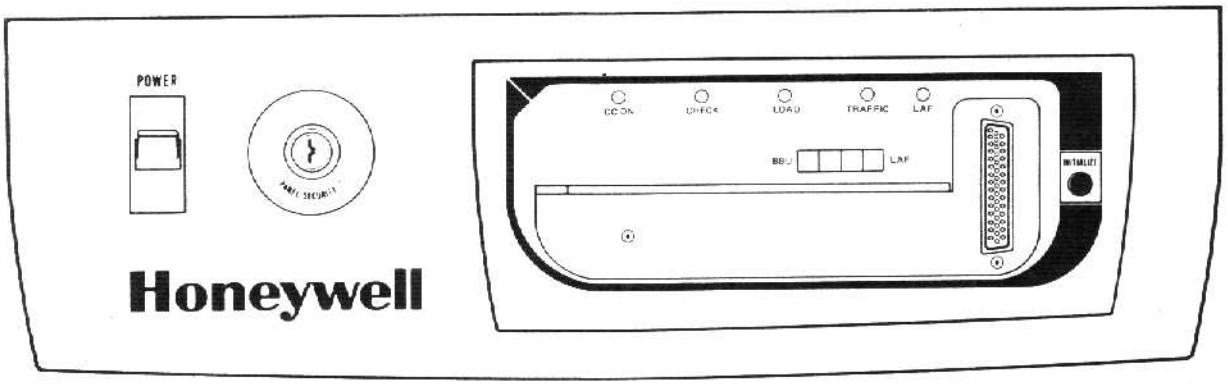
The CPU quality logic tests are firmware programs which reside in read only memory. When activated, they initially check CPU hardware and data paths. If successful the test progresses to perform tests on all main memory. Then extended QLT tests are executed. In these tests, pseudo software instructions are loaded into main memory and executed. The results are checked to verify correct operation of hardware. If all CPU tests are error free, the indicator on the CPU board is extinguished. A final check of a Megabus QLT signal is performed to determine if all other controllers on the bus have completed their self-contained QLT tests. If all units completed their test successfully, the CHECK indicator on the control panel is extinguished. A failure of any QLT test causes the CHECK and QLT indicator on the failing board to remain illuminated.

2.2.1.8 Control Panels

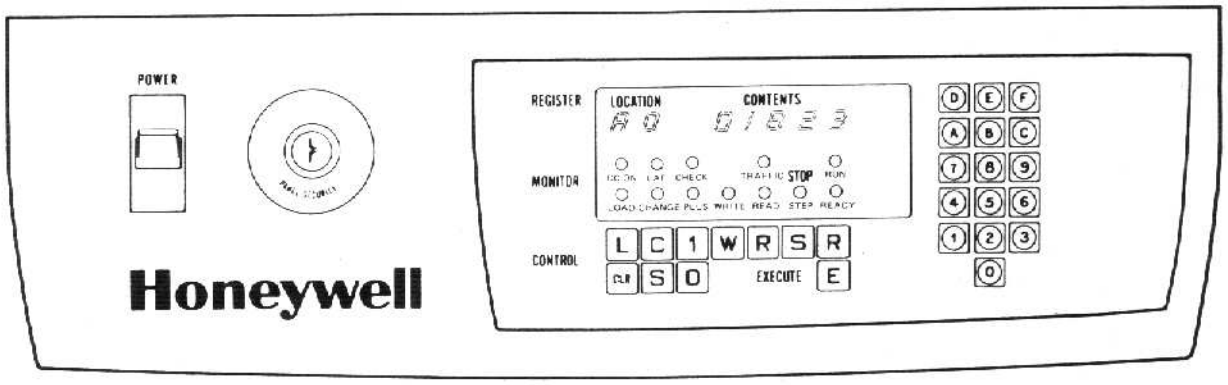
There are three types of control panels available for the system: full, basic, and portable.

The full control panel allows the CPU register and main memory contents to be entered and displayed. It controls system initialization, stopping and starting program execution, single-stepping a program, and data entry/display.

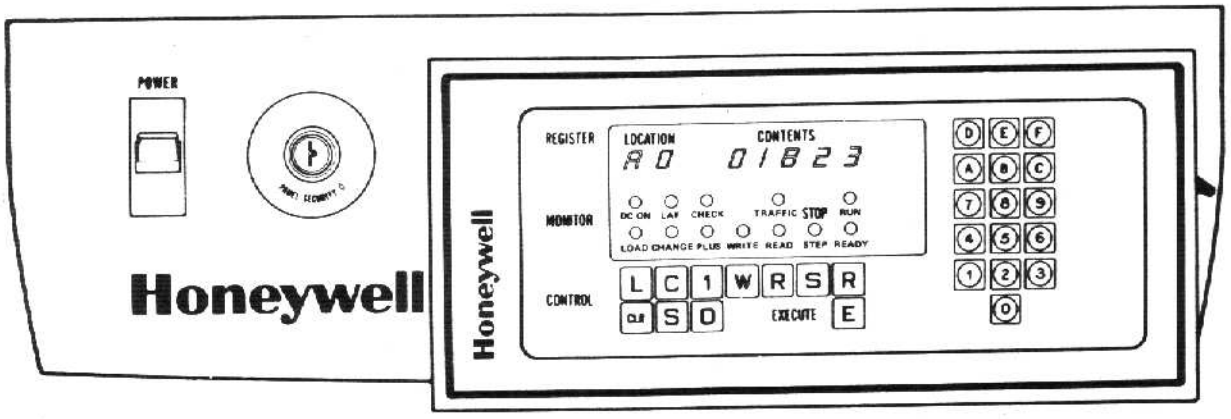
The basic control panel is for systems which do not require direct operator access to memory or CPU registers. This control panel's capability is to start the system initialization process. However, an optional portable control panel is available which be attached to the basic panel to give full panel functionality to the system equipped with the basic panel. See Figure 2-8.



a. BASIC CONTROL PANEL



b. FULL CONTROL PANEL (Local or Remote)



c. PORTABLE FULL CONTROL PANEL PLUG IN (Shown plugged into Basic Panel)

Figure 2-8 System Control Panels

The location of the system control panel is dependent on the type of cabinetry selected by the user. The tabletop system has the control panel recessed into the tabletop cover. The full size 60-inch high rack sysem has the control panel protruding from the cabinet on a hinged assembly which permits access to the card chassis. Systems configured in the 30-inch rack have a flat control panel mounted vertically on the rack, concealed behind the front door of the cabinet. The control panel can be operated in the vertical position or can swing up to an inclined position for the users convenience. In office furniture package systems the control panel can be located either in the 30 inch rack or it can be recessed in the tabletop.

Each control panel contains a circuit board, a switch and indicator assembly plus ac and lock hardware. Located on the internal circuit board is a configuration chip which houses four rocker switches. These switches supply configuration information to the central processor and must be set correctly before system operation. Access to the swiches is through a sliding door on the front of the basic panel and from the rear of the panel on a full control panel (see Figure 2-9). The portable control panel switches are preset at the factory and are not accessed. The switch settings are as follows:

- The switch in position 1 (on extreme left on the basic control panel) is the volatile memory switch which is set to OFF if a memory save (battery back up) unit or core memory is configured in the system. In the OFF position an auto restart will occur on power up after a power failure. This switch is set to ON if memory is volatile (i.e., no memory save unit or core memory). In the ON position an auto bootload will occur on power up after a power failure.

- The second switch (position 2) is not used.

- The third switch (position 3) indicates the type of panel. It should be set to ON if it is a full control panel and set to OFF for a portable control panel.

- The fourth switch (position 4) is the LAF switch which is set to ON to place the CPU in long address format mode or the switch is set to OFF to place the CPU in short address format mode.

NOTE

The volatile memory and address mode switch settings in the portable control panel have no significance. For these switches, the basic control panel setting overrides the portable control panel setting. Early revision control panels had switch positions swapped around. See installation manual. The chip on the full control panel is on the reverse side of the circuit board. Therefore, switch positions appear reversed (see Figure 2-9).

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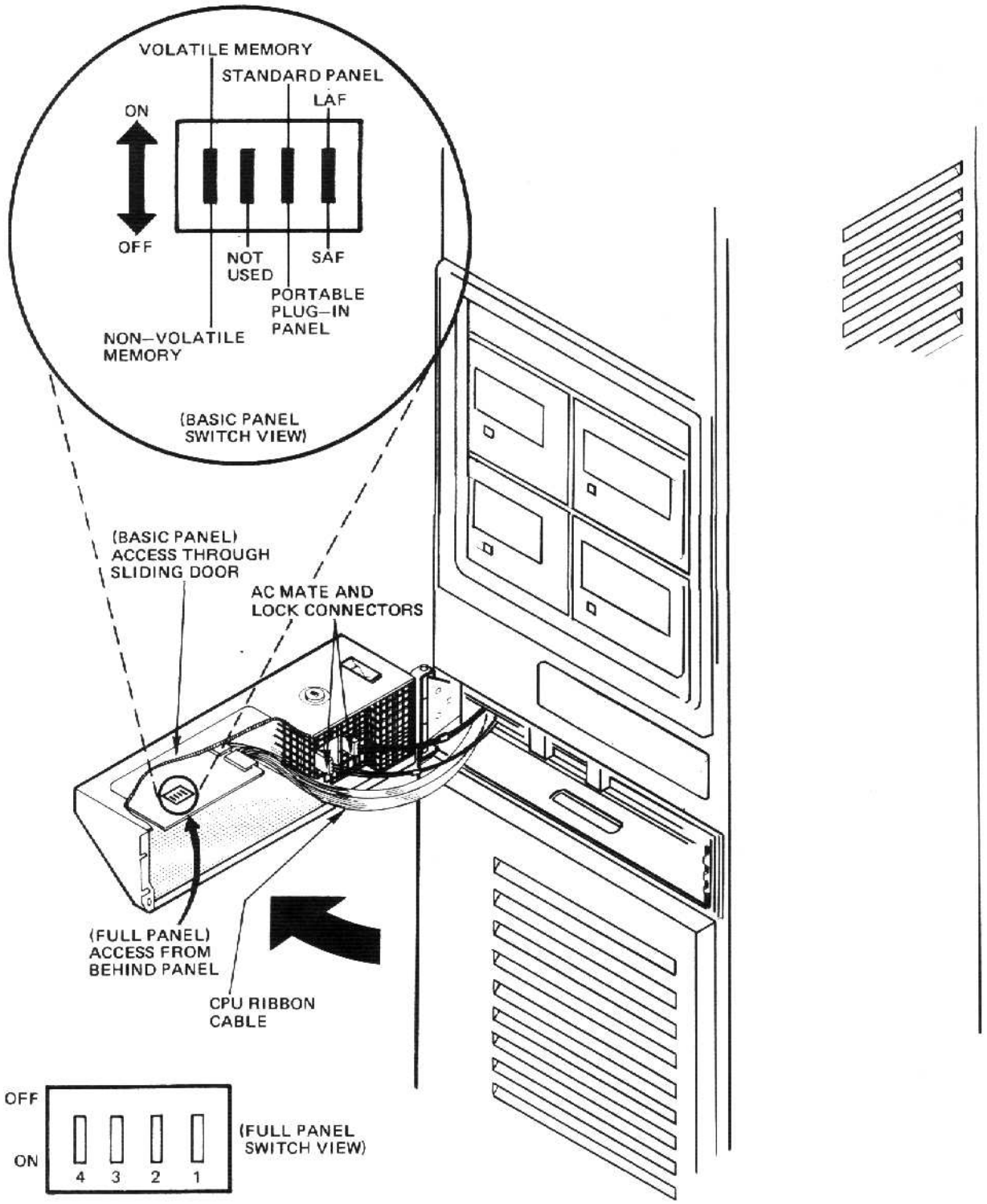


Figure 2-9 Control Panel Configuration Switch Access

2.2.1.9 Operational Modes

The system can operate in either manual or automatic mode.

Manual Mode

The system ooperates in the manual mode whenever it is configured with full control panel functionality and the control panel is in the unlocked state. When in this mode, operator intervention is required to initiate any activity, including initialization and bootload operations.

Automatic Mode

The system operates in the automatic mode whenever it is configured with a basic control panel or when a full control panel configuration is in the locked state. When in this mode, the CPU reacts to a system power up or an initialization signal as shown in Figure 2-10.

2.2.1.10 Multiple Central Processors

Up to four central processors can be attached to the same Megabus to form a multiprocessor configuration. Each CPU is assigned a unique channel number and one CPU is designated as the master CPU. The control panel only attaches to the master CPU (see Figure 2-11). There are no connections or paths between CPUs except the Megabus. All inter CPU communications are performed via interrupts and the following applies:

- The master CPU is assigned channel number 0000 hex. The other CPUs are assigned channel numbers 0040, 0080, 00C0 hex.
- The master CPU is used to perform all bootload operations.
- On power up, the master CPU will perform its own QLT test including the testing of all main memory. The other CPUs perform their own QLT tests but do not perform main memory tests.
- Dedicated memory locations for nonmaster CPUs are relocated by their channel number value.
- Separate cache memories and scientific instruction processors are required for each CPU, if the option is desired.

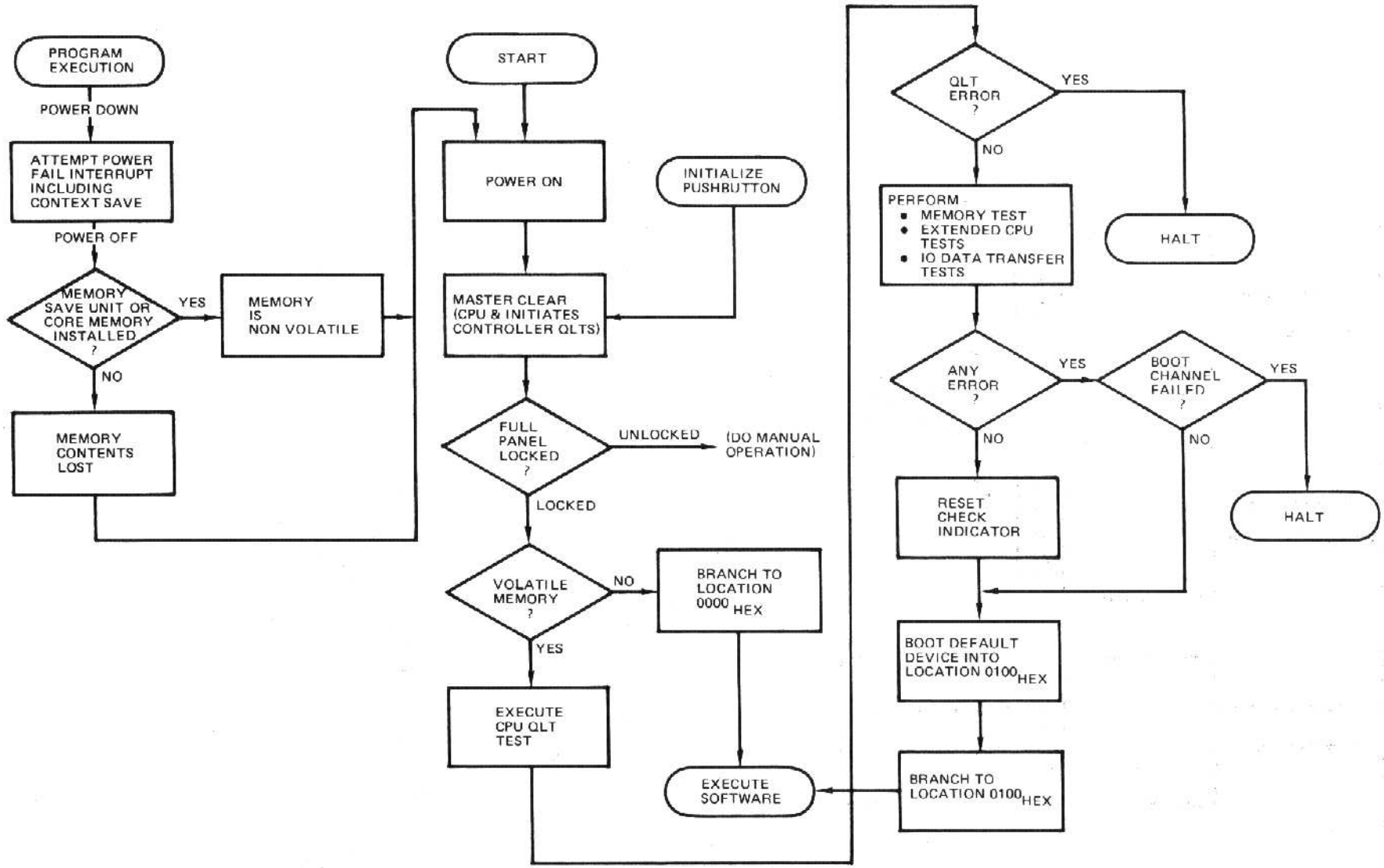


Figure 2-10 System Start Up/Initialization Sequence

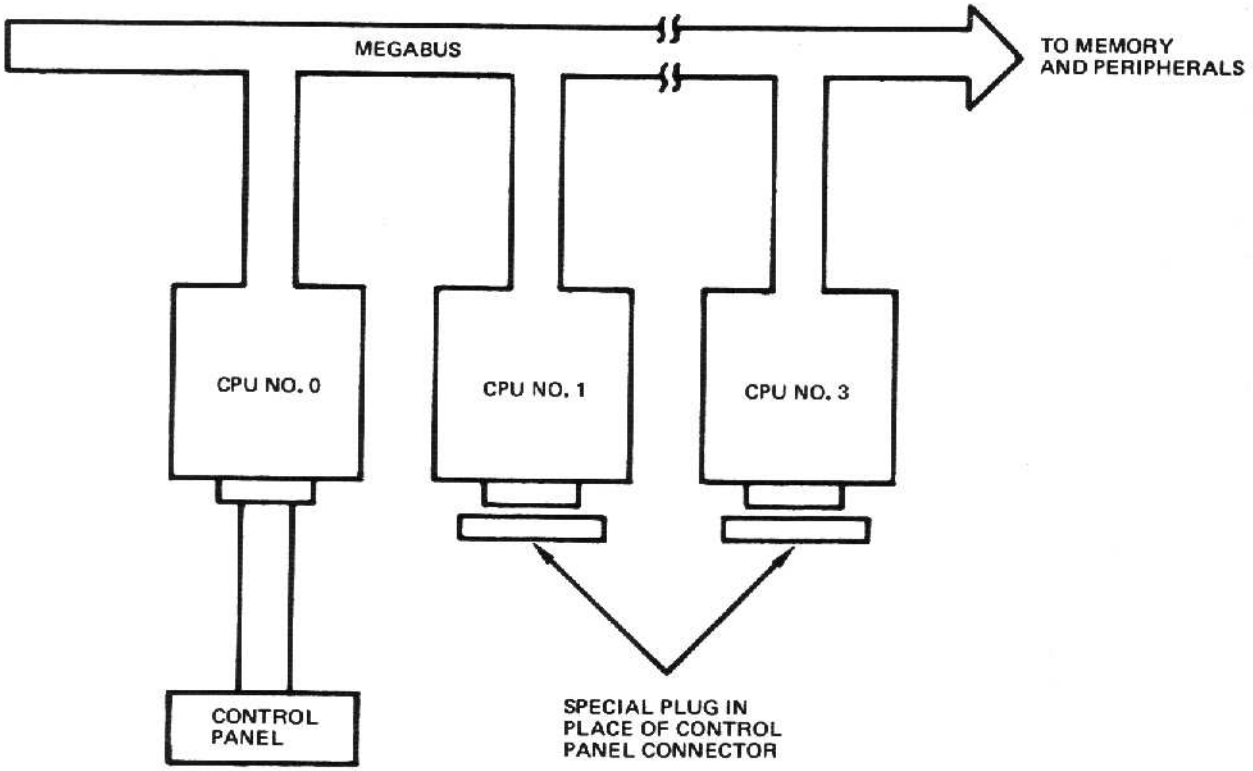


Figure 2-11 Multiprocessor Set Up

2.2.2 Model 53 System Differences

The Model 53 System contains all the components and functionality of the Model 43 system (refer to subsection 2.2) plus a 4KW cache memory, a memory management unit and the Model 53 system is always configured with a full control panel.

2.2.2.1 Cache Memory Unit

The cache memory unit is a standard part of the Model 53 system. This memory is used in conjunction with the CPU to improve speed and enhance the CPU performance by reducing the memory access time required to fetch information stored in main memory. The cache memory unit is a buffer, Random Access Memory (RAM) which contains high speed storage capabilities for up to 4KW from main memory, and makes this data available to the CPU via a private CPU/cache memory interface. The cache memory unit continually updates its storage area in order to maintain the most likely data required by the CPU (i.e., next instructions, operand fields). The cache memory has no direct operator or software interface, and is not visible to software. Figure 2-12 shows the cache memory unit. For more information refer to the Series 60 Level 6 Cache Memory Manual, Order Number FQ30.

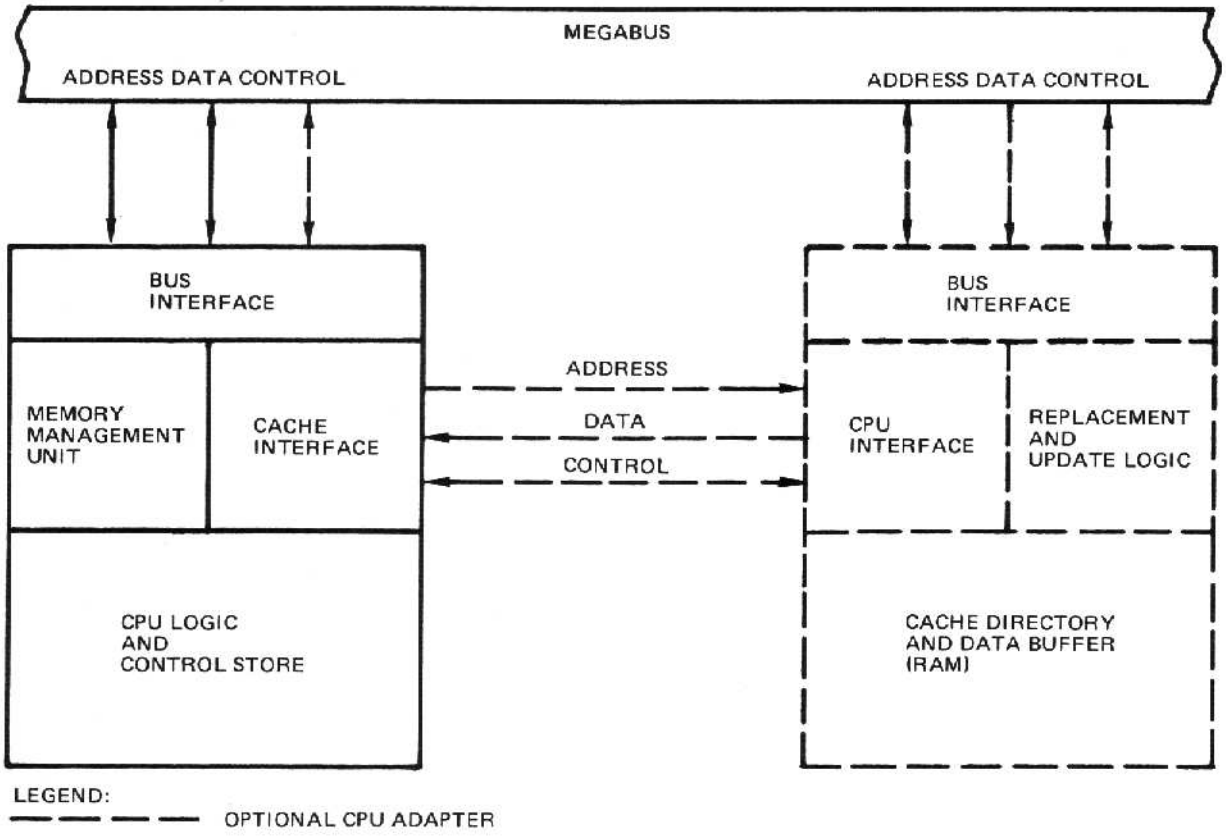


Figure 2-12 Cache Memory/CPU Block Diagram

The cache memory unit is contained on a full size controller board and a full size 4KW RAM adapter board mounted on the controller (see Figure 2-13). The cache controller board is always installed in the Megabus slot above and adjacent to the CPU slot. Three private interface ribbon cables between the CPU and cache units are attached with screws and cable restraints. This physically ties the two units together. Thus, if the CPU board is removed or installed in the Megabus chassis, the cache memory and CPU boards must be simultaneously removed or installed as one unit.

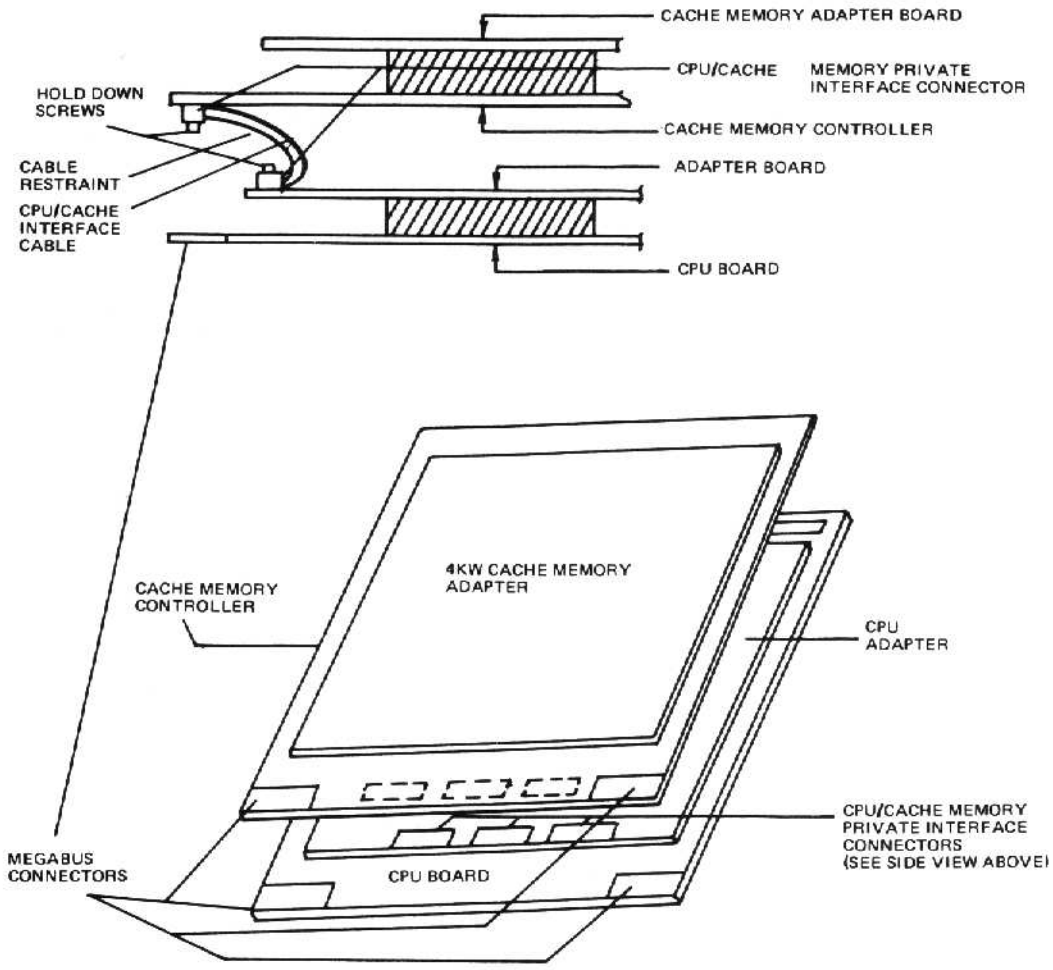


Figure 2-13 Model 53 System Cache Memory and Central Processor Boards

2.2.2.2 Memory Management Unit

The Memory Management Unit (MMU) provides the CPU with advanced memory protection and relocation capabilities. The MMU performs access right checks and relocates each memory reference address before it is permitted to take part in a memory access. With the MMU installed, software segments memory and assigns separate read access, write access, and execute access permission to each segment of memory. This information is stored in the MMU and is used by hardware to ensure each memory address is legitimate and does not violate any of the software imposed restrictions. If the MMU detects an illegal address or an address to a segment of memory not assigned the proper access permission, it inhibits the memory access and a protection violation trap results (see Figure 2-14).

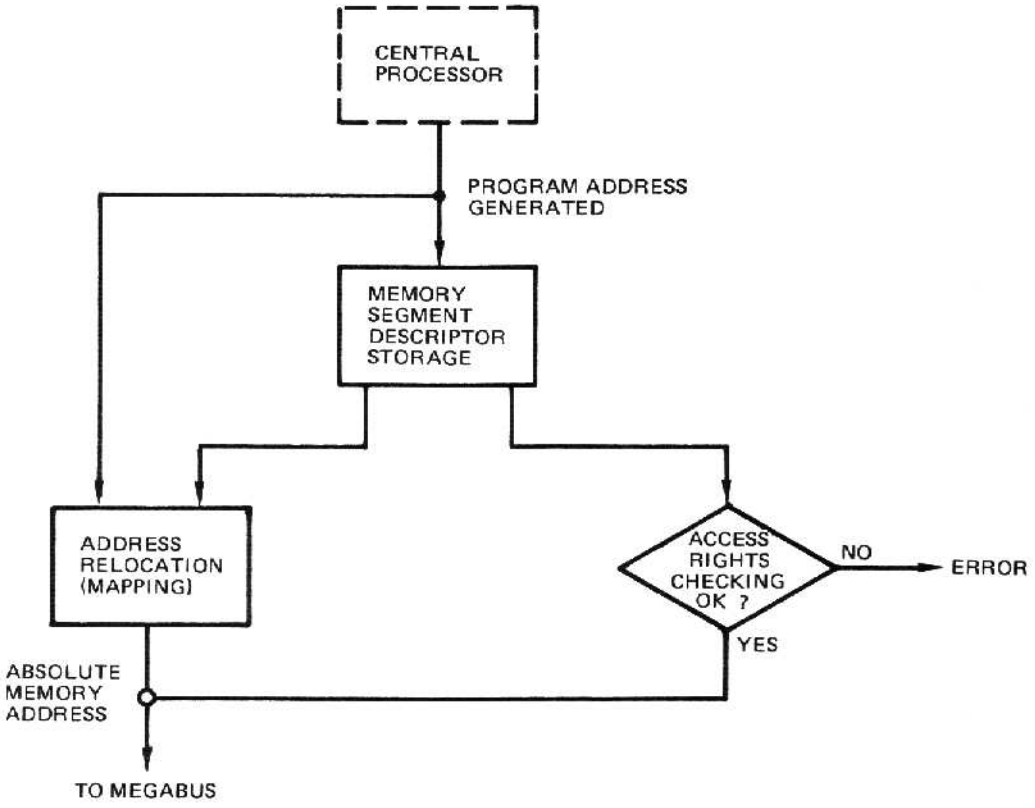


Figure 2-14 Memory Management Unit Block Diagram

2.2.3 Main Memory

Main memory consists of various controllers and memory adapters selected by the user which allows memory to be easily configured from a minimum of 16 kilowords to a maximum of one megawords. Two types of storage media are available: (1) Metal Oxide Semiconductor (MOS) and (2) core storage. The MOS memory is economical, reliable, and the standard storage media for the system. A battery backup option is available for data retention during power failures. Core memory requires no battery backup to retain stored data during power losses and can replace or be intermixed with MOS memory in a system. Memory options are listed in subsection 2.3.2.

2.2.3.1 MOS Memory

A variety of MOS memories are available. Offered is a byte parity MOS memory which includes logic for storing and retrieving two bits of parity and a 16-bit data word per location. Also offered is an Error Detection and Automatic Correction (EDAC) MOS memory. EDAC memory handles a 16-bit data word plus six bits of error correction information per location.

Data integrity for byte parity memories is enforced by returning the stored parity bits to the unit reading memory. For EDAC memories, the supplied parity is used with the data word bits to develop and store the EDAC information bits. When it is read, memory attempts to correct any internally caused data errors, reporting the results over to dedicated Megabus lines. Uncorrectable errors are reported as RED errors, correctable errors are reported as YELLOW errors. EDAC memory is particularly desirable on large systems requiring increased reliability.

In addition to being either EDAC or byte parity, MOS memories are either double-word fetch or single-word fetch memories. Double-word fetch functionality allows a unit to request two consecutive words from memory with just one request.

MOS memories are constructed in either 8KW or 32KW memory storage modules which mount on full size controller boards. Up to four modules can be supported by one controller board (see Figure 1-11). There are separate controllers (either 32K or 128K) for 8KW and 32KW modules, respectively, and separate controllers and modules for EDAC and byte parity type memories.

A typical MOS memory controller is shown in Figure 2-15. The controller communicates with the rest of the system through the Megabus. All MOS controllers contain refresh logic which is used to maintain data and they also contain Quality Logic Test (QLT) logic which is used during initialization to verify hardware integrity of the memories. In addition, controllers support address parity checking on the eight most significant address lines on the bus for each memory access. When a controller detects an address error, it does not respond and a bus timeout results.

An optional memory save power supply (battery back up unit) is available for MOS memories. It supplies refresh voltage for data retention purposes to a pair of MOS controllers for up to two hours in the event of line power failure. Power circuits on the Megabus are separated to minimize the power drain. The battery back up unit continuously charges the batteries when ac line voltage is available and indicates when battery power is diminished beyond support capabilities during power losses.

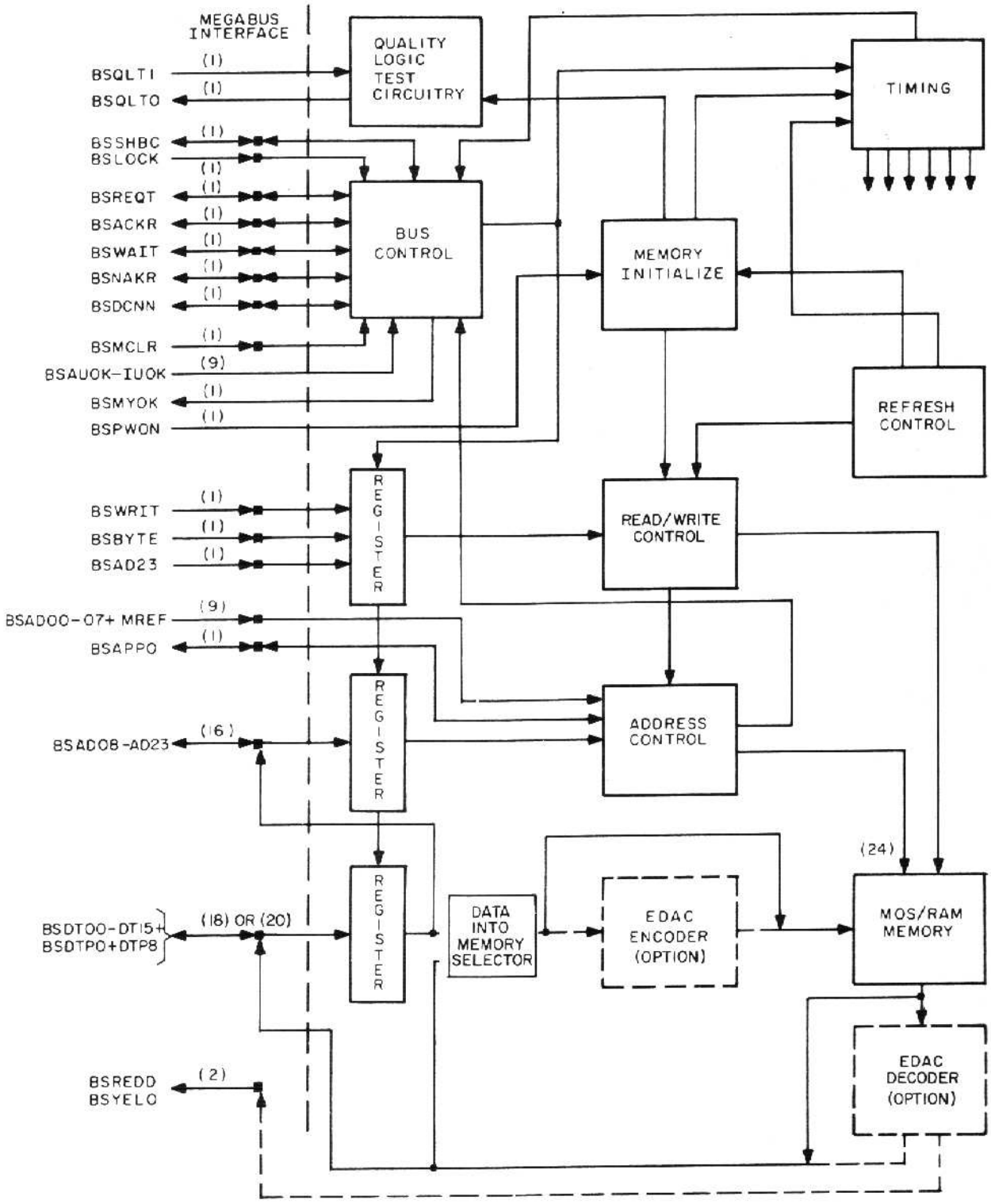


Figure 2-15 Typical Memory Controller Intermediate Block Diagram

2.2.3.2 Core Memory

Core memory is available as an option if maximum data retention is desired. Stored data remains unaltered in core memory regardless of the length of time power is removed from the system.

Core memory controllers and core modules are constructed as one unit and plug directly into the Megabus. The controller/module configuration comes in either a 16KW or 32KW unit. The core memory controllers only support single-word fetch and byte parity functionality. Address parity and QLT logic is supported by core memories.

2.2.4 System Megabus

The Megabus is the primary interconnecting link between the CPU, the memory, the device controllers, and any other optional controller configured in the system. The Megabus permits any two of the units to communicate with each other at a given time via a common signal path. Megabus communications are asynchronous, permitting units of different speeds to operate efficiently. Each unit attached to the Megabus contains all the control and timing logic necessary to use the bus without a central control unit of any kind.

The Megabus consists of 16 data lines, 24 address lines, 14 control lines, 9 integrity lines, and 10 tie breaking lines (refer to Table 2-2). Attachment to the Megabus is through plug-in board connectors (two per board slot) located at the rear of the system chassis, just forward of the power supply (see Figure 2-16). Two slot positions in each chassis are reserved for Megabus termination boards.

Table 2-2 Megabus Interface Signals (Sheet 1 of 2)

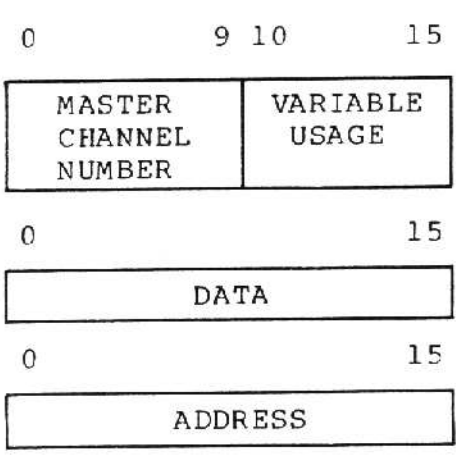
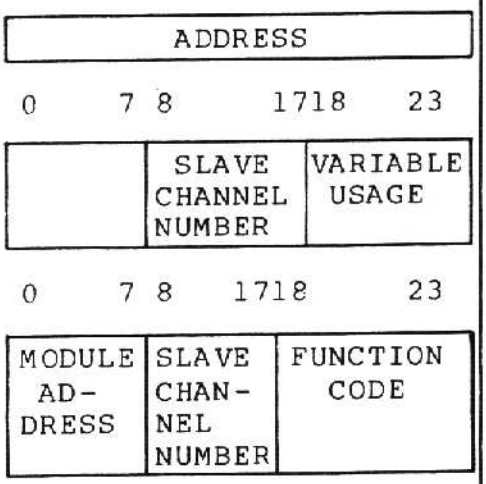
TYPE	FUNCTION	CLASS	BUS SIGNAL
Bus Control	Bus Request Data Cycle Now Acknowledge Negative Acknowledge Wait	Bus Timing	BSREQT- BSDCNM- BSACKR- BSNAKR- BSWAIT
Data Lines	Data Bit A (unused) Data Bit 0 Data Bit 1 Data Bit 2 Data Bit 3 Data Bit 4 Data Bit 5 Data Bit 6 Data Bit 7 Data Bit B (unused) Data Bit 8 Data Bit 9 Data Bit 10 Data Bit 11 Data Bit 12 Data Bit 13 Data Bit 14 Data Bit 15	Data Information (Formats) 	BSDT0A- BSDT00- BSDT01- BSDT02- BSDT03- BSDT04- BSDT05- BSDT06- BSDT07- BSDT0B- BSDT08- BSDT09- BSDT10- BSDT11- BSDT12- BSDT13- BSDT14- BSDT15-
Address Lines	Address Bit 0 Address Bit 1 Address Bit 2 Address Bit 3 Address Bit 4 Address Bit 5 Address Bit 6 Address Bit 7 Address Bit 8 Address Bit 9 Address Bit 10 Address Bit 11 Address Bit 12 Address Bit 13 Address Bit 14 Address Bit 15 Address Bit 16 Address Bit 17 Address Bit 18 Address Bit 19 Address Bit 20 Address Bit 21 Address Bit 22 Address Bit 23 (LSB)	Address Information (Formats) 	BSAD00- BSAD01- BSAD02- BSAD03- BSAD04- BSAD05- BSAD06- BSAD07- BSAD08- BSAD09- BSAD10- BSAD11- BSAD12- BSAD13- BSAD14- BSAD15- BSAD16- BSAD17- BSAD18- BSAD19- BSAD20- BSAD21- BSAD22- BSAD23-

Table 2-2 Megabus Interface Signals (Sheet 2 of 2)

TYPE	FUNCTION	CLASS	BUS SIGNAL
Transfer Control Lines	Memory Reference Byte (unused) Bus Write Second Half Read Lock (unused) Double Pull	Control Information Accompanying Transfer	BSMREF- BSBYTE- BSWRIT- BSSHBC- BSLOCK- BSDBPL-
	Memory Error (Red) Memory Error (Yellow) Data Parity Left Data Parity Right Address Parity (bits 0-7)	Integrity Information Accompanying Transfer	BSREDD- BSYELO- BSDP00- BSDP08- BSAP00-
Verify Bus Continuity	Logic Test Out Logic Test In Logic Test Active	Hardware Integrity	BSQLTO- BSQLTI- BSQLTA+
Establish Positional Priority	Tie-Breaking Network Tie-Breaking Network Tie-Breaking Network Tie-Breaking Network Tie-Breaking Network Tie-Breaking Network Tie-Breaking Network Tie-Breaking Network Tie-Breaking Network	Megabus Access Priority Control	BSAUOK+ BSBUOK+ BSCUOK+ BSDUOK+ BSEUOK+ BSFUOK+ BSGUOK+ BSHUOK+ BSIUOK+ BSMYOK+
Miscellaneous	Master Clear Power On Resume Interrupt Spare Line (unused) Spare Line (unused) Spare Line (unused) External Connection (unused)	Miscellaneous Control	BSMCLR- BSPWON+ BSRINT- BSSPR1- BSSPR3- BSSPR4- BSEXTC+

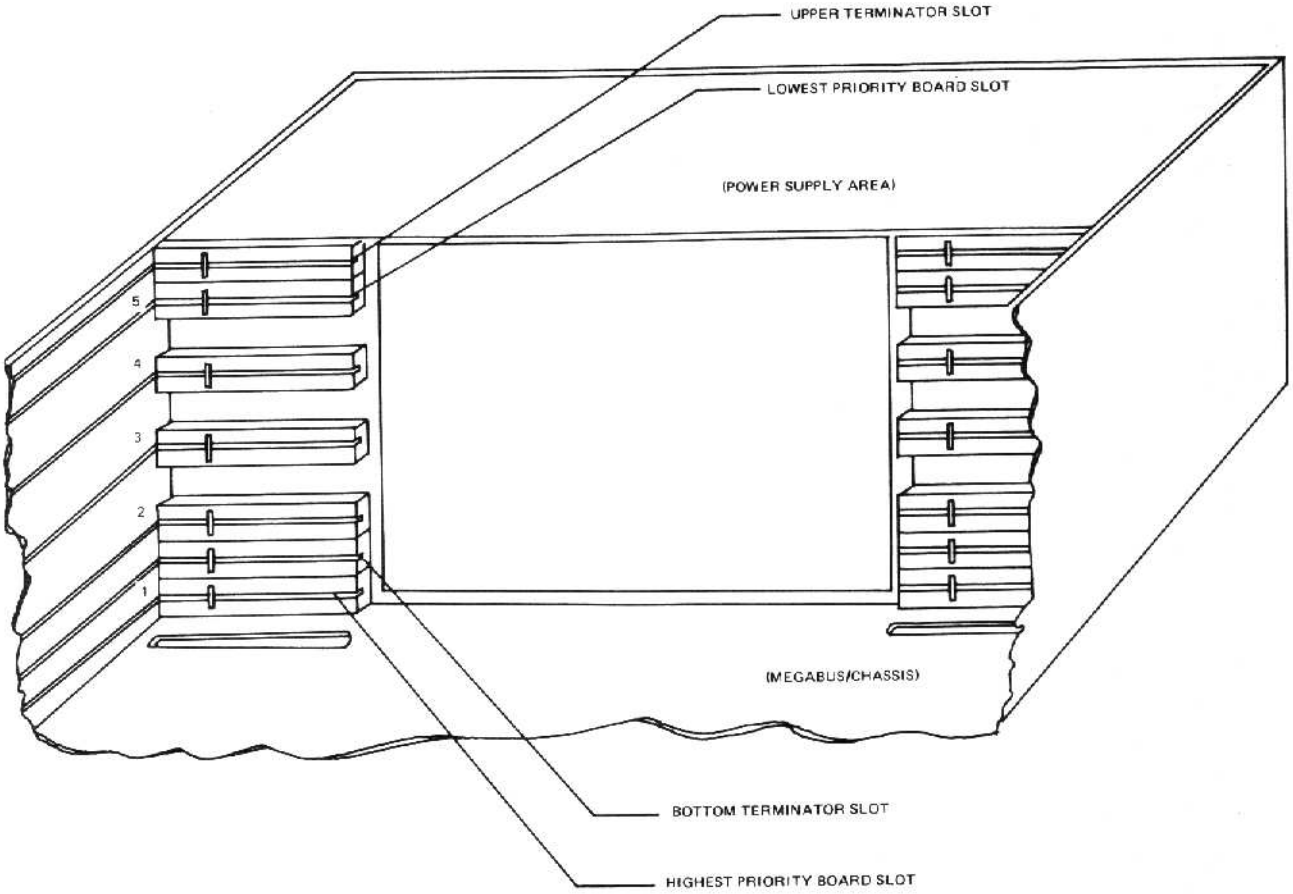


Figure 2-16 Megabus Chassis Connectors

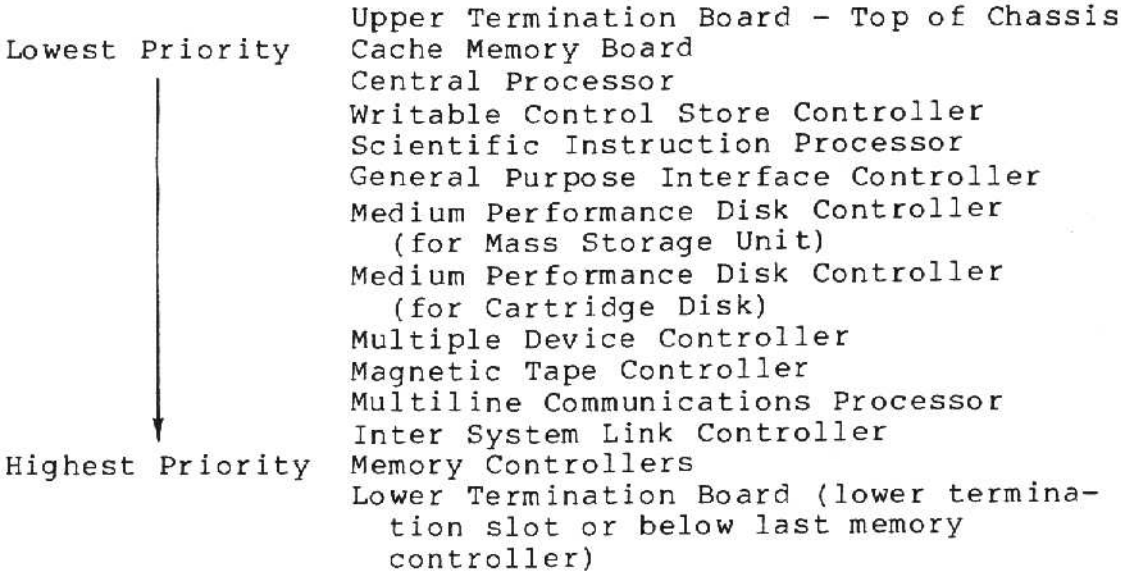
2.2.4.1 Chassis Priority

The system components plug into the Megabus on a priority basis. The priority is determined by the physical slot position occupied by each unit within the chassis. The lower the physical slot position within the chassis, the higher priority assigned the unit. Logic in each unit enforces this priority concept when granting Megabus cycles and resolving simultaneous requests.

Within the system, main memory is always inserted in the highest Megabus priority chassis slot (lowest physical position). The CPU is located at the top of the chassis and is assigned the lowest priority with one exception. If cache memory is configured in the system, cable restrictions require that the cache memory be installed in the board slot adjacent to and above the CPU (lower priority). The WCS option always occupies the slot just below the CPU if it is installed in the system. All other

components are inserted in the Megabus according to their transfer rates. Components with faster transfer rates are inserted in the chassis slots with higher Megabus priority assignments.

The recommended priority order for board positions is as follows:



The Megabus supports up to 23 controller slots. Expanding the Megabus beyond a single chassis is done through bus jumper cables. Figure 2-17 illustrates how chassis priority is maintained with the expansion chassis.

2.2.4.2 Megabus Operations

The Megabus is the primary path by which system components communicate with each other in order to execute software instructions. All Megabus operations are asynchronous and on a master/slave relationship. The unit transferring data is always the master unit, the receiving unit is the slave. Table 2-2 lists the Megabus lines. Figure 2-18 shows the data and address formats.

Any unit attached to the Megabus can become the master unit. For example: the CPU becomes the master unit when it transfers function commands to an I/O controller. The controller becomes the master unit when it independently writes memory or requests a memory read or it transmits an interrupt to the CPU. Memory is a slave when it is being written into. However, memory becomes a master when it returns read data to a requesting unit.

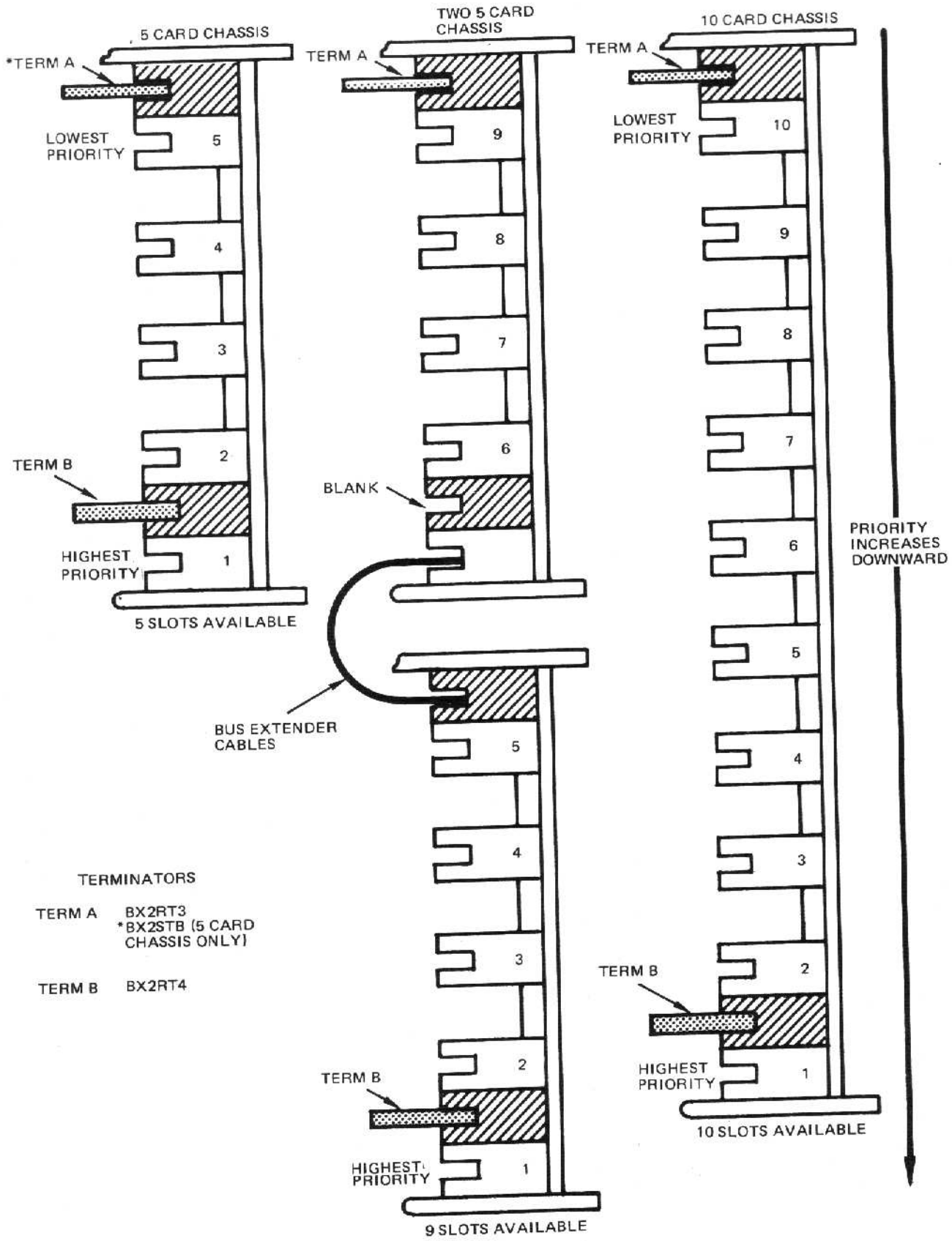


Figure 2-17 Chassis Controller Board Slot Position (Side View)

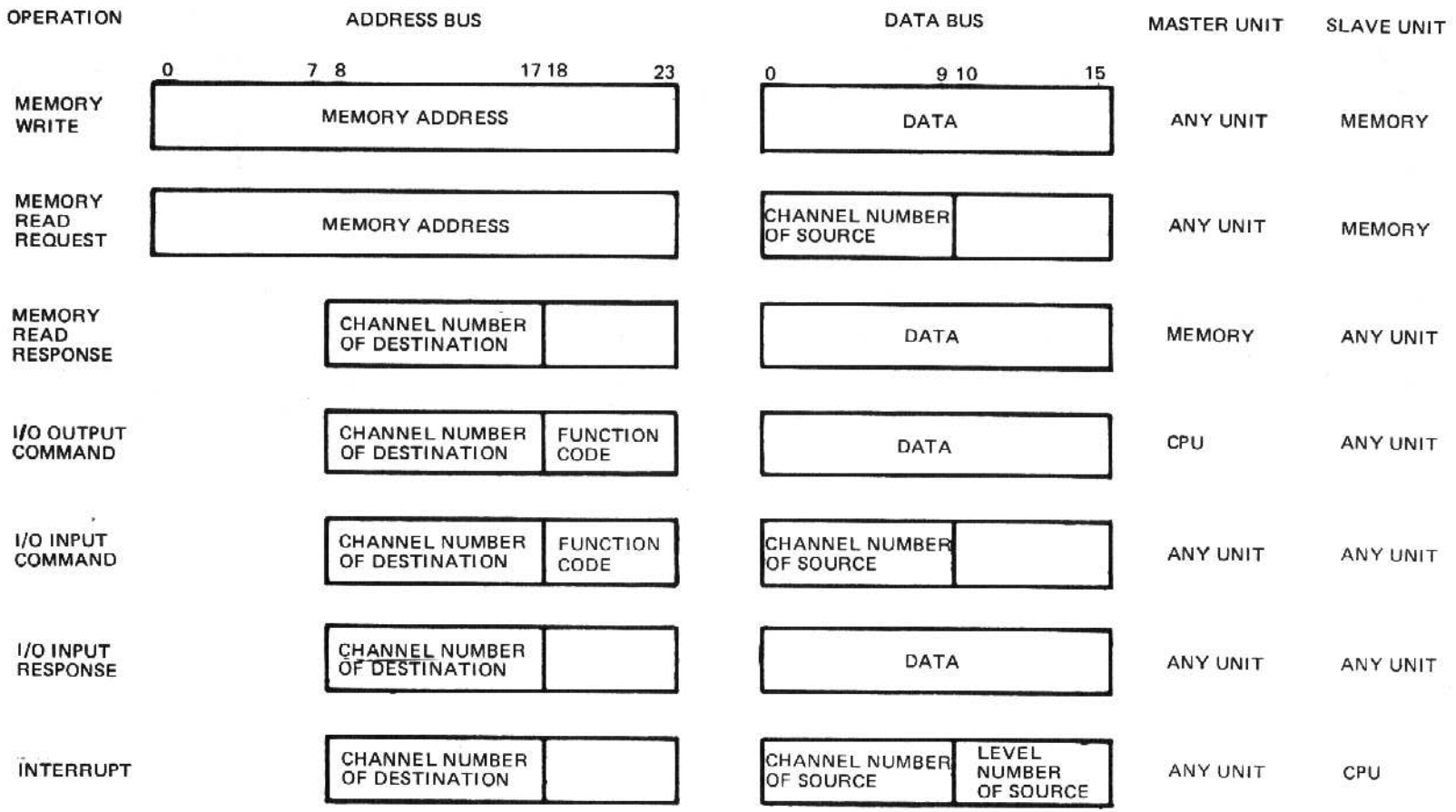


Figure 2-18 Address and Data Formats for Megabus Operations

Megabus operations are cyclical in nature. Any unit attached to the Megabus can request a bus cycle, and becomes a master unit when the request is granted. If two units simultaneously request a bus cycle, priority is granted according to the relative physical positions each unit occupies within the system chassis (refer to subsection 2.2.4.1). Some Megabus operations require more than one Megabus cycle. For example it requires two bus cycles for any unit to read memory; one cycle to request the read data, and a second cycle for memory to respond and transmit the data to the requesting unit. The following Megabus operations are possible:

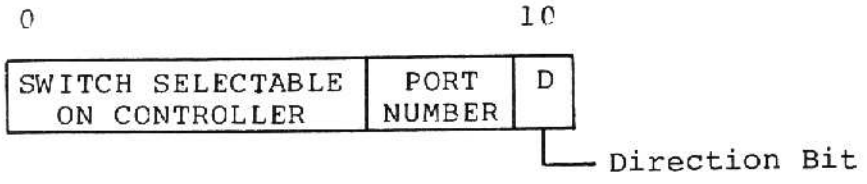
- Memory Write
- Memory Read
- I/O Output Command
- I/O Input Operation
- I/O Direct Memory Access
- I/O Interrupt

2.2.4.2.1 Channel Numbers

Since the Megabus is a common communications path between system components, unique channels exist for each unit attached to the system. Channel numbers identify the channel assigned to each peripheral device, communication line, central processor, or any end controller (i.e., WCS, SIP, cache memory) attached to the system with the exception of main memory, which is identified only by a memory reference address. The logical capacity of the system is 1024 channels.

Channel numbers are used by software to identify to which channel it wishes to direct an I/O instruction. Hardware uses the channel number to steer data transfers to the specified units and to determine the direction of I/O transfers. Odd numbered channels are assigned to output devices, even numbered channels are assigned to input devices. Every end unit is assigned two channel numbers, even though both are not always used. For example, the printer is ony an output device. Thus, only its odd channel number is used.

Channel numbers are assigned to each end unit by hardware switches and physical device connections. Each channel number is a 10-bit value. Of these, the high order bits are assigned by a switch located on the controller board and are easily field changeable. The low order bits are determined by the physical location (port) the adapter board occupies on the controller. The least significant bit is the direction bit, odd for output, even for input. A typical MDC device channel address is shown in the following illustration.



2.2.4.2.2 Memory Write Megabus Operation

It requires one Megabus cycle for any unit to store a word in memory. The unit requests a bus cycle and when granted the request, becomes the master unit. The master places the data and memory address on the Megabus along with the write and memory reference signals. The memory (slave) recognizes the write and memory reference signals and responds by writing the data in the specified location.

2.2.4.2.3 Memory Read Megabus Operation

A memory read operation requires two Megabus cycles; a read request cycle and a read response cycle. During a read request cycle the requesting unit is the master and the memory is the slave. When the requesting unit is granted the bus, it places its channel number on the data lines and the memory address on the address lines, along with a memory reference signal. The memory responds by storing the channel address of the requesting unit and enters its own access cycle to obtain the data specified by the address lines. After memory retrieves the data it issues a second half read response cycle. During this Megabus cycle the memory is the master unit and the unit requesting the data becomes the slave. The memory places the channel number of the requesting unit on address lines and the retrieved data on the data lines. The slave unit recognizes its channel number and responds by strobing the read data off the bus to complete the operation.

2.2.4.2.4 I/O Output Command Operation

During the execution of an I/O instruction the CPU may be required to transfer several words of information to a specific I/O device, taking one Megabus cycle to transfer each word. The CPU sends a word of information together with a channel address and function code defining what that word of data is. Typical words that must be transferred are task words identifying the operation to be performed, configuration words indicating the interrupt level assigned to the device, addresses showing the initial location I/O transfers must start at, and range words specifying the number of words or bytes to be transferred.

During this type of Megabus operation the CPU is the master unit. When granted the Megabus, the CPU places on the address lines the channel address of the unit it wishes to communicate with along with the function code. The data word if required, is placed on the data lines. The specified I/O controller recognizes its channel number and responds by strobing the function code and data from the bus. The I/O controller then performs the required action to complete the operation.

2.2.4.2.5 I/O Input Operation

The execution of some I/O instructions requires that the CPU or other processors obtain status information from a controller or I/O device. This type of operation requires two Megabus cycles for each word transferred; a read request and a read response cycle. During the read request cycle the processor is the master unit and initiates the read request cycle. The master unit supplies its channel number on the data lines and places on the address lines the channel number of the processor. After the slave unit assembles the required data it becomes the master by initiating the read response cycle. In this second half cycle, the stored channel number of the processor is placed on the address lines along with the requested data lines. The requesting processor recognizes its channel address and strobes the data information from the bus to complete the operation.

2.2.4.2.6 I/O Controller Direct Memory Communications

All I/O transfers in the system occur in the Direct Memory Access (DMA) mode. Once a controller has been conditioned by the central processor, controller input/output transfers are executed via the bus independent of the central processor. When a controller wants to input a word to memory, it becomes the master and initiates a write Megabus cycle transmitting the data and the memory address to memory. If an I/O controller is connected to an output device and wants to receive a word from memory, it initiates a read request cycle informing memory of the channel requesting the data. Then after memory has accessed the data, a half bus cycle (read response) is initiated to the requesting channel with the memory as the master and the controller as the slave.

2.2.4.2.7 Megabus Interrupt Cycle

The Megabus interrupt cycle is initiated by a controller when it wants to inform the central processor of a certain condition (typically the end of a data block transfer). Each channel operates at some software assigned interrupt level. This level is previously transferred to the controller with I/O command cycles. In the interrupt cycle, the interrupting device places it channel number and its interrupt level on the data lines together with the central processor's channel address on the address lines for transfer to the central processor. The CPU on recognizing its channel address, strobes the interrupt level from the bus. If the level number of the interrupting device is numerically lower (higher priority) than the current level of the CPU, an interrupt occurs. If not, the CPU rejects the interrupt informing the controller to reissue the interrupt cycle only when the CPU signals a priority change is occurring.

2.2.5 Peripheral Devices

The peripheral devices in the system interface with the CPU and memory via the Megabus through controller boards and adapter boards. The controller boards plug directly into the Megabus and control the interface between the controller and other units connected to the Megabus. The adapter boards mount on the controllers and mate specific devices to the controller. There are three primary peripheral controllers: (1) Multiple Device Controllers (MDC), (2) Magnetic Tape Controllers (MTC), (3) Medium Performance Disk Controllers (MPDC).

The MDC and specific adapters interface the following devices to the system:

- Serial Printers:

  PRU9101 (60 lpm, 64-character ASCII set)
  PRU9102 (60 lpm, 96-character ASCII set)

- Line Printers:

  PRU9103 (240 lpm, 96-character ASCII set)
  PRU9104 (300 lpm, 64-character ASCII set)
  PRU9105 (440 lpm, 96-character ASCII set)
  PRU9106 (600 lpm, 64-character ASCII set)
  PRU9108 (660 lpm, 96-character ASCII set)
  PRU9109 (900 lpm, 64-character ASCII set)
  PRU9112 (120 cps, 96-character ASCII set)
  PRU9114 (67 lpm, 96-character ASCII set)

- Card Readers:

  CRU9101 (300 cpm, PDI Punched Card Reader)
  CRU9102 (300 cpm, PDI Punched and Mark Sense Card Reader)
  CRU9103 (500 cpm, PDI Punched Card Reader)
  CRU9104 (500 cpm, PDI Punched and Mark Sense Card Reader)
  CRU9108 (300 cpm, CR500 Punched Card Reader)
  CRU9109 (300 cpm, CR500 Punched and Mark Sense Card Reader - IBM Mode)
  CRU9110 (300 cpm, CR500 Punched and Mark Sense Card Reader - HIS Mode)
  CRU9111 (500 cpm, CR500 Punched Card Reader)
  CRU9112 (500 cpm, CR500 Punched and Mark Sense Card Reader - IBM Mode)
  CRU9113 (500 cpm, CR500 Punched and Mark Sense Card Reader - HIS Mode)

- Card Punch:

  PCU 9101 (100 - 400 cpm, Card Punch)

- Card Reader/Punch:

  CCU9101 (400 cpm/100 - 400 cpm, Card Reader and Punch)

- Diskette Devices:

  DIU9101 (Single Diskette, 125 KW)
  DIU9102 (Dual Diskette, 250 KW)

- Consoles:

  ASR33 Teletype Console:

    TTU9101 (Without Autoshutdown)
    TTU9103 (With Autoshutdown)

  KSR33 Teletype Console:

    TTU9102 (Without Autoshutdown)
    TTU9104 (With Autoshutdown)

  CRT (TTY) Keyboard Console:

    DKU9101 (64-Character Set)
    DKU9102 (96-Character Set)
    DKU9103 (CRT Console, 64-Character Set)
    DKU9104 (CRT Console, 96-Character Set)

  Keyboard Typewriter Console (KSR)

    TWU9101 (30 cps, TTL, with keypad, 64-Character Set)
    DWU9104 (30 cps, MOS, 96-Character Set)
    TWU9106 (120 cps, MOS, 96-Character Set)

The MTC controller and specific adapters interface to the system the same devices listed above plus the following tape devices:

- Magnetic Tape Drives:

  MTU9104 (9-Track NRZI, 800 bpi, 45 ips)
  MTU9105 (9-Track NRZI, 800 bpi, 75 ips)
  MTU9109 (9-Track NRZI PE, 800/1600 bpi, 45 ips)
  MTU9110 (9-Track NRZI, PE, 800/1600 bpi, 75 ips)
  MTU9112 (7-Track NRZI, 556/800 bpi, 45 ips)
  MTU9113 (7-Track NRZI, 556/800 bpi, 75 ips)
  MTU9114 (9-Track PE, 1600 bpi, 45 ips)
  MTU9115 (9-Track PE, 1600 bpi, 75 ips)

The MPDC and specific adapters interface the following devices to the system:

- Cartridge Disk Units:

  CDU9101 (Low Density, One Removable Disk, 1.25 MW)
  CDU9102 (Low Density, One Removable and One Fixed Disk, 2.5 MW)
  CDU9103 (High Density, One Removable Disk, 2.5 MW)
  CDU9104 (High Density, One Removable and One Fixed Disk, 5.0 MW)
  CDU9113 (Low Density, One Removable Disk, 1.25 MW)
  CDU9114 (Low Density, One Removable and One Fixed Disk, 2.5 MW)
  CDU9115 (High Density, One Removable Disk, 2.5 MW)
  CDU9116 (High Density, One Removable and One Fixed Disk, 5.0 MW)

- Mass Storage Units:

  MSU9101 (40 MB Drive)
  MSU9102 (80 MB Drive)
  MSU9103 (143 MB Drive)
  MSU9104 (288 MB Drive)

The Multiline Communications Processor and its specific adapters can handle up to eight full duplex communications lines. These lines can be connected to remote terminals, modems, data sets, and can be used to connect a host processor to the system. The peripheral devices associated with the communication processor are as follows.

- Asynchronous Terminals:

  VIP7100 (CRT/keyboard, up to 9600 baud)
  VIP7200 (CRT/keyboard, with cursor control, line editing and buffered transmission, up to 9600 baud)
  VIP7205 (CRT/keyboard/display terminal, 96-character set)
  TWU1001 (Keyboard/printer 30 cps)
  TWU1003 (Keyboard/printer 30 cps)
  TWU1005 (Keyboard/printer 120 cps)
  PRU1001 (Printer Terminal 30 cps)
  PRU1003 (Printer Terminal 30 cps)
  PRU1005 (Printer Terminal 120 cps)

- Synchronous Terminals:

  VIP7700R (Nonpolled CRT/keyboard with optional ROP; 2000 to 4800 baud)
  VIP7700R (Polled CRT/keyboard with optional ROP; 2000 to 4800 baud)
  VIP7760-2A (Polled CRT/keyboard with optional ROP; 2000 to 4800 baud)

VIP7700 (Nonpolled CRT/keyboard with optional ROP; 2000 to 4800 baud)
VIP7700 (Polled CRT/keyboard with optional ROP; 2000 to 4800 baud)

- Receive-only printer for CRT terminals:

TN300 (Printer Terminal 30 cps)
TN1200 (Printer Terminal 120 cps)
PRU1001 (Printer Terminal 30 cps (available on VIP7100 and VIP7200 only))
PRU1003 (Printer Terminal 30 cps)
PRU1005 (Printer Terminal 120 cps)

2.2.6 Central System Power Supply

The central system power supply provides regulated +5Vdc, +12Vdc, -12Vdc to the adapter/controller boards plugged into the Megabus. One power supply is required for each five Megabus slots (i.e., a 10-slot chassis requires two power supplies). These power supplies are located at the rear of the system chassis (see Figure 1-8). Current requirements of the boards installed in the associated chassis slots require a Type M170 (70 amp) power supply.

Primary ac source power (120 Vac, 60 Hz) is provided through a three-wire cord which plugs into a filtered ac outlet on the power distribution unit for rack and office furniture package systems. On tabletop systems the power supply cord can plug directly into a 115 Vac outlet or into a switch controlled ac outlet on either the optional tabletop memory save unit or the tabletop diskette peripheral unit.

2.2.7 Power Distribution Unit

The Power Distribution Unit (PDU) provides single phase 115 Vac source power to all central system power supplies and all other units within a single system cabinet. One PDU is required for each cabinet configured in the system. The PDUs can be ganged together to permit all system components to be powered up with one switch. Each PDU contains several switched and unswitched ac outlets into which the units within the cabinet (requiring ac power) plug into. If a memory save unit is installed in the cabinet, it is always plugged into an unswitched ac outlet on the PDU. This ensures the memory save unit is continually energized.

All outputs of the PDU are filtered to reduce the noise on the ac line.

Six types of PDUs are available to connect to different input voltages (refer to subsection 1.4.1). The PDU is always located at the bottom front of the system cabinet rack for both the rack-mountable and office furniture package system. No PDU is required for a tabletop system.

2.3 SYSTEM OPTIONS

In addition to the cabinetry selected by the user, the options available for the system can be divided into the following categories:

- System/Processor Options
- Memory Options
- Peripheral Controller Options
- Special Options.

Subsections 2.3.1 through 2.3.4 explains the options in each category.

2.3.1 System/Processor Options

The following optional components are described in this subsection.

- Memory Management Unit
- Scientific Instruction Processor (SIP)
- Writable Control Store (WCS)
- Intersystem Link (ISL).

2.3.1.1 Memory Management Unit Option

The memory management unit is only optional for the Model 43 system, it is standard on the Model 53 system. The MMU is physically located on the CPU adapter (BF4MMU) and is briefly described in subsectrion 2.2.2.2. A detailed description of the MMU is contained in the Type CPF 9501 Memory Management Unit Manual, Order Number FN34.

2.3.1.2 Scientific Instruction Processor (SIP) Option

The SIP is physically contained on a single board which plugs into the Megabus. It enables scientific instructions to be executed by a central processor. The SIP executes floating point commands which are issued to it over the Megabus by the central processor. the CPU generates these commands by interpreting scientific instructions which it obtains from main memory during program execution.

The SIP operates as an attachment to a single CPU. Systems with multiple CPUs must have a separate SIP associated with each CPU that is to execute scientific instructions. Unique channel numbers are assigned to multiple CPUs and associated SIPs.

The general characteristics of the SIP are as follows:

- 32- and 64-bit operands
- 16M bytes of directly addressable main memory

- Three 64-bit software visible scientific accumulators
- Parallel execution with the CPU
- Direct communication with CPU registers with implicit floating point/integer conversion
- Full complement of calculation instructions
- Full (dual sense) branch instruction set
- Support of Level 6 trap functionality.

Figure 2-19 is a block diagram of the SIP. For an explanation of each block, refer to the Model 43 Scientific Instruction Processor Manual, Order Number FN30.

2.3.1.3 Writable Control Store (WCS) Option

The WCS options permit the user to add to the standard CPU instruction set, custom instructions that can be tailored to specific needs. This option allows the central processor to execute user defined instructions that direct hardware operations according to firmware that is created by the user and stored in the WCS. The WCS provides up to 2K of additional firmware storage that can be altered by program instructions. When a user defined instruction is encountered during program execution, firmware stored in the WCS directs the custom hardware operations necessary to execute the instruction.

Firmware coded by the user to implement the custom instructions is loaded into WCS storage via the Megabus using standard I/O instructions. A private interface between the CPU and WCS provides a direct path to the CPU for execution of custom firmware, when a user defined instruction is to be executed.

The WCS option consists of a WCS controller board that plugs into the Megabus, one or two (1K locations by 64 bit) RAM storage boards mounted on the controller, and a Micro Code Analyzer (MCA) that can be temporarily installed in the system (see Figure 2-20). The MCA is a diagnostic tool that is self contained and external to the card chassis and contains its own control panel (see Figure 2-21). The MCA is used as a diagnostic aid when debugging user coded firmware. For more information, refer to the Writable Control Store Product Manual, Order Number FN67 and the User's Guide, Order Number FQ41.

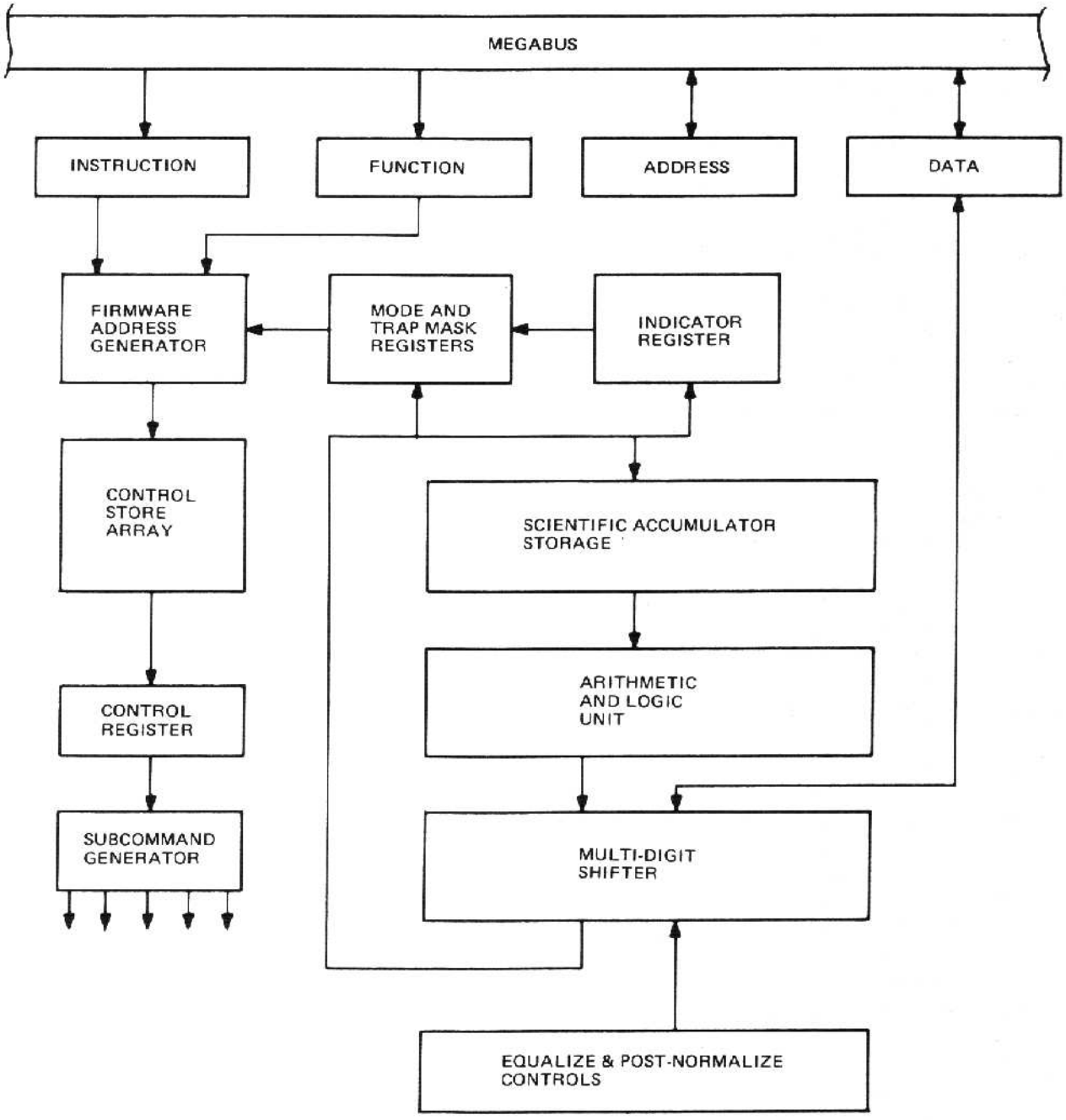


Figure 2-19 SIP Functional Block Diagram

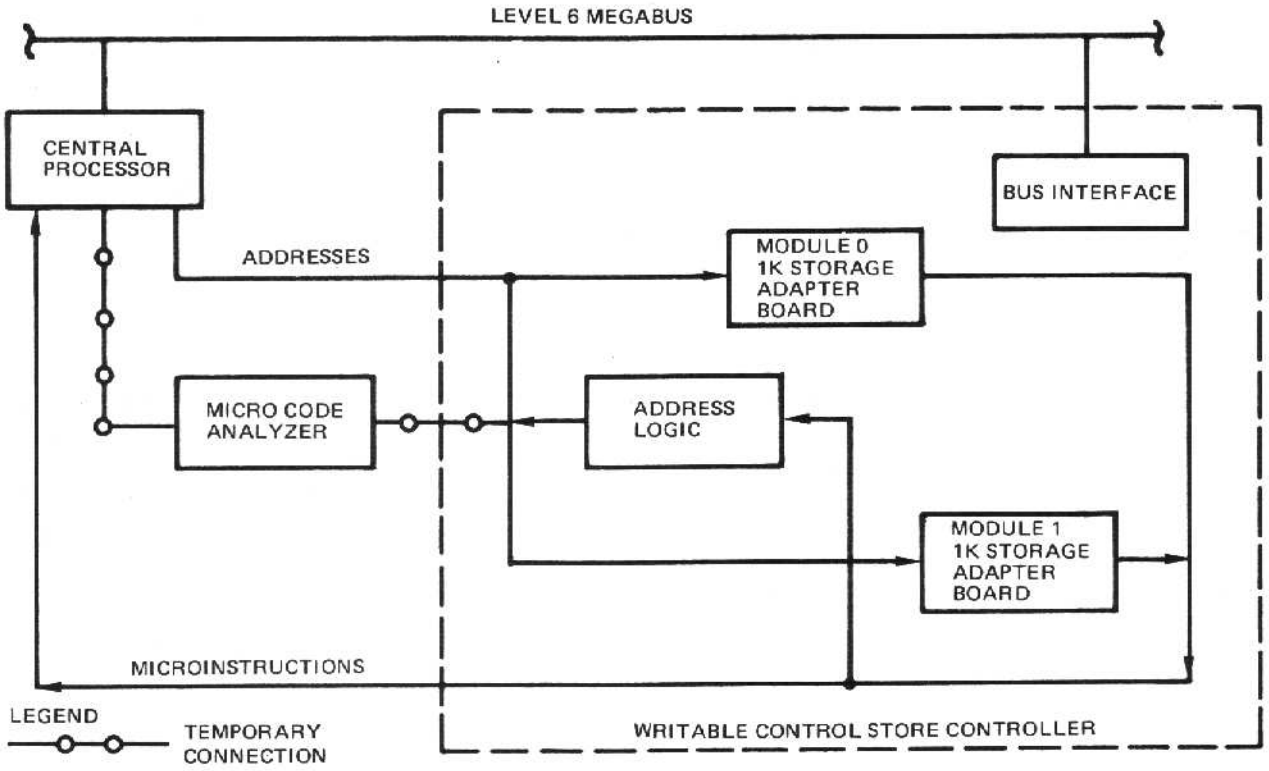


Figure 2-20 Writable Control Store Option Block Diagram

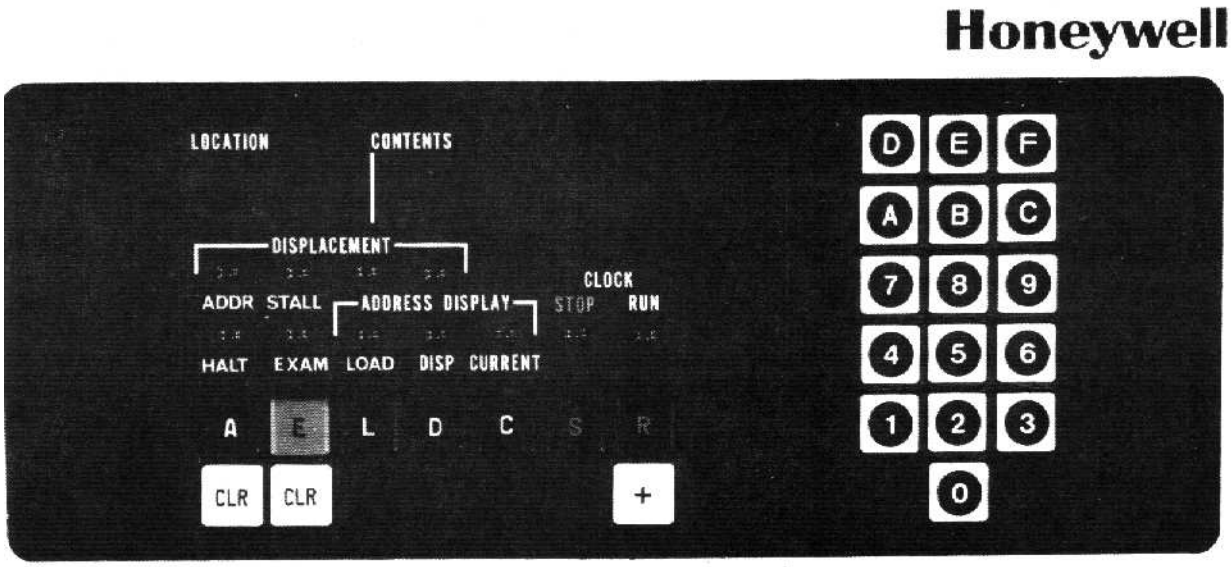


Figure 2-21 Micro Code Analyzer Front Panel

2.3.1.4 Intersystem Link (ISL) Option

The ISL option permits the interconnection of two separate system Megabuses, thereby providing a common path for data and control information between system components (CPU, memory, or I/O controllers) attached to one Megabus with system components attached to the other Megabus. Figure 2-22 shows how two identical (twin) ISL components link two buses together.

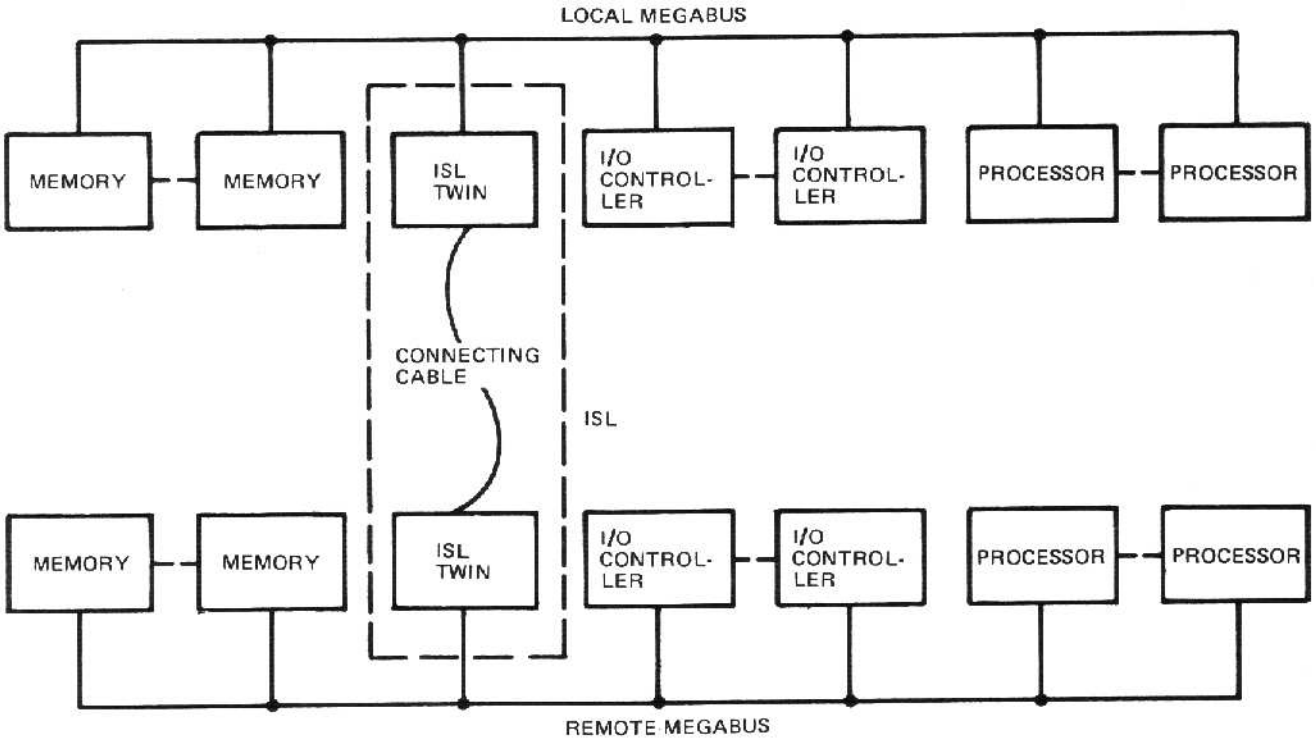


Figure 2-22 Intersystem Link Connecting Two Megabuses

The ISL consists of two identical controllers plus interface adapter boards interconnected by cables. The cables can be up to 25 feet in length. One controller board with its full-sized interface board plugs into a slot in one Megabus, the other twin controller board combination plugs into a slot in the other Megabus. The interconnection is by cables to the identical adapter boards mounted on each controller.

The ISL allows each controller to pass memory references, I/O commands, or interrupts from one bus to the other. Each ISL controller is configured to respond to certain memory addresses and certain channel numbers of components on each Megabus. During system operation, each ISL controller monitors all bus traffic and responds to individual bus request cycles within its range on behalf of the actual unit to which the cycle was directed. When

an ISL controller responds to a bus cycle for a unit attached to the other Megabus, it passes the information to the other twin controller which in turn reinitiates the bus request cycle on the opposite bus. The response cycle from the unit, if any, follows the same route in the reverse direction and is finally routed to the originating unit. The originating unit is always on the local bus. The receiving unit is on the remote bus. Either controller can be on the local or remote bus at different times.

Except for configuration, the ISL option has minimal software visibility. The intent is that the ISL will be transparent, and thereby permits components on one Megabus to communicate with components on the other Megabus as if there is only one Megabus. For more information, refer to the Level 6 Intersystem Link Manual, Order Number FN78.

2.3.1.5 Multiline Communications Processor Option

The Multiline Communications Processor provides the interface between the Megabus and the communication devices. It is a firmware controlled processor which can have up to four adapters mounted on it so that different communications lines can be connected to it. The Multiline Communications Processor can control up to eight full or half duplex communication lines which can be either synchronous or asynchronous. Listed below are the adapter boards which can be attached to the Multiline Communications Processor. For more information refer to the Type MLC9103 Multiline Communications Processor Manual, Order Number FL48. Figure 2-23 shows a typical application.

DCM9101 Communications Adapter Board - 2 asynchronous lines up to 9.6KB each
DCM9102 Communications Adapter Board - 1 asynchronous line up to 9.6KB
DCM9103 Communications Adapter Board - 2 synchronous lines up to 10.8KB each
DCM9104 Communications Adapter Board - 1 synchronous line up to 10.8KB
DCM9105 Communications Adapter Board - 1 broadband line up to 72KB (Bell 301, 303 compatible)
DCM9106 Communications Adapter Board - 1 synchronous HDLC line up to 10.8KB
DCM9108 Communications Adapter Board - 1 broadband line up to 72KB (CCITT - V35 compatible)
DCM9109 Communications Adapter Board - 1 synchronous line up to 10.8KB (MIL 188C compatible)
DCM9111 Communications Adapter Board - 1 line for current loop connection up to 9.6KB
DCM9114 Communications Adapter Board - 2 lines for current loop connection up to 9.6KB
DCM9110 Communications Adapter Board - autocall unit for 1 or 2 synchronous or asynchronous lines

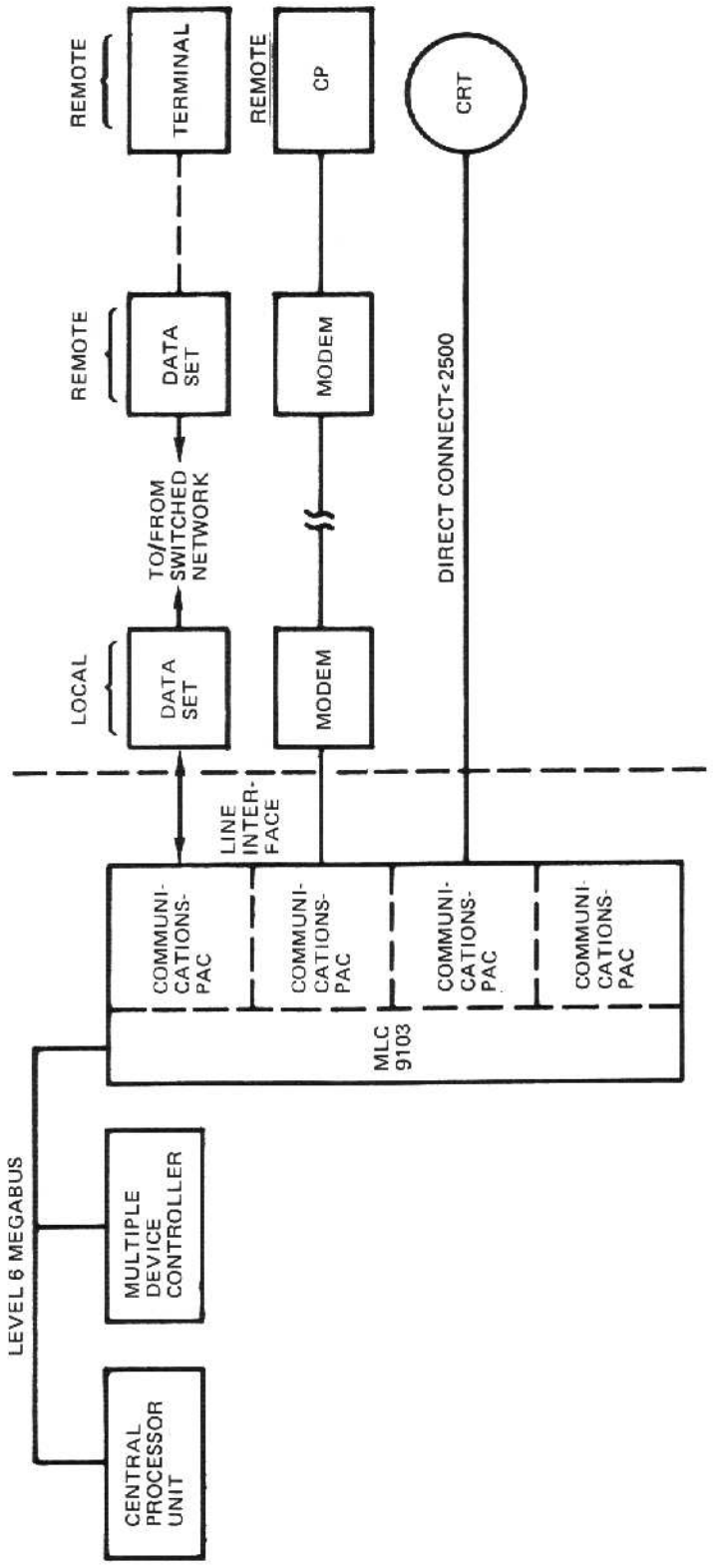


Figure 2-23 Multiline Communications Processor Configuration

2.3.2 Memory Options

Main memory is a separate item in the system and a variety of controllers and Memory-Pacs are available which allows memory to be configured from a minimum of 16KW to a maximum of 1028KW. Table 2-3 lists the memory controllers and their associated Memory-Pacs for these systems. A minimum of 16KW must be configured in the system and two types of memories are available: MOS memory and core memory.

MOS memory controllers are either single-word fetch or double-word fetch and are either byte parity (18 bits/location) or EDAC (22 bits/location) types. MOS memory is expanded by adding controllers and Memory-Pacs to the system until the desired number of locations is reached. The Memory-Pacs are either 8KW or 32KW locations and are different for parity and EDAC memory and require different controllers. A maximum of four Memory-Pacs can be attached to one controller. 32K controllers support 8KW Memory-Pacs, 128KW controllers support 32KW Memory-Pacs. If 32K controllers are used, memory can be expanded to 256KW locations. If 128KW controllers are used, memory can be expanded to 1028KW (two megabytes). Single-word fetch controllers permit memory to be expanded in single Memory-Pac (8KW or 32KW) increments. Double-word fetch controllers require memory to be expanded, two Memory-Pacs at a time i.e., in 16KW or 64KW increments.

Core memory can replace MOS memory with the advantage that data is retained when power is lost. Core memory is expanded by adding core controllers to the Megabus. Core memory controllers can contain either 16KW or 32KW core modules and are only single-word fetch controllers.

An optional memory save power supply is available to ensure data retention of up to two hours for two MOS controller boards. Refer to subsection 2.3.4.1.

2.3.3 Peripheral Controller Options

The optional peripheral controllers available for the Model 43 and Model 53 Systems are:

- MDC9101 Multiple Device Controller (MDC)
- MTC9101 Magnetic Tape Controller (MTC)
- MSC9101 Medium Performance Disk Controller (MPDC)
- GIS9001 General Purpose Interface Controller (GPI)

The controllers and specific adapters that attach to them are used to interface the peripheral devices with the system Megabus and are listed in subsection 2.2.5. Because these controllers are optional, a system can have any combination of peripheral controllers in order to satisfy the user's needs. The following subsections provide a brief explanation of the controllers.

Table 2-3 Model 43 and Model 53 Memory Controllers and Memory-Pacs

TYPE		BOARD TYPE
	MOS MEMORY	
CMC9003 CMM9001	32K Single-Fetch Parity Controller 8KW Parity Memory-Pac for BF2MAP BF2MAP replaces (interchangeable with) BF4MBO BS2TA6 replaces (interchangeable with) BD2T36	BF2MAP BS2TA6
CMD9004 CMM9002	32K Single-Fetch EDAC Controller 8KW EDAC Memory-Pac for BF2MAE BF2MAE replaces (interchangeable with) BF4MB1 BF2TA4 replaces (interchangeable with) BD2T44	BF2MAE BS2TA4
CMC9501	32K Double-Fetch Parity Controller 8KW Parity Memory-Pac for BF2MCP (double-fetch memory is expanded in 16KW increments by adding two BS2TC6)	BF2MCP
CMC9502 CMM9502	32K Double-Fetch EDAC Controller 8KW EDAC Memory-Pac for BF2MCE (double-fetch memory is expanded in 16KW increments by adding two BS2TC4)	BF2MCE BS2TC4
CMC9009	128K Single/Double-Fetch Parity Controller 32KW Parity Memory-Pac for BF2MYP (double-fetch memory is expanded in 64KW increments by adding two BS2SH6)	BF2MYP BF2SH6
CMC9010	128K Single/Double-Fetch EDAC Controller 32KW EDAC Memory-Pac for BF2MYE (double-fetch memory is expanded in 64KW increments by adding two BS2SH4)	BF2MYE BS2SH4
	CORE MEMORY	
CMC9005	16KW Core Memory (IPI No. BCRM016A)	BX4CRM
CMC9006	32KW Core Memory (IPI No. BCRM032A)	BX4CRM

2.3.3.1 Multiple Device Controller

The Multiple Device Controller (MDC) is a hardware/firmware controller that provides control for the unit record devices on the system (see Figure 2-24). The MDC and the four adapters that can be mounted on it provide the interface necessary to allow the unit record devices to communicate with the rest of the system by way of the Megabus. The hardware on the MDC and the adapters are controlled by a ROS memory (i.e., firmware) that contains micro-programs designed to perform specific tasks with reference to the unit record devices such as:

- Execution of Megabus sequences
- Command decoding
- Data transfers to or from devices through adapters
- Manage status, interrupt and control storage for each device channel
- Direct general flow of command execution.

The adapters that can be plugged into the MDC are the card reader adapter, the diskette adapter, the printer adapter, and the console adapter. The adapters provide the necessary interface logic to mate the specific devices to the MDC. The MDC supports four adapter positions. The diskette adapter is double-size and occupies two adapter positions and controls one or two diskette devices. All other adapters are single size and control one device. The combination of adapters that appear on any given system are customer specific.

2.3.3.2 Magnetic Tape Controller

The Magnetic Tape Controller (MTC) provides the logic necessary to interface the Megabus with up to four magnetic tape drives. Attached in a fixed position is a double sized tape drive adapter board which mates the tape drives to the MTC controller. Different adapter boards are used for nine-track and seven-track devices. If less than four tape drives are connected to the MTC, two additional adapter board positions can be fitted with the unit record (i.e., card reader or printer) adapter boards and allows the MTC to control these devices. A maximum of four devices can be controlled by the MTC. See Figure 2-25. For additional information refer to the Type MTC9101 Magnetic Tape Controller Manual, Order Number FM88.

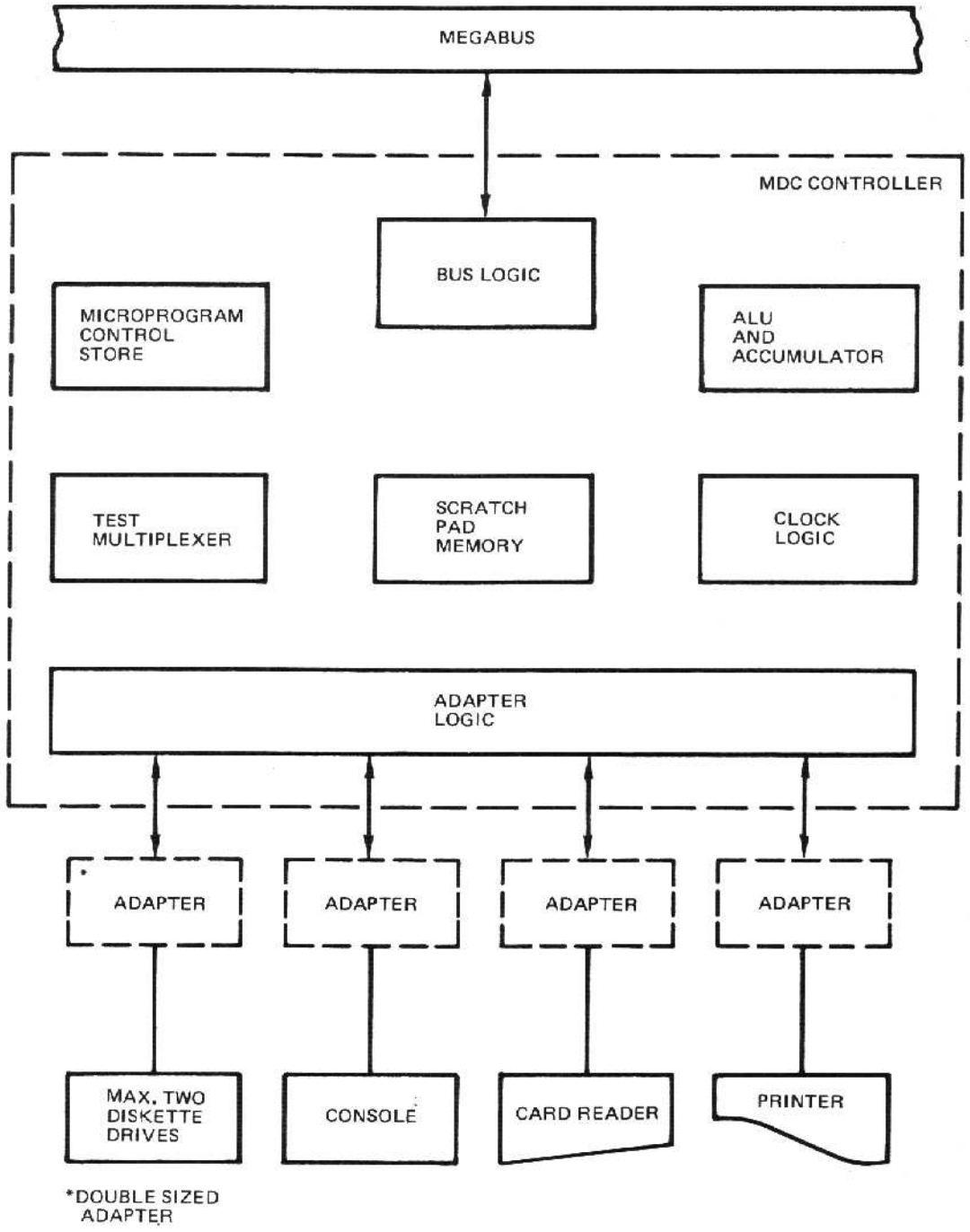


Figure 2-24 Multiple Device Controller Major Block Diagram

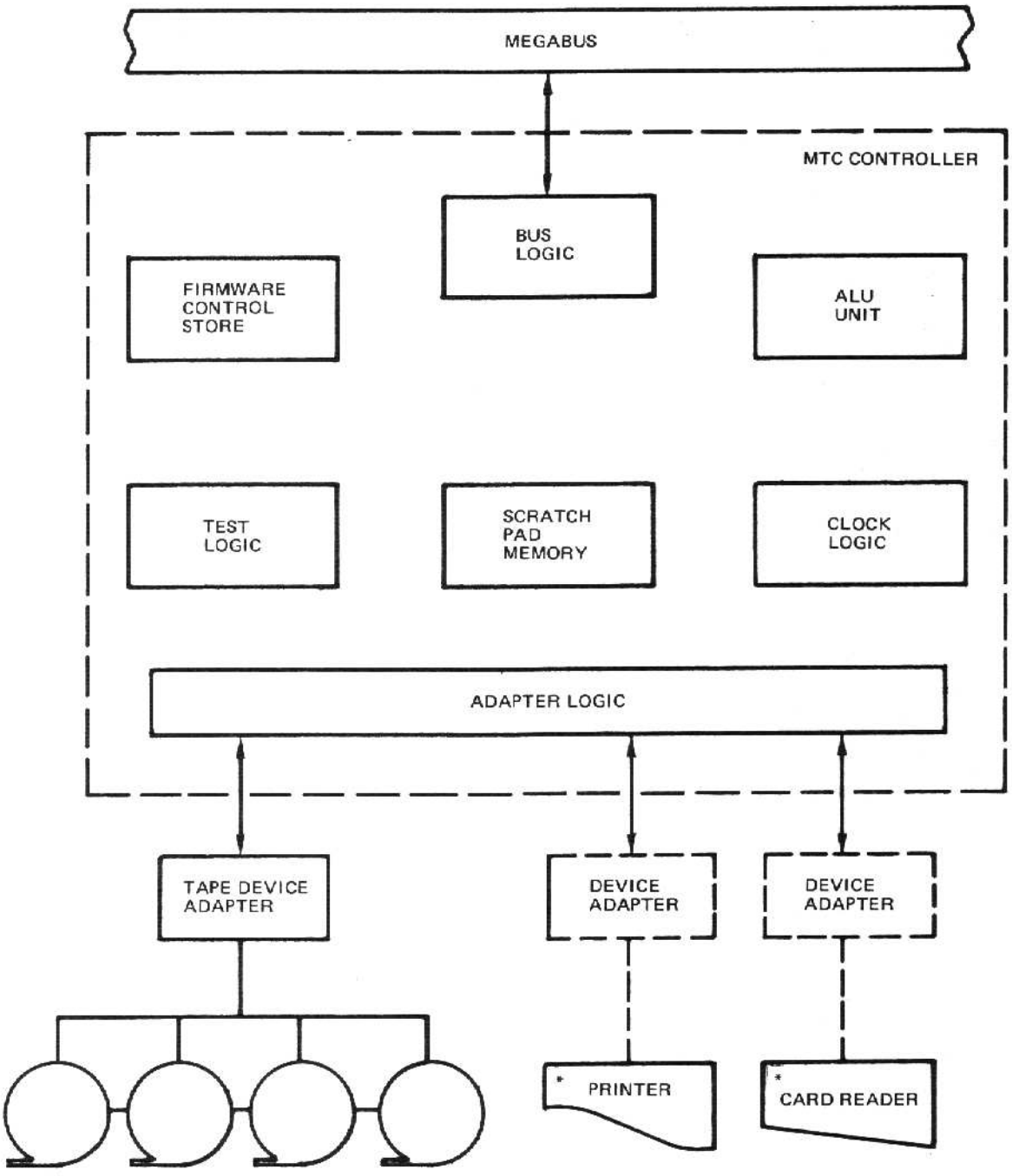


Figure 2-25 Magnetic Tape Controller Major Block Diagram

2.3.3.3 Medium Performance Disk Controller

The Medium Performance Disk Controller (MPDC) is a microprogrammed peripheral control subsystem that provides the systems with the facility to store and retrieve data from mass storage media. The MPDC is used to interface cartridge disk units or storage module units (mass storage units) to the Megabus. Attached to the MPDC are two adapters; (1) the ROS adapter, which contains the firmware microprogram instructions, and (2) the device adapter, which can handle a maximum of four daisy-chained devices. A specific set of adapters is used when cartridge disks are connected to the MPDC, a different set of adapters is used when storage modules are connected to the MPDC. They cannot be intermixed. See Figure 2-26.

The MPDC subsystem interfaces with other components in the system via the Megabus. The MPDC controls information to the attached device adapter. Information to/from the controller is transferred to/from the adapters in byte form. The device adapter supplies information to and retrieves information from the devices in bit serial form. On retrieval of information from the devices the adapter assembles the information in byte form before transfer to the MPDC. For more information refer to the Type MSC9101/9102 Medium Performance Disk Controller Manual, Order Number FM54.

2.3.3.4 General Purpose Interface Controller Option

The General Purpose Interface Controller is for users who wish to interface special devices with the system through the Megabus. It provides a simple user interface and isolates the Megabus from the user designed logic. This controller connects to the Megabus and provides the user with the following interfaces:

- Character wide interface
- Asynchronous interface
- Direct Memory Access (DMA) mode
- Ability to interrupt the CPU
- Support of multiple devices
- Simple control line interface
- Spare board area for user logic.

Additional physical space remains on the controller board so that the user can insert his own electrical and interface logic in order to meet his specific needs. For more information refer to the General Purpose DMA Interface Manual, Order Number FL14.

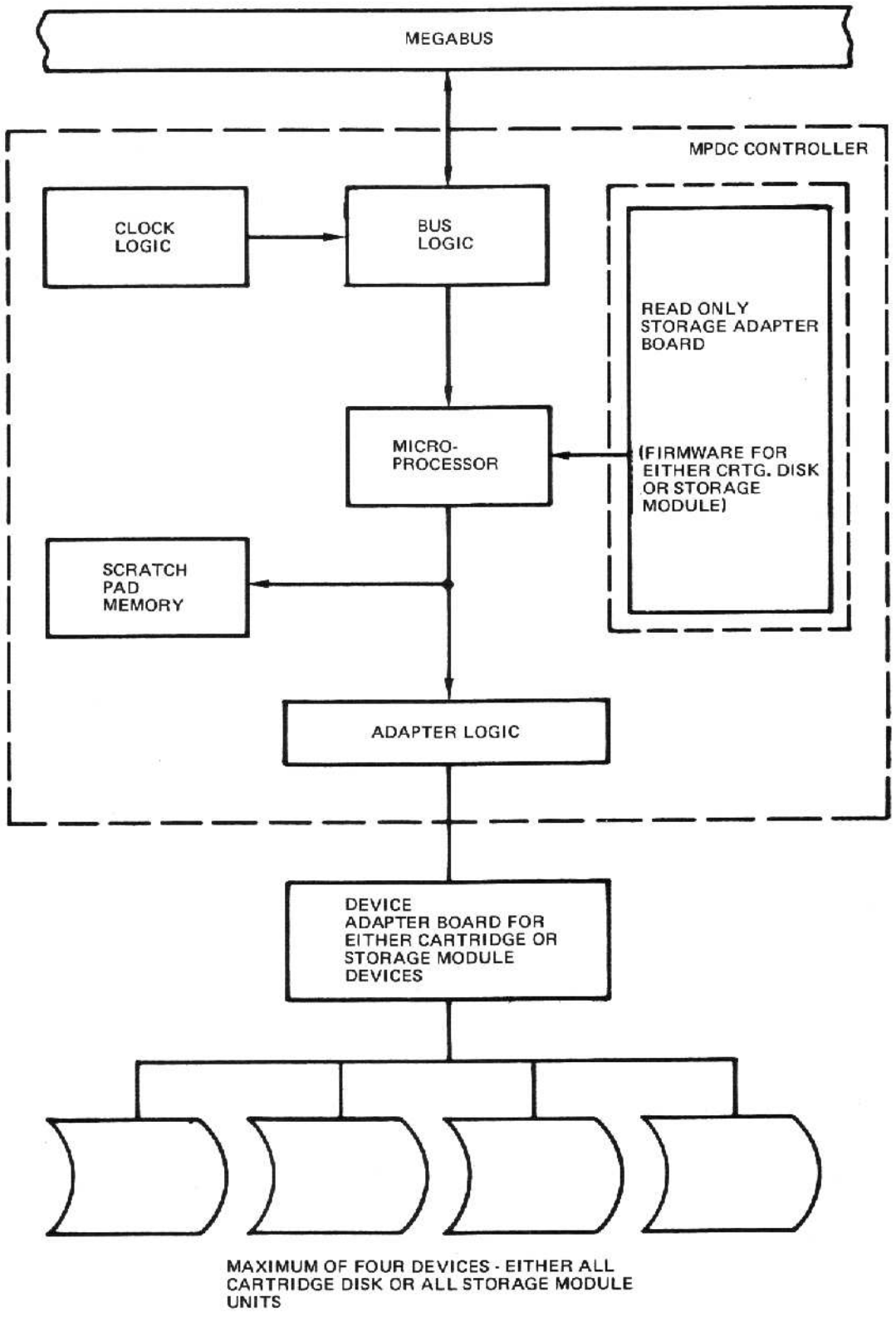


Figure 2-26 Medium Performance Disk Controller Major block Diagram

2.3.4 Special Options

2.3.4.1 Memory Save Power Supply

The memory save power supply provides emergency back-up power for the retention of data in MOS memory during power outages. During normal power-on operations the memory save power supply is energized by 120 Vac line voltage. The supply delivers +5Vdc and +12Vdc required for two MOS memory controllers and charges its maintenance free batteries. When primary power to the system is lost, the memory save batteries take over and supply the required memory voltages. When fully charged the batteries (three series-wired six-volt batteries) sustain the refresh voltage for approximately two hours. A LED on the front panel of the supply extinguishes if the memory refresh voltage has been interrupted or is not present.

The memory save power supply is a complete self contained unit approximately 17 inches in width and depth and 3.2 inches high (see Figure 1-9). The unit is normally installed just above the system chassis in a rack-mountable or office furniture package system. In tabletop systems, the tabletop system chassis sits on the top of the memory save power supply.

2.3.4.2 Level 6 Extender Board Option

The Level 6 extender board and extender board cable kit is an option for users who perform their own equipment maintenance and repair, and for system builders in the debugging of their general purpose interface boards.

The extender board option is intended for use with the five-card chassis, where in most cases its operation will be acceptable. However, it is not guaranteed for all Level 6 software because of the altered system timing and the possible generation of bus noise. The extender board may be used with larger systems (e.g., a 10-card chassis) for hardware debugging; however, full operation under Level 6 software may be seriously impaired.

2.3.4.3 Portable Control Panel Option

The portable (plug-in) control panel option is a self-contained version of the local full control panel, and is designed for exclusive use with the basic control panel (see Figure 2-8). The portable control panel is for users who perform their own equipment maintenance, repair, or debugging.

CAUTION

To avoid damaging the portable control panel, it should be removed from the basic control panel when not in use, especially when the basic control panel is swung open. The portable control panel is intended to be used only when the primary door is closed.