Appendix A
Instruction Timings

MODEL 23

Instruction timings for the Model 23 are listed in Tables A-1 through A-5.

NOTE: Processor timings can vary ± 20%.

TABLE A-1. MODEL 23 INSTRUCTION AND OPERAND FETCH TIMES

Addressing Forms	Op Codes/Fetch Times (μs)			
	Word Operand Instructions	Byte (LDH, LLH, CMH, ORH, XOH, ANH)	Byte (STH, CLH)	Bit (LB, LBF, LBC, LBS, LBT)
B, IMO, ↓B, B↑	3.5	4.5	3.0	4.0
B + X	4.0	6.0	4.5	7.5/8.0
IMA, P+D, B+D	4.5	5.5	4.0	5.0
IMA+X, B+↓X	4.5	6.5	5.0	8.0/8.5
B+X↑	5.0	6.5	5.0	8.0/8.5
R Register	3.0	4.0	2.5	8.0/8.5
B Register	3.0	–	–	–

NOTE: Add 1 μs if indirect addressing.

TABLE A-2. MODEL 23 EXECUTION TIMES

Op Codes	Address Syllable Times (μs)	
	R Register B Register	MAS
INC, DEC, NEG, CPL, CL STR, STB, STS, SWR	1	1.5
CLH, SWB	1	2
STM	2	2.5
CAD	1/1.5	1.5
LBS, LBT, LBF, LBC, STH	1.5	2
JMP, LNJ	–	1
LAB	–	0.5
CMB, LDB, CMN	0.5	1
ENT	–	2
ADD, SUB, LDR, LDH, OR XOR, AND, ORH, XOH, ANH CMH, CMR, CMZ, LB	0.5	
LLH	0.5/1	
MTM	4	
LEV, SAVE, RSTR, MUL DIV, LDI, SDI, IOH IO, IOLD	Not Available	

TABLE A-3. MODEL 23 R-BRANCH, I-BRANCH EXECUTION TIMES (INCLUDES FETCH)

Test Result	Instruction Times (μs)
Branch Unsuccessful	2.5
Branch Successful	3.5

TABLE A-4. MODEL 23 SHIFT INSTRUCTION TIMES (INCLUDES FETCH)

Op Codes	Instruction Times (μs)
SCL, SOR, SAR, SCR	2.5 + 0.5d
SOL	3.0 + 0.5d
SAL, DOR<16, DOL<16, DAR<16	3.5 + 0.5d
DCL, DAL 16, DCR	4.0 + 0.5d
DOR≥16	4.5 + 0.5d
DOL≥16, DAR≥16	5.0 + 0.5d
DAL≥16	5.5 + 0.5d

NOTE: d = shift distance; $1 \leq d \leq 15$

TABLE A-5. MODEL 23 SHORT VALUE IMMEDIATE INSTRUCTION TIMINGS (INCLUDES FETCH)

Op Codes	Instruction Times (μs)	
LDV, CMV, ADV	Positive operand	Negative operand
	2.5	3.0
MLV	Not available	

MODEL 33

Instruction timings for the Model 33 are listed in Tables A-6 through A-10.

NOTE: Processor timings can vary ±20%.

TABLE A-6. MODEL 33 INSTRUCTION AND OPERAND FETCH TIMES

Addressing Forms	Opcodes/Fetch Times (μs)						
	LDB, SWB, CMB, LDR, SWR, CMR, ADD, SUB, MUL, DIV, OR, XOR, AND, INC, DEC, CAD, CMZ, CPL, NEG, LEV, MTM	STB, STR, STM, CL, SAVE, JMP, RSTR, LNJ, ENT, LAB	LDH, LLH, CMH, ORH, XOH, ANH		STH, CLH	LB, LBF, LBC, LBS, LBT	LDV, CMV, ADV, MLV
			+ Operand	- Operand			
IMA, P + D, B + D[a]	3.72	2.77	4.01	3.72	2.77	3.72	Total Fetch and Execution times for immediate operands are shown in Table A-7.
IMA + X[a]	4.01	3.06	4.59	4.30	3.35	5.17	
B[a], IMO	2.77	1.82	3.06	2.77	1.82	2.77	
B + X[a]	3.06	2.11	3.64	3.35	2.40	4.22	
↓B, B↑	3.06	2.11	3.35	3.06	2.11	3.06	
B + ↓X, B + X↑	3.35	2.40	3.93	3.64	2.69	4.51	
R Register	1.53	1.53	2.49	2.21	1.53	1.53	
B Register	1.53	1.53	–	–	–	–	

[a]If indirect add 1.24 μs to time shown.

TABLE A-7. MODEL 33 EXECUTION TIMES

Op Codes	Address Syllable Times (μs)	
	R Register B Register	Any Other
INC, DEC, NEG, CPL, CL, STR, STB, STS	0.58	1.16
CLH, STH	1.16	1.16
STM	0.87	1.45
SWR, SWB	1.16	1.74
CAD	0.58/0.87	0.58/1.45
LBS (I[B] = 1), LBT	1.16	1.74/3.07
LBS (I[B] = 0), LBF, LBC	1.45	2.03/3.36
JMP, ENT	–	0.58
LNJ	–	0.29
LAB	–	0.0
ADD, SUB	0.38	
LDR, LBD, LDH, OR, XOR, AND, ORH, XOH, ANH	0.29	
CMR, CMB, CMH	0.38/0.67	
CMV[a]	1.91/2.20	
CMZ	0.67/0.96	
LEV	4.60/88.20	
SAVE	13.21/22.71	
RSTR	12.63/34.30	
MTM	1.74	
MUL (# ≠7)	11.20	
MUL (# =7)	10.73	
MLV[a] (# ≠7)	12.73	
MLV[a] (# =7)	12.26	
DIV (# ≠7)	13.22/14.56	
DIV (# =7)	13.22/14.27	
LLH	0.58	
LB	0.87	
ADV[a]	1.91	
LDV[a]	1.82	
CMN	Not Available	
LDI		
SDI		
SRM		
IOH		
LEV		

[a]Total Fetch & Execution Time

TABLE A-8. MODEL 33 SHIFT AND GENERIC INSTRUCTION TIMES (INCLUDES FETCH)

Shift Instruction Times (μs)		
SOL	1.53 + 0.29d	(See Notes 1 and 2)
SAL	1.82/2.11 + 0.29d	
SCL	1.53 + 0.29d	
DCL	1.82 + 0.29d	
DOL < 16	1.82 + 0.29d	
DOL ⩾ 16	2.11 + 0.29d	
DAL < 16	1.82/2.11 + 0.29d	
DAL ⩾ 16	2.11/2.69 + 0.29d	
SOR	1.53 + 0.29d	
SAR	1.53 + 0.29d	
SCR	1.53 + 0.29d	
DCR	1.82 + 0.29d	
DOR < 16	1.82 + 0.29d	
DOR ⩾ 16	2.11 + 0.29d	
DAR < 16	1.82 + 0.29d	
DAR ⩾ 16	2.11 + 0.29d	
Generic Instruction Times (μs)		
HLT	2.11	
MCL, BRK	16.75/17.07	
RTT	11.85	
RTCN, RTCF	2.11	
WDTN, WDTF	2.11	

NOTES: 1. d = shift distance. $1 \leqslant d \leqslant 15$

2. These are times for procedural shifts. For nonprocedural shifts (d = 0) add 0.96 μs to the above times.

TABLE A-9. MODEL 33 R-BRANCH, I-BRANCH EXECUTION TIMES (INCLUDES FETCH)

Test Success and Addressing Mode / Op Code	Unsuccessful (μs)	Successful (μs)		
		d ≠ 0, 1 (P + d)	d = 0 (IMA)	d = 1 (P + D)
BLZ, BGEZ, BEZ, BNEZ, BGZ, BLEZ, BEVN, BODD, BINC, BDEC	1.82	2.40/2.69 min/max	3.35	3.35
B, NOP, BAL, BAGE, BE, BNE, BAG, BALE, BOV, BNOV, BL, BGE, BG, BLE, BSU, BSE, BCT, BCF, BBT, BBF, BIOT, BIOF	1.53	2.11/2.40	3.06	3.06

TABLE A-10. MODEL 33 I/O INSTRUCTION TIMES

Address Syllable Form	I/O Instruction Times (μs)		
	IO		
	Input	Output	IOLD
IMA[a], P + D[a], B + D[a]	10.60	10.94	15.18
IMA + X[a]	11.18	11.52	16.34
B[a], IMO	8.70	9.04	12.33
B + X[a]	9.28	9.62	13.49
↓B, B↑	9.28	9.62	13.20
B + ↓X, B + X↑	9.86	10.20	14.36
IV + D	13.66	14.00	19.77
RA	6.22	5.93	8.32

[a]If indirect in any address syllable, add 1.24 μs for each indirection.

MODELS 43 AND 47

Instruction timings for the Models 43 and 47 are listed in Tables A-11 through A-14. The times given are for register addressing (SAF mode) utilizing a double-fetch EDAC memory. The minimum times are for the case where the instruction pre-fetch buffers are filled prior to attempting to execute the instruction. The maximum times involve empty pre-fetch buffers. The typical times are a statistical average – due to the nature of the 43/47, the instruction times may vary since the pre-fetch buffers may be full, empty, or half-full. The times do not take into account self-generated conflicts such as memory busy. Processor timing can vary ±20%.

TABLE A-11. MODELS 43 and 47 INSTRUCTION TIMINGS

Mnemonic	Instructions Description	Times (μs)			Notes
		Minimum	Maximum	Typical	
ACQ	Acquire Stack Space				N/A
ADD	Add to Reg	.79	1.47	1.01	
ADV	Add Value to R Reg	.79	1.47	1.01	
AID	Add Integer Double	1.16	1.84	1.38	
AND	And with R Reg	.66	1.34	.88	
ANH	And Half-word	.89	1.57	1.11	
ASD	Activate Segment Descriptor				N/A
B	(See separate listing for all Branch Instructions)				
CAD	Carry Add	.66	1.34	.88	
CL	Clear Memory	.89	1.57	1.11	
CLH	Clear Memory Half-word	1.42	2.10	1.64	
CMB	Compare B Reg	1.07	1.75	1.29	
CMH	Compare Half-word	1.32	2.00	1.54	
CMN	Compare with Null	.89	1.57	1.11	
CMR	Compare R Reg	1.05	1.73	1.27	
CMV	Compare with Value	1.05	1.73	1.27	
CMZ	Compare with Zero	1.30	1.98	1.52	
CPL	Complement	.89	1.57	1.11	

TABLE A-11 (CONT). MODELS 43 AND 47 INSTRUCTION TIMINGS

Mnemonic	Instructions Description	Time (μs) Minimum	Maximum	Typical	Notes
DAL	DBL Shift Left	.72+.16d	1.4+.16d	.94+.16d	1,2,3
DAR	DBL Shift Right	.72+.16d	1.4+.16d	.94+.16d	1,2,3
DCL	DBL Shift Closed Left	.68+.2d	1.36+.2d	.90+.2d	4
DCR	DBL Shift Closed Right	.68+.2d	13.6+.2d	.90+.2d	4
DEC	Decrement	.89	1.57	1.11	
DIV	Divide	11.81/11.96	12.49/12.64	12.03/12.16	7
DOL	DBL Shift Open Left	.18+.16d	.84+.16d	.4+.16d	5,6
DOR	DBL Shift Open Right	.18+.16d	.84+.16d	.4+.16d	5,6
DQA	Dequeue on Address				N/A
DQH	Dequeue on Head				N/A
ENT	Enter				N/A
HLT	Halt				N/A
INC	Increment	.89	1.57	1.11	
IO	Input/Output				N/A
IOH	Input/Output Half-word				N/A
IOLD	Input/Output Load				N/A
JMP	Jump	1.53	2.21	1.75	
LAB	Load EA into B Reg				N/A
LB	Load Bit	1.32	1.98	1.54	
LBC	Load Bit and Complement	1.83	2.49	2.05	
LBF	Load Bit and Set False	1.86	2.54	2.08	
LBS	Load Bit and Swap	1.73	2.41	1.95	
LBT	Load Bit and Set True	1.64	2.32	1.86	
LDB	Load B Reg	.66	1.34	.88	
LDH	Load Half-word	.89	1.57	1.11	
LDI	Load Double-word Integer	1.09	1.77	1.31	
LDR	Load R Reg	.66	1.34	.88	
LDT	Load Stack Register				N/A
LDV	Load Value	.66	1.34	.88	
LEV	Level Change				N/A
LLH	Load Logical Half-word	.89	1.57	1.11	
LNJ	Load and Jump	1.53	2.21	1.75	9
MCL	Monitor Call				N/A
MLV	Multiply By Value	7.85/7.96/7.28	8.53/8.64/7.96	8.07/8.18/7.50	8
MMM	Memory to Memory Move	4.28+.67n	4.76+.67n	4.5+6.7n	9
MTM	Modify M Reg				N/A
MUL	Multiply	7.86/7.29	8.54/7.97	8.08/7.51	7
NEG	Negate	.89	1.57	1.11	
NOP	No Operation	.45	1.13	.67	
OR	OR with R Reg	.66	1.34	.88	
ORH	OR Half-word	.92	1.60	1.14	
QOH	Queue on Head				N/A
QOT	Queue on Tail				N/A
RLQ	Relinquish Stack Space				N/A
RSTR	Restore Context	10.7+1.2d	11.75+1.2d	10.9+1.2d	
RTCF	Real-Time Clock Off				N/A
RTCN	Real-Time Clock On				N/A
RTT	Return From Trap				N/A

TABLE A-11 (CONT). MODELS 43 AND 47 INSTRUCTION TIMINGS

Instructions		Times (μs)			
Mnemonic	Description	Minimum	Maximum	Typical	Notes
SAL	SGL Shift Left	.72+.16d	1.4+.16d	.94+.16d	3,4
SAR	SGL Shift Right	.72+.16d	1.4+.16d	.94+.16d	3,4
SAVE	Save Context	10.4+.4n	11.08+.4n	10.6+.4n	
SCL	SGL Shift Closed Left	.5+.18d	1.18+.18d	.72+.18d	4
SCR	SGL Shift Closed Right	.5+.18d	1.18+.18d	.72+.18d	4
SDI	Store Double-word Integer	1.32	2.0	1.54	
SID	Subtract Integer Double	1.16	1.84	1.38	
SOL	SGL Shift Open Left	.5+.18d	1.18+.18d	.72+.18d	4
SOR	SGL Shift Open Right	.5+.18d	1.18+.18d	.72+.18d	4
SRM	Store Reg Masked	1.05	1.73	1.27	
STB	Store B Reg	.89	1.57	1.11	
STH	Store Half-word	1.42	2.10	1.64	
STM	Store M Reg	1.12	1.80	1.34	
STR	Store R Reg	.89	1.57	1.11	
STS	Store S Reg	.89	1.57	1.11	
STT	Store Stack Register				N/A
SUB	Subtract	.79	1.47	1.01	
SWB	Swap B Reg	1.12	1.80	1.34	
SWR	Swap R Reg	1.12	1.80	1.34	
VLD	Validate				N/A
WDTF	Watchdog Timer Off				N/A
WDTN	Watchdog Timer On				N/A
XOH	Exclusive OR Half-word	.89	1.57	1.11	
XOR	Exclusive OR	.66	1.34	.88	

NOTES:
1. Numbers given are for $1 \leq d \leq 15$. For $d > 15$ use 1.28+.16d.
2. For non-procedural shifts add .84 μs.
3. For overflow conditions add .3 μs.
4. For non-procedural shifts add .64 μs.
5. Numbers given are for $1 \leq d \leq 15$. For $d > 15$ use 1.0+.16 (d - 16).
6. For non-procedural shifts add .8 μs.
7. Numbers are given in the order of single precision/double precision.
8. Numbers are given in the order of single precision-no overflow/single precision-overflow/ double precision.
9. Another minimum address form for the instruction was used since register addressing is not applicable to the instruction.

N/A = Timings not available.

The times in Table A-11 are (where applicable) for data contained in registers; for the JMP and LNG instructions, they are for the simplest addressing modes. For other addressing modes including memory accessing where applicable, additional time is required. The times given below, in microseconds, should be added as necessary.

TABLE A-12. MODELS 43 AND 47 INSTRUCTION TIMINGS BY ADDRESS SYLLABLE FORM

Address Syllable Form[a]	Instruction Times (μs)								
	AID, SID, LDI	SDI	INC, DEC	CPL, NEG, SWB, SWR	LB	LBC, LBF, LBS, LBT	JMP, LNJ	All Stores[b]	All Others
IMA, B, IMO	2.46	0.74	1.19	1.17	0.68	1.19	0.00	0.19[c]	0.98
P+D, B+D, ↓B, B↑	2.64	0.92	1.37	1.35	0.86	1.37	0.18	0.37[c]	1.16
B+X, IMA+X	2.96	1.42	1.53	1.51	1.82	2.33	0.34	0.53	1.32[d]
B+↓X, B+X↑	3.16	1.62	1.73	1.71	2.02	2.53	0.54	0.73	1.52[d]

[a] Add 0.98 μs for indirect addressing.
[b] Except SDI; see SDI column.
[c] Subtract 0.16 μs for STH.
[d] Add 0.16 μs for all halfword instructions (ANH, CLH, etc.)

TABLE A-13. MODELS 43 AND 47 BRANCH TIMINGS

Op Code	Times (μs)					
	Unsuccessful			Successful		
	Minimum	Maximum	Typical	Minimum	Maximum	Typical
BDEC, BEVN, BEZ, BGEZ, BGZ, BINC, BLEZ, BLZ, BNEZ, BODD	.63	1.53	.76	.81	1.71	.97
B, BAG, BAGE, BAL, BALE, BBF, BBT, BCF, BCT, BE, BG, BGE, BIOF, BIOT, BL, BLE, BNE, BNOV, BOV, BSE, BSU	.49	1.37	.62	.67	1.55	.80

TABLE A-14. MODELS 43 AND 47 SCIENTIFIC INSTRUCTION TIMINGS

Instruction Mnemonic	Instruction Address Format	Overall Instr. Time (μs)	Models 43 and 47 Time (μs)	SIP Time (μs)	Available SIP/CP (for overlap)
SML	SA_D op SA_D	8.15	2.03	6.52	1.63/6.12
	SA_Q op SA_Q	11.45	2.03	9.82	1.63/9.42
	R op SA	8.60	2.59	6.97	1.63/6.01
	RR op SA	12.40	2.95	10.77	1.63/9.45
	M_D op SA_D	10.04	3.66	8.21	1.83/6.38
	M_Q op SA_Q	14.57	3.66	12.74	1.83/10.91
SDV	SA_D op SA_D	7.17	2.03	5.54	1.63/5.14
	SA_Q op SA_Q	14.52	2.03	12.89	1.63/12.49
	R op SA	7.62	2.59	5.99	1.63/5.03
	RR op SA	15.47	2.95	13.84	1.63/12.52
	M_D op SA_D	9.06	3.66	7.23	1.83/5.40
	M_Q op SA_Q	17.64	3.66	15.81	1.83/13.98
SCM	SA_D op SA_D	3.27	2.03	1.64	1.63/1.24
	SA_Q op SA_Q	3.27	2.03	1.64	1.63/1.24
	R op SA	3.72	2.59	2.09	1.63/1.13
	RR op SA	4.22	2.95	2.59	1.63/1.27
	M_D op SA_D	5.16	3.66	3.33	1.83/1.50
	M_Q op SA_Q	6.39	3.66	4.56	1.83/2.73
SCZD					
SCZQ					
SNGD					
SNQD					
SB	Branch on Indicator	3.23	3.23	0.95	1.63/0.0
SB–	Branch on Accumulator	3.23	3.23	0.95	1.63/0.0
SLD	SA_D op SA_D	2.28	2.03	0.65	1.63/0.25
	SA_Q op SA_Q	2.28	2.03	0.65	1.63/0.25
	R op SA	2.73	2.59	1.10	1.63/0.14
	RR op SA	3.23	2.95	1.60	1.63/0.28
	M_D op SA_D	4.17	3.66	2.34	1.83/0.51
	M_Q op SA_Q	6.00	3.66	4.17	1.83/2.34
SST	SA_D op SA_D	2.28	2.03	0.65	1.63/0.40
	SA_Q op SA_Q	2.28	2.03	0.65	1.63/0.04
	SA op R	2.79	2.79	1.10	1.63/0.0
	SA op RR	3.55	3.55	1.60	1.63/0.0
	SA_D op M_D	4.43	3.66	2.60	1.83/0.77
	SA_Q op M_Q	5.73	3.66	3.90	1.83/2.07

TABLE A-14 (CONT). MODELS 43 AND 47 SCIENTIFIC INSTRUCTION TIMINGS

Instruction Mnemonic	Instruction Address Format	Overall Instr. Time (μs)	Models 43 and 47 Time (μs)	SIP Time (μs)	Available SIP/CP (for overlap)
SSW	SA_D op SA_D	2.78	2.03	1.15	1.63/0.75
	SA_Q op SA_Q	2.78	2.03	1.15	1.63/0.75
	R op SA	3.79	3.79	1.60	1.63/0.0
	RR op SA	4.55	4.55	2.10	1.63/0.0
	M_D op SA_D	6.67	3.66	4.84	1.83/3.01
	M_Q op SA_Q	9.20	3.66	7.37	1.83/5.54
SAD	SA_D op SA_D	3.75	2.03	2.12	1.63/1.72
SSB	SA_Q op SA_Q	3.57	2.03	1.94	1.63/1.54
	R op SA	4.20	2.59	2.57	1.63/1.61
	RR op SA	4.52	2.95	2.89	1.63/1.57
	M_D op SA_D	5.64	3.66	3.81	1.83/1.98
	M_Q op SA_Q	6.69	3.66	4.86	1.83/3.03

op – Operation; e.g., SLD (Scientific Load)
SA_D – Scientific Accumulator (Double-word length)
SA_Q – Scientific Accumulator (Quadruple-word length)
SA – Scientific Accumulator (Double- or quadruple-word length)
M – Main Memory Location (Double-word length)
M_Q – Main Memory Location (Quadruple-word length)
R – Central Processor Register (Single integer length)
RR – Central Processor Registers (Double integer length)

MODELS 53 and 57

Approximate instruction timings for the Models 53 and 57 can be derived from the tables for the Model 43 and 47 (i.e., Tables A-11 and A-12) by calculating a 30% reduction. Table A-15 lists the timings for the Model 57 CIP, which may be used as a guideline for calculating the timing of Model 57 programs using the CIP. The times given in Table A-15 are for P+D addressing (SAF mode) utilizing a double-fetch EDAC memory. The times listed are typical; due to the nature of the Model 57 the instruction times may vary since the prefetch buffers may be full, empty, or half full. The times do not consider self-generated conflicts such as memory busy.

NOTE: Processor timing can vary ±20%.

TABLE A-15. MODEL 57 CIP INSTRUCTION TIMINGS

Instruction		Overall Instruction	
Mnemonic	Description	Time (μs) (Notes 1 and 2)	Comments
ACM	Alphanumeric Compare	11 + W1 + W2	
ALR	Alphanumeric Move	11 + n	Note 4
AME	Alphanumeric Move and Edit	20 + MOP times	
	All Branch Instructions	1.5 – No Branch 2.0 – Branch	
CBD	Convert Binary to Decimal	27 + W1 + W2	
CDB	Convert Decimal to Binary	19 + 2W1 + W2	
DAD	Decimal Add	14 + W1 + 2W2	Note 3
DCM	Decimal Compare	15 + W1 + W2	Note 3
DDV	Decimal Divide		Notes 3 and 7
DMC	Decimal Move and Convert	$16 + W1 + W2 + \frac{n}{4}$	
DME	Decimal Move and Edit	22 + T + MOP times	
DML	Decimal Multiply		Note 6
DSB	Decimal Subtract	14 + W1 + 2W2	
DSH	Decimal Shift	21 + 2W1 + (.2 X No. of Shifts)	
MAT	Alphanumeric Move & Translate	17 + 3n	Note 4
SRH	Alphanumeric Search	20 + W1 + (4 X No. of Compares)	
VRF	Alphanumeric Verify	20 + (3.6 X No. of Compares)	

TABLE A-16. MODEL 57 CIP MICRO OPERATION TIMINGS

Micro Operation (MOP)			
Mnemonic	Description	Time (μs) (Note 5)	Comments
CHT	Change Table	1	
ENF	End Floating Suppression	2	
IGN	Ignore Source Character	5	
INSA	Insert Asterisk on Suppress	5	
INSB	Insert Blank on Suppress	5	
INSM	Insert Table Entry 1 Multiple	7 + .4n	
INSN	Insert on Negative	5	
INSP	Insert on Positive	5	
MFLC	Move with Float Currency Insertion	13 + 1.1n	
MFLS	Move with Float Sign Insertion	13 + 1.1n	
MVC	Move Source Character	8 + 1.5n	
MVZA	Move with Zero Suppression	13 + 1.1n	
MVZB	Move with Zero Suppression	13 + 1.1n	
SEF	Set Edit Flags	2.5	

NOTES:

1. W1 = the number of words in field described by Data Description 1 (DD1).

   W2 = the number of words in field described by DD2.

   For string decimal, alphanumeric and binary data, the number of digits divided by two equals the number of words. For packed decimal data, divide by four.

   n = the number of characters (digits) actually moved.

   T = the number of words in DD1 field but not moved by any MOPs in a DME or AME instruction.

2. Values shown are for P&D addressing mode and in-line description. For other modes, add the following values:

   B+D – 0 μs
   B+D+R – 1.9 μs
   P+D+R – 2.0 μs
   IMO – 0 μs except if DD2 is IMO, then add 1 μs
   Indirect addressing – 2.0 μs
   Remote descriptions – 1.6 μs
   Register (L=0) – 0.5 μs

3. Values shown for decimal instructions are for unsigned data. For signed data add:

   Trailing overpunch – 1.0 μs
   Leading separate signs – 1.0 μs
   Trailing separate signs – 1.0 μs

4. Values shown are for no-fill case. For fill case add an additional 3 + 0.3n μs where n = # of ATOMS filled.

5. If MOP sets flags which cause post-edit/editing then add additionally:

   0.7 x fw for force-fill with zero
   2.2 x fw for force-fill with asterisk

   where fw = number of words in field.

6. Instruction is data-sensitive. To compute times, use the following formula:

$$t = 26 + W1 + 2W2 + \frac{(\Sigma MIER)(MAND) + (MAND)(MIER)}{2}$$

   W1 = Number of words in DD1
   W2 = Number of words in DD2
   ΣMIER = Summation of digits in multiplier
   MAND = Number of significant digits in multiplicand
   MIER = Number of digits in multiplier

   Example:

   10 digits (0000000001) x 10 digits (all 9s)

   W1 = 5
   W2 = 5
   ΣMIER = 90
   MAND = 1
   MIER = 10

   Using formula:

$$t = 26 + 5 + 2(5) + \frac{(90)(1) + (1)(10)}{2}$$

$$t = 91\ \mu s$$

NOTES (Cont.)

7. Instruction is data-sensitive. To compute time use the following statements:

$$t = 31 + W1 + 2W2 + \frac{LZ1}{2} + \frac{LZ2}{2} + \Sigma q\,(2 + \frac{LDV}{4}) + 2\,(Nq - 1) + \frac{D3}{4} + W3$$

W1 = Number of words in field described by DD1
W2 = Number of words in field described by DD2
W3 = Number of words in field described by DD3
LZ1 = Number of leading zeros in dividend
LZ2 = Number of leading zeros in divisor
Σq = Summation of digits in quotient
LDV = Number of significant digits in divisor
N_q = Number of quotient digits
D3 = Number of digits in DD3

Example:

10 digits (all 9s) divided by 10 digits (all 2s), quotient is 31 digits

W1 = 5
W2 = 5
LZ1 = 0
LZ2 = 0
Σq = 4
LDV = 10
N_q = 10
D3 = 31

Putting values in formula:

$$t = 31 + 5 + 2(5) + \frac{0}{2} + \frac{0}{2} + 4\,(2 + \frac{10}{4}) + 2\,(1 - 1) + \frac{10}{4} + 16$$

$t = 83\ \mu s$

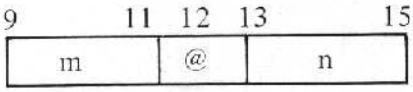
TABLE A-17. EXAMPLES OF MODEL 57 CIP INSTRUCTION TIMINGS

Mnemonic	DD1	DD2	DD3	Instruction Time (μs)
ACM	31 Characters	31 Characters		43
ALR	20 Characters	31 Characters		37 (Fill)
AME	31 Digits	31 Digits	INSM – 16 Chars. MVC – 15 Chars.	63
CBD	2 Binary Nos.	10 Digits		33
CDB	10 Digits	2 Binary Nos.		30
DAD	31 Digits	31 Digits		62
DCM	31 Digits	31 Digits		47
DDV	10 Digits	10 Digits	31 Digits	81 (See DDV example)
DMC	31 Digits	31 Digits		56
DME	31 Digits	31 Digits	INSM – 16 Digits MVC – 15 Digits	74
DML	10 Digits	10 Digits		89 (See DML example)
DSB	31 Digits	31 Digits		62
DSH	31 Digits	Shift 10 Digits		55
MAT	31 Characters	31 Characters		110 (No Fill)
SRH	1 Character		31 Characters	145 (Not Equal)
VRF	1 Character		31 Characters	132 (All Equal)

Appendix B

Address Syllable Reference Table

The single and double operand instructions generate address references through a field called the Address Syllable (AS). The format of the address syllable is as follows:



where:

m = address modifier
@ = indirect addressing bit
n = register number (value between 0 and 7, inclusive)

Table B-1 is a representation of the complete address syllable. An explanation of the mnemonics for the various address forms available appears at the bottom.

TABLE B-1. ADDRESS SYLLABLE REFERENCE TABLE

n = 0			n > 0			
m	@ = 0	@ = 1	@ = 0	@ = 1		
0	IMA	*IMA	Bn	*Bn		
1	IMA+D1	*IMA+D1	Bn+D1	*Bn+D1		
2	IMA+D2	*IMA+D2	Bn+D2	*Bn+D2		
3	IMA+D3	*IMA+D3	Bn+D3	*Bn+D3		
4	P+DSP	*(P+DSP)	Bn+DSP	*(Bn+DSP)		
5	RFU	RFU	Bn register or Dn register	n=1, 2, or 3 Bn +↓D1	RFU n=4	n=5, 6, or 7 B(n-4) +D1↑
6	RFU	RFU	↓Bn	n=1, 2, or 3 Bn +↓D2		n=5, 6, or 7 B(n-4) +D2↑
7	IMO	IV+DSP	Bn↑	n=1, 2, or 3 Bn +↓D3		n=5, 6, or 7 B(n-4) +D3↑

Notation Description

DSP	16-bit signed displacement that follows the instruction
*	Indirect operator (≠@)
+D	Specifies indexing
↑	Auto-increment (B↑ or D↑ indicates post-incrementation)
↓	Auto-decrement (↓B or ↓D indicates pre-decrementation)
IMA	Immediate Address
IMO	Immediate Operand
IV	Interrupt Vector
B	Base register
D	Operand register
P	Program counter; for the purpose of P relative addressing, P points to the word containing the displacement
( )	Logical binding
+	Addition operator

Appendix C

Hardware Dedicated Memory Locations

SAF Memory Location	Hardware Nomenclature	LAF Memory Location**	Contents
0000	RHU/RSU	0000	– Entry to Power Failure Restart Routine
0009	NATSAP 7	0002	– Pointing to Next Available TSAs
0010	NATSAP0	0010	
	RHU		
0014	RTCI	0014	– RTC Initial Value
0015	RTCC	0015	– RTC Current Value
0016	RTCL	0016	– RTC Level
0017	WDTC	0017	– WDT Current Value
	RHU		
001F	MERC	001F	– Memory Error Count
0020	0 → 15	0020	– Interrupt Level Activity Flags
0021	16 → 31 (IAF)	0021	
0022	32 → 47	0022	
0023	48 → 63	0023	
	RHU		Associated Event
0052	TV#46	0024	– Reserved for future use (RFU)
0061	TV#31	0042	– SIP Mini QLT Fault
0062	TV#30	0044	– Inoperative CIP
0063	TV#29	0046	– Commercial Overflow*
0064	TV#28	0048	– Commercial Truncation*
0065	TV#27	004A	– Commercial Illegal Character
0066	TV#26	004C	– Commercial Illegal Specification
0067	TV#25	004E	– Commercial Divide by Zero
0068	TV#24	0050	– Memory or Megabus Error seen by SIP or CIP
0069	TV#23	0052	– Unavailable Reference referenced by SIP or CIP
006A	TV#22	0054	– Scientific Precision Error*
006B	TV#21	0056	– Scientific Significance Error*
006C	TV#20	0058	– Scientific Program Error
006D	TV#19	005A	– Scientific Exponent Underflow*
006E	TV#18	005C	– RFU
006F	TV#17	005E	– Uncorrectible Memory or Megabus Error
0070	TV#16	0060	– Program Error
0071	TV#15	0062	– Unavailable Resource
0072	TV#14	0064	– Unauthorized Reference to Protected Memory (with optional protection)
0073	TV#13	0066	– Privilege Violation
0074	TV#12	0068	– RFU
0075	TV#11	006A	– RFU
0076	TV#10	006C	– Stack Overflow
0077	TV#9	006E	– Stack Underflow
0078	TV#8	0070	– Scientific Exponent Overflow
0079	TV#7	0072	– Scientific Divide by Zero
007A	TV#6	0074	– Integer Register Overflow
0078	TV#5	0076	– Uninstalled Option
007C	TV#4	0078	– Reserved for software use (RSU)
007D	TV#3	007A	– Uninstalled Scientific Option
007E	TV#2	007C	– Trace*/Breakpoint Trap
007F	TV#1	007F	– Monitor Call Trap
0080	IV#0	0080	
0081	IV#1	0082	
00BE	IV#62	00FC	
00BF	IV#63	00FE	
00FF	RHU	00FF	– Reserved for hardware use (RHU)

*Maskable Trap Conditions

**All LAF addresses and vectors are contained in two memory words.

NOTE: The Models 23 and 33 do not use TV#18–TV#46.

Figure C-1. Hardware Dedicated Memory Locations