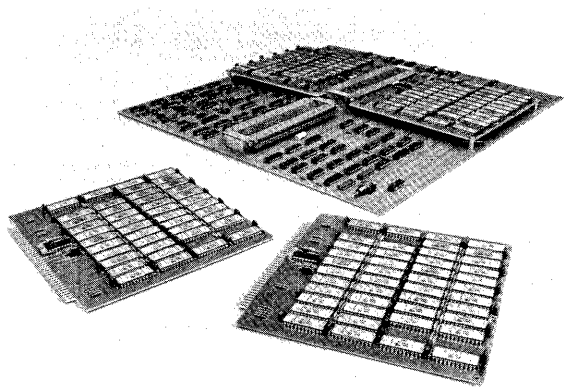
Honeywell

MOS Memory

SERIES 60 (LEVEL 6)

Level 6 memory uses state-of-the-art semiconductor technology, N-channel and 4096-bit dynamic RAMs as the storage media. The design emphasizes high reliability, low cost, modularity and simplified field maintenance.

Like other elements of Level 6, the memory is a Megabus-compatible subsystem that communicates directly with any other element on the bus and in the same fashion. TTL MSI circuitry minimizes power and space requirements for the extensive functionality provided. Self-contained on each memory module is Megabus support, refresh and initialization logic.



FEATURES

- Directly addressable memory
- 32KW (64KB) per Memory Controller board
- Compact 15 x 16-inch Memory Controller boards accommodate up to four plug-in 8KW Memory-Pacs
- Economical byte-parity memory or highly-reliable EDAC memory
- 650 nanosecond word write memory cycle time; 1420 nanosecond byte write memory cycle time
- Two-hour Memory Save with Autorestart option for up to 64KW
- Low power – 28/35 watts active for parity/EDAC version; 23/29 watts standby for parity/EDAC version for fully-loaded 32KW

TWO KINDS OF MEMORY

Level 6 offers two kinds of memory:

- *Byte-Parity Memory* – offered on all Level 6 models; includes logic for storing/retrieving two parity bits per word on each 8192-word Memory-Pac. Thus the actual word size in memory is 18 bits. The parity bits are returned to anyone reading the memory.
- *EDAC (Error Detection and Correction) Memory* – offered on the Models 6/36 and 6/06; includes logic for six parity bits per word on each 8192-word Memory-Pac. The supplied 2-bit parity is used together with the data to develop and store a 6-bit EDAC code. When read, memory attempts to correct any internally caused data error, reporting the results over two dedicated leads on the Megabus. Each lead sets a specific status bit depending on whether the error can be corrected or not. EDAC is particularly desirable for large systems, where extended reliability is required.

With either kind of memory, address parity accompanies the most significant eight bits on the address bus. When memory detects an error on these bits, it does not respond; the result is a bus timeout. Note also that each device/communication controller on the Megabus checks parity as it passes through and indicates an error by setting a parity error status bit.

An optional Memory Save and Autorestart capability is offered on the 6/30 Models (standard on Model 6/06) that provides data retention for 65,536 words of memory for a two-hour period. Support circuit power runs are separated to minimize standby power drain. Electronics within the optional unit maintain battery charge, regulate outputs, and indicate holdup failures.

A Level 6 memory configurator is shown in Figure 1.

SEMICONDUCTOR STORAGE

Commercially available 4K, N-channel MOS devices are used as the storage elements. Each device is exposed to vigorous functional testing on computerized test equipment. The result is a cost-effective quality product comparing favorably with core

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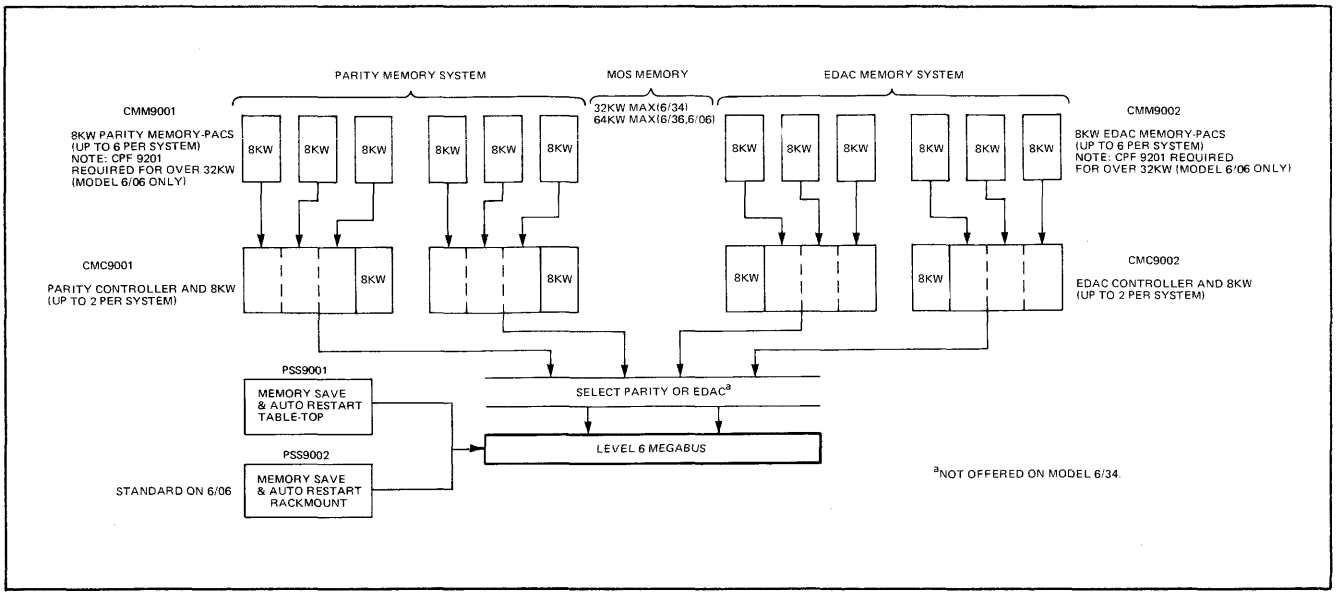

Figure 1. Memory Configurator

technology in all respects. TTL compatibility offered by N-channel MOS eliminates the need for extensive discrete and linear integrated circuitry required to interface with core memories as well as the liability. Packing density is superior and power requirements are dramatically reduced. Both characteristics again enhance the Level 6 size, weight, and MTBF advantages over core. Furthermore, integrated circuitry simplifies failure diagnosis and repair procedures. One other significant advantage over core is the increase in memory utilization made possible with the inherently shorter cycle times associated with semiconductor devices.

PACKAGING

Level 6 board technology advantages are significant. Field expansion in small capacity increments is now possible without the cost of repeating overhead circuitry. Sparing costs are minimized through the use of the 8192-word modules as Optimum Replacement Units (ORUs).

FUNCTIONALITY

Level 6 memory functions with minimum Megabus utilization. The interface is totally asynchronous; after a memory read request is acknowledged, the bus is released to other users. Meanwhile, the memory completes its internal cycle while retaining the identification of the requestor. As the internal cycle nears completion, the memory requests a Megabus cycle and upon acknowledgement of bus availability sends data to the requestor. A Megabus cycle is less than half the memory cycle time and so allows simultaneous utilization of two modules at their maximum cycle rates.

Level 6 addressability extends to 16 million bytes; hence future expansion of the maximum memory now available on Level 6 is foreseeable. Configuration switches mounted on the memory are set with the module identification address to establish each module's logical position with the address spectrum. (The module's logical position i.e., address, has no relationship to its physical chassis position.) Write operations require only one Megabus cycle. Both word and byte write modes are available. In EDAC parity checking, "Red" and "Yellow" bus signals are activated for noncorrectable and correctable errors, respectively. Parity on data is treated as a pseudo data bit by the check bit encoders. If bad parity is received, the "Red" line is activated during the subsequent readout.

A momentary contact switch is placed on the EDAC memory board within easy access behind the swing-out control panel. When the switch is depressed during the specified portion of the diagnostic routine, check bits are forced to all zeros for all new data. With careful selection of data patterns, all elements of the decoding, detecting, and correcting logic can be exercised and must be operating properly for the scrambled readout data to match that of a functioning system. Other

portions of the EDAC circuitry, including check bit chips, can be checked with special patterns in normal mode.

The sharing of the I/O bus with memory in Level 6 is a departure from much standard minicomputer practice; usually a second bus is dedicated to memory. Advantages of the Level 6 approach are as follows:

- A fully asynchronous memory interface that is fully-compatible with all other elements of Level 6 is achieved. Thus direct memory access is a fundamental ingredient of the architecture. Furthermore, the standard asynchronous interface expands configuration dimensionality by allowing simultaneous use of memory types with varying performance and cost.
- Bus hardware is minimized, with less than 100 signals paths required for the total function. This feature helps make possible the unique physical configuration of Level 6, providing front access board removal in conjunction with the simplicity of front-to-rear cooling airflow.

MEMORY OPTIONS

The following memory options are available for all Level 6 models unless otherwise noted. Maximum memory for the Model 6/34 is 32KW, and for the Models 6/36 and 6/06, 64KW. EDAC memory is offered on Models 6/36 and 6/06 only.

Option No.	Description
CMC9001	Memory Controller with parity, including 8KW Memory-Pac (CMM9001); Can add up to three more 8KW Memory-Pacs per Memory Controller
CMM9001	8KW Memory-Pac with parity
CMC9002	Memory Controller with EDAC, including 8KW Memory-Pac (CMM9002); can add up to three more 8KW Memory-Pacs per Memory Controller
CMM9002	8KW Memory-Pac with EDAC
CPF9201	Extended memory and memory lockout option (offered on 6/06 only and required with more than 32KW of memory.)
PSS9001	Memory Save and Autorestart for up to 64KW, table-top model
PSS9002	Memory Save and Autorestart for up to 64KW, rack mountable model (Standard on 6/06.)

Specifications may change as design improvements are introduced.

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