Honeywell

FOR INTERNAL USE ONLY

LEVEL 68 & 68/DPS CONFIGURATION GUIDE

SERIES 60 (LEVEL 68 & 68/DPS)

CONFIGURATION GUIDE

FOR INTERNAL USE ONLY

SUBJECT

Information for Configuring the Level 68 Processor, IOM, and System Control Unit

ORDER NUMBER

DJ05, Rev. 0

January 1979

Honeywell

Preface

This Guide provides nearly complete freestanding information for configuring the Level 68 Processor, IOM, and System Control Unit. Configuration rules for the peripheral subsystems are covered in the Level 66 Configuration Guide.

All Level 68 systems are freestanding; the ICU is not available. When configuring the peripheral subsystem for Model 68/60 and 68/80, use the rules for the Model 66/60 and Model 66/80 respectively. (See unsupported peripherals in the footnotes to Section 1,B.) for the Level 68/DPS follow the rules for Level 66/DPS. (See unsupported peripherals in the footnotes to Section 1,B.)

All configuring rules are given on the basis of use of 4K bit MOS memory chips with 16 pins. Shipment of this memory began in the third quarter, 1977. Prior 4K bit MOS chips had 22 pins. The 16-pin chip increases the quantity of memory which can be included in cabinets which contain memory.

This Guide is constructed to be as self-explanatory as possible, and it provides for configuring both initial system orders and subsequent add-ons. Material in this Guide dealing with Level 68 mainframes consists primarily of a set of charts and brief summaries. The charts provide a foundation based on definitions and fundamental rules. By following the appropriate flowcharts, step charts, and tables, you will be able to quickly and easily configure any initial system order or add-on order accurately.

This Guide is divided into gross functional sections. Before using the configuration material, it is advisable to become familiar with the contents of this document.

Section I summarizes key general rules and policies which govern configuration of Level 68 systems. Included also are key definitions, some of which are standard or official and others which are unofficial and used only in this material. Before doing any configuring you should always review Section I.

Section II provides a master flowchart which identifies the sequence and components to be considered in configuring mainframes. Pull out this flowchart and keep it in view to access other portions of this material in order to configure easily, completely, accurately. The flowchart has page number references for component configuration at each level of the flowchart.

Section III explains the initial order of a complete mainframe, where there are no optional replications (for example, modules) in the mainframe. It guides you to various pages and tables which define the CPS (Central Processing System) or base type numbers for each possible Level 68 model and mainframe packaging.

Section IV covers the configuration of the components needed within each IOM. These components relate to physical IOM channels for peripheral subsystems, the assignment of logical channels (data paths) for each physical channel, and the assignment of the scratchpad feature called DRE (data rate expansion).

File No.: 3LW2 DJ05

Section V provides for configuring optional mainframe functional components – processors, IOMs, SCUs. Use this section for both the initial order and for additional orders which involve these components.

Section VI deals with expanding the size of memory on an installed system.

Section VII gives examples of various mainframe configurations.

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Section I
General Policies and Definitions

A. Model Restrictions for the Level 68 Multidimensional Family

These restrictions are indicated for those models where special restrictions apply. All systems are governed by the peripheral subsystem maximums and minimums (below).

B. Minimum and Maximum Peripheral Subsystems per Level 68 System

1. Lower speed peripheral subsystems[1]

	Min.	Max.
a. System console (CSU6004)	1	(See footnote 2)
b. Card reader	0	As needed
c. Card punch	0	As needed
d. Printer	1	As needed[3]
e. FNP	0	4[4]

2. Higher speed peripherals[1]

	Min.	Max.
a. Magnetic tapes	1-3[5]	As needed
b. Disk storage	About 40-50 million bytes (See footnote 6)	As needed (See footnote 7)

---

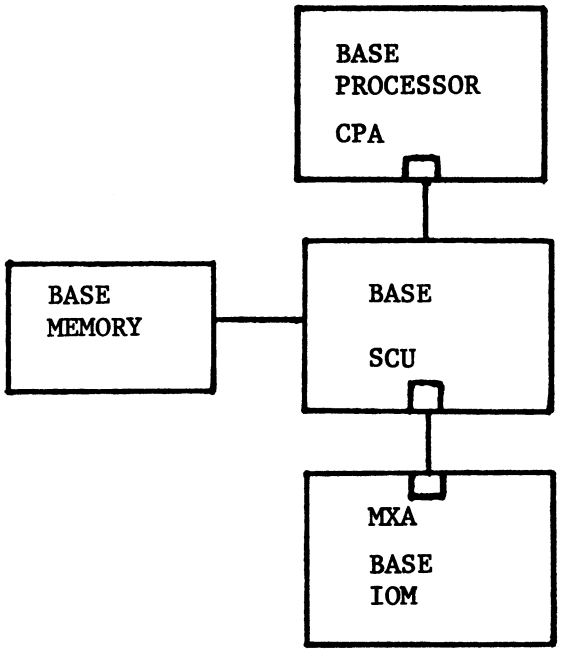
1. The following peripheral subsystems are not supported by Multics:
   - o System Control Center (CSU6005)
   - o Card Reader/Punch (CCU0401)
   - o Card Punch (PCU0300)
   - o Magnetic Tape Drive (MTU0410/0411/0412)
   - o Printer (PRU1100)
   - o Document Handler (DHP0700/0701)
2. Every system must contain at least one console subsystem. Multics supports a maximum of 4 consoles (4 console CRT screens). See console discussion in Peripherals outline of Level 66 Configuration Guide.
3. PRU1100 is not supported.
4. Also, it should be noted that MCS (Multics Communication System) is the FNP software and does not support the mass storage link (delta configuration).
5. Check with Multics technical support. Tape units may be needed for the Multics system journal file (used by V File for file recovery, etc.). At software release installation time the availability of a minimum of one tape unit complicates the system edit process. Two or three (better three) tape units make the system edit process easier and simpler. If three tape units are not available for system edit process, an appreciable quantity of disk scratch space must be available.
6. Check with Multics technical support. This figure does not provide for any user data files or user temporary files. It represents the recommended minimum of Multics residence, Multics scratch files, SYSOUT file space, and the minimum for other Phoenix-supported software.
7. A system should have a minimum of 4 disk drives with no less than 500 M3 of storage.

C. Key Mainframe Definitions

1. FOR NON-DPS SYSTEMS

a. Base CPS Systems (See Figure 1-1.)

This configuration is the heart of each mainframe. It is obtained by use of the CPS number shown on the pertinent Base Mainframe Configurator Chart (in Section III) for the model you want to order. The base CPS system type number is the first type number you write on your initial order. All additions at the time of the initial order or after the system has been installed are made to the base CPS system. The base CPS system is also known as base system, basic system, or base mainframe.



Each CPS number gives you a complete mainframe as shown:

One processor; *one* SCU with a base quantity of memory; *one* IOM, plus *one* central processor addressing feature or port (CPA) in base processor; and *one* IOM addressing feature or port (MXA) in base IOM. Components in base CPS system do not have individual type numbers.

Figure 1-1. Components of Each Base CPS System

b. Net Base System[1] (See Figure 1-2)

This is the base CPS system plus the second SCU which is required but not included for each 512K words module of memory. With each additional SCU, there must also be one CPA6002 (central processor addressing feature or port) and one MXA6001 (IOM addressing feature or port). The CPA and MXA are necessary to connect the base processor and base IOM to each extra SCU.

When you use the appropriate Base Mainframe Configurator Chart for the desired model and memory size, the net base system requirements are included in the type number shown.

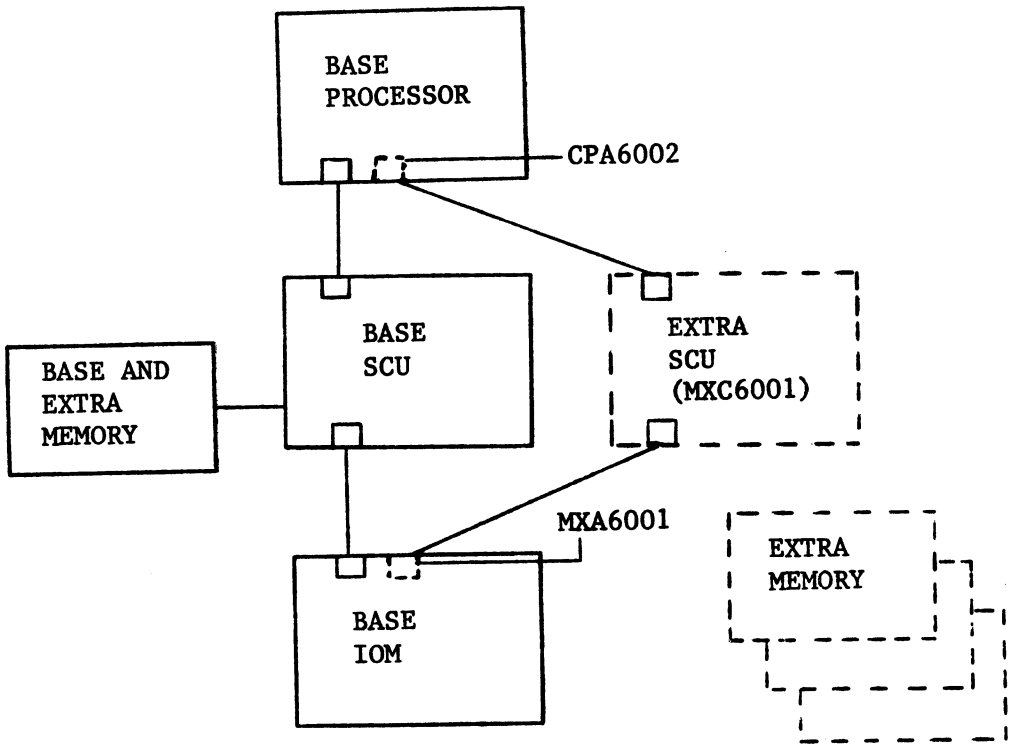


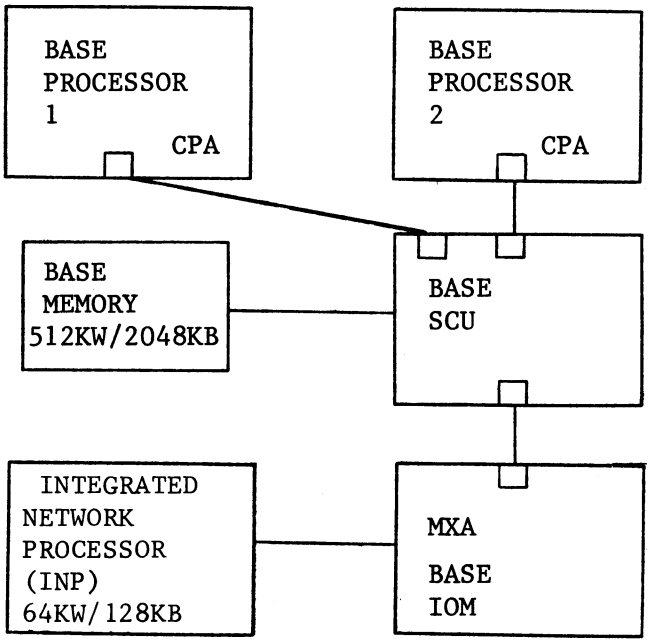
Figure 1-2. Net Base System – Non DPS

[1] The term "net base system" is not an official term and is used here only for purpose of clarifying configuring rules.

2. FOR DPS SYSTEMS

a. Base CPS System

This configuration is the heart of each basic mainframe. It is obtained by use of the CPS8802 number shown in Section III, paragraph A, 2. The base CPS system type number is the first type number you write on your initial order. All additions at the time of the initial order or after the system has been installed are made to the base CPS system. The base CPS system is also known as base system, basic system, or base mainframe.



The 68/DPS CPS number gives you a complete mainframe as shown:

Two processors; *one* SCU with a base quantity of memory; *one* IOM, plus *two* central processor addressing features or ports (CPA) in base processor; and *one* IOM addressing feature or port (MXA) in base IOM. Components in the base CPS system do not have individual type numbers.

Figure 1-3. Components of Each CPS8802 System for Any DPS Model

b. Net Base System (See Figure 1-4.)

This is the base CPS system plus the second SCU which is required but not included when the system has more than 1024K words/4096K bytes of memory.

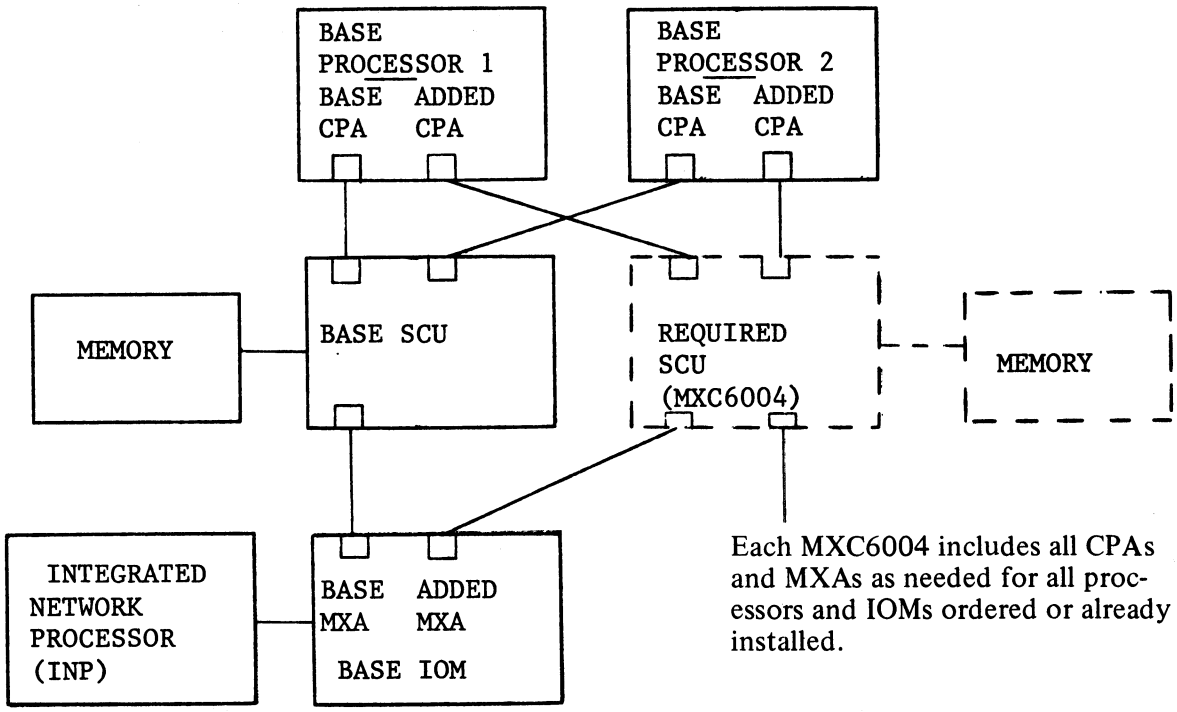


Figure 1-4. Upgraded Net Base System – DPS Models

D. Summary of Mainframe Replication Options (See Tables 1-1 through 1-3).

TABLE 1-1. NON-DPS SYSTEMS REPLICATION OPTIONS

MODEL AND TOTAL MEMORY	MAXIMUM SELECTIVE PROCESSORS	MAXIMUM SELECTIVE IOMs	SCUs		TANDEM SYSTEMS
			REQUIRED	OPTIONAL	
68/60	1	1			
192-512K Words			1	1-3	Yes, 2 CPS systems or module by module.
513-1024K Words			2	1-2	
68/80					
256-512K Words			1	1-7	Yes, 2 CPS systems or module by module.
513-1024K Words	3	3	2	1-6	
1025-1536K Words			3	1-5	
1537-2048K Words			4	1-4	

TABLE 1-2. SYSTEM CONTROLLER QUANTITIES PER SYSTEM

System Total Memory	68/60		68/80		DPS	
	Required[a]	Optional[b]	Required[a]	Optional[b]	Required[a]	Optional[b]
768KB/192KW	1	1-2	–	–	–	–
1024/256KW	1	1-3	1	1-7	1	1-7
1536KB/384KW	1	1-3	1	1-7	1	1-7
2048KB/512KW	1	1-3	1	1-7	1	1-7
3027KB/768KW	2	1-2	2	1-6	1	1-7
4096KB/1024KW	2	1-2	2	1-6	1	1-7
6144KB/1536KW	–	–	3	1-5	2	1-6
8192KB/2048KW	–	–	4	1-4	2	1-6
10204KB/2560KW	–	–	–	–	3	1-5
12288KB/3072KW	–	–	–	–	3	1-5
15336KB/3584KW	–	–	–	–	4	1-4
16384KB/4096KW	–	–	–	–	4	1-4

[a]Required = Quantity of SCUs required to support system total memory size. Main frame CPS number includes one SCU.

[b]Optional = Optional extra SCUs added selectively.

TABLE 1-3. DPS SYSTEMS REPLICATION OPTIONS

MODEL AND TOTAL MEMORY	MAXIMUM SELECTIVE PROCESSOR	MAXIMUM SELECTIVE IOMs	SCUs		TANDEM SYSTEMS
			REQUIRED	OPTIONAL	
DPS-1	0	3			Yes, module by module.
2048-4096K Bytes			1	1-7	
4097-8192K Bytes			2	1-6	
8193-12288K Bytes			3	1-5	
12289-16384K Bytes			4	1-4	
DPS-2	0	3			Yes, module by module.
2048-4096K Bytes			1	1-7	
4097-8192K Bytes			2	1-6	
8193-12288K Bytes			3	1-5	
12289-16384K Bytes			4	1-4	
DPS-3	0	3			Yes, module by module.
2048-4096KB			1	1-7	
4097-8192KB			2	1-6	
8193-12288KB			3	1-5	
12289-16384KB			4	1-4	
DPS-4	2	3[a]			
2048-4096K Bytes			1	1-7	
4097-8192K Bytes			2	1-6	
8193-12288K Bytes			3	1-5	
12289-16384K Bytes			4	1-4	

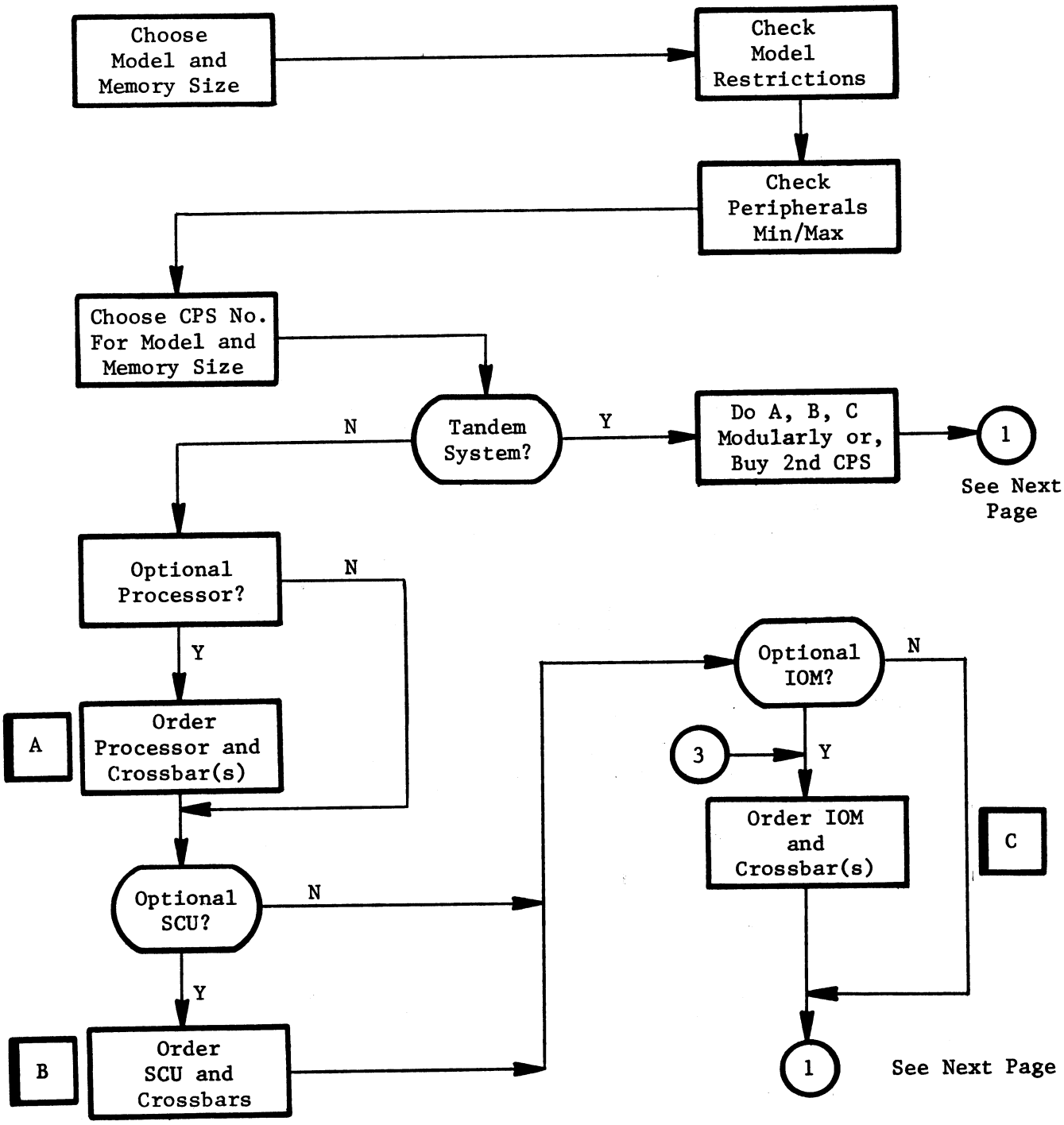
[a]The total of CPUs and IOMs cannot exceed eight.

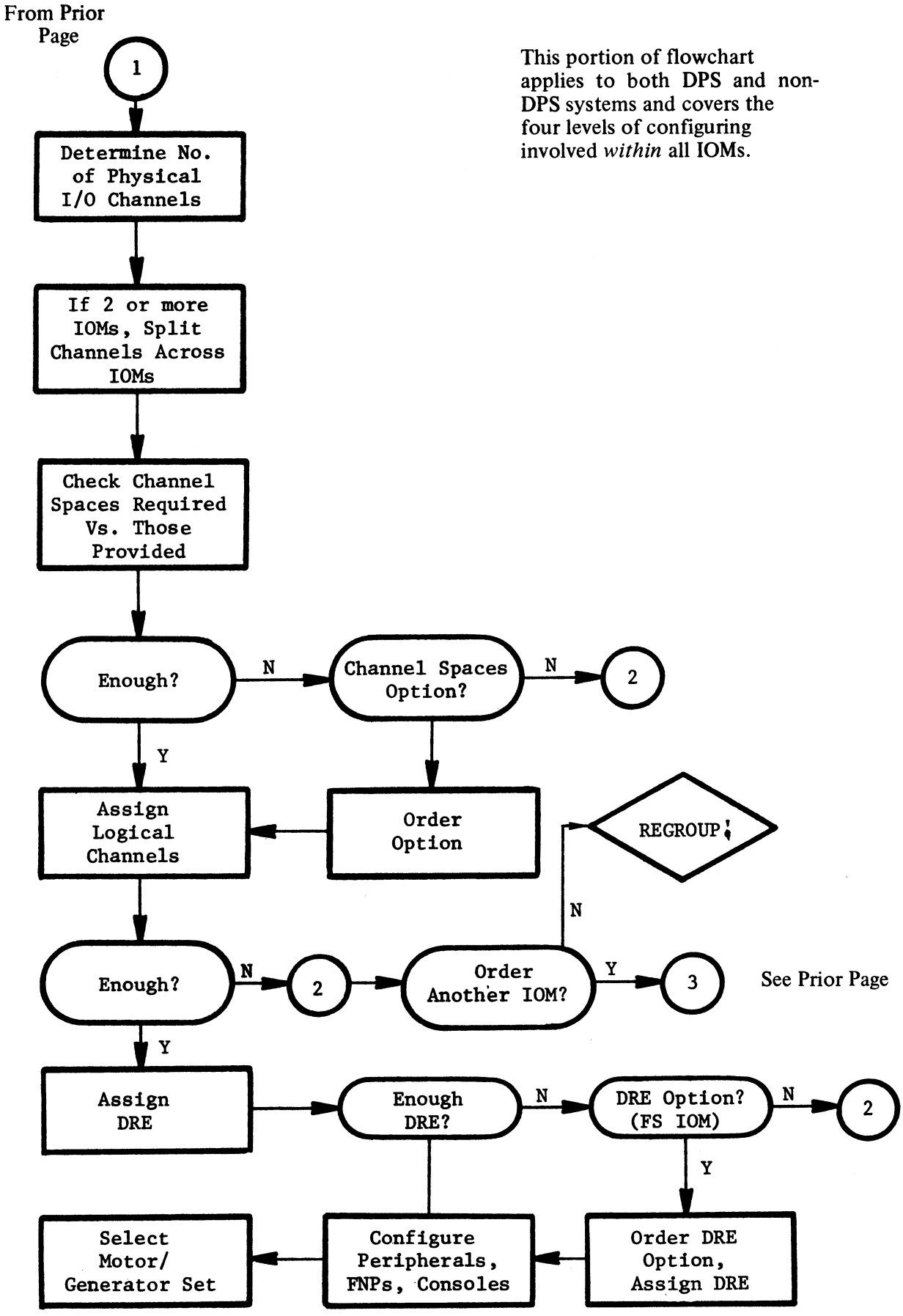
Section II

Master Flow Charts for Mainframe Configuring

A. Initial System Order

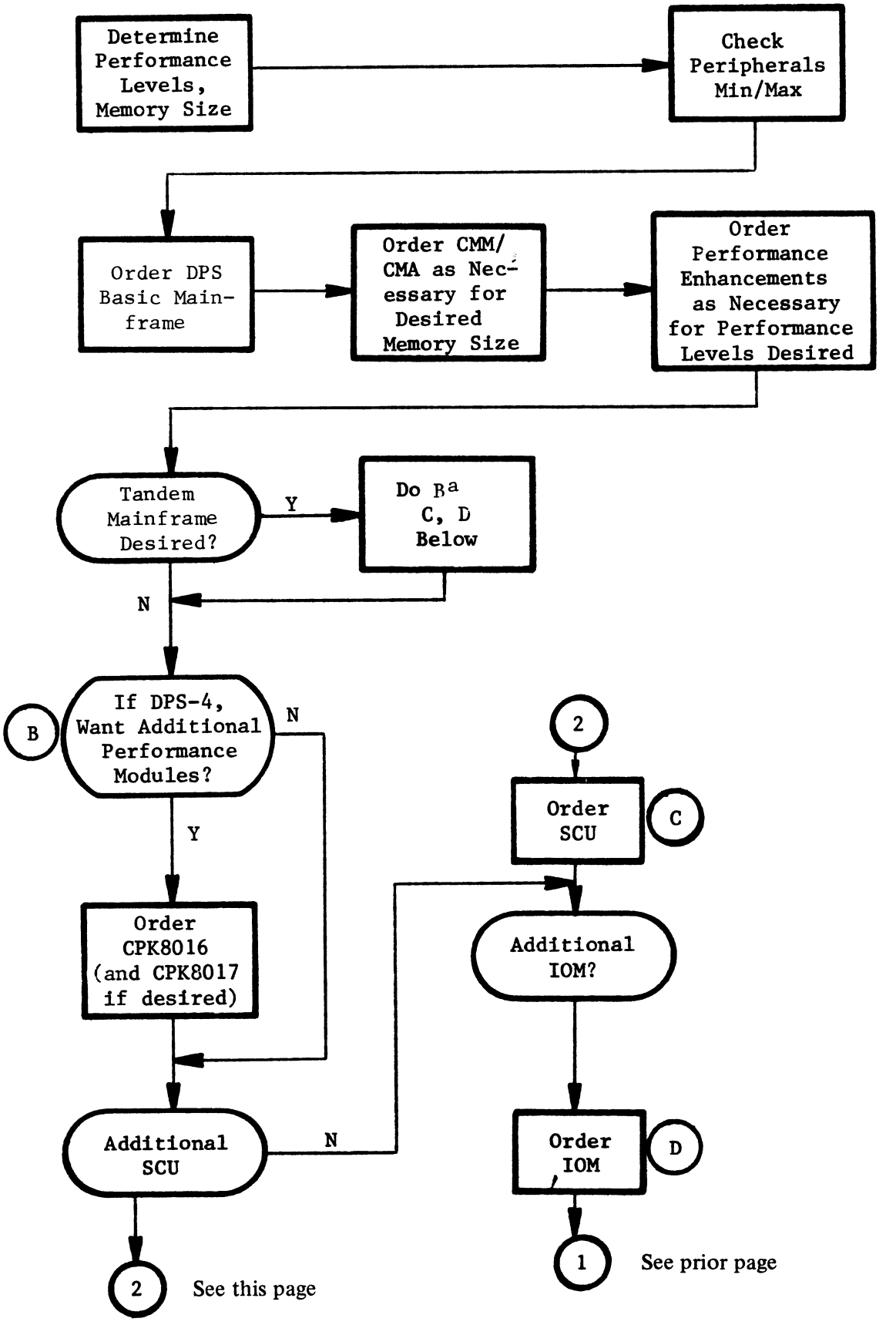
1. FOR NON-DPS SYSTEMS





This portion of flowchart applies to both DPS and non-DPS systems and covers the four levels of configuring involved *within* all IOMs.

2. FOR DPS SYSTEMS



[a]Yes at B means a 5th or 6th processor, since 4 processors are included in DPS-4.

Section III

Initial Order – Base Mainframe

A. Base Mainframe Configurator Tables (See Tables 3-1 through 3-3 and Figures 3-1 through 3-4)

1. NON-DPS FREESTANDING SYSTEMS (No FNP included)

TABLE 3-1. MODEL 68/60 BASE MAINFRAME – CPS8623 THROUGH CPS8636

Model	Central Systems Ident.	Basic Memory Size	Memory Upgrade Kits for Installed System[a]				
			192 – 256K Words	256 – 384K Words	384 – 512K Words	512 – 768K Words	768 – 1024K Words
68/60	CPS8623	192K Words/ 768K Bytes	CMK6035	CMK6036	CMK6037	CMK6038	CMK6039
↓	CPS8624	256K Words/ 1024K Bytes		CMK6036	↓	↓	↓
↓	CPS8626	384K Words/ 1536K Bytes			CMK6037	↓	↓
↓	CPS8628	512K Words/ 2048K Bytes				CMK6038	↓
↓	CPS8630	768K Words/ 3072K Bytes					CMK6039
↓	CPS8636	1024K Words/ 4096K Bytes					

[a]Memory upgrade kits contain all necessary memory addressing and SCUs if required.

Procedure:

1. Select the CPS number that provides the desired memory size.
2. If the system is installed and you wish to upgrade the memory size, use the CMK kits at right of appropriate CPS number.

NOTE:

K in memory size indicates a value of 1024. Maximum memory in system is 1024K words/ 4096K bytes whether two processors are used or not. Maximum is 512K words per SCU.

TABLE 3-2. MODEL 68/80 BASE MAINFRAME – CPS8824 THROUGH CPS8856

Model	Central System Ident.	Basic Memory Size	Memory Upgrade Kits for Installed System[a]					
			256 – 384K Words	384 – 512K Words	512 – 768K Words	768 – 1024K Words	1024 – 1536K Words	1536 – 2048K Words
68/80	CPS8824	256K Words 1024K Bytes	CMK6040	CMK6041	CMK6042	CMK6043	CMK6044	CMK6045
	CPS8826	384K Words 1536K Bytes		CMK6041				
	CPS8828	512K Words 2048K Bytes			CMK6042			
	CPS8832	768K Words 3072K Bytes				CMK6043		
	CPS8836	1024K Words 4096K Bytes					CMK6044	
	CPS8844	1536K Words 6144K Bytes						CMK6045
	CPS8856	2048K Words 8192K Bytes						

[a]Memory upgrade kits contain all necessary memory addressing and SCU's if required.

Procedure:

1. Select the CPS number that provides the correct memory size desired.

2. If the system is installed and you wish to upgrade the memory size use the CMK kits at right of appropriate CPS number.

NOTE:
K in memory size indicates a value of 1024. Maximum memory in system is 2048K words/ 8192K bytes whether two processors or not. Maximum is 512K words per SCU.

2. DPS SYSTEMS

a. Base mainframe (see Note 1 at the end of this section)
b. Memory expansion options (Note 6)
c. Processor incremental performance enhancements (Note 1)
d. Additional SCUs, IOMs (Note 5)
e. Additional communication network processors (Note 7)

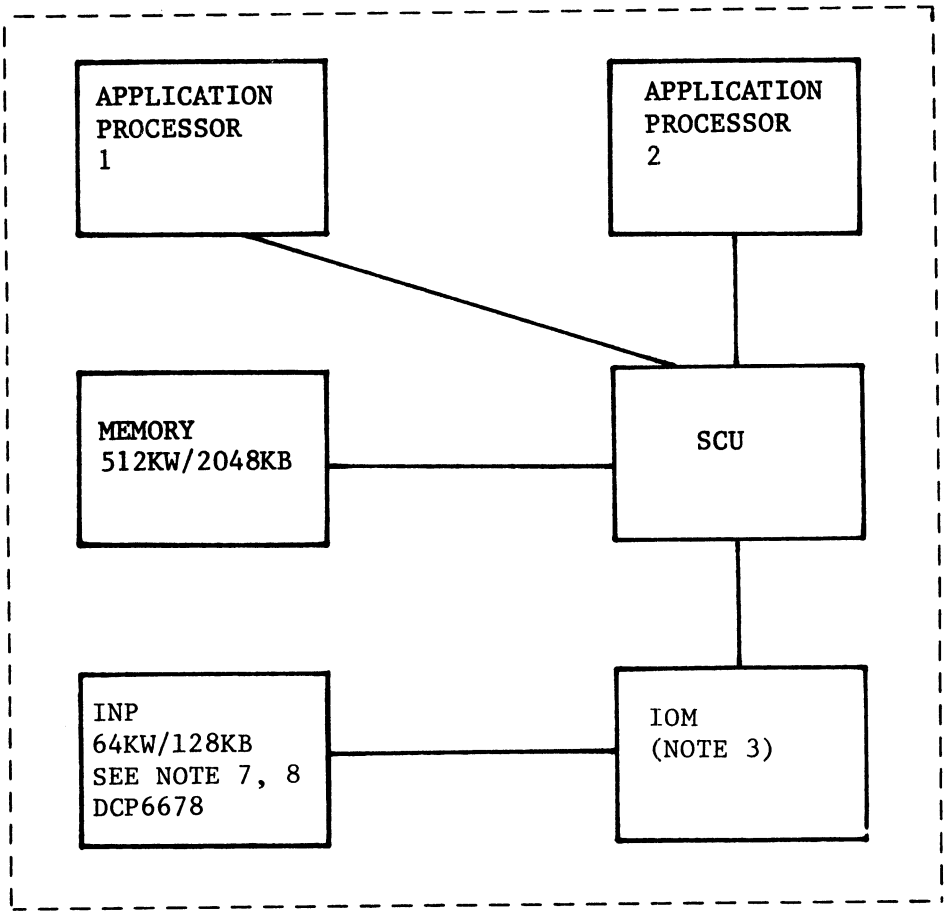


Figure 3-1. Base DPS CPS8802

TABLE 3-3. MEMORY EXPANSION OPTIONS

Memory Size	Memory Expansion Units										
512-768K Words 2048-3072K Words	CMM6052 CMA6052										
768-1024K Words 3072-4096K Bytes		CMM6053 CMA6053									
1024-1280K Words 4096-5120K Bytes			CMM6054 CMA6054								Order 2nd SCU MXC6004 Unless Already Installed
1280-1536K Words 5120-6144 K Bytes				CMM6055 CMA6055							
1536-1792K Words 6144-7168K Bytes					CMM6056 CMA6056						
1792-2048K Words 7168-8192K Bytes						CMM6057 CMA6057					
2048-2560K Words 8192-10240K Bytes							CMM6058 CMA6058				Order 3rd SCU MXC6004 Unless Already Installed
2560-3072K Words 10240-12288K Bytes								CMM6059 CMA6059			
3072-3584K Words 12288-14336K Bytes									CMM6060 CMA6060		
3584-4096K Words 14336-16384K Bytes										CMM6061 CMA6061	Order 4th SCU MXC6004

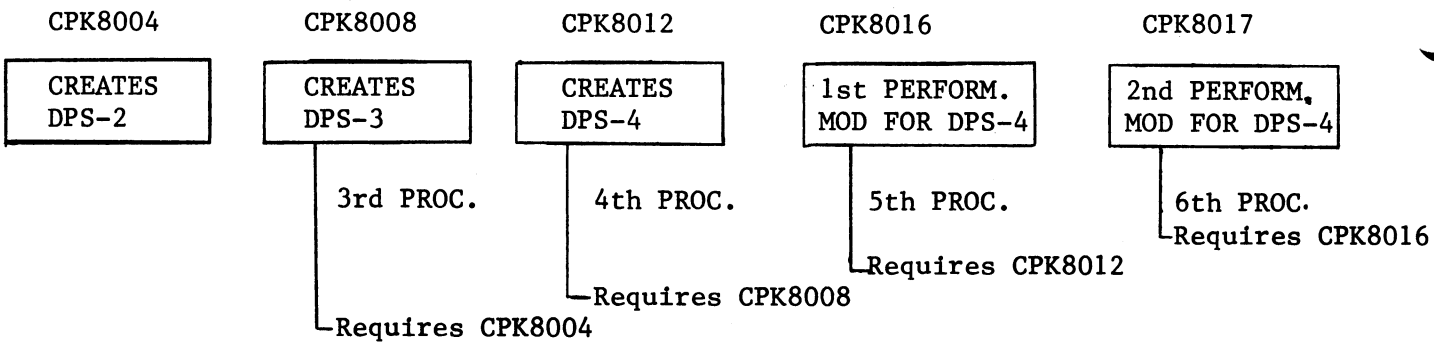


Figure 3-2. Processor Incremental Performance Enhancements

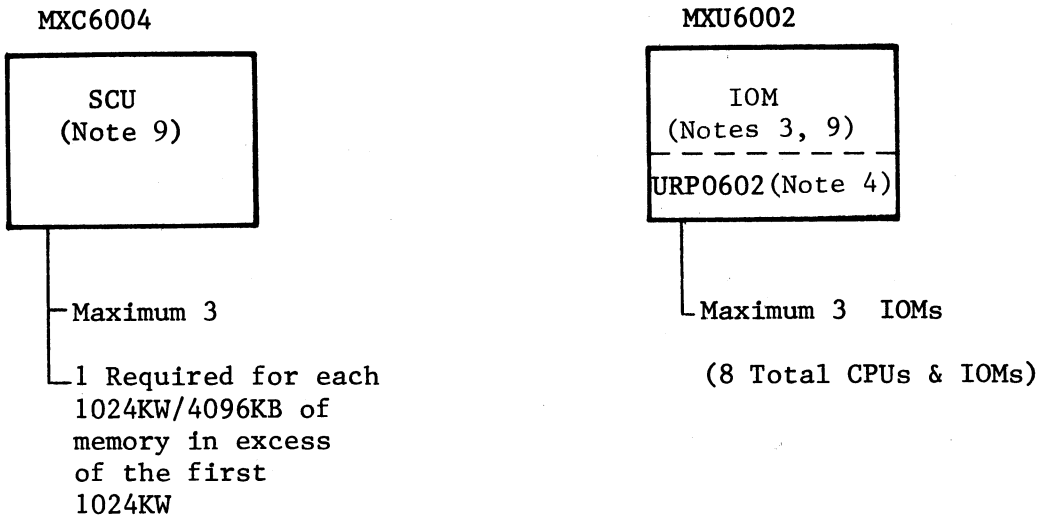


Figure 3-3. Additional SCUs and IOMs

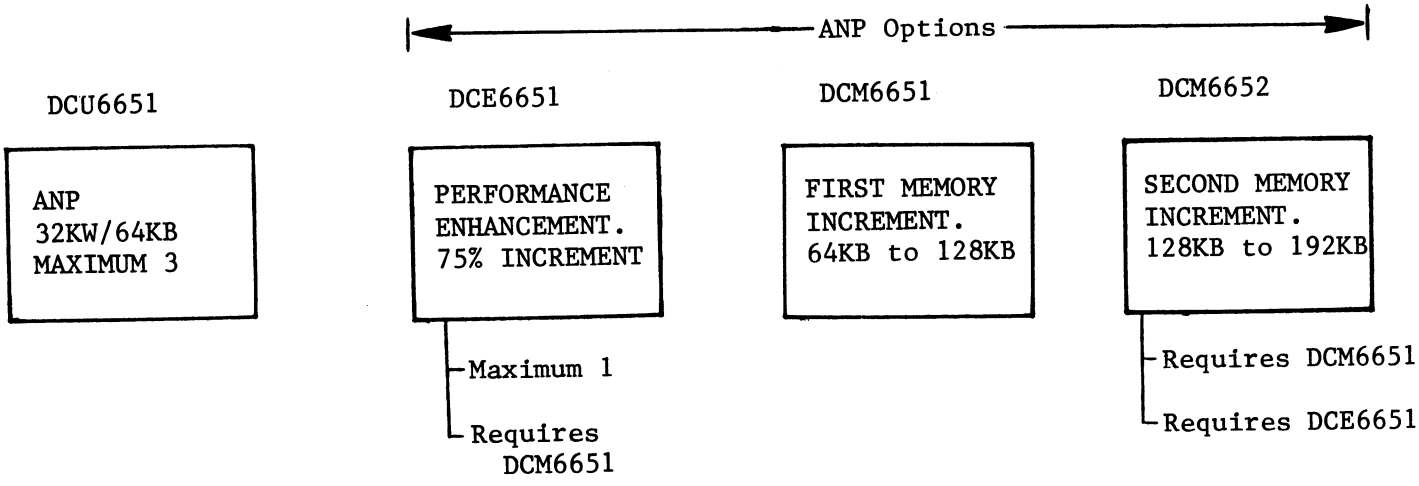


Figure 3-4. Additional Communication Network Processors (ANPs)

NOTES:

1. CPS8802 must always be ordered to provide the base mainframe (includes all components shown in box with dotted outline). This is base mainframe for entire DPS range of performance levels – DPS-1, -2, -3, -4. DPS-2 level is obtained by the addition of a performance enhancement as shown. DPS-3, -4 can be obtained only if DPS-2 is configured. DPS-1, -2, -3, -4 designations do not imply relative performance levels (i.e., DPS-2 is not twice as fast as DPS-1). All mainframe components are freestanding, except that base processors are packaged in one cabinet, and memory to the maximum of 1024K words/4096K bytes per SCU is contained in the SCU cabinet. Each processor, SCU, and IOM has own power supply.

2. At lease one moter/generator set is required but is not included in base main price. (See *Level 66 Configuration Guide.)*

3. For each IOM there are components which must be configured and considerations which apply within the IOM. See Section IV.

4. Every system must have at least one URP subsystem. You have the choice of using a unit record processor (URP0602) within an IOM cabinet, sharing the IOM power supply, or using a freestanding unit record processor (URP0600) which has its own power supply. Use of URP0602 affects the physical I/O channel capacity of IOM.

5. A minimum tandem mainframe consists of two processors, two SCUs, and two IOMs. The base main frame (CPS8802) always contains two processors. Additional SCUs, and IOMs must be separately configured.

6. Use the memory expansion table to configure memory beyond the base size (512K words/2048K bytes) on an initial order or for a memory size upgrade on an installed system. Each row represents a specific increment. Choose all increments necessary to reach a given total size of memory from any starting size. Remember that a second system controller must be used to support memory size greater than 1024K words/ 4096K bytes.

7. To complete the configuring of 68/DPS, INP/ANP communications processor, refer to *Configuring Level 6-Based FNPs* in the Level 66 Configuration Guide.

8. The Level 68/DPS INP is a full powered DN6678 (DCP6678) and includes: 64K words of memory, and an INP console. The Multics Communication System (MCS) does not support memory greater than 32K words.

9. All necessary ports to connect all processors and all IOMs to all SCUs are included in the price of the add-on components. You do not configure them in DPS systems.

Section IV

Configuring Within IOM

A. Objectives of this Section

1. To show how you determine the number of physical I/O channels required for the desired peripheral subsystems.

2. To show how, by using the information from number 1 above, you determine the quantity of 12" x 12" circuit boards required to contain the electronic logic for the number and type of physical I/O channels you desire. Also, in this section you will determine whether there are sufficient channel board spaces available on a standard basis or via option in the Level 68 system you wish to configure.

3. To show how, by using the information from number 1 above, you determine how many logical channels or data paths must be assigned for the quantity of physical I/O channels you wish. We will also explain the role of logical channels, indicate how many may be assigned optionally beyond the quantity required, and describe how they are physically assigned.

4. To show how, by using the information from number 3 above, you determine how to assign the scratchpad capabilities furnished by the data rate expansion (DRE) feature. We will also review the role of DRE feature, and explain how it is obtained and how it is physically assigned to appropriate logical channels.

B. Steps for Configuring Within a Freestanding IOM

1. The base IOM (freestanding systems) has no type number. All IOMs configured selectively beyond the base IOM are freestanding. The chart in Figure 4-1 applies to all freestanding IOMs.

   a. Freestanding IOMs may be obtained in 3 ways:

      - o One is included in the base CPS number of freestanding systems.
      - o One or more may be ordered optionally on your initial order along with the CPS components. One more is maximum on 68/60 and up to 3 more on 68/80 and DPS systems.
      - o One or more may be ordered optionally as add-on components after your system has been installed. Limits are the same as above.

   b. Each freestanding IOM, whether optional or included in the CPS number, has its own power supply.

   c. No ports for connection to SCUs on non-DPS systems are included in the price of optional IOMs, but a port (MXA6001 addressing feature) must be configured for each SCU in the system for non-DPS models (does not apply to DPS models).

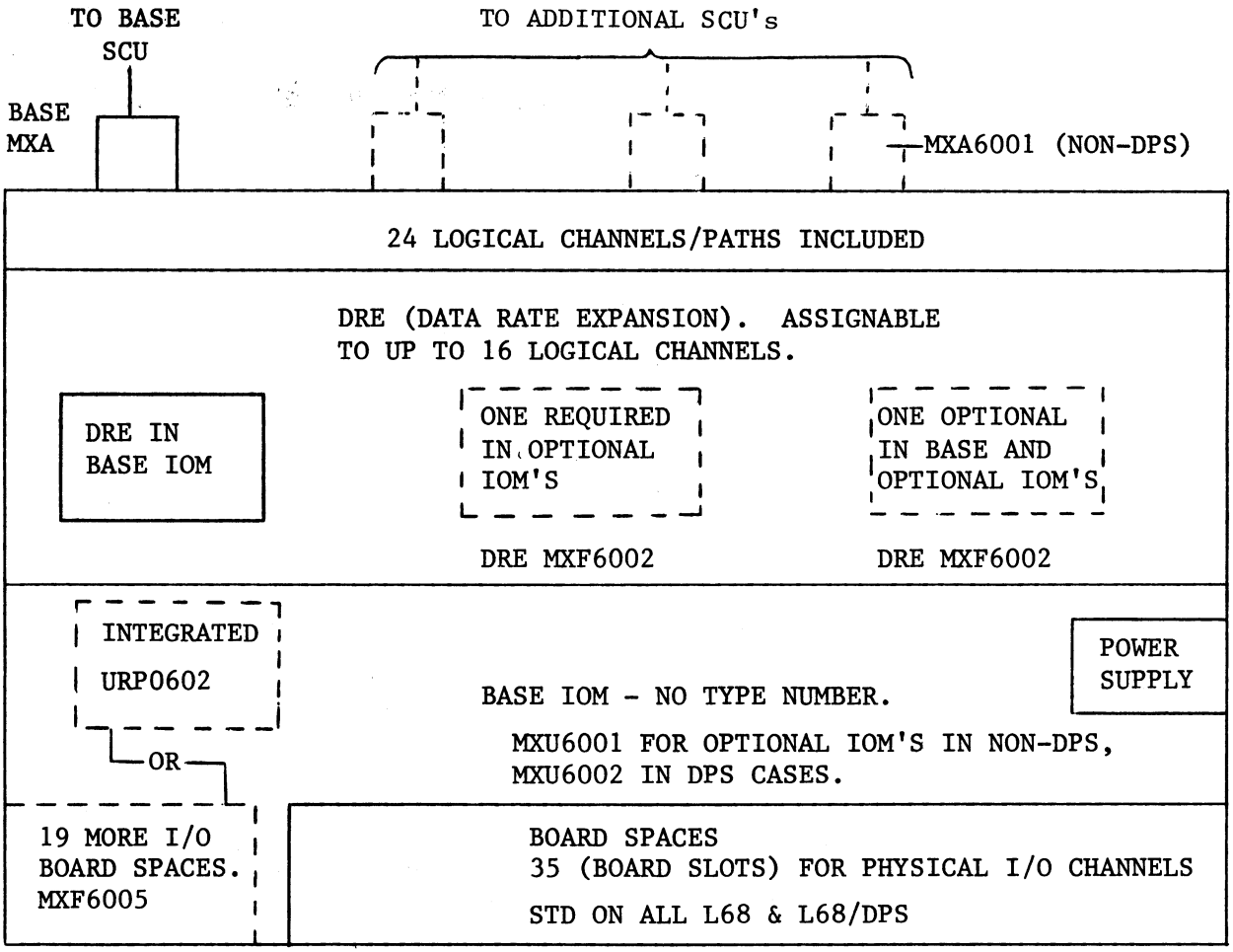


Figure 4-1. Block Diagram of Freestanding IOMs

2. Determine the quantity of physical I/O channels your planned mix of peripheral subsystems will require. See Section C.

3. Determine how many spaces for 12" x 12" circuit boards will be required based on Step 2, and how many spaces are furnished and can be added optionally, if any, for the Level 68 model you are configuring. See Section C.

4. Determine how many logical channels or data paths must be assigned (from the built-in complement of 24) for the quantity of physical I/O channels from Step 2. Determine how many more you wish to assign optionally, if any. See Section D.

5. Determine to how many, and which, logical channels assigned in Step 4 you wish to assign the scratchpad capability which is furnished by DRE feature (data rate expansion). See Section F.

C. **Determining the Quantity of Physical I/O Channels Required for Your Peripheral Subsystem Mix.**

1. Use the Table 4-1 below or the charts in Section 4, paragraph 3.

   a. Remember that MSP0602/0603 can be configured with or without MSU0500 spindles. If MSU0500 is not used, there can be one or two MSPs per subsystem, each with one or two prime channels. Each prime channel can be equipped with a switched channel path feature to terminate in an IOM physical channel.

   b. If MSU0500 spindles are included, with or without MSU0402/0451 spindles, MSPs cannot be configured with two prime channels.

   c. There can be one or two MSPs per subsystem, unless the subsystem includes MSU0500 spindles. Such subsystems can have up to 4 MSPs. Each MSP has one prime channel which can optionally be equipped with a switched channel path feature to terminate in an IOM physical channel.

2. Explanation of use of each column in Table 4-1 below.

   a. Make a separate calculation for each subsystem of each type. There may be different options used on each (represented by (1)).

   b. (2) represents the prime IOM channel always included in price of each subsystem device processor.

   c. (3) represents those device processors where a second prime channel can be configured. In case of MTP (MSP0602/0603 when no MSU0500 is configured) both channels can operate simultaneously. In case of DN6632/6670 and DPS INP/ANP, the second prime channel is non-simultaneous, acting as a back-up to the first, and not effective until after a Multics warm restart or reboot has occurred.

   d. (4) indicates that the path from a prime channel can be switched to 2 different IOM channels. The switch can be either electronic, controlled transparently by Multics and contained in the device processor (URP, MTP, MSP0602/0603), or can be an external, manually controlled peripheral switch. (See the Level 66 Configuration Guide.)

   e. (5) indicates the two cases where a switched path feature can be applied to a second prime channel. This switch could be electronic or manual as discussed in 4 above.

   f. (6) indicates the maximum possible number of physical I/O channels in an IOM for one subsystem of a type. It is the sum of (2) plus (3), (4), and (5), where these are applicable and actually configured.

   g. In column (7), you fill in this number. Remember that you use one repetition of each row for each subsystem of a given type. There could easily be different maximums for each subsystem when multiple subsystems of same type are used.

   h. For column (8), multiply for each row (and each subsystem of same type) the figure in (7) times the sum of (2), plus (3), (4), and (5) as applicable and as actually configured.

i. Multiply the figure per subsystem of each type in ⑧ times the figure in ⑨. Add the figures in all rows for all subsystems and place that figure in ⑩. Now go to Section D to see if the Level 68 model you are bidding has sufficient spaces for the required number of physical channel circuit boards ⑨.

TABLE 4-1. PHYSICAL I/O CHANNELS REQUIRED IN IOM

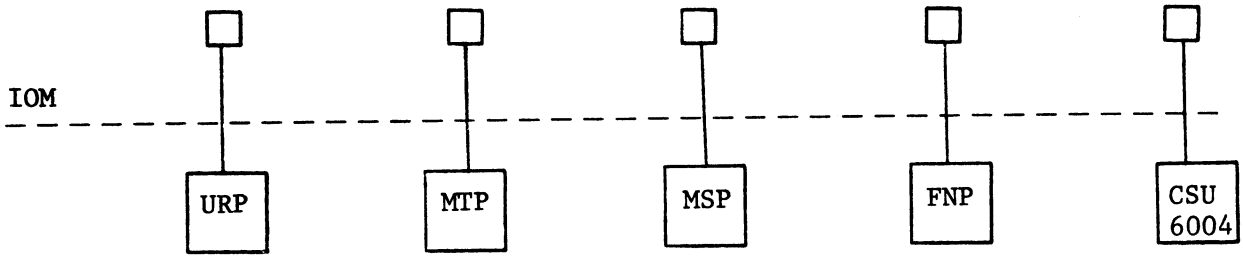
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
Sub-System	Standard Prime Channel	Optional Prime Channel	Optional Switched Path-Std Prime Channel	Optional Switched Path-Opt Prime Channel	Max IOM Channels This Sub-system	No. Sub-systems This Type	Total Physical Channels Required in IOM	Channel Boards Per Channel	Total Required Channel Slots
URP	1	-	1	-	2			3	
MTP	1	1[a]	1	1	4			3	
MSP0602 0603 w/o MSU0500	1	1	1	1	4			3	
MSP0602/ 0603 with MSU0500	1	-	1	-	2			3	
CSU6004	1	-	-	-	1			1[b]	
INP	1	-	-	-	1			1	
DN6632/ 6670	1	1	-	-	2			1	

[a]Required, not optional, when more than 8 tape units will be in subsystem.

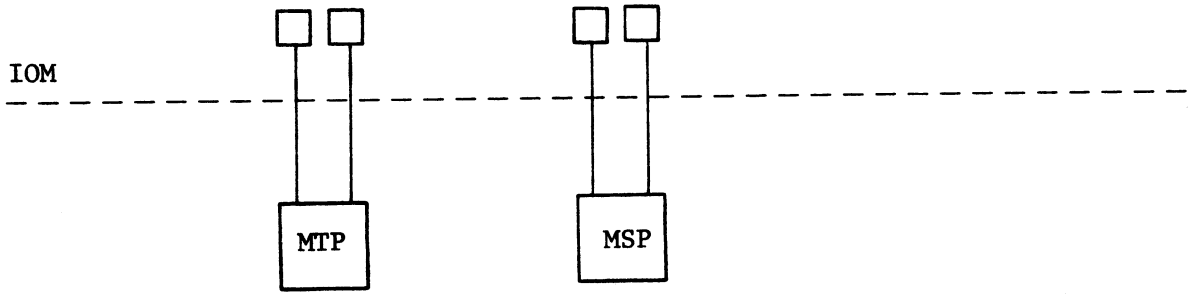
[b]If used in system with 384K words/1536K words or more, add 1 more board per channel (2 boards total per subsystem).

3. Alternate table for determining quantity of physical channels required in 10M (channel terminations). See paragraph d.

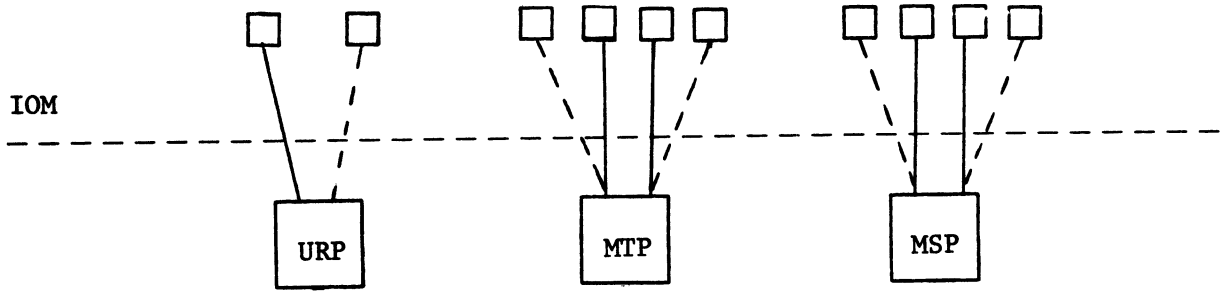
a. Each peripheral processor includes one physical IOM channel in its price.



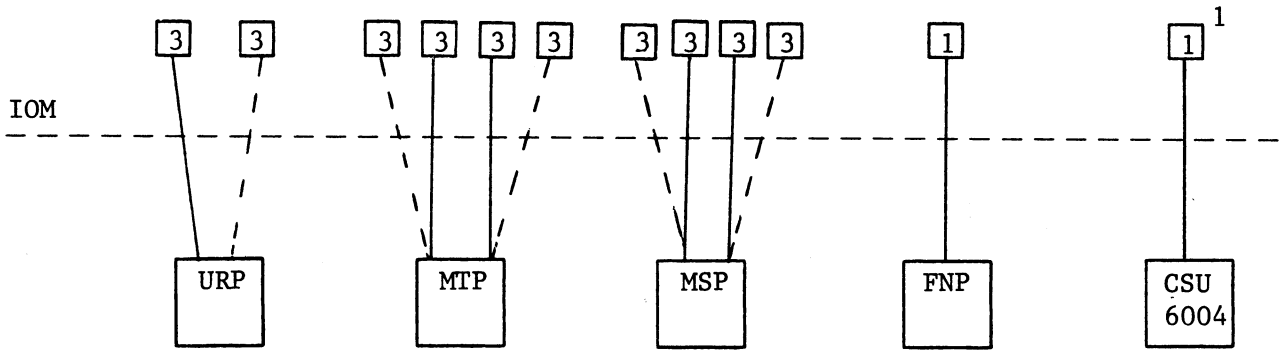
b. Additional simultaneous channels can be added to MTP, and MSP (if no MSU0500 spindles configured).



c. Software-switched, non-simultaneous channel features can be added to URP, MTP, and MSP channels.



d. Each □ represents physical channel (termination) in IOM, each requiring 1-3 circuit boards to carry the channel logic



D. Determining How Many Spaces are Available Per IOM for the 12" x 12" channel Logic Boards for Physical I/O Channels

1. Spaces needed for carrying electronic logic boards for the required number of physical channels are based on Section C above.

2. Refer to Figure 4-2. Once you have configured two or three systems you will probably be able to come directly to this figure for determining both the channel spaces available and the quantity required for each physical channel, by-passing Section C above. In any event before you use the figure below, you must know the number of physical I/O channels you need for each subsystem (i.e., channel terminations needed in IOM).

3. Figure 4-2 gives you the information necessary to determine how many peripheral subsystems can be configured in a Level 68 system.

4. If you cannot configure the desired number of peripheral subsystems and their complement of physical channels and switched paths, consider the following alternatives.

   - o Bid a second IOM if the Level 68 model permits and the prospect will allow it.
   - o Use fewer simultaneous channels and/or switched paths.
   - o Use fewer subsystems of same type.
   - o Use fewer subsystems.
   - o Use different mix of subsystems.
   - o Change the Level 68 model you are bidding.
   - o In case of a freestanding IOM use URP0600 (freestanding) instead of URP0602 (in IOM cabinet).

5. Determine next the logical channels or data paths which must be assigned to each physical channel and switched path and the quantity which may optionally be assigned. See Section E below.

6. Table 4-2 shows the number of circuit boards required for each physical channel termination in IOM. Use this to determine how many peripheral subsystems can be configured per Level 68 IOM. Prime channel is the physical channel in the device processor price, and the physical channel which can be added optionally to run simultaneously with first (except for FNP).

[1] Two boards if more than 256K words/1024K bytes in system.

TABLE 4-2. IOM PHYSICAL I/O CHANNEL BOARD SPACES ALLOCATION

	Model	Available Spaces for Boards			Boards Required			
					Subsystem		System Memory Size	
		Basic	Optional	Total	Type	Prime[d]	To 256K Words	Over 256K Words
Freestanding IOM					URP	1[b]	3	3
					MTP	1[b]	3	3
					MTP	2[b]	6	6
	68/60	35	19(MXF6005)	54	MSP	1[b]	3	3
	68/80	35	19(MXF6005)	54	MSP	2[b]	6	6
	68/DPS	35	19(MXF6005)	54	FNP	1[c]	1	1
Freestanding IOM With Int. URP	68/60	35	–	35	Sys Con	1	1	2
	68/80	35	–	35	CSU6004			With CSF6004[a]
	68/DPS	35	–	35				

[a]CSF6004 must be ordered.

[b]Add 3 spaces required for each switched or other non-simultaneous channel path used.

[c]Add 1 space required for each additional IOM prime channel connected (via DIA).

[d]This column represents the number of prime channels to be configured in the subsystem. See Section E to determine number of physical channels required.

E. Determining Logical Channel Assignments

1. Rules for assignment of IOM logical channels to physical channels.

   a. Every physical channel must be assigned one logical channel or data path. URP, MTP, and MSP may use more than one logical channel per physical channel, as explained below.

   b. Logical channels are related to physical channels by wiring and logic chips on the pertinent IOM logic boards. Assignment is established onsite by the FE according to the mix of required and optional logical channels specified by you.

   c. A table showing the assignment of logical to physical channels and of physical channels to peripherals is given to Multics at system startup time. Accordingly, Multics always knows what logical channels to use (thus physical channels) to reach a given device processor, console, or FNP.

      1) In effect Multics "sees" the peripherals it wants to reach via the logical channels.

      2) The logical channel concept provides a link to user program buffer areas (their size and locations). Without such a link the transfer path to/from memory could not be established. Review the IOM outline for the principle used, involving secondary mailboxes and connect channel mailbox.

2. Why assign more than one IOM logical channel to a physical channel?

   a. Use of multiple non-simultaneous logical channels or data paths per physical channel is our approach to the IBM concept of block multiplexing (BMX) type of channel. We both use similar principles with different nomenclature.

   b. Use of multiple logical channels per physical channel allows multiple places to which Multics can send or can queue I/O commands.

      1) As long as a logical channel is available, Multics can send the next I/O command to a given subsystem, even though the physical channel is busy with data transfers for a prior operation initiated through another logical channel. Otherwise, with a single logical channel, the physical and logical channel would be tied up during the data transfer and interrupt sequence, preventing the overlapped stacking of the next I/O command by Multics. Multics would have to wait for an opportunity to gain access to the single channel.

      2) The effect is potentially greater subsystem throughput by using the physical channel more efficiently, stacking commands in front of the subsystem at any time as long as a logical channel is available.

         Looking at it another way, the use of more than one logical channel per physical channel (block multiplexing) allows multiple I/O operations to be in some stage of execution concurrently. There can be as many concurrent stages as logical channels assigned to the subsystem involved. In the URP, for example, there could be as many as 7 card-reading/card-punching/line-printing operations simultaneously, using one physical channel.

   c. Summary of benefits of assigning more than one logical channel to a physical channel.

      1) Greater subsystem throughput.

      2) Use of fewer physical channels.

      3) Larger number of I/O operations in some stage of execution concurrently.

      4) Better use of physical channels.

      5) Combines with rotational position sensing (RPS) in disk subsystems to increase subsystem throughput further.

   d. See Figures 4-2 and 4-3.

3. Subsystems allowing multiple logical channels per physical channel.

   a. In Unit Record Processor (URP) subsystems, there must be one logical channel assigned to each unit record device connected to URP. A specific logical channel is assigned to each device.

      1) URP can handle up to 7 unit record devices.

2) URP, in combination with its channel and 1-7 logical channels in IOM, performs a block (unit record) multiplexing function, allowing up to 7 devices to run simultaneously. URP buffers a full physical record from/for each device and assigns each record to the IOM physical channel as soon as last record has transferred. Each unit record device must be permanently preassigned to a logical channel to be used by Multics in issuing commands to it. The logical channel controls the transfer into memory to/from the proper buffer area for the device concerned.

b. In Magnetic Tape Processor (MTP) subsystems, a second logical channel may optionally be assigned to each physical channel.

1) Note that the customer may assign more logical channels optionally if he has them available. The figures for optional channels above are based on those found sufficient for the usual customer site. Conceivably, a system with a large number of tape drives, a planned high multiprogramming depth (MPD),and heavy tape I/O activity might benefit from assigning more logical channels.

2) The value of the second logical channel for each physical channel is that it allows Multics to send a new command to an open logical channel, even though the physical channel may be transferring data under command of another logical channel assigned to the subsystem. As soon as the first operation terminates, a second could be initiated immediately from the command standing-by in the second logical channel. Multics could then send another command to the first logical channel, which is now open again. If only one logical channel is used, Multics cannot have any next command standing-by when a command is already in operation.

c. Disk subsystems

1) A normal useful maximum of logical channels for a mass store subsystem is eight regardless of the number of physical channels or MSPs in the particular subsystem. This figure includes the required logical channel per physical channel used in the subsystem involved.

2) MSP and disk spindles obtain automatic latency reduction via rotational position sensing and block multiplexing of the physical channel(s) involved. Both features can increase subsystem throughput and should always be used, at least on single-channel subsystems. They depend on multiple logical channels per subsystem.

3) The number of logical channels assigned for a subsystem should not normally exceed the number of spindles in the subsystem. There is little or no gain with a greater number of logical channels.

4) The number of logical channels assigned also should not be greater than the average anticipated multiprogramming depth (MPD). MPD would in general determine the average maximum possible I/O command queue size, thus dictating the usable number of logical channels.

5) The greatest benefit from multiple logical channels occurs on a single-channel MSP. With two-channel subsystems, commands tend to be serviced almost as soon as they are delivered to the subsystem. As a result, there is not as much chance to have command queues build up; thus there is less relative effect from multiple logical channels in a dual-channel subsystem case. Dual-channel systems will probably give greater throughput in all cases, especially where the subsystem includes more than four or five disk units.

d. See Figures 4-2 and 4-3 for determining required and optional logical channels.

4. Physical/logical channel concepts

a. Multiple logical channels/paths per physical channel. (See Figure 4-2).

b. Linkage to program to complete data transfer path (see Figure 4-3).

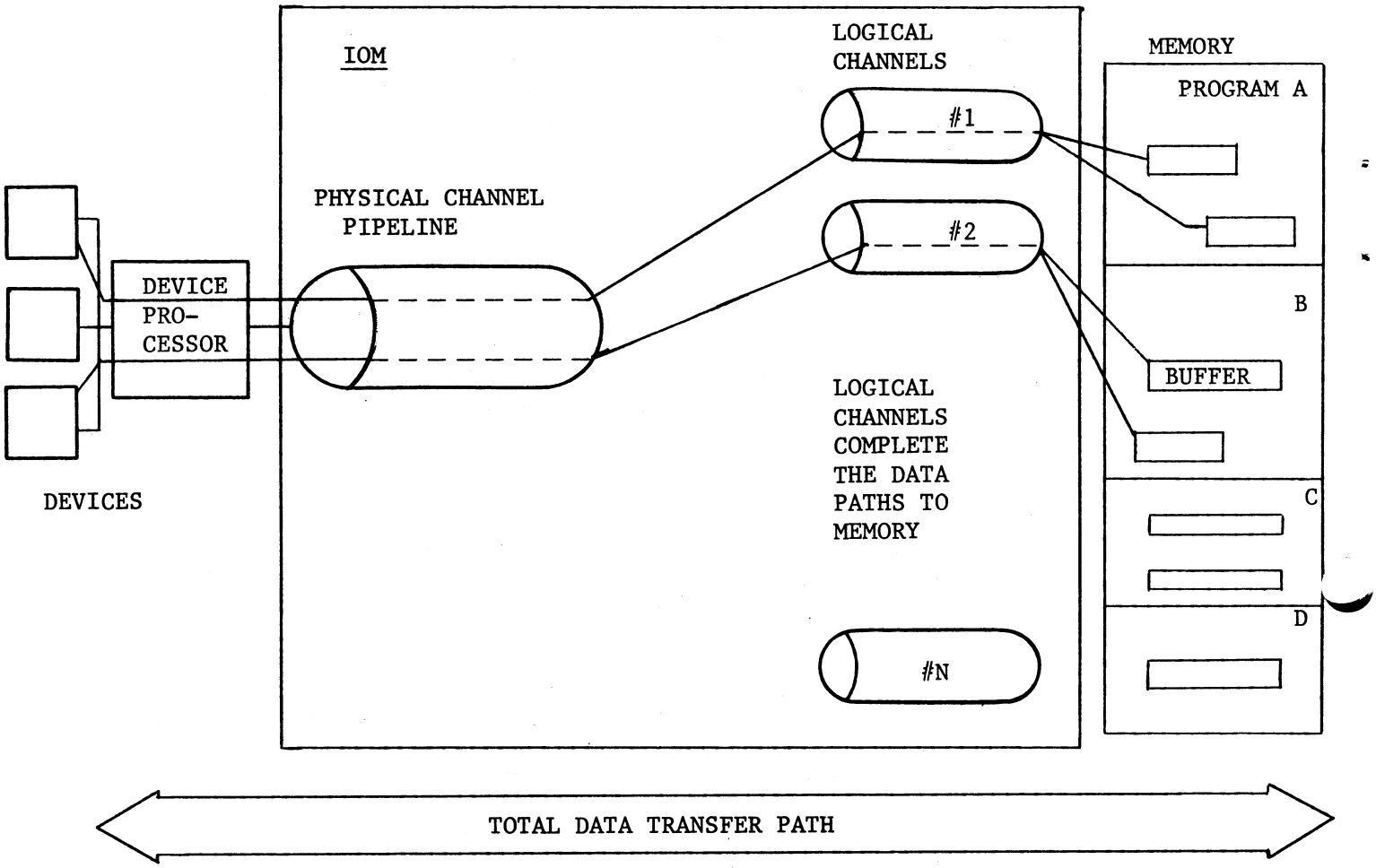


Figure 4-2. Multiple Logical Channels/Paths per Physical Channel

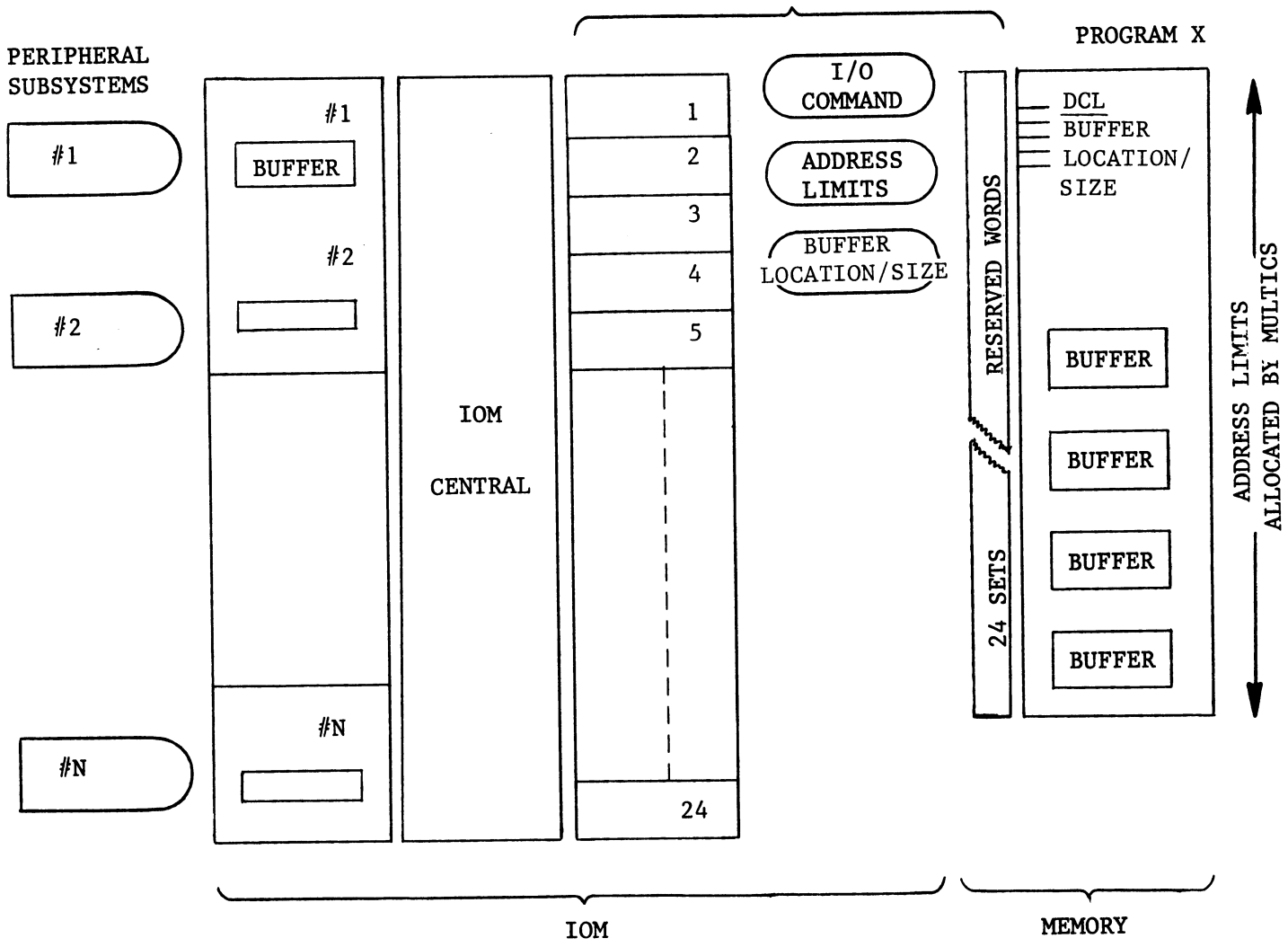


Figure 4-3. Linkage to Program to Complete the Data Transfer Path

5. IOM logical channel/data path assignment – tape and disk subsystems.

   a. Single-channel MTP (1x8) or single-channel MSP subsystem. (See Figure 4-4.)

   b. Dual-channel MTP (2x16) or dual-channel MSP or multi-MSP subsystem. (See Figure 4-5.)

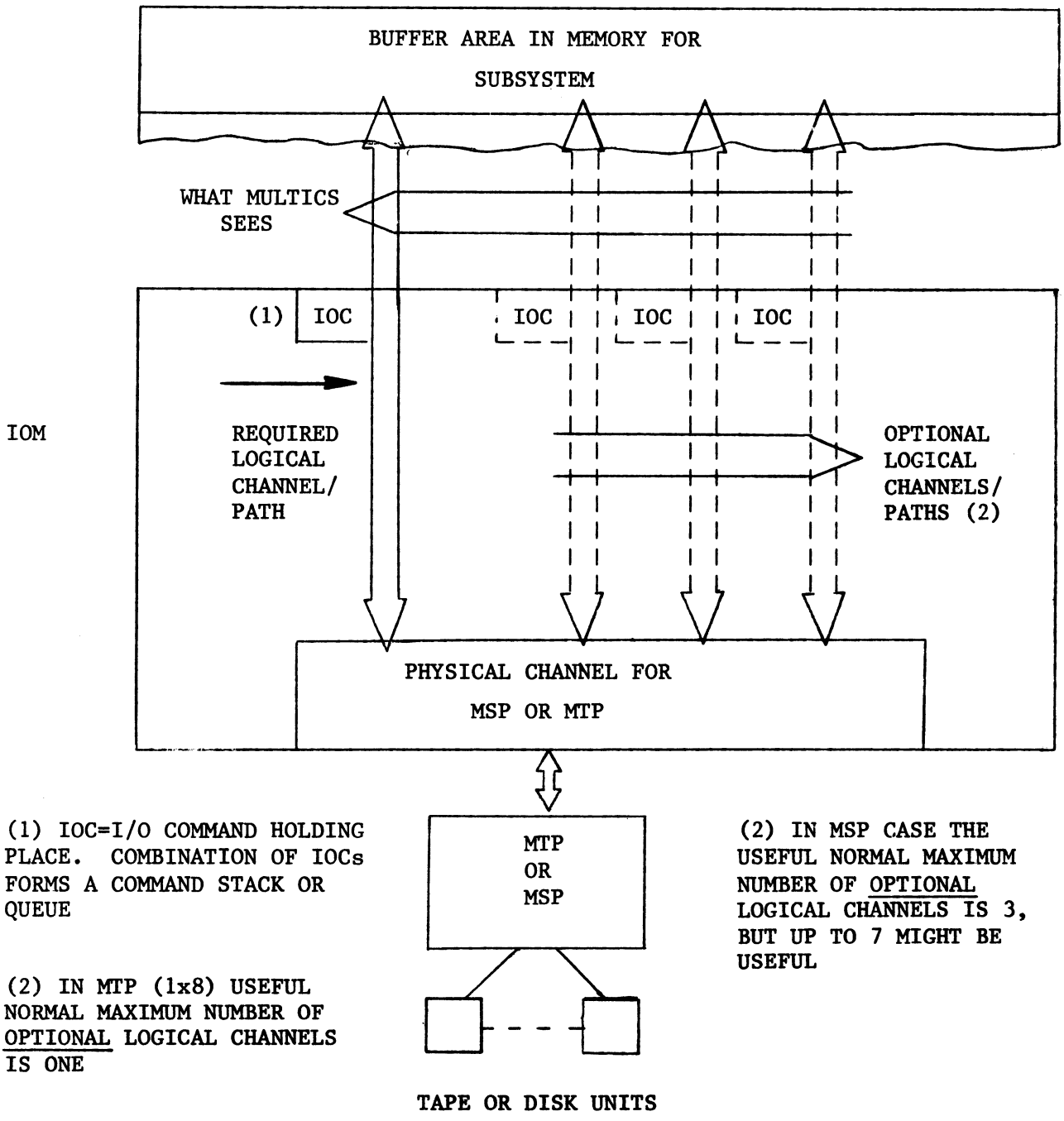


Figure 4-4. Single-Channel MTP (1x8) or Single-Channel MSP Subsystem

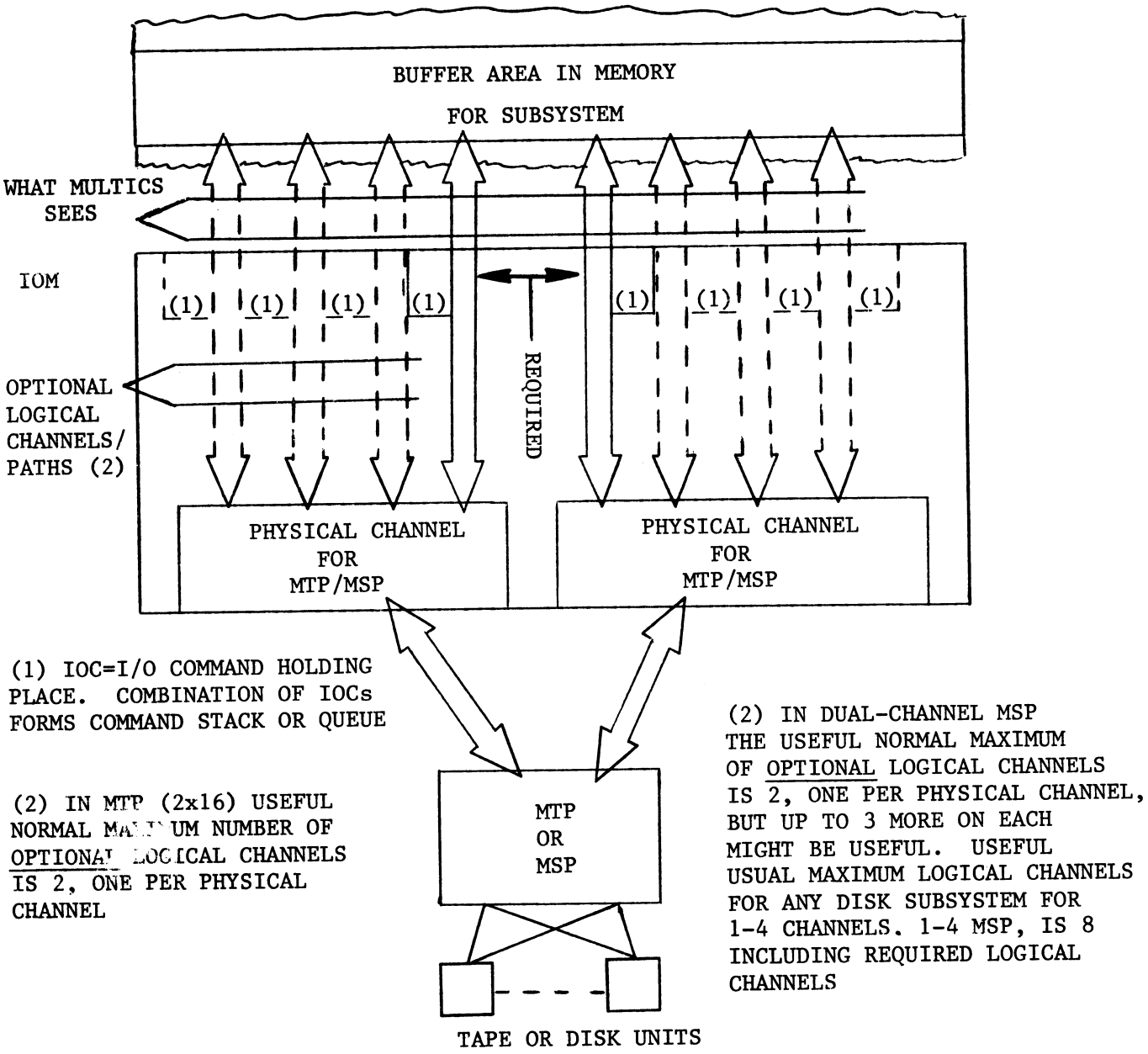


Figure 4-5. Dual-Channel MTP (2x16) or Dual-Channel MSP or Multi-MSP Subsystem

6. Logical channel assignments for Front-end Network Processors and Consoles (see Figure 4-6).

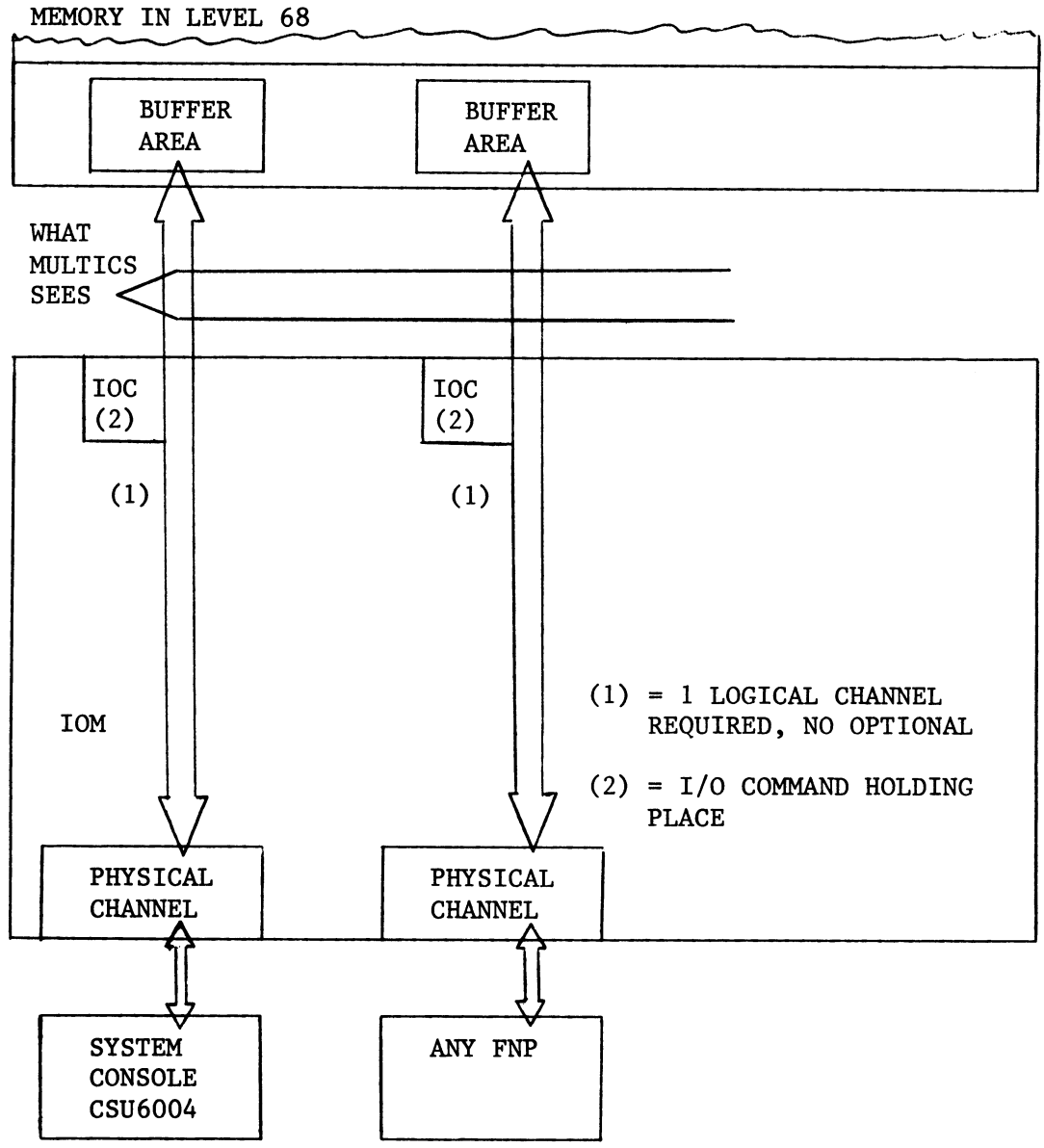


Figure 4-6. Logical Channel Assignments for Front-end Network Processors and Consoles

7. Logical channel assignments for Unit Record Processor subsystem (see Figure 4-7).

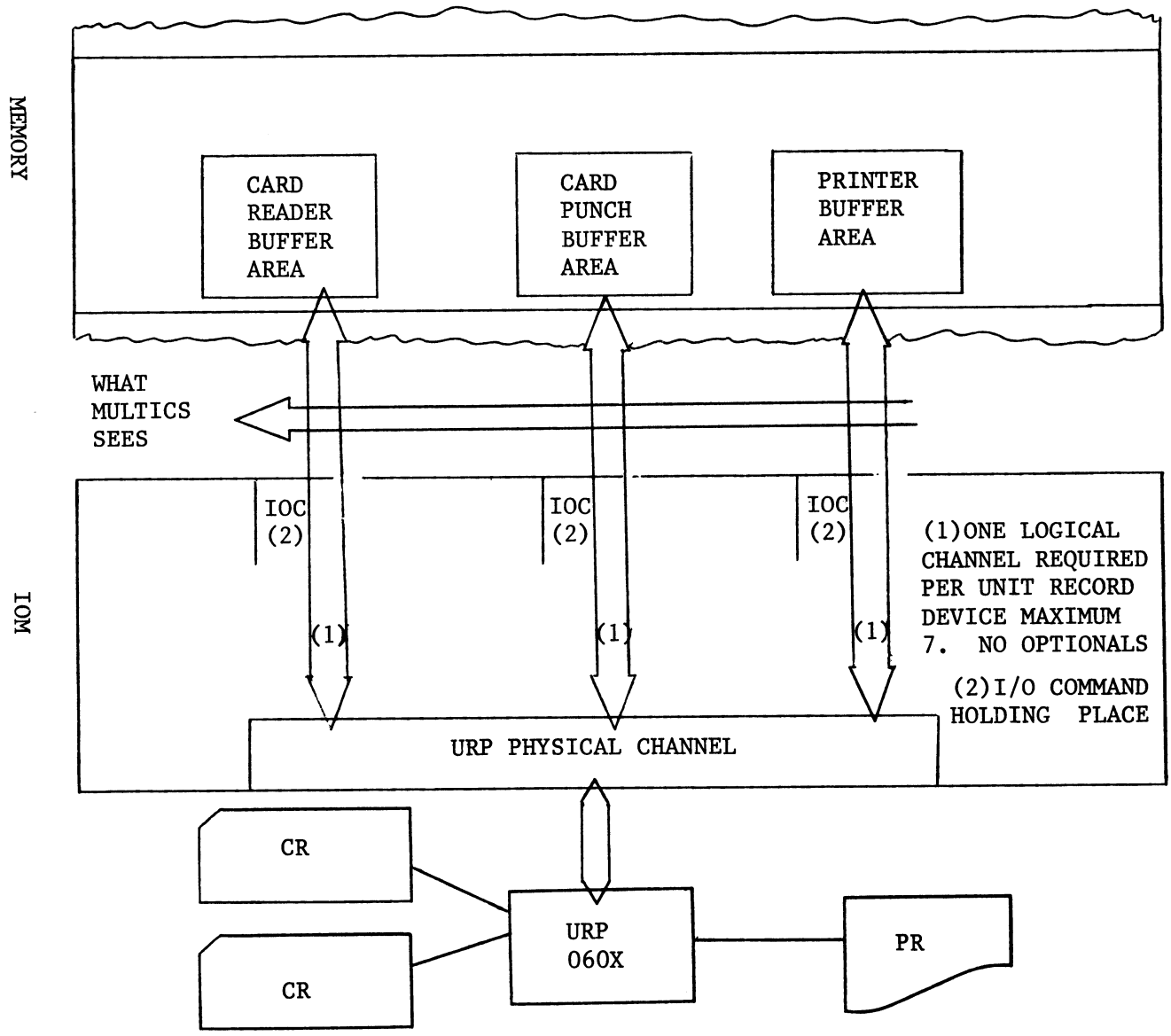


Figure 4-7. Logical Channel Assignments for the Unit Record Processor Subsystem

8. Table 4-3 is a summary of IOM physical and logical channels/paths per peripheral subsystem. Use it as a convenient summary to know how many physical and logical channels are required for a subsystem. Also to know how many more logical channels might optionally be assigned up to a normal useful subsystem maximum. 24 logical channels provided per IOM.

TABLE 4-3. IOM PHYSICAL AND LOGICAL CHANNELS/PATHS PER PERIPHERAL SUBSYSTEM

Peripheral Subsystem Device Processor	Physical Channel Type	Physical[a] Channels Required	Logical[b] Channels Required	Subsystem Total Useful Logical Channels
URP (Plus 1-7 Unit Record Devices)	PSI	1	1 per Device	Same
MSP/MSU0402/0451 (1x32) (2x16)	PSI	1 2	1 2	8
MSP/MSU0500	PSI	1 per MSP	1 per MSP	8
MTP (1x8) (2x16)	PSI	1 2	1 2	2 4
System Console CSU6004	Special	1	1	Same
Any FNP	Direct	1	1	Same

[a]Each device processor price includes one physical IOM channel.

[b]Don't forget that URP, MTP, and MSP allow for switched path feature to be added to each physical channel. *Each* termination must be allotted separate logical channel(s), of the same quantity for each termination.

F. Determining DRE (Date Rate Expansion) Requirements and Assignments

1. Use of DRE scratchpad storage feature

   a. One DRE feature is standard in each base IOM (i.e., the IOM included in base CPS system). The base IOM in a freestanding system can have one more DRE (MXF6002). Optional (freestanding) IOMs do not come with a DRE, but one must be ordered. A second can also be ordered for freestanding IOMs.

      Each DRE feature will be assigned by your FE to up to 16 logical channels, based on the assignments that you define. There are 24 logical channels per IOM.

   b. DRE scratchpad assignment must be used on the involved logical channels when:

      1) FNP is used.

      2) Disk spindles are used.

      3) Peripheral with transfer rate greater than 500KC/355K bytes is configured on a physical channel.

4) Combined data transfer rates of all I/O subsystems, planned to be in operation simultaneously on the IOM, exceed 1.3 million characters per second or 870 thousand bytes per second.

c. DRE assignment rules

1) Assign a DRE facility to each logical channel on a basis of transfer rates in descending speed. Each logical channel used for the subsystems below must have a DRE facility assigned to it, including logical channels used in switched non-simultaneous physical channel cases.

2) Assignment priorities for DRE facilities in descending order.

a) FNP

b) Disk (or tape if its transfer rate is higher)

c) Tape

d. DRE scratchpad assignment is recommended on the involved logical channels when:

1) 4 or more physical channels are to be used simultaneously for any disk and/or magnetic tape combination.

2) I/O channel traffic will be heavy. The DRE feature significantly cuts memory accesses by each logical channel assigned to it, by as much as 3 to 1. This frees memory cycles for use by processor or IOM.

e. When do you need more than one DRE?

1) Permitted only on freestanding IOM.

2) Determine your total logical channel assignments to physical channels using Table 4-3.

a) If the combined FNP, disk, and tape logical channel requirements exceed 16, order another MXF6002.

b) If you have unused scratchpad capacity left, assign it to other logical channels to the limit of 24 logical channels in the order of descending transfer rates of the peripherals.

Section V

Configuring Non-DPS Optional Processors, SCUs, and IOMs – Initially or as Upgrades

A. Non-DPS Processor and IOM Addressing Feature Rules

1. Prior to configuring your mainframe, draw a simple block diagram of the mainframe you want showing all modules and addressing features.

   a. Remember the simple rule that every processor and IOM must be ported (have an addressing feature) for every SCU. Processors and IOMs not included in base CPS system do not come equipped with addressing features. Base processor and base IOM come equipped with an addressing feature only for the base SCU.

   b. As you write down on your order the type numbers required based on the mainframe and model that you want, check off that component on the target mainframe you block-diagrammed in Step 1 above. You will save yourself problems from incorrect, incomplete, excessive ordering of type numbers.

   c. Check from your block diagram against the configurator in Figure 5-1. Remember that the base CPS system components have no individual type numbers. Every component added beyond the base CPS system has a specific type number which must be used on any order. In ordering optional processors the type number always starts with the "CPU" alphabetic prefix.

   d. Now use Section B below.

B. Steps for Configuring Non-DPS Optional Processors, IOMs, and SCUs

1. Use steps 2-5 below in sequence based on the configurator for adding optional main frame modules below. For optional configuring, where permitted, of processors beyond the base CPS processor, IOMs beyond the base CPS IOM, and SCUs (beyond the quantity required for the memory size, i.e., beyond the net base system), see Section I, Paragraph C,1. See also Section I, Paragraph D for summary of replication options.

2. Optional Processors – For each optional processor, order one CPA6002 (Central Processor Addressing feature or port) for each required SCU (net base system) in the configuration. If a processor is being added to an installed system, order a CPA6002 for each SCU in installed system.

   a. Find the appropriate type number for the additional processor (CPS6xxx) in the following table:

SYSTEM	CPS
68/60	CPU8600
68/80	CPU8800

   b. Configuring an optional processor involves only two type numbers, one for the appropriate processor and one for the processor addressing port feature(s).

c. The ability to configure optional processors is standard on all CPS models.

d. All optional processors are freestanding components.

e. Each freestanding processor, whether optional or included in base CPS number of freestanding systems, has its own power supply.

f. No ports for connection to SCUs are included in price of optional processors.

3. Non-DPS Level 68 Processor Upgrade Kits (see Table 5-1.)

TABLE 5-1. NON-DPS LEVEL 68 PROCESSOR UPGRADE KITS

MODEL	MKT IDENT	MEMORY SIZE	PERFORMANCE UPGRADE 68/60 TO 68/80
68/60	CPS8623	192K Words/768K Bytes	–
	CPS8624	256K Words/1024K Bytes	CPK6060
	CPS8626	384K Words/1536K Bytes	CPK6061
	CPS8628	512K Words/2048K Bytes	CPK6062
	CPS8632	768K Words/3072K Bytes	CPK6063
	CPS8636	1024K Words/4096K Bytes	CPK6064
ADDITIONAL PROCESSOR	CPU8600	–	CPK6065

4. Optional IOMs – For each optional IOM (MXU6001), order a quantity of MXA6001 (IOM addressing feature or port) for each required SCU (net base system) in the configuration. If an IOM is being added to an installed system, order a MXA6002 for each SCU in the installed system. Consult also Section IV for configuring rules within each IOM.

5. Optional SCUs – For each such SCU (MXC6001) beyond the quantity required (net base system) for the memory size, order as many CPA6001 Central Processor Addressing features as the total processors in the configuration, including any processors ordered in Step 2 above. Also order as many MXA6001 IOM addressing features as there are IOMs in the system, including any IOMs ordered under Step 4 above. Don't forget to count the IOM in any ICU included in the system.

   a. Configurating optional SCUs involves only three type numbers: one for the SCU itself, and one each for the processor and IOM addressing port features to connect the IOM and the processor to an extra SCU. An SCU must be ordered for each 512K words/2048K bytes of memory (net base system). In all models SCUs can be ordered optionally beyond the required number.

   b. All base and optional SCUs are freestanding components.

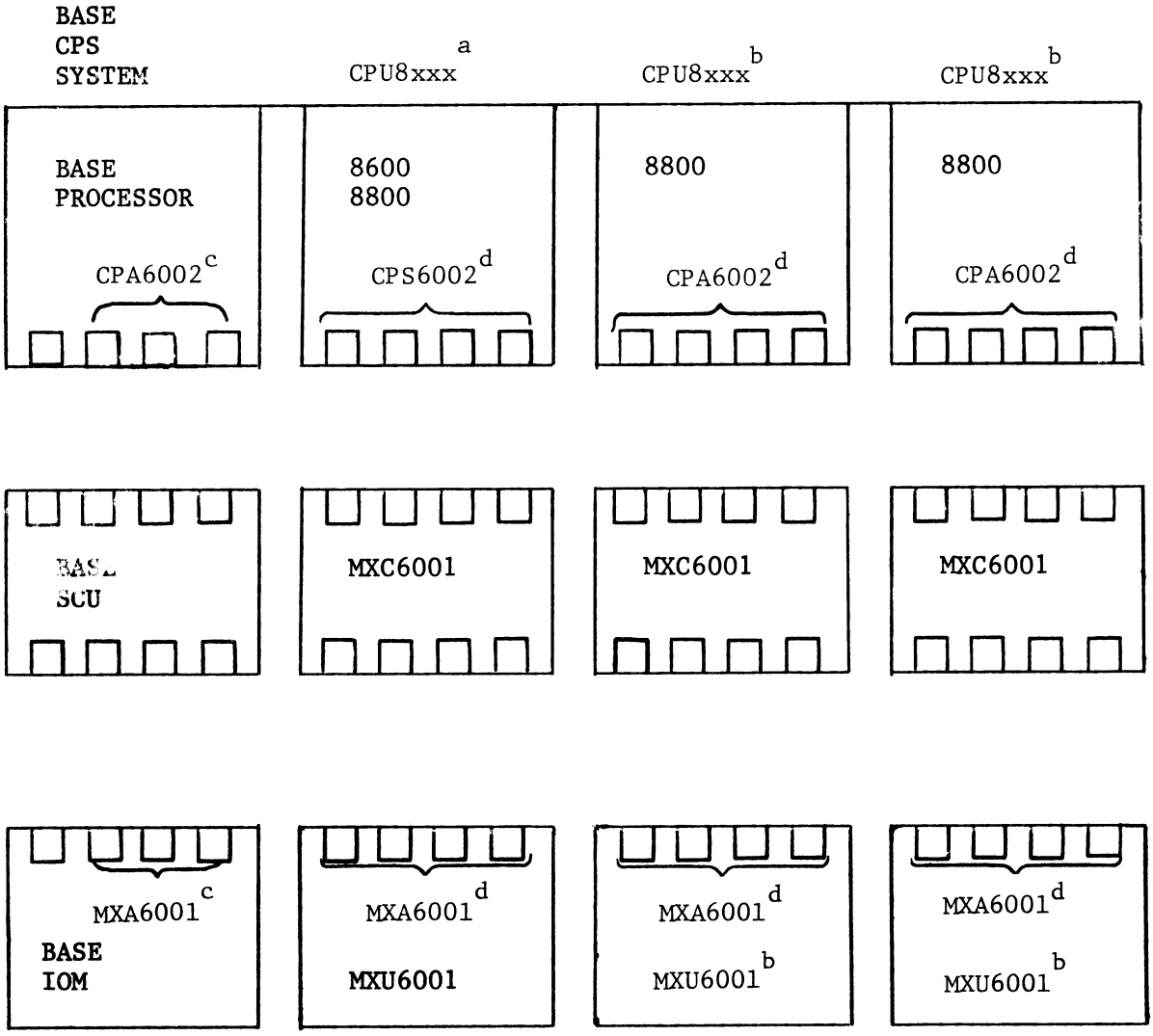
   c. All freestanding SCU cabinets can contain up to 512K words/2048K bytes of memory.

d. Each freestanding SCU, whether optional or required, has its own power supply. The power supply is also used for the memory contained in the SCU cabinet.

e. Each freestanding SCU provides up to 8 active module ports for connecting processors and IOMs. Processors and IOMs in turn must contain an addressing port feature for each SCU in system.

f. Maximum number of SCUs for any freestanding main frame is eight.

6. Configurator for Adding Optional Mainframe Modules – Non-DPS Systems (see Figure 5-1.)



[a]68/60 limited to one additional processor.

[b]Only 68/80 systems can have 3 or 4 processors and/or IOMs.

[c]One required for each SCU *beyond* base SCU.

[d]One required for *each* SCU in the system along with the extra processor (CPU8xxx) and/or extra IOM (MXU6001).

Figure 5-1. Additional Mainframe Modules

Section VI

Configuring Non-DPS Memory Additions/Upgrades

A. Steps for Memory Additions/Upgrades to Installed Non-DPS Systems

1. Refer to the Memory Upgrade Configurator (MUC) charts (Tables 6-1 and 6-2) on following pages. The MUCs relate only to upgrading (increasing) the amount of memory on an installed system. MUC data is based on a system with one processor and one IOM.

2. In the appropriate MUC, find the Level 68 model to which you are adding more memory. Begin with the square that represents the first add-on quantity of memory and read straight across through as many squares as necessary to give you the new total memory size you want. Use all the type numbers (marketing identifiers) in each square required for the total new memory size. For example, to increase a 68/60 from 192K Words/768K Bytes to 384K Words/1236K Bytes, order the hardware listed in the square for the 192K Words to 256K Words column plus the square for the 256 to 384K Words column.

3. When your memory upgrade or add-on crosses a 512K Words/2048K Bytes boundary on the MUC (marked by the triangle at the top), you must also configure an SCU, plus CPA6002 and MXA6001 to link the SCU to the base processor and base IOM in the installed system. However, your installed system may already have at least the required number of SCUs (via use of optional SCUs) for the total memory size to which your system is being upgraded. If so, disregard the MXC6001/CPA6002/MXA6001 combination.

4. For each additional processor already installed beyond the base processor, order another CPA6002 (for any SCU that you are ordering because of Step 3 above). For each additional IOM already installed beyond the base IOM, order another MXA6001 (for any SCU that you are ordering because of Step 3 above).

B. Non-DPS Memory Upgrade Configurator

1. Part 1 (See Table 6-1.)

TABLE 6-1. MODEL 68/60 BASE MAINFRAME

MODEL	CENTRAL SYSTEMS IDENT.	BASIC MEMORY SIZE	MEMORY UPGRADE KITS FOR INSTALLED SYSTEM[a]				
			192 – 256K Words	256 – 384K Words	384 – 512K Words	512 – 768K Words	768 – 1024K Words
68/60	CPS8623	192K Words 768K Bytes	CMK6035	CMK6036	CMK6037	CMK6038	CMK6039
↓	CPS8624	256K Words 1024K Bytes		CMK6036	↓	↓	↓
↓	CPS8626	384K Words 1536K Bytes			CMK6037	↓	↓
↓	CPS8628	512K Words 2048K Bytes				CMK6038	↓
↓	CPS8630	768K Words 3072K Bytes					CMK6039
↓	CPS8636	1024K Words 4096K Bytes					

[a]Memory upgrade kits contain all necessary memory addressing and SCUs if required.

Procedure:

1. Select the CPS number that provides the correct memory size desired.

2. If the system is installed and you wish to upgrade the memory size use the CMK kits at right of appropriate CPS number.

NOTE:
K in memory size indicates a value of 1024. Maximum memory in system is 1024K Words/4096K Bytes whether two processors are used or not. Maximum is 512K Words per SCU.

2. Part 2 (See Table 6-2.)

TABLE 6-2. MODEL 68/80 BASE MAINFRAME

Model	Central System Ident.	Basic Memory Size	Memory Upgrade Kits for Installed System[a]					
			256 – 384K Words	384 – 512K Words	512 – 768K Words	768 – 1024K Words	1024 – 1536K Words	1536 – 2048K Words
68/80	CPS8824	256K Words/ 1024K Bytes	CMK6040	CMK6041	CMK6042	CMK6043	CMK6044	CMK6045
↓	CPS8826	384K Words/ 1536K Bytes		CMK6041	↓	↓	↓	↓
↓	CPS8828	512K Words/ 2048K Bytes			CMK6042	↓	↓	↓
↓	CPS8832	768K Words/ 3072K Bytes				CMK6043	↓	↓
↓	CPS8836	1024K Words/ 4096K Bytes					CMK6044	↓
↓	CPS8844	1536K Words/ 6144K Bytes						CMK6045
↓	CPS8856	2048K Words/ 8192K Bytes						

[a]Memory upgrade kits contain all necessary memory addressing and SCUs if required.

Procedure:

1. Select the CPS number that provides the correct memory size desired.

2. If the system is installed and you wish to upgrade the memory size use the CMK kits at right of appropriate CPS number.

NOTE:
K in memory size indicates a value of 1024. Maximum memory in system is 2048K Words/8192K Bytes whether two processors or not. Maximum is 512K Words per SCU.

Section VII
Mainframe Configuration Examples

A. Initial Mainframe Order Examples

1. Customer wants a Level 68/DPS-2 system with 1.5 M words/6 M bytes of memory.

Quantity	Marketing Identifier	Description
1	CPS8802	Base Mainframe with 612 K words/2048 K bytes memory
1	CPK8004	DPS-1 to DPS-2 kit
1	CMA6013	Memory Addressing; 512-768 K words
1	CMA6014	Memory Addressing; 768-1024 K words
1	CMA6015	Memory Addressing; 1024-1536 K words
1	MXC6004	2nd SCU with all Processor and IOM Addressing features (Ports)
1	CMM6013	Memory Module; 512-768 K words
1	CMM6014	Memory Module; 768-1024 K words
1	CMM6015	Memory Module; 1024-1536 K words

2. Customer wants a 3 processor Level 68/DPS with 2 IOMs and 2M words/ 8 M bytes of memory.

Same configuration as in 1 above with the following additions.

Quantity	Marketing Identifier	Description
1	CPK8008	DPS-2 to DPS-3 Upgrade Kit
1	CMA6016	Memory Addressing; 1536-2048 K words
1	CMM6016	Memory Module; 1536-2048 K words
1	MXU6002	IOM with 35 Channel Function Slots (Includes one SCU port and one IOM port)
1	MXF6002	IOM Data Rate Expansion

B. Additions to Mainframe Orders

1. Customer has a Model 68/60 with 384 K words/1536 K bytes of memory and wants to upgrade to Level 68/80 with 768 K words/3072 K bytes of memory with 2 processors and 2 IOMs.

Additional Quantity	Marketing Identifier	Description
1	CPK6061	System Upgrade: 68/60 (CPS8626) to 68/80 performance
1	CMK6041[1]	Memory Expansion: 384-512 K words
1	CMK6042[1]	Memory Expansion: 512-768 K words
1	CPU8800	Additional Processor
2	CPA6002	Central Processor Addressing feature or port (One per SCU)
1	MXU6001	2nd IOM with 35 channel board slots
2	MXA6001	IOM Addressing (one per SCU)
1	MXF6002	IOM Data Rate Expansion

[1] All memory expansion kits include all necessary memory addressing and SCU functions.

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