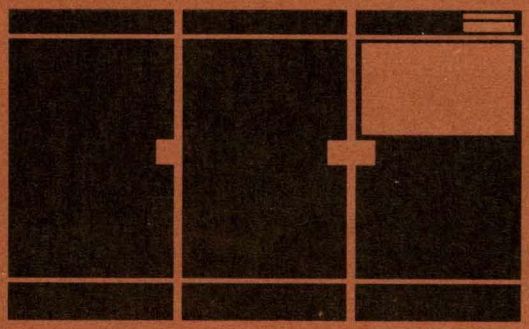
GENERAL ELECTRIC
COMPUTERS

DATANET-30
Systems Manual



GENERAL ELECTRIC

CPB-289A

DATANET-30
SYSTEMS MANUAL

July 1963
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GENERAL ELECTRIC
COMPUTER DEPARTMENT

PREFACE

DATANET is a General Electric registered trademark and is applied to GE products or systems using public or privately-owned transmission facilities to permit the processing of information at a point remote from its orgin. The DATANET-30 is a 128 channel data communications processor which enables remote terminal facilities to communicate with other remote terminal facilities, or a central information processing system.

This manual provides general information on DATANET-30 system configurations and on DATANET-30 hardware, but will not include information on transmission lines, digital subsets, remote terminal devices or other products included within a total communications complex.

Comments on this publication may be addressed to Technical Publications, Computer Department, General Electric Company, P. O. Box 2961, Phoenix, Arizona, 85002.

CONTENTS

ILLUSTRATIONS

INTRODUCTION

With the trend toward more decentralization of company operations over a wider geographic area, with more products to sell to more customers, there is also the trend to centralize management of company operations. In order to make the right decision at the right time--of what to build, what materials to buy, how much of an item to ship to an area warehouse, what type of an inventory to maintain and the many other involved problems of a far flung modern business--the managers who make these decisions must have accurate data that represents the situation at the moment--today--not last week.

For effective control, management requires timely and accurate information which reflects the decisions on the total business environment. For example, better customer service, with shorter lead time on orders received and faster answers to inquiries is often the determining factor in where an order is placed.

The requirements for this unified systems approach to management and customer service take on added significance when one considers the size of the communications problem in business operations. The continued growth of business, increased specialization, and decentralization have created many barriers to the flow of information. Undoubtedly the most formidable communications problem is the sheer volume of information to be handled.

Concurrent with the need for timely and reliable information, another requirement developed. The trend toward decentralization created the need for data processing at district locations which, in many cases, is not economically justified. Hence, management must rely on a centrally located computer to handle the processing load for each district--a practice which again poses a problem in communications.

The development of computer-based data communications networks has progressed to the point where it is economically feasible to transmit data over public carrier facilities. New services and reduced rates are offered for transmission of digital data. In order to take advantage of these developments, and at the same time satisfy many needs in business communications, General Electric developed the DATANET-30.

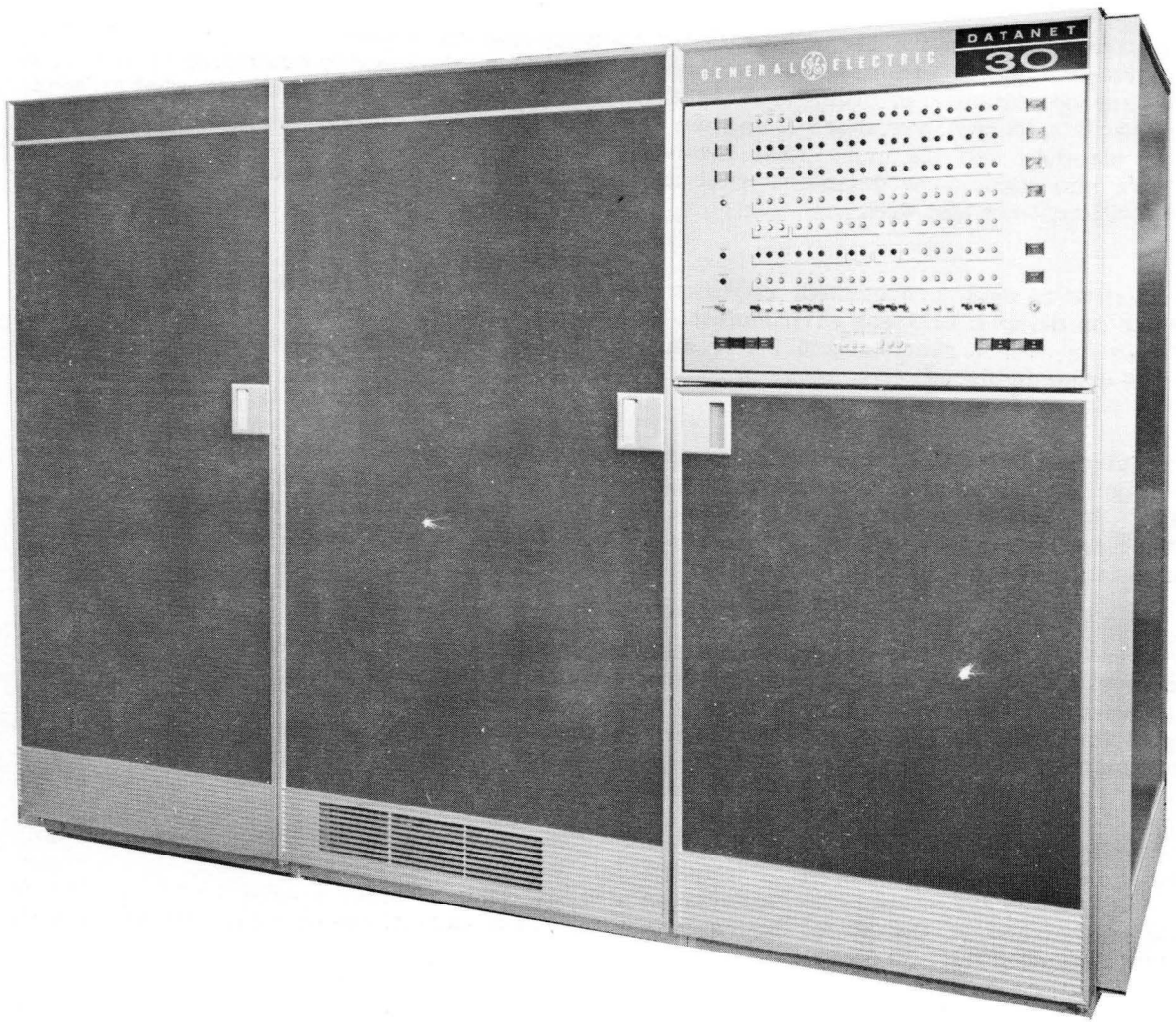


Figure 1. DATANET-30 Processor

1. GENERAL SYSTEMS DESCRIPTION

The DATANET-30 is a real-time computer--designed primarily to automatically receive and process information originated at locations remote from the central computer (remote terminals)--and to automatically transmit information to the remote terminals over normal common carrier communication facilities.

The DATANET-30 is:

- High speed
- Solid state
- Single address
- Special purpose
- Communications oriented
- Digital computer

has:

- A binary mode of operation
- A 7 microsecond word time
- A stored program
- A magnetic core memory
- Over 78 basic instructions
- 18-bit word in memory
- Up to 128 input/output channels
- Memory interrupt
- Indirect addressing and multiple indexing
- An elapsed time counter
- Patch plug adaptability to character and word length
- Patch plug adaptability to transmission and receiving speeds

performs:

- As central control for a DATANET-30 communication system
- As a communications controller for a GE-200, 400 or 600 Series General Purpose Computer
- Arithmetic and data manipulation operations
- On a real time basis

capable of:

- Controlled transmission of data over common carrier facilities
- Serving as a communications control between remote terminals and a computer
- Unattended operation
- Using a variety of remote terminal devices including Teletype keyboard printers, a computeral DATANET-760 Terminal
- Simultaneous transmission to remote terminals

- Simultaneous receiving from remote terminals
- Receiving and transmitting digital data over Teletype or telephone grade transmission lines--private or leased--or public dial-up services, manual and automatic
- Operating with 5, 6, 7, 8, level codes, and other codes up to 20 bits
- Operating at standard transmission/receive speeds (in bits per second) of 45; 50; 56.25; 66.2; 72.6; 75; 110; 150; 300; 600; 800; 1050; 1200; 1800; 2000 and 2400
- Storing and retrieving data on a disc storage unit
- Storing and retrieving data on magnetic tape compatible with a computer
- Printing reports on a high speed printer or Teletype machine

performs the functions of:

- Message assembly
- Message formatting
- Message disassembly
- Message scheduling
- Multiple message broadcast
- Store and forward communication
- Communications network control
- Control of switched network lines
- Message accounting and traffic analysis
- Producing traffic statistics
- Basic message routing and switching
- Handling priority messages
- Handling variable message lengths
- Maintaining a high line loading
- Journal keeping
- Alternate routing on a station or center basis
- Inserting time and date
- Message acknowledgment
- Control of multipoint private lines
- Code conversion
- Speed conversion
- Format control and conversion
- Providing cost allocation on message or station basis
- Error control--operator and code
- Character and word parity checking
- Automatic program reload
- "End of Transmission" and "End of Text" code detection under program control

The capability to receive the transmission of data from remote terminals allows a DATANET-30 system to perform as a:

- Message switching center where messages and data are going from one remote terminal to another
- Remote data processing where data from remote stations is processed at a central computer, and as needed, reports are sent to remote stations. The DATANET-30 can be programmed to handle data traffic for a data processing center with equal facility that it handles the administrative traffic normally associated with telegraph switching centers
- Remote inquiry where an answer is generated by the computer and transmitted to the station requesting
- Automatic data accumulation and distribution to/from a variety of points for batch processing by a computer
- File updating where reports from remote stations are processed by a central computer on a batch process basis

A DATANET-30 system consists of a variety of equipment, the choice of which depends upon system design and requirements. The following illustrations cover some of the combinations possible with a DATANET-30 to fill the communication requirements of modern business activities.

TELETYPE MESSAGE SWITCHING SYSTEM

The General Electric DATANET-30 switching center is a fully-automatic system designed to perform, store and forward message switching. The DATANET-30 switching center can be used to communicate with any of the following:

1. Direct-connected communication stations,
2. Multipoint private line connected stations,
3. Dial-up stations on public message networks,
4. Direct input/output with computer systems (core to core),
5. Indirect input/output with computer systems (via magnetic tape or a disc storage unit),
6. Communication with other networks or portions of a network.

Functions

All the functions of transmitting to or receiving messages (data) from a remote terminal, and handling the messages enroute from origin to destination must be coordinated within the message switching system. This coordination is accomplished by providing means for the functions of:

1. Message Accumulation--Messages are assembled and routed under program control.

2. Message Distribution--Messages are distributed under program control.

3. Automatic Multipoint Private Line Control (Party Line)--Polling and selection of stations on the line is accomplished under program control.

4. In-Transit Storage--Storage is provided for message queueing.

5. Journal Storage--Storage is provided for recording message journals.

6. Intercept Storage--Storage is provided for messages for stations closed due to limited time of operation, station malfunction, etc.

7. Message Accounting--Journal storage can be processed during off hours or low activity periods to provide daily status reports, and data for network study.

8. Traffic Analysis--The number of messages per line per station per day can be counted. The reports generated can then by typed out at the supervisory position. Such items as average message length, number of multiple message broadcasts, and operator errors in formatting may be included in the reports.

9. Multiple Message Broadcast--Individual messages can be routed to more than one outstation as designated by the routing indicators.

10. Automatic Restart--System is capable of automatically restarting itself in case of program malfunction.

11. Supervisory System Monitoring--One Automatic Send-Receive (ASR) and a Receive Only (RO) Teletype device are used for system monitoring. Headers of misrouted messages

can be printed out and corrected. The supervisor can send service messages to open or close out stations and/or to send data to intercept storage.

12. Format Conversion--Changing the order of spacing of data from the incoming order to the desired outgoing order.

13. Error Control--A variety of error detection and correction schemes can be used. Operator error codes can be recognized and a recovery or re-start procedure set up for that message. The DATANET-30 can be programmed to control the format of a message and notify the operator of any format errors. Also, transmission errors can be recognized through echoplex retransmission. Parity check of codes and block parity checks can be used.

14. Alternate Routing of Messages--Supervisory changes in routing on a temporary basis in case of line or terminal outage. Programmed automatic alternate routing is also possible.

15. Priority Messages--Messages may contain a "Priority Level Code" that can be recognized by the DATANET-30 program. Thus hot messages or data can be handled before routine administrative messages.

Operation

The operation of the switching center is fully automatic--under control of the program. The sequence of transmission of terminals on a multipoint private line is also controlled by the program. Each message contains a destination code--the name or number of the remote station or stations where the message is going. After a message is received from a remote station, the program interrogates the destination code of the message in memory, then transmits it to the proper remote terminals. The DATANET-30 is programmed to handle all normal messages in accordance with a standard format and standard routing codes for the system. A standard incoming message format would be used for all incoming traffic, including rush messages, normal messages, and service or control messages. The distinction between messages is made by the mnemonic address code.

The system is capable of operation with only occasional manual intervention and control. The control is accomplished through the supervisory terminal to open and close stations by time of day and enter other control messages. When a station is closed, the program forwards all messages for the closed station to intercept storage.

The supervisory terminal normally consists of a keyboard/printer Teletype unit. This terminal is used as a message intercept position for incorrectly routed or formatted messages. The supervisor looks at the messages and decides what action is necessary, such as, correct the heading and re-enter the message, ask for retransmission, etc. The terminal is also used to notify the supervisor of line malfunctions and for printing out periodic status reports on the switching center operation.

The detailed operation of each system will be developed according to individual system requirements, such as; routing, service and control codes, format, number of lines and remote terminals, and the many other overall system operational requirements.

SWITCHING CENTER SIZE

The number of communication lines to be connected to the DATANET-30 permits a broad definition for the size of a switching center and associated equipment. A switching center can be defined as small, medium or large.

Small Switching Center

A small switching center would have an RDC 930 Removable Disc Unit and up to 10 communication lines of half duplex or full duplex operation. The amount of traffic is assumed to be in the range of 1 million characters per day throughput. The RDC 930 Removable Disc Unit is especially adaptable to this size system.

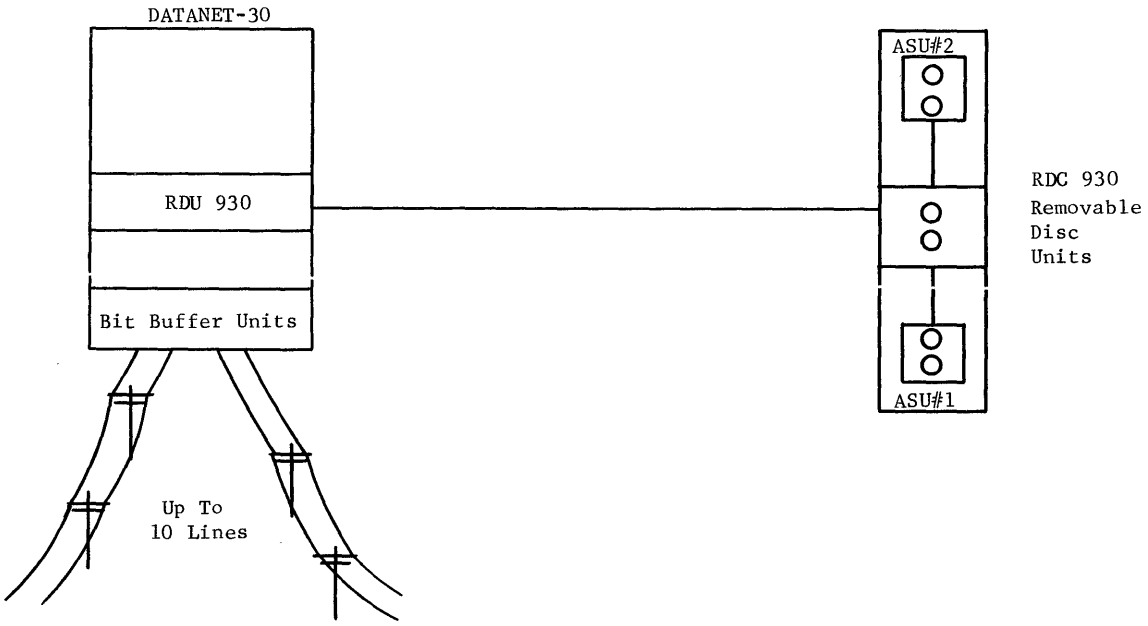


Figure 2. System with RDC 930 Units

Medium Switching Center

The medium switching center would have an M225B Disc Storage Unit and up to 30 communication lines of half duplex or full duplex operation. The amount of traffic is assumed to be in the range of 4 million characters per day throughput. The M225B Disc Storage Unit provides the capacity to operate this size system efficiently.

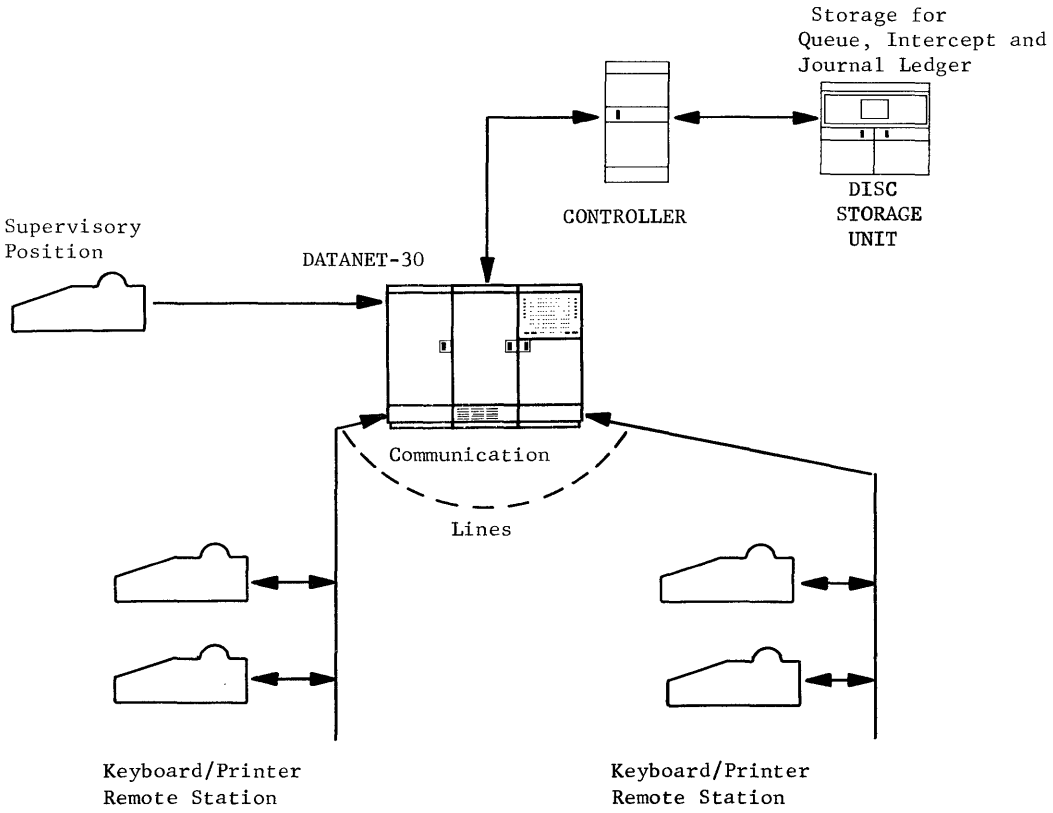


Figure 3. Medium Switching Center

Large Switching Center

The large switching center would have more than one DATANET-30, one or more M225BX Disc Storage Units with Dual Access Controllers, and more than 30 communication lines. The communication lines would be of half duplex or full duplex operation with up to ten stations per line, or private line. The amount of traffic is assumed to exceed 10 million characters per day throughput.

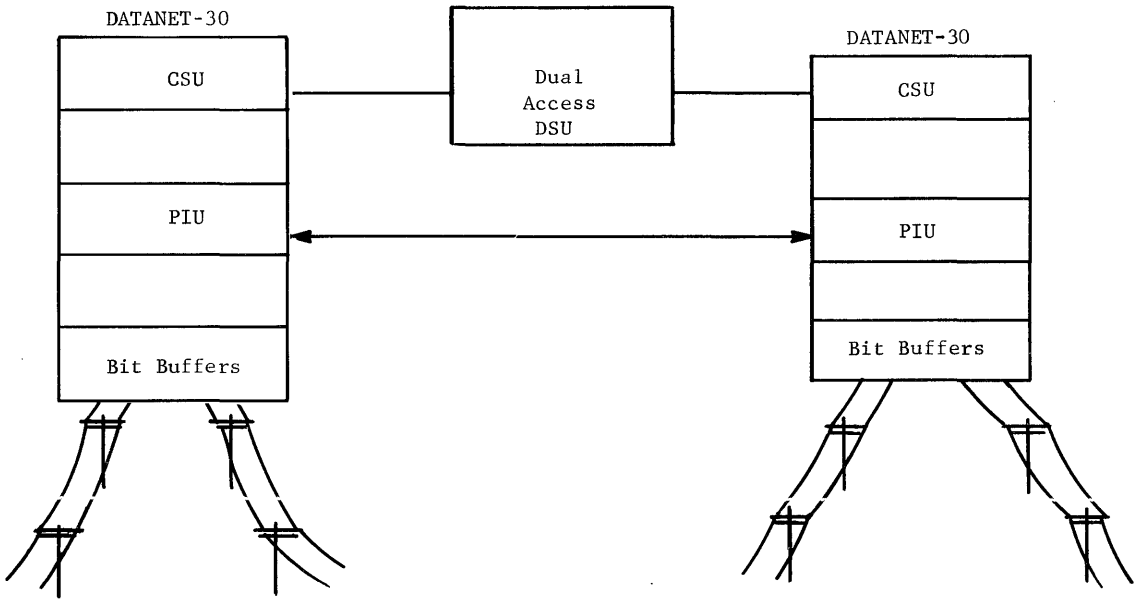


Figure 4. Large Switching Center

DATANET-30 AS A REMOTE CONCENTRATOR

When many remote stations are located many miles from the DATANET-30 switching center, it may be desirable to include one or more DATANET-30's to act as a concentrator for the more distant remote terminals. This will reduce the number of long distant lines coming into the switching center.

The remote concentrator is connected to the switching center via a "high speed" voice-quality trunk line. The DATANET-30 can "pack" many messages received at slow speed (75-110 bps) and transmit them. There are two main advantages:

1. Where the switching center would be overloaded if all remote terminals were directly connected, the use of the remote concentrator will reduce the time delay in a message from its origin to its destination. This is especially so if the remote stations were connected by multipoint private lines since it would then be possible to connect them via single lines on the remote concentrator.

2. Reduction in transmission line costs. If all remote stations were directly connected, there would be many "parallel" telegraph lines; whereas with the remote concentrator, there is one voice line.

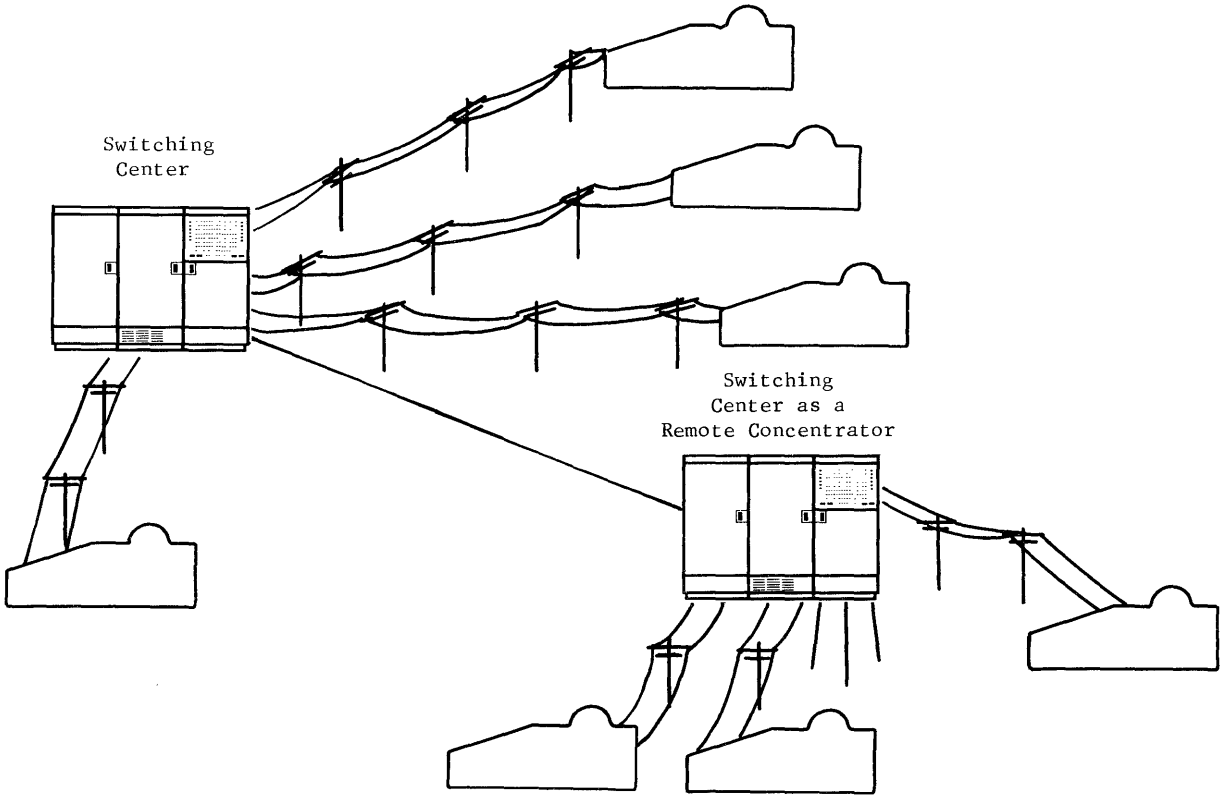


Figure 5. Communication Lines with a Remote Concentrator

Functions

As a remote concentrator, the DATANET-30 takes traffic from low volume areas with low speed terminal devices and depending upon the program, performs the following functions:

1. Message accumulation and distribution
2. Code conversion
3. Speed conversion
4. Multiprivate line control
5. Error control
6. In-transit storage
7. Unattended operation

Operation

The messages are accumulated from many remote terminals and held in the in-transit storage until they can be transmitted at higher speed over a trunk line to a DATANET-30 switching center. When messages are received by a DATANET-30 remote concentrator from another DATANET-30, speed and code conversion are accomplished and the messages are transmitted out to the lower speed terminal devices. Hence, an increase in line utilization is obtained between two DATANET-30 centers and the low speed remote terminals. Traffic can be handled two ways:

The concentrator can act as a store and forward switching center between those remote terminals connected into the concentrator.

The concentrator can be operating in the capacity of a relay station with the message switching being done by a DATANET-30 functioning as a switching center. All messages would go one way to the switching center and then back to the concentrator for transmission to one of the remote stations.

THE NETWORK

The DATANET-30 can be built up to a network configuration by interconnecting several DATANET-30 switching centers with high speed lines.

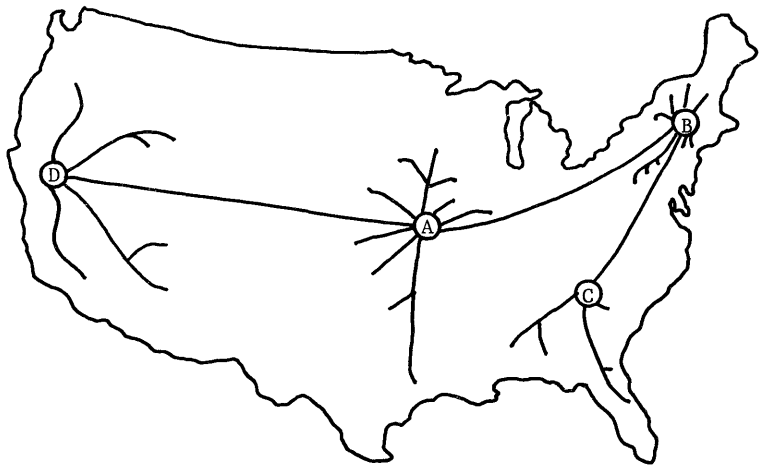


Figure 6. Nationwide Network

Functions

Each DATANET-30 would perform as a local switching center as well as a forwarding center for messages routed to a destination via one of the other DATANET-30 centers. Automatic alternate routing is also accomplished in the event that the line between any two centers should become inoperable or busy for long periods of time. Data processing could be associated with one of the DATANET-30 centers. Networks of this configuration require a comprehensive traffic analysis to insure that the capacity of the network is not exceeded.

Operation

An operator at a remote station on one DATANET-30 wishes to send a message to a remote station on another DATANET-30 of the network. The first DATANET-30 receives the message from the remote station, examines the destination code and determines that the message must be forwarded to another DATANET-30. When the trunk line is free, the message is forwarded to the other DATANET-30 where the destination code is examined and the message forwarded to the intended remote terminal. With proper coding of destination codes, messages may be simultaneously routed to several remote stations (multiple message broadcast).

COMMUNICATION/DATA PROCESSING SYSTEMS

In a direct access computer system, where remote terminals are capable of exchanging information with a central computer (EDP center) via data communication channels, the definition of the system depends on the job to be done. An individual system would be tailored to the requirement of the operating environment. The equipment variations are discussed later.

The list here is a generalized approach to system concepts:

Remote inquiry in real time
Remote file updating in real time
Remote file updating by batch processing
Remote data collection by batch processing
Remote data processing in real time
Computer-to-computer communication
Time sharing in real time

Remote Inquiry

Remote inquiry in real time can be defined as providing a reply to a remote terminal while the remote terminal is still on the line.

Remote File Updating

Remote file updating in real time is similar to remote inquiry except that the input is data to be used immediately to update existing records. The reply to the remote terminal supplying the data would be an acknowledgment or report of action taken.

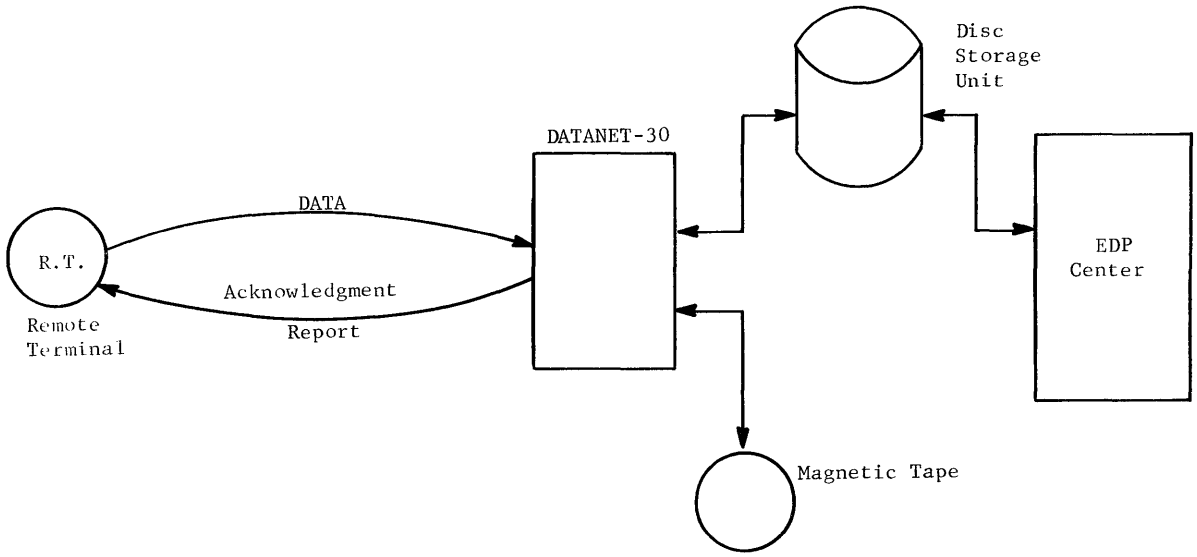


Figure 7. Remote File Updating

Remote file updating on a batch processing basis varies in the procedures used to update existing records. In this case, it may be more desirable to store the data on magnetic tape to process the data on a regular basis.

Data Collection

Data collection can be similar to remote file updating on both a real time and batch process basis. The data is collected on a real time basis and stored for later batch processing.

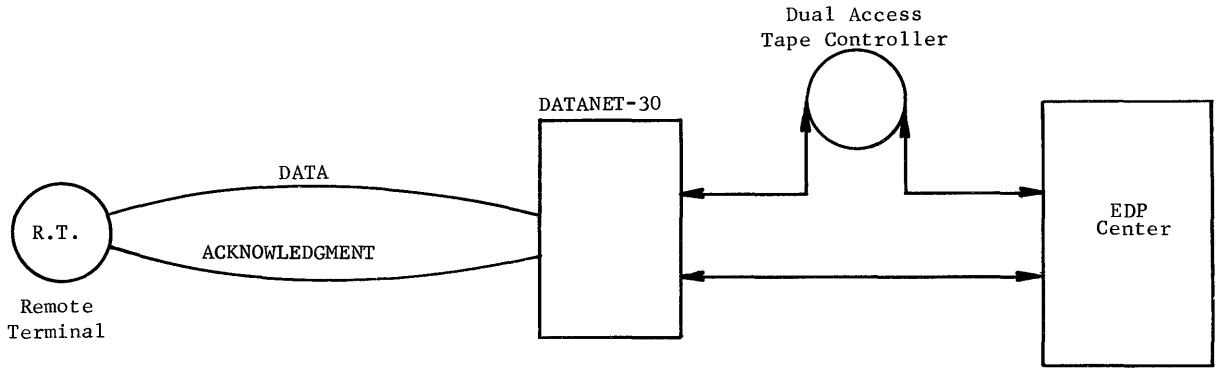


Figure 8. Data Collection

Remote Data Processing

Remote data processing in real time places additional requirements on system design and programming. The remote terminal requires direct access to the EDP center and waits for an answer.

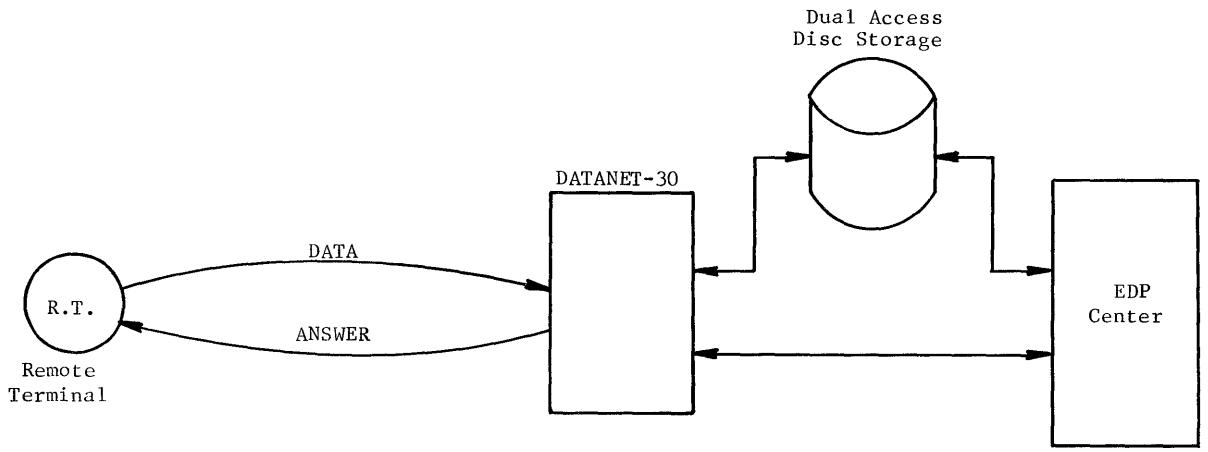


Figure 9. Remote Data Processing

Time Sharing

A GE-265 Time-Sharing System is a combination of a DATANET-30 communications processor, a GE-235 computer for high-speed scientific/data processing, and a proven software package with an easy-to-use language. A GE-265 System provides desk-side computations on an immediate and simultaneous basis. Remote terminals, such as Teletypes, access the system and provide computer access from any office where telephone service is available.

More information on the General Electric Time-Sharing System is available in various manuals covering operation and programming.

EQUIPMENT CONFIGURATIONS

Many factors are involved in deciding upon a system equipment configuration. The scope of this manual does not allow a full discussion of the various combinations. Therefore, equipment available for the design of a real time, direct access communication/data processing system is described from a functional viewpoint. Incorporation of the individual pieces into an operating system must necessarily be done on an individual basis.

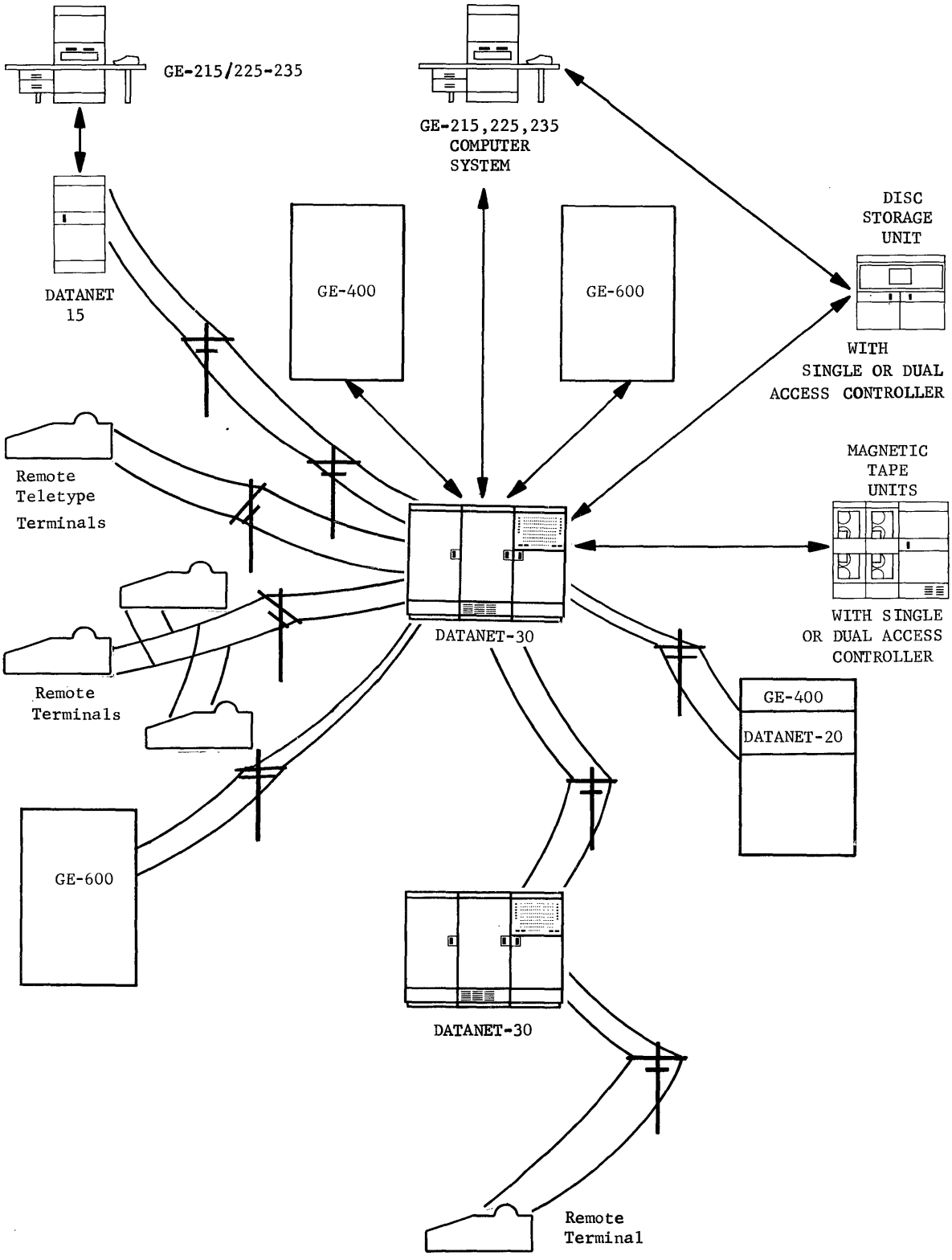


Figure 10. DATANET-30 System Components-Not a Typical System

2. DATANET-30 COMPONENTS

GENERAL DESCRIPTION

The DATANET-30 consists of:

The data communications processor, to control the input/output flow of data, and manipulate the data as necessary.

Buffers to connect the communication facilities to the communications processor.

Buffers to interconnect computers.

Buffers to connect computer peripheral equipment to the communications processor.

Data Communications Processor

The communications processor contains a core memory, power supply, control and working registers, and the buffer selector.

The magnetic core memory stores program instructions, alphanumeric information, and binary data. Standard memory units are available in sizes of 4,096, 8,192 and 16,384 words. Each word consists of 18 bits. The memory cycle time is 6.94 microseconds for a read-restore cycle, a clear-write cycle, or a read-compute-write cycle.

During a read-restore cycle, 18 bits of information are read from the memory and transferred to the working registers.

During a clear-write cycle, 18 bits of information are transferred from the working registers and written into memory.

During a read-compute-write cycle, 18 bits of information are read from memory, modified, and the new information is written back into memory.

The control and working registers include: An arithmetic unit capable of an 18-bit binary add; and logic for data manipulation.

Buffer Selector

The buffer selector is an important functional element of the DATANET-30. Low speed information flow between the communications processor and external equipment is through buffers connected to the buffer selector. All units directly connected to the buffer selector will be referred to as "buffers." The buffer selector contains one hundred twenty eight (128) channels numbered 0 to 127.

Channel Address

Each buffer occupies one channel address of the buffer selector whether it is for a simplex, half duplex, full duplex, or any other type of transmission facility. The desired buffer selector address of a channel is easily established by wiring a channel address plug. The address can be changed or new addresses (buffers) added by changing the plug wiring or inserting a different plug. The channel addresses in any given group of buffers need not be sequential. Channel 0 is always reserved for the paper tape reader.

DATANET-30 BUFFER MODULES

The DATANET-30 has physical space for 12 buffer modules. The buffer modules vary according to size of buffer storage and purpose. Depending upon the system, the twelve modules will contain the desired configuration of:

A. Communication Line Buffers
   - Bit Buffer Unit (BBU) Module
   - Character/Word Unit (CWU) Module
   - Dialing Adapter Unit (DAU) Module
   - Telpak A Buffer Module

B. Interconnecting Computer Buffers
   - Computer Interface Unit (CIU) Modules
   - Processor Interrupt Unit (PIU) Modules

C. Peripheral Equipment Buffers
   - Controller Selector Unit (CSU) Modules
   - Common Peripheral Channel (CPC) Modules
   - Removable Disc Unit (RDU) Module
   - Card Read Unit (CRU) Module
   - Punch Reader Unit (PRU) Modules

Other System Components

These components do not occupy space in the DATANET-30. They are connected externally to peripheral equipment and communication lines.

1. Parallel Channel Adapter
2. Manual Peripheral Switch
3. Programmed Peripheral Switch
4. Voltage Current Adapters
5. Digital Subsets
6. Communication Lines

DATANET-30 to DATANET-30

When one DATANET-30 is used as backup for another DATANET-30, or when it is otherwise necessary for one DATANET-30 to communicate with another, the following equipment is available:

Local
- Processor Interrupt Unit
- Dual Access DSU Controller
- Dual Access Tape Controller

Remote
- Word Buffer Unit
- Telpak A Buffer

DATANET-30 Peripheral Equipment

Once the real time data is captured from the communication line by the DATANET-30, the data must be stored or otherwise processed depending upon the system design. In order for the DATANET-30 to handle the additional optional requirements of a real time, direct access/data communications system, the following equipment is available:

- Controlled Selector Unit (CSU 931)
- Computer Interface Unit (CIU 930/931)
- Common Peripheral Channel (CPC 930)
- Card Read Unit (CRF 930)
- Punch Reader Unit (PRF 930)
- RDC 930 Removable Disc Unit

EDP Center

The EDP center can be any one of the three General Electric computer families. In order for the DATANET-30 to communicate with the EDP center, the following equipment is available:

- Computer Interface Unit CIU 930/931
- Common Peripheral Channel CPC 930
- Dual Access DSU Controller (GE-200 Series Computer)
- Dual Access Tape Controller (GE-200 Series Computer)

COMMUNICATION LINE BUFFERS

The Bit Buffer Unit Module

The bit buffer unit contains from one to ten buffer channels and one control section for that module. The control section contains a basic timing unit and common circuitry. The buffer control section contains hardware that is common to all the bit buffer channels in the unit module. Each bit buffer channel is capable of receiving and transmitting digital data. A bit buffer unit module may terminate from one to ten full duplex, half duplex, or simplex transmission lines which are all operating at the same bit rate.

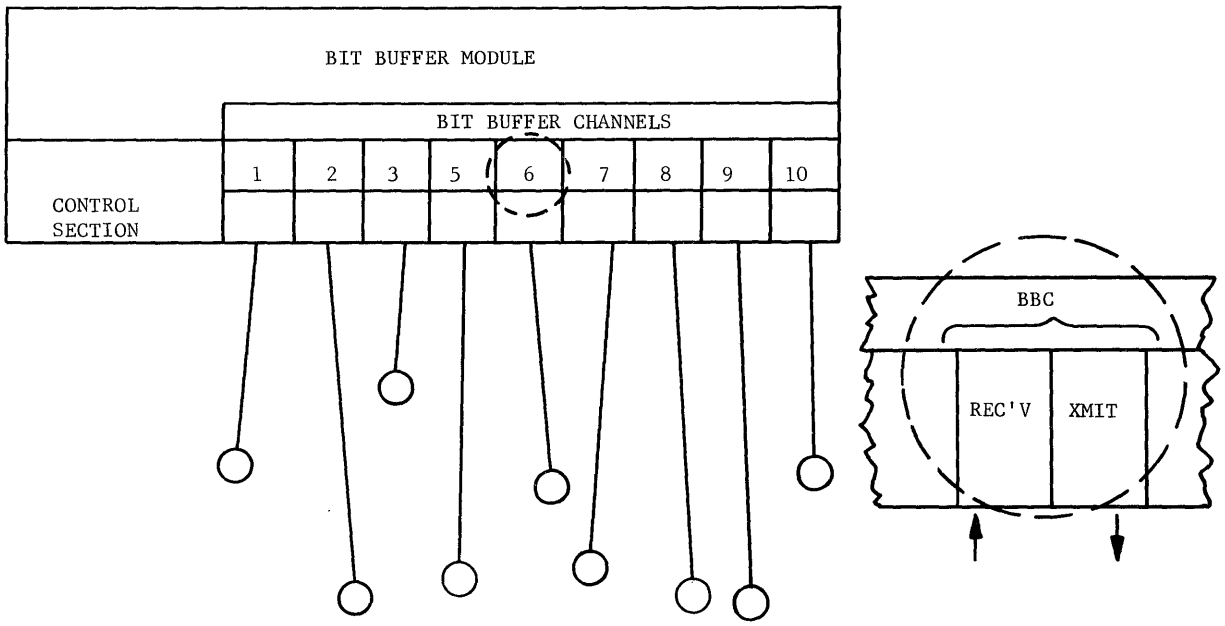


Figure 11. Bit Buffer Module

THE BIT BUFFER CHANNEL The Bit Buffer Channel (BBC) buffers one bit of information at a time between the DATANET-30 and the communication line. It is used on communication lines operating with stop-start asynchronous format (e.g., normal Teletype) and either 5, 6, 7 or 8 level codes.

Each bit buffer channel in a module is assigned a buffer selector address by the address plug for that module. The address applies to both the receive and the transmit section. The address for the bit buffers in a module can be whatever is desired for the system and they need not be sequential. Thus a bit buffer channel may be added to a module and given an address without disturbing the existing address arrangement.

System considerations limit operating speed of the bit buffer lines to the standard Teletype rates of 45, 50, 56.25, 66.2, 72.6, 75, 110, and 150 bits per second. The rate is established per module with a timing connector plug. The selected bit rate will apply to all the bit buffer channels physically located in a module. If more than one bit rate is used in a system, the different bit rate lines would be terminated in separate bit buffer unit modules using a timing connector plug set for the bit rate of that module.

The maximum number of lines which can operate simultaneously is dependent on the bit rate in use in the system, the volume of traffic and other factors. The slower the transmission rate, the higher is the number of remote stations that can be handled simultaneously.

More than one code level may be used within a bit buffer unit module. The program recognizes different code levels in use in the same system.

Receive Operation. The following is a brief description of the operation of the receive section of a bit buffer channel. Assume that the terminal device is sending marks, i.e., it is idle. Now the terminal device starts to send a bit stream (e.g., a character). When the start bit (a space) is received, a clock is started. The clock is used to time the future sampling of the line. The start bit is transferred into the receive data buffer and a receive flag is set. When the clock reaches the proper time, the line is sampled again, the bit on the line is transferred to the receive data buffer, and the receive flag is set. This process of sampling the line at regular intervals, transferring the data on the line to the receive data buffer, and setting the receive flag continues until the clock is stopped by the program. Since the bit buffer channel will transfer the information from the line into the receive data buffer every bit time, the program must test the receive flag and take away the bit in the receive data buffer before the line is sampled again. Whenever the bit is taken, the receive flag and the receive data buffer are automatically reset. At some point, the program decides that the appropriate number of bits have been received and sends a signal to the bit buffer channel which stops the clock. The receive flag will remain reset until another start bit is received. As a protection against noise on the transmission line causing the clock to start running, the bit buffer circuitry requires the space condition to exist on the line for at least one-half of a bit time to start the clock. Thus, noise of less duration than one-half of a bit time will have no effect.

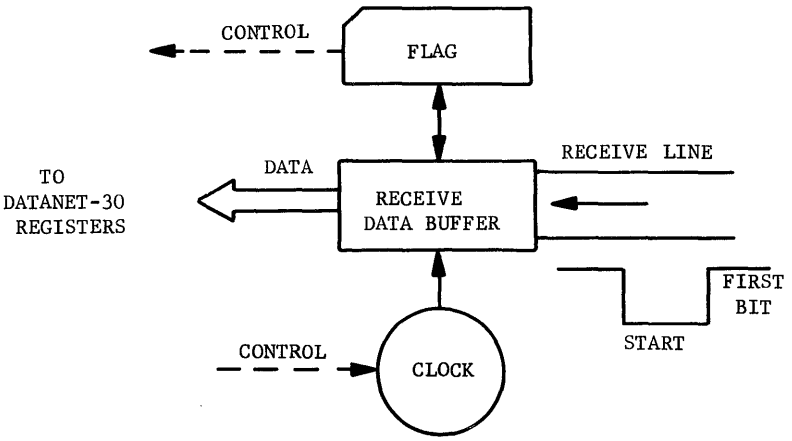


Figure 12. Receive Mode

Transmit Operation. The following is a brief description of the operation of the transmit section. Assume that the program is not sending anything and that the transmit flag is set. This means that the bit buffer is ready to take a new bit. The program sends a bit to the transmit data buffer. This automatically resets the transmit flag. At regular intervals, the bit buffer transfers the bit in the transmit data buffer to the transmission line. When this happens, the transmit flag is automatically set by the bit buffer unit.

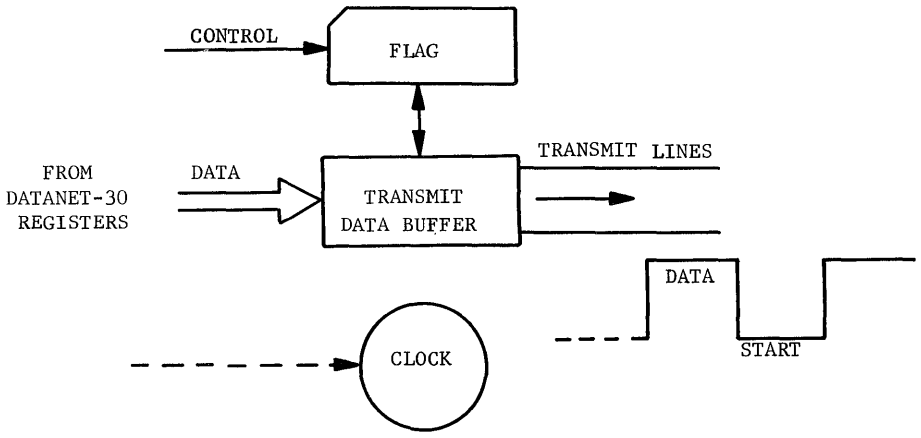


Figure 13. Transmit Mode

Since the bit buffer will transfer the bit in the transmit data buffer onto the line whether or not a new bit has been supplied, the program must test the transmit flag and provide a new bit before this transfer occurs. This process will repeat for each bit in the character. At the end of the bit stream which the program sends, the last bit will remain in the transmit data buffer and will be transferred to the line regularly. Therefore, the last bit in a bit stream will normally be a mark so that the line remains in the mark condition when no information is being transmitted. Note that with a bit buffer channel, the length of a character is completely under control of the program.

Echoplex

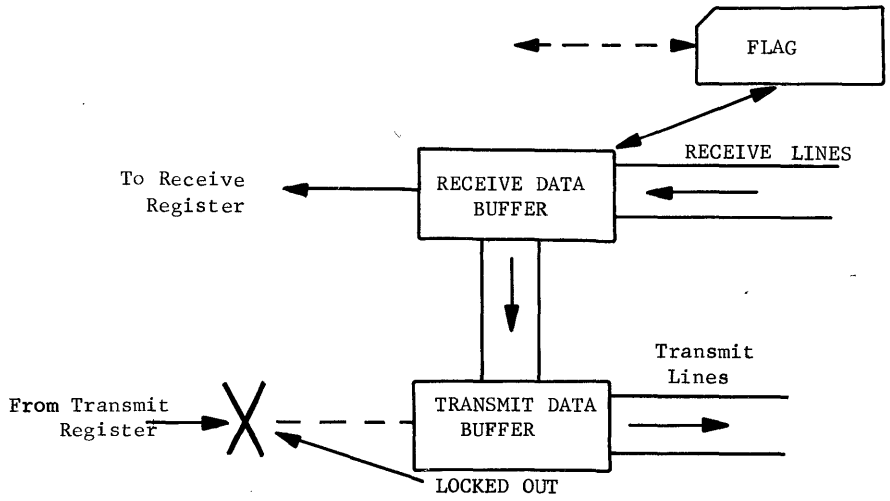


Figure 14. Echoplex Mode

Transmission errors may be detected by using a bit buffer with full duplex line in the following manner.

A bit buffer has the capability of echoing what is received. This is controlled by activating the appropriate instruction and, therefore, is under program control. When echoing, the bit received by the receive section is retransmitted over the transmit portion of the full-duplex line. In this way, a terminal device with error control capability can verify what was received by the DATANET-30 (actually, what is received back by the terminal device). Whenever a bit buffer channel is set up for echoing, the transmit section is locked out so that the bit ordinarily in the transmit data buffer cannot interfere with what is being sent back to the terminal device.

The usual equipment at the transmitting end is a keyboard printer send/receive unit. The information is transmitted in the normal manner but the printer does not print a hard copy as a direct result of the transmission. The transmitted signals are received by the receive section of a bit buffer and immediately transmitted back to the page printer of the transmitting terminal. Thus, the printed information indicates the number of possible errors involved in the transmission of the message.

This technique quickly shows whether or not the lines are working properly and in the case of an administrative message, whether or not it is possible to "read thru" the errors. If the errors are too high, the transmitting terminal can take appropriate action. If the transmission contains important numerical data where the numbers must be correct, the transmitting station again can immediately verify that the transmission was satisfactory.

The Character/Word Unit Module (CWU 930)

The character/word unit module occupies one module space and can contain either two Character Buffer Channels (CBC), two Word Buffer Channels (WBC), or one of each. The buffer selector address of each CBC or WBC is specified by the wiring of the address plug for the module, and each may be addressed independently of the other.

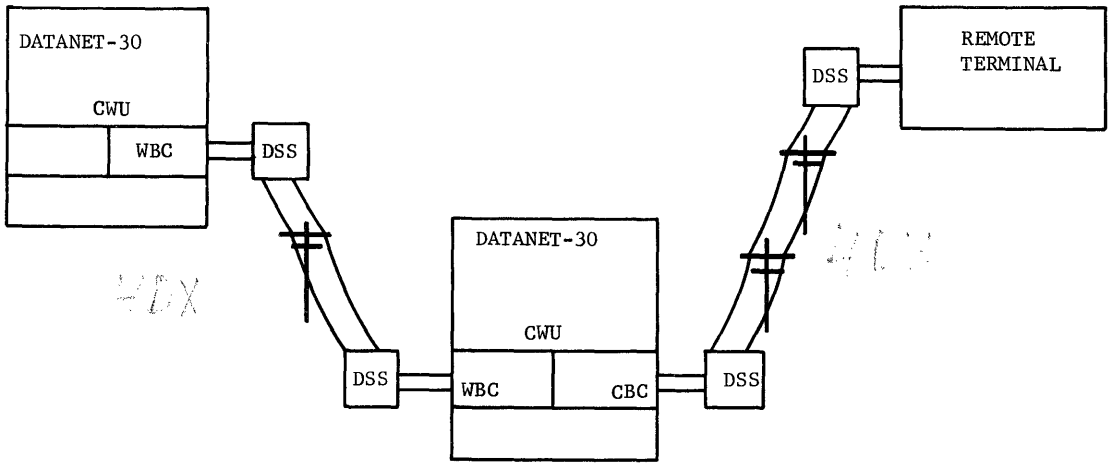


Figure 15. Character/Word Buffer Channel

The Character/Word Unit (CWU) provides buffering for one character (5, 6, 7 or 8 bits) of information between the DATANET-30 and the communications lines; or provides buffering for one word (20 bits) of information between two DATANET-30 data communications processors. As a character buffer, it is used on lines with transmission rates from 300 to 2400 bits per second with stop-start asynchronous format (e.g., normal Teletype).

THE CHARACTER BUFFER CHANNEL (CBC 930). The character buffer channel provides the interface between the DATANET-30 and a high speed remote terminal device over a half-duplex transmission line. Two character buffer channels are needed for full duplex operation.

A character buffer channel buffers a character length bit stream where the length is determined by the code of the remote terminal. Each CBC has a code level plug and a timing connector plug. The code level plug is specially wired for the character length of each CBC. The standard character lengths are 5, 6, 7 and 8 level code characters. System considerations require that a CBC be used on lines operating at 300 or more bits per second. The timing connector plug for a CBC would be wired for transmission speeds of 300, 600, 800, 1050, 1200, or 2400 bits per second. The transmission rate for each CBC may be independently selected.

Receive Sequence of the Character Buffer. The following is a brief description of the operation of an 8-bit character buffer channel in the receive mode. A word buffer channel will operate in exactly the same way except for the number of data bits. Assume that the CBC has been put in the receive mode by the program, that the receive flag is reset, and that the sending unit is transmitting marks, (i.e., it is idle). Now the sending unit starts to transmit an 8-bit word. The word is preceded by a start bit (a space) and followed by a stop bit (a mark). When the start bit is received, a clock is started. The clock is used to time the future sampling of the line. The start bit is shifted into the shift register. At regular intervals, the line is sampled and the bit which is there is shifted into the shift register. When the shift register is full, the 8-data bits are automatically transferred into the data register, the receive flag is set, and the clock is stopped. The clock will start again and the above process will repeat when the next start bit is received on the transmission line. As a protection against noise on the transmission line causing the clock to start running, the CBC circuitry requires the space condition to exist on the line for at least one-half of a bit time to start the clock; thus noise of less duration than one-half of a bit time will have no effect. Since the CBC will transfer a character from the shift register into the data register whether or not the data register and receive flag are reset, the program must test the receive flag and take the character before another one is transferred into the data register. When the program takes the character from the data register, the data register and the receive flag are automatically reset.

Transmit Sequence of the CBC. The following is a brief description of the operation of an 8-bit CBC in the transmit mode. Assume that the program has put the CBC in the transmit mode, the CBC is in the process of sending a word out on the line, and a word is waiting in the data register. When the current character has been shifted onto the line, the CBC will transfer the character in the data register to the shift register. At this time, the transmit flag will automatically be set. The 8 bits transferred into the shift register will automatically be preceded by a start bit and followed by 2 stop bits for transmission on the line, i.e., a total of 11 bits. When the shift register is again empty, the CBC will transfer the character in the data register to the shift register and repeat the process if the transmit flag is reset. However, if the transmit flag is still set, indicating that the program has not put a new character into the data register, the CBC will continue to put stop bits (marks) on the line until the transmit flag is reset. When the program transfers a character into the data register, the transmit flag will be automatically reset and the above process will be repeated. For maximum line utilization, the program must test the transmit flag and supply a new character before the current one has been completely shifted onto the line.

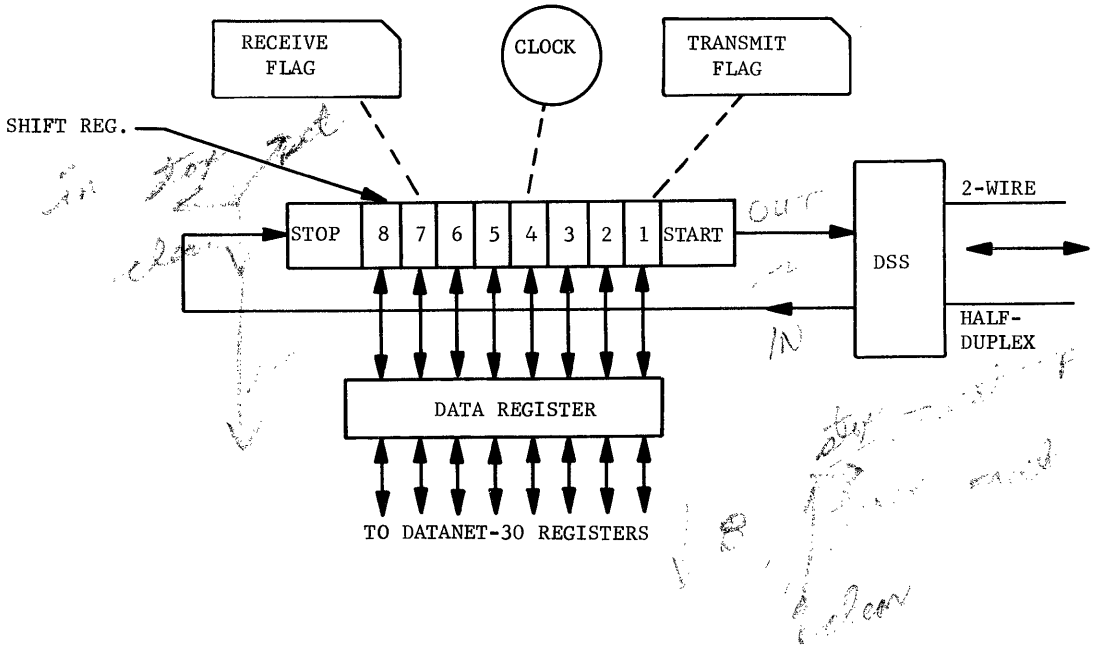


Figure 16. Character Buffer Transmit and Receive

WORD BUFFER CHANNEL (WBC). The word buffer channel provides the interface with another DATANET-30 via a half-duplex transmission line. The WBC buffers a 20-bit word (plus start/stop bits) at transmission speeds of 300, 600, 1200, 1800, 2000, or 2400 bits per second, depending on system considerations. The code level plug and the timing connector plug would be wired in

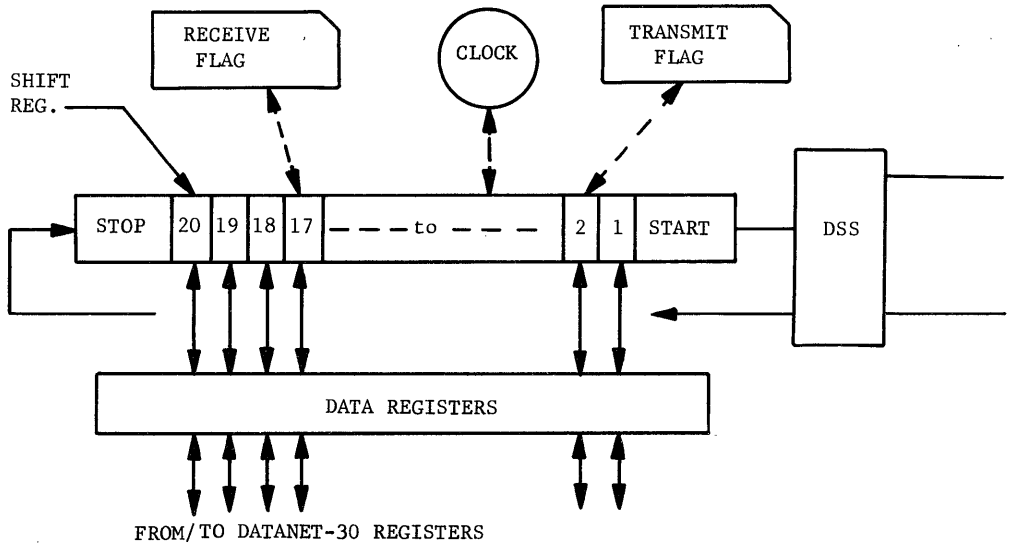


Figure 17. Word Buffer Channel Transmit and Receive

accordance with system requirements. The 20 bit word transmitted (received) consists of an 18 bit word from the DATANET-30 memory plus one parity bit and one control bit generated by the transmitting DATANET-30.

The sequence of transmit and receive for the WBC is the same as for the character buffer channel except for the automatic addition of the parity and control bits to the transmitted word.

Character/Word Unit Module (CWU 931)

The Character/Word Unit module CWU 931 occupies one module space and is similar to CWU 930 except that characters are transmitted and received on a character synchronous basis. The character/word unit module (CWU 930) can contain two character buffer channels (CBC 931). A code level plug is required for each CBC 931.

CHARACTER BUFFER CHANNEL (CBC 931). One buffer channel provides the interface between the DATANET-30 and a half-duplex transmission line. The CBC is synchronized by the digital subset connected to the transmission line and therefore does not require a timing connector plug.

The buffer control unit contains hardware to control the character length as defined by the code level plug. Buffers in a module may be operating at different character lengths. The buffer channel operates with a character oriented device at speeds determined by the subset and remote terminal. A synchronous digital subset must be on each end of the transmission line. The standard bit rates are 2000 and 2400 bits per second.

The code level may be from 5- to 16-bit codes with character synchronization (no start/stop bits). The code level (character length) is selected or changed by a code level plug for each CBC. By changing code level plugs, the code level may be varied to meet different remote terminal operations or programming techniques.

The code level plug also defines the bit configuration of the synchronizing character, the number of bits per character, and where the receive lines will enter the data bits into the "working" register (A or B register); that is, the high- or low-order position of the A or B register. The code level plug can be arranged to accept two characters (8 level) before setting the receive flag. Also, the code level plug can be arranged to mask off a bit. The line interface is Bell System Dataphone Model 201A or 201B Data Set or equivalent.

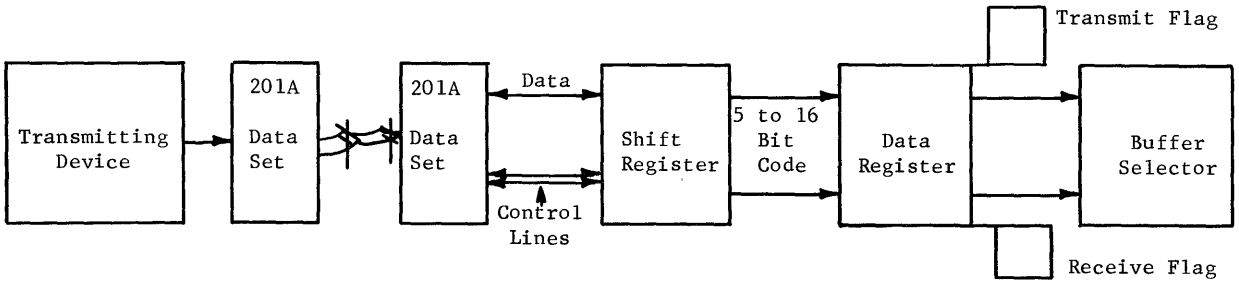


Figure 18. Character Buffer Channel Block Diagram

Dialing Adapter Unit Module (DAU 930)

The Dialing Adapter Unit module may contain from one to ten Dialing Adapter Channels, DAC 930. The module is mounted in one of the spaces provided for buffer modules that interface with the buffer selector. Each DAC is an independent unit operating through the buffer selector and is associated with one transmit/receive buffer, such as a bit buffer, or character buffer, etc. Two buffer selector addresses are required, one for the DAC and one for the associated buffer.

DIALING ADAPTER CHANNEL (DAC 930). The General Electric Dialing Adapter Channel (DAC 930) provides the means for dialing telephone numbers of remote locations to transmit or receive data. The DAC 930, with its associated telephone equipment, enables the DATANET-30 to dial virtually any telephone number connected with the Bell System.

The associated telephone equipment consists of an Automatic Calling Unit (ACU) and a Data Set. The DAC 930 is used only to place the telephone call. The ACU actually dials the number and makes the connection.

The transmission or reception of data takes place through the associated Data Set and buffer on the buffer selector. Only one transmission line is associated with each DAC, ACU, and Data Set. If it is desired to dial out on more than one line, a separate DAC, ACU, and Data Set are used for each line (or call). Incoming calls are handled by the Data Set.

The DAC provides one four-bit digit buffer. One four-bit binary-coded decimal digit (0_{10}-9_{10}) at a time is presented to the DAC by the DATANET-30 program. This digit occupies the four least-significant positions of a DATANET-30 word. The DAC then presents this digit to the telephone company ACU for dialing.

Configurations

A DAU may be set up in the configurations shown in Figures 19 and 20.

Controls and Indicators

There are no controls or indicators in the usual sense except for the MANUAL CLEAR button on the DATANET-30 control panel. All other controls and indicators are by program only.

Buffer Operations

The Dialing Adapter Channel and the Automatic Calling Unit may be used with several different digital subsets and transmit/receive buffers. The buffers in turn can connect to a variety of terminal equipment. The DEF and NES instructions for the transmit/receive buffers vary in accordance with the buffer used, the digital subset used, and the terminal equipment.

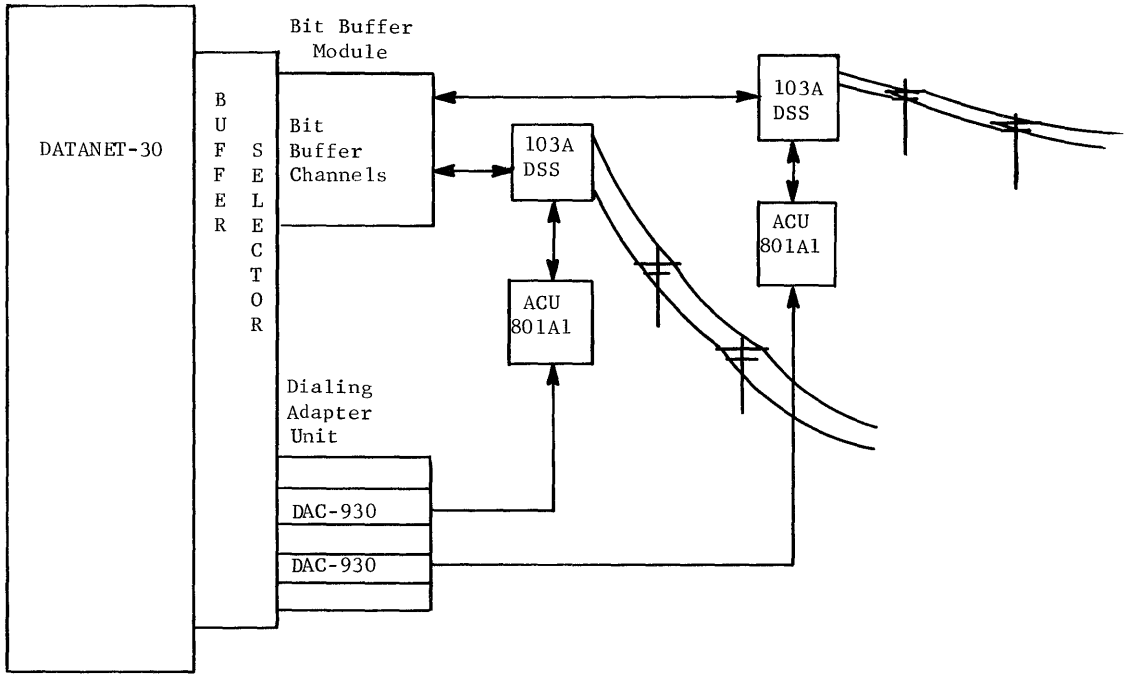


Figure 19. Dialing Adapter Units with Telephone Equipment and Bit Buffers

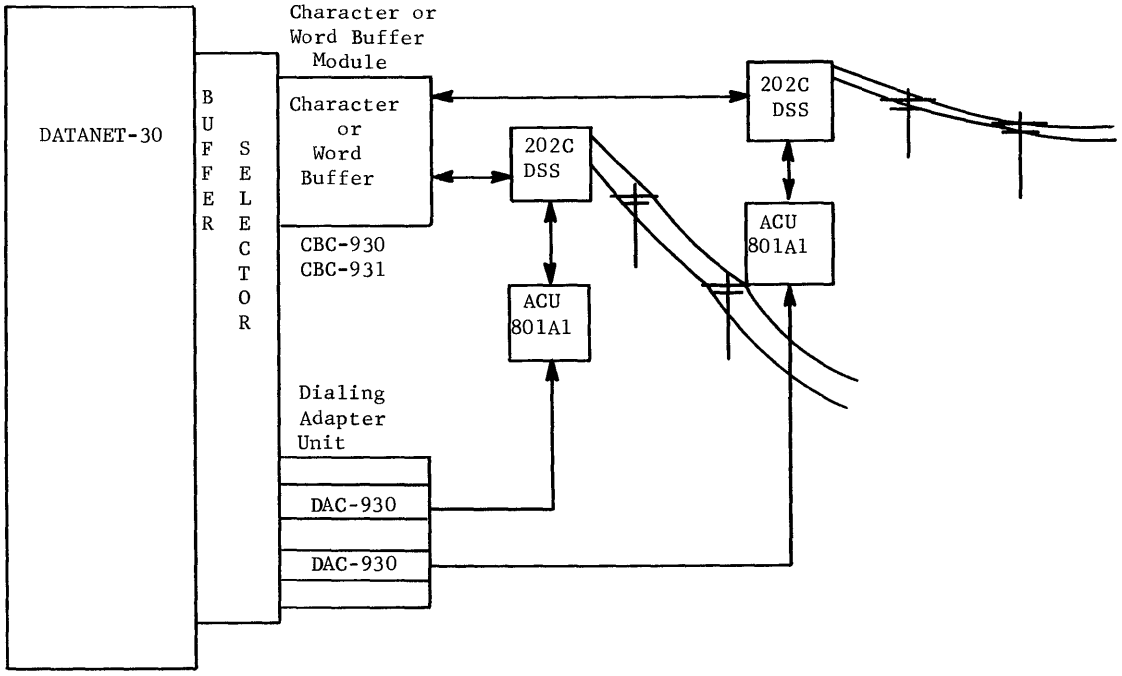


Figure 20. Dialing Adapter Units with Telephone Equipment and Character or Word Buffers.

Automatic Calling Unit (ACU)

The Telephone Company Data Auxiliary Set 801A for automatic calling is not covered in great detail. Anyone interested in more information than contained here may obtain a copy of the Data Auxiliary Set 801A-Interface Specification (March 1964) from:

Data and Teletypewriter Planning Engineer
American Telephone and Telegraph Company
195 Broadway
New York, New York 10007

The operating features of the ACU pertinent to the operation of the DAC are:

1. The ACU obtains the dial tone in response to a Call Request from the DAC.
2. The ACU dials the digit received from the DAC.
3. When the last digit has been dialed, the ACU waits for the called location to answer.
4. The ACU detects the answer signal.
5. The ACU then transfers control of the call (telephone line) to the Data Set connected to the ACU and the transmit/receive buffer.
6. If the call cannot be successfully completed, the Abandon Call and Retry timer of the ACU notifies the program.

INTERCONNECTING COMPUTER BUFFERS

Processor Interrupt Unit (PIU 930)

The DATANET-30 Processor Interrupt Unit (PIU 930) allows transfer of data from the memory of one DATANET-30 to the memory of another. One processor interrupt unit (PIU) for each DATANET-30 is required. Each PIU occupies one option module space and is assigned an address on the buffer selector. The address is specified by the address plug for the PIU.

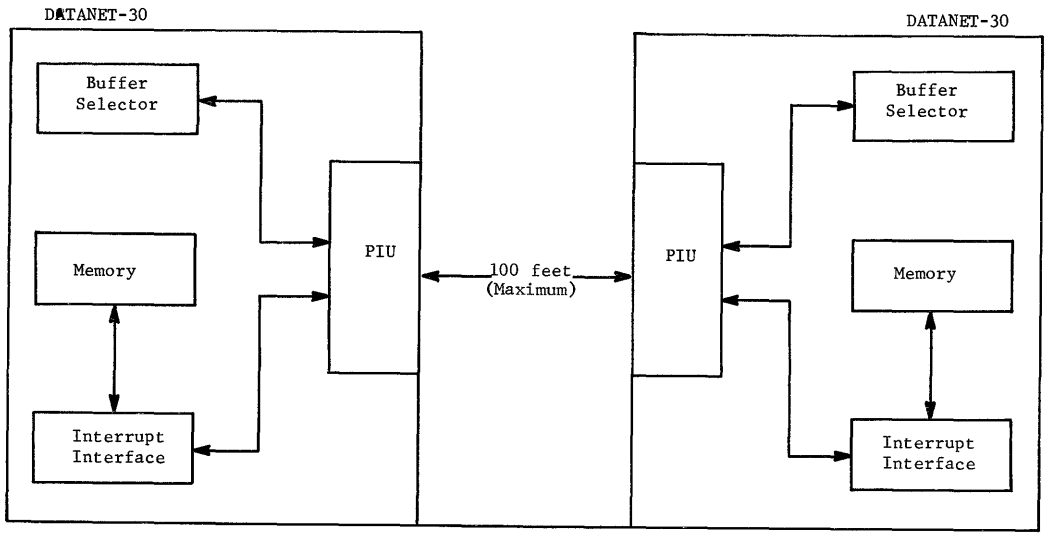


Figure 21. PIU Connecting Two DATANET-30's

Data Transfer

The PIU connects to the memory interrupt interface and is normally assigned interrupt cycle two. Only one interrupt cycle may be assigned to the PIU. This allows a transfer rate of 28,000 DATANET-30 words per second.

Data is transferred in both directions, but only in one direction at a time. Control of the direction of data transfer is established by either DATANET-30 on a receive only basis.

The PIU does not allow a program to initiate transmission. The DATANET-30 which is to receive data must initiate the data transfer. This method of operation protects the memory in one DATANET-30 from being destroyed by mistake by the other DATANET-30 program.

CONTROLS AND INDICATORS. All controls and indicators are by program only, except for manual reset on the control panel.

COMPUTER INTERFACE UNIT (CIU 931)

The CIU 931 Computer Interface Unit provides the means for connecting the DATANET-30 and a GE-400 or -600 Series computer (Figure 22).

The computer interface unit (CIU) connects into the buffer selector of the DATANET-30 and into one standard input/output channel of the other computer. The buffer selector address of the CIU is specified by the buffer selector address channel for the CIU. Since the CIU connects the DATANET-30 with either a GE-400 or -600 Series computer, for the purposes here, both of these computers will be referred to as the "external computer." More than one CIU can be installed in a DATANET-30. Each CIU occupies two modules. There is no restriction on the number used, other than the physical space occupied.

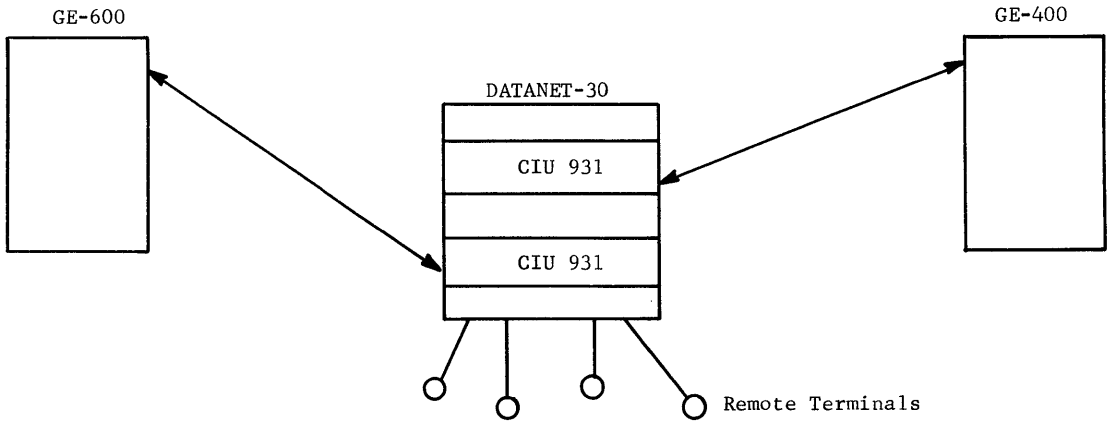


Figure 22. CIU 931 Connecting a DATANET-30 with an External Computer

Data Transfer

Data is transferred in both directions but only in one direction at a time. Control of the direction of data flow is established and maintained by either the external computer or the DATANET-30, Should both the DATANET-30 and the external computer desire control at exactly the same time, the external computer is given priority.

The CIU has an 18-bit buffer. Data is transferred one character at a time to or from the external computer and one DATANET-30 word at a time to or from the DATANET-30. The CIU contains the necessary shift circuitry to accumulate characters into words and separate sequential characters, depending on the direction of data transfer. Data transfer is illustrated in Figure 23.

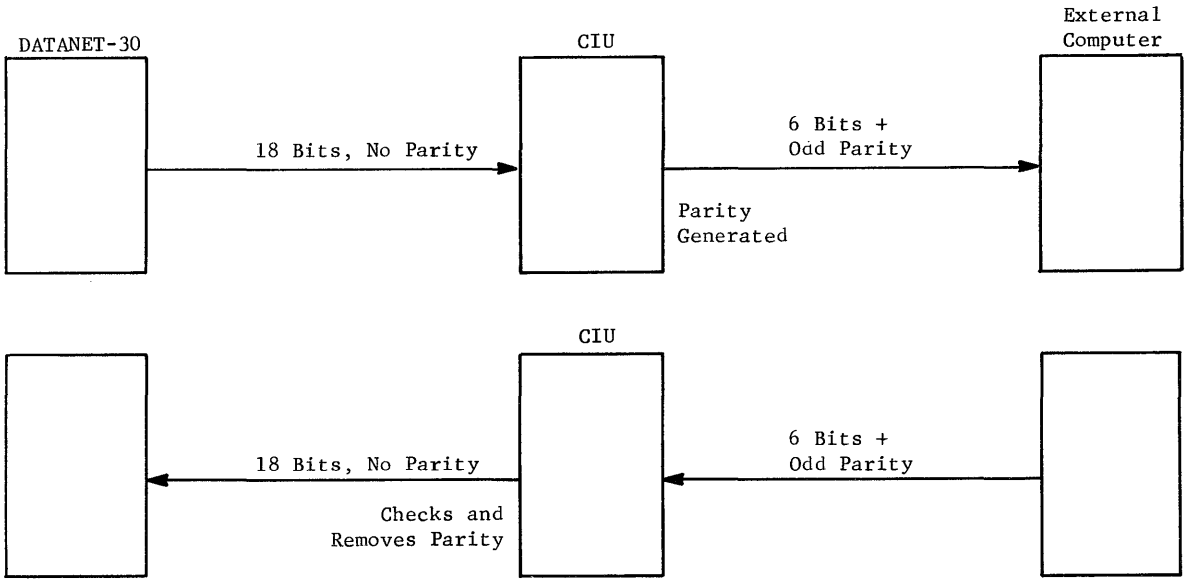


Figure 23. Data Transfer Through a CIU 931

DATANET-30 TO THE COMPUTER INTERFACE UNIT. When the CIU has received a word from the DATANET-30, a signal for the external computer to read is generated. The external computer initiates the transfer of one character at a time from the CIU. When the three characters have been transferred, the CIU notifies the DATANET-30 that another word can be transferred. The DATANET-30 program then transfers another word to the CIU. This process continues until the DATANET-30 or external computer sends an End Data Transfer signal to the CIU.

EXTERNAL COMPUTER TO THE COMPUTER INTERFACE UNIT. When the CIU has received three characters from the external computer, a signal for the DATANET-30 to transfer the three characters is sent to the DATANET-30. The DATANET-30 program must detect this signal and transfer the data from the CIU. When the data has been transferred from the CIU, the external computer can transfer three more characters to the CIU. This process continues until the external computer or DATANET-30 sends an End Data Transfer signal to the CIU.

DATA FLOW THROUGH THE COMPUTER INTERFACE UNIT. When data is transferred from the CIU to the external computer, the most significant character of the DATANET-30 word is transferred first and the least significant last.

Characters received by the CIU from the external computer are assembled into a three-character word. The first character is transferred to the most significant part of the DATANET-30 word and the third character is transferred as the least significant.

If an End Data Transfer signal is received from the external computer before a full three-character word is shifted into the CIU, the characters in the data register are shifted to the most significant positions. Zeros are inserted by the CIU into the unfilled character positions before the word is tranferred to the DATANET-30.

COMPUTER INTERFACE UNIT (CIU 930)

The Computer Interface Unit (CIU 930) provides the means for connecting a DATANET-30 and a General Electric 215/225/235 Computer. The Computer Interface Unit occupies one module of the DATANET-30. DATANET-30 must be within the standard distance of 50 feet from the computer. The DATANET-30 would be considered the same as another controller to the GE-200 Series computer as far as memory interrupt of the computer is concerned. However, the GE-200 Series computer cannot interrupt or access the DATANET-30 as is done with other controllers.

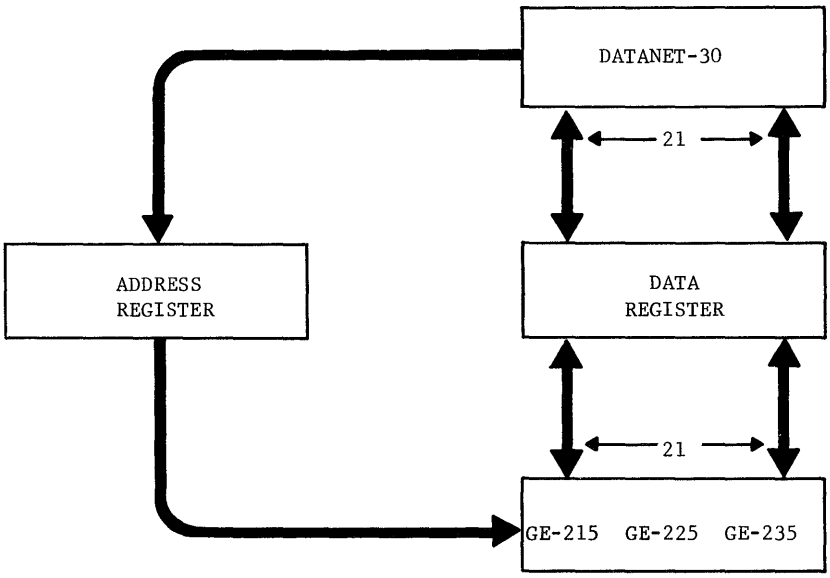


Figure 24. CIU 930 Connecting a DATANET-30 And a GE-200 Series Computer

Data Transfer

The CIU transfer 21-bit words between the DATANET-30 and the computer. The word is transferred in parallel. The memory address is also transferred in parallel from the address register to the GE-200 Series computer prior to data transfer. At the DATANET-30, the 21-bit word consists of an 18-bit word from memory, plus 1 parity bit and two control bits generated by the DATANET-30 circuitry. At the GE-215, 225, or 235 computer, this 21-bit word represents a 20-bit word plus memory parity.

The CIU allows addressing any location in the GE-200 Series computer memory. The CIU connects into any channel of the DATANET-30 buffer selector in the same manner as any other DATANET-30 buffer. The buffer selector address of CIU is specified by the wiring of the buffer selector address plug for the CIU module. There is no DATANET-30 hardware restriction on the number of CIU's which may be used, other than the physical space occupied. On the computer side, the CIU can connect into any plug of the GE-200 Series computer controller selector.

The computer interface unit can be tested for a Busy-Not Busy condition, by the DATANET-30. This Busy-Not Busy test tells the DATANET-30 whether or not it can put data into the data register and address register, and whether or not it can take data from the data and address registers.

When the computer has traffic for the DATANET-30, the computer will set a flag in the computer memory, which is interrogated by the DATANET-30. When the DATANET-30 is ready to accept the traffic, a control instruction is sent to the computer, the computer program is interrupted, and the traffic is transmitted under control of the DATANET-30. The DATANET-30 then processes the traffic and sends it on to the remote station for which the traffic is intended. Thus the computer and the DATANET-30 exchange control words, instructions and traffic under the control of the DATANET-30.

RECEIVE SEQUENCE. The following is a brief description of the operation of a CIU in the receive mode; that is, taking words out of the GE-225 memory. Assume that nothing is happening as far as the CIU is concerned. At some point, the program in the DATANET-30 decides to take a block of words. The program puts a number equal to one less than the initial address of the block--the GE-225 address--in the address register of the CIU. Then the program sends a control signal to the CIU which increases the address register by one, puts the CIU in the receive mode, resets the data register, interrupts the GE-225 program for 1 word time, and initiates the transfer of the word from the specified GE-225 memory location to the data register in the CIU. After the word is in the data register, the CIU is no longer busy--this condition can be tested by the program. The program now executes an instruction to take the word out of the data register of the CIU and into the DATANET-30. This instruction also increases the address in the CIU address register by one, puts the CIU in the receive mode, resets the data register, and initiates the transfer of another word from the GE-225 memory. This process repeats until the DATANET-30 program decides that sufficient words have been received.

TRANSMIT SEQUENCE. The following is a brief description of the operation of a CIU in the transmit mode; that is, transferring words into the GE-225 memory. Assume that nothing is happening as far as the CIU is concerned. At some point, the program in the DATANET-30 decides to put a block of words into the GE-225. The program puts a number equal to one less than the initial address--the GE-225 address--in the address register of the CIU. Then the program transfers a word into the CIU data register with an instruction. This instruction also puts the CIU in the transmit mode, increases the address in the address register by one, interrupts the 225 program for 1 word time, and initiates the transfer of the word from the data register into the GE-225 memory. After the word has been written in the GE-225 memory, the CIU is no longer busy. The DATANET-30 program can now put another word in the data register and send it to the GE-225. This process repeats until the DATANET-30 program decides that sufficient words have been transferred.

PERIPHERAL EQUIPMENT BUFFERS

The Controller Selector Unit

The controller selector unit permits attaching GE-200 Series computer peripherals to the DATANET-30 and enables simultaneous transfer of data to and from the DATANET-30 on a memory interrupt basis. The eight high speed channels, numbered 0 through 7, operate on a priority basis, with channel 0 having the highest priority and channel 7 the lowest.

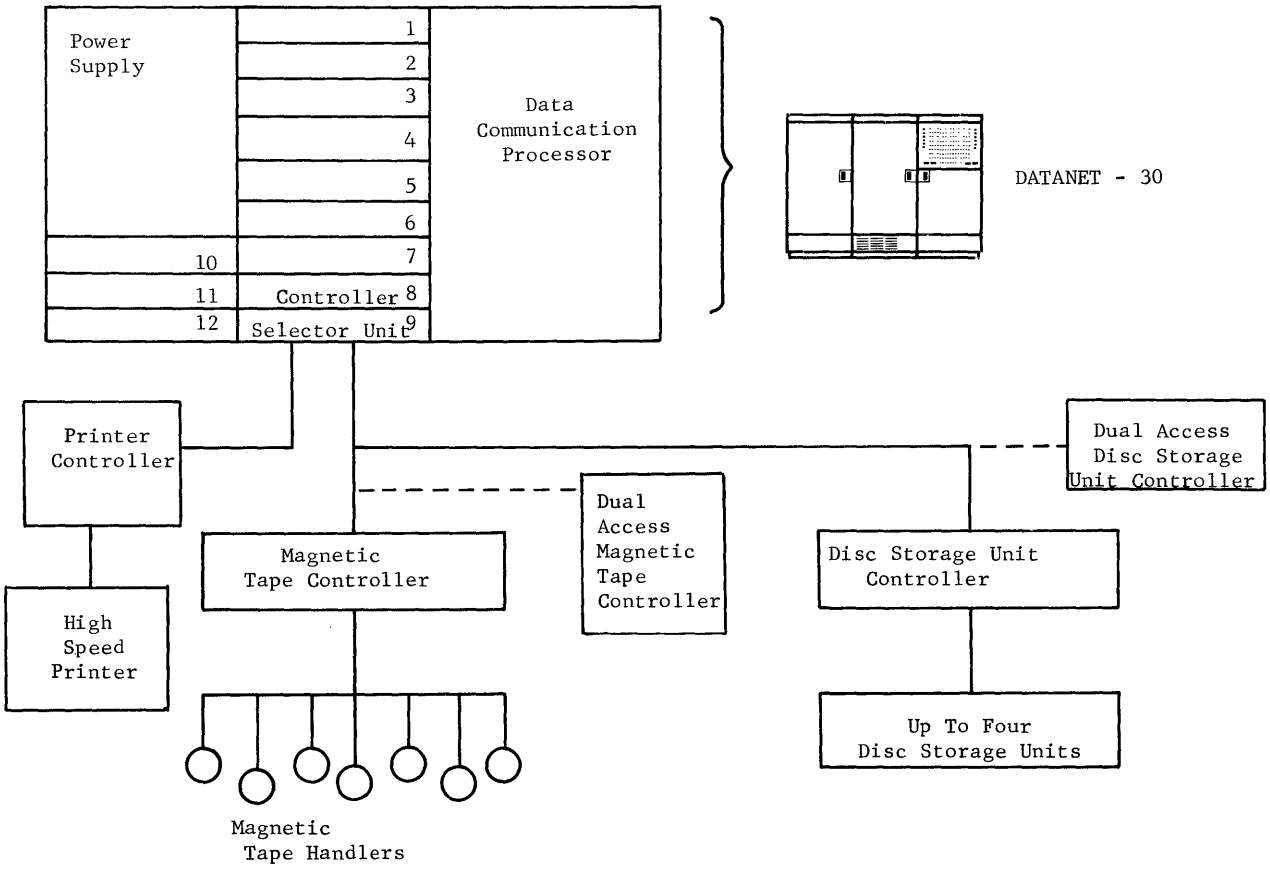


Figure 25. DATANET-30 with Controller Selector Unit and Peripheral Equipment

Peripheral Equipment Information. Information for each peripheral device is contained in the manual for the particular peripheral equipment and in the appropriate appendix of CPB 1019A, the DATANET-30 Programming Reference Manual.

Common Peripheral Channel

The Common Peripheral Channel (CPC) module permits connecting GE-400 or 600 Series peripheral equipment to the DATANET-30, and enables data transfer to and from the DATANET-30 on a memory interrupt basis.

Each CPC occupies two option module spaces, and is assigned an address on the buffer selector. The address is specified by the address plug for the CPC. One peripheral device at a time connects to one CPC.

From one to four CPC's can be installed in a DATANET-30. The maximum is determined by the space available or by the number of memory interrupt cycles used.

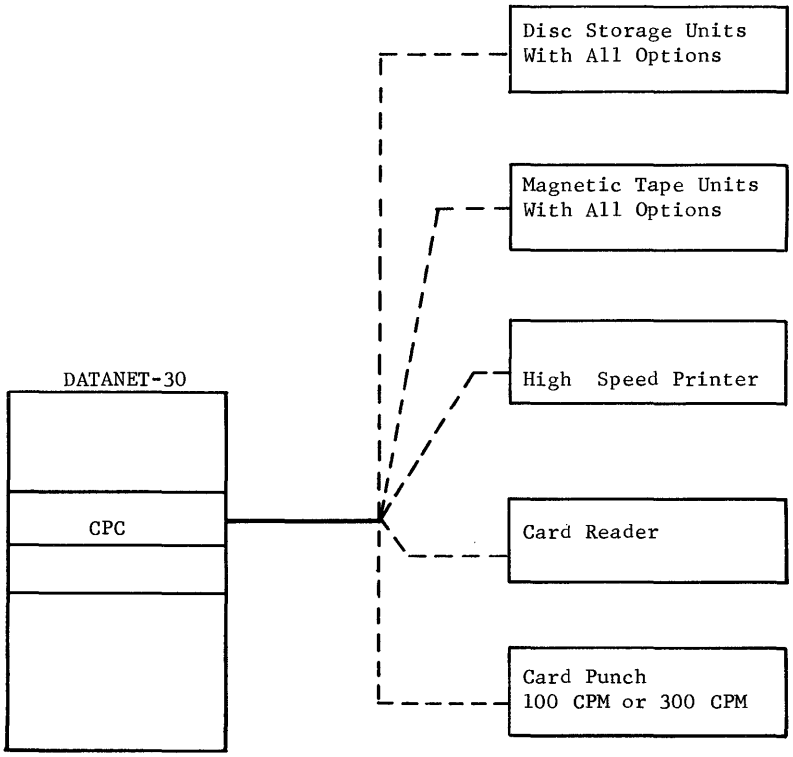


Figure 26. CPC Peripheral Equipment

DATA TRANSFER. Data is transferred via the CPC one character at a time to or from the peripheral and one DATANET-30 word at a time to or from the DATANET-30. The CPC contains the necessary shift circuitry to accumulate characters into words and to separate sequential characters, depending on the direction of transfer.

The CPC can transfer any number of characters from 0 to 49,152 (16,384 word memory at three characters/word) between a peripheral and the DATANET-30 memory. Any starting address within a 16k memory may be specified. The CPC accesses memory sequentially under memory interrupt control.

PERIPHERAL EQUIPMENT INFORMATION. Information for each peripheral device is contained in the manual for the particular peripheral equipment and in Appendix G of CPB 1019A, the DATANET-30 Programming Reference Manual.

RDC 930 REMOVABLE DISC STORAGE SUBSYSTEM

The RDC 930 Removable Disc Subsystem provides the DATANET-30 with a low-cost, removable media, random access storage unit packaged in modular free-standing cabinets. The disc control unit contains two disc mechanisms. Additional storage units may be added for a maximum of six disc mechanisms per system.

Communication with the DATANET-30 is provided by the Removable Disc Unit Module RDU 930 mounted in the DATANET-30 option module rack. One module space is required for the RDU 930. The RDU 930 interfaces with the buffer selector and interrupt interface of the DATANET-30. The buffer selector address is specified by the buffer selector address plug for the RDU 930. The block diagram, Figure 27 illustrates a complete DSU-100 Subsystem.

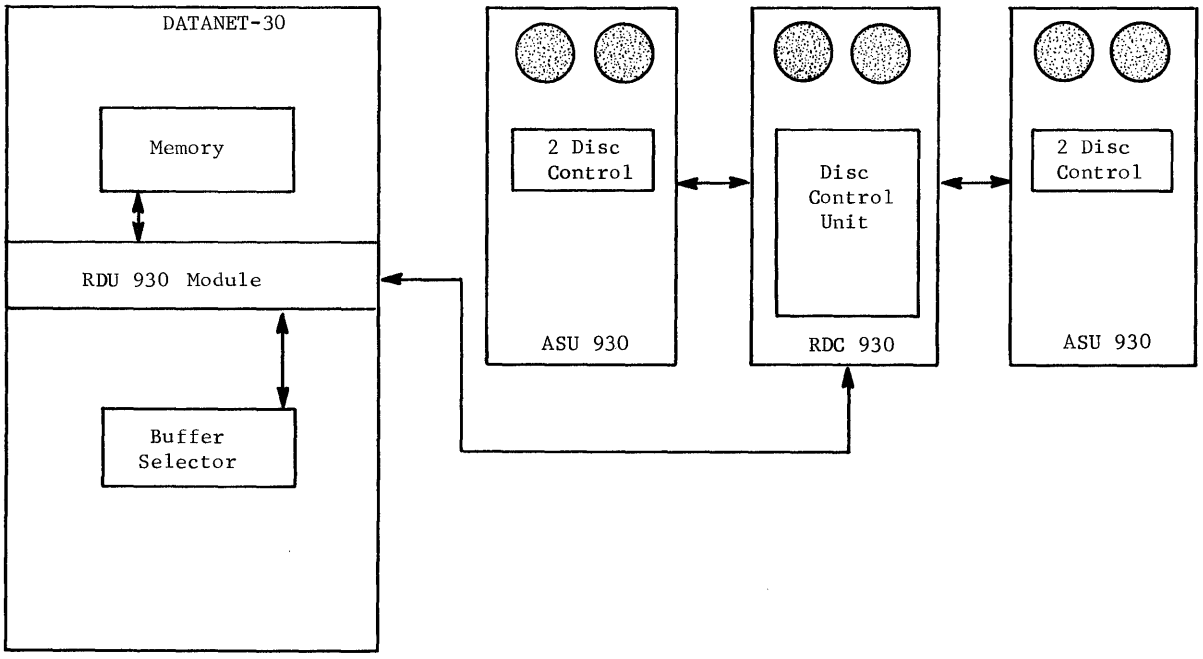


Figure 27. DATANET-30/RDC 930 Block Diagram

Removable Disc Unit Module (RDU 930)

The RDU 930 provides the necessary control functions to transfer data to or from memory, and to issue commands to the disc control unit. The interrupt interface allows the transfer of an 18-bit DATANET-30 word to or from memory on a memory interrupt basis.

The memory address counter directs the flow of data. Up to 16,384 consecutive memory locations may be addressed. The address counter is counted up one, each time a word is transferred to or from memory. Command word sequencing control directs the RDU and the disc control unit.

Controls and Indicators

Except for manual reset on the DATANET-30 control panel, all controls and indicators for the RDU 930 are by program only. The controls and indicators for the RDC 930 are located on the disc control unit.

Memory Interrupt Cycle Assignment

The RDC 930 is assigned two out of five nonadjacent memory cycles. Selection of the memory cycles is determined by what other equipment in the system also uses interrupt cycles. When determined, switches on the RDU 930 are set to assign cycles to the removable disc system.

Two disc control units (RDC 930) can be connected to a DATANET-30 if different memory cycles are assigned. The number of disc control units that can be connected to the DATANET-30 is limited by the memory cycles available. A different buffer selector address would be used to address each RDC 930.

The disc control unit contains the necessary logic and circuits to control the read/write head positioning, data transfer, and associated functions of the removable discs located in the control unit, as well as provide some control functions for each additional storage unit (ASU 930).

Additional Storage Unit (ASU 930)

The additional storage unit (ASU 930) provides two additional disc handlers for added storage capacity. This unit is an additional cabinet with electronics and two disc drivers. It is connected to and is under control of the RDC 930. Two ASU 930 units may be connected to each RDC 930 providing a maximum of six disc drive mechanisms per disc control unit.

Extra Removable Disc Cartridge (ASD 930)

Extra removable discs may be kept available in the same manner as magnetic tape reels, thus providing a removable storage media.

CARD READER UNIT

One card reader unit (CRU 930) connects the CRF 930 card reader to the DATANET-30. The card reader unit occupies one option module space and is assigned an address on the buffer selector. The buffer selector address is specified by the address plug for the CRU.

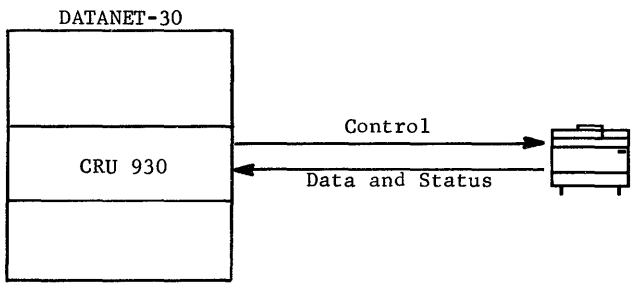


Figure 28. DATANET-30 with a Card Reader

Punch Reader Unit

The Punch Reader Unit (PRU 930) connects the CPF 930 card punch and the CRF 930 card reader to the DATANET-30. The card punch used is the GE-200 Series 100 card-per-minute punch. The card reader is optional with this module. When used, it operates the same as when the CRF 930 is installed with a CRU 930 module described above.

The card punch operates via the buffer selector and requires eight buffer selector addresses. The PRU 930 consists of two modules. Functional control of the punch is by the DATANET-30 program via the buffer selector.

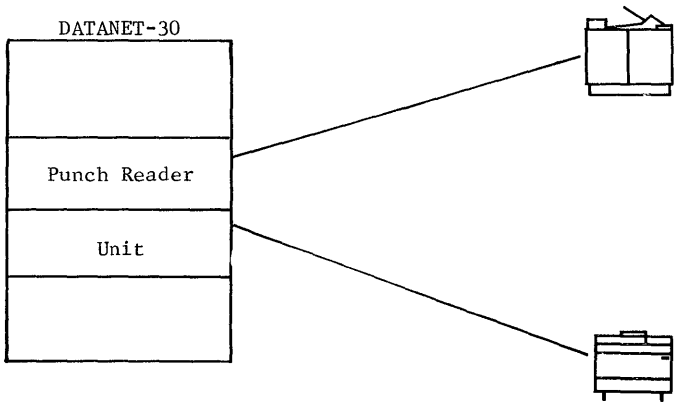


Figure 29. DATANET-30 with Card Punch and Reader Units

OTHER SYSTEM COMPONENTS

The GE-200 Series Peripheral Switch

The Peripheral Switch (PSC 201) is an optional feature for the GE-200 Series computers and the DATANET-30. The number of peripheral controllers which may be switched between the G-E systems is as follows:

GE-215	3 Peripheral Controllers
GE-225	8 Peripheral Controllers
GE-235	7 Peripheral Controllers
DATANET-30	8 Peripheral Controllers

This switching capability permits optimum utilization of all peripheral equipment for multiple systems operation. The peripheral switch control subsystem does not affect the independent and unrelated operation of the two central processors.

The peripheral switch consists of two types of units, the switch control console connected to two central processors, and the peripheral switch units each connected to one of the peripheral

controllers to be switched. A complete peripheral switch control subsystem consists of one switch control console and eight peripheral switch units. A minimum subsystem consists of a control console and one switch unit.

CONSOLE UNIT. The switch control console performs two functions: (1) assigns each controller selector to the desired central processor and (2) assigns the selected priority channel to each I/O device. The console is the control center of the peripheral switching subsystem. All controls necessary for the switching operation, and the interconnections for each of the peripheral switch units and the two central processors, are contained within the switch control console.

SWITCH UNITS. The switch unit contains switching relays. The unit is mounted inside the peripheral controller. Two standard priority control connectors on the switch unit connect to each of the central processors. Other connectors connect to the switch control console. Any combination of one or more peripheral controllers may be connected to the peripheral switch control console, limited only by any specific assignment characteristic of input/output devices on the controller selector.

Additional information is contained in the manual for the Compatibles 200 Peripheral Switch Control Subsystem.

PROGRAMMED PERIPHERAL SWITCH

The Programmed Peripheral Switch (PS-6010) is a modular, free-standing, program-controlled switch. It is used to connect either of two processors to a single peripheral controller. Each processor may be a GE-400 Series central processor, a GE-600 Series Processor, or a DATANET-30. A typical application of the PS-6010 switch is shown in Figure 30. For additional information, refer to the manual on this equipment.

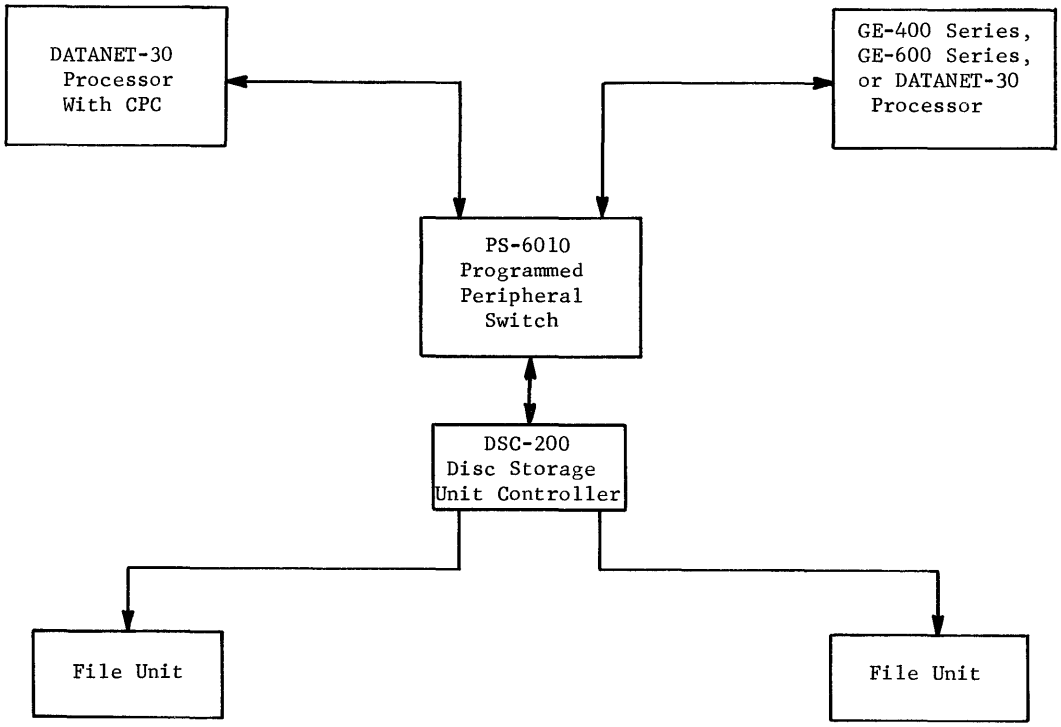


Figure 30. Typical PS-6010 Switch Application

THE GE-400/600 SERIES PERIPHERAL SWITCH. The peripheral switch subsystem (PSC 200) can be used with a GE-400/600 Series and DATANET-30 computer system.

One peripheral at a time would be switched to the CPC 930 of the DATANET-30. For additional information refer to the manual on this equipment.

Parallel Channel Adapter

The Parallel Channel Adapter is a manual switch used to switch communication lines from one DATANET-30 to another or to connect two DATANET-30's in parallel to the same line at the same time.

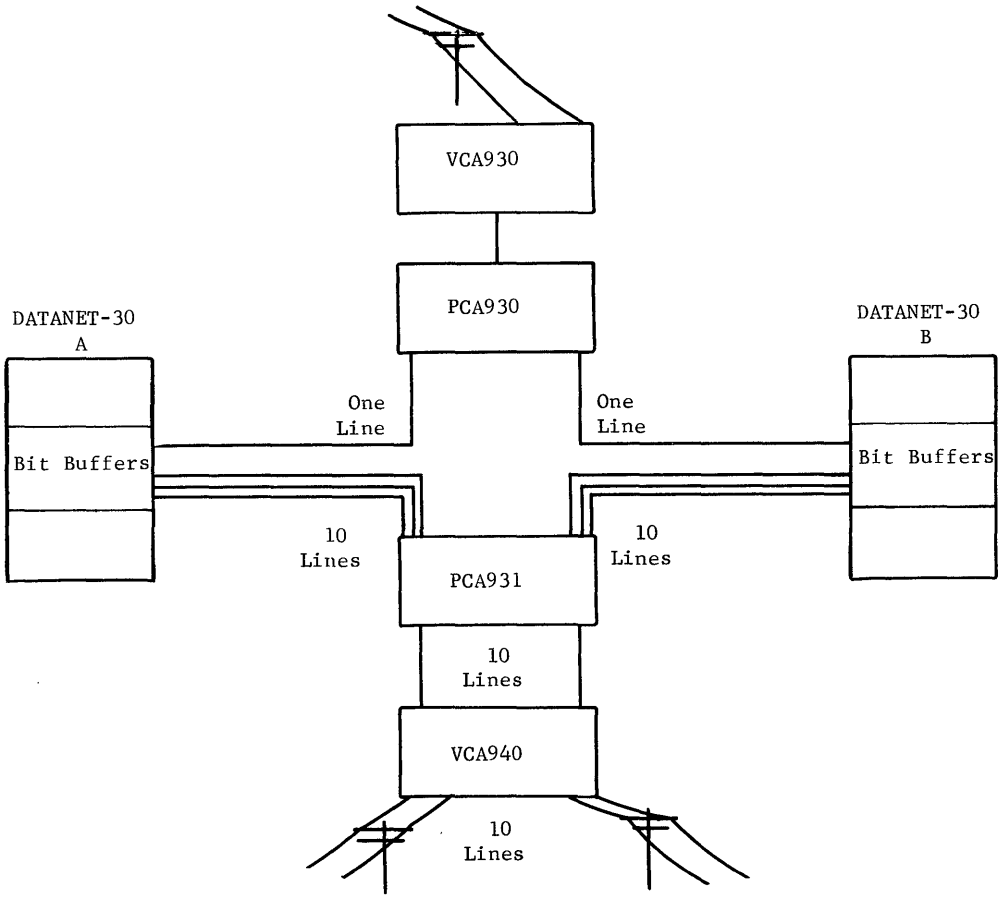


Figure 31. Parallel Channel Adapter Block Diagram

The Parallel Channel Adapter (PCA) can be used with bit buffers or character buffers, and is available in 2 models. PCA 930 is a single line switch used with buffers and Dataphone Dataset Model 103 A or F digital subsets, or character buffers and Dataphone Dataset 202 C or D. PCA 931 is a ten line switch used with buffers and voltage current adapters (line relay). Ten switches are provided so that any one, all, or any combination of circuits can be switched from either DATANET-30 to the other or operate in parallel.

The capability to operate in parallel means that the same communication lines are connected to each DATANET-30, both are receiving the same incoming data, and either can transmit on any circuit. The programs control which DATANET-30 is to transmit on which line.

The DATANET-30 With a GE-115 System

The GE-115 is ideal as a remote input/output terminal connected by communication lines to a central computer system. It can be taken off-line and will perform as a card processing system. As a remote terminal to a larger computer, it provides direct access to the larger system without the media conversion otherwise often required. For example, a GE-115 can generate an interrupt at a distant computer, and read in a program request followed by data to be processed. When the larger computer has performed the requested tasks, it transmits the data to the GE-115 to be printed or punched into cards.

On a voice grade line, card reading speed is 125 cards per minute minimum, card punching speed is 85 cards per minute minimum, or 95 lines per minute minimum on the line printer. Printer speeds can increase if printed lines are not a full 136 characters in length.

The Compact Card System offers a choice of: two memory sizes, one card reader, two card punches, and one line printer. The system can be tailored to fit most punched card center requirements. For additional information, refer to the manuals on the GE-115 Computer System.

DATANET-760 Keyboard/Display Terminal System

The DATANET-760 is an alpha-numeric display system that provides rapid, real time communications with a computer from local or remote locations. It uses a cathode-ray tube for displaying information, and enters data via the keyboard. For use with the General Electric Compatibles 200, 400, 600 and DATANET-30 processors, it provides convenient entry and display of data or requests, direct transmission to the computer, and receipt, storage and presentation of responses.

Data may be completely assembled and verified before it is sent to the computer. Changes, additions, or deletions can be made to existing records in the computer file, by displaying the data on the screen, and typing in changes on the keyboard. Hard copies of display data may be generated when optional page printers are installed.

SYSTEM CONFIGURATION. The DATANET-760 System consists of a Display Controller cabinet and a number of remotely located Display Terminals. The Display Controller is capable of communicating with a central computer system via a telephone data set or by direct connection. For additional information refer to the manual on the DATANET-760 system.

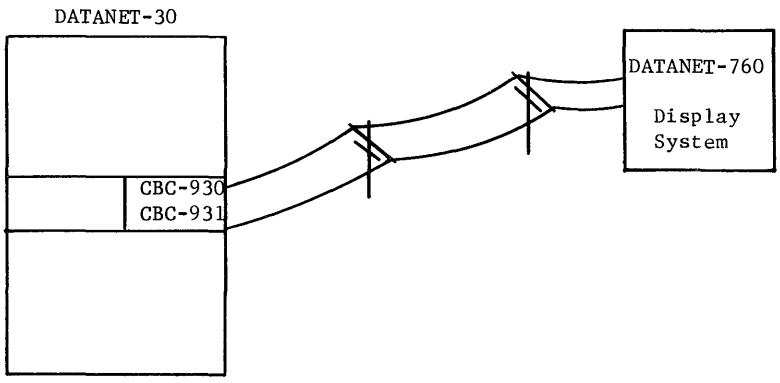


Figure 32. DATANET-760 Display System

SUMMARY OF DATANET-30 COMPONENTS

Summary of Buffer Modules

MODULE	# OF CHANNELS/MODULE	MODULE SPACE	MISCELLANEOUS INFORMATION
Bit Buffer	20 Simplex Channels 10 Half Duplex Channels 10 Full Duplex Channels 10 Full Duplex Channels in Echoplex Mode	1	VCA DSS-103 Timing Connector Plug Required 45 to 150 bits per second
Character/Word Buffer CWU-930	1 or 2 Simplex Channels 1 or 2 Half Duplex Channels 1 Full Duplex Channel 1 Simplex and 1 Half Duplex Channel	1	DSS-202,201,103,VCA One Timing Connector Plug and One Code Level Plug per Channel
Character/Word Buffer CWU-931	1 or 2 Half Duplex Channels	1	DSS-201 Synchronous. One Code Level Plug Required
Computer Interface Unit CIU-930	1 GE-215,225 or 235 Computer	2	One Channel of GE-200 Series Computer
Computer Interface Unit CIU-931	1 GE-400 or 1 GE-600 Computer	2	1 I/O Channel of the GE-400 or 600 Computer
Controller Selector Unit (CSU-931)	Disc Storage Unit Controllers and Disc Storage Units, Dual Access Controller Magnetic Tape Subsystem Dual Access Controller High Speed Printer	2	GE-200 Series Peripheral Equipment
Common Peripheral Channel CPC-930	1 Peripheral Equipment	2	One GE-400 or GE-600 Peripheral Equipment per CPC
Programmable Channel CPC-930	1 Peripheral Equipment	2	One GE-400 or GE-600 Peripheral Equipment per CPC
Programmable Peripheral Switch PS-60	1 Peripheral Equipment	None	Switches One Peripheral Controller Between Two Processors
Removable Disc Unit RDU-930	1 Removable Disc Storage Subsystem (RDC 930)	1	One Controller RDC-930 and 2,4 or 6 Removable Discs
Parallel Channel Adapter PCA-930	Parallels 1 Bit Buffer Channel or Character/Word Channel	None	VCA 103 A, F 202C 202D
Parallel Channel Adapter PCA-931	Parallels 10 Bit Buffer Channels	None	VCA
Dialing Adapter Unit DAU-930	10 Dialing Channels DAC-930	1	One Automatic Calling Unit, One Digital Subset and One Transmit/Receive Buffer Per Dialing Channel
Processor Interrupt Unit (PIU-930)	1 Channel	1	One for Each DATANET-30
Card Reader Unit	1 Reader (CRF-930)	1	Card Reader
Punch/Reader Unit PRU-930	1 Card Punch (CPF-930) 1 Card Reader (CRF-930)	2	Card Punch Card Reader

Summary of Transmission Speeds, Code Levels, Input/Output

Buffer		Transmission Speeds	Code Level	Word Length
Bit Buffer Unit		45 - 150 Bits Per Second	5,6,7 or 8	Optional to 18
Character/ Word Unit	Character Buffer Channel	300 - 2400 Bits Per Second	5,6,7 or 8	5,6,7 or 8
	Word Buffer Channel	300 - 2400 Bits Per Second	DATANET-30 Word	5 to 20 Bit Word
Computer Interface Unit CIU-930		13 KC Maximum Parallel 20-Bit Word Transfer rate	Computer Word	21 Bit Word
Controller Selector		57.6 Maximum Parallel Transfer Rate	Peripheral Coding	18 Bit Word
Computer Interface Unit CIU-931		13KC Maximum Word Transfer	Computer Word	18 Bit Word
Removable Disc Storage Subsystem RDC-930		40KC Words	Computer Word	18 Bit Word
Processor Interrupt Unit PIU-930		28.8KC Words	Computer Word	18 Bit Word

3. DATANET-30 PROCESSOR-DETAILED DESCRIPTION

FUNCTIONAL SEQUENCE

The normal flow of data occurs as shown below. The program periodically halts to allow the scan instruction to take bits from the bit buffers to form characters in memory. When a character is formed, it is transferred over to another area of memory where the program accumulates characters into words. The words are accumulated into blocks of variable lengths and then transferred to the disc storage unit, where the queue, journal, intercept and in-transit storage areas are established under program control.

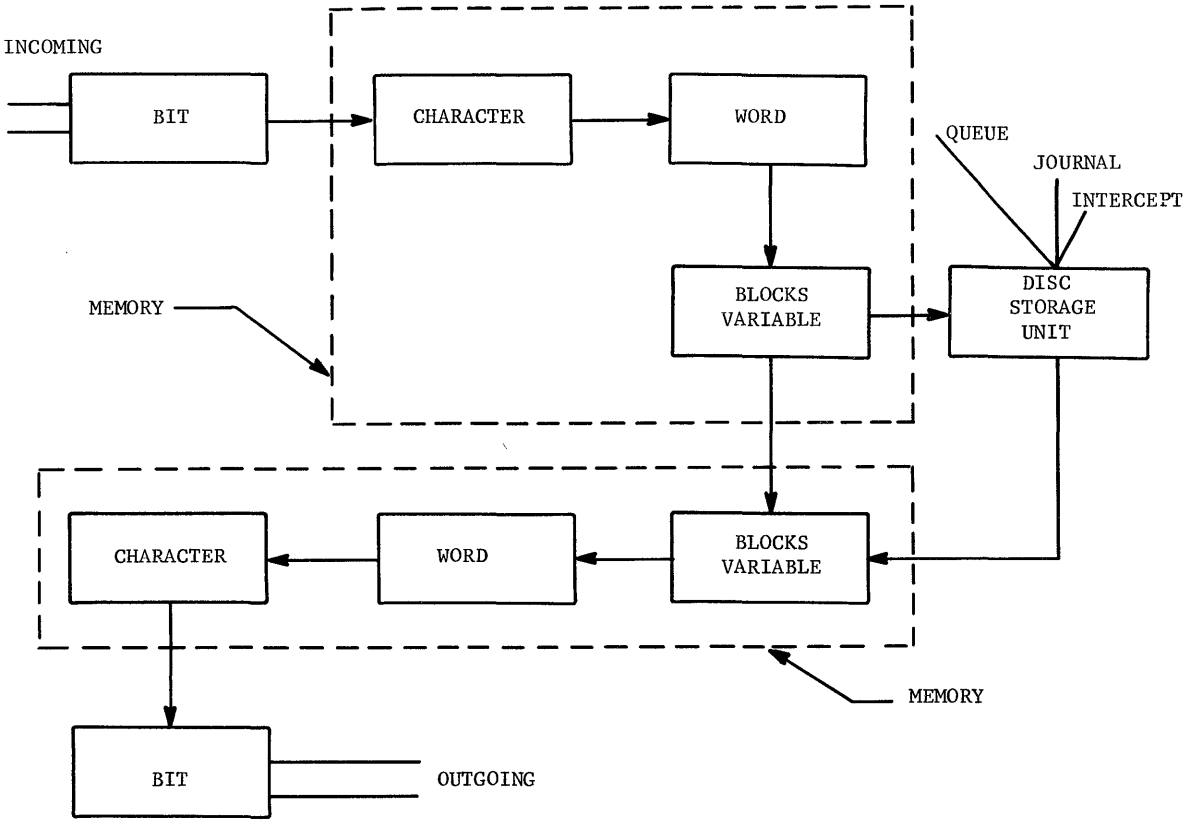


Figure 33. Data Flow Functional Block Diagram

Upon receipt of the message header, the program determines the destination, which outgoing line is to be used for retransmitting the message, and whether or not there is a queue for that line. If the line is available and there is no queue, the DATANET-30 can start transmitting the message

to the destination before the "end-of-message" is received. If a line is not immediately available, the message is placed in queue storage to be transmitted in queue sequence.

The same basic process occurs for the character and word buffers.

BLOCK DIAGRAM

The simplified block diagram shows the main paths for the flow of data. Data is moved over each path on an 18 bit parallel bus logic arrangement. For some instructions, data will be moved over several paths, with data flowing on only one path at a time. An example of this is transferring data from the B register to memory. The contents of B go to the Y register, straight through the arithmetic unit to the Z drivers, and then to memory.

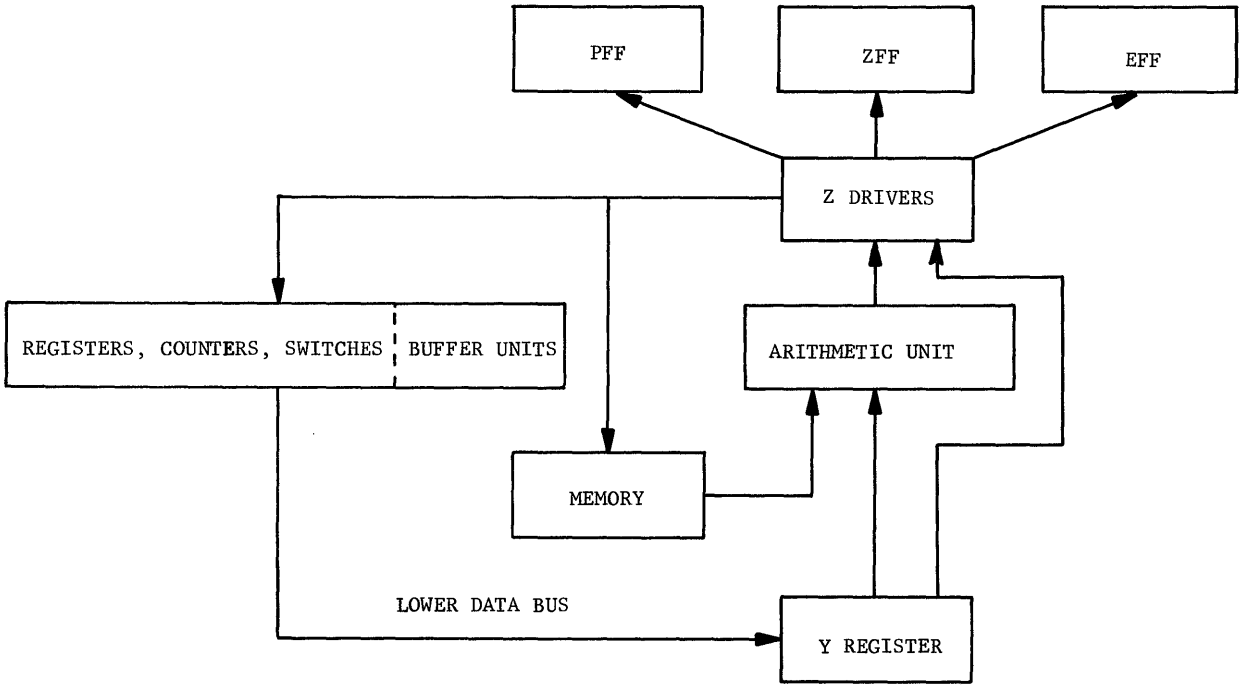


Figure 34. Simplified Block Diagram

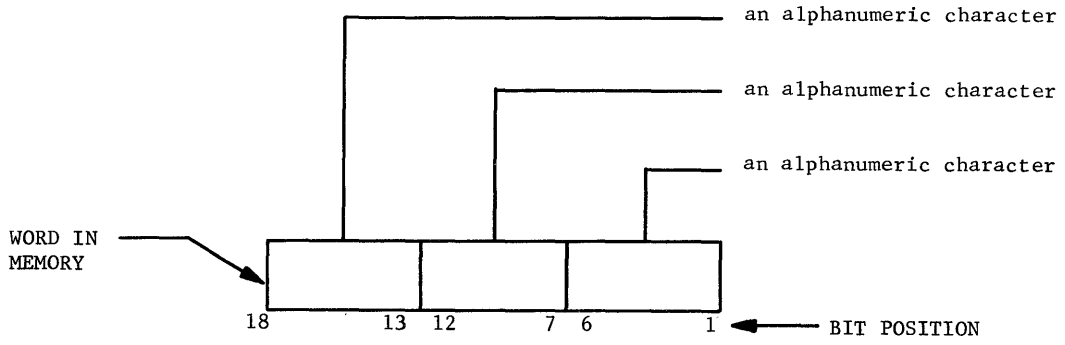
Other instructions, however, can cause data to flow over "parallel" paths at the same time. For example, performing the logical operation of combining the contents of the B register with a word in memory and storing the result in the B register will result in the following: The contents of the B register go to the Y register and on to the arithmetic unit. At the same time, the contents of the memory location go to the arithmetic unit. The logical operation is performed on the two words, the result goes to Z drivers; and is then placed in the B register in accordance with the program.

A novel and extremely effective feature are the Branch Flip-Flops (BFF). After the data has been processed by the arithmetic unit, it is sent to the Z drivers which are a common data distribution center for all data coming from the arithmetic unit and going to a working register, memory, control unit, or an output channel. Since the results of instructions go through the Z drivers on the way to their destinations, this is a point which is common to the result of every instruction. The branch flip-flops record whether the result was zero or non-zero, even or odd, plus or minus. This provides simple tests for equality, or for the end of a loop process. The branch flip-flops are not limited to these uses, and can be used with powerful effect.

REPRESENTATION OF INFORMATION IN MEMORY

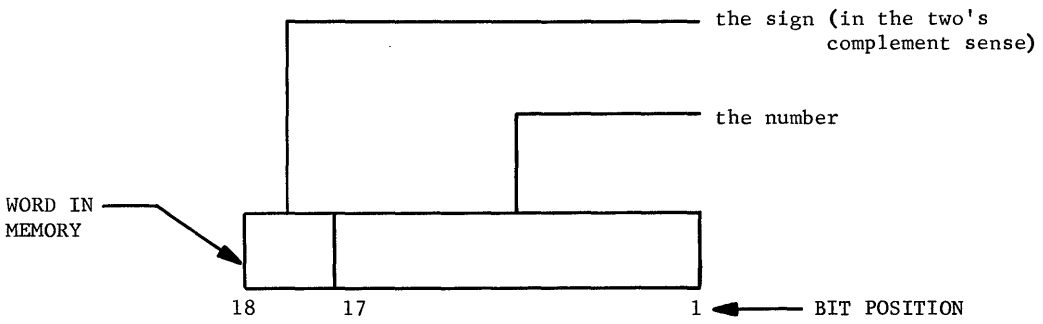
Alphanumeric Data Words

Each DATANET-30 word can contain three six-bit alphanumeric characters. The 64 possible bit combinations can be assigned to 64 symbols in any manner desired, because the DATANET-30 does not use alphanumeric data as such. Therefore, other system conditions (e.g., the character set of the computer, if there is one in the system) will determine the actual bit pattern-to-symbol assignment. An alphanumeric data word is formulated like this in memory:



Numeric Data Words

Numbers are represented by integers in the DATANET-30. Negative numbers are represented in the two's complement form. The DATANET-30 utilizes two's complement arithmetic. Therefore, the high-order bit is properly thought of as the sign bit, when it is understood that the sign is a two's complement sign, not an algebraic sign. A few examples are given below to show how various numbers are represented in the DATANET-30. The bits are shown in groups merely to simplify the presentation.

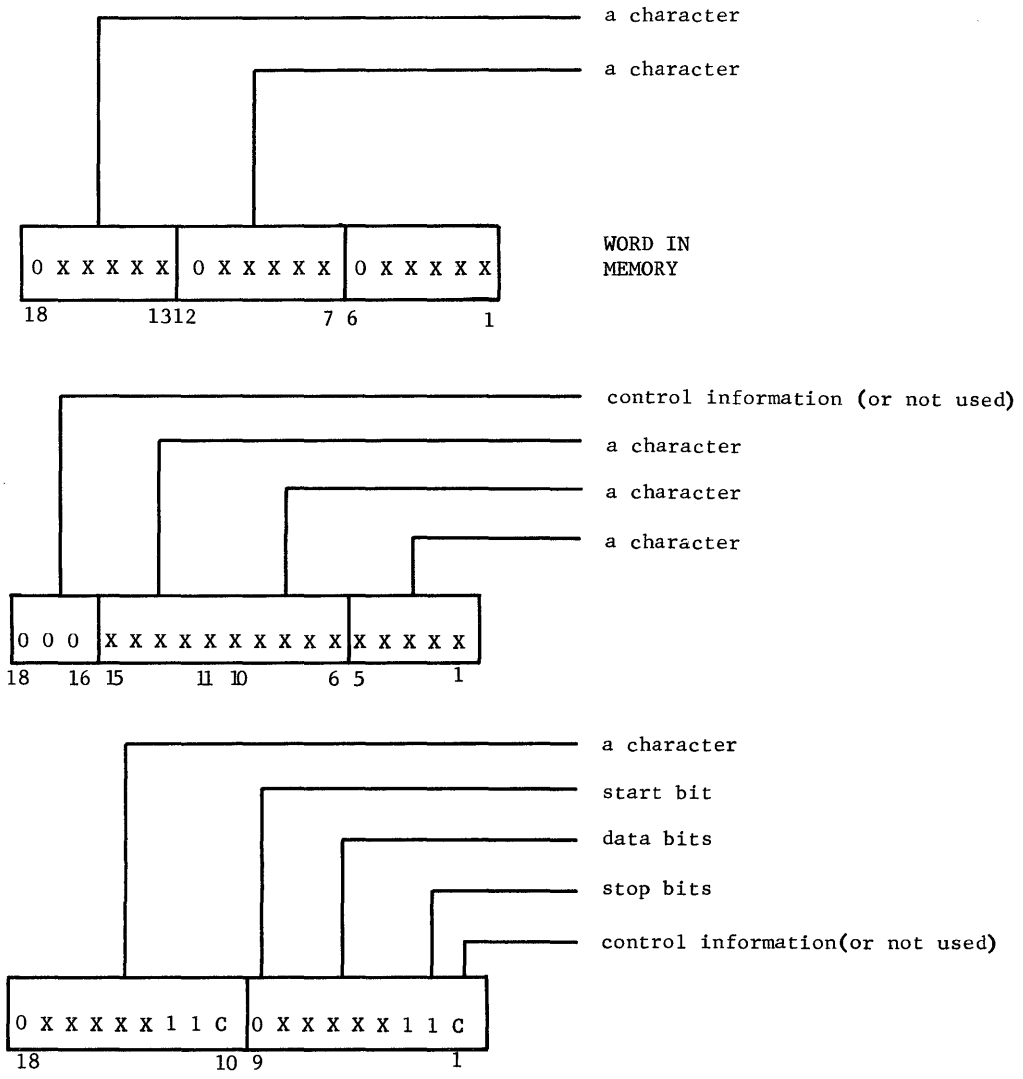


BINARY REPRESENTATION	NUMBER
0 00 000 000 000 000 000 (18 … 1)	0 (negative zero is not possible)
0 00 000 000 000 000 101 (18 … 1)	+5
1 11 111 111 111 111 011 (18 … 1)	-5
1 11 111 111 111 111 111 (18 … 1)	-1
1 00 000 000 000 000 000 (18 … 1)	-131,072 (the largest negative number)
0 11 111 111 111 111 111 (18 … 1)	+131,071 (the largest positive number)

Special Data Words

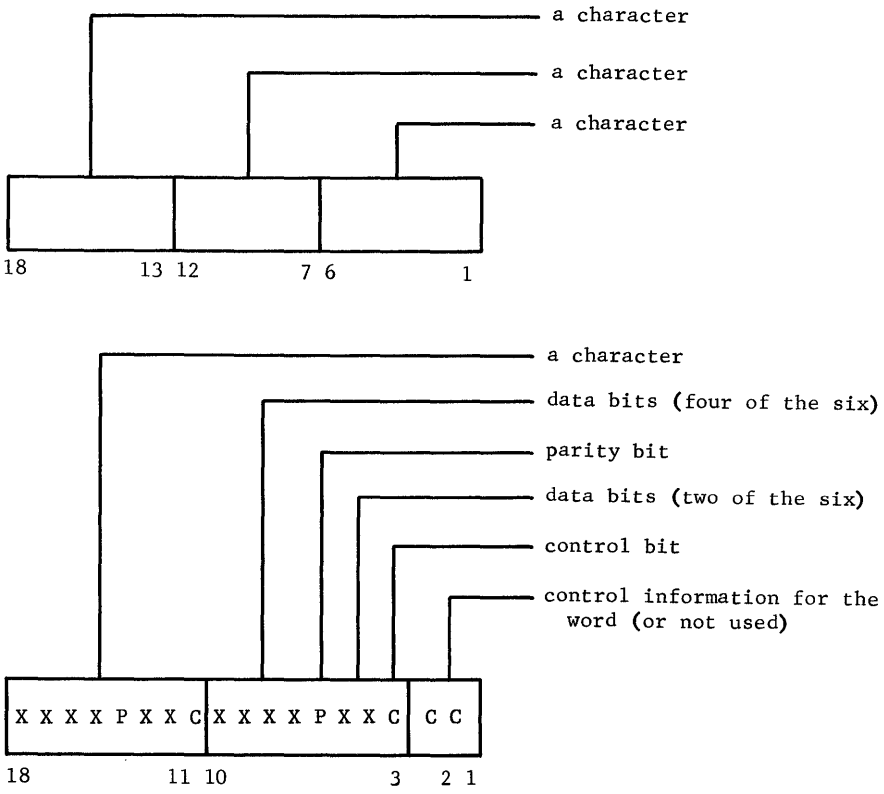
Some examples of special data words and their representation in memory are given below. These examples are intended to show a way of representing the data; other representations are possible.

Characters (five-level Teletype) could be represented in memory in the following ways (and more) with the choice depending on the particular application.



Eight-level Teletype characters can be stored conveniently in memory as six-bit characters because the DATANET-30 has special instructions to facilitate stripping off and checking the parity and control bits when a character is received and generation and insertion of parity and

control bits when a character is to be transmitted. If desired for some applications, two eight-level characters could be stored in a word as eight-bit characters including the parity and control bits.



Instruction Word Format

There are two main groups of instructions:

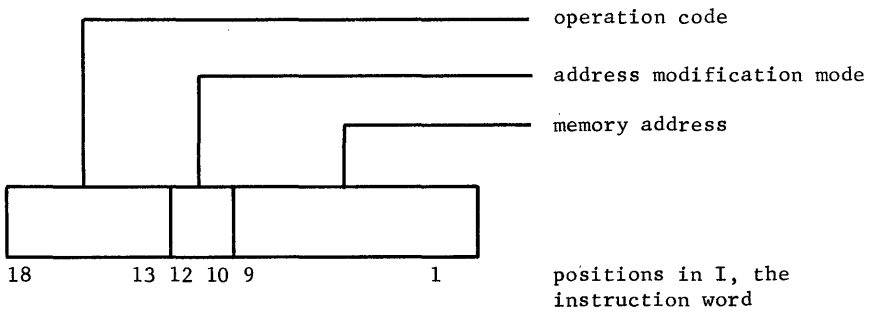
1. Those for which the low-order bits specify a memory address, and which may be subject to address modification.

2. Those for which the low-order bits contain information to be used by the instruction.

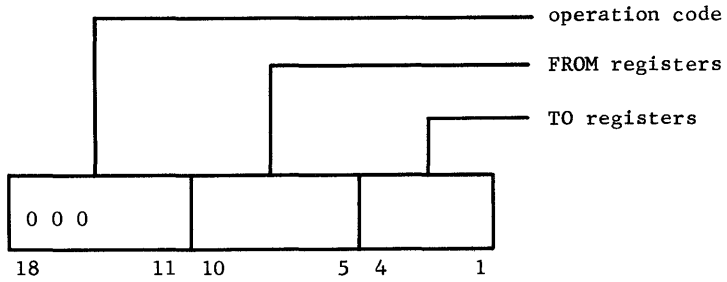
The second group is called "general" instructions and may be recognized by the fact that the three high-order bits, I (16-18), are all zeros. (When expressed in octal notation, the general instructions start with a 0.)

There is one format for the "non-general" instructions and three formats for the "general" instructions (one for register transfer instructions, one for status line and function driver instructions, and one for C counter instructions).

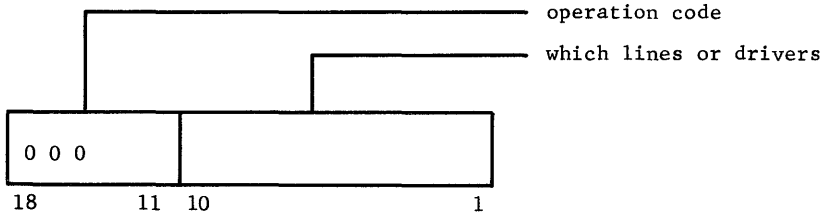
The "non-general" instructions have three fields:



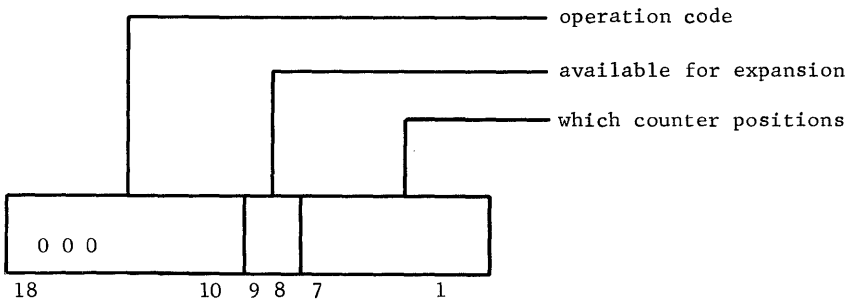
The register transfer instructions have three fields:



The status line and function driver instructions have two fields:



The C counter instructions have two fields plus some bits which are available for expanding the size of the C counter:



DETAILED BLOCK DIAGRAM

The detailed block diagram shows many more data paths of the data communications processor including data paths for the memory unit, the buffer selector, and the controller selector. In general, data flows from one or more registers to the lower data bus, through the Y register to the arithmetic unit, to the Z drivers, and then to one or more of the registers connected to the upper data bus. As illustrated below, data may also flow from the memory to the arithmetic unit at the same time that data is coming from the Y register.

Data coming from a working register, going to a transmit data line under program control, flows from the working register to the lower data bus into the Y register. From the Y register the data flows through the arithmetic unit and the Z drivers onto the upper data bus, where it is then distributed to the buffer selector. The buffer selector then routes the data to the proper output channel.

Data being received from a specified remote terminal is temporarily stored in a receive channel buffer. The buffer selector then routes the data from the receive channel through the receive data lines to the lower data bus where it is then sent to the Y register. From the Y register the data is sent through the arithmetic unit to the Z drivers where it is then distributed to the proper working register under program control.

The flow of data to and from the controller selector follows the same paths as for the buffer selector, with the exception that data going to a high speed peripheral comes from memory and data coming from a high speed peripheral is put into memory without first going through a working register. Data flows to and from the controller selector under automatic control of the DATANET-30 circuitry.

The register transfer instructions, a major class of instructions, permit any combination of up to six (specific) registers to be combined in the Y register, to be manipulated in some selected manner, and then have the result put in any combination of up to four (specific) registers. Further details of the register transfer instructions are given in the instruction repertoire description but note that the general data flow pattern still applies: data flows to the Y register, through the arithmetic unit, to the Z drivers, and then to the destination(s).

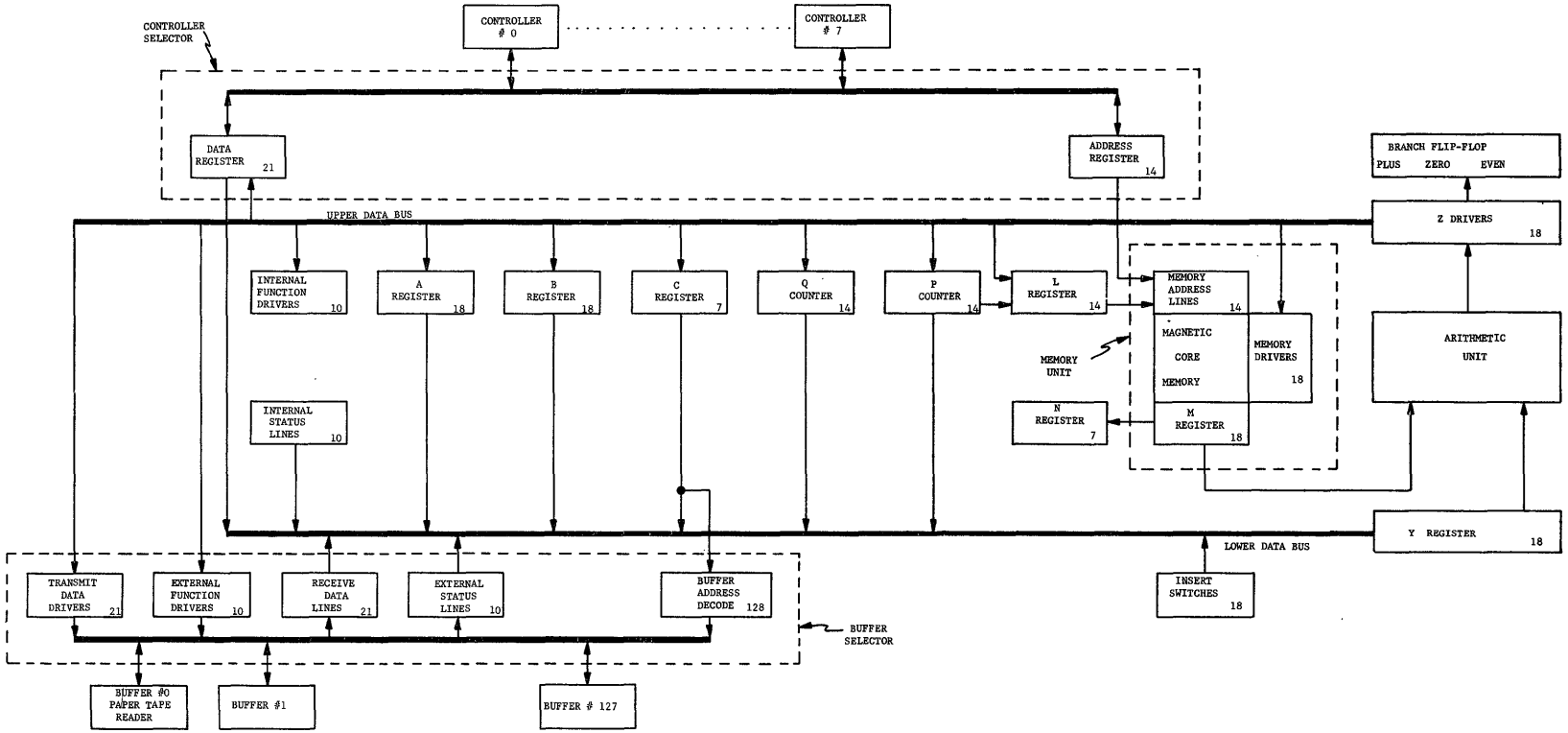


Figure 35. Detailed Block Diagram DATANET-30

Description of Blocks

The following is a brief description of each of the registers on the block diagram. Certain conventions are followed. These are:

First Item:	The size of the register.
Second Item:	The abbreviation for the name of the register (no abb. means no abbreviation is used).
Third Item:	A or N, to indicate that the register is accessible (A) or is not directly accessible (N) to the program.

A Register (18 bits, A, A)

B Register (18 bits, B, A)

The A and B registers are the principal working registers of the DATANET-30. They are identical and have identical functions and instructions except for the parity network, which is connected to just the B register.

C Register (7 bits, C, A)

The C register is used to access a specific input/output channel of the buffer selector. This is used both for selection of a particular buffer and for selection of a particular word in memory. In addition, C can be used as a normal index register when indirect addressing is used.

L Register (15 bits, L, N)

The L register contains the address of the next memory location to be accessed by the data communications processor.

N Register (7 bits, N, N)

The N register is used to facilitate the instruction decoding process.

P Counter (15 bits, P, A)

The P counter contains the address of the next instruction to be executed.

Q Counter (14 bits, Q, A)

The Q counter serves as the elapsed time clock.

Y Register (18 bits, Y, N)

The Y register is used to form and hold the intermediate operand for an instruction.

Z Drivers (18 bits, Z, N)

The Z drivers are a common data distribution center for all data coming from the arithmetic unit and going to a working register, memory, control unit, or an input/output channel.

Arithmetic Unit (18 bits, no abb., N)

The arithmetic unit performs the following functions on the contents of Y and/or M and puts the result in the Z drivers.

Binary Addition
Logical "AND"
Logical "OR"
Logical "EXCLUSIVE OR"
Shift left, right, circulate, etc.
Bit change
Scan
Other misc. operations as required, i.e., address modification

Branch Flip-Flops (3FF, BFF's, A)

The plus, zero and even flip-flops are connected to the Z drivers. These three flip-flops are set at the completion of every non-branch instruction and will reflect the branch conditions of any data passing through the Z drivers. The Plus Flip-Flop (PFF) stores the status of the high order bit of the result. The Zero Flip-Flop (ZFF) stores the status of the entire result. The Even Flip-Flop (EFF) stores the status of the low order bit of the result. The result of an operation is available for test on the next instruction.

Plus Flip-Flop (1 bit, PFF, A)

The PFF records (for testing) the condition of Z(18) at the end of an instruction. If Z(18) was zero, the PFF would be plus; but if Z(18) was one, the PFF would be minus. The notation Z(18) refers to bit position 18 of Z, i.e., the high order position of Z.

Zero Flip-Flop (1 bit, ZFF, A)

The ZFF records (for testing) the condition of Z at the end of an instruction. If all of the Z drivers were zero, the ZFF would be zero; but if any of the Z drivers were non-zero, the ZFF would be non-zero.

Even Flip-Flop (1 bit, EFF, A)

The EFF records (for testing) the condition of Z(1) at the end of an instruction. If Z(1) was zero, the EFF would be even; but if Z(1) was one, the EFF would be odd.

Insert Switches (18 switches, S, A)

The switches are located on the control console and are described in the discussion of the control console. They can be gated in under program control.

Internal Function Drivers (10 drivers, IFD, A)

These drivers can activate special control functions.

Internal Status Lines (10 lines, ISL, A)

These lines are used to test the status of various special conditions.

THE MEMORY UNIT

M Register (18 bits, no abb., N)

The M register is the memory output register. References to M in many places in this manual refer to the contents of a memory location, which is actually made available in the M register.

Memory Drivers (18 drivers, no abb., N)

The memory drivers are used to write a new word into the memory and to regenerate a word when it is read out of the memory.

Memory Address Lines (15 lines, no abb., N)

These contain the address of the memory location being accessed.

THE BUFFER SELECTOR

Receive Data Lines (21 lines, R, A)

These lines are used to receive data from a buffer channel.

Transmit Data Drivers (21 drivers, T, A)

These drivers are used to send data to a buffer channel.

External Function Drivers (10 drivers, EFD, A)

These drivers are used to send control signals to a buffer channel. The function of each driver depends on the particular type of buffer.

External Status Lines (10 lines, ESL, A)

These lines are used to test various conditions in a buffer channel. The condition tested by each line depends on the particular buffer.

Buffer Address Decode (128, N)

This unit decodes the C register into a 1 out of 128 signal to select the desired buffer address.

THE CONTROLLER SELECTOR

Data Register (21 bits, no abb., N)

The controller selector data register contains the data being transferred between the controller selector and the data communications processor.

Address Register (15 bits, no abb., N)

The controller selector address register contains the address of the next memory location to be accessed by the controller selector.

PARITY NETWORK (21 bits, no abb., N)

Although it is not shown on the block diagram (for simplicity), there is a parity network in the data communication processor. There are two outputs from the parity network, one for character parity and one for word parity. Either output may be tested to check the data. The appropriate output is automatically sent to a buffer channel when information is transmitted.

The parity networks are attached to the B register and consist of a word parity network and a character parity network. Each time a word is brought into the B register, the word parity network will generate correct parity on it. At the same time proper character parity will be generated on bits 1-6 of the B register. The input to the word parity network consists of the 18 bits of the B register, the control bit 1 and control bit 2 flip-flops. The output of the word parity network is bit 21 and is used with the word buffer and computer interface units. The inputs to the character parity network are bits 1-6 of the B register and the control bit 1 and 2 flip-flops. The character parity is used almost exclusively for generating correct parity on 8 level Teletype characters.

HARDWARE LOAD AND PAPER TAPE READER

The DATANET-30 has as standard equipment a 300 cps photoelectric paper tape reader and a bin to contain a 300 foot loop of paper tape. The hardware load function, when initiated, will search the tape for a "begin hardware-load" character, and then load the memory with data as specified by the characters punched in the paper tape. An "end hardware-load" character will automatically transfer control to the program.

With this function the hardware can selectively load data into the DATANET-30 memory. This is used to load programs initially, as well as to reload programs on an error condition. It is also used to load diagnostic programs for maintenance.

This function may be initiated in one of several ways.

1. Manually, by pressing a push button switch on the maintenance panel.
2. The Q counter counting down past zero to the hardware load value.
3. Under program control.

Paper tape may be read under program control in two modes, continuous mode at 300 cps or step mode up to 50 cps. Five to eight-level tape may be read in the unit, but normally only eight-level tape will be used. The paper tape reader is always buffer selector address zero.

Hardware Scan

Hardware scan is a special purpose communication oriented instruction. It is designed to greatly reduce the amount of real time needed to service low speed communication lines attached to bit buffer channels. This is accomplished with hardware which does the same things as a group of instructions which check for flags, receive bits for a character, and transmit bits for a character. Hardware scan requires 3 word times to service a full duplex line.

After the channel number of the first line to service has been placed in the C counter, the program initiates the hardware scan instruction. When the hardware scan process is finished, the DATANET-30 executes the instruction immediately following. The program must examine, at a character rate, the hardware scan's transmit character flags and receive character flags, take new characters as necessary, and reset the appropriate character flags.

The hardware scan instruction is a unique feature of the DATANET-30 hardware and adds significant value and higher performance with minimum equipment.

ELAPSED TIME CLOCK

The elapsed time clock (Q counter) can be loaded or read out under program control. The Q counter is decremented by one each word time, and thus serves as a word-time counter.

The Q counter has three primary functions:

1. To interrupt the program when a given amount of time has passed and transfer control to another part of the program (the part which services the input/output on a regular basis). This is accomplished by loading Q with a number; the interrupt will occur when Q counts down to zero. The number is chosen to give the desired amount of elapsed real time.

2. To serve as a "dead man" switch in conjunction with hardware load. If Q is not reloaded by the program interrupt instructions, Q will continue to count down for a given number of additional word times and then a hardware load will automatically be initiated. This is a method of detecting fault conditions in the operating program and automatically initiating a restart.

3. To measure the amount of "real time" used since the last time Q was changed. Q can be used in this way to provide an inexpensive real time clock, with the appropriate programming.

LINE SERVICE RATE

The service rate can be defined as the cycle time for the operation of the receive or transmit flag of the bit buffer.

When servicing transmission lines on serial bit stream basis there are certain timing considerations which must be taken into account. In the table below is shown the service rate for the six most common transmission speeds.

Bits per second	Service Rate
45	22.2 milliseconds
50	20.0 milliseconds
56.25	17.7 milliseconds
75	13.3 milliseconds
110	9.09 milliseconds
150	6.67 milliseconds

When scanning the bit buffers, the program initiates scanning at a rate of slightly faster than the service rate. For a 45 bit/second transmission line having a service rate of 22.2 milliseconds, the line would be scanned approximately every 21.0 milliseconds to insure that any speed variations in the remote terminal will not result in data lost at the DATANET-30.

BASIC PROGRAM CYCLE

A real time program response time to certain events must be very small. The communications programs can be divided into the following sequence of events.

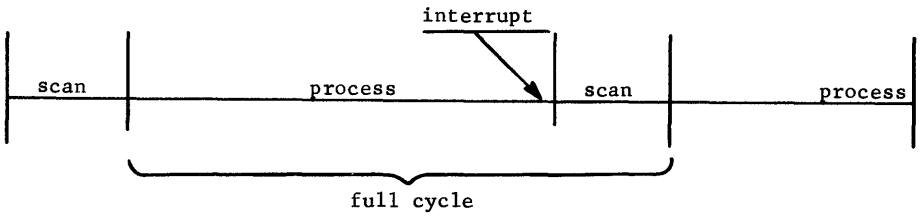
1. Receive bits
2. Assemble bits into characters
3. Assemble characters into words
4. Assemble words into blocks
5. Assemble blocks into messages
6. Assign message routing

The program to do this is divided into two basic cycles.

1. Scan cycle (hardware scan) - when each buffer is sampled within a bit time and the bit present is moved from the buffer into an assembly area.

2. Processing cycle - when all the rest of the processing to be done by the program must be accomplished.

Since a basic premise of the DATANET-30 is to service each line in time to receive (or transmit) each bit within rigid time limitations, both the scan cycle and the process cycle must be completed within a certain amount of time.



The time will vary with the line service rate required by the remote terminals. One full cycle must therefore be completed at a rate slightly faster than the fastest service rate. In order to do

this, processing must be interrupted to allow the hardware scan instruction to service the lines (3 word times per line). The interruption must be timed so that from the end of one scan cycle to the end of the next scan cycle, the total elapsed time is less than one bit time.

Although the above only discussed the bit time for serial bit stream transmission buffers, the scanning and processing of character and word buffers follow the same rules.

ADDRESSING MEMORY

There are six possible addressing modes on the DATANET-30. These modes were specially designed to solve the particular memory addressing problems involved in handling communication lines.

Direct Access to a Program Bank

The instruction address specifies a memory location within the 1024 memory locations (program bank) in which an instruction is located. Two numbers, 0-1, are in the mode number because the instruction address is really only 9 bits (512 locations), but the size of a program bank is extended to 1024 by using the low order bit of the addressing mode as part of the instruction address. This mode is used for branching to instructions which are in the same subdivision of the program, or, for accessing constants or working storage not needed in other program banks.

Direct Access to the Common Data Bank

The instruction address specifies a location in the common data bank, the first 512 memory locations. The location of an instruction is not significant. This mode is used for constants, variables, and subroutine linkages which are common to parts of the program located in more than one program bank. Any address in memory has direct access to these locations.

Direct Access to a Channel Table

The instruction address specifies the starting location of a channel table, i.e., an array of words with one word for each input/output channel. The true starting address must be modulo 16. When the instruction is converted from its symbolic form into binary by the assembler, the true address is divided by 16 and becomes the instruction address. When the instruction is executed, the DATANET-30 effectively multiplies the instruction address by 16 to recover the true starting address of the array. The contents of the C register select the word in the array which corresponds to the channel currently specified by the C register. This mode is used for various items which exist for each channel, such as channel type, number of characters received so far, where the next word is to be stored for a received message, etc.

Indirect Addressing

The remaining modes use indirect addressing to specify the actual location. With indirect addressing, some location, such as ALPHA, is specified by an instruction and the actual location used is determined by the contents of ALPHA. Ordinary indexing is possible when using indirect addressing.

Indirect Access from a Program Bank

This mode is similar to mode 0-1, except that the contents of the specified location determine the actual location to use. This mode is used to specify the location of the next part of the program, when a shift to another program bank is desired.

Indirect Access from the Common Data Bank

This mode is similar to mode 3, except that the contents of the specified location determine the actual location to use. This mode is used for indirectly accessing constants and variables which are common to parts of the program located in more than one program bank, and for returning from subroutines.

Indirect Access from a Channel Table

This mode is similar to mode 3, except that the contents of the specified location determine the actual location to use. This mode is used to pick up and store words which contain part of a message.

INTERRUPT INTERFACE

The Interrupt Interface feature of the DATANET-30 allows data transfer directly between memory and peripheral equipment or another DATANET-30. The data is transferred by interrupting the DATANET-30 one word-time for each data transfer. One DATANET-30 word is transferred to or from memory. The buffer modules and peripheral equipment that use the interrupt interface are as follows:

Option Module	To	Cycle No. Assigned
1. Controller Selector Unit (CSU931)	Disc Storage Unit Magnetic Tape Unit High Speed Printer	1 and 3
2. Common Peripheral Channel (CPC930)	Disc Storage Unit Magnetic Tape Unit High Speed Printer Card Reader Card Punch	X,X X X X X
3. Processor Interrupt Unit (PIU930)	A DATANET-30	2
4. Removable Disc Unit (RDU930)	Removable Disc Storage Controller	X,X

The interrupt interface provides for memory interrupt cycles that are assigned to the option modules listed above. The interrupt interface provides groups of 5 memory cycles, numbered 1,2,3,4&5. A certain numbered cycle can be individually assigned to an option module, and when a memory cycle is needed to transfer data, the assigned cycle can be obtained without interference.

When considering the options to be connected to the DATANET-30, the number of memory cycles to be used must also be considered. Since only 5 cycles are available for assignment, the options using the interrupt interface cannot exceed 5. However, this will not normally be a problem because of the types of options that use the interrupt cycles.

Allocation of Cycles

Allocation of cycles is based on requirements for frequency of memory interrupts. The DATANET-30 has a maximum total throughput limit of 144,000 18-bit words per second. Since DATANET-30 cycles will be designated in groups of 5 cycles, each device on interrupt utilizing one of the cycles can have a word input/output frequency no greater than one-fifth of the maximum throughput, or 28,800 words per second.

Generally, devices with transfer rates less than 28,800 words per second will be allocated a single cycle of the group of 5 cycles. Devices with transfer rates higher than 28,800 words per second will be allocated correspondingly more than one cycle out of 5 cycles in a group.

The CSU (Controller Selector Unit), for example, has a maximum transfer rate of 57,600 words per second. It will, therefore, be allocated 2 cycles out of the group of 5. In addition, the CSU is allocated a definite 2 cycles out of the 5; namely, cycles 1 and 3.

Some devices may be assigned definite cycles within the group while others may be required to have the cycle(s) plug selectable. In some instances, more than one mechanism requiring data interrupts may be assigned the same interrupt cycle. In this case, the device interrupt module receives the burden of allocating subpriorities to the mechanisms.

The DATANET-30 interrupt scheme is so designed that all 5 cycles of every group can be used for data interrupts. Even though subpriorities may be assigned to multiple mechanisms on a single interrupt cycle, all devices on data interrupt will be guaranteed their assigned cycles since no cycle will be assigned to more than one device. When multiple mechanisms are used, it can be assumed that these multiple mechanisms make up a single device.

CONTROL CONSOLE

The control console is designed to serve both operator and maintenance functions. The operator functions are at a minimum, however. The DATANET-30 is designed to operate without direct operator control via the control panel. Once the program is running, most control functions will be initiated from the supervisory position keyboard/printer.

The control panel provides means for the supervisor to start the program and check that the operate/maintenance, count P, count Q, Halt, mode select and buzzer switches are all in the correct position. The start-up sequence is: power on, check all the above switches and press the manual load button. This enters the program from the paper tape reader. When the paper tape reader stops, the program is running and all other control functions will be initiated from the supervisory position.

The other buttons and switches are not normally used by the supervisor. They are for maintenance, trouble shooting and program debugging purposes.

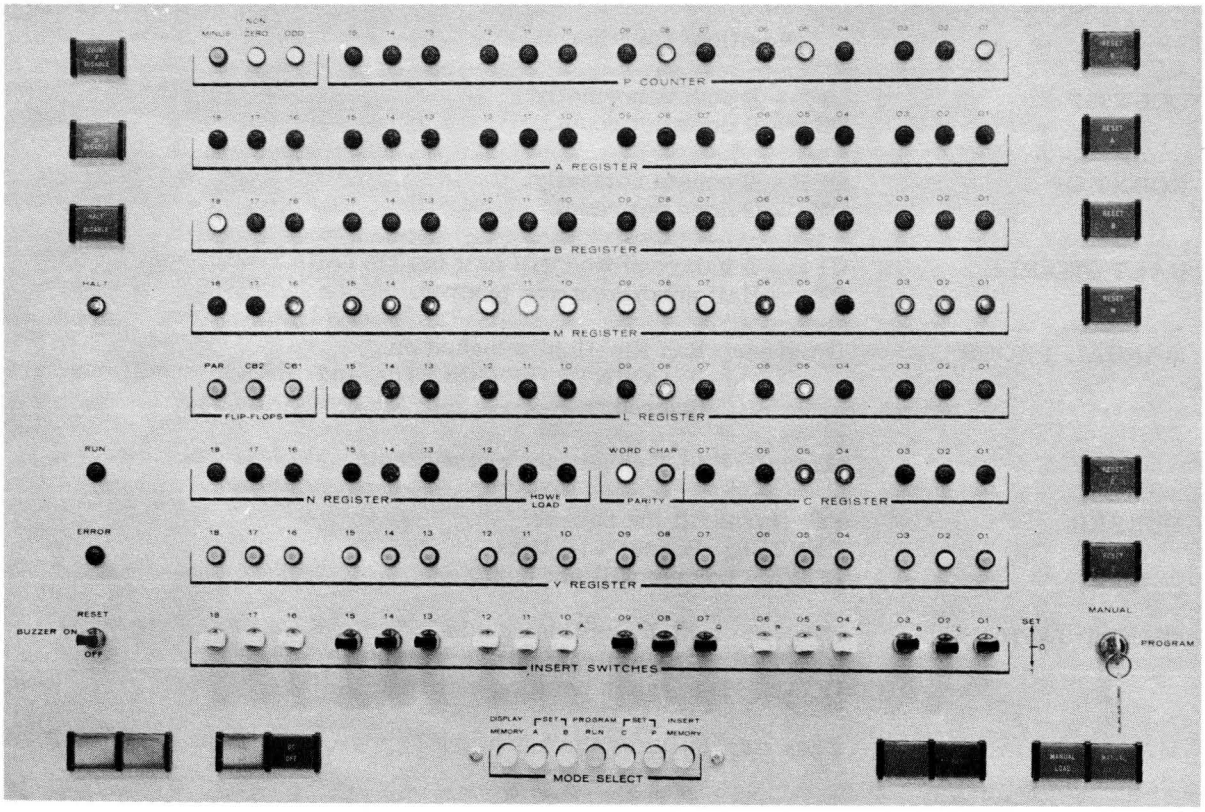


Figure 36. The Control Console

The following is a brief explanation of the more important functions of the switches and lights:

The contents of the A, B, C, P registers, and memory may be modified directly by the "insert" switches. The insert switches modify the register selected by the mode select switch.

The lights display the contents of the various registers and flip-flops as indicated. The P counter specifies the memory location to be displayed next in the M register. The P counter is automatically incremented and sequential locations in memory may be displayed by pressing the single cycle button.

DESCRIPTION OF CONTROL CONSOLE SWITCHES

Switch Name	Position/Function
COUNT P	OFF - P counts normally. ON - P does not count.
COUNT Q	OFF - Q counts normally. ON - Q does not count.
HALT DISABLE	OFF - A halt condition will halt the DATANET-30. ON - Halt conditions are ignored.
MANUAL/PROGRAM	Program: Run flip-flop is locked on. P COUNTS, Q COUNTS and HALT conditions are ignored. Manual: HALT conditions cause a halt.
BUZZER	UP: turns off the buzzer. CENTER: Buzzer will buzz. DOWN: Buzzer will not buzz.
INSERT SWITCHES	UP: The switch position equals 1. CENTER: The switch position equals 0. DOWN: The switch position equals 1.
MANUAL LOAD	Pressed: Initiates the hardware load process, if the mode selected is program run.
RUN	Pressed: Starts the DATANET-30 running continuously, if the mode selected is program run, display memory, or insert memory.
SINGLE CYCLE	Pressed: Halts the DATANET-30. When already halted, one instruction or action will be executed each time the the switch is pressed. The action depends on the mode selected.
MANUAL RESET	Pressed: Resets all registers, counters and flip-flops.
MODE SELECT	Set A: The insert switches can set A register. Set B: The insert switches can set B register. Set C: The insert switches can set C register. Program Run: Instructions are executed in the normal manner. Set P: The insert switches can set P. Display Memory: The contents of the location specified by P can be displayed. The contents will be compared to the insert switches. A discrepancy will result in a halt condition.

MODE SELECT (continued)	Insert Memory:	The data in the insert switches can be stored in the memory location specified by P. After storage, the location's contents will be read out and compared to the switches. A discrepancy will result in a halt condition and will turn on the buzzer.
RESET P	Pressed:	Resets P.
RESET A	Pressed:	Resets A.
RESET B	Pressed:	Resets B.
RESET M	Pressed:	Resets M.
RESET C	Pressed:	Resets C.
RESET Y	Pressed:	Resets Y.

4. PROGRAMMING

PROGRAM PREPARATION

The principal programming tool for the DATANET-30 is an assembly program. Writing programs at the assembler language level is the fastest and most economical way to create the efficient real time programs needed.

Assembly Programs

There are two assembly programs available. One runs on a GE-200 Series computer, and the other runs on a DATANET-30. Both assembly programs can be obtained from the Computer Department Program Library. The assembly program run on a GE-200 Series computer is discussed in detail in Appendix A of CPB 1019, the DATANET-30 Programming Reference Manual. The assembly program run on a DATANET-30 is covered by CPB 1074, DATANET-30 Assembly Program Reference Manual.

The assembly program run on the DATANET-30 will accept programs written for the assembly program run on the GE-200 Series computer, thus providing compatibility for assembling DATANET-30 source programs.

The DATANET-30 assembly program allows the programmer to work with the individual instructions of the DATANET-30. The programmer employs symbolic notation rather than the absolute code of the DATANET-30. The symbolic notation selected to designate each instruction is carefully chosen for high mnemonic value. For example, AAM is the mnemonic for ADD A TO MEMORY. The assembler translates the mnemonics into the absolute codes used by the DATANET-30.

Memory addresses may be assigned by using decimal notation or by using symbolic notation chosen for maximum convenience and mnemonic value for the particular program or programmer. For example, WORDS might be used to designate the memory location which contains the number of words in a message. DATANET-30 general assembly programming also provides for the assignment of addresses relative to some starting point. This feature can also be used to automatically calculate table sizes.

The assembler selects the proper addressing mode for the programmer, based on the location of the instruction, the location of the operand, whether or not the instruction is to use one of the indirect addressing modes and whether or not the operand is a channel table.

In addition to the mnemonics for the instructions, DATANET-30 assembly programming uses pseudo-instructions which are also assigned mnemonics. These pseudo-instructions are used

to control the DATANET-30 assembly program during the assembly process and to introduce various forms of constants in the program. For example, DEC is a pseudo-instruction used to provide a constant in the program, where the programmer wishes to use decimal notation in writing the constant. The assembler will convert the decimal constant to binary. Pseudo-instructions are written in the same general form as symbolic instructions and are included in the program listing.

Programming Aids

Various programming aids are available or are being developed. These include programs to be used with the DATANET-30 assembly program as well as part of an operating program. Constant development in this area precludes listing the various aids here. Current information may be obtained from the Computer Department's Program Library.

UTILITY ROUTINES

Since the output from the DATANET-30 Assembly Program is magnetic tape (switch option) or punched cards and the input to the DATANET-30 can be punched paper tape, a conversion program is needed. A utility routine (Assembly Program 3) on the DATANET-30 Assembly Program systems tape for the GE-200 Series computer will accomplish this, producing paper tape in various formats on a free-standing paper tape unit which has the eight-level straight transfer mode. One of the formats is compatible with hardware load, so that self-loading programs can be produced. Other formats are read by paper tape loader programs. The Paper Tape Conversion (Assembly Program 3) Utility Routine can be run following the DATANET-30 Assembly Program by setting the console switches.

Diagnostics

In addition to the usual diagnostics used to troubleshoot and maintain the DATANET-30 system, real-time diagnostics are also available for incorporation into a real-time program. These real-time diagnostics permit the DATANET-30 to check itself whenever small intervals of otherwise unused time occur in a program. In addition, real-time diagnostics can be used in a multi-DATANET-30 system so that the DATANET-30 systems can check each other. With real-time checking of the system, and the automatic restart capability of the DATANET-30, notification of apparent or real failures can be given to a supervisory terminal and the program can continue to run.

System Programming Considerations

The relative importance assigned to the system factors are:

1. operating time,
2. memory utilization, and
3. coding effort.

For real-time applications, item (1) is of paramount importance because system capability is strongly dependent upon the program's efficiency of operating time. Item (2) is also important since system performance depends strongly on the amount of memory available for data storage.

Item (3) is of much less importance because the amount of coding in each program is small and because any given installation will have at most a few programs.

For most systems, the system capability will be inversely proportional to the amount of time required to service a line, i.e., if the time per line can be reduced 20 per cent with more efficient programming, then the system has the capability to handle 20 per cent more lines with the same hardware configuration. Another way of looking at the importance of the operating time used by a program is this: Presume that system requirements specify that 10 ms are available in which to service all lines once. Then a program which requires 11 ms cannot be used unless the 10 ms specification is changed, the number of lines reduced, or the 11 ms program made more efficient. Because the amount of operating time is so important, several special features have been included in the DATANET-30 hardware to reduce the operating time. Writing the actual coding at the assembler level is the best way to utilize these special features and attain the necessary efficiency.

The amount of memory used for the instructions and tables in a program will determine how much memory is left over for data storage. Decreasing the program memory required will increase the data storage memory available and help smooth out the peaks in system traffic, thus improving the store and forward performance. In addition, for those applications which permit giving a busy signal, more data storage memory will delay or possibly eliminate the point at which a busy signal will have to be given because of a full memory. For those applications which do not permit giving a busy signal, decreasing the memory required for the program will decrease the total amount of memory needed in the system.

The actual coding effort for a system generally will be a small part of the cost of the system because each piece of the total program is small and the total program will seldom be modified. Since each piece of the total program is used frequently, the coding cost in obtaining the program is small when compared to the operating cost of the program over its lifetime.

Message Switching Center

When operating as a message switching center, the configuration of the overall system must be considered:

1. Number and type of incoming/outgoing lines--half duplex, full duplex, etc.
2. Number of receive-only remote terminals
3. Number of stations per multipoint line
4. The speed of transmission on each line, if there are transmission speed differences in the system.
5. The handling of priority messages, if any
6. Whether or not another DATANET-30 is included in the system
7. Routing codes: multiple broadcast or single address
8. Remote station identification codes
9. Message format
10. How communication with other networks will be handled
11. Control of the system for beginning of day and end of day
12. The type of remote terminal equipment and all operating characteristics.

The above list only partially covers the considerations necessary. After the characteristics of each system have been determined, the programming can proceed.

Firm figures on the total number of lines or remote stations that can be handled simultaneously, or the number of messages per day, characters per hour or other statistics cannot be defined because of the many variables--different combinations possible--from one system to another. In general, one DATANET-30 will handle 1 million characters per hour or more. This depends upon system parameters--speed and duplexing of lines, multipoint line control, whether or not speed, code and format conversions are performed and other requirements. Each system must be analyzed and balanced to obtain maximum system performance.

Integrated Data Processing

The inclusion of a computer in the overall system permits various methods of handling incoming/outgoing messages. In one case, incoming data intended for the computer is transferred directly. In another, the incoming data is stored first in a disc storage unit and retrieved by the computer.

A system may also store data on a disc storage unit or magnetic tape and transfer it to the computer at a certain time of day for batch processing. Individual operating procedures and program requirements will necessarily be developed for each system.

INSTRUCTION REPERTOIRE

There are over 78 basic instructions in the DATANET-30 repertoire, with many variations of some of them. These are broadly classified into three groups:

A. Internal Instructions
B. Buffer Selector Instructions
C. Controller Selector Instructions

Internal Instructions

The Internal Instructions are further classified into 7 subgroups:

1. Load
2. Store
3. Arithmetic
4. Logical
5. Register Transfer
6. Branch
7. Special

In the following discussion, an M in the Operand column means that the instruction refers to a memory location. All such instructions use one of the addressing modes; therefore, no specific mention is made of the modes below. Also, provision has been made in the operation code structure for easily adding more bit change instructions for specific system requirements. I or FROM, TO means that the information to be used in executing the instruction is the bits in the low-order part of the instruction itself. For the purposes of this manual, the description of each instruction is abbreviated. A complete discussion of each instruction is in the Programmer's Reference Manual.

For brevity, the notation I (1-7) will be used for the 7 low-order bits of the instruction word. B (18) stands for the high-order bit of B. M stands for all 18 bits of the memory location; B stands for all 18 bits of the B Register; C stands for all 7 bits of the C Register. In mnemonic for an instruction, the first letter has a functional meaning as indicated in the name of each instruction. At times the discussion will refer to M as a memory location (the effective address, i.e., the memory location specified by M and the addressing mode). The word times assume that direct addressing is used; one additional word time is needed for indirect addressing. All instructions that are directly addressable are also indirectly addressable.

MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
LOAD INSTRUCTIONS			
LDA	M	2	LOAD A. The contents of M replace the contents of A. The contents of M are unchanged.
LDB	M	2	LOAD B. The contents of M replace the contents of B. The contents of M are unchanged.
LDC	M	2	LOAD C. The contents of M (1-7) replace the contents of C. The high order bits of M are ignored and M is unchanged.
LDD	M	3	LOAD DOUBLE. The contents of M replace the contents A and the contents of M+1 replace the contents of B. M must be even. M and M+1 are unchanged.
LDQ	M	2	LOAD Q. The contents of M replace the contents of Q. The contents of M are unchanged.
LDZ	M	2	LOAD Z. The contents of M is placed only in Z and the Branch Flip-Flops. M remains unchanged.
CMA	M	2	COMPLEMENT MEMORY TO A. The ones complement of the contents of M replace the contents of A. The contents of M are unchanged.
CMB	M	2	COMPLEMENT MEMORY TO B. The ones complement of the contents of M replace the contents of B. The contents of M remain unchanged.
PIC	I	1	PLACE I IN C. I (1-7) are placed in C.
STORE INSTRUCTIONS			
STA	M	2	STORE A. The contents of A replace the contents of M. The contents of A remain unchanged.
STB	M	2	STORE B. The contents of B replace the contents of M. The contents of B remain unchanged.
STC	M	2	STORE C. The contents of C are stored in M (1-7). The contents of M (8-18) are reset to Zero and C remains unchanged.

MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
STORE INSTRUCTIONS (continued)			
STD	M	3	STORE DOUBLE. The contents of A are stored in M and the contents of B are stored in M+1. M must be even. The contents of A & B are unchanged.
STZ	M	2	STORE ZERO. A zero is stored in M.
CAM	M	2	COMPLEMENT A TO MEMORY. The ones complement of the contents of A is stored in M. The contents of A remain unchanged.
CBM	M	2	COMPLEMENT B TO MEMORY. The ones complement of the contents of B is stored in M. The contents of B remain unchanged.
CMM	M	2	COMPLEMENT MEMORY TO MEMORY. The ones complement of the contents of M is stored in M, the same memory location.
ARITHMETIC INSTRUCTIONS			
AMA	M	2	ADD MEMORY TO A. The contents of M are added to the contents of A and the result is placed in A.
AMB	M	2	ADD MEMORY TO B. The contents of M are added to the contents of B and the result is placed in B.
AIC	I	1	ADD I TO C. I(1-7) are added to the contents of C and the result is placed in C.
AMD	M	3	ADD MEMORY DOUBLE. The contents of M+1 are added to the contents of B and the result is placed in B, and the contents of M and a carry from the first are added to the contents of A and the result is placed in A. M must be even. M and M+1 are unchanged.
AAM	M	2	ADD A TO MEMORY. The contents of A are added to the contents of M and the result is stored in M. A remains unchanged.
ABM	M	2	ADD B TO MEMORY. The contents of B are added to the contents of M and the result is stored in M. B remains unchanged.
ADO	M	2	ADD ONE. One is added to the contents of M and the result is stored in M.
SBO	M	2	SUBTRACT ONE. One is subtracted from the contents of M and the result is stored in M.

MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
ARITHMETIC INSTRUCTIONS (continued)			
AAZ	M	2	ADD A TO Z. The contents of A are added to the contents of M. The result in the Z drivers is placed only in the Branch Flip-Flops. A and M are unchanged.
ABZ	M	2	ADD B TO Z. The contents of B are added to the contents of M. The result in the Z drivers is placed only in the Branch Flip-Flops. B and M remain unchanged.
LOGICAL INSTRUCTIONS			
NMA	M	2	AND MEMORY TO A. A logical "AND" is performed with the contents of M and the contents of A. The result is placed in A.
NMB	M	2	AND MEMORY TO B. A logical "AND" is performed with the contents of M and the contents of B. The result is placed in B.
NAM	M	2	AND A TO MEMORY. A logical "AND" is performed with the contents of A and the contents of M. The result is stored in M.
NBM	M	2	AND B TO MEMORY. A logical "AND" is performed with the contents of B and the contents of M. The result is stored in M.
NAZ	M	2	AND A TO Z. A logical "AND" is performed on the contents of A and the contents of M. The result in the Z drivers is placed only in the Branch Flip-Flops. A and M remain unchanged.
NBZ	M	2	AND B TO Z. A logical "AND" is performed on the contents of B and the contents of M. The result in the Z drivers is placed only in the Branch Flip-Flops. B and M remain unchanged.
NCZ	I	1	AND C TO Z. A logical "AND" is performed on I (1-7) and the contents of C. The result in the Z drivers is placed only in the Branch Flip-Flops. C remains unchanged.
RMA	M	2	OR MEMORY TO A. A logical "OR" is performed with the contents of M and the contents of A. The result is placed in A.
RMB	M	2	OR MEMORY TO B. A logical "OR" is performed with the contents of M and the contents of A. The result is placed in A.

MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
LOGICAL INSTRUCTIONS (continued)			
RAM	M	2	OR A TO MEMORY. A logical "OR" is performed with the contents of A and the contents of M. The result is stored in M.
RBM	M	2	OR B TO MEMORY. A logical "OR" is performed with the contents of B and the contents of M. The result is stored in M.
XMA	M	2	EXCLUSIVE OR MEMORY TO A. A logical "EXCLUSIVE OR" is performed with the contents of M and the contents of A. The result is placed in A.
XMB	M	2	EXCLUSIVE OR MEMORY TO B. A logical "EXCLUSIVE OR" is performed with the contents of M and the contents of B. The result is placed in B.
XAM	M	2	EXCLUSIVE OR A TO MEMORY. A logical "EXCLUSIVE OR" is performed with the contents of A and the contents of M. The result is stored in M.
XBM	M	2	EXCLUSIVE OR B TO MEMORY. A logical "EXCLUSIVE OR" is performed with the contents of B and the contents of M. The result is stored in M.
XAZ	M	2	EXCLUSIVE OR A TO Z. A logical "EXCLUSIVE OR" is performed on the contents of A and M. The result in the Z drivers is placed only in the Branch Flip-Flops. A and M remain unchanged.
XBZ	M	2	EXCLUSIVE OR B TO Z. A logical "EXCLUSIVE OR" is performed on the contents of B and the contents of M. The result in the Z drivers is placed only in the Branch Flip-Flops. B and M remain unchanged.
XCZ	I	1	EXCLUSIVE OR C TO Z. A logical "EXCLUSIVE OR" is performed on I (1-7) and the contents of C. The result in Z is placed only in the Branch Flip-Flops. C remains unchanged.

REGISTER TRANSFER INSTRUCTIONS

All of the register transfer instructions use the low-order bits of the instruction to specify which registers are to be included in the FROM group and which in the TO group. The possibilities are:

FROM:
- A The A Register
- B The B Register
- C The C Counter

Q The Q Counter
R The Receive Data Lines
S The Insert Switches

TO:
A The A Register
B The B Register
C The C Counter
T The Transmit Data Lines

If R, S, or T are specified, the Control Bit 1, Control Bit 2, and Parity Flip-Flops (Internal Functions) are used for the "extra" positions, since R and T are all more than 18 bits.

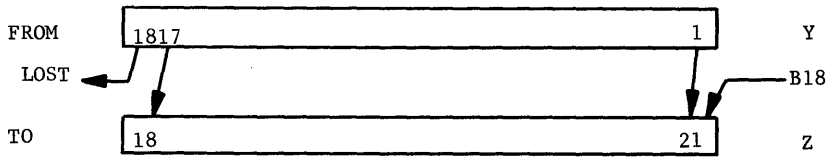
If R is specified in the FROM group, after the data is transferred, the Receive Flag and Receive Buffer are reset by an automatically generated signal activating External Function Driver Number 1 (EFD1).

If T is specified in the TO group, before the data is transferred, the Transmit Flag and Transmit Buffer are reset by an automatically generated signal activating External Function Driver Number 2 (EFD2).

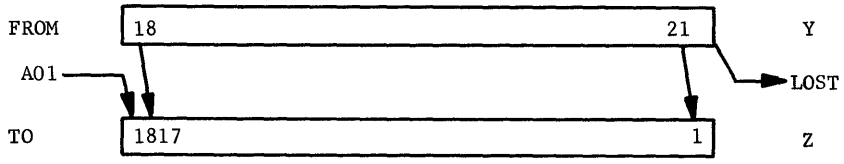
When a register transfer instruction is executed, the contents of those registers which are specified to be used as the FROM group for this instruction are logically "OR-ed" together into the Y Register. Then the data goes from Y to Z with the operation specified by the instruction being performed on the data as it goes from Y to Z. Finally the result goes from the Z drivers to all of those registers which are specified in the TO group. The Plus, Zero, and Even Flip-Flops will take on their new states in the normal manner. If no registers are specified in the FROM group, the output from the Y Register will be zero. If no registers are specified in the TO group, the only outputs are the new states of the Plus, Zero, and Even Flip-Flops. As an example, the instruction TRA AQ, BT can be represented by the equations B=T=(A OR Q).

MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
TRA	FROM, TO	1	TRANSFER. In going from Y to A, no change is made in the data.
TRC	FROM, TO	1	TRANSFER COMPLEMENT. In going from Y to Z, the data is changed into its ones complement.
SL1	FROM, TO	1	SHIFT LEFT ONE. In going from Y to Z, the data is shifted left one position. The high-order bit is lost and a zero goes into the low-order position.
SR1	FROM, TO	1	SHIFT RIGHT ONE. In going from Y to Z, the data is shifted right one position. The low-order bit is lost and a zero goes into the high-order position.
SL6	FROM, TO	1	SHIFT LEFT SIX. In going from Y to Z, the data is shifted left six positions. The six high-order bits are lost and zeros go into the six low-order positions.

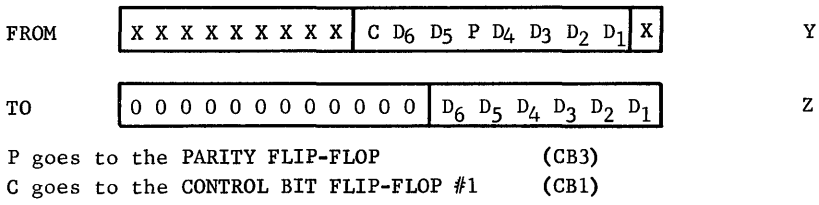
MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
SR6	FROM, TO	1	SHIFT RIGHT SIX. In going from Y to Z, the data is shifted right six positions. The six low-order bits are lost and zeros go into the six high-order positions.
CL1	FROM, TO	1	CIRCULATE LEFT ONE. In going from Y to Z, the data is circulated left one position. The high-order bit goes into the low-order positions; no bits are lost.
CR1	FROM, TO	1	CIRCULATE RIGHT ONE. In going from Y to Z, the data is circulated right one position. The low-order bit goes into the high-order position; no bits are lost.
CL6	FROM, TO	1	CIRCULATE LEFT SIX. In going from Y to Z, the data is circulated left six positions. The six high-order bits go into the six low-order positions; no bits are lost.
CR6	FROM, TO	1	CIRCULATE RIGHT SIX. In going from Y to Z, the data is circulated right six positions. The six low-order bits go into the six high-order positions; no bits are lost.
SLS	FROM, TO	1	SHIFT LEFT SPECIAL. This instruction is an SL1 instruction with one added function - Z01=B18.



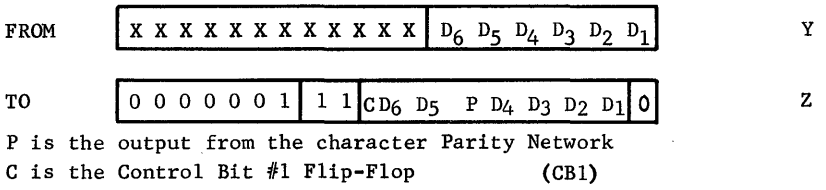
SRS	FROM, TO	1	SHIFT RIGHT SPECIAL. This instruction is an SR1 instruction with one added function - Z18=A01.



BC0	FROM, TO	1	BIT CHANGE ZERO. This is a special customer-oriented instruction, for use with eight-level Teletype data. In going from Y to Z, the data is rearranged from the eight-level Teletype format used on a transmission line to the six-bit alphanumeric format used in computers. The other two bits, the parity and control bits, are put in the CB 1 and CB 3 Flip-Flops.



MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
BC1	FROM, TO	1	BIT CHANGE ONE. This is the reverse operation of BC0. In going from Y to Z, the data is rearranged from the six-bit alphanumeric format into the eight-level Teletype format used on a transmission line. The control bit comes from CB 1 and the parity bit comes from the character parity output of the parity network.



BRANCH INSTRUCTIONS

The states of the Plus, Zero, and Even Flip-Flops are not changed by any branch instruction.

BRU	M	1	BRANCH UNCONDITIONALLY. Control is transferred to the instruction in M.
BRS	M	3	BRANCH TO SUBROUTINE. The location of the instruction following the BRS is stored in M; then, control is transferred to the location specified by the contents of M+1. M must be even.

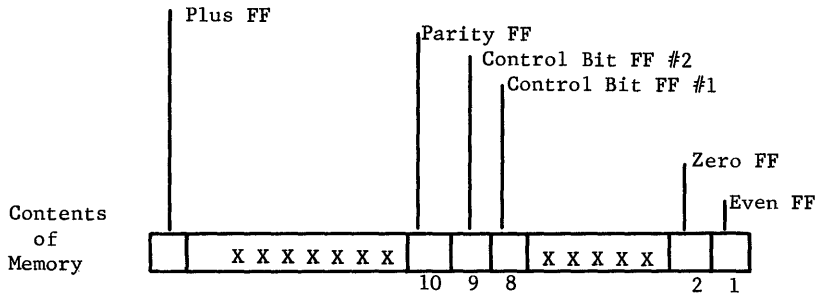
The remaining branch instructions are conditional branches. Control is transferred to M if the appropriate conditional test is satisfied, otherwise, control goes to the next instruction, i.e., the instruction following the branch instruction.

BZE	M	1	BRANCH ON ZERO. If the ZFF is zero, control is transferred to M.
BNZ	M	1	BRANCH ON NON-ZERO. If the ZFF is non-zero, control is transferred to M.
BPL	M	1	BRANCH ON PLUS. If the Plus Flip-Flop is plus, control is transferred to M.
BMI	M	1	BRANCH ON MINUS. If the Plus Flip-Flop is minus, control is transferred to M.

MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
BEV	M	1	BRANCH ON EVEN. If the Even Flip-Flop is even, control is transferred to M.
BOD	M	1	BRANCH ON ODD. If the Even Flip-Flop is odd, control is transferred to M.
SPECIAL INSTRUCTIONS			
DIF	I	1	DRIVE INTERNAL FUNCTION. A signal will be sent to those Internal Function Drivers which correspond to ones in I.
			Function
	DIF 1		Reset Control Bit Flip-Flops 1 and 2, and reset the Parity bit Flip-Flop.
	DIF 2		Reset the Buzzer Flip-Flop.
	DIF 3		Set the Buzzer Flip-Flop.
	DIF 4		Initiate the Hardware Load process.
	DIF 5-6		Not assigned.
	DIF 7		This is the SEL instruction.
	DIF 8		Set Control Bit Flip-Flop 1.
	DIF 9		Set Control Bit Flip-Flop 2.
	DIF 0		Set the Parity Bit Flip-Flop.
NIS	I	1	AND INTERNAL STATUS LINES TO Z. A logical "AND" is performed with I (1-10) and the Internal Status Lines. The only results are the new states of the Plus, Zero, and Even Flip-Flops.
			Function
	NIS 1		The character parity output of the parity network is a 1.
	NIS 2		The word parity output of the parity network is a 1.
	NIS 3		Control Bit Flip-Flop 2 and the word parity output of the parity network are identical. This is intended for use when transmitting data with error correcting techniques.
	NIS 4		The Operating Mode/Maintenance Mode switch is in the Maintenance Mode position.
	NIS 5-6		Not Assigned.
	NIS 7		Controller Selector is ready.
	NIS 8		Control Bit Flip-Flop 1 is a 1.
	NIS 9		Control Bit Flip-Flop 2 is a 1.
	NIS 0		The Parity Bit Flip-Flop is a 1.
LDF	M	2	LOAD SPECIAL FLIP-FLOPS. Selected bits from the contents of M are used to restore the conditions (saved by an STF instruction) of the Plus, Zero, Even, Control Bit 1, Control Bit 2, and Parity Flip-Flops. Bit position 1 goes to the Even Flip-Flop. Bit

MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION

position 2 goes to the Zero Flip-Flop and bit position 18 goes to the Plus Flip-Flop. Bits 8, 9, and 10 go to Control Bit FF#1, 2 and Parity FF, respectively.



STF	M	2	STORE SPECIAL FLIP-FLOPS. The conditions of the Plus, Zero, Even, Control Bit 1, Control Bit 2, and Parity Flip-Flops are stored in M in positions 18, 2, 1, 8, 9, and 10, respectively. (Same as LDF.)
HLT	I	1	CONDITIONAL HALT. The DATANET-30 will halt if this instruction is executed when the INHIBIT HALT switch on the MAINTENANCE panel is in DISABLE position.

BUFFER SELECTOR INSTRUCTIONS

There are six (6) Buffer Selector instructions. The Register Transfer FROM R, and the Register Transfer TO T have already been covered.

LDT	M	2	LOAD T. The contents of M are sent to the Transmit Data Drivers and from there to whichever channel has been preselected by the contents of the C Counter. The contents of M are unchanged.
DEF	I	1	DRIVE EXTERNAL FUNCTION. A signal will be sent to those External Function Drivers which correspond to ones in I. The signal(s) will actually get to only the Buffer Unit which has been preselected by the C Counter. The meaning of each driver varies with the particular input/output device.
NES	I	1	AND EXTERNAL STATUS LINES TO Z. A logical "AND" is performed with I (1-10) and the External Status Lines. The only results are the new states of the Plus, Zero, and Even Flip-Flops.

MNEMONIC	OPERAND	WORD TIMES	DESCRIPTION
SCN	I	1+3N	SCAN. The Bit Buffer Units are Scanned starting with Channel I. N equals the number of channels scanned. A detailed description of the operation of this instruction is given under the Bit Buffer Unit.

Controller Selector

There are three basic instructions which apply to all peripheral controllers via the controller selector.

CSR	I	3-10	CONTROLLER STATUS REQUEST. This instruction loads the B Register with an image of the status lines of the controller specified by I.
NIS7			AND INTERNAL STATUS LINE SEVEN. This command interrogates the controller selector to determine if the last controller select command issued has been completed.
SEL		1	SELECT. Select controller and initiate operations as specified by locations 3, 4, 5 of the memory.

INSTALLATION INFORMATION

Component Sizes

	Weight	Floor Area	Height	Minimum Clearance Area
3 Cabinets for the DATANET-30	2200 lbs.	117" x 32"	76"	9' 10" wide x 15' long

Electrical Requirements

The DATANET-30 is designed to operate from a standard 208Y/120-volt, 3-phase; 208/240-volt, single phase; or 120 volt, single phase, 60-cycle, a-c service. The equipment can also be operated from a 240v/120-volt, 3-phase, 60-cycle, a-c source of power without internal wiring changes. Maximum power input is 9.6 KVA. Maximum heat dissipation is approximately 22,000 BTU per hour, depending upon the selection of buffer modules.

Environmental Requirements

The ambient room temperature within the area should remain within the range of 65 to 85 degrees F., under all conditions of operation. The recommended temperature for optimum operation is

approximately 72 to 78 degrees. The temperature may cycle 20 degrees F., per hour (the possibility of condensation is excluded). The relative humidity should remain within a range of 40 to 60 per cent.

Ventilation

One of two types must be specified. Each type will include appropriate floor plates -

1. Under floor without blowers.
2. Self contained.

Cables to Communication Line Interface

Cables for each digital subset line relay are required. The cables are a fixed 50 feet long.

Controller Selector Cables

The cable from the controller selector to the peripheral controllers must be ordered by quantity and desired length--up to a maximum length of 100 feet. The DATANET-30 will accommodate 2 serial strings of controllers with the following options:

1. Two cables up to 100 feet long with 4 controllers each.

2. One cable up to 50 feet long with 6 controllers, plus one cable up to 100 feet long with 2 controllers.

3. One cable up to 100 feet long with 8 controllers.

INDEX

Page

SUMMARIES

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84.1