EXOS 204

Intelligent Ethernet Controller For UNIBUS Systems

Reference Manual

Revision B June 18, 1986
Publication No. 4200009-00

Excelan Inc.
2180 Fortune Drive
San Jose, CA 95131

EXOS 204

Intelligent Ethernet Controller
For UNIBUS Systems

Reference Manual

MANUAL REVISION HISTORY

MANUAL REVISION	DATE	SUMMARY OF CHANGES
A	03-22-85	Initial release EXOS 204 Ethernet Front-End Processor For UNIBUS Systems Reference Manual Publication No. 4200009-00
B	06-18-86	Manual Revision: Release B Product name changed to EXOS 204 Intelligent Ethernet Controller for UNIBUS Systems. Several technical/editorial changes to reflect enhancements made to the EXOS 204 Intelligent Ethernet Controller. Restructured the manual to include predominantly hardware information, which remains unchanged. NX 200 firmware information moved to a separate manual.

PREFACE

This manual describes the EXOS 204 Intelligent Ethernet Controller board. It covers information necessary to integrate the EXOS 204 in a UNIBUS-based system. The manual is intended to be used only as a reference manual and does not undertake to explain the product's design philosophy.

The Ethernet and UNIBUS standards are described in readily available documents; this manual makes no special effort to explain them.

Excelan supplies several TCP/IP protocol software packages (suitable for use with different operating systems) that can execute on the EXOS 204. Alternatively, users can design their own protocol and applications software.

For users who wish to design their own software, the EXOS 204 provides the on-board, EPROM-resident network executive NX 200, which includes a dedicated operating system kernel and a network services manager. By design, NX 200 insulates user protocol software from hardware implementation details. This approach simplifies software design and facilitates portability to future products, which will take advantage of latest hardware technologies.

Detailed documentation about the NX 200 Network Executive is available from Excelan. Refer to No. 7 listed below.

The following documents provide related reference and study material for EXOS 204 users.

EXOS 204 conforms to the following specification:

[1] *Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications (Standard 802.3-1985/International Standard 8802/3)*, The Institute of Electrical and Electronics Engineers, Inc., 1985.

[2] *The Ethernet: A Local Area Network: Data Link Layer and Physical Layer Specifications*, 1980.

[3] *The Ethernet: A Local Area Network: Data Link Layer and Physical Layer Specifications, Version 2.0*, 1982.

EXOS 204 conforms to the UNIBUS specifications:

[4] *UNIBUS Specifications Manual*, Mostek Corp., Motorola Inc., and Signetics Corp., Rev. B, 1982.

EXOS 204 uses the 82586 LAN Coprocessor for implementation of Ethernet Data Link protocol:

[5] *LAN Components User's Manual*, Document No. 230814-001, 1984.

EXOS 204 supports front-end processing of user-written higher-level protocols, on an 80186 CPU:

[6] *iAPX 86/88, 186/188 User's Manual*, Document No. 210911-001, 1983.

User-written protocol software must use the on-board, EPROM-resident NX 200 Network Executive:

[7] *NX 200 Network Executive Reference Manual*, Excelan, In., Document No. 4200036-00, 1986.

The following reference describes the C language, which is used for procedural specifications in this manual:

[8] Kernighan, B.W. and D.M. Ritchie, *The C Programming Language*, Prentice-Hall, Englewood Cliffs, New Jersey, 1978.

The following reference describes the ISO Open Systems Model:

[9] *Reference Model of Open Systems Interconnection*, International Organization for Standardization (ISO), Document ISO/TC97/SC16 N227, 1979.

For optimum accuracy, this manual should be used in conjunction with the Release Notes supplied with the product described in this manual.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1
INTRODUCTION

1.1. INTRODUCTION

The EXOS 204 Intelligent Ethernet Controller is a high-performance, front-end communications processor board that connects a UNIBUS system to an Ethernet* local area network. It implements the complete Ethernet Data Link Layer interface, with significant functional extensions, on a single UNIBUS double-height board.

The EXOS 204 Intelligent Ethernet Controller can be used both as an intelligent front-end processor and as a link-level controller. When used as a front-end processor, it executes the high-level network protocols on the board, thereby offloading this burden from the host CPU. When used as a link-level controller, it provides the standard Ethernet Data Link interface to the host system. Sections 1.1.1 and 1.1.2 briefly describe the two modes.

The EXOS 204 Intelligent Ethernet Controller is designed around three major hardware components and one firmware component. The hardware components are an Intel 80186 CPU, an Intel 82586 LAN Coprocessor, and RAM (128, 256 or 512 Kbytes). The firmware component is the EPROM-resident NX 200 Network Executive, also referred to as the NX 200 firmware.

The 80186 CPU executes the protocol software, which is downloaded to the board, and the NX 200 firmware. The 82586 LAN Coprocessor implements part of the Data Link layer. The RAM provides space for downloading protocol software and for buffering packets. The NX 200 firmware provides diagnostics, interfaces to host memory and the LAN Coprocessor, and operating system environments for execution of the downloaded protocol software. The NX 200 firmware also provides link-level controller functions.

The host UNIBUS system and the EXOS 204 communicate primarily through command and reply messages. These messages are stored in the host memory, which is accessible from the UNIBUS. The NX 200 firmware interprets the command messages and generates the replies.

1.1.1. EXOS 204 in Front-End Mode

In front-end processor mode, the host system downloads protocol software to the EXOS 204 at initialization time (or the EXOS 204 bootstraps itself from the Ethernet). This software then uses NX 200's real-time, multitasking process management services and I/O drivers to control the EXOS 204's Ethernet interface and to manage communications with the host system.

Standard protocol modules for the EXOS 204, such as the DARPA TCP/IP protocols, are available from Excelan. Figure 1-1 shows the relationship between these modules and the Open Systems Interconnection (OSI) reference model of the International Standards Organization (ISO).

Alternatively, users can develop or port their own protocols to run on the EXOS 204 under NX 200.

Please note that in this manual the term Ethernet refers to both Ethernet and Standard IEEE 802.3.

Programming information required to write protocol software that runs on the EXOS 204 is detailed in the *NX 200 Network Executive Reference Manual.*

1.1.2. EXOS 204 in Link-Level Mode

In link-level mode, the NX 200 firmware brings the EXOS 204's Data Link controller functions to the host interface. The host system obtains Data Link services through standard request/reply messages. In this mode, the EXOS 204's RAM is entirely available for buffering packets. Link-level controller mode is useful for applications where host-resident protocol software has already been developed or where it is otherwise not feasible to download high-level protocols to run on the EXOS 204.

Programming information required to write I/O drivers to interface host-resident protocol software to the NX 200 Data Link functions is detailed in the *NX 200 Network Executive Reference Manual.*

1.1.3. Manual Organization

This manual is organized as follows:

Chapter 1, Introduction, provides an overview of the EXOS 204 features and function.

Chapter 2, Hardware Reference, describes the architecture of the EXOS 204 Intelligent Ethernet Controller and the function of various on-board components.

Chapter 3, Installation, discusses how to install the EXOS 204 Intelligent Ethernet Controller in a generic UNIBUS system. The chapter also details step-by-step procedures for installing the EXOS 204 board in a Digital Equipment Corporation 11/700 Series UNIBUS-based system. Chapter 4, Service Information, details procedures on how to obtain factory service for the EXOS 204 Intelligent Ethernet Controllers.

Appendices A through C provide Component and Jumper Layout, Schematics, and Transceiver Pin-outs, respectively.

1.2. EXOS 204 HARDWARE

Figure 1-2 shows a block diagram of EXOS 204. Architecturally, EXOS 204 consists of two loosely-coupled elements: an Ethernet Data Link Layer controller and a microprocessor-based protocol processing engine. These components communicate with each other through an internal bus and 128, 256 or 512 Kbytes of dual-port RAM.

EXOS 204 implements the Ethernet Data Link protocol using the 82586 LAN Coprocessor. Functions such as address recognition, CRC checking, and buffer chaining are managed in hardware, leaving the 80186 CPU fully available for front-end processing applications. The protocol-processing engine is supported by 128, 256 or 512 Kbytes of RAM. Two 16–Kbyte EPROMs contain Excelan's NX 200 firmware, which includes self-diagnostic tests, an operating system kernel, host and network interfaces, and network bootstrap code.

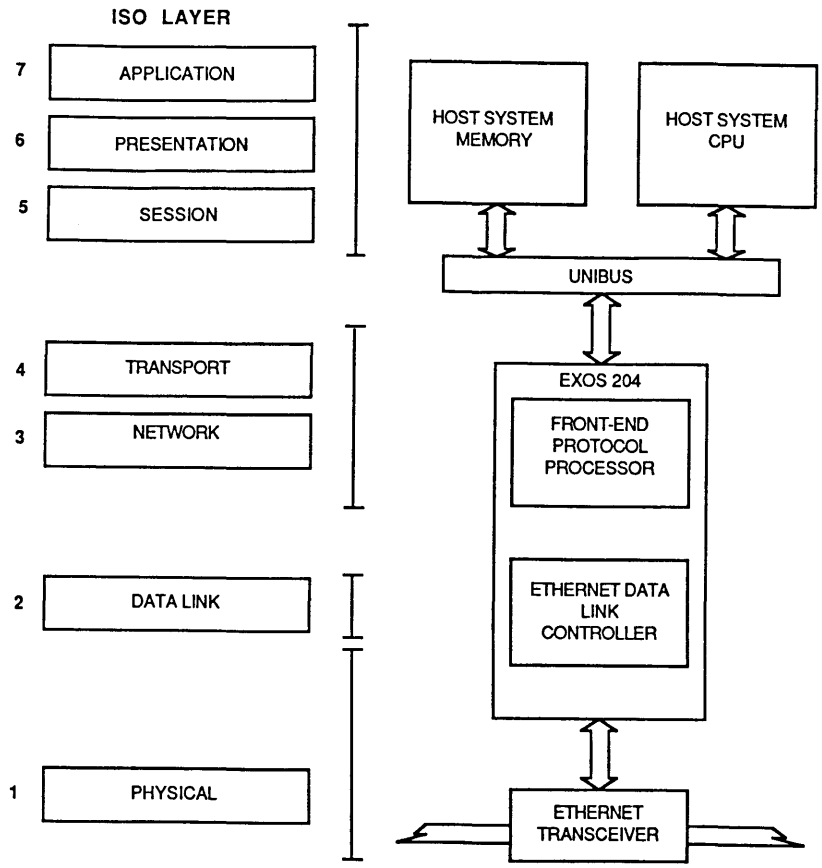


Figure 1-1: The EXOS 204 Front-End Mode Implementation and ISO/OSI

1.2.1. Principal Hardware Features

The following are the salient features of the EXOS 204:

- One quad-sized (8.9" by 10.44") UNIBUS board, which requires one SPC slot.
- On-board 8 MHz 80186 CPU microprocessor and 128 Kbytes of RAM on Model 2, 256 Kbytes on Model 3, or 512 Kbytes on Model 4 support high-level network protocols on-board.
- Dual-port memory allows concurrent, full-speed access by the on-board CPU and the on-board LAN Coprocessor.

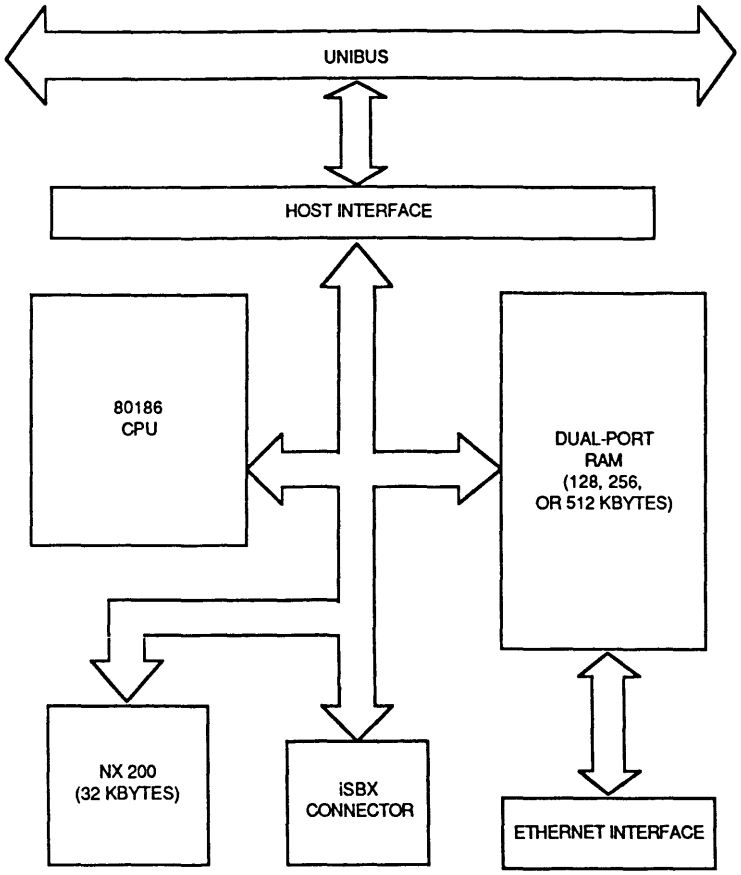


Figure 1-2: EXOS 204 Block Diagram

- Can receive successive frames with minimum interframe spacing (9.6 microseconds). Can receive immediately after transmitting, or vice versa, with minimum interframe spacing and without losing data.
- Hardware recognition of physical, broadcast, and multiple multicast addresses, in addition to promiscuous mode.
- Hardware-supported buffer chaining allows buffering of an arbitrary number of received frames without any CPU intervention. Allocation of buffers, both location and size, is completely under software control.

1.2.2. Ethernet Compatibility

EXOS 204 is fully compliant with the Standard IEEE 802.3 as well as with Ethernet specifications Versions 1.0 and 2.0. Used with a Standard IEEE 802.3 or Ethernet transceiver, the EXOS 204 provides all Data Link and Physical Layer services.

1.2.3. UNIBUS Compatibility

EXOS 204 conforms with UNIBUS specifications by DEC as a 16-bit master. Compliance is 8-bit and/or 16-bit transfers, 18-bit addressing, and bus-vectored interrupts.

1.2.4. UNIBUS Interface

EXOS 204 can access the entire UNIBUS system memory space (256 Kbytes), including the full 8-Kbyte I/O space, as a 16-bit bus master. A one-byte communication path is provided from the UNIBUS to the EXOS processor via a memory-mapped I/O port. This is used during initialization to transmit the address of a communication area in the shared UNIBUS memory.

EXOS 204 and host processors can interrupt each other. The board generates bus-vectored interrupts to interrupt the host. Interrupt priority can be set from level 4 to level 7, via jumper selection. The host can interrupt the EXOS 204 processor by writing to an I/O port.

1.2.5. Ethernet Functions

EXOS 204 performs all physical and Link Layer Ethernet functions except for transceiver functions. These include the following:

- Serial-to-parallel and parallel-to-serial conversions
- Address recognition
- Framing and unframing of messages
- Manchester encoding and decoding
- Preamble generation and removal
- Carrier sense and deference
- Collision detection and enforcement, including jamming, backoff timing, and retry
- FCS (CRC) generation and verification
- Error detection and handling

1.2.6. Address Recognition

Each board has a unique 48-bit Ethernet address, which is stored in an EPROM. (The host software can override this address at run time.) Recognition of physical, broadcast and multicast addresses is fully supported. Up to 252 multicast addresses can be assigned to a station; a very efficient filtering scheme reduces processing overhead. EXOS 204 also provides a promiscuous mode, in which it accepts all addresses.

1.2.7. Frame Format

Link-level frames are formatted as per the Ethernet specification: preamble (64 bits of synchronizing sequence), destination address (48 bits), source address (48 bits), message type (16 bits), data (46 to 1500 bytes) and FCS (32 bits). The preamble is generated and removed in hardware. Generation and checking of the Frame Check Sequence (FCS) is also handled in hardware.

1.2.8. Error Handling

EXOS 204 handles all Ethernet error conditions, including CRC, alignment, and length errors. Packets containing these errors can optionally be received.

1.2.9. High Level Protocol Support

On-board processing power supports execution of higher level communications protocols, above the Ethernet link layer. The elements of this protocol execution environment are the following:

- On-board 8 MHz Intel 80186 CPU, with on-chip clock timer and interrupt controller, operating at 8 MHz
- 128, 256 or 512 Kbytes of dual-port RAM
- 32 Kbytes of EPROM containing the NX 200 Network Executive firmware

Firmware supplied with the board (the NX 200 Network Executive) provides simplified Ethernet and host interface device drivers, and a multitasking environment for high-level network protocols.

1.3. NX 200 FIRMWARE – THE NETWORK EXECUTIVE

The NX 200 Network Executive, an EPROM-resident set of modules, is an integral part of the EXOS 204. It contains board diagnostics, an operating system kernel, interfaces to the host and the Ethernet, and network bootstrap code. When EXOS 204 is used in front-end mode, NX 200 provides the operating system environment for the downloaded protocol software that runs on the board. When the EXOS 204 is used in link-level mode, NX 200 provides the Data-Link Controller functions for the protocol software that runs on the host system.

NX 200 resides in EPROM memory, which appears at the high end of the 1 Mbyte address space of the 80186. NX 200 data structures use 4 Kbytes of the RAM; the rest is available for higher level software. Figure 1-3 provides a graphic representation of the NX 200 software architecture.

For users who use prepackaged software, such as Excelan's EXOS Series 8000 TCP/IP Network Software, NX 200 is transparent. Accordingly, they need not concern themselves with the internals of NX 200.

For users who plan to write their own protocol software or link-level drivers, it is necessary to understand the NX 200 internals. A summary of NX 200 features is given in the following sections. Refer to the *NX 200 Network Executive Reference Manual* for further details.

1.3.1. Principal Features of NX 200

The following is a list of the main features of NX 200:

- Self-diagnostics for testing the integrity of the EXOS 204 hardware.
- Booting process that allows higher level software to be downloaded either from the host or from the network.
- Real-time kernel that provides a multiasking environment, enabling the protocol software to be constructed in a structured manner as a set of cooperating processes.
- Device drivers for the Ethernet controller and host computer interface. Access through message queues simplifies pipelined communications.
- Supports network management functions by collecting network statistics.
- Allows the EXOS 204 to be used as a simple Data Link controller, giving direct access to the network without downloading any software.

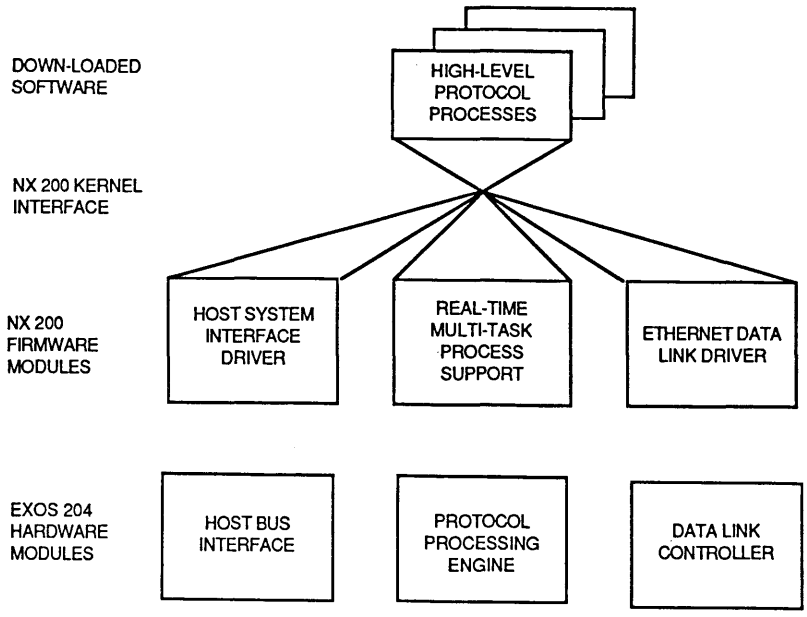


Figure 1-3: NX 200 Software Architecture

1.3.2. Initialization

On reset the NX 200 firmware performs a series of self tests that confirm the integrity of the hardware. In case of failure, the firmware communicates diagnostic codes through an LED display. After successful completion of the tests, the EXOS 204 either boots itself from the Ethernet or awaits initialization by the host system, depending on the jumper option selected on the board.

If the jumper selects initialization by a host system, the host then uses a configuration message to select NX 200's mode of operation and to specify several other parameters. It can download software directly, direct NX 200 to boot itself from the Ethernet, or select link-level controller mode. If initialization includes downloading software, then NX 200 spawns a process and enters front-end processor mode of operation.

1.4. INSTALLATION

Installing the EXOS 204 Intelligent Ethernet Controller is a relatively simple task. In a typical UNIBUS system, it consists of turning off the power, accessing the card cage, inserting the board, and establishing the required connection through appropriate cables and connectors. In general, the complexity of installation procedure depends on the physical design of the host machine rather than on the design of the EXOS 204 Intelligent Ethernet Controller.

1.5. CUSTOMER SERVICE

All EXOS 204 Intelligent Ethernet Controllers, like all other Excelan products, must pass very rigorous quality control procedures before they are shipped to customers. Even so, some problems and questions are bound to come up in real applications. Excelan maintains a highly qualified and trained customer service staff who resolve technical problems related to Excelan product and advise on procedures for shipping the products back to factory for service.

Chapter 2
HARDWARE REFERENCE

2.1. INTRODUCTION

Most of the hardware-dependent aspects of the EXOS 204 implementation are hidden by the NX 200 firmware. Therefore, this chapter discusses only those aspects that are "visible" to and are of concern to most users. These aspects include issues related to UNIBUS, Ethernet, on-board processing, NX 200 firmware, and jumper-selectable options. This chapter discusses these issues in detail. However, theory of operation is deliberately omitted. The schematics included in Appendix B may be referred to for further understanding of the board functions.

UNIBUS-related issues discussed in this chapter include bus interface, compliance, memory access, I/O access, interrupt configuration, and priority resolution.

Ethernet-related issues discussed include Ethernet interface, compliance, functions, address recognition, operation timing, packet buffering, error handling, and network connections.

The on-board processing issues encompass the resources available for high-level and link-level protocol processing.

The NX 200 firmware issues include firmware configuration, self-test, and diagnostics.

2.2. EXOS 204 COMPONENT LAYOUT

Physical layout of the EXOS 204 board, as seen from the component side, is shown in Figure A-1. This figure also shows the location of various jumpers. For development purposes, the following components are socketed:

- 80186 CPU
- Two 16 Kbyte EPROMs

Note that except for the jumpers and the socketed components mentioned above, all other components are not user-serviceable. If any performance problems are encountered, you should obtain authorized service as described in Chapter 4.

EXOS 204 provides several jumpers for selecting various options. The jumper-selectable options are described in detail in subsequent sections. Table 2-1 provides a quick reference to jumper-selectable options. (For convinence, this table is also included in Appendix A.)

EXOS 204 includes four Light Emitting Diodes (LEDs) to communicate status information. These are located in adjacent positions at the top left side of the board, seen from the component side, and can easily be seen while the board is installed. Figure 2-1 shows their relative locations and functions. Subsequent sections describe the LEDs in more detail.

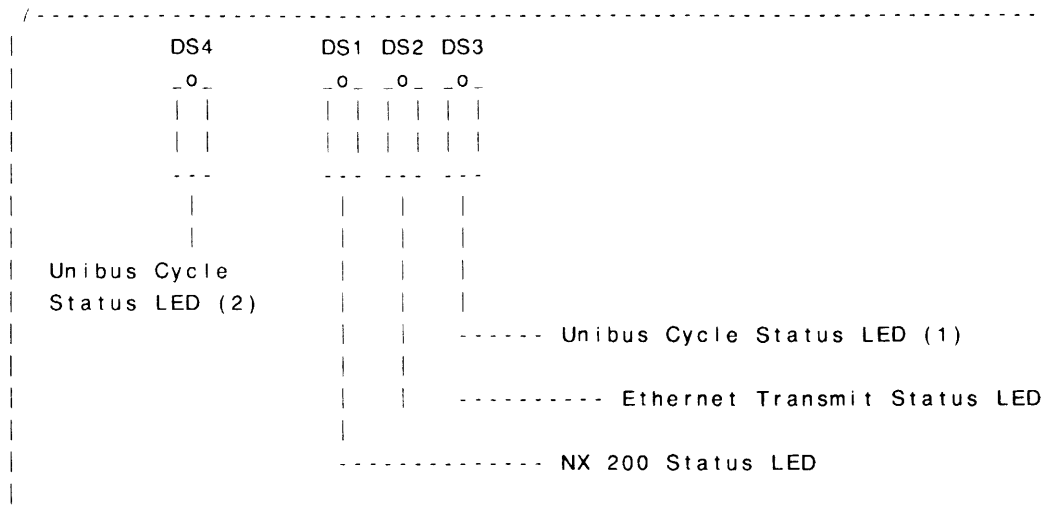


Figure 2-1: EXOS 204 Status LEDs

2.3. UNIBUS INTERFACE

The EXOS 204 Intelligent Ethernet Controller is built on a single quad-sized (8.9" by 10.44") UNIBUS board, which occupies one Unibus SPC slot. It represents one DC load on the UNIBUS.

2.3.1. UNIBUS Compliance

The EXOS 204 conforms to UNIBUS specifications as a 16-bit bus master. The compliance is as follows:

- 8-bit or 16-bit transfers
- 18-bit addressing
- Bus-vectored interrupts (software programmable vectors)
- D16 A24 UNIBUS slave
- 4-level Bus Arbitration Requester

2.3.2. UNIBUS Memory Access

EXOS 204 generates 18-bit memory addresses to access the entire 256 Kbytes of UNIBUS memory.

Note that the EXOS 204's own memory is not accessible from the UNIBUS.

Table 2-1: Quick Reference to Jumper Options

Jumper	Function (when jumper is installed)			Factory Setting
J2	Invoke the EPROM-resident Monitor program on power-up or reset			Absent
J3	DMA with burst capability present			Installed
J4	Disable SQE (Heartbeat) check, Version 1.0 mode			Installed
J6	Used in conjunction with J9; specifies available RAM:			Absent
	J6	**J9**	**RAM**	
	Absent	Absent	128K (factory setting)	
	Installed	Absent	256K	
	Absent	Installed	512K	
	Installed	Installed	Reserved	
J7	Boot from network			Absent
J8	Disable Carrier Sense			Absent
J9	See description under J6.			Absent
J10	Ground IRO from iSBX			Absent
J11	Ground IRO from iSBX			Absent
J12	27256 user EPROMS			Absent
J13	2764 or 27128 user EPROMs			Installed
J14	27256 Kernel EPROMs			Absent
J15	2764 or 27128 Kernel EPROMs			Installed
J16	(3 jumpers) bits 10-12 of I/O port address (Installed = 0; absent = 1.)			Absent J16-2; others installed.
J17-1	Select DMA burst length			Installed
J17-2	Select DMA burst length			Absent
	J17-1	**J17-2**	**burst-length**	
	Installed	Installed	2	
	Installed	Absent	4	
	Absent	Installed	8	
	Absent	Absent	16	
J17-3	Enable bus timeout			Absent
J18	(8 jumpers) bits 2-9 of I/O port address			All installed (0)
J19	Configure UNIBUS interrupt levels*			
J20	Configure UNIBUS interrupt levels*			

*Refer to Table 2-2 for details.

2.3.3. UNIBUS I/O (Slave) Access

EXOS 204 can access the full 8-Kbyte UNIBUS I/O address space. However, it does not generate any I/O commands unless requested by user software.

EXOS 204 presents two read/write host-memory-mapped I/O ports – A and B – to the UNIBUS. Their functions are documented in Section 5.2, of the *NX 200 Network Executive Reference Manual*. Port A's address is fully jumper selectable, at any even word address in the I/O address range 760000 to 777774 (octal) corresponding to 3FE800 to 3FE802 (Hexadecimal). Port B's address is the address of port A plus 2.

The UNIBUS addresses of I/O ports A and B are word addresses. For selection of an address, each of the 8 jumpers in J18 and of the 3 jumpers in J16 must be appropriately selected. Address bits 0 and 1 are not selectable. Currently, address bit 0 is always 0 (zero). Bit 1 selects port A when 0, and port B when 1. See Appendix A.

Address bits 13 through 17 are not selectable; they are always 1. As shipped from the factory, except J16-1, all jumpers are installed. Consequently the UNIBUS addresses 764000 and 764002 (octal) are selected for I/O ports A and B respectively.

The effects of reading and writing ports A and B are summarized below:

Read A: No Operation.

Write A: Resets the EXOS 204 board

Read B: Returns the EXOS 204 status byte:

- Bit 0: (Error Bit) when 0, indicates a fatal error in EXOS 204. When the EXOS 204 is reset, this bit is 0, but will be set to 1 if the self test completes successfully. If this bit is not set within 3 seconds, then the EXOS 204 has failed the self-diagnostics.
- Bits 1-2: Undefined.
- Bit 3: (Ready Bit) when 0, indicates that NX 200 is ready to accept a byte written into port B. When 1, NX 200 has not yet read the byte last written into port B.
- Bits 4-5: Undefined.
- Bit 6: (Loopback Test Bit) when 0, indicates loopback test passed. When 1, indicates loopback test failed, possibly due to faulty transceiver or faulty transceiver cable.
- Bit 7: Undefined.

Write B: Interrupts the EXOS 204 CPU, and communicates a 1-byte value. This is the only way to communicate a value to the EXOS 204 other than through shared memory.

2.3.4. UNIBUS Interrupt Mechanism

EXOS 204 can assert bus-vectored interrupts on the UNIBUS. Interrupt priority level is jumper-selectable in the range from level 4 thru 7. Factory setting is for level 5.

EXOS 204 can also be initialized to generate memory-mapped interrupts to the host. The host interrupts the EXOS 204 by writing to I/O port B.

Table 2-2: Interrupt Priority Set-Up Table

	J20 BUS GRANT								J19 BUS REQUEST			
	16	15	14	13	12	11	10	9	8	7	6	5
	o	o	o	o	o	o	o	o	o	o	o	o
LEVEL 4	|	|							|			
	o	o	o---o		o---o		o---o		o	o	o	o
	1	2	3	4	5	6	7	8	1	2	3	4
	16	15	14	13	12	11	10	9	8	7	6	5
	o	o	o	o	o	o	o	o	o	o	o	o
LEVEL 5			|	|					|		
(DEFAULT)	o---o		o	o	o---o		o---o		o	o	o	o
	1	2	3	4	5	6	7	8	1	2	3	4
	16	15	14	13	12	11	10	9	8	7	6	5
	o	o	o	o	o	o	o	o	o	o	o	o
LEVEL 6					|	|				|	
	o---o		o---o		o	o	o---o		o	o	o	o
	1	2	3	4	5	6	7	8	1	2	3	4
	16	15	14	13	12	11	10	9	8	7	6	5
	o	o	o	o	o	o	o	o	o	o	o	o
LEVEL 7							|	|			|
	o---o		o---o		o---o		o	o	o	o	o	o
	1	2	3	4	5	6	7	8	1	2	3	4

2.3.5. UNIBUS Priority Resolution

When several devices contend for bus mastership, the UNIBUS system grants control to the device physically closest to the processor module. Accordingly, the EXOS 204 should be installed closer to or farther from the processor module depending on the priority desired. The EXOS 204 uses the UNIBUS NPR line to request permissiom to transfer data to and from the host memory.

2.3.6. UNIBUS Error Interrupt Option

When Jumper J17-3 is present, the bus controller interrupts the 80186 if an error is detected on the UNIBUS; during the time the EXOS 204 is acting as the bus master (error is either bus timeout or parity error during read). When this jumper is not in and a bus error occurs, the bus hangs up, no interrupt is issued, and the LED DS4 lights up. (Also see Section 2.3.8.)

2.3.7. DMA Burst Length Selection

The EXOS 204 permits setting of DMA burst setting of 2, 4, 8, or 16 words per bus grant. Jumpers J17-1 and J17-2 set the DMA burst length as follows:

J17-1	J17-2	burst-length	
Installed	Installed	2	
Installed	Absent	4	(default setting)
Absent	Installed	8	
Absent	Absent	16	

2.3.8. UNIBUS Cycle Status LED

The Light Emitting Diodes (LEDs) in positions DS3 and DS4 on the EXOS 204 board indicates that a UNIBUS cycle is in progress as follows. If DS4 is constantly lit, then the EXOS 204 has probably attempted to access a non-existent address on the UNIBUS. In general, this condition points toward a user software bug. Note that this applies only if the bus time out feature is not selected by J17-3. If DS3 is constantly lit and DS4 is not lit, then most likely the EXOS 204 is unable to get DMA grant from the UNIBUS.

2.4. ETHERNET INTERFACE

Integrated with a standard Ethernet or IEEE 802.3 transceiver, the EXOS 204 performs all specified Ethernet physical and link-level functions. The EXOS 204 uses the 8023A ESI (Ethernet Serial Interface) chip to interface with Ethernet.

2.4.1. Ethernet Compliance

EXOS 204 conforms fully to the IEEE 802.3 standard as well as to Ethernet specification (Version 1.0 or 2.0).

As shipped from the factory, EXOS 204 is configured for Ethernet Version 1.0 use; for IEEE 802.3 and Version 2.0 use, jumper J4 should be removed.

2.4.2. Ethernet Functions

Ethernet functions implemented on the EXOS 204 Intelligent Ethernet Controller include the following:

- Serial/parallel and parallel/serial conversion
- Physical and multicast address recognition
- Packet framing and unframing
- Manchester encoding and decoding
- Preamble generation and removal
- Carrier sense and deference
- Collision detection and enforcement.
- Backoff and retry timing
- Frame check sequence (CRC) generation and verification
- Alignment and length error detection and handling

2.4.3. Ethernet Address Recognition

EXOS 204 recognizes physical, multicast, and broadcast addresses without user software intervention. A very efficient multicast address filter, implemented in hardware, greatly reduces the overhead of multicast address recognition. The multicast address filter can be disabled so that all multicast addresses are accepted. The EXOS 204 also provides a promiscuous mode, in which it accepts all addresses.

Each EXOS 204 Intelligent Ethernet Controller has a unique 48-bit Ethernet address, stored in a PROM. This is the board's physical address by default, but the effective physical address resides in RAM and can be modified by user software.

2.4.4. Ethernet Operation Timing

EXOS 204 can receive successive frames with minimum interframe spacing (9.6 microseconds). It can also receive immediately after transmitting, or vice versa, with minimum interframe spacing and without losing data.

2.4.5. Ethernet Packet Buffering

When EXOS 204 is running in front-end mode, under NX 200 firmware control, the EXOS 204 can buffer an arbitrary number of receive and transmit packets. The actual number of available buffers depends on the application criteria. User software can select both buffer size and location. The location can be between 01000H and 1FFFFH in the EXOS 204's dual-port memory.

Ethernet link-level controller hardware can buffer up to 32 receive packet buffers, and receive as many packets, without CPU intervention. Transmit packets are chained by NX 200 firmware and transmitted with minimal delay.

2.4.6. Ethernet Error Handling

EXOS 204 can be selectively enabled to receive packets normally rejected due to CRC and alignment errors.

2.4.7. Ethernet Transmit Status LED

EXOS 204 lights an LED at position DS2 while transmitting on the Ethernet.

2.4.8. Ethernet Transceiver Connector

EXOS 204's Ethernet connector is a 16-pin IDH type which mates with a 16-pin IDC type connector. Pinouts are defined as per Ethernet specifications. The connectors are keyed, and pin number 1 can also be identified by an arrow on the connector. Note that it is still possible to insert the connector backwards.

2.4.9. Pin Definition of Ethernet Connector

The Ethernet connector (P3) on the EXOS 204 is a 16-pin dual-row connector with latches. This accepts normal flat-cable connectors that have a 16-pin flat-cable connector at one end and a 15-pin D-Sub connector on the other. The flat-cable connector connects to the EXOS 204 and the D-Sub connector connects to the standard Ethernet transceiver cable. Note that the numbering scheme is different for the two types of connectors.

The pin-out for the P3 connector, using the flat-cable numbering scheme is shown in Table 2-3.

Table 2-3: Ethernet Connector (P3) Pin Definition

Pin #	Function	Polarity
2	Collision	(–)
3	Collision	(+)
4	Transmit	(–)
5	Transmit	(+)
8	Receive	(–)
9	Receive	(+)
10	Power	+12V
11	Power	Gnd
6,7,12,15	Signal	Gnd
1,14,16	Not Used	

2.5. ON-BOARD PROCESSING CAPABILITIES

The EXOS 204 is designed to facilitate the implementation of higher–level communications protocols on its own processor. The following are the major elements of this intelligent Ethernet controller:

- An 8-MHz 80186 CPU, clock speed 8 MHz
- 128 Kbytes of dual-port RAM (Model 2), 256 Kbytes of RAM (Model 3), and 512 Kbytes (Model 4). On all models, all but 4 Kbytes of RAM is available for user software.
- NX 200 Operating System kernel, residing in two 16-Kbyte EPROMs
- Sockets for two 32-Kbyte EPROMs for installing user-coded firmware.

The NX 200 operating system kernel provides a real-time, multitasking environment for the implementation of higher level protocols on EXOS 204. NX 200 implements consistent and portable access methods for the Ethernet and host interfaces. In addition, it executes self-diagnostics and can optionally drive the EXOS 204 as an intelligent link-level controller, in which case the user is not required to download protocol software.

The two 32-Kbyte user EPROMs can be used to install user-coded firmware on the board. These EPROMs are mapped to addresses C0000H to CFFFFH. Users can include their new protocols, programs, or routines in these EPROMs. This feature can be very useful for users who write their own network software.

2.6. FIRMWARE CONFIGURATION OPTIONS

Jumpers J7 selects NX 200 firmware options. If J7 is installed, the EXOS 204 attempts to download software from the Ethernet after self-test is complete. If the jumper is not installed, the EXOS 204 awaits initialization from the host after the self-test is complete.

Jumper J4 when installed (default) disables the SQE (Heartbeat) check that is performed after every transmit. This provides Ethernet Version 1.0 compatible

transceiver connection. Note that if a Version 2.0 or an IEEE 802.3 transceiver is to be used, jumper J4 should be removed.

It may be necessary to install jumper J8, that is disable the Carrier Sense function, when a broad-band transceiver is used. This requirement is indicated by a 20H Return Code described in Section 6.3.4 of *NX 200 Network Executive Reference Manual.*

2.7. iSBX CONNECTIONS

A 44-pin iSBX connector, which meets the IEEE P969 specifications, is provided for adding daughter boards (such as, a serial communications board). Two jumper-selectable interrupt lines (J10 and J11) are provided. These lines are active high. Therefore, if either one of these lines is used, then the other must be grounded. Unless a software driver is installed, both jumpers should be left open.

2.8. SELF-TEST OPERATION

The NX 200 firmware performs a series of tests which exercise the hardware and software components of the EXOS 204 Intelligent Ethernet Controller. In addition to ensuring the EXOS 204 board is functioning properly, the tests can be used to identify specific software or hardware problems associated with configuration or operation. The errors are reported via an LED making it possible for them to be identified and corrected.

When the EXOS 204 board is reset by the UNIBUS INIT line or by host software, NX 200 firmware runs these comprehensive diagnostic tests on the EXOS 204 components. The tests complete within three seconds, whereupon the board is ready to be configured. Any test failure is reported to the host via an I/O port. Refer to the applicable "Initialization and Host Interface" chapter of the *NX 200 Network Executive Reference Manual,* for additional information.

2.8.1. NX 200 Status LED

Test progress and status are also reported via an LED at position DS1. On EXOS 204 reset, this LED is lit, and it remains lit constantly while the self-tests are in progress. When the self-tests are complete, the LED flashes evenly until the EXOS 204 board is initialized by the host or from the Ethernet. After initialization, LED DS1 turns off.

If the diagnostics indicate a hardware problem, then the LED will be lit constantly, or communicate an error code by flashing long and short pulses. Software errors that occur during the process of configuration can also result in an error code display. Error codes are 8-bit numbers and are presented bit-by-bit, starting with the most significant bit. A long pulse is a "1" bit, and the short pulse is a "0" bit. The error code is continuously repeated, with a pause in between to demarcate the starting point. Table 2-4 specifies all defined error codes for EXOS 204.

2.8.2. Error Handling

As stated earlier, NX 200 handles all Ethernet error conditions, including user software configuration, and native hardware errors. Additionally, NX 200 also monitors for fatal hardware and software errors that may occur during general network operation.

2.9. ERROR CATEGORIES

The errors are logically categorized into three groups.

- A0H-AFH: Fatal software configuration errors
- B0H-BFH: Fatal hardware errors
- C0H-CFH: Fatal errors, either software or hardware, which occur during the course of normal operation

2.9.1. Fatal Software Errors

Although software configuration errors generally occur from entering inappropriate values for system configuration, on rare occasions, they can result from a bad bit in a memory chip being interpreted by NX 200 as an invalid value returned. The software generated error codes are also available and useful for debugging user software written to configure the Ethernet utilizing non-EXOS, user proprietary protocols.

An exception to this is error **AFH - Net Boot Failed** which results from utilizing the network bootstrap procedures for diskless workstations. This function, associated with an EXOS Intelligent Ethernet Controller jumper option, is not currently implemented in the NX 200 operating system kernel.

2.9.2. Fatal Hardware Errors

Fatal hardware errors generally occur when NX 200 encounters specific EXOS hardware failure. However, the following three errors can be exceptions to this case, and may be due to incorrectly seated or installed cabling. In the event these errors occur, check and reconnect the cables, then reset the system. If this does not correct the condition and the error continues to occur, refer to Chapter 4 for service information.

BBH - Transmission test failed
BCH - Receive test failed
BDH - Local loopback data path test failed

The third and final category is directly associated with fatal errors that occur during normal operation, and are not usually encountered upon executing a reset and standard self-test. These errors can be produced by either software, hardware, or a combination of both. The software errors may be intermittent, while the hardware errors may be misconnections between the host and the network, or host and EXOS 204 board.

The five errors listed below are generally associated with the physical interface between the host and the EXOS 204.

C1H - Host memory read-write test failed
C9H - NMI interrupt for bus timeout failed
CAH - Host interrupt test failed
CCH - Divide error exception
CDH - Undefined interrupt type

Table 2-4: Self-Diagnostic and Configuration Error Codes

Hex Code	Pulse Code	Explanation of Error Code
Software Generated Errors:		
A0H	-.-.	Invalid address for configuration message.
A4H	-.-. .-..	Invalid operation mode parameter.
A5H	-.-. .-.-	Invalid host data format test pattern.
A7H	-.-. .---	Invalid configuration message format.
A8H	-.-. -...	Invalid movable data block parameter.
A9H	-.-. -..-	Invalid number of processes parameter.
AAH	-.-. -.-.	Invalid number of mailboxes parameter.
ABH	-.-. -.--	Invalid number of address slots parameter.
ACH	-.-. --..	Invalid number of hosts parameter.
ADH	-.-. --.-	Invalid host queue parameter.
AEH	-.-. ---.	Improper objects allocation.
AFH	-.-. ----	Net boot failed.
Hardware Generated Errors:		
B0H	-.--	Checksum on NX 200 EPROM failed.
B1H	-.-- ...-	Memory test failed for 0-128K.
B2H	-.-- ..-.	Memory test failed for 128K up to the highest address.
B3H	-.-- ..--	Counter test failed.
B4H	-.-- .-..	Interrupts test failed.
B5H	-.-- .-.-	Transmission test failed.
B6H	-.-- .--.	Receive test failed.
B7H	-.-- .---	Local loopback data path test failed.
B8H	-.-- -...	CRC test failed.
B9H	-.-- -..-	Checksum on physical address EPROM failed.
BAH	-.-- -.-.	Bus Timeout.
BBH	-.-- -.--	Ethernet chip initialization failed.
BCH	-.-- --..	Ethernet chip self-test failed.
BDH	-.-- --.-	Ethernet chip resource counter failed.
BEH	-.-- ---.	External loop-back test alignment error.
BFH	-.-- ----	SBX board not in place.
Operation Generated Errors:		
C0H	--..	Specified time exhausted.
C1H	--.. ...-	Host memory read/write test failed.
C8H	--.. -...	Parity hardware logic failed.
C9H	--.. -..-	NMI interrupt for bus timeout failed.
CAH	--.. -.-.	Host interrupt test failed.
CBH	--.. -.--	Command unit test failed.
CCH	--.. --..	Divide error exception.
CDH	--.. --.-	Undefined interrupt type.
CEH	--.. ---.	Command not executed by the CU of the 82586.
CFH	--.. ----	Command block sync failed between h/w and s/w.

One error, **CBH - Command Unit Test Failed,** can occur between the host and the network if the transceiver malfunctions or is physically not connected to the network. If such is the case reconnect the host to the network and reboot. Repetition of the error code will usually indicate a transceiver malfunction.

2.10. GENERAL SPECIFICATIONS

The following are general specifications for EXOS 204.

Power Requirement:	+5VDC @ 5.0 Amp Max +15VDC @ 0.6 Amp Max (for transceiver and iSBX connector) -15VDC @ 0.1 Amp Max (for iSBX connector only)
Operating Environment:	
	Temperature: 5° C to 50° Humidity: 0% to 90% without condensation
I/O Register Addresses:	Jumper-selectable (from 760000 to 777774 (octal)) in increments of 2 Factory setting: Port A : 764000; Port B :764002
Interrupt Vector Address:	Software programmable
Interrupt Priority Level:	Jumper selectable (BR4, BR5, BR6, or BR7)
Data Transfer:	Direct Memory Access (DMA) with jumper selectable burst size (2, 4, 8 or 16 word per NPR) for all word-aligned data
UNIBUS Timeout:	16 microsecond after MSYN asserted and no SSYN returning (jumper selectable)
UNIBUS Loading:	AC - 2 DEC unit loads DC - 1 DEC unit load
Physical Size:	1 6-layer DEC quad-sized PCB

Chapter 3
EXOS 204 INSTALLATION

3.1. INTRODUCTION

The EXOS 204 Intelligent Ethernet Controller is a six-layer DEC quad-sized printed circuit board that interfaces only to the Small Peripheral Controller (SPC) slots on a UNIBUS back panel using connector rows C, D, E, and F. The EXOS 204 is designed for use in UNIBUS-based systems, such as the DEC PDP-11 Series and/or VAX Series of minicomputers.

This chapter describes installation procedures for the VAX minicomputer models 11/725, 11/730, 11/750, and 11/780. The EXOS 204 installation procedure for the 11/725 and the 11/730 is the same; it is described in Section 3.3. Similarly, the EXOS 204 installation procedure for the 11/750 and the 11/780 is the same; it is described in Section 3.4. For similar computer systems not included here (such as the DEC PDP-11 series of minicomputers), consult the applicable system hardware manual(s).

Section 3.5 provides general information about connecting the host system to the network.

The installation and connection procedures described in this section assume that you have acquired the required hardware components, including the EXOS VAX connecting cable, the transceivers, transceiver cables, and connectors.

NOTE

Before installing the EXOS 204, the jumper connecting the pins CA1 and CB1 on the UNIBUS backpanel must be removed. Otherwise, the EXOS 204 will not function properly.

3.2. SYSTEM ADDRESS FOR EXOS 204

The EXOS 204 uses two consecutive two-byte words of address space in the system. The factory-set default for this space address is 764000 (octal). Therefore, addresses 764000 and 764002 should not be used by any other device in the system. However, if there should be any contention for this address space, a different address space can be jumper-selected for the EXOS 204. The jumpers are described in Section 2. (If the EXOS 204 is assigned a new address, it must be supplied to the I/O driver when the driver is built during the network protocol software installation.)

The EXOS 204 also uses one interrupt vector. Excelan's EXOS 8000 Series network protocol software expects this vector to be at the address 770 (octal). If there should be a contention for this address, a different address can be specified when the I/O driver is built. No jumper change is required.

3.3. EXOS 204 INSTALLATION IN VAX 11/725 and VAX 11/730

The procedure for installing the EXOS 204 in VAX minicomputer models 11/725 and 11/730 is identical. A step-by-step description of the procedure is given below.

NOTE

Each unused slot in these systems always has a double-width NPG and Bus Grant continuity card installed in it. This card is called the "Bus Grant card" in the remainder of this section.

The following steps describe the installation procedure:

1. Switch off system power and remove the CPU cover panels.
2. Remove the Bus Grant card from the slot in which you want to install the EXOS 204 Intelligent Ethernet Controller.
3. Insert the EXOS 204 Intelligent Ethernet Controller in the C-D-E-F portion of the slot emptied in Step 2.
4. Plug the male end of the EXOS/VAX cable in to the Ethernet connector on the EXOS 204 Intelligent Ethernet Controller. Assure that the latches on the board have seated properly; this prevents the cable from being pulled out accidentally.
5. Route the EXOS/VAX cable to the back of the computer cabinet.
6. Bolt the bracket that holds the Ethernet connector to the I/O panel located at the back of the computer cabinet. If no space is available on the I/O panel, bolt the bracket to one of the vertical bars, using the spare connector bracket provided. (The Ethernet cable from the transceiver on the network will be plugged into this connector.)
7. Ensure that enough +15-volt power is available for the transceiver. Normally, the transceiver gets its power through the EXOS 204 intelligent Ethernet controller. Insufficient power can cause the VAX to crash. This can happen if a DMF32 multiport board is present or if other large power demands are placed on the system power supply by other devices. In such cases, use a transceiver multiplexer such as an EXOS 1130 or DEC DELNI.
8. Plug the Ethernet cable from the transceiver in to the Ethernet connector bolted to the I/O panel (or the vertical bar) in Step 6.

Assuming that the network hardware has already been installed, following Step 8 you are ready to install the network protocol software on your system.

3.4. EXOS 204 INSTALLATION IN VAX 11/750 and VAX 11/780

The procedure for installing the EXOS 204 in VAX minicomputer models 11/750 and 11/780 is identical. A step-by-step description of the procedure is given below.

NOTE

In the 11/750 and 11/780 models, each unused card slot originally comes with a small continuity card installed in it. In addition, pins CA1 and CB1 in each unused card slot are wire- However, you can replace any small continuity card with a regular double-width Bus Grant card and remove the wire link permanently. Whenever a continuity card is removed and an active board is installed, the wire link must also be removed with a

wire-unwrap tool. Conversely, whenever an active board is removed and a small continuity card re-installed, the wire link between pins CA1 and CB1 must also be re-installed. Wire link is not needed if a regular double-width Bus Grant card is re-installed.

The following steps describe the installation procedure:

1. Switch off system power and remove the CPU cover panels.
2. Remove the small continuity card or the regular Bus Grant card, as applicable, from the slot in which you want to install the EXOS 204 Intelligent Ethernet Controller.
3. If present, remove the wire link between pins CA1 and CB1 in the same slot. Use a wire-unwrap tool for this operation.
4. Insert the EXOS 204 Intelligent Ethernet Controller in the C-D-E-F portion of the card slot emptied in Step 2.
5. Plug the male end of the EXOS/VAX cable in to the Ethernet connector EXOS 204 Intelligent Ethernet Controller. Assure that the latches on the board have seated properly; this prevents the cable from being pulled out accidentally.
6. Route the EXOS/VAX cable to the back of the computer cabinet.
7. Bolt the bracket that holds the Ethernet connector to the I/O panel located at the back of the computer cabinet. If no space is available on the I/O panel, bolt the bracket to one of the vertical bars. using the spare connector bracket provided. (The Ethernet cable from the transceiver on the network will be plugged into this connector.)
8. Ensure that enough +15-volt power is available for the transceiver. Normally, the transceiver gets the power through the EXOS 204 Intelligent Ethernet Controller. Insufficient power for the transceiver can cause your VAX to crash. This can happen if a DMF32 multiport board is present or if other large power demands are placed on the system power supply by other devices. In such cases, use a transceiver multiplexer such as an EXOS 1130 or DEC DELNI.
9. Plug the Ethernet cable from the transceiver in to the Ethernet connector bolted to the I/O panel (or the vertical bar) in Step 7.

Assuming that the network hardware has already been installed, following Step 9 you are ready to install the network protocol software on your system.

NOTE

If the EXOS 204 Intelligent Ethernet Controller is removed from its slot, either a double-width Bus Grant or a small continuity card must be installed in that slot. Furthermore, if a small card is installed, the wire-link between pins CA1 and CB1 must also be installed. The wire link is not needed if a regular double-width Bus Grant card is used.

3.5. CONNECTING TO THE NETWORK

The network hardware should be installed according to the directions supplied with the individual components and in accordance with the Ethernet specifications jointly published by Xerox, Intel, and Digital Equipment Corporation.

Chapter 4
SERVICE INFORMATION

4.1. INTRODUCTION

Prior to shipping, each EXOS 204 Ethernet Intelligent Ethernet Controller board is thoroughly tested and exercised both at the component and the system level. However, since it is not possible to simulate every possible situation that might exist on the network, occasionally you might encounter performance problems with the EXOS 204. For such rare cases, Excelan provides prompt technical service assistance. After hearing from you, our technical support personnel will discuss the problem with you over the telephone. Quite often, the problem is a simple one and can be resolved during such discussions. At other times, it may be necessary for you to ship the board back to the factory for repair or replacement.

This chapter provides information on how to obtain service assistance. Note that when communicating with Excelan Service Center, you might need to provide or refer to information included in Appendices A and B of this manual.

Appendix A presents an assembly diagram of the EXOS 204 that shows the locations of the EXOS 204 serial number, assembly or part number, revision levels, various components, and jumpers. This appendix also contains a jumper table that shows functions of various jumpers.

Appendix B provides a set of EXOS 204 schematic diagrams.

4.2. HOW TO USE SERVICE ASSISTANCE

The following is a summary of procedure for using Excelan's service assistance. For detailed information, please refer to the "Warranty/Service Information" document shipped with your EXOS 204.

If you encounter any problem with your EXOS 204 and you or your system administrator cannot resolve it, please contact

Customer Service Center
Excelan, Inc.
2180 Fortune Drive
San Jose, CA 95131
(408) 434-2285

For prompt assistance the Service Center will require the following information. Please have it ready.

- Your Company name
- Technical contact
- Company address
- Telephone number
- Product name, part number, and serial number
- Your purchase order number or service contract number

The Customer Service staff will then discuss the problem you are experiencing with the EXOS 204. They will assist you in isolating the fault and fixing it if possible.

If the problem cannot be fixed, the service staff will provide you with a Return Material Authorization (RMA) number. You should then securely pack the unit in its original or similar packing and return it to to Excelan at the address given above. Please refer to the "Warranty/Service Information" document for detailed service terms.

At this point, depending on whether or not the unit is under warranty or extended warranty, the service staff will be able to advise you of any applicable charges for the service.

Appendix A
COMPONENT LOCATION

A.1. INTRODUCTION

Figure A-1 show the location of main components and various jumpers on the EXOS 204 board. Table A-1 lists the function of various jumpers.

A.2. I/O PORT ADDRESS ASSIGNMENT

The UNIBUS addresses of I/O ports A and B are word addresses. For selection of these addresses, each of the 8 jumpers in J18 and each of the 3 jumpers in J16 must be appropriately selected. **An absent jumper selects a 1 value and an installed jumper selects a 0 value.** Address bits 0 and 1 are not selectable – they are always zero. Currently, address bit 0 is always 0 (zero). Bit 1 selects port A when 0, and port B when 1.

Address bits 13 through 17 are not selectable; they are always 1. As shipped from the factory, except J16-1, all jumpers are installed. Consequently the UNIBUS addresses 760000 and 777774 (octal) corresponding to 3FE800 and 3FE802 (Hexadecimal), are selected for I/O ports A and B respectively. Relative address line positions in jumpers J16 and J18 are as follows:

J16:

Jumper No. --------->	1	2	3
Bit represented --->	12	11	10

J18:

Jumper No. --------->	1	2	3	4	5	6	7	8
Bit represented --->	9	8	7	6	5	4	3	2

Table A-1: EXOS 204 Jumpers

Jumper	Function (when jumper is installed)			Factory Setting
J2	Invoke the EPROM-resident Monitor program on power-up or reset			Absent
J3	DMA with burst capability present			Installed
J4	Disable SQE (Heartbeat) check, Version 1.0 mode			Installed
J6	Used in conjunction with J9; specifies available RAM:			Absent
	J6	**J9**	**RAM**	
	Absent	Absent	128K (factory setting)	
	Installed	Absent	256K	
	Absent	Installed	512K	
	Installed	Installed	Reserved	
J7	Boot from network			Absent
J8	Disable Carrier Sense			Absent
J9	See description under J6.			Absent
J10	Ground IRO from iSBX			Absent
J11	Ground IRO from iSBX			Absent
J12	27256 user EPROMS			Absent
J13	2764 or 27128 user EPROMs			Installed
J14	27256 Kernel EPROMs			Absent
J15	2764 or 27128 Kernel EPROMs			Installed
J16	(3 jumpers) bits 10-12 of I/O port address (Installed = 0; absent = 1.)			Absent J16-2; others installed.
J17-1	Select DMA burst length			Installed
J17-2	Select DMA burst length			Absent
	J17-1	**J17-2**	**burst-length**	
	Installed	Installed	2	
	Installed	Absent	4	
	Absent	Installed	8	
	Absent	Absent	16	
J17-3	Enable bus timeout			Absent
J18	(8 jumpers) bits 2-9 of I/O port address			All installed (0)
J19	Configure UNIBUS interrupt levels*			
J20	Configure UNIBUS interrupt levels*			

*Refer to Table 2-2 for details.

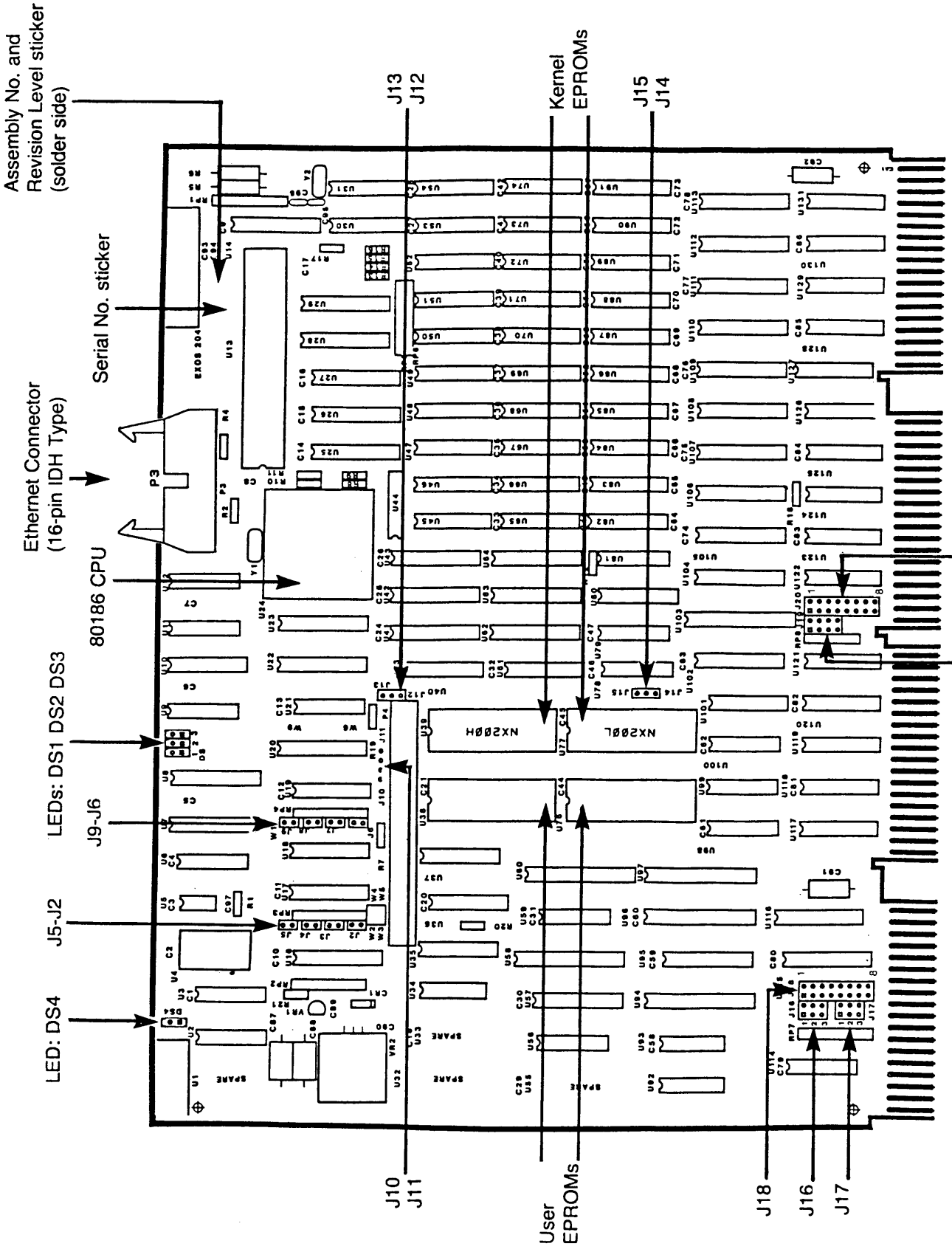
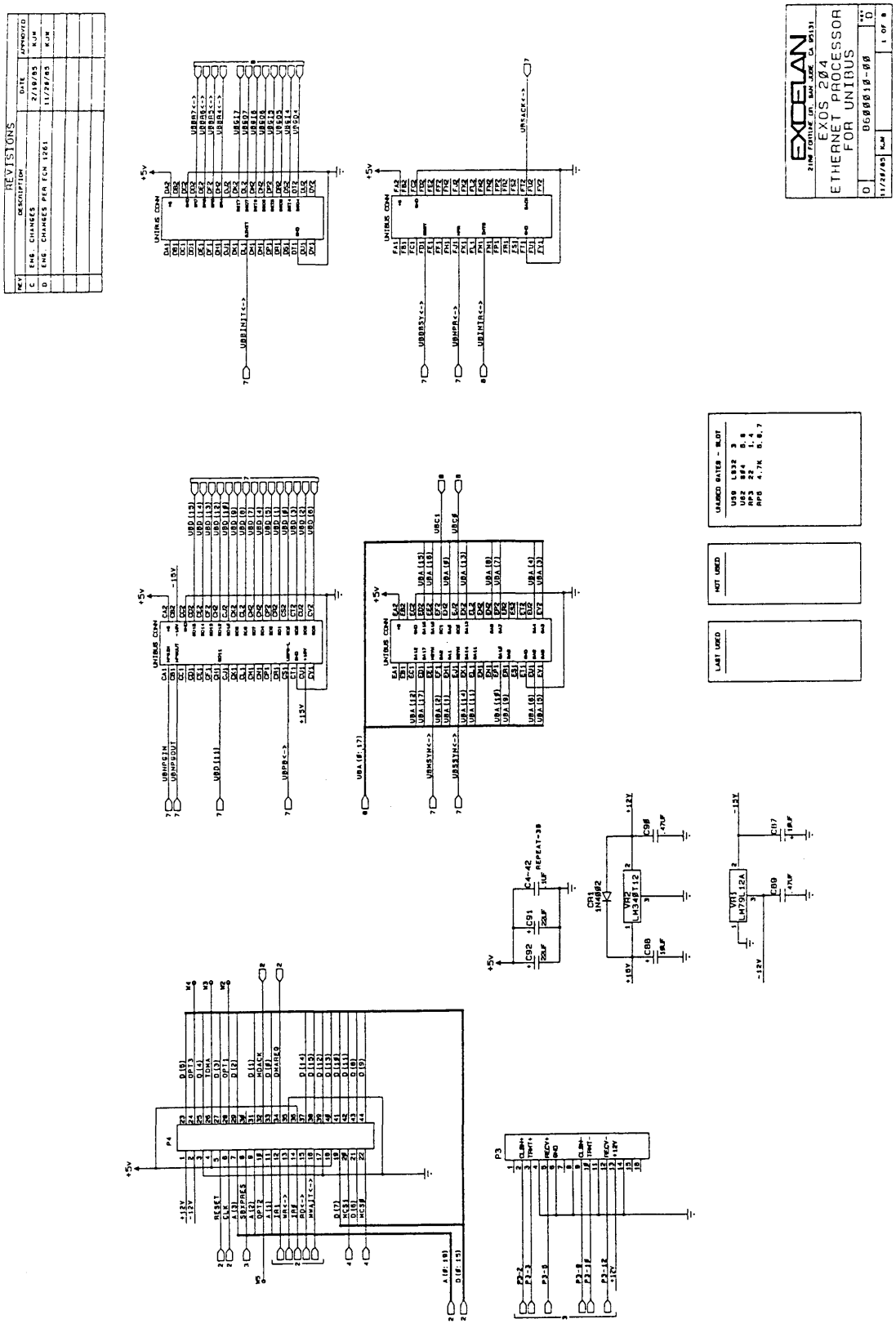


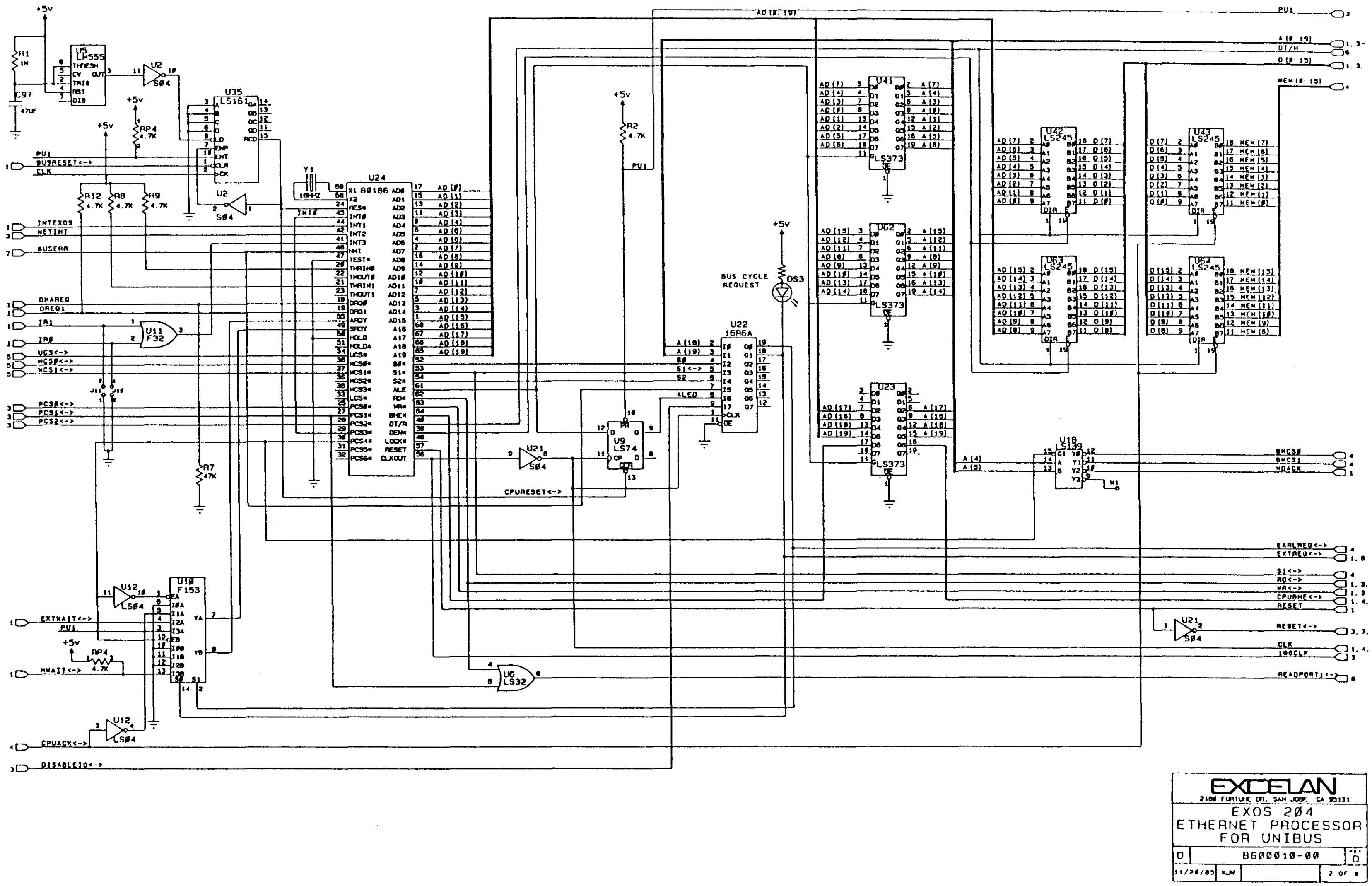
Figure A-1: EXOS 204 Component Layout

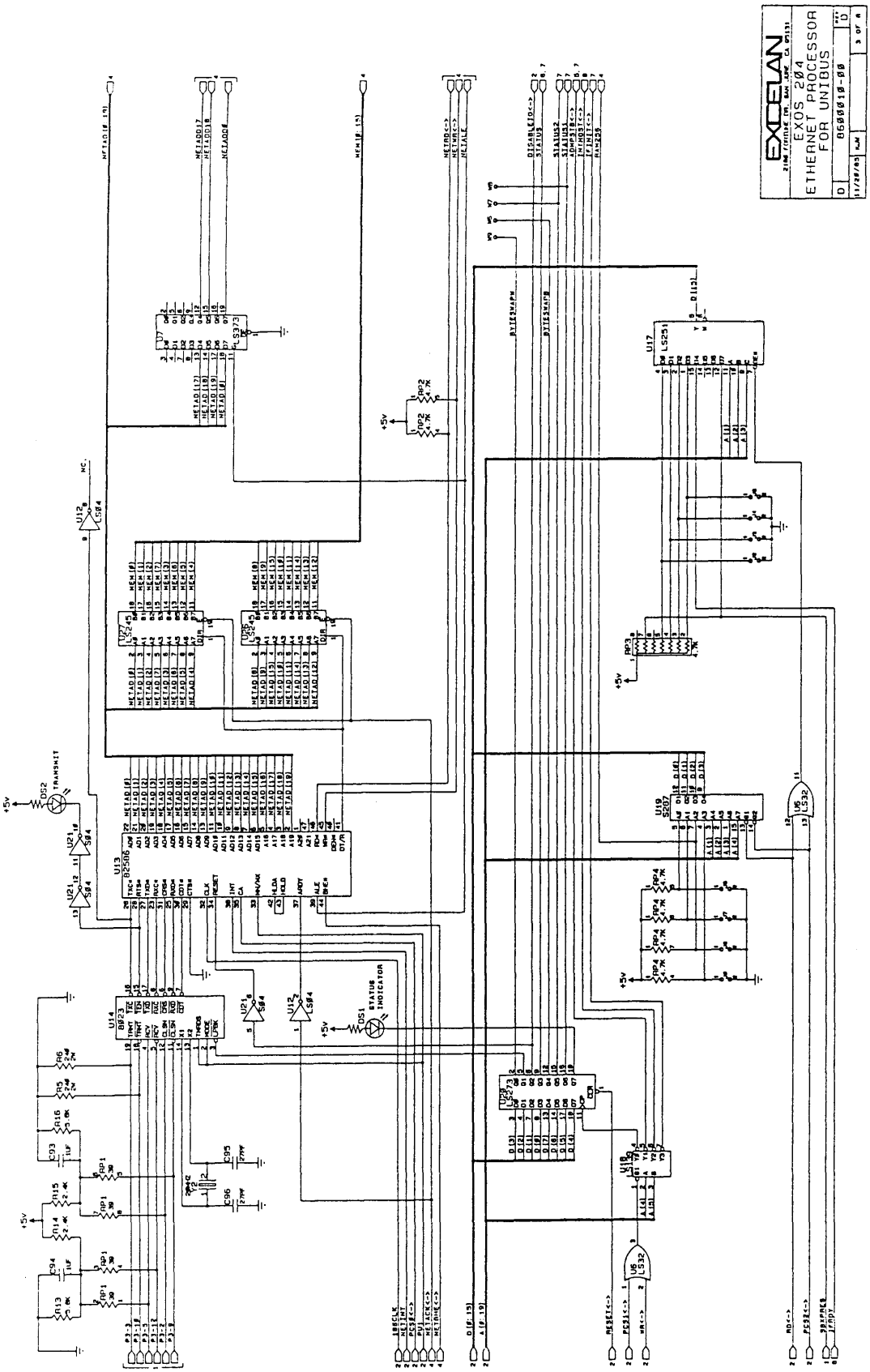
Appendix B
EXOS 204 SCHEMATICS

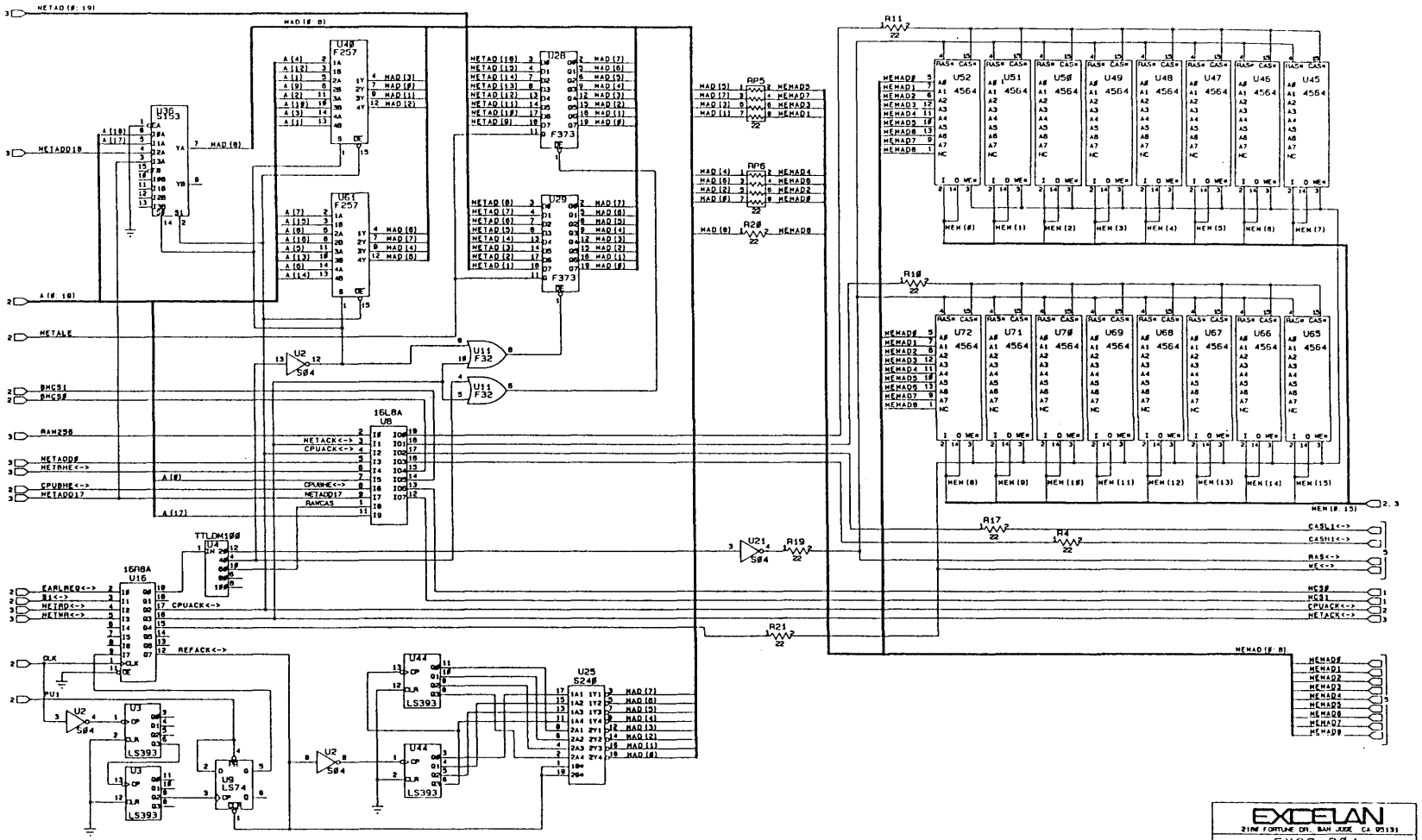
B.1. INTRODUCTION

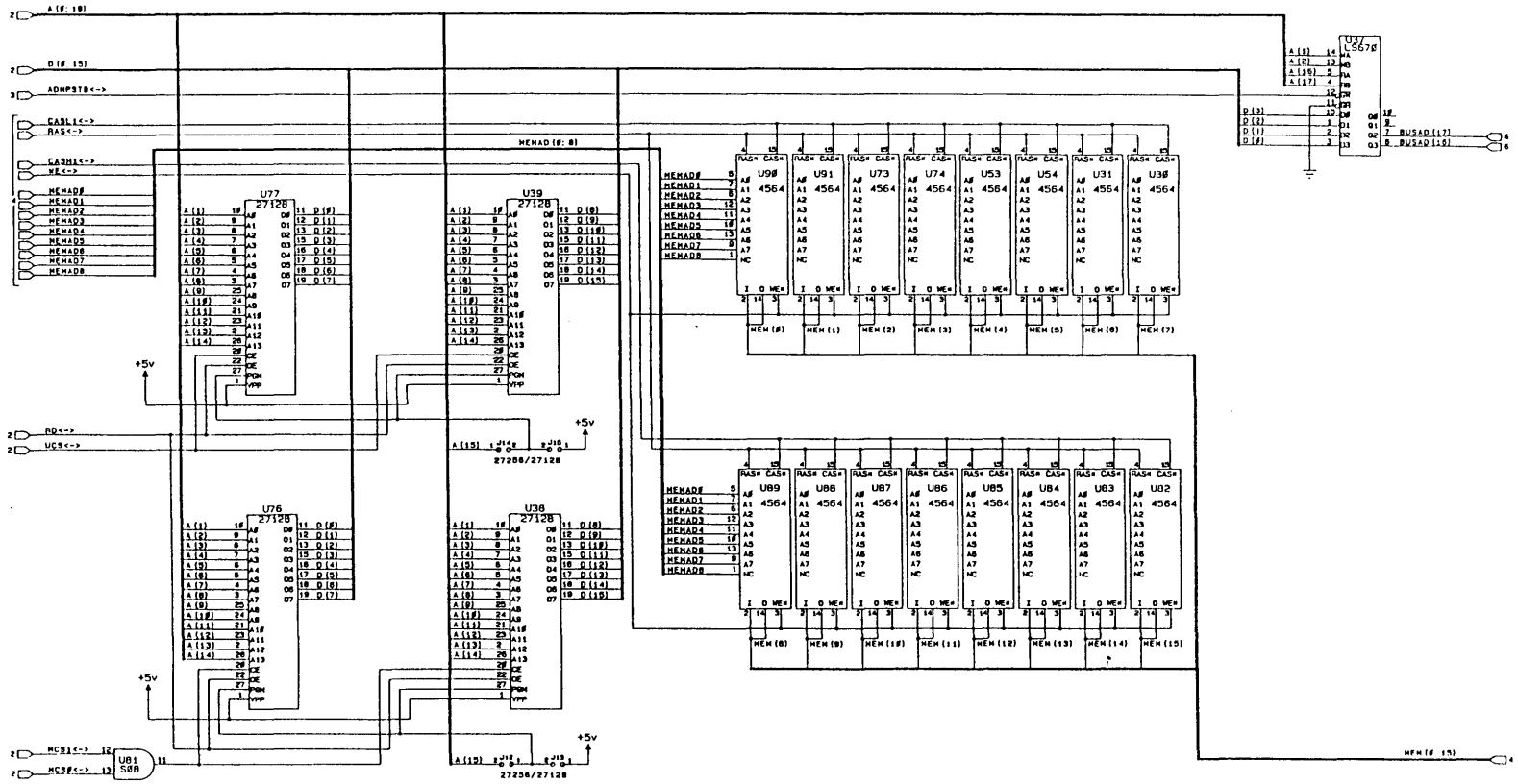
The schematics for the EXOS 204 Intelligent Ethernet Controller are shown on the following pages.


REVISIONS
EXCELAN
EXOS 204
ETHERNET PROCESSOR
FOR UNIBUS
LAST USED
NOT USED

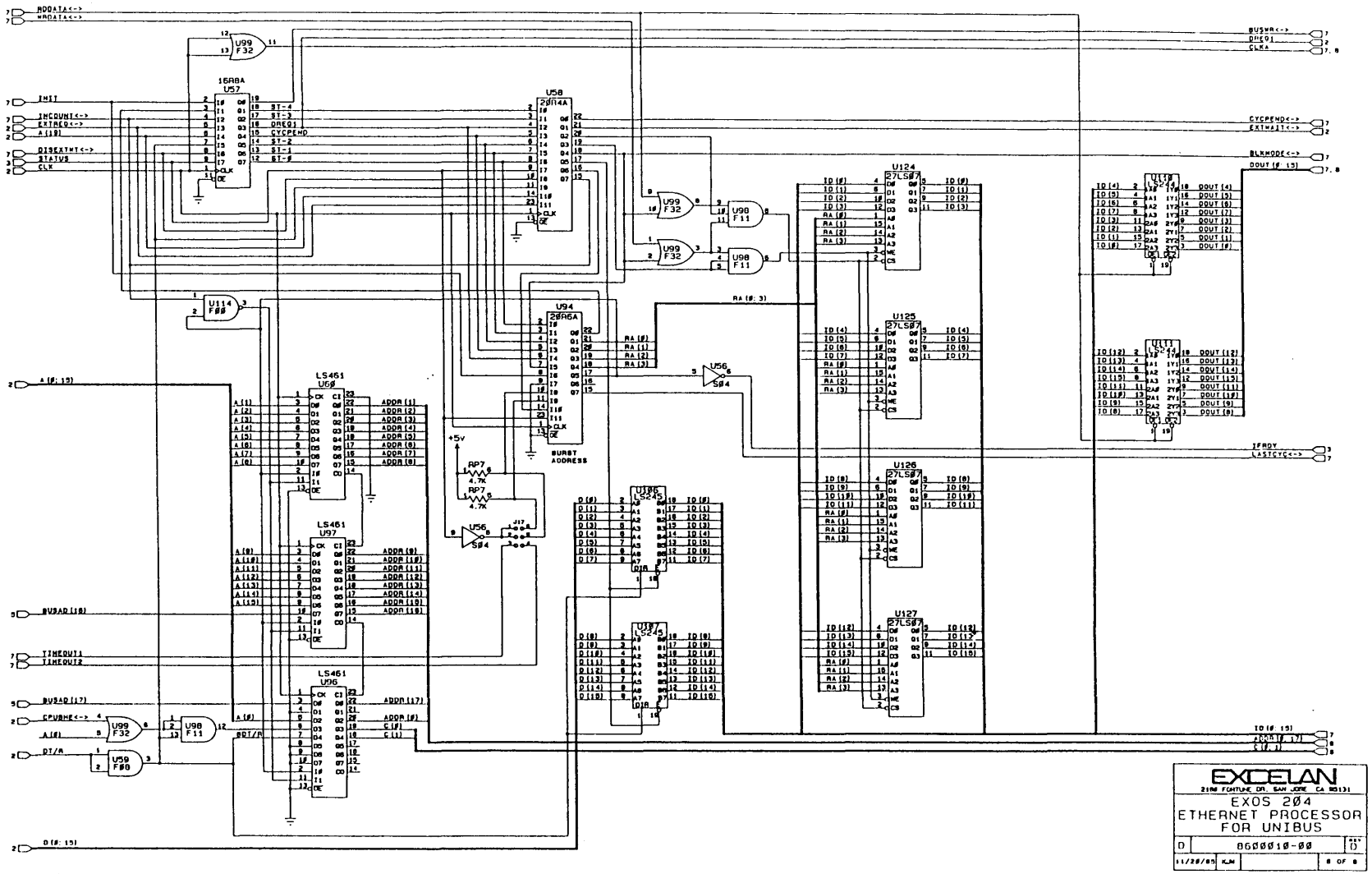

EXCELAN
EXOS 204
ETHERNET PROCESSOR
FOR UNIBUS
2 OF 8

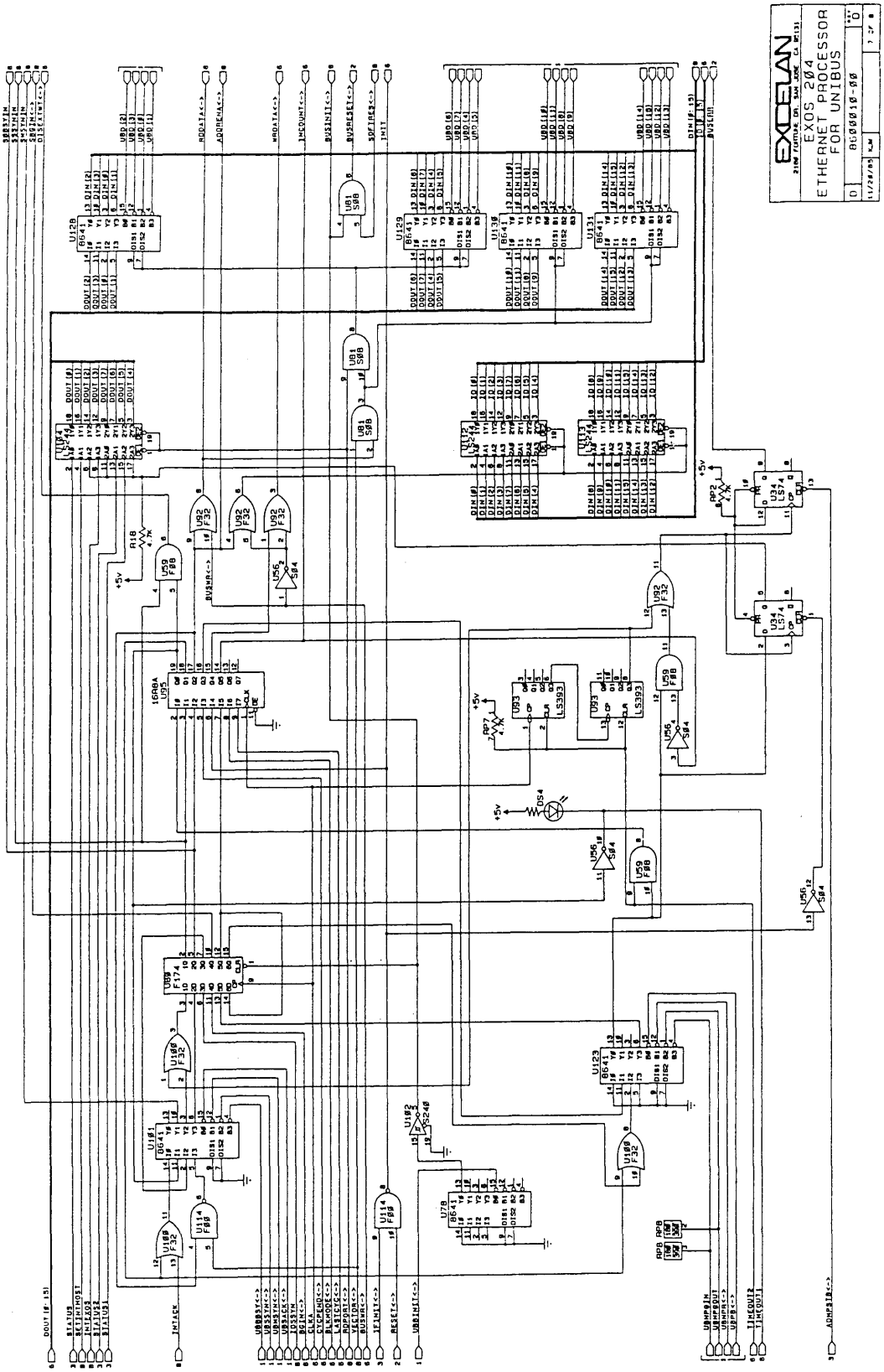

EXCELAN
EXOS 204
ETHERNET PROCESSOR
FOR UNIBUS

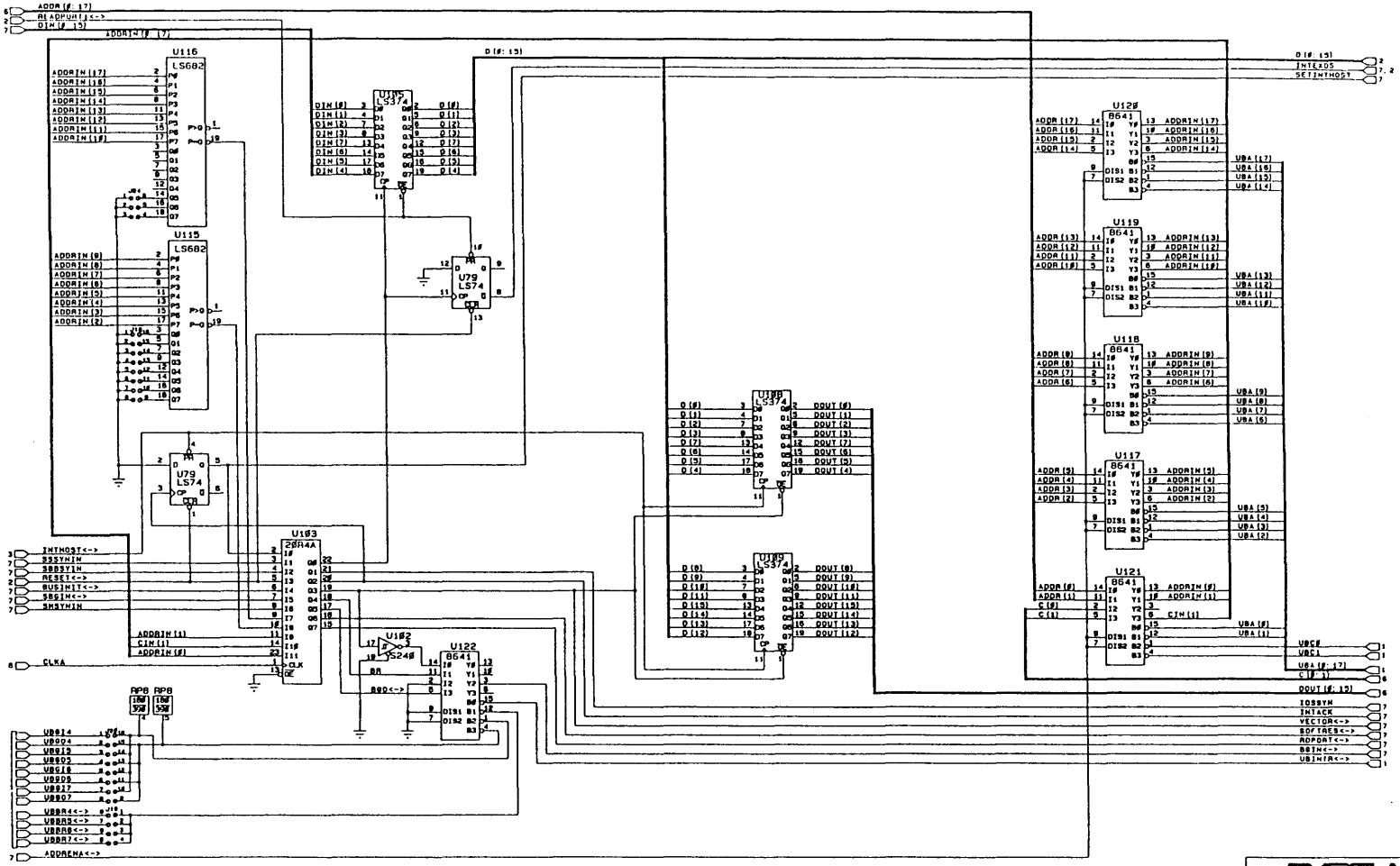

EXCELAN
2180 FORTUNE DR. SAN JOSE CA 95131
EXOS 204
ETHERNET PROCESSOR
FOR UNIBUS
D
8600010-00
11/28/85
KJM
4 OF 8



EXCELAN			
2180 FORTUNE DR. SAN JOSE, CA 95131			
EXOS 2#4 ETHERNET PROCESSOR FOR UNIBUS			
D	06###1#-##		### D
11/28/85	K.H		5 OF #


EXCELAN
2180 FORTUNE DR. SAN JOSE CA 95131
EXOS 204
ETHERNET PROCESSOR
FOR UNIBUS
D
860010-00
11/28/85
KJH
8 OF 8


EXCELAN
EXOS 204
ETHERNET PROCESSOR
FOR UNIBUS


EXCELAN
2180 FORTUNE DR. SAN JOSE CA 95131
EXOS 204
ETHERNET PROCESSOR
FOR UNIBUS
D
860001Ø-ØØ
D
11/20/85
KJH
8 OF 8

Appendix C
TRANSCEIVER CABLE CONNECTOR PIN-OUT

C.1. INTRODUCTION

The EXOS 204 board is compatible with IEEE 802.3 and Ethernet (Version 1.0 and 2.0) transceivers. Therefore, all standard transceiver cables available commercially are suitable for use with the EXOS 204 board.

For reference, the pin assignment for the cable connector on the EXOS 204 board is shown in Table C-1; the pin numbers are illustrated in Figure C-1.

Table C-1: EXOS 204 Pin Assignment for the Transceiver Cable Connector

Pin #	Function	Polarity
2	Collision	(–)
3	Collision	(+)
4	Transmit	(–)
5	Transmit	(+)
8	Receive	(–)
9	Receive	(+)
10	Power	+12V
11	Power	Gnd
6,7,12,15	Signal	Gnd
1,14,16	Not used	

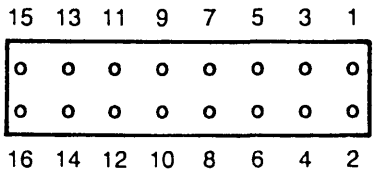


Figure C-1: Pin Layout for Transceiver Connector on EXOS 204

READER COMMENT FORM

At Excelan, we endeavor to provide thorough and accurate documentation for our products. We invite your comments about this manual so that we may improve the documentation even further. Please take a few minutes to rate this manual, note any comments, and mail this postage-paid form.

Please restrict your comments to this manual only. If you have other product-related comments, contact Customer Service at (408) 434-2285.

	Excellent	**Good**	**Adequate**	**Fair**	**Poor**
Fulfills needs	☐	☐	☐	☐	☐
Readability (style)	☐	☐	☐	☐	☐
Organization	☐	☐	☐	☐	☐
Technical accuracy	☐	☐	☐	☐	☐
Presentation (format)	☐	☐	☐	☐	☐
Overall quality	☐	☐	☐	☐	☐

Your Name _____ Date _____

Title _____ Phone _____

Company/Department _____

Address _____

City _____ State _____ Zip _____

Do you require a written reply? Yes ☐ No ☐

Comments: _____

_____

_____

_____

_____

_____

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 7391 SAN JOSE, CA

POSTAGE WILL BE PAID BY ADDRESSEE

Excelan, Inc.
2180 Fortune Drive
San Jose, CA 95131-9968

Attention: Technical Publications