ECMA

EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-33

FOR

TRACK FORMAT CHARACTERISTICS OF INTERCHANGEABLE 6-DISK PACKS

September 1971

ECMA

EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-33

FOR

TRACK FORMAT CHARACTERISTICS OF INTERCHANGEABLE 6-DISK PACKS

September 1971

BRIEF HISTORY

On April 30, 1965, ECMA adopted their Standard ECMA-6 for
a 7 Bit Coded Character Set. In the form adopted, it included
no proposals for implementation in media which were delibera-
tely left as the subject for specific standards.

Standard ECMA-32 defines the Mechanical, Physical and Magnetic
Characteristics for Interchangeable 6 Disk Packs.

This Standard ECMA-33, prepared by ECMA TC16, is directed to
the Track Format Characteristics for the same 6 Disk Packs.

Adopted by the General Assembly as Standard ECMA-33 on
June 2 - 3, 1971.

FOREWORD

This Standard, ECMA-33 describes the recording format for use
with the 6 Disk Pack defined in Standard ECMA-32.

No attempt is made to solve problems of data and file structure
standardization as the standard restricts itself to definition
of gaps and hardware detected codes.

The format chosen is a variable data length type, which is al-
ready in general use in the computer industry at the time of
writing this standard. Therefore, this standard serves to
quantify current practice and places an equal responsibility
on all manufacturers to meet the same requirements for inter-
change. This format is designed to handle eight bit characters
(bytes). However, in this standard the Standard ECMA-6 for a
7 Bit Coded Character Set is specified, with each seven bit
character occupying one byte position.

It should be noted that in this standard, plain binary numbers
in eight bit bytes, are used in the control fields to define the
lengths of the variable fields in terms of numbers of bytes.

Two Appendices describe the calculation of permissible speed
variation and track capacity.

CONTENTS

CONTENTS (cont'd)

1. GENERAL REQUIREMENTS

1.1 Rotation Speed and Clock Frequency

The total tolerance on rotation speed + clock frequency shall not exceed 2,4% (see Appendix A).

1.2 Mode of Recording

The mode of recording shall be double frequency where every bit cell has a clock transition. A one is represented by a transition between two clocks.

At the nominal rotational speed of 2400 rpm the all ZERO pattern consists of $1,25.10^6$ transitions per second nominally, and an all ones pattern consists of $2,50.10^6$ transitions nominally.

1.3 Index

A track has a beginning and an end indicated by the Index pulse.

1.4 Track Capacity

The capacity of a track is 31250 ± 750 bits. (See Appendix B).

1.5 Track Layout

Figure 1 shows the general track layout.

2. DEFINITION OF TERMS

2.1 Sector

A track is divided into sectors. A sector may be further subdivided.

2.2 Home Address

The Home Address contains information which defines the physical location and characteristics of a track.

2.3 Count

The Count contains information which defines the physical location and characteristics of a sector.

2.4 Key

The key, if used, will contain data.

2.5 Data Block

Part of a sector in which data is recorded.

2.6 Gap

A gap is the space between the various divisions of
a track.

2.7 Byte (or Octet)

A byte (or octet) consists of 8 serial bits, identified
B8 to B1 with B8 as most significant and recorded first.

2.8 Hexadecimal Notation

$(00)_{16}$ denotes a byte (or octet) with B8 to B1 = 00000000

$(FF)_{16}$ "   "   "   ("   "   ) "   "   "   " = 11111111

$(0E)_{16}$ "   "   "   ("   "   ) "   "   "   " = 00001110

$(CC)_{16}$ "   "   "   ("   "   ) "   "   "   " = 11001100

3. DETAILED DESCRIPTION OF TRACK LAYOUT

3.1 Sector 0

The first sector following Index is unique in that
it contains a Home Address and will therefore be described
separately.

3.1.1 Index Gap (see Fig. 2)

3.1.1.1 Starting from Index a gap of 30 bytes $(00)_{16}$ is
recorded as detailed in Fig. 2. Because of toler-
ances on Index when reading, this gap has a length
of 30 $\pm$ 14 bytes of which the first 14 may be un-
readable.

3.1.2 Home Address (see Fig. 2)

The Home Address consists of 14 bytes as follows:

3.1.2.1 Synchronization -(6 bytes) as follows:

$(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(FF)_{16}$ $(0E)_{16}$

3.1.2.2 F - Flag (1 byte) - is used to indicate defective
and alternative tracks. The significance of the bit
in this byte are a follows:

The first two bits (B8 and B7) are always zero.
B6 to B3 are reserved for future standardization
and are all ZERO.

B2 B1 = 00 indicates good original track
B2 B1 = 01   "   "   alternative track
B2 B1 = 10   "   defective track, alternative
                        has been allocated
B2 B1 = 11   "   defective track,
                        no alternative has been
                        allocated

3.1.2.3 C - Cylinder (2 bytes) - These specify in binary
the address of the cylinder. The first byte is
always ZERO. The second byte can have any value
in the range 0 to 202.

3.1.2.4 H - Head (2 bytes) - These specify in binary the
address of a track within a cylinder. The first
byte is always ZERO. The second byte can have any
value in the range 0 to 9.

3.1.2.5 CRC - Cyclic Redundancy Check (2 bytes) - These
consist of the ONES complement of the remainder
obtained after dividing the previous five in-
formation bytes by the code polynominal $(1 + x^{16})$.
They can be used for error checking when reading.

3.1.2.6 The Home Address ends with one byte $(CC)_{16}$.

3.1.3 An eleven byte gap is recorded between the end of the
Home Address and the start of the count. This gap
may subsequently become undefined because of repeated
writing operations. The gap will be written initially
as $(00)_{16}$.

3.1.4 Count of Sector 0 (see Fig. 3)

The count consists of 18 bytes as follows:

3.1.4.1 Synchronization - (6 bytes) as follows:

$(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(FF)_{16}$ $(0E)_{16}$

3.1.4.2 F - Flag (1 byte) - This is used for certain
control and checking operations and is also used
to indicate defective and alternative tracks. The
significance of the bits in this byte are as
follows:

B8   This is ZERO for Sector 0, see Section 3.2.1
for the use of this bit in other sectors.

B7 This is ZERO for Sector 0, see section 3.2.1 for the use of this bit in other sectors.

B6 to B3 are reserved for future standardization and are all ZERO.

B2 and B1 The state of these bits must always be the same as those in the Home Address (see section 3.1.2.2).

3.1.4.3 C and H - Cylinder and Head (4 bytes) - These bytes are identical to those in the Home Address except when appearing on defective or alternative tracks. On a defective track C and H contain cylinder and head number of the alternative track which re-places it. On an alternative track C and H contain cylinder and head number of the defective track which it replaces.

3.1.4.4 S - Sector (1 byte) - It is used to identify sectors on the track.

3.1.4.5 KL - Key Length (1 byte) - This specifies in bi-nary the number of information bytes in the Key.

3.1.4.6 DL - Data Length (2 bytes) - These specify in binary the number of information bytes in the data block.

3.1.4.7 CRC - Cyclic Redundancy Check (2 bytes) - These consist of the ONES complement of the remainder obtained after dividing the previous nine inform-ation bytes by the code polynominal $(1 + x^{16})$. They can be used for error checking when reading.

3.1.4.8 The Count ends with one byte $(CC)_{16}$.

3.1.5 An eleven byte gap is recorded between end of the Count and the start of the key. This gap may sub-sequently become undefined because of repeated writing operations. The gap will be written initially as 9 bytes of $(FF)_{16}$ followed by 2 bytes of $(00)_{16}$.

3.1.6 Key (see Fig. 4)

The key consists of (KL + 9) bytes, where KL is the number of information bytes (see 3.1.4.5). If KL in the preceding Count is ZERO the Key and the following gap (3.1.7) are omitted and the Count is followed by the Data Block (see section 3.1.8). Otherwise the key is as follows:

3.1.6.1 Synchronization (6 bytes) as follows:

$(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(FF)_{16}$ $(0E)_{16}$

3.1.6.2 Information – A number of information bytes as specified in the KL portion of the preceding Count. The data in these bytes shall be recorded in ECMA 7 bit code. Bits b7 to b1 of the ECMA 7 bit code (Standard ECMA-6) are recorded as B7 to B1 as defined in 2.7, B8 is always ZERO.

3.1.6.3 CRC-Cyclic Redundancy Check (2 bytes) – These consist of the ONES complement of the remainder obtained after dividing the previous information bytes by the code polynominal $(1 + x^{16})$. They can be used for error checking when reading.

3.1.6.4 The Key ends with one byte $(CC)_{16}$.

3.1.7 An eleven byte gap is recorded between the end of the Key and the start of the Data Block. The gap may subsequently become undefined because of repeated writing operations. The gap will be written initially as 9 bytes of $(FF)_{16}$ followed by 2 bytes $(00)_{16}$.

3.1.8 Data Block (see Fig. 5)

The Data Block consists of (DL + 9) bytes, where DL is the number of information bytes (see 3.1.4.6).

If DL in the preceding Count is ZERO, the Data Block does appear in rudimentary form.

The data Block is as follows:

3.1.8.1 Synchronization (6 bytes) as follows:

$(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(FF)_{16}$ $(0E)_{16}$

3.1.8.2 Information – A number of information bytes as specified in the DL portion of the preceding Count. The data in these bytes shall be recorded in ECMA 7 bit code. The bits b7 to b1 of the ECMA code are recorded in B7 to B1 as defined in 2.7, B8 is always ZERO. When DL is ZERO one byte $(00)_{16}$ is recorded.

3.1.8.3 CRC – Cyclic Redundancy Check (2 bytes) – These consist of the ONES complement of the remainder obtained after dividing the previous information bytes by the code polynominal $(1 + x^{16})$. They can be used for error checking when reading: if DL = 0 these two bytes are missing.

3.1.8.4 The Data Block ends with one byte $(CC)_{16}$.
If DL = 0 this byte is also missing.

3.1.9 A minimum gap of 21 bytes is recorded between the end
of the Data Block and the start of the next sector.
This gap is written initially as 21 bytes of $(FF)_{16}$.
The gap must be of sufficient length to prevent over-
writing of the following sector under worst case
conditions of disk speed and oscillator frequency.
This gap is therefore extended so that its length is:

$$21 + \left(\frac{537}{512} - 1\right) \cdot \left(KL + DL\right)$$

any fraction is truncated.

KL - is the number of information bytes in the Key

DL - is the number of information bytes in the Data
Block

This gap may subsequently become undefined because of
repeated writing operations.

3.2 Subsequent Sectors

3.2.1 Count (see Fig. 6)

The count of subsequent sectors consists of 20 bytes
as follows:

3.2.1.1 Synchronization (8 bytes) as follows:

$(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(00)_{16}$ $(FF)_{16}$

$(FF)^{*}_{16}$ $(FF)^{*}_{16}$ $(0E)_{16}$

where $(FF)^{*}_{16}$ denotes that the clock transitions
following the first five data transitions of each
of these two bytes are missing.

3.2.1.2 F - Flag (1 byte) - This is used in each Count for
certain control and checking operations and can be
used to indicate defective and alternative tracks.
The significance of the bits in this byte are as
follows:

B8 = 1 for the first sector following the Sector 0
and alternate sectors thereafter, and

B8 = 0 for the other sectors.

B7=1 indicates that the sector is an overflowing sector, i.e. the information in the associated Data Block is continued in another sector. Otherwise this bit must be 0.

B6 to B3 are reserved for future standardization and are all ZERO.

B2 to B1 see Count of Sector 0 (section 3.1.4).

3.2.1.3 The remainder of the Count is as described in sections 3.1.4.3 to 3.1.4.8.

3.2.2 The remainder of the Sector is as described in sections 3.1.5 to 3.1.9 except for the last sector.

3.3 Last Sector

3.3.1 Count (see 3.2.1)

3.3.2 The remainder of the last sector except for the last gap is described in sections 3.1.5 to 3.1.8.

3.3.3 The gap following the last sector will be approximately 30 bytes if the track is filled to maximum capacity (see appendix B) under conditions of maximum rotational speed and minimum clock frequency. Due to Index tolerance when reading, this gap may be further reduced by a factor of 14 bytes.
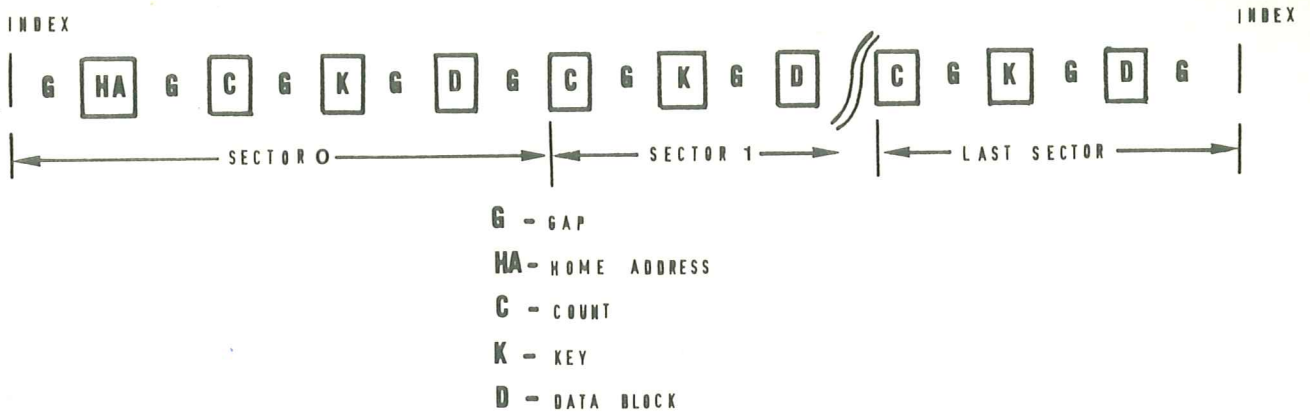
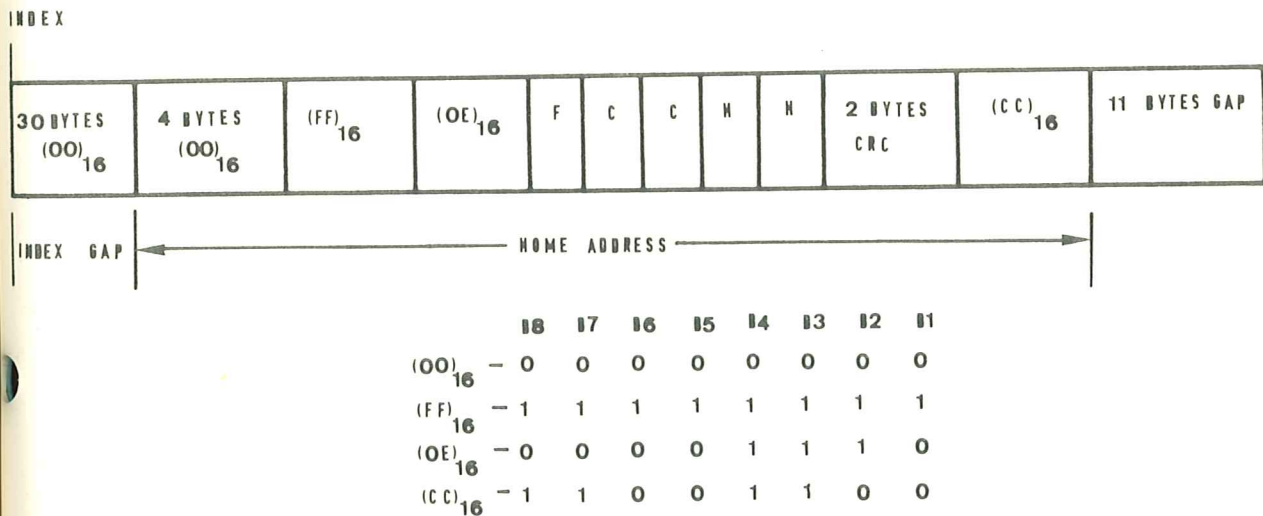INDEX   INDEX

| G | HA | G | C | G | K | G | D | G | C | G | K | G | D | ∫∫ | C | G | K | G | D | G |

|←——————— SECTOR 0 ———————→|←——— SECTOR 1 ———→|←——— LAST SECTOR ———→|

G — GAP
HA — HOME ADDRESS
C — COUNT
K — KEY
D — DATA BLOCK

Fig.1

INDEX

| 30 BYTES (00)$_{16}$ | 4 BYTES (00)$_{16}$ | (FF)$_{16}$ | (OE)$_{16}$ | F | C | C | H | H | 2 BYTES CRC | (CC)$_{16}$ | 11 BYTES GAP |

|← INDEX GAP →|←———————————— HOME ADDRESS ————————————→|

	B8	B7	B6	B5	B4	B3	B2	B1
(00)$_{16}$ —	0	0	0	0	0	0	0	0
(FF)$_{16}$ —	1	1	1	1	1	1	1	1
(OE)$_{16}$ —	0	0	0	0	1	1	1	0
(CC)$_{16}$ —	1	1	0	0	1	1	0	0

Fig.2

| 4 BYTES (00)$_{16}$ | (FF)$_{16}$ | (OE)$_{16}$ | F | C | C | H | H | S | KL | DL | DL | 2 BYTES CRC | (CC)$_{16}$ | 11 BYTES GAP |

|←———————————————— COUNT OF SECTOR 0 ————————————————→|

Fig.3

4 BYTES (00)$_{16}$	(FF)$_{16}$	(0E)$_{16}$	(KL) BYTES INFORMATION	2 BYTES CRC	(CC)$_{16}$	11 BYTES GAP

|←————————————————————————— KEY —————————————————————————→|

Fig.4

4 BYTES (00)$_{16}$	(FF)$_{16}$	(0E)$_{16}$	(DL) BYTES INFORMATION	2 BYTES CRC	(CC)$_{16}$	21 BYTES MINIMUM GAP

|←————————————————————— DATA BLOCK —————————————————————→|

Fig.5

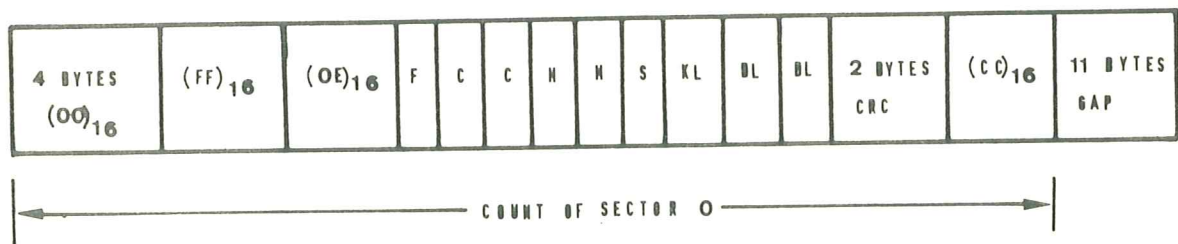| 4 BYTES (00)$_{16}$	(FF)$_{16}$	(FF)$_{16}$ *	(FF)$_{16}$ *	(0E)$_{16}$	F	C	C	H	H	S	KL	DL	DL	2 BYTES CRC	(CC)$_{16}$	11 BYTES GAP

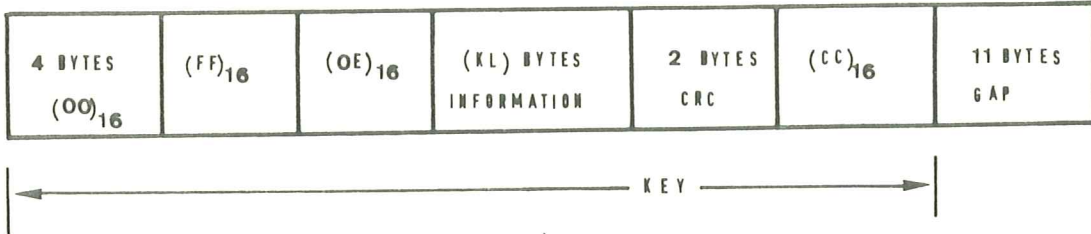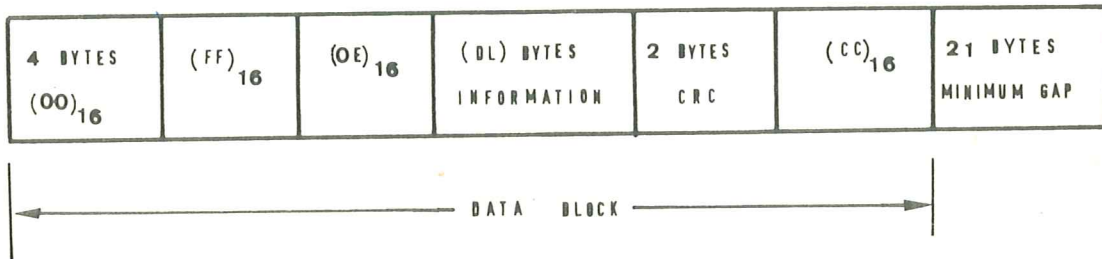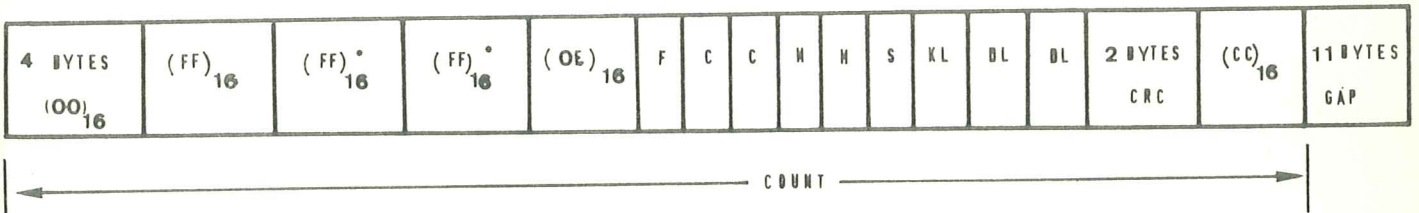|←—————————————————————————————— COUNT ——————————————————————————————→|

* The clock transition is missing from the first five bits of each of these two bytes.

Fig.6

APPENDIX A

Rotational Speed and Clock Frequency Tolerance

If the nominal record length is L, the minimum record length is L_1, the maximum record length is L_2 and the tolerance is x:

From current practice $\dfrac{L_2}{L_1} = 1,049$

and $L_1 = L - x$

$L_2 = L + x$

therefore $\dfrac{L + x}{L - x} = 1,049$

$L + x = 1,049L - 1,049x$

and solving for x

$$x = \frac{0,049}{2,049} \cdot L$$

$$= 2,39\% \text{ of } L$$

Hence the figure 2,4% is used.

APPENDIX B

The data capacity under worst case conditions is 3686 bytes.

The overhead due to Index gap, Home Address and End of Track gap have been deducted from the track capacity to arrive at this capacity.

The number of bytes required for the sectors is given by the following formula.

Number of bytes for each sector			
Sectors (except for last)		last sector	
without key	with key	without key	with key
$61 + \dfrac{537\ DL}{512}$	$81 + \dfrac{537\ (KL+DL)}{512}$	$61 + DL$	$81+KL+DL$

The term 61 of the formula consists of:
- 21 bytes minimum gap which is used for write/read switching
- 20 bytes for the count area (see 3.2.1)
- 11 bytes gap between Count (or Key) and Data block (see 3.1.7)
- 6 bytes synchronizing pattern in front of the Data block (see 3.1.8.1)
- 2 bytes CRC of the Data Block (see 3.1.8.3)
- 1 byte $(CC)_{16}$ at the end of the Data block (see 3.1.8.4)

The term 81 results as follows:
- 61 bytes as above
- 11 bytes gap between Count and Key (see 3.1.7)
- 6 bytes synchronizing pattern in front of the Key (see 3.1.8.1)
- 2 bytes CRC of the Key (see 3.1.8.3)
- 1 byte $(CC)_{16}$ at the end of the Key (see 3.1.8.4)