DATA TECHNOLOGY CORPORATION

DTC-520A CONTROLLER SPECIFICATION

PRELIMINARY

July 30, 1982

ADDENDUM 1: (Prototype Boards ONLY)

Features not implemented on this board:

1. 512 Byte/Sector
2. Copy Command Class 1, Opcode ØØ
3. RAM Diag. Class 7, Opcode ØØ
4. Read ID Class 7, Opcode Ø2
5. Drive Diag. Class 7, OPcode Ø3
6. Seagate and Tandom Fast Step algorithm SEEK.

Discrepancy on the board layout:

1. LED designators on PC Board are backwards.

Additional codes for the LED display:

1. LED code 4Ø Hex = Controller is in the idle loop.
2. LED code CØ Hex = Controller is selected.

Discrepancy in the Firmware:

1. The Max Cylinder Adr Hi and Max Cyl Adr Lo in the Class 6 Opcode 2 command is in the wrong order on this board. For this board only, Byte 4 should contain Max Cylinder Adr Lo and Byte 5 should contain Max Cylinder Adr Hi as shown below:

3	Max Head Adr
4	Max Cylinder Adr Lo
5	Max Cylinder Adr Hi
6	Reduce Write Current Cyl

Fixed.
J. Tseng

ADDENDUM 2:

Changes concerning the STEP PULSE WIDTH parameter of the Class 6 Opcode 2 command.

Step Pulse Width for Winchester Drive.

Parameter Value	Yield
Ø-6	6.8 us
7-13	13.6 us
14-2Ø	2Ø.4 us
21-27	27.2 us

Step Pulse Width for Floppy Drive

Parameters	Yield
1-17	17 us
18-25	25.5 us
26-34	34 us
35-42	42.5 us
43-51	51 us
52-59	59.5
6Ø-68	68 us

DTC-520A SPEC REVISION RECORD

Revision	Description
1/14/82	Preliminary release
1/19/82	mod (C.T.)
2/1/82	Released as a "PRELIMINARY SPECIFICATION"
6/22/82	Updated Interleave Computation Section 4.3.1
7/30/82	Reorganized the document. JT

TABLE OF CONTENTS

1.Ø Introduction

2.Ø DTC-52ØA Controller

- 2.1 Features
- 2.2 Electrical/Mechanical Requirements
- 2.3 Physical Specification
- 2.4 System Configuration
- 2.5 Theory of Operation

3.Ø DTC Host Bus

- 3.1 Introduction
- 3.2 Signal Definitions
- 3.3 Theory of Operation
- 3.4 Abnormal Terminations

4.Ø Commands/Programming

- 4.1 Description of Commands by Class
- 4.2 Command Format
- 4.3 Description of Commands by Opcode
- 4.4 Completion Status Format
- 4.5 Logical Address Computation
- 4.6 Interleave Computation
- 4.7 Error Code Descriptions
- 4.8 LED Error Display

5.Ø Diagnostic Philosophy

- 5.1 Error Indicators

6.Ø Sector Format

SECTION 1

INTRODUCTION

The DTC-520A Controller consists of a microprocessor-based controller with on-board data separator logic, and is able to control a maximum of 4 drives in any combination of up to 2 Seagate Technology ST506 fixed disk drives, or equivalent, and up to 4 5-1/4 inch floppy disk drives. The DTC-520A is a single printed circuit board, 5-3/4 inches by 10 inches.

Commands to the controller are issued over a bidirectional bus connected to the host computer via a host adapter. The data separator/"serdes" logic serializes bytes and converts to MFM data, and deserializes MFM data into 8-bit bytes.

Due to the microprogrammed approach utilized in the controller, extensive diagnostic capabilities are implemented. This methodology increases fault isolation efficiency and reduces system down time. Error detection and correction will tolerate media imperfections up to 4-bit burst errors.

SECTION 2

DTC520A CONTROLLER

2.1 FEATURES

The capabilities supplied as standard with the DTC-520A are listed below:

AUTOMATIC SEEK AND VERIFY	A seek command is implied in every data transfer command (READ, WRITE, CHECK, etc.). If the heads are not positioned over the correct cylinder, a seek is initiated, and a cylinder verification is performed after the seek completes.
FAULT DETECTION	Two classes of faults are flagged to improve error handling: * Controller faults * Disk faults
AUTOMATIC HEAD AND CYLINDER SWITCHING	If during a multi-block data transfer the end of a track is reached, the controller automatically switches to the next track. If the end of a cylinder is reached, the controller issues a seek and resumes the transfer.
DATA ERROR SENSING AND CORRECTION	If a data error is detected during a disk data transfer, the controller indicates whether or not it is correctable. If correctable the error is automatically corrected.
LOGICAL TO PHYSICAL DRIVE CORRELATION	Logical unit numbers (LUN's) are independent of physical port numbers. All accesses specify LUN's.
ON BOARD SECTOR BUFFER	A sector buffer is provided on the controller to eliminate the possibility of data overruns during a data transfer.

EFFICIENT HOST INTERFACE PROTOCOL	A bidirectional bus between the controller and host provides a simple yet efficient communication path. In addition, a high level command set permits effective command initiation.
BYTE TRANSFER	The byte to byte data mode transfer is less than 1.5us.
SECTOR INTERLEAVE	Sector interleaving is programmable with up to 16 way interleave.
ODD PARITY	The 8 data bits on the interface bus can have odd parity. Depending on user preference, parity can be disabled.
256/512 BYTES PER SECTOR ON HARD DISKS	Switch selectable sector size. 256 or 512 bytes/sector. 256 bytes/sector - 33 sectors/track 512 bytes/sector - 18 sectors/track
NUMBER OF DRIVES	The controller will connect to a maximum of four (4) drives. The drives can be a combination of up to two (2) ST506 interface compatible Winchester drives and up to four (4) industry standard mini-floppy disk drives that are single or double density, single or double-sided.
PROGRAMMABLE DISK PARAMETERS	The disk parameters for both hard and floppy can be passed to the controller to define the drive characteristics.
PROGRAMMABLE FLOPPY TRACK FORMAT	The type of track format on the floppy media that is going to be used can be passed to the controller through software.
ALTERNATE TRACK ASSIGNMENT	The host can assign an alternate track for a defective track. Subsequent accesses to the defective track will cause the controller to transfer data from the new track automatically.

2.2 ELECTRICAL/MECHANICAL SPECIFICATIONS

Physical Parameters

Width	5-3/4	inches (tentative)
Length	1Ø.Ø	inches "
Height	Ø.49	inches "
Weight	2.Ø	lbs. "

Mounting holes are the same as that of the disk drive.

Environmental Parameters

	Operating:	Storage:
Temperature (degrees F/C)	32/Ø to 131/55	-4Ø/-1Ø to 167/75
Relative Humidity (@ 4Ø degrees F, wet bulb temp., no condensation)	1Ø% to 95%	1Ø% to 95%
Altitude	sea level to 1ØK feet	sea level to 15K feet

Power Requirement

Voltage @ current	+5 VDC ± 5% @ 2.6A (max) 5Ø MVOLD P/P Ripple (max)

Controller Power Connections

1) No Connection

2) GND

3) GND

4) +5V @ 2.6A

power connector diagram

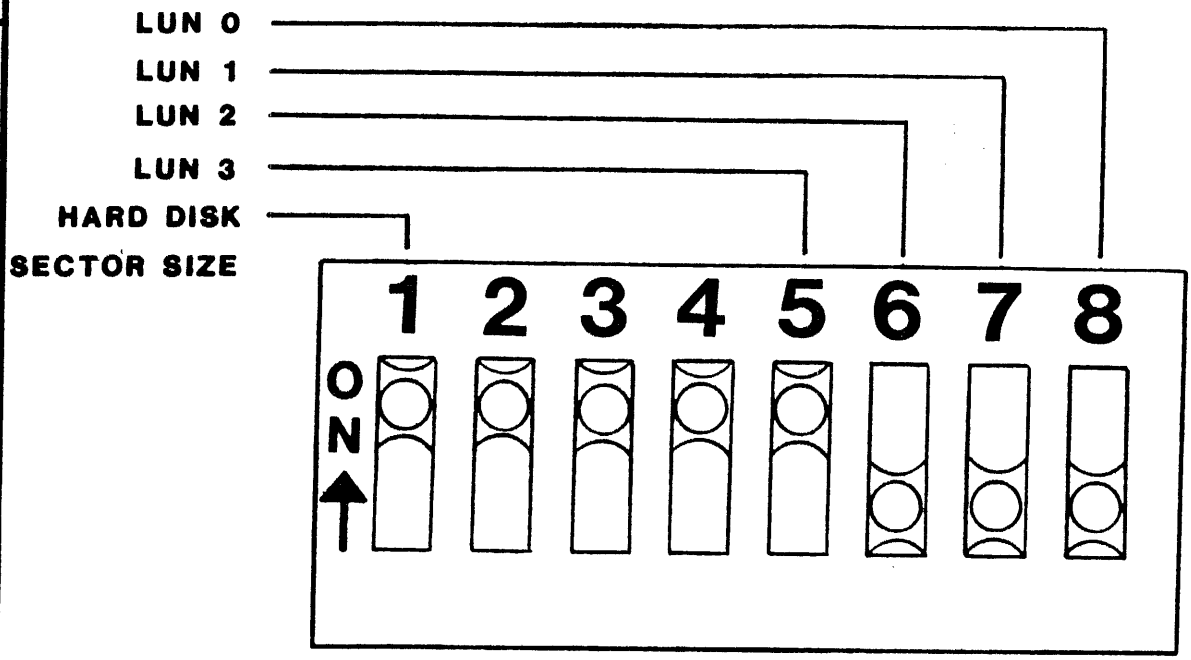
Electrical requirements on Drive Interface

The electrical interface to the 5 1/4 in. drives will conform to the requirements described in the disk drive interface specification.

2.3 PHYSICAL SPECIFICATION

DTC52ØA Board Outline Diagram is shown in Fig. 2.Ø

REV.	APPLICATION		REVISIONS			
SH	NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED
DWG. NO.						



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	DTC Data Technology Corporation	
MATERIAL	APPROVALS / DRAWN L. FOK	DATE 8-3-82	DTC 520A SWITCH SETTING
FINISH	CHECKED		SIZE A / FSCM NO. / DWG. NO. / REV.
DO NOT SCALE DRAWING	ISSUED		SCALE / SHEET 1 OF 2

RE	SH	DWG. NO.	APPLICATION		REVISIONS			
			NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED

SWITCH	DRIVE TYPE SELECT	ON	OFF
8	LUN 0	HARD DISK	FLOPPY DISK
7	LUN 1	HARD DISK	FLOPPY DISK
6	LUN 2	ILLEGAL	FLOPPY DISK
5	LUN 3	ILLEGAL	FLOPPY DISK
4	NOT USED		
3	NOT USED		
2	NOT USED		
1	HARD DISK SECTOR SIZE	256 BYTES/SECTOR 33 SECTORS/TRACK	512 BYTES/SECTOR 18 SECTORS/TRACK

NOTE: LUN 2 & 3 CAN ONLY BE ASSIGNED AS FLOPPY DRIVES.

DEFAULT DRIVE TYPES

HARD DISK...SEGATE TECHNOLOGY ST506 WITH BUFFERED STEP
FLOPPY DISK...SHUGART ASSOCIATES SA460, 16 SEC/TRACK

THESE ARE THE DEFAULT DRIVE TYPES ASSIGNED TO EACH DEVICE.
USE THE CLASS 6 COMMAND TO CHANGE TO THE ACTUAL DRIVE TYPE.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	DTC Data Technology Corporation	
MATERIAL	APPROVALS / DRAWN L. FOK	DATE 8-3-82	DTC 520A SWITCH SETTING
FINISH	CHECKED		SIZE A / FSCM NO. / DWG. NO. / REV.
DO NOT SCALE DRAWING	ISSUED		SCALE / SHEET 2 OF 2

Parity Jumper Setting

If terminal A is jumpered to B then parity is enabled.

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED

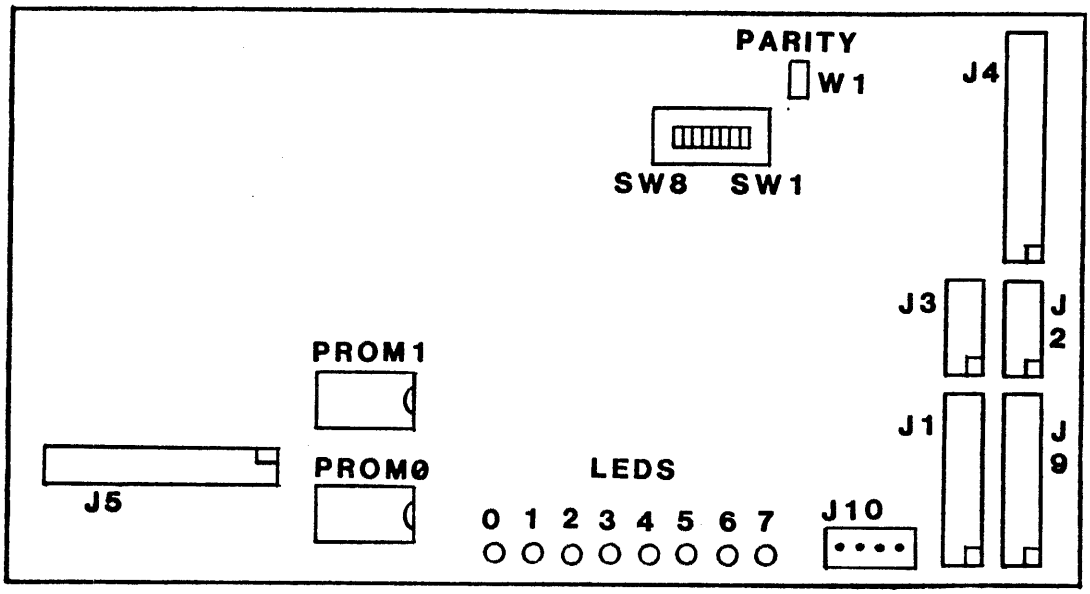


FIG. 2.0

J1....WINCHESTER CONTROL CABLE

J2,J3....WINCHESTER READ/WRITE CABLES

J4....HOST BUS CABLE

J5....UNUSED

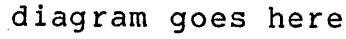
J9....FLOPPY CONTROL CABLE

J10....POWER CONNECTOR

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	DTC Data Technology Corporation	
MATERIAL	APPROVALS / DRAWN L. FOK	DATE 8-5-82	DTC 520A BOARD OUTLINE DIAGRAM
FINISH	CHECKED		SIZE A / FSCM NO. / DWG. NO. / REV.
DO NOT SCALE DRAWING	ISSUED		SCALE / SHEET

2.4 SYSTEM CONFIGURATION

The controller and data separator comprise a single PCB. A maximum of four (4) drives may be connected as shown in Fig. 2.1.



NEXT ASSY	USED ON	REVISIONS REV.	DESCRIPTION	DATE	APPROVED

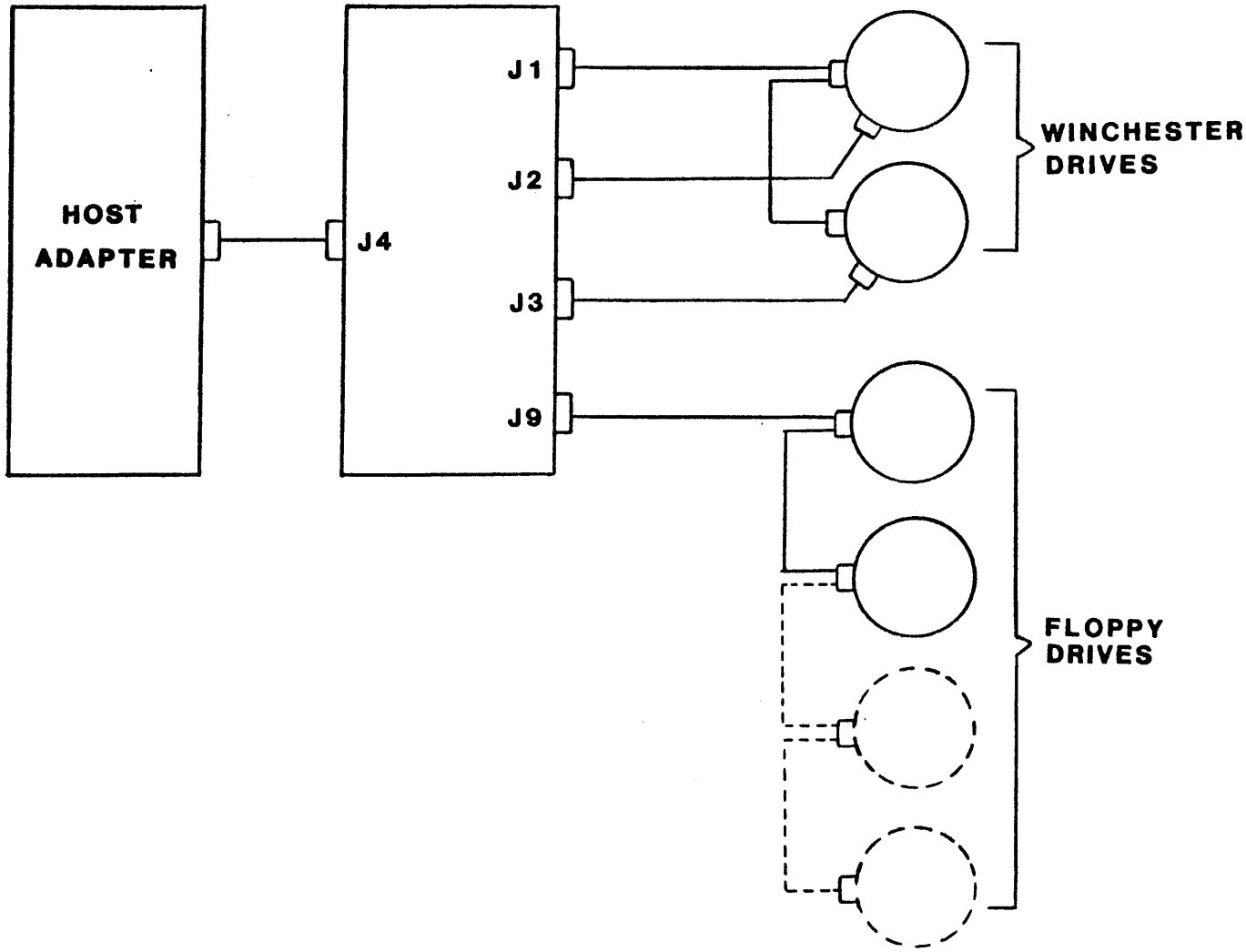


FIG. 2.1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	DTC Data Technology Corporation	
MATERIAL	APPROVALS / DRAWN L. FOK	DATE 8-5-82	DTC 520A SYSTEM CONFIGURATION
FINISH	CHECKED		SIZE A / FSCM NO. / DWG. NO. / REV.
DO NOT SCALE DRAWING	ISSUED		SCALE / SHEET

2.5 THEORY OF OPERATION

Disk commands are issued to the DTC-520A via the host bus following a defined protocol. The host initiates a command sequence by selecting the controller on the bus. If the controller is not busy, it requests command bytes from the host for task execution. (Command structure is described in Section 4.0). Depending on the type of command, the controller will request up to 10 bytes. Upon reception of the last command byte, the controller begins execution of the command.

For the data transfer commands, a check is performed on the disk address and status flagged if it exceeds the drive limits. The data is stored in a sector buffer before transfer to the host or disk drive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command, the controller will send the completion status to the host and if error is indicated further delineation of the completion status may be requested by issuing the appropriate sense commands.

Odd parity is generated by the DTC-520A for all information that it puts on the I/O bus. If enabled, the DTC-520A flags all information that it receives with bad parity.

SECTION 3

DTC HOST BUS

3.1 INTRODUCTION

The DTC Host Bus is a negative-logic, bidirectional 8-bit data bus utilizing odd parity. The electrical interface consists of an open collector bus terminated on each end by a 220/330 ohm resistor network. The controller regulates transfers across the bus in such a way that permits connection host systems that utilize direct memory transfer capability as well as those that only support program input/output implementations.

3.2 ELECTRICAL REQUIREMENTS ON THE HOST INTERFACE

The Host Bus is based on an open-collector philosophy terminated on each end with 220 ohms to Vcc and 330 ohms to ground. The typical cable used is a 50-pin, mass terminated, cable with a characteristic impedance of approximately 100 ohms. The recommended drivers and receivers for the Host Bus is 7438 and 74LS240, respectively. The maximum length of the Host Bus is 20 feet.

3.3 SIGNAL DEFINITION

The signals that comprise the Host Bus are separated into those that are driven by the controller, those that are driven by the host adaptor (H/A), and those that are bidirectional. The term "asserted" means that the signal on the Host Bus is between 0V and 0.8V. The term "deasserted" means that the signal on the host bus is between 2.5V and 3.5V (negative or low true logic).

I. Unidirectonal Signals Driven By Controller

I/O — Input/Output
When asserted, the data on the bus is driven by the controller. When deasserted, the data on the bus is driven by the host adapter. The host adapter must use this line to enable its drivers onto the data bus.

C/D — Command/Data
When asserted, the bytes transmitted across the bus are interpreted as command bytes. When deasserted, the bytes are data bytes.

BUSY — This bit is asserted as a response to the SEL line from the host adapter and to indicate that the host bus is currently in use.

MSG Message
When asserted, indicates that the command is completed. This bit is always followed with the assertion of I/O, and the assertion of REQ.

REQ Request
This bit operates in conjunction with I/O, C/D, & MSG. When asserted and I/O is asserted, REQ will mean that the data on the host bus is driven by the controller. When asserted and I/O is deasserted, REQ will mean that the data is driven by the host adapter (H/A). The following table lists the legal states of the control bits on the bus; the states are valid only when REQ is asserted.

I/O	C/D	MSG	Meaning
d	a	d	Get a command byte from H/A
d	d	d	Get a data byte from H/A
a	d	d	Send a data byte to H/A
a	a	d	Send the status byte to H/A
a	a	a	Send the message byte to H/A (Command is completed.)

a = asserted, d = deasserted

II. Unidirectional Signals Driven By Host Adapter

ACK Acknowledge
This bit is asserted as a response to REQ from the controller. ACK must be returned for each REQ assertion. The controller will wait for the assertion of ACK before REQ is deasserted. The H/A must not deassert ACK until after REQ has been deasserted. If the H/A keeps ACK asserted, the controller will not reassert REQ until after ACK is deasserted. This provides the H/A with a means of regulating the transfer of bytes across the bus. Byte transfer regulation can occurr for either command or data bytes.

RST Reset
When asserted, this bit forces the controller to the beginning of its microcode. Following a Reset, the controller will monitor the bus and wait for the H/A to assert Select. Reset will immediately terminate any pending command without the transmission of the status or the message bytes. All signals to the drives are deasserted. RST must be asserted for a minimum of 250ns and a maximum of 1 second.

SEL — Select

When asserted, indicates the beginning of the command transaction. The H/A asserts SEL to gain the attention of the controller. Data Bit Ø on the bus must also be asserted during SEL time to select the controller. The controller will return BUSY as acknowledgement for SEL. After the assertion of BUSY, the H/A will deassert SEL. The controller will wait until SEL is deasserted before it asserts REQ. This provides a way for the H/A to hold off the command byte fetch until it is ready for the controller. SEL can be asserted immediately following a Reset.

III. Bidirectional Data

DB(7-Ø,P) - Data lines 7 thru Ø represent the eight data bits (DBØ = lsb). Parity is represented by P. The controller utilizes odd parity (the number of asserted bits on the host bus is always odd).

3.4 THEORY OF OPERATION

Every command to the controller is performed in 4 phases as follows:

1) Select Phase
2) Command Fetch Phase
3) Data Transfer Phase (if required)
4) Status & Message Phase

I. Select Phase

Following a Reset, or the completion of a command, the controller will monitor the Host Bus for the assertion of SEL. The host adapter asserts SEL and DBØ (controller address bit) on the Host Bus to indicate that a command is ready for the controller. It then waits for the controller to respond with BUSY. Upon reception of BUSY, the H/A deasserts SEL. The controller now has control of the host bus. Note: The H/A may keep SEL/DBØ asserted until it is ready to enter Phase 2.

II. Command Fetch Phase

After the H/A deasserts Select and DBØ, the controller asserts C/D (to indicate command mode transfer), and deasserts I/O (to indicate output from the host adapter) to fetch the command bytes from the H/A. The command bytes are transferred over the host bus with the REQ/ACK handshake protocol until all command bytes are transferred to the controller. (The command byte fetch mode ends after the last REQ pulse from the controller is deasserted.) The H/A must not assert ACK until after REQ is asserted; H/A must not deassert ACK until after REQ is deasserted. The controller will wait until ACK from the previous byte transfer is deasserted before it reasserts REQ for to transfer the next byte. Note: This provides a means for the H/A to regulate the byte transfer across the Host Bus.

III. Data Transfer Phase

If the command does not require a transfer of data, this phase is skipped. If a data transfer is required for the command, such as read or write, the following occurs. The controller deasserts the C/D line to indicate data mode. Depending on the command type (read/write disk), the I/O bit on the host bus is asserted or deasserted by the controller, and the data is transferred (one byte at a time) with the same REQ/ACK handshake protocol used during the Command. After all bytes are transferred the controller exits this phase.

IV. Status & Message Phase

After all the data bytes have been transferred, a completion status byte is placed on the data bus by the controller - C/D and I/O are asserted, MSG deasserted. REQ is asserted and the controller waits for ACK from the host adapter. After the status byte transfer, the controller places zeros on the data bus and asserts C/D, I/O and MSG along with REQ to indicate to the host that the command is complete (this action can be used to generate an interrupt on the host system). After the H/A responds with ACK, the controller deasserts REQ, BUSY and

controller is now ready to be selected for the next command.

3.5 ABNORMAL COMMAND TERMINATION

If no errors occur, the command will proceed as previously described. However, if errors do occur the controller will terminate the command and immediately enter the status & message phase. Error conditions can be classified as follows:

1) Bus Parity errors - Upon the detection of a parity error in the byte (command or data) that is recieved from the H/A, the controller will complete the REQ/ACK handshake and enter the status and message phase. The status byte will indicate that a parity error has occurred.

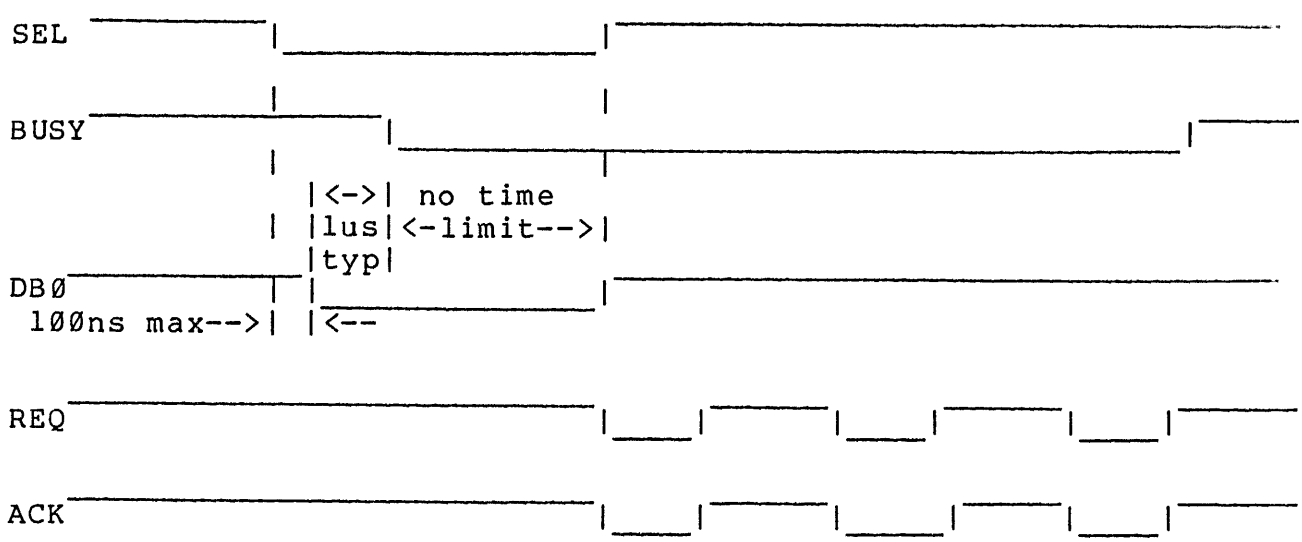
2) Drive Interface or Controller related errors - After the six command bytes have been accepted, errors of this type can be detected. Upon the detection of the error condition (Drive Fault, Drive Not Ready, Illegal Command) the controller will enter the status & message phase. The status byte will have the error bit set.

3) Read/Write Channel errors - Upon detection of these errors (Read data error, Record not found, Drive Fault during a write) the controller may transfer a sector, or more, of data before it enters the status & message phase. The error bit is set in the status byte.

In cases 2 & 3 a Request Sense command may be issued to retrieve error information. In either case, any another command may be issued if the host system does not care about the details of the errors.

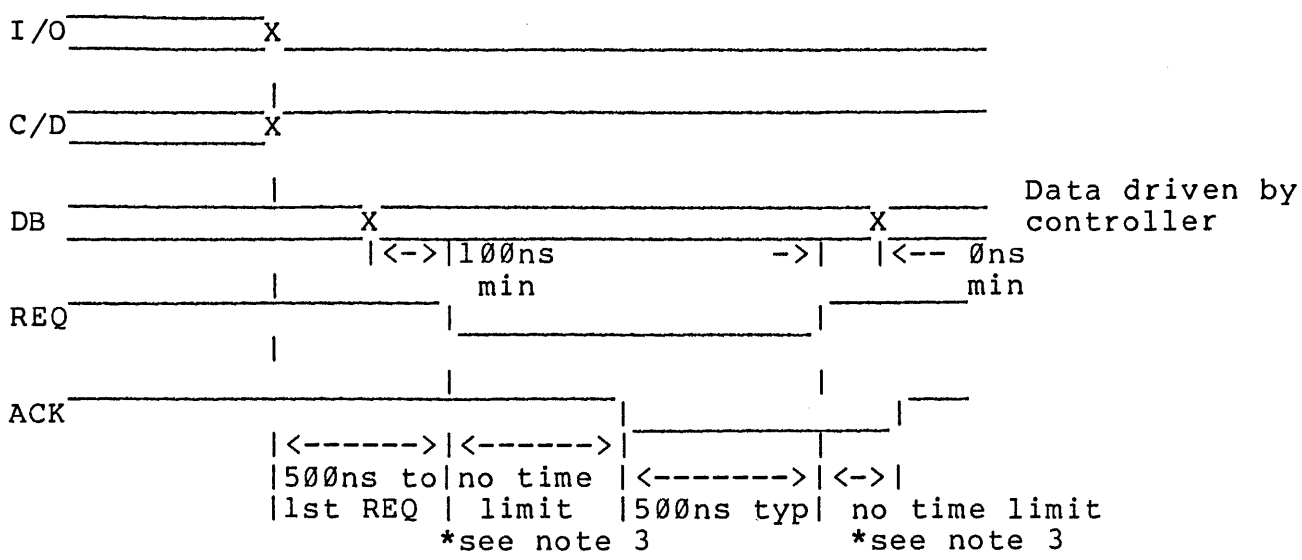
Timing Requirements for Controller Selection

I. Selection Phase



Note: SEL must be deasserted before the controller will assert REQ. Busy will remain asserted during the entire command. The three assertion times for REQ and ACK are shown merely to indicat that the handshake occurs during the assertion time of Busy. It does not imply that there are only three REQ/ACK transactions during a command.

Timing Requirements for Data Transfer
(To host adapter, typical byte)



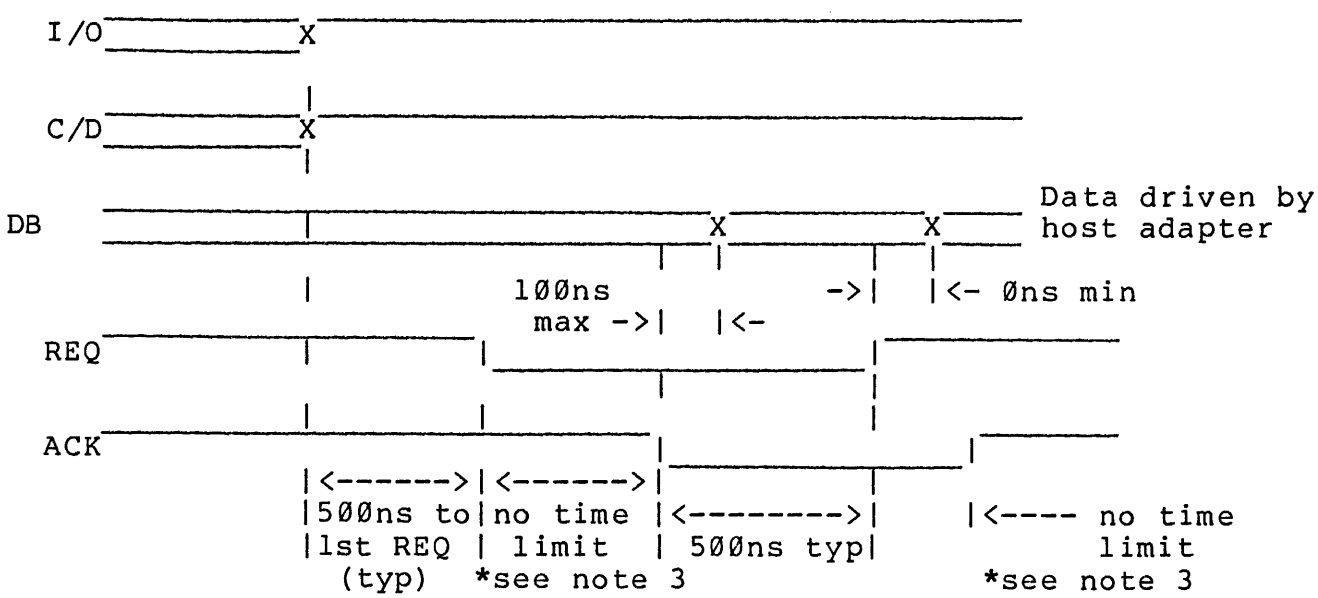
Note 1. For Status Byte Transfer (I/O, C/D asserted & MSG deasserted); or Interrupt Byte Transfer (MSG, I/O, C/D asserted), REQ is asserted 500ns (typical) after the assertion of any of the above bits.

2. Data driven by the controller is stable 100ns min at the host adapter end before REQ is asserted and 0ns min after REQ is deasserted.

3. Although there is no time limit on the REQ-ACK handshake the entire transfer must be done within 52.43ms otherwise a time-out error will occur.

4. The Status & Message bytes are transferred in the same manner described in this subsection. Of course MSG is also asserted during this time.

Timing Requirements for Data Transfer
(From host adapter, one byte)



Note 1. Data driven by the host adapter is stable 100ns max (at the host adapter end) after ACK is asserted and 0ns min after REQ is deasserted.

2. For command mode transfers, SEL must be deasserted before ACK is asserted. This sequence follows the selection protocol.

3. Although is no time limit on the REQ-ACK handshake, the entire transfer must be done within 52.43ms otherwise a time-out error will occur.

4. Command bytes are transferred using the same protocol. C/D, REQ are asserted and I/O, MSG are deasserted.

Host I/O Connector Pin Assignment.

The Host I/O Bus uses a 50-pin connector (AMP P/N 2-87227-5 or equivalent). The unused signal pins are considered to be spares for future use. The pin assignments are as follows:

Signal	Pin Number	
DATA0	2	
DATA1	4	
DATA2	6	
DATA3	8	
DATA4	10	
DATA5	12	
DATA6	14	
DATA7	16	
PARITY	18	
--	20	-----
--	22	|
--	24	|
--	26	Future
--	28	Usage
--	30	|
--	32	|
--	34	-----
BUSY	36	
ACK	38	
RST	40	
MSG	42	
SEL	44	
C/D	46	
REQ	48	
I/O	50	

NOTE: All signals are negative true and all odd pins are connected to ground. The signal lines are terminated with 220 ohms to 5V and 330 ohms to ground.

SECTION 4

COMMANDS / PROGRAMMING

4.1 DESCRIPTION OF COMMANDS BY CLASS

Commands to the controller are categorized into various classes as indicated below:

Class Ø - Non-data Transfer, Data Transfer and Status Commands

Class 1 - Disk Copy Commands

Class 2-5 - Reserved

Class 6 - Disk Parameter Assign Commands

Class 7 - Diagnostic Commands

4.2 COMMAND FORMATS

Class Ø Command Format

The Class Ø commands follow the general format shown:

Byte #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	OPCODE				
1	LUN			SLAD 2				
2	LAD 1							
3	LAD Ø							
4	# of BLOCKS / INTERLEAVE							
5	CONTROL							

Class 1 Command Format

The Class 1 commands follow the general format shown:

Byte #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	1	OPCODE				
1	SLUN			SLAD 2				
2	SLAD 1							
3	SLAD Ø							
4	# of BLOCKS							
5	DLUN			DLAD 2				
6	DLAD 1							
7	DLAD Ø							
8	set to Ø							
9	CONTROL							

Class 6 Command Format

The Class 6 commands follow the general format as shown:

Byte #	7	6	5	4	3	2	1	Ø
Ø	1	1	Ø	OPCODE				
1	LUN			set to Ø				
2	set to Ø							
3	set to Ø							
4	set to Ø							
5	set to Ø except Opcode Ø							

Class 7 Command Format

The Class 7 commands follow the general format shown:

Byte	7	6	5	4	3	2	1	Ø
Ø	1	1	1	OPCODE				
1	LUN			LAD 2				
2	LAD 1							
3	LAD Ø							
4	INTERLEAVE							
5	CONTROL							

Description of the fields used in the Command Descriptor Blocks

LUN

This field specify the logical unit number of the drive we are attempting to communicate with. It corresponds to Drive Select jumper on the drives as follows:

Drive Select 1 = LUN Ø
Drive Select 2 = LUN 1
Drive Select 3 = LUN 2
Drive Select 4 = LUN 3

SLUN = Source drive LUN
DLUN = Destination drive LUN

LAD (Ø-2)

This is a 21 bit logical sector address of the beginning sector of the group of sectors we wish to access. LAD Ø is the LSB. The LAD field can be from Ø up to the total number of sectors available on a particular drive.

OF BLOCKS

This field holds the number of sectors we wish to transfer per command. A value of Ø will result in a transfer of 256 sectors.

INTERLEAVE

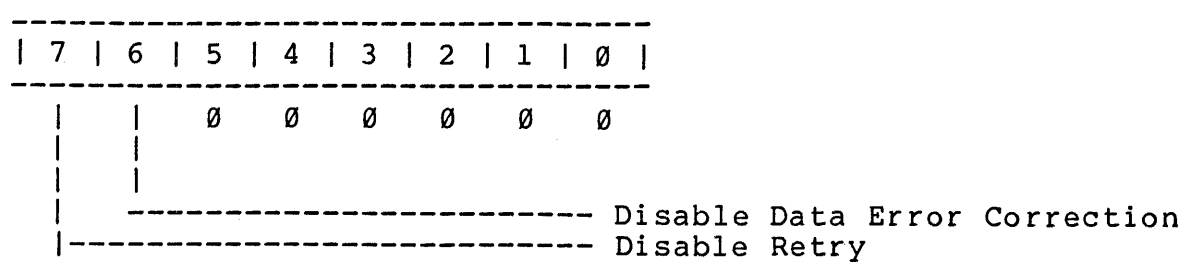
This field is used to tell the controller what interleave to use during the format commands, check track command or the read id command.

Interleave is a factor used while formatting a drive so the user can optimize the throughput of the data transfer of the system. The throughput of the system depends on the controller's turnaround time for next sector and the data transfer rate on the host bus.

CONTROL

This field contains the control bits that tells the controller how to react if an error condition is encountered during the command execution phase.

This byte is defined as follows:



Disable Retry

If this bit is set, the controller will not attempt to retry the command upon certain retryable error conditions. If it is not set, a total of eight retrys will be performed before an error is reported. If a retry is successful, the controller will not report the error to the host. The following errors can result in a retry attempt:

a) Record not found during Read or Write commands
b) Seek errors during Read or Write commands
c) Uncorrectable data error during Read commands

For error conditions (a) & (b), a recalibrate, reseek, and reread are performed. For error condition (c), only a reread is performed.

Disable Data Error Correction

If this bit is set, the controller will not correct the data that is read from the disk if an ECC error occurred during a read. If it is not set, data errors will always be corrected if correctable, before being transferred to the host.

The information returned by the Request Sense command will indicate whether or not the data error is correctable.

Regardless of the error condition, the data is transferred to the host.

4.3 DESCRIPTION OF COMMANDS BY OPCODE

Class Ø Commands

Opcode ØØ Test Drive Ready

This command selects the specified drive and verifies that the drive is ready for access.

The required fields for this command are: OPCODE and LUN.

Opcode Ø1 Recalibrate

This command positions the R/W arm of the drive to TrackØØ position and clears any possible error status in the drive.

The required fields for this command are: OPCODE and LUN.

Opcode Ø2 Not Used

Opcode Ø3 Request Sense

This command returns 4 bytes of drive and controller sense as Data (C/D deaserted) for the specified LUN. It must be issued immediately after an error to get the valid sense of the error.

The required fields for this command are: OPCODE and LUN.

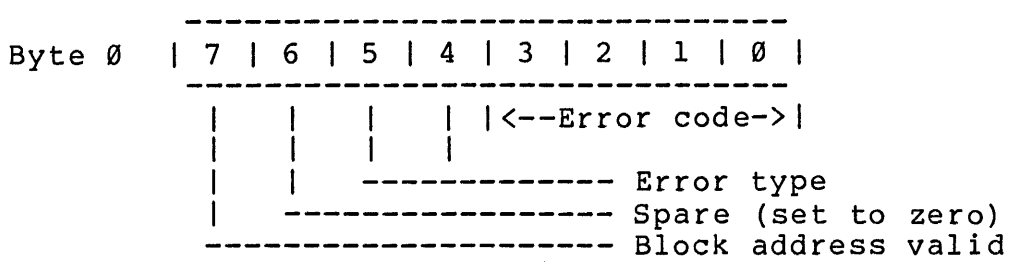
The sense bytes are return in the following format.

Byte	7	6	5	4	3	2	1	Ø
Ø	SENSE BYTE							
1	LUN			LAD 2				
2	LAD 1							
3	LAD Ø							

Definitions of the fields used in the Sense Block

SENSE BYTE

This is the byte that describe the details or the nature of the error itself. The bits are defined as follows:



Block Address Valid (Bit 7)
This bit indicates that the Logical Sector Address, LAD in bytes 1 thru 3 contain the valid logical address of the block at which the error occurred.

Error Type (Bit 5,4)
These two bits describes the general type of error. It can contain either one of the following:

ØØ	for controller related errors
Ø1	for drive related errors
1Ø	for command related errors
11	for miscelleneous errors

Error Code (Bit 3-Ø)
This is a 4 bit field that describes the actual error interpretation under each general type of error.

LUN

This byte indicates the logical unit number of the drive where the error had occured.

LAD 2,1,Ø

This is a 21 bit logical address of the sector at which the error occured. This field is valid only if the Block Address Valid bit is set in the SENSE byte.

Opcode Ø4 Format Drive

This command formats all the tracks on the specified drive with the selected track format. The sectors will be placed on the tracks according to the interleave code specified in the command block and the data fields will be filled with data pattern E5 hex.

The required fields for this command are: OPCODE, LUN and INTERLEAVE.

Opcode Ø5 Check Track

Check track command checks the track format on the specified track for the correctness of the contents of the ID fields and the interleave of the sectors. It does not read the data field.

The required fields for this command are: OPCODE, LUN, LAD 2,1,Ø and INTERLEAVE.

Opcode Ø6 Format Track

This command formats the specififed track with no flags set in the ID fields of all sectors on the track. It also fills the data field with data pattern E5 hex.

The required fields for this command are: OPCODE, LUN, LAD 2,1,Ø and INTERLEAVE.

Opcode Ø7 Format Bad Track

Format bad track command formats the specified track with the bad block flag set in all ID fields on the track. Data pattern of E5 hex is filled in the data field.

The required fields for this command are: OPCODE, LUN, LAD 2,1,Ø, and INTERLEAVE.

Opcode Ø8 Read

This command reads the specified number of sectors starting from the initial block address given in the LAD field and transfers them to the host.

The required fields for this command are: OPCODE, LUN, LAD 2,1,Ø,# of blocks and CONTROL.

Opcode ØA Write

The write command gets the data from the host and writes the specified number of sectors starting from the initial block address given in the LAD field.

The required fields for this command are: OPCODE, LUN, LAD 2,1,Ø, NUMBER OF BLOCKS and CONTROL.

Opcode ØB Seek

This command initiates a seek to the cylinder where the block specified in the LAD field is located. For winchester drives capable of doing overlap seeks, depending on how the drive parameter is set up, it could immediately return completion status before the seek complete is found from the drive. Normally it returns the completion status only after the seek is all done.

The required fields for this command are: OPCODE, LUN, and LAD 2,1,Ø.

Opcode ØC Not Used

Opcode ØD Not Used

Opcode ØE Assign Alternate Track

This command formats the track specified in the LAD field with the alternated bad track flag set in the ID fields and with the track address of the alternate track written in the data fields. Also it formats the alternate track itself with the alternate track identifier flag set in its ID fields and data pattern E5 hex filled in the data field.

Future write/read access to that specified track will cause the drive to seek to the alternate track, transparent to the host software, and do the write/read operations there.

The required fields for this command are: OPCODE, LUN, LAD 2,1,Ø and INTERLEAVE.

After the controller received the command, it will collect the alternate track address as data (C/D deasserted) from the host in the following format:

Byte #	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	LAD 2				
1	LAD 1							
2	LAD Ø							
3	set to Ø							

NOTE: Alternate tracks can be assigned one level only. That is, an alternate track cannot have another alternate track assigned to it.

Opcode ØØ Copy Blocks

<<TBD>>

Opcode ØØ Define Floppy Disk Track Format

This command is used for defining the track format of the floppy media to the controller, i.e. sides, density and bytes per sector.

The required fields for this command are: OPCODE, LUN and Byte 5.

The following track format codes are supported by the controller and the code byte is passed to the controller through Byte 5 of the Class 6 command block in the following format.

Track Format Code	Track Format Description
ØØ hex	Single density, single-sided; FM recording, 128 bytes/sector, 16 sectors/track.
Ø1 hex	Single density, double-sided; FM recording, 128 bytes/sector, 16 sectors/track.
Ø6 hex	Double density, single-sided; Side Ø, cylinder Ø - FM recording, 128 bytes/sector, 16 sectors/track. All other tracks - MFM recording, 256 bytes/sector, 16 sectors/track.
Ø7 hex	Double density, double-sided; Side Ø, cylinder Ø - FM recording, 128 bytes/sector, 16 sectors/track. All other tracks - MFM recording, 256 bytes/sector, 16 sectors/track.
86 hex	Double density, single-sided; MFM recording, 256 bytes/sector, 16 sectors/track.
87 hex	Double density, double-sided; MFM recording, 256 bytes/sector, 16 sectors/track.
8A hex	Double density, single-sided; MFM recording, 512 bytes/sector, 8 sectors/track.
8B hex	Double density, double-sided; MFM recording, 512 bytes/sector, 8 sectors/track.

Note: If track format information for floppy is not specified after each reset or power-on, the default code will be as follows:

Track format code Ø6 (hex).
Double density, single-sided;
512 bytes/sector, 8 sectors/track.

Opcode Ø2 Assign Drive Parameters

This command allows the host to setup the disk step pulse width, step period, step mode, max head address, max cylinder address, timing/delays and cylinder address to apply reduced write current for the specified LUN.

The required fields for this command are: OPCODE, and LUN.

Depending on how the switches are set up on the controller, 1Ø bytes of parameters will be collected from the host as Data (C/D deasserted) using 2 different formats for floppy drives or Winchester drives.

The parameters for a Winchester drive are passed as data to the controller using the following format.

Byte #	7	6	5	4	3	2	1	Ø
Ø	Step Pulse Width							
1	Step Period							
2	Step Mode							
3	Max Head Adr							
4	Max Cylinder Adr Hi							
5	Max Cylinder Adr Lo							
6	Reduce Write Current Cyl							
7	Drive Type Identifier							
8	set to Ø							
9	set to Ø							

Description of the parameters for Winchester drives

Step Pulse Width

This is the time the STEP signal is asserted in lusec increments.
Range- 1.Øusec to 256.Øusec

Step Period

This is the time between two step pulses. For the purpose of simplifying logics, this is the time the step signal is deasserted between two step pulses in 5Øusec increments.
Range- 5Øusec to 128msec.

Step Mode

This defines the type of stepping the drive is set up to do. The following describes the modes supported by the controller.

Mode Ø Normal or Buffered Step
This mode generates step pulses using the pulse width & rate specified in Byte Ø,1)

Mode 1 Seagate fast step algorithm
This mode steps the drive according to the Seagate fast step algorithm and it ignores the pulse width and rate specified in Byte Ø,1.

Mode 2 Tandon fast step algorithm
This mode steps the drive as described in the Tandon fast step algorithm and it ignores the pulse width and rate specified in Byte Ø,1.

Note: For Mode 1 & 2, refer to the drive specification on how to set up the drive to get the fast step mode.

Max head address

This bytes specifies the maximum head address on the drive.
Range- Ø to 7 (i.e. 1 to 8 heads)

Max cylinder address

These two bytes specify the maximum cylinder address on the drive.
Range- Ø to 1Ø23 (i.e. up to 1Ø24 cylinders)

e.g. Byte 4 = Ø, Byte 5 = 179 => 18Ø cylinders.

Reduced Write Current Cyl

This byte specifies the cylinder address where the reduced write current is to be first applied. If the value is 'Ø', reduced write current is never asserted.
Range- 1 to 255

e.g. 77 = the reduced write current is applied for all cylinders greater than or equal to 77 (during write operation)

Drive type identifier

This byte is defined as follows.

Bit 7
Must be set to Ø to indicate parameters are for hard disk.

Bit 6
This bit tells the controller whether to wait for the seek complete after a seek command (Class Ø, Opcode ØB) to the Winchester drive. If the drive is capable of overlap seek, this bit can be set to utilize the function.

e.g. Bit 6 = Ø => wait for seek complete after the last step pulse.
Bit 6 = 1 => do not wait for seek complete after the last step.

NOTE: The seek incomplete timeout is set to approximately 7ØØ msec. That is, any seek must complete within 7ØØ msec or the controller will report an error.

Default Parameters for Winchester drive type.

Upon reset, the controller will default to the parameters of Seagate Technology ST5Ø6 disk drive as shown below for the LUN's that are preassigned as Winchester drives on the dipswitch. The user should set the parameters for the type of Winchester drive being used after every reset or power-on.

Byte Ø	= 11	11 Usec Step pulse
Byte 1	= 6Ø	3.Ø Msec Step period
Byte 2	= Ø	Buffered step mode
Byte 3	= 3	4 heads
Byte 4	= Ø	High cylinder byte is zero
Byte 5	= 152	153 cylinders
Byte 6	= 77	Reduce Wr Current at cyl. 77 and above
Byte 7	= Ø	
Byte 8	= Ø	
Byte 9	= Ø	

The parameters for a mini floppy drive is passed to the controller using the following format.

Byte #	7	6	5	4	3	2	1	0
0	Step Pulse Width							
1	Step Interval							
2	Max Cylinder Address							
3	Head Settling							
4	Hd Sel --> Valid Rd/Wr							
5	Dr Sel --> Valid Rd/Wr							
6	Delay after Wr Gate off							
7	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
8	Ø							
9	Ø							

Description of the parameters for floppy drives

Step Pulse Width

This is the period of time when the STEP signal is asserted in lusec increments.
RAnge- 1.Øusec to 256usec

Step Interval

This byte specifies the period of time when the STEP signal is deasserted in lmsec increments
Range- 1.Ømsec to 256.Ømsec

Max Cylinder Address

This byte specifies whether the mini floppy drive is a single or double TPI drive. For compatibility sake, it should contain either the value 34 (decimal) for a single TPI drive or 79 (decimal) for a double TPI drive.

Head Settling

This specifies the delay required from last STEP pulse to valid Rd/Wr in lmsec increments.
RAnge- 1.Ømsec to 256.Ømsec

Hd Sel --> Valid Rd/Wr

This byte indicates the delay required from head selection to valid Rd/Wr in lusec increments.
RAnge- 1.Øusec to 256.Øusec

Dr Sel --> Valid Rd/Wr

This byte contains the delay required from drive selection to valid Rd/Wr in 1 msec increments.
Range- 1.Ømsec to 255.Ømsec

A value of Ø in this field means that this delay will not be applied as in the case of some mini floppy drives.

Delay after Wr Gate off

The delay required from the time Write Gate becomes inactive to Side Selection/ Drive Deselection/ Next Step Sequence in lmsec increments.
Range- Ø.lmsec to 25.5msec.

A value of Ø in this field means that this delay will not be applied as in the case of some mini floppy drives.

Default Parameters for a mini floppy drive.

Upon reset, the controller will default to the parameters of Shugart SA46Ø drive as shown below for the drives that are preassigned as floppy drives on the dipswitch. The user should set the parameters for the type of floppy drive being used after every reset or power-on.

Byte Ø	=	2	2.Øusec Step Pulse Width
Byte 1	=	7	7.Ømsec Step Interval
Byte 2	=	79	8Ø cylinders
Byte 3	=	22	22.Ømsec Head Settling
Byte 4	=	2Ø5	2Ø5.Øusec Hd Sel to Valid Rd/Wr
Byte 5	=	Ø	Ø.Ømsec Dr Sel to Valid Rd/Wr
Byte 6	=	11	1.1 msec Delay after Wr Gate off.
Byte 7	=	8Ø(Hex)	Mini floppy parameter indicator
Byte 8,9	=	Ø	Set spare bytes to zero

Class 7 Commands

Opcode ØØ RAM Diagnostic

This command performs a data pattern test on the RAM on the controller.

The required field for this command is: OPCODE.

Opcode Ø1 Write ECC

This command writes a block of data to the disk without generating ECC for the data. It displaces the data on the disk by three bytes so that the ECC bytes for the data can be written from the host in order to verify the ECC logic of the controller.

The required fields for this command are: OPCODE, LUN, LAD 2,1,Ø, and CONTROL.

Opcode Ø2 Read ID

This command reads only the 3 ID bytes and 3 ECC bytes of the specified sector and transfers them to the host as data (C/D deasserted).

The required fields for this command are: OPCODE, LUN, LAD 2,1,Ø, and INTERLEAVE.

Opcode Ø3 Drive Diagnostic Ø

This command performs a diagnostic on the specified LUN. It reads sector Ø on all tracks sequentially and then reads sector Ø on 256 random tracks.

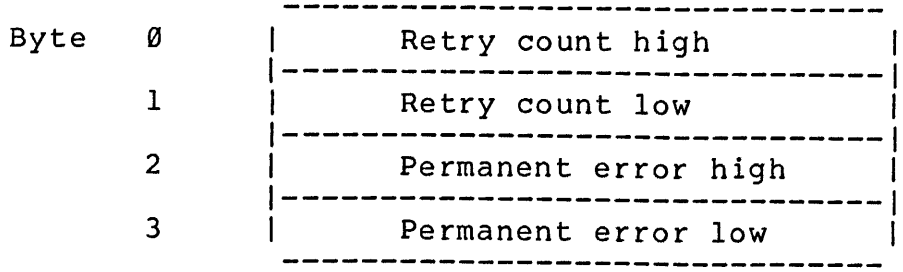
The required fields for this command are: OPCODE and LUN.

Opcode Ø6 Request Logout

This command is used to retrieve four bytes of error log for the specified LUN. Each device has its own error log area which is accumulated every time certain errors occured and it is cleared every time after transferring the error log.

The required fields for this command are: OPCODE and LUN.

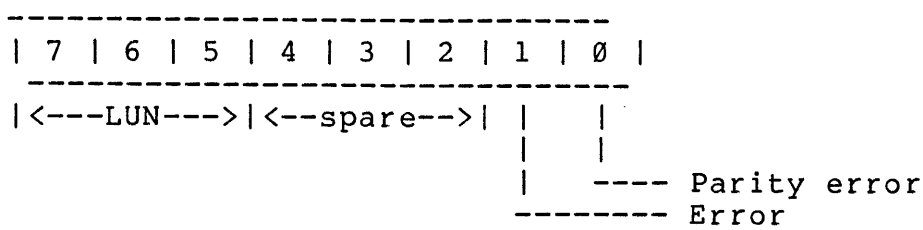
The log is transferred to the host as Data (C/D deasserted) using the following format.



The following errors get accumulated in the log:
1. Uncorrectable error in ID field.
2. Uncorrectable error in data field.
3. No ID address mark
4. No data address mark.
5. Seek error.
6. Record not found.

4.4 COMPLETION STATUS FORMAT

The following describes the Completion Status Byte returned to the host after every command.



Definition of the bits

Parity error

A 1 in this bit indicates that a parity error occurred during transfer from host to controller.

Error bit

A 1 in this bit indicates that an error occurred during the execution of a command.

Spare bits are always zero.

LUN

These bits indicate the logical unit number of the drive where the error occured.

4.5 LOGICAL ADDRESS COMPUTATION

The logical address is computed using the following formular:

Logical adr = (CYA * #HD per CYL + HDA) * #SE per TRK + SEA

Where: CYA = cylinder adress
HDA = head address
SEA = sector address
#HD per CYL = number of heads per cylinder
#SE per TRK = number of sectors per track

Note: Bit Ø of LAD Ø = the least significant bit.
Bit 4 of LAD 2 = the most significant bit.

4.6 INTERLEAVE COMPUTATION

The interleave mechanism on a track can be represented as follows.

Example: Interleave Code = 1Ø (decimal)
Maximum Sector Number = 33

The physical sectors are assigned the following logical sector numbers.

Phy. Sec.	Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12	13	14	15	16	17	18	19
Log. Sec.	Ø,	1Ø,	2Ø,	3Ø,	1,	11,	21,	31,	2,	12,	22,	32,	3,	13,	23,	33,	4,	14,	24,	5

Phy. Sec.	2Ø	21	22	23	24	25	26	27	28	29	3Ø	31	32	33
Log. Sec.	15,	25,	6,	16,	26,	7,	17,	27,	8,	18,	28,	9,	19	29

4.7 ERROR CODE DESCRIPTIONS

These error code descriptions are related to Byte Ø of the Sense Block after the Request Sense command (Class Ø, Opcode Ø3).

Type Ø (Drive) Error Codes

Ø	No status
1	No Index signal.
2	No Seek Complete.
3	Write fault
4	Drive not ready
5	Drive not selected.
6	No TrackØØ
7	Multiple winchester drives selected.
D	Seek in progress

Type 1 (Controller) Error Codes

Ø	ID read error. ECC error in the ID field.
1	Uncorrectable data error during a read.
2	ID Address Mark not found.
3	Data Address Mark not found.
4	Record not found. Found correct cylinder and head but not sector.
5	Seek error. R/W head positioned on a wrong cylinder and/or selected a wrong head.
6	Unused.
7	Write protected.
8	Correctable data field error.
9	Bad block found.
A	Format Error. The controller detected that during the Check Track command, the format on the drive was not expected.
C	Unable to read the Alternate Track address.
E	Attempted to directly access an Alternate Track.
F	Sequencer time out during disk or host transfer.

Type 2 (Command) Error codes

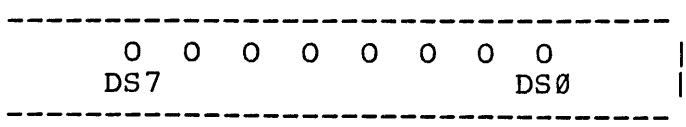
Ø	Invalid Command received from the host.
1	Illegal disk address. Address is beyond the maximum address.
2	Illegal function for the current drive type.
3	Volume overflow.

Type 3 (Misc) Error codes

Ø	RAM error. Data error detected during Sector buffer RAM diagnostic.

4.8 LED ERROR DISPLAY

The following error codes are displayed on the LEDs on the controller in conjunction with any error condition on the controller indicated by the Error bit in the Completion Status Byte.



Error Code (HEX)	Interpretation
ØØ	No Error
Ø1	No Index from drive
Ø2	No Track ØØ from drive
Ø3	Sector Address Out of Bounds
Ø4	Winchester disk not selected
Ø5	No Seek Complete from Winchester disk
Ø6	No ID Address Mark
Ø7	No Data Address Mark
Ø8	Seek Error (Cylinder or Head not correct)
Ø9	Sector not found
ØA	ID ECC error
ØB	Not used
ØC	Invalid Command
ØD	Incorrect DATA MARK
ØE	Incorrect ID MARK
ØF	Incorrect cylinder address from drive
1Ø	Incorrect sector address from drive
11	Incorrect head address from drive
12	Uncorrectable Data Error
13	Correctable Data Error
14	Drive not READY
15	Write fault
16	not used
17	Drive write protected
18	RAM diagnostic error
19 - 1E	not used
1F	Unable to read the Alternate Track Address
2Ø	Parity Error from host adaptor. If this error occurs, the host adaptor has a fault in the parity generation circuitry.
21	Bad Block detected from drive
22	Invalid function for this type
31	Attempted to directly access an alternate Track
32	Seek in progress
33	Volume overflow
81	Multiple Winchester disks selected. Fatal error.
82	Sequencer time-out during disk or Host transfer.

SECTION 5

DIAGNOSTIC PHILOSOPHY

5.1 ERROR INDICATORS

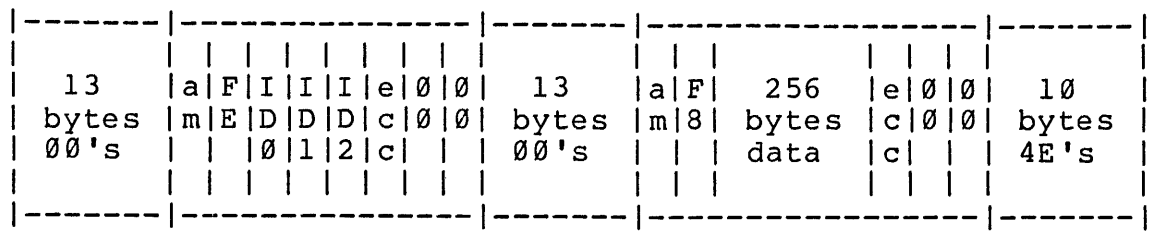
The controller contains 8 diagnostic LED error indicators. Each time an error occurs the controller deposits a value in the LED's and returns a failure status to the host adapter. The LED value can be decoded, but the error it indicates will always be available to the host software. The errors that are returned by the controller are very detailed. As a result, preliminary fault isolation is made fairly easily, narrowing the failure to the particular interface portion of the controller.

SECTION 6

SECTOR FORMATS

Winchester Drive Sector Formats

The track layout for the 256 bytes/sector 33 sectors/track is shown below.



am, FE, ID0, ID1, ID2, 00, F8 = 1 byte
ecc = 3 bytes

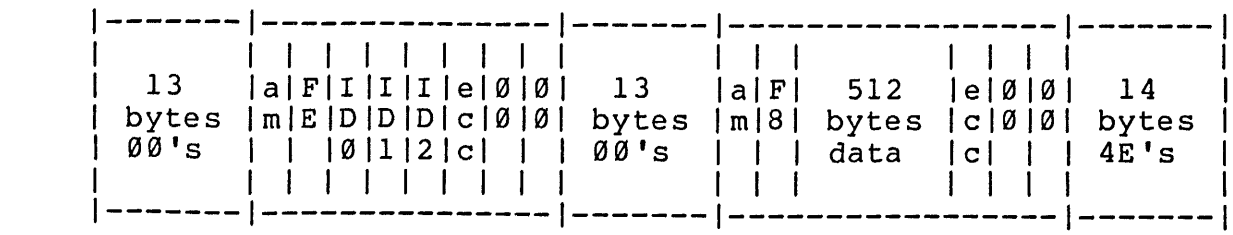
Track Capacity = 10416

16	= Index Gap (4E)
10197	= 33 sectors @ 309 bytes/sector
203	= Speed Tolerance Gap (4E)
10416	

309 bytes/sector including ID and overhead

This track format provides (+ or -) 1.77% speed tolerence.

The track layout for the 512 bytes/sector, 18 sectors/track is shown below.



am, FE, IDØ, ID1, ID2, ØØ, F8 = 1 byte
ecc = 3 bytes

Track Capacity = 10416

16	= Index Gap (4E)
10242	= 18 sectors @ 569 bytes/sector
158	= Speed Tolerance Gap (4E)
10416	

569 bytes/sector including ID and overhead

This track format provides (+ or -) 1.29% speed tolerence.