ECONORAM IX T.M.
USER'S MANUAL
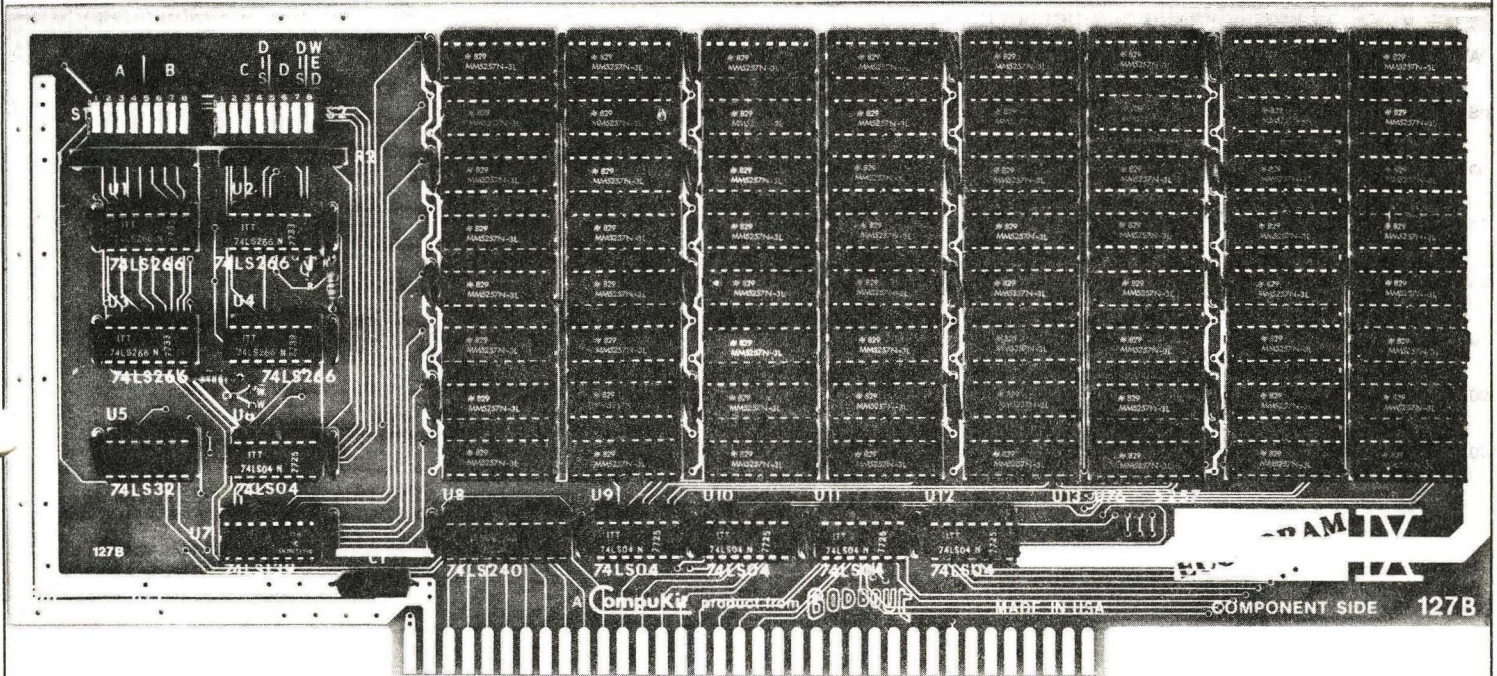
32K x 8 static memory
Digital Group Buss
using MM5257/TMS40L44 · 4MHz

2147

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ABOUT ECONORAM IX

Congratulations on your choice of the ECONORAM IX, a 32K x 8 memory board designed specifically for electrical and mechanical compatibility with the Digital Group buss.

All IC sockets, bypass capacitors, and other components, are soldered on the board in order to eliminate the most tedious and error-prone aspects of the assembly of this type of kit. Assembly should take only an hour or so. We encourage you to take the time to familiarize yourself with the features and the circuit design of the board prior to assembly. Several of the features - such as independent block organization, easy switch assignment of blocks to the desired memory address location, switch selectable block disable and write protect - have been unavailable to Digital Group System owners until now.

Upon completion of the board you will discover - as thousands of satisfied ECONORAM owners have discovered - the pleasure of using a fine memory board that just works, and works, and works.

As the first company to nationally offer memory kits to computer hobbyists, we thank you for choosing ECONORAM IX . . . welcome to the club.

TECHNICAL OVERVIEW

This board incorporates proven static memory technology using industrial design techniques and generous safety factors to avoid marginal operation.

Of the two currently popular approaches to memory design - static and dynamic - static memories are the overwhelming choice in applications where speed, simplicity, ease of use and reliability must be considered.

In order to retain data, dynamic memory must be continually refreshed. This board, due to its static design, will retain data as long as power is applied. This is of particular interest to Digital Group owners, since the Digital Group system makes use of the unique ability of the Z-80 CPU to take care of dynamic memory refresh rather than using refresh circuitry on each individual memory board. Unfortunately, while this is a valid and economical approach, it precludes the use of the normal system RESET or the use of the WAIT line since the CPU cannot continue to refresh the memory while RESET is held or CPU WAIT is used. For instance, in order to use the Digital Group disk controller with dynamic memory, both the controller board and the CPU board must be modified, an extra input port bit is required, and special software is necessary. The Econoram IX is not subject to the above problems because of its static design.

The individual memory chips used on this board are grouped together to form four blocks of memory: two 4K blocks, one 8K block and one 16K block. Each block may be assigned to any of its respective boundaries (i.e., either 4K block to any 4K boundary, the 8K block to any 8K boundary and the 16K block to any of the four 16K boundaries) by setting the starting address with the on-board DIP switches (no jumpers required). Additional features include a write-protect switch for the 16K block and disable switches for both the 8K and 16K blocks. Also included are jumper pads for adapting the board to non-standard polarities of the WRITE strobe and the ROM strobe (the signal which disables the board when the bootstrap EROM is being accessed). No jumpers are required for standard Digital Group systems, since traces have been provided to connect the pads for the standard signal polarities.

Extra heavy power supply traces, generous bypassing of power supply lines, sockets for all integrated circuits, careful layout and a double-sided, solder-masked printed circuit board with complete component and switch legends make this a versatile memory board which will give exceptionally long and trouble-free service.

Parts List

Upon receipt of your kit, check your parts against the list below.

- ☐ (1) Econoram IX circuit board

INTEGRATED CIRCUITS (note: the following parts may have letter suffixes and prefixes along with the key numbers given below).
- ☐ (64) MM5257 or TMS40L44 memories (U13-U76)
- ☐ (5) 74LS04 hex inverter (U6-U12)
- ☐ (1) 74LS32 quad 2-input OR gate (U5)
- ☐ (1) 74LS139 decoder / demultiplexer (U7)
- ☐ (1) 74LS240 TRI-STATE® buffer (U8)
- ☐ (4) 74LS266 ex-NOR o.c. (U1-U4)

OTHER ELECTRONIC COMPONENTS
- ☐ (2) S.I.P. resistor packs (R1, R2)*
- ☐ (2) 2K7 ohm ¼ watt resistors (red-violet-red R3, R4)*
- ☐ (1) 39 μF tantalum capacitor (C1)*
- ☐ (28) ceramic capacitors*

MECHANICAL COMPONENTS
- ☐ (76) low profile sockets*
- ☐ (2) 8 pole dipswitches (S1, S2)*
- ☐ (1) user manual

*supplied already soldered to board.

ASSEMBLY PROCEDURES

There is no soldering necessary to complete this kit, proper operation depends upon correct identification and handling of the parts used in its construction. Please read this manual *thoroughly* before assembly.

SOLDERING TECHNIQUES. Though no soldering should be required to complete assembly, you may have to 'touch up' an occasional void; or (heaven forbid) even replace a component at some future date. The Econoram board is *solder-masked* with a solder-resistant coating over the entire board, except where solder connections are made. This minimizes the chances of getting an unwanted *solder bridge* between adjacent traces.

Those who have not previously worked with a solder-masked board will find that it takes considerably less solder to make a good joint since the solder does not spread out across the solder pad. On this board, all soldering should be done on the *solder* side of the board (the back side or side opposite the component side). Use a low wattage iron (10-25 watts) with a small or 'PENCIL' tip. Use a good quality *rosin-core* solder ('60/40 alloy'). Because of the close spacing of pads we recommend keeping the component leads straight up while soldering (see figure 1). Bring the tip of the iron in at an angle, touching both the pad and the component lead, and feed a small amount of solder in at either side where the tip touches the pad and lead (see figure 2). Use only enough solder to fill the joint and make a very small 'fillet' around the lead. Keep the soldering iron on the joint only long enough to make sure that the solder has 'wetted' the lead and flowed smoothly into the joint; too little time may result in a poor joint and too much time may damage the component or the bond between the pad and the board. Be especially careful when soldering dipswitches, since some internal parts are thermoplastic and are very heat sensitive. Clip any excess leads off fairly close to the board to keep them from bending over and touching anything. Use eye protection while soldering or clipping leads.

NOTE: The use of any type of solder other than a good quality rosin-core solder invalidates the warranty. Do not use any type of solder paste or corrosive flux under any conditions.

> Any modification of this board not approved in advance by Godbout Electronics may void your warranty.

IDENTIFICATION OF PARTS. There are many ICs used in this kit; each one must be oriented correctly for proper operation. Most ICs have a dot near one corner that indicates pin 1 (see figure 3). Sometimes this dot appears in conjunction with a deeply cut notch or circle. Other types indicate the pin 1 end of the IC by a deep notch or a notch within a shallow circle (see figure 4). In case of doubt, place the IC in front of you so that any identifying numbers read from left to right; pin 1 is almost always in the lower left-hand corner (figure 5).

NOTE: If there is a recognizable mark for pin 1, always go by that rather than the printing.

HANDLING OF PARTS. All integrated circuits may be damaged by static electricity; however, MOS ICs - such as the memory ICs included with this kit - are more vulnerable than most. You can easily accumulate a static charge on your body in the thousands-of-Volts range by merely walk-

ing across a rug or sliding into a chair on a dry day. If you then touch the pins of an IC, this charge can flow through the IC and damage its internal structure. Most static discharges destroy the IC immediately, but it is possible for a low energy static discharge to puncture the gate oxide in such a manner than the IC functions properly for a while but fails some time later as metal migrates into the puncture and finally causes an internal short-circuit. To prevent this, leave the ICs in their protective foil until needed. Then, before plugging in each IC, touch an exposed trace on the board (pin 1 or 2 on the edge connector, for instance) to equalize any residual charge. This will force any charge to flow through your body instead of through the pins of the IC. Also, avoid wearing clothing which has a tendency to generate static charges (such as sweaters, almost all synthetic fabrics, and so on). (Industrial IC users recommend wearing a grounded wrist strap and working on a conductive surface which is grounded to the same point. Almost the same protection can be achieved by working on a sheet of aluminum foil which is electrically connected to the wrist with a flexible wire attached to a metal watch band or loop of bare wire around the wrist. If the aluminum foil can be conveniently grounded it will over even more protection).

● ● ●

Figure 1.

Figure 2.

Figure 3. **Figure 4.** **Figure 5.**

A B

D DW
C I D I E
S D S D

S1 S2

R1 R2

U1 U2

74LS266 74LS266 R1 R3 R

U3 U4

74LS266 R4 74LS266

C W W

U5 U6

74LS32 74LS04

AO
BO
CO
C1
DO
D1
D2
D3

U7

127B

C1

74LS139

U8 U9 U10 U11 U12 U13 - U76 = 5257

74LS240 74LS04 74LS04 74LS04 74LS04

ECONORAM IX

BM SC COPR. 1978 A **CompuKit** product from **GODBOUT** MADE IN USA COMPONENT SIDE 127B

COMPONENT SIDE

Component Layout

UP

CONSTRUCTION

Keeping the preceding information in mind, it is now time to mount the various components and install the ICs into their sockets. Orient the board as shown in the component layout; then referring to this layout, follow the steps below in the order given.

☐ **1.** Before inserting any components, check for any short circuits in the power distribution lines as follows:

A. If you are working on a conductive surface, insulate the board with a sheet of cardboard or other non-conducting material.

B. If the dipswitches on your board have already been installed, flip each switch to the OFF position.

C. Measure the resistance between pins 1 and 2 of the edgeboard connector with an ohmmeter (see figure 6a). The resistance should be (nearly) infinite. A reading below around 3000 ohms indicates a bad switch element and a reading near 0 ohms indicates an 'etch bridge' or solder bridge between the +5 and ground traces or (less likely) a shorted bypass capacitor.

☐ **2.** The board is shipped configured for an 'active low' memory write strobe and an 'active low' ROM access strobe ("PHANTOM" line in S-100 Systems). If you have a standard Digital Group system, skip this step. If you are assembling your board for use in a non-standard system, proceed as follows:

A. To configure the board for an 'active high' memory write strobe, cut the trace between 'c' and 'w bar' ($\overline{w}$) and install a jumper between 'c' and 'w' (see figure 6b).

B. To configure the board for an 'active high' ROM access strobe (the signal which disables RAM when the ROM is being accessed), cut the trace between 'c' and 'r bar' ($\overline{r}$) and install a jumper between 'c' and 'r' (see figure 6c).

☐ **3.** If you have a conductive work surface, remove the material which was insulating the board from it. All of the ICs should be oriented so that the pin 1 end is toward the left side of the board. Any numbers or other markings should normally be right side up with the board oriented normally (as shown in the component layout diagram). If any markings are upside-down, the IC may not be correctly installed.

A common problem with boards returned for repair is improper installation of an IC. Sometimes a pin will bend *under* the IC instead of going into the proper socket contact. We recommend inserting each IC halfway and verifying visually that all pins are started into the socket. Then, push the IC in the rest of the way.

Keeping this in mind, first insert the support ICs and then all of the memory ICs.

☐ **4.** Check the board over carefully for errors in construction. If all appears correct, assembly of your board is complete. Refer to the following sections for instructions on address selection and switch-selectable options.

Figure 6

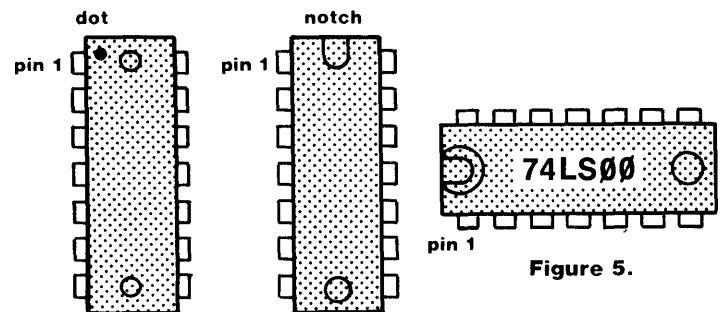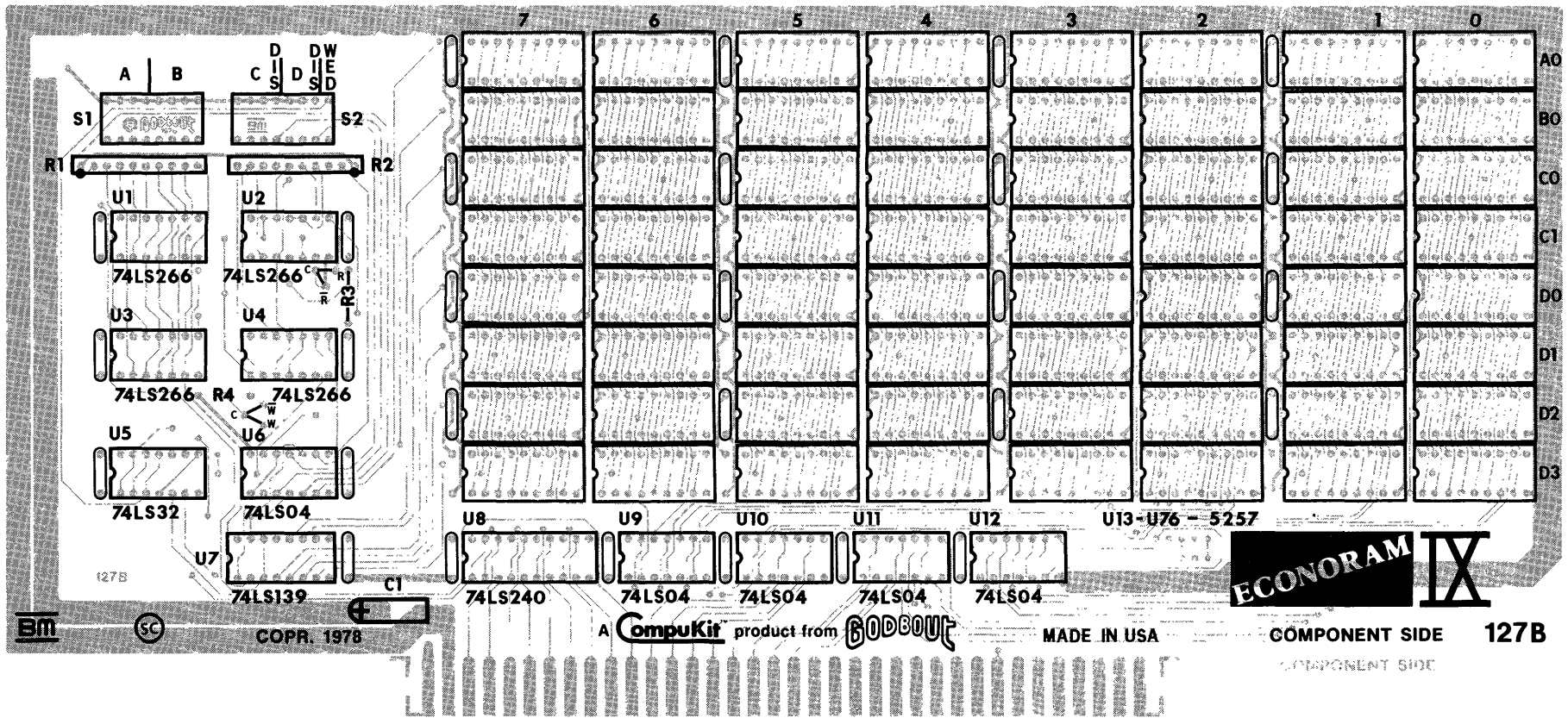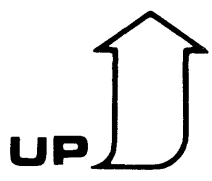**Figure 6a**

Figure 6b

Figure 6c

MEMORY ADDRESS ASSIGNMENT

This board is configured as two 4K blocks, one 8K block and one 16K block. Each 4K block may be assigned to any area of memory beginning on a 4K boundary (0K, 4K, 8K, 16K, etc.). The 8K block may be assigned to any 8K boundary (0K, 8K, 32K, 40K, etc.) and the 16K block on any 16K boundard (0K, 16K, 32K or 48K). The only other limitation is that the assigned locations should not overlap each other or any other RAM in your system.

NOTE: In the following table, S1 is the first dipswitch and S2 if the second dipswitch. Each dipswitch has eight individual switch sections numbered 1 through 8. "0" = switch off and "1" = switch on. S2-4, -7 and -8 are not used for address selection and are explained in the next section.

STARTING ADDRESS		SWITCH POSITION		
		BLOCK A, B	C	D
hex	(split octal)	4K	8K	16K
		A: S1-:1234	S2-:123	S2-:56
		B: S1-:5678		
0K 0000	(000/000)	0000	000	00
4K 1000	(020/000)	0001		
8K 2000	(040/000)	0010	001	
12K 3000	(060/000)	0011		
16K 4000	(100/000)	0100	010	01
20K 5000	(120/000)	0101		
24K 6000	(140/000)	0110	011	
28K 7000	(160/000)	0111		
32K 8000	(200/000)	1000	100	10
36K 9000	(220/000)	1001		
40K A000	(240/000)	1010	101	
44K B000	(260/000)	1011		
48K C000	(300/000)	1100	110	11
52K D000	(320/000)	1101		
56K E000	(340/000)	1110	111	
60K F000	(360/000)	1111		

NOTE: If the desired starting address is represented as a binary number, the switch setting represents the 2, 3, or 4 most significant bits of that address. Once you become familiar with the addresses of the various boundaries, you will find it easy to re-assign various boundaries, you will find it easy to re-assign memory blocks without referring to the above table.

BLOCK DISABLE SWITCHES

Switch S2-4 and S2-7 are disable switches for the 8K ("C") block and the 16K ("D") block respectively. These switches should be OFF for normal operation. If either switch is moved to the ON position, the corresponding block is effectively removed from memory (although as long as power is maintained, data previously stored in the block is not disturbed and may be re-accessed by returning the switch to the OFF position). This feature is primarily designed to allow the use of a partially populated board (any block without a full complement of memory ICs must be disabled to prevent conflicts if other RAM in the system is assigned an address which overlaps that of the incomplete block). However, the disable switch can also be used as an aid in trouble-shooting and as a *pseudo write-protect* to protect a section of code while de-bugging another program.

WRITE ENABLE SWITCH

Switch S2-8 is the WRITE ENABLE switch for the 16K ("D") block of memory. This switch should be ON for normal operation. However, if the switch is placed in the OFF position after data has been written into this block, the block will be WRITE PROTECTED and the data can be read but not changed. This is a very powerful tool for program development and debugging, since the data in the write protected block cannot be destroyed by a wayward program. You must remember, however, that data buffers which must be changed by the program must reside outside the protected area.

MEMORY TESTING

An excellent memory testing routine is distributed by the Digital Group which will test both the data integrity and the speed of the memory. If this is unavailable to you, we have included a test route (page 10) which gives the board a somewhat slow but thorough workout. It can be entered in machine code through the programming options in your operating system or in source code through an assembler (to use the Digital Group Assembler the mnemonics must be changed from INTEL 8080 mnemonics to Zilog Z-80 mnemonics).

The routine is initially set up to test a 32K segment of memory starting at 4000 hex and ending at BFFF hex. The starting address may be changed by entering the desired start address at 3001 and 3002 hex (low byte first). The ending address may be changed by entering the high byte of the address following the last tested byte at 3004 hex (if the test is to end at E7FF hex, enter E8 at 3004).

If the memory passes the test, it starts over again. Three bytes have been left open at "MARK" (3039 hex) to enable you to insert a call to a routine to display the test address if desired.
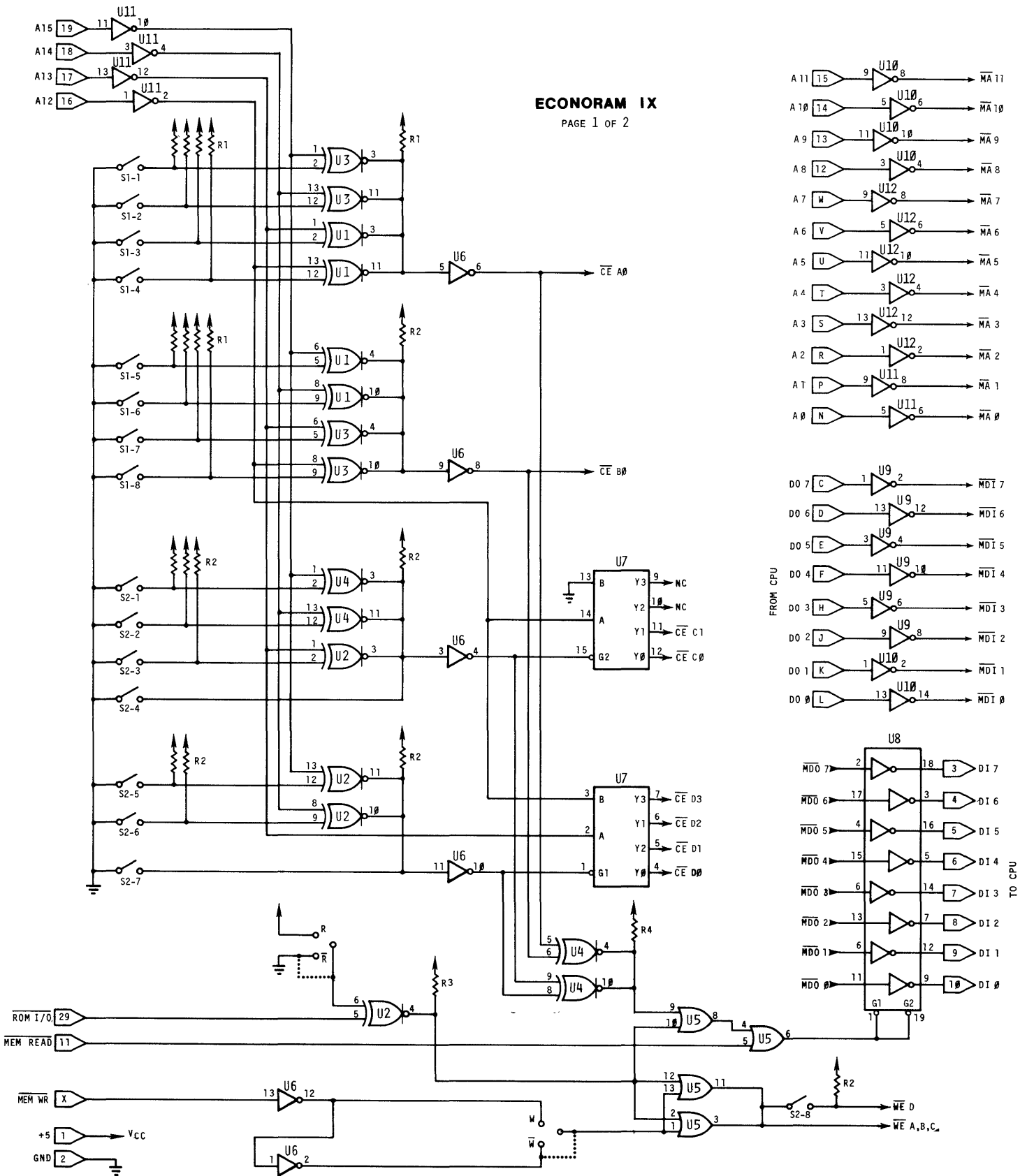
If any portion of memory fails the test, critical information is stored and the routine enters an endless loop at "SHLT" (307D hex). This "jump to itself" may be replaced by a "jump to a routine" which notifies you of the failure, or the loop may be terminated by a RESET to your monitor, from which you can examine the following locations where the information regarding the failure is stored:
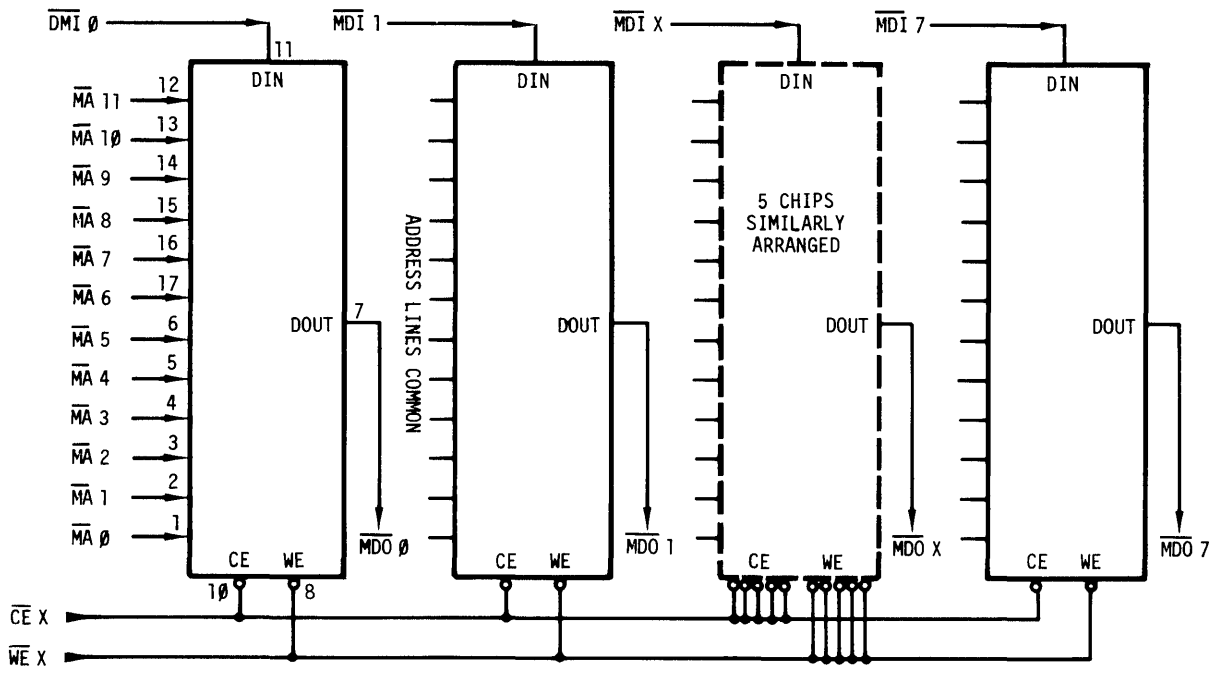
3069	"FDE"	test character
306A	"FDE"+1	fill character
306B	"FHL"	failure address (low-high)
306D	"FOUT"	data expected at this address
306E	"FIN"	data read from this address

The difference between "FOUT" and "FIN" should indicate which bit is failing, and together with "FHL" should point to the bad memory IC. If several bits are different, the problem could be an address decoding problem caused by the failure of one of the support chips.
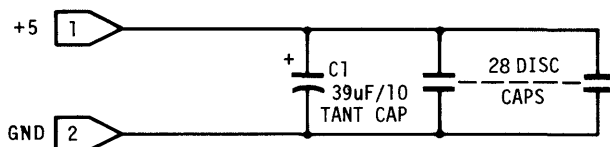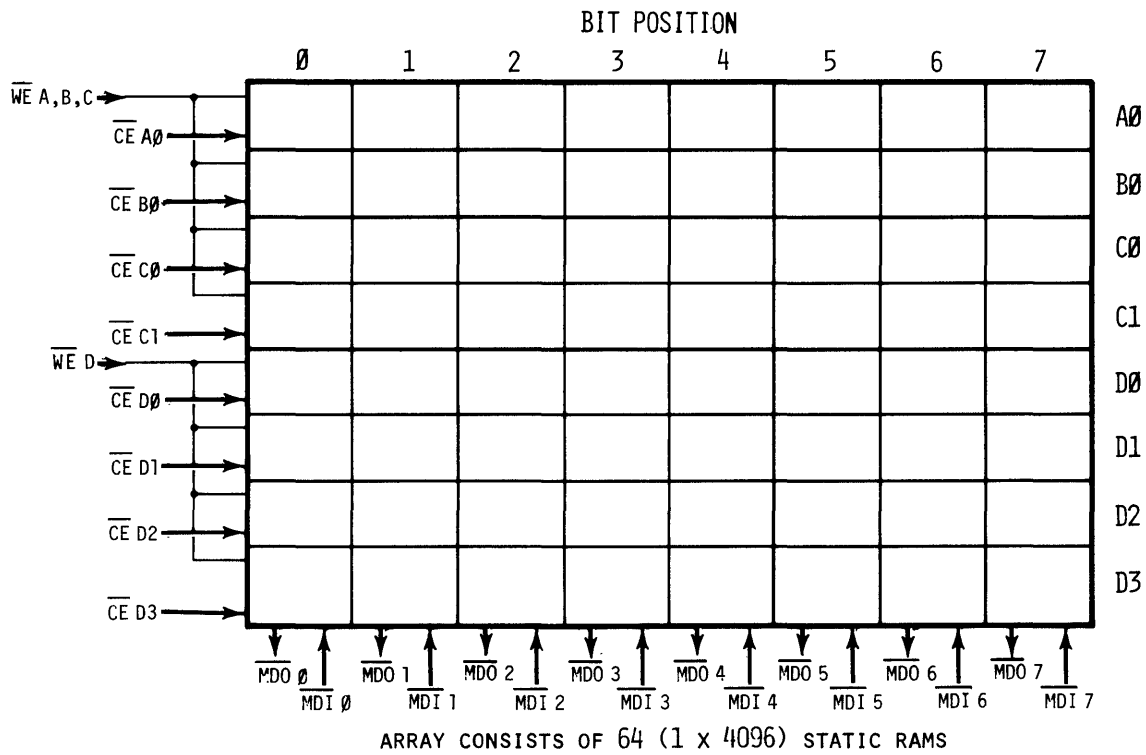
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$\overline{DMI}\ 0$ $\overline{MDI}\ 1$ $\overline{MDI}\ X$ $\overline{MDI}\ 7$

DIN   DIN   DIN   DIN

11

$\overline{MA}\ 11$ — 12
$\overline{MA}\ 10$ — 13
$\overline{MA}\ 9$ — 14
$\overline{MA}\ 8$ — 15
$\overline{MA}\ 7$ — 16
$\overline{MA}\ 6$ — 17
$\overline{MA}\ 5$ — 6
$\overline{MA}\ 4$ — 5
$\overline{MA}\ 3$ — 4
$\overline{MA}\ 2$ — 3
$\overline{MA}\ 1$ — 2
$\overline{MA}\ 0$ — 1

ADDRESS LINES COMMON

5 CHIPS SIMILARLY ARRANGED

DOUT   7   DOUT   DOUT   DOUT

CE   WE   CE   WE   CE   WE   CE   WE

10   8

$\overline{MDO}\ 0$ $\overline{MDO}\ 1$ $\overline{MDO}\ X$ $\overline{MDO}\ 7$

$\overline{CE}\ X$

$\overline{WE}\ X$

BIT POSITION

	0	1	2	3	4	5	6	7	
$\overline{WE}\ A,B,C$									A0
$\overline{CE}\ A0$									B0
$\overline{CE}\ B0$									C0
$\overline{CE}\ C0$									C1
$\overline{CE}\ C1$									D0
$\overline{WE}\ D$									D1
$\overline{CE}\ D0$									D2
$\overline{CE}\ D1$									D3
$\overline{CE}\ D2$									
$\overline{CE}\ D3$									

$\overline{MDO}\ 0$ $\overline{MDI}\ 0$ $\overline{MDO}\ 1$ $\overline{MDI}\ 1$ $\overline{MDO}\ 2$ $\overline{MDI}\ 2$ $\overline{MDO}\ 3$ $\overline{MDI}\ 3$ $\overline{MDO}\ 4$ $\overline{MDI}\ 4$ $\overline{MDO}\ 5$ $\overline{MDI}\ 5$ $\overline{MDO}\ 6$ $\overline{MDI}\ 6$ $\overline{MDO}\ 7$ $\overline{MDI}\ 7$

ARRAY CONSISTS OF 64 (1 x 4096) STATIC RAMS

+5   1

GND   2

C1
39uF/10
TANT CAP

28 DISC
CAPS

MEMORY TESTING ROUTINE

3000	21 00 40		0010	STRT	LXI	H,4000H
3003	3E A0		0020	END	MVI	A,0A0H
3005	32 6E 30		0030		STA	FIN
3008	3E 10		0040		MVI	A,10H
300A	84		0050		ADD	H
300B	4F		0060		MOV	C,A
300C	16 00		0070		MVI	D,0
300E	1E FF		0080		MVI	E,0FFH
3010	22 65 30		0090	DONE	SHLD	STAD
3013	AF		0100		XRA	A
3014	47		0110		MOV	B,A
3015	7B		0120	SCND	MOV	A,E
3016	5A		0130		MOV	E,D
3017	57		0140		MOV	D,A
3018	79		0150		MOV	A,C
3019	2A 65 30		0160		LHLD	STAD
301C	72		0170	FILL	MOV	M,D
301D	23		0180		INX	H
301E	BC		0190		CMP	H
301F	C2 1C 30		0200		JNZ	FILL
3022	2A 65 30		0210		LHLD	STAD
3025	73		0220	NEXT	MOV	M,E
3026	7B		0230		MOV	A,E
3027	BE		0240		CMP	M
3028	C2 6F 30		0250		JNZ	FAIL
302B	79		0260		MOV	A,C
302C	23		0270		INX	H
302D	94		0280		SUB	H
302E	C2 4D 30		0290		JNZ	NDON
3031	B8		0300		CMP	B
3032	44		0310		MOV	B,H
3033	CA 15 30		0320		JZ	SCND
3036	3A 66 30		0325		LDA	STAD+1
3039	00		0330	MARK	NOP	
303A	00		0331		NOP	
303B	00		0332		NOP	
303C	3A 6E 30		0340		LDA	FIN
303F	B9		0350		CMP	C
3040	CA 00 30		0360		JZ	STRT
3043	79		0370		MOV	A,C
3044	67		0380		MOV	H,A
3045	2E 00		0390		MVI	L,0
3047	C6 10		0400		ADI	10H
3049	4F		0410		MOV	C,A
304A	C3 10 30		0420		JMP	DONE
304D	22 67 30		0430	NDON	SHLD	NXAD
3050	7A		0440	LOPB	MOV	A,D
3051	BE		0450	LOPA	CMP	M
3052	C2 6F 30		0460		JNZ	FAIL
3055	2C		0470		INR	L
3056	C2 51 30		0480		JNZ	LOPA
3059	79		0490		MOV	A,C
305A	24		0500		INR	H
305B	BC		0510		CMP	H
305C	C2 50 30		0520		JNZ	LOPB
305F	2A 67 30		0530		LHLD	NXAD
3062	C3 25 30		0540		JMP	NEXT
3065			0550	STAD	DS	2
3067			0560	NXAD	DS	2
3069			0570	FDE	DS	2
306B			0580	FHL	DS	2
306D			0590	FOUT	DS	1
306E			0600	FIN	DS	1
306F	22 6B 30		0610	FAIL	SHLD	FHL
3072	32 6D 30		0620		STA	FOUT
3075	7E		0630		MOV	A,M
3076	32 6E 30		0640		STA	FIN
3079	EB		0650		XCHG	
307A	22 69 30		0660		SHLD	FDE
307D	C3 7D 30		0670	SHLT	JMP	SHLT
3080			0680	*		

┌─────── SUGGESTED ADDITIONS TO DIGITAL GROUP ───────┐
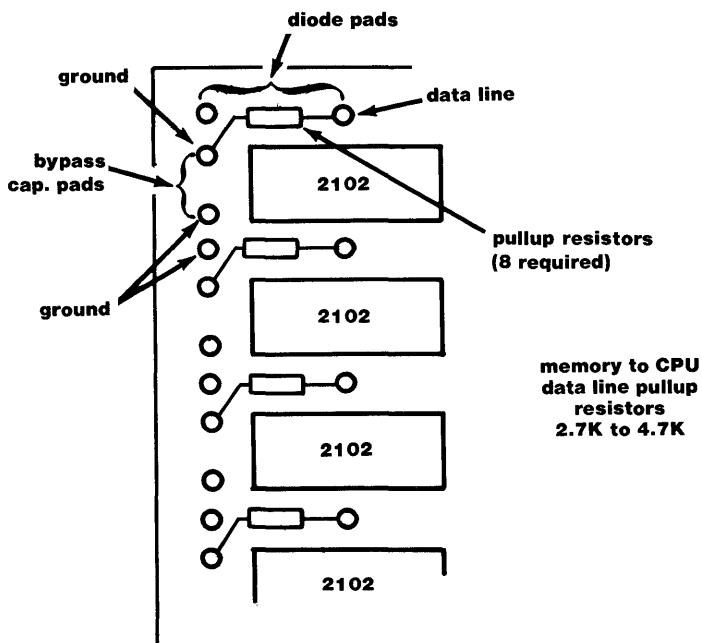## Z-80 CPU BOARD *

The following comments and fixes have been reported to us by digital group users:
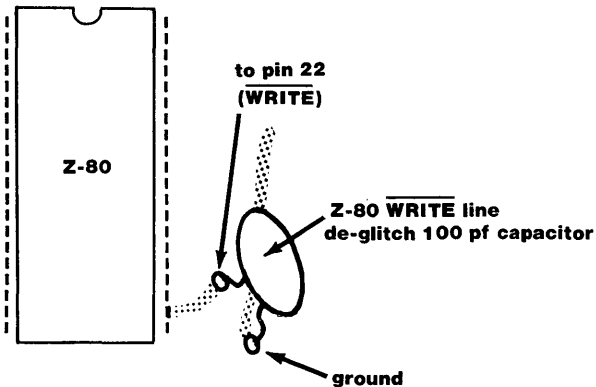
The data lines from memory to the CPU are not terminated on the Digital Group Z-80 CPU board, and because of this the CPU will occasionally get a data byte other than "FF" when accessing a non-existent memogxkmtqkuwxvs with programs (such as the Digital Group Memory Test Routines) which use this to find memory limits. These lines should be pulled up to +5 through 2.7K resistors (3.9K and 4.7K resistors have been used with satisfactory results). A convenient location to install these pullup resistors is on the *left-hand* side of the CPU board. Above each 2102 location in the first column of IC's two unused plated-through holes are provided (for undershoot clamping diodes). The right-hand hole is connected to its respective data line. Also, on the left side of each of these 2102's are two unused plated-through holes for bypass capacitors. The pullup resistors may be connected from the top hole (+5) of each of these pairs to the right-hand diode pad (data line) above each 2102.

There is an occational glitch on the "WRITE" line of some Z-80's which, if not corrected, can be a problem. With memory (such as this board) fast enough to respond to it, the glitch can write garbage into whichever location happens to be on the address buss at the time. The problem can be easily corrected by the addition of a 100 pF capacitor between pin 22 of the Z-80 and ground on the CPU board. Two plated-through holes connected to these lines are conveniently located near the lower right corner of the Z-80 and may be used to install the capacitor.

Although the above problems may not be noticeable on your system, we feel that the addition of the recommended fixes will add an extra measure of reliability to it and perhaps help you to avoid those inexplicable program crashes.

* These mods will help any system, but are mandatory for successful 4MHz operation.

diode pads

ground

data line

bypass cap. pads

2102

pullup resistors (8 required)

ground

2102

memory to CPU data line pullup resistors 2.7K to 4.7K

2102

2102

to pin 22
(WRITE)

Z-80

Z-80 WRITE line
de-glitch 100 pf capacitor

ground

Data to be written into a memory location is buffered and presented to the data in pins of each column of memory ICs. However, when a memory write strobe is received from the CPU, the data is loaded into the addressed location of the enabled row of ICs only.

When the output of a logic IC changes state, it draws a very short high-current 'spike' from the power lines. If unchecked, the electrical noise created by these transient spikes might couple into the logic lines and cause erratic operation of the board. To absorb these transients, bypass capacitors are liberally placed across the power distribution lines throughout the memory array and at every support IC.

This board is guaranteed to operate at 4.0 MHz over the full temperature range 0° to 70° C. and to draw less than 3500 mA (3.5 amps). The typical measured current draw is less than 3000 mA at cold start-up, rapidly decreasing to around 2400 to 2800mA as the board warms up.

It is interesting to note that static RAM technology has progressed to the point at which this high performance static RAM board is comparable in cost and power consumption to dynamic memory boards.

CIRCUIT DESCRIPTION

The heart of ECONORAM IX is the MM5257-3L or TMS40L44-25 memory IC (RAM), which can store 4096 bits ("4K" bits) of information (thus, each is a "4K x 1" memory IC). These are not standard MM5257/TMS40L44's, the memory ICs included in this kit are specifically tested and designated by the manufacturer as low power, high speed parts.

These ICs are arranged in rows that are 8 ICs wide - each IC contributing one bit of an 8-bit byte. Thus each row can store 4K x 8 bits (4K bytes). By connecting 8 of these rows together in parallel, a total of 32K bytes of memory storage is produced. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array and the row number corresponding to the 4K segment within a given block is indicated along the right hand edge of the array).

Now that we have this storage, there are other aspects to consider in order to be able to make use of it: First, addressing a specific location in memory; and second, writing data into the memory or reading data from it.

The logic diagram on pages 8 and 9 show the address decoding, read/write control, memory array, input buffering and output buss driver circuits for the Econoram IX. Each row of memory ICs requires 12 address bits (A0-A11) to select one unique location of the 4096 available locations. These bits are brought onto the board through inverting buffers (so as to present only one low-power TTL load to the buss) and distributed to the 12 address select pins on each of the memory ICs. The remaining 4 address bits are also buffered/ decoded, and if they represent a valid address for the board (as determined by the settings of the address select switches), used to enable the appropriate row of memory ICs.

When a row of ICs is thus enabled, it presents the data byte stored at the addressed location to the output buss driver. This IC is normally in a high-impedance state (essentially disconnected). When a valid address has been received and a MEMORY READ strobe is received from the CPU, the output driver places the selected data onto the data buss to the CPU.

THANK YOU

This board is the result of much time, work and experience on the part of a number of people. In addition to thanking you for choosing this board, we'd like to thank the Phantom* and many others for their help with this project.

We strive for a board that doesn't just work the first time, but continues to give reliable operation for a long time. If we can be of any help to you in applying this board, or if you have any questions, please let us know. As always, we solicit your comments, letters and new product suggestions.
HAPPY COMPUTING!

*Editor's Note: 'THE PHANTOM' is Doug Bell, who provided the impetous for producing this kit and then wrote these instructions using a word processor/text editor on his Digital Group System which included prototypes of this memory and a disk system of his own design.

CUSTOMER SERVICE INFORMATION

Our paramount concern is that you be satisfied with any Godbout CompuKit product. If this product fails to operate properly, it may be returned to us, see warranty information below.

If you have any questions about assembly, performance, specifications or need further information feel free to write us at:

P.O. Box 2355, Oakland Airport, CA 94614.

When writing, please be as specific as possible concerning the nature of your query. We maintain a 24 hour a day phone, for taking orders, (415) 562-0636. If you have problems or questions which cannot be handled by mail, this number can be used to connect you with our technical people ONLY during normal business hours (10am-5pm Pacific Time). Unfortunately, we cannot return calls, or accept collect calls.

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We are not responsible for damage caused by use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications other than those intended by Godbout Electronics, theft, fire, or accidents.

Return to purchaser of a fully functioning unit meeting all advertised specifications in effect as of date of purchase is considered to be complete fulfillment of all warranty obligations assumed by Godbout Electronics. This warranty covers only products marketed by Godbout Electronics and does not cover other equipment used in conjunction with said products. We are not responsible for incidental or consequential damages.

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