DIGITAL GROUP INPUT/OUTPUT CARD

General Design

The Digital Group I/O Card provides four 8-bit input ports and four 8-bit output ports. Decoding of port assignments is provided on the card as desired. A dual 36-pin connector provides external interface from/to the I/O board. A dual 22-pin connector provides interface to the driving microprocessor as well as supplying the needed voltages. This I/O board may be used with 16 or more bit microprocessors by using paralled board sets.

The I/O Card input ports are designed to interface to external TTL levels, and using the 7401's, a load of one TTL load will be placed on the external standard driving circuitry. The output data bits from the input ports are inverted. A simple interfacing/multiplexing circuit will be shown which allows attaching as many I/O cards as desired.

The I/O Card output ports interface to external circuitry with a driving capacity of up to 10 standard TTL loads. The driving data from the microprocessor is non-inverted. When driving long external data lines, line drivers are recommended to minimize noise pickup.

The I/O Card port decoding allows up to 65 thousand ports assignment in groups of four ports (16,384 possible combinations). While no one will use this many ports, several newer microprocessor designs address I/O as memory, meaning that a full addressing capability on each card is required to support such a design fully. Generally the full addressing capability is not required, and a number of parts may be omitted for most designs. A simplified picture is included to show addressing the I/O Card as ports 0-3 or ports 4-7.

Construction

The bulk of the assembly consists of placing the IC sockets in the board and soldering. Be sure to obtain a good solder connection at each pin. Avoid solder bridges between pins. Notice that the sockets are inserted on top side of the board, identified by the Digital Group label in the upper left.

After soldering in the 23 sockets, solder in the .01 disc bypasses. Plug in the 74100's (outputs) and 7401's (inputs), making sure that the keyed end or pin 1 is facing the top of the card (away from the socket end).

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Next, plug in IC's 9, 10, 11, 12, 18, 19, 21 and 23, also keeping pins 1 up. These IC's are capable of supporting up to 256 ports (64 different I/O cards), standard with such microprocessors as 8008 and 8080, and typical with microprocessors using "memory mapped I/O", such as 6800 and 650(X).

If using a scheme requiring full address mapping, also plug in IC's 13, 20 and 22, again making sure that all pin 1's are up.

Measure the resistance between pins 1 & 2 (top side) of the 22-pin connector. Since different voltmeters will result in a different value reading, what you are looking for is not a dead short between pins 1 & 2, and a very different resistance value should be given when on a low ohm scale and the leads to pins 1 & 2 are reversed. A dead short is generally caused by a bad IC. Very close low ohm readings are caused by accidentally reversing one or more IC's.

Jumpers in General

The needed jumpers are then inserted. If using the Digital Group System, merely follow the pictures included with the Digital Group System manual, Port 0-3 connections being required for the 1st I/O card.
If custom wiring for use elsewhere, then an understanding of the jumper functions is required.

No assumptions as to "addresses In" and "pulses" (strobes) have been made, so that a completely flexible board results, although this flexibility does result in some added complexity. The following circuit descriptions should enable you to make the correct jumper selections.

Circuit Description

Inputs to the microprocessor utilized are handled by the 7401 quad 2 input collector NAND Gates. Only if both inputs to a 7401 section are at a TTL "1" level, will the output go low or "Ø". By connecting one of the input legs externally and using the other leg as a gating strobe, a gated but inverted output results. An ungated section will have a "Ø" on its gating input, resulting in a high impedence state being outputed. Therefore, any reasonable number of inputs may have their outputs directly connected together, and only the 7401 section which has a "1" level input will be capable of controlling the common output line. All input ports share a common bus taking the selected input data to the microprocessor's data bus.

Output ports are handled by a 74100 assigned to each 8-bit output port required. Each 74100 is an 8-bit latch. Eight bits of data

from the microprocessor's data bus are held in a selected 74100. A given 74100 is selected by having its strobe lines (pins 12 and 23) momentarily go to a "1" level. Valid data is then externally available from that port.

Decoding of the Read and Write strobes comprises the rest of the circuitry. Just remember that the end result is a "1" pulse at the gating pins of the desired input port, or a "1" pulse at the strobe pulse of the selected output port. Two 7402 NOR gates are used for port steering, IC10 used for one of the four input ports selecting, and IC11 used for one of the four output ports strobing. A common leg of IC11 goes over towards a general output enabling input through IC23. This common leg must be at a Ø level for any output strobe to occur.

Similarly, IC10 has common gating inputs which must also be at a Ø level for any input port strobing to occur. Most microprocessor architecture does not require a common input port select at the card level, so generally the common input port is tied to ground (the jumper below IC8 performs this function). If common read strobing is desireable however, two sections of IC18 are available for buffering or inversion, again giving design flexibility. If your design has a "Ø" Read Strobe, then use the double inverter for non-inversion with one TTL load on the microprocessor. A design with a "1" Read Strobe uses only the first section for strobe inversion, but still presenting one TTL load on the microprocessor.

Output strobing does generally use a card level Write Strobe pulse besides the usual port addressing scheme. This is fed to the common legs of IC11, as previously mentioned, through two sections of IC23. The buffering/inversion system is used so that ~~Write Strobe~~ is buffered, or, Write Strobe is $\overline{\text{inverted}}$. The jumper besides IC23 at the bottom right controls $\overline{\text{Write}}$ (○---○) or Write (○~---○).

The 7442 (IC9) selects which of four inputs/outputs (if any) on the card is to be selected. A Ø level at the two inputs of any 7402 will result in the appropriate "1" strobe to input and/or output port. The inputs to the 7442 on pins 15, 14, 13 and 12, along with 7430's, IC12 and IC13 permit mapping the ports to 65,536 different combinations. IC13 and IC12 must both result in a "Ø" level output to pins 13 and 12 of the 7442 to permit any port operations from this I/O card. Pins 15 and 14 select which of the four ports are to be utilized. IC18 is used as a buffer/inverter as required, normally connected as shown in the pictorial.

The final gating operation is the 7430's. If only 256 ports or less at the bottom end of storage are required, IC's 13, 20 and 22 may be omitted, and the grounding jumper beneath IC13 inserted. IC's 21, 19, 22, 20 and 23 provide the buffering/inverting needed to decode the 16K possible port assignments.

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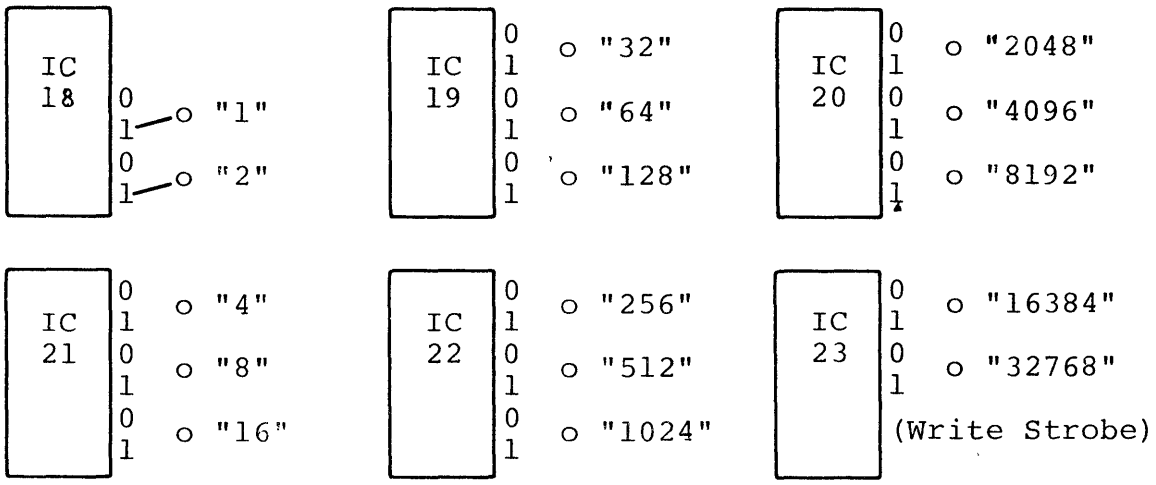
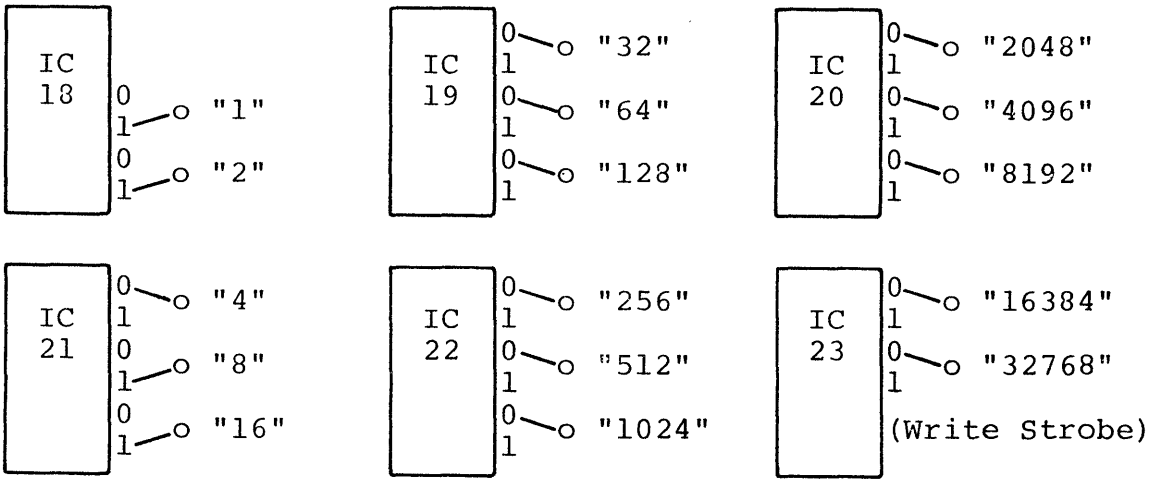
The jumpers are set in a binary relationship to derive the four port assignment of the card.



To determine a special jumper pattern, first determine the highest port number to be assigned on the card, e.g. a card for ports 24, 25, 26 and 27 will have 27 as its highest port number. Next determine the binary set of numbers required to sum to this port number, e.g. 27=16+8+2+1. Finally, connect the jumpers such that values required in the sum are connected between the sum value pin and the "1" pin. Values not required in the sum are connected between the value pin and the "Ø" pin of the set.

Following these rules for our ports 24-27 card:



Ports 24-27 Card

Cards should have their lowest port number an integral multiple of four, and this means the "1" and "2" jumpers would always be at the one state.

Troubleshooting the Digital Group I/O Card

The most likely problem will be missing or misplaced jumpers.

Another problem area that can arise is to mistake I/O cards and have the wrong ports card in a socket. Be sure to mark each I/O Card with its port assignments. Note that the lowest order port of the four will be at left of the card (looking at the IC's with the socket down).

IC's, socket connections, and socket pin soldering can be trouble-spots which can be very misleading. The Digital Group uses special plating to avoid these troubles. To spot these troubles, probe at the top side of the IC, right where the leads go inside the IC. Look out for levels between +.8 and +2.0 volts which generally indicate a floating input.

Actually chasing down a stubborn problem can best be attacked by looking for the gating pulses. If neither input nor output is functioning, look around the 7442 inputs as a starter. 7442 pins 12 and 13 should be going "Ø" simultaneously at some point. If this is occuring then check for a "1" output from the appropriate 7402 section(s).

If only write or read is not working concentrate on IC11 or IC10 respectively. Look for paired "Ø" in, and "1" strobes out to the selected port.

If you are hopelessly lost, the Digital Group will repair your I/O Card for a flat fee of $7.50. Be sure to indicate the port assignment when returning the card(s), or it will be impossible to determine the nature of the problem.

Using the Digital Group I/O Cards

The 36-pin sockets were specified to permit easy attachment of 8 conductor Molex connectors and flat cable. These connectors and cable are available from the Digital Group at 20¢ per foot for cable and 50¢ per connector.

The card is designed to plug into the Digital Group I/O Bus System to permit easy customized connection and movement. If user designed I/O accessories are designed using dual 36 and dual 22 pin connectors, a minimum amount of interface difficulty will result.

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INPUT/OUTPUT PORT CONNECTIONS

Top of Card - Component side				Bottom of Card - Circuit side			
Pin No.	Description	bit		Pin No.	Description	bit	
1	LSB	Ø		A	LSB	Ø	
2	LSB+1	1		B	LSB+1	1	
3	LSB+2	2		C	LSB+2	2	
4	LSB+3	3	Input	D	LSB+3	3	Output
5	MSB-3	4	Port Ø,4,8,..	E	MSB-3	4	Port Ø,4,8,...
6	MSB-2	5		F	MSB-2	5	
7	MSB-1	6		H	MSB-1	6	
8	MSB	7		J	MSB	7	
9	n/c			K	n/c		
10	LSB	Ø		L	LSB	Ø	
11	LSB+1	1		M	LSB+1	1	
12	LSB+2	2		N	LSB+2	2	
13	LSB+3	3	Input	P	LSB+3	3	Output
14	MSB-3	4	Port 1,5,9,...	R	MSB-3	4	Port 1,5,9,...
15	MSB-2	5		S	MSB-2	5	
16	MSB-1	6		T	MSB-1	6	
17	MSB	7		U	MSB	7	
18	n/c			V	n/c		
19	LSB	Ø		W	LSB	Ø	
20	LSB+1	1		X	LSB+1	1	
21	LSB+2	2		Y	LSB+2	2	
22	LSB+3	3	Input	Z	LSB+3	3	Output
23	MSB-3	4	Port 2,6,10,...	$\overline{A}$	MSB-3	4	Port 2,6,10,...
24	MSB-2	5		$\overline{B}$	MSB-2	5	
25	MSB-1	6		$\overline{C}$	MSB-1	6	
26	MSB	7		$\overline{D}$	MSB	7	
27	n/c			$\overline{E}$	n/c		
28	LSB	Ø		$\overline{F}$	LSB	Ø	
29	LSB+1	1		$\overline{H}$	LSB+1	1	
30	LSB+2	2		$\overline{J}$	LSB+2	2	
31	LSB+3	3	Input	$\overline{K}$	LSB+3	3	Output
32	MSB-3	4	Port 3,7,11,...	$\overline{L}$	MSB-3	4	Port 3,7,11,...
33	MSB-2	5		$\overline{M}$	MSB-2	5	
34	MSB-1	6		$\overline{N}$	MSB-1	6	
35	MSB	7		$\overline{P}$	MSB	7	
36	n/c			$\overline{R}$	n/c		

Note: MSB = Most Significant Bit
LSB = Least Significant Bit
n/c = no connection

INPUT/OUTPUT BUS

Top of Card - Component side			Bottom of Card - Pin side		
Pin No.	Use		Pin No.	Use	
1	+5V		A	+5V	
2	Ground		B	n/c	
3	MSB	Input	C	MSB	Output
4	MSB-1	Bus -	D	MSB-1	Bus -
5	MSB-2	Data to	E	MSB-2	Data from
6	MSB-3	CPU	F	MSB-3	CPU
7	LSB+3		H	LSB+3	
8	LSB+2		J	LSB+2	
9	LSB+1		K	LSB+1	
10	LSB		L	LSB	
11	Input Strobe		M	Spare	
12	MSB-7		N	LSB	
13	MSB-6		P	LSB+1	
14	MSB-5	Port	R	LSB+2	Port
15	MSB-4	Address	S	LSB+3	Address
16	MSB-3	Lines	T	LSB+4	Lines
17	MSB-2		U	LSB+5	
18	MSB-1		V	LSB+6	
19	MSB		W	LSB+7	
20	n/c		X	Output Strobe	
21	n/c		Y	n/c	
22	n/c		Z	n/c	

Note: MSB = Most Significant Bit
LSB = Least Significant Bit

INPUT/OUTPUT Parts List

IC1 - 8	7401
IC9	7442
IC10-11	7402
IC12-13	7430
IC14-17	74100
IC18-23	74L04 or 7404

All capacitors are
.01 mfd disc. (=6)

Miscellaneous:

IC Sockets

18 - 14pin
1 - 16pin
4 - 24pin

Connectors

1 - 22 pin dual readout
.156" centers

1 - 36 pin dual readout
.156" centers

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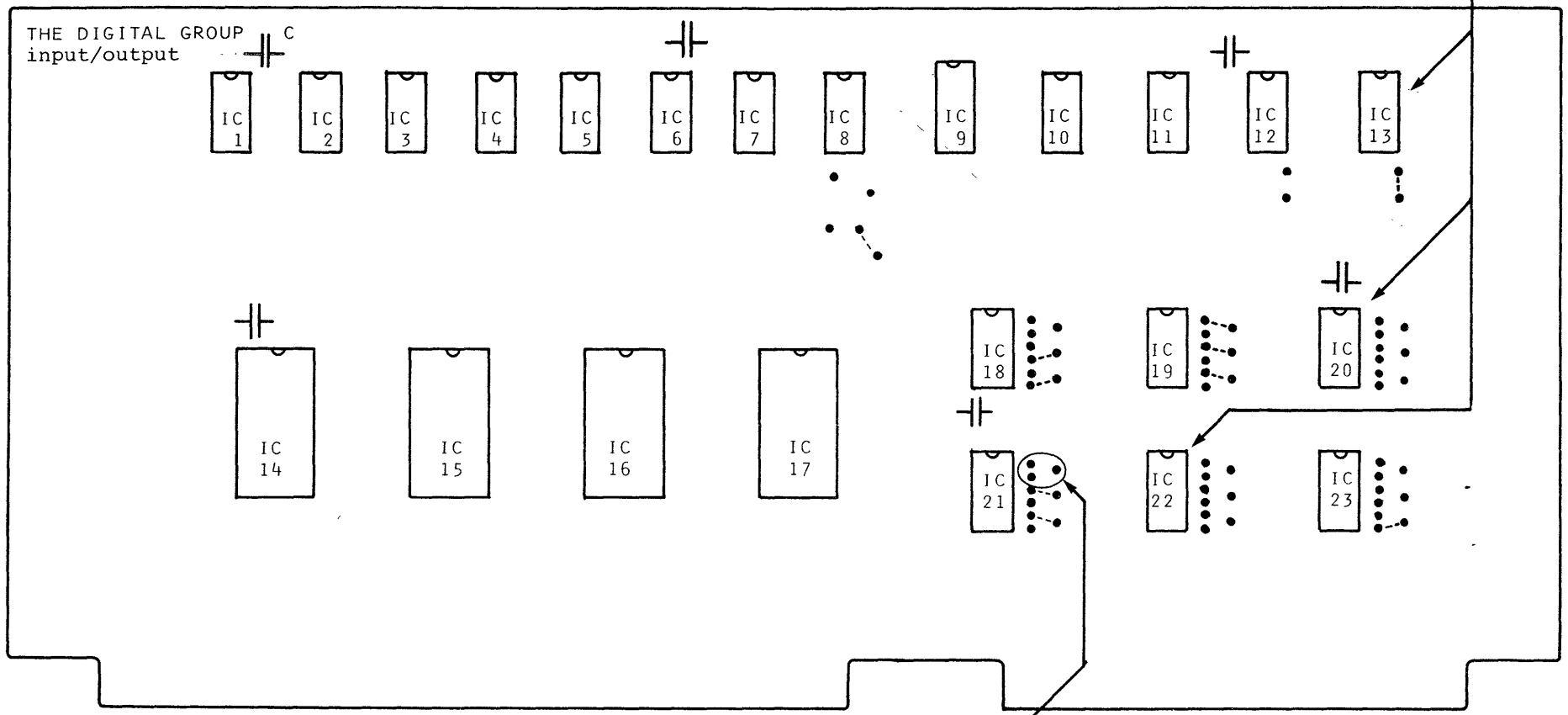
INPUT/OUTPUT

COMPONENT LAYOUT

DIOCL-1-R0

MOST FREQUENTLY UTILIZED
CONNECTIONS SHOWN

THESE IC'S USED ONLY
WITH FULL MEMORY MAPPING



NOTES: ALL IC'S HAVE KEYED END (PIN 1 END) UP.
DOTTED LINES SHOW STRAPPING FOR PORT
NUMBERS 0 - 3 OR 4 - 7. ICS #13, 20,
AND 22 ARE OMITTED WHEN STRAPPED AS SHOWN.

PORT Ø - 3

OR

PORT 4 - 7

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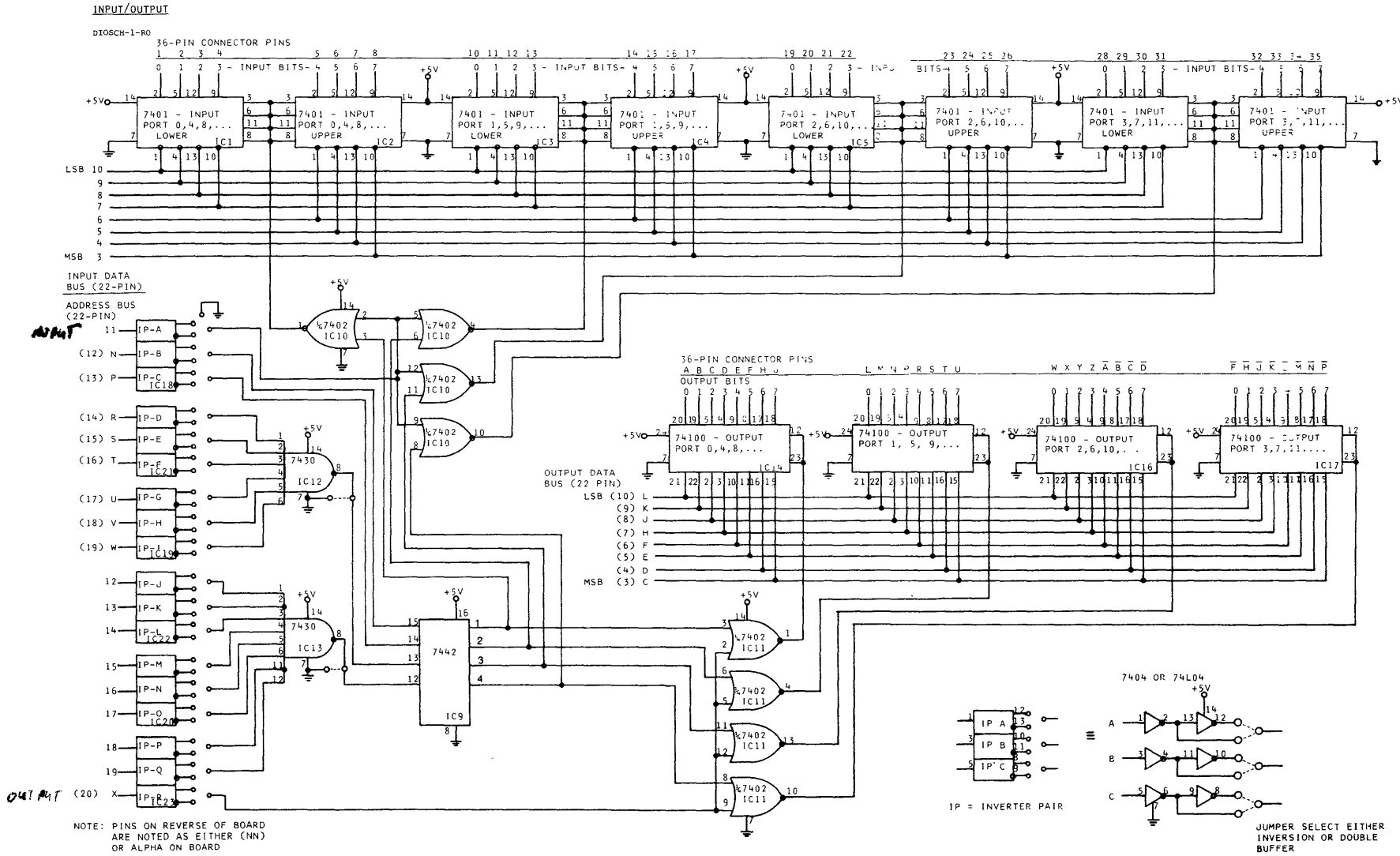

NOTE: PINS ON REVERSE OF BOARD ARE NOTED AS EITHER (NN) OR ALPHA ON BOARD