

EY-4818E-PP-0001

VAX 8600 TRAINING PRINT SET

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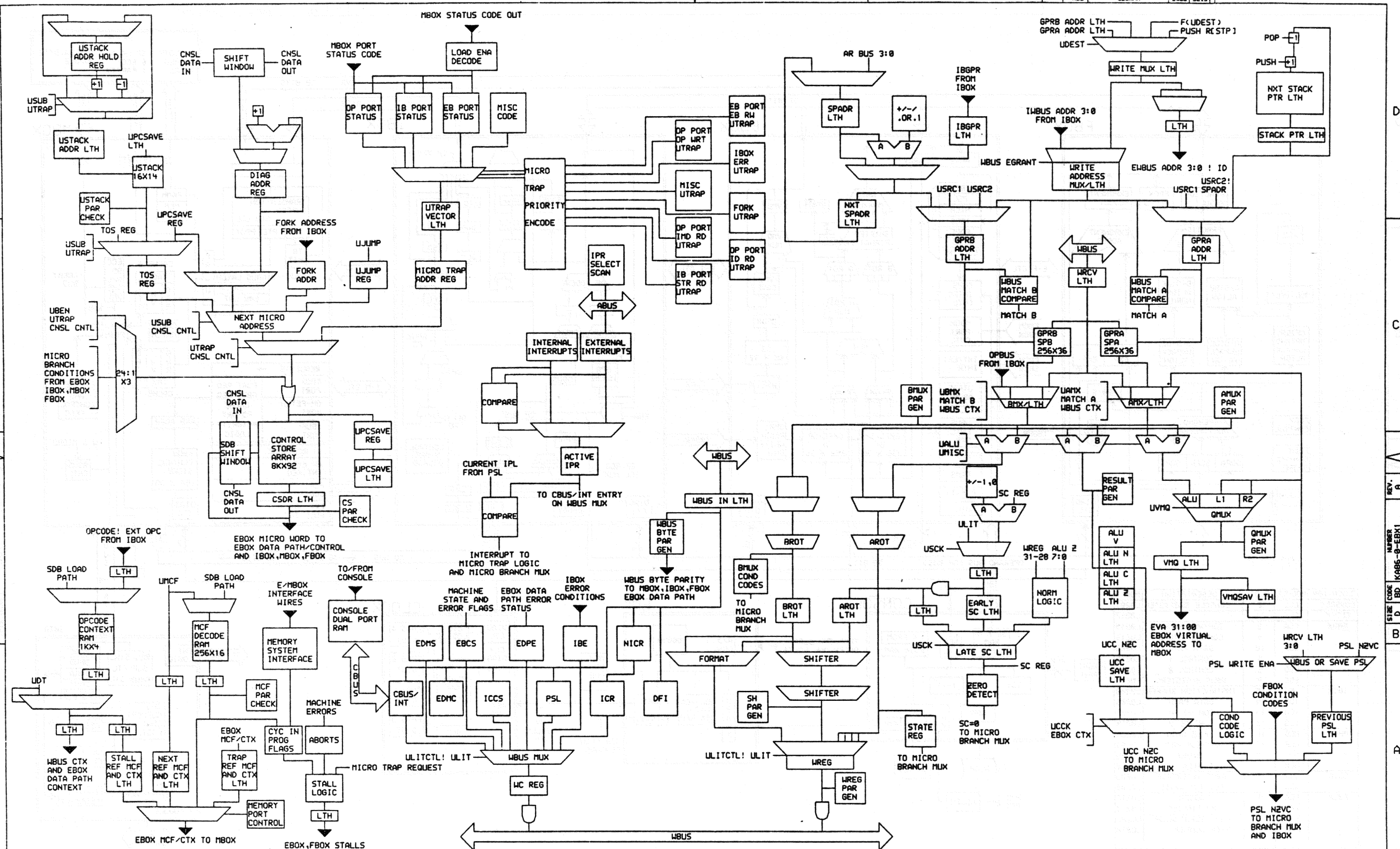
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Contents

	Page
Venus CPU Block Diagram	1
EBox Block Diagram	2
UWord	3
Venus IBox Data Paths	5
Venus IBox Control Paths	6
IBox Microword	7
IBox Dram Fields & Fork Address	9
Flush + LD CPC	10
VIBA Sel Adder INV IBuf	11
Flush + LD CPC Delayed MBox ACK	12
Venus System Pipeline Flow	13
SBIA Block Diagram	14
SBIA Registers Part 1	15
SBIA Registers Part 2	16
SBIA Registers Part 3	17
S-Data Path Output MUXing	18
CPU-SBI State Machine Flow	19
SBI State Machine Read/Write	20
SBI State Machine ISR/Quadclear	21
SBI Protocol Decision Flow	22
Console (CSL) Module	23
T-11 Micro Mem and Suprt Logic	24
QBus Adapter (QBA)	25
QBus Control	26
Serial Data Interface	27
CBus Interface	28
SDB Interface	29
Miscellaneous Cntrl/Status Logic	30
QBus & CBus Signals	31
Console BP Connectors	32
TOY Clock Controller	33
Clock Module Blk Diagram	34
Clock I/O Pin Connections	35
Clock Phases	36
Clock Relative Times	37
Microsequencer Block Diagram	38
Block Diagram EBC (L0210)	40
EBox Stall and Abort Logic	42
EBox Trap Logic	43
EBD Registers	44
Block Diagram EBE (L0219)	45
EBox Data Path Block Diagram	46
FBox Data Block Diagram	47
FBox Control Block Diagram	48
FBox Timing Diagram	49
FBox Data Block Diagram	50
FBox Control Block Diagram	51
FBox Timing Diagram	52
IBD Module Block Diagram	53

Contents

	Page
ICA Module Block Diagram	60
ICB Module Block Diagram	64
IDP Module Block Diagram	67
Address Module Block Diag	70
4 MByte Read Cycle	71
4 MByte 2WD WRT/4 WRT	72



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--	--	--	--	----------------	--	---	--	----------------------------------	--	--	------

HEX DIGIT
DEF. MIC/ULD NUMBER
PHYSICAL RAM BIT NUMBER

64	66	67	65	44	20	27	6	24	23	5	20	19	4	16	15	3	12	11	2	08	07	1	04	03	0	00
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
S	V	V	M	M	A	A	A	A	A	A	A	B	B	B	B	S	S	J	J	J	J	J	J	J	J	J
M	M	M	M	M	L	L	L	L	L	L	L	N	N	N	N	B	B	U	U	U	U	U	U	U	U	U
I	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	K	K	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	4	3	2	1	0	4	3	2	1	0	1	0	1	1	1	0	9	8	7	6	5	4
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U
SHI	LVMK	U	U	UALU 4:0				LIBEN 4:0				LJUSUB 11:0				LJUMP 12:0										

Key aline

USMI

00
0 START OF NEW MACRO INSTRUCTION
1 NOT START OF NEW MACRO INSTRUCTION

LVMK

01 00
0 0 HOLD
0 1 LOAD ALU RESULT
1 0 SHIFT LEFT 1, SHIFT IN ALU.C.31
1 1 SHIFT RIGHT 2, SHIFT IN ALU1:0

LIBMX

00
0 RAM B SELECT
1 OPBUS SELECT

LJAMX

00
0 RAM A SELECT
1 VMO SELECT

UALU

04	03	02	01	00	OPERATION	CARRY/BORROW
LOGICAL						
0	0	0	0	0	A.AND.B	X
0	0	0	0	1	A.XOR.B	X
0	0	0	1	0	B	X
0	0	0	1	1	A.OR.B	X
0	0	1	0	0	A.AND.(NOT.B)	X
0	0	1	0	1	A	X
0	0	1	1	1	(NOT.A).AND.B	X
ARITHMETIC						
0	0	1	1	0	DIVIDE A+/-B	UCC.C=0/1
0	1	0	0	0	A++	+0
0	1	0	0	1	A--	-0
0	1	0	1	0	A+B KORREKT (BCD)	
0	1	0	1	1	LOAD_CONFIG	
0	1	1	0	0	A-B	-1
0	1	1	0	1	A-B	-0
0	1	1	1	0	A-B	- NOT UCC.C
0	1	1	1	1	A-B	-PSL.C
1	0	0	0	0	A+B	+0
1	0	0	0	1	A+B	+1
1	0	0	1	0	A+B	+UCC.C
1	0	0	1	1	A+B	+PSL.C
1	0	1	0	0	B-A	-1
1	0	1	0	1	B-A	-0
1	0	1	1	0	B-A	- NOT UCC.C
1	0	1	1	1	B-A	-PSL.C
1	1	0	0	0	A+B (BCD)	+0
1	1	0	0	1	A+B (BCD)	+1
1	1	0	1	0	A+B (BCD)	+UCC.C
1	1	0	1	1	A+B (BCD)	+PSL.C
1	1	1	0	0	A-B (BCD)	-1
1	1	1	0	1	A-B (BCD)	-0
1	1	1	1	0	A-B (BCD)	- NOT UCC.C
1	1	1	1	1	A-B (BCD)	-PSL.C

DIAG. MODE ONLY
ONLY IF "EDPE" AND STATE = 2

LIBEN

04	03	02	01	00	LPC <2>	LPC <1>	LPC <0>
0	0	0	0	0	0	0	0
0	0	0	0	1	UCC.N	UCC.2	UCC.C
0	0	0	1	0	0	UCC.2	0
0	0	0	1	0	DIAG1	UCC.2	DIAG0
0	0	0	1	0	A.RAM.PE	0	B.RAM.PE
0	0	0	1	1	SC.EQ.0	0	UCC.C
0	0	1	0	0	PSL.N	PSL.2	PSL.C
0	0	1	0	1	ESA.VALID	ISA.VALID	UNWIND.DONE
0	0	1	1	0	OPCODE2	OPCODE1	OPCODE0
0	0	1	1	1	OPCODE4	0	EXT.OPCODE
0	1	0	0	0	STATE2	UCC.N	DECIMAL.STGN
0	1	0	0	1	IBUF.VA	NEXT.EB.VALID	TRAP.OP.WCHK
0	1	0	1	0	SC.EQ.0	VMO1	VMO0
0	1	0	1	1	PSL.IS	PSL.FPD	KERNEL
0	1	1	0	0	CPC.VALID	PSL.CH	INTERRUPT
0	1	1	0	1	STATE2	STATE1	STATE0
0	1	1	1	0	STATE5	STATE4	STATE3
0	1	1	1	1	STATE7	STATE6	UREG31
1	0	0	0	0	TRAP.EB.WCHK	YB.CHECK1	YB.CHECK0
1	0	0	0	1	0	VMO31	PSL.V
1	0	0	1	0	SC.EQ.0	UCC.2	30.LE.BFX.LE.39
1	0	0	1	1	BMX15	UCC.2	FL.EXP=0
1	0	1	0	0	FBOX2	FBOX CARRY	FBOX ENABLED
1	0	1	0	1	TRAP.EB.WRITE	NEXT.EB.WRITE	TRAP.EB.WORD.OR.BYTE
1	0	1	1	0	TRAP.OP.WRITE	0	NEXT.OP.WR
1	0	1	1	1	0	0	0
1	1	0	0	0	0	0	0
1	1	0	0	1	0	0	0
1	1	0	1	0	0	0	0
1	1	0	1	1	0	0	0
1	1	1	0	0	0	0	0
1	1	1	0	1	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	1	0	0	0

== GENERATES THE SIGNAL IRD

LJUSUB

01 00
0 0 JUMP
0 1 RETURN
1 0 FORK
1 1 CALL SUB.

LJUMP

12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	X	X	X	X	X

THIS FIELD SPECIFIES THE NEXT MICRO ADDRESS FOR E-BOX MICRO SEQUENCER

NOTES

RAM A	EBOX GPR A OR SCRATCH PAD A
RAM B	EBOX GPR B OR SCRATCH PAD B
AR BUS	A OPERAND OR ALU RESULT BUS
ECC0	FOR FUTURE USE

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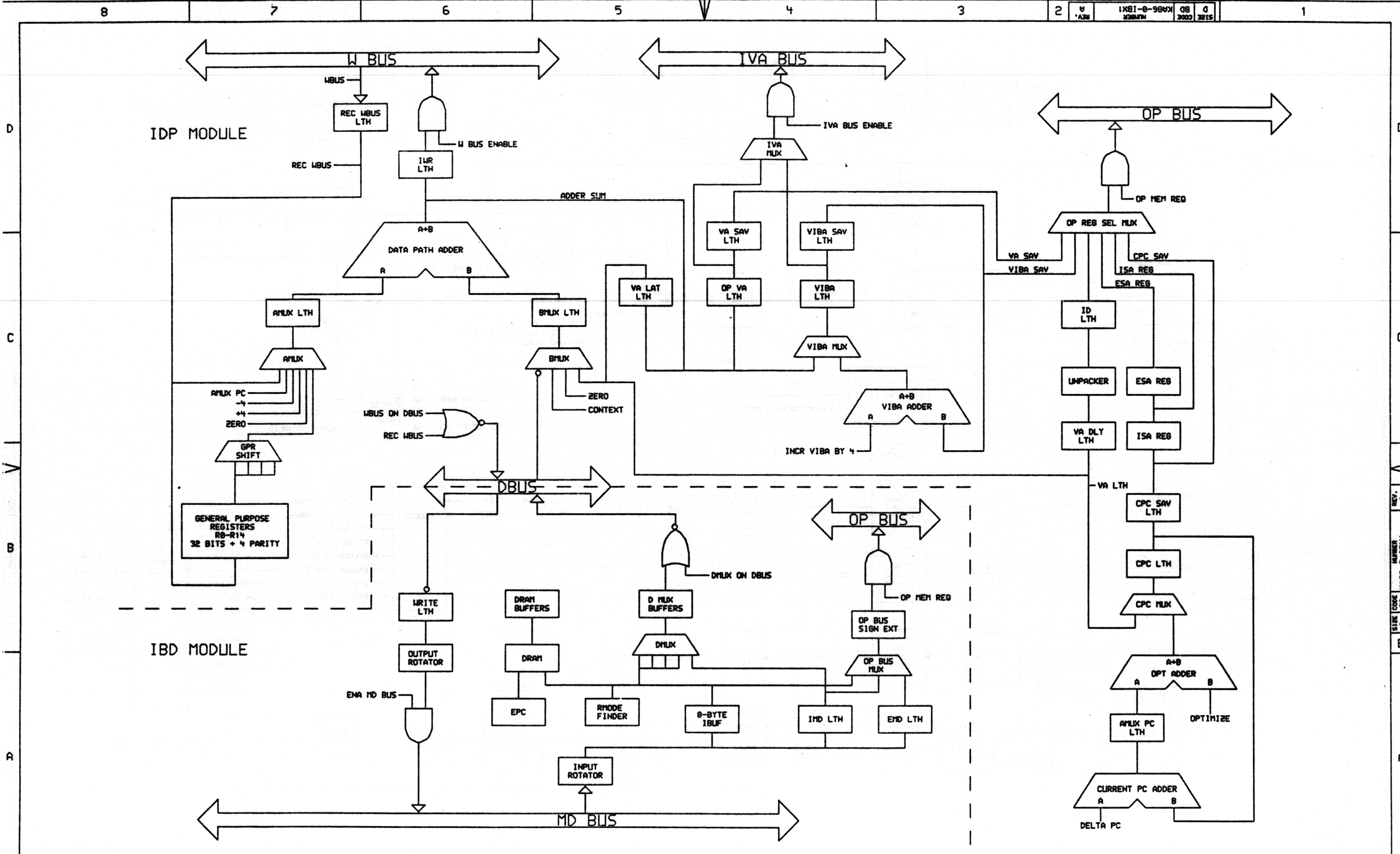
REVISIONS

CHK	CHANGE NO.	REV
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DRN. A. OPPENHEIM DATE 12-SEP-84 ENG. B. HILLIARD DATE 12-SEP-84
CHK'D L. NETZGER DATE 12-SEP-84 BOARD LOCATION: OF 1
VEN011: EBOX_SPECS_MACRO2.DWG 113-SEP-84 07:14 NEXT HIGHER ASSEMBLY: D-DD-KA86-0

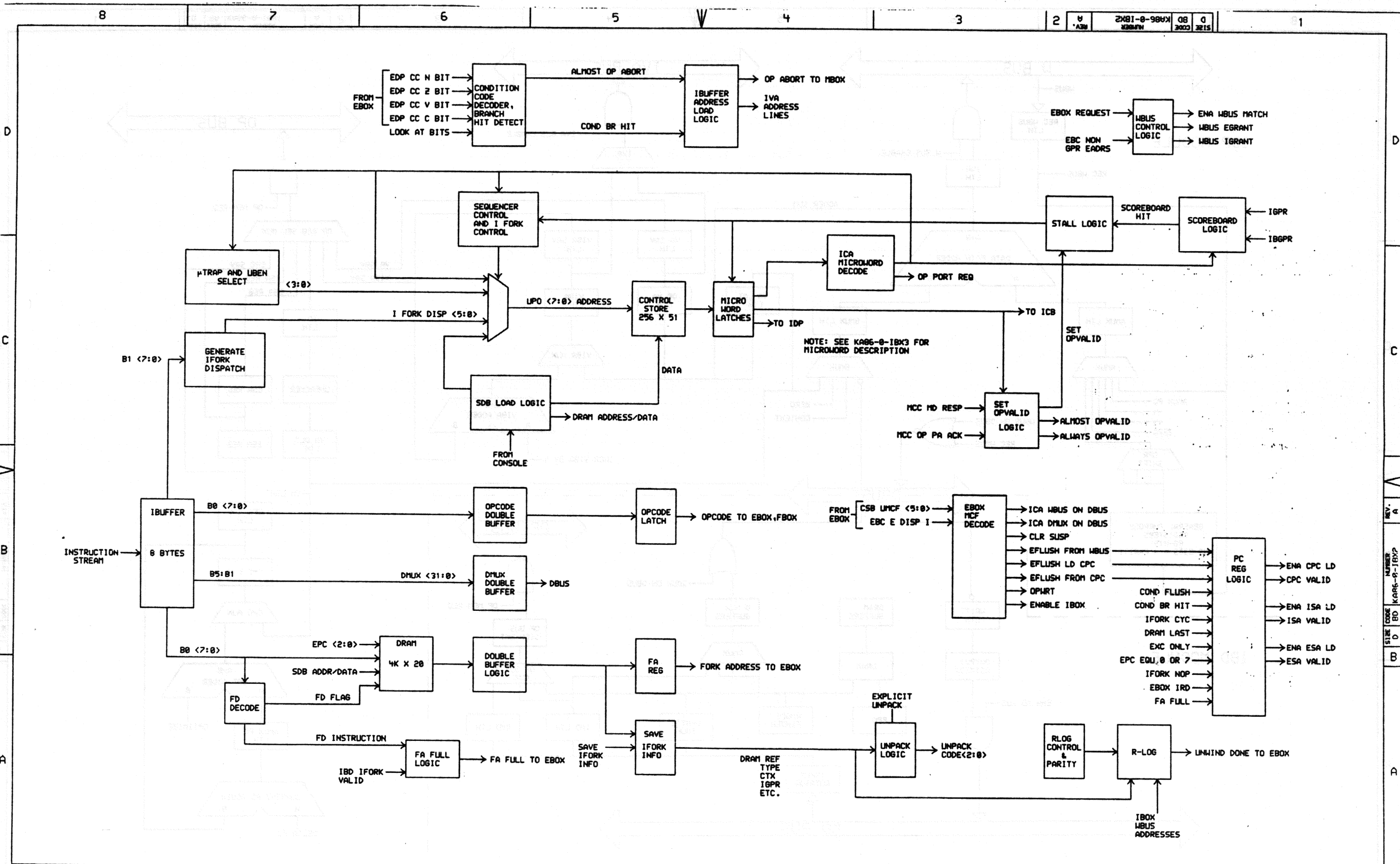
TITLE: UWORD PAGE 2
SIZE CODE D CS NUMBER KA86-0-EBX3 REV. A



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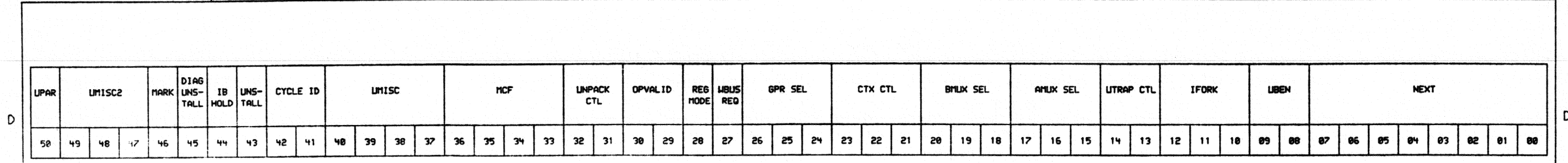
DRN. R. DAME	DATE 19-SEP-84	ENG. F. MCKEEN	DATE 19-SEP-84	TITLE: VENUS IBOX DATA PATHS
CHK'D L. METZGER	DATE 19-SEP-84	BOARD LOCATION: 1	SHEET 1	SIZE CODE NUMBER REV. D BD KA86-0-IBX1 A
VENUS IBOX (RD-50) IBD (RD-50) 18-SEP-84 13:23		NEXT HIGHER ASSEMBLY: D-DD-KA86-0		
FIRST USED ON OPTION/MODEL:				



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REVISIONS	
CHK	CHANGE NO. REV

	DRN C. CAIAZZI	DATE 07-OCT-84	ENG F. MCKEEN	DATE 07-OCT-84	TITLE: VENUS IBOX CONTROL PATHS
	CHK'D L. NETZGER	DATE 07-OCT-84	BOARD LOCATION: SHEET 1	OF 1	SIZE CODE NUMBER REV. D BD KA86-0-IBX2 A
VENUS IBOX BOARD SUB-ASSEMBLY 102-OCT-84 11:55 NEXT HIGHER ASSEMBLY: D-DD-KA86-0					2195



UPAR<0:0> ODD PARITY GENERATED ON MICROWORD
 UMISC2<2:0> MISCELLANEOUS 2
 0 = NOP
 1 = INDEX.IMM
 2 = ENA.OPBUS.PARITY
 3 = UNUSED
 4 = FORCE.SET.SB.VALID
 5 = INHIBIT.SET.SB.VALID
 6 = FORCE.SET.SB.ENA.OPBUS.PARITY
 7 = UTRAP.CIP

MARK<0:0> STOP CPU CLOCKS IN NEXT MICROCYCLE
 DIAG UNS-TALL<0:0> OVERRIDE ALL IBOX STALL TERMS
 IB HOLD<0:0> FREEZE IBUFFER FOR DIAGNOSTICS
 UNS-TALL<0:0> OVERRIDE IB.STOP AND SUSPEND STALL
 CYCLE ID<1:0>
 0 = NON-IFORK CYCLE
 1 = INDEX IFORK ENTRY [R]
 2 = BASE OPERAND ADDRESS (BOA) ENTRY
 3 = IFORK ENTRY AND -(BOA + [R])

UMISC<3:0> MISCELLANEOUS
 0 = NOP
 1 = STALL UNTIL EBOX.OP.WRITE COMMAND
 2 = IB.FLUSH.LD.CPC
 3 = IB.FLUSH
 4 = COND.BRANCH
 5 = IB.FLUSH.COND
 6 = READ.IMD
 7 = INH.SB.CHECK
 8 = RAF RESERVED ADDRESSING MODE
 9 = DIAG.DONE
 A = DIAG.RESET
 B = BMUX.CHK.CTX
 C = POP STACK
 D = CLEAR CPC VALID ; FOR FLUSH AND BRANCH
 E = COND.FA.OP.MEM.REQ
 F = FA.OP.MEM.REQ

MCF<3:0> MEMORY CONTROL FIELD
 0 = READ.RCHK IF DRAM MEM EQUALS READ
 READ.WCHK IF DRAM MEM EQUALS MODIFY
 1 = NO OP-PORT MEMORY REQUEST
 2 = WRITE+V+NOPAGE
 3 = WRITE+V+NOPAGE.2ND
 4 =
 5 = WRITE+V+WCHK
 6 =
 7 =
 8 = READ+V+WCHK
 9 =
 A = READ+V+RCHK
 B = READ+V+RCHK.2ND
 C = READ+V+NOPAGE
 D = READ+V+NOPAGE.2ND
 E = IB.FILL.OP
 F = IB.FILL.IBF

UNPACK CTL<1:0> UNPACKER CONTROL
 0 = NOP
 1 = SIGN EXTEND IF -ASRC
 2 = UNPACK AS SHORT LITERAL ACCORDING TO
 DRAM CTX AND TYPE FIELDS.
 3 = UNUSED
 OPVALID<1:0> OPERAND VALID
 0 = NOP
 1 = SET OPVALID IF ((READ+MODIFY+VSRC)≠RMODE) -(ASRC+RMODE)
 2 = SET OPVALID IF ASRC+((READ+MODIFY)≠ALIGNED)
 3 = SET OPVALID UNCONDITIONALLY

REG MODE<0:0> REGISTER MODE
 0 = INDICATES THAT THIS IS NOT RN SPECIFIER
 1 = INDICATES RN SPECIFIER
 MBUSREQ<0:0> MBUS REQUEST
 0 = RLOG ENTRY IS PUSHED IF THIS IS FIRST IFORK
 FOR THIS OPCODE. MBUS IS CONDITIONALLY
 REQUESTED IF DOING AN UNWIND.GPR SEL=3
 1 = RLOG ENTRY IS PUSHED WITH VALID GPR NUMBER
 AND CONTEXT ENTRY. MBUS IS REQUESTED.

GPR SEL<2:0> GENERAL PURPOSE REGISTER SELECT
 0 = GPR ADDRESS FROM IBUF ISTREAM (B1)
 1 = INDEX REGISTER IS BEING ADDRESSED BY A
 SAVED INDEX REGISTER NUMBER.
 2 = LAST GPR ADDRESS PLUS 1.
 3 = GPR ADDRESS IS PREVIOUS GPR ADDRESS.
 4 = RLOG+UNWIND
 5 = GPR ADDRESS <3:2> <--- CTX CTL<1:0>
 GPR ADDRESS <1:0> <--- UNPACK.CTL<1:0>
 6-7 = UNUSED

CTX CTL<2:0> CONTEXT CONTROL

	ADDER CTX	MEM CTX	RLOG CTX ENTRY
0	DRAM CTX	DRAM CTX	DRAM CTX
1	4	4	4
2			
3	+/-RLOG CTX	X	X
4	-DRAM CTX	DRAM CTX	-DRAM CTX
5	-4	4	X
6			
7			

BMUX SEL<2:0> BMUX SELECTION
 0 = ZERO
 1 = VA
 2 = ADDER CTX AS DEFINED BY CTX CTL
 3 = UNUSED
 4 = DMX.IBF
 5 = DMX.IMD
 6 = CPC ; USED FOR STRING CONTINUED FLUSHES.
 7 = HOLD VA ; INHIBIT VA CLOCKING.
 NOT A BMUX SEL FUNCTION.

AMUX SEL<2:0> AMUX SELECTION
 0 = ZERO
 1 = AMUX PC
 2 = +4
 3 = -4
 4 = GPR, IF MBUS MATCH REPLACE
 GPR DATA WITH MBUS DATA.
 5 = GPR (LEFT SHIFT 1)
 6 = GPR (LEFT SHIFT 2)
 7 = MBUS
 4-6 = ENABLE ISTALL IF SCOREBOARD HIT.
 5-6 = ENABLE ISTALL IF MBUS MATCH.

UTRAP CTL<1:0> MICRO-TRAP CONTROL
 0 = INHIBIT MICRO-TRAP DUE TO UNALIGNMENT.
 1 = MICRO-TRAP NEXT CYCLE FOR UNALIGNED INDIRECT FETCH.
 2 = MICRO-TRAP FOR UNALIGNED (RN) OR ANY OTHER
 UNALIGNED OPERAND.

IFORK CTL<2:0> IFORK CONTROL
 0 = DO NOT IFORK
 1 = IFORK IF ASRC+(READ*(BUL))
 2 = IFORK IF VSRC+WRITE+((READ+MODIFY)*(BUL))
 3 = IFORK IF READ*(BUL)
 4 = IFORK IF QUAD
 5 = IFORK IF EBOX UMCF EQUALS 24
 6 = UNCONDITIONAL IFORK
 7 = UNUSED

LIBEN<1:0> MICRO-BRANCH ENABLE

	LIBEN MUX 3	LIBEN MUX 2	LIBEN MUX 1	LIBEN MUX 0
0	0	0	0	0
1	0	QUAD+OCTA	DRAM MEM 1	DRAM MEM 0
2	RLOG FIRST	DRAM CTX 2	DRAM CTX 1	DRAM CTX 0
3	0	0	0	0

NA<7:0> NEXT ADDRESS

2196

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REVISIONS		
CHK	CHANGE NO.	REV

digital DRN. L.MELLO DATE 19-SEP-84 ENG. E.HANSON DATE 19-SEP-84 TITLE: IBOX MICROWORD

CHK'D L.METZGER DATE BOARD LOCATION: SHEET 1 OF 1

VENI((TRON.RD-SUB))IBOX.DRW 118-SEP-84 10:27 NEXT HIGHER ASSEMBLY: D-DD-KA86-0

FIRST USED ON OPTION/MODEL: D DD KA86-0-IBX3

SIZE CODE NUMBER REV. D BD KA86-0-IBX3 A

CTX			TYPE		REF		CTL		SUSP	BDEST	LAST	PAR	FPA	ADRS					
19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

CTX<2:0>
 0 = BYTE
 1 = WORD (2 BYTES)
 2 = LONG (4 BYTES)
 3 = QUAD (8 BYTES)
 4 = OCTA (16 BYTES)
 5:7 = UNPREDICTABLE

TYPE<1:0>
 0 = INTEGER, ASOURCE
 1 = FLOATING, F, D, OR H
 2 = S-FLOAT
 3 = VSOURCE

REF<1:0>	ACCESS CHECK	
	ON READ	WRITE
0 = ASOURCE	--	--
0 = VSOURCE	--	--
1 = READ	READ	--
2 = WRITE	--	WRITE
3 = MODIFY	WRITE	WRITE

CTL<1:0>
 0 = EXECUTE
 1 = SINGLE
 2 = OPT-TWO
 3 = OPT-TWO & EXECUTE

SUSP<0:0>
 0 =
 1 = SUSPEND ADDRESS CALCULATION

BDEST<0:0>
 0 = NEXT BYTE AFTER THIS SPECIFIER IS A MODE-REGISTER SPECIFIER OR NEW OPCODE.
 1 = NEXT BYTE AFTER THIS SPECIFIER IS A BRANCH DISPLACEMENT.

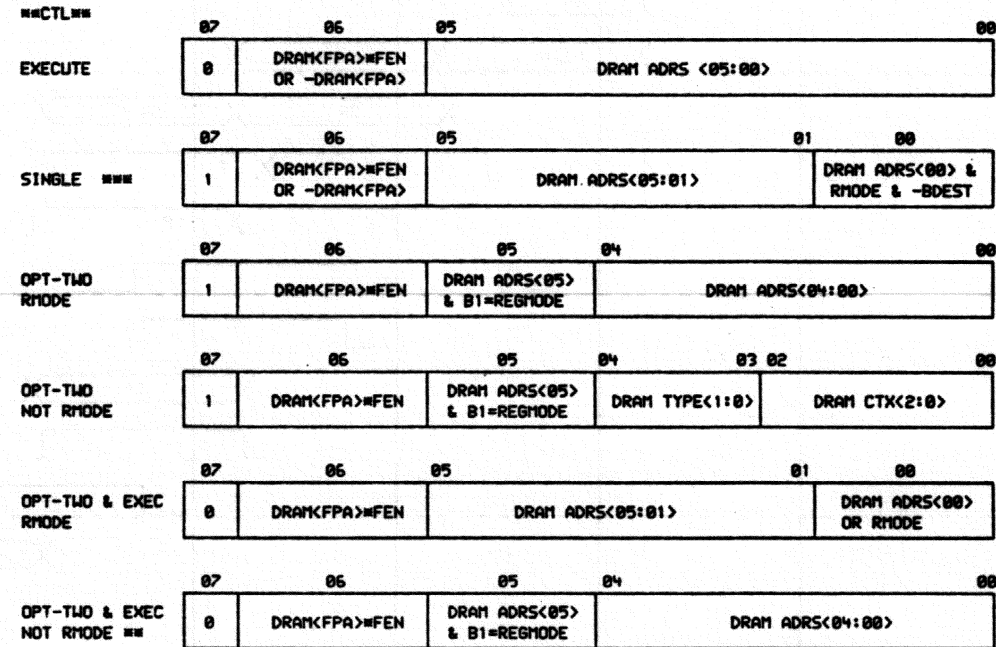
LAST<0:0>
 0 =
 1 = LAST ENTRY FOR THIS INSTRUCTION

PAR<0:0>
 X = ODD PARITY BIT

FPA<0:0>
 0 =
 1 = FPA MAY OVERRIDE THE EBOX FOR THE SPECIFIER

ADRS<5:0>
 X = BASIC FORK ADDRESS

FORK ADDRESSES BASED ON CTL FIELD



== IF FORK ADDRESS BIT 5 (FA<05>) = 1
 TURN OFF THE SCOREBOARD.
 === IF FORK ADDRESS BIT 0 (FA<00>) = 1
 TURN OFF THE SCOREBOARD.

TABLE 10
 USE OF THE DRAM

EPC	NON FD INSTRUCTIONS	FD INSTRUCTIONS
0	1ST OPERAND	FPD DISPATCH
1	2ND OPERAND	1ST OPERAND
2	ETC..	2ND OPERAND
3	.	ETC..
4	.	.
5	.	.
6	.	.
7	FPD DISPATCH	NOT USED

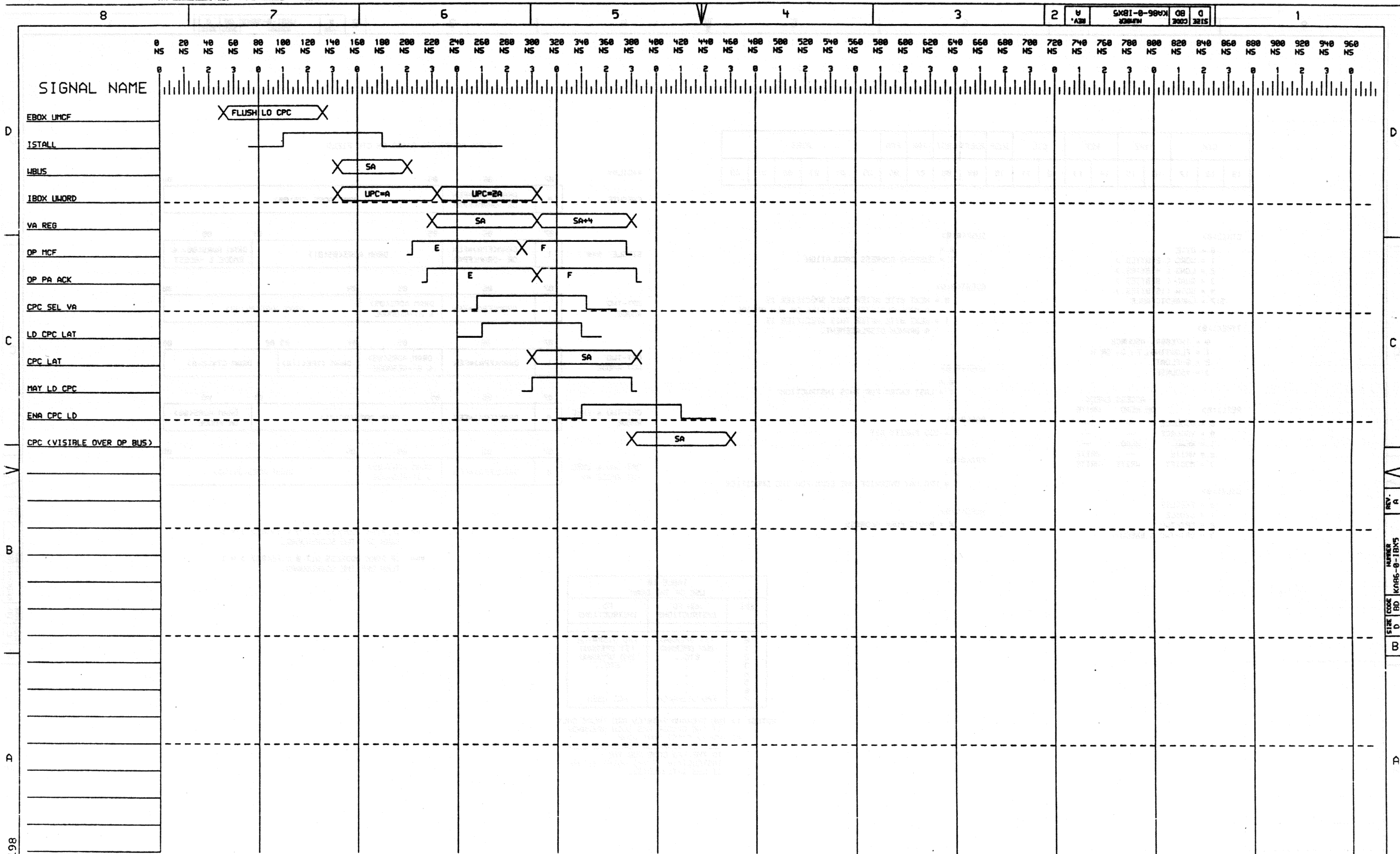
NOTES: 1) THE OPERAND ENTRIES ARE THERE ONLY IF THE OPCODE HAS SUCH OPERANDS.
 2) FPD => FIRST PART DONE.
 THE FPD DISPATCH FORKS THE EBOX TO THE FPD CODE FOR THE INSTRUCTION IT WAS DOING BEFORE IT WAS INTERRUPTED.

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digital	DRN. L.HELLO	DATE 19-SEP-84	ENG. C.MAIMAN	DATE 19-SEP-84
	CHK'D. L.METZGER	DATE 19-SEP-84	BOARD LOCATION: SHEET 1	OF 1
VENID: (100K.BD-SUD) (REV.D) 118-SEP-84		10: 70 NEXT HIGHER ASSEMBLY:		SIZE CODE D BD
FIRST USED ON OPTION/MODEL: D-DD-KA86-0		NUMBER KA86-0-IBX4		REV. A

TITLE: IBOX DRAM FIELDS & FORK ADDRESS

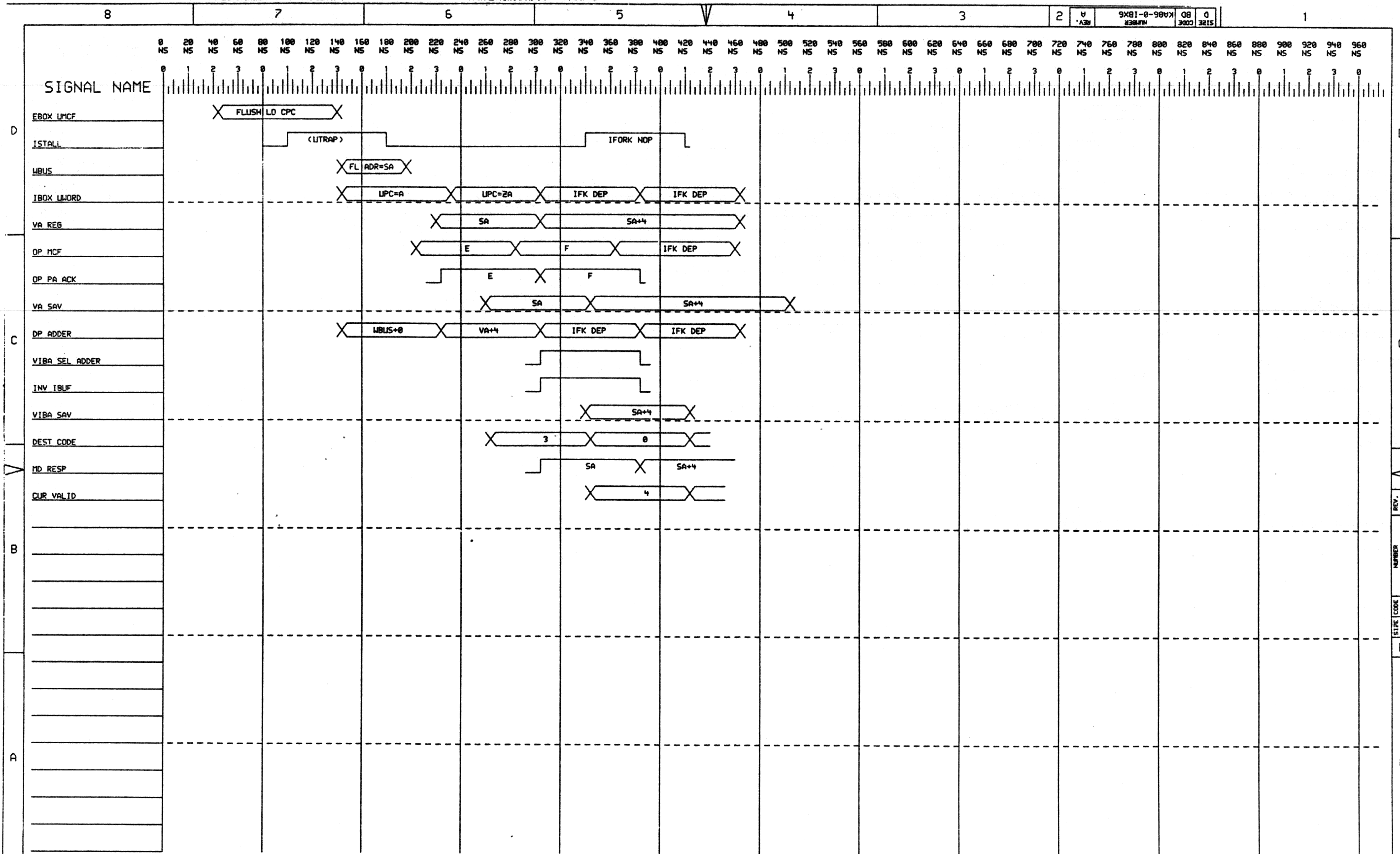


2198

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REVISIONS		
CHK	CHANGE NO.	REV

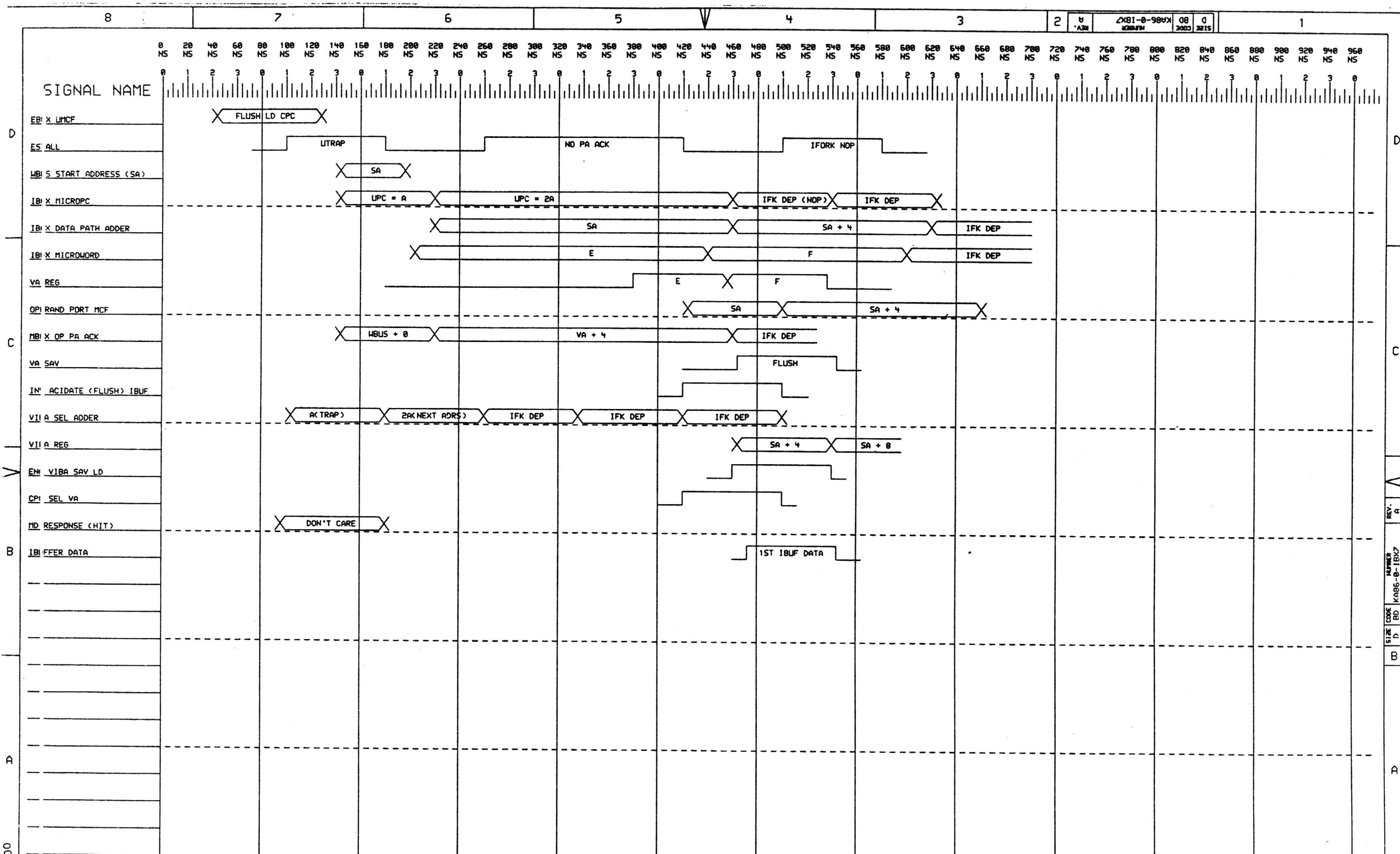
digital	DRN. B. CHARBONNEAU	DATE 19-SEP-84	ENG. F. MCKEEN	DATE 19-SEP-84	TITLE: FLUSH + LD CPC
	CHK'D. L. NETZGER	DATE 19-SEP-84	BOARD LOCATION:	SHEET	OF
FIRST USED ON OPTION/MODEL: 10-DD-KA86-0					SIZE CODE D BD
NUMBER KA86-0-IBX5					REV. A



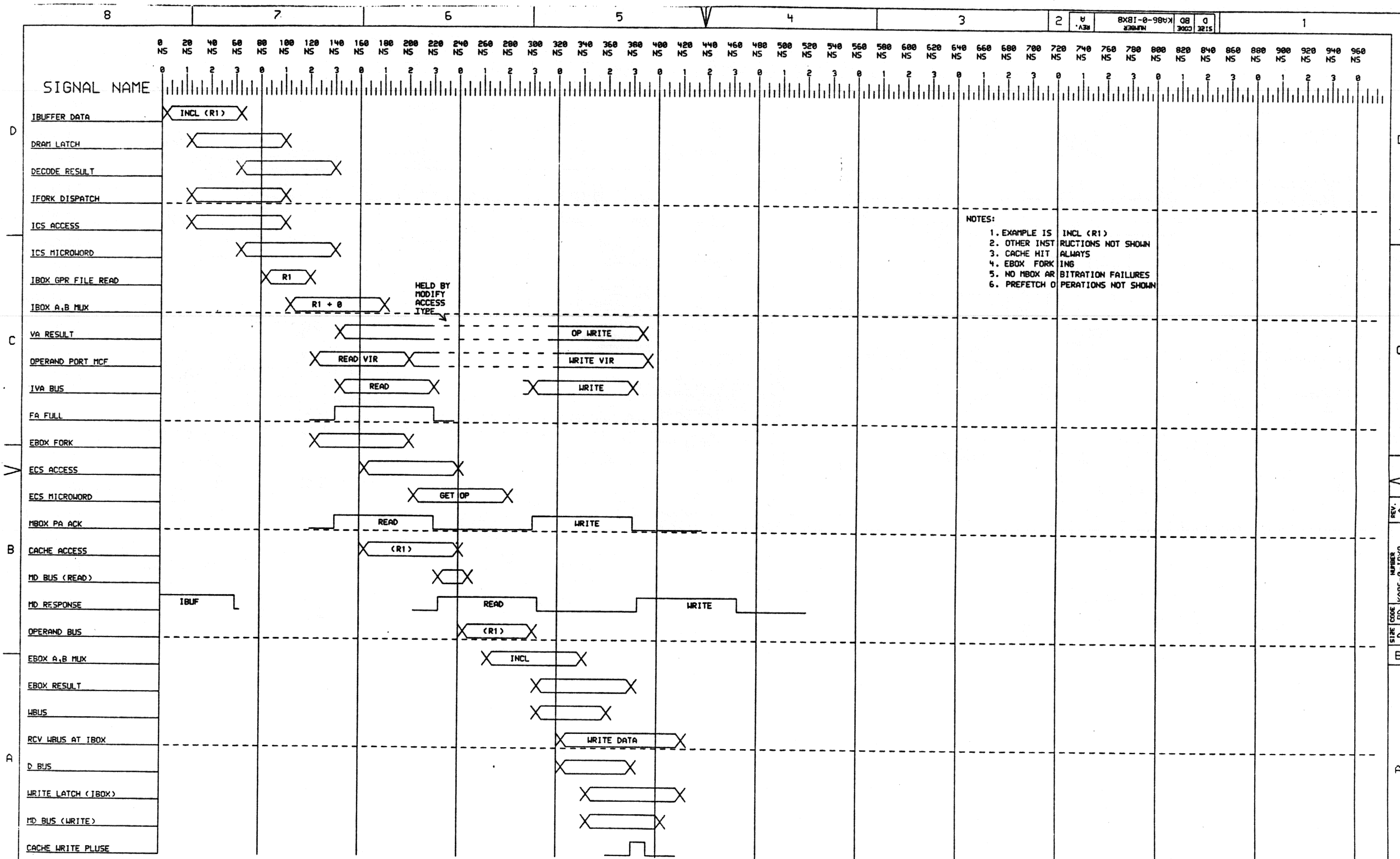
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REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN: B.CHARBONNEAU	DATE: 19-SEP-84	ENG: F.MCKEEN	DATE: 19-SEP-84	TITLE: VIBA SEL ADDER
	CHK'D: L.METZGER	DATE: 19-SEP-84	BOARD LOCATION: SHEET 1 OF 1		INV IBUF
NEXT HIGHER ASSEMBLY: D-DD-KA86-0					SIZE: D
IF FIRST USED ON OPTION/MODEL:					CODE: BD
					NUMBER: KA86-0-IBX6
					REV: A



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				NEXT HIGHER ASSEMBLY: D-DD-KAB6-0	SIZE CODE: D BD NUMBER: KAB6-0-IBX7
				REV. A	

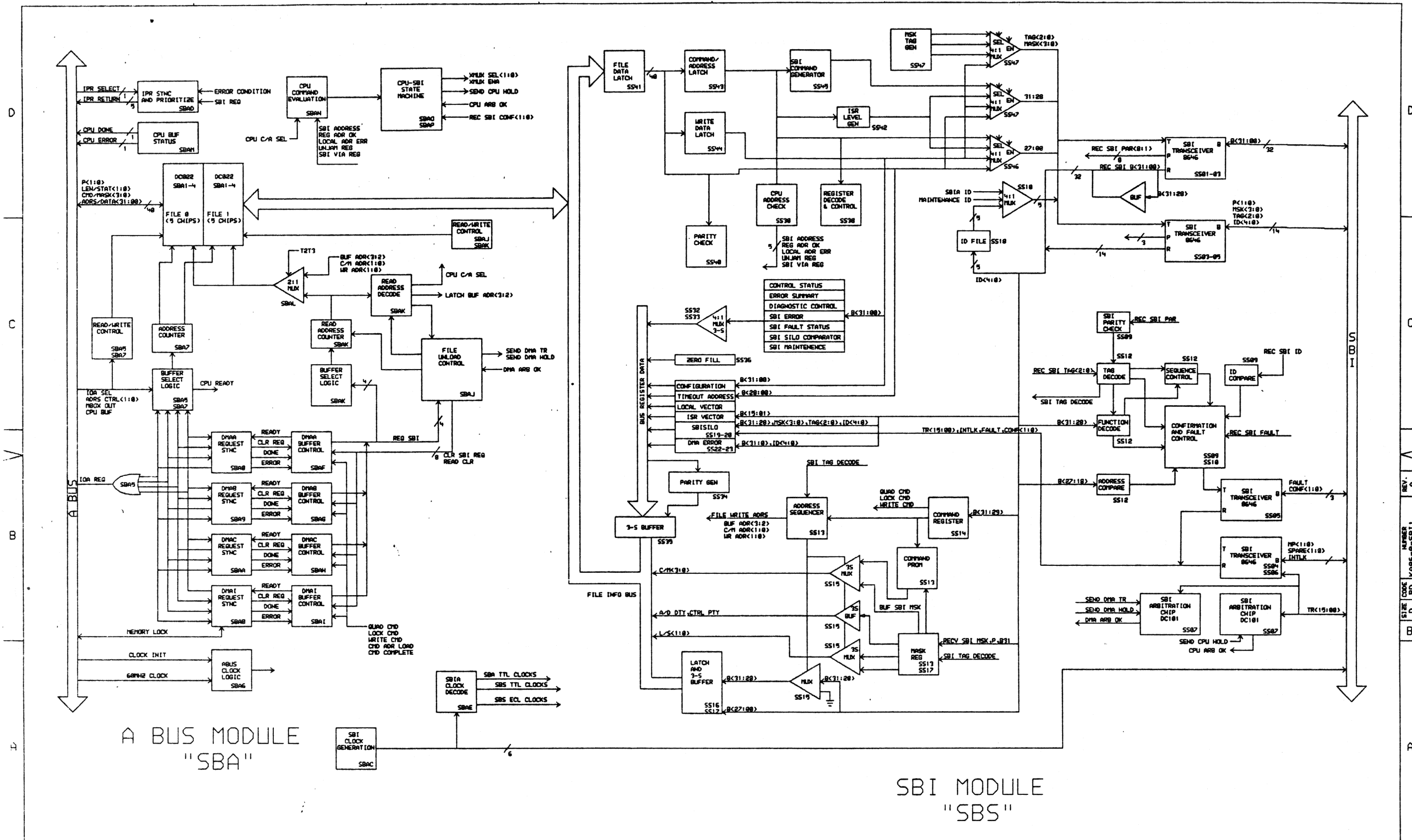


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REVISIONS		
CHK	CHANGE NO.	REV

	DRN: C. CAIAZZI	DATE: 19-SEP-84	ENG: F. MCKEEN	DATE: 19-SEP-84	TITLE: VENUS SYSTEM PIPELINE FLOW
	CHK'D: L. METZGER	DATE: 19-SEP-84	BOARD LOCATION: 1	OF: 1	
VENUS SYSTEM DD-SUB: IBOX.DRAW 19-SEP-84 12:35					NEXT HIGHER ASSEMBLY: D-DD-KA86-0
FIRST USED ON OPTION/MODEL:					SIZE: D
					CODE: BD
					NUMBER: KA86-0-1BX8
					REV: A

2201

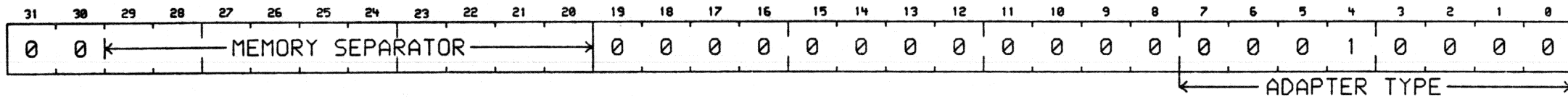


A BUS MODULE "SBA"

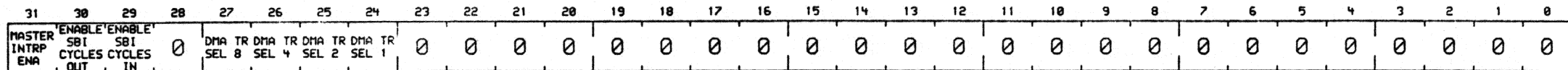
SBI MODULE "SBS"

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VENMG2:(MARTIN)SBI180.DRW 18-SEP-84 14:15 NEXT HIGHER ASSEMBLY: D-DD-KAB6-0	DATE: 18-SEP-84 DATE: 18-SEP-84 DATE: 18-SEP-84	ENG: J.MARTIN BOARD LOCATION:	SIZE: D BD CODE: KAB6-0-SB11 NUMBER: REV. A

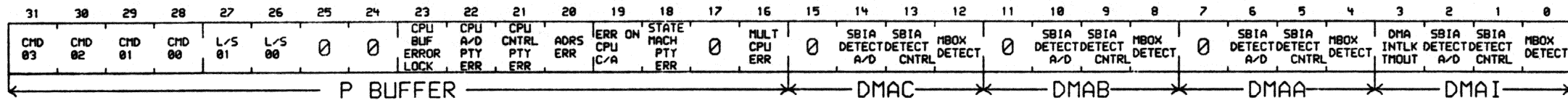
CONFIGURATION
2X08 0000



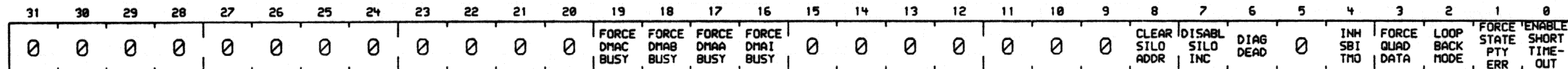
CTRL/STATUS
2X08 0004



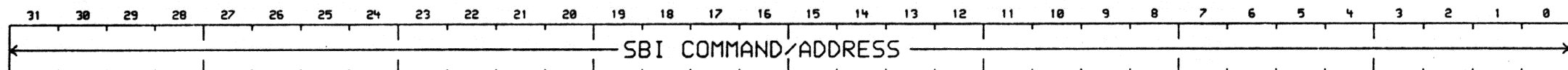
ERROR SUMMARY
2X08 0008



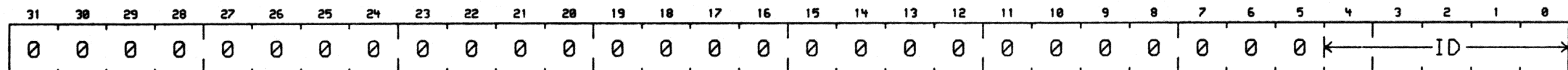
DIAGNOSTIC CONTROL
2X08 000C



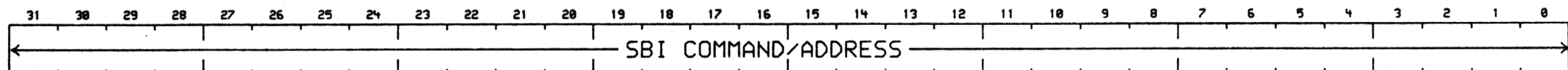
DMAI CMD/ADRS
2X08 0010



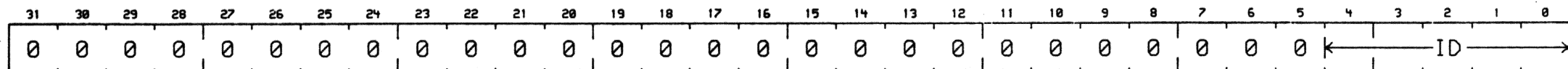
DMAI ID
2X08 0014



DMAA CMD/ADRS
2X08 0018



DMAA ID
2X08 001C



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REVISIONS

CHK CHANGE NO. REV

8

7

6

5

4

3

2

1

digital	DRN. J. J. J.	DATE 18-SEP-84	ENG. J. MARTIN	DATE 18-SEP-84	TITLE: SBIA REGISTERS PART 1
	CHK'D L. HETZGER	DATE 18-SEP-84	BOARD LOCATION: SHEET 1 OF 1	SIZE CODE D BD	NUMBER KAB6-0-SBI2
VENN82: (MARTIN) SBI2BD.DRW 112-SEP-84 14:54 NEXT HIGHER ASSEMBLY: D-DD-KAB6-0					REV. A

SBI SILO
COMPARATOR
2X08 0040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
COMP SILO LOCK	SILO LCK ENA	LOCK INT UNCND	COND LOCK CODE 01	COND LOCK CODE 00	COMP CMDMSK 03	COMP CMDMSK 02	COMP CMDMSK 01	COMP CMDMSK 00	COMP TAG 02	COMP TAG 01	COMP TAG 00	COUNT FIELD 03	COUNT FIELD 02	COUNT FIELD 01	COUNT FIELD 00	MAINT TR 15	MAINT TR 14	MAINT TR 13	MAINT TR 12	MAINT TR 11	MAINT TR 10	MAINT TR 09	MAINT TR 08	MAINT TR 07	MAINT TR 06	MAINT TR 05	MAINT TR 04	MAINT TR 03	MAINT TR 02	MAINT TR 01	MAINT TR 00																
																							FORCE SBI REQUEST = 1		MAINT REQ 07		MAINT REQ 06		MAINT REQ 05		MAINT REQ 04		MAINT ALERT														

SBI
MAINTENANCE
2X08 0044

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																					
FORCE P0 REV ON SBI	FORCE USQ FAULT	FORCE LINKD RD DAT FAULT	FORCE MULTI XMITTR FAULT	MAINT ID04	MAINT ID03	MAINT ID02	MAINT ID01	MAINT ID00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																					
																							FORCE P1 REV ON SBI		FORCE TIMOUT		0		0		0		0		0		0		0		0		0		0		0		0		0	

SBI
UNJAM
2X08 0048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SBI
QUADCLEAR
2X08 004C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00

VECTOR
2X08 0080
TO
2X08 00B8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	

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REVISIONS		
CHK	CHANGE NO.	REV

7	6	5	4	3	2	1
---	---	---	---	---	---	---

digital	DRN	DATE	ENG.	DATE	TITLE:	
	<i>J. Martin</i>	18-SEP-84	J. MARTIN	18-SEP-84	SBIA REGISTERS PART 3	
	CHK'D	DATE	BOARD LOCATION:			
	L. METZGER	18-SEP-84	SHEET 1 OF 1			
VENN62 (MARTIN) SBI480.DRW [17-SEP-84 14:56] NEXT HIGHER ASSEMBLY:			SIZE	CODE	NUMBER	REV.
FIRST USED ON OPTION/MODEL:			D-DD-KA86-0	D	BD KA86-0-SBI4	A

REV. A
NUMBER KA86-0-SBI4
SIZE CODE D BD
B
A

FUNCTION (INFORMATION TO BE TRANSMITTED ON THE SBI)	SPECIAL CASES	MASK, TAG MUX SEL A1 A0	B<31:29> MUX SEL A1 A0	B<27:00> MUX SEL A1 A0	TAG SOURCE	MASK SOURCE	B<31:28> SOURCE	B<27:00> SOURCE	PREDICT P1 SOURCE	PREDICT P0 SOURCE	COMMENTS
DMA READ DATA RETURN	NO ERROR PARITY ERROR OR L/S NOT 00	0 0 0 0	0 0 0 0	0 0 0 0	FORCED (000) FORCED (000)	FORCED (0000) FORCED (0010)	FILE DATA LATCH FILE DATA LATCH	FILE DATA LATCH FILE DATA LATCH	-LATCH A/D PAR LATCH A/D PAR	0<ERROR> 1<ERROR>	
CPU CMD/ADR READ		0 1	0 1	0 1	FORCED (011)	CPU ADRS LATCH L/S	SBI FUNCTION GEN	CPU ADRS LATCH	CPU ADRS PAR	FORCED (0)	
WRITE		0 1	0 1	0 1	FORCED (011)	WRITE DATA LATCH MASK	SBI FUNCTION GEN	CPU ADRS LATCH	CPU ADRS PAR	-DATA CNTRL PAR (WRITE DATA LATCH)	
QUADCLEAR		1 0	1 0	1 0	FORCED (011)	WRITE DATA LATCH MASK	WRITE DATA LATCH	WRITE DATA LATCH	-CPU DATA PAR (WRITE DATA LATCH)	-DATA CNTRL PAR (WRITE DATA LATCH)	
CPU WRITE DATA WRITE COMMAND	NORMAL FORCE WRITE SEQ FAULT	1 0 1 0	1 0 1 0	1 0 1 0	FORCED (101) FORCED (111)	FORCED (0000) FORCED (0000)	WRITE DATA LATCH WRITE DATA LATCH	WRITE DATA LATCH WRITE DATA LATCH	-CPU DATA PAR (WRITE DATA LATCH) -CPU DATA PAR (WRITE DATA LATCH)	FORCED (0) FORCED (1)	DIAGNOSTIC MODE
QUADCLEAR WD1	NORMAL FORCE WRITE SEQ FAULT	1 0 1 0	1 0 1 0	1 0 1 0	FORCED (101) FORCED (111)	WRITE DATA LATCH MASK WRITE DATA LATCH MASK	DISABLED (0) DISABLED (0)	DISABLED (0) DISABLED (0)	DISABLED (0) DISABLED (0)	-DATA CNTRL PAR (WRITE DATA LATCH) -DATA CNTRL PAR (WRITE DATA LATCH)	DIAGNOSTIC MODE
QUADCLEAR WD2	NORMAL FORCE WRITE SEQ FAULT FORCE QUAD DATA	1 0 1 0 1 0	1 0 1 0 1 0	1 0 1 0 1 0	FORCED (101) FORCED (111) FORCED (101)	FORCED (0000) FORCED (0000) WRITE DATA LATCH	DISABLED (0) DISABLED (0) WRITE DATA LATCH	DISABLED (0) DISABLED (0) WRITE DATA LATCH	DISABLED (0) DISABLED (0) -CPU DATA PAR (WRITE DATA LATCH)	FORCED (0) FORCED (1) FORCED (0)	DIAGNOSTIC MODE DIAGNOSTIC MODE
INTERRUPT SUMMARY READ		1 1	1 1	1 1	FORCED (110)	FORCED (0000)	FORCED (0000)	(27:00) FORCED (0) (07:04) DECODE OF CPU ADR(01:00) (03:00) FORCED (0)	FORCED (1)	FORCED (0)	
ISR RESPONSE	NORMAL FORCE ISR DATA	----- 1 0	----- 1 0	----- 1 0	----- DISABLED (0)	----- FORCED (0000)	----- WRITE DATA LATCH	----- WRITE DATA LATCH	----- FORCED (0)	----- FORCED (0)	NO TRANSMIT

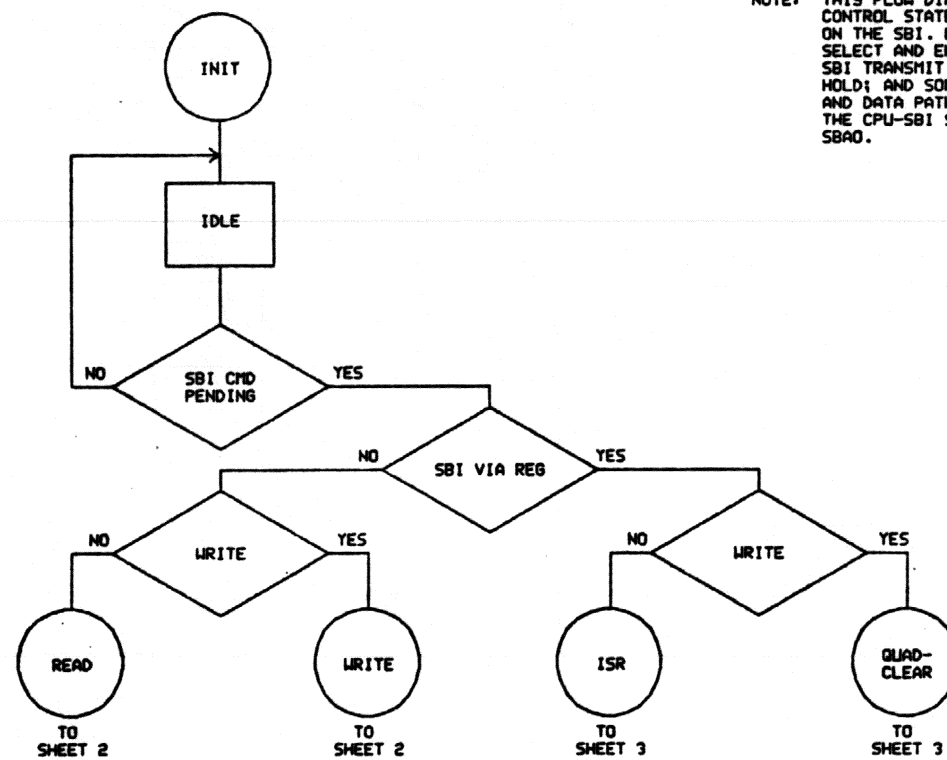
S-DATA ASSEMBLY DATA PATH MUXING

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REVISIONS		
CHK	CHANGE NO.	REV

digital	DRW. J. MARTIN	DATE 18-SEP-84	ENG. J. MARTIN	DATE 18-SEP-84	TITLE: S-DATA PATH OUTPUT MUXING
	CHK'D L. METZGER	DATE 18-SEP-84	BOARD LOCATION:	SHEET	
VEN:G2:(MARTIN)SBI500.DRW 18-SEP-84 10:45			NEXT HIGHER ASSEMBLY: D-DD-KA86-0		SIZE CODE NUMBER REV. D BD KA86-0-SBI5 A
FIRST USED ON OPTION/MODEL:					

8 7 6 5 4 3 2 1



NOTE: THIS FLOW DIAGRAM DESCRIBES THE CONTROL STATES FOR CPU TRANSACTIONS ON THE SBI. EACH STATE HAS SPECIFIC SELECT AND ENABLE INFORMATION FOR THE SBI TRANSMIT MUX; FOR SENDING SBI HOLD; AND SOME STATES TRIGGER CONTROL AND DATA PATH LOGIC. THE CPU-SBI STATE LOGIC IS ON SHEET SBA0.

CPU-SBI STATE MACHINE FLOW DIAGRAM

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REVISIONS		
CHK	CHANGE NO.	REV

digital

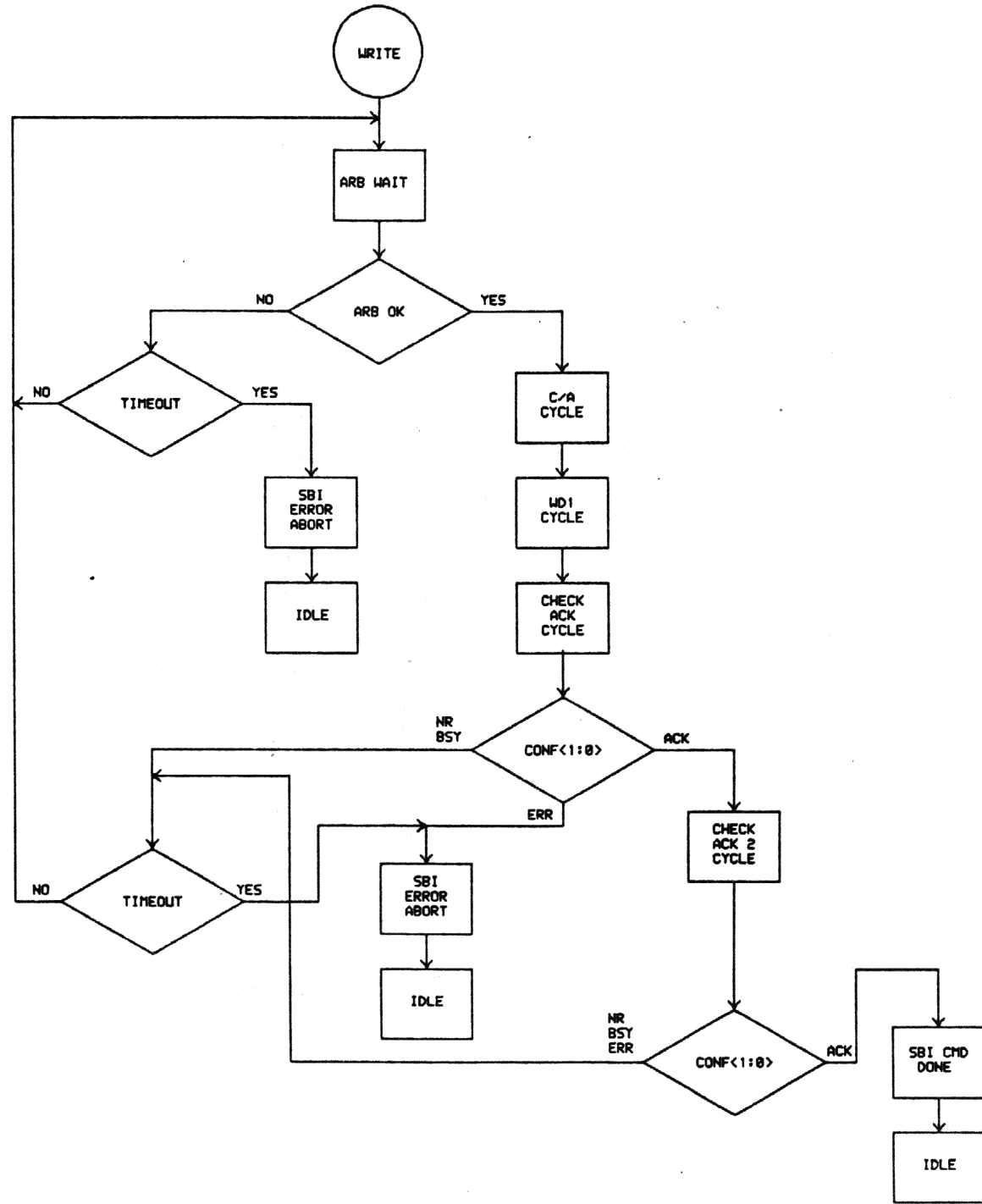
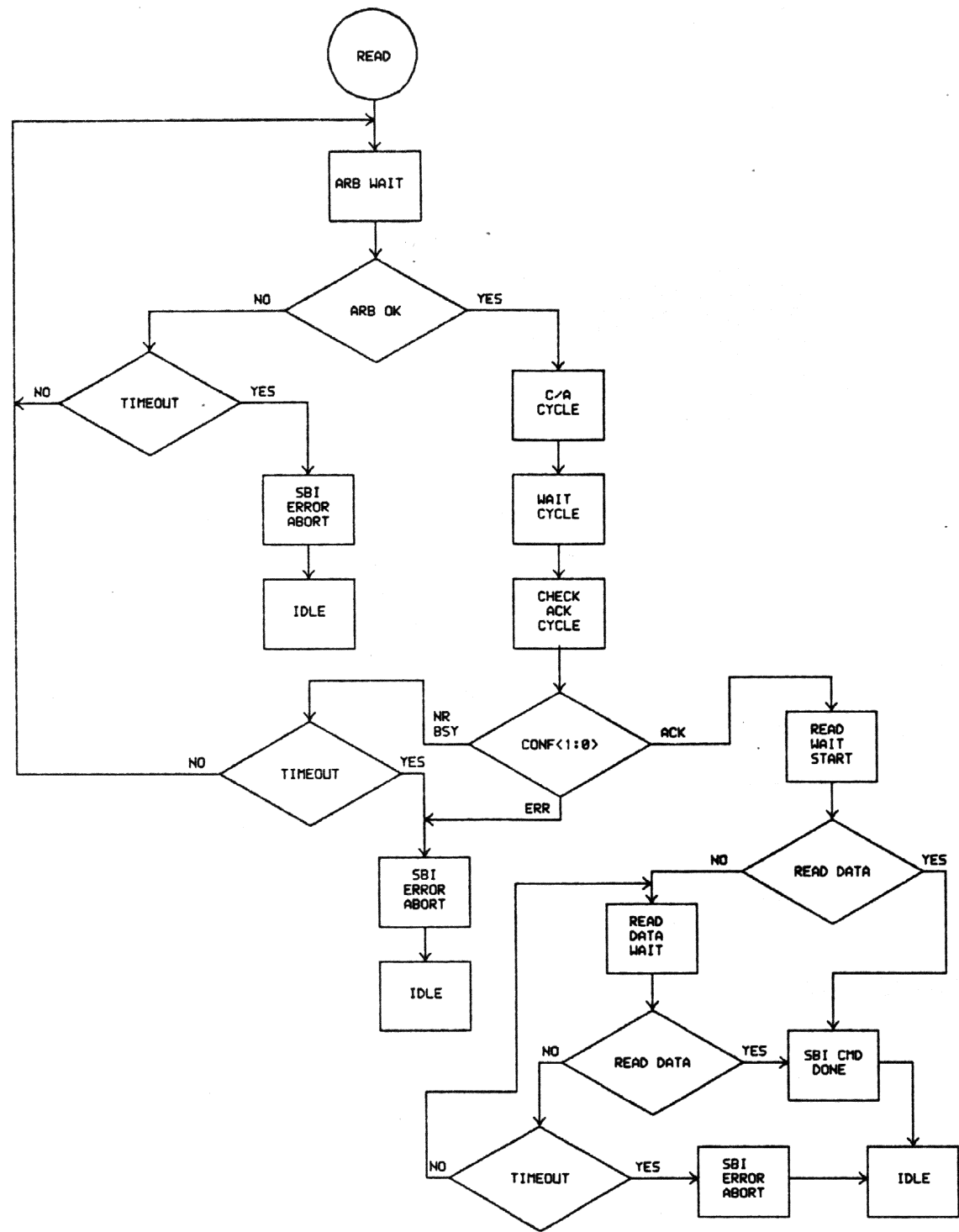
DRN. J. MARTIN
CHK'D. L. METZGER

DATE	ENG.	DATE
18-SEP-84	J. MARTIN	18-SEP-84
DATE	BOARD LOCATION:	OF
18-SEP-84		

TITLE: CPU-SBI STATE MACHINE FLOW

VENING2: <MARTIN>SBI680.DRW	18-SEP-84	10:48	NEXT HIGHER ASSEMBLY:	SIZE	CODE	NUMBER	REV.
FIRST USED ON OPTION/MODEL: D-DD-KA86-0				D	BD	KA86-0-SBI6	A

8 7 6 5 4 3 2 1



CPU-SBI STATE MACHINE FLOW DIAGRAM

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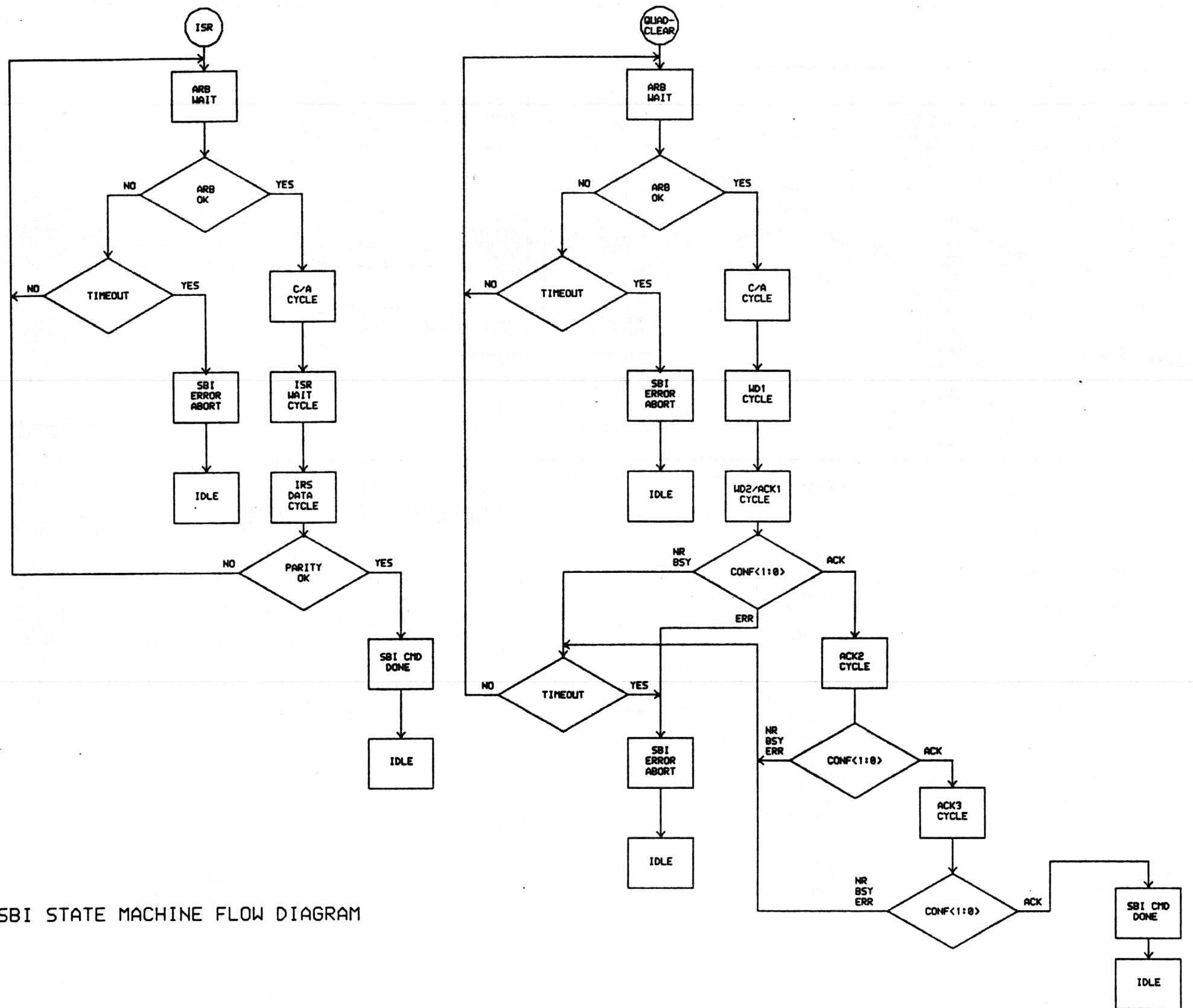
REVISIONS		
CHK	CHANGE NO.	REV

2208	8	7	6	5	4	3	2	1
------	---	---	---	---	---	---	---	---

digital
VENM21<MARTIN>SBI780.DRW 118-SEP-84 10:54
FIRST USED ON OPTION/MODEL:

DRW. J. Martin
CHK'D L. METZGER
DATE 18-SEP-84
DATE 18-SEP-84
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:
D-DD-KA86-0

ENG. J. MARTIN
BOARD LOCATION:
TITLE: SBI STATE MACHINE READ/WRITE
SIZE CODE D BD
NUMBER KA86-0-SBI7
REV. A



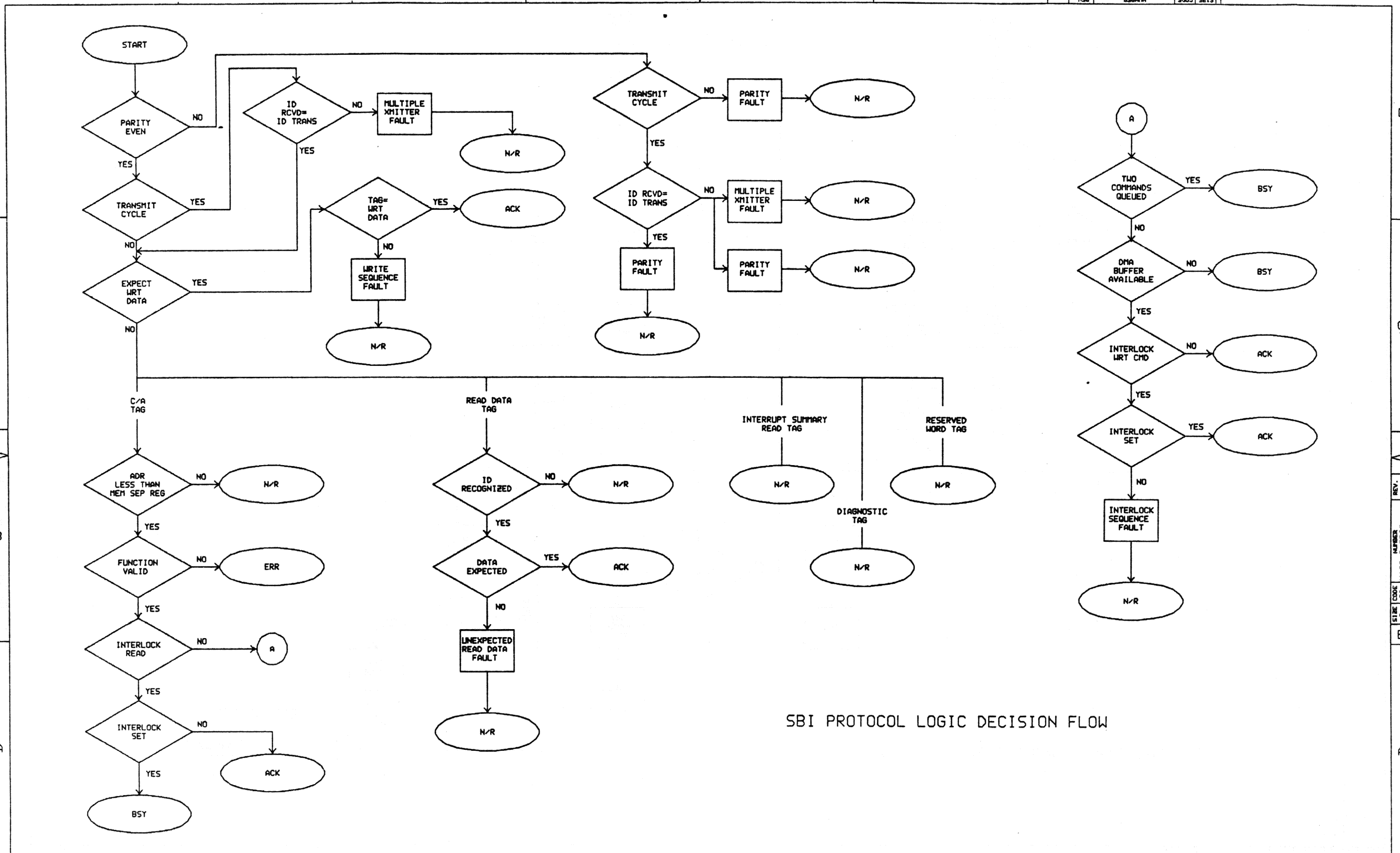
CPU-SBI STATE MACHINE FLOW DIAGRAM

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REVISIONS	
CHK	CHANGE NO. REV

VEN:MG2:(MARTIN)SBI08D.DRW 18-SEP-84 10:52	DATE 18-SEP-84	ENG. J. MARTIN	DATE 18-SEP-84	TITLE: SBI STATE MACHINE
CHK'D. L. NETZGER	DATE 18-SEP-84	BOARD LOCATION:	SHEET	ISR/QUADCLEAR
FIRST USED ON OPTION MODEL:	NEXT HIGHER ASSEMBLY: D-DD-KA86-0		SIZE CODE D BD	NUMBER KA86-0-SB18

8 7 6 5 4 3 2 1



SBI PROTOCOL LOGIC DECISION FLOW

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VENM21<MARTIN>SBI98D.DRW 118-SEP-84 10:58 NEXT HIGHER ASSEMBLY: D-DD-KA86-0				FIRST USED ON OPTION/MODEL:		SIZE CODE: D BD		NUMBER: KA86-0-SBI9		REV. A	
8	7	6	5	4	3	2	1				

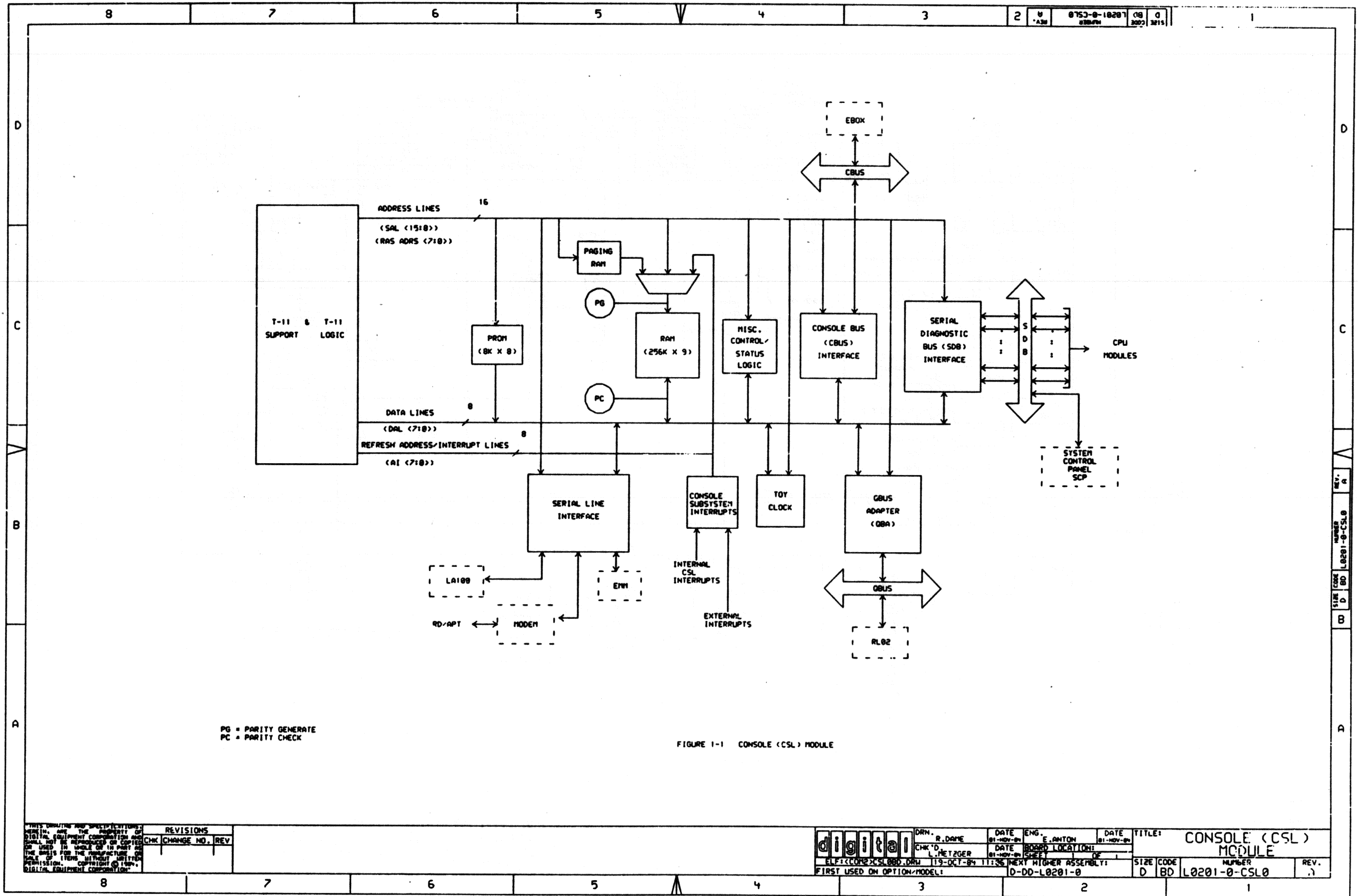


FIGURE 1-1 CONSOLE (CSL) MODULE

REVISIONS	
CHK	CHANGE NO. REV

	DRN. R. DANE	DATE 01-NOV-84	ENG. E. ANTON	DATE 01-NOV-84	TITLE: CONSOLE (CSL) MODULE
	CHK'D L. NETZGER	DATE 01-NOV-84	BOARD LOCATION: 08	SHEET: 01	REV. :
FIRST USED ON OPTION/MODEL: D-DD-L0201-0					SIZE CODE D BD
NUMBER L0201-0-CSL0					REV. :

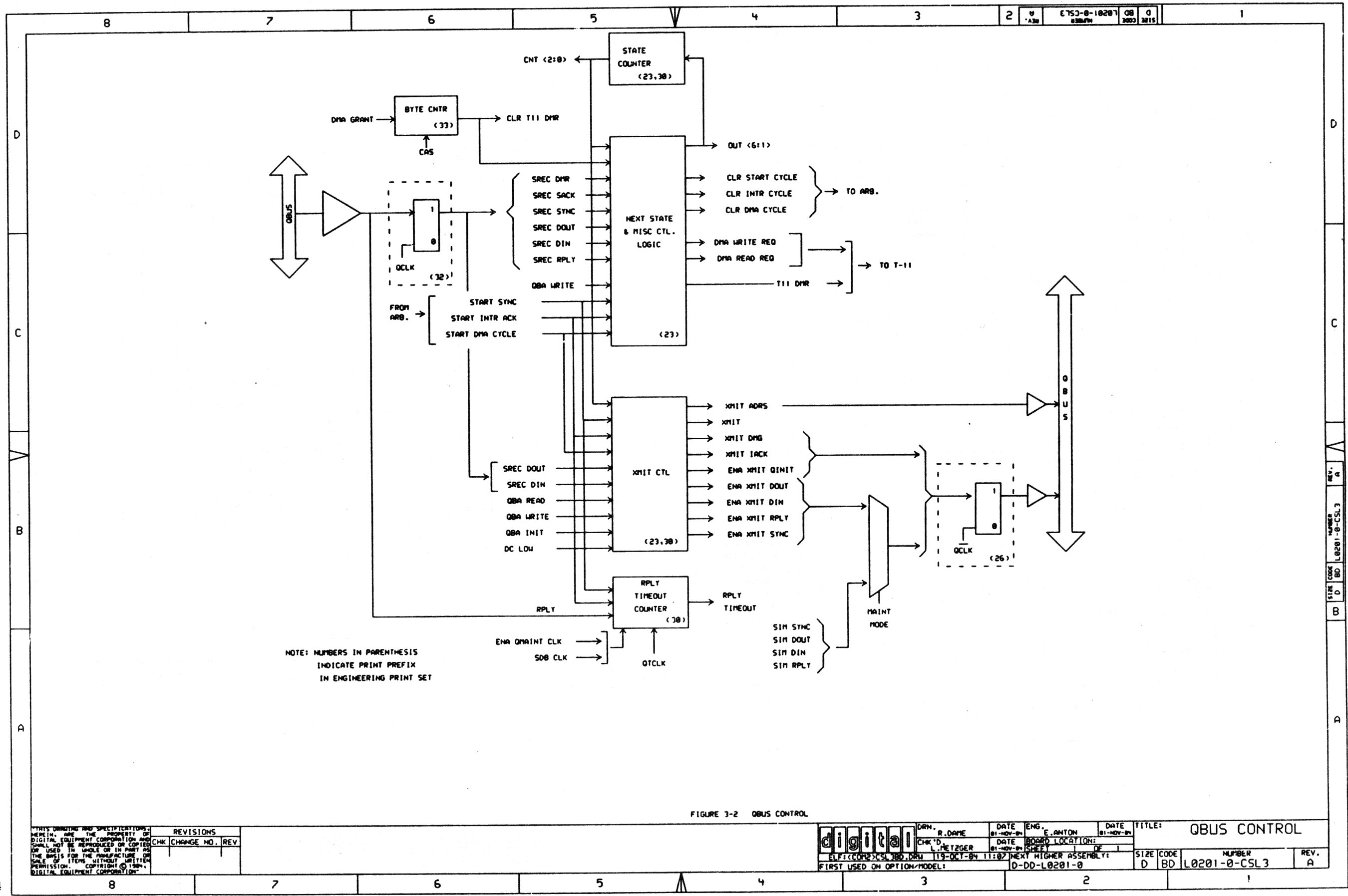


FIGURE 3-2 OBUS CONTROL

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REVISIONS	
CHK	CHANGE NO. REV

digital	DRN. R. DAME	DATE 01-NOV-84	ENG. E. ANTON	DATE 01-NOV-84	TITLE: OBUS CONTROL
	CHK'D L. NETZGER	DATE 01-NOV-84	BOARD LOCATION: DE 1	DE 1	
FIRST USED ON OPTION/MODEL: 0-DD-L0201-0					SIZE CODE D BD
NEXT HIGHER ASSEMBLY: 0-DD-L0201-0					NUMBER L0201-0-CSL3
					REV. A

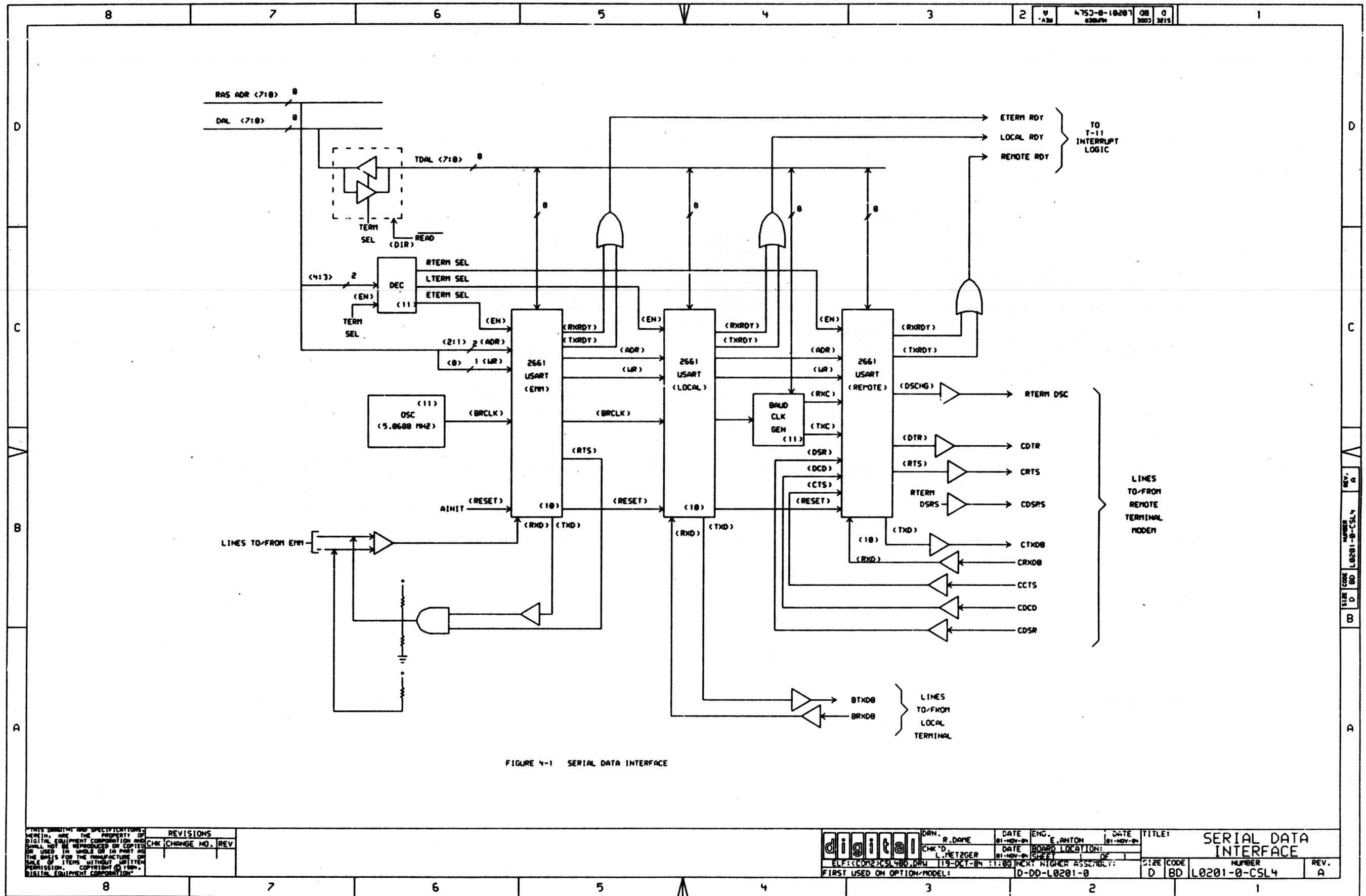


FIGURE 4-1 SERIAL DATA INTERFACE

REVISIONS	
CHK	CHANGE NO. REV

digital	DRN. R. DAME	DATE 01-NOV-84	ENG. E. ANTON	DATE 01-NOV-84	TITLE: SERIAL DATA INTERFACE
	CHK'D L. METZGER	DATE 19-OCT-84	BOARD LOCATION: 11:00	SHEET	
FIRST USED ON OPTION/MODEL: D-DD-L0201-0					SIZE CODE: D BD
					NUMBER: L0201-0-CSL4
					REV. A

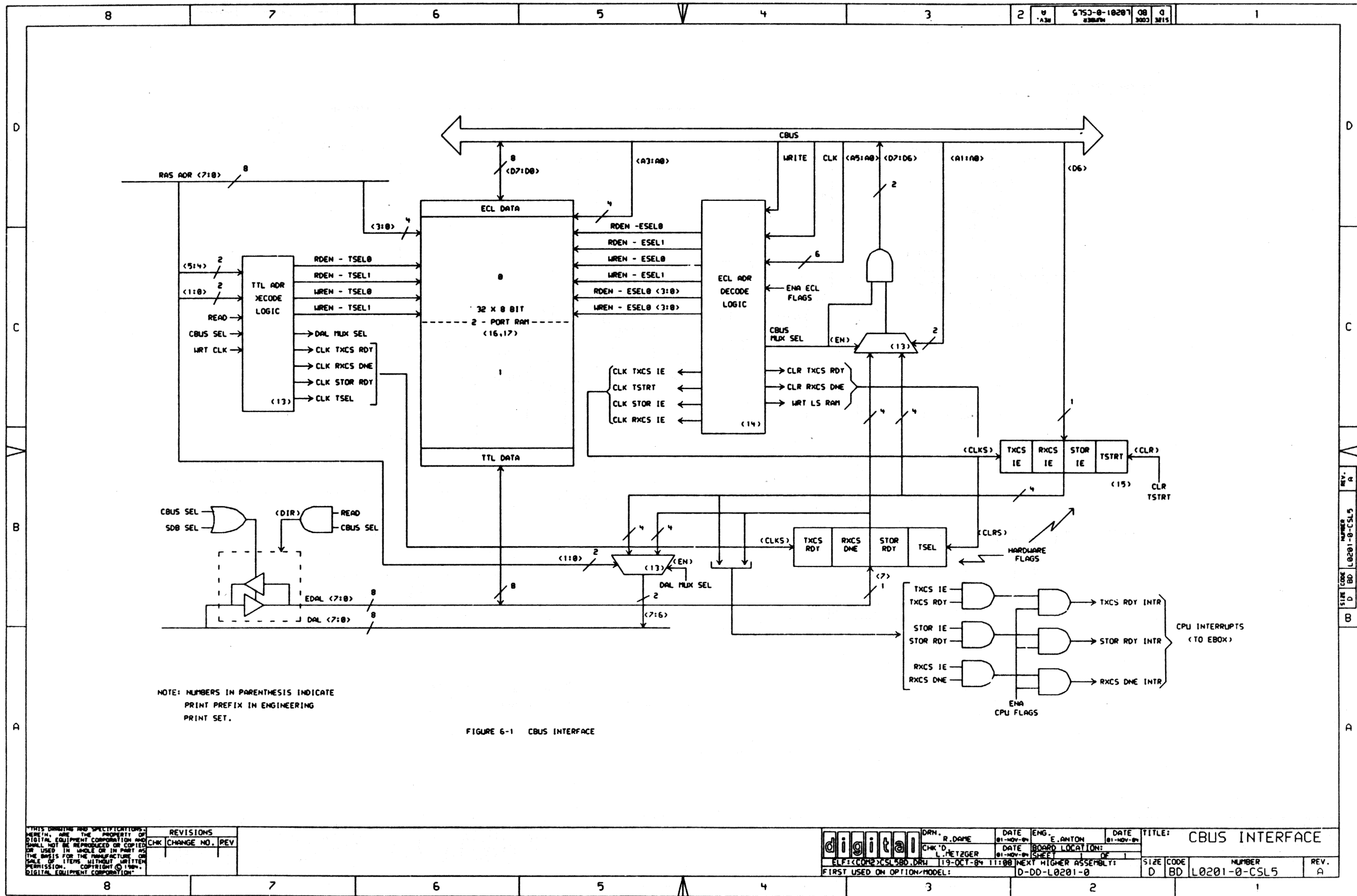


FIGURE 6-1 CBUS INTERFACE

REVISIONS	
CHK	CHANGE NO. REV

digital	DRN. R. DAME	DATE 01-NOV-84	ENG. E. ANTON	DATE 01-NOV-84	TITLE: CBUS INTERFACE
	CHK'D L. METZGER	DATE 01-NOV-84	BOARD LOCATION: 1		
ELF1(COMP)XSL580.DRW 119-OCT-84 11:00 NEXT HIGHER ASSEMBLY: 0-DD-L0201-0				SIZE CODE D BD	NUMBER L0201-0-CSL5
FIRST USED ON OPTION/MODEL: 0-DD-L0201-0				REV. A	

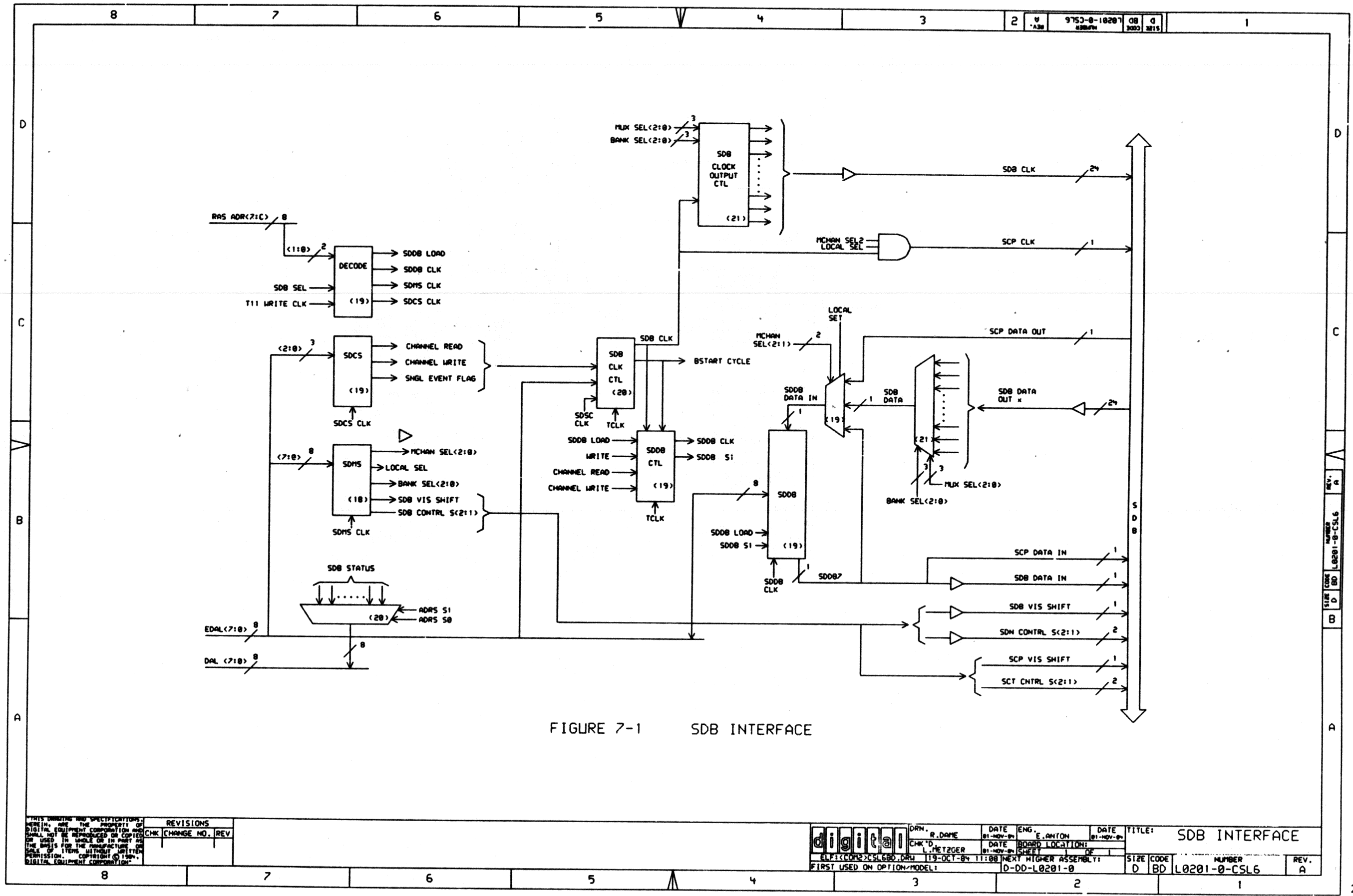


FIGURE 7-1 SDB INTERFACE

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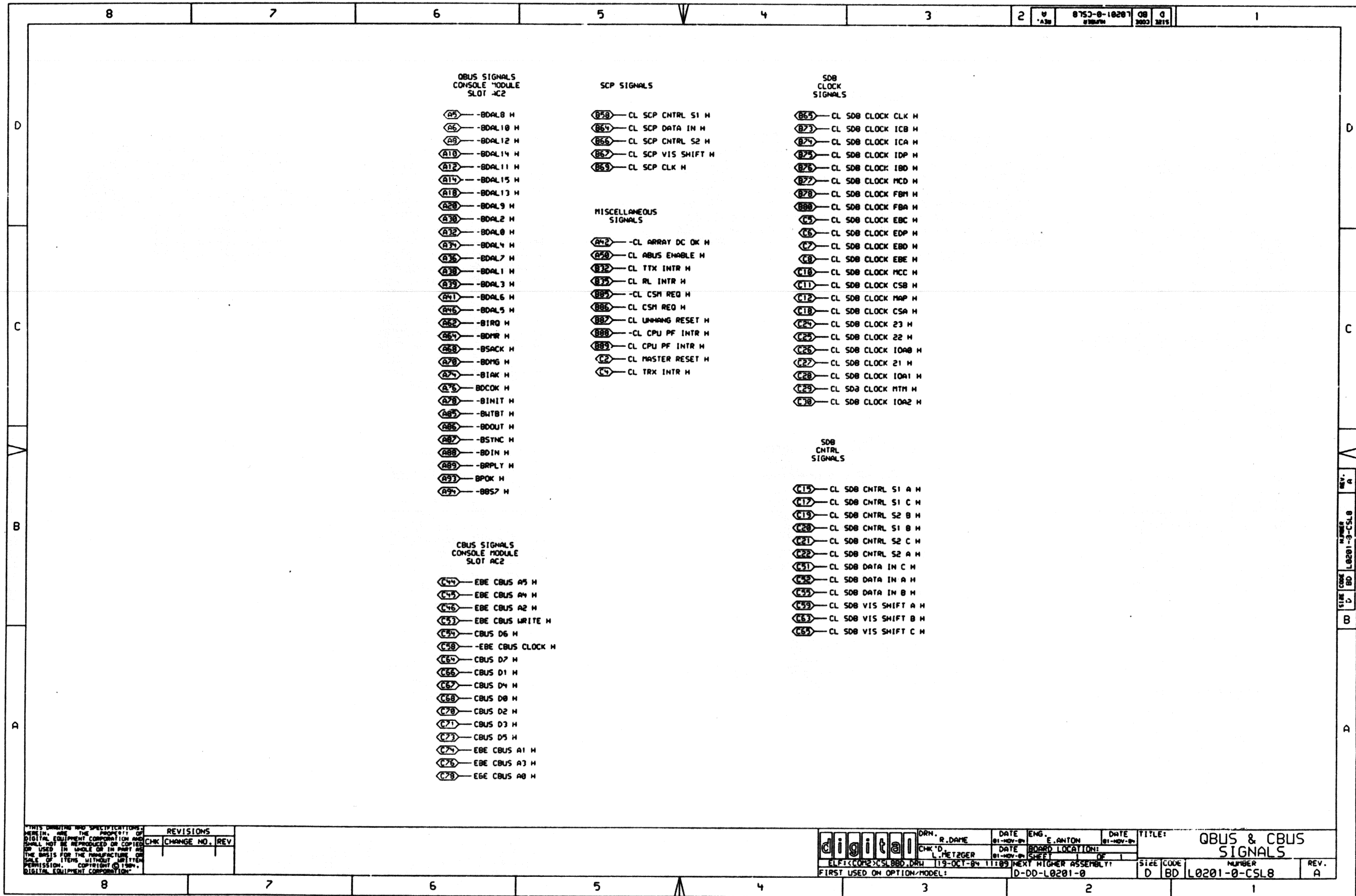
REVISIONS	
CHK	CHANGE NO. REV

digital

DRN. R. DAME	DATE 01-NOV-84	ENG. E. ANTON	DATE 01-NOV-84
CHK'D. L. METZGER	DATE 01-NOV-84	BOARD LOCATION:	
ELF1(C02)CSL60.DRW 119-OCT-84 11:00		NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL:		D-DD-L0201-0	

TITLE: SDB INTERFACE	
SIZE CODE D BD	NUMBER L0201-0-CSL6
REV. A	

REV. A



OBUS SIGNALS
CONSOLE MODULE
SLOT AC2

- (A5) -BDAL8 H
- (A6) -BDAL10 H
- (A8) -BDAL12 H
- (A10) -BDAL14 H
- (A12) -BDAL11 H
- (A14) -BDAL15 H
- (A18) -BDAL13 H
- (A20) -BDAL9 H
- (A30) -BDAL2 H
- (A32) -BDAL0 H
- (A34) -BDAL4 H
- (A36) -BDAL7 H
- (A38) -BDAL1 H
- (A39) -BDAL3 H
- (A41) -BDAL6 H
- (A45) -BDAL5 H
- (A62) -BIRD H
- (A64) -BDMR H
- (A68) -BSACK H
- (A70) -BDMG H
- (A74) -BIAK H
- (A75) -BDCOK H
- (A78) -BINIT H
- (A85) -BUTBT H
- (A86) -BDOUT H
- (A87) -BSTNC H
- (A88) -BDIN H
- (A89) -BRPLY H
- (A93) -BPOK H
- (A94) -BBS7 H

CBUS SIGNALS
CONSOLE MODULE
SLOT AC2

- (C44) -EBE CBUS A5 H
- (C45) -EBE CBUS A4 H
- (C46) -EBE CBUS A2 H
- (C53) -EBE CBUS WRITE H
- (C54) -CBUS D6 H
- (C58) -EBE CBUS CLOCK H
- (C64) -CBUS D7 H
- (C66) -CBUS D1 H
- (C67) -CBUS D4 H
- (C68) -CBUS D0 H
- (C70) -CBUS D2 H
- (C71) -CBUS D3 H
- (C73) -CBUS D5 H
- (C74) -EBE CBUS A1 H
- (C75) -EBE CBUS A3 H
- (C78) -EBE CBUS A0 H

SCP SIGNALS

- (B58) -CL SCP CNTRL S1 H
- (B64) -CL SCP DATA IN H
- (B66) -CL SCP CNTRL S2 H
- (B67) -CL SCP VIS SHIFT H
- (B69) -CL SCP CLK H

MISCELLANEOUS
SIGNALS

- (A42) -CL ARRAY DC OK H
- (A50) -CL ABUS ENABLE H
- (B12) -CL TTX INTR H
- (B15) -CL RL INTR H
- (B84) -CL CSM REQ H
- (B86) -CL CSM REQ H
- (B87) -CL UNHANG RESET H
- (B88) -CL CPU PF INTR H
- (B89) -CL CPU PF INTR H
- (C2) -CL MASTER RESET H
- (C4) -CL TRX INTR H

SDB
CLOCK
SIGNALS

- (B63) -CL SDB CLOCK CLK H
- (B73) -CL SDB CLOCK ICB H
- (B74) -CL SDB CLOCK ICA H
- (B75) -CL SDB CLOCK IDP H
- (B76) -CL SDB CLOCK IBD H
- (B77) -CL SDB CLOCK MCD H
- (B78) -CL SDB CLOCK FBM H
- (B80) -CL SDB CLOCK FBA H
- (C5) -CL SDB CLOCK EBC H
- (C6) -CL SDB CLOCK EDP H
- (C7) -CL SDB CLOCK EBD H
- (C8) -CL SDB CLOCK EBE H
- (C10) -CL SDB CLOCK MCC H
- (C11) -CL SDB CLOCK CSB H
- (C12) -CL SDB CLOCK MAP H
- (C18) -CL SDB CLOCK CSA H
- (C24) -CL SDB CLOCK 23 H
- (C25) -CL SDB CLOCK 22 H
- (C26) -CL SDB CLOCK IOA0 H
- (C27) -CL SDB CLOCK 21 H
- (C28) -CL SDB CLOCK IOA1 H
- (C29) -CL SDB CLOCK ITH H
- (C30) -CL SDB CLOCK IOA2 H

SDB
CNTRL
SIGNALS

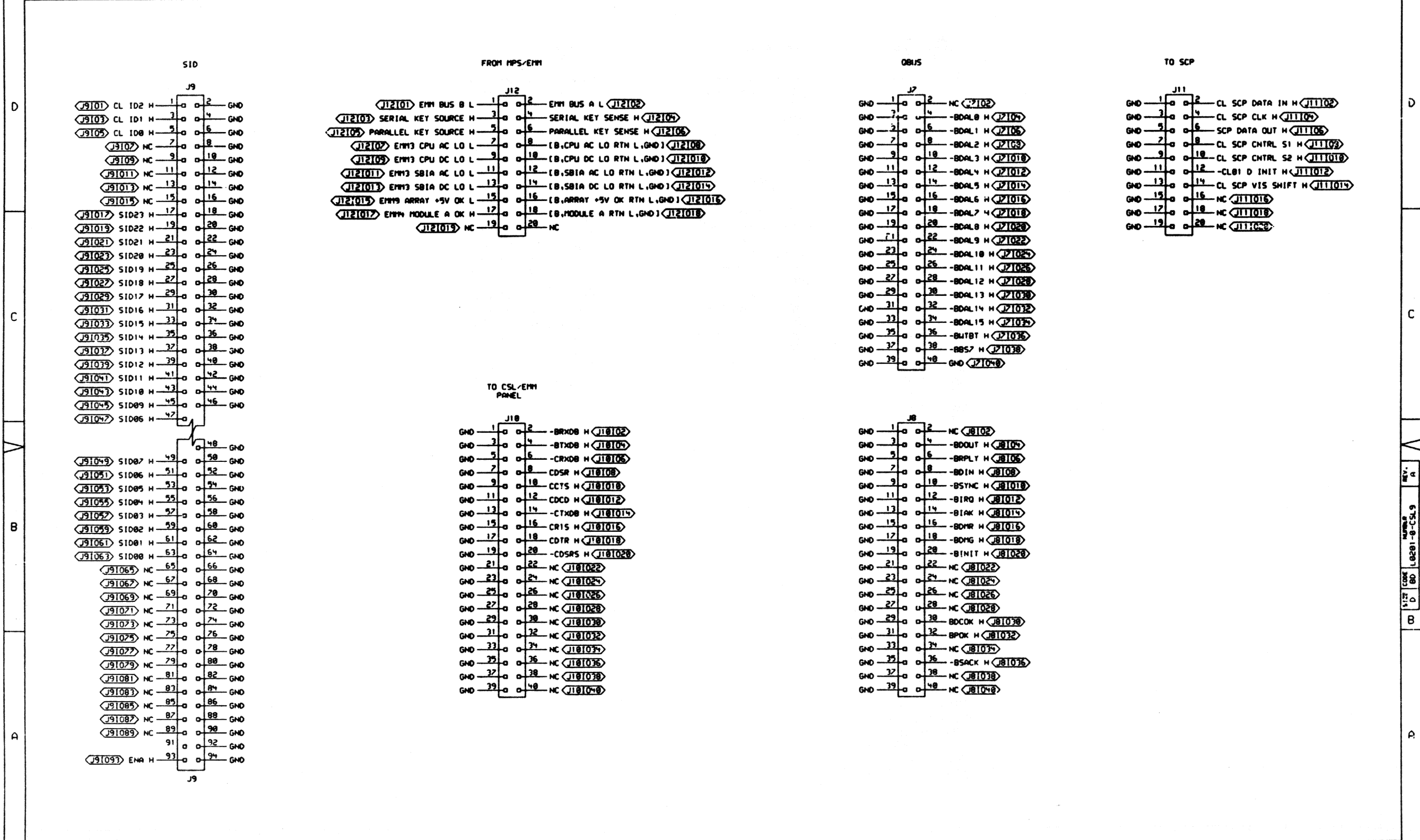
- (C15) -CL SDB CNTRL S1 A H
- (C17) -CL SDB CNTRL S1 C H
- (C19) -CL SDB CNTRL S2 B H
- (C20) -CL SDB CNTRL S1 B H
- (C21) -CL SDB CNTRL S2 C H
- (C22) -CL SDB CNTRL S2 A H
- (C51) -CL SDB DATA IN C H
- (C52) -CL SDB DATA IN A H
- (C55) -CL SDB DATA IN B H
- (C59) -CL SDB VIS SHIFT A H
- (C63) -CL SDB VIS SHIFT B H
- (C65) -CL SDB VIS SHIFT C H

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REVISIONS	
CHK	CHANGE NO. REV

digital	DRN. R. DAME	DATE 01-NOV-84	ENG. E. ANTON	DATE 01-NOV-84	TITLE: QBUS & CBUS SIGNALS
	CHK'D L. METZGER	DATE 119-OCT-84	BOARD LOCATION: 11109	SHEET	NUMBER L0201-0-C5L8
FIRST USED ON OPTION/MODEL: D-DD-L0201-0				SIZE CODE D BD	REV. A

REV. A
 NUMBER L0201-0-C5L8
 SIZE CODE D BD
 REV. A

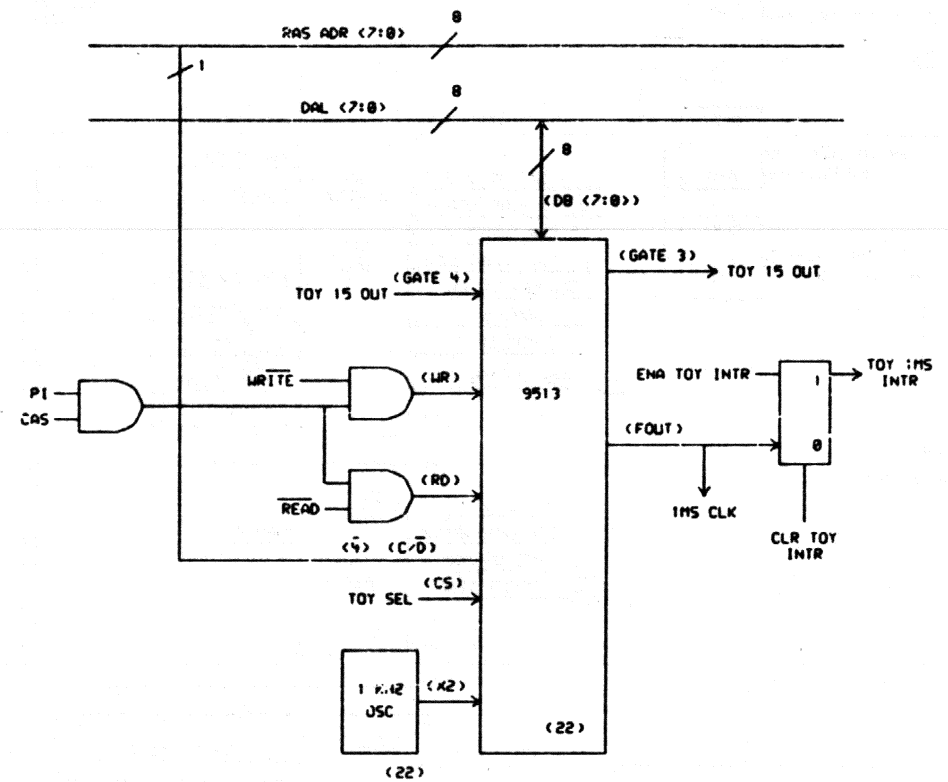


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REV.	CHANGE NO.	REV.

DATE	ENG.	DATE	FILE:
01-NOV-84	E. ANTON	01-NOV-84	

digital CORP. R. DATE DATE ENG. E. ANTON DATE FILE:
 CHK'D. L. METZGER DATE BOARD LOCATION: 01-NOV-84
 ELFCOMR:CSL980.DRW 119-OCT-84 11:09 NEXT HIGHER ASSEMBLY: DE
 FIRST USED ON OPTION/MODEL: D-DD-L0201-0 SIZE CODE NUMBER REV.
 D BD L0201-0-CSL9 A



NOTE : NUMBERS IN PARENTHESIS
INDICATE PRINT PREFIX
IN ENGINEERING PRINT SET

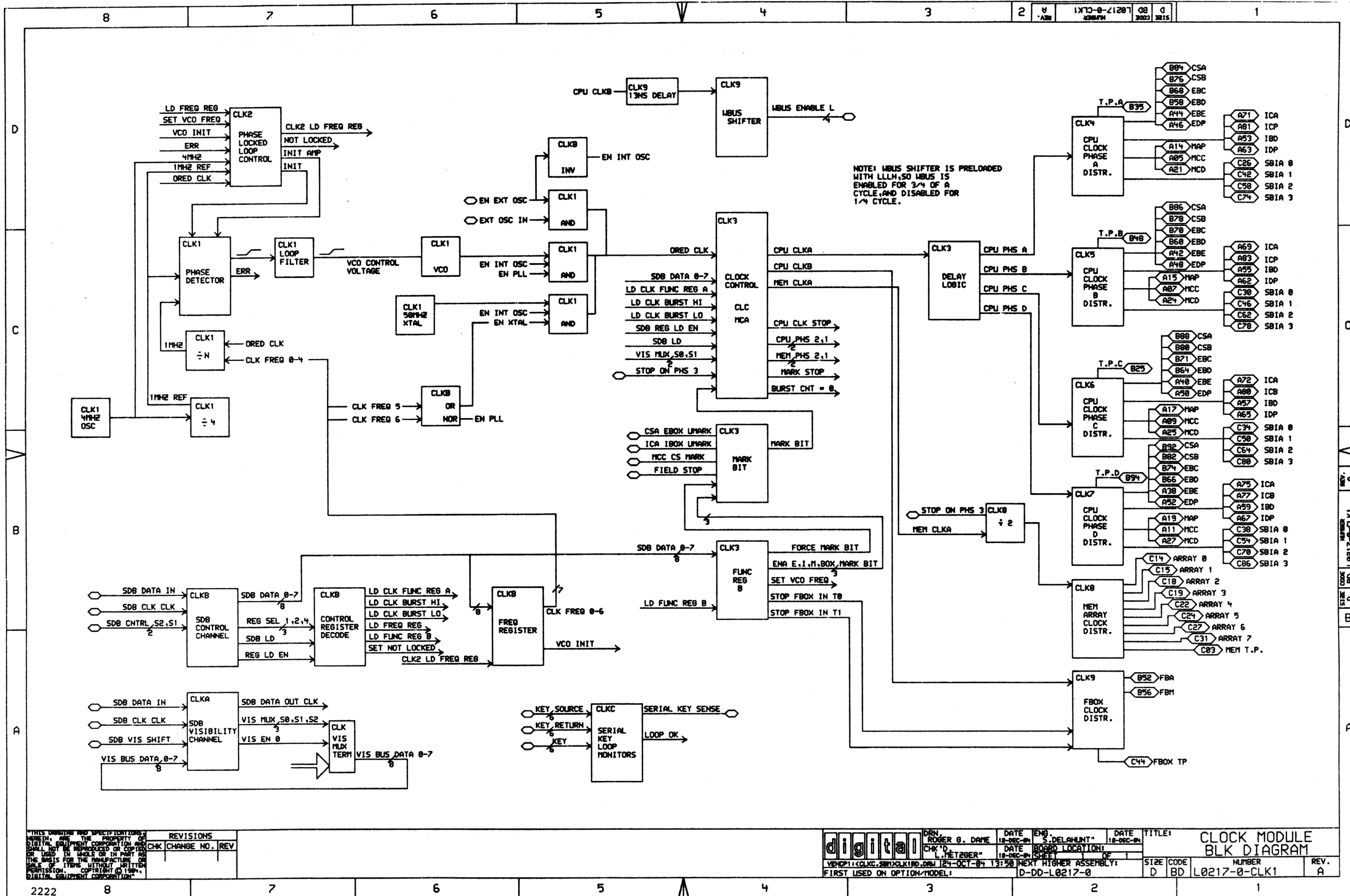
FIGURE 5-1 TOY CLOCK CONTROLLER

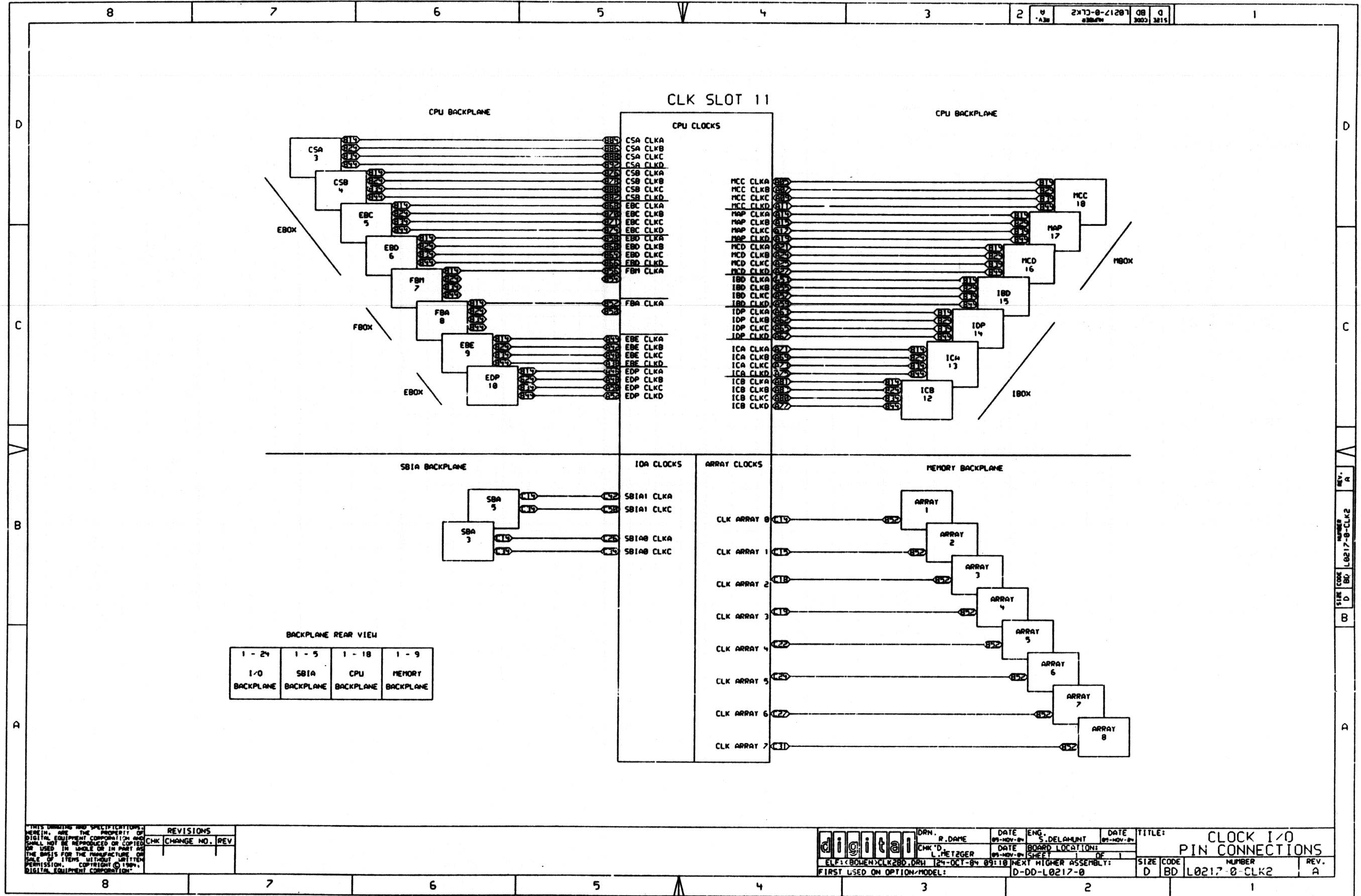
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REVISIONS	
CHK	CHANGE NO. REV.

digital	DRN. R. DAME	DATE 01-NOV-84	ENG. E. ANTON	DATE 01-NOV-84	TITLE: TOY CLOCK CONTROLLER
	CHK'D L. METZGER	DATE 01-NOV-84	BOARD LOCATION:	SHEET 1 OF 1	NUMBER L0201-0-CSLA
FIRST USED ON OPTION/MODEL: D-DD-L0201-0					REV. A

REV. A
NUMBER L0201-0-CSLA
SIZE CODE D BD
B



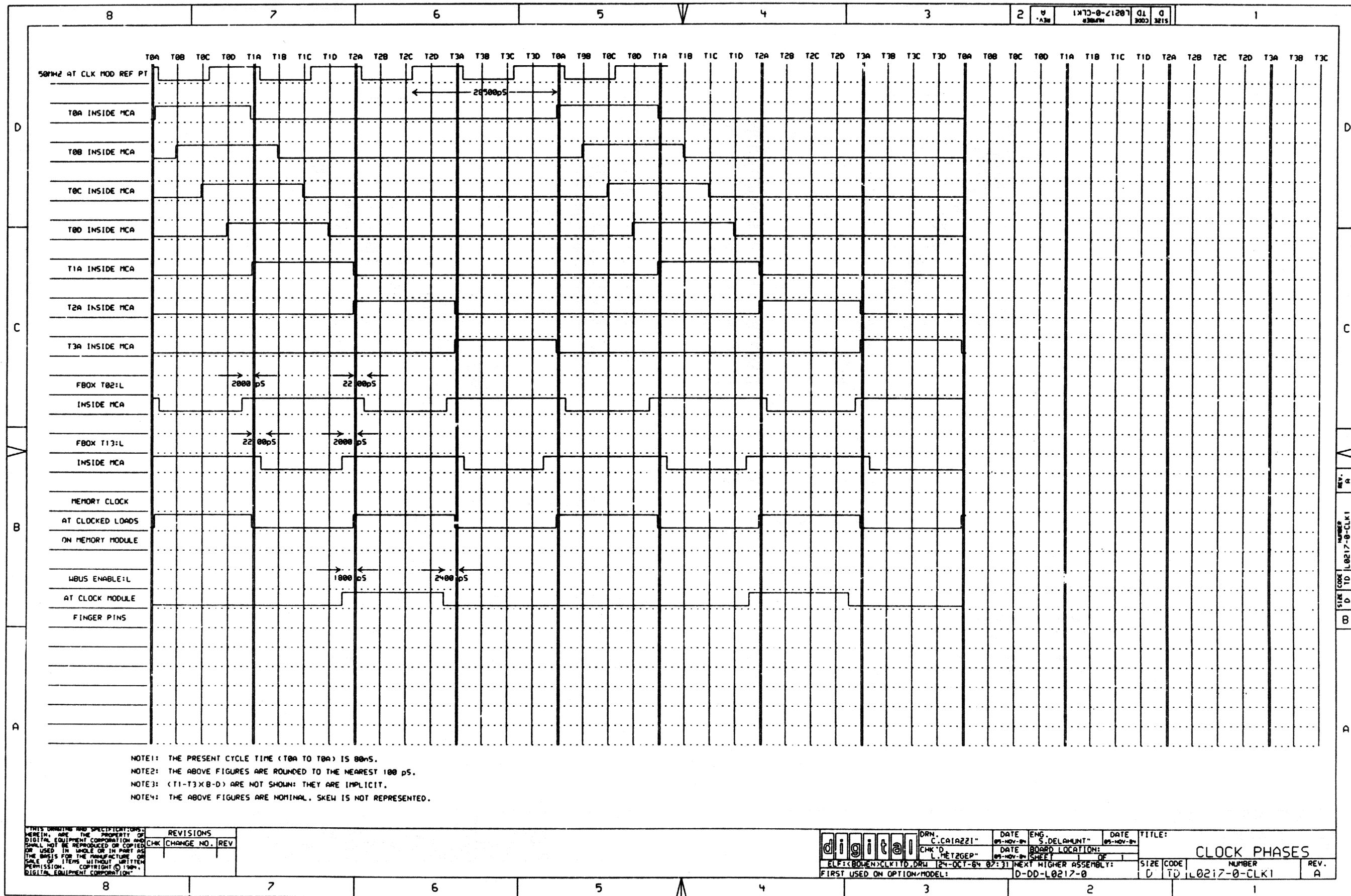


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REVISIONS	
CHK	CHANGE NO. REV

digital	DRN. R. DAME	DATE 03-NOV-84	ENG. S. DELAMUNT	DATE 03-NOV-84	TITLE: CLOCK I/O
	CHK'D L. METZGER	DATE 24-OCT-84	DATE BOARD LOCATION: 09-NOV-84	SHEET 1 OF 1	PIN CONNECTIONS
ELF: <BOWEN> CLK2BD.DRW		124-OCT-84 09:18	NEXT HIGHER ASSEMBLY: D-DD-L0217-0	SIZE CODE D BD	NUMBER L0217-0-CLK2
FIRST USED ON OPTION/MODEL:				REV. A	

REV. A
NUMBER L0217-0-CLK2
SIZE CODE D BD



NOTE 1: THIS DIAGRAM SHOWS THE RELATIONSHIPS BETWEEN THE NOMINAL TIMES OF THE CLOCKS AT VARIOUS POINTS IN THE SYSTEM. ALL TIMES ARE SHOWN IN PS (PICO SECONDS)

NOTE 2: ALL OF THE EBOX, IBOX, AND MBOX MODULES HAVE SIMILAR CLOCK DISTRIBUTION LOGIC. THE DESKEM TARGET VALUE FOR EACH OF THESE MODULES IS IDENTICAL (5300 PS)

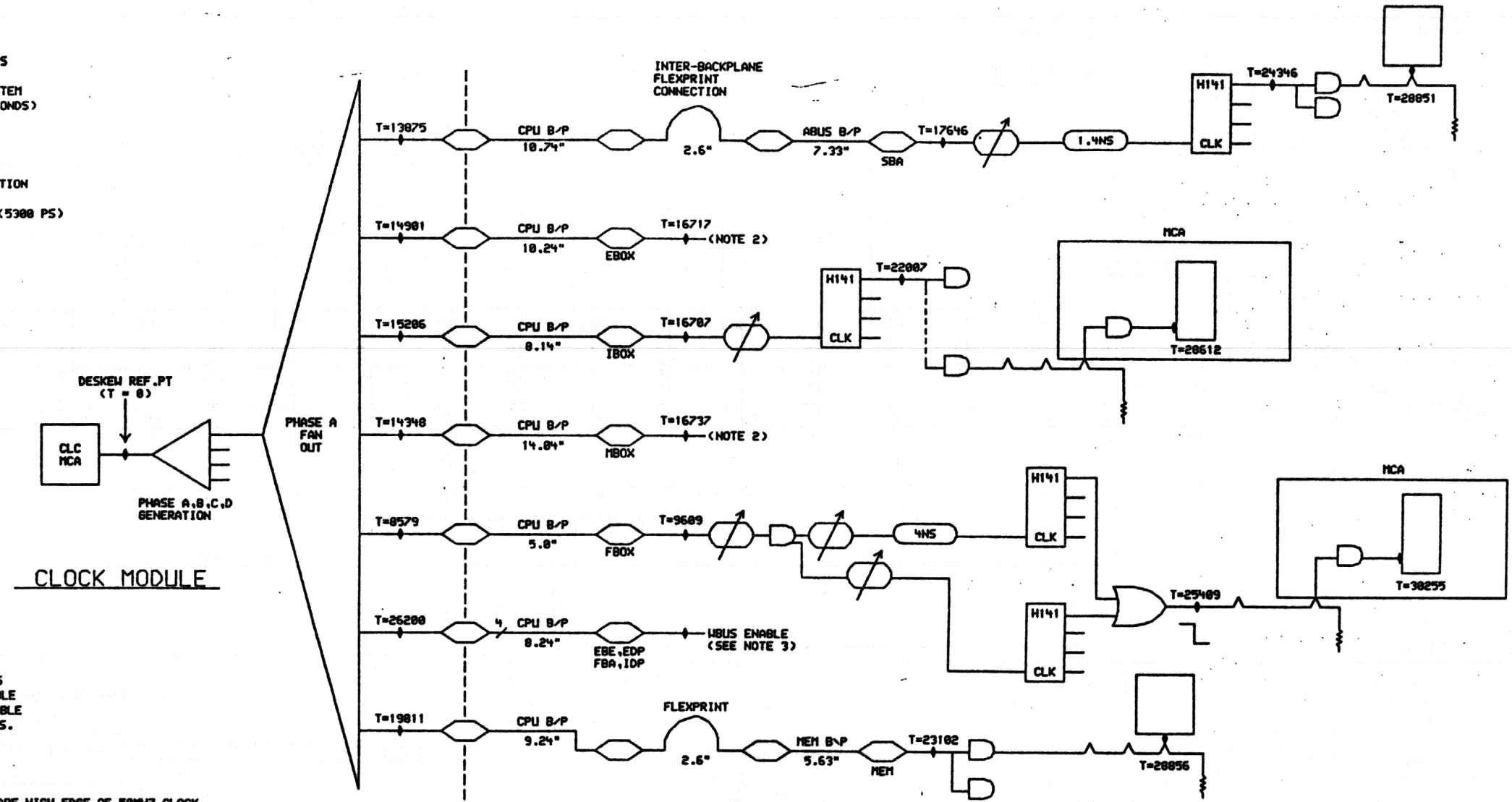
NOTE 3: EACH OF THE 4 MBUS MODULES RECEIVES AN INDIVIDUAL COPY OF THE MBUS ENABLE FROM THE CLOCK MODULE. THE MBUS ENABLE IS NOT DESKEMED ON THE LOGIC MODULES.

NOTE 4: TIMES AT CLOCK MODULE FINGER PINS ARE HIGH EDGE OF 50MHZ CLOCK. TIMES AT LOGIC MODULE FINGER PINS ARE HIGH EDGE OF 50MHZ CLOCK. TIMES AT OTHER POINTS ON E/I/M BOX MODULES ARE FOR LEADING EDGE OF T0A CLOCK.

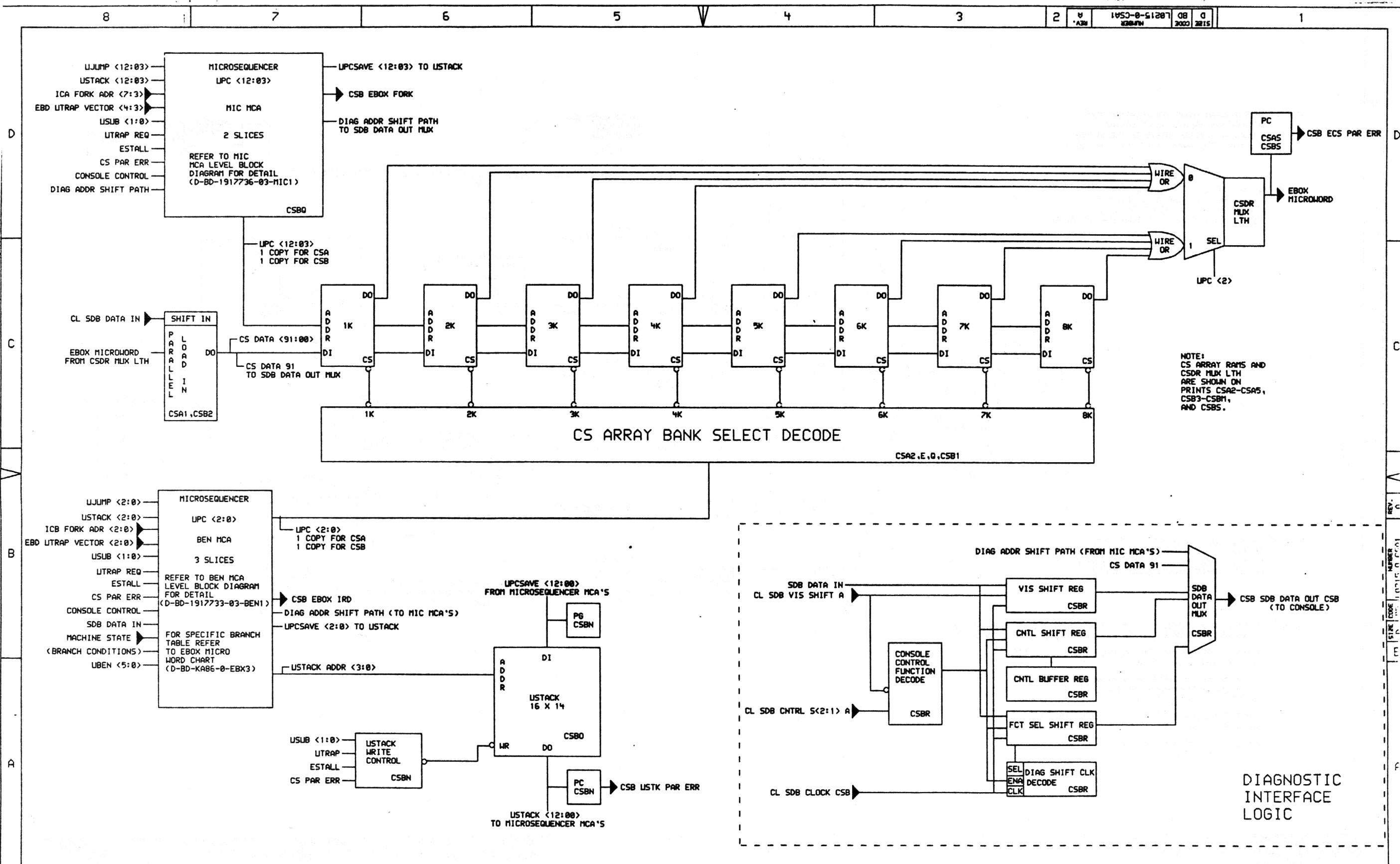
TO CALCULATE THE TIMES FOR T0B, T0C AND T0D, ADD 4545PS, 9091PS AND 13636PS RESPECTIVELY TO THE TIMES SHOWN FOR T0A.

TIMES AT OTHER POINTS ON FBOX MODULES ARE FOR LOW EDGE OF T02 CLOCK.

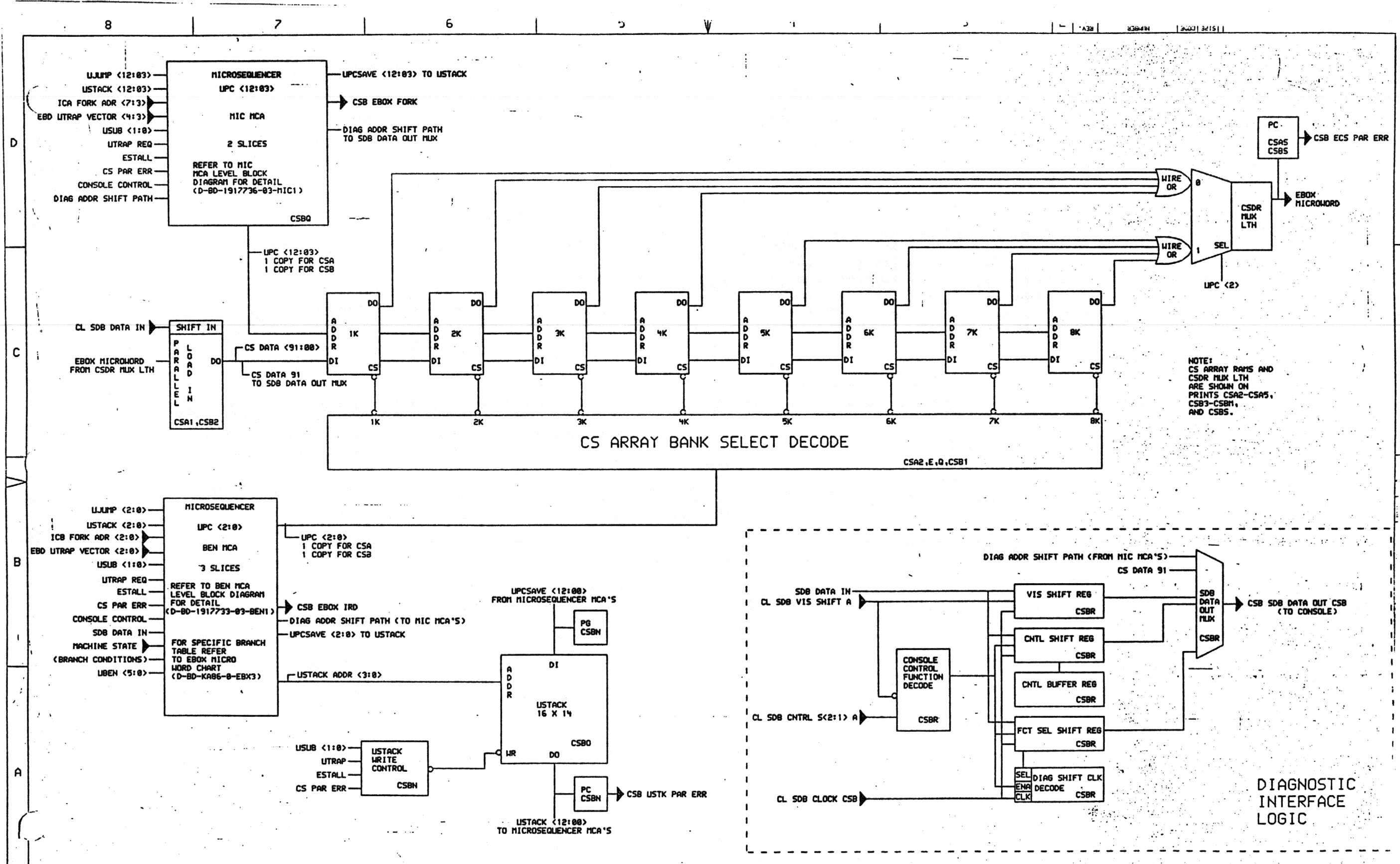
ALL TIMES SHOWN FOR MEMORY CLOCKS ARE FOR HIGH EDGE OF 25MHZ CLOCK.



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REVISIONS																																																			
CHK	CHANGE NO. REV																																																		
DRN	C. CAIAZZI	DATE	24-OCT-84	ENG.	S. DELAHUNT	DATE	24-OCT-84	TITLE:	CLOCK RELATIVE TIMES																																										
CHK'D	L. METZGER	DATE	24-OCT-84	BOARD LOCATION:		SHEET																																													
FIRST USED ON OPTION/MODEL:																																																			
SIZE	CODE	NUMBER	REV.																																																
D	TD	L0217-0-CLK2	A																																																
8	7	6	5	4	3	10/24	2	1																																											



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	CHK	CHANGE NO.	REV	CHK'D	L. METZGER	DATE	21-SEP-84	BOARD LOCATION:	OF	SHEET	OF	SIZE	CODE	NUMBER
													D	BD
FIRST USED ON OPTION/MODEL: D-DD-L0215-0										NEXT HIGHER ASSEMBLY:		REV. A		

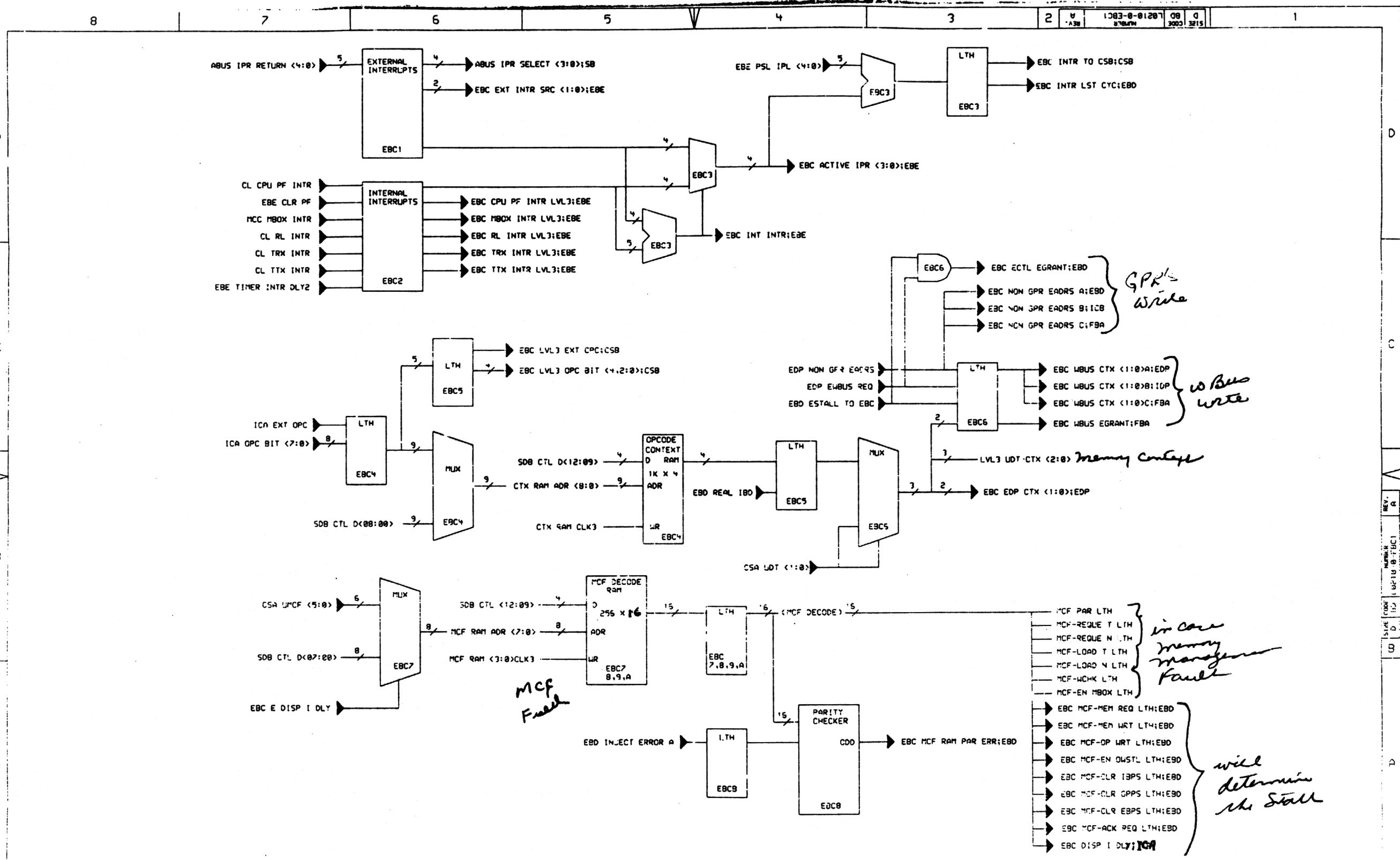


NOTE: CS ARRAY RAMS AND CSDR MUX LTH ARE SHOWN ON PRINTS CSA2-CSA5, CSB3-CSB4, AND CSB5.

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REVISIONS	
CHK	CHANGE NO. REV

digital	DRN. J. SMITH	DATE 21-SEP-84	ENG. B. HILLIARD	DATE 21-SEP-84	TITLE: MICROSEQUENCER BLOCK DIAGRAM
	CHK'D. HETZGER	DATE 21-SEP-84	BOARD LOCATION: 1	SHEET 1	SIZE CODE D BD
VENEER: CSB8, SBXCSB1BD, DRW 113-SEP-84 07:04			NEXT HIGHER ASSEMBLY: D-DD-L0216-0		NUMBER L0216-0-CSB1
FIRST USED ON OPTION/MODEL:					REV. A

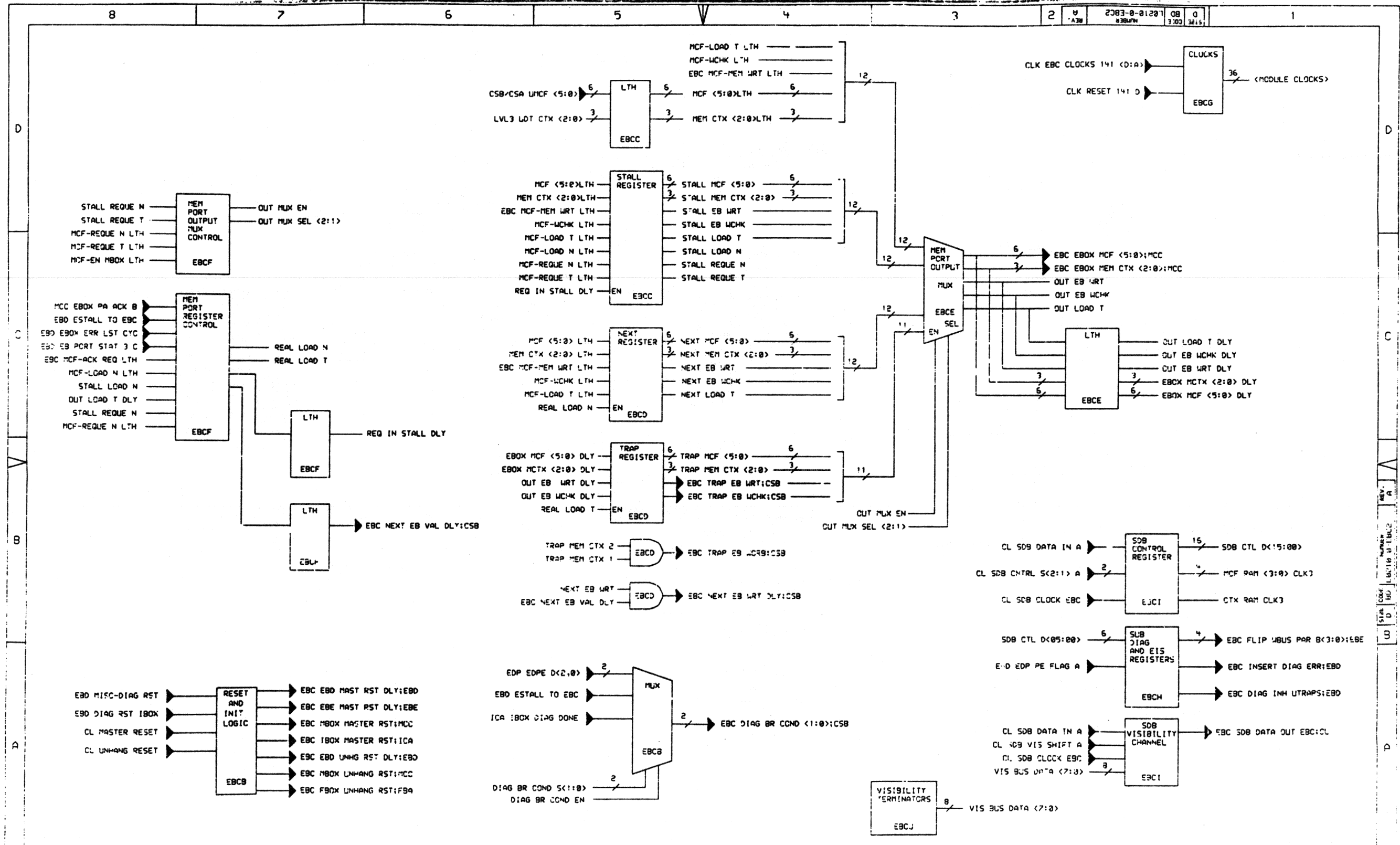


REV. NO.	DATE	BY	DESCRIPTION
1			

REV. NO.	DATE	BY	DESCRIPTION
1			

DRN	W. BCLAND	DATE	ENG. S. REICHERT	DATE	TITLE:
CHK'D	L. H. ZIGER	DATE	BOARD LOCATION:	REV.	BLOCK DIAGRAM
ELP. CONTROL DEPT. DRW	03-JUL-84	08-DEC-84		NUMBER	EBC (L0210)
FIRST USED ON OPTION/MODEL:	0-DD-L0210-0	0-DD-L0210-0		REV.	

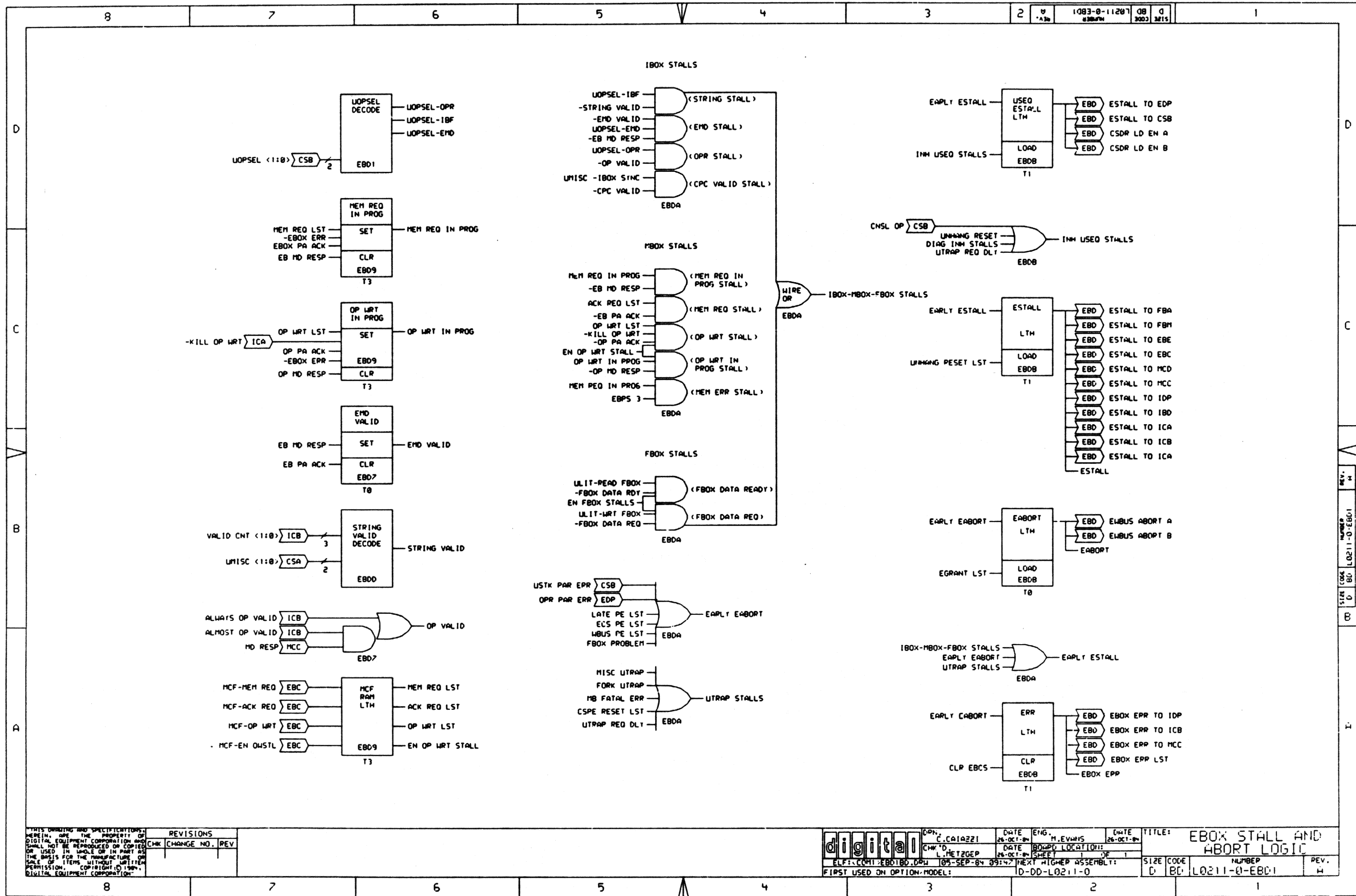
2228



REV.	NO.	DATE	BY	CHK	CHANGE NO.	REV.

DRN: U. BOLAND	DATE: 8-DEC-84	ENG: S. REICHERT	DATE: 20-DEC-84	TITLE: BLOCK DIAGRAM EBC (L2210)
CLK TO: NETZGER	DATE: 10-DEC-84	BOARD LOCATION: 3F	DATE: 10-DEC-84	SIZE: CODE: D BD
ELP: (CC) * EBC (20) DRU	03-JUL-84	10:25	NEXT FIGURE ASSEMBLY: D-00-L2210-0	NUMBER: 112
FIRST USED ON OPTION MODEL:	D-00-L2210-0	REV.:	A	

REV. A
 NUMBER 112
 CODE D BD
 SIZE 11x19 1/2
 SHEET 1 OF 1

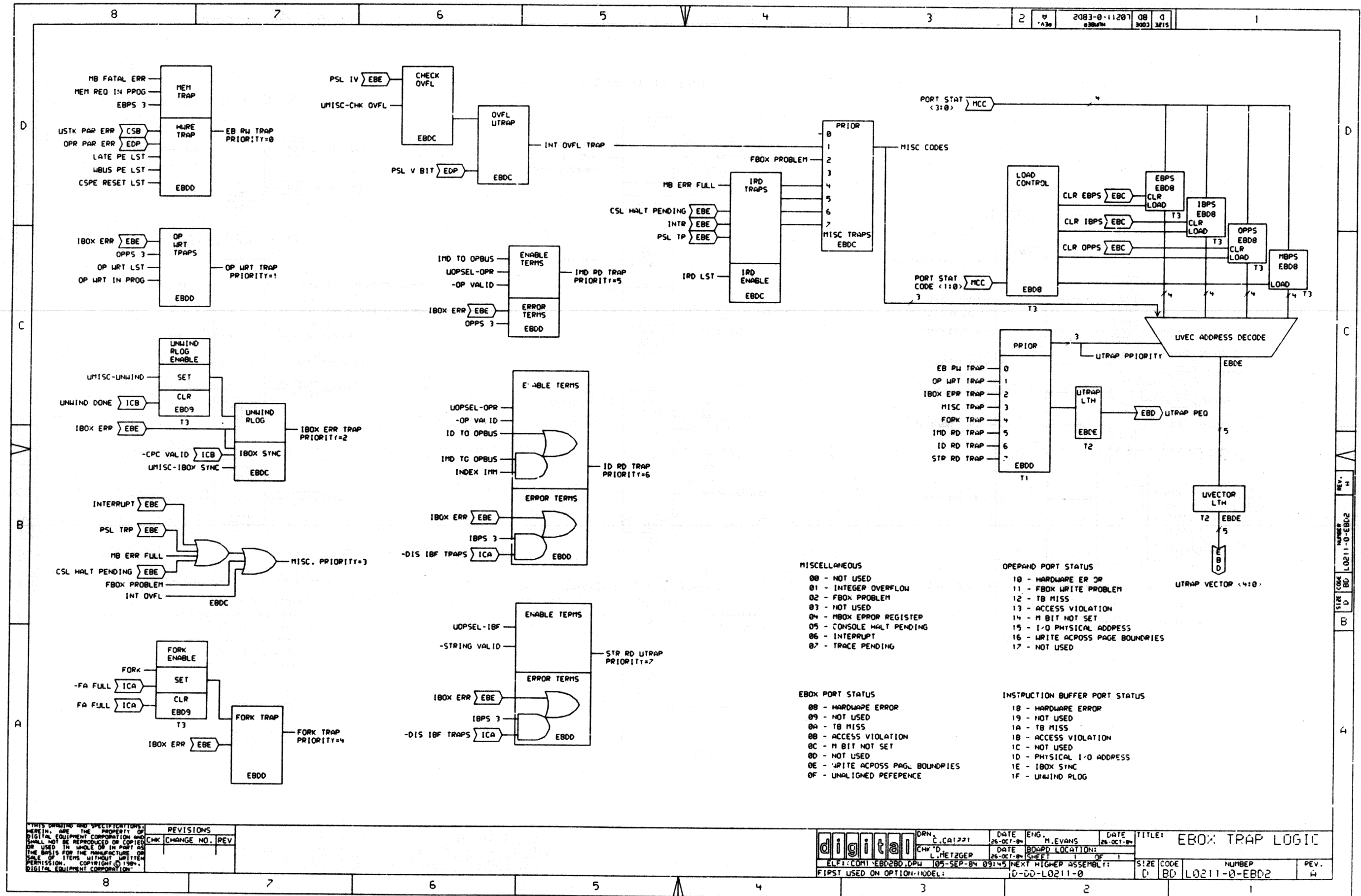


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REVISIONS	
CHK	CHANGE NO. REV.

digital	CON. C. CAIAZZI	DATE 26-OCT-84	ENG. M. EVANS	DATE 26-OCT-84	TITLE: EBOX STALL AND ABORT LOGIC
	CHK'D L. METZGER	DATE 26-OCT-84	BOUNDO LOCATION: 1	SHEET 1	
ELF:COM1:EB01BD.DWG	105-SEP-84 09:14	NEXT HIGHER ASSEMBLY: 10-DD-L0211-0			
FIRST USED ON OPTION MODEL: 10-DD-L0211-0					

REV. 2
SIZE CODE NUMBER
D B L0211-0-EB01
CO

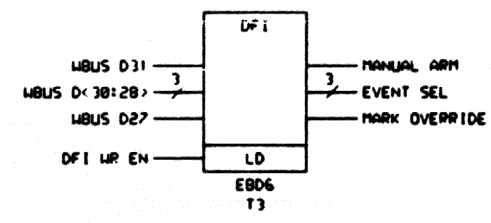


REVISIONS	
CHK	CHANGE NO. REV

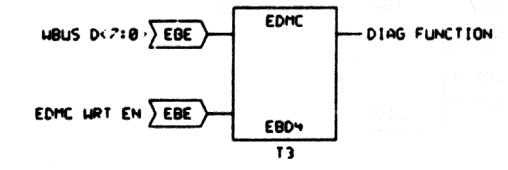
digital	DRN	C. CA! 221	DATE	26-OCT-84	ENG.	M. EVANS	DATE	26-OCT-84	TITLE	EBOX TRAP LOGIC				
	CHK'D	L. METZGER	DATE	26-OCT-84	BOWD. LOCATION:		SHEET	1 OF 1	SIZE	CODE	NUMBER	REV.		
FIRST USED ON OPTION MODEL:										0-DD-L0211-0	0	BD	L0211-0-EB02	4

D
C
B
A

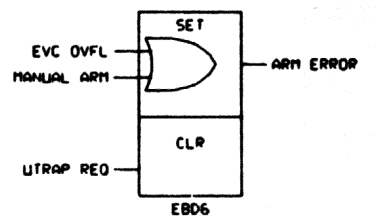
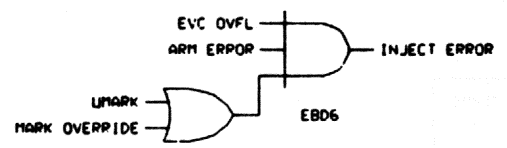
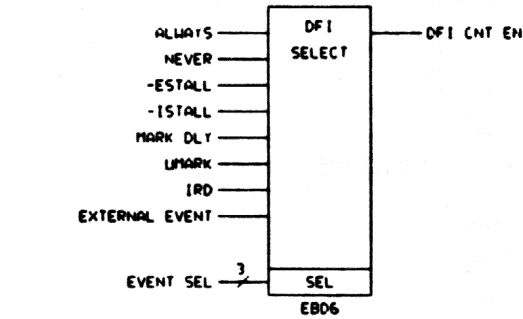
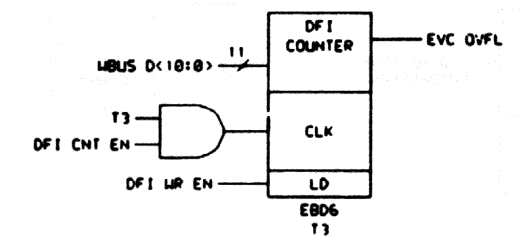
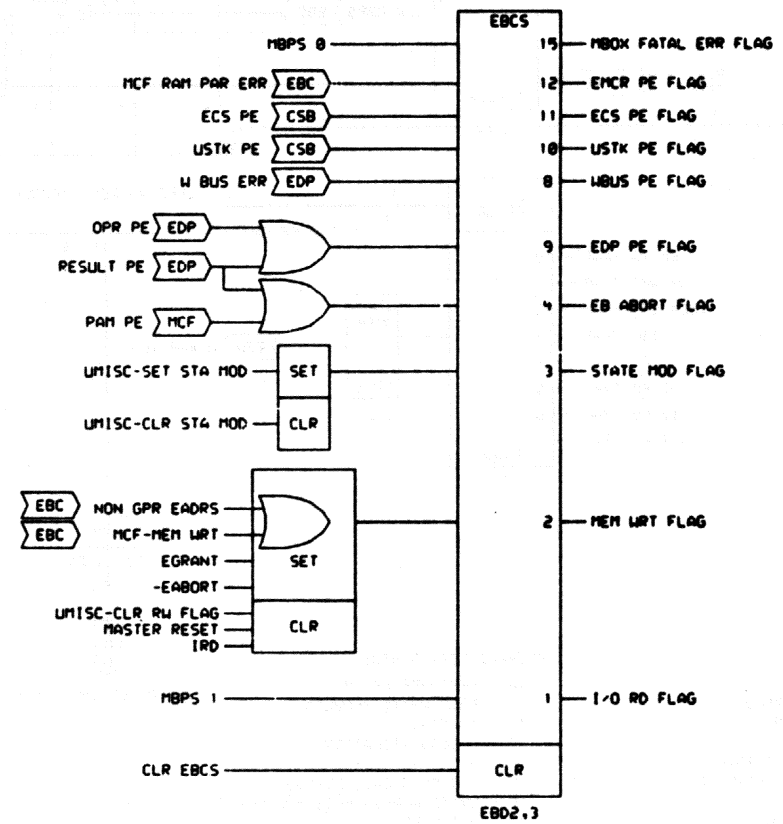
DFI REGISTER



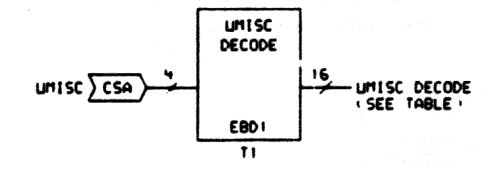
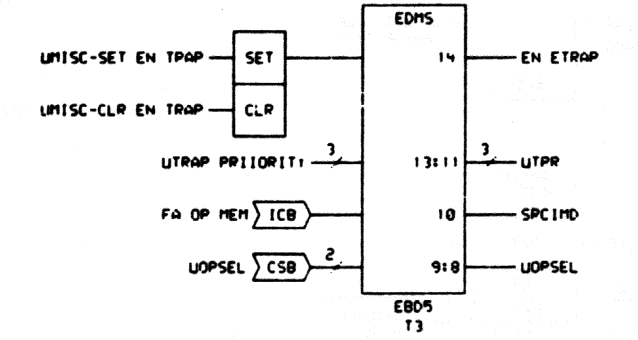
EDMC REGISTER



EBCS REGISTER



EDMS REGISTER



UMISC DECODE TABLE

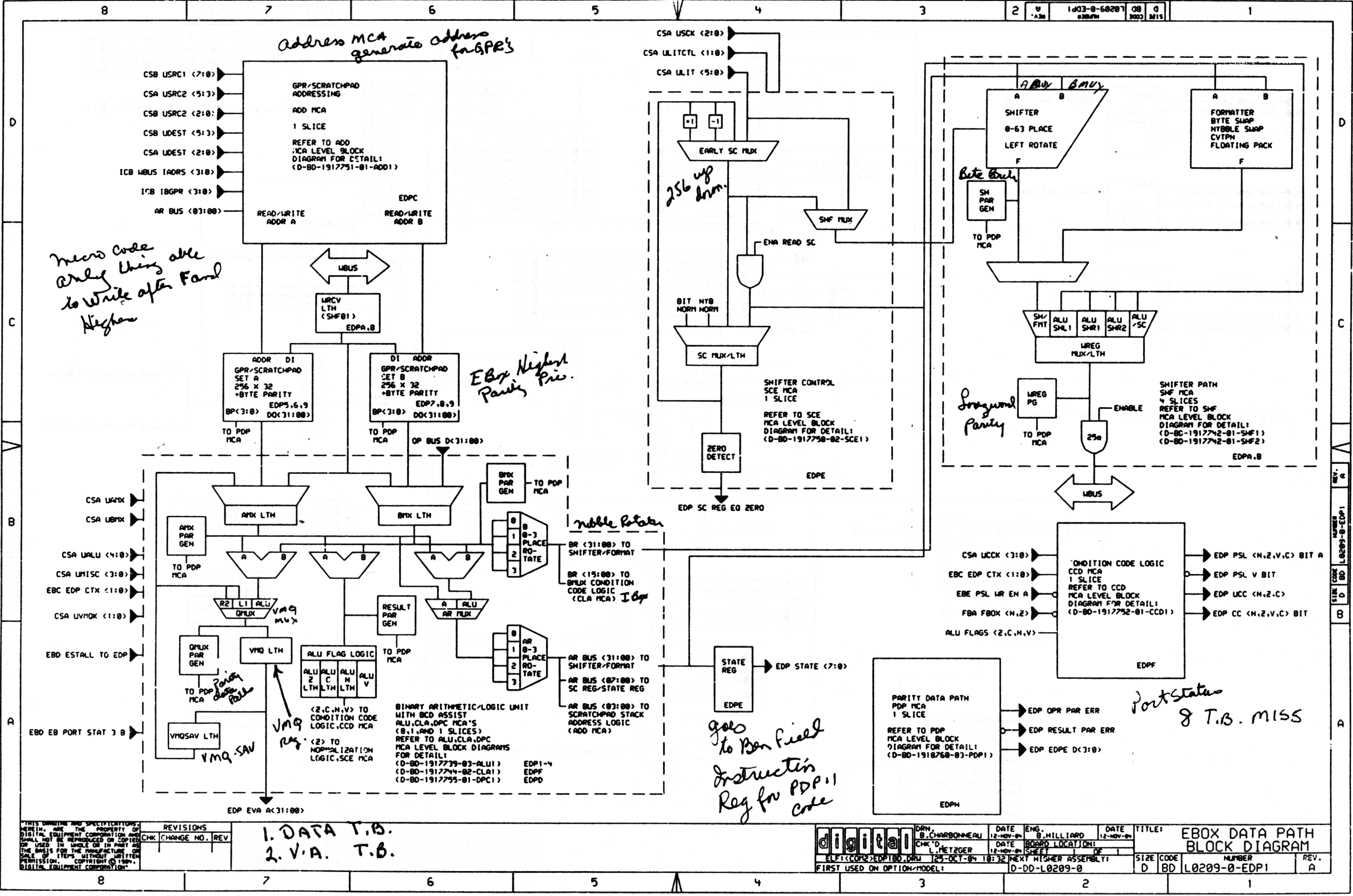
- 1 - UMISC-CLR RW FLAG
- 2 - UMISC-SET FPD (TO EBE)
- 3 - UMISC-CLR FPD (TO EBE)
- 4 - UMISC-SET EN TRAP
- 5 - UMISC-CLR EN TRAP
- 6 - UMISC-SET STA MOD
- 7 - UMISC-CLR STA MOD
- 8 - UMISC-IBOX SYNC (TO IBOX)
- C - UMISC-CHK OVFL
- D - UMISC-UNWIND RLOG (TO IBOX)
- E - UMISC-ENA FOPK
- F - UMISC-DIAG PESET

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REVISIONS		
CHK	CHANGE NO.	REV

digital	DPN	C. CAIAZZI	DATE	25-OCT-84	ENG.	M. EVANS	DATE	26-OCT-84	TITLE:	EBD REGISTERS
	CHK'D	L. METZGER	DATE	25-OCT-84	BOARDS LOCATION:		SHEET	1 OF 1	SIZE	CODE
ELF: CONT EBD3, EBD4, EBD5, EBD6		DATE	25-OCT-84	08:47	NEXT HIGHER ASSEMBLY:	D-DD-L0211-0	SIZE	CODE	NUMBER	REV.
FIRST USED ON OPTION MODEL:		D-DD-L0211-0		D		BC	L0211-0-EBD3	H		

REV. 4
NUMBER
L0211-0-EBD3
D
BC



*Micro Code
only thing able
to write after Ford
Highway*

*Address MCA
generate address
for GPR's*

*EBox Highest
Priority*

Nibble Rotate

*goes
to Ben Field
Instruction
Reg for PDP-11
code*

*Port Status
8 T.B. MISS*

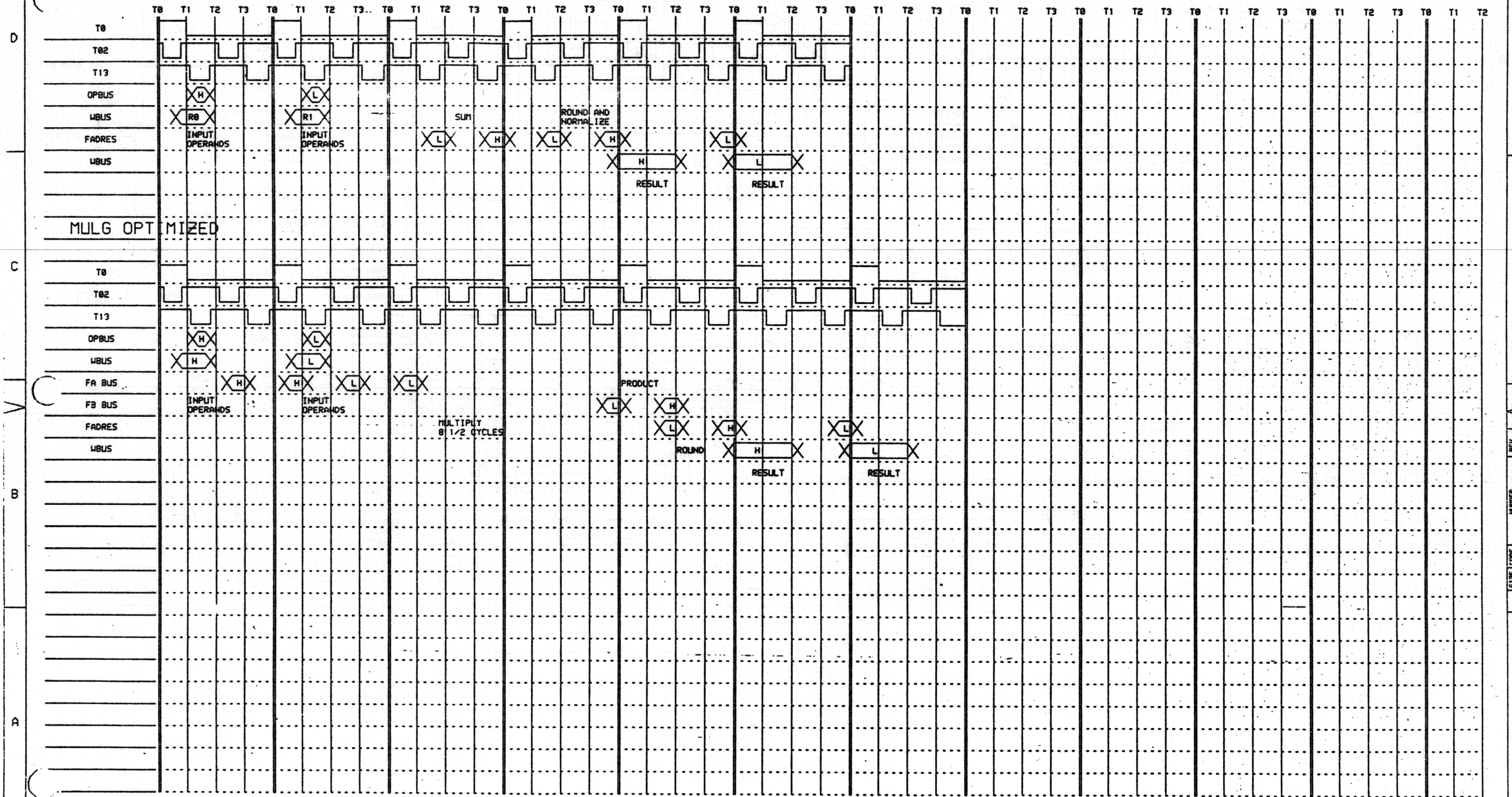
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REVISIONS
CHK CHANGE NO. REV
1. DATA T.B.
2. V.A. T.B.

digital	DRAWN	B. CHARBONNEAU	DATE	12-NOV-80	ENG.	B. HILLIARD	DATE	12-NOV-80	TITLE:	EBOX DATA PATH BLOCK DIAGRAM
	CHK'D	L. METZGER	DATE	12-NOV-80	BOARD LOCATION:		OF		SIZE CODE	D BD
	ELP:CC02:EDP1:BD		125-OCT-84	10:32	NEXT HIGHER ASSEMBLY:				NUMBER	L0209-0-EDP1
	FIRST USED ON OPTION/MODEL:								REV.	A

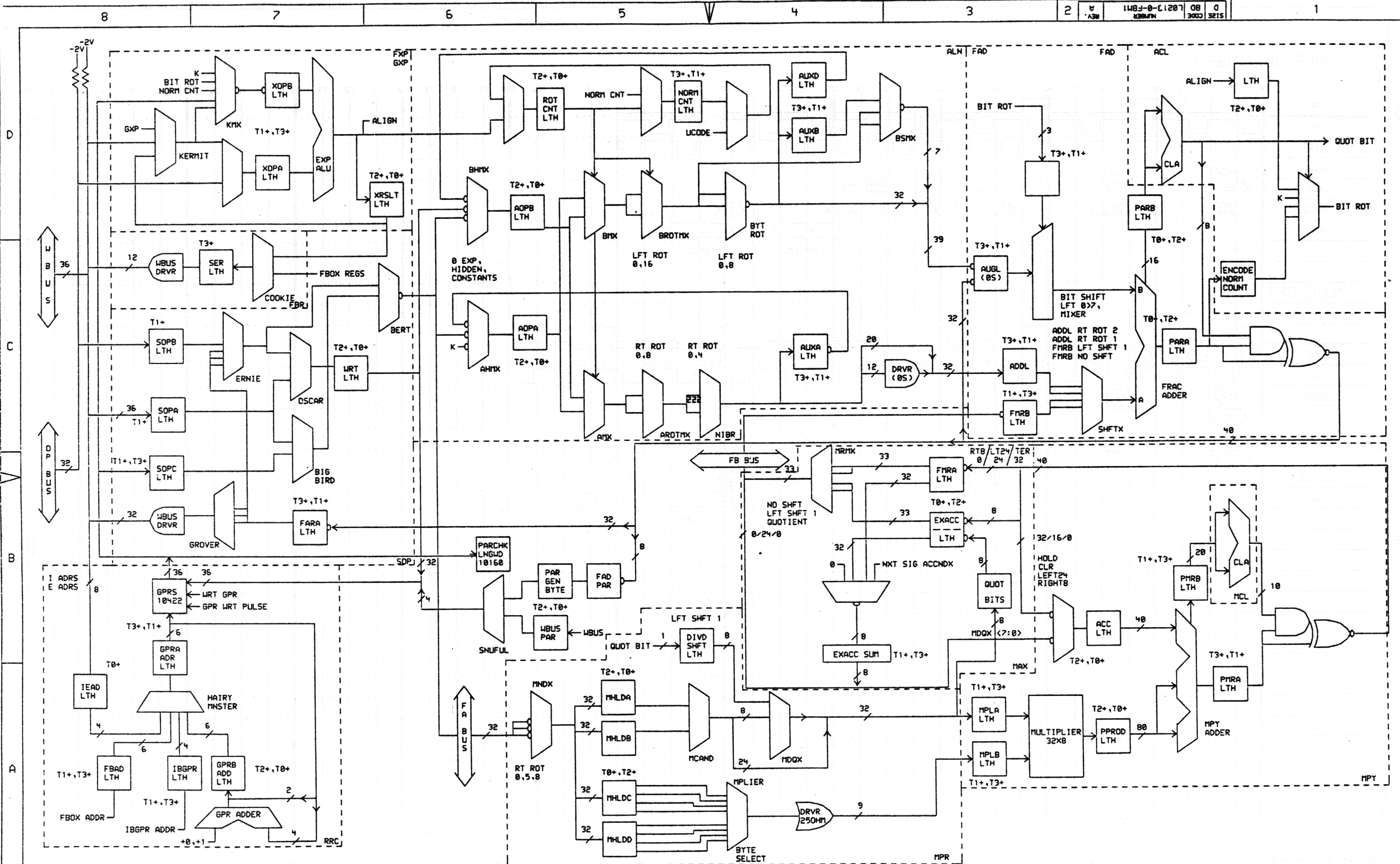
ADDG OPTIMIZED

MULG OPTIMIZED



REVISIONS	
CHK	CHANGE NO. REV

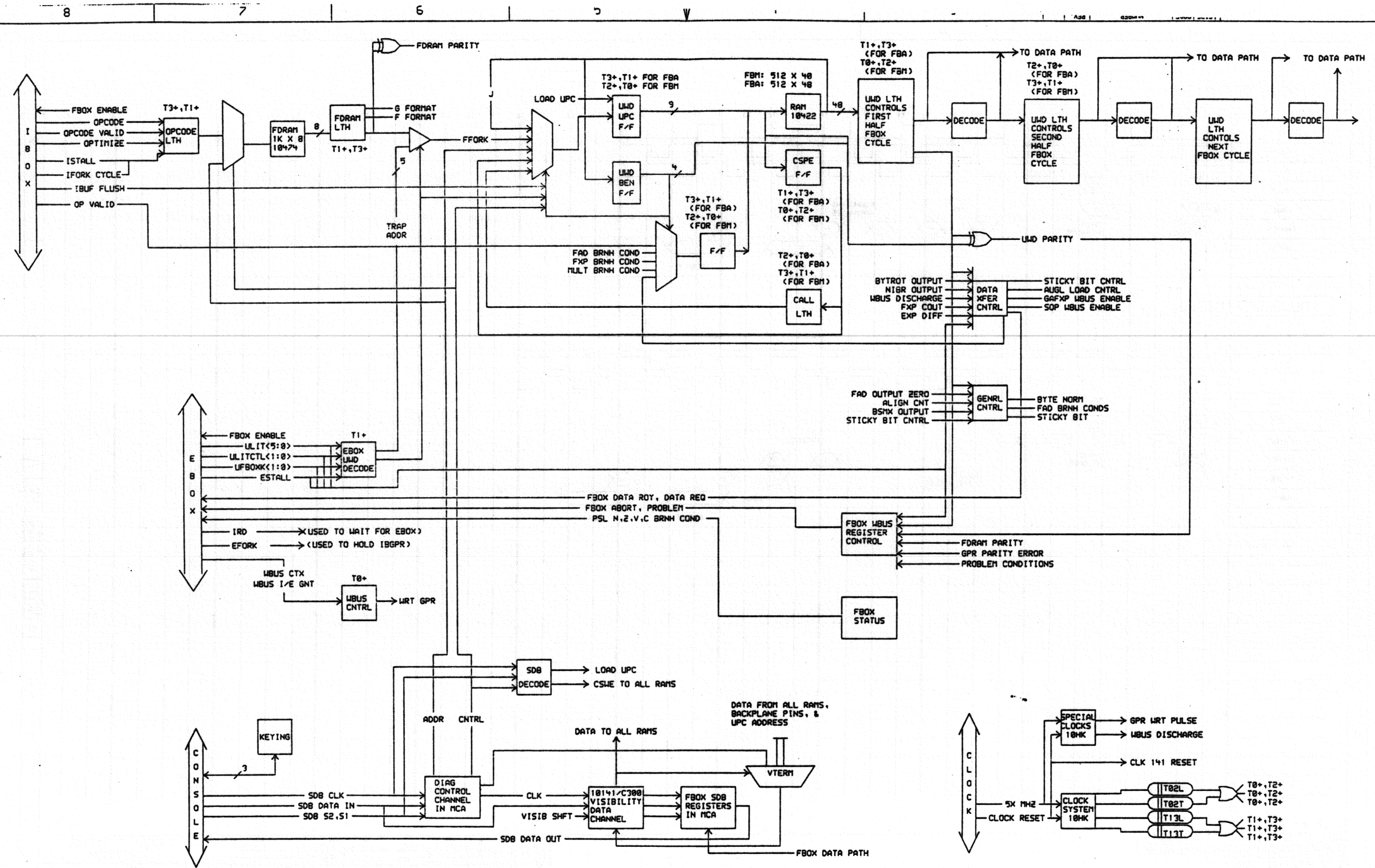
DRN C. CAIAZZI	DATE 21-SEP-84	ENG. B. GRUNDMANN	DATE 21-SEP-84	TITLE FBOX TIMING DIAGRAM
CHK'D L. METZGER	DATE 21-SEP-84	BOARD LOCATION SHEET	OF	
VENFIG: (FBAE_S01)FBOX-TIMING.DRW/20-SEP-84 08:25		NEXT HIGHER ASSEMBLY: D-DD-L0212-0		SIZE CODE D TD
FIRST USED ON OPTION/MODEL:				NUMBER L0212-0-FBA1
				REV. A



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REV.	DESCRIPTION
1	INITIAL RELEASE
2	REVISIONS
3	CHK CHANGE NO. 1 REV

digital	DRN. J. SMITH	DATE 24-OCT-84	ENG. B. GRUNDMANN	DATE 24-OCT-84	TITLE: FBOX DATA BLOCK DIAGRAM
	CHK'D L. MEZTGER	DATE 24-OCT-84	DATE BOARD LOCATION:		
	VENF02: (FBOX) SBX F01 B0 DRW 120 SEP-84	08:17	INEXT HIGHER ASSEMBLY:	SIZE CODE D	NUMBER L0213-0-F3M1
	FIRST USED ON OPTION MODEL: D-DD-L0213-0			REV. A	



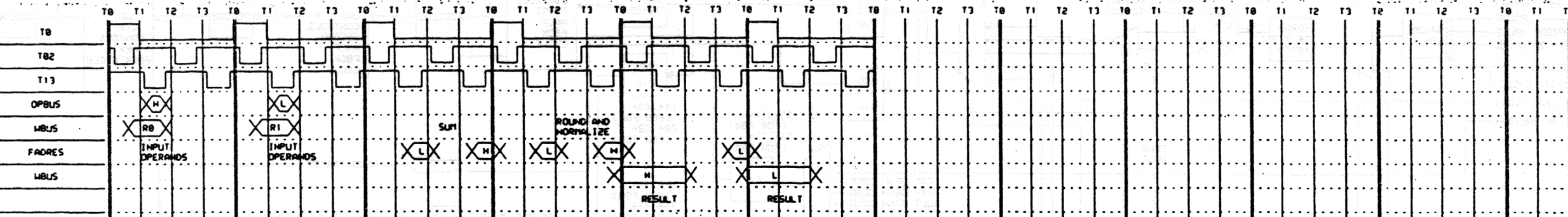
D
 C
 REV. A
 SIZE CODE NUMBER REV. A
 D BD L0213-0-FBM2
 D
 D
 TITLE: FBOX CONTROL BLOCK DIAGRAM
 DATE: 24-OCT-84
 ENG.: B. GRUNDMANN
 DATE: 24-OCT-84
 DRN.: J. SMITH
 DATE: 24-OCT-84
 CHK'D.: L. METZGER
 DATE: 24-OCT-84
 SHEET: 1 OF 1
 VENFG2: (FBOX.SBM) FBM20.DRW 120-SEP-84 08:19 NEXT HIGHER ASSEMBLY:
 FIRST USED ON OPTION/MODEL: 1D-00-L0213-0
 SIZE CODE NUMBER REV. A
 D BD L0213-0-FBM2 A

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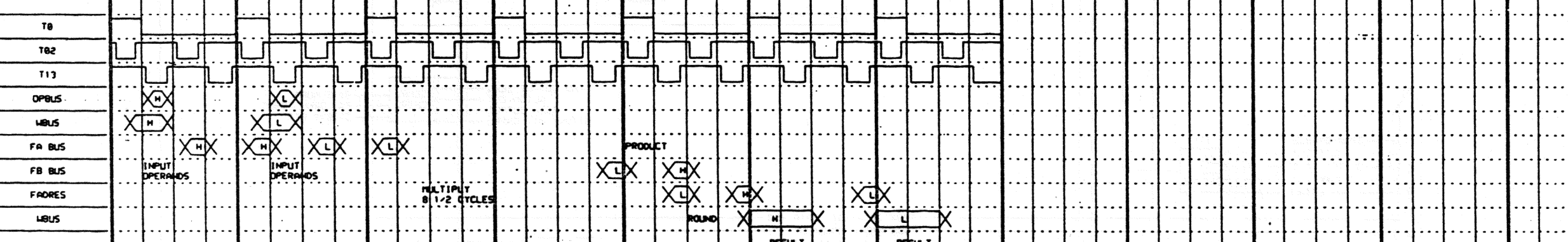
REVISIONS	
CHK	CHANGE NO. REV

8 7 6 5 4 3 2 1

ADDG OPTIMIZED



MULG OPTIMIZED

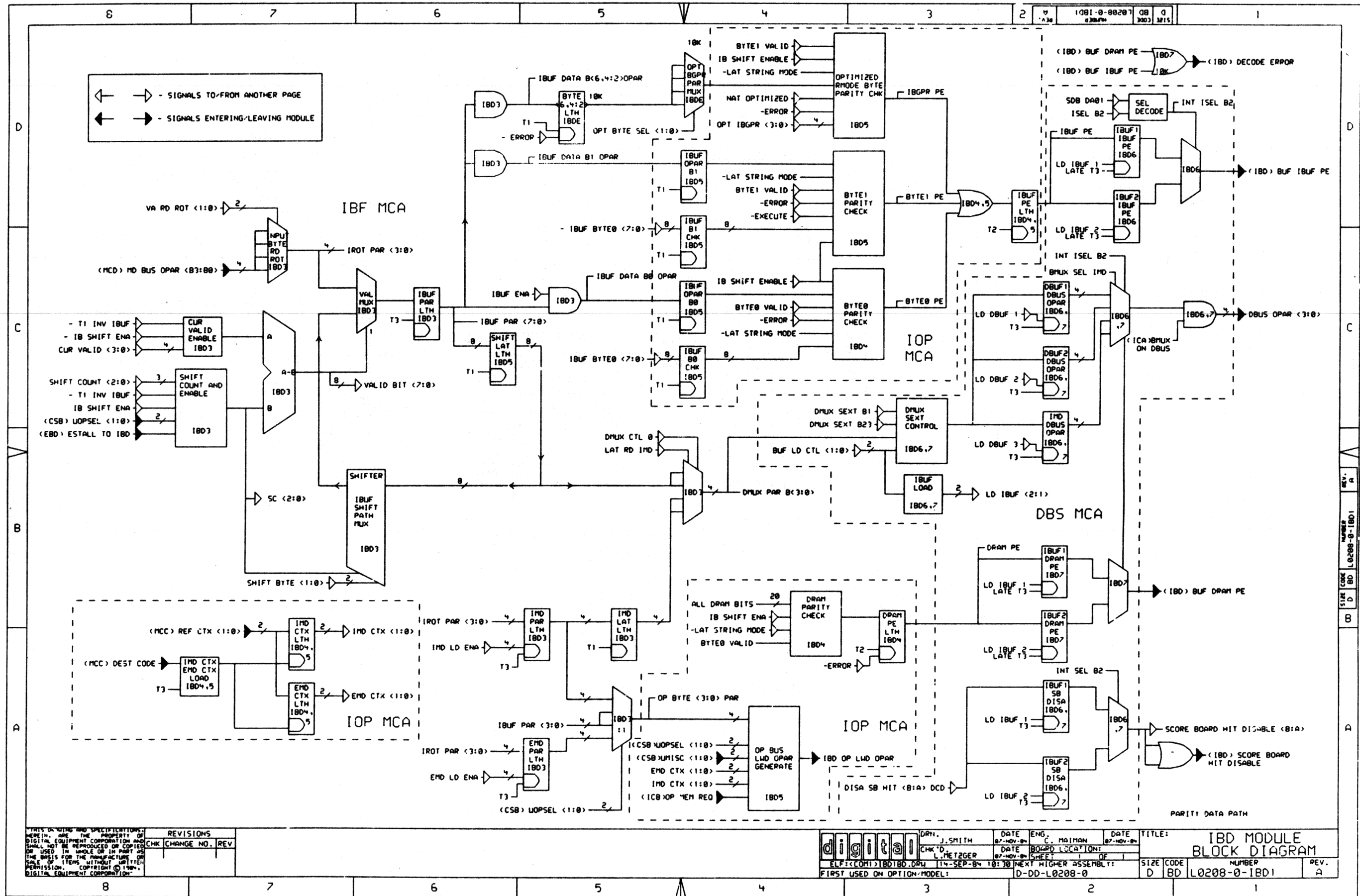


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REV.	DATE	BY	CHK	CHANGE NO.
1				

	DRN	C. CAIAZZI	DATE	ENG.	A. GRUNDORF	DATE	TITLE	FBOX TIMING DIAGRAM		
	CHK'D	L. PETZGER	DATE	ISSUED	LOCATION					
ELECTRONICALLY DERIVED FROM NEXT HIGHER ASSEMBLY							SIZE	CODE	NUMBER	REV.
FIRST USED ON OPT114 MODEL							D	TD	L0213-0-FB01	A

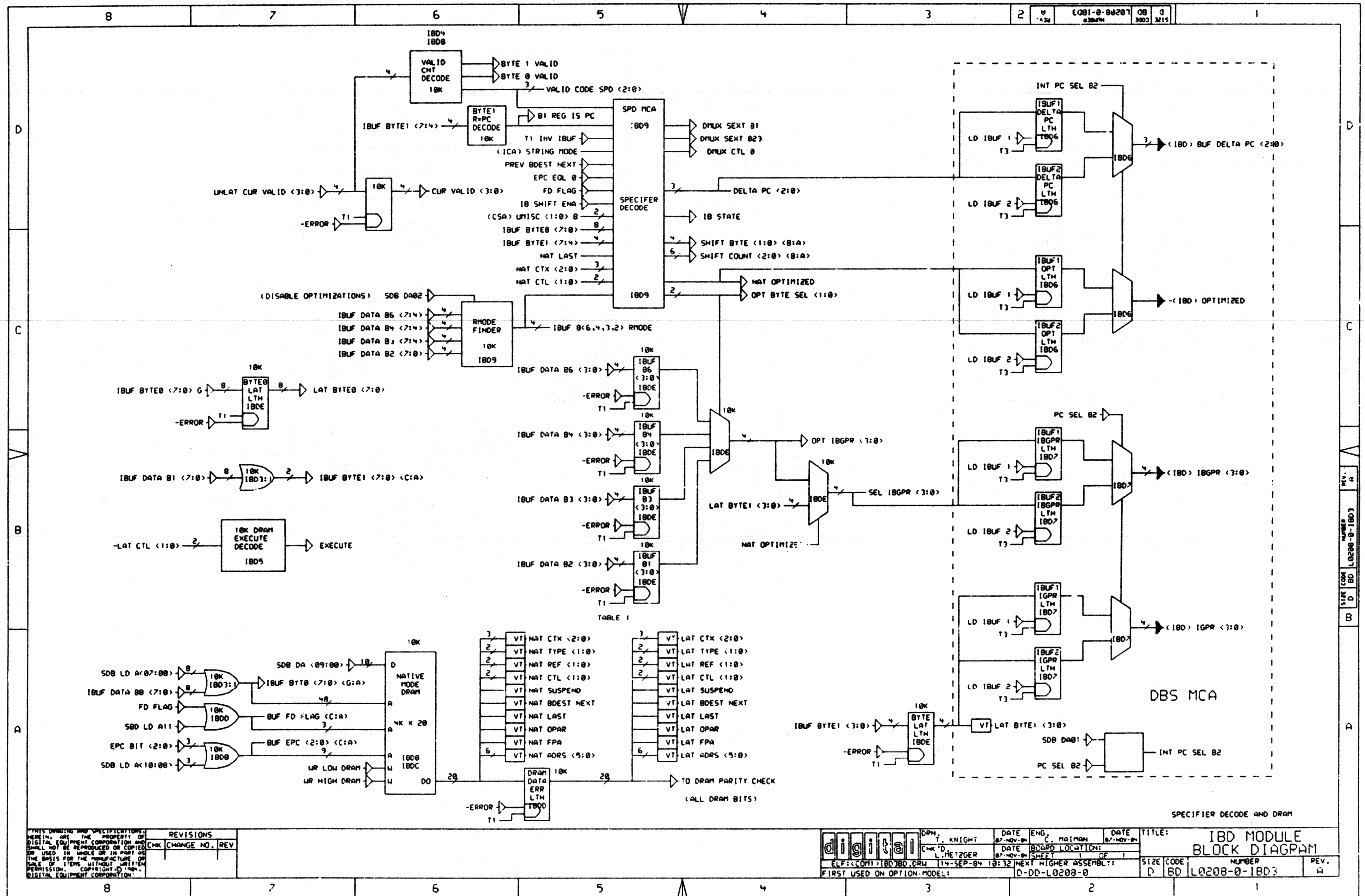
FILE USE ID L0213-0-FB01



REV.	CHG.	NO.	REV.

DATE	ENG.	DATE	REV.
07-NOV-84	C. MAIMAN	07-NOV-84	
14-SEP-84	L. METZGER		

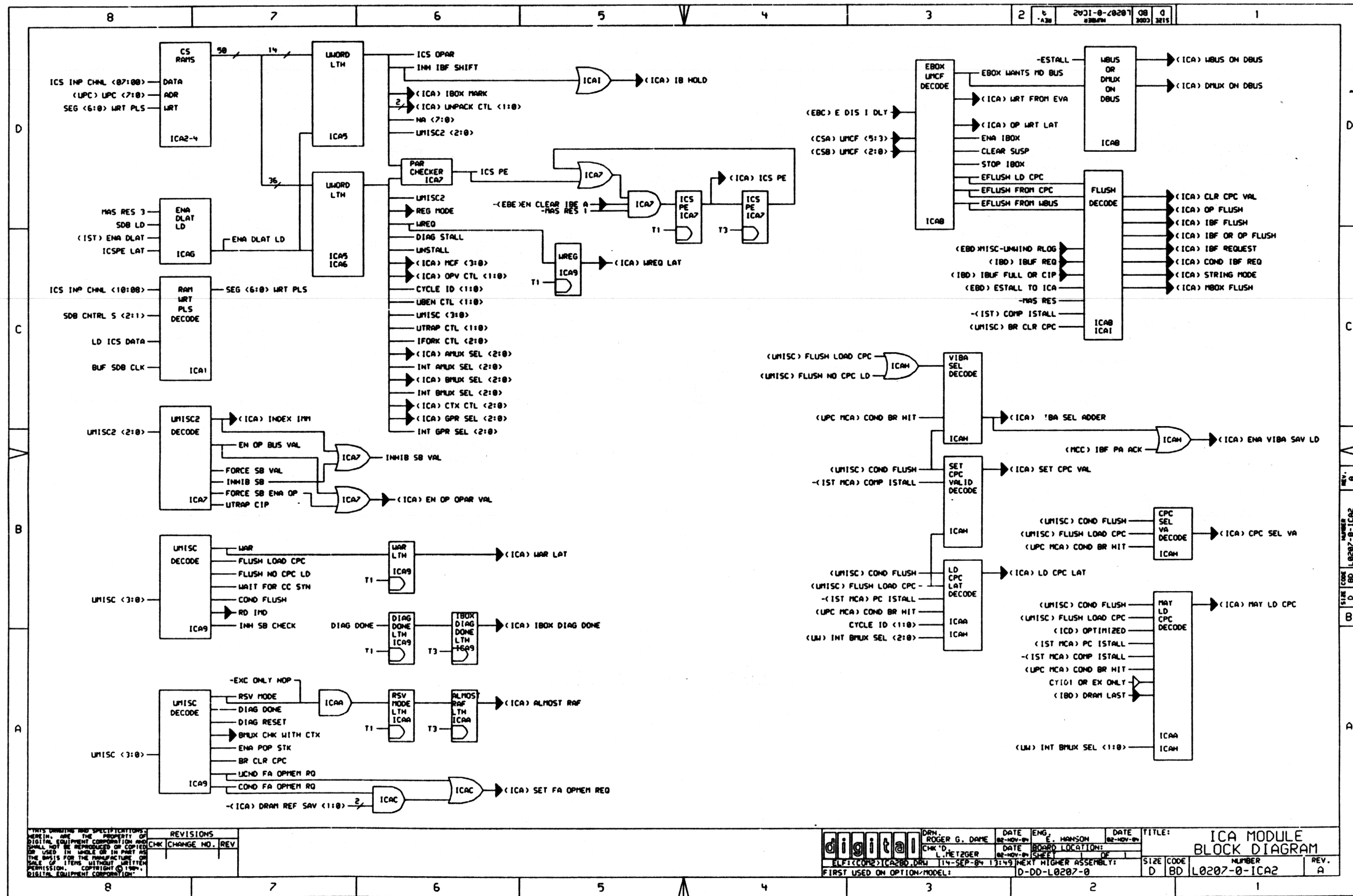
digital		DRN. J. SMITH		DATE 07-NOV-84		ENG. C. MAIMAN		DATE 07-NOV-84		TITLE: IBD MODULE BLOCK DIAGRAM	
ELF: (CONT) IBD10.DRW		CHK'D L. METZGER		DATE 14-SEP-84		BOARD LOCATION: 10:30		NEXT HIGHER ASSEMBLY: D-DD-L0208-0		SIZE CODE D BD	
FIRST USED ON OPTION MODEL:										NUMBER L0208-0-IBD1	
										REV. A	



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REVISIONS	CHANGE NO.	REV

digital DPN: T. KNIGHT DATE: 07-NOV-84 ENG: C. MAJMAN DATE: 07-NOV-84
 CHK'D: L. METZGER DATE: 07-NOV-84 BOARD LOCATION: 1 OF 1
 TITLE: IBD MODULE BLOCK DIAGRAM
 FIRST USED ON OPTION MODEL: D-DD-L0208-0 SIZE: D BD NUMBER: L0208-0-IBD3 REV: A

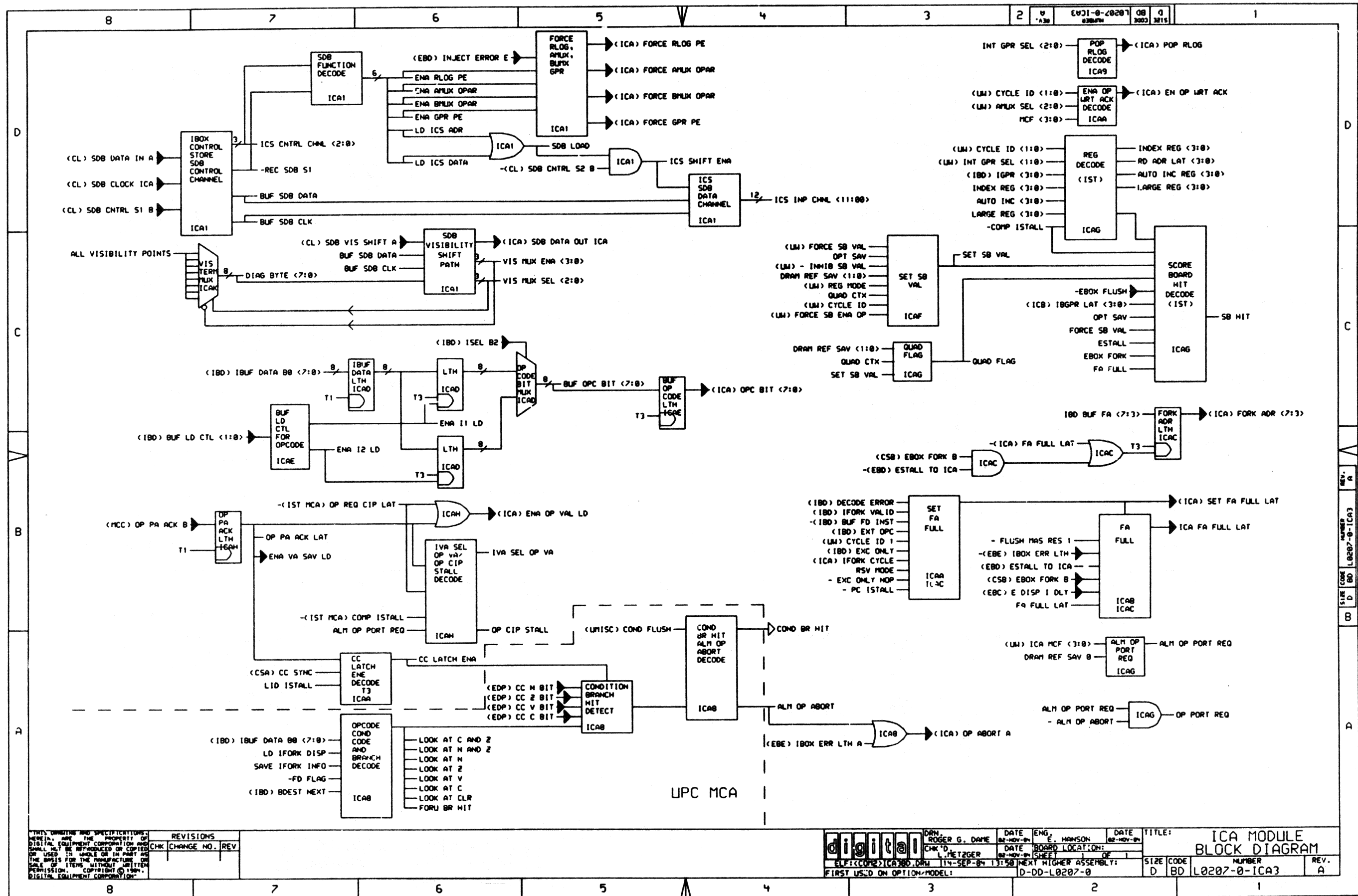


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REV.	CHG.	NO.	REV.

digital	DRN: ROGER G. DAME	DATE: 02-NOV-84	ENG: E. HANSON	DATE: 02-NOV-84	TITLE: ICA MODULE BLOCK DIAGRAM
CHK'D: L. HETZGER	DATE: 02-NOV-84	BOARD LOCATION: 1	DE: 1	SIZE: D	CODE: BD
FIRST USED ON OPTION/MODEL: L14-SEP-84 13:49	NEXT HIGHER ASSEMBLY: D-DD-L0207-0	NUMBER: L0207-0-ICA2	REV.:	A	

REV. A
 SIZE CODE NUMBER
 D BD L0207-0-ICA2
 A



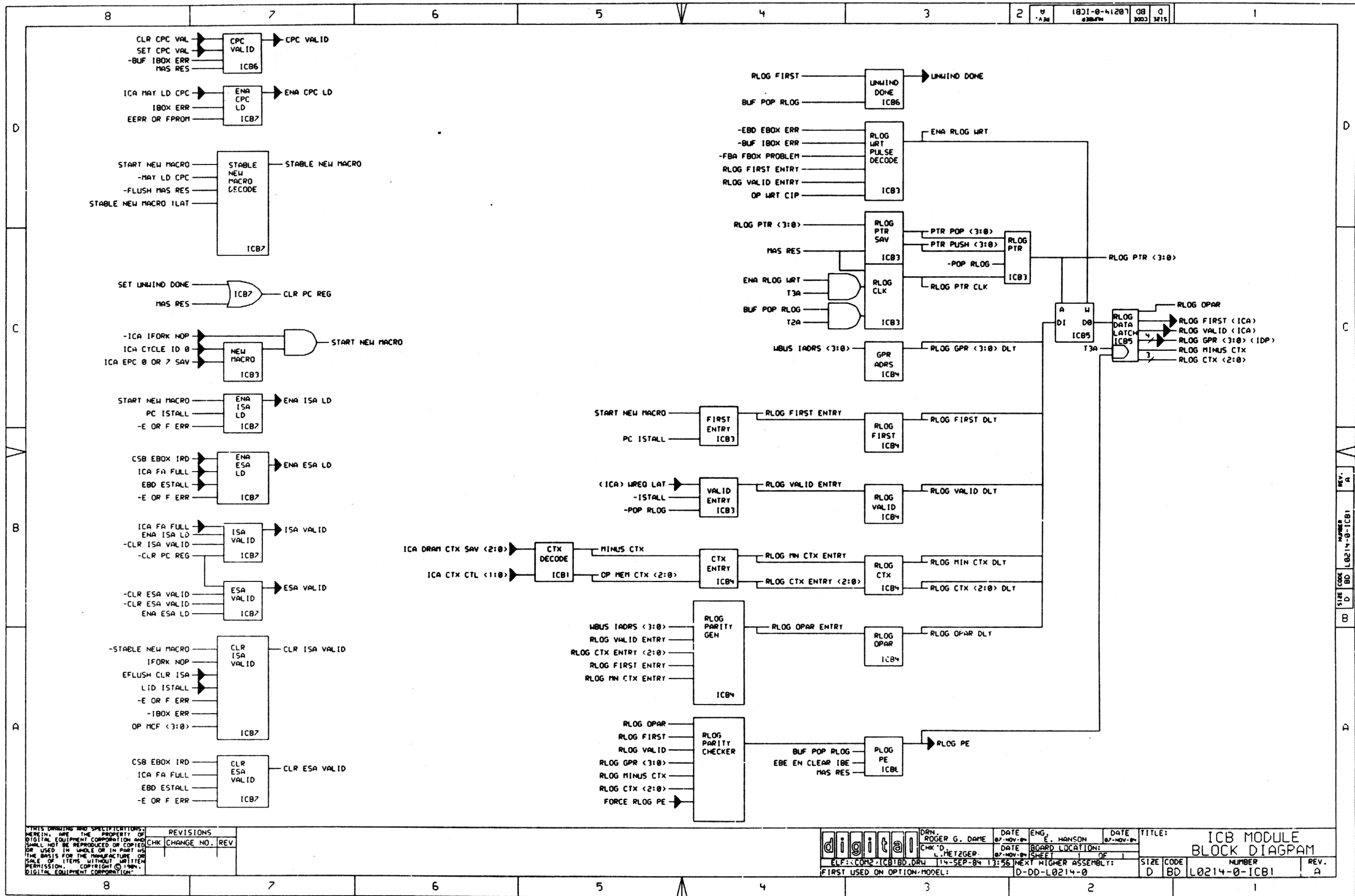
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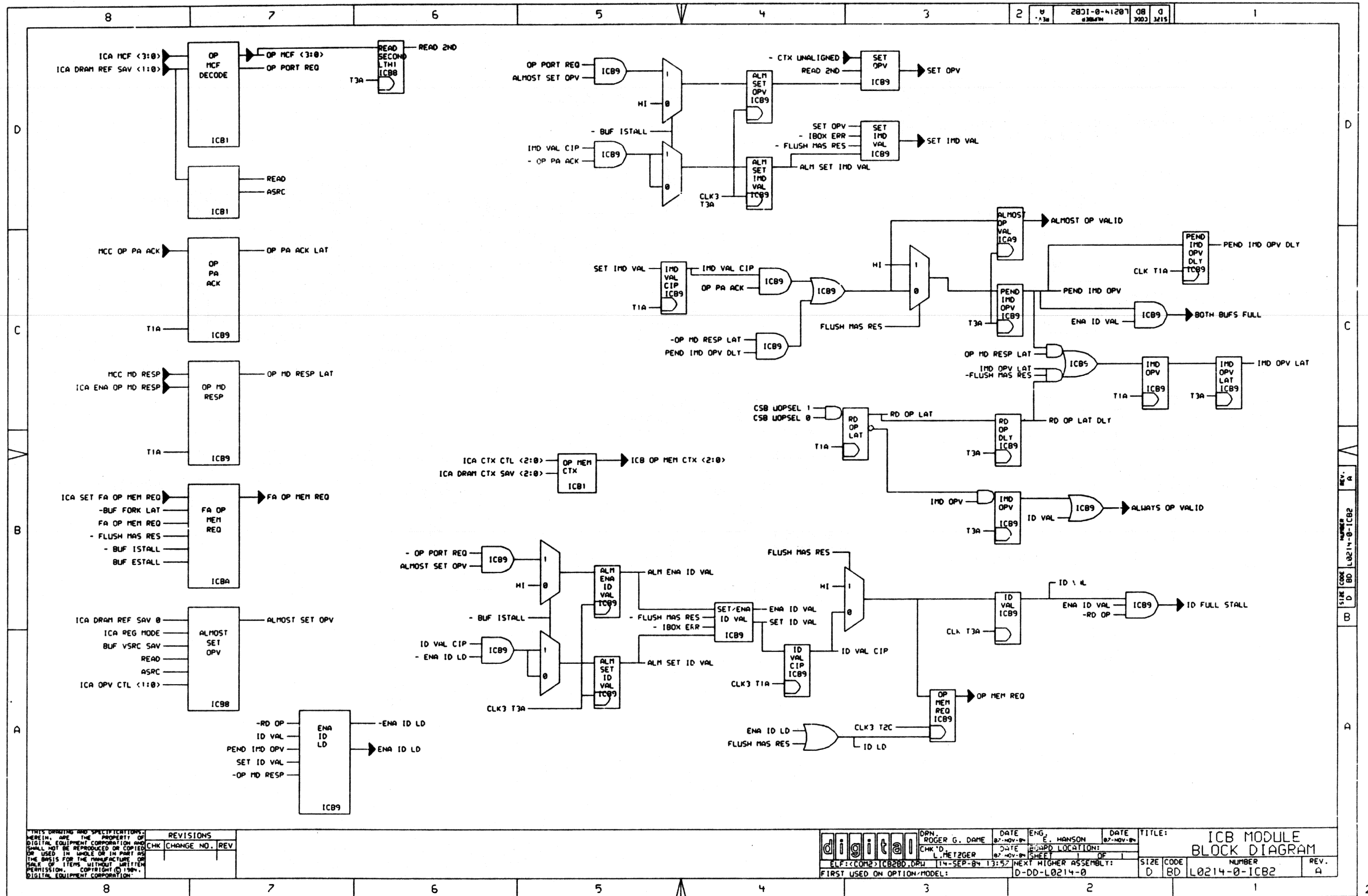
REV.	CHG	NO.	REV

REV.	CHG	NO.	REV

digital	DRW. ROGER G. DAINE	DATE 02-NOV-84	ENG. E. HANSON	DATE 02-NOV-84	TITLE: ICA MODULE BLOCK DIAGRAM
ELF(C002) (CA30) DRW	CHK'D L. METZGER	DATE 02-NOV-84	BOARD LOCATION:	OF	SIZE CODE D BD
FIRST USED ON OPTION MODEL:	114-SEP-84 13:50	NEXT HIGHER ASSEMBLY:	D-DD-L0207-0	NUMBER L0207-0-ICA3	REV. A

2250



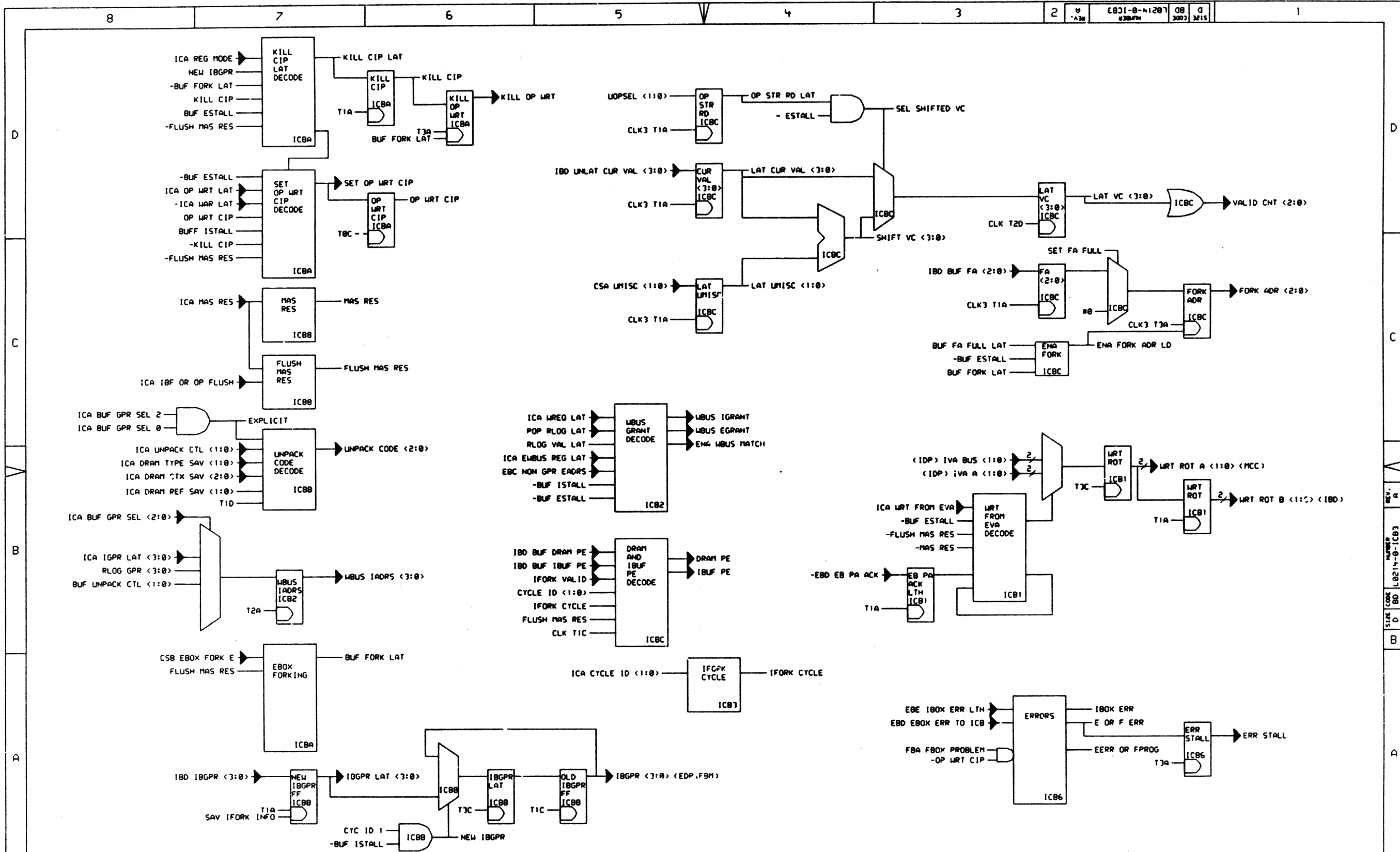


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REV.	NO.	DATE	BY	CHK'D	DATE	BY	CHK'D	DATE	BY
1	1	07-NOV-84	E. MANSON	L. METZGER	07-NOV-84	L. METZGER	07-NOV-84		

REV.	NO.	DATE	BY	CHK'D	DATE	BY	CHK'D	DATE	BY
1	1	07-NOV-84	E. MANSON	L. METZGER	07-NOV-84	L. METZGER	07-NOV-84		

DRN. ROGER G. DAME
 DATE 07-NOV-84
 ENG. E. MANSON
 DATE 07-NOV-84
 TITLE: ICB MODULE BLOCK DIAGRAM
 BOARD LOCATION:
 DATE 07-NOV-84
 SHEET 07-NOV-84
 SIZE CODE D
 NUMBER L0214-0-ICB2
 REV. A
 FIRST USED ON OPTION/MODEL: D-DD-L0214-0

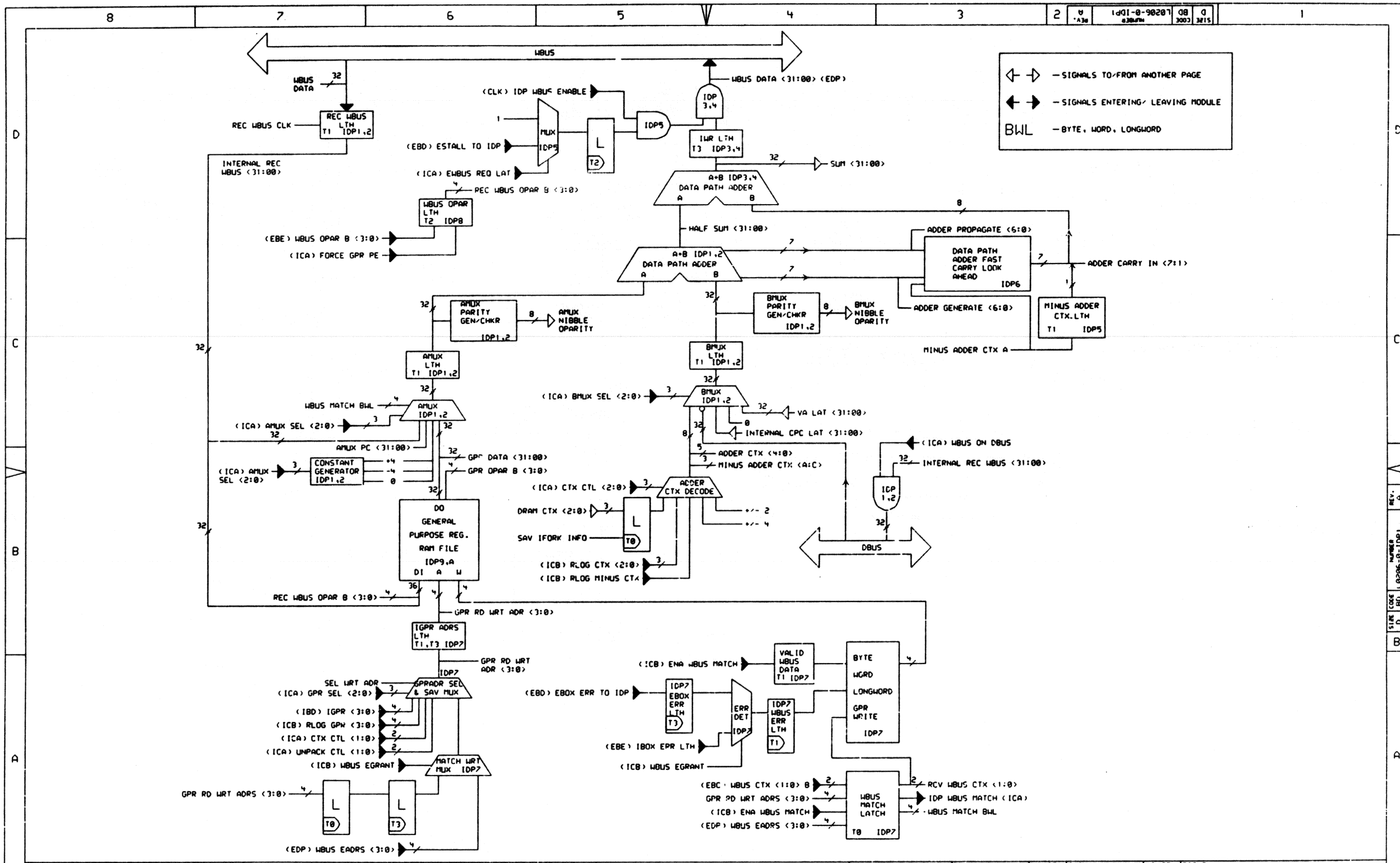


REVISIONS	
CHK	CHANGE NO. REV

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digital	DRN. ROGER S. DAME	DATE 07-NOV-84	ENG. E. HANSON	DATE 07-NOV-84	TITLE: ICB MODULE BLOCK DIAGRAM
	CHK'D L. METZGER	DATE 07-NOV-84	BOARD LOCATION:	SHEET	
ELF: (COR2) ICB380.DRW 14-SEP-84 13:57 NEXT HIGHER ASSEMBLY:					SIZE CODE D
FIRST USED ON OPTION MODEL:					RD L0214-0-ICB3

REV. A
SIZE CODE D
BOARD L0214-0-ICB3

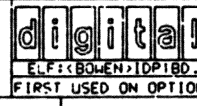


← → - SIGNALS TO/FROM ANOTHER PAGE
 ← → - SIGNALS ENTERING/ LEAVING MODULE
 BWL - BYTE, WORD, LONGWORD

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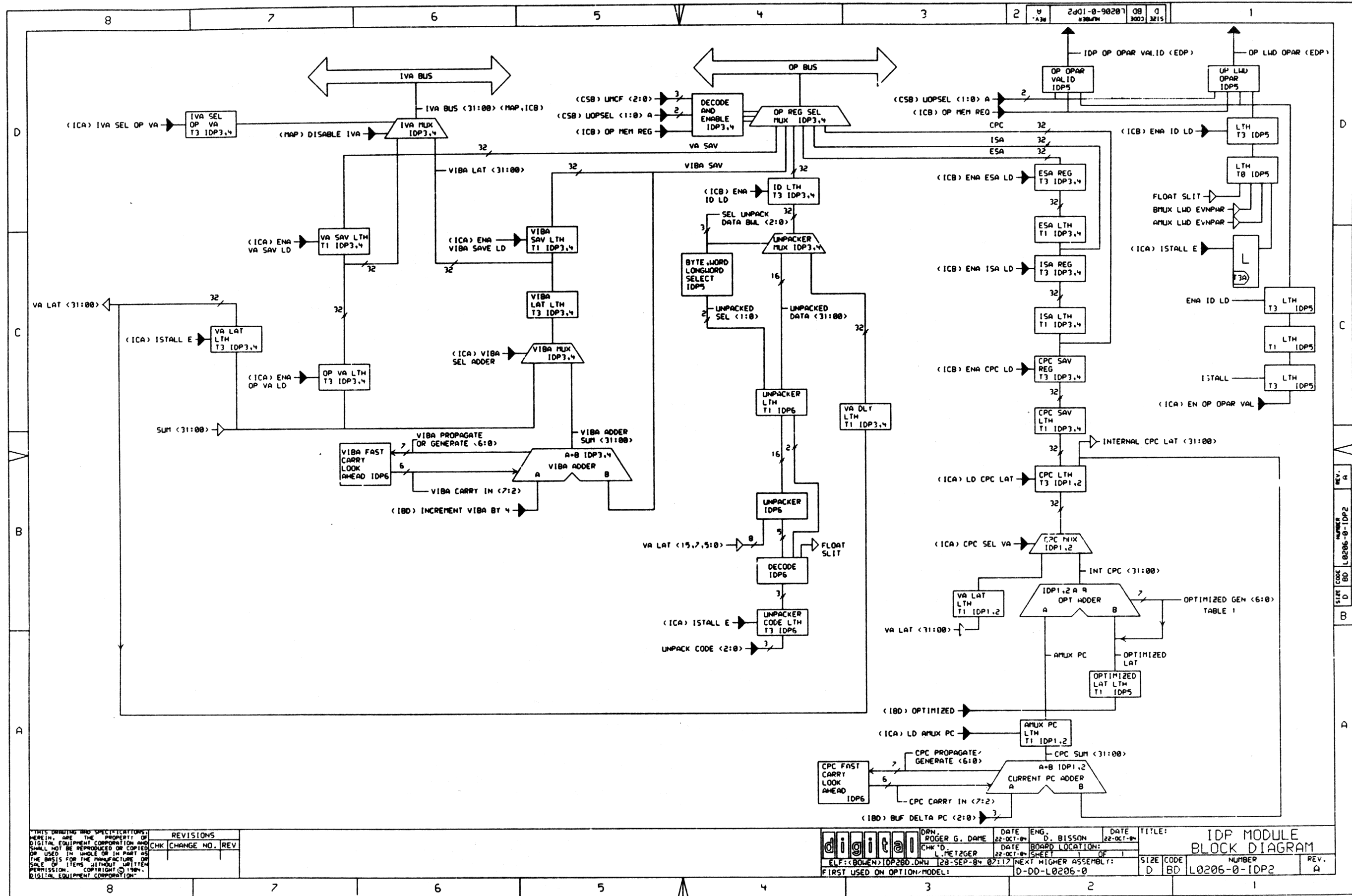
REVISIONS		
CHK	CHANGE NO.	REV

DATE	ENG.	DATE	TITLE:
22-01-84	O. BISSON	22-01-84	IDP MODULE
22-01-84	L. METZGER	22-01-84	BLOCK DIAGRAM



DRN. POGER G. DAME
 DATE 22-01-84
 CHK'D L. METZGER
 DATE 22-01-84
 FILE: BOWEN>IDP180.DRW 128-SEP-84 07:15
 FIRST USED ON OPTION MODEL: D-DD-L0206-0

SIZE	CODE	NUMBER	REV.
D	BD	L0206-0-IDP1	A

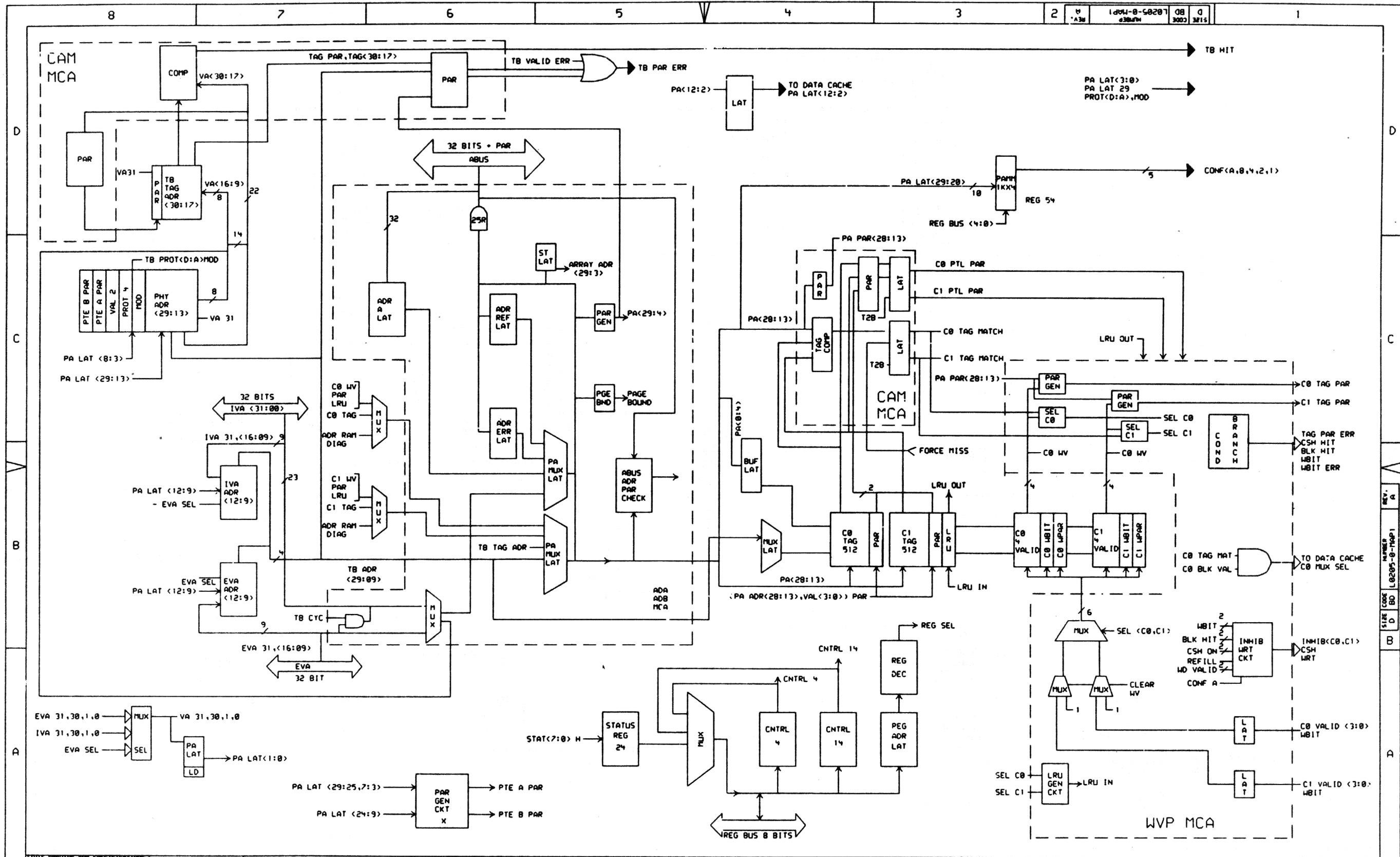


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REVISIONS	
CHK	CHANGE NO. REV

digital	DRN	ROGER G. DAME	DATE	22-OCT-84	ENG.	D. BISSON	DATE	22-OCT-84	TITLE:	IDP MODULE
	CHK'D	L. METZGER	DATE	22-OCT-84	BOARD LOCATION:		SHEET	OF	1	
E.P.: (BOLLEN) IDP280.DRW		28-SEP-84	02:17	NEXT HIGHER ASSEMBLY:						
FIRST USED ON OPTION/MODEL:		D-DD-L0206-0		SIZE CODE	D BD	NUMBER	L0206-0-IDP2	REV.	A	

2256



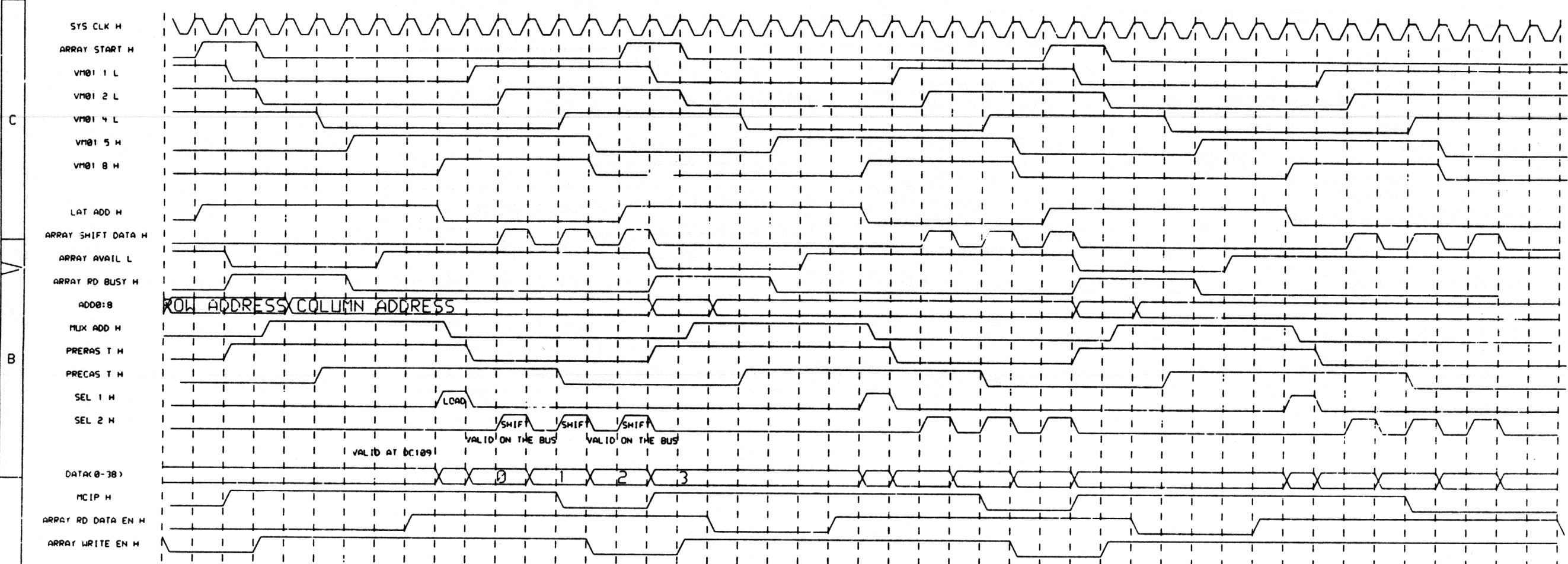
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REV	CHG	NO.	REV

DATE	ENG.	DATE	TITLE:
28-NOV-84	B. BRUCKERT	28-NOV-84	ADDRESS MODULE BLOCK DIAG
28-NOV-84	L. METZGER	28-NOV-84	

SIZE	CODE	NUMBER	REV.
D	BD	L0205-0-MAP1	A

ARRAY TIMING READ CYCLE

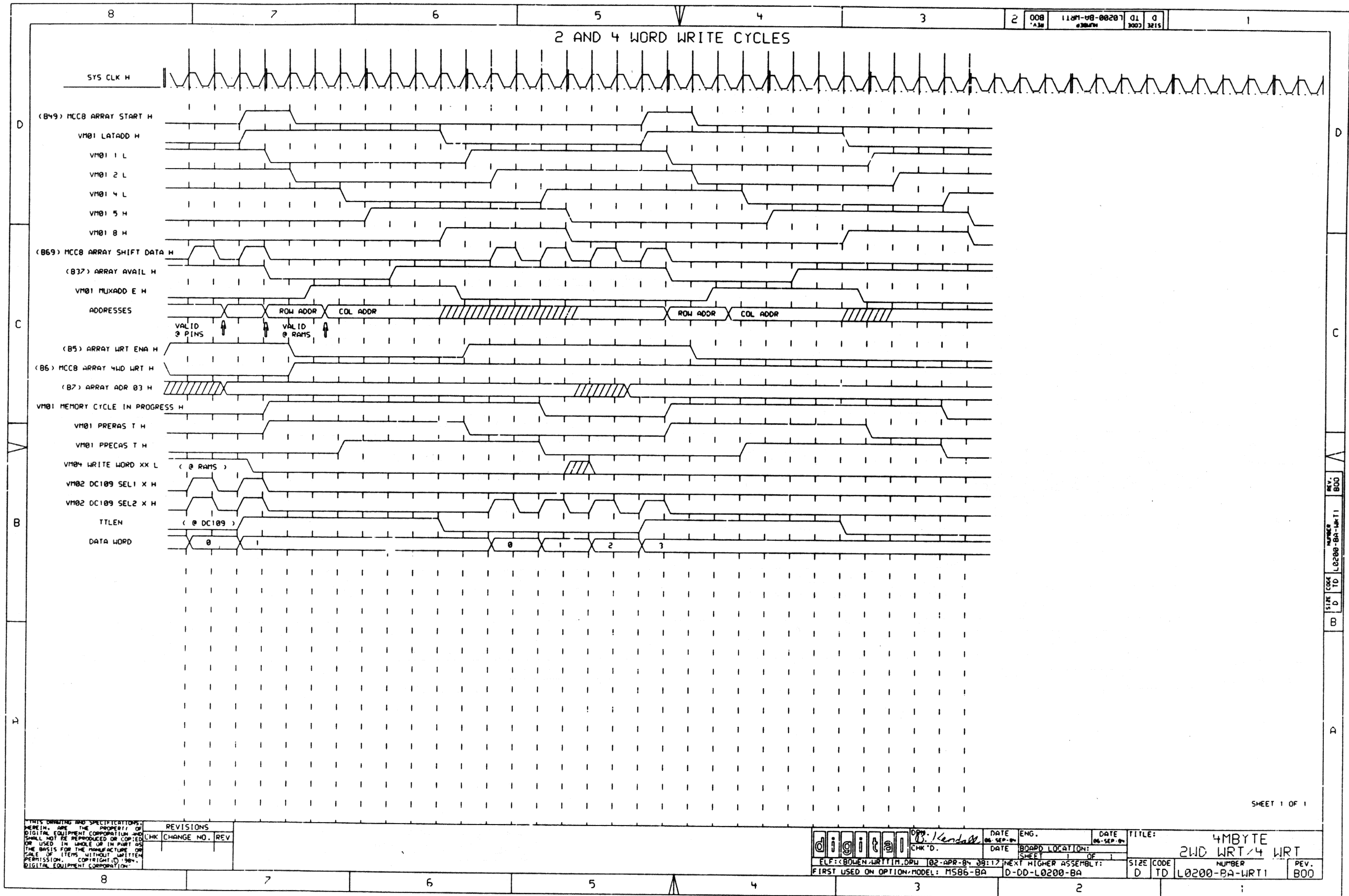


SHEET 1 OF 1

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REVISIONS		
CHK	CHANGE NO.	REV

digital	DATE: 06-SEP-84	ENG.:	DATE: 06-SEP-84	TITLE: 4 MBYTE READ CYCLE
	CHK'D: <i>J. Lashby</i>	DATE: 02-APR-84	BOARDS LOCATION: 00-00-L0200-BA	NUMBER: 10200-BA-VT11
FIRST USED ON OPTION/MODEL: M565-BA		NEXT HIGHER ASSEMBLY: 0-00-L0200-BA		REV. B00



SHEET 1 OF 1

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REVISIONS	
CHK	CHANGE NO. REV

digital	DATE	ENG.	DATE	FILE:
	06-SEP-84	Kendall	06-SEP-84	4MBYTE
DATE	BOARD LOCATION:	SHEET 1 OF 1		
02-APR-84	D-00-L0200-BA	2WD WRT/4 WRT		
FIRST USED ON OPTION/MODEL: MS86-BA	NEXT HIGHER ASSEMBLY:	SIZE CODE	NUMBER	REV.
D-00-L0200-BA	D-00-L0200-BA	D TD	L0200-BA-WRT1	B00