Technical Manual

Addendum for Models PC100-A, PC100-B, and Rainbow 100+

digital™

EK-RB100-TM-001

Technical Manual

Addendum for Models PC100-A, PC100-B, and Rainbow 100+

digital equipment corporation

First Edition, December 1984

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This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna.
- Move the computer away from the receiver.
- Plug the computer into a different outlet so that computer and receiver are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful.

How to Identify and Resolve Radio-TV Interference Problems

This booklet is available from the US Government Printing Office, Washington, DC 20402, Stock No. 004-000-00345-4.

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PREFACE

This addendum contains information for service engineers, technicians, or other interested persons who need to know how the Rainbow™ PC100-B and Rainbow™ 100+ computers are designed and operate.

Included are explanations of the features, capabilities, system architecture, and technical characteristics as well as general reference data. The addendum also describes the differences between the Rainbow PC100-A and Rainbow PC100-B computers. The addendum is divided into the following chapters and appendixes.

- **Chapter 1, Introduction**, contains a general description of the PC100-B system unit and describes the differences between the Rainbow PC100-A and PC100-B computers.

- **Chapter 2, Operating Information**, provides basic operator information, including using the keyboard and set-up modes for setting or changing the computer characteristics.

- **Chapter 3, PC100-B System Module Technical Description**, contains a technical description of the PC100-B system module.

- **Chapter 4, Winchester Hard Disk Controller**, provides a general, physical, and functional description of the Winchester hard disk controller as well as programming and interfaces information.

- **Chapter 5, Power Supply and Fan Assembly**, provides a physical, functional, and detailed circuit description of the H7842-D power supply.

- **Appendix A, Rainbow Computer Parts List**, contains a list of the user-replaceable parts for Rainbow computers.

- **Appendix B, Diagnostic Tests**, describes the internal ROM resident diagnostic and diskette resident diagnostic tests used to detect and isolate problems that may occur in the computer.

- **Appendix C, Character Generator ROM Codes**, contains a list of the hexadecimal codes used to display the characters of the ASCII, United Kingdom, Special Graphics, and DEC Multinational Character sets.

- **Appendix D, Glossary**, is a glossary of terms and abbreviations used in this addendum.

Many terms used in this addendum are written out the first time they appear followed by an abbreviation or mnemonic in parenthesis that is generally used thereafter. Numbers may be given in binary, octal, decimal, or hexadecimal (hex). The decimal form is used for numbers in general; the hexadecimal form for data and addresses. An H following a number indicates a hexadecimal number.

CHAPTER 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

There are three basic versions of the Rainbow personal computer; the Rainbow model PC100-A, the Rainbow model PC100-B, and the PC100-A with a Winchester upgrade kit. The PC100-B with a Winchester hard disk drive as standard equipment is called the Rainbow 100+. Each of these computers uses and 8088™ processor and Z80A® processor in a dual-processor system architecture that allows execution of 8-bit or 16-bit application programs using the CP/M®-86/80 or MS™-DOS operating system.

Each model of the Rainbow computer can store and access programs on a dual diskette drive and on a Winchester hard disk drive. The hard disk drive is standard on the Rainbow 100+ and can be added as an option to either the Rainbow model PC100-A or the model PC100-B.

The Rainbow computer comprises three basic units: the system unit, the monitor, and the keyboard. Figure 1-1 shows the Rainbow computer in two views, one showing the system unit positioned horizontally, and the other showing the system unit positioned vertically in the optional floor stand.

The same type of monitor and keyboard is used with either model of the computer. The VR201 monochrome monitor displays alphanumeric or graphics video information on a 12.7 × 20.3 cm (5 × 8 in) viewing area on a 30.5 cm (12 in) diagonal screen. A detailed description of the VR201 monitor is provided in the *Rainbow™ 100 Technical Manual* (EK-PC100-TM).

The LK201 keyboard is a low profile keyboard with 105 keys and is the user interface to the system. It detects keystrokes, encodes them and transmits the information to the system module. The keyboard can also receive instructions from the system unit. These instructions are used to change keyboard transmission characteristics and to control the keyboard indicators and beeper. A detailed technical description of the keyboard is provided in the *Rainbow™ 100 Technical Manual* (EK-PC100-TM).

The BA25-C small system unit enclosure houses the system module, option modules, and other assemblies of the Rainbow models PC100-B and 100+. The Rainbow model PC100-A uses the BA25-B small system unit enclosure.

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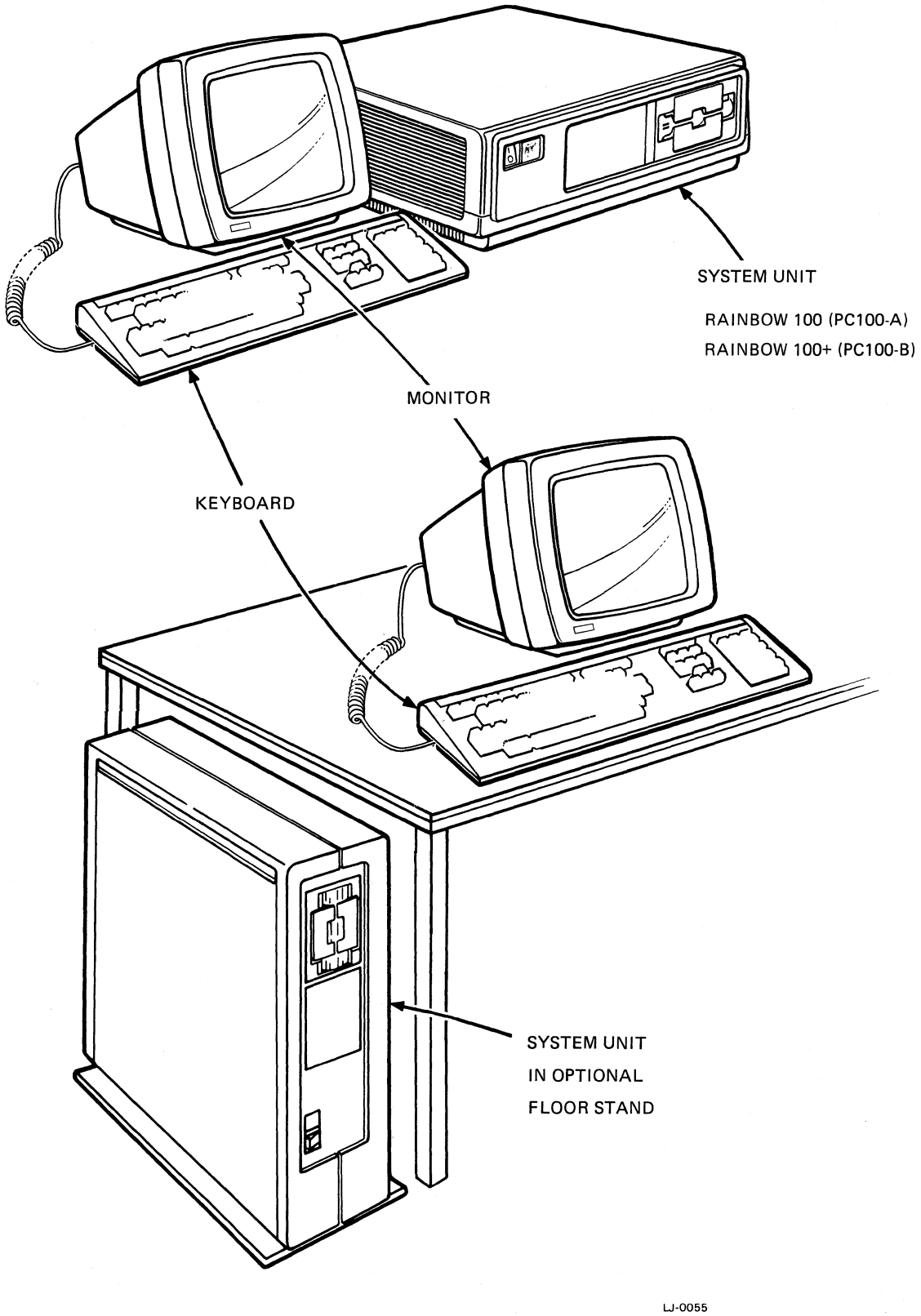


Figure 1-1 Basic Units of the Rainbow Computer

The Rainbow PC100-A system unit contains the following modules and assemblies.

- PC100-A system module (part number 70-19974-00)
- 64K bytes of main memory (expandable to either 128K bytes or 256K bytes)
- A standard dual-diskette drive with the capacity to hold 800K bytes of data on two 5-1/4 inch diskettes. An optional second dual-diskette drive provides an additional 800K bytes of memory storage capacity.
- An RX50 controller module
- A printer multiprotocol serial port for adding an optional printer
- A communications multiprotocol serial controller for adding an optional communication link to another computer
- An H7842-A dc power supply
- Three option slots for system expansion

A detailed description of the Rainbow 100 system unit is provided in the *Rainbow™ 100 Technical Manual* (EK-PC100-TM).

The Rainbow 100+ system unit contains the following modules and assemblies.

- PC100-B system module (part number 70-19974-02)
- 128K bytes of main memory (expandable to 320K bytes in 64K byte increments or 896K bytes in 256K byte increments)
- An RX50 dual-diskette drive with the capacity to hold 800K bytes of data on two 5-1/4 inch diskettes
- An RX50 controller module
- An RD51 hard disk drive which provides 10M bytes of formatted program storage
- An RD51 hard disk controller module
- Two option slots on the system module for system expansion
- An H7842-D dc power supply
- A printer multiprotocol serial port for adding an optional printer
- A communications multiprotocol serial port for adding an optional communication link to another computer

The Rainbow model PC100-B has all the modules and assemblies of the Rainbow 100+ with the exception of the Winchester hard disk drive and the hard disk controller module.

Table 1-1 provides a comparison of the different Rainbow models, their hardware differences, and system capabilities.

Table 1-1 Rainbow Model Comparisons

Hardware and Capability	Rainbow PC100-A	Rainbow PC100-A with Winchester	Rainbow PC100-B or 100+
System module	PC100-A (70-19974-00)	PC100-A (70-19974-00)	PC100-B (70-19974-02)
ROMs	3 (24K bytes)	3 (24K bytes)	2 (32K bytes)
Main system memory	64K bytes	64K bytes	128K bytes*
Memory options	64K and 192K bytes	64K and 192K bytes	128K and 256K bytes*
Total memory capacity	256K bytes	256K bytes	896K bytes
Power supply	H7842-A	H7842-D	H7842-D
Fan	AC	AC	DC
DC fan cable	Not present	Present, but not used	Yes
Winchester hard disk	No	Yes	Yes†
Color/graphics option	Yes	Yes	Yes
Extended communication option	Yes	No	‡
Automatic memory sizing	No	No	Yes
Automatic bootstrap	No	No	Yes
Capability to boot from Winchester	No	No	Yes

* The memory capacity of the 128K and 256K byte memory options can be increased in 64K or 256K byte increments.

† The Winchester hard disk is standard on the Rainbow 100+ and optional on the Rainbow PC100-B.

‡ The extended communications option is offered as an option only on the model PC100-B.

Printer Options – Any printer with the same FCC classification as the Rainbow 100+ computer, such as the LA50 Personal Printer, LA100 Printer, or LQP02 Letter-Quality Printer can be used with Rainbow computers.

1.2 FEATURES AND CAPABILITIES

The following features are standard on the Rainbow 100+ computer.

- Power-up selftest diagnostics with error messages and LED readouts
- 24 lines by 80- or 132-column video display
- 128K bytes of main memory (RAM)
- 800K bytes of diskette drive memory
- 10M bytes of Winchester hard disk drive memory
- Built-in controller for a serial printer port and an asynchronous/synchronous communications port
- Programmable baud rates for the printer and communications ports
- Hardware/software error messages
- Full VT102 ROM-based terminal emulation.

NOTE

The Rainbow model PC100-B has all the above standard features with the exception of the hard disk drive; however, this drive can easily be added to the system.

The Rainbow 100+ and the model PC100-B computers are capable of the following.

- Operating CP/M-86/80, concurrent CP/M-86/80, and MS-DOS software programs
- Automatically recognizing programs written for 8-bit or 16-bit (Z80 or 8088) processors when running CP/M-86/80
- Expanding main memory to 896K bytes
- Supporting an RS-423 printer and/or communications modem
- Providing optional color/graphics
- Providing optional extended communications ports (only on the model PC100-B)
- Automatically sizing memory
- Automatically bootstrapping

1.3 SPECIFICATIONS

The general system specifications for the Rainbow 100+ and model PC100-B computers follow. Additional specifications for each unit, module, or option are supplied in the appropriate chapters.

Environment

Temperature	
Operating*	15°C to 32°C (59°F to 90°F)
Not operating	−34°C to 60°C (−29°F to 140°F)
Relative Humidity	
Operating	20% to 80% with maximum wet bulb 25°C (77°F) and minimum dew point 2°C (36°F)
Not operating	5% to 90% (noncondensing)
Altitude (maximum)	
Operating	2.4 km (8,000 ft)
Not operating	9.1 km (30,000 ft)

1.3.1 System Unit and Power Supply Specifications

System Unit Weight and Dimensions:

Height	16.5 cm (6.5 in)
Length	48.3 cm (19 in)
Width	36.3 cm (14.3 in)
Weight	13.6 kg (30 lb)
Power Supply Type:	Transistor, switching type ac to dc converter
AC Input:	Switch-selectable
120 V (nominal)	Single-phase, 3-wire, (90 V to 128 V rms)
220 V to 240 V (nominal)	Single-phase, 3-wire, (174 V to 256 V rms)
Line Frequency:	47 Hz to 63 Hz low line, 57 Hz to 63 Hz high line
Line Current:	
115 Vac	3.0 A (rms), maximum
230 Vac	2.0 A (rms), maximum
AC Power Consumption:	237 W input maximum at full rated dc output load of 142 W, including 3 W of power for the system dc fan
Power Output:	142 W, maximum

* Maximum allowable temperature is reduced by 1.8°C per 1000 m (1°F per 1,000 ft) above sea level. Example: At 2.4 km (8,000 ft), the maximum temperature is 27.5°C (82°F).

Regulated Output Voltages:	+5.1 V ±6% +12.2 V ±6% −12.0 V ±7%
Load Current Range:	5.1 V (2.5 A minimum to 11.5 A maximum) 12.2 V (0.6 A minimum to 6.7 A maximum) 12.0 V (0.0 V minimum to 388 milliamp maximum with 5.1 V load current of 10.5 A and 12.2 V load current of 6.7 A)
Circuit Protection:	Circuit breaker, rated at 4.0 A, externally accessible
Power Supply Weight and Dimensions:	
Height	9.29 cm (3.66 in)
Length	36.83 cm (14.5 in)
Width	10.87 cm (4.28 in)
Weight	2.72 kg (6.0 lb)

1.3.2 Monochrome Monitor Specifications

Characters:	7 × 9 dot matrix, includes 2-dot descenders
Character Format:	24 lines × 80 or 132 characters
Graphics (with Graphics Option):	800 × 240 pixels
Screen Size:	30.5 cm (12 in) diagonal measurement
Screen Viewing Area:	12.7 cm × 20.3 cm (5 in × 8 in)
Cursor Type:	Keyboard-selectable, blinking block character or blinking underline
Standard Video Output:	RS170 compatible, monochrome character cell video
Screen Display Phosphor:	White, green, or amber
Monitor Viewing Angle:	Adjustable from +5 to −25 degrees
Monitor Weight and Dimensions:	
Height	29.2 cm (11.5 in)
Width	34.9 cm (13.75 in)
Depth	31.1 cm (12.25 in)
Weight	6.4 kg (14.0 lb)

1.3.3 Keyboard Specifications

Audio and Visual Indicators:	4 lights and bell-tone generator
Diagnostics:	Power-up selftest, generates identification code upon passing test

Keyboard:	Sculptured key array in four groups
Home Row Key Height:	3 cm (1.2 in) above desktop
Keys:	105 keys; matte, textured-finish, concave surface
Key Size (each):	1.27 cm (0.50 in) square
Key Spacing:	1.9 cm (0.75 in) center-to-center (single-width keys)
Key Wobble:	Less than 0.5 mm (0.020 in)
Travel to Activate Keys:	Less than 0.3 cm (0.12 in)
Numeric Data Entry Keypad:	18 keys
Typing Keys:	57 keys
Function Keys:	20 function keys horizontally positioned below label strip
Screen/Cursor Control Keys:	10 keys on the middle keypad
Power:	+12 V ±5% at 400 mA, 4.8 W maximum
Keyboard Weight and Dimensions:	
Height	1.25 cm (0.5 in) to 4 cm (1.6 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 kg (4.5 lb)

1.3.4 RX50 Dual-Diskette Drive Specifications

Performance:	
MFM Storage Capacity Per Diskette (80 tracks):	400K (409,600) bytes
MFM Storage Capacity Per Drive:	800K (819,200) bytes
MFM Storage Capacity Per Track (10 soft sectors):	5,120 bytes
MFM Storage Capacity Per Sector:	512 bytes
Average Access Time:	290 ns
MFM Data Transfer Rate:	250,000 bits/s
Functional Specifications:	
Diskettes Per Dual-Diskette Drive:	2
Number of Recording Surfaces Per Diskette:	1

Diskette Rotational Speed: 300 r/min (−1.5% to +1.5% maximum)

Track Density: 96 tracks per inch

Tracks (Per Diskette): 80

Input Power Requirements:

5.0 V (475 V minimum, 5.25 V maximum) at 0.5 A

12.0 V (11.4 V minimum, 12.6 V maximum) at 1.25 A

Power Dissipation:

Operating	17.5 W typical
Standby	4.2 W typical

Diskette Drive Weight and Dimension:

Height	8.4 cm (3.3 in)
Width	14.7 cm (5.8 in)
Depth	21.6 cm (8.5 in)
Weight	1.7 kg (3.8 lb)

1.3.5 RD51 Hard Disk Drive Specifications

Performance:

Formatted capacity per drive	10 Mbytes
Formatted capacity per surface	2.5 Mbytes
Formatted capacity per track	8,192 bytes
Formatted capacity per sector	256 bytes
Sectors per track	32
Average access time	85 ms
Data transfer rate	5 Mbits/s

Functional Specifications:

Disks per drive	2
Number of recording surfaces per disk	2
Disk rotational speed	3600 r/min ±1%
Track density	345 tracks per inch
Recording density	9,074 bits/in (maximum)
Cylinders	306
Read/write heads	4

Input Power Requirements:

12 V ±5%, 1.6 A typical, 3.5 A (at power on)
5 V ±5%, 1.1 A typical, 1.7 A (maximum)

Power Dissipation:

Typical	25 W
Maximum	32 W

Hard Disk Drive Weight and Dimensions:

Height	8.3 cm (3.3 in)
Width	14.6 cm (5.8 in)
Depth	20.4 cm (8.5 in)
Weight	2.3 kg (4.5 lb)

1.3.6 Memory Option Specifications

Memory Option Storage Capacity:

PC1XX-AC standard module configuration	128K bytes (18 64K × 1 bit chips)
PC1XX-AD standard module configuration	256K bytes (9 256K × 1 bit chips)

NOTE

To expand the storage capacity of the standard configurations install 64K byte (PC1XX-AY) or 256K byte (PC1XX-AZ) add-on memory chip sets.

Memory Option Functions:

Memory error reporting
Memory diagnostic capability
Memory option expansion capability

Power Requirements:

PC1XX-AC	5 Vdc
PC1XX-AD	5 Vdc

Module Dimensions:

Width	7.57 cm (2.9 in)
Length	25.4 cm (10.0 in)

1.3.7 Color/Graphics Option Specifications:

Graphics Type	
Resolution	Bit-mapped
High-resolution mode	800 pixels horizontally by 240 pixels vertically; 2 planes of memory
Medium-resolution mode	384 pixels horizontally by 240 pixels vertically; 4 planes of memory

Number of Colors Displayed (Color Monitor)

High-resolution mode	4 colors, selectable
Medium-resolution mode	16 colors, selectable
Palette	1,024 for the Rainbow PC100-A* 4,096 for the Rainbow PC100-B and Rainbow 100+

Number of Gray Shades Displayed (Monochrome Monitor)

High-resolution mode	4 gray shades
Medium-resolution mode	16 gray shades

Modes of Operation:

Text mode	Writes characters in a 10 × 10 character cell at a speed of 960 char/s.
Graphics mode	Supports vector drawing.
Scroll mode	Supports jump and 3 speeds of smooth vertical scrolling with a full or split screen.
Readback mode	Reads back a selected bit map memory plane to facilitate generation of hard copy on a printer or pen plotter. May also be used for diagnostic purposes.

Power Requirements:

5 Vdc +5% at 3.05 A (typical), 3.36 A (maximum)
12 Vdc +10% at 180 mA (typical), 220 mA (maximum)

Module Dimensions:

Width	14.48 cm (5.7 in)
Length	25.4 cm (10.0 in)

1.3.8 Color Monitor (VR241-A) Specifications

Video Format:	Red, green, and blue (RGB) color composite video (RS170 compatible)
Video Screen:	33 cm (13 in) diagonal, high-resolution color
Display Characteristics:	0.31 mm (0.012 in) dot pitch with bonded 62% anti-glare filter
Active Raster Size:	24 cm (9.45 in) width × 15 cm (5.9 in) height

* The palette for the Rainbow model PC100-A is 4096 if separate monitors are used for text and graphics.

Synchronization:	Selectable, on green or external
Vertical rate	60 Hz
Horizontal rate	15.72 kHz
Bandwidth	20 MHz
Power Supply Type:	Transistor, switch type ac to dc converter
AC input:	Switch-selectable
115 V nominal (100 V /115 V /120 V)	Single-phase, 3-wire, 90 V to 120 V rms, 47 Hz to 63 Hz line frequency
230 V nominal	Single-phase, 3-wire, 185 V to 256 V rms, 47 Hz to 63 Hz line frequency
Power consumption	85 W
Fuse	2.5 A, externally accessible

Monitor Weight and Dimensions:

Height	31.9 cm (12.8 in)
Width	36.3 cm (14.5 in)
Depth	43.2 cm (17.0 in)
Weight	16.6 kg (36.6 lb)

1.3.9 Extended Communications Option Specifications

Option Digital Part Number: PC1XX-BB

Functions:

Provides two additional serial communications ports

Supports asynchronous, bit-synchronous, and byte-synchronous protocols

Direct memory access (DMA) and programmed I/O modes

Provides internal serial data loopback for diagnostic testing

Communications Ports:

Port A	RS422/RS485 high-speed, half-duplex, fixed 722K baud rate
Port B	RS232C/RS423 low-speed, full-duplex with modem control, programmable baud rate

Programmable Baud Rates:

Port B	50, 75, 110, 134.5, 150, 200, 300, 600, 1,200, 1,800, 2,000, 3,600, 4,800, 9,600, 19,200

Protocols Supported:

Asynchronous	Data formats include 5, 6, 7, or 8 data bits, even, odd or no parity, and 1, 1.5, or 2 stop bits. Detects parity, framing, and overrun errors.
Byte-synchronous	DDCMP, BISYNC
Bit-synchronous	SLDC, HLDC, X.25 LAP, and ADCCP

Synchronization:

Byte-synchronous mode	External signal or internal detection of a one-byte or two-byte synchronization pattern. Data is checked by an internal CRC-16 or CRC-CCITT generation and detection circuit.
Bit-synchronous mode	HLDC/SLDC flag generation and recognition, 8-bit address recognition, automatic zero insertion and deletion, and automatic CRC-CCITT generation and checking

Power Requirements:

+5 Vdc at 790 mA (typical), 1.1A (maximum)
+12.0 Vdc at 39 mA (typical), 54 mA (maximum)
−12.0 Vdc at 39 mA (typical), 54 mA (maximum)

Module Dimensions:

Width	9.90 cm (3.9 in)
Length	25.4 cm (10.0 in)

Communications Connectors:

Port A	Nine pin subminiature "D" type
Port B	Twenty-five pin subminiature "D" type

1.4 REFERENCE DOCUMENTATION

Additional documentation containing information pertaining to the Rainbow computer is available from Digital as well as other sources.

Digital Documentation

Title	Digital Part No.*
Color/Graphics Option Programmer's Reference Guide	AA-AE36A-TV
Rainbow™ Installation Guide	EK-R100E-IN
Rainbow™ 100 Owner's Manual	EK-P100E-OM†
Rainbow™ Owner's Manual	EK-R100E-OM‡
Rainbow™ 100 User's Service Guide	EK-P100E-SV
Rainbow™ Memory Board Option Installation Guide	EK-RBMXE-IN
PC100 Rainbow™ System Unit IPB	EK-SB100-IP
Rainbow™ 100 Technical Manual	EK-PC100-TM
Rainbow™ Pocket Service Guide	EK-PC100-PS-002

Rainbow™ Winchester Disk Option Installation Guide	EK-RBWIN-IN†
Rainbow™ 100 Winchester Disk Option Upgrade and Installation Guide	EK-PCWIN-IN*
Rainbow™ Color/Graphics Option Installation Guide	EK-PCCOL-IN
Rainbow™ 100 Extended Communications Option Installation Guide	EK-PCEXC-IN
Rainbow™ 100 Extended Communications Programmer's Reference Guide	AA-V172A-TV
Rainbow™ CP/M-86/80 Getting Started	AA-Y523B-TV
Rainbow™ CP/M-86/80 User's Guide	AA-Y524A-TV
Rainbow™ MS™-DOS User's Guide	AA-Y894A-TV
Rainbow™ MS™-DOS Advanced User's Guide	AA-Y983A-TV
Rainbow™ 100 Getting Started	AA-N575B-TV*
Rainbow™ 100 User's Guide	AA-P300B-TV*
Rainbow™ GSX-86 Getting Started	AA-V526A-TV
Rainbow™ GSX-86 Programmer's Reference Manual	AA-W964A-TV
VR241-A Color Video Monitor Pocket Service Guide	EK-VR241-PS

These manuals can be ordered from:

Digital Equipment Corporation
Accessories and Supplies Group
P.O. Box CS2008
Nashua, New Hampshire 03061

Other Documentation

Title	**Order From**
iAPX 88 Book *8251A Programmable USART Specifications* *8237A-5 DMAC Specifications*	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051
Z80A Technical Manual	Zilog, Inc. 10340 Bubb Road Cupertino. CA 95014
7201 MPSC Specification *7220 GDC Design Manual*	NEC Microcomputers, Inc. 173 Worcester Street Wellesley, MA 02181
WD1010 Winchester Disk Controller Specification *WD1793 Floppy Disk Formatter/Controller Specification*	Western Digital Corp. 2445 McCabe Way Irvine, CA 92714

* The first two letters of the part number designate the type of manual. EK = hardware manual, AA = software manual.
† Rainbow PC100-A only (This manual has three magenta stripes on the cover.)
‡ Rainbow PC100-B only (This manual has a rainbow on the cover.)

CHAPTER 2
OPERATING INFORMATION

2.1 GENERAL

This chapter describes the procedures for operating the Rainbow PC100-B computer without going into details on software use or application programs. Refer to the *Rainbow™ CP/M®-86/80 User's Guide* (AA-Y524A-TV), the *Rainbow™ MS™-DOS User's Guide* (AA-Y894A-TV), and the *Rainbow™ GSX-86 Programmer's Reference Manual* (AA-W964A-TV) for information on the use of software or applications programs.

2.2 USING DISKETTES

1. Always handle diskettes by the label end.

2. Keep diskettes away from magnetic tools.

3. Insert diskettes so that the orange arrow on the diskette points to the orange strip on the front bezel which becomes visible when the drive door is open.

4. Never insert and remove diskettes when power is off.

5. Never remove a diskette when the light on the front of that drive is on.

6. Use pre-formatted diskettes when possible. RX50 diskettes can be pre-formatted or formatted in the field.

7. Use write-protect tabs for the operating system diskettes and for other diskettes you want to write-protect. Write-protect tabs are available at most computer stores.

2.3 POWERING UP THE RAINBOW PC100-B COMPUTER

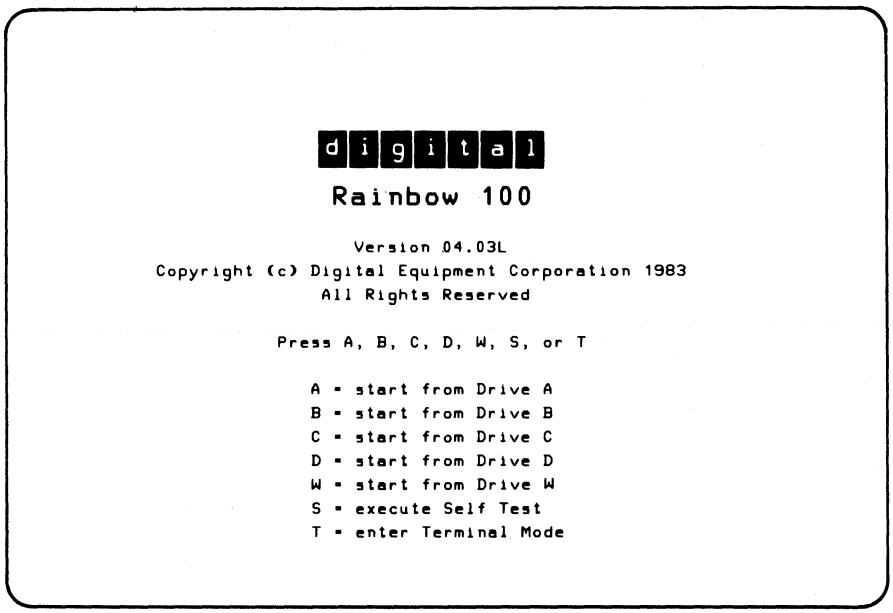
The Rainbow PC100-B computer has an auto-boot feature, that, when selected, automatically transfers (loads) the operating system program from a selected auto-boot device into memory when you turn on the computer. The screen the computer displays after power-on or reset depends on whether you select any of the auto-boot devices to auto-boot the operating system. The following paragraphs describe the operation performed and the displays produced by the computer when it is powered on either with or without the auto-boot feature selected.

The following power-on procedures assume that the Rainbow PC100-B computer has been properly installed and previously powered up in accordance with the instructions given in the *Rainbow™ Installation Guide* (EK-R100E-IN).

2.3.1 Power On Without Auto-Boot

1. Place the power switch on the front of the system unit to 1 (on). At this point the Rainbow PC100-B computer runs an internal ROM-based power-on selftest to determine if the computer

can load a diskette and run as a terminal. The computer displays the word TESTING in reverse video in the upper left corner of the screen while the test is in progress. If the power-on selftest completes successfully and the auto-boot feature has not been selected, the computer displays the Main System Menu and sounds the computer bell once. See Figure 2-1.



MR-10940

Figure 2-1 Rainbow Main System Menu

NOTE
The Main System Menu selection, "W - start from Drive W", is not available on the PC100-A or the PC100-A with the hard disk upgrade kit.

The screen shown in Figure 2-1 may not be identical to the one displayed on your computer. The general information should be the same; but specific information such as dates and version numbers may differ.

2. Run the extended selftest. This test runs more extensive internal diagnostic tests than those run upon power on or reset. Run this test when a problem is suspected in the diskette drives. Use the following procedure to run the extended selftest.

   a. Open drive A and, if desired, drive B.

   b. Load a formatted blank or scratch diskette into drive A and close its door.

   c. If also testing drive B, load a formatted blank or scratch diskette into the drive and close its door.

   d. Press the **S** key on the keyboard. The computer displays the word TESTING in reverse video in the upper left corner of the screen while the test is in progress. If the extended selftest is completed successfully, the computer displays the Main System Menu again (Figure 2-1), and sounds the computer bell once.

2.3.2 Power On with Auto-Boot

1. Placing the power switch to 1 (on) with the auto-boot feature selected causes the computer to run the power-on selftest. The computer displays the word TESTING in reverse video in the upper left corner of the screen while the test is in progress. If the power-on selftest is completed successfully, the computer then transfers the operating system from the previously selected diskette drive (A, B, C, or D) or the hard disk drive (W) into the main memory and displays the operating system title followed by the selected boot device and prompt character (Figure 2- 2).

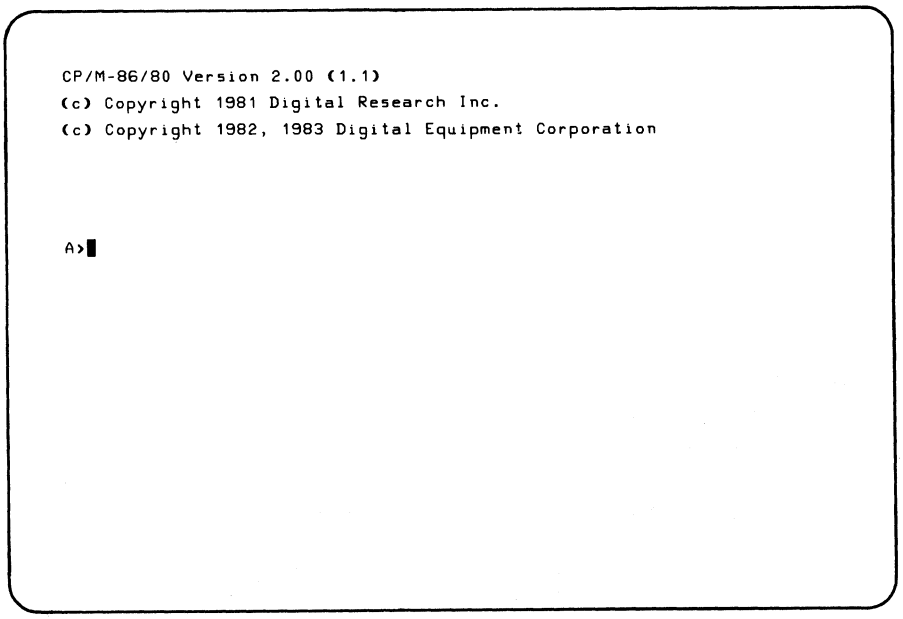


Figure 2-2 CP/M-86/80 Operating System Start-Up Message

NOTE

The screen shown in Figure 2-2 may not be identical to the one displayed on your computer. The general information should be the same, but specific information, such as dates and version numbers, may differ.

The last symbol displayed on the left side of the screen, A>, is called the operating system prompt, or prompt. The prompt consists of the drive the operating system is currently working from and a right angle bracket.

When auto-booting the operating system, the computer displays a letter indicating which drive loaded the operating system into memory. The computer displays letter A, B, C, or D if the operating system was loaded from a diskette drive. If the operating system was loaded from the hard disk drive, the computer displays the letters E, F, G or H, depending on how the disk drive was partitioned.

2. If you select a diskette drive (A, B, C, or D) as the auto-boot device, and an operating system diskette is not in the selected drive, or the drive door is open when the system is powered on, the computer runs the power-on selftest and then displays a drive-not-ready message (see Figure 2-3). Put the operating system diskette into the selected drive and load it into memory by pressing the appropriate keyboard key (A, B, C, or D).

3. If you select the hard disk drive as the auto-boot device and the operating system is not stored on the disk, the computer runs the power-on selftest, then displays the Main System Menu and a drive-not-ready message when you turn it on. See Figure 2-3.

   The procedure for storing the operating system program on the hard disk is described in Paragraph 2.4.2.6.

2.3.3 Power-On Error Messages

The computer displays error messages if the computer encounters an error while running the power-on selftest or the extended selftest. There are two types of error messages, nonfatal and fatal.

If a nonfatal error occurs while running the power-on selftest or the extended selftest, one bell sounds and the computer displays a message in flashing reverse video above the Main System Menu. An example of an error message display is shown in Figure 2-3. A nonfatal error indicates that only one of computer's operational modes is working. For example, if a diskette drive fails, the Rainbow computer can still be operated as a terminal connected to a remote computer. If the communications line fails, the Rainbow computer can still be operated as a personal computer.

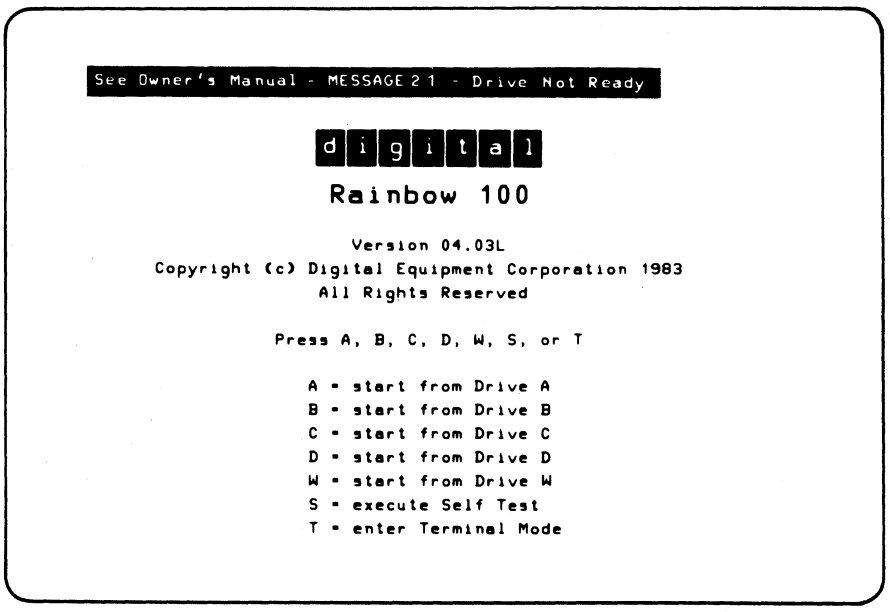


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Figure 2-3 Main System Menu with Message

If a fatal error occurs while running the power-on or extended selftest, three bell tones sound, the computer does not display the Main System Menu, and it may or may not display an error message (see Figure 2-4). An error code, displayed by the lights on the back of the system unit, also reports the error.

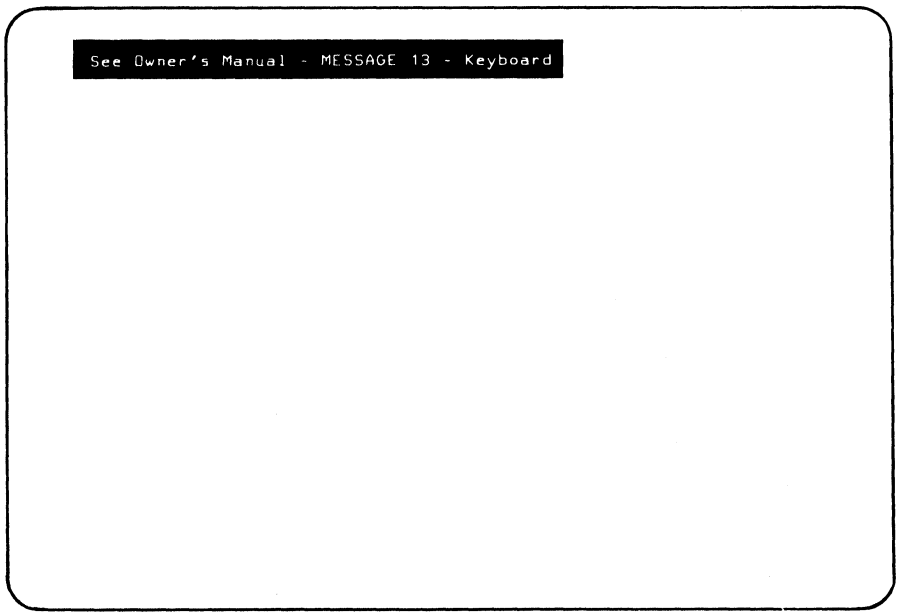


Figure 2-4 Error Message Display

When a fatal error occurs, you cannot operate the Rainbow computer in either the personal computer or terminal mode and you must correct the cause of the error before using the computer. Appendix B lists the error messages and error codes for determining the possible causes of reported errors.

2.4 SET-UP FEATURES

Set-Up features are a series of options in the Rainbow computer that allow you to tailor the computer to your operating environment. Set-Up features can be grouped in three general categories: installation, operator comfort, and compatibility with a remote computer and/or external devices.

You can change the Set-Up features temporarily or you can store them permanently in nonvolatile memory (NVM).

To change a Set-Up feature, enter the Set-Up mode, display the various Set-Up menus until you reach the desired feature, and make the change. The location of the **Set-Up** key is shown in Figure 2-5.

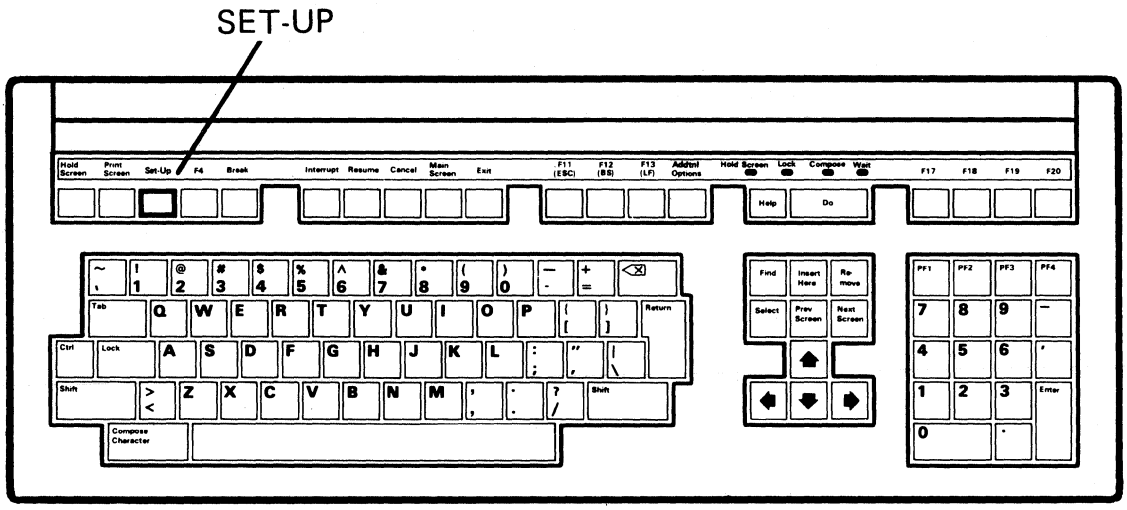


Figure 2-5 Set-Up Key Location

If you want the Set-Up feature change to be permanent, that is, to remain in effect after you turn the system off and back on again, you must save the Set-Up feature. Use the following procedures to manipulate the Set-Up features.

- To enter Set-Up, press **<Set-Up>**.
- To leave Set-Up, press **<Set-Up>** again.
- To perform a system reset, enter Set-Up and press **<Ctrl/Set-Up>**. This stops whatever program, diagnostic, or operating system is running; performs a brief test (3 seconds); and returns you to the Main System Menu.
- To restore the default Set-Up features, enter Set-Up and press **<Shift/D>**. This changes all the Set-Up features to the features the system had when it was originally shipped. This set of features is adequate for many installations. When you restore the default Set-Up features, the text that was on the screen before you entered Set-Up is lost.
- To recall the Set-Up features, enter Set-Up and press **<Shift/R>**. This returns the Set-Up features to what they were the last time they were saved. With Set-Up, this is the same as turning the system off and then back on again. When you recall the Set-Up features, the text that was on the screen before entering Set-Up is lost.
- To save the Set-Up features, enter Set-Up and press **<Shift/S>**. This saves the current Set-Up features in nonvolatile memory (NVM) so they will not be lost when you turn off the system.

- To move to another Set-Up menu, press the **<Next Screen>** or **<Prev Screen>** key.
- To select another variable within a Set-Up menu, press the ← or → key.
- To change the value of a variable, press the ↑ or ↓ key.

2.4.1 Terminal Mode

When the Rainbow computer is in the terminal mode, it acts like a terminal. It sends all the characters typed on the keyboard to the remote computer through the communications port. The remote computer processes the characters and echoes them on the screen. The Rainbow computer must be in the line mode (see Paragraph 2.4.2) to communicate with the remote computer. To enter terminal mode, press **T** when the computer displays the Main System Menu (Figure 2-1). To leave terminal mode and return to the Main System Menu, reset the computer (enter Set-Up and press **Ctrl/Set-Up**).

NOTE

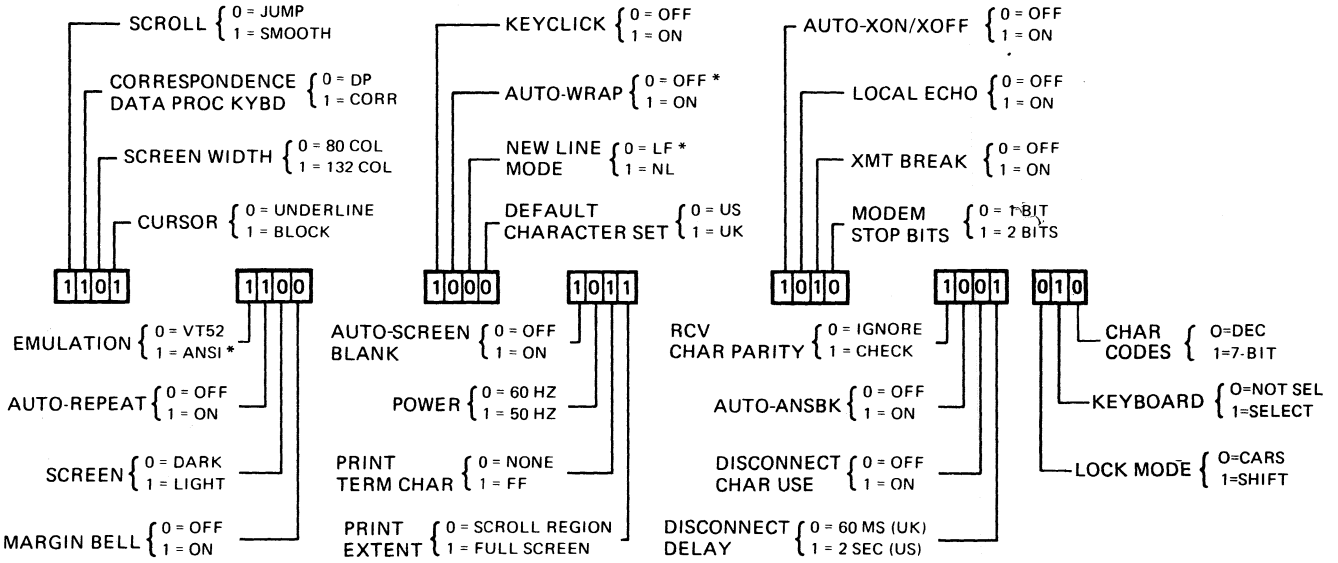
Certain features of the Rainbow computer must remain at their factory settings so that you can use the software that comes with the computer. You can change these features when you use the Rainbow computer as a terminal; but, you must change them back to their factory settings, shown in the table below, when you use the Rainbow as a personal computer.

Features	Selection	Factory Setting
Emulation (ANSI/VT52)	ANSI	1
Auto-wrap	Off	0
New line mode	LF (line feed)	0

Local and Line Modes – The local/line mode selection only affects the Rainbow computer when it is in terminal mode. In line mode, the mode normally used, the computer interacts with the remote computer, sending all the characters typed on the keyboard to the remote computer where they are processed and echoed back to the Rainbow computer. In local mode, the Rainbow computer acts like a typewriter. The computer displays everything typed on the screen but does not send it to the remote computer or process it by itself. You can enter the escape sequences to control cursor position, character set selection, bold, blinking, and other attributes directly from the keyboard. Pressing the **Print Screen** key in local mode sends the screen display to the printer. To change from line mode to local mode or from local mode to line mode, enter Set-Up and press **L**.

2.4.2 Set-Up Menus

There are six Set-Up menus in each version of the Rainbow computer, and each menu has selections (parameters) which can be changed. Figure 2-6 summarizes the selections available for the Rainbow PC100-B and 100+ computers and shows their default values. The Set-Up menus and their selections are described in the following paragraphs.



* THESE SETTINGS MUST BE SELECTED TO USE THE SOFTWARE THAT COMES WITH THE RAINBOW COMPUTER.
YOU CAN CHANGE THESE FEATURES WHEN YOU USE THE RAINBOW COMPUTER AS A TERMINAL; BUT, YOU MUST CHANGE THEM BACK TO THEIR FACTORY SETTING WHEN YOU USE THE RAINBOW AS A PERSONAL COMPUTER.

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Figure 2-6 Summary of Parameter Settings

2.4.2.1 Tabs Set-Up Menu

The Tabs Set-Up menu is shown in Figure 2-7. Use the ← and → keys to select tab columns; use the ↑, ↓, or **T** keys to set and clear tab stops. Press **<Ctrl/Tab>** to clear all of the tabs; press **<Shift/Tab>** to restore the default tab settings.

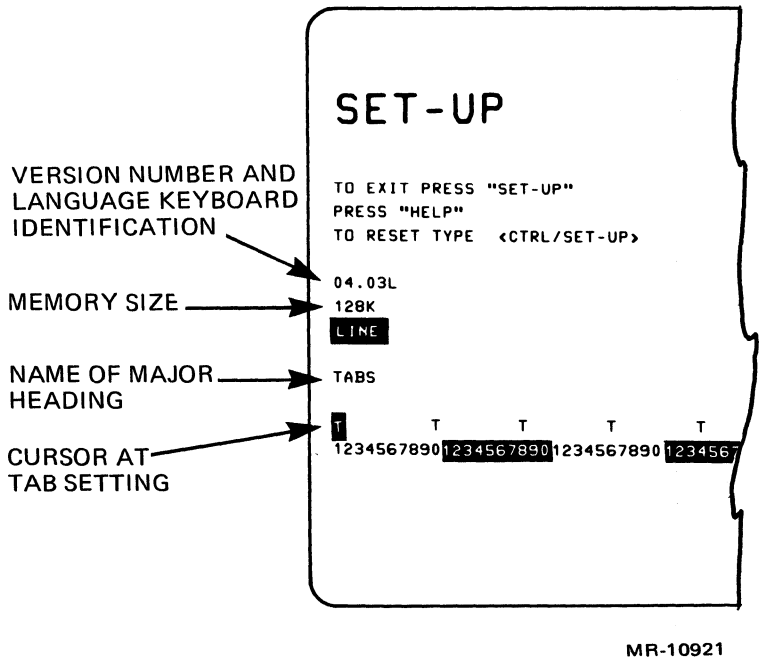


Figure 2-7 Tabs Set-Up Menu

2.4.2.2 Parameter Settings Set-Up Menu – Figure 2-8 shows the Parameter Settings (Param Set) Set-Up menu. Use this menu to manipulate the following features.

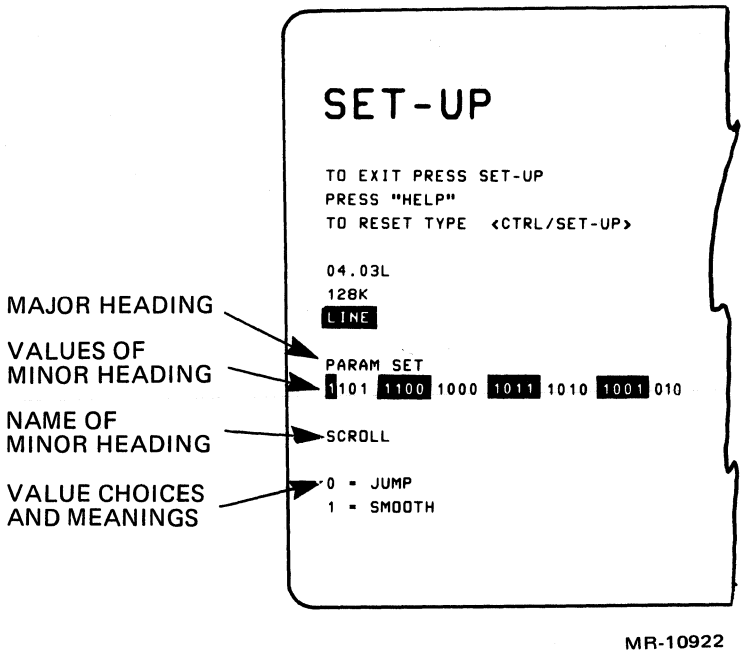


Figure 2-8 Parameter Settings Set-Up Menu

1. SCROLL – Select smooth or jump scrolling.

2. CORRESPONDENCE/DATA PROC KYBD – Use this feature with keyboards other than the U.S.A. keyboard. The correspondence setting enables characters on the left side of the key caps. The data processing setting enables characters on the right side of the keycaps.

3. SCREEN WIDTH – Select a width of 80 columns or 132 columns. When you change the width, the text that was on the screen before you entered Set-Up is lost.

4. CURSOR – Select an underline or block cursor.

5. EMULATION – When your Rainbow computer is connected to a remote computer you can choose to have the computer behave either like a VT52 terminal or according to the American National Standards Institute (ANSI) standard.

6. AUTO-REPEAT – You can choose to have keyboard keys repeat when you hold them down.

7. SCREEN – Select a dark (white characters on a black screen) or light screen display.

8. MARGIN BELL – You can choose to have a bell sound when you near the end of a line of typing.

9. KEYCLICK – You can choose to have keys click when you press them.

10. AUTO-WRAP – Select on to have the computer automatically start a new line when the text reaches the edge of the screen. Select off for CP/M-86/80 application software.

11. NEW LINE MODE – Select LF (line feed) or NL (new line) when using the Rainbow computer as a terminal; however, you must use LF (the 0 setting) when using the Rainbow as a personal computer to use the software that comes with the computer.

12. DEFAULT CHARACTER SET – Select US ASCII for the # character or UK for the £ character.

13. AUTO-SCREEN BLANK – You can choose to have the screen go blank after it has been idle for more than 30 minutes. A phantom cursor remains on the screen.

14. POWER – Match the monitor scan rate to the power line frequency to prevent screen jitter. (60 Hz is recommended regardless of line frequency.)

15. PRINT TERM CHAR – Select a print termination character. When set to FF (1), the system automatically sends a form feed character to the printer at the end of each print screen function. Used only for terminal mode.

16. PRINT EXTENT – Select scroll region or full screen. When set to scroll region, the computer prints only the lines selected by the remote computer. Used only for terminal mode.

17. AUTO-XON/XOFF – You can choose to enable the XON and XOFF signals. When on, the Rainbow computer uses XON and XOFF control signals to tell the remote computer to pause when the Rainbow computer's incoming buffer is full so that characters are not lost. This is used only for terminal mode.

18. LOCAL ECHO – Choose to turn local echo on or off. It is normally off. Turn it on when connected to a remote computer that does not echo the characters on the screen as you type them. Used only for terminal mode.

19. XMT BREAK – Choose to enable or disable the **Break** key. Use only for terminal mode.

20. MODEM STOP BITS – Select modem stop bits. Normally, you use 1 stop bit at baud rates over 110, and 2 bits at 110 and slower. This is used only for terminal mode.

21. RCV CHAR PARITY – Check for or ignore incoming data parity errors. Used only for terminal mode.

22. AUTO-ANSBK – Turn auto-answerback on or off. If auto-answerback is on, the Rainbow computer automatically sends a message to the remote computer when: 1) a connection is made; 2) the host sends an ENQ code; or 3) you press **<Ctrl/Break>**. To store an answerback message, press **<Shift/A>**, follow this with any convenient delimiter character that you are not going to use in your message, (for example, / or *), type your message (up to 20 characters), and follow your message with the same delimiter character. For example, to use Auto-Ansbk to log in on a remote computer whenever you turn on your Rainbow computer, you might type the following.

```
<Shift/A>*LOGIN PASSWORD<Return>*
```

The computer displays **<Return>** as a reverse video M. Used only for terminal mode.

23. DISCONNECT CHAR USE – Choose to enable a disconnect character to disconnect a telephone line. Used only for terminal mode.

24. DISCONNECT DELAY – Set how long the system will wait after loss of telephone carrier before disconnecting. In the United Kingdom, 60 ms is typical; in the United States and other countries, 2 seconds is typical. This value is only used with FDXB and FDXC modem protocols; it is ignored with FDXA. See Paragraph 2.4.2.3, Modem Set-Up Menu. Used only for terminal mode.

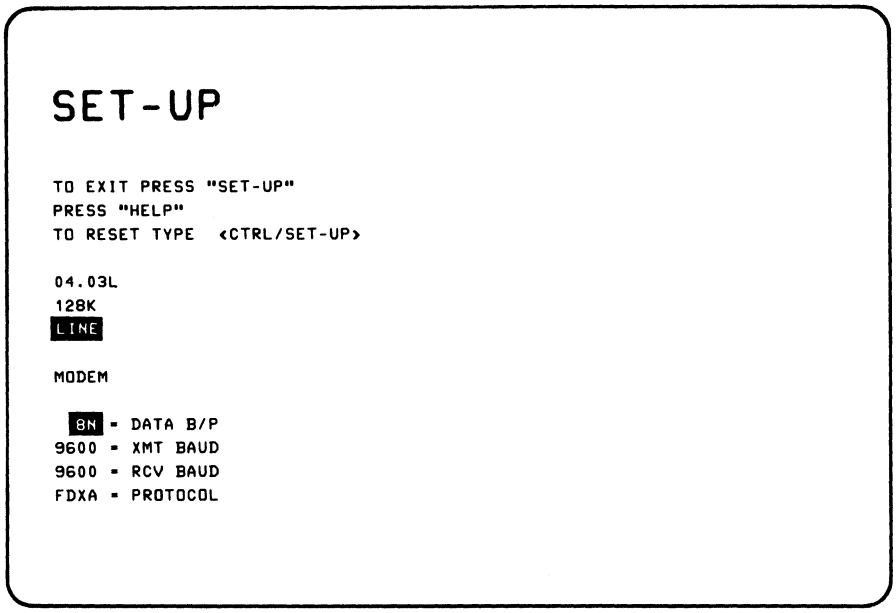
25. LOCK MODE (PC100-B and 100+ only) – Choose how you want to use the **Lock** key. Keyboards generate a different set of characters depending on how Lock Mode is set. If you select caps lock, only the alphabetic keys will generate shifted characters. If you select shift lock, all keys will generate shifted characters.

26. KEYBOARD (PC100-B and 100+ only) – Choose another keyboard language with this setting. Change the setting to 0, press **<Shift/S>** to save the setting, and press **<Ctrl/Set-Up>** to reset the computer. The computer will display the language selection menu (Figure 2-9). Follow instructions on the screen to select a new language.

Figure 2-9 Language Selection Menu

27. CHAR CODES (PC100-B and 100+ only) – Select the DEC Multinational Character set, which has 256 characters and uses 8 bits to code each character, or select the National Replacement Character set, which has 128 characters and uses 7 bits to code each character. The National Replacement Character set used is determined by the keyboard currently selected.

2.4.2.3 Modem Set-Up Menu – You can manipulate four features from the Modem Set-Up menu, shown in Figure 2-10, to configure the Rainbow computer to communicate with a remote computer.



MR-11131

Figure 2-10 Modem Set-Up Menu

1. DATA B/P (data bits and parity) – Set data bits to 7 or 8 data bits per character. Set parity to odd, even, or no parity. For example, 8N means 8 data bits per character and no parity bit transmitted or expected on reception.

2. XMT BAUD (transmit baud rate) – Set the rate at which data is sent from the Rainbow computer to the remote computer.

3. RCV BAUD (receive baud rate) – Set the rate at which the Rainbow computer will receive data from the remote computer.

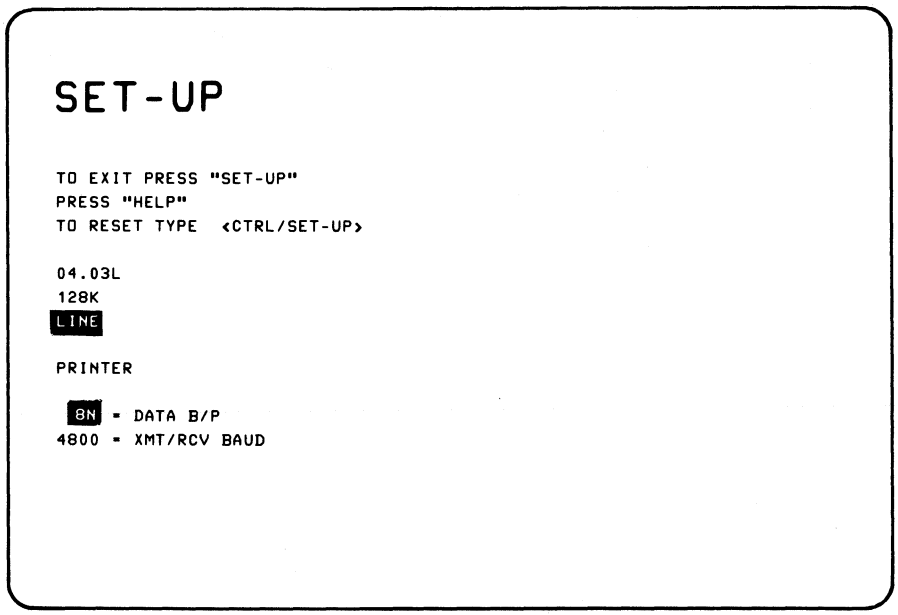
NOTE

When changing the data bits and parity, the computer does not recognize the change until reset. XMT and RCV BAUD rate changes are recognized immediately.

4. PROTOCOL – This feature, which includes three protocols, applies only to terminal mode.

   a. FDXA – Full-duplex, no modem (data leads only)
   b. FDXB – Full-duplex, full modem control
   c. FDXC – Asymmetrical full-duplex with full modem control (requires a special cable)

2.4.2.4 Printer Set-Up Menu – You can select two features from the Printer Set-Up menu, shown in Figure 2-11, to configure the Rainbow computer to communicate with its printer.



MR-11132

Figure 2-11 Printer Set-Up Menu

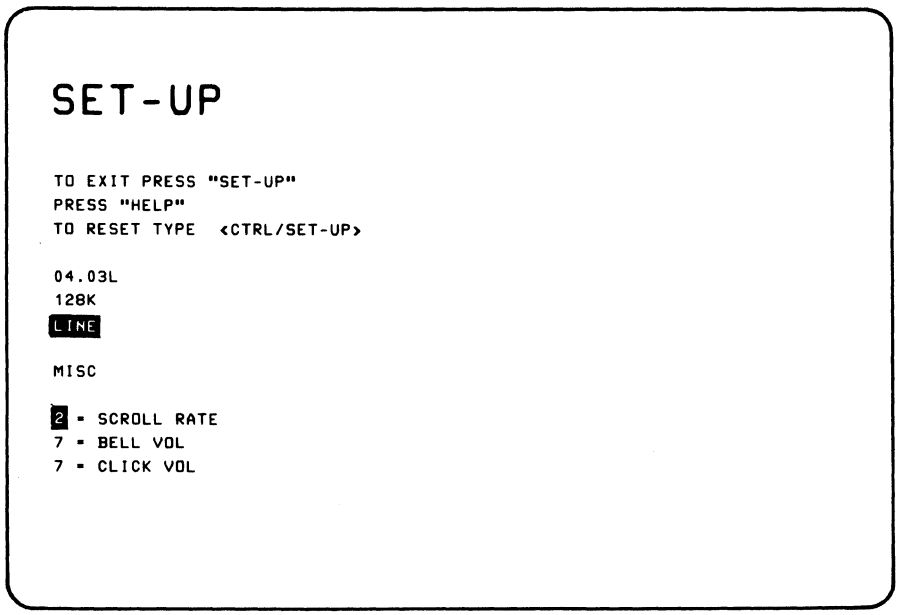
1. DATA B/P (data bits and parity) – Set data bits to 7 or 8 data bits per character. Set parity to odd, even, or no parity. For example, 8N means 8 data bits per character and no parity bits transmitted or expected on reception. The LA100, LQP02, and LA50 printers are set up for 8 data bits and no parity when shipped.

2. XMT/RCV BAUD (transmit/receive baud rate) – Set the rate at which the Rainbow computer sends data to its printer and the rate at which it receives status information from its printer. The LA100, LQP02, and LA50 printers are set for a baud rate of 4,800 when shipped.

NOTE

When changing the data bits and parity, the computer does not recognize the change until reset. XMT and RCV BAUD rate changes are recognized immediately.

2.4.2.5 Miscellaneous Set-Up Menu – You can select three features from the Miscellaneous (Misc) Set-Up menu, shown in Figure 2-12.



MR-11140

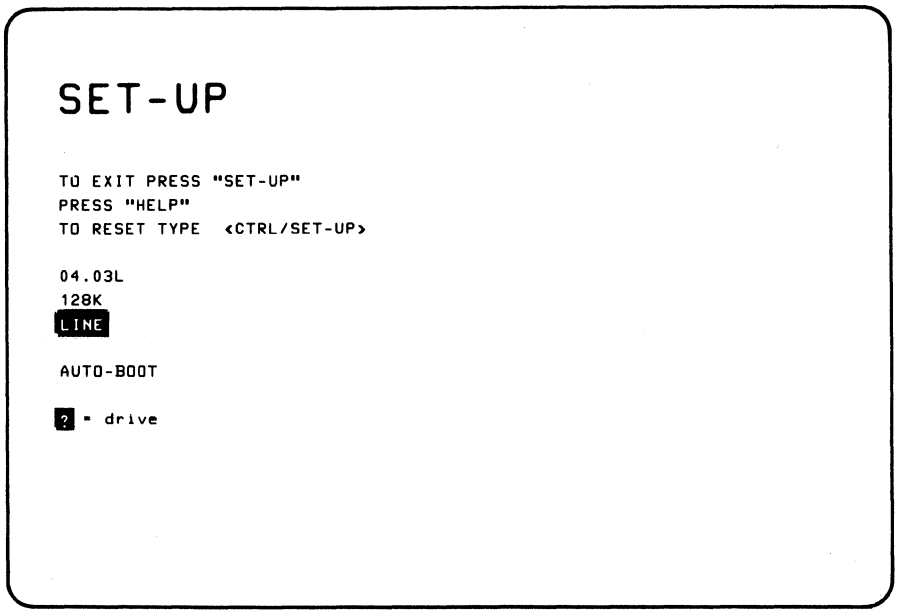
Figure 2-12 Miscellaneous Set-Up Menu

1. SCROLL RATE – Select 1, 2, or 3. Three is the fastest scroll rate (applicable only if smooth scrolling is selected).

2. BELL VOL – Select a bell volume level between 1 and 8. Eight is the loudest.

3. CLICK VOL – Select a keyclick volume level between 1 and 8. Eight is the loudest.

2.4.2.6 Auto-Boot Set-Up Menu (PC100-B and 100+ only) – Figure 2-13 shows the Auto-Boot Set-Up menu. Use this menu to enable one of the diskette drives (A, B, C, or D) or a hard disk drive (W) to load the operating system automatically. The default (represented by a '?' on your screen) indicates that no device is selected.



MR-10924

Figure 2-13 Auto-Boot Set-Up Menu (Rainbow PC100-B and 100+ only)

NOTE

W = start from Drive W is not available on the PC100-A or the PC100-A with the hard disk Winchester upgrade kit.

When you select the hard disk as the auto-boot device, the CP/M-86/80 operating system must be present on the hard disk to allow the computer to auto-boot it into memory-on/power up. If the CP/M-86/80 operating system is not on the hard disk, it can be loaded onto the disk by performing the following steps.

NOTE

See the *Rainbow™ Winchester Disk Option Installation Guide* (EK-RBWIN-IN) and Chapter 6 of the *CP/M-86/80 User's Guide* (AA-Y524-TV) for additional information on loading an operating system on the hard disk.

1. If desired, repartition the hard disk as follows.

NOTE
Repartitioning destroys all data.

   a. Load the Rainbow Hard Disk Utility Program diskette into drive A.
   b. Type **A** from the Main System Menu.
   c. Type **2** and press the **Do** key to repartition the hard disk.
   d. Follow the instructions on the screen.

2. Select Auto-Boot Partition as follows.

   a. From the Main Menu of the Rainbow Hard Disk Utility Program diskette, type **6** and press the **Do** key to select Auto-Boot Partition.

   b. Select the desired boot drive and press the **Do** key to enable auto-boot from that drive (the hard disk drive).

   c. Press **<Set-Up>** and **<Ctrl/Set-Up>** to reset the computer.

3. Load the operating system onto the hard disk as follows.

   a. Remove the write-protect tab from a copy of the operating system diskette (version 2.0 or higher); then, load it into drive A.

   b. Type **A** from the Main System Menu.

   c. After the prompt, type: **submit syscopy A: E:** if drive E is being loaded and press **<Return>**. If drive F is to be loaded, type: **submit syscopy A: F:** and press **<Return>**.

   d. When the program is through copying all files, remove the diskette from drive A and install a write-protect tab on it. List all files.

   e. All other files may be transferred by using the Peripheral Interchange Program (PIP) command.

4. Change Set-Up to boot from hard disk drive as follows.

   a. Press **<Set-Up>** and **<Prev Screen>** to access the Auto-Boot Set-Up menu.
   b. Press the ↓ key to display:
      W = drive
   c. Press **<Shift/S>** to save this selection.
   d. Press **<Ctrl/Set-Up>** to reset the computer.

CHAPTER 3
PC100-B SYSTEM MODULE TECHNICAL DESCRIPTION

3.1 INTRODUCTION

This chapter provides a technical description of the Rainbow PC100-B system module for repair and maintenance personnel. The system module is described to the functional block diagram level. The logic circuits are not described to the detailed circuit level in this addendum. The PC100-B system module contains many logic circuits which are similar to the logic circuits used in the PC100-A system module. A more detailed description of these logic circuits can be found in the *Rainbow™ 100 Technical Manual* (EK-PC100-TM).

Many terms used in this chapter are written out the first time they appear, followed by an abbreviation or mnemonic in parenthesis. Only the abbreviation or mnemonic is generally used after the first time it appears in the description. Appendix D is a glossary of terms and abbreviations.

Numbers are given in binary, octal, decimal, or hexadecimal (hex). The decimal form is used for numbers in general; the hexadecimal form for data and addresses. Numbers are subscripted B for binary, Q for octal, H for hexadecimal, and no subscript for decimal.

3.1.1 Chapter Organization

The information in this chapter is divided into five sections.

1. A general description of the functions performed by the system module (Paragraph 3.2)
2. A physical description of the system module (Paragraph 3.3)
3. A functional description of the system module (Paragraph 3.4)
4. A description of the system module connectors (Paragraph 3.5)
5. System module specifications (Paragraph 3.6)

3.1.2 Related Documentation

The detailed circuit logic for the PC100-B system module is on a set of 11 sheets of schematics. The drawing number for the set is D-CS-5416206-0-1.

3.2 GENERAL DESCRIPTION

The system module has a dual-processor architecture which uses an 8088 16-bit processor coupled with a Z80A 8-bit microprocessor. Figure 3-1 is a block diagram showing the relationship between the microprocessors and their supporting logic. The microprocessors operate from and transfer data through memory to direct, control, and monitor the system functions. The system module contains 128K bytes of standard RAM that is partitioned into a low order 64K byte bank and a high order 64K byte bank. 62K bytes of the low order bank can be accessed by both microprocessors. The Z80A microprocessor can access 2K bytes of private RAM in addition to the shared 62K bytes of RAM. The 8088 processor can access all 128K bytes of standard RAM and the following additional memory.

- 32K byte or 64K byte ROM
- 4K bytes of video screen RAM (static)
- 4K bytes of video attribute RAM (static)

- 256 × 4 bit NVM
- 64K byte to 768K byte optional unshared RAM

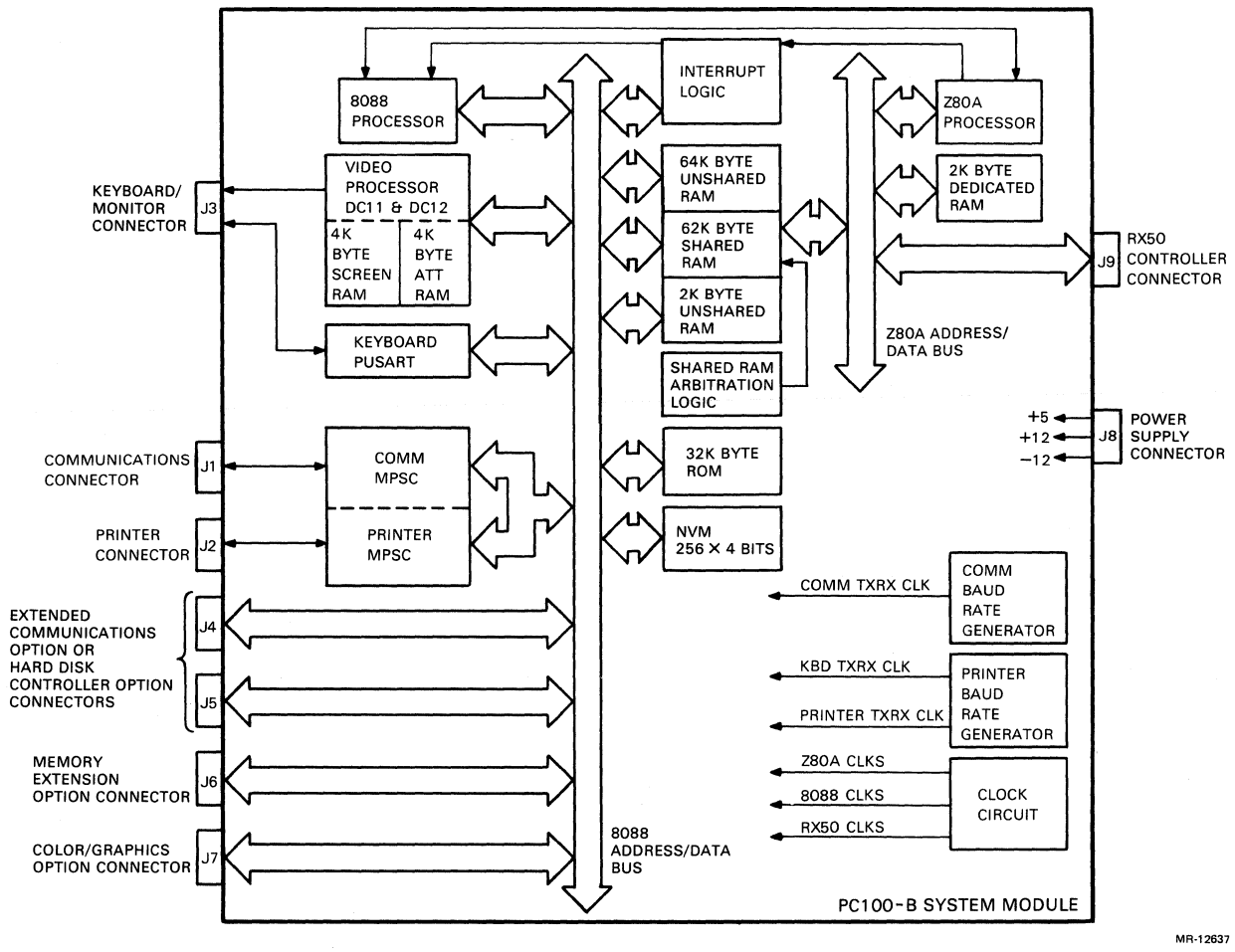


Figure 3-1 PC100-B System Module Block Diagram

Each microprocessor supports a portion of the system's function in addition to running 8-bit or 16-bit application/user software. The 8088 microprocessor (also referred to as the 8088 processor) controls the monitor, keyboard, communications connector, and all options added to the system. The 8088 processor communicates with its supporting logic and installed options via a 20-bit unidirectional address bus and an 8-bit bidirectional data bus.

The Z80A microprocessor (also referred to as the Z80A processor) transfers address/data and control signals to the RX50 controller, which uses these signals to read data from and write data to the dual-diskette drives. The Z80A processor communicates with its supporting logic and the RX50 controller via a 16-bit unidirectional address bus and an 8-bit bidirectional data bus.

The system module also contains two programmable baud rate generators, one for communications and one for the printer. The communications baud rate generator provides the transmitter and receiver clocks for the communications channel of the multiprotocol serial controller (MPSC). The user may independently program the transmitter and receiver clock baud rate for this channel programmer.

The printer baud rate generator provides the transmitter and receiver clocks for the printer channel of the multiprotocol serial controller (MPSC) and the keyboard PUSART. The transmitter and receiver clock

baud rates for the printer MPSC cannot be independently programmed. The printer baud rate generator also supplies the transmitter and receiver clocks for the keyboard PUSART at a fixed 4.8K baud rate.

The clock circuit on the system module provides three groups of clock pulses that are derived from the master crystal clock oscillator. The 8088 processor and its supporting logic use one group of clock pulses. The Z80A processor and its supporting logic use a second group of clock pulses. The RX50 controller logic uses a third group of clock pulses.

The system module includes the following features.

- 8088 microprocessor
- Z80A microprocessor
- 64K byte shared dynamic RAM
- 64K byte unshared dynamic RAM
- 2K byte Z80A dedicated RAM
- 32K bytes or 64K bytes ROM
- 256 × 4 bit (NVM)
- DC011, DC012 video processor
- 4K byte screen RAM
- 4K byte attribute RAM
- Asynchronous/bisynchronous communications port
- Printer port
- Keyboard interface
- RX50 controller interface
- Option expansion capability

  - Extended communications
  - Color/graphics
  - Extended memory (64K bytes to 768K bytes)
  - Hard disk controller

3.3 PHYSICAL DESCRIPTION

The system module is a modified quad module which is 35.56 cm (14 in) long, 26.42 cm (10.4 in) wide, and 2.25 cm (0.9 in) high. The module height is the combined thickness of the printed circuit board and printed circuit board connectors. A metal and plastic back panel attached to the rear of the printed circuit board contains three rectangular holes for the module connection to external devices and eight round holes for viewing the diagnostic lights. The back panel also contains four thumbscrews that secure the system module to the system unit.

The system module contains nine connectors of three different types.

1. Three D-type connectors mounted on the rear edge of the system board provide the external connections to the communications device, printer, and keyboard/monitor.

2. The input dc power connector is a 13-pin in-line connector with one of the pins removed to provide a locating key.

3. The remaining five connectors are dual-row headers and directly connect the system module to the RX50 controller module, the memory extension option, the extended communications option or the hard disk controller, and the color/graphics option. The RX50 controller module and option modules are secured by plastic standoffs located at appropriate places on the system module.

Figure 3-2 shows the locations of the connectors, the main logic elements, diagnostic lights, and manufacturing test/configuration jumpers.

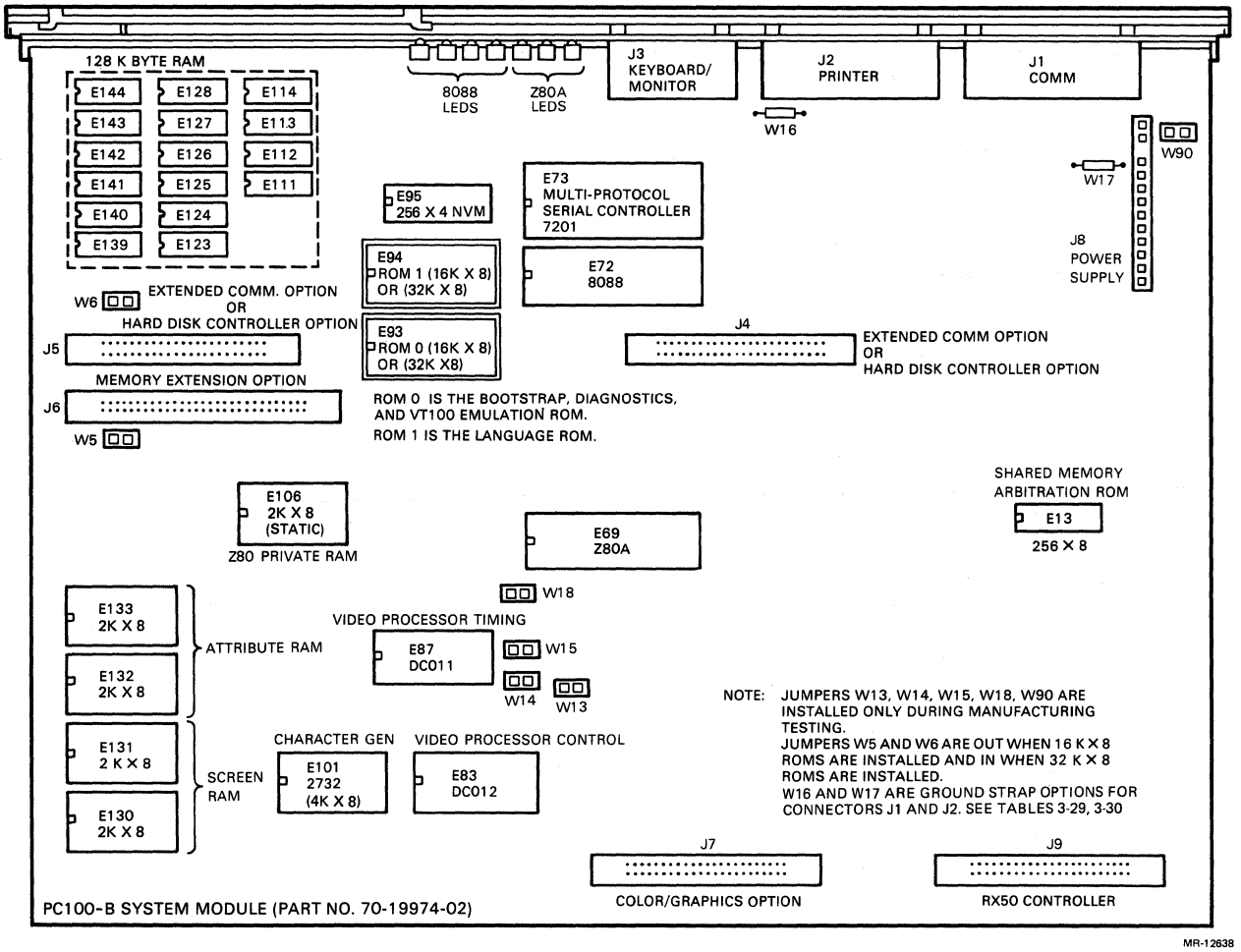


Figure 3-2 PC100-B System Module Physical Layout

3.4 SYSTEM MODULE FUNCTIONAL DESCRIPTION

The functions the 8088 and Z80A processors and their support circuits perform are described in this section. If you need detailed information on the 8088 or Z80A processors (not provided in this manual), refer to the manuals listed in Paragraph 1.4.

All illustrations in this chapter are functional block diagrams. Logic symbols on the block diagrams indicate function and may not represent circuitry. The sheet number inside the functional block refers to the sheet number of the circuit schematic set where the logic circuits are located.

3.4.1 System Module Address and Data Buses

The system module has two primary address and data buses: one for each of the 8088 and Z80A microprocessors over which they operate and transfer data to/from their supporting logic, I/O devices, and the shared/unshared memory. The system module also contains many secondary address and data buses. These secondary buses transfer data between the primary address and data buses and the video processor or shared memory logic. Figure 3-3 shows the primary and secondary address and data buses and their relation to the main logic elements on the system module.

3.4.1.1 8088 Address and Data Buses – The 8088 processor address A<19:0> and data BAD<7:0> buses support the monitor, keyboard and communications interfaces, options, the video processor, the shared memory logic, and the 8088 processor control logic. Latch and combine the AD<7:0> and

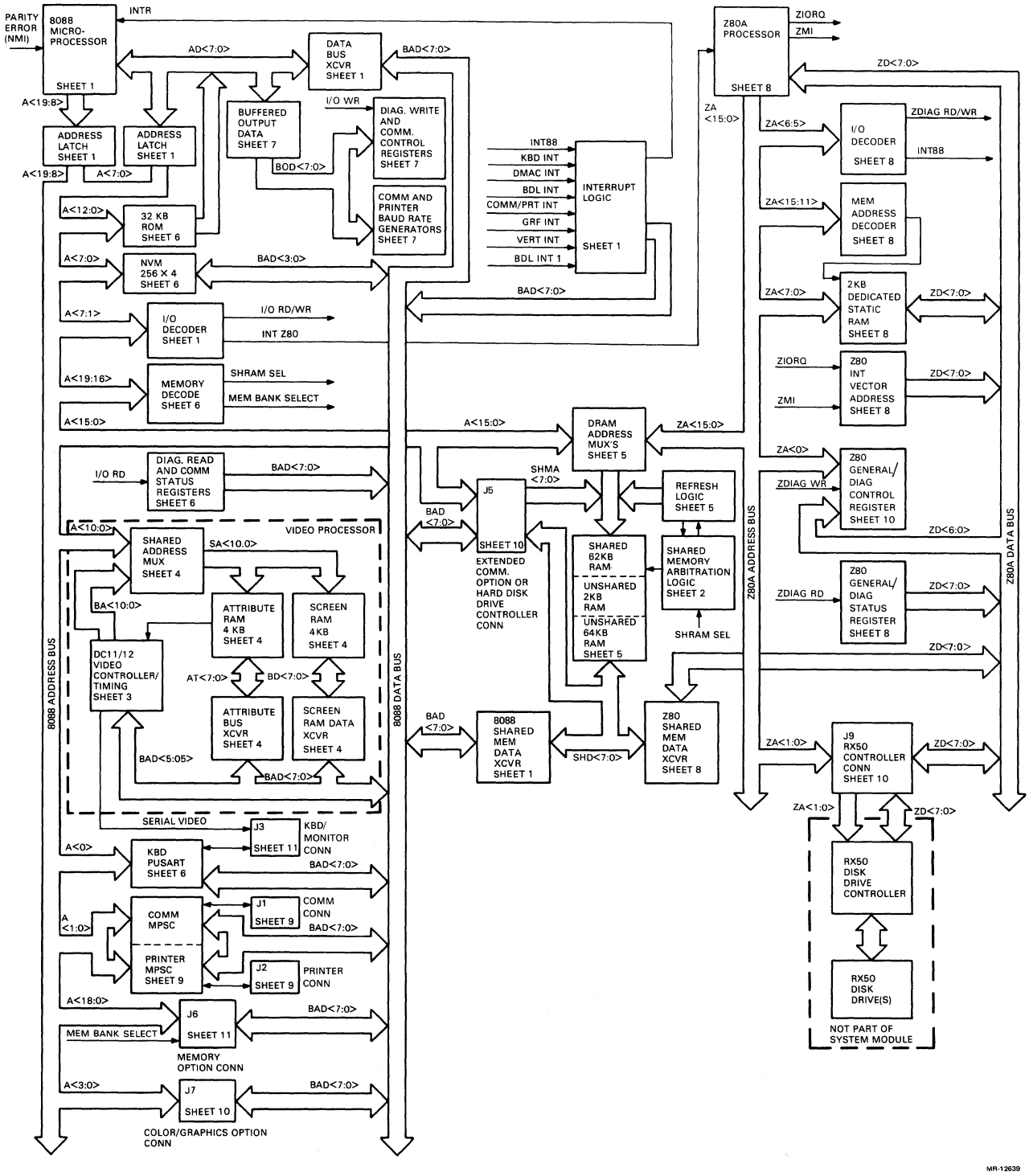


Figure 3-3 PC100-B System Module Address and Data Buses

A<19:8> bits from the 8088 processor to obtain the address bus, which is a 20-bit unidirectional bus. The address and data bus AD<7:0> connecting the 8088 processor with the address latch, output data buffer, 32K byte ROM, and the data bus transceiver is bidirectional for data transfers and unidirectional for address cycles.

3.4.1.2 Z80A Address and Data Buses – The Z80A processor address ZA<15:0> and data ZD<7:0> buses support the RX50 controller, the 2K byte RAM, and the Z80A control logic. The address bus is a 16-bit unidirectional bus which accesses 62K bytes of the 64K byte shared RAM through a DRAM address multiplexer. The data bus ZD<7:0> is an 8-bit bidirectional bus which transfers data to/from the 62K byte shared memory through the Z80A shared memory data transceiver.

3.4.1.3 Buffered Output Data Bus – Buffer the address and data AD<7:0> bits from the 8088 processor to obtain the buffered output data bus BOD<7:0> which is a unidirectional bus. The BOD bus supplies the bits to the communications control register, diagnostic write register, communications baud rate generator, and printer baud rate generator. It is pulled up to +5 volts to guarantee a sufficiently high (1) logic voltage level for the communications baud rate generator.

The 8088 processor uses this bus to write modem control and diagnostic error information into the communications register, diagnostic control information into the diagnostic register, and programming baud rates into the baud rate generators.

3.4.1.4 Video Processor Shared Address Bus – The shared address bus SA<10:0> is a unidirectional bus that accesses the 4K byte screen RAM and the 4K byte attribute RAM in the video processor subsystem. Multiplex the 8088 processor address A<10:0> and the buffered address BA<10:0> bits from the video processor to obtain the SA<10:0> bits.

The 8088 processor uses the bus to access the screen and attribute RAMs to store the character and attribute information to be displayed on the screen.

The video processor uses this bus to retrieve the stored character and attribute information by direct memory accesses to the screen and attribute RAMs.

3.4.1.5 Video Processor Buffered Address Bus – The video processor uses the buffered address bus BA<10:0> to access the screen and attribute RAMs to retrieve character and attribute information to be displayed on the screen.

3.4.1.6 Video Processor Attribute Bus – The attribute bus AT<7:0> is a bidirectional data bus that carries character, line, and screen attributes. The video processor only uses the four least significant bits.

The 8088 processor uses the AT bus to store the attributes in the attribute RAM. The PC100-B firmware obtains the default attribute information from the nonvolatile memory (NVM) via the BAD<7:0> bus and attribute RAM data transceiver.

The video processor uses the AT bus to retrieve the four least significant bits from the attribute RAM and then uses these bits to specify the attributes of the character, line, and screen display.

3.4.1.7 Video Processor Buffered Data Bus – The 8088 processor and the video processor use the buffered data bus BD<7:0>, which is a bidirectional data bus. The 8088 processor uses this bus to store an ASCII coded representation of a character to be displayed in the screen RAM. The 8088 processor obtains this character via the BAD<7:0> bus and screen RAM data transceiver.

The video processor uses this bus to retrieve the stored ASCII encoded character by direct memory accesses to the screen RAM, and then converts the data into an electrical signal that the monitor displays as letters, numbers, and symbols.

3.4.1.8 Shared Memory Address Bus – The 8088 and Z80A processors, the extended communications option or the hard disk drive controller, and the refresh logic use the shared memory address bus SHMA<7:0> which is an 8-bit unidirectional bus to access the 128K byte shared/unshared RAM. The 8088 address A<15:0> and Z80A address ZA<15:0> bits are transferred to the shared memory address bus through two DRAM address multiplexers that are controlled by the shared memory arbitration logic. The shared memory arbitration logic continuously monitors and establishes the priority for the devices using the SHMA<7:0> bus.

3.4.1.9 Shared Data Bus – The 8088 and Z80A processors and the extended communications option or the hard disk drive controller use the shared data bus SHD<7:0> which is a bidirectional bus to transfer data to and from the 128K byte shared/unshared RAM. The 8088 data BAD<7:0> and Z80A data ZD<7:0> bits are connected to their respective shared memory data transceivers. The control signals from the 8088 and the Z80A processors determine the direction and gating of the data bits through the 8088 and Z80A transceivers. The shared memory arbitration logic continuously monitors the devices and establishes priority for devices using the SHD<7:0> bus.

3.4.2 PC100-B System Module Clocks

The clock circuit logic on the system module generates three groups of clock pulses that determine the basic timing of the Rainbow computer. These three groups are derived from a crystal controlled oscillator that oscillates at 24.0734 MHz.

The first group of 4.815 MHz clock pulses runs the 8088 microprocessor and its support logic. The second group of 4.012 MHz clock pulses runs the Z80A microprocessor and its supporting logic. The third group of clock pulses at 8 MHz, 4 MHz, 1 MHz, and 500 kHz for the data separator's use, write precompensation, and diagnostic circuits in the RX50 controller module.

3.4.3 8088 Processor

The 8088 is a high performance processor implemented in N-channel, depletion load, silicon gate technology (HMOS). It is mounted in a 40-pin dual in-line (DIP) package. The processor has attributes of both 8- and 16-bit processors.

The 8088 processor features a time-multiplexed address and data bus that permits some pins to serve dual functions. It can be operated in one of two modes (minimum or maximum) depending on the strapping of a single input pin to ground or +5 Vdc. The 8088 processor operates in the minimum mode in all models of the Rainbow computer.

The 8088 processor has two processing units: the execution unit (EU) and the bus interface unit (BIU).

The EU executes all instructions, provides data and addresses to the BIU, and manipulates the eight general registers and a flag register. Except for a few control pins, the EU is completely isolated from the external support logic.

The BIU executes all external bus cycles. The BIU controls six segments and two communications registers, the instruction pointer register, and the 4-byte instruction object code queue. The BIU combines segment and offset values in its dedicated adder to derive 20-bit addresses, transfers data to and from the EU on the arithmetic logic unit (ALU) data bus, and loads instructions into the instruction queue.

When the EU is ready to execute an instruction, it fetches the instruction object code byte from the BIU's instruction queue and then executes the instruction. If the queue is empty, the EU waits for the instruction byte to be fetched. In the course of instruction execution, if a memory location or I/O port must be accessed, the EU requests the BIU to perform the required bus cycle.

The two processing sections of the processor operate independently. When one byte of the 4-byte queue is empty, the BIU executes an instruction fetch cycle. The 8088 processor accesses one instruction object code byte per bus cycle. If the EU issues a request for bus access while the BIU is processing an instruction fetch bus cycle, the BIU completes the cycle before honoring the EU's request.

8088 Pin Description – The 40 pins of the 8088 processor are divided into six functional groups.

1. Address bus
2. Address/status bus
3. Address/data bus
4. Bus control outputs
5. Processor control inputs
6. Power inputs

The voltage level (Vcc or ground) applied to the minimum/maximum mode input (pin 33) defines the function of many 8088 control pins. Three of the 40 available pins of the 8088 processor are not used in Rainbow computers. Tables 3-1 and 3-2 describe the pin functions.

Table 3-1 8088 Processor Pin Descriptions

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
9–16	AD7–AD0	AD7–AD0	I/O	ADDRESS DATA BUS: These lines are the time multiplexed memory/IO address (T1) and data (T2, T3, TW, and T4) bus. These lines are active high and float to 3-state off during interrupt acknowledge.
2–8,39	A15–A8	A15–A8	O	ADDRESS BUS: These lines provide address bits 8–15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active high and float to 3-state off during interrupt acknowledge.
38	A16	A16/S3	O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown in Table 3-2. This information indicates which segment register is currently being used for data accessing.
37	A17	A17/S4	O	
36	A18	A18/S5	O	
35	A19	A19/S6	O	

*Indicates direction of signal with respect to the 8088 processor. (O = Output, I = Input)

Table 3-1 8088 Processor Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
32	RD88 L	RD	O	READ 88: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/M pin or S2. This signal is used to read devices that reside on the 8088 local bus. RD is active low during T2, T3, and TW of any read cycle, and is guaranteed to remain high in T2 until the 8088 local bus has floated.
22	READY H	READY	I	READY: This is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. This signal is active high. The 8088 READY input is not synchronized. When READY is active low, wait states (TW) are added to the 8088 bus cycle.
18	INTR H	INTR	I	INTERRUPT REQUEST: This is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active high.
23	COMM/PRT INTR L	TEST	I	COMMUNICATION/PRINTER INTERRUPT REQUEST: Input is examined by the "wait for test" instruction. If the COMM/PRT INTR input is low, execution continues; otherwise, the processor waits in an idle state. This input is synchronized internally during each clock cycle on the leading edge of CLK88 H.
17	PARITY ERROR L	NMI	I	PARITY ERROR: This is a nonmaskable interrupt input from the memory extension option. It is active low when a parity error occurs. The edge triggered input causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. Parity error is not maskable internally by software.

*Indicates direction of signal with respect to the 8088 processor. (O = Output, I = Input)

Table 3-1 8088 Processor Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
				The transition of the parity error signal from HIGH to LOW initiates the interrupt at the end of the current instruction. This input is internally synchronized.
21	RESET H	RESET	I	RESET: This causes the processor to immediately terminate its present activity. The signal must be active high for at least four clock cycles. It restarts execution when RESET returns low. RESET is internally synchronized.
19	CLK88 H	CLK	I	CLOCK 8088: This provides the basic timing for the processor. It is asymmetric with a 33% duty cycle to provide optimized internal timing. The frequency of the clock signal is 4.815 MHz.
40	+5 V	Vcc		VCC: This is the +5 V power input.
1,20	GND	GND		GND: These are the ground pins.
33	MN/MX	MN/MX	I	MINIMUM/MAXIMUM: This determines the operating mode of the processor. A low on MN/MX selects maximum mode. A high on MN/MX selects minimum mode. This signal is tied to +5 V through a 330 ohm resistor in the Rainbow computer.
28	IO/M	IO/M	O	INPUT OUTPUT/MEMORY: This status line is used to distinguish a memory access from an I/O access. IO/M becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = high, M = low).
29	WR88 L	WR	O	WRITE 88: Strobe indicates that the processor is performing a write memory or write I/O cycle depending on the state of the IO/M signal. WR88 L is active for T2, T3, and TW of any write cycle. It is active low.
24	INTAL	INTA	O	INTERRUPT ACKNOWLEDGE: This is used as a read strobe for interrupt acknowledge cycles. It is active low for T2, T3, and TW of each interrupt acknowledge cycle.

*Indicates direction of signal with respect to the 8088 processor. (O = Output, I = Input)

Table 3-1 8088 Processor Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
25	ALE H	ALE	O	ADDRESS LATCH ENABLE: This is provided by the processor to latch the address into the address latches. It is a high pulse active during T1 of any bus cycle. ALE is never floated.
27	DT/R	DT/R	O	DATA TRANSMIT/RECEIVE: This is used to control the direction of data flow through the 8088 data transceivers. The timing of this signal is the same as IO/M (T = high, R = low).
26	DEN L	DEN	O	DATA ENABLE: This is an output enable for the AD<7:0> data bus transceiver and the video processor data transceivers. The signal is active low during each memory and I/O access, and for interrupt acknowledge (INTA) cycles. For a read or INTA cycle, it is active from the middle of T2 until the middle of T4. For a write cycle, it is active from the beginning of T2 until the middle of T4.
31		HOLD	I	HOLD: When active high, this signal indicates that another bus master is requesting a local bus hold. This signal is not used in the Rainbow computer and is tied to ground (low).
30		HLDA	O	HOLD ACKNOWLEDGE: This signal is active high to acknowledge a HOLD request to the processor. This signal is not used by the Rainbow computer.
34		SSO	O	STATUS LINE: The combination of SSO, IO/M, and DT/R allows the system to completely decode the current bus cycle. This signal is not used in the Rainbow computer.

*Indicates direction of signal with respect to the 8088 processor. (O = Output, I = Input)

Table 3-2 Segment Register Status Encoding

S4*	S3	Characteristics
0 (Low)	0	Alternate data
0	1	Stack
1 (High)	0	Code or none
1	1	Data

*S6 is 0 (low).

3.4.4 Z80A Microprocessor

The Z80A is an 8-bit parallel processor mounted in a 40-pin dual in-line package. It has a 16-bit unidirectional address bus and an 8-bit bidirectional data bus for interfacing to 62K bytes of shared RAM, 2K bytes of dedicated RAM, the RX50 controller, and supporting logic. All output signals are fully decoded and timed to control the memory and RX50 controller.

The Z80A processor has internal registers that contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets (main or alternate) of six general purpose registers, which can be used individually as either 8-bit registers or 16-bit pairs. In addition, there are two sets (main or alternate) of accumulator and flag registers. A group of exchange instructions make both sets of main or alternate registers accessible to the programmer.

The Z80A processor also contains an additional set of six registers with assigned functions. Four of these are 16-bit registers: one for the stack pointer, one for the program counter, and two for indexed addressing. The Z80A processor also has two 8-bit registers: the interrupt register and the 8-bit refresh register.

The 4.012 MHz clock pulses from the system module clock circuit provide the basic timing for the Z80A.

The Z80A processor requires only a single +5 V power supply source.

Z80A Pin Description – The 40 pins of the Z80A processor are divided into seven functional groups.

1. Address bus (16 pins)
2. Data bus (8 pins)
3. System control (6 pins)
4. Processor control (5 pins)
5. Processor bus control (2 pins)
6. Processor timing (1 pin)
7. Power (2 pins)

The Z80A processor as implemented in Rainbow 100 computers does not require the functions provided by all of the 40 pins. The Rainbow computers use only 36 of the 40 pins. The pin functions are described in Table 3-3.

Table 3-3 Z80A Microprocessor Pin Description

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
1–5, 30–40	ZA<15:0>	A0–A15	O	ADDRESS BUS: ZA<15:0> form a 16-bit address bus. The address bus provides the address for memory data bus exchanges and I/O device exchanges.
23		BUSACK	O	BUS ACKNOWLEDGEMENT: This indicates to the requesting device that the address bus, data bus, and control signals have entered their high-impedance states. This signal is not used by Rainbow computers.
25	BUSREQ	BUSREQ	I	BUS REQUEST: This signal, when active (low), forces the Z80A processor address bus, data bus, and control signals to go to a high-impedance state so that other devices can control these lines. This signal is always inactive in the Rainbow computer. It is tied to +5 V through a 4.7K resistor.
6	ZPHI L	CK	I	CLOCK: This provides the basic timing for the Z80A processor. It is a symmetrical clock signal with a frequency of 4.012 MHz.
7–10 12–15	ZD<7:0>	D0–D7	I/O	DATA BUS: This is the 8-bit bidirectional bus used for data exchanges with memory and I/O devices.
29	GND	GND		GROUND: This is the Z80A ground pin.
18		HALT	O	HALT STATE: When active (low), this signal indicates that the Z80A processor has executed a Halt instruction and is awaiting either a nonmaskable or a maskable interrupt before operation can resume. This signal is not used in the Rainbow computer.

* Indicates direction of signal with respect to the Z80A processor (O = Output, I = Input)

Table 3-3 Z80A Microprocessor Pin Description (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
16	INTZ80 L	INT	I	INTERRUPT REQUEST: This is the interrupt request from the 8088 processor. The Z80A processor honors this request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop is enabled.
20	ZIORQ L	IORQ	O	INPUT/OUTPUT REQUEST: When low, this signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. ZIORQ L is also generated concurrently with ZMI L during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.
27	ZMI L	MI	O	MACHINE CYCLE ONE: ZMI L, together with ZMREQ L, indicates that the current machine cycle is the operation code fetch cycle of an instruction execution. ZMI L, together with ZIORQ L, indicates an interrupt acknowledge cycle.
19	ZMREQ L	MREQ	O	MEMORY REQUEST: When LOW, ZMREQ L indicates that the address bus holds a valid address for a memory read or memory write operation.
17	NMI	NMI	I	NONMASKABLE INTERRUPT: This signal is not used in Rainbow computers. It is tied to +5 V through a 4.7K ohm resistor to hold it inactive (high).
21	ZRD L	RD	O	MEMORY READ: When low, this signal indicates that the Z80A processor wants to read data from memory or an I/O device. The addressed memory or I/O device uses this signal to gate data on the ZD<7:0> bus.

* Indicates direction of signal with respect to the Z80A processor (O = Output, I = Input)

Table 3-3 Z80A Microprocessor Pin Description (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
26	ZRESET L	RESET	I	RESET: When low, ZRESET L initializes the Z80A processor as follows: it resets the interrupt enable flip-flop, clears the PC and the I and R registers, and sets the interrupt status to mode 0. During reset time, the address and data bus go to a high impedance state, and all control output signals go to the inactive state.
28	ZRFSH L	RFSH	O	REFRESH: This signal is active low. ZRFSH L together with ZMREQ L indicates that the lower 7 bits of the system's address bus can be used as a refresh address to the system's dynamic memories.
24	ZWAIT L	WAIT	I	WAIT: ZWAIT L indicates to the Z80A processor that the addressed memory or I/O device is not ready for a data transfer. The Z80A processor continues to enter a wait state as long as this signal is active low.
22	ZWR L	WR	O	MEMORY WRITE: When low, this indicates that the Z80A processor data bus holds valid data to be stored at the addressed location.
11	+5 V	Vcc		VCC: This is the +5 V power input.

* Indicates direction of signal with respect to the Z80A processor (O = Output, I = Input)

3.4.5 8088 Memory

The 8088 processor can use six types of memory.

1. 128K bytes dynamic memory (62K bytes shared)
2. 32 to 64K bytes ROM
3. 4K bytes video screen memory (static)
4. 4K bytes video attribute memory (static)
5. 256 × 4 NVM with shadow RAM
6. 64K bytes to 768K bytes optional unshared dynamic memory

3.4.5.1 Standard Memory – The 128K bytes of standard memory is partitioned into a low order 64K ytes bank and a high order 64K bytes bank. 62K bytes of the low order 64K bytes bank is addressable by, and therefore accessible to, the Z80A processor. The Z80A processor is unable to address and therefore cannot modify the first 2K bytes portion of this bank. Therefore, the 8088 processor keeps its interrupt vectors and some other information safe from a Z80A application.

The high order 64K byte bank of standard memory is accessible to the 8088 processor via the same memory bus as the lower 64K bytes of standard memory. It is not addressable by the Z80A processor, and thus is not shared, but the Z80A processor accesses to the low order 64K byte bank and uses the standard memory bus. When the 8088 processor accesses the high order 64K byte bank of standard memory at the same time the Z80A processor accesses the low order 64K byte bank, this causes the 8088 processors to incur wait states.

If there is no contention for the standard memory bus at the time of an 8088 access, no wait states are required for the cycle. If the bus is busy due to a refresh cycle, DMA cycle, or a Z80A memory cycle, which was initiated prior to the 8088 processor's request, wait states will occur until the request can be filled.

Refresh has the highest priority for memory cycles. DMA has the second highest priority for memory cycles. The processors have the lowest priority. The 8088 processor has approximately equal priority with the Z80A processor.

No parity generation/checking is implemented for the standard 128K byte memory.

3.4.5.2 ROM – The 8088 processor can address 32K bytes to 64K bytes of ROM (ROM 0 and ROM 1) on the module. ROM 0 contains code for diagnostics, bootstrap, and part of the VT102 emulation code. ROM 1 contains the remainder of the VT102 emulation code, and the language translation codes needed to support the various international language keyboards. The 8088 processor must move the code for the Z80A processor into shared memory in order to be executed by the Z80A processor. No wait states are required when the 8088 processor accesses this memory; however, because the circuitry assumes that all memory is dynamic RAM, wait states will be executed whenever refresh cycles are in progress. Supported ROMs have the same pin assignments as the 27128/27256 ROMs, with access times less than or equal to 450 nanoseconds (ns). Each ROM socket has a jumper associated with it to select the 27128 (128K bit) pin assignments or the 27256 (256K bit) pin assignments. The default condition is with jumpers W5 and W6 removed, and the 27128 (128K bit) type pin assignments selected.

3.4.5.3 4K Byte Screen RAM and 4K Byte Attribute RAM – The video or 8088 processor can access the screen RAM and the attribute RAM. The 8088 processor uses these memories to temporarily store the character and attribute (character, line, and screen) data to be displayed on the screen. The video processor directly accesses the memories (DMA) via its address bus to retrieve the stored character and attribute data and then converts the data into a video signal that the monitor uses to produce the screen display. The parts of this memory not used for the video display are used for firmware variables.

3.4.5.4 256 × 4 Bit NVM – The PC100-B system module contains 1024 bits of nonvolatile storage that is organized 256 × 4 bits. The NVM is located on the 8088 bus at address OEDOOOH–OEDOFFH and the data path to the NVM is through data bits 0, 1, 2, and 3. Phantom images of the NVM exist from address OECOOOH–OECFFFH, and OED1OOH–OEDFFFH.

The device contains a 256 × 4 bit static RAM that performs as any other static memory. The NVM also contains a 256 × 4 bit nonvolatile memory that is overlaid with the 256 × 4 bit static memory. On initialization, the 8088 processor does a RECALL of the NVM which places that data into the static memory. At this time, any read or write to the memory occurs to the static memory. The RECALL is done via a bit in the diagnostic write register. On power-up, firmware sets the bit to a 0, and then to a 1 before data from the NVM RAM is available.

To perform a RECALL, set the bit to 0 and then set back to 1. The minimum width for this pulse is 450 ns. The data is available immediately after the RECALL bit is reset. The data in the static memory portion can be stored in the NVM by the 8088 processor via the PROGRAM NVM bit also located in the diagnostic write register. This bit is also set to 0 on power-up. To perform a PROGRAM NVM operation, the bit is set to 1 and then back to 0. This pulse has a minimum width of 100 ns. Once the PROGRAM NVM bit has met the minimum pulse width it can be removed, however, the 8088 processor cannot access the NVM for 10 milliseconds (ms). At this time, the device is storing the data into the NVM. Nothing indicates to the 8088 processor that the device is done other than 10 ms has passed. If another operation is done on the NVM during those 10 ms, it will be ignored. Once the operation is started, it cannot be terminated unless the power is turned off. In this case, data in the NVM is not valid.

3.4.5.5 Optional (Unshared) Dynamic Memory – The module can optionally be expanded with 64K bytes to 768K bytes of memory for the 8088 processor's use. If installed, this memory is always available and never requires wait states, except when the memory cycle contends with a refresh cycle.

3.4.5.6 8088 Memory Map – Figure 3-4 shows the 8088 memory map. The lower 64K bytes are shared with the Z80A processor as shown in Figure 3-5.

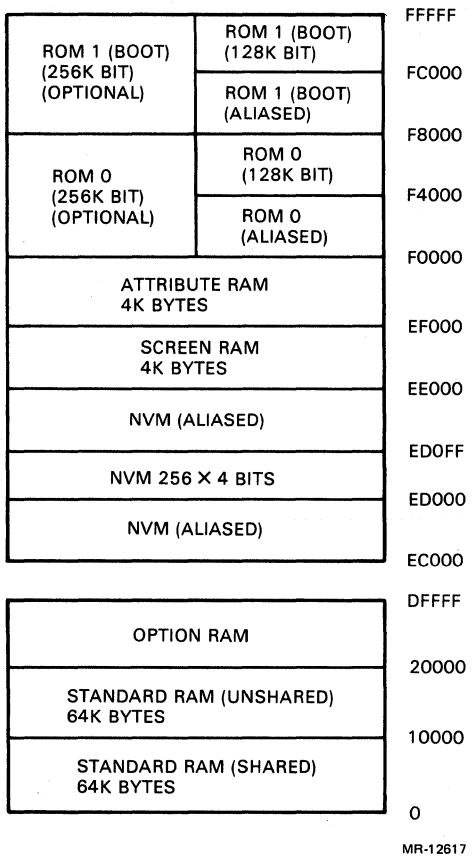


Figure 3-4 8088 Memory Map (PC100-B)

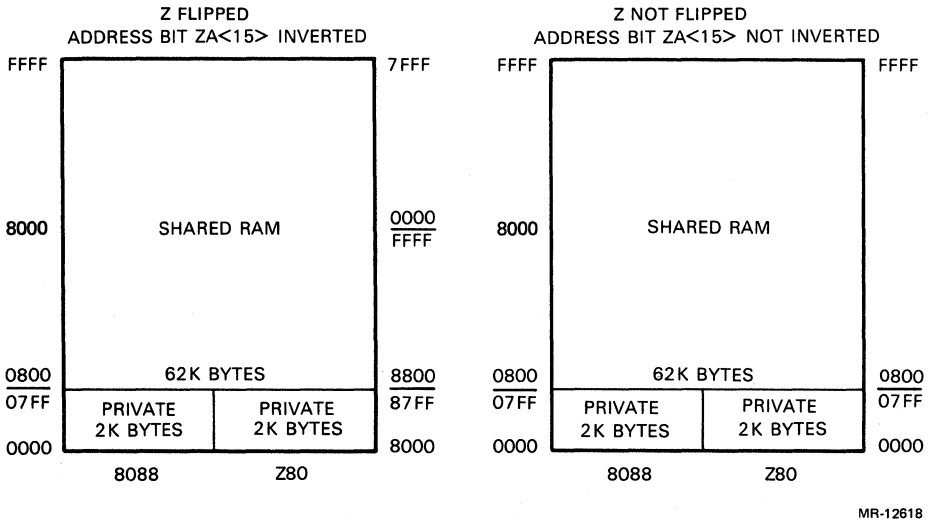


Figure 3-5 Z80A Memory Map and 8088 Low Memory Map

3.4.6 Z80A Shared Memory

The Z80A processor has available to it a 64K byte RAM that is divided into 62K bytes shared and 2K bytes unshared memory. Accesses to the shared portion of memory select the corresponding address in the standard bank of 64K byte RAMs. Accesses to the unshared memory select a private 2K × 8 byte-wide static RAM.

If the shared RAM is busy at the time of a Z80A access, the Z80A processor will execute wait states until the RAM is free. The RAM is considered busy when an 8088 cycle or a refresh cycle is in progress or is pending. In addition to wait cycles due to contention, all machine cycle #1 (M1) cycles from the shared RAM have one extra wait cycle due to the timing for this sort of machine cycle.

In any case, the Z80A processor is held in a wait state for no longer than approximately two microseconds. If both processors are executing out of the shared memory, the Z80A processor cannot reliably access the floppy disk. For example, lost data errors will often result.

3.4.6.1 Z80A Private RAM – The Z80A processor may access the 2K byte of unshared RAM (static) at any time without any wait states.

3.4.6.2 Z80A Memory Map–Figure 3-5 shows the Z80A memory map. The Z80A memory addresses are remapped in the 62K byte shared RAM and the 2K byte Z80A dedicated RAM when address bit ZA<15> is inverted. Write to the diagnostic write register at address 21H to invert the ZA<15>.

3.4.7 I/O Decoders

The system module contains two sets of I/O decoders that the 8088 and the Z80A processors use to select and control the transfer of data through the I/O ports. The 8088 and Z80A I/O decoders are described in the following paragraphs.

3.4.7.1 8088 I/O Decoders – The 8088 processor uses three I/O decoders to supply read/write control signals to various registers and select signals to the communications/printer serial controller, the keyboard PUSART, the color/graphics option, the extended communications option, and the hard disk drive controller. The three decoders are the I/O read decoder, the I/O write decoder, and the I/O port select decoder. Table 3-4 lists the addresses decoded by the 8088 I/O decoders.

Table 3-4 8088 I/O Addresses

Address (Hexadecimal)	Function	Type*
00H	Interrupts Z80A flop (Write)	WO
00H	Clears 8088 interrupt flop (Read)	RO
02H	Communications and LED register	WO
02H	General communications status	RO
04H	DC011 write register	WO
06H	Communications baud rate register	WO
08H	Option present status register	RO
OAH	Maintenance port	WO
0AH	Maintenance port	RO
0CH	DC012 write register	WO
OEH	Printer baud rate register	WO
10H	Keyboard data register (8251A)	R/W
11H	Keyboard control/status register (8251A)	R/W
20H–2FH	Extended communications option/option select 1	R/W
30H–3FH	Extended communications option/option select 3	R/W
40H	Comm data register (MPSC)	R/W
41H	Printer data register (MPSC)	R/W
42H	Comm control/status register (MPSC)	R/W
43H	Printer control/status register (MPSC)	R/W
5H0–5FH	Graphics option select	R/W
60H–6FH	Extended communications option/option select 2	R/W
70H–7FH	Extended communications option/option select 4	R/W

*WO = Write Only, RO = Read Only, R/W = Read/Write

3.4.7.2 Z80A I/O Decoders – The Z80A processor uses two I/O decoders to supply read/write control signals to nine status and control registers for the RX50 disk drive. These registers are located both on the system module and the RX50 controller module. The read/write control signals for the status and control registers located on the RX50 controller module are routed through the RX50 controller connector (J9). The decoders also supply interrupt control signals for the Z80A and the 8088 processors.

Table 3-5 lists the addresses decoded by the Z80A I/O decoders.

Table 3-5 Z80A I/O Addresses

Address* (Hexadecimal)	Function	Type†
00H	Clear interrupt to Z80A (Read)	RO
00H	Interrupts 8088 (Write)	WO
20H	Set ZFLIP	WO‡
21H	General/diagnostic status register	RO
21H	General/diagnostic control register	WO‡
40H	Diskette status register	RO
40H	Disk control register	WO
60H	FDC status register	RO
60H	FDC control register	WO
61H	FDC track register	R/W
62H	FDC sector register	R/W
63H	FDC data register	R/W

* The above Z80A I/O ports have many alias addresses throughout the Z80A's 256 I/O port address space. Prudent programming practice precludes using any Z80A I/O port address that is not defined above.

† WO = Write Only, RO = Ready Only, R/W = Read/Write

‡ Writing Diagnostic Write Register at address 21H will reset ZFLIP. Writing the Diagnostic Write Register at address 20H will set ZFLIP. Inadvertent use of these registers will likely cause program problems.

3.4.8 Interrupts

The 8088 processor accepts maskable interrupts from eight sources according to priority levels assigned to each interrupting source and one nonmaskable interrupt from the optional memory extension modules. The only interrupt source for the Z80A processor is the interprocessor interrupt from the 8088 processor. When the 8088 or the Z80A processor receives an interrupt request, the interrupted processor will complete execution of the current instruction and then jump to the interrupt service routine for the interrupting source.

3.4.8.1 8088 Interrupts – Software or hardware can initiate 8088 interrupts. Software interrupts originate directly from program execution or indirectly through program logic. Hardware interrupts originate from external logic and are classified as either maskable or nonmaskable. All interrupts, whether initiated by software or hardware, result in transfer of control to an interrupt service program.

The maskable hardware interrupts to the 8088 processor come from the following sources.

- Interprocessor interrupt from the Z80A processor
- Keyboard
- Communications or printer MPSC
- Video controller (DC12)
- Optional color/graphics module
- Optional extended communications module or the RD51 hard disk drive controller

The memory extension option asserts the nonmaskable hardware interrupt (NMI) to the 8088 processor when it detects a parity error. The NMI causes the 8088 processor to display an error message on the screen and then halt. To restart the 8088 processor after receiving an NMI, you enter Set-Up and reset the system.

When the 8088 processor accepts an interrupt request, it acknowledges the interrupt and gates interrupt type bits onto the BAD<7:0> bus. The 8088 processor uses the interrupt type bits as pointers to the interrupt vector addresses. The PC100-B system module supports hardware controlled relocation of the 8088 hardware interrupt vectors to accommodate the requirements of different operating systems. The VECTOR SEL control line is used for this purpose. Table 3-6 describes the 8088 interrupt vector addresses. Values given are in hexadecimal. The values are listed for VECTOR SEL = 1 (default condition), and VECTOR SEL = 0 (relocated vectors).

Table 3-6 8088 Processor Interrupt Vector Addresses

Priority Level*	Mnemonic	Interrupt Source	Interrupt Type Vector SEL (1)	Interrupt Type Vector SEL (0)	Interrupt Address Vector SEL (1)	Interrupt Address Vector SEL (0)
NMI	PARITY ERROR L	Memory extension option	02	02	08	08
7	VERT INTR L	DC012 video controller	20	A0	80	280
6	BDL INTR1L	Extended communications option	21	A1	84	284
5	GRF INTR L	Color/Graphics option	22	A2	88	288
4	DMAC INTR L	Extended communications option (DMA controller)	23	A3	8C	28C
3	COMM/PTR INTR L	Comm/Printer MPSC	24	A4	90	290
2	BDL INTR L	Extended communications option or RD51 hard disk controller	25	A5	94	294
1	KBD INT L	Keyboard (PUSART)	26	A6	98	298
0	INT88 L	Interrupt from Z80A	27	A7	9C	29C

*7 = Highest, 0 = Lowest

The VECTOR SEL control bit relocates the hardware interrupt vector space to accommodate the requirements of different operating systems. The VECTOR SEL bit is implemented as VECTOR SEL L, using the DTR L output of the keyboard PUSART. (See Paragraph 3.4.16)

3.4.8.2 Z80A Interrupts – Only the 8088 processor can interrupt the Z80A. When the Z80A processor accepts the interrupt it will complete execution of the current instruction and then initiate an interrupt request/acknowledge cycle. During this cycle, the Z80A processor asserts control signals that enable the Z80A interrupt vector encoder to gate the Z80A interrupt vector address onto the ZD<7:0> bus.

The interrupt vector address (F7H) placed on the bus is hardwired into the Z80A interrupt vector encoder. The F7H interrupt vector address causes the Z80A processor to perform an RST 30 instruction in interrupt mode 0.

3.4.9 Video Processor

The video processor is a subsystem of the system module that converts data from the 8088 processor into a composite video signal that the monitor uses to display letters, numbers, and symbols. The video processor subsystem comprises two central devices (the DC11 video timing and DC12 video control chips), the screen RAM, attribute RAM, a 4K × 8 bit character generator ROM, and supporting logic.

The 8088 processor stores ASCII encoded character data to be displayed in the screen RAM and attribute data in the attribute RAM. The video processor then retrieves the character data and attribute data one line at a time, by direct memory accesses (DMAs), to the screen and attribute RAMs. The character data is converted into streams of pulses, modified according to the attributes selected. The pulses are sent to the monitor where they are converted into light to form characters on the screen. The DC11 and DC12 custom ICs provide the complex timing and control signals necessary to convert the ASCII data into the composite video signal required by the monitor.

The video processor subsystem supports the following features.

- 24 × 80 or 24 × 132 column display
- Smooth scrolling (full screen and split screen)
- Jump scrolling (full screen and split screen)
- Double-height lines
- Double-width lines
- Reverse video
- Bold characters
- Underlined characters
- Blinking characters
- Block or underline blinking cursor
- A 255 ROM-resident character set
- Composite video output

The video processor can also modify various attributes of the monitor display. The DC11 and DC12 chips perform these functions. Three groups of attributes apply to the Rainbow computer display: screen, line, and character.

The screen attributes affect the characteristics of the entire screen area. The NVM stores the attributes. During Set-Up, power-up, or reset, the 8088 processor reads the Set-Up specifications and writes them into the DC11 and DC12 chips via the BAD<7:0> bus to establish the screen attributes. The screen attributes include the following.

- Jump or smooth scrolling
- 80- or 132-column screen width
- Dark or light screen background
- 50 Hz or 60 Hz screen refresh rate

Line attributes affect the characteristics of all characters on a single line of the screen. Software selects these attributes line-by-line. These attributes include the following.

- Single-width characters
- Double-width characters
- Double-height and double-width characters
- Scroll to indicate that the line is in a scrolling or nonscrolling area of the display

Software selects character attributes character-by-character to affect the appearance of characters displayed on the screen. The attributes can be selected separately or in any combination. The character attributes include the following.

- Underlined character
- Reversed video character
- Bold character (increased intensity)
- Blinking character

3.4.9.1 8088 Processor Video-Processor Interface – The 8088 processor communicates with the video processor in the following three ways.

1. During Set-Up, the 8088 processor reads the Set-Up specifications and writes them into the DC11 and DC12 chips to establish the screen attributes.

2. The contents of the screen RAM and the attribute RAM directly control the line and character display. These RAMs contain the displayable characters, character attributes, line attributes, and addresses that link one line of characters to the next.

3. During smooth scrolling, the 8088 processor updates the scroll latch in the DC12 control chip.

3.4.9.2 Screen RAM and Attribute RAM – The screen RAM and attribute RAM store the character and attribute data for display on the screen. The RAMs are organized according to the Set-Up screen width specifications. The RAMs can hold 24 lines of 80 or 132 characters and their line/character attributes.

The 8088 processor accesses these RAMs to read and write data 90 percent of the time. For the remaining time, the video processor takes full control of these memories to retrieve and process the data for display. When the video processor controls the memories, it holds the 8088 processor in a wait state and provides its own addresses BA<10:0> to directly access the memories (DMA) to retrieve the stored data. The video processor needs the fast access the DMA provides because the data rate required to display a line of characters is greater than the 8088 processor can handle.

Both the 8088 and the video processors access the 4K byte screen RAM and the 4K byte attribute RAM through a shared address multiplexer. The 8088 processor stores each character in a line in one of a group of adjoining locations in the screen RAM. The attribute RAM stores the character and line attributes in adjoining locations. The video processor only looks at the four least significant bits of the character attribute bytes.

The screen and attribute addresses access corresponding locations in adjacent 4K byte banks of the 8088 memory (Figure 3-4).

The screen RAM addresses access locations in the lower 4K byte bank and start at address EE000 H. The attribute RAM addresses access locations in the upper 4K byte bank and start at address EF000 H. Not all of the 8K bytes of the total memory are needed to store the characters and attributes for the video display. The firmware uses the remaining parts of the 8K byte memory for its variable storage.

3.4.9.3 DC11 Programming Information – The 8088 processor (write only) accesses the DC11 video timing chip via the BAD<5:4> bits at I/O address 04H. Program the DC11 chip with the desired refresh rate and column mode on power-up and after any mode changes. To program the DC11 chip, write two of the four command codes listed in Table 3-7.

Table 3-7 DC11 Command Codes

Code (Hexadecimal)	BAD<5>	BAD<4>	Configuration	Operation Performed
0 0	0	0	80-column mode	Sets interlaced mode
1 0	0	1	132-column mode	
2 0	1	0	60 Hz mode	Resets interlaced mode
3 0	1	1	50 Hz mode	

Interlaced/noninterlaced mode is determined by the order in which the 80/132 column and the 50/60 Hz refresh rate are set. When BAD<5> is low, the number of columns is programmed according to the state of BAD<4>. When BAD<5> is high, the refresh rate is programmed. Interlace mode is always selected when the column mode is set, and noninterlaced mode is selected when the refresh rate is set. The interlace mode used depends on whether the column mode or refresh mode was selected last.

Every time the DC11 chip is programmed, its internal timing chain is reset. Since this causes the screen display to jump, the DC11 should be programmed only if absolutely necessary. For example, the following two instructions set the DC11 to 80 column, 60 Hz, and no interlace.

```
1.  MOV AX,2000H
2.  OUT DC011,AX
```

NOTE

When 80-column mode is selected, the video processor can display 83 columns in single-width mode or 41 columns in double-width/double-height mode. When 132-column mode is selected, the processor can display 137 columns in single-width mode or 68 columns in double-width/double-height mode.

3.4.9.4 DC12 Programming Information – The 8088 processor (write only) can access the DC12 video control chip via the BAD<3:0> bits at I/O address 0CH. The four-bit command codes are defined for the DC12 chip in Table 3-8.

Table 3-8 DC12 Control Chip Command Codes

Code (Hexadecimal)	BAD 3	2	1	0	Result
0 0	0	0	0	0	Set scroll latch LSBs to 00
0 1	0	0	0	1	Set scroll latch LSBs to 01
0 2	0	0	1	0	Set scroll latch LSBs to 10
0 3	0	0	1	1	Set scroll latch LSBs to 11
0 4	0	1	0	0	Set scroll latch MSBs to 00
0 5	0	1	0	1	Set scroll latch MSBs to 01
0 6	0	1	1	0	Set scroll latch MSBs to 10
0 7	0	1	1	1	Set scroll latch MSBs to 11
0 8	1	0	0	0	Toggle blink flip-flop
0 9	1	0	0	1	Clear vertical frequency interrupt
0 A	1	0	1	0	Set reverse field on
0 B	1	0	1	1	Set reverse field off
0 C	1	1	0	0	Not supported
0 D	1	1	0	1	Set basic attribute to reverse video with 24 lines and set blink flip-flop off
0 E	1	1	1	0	Not supported
0 F	1	1	1	1	Set basic attribute to reverse video with 48 lines and set blink flip-flop off

On power-up, the DC12 control chip can be programmed to bring it to a known state. Typically, codes 00H, 04H, 09H, 0BH, and 0DH are programmed at power-up time.

The value to which the scroll latch is set determines on which scan row the first line of a scrolling region starts. Likewise, it determines the last scan row displayed for the last line in a scrolling region.

For example, when the latch is set to 0 (the degenerate case), the first line of the scroll region starts at scan row 0; the line is completely visible. The last line of the scrolling region terminates at scan row 9; this line is also completely visible.

When the scroll latch is nonzero, for example, 5, the first line of the scrolling region starts with scan row 5; only the bottom-half of the line is visible. The last line of the scrolling region terminates at scan row 4; only the top-half of the line is visible.

If the scroll latch is incremented from 0–9 and back to 0 again once each frame, the screen appears to smooth scroll from bottom to top (assuming that line linkages and line attributes are properly handled). On the other hand, if the scroll latch is decremented from 0 to 9 then down through 0, the screen seems to smooth scroll from top to bottom. (Assumption: all line linkages and line attributes are properly handled.)

A scrolling region is defined as a group of lines with their scrolling attributes set, surrounded by lines whose scrolling attributes are not set. Note that the scrolling attribute for a line resides in the line pointer information at the end of the previous line. Also, the first line on the screen (the one at RAM location 0), has its scrolling attribute reset by definition. Also note that the definition of a scrolling region does not preclude the definition of more than one scrolling region per screen, although that is of dubious value.

Whenever the scroll latch is nonzero, each scrolling region on the screen requires an extra (scrolling) line to be linked in. For example, if the scrolling region is 10 lines long when the scroll latch is set to nonzero, there must be an eleventh line linked in. If scrolling up (incrementing the scroll latch), the line must be linked in at the bottom. When the scroll latch is incremented back to 0 again, the top line of the scrolling region must be unlinked. When scrolling down (decrementing the scroll latch), new lines must be linked in at the top of the scroll region and unlinked down at the bottom. All line linking/unlinking should be done during the vertical blanking interval (after the vertical frequency interrupt is asserted). In 60 Hz mode, there are two blanked lines at the beginning of the screen: the line at RAM location 0, which points to the screen RAM address of the second blank line. The second blank line address bytes point to the starting location of the first line of data to be displayed.

The video processor guarantees to read the first line (at location 0) by the time that the interrupt service routine is entered. Changes to this line will not affect the screen until the next frame time. The second line will not be read for more than 500 microseconds (μs) after asserting the interrupt.

If the second line is to be changed, it must be changed very soon after entering the interrupt service routine to guarantee that the change will be visible in the current frame.

Therefore, if the first visible line on the screen is involved in the scroll region and is being either linked in or unlinked, then the vertical interrupt routine must guarantee that its pointer (which resides in the second invisible line) is changed within approximately 500 μs after the interrupt asserts.

Setting the scroll latch is much less time-critical than this. Because the scroll latch is loaded by the DC12 control chip by the vertical reset at the beginning of each frame, the only requirement is that the scroll latch be modified before the next frame begins. Note that the scroll latch value is the value that will be used during the next frame rather than the current frame.

3.4.9.5 Character Generator ROM – The character generator is a 4K $\times$ 8 bit ROM that is addressed by the coded representations of the desired characters stored in the screen RAM. Each code is used as the eight most significant bits of the ROM address. A scan counter in the DC12 control chip provides the four least significant bits of the ROM address. The eight character bits combine with the 4-bit scan count to provide the 12-bit address for the ROM. The data stored at each address (character + scan) are eight bits representing the presence or absence of dots of light at sequential horizontal positions within that scan.

The character generator ROM holds 255 characters corresponding to character codes OOH–FEH. Appendix C lists the codes and the corresponding characters they display. Character code FFH acts as the terminator byte for the termination detector. The character codes OOH–FEH correspond to address

OOOH–FEFH in the character generator ROM. The final hexadecimal digit of an address indicates the scan (ROW<3:0>) of the character being addressed. Table 3-9 lists the relation of the scan address digit to the scan number.

Each byte of information in the character generator ROM at a valid scan address represents eight bits of horizontal scan information. Figure 3-6 shows the bit patterns stored in the ROM for an uppercase and lowercase letter A. The computer displays characters on the screen in a 10 × 10 matrix of dots. Each 10 dot × 10 scan group is a character cell.

Table 3-9 Character Generator Scan Addresses

Scan Address	Character Scan Number	
F	1	Normally blank
0	2	Top of normal uppercase character
1	3	
2	4	
3	5	
4	6	
5	7	
6	8	Bottom of normal uppercase character
7	9	Normal descenders (underline scan)
8	10	Normal descenders
9-E		Not used (never displayed)

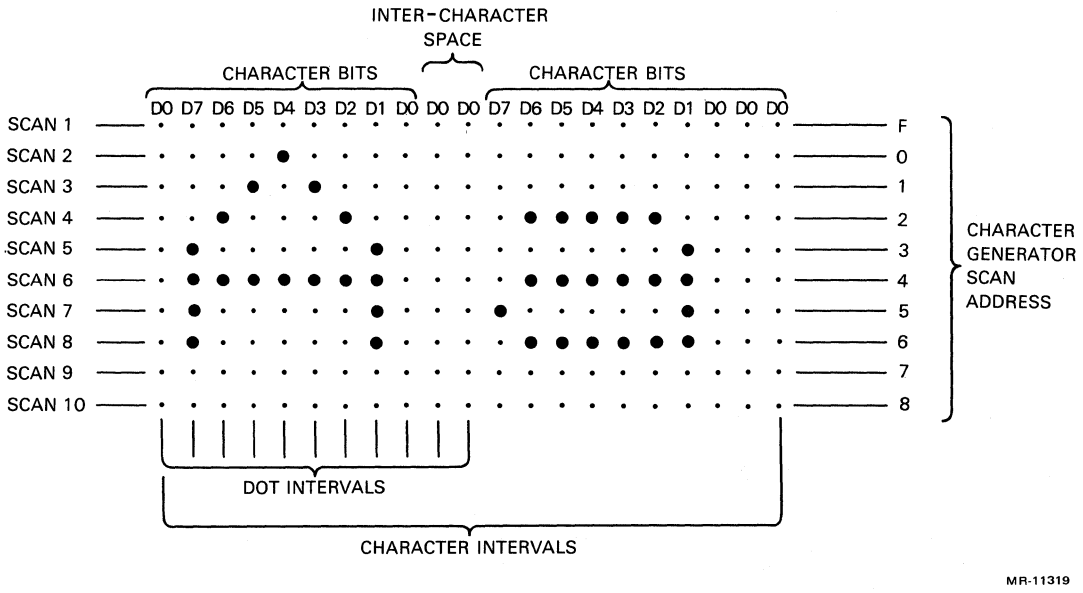


Figure 3-6 Character Generator ROM Patterns

The low order bit (D0) is a fill bit. It is used not only as the right-most bit in the character, but also fills in the right-hand space between characters. This inter-character space is two-dot intervals in 80-column mode, and one-dot interval in 132-column mode.

3.4.9.6 Composite Video Signal Characteristics – The composite video output of the video processor subsystem provides a compatible EIA RS-170 output generated by combining the video signal with a composite synchronous signal. The composite video signal is applied to connector J3 on the system module and can directly drive a standard video monitor.

NOTE

The use of dc coupling is not in strict agreement with the EIA RS-170 standard. To agree with RS-170, the video generator output load requires a 10 microfarad capacitor in series with the output. Without the capacitor, the RS-170 2 milliamp (mA) dc short circuit requirement is violated.

Figure 3-7 illustrates the composite video output.

The composite video output has five nominal characteristics.

1. Output impedance = 75 ohms, dc coupled to 0.0 V.
2. Sync level = 0.0 V.
3. Reference black level = approximately 0.3 V with a 75 ohm load.
4. Reference white level = approximately 1.0 V with a 75 ohm load.
5. The composite synchronous waveform conforms to EIA RS-170 standards. The vertical interval comprises six equalizing pulses, six vertical synchronous pulses, and six more equalizing pulses. The timing is as follows.

Equalizing pulse width	= 2.33 μs ±50 ns
Vertical pulse width	= 27.28 μs ±200 ns
Horizontal pulse width	= 4.71 μs ±50 ns
Horizontal blank width	= 11.84 μs ±50 ns/80-column mode
	= 12.34 μs ±50 ns/132-column mode
Front porch	= 1.54 μs ±50 ns

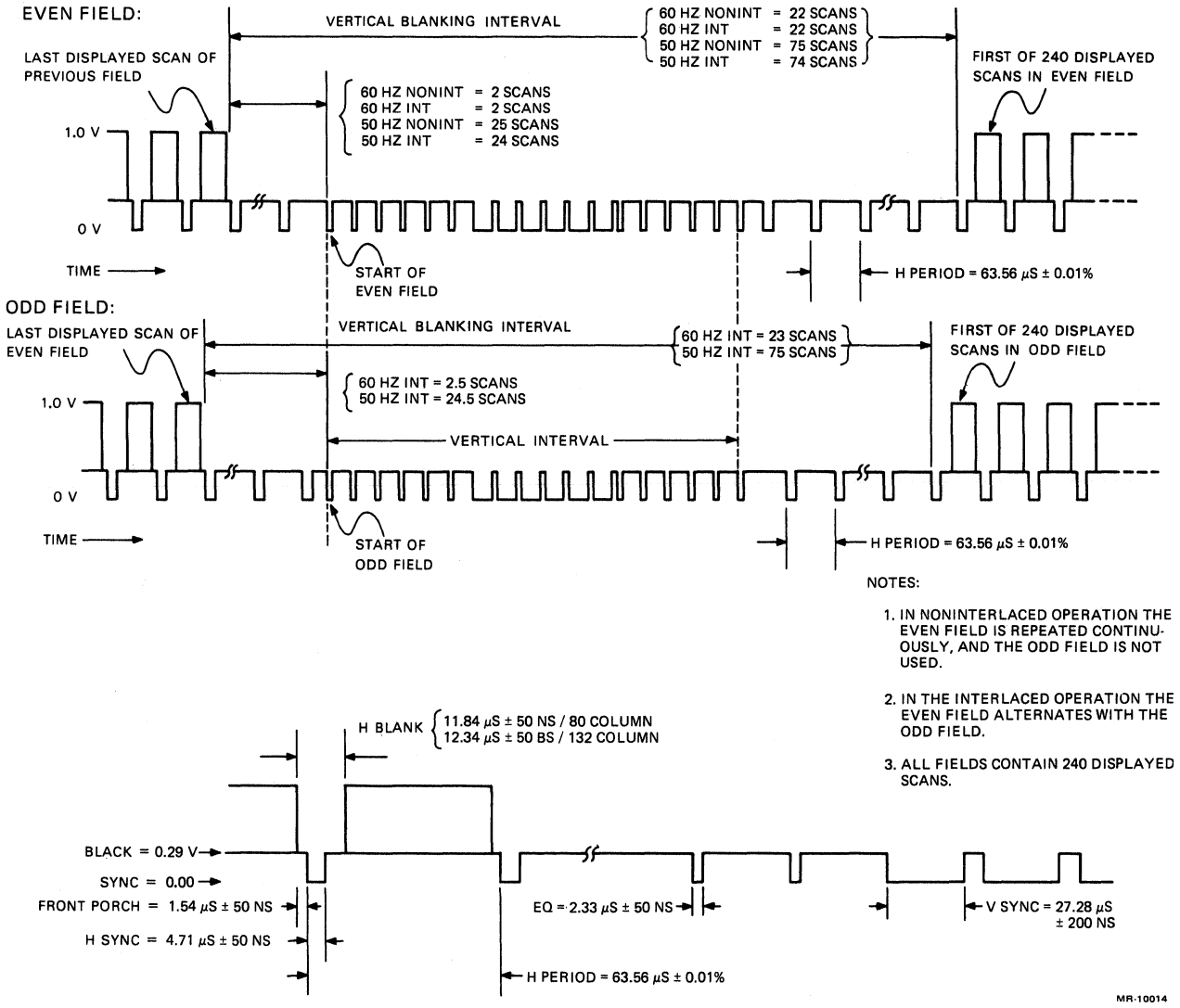


Figure 3-7 Composite Video Synchronous Timing Diagram

3.4.10 Language ROMs

The 16K × 8 bit language ROM is ROM 1 of the two-ROM set that make up the 32K byte ROM. See Figure 3-2. The language ROM contains language character translation codes necessary to support the various international keyboards.

The character storage space needed to include all language variations exceeds the capacity of a single 16K × 8 bit ROM. Because of this, the language codes are clustered in five sets of three languages. Five different language ROMs are needed to support the 15 available international language keyboards. English is a part of all five language ROMs. Table 3-10 lists the language ROMs and the languages they support.

Table 3-10 ROM Language Clusters

ROM 1 Cluster	Languages	Digital Part Number
1	German, French, English	23-020E5-00
2	Dutch, French, English	23-015E5-00
3	Finnish, Swedish, English	23-016E5-00
4	Danish, Norwegian, English	23-017E5-00
5	Spanish, Italian, English	23-018E5-00

3.4.11 8088 Diagnostic and Control/Status Registers

The 8088 processor accesses two diagnostic registers: one control register and one status register. The two 8-bit diagnostic registers control and read the status of various system functions during diagnostic testing. The control register controls the modem control lines of the communications port and writes diagnostic error codes into the four 8088 diagnostic LEDs. The status register reads the status of the modem control lines of the communications port, the interrupt line of each processor, and the MHFU logic enable signal. The registers are shown in Figure 3-8 and described in the following paragraphs.

3.4.11.1 Diagnostic Write Register: 8088 Processor – The diagnostic write register is an 8-bit write-only register that is used for diagnostic control purposes. This register also contains a bit to loopback the transmitted data of the ports through a loopback multiplexer into the received data input of the ports. To access this register, perform a write to the maintenance port (address 0AH). The register bit format is shown in Figure 3-9 and the bits are described in Tables 3-11, 3-12, 3-13, 3-14, and 3-15.

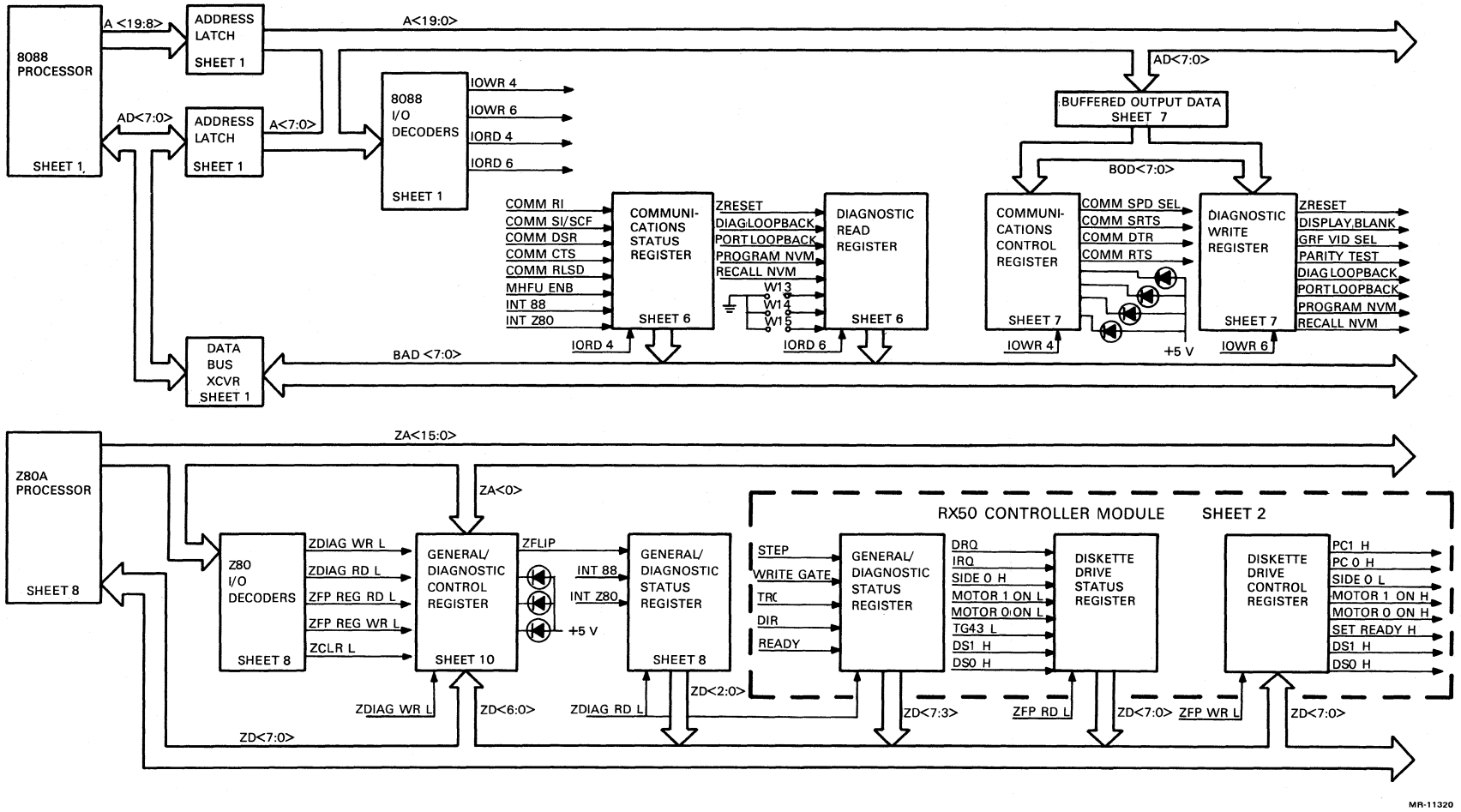


Figure 3-8 System Module Control/Status and Diagnostic Registers

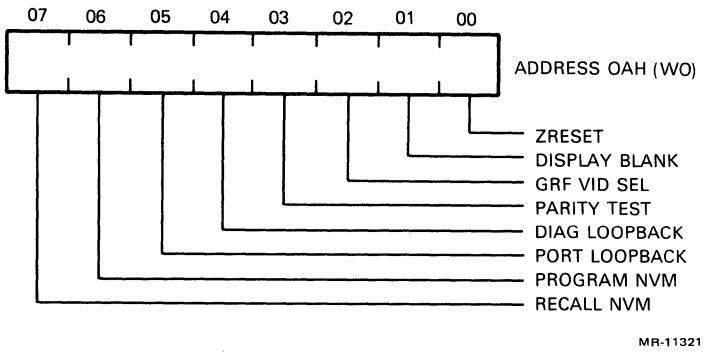


Figure 3-9 Diagnostic Write Register (8088) Format

Table 3-11 Diagnostic Write Register (8088) Bit Description

Bit	Name	Description
0	ZRESET	When this bit is high (1), it resets the Z80A processor from the 8088 processor side. This bit is active at power-up.
1	DISPLAY BLANK	When this bit is low (0), the computer will blank the display.
2	GRF VID SEL	When this bit is low (0), the system module video is selected. When high (1), the graphics module video is selected.
3	PARITY TEST	When high (1), this bit enables testing of the parity circuit on the optional memory module.
4	DIAG LOOPBACK	This bit is a maintenance bit that is cleared (0) on power-up. When high (1), this bit allows the RX50 controller data separator and the serial video output from the DC12 to be tested by using the printer port. Tables 3-12 and 3-13 describe how the signals are routed through the printer port.
5	PORT LOOPBACK	This bit is a communications port loopback maintenance bit. This bit is cleared (0) on power-up. When high (1), this bit sets up the loopback multiplexers for the communications, printer, and keyboard ports to allow testing. The port loopbacks are done in such a way that bit rate errors of one port can be detected by another. Tables 3-14 and 3-15 describe how the signals are routed through the ports.
6	PROGRAM NVM	When high (1), this bit allows data to be written into the NVM.
7	RECALL NVM	When high (1), this bit allows data to be recalled (read) from the NVM.

Table 3-12 Printer Port Diagnostic Signal Routing*

Diagnostic Loopback Bit 4 =	Signal Source From	Signal Input To
0	PRT RCV DATA	PRT RXD
1	VIDEO OUT 2	PRT RXD
0	PRT RXTXC	PRT RXTXC
1	500 KHZ	PRT RXTXC
0	MASTER CLK	VIDEO CLK
1	250 KHZ	VIDEO CLK
0	RAW DATA	DATA SEPARATOR
1	PRT TXD	DATA SEPARATOR

* During diagnostic loopback, the TEST input of the 8088 processor is connected to the COMM/PRINTER INTR L output of the multiprotocol serial controller (MPSC). Thus, using the 8088 processor's wait instruction in a polled I/O loop, the diagnostic firmware is able to keep up with the 500K baud data rate of the MPSC.

Table 3-13 Printer Port Diagnostic Signal Description

Direction	Signal Source	Description
From	PRT RCV DATA	Data received from the printer through connector J2
From	VIDEO OUT 2	DC12 serial video output data to the printer port during diagnostic loopback testing
To	PRT RXD	Printer received data input to the MPSC from the printer or DC12 serial video
From	PRT RXTXC	Printer receiver/transmitter clock input to the MPSC from the printer baud rate generator
From	500 KHZ	Printer receiver/transmitter clock input to the MPSC during diagnostic loopback testing
To	PRT RXTXC	Printer receiver/transmitter clock input to MPSC from printer baud rate generator or 500 kHz pulses from the clock circuit
From	MASTER CLK	Master clock pulse input to the video loopback multiplexer
From	250 KHZ	250 kHz clock pulse input to the video loopback multiplexer

Table 3-13 Printer Port Diagnostic Signal Description (Cont)

Direction	Signal Source	Description
To	VIDEO CLK	Video clock input to the DC11 control chip from the master clock or 250 kHz outputs of the clock circuit
From	RAW DATA	Raw data (clocks and data) from the disk drives
From	PRT TXD	Data transmitted from the MPSC to the printer, the keyboard loopback multiplexer, and the diskette drive data separator
To	DATA SEPARATOR	Data input to data separator from the diskette drives, or printer transmitted data from the MPSC

Table 3-14 Port Loopback Signal Routing

Port Loopback Bit 5 =	Signal Source From	Signal Input To
0	COMM RCV DATA	COMM RXD
1	COMM TXD	COMM RXD
0	PRT RCV DATA	PRT RXD
1	KBD TXD	PRT RXD
0	KBD RCV DATA	KBD RXD
1	PRT TXD	KBD RXD

Table 3-15 Port Loopback Signal Description

Direction	Signal Source	Description
From	COMM RCV DATA	Communications received data from the communications connector J1 applied to the communications loopback multiplexer
From	COMM TXD	Communications transmitted data from the MPSC applied to the communications loopback multiplexer
To	COMM RXD	Communications received data input to the MPSC from the communications device or communications transmitted data from the MPSC during port loopback testing
From	PRT RCV DATA	Printer received data from printer connector J2 applied to printer loopback multiplexer
From	KBD TXD	Keyboard transmitted data from the keyboard PUSART to the printer loopback multiplexer via the video loopback multiplexer
To	PRT RXD	Printer received data input to the MPSC from the printer or the keyboard transmitted data during port loopback testing
From	KBD RCV DATA	Keyboard received data from the keyboard connector J3 to the keyboard loopback multiplexer
From	PRT TXD	Printer transmitted data from the MPSC to the keyboard loopback multiplexer
To	KBD RXD	Keyboard received data input to the keyboard PUSART from the keyboard connector or the printer transmitted data during port loopback testing

3.4.11.2 Diagnostic Read Register: 8088 Processor – The diagnostic read register is an 8-bit read-only register that reads the status of a number of diagnostic control signals during diagnostic testing. To access the register, perform a read to the maintenance port (address 0AH). The register bit format is shown in Figure 3-10, and the bits are described in Table 3-16.

3.4.11.3 Communications Status Register: 8088 Processor – The communications status register is an 8-bit read-only register that stores the status of the modem control lines for the communications port, the interrupt line for each processor, and the MHFU enable signal. To access this register, perform a read to address 02H. The register bit format is shown in Figure 3-11, and the bits are described in Table 3-17.

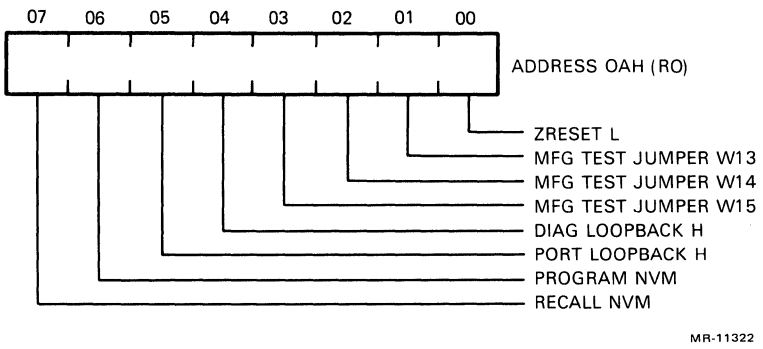


Figure 3-10 Diagnostic Read Register (8088) Format

Table 3-16 Diagnostic Read Register (8088) Bit Description

Bit	Name	Description
0	ZRESET L	This bit represents the state of bit 0 of the 8088 diagnostic write register.
1–3	MFG TEST JUMPER	These bits represent the state of the W13, W14, and W15 manufacturing test jumpers. These bits are normally high (1).
4	DIAG LOOPBACK H	This bit represents the state of bit 4 of the 8088 diagnostic write register (diagnostic loopback H).
5	PORT LOOPBACK H	This bit represents the state of bit 5 of the 8088 diagnostic write register (port loopback H).
6	PROGRAM NVM	This bit represents the state of bit 6 of the 8088 diagnostic write register (program NVM).
7	RECALL NVM	This bit represents the state of bit 7 of the 8088 diagnostic write register (recall NVM).

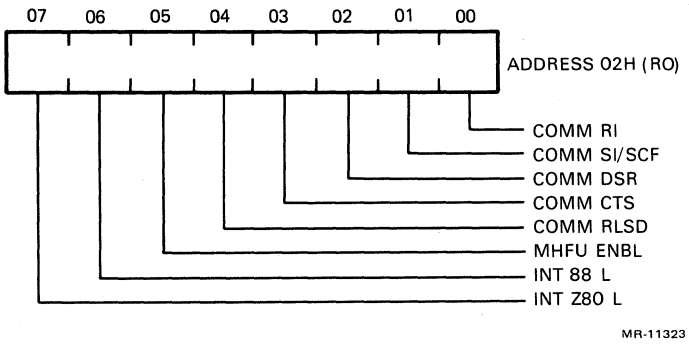


Figure 3-11 Communications Status Register (8088) Format

Table 3-17 Communications Status Register (8088) Bit Description

Bit	Name	Description
0	COMM RI	This bit reflects the status of the ring indicator line of the communications port.
1	COMM SI/SCF	This bit reflects the status of the speed indicator line or the secondary receive line signal detect of the communications port.
2	COMM DSR	This bit reflects the status of the data set ready line of the communications port.
3	COMM CTS	This bit reflects the status of the clear to send line of the communications port.
4	COMM RLSD	This bit reflects the status of the receive line signal detect of the communications port.
5	MHFU ENB L	This bit reflects the status of massive hardware failure (MHFU) detect enable L.
6	INT88 L	This bit reflects the status of the INT88 L bit that is asserted by the Z80A processor to interrupt the 8088 processor for interprocessor communications.
7	INTZ80A L	This bit reflects the status of the INTZ80A L bit that is asserted by the 8088 processor to interrupt the Z80A processor for interprocessor communications.

3.4.11.4 Communications Control Register: 8088 Processor – The communications control register is an 8-bit write-only register that controls the modem lines on the communications port and writes diagnostic error codes into the four 8088 LEDs. To access this register, perform a write to address 02H. The register bit format is shown in Figure 3-12, and the bits are described in Table 3-18.

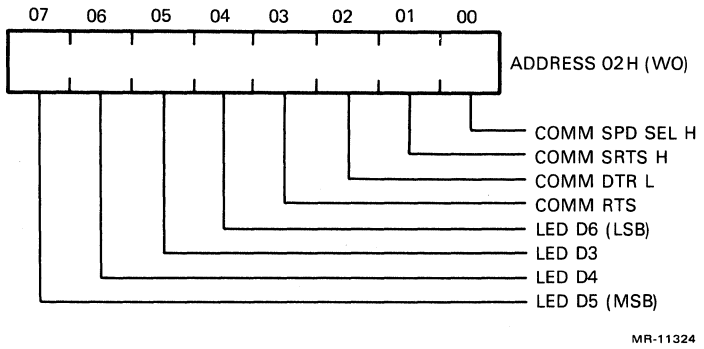


Figure 3-12 Communications Control Register (8088) Format

Table 3-18 Communications Control Register (8088) Bit Description

Bit	Name	Description
0	COMM SPD SEL H	This bit controls the speed select line of the communications port.
1	COMM SRTS H	This bit controls the secondary request to send line of the communications port.
2	COMM DTR L	This bit controls the data terminal ready line of the communications port.
3	COMM RTS	This bit controls the request to send line of the communications port.
4	LED (D6)	This bit displays the least significant bit of the diagnostic error message code. When written with a 0, the LED lights.
5	LED (D3)	This bit displays the second bit of the diagnostic error message code. When written with a 0, the LED lights.
6	LED (D4)	This bit displays the third bit of the diagnostic error message code. When written with a 0, the LED lights.
7	LED (D5)	This bit displays the most significant bit of the diagnostic error message code. When written with a 0, the LED lights.

3.4.12 Z80A Registers

The Z80A processor can access registers on the system module and the RX50 controller module to control, and it can monitor the status of the diskette drives and a number of other functions for diagnostic and general purposes. These registers are shown in Figure 3-8 and described in the following paragraphs.

The registers that the Z80A processor can access are as follows.

- General/diagnostic status register
- General/diagnostic control register
- Diskette drive status register
- Diskette drive control register

The Z80A processor can access five other diskette drive registers that are located in the floppy disk controller (FDC) chip on the RX50 controller module. These registers are listed here for reference only and are described in detail in Chapter 5 of the *Rainbow™ 100 Technical Manual* (EK-PC100-TM).

1. FDC status register
2. FDC control register
3. FDC track register
4. FDC sector register
5. FDC data register

3.4.12.1 General/Diagnostic Status Register: Z80A Processor – The general/diagnostic status register is an 8-bit read-only register that holds the status of interprocessor interrupts, ZFLIP, and diskette drive control signals. The three least significant bits of this register are located on the system module, and the five most significant bits are located on the RX50 controller module. To access this register perform a read to address 21H. The register bit format is shown in Figure 3-13 and the bits are described in Table 3-19.

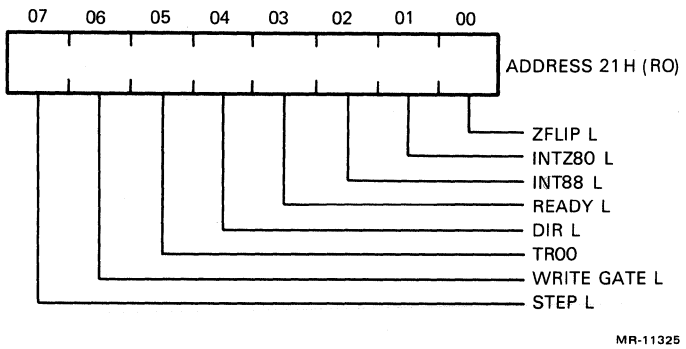


Figure 3-13 General/Diagnostic Status Register (Z80A) Format

Table 3-19 General/Diagnostic Status Register (Z80A) Bit Description (Cont)

Bit	Name	Description
0	ZFLIP L	This bit is the read back for the ZFLIP L bit in the general/diagnostic control register (Z80A).
1	INTZ80 L	This bit reads the INTZ80 bit that is sent by the 8088 processor to interrupt the Z80A processor.
2	INT88 L	This bit reads the INT88 bit that is sent by the Z80A processor to interrupt the 8088 processor.
3	READY L	This bit reflects the status of the READY L signal coming from the diskette drive.
4	DIR L	This bit reflects the status of the DIRECTION signal from the FDC chip going to the diskette drive. This bit is used to control the step direction (in or out) of the read/write heads in the diskette drive. High = head stepping away from center of diskette. Low = head stepping towards center of diskette.
5	TR00	This bit reflects the status of the TRACK 0 signal coming from the diskette drive. When high (1), the heads are on the track 0 position.
6	WRITE GATE L	This bit reflects the status of the WRITE GATE signal from the FDC chip. Used to gate write data to the diskette drive.
7	STEP L	This bit reflects the status of the STEP signal from the FDC chip that is used to step the diskette drive read/write heads in or out. When pulsed low, head will move one track space in the direction indicated by the DIR L signal.

3.4.12.2 General/Diagnostic Control Register: Z80A Processor – The general/diagnostic control register is an 8-bit write-only register that holds the bit (ZFLIP) that determines whether the Z80A address bit Z<15> is inverted and three bits of Z80A diagnostic LED information. Only the four most significant bits of this register are used. To access this register perform a write to address 20H or 21H. The register bit format is shown in Figure 3-14 and the bits are described in Table 3-20.

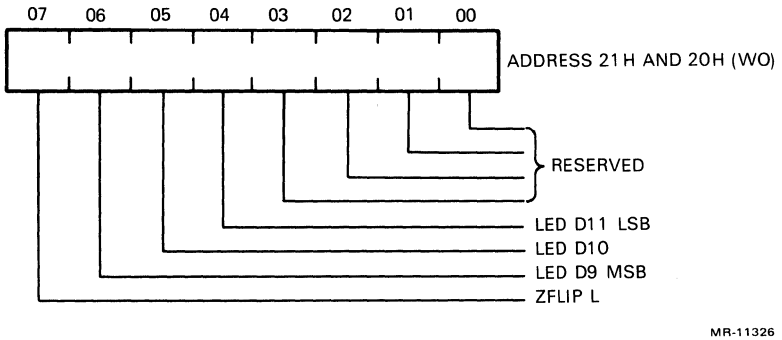


Figure 3-14 General/Diagnostic Control Register (Z80A) Format

Table 3-20 General/Diagnostic Control Register (Z80A) Bit Description

Bit	Name	Description
0–3		These bits are reserved for future use.
4	LED D11	This bit displays the least significant bit of the diagnostic error message code. When written with a 0, the LED lights.
5	LED D10	This bit displays the second bit of the diagnostic error message code. When written with a 0, the LED lights.
6	LED D9	This bit displays the most significant bit of the diagnostic error message code. When written with a 0, the LED lights.
7	ZFLIP L	Z80A processor address bit A<0> is the input for bit 7 of this register. When A<0>, address line A<15> of the Z80A processor is inverted. In this case, ZFLIP is low and the 2K-byte unshared RAM is at address 8000H instead of 0000H. ZFLIP is low whenever the Z80A is reset. To set it high, write to the register at address 21H. To reset it, write to address 20H.

3.4.12.3 Diskette Drive Status Register: Z80A Processor – The diskette drive status register is an 8-bit read-only register that holds the status of diskette drive lines coming from the RX50 controller module and going to the diskette drives. Three of the diskette drive status signals come from the FDC chip, and the remaining five come from the diskette drive control register. The diskette drive status register is located on the RX50 controller module and a read to address 40H accesses the register. The register bit format is shown in Figure 3-15 and the bits are described in Table 3-21.

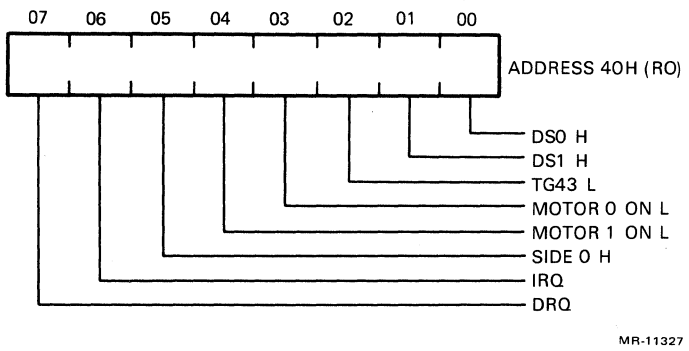


Figure 3-15 Disk Drive Status Register (Z80A) Format

Table 3-21 Diskette Drive Status Register (Z80A) Bit Description

Bit	Name	Description
0–1	DS0–DS1	These bits reflect the status of bits 0 and 1 from the diskette drive control register. They indicate the selected drives. DS1 DS0 DRIVE 0 0 A 0 1 B 1 0 C 1 1 D
2	TG43 L	This bit reflects the status of the TRACK GREATER THAN 43 signal sent from the FDC chip to the diskette drive.
3	MOTOR 0 ON L	This bit reflects the status of the MOTOR 0 ON line at connector J2 of the RX50 controller module. When low (0), this bit indicates that the MOTOR 0 ON bit is set in the diskette drive control register.
4	MOTOR 1 ON L	This bit reflects the status of the MOTOR 1 ON line at connector J3 of the RX50 controller module. When low (0), this bit indicates that the MOTOR 1 ON bit is set in the diskette drive control register.
5	SIDE 0 H	This bit reflects the status of the SIDE SELECT signal at connectors J2 and J3 of the RX50 controller module. For single-sided drives, this bit will always read low (0).
6	IRQ	This bit reflects the status of the INTERRUPT REQUEST signal coming from the FDC chip. It indicates that a status bit has changed.
7	DRQ	This bit reflects the status of the DATA REQUEST signal from the FDC chip. It indicates that the FDC chip has read data to be transferred or requires new write data.

3.4.12.4 Diskette Drive Control Register: Z80A Processor – The diskette drive control register is an 8-bit write-only register that holds the write data precompensation select signals (PC0,PC1), drive select signals (MOTOR ON 0 L and MOTOR ON 1 L), a diagnostic override bit (SET READY H), and a diskette side select signal (SIDE 0 L).

The drive motor on signals, drive select signals, and the diskette side select signal are sent to the diskette drives and the diskette drive status register. The write data precompensation select signals provide two of the address inputs for a write data precompensation ROM. The diagnostic override bit enables the FDC chip to perform a read-or-write operation.

To access the diskette drive control register, write to address 40H. The register bit format is shown in Figure 3-16 and the bits are described in Tables 3-22 and 3-23.

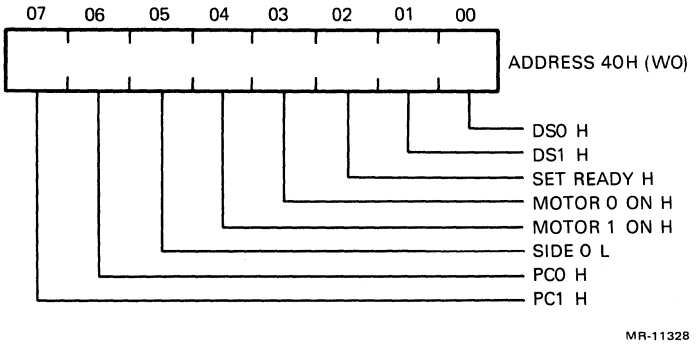


Figure 3-16 Disk Drive Control Register (Z80A) Format

Table 3-22 Diskette Drive Control Register (Z80A) Bit Description

Bit	Name	Description
0–1	DS0–DS1	These bits control the selection of the diskette drives. The binary values (0–3) written in these bits select drives A–D. Only one drive can be selected at any given time.
2	SET READY H	This bit is the diagnostic READY override bit. When set (1), this bit asserts DRIVE READY to the FDC chip.
3	MOTOR 0 ON H	When high (1), this bit turns on the motor in the first drive unit (drives A and B).
4	MOTOR 1 ON H	When high (1), this bit turns on the motor in the second drive unit (drives C and D).
5	SIDE 0 L	This bit selects the side of the diskette to be accessed. For single-sided drives, this bit is always set to 0 for side 0.
6–7	PC0–PC1	These binary bits are used to specify the write data precompensation values. Table 3-23 lists the precompensation values for all 80 tracks on the diskette.

Table 3-23 Write Data Precompensation Codes

TG43*	Precompensation PC1	PC0	Track Number
0	0	0	0–9
0	0	0	10–19
0	0	0	20–29
0	0	0	30–39
1	0	0	40–49
1	0	0	50–60
1	0	1	61–69
1	0	1	70–79

*0 = write operation to outer tracks (0–43);
1 = write operation to inner tracks (44–79)

3.4.13 MPSC General Description

The multiprotocol serial controller (MPSC) is a 40-pin dual-in-line microcomputer peripheral device that supports asynchronous (start/stop), byte synchronous (monosync, IBM bisync), and bit synchronous (ISOs, HDLC, SDLC) protocols.

The MPSC has the following features.

- Asynchronous, byte synchronous, and bit synchronous operation
- Two independent full-duplex transmitters and receivers
- Baud rate: 50 to 19200 baud
- Asynchronous
  - 5–8 bits per character
  - Odd, even, or no parity
  - 1 or 2 stop bits
  - Error detection: framing, overrun, and parity
- Byte synchronous
  - Character synchronization: internal or external
  - 1 or 2 synchronous characters
  - Automatic CRC generation and checking (CRC-16)
  - IBM bisynchronous compatible
- Bit synchronous
  - HDLC/SDLC flag generation and recognition
  - 8-bit address recognition
  - Automatic zero bit insertion and deletion
  - Automatic CRC generation and checking (CCITT-16)
  - CCITT X.25 compatible
- Polled and interrupt driven modes

The MPSC contains two independent serial receiver/transmitter channels: communications channel and printer channel. Rainbow computers use the communications channel for communications with a host computer (either directly or through a modem), and the printer channel interfaces to a printer through the printer connector. Each channel consists of a transmitter, receiver, and a set of read/write registers that initialize and control the device.

The MPSC as implemented on the system module supports two processor data transfer modes: polled and interrupt driven. In the polled mode of operation, the 8088 processor periodically reads (polls) an MPSC status register to determine when a character has been received, when a character is needed for transmission, and when transmission errors are detected. In the interrupt-driven mode, the MPSC interrupts the 8088 processor when a character has been received, when a character is needed for transmission, and when transmission errors are detected. Table 3-24 describes the MPSC pin functions.

Table 3-24 MPSC Pin Descriptions

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
1	2.5 MHZ	CLK	I	CLOCK INPUT: This is the 2.5 MHz clock pulse input to the MPSC.
2	INIT L	RESET	I	INITIALIZE: During power-up, this signal is low (0). The low signal forces the MPSC to an idle state. The COMM TXD and PRT TXD outputs are forced high. The modem interface signals are also forced high. The MPSC will remain idle until the control registers are initialized. INIT L must be low for one complete clock cycle.
3	COMM RLSD	DCDA	I	CARRIER DETECT (channel A): This signal indicates that line transmission has started. The MPSC will begin to sample data on the COMM RXD line if modem enables are selected.
4	PRINTER CLK	RXCB	I	PRINTER RECEIVER CLOCK: This signal clocks data (PRT RXD) from the printer into the channel B receiver at the baud rate programmed into the printer baud rate generator.
5		DCDB	I	CARRIER DETECT (channel B): This pin is not used in Rainbow computers.

* O = Output, I = Input, I/O = Input/Output

† See Paragraph 3.4.11.4 for information on these modem control signals.

Table 3-24 MPSC Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
6	PTR DTR L	CTSB	I	CLEAR TO SEND (channel B): This signal indicates that the printer is ready to accept data from the channel B transmitter.
7	PRINTER CLK	TXCB	I	PRINTER TRANSMITTER CLOCK (channel B): This signal clocks data (PRT TXD) from the channel B transmitter to the printer at the baud rate programmed into the baud rate generator.
8	PRT TXD	TXDB	O	PRINTER TRANSMIT DATA (channel B): This signal is the serial data transmitted to the printer.
9	PRT RXD	RXDB	I	PRINTER RECEIVE DATA (channel B): This signal is the input from the printer.
10		SYNC/RSTB	I/O	SYNCHRONOUS DETECTION (channel B): This pin is not used in Rainbow computers.
11		WAIT B/DRQTXA	I/O	WAIT/DMA REQUEST (channel B): This pin is not used in Rainbow computers.
12–19	BAD<7:0>	D7–D0	I/O	DATA BUS: This bus transfers data, control, command, and status information between the 8088 and the MPSC. BAD<0> is the least significant bit.
20	GND	GND		GROUND.
21	WR88 L	WR	I	WRITE 8088: This signal is negated low (0) to transfer data or commands from the 8088 processor to the MPSC.
22	RD88 L	RD	I	READ 8088: This signal, when low (0), indicates an I/O read operation is in progress. Used with A<1>, A<0> and COMM/PRT SEL L, it transfers data from the MPSC to the 8088 processor.

* O = Output, I = Input, I/O = Input/Output

† See Paragraph 3.4.11.4 for information on these modem control signals.

Table 3-24 MPSC Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
23	COMM/PRT SEL L	CS	I	COMMUNICATIONS/PRINTER SELECT: This signal, when low (0), enables the MPSC to accept command or data inputs from the 8088 processor during a write cycle, or to transmit data to the 8088 processor during a read cycle.
24	A<1>	C/D	I	CONTROL OR DATA SELECT: This address bit defines the type of information transfer performed between the 8088 processor and the MPSC. A high (1) during a processor write-to or read-from the MPSC indicates that the data on the BAD<7:0> bus is a command for the channel selected by address bit A<0>. A low (0) indicates a data transfer.
25	A<0>	B/A	I	CHANNEL A or B SELECT: This address bit selects channel A or B during a data transfer between the 8088 processor and the MPSC. When this address bit is high (1), channel B is selected.
26		HAI/DTRB	I	DMA ACKNOWLEDGE: This pin is not used by Rainbow computers.
27	+5 V	INTA	I	INTERRUPT ACKNOWLEDGE INPUT: When low (0), this signal allows the highest priority interrupting device to generate an interrupt vector. This signal is tied to +5 V in Rainbow computers.
28	COMM/PRT INTR L	INT	O	COMMUNICATIONS/PRINTER INTERRUPT REQUEST: When low (0), this signal informs the interrupt logic that the MPSC requires service from the 8088 processor.

* O = Output, I = Input, I/O = Input/Output

† See Paragraph 3.4.11.4 for information on these modem control signals.

Table 3-24 MPSC Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
29		PRI/DRQRXB	I	INTERRUPT PRIORITY IN: This pin is not used in Rainbow computers. It is tied to ground.
30		PRO/DRQTXB	O	INTERRUPT PRIORITY OUT: This pin is not used in Rainbow computers.
31		DTRA**	O	DATA TERMINAL READY (channel A): This pin is not used in Rainbow computers.
32		WAIT A/DRQRXA	I/O	WAIT/DMA REQUEST (channel A): This pin is not used in Rainbow computers.
33		SYNCA	I/O	SYNCHRONOUS DETECTION (channel A): This pin is not used in Rainbow computers.
34	COMM RXD	RXDA	I	COMMUNICATIONS RECEIVE DATA (channel A): This signal is the serial data input from the communications device.
35	COMM RXC	RXCA	I	COMMUNICATIONS RECEIVER CLOCK (channel A): This signal clocks data (COMM RXD) from the communications device into the channel A receiver at the baud rate programmed into the communications baud rate generator.
36	COMM TXC	TXCA	I	COMMUNICATIONS TRANSMITTER CLOCK (channel A): This signal clocks data (COMM TXD) from the channel A transmitter to the communications device at the baud rate programmed into the communications baud rate generator.
37	COMM TXD	TXDA	O	COMMUNICATIONS TRANSMIT DATA (channel A): This signal is the serial data transmitted to the communications device.

* O = Output, I = Input, I/O = Input/Output

† See Paragraph 3.4.11.4 for information on these modem control signals.

Table 3-24 MPSC Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
38		RTSA†	O	REQUEST TO SEND (channel A): This pin is not used in Rainbow computers.
39	COMM CTS	CTSA	I	COMMUNICATIONS CLEAR TO SEND (channel A): When low (0), this signal indicates that the modem is ready to accept data from the channel A transmitter.
40	+5 V	VCC		POWER: +5 V supply

* O = Output, I = Input, I/O = Input/Output

† See Paragraph 3.4.11.4 for information on these modem control signals.

The MPSC interfaces to the 8088 processor over the BAD<7:0> bus. The system interface control logic in the MPSC uses the A<1:0>, COMM/PTR SEL L, RD88 L, and WR88 L control signals from the 8088 processor to access the internal registers of the MPSC. Each serial I/O channel responds to two I/O addresses. Table 3-25 lists the addresses of the I/O registers.

Command, parameter, and status information is stored in 22 registers within the MPSC (8 write-only registers and 3 read-only registers for each channel). These registers are all accessed by means of the command/status ports for each channel. An internal pointer register selects which of the command or status registers will be written or read during a command/status access of an MPSC channel. The block diagram in Figure 3-17 shows the command/status register architecture for each serial channel. In the following discussion, the writable registers are referred to as WR0–WR7 and the readable registers as RR0–RR2.

The three least significant bits of WR0 are automatically loaded into the pointer register every time WR0 is written. After reset, WR0 is set to 0 so that the first write to a command register causes the data to be loaded into WR0 (which sets the pointer register). After WR0 is written, the following read or write accesses the register selected by the pointer. The pointer is reset after the read or write operation is completed. In this manner, reading or writing an arbitrary MPSC channel register requires two I/O accesses. The first access is always a write command. This write command sets the pointer register. The second access is either a read or write command; the pointer register (previously set) ensures that the correct internal register is read or written. After this second access, the pointer register is automatically reset. Note that writing WR0 and reading RR0 does not require presetting the pointer register.

During initialization and normal MPSC operation, various registers are read and/or written by the 8088 processor. These actions are discussed in detail in the following paragraphs. Note that WR6 and WR7 are not used in the asynchronous communications mode.

Table 3-25 MPSC Register Addressing

Address (Hex)	Register	Type*
40	Communications Data	R/W
42	Communications Control/Status	R/W
41	Printer Data	R/W
43	Printer Control/Status	R/W

*R/W = READ/WRITE

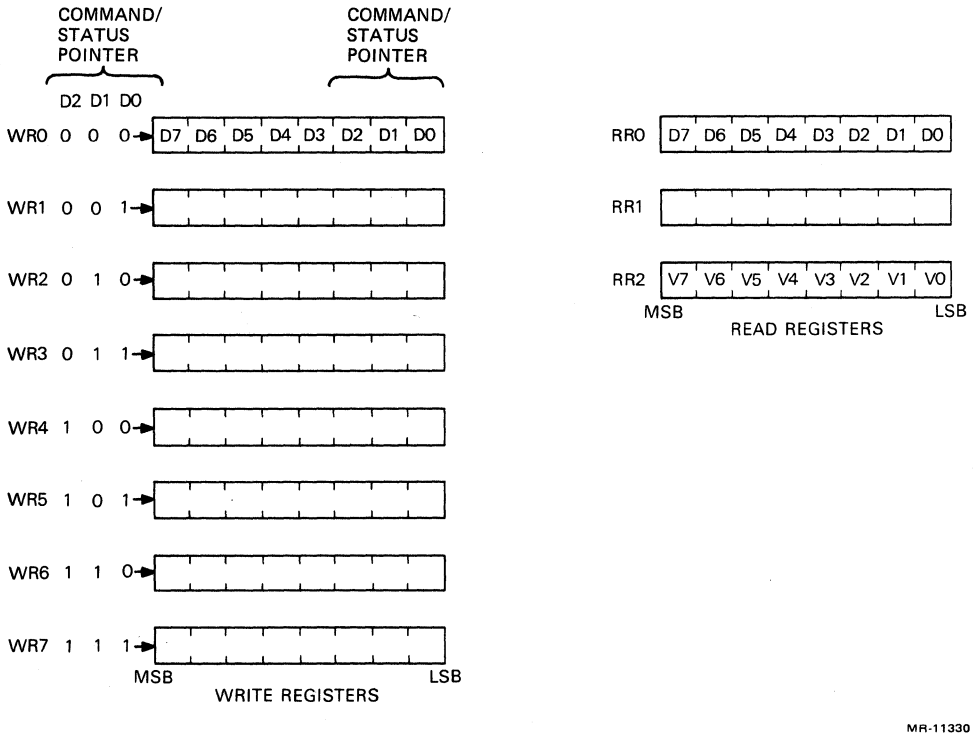


Figure 3-17 MPSC Command/Status Registers (Each Channel)

3.4.14 MPSC Communications Channel

The communications channel of the MPSC communicates with another computer through the communications port connector J2. It has full modem support and supports the same signals as the VT102 terminal. The *VT102 Video Terminal User's Guide*, (EK-VT102-UG) gives detailed information on the terminal. This port can support United States and European full- and half-duplex modems. The port has asynchronous as well as bisynchronous modes with an RS-423 (V.24, V.28) interface conforming to CCITT standards V.21, V.22, and V.23. Break detection by this port is supported. Baud rates supported are:

50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19200.

To set the bit rates, write a byte to the communications baud rate register at I/O address 06H. The four least significant bits D<3:0> of the byte D<7:0> select the communications receiver clock (COMM RXC) bit rate and the four most significant bits D<7:4> select the communications transmit clock (COMM TXC) bit rate. Figure 3-18 shows the format for the communications baud rate register.

The communications transmitter and receiver bit rates are software selectable according to the bit values in Table 3-26.

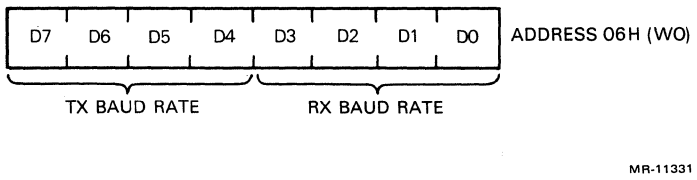


Figure 3-18 Communications Baud Rate Register Format

Table 3-26 Communications Baud Rate Selection

D<7:4>–D<3:0> Value (Hexadecimal)	Baud Rate	D<7:4>–D<3:0> Value (Hexadecimal)	Baud Rate
0	50	8	1200
1	75	9	1800
2	110	A	2000
3	134.5	B	2400
4	150	C	3600
5	200	D	4800
6	300	E	9600
7	600	F	19200

When the Rainbow computer is connected to a host computer through a modem, the modem supplies the transmit and receive clocks to the MPSC. Bit 3 of the printer baud rate register at address 0EH selects external clocks. When bit 3 is high (1), the external clock source supplies the transmit and receive clocks for the communications channel in the MPSC. When bit 3 is low (0), the communications baud rate generator supplies the transmit and receive clocks. Note that bits <2:0> of the printer baud rate register select the printer transmit and receive baud rates.

3.4.14.1 Asynchronous Operation – Asynchronous operation (start/stop) is a method of data transmission in which the transmitting and receiving systems need not be synchronized.

Instead of transmitting data clocking information with the data, the transmitting and receiving systems use locally generated clocks at the same rate or 16, 32, or 64 times as fast as the data transmission rate. When the transmitting system sends a character of information, special start and stop bits frame (precede and follow) the character data. This framing information permits the receiving system to temporarily synchronize with the data transmission.

For operation in the asynchronous mode, the following registers must be initialized with the specified parameters:

- Received character length: WR3, bits D7 and D6
- Transmitted character length: WR5, bits D6 and D5
- Clock rate: WR4, bits D7 and D6
- Number of stop bits: WR4, bits D3 and D2
- Odd, even, or no parity: WR4, bits D1 and D0
- Interrupt mode: WR1, WR2
- Receiver enable: WR3, bit D0
  or
- Transmitter enable: WR5, bit D3

Figure 3-19 shows the asynchronous mode register setup.

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 B/CHAR 11 RX 8 B/CHAR		AUTO ENABLES	0	0	0	0	RX ENABLE
WR4	00 X1 CLOCK 01 X16 CLOCK 10 X32 CLOCK 11 X64 CLOCK		0	0	00 ENABLE SYNC MODES 01 1 STOP BIT 10 1½ STOP BITS 11 2 STOP BITS		EVEN/ ODD PARITY	PARITY ENABLE
WR5	DTR	00 TX 5 B/CHAR 01 TX 7 B/CHAR 10 TX 6 B/CHAR 11 TX 8 B/CHAR		SEND BREAK	TX ENABLE	0	RTS	0

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Figure 3-19 Asynchronous Mode Register Setup

NOTE
Paragraph 3.4.11.4 gives information on the modem control bits DTR (bit D7) and RTS (bit D1) of register WR5.

When loading these parameters into the MPSC, WR4 information must be written before the WR1, WR3, and WR5 parameters/commands.

For transmission via a modem or RS-423 interface, the Request To Send bit (RTS) (WR5; D1) and Data Terminal Ready bit (DTR) (WR5; D7) must be set along with the Transmit Enable bit (WR5; D3). Setting the Auto Enables bit (WR3; D5) allows the programmer to send the first character of the message without waiting for a Clear To Send (CTS).

Both the framing error and receive overrun error flags are latched and cause an interrupt.

If the External/Status Interrupt bit (WR1; D0) is enabled, Break Detect (RR0; D7) and Carrier Detect (RR0; D3) cause an interrupt. Reset External/Status Interrupts (WR0; D5, D4, D3) clears Break Detect and Carrier Detect bits if they are set.

A status read after a data read includes error status for the next word in the buffer. If the Interrupt on First Character (WR1; D4, D3) is selected, then data and error status are held until an error reset command (WR0; D5, D4, D3) is given.

If the interrupt on the every character mode bit (WR1; D4, D3) is selected, the interrupt vector is different if there is an error status in RR1. When the character is read, the error status bit is set and the Special Receive Condition vector is returned if Status Affects vector (WR1; D2) is selected.

In a polled environment, the Receive Character Available bit (RR0; D0) must be monitored so that the CPU can determine when data is available. The bit is reset automatically when the data is read. If the X1 clock mode is selected, the bit synchronization must be accomplished externally.

3.4.14.2 Synchronous Operation (Monosynchronous, Bisynchronous) – Synchronous operation is a method of data transmission in which the transmitting station is synchronized to the receiving station through the recognition of a special synchronous character(s) (byte synchronous) or bit patterns (bit synchronous). Two examples of byte synchronous communications protocol are monosync and bisync. Monosync has one starting synchronous character per message, while bisynchronous has two starting sync characters per message. Bit synchronous (HDLC/SDLC) operation is described in Paragraph 3.4.14.3.

When using the MPSC for monosynchronous or bisynchronous communications, the following registers must be initialized with the specified parameters.

- Odd or even parity: WR4, bits D1 and D0
- X1 clock mode: WR4, bits D7 and D6
- 8- or 16-bit synchronous character: WR4, bits D5 and D4
- CRC polynomial: WR5, bit D2
- Transmitter enable: WR5, bit D3
- Interrupt modes: WR1, WR2
- Transmit character length: WR5, bits D6 and D5
- Receive character length: WR3, bits D7 and D6

Figure 3-20 shows the synchronous mode register setup for monosynchronous or bisynchronous communications.

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 B/CHAR 11 RX 8 B/CHAR		AUTO ENABLES	ENTER HUNT MODE	RX CRC ENABLE	0	SYNC CHAR LOAD INHIBIT	RX ENABLE
WR4	0	0	00 8-BIT SYNC 01 16-BIT SYNC 11 EXT SYNC		0	0	EVEN/ ODD PARITY	PARITY ENABLE
WR5	DTR	00 TX 5 B/CHAR 01 TX 7 B/CHAR 10 TX 6 B/CHAR 11 TX 8 B/CHAR		SEND BREAK	TX ENABLE	1 (SELECTS CRC-16)	RTS	TX CRC ENABLE

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Figure 3-20 Synchronous Mode Register Setup – Monosynchronous, Bisynchronous

NOTE

Paragraph 3.4.11.4 gives information on the modem control bits DTR (bit D7) and RTS (bit D1) of register WR5.

WR4 parameters must be written before WR1, WR3, WR5, WR6, and WR7.

The data is transmitted on the falling edge of the transmit clock (TXC) and is received on the rising edge of the receive clock (RXC). The X1 clock is used for both transmit and receive operations for all three synchronous modes: monosynchronous, bisynchronous, and external.

3.4.14.3 Synchronous Operation (HDLC/SDLC) – HDLC/SDLC synchronous communications is a bit-oriented, code independent protocol for data transmission between a transmitting and receiving station. The high level data link control (HDLC) is a standard communication link protocol established by the International Standards Organization (ISO). HDLC is the protocol used to implement ISO X.25 packet switching systems. The synchronous data link control (SDLC) is a communications link protocol for implementing the system network architecture (SNA). Both HDLC and SDLC are ideal for full-duplex communications.

When using the MPSC for HDLC or SDLC communications, the following registers must be initialized with the specified parameters.

- SDLC mode: WR4, bits D5 and D4
- SDLC polynomial: WR5, bit D2
- Request to send, data terminal ready, and transmit character length: WR5, bits D6 and D5
- Interrupt modes: WR1, WR2
- Transmit enable: WR5, bit D3
- Receive enable: WR3, bit D0
- Auto enable: WR3, bit D5
- External/status interrupt: WR1, bit D0

WR4 parameters must be written before WR1, WR3, WR5, WR6, and WR7.

Figure 3-21 shows the synchronous mode register setup for HDLC or SDLC communications.

REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 B/CHAR 11 RX 8 B/CHAR		AUTO ENABLES	ENTER HUNT MODE	RX CRC ENABLE	ADDRESS SEARCH MODE	0	RX ENABLE
WR4	0	0	1 0 (SELECTS SDLC/ HDLC MODE)		0	0	0	0
WR5	DTR	00 TX ≤5 B/CHAR 01 TX 7 B/CHAR 10 TX 6 B/CHAR 11 TX 8 B/CHAR		0	TX ENABLE	0 (SELECTS SDLC/ HDLC CRC)	RTS	TX CRC ENABLE

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Figure 3-21 Synchronous Mode Register Setup – HLDC/SLDC

NOTE

Paragraph 3.4.11.4 gives information on the modem control bits DTR (bit D7) and RTS (bit D1) of register WR5.

3.4.15 MPSC Printer Channel

The printer channel (channel B) of the MPSC, as a general-purpose printer port, provides an EIA RS-423 interface compatible with a number of Digital printers. The printer transmit/receive data and printer control signals are routed from the MPSC to the printer through connector J2 on the system module. The following EIA signals are supported.

- Transmit Data (PRT TXD)
- Receive Data (PRT RXD)
- Data Terminal Ready (PTR DTRL)
- Data Set Ready (PTR DSR), always asserted high
- Clear To Send (PTR CTS), always asserted high

Data transmission between the MPSC and the printer is an asynchronous operation. The MPSC WR3, WR4, and WR5 registers must be initialized with the character format required for asynchronous operation as described in Paragraph 3.4.14.1.

Software programmable character formats that are supported are 5 to 8 bits per character with 1 or 2 stop bits per character. Parity can be selected as odd, even, or none. Software should support XON/XOFF restraint protocol for the printer port. The data set ready (DSR) and clear to send (CTS) outputs of the printer port are tied to +5 V and therefore are always asserted high (1). A null modem cable is not required, and the printer is directly connected to the printer connector on the system module.

The printer port supplies the following software programmable baud rates.

75, 150, 300, 600, 1200, 2400, 4800, 9600

To set the baud rates write a byte to the printer baud rate register at address 0EH. The three least significant bits of the byte D<2:0> select a printer transmitter and receiver clock (PRINTER CLK) frequency, that is 16 times the baud rate. The transmitter and receiver clocks for the printer port cannot be independently programmed. Note that bit D<3> of the printer baud rate register selects either an internal or external transmitter and receiver clock for the communications channel.

Figure 3-22 shows the format for the printer baud rate register.

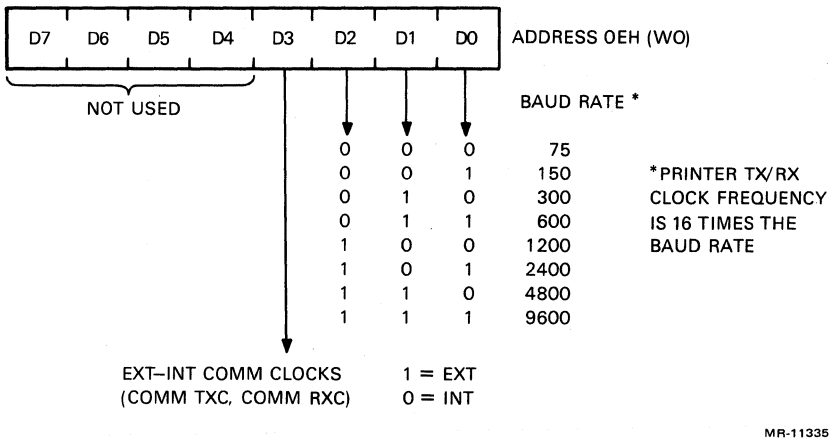


Figure 3-22 Printer Baud Rate Register Format

3.4.16 Keyboard Interface

The keyboard interface is a serial port (J3) on the system module that performs asynchronous serial communications between the keyboard and the 8088 processor using an 8251A programmable synchronous/asynchronous receiver-transmitter (PUSART), a line driver, and a line receiver. The interface provides standard EIA RS-423 signal levels and communicates with the keyboard using full-duplex communications protocol. The interface transfers the character information in groups of 8-bit standard patterns described by the American Standard Code for Information Interchange (ASCII). The character information is transferred at a fixed 4800 baud rate, with an 8-bit, no parity character format.

3.4.16.1 8251A PUSART General Description – The 8251A PUSART is a 28-pin, dual-in-line, microcomputer peripheral device. It contains a transmitter, receiver, I/O buffer, read/write control logic, and shift registers for controlling synchronous or asynchronous data transfers between the 8088 processor and the keyboard. The PUSART, as implemented in the PC100-B system module, is programmed to operate only in the asynchronous mode. The PUSART converts parallel data from the BAD<7:0> bus into serial data for transmission to the keyboard and converts serial data from the keyboard into parallel data that is placed on the BAD<7:0> bus for processing by the 8088. Table 3-27 describes the 8251A pin functions.

The system's software that programs internal control, status, and data buffer registers control the functions of the PUSART. These registers are described in the paragraphs after Table 3-27.

Table 3-27 8251A PUSART Pin Descriptions

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
1,2,5, 6,7,8, 27,28	BAD<7:0>	D7–DO	I/O	DATA BUS: This bus transfers data, control, command, and status information between the 8088 processor and the keyboard PUSART. The PUSART transmits or receives data upon execution of I/O instructions from the 8088. BAD<0> is the least significant bit.
3	KBD RXD	RXD	I	KEYBOARD RECEIVE DATA: This signal is serial input from the keyboard.
4	GND	GND		GROUND.
9	KBD RXTXC	TXC	I	KEYBOARD RECEIVE/TRANSMIT CLOCK: This signal controls the rate at which the character is transmitted to the keyboard. In asynchronous mode, the frequency of KBD RXTXC is 16 times the 4800 keyboard baud rate.
10	WR88 L	WR	I	WRITE 8088: This signal, when low (0), indicates that the 8088 processor is writing data or control information to the PUSART.
11	KBD SEL L	CS	I	KEYBOARD SELECT: This signal, when low (0), enables the PUSART to accept data, control, and command inputs from the 8088 processor during a write cycle, or to transmit data or status inputs to the 8088 during a read cycle.
12	A<0>	C/D	I	CONTROL/DATA SELECT: This address bit, in conjunction with the WR88 and RD88 inputs, informs the PUSART that the word on the data bus BAD<7:0> is either a data character, control word, or status information. 1 = Control, 0 = Data.

* O = Output, I = Input, I/O = Input/Output

Table 3-27 8251A PUSART Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
13	RD88 L	RD	I	READ 8088: This signal, when low (0), indicates that the 8088 processor is reading data or status information from the PUSART.
14	KBD INT L	RXRDY	O	RECEIVER READY: When low (0), this signal interrupts the 8088 processor to indicate that the PUSART is ready to accept a character. RXRDY is automatically reset when the 8088 processor reads the character.
15	KBD INT L	TXRDY	O	TRANSMITTER READY: When low (0), this signal interrupts the 8088 processor to indicate that the PUSART is ready to accept a character. TXRDY is automatically reset when a character is loaded from the 8088 processor.
16		SYNDET	I/O	SYNC DETECT: This pin is not used by Rainbow computers.
17		CTS	I	CLEAR TO SEND: This signal, when low (0), enables the PUSART to transmit serial data if the transmitter enable bit TXEN in the command byte is high (1). This signal is tied to ground in Rainbow computers.
18		TXEMPTY	O	TRANSMITTER EMPTY: This signal is not used in Rainbow computers.
19	KBD TXD	TXD	O	KEYBOARD TRANSMITTED DATA: This signal is the serial transmitted data from PUSART to the keyboard.
20	2.5 MHZ	CLK	I	CLOCK: This clock input generates internal PUSART timing and is connected to the 2.5 MHz clock source.

* O = Output, I = Input, I/O = Input/Output

Table 3-27 8251A PUSART Pin Descriptions (Cont)

Pin Number	Signal Mnemonic	Pin Symbol	Direction*	Signal Name and Function
21	INIT L	RESET	I	INITIALIZE: During power-up, this signal is low (0). The low signal forces the PUSART to an idle state. The PUSART will remain in the idle state until a new set of control words is written into the PUSART.
22		DSR	I	DATA SET READY: During normal operation, this signal is inactive high (1). During manufacturing testing, this signal is jumpered to ground.
23		RTS	O	REQUEST TO SEND: This signal is not used in Rainbow computers.
24	VECTOR SEL L	DTR	O	VECTOR SELECT: This signal is used in Rainbow PC100-B and 100+ computers to relocate hardware interrupt vectors. It is not used in Rainbow PC100-A computers.
25	KBD RXTXC	RXC	I	KEYBOARD RECEIVE/TRANSMIT CLOCK: This signal controls the rate at which the PUSART receives characters. In asynchronous mode, the frequency of KBD RXTC is 16 times the 4800 keyboard baud rate.
26	+5 V	VCC		POWER: +5 V Supply

* O = Output, I = Input, I/O = Input/Output

3.4.16.2 Control Register: 8251A – The 8088 processor must load a set of control words into the control register, which is an 8-bit write-only register before the PUSART can transmit or receive data. These control words define the complete functional definition of the PUSART and must immediately follow a reset operation (internal or external). The control words are split into two formats:

1. mode instruction, and
2. command instruction.

The mode instruction defines the general characteristics of the PUSART. It must follow a reset operation. Once the mode instruction has been written into the PUSART, command instructions can be written.

The command instruction defines a status word that controls the operation of the PUSART. Both the mode instruction and command instruction must conform to a specified sequence for proper operation. The mode instruction must be written immediately following a reset operation, prior to using the PUSART for data communications. All control words written into the PUSART after the mode instruction will load the command instruction. Command instructions can be written into the PUSART at any time in the data block during operation of the PUSART. To return to the mode instruction format, a bit (D6) in the command instruction word can be set to initiate an internal reset operation that automatically places the PUSART back into the mode instruction format.

To access the control register perform a write operation to address 11H. Figures 3-23 and 3-24 show the mode instruction and command instruction formats.

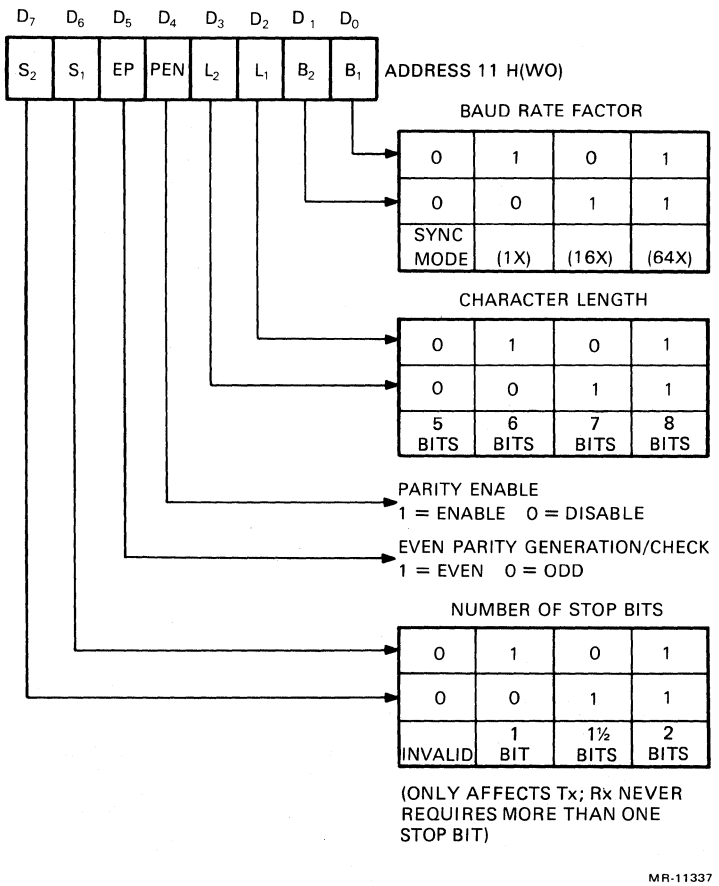
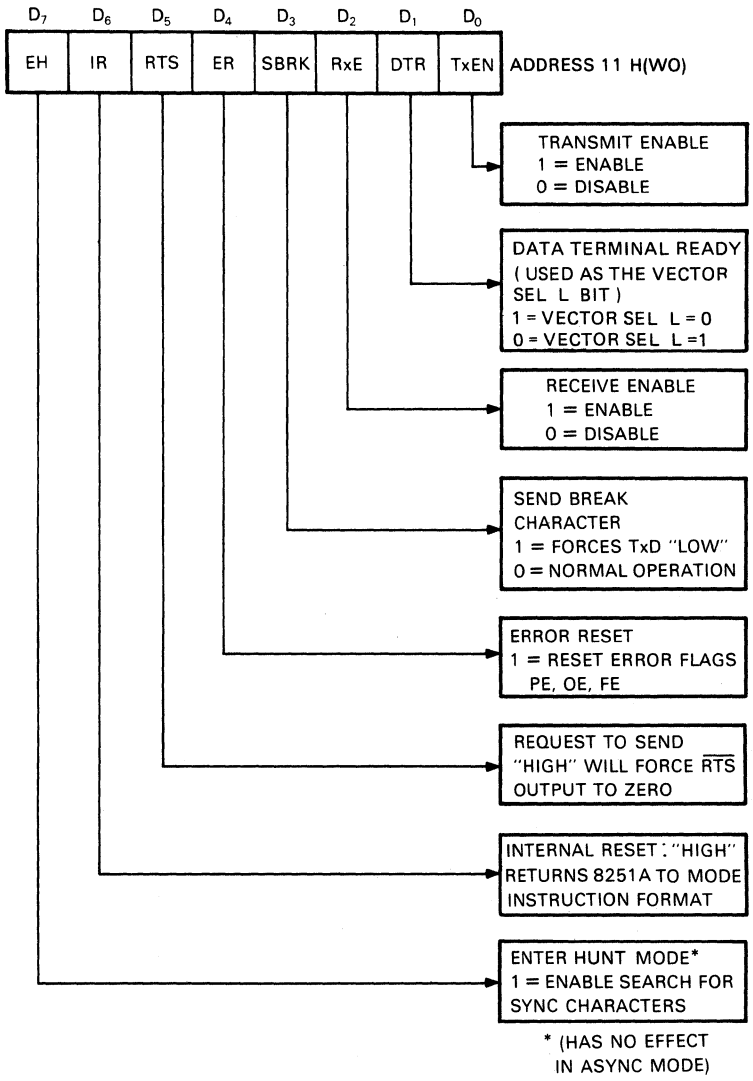


Figure 3-23 Mode Instruction (8251A) Format



NOTE: ERROR RESET MUST BE PERFORMED WHENEVER RxENABLE AND ENTER HUNT ARE PROGRAMMED.

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Figure 3-24 Command Instruction (8251A) Format

3.4.16.3 Status Register: 8251A – The status register is an 8-bit read-only register that holds the status of the active device to determine if data transfer errors or other conditions have occurred that require 8088 processor intervention. Issuing a normal read command at address 11H allows the status of the active device to be read at any time.

Some of the bits in the status register have identical meanings to the pin descriptions, listed in Table 3-27, so that the PUSART can be used in a completely polled environment or in an interrupt driven environment. Figure 3-25 shows the status register format.

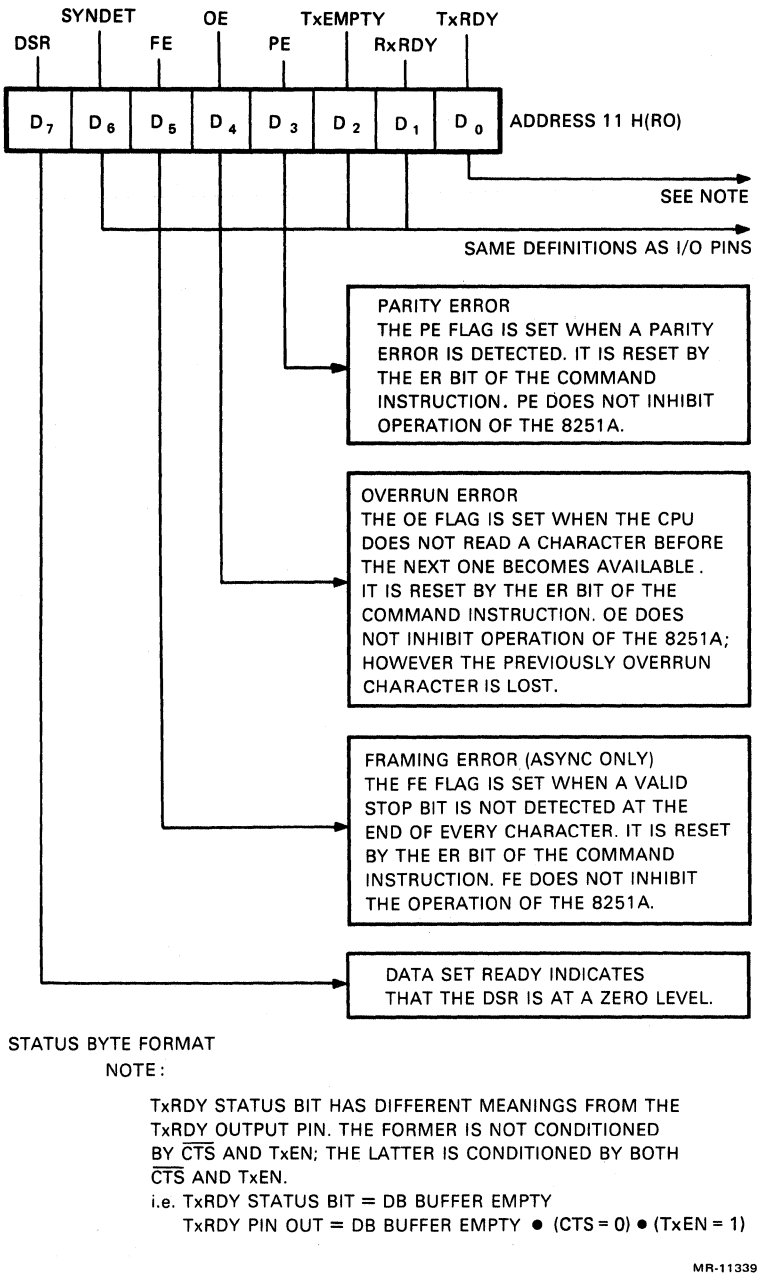

Figure 3-25 Status Register (8251A) Format

3.4.16.4 Transmit and Receive Data Registers: 8251A – The transmit data (WO) and receive data (RO) registers hold the 8-bit characters and the start/stop bits transmitted to or received from the keyboard. In the Rainbow computer, the transmit and receive character length will always be eight bits with no parity. The mode instructions written into the control register following a reset operation specify the character length and the number of stop bits.

When transmitting data, the 8251A will add start and stop bits to the 8-bit character output of the 8088 processor and then shift out the assembled serial data to the keyboard. When receiving data, the 8251A shifts the serial data (character, start, and stop bits) from the keyboard into the receive data register. The 8251A then checks the received data for the correct format, discards the start and stop bits, and places the 8-bit character in parallel on the BAD<7:0> bus. To access the keyboard data registers, perform a write or read operation to address 10H.

Figure 3-26 shows the transmit and receive data formats.

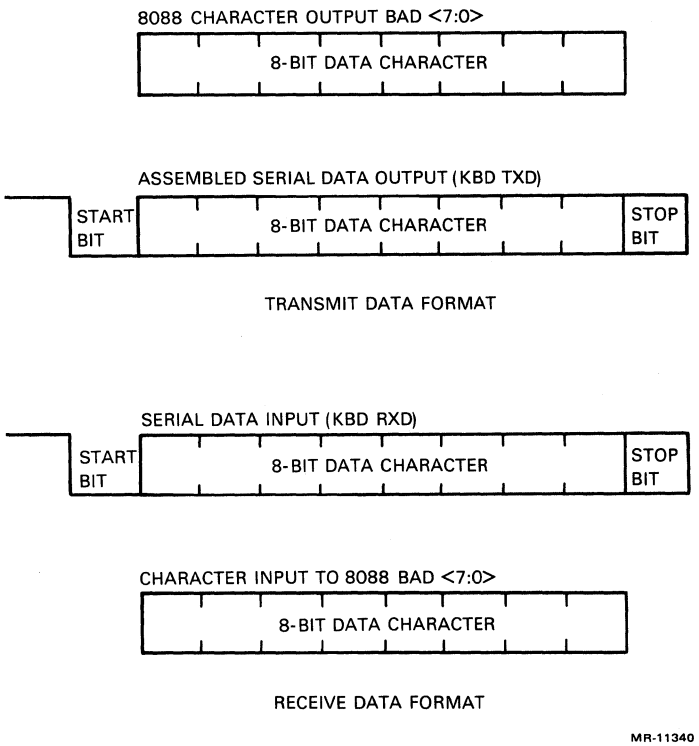

Figure 3-26 Transmit and Receive Data Format

3.4.17 MHFU Detection Logic

A massive hardware failure (MHFU) detection circuit on the system module is provided to detect that the 8088 processor has lost most of its functions. If the 8088 processor does not acknowledge a video processor vertical interrupt within approximately 108 ms, the MHFU detection circuit will apply a reset signal to the 8088 processor for 108 ms. This reset causes the 8088 processor to begin executing the power-up or reset boot ROM code at address FFFF:0.

To disable MHFU detection you write to the DC12 control chip write register at address 10CH. To enable it, you write to the DC12 control chip at address 0CH. The status of the MHFU enable/disable signal may be read from bit D<5> of the communications status register at address 02H. When the firmware begins executing the program at location FFFF:0, it assumes a power-up reset if MHFU detection is disabled or an MHFU reset if MHFU detection is enabled.

CAUTION

Leaving interrupts disabled for 100 ms or more causes the MHFU detection circuit to be activated. If it is mandatory to leave the interrupts masked for a longer period, use the following procedure to disable the MHFU detection circuit. This procedure may adversely affect the video display and any real-time dependent system; use with care and discretion.

1. **Disable interrupts using a CLI instruction.**

2. **Disable the MHFU detection circuit by writing a 00H to the 8088 processor I/O port 10CH. The MHFU detection circuit re-enables automatically, after the 8088 interrupt mask has been re-enabled, using the STI instruction.**

3.4.18 PC100-B System Module Firmware

The PC100-B firmware programs are contained in the 32K byte ROM. This 32K byte ROM comprises a set of two 16K × 8 bit ROMs (ROM 0 and ROM 1). ROM 0 contains the code for diagnostics, bootstrap, and part of the VT102 emulation code. ROM 1 contains the remainder of the VT102 emulation code and the language character translation codes necessary to support the 15 international keyboards used with Rainbow computers.

The PC100-B firmware includes two variations of VT102 emulation: terminal mode and console mode. Terminal mode enables the Rainbow computer to act like a VT102 terminal connected to a remote computer via the communications port. The console mode enables the Rainbow computer to act like a VT102 terminal (without printer port and using FDX data leads only as a protocol) when running programs on the Rainbow model PC100-B.

The firmware provides services to a user for console-out, console-in, console-in-status, enable/disable cursor, return version number, change interrupt vector map, ring the keyboard bell, transferring screen data a line at a time, initialize interrupt vectors, return clock rate, 16-bit key data, and keyboard LED control.

The operating system in console mode supplies the communications and printer port drivers.

The firmware also provides selftest diagnostics and a minimal bootstrap loader for diskette drives or the Winchester hard disk drive.

The PC100-B firmware provides the following 13 services.

1. Power-up initialization of hardware
2. Selftest diagnostics
3. VT102 emulation – available in terminal and console modes
4. Image of Z80A RAM space to be loaded
5. Boot loader to read track 0, sector 1 of a diskette drive or Winchester disk drive
6. Opening menu selection process
7. Automatic shut-off screen display after 30 minutes of non-use, and display restoration on first activity (any keyboard key or received char)
8. Rainbow PC100-A product supports the 15 keyboards
9. National language power-up and selftest system messages
10. National language boot menu
11. Implementation of the compose algorithm
12. National language set-up
13. Choice of Digital 8-bit codes or National Replacement Characters (NRC)

The firmware is organized so the VT102 emulation primitives form the console functionality for applications use through the interface layer. When in terminal mode a background loop is entered which calls on the console primitives and adds the necessary functionality to provide full terminal mode.

An interface layer is placed over the console primitives to provide an application with means of accessing those primitives.

NOTE

In console mode no support is provided for the printer or the communication ports. The operating system must directly control this hardware (MPSC).

For applications that need more immediate control of the hardware, the firmware provides services to obtain "low level" key information, enable/disable cursor, and transfer data directly to screen RAM.

Use a software interrupt, with arguments passed and returned in CPU registers to implement the interface between the application and the firmware.

This leads to a layered structure as shown in Figure 3-27. The firmware regards the operating system in this example as an application. It actually can be anything, including another firmware routine.

All entries to firmware routines from external processes are via a software interrupt, interrupt vector 40H. This makes the interface release-independent because ROM code loads the proper vectors during initialization.

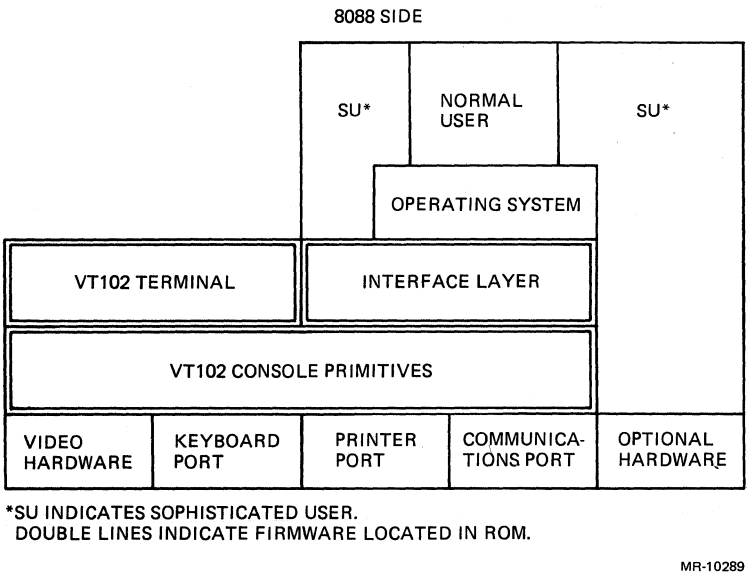

Figure 3-27 Firmware Organization

3.5 SYSTEM MODULE CONNECTORS

The system module contains nine connectors that provide the interconnection to the other system units and option modules. Three of these connectors (J1, J2, and J3) are D-type subminiature connectors that connect the system unit via cables to the video monitor, printer, and a remote computer. The other six connectors (J4–J9) are printed circuit board headers that provide the signal and power connection for option modules, the RX50 controller module, and the power supply. Figure 3-2 shows the connector locations on the system module. Paragraphs 3.5.1–3.5.8 describe the connector signals.

3.5.1 Communications Connector (J1) Signals

The communications connector (J1) allows the Rainbow computer to communicate with a remote computer over a cable connected directly to the remote computer or to a modem or telephone line. The Rainbow computer communicates with the remote computer using any one of the following three communications protocols.

1. FDXA Full-duplex with no modem control (data leads only)
2. FDXB Full-duplex with modem control
3. FDXC Asymmetrical full-duplex with modem control

The communications connector is configured as data terminal equipment (DTE). Table 3-28 lists the signals transmitted through the connector.

Table 3-28 Communications Connector (J1) Signals

Pin Number	Signal	Mnemonic	Direction*
1	Protective Ground	PROT GND	
2	Transmit Data	XMIT DATA	Out
3	Receive Data	REC DATA	In
4	Request to Send	RTS	Out
5	Clear to Send	CTS	In
6	Data Set Ready	DSR	In
7	Signal Ground	GND	
8	Receive Line Signal Detect	RLSD	In
9	Not Used		
10	Not Used		
11	Not Used		
12	Speed Indicator/Secondary Receive Line Signal Detect	SI/SRLSD	In
13	Not Used		
14	Not Used		
15	Send Clock	SEND CLK	In
16	Not Used		
17	Receive Clock	REC CLK	In
18	Not Used		
19	Secondary Request to Send	SRTS	Out
20	Data Terminal Ready	DTR	Out
21	Not Used		
22	Ring Indicator	RI	In
23	Speed Select	SPDSEL	Out
24	Not Used		
25	Not Used		

*Direction of signals with respect to the system module

Communications Signal Functions – Table 3-29 describes the functions of the signals on the communications connector pins.

Table 3-29 Communications Signal Functions

Signal	Function*
Protective Ground	This signal is connected to chassis ground via jumper W17. This jumper can be cut out if required by local conditions.
Transmitted Data	Signals on this line represent the serially encoded characters that are transmitted from the communications connector. This signal is held in the marking state during intervals between characters and at all times when no data is being transmitted.
Receive Data	Signals on this line represent the serially encoded characters to be received.
Request to Send	Assertion of this signal indicates that the channel is ready for transmission.
Clear to Send	When this signal is asserted, it indicates that the modem is ready for transmission.
Data Set Ready	The ON condition of DSR indicates that the modem is in data mode, and that the modem asserts valid control signals.
Signal Ground	This circuit establishes the common ground reference potential for all interface circuits except protective ground.
Receive Line Signal Detector	This is also called Carrier Detect. The modem asserts this signal ON when the received signal is of sufficient quality and magnitude.
Speed Indicator	This signal allows some modems to control channel bit rates.
Secondary Receive Line Signal Detect†	This circuit is used in half-duplex coded control with reverse channel.
Secondary Clear to Send‡	In FDX, this signal is the same as clear to send. In asymmetric FDX, it provides the functionality for a secondary channel.

* The following terminology is used interchangeably to describe the communications signals:
Negative Voltage = 1 = Mark = OFF
Positive Voltage = 0 = Space = ON

† Secondary Receive Line Signal Detect and Speed Indicator are two different functions performed by the same physical line.

‡ These signals are supported by using a special cable for FDXC modem protocol.

Table 3-29 Communications Signal Functions (Cont)

Signal	Function*
Secondary Transmitted Data‡	In FDX, this signal is the same as Transmitted Data, but when operating in asymmetric FDX, it provides functionality for the secondary channel.
Send Clock	This is an external transmit clock that is supplied by the modem. It substitutes for the communications transmit clock when the synchronous select bit is set.
Receive Clock	The modem supplies this external receive clock. It substitutes for the communication receive clock when the synchronous select bit is set.
Secondary Request to Send‡	This signal is used for HDX restraint mode and asymmetric FDX Secondary Request to Send.
Data Terminal Ready	This signal is turned ON whenever the channel is ready for transmission.
Ring Indicator	The ON condition indicates that a ringing signal is being received from the communications line.
Speed Select	This signal allows the 8088 processor to control the modulation method of the modem to coincide with its selected bit rate.

* The following terminology is used interchangeably to describe the communications signals:
Negative Voltage = 1 = Mark = OFF
Positive Voltage = 0 = Space = ON
† Secondary Receive Line Signal Detect and Speed Indicator are two different functions performed by the same physical line.
‡ These signals are supported by using a special cable for FDXC modem protocol.

3.5.2 Printer Connector (J2) Signals

The printer connector signals meet the following standards.

- Electronic Industry Association (EIA) standard RS-423 and RS-232-C
- International Telegraph and Telephone Consultative Committee (CCITT), recommendation V.28

The printer connector is configured as Data Communications Equipment (DCE).

Table 3-30 lists the printer connector signals and their pin assignments. Signals and pins not listed are not used by the Rainbow computer.

Table 3-30 Printer Connector (J2) Signals

Pin Number	Signal	Mnemonic	CCITT/EIA	Description
1	Protective Ground	PROT GND	101/AA	Chassis ground; ac power cord ground. This signal is connected to chassis ground via jumper W16. This jumper may be cut out if required by local conditions.
2	Transmitted Data (input)	TXD	103/BA	XON/XOFF control signals and other characters from the printer.
3	Received Data (output)	RXD	104/BB	Data received by the printer from the Rainbow computer. This signal is asserted high (mark state) when not in use.
5	Clear to Send (output)	CTS	106/CB	Always asserted high (mark state).
6	Data Set Ready (output)	DSR	107/CC	Always asserted high.
7	Signal Ground	SGND	102/AB	Common ground for all signals.
20	Data Terminal Ready (input)	DTR	108.2/CD	Indicates printer status. If the printer turns off DTR, the Rainbow PC100-B stops sending characters to the printer. When the printer turns on DTR, the Rainbow PC100-B sends characters to the printer. The Rainbow PC100-A ignores Data Terminal Ready.

3.5.3 Keyboard/Monitor Connector (J3) Signals

This connector carries the video signals, data signals, and power which the keyboard and monitor use. The connector signals meet the following standards.

- Video signals – Similar to EIA RS-170

NOTE

The composite video (Mono Video) signal on pin 12 is dc coupled and therefore not in strict agreement with RS-170. To agree with RS-170, the composite video signal requires a 10 microfarad capacitor in series with the output.

- Keyboard data signals – EIA RS-423

Table 3-31 lists the keyboard/monitor signals and their pin assignments.

Table 3-31 Keyboard/Monitor Connector (J3) Signals

Pin Number	Signal	Mnemonic	Description*
1	Red shield ground		Shield ground for color monitor cable
2	Green shield ground		Shield ground for color monitor cable
3	Blue shield ground		Shield ground for color monitor cable
4	Mono shield ground		Shield ground for composite video coaxial cable
5,6	Ground		Video, data, and power ground
7,8	+12 V		+12 V power to monitor and keyboard
9	Blue video		Composite blue video signal from graphics option
10	Green video		Composite green video signal from graphics option
11	Red video		Composite red video signal from graphics option
12	Mono video		Composite monochrome video output from the video processor on the system module
13	Not used		
14	Keyboard received data (output)	KBD RXD	Serial data transmitted to keyboard
15	Keyboard transmitted data (input)	KBD TXD	Serial data received from keyboard

* In a system configuration with a color/graphics option and color monitor only, the green gun of the color monitor is usually connected to the monochrome video output, rather than the green video output.

3.5.4 Hard Disk Controller/Extended Communications Connectors (J4 and J5)

Connectors J4 and J5 are 40-pin headers that provide the system module interface for the hard disk controller or the extended communications option. The connector signals used depend on which module is installed. Tables 3-32 and 3-33 describe the connector signals.

Table 3-32 Hard Disk Controller/Extended Communications Connector (J4) Signals

Pin Number*	Signal Used by Hard Disk Controller	Extented Comm. Option	Signal Name	Mnemonic	Direction†
1	X	X	Initialize	INIT L	O
2		X	−12 V Power	−12 V	O
3	X	X	Bundle Option Present	BDL PRES L	I
6,18,20,22 24,26,28	X	X	Ground	GND	O
4,8	X	X	+12 V Power	+12 V	O
5		X	DMA Controller Interrupt	DMAC INT L	I
7		X	Bundle Select 1	BDL SEL 1 L	O
9		X	Bundle Request	BDL REQ L	I
11	Not Used	Not Used	Bundle Select 3	BDL SEL 3 L	O
12,16	X	X	+5 V Power	+5 V	O
13	Not Used	Not Used	Bundle Select 4	BDL SEL 4 L	O
23	X	X	Bundle Interrupt	BDL INT L	I
25		X	Bundle Acknowledge	BDL ACK L	O
27	Not Used	Not Used		2.5 MHz	O
29		X	Extended Comm. Clock Pulses	05A H	O
31		X	Extended Comm. Clock Pulses	05C L	O
33	X	X	8088 Write	BWR 88 H	O
35	X	X	8088 Read	BRD 88 H	O
40		X	Nonshared Cycle	NONSHRCYC H	O

* Pins not listed are not used by the hard disk controller or extended communications option.

† Direction of signal with respect to system module, O = Output, I = Input.

Table 3-33 Hard Disk Controller/Extended Communications Connector (J5) Signals

Pin Number*	Signal Used by Hard Disk Controller	Extended Comm. Option	Signal Name	Mnemonic	Direction†
1,3,5,7 9,11,13,15	X	X	Address Data Bits 0–7	BAD 0–7 H	I/O
17,19,21,23	X	X	Latched Address Bits 0–3	A 0–3 H	O
25	X	X	Bundle Select 2	BDL SEL 2 L	O
27,31	X	X	+5 V Power	+5 V	O
33,35,37	X	X	Ground	GND	O
2,4,6,8 10,12,14,16		X	Shared Memory Data Bits 0–7	SHD 0–7	I/O
18,20,22,24 26,28,30,32		X	Shared Mem Address Bits 0–7	SHMA 0–7	I
34		X	Shared RAM Row Address Strobe	SHRAM 0 RAS L	I
36		X	Shared RAM Column Address Strobe	SHRAM CAS L	I
38		X	Bundle Shared RAM Read/Write	BDL SH WR L	I
39	Not used	Not used	Shared RAM 1 Row Address Strobe	SHRAM 1 RAS L	O

* Pins 29 and 40 are not used.
† Direction of signal with respect to system module, O = Output, I = Input.

The signals on the J4 connector perform the following functions.

INITIALIZE – This output signal initializes the registers in the hard disk controller or extended communications option when the system is powered up or reset.

BUNDLE OPTION PRESENT – This signal input from the hard disk controller or extended communications option informs the 8088 processor that an option is installed. It is tied to ground in the hard disk controller and extended communications option.

DMA CONTROLLER INTERRUPT – This input signal allows the extended communications option to make direct memory data transfers between Ports A and B and the shared 62K byte and private 2K byte of the 8088 memory without burdening the 8088 with processing interrupts.

BUNDLE SELECT 1 – This output signal selects Port A or Port B transmitter/receiver channel of the MPSC in the extended communications option.

BUNDLE REQUEST – This input signal from the extended communications option informs the shared memory arbitrator that it wishes to use the shared memory.

BUNDLE INTERRUPT – This input signal from the extended communications option or the hard disk controller requests an interrupt to the 8088 processor.

BUNDLE ACKNOWLEDGE – This output signal informs the extended communications option that its interrupt request is acknowledged.

8088 WRITE (BWR 88 H) – This output signal informs the extended communications option or the hard disk controller that the 8088 processor is performing a write cycle.

8088 READ (BRD 88 H) – This output signal informs the extended communications option or the hard disk controller that the 8088 processor is performing a read cycle.

NONSHARED CYCLE – This output signal from the shared memory arbitration logic informs the extended communications option that an unshared memory cycle is in progress.

The signals on the J5 connector perform the following functions.

ADDRESS DATA BITS 0–7 – These signals are the buffered address/data bits to/from the extended communications option or the hard disk controller.

LATCHED ADDRESS BITS 0–3 – These are latched address bits from the 8088 select read/write registers in the extended communications option or the hard disk controller.

BUNDLE SELECT 2L – The extended communications option and the hard disk controller use this output signal. In the extended communications option, the signal selects the DMA controller chip as the I/O device. In the hard disk controller, it enables reading and writing the disk controller registers.

SHARED MEMORY DATA BITS 0–7 – These signals are the eight shared memory data bits to/from the extended communications option.

SHARED MEMORY ADDRESS BITS 0–7 – These signals are the eight address bits from the extended communications option to the shared memory.

SHARED RAM ROW ADDRESS STROBE – This input signal is the row address strobe from the extended communications option.

SHARED RAM COLUMN ADDRESS STROBE – This input signal is the column address strobe from the extended communications option.

BUNDLE SHARED RAM READ/WRITE – This input signal from the DMA controller in the extended communications option enables the shared memory for a read or write operation.

3.5.5 Memory Option Connector (J6) Signals

The memory option plugs into a 52-pin header on the system module. This connector carries all the address, data, and control signals required to operate any one of four available memory option modules.

The PC100-B system module can support the following four option memory modules.

64K byte memory module (PC100-A) PC1XX-AA
192K byte memory module (PC100-A) PC1XX-AB
64K byte memory module (PC100-B) PC1XX-AC
256K byte memory module (PC100-B) PC1XX-AD

Both the PC100-A system module or the PC100-B system module can use memory modules PC1XX-AA and PC1XX-AB. Memory modules PC1XX-AC and PC1XX-AD can be used only in the system module PC100-B.

Whether a PC100-A or PC100-B memory option module is installed on the PC100-B system module affects the functions the signals on five pins (29, 30, 32, 43, and 47) of the J6 connector will perform. Table 3-34 describes the J6 connector signals and their pin assignments.

Table 3-34 Memory Option Connector (J6) Signals

Pin Number*	Signal	Mnemonic	Description
1,2,3,51,52	Ground	GND	
4	Row Address Strobe	RAS88 H	This output signal strobes the row address into the memory extension option.
6	Address Bit 6	A6 H	Memory extension address bit
7	Address Bit 15	A15 H	Memory extension address bit
8	Address Bit 1	A1 H	Memory extension address bit
9	Address Bit 13	A13 H	Memory extension address bit
10	Address Bit 8	A8 H	Memory extension address bit
11	Address Bit 3	A3 H	Memory extension address bit
12	Address Bit 10	A10 H	Memory extension address bit
13	Address Bit 0	A0 H	Memory extension address bit
14	Address Bit 14	A14 H	Memory extension address bit
15	Address Bit 7	A7 H	Memory extension address bit
16	Address Bit 2	A2 H	Memory extension address bit
17	Address Bit 5	A5 H	Memory extension address bit
18	Address Bit 9	A9 H	Memory extension address bit

*Pins not listed are not used by the memory extension option.

Table 3-34 Memory Option Connector (J6) Signals (Cont)

Pin Number*	Signal	Mnemonic	Description
19	Address Bit 12	A12 H	Memory extension address bit
20	8088 Multiplexer Select	MUX 88 H	This signal allows the 8088 processor Address bits <15:10> to be applied to the memory extension option.
21	Address Bit 11	A11 H	Memory extension address bit
22	Address Bit 4	A4 H	Memory extension address bit
23	Refresh Row Address Strobe	RFSH RAS H	This output signal refreshes the memory extension option.
24	Parity Test	PARITY TEST H	This output signal enables parity circuits testing on the memory extension option.
25,27,28,35	+5 V		+5 V output
26	Parity Error	PARITY ERROR L	This input signal informs the 8088 processor that a memory parity error has occurred.
29	Memory Option Present	MEM PRES L	The status of this input signal determines which set of four signals are used to select the memory banks in the PC100-A or PC100-B memory extension options. If a PC100-A memory option is installed, the signal is ground. If a PC100-B memory option is installed, this signal is high.
30	Nonshared Memory Cycle or IO/Memory cycle	NONSHRCYC L/IO/M	When a PC100-A memory option is installed, NONSHRCYC is asserted low to enable memory option accesses. When a PC100-B memory option is installed, the 8088 processor asserts IO/M low to enable memory option accesses.
31	Do Refresh	DO RFSH L	This output signal indicates that the extended memory must be refreshed.
32	Select Memory Bank 2 or Address Bit	S64K 2 L/A17 H	When a PC100-A memory extension option is installed, this output signal selects the second 64K byte memory bank. When the PC100-B memory extension option is installed, address bit 17 is used in conjunction with address bits 16, 18, and 19 to select the memory stack.

*Pins not listed are not used by the memory extension option.

Table 3-34 Memory Option Connector (J6) Signals (Cont)

Pin Number*	Signal	Mnemonic	Description
33	Refresh Done	RFSH DONE H	This output signal indicates that memory refresh operation is completed.
34	Initialize	INIT L	This output signal initializes the memory extension logic on power-up.
36	Buffered Address Data	BAD7 H	Memory extension data bit 7
37	Column Address Strobe	CAS88 H	This output signal strobes the column address into the extended memory.
38	Buffered Address Data	BAD6 H	Memory extension data bit 6
39	Data Transmit/Receive	R/DT	This output signal controls the direction of data to/from the memory extension option. Low = write data, high = read data.
40	Buffered Address Data	BAD5 H	Memory extension data bit 5
41	Memory Read	BRD88 H	When high, this output signal indicates that the 8088 processor is performing a read cycle.
42	Buffered Address Data	BAD4 H	Memory extension data bit 4
43	Select Memory Bank 3 or Address Bit 18	S64K 3 L/A18H	When a PC100-A memory extension option is installed, this output signal selects the third 64K byte memory bank. When the PC100-B memory extension option is installed, address bit 18 is used in conjunction with address bits 16, 17, and 19 to select the memory stack.
44	Buffered Address Data	BAD3 H	Memory extension data bit 3
45	Memory Write	BWR88 L	When low, this output signal indicates that the 8088 processor is performing a write cycle.
46	Buffered Address Data	BAD2 H	Memory extension data bit 2

*Pins not listed are not used by the memory extension option.

Table 3-34 Memory Option Connector (J6) Signals (Cont)

Pin Number*	Signal	Mnemonic	Description
47	Select Memory Bank 1 or Address Bit 16	S64K 1 L/A16 H	When a PC100-A memory extension option is installed, this output signal selects the first 64K byte memory bank. When a PC100-B memory extension option is installed, address bit 16 is used in conjunction with address bits 17, 18, and 19 to select the memory stack.
48	Buffered Address Data	BAD1 H	Memory extension data bit 1
49	Address Bit 19	OCA19 H	Memory extension address bit
50	Buffered Address Data	BAD0 H	Memory extension data bit 0

*Pins not listed are not used by the memory extension option.

3.5.6 Color/Graphics Connector (J7) Signals

The color/graphics option plugs into a 40-pin header on the system module. This connector carries all the address, data, monographics video, direct-drive color monitor signals, and power required for operation of this option. Table 3-35 lists the signals and their pin assignments.

Table 3-35 Color/Graphics Connector (J7) Signals

Pin Number*	Signal	Mnemonic	Description
1	Address Bit 3	A3 H	This output signal accesses the registers in the graphics option.
2	Initialize	INIT L	This output signal initializes the graphics option on power-up.
3	Buffered Address Data	BAD 0	Graphics option data bit 0
4	Graphics Select	GRAPHIC SEL L	This output signal from the 8088 I/O decoders selects the graphics option.
5	Buffered Address Data	BAD 1	Graphics option data bit 1
6	Graphics Read	BRD88 H	This output signal indicates that the 8088 processor is performing a read cycle.
7	Buffered Address Data	BAD 2	Graphics option data bit 2
8	Graphics Write	BWR88 H	This output signal indicates that the 8088 processor is performing a write cycle.
9	Buffered Address Data	BAD 3	Graphics option data bit 3
10,14,16,12	+5 V		+5 V output
11	Buffered Address Data	BAD 4	Graphics option data bit 4
13	Buffered Address Data	BAD 5	Graphics option data bit 5
15	Buffered Address Data	BAD 6	Graphics option data bit 6
17	Buffered Address Data	BAD 7	Graphics option data bit 7
18,20,22, 24,26,28	Ground	GND	
19	Address Bit 0	A0 H	This output signal accesses the registers in the graphics option.
21	Address Bit 1	A1 H	This output signal accesses the registers in the graphics option.
23	Address Bit 2	A2 H	This output signal accesses the registers in the graphics option.
25	Red Drive	RED	This input signal is routed to the keyboard/monitor connector (J3) to directly drive the red gun of a color monitor.

*Pins not listed are not used by the graphics option.

Table 3-35 Color/Graphics Connector (J7) Signals (Cont)

Pin Number*	Signal	Mnemonic	Description
27	Green Drive	GREEN	This input signal is routed to the keyboard/monitor connector (J3) to directly drive the green gun of a color monitor.
29	Blue Drive	BLUE	This input signal is routed to the keyboard/monitor connector (J3) to directly drive the blue gun of a color monitor.
30,32	+12 V		+12 V output
31	Graphics Video 1	GRF VID 1 H	This input signal is 1 of 4 used by the PC100-B system module to provide 16 gray shades on a monochrome monitor.
33	Graphics Video 2	GRF VID 2 H	This input signal is 1 of 4 used by the PC100-B system module to provide 16 gray shades on a monochrome monitor.
34	Graphics Video 3	GRF VID 3 H	This input signal is 1 of 4 used by the PC100-B system module to provide 16 gray shades on a monochrome monitor.
35	Graphics Blanking	GRF BLANK L	This input signal blanks out the graphics display during the CRT beam retrace interval.
36	Graphics Video 4	GRF VID 4 H	This input signal is 1 of 4 used by the PC100-B system module to provide 16 gray shades on a monochrome monitor.
37	Graphics Sync	GRF SYNC L	This input signal is the synchronizing signal for the graphics video.
38	Graphics Interrupt	GRF INTR L	The graphics option asserts this input signal to interrupt the 8088 processor when it wishes to display video.
39	Graphics Option Present	GRAPHICS PRES L	This input signal informs the 8088 processor that the graphics option is installed.
40	Vertical Blanking	VERT BLANK L	This input is the vertical blanking signal for the graphics video.

*Pins not listed are not used by the graphics option.

3.5.7 Power Supply Connector (J8) Signals

The power supply connector on the system module is a 13-pin in-line connector. A 13-pin flat cable, detachable at both ends, connects the system module to the power supply. Table 3-36 lists the power supply dc voltages and control signals that are applied to this connector.

Table 3-36 Power Supply Connector (J8) Signals

Pin Number	Signal	Mnemonic	Description
1	AC Voltage Okay	ACOK H	This signal indicates the presence or absence of valid ac power entering the power supply. When valid ac power is present, this signal will be high. When the ac power is lower than the required minimum input voltage, this signal will be low.
2	Voltage Bias	VBIAS	This signal is connected to the communications control register via a jumper on the system module. The jumper is installed only for manufacturing diagnostic testing.
3	None		This pin is missing to provide a key for the cable connector.
4	−12 V		−12 V input
5, 6	+12 V		+12 V input
7, 8, 9	+5 V		+5 V input
10, 11, 12, 13	Ground	GND	DC power return and signal ground

3.5.8 RX50 Controller Connector (J9) Signals

The RX50 controller connector is a 40-pin header providing the interface between the Z80A processor and the RX50 controller module. This connector carries all the address, read/write data, control signals, and dc power needed for operation of the module. Table 3-37 lists the signals and their pin assignments.

Table 3-37 RX50 Controller Connector (J9) Signals

Pin*	Signal	Mnemonic	Description
1	Diskette Drive Read	ZFPRD L	The Z80A I/O select logic asserts this output signal and allows the RX50 controller module to place read data from the diskette drive onto the Z80A data bus (ZD<7:0>).
2	Printer Transmitted Data	PRT TXD	This output signal is a serial stream of data from the printer PUSART. This data is sent to the data separator circuit when DIAG LOOPBACK H is asserted and allows the 8088 and Z80A processors to test the data separator circuits without the use of a diskette drive.
3	Diskette Drive Write	ZFPWR L	The Z80A I/O select logic asserts this output signal and gates data from the Z80A data bus (ZD<7:0>) into the RX50 controller.
4	Diagnostic Loopback	DIAG LOOPBACK H	This output signal, together with PRT TXD, allows the data separator circuit to be tested through the printer port.
5	Z80A Reset	ZRESET L	This output signal will reset the RX50 controller at power-up.
7	AC Voltage Okay	BACOK H	This output signal allows the RX50 controller to transfer write data to the disk drive only when the ac input to the power supply is at the correct voltage level.
9	Diskette Drive Register Read	ZFPREG RD L	The Z80A I/O select logic asserts this output signal asserts and allows the Z80A processor to read the status of the diskette drive.
10,30	+5 V		+5 V output
11	Z80A Data Bit 7	ZD 7	This bidirectional data bus bit transfers data, control, and status information between the Z80A processor and the RX50 controller.

*Pins not listed are not used by the RX50 Controller Module.

Table 3-37 RX50 Controller Connector (J9) Signals (Cont)

Pin*	Signal	Mnemonic	Description
12	Z80A Address Bit 0	ZA0	Address bit 0 together with address bit 1 selects 1 of 5 registers in the RX50 controller to transmit/receive data on the ZD<7:0> bus.
13	Z80A Data bit 6	ZD6	This bidirectional data bus bit transfers data, control, and status information between the Z80A processor and the RX50 controller.
14,24	Ground	GND	Signal and power ground
15	Z80A Data Bit 5	ZD5	
17	Z80A Data Bit 4	ZD4	
19	Z80A Data Bit 3	ZD3	These bidirectional data bus bits transfer data, control, and status information between the Z80A processor and the RX50 controller.
21	Z80A Data Bit 2	ZD2	
23	Z80A Data Bit 1	ZD1	
25	Z80A Data Bit 0	ZD0	
26	Z80A Address Bit 1	ZA1	Address bit 1 together with address bit 0 selects 1 of 5 registers in the RX50 controller to transmit/receive data on the ZD<7:0> bus.
27	8 MHz Clock Pulse	08 A H	The write precompensation circuit in the RX50 controller uses this clock pulse signal.
29	4 MHz Clock Pulse	4 MHZ	The write precompensation circuit in the RX50 controller uses this clock pulse signal.
31	2 MHz Clock Pulse	2 MHZ	The write precompensation circuit in the RX50 controller uses this clock pulse signal.
32,34	+12 V		+12 V Output
33	1 MHz Clock Pulse	1 MHZ	This clock pulse signal is used by the write precompensation circuit in the RX50 controller.

*Pins not listed are not used by the RX50 Controller Module.

Table 3-37 RX50 controller Connector (J9) Signals (Cont)

Pin*	Signal	Mnemonic	Description
35	500 kHz Clock Pulse	500 KHZ	This clock pulse signal is used by the data separator circuit in the RX50 controller.
36	−12 V		−12 V Output
37	Diskette Register Write	ZFPREG WR L	The Z80A I/O select logic asserts this output signal and enables a write only control register in the RX50 controller. The contents of the register select the drive; turn on the drive motor; write the precompensation values; and select diskette surface to be accessed.
38	Diskette Drive Present	FLPY PRES L	This input signal informs the 8088 processor that the RX50 controller is installed.
39	Diagnostic Read	ZDIAG RD L	The Z80A I/O select logic and asserts this output signal and enables the general/status register on the RX50 controller to place diskette drive status information on the ZD<7:0> data bus.

*Pins not listed are not used by the RX50 controller module.

3.6 SYSTEM MODULE SPECIFICATIONS

The following paragraphs describe the physical, power, and environmental specifications for the system module.

3.6.1 Physical Dimensions

Length	35.56 cm (14 in)
Width	26.42 cm (10.4 in)
Height	2.25 cm (0.9 in) The module height is the combined thickness of the printed circuit board and printed circuit board connectors.

3.6.2 DC Power

The system module requires the following dc power.

+5 Vdc	±5% at 5.5 A maximum
+12 Vdc	±10% at 0.3 A maximum
−12 Vdc	±10% at 0.3 A maximum

3.6.3 Environmental

The system module meets the environmental requirements of Digital Equipment Corporation Standard 102, Class B, and the conducted and radiation emission limits which the FCC rules established for Class B computing devices.

3.6.3.1 Temperature

Storage	−40°C to 80°C (−40°F to 176°F)

When the system module is at a temperature beyond the operating range, it must first be brought to an environment within the operating range and be allowed to stabilize for at least five minutes before operating the system.

Operating	−5°C to 60°C (41°F to 140°F)

When the system is operating at the maximum temperature, airflow must maintain the inlet-to-outlet air temperature rise across the system module at not more than 5°C (9°F). Derate the maximum operating temperature by 0.56°C (1°F) for each 305 m (1,000 ft) of altitude above 2,440 m (8,000 ft).

3.6.3.2 Relative Humidity

Storage	5% to 95%, noncondensing
Operating	5% to 95%, noncondensing

3.6.3.3 Altitude

Storage	15.24 km (50,000 ft), 90 mm mercury maximum

The module is not mechanically or electrically damaged at altitudes up to 15.24 km (50,000 ft).

Operating	2,440 m (8,000 ft)

The maximum operating temperature must be derated at high altitudes (Paragraph 3.6.3.1).

CHAPTER 4
WINCHESTER HARD DISK CONTROLLER

4.1 INTRODUCTION

The RCD51-BA Winchester subsystem consists of a Winchester hard disk drive and the PC1XX-DA Winchester hard disk option. The PC1XX-DA option is the control interface between the Rainbow computer and the RD51-A Winchester hard disk drive. The PC1XX-DA option consists of two field replaceable units (FRUs): the hard disk controller module (part number 54-16019), and a disk drive to controller module interconnect cable (part number 17-00427-01). Only the hard disk controller module and interconnect cable are described in detail in this chapter. A detailed description of the Winchester hard disk drive is in the documentation listed in Paragraph 4.1.2.

4.1.1 Chapter Organization

The information in this chapter is divided into six sections.

1. A general description of the functions performed by the Winchester subsystem (Paragraph 4.2)
2. A physical description of the hard disk controller module (Paragraph 4.3)
3. A functional description of the hard disk controller module (Paragraph 4.4)
4. Programming the hard disk controller registers (Paragraph 4.5)
5. A description of the signals on the interface connectors (Paragraph 4.6)
6. Winchester subsystem specifications (Paragraph 4.7)

4.1.2 Reference Documentation

Additional documentation containing information pertaining to the Winchester subsystem is available from Digital as well as other sources.

Digital Documentation

Title	Digital Part Number
Rainbow™ Winchester Disk Option Installation Guide	EK-RBWIN-IN*
Rainbow™ 100 Winchester Disk Option Upgrade and Installation Guide	EK-PCWIN-IN†
RD51 Controller Circuit Schematics	CS-5416019-0-1
RD51 Controller Unit Assembly Drawing	UA-5416091-0-0

*Rainbow PC100-B and 100+ only
†Rainbow PC100-A only

Other Documentation

Title	Source
ST406/412 Microwinchester Service Manual	Seagate Technology 920 Disk Drive Scotts Valley, CA 95066
WD1010 Winchester Disk Controller Specification	Western Digital Corp. 2445 McCabe Way Irvine, CA 92714

4.2 GENERAL DESCRIPTION

The Winchester subsystem for the Rainbow computer expands the on-line storage capacity of the system by 10 Mbytes of data. Data is passed between the system bus and the hard disk drive through a 512 byte sector buffer on the hard disk drive controller module. The data transfer rate is 5 Mbits/s from the drive and as fast as the 8088 processor can empty the sector buffer on the system side.

The hard disk controller module plugs into two 40-pin connectors on the system module. It uses the same system module connectors as the extended communications option, so only one of these options can be used in the Rainbow computer at one time. A 34 conductor shielded twisted molded cable that has one connector on one end and two connectors on the opposite end, connects the hard disk to the hard disk controller module. Figure 4-1 shows the connector and cable connections for the Winchester subsystem.

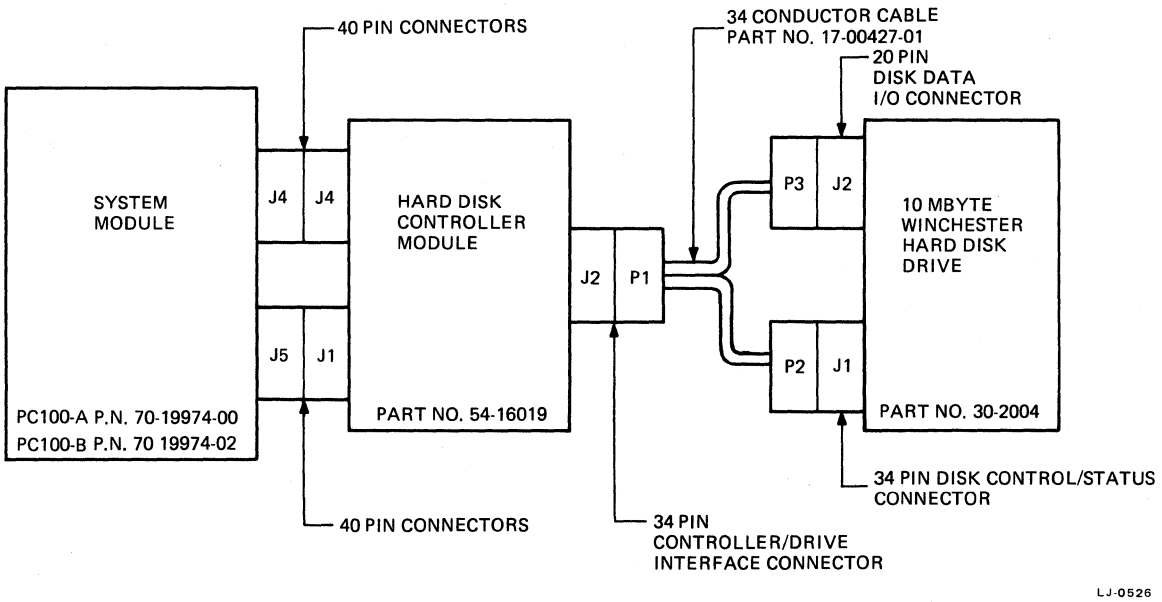

Figure 4-1 Winchester Subsystem Connections

4.3 PHYSICAL DESCRIPTION

The controller module is a 9.90 cm (3.9 in) wide × 32.51 cm (12.8 in) long multilayer printed circuit module which contains two 40-pin connectors (J1, J4) located on the component side and a 34-pin connector located on the solder side of the module. The two 40-pin connectors provide the controller module interface to the system module 8088 control, address, and data buses. The 34-pin connector provides the interface to the hard disk drive through an interconnect cable.

The controller module also contains three jumper clips (W1, W2, and W3), one 24-pin, and one 40-pin IC socket. The 24-pin socket holds a 2K × 8 bit RAM chip (sector buffer) and the 40-pin socket holds the WD1010 Winchester disk controller chip. These two ICs are the only IC components that are not soldered to the printed circuit module. Figure 4-2 shows the location of the connectors, removable ICs, and the jumpers on the controller module.

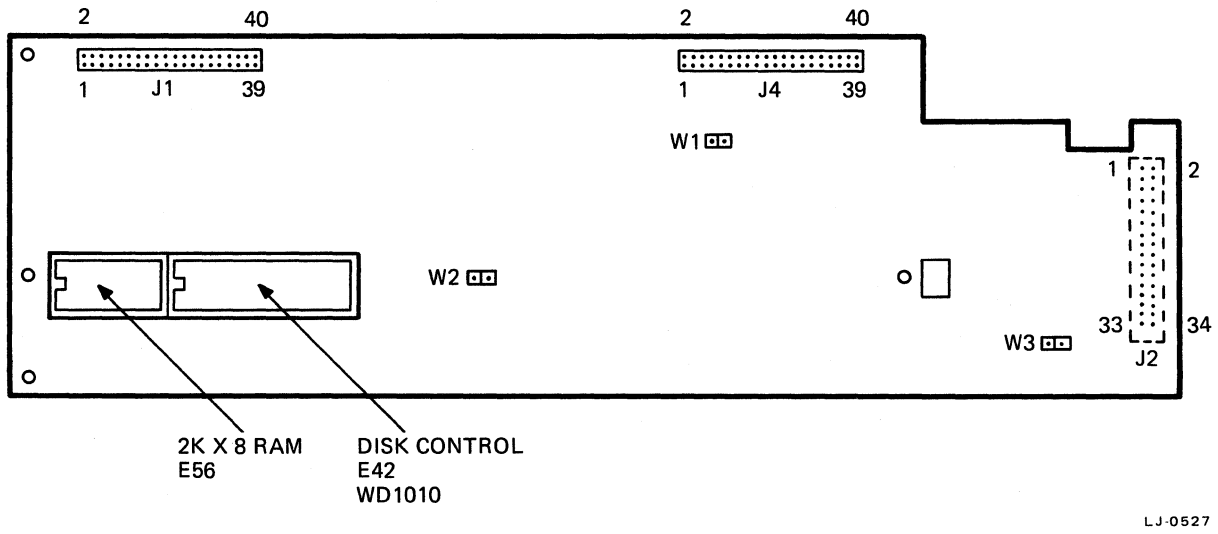

Figure 4-2 RD51 Controller Module Physical Layout

The controller module to hard disk drive interconnect cable is a 60.96 cm (24 in) molded assembly containing 30 twisted-pair conductors and terminated by 3 molded conductors and 2 ground drains.

The polyvinyl cloride (PVC) covered cable assembly comprises a shielded 4 conductor cable and a shielded 26 conductor cable. The 4 conductor cable is 45.72 cm (18 in) long, .635 cm (.250 in) in diameter, and terminates at the 20-pin disk I/O data connector P3. The 26 conductor cable is 53.34 cm (21 in) long, .889 cm (.35 in) in diameter, and terminates at the 34-pin disk control/status connector P2.

Two right angle fasteners terminate the cable shield through wire braid to the Rainbow computer chassis. One fastener is connected directly at connector P1 and the other is located 35.56 cm (14 in) from P1 in a 3.175 cm (1.25 in) molded terminator.

Figure 4-3 shows the interconnect cable. Table 4-1 describes the connector pin wiring.

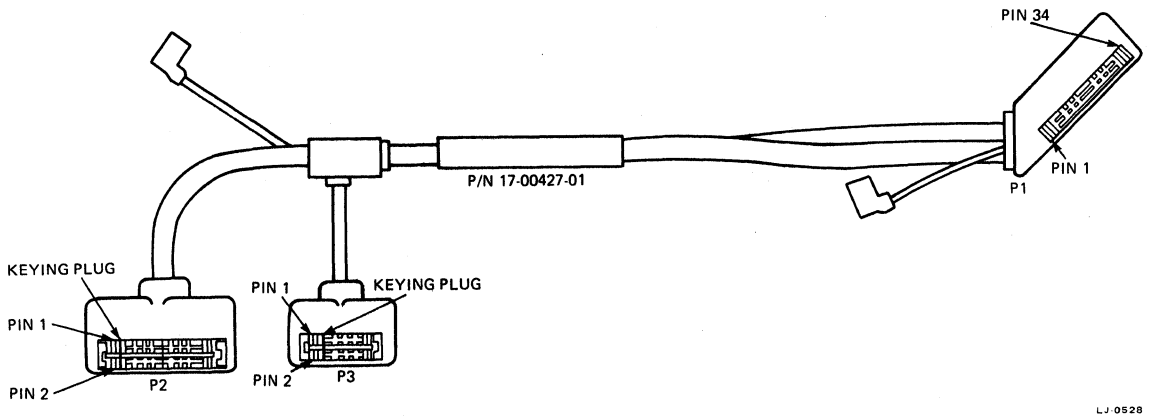

Figure 4-3 Controller/Hard Disk Interconnect Cable

Table 4-1 Interconnect Cable Wiring

From Connector*	Signal name	Mnemonic	To Connector†
P1-1	Reduced Write Current	RWC L	P2-2
P1-2	Ground	GND	P2-1
P1-3	Head Select 2	HD SEL 2 L	P2-4
P1-4	Ground	GND	P2-3
P1-5	Write Gate	WR GATE L	P2-6
P1-6	Ground	GND	P2-5
P1-7	Seek Complete	SEEK COMPLETE L	P2-8
P1-8	Ground	GND	P2-7
P1-9	Track 000	TK 000 L	P2-10
P1-10	Ground	GND	P2-9
P1-11	Write Fault	WRITE FAULT L	P2-12
P1-12	Ground	GND	P2-11
P1-13	Head Select 0	HD SEL 0 L	P2-14
P1-14	Ground	GND	P2-13
P1-15	Direction In	DIR L	P2-34
P1-16	Ground	GND	P2-33
P1-17	Head Select 1	HD SEL 1 L	P2-18
P1-18	Ground	GND	P2-17
P1-19	Index Pulse	INDEX L	P2-20
P1-20	Ground	GND	P2-19
P1-21	Ready	READY L	P2-22
P1-22	Ground	GND	P2-21
P1-23	Step Pulse	STEP L	P2-24
P1-24	Ground	GND	P2-23
P1-25	Drive Select 0	DRV SEL 0 L	P2-26
P1-26	Ground	GND	P2-25
P1-27	−MFM Write Data 0	MFM WRITE DATA 0 L	P3-14
P1-28	+MFM Write Data 0	MFM WRITE DATA 0 H	P3-13
P1-29	−MFM Read Data 0	MFM READ DATA 0 L	P3-18
P1-30	+MFM Read Data 0	MFM READ DATA 0 H	P3-17

* The following wires on connector P1 are twisted pairs; 1 and 2, 3 and 4, 5 and 6, 7 and 8, 9 and 10, 11 and 12, 13 and 14, 15 and 16, 17 and 18, 19 and 20, 21 and 22, 23 and 24, 25 and 26, 27 and 28, 29 and 30. There are no wires on pins 31–34.

† There are no wires on pins 15 and 16, 27–32 of P2 and no wires on pins 1–12, 15, 16, and 19 and 20 of P3.

4.4 FUNCTIONAL DESCRIPTION

The hard disk controller module provides the link between the 8088 processor on the system module and the Winchester hard disk drive. A Western Digital WD1010 Winchester disk controller chip is the center of the controller module design and it is compatible with the Seagate ST506 data and control interface of the RD51-A hard disk drive. Data is transferred between the main memory on the system module and the disk surface through a 512 byte sector buffer on the hard disk controller module. The data is transferred in two steps.

1. Main memory to/from the sector buffer by 8088 controlled program transfer
2. Sector buffer to/from the disk surface under WD1010 control

The controller module contains ten 8-bit registers which the 8088 processor accesses to write data to, read data from, and monitor the status of the disk drive. Seven of these registers are internal registers of the WD1010 controller chip and the remaining three registers are located on the controller module.

Figure 4-4 shows the controller chip and its relation to the supporting logic on the controller module.

4.4.1 WD1010 Winchester Disk Controller

The WD1010 controller chip is a 40-pin MOS/LSI device which performs the functions of a Winchester disk controller/formatter. The WD1010 chip contains seven registers for communicating with the BAD<7:0> bus on the PC100-A or PC100-B system module. All communications between the WD1010 chip and the 8088 processor are via these registers.

The WD1010 chip has the following features.

- 5 Mbits/s data rate
- Automatic retries (eight)
- Implied seeks
- Unlimited sector interleave
- Cyclic redundancy check (CRC)
- Variable sector size

Table 4-2 describes the WD1010 input and output signals.

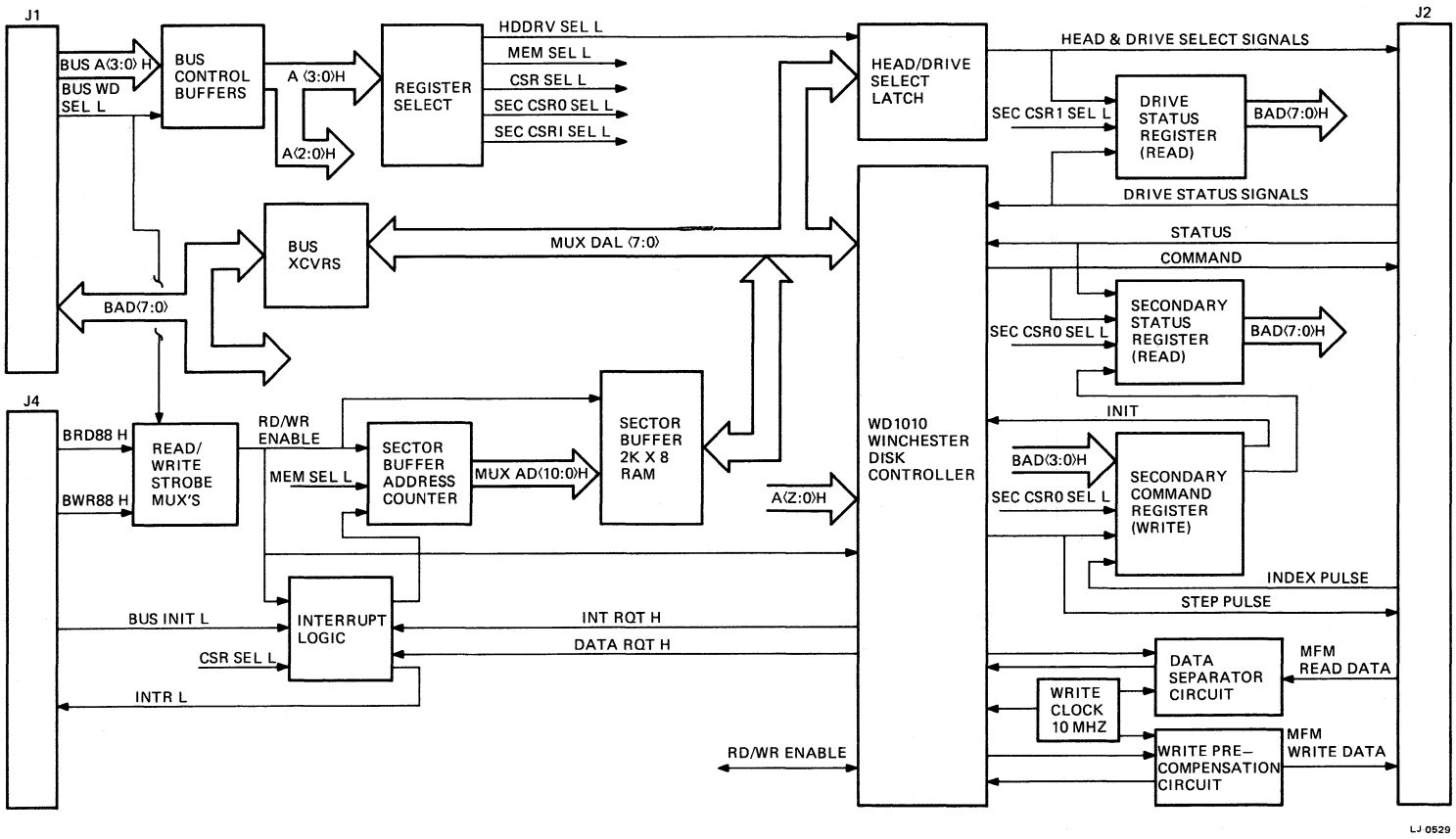

Figure 4-4 Hard Disk Controller Module

Table 4-2 WD1010 Controller Pin Description

Pin Number	Mnemonic	WD1010 Pin Symbol	Direction*	Signal Name and Function
1	BUSY L	-BCS	O	BUSY – This signal is asserted low to enable reading from or writing to the sector buffer.
2	BUF CNTR RST L	-BCR	O	BUFFER COUNTER RESET – This signal is asserted low prior to read/write operations. It is strobed whenever BUSY changes state.
3	INT RQT H	IRQ	O	INTERRUPT REQUEST – This active high signal interrupts the 8088 processor whenever the WD1010 chip has completed execution of any command.
4		NC		No Connection
5	INIT L	-MR	I	INITIALIZE – This input signal from the system module initializes all internal logic when the system is powered on or reset.
6	RE L	-RE	I/O	READ ENABLE – This three state bidirectional signal acts as an input when the 8088 processor is reading the task register and as an output when the WD1010 chip is reading the sector buffer.
7	WE L	-WE	I/O	WRITE ENABLE – This three state bidirectional signal acts as an input when the 8088 processor is writing into the task register and as an output when the WD1010 chip is writing to the sector buffer.
8	WD1010 SEL L	-CS	I	WD1010 SELECT – This signal input from the 8088 I/O decoders enables both the READ ENABLE and WRITE ENABLE signals.
9,10,11	A0H–A2H	A0–A2	I	ADDRESS BITS 1,2, and 3 – These three address bits from the 8088 processor select the register to transmit/receive on the MUX DAL 7-0 bus.

*I = Input, O = Output, I/O = Input/Output

Table 4-2 WD1010 Controller Pin Description (Cont)

Pin Number	Mnemonic	WD1010 Pin Symbol	Direction*	Signal Name and Function
12–19	MUX DAL7 H – MUX DAL 0 H	D7–D0	I/O	MULTIPLEXED DATA BITS 7–0 – This eight bit three state bidirectional bus transfers commands, status, and data among the WD1010 chip, the sector buffer, and the 8088 data bus.
20	GROUND	VSS	I	GROUND
21	WR DATA H	WD	O	WRITE DATA – This signal contains the MFM clock and data pulses that are sent through the write precompensation circuit and then recorded as flux transitions (written) on the disk surface.
22,23	LATE L, EARLY L	-LATE, -EARLY	O	LATE, EARLY PRECOMPENSATION – These two signals are used to tell the precompensation circuit how much delay is required on the write data about to be written on the disk.
24	WR GATE H	WG	O	WRITE GATE – This signal is asserted high before writing is to be performed on the disk.
25	WR CLK H	WC	I	WRITE CLOCK – These 5 MHz clock pulses are used for all internal write timing and to encode the write data in an MFM format.
26	DIR H	DIR	O	DIRECTION – This signal defines the direction of motion of the read/write heads when the STEP line is pulsed. High = heads will move away from center of disk. Low = heads will move towards center of disk.
27	STEP H	STP	O	STEP PULSE – This signal when pulsed high causes the read/write heads to move in the direction defined by the DIRECTION signal.
28	DRV RDY H	RDY	I	DRIVE READY – This signal when high together with SEEK COMPLETE, indicates that the drive is ready to read, write, or seek.

*I = Input, O = Output, I/O = Input/Output

Table 4-2 WD1010 Controller Pin Description (Cont)

Pin Number	Mnemonic	WD1010 Pin Symbol	Direction*	Signal Name and Function
29	INDEX H	IND	I	INDEX PULSE – Once each revolution (16.67 ms nominal), the hard disk drive provides the pulse to indicate the beginning of a track.
30	WRT FAULT H	WF	I	WRITE FAULT – This signal indicates a condition exists at the drive which may cause improper writing on the disk. When this signal is high, further writing is inhibited at the drive until the condition is corrected.
31	TK 000 H	TK0	I	TRACK ZERO – This signal indicates that the read/write heads are positioned at cylinder zero (the outermost data track).
32	SEEK COMPLETE H	SC	I	SEEK COMPLETE – When high, this signal indicates that the read/write heads have settled on the final track at the end of a seek.
33	RED WRT CUR H	RWC	O	REDUCED WRITE CURRENT – This signal goes to the disk drive and when high together with WRITE GATE, causes the disk drive to use a lower value of write current for writing on the disk. When this signal is low, the disk drive uses a higher value of write current. The RD51 disk drive has the ability to internally select a high or low value of write current.
34	WD DRUN H	DRUN	I	DATA RUN – The WD1010 chip uses this signal from the data separator circuit during a read command to assert a read gate (RD GATE H) when a sync mark (A1 Hexadecimal) is detected. When the read gate is asserted, the data separator is locked on the incoming data stream. A field of 13 bytes of zeros precedes the synchronous mark (A1 Hexadecimal).

*I = Input, O = Output, I/O = Input/Output

Table 4-2 WD1010 Controller Pin Description (Cont)

Pin Number	Mnemonic	WD1010 Pin Symbol	Direction*	Signal Name and Function
35	BUF RDY H	BR	I	BUFFER READY – This signal is bit 0 of the secondary command (write) register. Setting this bit to 1 informs the WD1010 controller chip that the sector buffer is full or empty. On a read sector command, it informs the WD1010 controller chip that the sector buffer is empty and the command is terminated. On a write sector command or format command, it informs the WD1010 controller chip that the sector buffer now contains valid data for the requested operation.
36	DATA RQT H	DRQ	O	DATA REQUEST – When high, this signal initiates data transfers to/from the sector buffer. On a read command, this signal goes high after the sector buffer is filled. On a write or format command, this signal goes high when the WD1010 chip is ready to access the information in the sector buffer.
37	WD RD H	RD	I	READ DATA – This is the data input from the disk drive after it is processed by the data separator circuit. This signal contains the resynchronized data pulses.
38	RD GATE H	RG	O	READ GATE – The WD1010 chip asserts this signal high to enable the data separator circuit when reading data from the disk drive.
39	READ CLK H	RC	I	READ CLOCK – This signal is a nominal square wave input derived from the voltage controlled oscillator (VCO) in the data separator circuit. The WD1010 controller chip uses it to decode the MFM data from the disk drive.
40	+5 V	VSS	I	+5 V INPUT

*I = Input, O = Output, I/O = Input/Output

4.4.2 System Module/Controller Module Interface

The primary interface between the 8088 processor and the WD1010 is through the BAD<7:0> bus. This bus transmits/receives data to/from both the WD1010 controller chip and a sector buffer through bus transceivers over the MUX DAL<7:0> bus. The bus transceivers are necessary to isolate the system module bus BAD<7:0> from the MUX DAL<7:0> bus during the time the WD1010 chip is accessing the sector buffer.

The sector buffer is composed of a 2K × 8 bit static RAM and an eleven bit address counter. The sector buffer gives the controller module the capability to store and retrieve data blocks of up to 1,024 bytes. Whenever the WD1010 chip is not using the sector buffer, the BUSY L signal is high (disabled). This allows the 8088 processor to access the registers of the WD1010 chip by placing an I/O address (60H–69H) on address bus A<7:0>H. The three least significant bits A<2:0>H of the address are decoded to select none or any one of seven internal registers of the WD1010 chip.

When address bits A<2:0>H are equal to 000, and the BUSY L signal is high (disabled), the MUX DAL<7:0>H pins of the WD1010 are three stated to isolate the WD1010 controller chip from the MUX DAL<7:0> bus. This allows the 8088 processor to access the WD1010 controller chip's task file to set parameters prior to issuing commands or to access sequential bytes within the sector buffer RAM.

When address bits A<2:0>H do not equal 000, the 8088 processor can access any one of the seven registers of the WD1010 controller chip but cannot access the sector buffer RAM because it is three stated at this time.

During write sector commands, the 8088 processor sets up data in the task file registers and issues the command. The WD1010 chip controller strobes the buffer counter reset (BUF CNTR RST L) signal to reset the sector buffer address counter to zero. Then the WD1010 controller chip generates a data request signal to inform the 8088 that it may load the sector buffer with the data to be written. When the address counter reaches a count of 512, a buffer ready (BUF RDY H) signal is generated to inform the WD1010 chip that the sector buffer is full. The WD1010 chip then asserts BUSY L, which prevents the read/write enable (BRD88 H and BWR88 H) signals from the 8088 processor from passing through the read/write strobe multiplexers and allows the RE L and WE L pins of the WD1010 chip to enable the sector buffer. When the WD1010 chip finishes using the sector buffer, it disables BUSY L and resets the address counter to again allow the 8088 processor to access the WD1010 chip and the sector buffer RAM.

The read sector commands operate in a similar manner, except the sector buffer is loaded by the WD1010 chip instead of the 8088 processor.

Other WD1010 control signals called interrupt request (INT RQT H) and data request (DATA RQT H) interrupt the 8088 processor when the WD1010 chip has completed executing a command and when the WD1010 chip is requesting data. In a read command, interrupts are generated at the termination of a command; an interrupt may be specified to occur either at the end of a command or when DATA RQT H is activated. DATA RQT H, once activated, will remain high until BUF RDY H is sensed, indicating the data transfer is completed. Either reading the status register or writing a new command in the command register clears the interrupt line (INT RQT H).

4.4.3 Controller Module/Disk Drive Interface

The WD1010 chip interfaces to the hard disk drive through buffer/receivers, a data separator circuit, a write precompensation circuit, and secondary command/status registers. The buffer/receivers condition the control lines to be driven through the interconnect cable to the disk drive. The control lines are single-ended, resistor terminated TTL levels. The data lines (MFM WRITE DATA and MFM READ DATA) to and from the drive also require buffering but are differential RS-422 levels.

4.4.3.1 Data Separator Circuit – The data separator circuit synchronizes the READ CLK H input to the WD1010 chip with the raw MFM data coming from the disk drive. The data separator circuit comprises a phase lock loop (PLL) data separator and associated components. The WD1010 chip interacts with the data separator through the data run (WD DRUN H) and read gate (RD GATE H) signals.

The data separator circuit processes MFM read data from the disk drive and applies it to the read data (WD RD H) input of the WD1010 chip. When the WD1010 chip is not inspecting data, its read gate (RD GATE H) is asserted low to disable the data separator circuit. When the data separator circuit is disabled, the phase lock loop is locked to a 5 MHz reference clock that is derived from the 10 MHz write clock.

When any read/write command is initiated and a search for address mark begins, the WD1010 chip examines the WD DRUN H input from the data separator circuit. The WD DRUN signal retriggers constantly on a field of ones and zeros. A counter in the data separator circuit times out to see if WD DRUN is high for 16 bits (2 byte times). Since 12 bytes of zeros precede all address marks, an attempt is made to read an address mark. If WD DRUN signal goes low prior to 64 bit times, the process is repeated. The WD1010 chip asserts the RD GATE H, switching the data separator to lock on to the incoming MFM data stream. READ GATE H will remain active high until a nonzero, nonaddress mark byte is detected. It then will lower READ GATE H for 2 byte times (to allow the PLL to lock back on the 5 MHz reference clock) and start the WD DRUN H search over again. If an address mark is detected, READ GATE H will be high and the command continues searching for the proper ID field.

4.4.3.2 Write Precompensation Circuit – Data from the WD1010 chip is written on the hard disk surface using the modified frequency modulation (MFM) method. This recording method produces an undesirable shifting of the peaks of adjacent flux transitions on the disk surface. They are moved from the write position. The write precompensation circuit shifts the data to be written in a direction opposite to the expected peak shift of the read data as a result of the MFM encoding.

The reduced write current (RED WRT CUR H), early (EARLY L), late (LATE L), and write gate (WR GATE H) signals from the WD1010 chip control the write precompensation circuit. The value loaded into the write precompensation cylinder register in the WD1010 chip controls the disk cylinder in which the reduced write current becomes active. When the RED WRT CUR H signal goes high, the write circuits in the disk drive will reduce the write current to the write head approximately 10 percent peak to peak.

The signals early and late tell the write precompensation circuit how much delay is required on the write data pulse to be sent. A tapped delay line provides the early and late signals selecting a delay value which determines the amount of precompensation delay. The delay line provides a write precompensation value of ±15 ns for cylinders at or greater than the cylinder number loaded into the write precompensation cylinder register. Since the signal early occurs after the fact, write data is delayed one interval (15 ns) when both early and late are low; two intervals (30 ns) when late is high; and no delay (0 ns) when early is high. Early and late will be active slightly ahead of the write data pulse; they will never be high at the same time, but they will be active regardless of the contents of the write precompensation cylinder register.

The WD1010 chip asserts high the WR GATE H signal before the writing on the disk. This signal enables both the write precompensation circuit and the write current source in the disk drive.

4.4.3.3 Head/Drive Select Circuit – The head/drive select circuit performs two functions; it provides a drive select signal to enable the disk drive for reading or writing and a three bit binary head address to select one of four read/write heads in the selected drive. The head/drive select signals are sent to the drive through connector J2 and to the drive status register.

Address bits BUS A<3:0>H from the 8088 processor and the WD SEL L signal from the 8088 I/O decoders produce a head/drive select (HDDRV SEL L) signal to enable a head/drive select latch. The multiplexed data address lines (MUX DAL<3:0>) specify the binary head address and the enabling signal for the selected drive. The BWR88 signal from the 8088 processor clocks these signals into the head/drive select latch.

4.4.3.4 Secondary Command/Status Registers – The secondary command/status registers are 8-bit registers that hold control and status information to/from the WD1010 chip and the disk drive. The 8088 processor accesses both registers through the register select circuit on the controller module. The register select circuit decodes I/O address 68H from the BUS A<3:0>A bits from the 8088 processor and the WD SEL L signal from the 8088 I/O decoders to generate the secondary control status register 0 select (SEC CSR0 SEL L) signal to provide one of the enable signals for the secondary command/status register.

The secondary command register is a write-only register that holds control signals going to the WD1010 chip and drive status signals for the secondary status register. The inputs for this register come from the BAD<3:0>H bits, the WD1010 chip, and the disk drive. The SEC CSR0 SEL L signal ANDed with the BWR88H signal from the 8088 processor enable this register.

The secondary status register is a read-only register that holds the status of signals coming from the WD1010 chip and status signals from the disk drive. The CSR0 SEL L signal ANDed with the BRD88 H signal from the 8088 processor enable this register. The contents of this register are sent to the 8088 processor over the BAD<7:0> bus.

4.4.3.5 Drive Status Register – This status register is an 8-bit read-only register that reflects the status of the disk drive. The inputs for this register come from the head/drive select circuit, the WD1010 chip, and the disk drive. The register contents are gated out to the 8088 processor over the BAD<7:0> bus.

The 8088 processor accesses the register through the register select circuit. This circuit decodes I/O address 69H from the BUS A<3:0>H bits from the 8088 processor and the WD SEL L signal from the 8088 I/O decoders to generate the secondary control status register 1 select (SEL CSR 1 SEL L) signal. This signal in conjunction with BRD88 H form the 8088 processor gates out the register contents.

4.5 PROGRAMMING REGISTERS

The hard disk subsystem stores and retrieves data blocks to/from the system module memory and the hard disk drive by communicating with the system module bus through 8-bit registers. Data blocks of 128 bytes to 1024 bytes can be stored or retrieved depending on the track format used. The following paragraphs describe the registers and the general sequence of operations for the subsystem.

4.5.1 Registers

The hard disk controller module contains ten 8-bit registers for communicating with the Rainbow computer bus. Seven registers are internal registers of the WD1010 controller chip and the remaining three are located on the controller module.

All communications between the controller module and the system module are via these registers.

The 8088 processor on the system module asserts an I/O bus address in the 60H–69H range to access these registers. The four most significant bits of the address define the I/O page reserved for the extended communications option and the four least significant bits define the registers on the controller module. All addresses not defined are reserved. Table 4-3 describes the ten valid registers.

All the registers are available to the 8088 processor except when the subsytem is executing a function; Busy (bit 7) is set in the status register, or Controller Busy (bit 0) is set in the secondary status register.

Table 4-3 Hard Disk Controller Module Registers

I/O Bus Address	Register Name	Type*	Location WD1010	Cont. Module
60H	Data Buffer	R/W		X
61H	Error/Precomp	R-Error/W-Precomp	X	
62H	Sector Count	R/W	X	
63H	Sector Number	R/W	X	
64H	Cylinder Low	R/W	X	
65H	Cylinder High	R/W	X	
66H	SDH Byte	R/W	X	
67H	Status/Command	R-Status/W-Command	X	
68H	Secondary Status/Command	R-Sec Status/W-Sec Command		X
69H	Drive Status	R		X

* R/W = READ/WRITE, R=READ ONLY, W = WRITE ONLY

NOTE

Accessing any register other than the secondary status register when the Controller Busy bit is set is not allowed. The controller ignores such accesses and does not acknowledge them.

4.5.1.1 Data Buffer Register (60H) – The data buffer register is a read/write register that the 8088 processor stores data in or removes data from the sector buffer RAM. When the 8088 processor reads/writes to I/O address 60H, the data pins of the WD1010 chip are three stated to isolate it from the sector buffer. Figure 4-5 shows the data buffer register bit format.

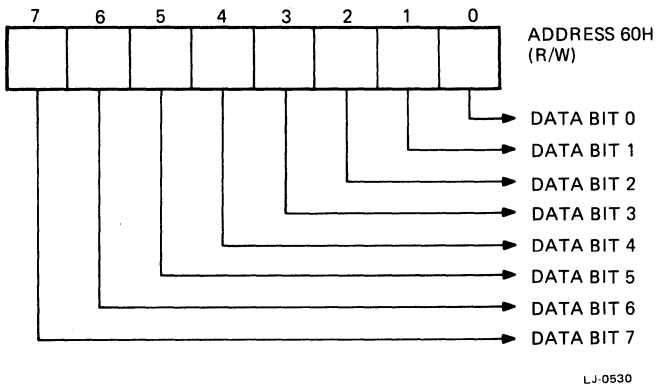

Figure 4-5 Data Buffer Register Format

4.5.1.2 Error/Precompensation Register (61H) – The error/precompensation register at I/O address 61H, when the 8088 processor reads it, contains drive and data error status bits after the completion of a command. The error register bit format is shown in Figure 4-6 and the bits are defined in Table 4-4.

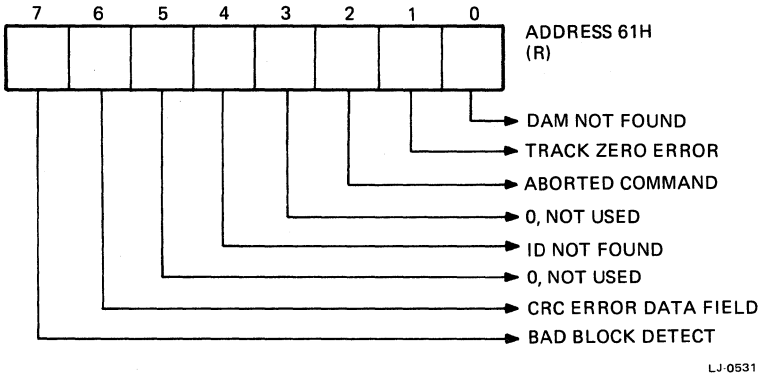

Figure 4-6 Error Register Format

The write precompensation register at I/O address 61H, when written to, contains the disk drive cylinder number where the WD1010 chip asserts the reduced write current (RED WRT CUR H) signal. The value (0–255) loaded into this register is internally multiplied by four to specify the actual cylinder where write precompensation begins. For example, a value of 01H causes reduced write current to begin on cylinder 4. Precompensation for the RD51 drive is recommended on cylinder 128 and above. Therefore, the decimal value 32(20H) must be loaded into the write precompensation register. Figure 4-7 shows the bit format for the write precompensation register.

Table 4-4 Error Register Bit Description

Bit Number	Name	Description
0	DAM NOT FOUND	This error indicates that the desired sector header was found but the data address mark (DAM) for the data field was not found.
1	TRACK ZERO ERROR	Only the restore command sets this error. It indicates that track zero line from the drive is not active after the controller issued 1024 step pulses.
2	ABORTED COMMAND	This bit is set if a command is issued while the drive ready (DRV RDY H) signal is low or the write fault (WRT FAULT H) signal is low. This bit also will be set if seek complete (SEEK COMPLETE H) does not go high within eight index pulses.
3	RESERVED	This bit is forced to zero because it is not used.
4	ID NOT FOUND	This bit is set if the desired header cannot be found.
5	RESERVED	This bit is forced to zero because it is not used.
6	CRC DATA FIELD	This bit is set if the desired sector is found but the data field does not equal zero.
7	BAD BLOCK DETECT	This bit is set if an attempt is made to access a sector with the bad block bit set in the ID header. It is used for mapping bad sectors.

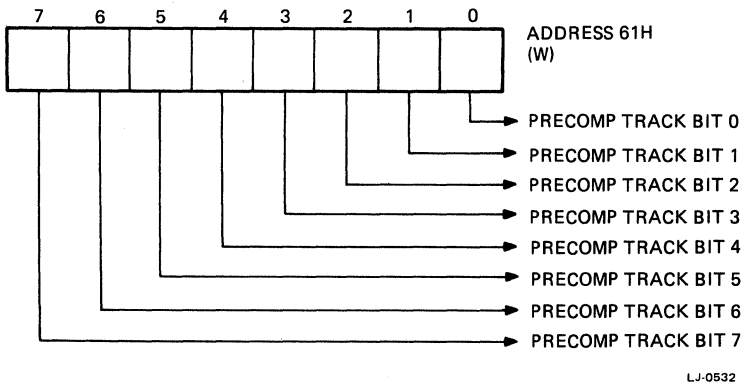

Figure 4-7 Write Precompensation Register Format

4.5.1.3 Sector Count Register (62H) – The sector count register is a read/write register at I/O address 62H. It is used when doing multiple sector reads or writes and during the format command.

During multiple sector reads or writes, this register indicates the number of sectors to transfer. The head or cylinder number is not incremented in multiple sector accesses. Therefore, if a multiple sector request is issued that exceeds the boundary of the current track, an ID not found will be returned for the remaining sectors. A value of zero in this register during a multiple sector access, represents a 256-sector request. During a format command, this register indicates the number of sectors per track. On the RD51 this is currently 16. Figure 4-8 shows the bit format for the sector count/register.

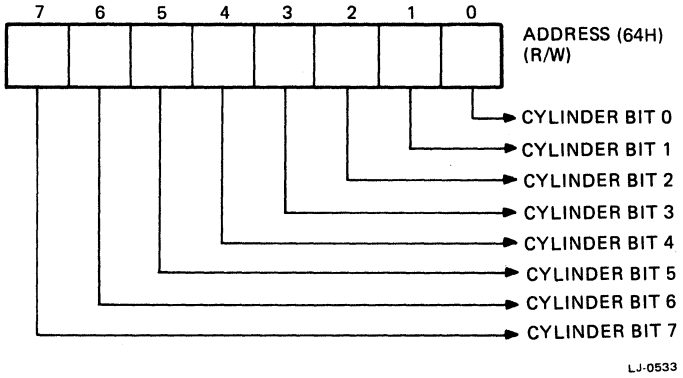

Figure 4-8 Sector Count Register Format

4.5.1.4 Sector Number Register (63H) – The sector number register is a read/write register at I/O address 63H. This register holds the desired sector number when doing single sector accesses. During a multiple sector command, this register specifies the first sector in the transfer. It is internally incremented after each transfer of data to the sector buffer. Figure 4-9 shows the sector numbers register bit format.

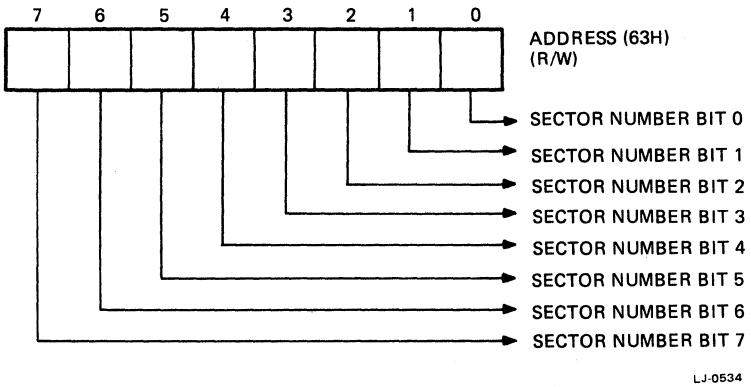

Figure 4-9 Sector Number Register Format

4.5.1.5 Cylinder Low Register (64H) – The cylinder low register is a read/write register at I/O address 64H. Its contents specify the lower byte of the desired cylinder number. In conjunction with the cylinder number high register contents it specifies a cylinder from 0–1023. The RD51 drive contains 306 cylinders. Figure 4-10 shows the cylinder low register bit format.

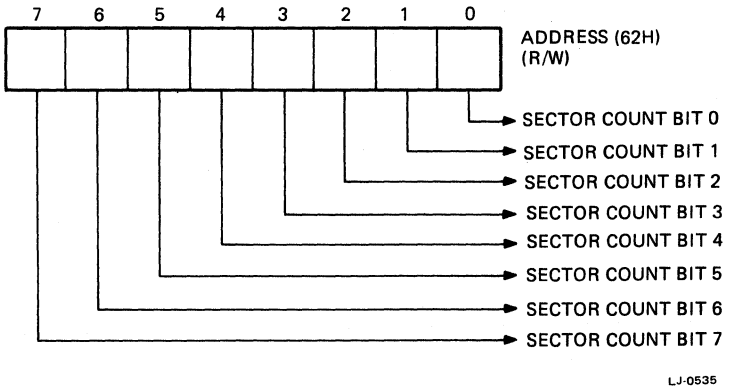

Figure 4-10 Cylinder Low Register Format

4.5.1.6 Cylinder High Register (65H) – The cylinder high register is a read/write register at I/O address 65H. The register contents specify the two most significant bits of the desired cylinder number. Figure 4-11 shows the cylinder high register bit format.

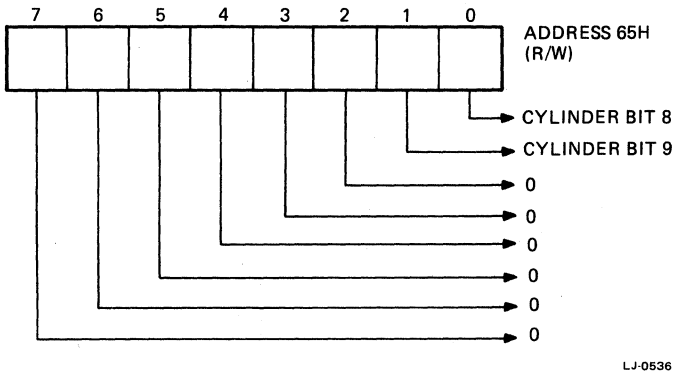

Figure 4-11 Cylinder High Register Format

4.5.1.7 SDH Byte Register (66H) – The SDH byte register is a read/write register at I/O address 66H. The register contents specify the desired sector size, drive number, and head number parameters. Both the head number and sector size number are compared against the disk's ID field. The drive number and head number are decoded to provide drive select and head select signals for the disk drive. The SDH byte register format is shown in Figure 4-12 and the bits are defined in Table 4-5.

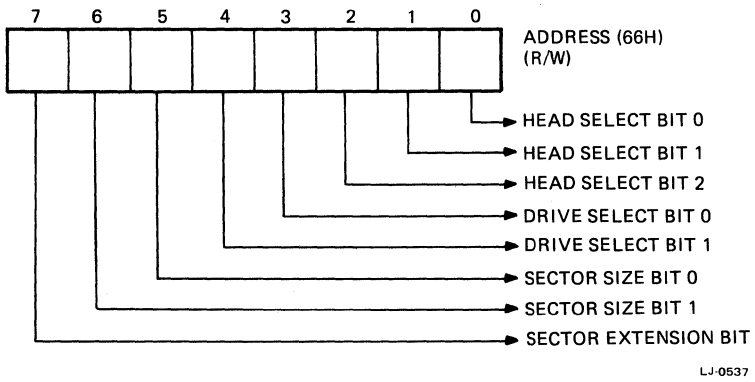

Figure 4-12 SDH Byte Register Format

Table 4-5 SDH Byte Register Bit Description

Bit Number	Name	Description
0–2	Head Select	These bits select the desired head. The controller will accommodate drives with up to 8 heads. The RD51 drive has only 4 heads. Attempting to access heads 4–7 results in an ID-not-found error.
3–4	Drive Select	The WD1010 chip includes support for multiple drives. The RD51 controller only supports a single drive. The drive number must always be 0.
5–6	Sector Size	The controller is capable of supporting 4 different sector sizes. On the RD51, the bad block cylinder will be formatted in 256K byte sectors. The remainder of the disk will be 512 byte sectors. Bit 6 / Bit 5 / Bytes/Sector 0 / 0 / 256 0 / 1 / 512 1 / 0 / 1024 1 / 1 / 128
7	Sector Extension	Setting this bit disables CRC checking and generation. Instead of adding the CRC to the data field, the controller instead reads or writes an additional 7 bytes to or from the sector buffer. If this bit is set, the controller module will not perform any CRC data checking.

4.5.1.8 Command/Status Register (67H) – The command/status register at I/O address 67H is a write-only register for commands and a read-only register for status signals.

The command register is loaded with one of six commands. The command begins to execute immediately upon loading. Do not load this register while the Busy (bit 7) or Command in Progress (bit 1) bits are set in the status register. If the WD1010 chip has asserted its interrupt request pin, a write to the command register will clear it.

The WD1010 chip executes six commands.

1. Restore – Restores the read/write heads to track zero, usually on a power-up
2. Seek – Primarily overlaps seek operations on multiple drives
3. Read Sector – Transfers one or more sectors of data from the disk drive
4. Write Sector – Writes one or more sectors of data to the disk drive
5. Scan ID – Updates the head, sector size, sector number, and cylinder registers
6. Format Track – Formats one track using the task file and sector buffer

Prior to loading the command register, the 8088 processor must first set up the task file registers with the proper information needed for the command. Except for the command byte, the other registers may be loaded in any order. The WD1010 chip ignores any subsequent writes to the command register until the WD1010 controller chip completes execution of the command and resets the command in progress bit in the status register. The command register formats for the six available commands are shown in Figure 4-13 and defined in Table 4-6.

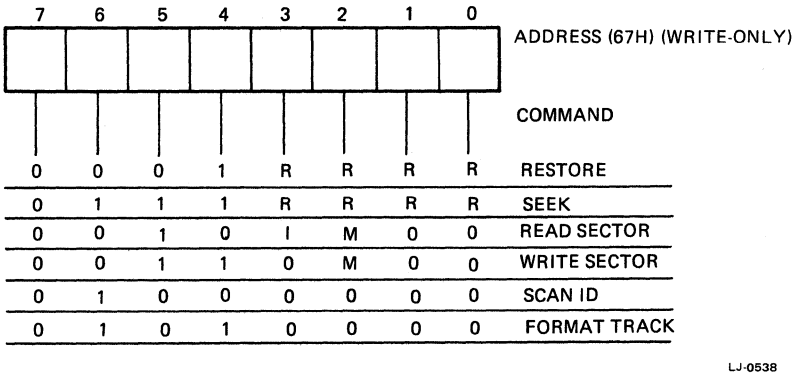

Figure 4-13 Command Register Format

Table 4-6 Command Register Bit Description

Bit Number	Name	Command	Description
0–3	Step Rate	Restore and Seek	The bits in the restore command and seek command that determine the rate at which the WD1010 chip will issue step pulses to move the read/write heads in the disk drive. The step rate field is coded as follows. Bits 3 2 1 0 Step Rate 0 0 0 0 Approximately 35 μs 0 0 0 1 .5 ms (for each increment of 1, the to step rate is increased by .5 ms) 1 1 1 1 7.5 ms The RD51 requires a .35 μs step rate for optimum performance.
2	Multiple Sector Flag	Read Sector and Write Sector	When this Mbit is set (1), the WD1010 chip will do multiple sector transfers. When this bit is 0, the WD1010 chip will do a single sector transfer.
3	Interrupt Flag	Read Sector	The WD1010 chip produces two types of interrupts. The interrupt logic on the controller module ORs these interrupts together. Clearing the I bit in the read sector command results in a single interrupt occurring at data request time. Setting the I bit results in a second interrupt when the controller has completely executed the command.
4–7			Figure 4-13 shows these four bits are programmed to select one of the six commands.

The status register is a read-only register whose contents inform the 8088 processor of certain events the WD1010 chip performs as well as reporting the status of some of the disk drive control lines. The status register format is shown in Figure 4-14 and the bits are defined in Table 4-7.

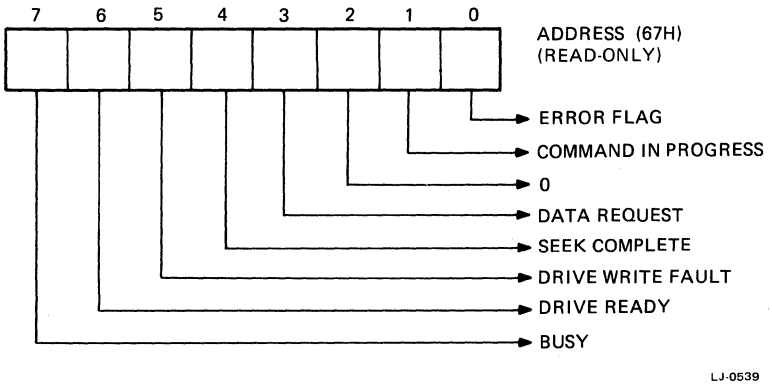

Figure 4-14 Status Register Format

4.5.1.9 Secondary Command/Status Registers (68H) – The secondary command/status registers at I/O address 68H are a write-only register for commands and a read-only register for status signals.

The secondary command register holds control signals going to the WD1010 chip and latched-status signals to/from the disk drive. The inputs for this register come from the BAD<3:0> bits, WD1010 chip, and disk drive. The register format is shown in Figure 4-15 and the bits are defined in Table 4-8.

The secondary status register holds the status of signals coming from the WD1010 chip, disk drive, and three hard-wired controller module identification bits. The status signals are gated out of the register onto the BAD<7:0> bus when the 8088 processor asserts I/O address 68H and the read strobe (BRD88 L) during an I/O read cycle.

The secondary status register format is shown in Figure 4-16 and the bits are defined in Table 4-9.

4.5.1.10 Drive Status Register (69H) – The drive status register at I/O address 69H is a read-only register that monitors the status of control and error signals to/from the disk drive. The drive status signals are gated onto the BAD<7:0> bus when the 8088 processor asserts I/O address 69H and the read strobe (BRD88 L) during an I/O read cycle.

The drive status register format is shown in Figure 4-17 and the bits are defined in Table 4-10.

Table 4-7 Status Register Bit Description

Bit Number	Name	Description
0	Error Flag	If this bit has been set, it indicates the current command has failed. The appropriate error code is in the error register. If this bit is not set but the error register is not zero, it indicates a retry was done. The code at that time in the error register was the error that caused the retry. If the error flag is set and the error code is data field CRC, the sector buffer still contains the data that was read from the disk. On a CRC error, the WD1010 chip will still wait for buffer ready before ending the command.
1	Command in Progress	This bit indicates the WD1010 chip is still processing a command or waiting for buffer ready. Do not load a new command unless this bit is cleared.
2	Reserved	This bit is forced to zero because it is not used.
3	Data Request	This bit is set after the sector buffer is filled on a read command. On a write or format command, it is set when the WD1010 chip is ready to access the information in the sector buffer. This DRQ interrupt is set anytime this bit is set. External logic disables the DRQ interrupt upon a CSR access. This bit is cleared upon receipt of buffer ready.
4	Seek Complete	This bit is a reflection of the drive seek complete line unless an error occurred. In the case of an error, this line is latched until the CSR is read.
5	Drive-Write Fault	This bit is the same as seek complete except it is a reflection of the drive-write fault line.
6	Drive Ready	This bit is the same as seek complete except it is a reflection of the drive ready line.
7	Busy	This bit is set when the WD1010 chip is accessing the disk. It is set at the beginning of all commands and is deactivated at the end of all commands except read sector. It is deactivated on a read sector command after the sector buffer is filled. Do not write commands into the controller when this bit is set.

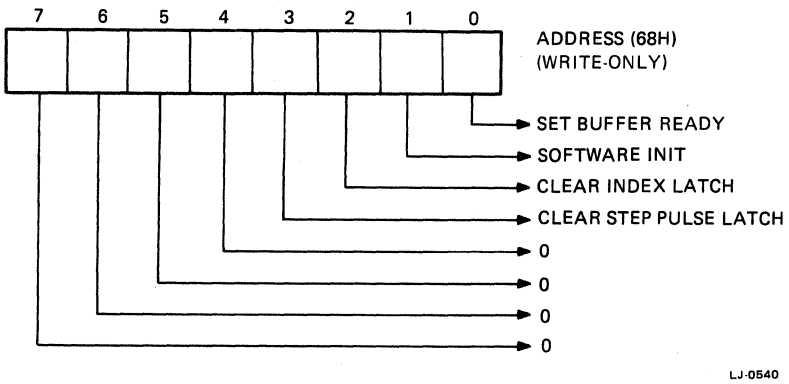

Figure 4-15 Secondary Command Register Format

Table 4-8 Secondary Command Register Bit Description

Bit Number	Name	Description
0	Set Buffer Ready	The BAD<0>H bit from the 8088 processor sets this bit. On a read sector command, this bit, when set, tells the WD1010 chip that the sector buffer was emptied which would then end the command. On a write sector or format command, this bit tells the WD1010 that the sector buffer now contains valid data for transfer to the disk drive.
1	Software Initialize	The BAD<1>H bit sets this bit. This bit, when set, initializes the controller. The controller cannot be accessed for 7 μs after the 8088 processor issues the software initialize.
2	Clear Index Latch	This bit BAD<2>H clears out the index latch. The index latch is set when the disk drive senses the index position on the disk. The index latch output is sent to the secondary status register.
3	Clear Step Latch	This bit BAD<3>H clears out the step pulse latch. The step pulse latch is set every time the WD1010 chip issues a step pulse. The output of the step pulse latch is sent to the secondary status register.
4–7	RESERVED	These bits are not used.

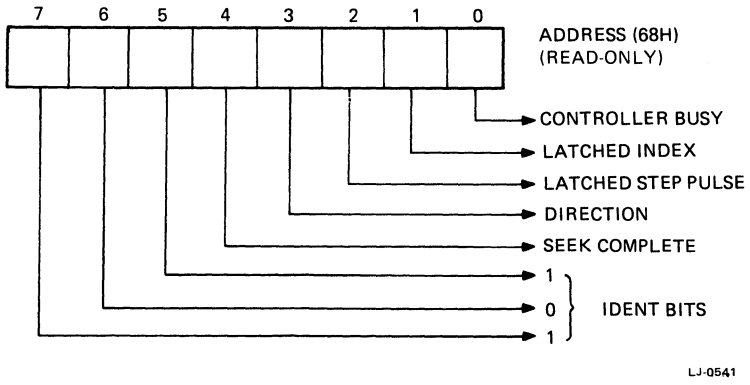

Figure 4-16 Secondary Status Register Format

Table 4-9 Secondary Status Register Bit Description

Bit Number	Name	Description
0	Controller Busy	This bit indicates that the WD1010 chip is accessing the sector buffer. When this bit is set, the 8088 processor cannot access the WD1010 registers.
1	Latched Index	This status bit from the index latch indicates if the disk drive encountered an index mark since the last time the 8088 processor cleared the index latch.
2	Latched Step Pulse	This status bit from the step pulse latch indicates if the WD1010 chip issued a step pulse since the last time the 8088 processor cleared the step pulse latch.
3	Direction	This bit indicates the direction the read/write heads in the disk drive will move when the WD1010 chip issues step pulse(s). When high (1), the R/W heads will move toward the spindle. When low (0), the heads will move away from the spindle, towards track 0.
4	Seek Complete	This status bit indicates that the disk drive positioned the R/W heads over the desired track on the disk surface.
5–7	Identification Bits	These hard wired bits inform the 8088 processor that the installed option is the RD51 controller module. Bits 5 and 6 are always high (1), and bit 6 is always low (0).

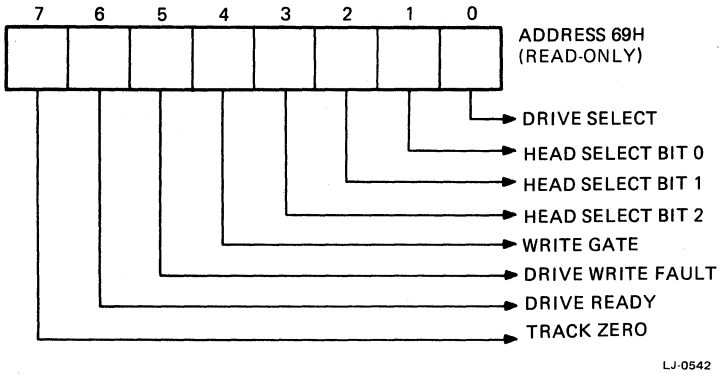

Figure 4-17 Drive Status Register Format

Table 4-10 Drive Status Register Bit Description

Bit Number	Name	Description
0	Drive Select	When this bit is high (1), it indicates that the controller module is selecting the drive.
1–3	Head Select	These three bits are the binary head address of the R/W head selected for the current read/write operation. Although eight binary addresses can be decoded from bus address bits A<2:0>H, the RD51 disk drive contains four heads so it only uses head addresses 0–3.
4	Write Gate	The WD1010 chip asserts this bit high (1) to inform the 8088 processor of data being written on the disk. This signal also enables the write current circuits in the disk drive.
5	Drive Write Fault	The disk drive asserts this bit high (1) to indicate that a condition exists at the drive that may cause improper writing on the disk. When this bit is set, the disk drive inhibits further writing on the disk until the error condition is corrected.
6	Drive Ready	When the disk drive together with SEEK COMPLETE asserts this bit high (1), it indicates that the drive is ready to read, write, or seek. When this bit is low (0), all reading, writing, and seeking are inhibited.
7	Track 0	The disk drive sets this bit high (1) when the R/W heads are positioned over cylinder 0 (the data track furthest away from the spindle).

4.5.2 Commands and Sequence of Operation

The controller module instruction set consists of six commands. The commands are summarized below and described in the following paragraphs.

1. Scan ID – Finds first valid header and return information
2. Seek – Moves disk heads to cylinder with no verify
3. Restore – Returns drive heads to cylinder zero
4. Format – Writes headers on desired track
5. Read Sector – Reads sector and check CRC
6. Write Sector – Writes data field with CRC

NOTE

The controller module does not support the WD1010 long command.

The purpose of the long command was to allow the user to append some form of error correction code (ECC) to a data field. No provision was made in the controller module to support ECC other than appending seven bytes to the end of the data field.

A write-long sector is the same as the write sector except that 2 bytes of CRC are not appended to the data field. Instead, seven additional bytes are read from the sector buffer and appended to the data field end.

A read-long command is the same as the read command except that no CRC check is made on the data field and an additional seven bytes are read from the disk into the sector buffer.

A multiple-sector command for either read or write is not supported on the current controller. This command's problem is possible incompatibilities between the current WD1010-00 and the WD1010-05 chips which will be the WD1010 chip version that will be used when it is available.

4.5.2.1 Scan ID Command – A scan ID command determines the location of the heads on the disk. The controller reads the disk, looking for the first valid header. Upon finding a valid header, the task register file is loaded with the appropriate data and an interrupt is generated indicating end of command. The controller issues an implied scan ID command if the drive selection is changed.

4.5.2.2 Seek Command – A seek command causes the controller to calculate the direction and number of steps to move the heads. Step pulses are issued and an interrupt is generated to indicate end of command. The controller does not wait for seek complete status nor does it do position verification. A stepping rate used for a seek command is retained as the default stepping rate until another seek command or a restore command is issued.

4.5.2.3 Restore Command – A restore command returns drive heads to a position over cylinder zero. The controller will set the direction line to step out. It will then issue a single step pulse to the drive, wait for a seek complete status, and then check for track zero indication. This will continue until track zero is seen or until 1024 step pulses have occurred. If track zero is seen, the controller will interrupt indicating end of command. If the controller issues the 1024 step pulses without seeing the track zero indication, it will set the track zero error bit in the error register, set the error flag in the status register, and interrupt indicating end of command. As with the seek command, a stepping rate indicated during a restore command will be

the default step rate until either another restore command is issued or until a seek command is issued. Although step rate is set during a restore command, the rate set will not affect a restore command's speed because the controller must wait for seek complete status after every step pulse.

4.5.2.4 Format Command – A format command causes the controller to write the headers for the head and cylinder indicated in the task register file. The sector counter register indicates the number of sectors to be written. The sector register indicates the size of the post index gap and the size of the intersector gaps. The actual size of these gaps is three bytes more than the number loaded into the register. The sector buffer is written with the sector numbers written in the order which they will appear on the disk. Also in the sector buffer is a flag for each sector indicating whether a sector will be written with the bad block bit set in the header. A format command is the only time the bad block bit may be set. The data structure in the sector buffer is as follows.

1st byte of sector buffer	Flag for first physical sector
2nd byte of sector buffer	Number of first physical sector
3rd byte of sector buffer	Flag for second physical sector
4th byte of sector buffer	Number of second physical sector

This structure continues until the information for all desired sectors is written into the sector buffer.

NOTE
No checking is done on data supplied. This means that if the controller is asked to write more than one sector 0, it will.

The controller starts writing the disk at index and continues until the next index. The controller fills the disk from the end of the last sector until index with hexadecimal 4E data. This is also the pattern used to write a post index and intersector gaps. Hexadecimal FF is the data pattern for writing the data field during a format.

The sequence of events for a format command are as follows.

1. Load task register file. The controller will move the heads if necessary to the desired cylinder. It will then issue a DRQ interrupt and wait for Buffer Ready to be set.

2. The 8088 processor loads the sector buffer with the desired format information and sets Buffer Ready.

3. The controller waits for index and begins writing the format onto the disk.

4. The controller interrupts after writing the disk to indicate end of command.

Only three errors can occur during a format command.

1. Drive not ready
2. Write fault
3. Seek not complete

The controller, however, does not verify the headers. To verify a format command, the 8088 processor must specifically issue a read command.

4.5.2.5 Read Sector Command – A read sector command moves the data field of a sector into the controller sector buffer. The task register file is loaded with the desired sector information and the command register written with the read command. The controller then repositions the heads if necessary and searches for the desired sector. It then moves the data field into the sector buffer. The controller then issues a DRQ interrupt. The 8088 processor then empties the sector buffer. After the processor empties the sector buffer, it sets Buffer Ready and the controller issues an interrupt to indicate the command end. Six errors can occur.

1. Drive not ready
2. Write fault
3. Seek not complete
4. ID not found
5. DAM not found
6. Data field CRC

The normal sequence of operation for a read from the disk is as follows.

1. Load the sector number, cylinder, and SDH registers with the target read location.
2. Wait for an operation complete interrupt.
3. Read 512 bytes of data from the data buffer register.
4. Set the Set Buffer Ready (bit 0) in the secondary command register.

4.5.2.6 Write Sector Command – A write sector command writes data into a sector data field. The desired location is loaded into the task register file and the write command is loaded into the command register. The controller moves the heads to the appropriate location on the disk and then issues a data request interrupt (DATA RQT). The host loads the data into the sector buffer and sets Buffer Ready. The controller writes the data stored in the sector buffer into the data field of the desired sector. The controller interrupts after writing the disk to indicate the command end. The write is a blind write, that is, the controller does not verify written data. Four errors can occur.

1. Drive not ready
2. Write fault
3. Seek not complete
4. ID not found

The normal sequence of operation for a write to the disk is as follows.

1. Load the sector number, cylinder, and SDH registers with the target write location.
2. wait for an operation complete interrupt.
3. Load 512 bytes of data into the data buffer register.
4. Set the Set Buffer Ready (bit 0) in the secondary command register.

4.6 INTERFACE CONNECTOR SIGNALS

The RD51 controller module contains two 40-pin connectors and one 34-pin connector. The two 40-pin connectors (J1 and J4) plug into J5 and J4 on the system module to allow the controller module to communicate with the 8088 processor through the address, data, and control buses on the system module. See Figure 4-1.

The 34-pin connector (J2) carries the disk control, status, and MFM read/write data through an interconnect cable between the controller module and the disk drive. The signals these connectors carry are described in Tables 4-11, 4-12, and 4-13.

Table 4-11 Controller Module/System Module Connector (J1) Signals

Pin Number	Signal Mnemonic	Direction†	Description
1	BAD0 H	I/O	Buffered Address/Data Bit 0 – Data bit 0 to/from the controller bus transceivers.
3	BAD1 H	I/O	Buffered Address/Data Bit 1 – Data bit 1 to/from the controller bus transceivers.
5	BAD2 H	I/O	Buffered Address/Data Bit 2 – Data bit 2 to/from the controller bus transceivers.
7	BAD3 H	I/O	Buffered Address/Data Bit 3 – Data bit 3 to/from the controller bus transceivers.
9	BAD4 H	I/O	Buffered Address/Data Bit 4 – Data bit 4 to/from the controller bus transceivers.
11	BAD5 H	I/O	Buffered Address/Data Bit 5 – Data bit 5 to/from the controller bus transceivers.
13	BAD6 H	I/O	Buffered Address/Data Bit 6 – Data bit 6 to/from the controller bus transceivers.
15	BAD7 H	I/O	Buffered Address/Data Bit 7 – Data bit 7 to/from the controller bus transceivers.
17	BUS A0 H	I	Bus Address Bit 0 – This bit in conjunction with address bits 1–3, selects the drive, R/W head, and accesses the controller registers.
19	BUS A1 H	I	Bus Address Bit 1 – This bit in conjunction with address bits 0, 2, and 3, selects the drive, R/W head, and accesses the controller registers.
21	BUS A2 H	I	Bus Address Bit 2 – This bit in conjunction with address bits 0, 1, and 3, selects the drive, R/W head, and accesses the controller registers.
23	BUS A3 H	I	Bus Address Bit 3 – This bit in conjunction with address bits 0–3, selects the drive, R/W head, and accesses the controller registers.
25	BUS WD SEL L	I	BUS WD1010 Select L – The 8088 I/O decoders assert this signal when the 8088 processor needs to access the registers in the WD1010 or read from/write to the sector buffer.
27,31	+5.0 V	I	+5 V dc input power
33,35,37	GND	I	Ground

* Pins not listed are not used.

† Direction of signal with respect to the controller module, I/O = Input/Output, I = Input.

Table 4-12 Controller Module/System Module Connector (J4) Signals

Pin* Number	Signal Mnemonic	Direction†	Description
1	BUS INIT L	I	Bus Initialize – This signal initializes the registers in the controller when the system is powered up or reset.
3,6,18, 20,22,24, 26,28	GND	I	Ground
4,8	+12.0 V	I	12 V dc input
6	GND	I	Ground
12,14,16	+5.0 V	I	5 V dc input
33	BWR88 H	I	Buffered Write 8088 – The 8088 processor asserts this signal to write commands to the WD1010 task file registers, the secondary command register, write data to the sector buffer, and select the drive and R/W head.
35	BRD88 H	I	Buffered Read 8088 – The 8088 processor asserts this signal to read the WD1010 task file registers, the secondary status register, the drive status register, and to read data from the sector buffer.

* Pins not listed are not used.
† Direction of signal with respect to controller module, I = Input.

Table 4-13 Controller Module/Disk Drive Connector (J2) Signals

Pin* Number	Signal Mnemonic	Direction†	Description
1	RWC L	O	Reduced Write Current – This signal goes to the disk drive and when low (0) together with write gate, causes the disk drive to use a lower value of write current for writing on the disk. When this signal is high (1), the drive uses a higher value of write current. The RD51 disk drive can internally select a high or low value of write current.
3	HD SEL 2 L	O	Select Head 2 – This signal in conjunction with HD SEL 0 L and HD SEL 1 L is the binary head address selects one of four R/W heads for reading or writing.
5	WR GATE L	O	Write Gate – When this signal is low (0), it enables the write drivers providing the disk drive has asserted SEEK COMPLETE low (0). When the write gate is high (1), it enables head actuator movement.
7	SEEK COMPLETE L	I	Seek Complete – When this signal from the disk drive goes low (0), it indicates that the R/W heads settled on the correct track. Writing is inhibited until this signal goes low (0). Seek complete is high (1) during normal seek operation.
9	TK000 L	I	Track Zero – When this signal from the disk drive goes low (0), it indicates that the R/W heads are positioned at track zero, i.e., the track furthest from the spindle.
11	WRITE FAULT L	I	Write Fault – When this signal from the disk drive goes low (0), it indicates that the disk drive detects any one of the following conditions. 1. Write current and no write gate 2. Drive select and write gate but no write current

* Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 32, and 34 are connected to controller module ground. Pins 31 and 33 are not used.

† Direction of signal with respect to controller module, O = Output, I = Input.

Table 4-13 Controller Module/Disk Drive Connector (J2) Signals (Cont)

Pin* Number	Signal Mnemonic	Direction†	Description
			3. Multiple heads, no head or improperly selected head 4. DC voltages grossly out of tolerance When Write Fault is low (0), any further writing or read/write head motion is inhibited. Write fault remains low (0) until the fault condition is corrected, and drive power is sequenced off and on.
13	HD SEL 0 L	O	Head Select 0 – This signal in conjunction with HD SEL 1 L and HD SEL 2 L is the binary head address for selecting one of four R/W heads for reading or writing.
15	DIR L	O	Direction – This output signal defines the direction the R/W heads will move when the controller issues a step pulse. When this signal is low (0), the R/W heads move towards the spindle. When high (1), the heads move from the spindle, i.e., towards track 0.
17	HD SEL 1 L	O	Head Select 1 – This signal in conjunction with HD SEL 0 L and HD SEL 2 L is the binary head address for selecting one of four R/W heads for reading or writing.
19	INDEX L	I	Index Pulse – This signal from the disk drive goes low (0), for approximately 1.5 ms once each revolution of the disk to indicate the beginning of a track.
21	READY L	I	Ready – When low (0), this signal together with SEEK COMPLETE L indicates that the disk drive is ready to read, write, or seek and that the I/O signals are valid. When high (1), all writing and seeking are inhibited.
23	STEP L	O	Step Pulse – When low (0), this signal causes the R/W heads to move in the direction which the DIR L signal defined.

* Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 32, and 34 are connected to controller module ground. Pins 31 and 33 are not used.

† Direction of signal with respect to controller module, O = Output, I = Input.

Table 4-13 Controller Module/Disk Drive Connector (J2) Signals (Cont)

Pin* Number	Signal Mnemonic	Direction†	Description
25	DRV SEL 0 L	O	Drive Select 0 – When low (0), this signal indicates to the disk drive that the controller is ready. This signal will go high if: 1. a reset command is received from the system module. 2. the ac OK signal on the system module is low (0). 3. the system module asserts BUS INIT L.
27,28	MFM WRITE DATA 0	O	+ and – MFM Write Data – This differential signal defines the data transitions to be written on the disk surface. The transition of the +MFM WRITE DATA 0 line going more positive than –MFM WRITE DATA 0 causes a flux reversal on the disk surface if the WRITE GATE is low (0).
29,30	MFM READ DATA 0	I	+ and – MFM Read Data – The controller uses this differential signal from the disk drive to recover read data from the selected drive. The transition of the +MFM READ DATA 0 signal going more positive than –MFM READ DATA 0 represents a flux reversal from the selected R/W head.

* Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 32, and 34 are connected to controller module ground. Pins 31 and 33 are not used.

† Direction of signal with respect to controller module, O = Output, I = Input.

4.7 SPECIFICATIONS AND GENERAL PERFORMANCE CHARACTERISTICS

The following paragraphs describe the physical dimensions, power requirements, environmental specifications, and general performance characteristics of the controller module.

4.7.1 Physical Dimensions

Length	32.51 cm (12.8 in)
Width	9.90 cm (3.9 in)

4.7.2 DC Power

The controller module requires the following dc power.

+5 Vdc, ±5% at 1.5 A typical (2.0 A maximum), 50 mV peak-to-peak ripple (maximum)

+12 Vdc, ±5% at 32 mA typical (50 mA maximum), 75 mV peak-to-peak ripple (maximum)

4.7.3 Environmental

The RD51 controller module meets the environmental requirements of Digital Equipment Corporation Standard 102, Class B, and the conducted and radiation emission limits which the FCC rules established for Class B computing devices.

Temperature

Operating*	10°C to 40°C (50°F to 104°F)
Storage	40°C to 70°C (–40°F to 158°F)

Humidity

10% to 90% noncondensing
maximum wet bulb, 28°C (82°F)
minimum dew point, 2°C (36°F)

Altitude (maximum)

Operating Limit	2440 m (8,000 ft)
Storage Limit	9144 m (30,000 ft)

4.7.4 General Performance Characteristics

The following paragraphs describe the general performance characteristics of the controller module when used with the RD51 disk drive.

4.7.4.1 Data Transfer Rate – The disk drive serial data transfer rate is 5 Mbits/s or one 512 byte sector is loaded into the sector buffer in approximately 1 ms. Since the WD1010 chip is capable of an interleave of 1, the actual interleave used and actual controller-to-system-module-data transfer rate depends on the rate the 8088 processor accesses the sector buffer.

4.7.4.2 Error Rate – The controller will meet an error rate of 10 raised to the tenth power bits passed per soft error when reading data from an RD51 disk drive with a window margin ±15 ns from the center of the window and a data transfer rate of 5 Mbits/s (±1%).

*Maximum temperature is reduced by 1.8°C per 1,000 m (1°F per 1,000 ft) above sea level.

4.7.4.3 Precompensation – The controller provides write precompensation of ±15 ns for the write data for cylinders at or greater than the cylinder specified by the precompensation register setting.

4.7.4.4 Track Format – Each track on the disk can contain 1 to 32 concatenated sectors of 128 bytes to 1024 bytes followed by a speed tolerance gap (Gap 4) and a 16 byte post index gap (Gap 1) of 4EH. The speed tolerance gap must be at least 208 bytes to provide for a disk speed tolerance of ±1%. The programmer chooses the number of sectors and sector size to meet this requirement.

4.7.4.5 Sector Format – Each sector is written on the disk in the following format.

Function	Number of Bytes	Pattern
Preamble	13	0
Sync Mark	1	Data = A1H, Clk = 0AH
Address Mark	1	FEH Exclusive ORed with 2 most significant bits (MSBs) of cylinder address
Cylinder ID	1	8 least significant bits (LSBs) of the cylinder address
Head ID	1	BSS00HHH B = Bad Block Mark (1) SS = Sector Size 00 = 256 bytes/sect 01 = 512 bytes/sect 10 = 1024 bytes/sect 11 = 128 bytes/sect HHH = Head Number
Sector	1	Logical sector number
CRC	2	$\times 16 + \times 12 + \times 5 + 1$
Head Turn On Gap	3	0
Data Preamble	12	0
Sync Mark	1	Data A1H, Clk = 0AH
Data Address Mark	1	F8H
Data	128–1024	User Data Field
CRC	2	$\times 16 + \times 12 + \times 5 + 1$
Head Turn Off Gap	3	0
Gap 3	40	4EH

CHAPTER 5
POWER SUPPLY AND FAN ASSEMBLY

5.1 INTRODUCTION

This chapter provides a description of the H7842-D power supply and the fan bracket assembly (part number 70-20816-01). This power supply and the fan bracket assembly are used in the Rainbow PC100-B and 100+ computers. The H7842-D power supply is also used with the Rainbow PC100-A computer when the 5 Mbyte (RCD50-BB) or 10-Mbyte (RCD51-BB) hard disk upgrade kit is installed.

The H7842-D power supply is an H7842-A power supply redesigned to provide a higher +5 V load current capacity to satisfy the additional power requirements of the hard disk drive. In addition, a two-wire cable and connector are added to supply +12 V power for a dc fan.

The H7842-D power supply is a single transistor, forward converter, switch mode ac-to-dc converter. Regulation of the dc output voltages is achieved with pulse-width-modulation techniques applied to the fixed-frequency converter.

5.2 PHYSICAL DESCRIPTION

The power supply, shown in Figure 5-1, is connected to the other system components as follows.

- To the fan bracket assembly on the front panel through 3-pin, 4-pin, and 6-pin connectors

  The 3-pin and 4-pin connectors carry the ac input power through the power switch to the power supply. Two pins of the 6-pin connector carry the +12 V power from the power supply to the dc fan.

- To the RX50 diskette drive and to an optional diskette drive through two 4-pin connectors

- To the system module through a 13-pin connector and power cable

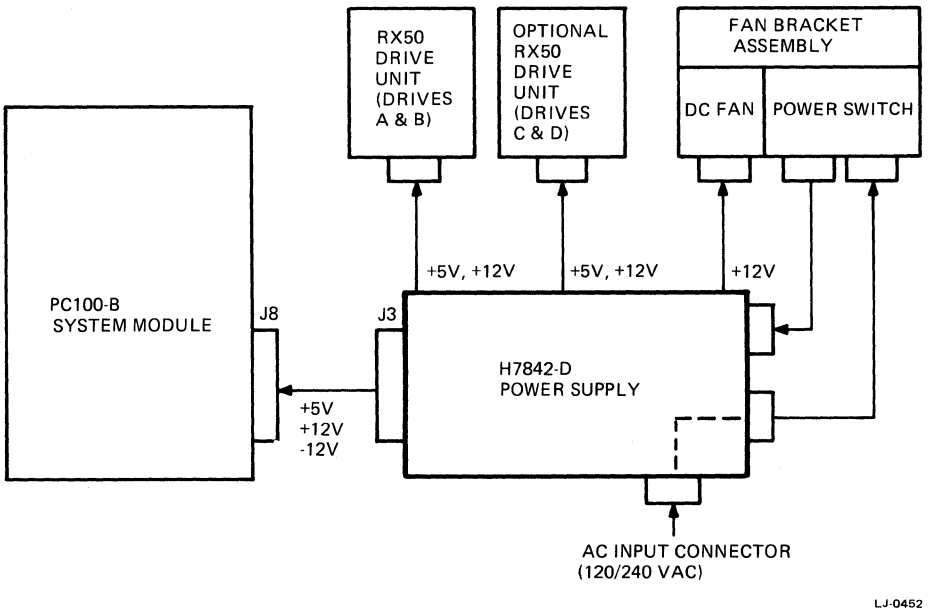

Figure 5-1 Power Supply Connections

A lip extending from one end of the power supply and a latch locking device on the opposite end secures the power supply mounts on the system unit. The fan bracket assembly is mounted on the left of the system unit and is held in place with three mounting screws on the top cover. The fan bracket assembly connectors can be inserted only one way.

A circuit breaker is on the back of the power supply to the left of the ac input connector and an ac selector switch is below the connector. See Figure 5-2. The ac selector switch slides to the right for 115 V and to the left for 230 V.

If 115 V power is applied with the ac selector switch in the 230 V position, you cannot operate the computer.

WARNING

The ac select switch must be in the 230 V position when applying 230 V or internal components will be damaged.

WARNING

Before removing the power supply cover, turn off the power and wait five minutes. Before handling any of the power supply components, use a voltmeter to make certain no high voltages are present.

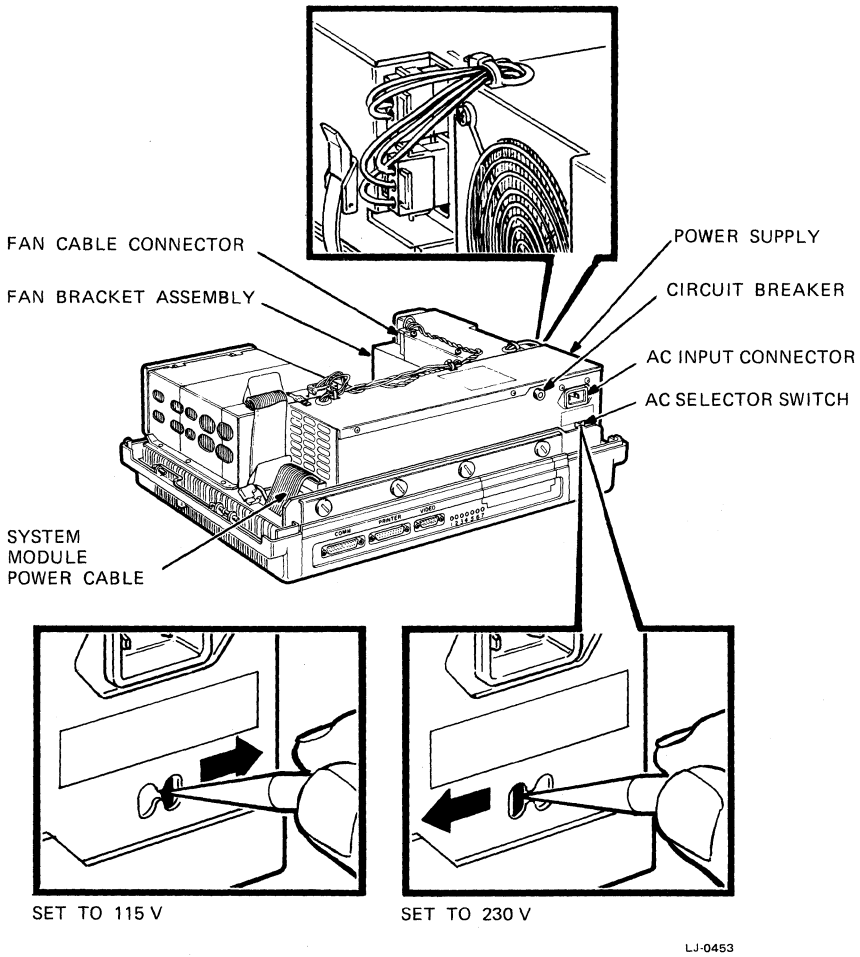

Figure 5-2 Power Supply and Fan Bracket Assembly

The ac input power and dc fan power are routed between the power supply and the fan bracket assembly as shown in Figure 5-3.

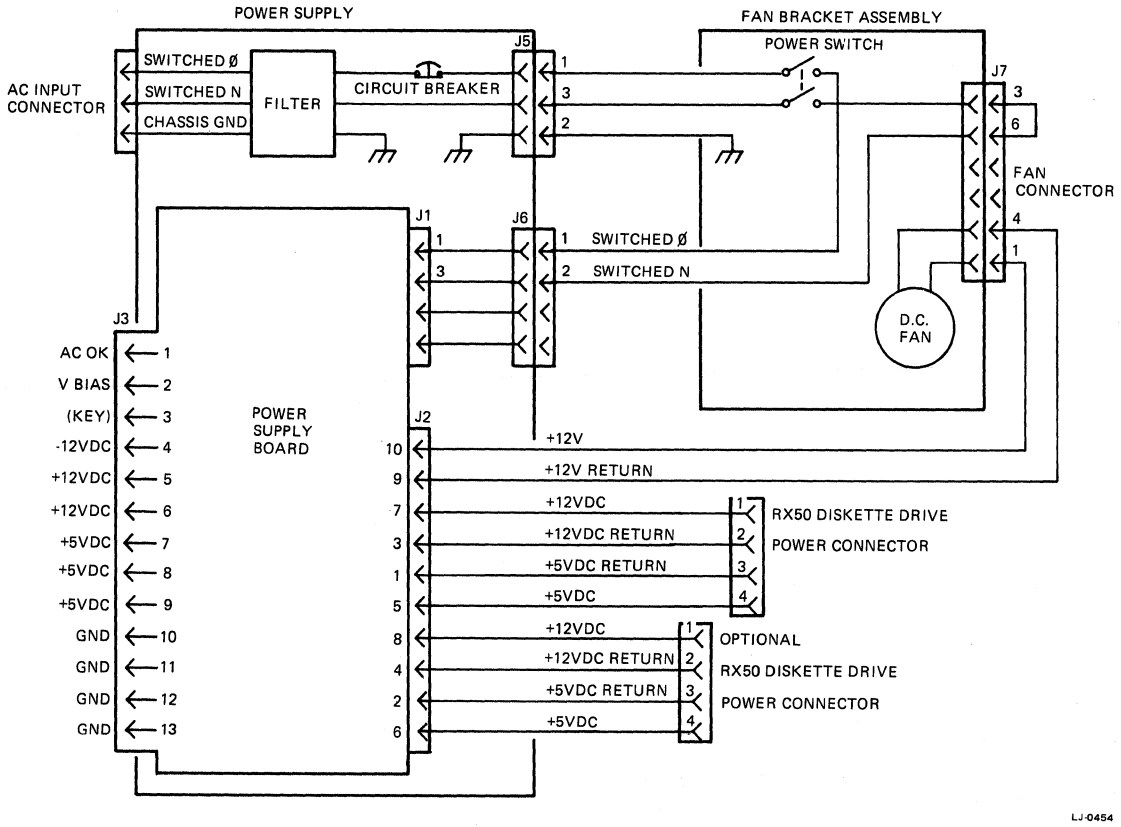

Figure 5-3 Power Supply and Fan Assembly Cabling

5.3 FUNCTIONAL DESCRIPTION

The power supply converts the ac input (either 115 Vac or 230 Vac) to +12 Vdc, −12 Vdc, and +5 Vdc. Figure 5-4 is a functional diagram of the power supply and the fan bracket assembly.

One side of the ac input line is connected across an EMI filter, 4A circuit breaker, and power switch (mounted on the front of the fan bracket assembly) to the transformer T1, and to a full wave bridge rectifier D1. The return side of the ac input line is connected across the EMI filter, power switch, ac select switch, to T1 (if 230 is selected) or to the fuse (F1) and voltage doubler (if 115 is selected). The other side of the fuse is connected to the center tap of T1. Fuse F1 is soldered into the power supply board.

D2 and D3 rectify the ac voltage at the secondary of T1 and apply it to a dc regulator. The output of the dc regulator is the V bias signal the control module uses.

With a 230 Vac input, the bridge rectifier D1 provides full-wave rectification of the input. With 115 Vac input, the bridge rectifier doubles the input voltage. With either input, the bridge rectifier output after filtering is 325 Vdc, which is applied to the primary winding (pin 1) of transformer T3.

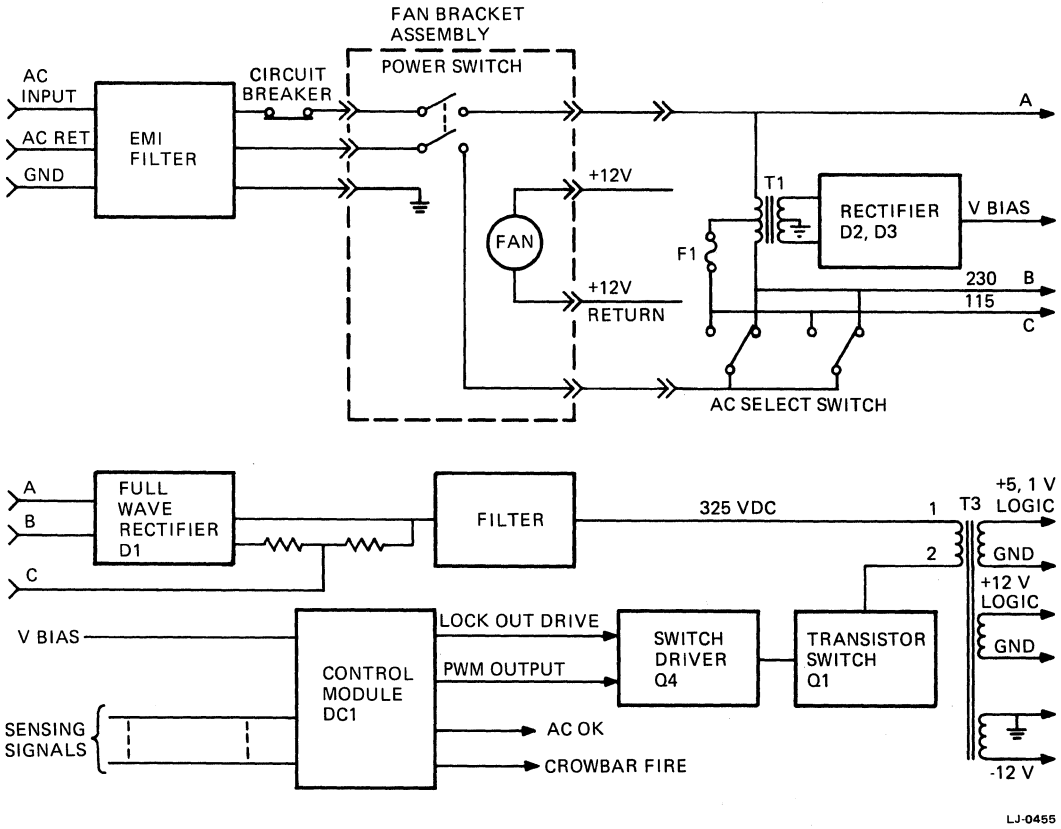

Figure 5-4 Power Supply Functional Diagram

Pin 2 of the primary winding is connected to the transistor switch (Q1). The transistor switch controls current flows through the primary winding of T3 and is turned on and off by the pulse width modulator (PWM), the output signal from the control module, through the switch driver (Q4).

Transformer T3 has three secondary windings which produce the output dc voltages of the power supply. The secondary winding for the +5.1 Vdc supply has two parallel connected windings, while the +12 Vdc and −12 Vdc secondary windings have single windings.

5.4 DETAILED CIRCUIT DESCRIPTION

Refer to circuit schematics CS-5415187-0-1 and CS-5415543-0-1 while reading the detailed circuit descriptions.

5.4.1 Power Conversion Circuits

The output of the bridge rectifier (when 230 V is used) or the voltage doubler (when 115 V is used) is 325 Vdc (measured between pins 1 and 4 of L1). L1 and C3 prevent switching spikes from contaminating the ac input line.

The secondary windings of T2 control the switching transistor Q1. The output of the pulse width modulator (PWM) from pin 19 of the control module determines the switching rate. The PWM output controls switch driver Q4, which induces current flow through the primary of T2. The power supply load determines the PWM output pulse width, thereby regulating the amount of power that is coupled across transformer T3 to the power supply output.

Transformer T3 comprises three secondary windings. The +5.1 V and +12 V secondaries operate in the forward converter mode providing half-wave rectification. Resistors R9 and R14 provide overcurrent sensing information (OC +5 V, OC +12 V), which is sent to the control module. Overvoltage sensing information (+5.1 V sense, +5.1 V O/V sense, +12.2 V sense, and −12 V O/V sense) from the output lines is also sent to the control module.

The +5.1 Vdc output is filtered and connected to pins 5 and 6 of J2 and pins 7, 8, and 9 of J3.

The +12.2 Vdc output is filtered and connected to pins 5 and 6 of J3 and pins 7, 8, 9, and 10 of J2.

The −12 Vdc secondary is operated in the fly-back mode and shunt regulated with Q2, Q3, and zener diode, D15. The −12 Vdc output is connected to pin 4 of J3.

5.4.2 Control and Sensing Circuits

The control module monitors the dc output voltages and shuts down the power supply when an overcurrent or overvoltage condition is sensed.

5.4.2.1 AC OK – The control module generates the AC OK signal (high) while a favorable comparison exists between the Bulk Sense signal and the V PR signal. The V PR signal, +5.1 Vdc, is the V Bias signal after going through the zener diode, D15.

5.4.2.2 Lockout Drive – The lockout drive circuit in the control module monitors the V Bias signal. A comparator circuit uses +5.1 Vdc as a reference. If the V Bias signal does not attain a high enough voltage level when turned on, the comparator output goes high, which turns on transistor Q1 and then transistor Q4. When Q4 turns on, +12 Vdc is applied to the base of switch driver transistor Q4, forcing it to stay on and thereby inhibiting transferring pulses to transistor switch Q11.

5.4.2.3 Crowbar Fire – The crowbar fire circuit monitors the +5 V and the −12 V overvoltage sense signals. Whenever either of these signals exceeds its tolerances, the crowbar fire signal is applied to the crowbar D10, causing it to fire, and creating an overcurrent condition on the +5.1 Vdc bus.

NOTE
Once the crowbar has fired, it can only be cleared by resetting the power supply.

5.4.2.4 Antisaturation – The antisaturation circuit monitors the voltage across D13. This voltage is a function of the −12 V current through pins 5 and 6 of T3. The comparator circuit samples the fly-back voltage pulse-to-pulse.

During a fault condition, when the voltage drop across D13 exceeds the sample input level to the comparator, pin 13 stays high and forces a high on the shut-down pin (pin 10) of the pulse width modulator, thereby shutting it down.

5.4.2.5 Voltage Time Limit (ETL) – The voltage time limit (ETL) circuit compares the half-wave rectified output from the +12 V secondary (pins 11 and 12) of T3 with the reference voltage applied to the comparator. While the output of the secondary is below the reference voltage, the comparator output remains low; otherwise, it goes high, thereby forcing a high on the shut-down pin (pin 10) of the pulse width modulator. When the comparator output goes high, it shuts down the pulse width modulator.

5.5 SPECIFICATIONS

The mechanical and electrical specifications for the H7842-D power supply are described in the following paragraphs.

5.5.1 Mechanical and Physical

Dimensions (overall)	Height 9.296 cm (3.66 in)
	Length 31.83 cm (14.50 in)
	Width 10.87 cm (4.28 in)
Weight	2.72 kg (6.0 lb)
Cooling (Forced Air)	40 CFM (minimum) dc fan

5.5.2 Input Specifications

Line Voltage Ranges	120 Vac nominal (104 Vrms to 128 Vrms) or 240 Vac nominal (191 Vrms to 256 Vrms)
Line Frequency	47 Hz to 63 Hz
Line Current	3.0 A (rms) maximum at 120 Vrms 2.0 A (rms) maximum at 240 Vrms
Real Input Power	237 W input maximum at full-rated dc output load of 142 W including 3 W for the dc fan

5.5.3 Output Specifications

Output Power at Full Load: 142 W

Output Requirement Summary:

+5.1 V at 2.5 A minimum to 11.5 A maximum
+12.2 V at 0.6 A minimum to 6.7 A maximum
−12 V at 0.0 A minimum to 0.15 A maximum

+5 Vdc, +12 Vdc, −12 Vdc Specifications

Output Voltage Variations:	+5 Vdc	+12 Vdc	−12 Vdc
Total tolerance	±6%	±6%	±7%
Initial tolerance	±2%	±2%	±3%
Line regulation	±1%	±1%	±1.5%
Load regulation	±3%	±3%	±4.0%
Load interaction	±3%	±3%	±3%
Temperature stability	±0.05%/°C	±0.05%/°C	±0.05%/°C
Long-term stability	±1%/1000 h	±1%/1000 h	±1%/1000 h

Ripple and Noise	50 mV peak-to-peak peak-to-peak	75 mV	120 mV peak-to-peak
Overcurrent Trip Point:			
Minimum	10.7 A	6.8 A	
Maximum	14.5 A	10.0 A	
Short Circuit Current	8.0 A (maximum)	4.0 A (maximum)	3.0 A (maximum)
Overvoltage Protection Range:			
Minimum trip point	5.80 V	NA	−13.0 V
Absolute maximum output voltage	7.0 V	NA	−15.0 V

5.5.4 Electromagnetic Interference Specifications

AC Power Line Susceptibility

CW RF: The power supply operates without system degradation with 3 V (rms) superimposed on the ac power lines in the frequency range of 10 kHz to 30 MHz.

Transients: The power supply operates without degradation when transients with an energy level of 2.5 W/s (maximum) are superimposed on all conductors of the power cord.

RF Field Strength Susceptibility

The power supply operates without degradation in the following amplitude modulated (AM) radio frequency (RF) fields. The RF field is 100 percent amplitude modulated with a 1000 Hz square wave.

10 kHz to 30 MHz: 2 V/m
30 MHz to 1 GHz: 3 V/m

Equipment Emissions:

Conducted: The interference voltage on all connections to commercial ac power does not exceed 80 dB above one microvolt at 10 kHz, decreasing with frequency to 58 dB above one microvolt from 150 kHz to 450 kHz, and 48 dB above one microvolt from 450 kHz to 30 MHz.

Radiated: The radiated field-strength does not exceed the following levels at 30 m (98.43 ft) from the power.

Frequency	Level
10 kHz–30 MHz	30 μ V
30 MHz–1 GHz	17 μ V

APPENDIX A
RAINBOW COMPUTER PARTS LIST

Table A-1 lists the recommended spare parts for Rainbow computers. For a more detailed parts list, refer to the *PC100 Rainbow™ 100 System Unit Illustrated Parts Breakdown*, EK-SB100-IP.

Table A-1 Rainbow 100 Computer Parts List

Part	Digital Part Number
System module, PC100-A*	70-19974-00
System module, PC100-B	70-19974-02
RX50 controller module	54-15482
Hard disk controller board	54-16019
64K byte memory board (PC100-A)†	PC1XX-AA
192K byte memory board (PC100-A)†	PC1XX-AB
128K byte memory board (PC100-B)	PC1XX-AC
256K byte memory board (PC100-B)	PC1XX-AD
64K byte memory component kit (9 chips) (PC100-B)	PC1XX-AY
256K byte memory component kit (9 chips) (PC100-B)	PC1XX-AZ
Color/graphics option board	54-15688
Extended communications option board	54-15703
ROM 0 PC100-B	23-022E5-00
ROM 1 CLUSTER 1 (German, French, English) (PC100-B)	23-020E5-00
ROM 1 CLUSTER 2 (Dutch, French, English) (PC100-B)	23-015E5-00
ROM 1 CLUSTER 3 (Finnish, Swedish, English) (PC100-B)	23-016E5-00
ROM 1 CLUSTER 4 (Danish, Norwegian, English) (PC100-B)	23-017E5-00
ROM 1 CLUSTER 5 (Spanish, Italian, English) (PC100-B)	23-018E5-00
Canadian (French) language ROM*	BG-R873A-BV
British (UK) language ROM*	BG-R876A-BV
German/Austrian language ROM*	BG-R878A-BV
Italian language ROM*	BG-R874A-BV
Swiss (French) language ROM*	BG-R376A-BV
Swiss (German) language ROM*	BG-R375A-BV
Belgian/French language ROM*	BG-R877A-BV
Spanish language ROM*	BG-R377A-BV
Dutch language ROM*	BG-R881A-BV
U.S.A. language ROM*	70-20274-15

* Part is for the Rainbow PC100-A version only.
† This memory board can be used on either the Rainbow PC100-A or PC100-B versions.
‡ The H7842-D power supply is also used on the PC100-A with the Winchester upgrade kit.

Table A-1 Rainbow 100 Computer Parts List (Cont)

Part	Digital Part Number
Belgian/Flemish language ROM*	BG-R378A-BV
Danish language ROM*	BG-R875A-BV
Finnish language ROM*	BG-R872A-BV
Norwegian language ROM*	BG-R879A-BV
Swedish language ROM*	BG-R880A-BV
Power supply (PC100-A)*	H7842-A
Power supply (PC100-B)‡	H7842-D
Communications connector loopback plug (PC100-A)*	12-15336-01
EXT COMM B loopback plug/COMM connector (PC100-B)	29-24631-00
RX50 diskettes (pack of ten)	RX50K-10
RX50 dual-diskette drive	RX50-AA
Keyboard, American/English	LK201-AA
Keyboard, British/English	LK201-AE
Keyboard, Belgian/French	LK201-AP
Keyboard, Belgian/Flemish	LK201-AB
Keyboard, Canadian/French	LK201-AC
Keyboard, Danish	LK201-AD
Keyboard, Finnish	LK201-AF
Keyboard, German/Austrian	LK201-AG
Keyboard, Dutch	LK201-AH
Keyboard, Italian	LK201-AI
Keyboard, Norwegian	LK201-AN
Keyboard, Spanish	LK201-AS
Keyboard, Swedish	LK201-AM
Keyboard, Swiss (French)	LK201-AK
Keyboard, Swiss (German)	LK201-AL
Keycap removal tool	74-27314-01
Video monitor assembly (white phosphor)	VR201-A
Color monitor	VR241-A
Cable, color monitor	BCC17
Cable, hard disk drive	17-00427-01
Cable, monitor, 1.8 m (6 ft)	17-00283-00
Cable, power supply to system module, 10.1 cm (4 in)	17-00318-02
Cable, RX50 shielded, 20.3 cm, (8 in)	17-00317-03
Cable, RX50 shielded, 36.8 cm (14.5 in)	17-00317-04
Cable, Comm printer, 3 m (10 ft)	BCC04-10
Cable, modem	BCC15
Fan bracket assembly, PC100-A*	70-19572-00
Fan bracket assembly, PC100-B	70-20816-01
Line cord, Australia	17-00198-00
Line cord, Belgium	17-00199-00
Line cord, Canada (French)	17-00083-09
Line cord, Denmark	17-00310-01
Line cord, Finland	17-00199-00
Line cord, France	17-00199-00

* Part is for the Rainbow PC100-A version only.
† This memory board can be used on either the Rainbow PC100-A or PC100-B versions.
‡ The H7842-D power supply is also used on the PC100-A with the Winchester upgrade kit.

Table A-1 Rainbow 100 Computer Parts List (Cont)

Part	Digital Part Number
Line cord, Germany	17-00199-00
Line cord, Holland	17-00199-00
Line cord, Italy	17-00199-00
Line cord, Japan	17-00083-09
Line cord, Norway	17-00199-00
Line cord, Spain	17-00199-00
Line cord, Sweden	17-00199-00
Line cord, Switzerland (French)	17-00210-00
Line cord, Switzerland (German)	17-00210-00
Line cord, United Kingdom	17-00209-00
Line cord, U.S.A.	17-00083-09
Cable, keyboard	17-00294-00
Standoffs, module	12-19857-01
Spacer, hard disk controller	74-29164-01
Filler panel, PC100 (rear)	74-27174-01
Rainbow 100 medallion*	74-27256-03
Rainbow script medallion	74-27256-06
Video alignment template	29-24371-00
Video alignment tool	74-27314-01
Packaging container for RD51	99-90045-01
Cover, plate bezel (Front)	74-26788-00

* Part is for the Rainbow PC100-A version only.
† This memory board can be used on either the Rainbow PC100-A or PC100-B versions.
‡ The H7842-D power supply is also used on the PC100-A with the Winchester upgrade kit.

APPENDIX B
DIAGNOSTIC TESTS

B.1 INTRODUCTION

The Rainbow computer runs two types of diagnostic tests that detect and isolate problems which may occur in the system.

1. An internal diagnostic test that runs when the computer is turned on, reset, or when the selftest option is selected from the Main System Menu.

2. A diskette diagnostic test that runs a series of test programs which reside on the diskette.

B.2 INTERNAL DIAGNOSTIC TEST

The internal diagnostic test is a series of test programs that are a part of the firmware which resides in ROM 0. The power-up test program checks the internal logic of the Rainbow computer automatically everytime it is powered on. If the Rainbow computer is not set to auto-boot and the power-up test runs successfully, the computer displays the Main System Menu as shown in Figure B-1.

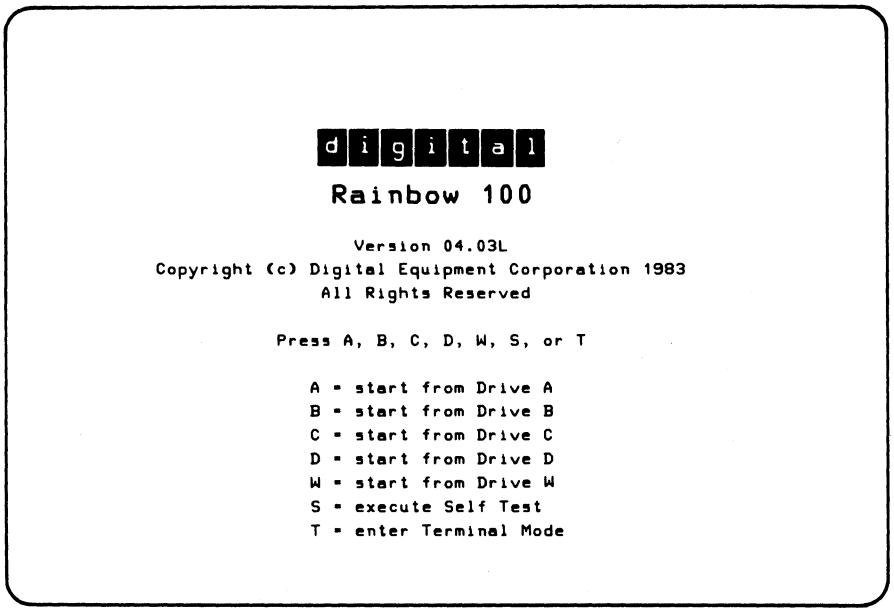

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Figure B-1 Rainbow Main System Menu

NOTE

The Main System Menu selection, "W = start from Drive W", is not available on the PC100-A or PC100-A with the Winchester upgrade kit.

When the Rainbow computer is set to auto-boot, the power-up test is run before starting the selected boot device. If the power-up test runs successfully, the computer loads the operating system program from the selected boot device and displays the operating system heading instead of the Main System Menu.

If the power-up test detects an error, the computer displays an error message above the Main System Menu and also displays an error code on the diagnostic lights on the back panel as shown in Figure B-2.

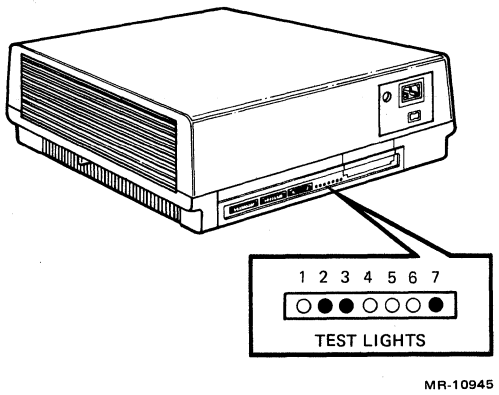

Figure B-2 Diagnostic Error Lights

The selftest program of the internal diagnostic test provides additional tests for the diskette drives. Load a blank diskette into the drive to run the selftest. To start the selftest press the S key while the Main System Menu is displayed on the screen. If the selftest detects an error, it prints a message on the screen and displays an error code on the diagnostic lights. If the selftest completes successfully, the computer once again displays the Main System Menu on the screen.

Table B-1 lists the error messages which the computer may display during the power-up, reset, and selftest, and the light display for each error message.

NOTE

The words in brackets in the message column are those that the model PC100-A displays.

Table B-1 Internal Diagnostic Test Messages

Message Number	Message	Tested During: Power-Up	Reset	Self-test	Light Display 1 2 3 4 5 6 7	Fatal
1	Main Board [video]	Yes	No	Yes	o x x o x o x	Yes
2	Main Board* [unsolicited interrupt]	Yes	Yes	Yes	x x x x o x o	Yes
3	Drive A (or B) [index]	No	No	Yes	o o x o o x x	No
4	Drive A (or B) [motor]	No	No	Yes	x x o o o x x	No
5	Drive A (or B) [seek]	No	No	Yes	o x o o o x x	No
6	Drive A (or B) [read]	No	No	Yes	x o o o o x x	No
7	Drive A (or B) [restore]	Yes	No	Yes	o x x o o x x	No
8	Drive A (or B) [step]	Yes	No	Yes	x o x o o x x	No
9	System Load Incomplete [system load]	No†	No	No	o o o o o o o	No
10	Main Board [video, vfr]	Yes	No	Yes	x x x o x o x	Yes
11	System Load Incomplete [boot load]	No†	No	No	o o o o o o o	No
12	Drive A (or B) [not ready]	No†	No	Yes	o o o o o x x	No
13	Keyboard	Yes	Yes	Yes	x x o x o x o	Yes
14	Main Board [nvm data]	Yes	No	Yes	x x x x o x x	No
16	Interrupts Off*	Yes	Yes	Yes	x x x o o o o	Cond.
17	Main Board [video ram]	Yes	Yes	Yes	x x x o x x o	Yes
18	Main Board [Z80 crc]	Yes	Yes	Yes	x x x x o o x	Yes
19	Main Board [ram 0–64K]	Yes	Yes	Yes	- - - x x o x	Yes
20	Main Board* [unsolicited interrupt, Z80]	Yes	Yes	Yes	x x x o o o x	Yes

NOTES:
o = on, o = off, - = on or off
Cond. = conditional
*These errors can occur at any time because their circuits are monitored constantly.
†These messages may occur during power-up if auto-boot is selected.

Table B-1 Internal Diagnostic Test Messages (Cont)

Message Number	Message	Tested During: Power-Up	Reset	Self-test	Light Display 1 2 3 4 5 6 7	Fatal
21	Drive Not Ready	No†	No	No	o o o o o o o	No
22	Remove Card or Diskette	Yes	Yes	Yes	o x x o o o x	No
23	Non-System Diskette	No†	No	No	o o o o o o o	
24	New Memory Size = nnnK	Yes	No	No	o o o o o o o	No
25	Set-Up Defaults Stored	Yes	Yes	Yes	o x x o o o x	No
26	Main Board [ram arbitration]	Yes	No	Yes	x x x o x o o	Yes
27	Memory Board [ram option]	No	No	Cond.	- - - x x o o	No
28	RX50 Controller Board	Yes	No	Yes	x x x o o x x	No, but you cannot use a diskette; use terminal mode only
29	Main Board* [Z80 response]	Yes	Yes	Yes	x x x x o o o	No
30	Main Board [rom crc, rom 0]	Yes	No	Yes	x x x x x x x	Yes
31	Main Board [rom crc, rom 1]	Yes	No	Yes	x x x x x x o	Yes
	Main Board, rom crc, rom 2	Yes	No	Yes	x x x o x x x	Yes
33	Main Board [contention]	Yes	No	Yes	o o o o o x o	Yes
40	Main Board [printer port]	Yes	No	Yes	x o x x o x o	No, but you cannot use the printer
50	Main Board [keyboard port]	Yes	No	Yes	o o x x o x o	Yes
60	Main Board [comm. port]	Yes	No	Yes	o x x x o x o	No, but terminal mode is not operational

NOTES:

x = on, o = off, - = on or off
Cond. = conditional
*These errors can occur at any time because their circuits are monitored constantly.
†These messages may occur during power-up if auto-boot is selected.

The following paragraphs describe some possible causes of the error messages listed in Table B-1. The message in parentheses after the message number is the message that is displayed on the PC100-A computer.

Drive A (or B) – Message 3 (index)
Message 6 (read)

The diskette is write-protected; is inserted incorrectly in the drive; or is for a different computer. Reinsert the diskette; run the selftest program again.

If the message persists, insert another diskette into the drive and run the selftest program again.

Make sure the drive cables are installed properly.

If the message still occurs, replace the parts in the following order.

1. diskette drive
2. diskette drive cable
3. RX50 controller module

Drive A (or B) – Message 7 (restore)
Message 8 (step)

Make sure that the diskette drive cables are installed correctly. If the error still persists, exchange the parts in the following order.

1. diskette drive
2. diskette drive cable
3. RX50 controller module

Drive A (or B) – Message 4 (motor)

The diskette may be bent and slowing down the motor, or the motor may be running too fast. Check the diskette for creases, smears, or dirt. Try another diskette in the drive and run the selftest again.

If the problem persists after trying several diskettes, replace the diskette drive.

Drive A (or B) – Message 5 (seek)

The diskette may be unformatted.

Insert another diskette into the drive; run the selftest again.

If the problem persists after trying several diskettes, make sure that the diskette drive cables are installed correctly. If the problem still persists, replace the diskette drive.

Drive A (or B) – Message 12 (not ready)

When you run the selftest program the computer displays this message if any of the following occur.

- There is no diskette in the specified drive. Insert a diskette into the drive.

- The diskette is upside-down in the drive. Reinsert the diskette into the drive.
- The drive door is not closed. Close the drive door.

Run the selftest program again after correcting the problem. If the problem persists, make sure that the diskette drive cables are installed correctly. If the problem still persists, replace the diskette drive.

Drive Not Ready – Message 21

When you start the operating system the computer displays this message if any of the following occur.

- There is no diskette in the specified drive. Insert a diskette into the specified drive.
- The diskette is upside-down in the drive. Insert the diskette correctly into the drive.
- Drive C, D, or W is specified on a computer with drives A and B only. Specify drive A or B.
- The drive door is not closed. Close the drive door.

If message still occurs, run the selftest to see if Message 12 occurs. Then follow the recommended steps for Message 12.

Interrupts Off – Message 16

The computer displays this message when you turn on the Rainbow computer or while you run an application program.

This message is displayed in three ways.

1. If the message appears alone on the screen (a fatal message), turn the computer off and on again. If the error persists after several tries, replace the system module.
2. If the message displays above the Main System Menu (a nonfatal message), turn the computer off and on again. If the problem persists, after several tries, replace the system module.
3. If the message displays while running an application program, you should remove the application program diskette from the drive, and then turn the computer off and on again.

   If the computer does not display the message when you turn the computer on, rerun the application program. If the computer displays the message while rerunning the program, report the problem to the vendor of the application program or, if you wrote the program, check the program for a "bug" that has turned the interrupts off.

Keyboard – Message 13

When you turn on the Rainbow computer the computer displays this message if the keyboard is not connected; a key is pressed; or the keyboard is not working properly. Check the following; then, turn the computer off and on again.

- Do not press any keys while the computer is going through power-up or reset.

- Make sure the keyboard cable is secured to the back of the monitor and to the bottom of the keyboard.
- Check for any keys that may be stuck; run your fingers over the top of the keyboard keys.
- Make sure video connector (VIDEO) is securely connected.

If the problem persists after several tries, replace the keyboard.

Main Board – **Message 1 (video)**
Message 10 (video, vfr)
Message 17 (video ram)
Message 18 (Z80 crc)
Message 19 (ram 0–64K)
Message 20 (unsolicited interrupt, Z80)
Message 26 (ram arbitration)
Message 33 (contention)
Message 50 (keyboard port)

Turn the computer off and on again. If the problem persists after several tries, replace the system module.

Main Board – Message 14 (nvm data)

When you turn on the Rainbow computer the computer displays this message if the previous Set-Up selections are not read correctly. The Set-Up selections that were previously saved are not in effect.

Have the customer review the Set-Up selections; press **<Shift/D>** to recall default settings; and press **<Shift/S>** to save them. Turn the computer off and on again. If the problem persists after several tries, replace the system module.

Main Board – Message 29 (Z80 response)

The computer displays this message when you turn on the Rainbow computer or when you start the operating system. Turn the computer off, on again. Make sure you are not using a VT180 system diskette. Insert another Rainbow operating system diskette into the drive and start again.

If the problem persists after several tries, replace the system module.

Main Board – Message 30 (rom crc, rom 0)
Message 31 (rom crc, rom 1)
(rom crc, rom 2)

Turn the computer off, on again. If the message still occurs after several tries, replace the system module

Main Board – Message 40 (printer port)

When you turn on the Rainbow computer the computer displays this message if the printer connecto (PRINTER) is not working properly.

Turn the computer off and on again. If the error persists after several tries, replace the system module

Main Board – Message 60 (comm. port)

When you turn on the Rainbow computer the computer displays this message if the communications connector (COMM) is not working properly.

Turn the computer off and on again. If the problem persists after several tries, replace the system module.

Main Board – Message 2 (unsolicited interrupt)
Memory Board – Message 27 (ram option)

The computer could display either of these messages when the selftest program finds a problem in the optional memory board.

Using the Rainbow diagnostic diskette, select the Individual Test Menu and run subtest [1], Memory (8088). If the problem persists reseat the optional memory board and run the same subtest.

If the error still persists, try to isolate the problem to a specific chip using procedures described in Appendix B of *Rainbow™ Pocket Service Guide* (EK-PC100-PS).

New Memory size = nnnK – Message 24

If you have just installed or removed additional memory, the system displays this message only once when you first turn on the Rainbow computer. Confirm that the number (nnnK) is the correct amount of memory. If the message appears and you have not installed or removed memory, check to see that the memory board is not loose.

Non-System Diskette – Message 23

When you start the operating system the computer displays this message if the diskette in the drive is not the system diskette. Insert a system diskette into a drive and start the operating system again.

Remove Card or Diskette – Message 22

When you turn on the Rainbow computer the computer displays this message if:

- the protective card is in the drive and the drive door is closed. Remove the protective card; and
- the diskette is upside-down or inserted incorrectly in the drive and the drive door is closed. Remove the diskette.

Insert the diskette correctly; then, turn the computer off and on again.

RX50 Controller Board – Message 28

Turn the computer off and on again. If the problem persists after several tries, remove the RX50 controller board and insert it again. It may have loosened from the system module. If the problem still persists, replace the RX50 controller board.

Set-Up Defaults Stored – Message 25

When you turn on the computer it displays this message to indicate that a problem was found and corrected in the part of the computer that saves your Set-Up selections. This message means you are at the

Language Selection Menu. The Set-Up selections that you have previously saved are not in effect; the default Set-Up selections (those set at the factory) are in effect. The message is informative only.

Reset and save the Set-Up selections you require.

System Load Incomplete – Message 9 (system load)
Message 11 (boot load)

When you start the operating system the computer displays this message if any of the following occur.

- The diskette is write-protected and is upside-down in the drive. Insert the diskette correctly in the drive.
- The diskette in the drive is not a Rainbow operating system diskette. Insert a Rainbow operating system diskette in the drive.
- The operating system program on the diskette is unreadable.
- The diskette is blank and unformatted.

Restart the operating system. If the problem persists, insert another operating system diskette into the drive and restart the operating system.

If the selftest runs successfully, run Test Drives A and B from the Rainbow diagnostic diskette menu, described in Paragraph B.3.1. Because the RX50 disk drives contain most of the moving parts in the system, a problem can be expected more often with the diskette drives than with the rest of the system.

Generally, you will find the trouble by running these tests. However, if the power-up test, selftest, and the Test Drives A and B all ran successfully, run the Test computer selection from the Rainbow diagnostic diskette menu, described in Paragraph 3.3.2. The Test Computer selection is a collection of individual tests that run one after the other. It takes about 30 minutes to run, but you can depend on this selection to detect most hardware faults. After the Test Computer selection finds the trouble and you replace the failing part, do not run the entire test again to verify the fix. Run the one test that found the trouble from the Display Individual Test menu described in Paragraph B.3.3.

When you know generally where a problem is, run one or more of the relevant individual tests described in Paragraph B.3.3. For example, if the system runs well but cannot print on the printer, run selftest, the comm/printer/keyboard port test, comm/printer external loopback test, and the printer confidence test.

Run selftest and any appropriate individual tests after you install a new part, to verify proper operation.

B.3 DIAGNOSTIC DISKETTE TESTS

To start the diagnostic diskette, insert it into drive A and type A at the Main System Menu. You can also start the diagnostic diskette from drives B, C, or D. The computer will display the Main Diagnostic Menu, as shown in Figure B-3. You can select the tests described in the following text from this menu. You must have two good blank diskettes to run selection 1 or 2 from this Menu. Table B-2 alphabetically lists the diagnostic diskette error messages that will display if a problem occurs, and the table also suggests corrective action.

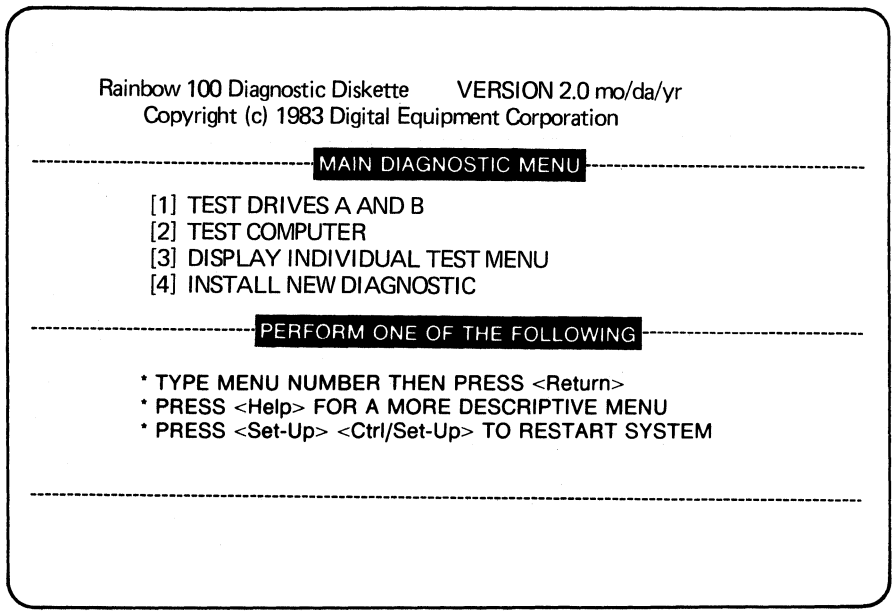

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Figure B-3 Main Diagnostic Menu

Table B-2 Diskette Diagnostic Test Messages

Messages	Possible Source/ Corrective Action
Diagnostic Executive Messages	
SYSTEM ERROR: COMPUTER CANNOT FIND SUFFICIENT MEMORY	Diagnostic diskette or system module. Try another diskette. Replace system module.
SYSTEM ERROR: DISK READ OR WRITE FAILED RESTART SYSTEM	Diagnostic diskette, diskette drive, or system module. Try another diskette. Replace system module.
SYSTEM ERROR: COMPUTER CANNOT READ TEST FILE FROM THE DISK	Diagnostic diskette. Try another diskette.
SYSTEM ERROR: COMPUTER CANNOT READ MESSAGE FILE FROM THE DISK	Diagnostic diskette. Try another
SYSTEM ERROR: COMPUTER NOT RUNNING CORRECTLY	Try another diagnostic diskette. Replace system module.
Memory (Set-Up) Test Messages	
FAILURE: MAIN BOARD: SET-UP MEMORY DOES NOT STORE DATA CORRECTLY	Make sure memory board is installed correctly.
FAILURE: MAIN BOARD: MEMORY STORES DATA INCORRECTLY	System module. Replace system module.
FAILURE: MAIN BOARD: CANNOT COPY SET-UP MEMORY	System module. Replace system module.
FAILURE: MEMORY OPTION BOARD: MEMORY STORES DATA INCORRECTLY	Optional memory board component. See Appendix B of *Rainbow™ Pocket Service Guide* (EK-PC100-PS) for corrective action.
Memory (8088) Test Messages	
FAILURE: MAIN BOARD: INVALID SET-UP DATA FOR OPTIONAL MEMORY	System module. Replace system module.
ERROR: OPTION MEMORY BOARD PRESENT; SET-UP SHOWS IT IS NOT PRESENT	Memory size is incorrect. Make sure memory board is installed correctly. Check memory size.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
ERROR: OPTION MEMORY BOARD NOT PRESENT; SET-UP SHOWS IT PRESENT	Memory size is incorrect. Make sure memory board is installed correctly. Check memory size.
SYSTEM ERROR: COMPUTER CANNOT FIND SUFFICIENT MEMORY	System module. Replace system module.
SYSTEM ERROR: SYSTEM CLOCK DOES NOT WORK	System module. Replace system module.
ERROR: SET-UP FOR MEMORY SIZE IS NOT CORRECT	Memory size is incorrect. Make sure memory board is installed correctly.
FAILURE: MEMORY OPTION BOARD: PARITY DETECTION DOES NOT WORK	Switch 4 on the memory board should be on; check switch. If problem persists, replace memory board.
FAILURE: OPTION MEMORY: MEMORY SIZING INCORRECT	Memory board component.
FAILURE: OPTION MEMORY BOARD: OPTION MEMORY SIGNAL IS INCORRECT	Replace memory board.
MEMORY TEST TERMINATED TEST CANNOT CONTINUE - PLEASE RESTART SYSTEM	Diagnostic diskette.
Memory (8088/Z80) Test Messages	
FAILURE: MAIN BOARD: MEMORY STORES DATA INCORRECTLY	System module. Replace system module.
SYSTEM ERROR: SYSTEM CANNOT FIND SUFFICIENT MEMORY	System module. Replace system module.
SYSTEM ERROR: TEST PROGRAM DOES NOT FUNCTION CORRECTLY	Diagnostic diskette.
Diskette System Error Messages	
FAILURE: MAIN BOARD: ILLEGAL INTERRUPT TO Z80	Repeat test; if error persists, replace system module.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
Z80 DIAGNOSTIC FILE NOT FOUND	Cannot find file on diskette.
FAILURE: MAIN BOARD: Z80 RESPONSE FAILURE	Repeat test; if message persists, replace system module.
SYSTEM ERROR: INSUFFICIENT MEMORY FOR DIAGNOSTICS	Repeat test; if message persists, replace system module.
FAILURE: RX50 CONTROLLER BOARD: FORCED LOST DATA (read) FORCED RECORD NOT FOUND (read) FORCED LOST DATA (write) FORCED RECORD NOT FOUND (write) FORCED SEEK HEAD LOAD TIMING INTERNAL REGISTER LOOPBACK READ MOTOR SHUT OFF NO TRACK GREATER THAN 43 SIGNAL RESTORE SEEK FAILURE (with no verify) WRITE SECTOR	Bad connection between system module and RX50 controller module; remove and reseat controller module. Run test again; if message persists, replace RX50 controller module.
FAILURE: RX50 CONTROLLER BOARD: WRITE SECTOR	Could be a bad diskette; try another diskette and run test again. If message persists, remove and reseat RX50 controller module; if error still persists, replace RX50 controller module.
FAILURE: DRIVE X (where X = A, B, C, or D) - DRIVE NOT READY	Diskette is not inserted properly or is upside-down; diskette drive door is open.
INDEX PULSE	Diskette may be upside-down or is not spinning.
SEEK (with verify)	Could be a bad diskette; rerun test using another diskette.
READ SECTOR	May occur after a write sector failure. Could be a bad diskette; try another diskette.
WRITE SECTOR	Could be a bad diskette; try another diskette.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
DISKETTE WRITE PROTECTED	Write-protect tab is on diskette.
NOTE **The following diskette drive error messages may occur from poor connection between the RX50 controller module and the diskette drive. Reseat cables and rerun tests. If any of these errors persist, remove and replace the diskette drive.**	
FAILURE: DRIVE X (where X = A, B, C, or D) - RESTORE	No track 0 signal coming from drive; insert and remove protective card; try again; replace diskette drive.
STEP	Head did not move in correct amount of time; insert and remove protective card; try again. Replace diskette drive.
MOTOR SPEED	Diskette drive motor is turning too fast or too slow; diskette may be warped; try another. Replace diskette drive.
STEP-IN	Head did not move toward spindle correctly; replace diskette drive.
STEP-OUT	Head did not move away from spindle correctly; replace diskette drive.
MULTI-TRACK TIMING	Head did not move away from spindle correctly; replace diskette drive.
Memory (Z80) Test Error Messages	
SYSTEM ERROR: CANNOT LOAD Z80 TEST PROGRAM FROM DISKETTE	Diagnostic diskette.
SYSTEM ERROR: TEST DOES NOT FUNCTION CORRECTLY	Diagnostic diskette or system module.
FAILURE: MAIN BOARD: Z80 FAILED TO START MEMORY TEST	System module. Replace system module.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
FAILURE: MAIN BOARD: Z80 FAILED TO COMPLETE MEMORY TEST	System module. Replace system module.
FAILURE: MAIN BOARD: Z80 PRIVATE MEMORY DOES NOT STORE DATA CORRECTLY	System module. Replace system module.
FAILURE: MAIN BOARD: Z80 CANNOT COPY DATA TO SHARED (Z80/8088) MEMORY	System module. Replace system module.
FAILURE: MAIN BOARD: Z80 CANNOT RESTORE DATA TO Z80 PRIVATE MEMORY - TEST CANNOT CONTINUE, PLEASE RESTART SYSTEM -	Reboot system and try again; if problem persists, replace system module.
FAILURE: MAIN BOARD: Z80 DID NOT EXECUTE THE TEST CORRECTLY	Diagnostic diskette or system module.
System Interaction Error Messages	
FAILURE: MAIN BOARD: I/O ERROR COMM CHANNEL (A) ERROR PRINTER KEYBOARD PORT ERROR DISKETTE WRITE ERROR SYSTEM ERROR	Try test again. If error persists, replace system module.
Z80 DIAGNOSTIC FILE NOT FOUND	Try another diskette
FAILURE: DRIVE B: WRITE ERROR	Try another diskette.
FAILURE: DISKETTE WRITE-PROTECTED	Remove write-protect tab.
Video Controller Test Error Messages	
FAILURE: MAIN BOARD: VIDEO ERROR VERTICAL RETRACE RATE	The vertical retrace rate is either too slow or too fast. Replace the system module.
FAILURE: MAIN BOARD: VIDEO ERROR A LOOPBACK CHECK IS INCORRECT	The information sent to the video output is being altered. Replace the system module.
Keyboard Test Error Message SYSTEM ERROR: KEY PROCESSING	Replace system module.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
Winchester (Hard Disk) Diagnostic Error Messages	
HARD DISK OPTION NOT DETECTED	The hard disk option is missing or is not seated correctly. Press the **Help** key for more information; then check inside the system unit. The hard disk controller or the cables may be loose. Check connections.
FAILURE: HARD DISK CONTROLLER: (followed by:) DRIVE NOT SELECTED DRIVE NOT READY	Check the cables that connect the drive to the controller.
FAILURE: HARD DISK CONTROLLER: R/W ERROR IN HEAD SELECT REGISTER	The hard disk controller is not seated firmly on the system module.
FAILURE: HARD DISK CONTROLLER: IMPROPER STATUS, COMMAND COMPLETION	Small connector on hard disk drive cable or 4-wire cable is not connected to disk drive.
FAILURE: HARD DISK CONTROLLER: (followed by:) A SEEK COMMAND DID NOT RESULT IN THE CORRECT NUMBER OF STEP PULSES CONTROLLER STEPPING TOO FAST HEAD NOT POSITIONED OVER EXPECTED TRACK NO INTERRUPT ON COMMAND COMPLETION R/W ERROR DETECTED IN REGISTER R/W ERROR IN SECTOR BUFFER SECTOR BUFFER COUNTER FAILED TO CLEAR SEEK ATTEMPTED IN WRONG DIRECTION STATUS NOT PROPERLY SET AFTER ISSUING A COMMAND STEP FLAG NOT CLEARED/SET	Reseat the hard disk controller board and run the hard disk diagnostic again. If error persists, replace the hard disk controller board.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
TRK00 NOT CLEARED AFTER A SEEK UNABLE TO CLEAR ERROR FLAG UNABLE TO FORCE ABORT ERROR UNABLE TO FORCE I.D. NOT FOUND UNABLE TO RESET INDEX LATCH UNEXPECTED RD51 INTERRUPT WRITE FAULT TRACK 00 NOT FOUND ABORTED COMMAND TRACK 00 NOT DETECTED AFTER RESTORE OR SEEK TO TRACK 0 HARD READ FAILURE, BAD SURFACE DRIVE ROTATIONAL SPEED TOO SLOW/FAST	
FAILURE: DRIVE OR CONTROLLER? (followed by:)	Pin 3 on large connector of the hard disk drive cable is damaged. Remove the cable from the hard disk drive. If pin cannot be straightened, install a new cable.
CRC ERROR DATA ERROR BAD WRITE OR READ SLOW/FAST STEPPING RATE UNABLE TO SET INDEX LATCH HARD SCAN FAILURE HARD WRITE FAILURE D.A.M. (data address mark) NOT FOUND I.D. NOT FOUND	Check the hard disk controller and make sure it is firmly seated in its connectors. If error persists, replace following components with known good components in the following sequence. 1. Hard disk drive cable 2. Hard disk drive 3. Hard disk controller
FAILURE: MEDIA: BAD SECTOR DETECTED ON CYLINDER 0	Press the **Help** key and follow the instructions on the screen. Re-initialize the hard disk using the hard disk utility program. Run the diagnostic again. If failure still occurs, replace the disk drive.
FAILURE: CONTROLLER OR DRIVE?: (followed by:) DIAGNOSTIC CYLINDER HAS INCORRECT DATA	Press the **Help** key and follow the instructions on the screen. Replace the parts in the following order.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
HARD READ FAILURE	1. Hard disk drive cable 2. Hard disk drive 3. Hard disk controller
Extended Communications Option Internal Diagnostic Error Messages	
FAILURE: COMM OPTION BOARD (followed by:) COMM OPTION NOT INSTALLED MPSC DATA BUS WRITING ZEROS	Verify that option has been installed. Reseat COMM option by removing and installing it. Rerun External Comm test. If error persists, replace COMM option module.
DMA TERMINAL COUNT CHANNEL 0 DMA TERMINAL COUNT CHANNEL 2 External Comm A BUFFER COMPARE ERROR External Comm B BUFFER COMPARE ERROR SYNC DETECT Ext. Comm A SYNC DETECT External Comm B	Make sure nothing is attached to COMM connectors. If there is,remove and rerun test. If error persists, reseat COMM option by removing and installing it. Rerun test. If error persists, persists, replace COMM option.
DMA REGISTER DATA TEST DMA DIAGNOSTIC INTERRUPT COMMAND STATUS REGISTER RESET COMMAND STATUS REGISTER READ MPSC DATA BUS BAUD RATE GENERATOR	A hardware fault exists in the COMM option. Reseat option by removing and installing it. Rerun test. If error persists, replace COMM option.
Extended Communications Option External Diagnostic Error Messages	
FAILURE: COMM OPTION BOARD: (followed by:) CARRIER SENSE CLOCK SUBSTITUTION	Check that loopback plug is attached *only* to EXT COMM B connector. If not, attach plug and rerun test. If error persists, reseat COMM option and rerun test. If error persists, replace COMM option.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
COMM SIGNAL "DTR" TO "DSR" COMM SIGNAL "RTS" TO "CTS" & "BRLSD/CD" COMM SIGNAL "SPSL" TO "RI" COMM SIGNAL "SRTS" TO "SI" COUNT DONE DMA TERMINAL COUNT CHANNEL 0 DMA TERMINAL COUNT CHANNEL 2 Ext. Comm A BUFFER COMPARE ERROR Ext. Comm B BUFFER COMPARE ERROR MISSING IDLE DETECT SYNC DETECT Ext. Comm A SYNC DETECT Ext. Comm B UNEXPECTED IDLE DETECT	Check that loopback plug is attached *only* to EXT COMM B connector. If not, attach plug and rerun test. If error persists, reseat COMM option and rerun test. If error persists, replace COMM option.
Color/Graphics Option Error Messages	
FAILURE: GRAPHICS OPTION: (followed by:) GRAPHICS BOARD NOT PRESENT	Option is not detected in the system. Verify that option has been installed. Remove and install option board to reseat it. Rerun test. If error persists, replace option and rerun test. If error persists, error may be in the system module.
CHARACTER BUFFER CLOCK TIMING CONTROLLER INVALID SYNCHRONIZATION CONTROLLER OR ADDRESSING	Reseat color/graphics option. Remove and install it, and rerun the test. If error persists, replace color/graphics option. Rerun test. If error persists, a hardware fault exists in the system module.

Table B-2 Diskette Diagnostic Test Messages (Cont)

Messages	Possible Source/ Corrective Action
CONTROLLER OR DATA BUS	
CONTROLLER RETURNS INVALID STATUS	
DATA BUS OR MEMORY	
ERRATIC INTERRUPT	
FOREGROUND/ BACKGROUND REGISTER OR PLANE SELECT	
GRAPHICS MASK	
MEMORY DATA	
MEMORY REFRESH	
PATTERN REGISTER OR PATTERN MULTIPLIER	
PROGRAMMABLE LOGIC ARRAY	
SCROLL MAP OR DATA BUS	
TEXT MASK	

B.3.1 Test Drives A and B Selection

The Test Drives A and B selection checks disk drives A and B only. Use the Disk System selection from the Individual Test Menu described in Paragraph B.3.3 to check drives C and D.

B.3.2 Test Computer Selection

The Test Computer selection checks most of the basic Rainbow computer functions including extended memory. It does not check other options or the line drivers on each port. It is a collection of individual tests that run one after the other. The Test Computer selection takes about 30 minutes to run; so use it only when you cannot find the problem with some other shorter test. After the Test Computer selection finds the trouble and you replace the failing part, do not run the Test Computer selection again to verify the fix. Run the test that found the trouble from the Individual Test Menu described in Paragraph B.3.3.

B.3.3 Display Individual Test Menu Selection

The Display Individual Test Menu selection, shown in Figure B-4, displays the individual tests that are included in the Test Computer selection. In addition, some tests require loopback connectors and user interaction and there are tests which the customer may add for optional equipment.

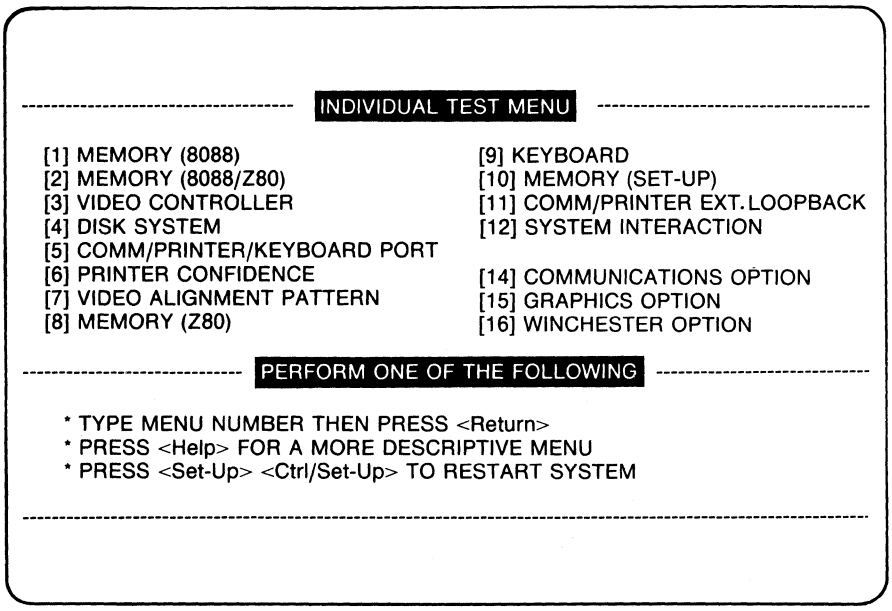

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Figure B-4 Individual Test Menu

The following paragraphs summarize the individual test selection. Press the **Help** key for additional information on each test.

1. MEMORY (8088) – The Memory (8088) test checks the memory including the optional memory board, if present. If you replace the memory board or add components to the memory board, use this test and the Memory (8088/Z80) test to verify that the new memory board works correctly.

2. MEMORY (8088/Z80) – This test checks the memory that is shared between the two internal processors.

3. VIDEO CONTROLLER – This test checks refresh signal timing, internal loopback signals, and displays each of the special video capabilities of the screen for 20 seconds. You must watch the screen to check these capabilities. To begin the displays, press the **Resume** key. To hold a display, press the **Interrupt** key. To continue to the next display, press the **Resume** key.

4. DISK SYSTEM – This diagnostic tests disk drives A and B, C and D, or all of them. This performs the same test as the drives A and B selection described in Paragraph B.3.1, however, it allows you to test drives C and D also.

5. COMM/PRINTER/KEYBOARD PORT – This test checks all internal data transmission paths except for the line driver circuits, on the system module. A loopback plug is not required for this test.

6. PRINTER CONFIDENCE TEST – This test checks the printer. Press the **Escape** key. Type your test message on the keyboard, then press the **Escape** key again. To stop the test, press the **Escape** key again or press the **Return** key.

7. VIDEO ALIGNMENT PATTERN – This test fills the entire screen with E's to help you perform screen adjustments and check intensity, sizing and spacing of characters. When the graphics option is present, this test produces a pattern with center cross hairs and corner marks that you can match with a transparent template (part number 29-24371-00).

8. MEMORY (Z80) – This test checks the 2K byte Z80A processor memory on the system module.

9. KEYBOARD – This test draws a complete keyboard on the screen. When you press a key, the monitor will indicate whether the key works. Press the **Help** key for information on exceptions. To exit the test, type out the letters.

10. MEMORY (SET-UP) – This test checks the nonvolatile memory which saves Set-Up selections after power is turned off.

11. COMM/PRINTER EXTERNAL LOOPBACK – This test checks the communications and printer circuits including the line drivers on the system module that could not be checked with selection 5 above. You must install a loopback connector on both the COMM connector and the PRINTER connector before you can run this test.

12. SYSTEM INTERACTION – This test exercises all system tasks at once to check for timing problems. If an error is detected, the test reduces the number of tasks competing for system resources to detect the failure.

13. Not used.

NOTE

Tests 14, 15, and 16 are diagnostic tests shipped with each option. Using selection 4 from the Main Diagnostic Menu, you can add these tests to your Rainbow diagnostic diskette (version 2.0 or higher). You cannot add these tests to Version 1.0 of the diagnostic diskette (part numbers BL-T309A-BV and BL-T309B-BV). Therefore, if you have Version 1.0, run these tests from the diagnostic diskette that comes with the option.

14. COMMUNICATIONS OPTION – This selection contains the internal and external diagnostic tests that come with the extended communications option. A loopback plug (part number 12-15336-04) is required for the external diagnostic test. See the *Rainbow™ Pocket Service Guide* (EK-PC100-PS) to run this test.

15. GRAPHICS OPTION – This selection contains the color/graphics diagnostic that comes with the color/graphics option. See the *Rainbow™ Pocket Service Guide* (EK-PC100-PS) to run this test.

16. WINCHESTER OPTION – This selection contains the hard disk diagnostic (also on the Rainbow Hard Disk Utility Program diskette) that comes with the Winchester (hard disk) option. See the *Rainbow™ Pocket Service Guide* (EK-PC100-PS) to run this test.

B.3.4 Install New Diagnostic Test Selection

This selection is a feature that allows you to add the tests for each option to your diagnostic diskette. Each new option has a diskette with the diagnostic tests for that option. Use the Install New Diagnostic selection on the Main Diagnostic Menu to copy this new test to the Rainbow diagnostic diskette. Type 4, press the **Return** key and follow the instructions on the screen. To select the test for a particular option, display the Individual Test Menu (Figure B-4), type the number of the test (14, 15, or 16), and press the **Return** key.

NOTE

You cannot use this feature if you have an early Rainbow diagnostic diskette, part numbers BL-T309A-BV or BL-T309B-BV.

B.4 EXITING A DIAGNOSTIC

To return to the Main System Menu from a diagnostic program, follow the instructions on the screen. Reset the computer by entering Set-Up and pressing **<Ctrl/Set-Up>**. If you cannot enter Set-Up, you will have to set the power switch to 0, and then back to 1.

APPENDIX C
CHARACTER GENERATOR ROM CODES

The character generator ROM contains the bit patterns needed to display the characters of the following character sets.

- UK (United Kingdom)
- ASCII (American Standard Code for Information Interchange)
- SG (Special graphics)
- DEC multinational character set (displayable right-half only)

The character generator ROM also contains space for 31 additional displayable characters reserved for future use.

Table C-1 lists the characters and corresponding codes available for display in the PC100-B computer. The codes are actually a part of the address of the bit-map of that character in the character generator ROM. They are the eight most significant bits of the 12-bit ROM address. The four least significant bits of the address select the proper scan line (1–10) within the character.

NOTE

All reserved characters are displayed as a reversed question mark.

Table C-1 Displayable Character Codes

Character Code in RAM 8-Bits (H)	Character Code Received 7-Bits	Character Set* UK	ASCII	SG	Name of Character
00	00	X	X	X	Null, ignored on RCV, displays a blank
	5F			X	Blank
01	60			X	Diamond
02	61			X	Checkerboard (BLOB)
03	62			X	HT (horizontal tab)
04	63			X	FF (form feed)
05	64			X	CR (carriage return)
06	65			X	LF (line feed)
07	66			X	Degree symbol
08	67			X	Plus/minus sign
09	68			X	NL (new line)
0A	69			X	VT (vertical tab)
0B	6A			X	Lower right corner
0C	6B			X	Upper right corner
0D	6C			X	Upper left corner
0E	6D			X	Lower left corner
0F	6E			X	Crossing lines
10	6F			X	Horizontal line, scan 1
11	70			X	Horizontal line, scan 3
12	71			X	Horizontal line, scan 5
13	72			X	Horizontal line, scan 7
14	73			X	Horizontal line, scan 9
15	74			X	Left 'T'
16	75			X	Right 'T'
17	76			X	Bottom 'T'
18	77			X	Top 'T'
19	78			X	Vertical bar
1A	79			X	Less than or equal
1B	7A			X	Greater than or equal
1C	7B			X	PI symbol
1D	7C			X	Not equal sign
1E	7D			X	U.K. pound sterling sign
1E	23	X			U.K. pound sterling sign
1F	7E			X	Centered dot
20	20	X	X	X	Space
21	21	X	X	X	Exclamation point
22	22	X	X	X	Double quotes
23	23	X	X	X	Number sign (pound sign)
24	24	X	X	X	Dollar sign
25	25	X	X	X	Percent sign
26	26	X	X	X	Ampersand sign
27	27	X	X	X	Single quote
28	28	X	X	X	Left parentheses
29	29	X	X	X	Right parentheses

* UK = United Kingdom, ASCII = American Standard Code for Information Interchange, SG = Special Graphics.
An X in the character set column means a RAM translation is required of 7-bit National Replacement Character codes to DEC Multinational Character codes.
Character set columns not marked indicate code translation is not required.

Table C-1 Displayable Character Codes (Cont)

Character Code in RAM 8-Bits (H)	Character Code Received 7-Bits	Character Set* UK	ASCII	SG	Name of Character
2A	2A	X	X	X	Asterisk sign
2B	2B	X	X	X	Plus sign
2C	2C	X	X	X	Comma
2D	2D	X	X	X	Dash (minus sign)
2E	2E	X	X	X	Period
2F	2F	X	X	X	Slash (fraction bar)
30	30	X	X	X	Numeral 0
31	31	X	X	X	Numeral 1
32	32	X	X	X	Numeral 2
33	33	X	X	X	Numeral 3
34	34	X	X	X	Numeral 4
35	35	X	X	X	Numeral 5
36	36	X	X	X	Numeral 6
37	37	X	X	X	Numeral 7
38	38	X	X	X	Numeral 8
39	39	X	X	X	Numeral 9
3A	3A	X	X	X	Colon
3B	3B	X	X	X	Semicolon
3C	3C	X	X	X	Left angle bracket
3D	3D	X	X	X	Equals sign
3E	3E	X	X	X	Right angle bracket
3F	3F	X	X	X	Question mark
40	40	X	X	X	At sign
41	41	X	X	X	Capital A
42	42	X	X	X	Capital B
43	43	X	X	X	Capital C
44	44	X	X	X	Capital D
45	45	X	X	X	Capital E
46	46	X	X	X	Capital F
47	47	X	X	X	Capital G
48	48	X	X	X	Capital H
49	49	X	X	X	Capital I
4A	4A	X	X	X	Capital J
4B	4B	X	X	X	Capital K
4C	4C	X	X	X	Capital L
4D	4D	X	X	X	Capital M
4E	4E	X	X	X	Capital N
4F	4F	X	X	X	Capital O
50	50	X	X	X	Capital P
51	51	X	X	X	Capital Q
52	52	X	X	X	Capital R
53	53	X	X	X	Capital S
54	54	X	X	X	Capital T
55	55	X	X	X	Capital U

* UK = United Kingdom, ASCII = American Standard Code for Information Interchange, SG = Special Graphics.
An X in the character set column means a RAM translation is required of 7-bit National Replacement Character codes to DEC Multinational Character codes.
Character set columns not marked indicate code translation is not required.

Table C-1 Displayable Character Codes (Cont)

Character Code in RAM 8-Bits (H)	Character Code Received 7-Bits	Character Set* UK	ASCII	SG	Name of Character
56	56	X	X	X	Capital V
57	57	X	X	X	Capital W
58	58	X	X	X	Capital X
59	59	X	X	X	Capital Y
5A	5A	X	X	X	Capital Z
5B	5B	X	X	X	Left square brackets
5C	5C	X	X	X	Backslash
5D	5D	X	X	X	Right square brackets
5E	5E	X	X	X	Circumflex
5F	5F	X	X	X	Underline
60	60	X	X		Accent grave
61	61	X	X		Lowercase A
62	62	X	X		Lowercase B
63	63	X	X		Lowercase C
64	64	X	X		Lowercase D
65	65	X	X		Lowercase E
66	66	X	X		Lowercase F
67	67	X	X		Lowercase G
68	68	X	X		Lowercase H
69	69	X	X		Lowercase I
6A	6A	X	X		Lowercase J
6B	6B	X	X		Lowercase K
6C	6C	X	X		Lowercase L
6D	6D	X	X		Lowercase M
6E	6E	X	X		Lowercase N
6F	6F	X	X		Lowercase O
70	70	X	X		Lowercase P
71	71	X	X		Lowercase Q
72	72	X	X		Lowercase R
73	73	X	X		Lowercase S
74	74	X	X		Lowercase T
75	75	X	X		Lowercase U
76	76	X	X		Lowercase V
77	77	X	X		Lowercase W
78	78	X	X		Lowercase X
79	79	X	X		Lowercase Y
7A	80	X	X		Lowercase Z
7B	7B	X	X		Left braces
7C	7C	X	X		Vertical line (broken)
7D	7D	X	X		Right braces
7E	7E	X	X		Tilde
7F	7F	X	X	X	Reserved for character generator ROM CHECKSUM. This character code displays miscellaneous characters and should not be used.

* UK = United Kingdom, ASCII = American Standard Code for Information Interchange, SG = Special Graphics.
An X in the character set column means a RAM translation is required of 7-bit National Replacement Character codes to DEC Multinational Character codes.
Character set columns not marked indicate code translation is not required.

Table C-1 Displayable Character Codes (Cont)

Character Code in RAM 8-Bits (H)	Character Code Received 7-Bits	Character Set* UK	ASCII	SG	Name of Character
80		X	X	X	Unfilled rectangle for 'auto-blanked cursor'
81					Reserved
82					Reserved
83					Reserved
84					Reserved
85					Reserved
86					Reserved
87					Reserved
88					Reserved
89					Reserved
8A					Reserved
8B					Reserved
8C					Reserved
8D					Reserved
8E					Reserved
8F					Reserved
90					Reserved
91					Reserved
92					Reserved
93					Reserved
94					Reserved
94					Reserved
95					Reserved
96					Reserved
97					Reserved
98					Reserved
99					Reserved
9A					Reserved
9B					Reserved
9C					Reserved
9D					Reserved
9E					Reserved
9F					Reserved
A0					Not used
A1					Inverted exclamation point
A2					Cent sign
A3					U.K. pound sterling sign
A4					Reserved (DEC STD 169)
A5					Yen sign
A6					Reserved (DEC STD 169)
A7					Section sign
A8					General currency sign
A9					Copyright sign
AA					Feminine ordinal indicator
AB					Left angle quotation marks

* UK = United Kingdom, ASCII = American Standard Code for Information Interchange, SG = Special Graphics.
An X in the character set column means a RAM translation is required of 7-bit National Replacement Character codes to DEC Multinational Character codes.
Character set columns not marked indicate code translation is not required.

Table C-1 Displayable Character Codes (Cont)

Character Code in RAM 8-Bits (H)	Character Code Received 7-Bits	Character Set* UK ASCII	SG	Name of Character
AC				Reserved (DEC STD 169)
AD				Reserved (DEC STD 169)
AE				Reserved (DEC STD 169)
AF				Reserved (DEC STD 169)
B0				Degree sign
B1				Plus/minus sign
B2				Superscript 2
B3				Superscript 3
B4				Reserved (DEC STD 169)
B5				Micro sign
B6				Paragraph sign
B7				Middle dot
B8				Reserved (DEC STD 169)
B9				Superscript 1
BA				Masculine ordinal indicator
BB				Right angle quotation mark
BC				Fraction 1/4
BD				Fraction 1/2
BE				Reserved (DEC STD 169)
BF				Inverted question mark
C0				Capital A with grave accent
C1				Capital A with acute accent
C2				Capital A with circumflex accent
C3				Capital A with tilde
C4				Capital A with umlaut
C5				Capital A with ring
C6				Capital AE with dipthong
C7				Capital C with cedilla
C8				Capital E with grave accent
C9				Capital E with acute accent
CA				Capital E with circumflex accent
CB				Capital E with umlaut
CC				Capital I with grave accent
CD				Capital I with acute accent
CE				Capital I with circumflex accent
CF				Capital I with umlaut
D0				Reserved (DEC STD 169)
D1				Capital N with tilde
D2				Capital O with grave accent
D3				Capital O with acute accent
D4				Capital O with circumflex accent
D5				Capital O with with tilde

* UK = United Kingdom, ASCII = American Standard Code for Information Interchange, SG = Special Graphics.
An X in the character set column means a RAM translation is required of 7-bit National Replacement Character codes to DEC Multinational Character codes.
Character set columns not marked indicate code translation is not required.

Table C-1 Displayable Character Codes (Cont)

Character Code in RAM 8-Bits (H)	Character Code Received 7-Bits	Character Set* UK	ASCII	SG	Name of Character
D6					Capital O with umlaut
D7					Capital OE with dipthong
D8					Capital O with slash
D9					Capital U with grave accent
DA					Capital U with acute accent
DB					Capital U with circumflex accent
DC					Capital U with umlaut
DD					Capital Y with umlaut
DE					Reserved (DEC STD 169)
DF					German small sharp S
E0					Lowercase A with grave accent
E1					Lowercase A with acute accent
E2					Lowercase A with circumflex accent
E3					Lowercase A with tilde
E4					Lowercase A with umlaut
E5					Lowercase A with ring
E6					Lowercase AE with dipthong
E7					Lowercase C with cedilla
E8					Lowercase E with grave accent
E9					Lowercase E with acute accent
EA					Lowercase E with circumflex accent
EB					Lowercase E with umlaut
EC					Lowercase I with grave accent
ED					Lowercase I with acute accent
EE					Lowercase I with circumflex accent
EF					Lowercase I with umlaut
F0					Reserved (DEC STD 169)
F1					Lowercase N with tilde
F2					Lowercase O with grave accent
F3					Lowercase O with acute accent
F4					Lowercase O with circumflex accent
F5					Lowercase O with tilde
F6					Lowercase O with umlaut
F7					Lowercase OE with dipthong
F8					Lowercase O with slash
F9					Lowercase U with grave accent
FA					Lowercase U with acute accent
FB					Lowercase U with circumflex accent
FC					Lowercase U with umlaut
FD					Lowercase Y with umlaut
FE					Reserved (DEC STD 169)
FF					Not allowed; this is 'termination' code

* UK = United Kingdom, ASCII = American Standard Code for Information Interchange, SG = Special Graphics.
An X in the character set column means a RAM translation is required of 7-bit National Replacement Character codes to DEC Multinational Character codes.
Character set columns not marked indicate code translation is not required.

APPENDIX D
GLOSSARY

A

Access Time – A time interval between the request to store (or retrieve) data and the actual start of the storage (or retrieval) process.

Address – A number, label, or name that indicates the location of data in memory.

Alphanumeric Character – A character generated by a standard keyboard (alphabetic, numeric, symbol, or control character).

ANSI – American National Standards Institute, 1430 Broadway, New York, N.Y. 10018. The Rainbow computer responds to certain control functions standardized by ANSI.

Answerback Message – A short message of up to 20 characters that the Rainbow computer transmits upon receipt of an enquiry control (ENQ) character; generated by a **<Ctrl/Break>** and sent to a remote computer or (optionally) upon first starting communications in the terminal mode.

Architecture – A basic building blocks of a hardware or software system.

ASCII – American Standard Code for Information Interchange.

ASCII Code – A standard code consisting of 7-bit coded characters (8 bits including parity check), used for information interchange among data processing systems, data communications systems, and associated equipment. The ASCII set includes numbers, letters, punctuation, and control characters.

Assembly – A hardware item consisting of two or more subassemblies, such as the power and fan assemblies. In software, the process of converting a program written in assembly language into a binary coded program that can be executed.

Asynchronous – Pertaining to a communications method in which the data has its own synchronizing information in start and stop bits. This method allows the transmitting and receiving devices to internally process data at their optimum speed.

Attribute – A characteristic assigned to a character or a word, such as boldface, underlining, or blinking.

Attribute RAM – A memory bank (4K bytes of random access memory) for storing the attributes of each character in screen memory.

Auto-Answerback – A feature in the Rainbow computer that allows it to send its answerback message to a host computer when communications are established between computers.

Auto-Screen Blank – A feature in the Rainbow computer that turns off the display on the screen after 30 minutes, leaving only a "phantom" blinking cursor.

Auto-Wrap – A feature in the Rainbow computer preventing characters from printing over the last character on a line; instead, they continue printing on the next line.

Auto-XON/XOFF – A feature in the Rainbow computer that automatically synchronizes it to a remote computer so not to lose data.

Auxiliary Memory – A device for storing information from the computer, such as disks, tapes, drums, and so on. (Also called secondary storage.)

B

Baud – 1) A unit of signaling speed equal to the number of discrete conditions or signal events per second in Morse code, one b/ps in a train of binary signals, and one 3-bit value per second in a train of signals each of which can assume one of eight different states. 2) In asynchronous transmission, the unit of modulation rate corresponding to one unit of interval per second. For example, if the duration of the unit interval is 20 ms, the modulation rate is 50 baud.

Baud Rate – Synonymous with signal events per second and measures serial data flow between a computer and/or communications devices. (See Baud.)

Binary – Two-valued arithmetic or logic, using values 1 and 0. All computer programs use the binary form.

Block Diagram – A simplified drawing that uses boxes and interconnecting lines to represent system components and their relationships.

Bit – 1) A binary digit whose value is either zero or one. 2) The smallest unit of data in a computer.

Bootstrap – 1) A technique or device designed to bring itself into a desired state by means of its own action. For example, a machine routine whose first few actions are sufficient to bring the rest of itself into the computer from an input device. 2) A program that loads the

operating system. The program only requires the application of power and proper insertion of the operating system disk into the disk drive.

Break – 1) To open. 2) A signal to stop transmission. 3) A space (0) on the transmit data line of transmission is enabled. 4) The key that generates such a signal.

Buffer – A storage area meant to temporarily hold data being transferred between two devices.

Bus – A circuit or group of circuits that provides a communication path between two or more devices, such as among a central processor, memory, and peripherals.

Byte – A group of binary digits that represents a unit of information, such as a letter of the alphabet, a numeral, a symbol, and so on. In the Rainbow computer, a byte consists of eight binary digits (bits).

C

CCITT – Comite Consultatif International Telegraphique et Telephoniques (International Telegraph and Telephone Consultive Committee), which sets international communications standards.

Channel – A path for electrical transmission between two points.

Character – A letter, a digit, a symbol, or an operation (such as a space, carriage return, tab, and so on) recognized by the computer.

Character Generator – An electronic circuit, in conjunction with other circuits, that causes a letter, numeral, or symbol to be displayed on a video monitor when a circuit receives an 8-bit code.

Character Set – A group of characters, each of which the computer recognizes in the form of 8 binary digits. The Rainbow computer character set consists of up to 255 characters, including foreign characters and symbols.

Checksum – A value which is the arithmetic sum of all bytes in a program or program segment. The checksum verifies that the entire program is loaded without error.

Chip – A thin slice of silicon or germanium containing electronic circuits. The chip is embedded in a multilead carrier that is typically soldered or plugged into a printed circuit board.

Command – An instruction to a computer program, entered by typing on the keyboard.

Communications Controller – Circuits interfacing the computer with another computer.

Component – A functional part of a system, subsystem, module, and so on.

Contention – A conflict between the two processors over a signal's availability in the Rainbow computer.

Control (Ctrl) – The key that starts a control function.

Control Character – A nondisplayable character, such as return, space, horizontal tab, and so on that in a particular context initiates, modifies, or halts operation.

Control Function – An action affecting the processing, transmitting, or interpreting of data.

Controller – Circuits controlling the transfer of address, data, and control signals between a computer and a peripheral device.

CP/M-86 – An operating system used with the Rainbow computer which Digital Research Inc., developed.

CRT – Cathode ray tube. Displays video information. Converts electrical signals to light.

Cursor – A blinking marker on the screen indicating where the next character typed will be placed.

Cyclic Redundancy Check (CRC) – An error detection scheme in which a check character is generated by taking the remainder after dividing all the serialized bits in a block of data by a predetermined binary number. This remainder is then appended to the transmitted data and recalculated and compared at the receiving point to verify data accuracy.

D

Data – A general term for information (numbers, letters, and symbols) stored on a diskette, for example.

Default – A selection value which the computer assumes when the user does not supply a specific value.

Delimiter – A character terminating a character string or message, or separating it from the surrounding text.

Diagnostic Program – A program detecting and isolating malfunctions.

Direct Memory Access (DMA) – A method of transferring blocks of data directly between a peripheral device and system memory without microprocessor intervention. This method significantly increases the data transfer rate, hence system efficiency.

Disk – A flat, circular, rigid platter with a magnetic coating on which information is stored. It features faster access time and greater storage capacity than a diskette.

Diskette – A flat, circular, flexible, plastic platter (similar to a 45-rpm phonograph record) that stores information. Normally, the diskette is housed in a square cover with cutouts to allow its use without removing it from its cover. (Also known as a floppy disk.)

Display – The current active area of the screen, that is, the area inside the scrolling region or the entire screen, depending on the origin mode.

Dot – The smallest displayable unit of information on the screen.

Dual-Diskette Drive – Storage device using a single motor to spin two diskettes for magnetically recording or reading information.

Dual Processor – Using two processors (the Z80A and the 8088) to execute 8- and 16-bit instructions, respectively.

Duplex – Simultaneous, two-way, independent transmissions in both directions; also called full duplex.

Dynamic RAM – Memory devices using the presence or absence of a capacitive charge to store a value. The charge must be refreshed periodically.

E

EIA – 1) Electronic Industry Association, 2001 Eye Street, N.W., Washington, D.C. 20006. 2) A communications standard set by the EIA. 3) A signal conforming to EIA standards.

Emulation – A Rainbow computer feature enabling control functions similar to those of the VT52 DECscope or those that agree with current ANSI standards.

EOT – End-of-transmission control character, created by typing control/D.

Escape (ESC) – A control character (ASCII 033_8) that provides supplementary characters or code extensions. ESC introduces a control or escape sequence.

Escape Sequence – A series of characters instructing the computer to perform a specific operation. The first is the Escape character. For example, the three characters ESC, C, and B, instruct the computer to consider the characters following as part of the British character set.

Extended Communications – A Rainbow computer option that provides an additional general-purpose port and a special high-speed port.

F

FCC – Federal Communications Commission, Washington, D.C.

FDXA – A full-duplex communications protocol that does not use modem control signals.

FDXB – A full-duplex communications protocol that uses modem control signals.

FDXC – A full-duplex communications protocol that uses modem control signals on a half-duplex modem; requires a special cable.

Firmware – An instruction program that is in read-only memory (ROM) so it will not be changed. The Rainbow computer's firmware includes a selftest program that runs when the computer is turned on and displays the Main System Menu.

Floppy Disk – A diskette.

Formatted Diskette – A diskette with its data track pattern already recorded on its surface.

Function Keys – Keys that, instead of representing a character, issue a command to the computer to perform a specific operation such as entering a Set-Up mode, displaying helpful information, and other functions that the software system assigns to these keys.

H

Hardware – The physical elements that make up a computer system; mechanical, electrical, or electronic devices.

Head – An electromagnetic device that reads data from, writes data to, or erases data from a diskette, disk, or tape.

Hertz (Hz) – A unit of frequency equal to one cycle per second.

Hexadecimal (Hex) – Pertaining to a selection, choice, or condition that has sixteen possible values or states. These values or states usually contain 10 digits and six letters A–F. Hexadecimal digits are equivalent to a power of 16.

Host Processor – A computer system containing an operating system that other computing systems or terminals can use by being electrically connected to it.

I

Index – 1) To move the cursor down to the same character position on the next line. 2) A small hole in the diskette marking the beginning of the recorded tracks.

Instructions – A repertoire of commands to the computer which follows a specific format. The command repertoire is usually referred to as the instruction set.

Integrated Circuit (IC) – A solid-state microcircuit consisting of interconnected active and passive semiconductor devices diffused into a single silicon chip.

Interface – Circuits allowing two or more components, units, subsystems, or systems to interact with each other.

Interlace – A kind of video display where the information from two fields is displayed by offsetting the vertical position of one field slightly from the other so the scans of one field appear between the scans of the other.

Interrupt – 1) Suspending a process, such as the execution of a computer program, in a way that the process can be resumed. 2) To stop a process in such a way that it can be resumed. 3) In data transmission, taking an action at a receiving station which causes the transmitting station to terminate a transmission.

K

Key – A single button on the keyboard that, when pressed, sends a letter, number, symbol, or function code to the keyboard's electronic circuitry.

Keyboard – A set of keys on or connected to a terminal. The keyboard causes the computer to generate alphanumeric characters or symbols when you press its keys. It enables you to input text and instructions to the computer.

Keyclick – An audible sound that the tone generator inside the keyboard makes when a key is pressed. In the Rainbow computer the keyclick volume is adjustable in Set-Up.

L

Large Scale Integration (LSI) – High-density integrated circuits for complex logic functions. LSI circuits can range up to several thousand transistors on a one-tenth of an inch silicon chip.

LED – A light emitting diode that illuminates when current passes through it.

Line Attribute – An attribute affecting an entire line of characters displayed on the screen, such as double-width and double-height characters.

Load – To insert a diskette into the diskette drive and close its door.

M

Mark State – The presence of a signal, or logical 1 condition, on the communications line.

Matrix – An arrangement that allows addressing of many individual points with few address lines. Used in the keyboard switch array.

Megabyte (Mbyte) – A measurement of storage capacity, abbreviated as Mbyte. One Mbyte is equal to a million bytes (characters).

Megahertz (MHz) – A unit of frequency equal to one million cycles per second.

Memory Map – A listing of addresses or symbolic representations of addresses defining the boundaries of the memory address space occupied by a program or series of programs.

Menu – A list of services or functions displayed on the screen from which you select one for the computer to do.

Microprocessor – A part of a microcomputer containing the circuits for fetching, decoding, and executing programmed instructions and maintaining the status of results as the program is executed.

Mnemonic – Symbol or symbols used instead of terminology more difficult to remember. A mnemonic usually has two or three letters.

Modem – Acronym for a device that modulates and demodulates a signal transmitting and receiving data over telephone lines.

Module – Usually refers to a plug-in electronic circuit board. For example, the RX50 controller module, extended communications module, and so on.

Monitor – 1) The device containing the video screen. 2) The video screen itself. 3) Software or hardware that observes, supervises, controls, or verifies the operations of a system.

Monochromatic – Having only one color.

MPSC – Multiprotocol Serial Controller. Provides three basic programmable protocols: asynchronous (start/stop), byte synchronous (monosync/bisync), and bit synchronous (HDLC and SDLC).

MS-DOS – A disk operating system that Microsoft Corporation developed, used widely with personal computers.

Multiplexer (MUX) – A circuit that allows selecting one of two or more input signals as the output signal.

N

New Line Mode – A feature in the Rainbow computer that, when in effect, causes the cursor to move to the beginning of the next line when the **Return** key is pressed.

Nonvolatile Memory (NVM) – A type of memory that can have its contents changed. The data, however, is not lost when the computer power is turned off.

Nonvolatile RAM – Same as nonvolatile memory.

Null Modem Cable – A cable connecting two RS-232 devices when a modem is not needed. The transmit and receive lines are reversed at the cable connectors.

O

Octal – A number system with a radix of eight.

Off-Line – Pertaining to equipment or devices that are not under the direct control of a computer. For example, when a hard copy terminal is off-line, you can use it as a typewriter.

On-Line – Pertaining to equipment, devices, and events that are in direct communication with the CPU and thereby under its control.

Operating System – A structured set of software routines that controls the execution sequence of programs run on a computer; supervises the input/output activities of these programs, and supports the development of new programs through such functions as assembly, compilation, editing, and debugging.

Overrun Error – Occurs in the PUSART if the microprocessor did not read a character before the next one arrived.

P

Palette – A choice of colors available for computer graphics.

Parallel – A data path where all bits travel simultaneously on separate wires.

Parity – 1) A method of checking for correct data which involves counting the 1 bits in each character's data pattern, and then making the sum either even or odd. 2) The choice in Set-Up for the method of checking parity, whether even, odd, mark, space, or no parity.

Peripheral Device – A general term designating various kinds of machines which operate in combination or conjunction with a computer and may or may not be physically part of the computer. Peripheral devices typically display computer data; store data from the computer and return data to the computer on demand; prepare data for human use; or acquire data from a source and convert it to a form for the computer's use. Peripheral devices include printers, keyboards, graphic display terminals, paper tape readers/punches, analog-to-digital converters, disk drives, and tape drives.

Phase Locked Loop (PLL) – A circuit separating and synchronizing the data and clocks from the raw read data received from the diskette drive or Winchester hard disk drive.

Polling – A process in which a number of peripheral devices, remote stations, or modes in a computer network are interrogated one at a time to determine if service is required.

Priority – A sequence in which various entries and tasks are processed or peripheral devices serviced. Priorities are based on analyses of codes associated with an entry or task, or the positional assignment of a peripheral device.

Program – A complete sequence of computer instructions necessary to solve a specific problem, perform a specific action, or respond to external stimuli in a prescribed manner. As a verb, it means to develop a program.

Protocol – A formal set of conventions governing the format, sequence, and relative timing of message exchange between two communications processes.

PUSART – Programmable Universal Synchronous/Asynchronous Receiver Transmitter. Receives parallel data from the microprocessor and converts it to serial data, which PUSART transmits to the keyboard. Receives serial data from the keyboard and converts it to parallel data, which PUSART transmits to the microprocessor.

R

Random Access – Accessing or storing information by using its location (address). Any random location can be read or written into in the same amount of time as any other location.

Random Access Memory (RAM) – A computer's main memory to which data is written and from which data is read. Adding a memory extension option expands this memory in the Rainbow computer.

Raster Scan – A deflection technique that causes the cathode ray tube (CRT) electron beam to move in a predefined left-to-right, top-to-bottom pattern across the CRT's face irrespective of the displayed image. The computer provides video signals which blank or unblank the beam to display the required image.

Read-Only Memory (ROM) – 1) The Rainbow computer memory that contains the instructions for the power-up and reset sequences, selftest, VT102 emulation, and the program that interprets the keyboard's keys. 2) Firmware. The information in read-only memory cannot be changed.

Refresh – 1) The process of repeatedly rewriting the screen with data so it seems constantly lit. 2) Periodically accessing dynamic memory so it will not lose its data.

Reverse Screen – A screen attribute. When this attribute is selected, the entire screen is rendered as black characters on a white background.

Reverse Video – A character attribute. Characters are seen as dark areas in fields of light.

Rollover – Ability to accept more than one key pressed at the same time.

RS-232-C – EIA standard for communications equipment. Off or mark signals can be −3 V to −25 V; on or space signals can be +3 V to +25 V.

RS-423 – EIA standard for digital interface circuits. Signals for a binary 1 state can be −4 V to −6 V; signals for a binary 0 state can be +4 V to +6 V.

S

Screen Attribute – Applies to the entire display area; reverse screen, smooth scrolling.

Screen Memory – A memory bank (4K bytes of random access memory) for storing the displayable characters. Same as screen RAM.

Screen Width – 1) The maximum number of characters that can be displayed across the screen on one line. 2) The setting in Set-Up that allows you to select 80 or 132 columns.

Scrolling – The movement of lines of characters on a video monitor in a direction toward the top or bottom of the screen.

SCS Sequence – A Select Character Set sequence is a series of characters beginning with the Escape character instructing the computer to consider the characters that follow as part of the character set designated by the sequence. (See also Escape sequence.)

Sector – 1) One-tenth of a track on a diskette; it holds 512 bytes (characters). 2) One-sixteenth of a track on a hard disk; it holds 512 bytes (characters).

Serial Transmission – A method of transferring data in which the bits of the characters are sent sequentially on a single path.

Set-Up – A mode of the computer that is entered by pressing the **Set-Up** key, which allows you to change such features as the screen width, tab stops, margins, printer/communications baud rates, and so on.

Shared Memory – A part of the random access memory that both processors can access.

Smooth Scroll – Scrolling in which the data on the screen moves only one scan per frame.

Software – The computer programs necessary for doing useful work with the computer. Software is generally meant to include the operating system. Software can be stored on magnetic devices such as disks and diskettes. It is soft because it can be readily changed or destroyed.

Space – Absence of a signal on a communications line; a logical 0 condition.

Split Screen – Display operation where one part of the screen can scroll while another part remains stationary.

Start Bit – The first bit in a serial, asynchronous byte transmission is always a space.

Static RAM – Memory devices that do not require periodic refresh cycles, unlike dynamic RAMs which must be refreshed by external logic.

Stop Bit(s) – One or two pulses at the end of a character's data pattern that signal(s) the end of that pattern.

Synchronization – 1) Operation in exact coincidence in time or rate 2) Timing.

Synchronous Communication – A method of transferring serial binary data between computer systems or between a computer system and a peripheral device. Binary data is transmitted at a fixed rate, with the transmitter and receiver synchronized. Synchronization characters are located at the beginning of each message or block of data to synchronize the flow.

System – A combination of hardware and software that performs specific processing operations.

T

Terminal Mode – 1) An operational mode in the Rainbow computer that allows it to act like a terminal, such as a VT102 video terminal. 2) Selection T on the Main System Menu.

Track – A path on a diskette or hard disk that holds data. Eighty tracks on each diskette are used in the RX50 diskette drive, and 612 tracks on each of the two hard disks used in the RD51 disk drive.

U

Unit – A major component of a system, such as the keyboard, the monitor, and so on.

V

Vector – The address of the first instruction for an interrupt handling routine.

Vectored Interrupt – An interrupt pointing to a location in memory where a routine is stored that is associated with the interrupt.

Voltage Controlled Oscillator (VCO) – An oscillator whose frequency output is varied by increasing or decreasing the amplitude of a dc voltage input.

W

Wait State – A condition in which a process is interrupted until completion of another process, after which the interrupted process is resumed.

X

XON/XOFF – 1) The control characters synchronizing the Rainbow computer to a remote computer so data transmitted between them is not lost. XON starts data transmission, XOFF stops it. 2) The Set-Up feature that enables these characters automatically. (See Auto-XON/XOFF.)

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