TS03/TM8-E
DECmagtape system maintenance manual

EK-T3TM8-MM-001

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PREFACE

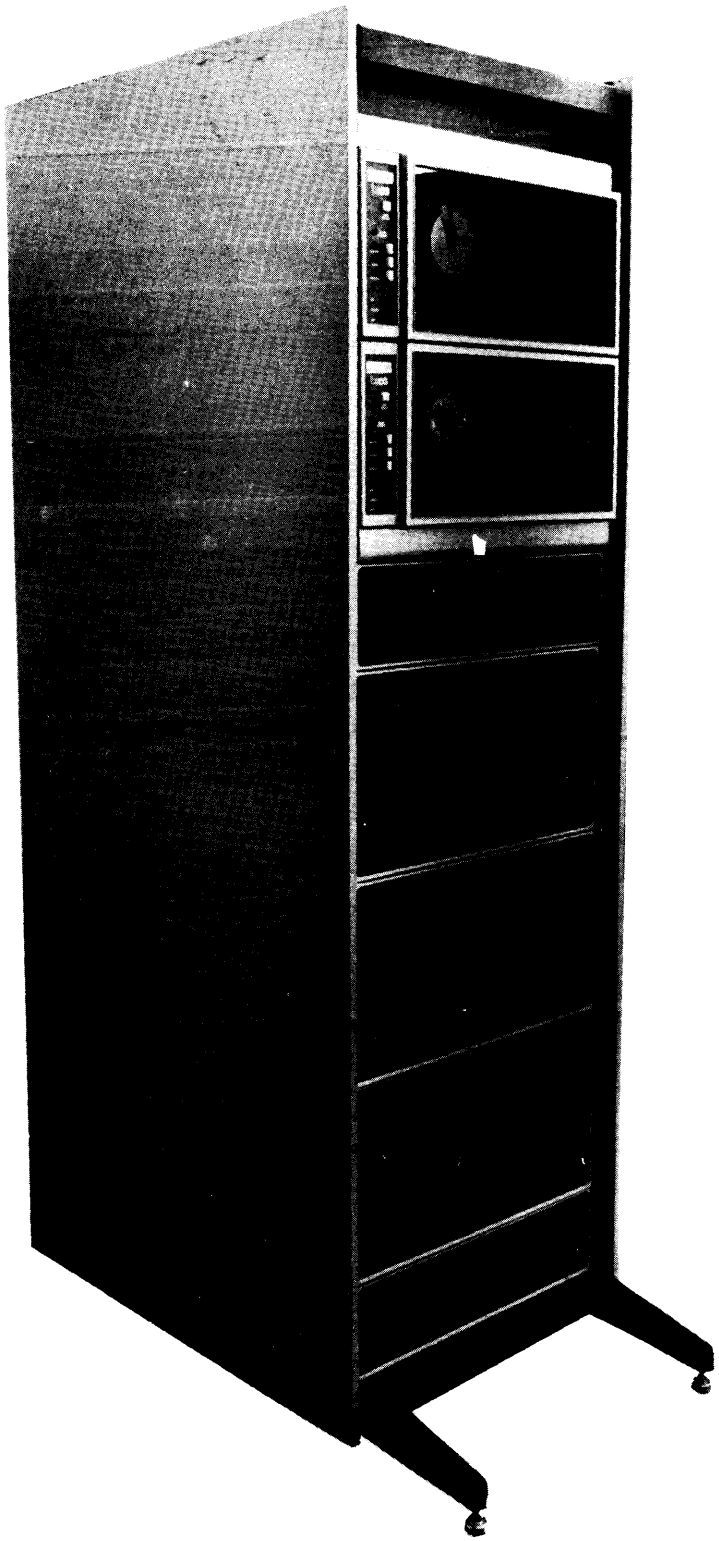
This manual provides a complete description of the TS03/TM8-E DECmagtape System henceforth referred to as the TM8-M. Included are installation instructions, operation and programming information, functional block and logic level descriptions, preventive and corrective maintenance procedures, and removal and replacement procedures. The manual is divided into three parts:

Part I contains a general description of the system, complete system installation instructions and maintenance information including customer care and operation, preventive maintenance, corrective maintenance, and removal and replacement procedures.

Part II contains a complete description of the TM8-E Controller including specifications, programming information, and functional block, logic level, and flow diagram descriptions.

Part III contains a complete description of the TS03 DECmagtape Transport including specifications, operation, and functional block, logic level, and flow diagram descriptions.

PART I
SYSTEM INFORMATION



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TM8-M DECmagtape System

CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The TM8-MA/MB* DECmagtape System is a magnetic tape storage system that interfaces with the PDP-8/A, E, F and M family of processors and peripherals and provides storage for digital information. The system reads and records digital data in parallel in a nine-channel, industry-compatible format.

1.2 SYSTEM CONFIGURATION

The TM8-M DECmagtape System is composed of the units shown in Figures 1-1, 1-2, 1-3 and 1-4, and listed below.

1. DECmagtape Controller – The TM8-E interfaces the DECmagtape system to the PDP-8 Omnibus. The controller consists of four modules which plug into the Omnibus. It controls data transfers, issues control commands to the TS03 master, and monitors system operation. Each TM8-E can control two TS03 transports: a master and a slave.

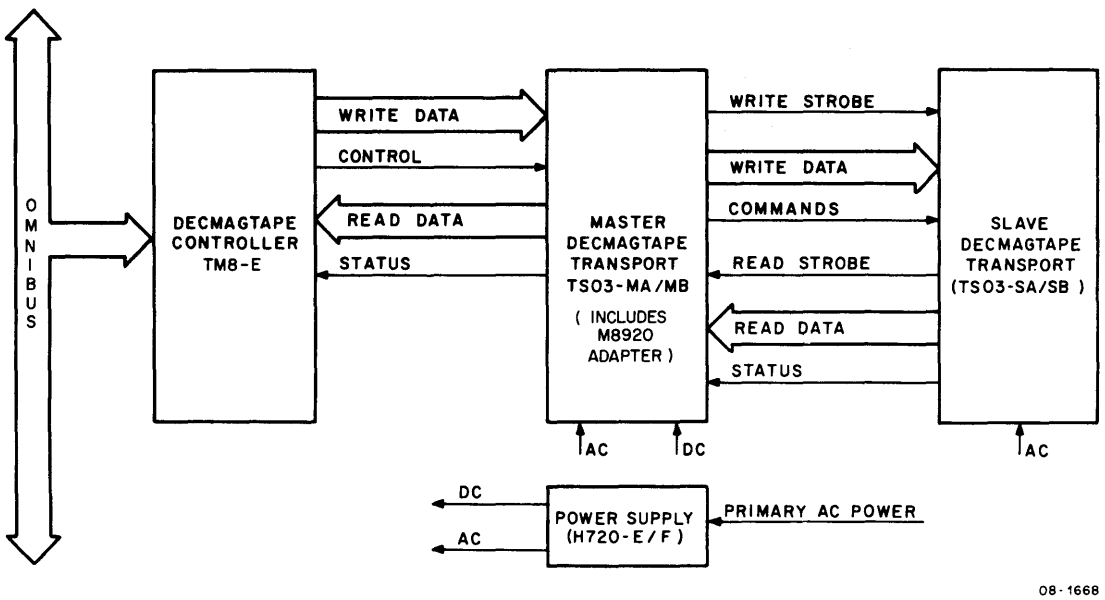


Figure 1-1 TM8-M System Configuration

*The TM8-M System is commonly referred to by its component sub-units – the TS03 and the TM8-E, hence the manual title "TS03/TM8-E DECmagtape System Maintenance Manual." However, within this manual the system will be referred to as the TM8-M. The TM8-MA is a 115 V, 60 Hz system. The TM8-MB is a 230 V, 50 Hz system.

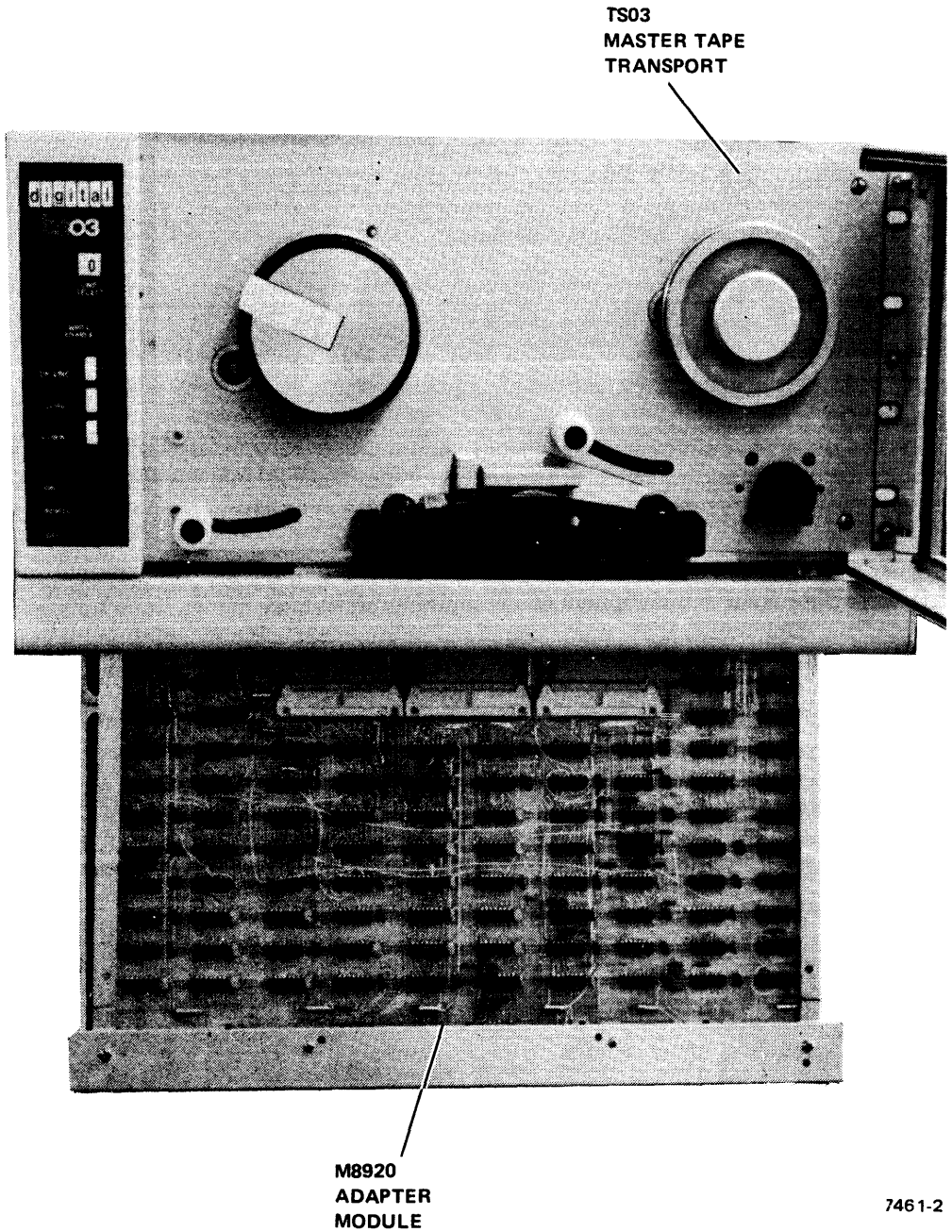


Figure 1-2 TS03-M Master Tape Transport with M8920 Adapter Module

2. Master DECmagtape Transport – The TS03-M consists of an M8920 adapter module and a TS03 tape transport. The M8920 processes commands from the controller and issues motion and read/write commands to the master and slave transports; the M8920 also monitors status lines from the master and slave transports. Any status changes at the selected transport are reported immediately to the controller. In response to inputs from the adapter, the tape transport controls tape motion and records and reads data on magnetic tape. Two models of the master DECmagtape transport are available: the TS03-MA, which requires 115 V, 60 Hz primary power and the TS03-MB, which requires 230 V, 50 Hz primary power. Both models also require +5 ± 5% V at 3 A and an AC LO signal.

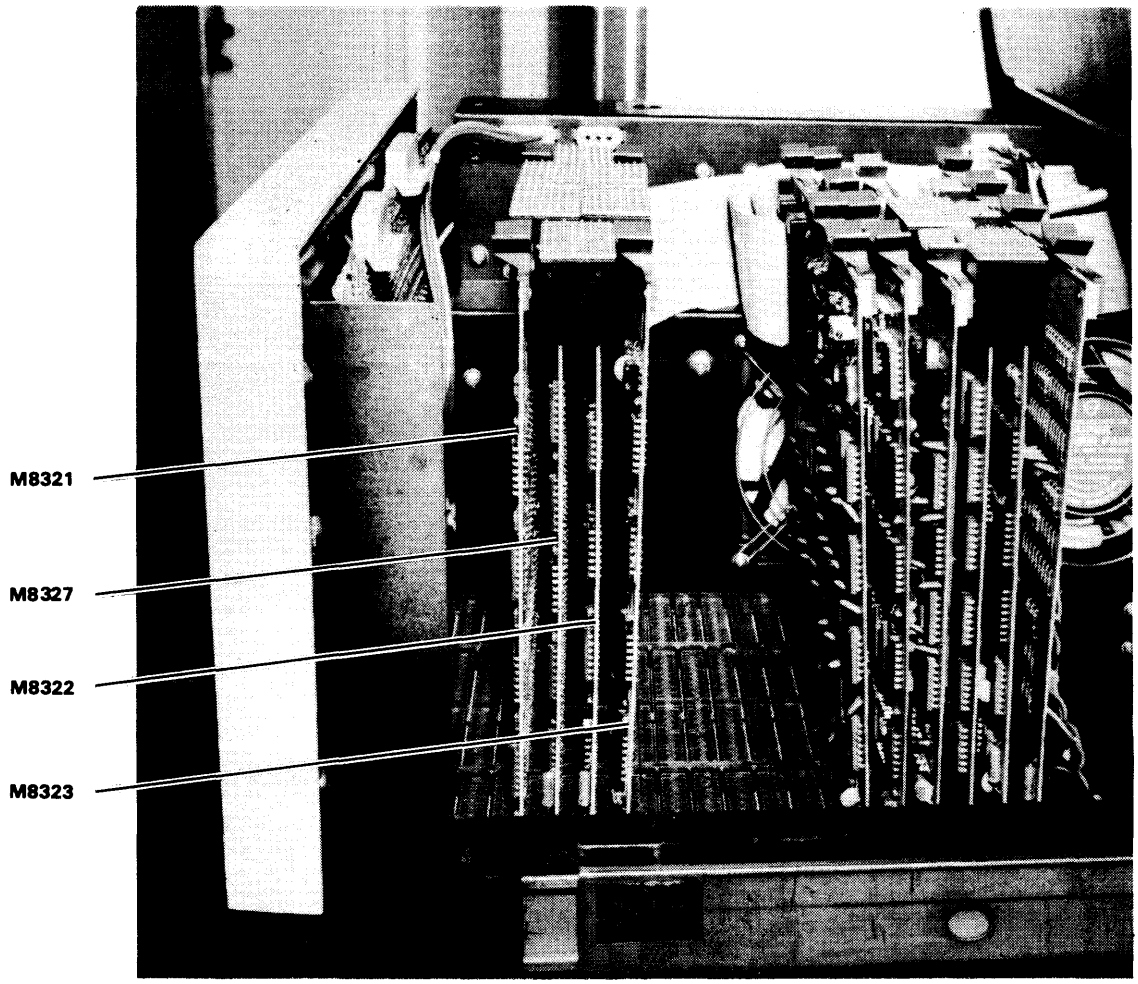


Figure 1-3 TM8-E Controller

3. Slave DECmagtape Transport – The TS03-S consists of a tape transport only. In response to inputs from the master transport adapter, it controls tape motion and records and reads data on magnetic tape. The TS03-SA requires 115 V, 60 Hz primary power and the TS03-SB requires 230 V, 50 Hz primary power.

4. Power Supply – the H720 provides switched ac and dc operating power for the TM8-M system. Two models of the power supply are available: the H720-E, which requires 115 V primary power and the H720-F, which requires 230 V primary power.

1.3 TM8-M FUNCTIONAL BLOCK DIAGRAM DESCRIPTION (Figure 1-4)

The TM8-E Controller interfaces the PDP-8 with the TS03-M Tape Transport. Bits MD0 to MD11 are transferred from the Omnibus to the data mux and register. In the Write 9-Channel Mode the output from the mux/register is DB4 to DB11, which passes through the data select logic and becomes WD0 to WD7. In the write Core – Dump Mode the data mux and register outputs data in two cycles: DB0 to DB5 in the first cycle and DB6 to DB11 in the second cycle. The data select logic outputs two 6-bit data cycles using channels WD0 to WD5. Channels WD6 and WD7 are not used in the Core Dump Mode.

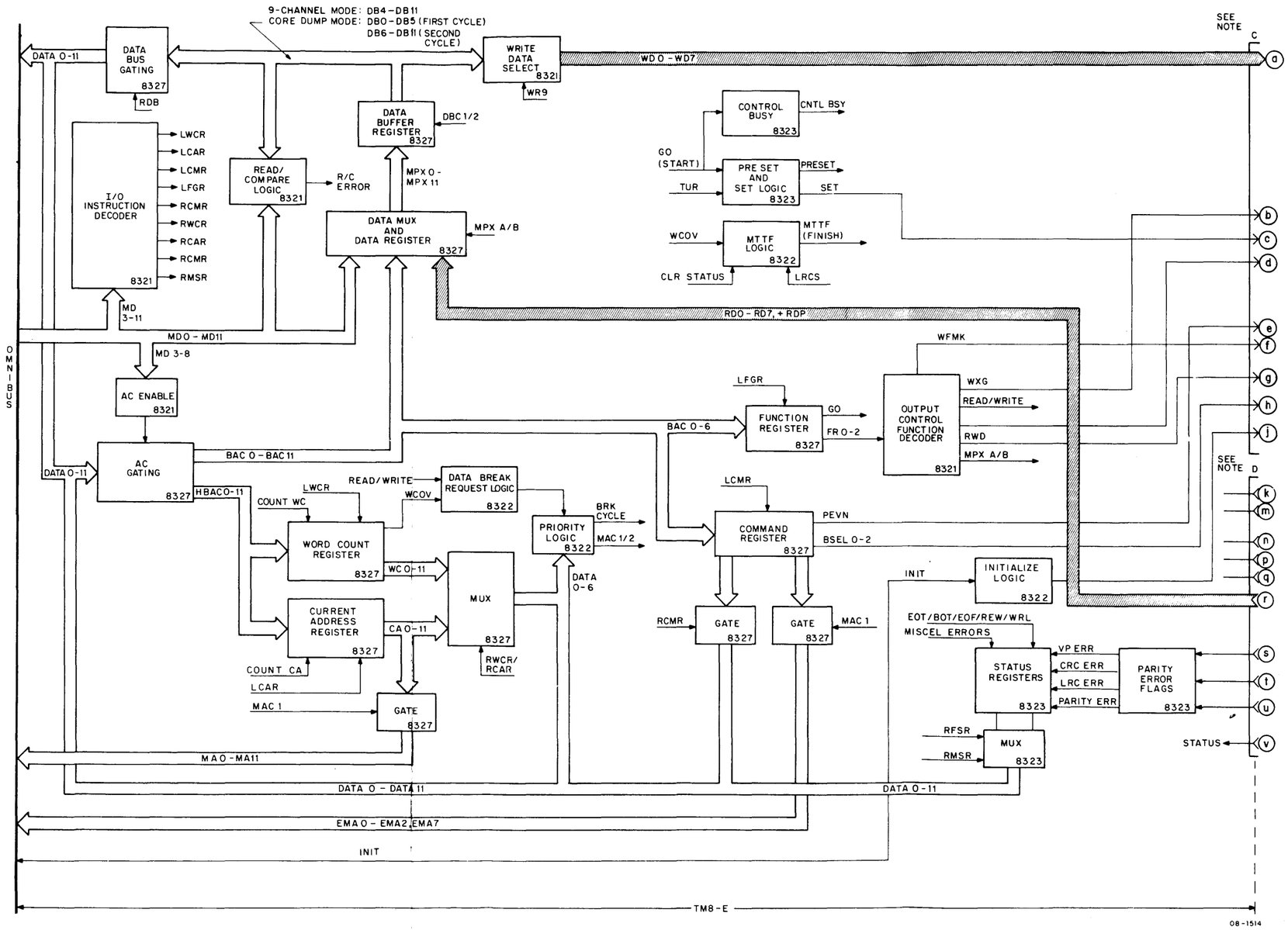


Figure 1-4 TM8-M Functional Block Diagram
(Sheet 1 of 2)

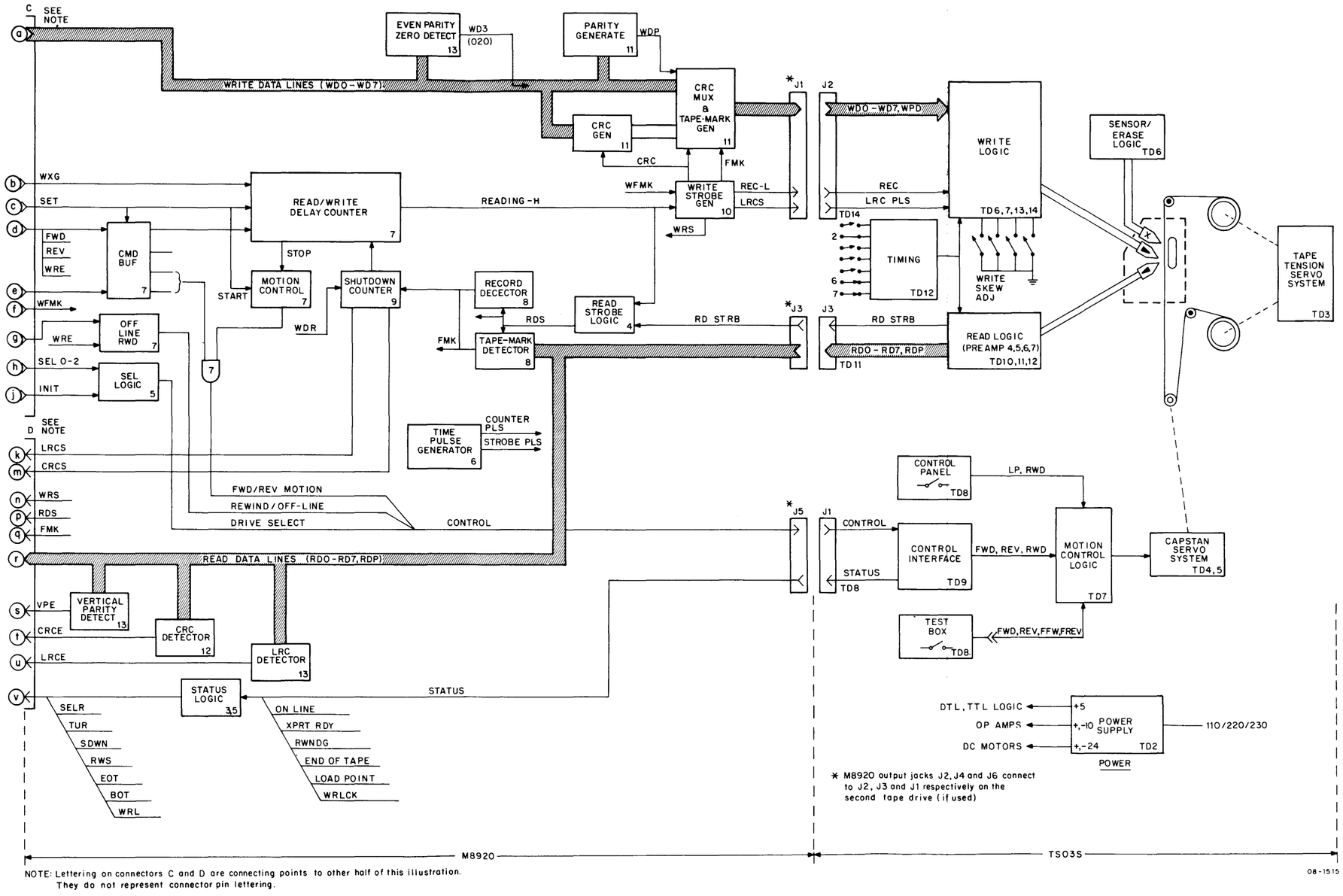


Figure 1-4 TM8-M Functional Block Diagram (Sheet 2 of 2)

Write data lines WD0 to WD7 are fed into the M8920 adapter where parity and CRC are generated. The write logic amplifies the eight data channels plus the parity channel (six data channels plus parity in Core Dump Mode) and drives the transport write heads. Write (REC) pulses and LRC pulses are obtained from the write strobe generator in the M8920 adapter.

The read logic receives data from the read heads and sends it to the M8920 adapter where the data is checked for LRC, CRC and vertical parity errors. Any such errors will raise error flags in the TM8-E and set appropriate error bits in the status register. The contents of the status register are sent to the processor via the Data Bus. In addition, the data bits are monitored for tape marks which signify an end-of-file condition.

In the Read 9-Channel Mode of operation, read channels RD0 to RD7 carry eight data bits and RDP carries a parity bit into the data mux and register in the TM8-E. From there, the bits are sent to the data lines of the Omnibus via the data bus gating logic. In the Read Core – Dump Mode, data is read from the tape in two cycles. During the first cycle, RD0 to RD5 carry six bits to the data register where they are held until the second cycle. During the second cycle, six more bits are added to the first cycle bits in the data register which then outputs 12 bits over the data lines to the Omnibus.

Detailed operation of the TM8-E and the TS03-M is given in Parts II and III of this manual. Figure 1-4 can be used along with the detailed illustrations contained therein.

1.4 APPLICABLE DOCUMENTS

Table 1-1 lists PDP-8 documents that are applicable to the TM8-M DECmagtape System.

Table 1-1
Applicable Documents

Title	Number	Description
H720 Power Supply and Mounting Box Manual	EK-H720-TM-003	A theory manual that provides a functional and detailed circuit description of the H720 Power Supply.
PDP-8 Processor and Systems Manuals.	*	A series of maintenance and theory manuals that provide a detailed description of the basic PDP-8 System.
PDP-8 Processor Handbook	†	A general handbook that discusses system architecture, addressing modes, the instruction set, programming techniques, and software.
PDP-8/E, F, M External Bus Options; Maintenance Manual Volume 3	DEC-8E-HMM3A-C-D	A handbook devoted to a discussion of the various peripherals used with PDP-8 systems. It also provides detailed theory, flow, and logic descriptions of the Omnibus and external device logic; methods of interface construction; and examples of typical interfaces.
PDP-8/A Miniprocessor Users Manual	EK-8A002-MM-001	Contains the necessary information to operate, interface to, maintain and troubleshoot the PDP-8/A.

*Applicable manuals are furnished with the system at time of installation. The document number depends upon the specific PDP-8 family processor.

†Use the processor handbook unique to the actual CPU.

1.5 MAGNETIC TAPE FUNDAMENTALS - DEFINITIONS

1. Reference Edge - The edge of the tape as defined by Figure 1-5. For tape loaded on a TS03, the reference edge is toward the observer.

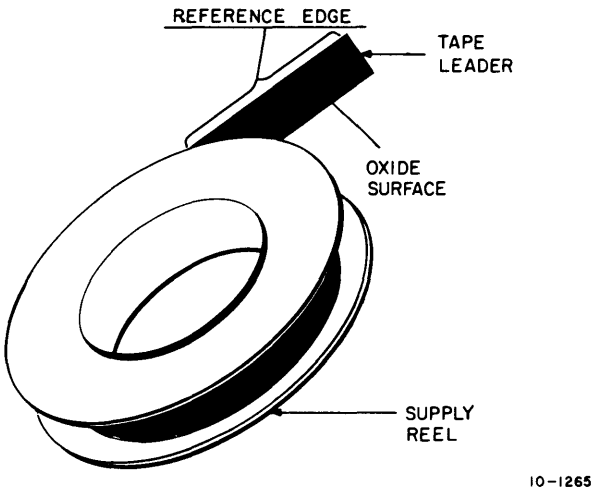


Figure 1-5 Reference Edge of Tape

2. BOT (Beginning-of-Tape) Marker - A reflective strip placed on the nonoxide side of the tape, against the reference edge, 15 ft (±1 ft) (457 cm, ±30.5 cm) from the beginning of the tape.

3. EOT (End-of-Tape) Marker - A reflective strip placed on the nonoxide side of the tape, against the nonreference edge, 25 to 30 ft (762 to 914 cm) from the trailing edge of the tape.

4. 9-Channel Recording - Eight tracks of data plus one track of vertical parity. Figure 1-6 shows the relationship between track and bit weight for a 9-channel transport.*

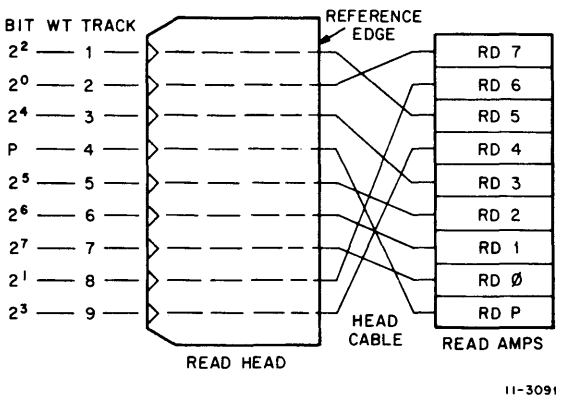


Figure 1-6 Track-Bit Weight Relationship for Nine-Channel Transport

*When the track vs bit channel standard was adopted, the outer tracks were more susceptible to bit dropping errors. Consequently, channels containing the least 1s were assigned the outer locations on the tape.

5. Tape Character - A bit recorded in each of the nine channels.

6. Record - A series of consecutive tape characters.*

7. File - An undefined number of records (minimum = zero, no maximum).

8. Interrecord Gap (IRG) - A length of erased tape used to separate records (0.5 in. (1.27 cm) minimum for 9-track; maximum IRG is 25 ft)(762 cm).

9. Extended IRG - A length of erased tape (3 in. (7.62 cm) minimum) optionally used to separate records. It must be used between BOT and the first record.

10. Tape Speed - The speed at which tape moves past the read/write heads; normally stated in inches per second.

11. Tape Density - The density of sequential characters on the tape. It is normally specified in bytes per inch (bpi), which is equivalent to characters per inch.

12. Write Enable Ring - A rubber ring which must be inserted on the supply reel to allow the transport to write on the particular tape. This safety feature helps prevent accidental destruction of previously recorded data.

13. Tape Mark (TM) - A record written on the tape to designate the end of a file; sometimes referred to as a file mark (FMK). *In the TM8-M, the tape mark is always preceded by an extended IRG.*

1.6 RECORDING METHODS AND DECmagtape FORMATS

The DECmagtape system is an on-line mass storage system for programs or data. Data is recorded on tape in vertical rows termed characters. Each character consists of eight data bits and one vertical parity bit. The vertical parity bit is program-selected as even or odd. The odd parity bit guarantees that each character records at least one 1-bit.

The parity bit is generated according to the rule that the number of 1s in a character (parity bit included) is odd or even. For example, if odd parity is used and the character contains an even number of 1 bits, the parity bit is generated as a 1 bit and an odd number of 1 bits are recorded; then, if an even number of bits are read back from tape, a vertical parity error is generated to notify the program that the data is in error.

The data characters are recorded in blocks of characters termed records (Figure 1-7). Each record contains a specified number of characters determined by the word count. The minimum record length is 3 characters; the minimum word count is the 2's complement of 3 or 7775_8. If a write operation is attempted for a record with less than 3 characters, the controller's response is undefined (i.e., the operation may be successful or unsuccessful depending on the data pattern. If the operation is unsuccessful the tape drive will run away and refuse to accept further commands until halted by a clear command.)

Records are separated by interrecord gaps (IRGs). The IRG is 0.5 in. (1.27 cm) minimum (approximately 0.6 in. (1.5 cm) in normal operation), but may be extended to 3 in. (7.62 cm) by performing an extended gap operation. Tape IRGs (unrecorded areas) provide areas on the tape for the transport to start or stop and also separate data records.

*In the TM8-M System a record must be $\geq$3 characters long to be recognized as such.

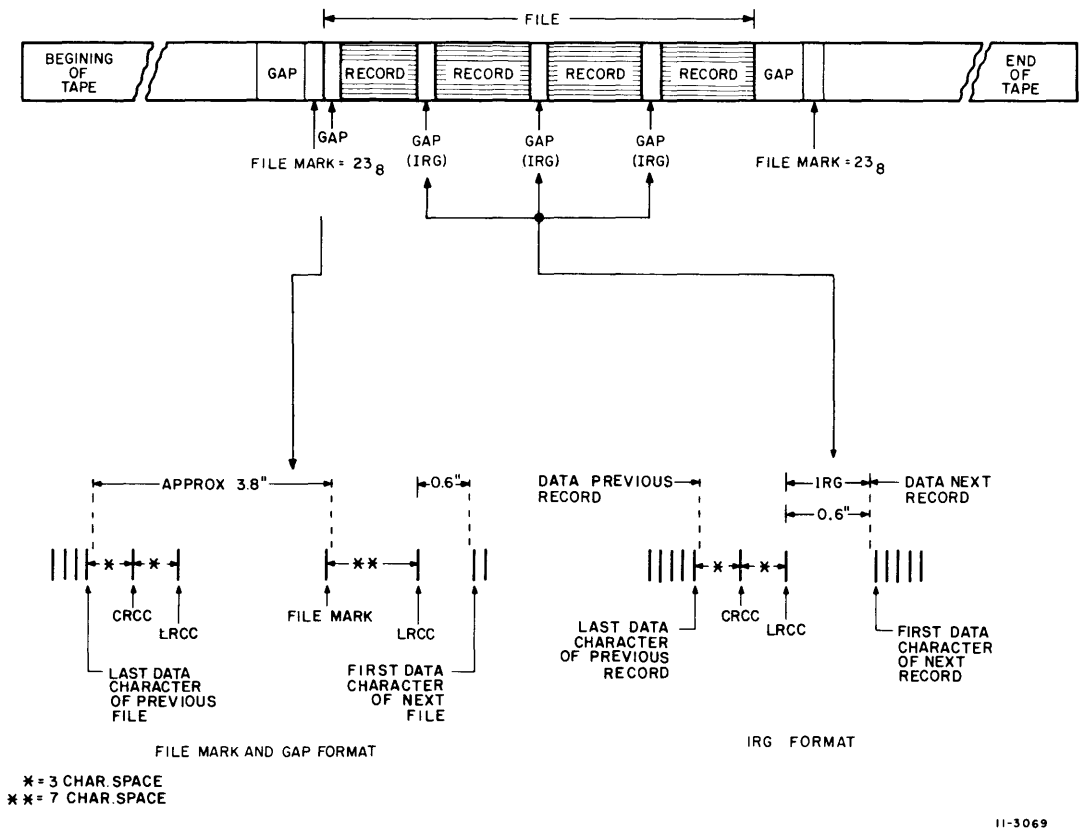


Figure 1-7 Data Recording Scheme

1.6.1 NRZI Recording Method

The TS03 employs the NRZI (non-return-to-zero change on one) recording method. In the NRZI method, a 1 bit is represented by a reversal in the direction of tape magnetization on a track; a 0 bit is represented by no change in tape magnetization.

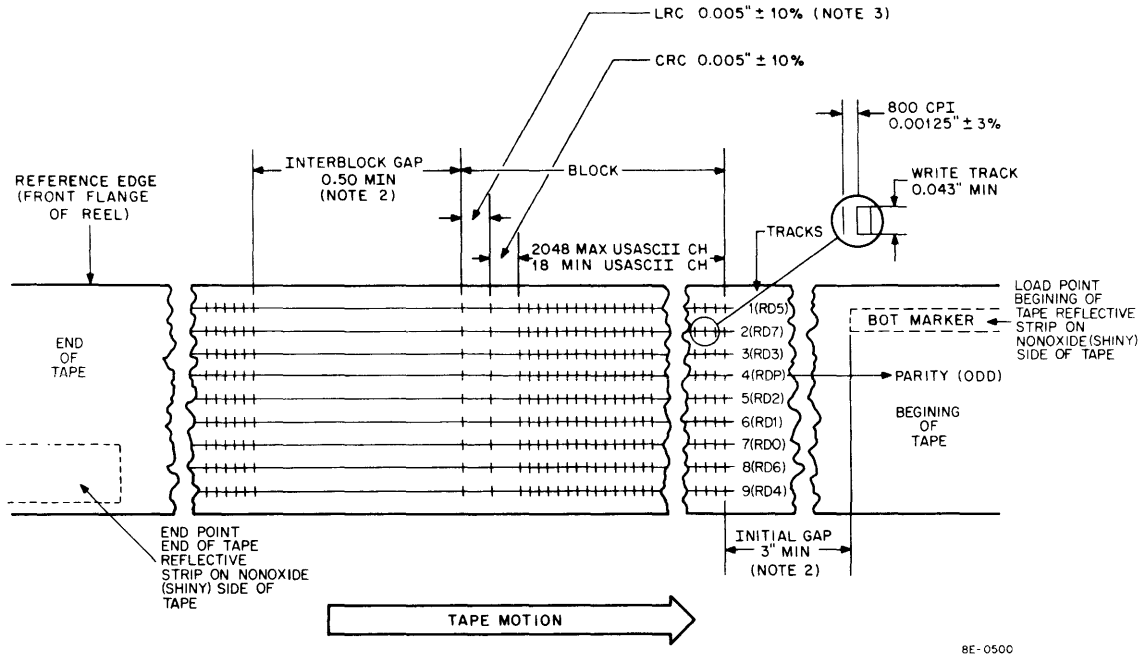
1.6.2 Tape Format

The format (Figure 1-8) is composed of from 18* to 2048 nine-bit characters spaced 1/800 in. (3 mm) apart, followed by 3 character spaces, a CRC character, 3 more spaces and an LRC character. This unit of data is called a record. At 800 characters per inch, the record is between 1/32 in. (79 mm) (minimum) and 5 in. (12.7 cm) (maximum). Between each record is a gap of at least 1/2 in.** The tape structure consists of a number of records followed by a file mark (Figure 1-7). Since data is recorded and read at high speed, IRGs are used to provide space for starting and stopping the TS03 transports. The TS03 transport accelerates from standstill to full speed in approximately 0.2 in. (0.5 cm) of tape and decelerates from full speed to standstill in 0.2 in. (0.5 cm) of tape; thus, the minimum IRG of 0.5 in. (1.27 cm) provides adequate space for starting and stopping the tape transport.

The CRC character (Paragraph 1.6.3) is generated in the TS03 master logic during a write operation and written at the end of a record. The check character performs the same function to a record as the parity bit does to a character.

*USASCII program standards, not a hardware limit.

**0.5 in. (1.27 cm) minimum; 0.6 in. (1.5 cm) nominal.



LEGEND:

BPI Tape Bits per Inch
BOT Beginning of Tape
LRC Longitudinal Redundancy Check
CRC Cyclic Redundancy Check

NOTES:

1. Tape is shown with oxide side up, read/write head on same side as oxide. Tape shown representing 1 bits in all NRZI recording; 1 bit produced by reversal of flux polarity, tape fully saturated in each direction.

2. Tape to be fully saturated in the erased direction in the interrecord gap and the initial gap.

3. An LRC bit is written in any track if the longitudinal count in that track is odd. Character parity is ignored in the LRC character.

4. CRC – Parity of CRC character is odd if an even number of data characters are written, and even if an odd number of characters are written.

Figure 1-8 Tape Format

The LRC is the final character in the record and is generated so that for each track the sum of 1 bits (CRC character included) is even. The LRC character is written on tape by clearing the write buffer in the tape transport after the CRC character is written. The LRC strobe resets the write buffer, causing a 1 to be written on each track containing an odd number of 1s; a 0 is written on each track containing an even number of 1s.

1.6.3 Cyclic Redundancy Check (CRC) Characters

The CRC character provides a method of error detection and correction on TS03 DECmagtape Transports. The code has nine check bits that form a check character at the end of each record. To perform a correction, a record in which an error has been detected must be reread into memory with the LRC and CRC characters for program evaluation. Errors involving more than one track can be detected but not corrected.

The CRC character is generated as follows:

1. The CRC register, located in the TS03, is cleared at the beginning of each record. As each data bit is written on tape, it is exclusively-ORed with its corresponding bit in the CRC register.

2. The CRC register is shifted one position to the right after the exclusive-OR operation has taken place.

3. The bits entering CRC 2, CRC 3, CRC 4, and CRC 5 of the CRC register are inverted if the bit entering CRCP is a 1. Data is shown in Table 1-2; the resultant CRC character is shown in Table 1-3.

Table 1-2
Five-Character Record

Bit	Characters				
	Data Character 0	Data Character 2	Data Character 3	Data Character 4	Data Character 5
P	0	0	1	0	1
0	1	0	0	1	0
1	0	1	0	1	0
2	0	1	0	1	1
3	1	0	1	1	0
4	0	1	1	0	1
5	0	1	1	0	1
6	1	0	1	0	1
7	0	1	0	1	0

Table 1-3
CRCC In Register When Writing

CRC Bits	CRC Cleared	CRC Register				Final CRC	CRCC On Tape
		Character 1	Character 2	Character 3	Character 4		
CRCP	0	0	0	0	1	1	0
CRC0	0	0	0	1	0	0	1
CRC1	0	1	0	0	0	0	1
CRC2	0	0	0	0	0	1	1
CRC3	0	0	1	0	0	0	1
CRC4	0	1	0	0	0	1	1
CRC5	0	0	0	1	1	0	1
CRC6	0	0	1	1	1	0	1
CRC7	0	1	0	0	1	0	1

4. Steps 1–3 are repeated for each data character of record.

5. At CRC time, all positions of the CRC register, except CRC 2 and CRC 4, are complemented and the resultant CRC character is written on tape.

6. The CRC register is cleared for the next record.

1.6.4 Longitudinal Redundancy Check (LRC) Character

The LRC character is written three spaces after the CRC character. The vertical parity bit is always written on the LRC character; the vertical parity of LRC is never checked. The LRC character makes the longitudinal parity even for the entire record, including the CRC. The LRC is generated in the TS03 by the LRC register in the following manner:

1. The LRC register is cleared at the beginning of a record.

2. As characters are written on tape, corresponding 1 bits complement the LRC register at the time data is written on tape.

3. At LRC time, the LRC strobe clears the write buffer and 1s are written on tape in only those channels for which the write buffer is set prior to clearing.

4. Following this method, the LRC character forces an even number of bits to be recorded on each track of the tape. The CRC character is included in determining the LRC character.

1.6.5 Data Files

As previously stated, a record is a group of characters preceded by an IRG and terminated by three spaces, a CRC character, three more spaces and an LRC character. A file is a group of records separated by IRGs and terminated by a 3 in. (7.62 cm) gap followed by a file mark. The file mark is a record consisting of a single data character [the end-of-file (EOF) character] followed by seven blank characters and an LRC character. The CRC character is not written on an EOF record. The LRC character with a file mark is a duplicate of the EOF character (23_8).

1.6.6 Track Assignments

The track assignments for read, write, and parity bits are shown in Table 1-4.

Table 1-4
TS03 Track Assignments for Data and Parity

Transport Track Number	Write Data Bits	Read Data Bits	Binary Weight
1 furthest from transport	WD5	RD5	2^2
2	WD7	RD7	2^0
3	WD3	RD3	2^4
4	WDP	RDP	-
5	WD2	RD2	2^5
6	WD1	RD1	2^6
7	WD0	RD0	2^7
8	WD6	RD6	2^1
9 closest to transport	WD4	RD4	2^3

1.7 SPECIFICATIONS

Main Specifications

Storage medium	1/2-in. (1.27 cm) wide magnetic tape (industry compatible)
Capacity/tape reel	5 million characters
Data transfer speed	10,000 char/sec
Drives/control, max.	2

Data Organization

Number of tracks	9
Recording density	800 bpi
Inter-record gap	0.5 in. min. (1.27 cm)
Recording method	NRZI

Tape Motion

Read/write speed	12-1/2 in./sec
Rewind time	1 minute, max.
Tape drive	single capstan
Reel braking	dynamic servo control
Speed variation	3% instantaneous; 1% long term
Start/stop distance	0.19 in. (0.48 cm)
Start/stop time	30 msec

Tape Characteristics

Length	600 ft (182.9 m)
Type	Mylar base, iron-oxide coated
Reel diameter	7 in. (17.8 cm)

Mechanical

Tape drive, mounting	Mounts on slides in a std 19-in. (48.3 cm) cabinet
Tape drive, size	10-1/2 in. (26.7 cm) panel height, 17-in. (43 cm) deep
Tape drive, weight	37 lb. (16.7 kg)
Control unit, PDP-11	Panel mounted, 5-1/4 in. (13.3 cm) high
Control unit, PDP-8	Mounts in the computer assembly

Power

Input Current	1 A at 90 to 132 Vac, or 0.5 A at 180 to 240 Vac
Heat dissipation	100 W

Environmental

Operating temperature	15° C to 32° C
Relative humidity	20% to 80%, with max wet bulb 25° C and min dew point 2° C
Altitude	10,000 ft (3,048 m)

Miscellaneous

BOT, EOT detection	Photoelectric sensing of reflective strip, industry compatible
Magnetic head	Dual gap, read after write, 0.15-in. (0.4 cm) gap

Models

TM8-MA	Tape drive and PDP-8 control, 115 Vac, 60 Hz
TM8-MB	Tape drive and PDP-8 control, 230 Vac, 50 Hz
TS03-MA	Master tape drive, 115 Vac, 60 Hz
TS03-MB	Master tape drive, 230 Vac, 50 Hz
TS03-SA	Slave tape drive, 115 Vac, 60 Hz
TS03-SB	Slave tape drive, 230 Vac, 50 Hz

CHAPTER 2
INSTALLATION

2.1 SITE PLANNING AND CONSIDERATIONS

2.1.1 Space Requirements
Figure 2-1 illustrates the space and service clearances required. Adequate space must be provided to slide the equipment out of the rack for servicing and to open the front door on the TS03 DECmagtape Transport.

2.1.2 Power Requirements
The TM8-M DECmagtape System can be operated from a nominal 115 or 230 Vac, 50/60 Hz power source. Line voltage should be maintained to within 10 percent of the nominal value and the frequency should not vary more than 3 Hz. Ensure that primary power is compatible with the H720 Power Supply.

2.1.3 Environmental Requirements
The operating environment should have cool, well filtered, humidified air, a temperature range of 15° to 27° C, and relative humidity of 40 to 60 percent.

2.2 UNPACKING
The TM8-M may be shipped in two different configurations: with the system installed in an equipment rack or with each device packaged separately.

2.2.1 Cabinet Unpacking Instructions
To unpack the cabinet, proceed as follows:

1. Remove outer shipping container.

NOTE

The container may be either heavy corrugated cardboard or plywood. In either case, remove all metal straps first, then remove any fasteners and cleats securing the container to the skid. If applicable, remove wood framing and supports from around the cabinet perimeter

2. Remove the polyethylene cover from the cabinet.

3. Unbolt cabinet(s) from the shipping skid. The bolts are located on the lower supporting side rails, and are exposed by opening the access door(s). Remove the bolts.

4. Raise the leveling feet above the level of the roll-around casters.

5. Use wood blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinet onto the floor.

6. Roll the system to the proper location for installation.

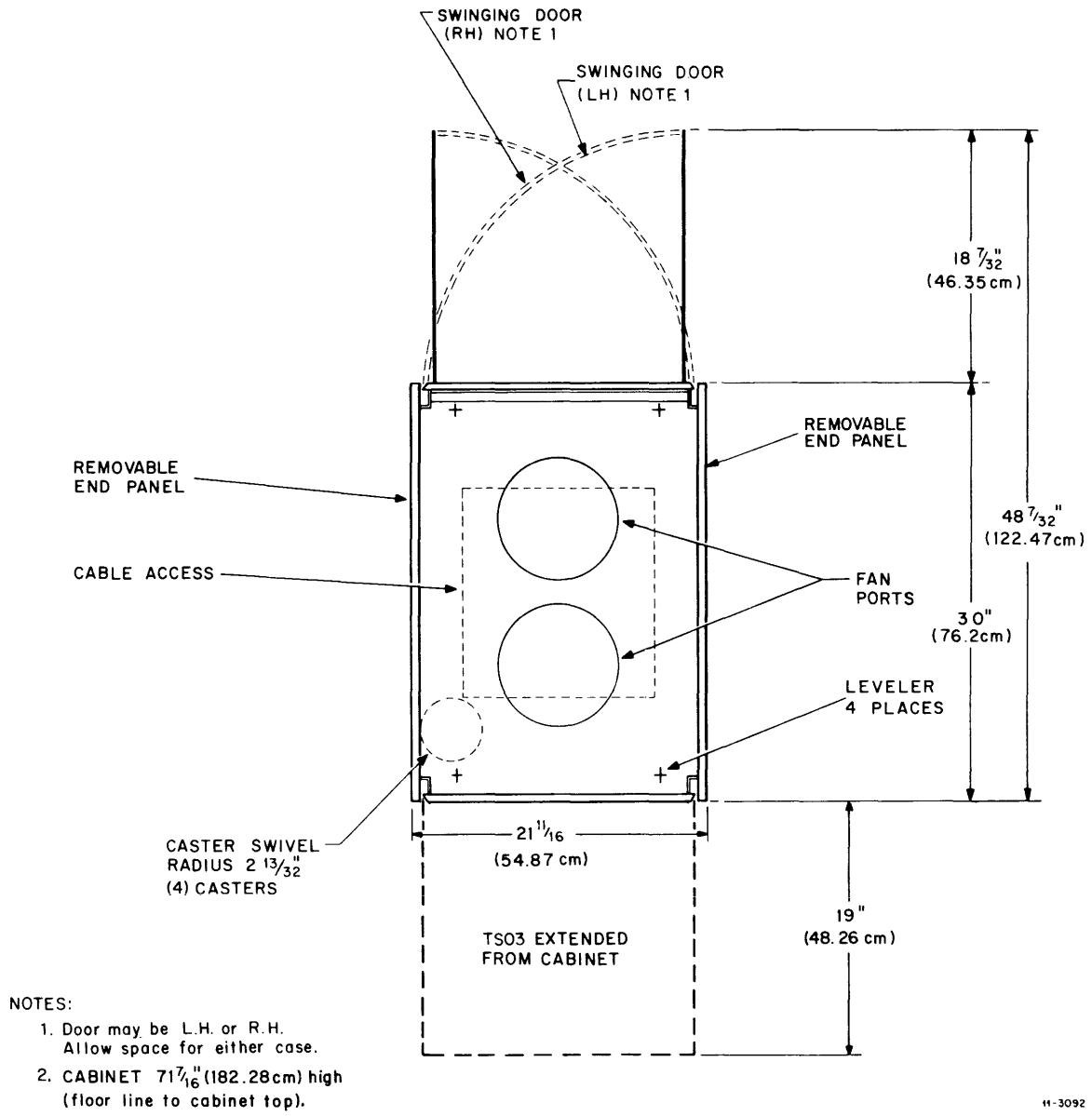


Figure 2-1 Space and Service Clearance, Top View

2.2.2 Device Unpacking Instructions

Before unpacking the equipment, check the shipping list to ensure that the correct number of packages have been received. Check the shipping list for the correct TM8-E module types. Carefully remove each device from its shipping carton. Note that the side mounts are already attached to the TS03 transport(s) and the mounting hardware is packed in a bag in each shipping carton.

2.3 INSPECTION

After removing the equipment from its container(s), inspect it and report any damage to the responsible shipper and the local DIGITAL Sales Office. Inspect as follows:

1. Inspect all switches, indicators, and panels for damage.
2. Remove equipment covers where necessary and inspect for loose or broken modules, blower or fan damage, cable damage, and loose nuts, bolts, screws, etc.
3. Inspect wiring side of logic panels for bent pins, broken wires, loose external components, and foreign material.
4. Check TS03 transport(s) for any foreign material that may have lodged in the tension arm, reel hubs, and other moving parts.
5. Check power supply for proper seating of fuses and power connectors.
6. Inspect each TM8-E module for shipping damage.

2.4 INSTALLATION

2.4.1 Cabinet Installation

If the equipment is already mounted in the cabinet, proceed as follows:

1. Lower the leveling feet so that the cabinet is resting on the floor, not on the roll-around casters.
2. Use a spirit level to level the cabinet; ensure that all leveling feet are firmly on the floor.
3. Remove the shipping screws which secure the equipment to the cabinet.
4. Plug the H720 Power Supply ac power cord into a receptacle having the correct voltage and frequency.

2.4.2 Device Installation

The equipment should be mounted in a 19 in. by 20 in. (48.3 cm by 50.8 cm) equipment bay. Figure 2-2 shows a recommended cabinet layout. The equipment should be mounted from the top down.

2.4.2.1 TS03 Mounting Instructions – To mount the TS03, proceed as follows.

NOTE

If two TS03 transports (master and slave) are to be installed, the slave (the unit without the M8920 adapter module) is installed at the uppermost position.

1. Remove the outer portions of the guides from the TS03 chassis by actuating the slide releases and mount the guides to the cabinet in the 19th hole from the top of the cabinet using the eight screws provided. Ensure that the guides are level and parallel to each other.
2. Lift the TS03 up and slide it carefully into the guides until the slide releases lock.

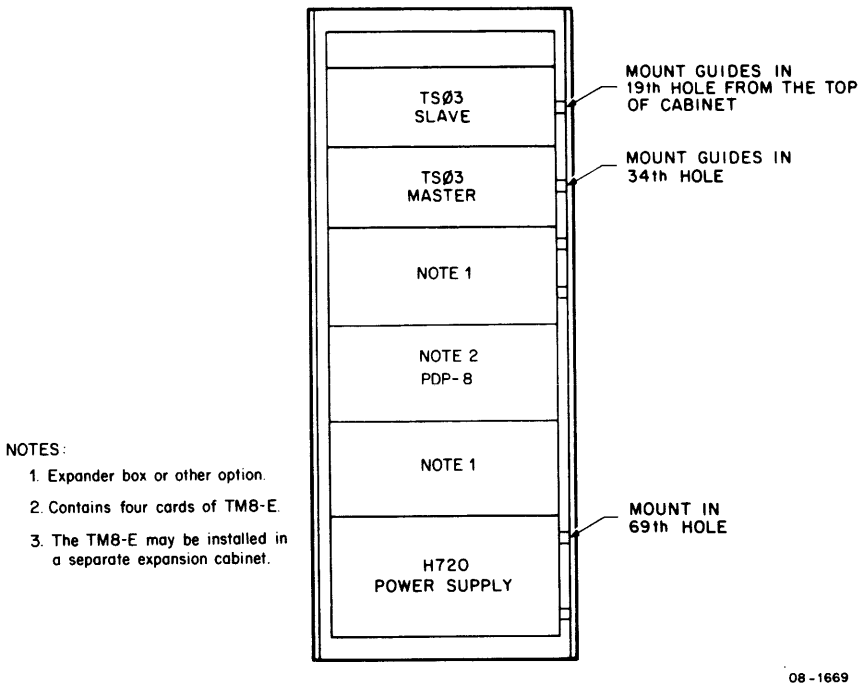


Figure 2-2 Cabinet Installation

3. Carefully lift the slide releases and push the transport fully into the cabinet.

4. If a second TS03 transport is to be installed, repeat steps 1 through 3 above, but mount the guides in the 34th hole.

2.4.2.2 TM8-E Controller Mounting Instructions – Perform the following procedure to install the four TM8-E modules:

1. Ensure that power is removed from the PDP-8 and the TS03(s).

2. If the TM8-E and the TS03 are installed in more than one cabinet, ensure that the cabinets are tied to the same ground or install a ground wire between the cabinets.

3. Ensure that the TM8-E module jumpers are correctly installed to select the priority assigned to the TM8-E. (See "Data Break Priority Logic" in Chapter 9 of Part II of this manual.)

4. Insert the TM8-E modules into the Omnibus in the order shown in Figure 2-3.

CAUTION

The modules must not be installed upside down. The +5 V, 0.01 μF capacitors should be at the bottom (next to the Omnibus) on all modules installed on the Omnibus.

5. Install six H851 edge connectors between the four modules as shown in Figure 2-5. The interconnections are made via connectors E, F, H and J as shown in Figure 2-5 and on Signal Mapping Drawing TM8-E-2.

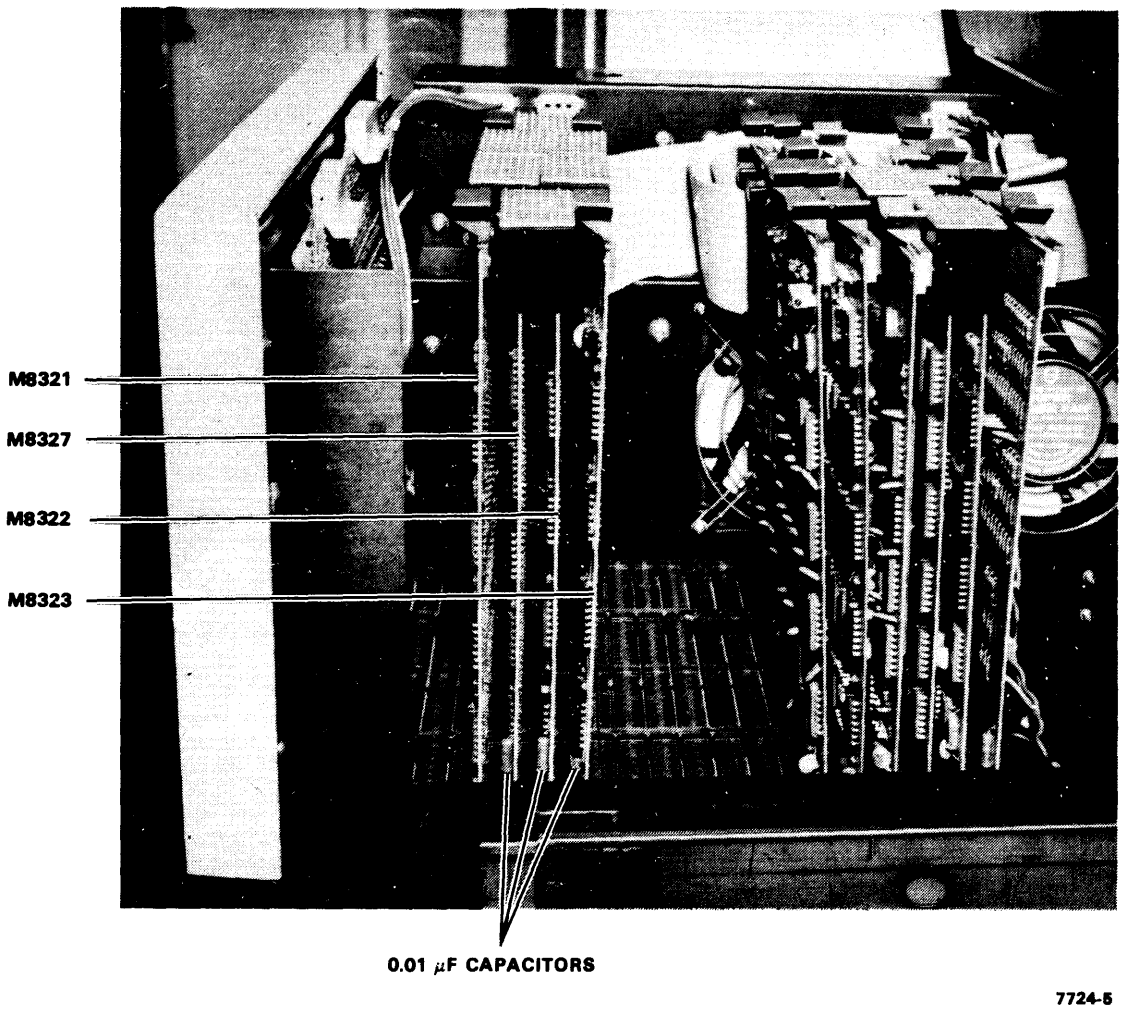


Figure 2-3 TM8-E Module Orientation

2.4.2.3 H720 Power Supply Mounting Instructions – Using the hardware provided, mount the H720 Power Supply in the cabinet at the 69th hole position.

2.4.3 I/O Signal Cable Connections

To install the I/O signal cables, perform the following steps.

1. Check both 7011571 cables to ensure that the jumpers shown in Figure 2-4 are installed.*

*The 7011571 cable is a modified BC08L cable. The modification consists of connecting the cable ground plane to M8920 output ground (pins T1 and C2) on the paddle card.

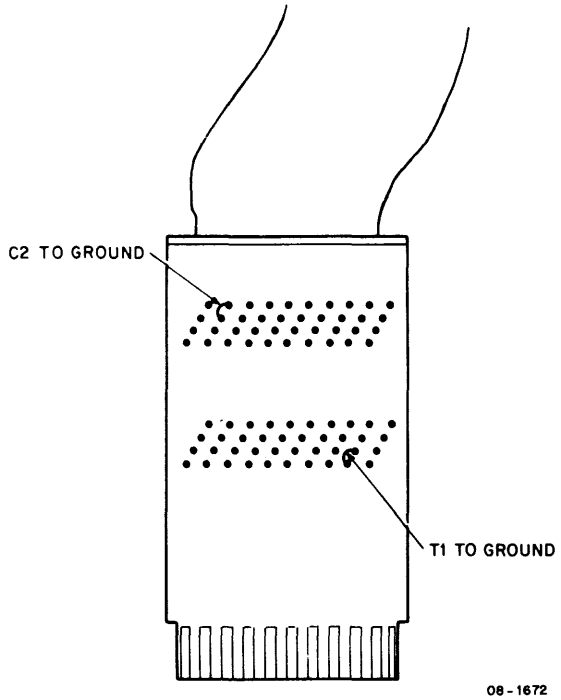


Figure 2-4 Paddle Board Jumpers on Side 2
of Cable Assembly 7011571

2. Connect the two 40-pin connectors (P1 and P2) of one of the 7011571 cables to J1 and J2 respectively on the M8321 module. The rough side of the cable faces the module. Connector P2 extends out beyond P1 and connects to the inner jack (J2) on the module. (See Figure 2-5.)

NOTE

The two ribbon cables that make up a 7011571 cable assembly are the same length. The position of the cable ends on the paddle board causes one of the cable plugs (P2) to extend out beyond the other (P1) at the other end of the cable assembly. (See Figure 2-6.)

3. Tag the paddle board end of the cable as connecting to M8321.

4. Connect the two 40-pin connectors (P1 and P2) of the other 7011571 cable to J1 and J2 respectively on the M8323 module. The rough side of the cable faces the module. Connector P2 extends out beyond P1 and connects to the inner jack (J2) on the module.

5. Slide out the TS03-M drawer. Unscrew the two knurled screws holding the M8920 module and allow the module to hang down as shown in Figure 2-7.

6. Connect the cable from the M8321 module to the "C" connector on the M8920 module and connect the cable from the M8323 module to the "D" connector of the M8920 module using the two H870 edge connectors.

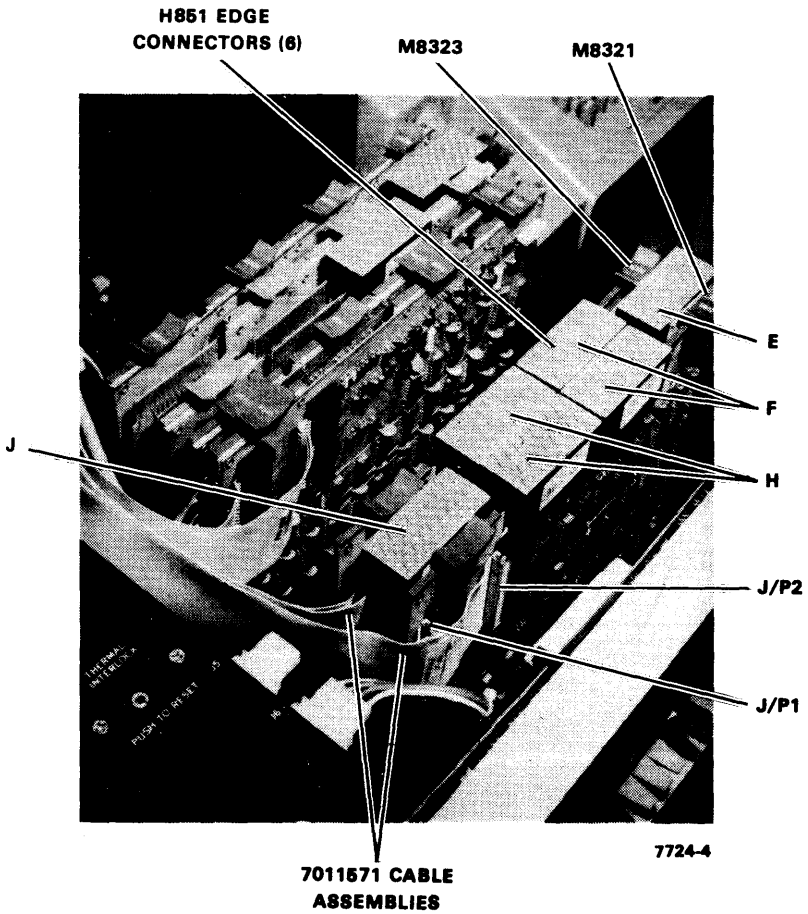


Figure 2-5 TM8-E Controller Cabling

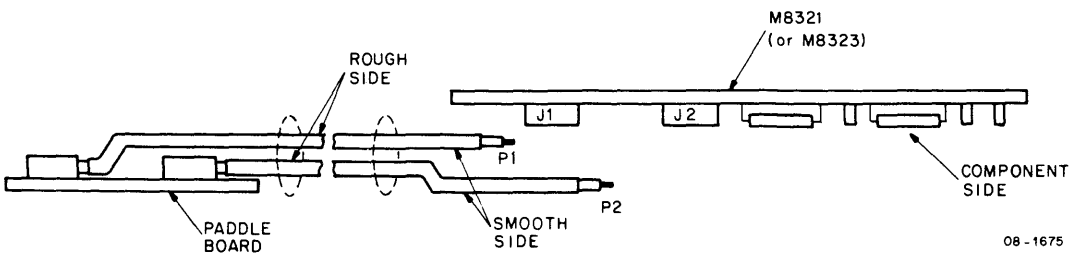


Figure 2-6 7011571 Cable Assembly

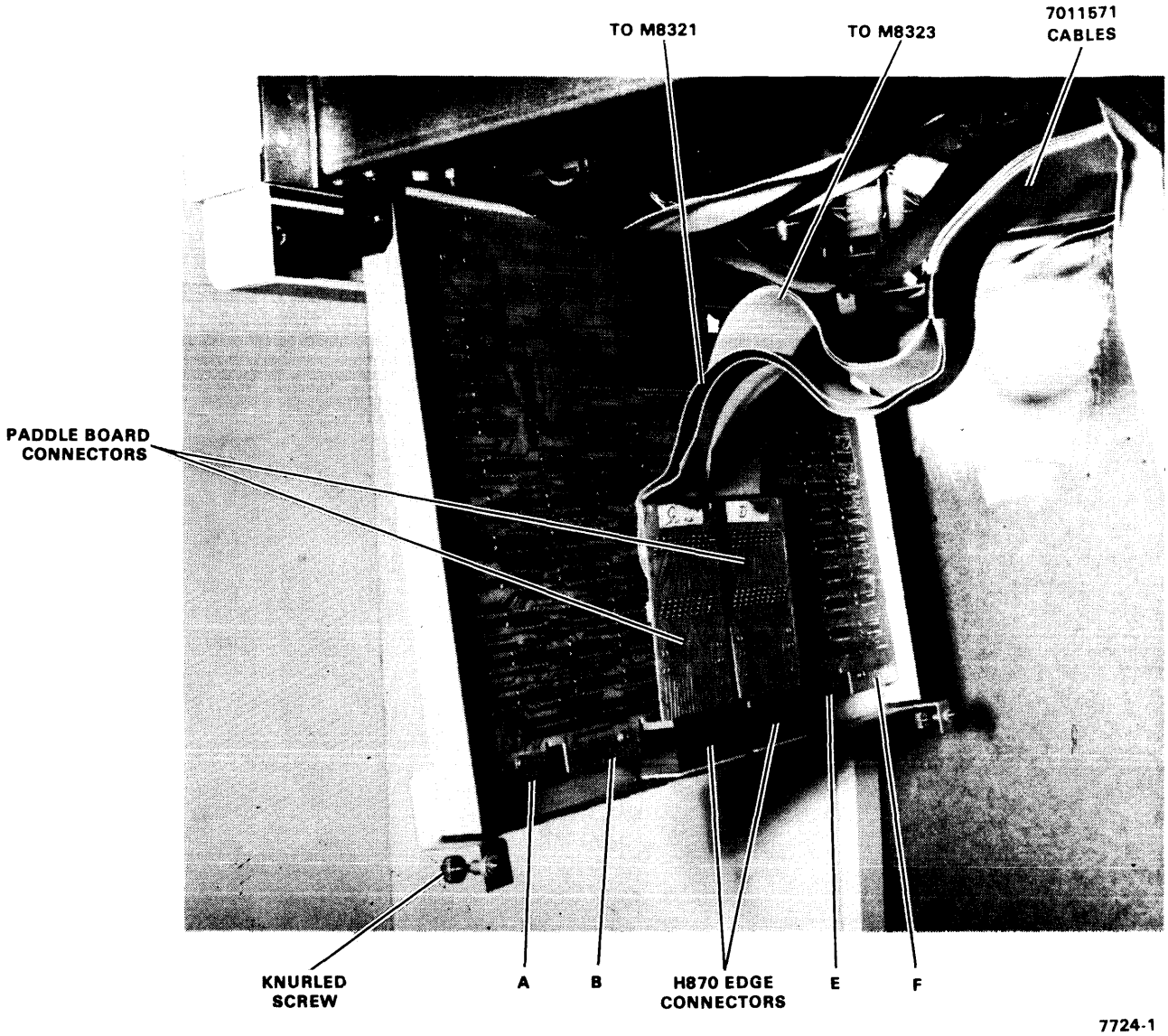


Figure 2-7 M8920 Cabling to TM8-E

7. Remove one screw from the center cable strain relief and loosen the other. (See Figure 2-8.)

8. Swing the strain relief out and place the two 7011571 cables up against the edge of the chassis. Leave enough slack so that the cables are not strained when the M8920 module is swung down.

9. Swing the top of the strain relief back into place. Insert the removed screw and tighten both screws.

10. Install the 7010570 master/slave cables between the M8920 module connectors (J1 through J6) and the TS03 master and slave transport connectors as listed in Table 2-1 and shown in Figure 2-9. Use the three strain reliefs as in steps 7, 8, and 9 to secure the 7010570 cables. Tighten the two screws on each of the transport connectors.

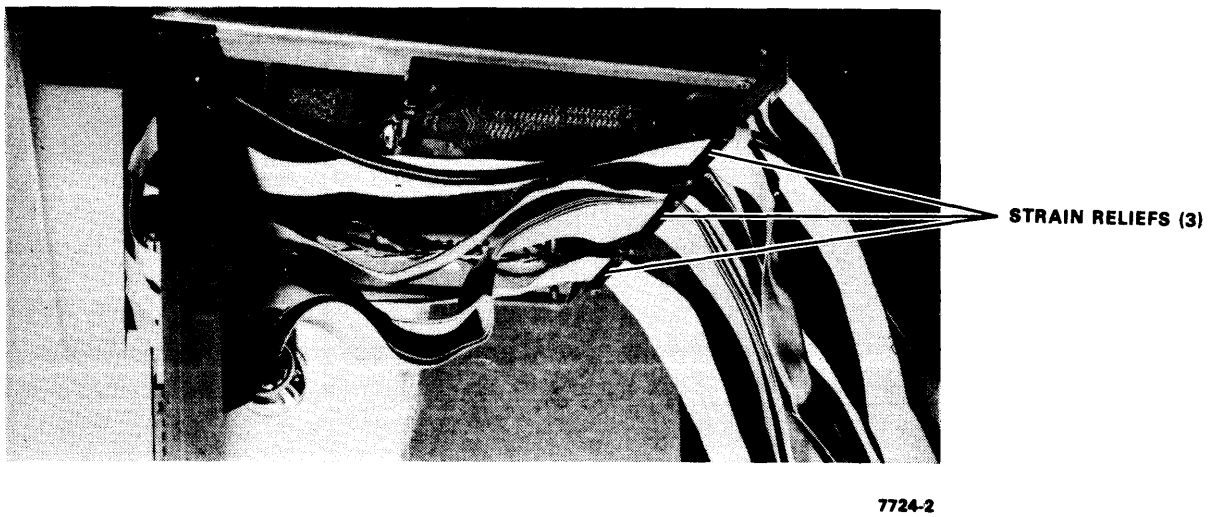


Figure 2-8 Securing TM8-M Cables

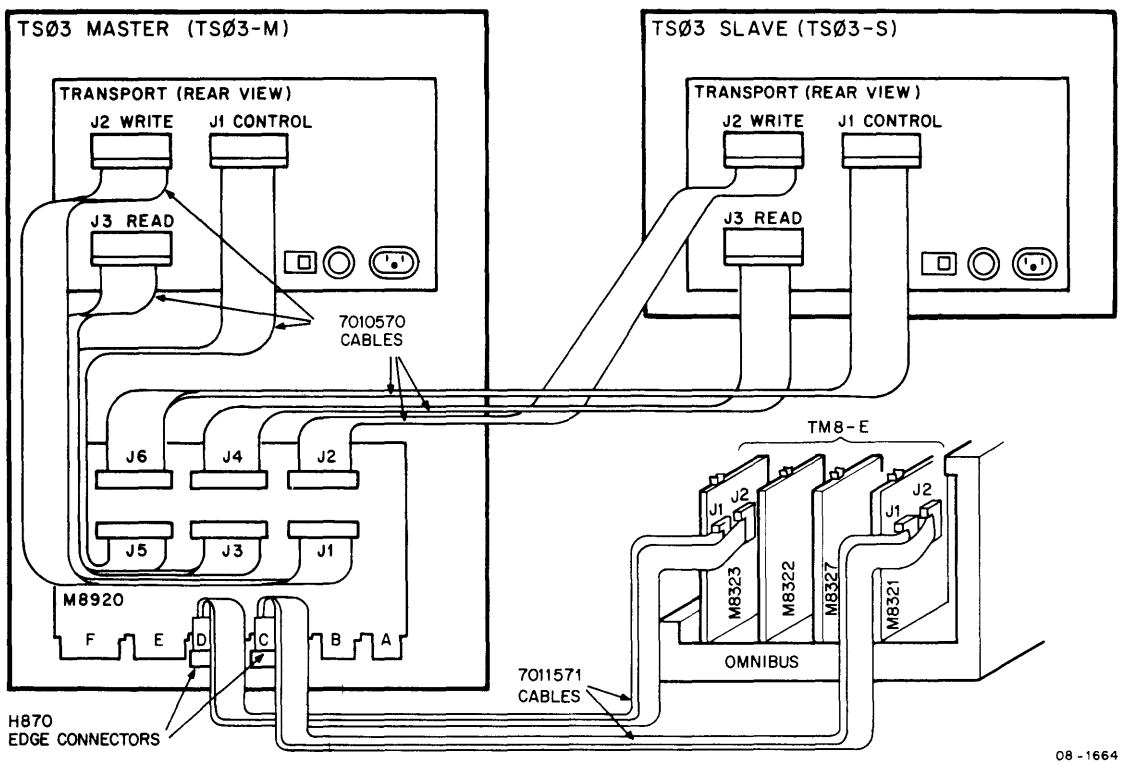


Figure 2-9 I/O Cable Connection Diagram

Table 2-1
7010570 Cable Connections

From M8920 Adapter Board Connector	To TS03 Master Connector	TS03 Slave Connector
J1	J2	
J3	J3	
J5	J1	
J2		J2
J4		J3
J6		J1

2.4.4 Power Connections

To make power connections, proceed as follows. (See Figure 2-10.)

1. Install the power harness (70-10832) between the H720 Power Supply and the M8920 adapter module in accordance with color coding listed in Table 2-2.

2. Plug the TS03 master and slave transport ac power cords into the H720 Power Supply switched receptacles.

3. Plug the H720 Power Supply power cord into the site's primary ac power outlet having the proper ac voltage and frequency. Check the label on H720 Power Supply for power requirements.

4. Using tie wraps, neatly dress all cables and harnesses. Leave service loops so TS03 drives can be extended from the cabinet and the M8920 adapter can be swung down on its hinges.

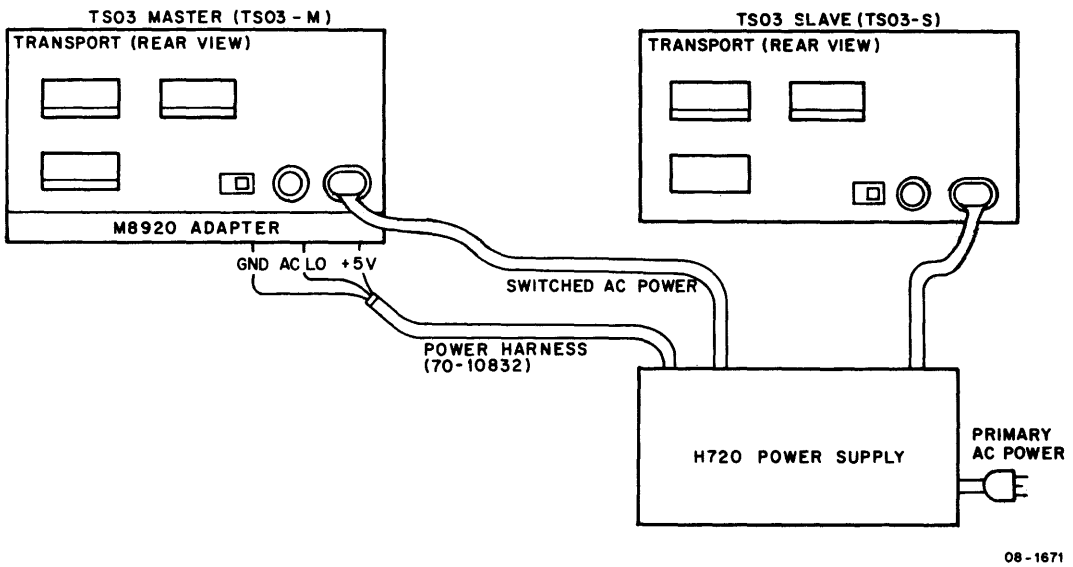


Figure 2-10 Power Connection Diagram

Table 2-2
Power Harness Color Coding

DC Voltage/Signal	Wire Color
+5 V	Red
Gnd	Black
AC LO	Yellow

2.5 ACCEPTANCE TESTING

Refer to the TM8-MA & MB/TS03 Drive System Checkout and Acceptance - WM (Engineering Drawing No. SP-TM8-M-1) for the acceptance test procedures for the TM8-M Tape Drive System.

CHAPTER 3
SYSTEM OPERATING INSTRUCTIONS

3.1 SCOPE
This chapter covers operation of the TM8-M, including a description of controls and indicators and all operating procedures.

3.2 CONTROLS AND INDICATORS
Figure 3-2 describes the controls and indicators.

3.3 OPERATING PROCEDURES

3.3.1 Tape Threading
To thread the tape on the transport, proceed as follows:

1. Raise the latch of the quick-release hub and place the tape file reel to be used on the supply hub (Figure 3-1) with the write enable ring side next to the transport deck.

2. Hold the reel flush against the hub flange and secure it by pressing the hub latch down.

3. Thread the tape along the path as shown in the threading diagram (Figure 3-1).

4. Holding the end of the tape with a finger, wrap a few turns counterclockwise around the takeup hub.

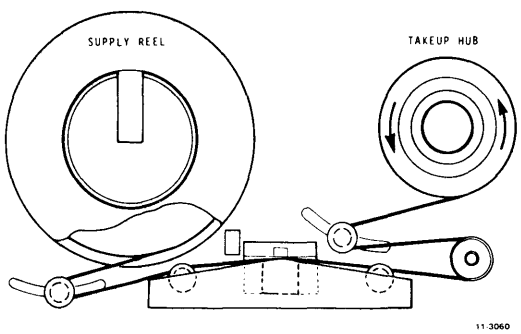
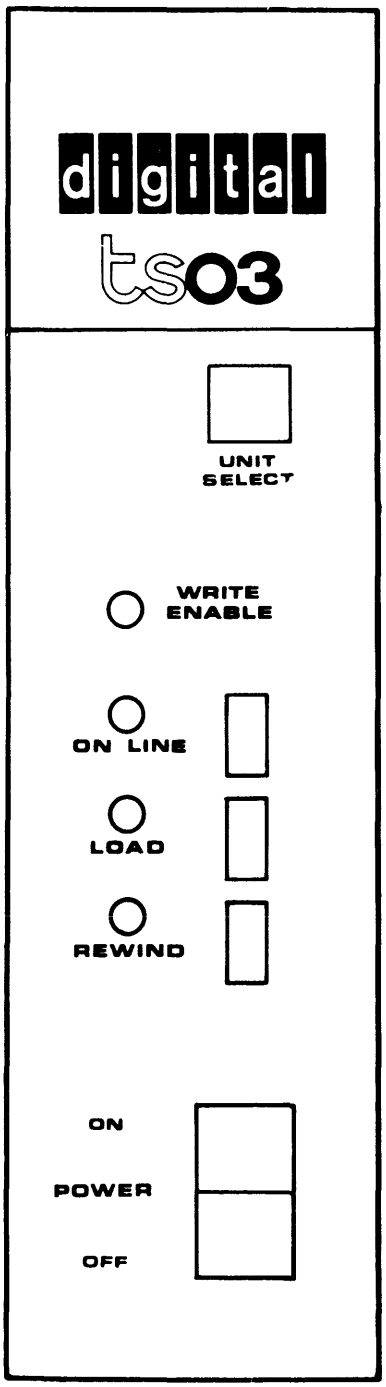


Figure 3-1 Tape Threading Diagram

3.3.2 Tape Loading
Pressing the LOAD pushbutton energizes the reel servos and initiates a load sequence. Tape advances to the load point marker and stops. If for some reason the load point marker is already past the sensor (as, for example, in restoring power after a shutdown), tape will continue to move. Under these conditions, press LOAD and then REWIND and the tape will rewind to the load point. Once pressed, the LOAD switch is illuminated and is inactive until power has been turned off or tape is removed from the machine.



UNIT SELECT Plug – One of two plugs can be inserted, designating unit as 0 or 1.

NOTE

In a single drive system, the drive is always designated as drive 0. In a dual drive system, either drive can be designated as drive 0.

WRITE ENABLE Indicator – Illuminated whenever a reel with a write enable ring is mounted on the supply hub.

ON LINE Pushbutton/Indicator – A momentary pushbutton, which functions as alternate action. When first activated, the tape unit is placed in an on-line condition; when the tape unit is on-line, it can be remotely selected and will be ready if tape is loaded to or past the load point. When activated again it takes the unit off-line. The indicator is illuminated in the on-line condition. The load function must be performed before the unit will go on-line.

LOAD Pushbutton/Indicator – The momentary pushbutton activates the reel servos (tensions tape) and starts the load sequence. The indicator is illuminated when the reel servos are activated and tape is tensioned.

REWIND Pushbutton/Indicator – The momentary pushbutton activates a rewind operation. This control is enabled only when tape is tensioned and the unit is off-line. The indicator is illuminated during either a local or a remote rewind operation.

POWER Switch – The ON/OFF switch applies ac power to the tape transport.

Figure 3-2 Controls and Indicators

3.3.3 Placing Tape Unit On-Line

After the tape is properly threaded and has been loaded and brought to the load point, press the ON LINE pushbutton and check that the ON LINE indicator illuminates. (The REWIND pushbutton is disabled when the tape unit is on-line.) On-line status enables the tape unit to be remotely selected and to perform all normal operations under remote control.

3.3.4 Tape Unloading and Rewind

Provision is made in the TS03 transport for rewinding a tape to the load point under remote control. However, this operation may also be performed manually. Proceed as follows:

1. If the ON LINE indicator is illuminated, press the ON LINE pushbutton. Check that the indicator extinguishes when pressure is removed.

2. Press the REWIND pushbutton. The tape will now rewind to the load point marker.

3. After the tape has been positioned at the load point under remote or local control, press the REWIND pushbutton to rewind the tape past the load point to the physical beginning of the tape.

NOTE

The rewind sequence cannot be stopped until the tape has rewound either to the load point or until tension is lost at the physical beginning of the tape.

3.3.5 Power Shutdown

A tape transport should not be turned off when tape is loaded and is past the load point marker. The TS03 transport is designed to prevent physical damage to the tape in the event of power failure, and to minimize operator error which could destroy recorded data. In the event of power failure during tape unit operation, manually wind the tape forward several feet before restoring power. When power has been restored, press the LOAD pushbutton, then the REWIND pushbutton. This will rewind the tape to the load point. If desired, the tape can then be advanced to the data block nearest the point at which the power failure occurred by initiating the appropriate control commands.

CAUTION

In dual drive systems, when one drive is on-line and running, *do not* turn power off at the unused drive, i.e., do not set the TS03 POWER ON/OFF switch to OFF. To do so may result in data errors on the drive that is running.

CHAPTER 4
CUSTOMER EQUIPMENT CARE AND OPERATION

4.1 SCOPE

The information contained in this chapter will assist the customer in caring for his equipment and ensure the highest level of performance and reliability.

4.2 REQUIREMENTS

The customer is directly responsible for:

1. Obtaining operating supplies, including disk cartridges, disk packs and filters, magnetic tape, DECtape, paper tape, cassettes, printer paper, printer ribbons, plotter paper, etc.

2. Supplying accessories, including disk storage racks, DECtape storage racks, carrying cases for disk cartridges and DECtape, cabinetry, tables and chairs.

NOTE

Users of Digital Equipment Corporation equipment may obtain the proper operating supplies and accessories by contacting:

Digital Equipment Corporation
DEC Supplies Order Processing
146 Main Street
Maynard, Massachusetts 01754
Phone: (617)897-5111, Ext. 5218, 5907
Boston Area: (617)890-0330
TWX: 710-347-0212
Cable: Digital Mayn
Telex: 94-8457

3. Maintaining the required logs and report files consistently and accurately.

4. Making the necessary documentation available in a location convenient to the system.

5. Keeping the exterior of the system and the surrounding area clean.

6. Turning off the teletypewriter and/or line printer when these devices are not in use.

7. Performing the specific equipment care operations described for the various devices at the suggested frequencies, or more often if usage and environment warrant.

8. Ensuring that ac plugs are securely plugged in each time equipment care operations are performed.

4.3 CARE OF MAGNETIC TAPE

1. Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head; it is imperative that the tape be kept clean.

2. Always store tape reels inside containers when not in use; keep the empty containers tightly closed to keep out dust and dirt.

3. Never touch the portion of tape between the BOT and EOT markers; oil from fingers attracts dust and dirt.

4. Never use a contaminated reel of tape; this will spread dirt to clean tape reels, and could have an adverse effect on tape transport reliability.

5. Always handle tape reels bv the hub hole; squeezing the reel flanges could lead to tape edge damage in winding or unwinding tapes.

6. Do not smoke near the tape transport or storage area; tobacco smoke and ash are especially damaging to tapes.

7. Do not place magnetic tape near any line printer or other device that produces paper dust.

8. Do not place magnetic tape on top of the tape transport, or in any other location where it might be affected by hot air.

4.4 CARE OF TS03 TAPE TRANSPORT

4.4.1 General

Digital Equipment Corporation tape transports are highly reliable precision instruments which will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability.

4.4.2 Preventive Maintenance

To ensure continuing trouble-free operation, a preventive maintenance schedule should be kept. Oniy a few items are involved, but they are very important to proper tape transport operation. The frequency of performance will vary somewhat with the environment and degree of use of the transport so a rigid schedule applying to all machines is difficult to define. The recommended periods apply to units in constant operation in ordinary environments. They should be modified if experience shows other periods are more suitable.

Before performing any cleaning operation (Table 4-1), remove the supply reel and store it properly. All items in the tape path must be cleaned on a per-shift basis. In cleaning, it is important to be thorough yet gentle and to avoid certain dangerous practices. It should be remembered that the tape cleaner is a strong cleaning agent and should not come in contact with painted surfaces or plastic.

CAUTION

Do not use: acetone or lacquer thinner; aerosol spray cans; rubbing alcohol; excessive cleaner. Be extremely careful not to allow the cleaner to penetrate ball bearings, tension rollers, and motors.

4.4.3 Materials Required

1. DECmagtape system and magtape cleaning kit

2. Lint-free wipers

Part I

Table 4-1
Customer Equipment Care Operations

Device: TS03 DECmagtape Transport

Frequency	Operation
Once per shift	1. Clean tape path according to the following procedure. (Time required = 5 min.) a. Remove tape from transport. b. Using head cleaner and lint-free cloth, clean the following (Figure 4-1): Head and head shield Load point/end-of-tape sensor Missing tape sensor Both tape guides Tape cleaner Tape tension roller (not shown) Capstan (not shown) c. Using a clean, dry, lint-free cloth or wipe, once again go over each surface listed above to dry and remove any residue. **NOTE** **Do not use any cloth or wipe that has come in contact with the tape path as it is probably contaminated.** d. Using a clean, lint-free cloth or wipe, dust the inside and outside of the plexiglass door. If dirt and dust have accumulated, a mild soap and water solution or antistatic cleaner may be used. Ensure that the door is dry before returning the tape transport to service.

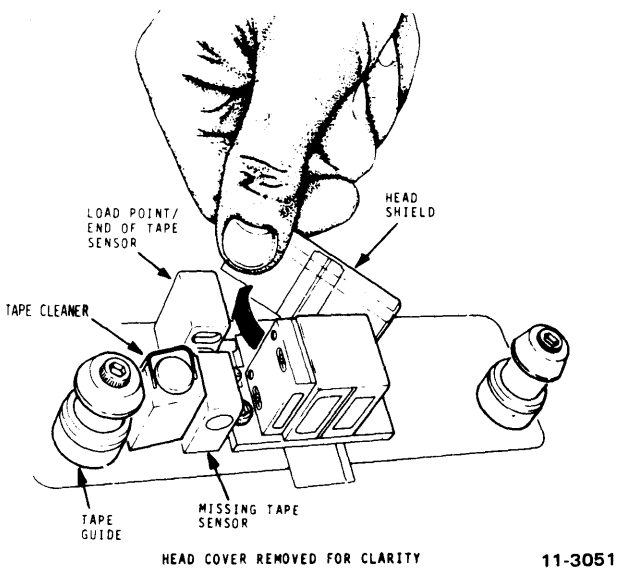


Figure 4-1 Opening Head Shield

CHAPTER 5
SYSTEM MAINTENANCE

5.1 SCOPE
This chapter provides a complete description of TM8-M preventive and corrective maintenance procedures.

5.2 MAINTENANCE PHILOSOPHY
The TM8-M DECmagtape System is highly reliable and will provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability.

The preventive maintenance required on each unit differs in accordance with its design. The TM8-E Controller, M8920 adapter, and H720 Power Supply are total solid state units with no moving parts; therefore, no preventive maintenance is required on these units. The TS03 transport, however, requires daily customer care consisting of head and tape path cleaning (Chapter 4). Otherwise, the transport requires very few adjustments and these should not be performed unless problems are encountered in transport operation. See Paragraph 5.4 for the recommended preventive maintenance procedure.

Corrective maintenance consists of troubleshooting at the system level using system diagnostics and visual observations to localize the failure to a particular unit, whether it be the TM8-E Controller, the M8920 adapter, the TS03 transport, or the H720 Power Supply. Once the faulty unit is determined, unit level troubleshooting will be performed using unit functional block diagrams, engineering flow diagrams, timing diagrams, and detail logic diagrams to localize the failure to an electrical module or mechanical part.

NOTE

In the case of the TS03 transport, troubleshooting tables are provided (see Tables 5-5, 5-6 and 5-7) listing the symptoms, possible causes, indications, and recommended actions.

Once the faulty module or mechanical part is located, it should be replaced. If the faulty part is a module, it should be returned to the depot for repair; if a mechanical part fails, it should be replaced and repaired only if the cost warrants it.

5.3 TEST EQUIPMENT
Test equipment required to maintain the TM8-M falls into two categories: standard test equipment and special test equipment.

5.3.1 Standard Test Equipment
Maintenance procedures for the TM8-M require the standard test equipment and diagnostic programs listed in Table 5-1, in addition to standard hand tools, cleaners, test cables, and probes. Table 5-2 describes the diagnostic programs.

Table 5-1
Standard Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630NA or 260
Oscilloscope	Tektronix	Type 453 or equivalent
X10 Probes (2)	Tektronix	P6008
Diagnostics (MAINDECS)	DIGITAL	MAINDEC-08-DHTSA MAINDEC-08-DHTSB MAINDEC-08-DHTSC MAINDEC-08-DHTSE MAINDEC-08-DHTSF

Table 5-2
Diagnostic Descriptions

Number	Title	Description
MAINDEC-08-DHTSA	TM8-E/TS03 Control Test, Part 1	Twelve tests to checkout the TM8-E independent of the TS03.
MAINDEC-08-DHTSB	TM8-E/TS03 Control Test, Part 2	Twelve tests to checkout the TM8-E and the TS03 together as a subsystem.
MAINDEC-08-DHTSC	TM8-E/TS03 Data Reliability 9 Track	Used to collect statistical information pertaining to the data reliability of 9-track transports used with the TM8-E.
MAINDEC-08-DHTSE	TM8-E/TS03 Drive Function Timer	Tests the TM8-E and TS03 with selected operations that are timed and the execution times are printed out.
MAINDEC-08-DHTSF	TM8-E/TS03 Utility Driver	Allows operator to perform any test in any order. Tests will operate regardless of results or errors.

5.3.2 Special Test Equipment
The special test equipment and tools required are listed in Table 5-3.

5.4 PREVENTIVE MAINTENANCE
Refer to *TS03 DECmagtape Transport Preventive Maintenance Manual,* Document No. EK-TS03-PM-001.

Table 5-3
Special Test Equipment and Tools

Equipment	Manufacturer	Part No.
Test box	DIGITAL	29-21922
Tape path alignment tool	DIGITAL	29-21904
Transport module extender	DIGITAL	29-21925
Skew tape (7 in. (7.78 cm) reel)	DIGITAL	29-22020
Scratch tape (600 ft.(182.9 cm))	DIGITAL	18-09540-00*
Scratch tape (600 ft.(182.9 cm))	DIGITAL	18-09540-02*
Magna-See® (also renew solution)	CBS	29-16871
Magnifying glass	–	29-20273
Reflective tape marker	DIGITAL	90-09177
Write ring	DIGITAL	–
Head cleaner, capstan cleaner, lint-free cloth (Kimwipes)	–	TUC01
Scotch tape (3/4 in.)	Buy Locally	–

5.5 ADJUSTMENTS

5.5.1 General

Most of the adjustments in this paragraph relate to ensuring that data is written and read perpendicular to the reference edge of the tape. Properly written data is necessary to ensure that a tape written on one machine can be read on another (compatibility). Many of the adjustment procedures utilize the test box, shown in Figures 5-1 and 5-2. A description of the test box is given in Paragraph 5.5.2.

The TS03 adjustment procedures are summarized in Figure 5-3. The sequence of the procedures is logical providing complete adjustment of the TS03 while minimizing adjustment time and tape handling. Adjustments can be performed separately and in any order, except as noted in Figure 5-3.

5.5.2 Test Box

5.5.2.1 Functions of Test Box – The test box provides:

1. An alternative motion control source bypassing the controller interface logic and the TS03 control panel logic. All combinations of speed and direction are available with BOT (LOAD POINT) and EOT interlocks to prevent running tape off of the reels.

2. A write test feature to generate an all 1s pattern for correcting write skew.

3. A skew light indicator to detect when data falls outside the skew window.

4. A choice of instantaneous and average (dynamic) skew error indication in the form of a voltage level.

5. Automatic, rapid, stop-start capability for use in ramp time adjustments.

®Magna-See is a registered trademark of Columbia Broadcasting System, Inc., Danbury, Conn.
*No. 00 is packaged in a canister. No. 02 is tape-seal package.

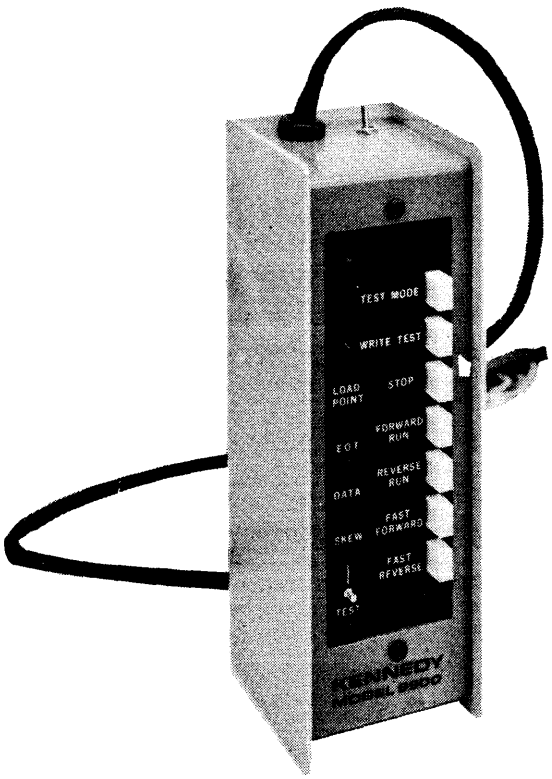


Figure 5-1 TS03 Test Box

5.5.2.2 Test Box Operation

1. Hookup - The test box is connected to the only exposed edge connector among the PC boards (slot 10). The connector is not keyed and must be installed with the RED wire (pin A) to the left and to the rear. (See Figure 5-2.)

2. Activation - To enable the test box:
   a. Drive must be OFF-LINE (TS03 Control Panel).
   b. STOP Switch must be pressed.
   c. TEST MODE must be pressed.

NOTE

Test mode is terminated by pressing the test mode switch a second time or placing the drive ON LINE pushbutton.

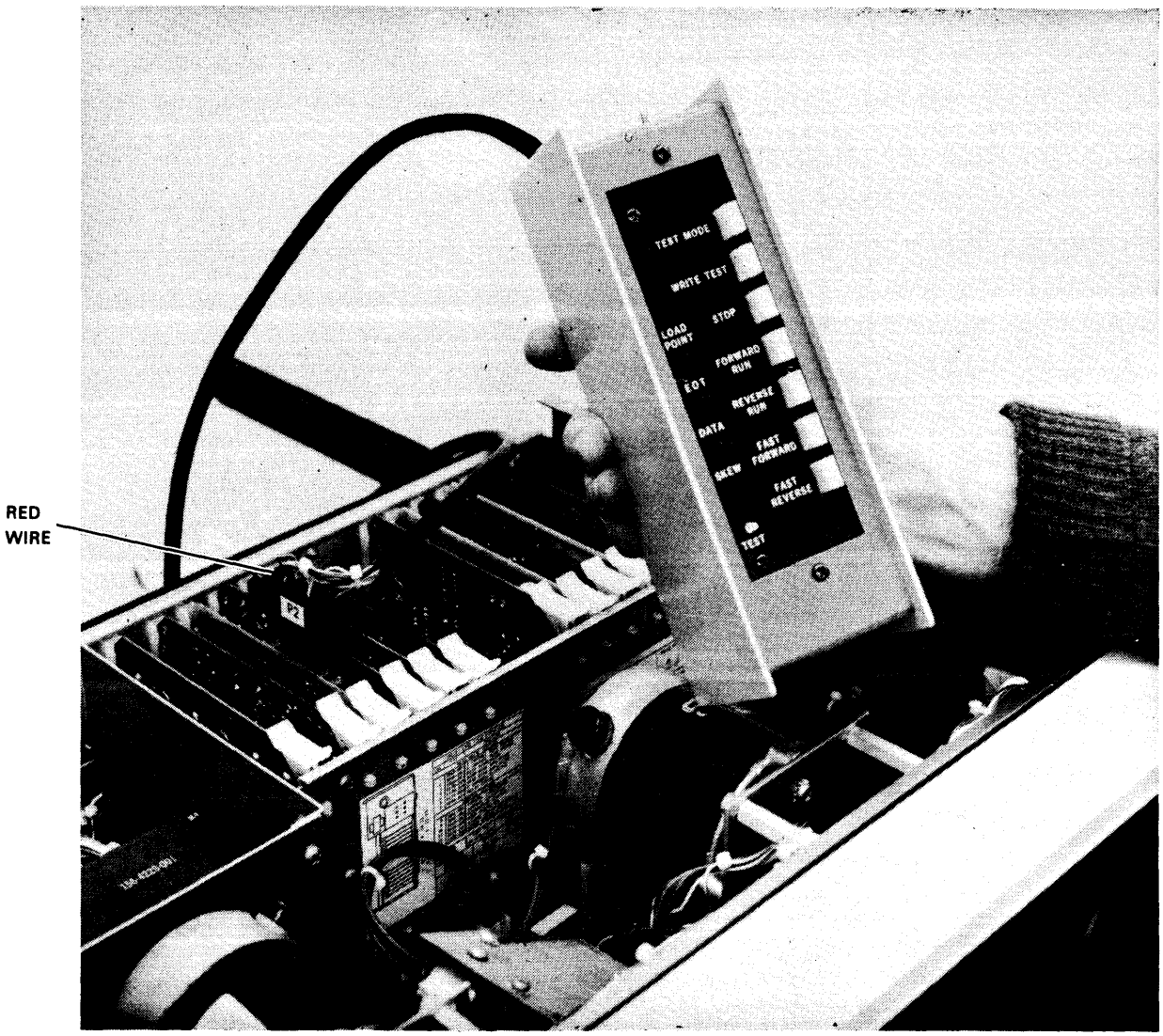


Figure 5-2 Test Box Installation

3. Motion Switches
   a. Each of the four motion switches performs its indicated function and is interlocked with the other motion switches.

   b. Motion is terminated by the STOP button or by reaching either tape sensor (BOT or EOT).

   c. Pulling the toggle switch (next to the connector cable) forward causes normal test motion to be cycled on and off at approximately 10 times per second.

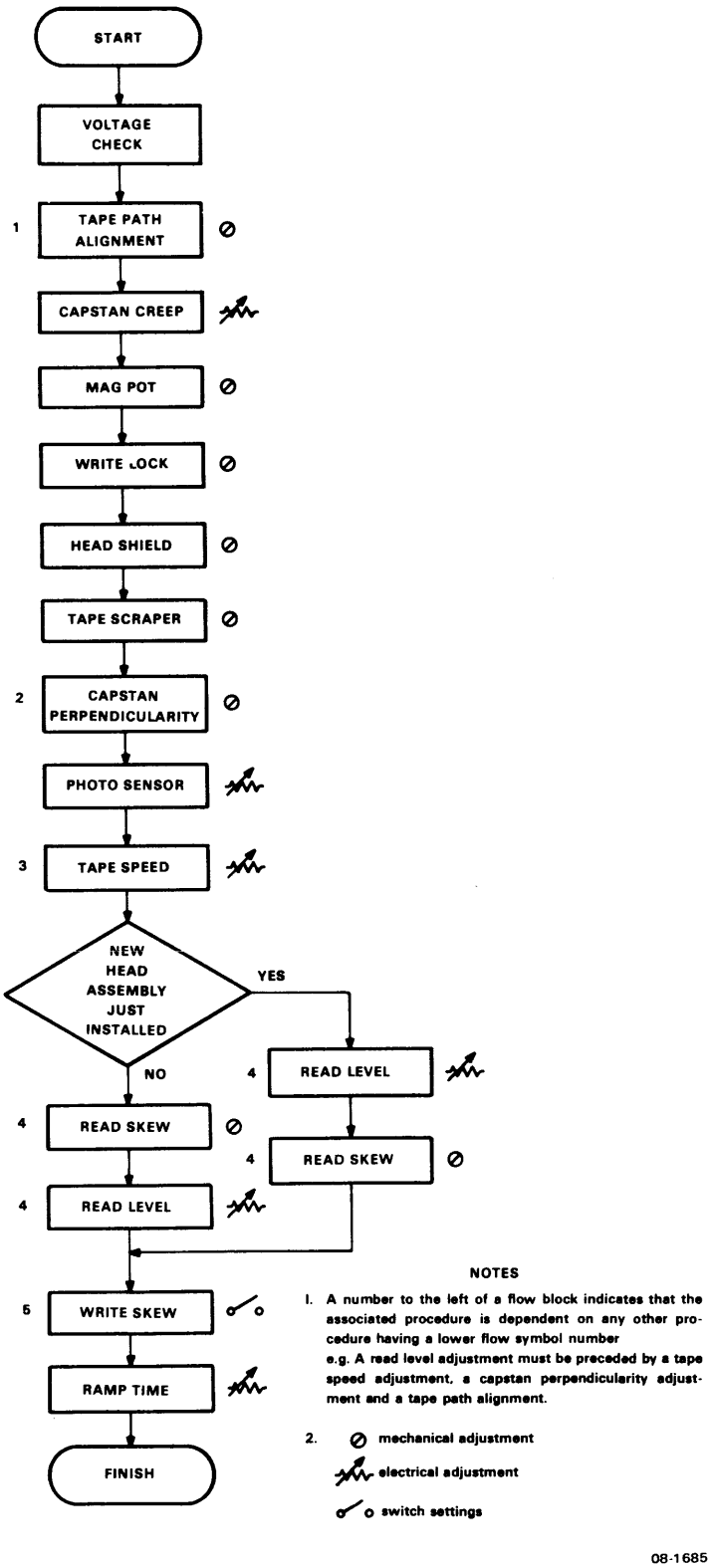


Figure 5-3 TS03 Adjustment Flowchart

4. Toggle Switch - The three-position toggle switch at the top of the test box selects instantaneous skew (middle position) or average (dynamic) skew (rear position). The forward position provides rapid (10 cps) start/stop operation.

5. Write test
   a. Must be in test mode.
   b. Operates only in Forward Run condition.

6. Indicators - All indicators operate whether in test mode or not.
   a. Test mode - Test mode is selected
   b. Write test - All 1s being written on tape.
   c. Load Point - At beginning of tape (BOT).
   d. EOT - At end of tape.
   e. DATA - Data is being read.
   f. SKEW - Data packet width exceeds skew window.
      (normal window = 16/32 in. (1.264 cm);
      read while write = 12/32 in. (0.948 cm);
      test mode = 5/32 in. (0.395 cm))

7. Test Point - Provides skew error indication in the form of a voltage level. The skew error is proportional to the measured voltage such that 1 V equals 10 μs of error.

8. Adjustments - Two calibration adjustments are associated with the skew conversion circuit. Engineering Drawing TD8 contains the information necessary for making these calibrations. Both adjustments are located inside of the Test Box.

5.5.3 Adjustment Procedures

Remove the screen covering over the PC boards and the protective cover in front of the head assembly.

CAUTION

Always remove power from the tape drive when removing a PC board.

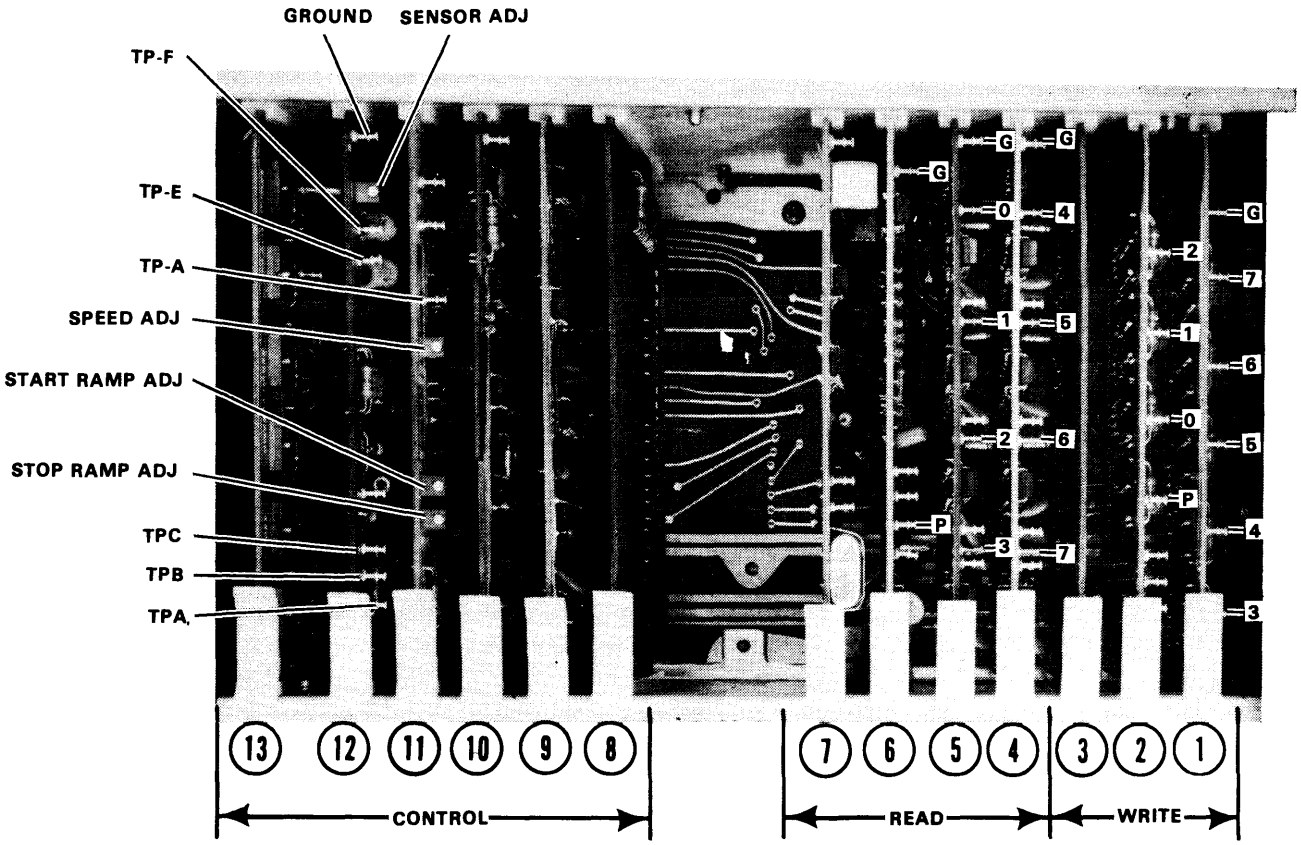
The PC boards are identified in Figure 5-4. Most adjustments and test points referred to in the procedure are found in Figure 5-4.

5.5.3.1 Voltage Check - The power supply provides ±24 Vdc (unregulated), ±10 Vdc (regulated), and +5 Vdc (regulated). These voltages are not adjustable but should be checked to verify correct operating voltages. Perform the following steps to check the operating voltages.

1. Power Switch ON.

2. Measure +24 Vdc and -24 Vdc supplies (Figure 5-5). Both supplies will measure about 26 Vdc when under light load.

3. Measure +10 Vdc, -10 Vdc, and +5 Vdc at test points A, B, and C on sensor amplifier. Voltage tolerance is ±5%.



◄X INDICATES TAPE CHANNEL NUMBER

ITEM NO.	PART NO.*	ITEM
13	4306-002	SERVO PREAMPLIFIER
12	3844-001	SENSOR AMPLIFIER/DRIVER
11	3645-002	RAMP GENERATOR
10	3843-001	TAPE MOTION CONTROL
9	3842-001	INTERFACE CONTROL
8	3841-001	CONTROL TERMINATOR
7	4845-001	TIMING DELAY
6	4179-004	P CHANNEL/CLIPPING
5	4178-004	QUAD READ AMPLIFIER
4	4178-004	QUAD READ AMPLIFIER
3	3860-001	DATA TERMINATOR
2	3848-001	4 CHANNEL HEAD DRIVER
1	3849-001	5 CHANNEL HEAD DRIVER

*Vendor part nos. See Appendix J for cross reference to DEC part nos.

Figure 5-4 Plug-In Modules and Test Point Locations

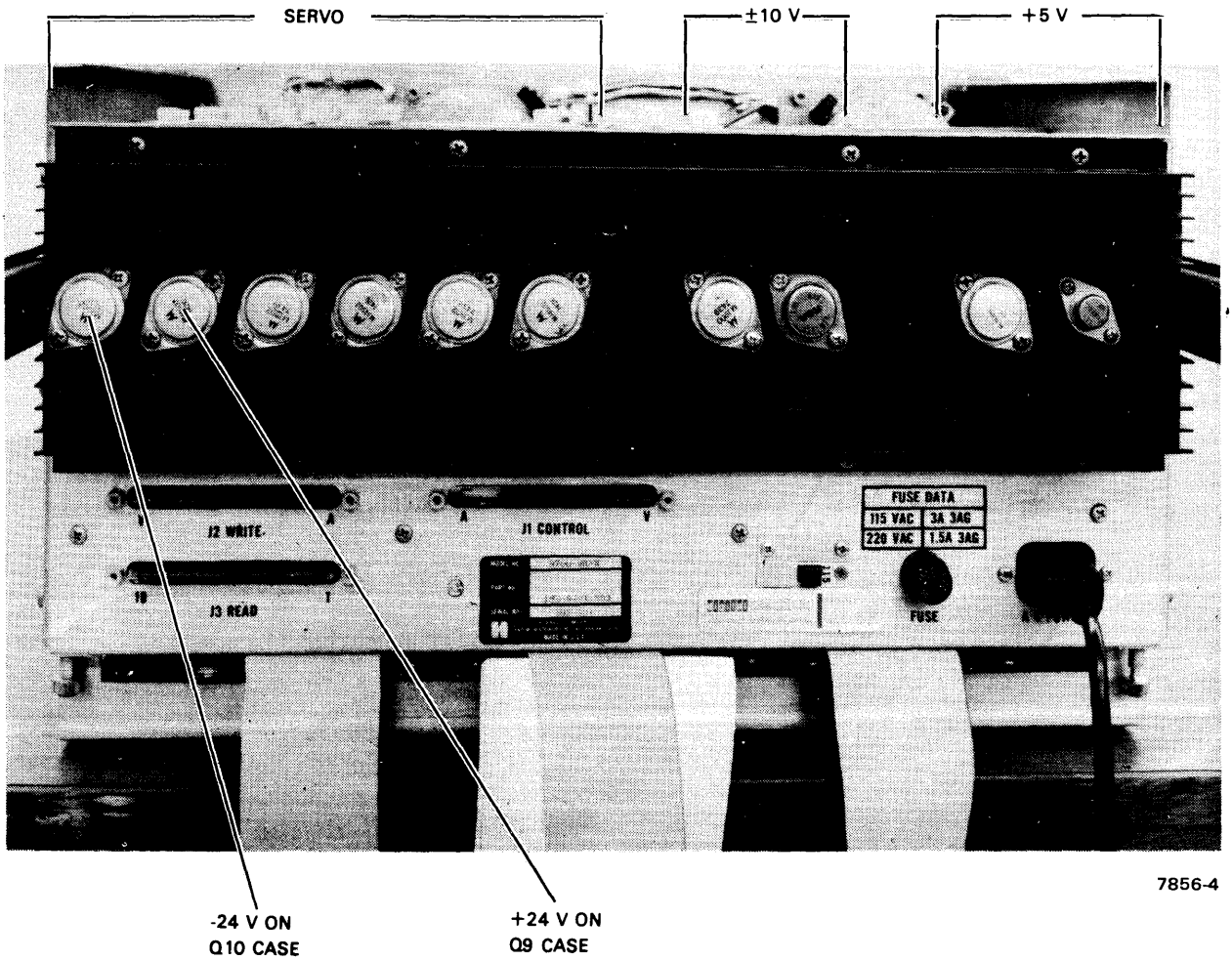


Figure 5-5 TS03 Tape Transport, Rear View

5.5.3.2 Tape Path Alignment – The tape path leading to and from the tape head must be as straight as possible. Variations in the tape path will cause the tape to be twisted as it moves over the head. The alignment procedure will compensate for mechanical tolerances and wear of buffer arm rollers and tape guides. Perform the following steps to accomplish a tape path alignment.

NOTE

An alternate tape path alignment procedure, not requiring the tape path alignment tool, can be found immediately following this procedure.

1. Remove protective covering in front of M8920 module by removing two Phillips head screws (master drive only).

2. Remove the control panel cover by lifting up and outwards from bottom.

3. Remove both tape guides (screws will be used to mount alignment tool) (Figure 5-6).

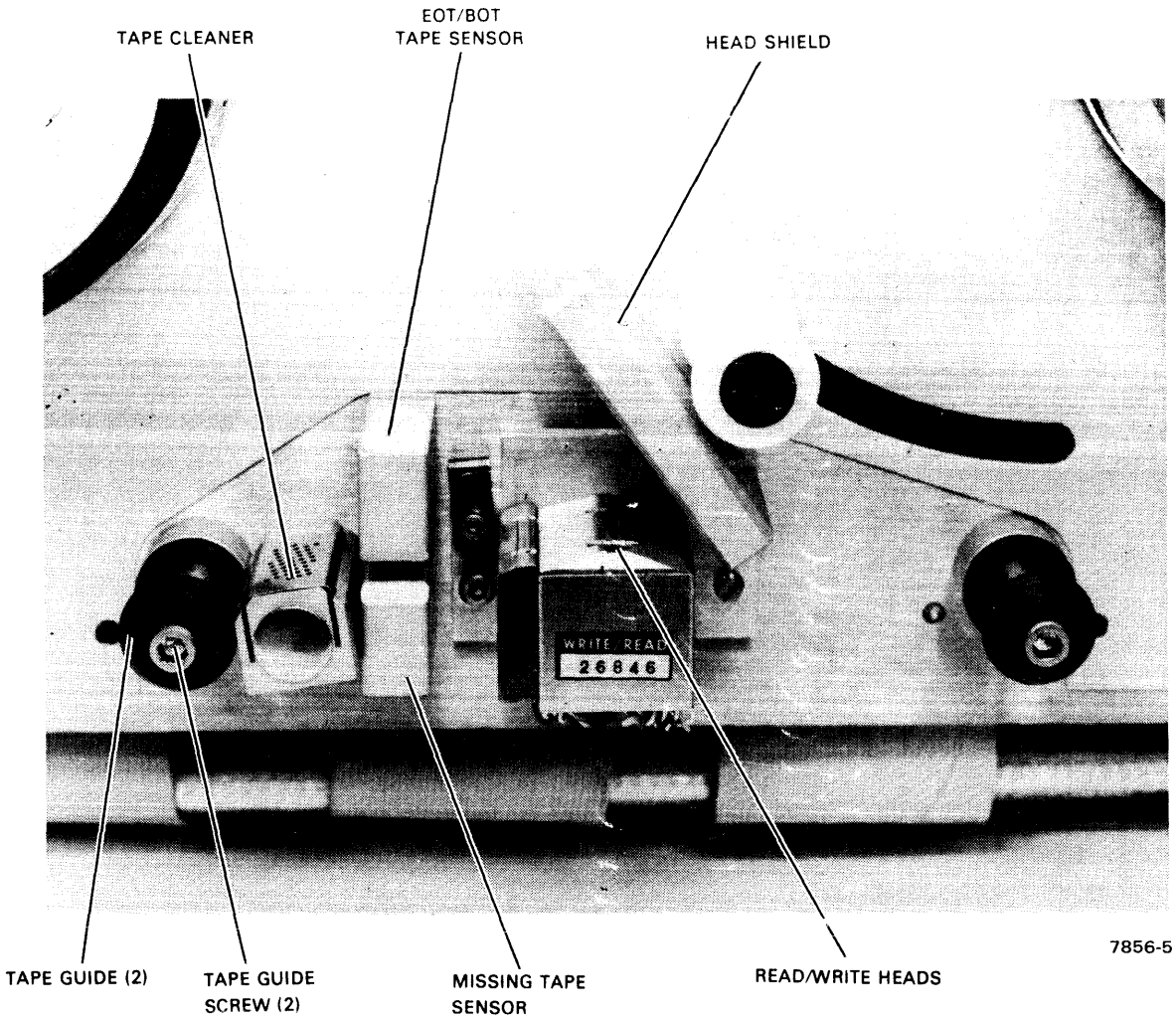


Figure 5-6 Head Assembly with Tape Guides

4. Mount tape path alignment tool using tape guide screws. Tighten screws finger-tight.

5. Use an Allen wrench to loosen tape path alignment clamp screws on both tape tension arms from bottom side of drive (Figure 5-7).

6. Loosen perpendicularity adjustment lock screws.

7. Center each roller guide in the "Vee" of the alignment tool and lock in place with the clamp. The clamp handle has a slip clutch to prevent damage to the roller (Figure 5-8).

8. Tighten perpendicularity adjustment lock screw for both rollers.

9. Disengage one clamp.

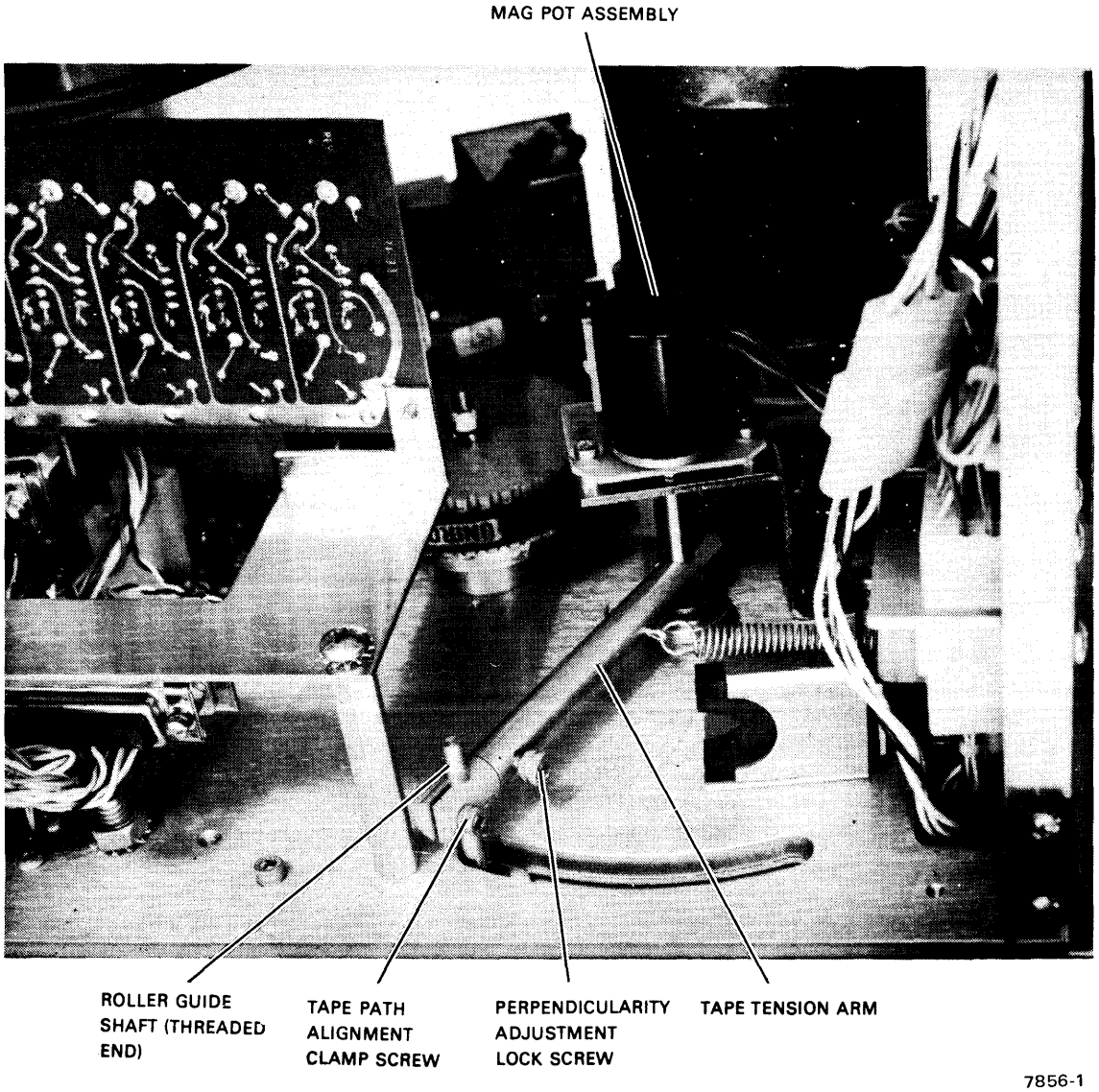


Figure 5-7 Roller Guide/Tape Tension Arm Connection, Bottom View

10. Align the roller path with a guide by pressing the released roller inward until the roller guide face just touches the outer face of the alignment tool. (Figure 5-9).

11. Tighten the tape path alignment clamp.

12. Repeat steps 9, 10, and 11 for the other roller guide.

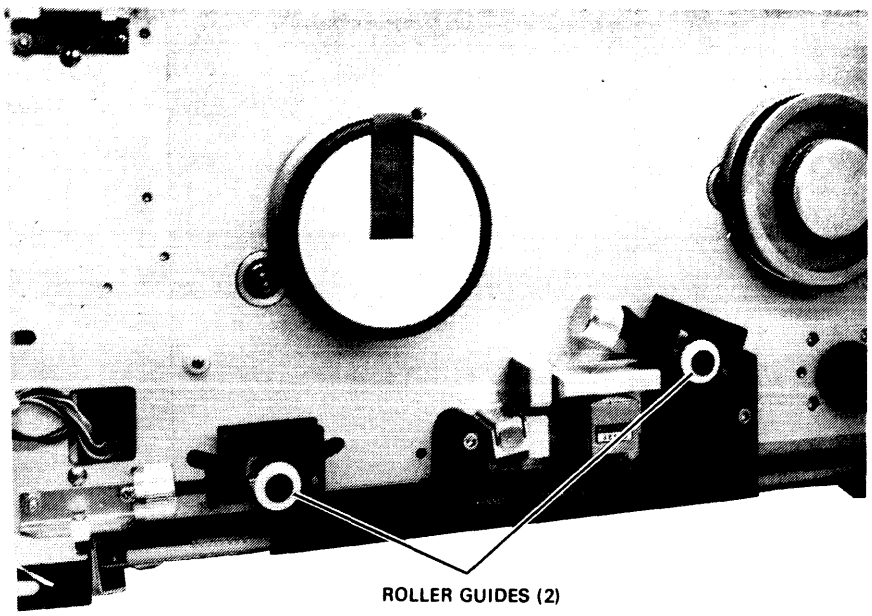


Figure 5-8 Use of Alignment Tool

ALTERNATE PROCEDURE

Tape Path Alignment Without Use of Alignment Tool

This procedure is provided in case the special purpose alignment tool is not available. The following material is required for this special procedure:

- Stainless steel 3/16 in. rod (0.1875 in. dia. by approximately 4 in. (10.16 cm) long)
- 10-32 nut (2)
- #10 washers (10)

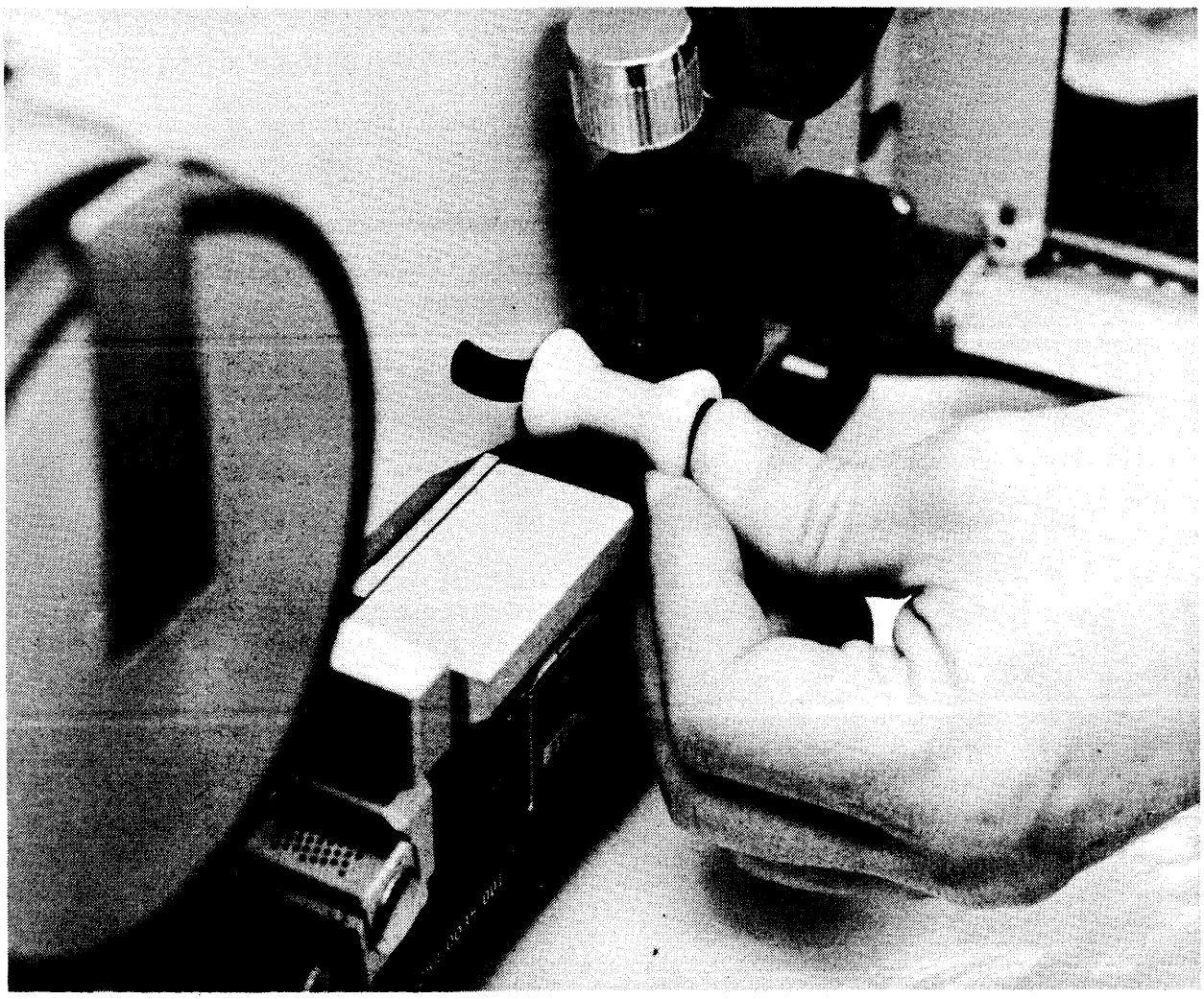
(Refer to Figure 5-7 throughout this procedure.)

1. Remove the roller guide to be aligned and replace it with a length (4 in. (10.16 cm) approximately) of 3/16 in. (0.1875 in.) stainless steel round rod stock. Clamp in place with the tape path alignment clamp screw.

2. Loosen the perpendicularity adjustment lockscrew slightly so that with moderate pressure the end of the tape tension arm can be rotated.

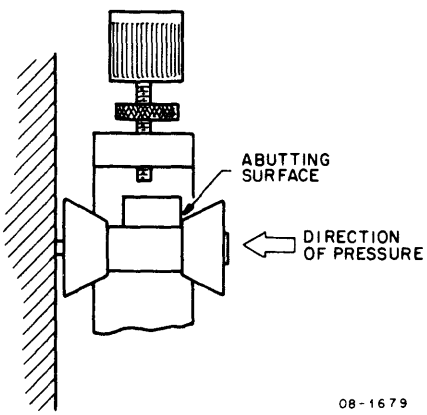
3. Thread mag-tape over the rod.

4. While holding the rod, run the tape forward. Tilt the rod up and down until a position is found at which the tape runs with equal tension on its inside and outside edge and the tape enters the tape guides correctly and winds correctly on the center of the take-up reel.



7856-7

a. Setting Roller Guide Position



b. Proper Alignment Position

Figure 5-9 Tape Path Alignment

5. When this position is found, tighten the perpendicularity adjustment lockscrew securely.

6. Replace the roller guide and clamp lightly by gently tightening the tape path alignment clamp screw.

7. The roller guide shaft end is threaded to allow use of a nut for fine adjustment. Place several No. 10 flat washers over the threaded end and install a 10-32 nut on the shaft.

8. Pull the roller guide so that the roller is too far out. Lightly tighten the adjustment nut.

9. Load the tape on the transport and feed it forward.

10. Tighten the nut pulling the roller guide back in toward the transport until the tape runs along the reference edge just inside the outer surface of the roller guide with the spring-loaded side of the tape guide manually pushed in.

11. Tighten the tape path alignment clamp screw.

12. Remove the adjusting nut and washers.

5.5.3.3 Capstan Creep Adjustment – The capstan servo loop employs an operational amplifier which is subject to dc offset due to component tolerances and aging. This offset could cause the capstan motor to creep. To adjust for capstan creep, perform the following steps:

NOTE
Tape tension arms may be clamped in alignment tool to reduce noise distraction.

1. With power OFF, extend servo Pre-Amp Card (No. 13) using the extender board.

2. Power up the drive unit.

3. Fold a piece of white paper in half twice to obtain quadruple thickness.

4. Press LOAD button and hold.

5. Insert quadruple thickness paper under EOT/BOT sensor lamp (Figure 5-6). Insert paper from the front, not the side, taking care that the paper does not get between the head and head shield.

6. Release the LOAD switch; capstan should be stationary.

7. Attach voltage probe to test point "A" (Figure 5-10).

8. Set capstan creep adjustment (R56) for minimum voltage.

9. Remove folded white paper.

10. Remove power from tape drive.

11. Remove extender board and replace Servo Pre-Amp Card in slot 13.

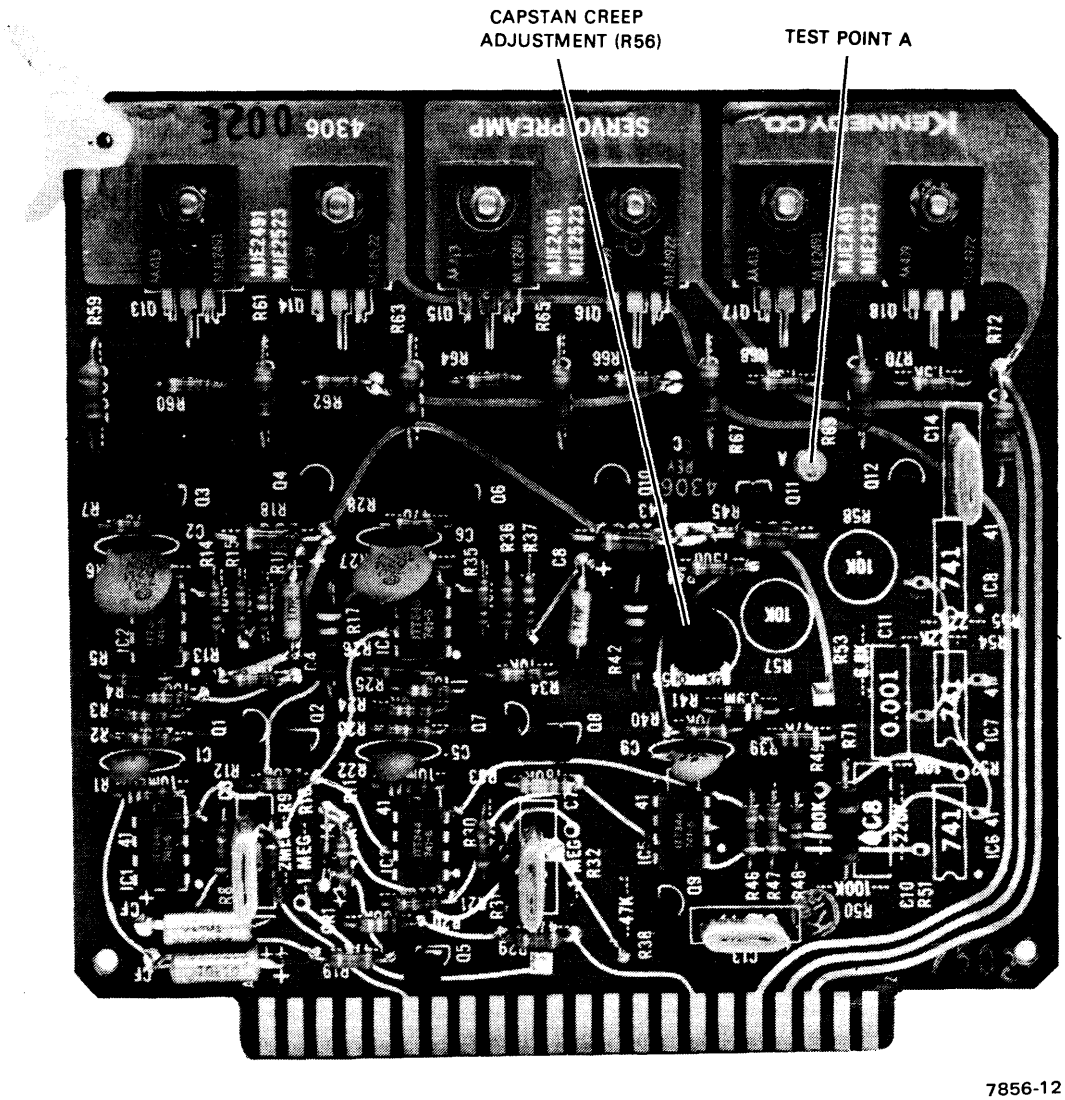


Figure 5-10 Servo Pre-Amp, Card No. 13

5.5.3.4 Mag Pot Adjustment – A magnetic potentiometer provides an electrical indication of spring tension on the tape tension arm. An electrical null point in the center of the tension arm travel arc indicates when the tape tension is at approximately 8 ounces. The procedure will ensure that the tension arm is at a null when in the center of the travel arc and that the null is the correct one. Refer to Figure 5-11 during the procedure.

1. With power ON and the tape path alignment tool attached, press LOAD button on the drive control panel. Both reels will rotate counterclockwise.

2. Insert folded white paper under BOT/EOT sensor lamp.

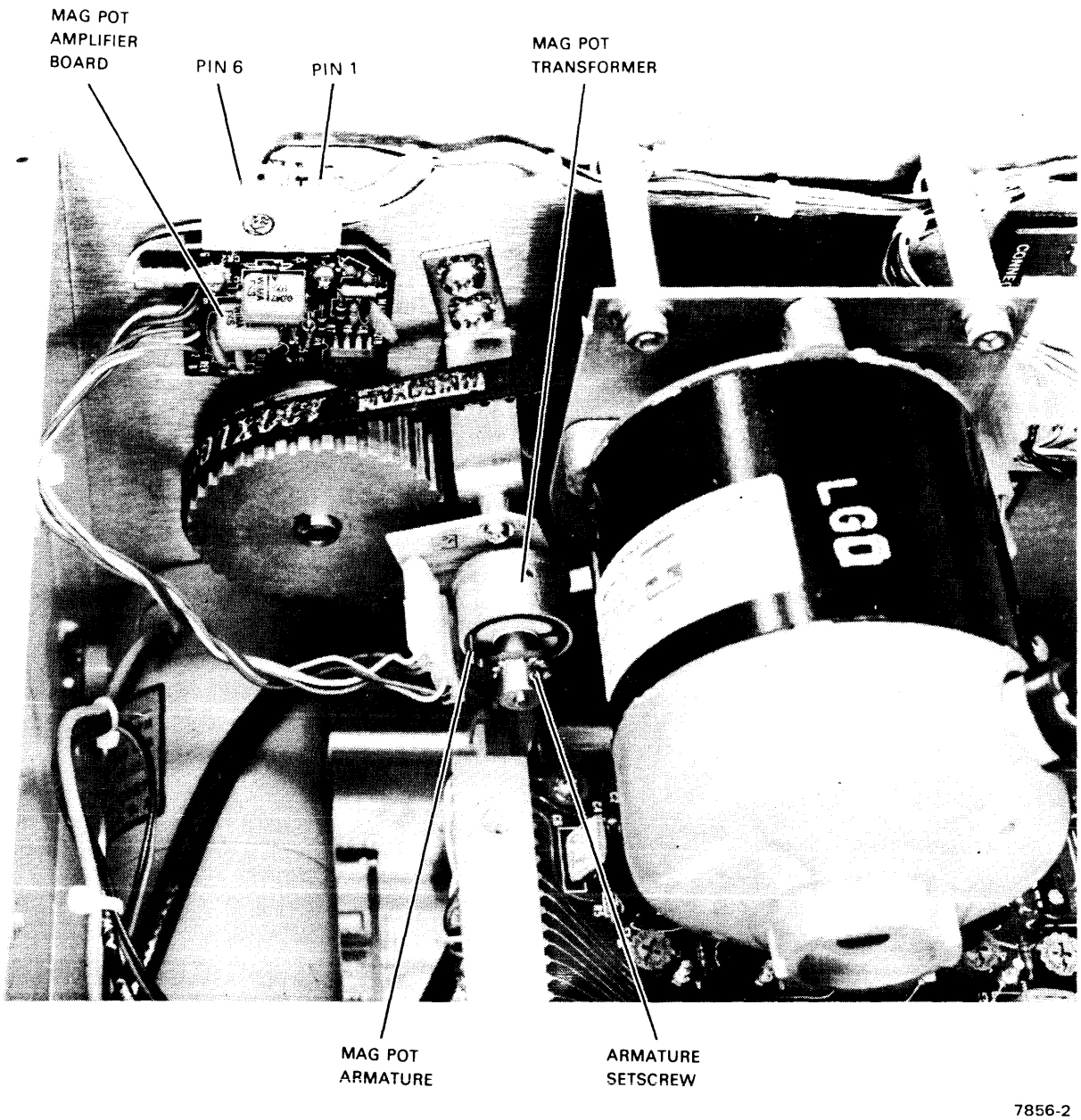


Figure 5-11 Mag Pot Position Sensor Assembly, Plastic Cover Removed

3. Manually swing tension arm into "Vee" of alignment tool and clamp in place. Reel should stop. Slow reel motion is acceptable. Perform this procedure for both reels.

4. If conditions in step 3 are not met, adjustment is required. Slip off the plastic mag pot cover.

5. Loosen armature set screw.

6. Adjust armature until motion stops.

7. Tighten armature set screw.

CAUTION

The magpot has two null positions 180° apart. Adjusting for the wrong null will cause the tape tension arm to seek the limits of the arc instead of its center. A 180° null position is also indicated if the tape hub spins clockwise when the tape tension arm is released without the tape threaded.

8. Replace mag pot cover.

9. Remove alignment tool and replace tape guides.

10. Verify proper operation by checking output of mag pot at pin 4 of the mag pot connector for approximately +5 to -5 V change while manually moving the buffer arm from one stop to the other (pin 4 wire on take-up reel is violet; pin 4 wire on supply reel is grey).

5.5.3.5 Write Lock Adjustment - A mechanical sensor detects the presence of the write ring. When the ring is detected, a solenoid withdraws the sensor away from the write ring and provides a write enable indication on the front panel. The adjustment procedure compensates for mechanical tolerances and verifies that the write lock operation is functioning.

1. Hold control panel LOAD button pressed.

2. Press write ring sensor approximately 1/8 in. (0.32 cm). Sensor should retract and hold itself just behind hub flange (Figure 5-12).

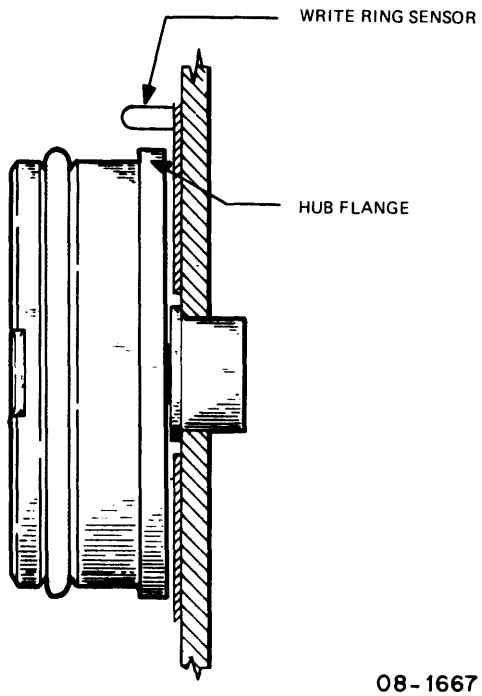


Figure 5-12 Supply Reel, Side View

3. Release LOAD switch. Sensor should extend to original position.

4. If the sensor does not withdraw behind the hub flange, loosen two adjustment screws in the sensor assembly and reposition the assembly so that the sensor is behind the hub flange when in the withdrawn state.

5.5.3.6 Head Shield Adjustment – Write head flux generated during a read-while-write operation is great enough to effect data being read. The "cross-talk" from write heads to read heads may cause parity, CRC, or LRC errors to be indicated at the controller when no errors exist. The head shield provides magnetic shielding between the read and write heads. To adjust the head shield, perform the following steps:

1. With tape removed from machine, loosen the stop screw (Figure 5-13).

2. Fold a section of magtape onto itself to obtain a triple thickness (0.006 in. (15 mm)).

3. Insert the triple thickness of tape between the head shield and the top surface of the head.

CAUTION

Do not **use feeler gauges – they will scratch the head surface.**

4. Press the shield firmly against tape and tighten stop screw.

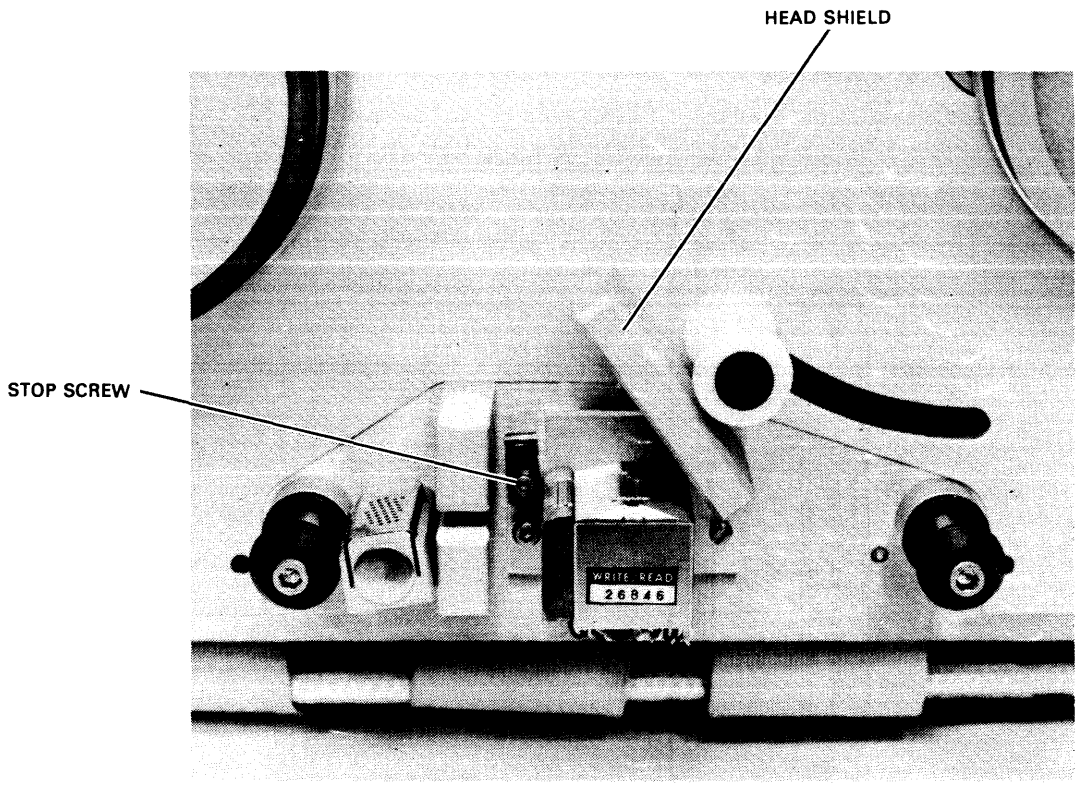


Figure 5-13 Head Shield Adjustment

5. Remove tape by lifting head shield.

6. Close the head shield.

5.5.3.7 Tape Cleaner Adjustment – The tape cleaner catches loosened oxide from the surface of the tape before it can relocate itself to the head or another part of the tape.

1. Mount tape on drive.

NOTE
Choice of skew tape here will simplify later adjustments.

2. Verify that the surface of the tape cleaner (Figure 5-6) presses lightly against the tape (just enough to deflect the tape path) and that it is parallel to the tape (Figure 5-14).

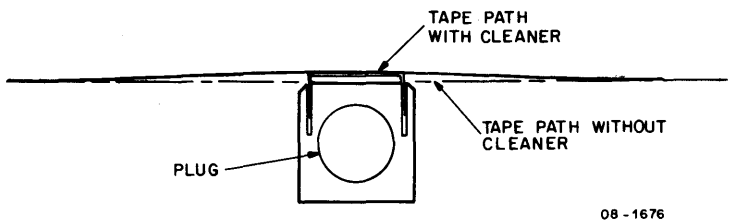


Figure 5-14 Tape Cleaner Adjustment

3. If the requirements of step 2 are not met, remove the plug in the end of the tape cleaner and loosen the Allen screw inside.

4. Adjust cleaner for proper position, tighten the Allen screw, and replace the plug.

5.5.3.8 Capstan Perpendicularity Adjustment – The capstan axis must be perpendicular to the tape path or the tape will move sideways on the capstan as the tape direction is changed. To adjust for capstan perpendicularity, perform the following steps:

NOTE
See Figure 5-3 for adjustments which must precede the capstan perpendicularity adjustment.

1. With the tape threaded, move it forward several feet (about 2 meters) at normal speed.

2. Note the position of the tape relative to the inner edge of the capstan.

3. Run the tape reverse for one foot and note the position of the tape as in step 2.

4. If the difference between the two edge positions is less than 1/32 in. (79 mm), (half the thickness of a penny), capstan perpendicularity is all right (Figure 5-15). If the difference is more than 1/32 in. (79 mm), and if adjustment screws A and B in Figure 5-16 are provided, proceed to step 5.

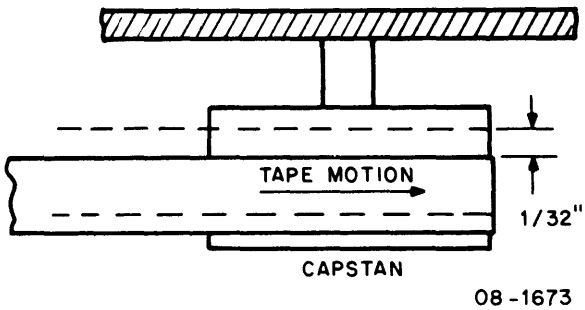


Figure 5-15 Capstan Perpendicularity Check

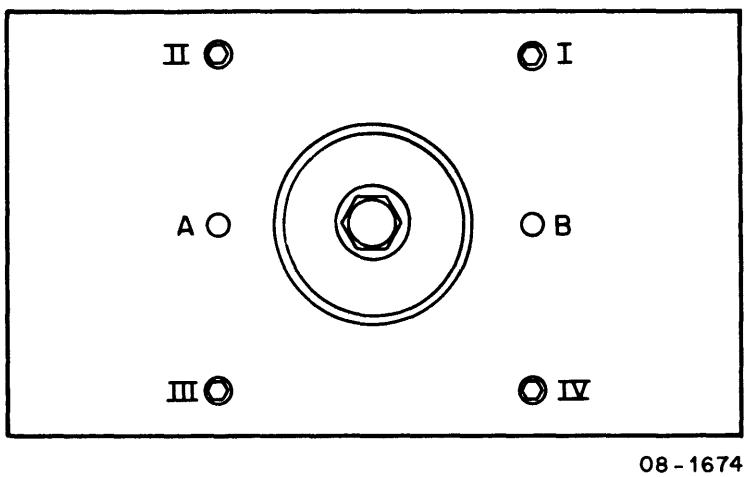


Figure 5-16 Capstan Motor Mounting Screws

5. Slightly loosen mounting screws I and IV, then II and III.

6. Adjust set screws A or B for minimum sideway tape movement when running tape one foot (30 cm) forward to one foot (30 cm) reverse.

7. Tighten four mounting screws so that those closest to the adjusted set screw are adjusted last.

8. Observe the tape motion through tape guide. When properly aligned, the tape will have a slight tendency to follow the spring loaded (inside) edge guide when the inner guide is pressed manually. The tape should not run hard against either guide surface.

5.5.3.9 Photo Sensor Adjustment - The Load Point (BOT) and EOT sensors employ a balanced analog circuit using two cadmium sulfide photo resistors. The photo sensor adjustment compensates for aging of the photo resistor elements. Perform the following steps:

1. Verify that both upper and lower photo sensor lamps are illuminated.

2. Verify that tape is threaded and that a reflective maker is not positioned between the sensor lamps.

3. Measure voltage between TP-E and TP-F on the sensor amplifier board (No. 12) (Figure 5-4).

4. Set the photo sensor adjustment for 0 V difference between test points.

5.5.3.10 Tape Speed Adjustment – Tape speed must be maintained at a constant value so that tapes written on one drive will be compatible with other drives. To adjust tape speed, perform the following steps.

NOTE
See Figure 5-3 for adjustments which must precede the tape speed adjustment.

1. Mount skew master tape.

2. Attach test box.

3. Run tape FWD.

4. Observe any of the read preamp test points (Figure 5-17) using the oscilloscope; check for a sine wave with a period of approximately 200 μs. The waveform may not be stationary due to small tape speed variations.

5. Adjust speed control potentiometer for a 200 μs period. Refer to Figures 5-4 and 5-17 for location of potentiometer.

5.5.3.11 Read Skew Adjustment – This adjustment serves to mechanically position the read heads perpendicular to the reference edge of the tape as shown in Figure 5-18.

NOTE
See Figure 5-3 for adjustments which must precede a read skew adjustment.

1. Run skew master tape forward.

CAUTION
Do not run skew tape at fast speed — FWD or REV.

2. If skew error LED on the test box is lit, adjust the skew adjustment screw until the light is out (Figure 5-19).

   a. An alternate procedure is to use an oscilloscope and adjust for *minimum* voltage level at the test point on the test box (Figure 5-20). Set sweep speed for 100 ms/division. Set vertical gain to 0.5 V/division thereby giving 10 μs of character skew per 1 V of output.

   b. Still another method (not using the test box) is to place the scope on pin 8 on the edge connector at the top of the motion control card and adjust for minimum data packet spread.

3. Select REVERSE RUN. When the tape stops, remove the master skew tape.

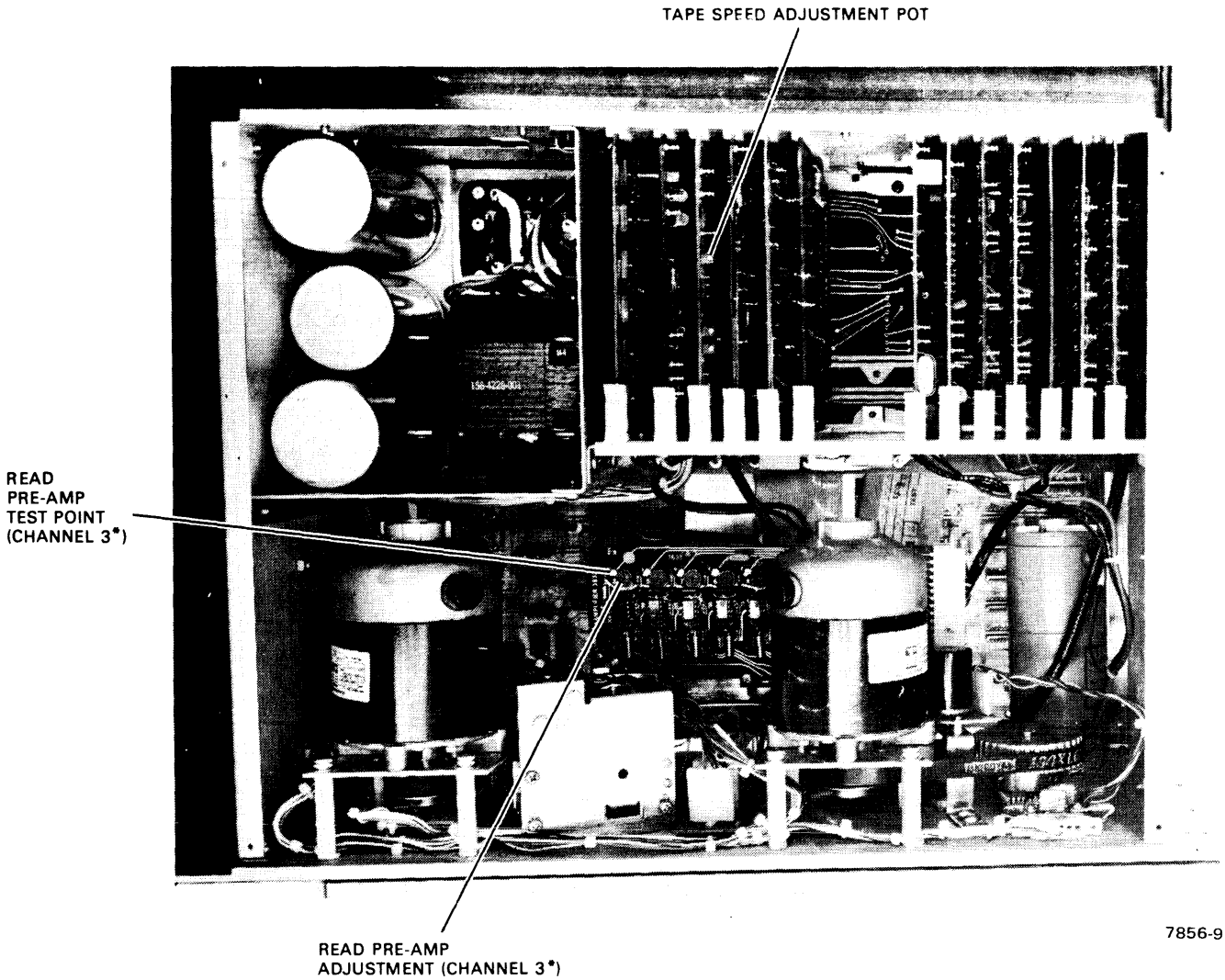


Figure 5-17 Tape Speed and Read Pre-Amp Adjustment

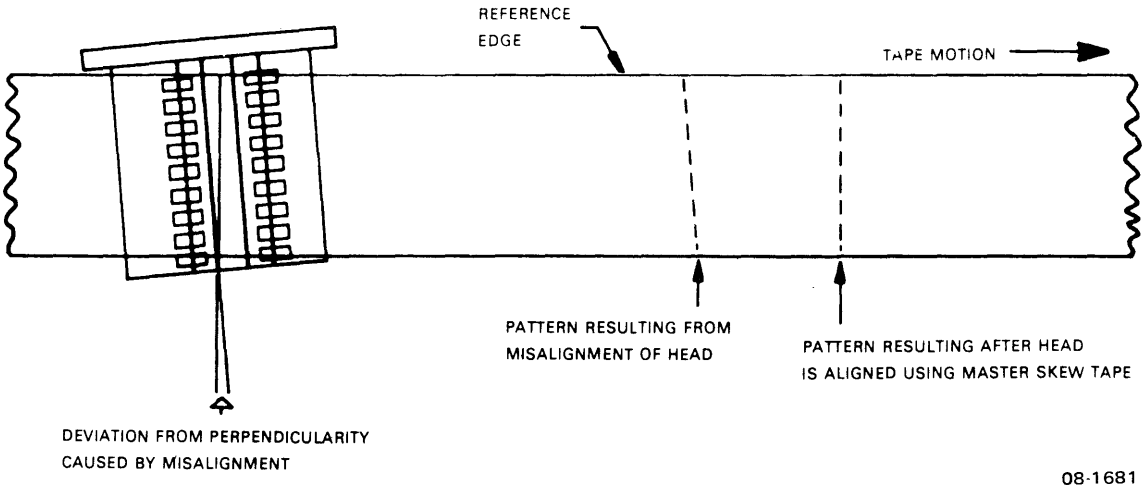


Figure 5-18 Skew Error (Caused by non-perpendicularity of head assembly to reference edge of tape)

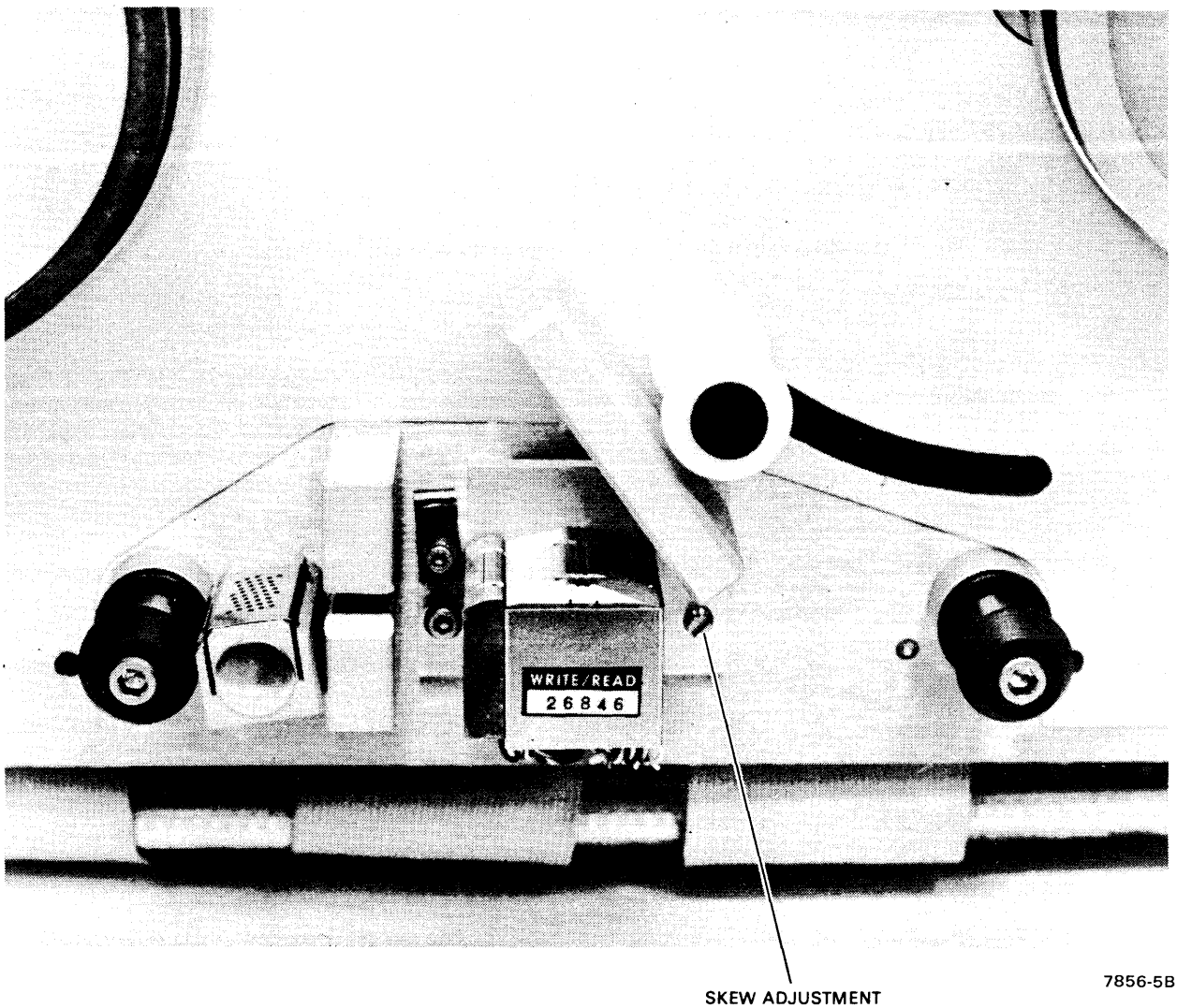


Figure 5-19 Location of Skew Adjustment

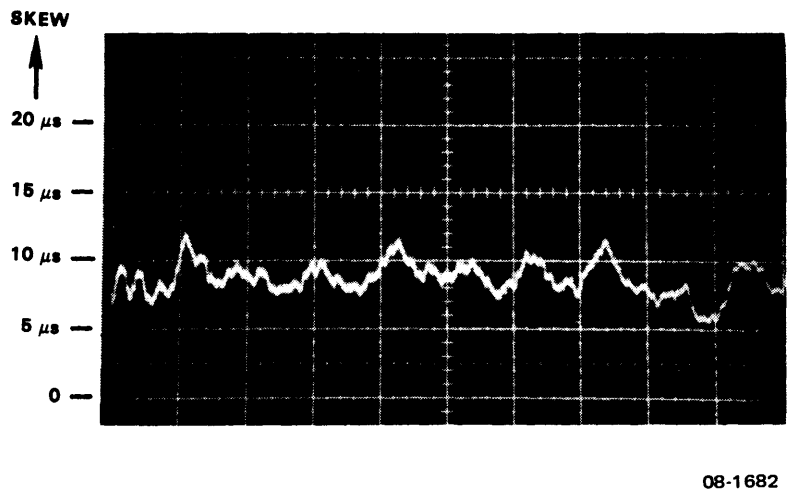


Figure 5-20 Read Skew Adjustment Waveform

5.5.3.12 Read Level Adjustment – This adjustment is made by measuring the read signal while writing an all 1s pattern. (This technique results in an observed signal amplitude that is more constant and 10 percent greater than a normal read.)

NOTE
See Figure 5-3 for adjustments which must precede a read level adjustment.

1. Mount scratch tape with write ring.
2. Write an all 1s pattern by making the following selections on the test box:
   a. Test mode
   b. Write test
   c. Forward run
3. Using an oscilloscope, observe the waveform at the first test point (Channel 3) on read preamp (Figure 5-17).
4. Adjust the potentiometer adjacent to the test point for a sine wave of 9 V (±0.5 V) peak-to-peak.
5. Repeat this procedure for each of the remaining eight read preamplifiers.

5.5.3.13 Write Skew Adjustment – Although read and write heads share the same head assembly, they are not perfectly parallel due to machining tolerances (Figure 5-21).

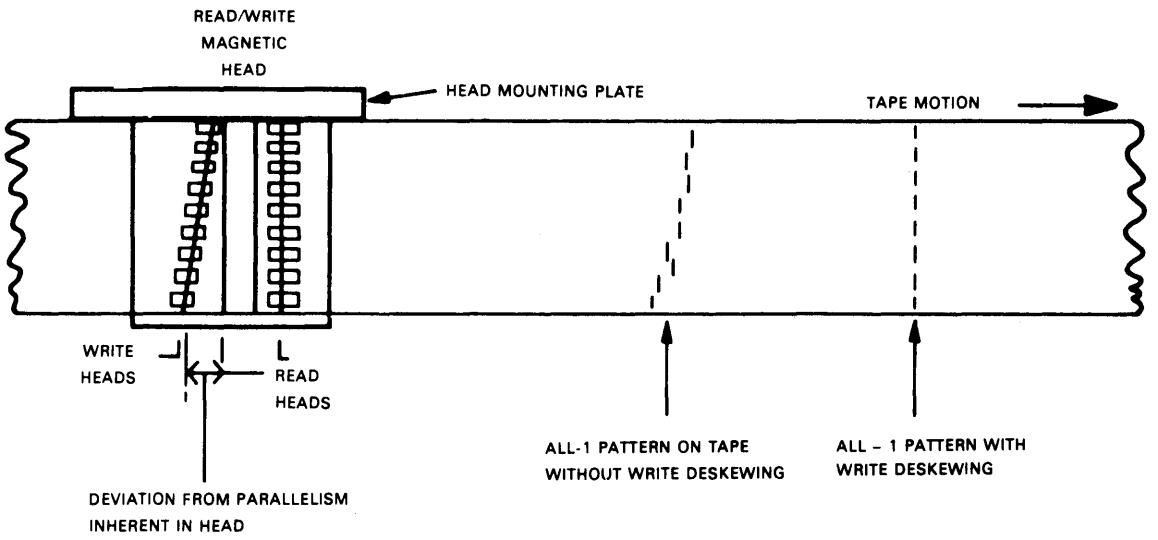


Figure 5-21 Skew Error (Caused by misalignment of Read/Write heads)

After the mechanical read deskewing has been accomplished, the write heads are deskewed by providing appropriate electrical delays to each write channel.

NOTE

See Figure 5-3 for adjustments which must precede a write skew adjustment.

1. With SCRATCH TAPE still mounted, make the following selections on the test box.

   a. Test mode
   b. Write test
   c. Forward run

   This operation causes an all 1s pattern to be written on tape.

2. Attach the reference probe (channel No. 1), of a dual channel oscilloscope, to test point p (parity channel) board no. 6 (Figure 5-4).

3. Attach channel no. 2 test probe to test point 0 (read channel 0) on board no. 5.

4. Verify that the second read pulse has less than 1.7 μs separation from the reference channel, as shown in Figure 5-22.

NOTE

The instability in the untriggered pulse is caused by dynamic skew.

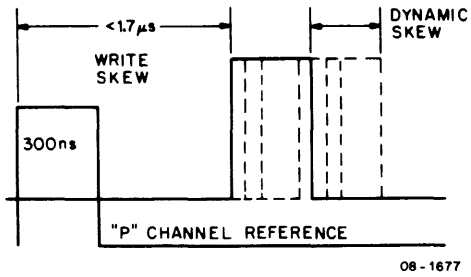


Figure 5-22 Write Skew Adjustment

5. Repeat steps 3 and 4 for the remaining seven read channels. Channels 4 through 7 are located on an identical PC board in slot 4. Make note of any channels that exceed the 1.7 μs tolerance.

6. If any channel has a pulse separation greater than 1.7 μs, power down and extend the appropriate write amplifier card (channels 0 through 2 on card 2; channels 3 through 7 on card 1).

7. Restore power and test conditions, and adjust the appropriate four bit "DIP" switches for minimum pulse separation. Note that each switch doubles the change of the previous switch. Switch S1 provides a 3.1 μs change while S4 provides a 25 μs change. A closed switch will move the corresponding pulse to the left.

5.5.3.14 Ramp Time Adjustments - Tape acceleration and deceleration times must have close tolerances to provide interrecord gap compatible with other tape drives.

1. With the scratch tape mounted, press FORWARD RUN on the test box to run the tape forward at low speed.

2. Pull the test box toggle switch forward.

3. Attach the oscilloscope external trigger to red wire on the test box connector (Figure 5-2).

4. Observe test point "A" on the ramp generator card (Figure 5-4) for positive going RAMP (Figure 5-23).

5. Adjust Start Ramp Potentiometer for 30 ms ramp time.

6. Adjust Stop Ramp Potentiometer for 30 ms ramp time.

7. Power down and restore the drive to its original condition.

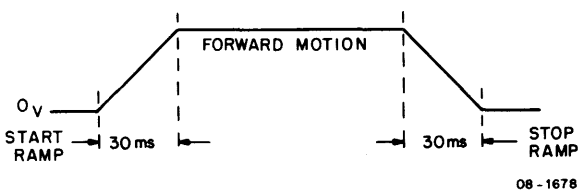


Figure 5-23 Ramp Time Adjustments

5.6 CORRECTIVE MAINTENANCE

Corrective maintenance information is provided to guide and aid the maintenance technician when isolating and repairing faults. The information consists of five troubleshooting aids: the TM8-M diagnostics, the corrective action flow diagram, the functional block diagram, TS03 transport troubleshooting hints, and TS03 transport troubleshooting tables.

5.6.1 TM8-M Diagnostics

Diagnostics, consisting of a paper tape and documentation, are provided with each system. The documentation includes instructions on loading, running, and interpreting diagnostic printouts. The diagnostics provided with the TM8-M are listed in Table 5-4.

Table 5-4
TM8-M Diagnostics

Title	Designation
TM8-E/TS03 Control Test, Part 1	MAINDEC-08-DHTSA
TM8-E/TS03 Control Test, Part 2	MAINDEC-08-DHTSB
TM8-E/TS03 Data Reliability, 9-Track	MAINDEC-08-DHTSC
TM8-E/TS03 Drive Function Timer	MAINDEC-08-DHTSE
TM8-E/TS03 Utility Driver	MAINDEC-08-DHTSF

5.6.2 Corrective Action Flow Diagram

Figure 5-24 provides sequential procedures for troubleshooting the TM8-M.

5.6.3 Functional Block Diagram

Figure 1-4 functionally separates the circuitry comprising the three major units (TM8-E, M8920, TS03) into functional blocks and depicts signal flow between those blocks within each unit; it also depicts interfacing between each unit and interfacing between the TM8-E and the Omnibus. The functional block diagram can be used in conjunction with Figure 5-24 for troubleshooting and maintenance.

5.6.4 TM8-E Controller Troubleshooting Hints

The diagnostics listed in Table 5-4 will test and troubleshoot all functions of the TM8-E Controller. By using the diagnostics and the functional block diagram (Figure 1-4), troubles within the controller can be isolated and repaired.

5.6.5 TS03 Transport Troubleshooting Hints

Table 5-5 suggests possible causes when problems are encountered with the transport.

5.6.6 TS03 Transport Troubleshooting Tables

Tables 5-6 and 5-7 list transport symptoms versus possible causes, indications, and corrective actions.

5.6.7 Troubleshooting Procedure

When problems are encountered in system operation, the technician should

1. Discuss the symptoms with operation personnel to determine the exact nature of the failure.

2. Refer to the corrective action flow diagram (Figure 5-24) and proceed as directed.

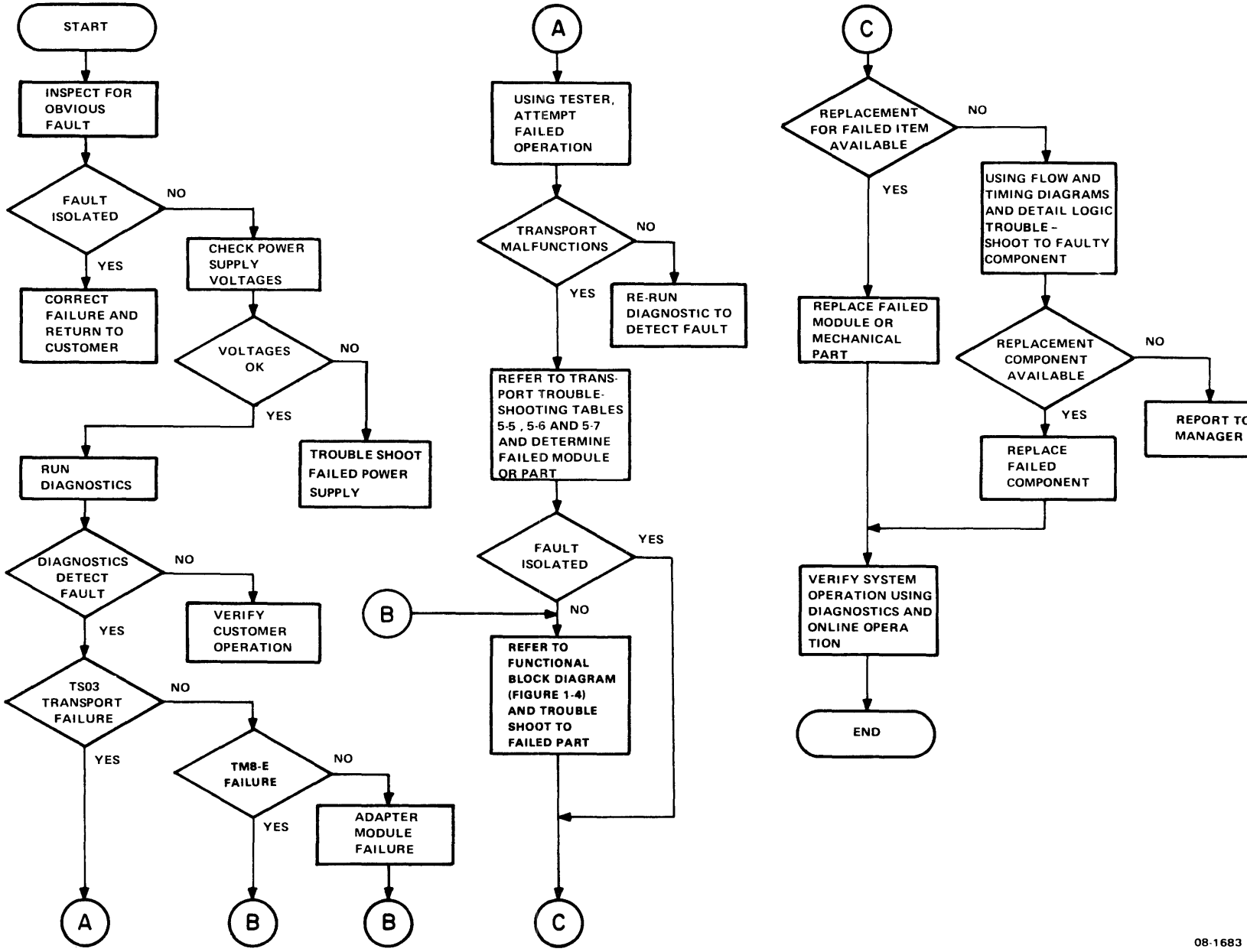


Figure 5-24 TM8-M Corrective Action Flow Diagram

Table 5-5
TS03 DECmagtape Transport Troubleshooting Hints

Problem	Hints
General	Problems in the TS03 transport can usually be classified as either mechanical or electrical but often the classification may be confusing because a basically mechanical problem can cause what appears to be an electronic malfunction and vice versa. In any case the problem should be thoroughly analyzed before adjustments are made. Electronic troubleshooting is greatly facilitated by the modular construction – a new card may be substituted and the effect observed. Most difficult, of course, are subtle problems and those of an intermittent nature. Visualizing solution (Magna-See) is useful under certain conditions for troubleshooting. At high densities the data cannot be satisfactorily resolved but such problems as a dead track, improper gap length, etc., can be isolated rapidly by its use. If a tape has had visualizing solution applied to it, *do not* reuse that portion of the tape as it will contaminate the head. Cut the visualized portion off and discard. To use visualizing solution, shake the can thoroughly, remove top, and pass portion to be visualized through the solution. Snap the tape vigorously to remove excess solution and let dry. Iron powder will be left in magnetized areas. This can be picked off using Scotch tape and applied to a sheet of paper for a permanent record.
High Error Rate	Usually the more difficult problems involve a higher than permissible error rate for which there is no obvious reason. If operating properly with good tape, the transport should make very few errors in writing and, if rewriting is included in the program, it should make no read errors. Useful clues are: 1. In what mode (read or write) are many errors occurring? 2. At what point in the block does the error occur? 3. What is the nature of the error: VRC, CRC, LRC? 4. Are the errors pattern related? 5. Do errors occur only on certain sets of commands? The first thing to be done is to inspect the head and other items in the tape path for dirt accumulations. Be sure everything is clean. Check the tape being used and try a new reel if tape is doubtful. Check interface connections for broken wires or bad contacts. Table 5-6 is a troubleshooting chart concerned with high error rate.

Table 5-5 (Cont)
TS03 DECmagtape Transport Troubleshooting Hints

Problem	Hints
Compatibility	The TS03 transport accepts and produces tapes conforming to the ANSI standards. Occasionally compatibility problems can arise: 1. Tapes written by and acceptable to the TS03 transport are not acceptable to another transport. 2. Foreign tapes cannot be read by the TS03 transport but its own tapes can be. Three items may be involved: skew, speed, ramp times. These should be checked as described in the adjustment procedures.
Other Malfunctions	Normal troubleshooting procedures are involved in finding electronic malfunctions. The first things to check are the supply voltages: ±24 V nominal unregulated will normally be about ±26 V under light load. ±10 V ± 0.5 V +5 V ± 0.25 V Convenient test points for measuring supply voltages are: +24 V – Case of Q9 (MJ802) on heat sink -24 V – Case of Q10 (MJ4502) on heat sink +10 V – Sensor amplifier/driver TPA -10 V – Sensor amplifier/driver TPB +5 V – Sensor amplifier/driver TPC Voltages are measured to chassis (ground). **NOTE** **Turn power off when removing or inserting cards.** If the voltages are not correct, the trouble is in the power supply or the malfunction is loading the supply excessively. Pulling cards from their sockets can help isolate an overloaded condition. The power supply is short-circuit protected on the regulated voltages. A short circuit on +24 V should blow the fuse. Assuming the voltages are correct, Table 5-7 should help in isolating malfunctions.

Table 5-6
High Error Rate Troubleshooting

Symptom	Possible Cause	Indication	Action	Reference
Continuous errors, every block (read mode).	Broken connection to interface or internally.	Continuity.	Correct connection.	
	Bad preamplifier channel.	No output at test point on write test.	Replace preamplifier.	
	Bad quad read amplifier channel.	No data at test point.	Replace quad read amplifier.	
	Tape speed grossly wrong.	Visual or skew master.	Adjust speed.	5.5.3.10
	Bad head channel.	No output at preamplifier test point on write test.	Replace head.	5.7.6
Continuous errors, write mode only.	Broken connection on write data or WDS lines.	Continuity.	Correct connection.	
	Bad write amplifier channel.	Wrong or no signal at write amplifier test point in write test mode.	Replace write amplifier.	
Frequent write errors, few or no read errors.	Write-read crosstalk.	Noisy signal at preamplifier test point.	Check preamplifier gain. Check head shield spacing.	5.5.3.12 5.5.3.6
Frequent CRC and LRC errors, no VRC errors.	Wrong CRC generation in interface.	Wrong data at input.	Correct interface.	
Read or write errors only at start of block.	Ramp time wrong.	Read signals appear before ramp is complete.	Adjust ramp time.	5.5.3.14
Read errors on long blocks only.	Tape path misaligned.	Tape bears heavily on one guide surface.	Tape Path alignment.	5.5.3.2
Pattern related errors.	Write-read crosstalk.	Noisy signal at preamplifier test point.	Check preamplifier gain. Check head shield spacing.	5.5.3.12 5.5.3.6

Table 5-7
Control Malfunctions Troubleshooting

Symptom	Possible Cause	Location	Action	Reference
LOAD pushbutton activates servos when pressed but does not hold.	Broken tape signal clears load flip-flop.			
	Sensor amplifier driver module	Card cage	Replace module.	
	Pushbutton control module	Card cage	Replace module.	
	Photosensor (BKN) malfunction	Deck	Replace sensor.	5.7.7
After load, tape runs and does not stop.	Tape feeds forward after load point marker is sensed.			
	Marker strip missing from tape.	Tape	Apply reflective strip.	
	Misadjustment of photosensor on sensor amplifier driver module.	Card cage	Adjust photosensor.	5.5.3.9
No EOT signal.	Same as load point above but for EOT.			5.5.3.9
REWIND pushbutton inoperative.	Logic malfunction, pushbutton control module.	Card cage	Replace module.	
Rewind does not stop at LP but continues until tape is wound off reel.	Same as above.			
	Photosensor adjustment wrong on sensor amplifier driver module.	Card cage	Adjust photosensor	5.5.3.9
Reels rotate uncontrolled when power is turned on	Servo preamplifier malfunction.	Card cage	Remove preamplifier. If reels stop, replace preamplifier module.	
	Servo power amplifier (bad power transistors).	Heat sink	Replace heat sink assembly or locate and replace bad power transistors.	
Arms badly off center of arc at rest.	Magpot adjustment.	Deck	Adjust magpot setting.	5.5.3.4

Table 5-7 (Cont)
Control Malfunctions Troubleshooting

Symptom	Possible Cause	Location	Action	Reference
Arms bottom when starting or stopping. Weak reel torque, otherwise normal.	Servo preamplifier malfunction. Magpot adjustment (spacing). Bad reel motor.	Card cage Deck Deck	Replace module. Check adjustment. Replace reel motor.	5.5.3.4
Tape moves erratically, slips on capstan.	Head face shield touching tape. Defective tension roller.	Deck Deck	Adjust head shield setting. Replace roller.	5.5.3.6 5.7.1
Capstan turns slowly when it should be stopped.	Capstan zero adjustment on servo preamplifier module.	Card cage	Adjust zero.	5.5.3.3

5.7 PARTS REPLACEMENT

In most instances, assembly methods for parts replacement are obvious. Electronic parts are nearly all on plug-in modules. Items in the transport tape path may require machine realignment if replaced. If only one item in the transport tape path is replaced at a time, the complete alignment procedure may usually be avoided. Examples of transport parts replacement follow.

5.7.1 Roller Guide Replacement (Figure 5-7)

1. Loosen the tape path alignment clamp screw and remove the roller shaft from the tape tension arm. Do not loosen the perpendicularity adjustment lockscrew.

2. Insert a new roller guide shaft and clamp lightly by tightening the clamp screw.

3. Follow the tape path alignment procedure of paragraph 5.5.3.2 to install and align the new roller guide.

5.7.2 Tape Tension Arm Replacement

Tension arms are replaced by removing roller guides and disassembling. Do not attempt to remove the pin holding the arm to its shaft; replacement assemblies are supplied pinned. Reassemble the arm mechanism.

It will be necessary, if tension arms are replaced, to perform the complete tape path alignment procedure (Paragraph 5.5.3.2).

5.7.3 Reel Motor or Belt Replacement

1. Unplug the motor and remove the motor and mounting plate.

2. Remove the motor from mounting plate. Replace with a new motor.

3. Hook the drive belt on the motor pulley and replace the screws holding the motor mounting plate to the deck assembly.

4. Hold tension against the belt and tighten the mounting screws.

5. Check belt tension by squeezing between thumb and forefinger. The belt should deflect about 1/4 in. (0.6 cm). If not, loosen the screws and move the motor.

6. Plug in the motor.

5.7.4 Capstan Motor Replacement.

1. Remove the capstan lockscrew.

2. Remove the capstan. The capstan fits a taper on the motor shaft so it may be readily removed once loosened. It may require considerable force to break loose, however. Pullers are available for this use but a screwdriver properly protected to prevent marring may be used to pry against the panel.

3. Remove the four capstan motor mounting screws. Unplug and remove the motor.

4. Install a new motor. Note if a red dot is present on the motor housing. If a dot is present, the motor should be oriented to place the dot as near as possible to the outside end of the deck.

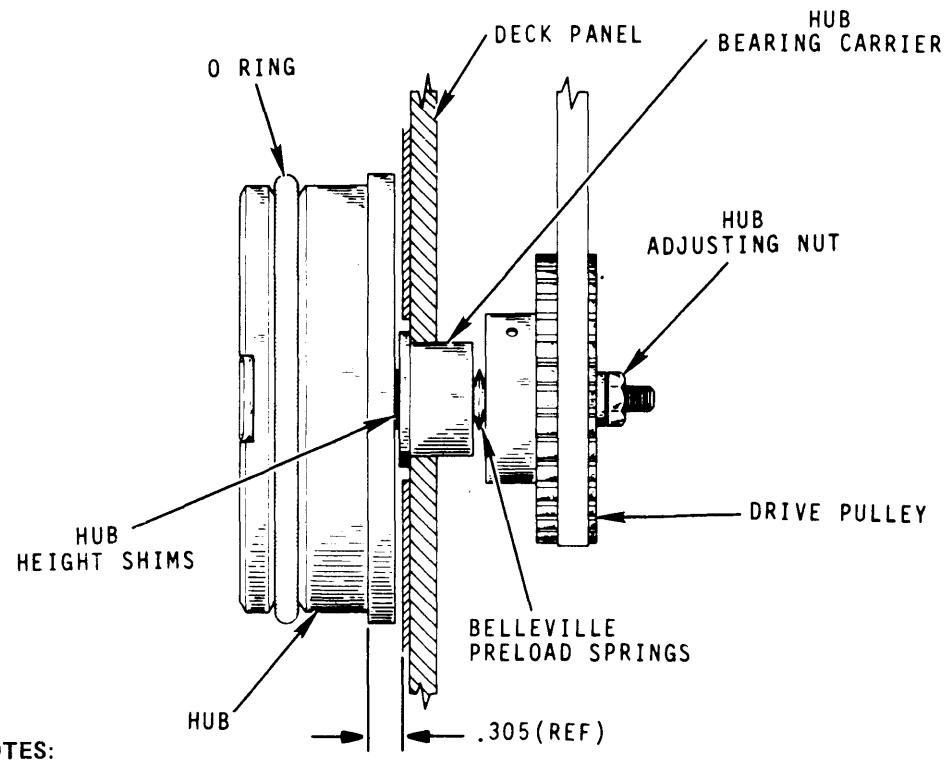
5. Adjust by procedure given under tape path alignment, Paragraph 5.5.3.2.

5.7.5 Supply Hub Replacement

After long use, components in the quick-locking mechanism may become worn to the point that adjustment of locking pressure cannot securely hold the tape reel. It is not necessary to replace the hub in its entirety; a hub repair kit is included.

Repair kits consist of a replacement lock lever, thrust washer, and O ring. (See Replaceable Parts List, Part III, Chapter 13.) To install:

1. Remove the lock adjusting nut.
2. Pull the lock lever out.
3. Remove the thrust washer.
4. Replace the thrust washer.
5. Install a new lock lever and replace the adjusting nut.
6. Install a new O ring.
7. Adjust the hub for proper holding force. Verify using several different reels. Refer to Figure 5-25 for more detailed adjustment procedures.



NOTES:

1. Loosen hub adjustment nut.
2. Open hub, install tape reel.
3. Close hub. Tighten hub adjusting nut until O ring presses firmly against reel.
4. Check for slippage under torque by holding hub or drive pulley. Reel should not slip on hub.
5. Open and close several times and recheck for slippage.
6. Try several reels, checking for slippage.

Figure 5-25 Reel Hub Adjustment

5.7.6 Magnetic Head Replacement

Replacement heads are supplied as complete assemblies together with mounting plate and face shield. A write deskewing chart is supplied with each head.

1. Unplug the head connectors.
2. Remove the head mounting screw and remove the head, passing connectors through the panel hole provided.
3. Be sure the adjusting screw on the replacement head is almost completely unscrewed.
4. Mount a new head with the mounting screw fairly loose. Screw in adjusting screw until point protrudes enough to engage its conical locating hole. Tighten the mounting screw.
5. Plug in the head.
6. Deskew the read head as described in the deskew adjustment procedure (Paragraph 5.5.3.11).
7. Set the deskewing switches on the write amplifiers to correspond to the chart supplied.
8. Place the chart over the old chart to record switch settings.

5.7.7 Photosensor Replacement

1. Remove the photosensor assembly by unplugging and removing the mounting screws. Since it will not pass through the hole provided, the connector must be removed by cutting the cable. Retain the connector.
2. Replacement sensors are provided with connector pins crimped to wires but with no connector shell installed.
3. Replace the assembly, passing the wires through the hole provided. Replace the screws.
4. Snap pins into the connector shell in the same color sequence as in the shell just removed; plug in the assembly.
5. Adjust as described in adjustment procedure.

5.7.8 Magpot Replacement (Figure 5-11)

1. Unplug the magpot assembly from its cable.
2. Remove the rotor by loosening the set screw.
3. Remove the screws holding the magpot PC board and remove the assembly.
4. Install a replacement unit.
5. Adjust the magpot according to Paragraph 5.5.3.4.

5.7.9 Tape Cleaner Replacement

1. Remove the circular snap-in plug cover.
2. Remove the mounting screw and tape cleaner.
3. Mount a new cleaner assembly with the mounting screw finger-tight.
4. Adjust the cleaner surface so that it just touches the tape and is parallel to the tape surface.
5. Tighten the mounting screw and install the snap-in plug cover.

PART II
TM8-E CONTROLLER

CHAPTER 6
INTRODUCTION

6.1 GENERAL DESCRIPTION

The TM8-E DECmagtape Control interfaces the PDP-8/A, E and M with the TS03 Transport (Figure 6-1).

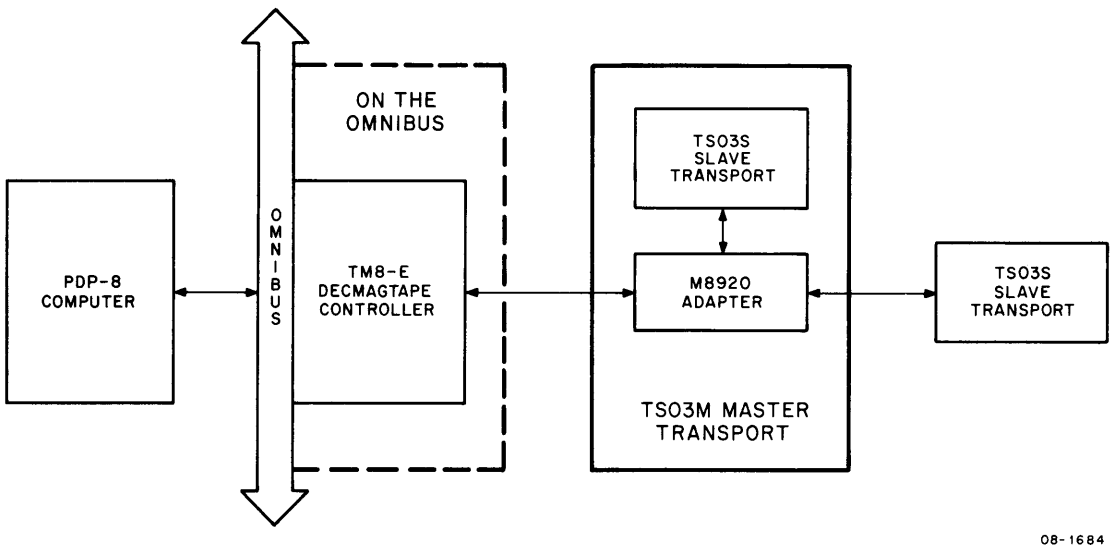


Figure 6-1 TM8-M Block Diagram

To perform this function, the TM8-E:

1. Decodes programmed instructions.
2. Accepts and stores word count, current address, command, and function words.
3. Selects a program-designated transport (two maximum in the system) and starts the operation designated by the program.
4. Generates break requests to initiate a single cycle data break.
5. Generates interrupts and skips for flag checking.
6. Buffers the input/output data and controls the writing on the 8 LSBs of a 12-bit word on 9-track transports.

7. Performs housekeeping chores for single cycle data breaks, i.e., increments Word Count and Current Address Registers.

8. Provides Error and Job Done flags.

9. Provides IOTs for TM8-E maintenance.

6.2 PHYSICAL DESCRIPTION

The following quad modules comprise the TM8-E:

M8321 Output Control Module
M8322 Control and Data Break Module
M8323 Transport Status and Control Module
M8327 Registers Module

These quad modules must be inserted into the Omnibus and connected together via H851 edge connectors. Two 7011571 cables are used to connect the TM8-E (input and output) to the TS03. The TM8-E receives +5 V logic power from the PDP-8 Omnibus. No power is supplied to or received from the TS03 by the TM8-E or PDP-8.

CHAPTER 7
BLOCK DIAGRAM DESCRIPTION

7.1 INTRODUCTION

Figure 7-1, a block diagram of the TM8-E DECmagtape Control, depicts the flow of signals among the modules, Omnibus, and the TS03 DECmagtape and slave. The modules are inserted into the Omnibus and signals are carried between the modules by H851 edge connectors. The TM8-E is connected to the TS03 DECmagtape by two 7011571 cables. The TM8-E modules are described in the following paragraphs.

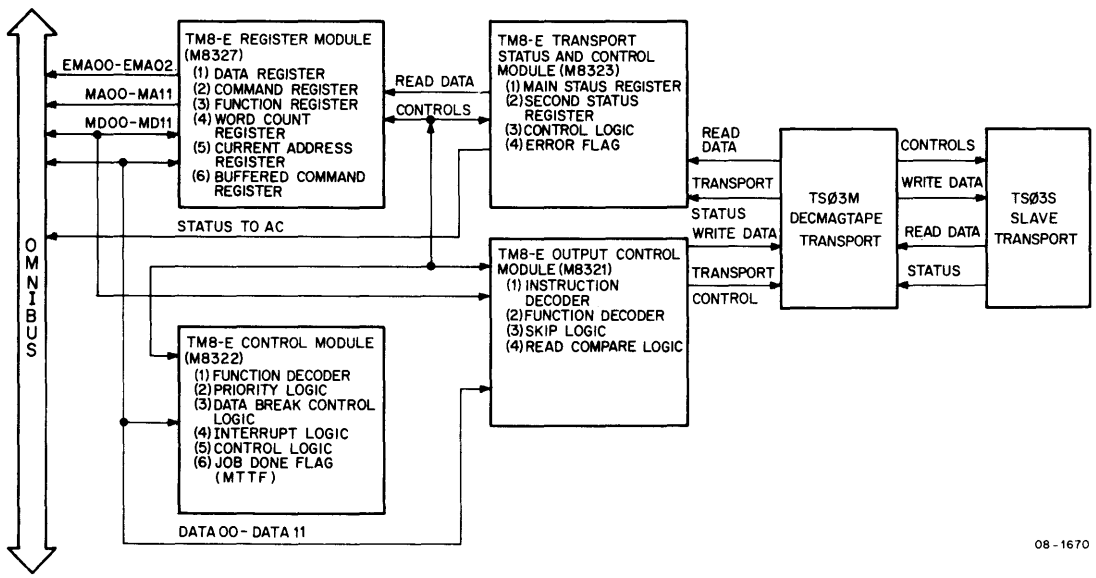


Figure 7-1 TM8-E Block Diagram

7.2 M8321 OUTPUT CONTROL MODULE

The M8321 Output Control module comprises three IOT instruction decoders, a function decoder, read/compare error detection logic, buffers, gating logic to multiplex data to be written on DECmagtape during a write operation, and skip logic.

7.2.1 IOT Instruction Decoder

The three decoders (device codes 70, 71, and 72) provide control signals in response to the IOT instructions. The IOT decoders generate control signals that are distributed to the logic of the other TM8-E modules to control data transfer between the TS03 and core memory. The control signals also control the loading and reading of TM8-E Registers and enable the error detection logic to monitor data transfer operations.

7.2.2 Function Decoder

The function decoder receives three function bits from the Function Register and decodes them to select one of the following DECmagtape functions (Paragraph 7.3.3).

Offline	Write
Rewind	Write End-of-File
Read	Space Forward
Read/Compare	Space Reverse

The function signals generated by the function decoder are sent to the TS03 master to control the selected DECmagtape transport.

7.2.3 Gating Logic

The WD bits are gated to the Write Data Buffers in response to control signals from the TM8-E control module and transferred to the TS03. Data is written in 9-bit characters (8 data bits plus parity). Parity for each character is generated in the TS03 master.

7.2.4 Read/Compare Error Detection Logic

The read/compare error detection logic compares data read from the DECmagtape with data in memory during the break cycle and generates a read/compare error if the data is different. This operation is accomplished by Exclusively-Oring the memory data with the data read from the DECmagtape. Note the parity bit is not checked by read/compare.

7.2.5 Skip Logic

The skip logic grounds the skip line and causes the program to skip the next instruction when the following conditions exist:

1. Tape Unit Ready (TUR) and an SKTR instruction is executed by the program.
2. ERROR flag is set and an SKEF instruction is executed by the program.
3. Control not busy and an SKCB instruction is executed by the program.
4. JOB DONE (MTTF) is set and an SKJD instruction is executed by the program.

This logic is used by the programmer for flag and error checking operations.

7.3 M8327 REGISTERS MODULE

The M8327 Registers module contains all of the TM8-E registers except the Main Status Register and Second Status Register. Each of the registers on the M8327 module is described in the following paragraphs.

7.3.1 Multiplexer and Data Register

The Multiplexer and Data Register stores information to be multiplexed to or from the transport or Omnibus. It accomplishes this task in the following manner:

1. It receives data to be written on tape from the MD lines during a write break cycle.
2. It receives data from the AC via IOT instructions.
3. The Omnibus receives data from the tape transport during a read operation via the Data Bus.
4. The Data Register receives data from the tape transport.
5. The master system receives data from Data Buffers during a write break cycle.

7.3.2 Command Register

The Command Register (Figure 7-2) is loaded with a 12-bit word from the AC by an LCMR instruction. The Command Register is used to select a tape transport (0–7),* enable or disable interrupts, select parity mode (odd or even), select memory field, and select DECmagtape recording densities. The contents of the Command Register are transferred to the AC for program evaluation by an RCMR instruction.

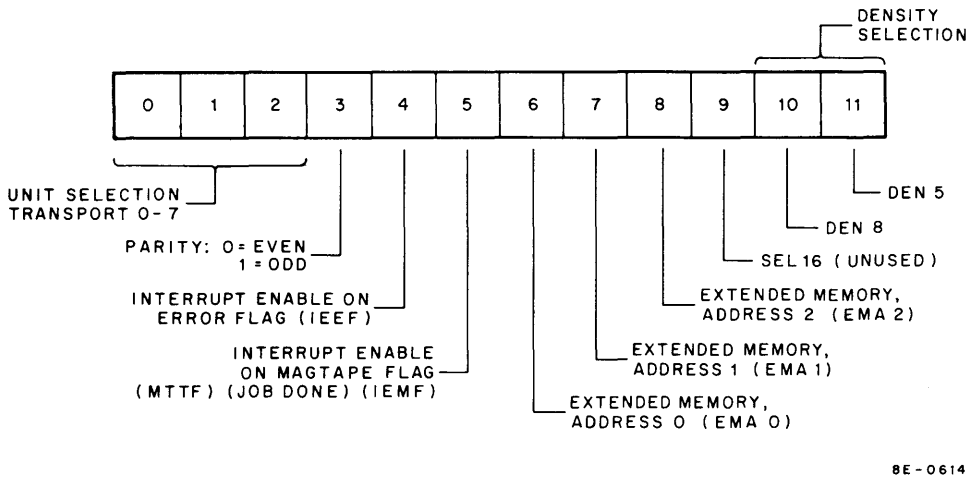


Figure 7-2 Contents of Command Register

7.3.2.1 Buffered Command Register (BCM) – The Buffered Command Register is loaded with SEL 0 through SEL 2 when LBCM is asserted by the control logic. The output of BCM (B SEL 0 through B SEL 2) is compared with SEL 0 through SEL 2 to determine when a new transport has been selected by the program. If the program selects a new transport, CHG TRANS is asserted to inform the controller that a new transport has been selected. LBCM is asserted when the following conditions exist:

1. The CHG TRANS flip-flop is set and the Rewind Status from the selected transport is asserted.
2. CLR ALL is asserted.
3. At TP4 time, if any one of the following conditions exist:
   a. C TUR L asserted.
   b. C SDWN L asserted.
   c. C SELR L negated.

7.3.3 Function Register

The Function Register (Figure 7-3) is loaded from the AC by an LFGR instruction. The three most significant bits (F0–2) are decoded by function decoders in the M8321 Output Control module and the TM8-E M8322 Control module to select the following DECmagtape functions.

Offline	Selected transport is taken OFFLINE and rewound to beginning of tape (BOT).
Rewind	The selected transport rewinds to BOT at 75 in./sec and stops.
Read	Data is transferred from tape to memory in the forward direction only.
Read/Compare	Data read from the tape is compared to data in core memory; if there is a comparison error, the Current Address (CA) Register stops incrementing and the CA Register holds the memory address in error at the end of the operation.

*0–1 for TM8-M.

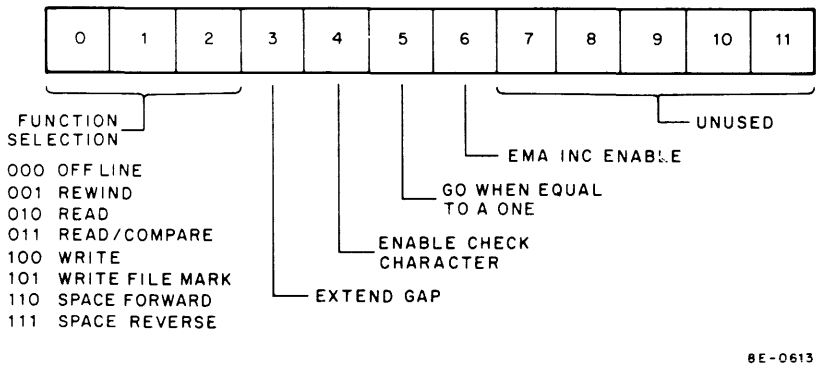


Figure 7-3 Contents of Function Register

Write	Data is written on tape in the forward direction only.
Write End-of-File	The transport leaves a 3-inch (7.62 cm) gap and writes a File Mark that consists of one character followed by three character spaces and an LRC character.
Space Forward	The transport moves forward, at 12.5 ips, the number of records specified by the Word Count (WC) Register (Paragraph 7.3.5). If File Mark is encountered, the transport stops at IRG; if EOT is encountered, the transport stops at the next IRG.
Space Reverse	The transport spaces in reverse, at 12.5 ips, the number of blocks specified by the WC Register. If at the beginning of tape (BOT) a File Mark is encountered, the tape stops.

The remaining bits of the Function Register enable the following operations if they are set by a 1 from the AC.

Extended Gap	If bit 3 is a 1, there is a 3-inch (7.62 cm) gap between records. This bit is used only during write functions.
Enable Check Character	If bit 4 is a 1 and a 9-track transport is selected, the LRC and CRC are transferred to memory at the end of a record during read operations. This operation is accomplished by executing two more data breaks after the WC Register overflows. Record Length Incorrect is disabled at this time.
Go	When bit 5 is a 1, the controller asserts GO, sets CNTL BSY (Control Busy), generates PRESET, and if no illegal functions exist, SET is asserted to start an operation. A GO command is issued to the transport if it is ready (TUR is true, and SELECT REMOTE is low).
EMA INC Enable	If bit 6 is a 1, the EMA bits in the Command Register and the CA Register are used as a 15-bit register to address the PDP-8 core memory as a block instead of in 4K segments.
Continuous Operation	The MTTF (JOB DONE) signifies the end of a specified operation. If an LFGR instruction is desired immediately, prior to TUR, this instruction may be executed by the program.

7.3.4 Current Address Register

The CA Register is loaded from the AC by an LCAR instruction with a memory address that is one location less than the desired starting memory location. The CA Register is incremented before each data transfer to sequentially address a block of memory during a data transfer operation. The contents of the CA Register are placed on the MA lines during a single cycle data break to address memory.

7.3.5 Word Count Register

The WC Register counts the number of words in a block of data transferred to or from memory by the TM8-E. The 2s complement of the number of words to be transferred is loaded into the WC Register by an LWCR instruction at the beginning of a data transfer. The WC Register is incremented before each data character is transferred until the WC Register contains all 0s, causing an OVERFLOW. When the WC Register overflows, data transfer is stopped. This register is also used in spacing operations to count records to be spaced over.

7.4 M8323 TRANSPORT STATUS AND CONTROL MODULE

The TM8-E transport status and control logic contains the majority of the Main Status Register, the second Status Register, the error detection logic (ERROR flag), an illegal function detection logic, and receives read data (RD0–RD7) from the TS03 master before it is applied to the Data Register.

7.4.1 Main Status Register

The Main Status Register (Figure 7-4) retains transport status information that is transferred to the AC by an RMSR instruction for evaluation by the program.

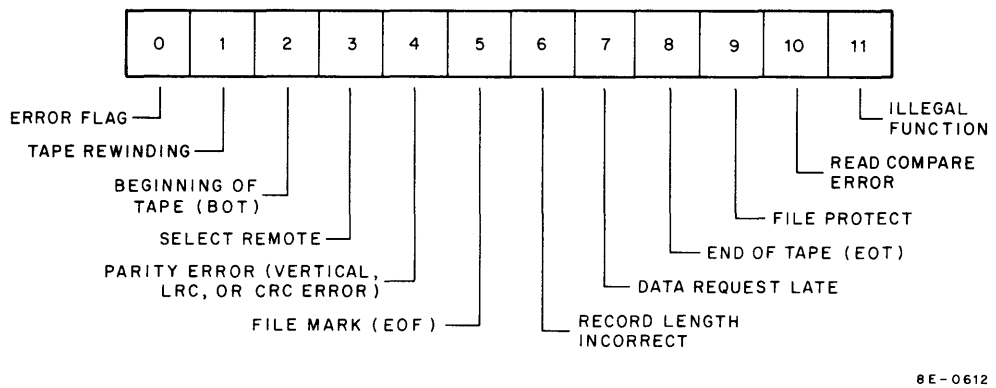


Figure 7-4 Contents of Main Status Register

7.4.2 Second Status Register

The Second Status Register (Figure 7-5) retains additional transport status information that is transferred to the AC by an RFSR instruction for evaluation by the program.

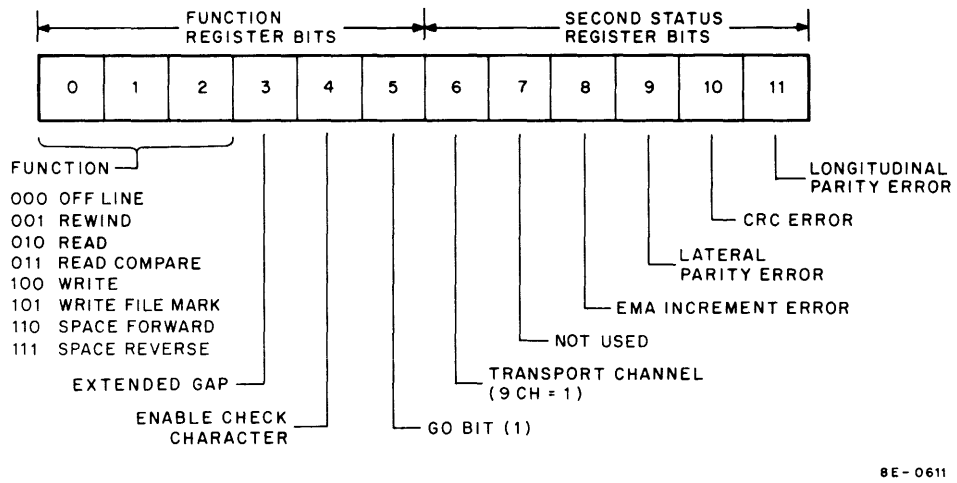


Figure 7-5 Contents of Function and Second Status Register

7.4.3 Error Flag

The Error flag is set by any one of the following error conditions:

End of Tape (EOT)
Read/Compare (R/C) ERROR
Parity Error
Beginning of Tape (BOT)
EMA 7 INC ERR
Record Length Incorrect
Data Late
Illegal Function
File Mark

7.4.4 Illegal Function Detection

The Illegal Function flag sets, setting the Error flag, if any of the following are attempted:

1. A rewind is attempted when tape is at BOT.
2. A space reverse is attempted when tape is at BOT.
3. An attempt is made to select other than 800 bpi density on 9-track transports.
4. An attempt is made to read after write on the same transport.
5. IOTs are executed to load the Data Buffer Register, Command Register, or Function Register while the control is busy.

6. Issue a write or write File Mark to a tape transport with the write ring removed.

7. An attempt is made to start an operation when the following conditions exist:

   a. CHG TRANSPORT L is true.
   b. TUR H is true.
   c. PRESET is true.

7.4.5 PRESET and SET Pulse Generator

PRESET is a fixed delay which is generated to allow adequate time for interrogation of the control to check for errors and illegal functions prior to asserting the SET pulse. If there are no illegal functions or errors, the SET pulse is asserted, thus asserting the C SET H signal to the tape transport and starting tape motion.

7.4.6 Control Busy (CNTL BSY)

CNTL BSY is set when the GO bit is issued to indicate that an operation is pending.

7.5 M8322 CONTROL AND DATA BREAK MODULE

The M8322 Control and Data Break module comprises the data break control logic, a control function decoder, and the interrupt logic.

7.5.1 Data Break Control Logic

The data break control logic allows the TM8-E to transfer large blocks of data between the TS03 Master and memory. When the TM8-E asserts BRK RQST, a priority check is made by the controller. A priority network on the M8322 module is compared with priorities of other peripherals requesting a data break and, if the TM8-E has the highest priority, the break control allows the TM8-E to assert the break control lines. This action enables the TM8-E to assume control of the CP Major Register gating and to address memory using the current address logic and data break control logic. When BRK RQST is granted by the TM8-E, data is transferred from the TM8-E Data Register to the Data Bus (read) or from the MD lines to the M8321 Output Control module (write or read/compare). The TM8-E is capable of one Single Cycle Data Break approximately every 100 μs until a complete record is transferred to or from memory. The CRC and LRC characters are also transferred to memory during a read operation if the ENABLE CHECK CHARACTER bit in the Function Register is set.

7.5.2 Function Decoder

The control function decoder decodes FR0–FR2 from the Function Register and generates the same function as the output control function decoder on the M8321 Output Control module (Paragraph 7.2.2). The outputs of this function decoder are applied to the control logic on the control module. The FR0–FR2 function bits are applied to the control function decoder from the Function Register.

7.5.3 Interrupt Logic

The interrupt logic on the TM8-E control module generates an interrupt request (INT RQST) when the following conditions exist (Table 7-1):

1. Bit 4 in the Command Register (IEEF) is set (1) and the Error flag is set.
2. Bit 5 in the Command Register (IEMF) is set (1) and the Job Done flag (MTTF) is set.

Table 7-1
Command Register Contents and Function

Bit No.			Function
Bits 0, 1, and 2			
SEL 0 (Bit 0)	SEL 1 (Bit 1)	SEL 2 (Bit 2)	
0	0	0	Transport 0
0	0	1	Transport 1
0	1	0	Transport 2
0	1	1	Transport 3
1	0	0	Transport 4
1	0	1	Transport 5
1	1	0	Transport 6
1	1	1	Transport 7
			TM8-M System has a maximum of two transports.
Bit 3			0 = Even parity; 1 = Odd parity
Bit 4			If bit 4 is a 1, enable interrupt Error flag.
Bit 5			Enable interrupt on JOB DONE (MTTF) if bit 5 is a 1.
Bits 6, 7, and 8			Extended memory address (EMA), these bits determine which memory field the controller uses for data transfer operations during a Data Break. Function Register bit 6 (Table 8-1) determines if the EMA address is to be incremented or used in the Wrap-around mode.
Bit 6 (EMA 0)	Bit 7 (EMA 1)	Bit 8 (EMA 2)	
0	0	0	Field 0
0	0	1	Field 1
0	1	0	Field 2
0	1	1	Field 3
1	0	0	Field 4
1	0	1	Field 5
1	1	0	Field 6
1	1	1	Field 7
Bit 9			Reserved for future use.

Table 7-1 (Cont)
Command Register Contents and Function

Bit No.		Function
Bits 10 and 11		Density bits, these bits select the density for tape transport operation and are referred to as Den 8 (bit 10) and Den 5 (bit 11).
Bit 10 Den 8	Bit 11 Den 5	
0	0	200 bpi, 7-track (Not used)
0	1	556 bpi, 7-channel (Not used)
1	0	800 bpi, 7-channel*
1	1	800 bpi, 9-channel

*This mode is also referred to as Core Dump Mode. When this command is issued to a 9-track transport, zeros are written on tracks 0 and 1 of the DECmagtape and the 9-track transport operates as a 7-track transport.

CHAPTER 8
PROGRAMMING INFORMATION

8.1 INTRODUCTION

This chapter describes the instructions used to program the TM8-E and the register bits associated with each instruction. The single cycle data break data transfer operation is also described. Programming notes and examples are provided.

8.2 INSTRUCTIONS AND REGISTER BITS

The following instructions are used to program the TM8-E. Refer to the appropriate table for the register bits associated with each instruction.

Load Word Count Register (LWCR)

Octal Code: 6701

Operation: Loads the WC Register with the contents of the AC (Figure 8-1) and clears the AC. The WC Register should not be loaded when the control is busy. If the register is loaded during CNTL BSY, data reliability and tape compatibility are not ensured. The WC Register is loaded with the 2s complement of the number of words to be transferred or number of blocks to be spaced. The WC Register is incremented at TP1 of a data break cycle during data transfers, at LRCS during a space forward, or at the first word of a record during a space reverse operation.

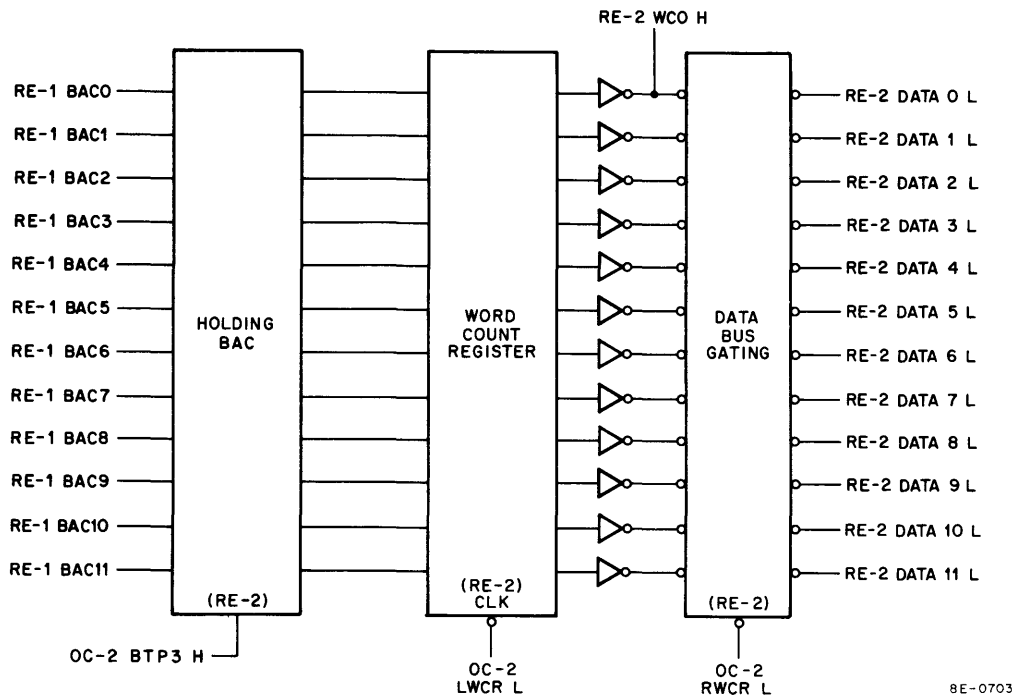


Figure 8-1 LWCR and RWCR Instruction Data Flow

Clear Word Count Register (CWCR)

Octal Code: 6702

Operation: Clears the WC Register. This instruction is used primarily in maintenance operations and should never be used during CNTL BSY.

Load Current Address Register (LCAR)

Octal Code: 6703

Operation Loads the CA Register with the contents of the AC (Figure 8-2) and clears the AC. The CA Register is loaded to one less than the memory address of the first word to be transferred. If this instruction is executed during CNTL BSY, one of the following occurs:

1. In the Wrap-around Modes (Function bit 6 = 0), the location of the data transfer cannot be ensured within the selected memory field.

2. In the EMA INC ENABLE Mode (Function bit 6 = 1), the location of the data transfer cannot be ensured within memory.

The CA Register is incremented at each BRK RQST.

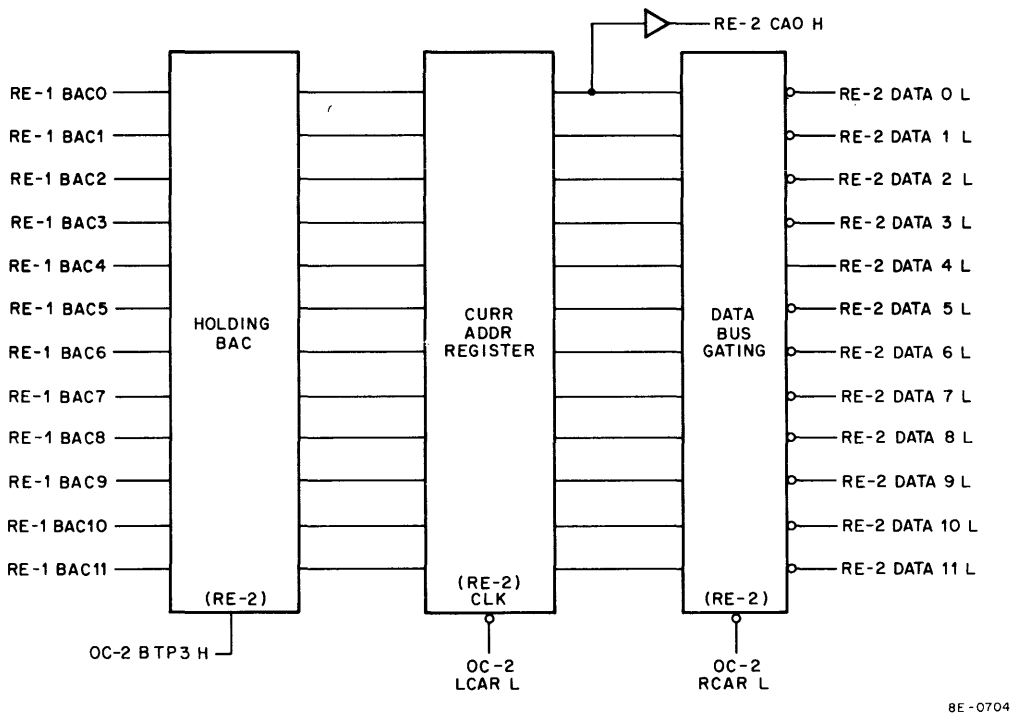


Figure 8-2 LCAR and RCAR Instruction Data Flow

Clear Current Address Register (CCAR)

Octal Code: 6704

Operation: Clears the CA Register. This instruction is used primarily for maintenance and should never be used during CNTL BSY.

Load Command Register (LCMR)

Octal Code: 6705

Operation: Loads the Command Register with the contents of the AC and clears the AC (Figure 8-3). This instruction must not be issued during CNTL BSY. The LCMR instruction selects tape transport, Parity Mode, memory field, recording densities, and enables or disables interrupts (Table 7-1 and Figure 7-2).

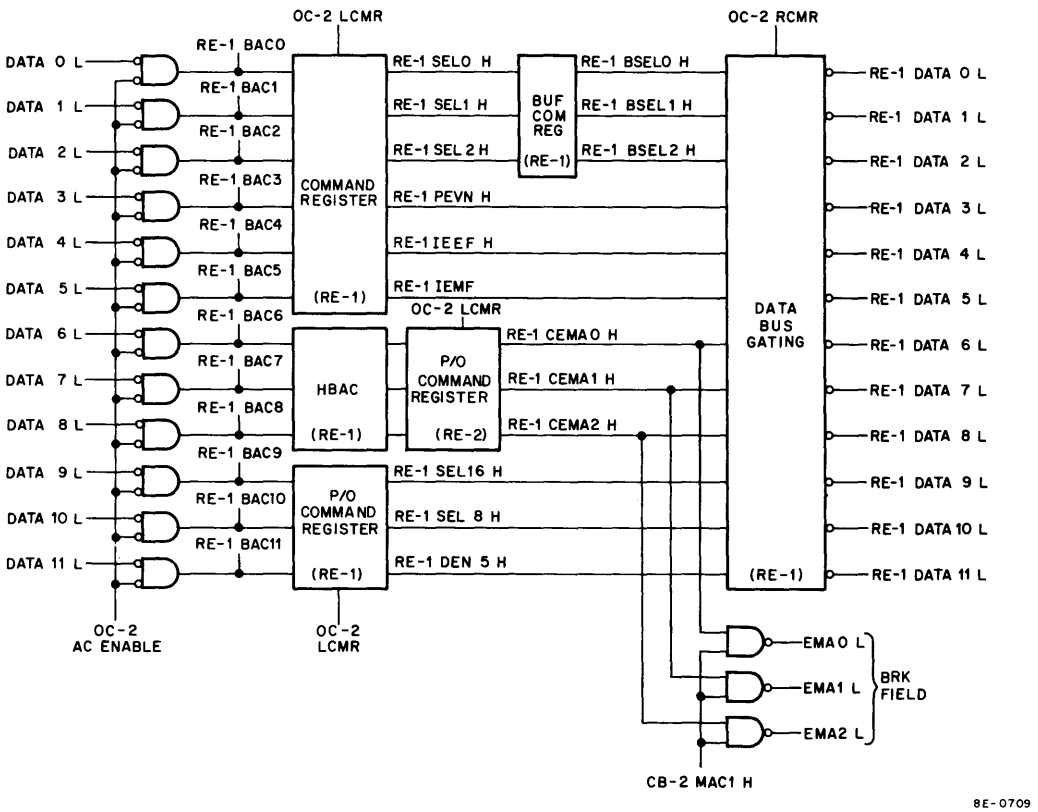


Figure 8-3 LCMR and RCMR Instruction Data Flow

Load Function Register (LFGR)

Octal Code: 6706

Operation: Loads the Function Register with the contents of the AC and clears the AC (Figure 8-4). The Function Register is the last register loaded because it contains the GO bit. This instruction determines the function the transport is to perform (Table 8-1 and Figure 7-3).

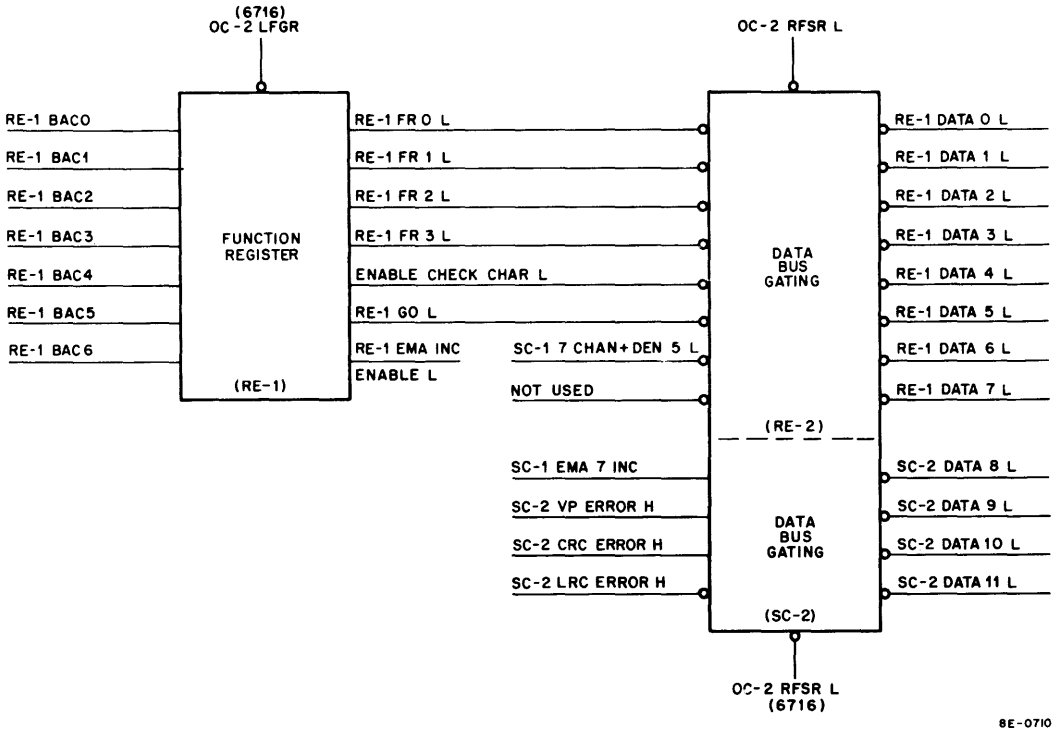


Figure 8-4 LFGR and RFSR Instruction Data Flow

Table 8-1
Function Register Contents and Functions

Bit No.			Function
Bit 0, 1, and 2			Function Selection: These bits determine the function the transport is to perform.
Bit 0	Bit 1	Bit 2	
0	0	0	Offline: The selected transport is taken offline and rewound to BOT. The MTTF is set when the transport responds to this function and the controller can select and use another transport. The transport must be manually reset to the on-line state. The WC and CA Registers need not be loaded.
0	0	1	Rewind: The transport rewinds at high speed (75 in/sec) to BOT and stops. The MTTF is set when the transport responds to the Rewind function. The controller can select and use another transport. The WC and CA Registers need not be loaded.

Table 8-1 (Cont)
Function Register Contents and Functions

Bit No.			Function
Bit 0, 1, and 2 (Cont)			
Bit 0	Bit 1	Bit 2	
0	1	0	Read: Data is transferred from the tape to memory in the forward direction only. All registers must be loaded.
0	1	1	Read/Compare: Tape data is compared to data in core memory. All registers must be loaded. If there is a comparison error, CA incrementation ceases, the R/C ERROR bit is set, and tape motion continues to the end of the record. The CA Register contains the address of the word that produced the error.
1	0	0	Write: Data is written on the tape in the forward direction only. All registers must be loaded. The write function is controlled by WC OVERFLOW (which disables the write); the transport writes the appropriate check characters to end the block.
1	0	1	Write End-of-File (File Mark): The transport writes the File Mark, which consists of a one word record. The CA and WC Registers need not be loaded.
1	1	0	Space Forward: The tape moves forward at 12.5 ips the number of records specified by the WC Register, or until a File Mark is read. If EOT is read, space forward stops at the first interrecord gap. The CA Register need not be loaded for space forward to occur.
1	1	1	Space Reverse: The tape moves in the reverse direction at 12.5 ips the number of blocks specified by the WC Register, or until a File Mark or BOT marker is read. The CA Register need not be read during a space reverse.
Bit 3			Extended Gap: When bit 3 is a 1, the transport writes with an additional 3-inch (7.62 cm) gap between records.

Table 8-1 (Cont)
Function Register Contents and Functions

Bit No.	Function
Bit 4	Enable Check Character: When this bit is set (1), it allows the check characters to be read into the computer during a read function. When the word count overflows, this bit allows two breaks for the CRC and LRC to be transferred to memory. If a record length incorrect error occurs, the check character is considered bad and is not used. This bit is used primarily for error correction.
Bit 5	Go: This bit causes the controller to issue a set command to the transport when the transport is capable of accepting it. The set command is not issued if the specified function is illegal.
Bit 6	EMA INC Enable: If this bit is not set (0), the TM8-E (like all other PDP-8 data break options) treats the extended memory the same way, i.e., each 4K block is used in a Wrap-around Mode. If this bit is set (1), the extended memory is treated as a continuous memory rather than 4K blocks. When the last location in one field is reached, the EMA bits are incremented and the transfer continues in the next field; i.e., if a word is placed in Field 2, location 7777, the following word is placed in Field 3, location 0000 if the EMA increment bit is set. If bit 6 is not set, the word is placed in Field 2, location 0000. In both modes of operation, the current address is set to one less than the first location to be accessed. In EMA increment mode, the 12-bit CA Register and the three EMA bits are treated as one 15-bit register with the EMA bits most significant. For example, to access Field 2, location 20, load EMA = 2 and CA = 0017; to access Field 2, location 0, load EMA = 1 and CA = 7777. If Field 7 is selected, the EMA cannot increment, but wraps around in Field 7 and an EMA 7 INCREMENT ERROR occurs.

Load Data Buffer Register (LDBR)

Octal Code: 6707

Operation: Loads the Data Buffer Register with the contents of the AC, clears the AC, and sets the MTTF flag (Figure 8-5). This instruction is used for maintenance purposes.

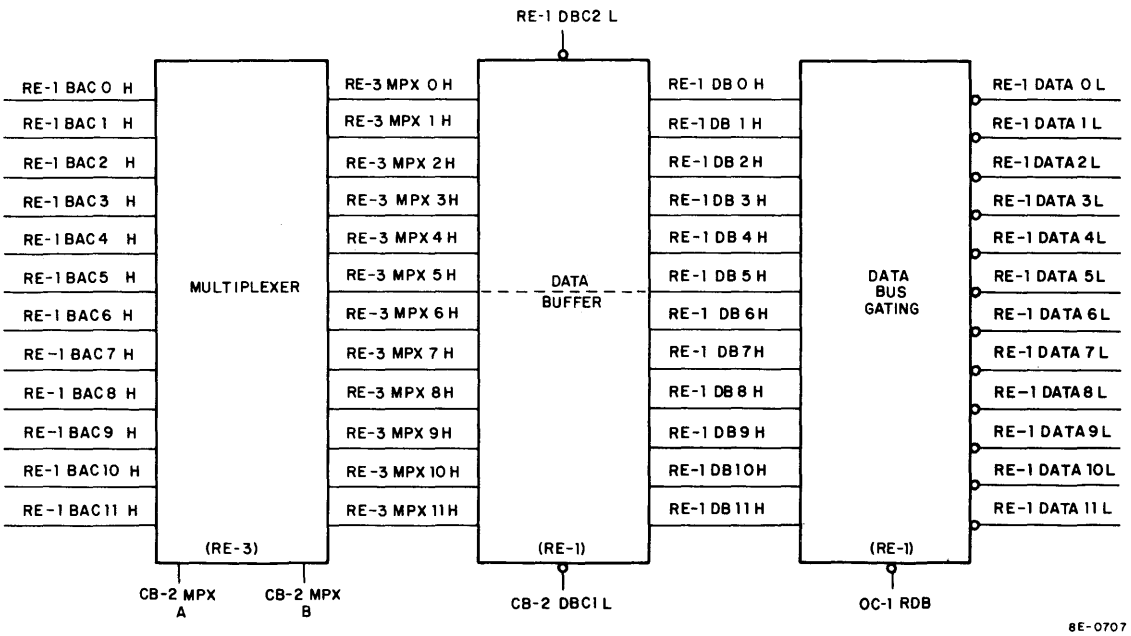


Figure 8-5 LDBR and RDBR Instruction Data Flow

Read Word Count Register (RWCR)

Octal Code: 6711

Operation: Clears the AC and transfers the contents of the WC Register into the AC (Figure 8-1). This instruction is used primarily for maintenance, but it can also be used during error check routines.

Clear Transport (CLT)

Octal Code: 6712

Operation: Clears the transport master registers and all TM8-E registers and flags.

Read Current Address Register (RCAR)

Octal Code: 6713

Operation: Clears the AC and transfers the contents of the CA Register to the AC (Figure 8-2). This instruction is used primarily for maintenance, but it can be used for error check routines.

Read Main Status Register (RMSR)

Octal Code: 6714

Operation: Clears the AC and transfers the contents of the Main Status Register to the AC (Figure 8-6). The 12-bit Status Register contains the status of the transport and control logic (Table 8-2 and Figure 7-4)..

Table 8-2
Main Status Register Contents and Indications

Bit No.	Status Indication
0	Error: The Error flag interrupts the processor if bit 4 in the Command Register is set (1). An ILLEGAL FUNCTION or SELECT ERROR sets the MTTF flag immediately and stops data break operations. The following errors, if they occur during any operation, set the Error flag after the MTTF flag is set. BOT EOT READ/COMPARE ERROR Parity Error (VPE, CRCE, or LRCE) RECORD LENGTH INCORRECT File Mark (EOF) DATA LATE EMA 7 INCREMENT ERROR
1	Rewind Status (RWS): A 1 indicates the selected transport is rewinding.
2	Beginning of Tape (BOT): A 1 indicates the BOT reflective strip is sensed by the selected transport.
3	Select Remote: A 1 indicates the selected transport is not on-line.
4	Parity Error: A 1 indicates a longitudinal parity error, vertical parity error, or CRC error has been detected.
5	File Mark (FMK): A 1 indicates the selected transport has detected a File Mark during a write FMK, space, read, or read/compare operation.
6	Record Length Incorrect: A 1 indicates that during a read or read/compare operation, the record length was different from the contents of the WC Register. The WC Register is read to determine whether the record was long or short.
7	Data Request Late: A 1 indicates the computer failed to service the BRK RQST before the next data transfer to or from the transport.
8	End of Tape (EOT): A 1 indicates the EOT reflective strip has been sensed by the selected transport.
9	File Protect: A 1 indicates the selected transport has a write lockout ring removed, and no write functions are accepted.
10	R/C ERROR: A 1 indicates a comparison failure occurred during the read/compare function. The CA Register contains the address of the word that produced the error.

Table 8-2 (Cont)
Main Status Register Contents and Indications

Bit No.	Status Indication
11	A 1 indicates that one of the following Illegal Functions has been programmed. 1. Execution of LCMR, LFGR, or LDBR while the control is busy. 2. Specifying any density but 800 bpi for a 9-track transport. 3. A space reverse function when the transport is at BOT. 4. Read, read/compare, or space forward after a write or write end-of-file (WEOF) command on same transport. 5. Changing to transports that are not ready (TUR is false). 6. Attempting to rewind when tape is at BOT.

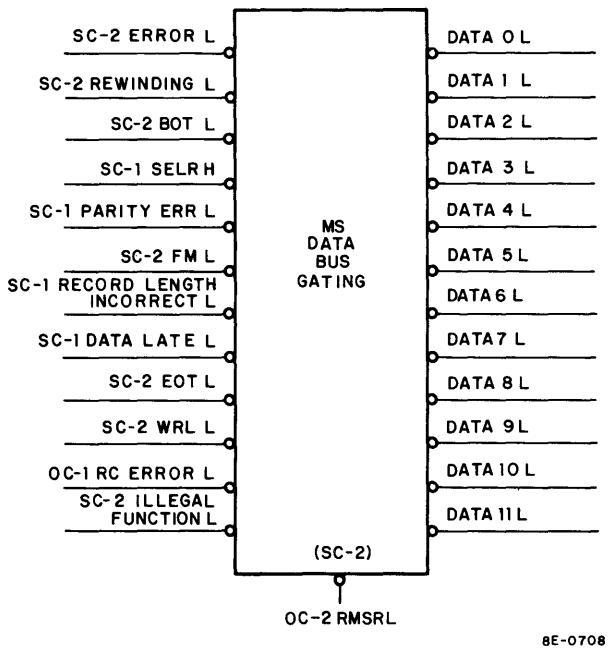


Figure 8-6 RMSR Instruction Data Flow

Read Command Register (RCMR)

Octal Code: 6715

Operation: Clears the AC and transfers the contents of the Command Register to the AC. The contents of the Command Register for this instruction are the same as that for the Load Command Register instruction shown in Table 7-1 and Figure 7-2.

Read Function Register and Second Status Register (RFSR)

Octal Code: 6716

Operation: Clears the AC and transfers the contents of the Function Register and Second Status Register to the AC (Figure 8-4). The contents of the Second Status Register and Function Register are shown in Table 8-3.

Table 8-3
Second Status Register Contents and Functions

Bit No.	Function
7	Not used.
8	EMA 7 INC ERROR: EMA 7 INC ERROR occurs if an attempt is made to increment the EMA from Field 7 to Field 0. The data wraps around in Field 7.
9	Vertical Parity Error (VPE): A 1 indicates that a VPE error has been detected. This bit is set only on the character that is bad and cleared by the next good character.
10	CRC Error (CRCE): A 1 indicates a CRC error has been detected.
11	Longitudinal Parity Error (LPCE): A 1 indicates that an LPCE has been detected.

Read Data Buffer Register (RDBR)

Octal Code: 6717

Operation: Clears the AC and transfers the contents of the Data Buffer Register to the AC (Figure 8-5). This instruction can be used in an error check routine to read the contents of the LRC Register.

Skip If ERROR Flag Is Set (SKEF)

Octal Code: 6721

Operation: Skip the next instruction if the Error flag is set.

Skip Control Not Busy (SKCB)

Octal Code: 6722

Operation: Skip the next instruction if the control is not busy. Control is busy when the transport is in a GO condition, control is not busy when MTTF is set at the End of Job (data transfer completed).

Skip Job Done (SKJD)

Octal Code: 6723

Operation: Skip the next instruction under following conditions.

1. When JOB DONE (MTTF) is set at LRCS time of a read, read/compare, write, or write File Mark operation.

2. At the IRG following EOT, FMK, or WCOV during space operations.

3. MTTF is set by OFFLINE function, SELECT ERROR, or REWINDING status.

4. MTTF is set by an LDBR (Load Data Buffer Register) instruction.

Skip if Tape Unit Ready (SKTR)

Octal Code: 6724

Operation: Skip the next instruction if TUR is true.

Clear All Registers and Flags (CLF)

Octal Code: 6725

Operation: Clear all TM8-E registers and flags if TUR is true. If TUR is false clear MTTF, Error flag, and Status Registers.

Check for Data Late Error (CKDL)

Octal Code: 6726

Operation: Force a DATA LATE error condition during a data transfer. This instruction is used only for maintenance (Paragraph 9.4.7).

Set Break Request (SBRM)

Octal Code: 6727

Operation: Set BRK RQST for one data break. This instruction is used for maintenance only.

8.3 SINGLE CYCLE DATA BREAK

The single cycle data break is used for data transfers between PDP-8 core memory and the TS03 DECmagtape transports (Figure 8-7). The concept of data transfers and the interrelationship of the data break interface are explained in Chapter 6 of the *PDP-8/E & PDP-8/M Small Computer Handbook,* 1972. Figure 8-8 is a timing diagram of the single cycle data break interface; reference this diagram during the discussion of the TM8-E functions and programming that follows. Data flow for the Core Dump Mode of operation is shown in Figure 8-9. TM8-E functions are illustrated in Figure 8-10.

NOTE

The programs and timing diagrams presented here are not necessarily the best or only way to program the TM8-E. They are shown to illustrate TM8-E functional operation and the interaction of functional groups of logic. The timing diagram referred to in the description of TM8-E functions is part of the TM8-E print set (Drawing D-TD-TM8-E-1).

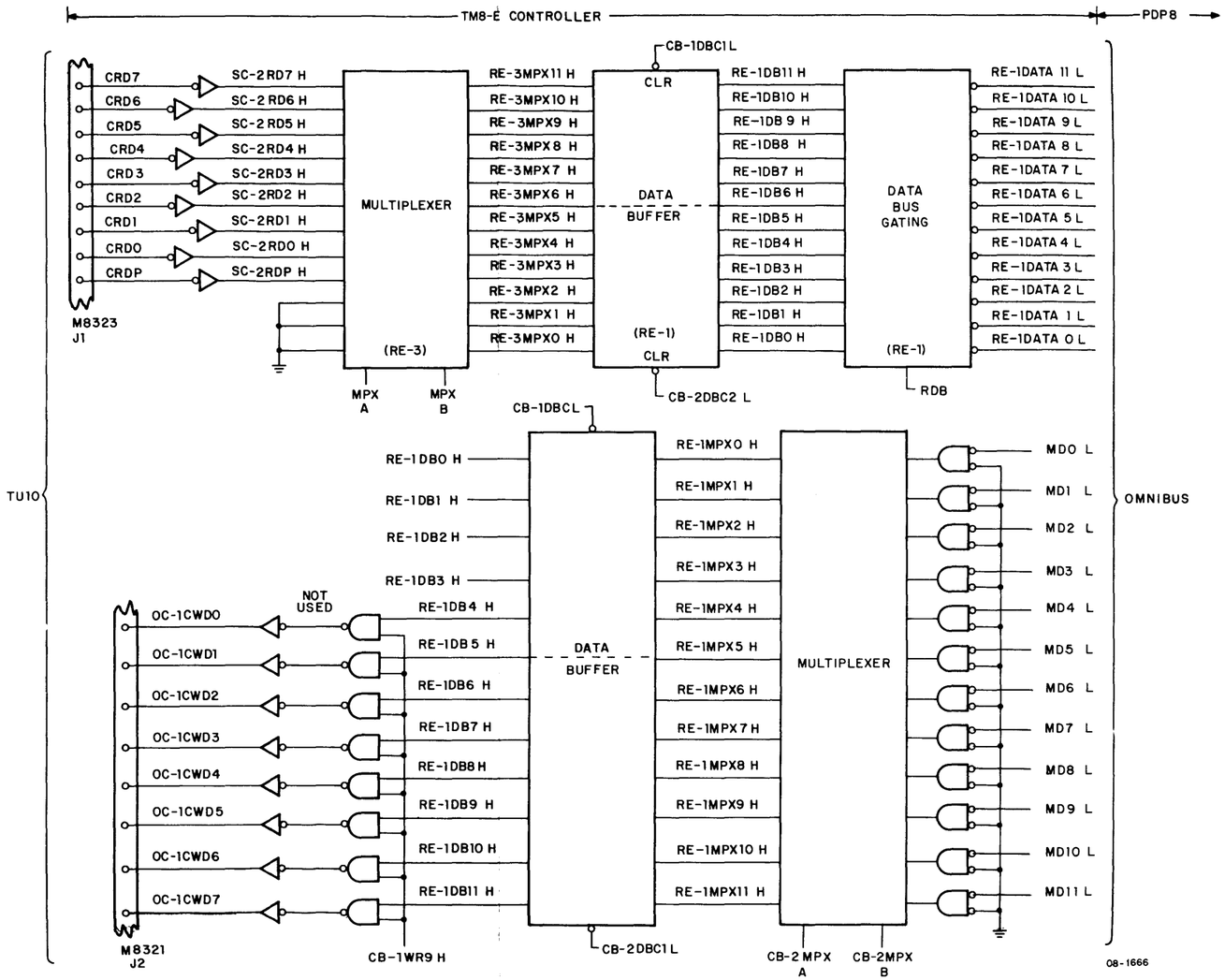


Figure 8-7 Single Cycle Data Break
Data Transfer Data Flow

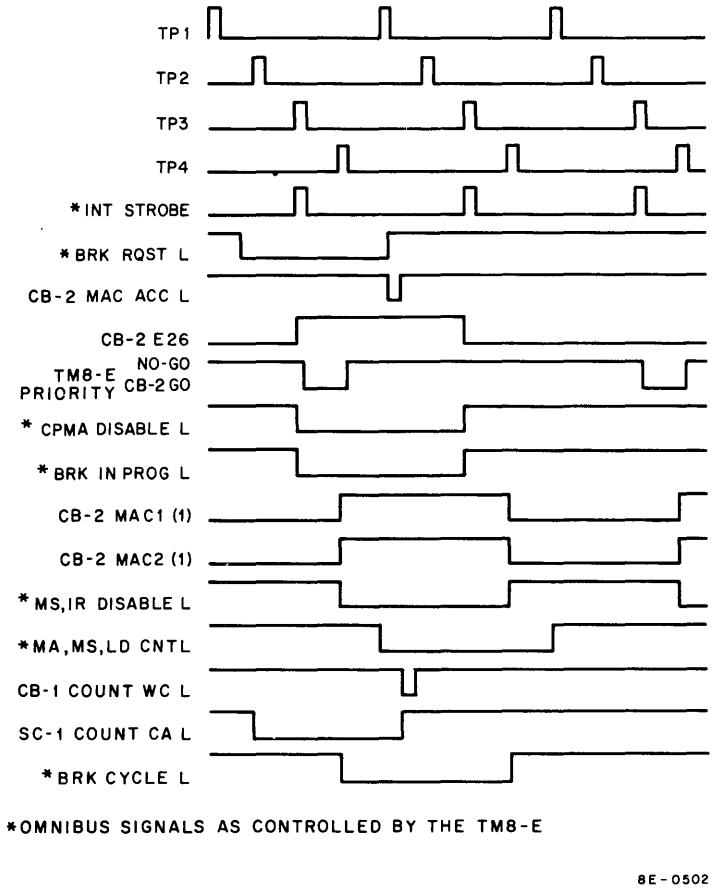


Figure 8-8 Single Cycle Data Break Timing Diagram

8.3.1 Signal Conventions

The following signal conventions are used in the TM8-E.

1. Interface signals. All signals that are used to interface the TM8-E with the TS03 are preceded by C, e.g.,C SET L. All signals applied to the TS03 are asserted when they are low (0.0 V); all signals from the TS03 are asserted when they are high (+3.0 V).

2. All signals on the TM8-E modules followed by L, e.g., SBRM L, are asserted (true) when they are 0 V. All signals followed by H, e.g., SEL 1 H, are asserted (true) when they are 3.0 V.

3. All signals on the TM8-E preceded by B, e.g., BTP3 L, are inverted signals or the outputs of holding registers, e.g., B SEL 0 H.

4. All signals on the TM8-E have a prefix to indicate their origin as shown in Appendix F.

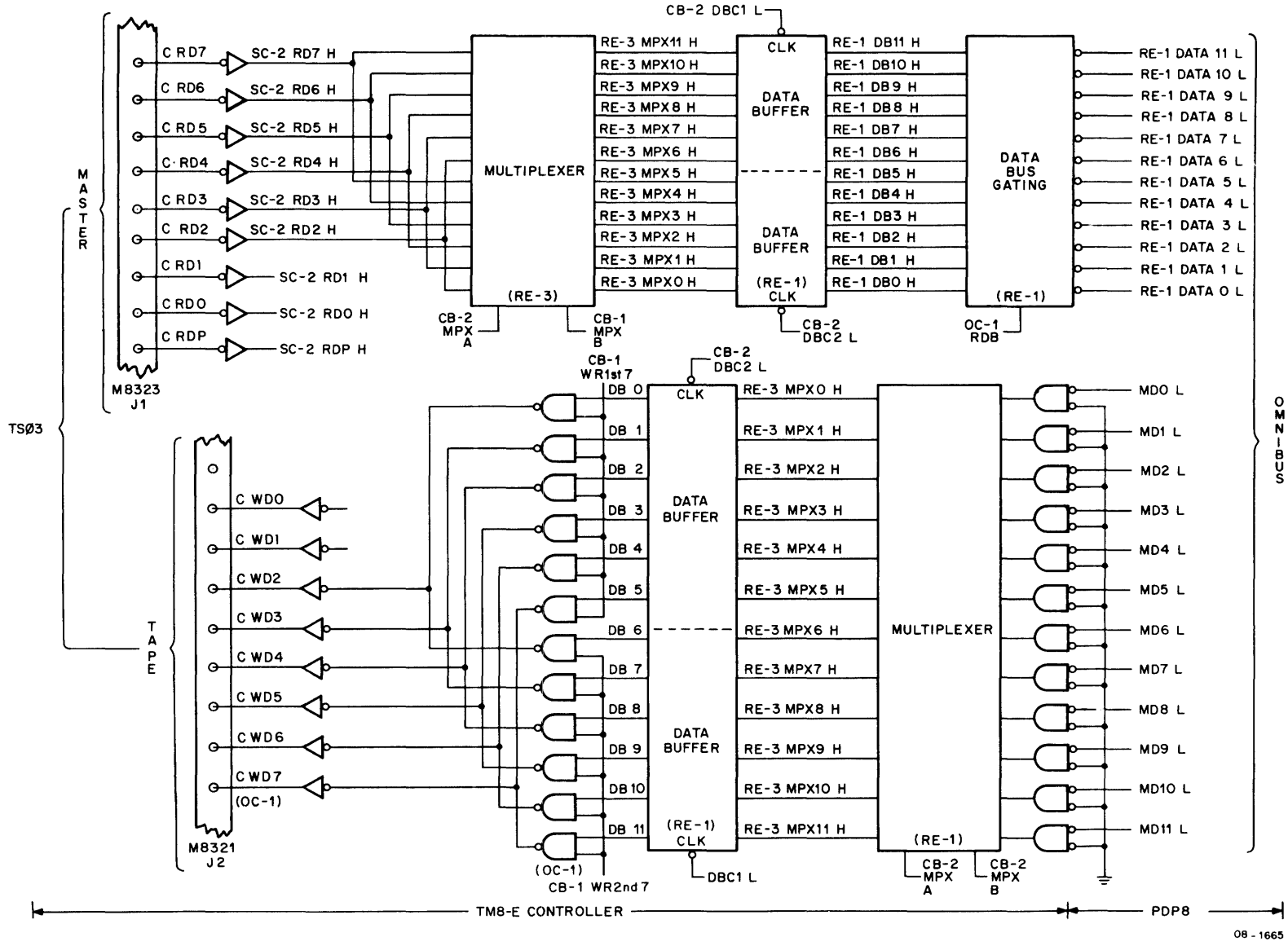


Figure 8-9 Core Dump Data Flow

Figure 8-9 Core ap Data Flow

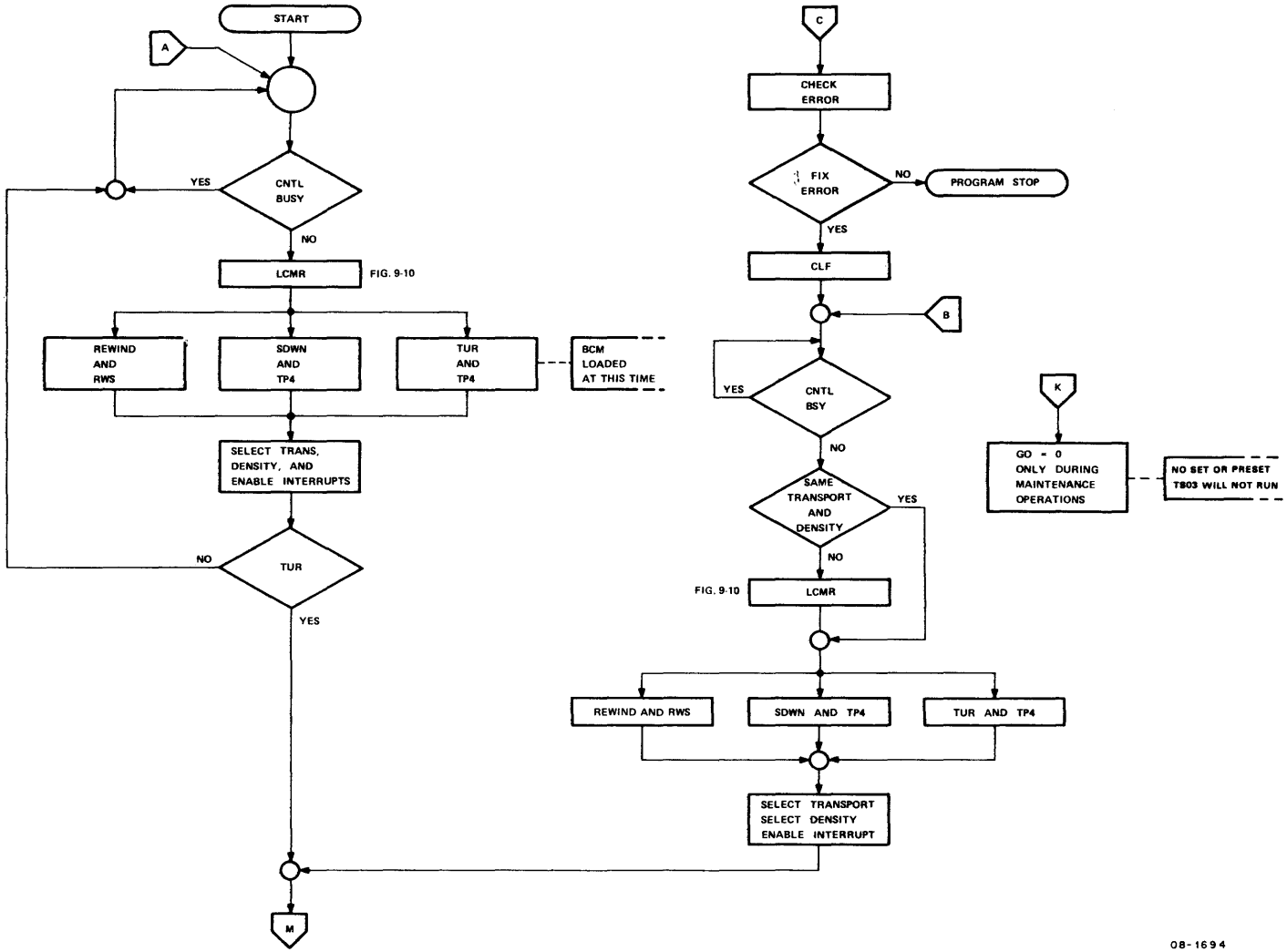


Figure 8-10 TM8-E Flow Diagram (Sheet 1 of 9)

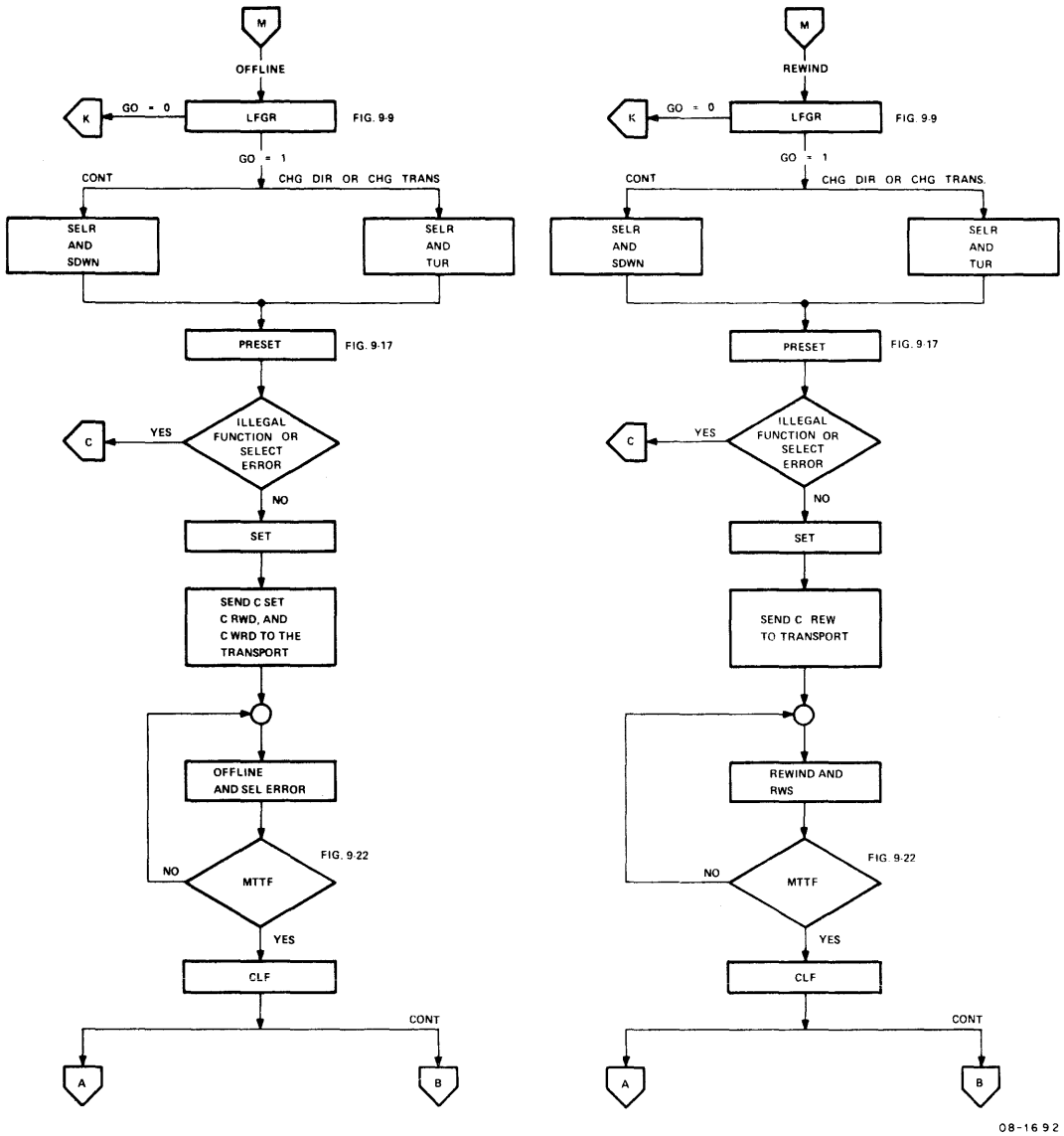


Figure 8-10 TM8-E Flow Diagram (Sheet 2 of 9)

8.3.2 Write Data

Data can be written on a DECmagtape only in the forward direction (see D-TD-TM8-E-1, sheets 7 and 8 for timing diagram). The CA Register must be loaded with the starting memory address minus one; the WC Register must be loaded with the 2s complement of the number of words to be transferred. The density and parity bits in the Command Register (Table 7-1) must be set to select tape density, parity mode, and tape unit. The write function is controlled by the WC Register such that when WCOV occurs, the data transfer stops. CB-3 MTTF is set when the LRC character passes under the read heads. Note that the WC, CA, and Command Registers must be loaded prior to the Function Register because the Function Register contains the GO bit, which initiates tape movement and sets SC-1 CNTL BSY (control busy). If any errors other than illegal functions or select errors occur during a write operation, the Error flag is set after MTTF is set. Operation may be continued on the same transport in the same direction immediately if the registers are reloaded following MTTF. A continuous operation may still be achieved when a change direction or change transport is encountered; however C TUR from the selected transport must be asserted.

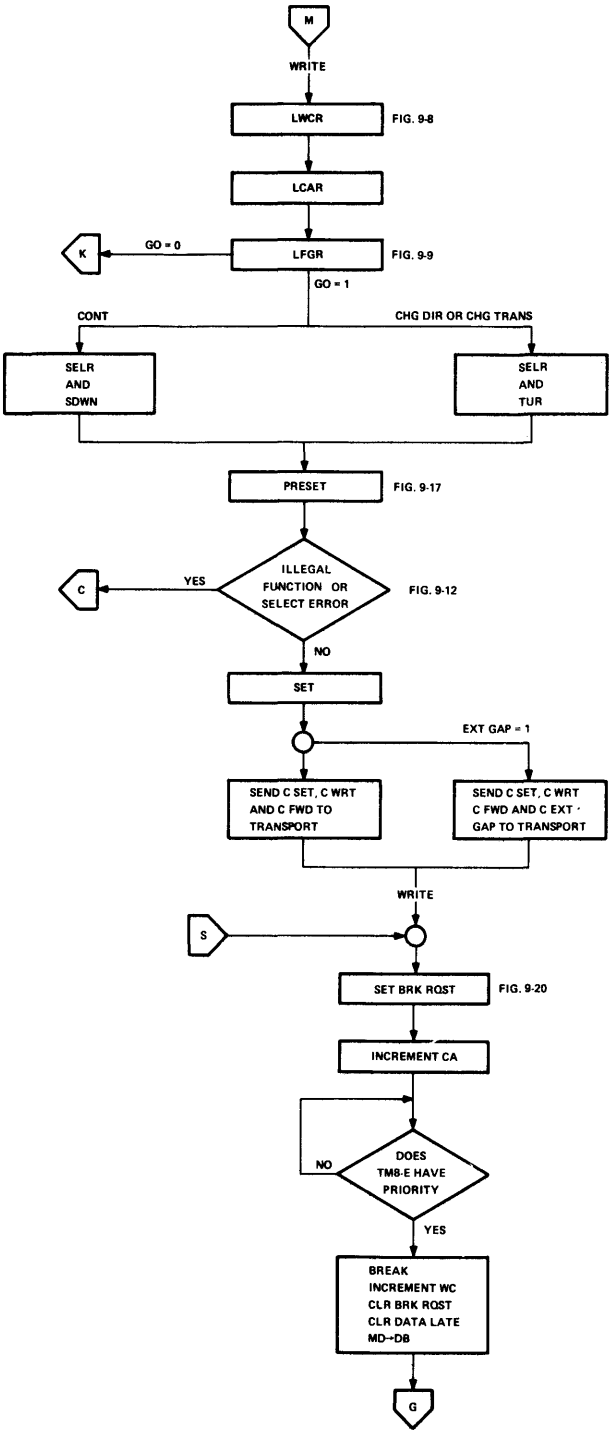


Figure 8-10 TM8-E Flow Diagram (Sheet 3 of 9)

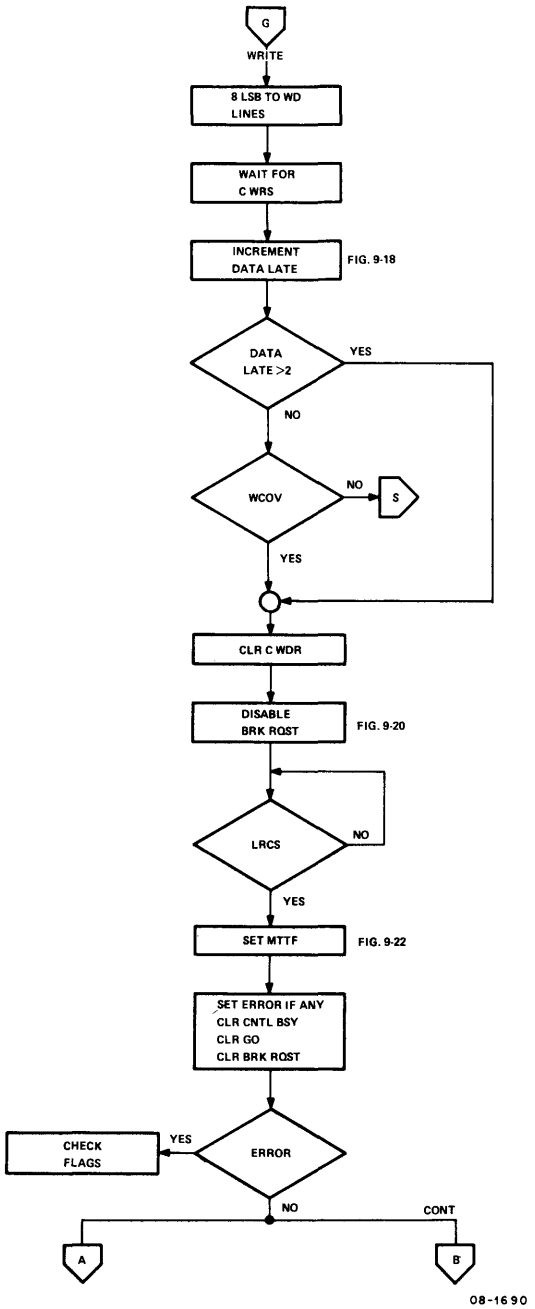


Figure 8-10 TM8-E Flow Diagram (Sheet 4 of 9)

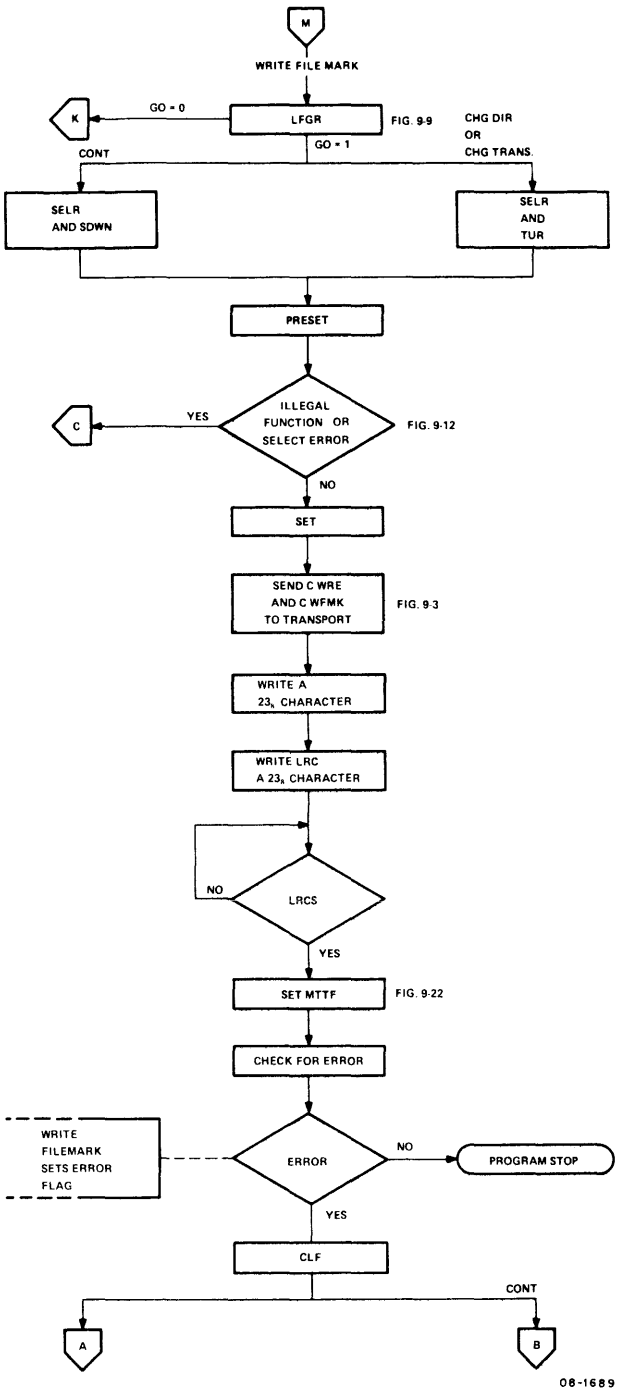


Figure 8-10 TM8-E Flow Diagram (Sheet 5 of 9)

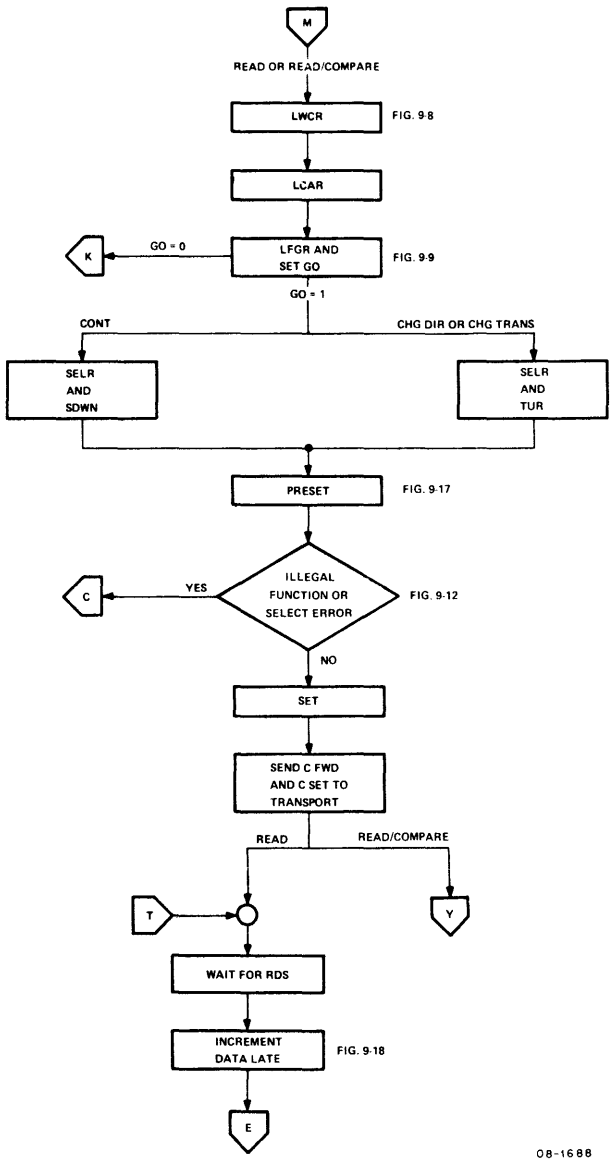


Figure 8-10 TM8-E Flow Diagram (Sheet 6 of 9)

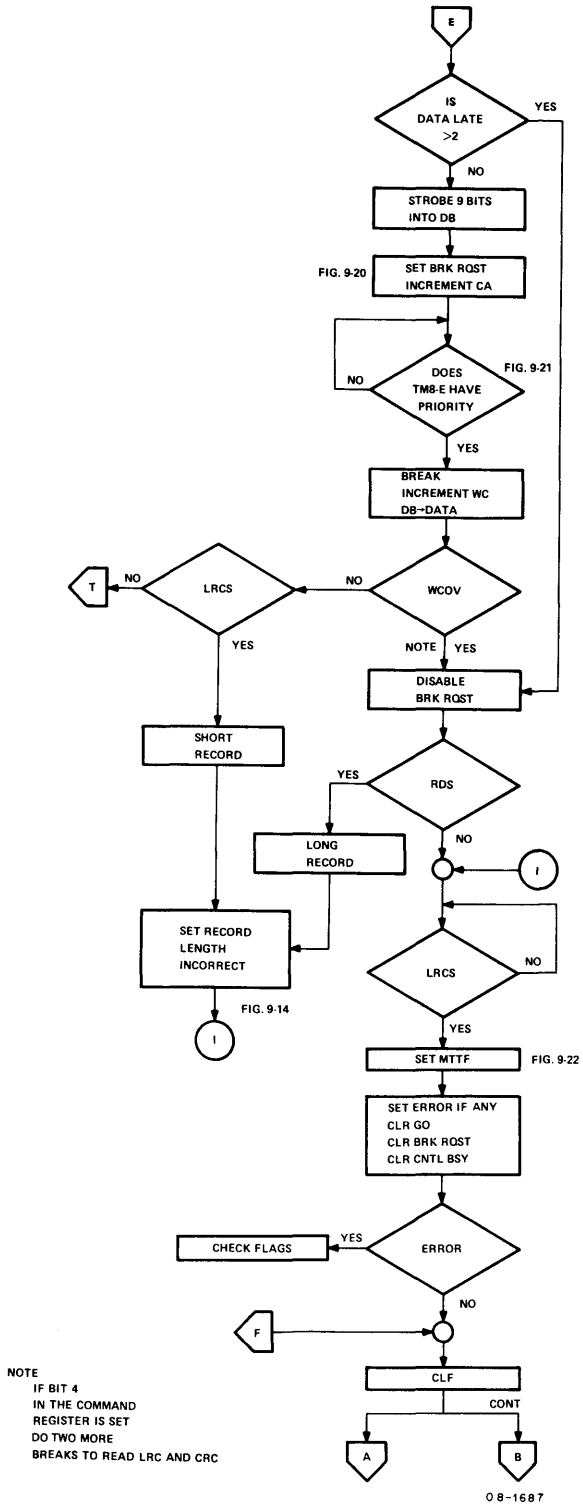


Figure 8-10 TM8-E Flow Diagram (Sheet 7 of 9)

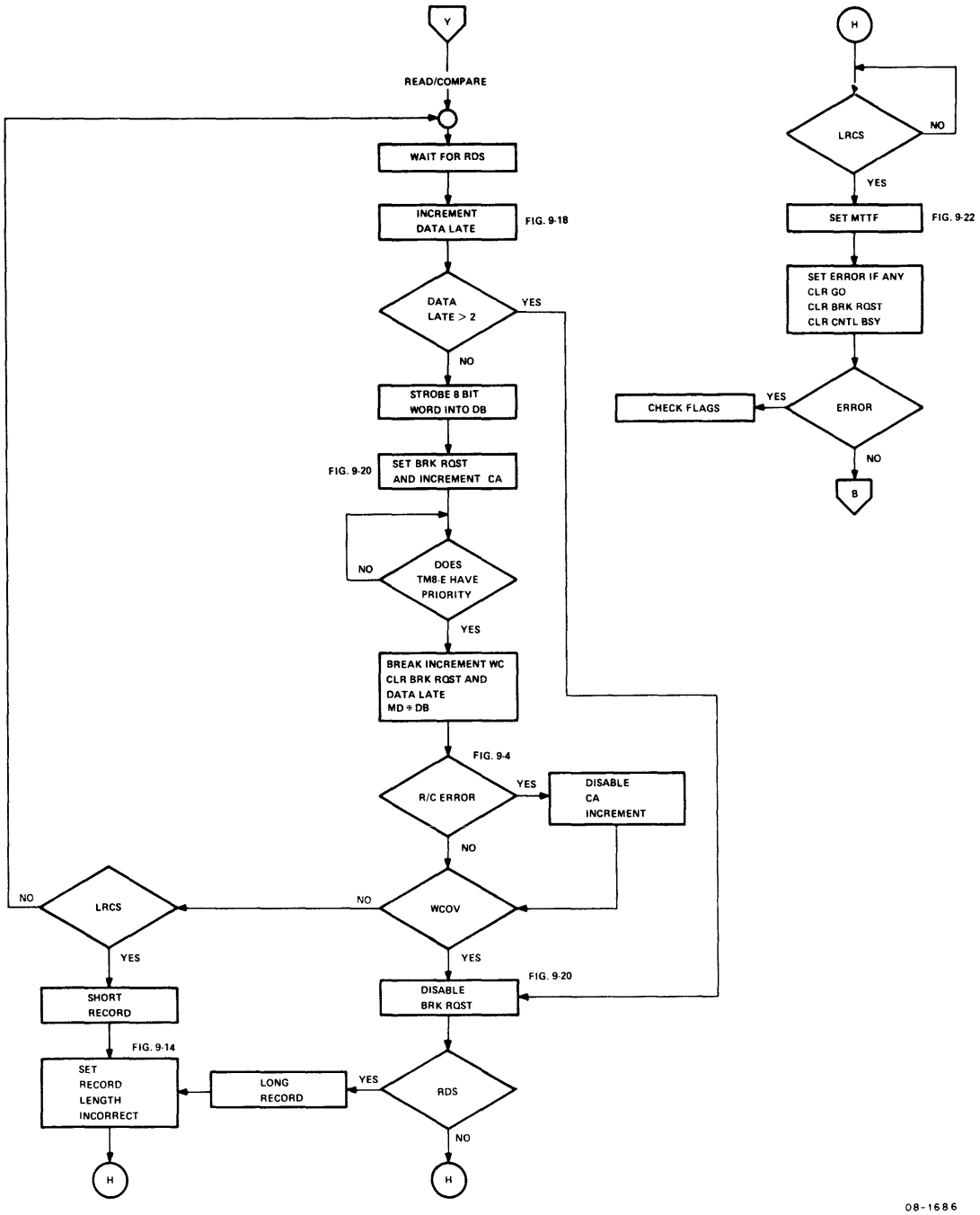


Figure 8-10 TM8-E Flow Diagram (Sheet 8 of 9)

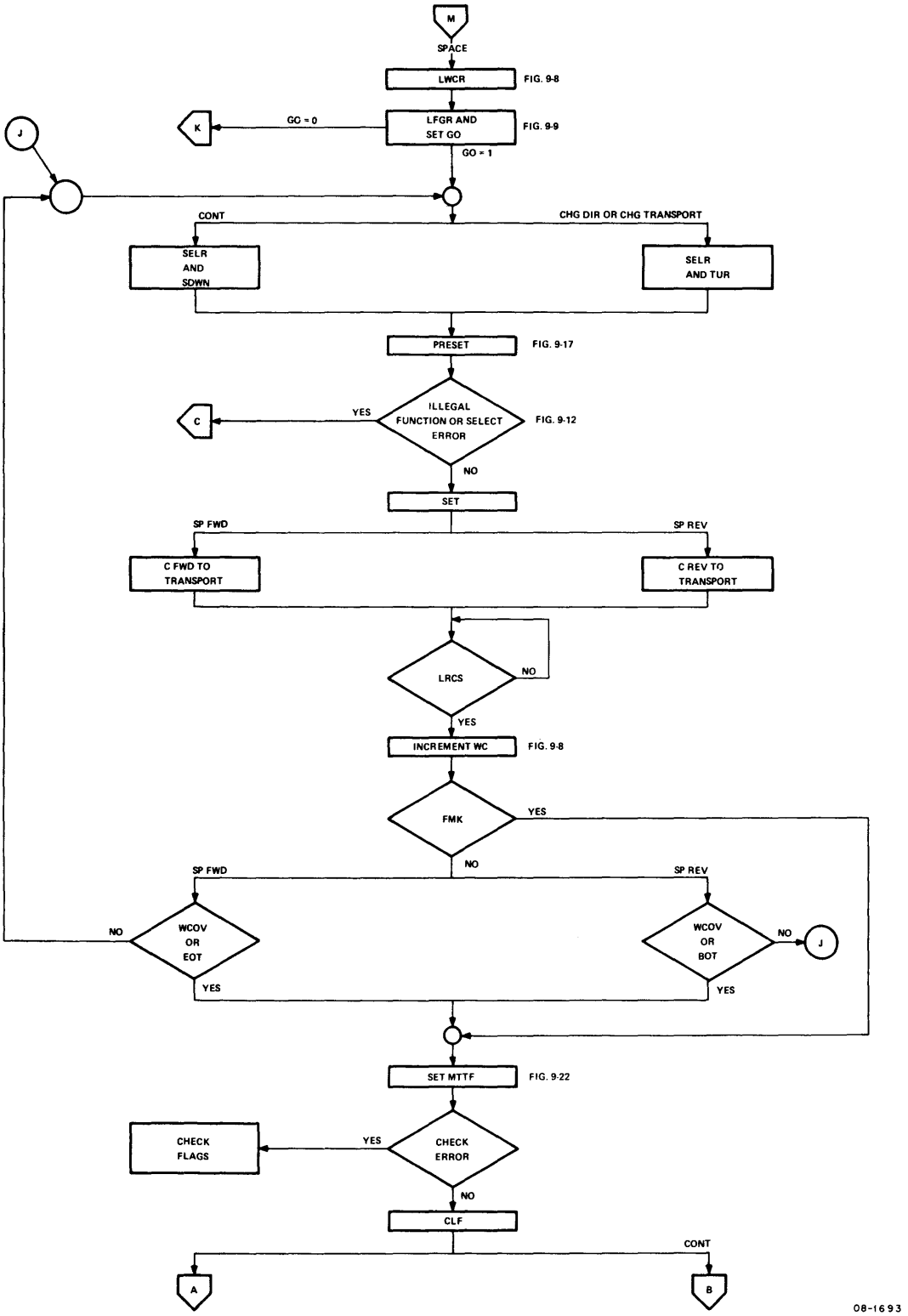


Figure 8-10 TM8-E Flow Diagram (Sheet 9 of 9)

8.3.3 Read Data

Records are read from a DECmagtape transport and transferred to memory only in the forward direction (D-TD-TM8-E-1, sheets 1 and 6 for timing diagrams). The WC, CA, and Command Registers must be loaded because they are for a write operation. Density tape unit, and parity must be selected; density and parity must be the same as they were when the data was written on tape. During a read operation, the number of words loaded into the WC Register (in 2s complement) is transferred to memory. If the WC Register is set to less than the actual record length, only the number of words in the WC are transferred. If the WC Register is greater than or equal to the actual record length, the entire record is transferred to memory. In either case, a record length incorrect error (SC-1 REC LNG INCORRECT) is generated for evaluation by the program. The WC and CA Registers contain the number of words read from tape and the address where the last word was stored. The contents of the WC Register can be checked by the program to determine the cause of error (record too long or too short).

Parity checks are made by the TS03 as data is read from tape. If any parity errors are detected, the SC-2 ERROR flag is set at the same time as CB-3 MTTF. The Second Status Register must be read and evaluated by the program to determine what caused the error. CB-3 MTTF (Job Done flag) is set when the LRCS character is read from tape. Note that a BRK RQST is made for each character read from tape except in the Core Dump Mode where two characters are read before a BRK RQST is made. Continuous operation may be obtained under the same conditions as a write operation. Read after write operations set the Illegal Function flag. To read the CRC and LRC characters, bit 4 in the Function Register must be 1.

8.3.4 Read/Compare

The read/compare operation (see D-TD-TM8-E-1 sheet 2 for timing diagram) compares data read from tape with data from memory that is addressed by the CA Register. The WC and CA Registers must be loaded and density and parity modes must be set. If an OC-1 R/C ERROR occurs, the incrementation of the CA Register stops and the CA Register contains the address of the data that produced the error. An OC-1 R/C ERROR also sets bit 10 in the Main Status Register (Figure 7-4). Tape motion continues to the end of record and MTTF is set. If interrupt is enabled (Figure 7-2), the program is interrupted by an OC-1 R/C ERROR and the Main Status Register is read to determine if the error was a OC-1 R/C ERROR. The CA Register must be read by the program to determine the memory location where data was stored that caused the error. Note a read/compare operation cannot follow a write operation; the tape must be backspaced before starting a read/compare operation.

8.3.5 Extended Gap

Extended Gap is used with write operation (bit 3 in the Command Register must be set) to cause the transport to leave a 3-inch (7.62 cm) blank space (gap) at the beginning of a record (Drawing No. TD-TM8-E-1, sheets 1 through 9). This feature is used to leave spaces to separate records or groups of records and to space over bad spots on tape. Note that the only difference between this operation and a normal write operation is the time required to obtain the first write strobe pulse from the TS03 (Table F-7 for definition).

8.3.6 Write End-of-File

The write end-of-file operation (D-TD-TM8-E-1, sheet 4) writes a single character (23_8) on tape to designate the end of a record or group of records. The EOF character is followed by an LRC character that is identical to the EOF character. The WC and CA Registers do not have to be loaded for this operation.

8.3.7 Space Forward

The space forward operation (see D-TD-TM8-E-1, sheet 5 for timing diagram) causes the tape to space forward a number of records specified by the WC Register. The WC Register must be loaded with the 2s complement of the number of records to be spaced over. The WC Register is incremented by the C LRCS pulse at the end of each record. CB-3 MTTF sets when the WC Register overflows and the last record has been passed over. Note that an attempt to Space Forward when the tape is at EOT is an error that sets the SC-2 ERROR flip-flop after CB-3 MTTF is set. Space forward is terminated if a File Mark is encountered. SC-2 ILLEGAL FUNCTION is set if space forward is initiated after a write or write File Mark function.

8.3.8 Space Reverse

The space reverse operation (see D-TD-TM8-E-1, sheet 3 for timing diagram) causes the tape to space reverse a number of records specified by the WC Register. The WC Register must be loaded with the 2s complement of the number of records to be spaced over. CB-3 MTTF sets when the WC Register overflows and the last record has been passed over. Note that an attempt to do a space reverse operation when tape is at BOT is an illegal function that sets the SC-2 ILLEGAL FUNCTION flip-flop and ends the operation. A space reverse operation is terminated if a File Mark, BOT, or WCOV is encountered.

8.3.9 Rewind

The rewind operation causes the tape to rewind at high speed to BOT. The WC and CA Registers need not be loaded for this operation. CB-3 MTTF is set when the selected transport asserts Rewind Status. After one transport is given the command to rewind, another transport can be selected for other operations. If the selected unit is rewinding, C TUR is false (not ready) and no operations can be performed on that transport.

8.3.10 Continuous Operation

As previously stated, an operation ends when the CB-3 MTTF (Job Done) flag is set. To continue an operation after CB-3 MTTF sets, the program must execute the LFGR instruction before SDWN (tape settling down time) to restart the transport and continue the operation. Note that the WC and CA Registers may have to be loaded to select new word count and memory address parameters. The operation continues until the WC Registers overflow and the operation is terminated.

8.4 PROGRAMMING NOTES AND EXAMPLES

This section is not designed to teach programming but to give some programming notes and examples to be used when programming the TM8-E. For programming information, refer to *Introduction to Programming,* 1970 and *PDP-8/E and PDP-8/M Small Computer Handbook,* 1972.

8.4.1 Programming Notes

The only programming restrictions to be considered are those that generate SC-2 ILLEGAL FUNCTIONS (Table 8-2), which includes attempting to perform read operations after write operations. To read after writing a record, the program must perform at least one tape move operation, i.e., space reverse or rewind.

8.4.2 Programming Examples

The following routine is an example of the method to be used to program the TM8-E. Note that in this particular example program interrupts are not used.

The general method of calling this TM8-E routine is as follows:

1. Set locations COMMAND (Figure 7-2), CUR ADR, WRD CNT, and FUNCTN (Figure 7-3) as indicated at the end of the TM8-E routine.

2. Execute JMS TM8-E.

The routine returns to the next location if and only if the CB-3 Error flag is set with the final contents of the Function/Status Register in the MQ and the final contents of the Main Status Register in the AC. Refer to Table 8-2 for conditions to set the CB-3 Error flag. The routine returns to the second location following JMS TM8 if the Error flag is cleared (the AC is all 0s and the MQ is unchanged).

```
TM8E,     0
          CLA                    Ensure AC = 0000
          CLF                    Clear TM8-E flags.
          TAD       COMMAND      Get drive, parity, field, and density.
          LCMR                   Load Command Register.
          CLA CMA                Get starting address minus one.
          TAD       CURADR
          LCAR                   Load CA Register.
          TAD       WRDCNT       Get 2's complement of the number of words to be transferred
                                 or records to be spaced.
          LWCR                   Load WC Register.
          TAD       FUNCTION     Get Function, Gap, GO bit, and EMA Increment.
          LFGR                   Load Function Register and GO.
          SKEF                   Wait for ERROR flag or MTTF flag.
          SKP
          JMP       TM8ENO       ERROR flag set.
          SKTD
          JMP       -4
          SKEF                   MTTF set? ERROR flag set?
          JMP       TM8EOK       No. No errors reported for this operation.
TM8ENO,   RFSR                   ERROR flag set. Read Function/Status.
          MQL                    Register and load into MQ.
          RMSR                   Read Main Status Register and leave in AC.
          SKP                    Bypass return address update if in error.
TM8EOK,   ISZ       TM8E         No error reported then update return address.
          CLF                    Clear TM8-E flags.
          JMP 1     TM8E         Exit.
COMMAND,  0                      This location must contain all information to be loaded into the TM8-E Command
                                 Register.
FUNCTION, 0                      This location must contain all information to be loaded into the TM8-E Function
                                 Register.
CURADR,   0                      This location must contain the first memory address minus one to be used in
                                 Write, Read, or Read/Compare operations.
WRDCNT,   0                      This location must contain the 2's complement of absolute value of the number
                                 of words to be transferred in Write, Read or Read/Compare operations, or the
                                 absolute number of records to be spaced in Space Forward or Space Reverse
                                 operations.
```

The following is an example of a TM8-E routine using the Program Interrupt System.

```
TM8-E     0                      Enter here.
          CLA                    Clear AC (AC = 0000).
          CLF                    Clear TM8-E flags.
          TAD       COMMAND      Get drive, parity, field, and density (Table 8-1).
          IOF                    Turn PDP-8/E Interrupt System off.
          LCMR                   Load Command Register (Table 7-1).
          CLA CMA                Get starting address minus one.
          TAD                    CURADR.
          LCAR                   Load CA Register.
          TAD       WRDCNT       Get 2's complement of number of words to be transferred or
                                 records to be spaced.
          LWCR                   Load WC Register.
```

TM8-E (Cont)	TAD	FUNCTN	Get Function, Gap, GO bit, and EMA Increment (Table 8-2).
	LFGR		Load Function Register and GO (Table 8-2).
	ION		Turn on program interrupt system.
	INT SET,		ERROR flag set.
Poll another Device	TM8-EOK		Service another device if Interrupt Request is made.
TM8-E No,	RFSR		If ERROR flag is set then Read Function/Status Register and load into MQ.
	MQL		
	RMSR		Read Main Status Register and leave in AC.
TM8EOK,	ISZ	TM8-E	No error reported then update return address.
	CLF		Clear TM8-E flags.
	JMP 1	2	
	INT SER		Continue servicing other devices.

CHAPTER 9
DETAILED LOGIC DESCRIPTIONS

9.1 INTRODUCTION

The logic in the TM8-E is broken into functional groups for discussion purposes. Figures 9-1 through 9-28 should be used to understand the interaction of the logic, signal flow between groups of logic, and the input or output signals. The purpose of each group of logic is discussed in Chapter 7.

NOTE

The signals on the TM8-E print set are preceded by two letters and a number to indicate the origin of the signal, i.e., a signal with SC1 in front of it originates on sheet 1 of the status and control module prints. Signals without prefixes are Omnibus signals.

9.2 M8321 OUTPUT CONTROL MODULE

9.2.1 Input/Output Instruction Decoder

The I/O instruction decoders (Figure 9-1) decode instructions from the Memory Data Bus and generate signals to control the operation of the TM8-E. Bits MD 3 through MD11 are gated by I/O PAUSE when an I/O instruction is executed by the processor. Bits MD 3 to MD 6 generate a signal, 67XX, which partially enables the gates to the I/O decoders. MD 7 and MD 8 generate a signal (670X, 671X, or 672X) to apply bits MD 9, MD 10, and MD 11 to the I/O decoder. Each I/O decoder is an 8251 IC; the 8251 IC is a binary-to-decimal decoder, which decodes MD 9 through MD 11 and produces a low on one output line. The low out of the 8251 IC indicates which instruction is to be executed. As an example, a 670X instruction with MD 9 low and MD 10 and 11 high (100) produces a low on pin 4 of the 670X decoder to indicate that a LFGR instruction (6706) was executed by the program. INT I/O L is grounded to prevent execution of IOT instructions by the processor while TM8-E instructions are underway.

9.2.2 C Line Select Logic

The C line select logic (Figure 9-1) controls the direction of data flow between the Data Bus and AC and determines if the AC is to be cleared or not. Table 9-1 shows the status of C0 and C1 to transfer data between the AC and Data Bus using the TM8-E IOT instructions.

9.2.3 TP3 Logic

TP3 is used to enable the selection of the 670X I/O decoder and is used throughout the TM8-E to enable the execution of instructions (Figure 9-1) and to enable data transfers using the single cycle data break interface.

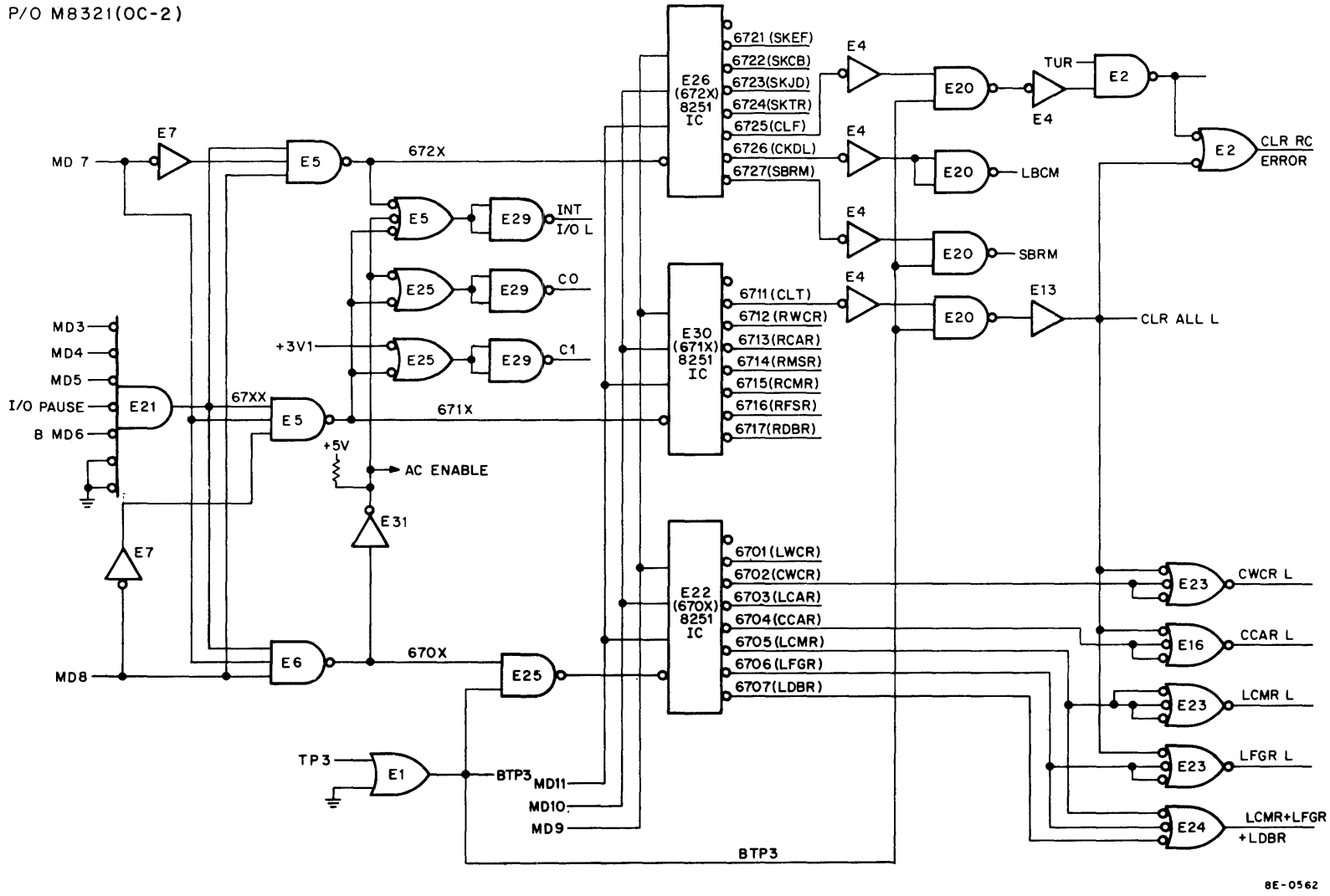


Figure 9-1 IOT Decoder Logic

Table 9-1
C Line Select Levels for TM8-E Transfer Operations

Instruction	C0	C1	Transfer of Operation
LWCR	Low	High	AC → Data Bus 0 → AC
LCAR	Low	High	AC → Data Bus 0 → AC
LCMR	Low	High	AC → Data Bus 0 → AC
LFGR	Low	High	AC → Data Bus 0 → AC
LDBR	Low	High	AC → Data Bus 0 → AC
RWCR	Low	Low	Data Bus → AC
RCAR	Low	Low	Data Bus → AC
RMSR	Low	Low	Data Bus → AC
RCMR	Low	Low	Data Bus → AC
RFSR	Low	Low	Data Bus → AC
RDBR	Low	Low	Data Bus → AC

9.2.4 CLR ALL Logic

CLR ALL L (Figure 9-1) is asserted to clear TM8-E logic under the following conditions:

1. At TP3 time, if a CLT (6711) instruction is executed by the program.
2. When a CLF (6725) instruction is executed by the program (if C TUR is true).
3. When PWR OK H from the processor is lost due to a power failure.
4. When the processor asserts INIT H. This occurs during power up or when the CLEAR key is pressed on the PDP-8 console.

9.2.5 AC ENABLE Logic

OC-2 AC ENABLE (Figure 9-1) is asserted when a 670X instruction is executed by the program to enable gates to apply the Data Bus information to the TM8-E registers that are loaded from the AC (Figure 9-7) and Control C0 and C1 levels (Paragraph 9.2.2).

9.2.6 Skip Logic

The skip logic (Figure 9-2) asserts OC-2 SKIP BUS L and causes the processor to skip an instruction when the following conditions exist.

1. The 6721 (SKEF) instruction is executed and the SC-2 Error flag is set.
2. The 6722 (SKCB) instruction is executed and SC-1 CNTL BSY flag is set.
3. The 6723 (SKJD) instruction is executed and CB-3 MTTF flag is set.
4. The 6724 (SKTR) instruction is executed and C TUR L is true.

9.2.7 Output Control Function Decoder

The output control function decoder (Figure 9-3) is an 8251 IC, which decodes the three most significant bits of the Function Register and determines what function the TS03 transport performs (Table 8-1). The 8251 IC is a BCD-to-decimal decoder which decodes FR0, FR1, and FR2 and produces a low on one output line. The low out of the 8251 IC indicates the function to be performed. As an example, if FR0 is low, and FR1 and FR2 are high, pin 9 is low indicating a write operation is to be performed. The outputs of the function decoder, applied to the tape transport, are defined in Table F-7 and Figure 7-3.

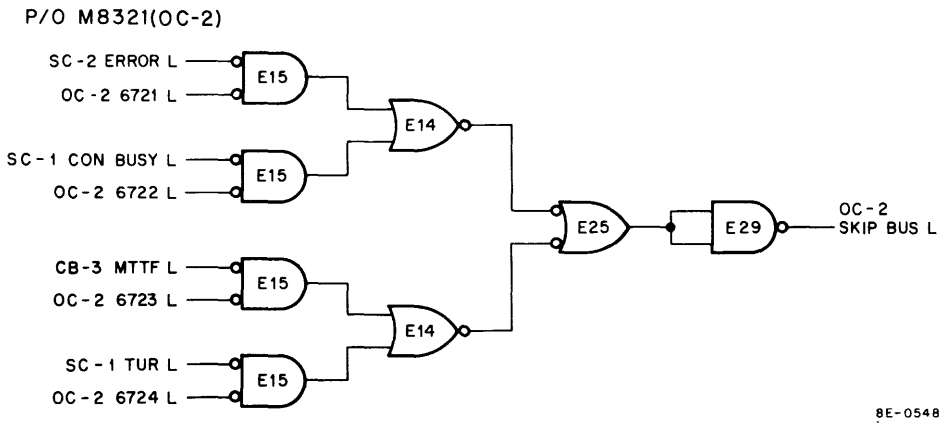


Figure 9-2 Skip Logic

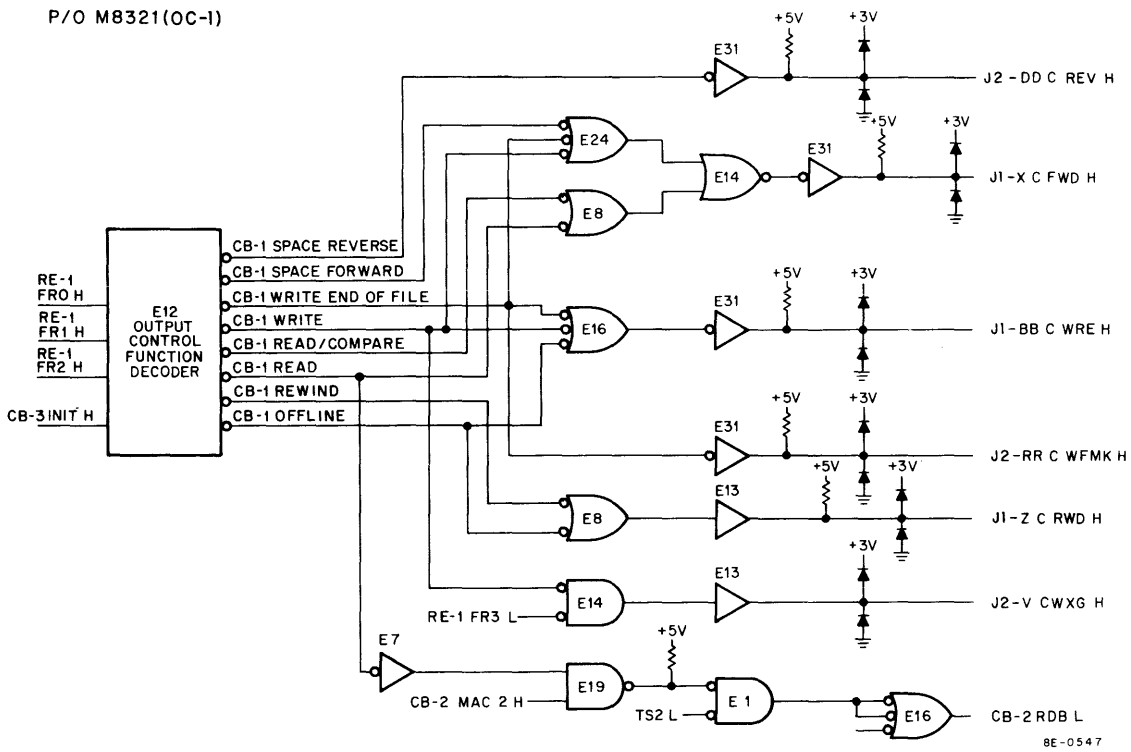


Figure 9-3 Output Control Function Decoder

9.2.8 Read/Compare Logic

The read/compare logic consists of 12 Exclusive-OR gates and the OC-1 R/C Error flag (flip-flop). The 12 bits of data from the Memory Data Bus (data read from memory) are Exclusively-ORed with 12 bits of data from the Data Register (data read from tape). During the data break, at TP3 time, if the data from memory is different from data read from DECmagtape the SC-1 R/C ERROR flag is set and CA incrementation stops. Tape motion continues until an LRC strobe is obtained at end of record. RE-1 DEN 5 H and RE-1 DEN 8 H are used to enable a gate on the outputs of the Exclusive-OR gates for the four most significant bits to prevent them from causing a read/compare error. RE-1 R/C ENABLE is always high when a read/compare function is selected by the program. Refer to D-TD-TM8-E-1, sheet 2, for the timing during a read/compare operation.

9.2.9 Write Data Select Logic

The write data select logic selects 6 or 8 bits of data from memory to be written on DECmagtape (Figure 9-4). The gates labeled C on Figure 9-4 are enabled by CB-1 WR 9 H to apply 8 bits of data from the Data Buffer Register to the selected transport (see D-TD-TM8-E-1, sheet 8, for timing).

The control signals for the gates originate in the control logic shown in Figure 9-26. The outputs to the transport are limited to 0.0 V and +3 V levels by the diode and resistor networks tied to the output lines.

9.3 M8327 REGISTERS MODULE

The TM8-E Registers are used to address memory, count the words in a data transfer, select DECmagtape operations, and generate command signals for the TM8-E control logic and the tape transports. Each of the registers used in the TM8-E are discussed in the following paragraphs; the Status Register is discussed with the Transport Status and control logic in Paragraph 9.4.1.

9.3.1 Data Buffer Register and Multiplexer

The Data Buffer Register and Multiplexer (Figure 9-5) provides temporary storage for data manipulation (transfers and read/compares). Inputs to the Data Multiplexer come from memory (MD 0 through MD 11), from the AC (DATA 0 -DATA 11), or from the tape (CRD 0 through CRD 7). The Data Multiplexer is a 74153 IC (refer to Appendix H for logic diagram, truth table and pin locations), which selects one of the four data inputs to be applied to the Data Buffer Register. CB-2 DB MPX A and CB-2 DB MPX B controls the selection of data that is supplied to the Data Buffer Register. Table 9-2 shows the levels required to load the Data Buffer Register for each operation. CB-1 DBC 1 and CB-1 DBC 2 are used to clock the output of the multiplexer into the Data Buffer Register. The Data Buffer Register is two 74174 ICs (refer to Appendix H for truth table, logic diagram, and pin locations) each containing six flip-flops that are set or cleared by the input from the multiplexer. The contents of the Data Buffer Register are applied to the read/compare logic, to output control logic, and to an 8235 IC as shown in Figure 9-6. During a read operation or when a RDBR instruction is executed, the data is transferred to the Data Bus. During a read operation, data is transferred to a memory location selected by the Current Address Register during single cycle data break. If the RDBR (6717) instruction is executed, the data is transferred to the AC via Data Bus. Refer to the flow diagram (Figure 8-10 and Figure 8-5) for an illustration of this operation. The timing diagrams for these operations are shown in Drawing No. D-TD-TM8-E-1, sheets 1 through 9.

Table 9-2
Data Multiplexer Selection Levels

Operation	CB-2 DB MPXA H (pin 14)	CB-2 DB MPXB H (pin 2)
Load Data Buffer	low	low
Write	high	low
Read 7 Channels	low	high
Read 9 Channels	high	high

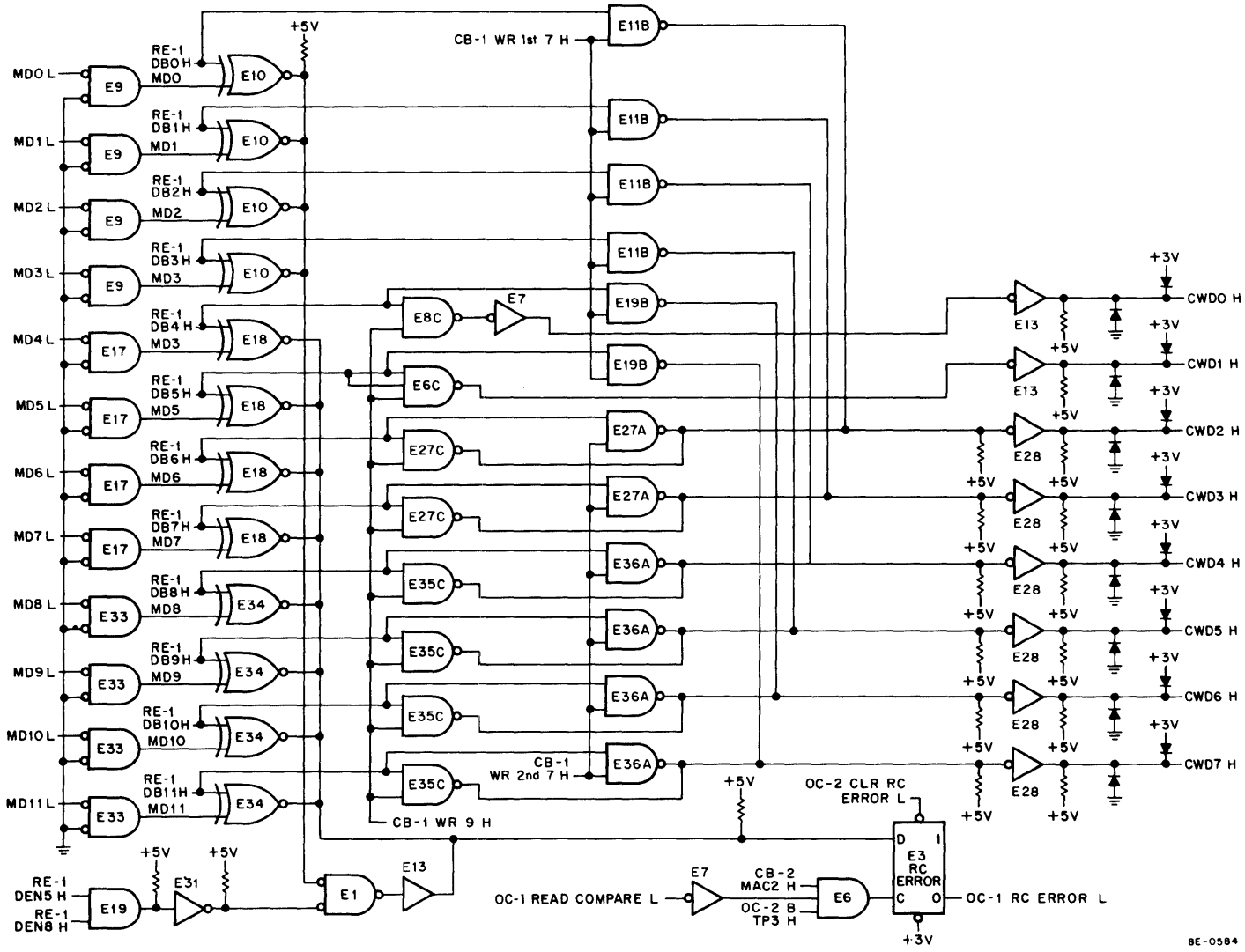


Figure 9-4 Read/Compare and Write Data Select Logic

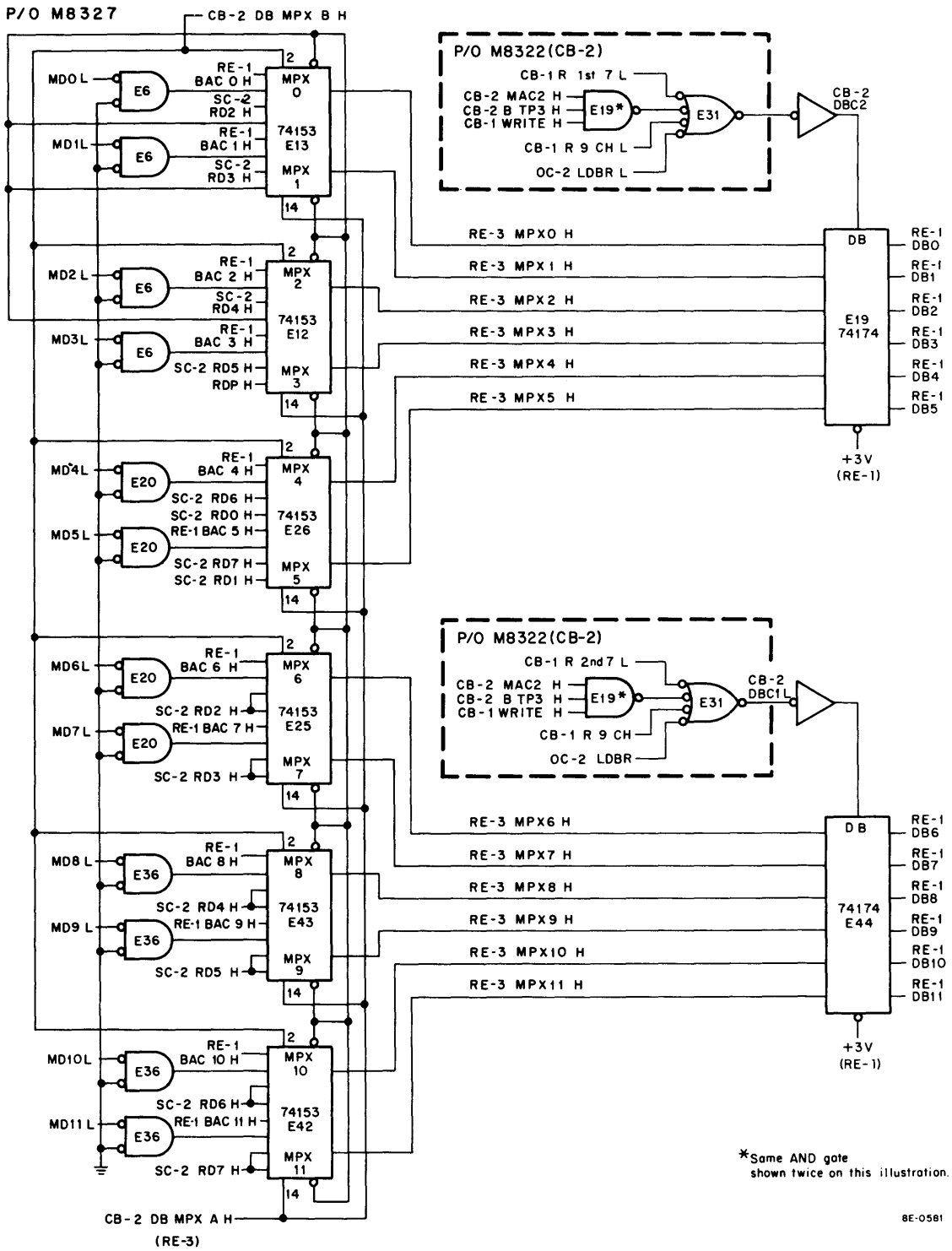


Figure 9-5 Input Data Multiplexer and Data Register

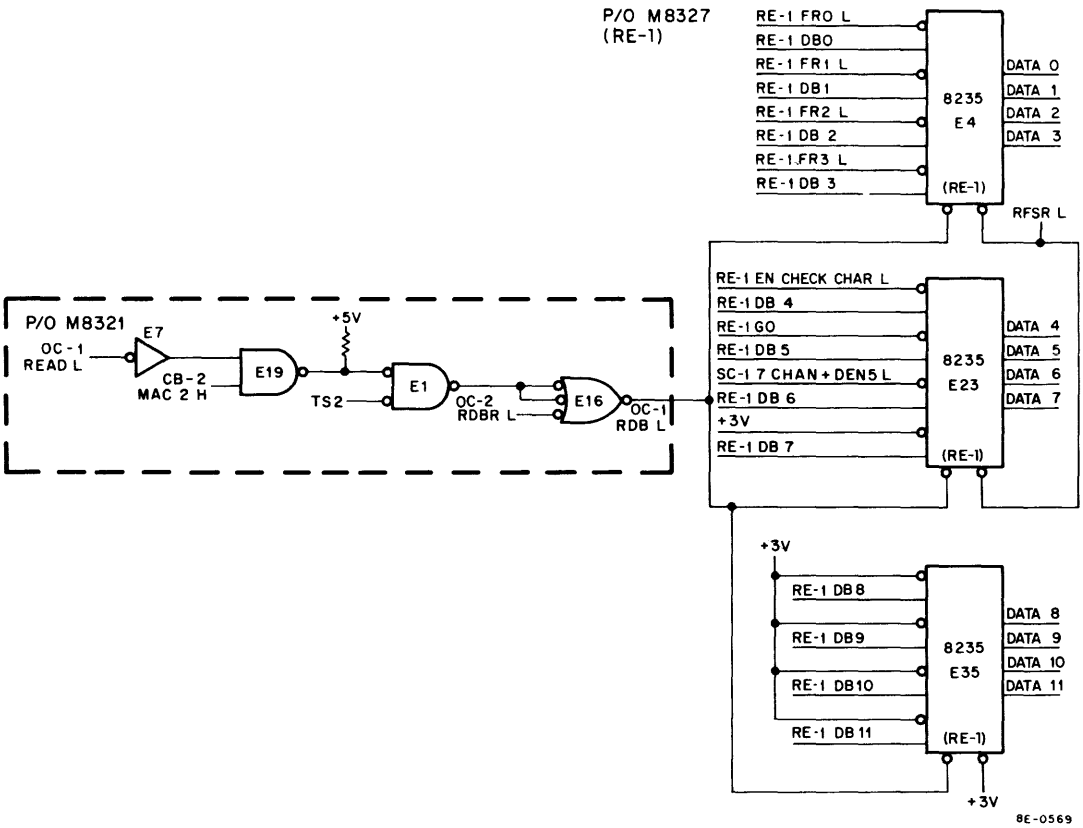


Figure 9-6 Data Register and Function Register Output Multiplexer

9.3.2 AC Input Gating

The AC input gating (Figure 9-7) is used as a buffer between the Data Bus (inputs from the AC) and the TM8-E Registers. OC-2 AC ENABLE L is asserted (low) any time a 670X instruction is executed by the program to transfer data from the AC to the TM8-E Registers. The outputs of the NAND gates enabled by OC-2 AC ENABLE are applied to the Command, Data, and Function Registers, and to two 74174 ICs, which provide a Holding Buffer for inputs from the AC. The 74174 ICs (refer to Appendix H for truth table, logic diagram, and pin locations) are 6-bit buffer registers for inputs to the WC and CA Registers and bits 6 through 8 of the Command Register. SC-1 B TP3 is used to clock the outputs of the NAND gates into the AC Holding Buffer Register. The outputs of the AC Holding Buffer Register are applied to the WC and CA Registers (Figure 9-8).

9.3.3 Current Address (CA) Register

The Current Address Register (Figure 9-8) is a ripple counter that sequentially addresses locations in memory by incrementing before each data transfer. The CA Register is loaded with a 12-bit address that is one less than the desired starting address. The CA Register is incremented by the leading edge of SC-1 COUNT CA L (Figure 9-8) each time a BRK RQST is made by the TM8-E. CB-2 MAC ACC is asserted after a BRK RQST is granted to the TM8-E and removes the SC-1 COUNT CA L signal from the CA Register. The CA Register is not incremented when SC-1 COUNT CA L goes high because the counter increments only a high-to-low transition of the signal. The CA Register is loaded by the LCAR instruction before each DECmagtape operation and must not be loaded during CNTL BSY.

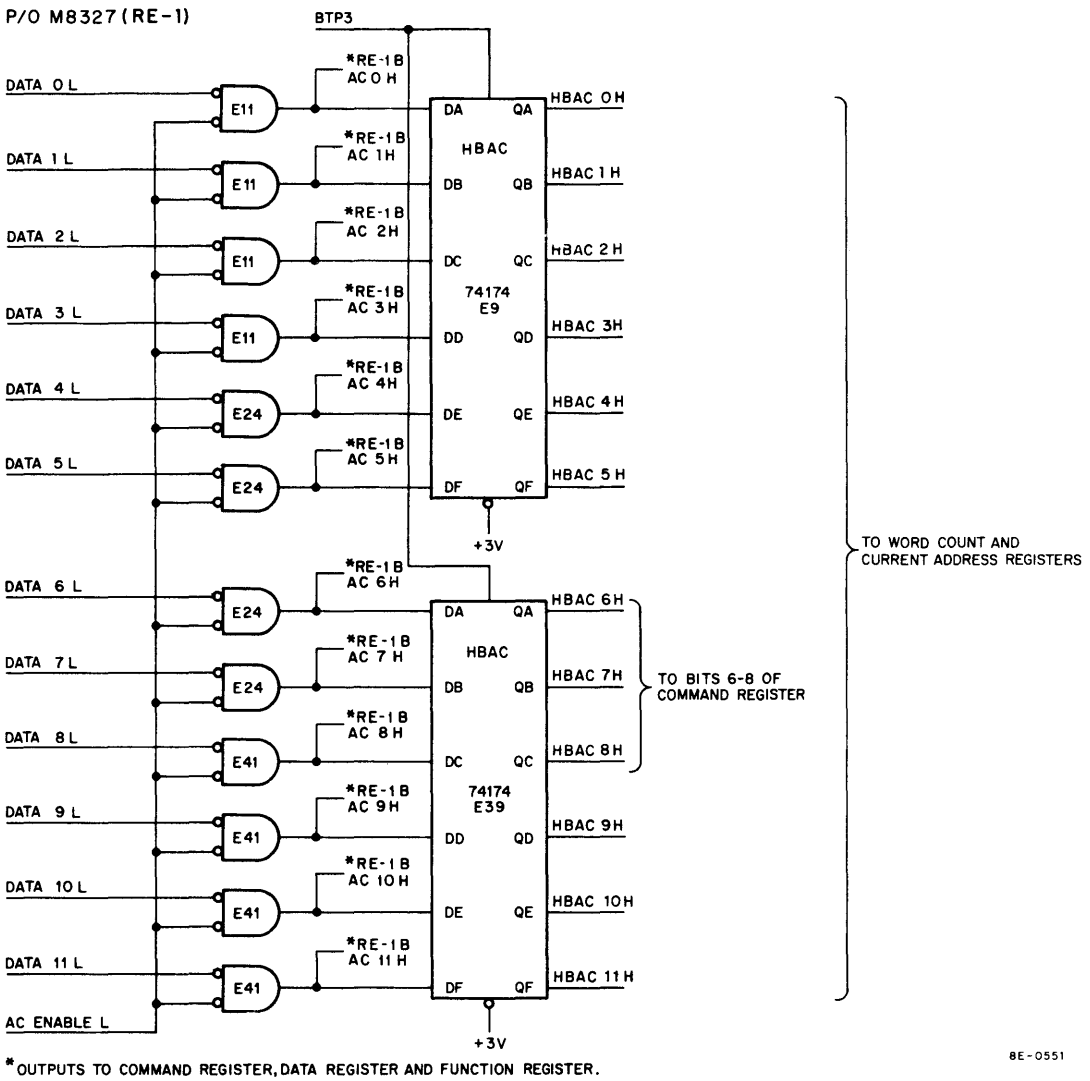


Figure 9-7 AC Input Gating and Holding Buffer Register

The output of the CA Register is applied to the MA lines when CB-2 MAC 1 H enables the NAND gates (Figure 9-8) to select a location in memory which contains data to be read or a location to store data from the DECmagtape. The contents of the CA Register are also applied to an 8235 IC for transfer to the AC when an RCAR instruction is executed by the program. The CA Register is read by the program during error check routines and maintenance operations to determine what address in memory generated an error. The CA Register is cleared by a CCAR instruction.

9.3.4 Word Count (WC) Register

The Word Count Register is a ripple counter that (Figure 9-8) counts the data words transferred to or from the DECmagtape during transfers and counts the records during space operations. The WC Register is loaded from the AC with the 2s complement of the number of words to be transferred or number of records to be spaced when a LWCR instruction is executed by the program.

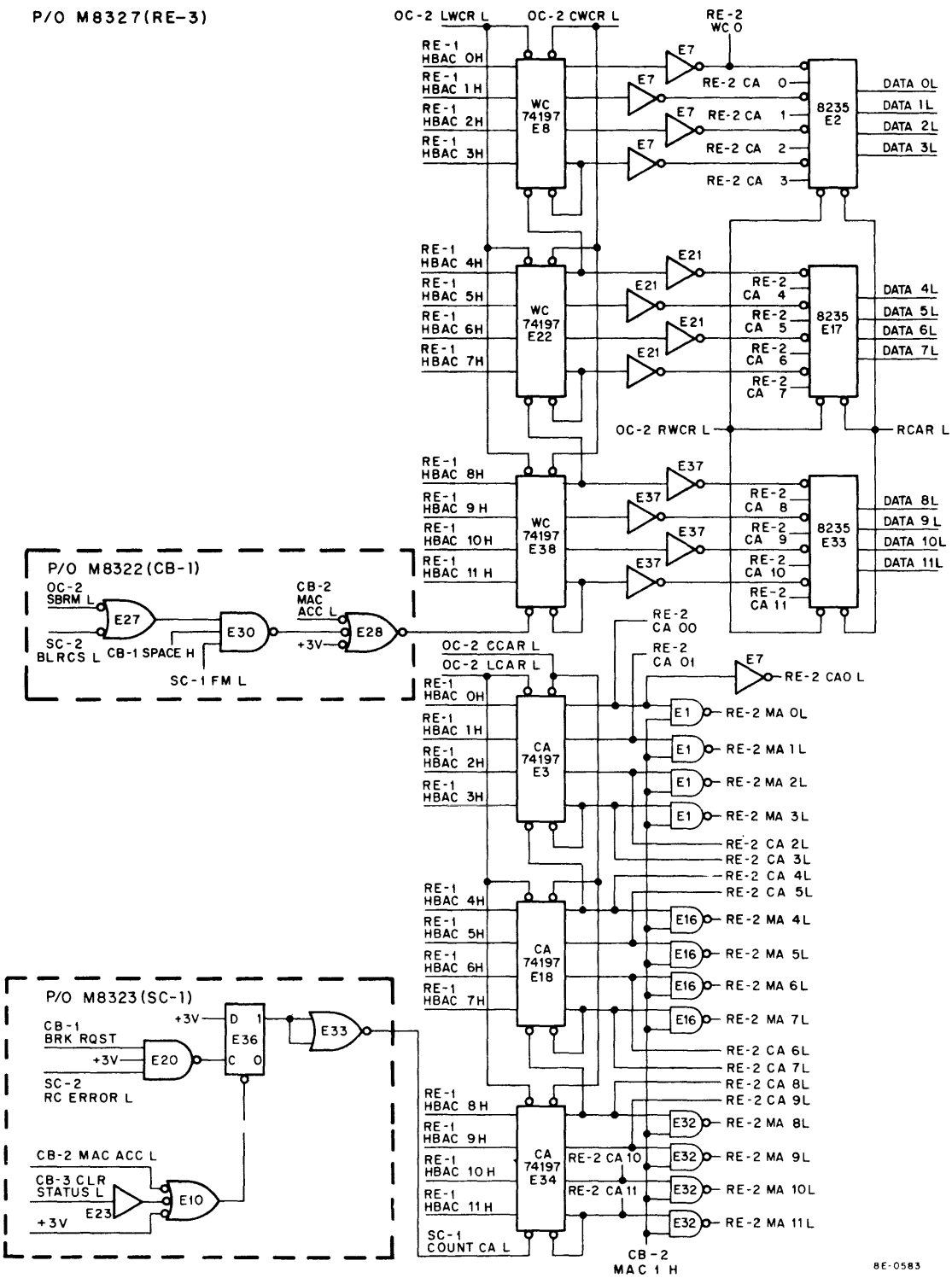


Figure 9-8 Current Address and Word Count Registers

The output of the WC Register is applied to an 8235 IC and is transferred to the AC when an RWCR instruction is executed by the program. When bit 0 makes the transition from the high to low state RE-2 WC 0 is applied to the CB-1 WCOV flip-flop (Figure 9-1). CB-1 WCOV indicates to the control logic that the data transfer is complete (the specified number of words have been transferred). Word count is incremented during the break cycle when SC-1 COUNT WC makes a high to low transition by asserting one of the following:

1. CB-2 MAC ACC L during a Read or Write operation.
2. C LRCS L during a CB-1 SPACE operation if a File Mark is not detected.

9.3.5 Function Register

The Function Register (Figure 9-9) is loaded with 6 bits of data from the AC by an LFGR instruction. The 6 bits determine the function (Table 8-1) the transport is to perform and provide control signals to initiate DECmag-tape operations. The Function Register consists of two 74175 ICs (refer to Appendix H for truth table, logic diagram, and pin locations) which contain the flip-flops that are set or cleared by bits from the AC. The three most significant bits of the Function Register (FR0 through FR2) are applied to the output control function decoder (Figure 9-3) and the control function decoder (Figure 9-19). FR3 through FR6 are applied to the control logic to accomplish the functions shown in Table 8-1. The CB-3 MTTF input to the 74175 IC clears the three least significant bits FR4 through FR6 when the CB-3 MTTF (Job Done) flag is set at LRCS time (Figure 9-22).

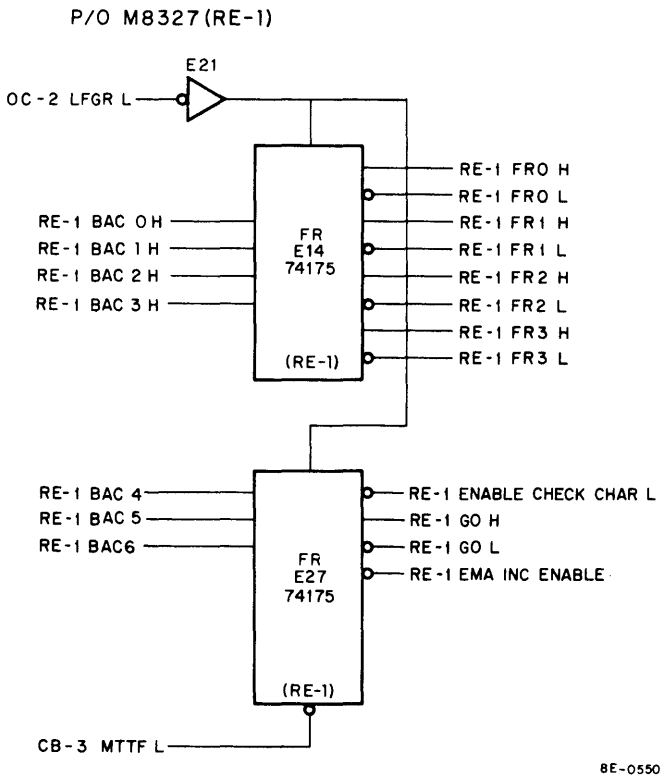


Figure 9-9 Function Register

The outputs of the Function Register are also applied to an output multiplexer (Figure 9-8) for transfer to the AC when an RFSR instruction is executed by the program. The 8235 IC transfers the function and status to the Data Bus for display in the AC or evaluation by the program when RE-1 RFSR L is asserted. RE-1 RFSR L is asserted when an RFSR instruction is executed by the program.

NOTE

The Function Register must be the last register loaded because it contains the GO bit, which initiates CNTL BSY, PRESET, and SET to start the tape transport.

9.3.6 Command Register

The Command Register (Figure 9-10) consists of nine flip-flops and a 3-bit ripple counter that are loaded from the AC when an LCMR instruction is executed by the program (Table 7-1).

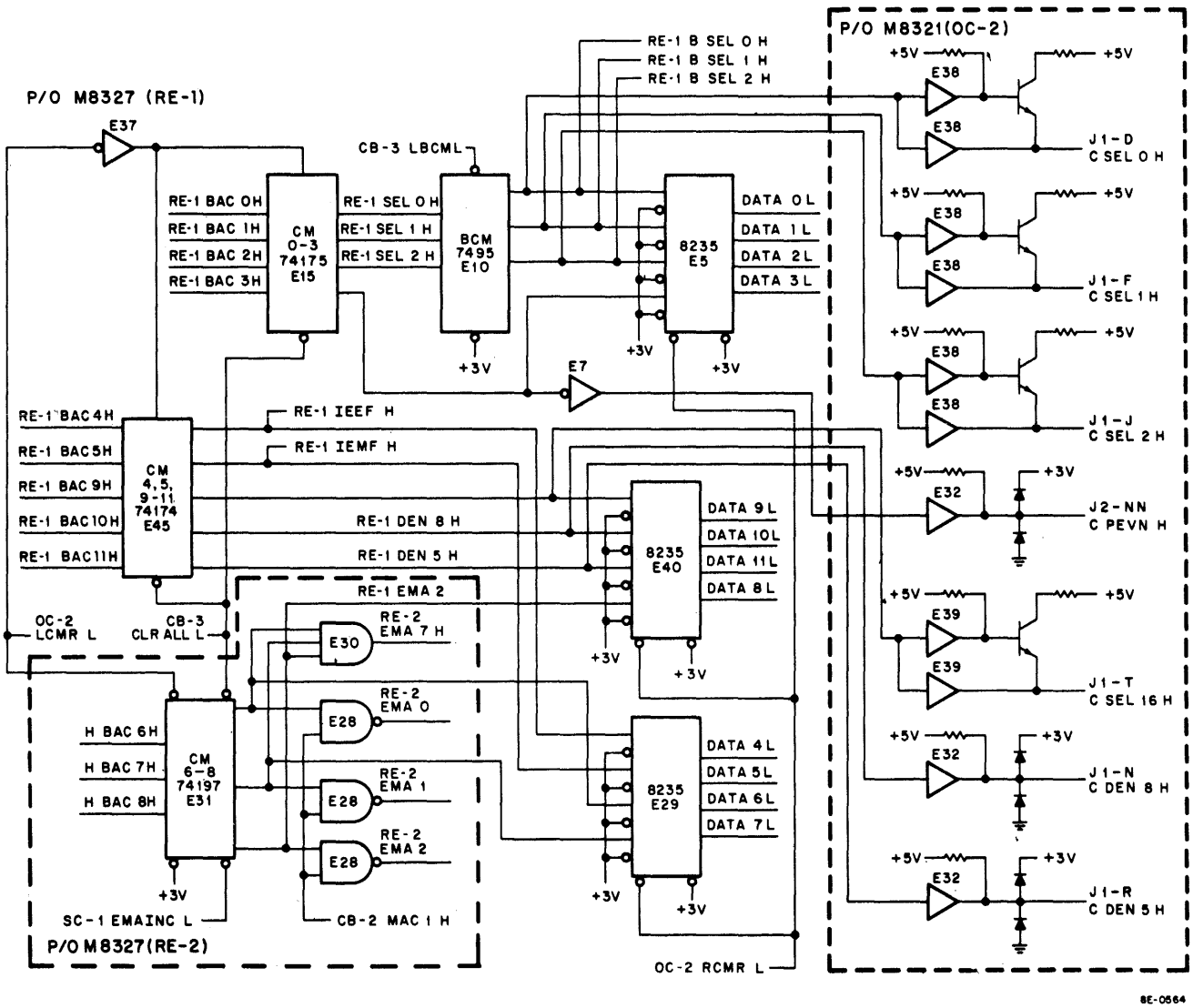


Figure 9-10 Command Register and Multiplexer

The four flip-flops that receive RE-1 BAC 0 through RE-1 BAC 3 (Table 7-1) as inputs are on a 74175 (refer to Appendix H for truth table, logic diagram, and pin locations). Three of the flip-flops on this IC generate SEL 0 through SEL 2 for indicating selection of one of the transports and provide an input to the Buffered Command Register for transport selection (Paragraph 9.3.7). AC 03 is used to select odd or even parity mode for the TS03 Transport. If this flip-flop is in a 0 state, even parity is selected and C PEVN L to the TS03.is asserted.

RE-1 BAC 4, RE-1 BAC 5, and RE-1 BAC 9 through RE-1 BAC 11 are applied to a 74174 IC (refer to Appendix H for truth table, logic diagram, and pin locations), containing six flip-flops that are loaded by the inputs from the AC (Table 7-1).

The remainder of the bits from the AC (AC 6 through AC 8) are applied to a 74197 IC (refer to Appendix H for truth table, logic diagram, and pin locations) containing three flip-flops to select a memory field during data transfer. The 74197 IC is a 3-bit ripple counter that is incremented by SC-1 EMA INC L if bit 6 in the Function Register is set (1). The output of the 74197 IC (RE-1 EMA 0 – RE-1 EMA 2) is applied to the Omnibus when CB-2 MAC 1 H enables the three AND gates (Figure 9-10) during a single cycle data break. Refer to Paragraph 9.4.2 for a discussion of the SC-1 EMA INC L signal generation.

The contents of the Command Register are transferred to the Data Bus when the program executes an RCMR instruction to assert the control input of the 8235 ICs (Figure 9-10). The Command Register is cleared by CB-3 CLR ALL L (Paragraph 9.2.4).

9.3.7 Buffered Command Register (BCM)

The Buffered Command Register (Figure 9-10) receives RE-1 SEL 0 through RE-1 SEL 2 as inputs from the command register. RE-1 B SEL 1 through RE-1 B SEL 2 out of the BCM are applied to the TS03 to select a transport and provides an input to a comparison circuit to determine when a new transport has been selected (Figure 9-23). CB-2 CHG TRANS L is asserted if RE-1 SEL 0 through RE-1 SEL 2 from the command register and RE-1 B SEL 0 through RE-1 B SEL 2 from the Buffered Command Register are different; thus CB-2 CHG TRANS L is asserted if a new transport is selected by the program. The output of the BCM holds the select lines to the previously selected transport in the same state until C SDWN L (settled down) is obtained from the transport. Then the BCM is loaded by RE-2 LBCM L to select a new transport. Thus the BCM allows the program to load the command and select a new transport without deselecting the previously selected transport before it stops.

9.4 M8323 TRANSPORT STATUS AND CONTROL MODULE

The M8323 Transport Status and Control module consists of the Main Status Register (Table 8-2), Second Status Register (Table 8-3), logic for generation of timing and control signals, and a Data Multiplexer to transfer the contents of the Status Registers to the Data Bus.

9.4.1 Main Status Register

The logic elements that make up the Main Status Register perform as follows.

9.4.1.1 SC-2 Error Flag Logic – The SC-2 Error flag (Figure 9-11) is set immediately if the program attempts an illegal function or if SC-2 SEL ERROR is asserted by the selected transport. The SC-2 Error flag is set after CB-3 MTTF is set if any of the following errors are detected.

1. EOT
2. BOT
3. DATA LATE
4. PARITY ERROR (LRCE, CRCE, or VPE in Second Status Register)
5. REC LNG INCORRECT
6. EMA 7 INC ERROR (Second Status Register)
7. R/C ERROR
8. File Mark (FM)

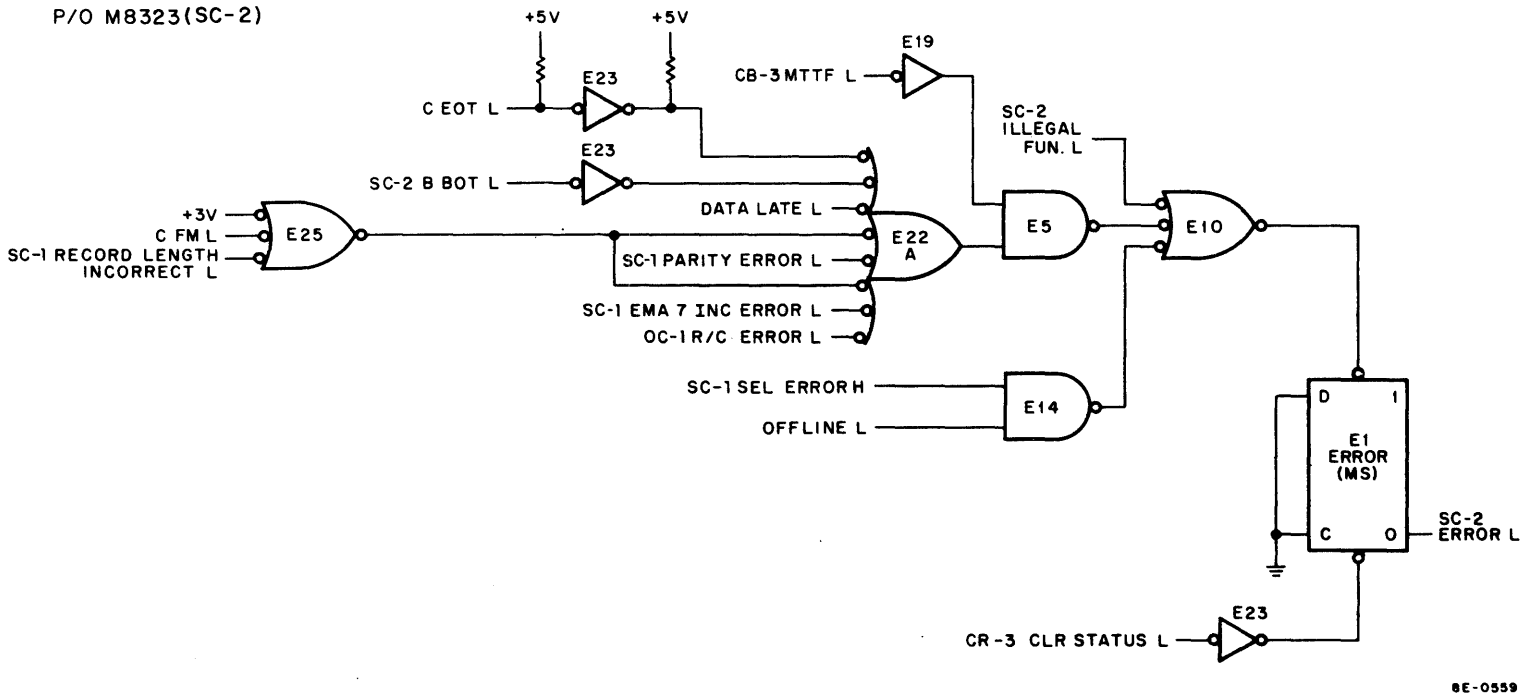


Figure 9-11 Error Flags

9.4.1.2 Illegal Function Logic - The SC-2 ILLEGAL FUNCTION flip-flop (Figure 9-12) is set if the program attempts any of the following SC-2 ILLEGAL FUNCTIONS:

1. The program executes an LCMR, LFGR, or LDBR instruction when the SC-1 CNTL BSY flip-flop is set (Paragraph 9.4.5).

2. Selection of any density other than 800 bpi.

3. Selection of a space reverse operation when the selected TS03 Transport is at BOT.

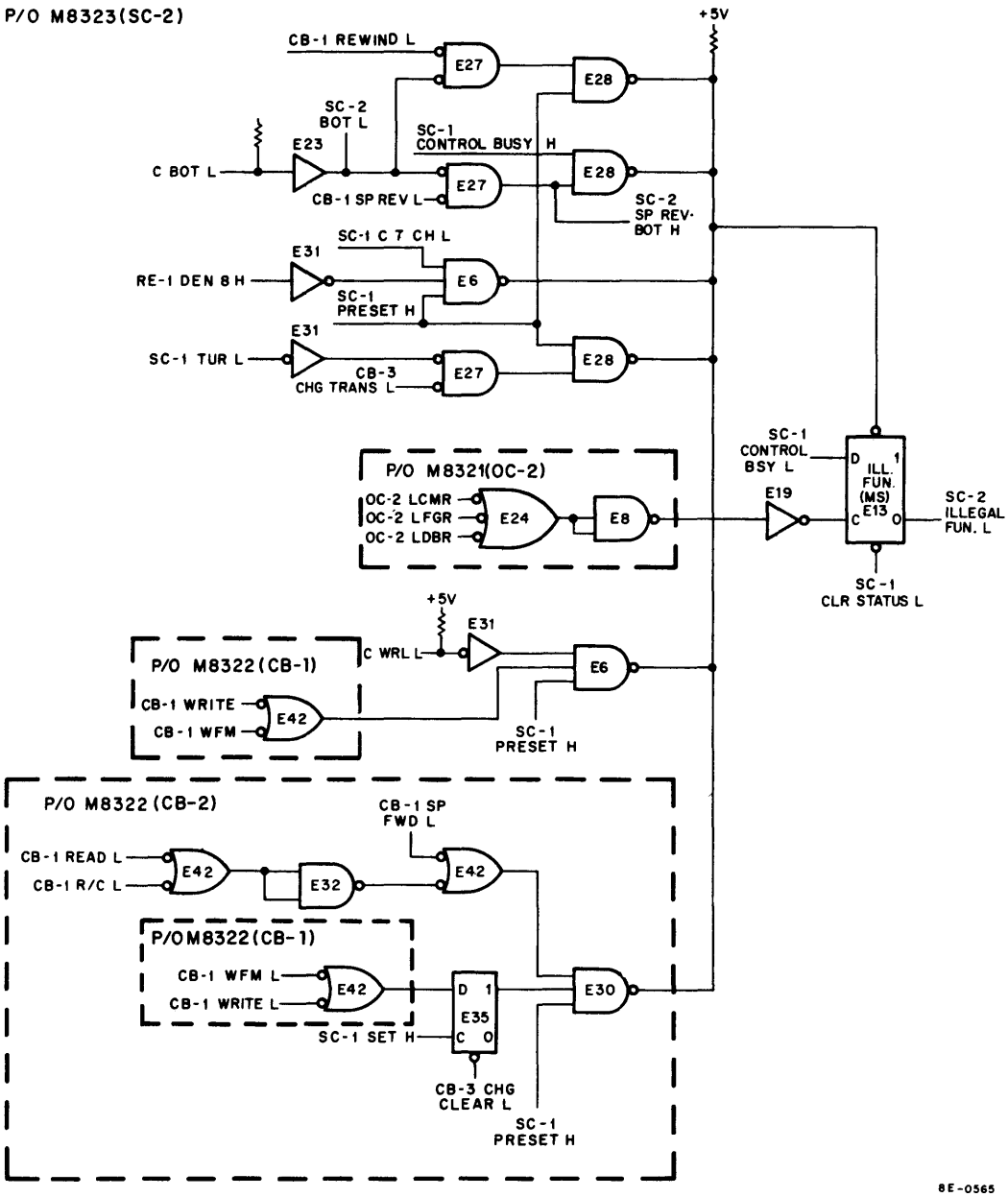


Figure 9-12 Illegal Function Flag and Control Logic

4. Selection of read, read/compare, or space forward after a write or write end-of-file operation if the same transport is used.

5. Changing to a transport that is not ready (C TUR is false) and SC-1 PRESET is issued.

6. Attempting a rewind when tape is at BOT.

7. Any write command issued to a transport with write lockout set.

9.4.1.3 Data Late Logic – The SC-1 Data Late (Figure 9-13) flip-flop is set if the computer fails to service a BRK RQST before the next word is transferred to or from tape. A counter made up of flip-flops A, B, and C (Figure 9-13) counts the Read Strobe or Write Strobe pulses generated by the tape transport each time a character is read from or written on tape. SC-1 WRS L or SC-1 B RDS L clocks the three flip-flops (A, B, and C). CB-2 MAC ACC L (Figure 9-13) is asserted after a BRK RQST is granted to the TM8-E by the processor to clear the counter and prevent the SC-1 DATA LATE flip-flop from setting when the next SC-1 WRS or SC-1 B RDS pulse occurs. If CB-2 MAC ACC is not asserted by the time the next SC-1 WRS or SC-1 B RDS pulse occurs, the set side of the B flip-flop causes SC-1 DATA LATE to set. The set output of the B flip-flop is applied to the clock input of SC-1 DATA LATE if the NAND gate tied to the set output is not disabled by C 7 CH L or RE-1 DEN 5 H. The SC-1 DATA LATE flip-flop is always cleared during a space operation since no data is transferred. SC-1 DATA LATE is also cleared when a File Mark (C FMK) is detected during a read operation or by CB-3 CLR STATUS L.

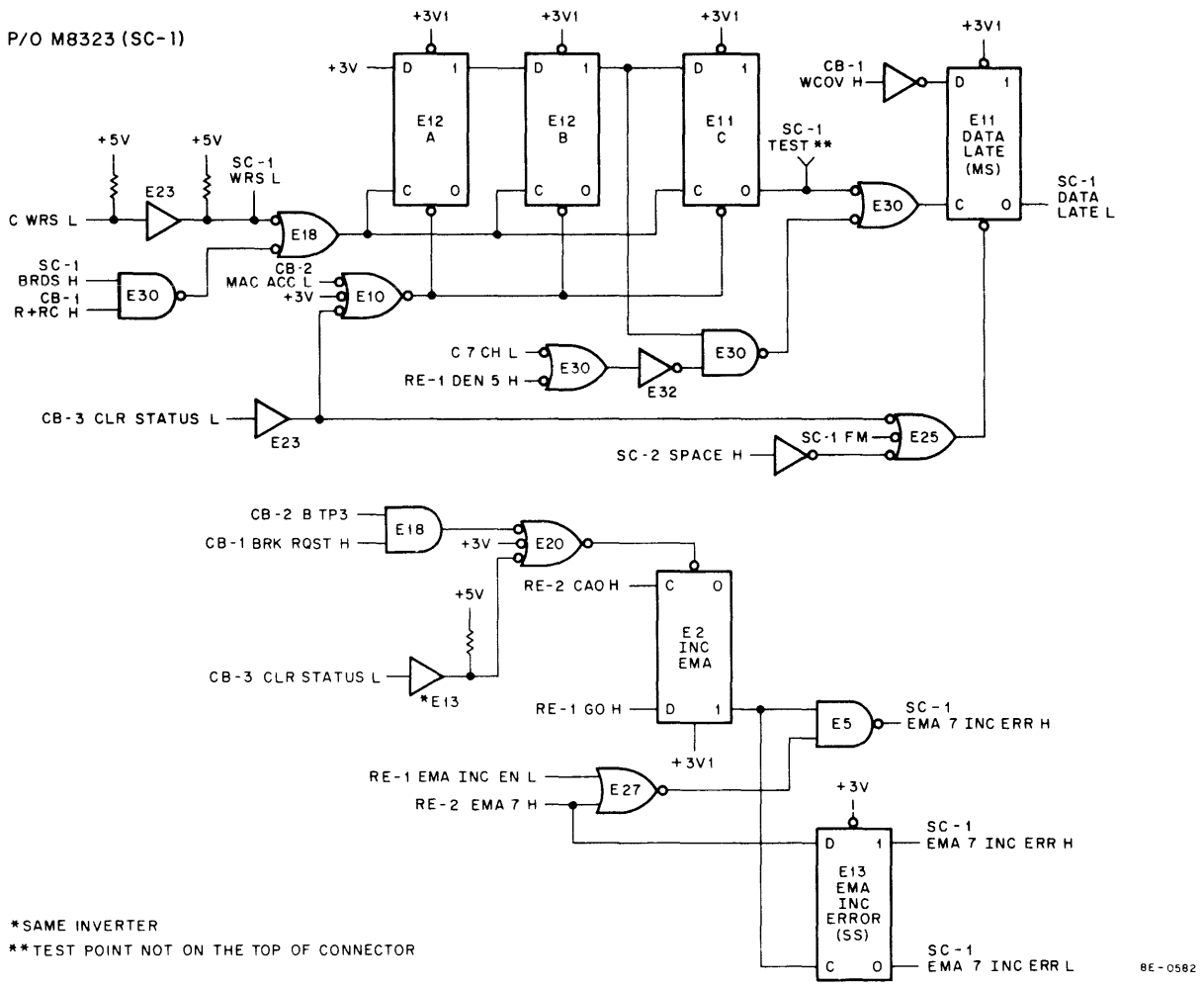


Figure 9-13 Data Late and EMA Increment Error Flags

9.4.1.4 Record Length Incorrect Logic - The SC-1 RECORD LENGTH INCORRECT flip-flop (Figure 9-14) is set when the number of data words read from the tape and the contents of the WC Register are different (record too long or too short). As previously stated, the WC Register is loaded with the 2s complement of the number of words to be transferred. Word count is incremented during the data transfer. The WC Register should contain all 0s and generate CB-1 WCOV L before the LRC character is read from tape. If C LRCS H occurs before CB-1 WCOV, gate E33 (Figure 9-14) is enabled, and the SC-1 RECORD LENGTH INCORRECT flip-flop sets. This condition occurs if the WC Register has been loaded with a word count greater than the number of words in the record (record is short). To detect a record that is too long, a counter made up of flip-flops A and B (Figure 9-14) counts the RDS pulses that occur after CB-1 WCOV H. If two or more C RDS L pulses occur after CB-1 WCOV and there are no C LRCS L or C CRCS L pulses, the SC-1 RECORD LENGTH INCORRECT flip-flop sets. This condition occurs if the Word Count Register is loaded with a word count less than the number of words transferred (record is long). Note that flip-flop A is cleared by C CRCS L or C LRCS L so that SC-1 RECORD LENGTH INCORRECT is not set during the termination of a normal operation.

CB-1 SPACE H and C FILE MARK L keep the SC-1 RECORD LENGTH INCORRECT flip-flop cleared during a space or write File Mark operation. CB-3 CLR STATUS L clears the SC-1 RECORD LENGTH INCORRECT flip-flop when the Status Register is cleared by a CLF instruction.

9.4.1.5 Tape Rewinding - Tape rewinding (C RWS L) is asserted (Figure 9-16) if the selected transport is rewinding.

9.4.1.6 End of Tape - End of tape (C EOT) is asserted if the End of Tape reflective strip has been detected by the TS03 (Figure 9-11). If C EOT is detected before CB-3 MTTF (JOB DONE) is set, the SC-2 ERROR flip-flop sets and the Main Status Register must be read by the program to determine the cause of the error.

9.4.1.7 Beginning of Tape - Beginning of tape (C BOT) is asserted when the BOT reflective strip is detected by the tape transport. If BOT is detected before CB-3 MTTF (JOB DONE) is set, the SC-2 ERROR flip-flop (Figure 9-11) sets. The Main Status Register must be read by the program to determine the cause of the error.

9.4.1.8 Read/Compare Error - The read/compare operation is discussed in Paragraph 7.2.4.

9.4.1.9 Parity Error - The SC-1 PARITY ERROR flip-flop (Figure 9-15) is set if the TS03 detects any of the following errors.

1. C LRCE (Longitudinal Parity Error)
2. C CRCE (Cyclic Redundancy Check Error)
3. C VPE (Vertical Parity Error)

If SC-1 PARITY ERROR is set, the SC-2 ERROR flip-flop (Figure 9-11) sets when MTTF (JOB DONE) sets. SC-1 PARITY ERROR is cleared any time a File Mark is read from tape. During space operations, CB-1 SPACE H keeps SC-1 PARITY ERROR cleared (Figure 9-15) to prevent generation of erroneous parity errors. Note that the C VPE is cleared by the next good word read from tape and will not be seen unless it occurs as the last word read from tape.

9.4.1.10 File Mark (EOF) - The File Mark flip-flop (Figure 9-15) is set any time the TS03 detects a File Mark during a space, read, or read/compare operation.

9.4.1.11 Select Remote - SC-1 SELR L (Select Remote) (Figure 9-17) is true when the selected transport is OFFLINE (not ready). SC-1 SEL ERROR is set if SC-1 SELR L is lost during data transfer operation.

9.4.1.12 File Protect - File Protect is a 1 when write lockout (C WRL L) is asserted by the TS03, indicating that the selected transport has the write lockout ring removed. Transports without a write lockout ring will set the ILLEGAL FUNCTION flag during SC-1 PRESET time (Figure 9-12) if they are selected for a write or write File Mark operation.

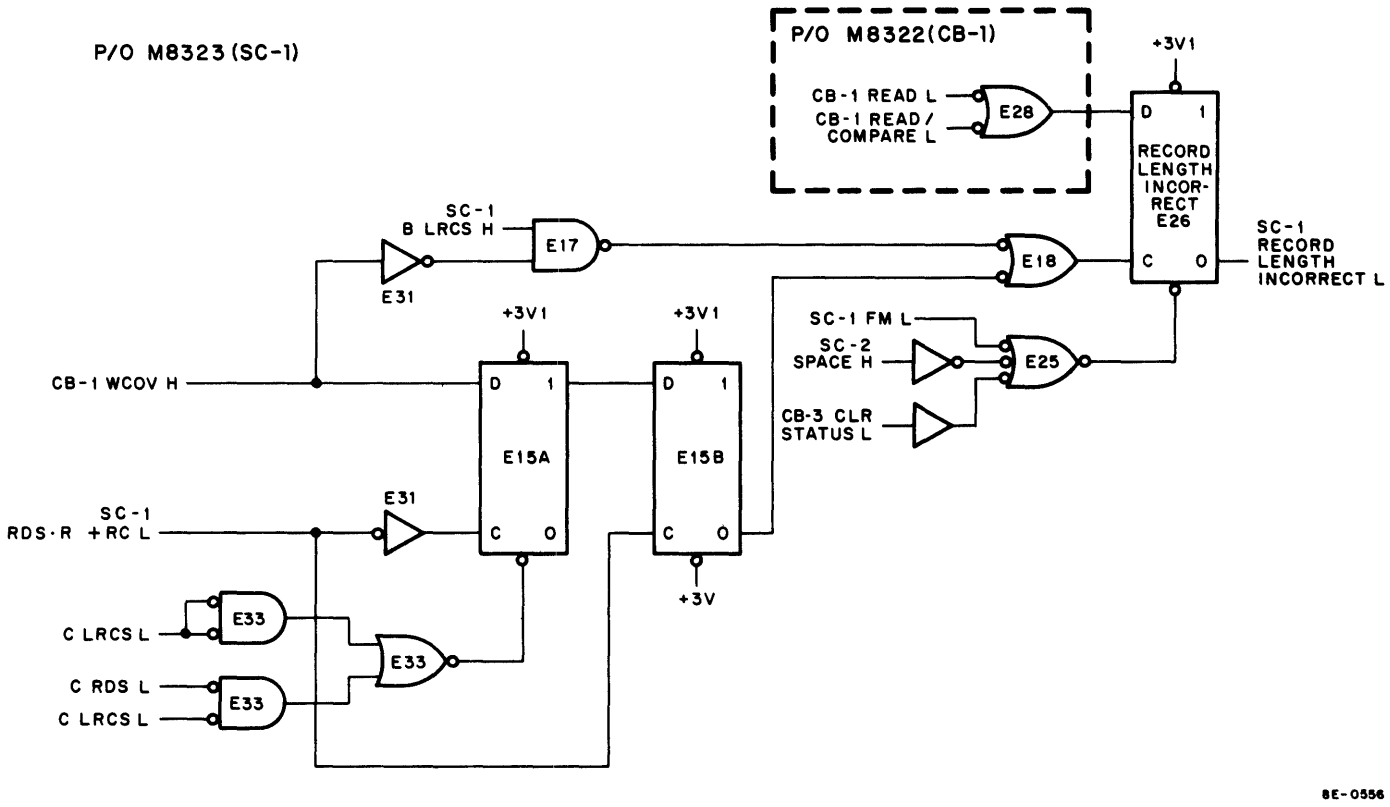


Figure 9-14 Record Length Incorrect Error Detection Logic

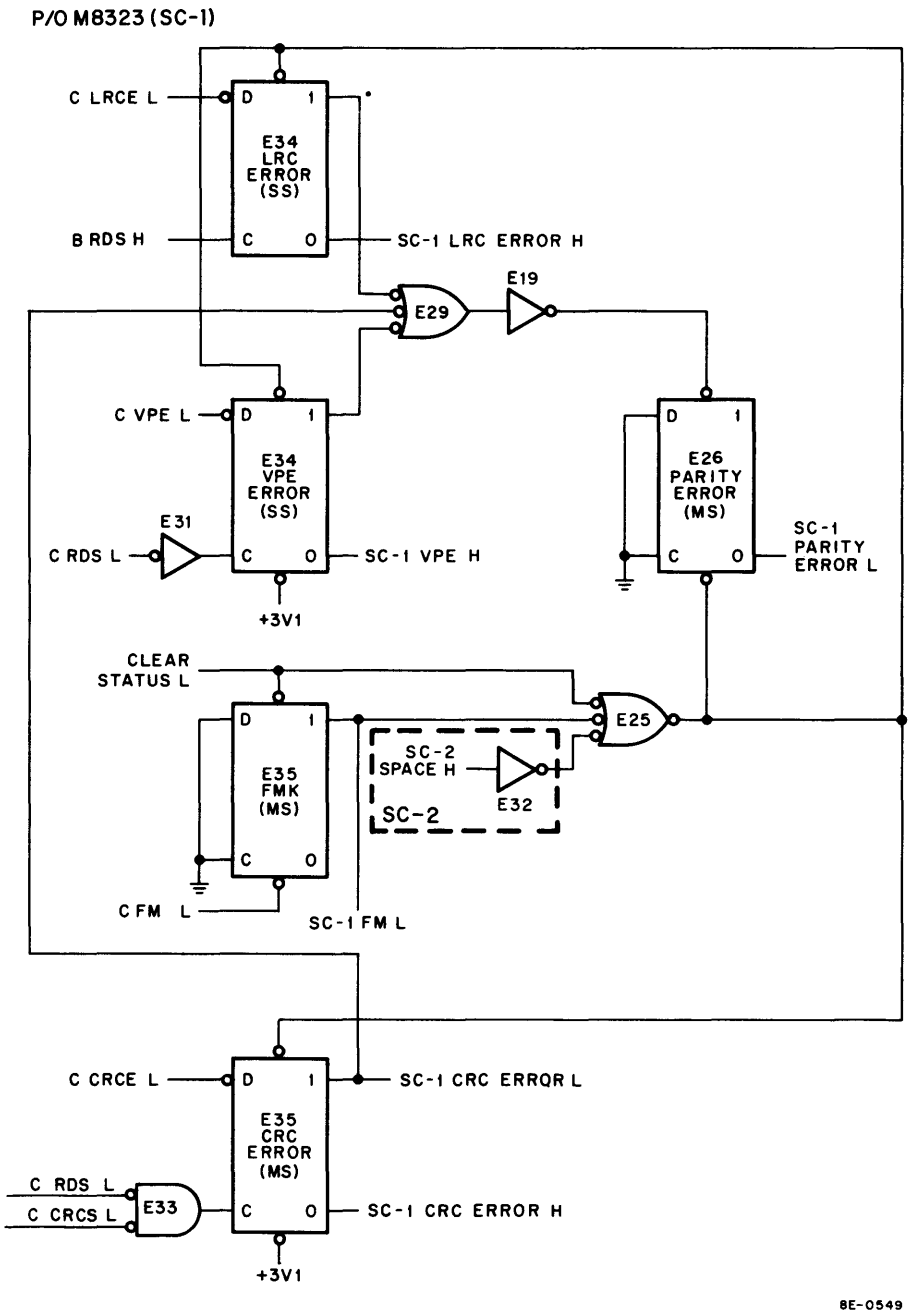


Figure 9-15 Parity Error Flags

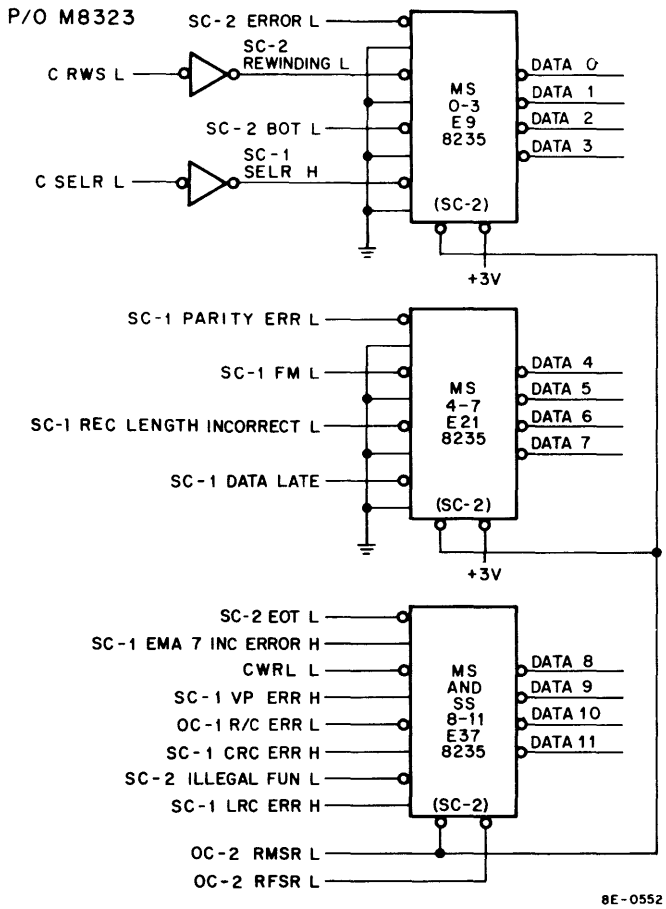


Figure 9-16 Main Status Register and Second Status Register Multiplexer

9.4.2 Second Status Register

The Second Status Register is read using the RFSR IOT (Figure 8-4). This IOT transfers the condition of the Second Status Register to the AC for evaluation by the program. The logic elements in the Second Status Register perform as follows.

9.4.2.1 EMA 7 Increment Error - RE-2 EMA 7 flip-flop (Figure 9-13) is set if the program tries to increment from Field 7 to Field 0 (RE-1 EMA INCREMENT bit must be set). If RE-2 EMA 7 H (Figure 9-10) is applied to the data input and RE-1 EMA INC L is asserted, the RE-2 EMA 7 flip-flop sets, which in turn sets the SC-2 ERROR flag when CB-3 MTTF is set (Figure 9-11). Refer to Paragraph 9.4.3 for a discussion of the EMA INC logic. The Second Status Register must be read by the program after CB-3 MTTF is set to determine the cause of the error.

9.4.2.2 Vertical Parity Error (C VPE) - The SC-1 VPE flip-flop (Figure 9-15) is set during a read or read/compare operation if the TS03 detects a vertical parity error and asserts C VPE L. SC-1 VPE is cleared when the next good word is read from tape. If SC-1 VPE is set at the end of an operation, the last word in the record was the one that set SC-1 VPE.

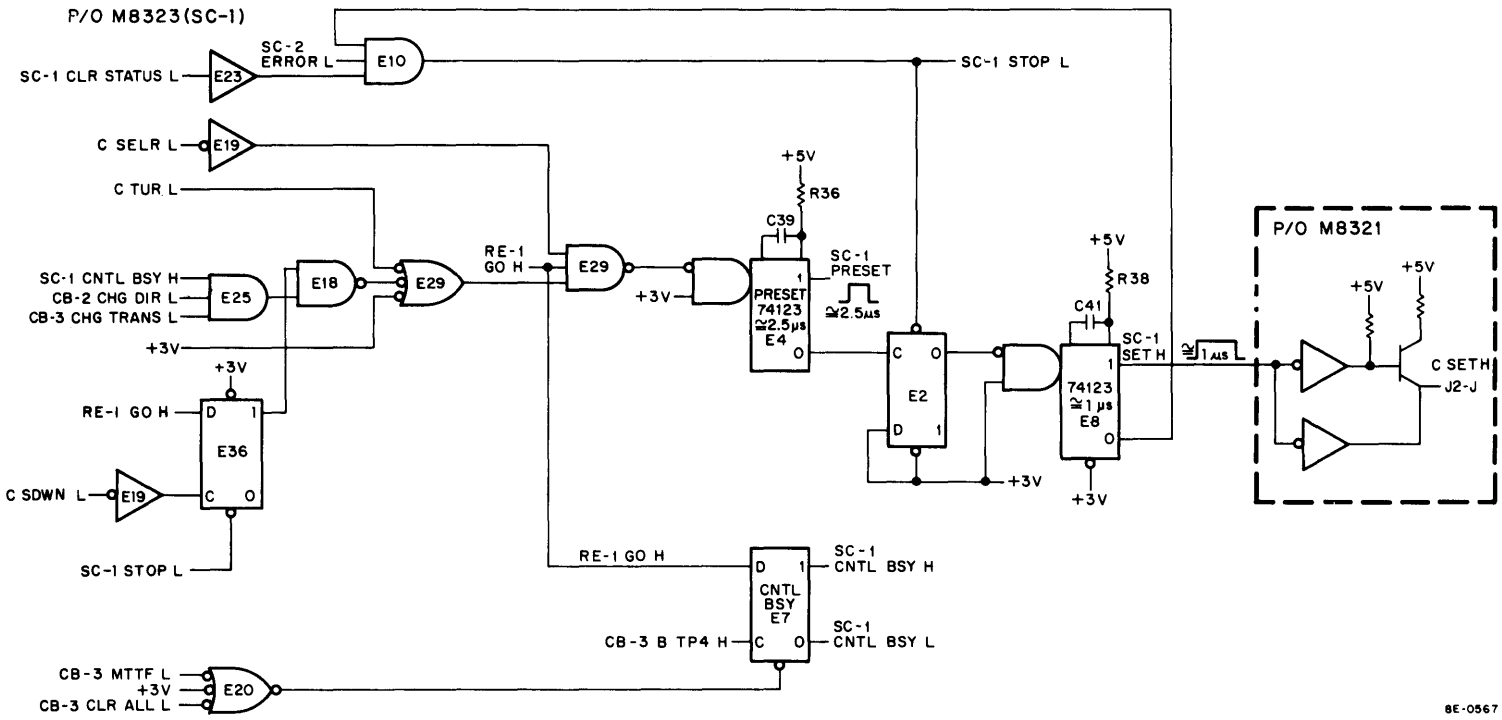


Figure 9-17 PRESET and SET Pulse Generation Logic

9.4.2.3 LRC ERROR - The SC-1 LRC ERROR flip-flop (Figure 9-15) sets if the TS03 detects an LRC error when the LRC character is read. The TS03 asserts C LRCE L when an error is detected and sets SC-1 PARITY ERROR and SC-1 LRC ERROR.

9.4.2.4 CRC ERROR - The SC-1 CRC ERROR flip-flop (Figure 9-15) sets if the TS03 detects a CRC error when it reads the CRC character from tape. The TS03 asserts C CRCE L when a CRC error is detected to set the SC-1 CRC ERROR flip-flop and the SC-1 PARITY ERROR flip-flop.

9.4.3 Main and Second Status Register Multiplexer

The contents of the Main Status Register and Second Status Register (Figure 9-16) are applied to three 8235 ICs. The 12 bits (Figures 7-4 and 8-6) from the Main Status Register are applied to the Data Bus if an RMSR instruction is executed by the program and the 4 bits from the Second Status Register (Figures 7-5 and 8-4) are transferred to the Data Bus if an RFSR instruction is executed by the program. Note that 8 bits of the Function Register (Figure 9-9) are also applied to the Data Bus when the RFSR instruction is executed by the program.

9.4.4 Extended Memory Address Increment Logic

The EMA bits (6, 7, and 8) in the Command Register (Figure 9-10) are used to select one of the memory fields during a data break operation if bit 6 in the Function Register is a 1. When bit 6 is set, the PDP-8 memory is treated as continuous memory instead of 4K blocks (Table 8-1). To accomplish this, the EMA bits must be incremented when the last memory location (7777) in each field is addressed and SC-1 COUNT CA L is asserted. The RE-1 EMA INC flip-flop (Figure 9-13) is set when the Current Address Register goes to all 0s and RE-1 EMA INC EN L is asserted (bit 6 in the Function Register is 1). The EMA bits in the Command Register are incremented each time bit 0 in the CA Register makes a 1 to 0 transition until the EMA bits are all 1s (RE-2 EMA 7). When RE-2 EMA 7 H is asserted, the NAND gate on the output of RE-1 EMA INC is disabled. If an attempt is made to increment beyond Field 7, the RE-1 EMA INC ERROR flip-flop is set by RE-2 EMA 7 H and the set side of RE-1 EMA INC. The RE-1 EMA INC flip-flop is cleared at TP3 time of BRK RQST and remains cleared until RE-2 CA 0 L makes a high-to-low transition at the end of a memory field.

9.4.5 Control Busy (CNTL BSY)

The SC-1 CNTL BSY flip-flop (Figure 9-17) is set by RE-1 GO and OC-2 B TP4 when bit 5 in the Function Register is loaded with a 1. SC-1 CNTL BSY is cleared when MTTF (JOB DONE) sets at the end of an operation or by CB-3 CLR ALL.

9.4.6 PRESET and SET Pulse Generator

Figure 9-17 shows the SC-1 PRESET and SC-1 SET pulse generation logic. The 74123 ICs are monostable multivibrators that generate a pulse on the output when the input signal makes a high-to-low transition. The duration of the output pulse is determined by an external resistor and capacitor, i.e., C39 and R36.

SC-1 PRESET is a 2.5 μs pulse (approximate time) that is triggered when the RE-1 GO bit (bit 5) in the Function Register is set. Note that C SELR L and C TUR L must be asserted to enable the gate when starting from a standstill condition. In a continuous mode of operation, C SDWN L allows the RE-1 GO signal to trigger the 74123 IC if CB-2 CHG DIR or CB-2 CHG TRANS are both high (false). If CB-3 CHG DIR or CB-3 CHG TRANS are asserted the TM8-E must wait for C SELR L and C TUR L. When SC-1 PRESET returns to the clear state, E2 is clocked, and if the SC-2 ERROR flag is not set the second 74123 IC is triggered. When the second 74123 IC is triggered, it outputs a 1.0 μs pulse (approximate time) that is applied to the TS03 to initiate tape motion. The E2 flip-flop is cleared by CB-3 CLR STATUS L, the SC-1 SET pulse, or the SC-2 ERROR flag.

9.4.7 Data Late Error Check Logic

The logic shown in Figure 9-18 is used to check the Data Late Error Logic (Figure 9-13). The processor timing is stopped at TP3 time by the assertion of SC-1 NOT LAST XFER and restarted by asserting SC-1 BUS STROBE.

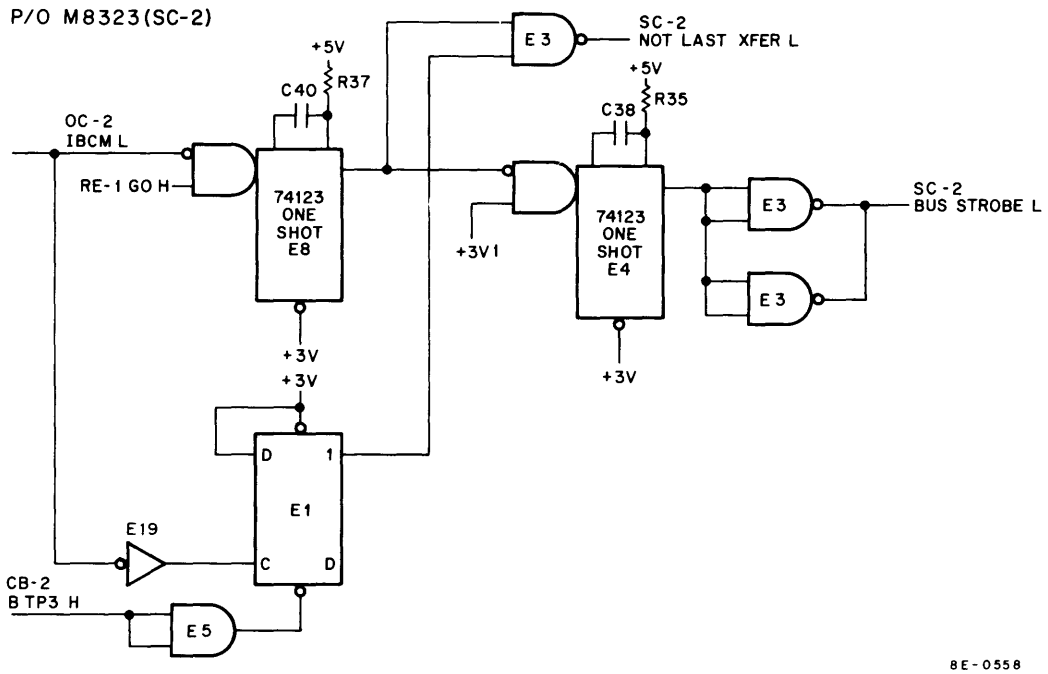


Figure 9-18 Data Late Error Check Logic

The 74123 ICs are monostable multivibrators that are triggered on a high-to-low transition of the input signal to generate an output pulse. The duration of the output pulse is determined by an external capacitor and resistor, i.e., C40 and R37. When the CKDL instruction is executed by the program, OC-2 IBCM L is asserted to trigger the first 74123 IC and generate a long timing pulse, which is ANDed with E1 flip-flop and applied to the Omnibus as SC-1 NOT LAST XFER to stop processor timing. E1 is cleared at TP3 time and the trailing edge of the first 74123 causes the second 74123 IC to output a pulse. This pulse asserts SC-1 BUS STROBE L and restarts processor timing. During the time processor timing was stopped, an attempt was made by the TM8-E to transfer data. The SC-1 DATA LATE ERROR flip-flop (Figure 9-13) should be set, because the TM8-E would normally transfer several words in a time period this long. If the SC-1 DATA LATE ERROR flip-flop does not set, this group of logic is not working properly.

9.5 M8322 CONTROL MODULE

The logic elements of the M8322 Control module are described in the following paragraphs.

9.5.1 Control Function Decoder

The control function decoder (Figure 9-19) is an 8251 IC that decodes the three most significant bits (FR0–FR2) of the Function Register (Table 8-1) to set up the control logic for the tape transport operation.

NOTE

This decoder is identical to the output control function decoder (Paragraph 9.2.7).

The 8251 IC is a BCD-to-decimal decoder that decodes bits FR0 through FR2 and produces a low on one output line of the IC for each 3-bit combination, i.e., 100_2 causes pin 9 to be low and indicates a write operation. The outputs of the IC are NORed to generate one signal to represent a combination of operations, i.e., CB-1 SP REV L and CB-1 SP FWD L are NORed to generate CB-1 SPACE H, to reduce the number of signals that are applied to elements of the control logic.

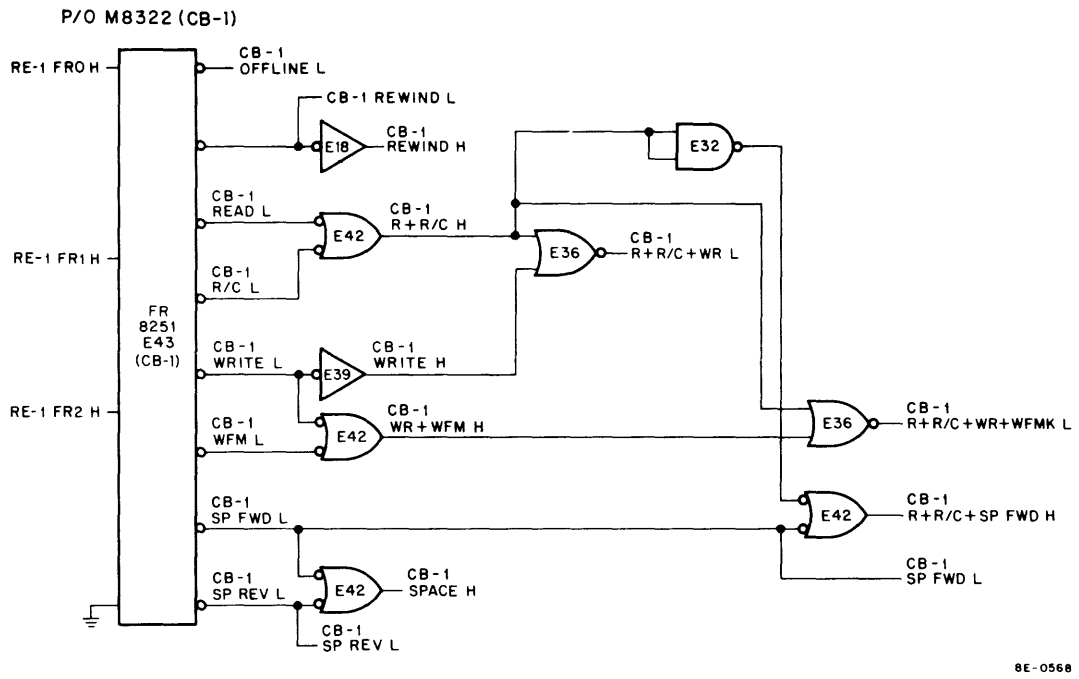


Figure 9-19 Control Function Decoder

9.5.2 Data Break Request Logic

Figure 9-20 shows the logic used to make a BRK RQST during data transfer operations. The CB-1 BRK RQST flip-flop is cleared and CB-1 BRK RQST H is asserted when the following conditions exist during read, write, and read/compare operations.

1. Write operation and SC-1 SET H are asserted for the first CB-1 BRK RQST at the beginning of a write operation.

2. If CB-1 WRITE 1st 7H is low and SC-1 WRS L (write strobe) is asserted during a write operation. Refer to Paragraph 9.5.10 for origin and discussion of these signals.

3. If CB-1 READ 9 or SC-2 READ 2nd 7 is asserted (Figure 9-20) during a read operation.

4. If an SBRM instruction (for maintenance only) is executed by the program.

Note that the CB-1 BRK RQST flip-flop is set for only write, read, or read/compare operations, which are the only operations requiring data transfers. CB-1 BRK RQST is set and CB-1 BRK RQST H is negated by CB-1 MAC ACC L at TP1 time when the BRK RQST is accepted by the processor. The BRK RQST flip-flop is negated by SC-1 DATA LATE, CB-3 CLR ALL, RECORD LENGTH INCORRECT, or CB-1 WCOV if RE-1 ENAB CHK CHAR is not asserted. E24 is cleared at the beginning of each data transfer operation by SC-1 PRESET H so that SC-1 RECORD LENGTH INCORRECT, CB-1 WCOV, or SC-2 ERROR can be reported during the operation and stop data transfers if these errors occur.

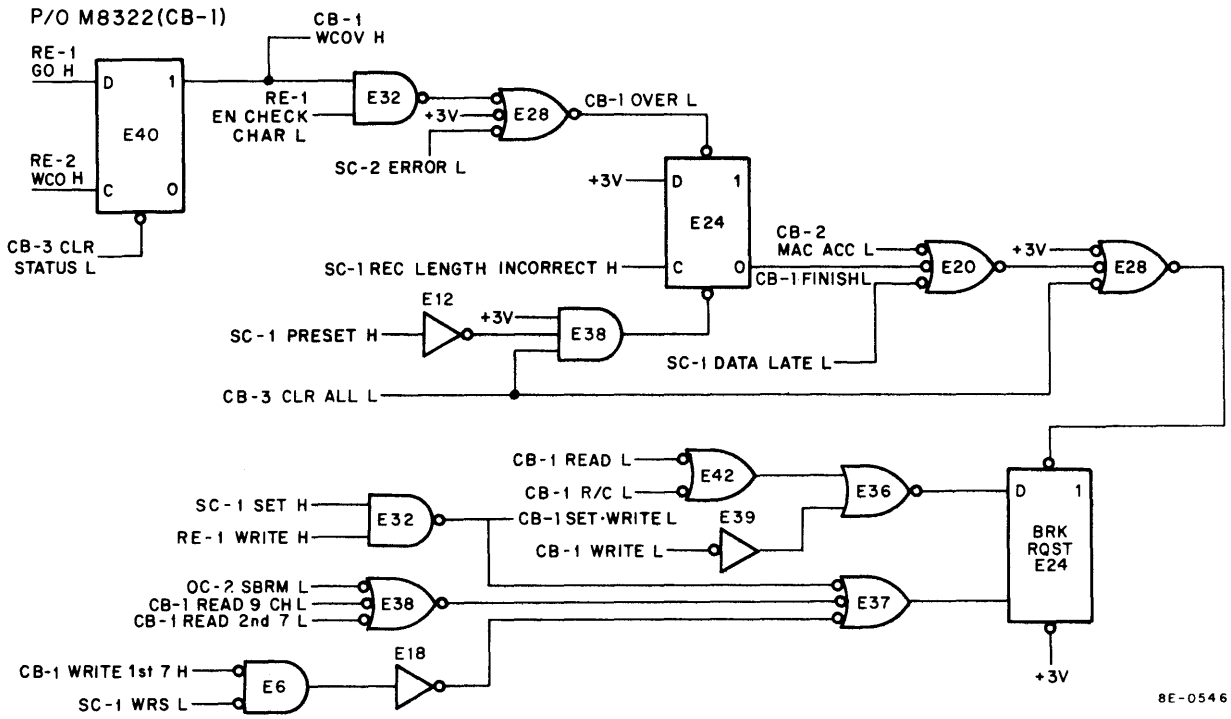


Figure 9-20 Data Break Control Logic

9.5.2.1 Word Count Overflow Logic – The CB-1 WCOV flip-flop (Figure 9-20) is set by RE-2 WC0 L when bit 0 in the WC Register makes a high-to-low transition (Figure 9-9). The set side of CB-1 WCOV is applied to NAND gate E32, which has as its other input RE-1 ENAB CHK CHAR L. If bit 4 in the Function Register (Table 8-1) is 0, RE-1 ENAB CHK CHAR is high and CB-1 WCOV (Figure 9-20) sets E24 flip-flop which causes CB-1 BRK RQST to negate and stop data transfers. If bit 4 in the Function Register is a 1, RE-1 ENAB CHK CHAR L is asserted and CB-1 WCOV does not set E24. This allows two more data breaks to transfer the CRC and the LRC character on a Read from the transport to memory. CB-1 WCOV is cleared by CB-3 CLR STATUS when a CLF instruction is executed by the program.

9.5.3 Data Break Priority Logic

The priority of the TM8-E (Figure 9-21) is established by removing one of the A jumpers (A0–A5) and installing one of the B jumpers (B0–B5); thus to establish a 0 priority (the highest priority) for the TM8-E, remove A0 and install B0. By this action all five NAND gates are disabled and the output of E9 is high, which enables E21. This enables the set side of E26 to be applied to the CB-2 MAC 1 and CB-2 MAC 2 flip-flops and allows the TM8-E to begin a data break operation at TP4, because the TM8-E has been assigned the highest priority. No other peripheral using the data break interface can have its A0 jumper removed and its B0 jumper installed. Note that when NAND gate E34 is enabled at TS4 time, DATA 0 line is low (the TM8-E B0 line is in place). Since all of the other peripherals are monitoring the Data Bus, one of the NAND gates in their priority logic is enabled and their BRK RQST is not accepted.

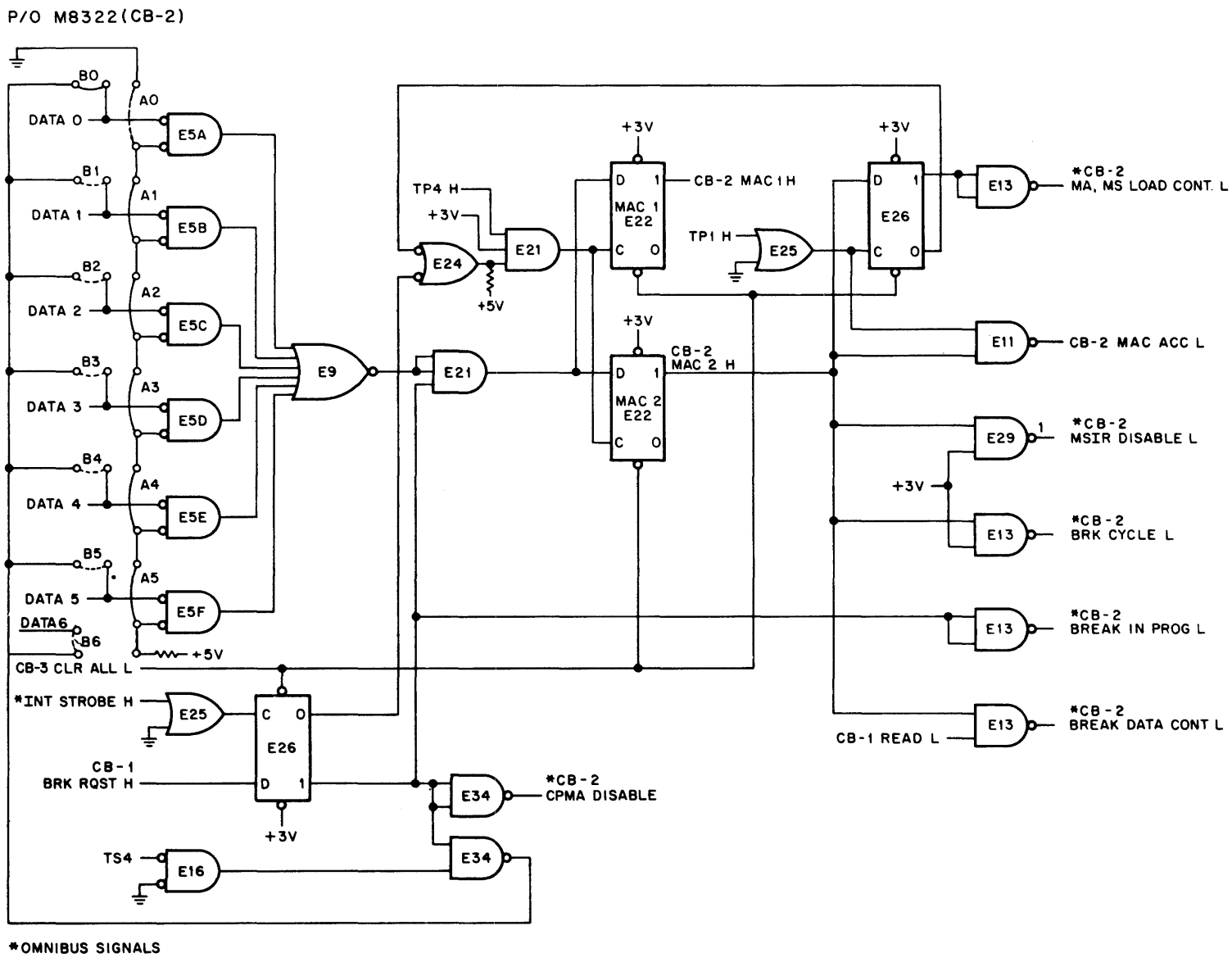


Figure 9-21 Priority and Processor Control Logic with 0 (Highest) Priority Installed

As a further example, consider what happens if the TM8-E ranks third in the priority structure. This priority is established by removing jumper A2 and installing jumper B2. Because jumpers A0 and A1 are left in place, two other peripherals can keep the TM8-E from making a BRK RQST. If the second highest priority peripheral has a BRK RQST at the same time as the TM8-E, its interface brings the DATA 1 line low during TS4 and NAND gate E5B is enabled. The output of E5B causes the output of E9 to go low and disable AND gate E21. This prevents the set side of E26 from setting CB-2 MAC 1 and CB-2 MAC 2 until the other peripheral completes its data break operation. As implied, priority decreases from 0 through 11, and the TM8-E is assigned any priority between 0 and 5 by removing the correct A jumper and installing the correct B jumper.

9.5.4 Processor Control Logic

The logic shown in Figure 9-21 is used to control the PDP-8 processor during a single cycle data break operation. If E21 is enabled by the priority logic and the set side of E26, CB-2 MAC 1 and CB-2 MAC 2 are set to assert the Omnibus signals (the Omnibus signals are explained in Chapter 9 of the *PDP-8/E and PDP-8/M Small Computer Handbook)* and take control of the processor for a single cycle data break operation. Note that MA, MS is not asserted until TP1 time. CB-2 BREAK DATA CONT L, which controls direction of data flow on the Data Bus, is controlled by READ L. During a read operation, CB-1 READ L is asserted and data is transferred from tape to memory. During write and read/compare operations, CB-1 READ L is high to transfer data from memory to the TM8-E. CB-2 MAC 1 and CB-2 MAC 2 are cleared by the output of AND gate E21 at TP4 time if BRK RQST is removed. CB-1 BRK RQST (Figure 9-20) is cleared by CB-2 MAC ACC L at the same time CB-2 MAC 1 and CB-2 MAC 2 are set to start a single cycle data break. The TM8-E continues to make break requests and to transfer data to or from memory until the WC Register reads all 0s (WCOV).

9.5.5 MTTF (JOB DONE) Logic

MTTF (Job Done flag shown in Figure 9-22) is set by one of the following conditions to indicate that a specified function is complete or cannot be performed.

1. C LRCS (LRC character read from tape at the end of a record) during a read, read/compare, write, or write File Mark operation.

2. The C LRCS is read from tape during a space operation.

3. File Mark, EOT, or WCOV are encountered during a space operation.

4. The selected transport is given a command to rewind and C RWS is asserted by the selected transport to indicate rewind has started.

5. The selected transport is given the CB-1 OFFLINE command and C SEL ERR L is asserted by the TS03.

6. If IOT LDBR is executed by the program and CB-1 WCOV L is asserted.

9.5.6 Interrupt Logic

The Interrupt logic (Figure 9-22) asserts INT RQST L, which is serviced by the processor (i.e., perform a flag check routine) when one of the following conditions exist.

1. Bit 6 in the Command Register (Interrupt Enable on SC-2 ERROR flag) is a 1 and the SC-2 ERROR flag is set (Figure 9-12). Note that the SC-2 ERROR flag does not set until after CB-3 MTTF is set unless CB-3 SEL ERR or SC-2 ILLEGAL FUN is set at the beginning of an operation.

2. Bit 5 in the Command Register (Interrupt Enable on Job Done flag) is a 1 and the CB-3 MTTF flag is set.

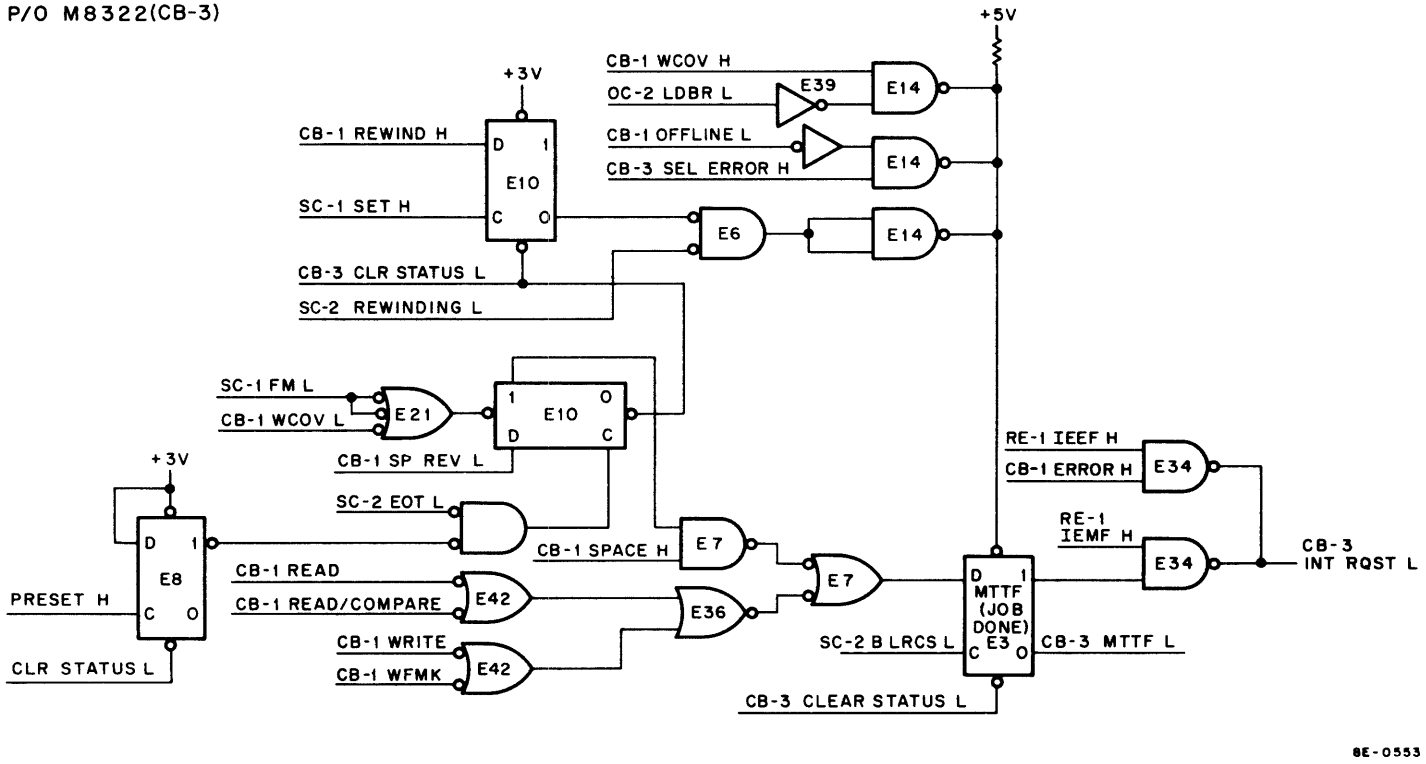


Figure 9-22 MTTF (JOB DONE Flag) and Interrupt Request Logic

9.5.7 Change Transport Control Logic

Figure 9-23 shows the logic used to generate the CB-3 CHG TRANS L signal when a new transport is selected by the program. If an LCMR instruction is executed by the program, flip-flop E3 clears (Figure 9-23) and enables NAND gate E7. At TP4 time, the output of E7 supplies a clock input to E8 and if any of the inputs (RE-1 SEL 0 - RE-1 SEL 2 and RE-1 B SEL 0 - RE-1 B SEL 2) to the E4 Exclusive-OR gates are different, E8 zeroes and asserts CB-3 CHG TRANS L. The output of E7 also clocks the E3 flip-flop, causing it to set and disable E7. If C TUR L and C SDWN L are asserted or SEL REM L is negated, NAND gate E11 is enabled at TP4 time. LBCM L is asserted to load the Buffered Command Register with bits RE-1 SEL 0 through RE-1 SEL 2 from the Command Register (Figure 9-10). If CB-3 CHG TRANS is set and C RWS L is asserted, RE-1 LBCM L is asserted to load the BCM (Figure 9-23). CB-3 CLR STATUS resets the CB-3 CHG TRANS flip-flop. The Buffered Command Register is also loaded with RE-1 SEL 0 through RE-1 SEL 2 when CB-3 CLR ALL is asserted (CLF instruction executed by the program).

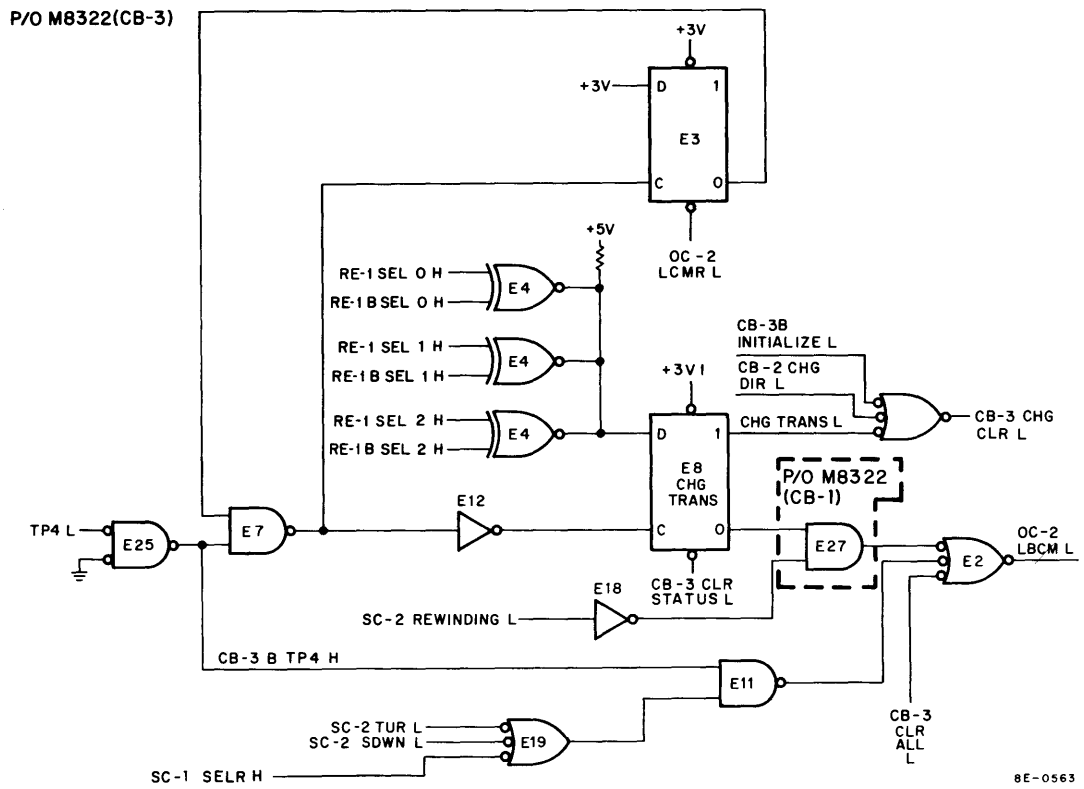


Figure 9-23 Change Transport and Buffered Command Register Control Logic

9.5.8 Change Direction Control Logic

Figure 9-24 shows the logic used to detect a change in direction of tape movement. E35 flip-flop is cleared by SC-1 SET H at the beginning of all operations except space reverse, rewind, or offline. This applies a high to the input of E4, which is the same as the high out of E19. E4 has a high output if both inputs are equal and a low output if the inputs are unequal. If CB-1 SP REV L, CB-1 REWIND L, or CB-1 OFFLINE L are asserted, the output of E19 goes low and the output of E4 (CB-3 CHG DIR L) is asserted. CB-3 CHG DIR L forces the control to wait for C TUR L and C SELR L before starting a new operation.

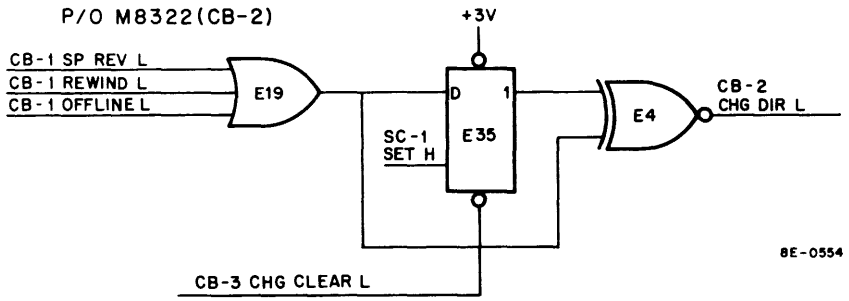


Figure 9-24 Change Direction Detection Logic

9.5.9 Write Data Ready Logic

Figure 9-25 shows the write data ready logic. C WDR H is applied to the selected transport when the TM8-E is ready to start a write operation. SC-1 SET H and CB-1 WRITE H enable NAND gate E32 to set flip-flops E23A and E23B. This enables E27B to assert CB-1 WDR H. E23A is cleared when CB-1 WCOV L is asserted, which in turn disables NAND gate E27B and CB-1 WDR H goes low. This operation disables NAND gate E27A and C WDR H goes low. SC-1 DATA LATE L and SC-2 ERROR L clear both E23 flip-flops if these errors occur during a write operation. If a CLF instruction is executed by the program, CB-3 CLR STATUS sets E23A and E23B to cause CB-1 WDR H to go low, which terminates a write operation.

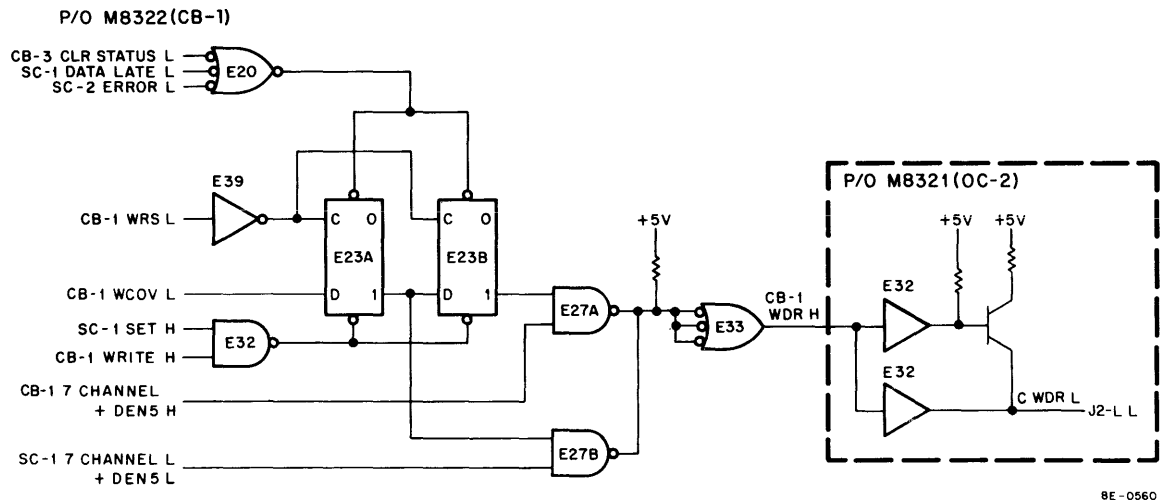


Figure 9-25 Write Data Ready Logic

9.5.10 Read and Write Control Logic

The logic shown in Figure 9-26 is used to generate control signals during read and write operations. Table 9-3 shows the levels of the control signals and the logic used to assert each signal for each read and write operation on the transports.

The Read and Write control signals are applied to the CB-1 BRK RQST control logic to determine when a BRK RQST is to be made by the TM8-E (Figure 9-20). CB-1 BRK RQST is clocked on the falling edge of the SC-1 RDS or SC-1 WRS pulses. Refer to Drawing D-TD-TM8-E-1, sheets 1 through 8, for the timing diagrams that illustrate these operations.

Table 9-3
Read and Write Control Logic Signal Levels

Operation	SC-1 RDS L	SC-1 WRS L	CB-1 READ 9 L	CB-1 READ 1st 7 L	CB-1 READ 2nd 7 L	CB-1 WRITE 9 L	CB-1 WRITE 1st 7 L	CB-1 WRITE 2nd 7 L	Enabled Gate	Condition of E40
Read a 9-bit Character From Transport	low pulse	high level	low pulse	high level	high level	high level	high level	high level	E32	*
Read 1st 7-bit Character From Transport in Core Dump Mode	low pulse	high level	high level	low pulse	high level	high level	high level	high level	E37A	Set to 1 state on rising edge of C RDS
Read 2nd 7-bit Character From Transport in Core Dump Mode	low pulse	high level	high level	high level	low pulse	high level	high level	high level	E37B	Reset to 0 state on the rising edge of RDS
Write a 9-bit Character on Transport	high level	low pulse	high level	high level	high level	low pulse	high level	high level	E41C	*
Write 1st 7-bit Character on Transport in Core Dump Mode	high level	low pulse	high level	high level	high level	high level	high level	low pulse	E41A	Set to 1 state on rising edge of C WRS
Write 2nd 7-bit Character on Transport in Core Dump Mode	high level	low pulse	high level	high level	high level	high level	low level	high level	E41B	Reset to 0 state on rising edge of C WRS

*Condition of E40 does not matter.

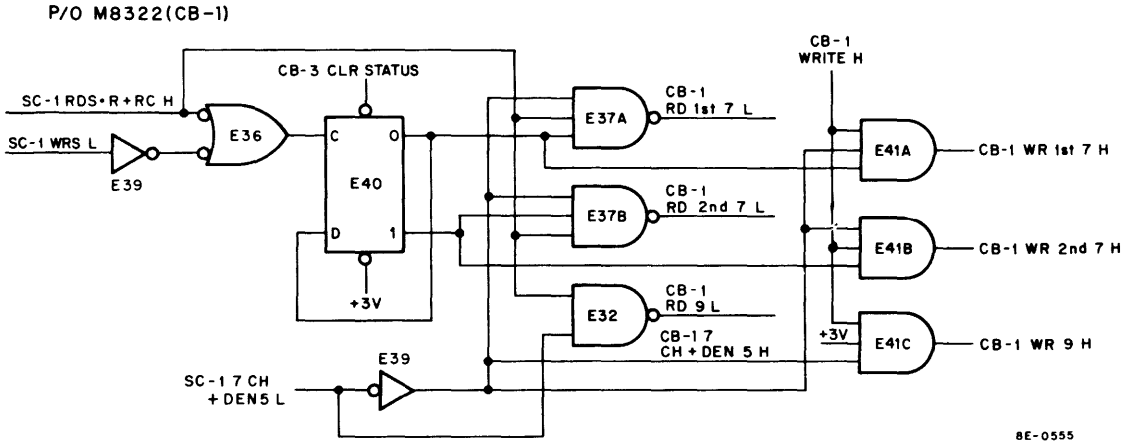


Figure 9-26 Read and Write Control Logic

9.5.11 Data Multiplexer Control Logic

Figure 9-27 shows the Data Multiplexer Control logic used to select data read from tape, from memory, or from the AC as input to the Data Register (Figure 9-5). Table 9-2 shows the level of CB-2 DB MPXA H and CB-2 DB MPXB H for all TM8-E operations.

9.5.12 POWER OK Logic

The POWER OK logic shown in Figure 9-28 is used to assert CB-3 CLR ALL if PDP-8 power falls below a certain level. If PWR OK H goes low, NAND gate E16 is enabled to assert CB-3 CLR ALL. This initializes all TM8-E logic and the TS03.

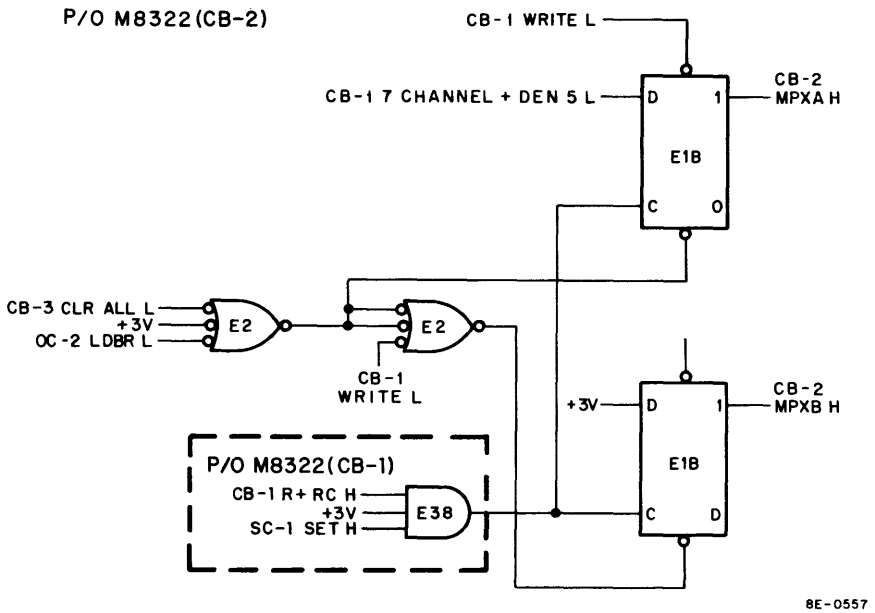


Figure 9-27 Data Multiplexer Control Logic

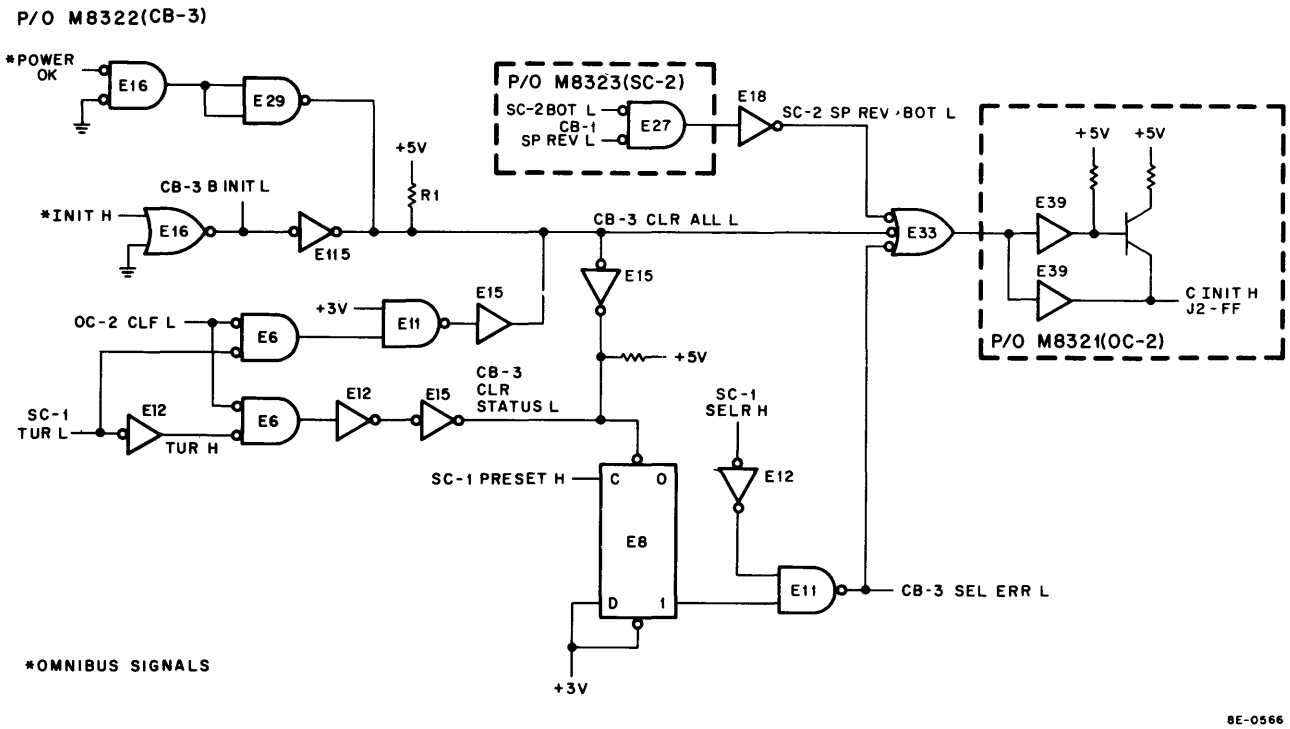


Figure 9-28 Initialize and Clear Logic

9.5.13 Initialize Logic

INIT H (Figure 9-28) is asserted when the PDP-8 is powered up or by pressing the CLEAR key on the PDP-8 power control console. Note that INIT H is not the same signal as C INIT H; C INIT H is used to clear all logic in the TS03 when the following conditions exist.

1. INIT H is asserted by the processor.
2. If the tape unit is ready (C TUR L true) when a CLF instruction is executed by the program (CB-3 CLR ALL is asserted).
3. If a space reverse operation is attempted and transport is at BOT.
4. If the CLT instruction is executed to assert CB-3 CLR ALL.

CHAPTER 10
GENERAL INFORMATION

10.1 GENERAL DESCRIPTION

The TS03 DECmagtape Transport is a synchronous digital tape unit capable of reading and writing industry-compatible tapes and read-after-write operation. The unit is designed for applications requiring high reliability at moderate tape speeds.

The TS03 is designated as either a master transport (TS03M) or a slave transport (TS03S). The TS03M comprises a TS03S and a M8920 adapter module with the M8920 adapter interfacing up to two TS03S slave units (Figure 11-1). Thus a TM8-M System will have one TS03M Transport and possibly one TS03S Transport.

The TS03 contains all the electronics necessary to accept, format, and record data and to retrieve, check, and output data. To accomplish this, the TS03 performs the following functions:

Tape motion control
Tape formatting
Parity generation
Cyclic redundancy check (CRC) character generation
Longitudinal redundancy check (LRC) character generation
Interrecord gap control
Even parity zero character conversion
Status monitoring
Parity, CRC character, and LRC character error detection
File protection

The TS03 is a 9-track, 800 bpi unit with a standard tape speed of 12.5 in. per second and a data transfer rate of 10 kHz.

10.2 PHYSICAL DESCRIPTION

The transport portion of the TS03 is completely housed in a 19 in. wide by 17 in. deep by 9 in. high chassis; the adapter portion is contained on a hex height module which mounts just below the chassis in a special mounting bracket. The transport (Figure 10-1) contains the read/write and motion control electronics. The adapter module (Figure 10-1) contains the formatting, parity, CRC, gap control, and error detection electronics.

10.3 ELECTRICAL AND MECHANICAL SPECIFICATIONS

Tape (Computer Grade)

Width	0.5 in. (1.27 cm)
Thickness	1.5 mils (0.038 mm)
Tension	8.0 oz (227 g)
Reel Diameter	To 7.0 in. (17.78 cm)
Capacity	600 ft (182.40 m)
Reel Hub	3.69 in. (9.37 cm) dia. (per industry standards)

Reel Braking	Dynamic
Recording Mode (Industry-Compatible)	NRZI
Tape Drive	Single capstan
Tape Speed	12.5 in./sec
Instantaneous Speed Variation	±3%
Long-term Speed Variation	±1%
Start/Stop Displacement	0.1875 in. (0.476 cm)
Start/Stop Time at 12.5 in./sec	30 ms
Rewind Speed	75 in./sec(190.5 cm)
Magnetic Head Assembly (Write to Read Gap Displacement)	
Dual Gap Nine-Track	0.15 in. (0.38 cm)
Read After Write Interchannel Displacement Error (Measured with Master Skew Tape)	
Write	150 μin. (3.8 μm) maximum
Read	150 μin. (3.8 μm) maximum
Erase Head	Full width
Beginning-of-Tape (Load Point) and End-of-Tape Reflective Strip Detection (Industry-Compatible)	Photoelectric
Broken Tape Detection	Photoelectric
Dimensions (Figure 10-2)	
Transport Mounting (Horizontal)	Standard 19 in. (48.26 cm) RETMA rack
Height	8.72 in. (22.14 cm)
Width	19.00 in. (48.26 cm)
Depth (From Mounting Surface)	14.38 in. (36.53 cm)
Depth (Overall)	16.88 in. (42.88 cm)
Weight	35 lb (15.85 kg)
Shipping Weight	45 lb (20.38 kg)
Operating Environment	
Ambient Temperature	+2° to +50° C
Relative Humidity (Noncondensing)	15% to 95%
Altitude	To 30,000 ft (9120 m)
Power Requirements	115/230 Vac, 50 to 500 Hz, single phase 200 VA nominal; 300 VA maximum

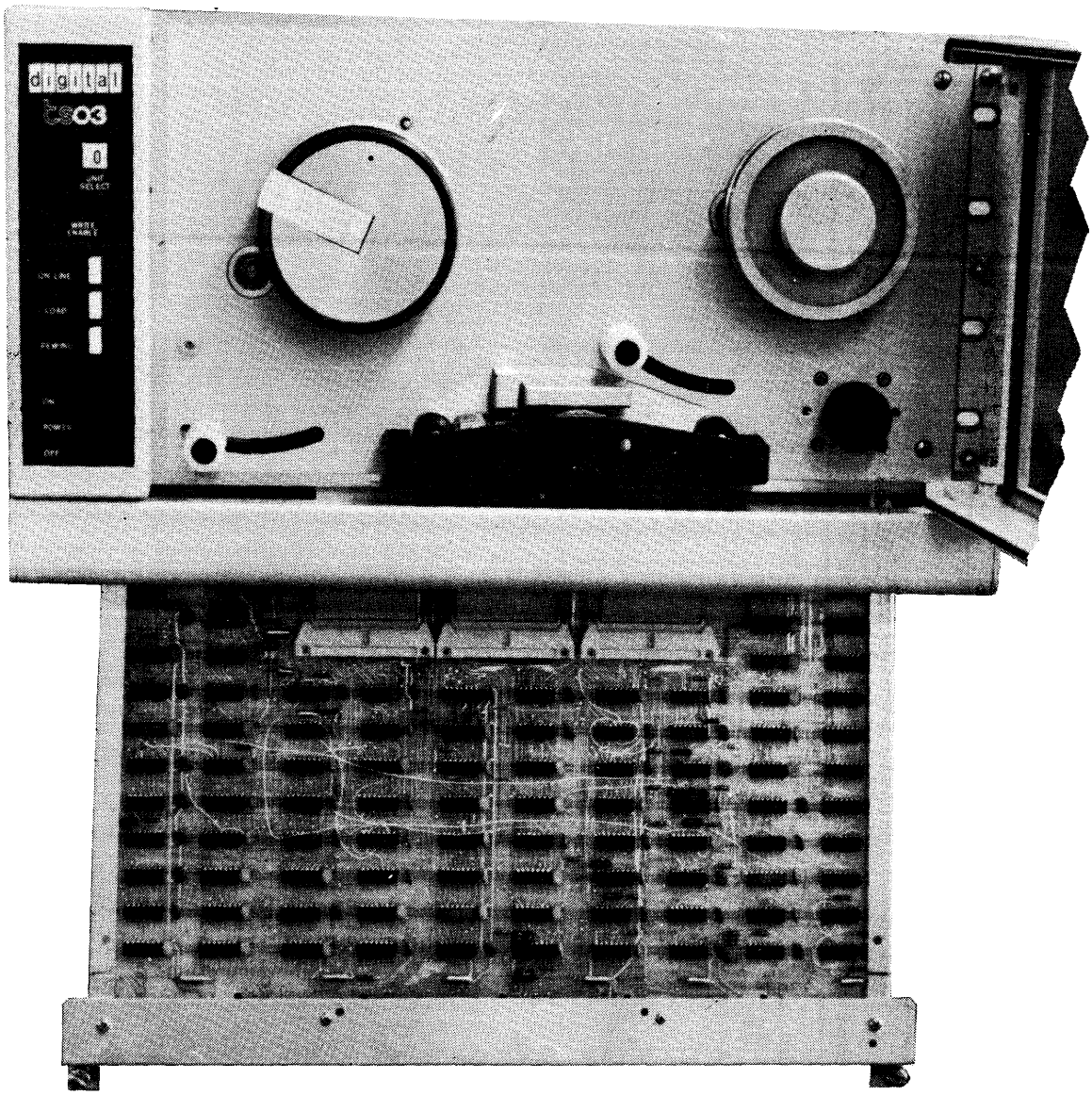


Figure 10-1 TS03 Transport and TS03 Adapter Module (M8920)

NOTE: DIMENSIONS FIRST SHOWN ARE IN INCHES.
DIMENSIONS IN PARENTHESES ARE IN CENTIMETERS.

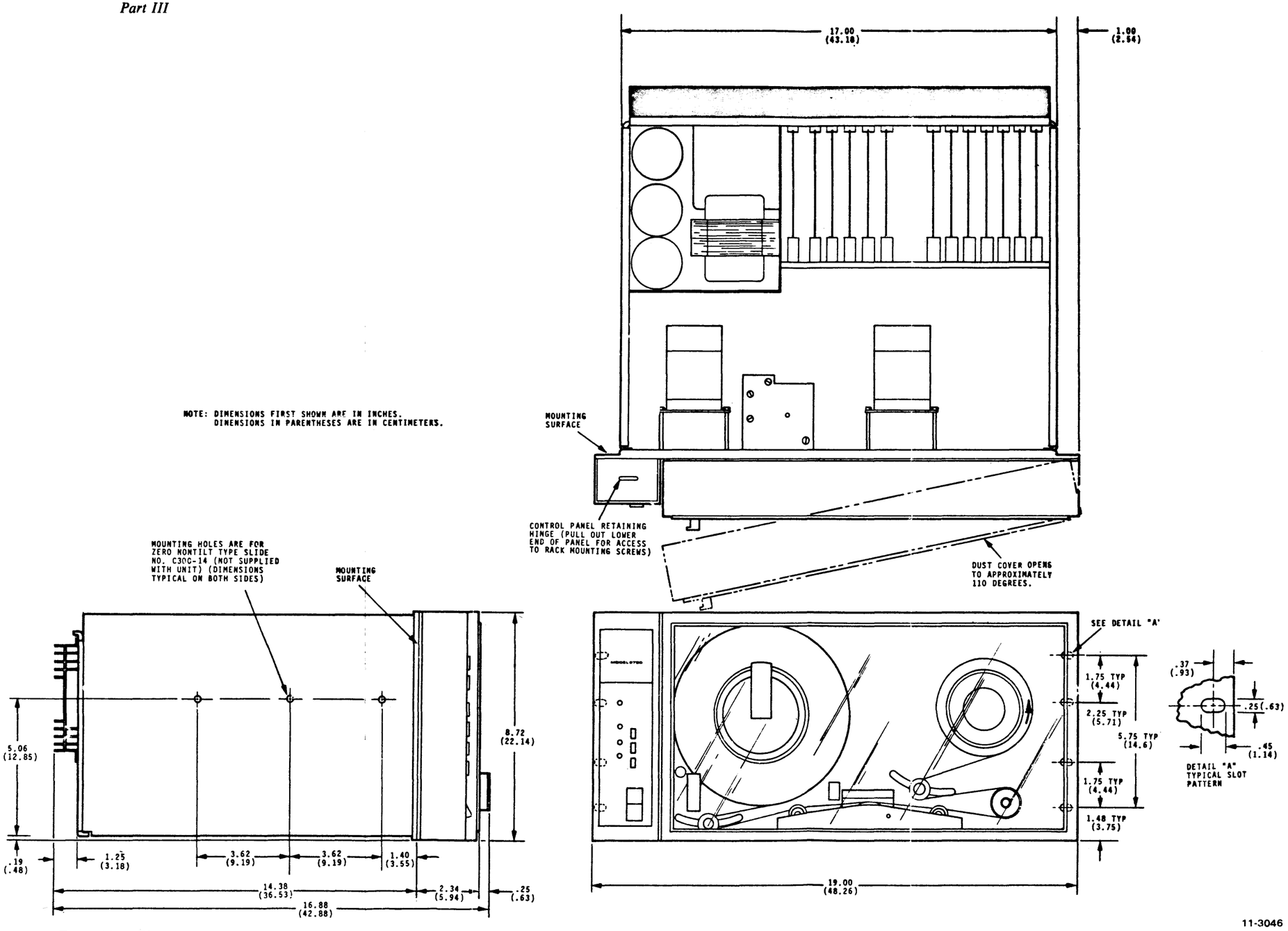


Figure 10-2 TS03 Transport
Physical Dimensions

PART III
TS03 DECmagtape TRANSPORT

CHAPTER 11
THEORY OF OPERATION

11.1 INTRODUCTION

This chapter provides a complete description of the TS03 to the functional block level. Functionally, the TS03 can be divided into four major blocks (Figure 11-1):

Adapter Logic
Transport Control Logic
Servo System
Data Section

The adapter logic interfaces the TS03 transport to the controller. In response to commands from the controller, the adapter:

1. Formats the data on the tape.
2. Generates motion signals to start and stop the tape drive, to move the tape forward or backward, and to move the tape at normal read/write speed or at a higher speed during a rewind operation.
3. Generates strobes to write data and CRC, LRC, and file mark characters on tape.
4. Generates write strobes to notify the controller to send the next write character.
5. Transmits read strobes received from the tape transport out to the controller.
6. Generates parity and the CRC characters for recording on the tape.
7. Performs parity, CRC, and LRC error checks on all read data.
8. Detects file mark records on the tape and notifies the controller.

The Control logic:

1. Controls ramp voltage to the servo, thereby controlling direction and speed of tape movement.
2. Generates control signals to the data section which enable and disable the read and write amplifiers.
3. Controls the erase head.

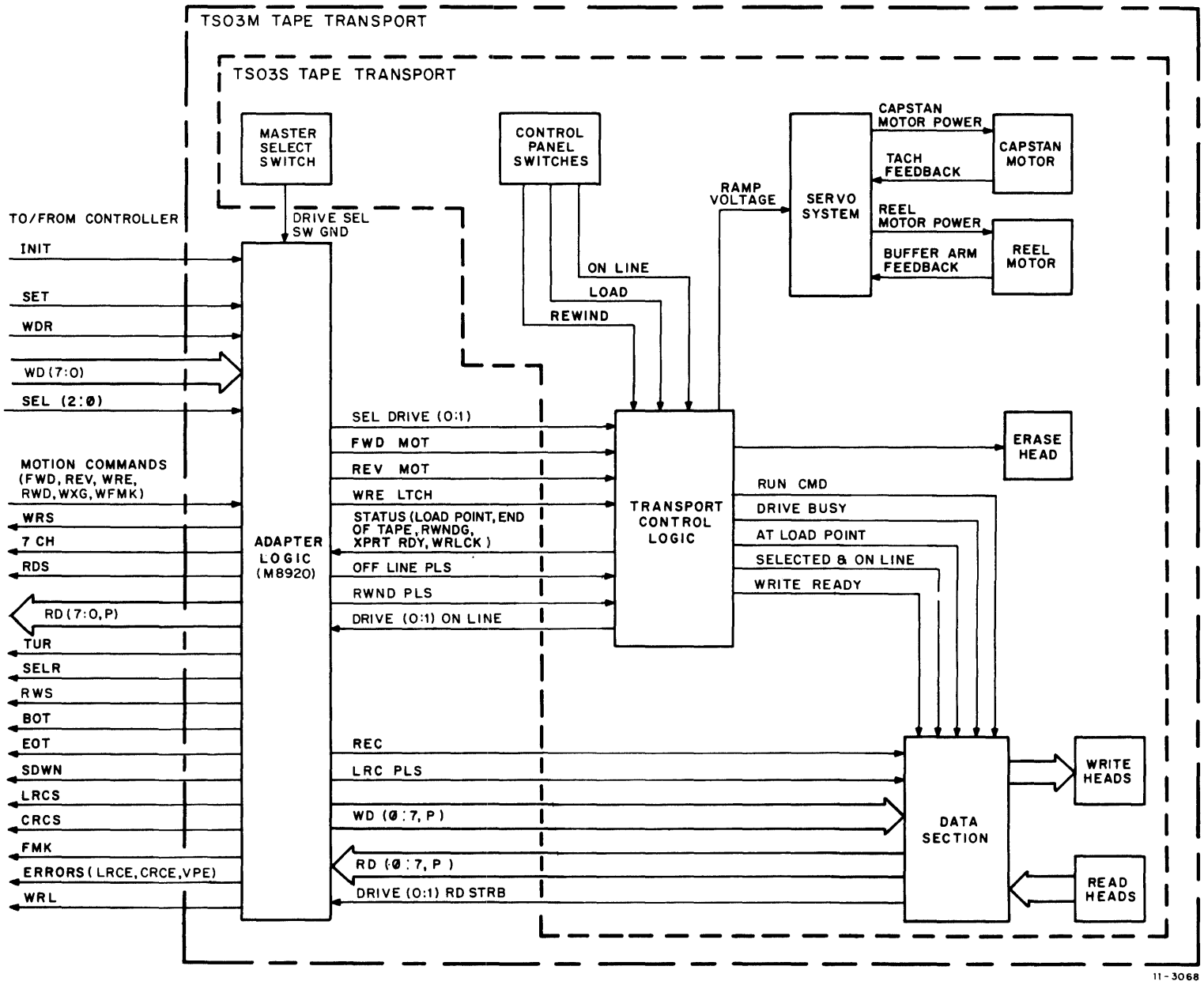


Figure 11-1 TS03 Block Diagram

The servo system consists of the electronics and electromechanical components that are required to advance the tape past the magnetic heads at accurately controlled speeds while maintaining constant tape tension. The servo system is composed of two subsystems: the capstan subsystem, which drives the tape at accurately controlled speeds, and the reel servo subsystem, which maintains constant tape tension.

The data section consists of read and write amplifiers, output drivers, and timing and control logic. The data section controls the read/write heads and generates a read data strobe that is used by the adapter logic to transfer data out to the controller.

11.2 TRANSPORT OPERATIONS

The TS03 performs three basic types of operations: write, read and rewind; all other operations are simply variations. The following paragraphs explain how these operations are performed (Figure 11-1).

Once the controller initializes the adapter logic by asserting INIT, the controller must select the transport (drive 0 or 1) and parity sense (odd or even) before any operations can be performed.

When the controller selects a transport via the SEL lines, the adapter asserts SEL (select) to the selected transport and, if the transport is on-line (ON LINE indicator illuminated), DRIVE ON-LINE is asserted to the adapter and the adapter asserts SELR (select remote) back to the controller. If the selected transport is ready (i.e., tape is loaded and is not rewinding or advancing to the load point (BOT marker)), the transport also asserts XPRT RDY (transport ready) to the adapter, causing the adapter to assert TUR (tape unit ready) to the controller. With these conditions satisfied, the controller can now raise the command lines required to perform a given operation and asserts SET to initiate that operation.

11.2.1 Write Operation

To perform a write operation, the controller raises WRE (write enable) and FWD (forward) and asserts SET. The adapter logic responds by asserting FWD MOT (forward motion) and WRE LTCH (write enable latch) to the transport control logic, begins to count off a delay, and clears TUR to the controller. The transport logic responds by asserting WRITE READY and SEL DRIVE to the data section and a ramp-up, forward motion voltage to the servo system. Hence the servo system starts moving the tape forward at normal speed and the data section is enabled. The adapter then completes the delay count. (The delay allows the tape to accelerate to normal operating speed and ensures that the heads have moved well past the BOT marker when starting from a BOT position.) Assuming the controller will have placed a character on the write data lines and asserted WDR (write data ready) to the adapter when the delay expires, the adapter immediately generates a parity bit and a write strobe (REC) to load the data character with parity into the data section. The data section immediately records the character, reads it back, and places it on the read data lines to the adapter along with a read strobe. The adapter then checks the read character for parity errors and outputs the character back to the controller, along with a read strobe (RDS). The adapter then asserts a write strobe (WRS) to the controller to request the next character. The controller then places the next character on the write data lines. This process is repeated over and over until the last character is recorded and the controller clears WDR.

When WDR clears, the adapter generates two more write strobes to properly terminate the record. REC is asserted along with the CRC character to the data section for recording. Then the LRC PLS is generated to the data section to generate the LRC character, which is then recorded. The adapter reads the two check characters, outputs them to the controller, along with the CRC and LRC strobes (CRCS and LRCS), and checks for CRC and LRC errors. If a CRC or LRC error is detected, the respective error line is also asserted to the controller.

Next, the adapter terminates the write operation by clearing FWD MOT to the transport control logic, asserting SDWN (settle down) to the controller and counting off deceleration delay. When FWD MOT clears, the transport control logic applies a ramp-down voltage to the servo system and clears the WRITE READY and SEL DRIVE lines to the data section. Hence, the servo system stops the tape and the data section stops writing and reading data.

When the deceleration delay expires, the adapter asserts TUR and clears SDWN to the controller. Thus the TS03 is ready to perform the next operation.

11.2.2 Read Operation

To perform a read operation, the controller raises FWD and asserts SET. The adapter logic responds by asserting FWD MOT to the transport control logic, starting the delay count and clearing TUR. The transport control responds by asserting SEL DRIVE to the data section and a ramp-up voltage to the servo system. The servo system then begins to move the tape forward, and the read portion of the data section is enabled. The adapter completes the delay count and begins to accept read data, along with read strobes from the data section. Each character read is checked for a parity error and output to the controller, along with a read strobe. Upon reading the final two characters (normally a CRC and LRC character) and checking for errors, the adapter clears FWD MOT, asserts SDWN to the controller, and begins to count off a deceleration delay. When FWD MOT clears, the transport control logic applies a ramp-down voltage to the servo system to stop tape motion and clears the SEL DRIVE line to the data section to stop reading. When the deceleration delay expires, the adapter asserts TUR and clears SDWN to the controller.

11.2.3 Rewind Operation

To perform a rewind operation, the controller asserts RWD (rewind) and SET. The adapter logic responds by asserting RWND PLS to the transport control logic. The transport control logic responds by clearing XPRT RDY, asserting RWNDG to the adapter and applying a high-speed reverse, ramp-up voltage to the servo system. The adapter asserts RWS (rewind status) to the controller while the servo system rewinds the tape past the load point. The transport control logic then applies a forward motion ramp-up voltage to the servo system, which moves the tape forward to the load point and stops the tape. The transport control logic then clears RWNDG and asserts LOAD POINT and XPRT RDY to the adapter. The adapter clears RWS and asserts TUR to the controller.

11.3 FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

11.3.1 Adapter Logic

Figure 11-2 is a block diagram of the adapter logic. The diagram separates the adapter logic into six areas and shows adapter data and signal flow.

As stated previously, the adapter logic enables software control of the TS03 DECmagtape Transport. Referring to Figure 11-2, note that the control logic responds to inputs from the controller by generating control signals for the write logic and the read logic as well as control signals for the tape transport. These control signals control the reading and writing of data, tape motion, and interrecord gaps. In addition, the control logic provides clock signals (TIME PLS 1,0) for the adapter logic, monitors transport status lines, and initializes the adapter logic whenever INIT is asserted by the controller.

In response to inputs from the control logic and the controller, the write logic and read logic transfer data to and from the tape transport. The write logic accepts write data from the controller and monitors the controller C WDR (write data ready) line. If the C WDR line is true, the write logic generates parity, write strobes (REC), CRC characters, LRC strobes (LRC PLS), and the file mark character and outputs this information to the tape transport via the transport drivers for recording. The read logic accepts read data from the transport and monitors the RD STRB line. Using RD STRB and the read data, the read logic detects data records and file mark records. In addition, checks are made for parity, CRC, and LRC errors.

11.3.1.1 Control Logic – The control logic can be divided into nine logic sections (Figure 11-3). Each section performs a specific function to perform the eight different operations of which the control logic is capable. Table 11-1 lists those operations and indicates the commands that must be issued by the controller to initiate them.

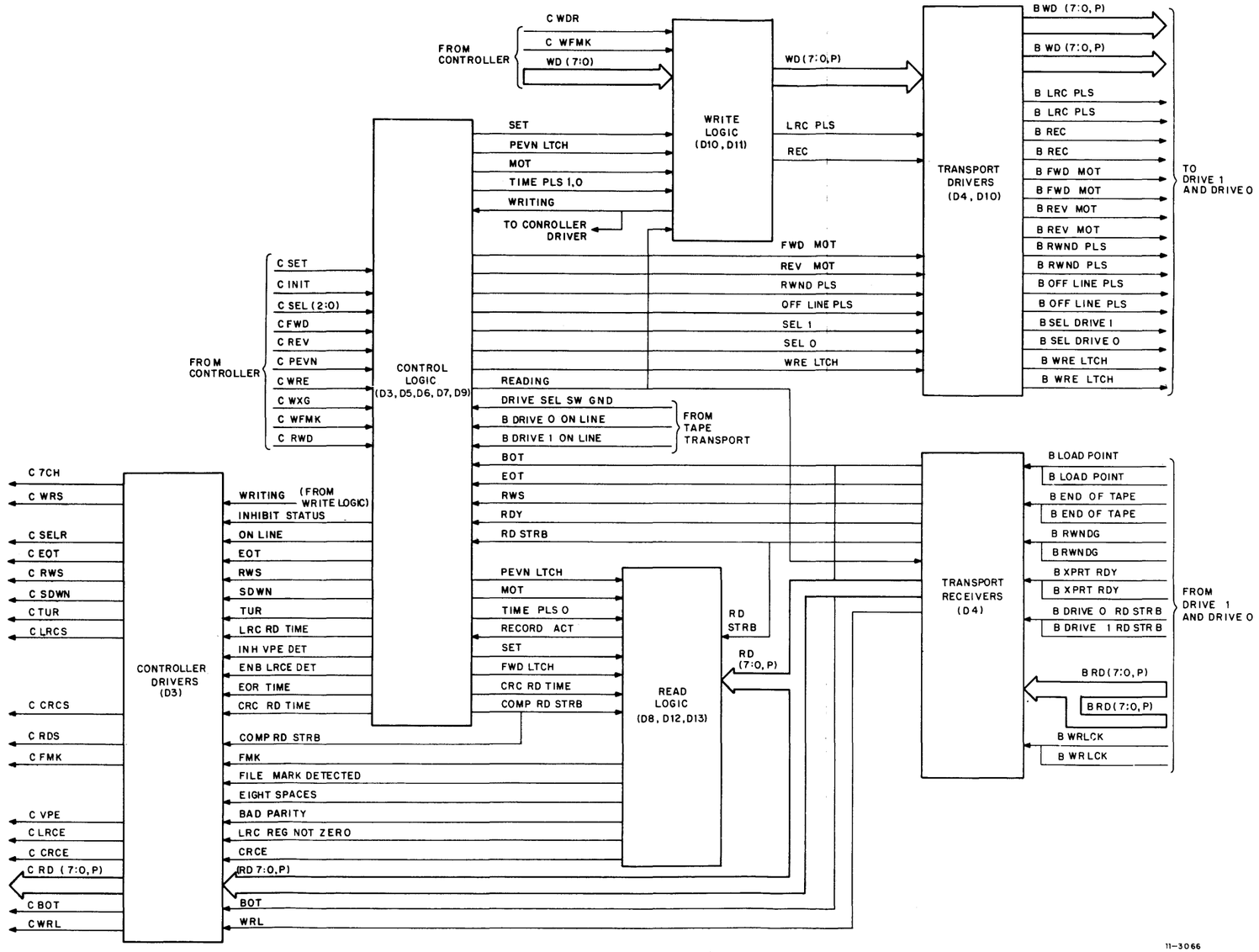


Figure 11-2 Adapter Block Diagram

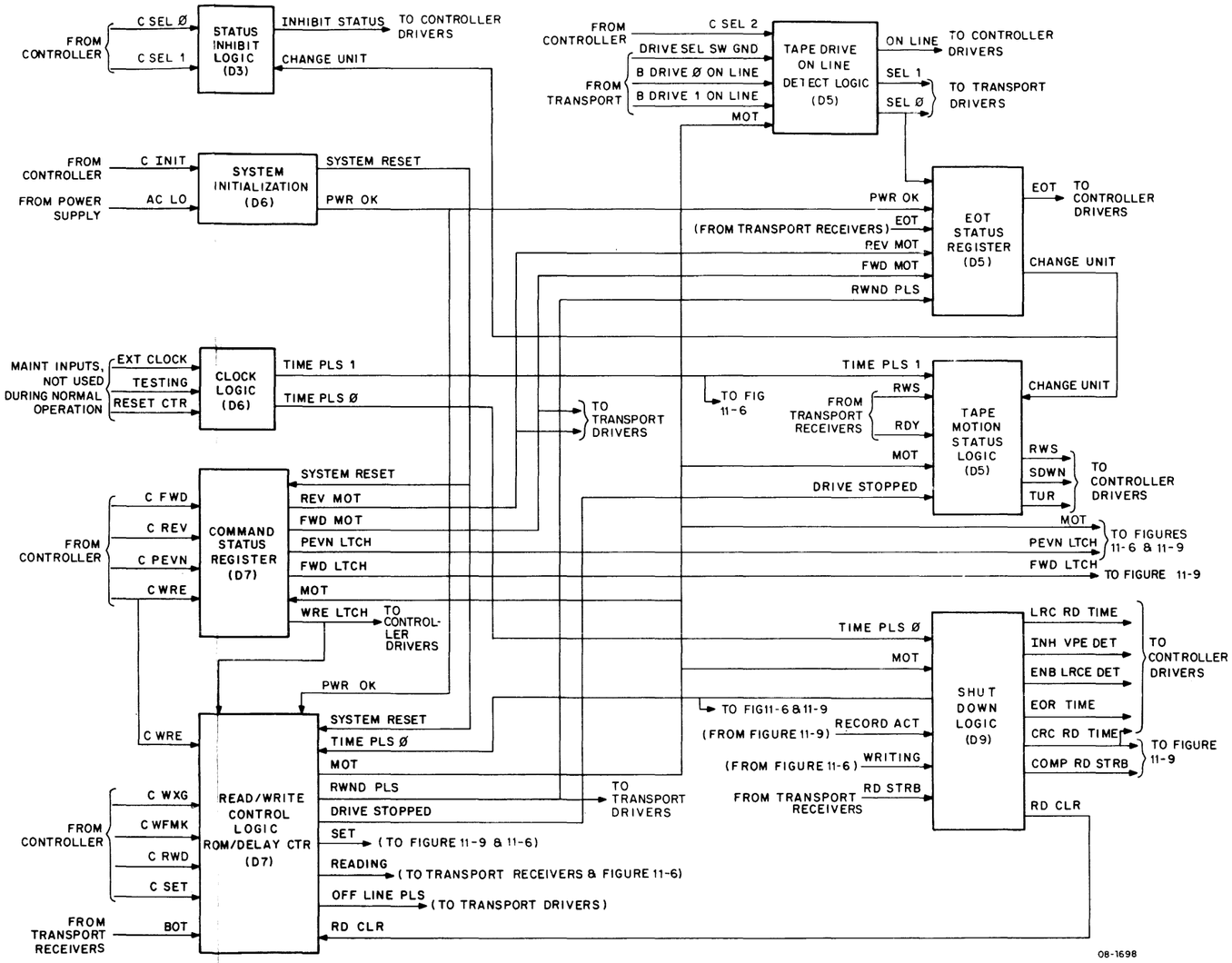


Figure 11-3 Control Logic Functional Block Diagram

Table 11-1
Operations Versus Commands Required

Operations	Controller Commands Required					
	Write Extended Gap (WXG)	Write File Mark (WFMK)	Write Enable (WRE)	Forward (FWD)	Reverse (REV)	Rewind (RWD)
Rewind, Off-Line			X			X
Rewind						X
Write			X	X		
Write-with-extended Interrecord-Gap	X		X	X		
Write File Mark		X	X	X		
Read				X		
Space Forward				X		
Space Reverse					X	

To prepare the control logic to receive commands, the controller asserts C INIT. Asserting C INIT generates SYSTEM RESET, which clears the command status register and resets the motion flip-flop in the read/write control logic.

The controller then issues the commands by asserting the command lines and generating a C SET pulse. The command processing sequence that results is illustrated in Figure 11-4. Note that different operations require that different delays be generated by the delay counter (Table 11-2). These delays are incorporated for the following reasons:

1. To allow time for the tape to accelerate to normal operating speed from a stopped condition.

2. To allow time for the tape to decelerate from normal operating speed to a stopped condition.

3. To allow time for the transport to move the tape BOT marker well past the read/write heads when starting from the BOT position.

4. To enable the writing of industry-compatible extended interrecord gaps and file marks.

Note that the rewind operation does not require a delay.

Due to the similarities of the eight operations performed by the control logic, the following paragraphs will explain first a write operation and then point out the differences between a write operation and the other operations.

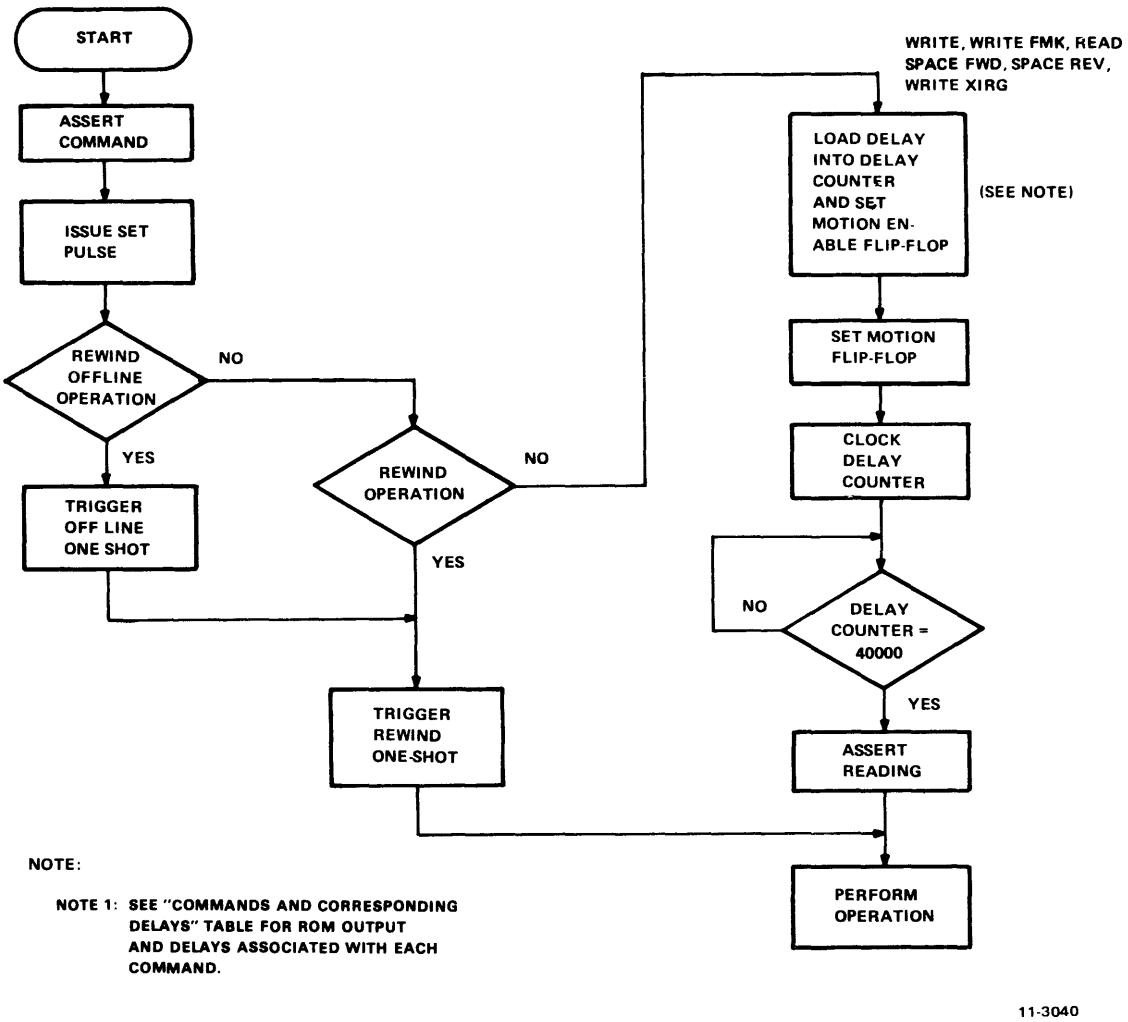


Figure 11-4 Commands Processing Sequence Flow Diagram

Table 11-2
Commands and Corresponding Delays

Commands	ROM Address	2s Complement of Delay	Delay (ms)	Delay (in.)
(WFMK + WXG)·BOT	14_8	20000	819.2	10.05
WRE·FWD·BOT	16_8	25000	563.2	6.85
(WFMK + WXG)·$\overline{\text{BOT}}$	4_8	31400	332.8	3.97
FWD·BOT	12_8	33400	256.0	3.01
WRE·FWD·$\overline{\text{BOT}}$	6_8	37230	35.7	0.256
FWD·$\overline{\text{BOT}}$	2_8	37423	23.7	0.117
DRIVE STOPPED·WRE	24_8, 26_8	37754	2.0	0.025
DRIVE STOPPED·$\overline{\text{WRE}}$	20_8, 22_8	37777	0.1	0.001

Write Operation (Figure 11-5) – To initiate a write operation, the controller must raise the C WRE and C FWD lines and issue the C SET pulse. Assuming the tape is positioned at the BOT marker, the control logic responds to these inputs by presetting the delay counter to 25000 and then asserting MOT, WRE LTCH, and FWD MOT and clearing TUR. When FWD MOT asserts, the transport begins to move the tape forward while the delay counter counts off the delay period. The transport actually moves the tape forward 6.85 in. (17.4 cm) before the delay period expires. This distance ensures that the tape has reached operating speed and is well past the BOT marker and that start-up transients and noise have subsided. When the delay period expires (counter equals 40000), the READING line asserts, enabling the read and write logic. When the controller raises the C WDR (write data ready) line, a write strobe (REC) is generated and the data is actually written on the tape. A write strobe (C WRS) is sent to the controller 50 μs later, requesting the next character. While the write head records the data, the read head reads the data back. Each time the read head detects a character, a RD STRB (read strobe) is sent back to the read logic. Upon receiving three read strobes (minimum record length), the read logic asserts RECORD ACT to the shutdown logic. The recording operation then continues until all the data is recorded and the controller clears the C WDR line. When C WDR is cleared, WRITING (which is controlled by the write logic, Figure 11-6) clears and the shutdown logic is enabled.

When the shutdown logic detects a gap three character times long between successive read strobes, CRC RD TIME is asserted to the read logic and the controller drivers. If the record was recorded correctly, the next two characters detected by the read head should be the CRC character and the LRC character in that order. The read strobe resulting from the CRC character clears CRC RD TIME and asserts LRC RD TIME to the controller drivers. The read strobe resulting from the LRC character clears LRC RD TIME and eight character times later the shutdown logic asserts RD CLR. If the CRC and LRC characters are not detected by the read head, the RD STRB will be generated internally by the shutdown logic; however, the shutdown will wait 56 character times instead of the normal 8 before asserting RD CLR. The extra delay is provided to ensure that the read head has passed the end of the record before the tape stops in the event of a bad tape spot or a write circuitry malfunction.

The assertion of RD CLR loads the delay counter for a delay and clears READING. In this case, because it was a write operation, the counter is set for a delay of 2 ms. In the case of read operations, the counter is set for a 0.1 ms delay. A smaller delay is used during a read operation to ensure that any unwanted data that may be written on the tape by the write heads while turning off is erased. When the delay expires, the read/write control logic clears MOT, WRE LTCH, and FWD MOT. When MOT is cleared, the tape motion status logic asserts SDWN (settle down) to the controller drivers to indicate that the transport is in the process of stopping. Clearing WRE LTCH and FWD MOT actually causes the transport to stop the tape. The read/write control logic delay counter then counts off a 32 ms deceleration delay (which allows time for the tape to stop) and asserts DRIVE STOPPED to the tape motion status logic. The tape motion status logic then clears SDWN and asserts TUR (tape unit ready) to the controller drivers, indicating that another operation may be performed.

Read and Space Forward Operations – The differences between a BOT write operation and a BOT read operation or BOT space forward are as follows:

1. The controller asserts C FWD but does not assert C WRE and C WDR.

2. The read/write control logic delay counter is preset to 33400 and the tape is only advanced 3.01 in. (7.65 cm) instead of 6.85 in. (17.4 cm) before the delay expires and READING is asserted.

3. C WRE is not asserted so the transport write logic is disabled.

4. C WDR is not asserted so the adapter write logic is disabled.

5. The delay counter counts off a 0.1 ms delay before clearing MOT and FWD MOT.

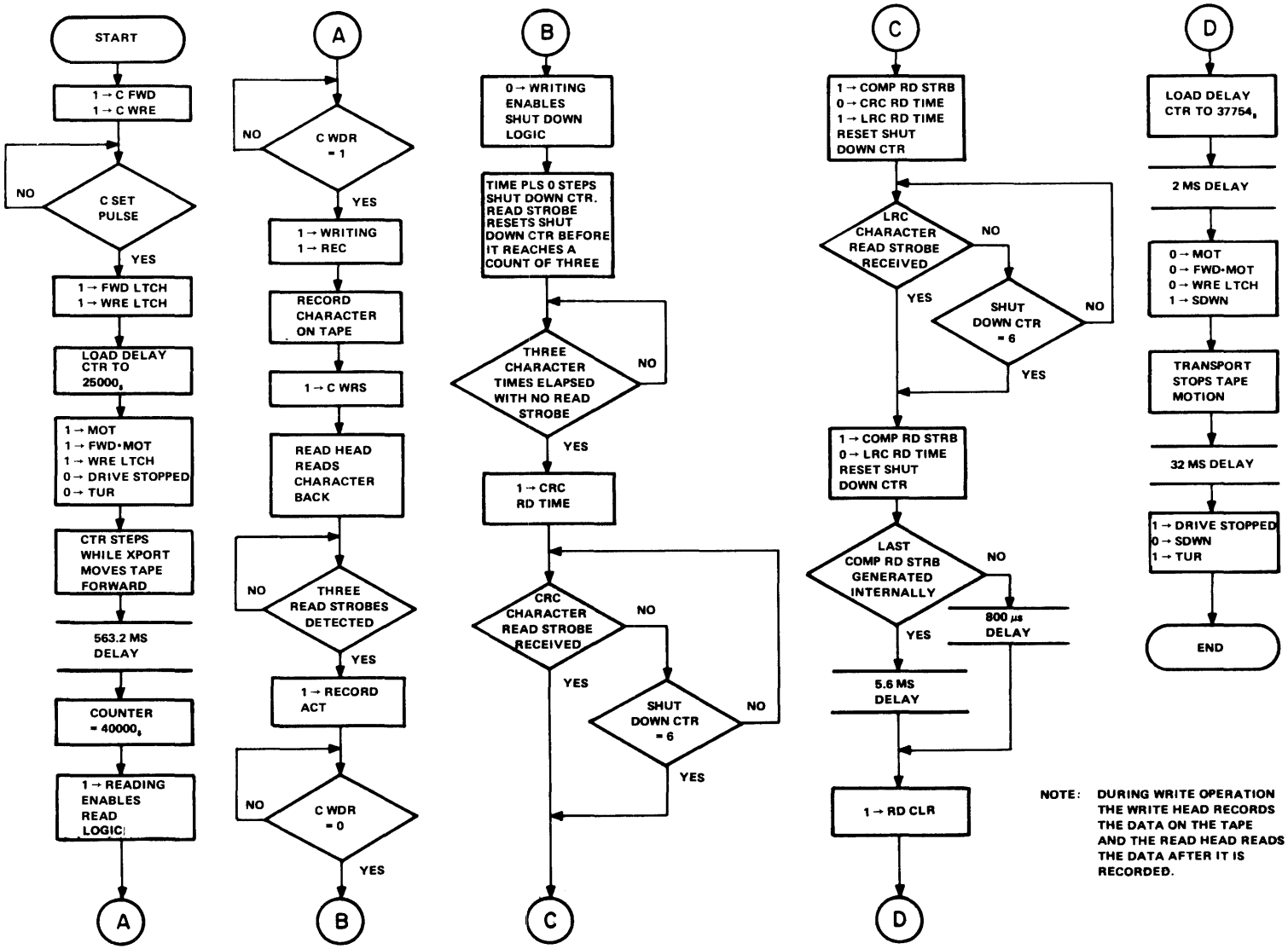


Figure 11-5 Control Logic BOT Write Operation Flow Diagram

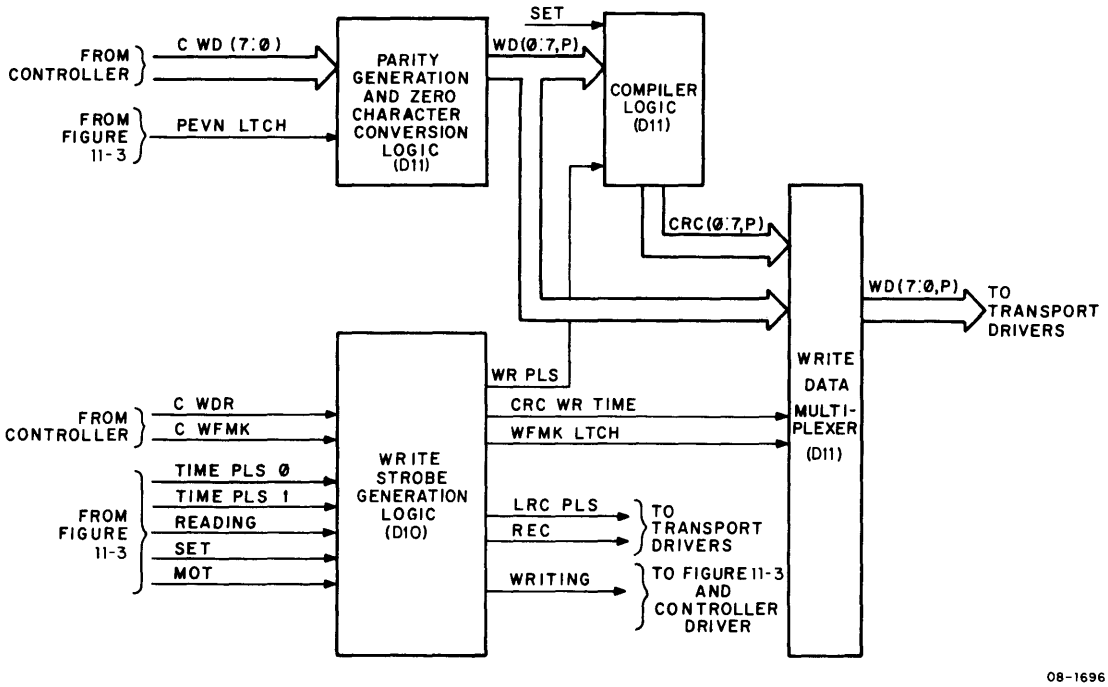


Figure 11-6 Write Logic Functional Block Diagram

Write File Mark Operation – The differences between a BOT write operation and BOT write file mark operation are as follows:

1. In addition to C FWD and C WRE, the controller asserts C WFMK but does not assert C WDR.

2. The read/write control logic delay counter is preset to 20000 and the tape is advanced 10.05 in. (25.5 cm) before the delay expires and READING is asserted.

3. C WFMK enables the adapter write logic to write the file mark character and to generate the LRC PLS which causes the transport data section to write the LRC character.

Write Extended Interrecord Gap Operation – The only difference between a BOT write operation and a BOT write-with-extended-interrecord-gap is that the tape is advanced 10.05 in. (25.5 cm) instead of 6.85 in. (17.4 cm) before the delay expires and READING is asserted.

Space Reverse Operation – The differences between a BOT write operation and a space reverse opperation are as follows:

1. The controller asserts the C REV line only.

2. The read/write control logic delay counter is preset to 37423 and the tape is moved backward only 0.117 in. (2.97 mm) before the delay expires and reading is asserted.

3. C WDR is not asserted so the adapter write logic is disabled.

4. Because there are no CRC and LRC characters at the beginning of a record, two COMP RD STRB pulses must be generated internally by the shutdown logic and the shutdown counter counts off 5.6 ms before asserting RD CLR.

5. The read/write control logic deceleration delay is 0.1 ms.

Rewind Operations – The differences between a BOT write operation and a rewind off-line operation are as follows:

1. The controller asserts C WRE and C RWD but does not assert C FWD and C WDR; thus OFF-LINE PLS and RWND PLS are generated and sent to the tape transport, initiating a high-speed rewind operation and extinguishing the transport ON LINE indicator.

2. The read/write control logic delay counter is preset for no delay and the motion flip-flop is held in a reset condition; therefore, DRIVE STOPPED is asserted immediately to the tape motion status logic.

3. At the tape motion status logic, RWS (rewind status) asserts and RDY clears, causing TUR to clear and RWS to assert to the controller. If the transport is still selected when the rewind is completed, RWS clears and RDY asserts, causing RWS to clear and TUR to assert.

The rewind operation differs from the rewind off-line operation in that C WRE is not asserted by the controller; therefore, OFF-LINE PLS is not generated and the transport ON LINE indicator remains illuminated.

The only control logic functional blocks not fully discussed in the preceding paragraphs are listed below and discussed in the following paragraphs.

Tape Motion Status Logic
Tape Drive On-Line Detect Logic
EOT Status Register Logic
Status Inhibit Logic

Tape Motion Status Logic – This logic determines the tape motion status and generates outputs to the controller drivers to notify the controller. The logic monitors MOT and DRIVE STOPPED from the read/write control logic and the RWS and RDY inputs from the tape transport. If the transport is on-line with tape loaded and is not rewinding or advancing to the load point, the transport asserts RDY as soon as it is selected by the adapter (B SEL DRIVE asserted). When RDY is asserted by the transport, the tape motion status logic asserts TUR to the controller drivers.

The tape motion logic essentially operates in two modes: the rewind mode and the nonrewind mode. If the controller issues a nonrewind command (for example, a write command), the MOT input is asserted and DRIVE STOPPED is cleared, causing the TUR output to clear. When the operation is completed, the MOT input clears and SDWN asserts. DRIVE STOPPED asserts 32 ms later, SDWN clears, and TUR asserts. If the controller issues a rewind command, the transport clears RDY and asserts RWS; MOT and DRIVE STOPPED remain unchanged, i.e., cleared and asserted, respectively. In response, the tape motion status logic clears TUR and asserts RWS. The transport then rewinds the tape past the BOT marker, clears RWS, advances the tape forward to the BOT marker, and asserts RDY and BOT. The tape motion status then clears RWS and asserts TUR.

The CHANGE UNIT input to the tape motion status logic merely serves to reset the logic each time a new drive is selected by the controller.

Tape Drive On-Line Detect Logic – This logic monitors C SEL 2 from the controller, MOT from the read/write control logic, and DRIVE (1:0) ON-LINE and DRIVE SEL SW GND from the master and slave tape transports.

The DRIVE SEL SW GND input determines which transport is drive 0 and which transport is drive 1 as addressed by the controller. The unit select switches located on the master and slave transport front panels control this input. If an even number switch is installed in the master tape transport, it is addressed as drive 0. If an odd switch is installed in the master transport and an even switch in the slave, the master is addressed as drive 1. If no switch is installed in the slave transport, the master is addressed as drive 0. If the master is the only transport in the system, it is addressed as drive 0.

In accordance with the controller input, the tape drive on-line detect logic selects either the master or slave tape transports by asserting SEL 1 or SEL 0 provided the motion flip-flop is reset. If the transport selected is on-line (ON LINE indicator illuminated) the ON-LINE output is asserted to the controller drivers and C SELR is asserted, notifying the controller that the designated transport is on-line and has been selected. If, for example, the master transport is drive 0, the controller must clear C SEL 2 to select the master transport. Note that the tape drive on-line logic will not select a new transport while the motion flip-flop is set.

EOT Status Register Logic – The EOT status register logic monitors the EOT input from the tape transport and the SEL 0 line from the tape drive on-line detect logic and stores the EOT status of each transport in a register. If drive 0 is selected and EOT asserts while FWD LTCH is asserted, EOT is asserted to the controller drivers. If drive 1 is then selected, the EOT status of drive 0 is stored and EOT is cleared. The REV MOT and RWND PLS inputs reset the portion of the EOT status register relating to the drive currently in use. The PWR OK input clears the entire register.

Status Inhibit Logic – This logic inhibits status outputs to the controller when the controller selects a drive other than 0 or 1 and whenever a new drive is selected. If the controller asserts C SEL 0 or C SEL 1, INHIBIT STATUS asserts to the controller drivers and inhibits all status outputs until both inputs are cleared. Whenever the controller clears or asserts C SEL 2, the EOT status register asserts CHANGE UNIT (250 ns pulse), which also causes the status inhibit logic to assert INHIBIT STATUS but for only 250 ns. This prevents the transfer of erroneous status during the drive select operation. Thus, status outputs to the controller are inhibited as long as an illegal drive unit is selected and each time the controller selects drive 0 or drive 1.

11.3.1.2 Write Logic – The write logic generates the strobes necessary to write data, the CRC character, and the file mark character (Figure 11-6). In addition, the write logic generates parity and the CRC and file mark characters and converts all zero characters to 20_8 when even parity (PEVN LTCH asserted) is selected.

The write strobe generation logic is enabled by READING and either C WDR or C WFMK. If READING and C WDR assert, a normal write operation is performed. If READING and C WFMK assert, a write file mark operation is performed. See Figures 11-7 and 11-8 for write operation and write file mark operation flow and timing diagrams.

11.3.1.3 Read Logic – The read logic (Figure 11-9) monitors the read data and RD STRB inputs to determine whether a data record or a file mark record is being read and also checks for parity, CRC, or LRC errors.

The record and file mark detection logic decodes the characters read and generates outputs accordingly. The clearing of MOT at the end of the previous operation and the assertion of SET at the beginning of the current operation serve to initialize the logic and assert FMK.

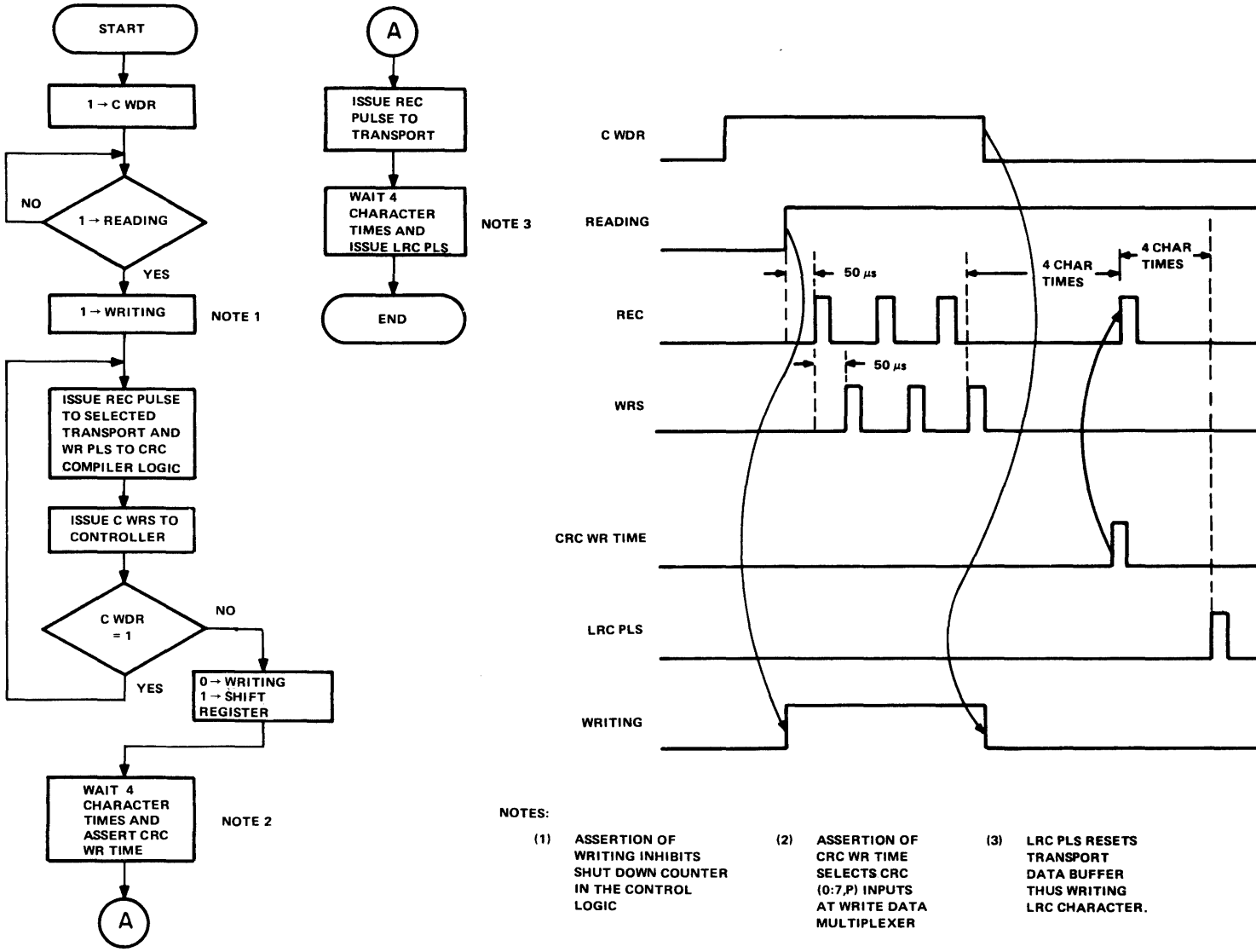


Figure 11-7 Write Operation Flow and Timing Diagram

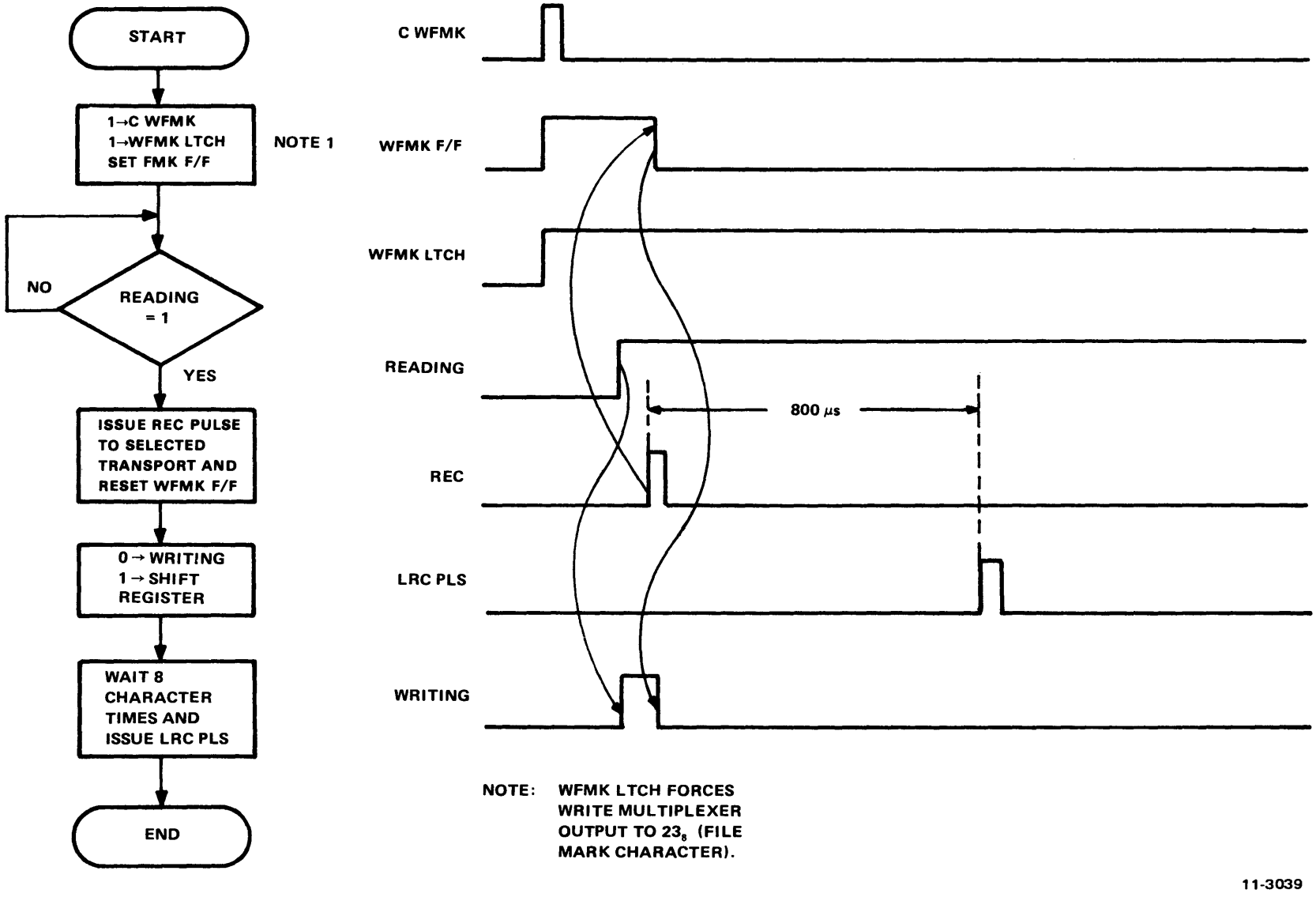


Figure 11-8 Write File Mark Operation Flow and Timing Diagram

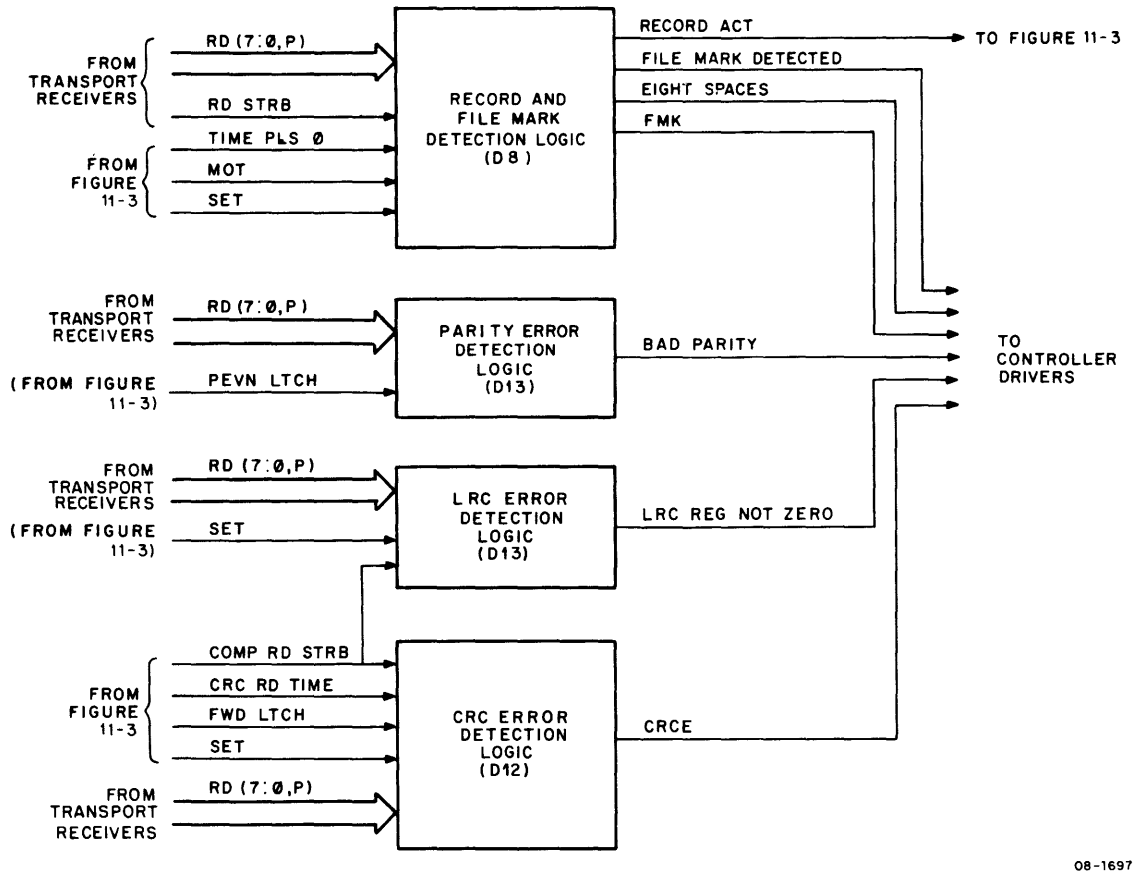


Figure 11-9 Read Logic Functional Block Diagram

The logic decodes characters read as well as the format in which they are recorded. If a file mark record is detected (a file mark character followed by seven blank character frames and an LRC character), all four outputs are asserted, indicating that a record has been detected and that record was a file mark. The three outputs to the controller drivers serve to notify the controller that a file mark record has been detected. The RECORD ACT output enables the shutdown counter in the control logic. If a data record is detected (three or more data characters followed by a CRC and an LRC), FMK is cleared, RECORD ACT is asserted, and FILE MARK DETECTED and EIGHT SPACES remain cleared.

The parity error detection logic uses the simple generate-and-compare technique to check for parity errors. The logic uses the character read to generate the parity bit as selected by the PEVN LTCH input, then compares the parity bit generated to the parity bit read. If they do not match, BAD PARITY is asserted to the controller drivers.

The LRC error detection logic uses a flip-flop register and a compare network to check the number of 1 bits recorded on each channel of a record, including the CRC and LRC characters. If the number of ones recorded is odd, LRC REG NOT ZERO asserts to the controller drivers, causing LRCE to be asserted to the controller. Note that LRC REG NOT ZERO may assert several times during a particular record; however, the controller driver is only enabled during LRC read time while the tape is moving forward. The CRC error detection logic uses the data characters in each record to compile the CRC character; it then compares the character compiled to the CRC character recorded. If they do not compare, CRCE is asserted to the controller drivers. Note that the CRCE output from the CRC error detection logic is only enabled when CRC RD TIME and FWD LTCH are asserted. At the controller drivers, the C CRCE output is disabled whenever a file mark record is detected.

11.3.2 Transport Control Logic

The control logic section of the tape transport generates the appropriate internal tape motion commands in response to input commands from the adapter, the front panel and the test panel. The control logic receives these commands and generates transport motion if all internal interlocks are satisfied. In addition, the control logic returns the transport status outputs to the adapter and illuminates the respective indicators on the front panel and the test panel. Table 11-3 lists the signals interfacing between the adapter and the transport.

Table 11-3
Adapter/Transport Interface Signal Names

B FWD MOT
B REV MOT
B OFF-LINE PLS
B RWND PLS
B WRE LTCH
B SEL DRIVE (1:0)
B DRIVE (0:1) ON LINE
B WD (0:7, P)
B XPRT RDY
B RD (0:7, P)
B WRLCK
B RWNDG
B LOAD POINT
B END OF TAPE
REC
LRC PLS
RD STRB
DRIVE SEL SW GND

11.3.2.1 Functional Operation – Five plug-in circuit cards constitute the control section logic (Figure 11-10): Control Terminator Type 3841 (not shown), Interface Control Type 3842, Pushbutton Control Type 3843, Ramp Generator Type 3645, and Sensor Amplifier/Driver Type 3844. The modules are housed in the card cage assembly and plug into the master board. Figure 11-10 is a simplified block diagram of the control logic, showing the signal flow between the control modules. The input signals from the adapter are supplied, after being terminated on the control terminator module, to the control interface module, where these signals are acknowledged if certain interlocks are satisfied. The motion commands are then supplied to the pushbutton control module. This card also includes the interlocks for the front panel pushbuttons and for the test panel pushbuttons. If the interlocks are satisfied, the pushbutton control module encodes all tape motion commands onto three command lines: RUN NORMAL, RUN FAST, and RUN REVERSE. The three command lines are then supplied to the ramp generator module, which produces accurate analog voltage output. The voltage output of the ramp generator is then supplied to the capstan servo amplifier module in the servo system. The voltage output of the ramp generator in conjunction with the feedback from the capstan tachometer is used to energize the capstan motor and to advance the tape in the desired direction at the proper speed. The ramp generator provides linear ramp-ups to speed and linear ramp-downs to standstill in order to minimize the stress on the tape and maintain accurate speeds.

The sensor amplifier driver module receives the inputs from the file protect switch, the load point sensor, end-of-tape sensor, and broken tape sensor. These signals are amplified and supplied to the other modules in the control section where they provide the inputs to the interlocks. The sensor amplifier driver module also contains the drivers for the front panel indicators, the driver for the file protect solenoid, and the write and erase head drivers.

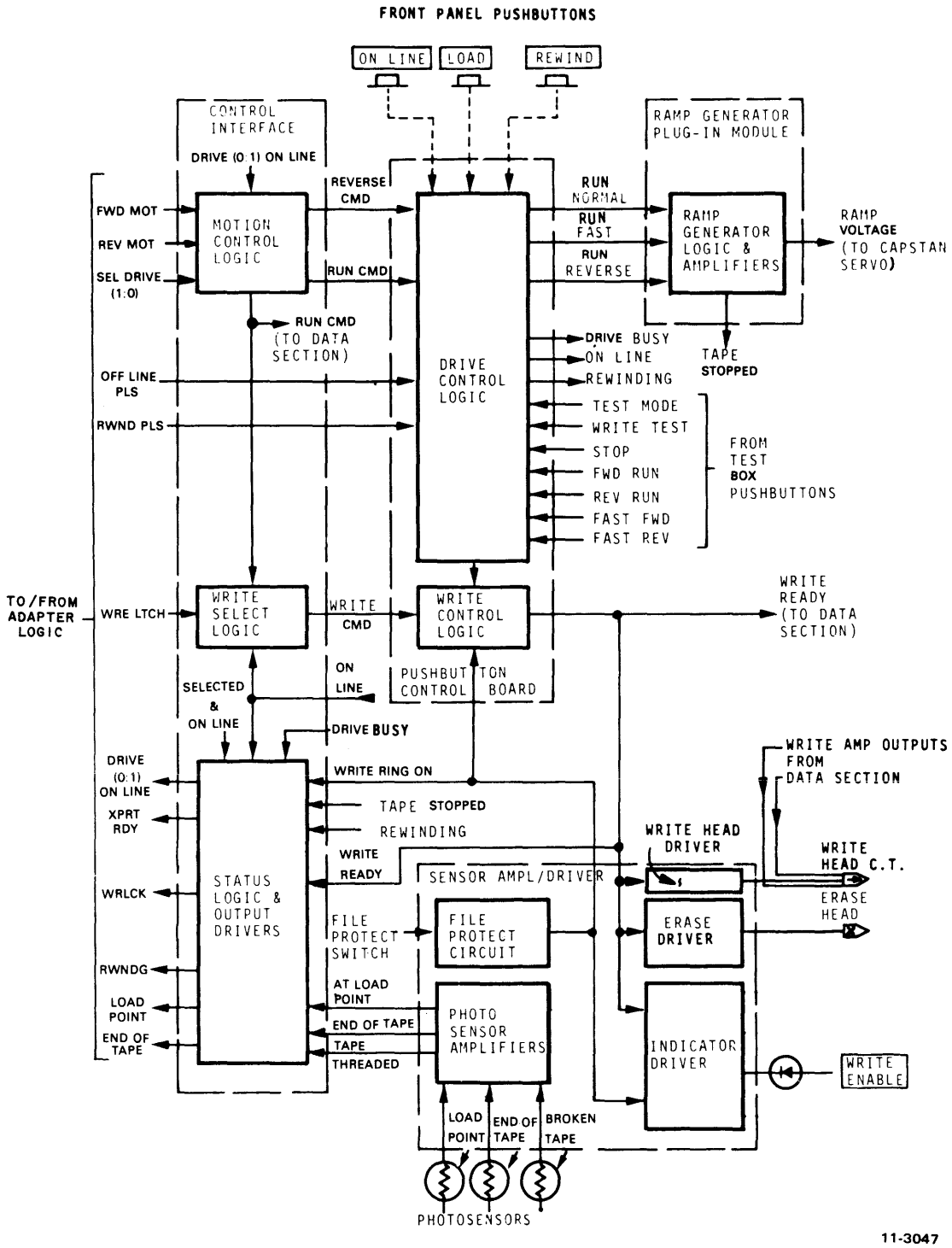


Figure 11-10 Control Logic Block Diagram

11.3.2.2 Transport Control Logic Operation During a Write Sequence – A write operation will be used as an example to demonstrate the interaction of the different components of the control logic. The whole operation is described, showing the flow of commands and the required control interlocks.

The front panel is used to prepare the transport for operation. After the power is turned on and the tape is properly threaded, the front panel LOAD pushbutton is pressed. This sets the load flip-flop on the pushbutton control modules, generating RUN NORMAL true to the ramp generator card. The ramp generator outputs a linear ramp voltage to the capstan servo amplifier card, initiating forward tape motion at normal running speed. The ramp generator also supplies TAPE STOPPED to the interface control card where it is converted to TAPE RUNNING STATUS and then sent to the adapter logic. When the load point reflector marker is detected by the respective photocell, the signal is amplified by the sensor amplifier/driver card and is supplied as AT LOAD POINT to the pushbutton control module. AT LOAD POINT true sets the ON TAPE flip-flop to the true condition, terminating the synchronous forward motion by setting RUN CMD false. The tape is stopped at the load point and is properly loaded. Pressing the front panel ON LINE pushbutton now places the transport on-line, preparing the transport to respond to adapter commands once it is selected by the adapter. When the transport is selected (input line select going true), the transport can accept commands from the adapter and return the transport status outputs back to the adapter. At this time, the transport status lines would be in the states shown in Table 11-4. In addition to the status lines, the front panel ON LINE and UNIT SELECT indicators are illuminated, as is the WRITE ENABLE indicator if the supply reel contains a write enable ring.

If the write operation is to be initiated, the adapter logic now supplies WRE LTCH (set write status) level true and then a FWD MOT (forward command). The WRE LTCH level is sampled on the leading edge of FWD MOT. If the level is true, a flip-flop on the interface control module is set, which generates WRITE CMD true. WRITE CMD is supplied to the pushbutton control module where it generates WRITE READY true provided WRITE RING ON (file protect) is false (supplied from the sensor amplifier/driver module), DRIVE BUSY is false (this signal is generated on the pushbutton control and is true whenever the transport is searching for load point and is rewinding), and a forward motion command is given. These interlocks ensure that the transport writes data on tape only when the tape is properly loaded, the reel has a write enable ring, and the tape is moving forward at normal running speed. WRITE READY true is supplied to the sensor amplifier/driver module where it turns on write and erase head current drivers. WRITE READY and SELECTED & ON LINE (combining ON LINE true and SEL DRIVE (1:0) true) are also supplied to the data electronics card cage where they enable the write and read amplifier stages.

If WRITE READY does go true, the adapter logic supplies the properly formatted data to be written on tape. The write operation can be interrupted in case of broken tape; when the TAPE THREADED (broken tape) signal is supplied from the sensor amplifier/driver module, all servos are disabled immediately. Note that an END OF TAPE indication does not terminate a write operation, but leaves it up to the adapter to do so. When the write operation is terminated by the adapter, the tape is rewound to the load point when the adapter issues RWND PLS. Note that the tape cannot be rewound past the load point by a command from the adapter. In order to rewind the tape off the takeup reel, the transport must be taken off-line, either through an adapter command or by pressing the front panel ON LINE pushbutton again. Once the transport is off-line, the front panel REWIND pushbutton can be activated to rewind the tape completely off the takeup reel.

11.3.2.3 Test Box – The test box provides a means of exercising, testing, and adjusting the tape transport while it is off-line, eliminating the need for a separate test fixture or for the use of valuable computer time. The test box can initiate forward and reverse tape motions at either normal or high tape speeds. It can also initiate a write test, generating a crystal-controlled all-1s test pattern on tape. The test box also provides indicators for load point, end-of-tape, and data. A toggle switch on top of the test box can select a start/stop operation of the capstan servo system for checking the ramp generator.

Table 11-4
Transport Status

Status Line	State	Point of Origin
DRIVE (0:1) ON-LINE	True	Supplied from the on-line flip-flop on the pushbutton control module, routed through the interface control module.
XPRT RDY	True	This signal, generated on the interface control module, combines DRIVE BUSY false (meaning the transport is loaded and not rewinding or searching for load point) and SELECTED & ON LINE true (meaning the transport is on-line and SEL DRIVE (1:0) is true).
TAPE RUNNING STATUS	False	This signal goes true on the ramp generator when tape motion is initiated. It is not used in the TM8-M System.
RWNDG	False	At this time, the rewind flip-flop on the pushbutton control module is in the cleared state.
WRLCK		This signal is true if the reel of tape mounted on the supply hub does not contain a write enable ring. It is false if the reel does contain the ring and is available for writing. The signal originates on the sensor amplifier/driver module.
LOAD POINT	True	Since the tape is at load point, the sensor amplifier/driver supplies this signal true. When OFF LD PT is true, the transport does not acknowledge a REWIND CMD or REVERSE CMD from the interface, but must be taken off-line and rewound by using the front panel pushbutton.
WRITE ENB		This signal is equivalent to the inverse of the WRLCK signal and is true whenever the other is false, e.g., whenever the supply reel contains a write enable ring. The signal originates on the interface control module. It is not used in the TM8-M System.
END OF TAPE	False	This signal goes true only when the end-of-tape reflective marker is detected by the respective photosensor. The signal is supplied to the sensor amplifier/driver module.

An additional indicator monitors excessive skew, and is used in the aligning of the read/write head when using an 800 character/in. skew master tape. When the head is properly aligned and the data is written on tape properly, the SKEW indicator is extinguished. The toggle switch on top of the test box can select instantaneous skew or average skew for the head alignments.

The controls and interlocks for the test box are located on the pushbutton control card. The skew detect network is located on the delay timing module in the read logic section of the transport. The test box becomes operational only when the transport is off-line, with the test box STOP pushbutton pressed. If these conditions are satisfied, the test box pushbuttons are enabled when the TEST MODE pushbutton is pressed.

11.3.3 Servo System

The servo system includes two subsystems: the capstan servo subsystem, which drives the tape at accurately controlled speed, and the reel servo system, which maintains constant tape tension.

11.3.3.1 Reel Servos – Two identical reel servos are employed for the supply and the takeup reels. A simplified block diagram is shown in Figure 11-11. Each reel servo includes a spring-loaded buffer arm, a magnetic position sensor coupled to the buffer arm shaft, a servo amplifier (located on the Servo Preamplifier Type 4306 module), power transistors (located on the chassis heat sink), and a high power dc motor.

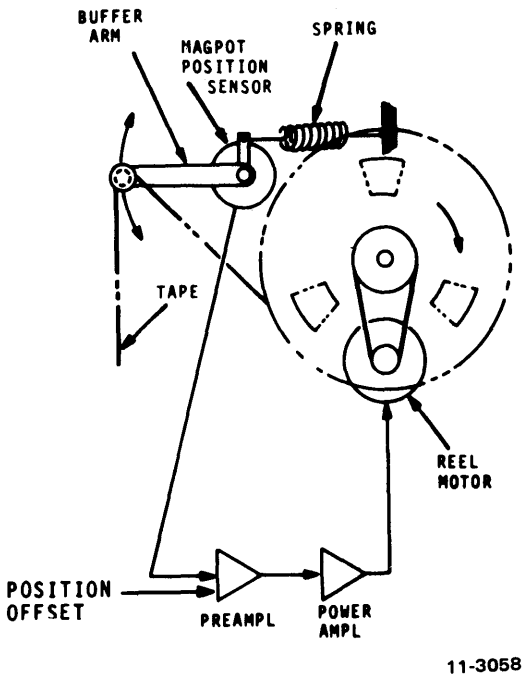


Figure 11-11 Reel Servo System

The tape tension is maintained by the interaction of the spring-loaded buffer arms, the capstan, and the respective reel motors. The magnetic position sensors, called magpots, produce a corrective voltage whenever the buffer arms swing away from the center of their arcs. The magpots are rotary differential transformers with oscillator and phase detector circuitry. The output of the magpot circuitry provides a bipolar dc voltage which has a linear relationship to the tension arm position and a null at the center position. The magpot output is summed with a signal from the capstan tachometer in the higher speed versions of the machine. The effect of the tachometer component is to speed up the response of the reel servos.

As shown in Figure 11-11, the corrective voltage approaches 0 V in the rest position where the torque of the motor is balanced against the buffer arm spring tension near the center of the tension arm swing. When capstan motion pulls the tape, the buffer arm moves, causing a change in the magpot output. This is amplified in the servo preamplifier whose signal drives power transistors that control the dc motor current to provide a change in torque until the torque matches the buffer arm spring tension at the null position again. Since the system is bipolar, seeking a null which is controlled by a magnetic core position, the adjustments are mechanical and will not drift with temperature or component degradation.

11.3.3.2 Capstan Servo – The single capstan drive motor is part of a high performance velocity servo system. In addition to the motor, the capstan servo system includes a dc tachometer, coupled to the capstan motor shaft, and the capstan amplifier, located on the servo preamplifier module. The linear analog ramp voltage produced by the ramp generator card (in the control logic section) is supplied to the servo preamplifier module where it is compared with the feedback supplied from the capstan tachometer. Any resulting difference is amplified and is supplied to the capstan power transistors, located on the chassis heat sink. The output of the power transistors energizes the capstan motor, advancing tape at accurately controlled speeds.

11.3.4 Data Section

The data section includes read and write amplifiers and interface cards providing output drivers and timing controls. Block diagrams are shown in Figures 11-12, 11-13 and 11-15.

The data section consists of eight circuit cards, seven of which plug into the master board. These are a delay timing module, a read amplifier/clipping control card, a pair of quad read amplifier modules, a four-channel write amplifier card, a five-channel write amplifier card, and a data terminator card. A read preamplifier board is mounted on the TS03 main chassis.

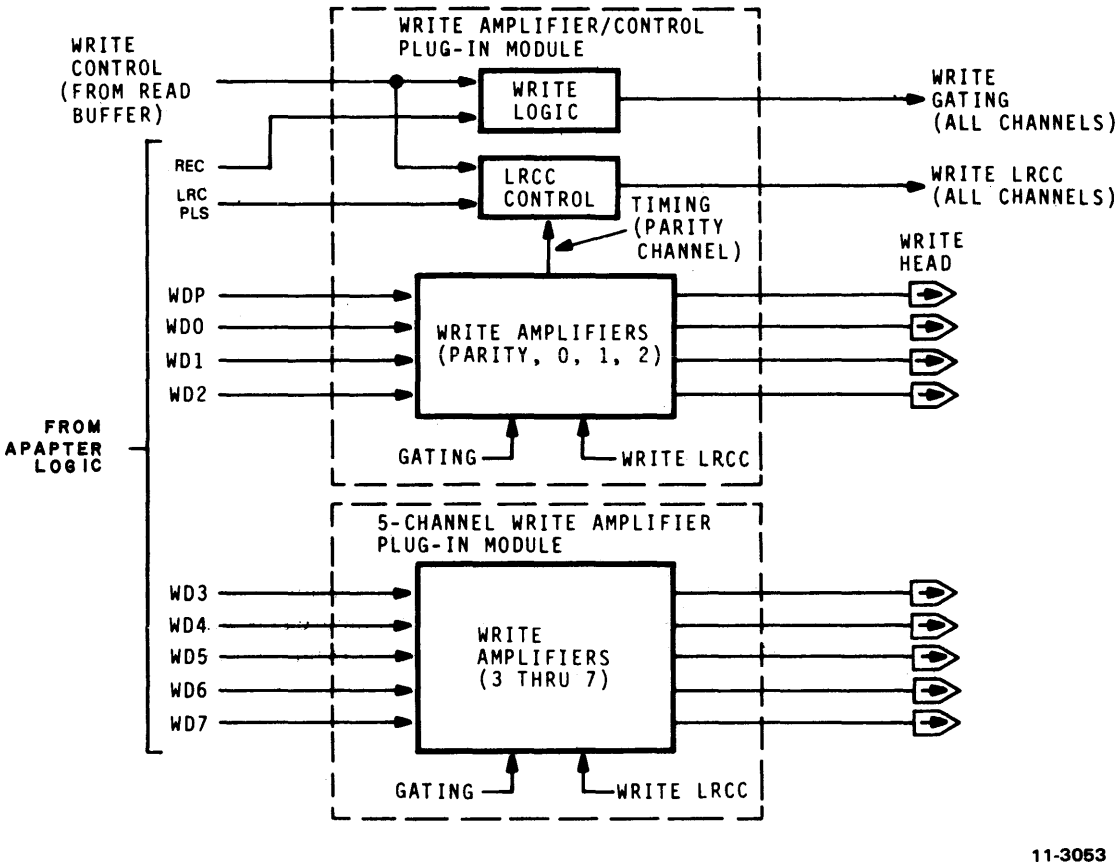


Figure 11-12 Write Data Section

11.3.4.1 Write Electronics – A write amplifier channel is provided for each tape channel. Four such channels and the circuitry common to all write amplifiers are contained on Write Amplifier Type 3848, and the five remaining write amplifier stages are located on Write Amplifier Type 3849. These cards plug into the master board, from which the necessary head connections are made.

Each write amplifier channel consists of an input buffer, a digitally adjustable deskewing circuit, a clocked flip-flop, and a pair of head drivers, as shown in Figure 11-13. Digital write deskewing and its advantages are explained in the following paragraphs.

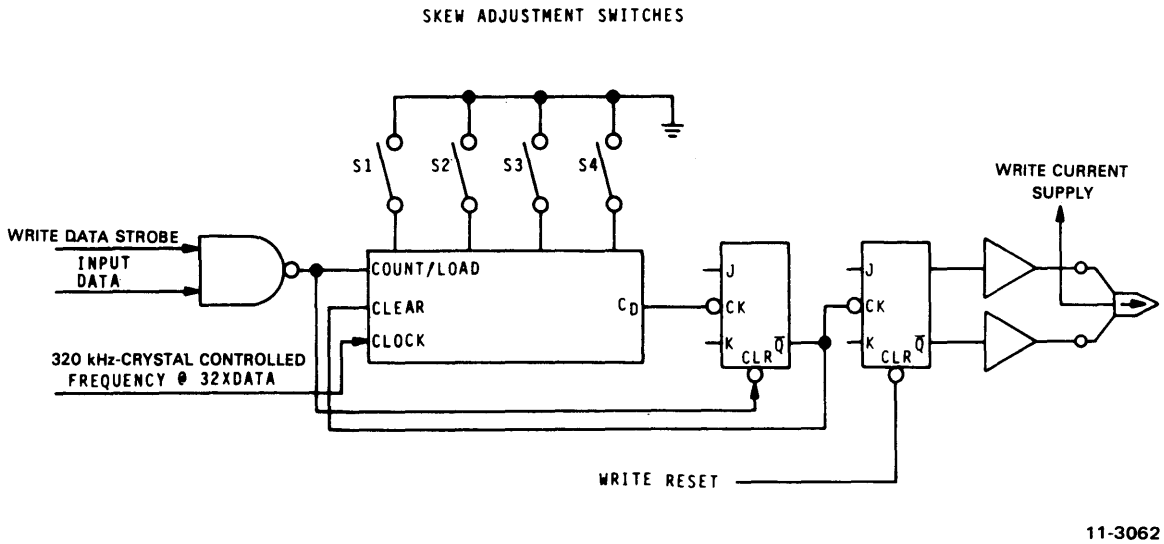


Figure 11-13 Typical Write Amplifier Channel (0–7), Fixed Channel P Delay

Manufacturing tolerances in the production of magnetic heads cause deviations in the parallelism between the write gap and the read gap of the magnetic heads, as shown in Figure 11-14. While the magnetic heads are manufactured so that this deviation does not exceed 250 microinches, it is important to correct for it; otherwise the skew across the bits of a character may cause errors during the reading of the data on compatible systems.

The skew caused by the physical characteristics of the head should not be confused with azimuth or with the skew caused by the misalignment of the whole magnetic head with respect to the tape path, shown in Figure 11-14. Azimuth can be corrected by aligning the read head to be perpendicular to the tape path using a skew master tape – a tape written by a special machine equipped with a full-width write head set perfectly perpendicular to the tape. The head aligning procedure is made particularly simple by the use of the optional test panel, as described in Part I, Chapter 5 of this manual.

While azimuth can be corrected by manually adjusting the position of the read head, the skew caused by the parallelism tolerance between the write head and read head must be corrected electronically. This is done by delaying the channels with respect to a fixed reference so that all the bits of the character are read simultaneously.

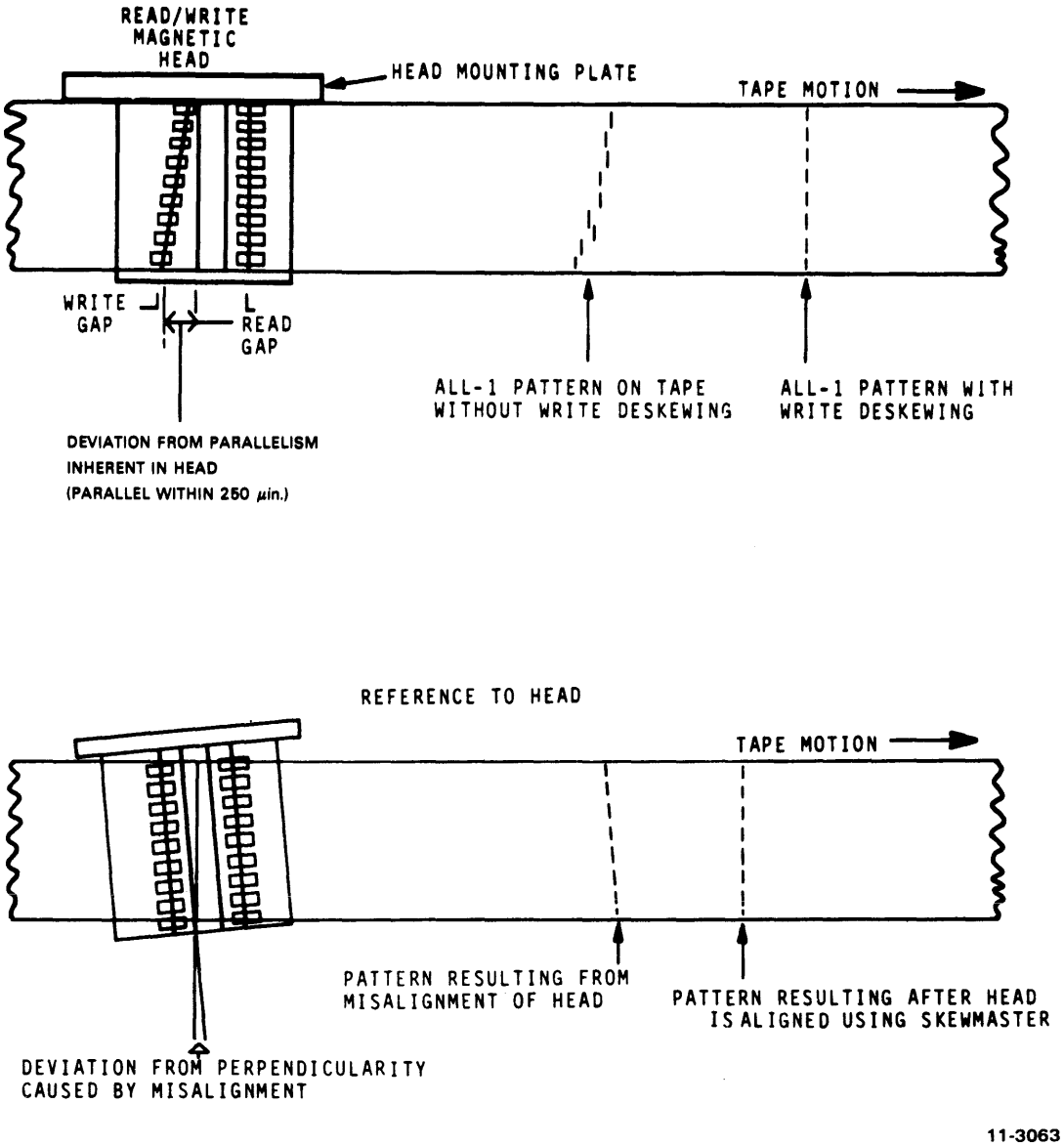


Figure 11-14 Skew Characteristics

Conventional skew correction methods employ adjustable delays supplied by analog circuitry in the read circuits. While these methods compensate for the skew of the character written on tape by the same machine, they do not correct the character itself as it is written on tape; consequently when the tape is read on a different machine, the skew is uncorrected. Also the delays generated by analog circuits are subject to drift and may require periodic readjustment.

In this tape unit, the skew correction problems are overcome by write deskewing circuits, shown in Figure 11-13. The main component of the deskewing circuit is a divide-by-16 counter clocked by a crystal-derived frequency (320 kHz) at 32 times the data rate (generated on the delay timing module). The counter of channel P is preset to the count of eight, supplying a fixed 1/4 character delay. The parallel inputs of the counters of the other eight channels are adjustable using a set of four switches for each counter, varying the skew delay of each channel in 1/32 character increments. Each head is pretested and the switch positions are determined to compensate for any deviation from parallelism between the write and the read gaps, using channel P as a reference. Once the head is installed on a machine and the write amplifier switches are set, the switch positions should not be changed for the life of the magnetic head. These switch positions are displayed on a tape inside the machine. If the magnetic head is replaced, the replacement head is pretested in the factory and is supplied with a new tag showing the switch positions required to compensate for the characteristics of the new head.

The digital write deskewing method ensures that the character written on tape has minimum skew, increasing the compatibility of tapes between different tape transports. Using digital circuitry with a crystal-controlled reference frequency provides for a high degree of precision and stability for all skew adjustments.

The write electronics section also includes the write data strobe buffer which clocks the write amplifier flip-flops, and a write amplifier reset circuit to clear all write amplifier flip-flops. The write amplifier reset is used to write the LRC character. During a write test mode, initiated by the test box with the recorder off-line, the write electronics generates an all 1s test pattern on tape derived from a crystal-controlled reference frequency (10 kHz), supplied from the delay timing module in the read electronics. The test pattern can be used to test the write deskewing, as well as the other functions of the data electronics.

11.3.4.2 Read Electronics – The function of the read electronics is to convert the data recovered from the tape into digitized waveforms, deskew it, and supply it to the adapter logic with its respective read strobe. The read electronics also detect the interrecord gap and excessive skew. The components comprising the read section include the magnetic read head, the Read Preamplifier Type 3631 module, Delay Timing Type 4845 module, Read Amplifier/Clipping Control Type 4179 module, and a pair of Quad Read Amplifier Type 4178 modules. Figure 11-15 is a functional block diagram of the read section, showing the general signal flow between the cards.

The low level analog signals, on the order of tens of millivolts, are supplied from the read head to the read preamplifier module where they are linearly amplified to an output voltage (adjusted by a potentiometer for each read preamplifier stage) of approximately 9 V peak-to-peak in 800 character/in NRZI read operation. The amplified analog signals are then supplied to the nine read amplifier stages, eight of which are located on the quad read amplifier modules while that of channel P is located on the read amplifier/clipping control module. Each read amplifier stage includes a peak detection circuit, a filtering network, an output data register, and a pulse generator.

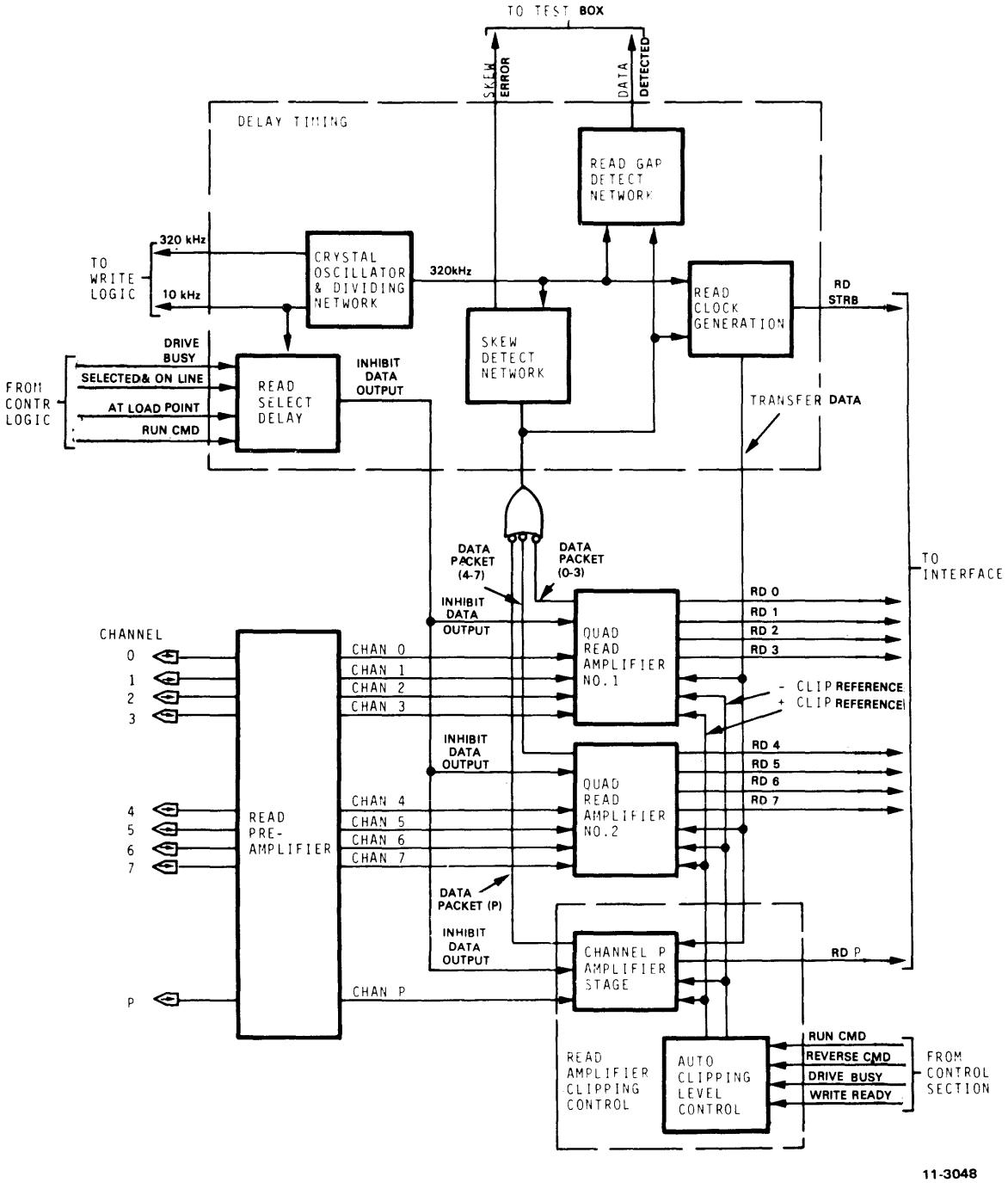


Figure 11-15 Read Data Section

The analog signals from the preamplifier are detected only when they exceed the positive or negative clipping levels provided by the read amplifier/clipping control module. They are then rectified and peak detected, with the resulting digitized waveforms containing negative-going transitions corresponding to the peaks of the input analog signals, e.g., 1 bits in the NRZI code. The digitized waveforms are supplied to a filtering network which eliminates spurious pulses between transitions. The data of each channel is then stored in a register and generates a DATA PACKET to the delay timing module. Following the skew delay, the delay timing card supplies a TRANSFER DATA output to clock the data registers of all nine channels simultaneously, supplying the data character and read clock to the interface.

When an error is detected and the transport is commanded by the adapter logic to reread a block, the read amplifier clipping levels are switched automatically by the read amplifier/clipping control module to maximize the recoverability of marginally recorded data. The clipping levels are kept normal on the first reread; on the second reread they are switched to lower levels in order to recover possible partial dropouts. If the block is still in error and a third reread is commanded, the clipping levels are switched to higher levels to eliminate possible baseline spikes. During read-after-write operations, higher clipping levels are used.

The delay timing module contains circuitry common to all nine channels. It includes a crystal-controlled oscillator and divider network which produce the synchronous clocks used in the skew delay network, the data strobe generation, and the gap detect network, and are also supplied to the Write Amplifier Type 3848 module to generate the write test pattern. The crystal-controlled clocks ensure high precision in the performance of all data synchronized functions.

CHAPTER 12
DETAILED LOGIC DESCRIPTIONS

12.1 INTRODUCTION

This chapter contains circuit descriptions of the individual circuit cards comprising the TS03 DECmagtape Transport. Module layout drawings are provided with each description. (See engineering drawing for module schematics.) The descriptions are arranged by functional group as listed below.

Functional Group	Module Name and Type
Adapter Logic	M8920 Adapter
Overall	TS03S Power Supply
Control Electronics	Control Interface Module (Type 3842) Pushbutton Control Module (Type 3843) Ramp Generator Module (Type 3645) Sensor Amplifier/Driver Module (Type 3844) Connector Board (Type 4013) Control Terminator Module (Type 3841)
Servo System	Servo Preamplifier Module (Type 4306) Magpot Sensor (Type 4218)
Read Electronics	Data Terminator Module (Type 3860) Read Preamplifier Card (Type 3631) Delay Timing Module (Type 3845) Quad Read Amplifier Module (Type 4178) Read Amplifier/Clipping Control Module (Type 4179)
Write Electronics	Four-Channel Write Amplifier Module (Type 3848) Five-Channel Write Amplifier Module (Type 3849)

12.2 NOTES TO TRANSPORT SCHEMATIC DIAGRAMS

The following conventions have been observed in preparing schematics for this manual:

1. Resistor values are given in ohms. If wattage is unspecified, the resistor may be either 1/4 or 1/2 W.

2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens, they are designated as CF.

3. Normally, IC power connections are on pins 14 (+5 V) and 7 (ground) for 14-pin packages, and 16 (+5 V) and 8 (ground) for 16-pin packages. Some ICs (7476, 7492, 7493, for example) have power connections on pin 5 (+5 V) and pin 10 (ground). Operational amplifiers in the 8-pin package have power connections on pin 4 (-Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.

4. Where multiple inputs are tied together only one pin may be designated on the schematic.

5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.

6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.

7. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.

8. Unless otherwise specified, light-emitting diodes are FLV102 or equivalent.

9. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double-sided socket is used. These are the designations on the socket. When a single-sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22-pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.

12.3 TYPE M8920 ADAPTER CIRCUIT DESCRIPTION

The following paragraphs provide detailed circuit descriptions on those portions of the adapter logic which perform unique or complex operations. Each description covers a functional block on the control logic, write logic, and read logic functional block diagrams and is titled accordingly. The circuits described are listed as follows:

Functional Area	Circuit	Engineering Drawing Reference
Control Logic	Clock Logic	D6
Control Logic	Read/Write Control Logic (ROM/Delay Counter)	D7
Control Logic	Shutdown Logic	D9
Write Logic	Write Strobe Generation	D10
Read Logic	Record and Tape Mark Detection Logic	D8

12.3.1 Clock Logic

The clock logic generates two 10 kHz pulse trains which are 180 degrees out of phase. See the timing diagram for logic operation and timing specifications (Figure 12-1).

12.3.2 Read/Write Control Logic (ROM/Delay Counter)

The following paragraphs describe the read/write control logic relative to two different operations: a write operation and a rewind off-line operation (engineering drawing D7).

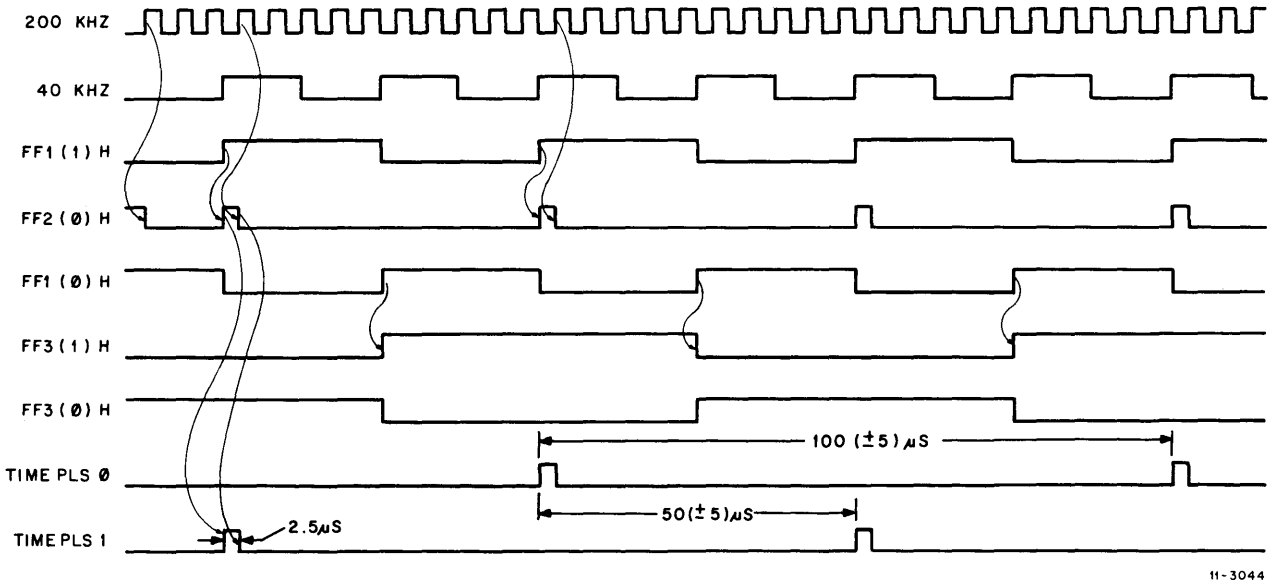


Figure 12-1 Clock Logic Timing

12.3.2.1 Write Operation – To initiate a write operation, C WRE H and C FWD H must be asserted by the controller. When SET L asserts, the following operations occur at the read/write control logic:

1. The ROM is addressed and the proper count is output to the delay counter. The count varies in accordance with the tape position relative to the BOT. If the tape is positioned at the BOT (BOT H asserted), the delay counter is set to 25000_8.

2. The motion enable flip-flop is set.

3. The load delay counter one-shot (E27-5) is triggered and the LD input to the delay counter asserts.

Assuming the tape is positioned at BOT, the assertion of the LD input loads the delay counter to a count of 25000_8 using the output from the ROM and RWND L. Note that zeros are loaded into the first and second most significant bits (R3 and R2) of Part D of the delay counter due to the assertion of SET L. The load delay counter one-shot then resets and sets the motion flip-flop, asserting MOT H. Thus READING H remains cleared. TIME PLS 0 then clocks the delay counter for 563.2 ms, the second most significant bit of Part D of the delay counter sets, and READING H asserts. The read/write control logic remains in this state until RD CLR (1) H is asserted by the shutdown logic.

The assertion of RD CLR (1) H loads the delay counter with a deceleration delay using the ROM output RWND L. In this case, because a write operation is being performed, the delay counter is set to 37754_8. RD CLR (1) H also sets the two most significant bits (R2 and R3) of Part D of the delay counter because SET L is cleared. TIME PLS 0 L then clocks the delay for 2 ms, the most significant bit (R3) is reset, and the motion enable flip-flop (E25-9) is reset. Resetting the motion enable flip-flop asserts E14-3, which resets the motion flip-flop, thereby clearing MOT H and the FWD MOT H output to the tape transport. The transport begins to stop the tape. TIME PLS 0 L then clocks the delay counter for 32 ms (allowing time for the transport to stop the tape), and INHIBIT DELAY COUNT L asserts, inhibiting the clock input to the delay counter and asserting DRIVE STOPPED L. Assertion of DRIVE STOPPED L notifies the tape motion status logic that tape deceleration delay has expired.

12.3.2.2 Rewind Off-Line Operation – To initiate a rewind off-line operation, C RWND H and C WRE H must be asserted by the controller. When C SET H asserts, the following operations occur:

1. The ROM is addressed and a stop count is output to the delay counter.
2. The motion enable flip-flop is set.
3. The off-line one-shot (E33-13) is triggered, asserting OFF-LINE PLS H to the tape transport.
4. The rewind pulse one-shot (E27-13) is triggered, asserting RWND PLS H to the tape transport.
5. The load delay counter one-shot (E27-5) is triggered, asserting LOAD DELAY CTR L.

The assertion of LOAD DELAY CTR L loads the delay counter with a stop count, i.e., the counter is set so that DRIVE STOPPED L asserts. When the load delay counter one-shot resets, the motion flip-flop is held in the reset state by RWND PLS H. Thus MOTION H remains cleared, DRIVE STOPPED L remains asserted, and the tape is rewound to the BOT.

12.3.3 Shutdown Logic (Engineering Drawing D9)

The shutdown logic is enabled when RECORD ACT H asserts and WRITING L clears. With those conditions established, TIME PLS 0 H clocks the shutdown counter. However, the counter is prevented from counting past a count of 2 initially by COMP RD STRB L (composite read strobe), which is generated each time RD STRB H (read strobe) is received. After the last data character is read, there is a gap of three character times before the CRC character is read. During that time, the shutdown counter reaches a count of 3, the CRC flip-flop (E61-5) is set, and CRC RD TIME (1) H asserts. A read strobe is then received due to the CRC character and COMP RD STRB L asserts and clears the shutdown counter again. When COMP RD STRB L returns high, the CRC flip-flop is reset and the LRC flip-flop (E45-5) is set, asserting LRC RD TIME (1) H. The counter then counts to 3 again, but this time LRC RD TIME (1) H holds the CRC flip-flop in the reset state. Another read strobe is then received due to the LRC character, and COMP RD STRB L asserts again, clearing the shutdown counter. When COMP RD STRB L clears, the LRC flip-flop is reset and the EOR flip-flop (E45-9) is set. Note that the read strobe resulting from the LRC character is also ANDed with LRC RD TIME (1) H to load the shutdown counter with a binary count of 56 (0111000). The shutdown counter is then clocked by TIME PLS 0 and, at a binary count of 64, the read clear one-shot is triggered, the counter is disabled, and RD CLEAR (1) H asserts to the read/write control logic.

The EOR one-shot (E28-5) is provided to ensure that the shutdown process is completed when the CRC and LRC characters are not detected at the end of a record. This is always the case when the tape is moving backward, and might occur when the tape is moving forward if there is a bad spot in the tape or the write circuitry malfunctions. Note that when the last data character read strobe is received, the shutdown counter counts to 3 and sets the CRC flip-flop, thus asserting CHK CHAR RD TIME H. If the CRC read strobe is not received, the shutdown counter counts to 5, placing a low on the EOR one-shot. At a count of 6, the EOR one-shot is triggered, asserting INTERNAL STRB (1) H and thereby generating COMP RD STRB H. Thus the counter is cleared, the LCR flip-flop is set, and the CRC flip-flop is reset. The counter then counts up again and if the LRC read strobe is not received, the same operation is repeated. The shutdown counter then starts its final count cycle; however, in this case the counter starts from a count of 8 instead of a binary 56, due to the absence of the LRC read strobe. Therefore the final count cycle is 56 counts long instead of the normal 8. In the event a bad tape spot is encountered or the write circuitry malfunctions, this extended count cycle ensures that the tape moves past the end of the record before stopping.

12.3.4 Write Strobe Generation Logic

The following circuit description will cover the two modes in which the write logic can operate: write data and write tape mark (engineering drawing D10).

12.3.4.1 Write Data Circuit – When the C WDR H and READING H inputs are asserted, the write data mode is enabled and WRITING L and WRITING H assert. WRITING H enables the clock pulse (TIME PLS 1 H) to generate write strobes to the transport (REC H) and is also output to the controller driver where it enables the clock pulse (TIME PLS 0 H) to generate the write strobe (C WRS L), thus notifying the controller that a character has been recorded and requesting the next character. When the last data character has been strobed to the transport, the controller clears the C WDR H input, causing WRITING L to go high, inhibiting the strobe outputs, and setting the writing done flip-flop (E47-6). Setting the writing done flip-flop places a high on the input to the shift register and the next assertion of TIME PLS 0 loads a 1. The shift register output then resets the writing done flip-flop so that no more ones will be loaded into the shift register. TIME PLS 0 then shifts the 1 bit through the shift register and, at bit position 3, CRC WR TIME H asserts, enabling another write strobe (REC H) to the transport to record the CRC character. The 1 bit is then shifted to bit position 7 and LRC PLS H is generated and sent to the transport to record the LRC character. Thus the CRC and LRC characters are recorded at the end of each record.

12.3.4.2 Write File Mark Circuit – To write a file mark, the controller asserts C WFMK H and C WRE H, places a file character on the write data lines, and issues a SET H pulse, thereby setting the file mark flip-flop (E44-5) and file mark latch flip-flop (E44-9). After the acceleration delay expires, READING H asserts, WRITING L asserts, and the clock pulse generates REC H. The same clock pulse that generates REC H also generates WR PLS L, which resets the file mark flip-flop on its trailing edge, thereby clearing WRITING L. Thus only one write strobe is generated to record the file mark character. Clearing WRITING L sets the writing done flip-flop and the shift register is loaded and shifted up. However, when CRC WR TIME H asserts, REC H is inhibited by WFMK LTCH (0) H. Therefore, the CRC character is not written. When the 1 is shifted to bit position 7, LRC PLS H is generated the same as in the normal write data mode. Thus the file mark record consists of only two characters.

12.3.5 Record and File Mark Detection Logic

This logic detects data records and file marks (engineering drawing D8). File marks are detected by decoding the characters read; two octal 23 characters at the beginning of a record followed by at least seven blank character frames constitute a file mark record. Data records are detected by counting read strobes; a minimum of three read strobes constitutes a data record.

The MOT H and SET L inputs preset the record and file mark detection logic before the first character (of a current record) and accompanying read strobe is detected. SET L asserts at the beginning of each operation and sets the file mark flip-flop (E47-9), thereby asserting FMK (1) H. MOT H is cleared at the end of each operation and serves to preset the read strobe counter to a count of 1.

12.3.5.1 File Mark Record Detection – When a file mark character (23_8) is the first character read, FMK CHAR L asserts. The assertion of FMK CHAR L is ANDed with the set condition of the file mark flip-flop, placing a high on the D input. Thus the assertion of RD STRB H leaves the flip-flop unchanged and steps the read strobe counter to a count of 2. Now assuming the octal 23 character detected was in fact the first character of a file mark record, the next and final character detected will be the LRC character which is also an octal 23. Therefore when the next character is read, FMK CHAR L remains asserted, the file mark flip-flop remains set, and the read strobe counter is stepped to a count of 3. At a count of 3, ENB FMK CTR H (enable file mark counter) asserts and enables the file mark counter. The file mark counter is then clocked to a count of 8 by TIME PLS 0 L and EIGHT SPACES H asserts, which inhibits the counter and asserts RECORD ACT H. EIGHT SPACES H is ANDed with FMK (1) H to assert FILE MARK DETECTED L.

Note that if another read strobe is received before the file mark counter reaches a count of 8, ENB FMK CTR H clears and RD STRB CTR = 4 (1) H asserts. Thus the file mark counter is cleared and disabled, the read strobe counter is disabled, and RECORD ACT H is asserted. In this case, the two successive octal 23 characters do not constitute a file mark record because data does not follow a file mark record that closely.

12.3.5.2 Data Record Detection – When a character other than an octal 23 is the first character read, FMK CHAR L remains cleared and a low is applied to the file mark flip-flop. Thus the accompanying read strobe resets the file mark flip-flop and steps the read strobe counter to 2. Now, regardless of what the next character is, the file mark flip-flop remains cleared and the read strobe counter is stepped to 3. As previously stated, a count of 3 enables the file mark counter; however, the file mark detection logic was disabled by resetting the file mark flip-flop. Upon the receipt of the next character, the read strobe counter is stepped to a count of 4, RECORD ACT H asserts, and the read strobe counter is disabled.

12.4 TS03 POWER SUPPLY CIRCUIT DESCRIPTION

The TS03 Power Supply produces the unregulated and regulated voltages required by motors and electronics.

12.4.1 Primary Power

Primary power is switchable to allow either 115 V or 220 V mains. Frequency is not critical and may be from 48 Hz to 500 Hz. These voltages were selected because 220 V mains predominate in Europe. A simple modification allows 230 V operation if required. For 115 V operation, the two 115 V primary windings of T1 are connected in parallel by S2. For 220 V operation, a 105 V tap on primary winding 2 is connected in series with primary 1. Modification for 230 V operation requires removal of the violet wire and installation of a jumper from S2-6 to S2-3.

12.4.2 Secondary Power

Transformer secondary voltages are rectified to produce nominal unregulated voltages of ±24 V (±26 V under light load) and +8 V. A voltage of ±24 V regulated is supplied to motor drive circuits and provides sources from which ±10 V regulated is produced. A voltage of +8 V is the source for a high efficiency +5 V regulator.

12.4.3 +10 Volt Regulator

Pass transistor Q3 is fed from +24 V and its base is driven by monolithic regulator E2. Voltage output is determined by R8 and R9. Q7 and Q8 control power supply tracking when powering down. As +24 V drops due to the discharge of C1, Q8 cuts off at approximately 13 V on the +24 V line. When this happens, Q7 is turned on, shorting out R9 and dropping the regulator reference voltage to zero. The +10 V output is cut off and drops to zero. Since +10 V is the reference for −10 V, −10 V also drops to zero. This action occurs before the +5 V supply has dropped sufficiently to cause indeterminate logic states; turn-off transient motions are prevented.

12.4.4 −10 Volt Regulator

The −10 V supply is regulated by pass transistor Q4 driven by Q6. Its reference is +10 V as determined by R13, R14. In this way, the two regulated voltages are made to track or retain a constant relationship to each other.

12.4.5 +5 Volt Regulator

Integrated Circuit regulator E1 controls +5 V output in conjunction with pass transistor Q1 and driver Q2. Output voltage is set by R4, R5. Q2 assures that sufficient base drive is available for Q1. Integrated circuits E1 and E2 consist of a differential amplifier with built-in zener reference together with facilities for short-circuit protection.

12.4.6 Short-Circuit Protection

Drop-through series resistors (e.g., R10 in the −10 V supply), provide short-circuit protection. If the drop across R10 exceeds approximately 0.6 V, Q5 is turned on, connecting Q4 base to emitter and cutting off Q4. This corresponds to approximately 1.5 A under short-circuit conditions. Similar circuits are provided in IC1 and IC2.

12.5 TYPE 3842 CONTROL INTERFACE MODULE CIRCUIT DESCRIPTION (TD9)

This module contains a set of receivers for the adapter control commands:

FWD MOT
REV MOT
OVERWRITE (Not used)
RWND PLS
SEL DRIVE
WRE LTCH
OFF LINE PLS

It also contains drivers that return the recorder status outputs to the interface:

DRIVE ON LINE
RWNDG
WRLCK
LOAD POINT
WRITE ENB (Not used)
XPRT RDY
END OF TAPE
TAPE RUNNING STATUS (Not used)

Certain controls and delays are also provided to ensure proper tape motion and transport operation.

12.5.1 Tape Motion Controls

The motion control commands from the adapter, FWD MOT and REV MOT, are translated on this card into the internal motion commands of the transport: run normal (RUN CMD) and reverse (REVERSE CMD). These internal motion commands are supplied to the pushbutton control modules, where they are combined with commands supplied from the transport pushbuttons and internal interlocks to generate the commands that initiate actual tape motion on the ramp generator module.

On this module, FWD MOT and REV MOT are supplied to an interlocking network that ensures that the tape comes to a stop before its direction of motion is reversed. The interlocking network includes flip-flop E1-3, edge circuits E2-6 and E2-8, NAND gate E3-6, and interlocking flip-flop E3-10. Whenever flip-flop E1 changes states due to a change in the direction of motion (e.g., from FWD MOT to REV MOT), its output generates a pulse through the edge circuits consisting of inverters E2 and the associated capacitors. The pulse is gated through E3-6 to the set input of interlocking flip-flop E3-10. The flip-flop can be set only if TAPE STOPPED is true, indicating that the tape is still moving. In this case, TAPE STOPPED low at input pin W is inverted by E18-12 and supplies a high input to the clear of E3. The flip-flop can then be set by the pulse on its set input, its 0 output going low. The 0 output of E3 then inhibits run normal gate E15 at pin 2, setting RUN CMD false. After the tape has ramped down to a stop, TAPE STOPPED goes false clearing interlocking flip-flop E3, whose output then enables the run normal gate. RUN CMD then goes true if the following conditions are satisfied: SELECTED & ON LINE is true, indicating that the transport is on-line and selected by the adapter; DRIVE BUSY is false, indicating that the transport is not rewinding or searching for the load point; and a REV MOT command is not given at the load point. (This would activate NAND gate E15-8 and would disable the run normal gate at E15-1.) If the above conditions are satisfied, RUN CMD goes true at output pin V, and is supplied to the pushbutton control module where it initiates tape motion at the normal running speed. The direction of motion is determined by the state of flip-flop E1. If a reverse command (REV MOT) has been given, flip-flop E1 is cleared and enables NAND gate E14-6, generating REVERSE CMD (reverse) true, providing SELECTED & ON LINE is true, DRIVE BUSY is false, and AT LOAD POINT is false. No adapter reverse command is acknowledged by the transport when the load point is detected. If a forward command (FWD MOT) has been given, the E1 flip-flop is set thereby inhibiting E14 and negating REVERSE CMD.

12.5.2 Write Select

During a write operation, the adapter supplies WRE LTCH (write latch) true at pin K; WRE LTCH is inverted by E9-4 and is supplied to the D input of flip-flop E7. The flip-flop is toggled provided that the transport is selected and on-line, after NOR gate E1-11 is activated by a synchronous motion command. This would activate NAND gate E1-8 and trigger one-shot E4-4, generating a 2 μs pulse. On the trailing edge of the pulse, the $\overline{Q}$ output of the one-shot toggles E7-3, causing the Q output of the flip-flop to go high and activating NAND gate E10-11, generating WRITE CMD true at output pin H. The E10-12 input from some unused circuitry stays high to keep E10 enabled.

12.5.3 Rewind Flip-Flop

When a RWND PLS (rewind command) is given by the adapter, it sets the rewind flip-flop E5-3, provided that the transport is selected, on-line, and not at the load point. The 1-output of the flip-flop then goes high, generating RWNDG true to the adapter and REWIND CMD through an edge circuit consisting of inverter E6-6, NAND gate E6-8, and capacitor C5. REWIND CMD is supplied to the pushbutton control module. The flip-flop is cleared when the tape returns to and stops at the load point, or when TAPE THREADED is detected.

12.5.4 End-of-Tape

An end-of-tape indication is set when the EOT marker is encountered in the forward direction and remains set until the marker is passed in the reverse direction.

A true END OF TAPE signal at pin Z if machine status is NOT REWINDING (E5-5,8) and REVERSE CMD (E14-6) causes E11 to be preset by E19-8. An EOT status is then signaled at the interface by E16-3.

Upon passing the EOT marker in the reverse direction, E13-3 is high and the END OF TAPE signal clocks E11 clear on the trailing edge of the END OF TAPE signal, dropping the END OF TAPE signal at the interface. E11 is preset to the clear state by TAPE THREADED at pin X.

12.5.5 Output Status

The status gates on this module are all preconditioned by select and on-line being true; consequently, the transport returns status indications only when it is selected and on-line. The XPRT RDY status is generated when DRIVE BUSY, supplied from the pushbutton control module, is false and the transport is not rewinding. The LOAD POINT output is also preconditioned by the rewinding status being false.

12.6 TYPE 3843 PUSHBUTTON CONTROL MODULE CIRCUIT DESCRIPTION (TD7,8)

The circuitry used to carry out the motion commands issued by the adapter or by the pushbutton panels (both the main control panel and the test panel), is located on the pushbutton control module. This module generates the motion command lines RUN NORMAL, RUN FAST, and RUN REVERSE, which are supplied to the ramp generator module to initiate actual tape motion.

12.6.1 Front Panel Pushbutton Controls

The LOAD, ON LINE, and REWIND pushbuttons, located on the main control panel, are connected to respective flip-flops on the pushbutton control card. When the LOAD pushbutton is activated, it grounds the input to inverter E12-1, setting the load flip-flop which consists of NOR gate E13-6 and inverter E12-1. Once the load flip-flop is set, E13-6 goes low, is inverted by E12-4, and removes the direct-clear from on-line flip-flop E10-3. Thus the on-line flip-flop can be set only after the transport has been loaded. When the ON LINE pushbutton is activated the first time, it toggles E10-1 to the set, or on-line, position and the outputs of the flip-flops generate ON LINE true. Inverters E12-8 and E12-10 are connected as a protective flip-flop on the clock input to E10-1. Once the on-line flip-flop has been set, ON LINE true is inverted twice by E9, setting the common of the REWIND pushbutton on the control panel high, disabling that pushbutton. The on-line flip-flop can be cleared by pressing the front panel pushbutton a second time, or by an adapter off-line command (OFF LINE CMD), supplied from the adapter control module.

The REWIND pushbutton can be activated only when the transport is off-line. When activated, the REWIND pushbutton sets the flip-flop that consists of gates E8-8 and E8-6, provided that the transport is loaded at the time (LOAD true at E8-13) and test mode is not selected (E7-8 high). Consequently the transport cannot be rewound by the pushbutton during test mode, when on-line, or when LOAD is false. When the transport is on-line, the rewind flip-flop can be alternately set by REWIND CMD, supplied from the adapter control module. The output of the rewind flip-flop, (REWINDING), activates NOR gates E15-8 and E14-6, generating RUN FAST and RUN REVERSE true to the ramp generator module, initiating a fast reverse motion to the load point. When the load point is detected, the photosensor amp driver module supplies the load point pulse at input pin H of the pushbutton control module, clearing the rewind flip-flop.

An additional flip-flop, E10-6, is used to locate the tape position. Before the tape is loaded, the flip-flop is cleared by LOAD false at E10-8. When the transport is loaded, the direct-clear is removed and NAND gate E14-11 is enabled. Since the on-tape flip-flop is still cleared, its $\overline{Q}$ output high activates NAND gate E14-8, generating RUN NORMAL at output pin Y, advancing the tape to the load point. When the load point marker is detected, AT LOAD POINT true at input pin 21 from the photosensor module is gated through E16-3 and direct-sets flip-flop E10-7 to the on-tape state, terminating the tape motion. Similarly, when the load point is detected during reverse tape motion, the on-tape flip-flop is toggled by NAND gate E16-11 to the clear state, initiating forward tape motion back to the load point.

12.6.2 Busy

This module generates a DRIVE BUSY output when the tape is not loaded, when it is advancing to the load point, or when the transport is off-line and not in test mode. In any of these cases, NOR gate E4-8 is activated and supplies DRIVE BUSY true to the adapter control module.

12.6.3 Write Ready

WRITE READY true is generated in two different cases: when the control interface module adapter supplies WRITE CMD true and the transport is not in test mode (TEST MODE false), or when the transport is in the write test mode and flip-flop E6-14 is set. In either case, NOR gate E1-8 is activated, enabling NAND gate E4-5. The gate is activated provided that DRIVE BUSY is false, WRITE RING ON (file protect) is false, and the transport is not in reverse motion (RUN REVERSE is false). E4-6 then goes low, is inverted by E5-12, and generates WRITE READY true at output pin J to the four-channel write amplifier module.

12.6.4 Test Panel Control

To activate the test panel, the transport must be off-line and the test panel STOP pushbutton must be pressed. In that case, the TEST MODE pushbutton on the test panel can be activated, setting the flip-flop that consists of inverters E11-8 and E11-10, which in turn toggles the test mode flip-flop E6-6 to the test mode state, generating TEST MODE true. The test mode flip-flop is direct-cleared when the transport is placed on-line or when the TEST MODE pushbutton is activated a second time. After the test mode flip-flop has been set, the other test panel pushbuttons are enabled. The WRITE TEST pushbutton may then be activated, setting the protective flip-flop consisting of inverters E11-4 and E11-6, which in turn toggles write test flip-flop E6-1 to the write test mode, provided that forward motion is selected. The $\overline{Q}$ output of the write test flip-flop then activates NOR gate E1-8, in turn activating write ready gate E4-5, provided that WRITE RING ON, RUN REVERSE and DRIVE BUSY are all false. In that case, WRITE READY true is generated at output pin J to the write amplifier module, where it enables the write data strobe circuitry. During the write test, the write amplifiers generate consecutive all-1s characters which may be used to adjust the skew.

Additional test panel pushbuttons are FORWARD RUN, a normal forward run button, FAST FORWARD, a high-speed forward button, REVERSE RUN and FAST REVERSE buttons. The reverse motion buttons can be activated only if on-tape flip-flop E10 is set and the tape is not at the load point, activating NAND gate E3-3, which in turn activates NAND gate E7-6 (when the test mode flip-flop is set) and setting the common of the reverse buttons low. The forward motion commands are terminated when either the STOP pushbutton is activated, clearing the test mode flip-flop, or the end of tape is detected, in which case END OF TAPE IND true is inverted by E17-4, disabling NAND gate E7-3 and setting the common of both forward motion buttons high.

Similarly, the reverse motion can be terminated by activating the STOP pushbutton, which terminates all test mode operations, or when the load point is detected, in which case AT LOAD POINT true is inverted by E17-3 and disables NAND gates E3-3 and E7-6, setting the common of the reverse buttons high. The pushbutton control module also drives the test panel indicators, lighting the DATA lamp when any data is being processed by the write/read electronics, illuminating the SKEW indicator when the skew is out of adjustment, illuminating the EOT indicator when the transport is at the end of tape, and illuminating the LOAD POINT indicator when the transport is at the beginning of tape.

12.7 TYPE 3645 RAMP GENERATOR MODULE CIRCUIT DESCRIPTION (TD5)

The ramp generator produces the proper analog signal inputs to the capstan servo system to control the direction and velocity of tape motion. The outputs are voltages that rise and fall linearly at controlled rates to highly stable levels. These analog signals are controlled by digital logic outputs from the control section. Waveforms produced are shown with the schematic.

Two similar ramp generator circuits are provided: one for normal speed operation and one for high speed operation. E4 is an operational amplifier in the run normal speed circuit. The amplifier output is normally saturated in the negative direction. When its positive input at pin 5 is high, the output saturates at +10 V. This occurs when the RUN NORMAL input sets flip-flop E7. E4 feeds FETS Q1, Q2 which are connected in a constant-current circuit. The magnitude of current flow in the circuit is controlled by R3 and R4. R3 controls current in the positive-going direction, or start ramp, while R4 controls the negative-going stop ramp

Since C1 is charged by a constant current, its voltage rises linearly until clamped by CR1 to a value one diode drop below +5 V. Q3 is an emitter follower whose output rises to a value of +5 V, since the emitter can rise one diode drop higher than the base. When the input from E7 to E4 drops, the voltage fed to Q1, Q2 goes to −10 V and C1 is discharged linearly until clamped by the base-collector diode of Q3. Since Q3 base goes one diode drop negative, and the emitter is at zero, a positive-going ramp has been generated.

The ramp voltage output from Q3 is fed to FET switches Q4 and Q5. If forward direction has been selected, Q4 is on and Q5 is off. The ramp is then amplified by unity gain operational amplifier E3, without inversion, and appears as a positive-going ramp at test point A. If reverse is selected, Q5 is on and Q4 is off. The ramp is then fed to the inverting input of E3 and appears as a negative-going ramp at test point A. Forward/reverse selection is controlled by flip-flop E6 and Q9, Q10.

Ramp amplitude and, therefore, tape speed is controlled by normal speed control R14 and output summing resistor R15. The fast forward and reverse ramps are produced by a similar circuit involving amplifiers E1 and E2. However, since rewind speed and ramp time need not be precisely controlled, resistors are used instead of FETs to charge and discharge C4 and produce an approximate 0.5 second rise/fall time. CR9 and CR10 isolate the ramp output from any small offsets that may be present in E2. Rewind speed is controlled by summing resistor R16. Operational amplifier E5 at zero ramp output has a slight bias produced by R37 and R38, keeping its output negative. When the ramp rises above the bias, E5 switches to positive output, indicating that the tape is running. This output is used to gate off the input circuits through E10 and E9. Flip-flops E7 and E8 may be reset by run normal or run fast inputs going false, but cannot be set again until the tape comes to a stop. This prevents damage from illegal commands and reduces timing requirements.

Type 3645 Ramp Generator includes an additional flip-flop, E11-8, whose function is to enable consecutive run normal commands to be received without requiring the tape to ramp down to a stop following each normal speed operation. Following a run fast command, however, flip-flop E11 is set by E8, inhibiting any run normal commands until the tape comes to a stop, at which point E9-6 clears E11-9, and the 0 output at E11-8 enables E7-2.

12.8 TYPE 3844 SENSOR AMPLIFIER/DRIVER MODULE CIRCUIT DESCRIPTION (TD6)

This module responds to signals from photoresistive cells which sense load point and end-of-tape reflective strips, and broken tape. In addition, this module contains the file protect circuitry and the write and the erase head drives.

12.8.1 BOT, EOT, and TAPE THREADED Sensor Amplifiers

The load point sensor amplifier and the end-of-tape sensor amplifier operate interdependently to detect the load point and the end-of-tape markers. The active components in detecting EOT and load point are two operational amplifiers, E6 and E8, and two transistors, Q1 and Q2, in conjunction with associated components. Transistors Q1 and Q2 act as current sources; potentiometer R16 is used to adjust the transistor base currents to equalize the voltage at the inputs of E8, the load point sensor amplifier, and E6, the end-of-tape sensor amplifier. Resistors R18, R19, R20, and R21 are used to bias the amplifiers' inputs when plain tape is in front of the photo sensors. When either the load point marker or the end-of-tape marker is detected, the resistance of the respective photoresistive cell is lowered by approximately 60 percent of its unilluminated value. Each cell is returned to +10 V, and a 30 percent change in its resistance, causing a 30 percent change in the input potential, will be sufficient to switch the output of the respective operational amplifier. Resistors R17 and R22 serve as feedback loops for noise protection. Thus when load point is detected, the load point sensor output at input pin Y of this module saturates E8, causing its output to go high, and is inverted twice by E7 to generate AT LOAD POINT true at output pin 19 to the pushbutton control module. The output of inverter E7-8 is also supplied to an edge circuit which produces a 1 μs pulse on the trailing edge of AT LOAD POINT. This pulse is output at pin 8 to the pushbutton control module. The EOT sensor amplifier operates in the same manner, generating a high output when the EOT marker is detected, and supplying END OF TAPE true at output pin X to the pushbutton control and control adapter modules.

When the broken tape photoresistive cell is illuminated, the resistance of the cell is reduced enough for the +10 V to turn on transistor Q3. The collector of the transistor goes to ground, generating TAPE THREADED true at output pin 18. When LOAD SW is high at input pin U, the output of E4-8 is low. This causes the collector of Q3 to be low through the diode CR3 and the TAPE THREADED output will be true at output pin 18. Also, when power is initially turned on, capacitor C9 will cause the TAPE THREADED output to be high, which presets the load flip-flop on the adapter control module.

12.8.2 File Protect Circuits

The file protect switch output is supplied to this module at input pin T. When a reel is loaded without a write enable ring, the switch contact remains grounded; the switch input at pin T is inverted by E2-6 and enables NAND gate E4-13. The gate is activated when TAPE THREADED is true before the transport is loaded. Whenever the LOAD pushbutton has not been energized, E4-8 low grounds the clear input of flip-flop E4-1 through diode CR14. E4-2 then issues WRITE RING ON (file protect) true at output pin 9 to the adapter control card, while the 0 output of E4 high is inverted by E2-8 to turn off transistor Q5, disabling the file protect solenoid output at pin P.

When a reel with a write enable ring is used, the file protect switch is opened, setting input pin T high and enabling NAND gate E2-13. Again the gate can be activated only when TAPE THREADED is high, before the transport is loaded. The output of the gate then goes low to set flip-flop E4-5; the flip-flop can be set only after LOAD SW has gone false. This provision is made to ensure that the write mode can be selected only at the time tape is first loaded. Once flip-flop E4 is set, its 1 output issues WRITE RING ON false, and, after being inverted by E1-10, lights the WRITE ENABLE lamp through output pin H. The 0 output of the flip-flop low is inverted by E2-8 and turns on transistor Q5, activating the file protect solenoid through pin P. The file protect solenoid then draws in the switch pin, and the transport is ready for the write operation.

12.8.3 Write, Erase Drives

When the file protect switch is grounded, it also turns off transistor Q7, in turn shutting off the current at the base of Q8. This cuts off the write head and erase head drive currents supplied by transistor Q8. In order for the write and erase drives to be turned on, the file protect switch must be opened and WRITE READY must be true at input pin 7. This will activate NAND gate E2-3 causing op amp E3 to turn off transistor Q9, in turn enabling transistor Q8 to turn on and supply the write and erase head currents at pins 22 and J.

The zener diode in the base of Q7 detects when power is being dropped. This turns off Q7 early enough in the power-down sequence to turn on Q9 and remove the head current supplied by Q8. This avoids putting unwanted remnants on tape during a power failure.

12.9 TYPE 4306 SERVO PREAMPLIFIER MODULE CIRCUIT DESCRIPTION (TD3,4)

This module contains the capstan servo and reel servo amplifier stages. The following paragraphs describe their operation.

12.9.1 Capstan Servo Amplifier Stage

The capstan servo amplifier portion of this module is a part of a velocity servo system which produces accurately controlled capstan speeds with linear ramp-ups and ramp-downs. The analog linear signal supplied from the ramp generator module is input at pin N of this module and is summed with the output of the dc tachometer coupled to the capstan motor shaft, supplied at pin P of this module. Any difference between the two voltages is amplified by operational amplifier E5. The amplification of E5 is controlled by two negative feedback loops, one supplied directly from the output of E5 through resistors R39, R40 and capacitor C9, and the other loop from the capstan motor through resistor R71. The zero offset of the amplifier is adjusted by potentiometer R56 to eliminate capstan creep during standstill.

The output of amplifier E5 is supplied to a pair of complementary driver stages, including transistors Q11, Q12, Q17, and Q18. The output of these stages is supplied to a pair of power transistors located on the heat sink servo power assembly, which is on the rear of the unit. The power transistors' output then energizes the capstan motor, advancing tape at accurately controlled speeds.

12.9.2 Reel Servo Amplifiers

Takeup and supply reel servos are provided to maintain tape tension at a constant value. Three main components are included: magpot position sensor, reel servo amplifier, and reel motor.

The magpot position sensor measures tape tension by the position of a spring-loaded buffer arm. At the approximate center of the arc, sensor output is zero. As the buffer arm moves off center, a positive or negative voltage is produced which is proportional to the error.

The output of the reel servo amplifier on this module is supplied to a pair of power transistors located on the servo power assembly on the heat sink on the rear of the unit. The output of the power transistors then energizes the respective reel motor, returning the buffer arms to their proper locations.

12.10 TYPE 3631 READ PREAMPLIFIER CARD CIRCUIT DESCRIPTION (TD10)

Read Preamplifier Type 3631 includes nine identical amplifier stages which accept the analog signals from the read head winding and supply the amplified outputs to the read amplifier modules.

The channel 0 amplifier stage is shown in the schematic; the other channels are identical. The amplifier stage consists of high-gain operational amplifier E1 and negative feedback including resistors R2, R3, R4, R5, and capacitor C2. The input head signal is filtered by resistor R1 and capacitor C1, and is supplied to the non-inverting input of E1. The negative feedback network controls the output amplitude and response.

Potentiometer R4, located in the feedback network, is adjusted so that the amplified analog output at test point A is 9 V peak-to-peak while writing 800 flux reversals per inch (see adjustment procedures in Part 1 of this manual).

12.11 TYPE 4218 MAGPOT TENSION ARM POSITION SENSOR CIRCUIT DESCRIPTION (TD3)

In the reel servo system, it is necessary to produce an analog signal representing tension arm position. The signal must be zero at the nominal resting position of the tension arms and should linearly represent angular deviations from the center of arm travel by positive and negative voltages. A common method utilizes lamps, photocells, and a shutter to produce the required voltage. This method suffers from the mortality of lamps and the relatively slow response of photocells.

Part III

The magpot operates as a differential transformer, an example of which is shown in Figure 12-2.

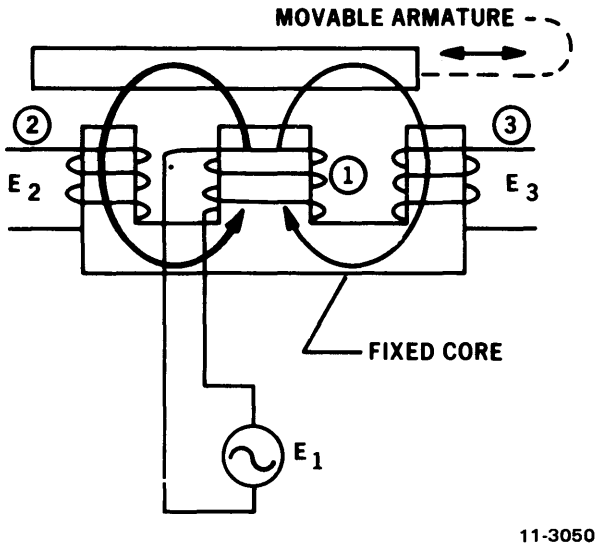


Figure 12-2 Differential Transformer

Magnetic flux produced by current in winding 1 will produce voltages E_2 and E_3 in the other windings. If the armature is symmetrically located with respect to 2 and 3, flux in the two windings will be equal, and since they have the same number of turns, $E_2 = E_3$. If the armature is displaced as shown, $E_2 > E_3$ since the flux coupling E_3 has been reduced. Displacement in the opposite direction produces $E_3 > E_2$. Displacement from center then is represented by $E_0 = E_2 - E_3$. In the configuration shown in Figure 12-2, this relation is linear only for very small displacements because area relations are not linear.

The magpot is an adaptation of the above scheme in that there are three windings on a magnetic core. The core in this case is a ferrite pot core while the armature is half a pot core. Windings 2 and 3 are around legs of the pot core while 1 is around the center portion common to the two legs. Winding 1 is energized by a high-frequency oscillator (approximately 200 kHz). The magpot is in balance and $E_2 = E_3$ when the armature couples equally to the two legs. As the armature is rotated, the area available for magnetic flux increases linearly for one leg and decreases linearly for the other leg. Thus the difference in induced voltages is a linear representation of angular movement.

The 200 kHz oscillator is a Hartley circuit comprising Q1, C1, C2, R1, R2. It produces a 40 V peak-to-peak sine wave across the primary winding.

The two secondary windings are connected in series and their voltages are rectified by CR1, CR2. The two rectified voltages are subtracted and referenced to ground. Thus the input to E1 operational amplifier is a dc voltage equal to $E_2 - E_3$. This voltage is null when $E_2 = E_3$ and is positive or negative depending upon which is larger. Secondary voltages induced are at all times large enough to overcome the diode drops in CR1, CR2.

DC output of the rectifier circuit is amplified by E1 and fed from the output to the appropriate reel servo amplifier.

Voltage output for a given angular deflection depends upon coupling between the fixed core and armature at that setting. The gain relations are such that a spacing of 0.030 in. (76.2 mm) between core and armature results in ±5 V output for full arm travel. Spacing is established by two 0.015-in. thick plastic spacer washers on the shaft.

12.12 TYPE 4845 DELAY TIMING MODULE CIRCUIT DESCRIPTION (TD12)

Crystal oscillator, dividers, and timing circuits associated with read electronics comprise Type 4845 Delay Timing. Use of this circuitry eliminates the need for analog delays in forming the read skew gate, detecting gaps, etc. Since the delays required vary with tape speed, switches are provided to select appropriate delays. Delays required are fractions or multiples of character times; therefore it is only necessary to change the division ratio to accomplish all required modifications. As the TM8-M System operates only at a speed of 12.5 inches per second, the switches are shown on the logic diagram set for that speed; i.e., S2, S6 and S7 closed. Crystal-controlled pulses generated are also supplied to write electronics in the test mode to allow writing an all 1s test pattern.

12.12.1 Crystal Oscillator Divider

E5 together with several discrete components is connected as a crystal oscillator. The two inverter sections are biased into the linear region by R1, R2, and R3. Positive feedback through Y1 causes the circuit to oscillate at the crystal frequency. A series of dividers E2 (÷ 12), E1, E4 (÷ 16) are selected by S2, S6, and S7 to produce two output frequencies: 10 kHz, which is the repetition frequency of the data to be read and 320 kHz which is 32 × 10 kHz and divides the bit cell into 32 increments. These are fed to counter circuits which determine delays.

12.12.2 Skew Gate Generation

Skew gate length has three values depending upon operating mode: 1/2 of one bit cell for read, 3/8 for write, and 5/32 for test mode. The write skew gate is shortened to provide a more stringent skew criterion to reveal incipient skew problems.

Pulse outputs from the nine read amplifiers are wire-ORed and appear at pin R. E3 buffers the pulse input and feeds out to the test panel for service use.

The first DATA PACKET pulse to appear clears E14 and counter E15 begins to count 320 kHz pulses. E15 has been preset clear by low levels on inputs ABCD. At the count of 16, representing 1/2 character time, E15 Q_D has been high and goes low, setting E14 and stopping the count. With E14 set, E11, a four-stage shift register, starts shifting right. A 1 has been preset in position A and 0s are shifted in, causing the 1 to progress to the right. Shift frequency is 320 kHz. At the time E14 is set, a 1 is in Q_A and E12 produces a data transfer pulse to the read amplifiers, causing the data to appear at their outputs. At the next count Q_B goes high, triggering one-shot E10 (2 μs) and producing a read data strobe RD STRB at the output. At the third count, Q_C goes high as a delay, and on the fourth count Q_D goes high. If strap ST1 is installed, a second data transfer pulse is produced, returning the read amplifier output to zero. After the fourth shift pulse, the circuit remains quiescent until the next DATA PACKET.

12.12.3 Skew Lamp

At a time just after the skew gate (at RD STRB time), output from E14 is inspected by one-shot E10. If the skew delay circuit has been retriggered by a skewed input, E10 is triggered, producing a relatively long SKEW ERROR pulse to the SKEW indicator lamp.

12.12.4 Write Mode

If write is selected, WRITE READY is high, causing counter E15 to be preset with a count of 4 by E12. Operation is otherwise identical to read operation but delay is reduced from 16 to 12 counts or 3/8 of one bit cell.

12.12.5 Test Mode

In test mode, delay is further reduced to provide a marginal skew check. The counter is preset by the TEST MODE input (pin U) to E15 and delay is five counts or 5/32 of one bit cell. An all 1s pattern on a properly deskewed machine should fall within this time; however, due to bit crowding on tape, random data generally will not.

12.12.6 Blank Space Detection

Type 4845 detects the space between the last data character and the CRC and clears read amplifier outputs. The read amplifier outputs are again cleared after the CRC (if not all zeros) and once again after the LRC, leaving all outputs cleared in the IRG. Whenever E14 is set (between bits), counter chain E6, E7 counts 320 kHz; it is cleared by E14 if a DATA PACKET is detected. Should the counter reach a count of 32, indicating a missing bit, E7 is set which in turn sets E8. The next 320 kHz pulse, through E8 pin 3, clears E7, leaving E8 set and the counter held clear by E8 pins 8, 12. E9 produces a RESET pulse at pin K, clearing the read amplifier. At the next DATA PACKET, input E8 is cleared and the cycle is free to repeat. This DATA PACKET may result from the CRC, LRC, or the first character of the succeeding block.

12.12.7 Read Delay

When the tape is stopped as indicated by RUN CMD false, SELECTED & ON LINE false, AT LOAD POINT true or DRIVE BUSY true, the E19-6 output (INHIBIT DATA OUTPUT) is asserted thereby gating off RD STRB pulses at E9.

Upon receipt of a RUN CMD input, counter chain E17, E18 is enabled for a count of 128 10 kHz pulses. This corresponds to 0.16 in. (0.41 cm) of tape movement. During this time, outputs remain disabled.

12.12.8 Data Lamp

Drive for the test panel DATA lamp comes from E14 through E8 pin 6, which is low whenever E14 is set (between characters). An inverter on the PCB module actually drives the LED indicator.

12.13 TYPE 3848 FOUR-CHANNEL WRITE AMPLIFIER MODULE CIRCUIT DESCRIPTION (TD13)

This module generates the internal write data strobe and contains the write amplifier stages for four of the data channels, channel P through channel 2. These are explained in detail in the following paragraphs.

12.13.1 Write Data Strobe Generation

The REC (write data strobe) is input from the adapter at pin A and is supplied to an edge circuit consisting of inverters E5 and E6, capacitor C8, and NAND gate E6-8. If WRITE READY and SELECTED & ON LINE are true at input pins 12 and 13 of E6, the gate transmits a short pulse on the leading edge of each REC input. The pulse is gated through NOR gate E5-6 and triggers one-shot E1-1 on its trailing edge. The Q output of the one-shot supplies a positive 0.5 μs pulse which is gated through NAND gate E7-3, provided that the transport is not in a test mode. The pulse then enables write NAND gates E11 and E15*, gating the input write data to the write amplifier stages. It is also supplied as WRITE DATA STROBE to Type 3849 five-channel write amplifier module. When E1-13 generates the write strobe, its $\overline{Q}$ output triggers the second E1 one-shot, which in turn inhibits E6 for a 3.5 μs duration, inhibiting any pulses during that time.

If the transport is in test mode, TEST MODE true at pin K enables NAND gates E5-2 and E7-10, 12 while disabling NAND gate E7-2. If WRITE READY is true, crystal-controlled data frequency (10 kHz) supplied from the delay timing module, is gated through NAND gate E5-12 and NOR gate E5-6 to generate the test mode strobes. These are gated through the E7-8 and E7-11 NAND gates and direct-clear the write amplifier flip-flops on this module and on the other write amplifier module, writing the all-1s characters of the test mode.

12.13.2 Write Amplifier Stages

The data inputs are supplied from the data terminator card at pins 11, 12, 13, and 14, are inverted, and then strobed through NAND gates E11 and E15* by the WRITE DATA STROBE, generated at test point B. The write channels are then supplied to the amplifier stages, each consisting of a divide-by-16 counter, a pair of flip-flops, and a pair of drivers. The amplifier stages are digitally deskewable, where the delay of channels 0 through 7 is adjusted to coincide with that of the reference channel, channel P, when read back.

*E15 is the E11 equivalent in channels 1 and 2 which are not shown.

The delay of channel P is permanently set to the count of eight, equivalent to 1/4 character delay, by counter E8. Whenever the input data is 1, the WRITE DATA STROBE pulse is gated through E11-8 and direct-clears flip-flop E9-13. The $\overline{Q}$ output of the flip-flop goes high, removing the direct-clear from the E8 counter. The counter is then clocked by 320 kHz at 32 times the data frequency until the count of eight, at which point the Q_d output of the counter goes low and toggles the E9 flip-flop to the set state. The $\overline{Q}$ output of E9 then goes low, locking the counter and toggling the output flip-flop E9-9. During the next 1 character, the same process is repeated with output flip-flop E9-9 toggling to the opposite state. When a 0 is input, the input NAND gate E11-8 does not transmit the write data strobe, and consequently the write amplifier flip-flops are not toggled. The outputs of flip-flop E9-5, 6 are then supplied to a pair of drivers E10 which energize the write head, reversing the flux for each 1 while remaining unchanged for each 0, as required for NRZI.

The operation of the amplifier stages of the eight other channels is identical to that of channel P, except that their delay is digitally adjustable. Four switches are connected to the parallel inputs of the skew delay counters of the eight channels, as shown for data channel 0. The skew of each channel can be measured and adjusted during the write test mode, which writes all-1s characters, by observing the analog outputs at the Type 3631 read preamplifier module.

Opening the switches reduces the count while closing them increases it. Thus when the switches are all opened, the counter is direct-set to 16, gating the data character to the output without any delay. When the switches are all closed, the skew counter is set at 0 and the character will be delayed 16 counts, or 1/4 character time behind channel P.

12.13.3 Write Amplifier Reset

An LRC PLS pulse is input at pin J from the data terminator card, and is gated through NAND gate E2-3, provided that SELECT & ON LINE is true, to set flip-flop E2-12. The 1 output of the flip-flop goes high, removing the direct-clear from shift register E3. The register is then clocked by 320 kHz at 32 times the data frequency. On the seventh pulse, the Q_g output of the register goes high and is inverted by E4-8 to issue WRITE RESET, resetting the write amplifier flip-flops on this module. WRITE RESET is also output at pin H to the Type 3849 write amplifier where it resets the flip-flops of the other amplifier stages. On the eighth pulse to the register, the Q_h output goes high and is inverted by E4-11, clearing flip-flop E2 and locking itself until the next LRC is issued by the interface.

12.14 TYPE 4178 QUAD READ AMPLIFIER MODULE CIRCUIT DESCRIPTION (TD10, 11)

Quad read amplifier type 4178 accepts amplified head signals from the head preamplifier module and supplies decoded and deskewed data outputs to the adapter. Each module contains four amplifier stages, and each transport contains two of these modules. The channel P amplifier stage is located on the read amplifier/clipping control module. The operation of the channel A amplifier stage is explained in the following paragraphs. The other amplifier stages operate identically.

The amplified analog signal is supplied from the read preamplifier at input pin J. The signal is filtered through R1; the negative half-waves are routed through diode CR1 while the positive half-waves are routed through CR2. CR1 and CR2 are back biased by the negative and positive clipping levels, respectively, supplied from the Data Clip Level Control to eliminate spurious baseline pulses. The negative half-waves are then differentiated by C4 and R6 and are input at the inverting input of operational amplifier E1. At the leading edge of the negative analog half-wave, the differentiated output of C4 and R6 swings negative, crossing zero at the peak of the analog signal and then going positive until the trailing edge of the analog signal. Normally the op amp output is low, since the noninverting input of E1 is negatively biased through R7 and R9. When the leading edge of the differentiated signal exceeds the input threshold, the output of the amplifier swings positive. The amplifier output returns to 0 V at the zero crossover of the differentiated signal, corresponding to the peak of the input analog signal. A similar transition occurs for the positive half-wave, since it is input at the noninverting input of the amplifier. Consequently the amplifier output goes high and returns low for each 1 character, with the negative-going transition occurring at the analog peak. The output of the amplifier is limited by diodes CR3 and CR4 and

is inverted by NAND gate E2-3. E2-3 output is supplied to a filtering network, consisting of C6, R11, R12, and CR5, whose output is in turn supplied to the Schmitt trigger input of one-shot E3. The output of E2-3 is normally high, and the voltage at the input of E3-5 is at 3.3 V. When the output of E1 swings positive, E2-3 goes low and capacitor C6 discharges through R12 with a slow time constant, approximately 5 μs at 25 in./sec. The voltage is clamped at 0 V by diode CR5. When the output of E1 goes low again at the peak of the analog input, E2-3 goes high and C6 charges with a much faster time constant, approximately 300 ns. When C6 charges up to 1.8 V, one-shot E3 triggers, generating a 300 ns pulse. The $\overline{Q}$ output of the one-shot is connected back to E2-2, disabling the gate and preventing the one-shot from being retriggered by spurious pulses on the input.

The positive pulse generated by the Q output of E3 is inverted by E2-11 and is output as DATA PACKET at pin V. The pulses of all the amplifier stages are wire-ORed and supplied to the delay timing module where they are used for read deskewing and read data strobe generation. The $\overline{Q}$ output of one-shot E3 direct-sets flip-flop E4-4, the data storage register. The Q output of E4-5 sets the D input of output register E4-12 high. A skew delay time is provided for all channels to be read after the leading data pulse is detected. TRANSFER DATA (supplied from the delay timing module) toggles the output register flip-flops of all channels simultaneously after the allowed skew delay time, outputting the deskewed, decoded data to NAND gate E2-9 and, on its trailing edge, clears the first stage of E4. The gate is enabled by INHIBIT DATA OUTPUT false, supplied from the delay timing module at input pin S. E2-8 supplies the output data at pin W to the interface. The length of the skew delay time is varied depending on the operation being performed. This is described in the delay timing module circuit description.

12.15 TYPE 4179 READ AMPLIFIER/CLIPPING CONTROL MODULE CIRCUIT DESCRIPTION (TD10)

This module contains the P channel read amplifier stages and the read amplifier clipping level control. The operation of the P channel amplifier is explained in the circuit description of the quad read amplifier module, and the read amplifier clipping level control is explained below.

The read amplifier/clipping control provides four clipping levels to the read amplifier: normal, low, high, and very high. When an error is detected during a read operation, the transport may be commanded by the tape control unit to backspace over the erroneous block to reread it. The clipping level is kept at a normal level during the first reread. If a second reread is commanded, the clipping level is switched from normal to a lower clipping level, to compensate for a possible partial dropout. If a third reread is initiated, the clipping level is switched to a higher than normal level to eliminate possible baseline noise spikes. During a read-after-write operation, the normal and high clipping levels are combined to supply a still higher clipping level which is not used during a read operation. The switching of the clipping levels is explained in detail below.

The initial stage of the circuitry will be both E10 flip-flops set and both E11 flip-flops clear. This is established by DRIVE BUSY at pin Y true when tape is initially loaded or rewound. Since the first command from the load point is always a run forward command, RUN CMD (run normal) at pin H true and REVERSE CMD (reverse select) at pin W false causes E8-8 to be low, clearing the E9 flip-flop. The E10 flip-flops remain in the set state when clocked by E9-3 high. The circuitry remains in the states just described until a reverse command is given to the tape unit. When RUN CMD and REVERSE CMD are true, E8-6 goes low, direct-clearing the E10 flip-flops which causes E10-8 to go high removing the direct-clear from the E11 counter flip-flops. Also E8-6 low sets the E9 flip-flop which makes E9-6 low; E11-12 toggles causing E11-3 to go high, putting the counter in the "01" state. The clipping level does not change because the E12, E13 gating described in the next paragraph establishes the same clipping level. The circuitry will now remain in this state until a forward command is given. The next forward command causes E8-8 to go low, clearing the E9 flip-flop and toggling E10-5 high. At this point two things could happen: the tape unit will be commanded to go forward to continue reading the next data block, or to backspace if the adapter decides to reread the data block. If the tape unit is commanded to go forward to continue reading, then E8-8 low makes E9-3 high, causing E10-8 to go low which direct-clears the E11 counter to its initial state. If instead the tape unit is commanded to go in reverse, E11-12 goes low, toggling the E11 counter to its next state. This establishes the next clipping level in the sequence.

The E10 flip-flops are cleared as just described. The E11 counter will continue to toggle every time the tape unit is commanded to backspace after being commanded to go forward once. Two forward commands in succession will reset the E11 counter by setting E10-8 low, and reading continues at the normal clipping level.

The clipping levels established by the E11 counter through E12 and E13 are as follows:

1. 00 and 01 cause E13-6 and E13-11 to be low and E13-3 to be high, establishing the normal read clipping level;

2. 10 causes E13-6 and E13-3 to be low and E13-11 to be high, establishing the low clipping level;

3. 11 causes E13-3 and E13-11 to be low and E13-6 to be high, establishing the high read clipping level.

During a read-after-write operation, WRITE READY at input pin J is inverted by E7-12 and disables the automatic clipping level control by direct-setting the E10 flip-flops, keeping the E11 counter direct-cleared. At the same time, WRITE READY true activates NOR gate E13-4, enabling the higher clipping level, while the Q output of E11-5 low enables the normal clipping level. Thus the normal and high clipping levels are combined to generate a still higher clipping level used during read-after-write only.

The automatic clipping level control is also disabled when DRIVE BUSY is true at input pin Y of the module. In this case, NOR gate E7-6 is high, and direct-sets the E10 flip-flops which in turn keep the reread counter E11 cleared.

Operational amplifier E6 is connected with negative feedback through R26, establishing its gain at a value determined by the ratio of the input resistance to +10 V switched by E13 to the value of R26 (22K).

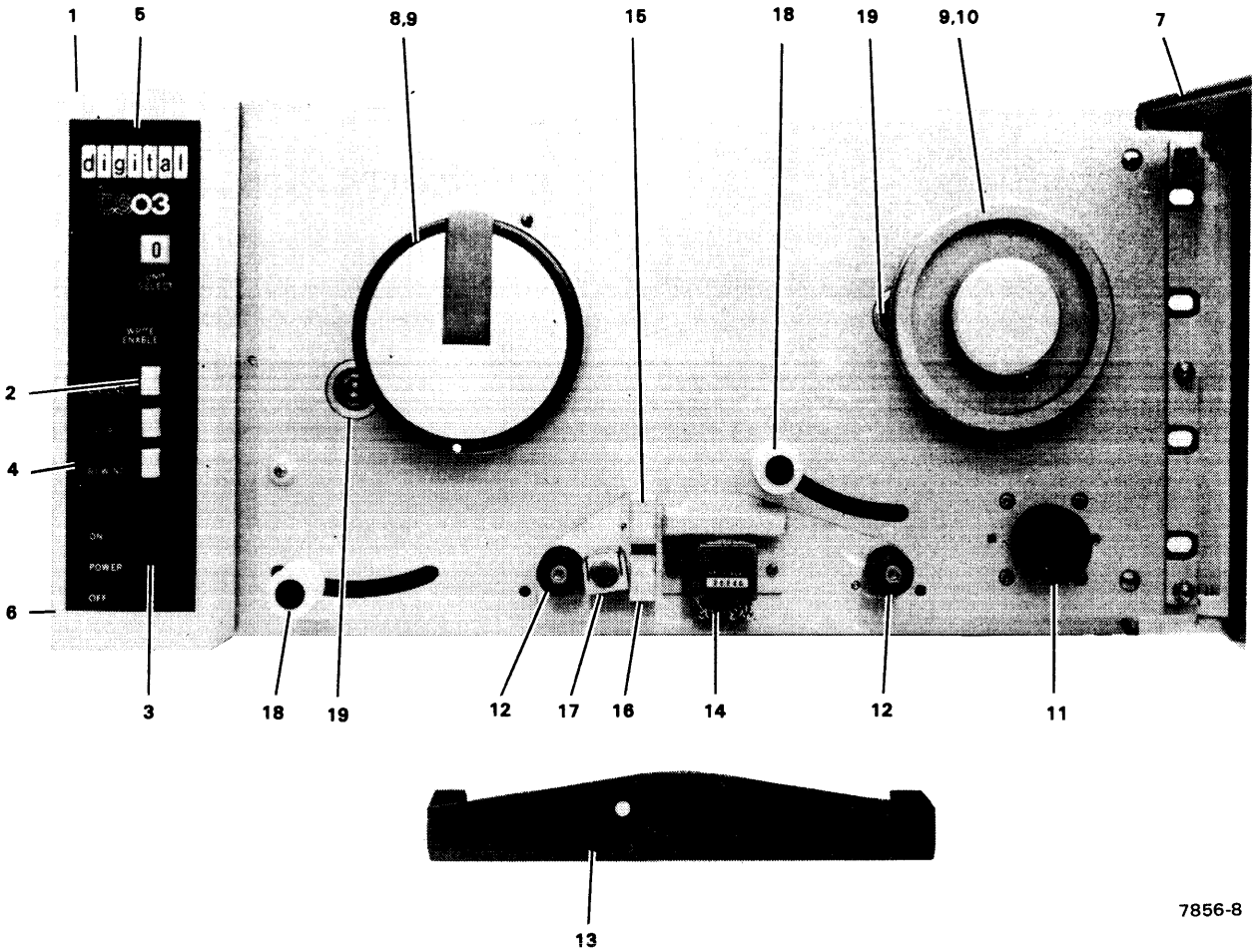
Capacitor C10 acts as an integrator, slowing the response of E6 to a change in input, which avoids coupling enough signal through C4 and C5 into E1 to cause a spurious output. E5 is connected as an inverter, outputting an equal but opposite polarity voltage to that voltage at E6-6. The negative clipping level voltage (TPD) and positive clipping level voltage (TPC) are then applied to each read amplifier through a resistor-dividing network to backbias diodes CR1 and CR2. This establishes the amplitude of analog input from the read preamplifier required for E1 to switch and thus detect data.

CHAPTER 13
PARTS IDENTIFICATION

Figures 13-1 through 13-3 and Tables 13-1 through 13-3 show the location and identify parts comprising the TS03 DECmagtape Transport. Tables 13-4, 13-5, and 13-6 list replaceable/spare parts.

NOTE

See the engineering drawing set for parts information on the M8920 adapter module.



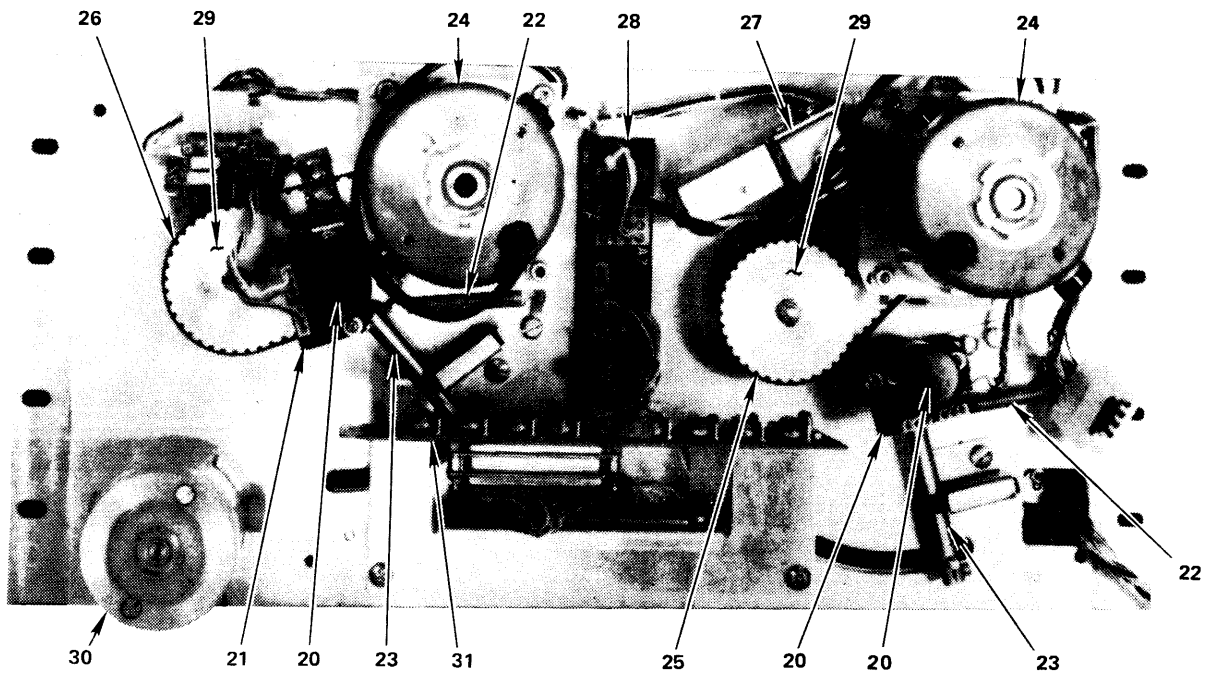


Figure 13-1 Front Panel Parts Identification

Table 13-1
Illustrated Parts Breakdown for Figure 13-1

Item	Part No.	Description
1	*	Control Panel Assembly (Note 1)
2	151-0057-001	Pushbutton Switch Assembly
3	151-0038-001	Power Switch
4	190-4448-001	LED Display, PC Board Assembly
5	291-3922-xxx	Switch Cover (Note 1)
6	391-4440-xxx	Control Panel (Note 1)
7	*	Dust Cover Assembly
8	190-2744-001	Hub, Quick Release (Note 2)
9	198-0011-001	Hub Bearing Assembly
10	190-2772-001	Takeup Hub
11	*	Capstan Wheel
12	*	Tape Guide Assembly
13	291-1509-001	Head Cover (Note 1)
14	*	Head Assembly
15	*	Photosensor Assembly, Load Point, EOT
16	*	Photosensor Assembly, Broken Tape
17	*	Tape Cleaner
18	*	Tension Roller Guide Assembly
19	190-4554-001	Tension Arm Bearing Assembly
20	*	Magpot Tension Sensor Assembly
21	*	Magpot Circuit Module
22	*	Spring, Tension
23	*	Tension Arm Assembly
24	*	Reel Motor Assembly
25	*	Belt, Supply Drive
26	*	Belt, Takeup Drive
27	*	File Protect Switch Assembly
28	190-4013-001	Connector PC Board Assembly
29	191-0805-001	Pulley, Reel Drive
30	*	Capstan Motor/Tachometer Assembly
31	*	Read Preamplifier PC Board Assembly

NOTES
1. Specify logo and paint color if different from standard.
2. Order repair kit 198-0100-001 as spare (Table 13-6).

*Indicates replaceable part. For part number, see Replaceable Parts List (Table 13-4).

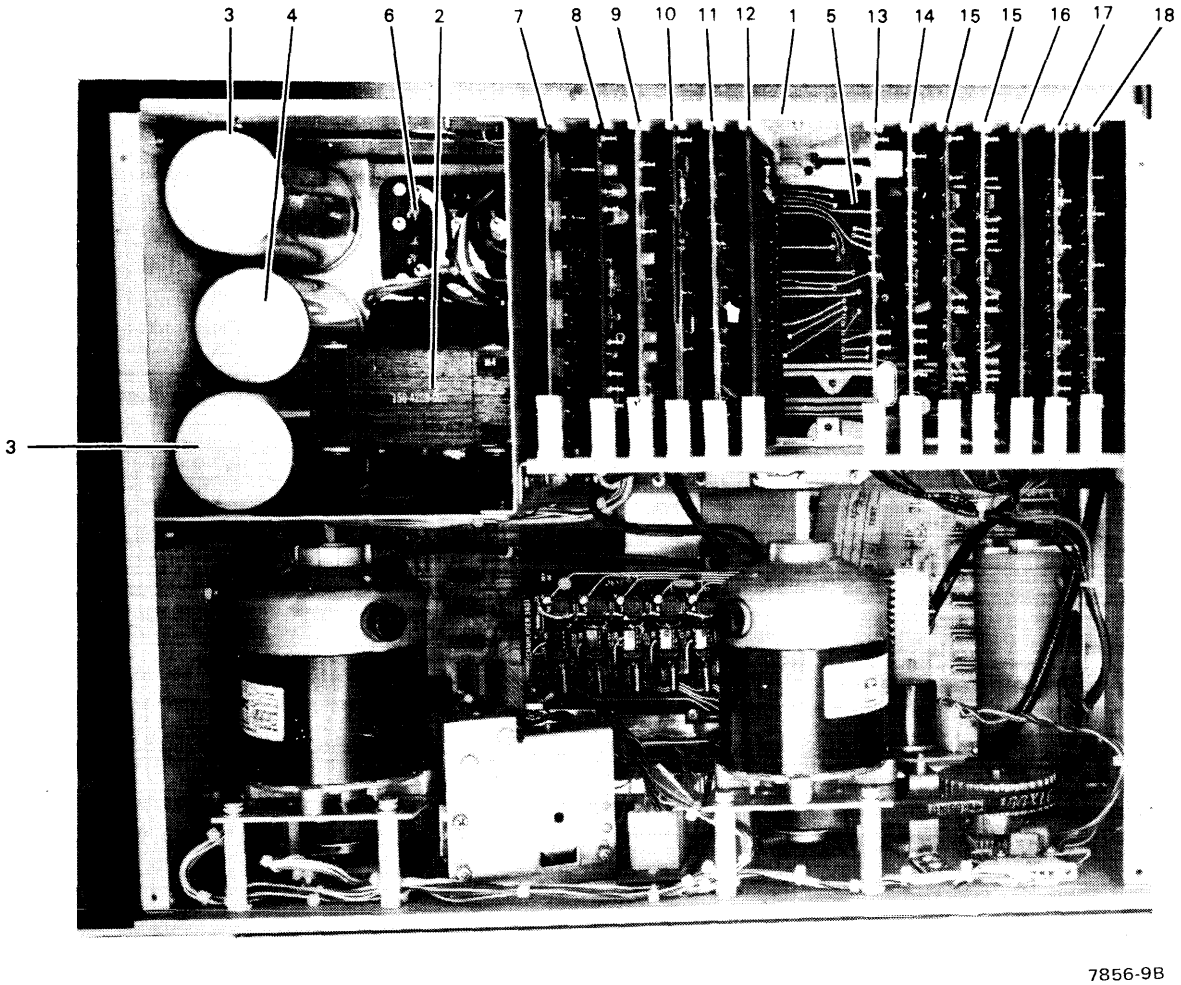


Figure 13-2 Tape Transport Parts Identification (Top View)

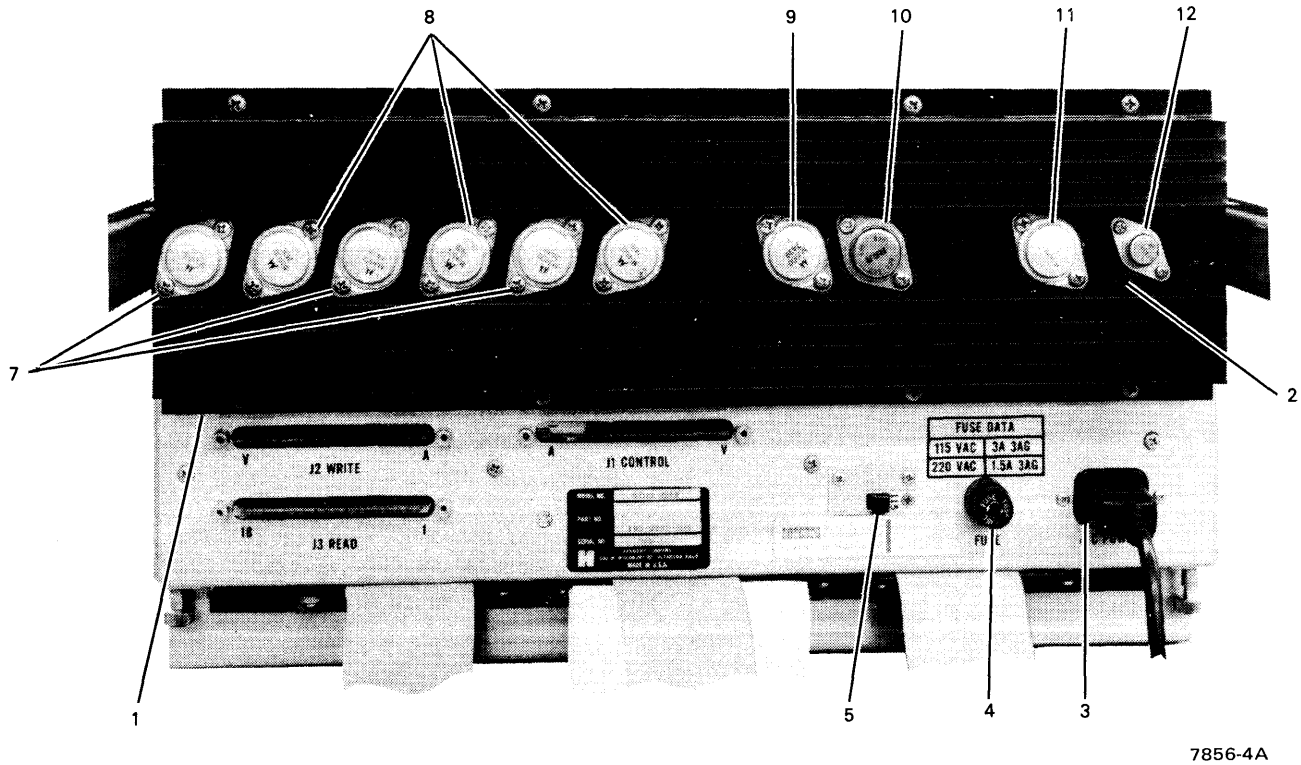


Figure 13-3 Tape Transport Parts Identification (Rear View)

Table 13-2
Illustrated Parts Breakdown for Figure 13-2

Item	Part No.	Description
1	190-4442-001	Power Supply/Card Cage Assembly
2	*	Transformer Assembly
3	*	Capacitor, 18,000 mF/25 V
4	*	Capacitor, 39,000 mF/10 V
5	190-4206-001	Motherboard Assembly
6	*	Rectifier
7	*	Servo Preamplifier Module
8	*	Sensor Amplifier/Driver Module
9	*	Ramp Generator Module
10	*	Pushbutton Control Module
11	*	Control Interface Module
12	190-3841-001	Control Terminator Module
13	*	Delay Timing Module
14	*	Read Amplifier/Clipping Control Module
15	*	Quad Read Amplifier Module
16	190-3860-001	Data Terminator Module
17	*	Four-Channel Write Amplifier Module
18	*	Five-Channel Write Amplifier Module

*Indicates replaceable part. For part number, see Table 13-5.

Table 13-3
Illustrated Parts Breakdown for Figure 13-3

Item	Part No.	Description
1	*	Voltage Regulator/Servo Power Assembly
2	190-4352-001	Voltage Regulator PC Board Assembly (Note 1)
3	127-0003-001	Power Receptacle
4	*	Fuseholder
4	*	Fuse, 3AG, 3 A (115 V operation)
4	*	Fuse, 3AG, 1.5 A (220/230 V operation)
5	*	Switch, 115/220 V
6	*	Power Cord (not shown)
7	148-0122-001	Power Transistor Type MJ802 Motorola (Note 1)
8	148-0121-001	Power Transistor Type MJ4502 Motorola (Note 1)
9	148-0102-003	Power Transistor Type MJ900 Motorola (Note 1)
10	148-0102-004	Power Transistor Type MJ1000 Motorola (Note 1)
11	148-0053-001	Power Transistor Type 2N3055 (Note 1)
12	148-0075-001	Power Transistor Type 2N4910 (Note 1)

NOTES
1. Normally voltage regulator/servo power assembly is replaced as a module. These parts are listed for reference purposes.

*Indicates replaceable part. For part number, see Table 13-6.

Part III

Table 13-4
Replaceable/Spare Parts for Figure 13-1

Item	Part No.	Description	Qty Spare	Note
1	198-4439-001	Control Panel Assembly	1	1
7	198-2771-xxx	Dust Cover Assembly		1
11	198-2605-001	Capstan Wheel	1	
12	198-1509-001	Tape Guide Assembly	2	
14	198-2399-010	Head Assembly, Nine-Track	1	2
14	198-2399-003	Head Assembly, Seven-Track	1	2
15	198-1138-001	Photosensor Assembly, Load Point/EOT	1	
16	198-1139-001	Photosensor Assembly, Broken Tape	1	
17	198-2747-001	Tape Cleaner Assembly	1	
18	198-2647-002	Roller Guide Assembly	1	
20	198-0013-001	Magpot Tension Sensor Assembly (includes Magpot Circuit Module)	1	
22	198-0017-002	Spring, Tension (package of 2)	1	
23	198-2827-001	Tension Arm Assembly		
24	198-4438-001	Reel Motor Assembly	1	
25/ 26	198-0101-001	Belt Kit (1 each supply/takeup)		
27	198-2641-001	File Protect Switch Assembly		
30	198-2484-001	Capstan Motor Assembly	1	3
31	198-3631-xxx	Read Preamplifier Printed Circuit Board Assembly	1	3

NOTES

1. Unless specified, control panels and dust covers will be shipped with standard paint colors. If special paint or logo is required, please specify.

2. Head is supplied on mounting plate and with face shield and connector. Specify number of tracks. All heads are read after write with side mounted erase. Deskew chart is furnished with each head.

3. Capstan motor/tachometer assembly is supplied with capstan wheel in case of damage to capstan in removal.

4. Assembly varies with speed of machine. Please specify when ordering.

5. Delay timing module version varies with machine specifications. Consult card identification strip or schematic section for module type required.

6. Heat sink assembly includes regulation module 190-4352-001. This module is not readily replaceable without replacing heat sink.

7. Repair kit contains those items subject to wear.

Table 13-5
Replaceable/Spare Parts for Figure 13-2

Item	Part No.	Description	Qty Spare	Note
2	198-4474-601	Transformer Assembly		
3	198-3625-199	Capacitor, Electrolytic, 18,000 mF, 25 V min		
4	198-3610-449	Capacitor, Electrolytic, 39,000 mF, 10 V min		
6	198-0108-001	Rectifier, MR751, Motorola (package of 6)		
7	198-4306-xxx	Servo Preamplifier Module	1	4
8	198-3844-001	Sensor Amplifier/Driver Module	1	
9	198-3194-xxx	Ramp Generator Module	1	4
10	198-3843-001	Pushbutton Control Module	1	
11	198-3842-001	Control Interface Module	1	
13	198-4845-xxx	Delay Timing Module (9-track, special)	1	4, 5
14	198-4179-xxx	Read Amplifier/Clipping Level Module	1	4
15	198-4178-xxx	Quad Read Amplifier Module	1	4
17	198-3848-001	Four-Channel Write Amplifier Module	1	
18	198-3849-001	Five-Channel Write Amplifier Module	1	

Table 13-6
Replaceable/Spare Parts for Figure 13-3

Item	Part No.	Description	Qty Spare	Note
1	198-4441-001	Voltage Regulator/Servo Power Assembly	1	6
4	198-0802-001	Fuse Holder		
	198-0133-030	Fuse 3AG, 3 A (115 V) (box of 5)	1	
	198-0133-015	Fuse 3AG, 1.5 A (230 V) (box of 5)	1	
5	198-5001-103	Switch, 115/220 V		
6	198-0068-001	Power Cord		
	198-0100-001	Hub Repair Kit	1	7
	198-0102-001	Brush Replacement Kit, Reel Motor (4 brushes)	1	
	198-0103-001	Brush Replacement Kit, Capstan Motor (2 brushes)	1	

APPENDIX A
TM8-E/TS03 CONTROL TEST, PART 1

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                    IDENTIFICATION
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PRODUCT CODE:   MAINDEC-08-DHTSA-A-D

PRODUCT NAME:   TM8-E/TS03 CONTROL TEST PART 1

DATE CREATED:   21 JUNE 75

MAINTAINER:     DIAGNOSTIC GROUP

AUTHOR:         R. B. BARNES
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NOTE

THERE ARE FIVE DIAGNOSTIC PROGRAMS ASSOCIATED WITH THE TM8-E/TS03 DECMAGTAPE CONTROL AND ITS TRANSPORT SYSTEM. ALTHOUGH PHYSICALLY SEPARATE, THESE PROGRAMS MUST BE TREATED AS A LARGE INTEGRATED TEST, AND TO ENSURE PROPER SYSTEM OPERATION, THESE TESTS MUST BE EXECUTED IN THE ORDER DELINEATED BELOW.

IF A GIVEN TEST SHOULD FAIL AND IT APPEARS THAT A FIX HAS BEEN FOUND, ALL PROGRAMS MUST ONCE AGAIN BE RUN. ONLY WHEN ALL TESTS HAVE RUN WITHOUT ANY UNACCEPTABLE ERRORS CAN THE TM8-E/TS03 SYSTEM BE CONSIDERED UP.

TM8-E DIAGNOSTIC PROGRAMS' ORDER OF EXECUTION

1. TM8-E/TS03 CONTROL TEST PART 1 (MAINDEC-08-DHTSA)
2. TM8-E/TS03 CONTROL TEST PART 2 (MAINDEC-08-DHTSB)
3. TM8-E/TS03 DRIVE FUNCTION TIMER (MAINDEC-08-DHTSE)
4. TM8-E/TS03 DATA RELIABILITY 9 TRACK (MAINDEC-08-DHTSC) (IF 4K SYSTEM)
5. TM8-E/TS03 MULTIDRIVE DATA EXERCISER (MAINDEC-08-DHTSD) (IF 8K OR LARGER SYSTEM)

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1. ABSTRACT

THE TM8-E/TSØ3 CONTROL TEST PART 1 IS AN INTEGRATED SERIES OF SUB-TESTS DESIGNED TO AID IN THE CHECKOUT AND MAINTENANCE OF THE TM8-E DECMAGTAPE CONTROL WITHOUT DEPENDENCE ON TRANSPORT SYSTEM USE. VERSATILITY OF USEAGE IS AFFORDED THROUGH A MODEST KEYBOARD MONITOR AND SWITCH REGISTER CONTROL OPTIONS.

THIS PROGRAM CONSISTS OF 12 MAJOR TESTS (TEST Ø1 THROUGH TEST 14) EACH OF WHICH CONSISTS OF A NUMBER OF SUBTESTS DESIGNATED BY THE LETTERS A THROUGH Z.

2. REQUIREMENTS

2.1 HARDWARE

PDP-8/E, 8/M, 8/F
TELETYPE OR COMPATIBLE DEVICE (TTY)
TM8-E DECMAGTAPE CONTROL

2.2 MEMORY

THIS PROGRAM REQUIRES 4K OF MEMORY AND MAY RESIDE IN ANY MEMORY FIELD. ALL OF EXISTING MEMORY IS USED
TO TEST THE ABILITY OF THE TM8-E TO ADDRESS CORRECTLY DURING DMA TRANSFERS.

2.3 PRELIMINARY PROGRAMS

ALL PROCESSOR/MEMORY DIAGNOSTICS

(PAGE 2)

3. CONVENTIONS

IN THE DESCRIPTION OF ANY KEYBOARD COMMANDS GIVEN IN THIS MANUAL, THE BACK ARROW (←) CORRESPONDS TO DEPRESSING THE RETURN KEY, AND THE NUMBER SIGN (#) CORRESPONDS TO DEPRESSING THE LINE-FEED KEY.

THE PROGRAM PRINTS A LEFT BRACKET ([) WHEN IT IS READY TO ACCEPT A KEYBOARD COMMAND.

4. PROGRAM LOADING PROCEDURE

LOAD THE PROGRAM INTO ANY DESIRED MEMORY FIELD USING THE STANDARD BINARY LOADER TECHNIQUE.

5. PROGRAM STARTING PROCEDURE

A. LOAD ADDRESS 0200.

B. LOAD THE EXTENDED ADDRESS WITH THE PROGRAM FIELD.

C. SET THE SR TO 4000.

D. DEPRESS CLEAR, THEN CONTINUE.

E. THE PROGRAM WILL PRINT ITS TITLE AND MAINDEC NUMBER, THEN ASK "EXTENDED MEMORY?(0-7)". TYPE THE NUMBER OF THE HIGHEST EXISTING MEMORY FIELD. THEN THE PROGRAM MONITOR WILL ASSUME CONTROL. GO TO THE STANDARD TEST PROCEDURE IN PARAGRAPH 6.

NOTE: THE PROGRAM MAY BE RESTARTED AT ANY TIME AT ADDRESS 0201. IN THIS CASE THE PROGRAM BYPASSES ALL PROGRAM INITIALIZATION AND GOES DIRECTLY TO THE PROGRAM MONITOR TO ACCEPT KEYBOARD COMMANDS.

(PAGE 3)

6. STANDARD TEST PROCEDURE

USE OF THE STANDARD TEST PROCEDURE ENSURES PROPER TM8-E CHECKOUT. ANY ERROR OCCURRENCE RESULTS IN AN ERROR REPORT ON THE TTY AND IN A RETURN TO THE PROGRAM MONITOR. ALL OPTIONAL TEST PROCEDURES AFFORDED BY PROGRAM MONITOR AND SWITCH REGISTER CONTROL ARE DESCRIBED IN PARAGRAPH 7. ERROR RECOVERY PROCEDURES AND RELATED INFORMATION ARE GIVEN IN PARAGRAPH 8.

ACCOMPLISH THE FOLLOWING STEPS.

A. START THE PROGRAM AS DESCRIBED IN PARAGRAPH 5.

B. IF A TS03 TRANSPORT SYSTEM IS CONNECTED, ENSURE THAT ALL DRIVES ARE OFF LINE. ALL LEVELS INPUT FROM THE TS03 TO THE TM8-E SHOULD BE AT A "HIGH" LEVEL.

C. SET THE SR=0001.

D. TYPE "TA<" WHICH RESULTS IN THE EXECUTION OF TEST 01 THROUGH TEST 14. SEVERAL PASSES WILL BE MADE OF EACH TEST.

E. AFTER ALL TESTS HAVE BEEN EXECUTED, THE PROGRAM WILL PRINT "PASS 0001". THEN ANOTHER PASS IS AUTOMATICALLY STARTED.

F. ALLOW THE PROGRAM TO RUN FOR AT LEAST 2 PASSES. EACH PASS TAKES APPROXIMATELY 15 MINUTES.

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7. PROGRAM CONTROLS

THE FOLLOWING SUBPARAGRAPHS DESCRIBE THOSE CONTROLS WHICH THE USER HAS OVER THE PROGRAM.

THERE ARE TWO MAIN SOURCES OF PROGRAM CONTROL: A) PROGRAM MONITOR CONTROL VIA KEYBOARD COMMANDS; AND B) SWITCH REGISTER CONTROL.

7.1 PROGRAM MONITOR CONTROL VIA KEYBOARD COMMANDS

THE PROGRAM MONITOR KEYBOARD COMMANDS ARE DESCRIBED BELOW. IF A COMMAND ERROR IS DETECTED, MONITOR PRINTS "?" AND THE COMMAND MUST BE RETYPED. COMMANDS MAY BE INPUT AFTER MONITOR HAS PRINTED A LEFT BRACKET ([). THE TEST INTERRUPT COMMAND MAY BE TYPED AT ANY TIME.

THE PROGRAM MONITOR IS ENTERED UNDER ANY OF THE FOLLOWING CONDITIONS.

A. AFTER PROGRAM STARTUP WITH SR Ø=1, OR A RESTART AT Ø2Ø1.

B. AN ERROR OCCURS AND SR_2=Ø.

C. ALL SELECTED TESTS ARE DONE.

D. THE TEST INTERRUPT COMMAND (REFERENCE PARAGRAPH 7.1.3) IS TYPED BY THE USER.

7.1.1 TEST SELECTION COMMANDS

THE FOLLOWING COMMANDS ARE USED TO SELECT FROM ONE TO TWELVE TESTS FOR EXECUTION. REGARDLESS OF THE ORDER IN WHICH A TEST SELECTION IS MADE, THOSE TESTS ARE EXECUTED IN NUMERICAL ORDER. IF A GIVEN TEST IS SPECIFIED TWICE IN THE SAME SELECTION, IT WILL BE DELETED FROM THAT SELECTION.

COMMAND	RESULT
TA↵	RUN ALL TESTS (TEST Ø1 THROUGH TEST 14)
TØ1T1ØTNN↵	RUN THE TEST(S) INDICATED. TØ1 THROUGH T14 IN OCTAL ARE THE VALID SELECTIONS. IF THE USER SELECTS OTHER THAN TØ1 THROUGH T14 THE PROGRAM WILL EXECUTE ONE OF THE VALID TESTS (UNDETERMINED).

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7.1.2 TEST CONTINUATION COMMANDS

THE FOLLOWING COMMANDS ARE USED TO CONTINUE IN THE TEST SEQUENCE IF THAT SEQUENCE HAS BEEN INTERRUPTED BY AN ERROR WITH SR2=0.

COMMAND	RESULT
C↵	CONTINUE IN THE TEST SEQUENCE. IF NO TESTS ARE SELECTED, MONITOR WILL PRINT "?". IF THIS OCCURS A NEW TEST SELECTION MUST BE MADE.
EX↵	CONTINUE WITH THE NEXT SUBTEST IF THE CURRENT SUBTEST IS FAILING AND SEVERAL SETS OF DATA REMAIN TO BE USED IN THAT SUBTEST. THIS COMMAND ENABLES THE USER TO EXIT A FAILING DATA SUBTEST AND CONTINUE WITH THE NEXT SUBTEST. AFTER THE CURRENT "EX↵" COMMAND HAS BEEN UTILIZED FOR A FAILING DATA SUBTEST EXIT, IT IS NO LONGER EFFECTIVE. IF NO TESTS ARE SELECTED, MONITOR WILL PRINT "?". IN THIS CASE A NEW TEST SELECTION MUST BE MADE.

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7.1.3 TEST INTERRUPT COMMAND

THE FOLLOWING COMMAND MAY BE USED TO INTERRUPT TESTING AND RETURN TO THE PROGRAM MONITOR.

COMMAND	RESULT
ALTMODE KEY	INTERRUPT TEST EXECUTION, RESPONDS TO "ALT" AND "ESC" KEYS. TEST SELECTION IS UNAFFECTED.

7.1.4 MISCELLANEOUS COMMANDS

COMMAND	RESULT
TR	TRACE THE PROGRAM FLOW USING THE ERROR REPORT FORMAT (MODIFIED). THIS COMMAND IS A PREFIX TO ALL "TEST SELECTION" AND "TEST CONTINUATION" COMMANDS, AND RESULTS IN A MODIFIED ERROR REPORT FOR EACH SUBTEST THAT PASSES. TRACE REPORTS ARE CONTROLLED VIA SR BITS 3 AND 4 IN THE SAME MANNER AS ERROR REPORTS. "TR" REMAINS IN EFFECT UNTIL THE NEXT ENTRY TO THE PROGRAM MONITOR.
DMNNNN↵	DUMP THE CONTENTS OF MEMORY LOCATION NNNN IN FIELD M ON THE TTY. LINE-FEED DUMPS THE CONTENTS OF THE NEXT LOCATION; CARRIAGE RETURN RETURNS TO THE PROGRAM MONITOR. TEST SELECTION IS UNAFFECTED.

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7.2 SWITCH REGISTER CONTROL OPTIONS

SR BIT	STATE	FUNCTION
0	0	RUN ALL TESTS NORMALLY.
	1	QUICK VERIFY (ONE PASS IS MADE OF EACH SELECTED TEST).
1	0	ENABLE TEST IN PROGRESS REPORTS. AS SOON AS A TEST IS STARTED THE TEST NUMBER (TESTNN) IS PRINTED ON THE TTY.
	1	DISABLE TEST IN PROGRESS REPORTS.
2	0	RETURN TO PROGRAM MONITOR ON ANY ERROR OCCURRENCE.
	1	RETURN TO PROGRAM MONITOR ONLY IF A FATAL ERROR HAS OCCURRED.
3	0	ENABLE ERROR AND TRACE REPORTS.
	1	DISABLE
4	0	ERROR AND TRACE REPORTS INCLUDE APPLICABLE DATA ONLY.
	1	FORCE ERROR AND TRACE REPORTS TO INCLUDE ALL POSSIBLE DATA.
5	0	DISABLE SUBTEST LOOP.
	1	LOOP ON CURRENT SUBTEST. ALL VARIABLE DATA REMAINS CONSTANT.
6-9	0	INHIBIT LOOPS 6-9 RESPECTIVELY.
	1	ENABLE LOOPS 6-9 RESPECTIVELY. LOOPS 6-9 ALLOW THE USER TO LOOP ON A SMALL GROUP OF SUBTESTS WITHIN THE CURRENT TEST THEREBY ENABLING INCREASING THE TESTING FREQUENCY OF A SMALL SET OF FUNCTIONS. THE LISTING MUST BE REFERENCED TO DETERMINE WHICH SUBTESTS ARE INCLUDED IN EACH LOOP. THE END OF EACH LOOP IS MARKED AS "*****LOOP N*****".
10	0	INHIBIT LOOP ON CURRENT TEST (TEST 01 - TEST 14).
	1	ENABLE LOOP ON CURRENT TEST.
11	0	TERMINATE TESTING UPON COMPLETION OF ALL SELECTED TESTS AND DELETE TEST SELECTION.
	1	RUN ALL SELECTED TESTS CONTINUOUSLY. AT THE COMPLETION OF EACH PASS THROUGH THE ENTIRE TEST SELECTION, THE NUMBER OF PASSES EXECUTED (IN OCTAL) IS PRINTED (PASS NNNN).

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8. ERRORS

8.1 ERROR HALTS

THERE ARE NO ERROR HALTS IN THIS PROGRAM. IF AN ERROR SHOULD OCCUR AND SR2=0, THE PROGRAM WILL STOP TESTING AND RETURN TO THE PROGRAM MONITOR TO AWAIT A USER COMMAND. REFER TO PARAGRAPH 7.1 FOR AVAILABLE COMMANDS.

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8.2 ERROR REPORTS

WHEN SR4=Ø, ERROR REPORTS INCLUDE ONLY THAT INFORMATION WHICH APPLIES DIRECTLY TO THE ERROR. IF SR4=1, ALL POSSIBLE INFORMATION IS PRINTED WHETHER APPLICABLE OR NOT. AN EXAMPLE OF A MAXIMUM INFORMATION ERROR REPORT IS SHOWN BELOW.

```
*ERØ1D  PC:0250 I1:6706 I2:6716 GD:0000 BD:7777 OD:7777
WC:1234 CA:2345 CM:0000 FS:0000 MS:0000 DB:0000 AC:0000
```

THE SYMBOLS USED IN THE ERROR REPORTS ARE DEFINED BELOW.

SYMBOL	DEFINITION
*ERNNX	ERROR OCCURRED IN TEST NN, SUBTEST X. (IF NN=ØØ, THE ERROR OCCURRED OUTSIDE OF A FORMAL TEST.)
*FENNX	FATAL ERROR
TR*NNX	TRACE REPORT INDICATOR. NO ERROR OCCURRED BUT TRACE IS ENABLED.
PC:NNNN	ADDRESS IN PROGRAM AT WHICH ERROR WAS DETECTED.
I1:NNNN	OCTAL CODE FOR IOT1 IN A VARIABLE SUBTEST.
I2:NNNN	OCTAL CODE FOR IOT2 IN A VARIABLE SUBTEST.

THE FOLLOWING THREE SYMBOLS ARE FURTHER DEFINED IN THE PROGRAM LISTING IN THE SUBTEST COMMENTS.

GD:NNNN	GOOD TEST VALUE
BD:NNNN	REAL TEST VALUE (BAD)
OD:NNNN	PREVIOUS GOOD TEST VALUE (OLD)

THE FOLLOWING SYMBOLS INDICATE THE CONTENTS OF THE SPECIFIED REGISTER AT THE TIME THE ERROR WAS DETECTED.

WC:NNNN	WORD COUNT REGISTER
CA:NNNN	CURRENT ADDRESS REGISTER
CM:NNNN	COMMAND REGISTER
FS:NNNN	FUNCTION/STATUS REGISTER
MS:NNNN	MAIN STATUS REGISTER
DB:NNNN	DATA BUFFER REGISTER
AC:NNNN	PROCESSOR ACCUMULATOR (VALID ONLY FOR ILLEGAL SKIP ERRORS.)

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8.3 STANDARD ERROR RECOVERY PROCEDURE

THE STANDARD ERROR RECOVERY PROCEDURE ASSUMES THAT THE STANDARD TEST PROCEDURE IS BEING USED; THAT IS, THAT ALL ERROR OCCURRENCES RESULT IN AN ERROR REPORT AND IN A RETURN TO THE PROGRAM MONITOR.

WHEN AN ERROR OCCURS, USE THE FOLLOWING STEPS AS A GUIDE FOR RECOVERY REFERRING TO PARAGRAPH 8.2 FOR ERROR REPORT SYMBOL DEFINITIONS.

A. REFERENCE THE POINT IN THE PROGRAM LISTING INDICATED BY THE "PC:" NUMBER.

B. THE ERROR CODE IN THE LISTING SHOULD MATCH THE CODE IN THE ERROR REPORT (ERNNX OR FENNX).

C. COMMENTED IMMEDIATELY BELOW THE ERROR CODE IN THE LISTING IS AN EXPLANATION OF THE NUMBERS PRINTED AFTER THE GD, BD AND OD SYMBOLS.

D. IN THE IMMEDIATE VICINITY OF THE ERROR CODE AND RELATED SUBTEST A DESCRIPTION OF THE SUBTEST WILL BE FOUND.

E. IF THE ERROR IS FATAL (FENNX), THERE IS NO STANDARD RECOVERY. THE CAUSE OF THE FAILURE MUST BE DETERMINED THROUGH STATIC MEANS.

F. IF THE ERROR IS NON-FATAL (ERNNX), THE USER MAY ELECT TO CONTINUE IN THE TEST SEQUENCE (C+), OR TO ENTER A SUBTEST LOOP AS DESCRIBED BELOW.

8.3.1 SUBTEST LOOPS

TO ENTER A SUBTEST LOOP, CARRY OUT THE FOLLOWING STEPS.

A. SET SR BITS 2, 3 AND 5=1.

B. TYPE "C+".

TO EXIT A SUBTEST LOOP, RESTORE THE SWITCHES TO THEIR NORMAL POSITION.

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9. RESTRICTIONS

NONE.

10. EXECUTION TIME

ONE NORMAL PASS OF ALL TESTS TAKES APPROXIMATELY 15 MINUTES.
A QUICK VERIFY PASS (SR0=1) TAKES ONLY 2 MINUTES.

11. TEST ABSTRACTS

TEST 01 VERIFIES THE EXISTENCE OF THE VARIOUS 670X AND 671X IOT'S EXCEPT RMSR (6714), AND TESTS THE BASIC OPERATION OF ALL TM8-E REGISTERS EXCEPT THE MAIN STATUS AND STATUS PORTION OF THE FUNCTION/STATUS REGISTERS.

TEST 02 IS A WORST CASE DATA TEST. DATA IS LOADED INTO AND READ BACK FROM ALL NON-STATUS REGISTER BITS AND VERIFIED.

TEST 03 VERIFIES THE EXISTENCE OF THE VARIOUS FUNCTIONS (AS FAR AS POSSIBLE WITHOUT A TRANSPORT) BY CHECKING EACH FUNCTION'S AFFECT ON CURRENT ADDRESS AND WORD COUNT INCREMENTING, AS WELL AS VERIFYING THAT DATA IS TRANSFERRED BETWEEN THE CONTROL AND THE PROCESSOR IN THE PROPER DIRECTION DURING DMA TRANSFERS.

TEST 04 TESTS THE ABILITY OF WORD COUNT, CURRENT ADDRESS AND COMMAND REGISTER BITS 6-8 TO INCREMENT PROPERLY.

TEST 05 VERIFIES THAT PROPER DATA TRANSFERS ARE MADE BETWEEN THE DATA BUFFER AND MEMORY IN BOTH DIRECTIONS.

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TEST Ø6 VERIFIES THAT THE CURRENT ADDRESS REFERENCES THE CORRECT MEMORY LOCATION AND THAT COMMAND REGISTER BITS 6-8 REFERENCE THE CORRECT MEMORY FIELD. ALL EXISTING FIELDS ARE UTILIZED IN THIS TEST

TEST Ø7 TESTS THE VARIOUS STATUS BITS TO CONTAIN THE PROPER STATUS AS GOVERNED BY THE "NO TRANSPORT" CONDITION.

TEST 1Ø CHECKS VARIOUS POSITIVE AND NEGATIVE CONDITIONS OF MAG TAPE FLAG, ERROR FLAG, GO BIT, ILLEGAL FUNCTION, READ-COMPARE ERROR AND EMA OVERFLOW ERROR AS A NO TRANSPORT CONDITION WILL ALLOW.

TEST 11 EXERCISES THE IOT'S SKEF AND SKTD UNDER INTERESTING CONDITIONS AS WELL AS OTHER SKIP AND NO SKIP IOT'S IN THE 672X IOT DECODER.

TEST 12 CHECKS THE UNIQUENESS OF INTERRUPTS AS CAUSED BY MAG TAPE FLAG AND THE ERROR FLAG.

TEST 13 VERIFIES THE UNIQUENESS OF ALL 672X IOT'S IN RELATION TO CLF AND SBRM.

TEST 14 COMPLETELY TESTS THE PROPER OPERATION OF THE READ-COMPARE LOGIC.

12. LISTING (ATTACHED)

APPENDIX B
TM8-E/TS03 CONTROL TEST, PART 2

IDENTIFICATION

PRODUCT CODE: MAINDEC-ØB-DHTSB-A-D

PRODUCT NAME: TM8-E/TSØ3 CONTROL TEST PART 2

DATE CREATED: 15 JUNE 75

MAINTAINER: DIAGNOSTIC GROUP

AUTHOR: R. B. BARNES

NOTE

THERE ARE FIVE DIAGNOSTIC PROGRAMS ASSOCIATED WITH THE TM8-E DECMAGTAPE CONTROL AND ITS TRANSPORT SYSTEM. ALTHOUGH PHYSICALLY SEPARATE, THESE PROGRAMS MUST BE TREATED AS A LARGE INTEGRATED TEST, AND TO ENSURE PROPER SYSTEM OPERATION, THESE TESTS MUST BE EXECUTED IN THE ORDER DELINEATED BELOW.

IF A GIVEN TEST SHOULD FAIL AND IT APPEARS THAT A FIX HAS BEEN FOUND, ALL PROGRAMS MUST ONCE AGAIN BE RUN. ONLY WHEN ALL TESTS HAVE RUN WITHOUT ANY UNACCEPTABLE ERRORS CAN THE TM8-E SYSTEM BE CONSIDERED UP.

TM8-E/TS.3 DIAGNOSTIC PROGRAMS' ORDER OF EXECUTION
---

1. TM8-E/TS03 CONTROL TEST PART 1 (MAINDEC-08-DHTSA)
2. TM8-E/TS03 CONTROL TEST PART 2 (MAINDEC-08-DHTSB)
3. TM8-E/TS03 DRIVE FUNCTION TIMER (MAINDEC-08-DHTSE)
4. TM8-E/TS03 DATA RELIABILITY 9 TRACK (MAINDEC-08-DHTSC)
5. TM8-3/TS03 MULTIDRIVE DATA EXERCISER (MAINDEC-08-DHTSD)

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1. ABSTRACT

THE TM8-E CONTROL TEST PART 2 IS AN INTEGRATED SERIES OF SUB-TESTS DESIGNED TO AID IN THE CHECKOUT AND MAINTENANCE OF THE TM8-E DECMAGTAPE CONTROL AND TSØ3 MASTER/SLAVE TRANSPORT SYSTEM. VERSATILITY OF USEAGE IS AFFORDED THROUGH A MODEST KEYBOARD MONITOR AND SWITCH REGISTER CONTROL OPTIONS.

THIS PROGRAM CONSISTS OF 12 MAJOR TESTS (TEST 15 THROUGH TEST 3Ø) EACH OF WHICH CONSISTS OF A NUMBER OF SUBTESTS DESIGNATED BY THE LETTERS A THROUGH Z. THESE TESTS PROGRESS FROM THE FUNCTIONS TESTED IN THE TM8-E CONTROL TEST PART 1 AND REQUIRE A TSØ3 TRANSPORT SYSTEM TO BE ON LINE FOR PROPER EXECUTION.

2. REQUIREMENTS

2.1 HARDWARE

PDP-8/E, 8/M, 8/F
TELETYPE OR COMPATIBLE DEVICE (TTY)
TM8-E DECMAGTAPE CONTROL
TSØ3 MASTER/SLAVE TRANSPORT SYSTEM

2.2 MEMORY

THIS PROGRAM REQUIRES 4K OF MEMORY AND MAY RESIDE IN ANY MEMORY FIELD.

2.3 PRELIMINARY PROGRAMS

ALL PROCESSOR/MEMORY DIAGNOSTICS
TM8-E CONTROL TEST PART 1

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3. CONVENTIONS

IN THE DESCRIPTION OF ANY KEYBOARD COMMANDS GIVEN IN THIS MANUAL, THE BACK ARROW (←) CORRESPONDS TO DEPRESSING THE RETURN KEY, AND THE NUMBER SIGN (#) CORRESPONDS TO DEPRESSING THE LINE-FEED KEY. A LETTER PRECEDED BY AN UP ARROW (↑) SHOULD BE TYPED WITH THE "CTRL" KEY DEPRESSED. THE PROGRAM PRINTS A LEFT BRACKET ([) WHEN IT IS READY TO ACCEPT A KEYBOARD COMMAND.

WHEN THE PROGRAM PRINTS:

SETUP DRV N (N TRK)

THE OPERATOR MUST ENSURE THAT THE FOLLOWING STEPS ARE CARRIED OUT.

A. MOUNT A SPARE REEL OF INDUSTRY COMPATIBLE MAGNETIC TAPE ON THAT DRIVE WITH THE FILE PROTECT RING IN PLACE (WRITE ENABLED).

B. LOAD THE TAPE AND POSITION AT BOT.

C. SET THE DRIVE SELECTOR SWITCH TO THE CORRECT DRIVE POSITION.

D. SWITCH THAT DRIVE ON LINE.

E. ENSURE THAT ALL OTHER DRIVES ARE OFF LINE.

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4. PROGRAM LOADING PROCEDURE

LOAD THE PROGRAM INTO ANY DESIRED MEMORY FIELD USING THE STANDARD BINARY LOADER TECHNIQUE.

5. PROGRAM STARTING PROCEDURE

A. LOAD ADDRESS 0200.

B. LOAD THE EXTENDED ADDRESS WITH THE PROGRAM FIELD.

C. CLEAR ALL SWITCHES.

D. DEPRESS CLEAR, THEN CONTINUE.

E. THE PROGRAM WILL PRINT ITS TITLE AND MAINDEC NUMBER, THEN ASK FOR DRIVE SELECTION. PRIOR TO MAKING DRIVE SELECTION, GO TO THE STANDARD TEST PROCEDURE IN PARAGRAPH 6.

NOTE: THE PROGRAM MAY BE RESTARTED AT ANY TIME AT ADDRESS 0201. IN THIS CASE THE PROGRAM BYPASSES ALL PROGRAM INITIALIZATION AND GOES DIRECTLY TO THE PROGRAM MONITOR TO ACCEPT KEYBOARD COMMANDS.

6. STANDARD TEST PROCEDURE

USE OF THE STANDARD TEST PROCEDURE ENSURES PROPER TM8-E/TS03 CHECKOUT. ANY ERROR OCCURRENCE RESULTS IN AN ERROR REPORT ON THE TTY AND IN A RETURN TO THE PROGRAM MONITOR. ALL OPTIONAL TEST PROCEDURES AFFORDED BY PROGRAM MONITOR AND SWITCH REGISTER CONTROL ARE DESCRIBED IN PARAGRAPH 7. ERROR RECOVERY PROCEDURES AND RELATED INFORMATION ARE GIVEN IN PARAGRAPH 8.

6.1 DRIVE SELECTION

TO SPECIFY THE DRIVE TO BE TESTED, CARRY OUT THE FOLLOWING STEPS.

A. EITHER START THE PROGRAM AT 0200 AS DESCRIBED IN PARAGRAPH 5, OR WITH THE PROGRAM MONITOR IN CONTROL TYPE "I+".

B. RESPOND TO "DRIVE?" BY TYPING THE DRIVE NUMBER (0-7).

C. RESPOND TO "7 OR 9 TRACK?" BY TYPING "7" OR "9".

D. TAKE THE ACTION DESCRIBED IN PARAGRAPH 3 TO "SETUP DRV N (N TRK)".

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6.2 TEST PROCEDURE

THE FOLLOWING STEPS ARE TO BE ACCOMPLISHED FOR EACH DRIVE IN THE SYSTEM UNDER TEST.

A. SELECT THE DRIVE UNDER TEST AS DRIVE Ø AND ACCOMPLISH THE SETUP (REFER TO 6.1).

B. SET THE SWITCH REGISTER (SR) TO ØØØØ.

C. TYPE "TA←" WHICH RESULTS IN THE EXECUTION OF TEST 15 THROUGH TEST 3Ø. SEVERAL PASSES WILL BE MADE OF EACH TEST WITH THE EXCEPTION OF TEST 3Ø. DURING TEST 3Ø FOLLOW THE DIRECTIONS AS PRINTED BY THE PROGRAM. WHEN EACH STEP HAS BEEN CARRIED OUT, TYPE "C←" TO CONTINUE IN THE TEST.

D. WHEN ALL TESTS ARE COMPLETED, "SELECTED TESTS DONE" WILL BE PRINTED AND THE PROGRAM MONITOR WILL BE READY TO ACCEPT A NEW COMMAND.

E. USING THE SAME DRIVE, SELECT THAT DRIVE AS DRIVE 1 (REFER TO 6.1).

F. SET THE SR TO ØØØØ.

G. TYPE "TAX←" WHICH RESULTS IN THE EXECUTION OF TEST 15 THROUGH TEST 27. ONLY ONE PASS WILL BE MADE OF EACH TEST.

H. WHEN ALL TESTS ARE COMPLETED, "SELECTED TESTS DONE" WILL BE PRINTED AND THE PROGRAM MONITOR WILL BE READY TO ACCEPT A NEW COMMAND.

I. USING THE SAME DRIVE, EXECUTE STEPS E THROUGH H WITH THAT DRIVE SELECTED AS DRIVE 2, 3, 4, 5, 6 AND 7.

J. FOR EACH ADDITIONAL DRIVE ON THE SYSTEM REPEAT STEPS A THROUGH I.

7. PROGRAM CONTROLS

THE FOLLOWING SUBPARAGRAPHS DESCRIBE THOSE CONTROLS WHICH THE USER HAS OVER THE PROGRAM.

THERE ARE TWO MAIN SOURCES OF PROGRAM CONTROL: A) PROGRAM MONITOR CONTROL VIA KEYBOARD COMMANDS; AND B) SWITCH REGISTER CONTROL.

7.1 PROGRAM MONITOR CONTROL VIA KEYBOARD COMMANDS

THE PROGRAM MONITOR KEYBOARD COMMANDS ARE DESCRIBED BELOW. IF A COMMAND ERROR IS DETECTED, MONITOR PRINTS "?" AND THE COMMAND MUST BE RETYPED. COMMANDS MAY BE INPUT AFTER MONITOR HAS PRINTED A LEFT BRACKET ([). TEST INTERRUPT COMMANDS MAY BE TYPED AT ANY TIME.

THE PROGRAM MONITOR IS ENTERED UNDER ANY OF THE FOLLOWING CONDITIONS.

A. AFTER PROGRAM STARTUP.

B. AN ERROR OCCURS AND SR_2=Ø.

C. ALL SELECTED TESTS ARE DONE.

D. A TEST INTERRUPT COMMAND (REFERENCE PARAGRAPH 7.1.3) IS TYPED BY THE USER.

7.1.1 TEST SELECTION COMMANDS

THE FOLLOWING COMMANDS ARE USED TO SELECT FROM ONE TO TWELVE TESTS FOR EXECUTION. REGARDLESS OF THE ORDER IN WHICH A TEST SELECTION IS MADE, THOSE TESTS ARE EXECUTED IN NUMERICAL ORDER. IF A GIVEN TEST IS SPECIFIED TWICE IN THE SAME SELECTION, IT WILL BE DELETED FROM THAT SELECTION.

COMMAND	RESULT
TA←	RUN ALL TESTS (TEST 15 THROUGH TEST 3Ø)
TAX←	RUN ALL TESTS EXCEPT TEST 3Ø (MANUAL INTERVENTION TEST)
T15T22TNN←	RUN THE TEST(S) INDICATED. T15 THROUGH T3Ø IN OCTAL ARE THE VALID SELECTIONS. IF THE USER SELECTS OTHER THAN T15 THROUGH T3Ø THE PROGRAM WILL EXECUTE ONE OF THE VALID TESTS (UNDETERMINED).

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7.1.2 TEST CONTINUATION COMMANDS

THE FOLLOWING COMMANDS ARE USED TO CONTINUE IN THE TEST SEQUENCE IF THAT SEQUENCE HAS BEEN INTERRUPTED BY AN ERROR WITH SR2=Ø, OR AS IN THE CASE OF TEST 30 WHERE THE USER MUST CARRY OUT SOME MANUAL INTERVENTION.

COMMAND	RESULT
C↵	CONTINUE IN THE TEST SEQUENCE. IF NO TESTS ARE SELECTED, MONITOR WILL PRINT "?". IF THIS OCCURS A NEW TEST SELECTION MUST BE MADE.
EX↵	CONTINUE WITH THE NEXT SUBTEST IF THE CURRENT SUBTEST IS FAILING AND SEVERAL SETS OF DATA REMAIN TO BE USED IN THAT SUBTEST. THIS COMMAND ENABLES THE USER TO EXIT A FAILING DATA SUBTEST AND CONTINUE WITH THE NEXT SUBTEST. AFTER THE CURRENT "EX↵" COMMAND HAS BEEN UTILIZED FOR A FAILING DATA SUBTEST EXIT, IT IS NO LONGER EFFECTIVE. IF NO TESTS ARE SELECTED, MONITOR WILL PRINT "?". IN THIS CASE A NEW TEST SELECTION MUST BE MADE.
SNN↵	MINI SCOPE LOOP. THIS COMMAND SHOULD BE USED ONLY WHEN AN ERROR HAS OCCURRED IN A SUBTEST WHICH TESTS TIME SEQUENCED OPERATIONS. "NN" IS THE BIT NUMBER (IN OCTAL) IN THE ERROR STATUS WORD (ERSTAT) WHICH INDICATES A FAILURE. SR5 MUST BE SET TO A 1 TO UTILIZE THIS FEATURE CORRECTLY. REFER TO PARAGRAPH 8 FOR MORE INFORMATION.

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7.1.3 TEST INTERRUPT COMMANDS

THE FOLLOWING COMMANDS MAY BE USED TO INTERRUPT TESTING AND RETURN TO THE PROGRAM MONITOR. IN MOST CASES, ALL TEST SELECTIONS WILL BE DELETED AND THE USER MUST RESELECT THE TESTS TO BE EXECUTED. THE MOST COMMON USES OF THESE COMMANDS ARE TO REWIND THE SELECTED DRIVE, AND TO EXIT A MINI SCOPE LOOP.

COMMAND	RESULT
ALTMODE KEY	INTERRUPT TEST EXECUTION. RESPONDS TO "ALT" AND "ESC" KEYS.
↑R	INTERRUPT TEST EXECUTION, DELETE ALL TEST SELECTIONS, AND REWIND THE SELECTED DRIVE TO BOT.
↑C	INTERRUPT TEST EXECUTION, DELETE ALL TEST SELECTIONS, AND FORCE A DUMP OF ALL TM8-E REGISTERS ON THE TTY. (THE REGISTER DUMP FORMAT IS A MODIFIED ERROR REPORT FORMAT.)

7.1.4 MISCELLANEOUS COMMANDS

COMMAND	RESULT
I↵	INITIALIZE AND ALLOW NEW DRIVE SELECTION.
TR	TRACE THE PROGRAM FLOW USING THE ERROR REPORT FORMAT (MODIFIED). THIS COMMAND IS A PREFIX TO ALL "TEST SELECTION" AND "TEST CONTINUATION" COMMANDS, AND RESULTS IN A MODIFIED ERROR REPORT FOR EACH SUBTEST THAT PASSES. TRACE REPORTS ARE CONTROLLED VIA SR BITS 3 AND 4 IN THE SAME MANNER AS ERROR REPORTS. "TR" REMAINS IN EFFECT UNTIL THE NEXT ENTRY TO THE PROGRAM MONITOR.
D*:NNNN↵	DUMP THE CONTENTS OF MEMORY LOCATION NNNN IN FIELD * ON THE TTY. LINE-FEED DUMPS THE CONTENTS OF THE NEXT LOCATION; CARRIAGE RETURN RETURNS TO THE PROGRAM MONITOR. TEST SELECTION IS UNAFFECTED.

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7.2 SWITCH REGISTER CONTROL OPTIONS

SR BIT	STATE	FUNCTION
0	0	RUN ALL TESTS NORMALLY (SEVERAL PASSES OF EACH SELECTED TEST EXCEPT TEST 30).
	1	QUICK VERIFY (ONE PASS IS MADE OF EACH SELECTED TEST).
1	0	ENABLE TEST IN PROGRESS REPORTS. AS SOON AS A TEST IS STARTED THE TEST NUMBER (TESTNN) IS PRINTED ON THE TTY.
	1	DISABLE TEST IN PROGRESS REPORTS.
2	0	RETURN TO PROGRAM MONITOR ON ANY ERROR OCCURRENCE.
	1	RETURN TO PROGRAM MONITOR ONLY IF A FATAL ERROR HAS OCCURRED.
3	0	ENABLE ERROR AND TRACE REPORTS.
	1	DISABLE
4	0	ERROR AND TRACE REPORTS INCLUDE APPLICABLE DATA ONLY.
	1	FORCE ERROR AND TRACE REPORTS TO INCLUDE ALL POSSIBLE DATA.
5	0	DISABLE SUBTEST LOOP.
	1	LOOP ON CURRENT SUBTEST. ALL VARIABLE DATA REMAINS CONSTANT. THIS SWITCH MUST ALSO BE SET TO ENTER A "MINI SCOPE LOOP".
6-9	0	INHIBIT LOOPS 6-9 RESPECTIVELY.
	1	ENABLE LOOPS 6-9 RESPECTIVELY. LOOPS 6-9 ALLOW THE USER TO LOOP ON A SMALL GROUP OF SUBTESTS WITHIN THE CURRENT TEST THEREBY ENABLING INCREASING THE TESTING FREQUENCY OF A SMALL SET OF FUNCTIONS. THE LISTING MUST BE REFERENCED TO DETERMINE WHICH SUBTESTS ARE INCLUDED IN EACH LOOP. THE END OF EACH LOOP IS MARKED AS "*****LOOP N*****".
10	0	INHIBIT LOOP ON CURRENT TEST (TEST 15 - TEST 30).
	1	ENABLE LOOP ON CURRENT TEST.
11	0	TERMINATE TESTING UPON COMPLETION OF ALL SELECTED TESTS AND DELETE TEST SELECTION.
	1	RUN ALL SELECTED TESTS CONTINUOUSLY. AT THE COMPLETION OF EACH PASS THROUGH THE ENTIRE TEST SELECTION, THE NUMBER OF PASSES EXECUTED (IN OCTAL) IS PRINTED (PASS NNNN).

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8. ERRORS

8.1 ERROR HALTS

THERE ARE NO ERROR HALTS IN THIS PROGRAM. IF AN ERROR SHOULD OCCUR AND SR2=Ø, THE PROGRAM WILL STOP TESTING AND RETURN TO THE PROGRAM MONITOR TO AWAIT A USER COMMAND. REFER TO PARAGRAPH 7.1 FOR AVAILABLE COMMANDS.

8.2 ERROR REPORTS

WHEN SR4=0, ERROR REPORTS INCLUDE ONLY THAT INFORMATION WHICH APPLIES DIRECTLY TO THE ERROR. IF SR4=1, ALL POSSIBLE INFORMATION IS PRINTED WHETHER APPLICABLE OR NOT. AN EXAMPLE OF A MAXIMUM INFORMATION ERROR REPORT IS SHOWN BELOW.

```
*ER15D  PC:0250 I1:6706 I2:6716 GD:0000 BD:7777 OD:7777
WC:1234 CA:2345 CM:0000 FS:0000 MS:0000 DB:0000 AC:0000
```

THE SYMBOLS USED IN THE ERROR REPORTS ARE DEFINED BELOW.

SYMBOL	DEFINITION
*ERNNX	ERROR OCCURRED IN TEST NN, SUBTEST X. (IF NN=31, THE ERROR OCCURRED OUTSIDE OF A FORMAL TEST.)
*FENNX	FATAL ERROR
TR*NNX	TRACE REPORT INDICATOR. NO ERROR OCCURRED BUT TRACE IS ENABLED OR THE "^C" COMMAND WAS TYPED BY THE USER.
PC:NNNN	ADDRESS IN PROGRAM AT WHICH ERROR WAS DETECTED.
I1:NNNN	OCTAL CODE FOR IOT1 IN A VARIABLE SUBTEST.
I2:NNNN	OCTAL CODE FOR IOT2 IN A VARIABLE SUBTEST.

THE FOLLOWING THREE SYMBOLS ARE FURTHER DEFINED IN THE PROGRAM LISTING IN THE SUBTEST COMMENTS.

GD:NNNN	GOOD TEST VALUE
BD:NNNN	REAL TEST VALUE (BAD)
OD:NNNN	PREVIOUS GOOD TEST VALUE (OLD)

THE FOLLOWING SYMBOLS INDICATE THE CONTENTS OF THE SPECIFIED REGISTER AT THE TIME THE ERROR WAS DETECTED.

WC:NNNN	WORD COUNT REGISTER
CA:NNNN	CURRENT ADDRESS REGISTER
CM:NNNN	COMMAND REGISTER
FS:NNNN	FUNCTION/STATUS REGISTER
MS:NNNN	MAIN STATUS REGISTER
DB:NNNN	DATA BUFFER REGISTER
AC:NNNN	PROCESSOR ACCUMULATOR (VALID ONLY FOR ILLEGAL SKIP ERRORS.)

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8.3 STANDARD ERROR RECOVERY PROCEDURE

THE STANDARD ERROR RECOVERY PROCEDURE ASSUMES THAT THE STANDARD TEST PROCEDURE IS BEING USED; THAT IS, THAT ALL ERROR OCCURRENCES RESULT IN AN ERROR REPORT AND IN A RETURN TO THE PROGRAM MONITOR.

WHEN AN ERROR OCCURS, USE THE FOLLOWING STEPS AS A GUIDE FOR RECOVERY REFERRING TO PARAGRAPH 8.2 FOR ERROR REPORT SYMBOL DEFINITIONS.

A. REFERENCE THE POINT IN THE PROGRAM LISTING INDICATED BY THE "PC:" NUMBER.

B. THE ERROR CODE IN THE LISTING SHOULD MATCH THE CODE IN THE ERROR REPORT (ERNNX OR FENNX).

C. COMMENTED IMMEDIATELY BELOW THE ERROR CODE IN THE LISTING IS AN EXPLANATION OF THE NUMBERS PRINTED AFTER THE GD, BD AND OD SYMBOLS.

D. IN THE IMMEDIATE VICINITY OF THE ERROR CODE AND RELATED SUBTEST A DESCRIPTION OF THE SUBTEST WILL BE FOUND.

E. IF THE SYMBOLS "GD" AND "BD" ARE DEFINED AS THE GOOD AND REAL (BAD) VALUES OF ERSTAT (ERROR STATUS WORD), THAT SUBTEST TESTS TIME SEQUENCED OPERATIONS. IN THIS CASE, ANY BITS WHICH DIFFER BETWEEN GD AND BD INDICATE WHICH TIME SEQUENCED OPERATION(S) FAILED. THE TIME SEQUENCED OPERATIONS ARE COMMENTED WITH THE BIT POSITION TO WHICH THEY CORRESPOND AND EXACTLY WHAT IS BEING TESTED AT THAT TIME.

F. IF THE ERROR IS FATAL (FENNX), THERE IS NO STANDARD RECOVERY. THE CAUSE OF THE FAILURE MUST BE DETERMINED THROUGH STATIC MEANS.

G. IF THE ERROR IS NON-FATAL (ERNNX), THE USER MAY ELECT TO CONTINUE IN THE TEST SEQUENCE (C+), OR TO ENTER A SUBTEST OR MINI SCOPE LOOP AS DESCRIBED BELOW.

H. IF THE FAILING SUBTEST DOES NOT TEST TIME SEQUENCED OPERATIONS, ENTER A SUBTEST LOOP AS DESCRIBED IN 8.3.1 BELOW.

I. IF THE FAILING SUBTEST DOES TEST TIME SEQUENCED OPERATIONS, THE USER MAY ENTER A SUBTEST LOOP AS DESCRIBED IN 8.3.1 OR A MINI SCOPE LOOP AS DESCRIBED IN 8.3.2.

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8.3.1 SUBTEST LOOPS

TO ENTER A SUBTEST LOOP, CARRY OUT THE FOLLOWING STEPS.

A. SET SR BITS 2, 3 AND 5=1.

B. TYPE "C↵"

TO EXIT A SUBTEST LOOP, RESTORE THE SWITCHES TO THEIR NORMAL POSITION.

8.3.2 MINI SCOPE LOOPS

NOTE: MINI SCOPE LOOPS WILL WORK ONLY FOR SUBTESTS WHICH TEST TIME SEQUENCED OPERATIONS.

TO ENTER A MINI SCOPE LOOP, CARRY OUT THE FOLLOWING STEPS.

A. SET SR BITS 2, 3 AND 5=1.

B. TYPE "SNN↵" WHERE NN IS THE BIT NUMBER (IN OCTAL) OF THE FIRST FAILING TIME SEQUENCED OPERATION. THE PROGRAM WILL LOOP CONTINUOUSLY FROM THE LAST "SET" COMMAND THROUGH THE TIME SEQUENCED OPERATION TEST SPECIFIED IN "SNN↵". A "CLEAR TRANSPORT" (CLT) IS ISSUED AFTER THE COMPLETION OF EACH LOOP.

TO EXIT A MINI SCOPE LOOP, TYPE "↑R" WHICH WILL INTERRUPT THE LOOP, DELETE ALL TEST SELECTIONS, REWIND THE SELECTED DRIVE, AND RETURN TO THE PROGRAM MONITOR.

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9. RESTRICTIONS

ONLY ONE DRIVE MAY BE TESTED AT ONE TIME.
ALL OTHER DRIVES MUST BE OFF LINE.

10. EXECUTION TIME

EXECUTION TIME VARIES DEPENDENT UPON THE TYPE OF DRIVE BEING TESTED. ONE LONG PASS OF A FULL TEST SELECTION FOR A 9 TRACK DRIVE TAKES APPROXIMATELY 15 MINUTES.

11. TEST ABSTRACTS

TEST 15 CHECKS BASIC TM8-E CONTROL FUNCTIONS THAT DO REQUIRE A DRIVE TO BE ON LINE. NO TAPE MOTION, HOWEVER, IS INITIATED.

TEST 16 CHECKS TIME SEQUENCED CONDITIONS INCLUDING TAPE MOTION FOR WRITE, READ, READ-COMPARE, SPACE FORWARD, SPACE REVERSE AND REWIND FUNCTIONS. ALL OPERATIONS ARE DONE AT 800 BPI WITH 9 TRACK DRIVES IN CORE DUMP MODE.

TEST 17 VERIFIES THAT RECORDS WRITTEN IN ONE PARITY MODE, THEN READ IN THE OTHER MODE CAUSE LATERAL (VERTICAL) PARITY ERRORS.

TEST 20 VERIFIES THE ABILITY OF THE DRIVE TO WRITE A FILE MARK AND ALSO THE ABILITY TO RECOGNIZE A FILE MARK.

TEST 21 EXERCISES VARIOUS COMBINATIONS OF WRITE, WRITE FILE MARK AND SPACE REVERSE.

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TEST 22 CONTINUES VARIOUS POSITIVE AND NEGATIVE TESTING SEQUENCES ON THE TM8-E CONTROL UTILIZING TAPE MOTION.

TEST 23 VERIFIES THE PROPER OPERATION OF THE CONTINUOUS MODE OF SINGLE DRIVE OPERATION UTILIZING VARIOUS COMBINATIONS OF DRIVE FUNCTIONS.

TEST 24 TESTS THE CHANGE DIRECTION MODE OF OPERATION UTILIZING VARIOUS COMBINATIONS OF FUNCTIONS WHICH CAUSE DIRECTION REVERSAL.

TEST 25 IS A BASIC TEST OF THE ABILITY OF THE TM8-E/TS03 TO PASS DATA CORRECTLY.

TEST 26 VERIFIES THE PROPER GENERATION OF THE CYCLIC REDUNDANCY CHECK CHARACTER (CRCC) BY COMPARING SIMULATED VALUES TO THOSE VALUES GENERATED BY THE HARDWARE AND WRITTEN ON TAPE. THIS TEST IS RUN ON 9 TRACK DRIVES ONLY.

TEST 27 DOES NOT APPLY TO THE TS03*****

TEST 30 IS A MANUAL INTERVENTION TEST WHICH TESTS SUCH THINGS AS FILE PROTECT, THE OFF LINE FUNCTION AND THE PROPER EFFECT ON THE CONTROL BY THE PROCESSOR "INITIALIZE" SIGNAL.

12. LISTING (ATTACHED)

APPENDIX C
TM8-E/TS03 DATA RELIABILITY, 9-TRACK

IDENTIFICATION

PRODUCT CODE: MAINDEC-08-DHTSC-A-D

PRODUCT NAME: TM8-E/TS03 DATA RELIABILITY 9 TRACK

DATE CREATED: 15 JUNE 75

MAINTAINER: DIAGNOSTIC GROUP

AUTHOR: R. B. BARNES

NOTE
****

THERE ARE FIVE DIAGNOSTIC PROGRAMS ASSOCIATED WITH THE TM8-E DECMAGTAPE CONTROL AND ITS TRANSPORT SYSTEM, ALTHOUGH PHYSICALLY SEPARATE, THESE PROGRAMS MUST BE TREATED AS A LARGE INTEGRATED TEST, AND TO ENSURE PROPER SYSTEM OPERATION, THESE TESTS MUST BE EXECUTED IN THE ORDER DELINEATED BELOW.

IF A GIVEN TEST SHOULD FAIL AND IT APPEARS THAT A FIX HAS BEEN FOUND, ALL PROGRAMS MUST ONCE AGAIN BE RUN, ONLY WHEN ALL TESTS HAVE RUN WITHOUT ANY UNACCEPTABLE ERRORS CAN THE TM8-E SYSTEM BE CONSIDERED UP.

TM8-E DIAGNOSTIC PROGRAMS' ORDER OF EXECUTION
---

1. TM8-E/TS03 CONTROL TEST PART 1 (MAINDEC-08-DHTSA)
2. TM8-E/TS03 CONTROL TEST PART 2 (MAINDEC-08-DHTSB)
3. TM8-E/TS03 DRIVE FUNCTION TIMER (MAINDEC-08-DHTSE)
4. TM8-E/TS03 DATA RELIABILITY 9 TRACK (MAINDEC-08-DHTSC) FOR 4K SYSTEMS
5. TM8-E/TS03 MULTIDRIVE DATA EXERCISER (MAINDEC-11-DHTSD) FOR 8K AND LARGER

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WARNING: ANY PROGRAM INTERRUPT THAT OCCURS FROM A DEVICE OTHER THAN THE TM8-E IS A FATAL ERROR AND WILL RESULT IN A PROGRAM HALT.

1. ABSTRACT

THE TM8-E DATA RELIABILITY TEST (9 TRACK) IS PRIMARILY DESIGNED FOR THE COLLECTION OF STATISTICAL INFORMATION PERTAINING TO THE DATA RELIABILITY OF THE 9 TRACK TAPE DRIVES ASSOCIATED WITH THE TM8-E DECMAGTAPE CONTROL. THE PROGRAM IS ALSO DESIGNED TO BE USEABLE AS AN AID IN THE CHECKOUT AND MAINTENANCE OF THE TM8-E AND ASSOCIATED 9 TRACK DRIVES.

THIS PROGRAM MAY ALSO BE USED AS AN EXTENDED DATA RELIABILITY ACCEPTANCE TEST FOR 9 TRACK DRIVES.

ALL TAPE OPERATIONS ARE DONE IN 9 TRACK COMPATIBLE MODE. CORE DUMP MODE IS NOT UTILIZED.

2. REQUIREMENTS

2.1 HARDWARE

PDP-8/E, 8/M, 8/F
TELETYPE OR COMPATIBLE DEVICE (TTY)
TM8-E DECMAGTAPE CONTROL
TS03 MASTER/SLAVE TRANSPORT SYSTEM WITH FROM ONE TO EIGHT 9 TRACK DRIVES.

2.2 MEMORY

THIS PROGRAM REQUIRES 4K OF MEMORY AND MAY RESIDE IN ANY MEMORY FIELD.

2.3 PRELIMINARY PROGRAMS

ALL PROCESSOR/MEMORY DIAGNOSTICS
TM8-E CONTROL TEST PART 1
TM8-E CONTROL TEST PART 2
TM8-E DRIVE FUNCTION TIMER

3. PROGRAM LOADING PROCEDURE

LOAD THE PROGRAM INTO ANY DESIRED MEMORY FIELD USING THE STANDARD BINARY LOADER TECHNIQUE.

4. PROGRAM STARTING PROCEDURE

A. LOAD ADDRESS 0200.

B. LOAD THE EXTENDED ADDRESS WITH THE PROGRAM FIELD.

C. CLEAR ALL SWITCHES.

E. THE PROGRAM WILL PRINT ITS TITLE AND MAINDEC NUMBER, THEN ASK FOR DRIVE SELECTION. PRIOR TO MAKING DRIVE SELECTION GO TO THE STANDARD TEST PROCEDURE IN PARAGRAPH 5.

NOTE: THE PROGRAM MAY BE RESTARTED AT ANY TIME AT ADDRESS 0201. IN THIS CASE THE PROGRAM ASKS IMMEDIATELY FOR DRIVE SELECTION.

5. STANDARD TEST PROCEDURE

USE OF THE STANDARD TEST PROCEDURE RESULTS IN EACH SELECTED TEST SEQUENCE RUNNING FROM BOT TO EOT. NO REPORTS WILL OCCUR WHEN NON-FATAL ERRORS ARE DETECTED, HOWEVER, THESE ERRORS WILL BE ACCUMULATED AND REPORTED AT THE END OF EACH PASS OF TAPE. ANY VARIATIONS FROM THIS SCHEME ARE CONTROLLED THROUGH THE SWITCH REGISTER OPTIONS AS LISTED IN PARAGRAPH 6. ERROR REPORT DESCRIPTIONS AND RELATED INFORMATION ARE GIVEN IN PARGRAPH 7.

5.1 DRIVE SELECTION

ACCOMPLISH THE FOLLOWING STEPS TO SETUP AND SELECT THOSE 9 TRACK DRIVES TO BE TESTED.

A. PLACE A SPARE REEL OF INDUSTRY COMPATIBLE MAGNETIC TAPE WITH THE FILE PROTECT RING IN PLACE (WRITE ENABLED) ON EACH DRIVE TO BE TESTED.

B. LOAD THE TAPE, POSITION TO BOT AND SWITCH THE DRIVE ON LINE.

C. START THE PROGRAM AS DESCRIBED IN PARAGRAPH 4.

D. THE PROGRAM WILL EVENTUALLY PRINT "SELECT DRIVES".

E. TYPE THE DRIVE NUMBERS OF THOSE 9 TRACK DRIVES TO BE TESTED, TYPING THE SAME DRIVE NUMBER TWICE WILL DELETE THAT DRIVE FROM THE SELECTION.

F. WHEN ALL DRIVE NUMBERS HAVE BEEN TYPED IN, TYPE CARRIAGE RETURN.

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5.2 TEST SELECTION

ACCOMPLISH THE FOLLOWING STEPS TO SELECT THE DESIRED TEST SEQUENCES.

A. AFTER DRIVE SELECTION IS COMPLETE, THE PROGRAM WILL PRINT:

"TST PAT PAR DEN RLS WMO RMO"

B. RESPOND BY TYPING THE DESIRED CODE FOR EACH OF THE PARAMETERS USING THE TABLE BELOW AND REFERENCING THE INDICATED PARAGRAPH.

PARAMETER	DEFINITION	REFERENCE PARA.
TST	TEST SEQUENCE	5.2.1
PAT	DATA PATTERN	5.2.2
PAR	PARITY	5.2.3
DEN	DENSITY	5.2.4
RLS	RECORD LENGTH SEQUENCE	5.2.5
WMO	WRITE STOP MODE	5.2.6
RMO	READ STOP MODE	5.2.7

C. AFTER ALL PARAMETERS FOR A SPECIFIED TEST SEQUENCE HAVE BEEN ENTERED, TYPE A SPACE. IF THE SELECTION IS VALID, THE PROGRAM WILL PRINT "O.K.".

D. REPEAT STEPS B AND C FOR ALL DESIRED TEST SEQUENCES.

E. WHEN ALL DESIRED TEST SEQUENCES HAVE BEEN SPECIFIED AND "O.K." HAS BEEN PRINTED BY THE PROGRAM FOR EACH SET OF TEST SEQUENCE PARAMETERS, TYPE CARRIAGE RETURN.

F. THE PROGRAM WILL NOW START EXECUTING THE SELECTED TEST SEQUENCES ON THE DRIVES UNDER TEST.

G. AS EACH TEST SEQUENCE IS COMPLETED ON EACH DRIVE, THE ACCUMULATED ERRORS DETECTED WILL BE REPORTED. REFERENCE PARAGRAPH 7 FOR DETAILS.

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5.2.1 TEST SEQUENCE SELECTION TABLE (TST)

THE FIRST SELECTION MADE IS "TST"
TYPE IN THE NUMBER OF THE TEST DESIRED.

TEST NUMBER	DESCRIPTION
0	WRITE TO EOT ON ONE DRIVE, TYPE ACCUMULATED WRITE ERRORS, CHANGE DRIVES.
1	WRITE ONE RECORD LENGTH SEQUENCE OR 256 RECORDS, CHANGE DRIVES, AS EACH DRIVE REACHES EOT TYPE ACCUMULATED WRITE ERRORS.
2	WRITE ONE RECORD, CHANGE DRIVES, AS EACH DRIVE REACHES EOT TYPE ACCUMULATED WRITE ERRORS.
3	WRITE TO EOT, TYPE ACCUMULATED WRITE ERRORS, REWIND, CHANGE DRIVES, READ TO EOT, TYPE ACCUMULATED READ ERRORS, CHANGE DRIVES.
4	WRITE ONE RECORD LENGTH SEQUENCE, BACKSPACE, READ, CHANGE DRIVES AS EACH DRIVE REACHES EOT TYPE ACCUMULATED WRITE AND READ ERROR INFORMATION.
5	WRITE ONE RECORD, BACKSPACE, READ, CHANGE DRIVES, AS EACH DRIVE REACHES EOT TYPE OUT ACCUMULATED ERROR INFORMATION.
6	WRITE ONE RECORD LENGTH SEQUENCE OR 256 RECORDS, CHANGE DRIVES, BACKSPACE, CHANGE DRIVES, READ, CHANGE DRIVES, AS EACH DRIVE REACHES EOT TYPE ACCUMULATED ERROR INFORMATION.
7	WRITE ONE RECORD, CHANGE DRIVES, BACKSPACE, CHANGE DRIVES, READ, CHANGE DRIVES, AS EACH DRIVE REACHES EOT TYPE ACCUMULATED ERROR INFORMATION.
8	TEST 8 RUNS DIFFERENTLY DEPENDING ON THE WMO AND RMO SELECTION. IF BOTH ARE SELECTED 0 (NONSTOP), EACH WRITE AND READ PASS WILL BE MADE TO THE END OF A RECORD LENGTH SEQUENCE BEFORE CHANGING DRIVES. IF EITHER SELECTION IS START/STOP (1) OR RANDOM (2) THAT PASS WILL BE MADE WITH DRIVE CHANGE BETWEEN EACH RECORD. (I.E., WMO=0 AND RMO=1, THE WRITE PASS IS MADE NONSTOP ON EACH DRIVE TO END OF RLS, THE READ PASS IS MADE START STOP WITH A DRIVE CHANGE BETWEEN EACH RECORD).

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TEST 9 IS A READ ONLY TEST THAT MAY BE USED TO TEST DRIVE COMPATABILITY OR MULTIPLE READ PASSES OVER DATA PREVIOUSLY WRITTEN. EITHER PATTERN 7 (RANDOM DATA) IS NOT A VALID SELECTION FOR TEST 9 EXCEPT WITH CERTAIN RESTRICTIONS.

A. TEST 9 SELECTION FOLLOWS TEST 3.

B. TEST 9 SELECTION FOLLOWS TEST 6 WITH SR0=1

C. TEST 9 SELECTION FOLLOWS TEST 8 WITH SR0=1

D. TEST 9 SELECTION FOLLOWS TEST 5 WITH SR0=1
AND ONLY A SINGLE DRIVE WAS SELECTED.

5.2.2 DATA PATTERN SELECTION TABLE (PAT)

THE SECOND SELECTION IS "PAT".
TYPE IN THE NUMBER OF THE DATA PATTERN DESIRED. USE TABLE "A" IF PARITY SELECTION WILL BE EVEN, TABLE "B" IF PARITY WILL BE ODD.

A. EVEN PARITY DATA PATTERNS

PAT	DATA	DESCRIPTION
0	0014	HIGH FREQUENCY OUTSIDE SKEW
1	0377 0177 0277 0337 0357 0367 0373 0375 0376	SLIDING NO BIT (0) CHARACTER PATTERN
2	0103	HIGH FREQUENCY EVERY OTHER TRACK
3	0273	HALF FREQUENCY OUTSIDE TRACKS HIGH FREQUENCY ALL INSIDE TRACKS
4	0001 0002 0003 0004	INCREMENTING CHARACTER PATTERN NO 00 CODES

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5	0377 0177 0277 0337 0357 0367 0373 0375 0376	THREE 0 BITS EACH TRACK EVERY 7TH WORD
6	0377	ALL 1'S ALL TRACKS
7	RANDOM	RANDOM DATA PATTERN WITH NO 00 CODES

B. ODD PARITY DATA PATTERNS

PAT	DATA	DESCRIPTION
0	0004	HALF FREQUENCY OUTSIDE SKEW
1	0000 0200 0100 0040 0020 0010 0004 0002 0001	SLIDING 1 BIT CHAR- ACTER PATTERN (ISO- LATED BIT)
2	0274	HIGH FREQUENCY EVERY OTHER TRACK
3	0037 0076 0201 0174 0003 0370 0007 0360	THREE 0'S, THREE 1'S, THREE 0'S, THREE 2'S, SIX 0'S EVERY TRACK

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4	0001 0002 0003 0004	INCREMENTING CHARACTER PATTERN 00 CODES INCLUDED
5	0000 0200 0100 0040 0020 0010 0004 0002 0001	EACH TRACK 3 BITS EVERY SEVENTH WORD
6	0377	ALL ONES HIGH FREQUENCY ALL TRACKS
7	RANDOM	RANDOM DATA WORD PATTERN 00 CODES INCLUDED

5.2.3 PARITY SELECTION (PAR)

THE THIRD SELECTION IS "PAR"
SPECIFY PARITY BY TYPING THE DESIRED CODE AS DESCRIBED BELOW.

CODE	PARITY
0	EVEN
1	ODD

5.2.4 DENSITY SELECTION (DEN)

AFTER PARITY HAS BEEN SELECTED, 800 BPI WILL AUTOMATICALLY BE SELECTED AND PRINTED BY THE PROGRAM.

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5.2.5 RECORD LENGTH SEQUENCE SELECTION (RLS)

AFTER THE DENSITY SELECTION SPECIFY THE DESIRED RECORD LENGTH SEQUENCE SELECTION (RLS) BY TYPING THE DESIRED CODE AS DEFINED BELOW.

CODE	RECORD LENGTH SEQUENCE
0	ALL RECORDS ARE 24 WORDS (24 CHARACTERS)
1	ALL RECORDS ARE 4008 WORDS (4008 CHARACTERS)
2	RECORDS PROGRESS FROM 24 WORDS TO 4008 WORDS (MIN TO MAX)
3	RECORDS PROGRESS FROM 4008 WORDS TO 24 WORDS (MAX TO MIN)

5.2.6 WRITE STOP MODE SELECTION (WMO)

AFTER THE RECORD LENGTH SEQUENCE SELECTION, SPECIFY THE APPROPRIATE CODE FOR THE DESIRED WRITE STOP MODE (WMO).

CODE	WRITE STOP MODE
0	NONSTOP,THE NEXT WRITE OPERATION IS INITIATED WITHOUT WAITING FOR TAPE UNIT READY.
1	START/STOP. ALL WRITE OPERATIONS ARE INITIATED AFTER TAPE UNIT READY.
2	RANDOM. COMBINED NONSTOP, START/STOP AND RANDOM STALL OPERATIONS.

5.2.7 READ STOP MODE SELECTION (RMO)

AFTER WRITE STOP MODE SELECTION, SPECIFY THE APPROPRIATE CODE FOR THE DESIRED READ STOP MODE (RMO).

CODE	READ STOP MODE
0	NONSTOP. THE NEXT READ-COMPARE OPERATION IS INITIATED WITHOUT WAITING FOR TAPE UNIT READY.
1	START/STOP. ALL READ-COMPARE OPERATIONS ARE INITIATED AFTER TAPE UNIT READY.
2	RANDOM. COMBINED NONSTOP, START/STOP AND RANDOM STALL READ-COMPARE OPERATIONS.

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6. SWITCH REGISTER CONTROLS

THE FOLLOWING TABLE INDICATES THE CONTROL THE SWITCH REGISTER HAS OVER PROGRAM OPERATION WHEN A PARTICULAR SR BIT IS SET TO THE "1" STATE.

SR BIT	FUNCTION
0	DUMP ERROR COUNTERS AND PROCEED TO NEXT TEST SEQUENCE AT THE END OF ONE RECORD LENGTH SEQUENCE. (256 RECORDS FOR RLS=0 OR 1, ONE MIN TO MAX SEQUENCE FOR RLS=2, OR ONE MAX TO MIN SEQUENCE FOR RLS=3.)
1	DELETE WRITE WITH EXTENDED INTERRECORD GAP. USE OF THIS SWITCH WILL CAUSE RECORDS WITH WRITE ERRORS TO BE LEFT ON TAPE.
2	REPORT ALL WRITE ERRORS AS THEY OCCUR.
3	SELECT WRITE STATISTICAL RECOVERY. USE OF THIS SWITCH WILL SELECT THE BACKSPACE 2 RECORDS, SPACE FORWARD 1 RECORD, REWRITE SEQUENCE. THIS SEQUENCE CAUSES THE SAME RECORD TO BE REWRITTEN ON APPROXIMATELY THE SAME AREA OF TAPE IF A WRITE ERROR OCCURS.
4	REPORT ALL READ-COMPARE STATUS AND DATA ERRORS AS THEY OCCUR.
5	DELETE READ RETRIES. THIS SWITCH IS AN AID TO SCOPING READ CIRCUITS BY DELETING THE BACKSPACE, REREAD TWICE SEQUENCE.
6	INCREMENT PATTERN SELECTION AND REPEAT LAST TEST SEQUENCE. PATTERN SELECTION IS RESET TO ITS ORIGINAL SELECTION AFTER PATTERN 7 HAS BEEN EXERCISED.
7	COMPLEMENT PARITY SELECTION AND REPEAT TEST SEQUENCE IF NEW PARITY SELECTION IS DIFFERENT THAN THE ORIGINAL TEST SEQUENCE.

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8	NO FUNCTION
9	INCREMENT RLS SELECTION TO THE NEXT SEQUENCE, AFTER MAX, TO MIN, HAS BEEN EXERCISED RESET RLS SELECTION TO ITS ORIGINAL TEST SEQUENCE SELECTION,
10	INCREMENT WMO TO THE NEXT STOP MODE, AFTER RANDOM START/STOP HAS BEEN EXERCISED, RESET WMO TO ITS ORIGINAL TEST SELECTION,
11	INCREMENT RMO TO THE NEXT READ STOP MODE, AFTER READ RANDOM START/STOP HAS BEEN EXERCISED, RESET RMO TO ITS ORIGINAL TEST SELECTION,

7. ERROR REPORTS

THE NORMAL MODE (SR=0000) OF OPERATION FOR THIS TEST IS TO SIMPLY ACCUMULATE THE ERRORS THAT OCCUR AND TO DUMP THE CONTENTS OF THE COUNTERS ON THE TTY AS EACH DRIVE REACHES EOT, THE ONLY ERROR REPORT THAT CAN OCCUR IN THIS MODE IS IF THE SYSTEM FAILS TO WRITE THE SAME RECORD FOUR TIMES IN A ROW WITH EXTENDED INTERRECORD GAP,

SWITCH REGISTER BITS 2 AND 4 ALTER THIS MODE OF ERROR REPORTING BY FORCING REPORTS FOR ALL WRITE AND READ-COMPARE ERRORS, RESPECTIVELY, AS THEY OCCUR,

7.1 ACCUMULATED WRITE ERRORS REPORT

WHEN A WRITE OPERATION ENCOUNTERS EOT, THE FOLLOWING REPORT IS PRINTED,

```
END OF TAPE
DRV PAT PAR DEN MODE RECORDS LENGTH
1   7   1   800 SSTP   02954 2016 MAX TO MIN
WRITE ERRORS=0009
RECOVERED AT 1 0002
RECOVERED AT 2 0003
RECOVERED AT 5 0001
PERMANENT BADSPT 0003
```

WITH THE FOLLOWING DEFINITIONS:

SYMBOL	DEFINITION
DRV	DRIVE NUMBER
PAT	SELECTED DATA PATTERN

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PAR	SELECTED PARITY
DEN	SELECTED DENSITY
MODE	WRITE STOP MODE
RECORDS	NUMBER OF RECORDS WRITTEN
LENGTH	SELECTED RECORD LENGTH SEQUENCE (2016 SHOWN IS AVERAGE LENGTH)
WRITE ERRORS	TOTAL WRITE ERRORS
RECOVERED AT N	NUMBER OF WRITE ERRORS RECOVERED ON THE NTH REWRITE
PERMANENT BADSPT	NUMBER OF WRITE ERRORS NOT RECOVERED AFTER 7 REWRITES

A SIMILAR REPORT WILL OCCUR WHEN THE END OF A RECORD LENGTH SEQUENCE IS REACHED AND SR0=1, HOWEVER "END OF TAPE" IS REPLACED BY "WRITE DUMP".

7.2 WRITE STATUS ERROR REPORT

IF SR2=1 WHEN A WRITE ERROR IS DETECTED, THE FOLLOWING ERROR REPORT WILL BE PRINTED.

```
WRITE STATUS ERROR
COMD FUNCTN STATUS WRDCNT CURADR RECORDS LENGTH
NNNN   NNNN   NNNN   NNNN   NNNN   NNNNN   NNNN
```

WITH THE FOLLOWING DEFINITIONS.

SYMBOL	DEFINITION
COMD	COMMAND REGISTER
FUNCTN	FUNCTION/STATUS REGISTER
STATUS	MAIN STATUS REGISTER
WRDCNT	WORD COUNT REGISTER
CURADR	CURRENT ADDRESS REGISTER
RECORDS	RECORD NUMBER
LENGTH	RECORD LENGTH

THE ABOVE REPORT WILL ALSO BE FORCED, REGARDLESS OF SR SETTINGS, IF A WRITE ERROR PERSISTS AFTER FOUR REWRITES WITH EXTENDED INTERRECORD GAP. THE REPORT IS AMENDED WITH:

"XRIG WRITTEN 4 TIMES".

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7.3 ACCUMULATED READ ERRORS REPORT

WHEN A READ-COMPARE OPERATION ENCOUNTERS EOT, THE FOLLOWING REPORT IS PRINTED.

```
READ PASS
END OF TAPE
DRV PAT PAR DEN MODE RECORDS LENGTH
1   7    1  800 NSTP  02954  2016 MAX TO MIN
READ ERRORS=0010
NON RECOVERABLE=0002
DATA ERRORS=0003
DATA NO STATUS=0001
```

WITH THE FOLLOWING DEFINITIONS (REFER TO 7.1):

SYMBOL	DEFINITION
READ ERRORS	TOTAL NUMBER OF READ ERRORS INCLUDING ERRORS ON REREAD.
NON RECOVERABLE	TOTAL NUMBER OF NON RECOVERABLE READ ERRORS (AFTER TWO REREADS)
DATA ERRORS	TOTAL NUMBER OF DATA (READ-COMPARE) ERRORS NOT INCLUDING REREADS.
DATA NO STATUS	TOTAL NUMBER OF DATA ERRORS NOT INCLUDING REREADS, WITHOUT ACCOMPANYING PARITY ERRORS OR OTHER STATUS ERRORS. THIS TYPE OF ERROR SHOULD ALWAYS BE CONSIDERED NON RECOVERABLE IN NATURE.

A SIMILAR REPORT WILL OCCUR WHEN THE END OF A RECORD LENGTH SEQUENCE IS REACHED AND SR0=1, HOWEVER "END OF TAPE" IS REPLACED BY "READ DUMP".

7.4 READ STATUS ERROR REPORT

IF SR4=1 WHEN A READ-COMPARE STATUS ERROR IS DETECTED, THE FOLLOWING ERROR REPORT WILL BE PRINTED.

```
READ STATUS ERROR
COMD FUNCTN STATUS WRDCNT CURADR RECORDS LENGTH
NNNN   NNNN   NNNN   NNNN   NNNN  NNNNN   NNNN
```

REFER TO 7.2 FOR SYMBOL DEFINITIONS.

8. RESTRICTIONS

IF ANY DEVICE OTHER THAN THE TM8-E CAUSES A PROGRAM INTERRUPT, THE PROGRAM WILL HALT. THE REASON FOR THIS RESTRICTION IS THAT EXTREMELY TIME CRITICAL OPERATIONS ARE BEING EXECUTED IN THE BACKGROUND WHILE RECORDS ARE BEING WRITTEN AND READ-COMPARED. THE PROGRAM MUST CONSTANTLY MONITOR THE TM8-E CURRENT ADDRESS REGISTER AS DATA TRANSFERS ARE TAKING PLACE.

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9. PROGRAM DESCRIPTION

THIS PROGRAM IS DESIGNED AROUND TWO MAIN SUBROUTINES AND A SERIES OF SHORTER SUBROUTINES FOR MANIPULATING DRIVE SELECTION AND ERROR AND RECORD POSITION TABLES.

THE TWO MAIN SUBROUTINES ARE THE WRITE AND READ-COMPARE ROUTINES. THE WRITE ROUTINE EXITS AFTER EVERY RECORD, EVERY RECORD LENGTH SEQUENCE, OR AT END OF TAPE. THE READ ROUTINE EXITS WHEN THE LAST RECORD WRITTEN ON TAPE HAS BEEN READ. SOME TESTS MANIPULATE THE LAST RECORD COUNTER SO THE READ ROUTINE EXITS AFTER EVERY RECORD.

OTHER SUBROUTINES USED SET UP DRIVE SELECTION TO THE LOWEST DRIVE NUMBER, CHANGE DRIVE SELECTION TO THE NEXT HIGHEST DRIVE, AND GET AND SAVE ERROR AND POSITION TABLES FOR THE DRIVE CURRENTLY SELECTED.

ALL THESE SUBROUTINES ARE TIED TOGETHER IN VARIOUS SEQUENCES FOR TEST SELECTIONS 0 THROUGH 9.

ALL DATA IS CHECKED USING THE READ-COMPARE FUNCTION. THE READ FUNCTION IS NEVER USED. BY USING THIS METHOD, RECORDS ARE USED WHICH ARE MUCH LONGER THAN COULD EVER BE POSSIBLE IN A 4K SYSTEM THAT ALSO CONTAINS THIS PROGRAM. THE OVERALL CONCEPT USED TO ALLOW UTILIZING LONG RECORDS IN THIS PROGRAM IS TO USE A RELATIVELY SHORT DATA BUFFER, THEN MONITORING THE CURRENT ADDRESS REGISTER, RESET THE CURRENT ADDRESS TO THE START OF THE BUFFER WHEN IT REACHES THE END OF THE BUFFER. THIS TECHNIQUE INVOLVES TIME CRITICAL PROGRAM EXECUTION, HENCE NO PROGRAM INTERRUPTS ARE ALLOWED OTHER THAN THOSE CAUSED BY THE IM8-E.

10. LISTING (ATTACHED

APPENDIX D
TM8-E/TS03 DRIVE FUNCTION TIMER

```
                    IDENTIFICATION
                    --------------

PRODUCT CODE:   MAINDEC-08-DHTSE-A-D

PRODUCT NAME:   TM8-E/TS03 DRIVE FUNCTION TIMER

DATE CREATED:   JUNE 16, 1975

MAINTAINER:     DIAGNOSTIC GROUP

AUTHOR:         R. B. BARNES
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NOTE

THERE ARE FIVE DIAGNOSTIC PROGRAMS ASSOCIATED WITH THE TM8-E DECMAGTAPE CONTROL AND ITS TRANSPORT SYSTEM. ALTHOUGH PHYSICALLY SEPARATE, THESE PROGRAMS MUST BE TREATED AS A LARGE INTEGRATED TEST, AND TO ENSURE PROPER SYSTEM OPERATION, THESE TESTS MUST BE EXECUTED IN THE ORDER DELINEATED BELOW.

IF A GIVEN TEST SHOULD FAIL AND IT APPEARS THAT A FIX HAS BEEN FOUND, ALL PROGRAMS MUST ONCE AGAIN BE RUN. ONLY WHEN ALL TESTS HAVE RUN WITHOUT ANY UNACCEPTABLE ERRORS CAN THE TM8-E SYSTEM BE CONSIDERED UP.

TM8-E DIAGNOSTIC PROGRAMS: ORDER OF EXECUTION

1. TM8-E/TS03 CONTROL TEST PART 1 (MAINDEC-08-DHTSA)
2. TM8-E/TS03 CONTROL TEST PART 2 (MAINDEC-08-DHTSB)
3. TM8-E/TS03 DRIVE FUNCTION TIMER (MAINDEC-08-DHTSE)
4. TM8-E/TS03 DATA RELIABILITY 9 TRACK (MAINDEC-08-DHTSC) FOR 4K SYSTEMS
5. TM8-E/TS03 MULTIDRIVE DATA EXERCISER (MAINDEC-08-DHTSD) FOR 8K AND LARGER

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1. ABSTRACT

THE TM8E DRIVE FUNCTION TIMER ASSISTS IN THE TESTING OF THE TM8E CONTROL UNIT AND TS03 TAPE UNIT. SELECTED OPER/ ONS ARE EXECUTED, TIMED, AND THE TIMES ARE THEN PRINTED (IN MILLISECONDS). THERE IS NO LIMIT OR ERROR TESTING FACILITIES IN THE PROGRAM, THE DECISION ON THE VALIDITY OF TIMES MEASURED MUST BE MADE BY THE OPERATOR. ANY CONFIGURATION OF UP TO 8 TS03 TAPE UNITS (7 AND 9 CHANNEL) MAY BE SELECTED.

2. REQUIREMENTS

2.1 HARDWARE

PDP-8/E, 8/M, 8/F
TELETYPE OR COMPATIBLE DEVICE (TTY)
TM8-E DECMAGTAPE CONTROL
TS03 MASTER/SLAVE TRANSPORT SYSTEM

2.2 MEMORY

THIS PROGRAM REQUIRES 4K OF MEMORY AND MAY RESIDE IN ANY MEMORY FIELD.

2.3 PRELIMINARY PROGRAMS

ALL PROCESSOR/MEMORY DIAGNOSTICS
TM8-E CONTROL TEST PART 1
TM8-E CONTROL TEST PART 2

3. PROGRAM LOADING PROCEDURE

LOAD THE PROGRAM INTO ANY DESIRED MEMORY FIELD USING THE STANDARD BINARY LOADER TECHNIQUE.

4. PROGRAM STARTING PROCEDURE

A. LOAD ADDRESS 0200
B. LOAD THE EXTENDED ADDRESS WITH THE PROGRAM FIELD.
C. CLEAR SWITCHES
D. DEPRESS CLEAR, THEN CONTINUE
E. THE PROGRAM WILL PRINT ITS TITLE AND MAINDEC NUMBER, THEN ASK FOR DRIVE SELECTION. PRIOR TO MAKING DRIVE SELECTION, GO TO THE STANDARD TEST PROCEDURE IN PARAGRAPH 5.

NOTE: THE PROGRAM MAY BE RESTARTED AT ANY TIME AT ADDRESS 0201. IN THIS CASE THE PROGRAM BYPASSES PRINTING ITS TITLE AND IMMEDIATELY ASKS FOR DRIVE SELECTION.

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5. STANDARD TEST PROCEDURE

USE OF THE STANDARD TEST PROCEDURE ENSURES PROPER TM8-E/TS03 CHECKOUT. INFORMATION REGARDING THE TIME LIMIT SPECIFICATIONS FOR THE TAPE OPERATIONS TIMED BY THIS PROGRAM ARE GIVEN IN PARAGRAPH 7.1. NO ERROR DETECTION OR DECISIONS REGARDING PROPER FUNCTION TIMES ARE CARRIED OUT BY THE PROGRAM.

5.1 DRIVE SELECTION

TO SPECIFY THE DRIVE(S) TO BE TESTED, CARRY OUT THE FOLLOWING STEPS:

A. MOUNT A SPARE REEL OF INDUSTRY COMPATIBLE MAGNETIC TAPE ON ALL DRIVES TO BE SELECTED WITH THE WRITE ENABLE RING IN PLACE (WRITE ENABLED). LOAD THE TAPES AND POSITION AT BOT. ASSIGN DRIVE NUMBERS IN THE FOLLOWING SEQUENCE: 0,7,1,1,6,2,5,3,4 AND THEN SWITCH ON LINE.

B. START OR RESTART THE PROGRAM AS DESCRIBED IN PARAGRAPH 4.

C. RESPOND TO "SELECT DRIVES" BY SETTING SR BIT N = 1 FOR EACH DRIVE TO BE TESTED (DRIVE N). THEN DEPRESS CONTINUE.

D. RESPOND TO "SELECT 7 AND/OR 9 TRACK OPERATION" BY SETTING SR BIT N = 1 ONLY FOR THOSE SELECTED DRIVES WHICH ARE 9 TRACK UNITS. THEN DEPRESS CONTINUE.

5.2 TEST PROCEDURE

ACCOMPLISH THE FOLLOWING STEPS FOR ALL DRIVES IN THE SYSTEM UNDER TEST.

A. SELECT ALL DRIVES IN THE SYSTEM UNDER TEST AS DESCRIBED IN PARAGRAPH 5.1 ABOVE.

B. AS SOON AS TRACK SELECTION IS COMPLETE, THE PROGRAM WILL START TIMING THE VARIOUS TAPE OPRATIONS AND INDICATING ALL TIMES ON THE TTY.

C. REPEAT THE ENTIRE TIMING PROCEDURE 2 TIMES.

D. COMPARE THE RESULTS AS PRINTED ON THE TTY WITH THE LIMITS SPECIFIED IN PARAGRAPH 7.1. ADDITIONAL INFORMATION IS GIVEN IN THE PROGRAM DESCRIPTION IN PARAGRAPH 10.

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6. PROGRAM CONTROLS

THERE ARE NO SWITCH REGISTER OPTIONS ASSOCIATED WITH THIS PROGRAM.

7. ERRORS

THERE IS NO ERROR DETECTION INCLUDED IN THIS PROGRAM.
ALL DECISIONS MUST BE MADE BY THE USER BY COMPARING
THE FUNCTION TIMES PRINTED ON THE TTY WITH THOSE TIMES
GIVEN IN THE TABLE BELOW.

7.1 TIME LIMITS SPECIFICATION

THE TABLE BELOW LISTS THE TIME LIMITS IN THE SAME FORMAT
AS THEY ARE PRINTED ON THE TTY.

FUNCTION			
800 BPI	UNIT0	+/-	UNIT1
WR FM BOT DELAY	564	50	SAME
WRITE SHUTDOWN	2.8	.5	SAME
WRITE START	36	4	SAME
WR NONSTOP GAP	39	4	SAME
BKSP SHDWN+SDWN	38	4	SAME
READ SHUTDOWN	.8	.5	SAME
WRITE XIRG	333	30	SAME
LAST CHAR TO CUR	.8	.5	SAME
RD FM BOT DELAY	564	50	SAME
SPCE SHDWN+SDWN	33	3	SAME
WRITE EOF	349	30	SAME
ER TO EF SP TIME	348	30	SAME
WR TO ERASE HEAD	53	6	SAME
1 INCH DATA TIME	80	2	SAME
GAP1			
GAP2			
GAP3			
GAP4	GAPS: 8>7>6>5>4>1		2>3
GAP5			
GAP6			
GAP7			
GAP8			

8. RESTRICTIONS

NONE.

9. EXECUTION TIME

EXECUTION TIME VARIES DEPENDING ON THE NUMBER AND TYPES OF DRIVES BEING TESTED.

10. PROGRAM DESCRIPTION

10.1 WRITE FROM BOT DELAY

THIS IS THE TIME NECESSARY TO MOVE BEGINNING OF TAPE (BOT) MARKER APPROXIMATELY 6 INCHES PAST THE WRITE HEAD.
THE FIRST RECORD ON TAPE MUST BE WRITTEN AT LEAST 3" AWAY FROM THE BOT MARKER.

PROCEDURE TO MEASURE TIME:

A. REWIND TO BOT.

B. INITIALIZE WC & CA LOCATIONS.

C. LOAD COMMAND REGISTER WITH DRIVE SELECT, 800 BPI, ODD PARITY.

D. LOAD FUNCTION WITH WRITE & GO BITS.

E. MONITOR CA REGISTER UNTIL IT INDICATES FIRST WORD HAS BEEN TAKEN.

F. THE TIME FROM "GO" UNTIL FIRST WORD IS OUTPUT IS "WRITE FROM BOT DELAY."

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10',2 WRITE SHUTDOWN

THIS IS THE TIME NECESSARY TO CONTINUE MOVING TAPE AFTER A RECORD IS WRITTEN SO THAT THE PROPER INTERRECORD GAP WILL EXIST BETWEEN RECORDS.

PROCEDURE TO MEASURE TIME:

A. REWIND TO BOT',

B. INITIALIZE WC & CA LOCATIONS TO WRITE ONE 200(10) WORD RECORD FROM BOT,

C. LOAD COMMAND REGISTER WITH DRIVE SELECT, 800 BPI, ODD PARITY,

D. LOAD FUNCTION WITH WRITE & GO BITS',

E. AFTER MTTF SETS INDICATING THE END OF RECORD, INITIATE A CONTINUOUS WRITE AND TIME TILL THE FIRST WORD IS TRANSFERRED FROM MEMORY TO THE TM8-E CONTROL (OCCURS APPROXIMATELY ON THE LEADING EDGE OF SDWN)

10',3 WRITE START

THE TIME NECESSARY FOR TAPE TO ACCELERATE TO FULL SPEED + GUARANTEE A 1/2" INTERRECORD GAP',

PROCEDURE TO MEASURE TIME:

SAME AS "WRITE FROM BOT" EXCEPT NOW WE ARE NOT AT BOT',

A. INITIALIZE WC & CA REGISTER,
B. LOAD COMMAND WITH DRIVE SELECT, 800 BPI, ODD PARITY,
C. LOAD FUNCTION WITH WRITE & GO BITS',
D. MONITOR CA FOR ITS SECOND INCREMENT,
E. THE TIME FROM "GO" UNTIL 2ND INCREMENT OF CA IS APPROXIMATELY EQUAL TO "WRITE START",

10',4 WRITE NONSTOP GAP

WRITE NONSTOP GAP IS EQUIVALENT TO THE SUM OF "WRITE SHUTDOWN" & "WRITE START" AND IS THE TIME NECESSARY TO INSURE THAT THE INTERRECORD GAP WILL BE AT LEAST 1/2" WHEN WRITING NON-STOP.

PROCEDURE TO MEASURE TIME:

A. INITIALIZE WC & CA LOCATIONS
B. LOAD COMMAND WITH DRIVE SELECT, 800 BPI, ODD PARITY,
C. LOAD FUNCTION;WRITE, GO BITS,
D. WAIT FOR "JOB DONE,"
E. ISSUE "CLF,"
F. RE-INITIALIZE WC & CA LOCATIONS,
G. LOAD FUNCTION;WRITE, GO BITS,
H. TIME FROM 2ND "GO" UNTIL FIRST WORD OF 2ND WRITE IS OUTPUT IS "WRITE NONSTOP GAP,"

(PAGE 6)

10,5 BACKSPACE SHUTDOWN + SETTLE DOWN DELAY

THIS IS THE LENGTH OF TIME NECESSARY TO GUARANTEE THAT IF A WRITE OPERATION FOLLOWS A BACKSPACE THE TAPE WILL BE POSITIONED SUCH THAT ALL PREVIOUS DATA IS IN FRONT OF THE WRITE AND ERASE HEADS AND WILL BE ERASED.

PROCEDURE TO MEASURE TIME:

RECORD IS USED WHICH WAS JUST WRITTEN IN PREVIOUS TEST "WRITE NONSTOP GAP".

A. LOAD COMMAND WITH DRIVE SELECT, 800 BPI, ODD PARITY.

B. SET WC TO BACKSPACE 1 RECORD.

C. ISSUE BACKSPACE, GO.

D. AFTER JOB DONE BECOMES A ONE INDICATING THE BEGINNING OF THE RECORD MONITOR TUR UNTIL IT BECOMES A "1". THE TIME FROM JOB DONE UNTIL TUR IS "BACKSPACE SHUTDOWN + SETTLEDOWN DELAY."

10,6 READ SHUTDOWN

THIS IS THE AMOUNT OF TIME NECESSARY TO CONTINUE MOVING TAPE AFTER A RECORD IS READ SO THAT THERE IS ENOUGH GAP FOR TAPE TO BE FULLY ACCELERATED IF A READ IS FOLLOWED BY A BACKSPACE. "READ SHUTDOWN" MUST ALSO BE LESS THAN "WRITE SHUTDOWN" TO GUARANTEE THAT THE WRITE AND ERASE HEADS WILL BE POSITIONED SUCH THAT ALL PREVIOUS DATA IS IN FRONT OF THE HEADS AND WILL BE ERASED IF A WRITE FOLLOWS A READ. IN ADDITION WHEN A WRITE FOLLOWS A READ THE INTERRECORD GAP MUST STILL BE AT LEAST 1/2".

PROCEDURE TO MEASURE TIME:

A. RECORD USED IN "BACKSPACE SHUTDOWN" IS READ.

B. INITIALIZE WC & CA REGISTERS.

C. ISSUE READ FUNCTION, 800 BPI, GO.

D. AFTER MTTF SETS INDICATING THE END OF RECORD, INITIATE A CONTINUOUS WRITE AND TIME TILL THE FIRST WORD IS TRANSFERRED FROM MEMORY TO THE TM8-E CONTROL (OCCURS APPROXIMATELY ON THE LEADING EDGE OF SDWN).

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10,7 WRITE XIRG

THIS IS THE TIME NECESSARY TO CAUSE THE GENERATION OF AN INTERRECORD GAP THAT IS AT LEAST 3" LONG AS COMPARED WITH THE NORMAL 3/5" GAP. THE PURPOSE IS TO ELIMINATE WRITE ERRORS THAT MAY BE CAUSED BY A DEFECTIVE AREA ON TAPE. NORMALLY ONE REWRITE WITH XIRG WOULD BE SUFFICIENT IF IT ISN'T THE PROCEDURE WOULD BE TO REPEAT THE "BACKSPACE=REWRITE WITH XIRG" SEQUENCE UNTIL A RECORD IS WRITTEN WITHOUT ERRORS. EACH SUCCESSIVE REWRITE WOULD ADD 3" TO THE INTERRECORD GAP UNTIL "GOOD" TAPE WAS REACHED.

PROCEDURE TO MEASURE TIME:

A. TAPE IS NOT BOT.

B. INITIALIZE WC & CA REGISTERS.

C. ISSUE WRITE WITH XIRG FUNCTION, 800 BPI, GO.

D. MONITOR CA TO DETERMINE WHEN FIRST WORD IS OUTPUT.

E. THE TIME FROM "GO" UNTIL FIRST WORD IS OUTPUT IS "WRITE WITH XIRG".

10,8 LAST CHARACTER TO CU READY

THIS IS THE AMOUNT OF TIME IT TAKES FOR THE CONTROL TO SENSE 3 MISSING WORDS ON TAPE (END OF RECORD) UNTIL "CU READY" BECOMES A "1."

PROCEDURE TO MEASURE TIME:

A. PROGRAM USES SAME RECORD THAT WAS WRITTEN DURING "WRITE XIRG."

B. LOAD COMMAND WITH DRIVE SELECT, 800 BPI, ODD PARITY.

C. INITIALIZE WC TO SPACE REVERSE 1 RECORD.

D. WAIT FOR JOB DONE.

E. REINITIALIZE WC & CA LOCATIONS.

F. LOAD COMMAND WITH DRIVE SELECT, 800 BPI, ODD PARITY.

G. ISSUE READ FUNCTION, GO.

H. WAIT UNTIL WC=0 AND THEN MONITOR "CU READY" UNTIL IT BECOMES A "1".

J. THE TIME FROM WC=0 UNTIL "CU READY" = 1 IS "LAST CHARACTER TO CU READY".

(PAGE 8)

10,9 READ FROM BOT

THE FIRST RECORD WRITTEN ON TAPE IS SUPPOSED TO BE AT LEAST 6" FROM THE BOT MARKER, IN THE EVENT THAT THIS CONDITION WASN'T MET IT IS STILL DESIREABLE TO READ THE RECORD, READ FROM BOT IS THE TIME FROM WHEN A READ FUNCTION IS ISSUED UNTIL THE FIRST WORD IS OUTPUT.

PROCEDURE TO MEASURE TIME:

A. THE RECORD THAT WAS WRITTEN JUST OFF BOT DURING "WRITE START" IS USED.

B. TAPE IS REWOUND TO BOT.

C. INITIALIZE WC & CA REGISTERS.

D. ISSUE READ FUNCTION, 800 BPI, GO.

E. MONITOR CA TO DETERMINE WHEN FIRST WORD IS OUTPUT.

F. THE TIME FROM "GO" UNIL FIRST BREAK IS "READ FROM BOT."

10,10 SPACE SHUTDOWN + SETTLEDOWN DELAY

SPACE SHUTDOWN IS THE AMOUNT OF TIME NECESSARY TO CONTINUE MOVING TAPE AFTER A RECORD IS SPACED OVER IN THE FORWARD DIRECTION FOR THE SAME REASONS AS "READ SHUTDOWN".

PROCEDURE TO MEASURE TIME:

A. SAME RECORD IS USED AS IN T3 WRITE START.

B. INITIALIZE WC TO SPACE FORWARD 1 RECORD.

C. ISSUE SPACE FORWARD FUNCTION, 800 BPI, GO.

D. MONITOR JOB DONE UNTIL IT IS #1.

E. TIME FROM JOB DONE #1 UNTIL TUR IS "SPACE SHUTDOWN + SETTLEDOWN DELAY".

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10,11 WRITE EOF

TO WRITE AN END OF FILE MARK IT IS NECESSARY
FOR TAPE TO MOVE 3 INCHES BEFORE WRITING
A RECORD WITH EXTENDED INTERRECORD GAP,
HOWEVER, AN EOF MARK CORRESPONDS TO A
1 WORD RECORD, THE TIME SHOULD BE
SLIGHTLY LARGER THAN "WRITE XIRG",

PROCEDURE TO MEASURE TIME;

A, TAPE UNIT IS REWOUND TO BOT,

B, INITIALIZE WC & CA REGISTERS,

C, ISSUE WRITE, 800 BPI, GO,

D, WAIT FOR JOB DONE,

E, ISSUE CLF,

F, ISSUE WRITE EOF FUNCTION, 800 BPI, GO,

G, WAIT FOR JOB DONE #1

H, THE TIME FROM "GO" UNTIL "JOB DONE" IS
"WRITE EOF,"

10,12 EOR TO EOF TIME

THIS IS THE TIME NEEDED TO MOVE TAPE FROM
THE END OF A RECORD TO AN END OF FILE MARK
WRITTEN AFTER IT, THE PROCEDURE USED TURNS
OUT TO BE A TEST OF THE WRITE AND ERASE
HEAD POLARITIES, IF THE TIME PRINTED IS
EQUAL TO ZERO IT IS AN INDICATION THAT THE
EOF WAS NOT FOUND WHEN "JOB DONE" BECAME A ONE,

THIS COULD INDICATE ONE OR MORE OF THE FOLLOWING
PROBLEMS;

1, ERASE HEAD POLARITY REVERSED,

2, ERASE HEAD CURRENT NOT SUFFICIENT TO FULLY
SATURATE TAPE,

3, ONE OR MORE OF WRITE HEAD TRACKS POLARITY
REVERSED,

4, ONE OR MORE SENSITIVE READ AMPLIFIERS,

5, WRITE EOF FUNCTION DIDN'T REALLY WRITE AN EOF MARK,

OTHERWISE "EOR TO EOF SPACE TIME" SHOULD BE
SLIGHTLY LARGER THAN "WRITE EOF,"

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PROCEDURE TO MEASURE TIME:

A, A RECORD AND EOF WAS PREVIOUSLY WRITTEN
FROM BOT FOR "WRITE EOF",

B, TAPE IS REWOUND TO BOT,

C, REWRITE RECORD OVER PREVIOUSLY WRITTEN RECORD,

D, BACKSPACE OVER RECORD JUST WRITTEN;

E, SET WC REGISTER TO SPACE 2 RECORDS;

F, ISSUE SPACE FORWARD FUNCTION, SET GO,

G, WAIT FOR WC REGISTER TO INDICATE THAT
FIRST RECORD HAS BEEN SPACED OVER THEN
MONITOR "CU READY" UNTIL IT BECOMES A
"1", AFTER "CU READY" CHECK TO SEE IF "EOF"
IS A 1 IN STATUS REGISTER, IF EOF IS NOT
SET THEN ZERO TIME COUNTER;

H, TIME FROM WC=-1 UNTIL "CU READY" IS "EOR TO EOF SPACE TIME"

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10,13 WRITE TO ERASE HEAD

THE "WRITE TO ERASE HEAD" TEST INSURES THAT THE TAPE IN FRONT OF THE WRITE HEAD IS ERASED DURING A WRITE OPERATION.

PROCEDURE TO MEASURE TIME:

A. A LONG RECORD HAS BEEN WRITTEN FROM BOT, SAME RECORD THAT WAS USED TO TIME "WRITE FROM BOT DELAY"

B. TAPE IS REWOUND TO BOT.

C. WC REGISTER IS INITIALIZED FOR A 3 WORD RECORD
CA REGISTER IS INITIALIZED TO 3775.

D. LOAD COMMAND REGISTER WITH DRIVE SELECT, 800 BPI, ODD PARITY.

E. LOAD FUNCTION REGISTER WITH WRITE & GO BITS.

F. MONITOR CA UNTIL IT IS 3777 INDICATING 2 WORDS HAVE BEEN OUTPUT, THEN ISSUE CLT WHICH STOPS ALL DATA TRANSFERS & CAUSES THE DRIVE TO SHUTDOWN.

G. REWIND TO BOT.

H. INITIALIZE CA TO 3775

I. ISSUE READ FUNCTION, 800 BPI, SET GO.

J. MONITOR CA UNTIL IT IS 3777 THEN
GO TO TIMING ROUTINE AND TIME UNTIL CA=4000
THIS TIME WILL INDICATE THE DISTANCE BETWEEN THE LAST WORD OF THE NEW DATA AND THE FIRST WORD OF THE OLD DATA WHICH IS ALSO THE AMOUNT OF TAPE THAT WAS ERASED BY THE ERASE HEAD DURING THE WRITE OPERATION.

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10,14 ONE INCH DATA TIME

ONE INCH OF DATA, 800 BPI (ALSO 556 & 200 IF 7 CHANNEL UNIT), IS WRITTEN AND TIMED TO DETERMINE IF TAPE IS MOVING AT PROPER SPEED.

PROCEDURE TO MEASURE TIME:

A. INITIALIZE WC & CA REGISTERS, CA(3776) WC(=2000)

B. ISSUE WRITE FUNCTION, 800, 556 OR 200 BPI, GO,

C. WAIT FOR CURRENT MEMORY ADDRESS REGISTER TO INDICATE FIRST WORD IS TAKEN AND THEN MONITOR WORD COUNT UNTIL EQUAL TO ZERO,

D. TIME FROM FIRST WORD OUTPUT UNTIL WORD COUNT=0 IS "ONE INCH DATA TIME,"

10,15 GAP CONSISTENCY

FOR PROPER OPERTION THE INTERRECORD GAPS ON TAPE MUST ALWAYS BE AT LEAST 1/2 OF AN INCH, THIS WILL ALLOW DATA WRITTEN USING ONE TAPE UNIT TO BE READ ON ANOTHER TAPE UNIT WHEN THE START/STOP CHARACTERISTICS OF EACH UNIT ARE DIFFERENT. THE MINIMUM GAP SIZE OF 1/2 AN INCH IS GENERATED WHEN A WRITE FOLLOWS A READ; ALL OTHER GAPS SHOULD BE LARGER DEPENDING ON HOW THEY WERE WRITTEN.

PROCEDURE TO MEASURE TIME:

A. A TOTAL OF NINE RECORDS ARE WRITTEN ON TAPE (FROM BOT) UTILIZING DIFFERENT SEQUENCES TO GENERATE THE INTERRECORD GAPS,

B. THE TAPE IS REWOUND TO BOT,

C. INITIALIZE WORD COUNT AND CURRENT ADDRESS REGISTERS,

D. ISSUE READ FUNCTION, 800 BPI, SET "GO",

E. WAIT FOR "CU READY" TO BECOME A 1 THEN REPEAT STEP C AND RESET "GO" TO CONTINUE NONSTOP,

F. NOMITOR CA REGISTER TO DETERMINE WHEN FIRST WORD IS INPUT,

G. THE TIME FROM WHEN "GO" IS RESET UNTIL THE FIRST WORD IS INPUT WILL REFLECT THE SIZE OF THE GAP,

H. STEPS E,F ARE REPEATED UNTIL ALL 8 GAPS ARE MEASURED,

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PROGRAM SEQUENCE FOR EACH GAP:

GAP1 WRITE FOLLOWED BY A WRITE (NONSTOP);

GAP2 WRITE FOLLOWED BY A WRITE (START/STOP),

GAP3 READ FOLLOWED BY A WRITE (START/STOP),

GAP4 WRITE-BACKSPACE FOLLOWED BY A WRITE (START/STOP);

GAP5 SAME AS GAP4 EXCEPT WRITE-BACKSPACE REPEATED 2 TIMES;

GAP6 SAME AS GAP4 EXCEPT WRITE-BACKSPACE REPEATED 3 TIMES;

GAP7 SAME AS GAP4 EXCEPT WRITE-BACKSPACE REPEATED 4 TIMES;

GAP8 SAME AS GAP4 EXCEPT WRITE-BACKSPACE REPEATED 5 TIMES;

GAP LENGTHS SHOULD REFLECT THE FOLLOWING RELATIONSHIP:
8>7>6>5>4>1, 2>3

11; LISTING (ATTACHED)

APPENDIX E
TM8-E/TS03 UTILITY DRIVER

IDENTIFICATION

PRODUCT CODE:	MAINDEC-08-DHTSF-A-D
PRODUCT NAME:	TM8-E/TS03 UTILITY DRIVER
DATE CREATED:	21-SEPT-75
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	R. B. BARNES

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1. ABSTRACT

THIS PROGRAM IS INTENDED AS A BRUTE FORCE ROUTINE TO EXECUTE AN OPERATION OR SEQUENCE OF OPERATIONS CONTINUOUSLY REGARDLESS OF THE RESULTS OF THE OPERATION. THE UTILITY DRIVER WILL ALLOW THE OPERATOR TO DO ANYTHING IN ANY ORDER, THERE ARE NO ERROR CHECKS OR PRINTOUTS MADE, AND ANY VARIATION FROM PRESET SEQUENCES AND VALUES ARE MADE BY CHANGING THE APPROPRIATE MEMORY LOCATIONS.

2. REQUIREMENTS

A. ANY PDP-8 PROCESSOR
B. TM8-E MAGTAPE CONTROLLER
C. AT LEAST ONE TAPE DRIVE
D. AT LEAST 1K OF CORE

3. LOADING PROCEDURE

USE STANDARD BINARY LOADING PROCEDURE.

4. STARTING PROCEDURE

ALWAYS START AT 200(8).

5. CONSOLE SWITCH SETTINGS

SW0: 1 = STOP AFTER EACH OPERATION
0 = PROCEED

SW1: 1 = STOP AT THE END OF THE OPERATION
0 = PROCEED

SW2: 1 = IGNORE END OF TAPE
0 = REWIND AT EOT

SW3: 1 = DISPLAY REGISTER (SEE PAGE 4)
0 = DO NOT DISPLAY

6. OPERATION

THE PROGRAM OPERATION IS QUITE SIMPLE, BUT DOES REQUIRE THE OPERATOR TO HAVE KNOWLEDGE OF MAGTAPE SYSTEM AS OPERATED ON TM8E CONTROLLER. THE OPERATOR MUST BE ABLE TO DECIDE WHICH SEQUENCE OF OPERATIONS SHOULD BE RUN AND WHAT VALUES TO ASSIGN THE VARIOUS PARAMETERS REQUIRED TO RUN THEM. THE OPERATION SEQUENCE IS SET UP BY FILLING A TABLE (FNTBL) WITH OP-CODES IN THE DESIRED SEQUENCE AND LOADING THE NUMBER OF OPERATIONS IN A COUNTER (FNCTR). THE PROGRAM WILL EXECUTE EACH OF THE OPERATIONS IN THE TABLE IN THAT ORDER CONTINUOUSLY UNLESS STOPPED BY SW0 OR SW1 BEING SET TO A ONE (1). THE PROGRAM IS PRESET TO DO CONTINUOUS WRITE TO UNIT ZERO (0) WITH DENSITY OF 800 BPI (9 TRK) IN ODD PARITY, EACH RECORD IS TWENTY (20) CHARACTERS AND DATA IS TAKEN FROM MEMORY STARTING AT LOCATION 400. IF THE PROGRAM IS LOADED AND STARTED AT 200 WITH NO CHANGES MADE AND SWITCHES 14 AND 15 SET TO ZERO (0), THIS OPERATION WILL EXECUTE CONTINUOUSLY.

THE FOLLOWING IS A LIST OF PARAMETERS WHICH MAY BE VARIED PLUS THEIR DESCRIPTION AND CORE LOCATIONS:

PARAMETER	LOCATION	DESCRIPTION
UDES	20	UNIT DESCRIPTION: DESITY, PARITY, UNIT NUMBER, ETC;
WDCNT	21	NUMBER OF WORDS PER READ OR WRITE
WADD	22	STARTING ADDRESS OF WRITE BUFFER.
RADD	23	STARTING ADDRESS OF READ BUFFER.
SCNT	24	NUMBER OF RECORDS TO BE SPACED OVER (FORWARD OR REVERSE).
FCNTR	25	NUMBER OF OPERATIONS TO BE EXECUTED IN SEQUENCE FROM FUNCTION TABLE.
JDDLY	26	DELAY TIME FOR JOB DONE FLAG.
OPDLY	27	DELAY BETWEEN OPERATIONS.

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INTBL 44-45 TABLE OF OP-CODE TO BE EXECUTED.

6',1 FUNCTION CODES (FILL INTBL WITH ANY OF THE FOLLOWING)

0000 = OFFLINE
1000 = REWIND
2000 = READ
3000 = READ COMPARE
4000 = WRITE
5000 = WRITE END OF FILE
6000 = SPACE FORWARD (SEE SCNT)
7000 = SPACE REVERSE (SEE SCNT)

6',2 DENSITY SELECT (BITS 10 + 11 OF UDES)

00 = 200BPI 7TRK
01 = 556BPI 7TRK
10 = 800BPI 7TRK
11 = 800BPI 9TRK

6',3 PARITY (BIT 3 OF UDES)

0 = EVEN PARITY
1 = ODD PARITY

6',4 UNIT SELECT (BITS 0, 1, 2 OF UDES)

000 = UNIT 0
001 = UNIT 1

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7', PROGRAM DESCRIPTION

IN ORDER TO MAINTAIN THE CONTINUOUS EXECUTION OF OPERATION AS DESCRIBED, THE PROGRAM IS ORGAINZED AS FOLLOWS,

```
START
CLEAR ALL FLAGS          HOUSEKEEPING
SETUP                    SETUP OP-CODE REQUIRED PARAMETERS
EXECUTE                  START FUNCTION
AWAIT END                WAIT FOR JOB DONE; PER RDDLY
DELAY                    PAUSE PER OPDLY
END OF SEQUENCE?         IF END OF SEQUENCE; STOP =
                         ELSE JUMP TO START
STOP
JUMP TO START            RESTART SEQUENCE
```

8', REGISTER DISPLAY (PER SW3=1)

BECAUSE IT IS NOT POSSIBLE TO EXAMINE THE CONTENTS OF VARIOUS HARDWARE REGISTERS OF THE TM8-E DIRECTLY, A SOFTWARE ROUTINE IS PROVIDED TO DISPLAY THEM IN THE ACCUMULATOR (AC) WHENEVER THE PROGRAM IS STOPPED BY SW0 OR 1. WHEN STOPPED AT THE END OF AN OPERATION OR SEQUENCE OF OPERATIONS, SET SW3=1 AND PRESS CONTINUE SIX (6) TIMES. EACH CONTINUE/HALT, WILL DISPLAY A DIFFERENT REGISTER. TO EXIT THIS ROUTINE AND CONTINUE OPERATION, SET SW3=0 AT ANY TIME. CONTINUE/HALT MAY BE PERFORMED MORE THAN SIX (6) TIMES TO REEXAMINE ALL REGISTERS.

FOLLOWING IS THE LIST OF REGISTERS DISPLAYED AND THE ORDER IN WHICH THEY APPEAR.

```
1.  RWCR     WORD COUNT
2.  RCAR     CURRENT ADDRESS
3.  RMSR     MAIN STATUS
4.  RCMR     COMMAND REGISTER
5.  RFSR     FUNCTION/STATUS
6.  RDBR     DATA BUFFER
```

9', LISTING

APPENDIX F
TM8-E INTERFACE AND INTERNAL SIGNALS

Appendix F lists and identifies all the TS03/TM8-E interface signals. Figure F-1 identifies the interface with the Omnibus along with the Omnibus pin assignment for each signal. Also listed are all the signals internal to the TM8-E.

Two 7011571 cables are used to connect the TM8-E to the TS03. One cable is connected between the M8321 Output Control module and the "C" connector on the M8920 adapter module to provide control signals to the tape drive and data to be written on the TS03 DECmagtape (Table F-1). The other cable connects the M8323 Status and Control module to connector "D" on the M8920 adapter module to provide status information and data read from the TS03 DECmagtape to the TM8-E Controller (Table F-2). The signals on the H851 edge connectors that interconnect the four TM8-E modules, are shown in Tables F-3 through F-6. Table F-7 lists and defines all signals within the TM8-E Controller.

The signal prefix indicates the origin of the signal, i.e., all signals prefixed by C originate at the TS03. The following is a list of the prefixes and their meaning.

Prefix	Origin
C	TS03
OC	M8321 module
CB	M8322 module
SC	M8323 module
RE	M8327 module

The numeral following the prefix indicates the sheet of the module print where the signal originates, i.e., RE-2 indicates the signal originates on the M8327 Module, sheet 2.

PIN	D1	D2	C1	C2	B1	B2	A1	A2
A	TP	+15V	TP	+5V	TP	+5V	TP	+5V
B	TP	− 15V	TP	− 15	TP	− 15V	TP	−15V
C	GND	GND	GND	GND	GND	GND	SP GND	GND
D	MA8L	IRØ L	I/O PAUSE L	TP1 H	MA4 L	INT STROBE H	MAØ L	EMAØ L
E	MA9 L	IR1L	CØL	TP2 H	MA5 L	BRK IN PROG L	MA1L	EMA 1L
F	GND	GND	GND	GND	GND	GND	GND	GND
H	MA1Ø L	IR2 L	C1L	TP3 H	MA6 L	MA,MS LOAD CONT L	MA2 L	EMA2 L
J	MA11 L	FL	C2 L	TP4 H	MA7 L	OVERFLOW L	MA3 L	MEM START L
K	MD8 L	D L	BUS STROBE L	TS1 L	MD4 L	BREAK DATA CONT L	MDØ L	MD DIR L
L	MD9 L	E L	INTERNAL I/O L	T S2 L	MD5 L	BREAK CYCLE L	MD1 L	SOURCE H
M	MD1Ø L	USER MODE L	NOT LAST XFER L	TS3 L	MD6 L	LA ENABLE L	MD2 L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND
P	MD11 L	F SET L	INT ROST L	TS4 L	MD7 L	INT IN PROG H	MD3 L	INHIBIT H
R	DATA 8 L	PULSE LA H	INITIALIZE H	LINK DATA L	DATA 4 L	NTS STALL L	DATA Ø L	RETURN H
S	DATA 9 L	STOP L	SKIP L	LINK LOAD L	DATA 5 L	RES H	DATA 1 L	WRITE H
T	GND	GND	GND	GND	GND	GND	GND	GND
U	DATA 1Ø L	KEY CONTROL L	CPMA DISABLE L	IND 1 L	DATA 6 L	RUN L	DATA 2 L	ROM ADDRESS L
V	DATA 11 L	SW	MS,IR DISABLE L	IND2 L	DATA 7L	POWER OK H	DATA 3 L	LINK L

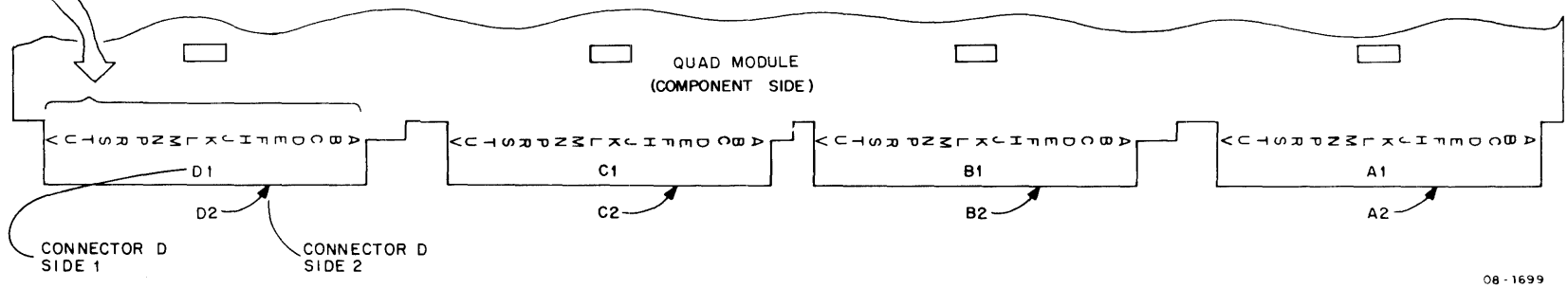


Figure F-1 Omnibus Pin Assignment

Table F-1
M8321 Output Control Module Signals and Interface

M8920 Connector C Pin No.	J1 M8321 Pin No.	J2 M8321 Pin No.	Signal	Description
A1	D		C SEL 0 H	Buffered SELECT 0
B1	F		C SEL 1 H	Buffered SELECT 1
C1	J		C SEL 2 H	Buffered SELECT 2
D1	L		C SEL 16 H	Not used
E1	R		C DEN 5 H	*Density 5
F1	N		C DEN 8 H	*Density 8
S1	LL		C FMK L	File Mark
J1	V		C WXG H	Extended gap
K1	X		C FWD H	Move tape forward
L1	Z		C RWD H	Move tape reverse
M1	BB		C WRE H	Write Enable with CFWD H, go off line with C REW H
D2		L	C WD0 H	Write bit 0
E2		N	C WD1 H	Write bit 1
F2		R	C WD2 H	Write bit 2
H2		T	C WD3 H	Write bit 3
J2		V	C WD4 H	Write bit 4
K2		X	C WD5 H	Write bit 5
L2		Z	C WD6 H	Write bit 6
M2		BB	C WD7 H	Write bit 7
N2		DD	C REW H	Rewind
P2		FF	C INIT H	Initialize
R2		JJ	C SET H	Begin tape operation
S2		LL	C WDR H	Write Data Ready
T2		NN	C PEV W H	Generate or check for even parity when asserted
U2		RR	C WFMK H	Write File Mark

*Not used in TM8-M system.

Table F-2
TM8-E M8323 Transport Status Control Module Signals and Interface

M8920 Connector D Pin No.	J1 M8323 Pin No.	J2 M8323 Pin No.	Signal	Description
A1	D		C RDS L	Read Data strobe
B1	F		C SDWN L	Tape motion is stopping
C1	J		C TUR L	Tape Unit Ready
F1	R		C RD0 L	Read bit 0 from tape unit
H1	T		C RD1 L	Read bit 1 from tape unit
J1	V		C RD2 L	Read bit 2 from tape unit
K1	X		C RD3 L	Read bit 3 from tape unit
L1	Z		C RD4 L	Read bit 4 from tape unit
M1	BB		C RD5 L	Read bit 5 from tape unit
N1	DD		C RD6 L	Read bit 6 from tape unit
P1	FF		C RD7 L	Read bit 7 from tape unit
R1	JJ		C RDP L	Read Parity bit
S1	LL		C FMK L	File Mark (end of file)
D2		L	C WRS L	Write Strobe indicates data on CWD lines has been written on tape
E2		N	C CRCS L	CRC strobe, appears with CRC character
F2		R	C RWS L	Tape Rewinding
K2		X	C BOT L	Beginning of Tape
L2		Z	C WRL L	Write Lock prevents writing on tape
M2		BB	C VPE L	Vertical Parity Error
N2		DD	C SELR L	Existing transport is on line
P2		FF	C 7CH L	7 channel asserted when 7 channel tape unit is selected
R2		JJ	C EOT L	End of Tape
S2		LL	C CRCE L	CRC Error
T2		NN	C LRCE L	LRC Error
U2		RR	C LRCS L	LRC strobe appears with the LRC character

Table F-3
TM8-E M8321 Output Control Module Edge Connector Signals

To M8327 Connector F		To M8327 Connector H	
Signal	**Pin No.**	**Signal**	**Pin No.**
Not used	A1	CB-2 MAC 2 H	A1
OC-2 RWCR L	B1	RE-1 SEL 16 H	B1
RE-1 DB7 H	C1	RE-1 PEVN H	C1
RE-1 FR0 H	D1	SC-1 SET H	D1
RE-1 DB5 H	E1	Not used	E1
CB-1 WR 1st 7 H	F1	RE-1 DB8 H	F1
Not used	H1	Not used	H1
RE-1 DB3 H	J1	RE-1 DB9 H	J1
RE-1 DB2 H	K1	Not used	K1
Not used	L1	RE-1 DB10 H	L1
CB-3 MTTF L	M1	Not used	M1
SC-2 ERROR L	N1	CB-1 WR 2nd 7 H	N1
OC-2 LCAR L	P1	RE-1 DEN 8 H	P1
SC-1 TUR L	R1	RE-1 FR1 H	R1
OC-2 LCMR L	S1	RE-1 FR2 H	S1
CB-3 CLR ALL L	T1	OC-2 CWCR L	T1
OC-2 LCM/F/DB H	U1	OC-2 RMSR L	U1
OC-2 LFGR L	V1	OC-2 RCAR L	V1
Not used	A2	Not used	A2
Not used	B2	Not used	B2
RE-1 DB6 H	C2	CB-1 WDR H	C2
Not used	D2	Not used	D2
OC-1 R/C ERROR L	E2	CB-3 INIT H	E2
RE-1 CB1 H	F2	RE-1 BSEL2 H	F2
OC-2 LWCR L	H2	RE-1 BSEL1 H	H2
OC-1 RDB L	J2	RE-1 BSEL0 H	J2
RE-1 DB0 H	K2	CB-1 WR9 H	K2
OC-2 CCAR L	L2	RE-1 DB11 H	L2
RE-1 FR3 L	M2	RE-1 DEN5 H	M2
OC-2 IBCM L	N2	OC-2 AC ENABLE L	N2
OC-2 CLF L	P2	OC-2 B TP3 H	P2
SC-1 CONTROL BSY L	R2	OC-2 RFSR L	R2
OC-2 SBRM L	S2	OC-2 RCMR L	S2
OC-2 LDBR L	T2	RE-1 DB4 H	T2
Not used	U2	Not used	U2
Not used	V2	Not used	V2

Table F-4
TM8-E M8327 Register Module, Edge Connector Signals

To M8322 Connector E		To M8321 Connector F		To M8321 Connector H		To M8322 Connector J	
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.
OC-2 LDBR L	A1	Not used	A1	CB-2 MAC 2 H	A1	SC-2 RD 6 H	A1
OC-2 SBRM L	B1	OC-2 RWCR L	B1	RE-1 SEL16 H	B1	CB-1 COUNT WC L	B1
CB-1 WDR H	C1	RE-1 DB7	C1	RE-1 PEVN H	C1	CB-2 MAC 1 H	C1
OC-2 CLF L	D1	RE-1 FR0 H	D1	SC-1 SET H	D1	OC-2 LCMR L	D1
SC-1 SET H	E1	RE-1 DB5	E1	Not used	E1	RE-1 SEL16 H	E1
RE-1 ENABLE CHECK CHAR L	F1	CB-1 WR 1st 7 H	F1	RE-1 DB8 H	F1	IEEF L	F1
SC-2 RD1 H	H1	Not used	H1	Not used	H1	RE-1 IEEF L	H1
SC-2 ERROR L	J1	RE-1 DB3	J1	RE-1 DB9 H	J1	SC-1 COUNT CA L	J1
RE-1 SEL2 H	K1	RE-1 DB2	K1	Not used	K1	Not used	K1
RE-1 SEL1 H	L1	Not used	L1	RE-1 DB10 H	L1	Not used	L1
CB-3 LBCM L	M1	CB-3 MTTF L	M1	Not used	M1	CB-1 WR 9 H	M1
RE-1 B SEL0 H	N1	SC-2 ERROR L	N1	CB-1 WR 2nd 7 H	N1	OC-2 LCM/F/DB H	N1
RE-2 CAO H	P1	OC-2 LCAR L	P1	RE-1 DEN 8 H	P1	Not used	P1
SC-2 RD 2 H	R1	SC-1 TUR L	R1	RE-1 FR1 H	R1	OC-1 RC ERROR L	R1
CB-2 DB MPXB H	S1	OC-2 LCMR L	S1	RE-1 FR2 H	S1	OC-2 RMSR L	S1
SC-2 RD3 H	T1	CB-3 CLR ALL L	T1	OC-2 CWCR L	T1	CB-2 WR 2nd 7 H	T1
SC-2 RDP H	U1	OC-2 LCM/F/DB H	U1	OC-2 RMSR L	U1	CB-3 CLR ALL L	U1
SC-2 RD5 H	V1	OC-2 LFGR L	V1	OC-2 RCAR L	V1	CB-1 WR 1st 7 H	V1
Not used	A2	Not used	A2	Not used	A2	Not used	A2
Not used	B2	Not used	B2	Not used	B2	Not used	B2
SC-1 CONTROL BSY L	C2	RE-1 DB6	C2	CB-1 WR 7 H	C2	RE-1 EMA INC ENABLE L	C2
OC-2 IBCM L	D2	Not used	D2	Not used	D2	CB-2 DBC1 L	D2
SC-1 TUR L	E2	OC-1 RC ERROR L	E2	CB-3 INIT H	E2	RE-1 DEN 5 H	E2
SC-1 EMA INC L	F2	RE-1 DB1	F2	RE-1 B SEL 2 H	F2	OC-2 RFSR L	F2
SC-2 RD 0 H	H2	OC-2 LWCR L	H2	RE-1 B SEL 1 H	H2	SC-2 RD 4 H	H2
Not used	J2	OC-1 RD B L	J2	RE-1 B SEL 0 H	J2	CB-3 MTTF L	J2
SC-1 7 CHANNEL H + DEN 5 H	K2	RE-1 DB0	K2	CB-1 WR 9 H	K2	RE-1 GO H	K2
SC-2 RD 7 H	L2	OC-2 CCAR	L2	RE-1 DB11 H	L2	RE-2 EMA 7 H	L2
RE-1 B SEL 0 H	M2	RE-1 FR3 H	M2	RE-1 DEN 5 H	M2	CB-2 MAC 2 H	M2
RE-1 SEL H	N2	OC-2 IBCM	N2	OC-2 AC ENABLE L	N2	RE-1 FR2 H	N2
CB-2 DBC 2 L	P2	OC-2 CLF	P2	OC-2 BTP 3 H	P2	RE-1 FR0 H	P2
RE-2 WCO H	R2	SC-1 CONTROL BSY	R2	OC-2 RFSR L	R2	RE-1 FR1 H	R2
RE-1 DBC 1 H	S2	OC-2 SBRM	S2	OC-2 RCMR L	S2	CB-3 INIT H	S2
CB-2 DB MPX A H	T2	OC-2 LDBR	T2	RE-1 DB4 H	T2	RE-1 DEN 8 H	T2
Not used	U2	Not used	U2	Not used	U2	Not used	U2
Not used	V2	Not used	V2	Not used	V2	Not used	V2

Table F-5
TM8-E M8322 Control Module, Edge Connector Signals

To M8327 Connector E		To M8323 Connector F		To M8323 Connector H		To M8327 Connector J	
Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.
SC-2 RD3 H	T1	SC-1 PRESET H	T1	CB-1 SP REV L	T1	CB-1 WR 2nd 7 H	T1
SC-2 RDP H	U1	SC-1 TUR L	U1	CB-1 REWIND L	U1	CB-3 CLR ALL L	U1
SC-2 RD5 H	V1	SC-1 FM L	V1	CB-1 BRK RQST H	V1	CB-1 WR 1st 7 H	V1
Not used	A2	SC-1 Test	A2	Not Used	A2	Not used	A2
Not used	B2	Not used	B2	Not used	B2	Not used	B2
SC-1 CONTROL BSY L	C2	SC-1 SDWN L	C2	RE-1 DEN 8 H	C2	RE-1 EMA INC ENABLE L	C2
OC-2 IBCM L	D2	CB-2 CHG DIR L	D2	OC-2 RMSR L	D2	CB-2 DBC 1 L	D2
SC-1 TUR L	E2	SC-2 RDP H	E2	OC-1 RC ERROR L	E2	RE-1 DEN 5 L	E2
SC-1 EMA INC L	F2	SC-2 RD5 H	F2	OC-2 LCM/F/DB H	F2	OC-2 RFSR L	F2
SC-2 RD0 H	H2	SC-2 RD3 H	H2	RE-2 EMA 7	H2	SC-2 RD4 H	H2
Not used	J2	SC-2 RD2 H	J2	SC-1 COUNT CA L	J2	CB-3 MTTF L	J2
SC-1 7 CHANNEL H + DEN 5 L	K2	RE-2 CA0 L	K2	RE-2 GO H	K2	RE-1 GO H	K2
SC-2 RD7 H	L2	SC-1 RD7 H	L2	SC-2 RD4 H	L2	RE-2 EMA 7 H	L2
RE-1 B SEL1 H	M2	SC-2 RD1 H	M2	OC-2 RFSR L	M2	CB-2 MAC 2 H	M2
RE-1 B SEL0 H	N2	Not used	N2	RE-1 DEN 5 H	N2	RE-1 F2 H	N2
CB-2 DBC 2 L	P2	SC-2 RD0 H	P2	RE-1 EMA INC ENABLE L	P2	RE-1 FR0 H	P2
RE-2 WCO L	R2	SC-1 EMA INC L	R2	RD6 H	R2	RE-1 FR1 H	R2
OC-2 LDBR L	A1	SC-2 ERROR L	A1	CB-1 R/RC H	A1	SC-2 RD6 H	A1
OC-2 SBRM L	B1	SC-1 DATA LATE L	B1	RE-1 WR/WFM	B1	CB-1 CONT WC L	B1
CB-1 WDR L	C1	CB-3 CLR STATUS L	C1	CB-2 R/RCAFT WR	C1	CB-2 MAC1 H	C1
OC-2 CLF L	D1	CB-1 OFF LINE	D1	Not used	D1	OC-2 LCMR L	D1
SC-1 SET H	E1	CB-2 BTP3 H	E1	Not used	E1	RE-1 SEL 16 H	E1
RE-1 ENABLE CHECK CHAR L	F1	CB-1 SPACE H	F1	SC-1 RDS · R + RCH	F1	RE-1 IEEF	F1
SC-2 RD1 H	H1	CHG TRANS L	H1	SC-1 WRS H	H1	RE-1 IEMF	H1
SC-2 ERROR L	J1	SC-2 EOT L	J1	CB-1 WCOV H	J1	SC-1 COUNT CA L	J1
RE-1 SEL0 H	K1	CB-3 MTTF L	K1	SC-1 SET H	K1	Not used	K1
RE-1 SEL1 H	L1	Not used	L1	SC-2 B LRCS L	L1	Not used	L1
CB-3 LBC M L	M1	SC-2 REWINDING L	M1	CB-2 MAC ACC L	M1	CB-1 WR9 H	M1
RE-1 B SEL 0 H	N1	SC-2 BOT L	N1	SC-1 7 CHANNEL + DEN 5 L	N1	OC-2 LCM/F/DB H	N1
RE-2 CA 0 L	P1	CB-3 SEL ERROR L	P1	CB-3 BTP4 H	P1		P1
SC-2 RD2 H	R1	SC-1 WRS L	R1	CB-3 CLR ALL	R1	OC-1 RC ERROR L	R1
CB-2 DB MPX B H	S1	SC-1 SELR L	S1	SC-1 RECORD LENGTH INCORRECT H	S1	OC-2 RMSR L	S1
RE-1 DBC 1 H	S2	OC-2 IBCM L	S2	Not used	S2	CB-3 INIT H	S2
CB-2 CB MPX A H	T2	CONTROL BSY H	T2	SC-2 SP REV · BOT H	T2	RE-1 DEN 8 H	T2
Not used	U2	Not used	U2	Not used	U2	Not used	U2
Not used	V2	Not used	V2	Not used	V2	Not used	V2

Table F-6
TM8-E M8323 Transport Status and Control Module, Edge Connector Signals

To M8322 Connector H		To M8322 Connector F	
Signal	Pin No.	Signal	Pin No.
CB-1 R/RC H	A1	SC-2 ERROR L	A1
RE-1 WR/WFM	B1	SC-1 DATA LATE L	B1
R/RC AFT WR	C1	CB-3 CLR STATUS L	C1
Not used	D1	CB-1 OFF LINE L	D1
Not used	E1	CB-2 B TP 3 H	E1
SC-1 RDS · R + RCH	F1	CB-1 SPACE H	F1
SC-1 WRS H	H1	CB-3 CHG TRANS L	H1
CB-1 WCOV H	J1	SC-2 EOT L	J1
SC-1 SET H	K1	CB-3 MTTF L	K1
SC-2 B LRCS L	L1	Not used	L1
CB-2 MAC ACC L	M1	SC-2 REWINDING L	M1
SC-1 7 CHANNEL + DEN 5 L	N1	SC-2 BOT L	N1
CB-3 BTP4 H	P1	CB-3 SEL ERROR L	P1
CB-3 CLR ALL	R1	SC-1 WRS L	R1
SC-1 RECORD LENGTH INCORRECT H	S1	SC-1 SELR L	S1
CB-1 SP REV L	T1	SC-1 PRESET H	T1
CB-1 REWIND L	U1	SC-1 TUR L	U1
CB-1 BRK RQST H	V1	SC-1 FM L	V1
Not used	A2	SC-1 Test	A2
Not used	B2	Not used	B2
RE-1 DEN 8 H	C2	SDWN L	C2
OC-2 RMSR L	D2	CB-2 CHG DIR L	D2
OC-1 RC ERROR	E2		
OC-2 LCM/F/DB H	F2	SC-2 RDP H	E2
RE-2 EMA 7 L	H2	SC-2 RD 5 H	F2
SC-1 COUNT CA L	J2	SC-2 RD 3 H	H2
RE-2 GO H	K2	SC-2 RD 2 H	J2
SC-2 RD 4 H	L2	SC-1 RD 7 H	L2
OC-2 RFSR L	M2	SC-2 RD 1 H	M2
RE-1 DEN 5 H	N2	Not used	N2
RE-1 EMA INC ENABLE L	P2	SC-1 RD 0 H	P2
SC-2 RD 6 H	R2		
Not used	S2	SC-1 EMA INC L	R2
SC-2 SP REV BOT H	T2	OC-2 LBCM L	S2
Not used	U2	SC-1 CONTROL BSY H	T2
Not used	V2	Not used	U2
		Not used	V2

Table F-7
TM8-E Signals and Signal Functions

Signal	Origin	Function
BAC 0 – BAC 11	Processor AC	A 12-bit data word transferred from the processor AC to load TM8-E registers.
OC-2 AC ENABLE	M8321	AC ENABLE is asserted any time a 670X instruction is executed to enable bits on the Data Bus to be applied to the TM8-E registers.
C BOT	TS03	BOT indicates the reflective strip at the beginning of the tape is being sensed by the tape transport. If the transport is rewinding or doing a space reverse operation when C BOT is asserted, the transport stops.
*BREAK CYCLE L	M8322	**
*BRK IN PROG L	M8322	**
*BRK RQST	M8322	The BRK RQST flip-flop is set by an SBRM instruction or during the write, read, and read/compare operations to initiate the single cycle data break and transfer data.
RE-1 B SEL 0 RE-1 B SEL 1 RE-1 B SEL 2	M8327	RE-1 B SEL 0 through RE-1 B SEL 2 are outputs of the Buffered Command Register applied to the TS03. They are compared with RE-1 SEL 0 through RE-1 SEL 2 on the M8323 module; if they are different, the CB-2 CHG TRANS L signal is asserted.
*BUS STROBE	Processor M8323	***
OC-2 CCAR	M8321	OC-2 CCAR is asserted when a 6702 instruction is executed to clear the CA Register.
*C0 and C1	M8321	**
OC-2 CLF	M8321	Clear all Flags (CLF) is asserted when the 6725 instruction is executed to clear the TM8-E and the Transport Master System Register if tape unit is ready (TUR). If tape unit is not ready, clear status register, MTTF, and ERROR flag.

*Omnibus signals.
**Refer to Table 9-3, *PDP-8/E & PDP-8/M Small Computer Handbook.*
***Refer to Table 9-2, *PDP-8/E & PDP-8/M Small Computer Handbook.*

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
CB-3 CLR ALL L	Processor M8322 M8321	Signal asserted by INIT from processor, SC-1 TUR AND OC-2 CLF, OC-1 CLT, and the INITIALIZE instruction to clear all TM8-E and TS03 Master System registers.
CB-3 CLR STATUS	M8322	CB-3 CLR STATUS is asserted to clear the status registers, ERROR flag, and MTTF if a CLF instruction is executed and C TUR is not asserted by the transport.
SC-1 CONTROL BSY	M8323	The Control Busy flip-flop is set by an RE-1 GO command at the Command Register (bit 5 = 1) on the next TP4 time and cleared by MTTF.
SC-1 COUNT CA L	M8323	SC-1 COUNT CA L is asserted at break request time. If the Read/Compare (R/C) Error flag is set to stop incrementing the CA Register, the address of the data that produced a Read/Compare error is left in the CA Register.
C REV H	M8321	C REV H is asserted by the space reverse function.
CB-2 CHG DIR L	M8322	The change direction flip-flop is set any time a change in direction is sensed.
C SDWN L	TS03	Tape settling down (C SDWN L) is asserted 2.3 ms after the MTTF flag sets for 10 ms.
C LRCS L	TS03	LRC strobe (C LRCS) is asserted by the TS03 when a LRC character is read from the tape.
C CRCS L	TS03	CRC Strobe (C CRCS) is asserted when a CRC character is read from tape.
C VPE L	TS03	Vertical Parity Error (C VPE L) is asserted when the TS03 detects a vertical parity error to set the VPE flip-flop.
C CRCE L	TS03	Cyclic redundancy check error (C CRCE L) is asserted when the TS03 detects a CRC error.
C LRCE L	TS03	Longitudinal redundancy check error (C LRCE L) is asserted when the TS03 detects an LRC error.
C SELR L	TS03	Select remote (C SELR L) is asserted when the transport is selected and on-line. Other status signals are not valid until C SELR L is asserted.
C SEL 16 H	M8327	For future use.

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
C FWD H	M8321	C FWD H is asserted by read, read/compare, write, write File Mark, and space forward functions.
C RWS L	TS03	Rewind status (C RWS L) is asserted any time the selected transport is rewinding.
C CRCE	TS03	The CRC Error (CRCE) is set when the TS03 detects a CRC error.
CB-3 T INIT L	M8322	T INIT (tape initialize) is asserted by space reverse at BOT, select error, and CLR ALL L.
C INIT L	M8321	C INIT L (initialize transport) is asserted by INIT from processor.
C SET H		SET (C SET H) is generated by the TM8-E to initiate transport operation.
C REW H	M8321	C REW H is asserted when 1XXX is loaded into the Function Register and initiates the rewind operation. The three bits are decoded by the output control function decoder and applied to the tape transport. The transport rewinds to BOT and stops.
C WDR H	M8322	Write data ready (C WDR H) is asserted by SC-1 SET during a write operation and is negated when word count goes to zero by word count overflow (CB-1 WCOV).
C WFMK H	M8321	Write File Mark (C WFMK) is asserted when 5XXX is loaded into the Function Register. The 3 bits (FR0–FR2) are decoded by the output function decoder, and C WFMK is asserted to cause the TS03 to write the End of File Mark (EOF).
C WRE H	M8321	Write enable (C WRE H) is asserted to inform the TS03 that the TM8-E is ready to write, write File Mark, or rewind.
C WD0 H C WD1 H C WD2 H C WD3 H C WD4 H C WD5 H C WD6 H C WD7 H	M8321	C WD0 H through C WD7 H are data bits to be written on tape during a Write operation. C WD0 H and C WD1 H are zero values in the core dump mode.

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
C WXG H	M8321	Extended Gap (C WXG H) is asserted when bit 3 in the Function Register is a 1 to cause the transport to leave a 3-inch gap between records.
SC-1 DATA LATE L	M8323	SC-1 DATA LATE L is asserted when the computer fails to service a BRK RQST before the next data transfer to or from tape.
C RD0 L C RD1 L C RD2 L C RD3 L C RD4 L C RD5 L C RD6 L C RD7 L	TS03	C RD0 L through C RD7 L are data bits read from the tape during a read or read/compare operation. C RD0 and C RD1 are zero values in the Core Dump Mode.
C PEVN L	M8321	C PEVN L is asserted when bit 3 in the Command Register is a 1 to select odd parity. Even parity operation on 9-track tapes causes a 1 to be written on channel 3 (on the Parity track) if Data is all 0s.
C RDS L	TS03	Read Strobe (C RDS L) is a 100-ns pulse asserted by the TS03 each time a data character is read from DECmagtape.
C TUR L	TS03	Tape unit ready (C TUR L) is asserted by the TS03 when the selected tape unit is ready.
C 7 CH L	TS03	Not used in TM8-M System. Remains negated.
CB-3 CHG TRANS L	M8322	The CB-3 CHG TRANS flip-flop sets and asserts CB-3 CHG TRANS L when RE-1 BSEL 0 through RE-1 BSEL 2 from the Buffered Command Register and RE-1 SEL 0 through RE-1 SEL 2 are different. CB-3 CHG TRANS is cleared by the next SC-1 SET Pulse.
CPMA DISABLE	M8322	*
OC-1 R/C ERROR L	M8321	The OC-1 R/C Error flag is set to assert OC-1 R/C ERROR if an error occurs during a read/compare operation (data read from DECmagtape is different from data in memory).

*Refer to Table 9-3, *PDP-8/E & PDP-8/M Small Computer Handbook.*

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
RE-1 DB00–RE-1 DB11	M8327	RE-1 DB 00 through RE-1 DB 11 is a 12-bit word from the Data Register which could be data read from tape, data from the AC, or data from the Memory Data lines. The input to the Data Register is controlled by a data multiplexer on the input of the Data Register. These bits are applied to the read/compare error detection logic to compare them with memory data during a read/compare operation.
CB-2 DB MPX A L	M8322	Selects data for input to the Data Register (Table 9-2).
CB-2 DB MPX B L	M8322	Selects data for input to the Data Register (Table 9-2).
RE-1 DEN 5 H (bit 10)	M8321	See Table 8-1 for this function bit.
RE-1 DEN 8 H	M8321	See Table 8-1 for this function bit.
RE-1 IEEF	M8327	Enable Interrupt when ERROR flag (RE-1 IEEF) is asserted if bit 4 in the Command Register is a 1.
RE-1 IEJF	M8327	Enable Interrupt when JOB DONE (RE-1 IEJF) is asserted if bit 5 in the Command Register is a 1.
RE-1 EMA 0 RE-1 EMA 1 RE-1 EMA 2	M8327	RE-1 EMA 0 through RE-2 EMA 2 are used to address extended memory (Table 7-1). Bit 6 in the Function Register must be a 1 to use extended memory addressing.
RE-2 EMA 7 INC ERR L	M8327	RE-2 EMA 7 INC ERR L is asserted when the program tries to increment beyond memory fields 7 and sets bit 8 in the Second Status Register.
RE-1 EMA INC EN L	M8327	Extended memory address increment (RE-1 EMA INC EN L) is asserted when bit 6 in the Function Register is a 1 to allow memory to be treated as a continuous memory rather than 4 K blocks.
RE-1 ENAB CHK CHAR L	M8327	Enable check character (RE-1 ENAB CHK CHAR L) is asserted and sets bit 4 of the Second Status Register if bit 4 of the Function Register is a 1 to read the CRC and LRC character.

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
SC-2 EOT L	TS03	End of Tape (SC-2 EOT) is asserted if the EOT reflective strip is sensed by the selected transport. C EOT sets bit 8 of the Main Status Register.
SC-2 ERROR L	M8323	The SC-2 ERROR flag is set by any one of the following conditions: EOT R/C ERROR PARITY ERROR BOT EMA 7 INC ERR REC LENGTH INCORRECT DATA LATE EOF ILLEGAL FUNCTION SELECT ERROR The Error flag allows the skip line to be grounded if the SKEF instruction is executed by the program.
RE-1 FR0–FR2	M8327	Function bits FR0 through FR2 are decoded by function decoders in the TM8-E output control module and TM8-E control module to determine TS03 DECmagtape functions and generate TM8-E control signals (Table 8-1).
RE-1 GO	M8327	RE-1 GO is asserted when bit 5 in the Function Register is a 1. RE-1 GO must be a 1 to allow tape operation to start.
SC-2 ILLEGAL FUNCTION	M8323	SC-2 ILLEGAL FUNCTION is asserted by any of the conditions listed in Table 8-2 to set bit 11 in the Main Status Register.
INT STROBE H	Processor	*
INT I/O L	M8321	**
INIT	Processor	*Clears all flags in the TM8-E and TS03. It is asserted by pressing the CLEAR key on the front panel or by a 6007 IOT instruction.

*Refer to Table 9-3, *PDP-8/E & PDP-8/M Small Computer Handbook.*
**Refer to Table 9-1, *PDP-8/E & PDP-8/M Small Computer Handbook.* } Omnibus signals

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
*CB-3 INT RQST L	M8322	CB-3 INT RQST L is asserted by one of the following conditions: Bit error in the Command Register is a 1 and the SC-2 ERROR flag is set. Bit 5 in the Command Register is a 1 and the JOB DONE (CB-3 MTTF) flag is set.
*I/O PAUSE L	M8321	*
C LRCE L	TS03	LRC ERROR (C LRCE L) is set by the TS03 when a LPE is detected by the Master System.
OC-2 LWCR L	M8321	OC-2 LWCR is asserted to load the WC Register when a 6701 instruction is executed by the program.
OC-2 LDBR	M8321	Load Data Buffer (OC-2 LDBR) is asserted when a 6707 instruction is executed by the program to transfer the contents of the AC to the Data Buffer Register. This instruction also sets CB-3 MTTF (JOB DONE).
MA0–MA11	Omnibus**	MA0 through MA11 are used to address 4096 possible memory locations. During a data break, the CA Register controls the MA lines to select a memory location for a data transfer between memory and the DECmagtape.
CB-2 MAC ACC L	M8322	CB-2 MAC ACC is asserted when a BRK RQST is granted to enable the data transfer and clear BRK RQST.
SC-2 NOT LAST XFER L	M8322	**
MD0–MD11	Processor	***
MSIR DISABL	M8322	****
CB-1 OFFLINE L	M8322 and M8321	CB-1 OFFLINE is asserted when 0XXX is loaded into the Function Register by a LFGR instruction and the selected transport rewinds to beginning of tape and stops. The transport must be manually reset to on-line condition.
SC-1 PARITY ERROR L	M8323	The SC-1 PARITY ERROR flip-flop is set when an LRC, CRC, or VPE error is detected by the selected tape transport.

*Refer to Table 9-1, *PDP-8/E & PDP-8/M Small Computer Handbook.*
**Refer to Table 9-2, *PDP-8/E & PDP-8/M Small Computer Handbook.*
***Refer to Table 9-4, *PDP-8/E & PDP-8/M Small Computer Handbook.*
****Refer to Table 9-3, *PDP-8/E & PDP-8/M Small Computer Handbook.*

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
RE-1 PEVN H	M8327	If RE-1 PEVN is high, the TS03 generates and checks for even parity; if it is low, the TS03 generates and checks for odd parity. The level of RE-1 PEVN is controlled by bit 3 of the Command Register (when bit 3 is a 1, RE-1 PEVN is low).
*POWER OK H	Processor	POWER OK goes high when a PDP-8 power failure occurs and generates a CB-3 CLR ALL to stop all transports and end any operation occurring at the time of a power failure.
SC-1 PRESET H	M8323	SC-1 PRESET H is a 2.5 μs pulse that is triggered by setting the RE-1 GO bit in the Function Register to a 1 if the selected transport is ready (C TUR is true). RE-1 PRESET H triggers the RE-1 SET pulse.
RE-1 RCAR L	M8321	Read CA Register (RE-1 RCAR) is asserted when the 6713 instruction is executed by the program to transfer the contents of the CA Register to the AC.
OC-1 RDB L	M8321	Read Data Buffer (OC-1 RDB) is asserted by an RDBR instruction or by CB-2 MAC 1 H during a read data break to transfer the contents of the Data Buffer Register to the data lines.
RE-1 RDBR L	M8321	Read Data Buffer Register (RE-1 RDBR) is asserted when a 6717 instruction is executed by the program to ground OC-1 RDB L and transfer the contents of the Data Buffer Register to the AC.
SC-1 RECORD LENGTH INCORRECT H	M8323	SC-1 RECORD LENGTH INCORRECT is asserted and sets bit 6 in the Main Status Register if the record length differs from the WC Register. The WC Register must be read by the program to determine if the record was too short or too long.
RE-1 REWIND	M8321	RE-1 REWIND is asserted by the function decoders if a 1XXX is loaded into the three most significant bits of the Function Register.
RE-1 RFSR L	M8321	RE-1 RFSR is asserted when a 6716 instruction is executed to transfer the contents of the Second Status Register and Function Register to the AC.
OC-2 RMSR L	M8321	OC-2 RMSR is asserted when a 6714 instruction is executed by the program to transfer the contents of the Main Status Register to the AC.

*Omnibus signals.

Part II

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
OC-2 RWCR L	M8321	OC-2 RWCR is asserted when a 6711 instruction is executed by the program to transfer the contents of the WC Register to the AC.
RE-1 SEL 0 H RE-1 SEL 1 H RE-1 SEL 2 H	M8327	RE-1 SEL 0 through RE-1 SEL 2 are loaded into the three most significant bit positions of the Command Register by an LCMR instruction. These bits are used to select one of the two transports for a data transfer operation (Table 7-1).
SC-1 SET H	M8323	SC-1 SET H is approximately a 5 μs pulse that is triggered by setting the GO bit in the Function Register to 1. SC-1 SET H is applied to the selected transport to start tape movement if TUR is true (tape unit ready).
OC-2 SKIP L	M8321	The OC-2 skip line is grounded when one of the following conditions exist: SKEF instruction is executed and the SC-2 Error flag is set. SKCB instruction is executed and SC-1 CONTROL BSY is not set. SKTR instruction is executed and C TUR is asserted. SKJD instruction is executed and the JOB DONE (CB-3 MMTF) flag is set.
CB-1 SPACE H	M8322	CB-1 SPACE H is asserted during space reverse or space forward operation and continued until EOT, FMK, or WCOV, is encountered. File Mark is read from the tape.
CB-1 SP FWD L	M8322	CB-1 SP FWD is asserted when 6XXX is loaded into the three most significant bit positions of the Function Register. The transport spaces forward the number of records specified by the WC Register.
CB-1 SP REV L	M8322	CB-1 SP REV is asserted when 7XXX is loaded into the three most significant bit positions of the Function Register. The transport spaces in reverse the number of records specified by the WC Register.

Table F-7 (Cont)
TM8-E Signals and Signal Functions

Signal	Origin	Function
SC-1 SELR L	M8323	Select remote (SC-1 SELR L) indicates to the control that the selected transport is on-line.
OC-2 SBRM L	M8321	Set BRK RQST Maintenance (OC-2 SBRM) is asserted when a 6727 instruction is executed by the program to initiate one single cycle data break.
SC-1 TUR L	TS03 and M8322	Tape unit ready (SC-1 TUR L) is asserted when the selected tape transport is ready.
RE-2 WC0L	M8327	Word count 0 (WC0) is asserted when the WC Registers read all 0s to indicate the data transfer is complete. RE-2 WC0 is used to generate CB-1 WCOV (word count overflow).
CB-1 WCOV L	M8322	Word count overflow (RE-2 WCOV) is asserted when the WC Register contains all 0s to negate C WDR and end a data transfer operation.
CB-1 WR 9 L	M8322	Enables logic to apply 8 bits of data to the selected transport during a write operation.
CB-1 WR 1st 7 L	M8322	Enables the logic to apply the six most significant bits of a 12-bit data word from memory to the selected transport during a write operation. Tracks 0 and 1 are 0s in the Core Dump Mode.
CB-1 WR 2nd 7 L	M8322	Enables logic to apply the six least significant bits of a 12-bit data word to the selected transport during a write operation. Tracks 0 and 1 are 0s in the Core Dump Mode.
SC-1 WRS L	TS03	Write strobe (SC-1 WRS) is asserted by C WRS from the TS03 when the selected transport is ready to write new data: C WRS is a 100 ns pulse that is asserted once for each character written on tape.

APPENDIX G
SPARE PARTS

Table G-1 lists the recommended spare parts for the TM8-E.

Table G-1
TM8-E Spare Parts

DEC Part Number	Description	Quantity
10-00007	Capacitor, 15 pF, 100V	1
10-00042	Capacitor, 1000 pF, 100V	1
10-00067	Capacitor, 618 pF, 35V	2
10-01610	Capacitor, 0.01 μF, 100V	2
12-09941	Connector, 40 pins	1
13-00204	Resistor, 47Ω, ¼W	1
13-00229	Resistor, 100Ω, ¼W	1
13-00275	Resistor, 220Ω, ¼W	2
13-00286	Resistor, 270Ω, ¼W	2
13-00293	Resistor, 330Ω, ¼W	3
13-00317	Resistor, 470Ω, ¼W	3
13-00443	Resistor, 417Ω, ¼W	1
13-00498	Resistor, 18 KΩ, ¼W	1
13-00534	Resistor, 100 KΩ, ¼W	1
13-01316	Resistor, 8.2 KΩ, ¼W	1
13-01401	Resistor, 750Ω, ¼W	3
13-01420	Resistor, 27Ω, ¼W	1
15-10015	IC, DEC 4008	2
19-05547	IC, DEC 7474	2
19-05575	IC, DEC 7400	2
19-05576	IC, DEC 7410	2
19-05578	IC, DEC 7430	1
19-05570	IC, DEC 7401	2
19-09004	IC, DEC 7402	2
19-09055	IC, DEC 7495	1
19-09056	IC, DEC 74H00	1
19-09057	IC, DEC 74H10	1
19-09058	IC, DEC 74H21	1
19-09267	IC, DEC 74H11	3
19-09485	IC, DEC 380	3

Table G-1 (Cont)
TM8-E Spare Parts

DEC Part Number	Description	Quantity
19-09486	IC, DEC 384	2
19-09584	IC, DEC 8251	1
19-09667	IC, DEC 74H74	1
19-09686	IC, DEC 7404	2
19-09704	IC, DEC 314	1
19-09705	IC, DEC 8881	3
19-09712	IC, DEC 8242	1
19-09928	IC, DEC 7416	1
19-09929	IC, DEC 7414	2
19-09935	IC, DEC 8235	2
19-09937	IC, DEC 74153	1
19-09955	IC, DEC 7412	1
19-10035	IC, DEC 74197	1
19-10435	IC, DEC 74123	1
19-10651	IC, DEC 74175	1
19-10652	IC, DEC 74174	1

APPENDIX H
IC DESCRIPTIONS

This appendix provides detailed descriptions of ICs used in the TM8-E. A detailed schematic plus a packaging diagram with pin number assignments, and a truth table are provided on each of the following ICs:

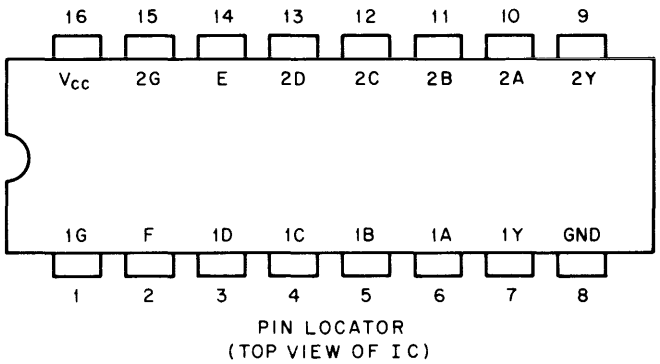
DEC 74153
DEC 74174
DEC 74175
DEC 74197

DEC 74153 IC

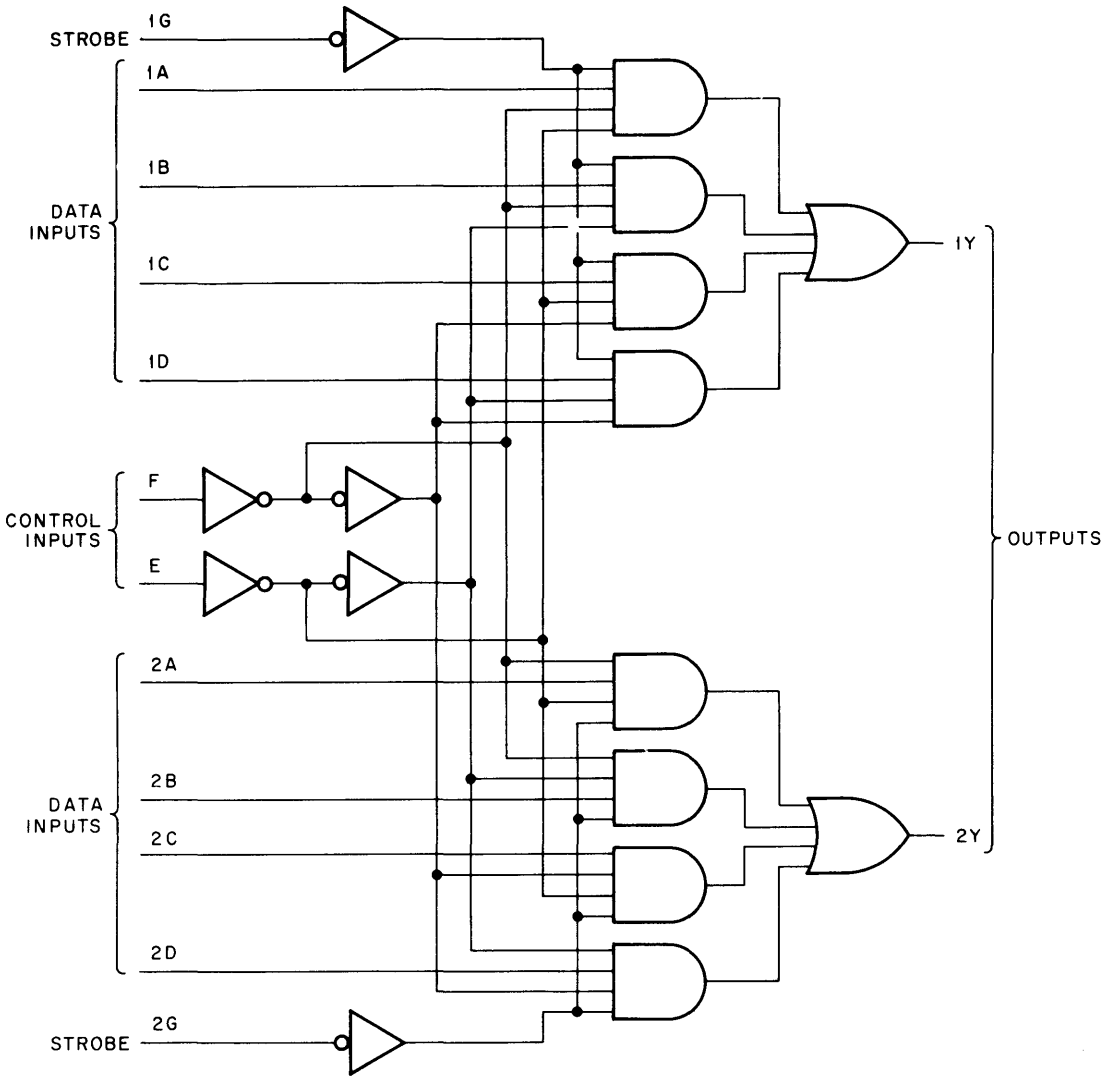
The DEC 74153 IC is a Dual 4-Line to 1-Line Data Selector/Multiplexer (see below for truth table, logic diagram, and pin numbers). The IC can be used in one of two modes, a 4-line to 1-line multiplexer or a parallel-to-serial converter. A strobe enable signal line is provided to select each of the input lines as an output. In the TM8-E, the strobe lines are tied together to allow the selection of signals from the MD lines, Data Bus, or data read from the TS03 Transport.

CONTROL INPUT		STROBE	OUTPUT
E	F	G	Y
LOW	LOW	LOW	A
HIGH	LOW	LOW	B
LOW	HIGH	LOW	C
HIGH	HIGH	LOW	D
DON'T CARE		HIGH	LOW

TRUTH TABLE (EACH HALF)



DEC 74153 IC (Sheet 1)



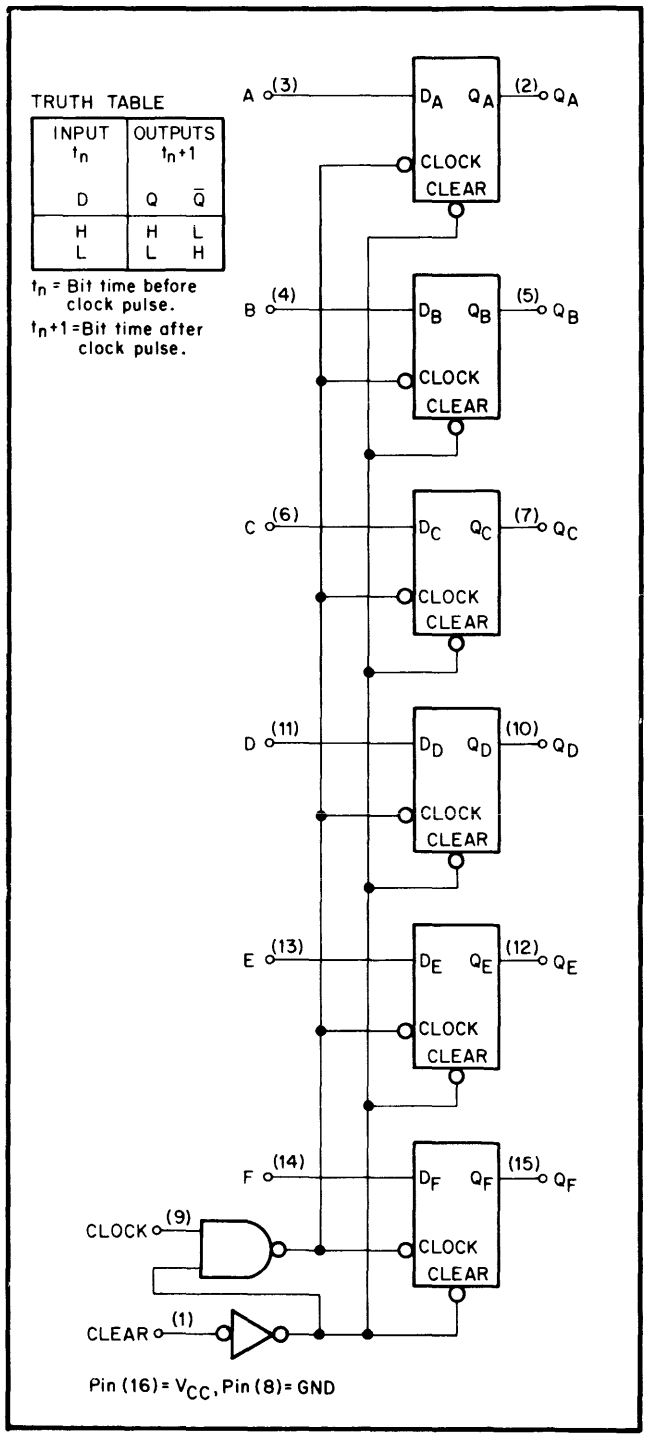
LOGIC DIAGRAM

DEC 74153 IC (Sheet 2)

DEC 74174 IC

The 74174 IC contains six flip-flops with single rail output with a buffered clock and direct clear input. Each flip-flop has an individual data input. The truth table and logic diagram are shown below.

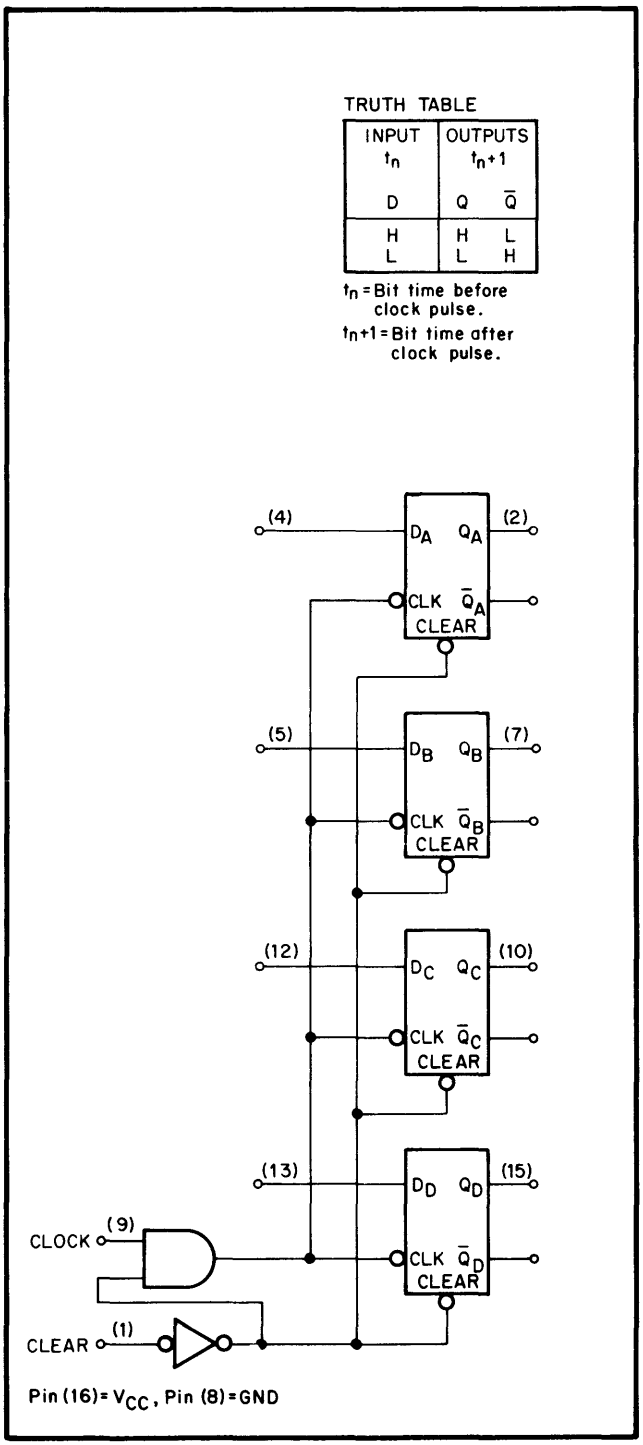
Input t_n	Outputs t_{n+1}	
D	Q	$\bar{Q}$
H	H	L
L	L	H



11-1112

DEC 74175 IC

The 74175 IC contains four flip-flops with double rail outputs with a buffered clock and direct clear input. Each flip-flop has an individual input. The truth table and logic diagram are shown below.



11-1113

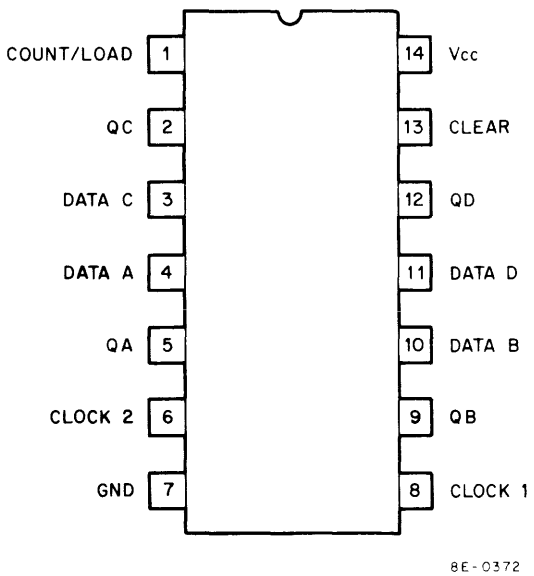
DEC 74197 IC

The DEC 74197 IC is a pre-settable binary counter that can also be used as a latch. The IC consists of four dc-coupled master-slave flip-flops connected to provide a divide-by-2 counter and a divide-by-8 counter. The logic diagram, a truth table, and a pin locator are shown in the 74153 description.

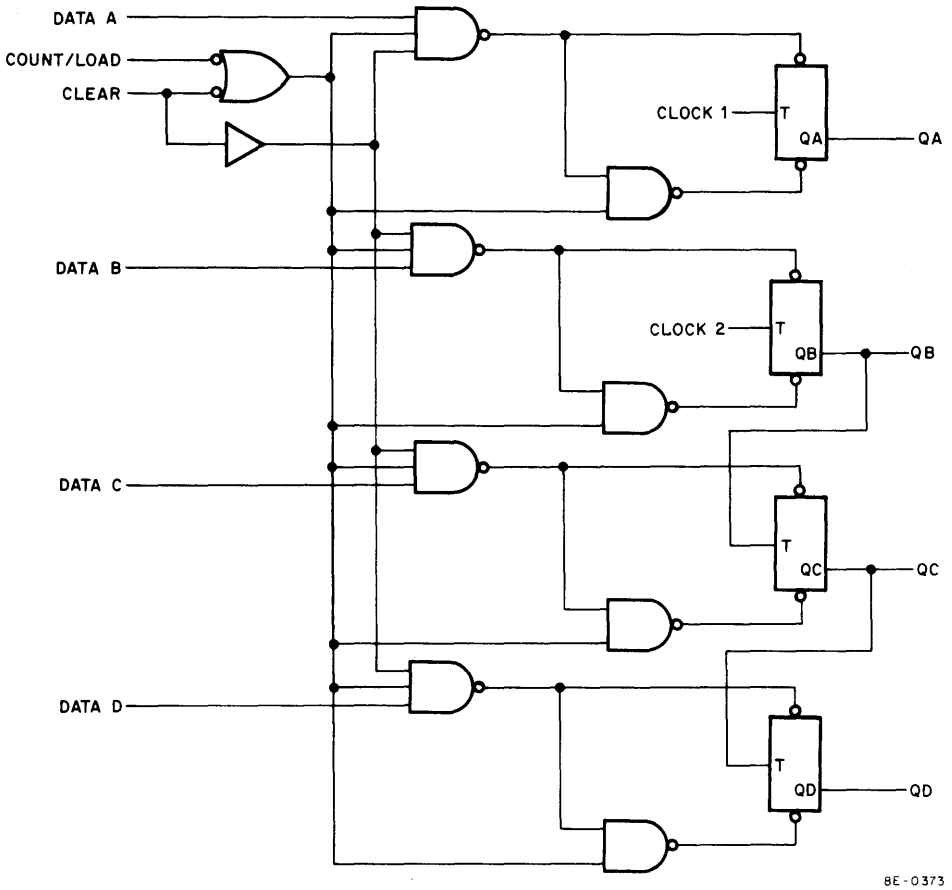
The 74197 can be used in any one of three modes, viz; the divide-by-2/divide-by-8 mode, requiring no external interconnection or IC pins, the latch mode, and the binary counter mode. If the first listed mode is used, an input at pin 8 is divided by 2 by flip-flop A and the result is taken from pin 5; an input at pin 6 is divided by 8 by flip-flops B, C, and D and the result is taken from pin 12. Transfer of information to the outputs takes place on the negative-going (trailing) edge of the clock pulse.

To use the latch mode, enter data at the four data inputs (pins 4, 10, 3, and 11) and enter a strobe pulse at pin 1. The output pins, 5, 9, 2, and 12, respectively, will follow the inputs when pin 1 is low, but will remain unchanged when pin 1 is high and the clock inputs are inactive.

Count Clock 1 Input	Output			
	QD	QC	QB	Q4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



DEC 74197 IC (Sheet 1 of 2)



DEC 74197 IC (Sheet 2 of 2)

APPENDIX I
TRANSPORT SIGNAL DESCRIPTIONS AND INTERFACE INFORMATION

I.1 INPUT SIGNALS

All commands from and to the input/output connector are preconditioned by loading the machine and placing it on-line using the front panel controls. The next commands set up the recorder.

I.1.1 Setup Commands

Signal	Pin No.	Description
Transport Select (SLT)	P1-J	A level that when true enables all the adapter drivers and receivers in the transport, thus connecting the transport to the controller. The transport must also be on-line, and SLT must be true for the entire write sequence (until tape motion stops). The SLT level may be removed to disconnect the machine from the system. The machine will remain in the last condition established by SWS.
Data Density Select (DDS) (Dual Density Only)	P1-D	Used when the TRANSPORT DENSITY SELECT switch is in the remote position. When true, this level selects the high read density (dual density).

I.1.2 Tape Motion Commands

Signal	Pin No.	Description
Overwrite (OVW) (Optional)	P1-B	A level that when true conditions appropriate circuitry in the transport to allow updating (rewriting) of a selected record. The transport must be in the write mode of operation to utilize the OVW feature.
Synchronous Forward Command (SFC)	P1-C	A level that when true, with the transport ready and on-line, causes tape to move forward at the specified speed. When the level goes false, tape motion ramps down and ceases.
Synchronous Reverse Command (SRC)	P1-E	A level that when true, with the transport ready and on-line, causes tape to move in a reverse direction at the specified speed. When the level goes false, tape motion ceases. If the load point marker is detected during an SRC, the SRC will be terminated. If an SRC is given when the tape is at the load point, it will be ignored.

Signal	Pin No.	Description
Rewind Command (RWC)	P1-H	A pulse input will rewind the tape past the load point and stop. The transport will then initiate a load forward sequence and return the tape to the load point marker. This input will be accepted only if the load point output is false. The transport may be taken off-line while rewind is still in process. Rewind will continue normally.

I.1.3 Write Commands

Signal	Pin No.	Description
Set Write Status (SWS)	P1-K	A level that must be true at the leading edge of an SFC (or RUN and FWD) when the write mode of operation is required, and must remain true for a minimum of 10 μs after the leading edge of the SFC (or RUN and FWD). SWS is sampled at the leading edge of the SFC or SRC (or RUN and FWD), toggling the read/write flip-flop to the appropriate state. Internal interlocks in the 9800/9700 will prevent writing in the reverse direction, when the write enable ring is missing, when the tape unit is off-line, when loading to a load point, and during a rewind.
Write Data Inputs		These are levels that if true at WDS time will result in a flux transition being recorded on tape (transport is in the write mode). Data inputs must have settled 0.5 μs before the leading edge of the WDS pulse and must remain quiescent 0.5 μs beyond the trailing edge of the WDS pulse. The CRCC is written by providing the correct data character together with a WDS four character times after the last data character of the record.
WDP	P2-L	
WD0	P2-M	
WD1	P2-N	
WD2	P2-P	
WD3	P2-R	
WD4	P2-S	
WD5	P2-T	
WD6	P2-U	The LRCC is written using the WARS signal. The LRCC can also be written by providing the correct data character together with a WDS. If the LRCC is written (DATA-WDS) in this manner, a WARS should be given one character time after the LRCC to ensure proper IRG erasure in case of data input error.
WD7	P2-V	
Write Data Strobe (WDS)	P2-A	A pulse of 2 μs nominal width for each character to be written. Writing occurs on the leading edge of the WDS. WDS may be a 1 μs minimum, 3 μs maximum pulse. Data inputs must have settled for at least 0.5 μs before the leading edge of WDS and remain quiescent for at least 0.5 μs beyond the trailing edge.
Write Amplifier Reset (LRC PLS)	P2-C	A pulse of 2 μs nominal width that, when true, resets the write amplifier circuits on the leading edge. The purpose of this line is to enable writing of the longitudinal redundancy check character (LRCC) at the end of a record. This ensures that all tracks are properly erased in an interrecord gap (IRG). The leading edge of the WARS pulse should be eight character times after the leading edge of the WDS associated with the last data character in the block (four character times after the CRCC is written).

I.1.4 Read Commands

A read-after-write machine will always have read selected. When write is selected (SWS), the data just written will be read back using a high threshold level on the read amplifiers. When SWS is false, the normal threshold is applied to the read amplifiers.

Signal	Pin No.	Description
Automatic Clipping Level Disable (ACLD)	P3-6	When true, this level overrides the automatic clipping level electronics and holds the read electronics in the normal clipping level.

I.1.5 Shutdown Commands

The use of a given magnetic tape unit may be terminated by an off-line command. Once this command is given, the tape unit may be returned to an adapter command only by operating the front panel ON LINE switch.

Signal	Pin No.	Description
Off-Line Command (OFFC)	P1-L	A level or pulse (minimum width 2 μs) that resets the on-line flip-flop to the zero state, placing the transport under manual control. It is gated only by SELECT in the transport logic, allowing an OFFC to be given while a rewind is in progress. An OFFC should be separated from a rewind command by at least 2 μs.

I.2 INTERFACE OUTPUT SIGNALS

All output signals are enabled only when the tape transport is on-line and selected.

I.2.1 Status Outputs

Signal	Pin No.	Description
On-Line (ONL)	P1-M	A level that is true when the on-line flip-flop is set. When true, the transport is under remote control. When false, the transport is under local control.
Transport Ready (RDY)	P1-T	A level that is true when the tape transport is on tape; that is, when the initial load sequence is complete and the transport is not rewinding. When true, the transport is ready to receive a remote command.
High Density Indicator (HDI) (Dual Density Only)	P1-F	A level that is true only when the high-density mode of operation is selected.
File Protect (FPT)	P1-P	A level that is true when a reel of tape without a write enable ring is mounted on the transport supply (or file) hub.
Write Enable (WEN)	P1-S	A level that is true when a reel of tape with a write enable ring is mounted on the transport supply (or file) hub. Opposite of file protect.

Signal	Pin No.	Description
Load Point (LDP)	P1-R	A level that is true when the load point marker is under the photosensor and the transport is not rewinding. After receipt of an SFC, the signal will remain true until the load point marker leaves the photosense area. (Circuitry using this output should not use the transitions to and from the true state.)
Tape Running (RNG)	P1-V	This is a level that is true when tape is being moved under capstan control and remains true until tape motion has ceased. (Includes forward, reverse, and rewind tape motion.)
End-of-Tape (EOT)	P1-U	A level that is true for the duration of the EOT marker. (Circuitry using this output should not use the transitions to and from the true state.)
Rewinding (RWD)	P1-N	A level that is true only when the transport is engaged in a rewind operation or returning to the load point. (Goes true approximately 5 μs after a rewind command is given.)

I.2.2 Read Outputs

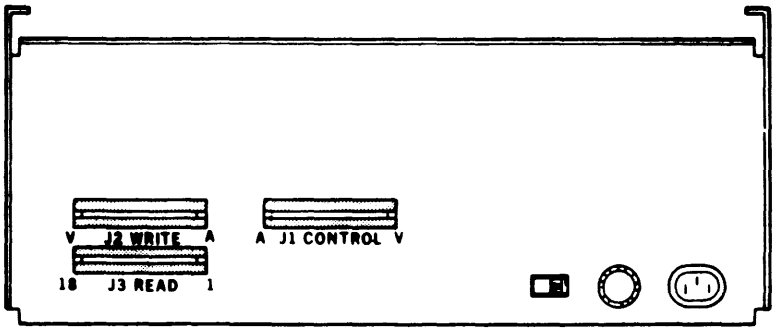
Read outputs are present at all times in tape units when a dual gap head is used (read after write). The high threshold level is selected internally when SWS is selected. In a read/write tape unit (single-gap head), read outputs are inhibited when SWS is true.

Signal	Pin No.	Description
Read Data Strobe (RDS)	P3-B	A pulse of 2 μs minimum width for each data character read from tape. Although the average time between two read data strobes is τ_1 (sec) = [1/s•d)] where s = tape speed in inches per second d = density characters per inch the minimum time between consecutive read data strobes is less than this figure due to skew and bit crowding effects. A guaranteed safe value for the minimum time is $1/2\ \tau_1$.
Read Gap Detect (RGAP)	P3-N	A level that is true approximately nine character spacings after the last data byte, and remains true until the first data byte of the subsequent data block. **NOTE** **This level will be true whenever tape motion is at rest.**

Signal	Pin No.	Description
Read Data Level		Nine staticisers are provided, which act as a one-stage read deskewing buffer. Each output is a level that changes to the appropriate state approximately 1 μs before the read data strobe and remains in that state until 1 μs before the next read data strobe. Data lines return to false condition in the IRG when tape motion stops, regardless of the last character read.
RDP	P3-1	
RD0	P3-3	
RD1	P3-4	
RD2	P3-8	
RD3	P3-9	
RD4	P3-1	
RD5	P3-1	It is recommended that read data strobes and the read gap detect be ignored during the first read or write operation from load point for τ_2 ms after the load point output goes false, where $\tau_2 = 1000/s$ (s = speed of tape unit).
RD6	P3-1	
RD7	P3-1	
		The read gap in a read-after-write tape unit is downstream from the write gap. Thus when the write gap is initially energized, the read gap may detect a flux change depending on the initial state of magnetism on the tape.

I.3 SUMMARY OF INTERFACE CHARACTERISTICS

Figure I-1 shows the location of connectors and pin numbers with signal names.



11-3059

→ INPUT
← OUTPUT

WRITE CONNECTOR J2

Active	Ground		Signal	Mnemonic
A	1	←	Write Data Strobe	REC
B	2		N. C.	
C	3	←	Write Amplifier Reset	LRC PLS
D	4		Not Used	
E	5		Not Used	
F	6		Not Used	
H	7		Not Used	
J	8		Not Used	
K	9		Not Used	
L	10	←	Write Data Channel P	WDP
M	11	←	Write Data Channel 0	WD0
N	12	←	Write Data Channel 1	WD1
P	13	←	Write Data Channel 2	WD2
R	14	←	Write Data Channel 3	WD3
S	15	←	Write Data Channel 4	WD4
T	16	←	Write Data Channel 5	WD5
U	17	←	Write Data Channel 6	WD6
V	18	←	Write Data Channel 7	WD7

CONTROL CONNECTOR J1

A	1		Spare	
B	2	←	Overwrite (Not Used)	OVERWRITE
C	3	←	Synchronous Forward	FWD MOT
D	4	←	Data Density Select	DDS (Not Used)
E	5	←	Synchronous Reverse	REV MOT
F	6	→	Data Density Indicator	DDI (Not Used)
H	7	←	Rewind Command	RWND PLS
J	8	←	Select	SEL DRIVE (1:0)
K	9	←	Set Write Status	WRE LTCH

CONTROL CONNECTOR J1 (Cont)

Active	Ground		Signal	Mnemonic
L	10	←	Off-Line Command	OFF LINE PLS
M	11	→	On-Line Command	DRIVE (0:1) ON LINE
N	12	→	Rewinding	RWNDG
P	13	→	File Protect	WRLCK
R	14	→	Load Point	LOAD POINT
S	15	→	Write Enable	WRITE ENB
T	16	→	Transport Ready	XPRT RDY
U	17	→	End-of-Tape	END OF TAPE
V	18	→	Tape Running	TAPE RUNNING
				STATUS (Not Used)

READ CONNECTOR J3

1	A	→	Read Data Channel P	RDP
2	B	→	Read Data Strobe	RD STRB
3	C	→	Read Data Channel 0	RD0
4	D	→	Read Data Channel 1	RD1
5	E		Not Used	
6	F	→	Auto Disable (Not Used)	
7	H		Not Used	
8	J	→	Read Data Channel 2	RD2
9	K	→	Read Data Channel 3	RD3
10	L		Not Used	
11	M		Not Used	
12	N	→	Gap Detect	
13	P		Not Used	
14	R	→	Read Data Channel 4	RD4
15	S	→	Read Data Channel 5	RD5
16	T		Not Used	
17	U	→	Read Data Channel 6	RD6
18	V	→	Read Data Channel 7	RD7

Figure I-1 Summary of Adapter Characteristics

APPENDIX J
DEC/VENDOR TS03 TRANSPORT PART NUMBERS

Vendor Number	DEC Number	Description
154-0035-001	29-21904	Tape Path Alignment Tool
190-1509-001	29-21905	Tape Guide
190-2399-010	29-21906	Head Assembly
190-2641-001	29-21907	File Protect Assembly
190-2747-001	29-21908	Tape Cleaner Assembly
190-3631-005	29-21909	Read Preamplifier Module
190-3645-002	29-21910	Ramp Generator Module
190-3841-001	29-22269	Control Terminator Module
190-3842-001	29-21911	Interface Control Module
190-3843-001	29-21912	Tape Motion Control
190-3844-001	29-21913	Sense Amplifier/Driver Module
190-3848-001	29-21914	Write Amplifier (4-Channel) Module
190-3849-001	29-21915	Write Amplifier (5-Channel) Module
190-3860-001	29-22268	Data Terminator Module
190-4178-004	29-21916	Quad Read Amplifier Module
190-4179-004	29-21917	Read Amplifier/Clip Control Module
190-4220-001	29-21918	Mag Pot PLB
190-4306-001	29-21919	Servo Preamplifier Module
190-4352-001	29-21920	Voltage Regulator PCB
190-4845-001	29-21921	Timing Delay Module
192-9900-001	29-21922	Test Panel
190-4448-001	29-21923	LED Display
190-4441-001	29-21924	Voltage Regulator/Servo Power Amplifier
190-3468-001	29-21925	Module Extender
190-2647-002	29-21926	Tension Roller
190-2484-001	29-21927	Capstan Motor
128-0091-001	29-21928	Spring
125-0030-006	29-21929	O-Ring
190-4218-001	29-21930	Mag Pot
190-4438-001	29-21931	Reel Motor
151-0057-001	29-21932	Switch
190-1139-001	29-21933	Broken Tape Sensor
190-1138-001	29-21934	Tape Photo Sensor
151-0038-001	29-21935	Switch
125-0006-001	29-21936	Reel Drive Belt (Supply)
125-0015-001	29-21937	Reel Drive Belt (Take-Up)
125-0008-103	29-21938	Bearing
125-0040-001	29-21939	Bearing
154-0001-001	29-21940	Capstan Puller

Vendor Number	DEC Number	Description
190-4474-601	29-21941	Transformer
148-0114-001	29-21942	LED Fairchild FLV-102
148-0108-001	29-21943	Diode MR751
148-0122-001	29-21944	Power Transistor MJ802
151-0802-002	29-21945	Fuse Holder
115-3625-199	29-21946	Capacitor (18K MFD or larger)
115-3610-449	29-21947	Capacitor (40K MFD or larger)
198-0100-001	29-21964	Hub Repair Kit
148-0121-001	29-10334	Power Transistor MJ4502
148-0075-001	29-19037	Transistor 2N4910
148-0053-001	15-10008	Transistor 2N3055A
148-0102-003	15-10712	Transistor MJ-900
148-0102-004	15-10853	Transistor MJ-1000
198-0133-030	90-07217	Fuse 3 A–3 AG (115 V)
198-0133-015	90-08388	Fuse 1.5 A–3 AG (230 V)

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