Digital Equipment Corporation
Maynard, Massachusetts

digital

Maintenance Manual

RF08 DISK CONTROL AND RS08 DISK

DEC-08-HIEA-D

RF08 DISK CONTROL AND RS08 DISK
MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Printing December 1969

CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

TABLES

TABLES (Cont)

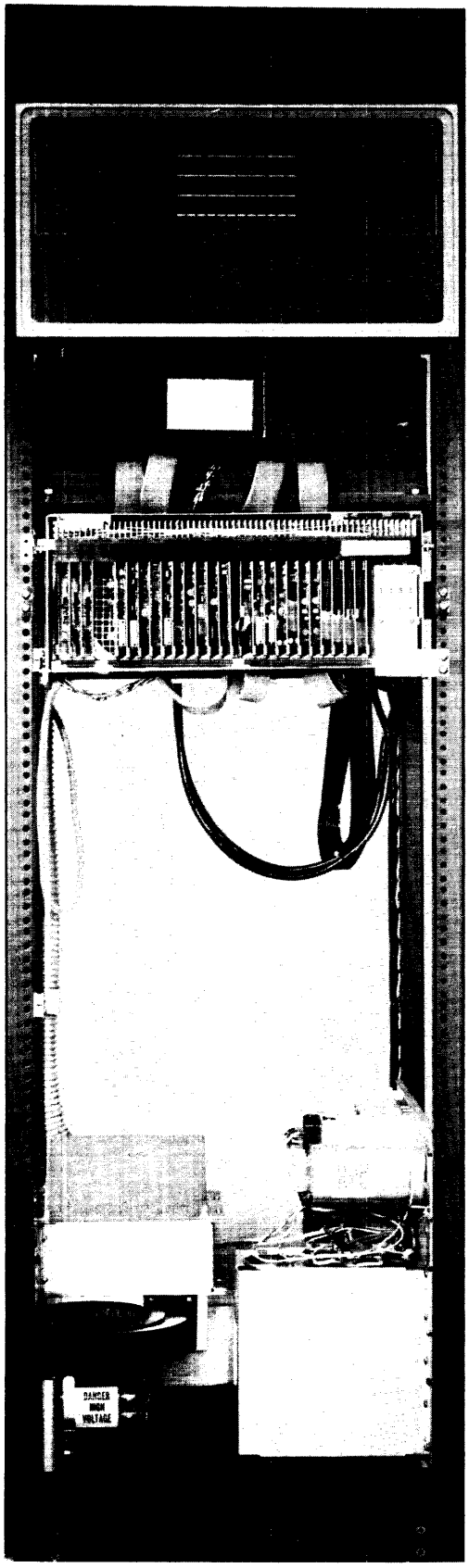


Figure 1-1 Front View of RF08 Disk Control and RS08 Disk (Rack Mounted)

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The RF08 Disk Control and the RS08 Disk (Figure 1-1) combine to provide high-speed bulk storage for DEC PDP-8, PDP-8/I, PDP-8/L, LINC-8 and PDP-12 computers. Each RS08 Disk has a storage capacity of 2048_{10} addresses on each of 128 tracks, giving a total of $262,144_{10}$ addresses. Each address contains a 12-bit word, plus a 13th bit for read parity checking. The RF08 Disk Control (Figure 1-2) controls up to four RS08 Disks (Figure 1-3) giving the disk file a maximum capacity of $1,048,576_{10}$ words.

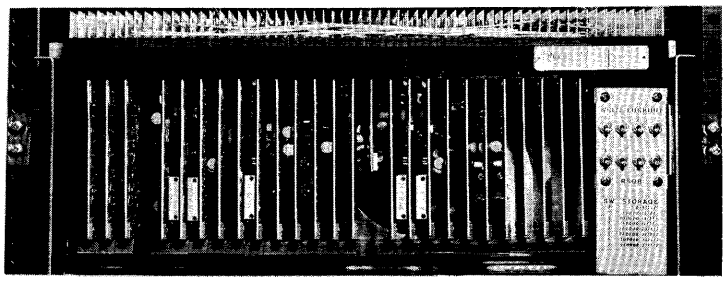


Figure 1-2 RF08 Disk Control (Logic Modules and Write Lockout Switches)

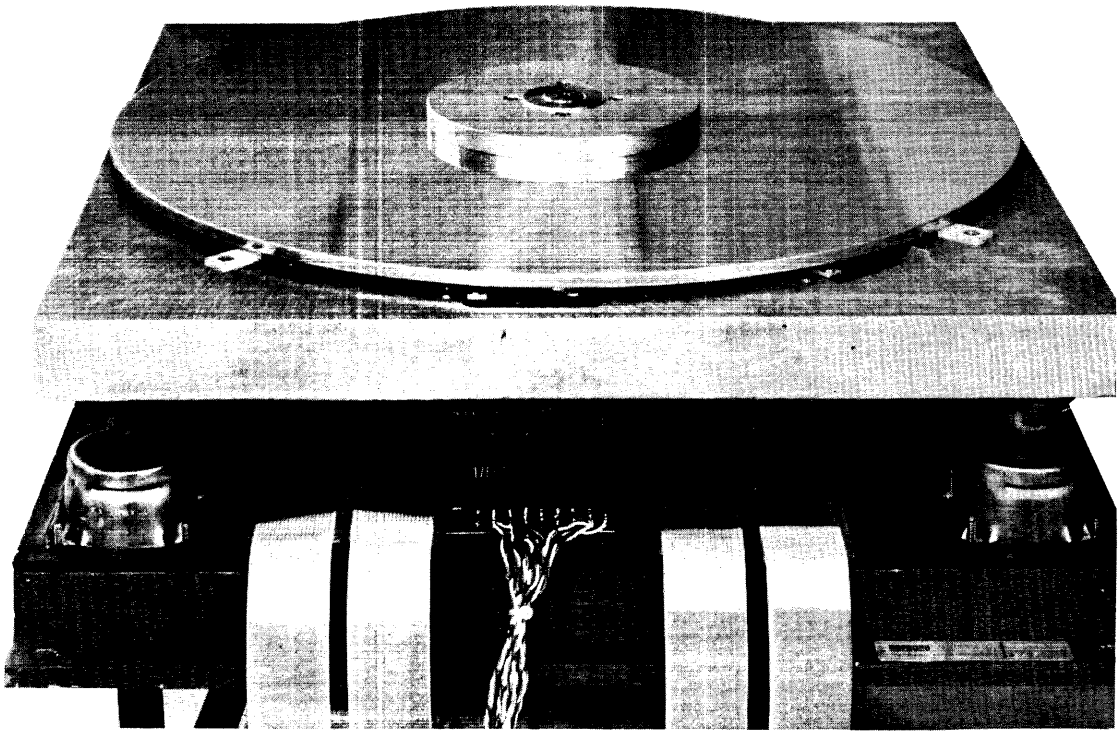


Figure 1-3 RS08 Disk (With Cover Removed)

The disk file is under program control of the associated compatible computer and uses the three-cycle data break facility of the computer. While operation is identical with any central processor; all references in this manual are to the PDP-8 central processor.

The length of a data block is variable, and is specified by loading the length as a negative number into the word count register. The length of a single block is limited only by the maximum number of words (4096_{10}) that can be specified in a 12-bit register.

The starting address for a data transfer can be randomly selected. The data words in the data block are then transferred sequentially to or from the disk. The initial instruction (to read or write) executes the block transfer. This may be from 1 to 4096_{10} words long. The first address in the PDP-8 to be used for data transfer is placed in the current address register. As the block transfer proceeds, the current address register is incremented, and data is transferred sequentially to or from a block of consecutive memory addresses.

Address 7750_8 in the PDP-8 is permanently assigned as the word count (WC) register; address 7751_8 is the current address (CA) register. When the disk is addressed, these memory locations are selected automatically.

CAUTION

The disk file, with one or two disks, is housed in a free-standing rack. A second rack is used to house the third and fourth disks when they are installed. Both disk cabinets are "dedicated" units and no other equipment should be mounted in cabinets housing RS08 Disks.

NOTE

Appendix A presents a list of reference documents to supplement the data presented in this manual.

1.2 SPECIFICATIONS

Specifications for the RF08 and RS08 Disk File system are summarized in Table 1-1.

Table 1-1
RF08 and RS08 Disk File System Summary of Specifications

Disks	Four RS08's may be controlled by one RF08 for $1,048,576_{10}$ words	
Storage Capacity	Each RS08 stores $262,144_{10}$ 13-bit words (12 data bits plus 1 even parity bit)	
Data Transfer Path	3-Cycle Break	Address Locations
	Negative bus	7750_{10} Word Count
	0 and -3V levels	7751_{10} Current Address
Data Transfer Rate	60-Hz Power	50-Hz Power
	16.0 μs per word	19.2 μs per word
Minimum Access Time	258 μs	320 μs
Average Access Time	16.9 ms	20.3 ms
Maximum Access Time	33.6 ms	40.3 ms
Program Interrupt	33 ms clock flag Data transmission complete flag Error flag	
Write Lock Switches	Eight switches per RS08 are capable of locking out any combination of eight $16,384_{10}$ word blocks in addresses 0 to $131,071_{10}$.	
Data Tracks	128	
Words Per Track	2048	
Recording Method	NRZI	
Density	1100 bpi (maximum)	
Timing Tracks	Three plus three spare (spares can be used to recover data on disk)	

Table 1-1 (Cont)
RF08 and RS08 Disk File System Summary of Specifications

Operating Environment	Recommended temperature 65° to 90°F. Relative humidity 10% to 55%. No condensation (storage or operating) can be allowed
Vibration/Shock	Adequate isolation is provided to prevent data errors CAUTION Extreme vibrations should be avoided while the RS08 is transferring information.
Heat Dissipation	RF08: 150W RS08: 300W
AC Power Requirements	115/230 ± 10% Vac, single phase, 50 ± 2 or 60 ± 2 Hz, 5A (maximum) for logic power NOTE Logic power for one RF08 and up to four RS08's is provided by one DEC type 705B power supply.
RS08 Motor Power Requirements	Motor Start: 5.5A for 20 ± 3s. Motor operation: 4.0A continuous @ 115 Vac. NOTE A stepdown autotransformer is provided for 230 Vac operation.
Line Frequency Stability	Maximum line frequency drift 0.1 Hz/s. A constant frequency motor-generator set or static AC/AC inverter should be provided for installation with unstable power sources
Motor Bearing Life	Expected operating life of at least 20,000 hours, under standard computer operating environment
Reliability	Six recoverable errors and one non-recoverable error in 2×10^9 bits transferred. A recoverable error is defined as an error that occurs only once in four successive reads. All other errors are non-recoverable

Table 1-1 (Cont)
RF08 and RS08 Disk File System Summary of Specifications

	CAUTION On-off cycling of the RS08 is not recommended. For this reason, the RS08 motor control operates independently of the computer power control.
Cabinet	A "dedicated" cabinet is designed to accommodate one RF08, up to two RS08's and power supply. Two additional RS08's can be mounted in a second cabinet. Other equipment should not be mounted in disk cabinets
Shipping Information	Weight of RF08, two (2) RS08, power supply and cabinet: 590 lb (crated) 500 lb (uncrated) Weight of RF08, two (2) RS08, power supply and cabinet: 690 lb (crated) 600 lb (uncrated) (The RF08/RS08(s) are shipped mounted in cabinets)

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The RF08 and RS08 mount in a standard DEC cabinet Type H950 using "Chassis-Track" slides (part number C-300-S-20). Installations with one or two RS08 Disks require a single cabinet. If three or four disks are to be installed, a second cabinet is required. A single model power supply, Model 705B supplies power to all logic circuits. Each disk is a sealed unit that contains the drive motor, disk, heads, and electrical networks for the heads. A separate chassis for each disk contains the RS08 Logic and Motor Control.

CAUTION

The RS08M Disk Assembly MUST NOT be opened in the field by personnel other than authorized DEC Field Engineers. Special procedures, alignment and adjustment fixtures, and cleaning equipment is required to service the disk. Any attempt to remove the recording surface by inexperienced or untrained personnel will invariably destroy the surface of the disk. Any unauthorized openings of the RS08M Disk Assembly will void all warranties applying to the unit.

2.2 REQUIREMENTS

For disk file power requirements refer to Figures 2-1, 2-2, and 2-3. The disk system is supplied with a 25 ft 30A 3-wire pigtail-line-cord for North American installations. Table 2-1 specifies the Hubble connectors which are to be attached to the line cord.

2.2.1 Disk Motor Power

The disk motor operates from 105-130 Vac, 50 Hz (50 Hz, 230 Vac on special order) ±2 Hz. Because of synchronous drive motor characteristics the maximum rate of ac power source frequency drift should not exceed 0.1 Hz/s. Line transients exceeding the operating voltage limits will require site provisions for regulating power supply voltage. Disk motor power must be supplied from an unswitched bus.

Table 2-1
Primary Power Connectors
(North American Installations Only)

Line Voltage (Single Phase)	Hubbell Connector Part Number
115V 60 Hz 30A	3331-6 or 3331
230V 60 Hz 20A	none supplied
115V 50 Hz 30A	none supplied
230V 50 Hz 20A	3321-6 or 3321

2.2.2 Logic Power

The logic power supply should be connected to the central processor switched power bus. The power supply has sufficient capacity to power one RF08 Disk Control and four RS08 Disks. This supply must not be used to supply power to other units. Noise generated on the power supply busses could affect data transfer reliability.

2.2.3 Ground Circuits

The cabinet(s) containing the disk file must be grounded by mechanical connection to the central processor. All grounds should be connected to a common ground point to prevent circulating currents in the ground circuits.

2.2.4 Connection of RF08 to Central Processor

Interconnection of cabling between the RF08 and the computer is shown in Figure 2-4. The proper termination techniques required at the time of installation are also shown.

NOTE

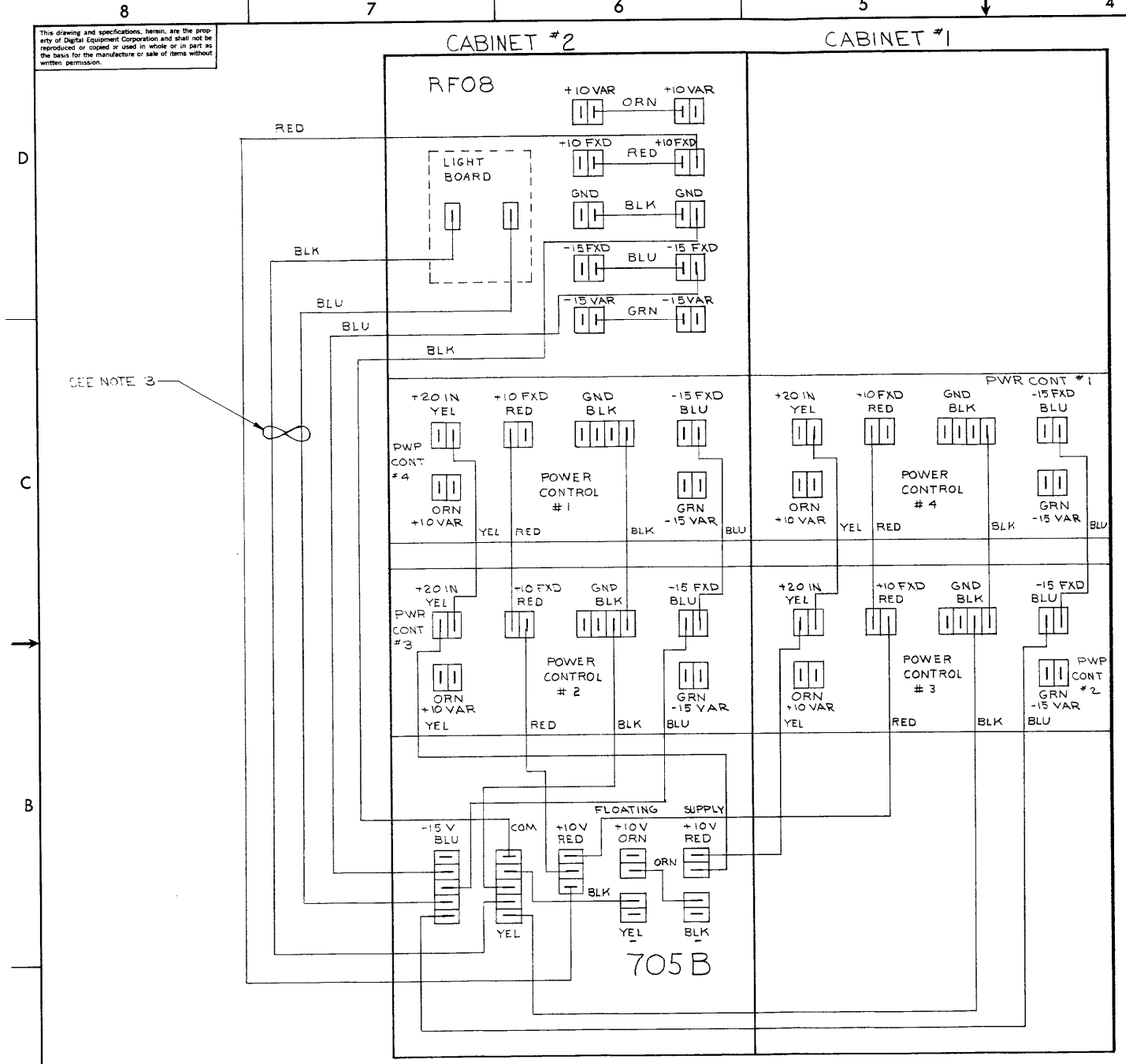
Cables should be routed away from ac power lines and from other data cables that might introduce noise.

2.2.5 Connection of RF08 to RS08

The interconnection for installations with one to four RS08 Disks is shown in Figure 2-5. Cables should be routed to allow the RS08 Disk Logic Chassis to be pulled all the way out without damaging the cables.

2.2.6 Connecting the Purging Blowers

The purging blowers are located at the bottom of the cabinet. Connect the air duct from each purging unit outlet to its corresponding disk.



DC WIRING

NOTES:

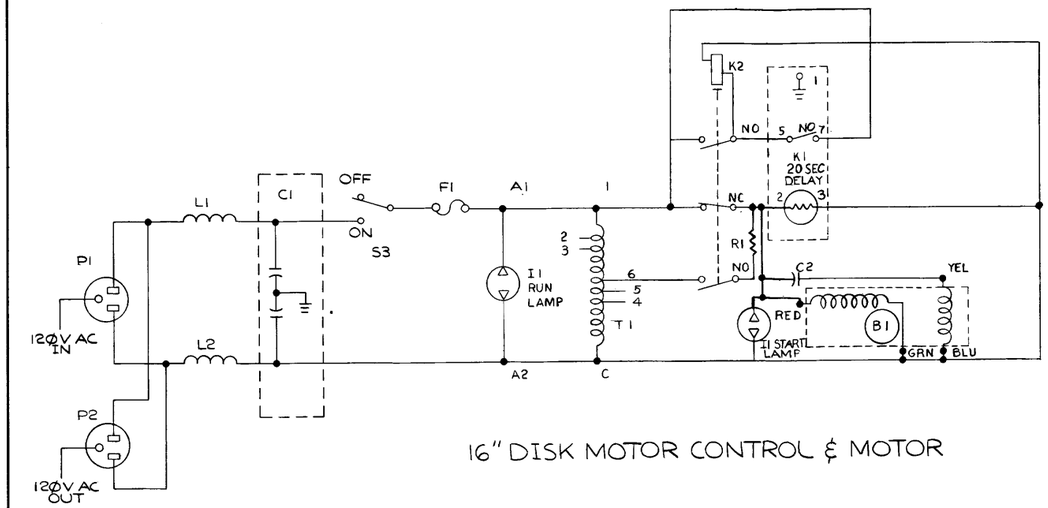
1. ALL DC WIRES TO BE #14 AWG STRD TEF.
2. DC WIRES ARE TO BE KEPT SEPARATE FROM AC WIRES. DC WIRES TO BE DRESSED TO REAR RIGHT HAND CORNER OF CABINET.
3. TWIST BLU/BLK LIGHT BOARD WIRES APPROXIMATELY ONE TWIST PER INCH.
4. DRESS POWER CONTROL WIRES WITH SUFFICIENT SLACK TO PERMIT CHASSIS TRAVEL, COVER WITH SPIRAL WRAP.

REVISIONS | REV. | CHANGE NO. | CHK

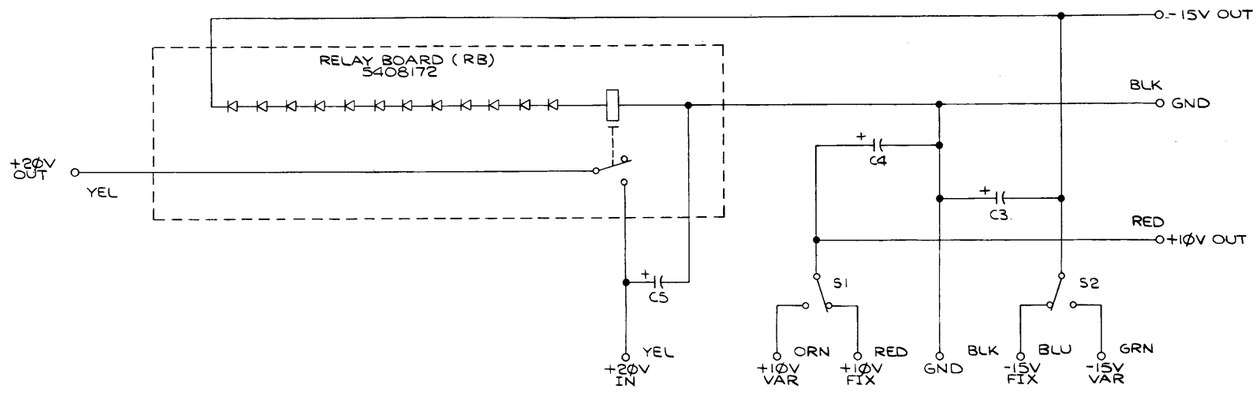
SIZE D | CODE IC | NUMBER RS08-0-2 | REV A

DEC FORM NO DRD 100

Figure 2-1 DC Power Wiring Diagram



16" DISK MOTOR CONTROL & MOTOR

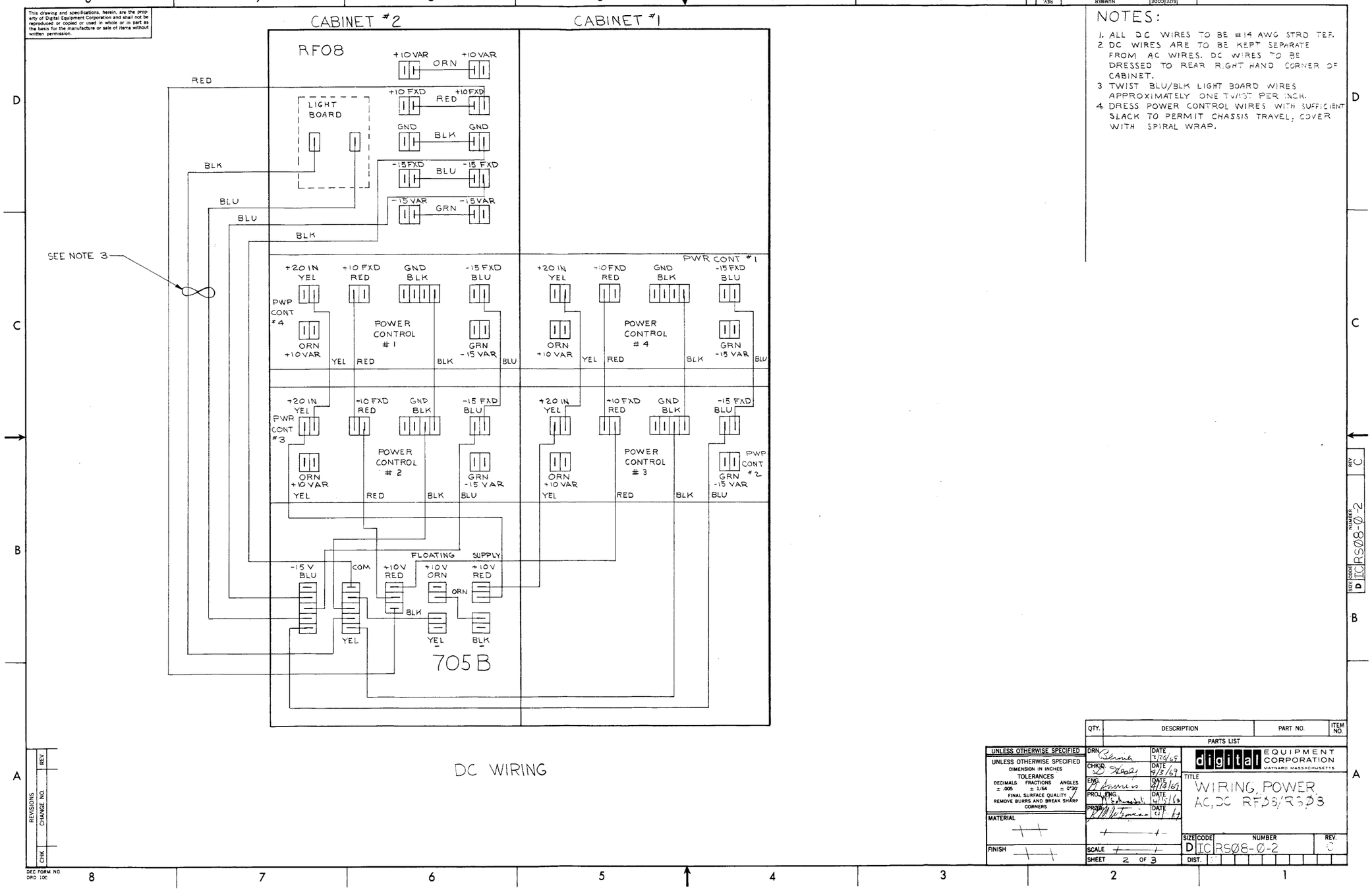


RSØ8 D.C. POWER CONTROL

REF DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	
R1	RES 1.5 Ω 10W	1300148
C1	CAP 2<.1MFD 600VDC	1002153
C2	CAP 30MFD 370V	1009122
C3,C4,C5	CAP 50MFD 50V	1000080
K1	TIMING RELAY	1209121
K2	EBERT RELAY	1209491
B1	MOTOR 50 HZ	1209003-21
B1	MOTOR 60 HZ	1209003-20
I1,I2	LIGHT PILOT 110V	1205458
T1	2:1 AUTO XMFR	1609313
S1,S2,S3	SWITCH SPDT	1202279
L1,L2	TUBE FERROXCUBE	1605147
F1	7 AMP S.B. FUSE	9007224
RB	RELAY BCARD	5408172
P1	SOC 3 PIN AC MALE	1201252
P2	SOC 3 PIN FEMALE	1201251

SIZE D | CODE 05 | NUMBER 7006156-0-1 | REV C

Figure 2-2
Power and Motor Control Circuit Schematic Diagram



DC WIRING

NOTES:

1. ALL DC WIRES TO BE #14 AWG STRD TEF.
2. DC WIRES ARE TO BE KEPT SEPARATE FROM AC WIRES. DC WIRES TO BE DRESSED TO REAR RIGHT HAND CORNER OF CABINET.
3. TWIST BLU/BLK LIGHT BOARD WIRES APPROXIMATELY ONE TWIST PER INCH.
4. DRESS POWER CONTROL WIRES WITH SUFFICIENT SLACK TO PERMIT CHASSIS TRAVEL; COVER WITH SPIRAL WRAP.

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

		DATE
DRN		3/20/69
CHK'D		4/3/69
ENG		4/3/69
PROJ. ENG.		4/15/69
PROG		4/17/69

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: WIRING, POWER AC, DC RF35/R3?B

SIZE D | CODE IC | NUMBER RSØ8-Ø-2 | REV. C

SCALE

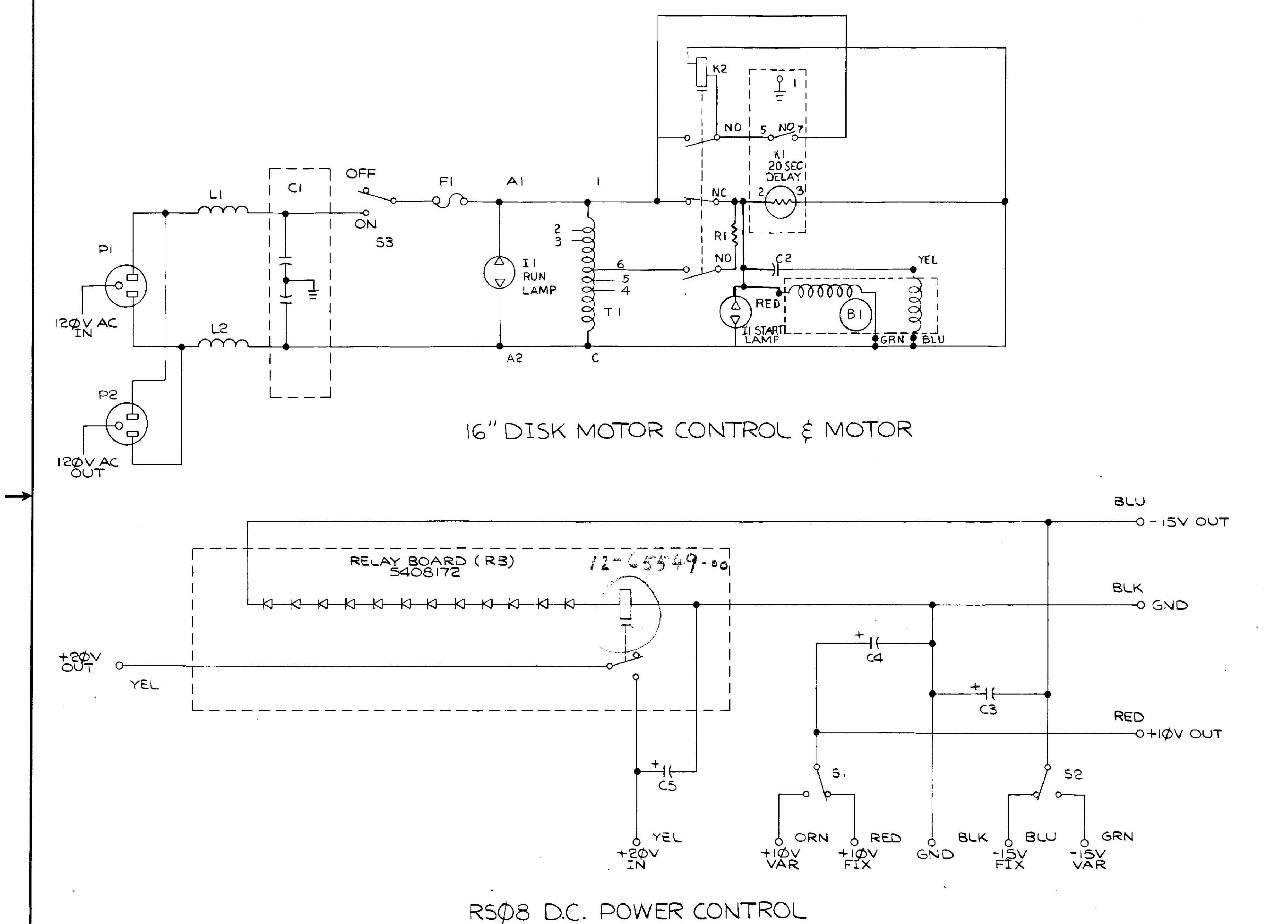
SHEET 2 OF 3

DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 10C

Figure 2-1 dc Power Wiring Diagram



R1	RES 1.5 Ω 10 W	1300148
C1	CAP 2×.1MFD 600VDC	1002153
C2	CAP 30 MFD 370V	1009122
C3, C4, C5	CAP 50 MFD 50V	1000080
K1	TIMING RELAY	1209121
K2	EBERT RELAY	1209491
B1	MOTOR 50 HZ	1209003-21
B1	MOTOR 60 HZ	1209003-20
I1, I2	LIGHT PILOT 110V	1205458
T1	2:1 AUTO XMFR	1609313
S1, S2, S3	SWITCH SPDT	1202279
L1, L2	TUBE FERROXCUBE	1605147
F1	7 AMP S.B. FUSE	9007224
RB	RELAY BOARD	5408172
P1	SOC 3 PIN AC MALE	1201252
P2	SOC 3 PIN FEMALE	1201251
REF DESIGNATION	DESCRIPTION	PART NO.

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE POWER CONTROL AND MOTOR CONTROL

SIZE D CODE CS NUMBER 7006156-0-1 REV. C

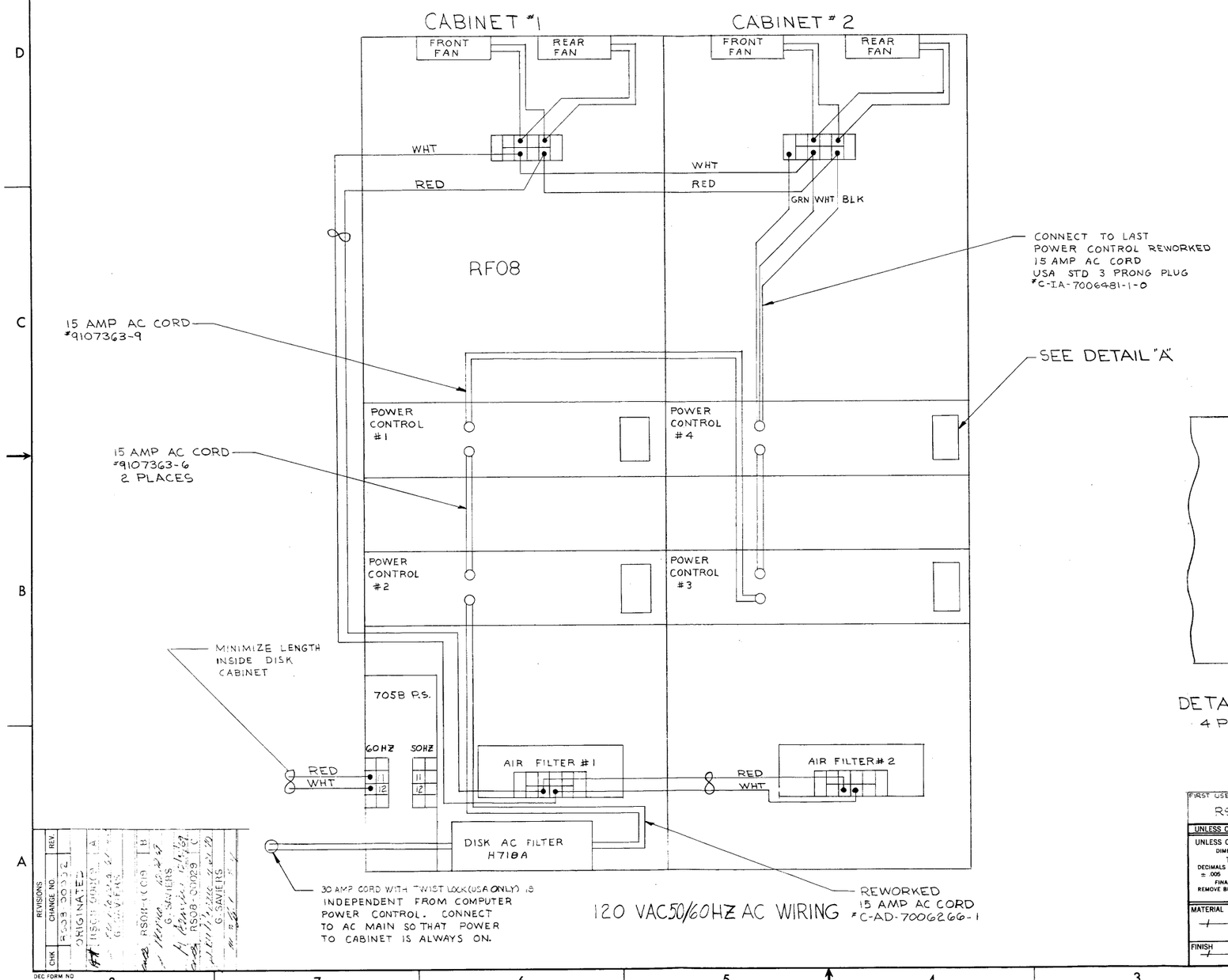
PRINTED CIRCUIT REV.

DEC FORM NO. DRD 101

Figure 2-2 Power and Motor Control Circuit Schematic Diagram

NOTES:

1. JUMPERS BETWEEN PWR CONTS. ARE WIRED WITH 15 AMP 120VAC CORD FOR MAIN POWER.
2. ALL WIRES TO BE #14 AWG STRD TEF UNLESS OTHERWISE SPECIFIED.
3. ALL AC WIRES TO BE #14 AWG STRD TEF RED & WHT TWISTED PAIRS UNLESS OTHERWISE SPECIFIED.
4. POWER CONTROL CONNECTOR – USA STD 3 PRONG PLUG. DEC SPEC #9107363-(SEE DWG)
5. FRAME GROUNDS ARE PROVIDED ON OUTPUT SIDE OF H718A ONLY. DO NOT CONNECT FRAME GROUND ON 705B POWER SUPPLY.



REVISIONS:	REV.	CHANGE NO.
CHK	A	RS08-30552 ORIGINATED
	B	RS08-10019
	C	RS08-30029

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RS08-0		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

		DATE
DRN	Bennis	3/18/69
CHK'D.	[illegible]	3/18/69
ENG.	[illegible]	4/13/69
PROJ. ENG.	[illegible]	4/12/69
PROD.	[illegible]	4/14/69

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: WIRING, POWER, AC, DC RF08/RS08

NEXT HIGHER ASSY: A-ML-RS08-0

SIZE D | CODE IC | NUMBER RS08-C-2 | REV. C

SCALE

SHEET 1 OF 3

DEC FORM NO DRD 100

Figure 2-3 120 Vac 60 Hz Schematic Diagram

2.3 ENERGIZING THE DISK

a. Remove the disk drive motor shaft locks from each RS08M Disk in the system and check for loose wires.

b. Turn the H718A Power Line Filter on and observe that the pilot lamp is illuminated indicating that power is available at the output of the H718A. The switch is located in the bottom rear part of the RF08 Cabinet.

c. Turn DISK POWER switch ON. This switch is located on the rear of the disk logic chassis. The START and OPERATE lamps will light.

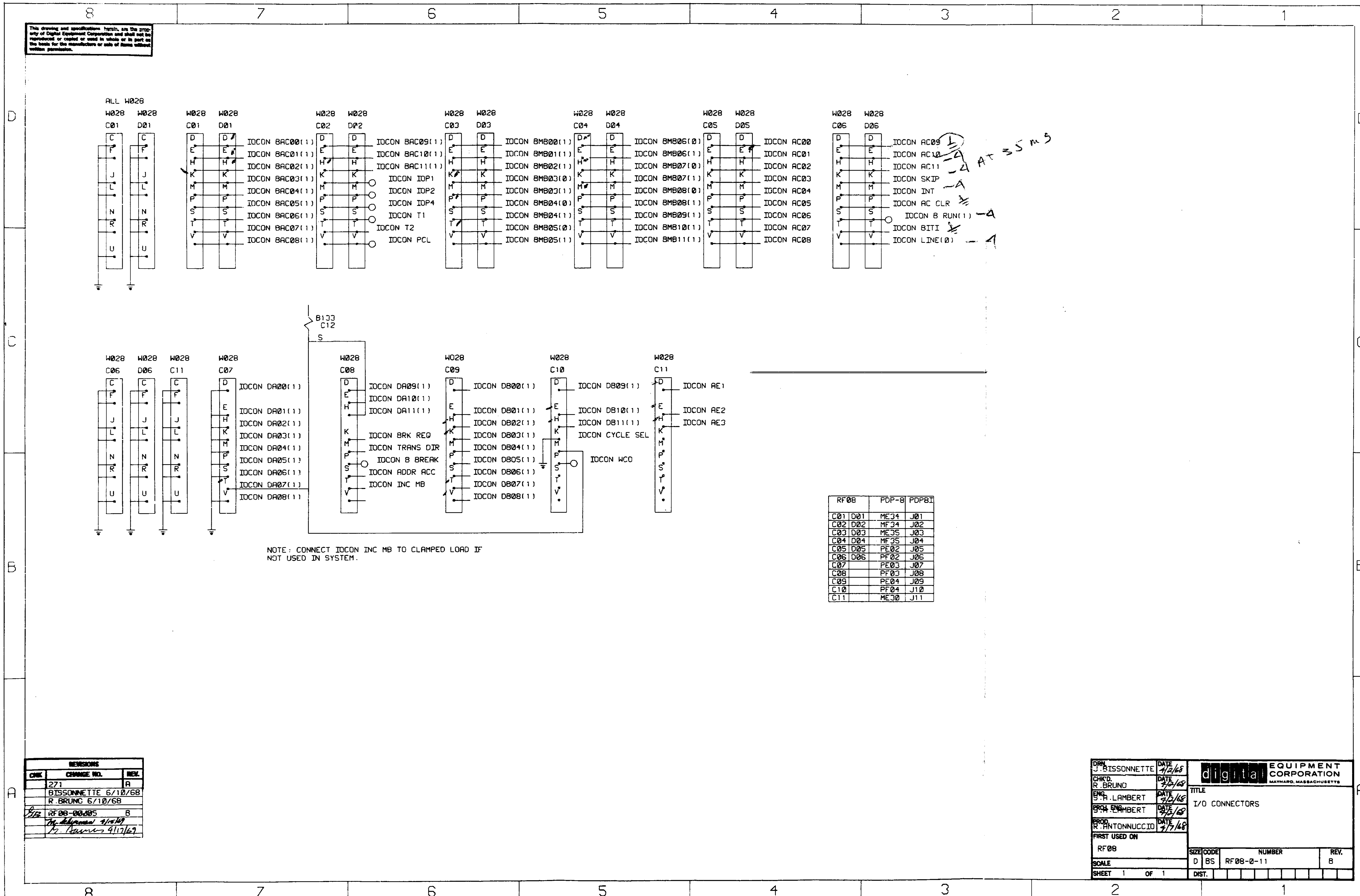
NOTE

The disk is inoperable while the START lamp is lit. Power transients caused when the DISK POWER switch is operated may cause data errors if another disk in the system is in operation and transferring data.

d. Check that the disk is running and that its blower motor is operating.

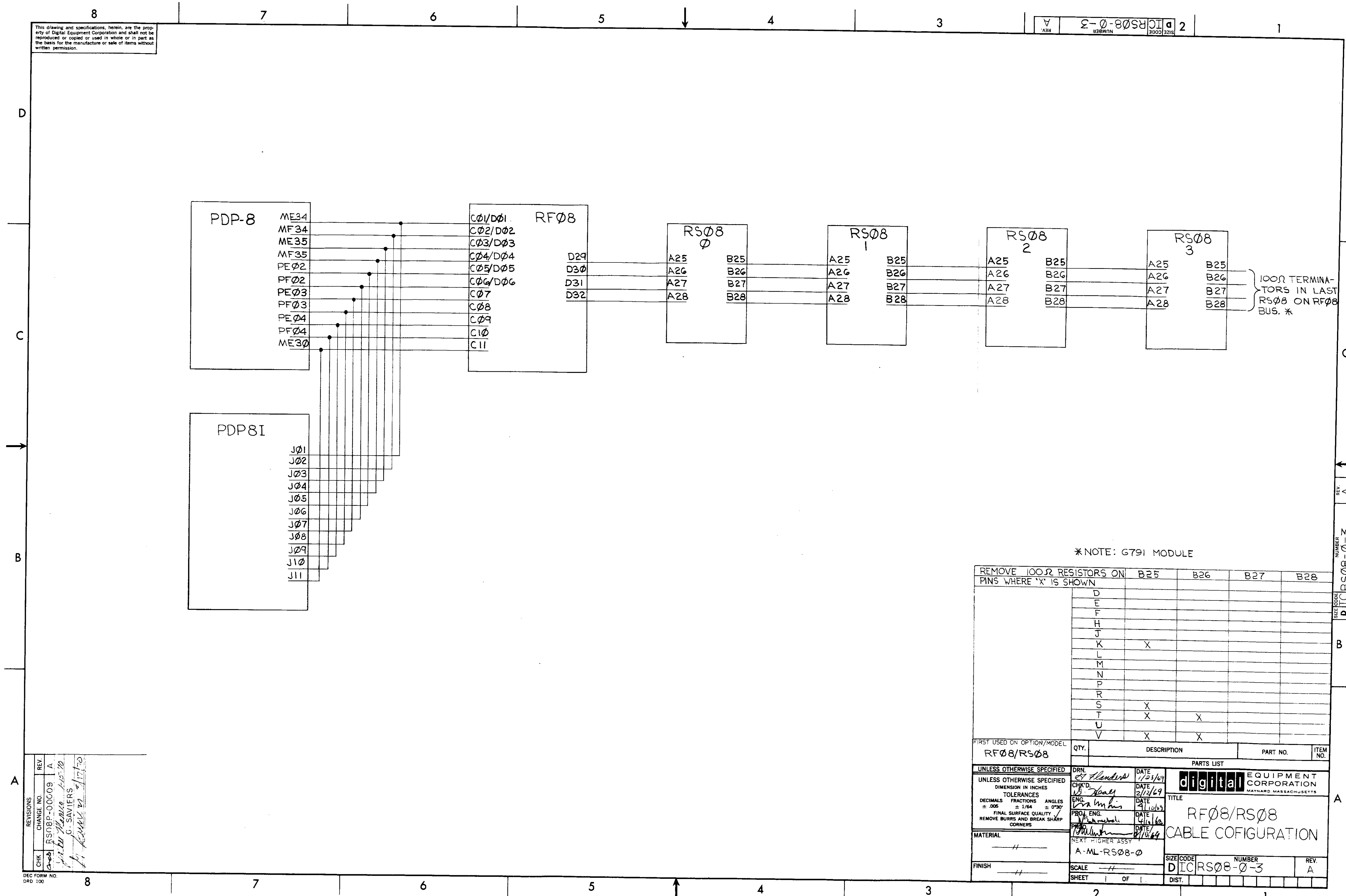
e. After 20s, the START lamp will go out, indicating that the acceleration run is complete, and that the disk motor has switched to run power.

f. Repeat steps a through e above for the other disks.



RF08		PDP-8	PDP8I
C01	D01	ME34	J01
C02	D02	MF34	J02
C03	D03	ME35	J03
C04	D04	MF35	J04
C05	D05	PE02	J05
C06	D06	PF02	J06
C07		PE03	J07
C08		PF03	J08
C09		PE04	J09
C10		PF04	J10
C11		ME30	J11

Figure 2-5 RF08 to PDP-8/PDP-8/I Interconnection Cable Diagram



REMOVE 100Ω RESISTORS ON PINS WHERE 'X' IS SHOWN	B25	B26	B27	B28
D				
E				
F				
H				
J				
K	X			
L				
M				
N				
P				
R				
S	X			
T	X	X		
U				
V	X	X		

Figure 2-6 RF08 to RS08 Interconnection Cable Diagram

CHAPTER 3

PRINCIPLES OF OPERATION

3.1 INTRODUCTION

The description in this chapter generally refers to operation with one RS08 Disk. The RF08 Disk Control is provided with control logic for addressing up to four RS08's. The disks are connected in parallel to the data address lines. Each supplemental disk has a modified decoding card which decodes the addresses supplied by bits 7 and 8 of the Extended Memory Address (EMA). All other functions are identical when extra disks are installed.

3.2 FUNCTIONAL DESCRIPTION

The RS08 contains the disk and read/write data heads, the data write driver, and an address reader. Except for head selection, all data transfers between the RS08 and RF08 are serial binary. Head selection is parallel binary. RS08 Block Diagram (Figure 3-1) is a description of the RS08. Figure 3-2 is a circular timing diagram of the address tracks. Table 3-1 lists the Signal Mnemonics.

NOTE

Appendix B contains a typical RS08/RF08 I/O routine.

3.2.1 Address Tracks

There are three address tracks, which are written permanently on the disk and detected by three independent read amplifiers. A set of complete spare tracks is provided. The spare tracks are written on the disk in exact phase-lock with the primary set of tracks. Thus data written on the disk can be recovered even if the primary set of tracks is lost by accidental erasure or component failure. When switching to spare tracks the timing track amplifiers must first be adjusted before attempting to recover data.

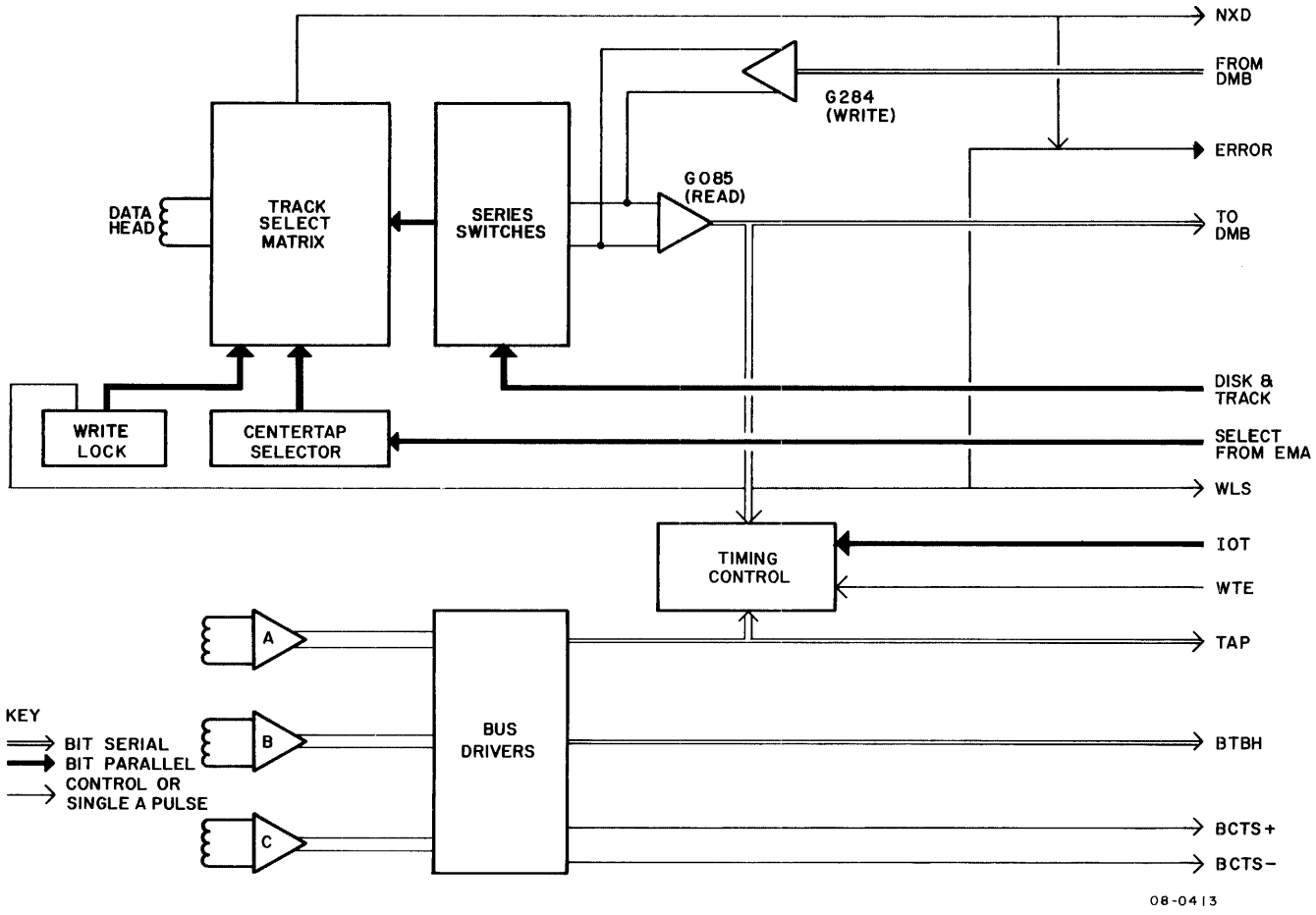
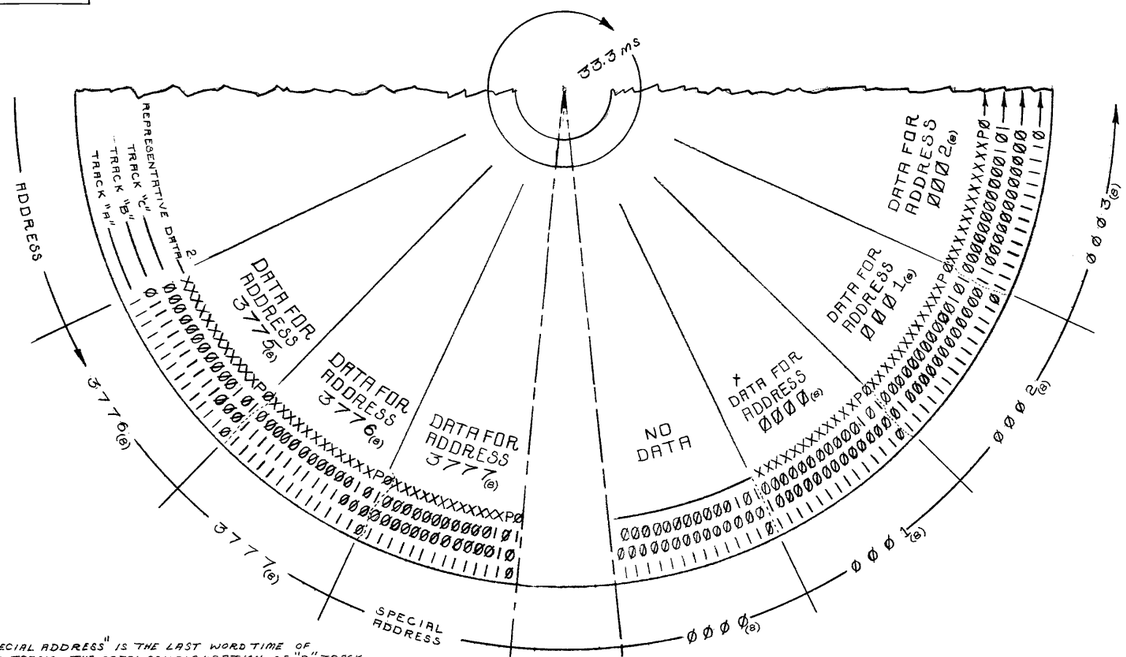


Figure 3-1 RS08 Block Diagram

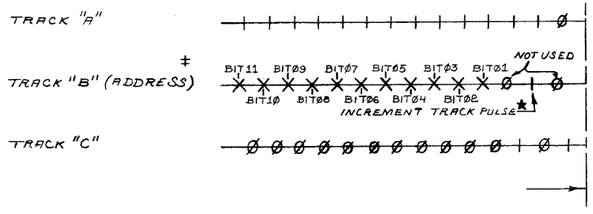
CAUTION

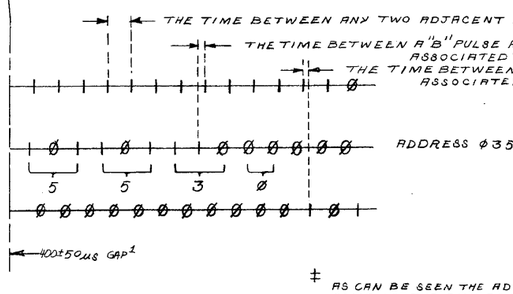
In NO case should an ohmmeter be used to test the timing tracks. Connection of such a meter to the disk heads will erase the prerecorded timing tracks. Extreme care should be used when making oscilloscope measurements near the timing track connector since even a momentary short to ground of these pins will erase the timing tracks.

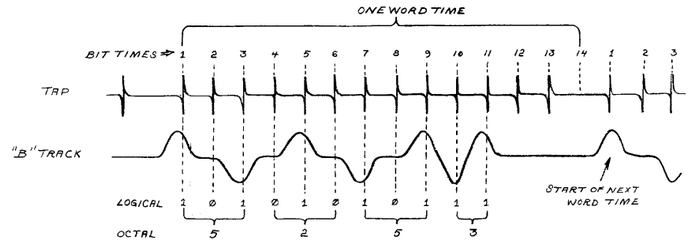
The RS08 has no circuitry for writing new address tracks. This is done with a separate track writer. The address tracks (Figure 3-2) are identified in 3.2.1.1, 3.2.1.2, and 3.2.1.3.



THE "SPECIAL ADDRESS" IS THE LAST WORD TIME OF EVERY TRACK. THE OCTAL CONFIGURATION OF "B" TRACK CAN BE READ AS 10,000. THE PURPOSE OF SPECIAL ADDRESS IS TO STORE THE DATA FOR THE PREVIOUS ADDRESS (3777) AND TO PRODUCE THE INCREMENT TRACK PULSE.







REVERSED = 3525

DECODING THE ADDRESS TRACK

ANALOG AMPLIFIED "B" TRACK IS DISPLAYED ON ONE CHANNEL OF THE OSCILLOSCOPE. TRACK "A" PULSE (TRP) IS DISPLAYED ALTERNATELY ON THE OTHER CHANNEL TO GIVE A TIME RELATIONSHIP. SYNC IS EXTERNAL ON SYNC MARK. THE ADDRESS BEING DISPLAYED IS 3525.

ALL REFERENCES MADE TO 60 HZ

SYMBOL CODE:

- 1 ALWAYS A LOGICAL "ONE"
- Ø ALWAYS A LOGICAL "ZERO" (UNLESS OTHERWISE INDICATED)
- X POSSIBLE "ONE" OR "ZERO"
- P POSSIBLE PARITY BIT. (RS-08 USES EVEN PARITY)

‡ AS CAN BE SEEN THE ADDRESS TRACK WILL COME OFF THE DISK BACKWARDS. TO DECODE AN ADDRESS, DISREGARD THE LAST THREE BIT TIMES AND READ THE REMAINING ELEVEN FROM RIGHT TO LEFT.

✱ TIME IS MEASURED FROM LEADING EDGE TO LEADING EDGE OF THE SLICED ANALOG SIGNALS.

† DATA FOR A PARTICULAR ADDRESS IS WRITTEN INTO THE NEXT SEQUENTIAL ADDRESS.

★ THE INCREMENT TRACK PULSE (OCTAL CONFIGURATION 10,000) OCCURS ONLY DURING SPECIAL ADDRESS.

1. ON THE RS-08, SYNC MARK AND THE GUARD BANDS ARE DERIVED THRU THE TIMING AND DELAY LINES NOT THRU A PHOTOCELL.
2. FOR A REPRESENTATION OF TRACK POSITIONING REFER TO THE TRACK INTERLACEMENT DIAGRAM.

REVISIONS	REV.	CHANGE NO.	CHK.

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

		DATE
DRN.	P. DIGREGORIO	10-29-68
CHK'D	Gary Levine	9-9-69
ENG.	Gary Levine	9-9-69
PROJ. MGR.	P. D'Amico	9-9-69
PROD.	R. D. Tavares	9/9/69

FIRST USED ON: RS Ø8

SCALE

SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: RS Ø8 CIRCULAR TIMING DIAGRAM

SIZE	CODE	NUMBER	REV.
D	TD	RSØ8-Ø-5	

DIST.

DEC FORM NO. 102A

Figure 3-2 Circular Timing Diagram

Table 3-1
RF08 Signal Mnemonics

Mnemonic	Description
ABC	Address Bit Comparator flip-flop. Address track bits and DMA contents are compared serially. If they do not compare, ABC is set, to indicate no comparison. ABC is also set by TEP. Cleared at the end of each address word by WEP.
ADC	ADdress Confirmed flip-flop. Set at the end of an address word when the track address and DMA address compare (ABC clear). ADC is cleared by DRE (0), indicating that no data transfer is to occur, and may be set only when DRE is 1. The set pulse is strobed in by TCP, at the end of an address word, and delayed 60 ns. ADC is also cleared at the end of a track by HSE (1) and DEP (1), and by SCLP 1.
ACH	Address Compare Hold flip-flop. Determines polarity of IDMAE when searching for an address and incrementing the DMA. ACH is set initially by SCLP, causing IDMAE to be true with respect to the contents of DMA 11. ACH is cleared by DEP at the end of any word in which data was transferred. This causes IDMAE to be the complement of the contents of DMA 11. ACH is set during the next address word by SDMAP and DMA 11 (0). This allows all of the low-order 1's and the first 0 in the DMA to be complemented as the address rotates through the DMA. ACH is also set by ADC going to set when the first address (0000_8) is compared after head switch, when writing a block of data.
BDDMB 11 (1)	Buffered-Delayed Disk Memory Buffer 11 (1). This signal reflects the state of DMB 11, delayed 250 ns after SDMBP. It is used as the writing command sent to the disk.
BTAS	Buffered Track A Sliced. The clock-strobe signal generated from timing track A. This signal is differentiated to form the TAP pulses, which represent the time location of each of the 13 bits of data.
BTCS-	Buffered Track C Sliced. A pulse generated at bit-time 12 from timing track C. This pulse sets WDE, denoting the end of data in each data word.
BTCS+	Buffered Track C Sliced. Generated from timing track C at bit-time 14. This pulse generates TCP and WEP, and clears WEP. Denotes the end of an address word.
CDMBP	Clear Disk Memory Buffer Pulse. Generated by IOT 604 (DMAW) and by BTCS- when writing. Clears the 12 DMB flip-flops to allow data transfer from the MBH register. Not generated during the read cycle.
CEMAP	Clear Extended Memory Address Pulse. Generated by PCL or by IOT 641 (DXAL). Generation inhibited by IOT 645 (DXAC). Clears the EMA to allow a new address to be written in from the central processor AC.
CIE	Completion Interrupt Enable flip-flop. Enables interrupt of the central processor by the DCF, when set. Set by IOT 614 (DIML) when central processor AC 5 is 1. Cleared by Power Clear (PCL) or IOT 611 (DCIM).

Table 3-1 (Cont)
RF08 Signal Mnemonics

Mnemonic	Description
CMBH	Clear Memory Buffer Hold flip-flop. Generates CMBHP in write mode. Set by B Break (pulse) and R/W (1) (level), and cleared by WLMBHP- or SCLP 1.
CMBHP	Clear Memory Buffer Hold Pulse. Clears MBH before data transfer. Generated during write by CMBH (1). Generated during read by ADC (1) and R/W (0), strobed by BTCS-.
DATA	DATA flip-flop (maintenance). Complemented by TGP if central processor AC 7 is 1. Cleared by SCLP 2.
DBR	Data Break Request flip-flop. Requests three-cycle data break from central processor when disk is ready to transfer data to or from central processor. In write mode, initially set by IOT 604 (DMAW), then set by HSE (1) and WCS (0) (level); and LDMBP (pulse). In read mode, set by RLMBHP (1) and WCS (0) (pulse). Cleared by ADDR ACC or SCLP 1.
DCF	Data Completion Flag flip-flop. Set at the end of a data transfer. Set enabled by WCO (0) (level) and DEP (pulse). Also set by ROFP and NXD. Cleared by SCLP 1.
DEP	Data End Pulse flip-flop. Generates 100 ns pulse at the end of each data word transfer. Enabled by ADC (1) (level), strobed by TCP (pulse). Cleared by delay loop.
DMA	Disk Memory Address register. 11-bit flip-flop register which contains disk memory angular address. Loaded from central processor AC by IOT 602 (DMAR) or IOT 604 (DMAW). Bit 1 corresponds with address bit being read from track. Address shifted through DMA 1 position toward DMA 11 by SDMAP. State of DMA 11 is written into DMA 1 at SDMAP, either true or complemented, controlled by AC, using states of IDMAE ±. Contents read into central processor AC by IOT 624 (DMAC). Cleared by SCLP 2. Note that EMA bit 0 is loaded and read back to and from the central processor with these instructions, but is not shifted.
DMB	Disk Memory Buffer. 12-bit flip-flop register which contains (during write) the data word to be written on the disk, or is loaded (during read) with the data word on the disk. Loaded with the contents of the MBH by LDMBP, during write. Contents of bit 11 generate BDDMB which is used to control writing. During read, contents of each disk bit generate BMBI, which represents the data bit on the disk. The contents of BMBI are strobed into DMB 0 by TAP. Contents of the DMB are shifted one position toward DMB 11 by SDMBP. Cleared by IOT 604 (DMAW), R/W (1), and BTCS-.
DRE	Data Request Enable flip-flop. Must be set to allow address search, inhibits data transfer when clear. Set by TCD going to 0, or by LDMAP if PCA true. Cleared by DCF (1) or SCLP. Also cleared by EMA 6 going to 0 (level).
DRL	Data Request Late flip-flop. Error indication when set. Set by DEP if DBR is set. Cleared by SCLP 1.

Table 3-1 (Cont)
RF08 Signal Mnemonics

Mnemonic	Description
EA 1,2,3	Extended Address flip-flops. Set to indicate selection of central processor extended memory fields. Set by IOT 614 (DIML) and contents of central processor AC 8 through 10. Cleared by PCL or IOT 611 (DCIM).
EIE	Error Interrupt Enable flip-flop. Set by IOT 614 (DIML) if central processor AC 3 is set. Cleared by PCL or IOT 611 (DMIM). Errors selected for interrupt by setting EIE are: DRL, PER, WLS, and NXD.
EMA	Extended Memory Address register. 9 bit flip-flop register whose contents select the disk (of 4 possible) and track (of 128 possible) for data transfer. EMA 1 through 8 loaded with contents of central processor AC 11-4 by IOT 642 (DXAL). EMA 0 loaded with DMA instructions. Cleared by CEMAP. EMA 0 also cleared by SCLP 2. Incremented by HSE (1). EMA bits 0 through 6 select track. Bits 7 and 8 (corresponding to central processor AC bits 4 and 5) select disk.
ERROR	Indicates error in operation. True for any of the following: DRL, PER, WLS, NXD.
HSE	Head Switch Enable flip-flop. Set by TEP if ADC and WCO are set, to indicate end-of-track during data transfer. Cleared when ADC goes to 0, or by SCLP 2.
IDMAE and IDMAE-	Increment Disk Memory Address Enable levels. Used for address search and to increment the contents of the DMA. Polarity controlled by contents of DMA 11 and ACH. When ACH is set, IDMAE is true with respect to contents of DMA 11. When ACH is clear, IDMAE is complement of DMA 11. Contents of IDMAE are compared with BTBH during address search. Contents of IDMAE are placed in DMA 1 at SDMAP. IDMAE- is IDMAE inverted, used by exclusive OR gate when searching for address to indicate DMA 11 (0), and to write a 0 into DMA 1.
IOT	Input-Output Timing pulse. Generated by IOP 1, 2, or 4, when present, and BMB 3-8 decoded to equal octal 60_8, 61_8, 62_8, or 64_8.
LDMAP	Load Disk Memory Address Pulse. Generated by IOT 602 (DMAR) or IOT 604 (DMAW) to load contents of central processor AC into DMA and EMA 0.
LDMBP	Load Disk Memory Buffer Pulse. Loads contents of MBH into DMB during write mode. Generated by WEP if ADC (1) and R/W (1).
MBH	Memory Buffer Hold register. 12-bit flip-flop register which buffers data between central processor and DMB. Cleared by CMBHP. Loaded in read mode with contents of DMB 0-11 by RLMBHP at end of data word on disk. Loaded with contents of central processor BMB 0-11 in write mode by WLMBHP during data break. The contents of MBH are strobed into central processor MB during read by central processor logic, and into DMB during write by LDMBP.
MRS	Memory Request Synchronizer flip-flop. Controls 16 word holdoff of DRE set by TCA, TCB, TCC, and TCD. Set by LDMAP or EMA 6 going to 0 (pulse) if DRE(1) is present. Cleared by SCLP 1 or DRE going to 1. When set, MRS allows TCA to be toggled.

Table 3-1 (Cont)
RF08 Signal Mnemonics

Mnemonic	Description
NXD	Non-eXistent Disk. Error indication. True if disk selected by EMA 7 and 8 is not installed in system. If four disks are installed, NXD will not go true, and one of the four disks will always be selected by EMA 7 and 8.
PCA	Switching Gap Gate. Goes true during 450 μs gap in disk between tracks. Used to select direct set of DRE when PCA is true and LDMAP occurs.
PCA (track generator)	Photocell flip-flop. (Maintenance use.) Set by TGP if BAC 6 is set. Cleared by SCLP 2.
PER	Parity Error flip-flop. Set to indicate read parity error. Set if R/W is clear, and ADC and BPAR are set, strobed by TCP.
PIE	Photocell Interrupt Enable flip-flop. Enables interrupt when switching gap gate is present. Set by IOT 614 (DIML) when central processor AC 4 is set. Cleared by IOT 614 (DCIM) or PCL.
ROFP	Read Overflow Pulse. Indicates last read data transfer. Set by central processor WCO pulse when R/W is 0.
R/W	Read/Write flip-flop. State determines data transfer direction. Set by IOT 604 (DMAW) for writing; cleared by IOT 602 (DMAR) for reading. Also cleared by SCLP 1.
SAD	Search ADdress flip-flop. Set to allow generation of SDMAP pulses. Set by first TAP pulse of each address word, if SAD is clear and DRE is set. Cleared at end of each address word by WDE. Set is delayed 60 ns to inhibit generation of SDMAP by first TAP pulse.
SCLP 1 and 2	Start-Clear Pulse. Generated by power clear (PCL) or IOT 601 (DMAC). Clears data transfer logic and DMA.
SDMAP	Shift Disk Memory Address Pulse. Generated by TAP if SAD is set. Pulse generated by a flip-flop which clears itself through a delay loop. 11 SDMAP pulses are generated per address word.
SDMBP	Shift Disk Memory Buffer Pulse. This pulse shifts the contents of the DMB one position toward DMB 11. Generated by TAP if ADC is set. Pulse generated by flip-flop, cleared by delay loop.
TAP	Track A Pulse. Main strobe-timing pulse for the system. Generated by timing track A of the disk. There are 13 TAP pulses for each address word.
TAG	(Maintenance) Track A Generator flip-flop. Complemented by TGP delayed if BAC 11 is set. Cleared by SCLP 2.
TBG	(Maintenance) Track B Generator flip-flop. Complemented by TGP if BAC 10 is set. Cleared by SCLP 2.
TBH	Track B Hold (also BTBH). Contents of address track read serially from disk. Compared during address search with IDMAE to locate track address. Comparison circuit operates after ADC is set, but has no logical effect on data transfer.

Table 3-1 (Cont)
RF08 Signal Mnemonics

Mnemonic	Description
TCA TCB TCC TCD	Time Counter flip-flops A, B, C, and D. Four bit counter which holds off setting DRE until 16 words have passed, after LDMAP. TCA toggled by WEP when enabled by MRS (1). Binary chain from TCA to TCD. TCD going from 1 to 0 sets DRE. Counter is held at 00002 by resetting MRS after 16th count. Cleared by SCLP 1.
TCG	Track C Generator flip-flop (maintenance). Complemented by TGP delayed if BAC 9 is set. Cleared by SCLP 2.
TCP	Track C Pulse. Generated by BTCS+ at bit-time 14 of each address word. Denotes end of address word.
TEP	Track End Pulse. Generated by 1 in timing track B at bit-time 13, while WDE is 1. This address is 10000_8, which is the address content of special address at the end of the track.
TGP	Track Generator Pulse (maintenance). Generated by IOT 642 (DMMT) if MB 9 is set. TGP controls generation of other maintenance pulses.
WCO	Word Count Overflow flip-flop. Set by LDMAP to indicate data transfer in process. Cleared by LDMBP and WCS (1) during write. Cleared by ROFP during read. Delay during write allows last data word to be written on disk. WCO (0) and DEP (1) indicates the actual end of data transfer by setting DCF.
WCS	Word Count Synchronizer. Cleared by LDMAP. Set by WCOP when Word Count Register is incremented to 0. During write, WCS indicates the WCO has occurred, and allows clearing WCO at next LDMBP. During read, WCS and WCO are complemented simultaneously.
WDE	Write Data Enable flip-flop. Set by BTCS- at bit-time 12. Cleared by WEP at bit-time 14. Set to inhibit writing data on disk, and to write parity bit.
WEPD	Word End Pulse Delayed. Generated by WEP, delayed 50 ns.
WLMBHP	Write Load Memory Buffer Hold Pulse. Generates pulse which loads MBH with data in the central processor MB. Generated when R/W (1), B BREAK true, strobed by T1. Generation of this signal is controlled by the central processor data break.
WLS	Write-Lock Status. True when the contents of the EMA select a head in the disks which has its associated write-lock switch set for lock which denotes an error signal.
WTE	WriTe Enable. True when ADC (1) and R/W (1). Level must be true to allow writing on the disk. When level is false, no write current passes through the disk head.

3.2.1.1 Track A, Strobe-Clock Track - This track contains thirteen 1's followed by a single 0 for each angular address. The output from this track is used to strobe all of the serial data and address operations in the RF08 and the RS08. Track A provides the clock rate for the disk, with 1160 ns (60 Hz) between bits. The 13th bit is used

for even parity check and the 14th bit-time is used as a gap to permit turn off/on of the write amplifier. The 14th bit-time is not provided with a TAP, preventing data transfer between data words.

3.2.1.2 Track B, Binary Address Track - The addresses are written sequentially around the track. Track B is read with the lowest order bit coming off first, and the highest order last. This allows the disk memory address logic in the RF08 to increment the DMA register by performing a serial add of plus one as the address is read and compared. The address is placed one word before the actual location in which data for that address is written. This allows the disk file to locate an angular address and begin data transfer in the next word time. An extra address, shown as special address, is provided. This address has $10,000_8$ written onto track B, which is sensed by the RF08 to instruct the disk file to switch to the next higher track. Approximately 450 μs head switching gap is provided to allow this switching to occur. The data for address 3777_8 is written during the special address word period; therefore, no data is recorded during address time 0000_8.

3.2.1.3 Track C, Word-End Track - Contains binary 1's at bit-times 12 and 14, all other bit times contain binary 0's. These bits indicate the boundaries of a data word. The binary 1 at bit-time 12 appears as BTCS- and the binary 1 at bit-time 14 appears as BTCS+. These signals are separated in the RS08 to allow them to control separate word-end functions in the RS08.

3.2.2 Disk Selection

EMA bits 7 and 8 are used to select one of the four disks that can be installed with the RF08. When only one disk is installed, it is always designated as disk 0.

A select level from the disk select circuit inhibits the reading of the address track and the reading and writing of data, except when that disk has been selected by EMA bits 7 and 8.

When more than one RS08 is installed, the address tracks of the units not selected must be disabled. A logic signal from the disk select circuit enables the recognition of the address tracks for the selected disk only. The enabled signals are then placed on a negative (-3V) OR bus between the RS08 and the RF08.

3.2.3 Track Selection

Extended memory bits 0 through 6 select the disk head using an X-Y diode matrix selector scheme. Identical paths are used for disk reading and writing of data.

The selection of the X diode matrix uses EMA bits 0, 1, 2 and 6 to select 1 of 16 data lines which go to the G286 Center-tap Selector Modules. A selected center-tap is connected to the +20 Vdc power supply through a saturated transistor with the unselected center-taps connected to the -15 Vdc supply through a resistor.

The G285 Series Switch Module is used to select one of the eight Y line pairs. A selected series which enables a pair of transistors to pass the differential read or write signals.

NOTE

Only at the coincidence of a selected Y line pair and X center-tap are the head diodes biased into conduction. Thus, only 1 of the 128 tracks can be read or written at a time.

The outputs of the eight series switches are bussed to permit the use of a single read and a single write amplifier.

3.2.4 Write Lock Out

Any of the eight Y lines can be locked out from reading or writing when bit 6 of the EMA address is 0. This allows the addresses for the lower half (addresses 0 to 377777_8) of the disk addresses to be locked out in blocks of 40000_8 words. The lockout circuits are controlled by toggle switches on the RS08 unit. When EMA bit 6 is a 1, the lockout circuits are inhibited. When a locked-out track is selected by the program, a logic level is sent to the RF08 to enable setting of the appropriate flags.

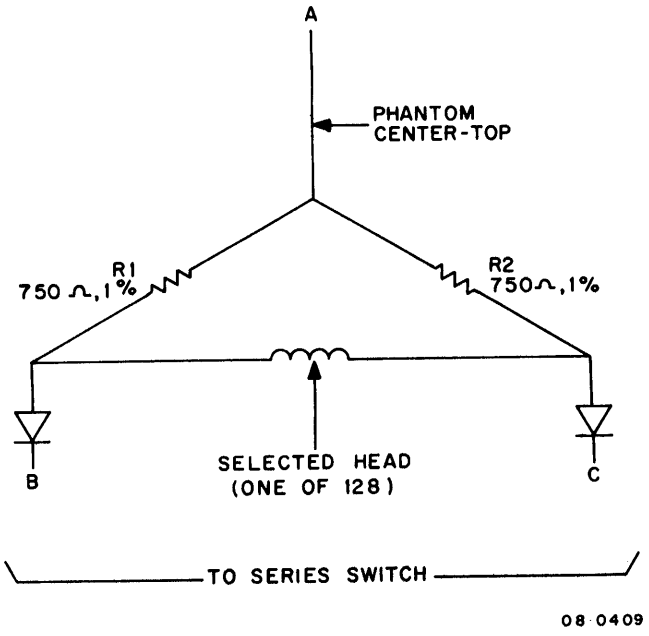


Figure 3-3 Selected Write Head Simplification Diagram

3.2.5 Writing Data

The data head selected by the EMA to write the data is described in section 3.2.3. The output from the write amplifier is connected to the same point as is the input to the read amplifier, permitting use of the signal paths for reading or writing.

A "phantom center-tap" (Figure 3-3) is used to select the direction of write current through the head. The value of resistors R1 and R2 are large compared to the resistance of the selected head. When point A is connected to +20 Vdc through a center-tap selector, the head is enabled for writing. When reading, a magnitude of current of approximately 5 mA with good balance, flows from points B and C.

Writing is achieved by connecting point B or C (one at a time) to the -15 Vdc through the write amplifier

The resistance of the head is low (5 ohms); thus, equal current will flow in R1 and R2 under steady state conditions. For example, if point B is connected to -15 Vdc (with point C floating) approximately 45 mA flows through the head windings. When point C is at -15 Vdc (point B is floating) approximately 45 mA flows in the opposite direction.

Saturation magnetic recording is used; thus, either polarity current is flowing when writing. Previously recorded data are always erased during writing.

The NRZI recording technique is used in the RS08 Disk. A binary 1 is represented by a change in the direction of the magnetic flux along the disk track, and a binary 0 is represented by no change in magnetic flux. A 1 is written by inverting the polarity of the write current in the head.

The Write Flip-Flop (WFF) is used in the RS08 Disk to determine the polarity of the write current. Since a change in magnetic flux represents a binary 1, the WFF circuit is toggled to write a 1 (See Figure 3-4).

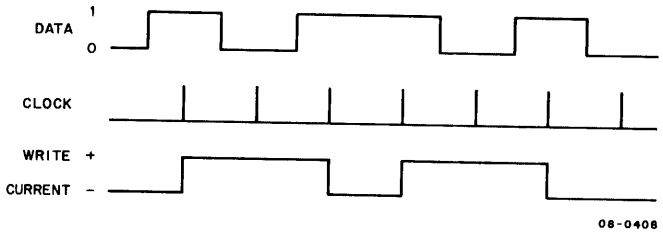


Figure 3-4 Writing Current Pulse Diagram

3.2.6 Reading Data

When data on a track is to be read, the write drivers are disabled by a logic signal from the RF08. Figure 3-5 represents the output signals from the head that has been selected. Head selection for the read mode is identical to that for the write mode. However, the output signals, which appear on the Y select lines, are supplied to an amplifier and amplitude detection circuit. Since the magnetic head can respond only to a change in magnetic flux, an output appears only when a binary 1 was written. The output voltage from the selected head is proportional to the time derivative of the magnetic flux in the head. Because of the recording surface and head parameters, the output approximates the shape of a $\cos^2$ (bell) pulse. A binary 0 is indicated for no output signal, since the magnetic flux on the disk is not altered when writing a binary 0.

3.3 RF08 BLOCK DESCRIPTION

The general block discussion of the RF08 circuits is followed by a detailed block discussion of the functions of the RF08 (See Figure 3-6).

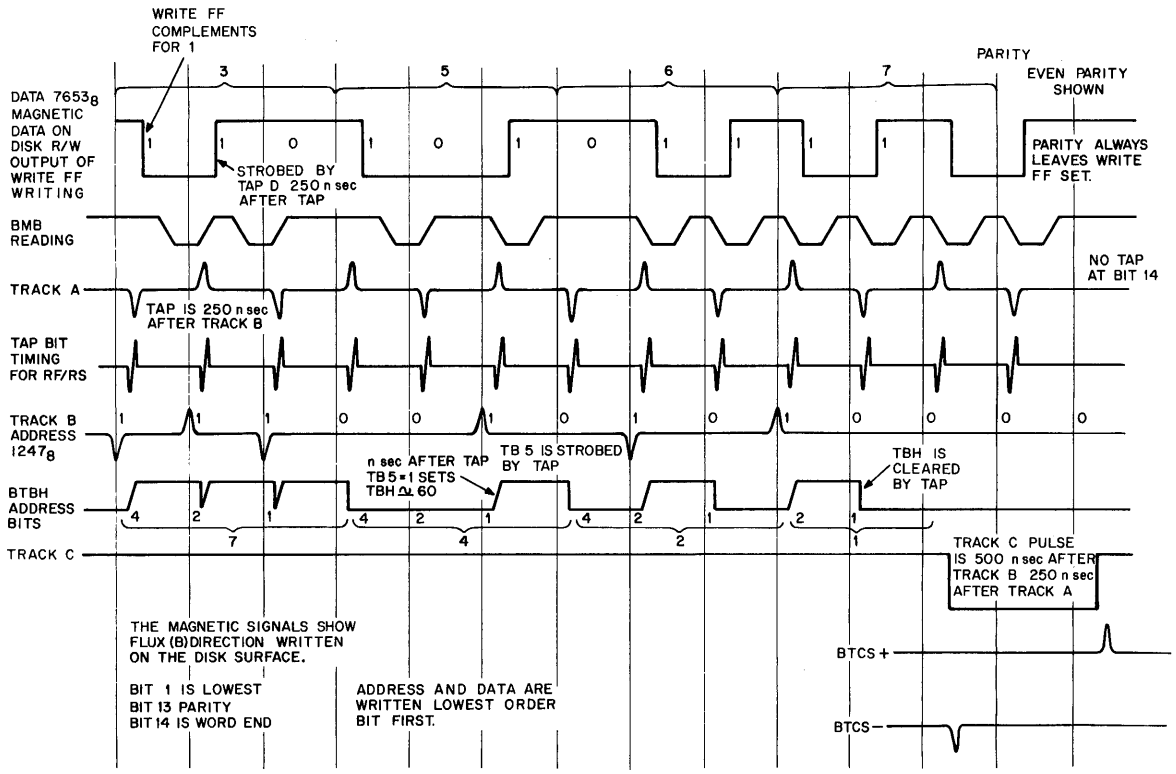


Figure 3-5 Disk Address and Data Track Timing Diagram

3.3.1 Address Registers

The RF08 has two address registers, loaded with separate program instructions. The DMA contains the lower order 11 bits of the address, which correspond to the addresses (0000_8 to 3777_8) on the RF08 track. The address loaded into the DMA is compared by a bit comparator in the address control of the RF08. This is done by shifting the address through the DMA and comparing the lowest order bit in the DMA with the bit of the address being read off the disk. The timing control provides timing signals for this function. When the angular address is located, a signal is sent to the data control to allow information transfer. After information transfer starts, the address in the DMA is incremented in the word following each data-word transfer. At the end of the data transfer the DMA contains the address of the last data word transferred; this address can be read by the PDP-8.

The EMA is loaded by a separate command from the PDP-8, except for the lowest order bit, which is loaded with the highest order bit of the DMA address. Two address transfers are required, since the 20-bit address capability of the disk file system must be loaded from the 12-bit contents of the PDP-8 accumulator. Bits 7 and 8 of the EMA select the disk, of the four disks that can be controlled by the RF08, and bits 0-6 select the head in that disk (track number) that is to be used for data transfer.

The EMA register is a 9-bit binary ripple counter, which can be cleared and loaded with a parallel jam transfer.

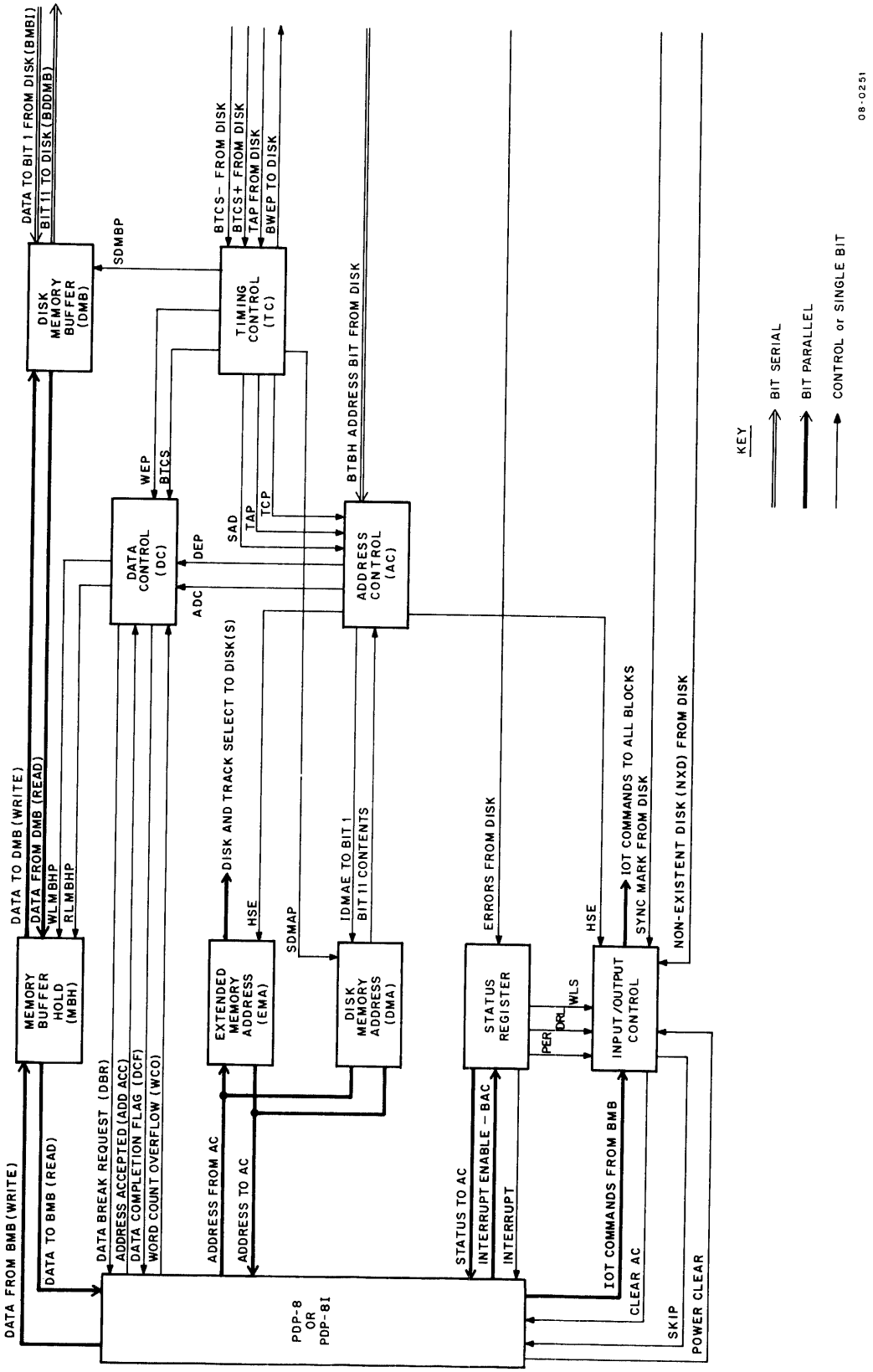


Figure 3-6 RF08 Disk Control Block Diagram

3.3.2 Memory Buffer Registers

There are two memory buffer registers. The MBH is connected to the PDP-8. It is loaded by the PDP-8 Memory Buffer in parallel transfer with data to be written on the disk, in the write mode. In the read mode, the MBH is loaded by parallel transfer from the DMB. Data in the MBH are transferred by another parallel transfer to the DMB in the write mode, and to the PDP-8 in the read mode. Since the DMB register is continuously performing a serial-to-parallel read or parallel-to-serial write conversions, two registers are required for each data word. Since only the bit-time (1160 ns) between words is available to load the DMB with data from the PDP-8, MBH is required to buffer that data.

When a word transfer is complete, data for the next word is parallel transferred into the DMB from the MBH when writing, or out of the DMB to the MBH when reading. This transfer occurs at the end of a word.

When writing, the data in the lowest order bit (DMB 11) is supplied to the disk. After each bit is written, the data is shifted down one bit, and the new bit in DMB 11 is written. After 12 shifts, the data has been shifted completely through the DMB, a clear signal clears the DMB flip-flops, and another parallel transfer of data from the MBH occurs.

When reading, the bit that is read from the disk is loaded into DMB 0, and then shifted down one bit. The lowest order bit is written onto the disk first, causing the first bit read to be in DMB 11 after all 12 bits are read. The data is then transferred in parallel to the MBH. A double rail jam transfer is used to transfer data from DMB to MBH when in the read mode. Signals from the data control determine the direction of transfer, and also the timing.

3.3.3 Address Control

The address control compares the address being read from the disk address track with the address loaded into the DMA. When the address in the DMA is located, the address control generates an ADC logic level that allows the data transfer to begin. After each word of data is written, the address control generates a DEP, which is used by the data control as an end-of-word strobe signal. The address control increments the address in the DMA by 1 using a serial add during each word following a DEP. Therefore, the DMA is incremented by the number of data words transferred.

The address control also provides an HSE signal which increments to the contents of the EMA after the last address (3777_8) is read from the address track of the disk. This allows data transfer to continue, using the next head on the disk (or the next disk when the last address on a disk has been reached). The address in the DMA is reset to 0000_8 after data has been transferred to or from the last angular address on the track.

The origin gap in the timing tracks is long enough to permit "spiral" read and write operations. During reading, the amplifier recovers from the track switching overload.

In multiple disk installations the rotational positions of the disks are not synchronized and a normal rotational positioning latency occurs when "spiralling" between disks. The overflow from the most significant EMA bit (AC bit 4) is used to reset the synchronizing logic for automatic disk switching. A normal address search is initiated with the transfer continuing after ADC is set.

3.3.4 Data Control

The data control is instructed, by decoded IOT instructions, to control either wirting or reading of data. When address control supplies an ADC signal, indicating that the angular address has been located, the data control is enabled to control transfer of data between the disk and the memory buffers as described in paragraph 3.3.2. The data transfers within the RF08 occur at the end of a data word, strobed by DEP received from the AC. In the write mode, the MBH is loaded and the data control is strobed by the T1 timing signal from the PDP-8.

The PDP-8 supplies a WCO pulse during the last transfer for which the system has been programmed. This pulse ends data transfer, and sets the DCF.

3.3.5 Timing Control

The timing pulses from disk tracks A and C are used as clock signals by the RF08. The track A pulse is a strobe pulse for address search and data transfer, and occurs in the first 13 of the 14 bit-times. The track C pulses signify the end of a data word, and are transmitted separately on two lines.

The TAP are used to shift the data through the DMA. A delay is provided that prevents shifting the DMA contents until the contents of bit 11 are set-up by the address control. The next 11 TAP pulses each are used to generate SDMAP. After the end of the 11th shift, the circuit is reset by the track C pulse (BTCS-), which occurs at bit-time 12. This holds off generation of the SDMAP for the last A pulse and the first A pulse in a data word.

Once the address confirmed signal is received from the address control, the TAP pulses are used to produce the SDMBP. These pulses continue to be produced as long as data is to be transferred to or from the disk. There are 13 SDMAP pulses developed for each data word; however, because of information transfer timing between the MBH and DMB, the 13th pulse has no effect on the data loaded into the DMB.

Two separate Track C pulses are provided by the disk. The first, occurring at bit-time 12, is BTCS-, which is used to establish a WDE signal. This signal appears as a pulse, and is used to present data transfer for the last two bit-times.

The second track C pulse is BTCS+, occurring at bit-time 14. In addition to ending the WDE hold-off period, this pulse develops the TCP and the WEP. This pulse is used by other sections of the RF08, and by the RS08 to signify the end of a data word.

3.3.6 Input-Output Control

The RF08 is controlled by IOT instructions received from the PDP-8. These instructions are decoded by the W103 Device Selection Modules in the input/output control. The octal device codes assigned to the RF08 Disk Control are 60_8, 61_8, 62_8, and 64_8. The IOP lines are used to specify the operations. Note that microprogramming of IOP lines are used for IOT's such as read (DMAR:6603) and write (DMAW:6605).

The decoded IOT instructions are gated with conditions in the RF08 and with the BMB lines to provide control pulses.

3.4 RF08 LOGIC DESCRIPTION

3.4.1 Address Selection

The address selection is divided between the track selection, and the angular address (See Figure 3-7). The angular address is located by the DMA and the address control circuits. The track selection is performed by the EMA over a 7-bit bus to the RS08. Bits 7 and 8 of the EMA select the disk in multiple-disk installations.

3.4.1.1 Locating a Track Address - There are three address tracks permanently written on the disk. These tracks are described in detail in paragraph 3.2.1. An 11-bit starting address is loaded from the PDP-8 AC into the DMA by the DMAR or DMAW command at IOP time 2 or 4. When a DRE signal is generated by the input/output control, the address control begins to compare the bits in the DMA with the bits read off track B on the Disk. Figure 3-8 is a flow diagram of address comparison for track addresses (address 0000_8 to 3777_8). The special case where address 3777_8 is followed by "special address", which causes a head switch (Figure 3-9). Referring to Figure 3-8, the sequence of events is:

a. A DMAR (6603) or DMAW (6605) is placed in the MB of the PDP-8. This generates IOT 602 or 604 in the RF08. Either IOT generates a LDMAP, which loads the contents of the AC bits 1 through 11 into DMA bits 1 through 11. Note that the content of AC bit 0 is loaded into the EMA bit 0 at the same time; however, the EMA is not involved with track address selection.

b. The DRE is set by either of two signals. If the disk is passing through the head switching gap, the LDMAP sets the DRE. If the disk is positioned on an address, MRS is set by LDMAP. The 4-bit time-counter (TCA, TCB, TCC, TCD) receives WEP, derived from BTCS+, to count to 16_{10} and reset to 0000_8, setting the DRE. This waiting time is provided as a settling time for DMA logic. Once set, DRE remains set until all the data words have been transferred, or until the last word on the disk has been used.

c. When DRE is set, at the end of a word, an enabling level is provided to allow the next TAP to set the SAD flip-flop. SAD is set by the first TAP pulse, and address search begins at the beginning of an address word.

d. The first address bit appears at the address control as BTBH and TBH. The contents of DMA 11 are ANDed, with the state of the ACH. ACH is set, resulting in the generation of true IDMAE and IDMAE-, which represent the contents of DMA bit 11. The IDMAE levels and the TBH levels are connected to an exclusive OR gate. If the exclusive OR is true, indicating that BTBH and DMA 11 contain complements, ABC is set, indicating that the bits do not compare. ABC was cleared by WEPD before address comparison began, and remains clear if the exclusive OR is not true.

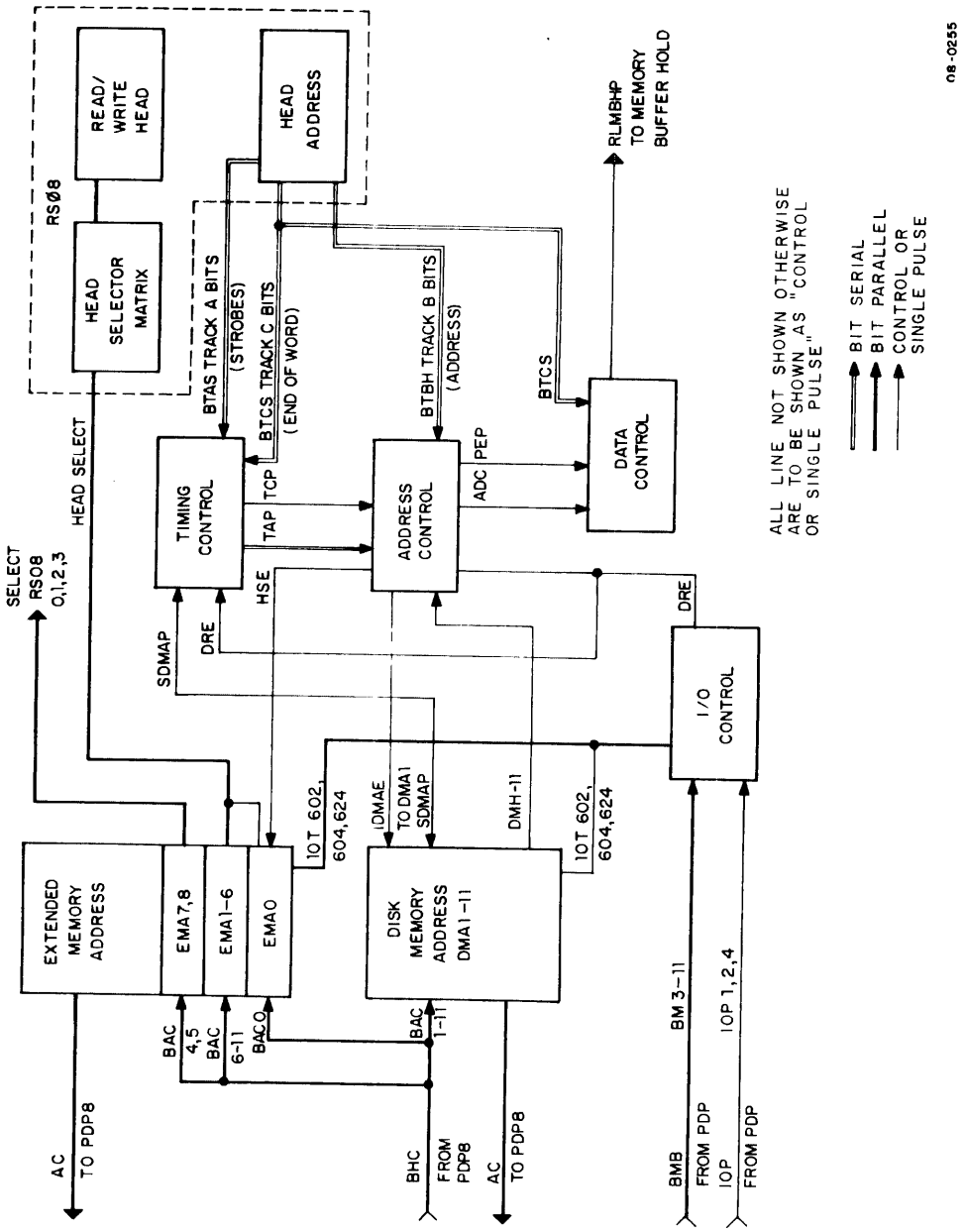


Figure 3-7 Address Selection Simplified Block Diagram

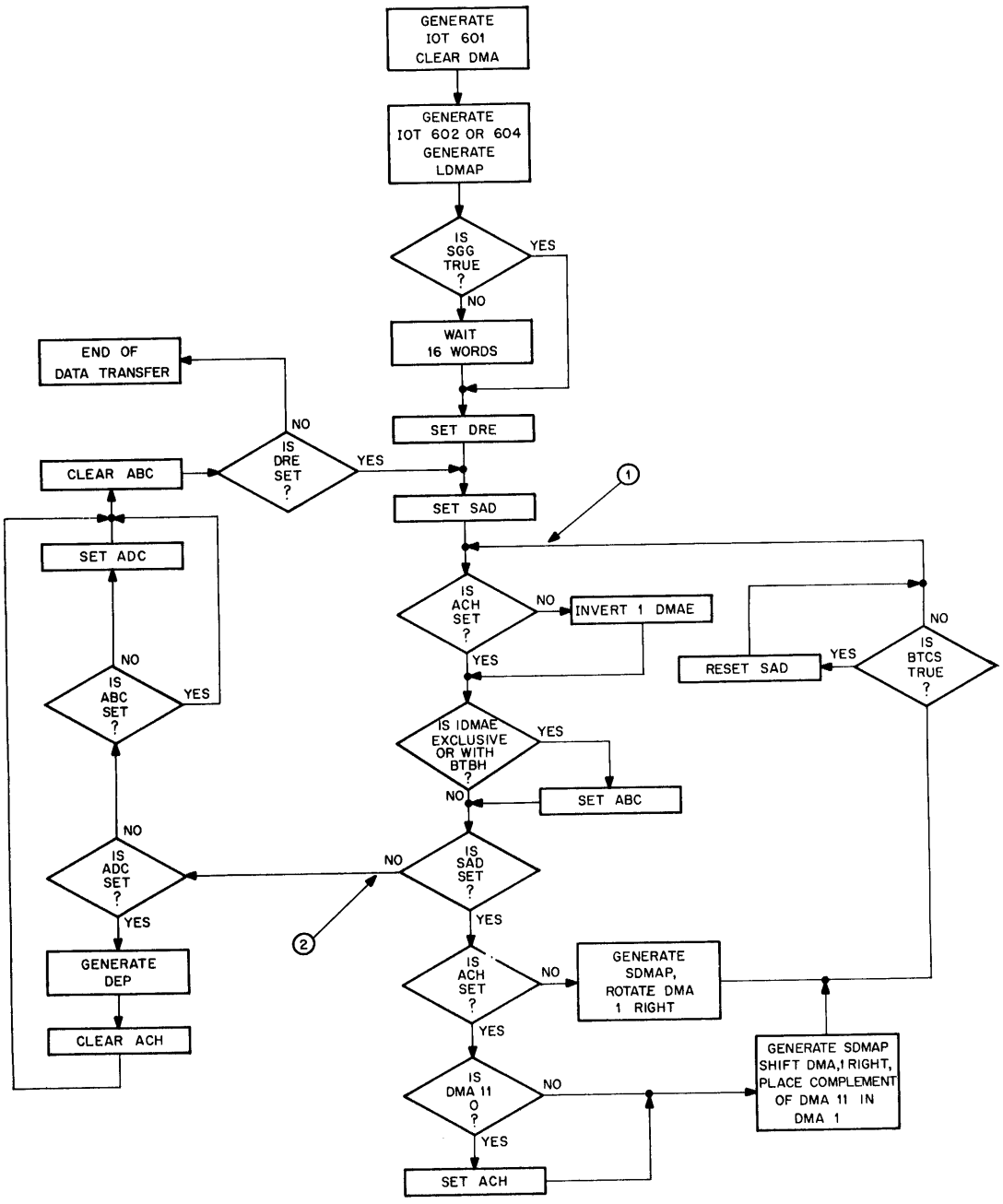


Figure 3-8 Address Flow Diagram

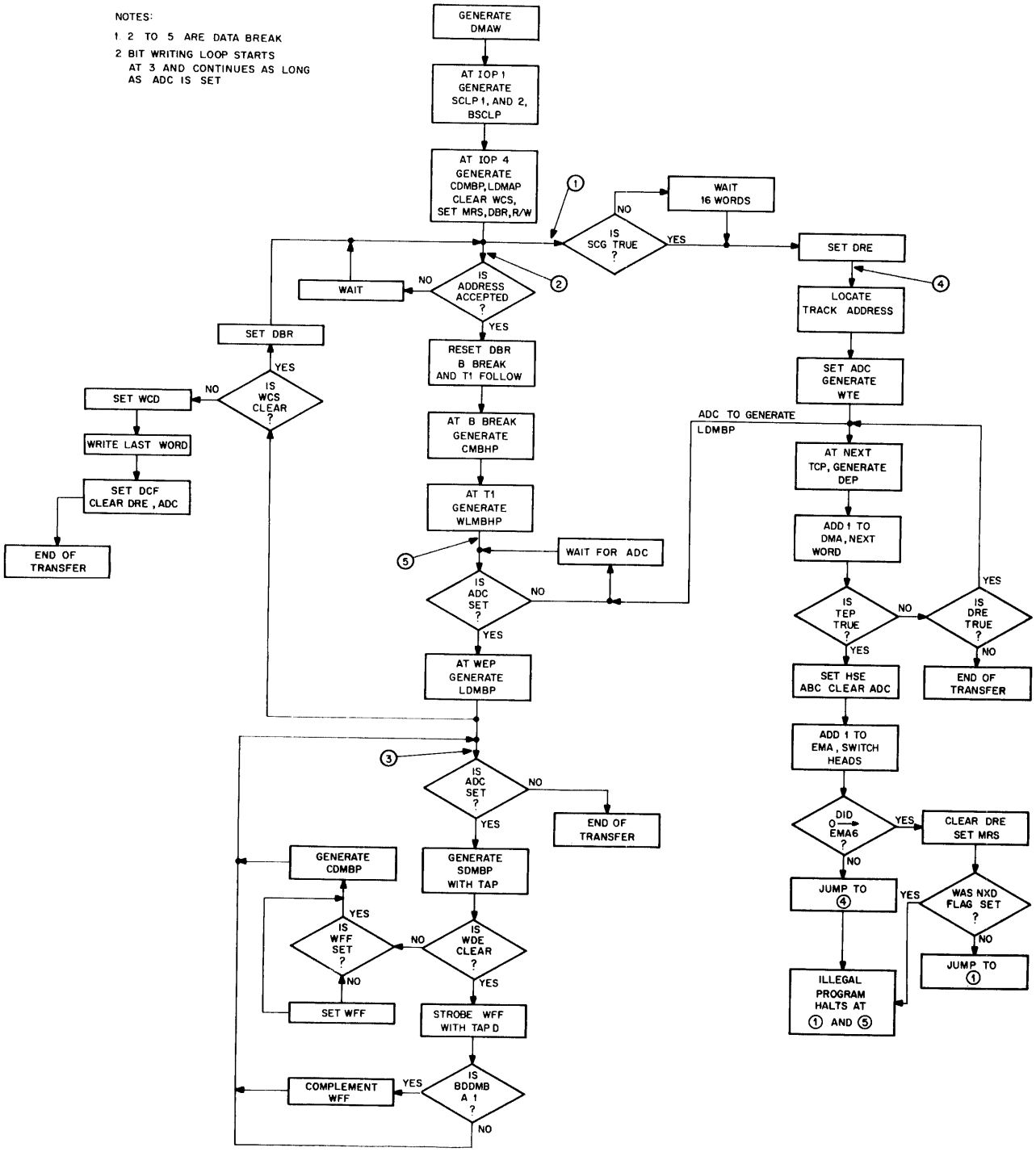


Figure 3-9 Write Flow Diagram

e. For the first bit comparison, TCP is not true, as it is generated at bit-time 14 by BTCS+. The ACH flip-flop is set previously. The second TAP pulse is ANDed with SAD, which is not set, to generate the SDMAP. The contents of the DMA are shifted one bit to the right. At the same time, the state of IDMAE is placed in DMA bit 1. This places the contents of DMA bit 11 into DMA bit 1; the result is rotation of the address in the DMA.

f. The new contents of DMA bit 11 generate a new IDMAE, and the process returns to point 1 on the flow chart.

g. The last address bit occurs at bit-time 12. This is followed by BTCS-, which resets SAD and causes a branch at point 2 on the flow chart. WDE is set resetting SAD, and inhibiting the generation of SDMAP until the first TAP pulse after SAD is reset (at the beginning of the next word). The first and thirteenth TAP pulses are prevented from generating SDMAP pulses.

h. The ADC was cleared when DRE was cleared. DRE is now set, allowing the state of the ABC to be strobed by the 13th TAP pulse. If the ABC is set, the address has not been located, since at least one bit of the DMA contents was the complement of the associated BTBH bit. In this case the next address word is compared. The first bit of the next address word is compared with the contents of DMA 11, and SAD is set by the first TAP pulse of the next address word. Another comparison of 11 bits takes place, and the process branches again, checking to see if ABC was set.

i. When the track address that corresponds to the address in the DMA is read, the ABC will be clear at bit-time 13. The 13th TAP pulse strobes a set command into the ADC. This enables data transfer starting with the next word. The process continues to point 1 on the flow chart, and continues shifting the contents of the DMA through one address word, until BTCS- is true again. The ADC was set on the last word, enabling the Track C Pulse derived from BTCS+ at bit-time 14 to strobe the generation of a Data End Pulse (DEP).

j. DEP resets ACH. The process then returns to point 1. When it reaches point 3, IDMAE contents are the complement of DMA bit 11. When SDMAP rotates the contents of the DMA, the complement of the contents of DMA 11 is placed in DMA 1. The process returns to point 1 after each DMA 11 (1) is placed in DMA 1 as a binary 0. When the content of DMA 11 is binary 0, ACH is set by SDMAP. Because of propagation delay, a binary 1 is written into DMA 1. The process returns to point 1 and the remaining SDMAP shifts place the contents of DMA 11 into DMA 1. Because the address is read off the lowest order bit first, the effect is to add one count to the DMA.

k. After the last data word is transferred, DRE is cleared by DCF. This clears ADC and also inhibits setting SAD. ABC is reset, and ACH remains set. The address control is now ready for a new address comparison when IOT 602 or 604 is generated. At the end of the data transfer, the contents of the DMA are the last address used for data transfer in read, and one more than last address in write.

3.4.1.2 Operation of the EMA - The EMA is used to address the disk and the track. Since the PDP-8 has a fixed 12-bit word length, a second word is used to load the EMA. 11 bits of the DMA address are used to load the DMA. The 12th bit, bit 0, is loaded into bit 0 of the EMA. Bits 1 through 8 of the EMA are loaded separately. While sections of the EMA are loaded with separate instructions, it operates as a single register, with EMA 0 being the lowest order EMA bit. The numbering of EMA bits is the reverse of the numbering of the PDP-8 AC bits. Therefore, the highest order bit of the EMA is bit 8, and is loaded with the contents of bit 4 of the AC, while EMA bit 6 is loaded with bit 11 of the AC.

The EMA operates as a binary counter, and is incremented once each time a head switch enable occurs. The output of the EMA is parallel binary to the disks.

3.4.1.3 Head Switch Enable (HSE) - The last address on a disk track is address 3777_8. One more address is provided, known as special address. Figure 3-2 shows the format of this address on the disk. The location of special address is the location of data for address 3777_8, because data is written during the word time following the associated address. Head switch operation differs from angular address operation, in that it increments the EMA by one count. A head-switching gap is provided immediately afterward, on the disk, allowing 450 μs for the electronics to respond to the switch. The DMA is complemented to 0000_8 by adding one count to the last angular address (3777_8); therefore, no provision is required for resetting the DMA to 0. Note that the two highest order bits (bits 6 and 7) of the EMA determine which of the four possible disks is to be addressed. If the current disk is filled, the head switching logic also switches to the next higher disk. This is signified by EMA bit 6 being complemented from binary 1 to binary 0. Re-entry into the data transfer loop is slightly different when a new disk is addressed. The differences are described in section 3.4.1.4. Referring to Figure 3-2, the logic flow for track switch is:

a. At the beginning of address word 3777_8, the DMA contains 3775_8. Note that the contents of the DMA follow the disk address location by 1 count, and that the DMA is incremented by adding 1 to its contents, not by referring to the address read from the disk. During address 3777_8, the 11 SDMAP pulses will be generated, adding 1 count to the contents of the DMA.

b. At the end of address 3777_8, the DEP clears ACH. The contents of the DMA are binary 1's, except for DMA 11, which is binary 0. During the next address (special address), another 1 is added to the DMA, leaving all 1's in the DMA at the end of this address. Data for address 3777_8 is written during the special address time, and a DEP is generated at the end of special address. This clears ACH again.

c. At the end of the special address, the ACH is clear, inverting the contents of DMA 11. The DMA contains all binary 1's. The ABC will be set, since the contents of the DMA did not compare with the track address. (This is true for every address following the one which compares and sets ADC.)

d. At the end of special address, BTCS- goes true at bit-time 12, setting WDE. The address track at special address contains the address $10,000_8$ (all binary 0's except at bit-time 13, which contains a binary 1). This 1 causes BTBH to go true at bit-time 13, which is ANDed with WDE to generate the TEP. WDE is reset by BTCS+ at bit-time 14 in the normal manner.

e. The TEP pulse is used as a set pulse at the HSE. This pulse is gated by a level at the flip-flop. For the level to be true, ADC must be set and WCO must be set, indicating that a data transfer has been occurring, and that words remain to be transferred. If these conditions are met, HSE is set. The output of HSE (1) generates an enabling level to reset ADC. However, ADC is not reset until the DEP pulse is generated at bit-time 14. Clearing ADC prevents data transfer. When ADC is reset, a pulse is sent to reset HSE.

f. HSE being set also complements EMA 0. Complementing EMA 0 adds a 1 to the contents of the EMA. Bits 0 through 6 of the EMA select the head used to read or write on the disk; adding 1 to the EMA instructs the disk to move to the next track. For a head switch on the same disk, EMA bits 7 and 8 are not changed.

g. Following special address is a time gap, the head switching gap of approximately 450 μs, and is provided to allow the head selection matrix in the RS08 to settle before attempting data transfer. A switching gap gate (PCA) is generated in the RS08. This gate is used in the disk switching function only.

h. At the end of the switching gap, address 0000_8, with its associated TAP pulses and BTCS pulses, is read. In order to continue data transfer, this address must be confirmed, and ADC set. The contents of the DMA are 3777_8 (all binary 1's); however, the ACH flip-flop is clear. ACH and the DMA11 are ORed exclusively to form IDMAE- which effectively inverts all 1's in the DMA to 0's. Each BTBH (0) is compared with the IDMAE- signal, which appears at an exclusive OR gate as 0's. DMA 11 will always be a

binary 1 as the address is shifted through the DMA, and the ACH flip-flop will not be set by the SDMAP pulses because a 0 must be present in DMA 11 at SDMAP time to set ACH. Each SDMAP pulse will shift a binary 0 into DMA bit 1; at the end of the address (word 0) the DMA will contain 0000_8.

i. At the end of the address 0 word, the ABC will be clear. The TCP pulse will strobe the contents of the ABC, and set ADC. However, the ACH flip-flop is still reset at the end of the address 0 word, because no DMA 11 (0) was seen. Setting the ADC also provides a pulse to set ACH. This prevents adding 1 to the DMA during address word 1.

j. Data for address 0000_8 is written during address word 1. A DEP is generated, clearing the ACH flip-flop, and the DMA will have 1 count added to it during address word 2, in the normal manner.

k. Note that the TEP pulse is connected to set the ABC flip-flop. This is to assure that the ABC does not compare the binary 0's in special address, and set ADC. While this cannot occur during the head switch function, it could occur at the beginning of a read or write instruction. If the DMA is loaded with 0000_8 by the DMAW or DMAR instruction, and address search starts after address 0000_8 has passed the address heads, the special address would leave the ABC clear. Therefore, TEP is used to set the ABC at special address, and prevent setting ADC.

3.4.1.4 HSE with Filled Disk - The last angular address on the last track of a disk is represented by bits 0 through 6 of the EMA being binary 1's. In this case, generation of the HSE (1), as described in 3.6.1.3 d. will cause bits 0 through 6 of the EMA to go to 0, and complement bit 7. EMA 6 going from binary 1 to binary 0 provides a pulse to reset DRE and set MRS. Head switch is accomplished as previously described. However, clearing the DRE prevents address search until 16 words have been counted. The 16 word settling time is required because a new disk has been selected. If the new disk is positioned at the switching gap, the 16 word wait is bypassed, and address search starts at address 0000_8.

3.5 WRITING DATA ON THE DISK

A discussion of writing data on the disk is as follows:

3.5.1 General

Figure 3-10 is a simplified block diagram of the functions used in writing data on the disk. Figure 3-9 is a flow diagram that shows the operations in order, and identifies the circuit components used. Address circuit operation has been described in 3.4, and discussion of the address search in this section is limited to the placing of the operation of the address circuits in their functional position as part of the writing sequence. The writing instruction is DMAW (6605_8). This instruction, at IOP time 1, clears the DMA and the MBH, and clears the RF08 logic to prepare for writing. At IOP time 4, the DMA is loaded with the address of the first data word location. A separate instruction has already loaded the EMA with the disk and track number. The three-cycle data break facility of the PDP-8 is requested. When the PDP-8 accepts this request, it locates the data for the first word and loads it into the MBH. The specified track address is located, and the data is loaded into the DMB. The data is then written on the disk serially, lowest order bit first, and a new request for a data break is sent to the PDP-8. While the data is being transferred from the DMB to the disk, a new data word is loaded into

the MBH. This continues, without issuing a new DMAW instruction, until the number of data words in the word count register have been transferred. Information required by the PDP-8 before the DMAW instruction can be issued is described in Chapter 4. If the number of words transferred is sufficient to fill one address track (or the remainder of one), the system automatically switches to address 0000_8 of the next track and continues writing. If the last address of the last track is used on a disk, the system automatically switches to the next disk, if one is installed. If not, an NXD flag is set, and can be used in the program as an error indication. However, if the disk file has the maximum of 4 disks installed, a program that exceeds the capacity of the disk file will cause the system to switch to the first address of the first disk and continue writing. At the completion of writing (word count register = 1), the last address +1 is present in the EMA and DMA.

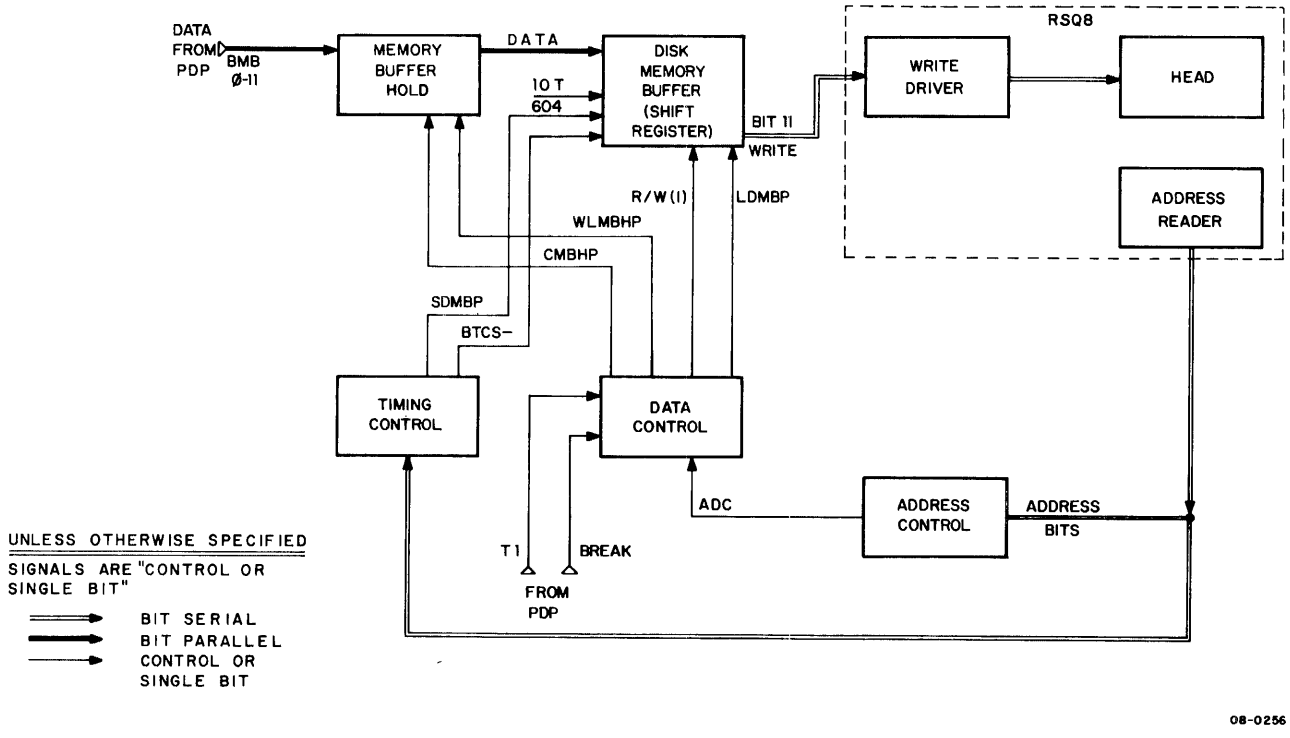


Figure 3-10 Simplified Writing Data on the Disk Diagram

3.5.2 Logic Flow when Writing

The logic signal flow when in the writing mode is discussed in sections 3.5.2.1 and 3.5.2.2.

3.5.2.1 The sequence of events that load the DMB are:

a. The DMAW command is generated in the PDP-8. At IOP time 1, the CDMAP and the SCLP's 1 and 2 are generated, clearing the DMA and RF08 logic. Note that this is the same as the operation for instruction DCMA, described in Chapter 4.

b. At IOP time 4, the DMA is loaded with the first data word address from the accumulator of the PDP-8. The DBR is set, requesting a three-cycle data break from the PDP-8. The R/W is set, indicating the write mode.

c. At this point, the logic flow divides into two alternate paths. Point 1 indicates the beginning of the address search, which is shown on this flow chart to indicate the control the address circuits have over data transfer. The operation of the address circuits is described in detail in 3.3.

d. At point 2, the system waits for an ADDRess ACCepted (ADDR ACC) signal from the PDP-8, indicating the start of the data break cycle. When ADDR ACC is received, DBR is reset. The PDP-8 supplies a B Break pulse and a T1 pulse as it continues through the data break cycle.

e. The B Break Pulse sets the CMBH, generating a clearing pulse (CMBHP) for the MBH. The T1 pulse follows. The B Break, T1, and R/W (1) are ANDed to reset the CMBH flip-flop and generate the WLMBHP 1 and 2. This loads the MBH with the contents of the PDP-8 memory buffer. After this step, the data break is completed, and the PDP-8 continues with the next instruction.

f. The disk file waits until the angular address has been located. The time required for this depends on the time required to read the track address. The minimum time for this is approximately 260 μs (this is the time it takes TCA, TCB, TCC, and TCD to count 16_{10} words of 16 μs each), which assumes that the correct track address appeared on the 17th word following the LDMAP pulse. TCA, TCB, TCC, and TCD get reset when any of the following conditions occur: a change takes place from read to write, from write to read, or a track select or disk select. This resetting allows the read/write amplifiers to settle before any reading or writing is done. If the address being searched on the disk was in the correct position during the time that TCA, TCB, TCC, and TCD were counting, then the time until that address appears again is 33.3 ms (60 Hz). The DBR is accepted at the end of the instruction in progress in the PDP-8, usually within 4 μs; therefore, no inhibiting logic is provided to prevent continuation if the DBR has not been accepted. When the address circuits locate the track address, the ADC level goes true. The WEP occurring at bit-time 14, the ADC level, and the R/W (1) level are ANDed to generate the LDMBP, which transfers the data in the MBH to the DMB.

g. The logic flow divides after LDMBP has been generated. This point is identified as 3 on the logic diagram. Continuation of the writing process is described in 3.5.2.2.

h. If the WCS is clear when LDMBP is generated, the DBR flip-flop is again set, and a new data break is initiated at point 2 on the flow diagram.

i. When the last data word is transferred to the MBH, the WCO is received from the PDP-8. This pulse sets the WCS at point 3 on the flow diagram. This inhibits the DBR flip-flop from being set by the LDMBP pulse. Instead, the LBMBP pulse sets the WCO flip-flop. The last data word is written on the disk, and the DEP, at the end of this word, sets the DCF flip-flop. End of transfer is indicated to the PDP-8 by the DCF being set. A DFSC instruction may be generated by the PDP-8 to generate a skip instruction. This is described in Chapter 4.

3.5.2.2 Writing the data word in the DMB on the disk:

a. In 3.4.2.1 the data word had been transferred into the DMB, at point 3 on Figure 3-9. In the RS08, the Write Flip-Flop (WFF) was set by the BSCLP. Before the address is confirmed, the buffered write (BWTE) level is false, inhibiting writing current. In addition, EMA bits 7 and 8 select the disk to be used. The select (SLT) level is true only for the disk that has been selected.

b. When ADC becomes true, indicating that the address has been located, it is ANDed with SLT and WFF (1) to energize the DSL+ data sense line. Write current flows in the head, writing a flux transition onto the disk. This write current writes over any previous information written on the selected track.

c. The enabling level for the WFF is provided by BWDE being true and the contents of DMB 11 being a 1. If DMB 11 is a binary 0, the enabling level is not generated. The BWDE level is true (logic 1) for the first 12 bit-times, and false (logic 0) for bit-times 13 and 14.

d. The WFF is strobed by Track A Pulse Delayed (TAPD) when BWTE is present. TAPD is generated by the track A pulse and is delayed 250 ns. If the enabling level at the WFF is true, the WFF is complemented by TAPD. This clears the WFF (for the first 1 written), and reverses the writing current, energizing DSL-. The magnetic flux written on the disk is reversed. For each 1 to be written on the disk, the WFF is complemented, reversing writing current direction.

e. If a binary 0 is to be written on the disk, the content of DMB 11 is a logic 0 at BDDMB 11. This inhibits the enabling level at the WFF. Therefore, there is no effect when TAPD strobes the WFF. The write current remains as before, and any previous data is erased.

f. If ADC remains true, TAP is used to generate the SDMBP to write the next bit.

g. After the 12th bit is written on the disk, BTCS- occurs, setting the WDE flip-flop. This inhibits the enabling level at the WFF. At the same time, however, the WDE (1) level appears as BWDE (1) at the set input to the WFF. At bit-time 13, the last TAP pulse in the data word strobes the WFF and sets it. If an even number of binary 1's were written, the WFF is already set and a binary 0 is written. If an odd number of binary 1's were written, the WFF is set from binary 0 to 1, and a binary 1 is written. This 13th bit is the parity bit, and assures that each word has an even number of binary 1's written, including a parity bit. Since this is the last bit in a word, the WFF is always set at the beginning of the next word. When reading, the number of binary 1's in a word is counted by a 1-bit register; therefore, loss of a bit in reading can be detected.

h. The process loops back to point 3, and continues as long as ADC is set. ADC can be cleared either by the end of a data transfer, or by a head switch. A head switch on the same disk re-enters the process at point 4, and a disk switch re-enters the process at point 1. When the address is confirmed again and ADC is set, the writing starts again at point 5.

i. If EMA bit 6 was a binary 1 and is incremented to binary 0 during a head switch, the current disk is filled. If the next higher disk is not installed a nonexistent disk (NXD) flag is set. However, addressing a nonexistent disk prevents the timing track signals from operating the RF08 address circuits. DRE and ADC remain clear, and the process halts at points 1 and 5. The data word loaded in the MBH cannot be written on a disk. However, the associated data break for loading this word into the MBH has been executed; and the word count and current address registers hold a count that is 1 greater than both the number of words to be transferred and the current address. (Remember that the number in the word count register is a negative number).

3.6 READING DATA FROM THE DISK

The DMAR instruction sets the RF08 logic for reading. First, the address placed in the DMA is located on the disk and once located the data is read from the disk serially, low-order bit first, and then shifted into the DMB. At the end of each word read, the data shifted into the DMB is parallel transferred into the MBH and a data break is requested. The next data word from the next higher data address is read into the DMB. When the PDP-8 accepts the DBR, the data in the MBH is strobed into the PDP-8 memory buffer, and is stored in the address specified. Each data word is read until the word count is 0. The number of words read in the block is specified before the instruction DMAW by placing the number in the word count register. The addresses to which

the data read is transferred is specified by the current register. These are both located in the PDP-8, and are described in Chapter 4. The current address is incremented by 1 each time a DBR occurs. The series of words read from the disk is transferred to a series of addresses. The word series in a block on a disk is read from adjacent addresses; that is, the first word read comes from the address specified by the DMA contents, the second word comes from the next address, etc. No addresses are skipped during a block transfer.

3.6.1 Data Flow When Reading

Figure 3-11 is a block diagram of data flow when reading. The following is a discussion of the logic flow (Figure 3-12):

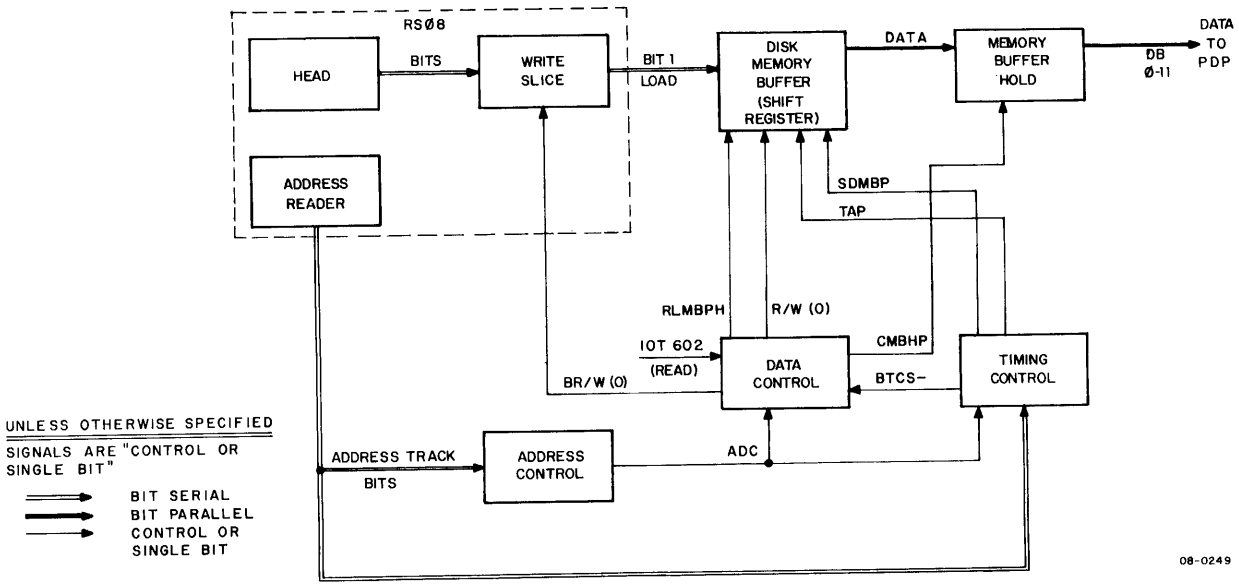


Figure 3-11 Data Transfer when Reading Block Diagram

a. The instruction DMAR is generated by the PDP-8. At IOP time 1, SCLP, and SCLP 1 and 2 pulses are generated, clearing TCA, TCB, TCC, TCD and DMA.

b. At IOP time 2, the first disk address is loaded into the DMA. The R/W flip-flop is clear, enabling the contents of the MBI in the RS08 to be read into DMB 0 when ADC becomes true.

c. The track address is located, as described in 3.4.1. ADC goes true at the end of the address word that matches the contents of the DMA.

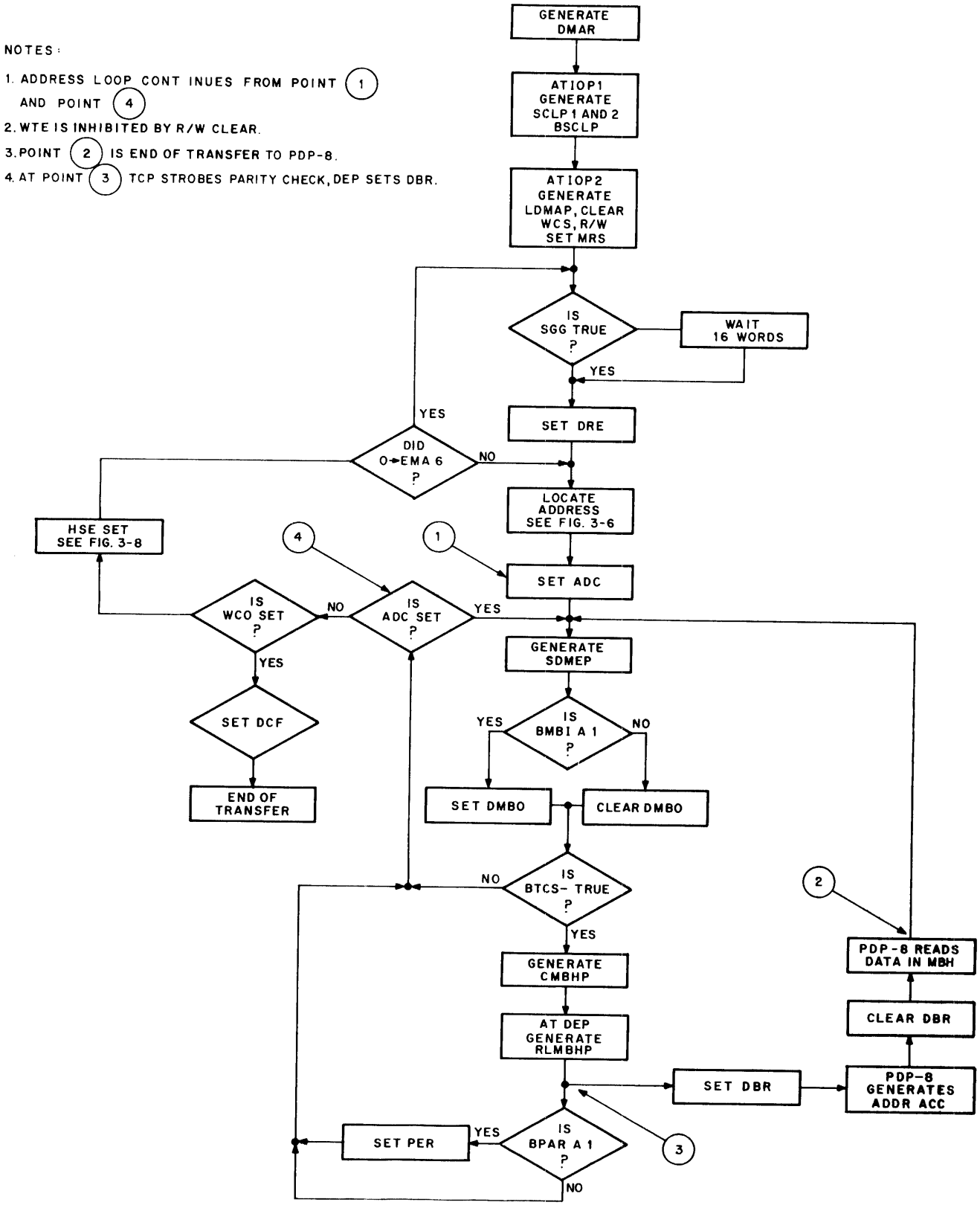


Figure 3-12 DMAR Read Flow Diagram

d. The first TAP pulse of the next data word generates the SDMBP shift pulse which shifts the DMB 1 right before any data is strobed in. There are 12 more TAP pulses in each data word, therefore, the data is shifted 12 times although SDMBP generates 13 shifts in the DMB.

e. MBI is cleared by the first TAP pulse and the contents of MBI delayed 40 ns before acting on DMB 0. This delay compensates for cable and logic skew time, insuring that MBI is present at the correct time to act upon DMB 0. The contents of MBI are jam-transferred into DMB 0.

f. After the first bit of the data word is read, BTCS- is not true, and the reading process loops. ADC is set, and the second TAP pulse generates the second SDMBP pulse. This shifts the data in DMB 0 into DMB 1. Following SDMBP, the contents of MBI, representing the second bit of information read from the disk, are loaded into DMB 0.

g. At the end of a data word (bit time 12), BTCS- goes true. This is ANDed with R/W (0) and ADC (1) to generate a CMBHP, which clears the MBH. At bit time 14, BTCS+ goes true, generating the TCP pulse. This generates DEP which is ANDed with R/W (0) to generate the Read Load Memory Buffer Hold Pulses (RLMBHP 1 and 2).

h. RLMBHP 1 and 2 transfer the data in the DMB to the MBH. Only after all 12 data bits have been strobed into DMB 0 and shifted are RLMBHP 1 and 2 generated. The first data bit strobed, which is the lowest order bit, is not in DMB 11.

i. RLMBHP 1 and 2 is ANDed with WCS (0) to set Data Break Request (DBR). This is shown at point 3 on the flow diagram. WCS will inhibit a DBR after the PDP-8 word count register becomes 0000_8. This signifies the end-of-transfer.

j. When the PDP-8 accepts the DBR, it generates ADDR ACC as part of the three-cycle data break. This clears the DBR flip-flop. The data in the MBH is strobed into the PDP-8 MB. This point is the end of read transfer between the disk and the PDP-8. If words remain to be transferred (indicated by WCO being negative), the transfer loops back to point 1 on the flow chart.

3.6.2 Operation at the End of an Address Track

When all of the data from one address track has been read, and data transfer is to continue at the beginning of the next track, ADC is cleared, and data transfer is inhibited until the switch is completed. When the switch is completed, ADC is set again, and data transfer continues from address 0000_8 of the new track selected. The automatic head switch to the new track increments the EMA by 1, and the new track number is the old track number +1. Operation of the head switching logic is described in detail in 3.4.1.3. Operation at the end of a disk, when a new disk is automatically selected, is described in 3.4.1.3 and 3.4.1.4. Figure 3-12 shows this function in the read sequence.

On Figure 3-12, at point 4, the program branches. If ADC is clear, and WCO is set, HSE is set to indicate the end of a track. The EMA is incremented, and the next head is addressed. If EMA 6 did not go to 0, the new head is on the same disk, and address search begins at address 0000_8. This address is confirmed, and reading transfer begins at the next address time. The data is delayed one word from its associated address; therefore, the first data will be read from address 0000_8. If EMA 6 did go to 0, a new disk has been addressed. If the switch trys to find the new disk at any point on a track other than the head switching gap, DRE is cleared to prevent address search. When address 0000_8 is located on the new disk, reading begins again.

3.6.3 End of Data Transfer

The number of data words transferred is specified by the number placed in the Word Count Register (WCR) before the DMAR instruction is generated. Each time that a data word is transferred, the WCR is incremented by 1. The 1 is added before the data is transferred, and before the contents of the WCR are checked. If the contents of the WCR are 0, WCO is generated. Operation is similar to the execution of an ISZ instruction, except that the WCO pulse is generated, rather than a skip. In a read transfer, the WCO pulse clears the WCO flip-flop immediately, and sets the WCS flip-flop at the same time. The data word corresponding to the last DBR is transferred. The next data word on the disk is read into the DMB and loaded into the MBH. However, DBR is not set. DEP 1 and WCO (0) are ANDed at the input to the DCF flip-flop, setting DCF.

CHAPTER 4

OPERATION AND PROGRAMMING

4.1 INTRODUCTION

Operation of the RF08 and RS08 is under program control of the computer. The only operator controls are the write lockout switches (Figure 4-1) located on the RS08 logic chassis.

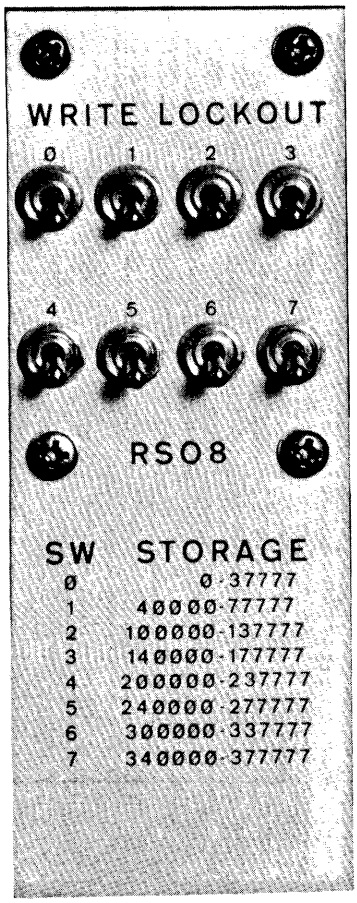


Figure 4-1 Write Lockout Switch Diagram

While the discussion in this chapter refers generally to a single RS08, the other RS08's in an expanded system are connected in parallel to the RF08, and the discussion is equally applicable to all of the RS08's in a system, except where noted.

The RS08 motor power control is independent from the computer power control, and should always be energized. When the disk is at rest, the heads are in contact with the disk; excessive starting and stopping causes wear to the disks and the heads. When the disk is operating, the heads are held a small distance from the disk by a cushion of air. During installation, system primary power is connected so that disk power is separate from the computer power control, which also controls logic power in the RF/RS08.

4.2 TABLE OF INSTRUCTIONS

Table 4-1 shows the instructions used to program the RF08/RS08. All of the instructions use the standard IOT instruction with IOP pulses as described in the central processor maintenance manuals.

Table 4-1
Mnemonic and Octal Code Instructions

Mnemonic	Octal Code	Description
DCMA	6601	Generates System Clear Pulse (SCLP) at IOP time 1. Clears disk memory address, parity error flag, data request late flag, and sets logic to initial state for read or write. Does not clear interrupt enable or extended address registers.
DMAR	6603	Generates SCLP at IOP time 1 (see DCMA). At IOP time 2, the computer loads DMA with contents of AC and then clears the AC. Read continues for number of words in WC register (address 7750 of PDP-8).
DMAW	6605	Generates SCLP at IOP time 1 (see DCMA). At IOP time 4, the DMA is loaded with the contents of the AC and the AC is then cleared. The Data Break Request (DBR) flag is set. When the disk angular address is located writing begins, the disk address is incremented for each word that is written.
DCIM	6611	Clear the disk interrupt enable and the extended address registers at IOP time 1. This instruction, with DCMA, clears all flags.
DSAC (Maintenance Instruction)	6612	At IOP time 2, skip the next instruction if ADdress Confirmed (ADC) is true, indicating that DMA address and disk angular address compare (ABC is clear at TCP). The AC is then cleared.
DIML	6615	At IOP time 1, clear the interrupt enable and the memory address extension register. At IOP time 4, load the interrupt enable and memory address extension register with data in the AC and clear the AC.
DIMA	6616	Clear the accumulator at IOP time 2. At IOP time 4, load the contents of the status register into the AC for evaluation. Contents of the status register are saved. Similar to DSAC; however, MB9 is a binary 1, inhibiting skip on ADC.
DFSE	6621	Skip next instruction is enabled at IOT time 1 if data request late, parity parity error, write locked track selected or nonexistent disk (NXD) flag set.
DFSC	6622	Skip next instruction if the Data Completion flag (DCF) is set.
DISK	6623	Skip next instruction if either the error or completion flag is set, or both. Skip occurs at IOP time 2, MB11 (1) is used as a logic level.
DMAC	6626	Clear the AC at IOP time 2. Load the contents of the DMA into the AC at IOP time 4. The contents of the DMA are not disturbed.
DCXA	6641	Clears the 8 EMA register bits.

Table 4-1 (Cont)
Mnemonic and Octal Code Instructions

Mnemonic	Octal Code	Description
DXAL	6643	At IOP time 1, clears the 8 EMA register bits (same as DCXA). At IOP time 2, loads the EMA with bits 4 through 11 of the AC. Data in bits 0 through 3 of the AC are ignored. The AC is cleared at the end of IOP time 2. See Figure 4-2.
DXAC	6645	Clears the AC at IOP time 1. At IOP time 4, the 8 EMA register bits are loaded into bits 4 through 11 of the AC. The contents of the EMA are not disturbed.
DMMT	6646	For Maintenance purposes only. With the appropriate maintenance cable connections and the disk disconnected from the RS08 logic the following standard signals may be generated at IOT 646 and associated AC bits. AC is cleared. The maintenance register is initiated by issuing an IOT 601 command. AC_{11} (1) → TTA pulse AC_{10} (1) → TTB pulse AC_{9} (1) → TTC pulse AC_{7} (1) → DATA PULSE (DATA HEAD #0) AC_{6} (1) + 1 → Photocell AC_{0} (1) + 1 → DBR Setting DBR to binary 1 causes Data Break Request in computer.

NOTE

TTA must be generated to strobe TTB signal into address comparison network.

Two instructions initiate the operation of the three-cycle data break facility. These are the instruction DMAW, which loads the Disk Memory Address (DMA) with the contents of the AC and begins writing; and the instruction DMAR, which loads the DMA with the contents of the AC and begins reading.

4.3 ADDRESS CONFIGURATION

To address the maximum storage capability of the Disk system (1,048,576 words), a 20 bit binary address is required. The lower order 12 bits are called the disk memory address (DMA), and are loaded with the contents of

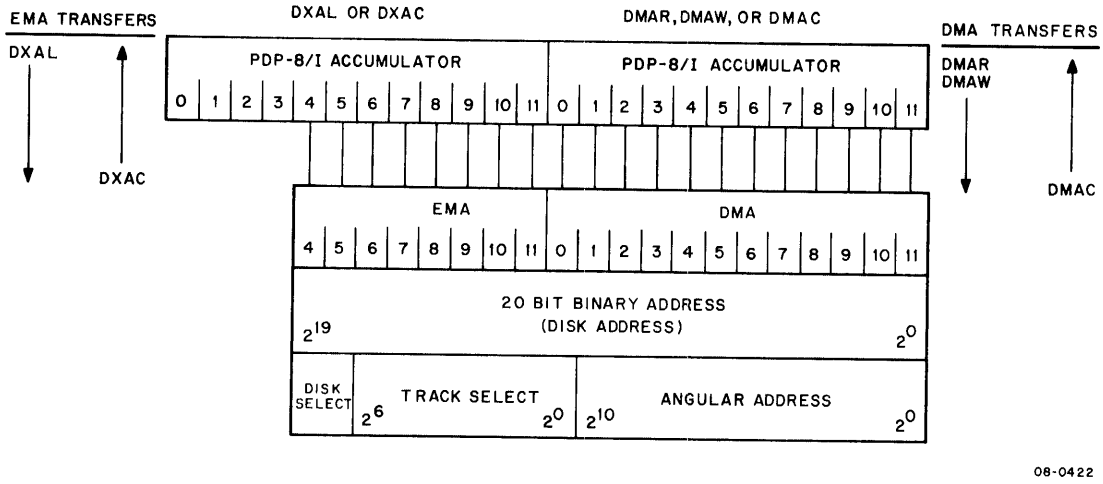


Figure 4-2 EMA and DMA Transfer Diagram

the accumulator by the DMAW write or the DMAR read instruction.

The higher order eight bits, the Extended Memory Address (EMA), are loaded from bits 4 through 11 of the PDP-8 accumulator. Refer to Figure 4-2 for this transfer.

Assignment of the PDP-8 AC bits is chosen to form a 20-bit true binary address. Since there are 2048 words per track, 11 bits are required to determine the angular address. For 128 tracks per disk seven bits of the address are required. Similarly two bits are required to select one of four disks. Thus sub-fields of the EMA and DMA are related to the actual physical placement of data bits.

It is intended that the average program be concerned with a true binary address rather than with angular addresses, tracks, or disks.

Sequencing across tracks or disks is program transparent except for disk switching latency.

The contents of the EMA are loaded into the PDP-8 AC by the DXAC instruction. This instruction clears the AC at IOP time 1 and transfers the contents of the EMA to the AC at IOP time 4. Since AC bits 0 through 2 are not involved in the EMA address, these bits will be zeroes after the DXAC command.

The highest order bit of the EMA, bit 0, is programmed by the instructions for the DMA. The EMA instructions operate on EMA bits 1 through 8. Figures 4-1 and 4-2 show this division. Since the RF08 is programmed with a 2-word absolute address, this division becomes significant only to the maintenance of the RF08 and for critical software timing.

4.4 WRITING DATA ON THE DISK

The DMAW instruction establishes a data break request for the PDP-8. When the request is acknowledged by the PDP-8, a three-cycle data break transfer is selected by the interconnecting wiring. Before data transfer can occur, two words of information must be loaded into the PDP-8 memory. Memory locations 7750_8 and 7751_8 are specified by hard wiring in the RF08 as the Word Count (WC) and Current Address (CA) registers, respectively, for the disk file. The number placed in the WC register (address 7750_8) is the two's complement negative of the number of words to be transferred. That is, if seven data words are to be transferred, 7771_8 is loaded into address 7750_8. The CA (core memory location 7751_8) is always incremented BEFORE use, therefore, it is set to one less than the core memory location to be affected by the next transfer.

For example, if a block transfer is to write core locations 4000_8 through 4006_8 onto the disk, the WC register should be loaded with 7771_8 and the current address register with 3777_8 before issuing the DMAW IOT. The PDP-8 will then place the contents of address 4000_8 in its Memory Buffer (MB), and strobe these contents into the RF08 Memory Buffer Hold (MBH) to begin the transfer.

Once the PDP-8 completes the 3-cycle data break, it returns to the program. The RS08 writes the information loaded into the MBH onto the disk. At the end of writing, the RF08 generates another Data Break Request (DBR), and the three-cycle data break is repeated. The end of the transfer is signaled to the RF08 by the Word Count Overflow (WCO) from the PDP-8 when the RF08 requests the last data word to be written. When the transfer is complete, (DCF set) the DMA, and EMA registers in the RF08 contain the address of the last data word written.

4.5 READING DATA FROM THE DISK

Reading uses the 3-cycle data break facility of the PDP-8 as described in the preceding paragraph. Before starting a read cycle, one less than the first core address into which information read from the disk is to be transferred must be placed in address 7751_8. The number of words to be transferred must be placed in address 7750_8 as the 2's complement. The Extended Memory Address (EMA) must be placed in the EMA from the PDP-8 accumulator with the DXAL instruction. See paragraph 4.3 for a discussion of loading the memory address. The initial disk address is placed in the PDP-8 accumulator, to be transferred at the beginning of the DMAR read command. After the DMA address is loaded, the address on the disk track is located and reading begins. At the end of the word, the data is transferred from the Disk Memory Buffer (DMB) to the Memory Buffer Hold (MBH), and the Data Break Request (DBR) flag is set. The DMB is now free to read the next data word, as the PDP-8 accepts the data word in the MBH, resetting the DBR flag. As the PDP-8 goes through its data break cycle, initiated by accepting the DBR flag, it adds a 1 to both the word count (in 7751_8) and the current address (in 7751_8). When the next data word has been transferred to the DMB, the cycle repeats. This continues until the word count becomes 0, which sets the Data Completion Flag (DCF), ending the transfer. At the end of a data transfer one greater than the last disk address from which data was transferred is contained in the DMA and EMA, which may be read into the PDP-8.

The address 7751_8 contains the last address into which data was stored in the PDP-8 memory. Address 7750_8 will contain 0000_8.

4.6 DATA TRANSFER INVOLVING TWO DISKS

If more than one disk is installed, a transfer can start on one disk and end on a second disk. The switching between disks is made automatically by the RF08. That is, no additional instructions are required in the program. Since the angular positions of RS08M disks are not synchronized, an accessing latency will occur when the transfer sequences from the last address of disk n to the first address of disk n +1 takes place.

4.7 OVERFLOW OF DISK CAPACITY

When less than four disks are controlled by an RF08 Control, a read/write transfer from the last physical address causes the Non-eXistent Disk (NXD) flag to be set.

If four disks are controlled by a RF08 Control, the addressing "wraps around". That is, the addressing will sequence from address $3,777,777_8$ to 0_8 without setting the NXD flag. Transfers will continue as described in paragraph 4.5, Data Transfers Involving Two Disks.

When switching disks, the RF08 logic must resynchronize to the new timing tracks. Also, when switching tracks on a given disk, a delay must be provided to permit the read amplifier to recover. The synchronizing or amplifier recovery requires 16 word times. Thus, the minimum access time is 260 μs for 60 Hz disks and 320 μs for 50 Hz disks. The origin gap is of sufficient length (450 μs) to permit spiral reading or writing.

The write to read recovery of the data amplifier must be considered for specialized programming applications. The amplifier recovery time is dependent on the data previously written. Worst case occurs after a 2048_{10} write of all zeros. Best case is defined by the minimum access time.

4.8 PROGRAMMING DIFFERENCES BETWEEN RF/RS08 AND DF32.

Programming for the RF/RS08 follows the general layout of programming for the DF32. Table 4-2 lists the mnemonic instructions for the RF/RS08 and the corresponding octal code and the corresponding information for the DF32. Each instruction is followed by comments on the differences between the two units. The addressing of both disks is similar; however, the RS08 has 2^7 tracks, while the DF32 has only 2^4. This added addressing capability is placed in the Extended Memory Address (EMA) register, which has been extended with three more significant bits. The most significant two bits address the disk by number (disk 0-3), in both units. Where the mnemonics differ, the DF32 mnemonic can be used to obtain the desired octal code during assembly.

Table 4-2
DF32 Instructions Compared with RF/RS08 Instructions

DF32 Mnemonic	Octal Code	RF08 Mnemonic	RF08 to DF32 Comparison
DCMA	6601	same	Identical functions.
DMAR	6603	same	Identical functions.
DMAW	6605	same	Identical functions.
DCEA	6611	DCIM	Clears interrupt enable, does not clear EMA. On both units, clears memory address extension.
DSAC	6612	same	Identical functions.
DEAL	6615	DIML	Similar, except functions transmitted from the AC are different. EMA information not transmitted. See DXAL.
DEAC	6616	DIMA	Similar, except that functions transmitted to the AC are different. See DXAC.
DFSE	6621	same	Instruction is skip on error, rather than skip -- no error. NXD added as an error.
DFSC	6622	same	Identical function.
(none)	6623	DISK	New instruction. Skips on error or data completion, or both. (DFSE and DFSC combined). Skip enabled at IOP 2.
DMAC	6626	same	Identical functions.
(none)	6641	DCXA	Clears EMA.
(none)	6643	DXAL	Clear and load EMA with information in the accumulator.
(none)	6645	DXAC	Clear accumulator and load address in EMA into the accumulator.
(none)	6646	DMMT	Maintenance instruction. See description in Table 4-1.

4.9 INSTRUCTION AND DATA TRANSFER EXECUTION TIMES

4.9.1 IOT Execution

All of the instructions used by the central processor to control the RF08 are IOT instructions. These are fully described in the maintenance manual for the central processor. In the PDP-8 series, execution time for an IOT instruction is 4.25 μs.

4.9.2 Data Transfer

Each 12-bit data word transferred require a 3-cycle data break, which takes 4.5 μs. Timing of the Data Break Requests is controlled by operation of the disk file, and is asynchronous with respect to the central processor operation. The central processor acknowledges the highest priority Data Break Request at the end of an instruction cycle. After all data breaks are serviced, the central processor continues with the next instruction.

4.9.3 Data Break Priority

Two factors affect the latency between the DBR and the transfer of data between the PDP-8 and the RF08.

First, the data break can not be honored until completion of the current instruction which can be up to 18.5 μs for worst case conditions such as EAE (optional).

Second, any outstanding break requests from higher priority devices must be honored before responding to the RF08 DBR.

If the particular installation uses the DM01 Data Multiplexer the RF08 system should be attached to the device zero port so that it is the highest priority data break device.

The RF08 is provided with the Data Request Late (DRL) flag to indicate that a DBR was not honored in time for normal operation. If the DRL is set, one or more words will have been omitted on a read (although the correct number of words will have been transferred). Similarly on a write, too many words will be transferred from core, but one or more will be missing "in the middle".

CHAPTER 5

MODULE CIRCUIT SCHEMATICS

5.1 INTRODUCTION

The Module schematic diagrams in the Chapter pertain to the B, S, and W Series Modules used in the RF08 Disk Control and the RS08 Disk. Tables 5-1 and 5-2 lists the Modules and the quantity of each used in the System.

Table 5-1
B, S, and W RF08 Modules

Figure	Module Type	Quantity	Description	Drawing Number
5-1	B133	7	Diode Gate	B-CS-B133-0-1
5-2	B134	3	Diode Gate	B-CS-B134-0-1
5-3	B135	4	Diode Gate	B-CS-B135-0-1
5-4	B137	1	Diode Gate	B-CS-B137-0-1
5-5	B165	11	Diode Inverter	B-CS-B165-0-1
5-6	B212	5	Dual RS Flip-Flop	C-CS-B212-0-1
5-7	B310	3	Delay Line	A-RS-B-310
5-8	B311	1	Tapped Delay Line	B-CS-B311-0-1
5-9	B312	1	Diode Gate	B-CS-B312-0-1
5-10	B611	1	Pulse Amplifier	B-CS-B611-0-1
5-11	B683	8	Bus Driver	B-CS-B683-0-1
5-12	S123	10	Diode Gate	
5-13	S202	8	Dual Flip-Flop	B-CS-S202-0-1
5-14	S203	7	Triple Flip-Flop	B-CS-S203-0-1
5-15	S206	18	Dual Flip-Flop	B-CS-S206-0-1
5-16	W103	8	Device Selector	C-CS-W103-0-1

Table 5-2
B, S, W, and G RS08 Modules

Figure	Module Type	Quantity	Description	Drawing Number
5-1	B133	2	Diode Gate	B-CS-B133-0-1
5-2	B134	1	Diode Gate	B-CS-B134-0-1
5-3	B135	1	Diode Gate	B-CS-B135-0-1
5-4	B137	1	Diode Gate	B-CS-B137-0-1
5-17	B152	3	Binary to Octal Decoder	B-CS-B152-0-1
5-5	B165	2	Diode Inverter	B-CS-B165-0-1
5-18	B172	1	Diode Gate	B-CS-B172-0-1
5-6	B212	2	Dual RS Flip-Flop	B-CS-B212-0-1
5-19	B301	3	Delay One Shot	B-CS-B301-0-1
5-9	B312	1	Diode Gate	B-CS-B312-0-1
5-10	B611	1	Pulse Amplifier	B-CS-B611-0-1
5-11	B683	2	Bus Driver	B-CS-B683-0-1
5-20	G085	4	Disk Read Amp and Slice	B-CS-G085-0-1
5-21	G284	1	Disc Writer	B-CS-G284-0-1
5-22	G285	4	Series Switch	B-CS-G285-0-1
5-23	G286	4	Center Tap Selection	B-CS-G286-0-1
5-24	R002	1	Diode Cluster	B-CS-R002-0-1
5-25	R111	1	Diode Gate	B-CS-R111-0-1
5-26	R302	1	Delay	B-CS-R302-0-1
5-27	R303	1	Integrating One Shot	B-CS-R303-0-1
5-15	S206	0	Dual Flip-Flop	B-CS-S206-0-1

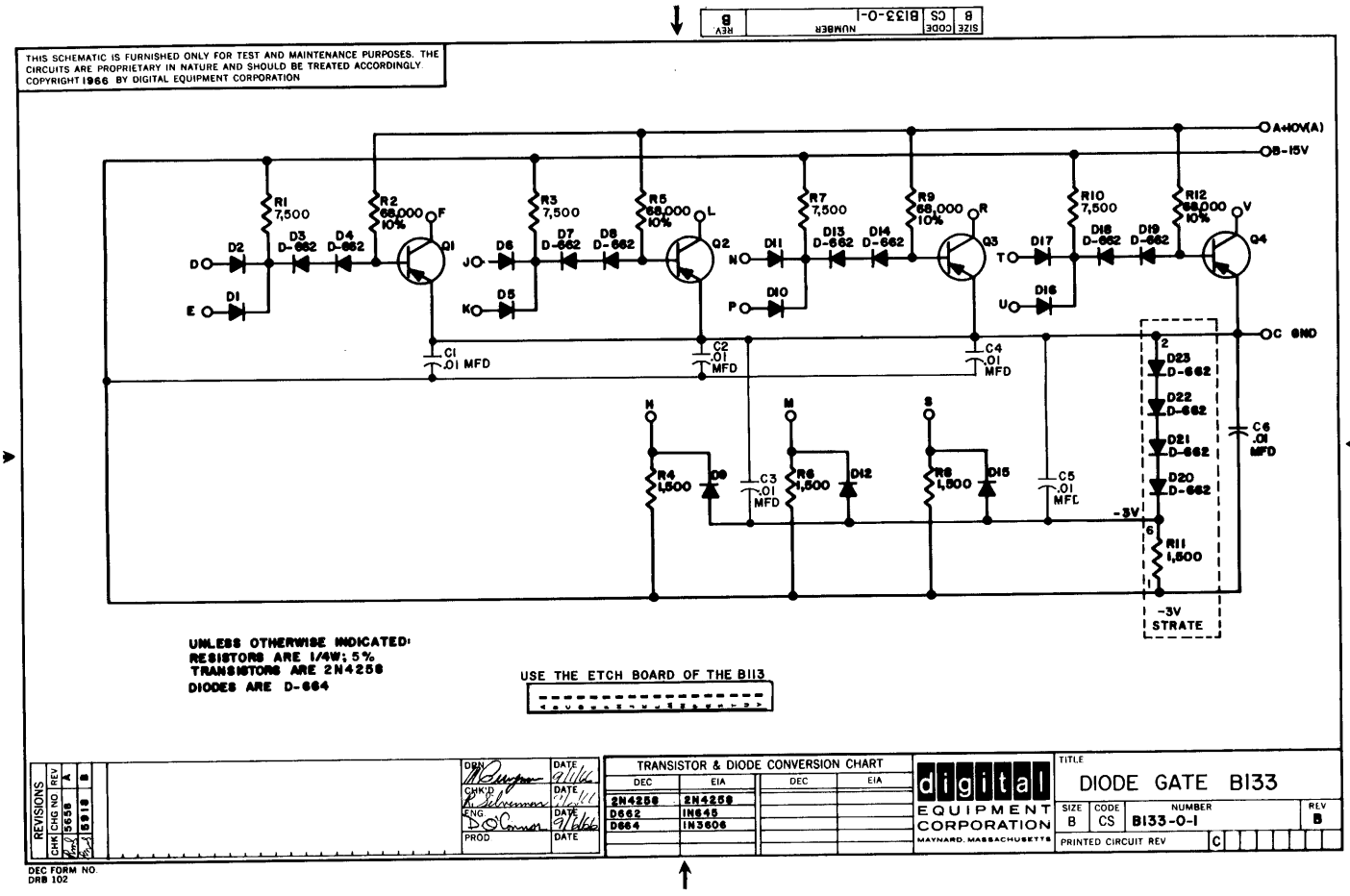


Figure 5-1 Diode Gate B133

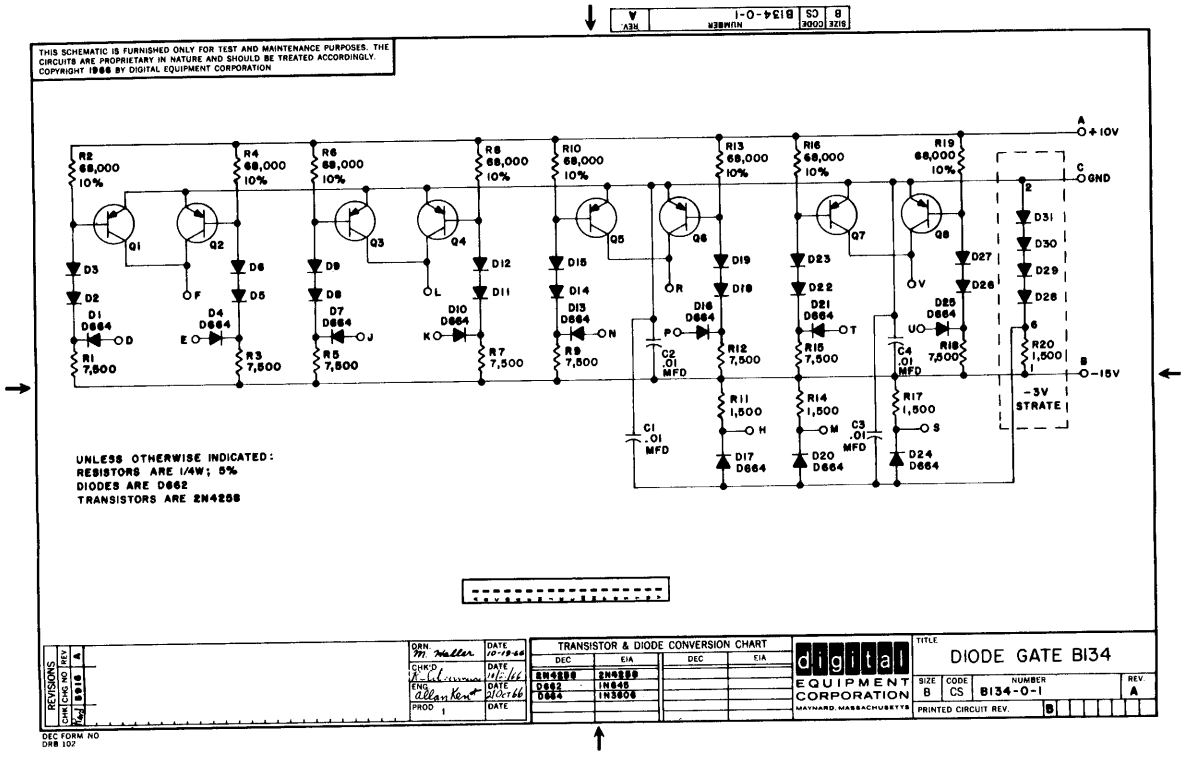


Figure 5-2 Diode Gate B134

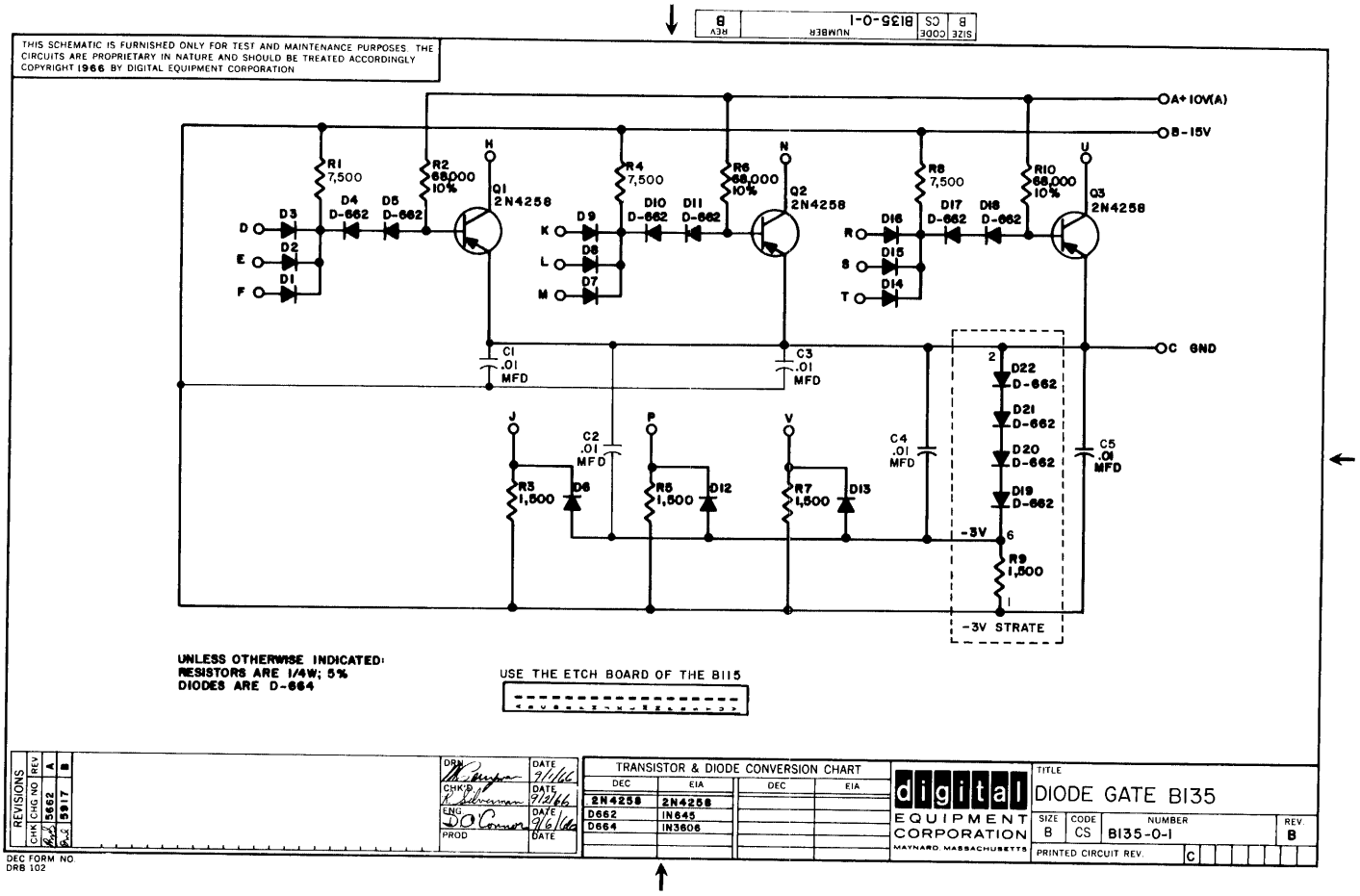


Figure 5-3 Diode Gate B135

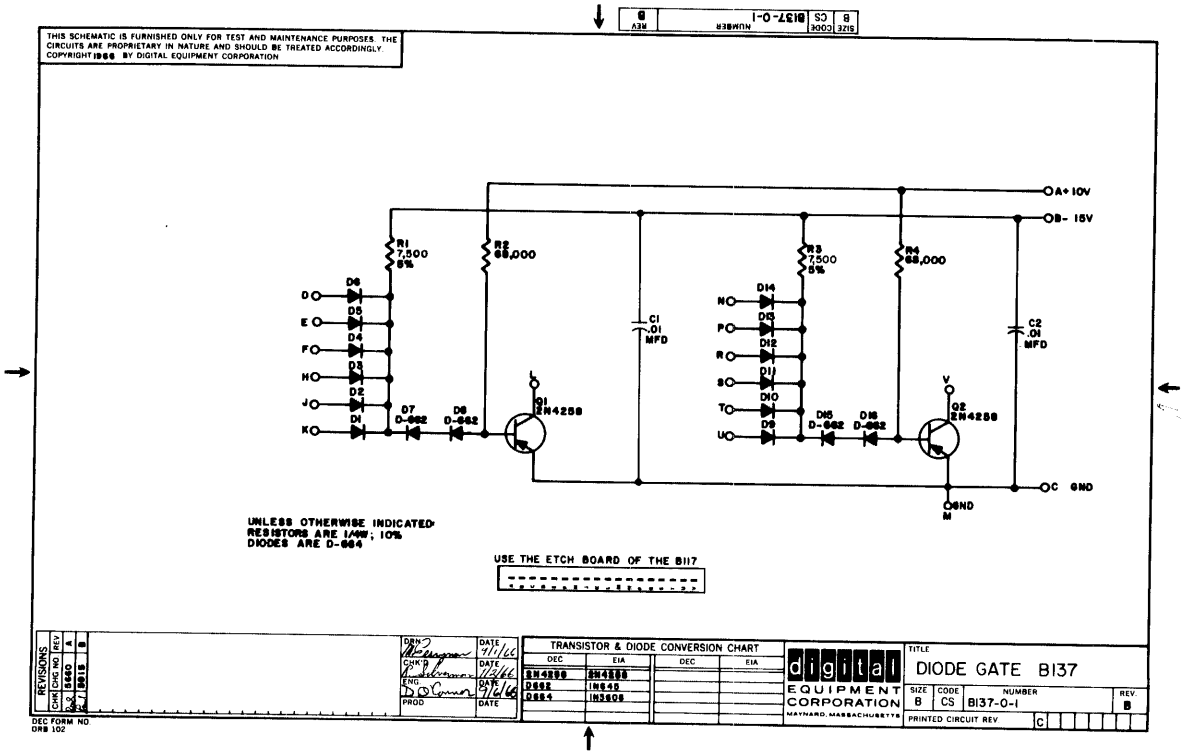


Figure 5-4 Diode Gate B137

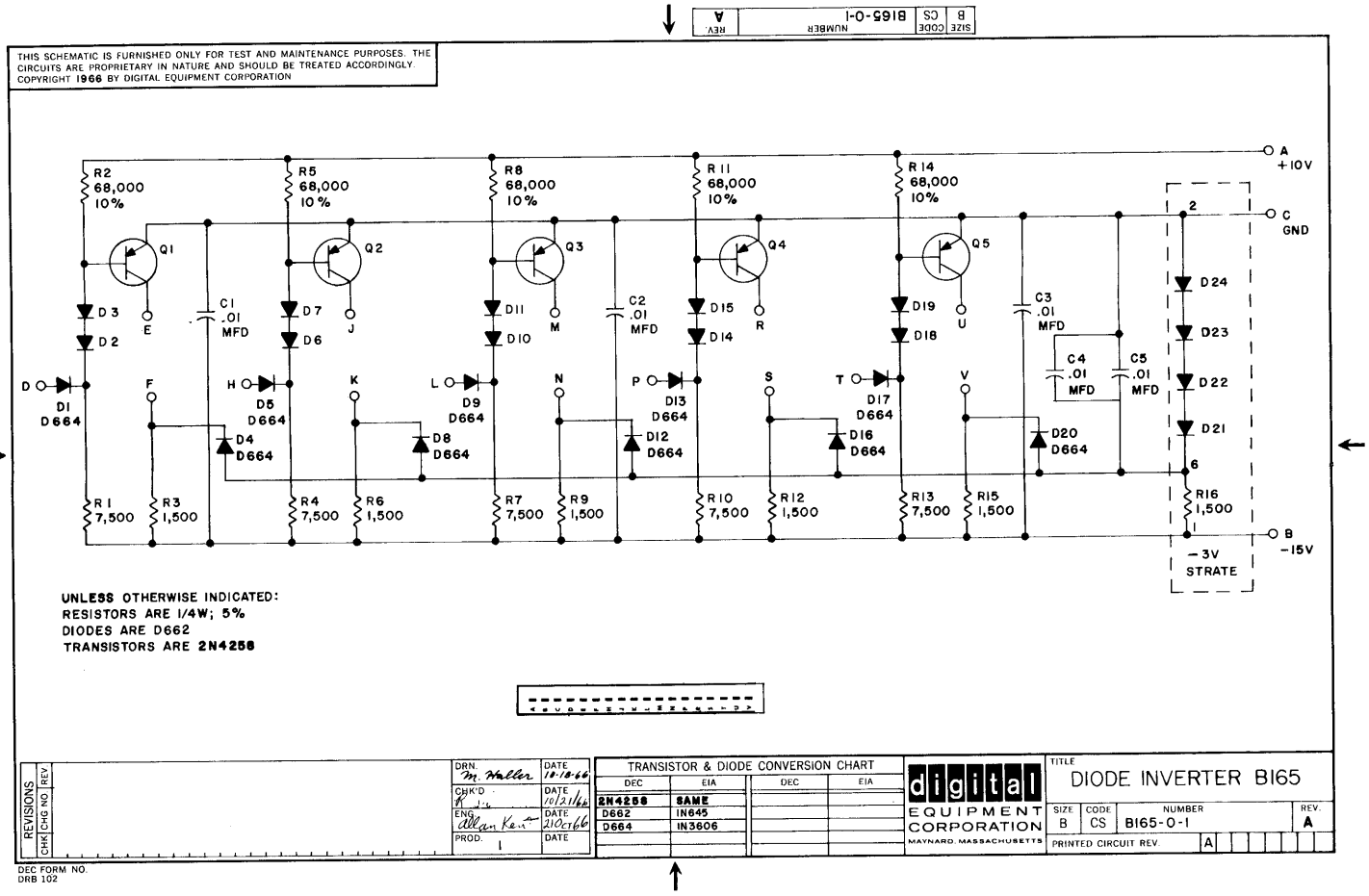


Figure 5-5 Diode Inverter B165

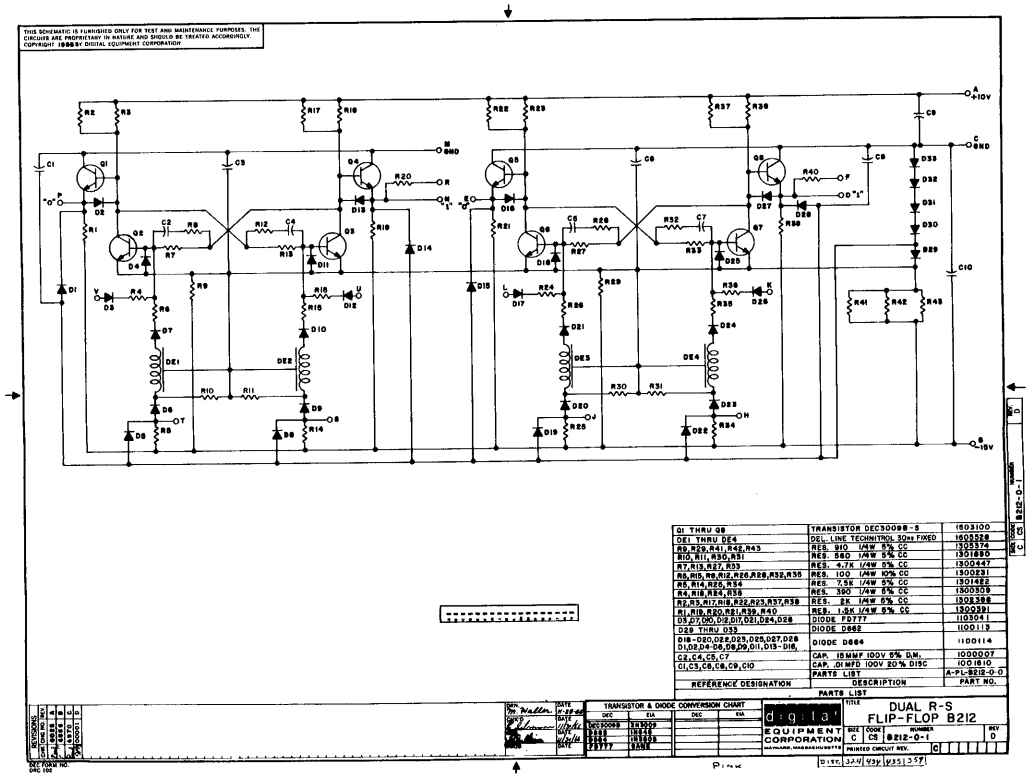


Figure 5-6 Dual R-S Flip-Flop B212

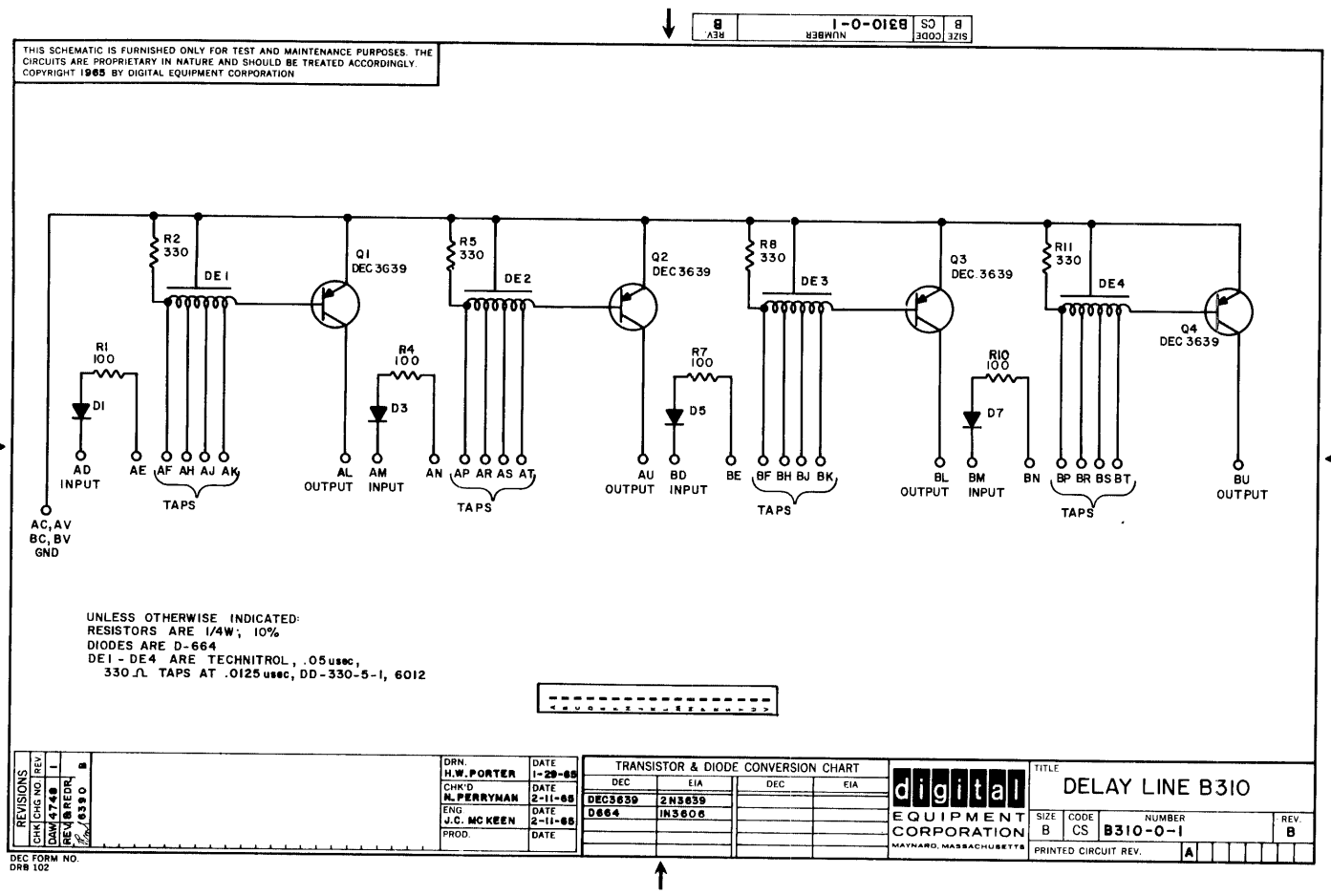


Figure 5-7 Delay Line B310

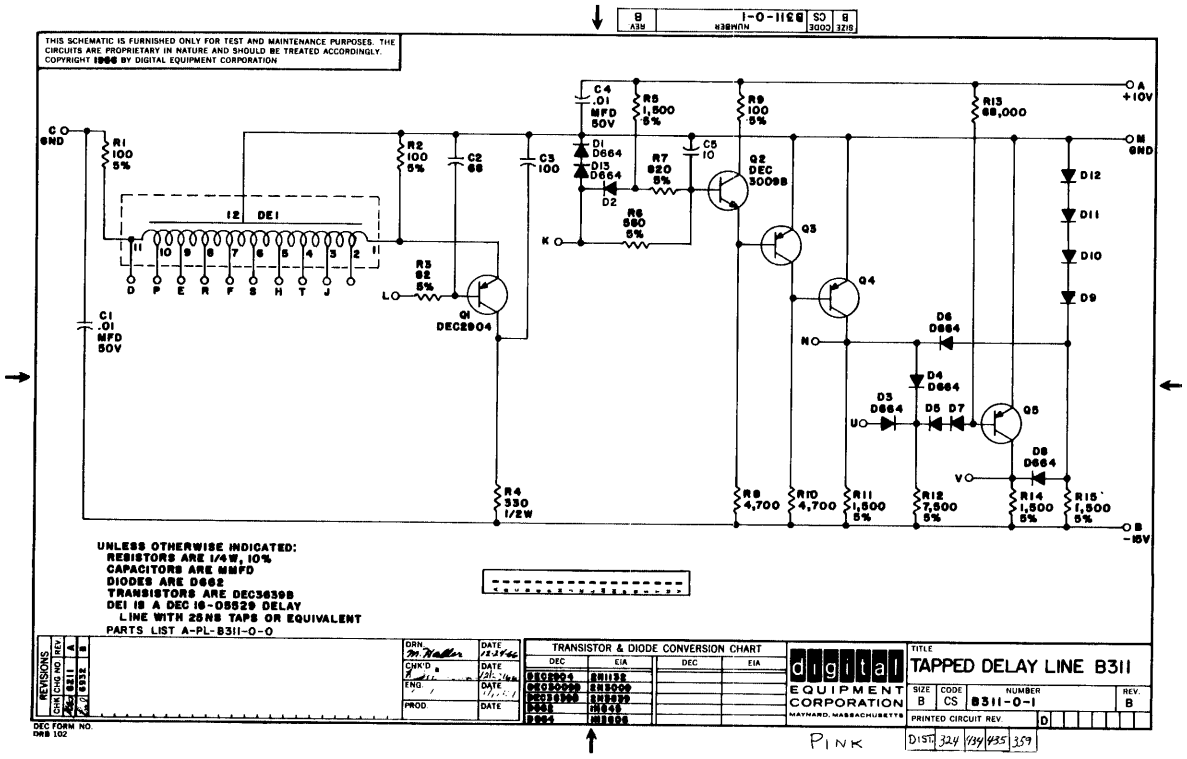


Figure 5-8 Tapped Delay Line B311

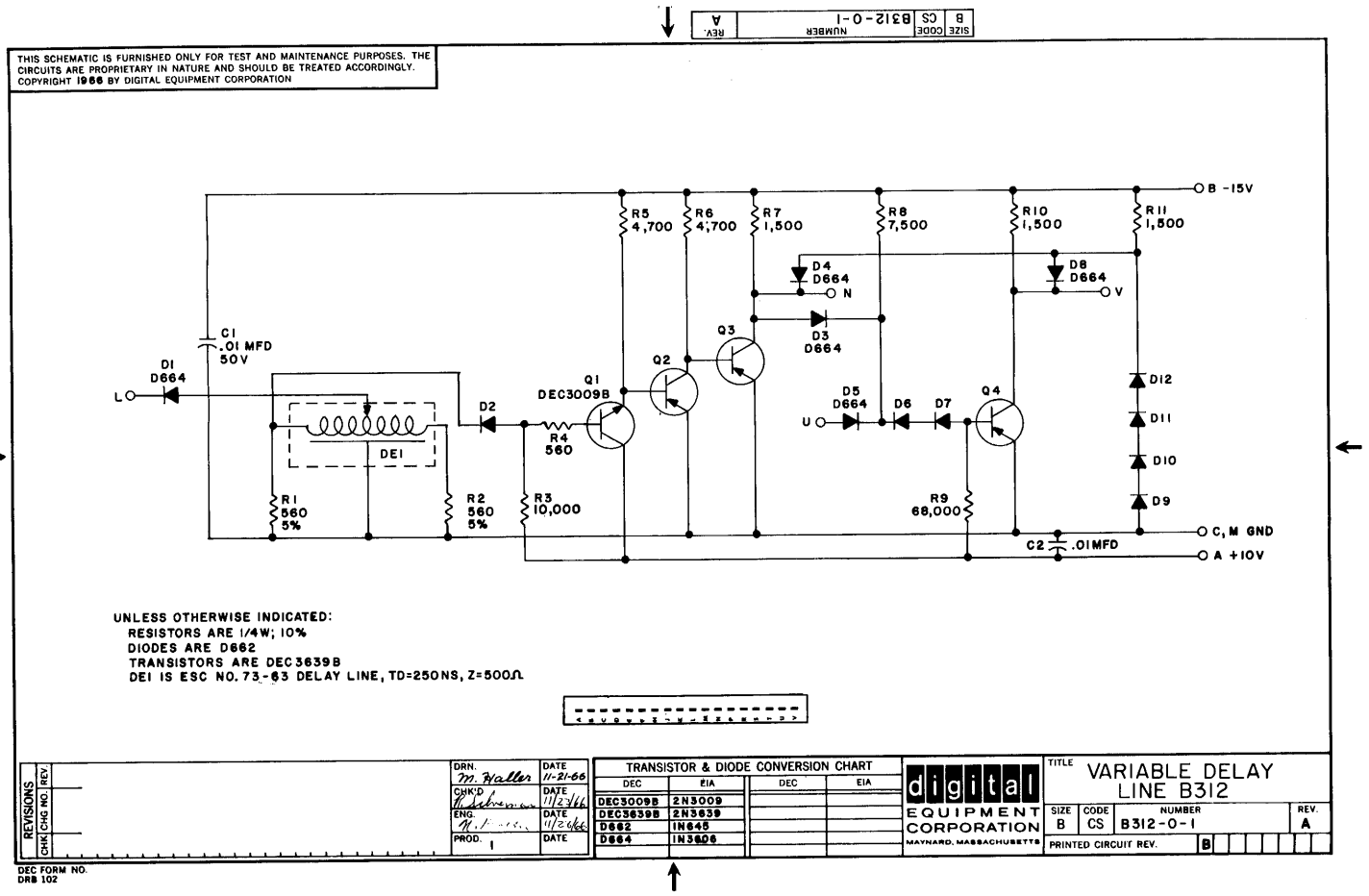


Figure 5-9 Variable Delay Line B312

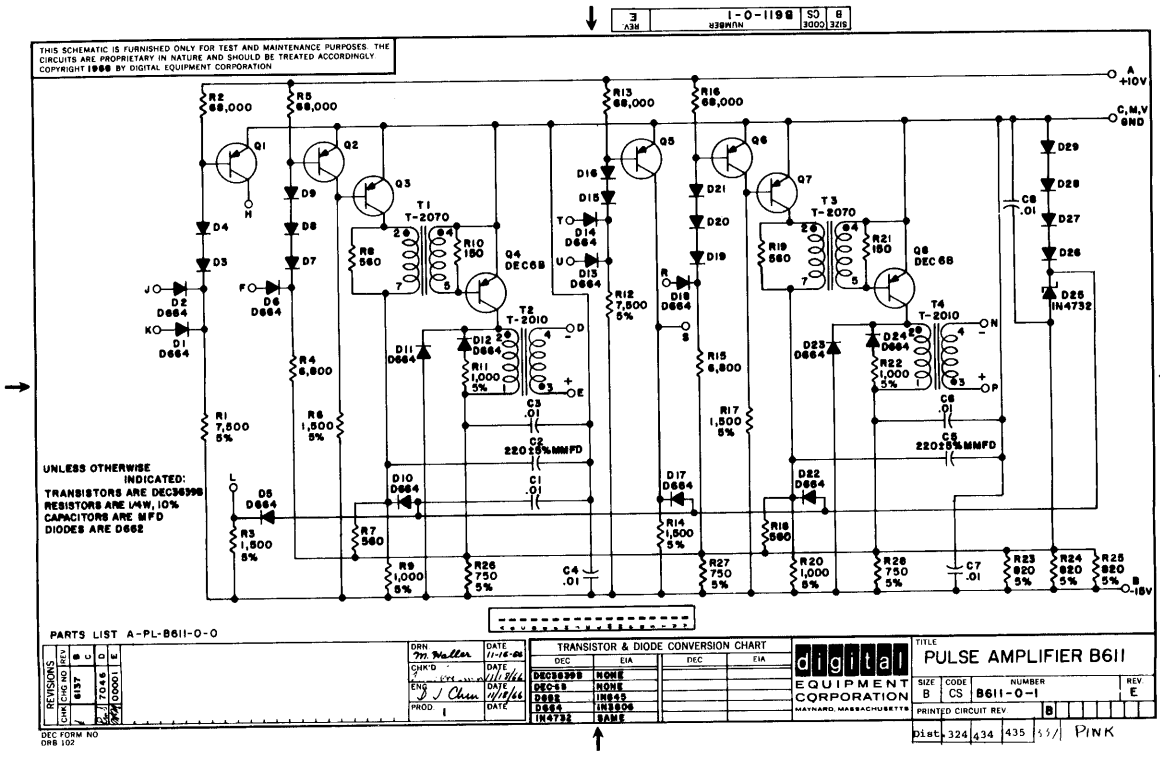


Figure 5-10 Pulse Amplifier B611

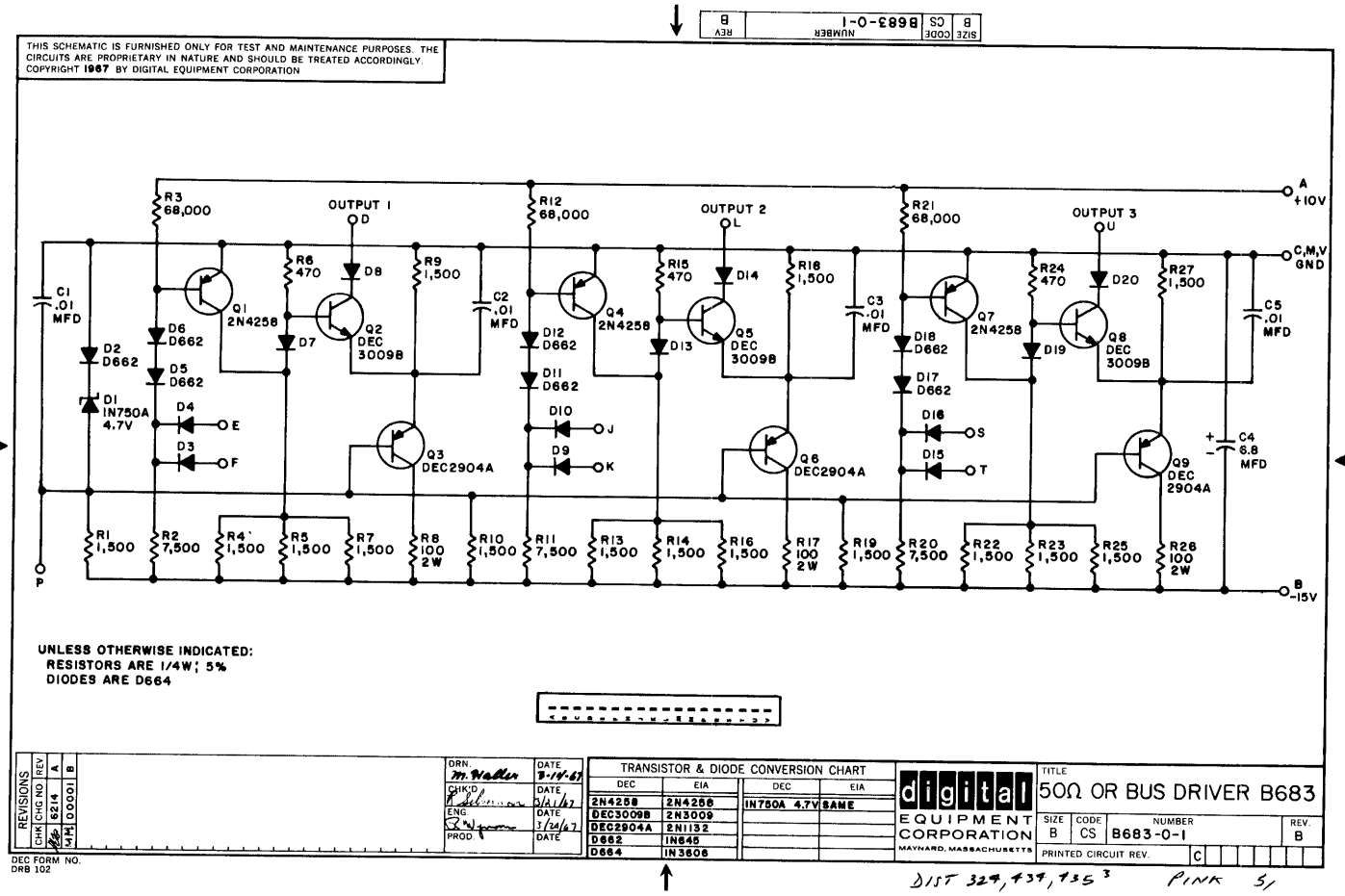


Figure 5-11 50Ω OR Bus Driver B683

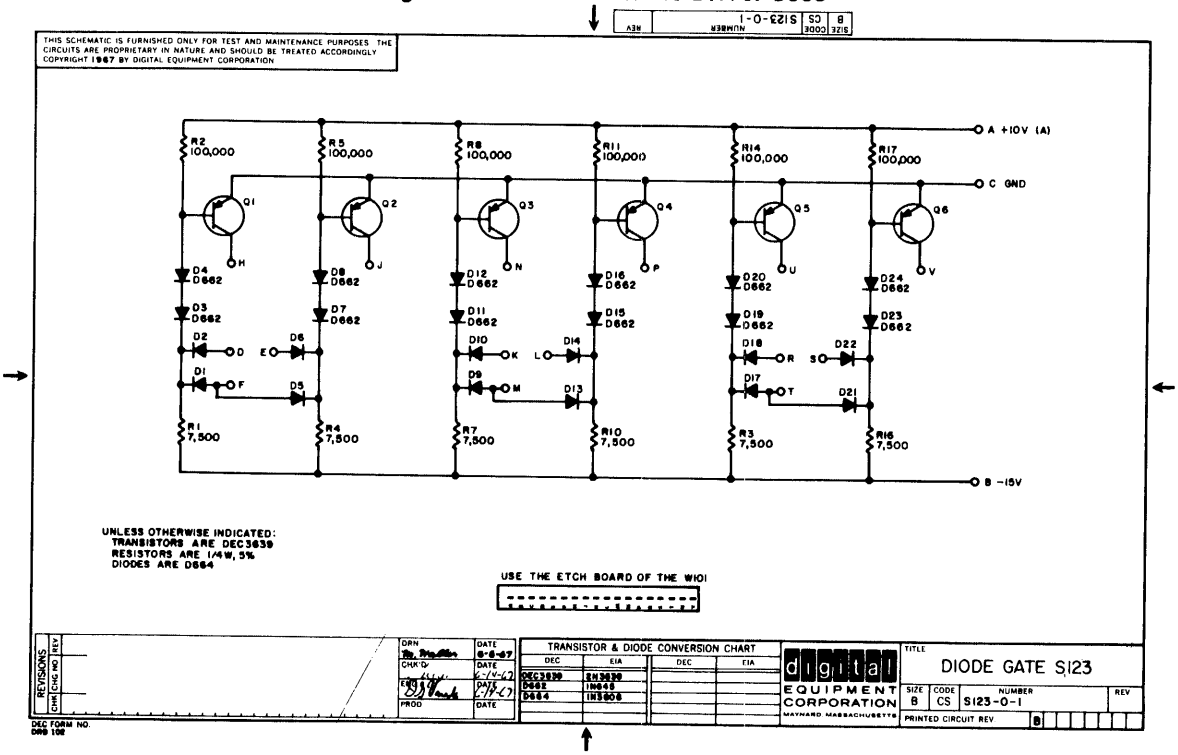


Figure 5-12 Diode Gate S123

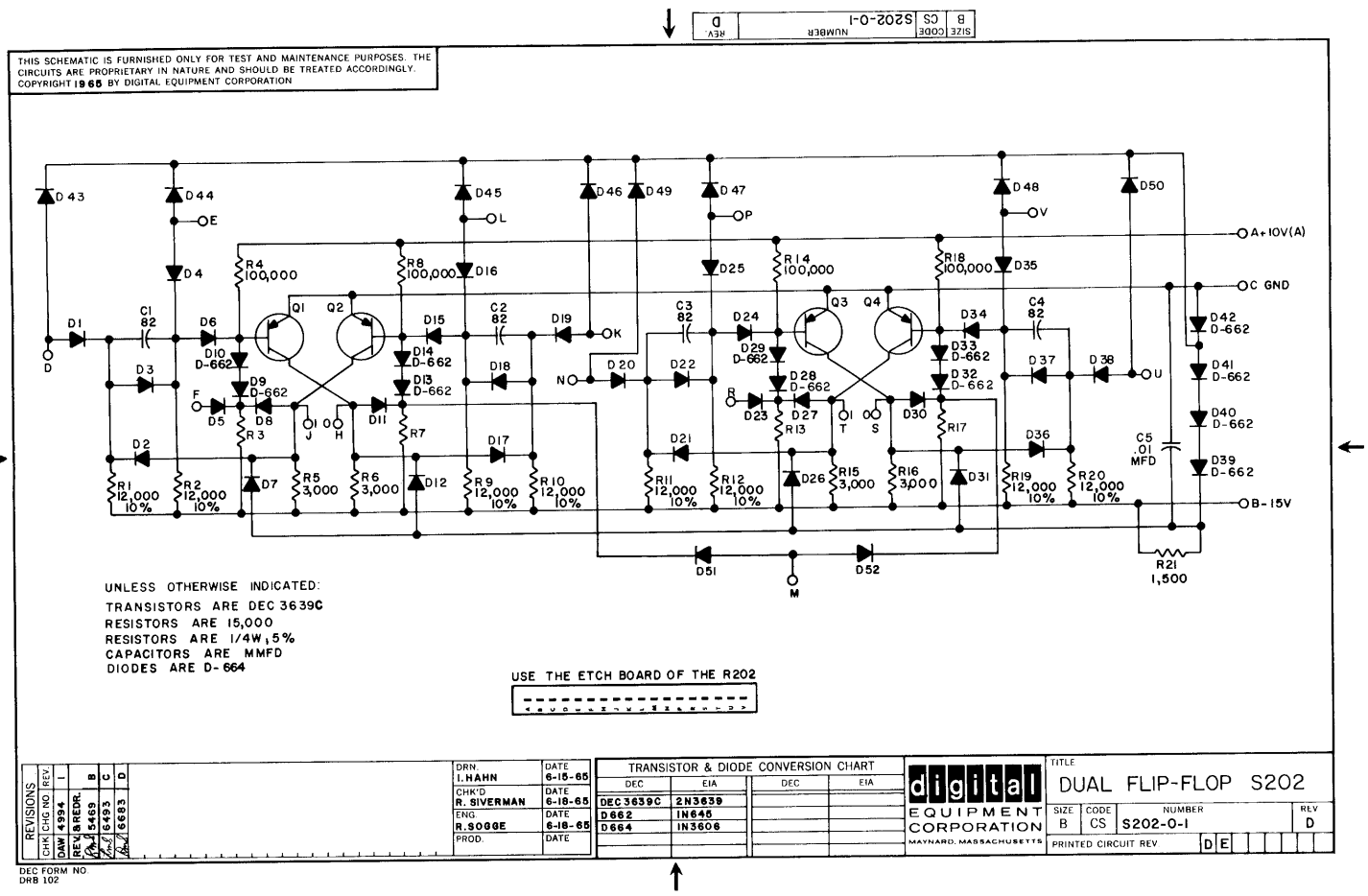


Figure 5-13 Dual Flip-Flop S202

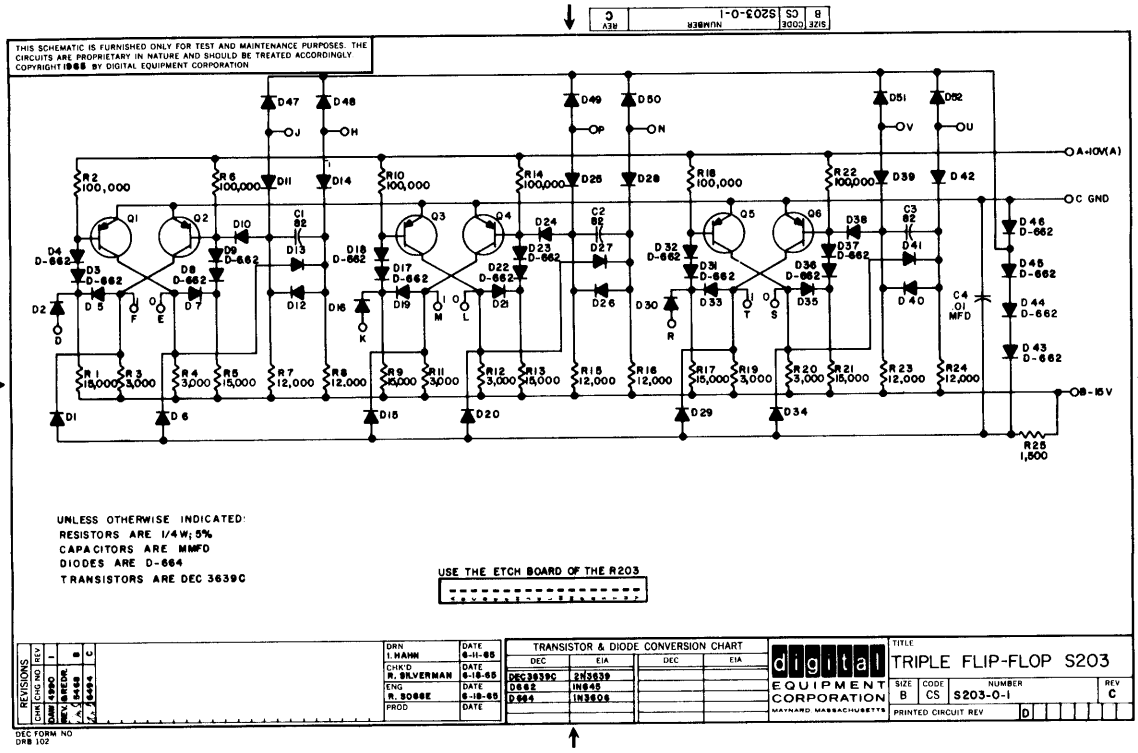


Figure 5-14 Triple Flip-Flop S203

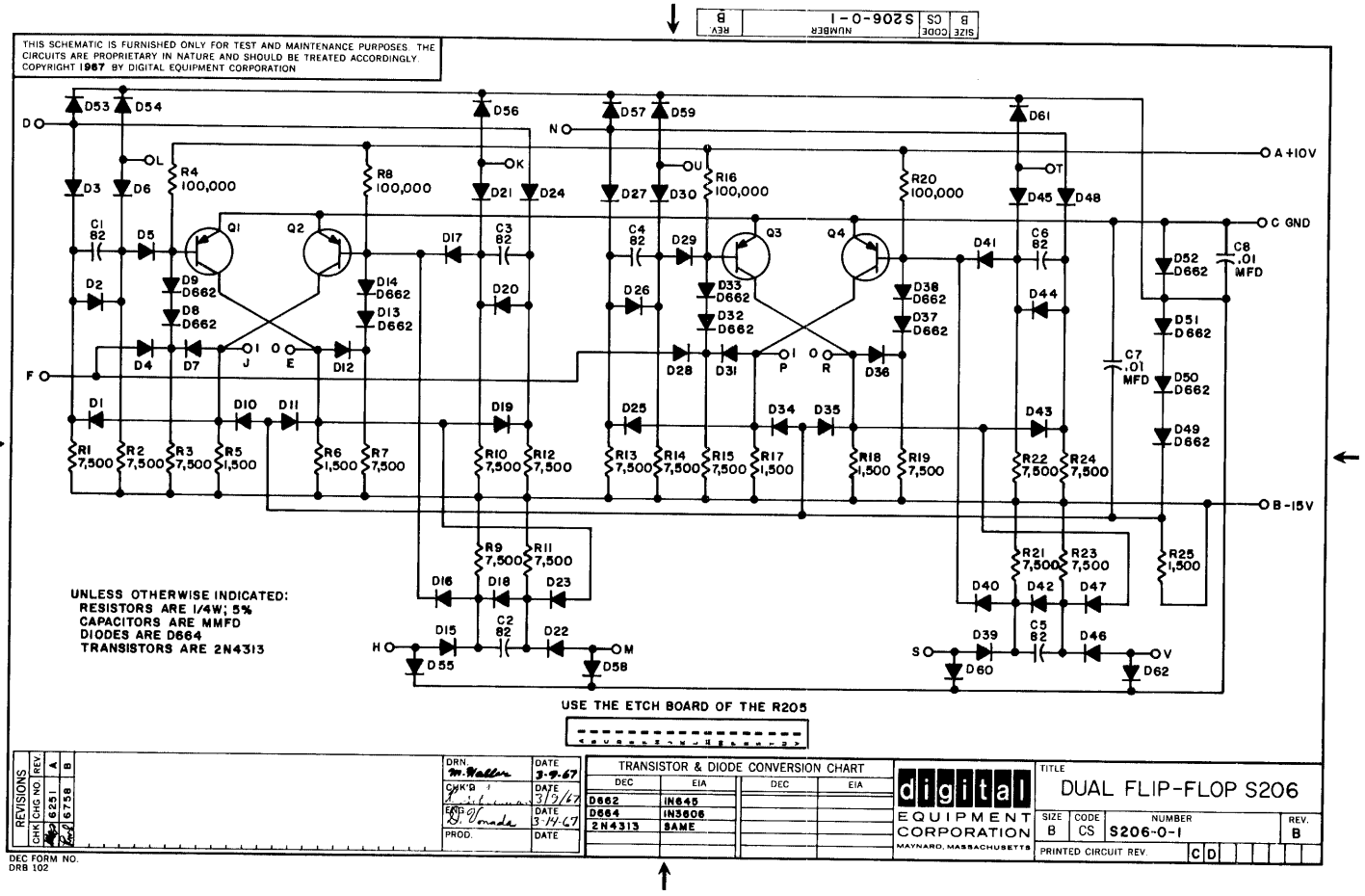


Figure 5-15 Dual Flip-Flop S206

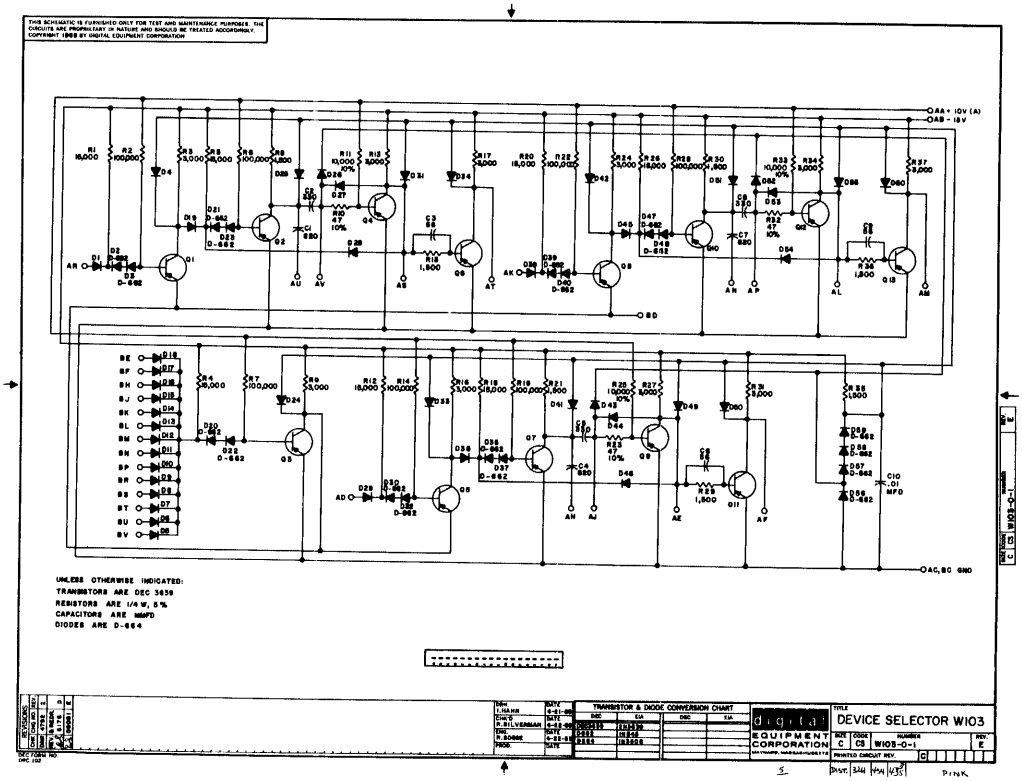


Figure 5-16 Device Selector W103

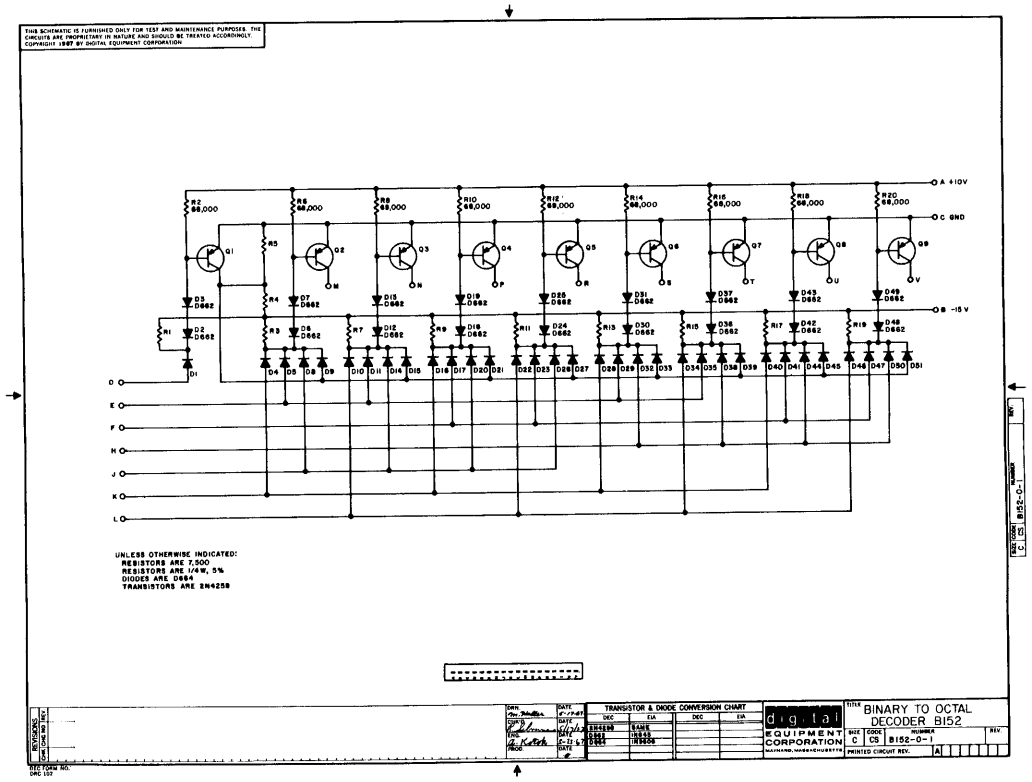


Figure 5-17 Binary To Octal Decoder B152

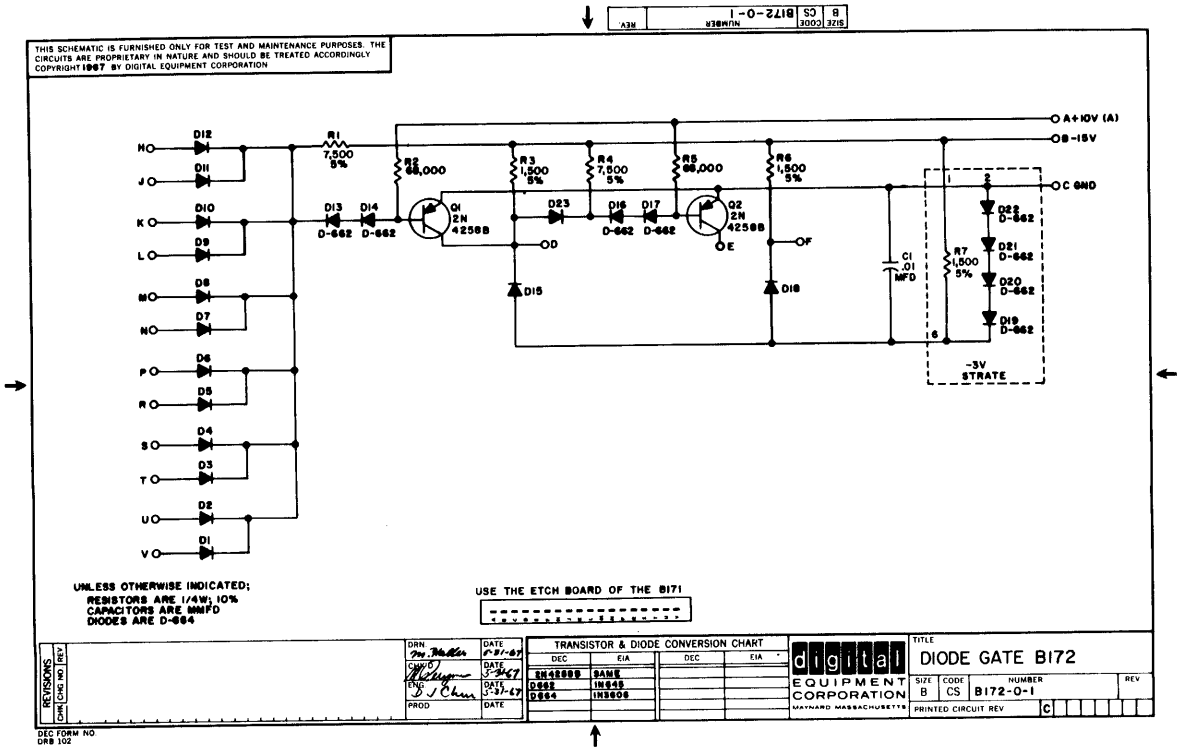


Figure 5-18 Diode Gate B172

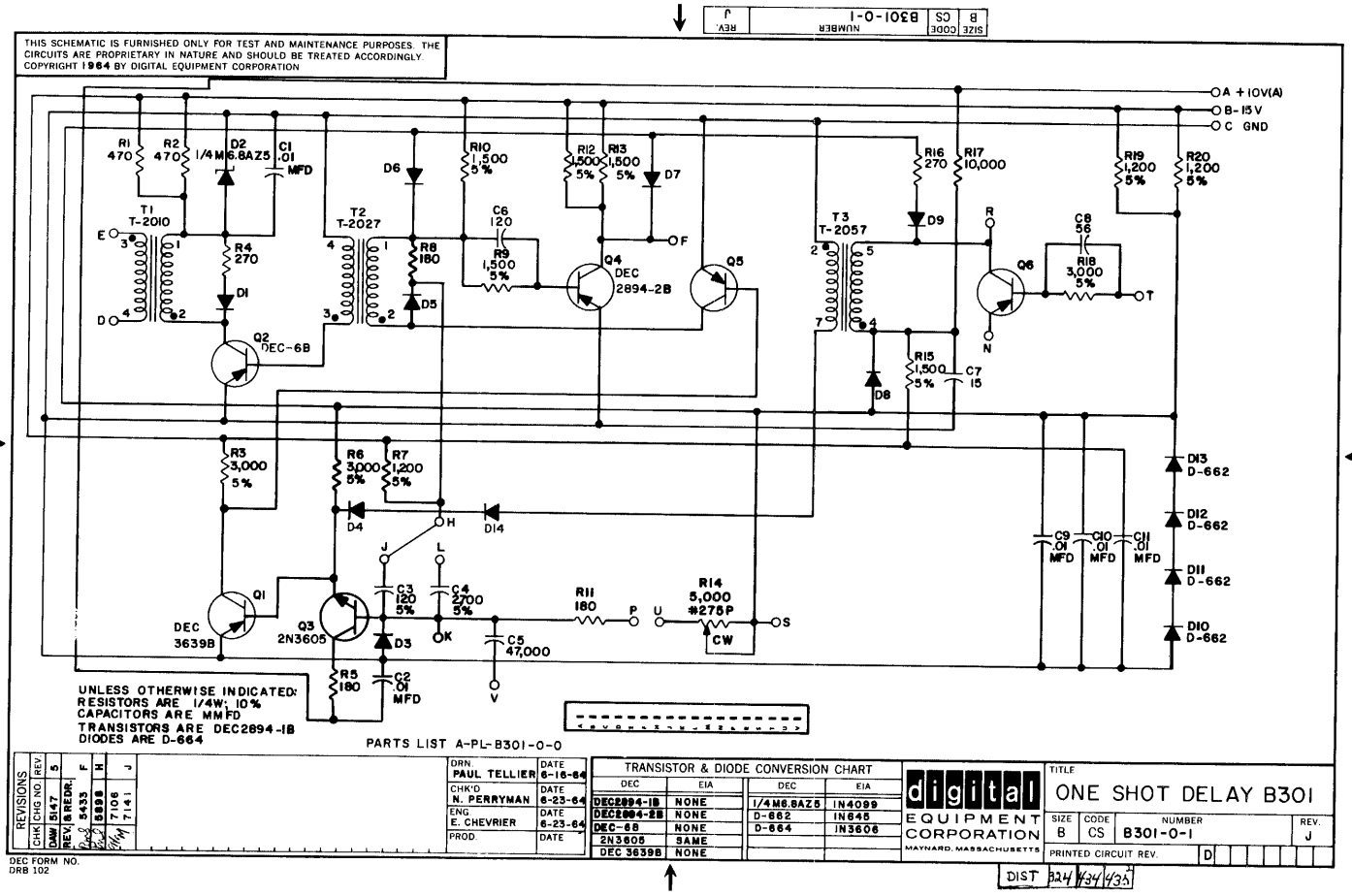


Figure 5-19 One Shot Delay B301

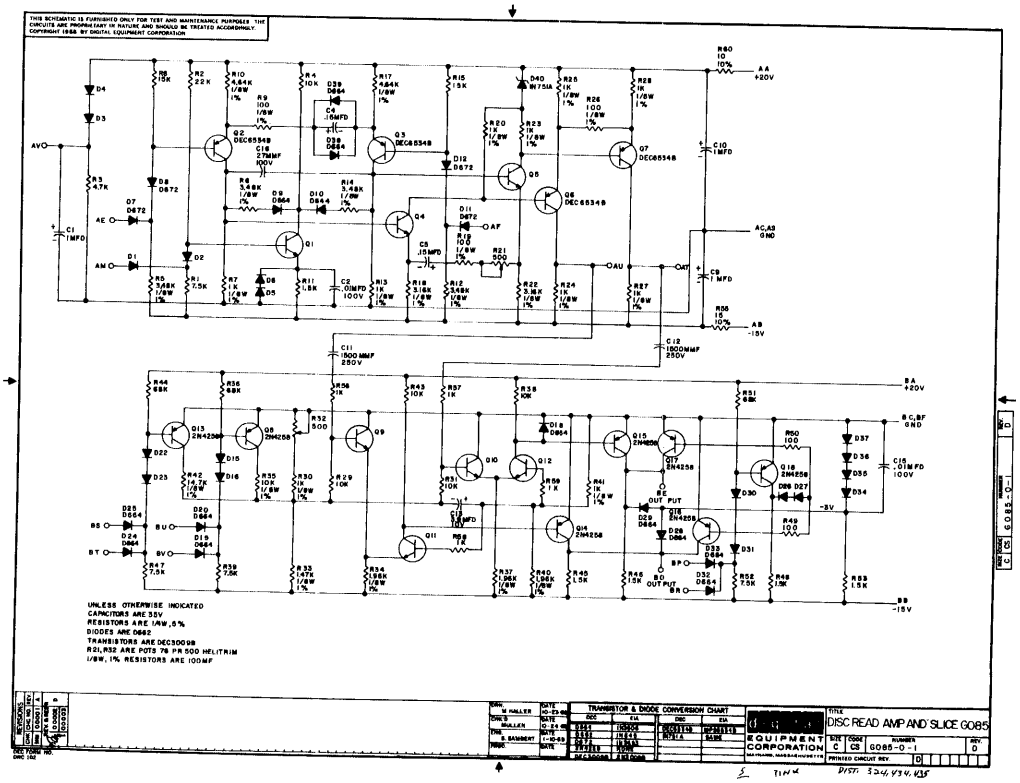


Figure 5-20 Disc Read Amp and Slice G085

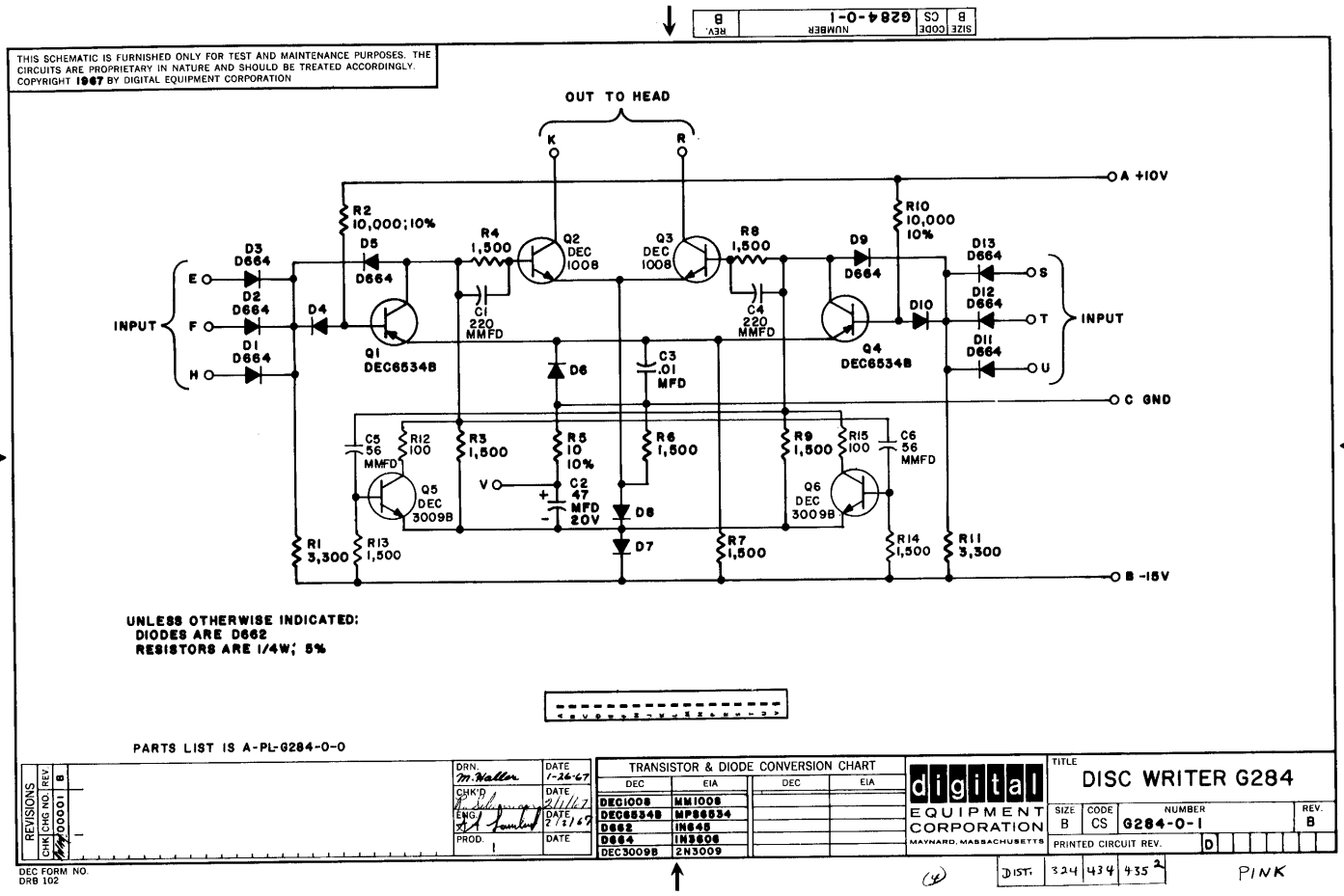


Figure 5-21 Disc Writer G284

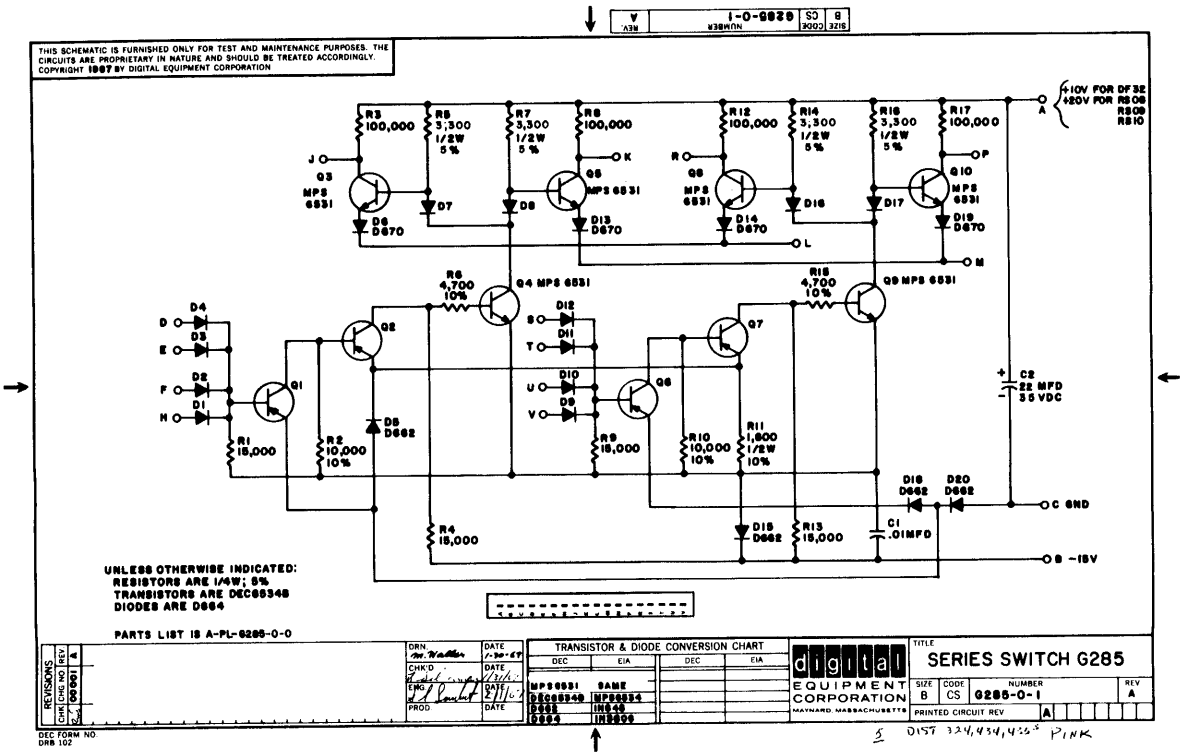


Figure 5-22 Series Switch G285

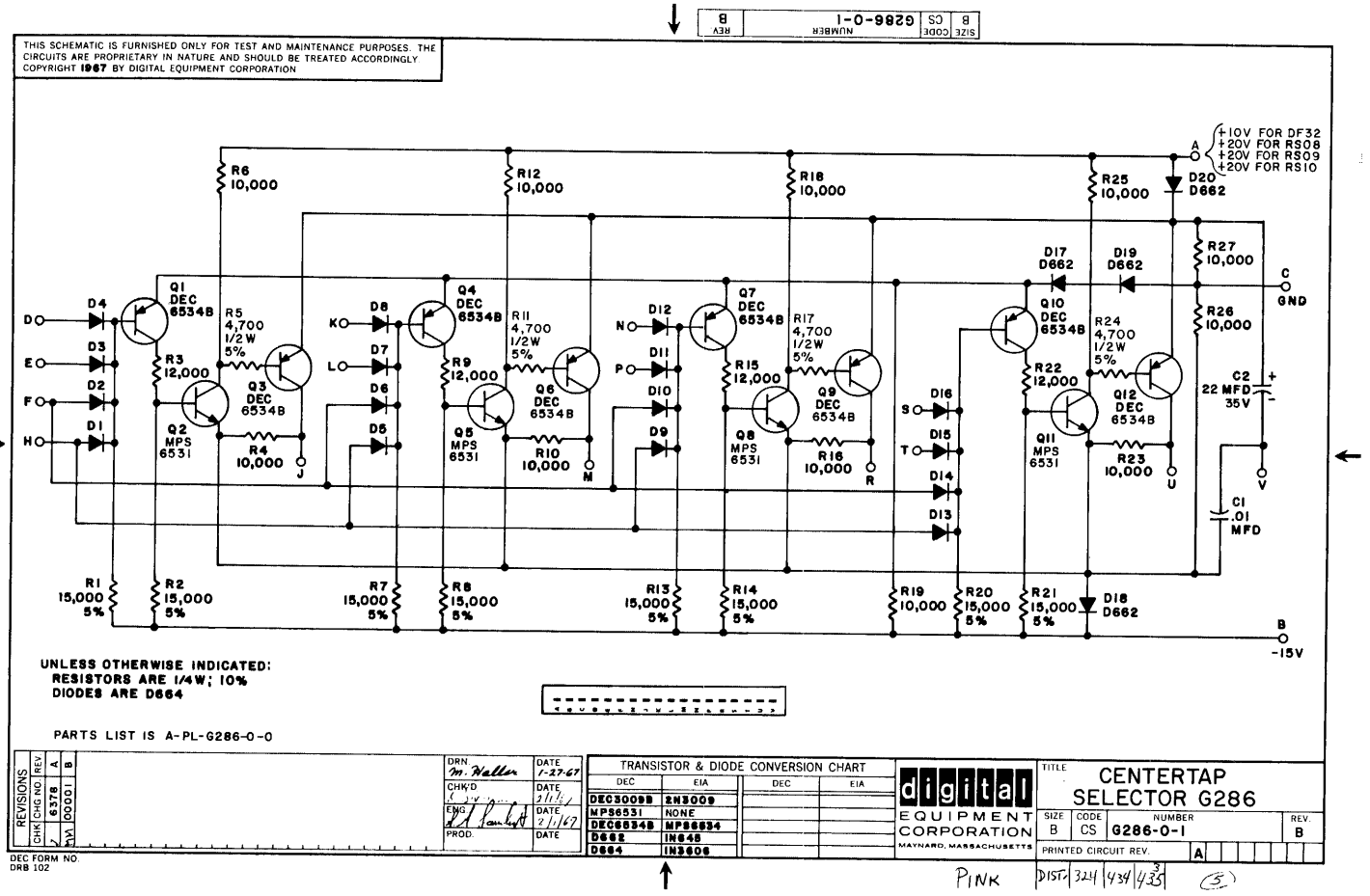


Figure 5-23 Centertap Selector G286

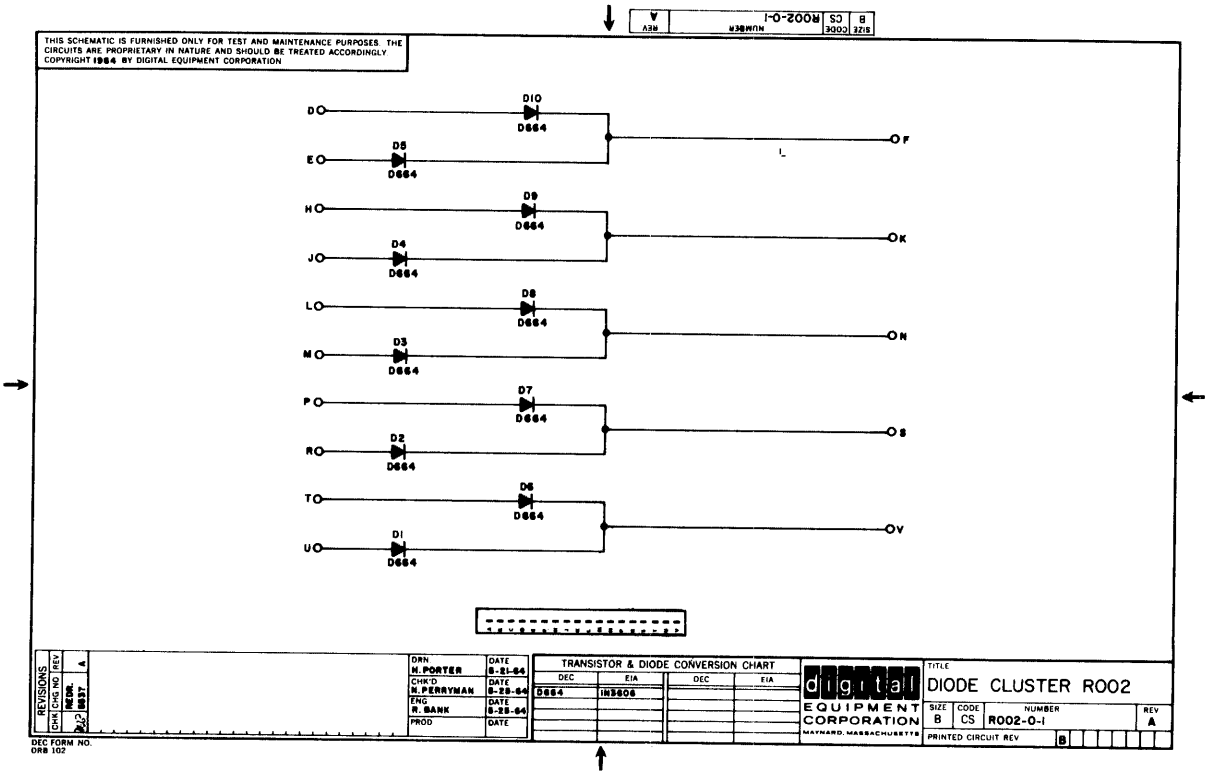


Figure 5-24 Diode Cluster R002

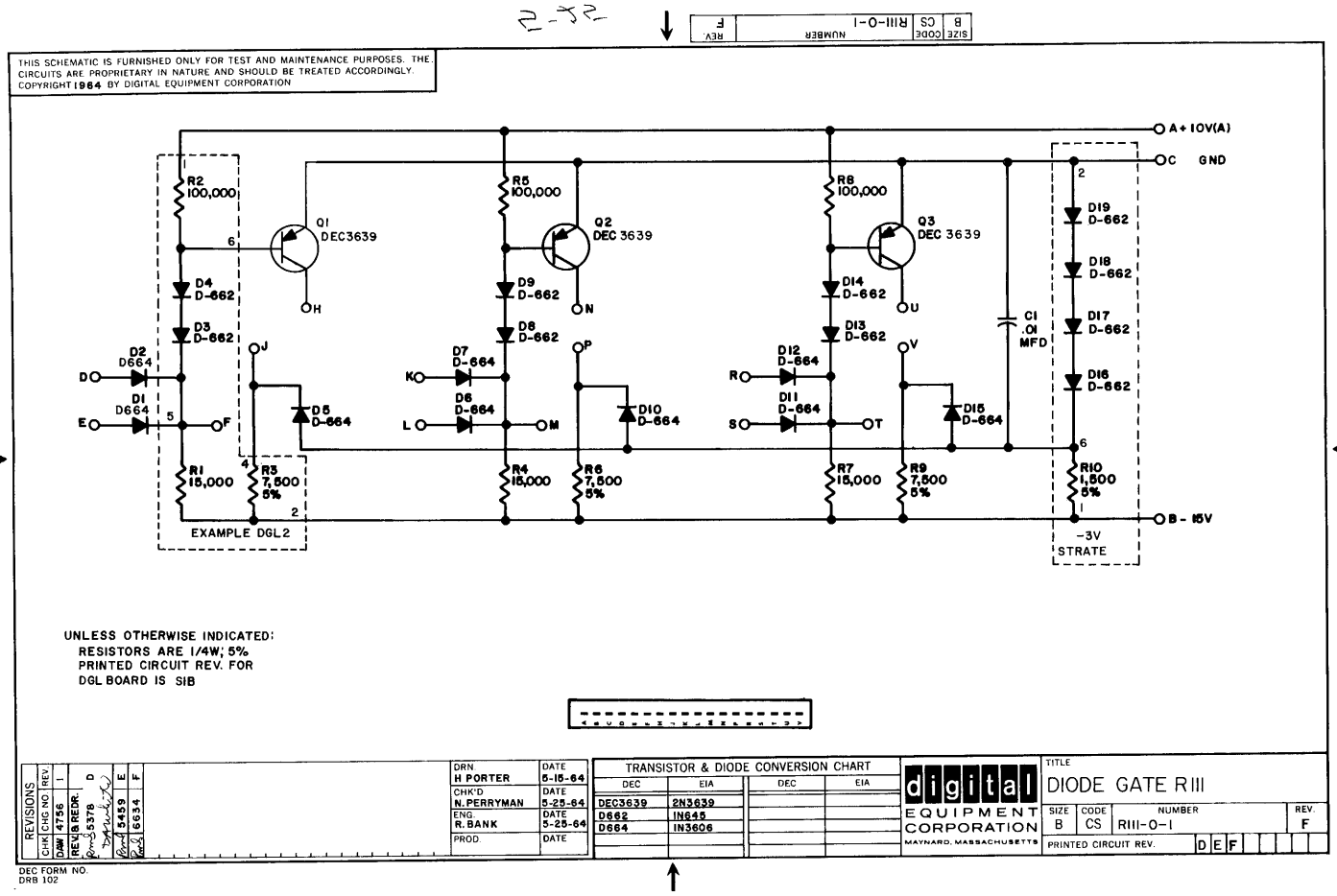


Figure 5-25 Diode Gate R111

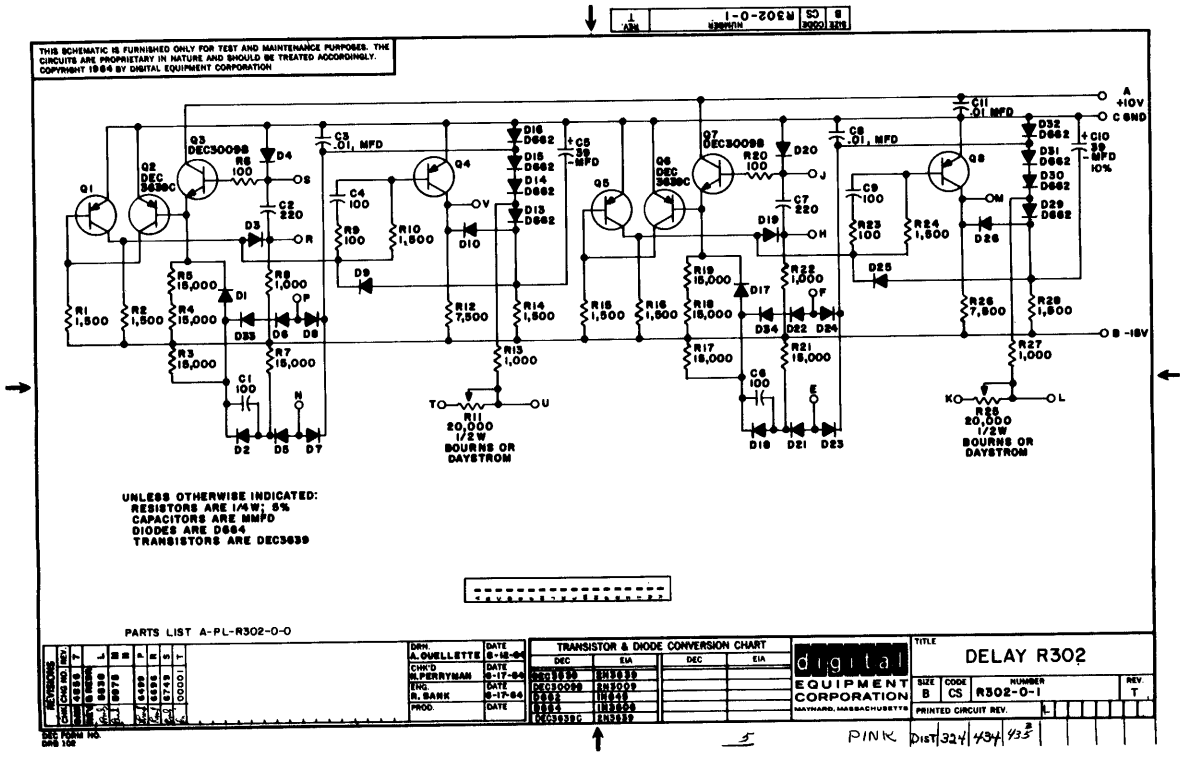


Figure 5-26 Delay R302

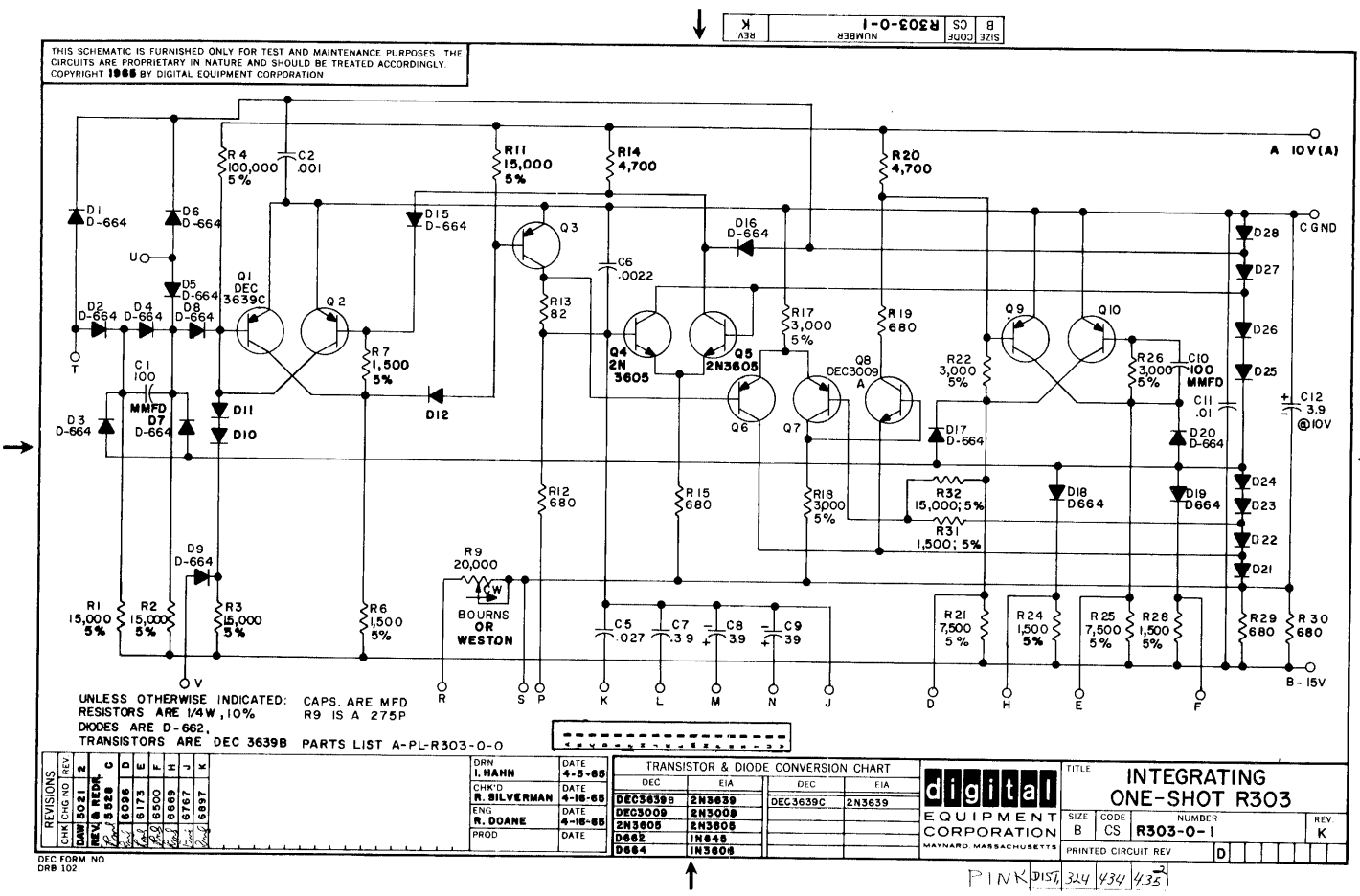
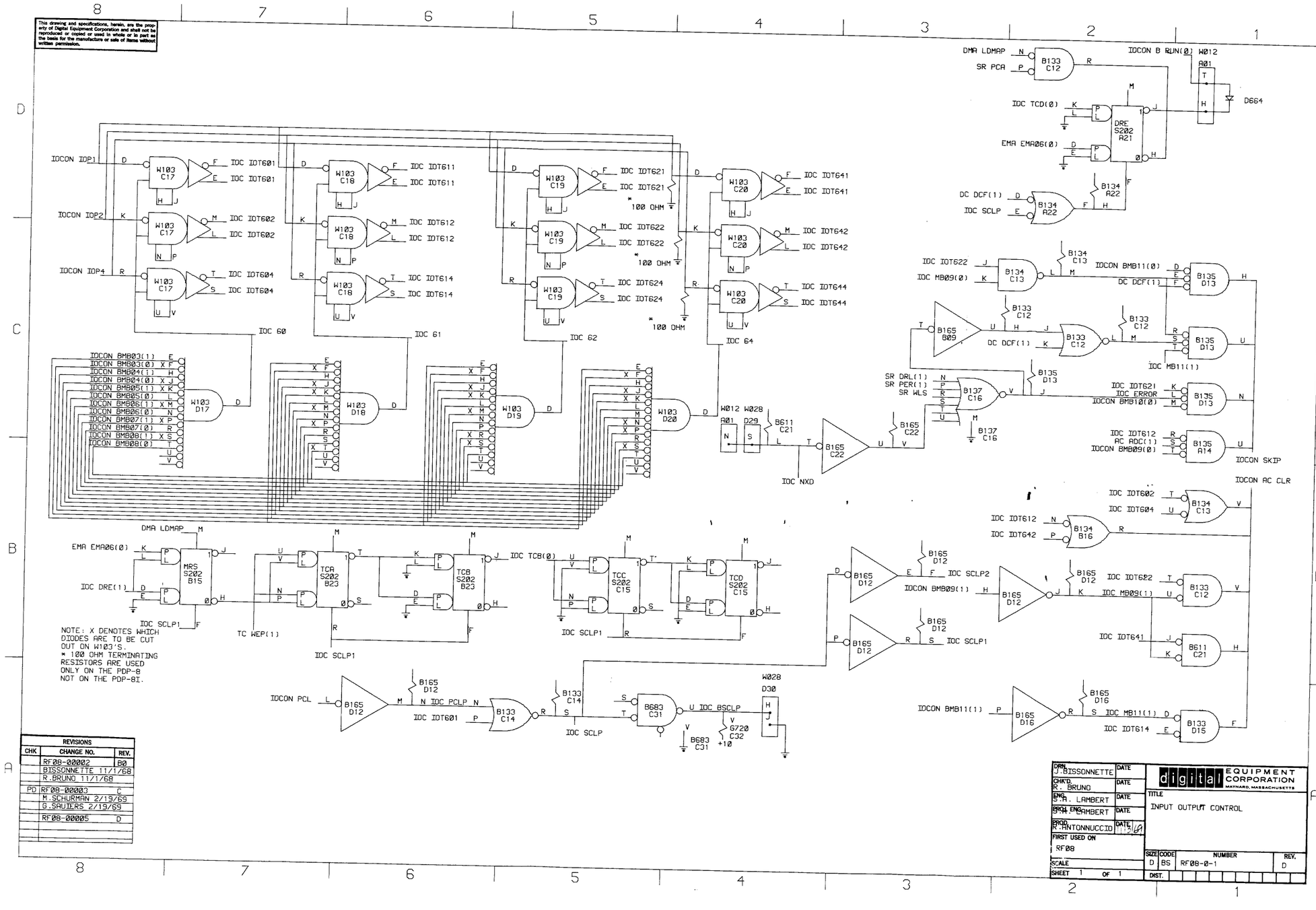


Figure 5-27 Integrating One-Shot R303

CHAPTER 6
LOGIC BLOCK SCHEMATICS

6.1 INTRODUCTION

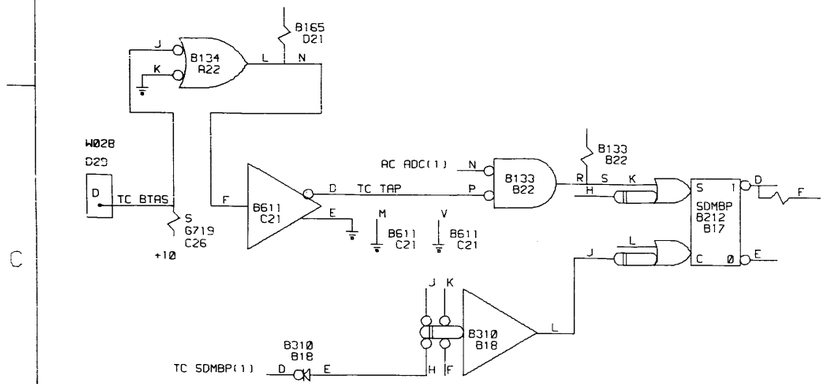
Figures 6-1 through 6-10 are the logic block schematics pertaining to the RF08 Disk Control and RS08 Disk.

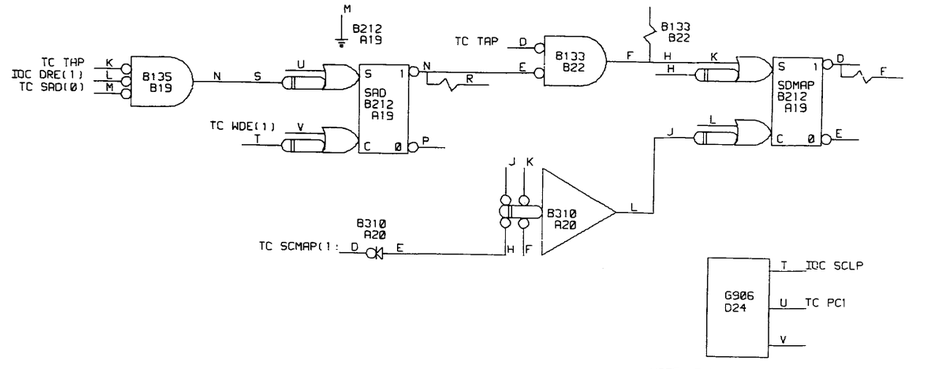


REVISIONS		
CHK	CHANGE NO.	REV.
	RF08-00002	B0
	BISSONNETTE 11/1/68	
	R.BRUNO 11/1/68	
PD	RF08-00003	C
	M.SCHURMAN 2/19/69	
	G.SAUERS 2/19/69	
	RF08-00005	D

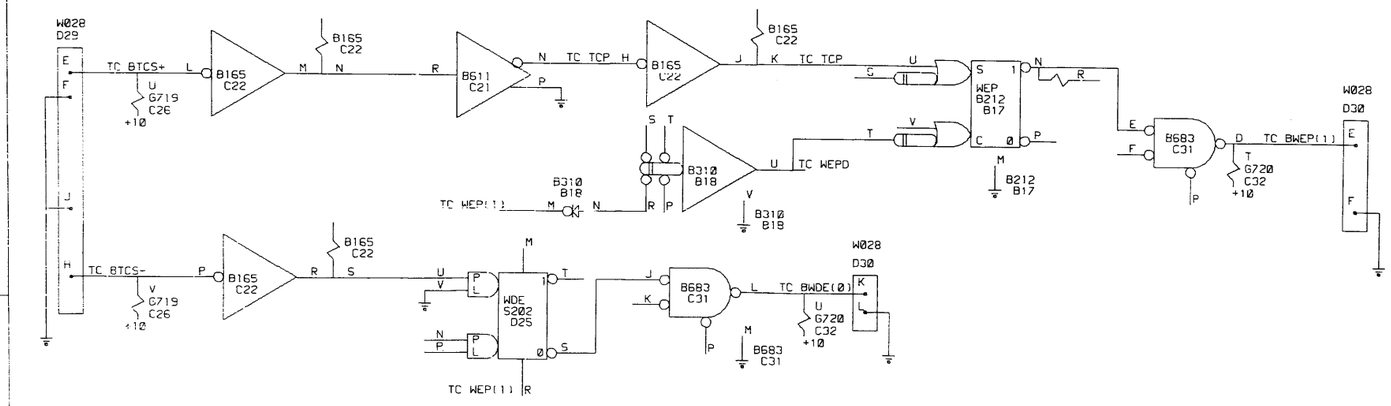
DRN. J.BISSONNETTE	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. R. BRUNO	DATE	
ENG. S.H. LAMBERT	DATE	TITLE: INPUT OUTPUT CONTROL
ENGR ENG. S.H. LAMBERT	DATE	
PROD. R.ANTONNUCCIO	DATE 11/5/69	
FIRST USED ON: RF08		SIZE D · CODE BS · NUMBER RF08-0-1 · REV. D
SCALE		SHEET 1 OF 1 · DIST.

Figure 6-1 Input Output Control





NOTE: THIS MODULE GENERATES LOCAL POWER CLEAR WHEN -15 IS MORE POSITIVE THAN -8VOLTS.



REVISIONS			REVISIONS		
CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.
	RF0B-00002	B0	G.N	RF0B-00006	E
	BISSONNETTE 11/1/68				
	R.BRUNO 11/1/68				
	RF0B-00003	C			
	M.SCHURMAN 2/19/69				
	G.SAVIERS 2/19/69				
	RF0B-00005	D			
	M.SCHURMAN 4/15/69				
	G.SAVIERS 4/17/69				

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRN.	J.BISSONNETTE	DATE
CHK'D.	R. BRUNO	DATE
ENG.	S.A. LAMBERT	DATE
PROJ. ENG.	S.A. LAMBERT	DATE
PROD.	R.ANTONNUCCIO	DATE

FIRST USED ON: RF08
SCALE:
SHEET 1 OF 1

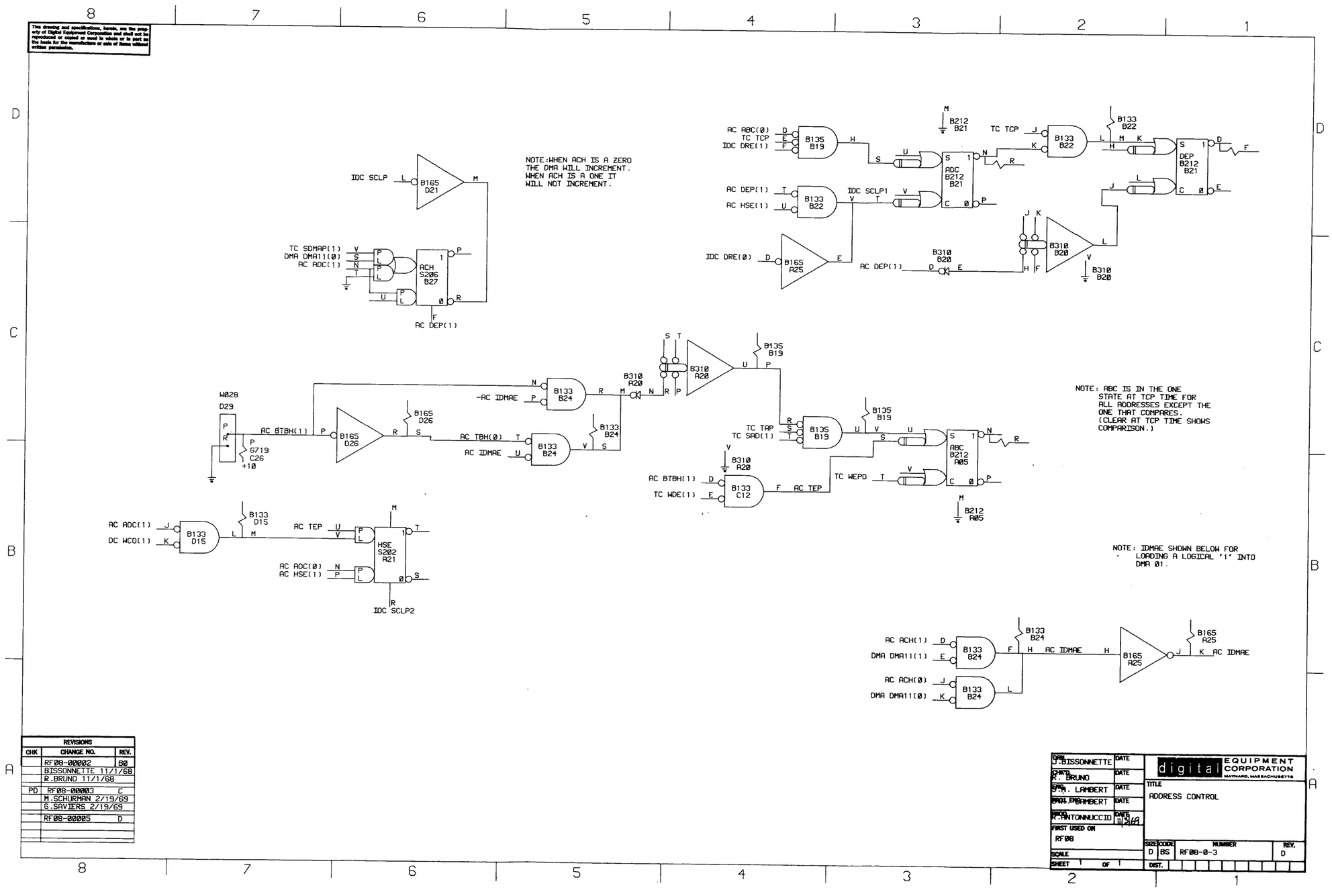
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: TIMING CONTROL

SIZE	CODE	NUMBER	REV.
D	BS	RF0B-0-2	E

DIST.

Figure 6-2 Timing Control



REVISIONS		
CHK	CHANGE NO.	REV.
	RF08-00002	B0
	BISSONNETTE 11/1/68	
	R.BRUNO 11/1/68	
PD	RF08-00003	C
	M.SCHURMAN 2/19/69	
	G.SAVIERS 2/19/69	
	RF08-00005	D

DRWN J.BISSONNETTE	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHKD R. BRUNO	DATE	
ENGR G.A. LAMBERT	DATE	TITLE: ADDRESS CONTROL
APPD G.LAMBERT	DATE	
PROJ R.ANTONNUCCIO	DATE 11/5/68	
FIRST USED ON: RF08		SIZE D | CODE BS | NUMBER RF08-0-3 | REV. D
SCALE		
SHEET 1 OF 1		DIST.

Figure 6-3 Address Control

NOTE: WHEN WCO IS A ONE, A WORD COUNT OVERFLOW PULSE HAS NOT YET OCCURED. WHEN WCO IS A ZERO IT HAS OCCURED.

REVISIONS			REVISIONS		
CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.
	RF08-00002	B0		RF08-00006	E
	BISSONNETTE 11/1/68				
	R.BRUNO 11/1/68				
PD	RF08-00003	C			
	M.SCHURMAN 3/19/69				
	G.SAVIERS 3/19/69				
	RF08-00005	C			
	M SCHURMAN 4/15/69				
	G SAVIERS 4/17/69				

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

DRN. J.BISSONNETTE DATE
CHK'D. R. BRUNO DATE
ENG. S.H. LAMBERT DATE
SRTL ENG. S.H. LAMBERT DATE
PROD. R.ANTONNUCCIO DATE
FIRST USED ON RF08
SCALE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DATA CONTROL

SIZE	CODE	NUMBER	REV.
D	BS	RF08-0-4	E

DIST.

Figure 6-4 Data Control

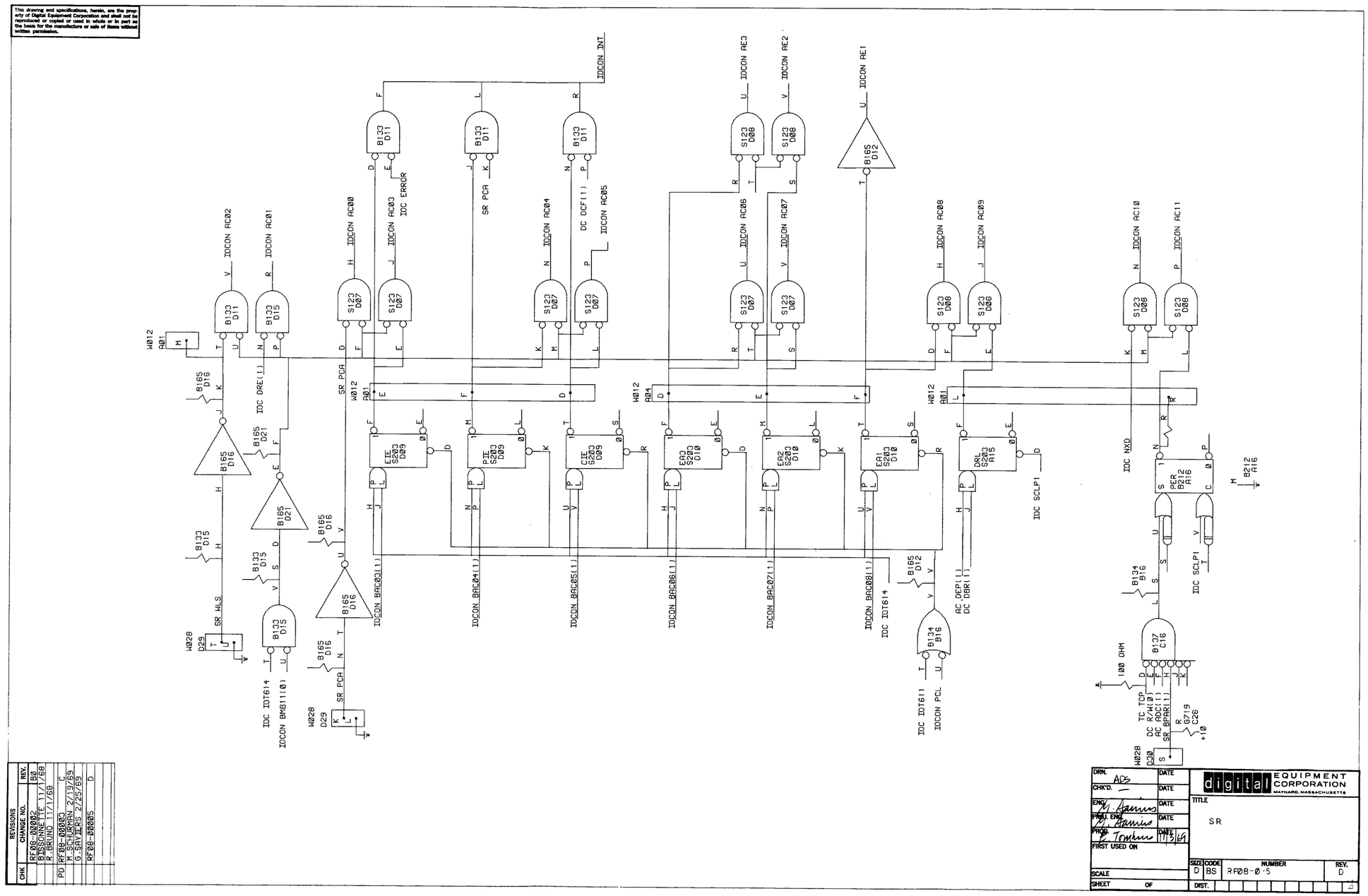
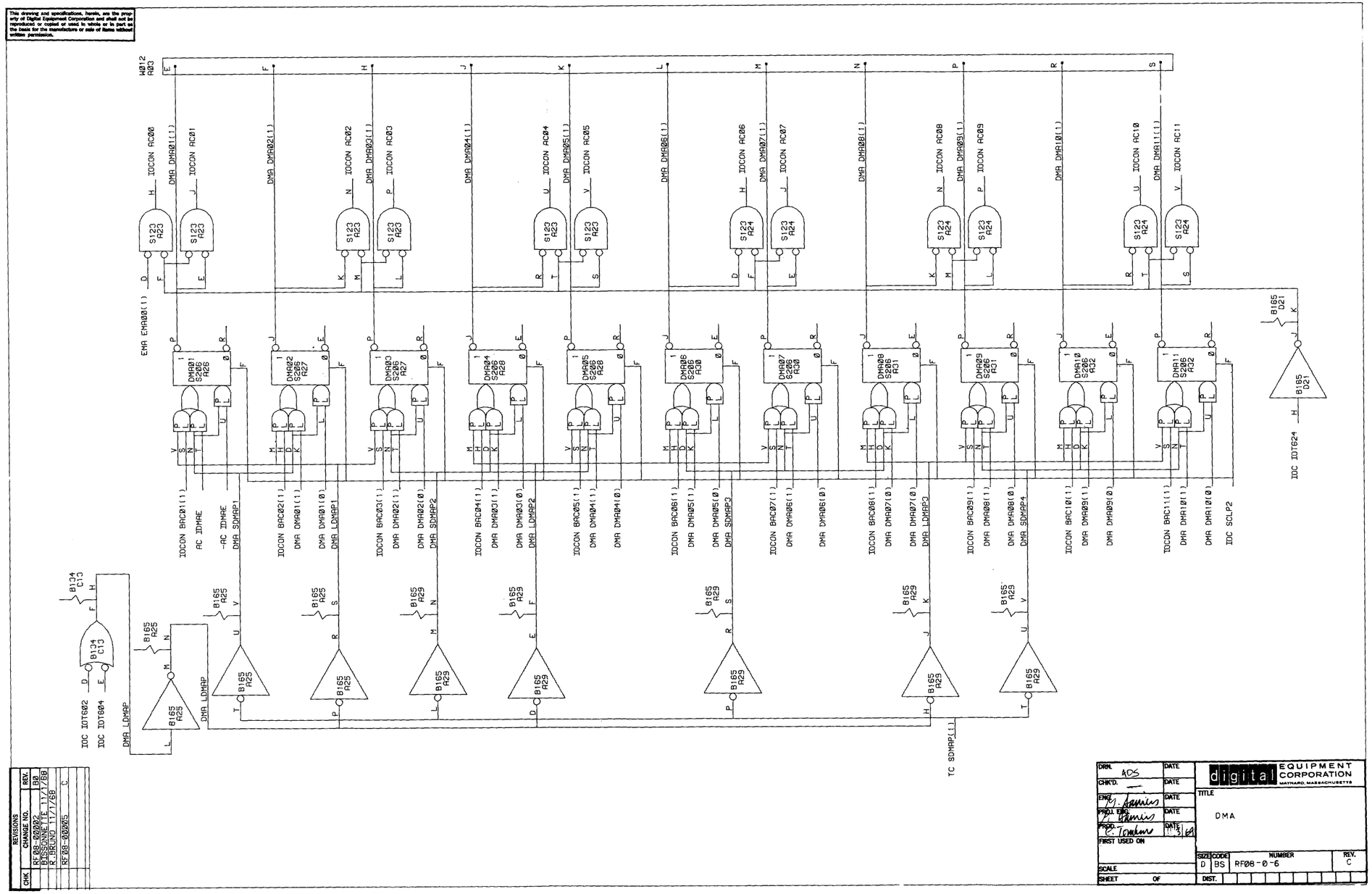


Figure 6-5 Status Register



REVISIONS			
CHK.	CHANGE NO.	REV.	
	RF08-00002	B0	
	BISSONNETTE 11/1/88		
	R. BRUNO 11/1/88	C	
	RF08-00005		

DRN. ACS	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. —	DATE	
ENG. M. Jamins	DATE	TITLE: DMA
PROJ. ENG. M. Jamins	DATE	
PROD. E. Tomkins	DATE 11/5/88	
FIRST USED ON		SIZE D | CODE BS | NUMBER RF08-0-6 | REV. C
SCALE		
SHEET OF		DIST.

Figure 6-6 Disc Memory Address

Figure 6-7 Extended Memory Address

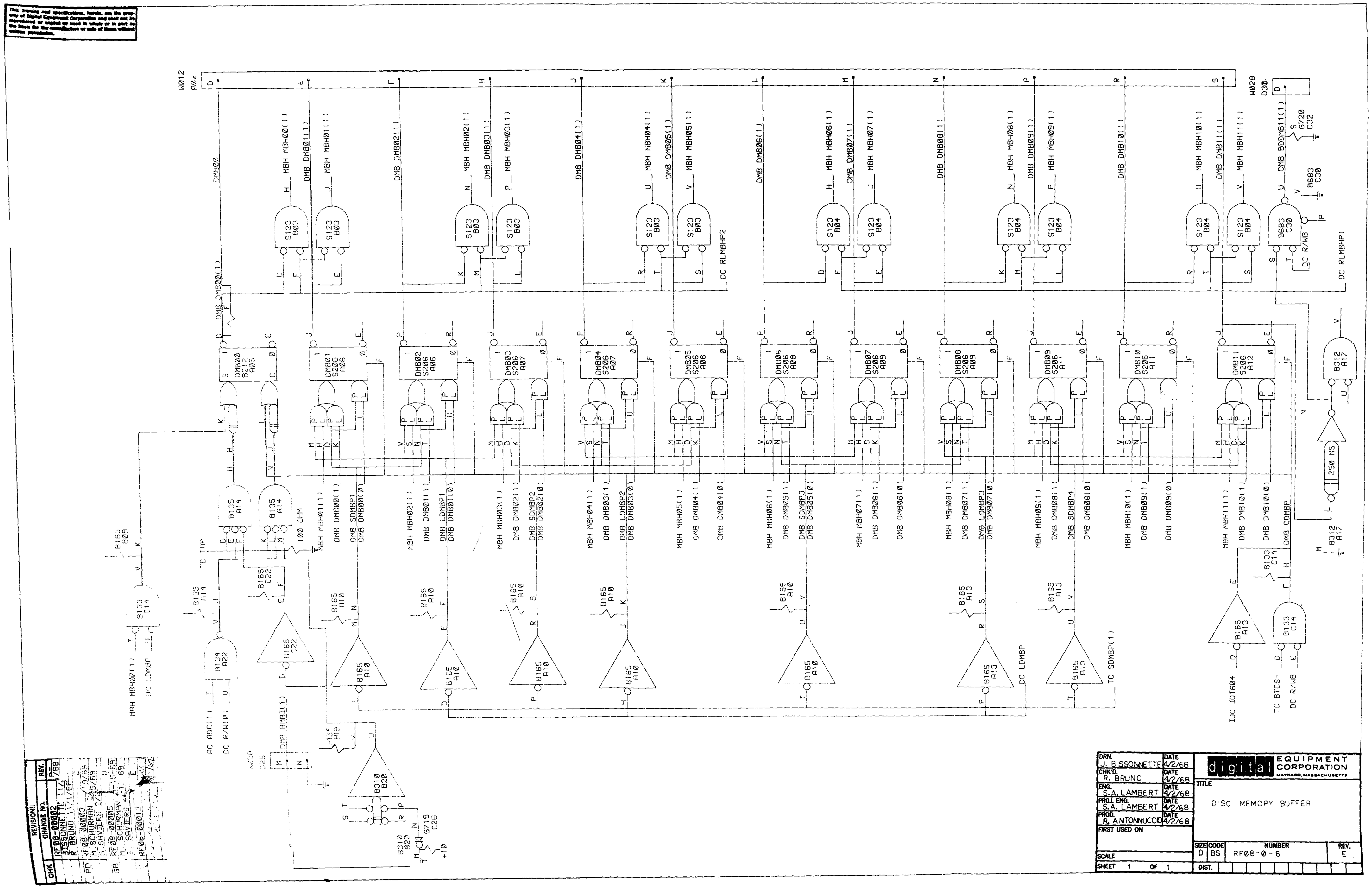
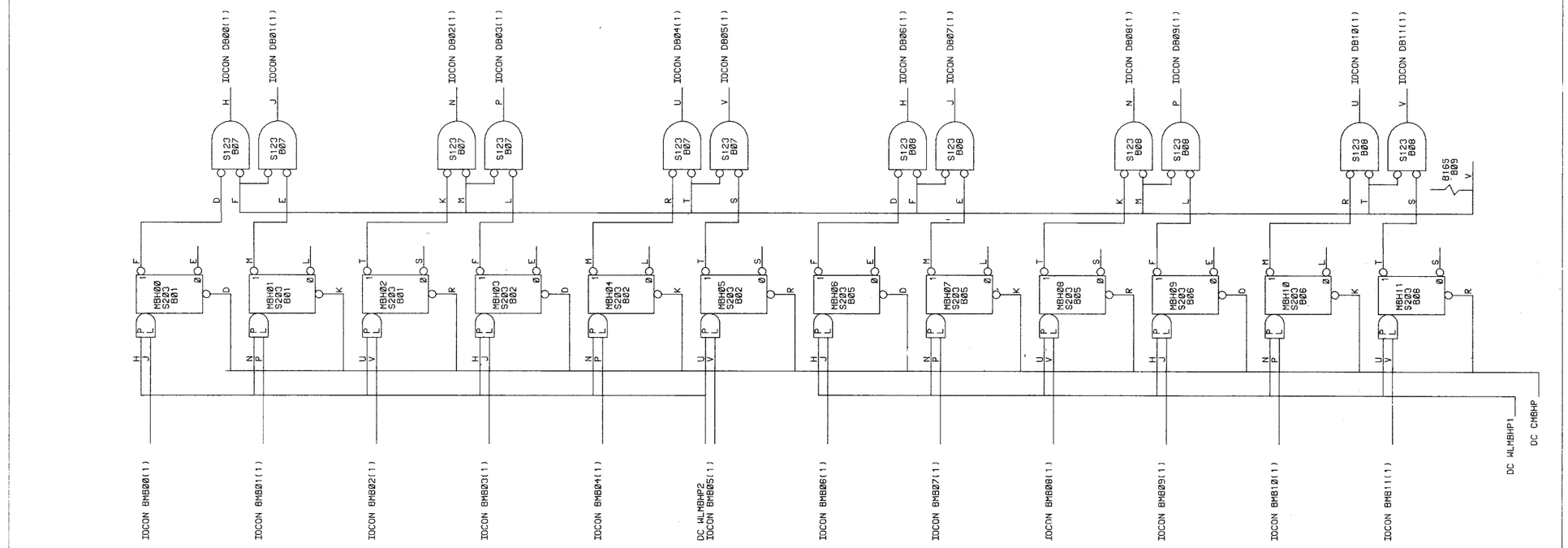


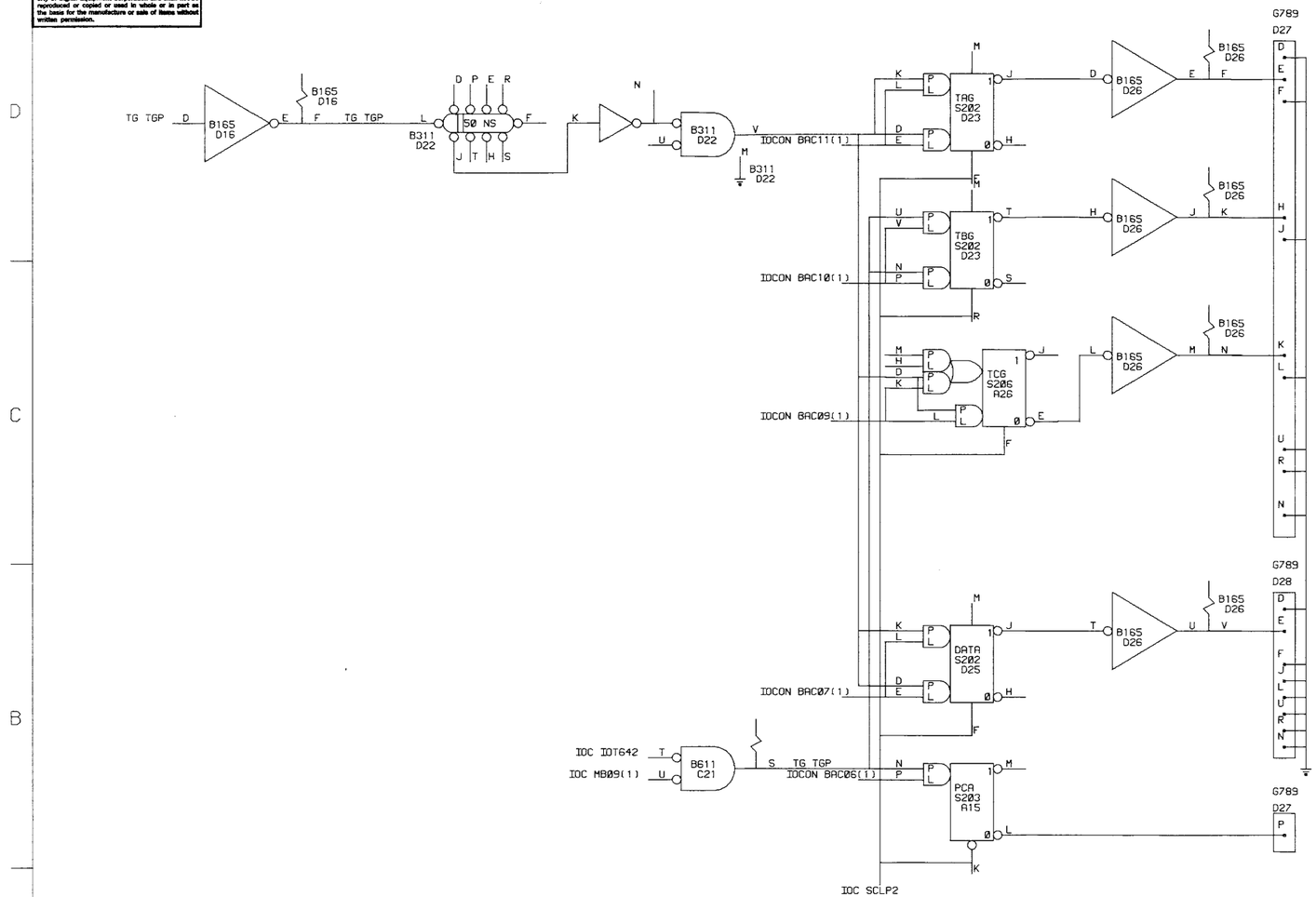
Figure 6-8 Disc Memory Buffer



REVISIONS		
CHK	CHANGE NO.	REV.
	271	A
	BISSONNETTE 6/10/69	
	R BRUNO 6/10/69	
	RF 08-00005	B

DRN. BDS	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. —	DATE	
ENG. M. Jamins	DATE	TITLE: M BH
PROJ. ENG. M. Jamins	DATE	
PROD. E. Tomkins	DATE 11/5/69	
FIRST USED ON		SIZE D · CODE BS · NUMBER 29-08-0-3 · REV. B
SCALE		
SHEET OF		DIST.

Figure 6-9 Memory Buffer Hold



REVISIONS		
CHK	CHANGE NO.	REV.

DRN. BISSONNETTE	DATE	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CH'K'D. R. BRUNO	DATE	
ENG. S.A. LAMBERT	DATE	TITLE: TRACK GENERATOR
ENGL ENG. S.A. LAMBERT	DATE	
PROD. E. Tonkens	DATE 11/5/69	
FIRST USED ON: RF08		SIZE D / CODE 85 / NUMBER RF08-0-10 / REV. C
SCALE		SHEET 1 OF 1 / DIST.

Figure 6-10 Track Generator

APPENDIX A
REFERENCE DOCUMENTS

Related Document and Programs

Reference Documents are listed in Table A-1. Program documents are listed in Table A-2. In addition, several program systems such as the TSS-8 Time Sharing System use the disk file as part of the hardware required for those systems. The documents for these systems contain programming information using the disk file. Such system programs are not listed here.

These publications can be obtained upon request from the nearest DEC field office, or from the following address:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Table A-1
Reference Documents

Document	Description
Digital Logic Handbook (C105)	Function and specifications of FLIP-CHIP modules, cabinets, power supplies and accessories.
PDP-8 Maintenance Manual (F87)	Theory, operation, and maintenance information on the PDP-8 Processor.
PDP-8/I Maintenance Manual (DEC-8I-HR1A-D and DEC-8I-HR2A-D)	Theory, operation, and maintenance information on PDP-8/I Processor.
Small Computer Handbook (C500)	Describes operation and programming of PDP-8 and PDP-8/I computers.

Table A-2
Operation and Maintenance Programs

Program	Description
RF08 Software Package	Perforated program tapes and description of symbolic assembly, assembly language, and utility subroutines.
Multi Disk (Maintenance) DEC-08-D5FA	Tests system logic with the disk in operation.
Disk Data (Maintenance) DEC-08-D5FE	Tests the entire disk logic and disk including the interface, addressing and data.

APPENDIX B

DISK I/O PROGRAMMING EXAMPLE

```
/A SAMPLE OF A TYPICAL I/O ROUTINE FOR THE RF08/RS08 IS INCLUDED BELOW.

0200  4777            JMS I (DISKIO
0201  0000  FUNCT,     0              /X0=READ, X1=WRITE (X=0-7 MEMORY
                                       FIELD)
0202  0000  WDCT,      0              /* WORD COUNT
0203  0000  CORE,      0              /CORE LOCATION
0204  0000  DSKHI,     0              /HIGH ORDER 8 BITS
0205  0000  DSKLOW,    0              /LOW ORDER 12 BITS
0206  5020            JMP ERROR          /ERROR RETURN (AC=ERROR CONDITION)
                                     /NORMAL RETURN (AC=0)

0207  0000  DISKIO,    0
0210  7300            CLL CLA
0211  1607            TAD I DISKIO
0212  6615            DIML           /LOAD EXTENDED MEMORY BITS
0213  1607            TAD I DISKIO
0214  0376            AND (7
0215  7640            SZA CLA

0216  7126            STL RTL        /*2
0217  1375            TAD (3
0220  1374            TAD (6600
0221  3236            DCA RORW           /6603=READ, 6605=WRITE
0222  2207            ISZ DISKIO
0223  1607            TAD I DISK IO
0224  7041            CIA
0225  3773            DCA I (7750    /STORE = WORD COUNT
0226  2207            ISZ DISKIO
0227  1607            TAD I DISKIO
0230  3772            DCA I (7751    /LOAD CORE ADDRESS
0231  2207            ISZ DISKIO
0232  1607            TAD I DISKIO
0233  6643            DXAL           /LOAD HIGH ORDER 9
                                     /BITS OF DISK ADDRESS,
0234  1607            TAD I DISKIO
0235  2207            ISZ DISKIO

0236  0000  RORW,      0              /READ OR WRITE

0237  6623  DISK      DISK           /DONE?
0240  5237            JMP .-1        /NO
0241  6621            DFSE           /YES, ERROR?
```

```
0242  2207            ISZ DISKIO     /SKIP TO NORMAL RETURN
0243  5607            JMP I DISKIO   /RETURN

      6615  DIML=6615
      6623  DISK=6623
      6643  DXAL=6643
      6621  DFSE=6621
      0020  ERROR=20


                    $
      0372     7751
      0373     7750
      0374     6600
      0375     0003
      0376     0007
      0377     0207

      CORE     0203
      DFSE     6621
      DIML     6615
      DISK     6623
      DISKIO   0207
      DSKHI    0204
      DSKLOW   0205
      DXAL     6643
      ERROR    0020
      FUNCT    0201
      RØRW     0236
      WDCT     0202
```

APPENDIX C

LOADING PROCEDURES

Read-In Mode (RIM) Loader

The RIM Loader is a program used to load the Binary Loader. The RIM Loader must be toggled into memory using the switches on the computer console.

To load the RIM Loader, follow the procedure below.

a. Check to see if the RIM Loader program is in memory correctly by examining the following locations for the appropriate instructions (contents).

	Instruction	
Location	ASR33 Reader	High-Speed Reader
7756	6032	6014
7757	6031	6011
7760	5357	5357
7761	6036	6016
7762	7106	7106
7763	7006	7006
7764	7510	7510
7765	5357	5374
7766	7006	7006
7767	6031	6011
7770	5367	5367
7771	6034	6016
7772	7420	7420
7773	3776	3776
7774	3376	3376
7775	5356	5357
7776	0000	0000

b. If the instruction in any location does not agree with the above list, deposit the correct instruction into that location.

Binary Format (BIN) Loader

The BIN Loader is a program used to load MAINDEC into memory. The BIN Loader tape is loaded by the RIM Loader as explained below.

The BIN Loader is loaded into locations 7612-7616, 7626-7752, and 7777, with its starting address at location 7777. A detailed description of the BIN Loader is in the User's Handbook F-85.

To load the BIN Loader, follow the procedure below.

a. Check the RIM Loader for correctness, and correct if necessary.

b. Put Binary Loader tape in reader (always put leader-trailer code over reader head, never blank tape).

c. Turn reader ON.

d. Set Switch Register (SR) to 7756 (the starting address of the RIM Loader).

e. Depress LOAD ADDress switch on computer console.

f. Depress START switch on computer console.

g. Tape should begin reading in, if not, check the RIM Loader and start again at step a.

h. After program is read in, depress STOP switch on the computer console.