

## IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DZDMG-C-D
PRODUCT NAME:	DMC11 CROM AND JUMP TESTS
DATE:	MAY 1977
MAINTAINER:	DIAGNOSTICS
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## 1. ABSTRACT

The function of the DMC11 diagnostics is to verify that the option operates according to specifications. The diagnostics verify that there are no malfunctions and the all operations of the DMC11 are correct in its environment.

Parameters must be set up to alert the diagnostics to the DMC11 configuration. These parameters are contained in the STATUS TABLE and are generated in two ways: 1) Manual Input - the operator answers questions. 2) Autosizing - the program determines the parameters automatically.

DZDMG tests the DMC11-AR and DMC11-AL micro-processors (M8200-YA M8200-YB). It performs jump tests on the micro-processor and verifies the control ROM of the M8200. This diagnostic will not run on a KMC (M8204), however it is possible to load the KMC CRAM with the DMC micro-code. See test 2 for details.

Currently there are five off line diagnostics that are to be run in sequence to insure that if an error should occur it will be detected at an early stage.

NOTE: Additional diagnostics may be added in the future.

The five diagnostics are:

1. DZDMC [REV] Basic w/R and Micro-processor tests
2. DZDME [REV] DDCMP Line unit tests
3. DZDMF [REV] BITSTUFF Line unit tests
4. DZDMG [REV] Jump and CRUM tests
5. DZDMH [REV] Free-running tests (Heat test tape)

## 2. REQUIREMENTS

## 2.1 EQUIPMENT

Any PDP11 family CPU (except an LSI-11) with minimum 8K memory  
ASR 33 (or equivalent)  
DMC11-AR (M8200-YA) or an DMC11-AL (M8200-YB)

## 2.2 STORAGE

Program will use all 8K of memory except where ABL and BOOTSTRAP LOADER reside. Locations 1500 thru 1640; contain the "STATUS TABLE" information which is generated at start of diagnostics by manual input (questions) or automatically (auto-sizing). This area is an overlay area and should not be altered by the operator.

## 3. LOADING PROCEEDURE

### 3.1 METHOD

All programs are in absolute format and are loaded using the ABSOLUTE LOADER. NOTE: if the diagnostics are on a media such as DISK, MAGTAPE, DECTAPE, or CASSETTE; follow instructions for the monitor which has been provided on that specific media.

ABSOLUTE LOADER starting address \*500

MEMORY \* SIZE

4k	17
8k	37
12k	57
16k	77
20k	117
24k	137
28k	157

- 3.1.1 Place address of ABS loader into switch register.  
(also place "HALT" SW up)
- 3.1.2 Depress "LOAD ADDRESS" key on console and release.
- 3.1.3 Depress "START KEY" on console and release (Program should now be loading into CPU)

## 4. STARTING PROCEEDURE

- a. Set switch register to 000200
- b. Depress 'LOAD ADDRESS' key and release
- c. Set SWR to zero for 'AUTO SIZING' or SWR bit0=1 for manual input (questions) or SWR bit7=1 to use existing parameters set up by a previous start or a previously run DMC11 diagnostic.
- d. Depress 'START KEY' and release. The program will type Maindec Name and program name (if this was the first start up of the program) and also the following:

## MAP OF DMC11 STATUS

```

-----
PC      CSR      STAT1  STAT2  STAT3
--      ---      -----
001500 160010 145310 177777 000000
001510 160020 145320 177777 000000

```

The program will type 'R' and proceed to run the diagnostic. The above is only an example. This would indicate the status table starting at add. 1500 in the program. In this example the table contains the information and status of two DMC11'S. THE STATUS TABLE MUST BE VERIFIED BY THE USER IF AUTO SIZING IS DONE. For information of status table see Section 8.4 for help.

If the diagnostic was started with SW00=1 indicating manual parameter input then the following shows an example of the questions asked and some example answers:

HOW MANY DMC11'S TO BE TESTED?1

```

t1
CSR ADDRESS?160010
VECTOR ADDRESS?310
BR PRIORITY LEVEL? (4,5,6,7)?5
DOES MICRO-PROCESSOR HAVE CRAM? (Y OR N)N
WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF
M8202 TYPE "2"?1
IS THE LOOP BACK CONNECTOR ON?Y
SWITCH PAC#1 (DDCMP LINE#)?377
SWITCH PAC#2 (B#873 BOOT ADD)?377

```

Following the questions the status map is printed out as described above, the information in the map reflects the answers to the questions. If the diagnostic was started with SW00=0 and SW07=0 (AUTO-SIZING) then no questions are asked and only the status-map is printed out. If AUTO-SIZING is used the status information must be verified to be correct (match the hardware). If it does not match the hardware the diagnostic must be restarted with SW00=1 and the questions answered.

## 4.1 CONTROL SWITCH SETTINGS

SW 15 Set: Halt on error  
SW 14 Set: Loop on current test  
SW 13 Set: Inhibit error print out  
SW 12 Set: Inhibit type out/abell on error.  
SW 11 Set: Inhibit iterations. (quick pass)  
SW 10 Set: Escape to next test on error  
SW 09 Set: Loop with current data  
SW 08 Set: Catch error and loop on it  
SW 07 Set: Use previous status table.  
SW 06 Set: Halt in RCMCLK routine before clocking  
micro-processor  
SW 05 Set: Reserved  
SW 04 Set: Reserved  
SW 03 Set: Reselect DMC11's desired active  
SW 02 Set: Lock on selected test  
SW 01 Set: Restart program at selected test  
SW 00 Set: Build new status table from questions. (If SW07=0  
and SW00=0 a new status table is built by  
auto-sizing)

Switch 06 and 08-15 are dynamic and can be changed as needed while the diagnostic is running. Switches 00-03 and switch 07 are static, and are used only on starting or restarting the diagnostic.

## 4.1.2 SWITCH REGISTER OPTIONS (at start up)

- SW 01 RESTART PROGRAM AT SELECTED TEST. It is strongly suggested that at least one pass has been made before trying to select a test, the reason being is that the program has to clear areas and set up parameters. When this switch is used the diagnostic will ask TEST NO.? Answer by typing the number of the test desired and carriage return to begin execution at the selected test.
- SW 02 LOCK ON SELECTED TEST. This switch when used with SW01 will cause the program to constantly loop on the selected test. Hitting any key on the console will let it advance to the next test and loop until a key is hit again. If SW02=0 when SW01 is used. The program will begin at the selected test and continue normal operations.
- SW 03 RESELECT DMC11'S DESIRED ACTIVE. Please note that a message is typed out for setting the switch register equal to DMC11's active. This means if the system has four DMC11s; bits 00,01,02,03 will be set in loc "DMACTV" from the switch register. Using this switch(SW00) alters that location; therefore if four DMC11s are in the system \*\*\*DO NOT\*\*\* set switches greater than SW 03 in the up position. This would be a fatal error. do not select more active DMC11s than there is information on in the status table.

METHOD: A: Load address 200  
B: Start with Sw 00=1  
C: Program will type message  
D: Set a switch for each DMC desired active.  
EXAMPLE: If you have 4 DMC's but only want to run the first and the last set SWR bits 0 and 3 = 1. PRESS CONTINUE  
E: Number (IF VALID) will be in data lights (excluding 11/05)  
F: Set with any other switch settings desired. PRESS CONTINUE.

## 4.1.3 DYNAMIC SWITCHES

## ERROR SWITCHES

1. SW 12 Delete print out/bell on error.
2. SW 13 Delete error printout.
3. SW 15 Halt on the error.
4. SW 08 Goto beginning of the test(on error).
5. SW 10 Goto next test(on error).

## SCOPE SWITCHES

1. SW06 Halt in ROMCLK routine before clocking micro-processor instruction. This allows the operator to scope a micro-processor instruction in the static state before it is clocked. Hit continue to resume running.
2. SW09 (if enabled by "SCOPI") on an error; if an '\*' is printed in front of the test no. (ex. \*TEST NO. 10 ) SW09 is incorporated in that test and therefore SW09 is usually the best switch for the scope loop (SW14=0, SW10=0, SW09=1, SW08=0). If SW09 is not enableed; and there is a HARD error (constant); SW08 is best. (SW14=1,0, SW10=0, SW09=0, SW08=1). for intermittemt errors; SW14=1 will loop on test regardless of error or not error. (SW14=1, SW10=0, SW09=0, SW08=1,0)
3. SW11 Inhibit iterations.
4. SW14 Loop on current test.

## 4.2 STARTING ADDRESS

Starting address is at 000200 there are no other starting addresses for the DMC11 diagnostics. (See Section 4.0)

NOTE: If address 000042 is non-zero the program assumes it is under ACT11 or XXDP control and will act accordingly after all available DMC11's are tested the program will return to 'XXDP' or 'ACT-11'.

## 5. OPERATING PROCEDURE

when program is initially started messages as described in section 4.0 will be printed, and program will begin running the diagnostic

## 5.2 PROGRAM AND/OR OPERATOR ACTION

The typical approach should be

1. Halt on error (via SW 15=1) when ever an error occurs.
2. Clear Sw 15.
3. Set SW 14: (loop on this test)
4. Set SW 13: (inhibit error print out)

The TEST NUMBER and PC will be typed out and possibly an error message (this depends on the test) to give the operator an idea as to the source of the problem. If it is necessary to know more information concerning the error report; LOOK IN THE LISTING for that TEST NUMBER which was typed out and then NOTE THE PC of the ERROR REPORT this way the EXACT FUNCTION of the test CAN BE DETERMINED.

## 6. ERRORS

As described previously there will always be a TEST NUMBER and PC typed out at the time of an error (providing SW 13=0 and SW 12=0). In most cases additional information will be supplied in the the error message to give the operator an indication of the error.

### 6.2 ERROR RECOVERY

If for some reason the DMC11 should "HANG THE BUS" (gain control of bus so that console manual functions are inhibited) an init or power down/up is necessary for operator to regain control of cpu. If this should happen; look in location "TSTNO" (address 1226) for the number of the test that was running at the time of the catastrophic error. In this way the operator will have an idea as to what the DMC11 was doing at the time of the error.

## 7. RESTRICTIONS

### 7.1 STARTING RESTRICTIONS

See section 4. (PLEASE)  
Status table should be verified regardless of how program was started. Also it is important to use this listing along with the information printed on the TTY to completely isolate problems.



## 7.2 OPERATING RESTRICTIONS

The first time a DMC11 diagnostic is loaded into core and run the STATUS TABLE must be set up. This is done by manual input (SW00=1) or by autosizing (SW00=0 and SW07=0). Hereafter however the status table need not be setup by subsequent restarts or even loading the next DMC diagnostic because the STATUS TABLE is overlayed. The current parameters in the STATUS TABLE are used when SW07=1 on start up.

## 7.3 HARDWARE CONFIGURATION RESTRICTIONS

DMC11(M8200)- Jumper W1 must be in, and switch 7 of E76 must be in the OFF position.

KMC(M8204)- Jumper W1 must be in.

## 8. MISCELLANEOUS

## 8.1 EXECUTION TIME

All DMC11 device diagnostics will give an 'END PASS' message (providing no errors and sw12=0) within 4 mins. This is assuming SW11=1 (DELETE ITERATIONS) is set to give the fastest possible execution. The actual execution time depends greatly on the PDP11 CPU configuration and the amount of memory in the system.

## 8.2 PASS COMPLETE

NOTE: EVERY time the program is started; the tests will run as if SW11 (delete iterations) was up (=1). This is to 'VERIFY NO HARD ERRORS' as soon as possible. Therefore the first pass -EACH TIME PROGRAM IS STARTED- will be a 'QUICK PASS' until all DMC11's in system are tested. When the diagnostic has completed a pass the following is an example of the print out to be expected.

```
END PASS DZDMG CSR: 175000 VEC: 0300 PASSES: 000001
ERRORS: 002000
```

NOTE: The pass count and error counts are cumulative for each DMC11 that is running, and are set to zero only when the diagnostic is started. Therefore after an overnight run for example, the total passes and errors for each DMC11 since the diagnostic was started are reflected in PASSES: and ERRORS:.

## 8.4 KEY LOCATIONS

RETURN (1214) Contains the address where program will return when iteration count is reached or if loop on test is asserted.

NEXT (1216) Contains the address of the next test to be performed.

TSTNO (1226) Contains the number of the test now being performed.

RUN (1316) The bit in "RUN" always points to the DMC11 currently being tested. EXAMPLE: (RUN) 1302/0000000001000000 Means that DMC11 no.06 is the DMC11 now running.

DMCR00-DMCR17  
DMST00-DMST17  
(1500)-(1640)

These locations contain the information needed to test up to 16 (decimal) DMC11s sequentially. they contain the CSR,VECTOR and STATUS concerning the configuration of each DMC11.

DMACTV (1306) Each bit set in this location indicates that the associated DMC11 will be tested in turn. EXAMPLE: (DMACTV) 1276/0000000000011111 means that DMC11 no. 00,01,02,03,04 will be tested. EXAMPLE: (DMACTV) 1276/0000000000010001 Means that DMC11 no. 00,04 will be tested.

DMCSR (1444) Contains the CSR of the current DMC11 under test.

## 8.4A "STATUS TABLE" (1500-1640)

The table is filled by AUTO SIZING or by the manual parameter input (questions) as described previously. Also if desired by user; the locations may be altered by hand (toggled in) to suit the specific configuration.

The example status map shown below contains information for two DMC11'S. the table can contain up to 16 DMC11'S. Following the map is a description of the bits for each map entry

## MAP OF DMC11 STATUS

```

-----
PC      CSR   STAT1  STAT2  STAT3
--      ---   -----
001500  160010 145310 177777 000000
001510  160020 016320 000000 000000

```

Each map entry contains 4 words which contain the status information for 1 DMC11. The PC shows where in core memory the first of the 4 words is. In the example above the first DMC'S status is in locations, 1500, 1502, 1504, and 1506. The second DMC status is located at 1510, 1512, 1514, and 1516. The information contained in each 4 word entry is defined as follows:

CSR: Contains DMC11 CSP address

STAT1: BITS 00-08 IS DMC11 VECTOR ADDRESS  
BIT15=1 MICRO-PROCESSOR HAS CRAM  
BIT15=0 MICRO-PROCESSOR HAS CROM  
BIT14=1 TURNAROUND CONNECTOR IS ON  
BIT14=0 NO TURNAROUND CONNECTOR  
BIT13=0 LINE UNIT IS AN M8201  
BIT13=1 LINE UNIT IS AN M8202  
BIT12=1 NO LINE UNIT  
BITS 09-11 IS DMC11 BR PRIORITY LEVEL

STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)  
HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)

STAT3: BIT0=1 PERFORM FREE RUNNING TESTS ON KMC  
BIT1=0 DMC11-AR (LOW SPEED)  
BIT1=1 DMC11-AL (HIGH SPEED)

## 8.5 METHOD OF AUTO SIZING

### 8.5.1 FINDING THE CONTROL STATUS REGISTER.

The auto-sizing routine finds a DMC11 as follows: It starts at address 160000 and tests all address in increments of 10 up to and including address 167760. If the address does not time out, the following is done, the first CROM address is written to a 125252 then it is read back. If it contains a -1 or 125252 or 626 or 16520 a DMC11 or KMC11 has been found, if not, the address is updated by 10 and the search continues. A -1 indicates a DMC11 with no CROM, a 125252 indicates a KMC11 with CROM, a 626 indicates a DMC11-AL, and a 16520 indicates a DMC11-AL. Further tests are performed at this point to determine which line unit, if any, is installed, if a loop-back connector is installed and various switch settings on the line unit. THIS IS WHY THE STATUS TABLE MUST BE VERIFIED BY THE USER AND IF ANY OF THE INFORMATION DOES NOT AGREE WITH THE HARDWARE THE DIAGNOSTIC MUST BE RESTARTED AND THE QUESTIONS MUST BE ANSWERED. All DMC11's in the system will be found by the auto-sizer. If it does not find a DMC11 the diagnostic must be restarted and the questions answered.

### 8.5.2 FINDING THE VECTOR AND BR LEVEL

The vector area (address 300-776) is filled with the instruction IOT and '+2' (next address). The processor status is started at 7 and the DMC is programmed to interrupt. The PS is lowered by 1 until the DMC interrupts, a delay is made and if no interrupt occurs at ps level 3 (because of a bad DMC11) the program assumes vector address 300 at BR level 5 and the problem should be fixed in the diagnostic. Once the problem is fixed; the program should be re-setup again to get correct vector. If an interrupt occurred; the address to which the DMC11 interrupted to is picked up and reported as the vector. NOTE: if the vector reported is not the vector set up by you; there is a problem and AUTO SIZING should not be done.

## 8.6 SOFTWARE SWITCH REGISTER

If the diagnostic is run on an 11/04 or other CPU without a switch register then a software switch register is used to allow user the same switch options as described previously. If the hardware switch register does not exist or if one does and it contains all ones (177777) this software switch register is used.

### Control:

To obtain control at any allowable time during execution of the diagnostic the operator types a CTRL G on the console terminal keyboard. As soon as the CTRL G is recognized, by the diagnostic, the following message will be displayed:

SWR=XXXXXX NEW?

Where XXXXXX is the current contents of the software switch register in octal. The software control routine will then await operator action. At which time the operator is required to type one or more of the legal characters: 1) 0 - 7, 2) line feed(<LF>), 3) carriage return(<CR>), or 4) control-U (CTRL U). No check is made for legality. If the input character is not a <LF>, <CR>, or CTRL U it is assumed to be an octal digit.

To change the contents of the SSR the operator simply types the new desired value in octal - leading zeros need not be typed. And terminates the input string with a <CR> or <LF> depending on the program action desired as described below. The input value will be truncated to the last 6 digits typed. At least one digit must be typed on any given input string prior to the terminator before a change to the SSR will occur.

when the input string is terminated with a <CR> the diagnostic will continue execution from the point at which it was interrupted. If a <CR> is the only thing typed the program will continue without changing the SSR. The <LF> differs from the <CR> by restarting the program as if it were restarted at address 200.

If a CTRL U is typed at any point in the input string prior to the terminator the input value will be disregarded and the prompt displayed (SWR = XXXXXX NEW?).

To set the SSR for the starting switches, first load the diagnostic, then hit CTRL G, then start the diagnostic.

DOCUMENT  
\*\*\*\*\*  
DZDMG LST  
\*\*\*\*\*

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- 6 MAINDEC-11-DZDMG-C DMC11 CROM AND JUMP TESTS  
 COPYRIGHT 1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754  
 -----
- 1675 \*\*\*\*\* TEST 1 \*\*\*\*\*  
 THIS IS A SPECIAL TEST WHICH IS ONLY EXECUTED ONE TIME,  
 THE FIRST PASS AFTER THE DIAGNOSTIC IS LOADED. IT TYPES ON  
 THE CONSOLE THE PART NUMBERS OF THE CROMS WHICH THIS  
 REVISION SUPPORTS. TO FORCE A TYPE OUT PATCH LOCATION  
 ROMNUM: TO A ZERO.
- 1696 \*\*\*\*\* TEST 2 \*\*\*\*\*  
 THIS IS A SPECIAL TEST WHICH WILL RUN ON A KMC (DMC WITH  
 WRITABLE CONTROL STORE) TO LOAD THE CROM WITH THE DDCMP  
 MICRO-CODE. FIRST BE SURE BIT1 OF STAT3 IS SET UP AS FOLLOWS  
 1=LOCAL HIGH SPEED CODE, 0=REMOTE LOW SPEED CODE THE STATUS  
 OF STAT3 BIT1 DETERMINES WHICH MICRO-CODE WILL  
 BE LOADED IN THE KMC. LOOP ON THIS TEST FOR A FEW SECONDS  
 TO LOAD THE KMC.
- 1727 \*\*\*\*\* TEST 3 \*\*\*\*\*  
 TEST OF BR RIGHT SHIFT  
 VERIFY THAT A DEST OF BR RSH (011) OF A MICRO-INSTRUCTION  
 SHIFTS THE RESULTING BR DATA RIGHT ONCE.
- 1768 \*\*\*\*\* TEST 4 \*\*\*\*\*  
 CROM READ TEST  
 THIS TEST READS EACH ROM LOCATION AND COMPARES  
 IT TO A SOFTWARE DUPLICATE OF THE CROM. THIS TEST  
 ALSO TESTS THE JUMP(I) MICRO-PROCESSOR INSTRUCTION.
- 1773 IF THIS TEST FAILS CHECK YOUR CROM PART NUMBERS.  
 DZDMG-C SUPPORTS THE FOLLOWING PART NUMBERS:
- DMC11-AR (M8200-YA)  
 23-414A9  
 23-415A9  
 23-416A9  
 23-417A9  
 23-418A9  
 23-419A9  
 23-420A9  
 23-421A9
- DMC11-AL (M8200-YB)  
 23-392A9  
 23-393A9  
 23-394A9  
 23-395A9  
 23-396A9  
 23-397A9  
 23-398A9  
 23-399A9

1840 \*\*\*\*\* TEST 5 \*\*\*\*\*  
CROM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.  
PERFORM THE JUMP INSTRUCTION  
VERIFY THAT THE JUMP DID NOT OCCUR BY READING  
THE CONTENTS OF THE NEW ROM PC (IT SHOULD INCREMENT BY ONE).

1898 \*\*\*\*\* TEST 6 \*\*\*\*\*  
CROM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.  
PERFORM THE JUMP INSTRUCTION  
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

1952 \*\*\*\*\* TEST 7 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.  
SET THE C BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2009 \*\*\*\*\* TEST 10 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.  
SET THE Z BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2066 \*\*\*\*\* TEST 11 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON BR0 SET MICRO-PROCESSOR INSTRUCTION.  
SET THE BR0 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2123 \*\*\*\*\* TEST 12 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.  
SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2180 \*\*\*\*\* TEST 13 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.  
SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2237 \*\*\*\*\* TEST 14 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.  
SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2294 \*\*\*\*\* TEST 15 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.  
CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THAT THE JUMP DID NOT OCCUR BY READING  
THE CONTENTS OF THE NEW ROM PC (IT SHOULD INCREMENT BY ONE).

2352 \*\*\*\*\* TEST 16 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.  
CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THAT THE JUMP DID NOT OCCUR BY READING  
THE CONTENTS OF THE NEW ROM PC (IT SHOULD INCREMENT BY ONE).



2410 \*\*\*\*\* TEST 17 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON BR0 SET MICRO-PROCESSOR INSTRUCTION.  
CLEAR THE BR0 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THAT THE JUMP DID NOT OCCUR BY READING  
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2468 \*\*\*\*\* TEST 20 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.  
CLEAR THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THAT THE JUMP DID NOT OCCUR BY READING  
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2526 \*\*\*\*\* TEST 21 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.  
CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THAT THE JUMP DID NOT OCCUR BY READING  
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2584 \*\*\*\*\* TEST 22 \*\*\*\*\*  
CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.  
CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,  
VERIFY THAT THE JUMP DID NOT OCCUR BY READING  
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

```

1
2
3
4
5
6
7      ;*MAINDEC-11-DZDMG-C  DMC11 CROM AND JUMP TESTS
8      ;*COPYRIGHT 1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
9      ;*-----
10     ;STARTING PROCEDURE
11     ;LOAD PROGRAM
12     ;LOAD ADDRESS 000200
13     ;SWR=0  AUTOSIZE DMC11
14     ;SW07=1  USE CURRENT DMC11 PARAMETERS
15     ;SW00=1  INPUT NEW DMC11 PARAMETERS
16     ;PRESS START
17     ;PROGRAM WILL TYPE "MAINDEC-11-DZDMG-C  DMC11 CROM AND JUMP TESTS"
18     ;PROGRAM WILL TYPE STATUS MAP
19     ;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
20     ;AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
21     ;AND THEN RESUME TESTING
22     ;SUBSEQUENT RESTARTS WILL NOT TYPE PROGRAM TITLE
23
24
25
26
27     ;SWITCH REGISTER OPTIONS
28     ;-----
29
30     100000      SW15=100000      ;=1, HALT ON ERROR
31     040000      SW14=40000      ;=1, LOOP ON CURRENT TEST
32     020000      SW13=20000      ;=1, INHIBIT ERROR TYPEOUT
33     010000      SW12=10000      ;=1, DELETE TYPEOUT/BELL ON ERROR.
34     004000      SW11=4000      ;=1, INHIBIT ITERATIONS
35     002000      SW10=2000      ;=1, ESCAPE TO NEXT TEST ON ERROR
36     001000      SW09=1000      ;=1, LOOP WITH CURRENT DATA
37     000400      SW08=400       ;=1, LOOP ON ERROR
38     000200      SW07=200       ;=1, USE CURRENT DMC11 PARAMETERS, =0, AUTOSIZE DMC11
39     000100      SW06=100       ;=1, HALT BEFORE CLOCKING MICRO-PROCESSOR INSTRUCTION
40     000040      SW05=40
41     000020      SW04=20
42     000010      SW03=10       ;RESELECT DMC11'S TO BE TESTED (ACTIVE)
43     000004      SW02=4         ;LOCK ON TEST SELECT
44     000002      SW01=2         ;RESTART PROGRAM AT SELECTED TEST
45     000001      SW00=1         ;INPUT DMC11 PARAMETERS

```

```

46
47
48     ;REGISTER DEFINITIONS
49     ;-----
50
51     000000      R0=R0          ;GENERAL REGISTER
52     000001      R1=R1          ;GENERAL REGISTER
53     000002      R2=R2          ;GENERAL REGISTER
54     000003      R3=R3          ;GENERAL REGISTER
55     000004      R4=R4          ;GENERAL REGISTER
56     000005      R5=R5          ;GENERAL REGISTER
57     000006      SP=R6          ;PROCESSOR STACK POINTER
58     000007      PC=R7          ;PROGRAM COUNTER
59
60     ;LOCATION EQUIVALENCIES
61     ;-----
62
63     177776      PS=177776      ;PROCESSOR STATUS WORD
64     001200      STACK=1200     ;START OF PROCESSOR STACK
65
66     ;INSTRUCTION DEFINITIONS
67     ;-----
68
69     005746      PUSH1SP=5746    ;DECREMENT PROCESSOR STACK 1 WORD
70     005726      POP1SP=5726     ;INCREMENT PROCESSOR STACK 1 WORD
71     010046      PUSHRO=10046    ;SAVE R0 ON STACK
72     012600      POPRO=12600     ;RESTORE R0 FROM STACK
73     024646      PUSH2SP=24646  ;DECREMENT STACK TWICE
74     022626      POP2SP=22626   ;INCREMENT STACK TWICE
75     .EQUIV ENT,HLT ;BASIC DEFINITION OF ERROR CALL
76
77     ;BIT DEFINITIONS
78     ;-----
79
80     100000      BIT15=100000
81     040000      BIT14=40000
82     020000      BIT13=20000
83     010000      BIT12=10000
84     004000      BIT11=4000
85     002000      BIT10=2000
86     001000      BIT9=1000
87     000400      BIT8=400
88     000200      BIT7=200
89     000100      BIT6=100
90     000040      BIT5=40
91     000020      BIT4=20
92     000010      BIT3=10
93     000004      BIT2=4
94     000002      BIT1=2
95     000001      BIT0=1
96
97

```

TRAPCATCHER FOR UNEXPECTED INTERRUPTS

```

98
99
100 ;*****
101 ;-----
102 ;TRAPCATCHER FOR ILLEGAL INTERRUPTS
103 ;THE STANDARD "TRAP CATCHER" IS PLACED
104 ;BETWEEN ADDRESS 0 TO ADDRESS 776.
105 ;IT LOOKS LIKE "PC+2 HALT".
106 ;-----
107 ;*****
108
109 .=0
110 ;STANDARD INTERRUPT VECTORS
111 ;-----
112
113 .=24
114 .PFAIL ;POWER FAIL HANDLER
115 .340 ;SERVICE AT LEVEL 7
116 .HLT ;ERROR HANDLER
117 .340 ;SERVICE AT LEVEL 7
118 .TRPSRV ;GENERAL HANDLER DISPATCH SERVICE
119 .340 ;SERVICE AT LEVEL 7
120
121 .=40
122 0 ;SAVE FOR ACT-11 OR XXDP
123 0 ;RETURN ADDRESS IF UNDER ACT-11 OR XXDP
124 0 ;SAVE FOR ACT-11 OR XXDP
125 $ENDAD ;FOR USE WITH ACT-11 OR XXDP
126
127 .=52
128 0 ;ACT-11 PROGRAM CHARACTERISTICS
129
130 .=174
131 DISPREG:0 ;SOFTWARE DISPLAY REGISTER
132 SWREG: 0 ;SOFTWARE SWITCH REGISTER
133
134 .=200
135 JMP .START ;GO TO START OF PROGRAM
136
137 .=1000
138 MTITLE: .ASCII <377><12>/MAINDEC-11-DZDMG-C/<377>
139 .ASCIZ /DMC11 CROM AND JUMP TESTS/<377>
140
141 .=1200
142 ;INDIRECT POINTERS TO SWITCH REGISTER AND LIGHT DISPLAY
143 ;-----
144 DISPLAY:177570
145 SWR: 177570

```

PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

```

144
145 ;INDIRECT POINTERS TO TELETYPE VECTORS AND REGISTERS
146 ;-----
147
148 TKCSR: 177560 ;TELETYPE KEYBOARD CONTROL REGISTER
149 TKDBR: 177562 ;TELETYPE KEYBOARD DATA BUFFER
150 TPCSR: 177564 ;TELEPRINTER CONTROL REGISTER
151 TPDBR: 177566 ;TELEPRINTER DATA BUFFER
152
153 ;PROGRAM CONTROL PARAMETERS
154 ;-----
155
156 RETURN: 0 ;SCOPE ADDRESS FOR LOOP ON TEST
157 NEXT: 0 ;ADDRESS OF NEXT TEST TO BE EXECUTED
158 LOCK: 0 ;ADDRESS FOR LOCK ON CURRENT DATA
159 ICOUNT: 3 ;NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE
160 LPCNT: 0 ;NUMBER OF ITERATIONS COMPLETED
161 TSTNO: 0 ;NUMBER OF TEST IN PROGRESS
162 PASCNT: 0 ;NUMBER OF PASSES COMPLETED
163 ERRCNT: 0 ;TOTAL NUMBER OF ERRORS
164 LSTERR: 0 ;PC OF LAST ERROR CALL
165
166 ;PROGRAM VARIABLES
167 ;-----
168
169 STRTSM: 0 ;SWITCHES AT START OF PROGRAM
170 STAT: 0 ;DM STATUS WORD STORAGE
171 CLKX: 0
172 MASKX: 0
173 TEMP1: 0 ;TEMPORARY STORAGE
174 TEMP2: 0 ;TEMPORARY STORAGE
175 TEMP3: 0 ;TEMPORARY STORAGE
176 TEMP4: 0 ;TEMPORARY STORAGE
177 TEMP5: 0 ;TEMPORARY STORAGE
178 SAVR0: 0 ;R0 STORAGE
179 SAVR1: 0 ;R1 STORAGE
180 SAVR2: 0 ;R2 STORAGE
181 SAVR3: 0 ;R3 STORAGE
182 SAVR4: 0 ;R4 STORAGE
183 SAVR5: 0 ;R5 STORAGE
184 SAVSP: 0 ;STACK POINTER STORAGE
185 SAVPC: 0 ;PROGRAM COUNTER STORAGE
186 ZER0: 0
187 ONE: 1
188 NEMLM: 0
189 DMACTV: .BLKW 1 ;HIGHEST LOCATION FOR NPN'S
190 DMNUM: .BLKW 1 ;DMC11'S SELECTED ACTIVE.
191 SAVACT: .BLKW 1 ;OCTAL NUMBER OF DMC11'S.
192 SAVNUM: .BLKW 1 ;ORIGINAL ACTV DEVICES
193 KUN: .BLKW 1 ;WORKABLE NUMBER
194 .EVEN ;POINTER TO RUNNING DEVICE.
195 CREAM: DM,MAP-6 ;TABLE POINTER.
196 MILK: CNT,MAP-4 ;TABLE POINTER

```

```
197  
198 ;PROGRAM CONTROL FLAGS  
199 ;-----  
200  
201 001324 000 ;PROGRAM INITIALIZATION FLAG  
202 001325 000 ;ERROR OCCURED FLAG  
203 001326 000 ;LOCK ON CURRENT TEST FLAG  
204 001327 000 ;QUICK VERIFY FLAG.  
205 ;ON FIRST PASS OF EACH DMC11 ITERATIONS WILL BE  
206  
207  
208 ;DEFINITIONS FOR TRAP SUBROUTINE CALLS  
209 ;POINTERS TO SUBROUTINES CAN BE FOUND  
210 ;IN THE TABLE IMMEDIATLY FOLLOWING THE DEFINITIONS  
211  
212 ;*****  
213 ;-----  
214 001330 ;  
215 001330 104400 ;CALL TO SCOPE LOOP AND ITERATION HANDLER  
216 001330 003576 ;SCOPE  
217 001330 104401 ;CALL TO LOOP ON CURRENT DATA HANDLER  
218 001332 003736 ;SCOPI  
219 001332 104402 ;CALL TO TELETYPE OUTPUT ROUTINE  
220 001334 003766 ;TYPE  
221 001334 104403 ;CALL TO ASCII STRING INPUT ROUTINE  
222 001336 004050 ;INSTR  
223 001336 104404 ;CALL TO INPUT ERROR HANDLER  
224 001340 004154 ;INSTER  
225 001340 104405 ;CALL TO NUMERICAL DATA INPUT ROUTINE  
226 001342 004174 ;PARAM  
227 001342 104406 ;CALL TO REGISTER SAVE ROUTINE  
228 001344 004374 ;SAV05  
229 001344 104407 ;CALL TO REGISTER RESTORE ROUTINE  
230 001346 004434 ;RES05  
231 001346 104410 ;CONVRT  
232 001350 004466 ;CALL TO DATA OUTPUT ROUTINE  
233 001350 104411 ;CONVRT  
234 001352 004472 ;CALL TO DATA OUTPUT ROUTINE WITHOUT CR/LF.  
235 001354 104412 ;CNVRT  
236 001354 005466 ;MSTCLR  
237 001354 104413 ;CALL TO ISSUE A MASTER CLEAR  
238 001356 005436 ;DELAY  
239 001356 104414 ;CALL TO DELAY  
240 001360 005504 ;ROMCLK  
241 001360 104415 ;CALL TO CLOCK ROM ONCE  
242 001362 005552 ;DATACLK  
243 001362 104416 ;CALL TO CLK DATA  
244 001364 005616 ;TIMER  
245 ;CALL TO DELAY A CLOCK TICK  
246 ;-----  
247 ;*****
```

```
248 ;DMC11 CONTROL INDICATORS FOR CURRENT DMC11 UNDER TEST  
249 ;-----  
250  
251 001366 000000 STAT1: 0  
252 001370 000000 STAT2: 0  
253 001372 000000 STAT3: 0  
254  
255 ;DMC11 VECTOR AND REGISTER INDIRECT POINTERS  
256 ;-----  
257  
258 001374 000000 DMRECV: 0 ;POINTER TO DMC11 RECEIVER INTERRUPT VECTOR  
259 001376 000000 DMRLVL: 0 ;POINTER TO DMC11 RECEIVER INTERRUPT SERVICE PS  
260 001400 000000 DMTRVEC: 0 ;POINTER TO DMC11 TRANSMITTER INTERRUPT VECTOR  
261 001402 000000 DMTLVL: 0 ;POINTER TO DMC11 TRANSMITTER INTERRUPT SERVICE PS  
262 001404 000000 DMCSR1: 0 ;POINTER TO DMC11 CONTROL STATUS REGISTER  
263 001406 000000 DMCSRH: 0 ;POINTER TO DMC11 CONTROL STATUS REGISTER HIGH BYTE.  
264 001410 000000 DMCTL: 0 ;POINTER TO DMC11 CONTROL OUT REGISTER  
265 001412 000000 DMPO4: 0 ;POINTER TO DMC11 PURT REGISTER(SEL 4)  
266 001414 000000 DMPO6: 0 ;POINTER TO DMC11 PURT REGISTER(SEL 6)  
267  
268 ;TEMP STORAGE  
269 ;-----  
270  
271 001416 000000 TEMPT: 0  
272 001416 001400 ;.F.+40  
273  
274 ;DMC11 STATUS TABLE AND ADDRESS ASSIGNMENTS  
275 ;-----  
276  
277 ;=1500  
278 001500 DM,MAP: ;  
279 001500 000001 DMC00: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 00  
280 001502 000001 DMS100: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 00  
281 001504 000001 DMS200: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 00  
282 001506 000001 DMS300: .BLKW 1 ;3RD STATUS WORD  
283  
284 001510 000001 DMC01: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 01  
285 001512 000001 DMS101: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 01  
286 001514 000001 DMS201: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 01  
287 001516 000001 DMS301: .BLKW 1 ;3RD STATUS WORD  
288  
289 001520 000001 DMC02: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 02  
290 001522 000001 DMS102: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 02  
291 001524 000001 DMS202: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 02  
292 001526 000001 DMS302: .BLKW 1 ;3RD STATUS WORD  
293  
294 001530 000001 DMC03: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 03  
295 001532 000001 DMS103: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 03  
296 001534 000001 DMS203: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 03  
297 001536 000001 DMS303: .BLKW 1 ;3RD STATUS WORD  
298  
299 001540 000001 DMC04: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 04  
300 001542 000001 DMS104: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 04  
301 001544 000001 DMS204: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 04  
302 001546 000001 DMS304: .BLKW 1 ;3RD STATUS WORD  
303
```

```

304 001550 000001 DMS005: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 05.
305 001552 000001 DMS105: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 05
306 001554 000001 DMS205: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 05
307 001556 000001 DMS305: .BLKW 1 ;3RD STATUS WORD
308
309 001560 000001 DMS006: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 06
310 001562 000001 DMS106: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 06
311 001564 000001 DMS206: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 06
312 001566 000001 DMS306: .BLKW 1 ;3RD STATUS WORD
313
314 001570 000001 DMS007: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 07
315 001572 000001 DMS107: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 07
316 001574 000001 DMS207: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 07
317 001576 000001 DMS307: .BLKW 1 ;3RD STATUS WORD
318
319 001600 000001 DMS100: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 10
320 001602 000001 DMS110: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 10
321 001604 000001 DMS210: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 10
322 001606 000001 DMS310: .BLKW 1 ;3RD STATUS WORD
323
324 001610 000001 DMS111: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 11
325 001612 000001 DMS111: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 11
326 001614 000001 DMS211: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 11
327 001616 000001 DMS311: .BLKW 1 ;3RD STATUS WORD
328
329 001620 000001 DMS112: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 12
330 001622 000001 DMS112: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 12
331 001624 000001 DMS212: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 12
332 001626 000001 DMS312: .BLKW 1 ;3RD STATUS WORD
333
334 001630 000001 DMS113: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 13
335 001632 000001 DMS113: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 13
336 001634 000001 DMS213: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 13
337 001636 000001 DMS313: .BLKW 1 ;3RD STATUS WORD
338
339 001640 000001 DMS114: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 14
340 001642 000001 DMS114: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 14
341 001644 000001 DMS214: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 14
342 001646 000001 DMS314: .BLKW 1 ;3RD STATUS WORD
343
344 001650 000001 DMS115: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 15
345 001652 000001 DMS115: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 15
346 001654 000001 DMS215: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 15
347 001656 000001 DMS315: .BLKW 1 ;3RD STATUS WORD
348
349 001660 000001 DMS116: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 16
350 001662 000001 DMS116: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 16
351 001664 000001 DMS216: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 16
352 001666 000001 DMS316: .BLKW 1 ;3RD STATUS WORD
353
354 001670 000001 DMS117: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 17
355 001672 000001 DMS117: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 17
356 001674 000001 DMS217: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 17
357 001676 000001 DMS317: .BLKW 1 ;3RD STATUS WORD
358
359 001700 000000 DN.END: 000000

```

```

360 ;DMC11 PASS COUNT AND ERROR COUNT TABLE
361 ;-----
362
363
364 CNT.MAP:
365 001702 000000 FACT00: 0 ;PASS COUNT FOR DMC11 NUMBER 00
366 001704 000000 ERCT00: 0 ;ERROR COUNT FOR DMC11 NUMBER 00
367
368 001706 000000 FACT01: 0 ;PASS COUNT FOR DMC11 NUMBER 01
369 001710 000000 ERCT01: 0 ;ERROR COUNT FOR DMC11 NUMBER 01
370
371 001712 000000 FACT02: 0 ;PASS COUNT FOR DMC11 NUMBER 02
372 001714 000000 ERCT02: 0 ;ERROR COUNT FOR DMC11 NUMBER 02
373
374 001716 000000 FACT03: 0 ;PASS COUNT FOR DMC11 NUMBER 03
375 001720 000000 ERCT03: 0 ;ERROR COUNT FOR DMC11 NUMBER 03
376
377 001722 000000 FACT04: 0 ;PASS COUNT FOR DMC11 NUMBER 04
378 001724 000000 ERCT04: 0 ;ERROR COUNT FOR DMC11 NUMBER 04
379
380 001726 000000 FACT05: 0 ;PASS COUNT FOR DMC11 NUMBER 05
381 001730 000000 ERCT05: 0 ;ERROR COUNT FOR DMC11 NUMBER 05
382
383 001732 000000 FACT06: 0 ;PASS COUNT FOR DMC11 NUMBER 06
384 001734 000000 ERCT06: 0 ;ERROR COUNT FOR DMC11 NUMBER 06
385
386 001736 000000 FACT07: 0 ;PASS COUNT FOR DMC11 NUMBER 07
387 001740 000000 ERCT07: 0 ;ERROR COUNT FOR DMC11 NUMBER 07
388
389 001742 000000 FACT10: 0 ;PASS COUNT FOR DMC11 NUMBER 10
390 001744 000000 ERCT10: 0 ;ERROR COUNT FOR DMC11 NUMBER 10
391
392 001746 000000 FACT11: 0 ;PASS COUNT FOR DMC11 NUMBER 11
393 001750 000000 ERCT11: 0 ;ERROR COUNT FOR DMC11 NUMBER 11
394
395 001752 000000 FACT12: 0 ;PASS COUNT FOR DMC11 NUMBER 12
396 001754 000000 ERCT12: 0 ;ERROR COUNT FOR DMC11 NUMBER 12
397
398 001756 000000 FACT13: 0 ;PASS COUNT FOR DMC11 NUMBER 13
399 001760 000000 ERCT13: 0 ;ERROR COUNT FOR DMC11 NUMBER 13
400
401 001762 000000 FACT14: 0 ;PASS COUNT FOR DMC11 NUMBER 14
402 001764 000000 ERCT14: 0 ;ERROR COUNT FOR DMC11 NUMBER 14
403
404 001766 000000 FACT15: 0 ;PASS COUNT FOR DMC11 NUMBER 15
405 001770 000000 ERCT15: 0 ;ERROR COUNT FOR DMC11 NUMBER 15
406
407 001772 000000 FACT16: 0 ;PASS COUNT FOR DMC11 NUMBER 16
408 001774 000000 ERCT16: 0 ;ERROR COUNT FOR DMC11 NUMBER 16
409
410 001776 000000 FACT17: 0 ;PASS COUNT FOR DMC11 NUMBER 17
411 002400 000000 ERCT17: 0 ;ERROR COUNT FOR DMC11 NUMBER 17
412

```

413

FORMAT OF STATUS TABLE

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	CSR
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	STAT1
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	STAT2
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	STAT3
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	

DEFINITION OF FORMAT

CSR: CONTAINS DMC11 CSR ADDRESS

STAT1: BITS 00-09 IS DMC11 VECTOR ADDRESS  
 BIT15=1 MICRO-PROCESSOR HAS CROM  
 BIT15=0 MICRO-PROCESSOR HAS CROM  
 BIT14=1 ??? TURNAROUND CONNECTOR IS ON  
 BIT14=0 NO TURNAROUND CONNECTOR  
 BIT13=0 LINE UNIT IS AN M8201  
 BIT13=1 LINE UNIT IS AN M8202  
 BIT12=1 NO LINE UNIT  
 BITS 09-11 IS DMC11 BR PRIORITY LEVEL

STAT2: LOW BYTE IS SWITCH PAC#1 (0DCMP LINE NUMBER)  
 HIGH BYTE IS SWITCH PAC#2 (BM073 BOOT ADD)

STAT3: BIT0=1 DO FREE RUNNING TESTS ON KMC  
 (MUST BE SET TO A ONE MANUALLY [PROGRAM DZDMI ONLY])  
 KMC MUST HAVE MICRO-CODE WRITTEN FROM RUNNING  
 DZDMG TEST 2 FIRST  
 BIT1=1 DMC11-AL LOCAL HIGH SPEED MICRO-CODE  
 BIT1=0 DMC11-AR REMOTE LOW SPEED MICRO-CODE

```

468
469 ;PROGRAM INITIALIZATION
470 ;LOCK OUT INTERRUPTS
471 ;SET UP PROCESSOR STACK
472 ;SET UP POWER FAIL VECTOR
473 ;CLEAR PROGRAM CONTROL FLAGS AND COUNTS
474 ;TYPE TITLE MESSAGE
475
476 002002 012737 000340 177776 .START: MOV #340,PS ;LOCK OUT INTERRUPTS
477 002010 012706 001200 MOV #STACK,SP ;SET UP STACK
478 002014 012737 005336 000024 MOV #,PFAIL,0#24 ;SET UP POWER FAIL VECTOR
479 002022 013737 001310 001314 MOV DNUM,SAVNUM ;SAVE NUMBER OF DEVICES IN SYSTEM.
480 002030 005037 010010 CLR SWFLG ;CLEAR SOFT TYPEDOUT FLAG
481 002034 105037 001325 CLR ERRFLG ;CLEAR ERROR FLAG
482 002040 105037 001327 CLR QV,FLG ;ZERO QUICK VERIFY FLAG
483 002044 012737 001470 001320 MOV #DM,MAP-10,CREAM;GET MAP POINTER.
484 002052 012737 001676 001322 MOV #CNT,MAP-4,MILK;GET PASS COUNT MAP POINTER
485 002060 012737 100000 001316 MOV #BIT15,RUN ;POINT POINTER TO FIRST DEVICE.
486 002066 012709 001702 MOV #CNT,MAP,R0 ;PASS COUNT POINTER TO R0
487 002072 005020 238: CLR (R0)+ ;CLEAR TABLE
488 002074 022700 002002 CMP #CNT,MAP+100,R0 ;DONE YET?
489 002100 001374 BNE 238 ;KEEP GOING
490 002102 005037 001234 CLR LSTERR ;CLEAR LAST ERROR POINTER
491 002106 012737 000001 001226 MOV #1,TSTNO ;SET UP FOR TEST 1
492 002114 012737 002002 001214 MOV #,START,RETURN ;SET UP FOR POWER FAIL BEFORE
493 ;TESTING STARTS
494 002122 013746 000006 MOV #*6,-(SP) ;SAVE CURRENT VECTORS
495 002126 013746 000004 MOV #*4,-(SP) ;
496 002132 012737 002166 000004 MOV #66,0#4 ;SET UP FOR TIMEOUT
497 002140 012737 177570 001202 MOV #177570,SWR ;SET SWR TO HARD SWR ADDRESS
498 002146 012737 177570 001200 MOV #177570,DISPLAY ;SET DISPLAY TO HARD SWR ADDRESS
499 002151 022777 177777 177020 CMP #-1,0SWR ;REFERENCE HARDWARE SWITCH REGISTER
500 002162 001402 BEQ 68+2 ;IF = -1 USE SOFT SWR ANYWAY
501 002164 000407 BR 78 ;IF IT EXISTS AND NOT = -1 USE HARD SWR
502 002166 022626 68: CMP (SP)+,(SP)+ ;ADJUST STACK
503 002170 012737 000176 001402 MOV #SWREG,SWR ;POINTER TO SOFT SWR
504 002176 012737 000174 001200 MOV #DISPREG,DISPLAY;POINTER TO SOFT DISPLAY REG
505 002204 012637 000004 78: MOV (SP)+,#*4 ;RESTORE VECTORS
506 002210 012637 000006 MOV (SP)+,#*6 ;
507 002214 105737 001324 TSTH INIFLG ;HAS INITIALIZATION BEEN PERFORMED
508 002220 001006 BNE 208 ;BR IF YES
509 002222 022737 003522 000042 CMP #SENDAD,0#42 ;IF ACT-11 AUTOMATIC MODE, DON'T TYPE ID
510 002230 001402 BEQ 206
511 002232 101402 TYPE #,MTITLE ;TYPE TITLE MESSAGE
512 002236 001737 007606 206: JSR PC,CKSWR ;CHECK FOR SOFT SWR
513 002242 017737 176734 001236 MOV #SWR,STRTSW ;STORE STARTING SWITCHES
514 002250 005737 000042 TST 0#42 ;IS IT RUNNING IN AUTO MODE?
515 002254 001402 BEQ +6 ;BR IF NO
516 002256 005037 001236 CLR STRTSW ;IF YES, CLEAR SWITCHES
517 002262 012737 000001 001236 BIT #SW00,STRTSW ;IF SW00=1, QUESTIONS ARE ASKED.
518 002270 001012 BNE 178 ;BR IF SW00=1
519 002272 105737 001236 TSTH STRTSW ;BIT7=1??
520 002274 100007 BPL 178 ;BR IF SW07=0
521 002300 005737 001306 TST UMACTV ;ARE ANY DEVICES SELECTED?
522 002304 001006 BNE 168 ;BR IF YES
523 002306 101402 TYPE #,NOACT ;NO DEVICES SELECTED.

```

PROGRAM INITIALIZATION AND START UP.

```
524 J02312 000000 HALT ;STOP THE SHOW
525 J02311 000776 BR ;DISQUALIFY CONTINUL SWITCH
526 J02316 004737 175: JSR PC,AUTO.SIZE ;GO DO THE AUTO SIZE
527 J02322 105737 001324 160: TSTB INIFLG ;FIRST TIME?
528 J02326 001410 BEQ 218 ;BR IF YES
529 J02330 105737 001236 TSTB STRTSM ;IF USING SAME PARAMETERS DONT TYPE MAP
530 J02334 100431 BMI 15
531 J02336 022737 000406 001236 BIT #BIT15,2,STRTSM;IS TEST NO. OR LOCK SELECTED
532 J02344 001403 BEQ 248 ;IF NO THEN TYPE STATUS
533 J02346 000424 BR 15 ;IF YES DO NOT TYPE STATUS
534 J02350 000137 001324 218: COM INIFLG ;SET FLAG
535 J02354 104402 000224 248: TYPE ,AHEAD ;TYPE HEADER
536 J02360 012704 001500 MOV #DM,MAP,R4 ;SET POINTER
537 J02364 010437 001246 56: MOV R4,TEMP1 ;SET ADDRESS
538 J02370 012437 001250 MOV (R4)+,TEMP2 ;SET CSR
539 J02374 001411 BEQ 15 ;ALL DONE IF ZERO
540 J02376 012437 001252 MOV (R4)+,TEMP3 ;SET STAT1
541 J02402 012437 001254 MOV (R4)+,TEMP4 ;SET STAT2
542 J02406 012437 001256 MOV (R4)+,TEMP5 ;SET STAT3
543 J02412 104410 CONVRT ;TYPE OUT STATUS MAP
544 J02414 007454 XSTATQ ;
545 J02416 000762 BR 56
546 J02420 012700 001500 15: MOV #DM,MAP,R0 ;R0 POINTS TO STATUS TABLE
547
548 ;*****
549 ;*AUTO SIZE TEST
550 ;*THIS TEST VERIFYS THAT THE DMC11S AND/OR KMC11S ARE AT THE CORRECT FLOATING
551 ;*ADDRESSES FOR YOUR SYSTEM. IF THIS TEST FAILS, IT IS NOT A HARDWARE ERROR.
552 ;*CHECK THE ADDRESSES OF ALL FLOATING DEVICES (DJ,OH,DO,DU,DUP,LK,DMC,DZ,KMC),
553 ;*IF THERE ARE NO OTHER FLOATING DEVICES BEFORE THE DMC11, THE FIRST
554 ;*DMC11 ADDRESS IS 760070, KMC11 IS 760110. NO DEVICE SHOULD EVER BE AT
555 ;*ADDRESS 760000. THIS TEST MAY REQUIRE 2 OR MORE ATTEMPTS TO GET THE
556 ;*RIGHT ADDRESSES. AFTER YOU HAVE CHANGED THE ADDRESS TO WHAT IT TOLD
557 ;*YOU THE FIRST TIME, IT MAY COME BACK AND TELL YOU A DIFFERENT ADDRESS
558 ;*THE NEXT TIME YOU RUN IT. PLEASE HAVE PATIENCE, THE FINAL ADDRESS
559 ;*WILL BE CORRECT (AS LONG AS ALL DEVICES IN FRONT OF THE DMC'S ARE
560 ;*CORRECT).
561 ;*****
562
563 J02424 013746 000004 MOV #4,-(SP) ;SAVE LOC 4
564 J02430 013746 000006 MOV #6,-(SP) ;SAVE LOC 6
565 J02434 005037 000006 CLR #6 ;CLEAR VEC+2
566 J02440 005037 001252 CLR TEMP3 ;CLEAR FLAG
567 J02444 005005 CLR RS ;RS=0=DMC, RS=-1=KMC
568 J02446 011037 001404 AUSTRT: MOV (R0),DMCSR ;GET NEXT DMC CSR
569 J02452 001564 BEQ AUDONE ;BR IF DONE
570 J02454 005705 TST RS ;DMC OR KMC?
571 J02456 001005 BNE 16 ;BR IF KMC
572 J02460 032760 100000 000002 BIT #BIT15,2(R0) ;CHECK FOR DMC CSR
573 J02466 001061 BNE SKIP ;SKIP IF NOT DMC
574 J02470 000404 BR 26 ;IT'S A DMC SO CONTINUE
575 J02472 032760 100000 000002 15: BIT #BIT15,2(R0) ;CHECK FOR KMC CSR
576 J02500 001454 BEQ SKIP ;SKIP IF NOT KMC
577 J02502 012737 002674 000004 26: MOV #NODEV,##4 ;SET UP FOR TIMEOUT
578 J02510 005705 TST RS ;DMC OR KMC?
579 J02512 001003 BNE 36 ;BR IF KMC
```

PROGRAM INITIALIZATION AND START UP.

```
580 J02514 012703 000006 MOV #6,R3 ;R3 IS COUNT OF DEVICES BEFORE DMC
581 J02520 000402 BR 46 ;GO ON
582 J02522 012703 000010 35: MOV #10,R3 ;R3 IS COUNT OF DEVICES BEFORE KMC
583 J02526 012702 003010 45: MOV #DEVTAB,R2 ;R2 IS DEVICE TABLE POINTER
584 J02532 012701 160010 MOV #160010,R1 ;START WITH ADDRESS 160010
585 J02536 005711 FLOAT: TST (R1) ;CHECK ADDRESS IN R1
586 J02540 111204 MOV#B ADD (R2),R4 ;IF NO TIMEOUT, GET NEXT ADDRESS
587 J02542 000401 R4,R1 ;IN R1
588 J02544 005201 INC R1 ;
589 J02546 000401 BIC R4,R1 ;
590 J02550 005703 TST R3 ;ANY MORE DEVICES TO CHECK FOR?
591 J02552 001371 BNE FLOAT ;BR IF YES
592 J02554 012737 002700 000004 MOV #ERR,##4 ;OK ONLY DMC'S ARE LEFT, SET UP FOR TIMEOUT
593 J02556 010137 003022 35: MOV R1,XLOC ;SAVE FIRST DMC/KMC ADDRESS
594 J02560 005705 FY: TST R5 ;DMC OR KMC?
595 J02570 001005 BNE 16 ;BR IF KMC
596 J02572 032760 100000 000002 BIT #BIT15,2(R0) ;CHECK FOR DMC CSR
597 J02600 001014 BNE SKIP ;SKIP IF NOT DMC
598 J02602 000404 BR 26 ;IT'S A DMC SO CONTINUE
599 J02604 032760 100000 000002 15: BIT #BIT15,2(R0) ;CHECK FOR KMC CSR
600 J02612 001407 BEQ SKIP ;SKIP IF NOT KMC
601 J02614 005711 26: TST (R1) ;CHECK DMC ADDRESS
602 J02616 020137 001404 CMP R1,DMCSR ;DOES IT MATCH
603 J02622 001011 BEQ OK ;BR IF YES
604 J02624 002701 000010 ADD #10,R1 ;GET NEXT DMC ADDRESS
605 J02630 000756 FY ;DO IT AGAIN
606 J02632 002700 000010 SKIP: ADD #10,R0 ;SKIP TO NEXT CSR IN TABLE
607 J02636 011037 001404 MOV (R0),DMCSR ;GET NEXT CSR
608 J02642 001470 BEQ AUDONE ;BR IF DONE
609 J02644 000750 BR FY ;ELSE CONTINUE
610 J02646 002700 000010 OK: ADD #10,R0 ;SKIP TO NEXT DMC CSR
611 J02652 002737 000014 003022 ADD #10,XLOC ;UPDATE EXPECTED DMC/KMC ADDRESS
612 J02660 011037 001404 MOV (R0),DMCSR ;GET NEXT DMC/KMC CSR
613 J02666 001457 BEQ AUDONE ;BR IF DONE
614 J02670 013701 003022 MOV XLOC,R1 ;GET EXPECTED DMC/KMC ADDRESS
615 J02672 000735 BR FY ;CONTINUE
616 J02674 122243 NODEV: CMPS (R2)+,-(R3) ;ON TIMEOUT, INC R2, DEC R3
617 J02676 000002 RTI ;RETURN
618 J02700 005737 001252 ERR: TST TEMP3 ;CHECK FLAG IF = 0 TYPE HEADER
619 J02704 001011 BNE 15 ;SKIP HEADER
620 J02706 104402 TYPE ;TYPEOUT HEADER MESSAGE
621 J02710 007223 CONERR ;CONFIGURATION ERROR!!!
622 J02712 012737 002700 001276 MOV #ERR,SAVPC ;SAVE PC FOR TYPEOUT
623 J02720 104411 CHVRT ;TYPE OUT ERROR PC
624 J02722 002770 ERRPC ;
625 J02724 104402 TYPE ;TYPE REST OF HEADER
626 J02726 007277 CHERR ;
627 J02730 012737 177777 001252 15: MOV #1,TEMP3 ;SET FLAG SO IT ONLY GETS TYPED ONCE
628 J02736 010137 001262 MOV R1,SAVH1 ;SAVE R1 FOR TYPEOUT
629 J02742 104410 CONVRT ;
630 J02744 002776 CONTAB ;TYPE CSR VALUES
631 J02746 005705 TST R5 ;DMC OR KMC ?
632 J02750 001003 BNE 36 ;BR IF KMC
633 J02752 104402 TYPE ;
634 J02754 007320 DMCM ;
635 J02756 000132 BR 46 ;CONTINUE
```

```
636 002760 104402 3S: TYPE
637 002762 007330 KMCB
638 002764 022626 4S: CMP (SP)+,(SP)+ ;ADJUST STACK
639 002766 000727 BR OK ;BR TO GET OUT
640 002770 000001 ERRPC: 1
641 002772 006 002 ,BYTE 0,2
642 002774 001276 ,BYTE SAVPC
643 002776 000002 CONTAB: 2
644 003000 006 004 ,BYTE 0,4
645 003002 003022 XLOC
646 003004 006 002 ,BYTE 0,2
647 003006 001404 DMCSR
648 003010 007 DEVTAB: ,BYTE 7 ;DJ
649 003011 017 ,BYTE 17 ;DH
650 003012 007 ,BYTE 7 ;DO
651 003013 007 ,BYTE 7 ;DU
652 003014 007 ,BYTE 7 ;DUP
653 003015 007 ,BYTE 7 ;LK
654 003016 007 ,BYTE 7 ;DMC
655 003017 007 ,BYTE 7 ;DZ
656 003020 007 ,BYTE 7 ;KMC
657 003022 000000 ,EVEN
658 003024 005705 XLOC: 0
659 003026 001005 AUDONE: TST R5 ;DMC?
660 003030 012705 17777 BNE 18 ;BR IF KMC AND ALL DONE
661 003034 012700 001500 MOV #1,R5 ;SET R5 TO #1 (KMC)
662 003040 000602 BR #DM,MAP,R0 ;RESET R0 TO START OF TABLE
663 003042 012637 000006 1S: MOV AUSTRT ;GO DO KMC'S
664 003046 012637 000004 MOV (SP)+,#06 ;RESTORE LOC 6
665 003050 012637 000010 MOV (SP)+,#04 ;RESTORE LOC 4
666 003052 012737 000010 001236 BIT #SW03,STRTSW ;SELECT SPECIFIC DEVICES??
667 003060 001422 BEQ 3S ;BR IF NO.
668 003062 104402 006144 TYPE ,MNEW ;TYPE THE MESSAGE.
669 003065 005000 CLR R0 ;ZERO DATA LIGHTS
670 003070 000000 HALT ;WAIT FOR USER TO TELL WHAT DEVICES TO RUN
671 003072 027737 176104 001312 CMP #SWR,SAVACT ;IS THE NUMBER VALID?
672 003100 101404 BLOS 2S ;BR IF NUMBER IS OK.
673 003102 104402 006005 TYPE ,MERR3 ;TELL USER OF INVALID NUMBER.
674 003106 000000 HALT ;STOP EVERY THING.
675 003110 000776 BR #-2 ;RESTART THE PROGRAM AGAIN.
676 003112 017737 176064 001306 2S: MOV #SWR,DMACTV ;GET NEW DEVICE PATTERN
677 003120 013700 001306 MOV DMACTV,R0 ;SHOW THE USER WHAT HE SELECTED.
678 003124 000000 HALT ;CONTINUE DYNAMIC SWITCHES.
679 003126 012700 000300 3S: MOV #300,R0 ;PREPARE TO CLEAR THE FLOATING
680 003132 012701 000302 MOV #302,R1 ;VECTOR AREA, 300-776
681 003136 010120 4S: MOV R1,(R0)+ ;START PUTTING "PC+2 = HALT"
682 003140 005021 CLR (R1)+ ;IN VECTOR AREA.
683 003142 022021 CMP (R0)+,(R1)+ ;POP POINTERS.
684 003144 022700 001000 CMP #1000,R0 ;ALL DONE??
685 003150 001372 BNE 4S ;BR IF NO.
686
687 ;TEST START AND RESTART
688 ;-----
689
690 003152 012706 001200 ,BEGIN: MOV #STACK,SP ;SET UP STACK
691 003156 013746 000000 MOV #6,-(SP) ;SAVE LOC 6
```

```
692 003162 013746 000004 MOV #4,-(SP) ;SAVE LOC 4
693 003166 005000 CLR R0 ;START AT 0
694 003170 012737 003234 000004 MOV #28,#04 ;SET UP FOR TIME OUT
695 003176 005037 000006 CLR #06 ;TO AUTOSIZE MEMORY
696 003202 005720 6S: TST (R0)+ ;CHECK ADDRESS IN R0
697 003204 022700 157776 CMP #157776,R0 ;IS IT AT LEAST 28K
698 003210 001374 BNE 6S ;BR IF NO
699 003212 102700 007776 SUB #7776,R0 ;SAVE 2K FOR MONITORS
700 003216 010037 001304 7S: MOV R0,MENLIM ;STORE MEMORY LIMIT
701 003222 012637 000004 MOV (SP)+,#04 ;RESTORE LOC 4
702 003226 012637 000006 MOV (SP)+,#06 ;RESTORE LOC 6
703 003232 002113 BR 10S ;CONTINUE
704 003234 022626 2S: CMP (SP)+,(SP)+ ;ADJUST STACK
705 003236 102700 000004 SUB #4,R0 ;GET LAST GOOD ADDRESS
706 003242 102700 007776 SUB #7776,R0 ;SAVE 2K FOR MONITORS
707 003246 022700 030000 CMP #30000,R0 ;IS IT OK?
708 003252 001361 BNE 7S ;BR IF NO
709 003254 012700 037400 MOV #37400,R0 ;IF OK DON'T SAVE 2K
710 003260 000756 BR 7S ;
711 003262 012737 000340 10S: MOV #340,PS ;LOCK OUT INTERRUPTS
712 003270 012737 000004 001236 BIT #BIT2,STRTSW ;CHECK FOR LOCK ON TEST
713 003276 001411 BEQ 1S ;BR IF NO LOCK DESIRED.
714 003300 104402 006043 TYPE ,MLOCK ;TYPE LOCK SELECTED.
715 003304 012737 000240 003012 MOV #NOP,TTST ;ADJUST SCOPE ROUTINE.
716 003312 012737 000240 003014 MOV #NOP,TTST+2 ;SET UP TO LOCK
717 003320 000406 BR 3S ;CONTINUE ALONG.
718 003322 013737 003730 003012 1S: BRW,TTST ;PREPARE NORMAL SCOPE ROUTINE
719 003330 013737 003732 003014 MOV BRX,TTST+2 ;LOCK NOT SELECTED, SET UP FOR NORMAL SCOPE LOOP
720 003336 012737 010060 001214 3S: MOV #CYCLE,RETURN ;START AT "CYCLE" FIND WHICH DEVICE TO TEST
721 003344 012737 000002 001236 4S: BIT #SW01,STRTSW ;IS TEST NO. SELECTED?
722 003352 001002 BNE 5S ;BR IF YES
723 003354 104402 005755 TYPE ,MR ;TYPE R
724 003360 012177 175630 5S: JMP @RETURN ;START TESTING
```



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725 ;END OF PASS
726 ;TYPE NAME OF TEST
727 ;UPDATE PASS COUNT
728 ;CHECK FOR EXIT TO ACT-11
729 ;RESTART TEST
730
731 003364 000005 ;EOP: RESET ;MAKE THE WORLD CLEAN AGAIN.
732 003365 005037 001234 CLR LSTERR ;CLEAR LAST ERROR PC
733 003372 105037 001325 CLR ERRFLG ;CLEAR ERROR FLAG
734 003376 005237 001230 INC PASCNT ;UPDATE PASS COUNT
735 003402 013777 001230 175570 MOV PASCNT,0DISP ;DISPLAY PASS COUNT
736 003410 104402 005733 TYPE ,REPASS ;TYPE END PASS
737 003414 104402 006072 TYPE ,MCSR1 ;TYPE CSR
738 003424 104411 003546 CNVRT ,XCSR ;SHOW IT
739 003424 104402 006100 TYPE ,MVCX ;TYPE VECTOR
740 003430 104411 003554 CNVRT ,XVEC ;SHOW IT
741 003431 104402 006106 TYPE ,XPASS ;TYPE PASSES
742 003440 104411 003562 CNVRT ,XERR ;SHOW IT
743 003444 104402 006117 TYPE ,MERR ;TYPE ERRORS
744 003450 104411 003570 CNVRT ,XERR ;SHOW IT
745 003454 013700 001322 MOV ,R0 ;GET POINTER TO PASS COUNT
746 003460 013720 001230 MOV PASCNT,(R0)+ ;STORE PASS COUNT FOR THIS DMC11
747 003464 013720 001232 MOV ERRCNT,(R0)+ ;STORE ERROR COUNT FOR THIS DMC11
748 003470 005337 001314 DEC SAVNUM ;ARE ALL DEVICES TESTED?
749 003474 001317 BNE RESTR ;BR IF NO.
750 003476 112737 000377 001327 MOV ,R0 ;SET THE QUICK VERIFY FLAG.
751 003504 013737 001310 001314 MOV DNUM,SAVNUM ;RESTORE THE COUNT
752 003512 013701 000042 MOV ,R1 ;CHECK FOR ACT-11 OR DDP
753 003516 001406 BEQ RESTR ;IF NOT, CONTINUE TESTING
754 003520 000005 RESTR ;STOP THE SHOW--CLEAR THE WORLD
755 003522
756 003522 004711 SENDAD: JSR PC,(R1)
757 003524 000240 NOP
758 003526 000240 NOP
759 003530 000240 NOP
760 003532 000240 NOP
761 003534 012737 010060 001214 RESTR: MOV #CYCLE,RETURN
762 003542 001317 010060 JMP CYCLE
763 003546 000001 XCSR: 1
764 003550 006 ,BYTE
765 003552 001404 DCSR 6,2
766 003554 000001 XVEC: 1
767 003556 004 ,BYTE
768 003560 001374 DMRVEC 4,2
769 003562 000001 XPASS: 1
770 003564 006 ,BYTE
771 003566 001230 PASCNT 6,2
772 003570 000001 XERR: 1
773 003572 006 ,BYTE
774 003574 001232 ERRCNT 6,2
775
776 ;SCOPE LOOP AND ITERATION HANDLER
777 ;-----
778
779 003576 034737 007606 .SCOPE: JSR PC,CKSWR ;CHECK FOR SOFT SWR
780 003602 010016 MOV R0,(SP) ;SAVE R0 ON THE STACK

```

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781 003604 032777 000000 175170 TTST: BIT #BIT14,0SWR ;"LOOP ON THIS TEST?"
782 003612 001307 BEO 10 ;BR IF NO. (IF LOCK SW01=1; THIS LOC =240)
783 003614 000437 BR 30 ;GOTO 30 (IF LOCK SW01=1; THIS LOC =240)
784 003616 005737 003734 TST DONE ;WAS TCSR DONE SET?
785 003622 001434 BEO 30 ;BR IF NO (LOCKED ON TEST)
786 003624 005037 003734 CLK DONE ;YES, CLEAR FLAG
787 003630 000415 BR 20 ;GO TO NEXT TEST
788 003632 032777 004000 175342 1S: BIT #SW11,0SWR ;DELETE ITERATION? (QUICK PASS)
789 003640 001011 BNE 20 ;BR IF YES
790 003642 005737 001327 TSTB OV,FLG ;HAVE PASSES BEECOMPLETED?
791 003646 001406 BEO 20 ;BR IF QUICK PASS.
792 003650 005237 001224 INC LPCNT ;UPDATE ITERATION COUNTER
793 003654 023737 001224 001222 CMP LPCNT,ICOUNT ;ARE ALL ITERATIONS DONE??
794 003662 001414 BLOS 30 ;BR IF NOT YET
795 003664 105037 001325 2S: CLR ERRFLG ;PREPARE FOR NEW TEST
796 003670 005037 001224 CLR LPCNT ;START ICOUNTER AT 0
797 003674 005037 001230 MOV ,R0 ;RESET ITERATIONS
798 003700 012737 000020 001222 MOV ,R0 ;GET NEXT TEST
799 003706 013737 001216 001214 MOV (SP),R0 ;POP R0 OFF OF THE STACK
800 003714 011600 POP2SP ;FARL AN "RTI"
801 003716 022626 MOV DCSR,R1 ;R1 CONTAINS BASE DMC ADDRESS
802 003720 013701 001404 JMP @RETURN ;GO DO THE TEST
803 003724 000177 175264 BRN: 1407
804 003730 001407 BRT: 437
805 003732 000437 DONE: 0
806 003734 000000

```

;CHECK FOR FREEZE ON CURRENT DATA

```

807
808
809
810
811 003736 004737 007606 .SCOPE1: JSR PC,CKSWR ;CHECK FOR SOFT SWR
812 003742 032777 001000 175232 BIT #SW09,0SWR ;IS SW09=1(SET)?
813 003750 001405 BEO 10 ;BR IF NOT SET.
814 003752 005737 001220 TST LOCK
815 003756 001402 BEO 10
816 003760 013716 001220 MOV LOCK,(SP) ;GOTO THE ADDRESS IN LOCK.
817 003764 000002 RTI ;GO BACK.

```

;TELETYPE OUTPUT ROUTINE

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818
819
820
821
822 003766 010546 .TYPE: MOV R5,(SP) ;SAVE R5 ON THE STACK.
823 003770 017605 MOV @2(SP),R5 ;GET ADDRESS OF MESSAGE.
824 003774 002766 000002 000002 ADD #2,(SP) ;POP OVER ADDRESS.
825 004002 005737 010316 TST SWFLG ;SOFT SWR MESSAGE?
826 004006 001004 BNE 10 ;IF YES TYPE IT OUT REGARDLESS OF SW12
827 004010 032777 010000 175164 BIT #SW12,0SWR ;INHIBIT ALL PRINT OUT??
828 004014 001012 BNE 30 ;BR IF NO PRINT OUT WANTED (SW12=1)
829 004020 105715 1S: ISTB (R5) ;IS NUMBER MINUS? (MSB=(BIT7))
830 004022 100002 BPL 20 ;BR IF NUMBER IS PLUS
831 004024 104402 005672 TYPE ,MCRLF ;TYPE A CR/LF!
832 004030 105777 175154 2S: TSTB *TPCSR ;TTY READY?
833 004034 100375 BPL 20 ;BR IF NO.
834 004036 112577 175150 MOVB (R5)+,@TPDBF ;PRINT CURRENT CHAR.
835 004042 001357 BNE 40 ;IF NOT ZERO KEEP PRINTING!
836 004044 001357

```

```

037 004046 000002 RTI ;GO HOME
038 ;-----
039
040 004050 010346 .INSTR1 MOV R3,-(SP) ;SAVE R3 ON STACK
041 004052 010446 MOV R4,-(SP) ;SAVE R4 ON STACK
042 004054 017637 000004 004072 MOV 04(SP),.MSG
043 004062 002706 000002 000004 ADD #2,4(SP)
044 004070 004002 .INSTR1 TYPE
045 004072 000000 .MSG: 0
046 004074 012704 007502 MOV #INBUF,R4
047 004100 012703 000007 MOV #7,R3
048 004104 005777 075074 18: TSTB #TKCSR
049 004110 000375 BPL 18
050 004112 017714 075070 MOV #TKDBR,(R4)
051 004116 002714 000200 BICB #200,(R4)
052 004122 022427 000015 CMPB (R4)+,#15
053 004126 001417 BEQ INSTR2
054 004130 005777 075054 28: TSTB #TPCSR
055 004134 000375 BPL 28
056 004136 017777 075044 075046 MOV #TKDBR,#TPDBR
057 004144 005303 DEC R3
058 004146 001356 BNE 18
059 004150 012604 MOV (SP)+,R4
060 004152 012603 MOV (SP)+,R3
061 004154 004002 005666 .INSTR1 TYPE ,NOM
062 004160 010346 MOV R3,-(SP)
063 004162 010446 MOV R4,-(SP)
064 004164 000741 BR .INSTR1
065 004166 012604 INSTR2: MOV (SP)+,R4 ;RESTORE R4
066 004170 012603 MOV (SP)+,R3 ;RESTORE R3
067 004172 000002 RTI
068
069 ;CONVERT ASCII STRING TO OCTAL
070 ;-----
071
072 004174 010546 .PARAM: MOV R5,-(SP)
073 004176 010446 MOV R4,-(SP)
074 004200 016005 000004 MOV 4(SP),R5
075 004203 012537 004364 MOV (R5)+,LOLIM
076 004210 012537 004366 MOV (R5)+,HILIM
077 004214 012537 004370 MOV (R5)+,DEVADR
078 004220 012537 004372 MOV #R5+,LOBITS
079 004224 012537 004373 MOV #R5+,ADRCNT
080 004230 010566 000004 MOV R5,4(SP)
081 004234 005005 PARAM1: CLR R5
082 004236 012704 007502 MOV #INBUF,R4
083 004242 022714 000015 CMPB #15,(R4)
084 004246 001420 BEQ PARERR
085 004250 021427 000060 18: CMPB (R4),#60
086 004254 002415 BLT PARERR
087 004256 021427 000067 CMPB (R4),#67
088 004262 003012 BGT PARERR
089 004264 022714 000060 BICB #60,(R4)
090 004270 022405 BICB (R4)+,R5
091 004272 022714 000015 CMPB #15,(R4)
092 004276 001406 BEQ LIMITS

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093 004300 006305 ASL R5
094 004302 006305 ASL R5
095 004304 006305 ASL R5
096 004306 000760 BR 18
097 004310 004404 PARERR: INSTR
098 004312 000750 BR PARAM1
099
100 ;TEST TO SEE IF NUMBER IS WITHIN LIMITS
101 ;-----
102
103 004314 020537 004366 LIMITS: CMP R5,HILIM
104 004320 001373 BHI PARERR
105 004322 020537 004364 CMP R5,LOLIM
106 004326 003770 BLO PARERR
107 004330 033705 004372 BTR LOBITS,R5
108 004334 001365 BNE PARERR
109
110 ;STORE NUMBER AT SPECIFIED ADDRESS
111
112 004336 013704 004370 18: MOV DEVADR,R4
113 004342 010524 MOV R5,(R4)+
114 004344 002705 000002 ADD #2,R5
115 004350 005337 004373 DECB ADRCNT
116 004354 001372 BNE 18
117 004356 012604 MOV (SP)+,R4
118 004360 012605 MOV (SP)+,R5
119 004362 000002 RTI
120 004364 000000 LOLIM: 0
121 004366 000000 HILIM: 0
122 004370 000000 DEVADR: 0
123 004372 000000 LOBITS: 0
124 004374 004373 ADRCNT:LOBITS+1
125
126 ;SAVE PC OF TEST THAT FAILED AND R0=R5
127 ;-----
128
129 004376 016037 000004 001276 .SAV05: MOV 4(SP),SAVPC ;SAVE R7 (PC)
130
131 ;SAVE R0=R5
132
133 004402 010537 001272 SV05: MOV R5,SAVR5 ;SAVE R5
134 004406 010437 001270 MOV R4,SAVR4 ;SAVE R4
135 004412 010337 001266 MOV R3,SAVR3 ;SAVE R3
136 004416 010237 001264 MOV R2,SAVR2 ;SAVE R2
137 004422 010137 001262 MOV R1,SAVR1 ;SAVE R1
138 004426 010037 001260 MOV R0,SAVR0 ;SAVE R0
139 004432 000002 RTI ;LEAVE.
140
141 ;RESTORE R0=R5
142
143 004434 013704 001260 .RES05: MOV SAVR0,R0 ;RESTORE R0
144 004436 013701 001262 MOV SAVR1,R1 ;RESTORE R1
145 004438 013702 001264 MOV SAVR2,R2 ;RESTORE R2
146 004440 013703 001266 MOV SAVR3,R3 ;RESTORE R3
147 004442 013704 001270 MOV SAVR4,R4 ;RESTORE R4
148 004444 013705 001272 MOV SAVR5,R5 ;RESTORE R5

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949 004464 000002 RTI ;LEAVE
950
951 ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
952 ;-----
953
954 004466 104402 005672 .CONVRT: TYPE ;MCLRF
955 004472 010006 .CONVRT: MOV R0,-(SP)
956 004474 010146 MOV R1,-(SP)
957 004476 010346 MOV R3,-(SP)
958 004500 010446 MOV R4,-(SP)
959 004502 010546 MOV R5,-(SP)
960 004504 017001 000012 MOV #12(SP),R1
961 004510 002766 000002 000012 ADD #2,12(SP)
962 004516 012137 004710 MOV (R1)+,WRDCNT
963 004522 112137 004712 18: MOVB (R1)+,CHRCNT
964 004526 112137 004713 MOVB (R1)+,SPACNT
965 004532 013137 004714 MOV #0(R1)+,BINWRD
966 004536 122737 000003 004712 CMPB #3,CHRCNT
967 004544 001003 BNE Z8
968 004546 002737 177400 004714 BIC #177400,BINWRD
969 004554 013704 004714 28: MOV BINWRD,R4
970 004560 113705 004712 MOVB CHRCNT,R5
971 004564 012700 001416 MOV #TEMP,R0
972 004570 010403 36: MOV R4,R3
973 004572 042703 177770 BIC #177770,R3
974 004576 062703 000000 ADD #060,R3
975 004602 110320 MOVB R3,(R0)+
976 004604 000241 CLC
977 004606 006004 ROR R4
978 004610 000241 CLC
979 004612 006004 ROR R4
980 004614 000241 CLC
981 004616 006004 ROR R4
982 004620 005305 DEC R5
983 004622 001362 BNE Z4
984 004624 012703 007544 MOV #MDATA,R3
985 004630 114023 48: MOVB -(R0),(R3)+
986 004632 105337 004712 DECB CHRCNT
987 004636 001374 BNE Z6
988 004640 105737 004713 .TSTB SPACNT
989 004644 001405 BEQ Z6
990 004646 112723 000040 58: MOVB #040,(R3)+
991 004652 105337 004713 DECB SPACNT
992 004656 001373 BNE Z6
993 004660 105013 68: CLRB (R3)
994 004662 104402 007544 TYPE #MDATA
995 004666 005337 004710 DEC WRDCNT
996 004672 001313 BNE Z6
997 004674 012605 MOV (SP)+,R5
998 004676 012604 MOV (SP)+,R4
999 004700 012603 MOV (SP)+,R3
1000 004702 012601 MOV (SP)+,R1
1001 004704 012600 MOV (SP)+,R0
1002 004706 000032 RTI
1003 004710 000000 WRDCNT: 0
1004 004712 000000 CHRCNT: 0

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1005 SPACNT=CHRCNT+1
1006 004714 000000 BINWRD: 0
1007
1008
1009 ;TRAP DISPATCH SERVICE
1010 ;ARGUMENT OF TRAP IS EXTRACTED
1011 ;AND USED AS OFFSET TO OBTAIN POINTER
1012 ;TO SELECTED SUBROUTINE
1013
1014 004716 011646 .TRPSR: MOV (SP),-(SP) ;GET PC OF RETURN
1015 004720 102716 000002 SUB #2,(SP) ;PC OF TRAP
1016 004724 017616 000000 MOV #0(SP),(SP) ;GET TRP
1017 004730 006316 TRPOK: ASL (SP) ;MULTIPLY TRAP ARG BY 2
1018 004732 042716 177001 BIC #177001,(SP) ;CLEAR UNWANTED BITS
1019 004736 002716 001330 ADD #,TRPTAB,(SP) ;POINTER TO SUBROUTINE ADDRESS
1020 004742 017616 000000 MOV #0(SP),(SP) ;SUBROUTINE ADDRESS
1021 004746 000136 JMP #0(SP)+ ;GO TO SUBROUTINE
1022
1023 ;ERROR HANDLER
1024 ;-----
1025
1026 004750 004737 007606 .HLT: JSR PC,CKSWR ;CHECK FOR SOFT SWR
1027 004754 032777 010000 174220 BIT #SW12,0SWR ;BELL ON ERROR?
1028 004762 001406 BEQ ;BFR IF NO BELL
1029 004764 105777 174220 .TSTB #TPCSR ;TTY READY.
1030 004770 100003 ASL ;DON'T WAIT IF TTY NOT READY.
1031 004772 112777 000207 174212 MOVB #207,0TPD0R ;PUSH A BELL AT THE TTY.
1032 005000 032777 020000 174174 XBX: BIT #SW13,0SWR ;DELETE ERROR PRINT OUT?
1033 005006 001105 BNE HALTS ;BFR IF NO PRINT OUT WANTED.
1034 005010 021637 001234 CMP (SP),LSTERR ;WAS THIS ERROR FOUND LAST TIME?
1035 005014 001404 BEQ Z8 ;BFR IF YES
1036 005016 011637 001234 MOV (SP),LSTERR ;RECORD BEING HERE
1037 005022 105037 001325 CLRB ERRFLG ;PREPARE HEADER
1038 005026 104406 19: SAV05 ;SAVE ALL PHOC REGISTERS
1039 005030 011005 MOV (SP),R5 ;GET THE PC OF ERROR
1040 005032 102705 000002 SUB #2,R5 ;GET ADDRESS OF TRAP CALL
1041 005036 011504 MOV (R5),R4 ;GET HLT INSTRUCTION
1042 005040 000304 ASL R4 ;MULT BY 100
1043 005042 001504 ADD (R5),R4 ;DOUBLE IT
1044 005044 006404 ASL R4 ;MULT AGAIN
1045 005046 042704 177001 BIC #177001,R4 ;CLEAR JUNK
1046 005052 002704 027602 ADD #,ERRTAB,R4 ;GET POINTER
1047 005056 012437 005172 MOV (R4)+,ERRMSG ;GET ERROR MESSAGE
1048 005062 012437 005204 MOV (R4)+,DATAHD ;GET DATA HEADER
1049 005066 011437 005216 MOV (R4),DATABP ;GET DATA TABLE
1050 005072 105737 001325 .TSTB ERRFLG ;TYPE HEADREER
1051 005076 001403 BEQ TIPMSG ;BFR IF YES
1052 005100 005737 005216 .TST DATABP ;DOES DATA TABLE EXIST?
1053 005104 001403 BNE TYPDAT ;BFR IF YES.
1054 005106 104402 005672 TYPMSG: TYPE ;MCLRF
1055 005112 104402 005672 TYPE ;MCLRF
1056 005116 005737 001220 IST LOCK
1057 005122 001102 BEQ Z8
1058 005124 104402 000142 TYPE ;MASTEK
1059 005130 104402 000130 TYPE ;*TSTN
1060 005134 101111 005330 CNVRT ;,X1STN ;SHOW 11

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1061 005140 104402 006217 TYPE ,MERRPC ;TYPE PC.
1062 005144 104411 005322 CNVRT ,ERTAB0 ;SHOW IT
1063 005150 104402 005672 TYPE ,MCRFLF ;GIVE A CR/LF
1064 005154 112737 177777 001320 MOV0B #1,ERRFLG ;NO MORE HEADER UNLESS NO DATA TABLE.
1065 005162 005737 005172 TST ERRMSG ;IS THERE AN ERROR MESSAGE?
1066 005166 104402 BEQ WKKU,FM ;BR IF NO.
1067 005170 104402 TYPE ;TYPE
1068 005172 000000 ERRMSG: 0 ; ERROR MESSAGE
1069 005174 WKKU,FM: ;
1070 005174 005737 005204 TST DATAHD ;DATA HEADER?
1071 005200 001402 BEQ TYPDAT ;BR IF NO
1072 005202 104402 TYPE ;TYPE
1073 005204 000000 DATAHD: 0 ; DATA HEADER
1074 005206 005737 005216 TYPDAT: TST DATABP ;DATA TABLE?
1075 005212 001402 BEQ RESREG ;BR IF NO.
1076 005214 104410 CNVRT ;SHOW
1077 005216 000000 DATABP: 0 ; DATA TABLE
1078 005220 104407 RESREG: RES05 ;RESTORE PROC REGISTERS
1079 005222 322737 003522 000042 HALTS: CMP #ENDAD,0#42 ;IF ACT=11 AUTOMATIC MODE, HALTI!
1080 005230 001403 BEQ 10 ;
1081 005232 005777 173744 TST 0SWR ;HALT ON ERROR?
1082 005236 100005 SPL EXITER ;BR IF NO HALT ON ERROR
1083 005240 010046 10: PUSHRO ;SAVE RO
1084 005242 000000 MOV 2(SP),RO ;SHOW ERROR PC IN DATA LIGHTS
1085 005246 000000 HALT ;HALT
1086 005250 012000 POPPR0 ;GET RO
1087 005252 005237 001232 EXITER: INC ERRCNT ;UPDATE ERROR COUNT
1088 005256 032777 000400 173716 BIT #SW00,0SWR ;GOTO TOP OF TEST?
1089 005264 001007 ONE 10 ;BR IF YES
1090 005266 032777 002000 173706 BIT #SW10,0SWR ;GOTO NEXT TEST?
1091 005274 001411 BEQ 20 ;BR IF NO
1092 005276 013737 001216 001214 10: MOV NEXT,RETURN ;SET FOR NEXT TEST
1093 005300 012706 001200 10: MOV #STACK,SP ;RESET SP
1094 005310 013701 001404 MOV DMCSR,R1 ;SET UP R1
1095 005314 000177 173674 JMP 0RETURN ;GOTO SPECIFIED TEST
1096 005320 000002 20: RTI ;RETURN
1097 005322 000001 ERTAB0: 1
1098 005324 006 .BYTE 6,2
1099 005326 001276 SAVPC
1100 005330 000001 XTSTN: 1
1101 005332 003 .BYTE 3,2
1102 005334 001226 TSTNO
;ENTER HERE ON POWER FAILURE
;-----
1103
1104
1105
1106
1107 005336 .PFAIL:
1108 005336 012737 005350 000024 MOV #RESTART,24 ;SET UP FOR POWER UP TRAP
1109 005344 000000 HALT ;HALT ON POWER DOWN NORMAL
1110 005346 000777 BR .
1111
1112 ;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
1113
1114 005350 RESTART:
1115 005350 012737 005336 000024 MOV #.PFAIL,24 ;SET UP FOR POWER FAILURE
1116 005356 012706 001200 MOV #STACK,SP ;RESET THE STACK POINTER

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1117 005362 013701 001404 MOV DMCSR,R1 ;RESTORE R1
1118 005366 005737 001416 CLR TEMP ;READY FOR TIMER
1119 005372 005237 001416 INC TEMP ;PLUS ONE TO THE TIMER!
1120 005376 001375 BNE -4 ;BR IF MORE TO GO
1121 005400 104402 005675 TYPE ,MPFAIL ;TYPE THE MESSAGE
1122 005404 104411 005430 CNVRT ,PFTAB ;TELL WHAT TEST TO RETURN TO.
1123 005410 105037 001325 CLR0 ERRFLG ;START CLEAN
1124 005414 005037 001234 CLR LSTERR ;*****
1125 005420 005011 CLR (R1) ;CLEAR MAINT BITS
1126 005422 104412 MSTCLR ;START CLEAN UP OF DEVICE
1127 005424 000177 173564 JMP 0RETURN ;START DOING THAT TEST AGAIN.
1128 005430 000001 PFTAB: 1
1129 005432 003 .BYTE 3,2
1130 005434 001226 TSTNO
1131
1132 005436 .DELAY:
1133 005436 012777 000020 173746 MOV #20,0DMP04
1134 005444 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1135 005446 121111 121111 10: ;POKE CLOCK DELAY BIT
1136 005450 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1137 005452 121224 121224 10: ;PORTA_IBUS*11
1138 005454 032777 000020 173730 BIT #BIT4,0DMP04 ;IS CLOCK BIT SET?
1139 005462 001772 BEQ 10 ;BR IF NO
1140 005464 000002 RTI
1141
1142 .MSTCLR:
1143 005466 152777 000100 173712 BISB #BIT6,0DMCSRH ;SET MASTER CLEAR
1144 005474 142777 000300 173704 BICB #BIT6,BIT7,0DMCSRH ;CLEAR MASTER CLEAR AND RUN
1145 005502 000002 RTI ;RETURN
1146
1147 .ROMCLK:
1148 005504 152777 000002 173674 BISB #BIT1,0DMCSRH ;SET ROM1
1149 005512 013677 173676 MOV 0(SP)+,0DMP06 ;LOAD INSTRUCTION IN SEL6
1150 005516 002746 000002 ADD #2,-(SP) ;ADJUST STACK
1151 005522 032777 000100 173452 BIT #SW00,0SWR ;HALT IF SW06 =1
1152 005530 001401 BEQ 10 ;BR IF SW06 =0
1153 005532 000000 HALT ;HALT BEFORE CLOCKING INSTRUCTION
1154 005534 152777 000003 173644 10: BISB #BIT1,BIT0,0DMCSRH ;CLOCK INSTRUCTION
1155 005542 142777 000007 173636 BICB #BIT2,BIT1,BIT0,0DMCSRH ;CLEAR ROM0, ROM1, STEP
1156 005550 000002 RTI
1157
1158 .DATACLK:
1159 005552 013637 001416 MOV 0(SP)+,TEMP ;PUT TICK COUNT IN TEMP
1160 005556 002746 000002 ADD #2,-(SP) ;ADJUST STACK
1161 005562 152777 000020 173616 10: BISB #BIT4,0DMCSRH ;SET STEP LD
1162 005570 027777 173610 173606 CMP 0DMCSR,0DMCSR ;WASTE TIME
1163 005576 142777 000020 173602 BICB #BIT4,0DMCSRH ;CLEAR STEP LD
1164 005604 005737 001416 DEC TEMP ;DEC TICK COUNT
1165 005610 001364 BNE 10 ;BR IF NOT DONE
1166 005612 000002 RTI ;RETURN
1167
1168 005614 000001 30: .BLKW 1
1169
1170 .TIMER:
1171 005616 013637 001416 MOV 0(SP)+,TEMP ;MOVE COUNT TO TEMP
1172 005622 002746 000002 ADD #2,-(SP) ;ADJUST STACK

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1173 005626 104114 1S: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1174 005626 104114 ;PORT4_IBUS* REG11
1175 005630 021364 BIT ;IS PGM CLOCK BIT CLEAR?
1176 005632 032777 000002 173552 BEQ #2,0DMP04 ;BR IF YES
1177 005640 001772 2S:
1178 005642 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1179 005644 021364 ;PORT4_IBUS* REG11
1180 005646 032777 000002 173536 BIT #2,0DMP04 ;IS PGM CLOCK BIT SET?
1181 005651 001372 28 ;BR IF YES
1182 005651 001372 DEC TEMP ;DEC COUNT
1183 005656 005337 001416 BNE ;BR IF NOT DONE
1184 005662 001361 RTI ;RETURN
1185 005664 000002
1186
1187 005666 020040 000077 MQM: .ASCIZ / ?/
(2) 005672 005015 000 MCRFB: .ASCIZ <15><12>
(2) 005675 377 053520 020122 MFAIL: .ASCIZ <377>/PWR FAILED, RESTART AT TEST /
(2) 005733 377 047105 020104 MFPASS: .ASCIZ <377>/END PASS DZDMG /
(2) 005755 377 000122 MR: .ASCIZ <377>/R/
(2) 005760 047377 020117 042504 MERR2: .ASCIZ <377>/NO DEVICES PRESENT./
(2) 006005 377 047111 052523 MERR3: .ASCIZ <377>/INSUFFICIENT DATA!/
(2) 006031 377 042524 052123 HTSTPC: .ASCIZ <377>/TEST PC-/
(2) 006043 377 047514 045503 WLOCK: .ASCIZ <377>/LOCK ON SELECTED TEST/
(2) 006072 051503 035122 000040 MCSR: .ASCIZ /CSR: /
(2) 006100 042526 035103 000040 MVECI: .ASCIZ /VEC: /
(2) 006106 040520 051523 051505 MPASSX: .ASCIZ /PASSES: /
(2) 006117 105 051122 051117 MERRX: .ASCIZ /ERRORS: /
(2) 006130 042524 052123 047040 MTEST: .ASCIZ /TEST NO: /
(2) 006142 000052 MSTEK: .ASCIZ /*/
(2) 006144 051777 052105 051440 MNEW: .ASCIZ <377>/SET SWITCH REG TO DMC11'S DESIRED ACTIVE./
(2) 006217 120 035103 000040 MERRPC: .ASCIZ /PC: /
(2) 006224 020212 020040 020040 XHEAD: .ASCIZ <212>/
(2) 006263 377 020040 020040 .ASCIZ <377>/
(2) 006322 020212 050040 020103 .ASCIZ <212>/ PC CSR STAT1 STAT2 STAT3/
(2) 006374 026777 026455 026455 .ASCIZ <377>/-----
(2) 006450 044377 053517 040440 NUM: .ASCIZ <377>/HOW MANY DMC11'S TO BE TESTED?/
(2) 006510 041777 051123 040440 CSR: .ASCIZ <377>/CSR ADDRESS?/
(2) 006526 053377 041505 047524 VEC: .ASCIZ <377>/VECTOR ADDRESS?/
(2) 006547 377 051102 050040 PRIO: .ASCIZ <377>/BR PRIORITY LEVEL? (4,5,6,7)?/
(2) 006606 044777 020106 046504 CRAM: .ASCIZ <377>/IF DMC HAS CRAM (M8204) TYPE *Y*, IF CROM (M8200) TYPE *N*
(2) 006704 053777 044510 044103 MODU: .ASCIZ <377>/WHICH LINE UNIT? (DDCMP LINE #)?/
(2) 007016 051777 044527 041524 LINE: .ASCIZ <377>/SWITCH PAC#1 (DM873 BOOT ADD)?/
(2) 007054 051777 044527 041524 B4: .ASCIZ <377>/SWITCH PAC#2 (DM873 BOOT ADD)?/
(2) 007114 044777 020123 044124 CONN: .ASCIZ <377>/IS THE LOOP BACK CONNECTOR ON?/
(2) 007154 047377 020117 042504 NOACT: .ASCIZ <377>/NO DEVICES ARE SELECTED/
(2) 007205 377 051412 051127 SWMES: .ASCIZ <377><12>/SWR= /
(2) 007215 116 053505 020077 /NEW? /
(2) 007223 377 042377 041515 CONERR: .ASCIZ <377><377>/DMC11 FOUND AT NON-STANDARD ADDRESS PC: /
(2) 007277 377 054105 042520 CNERR: .ASCIZ <377>/EXPECTED FOUND/
(2) 007320 024040 046504 024503 DMCN: .ASCIZ / (DMC) /
(2) 007330 024040 046513 024503 KMCN: .ASCIZ / (RMC) /
(2) 007340 042377 041515 030461 SPEED: .ASCIZ <377>/DMC11-AR(REMOTE,LOW SPEED) OR DMC11-AL(LOCAL,HIGH SPEED) T
(2)
(2) 007454 000005 .EVEN
1188 007456 006 003 XSTATQ: 5
1189 007460 001246 .BYTE 6,3
TEMP1

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1190 007462 006 003 .BYTE 6,3
1191 007464 001250 TEMP2
1192 007466 006 003 .BYTE 6,3
1193 007470 001252 TEMP3
1194 007472 006 003 .BYTE 6,3
1195 007474 001254 TEMP4
1196 007476 006 002 .BYTE 6,2
1197 007500 001256 TEMP5
1198
1199 .EVEN
1200 ;BUFFERS FOR INPUT-OUTPUT
1201
1202 007502 000000 INBUF: 0
1203 007544 000000 ., +40
1204 007544 000000 MDATA: 0
1205 007600 ., +40
1206
1207
1208 ;ROUTINE USED TO CHANGE SOFTWARE SWITCH
1209 ;REGISTER USING THE CONSOLE TERMINAL
1210 ;-----
1211
1212 007606 022737 000176 001202 CKSWR: CMP #SWREG,SWR ;IS THE SOFT SWR BEING USED?
1213 007614 001077 BNE CKSWR5 ;BR IF NO
1214 007616 105777 171362 TSTB @TKCSR ;IS DONE SET?
1215 007622 100003 BPL 28 ;GO ON IF NOT SET
1216 007624 012737 177777 003734 MOV #=1,DONE ;IF DONE SET, SET FLAG
1217 007632 022777 000007 171346 2S: CMP #7,@TKDBR ;WAS CTRL G TYPED? (7 BIT ASCII)
1218 007640 001004 BEQ 16 ;BR IF YES
1219 007642 022777 000207 171336 CMP #207,@TKDBR ;WAS CTRL G TYPED? (8 BIT ASCII)
1220 007650 001061 BNE CKSWR5 ;BR IF NO
1221 007652 010246 1S: MOV R2, -(SP) ;STORE R2
1222 007654 010346 MOV R3, -(SP) ;STORE R3
1223 007656 010446 MOV R4, -(SP) ;STORE R4
1224 007660 012737 177777 010016 MOV #=1,SWFLG ;SET SOFT TYPE OUT FLAG
1225 007666 005002 CKSWR1: CLR R2 ;CLEAR NEW SWR CONTENTS
1226 007670 012704 MOV #=1,R4 ;SET FLAG TO ALL UNES
1227 007674 104402 007205 TYPE :SWRES ;TYPE "SWR="
1228 007700 104411 CKSWR2: CNVRT ;TYPE OUT PRESENT CONTENTS
1229 007702 010052 SOFTSW ;OF SOFT SWITCH REGISTER
1230 007704 104402 007215 CKSWR3: TYPE ,SWMES1 ;TYPE "NEW? "
1231 007710 004737 010020 CKSWR4: JSR PC,INCHAR ;GET RESPONSE
1232 007714 022703 000015 CMP #15,R3 ;WAS IT A CH?
1233 007720 001424 BEQ 56 ;BR IF YES
1234 007722 022703 000012 CMP #12,R3 ;WAS IT A LF?
1235 007726 001416 BEQ 46 ;BR IF YES
1236 007730 022703 000025 CMP #25,R3 ;WAS IT CTRL U?
1237 007734 001754 BEQ CKSWR1 ;BR IF YES(START OVER)
1238 007736 022703 000007 CMP #7,R3 ;IF CTRL G GET NEXT CHAR
1239 007742 001762 BEQ CKSWR4
1240 007744 005004 CLR R4 ;IT MUST BE A DIGIT SO CLR FLAG
1241 007746 042703 177770 BIC #17770,R3 ;ONLY 0-7 ARE LEGAL SO MASK OFF BITS
1242 007752 006302 ASL R2 ;SHIFT R2 3 TIMES
1243 007754 006302 ASL R2
1244 007756 006302 ASL R2
1245 007760 006302 BLS R3,R2 ;ADD LAST DIGIT

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1246 007762 000752          BR      CKSWR4      ;GET NEXT CHARACTER
1247 007764 012760 002002 000000 48:  MOV      *.START,6(SP) ;LF WAS TYPED SO GO TO START
1248 007772 005704          55:  TST      R4          ;IS FLAG CLEAR?
1249 007774 001002          BNE     66          ;IF NOT DON'T CHANGE SOFT SWR
1250 007776 010277 171200  MOV      R2,0SWR    ;IF YES THEN WRITE NEW CONTENTS TO SOFT SWR
1251 010002 005037 010016 68:  CLR      SWFLG     ;CLEAR TYPEOUT FLAG
1252 010006 012004          MOV      (SP)+,R4   ;RESTORE R4
1253 010010 012003          MOV      (SP)+,R3   ;RESTORE R3
1254 010012 012002          MOV      (SP)+,R2   ;RESTORE R2
1255 010014 000207          CKSWR5: RTS      PC      ;RETURN
1256
1257 010016 000000          SWFLG:  0
1258
1259 010020 105777 171160  INCHAR: TSTB     0TKCSR
1260 010024 100375          BPL     -4
1261 010026 017703 171154  MOV      0TKDBR,R3
1262 010032 105777 171152  TSTB     0TPCSR
1263 010036 100375          BPL     -4
1264 010040 010377 171146  MOV      R3,0TPDBR
1265 010044 042703 000200  BIC     0BIT7,R3
1266 010050 000207          RTS      PC
1267
1268 010052 000001          SOFTSW: 1
1269 010054 006 002      .BYTE 6,2
1270 010056 000176          SWREG

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1271
1272
1273
1274
1275
1276
1277
1278
1279
1280 010060 005737 001306  CYCLE: TST      DMACTV   ;ARE ANY DMC11'S TO BE TESTED?
1281 010064 001001          BNE     18          ;BR IF OK.
1282 010066 104402 007154          TYPE     ,NOACT    ;NO DMC11'S SELECTED!!
1283 010072 000000          HALT     ;STOP THE SHOW.
1284 010074 000776          BR      -2          ;DISQUALIFY COM1. SW.
1285 010076 000241          15:  CLC      ;CLEAR PROC. CARRY BIT.
1286 010100 006137 001316  ROL      ;UPDATE POINTER
1287 010104 005537 001316  ADC      ;CATCH CARRY FROM RUN
1288 010110 002737 000004 001322  ADD      #4,MILK    ;UPDATE POINTER
1289 010116 002737 000010 001320  ADD      #10,CREAM  ;UPDATE ADDRESS POINTER.
1290 010124 022737 001700 001320  CMP      #DM.MAP+200,CREAM
1291 010132 001006          BNE     28          ;KEEP GOING; NOT ALL TESTED FOR.
1292 010134 012737 001500 001320  MOV      #DM.MAP,CREAM ;RESET ADDRESS POINTER.
1293 010142 012737 001702 001322  MOV      #CNT.MAP,MILK ;RESET PASS COUNT POINTER
1294 010150 003737 001316 001306  25:  BIT      RUN,DMACTV ;IS THIS ONE ACTIVE?
1295 010156 001747          BEQ     18          ;BR IF NO
1296 010160 013700 001320  MOV      CREAM,R0    ;GET ADDRESS POINTER
1297 010164 013702 001322  MOV      MILK,R2     ;GET PASS COUNT POINTER
1298 010170 012037 001404  MOV      (R0)+,DMCSR ;LOAD SYSTEM CTRL. REG
1299 010174 011037 001374  MOV      (R0),DMRVEC ;LOAD VECTOR
1300 010200 042737 177000 001374  BIC     #177000,DMRVEC ;CLEAR UNWANTED BITS
1301 010206 012037 001366  MOV      (R0)+,STAT1 ;LOAD STAT1
1302 010212 012037 001370  MOV      (R0)+,STAT2 ;LOAD STAT2
1303 010216 012037 001372  MOV      (R0)+,STAT3 ;LOAD STAT3
1304 010222 012237 001230  MOV      (R2)+,PASCNT ;LOAD PASS COUNT
1305 010226 012237 001232  MOV      (R2)+,ERRCNT ;LOAD ERROR COUNT
1306 010232 012700 000002  MOV      #2,R0      ;SAVE CORE THIS WAY!
1307 010236 013737 001404 001406  MOV      DMCSR,DMCSRH
1308 010244 005237 001406  INC      DMCSRH
1309 010250 013737 001406 001410  MOV      DMCSRH,DMCTL
1310 010256 005237 001410  INC      DMCTL
1311 010262 013737 001410 001412  MOV      DMCTL,DMP04
1312 010270 000037 001412  ADD      R0,DMP04
1313 010274 013737 001412 001414  MOV      DMP04,DMP06
1314 010302 000037 001414  ADD      R0,DMP06
1315
1316 010306 013737 001374 001376  MOV      DMRVEC,DMRVLV ;PTY LVL
1317 010314 000037 001376  ADD      R0,DMRVLV
1318 010320 013737 001376 001400  MOV      DMRVLV,DMTVEC ;TA VEC
1319 010326 000037 001400  ADD      R0,DMTVEC
1320 010332 013737 001400 001402  MOV      DMTVEC,DMTLVL ;TX LVL
1321 010340 000037 001402  ADD      R0,DMTLVL
1322
1323 010344 022737 000002 001236  BIT      #SW01,STRISM ;IS TEST NO. SELECTED
1324 010352 001450  BEQ     76          ;BR IF NO
1325 010354
1326 010354 005737 000042          45:  TST      #042      ;RUNNING IN AUTO MODE?

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1327 010360 001045      BNE 78 ;BR IF YES
1328 010362 104402      TYPE ,MCRLF
1329 010366 104403      INSTR ;GET TEST NO.
1330 010370 000130      MTSTN
1331 010372 104405      PARAM
1332 010374 000001      I
1333 010376 001000      1000
1334 010400 001226      TSTNO
1335 010402 000      .BYTE 0
1336 010403 001      .BYTE 1
1337 010404 012700 022322      MOV #TST1,R0
1338 010410 022710      CMP (PC)+,(R0) ;CMP FIRST WORD TO 12737
1339 010412 012737      MOV (PC)+,0(PC)+
1340 010414 001020      BNE 68 ;BR IF NOT SAME
1341 010416 023760 001226 000002      CMP TSTNO,2(R0) ;DOES TSTNO MATCH?
1342 010424 001014      BNE 68 ;BR IF NO
1343 010426 022760 001226 000004      CMP #TSTNO,4(R0) ;IS LAST WORD OK?
1344 010434 001010      BNE 68 ;BR IF NO
1345 010436 010037 001214      MOV R0,RETURN ;IT IS A LEGAL TEST SO DO IT
1346 010442 104402 005755      TYPE ,MR
1347 010446 042737 000002 001236      BIC #S01,STRSW
1348 010451 000412      BR 88
1349 010456 005720      68: TST (R0)+ ;POP R0
1350 010460 020027 026472      CMP R0,#TLAST+10 ;AT END YET?
1351 010464 001351      BNE 58 ;BR IF NO
1352 010466 104402 005666      TYPE ,MQM ;YES ILLEGAL TEST NO.
1353 010472 000730      BR 48 ;TRY AGAIN
1354
1355 010474 012737 022322 001214      78: MOV #TST1,RETURN ;PREPARE RETURN ADDRESS
1356 010502 013701 001404      88: MOV DMC SR,R1 ;R1 = BASE DMC11 ADDRESS
1357 010506 000177 170502      JMP 0RETURN ;GO START TESTING.
1358
1359
1360 ;ROUTINE USED TO "AUTO SIZE" THE DMC11
1361 ;CSR AND VECTOR.
1362 ;NOTE: THE CSR MAY BE ANY WHERE IN THE FLOATING
1363 ; ADDRESS RANGE (160000:164000)
1364 ; AND THE VECTOR MAY BE ANY WHERE IN THE
1365 ; FLOATING VECTOR RANGE (300:770)
1366 ;
1367 ;
1368 AUTO_SIZE:
1369 010512 000005      RESET ;INSURE A BUS INIT.
1370 010514 012702 001500      CSRMAP: MOV #DM_MAP,R2 ;LOAD MAP POINTER.
1371 010520 005022      18: CLR (R2)+ ;ZERO ENTIRE MAP
1372 010522 022702 001700      CMP #DM_END,R2 ;ALL DONE?
1373 010526 001374      BNE 18 ;BR IF NO
1374 010530 005037 001310      CLR DMNUM ;SET OCTAL NUMBER OF DMC11'S TO 0
1375 010534 012702 001500      MOV #DM_MAP,R2 ;R2 POINTS TO DMC MAP
1376 010540 005037 001306      CLR DMACTV ;CLEAR ACTIVE
1377 010544 032737 000001 001236      BIT #S00,STRSW ;QUESTIONS?
1378 010552 001002      BNE ,+6 ;BR IF YES
1379 010554 000137 011252      JMP 78 ;IF NO SKIP QUESTIONS
1380 010560 012737 000001 001256      MOV #1,TEMP5 ;START WITH 1
1381 010566 104403      INSTR
1382 010570 066450      NUM
  
```

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1383 010572 104405      PARAM
1384 010574 000001      I
1385 010576 000020      16,
1386 010600 001252      TEMP3
1387 010602 000      .BYTE 0
1388 010603 001      .BYTE 1
1389 010604 013737 001252 001310      MOV TEMP3,DMNUM ;DMNUM = HOW MANY
1390 010612 104402 005672      128: TYPE ,MCRLF
1391 010616 104410      CONVRT
1392 010620 012002      WHICH ;TYPE WHICH DMC IS BEING DONE
1393 010622 005237 001256      INC TEMP5 ;TEMP5 IS WHICH DMC
1394 010626 104403      INSTR
1395 010630 006510      CSR
1396 010632 104405      PARAM
1397 010634 160000      160000
1398 010636 164000      164000
1399 010640 001254      TEMP4
1400 010642 000      .BYTE 0
1401 010643 001      .BYTE 1
1402 010644 013722 001254      MOV TEMP4,(R2)+ ;STORE CSR IN MAP
1403 010650 104403      INSTR
1404 010652 006526      VEC
1405 010654 104405      PARAM
1406 010656 000000      0
1407 010660 000776      776
1408 010662 001254      TEMP4
1409 010664 000      .BYTE 0
1410 010665 001      .BYTE 1
1411 010666 013712 001254      MOV TEMP4,(R2) ;STORE VECTOR IN MAP
1412 010672 104402      108: TYPE
1413 010674 006547      PRIO ;ASK WHAT BR LEVEL
1414 010676 004737 012266      JSR PC,INTTY ;GET RESPONSE
1415 010702 022703 000024      CMP #24,R3 ;
1416 010706 101014      BHI 508 ;BR IF LESS THAN 4
1417 010710 022703 000027      CMP #27,R3 ;
1418 010714 103411      BLO 508 ;BR IF GREATER THAN 7
1419 010716 012704 000011      MOV #11,R4 ;R4 = NUMBER OF SHIFTS
1420 010722 006303      ASL R3 ;SHIFT R3 LEFT
1421 010724 005304      DEC R3 ;DEC SHIFT COUNT
1422 010726 001375      BNE ,+4 ;BR IF NOT DONE
1423 010730 004703 170777      BIC #170777,R3 ;BIC UNWANTED BITS
1424 010731 0050312      BIS R3,(R2) ;PUT BR LEVEL IN STATUS MAP
1425 010736 000403      BR 88 ;CONTINUE
1426 010740 104402      506: TYPE
1427 010742 005666      MQM ;RESPONSE IS OUT OF LIMITS
1428 010744 000752      BR 108 ;TRY AGAIN
1429 010746 104402      88: TYPE
1430 010750 006606      CRAM ;DOES DMC HAVE CRAM?
1431 010752 004737 012266      JSR PC,INTTY ;GET REPLY
1432 010756 022703 000131      CMP #131,R3 ;
1433 010762 001027      BEQ 98 ;YES
1434 010764 022703 000116      CMP #116,R3 ;NO
1435 010770 101403      BEQ 408 ;NOT A Y OR N
1436 010772 104402      TYPE
1437 010774 005666      MQM ;TYPE "7"
1438 010776 006763      BR 88 ;ASK AGAIN
  
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1439 011000 104402 406: TYPE ;  
1440 011002 007340 SPEED ;  
1441 011004 004737 012266 PC,INTTY ;DMC11-AR OR DMC11-AL7  
1442 011010 022703 000122 JSR ;GET RESPONSE  
1443 011014 001414 CMP #12,R3 ;IS IT R  
1444 011016 022733 000114 BEQ 160 ;BR IF REMOTE  
1445 011022 001403 CMP #14,R3 ;IS IT L  
1446 011024 104402 BEQ 418 ;BR IF LOCAL  
1447 011026 005666 TYPE ;  
1448 011030 000763 MOM ;  
1449 011032 052762 000002 000004 418: BR 406 ;TRY AGAIN  
1450 011040 000402 BIS #BIT1,4(R2) ;SET BIT1 IN STAT3  
1451 011042 052712 100000 BR 160 ;CONTINUE  
1452 011046 104402 168: BIS #BIT15,(R2) ;SET BIT 15 IF CRAM  
1453 011050 006704 TYPE ;  
1454 011052 004737 012266 MODU ;ASK WHICH LINE UNIT  
1455 011056 022703 000021 JSR #21,R3 ;GET REPLY  
1456 011062 001417 BEQ 308 ;"1"  
1457 011064 022703 000022 CMP #22,R3 ;"2"  
1458 011070 001412 BEQ 316 ;"3"  
1459 011072 022703 000116 CMP #16,R3 ;"N"  
1460 011076 001403 BEQ 320 ;  
1461 011100 104402 TYPE ;  
1462 011102 005666 MOM ;IF NOT A 1,2 OR N TYPE "7"  
1463 011104 000760 BR 160 ;TRY AGAIN  
1464 011106 052722 010000 326: BIS #BIT12,(R2)+ ;SET BIT 12 IN STAT2 IF NO LU  
1465 011112 022222 CMP (R2)+,(R2)+ ;POP OVER STAT2 AND STAT3  
1466 011114 000447 BR 336 ;  
1467 011116 052712 020000 318: BIS #BIT13,(R2) ;SET BIT 13 IN STAT2 IF M202  
1468 011122 104402 308: TYPE ;  
1469 011124 007114 CONN ;ASK IF LOOP-BACK IS ON  
1470 011126 004737 012266 JSR PC,INTTY ;GET REPLY  
1471 011132 022703 000131 CMP #13,R3 ;Y  
1472 011136 001406 BEQ 176 ;  
1473 011140 022703 000116 CMP #16,R3 ;N  
1474 011144 001406 BEQ 180 ;  
1475 011146 104402 TYPE ;  
1476 011150 005666 MOM ;IF NOT Y OR N TYPE "7"  
1477 011152 000763 BR 308 ;TRY AGAIN  
1478 011154 052722 040000 178: BIS #BIT14,(R2)+ ;TURNAROUND IS CONNECTED  
1479 011160 000402 BR 198 ;  
1480 011162 042722 040000 186: BIC #BIT14,(R2)+ ;NO TURNAROUND  
1481 011166 196: ;  
1482 011166 104403 INSTR ;  
1483 011170 007016 LINE ;  
1484 011172 104405 PARAM ;  
1485 011174 000000 0 ;  
1486 011176 000377 377 ;  
1487 011200 001254 TEMP4 ;  
1488 011202 000 0 ;  
1489 011203 001 1 ;  
1490 011204 113722 001254 MOVB TEMP4,(R2)+ ;STORE SWITCH PAC IN MAP  
1491 011210 104403 INSTR ;  
1492 011212 007054 BR ;  
1493 011214 104405 PARAM ;  
1494 011216 000000 0 ;
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1495 011220 000377 377 ;  
1496 011222 001254 TEMP4 ;  
1497 011224 000 0 ;  
1498 011225 001 1 ;  
1499 011226 113722 001254 MOVB TEMP4,(R2)+ ;STORE SWITCH PAC IN MAP  
1500 011232 005722 TST (R2)+ ;POP OVER STAT3  
1501 011234 005337 001252 338: DEC TEMP3 ;DEC DMC COUNT  
1502 011240 001402 BEQ 348 ;BR IF DONE  
1503 011242 000137 010612 JMP 128 ;JUMP IF NOT  
1504 011246 000137 011702 348: JMP 138 ;CONTINUE  
1505 011252 012701 160000 781: MOV #160000,R1 ;SET FOR FIRST ADDRESS TO BE TESTED  
1506 011256 012737 011774 000004 MOV #68,0#4 ;SET FOR NON-EXISTANT DEVICE TIME OUT  
1507 011264 005011 28: CLR (R1) ;CLEAR SEL0  
1508 011266 005711 TST (R1) ;IF DMC11 DMC SR S/B 0  
1509 011270 001172 BNE 36 ;IF NO DEV ; TRAP TO 4. IF NO BIT 8 THEN NO DMC1  
1510 011272 005061 000006 CLR 6(R1) ;CLEAR SEL6  
1511 011275 005761 000006 TST 6(R1) ;IF DMC11 THEN DMC RC S/B =0  
1512 011302 001165 BNE 36 ;BR IF NOT DMC11  
1513 011304 012711 002000 MOV #BIT10,(R1) ;SET ROM0  
1514 011310 005061 000004 CLR 4(R1) ;CLEAR SEL4  
1515 011314 012761 125252 000006 MOV #125252,6(R1) ;WRITE THIS TO SEL6  
1516 011322 002711 020000 BIS #BIT13,(R1) ;WRITE IT  
1517 011326 022761 125252 000004 CMP #125252,4(R1) ;WAS IT WRITTEN?  
1518 011334 001004 BNE 218 ;IF NO IT IS NOT CRAM  
1519 011336 052762 100000 000002 BIS #BIT15,2(R2) ;SET BIT15 IF CRAM  
1520 011344 000431 BR 228 ;  
1521 011346 012711 001000 218: MOV #BIT9,(R1) ;SET ROM1  
1522 011352 012761 100417 000006 MOV #100417,6(R1) ;PUT INSTRUCTION IN SEL6  
1523 011360 012711 001400 MOV #BIT9|BIT8,(R1) ;CLOCK INSTRUCTION (MICRO PROC PC TO 0)  
1524 011364 012711 002000 MOV #BIT10,(R1) ;SET ROM0  
1525 011370 022761 000626 000006 CMP #626,6(R1) ;IS IT LOCAL CROM  
1526 011376 001411 BEQ 238 ;BR IF YES  
1527 011400 022761 016520 000006 CMP #16520,6(R1) ;IS IT REMOTE CROM?  
1528 011406 001410 BEQ 228 ;BR IF YES  
1529 011410 022761 177777 000006 CMP #-1,6(R1) ;NO CROM?  
1530 011416 001404 BEQ 228 ;BR IF YES  
1531 011420 000516 BR 36 ;NOT A DMC  
1532 011422 052762 000002 000006 238: BIS #BIT1,6(R2) ;SET BIT 1 IN STAT3  
1533 ;AT THIS POINT IT IS ASSUMED THAT R1 HOLDS A DMC11 CSR ADDRESS.  
1534 011430 014122 225: MOV R1,(R2)+ ;STORE CSR IN CORE TABLE.  
1535 011432 012711 001000 156: MOV #BIT9,(R1) ;CLEAR LINE UNIT LOOP  
1536 011436 005061 000004 CLR 4(R1) ;CLEAR PORT4  
1537 011442 012761 122113 000006 MOV #122113,6(R1) ;LOAD INSTRUCTION (CLR DTR)  
1538 011450 002711 000400 BIS #BIT8,(R1) ;CLOCK INSTRUCTION  
1539 011454 012761 021264 000006 MOV #021264,6(R1) ;LOAD INSTRUCTION  
1540 011462 002711 000400 BIS #BIT8,(R1) ;CLOCK INSTRUCTION  
1541 011466 122761 000377 000004 CMP# #377,4(R1) ;IS IT ALL UNES?  
1542 011474 001003 BNE +10 ;BR IF NO  
1543 011476 052712 010000 BIS #BIT12,(R2) ;IF YES, NO LINE UNIT, SET STATUS BIT  
1544 011502 000436 BR 208 ;  
1545 011504 032761 000002 000004 BIT #BIT1,4(R1) ;IS SWITCH A ON?  
1546 011512 001403 BEQ +10 ;BR IF M201  
1547 011514 052712 060000 BIS #BIT13|BIT14,(R2) ;M202 ASSUME CONNECTOR  
1548 011520 000427 BR 208 ;CONNECTOR ON  
1549 011522 032761 000010 000004 BIT #BIT3,4(R1) ;IS MPDY SET  
1550 011530 001423 BNE 208 ;BR IF M201 NO CONNECTOR (ON LINE)
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1551 011532 012761 000100 000004      MOV      #BIT6,4(R1)      ;LOAD PORT4
1552 011540 012761 122113 000006      MOV      #122113,6(R1)   ;LOAD INSTRUCTION
1553 011546 052711 000430      BIS      #BIT8,(R1)      ;CLOCK INSTRUCTION(SET DTK)
1554 011552 012761 021264 000006      MOV      #021264,6(R1)   ;LOAD INSTRUCTION
1555 011560 052711 000400      BIS      #BIT9,(R1)      ;CLOCK INSTRUCTION(READ MODEM REG)
1556 011564 032761 000010 000004      BIT      #BIT3,4(R1)     ;IS MRDY SET NOW?
1557 011572 001402      BEQ      200             ;BR IF NO CONNECTOR
1558 011574 052712 040000      BIS      #BIT14,(R2)     ;SET STATUS BIT FOR CONNECTOR
1559 011600 005722      TST      (R2)+          ;POP POINTER
1560 011602 012761 021324 000006      MOV      #021324,6(R1)   ;PUT INSTRUCTION IN PORT6
1561 011610 012711 001400      MOV      #BIT9,BIT8,(R1) ;PORT4,LLU 15
1562 011614 156122 000004      BISH    4(R1),(R2)+     ;STORE ODCMP LINE # IN TABLE
1563 011620 012761 021344 000006      MOV      #021344,6(R1)   ;PORT6,INSTRUCTION
1564 011626 012711 001400      MOV      #BIT8,BIT9,(R1) ;CLOCK INSTR.
1565 011632 156122 000004      BISH    4(R1),(R2)+     ;STORE BH07, ADD IN TABLE
1566 011636 005722      TST      (R2)+          ;POP OVER STAT3
1567 011640 005011      CLR      (R1)+          ;CLEAR ROMI
1568 011642 005237 001310      DNNUM   ;UPDATE DEVICE COUNTER
1569 011644 022737 000020 001310      CMP      #20,DMNUM      ;ARE MAX. NO. OF DEV FOUND?
1570 011654 001412      BEQ      130             ;YES DON'T LOOK FOR ANY MORE.
1571 011656 005011      CLR      (R1)           ;CLEAR BIT 10
1572 011660 005061 000006      CLR      6(R1)          ;CLEAR SEL 6
1573 011664 002701 000010      ADD      #10,R1         ;UPDATE CSR POINTER ADDRESS
1574 011670 022701 164000      CMP      #164000,R1     ;BR IF DONE
1575 011674 001402      BEQ      130             ;JUMP IF NOT
1576 011676 000137 011264      JMP      200             ;BR IF DONE
1577 011702 005037 001306      CLR      DMACTV         ;JUMP IF NOT
1578 011706 005737 001310      DNNUM   ;WERE ANY DMC11'S FOUND AT ALL?
1579 011712 001423      BEQ      50              ;ERROR AUTO SIZER FOUND NO DMC11'S IN THIS SYS.
1580 011714 013701 001310      MOV      DMNUM,R1       ;SAVE NUMBER OF DEVICES
1581 011720 010137 001314      MOV      R1,SAVNUM      ;SAVE NUMBER OF DEVICES
1582 011724 000241      CLC                                     ;GENERATE ACTIVE REGISTER OF DEVICES.
1583 011726 006137 001306      ROL      DMACTV         ;SET THE BIT
1584 011732 005237 001306      INC      DMACTV
1585 011736 005301      DEC      R1
1586 011740 001371      BNE      40              ;BR IF MORE TO GENERATE
1587 011742 012737 000006 000004      MOV      #6,0#4         ;RESTORE TRAP VECTOR
1588 011750 013737 001326 001312      MOV      DMACTV,SAVACT  ;SAVE ACTIVE REGISTER
1589 011756 000137 012010      JMP      VECMAP         ;GO FIND THE VECTOR NOW.
1590 011762 104402 005760      JMP      ,MERR2        ;NOTIFY OPR THAT NO DMC11'S FOUND.
1591 011766 005000      CLR      R0             ;MAKE DATA LIGHTS ZERO
1592 011770 000000      HALT                                     ;STOP THE SHOW
1593 011772 000776      BR      #-2             ;DISABLE CONT. SW.
1594 011774 012716 011664      MOV      #140,(SP)     ;ENTERED BY NON-EXISTANT TIME-OUT.
1595 012000 000002      RTI                      ;RETURN TO MAINSTREAM
1596                                     WHICH: 1
1597 012002 000001      ,BYTE 2,2
1598 012004 002          TEMPS
1599 012006 001256
1600
1601 012010 032737 000001 001236      VECMAP: BIT      #SW00,STRMSW
1602 012016 001114      BNE      50
1603 012020 012737 000340 000022      MOV      #340,0#22     ;SET IOT TRAP Prio TO 7
1604 012026 012737 012202 000020      MOV      #40,0#20     ;SET IOT TRAP VECTOR
1605 012034 012702 001500      MOV      #DM.MAP,R2    ;SET SOFTWARE POINTER
1606 012040 012700 000300      MOV      #300,R0       ;FLOATING VECTORS START HERE.

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1607 012044 012701 000302      MOV      #302,R1        ;PC OF IOT INSTR.
1608 012050 010120      MOV      R1,(R0)+       ;START FILLING VECTOR AREA
1609 012052 012721 000004      MOV      #4,(R1)+       ;WITH +21 IOT
1610 012056 022021      CMP      (R0)+,(R1)+    ;ADD 2 TO R0 +R1
1611 012060 020127 001000      CMP      R1,#1000
1612 012064 001771      BLOS    10              ;BR IF MORE TO FILL
1613 012066 013737 001306 001246      MOV      DMACTV,TEMP1   ;STORE TEMPORALLY
1614 012074 006037 001246      ROR      TEMP1          ;BRING OUT A BIT
1615 012100 103063      BCC     50              ;BR IF ALL DONE
1616 012102 012704 000012      MOV      #12,R4         ;R4 IS INDEX REGISTER
1617 012106 016437 012252 177776      MOV      BRLVL(R4),PS   ;SET PS TO 7
1618 012114 011201      MOV      (R2),R1
1619 012116 012761 000200 000004      MOV      #200,4(R1)     ;SET ROMI
1620 012124 012711 001000      MOV      #BIT9,(R1)     ;PUT INSTRUCTION IN PORT6
1621 012130 012761 121111 000006      MOV      #121111,6(R1)  ;FORCE AN INTERRUPT
1622 012136 012711 001400      MOV      #BIT9,BIT8,(R1)
1623 012142 105200      70:  INCB      R0        ;STALL
1624 012144 001376      BR      #-2            ;FOR TIME TO INTERRUPT
1625 012146 162704 000002      SUB      #2,R4          ;GET NEXT LOWEST PS LEVEL
1626 012152 001404      BEQ     60              ;BR IF R4 = 0
1627 012154 016437 012252 177776      MOV      BRLVL(R4),PS   ;MOVE NEXT LOWER LEVEL IN PS
1628 012162 000767      BR      70             ;BR TO DELAY
1629 012164 002762 005300 000002      BIS      #5300,2(R2)    ;NO INTERRUPT ASSUME 300 AT LEVEL 5 AND FIX DMC11
1630 012172 005011      CLR      (R1)           ;CLEAR ROMI
1631 012174 002702 000010      ADD      #10,R2         ;POP SOFTWARE POINTER
1632 012200 000735      BR      28              ;KEEP GOING
1633 012202 001062 000002      BIS      (SP),2(R2)     ;GET VECTOR ADDRESS
1634 012206 042762 000007 000002      BIC      #7,2(R2)      ;CLEAR JUNK
1635 012214 016405 012254      MOV      BRLVL+2(R4),R5 ;GET BR LEVEL OF DMC11
1636 012220 000305      ASL      R5             ;SHIFT LEVEL 4 PLACES
1637 012222 000305      ASL      R5             ;TO THE LEFT FOR THE
1638 012224 000305      ASL      R5             ;STATUS TABLE
1639 012226 000305      ASL      R5
1640 012230 042705      BIC      #170777,R5     ;CLEAR UNWANTED BITS
1641 012234 000562 000002      BIS      R5,2(R2)      ;PUT BR LEVEL IN STATUS TABLE
1642 012240 022026      CMP      (SP)+,(SP)+    ;POP IOT JUNK OFF STACK
1643 012242 012710 012172      MOV      #30,(SP)      ;SET FOR RETURN
1644 012246 000002      RTI
1645 012250 000207      50:  RTS      PC        ;ALL DONE WITH "AUTO SIZING"
1646
1647 012252 000000      BRLVL: 0              ;LEVEL 0
1648 012254 000000      0              ;LEVEL 0
1649 012256 000200      200          ;LEVEL 4
1650 012260 000240      240          ;LEVEL 5
1651 012262 000300      300          ;LEVEL 6
1652 012264 000340      340          ;LEVEL 7
1653
1654
1655 012266 105777 166712      INTY:  TSTB     #TKCSR   ;WAIT FOR DONE
1656 012272 100375      BPL     #-4
1657 012274 017703 166706      MOV     #TKDBR,R3      ;PUT CHAR IN R3
1658 012301 105777 160704      TSTB   #TPCSR        ;WAIT UNTIL PRINTER IS PEADY
1659 012304 100375      BPL     #-4
1660 012306 100377 166700      MOV     R3,#TPDBR     ;ECHO CHAR
1661 012312 042703 000240      BIC     #BIT7,BIT5,R3 ;MASK OFF LOWER CASE
1662 012316 000297      RTS     PC             ;RETURN

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1663  
1664  
1665 012320 000000 01000 ; POINTER TO HI OR LO SPEED MICRO-CODE  
1666 01200  
1667 012322 01300 LOWAP; ; LOW SPEED (REMOTE) MICRO-CODE

7 MACRO DEFINITIONS  
9 REVISION 00  
10 FEBRUARY 25, 1975  
11  
12 REVISION 01  
13 MARCH 18, 1975  
14 NEW CSR BOARD CHANGES  
15  
16 HARVEY M. SCHLESINGER  
18 COPYRIGHT 1975 DIGITAL EQUIPMENT CORPORATION  
70 MICRO INSTRUCTION DEFINITIONS  
71 BRANCH INSTRUCTIONS  
114 INDEXED BRANCH INSTRUCTIONS  
154 MOVE INSTRUCTIONS  
250 INPUT/OUTPUT ASSIGNMENTS  
310 PROTOCOL DEPENDANT MACROS  
353 DMC11 DDCMP MICRO CODE ASSEMBLED FOR USE WITH THE M8201 LINE UNIT  
361 VERSION 00A FEBRUARY 26, 1975  
362  
363 HARVEY M. SCHLESINGER  
364  
365 COPYRIGHT 1975, DIGITAL EQUIPMENT CORPORATION  
366  
367 VERSION 00B MARCH 17, 1975  
368 CSR AND MICROPROCESSOR CHANGES  
369  
370 VERSION 00C NOVEMBER 6, 1975  
371 RETRANSMISSION CHANGES  
372  
373 VERSION 00D DECEMBER 3, 1975  
374 TRANSMIT DONE CHANGES  
375  
376 THE LATEST MODIFICATIONS WERE ADDED ON:  
377 OCTOBER 13, 1976  
378 THIS VERSION WAS USED TO BLAST THE FIRST  
379 RELEASE ON OCTOBER 13, 1976  
381 MICROPROCESSOR MAIN MEMORY ASSIGNMENTS  
443 SCRATCH PAD ASSIGNMENTS  
478 INIT--INITIALIZATION ROUTINE  
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637 INWAIT---WAIT FOR RQ1 TO CLEAR  
692 OUTINT---SET UP OUTPUT INTERRUPT (RDY0)  
740 OUTWAI---WAIT FOR RDY0 TO GO AWAY  
747 CTLSRV---CNTL I SERVICE  
768 TBASRV---TRANSMITTER BUFFER ADDRESS SERVICE  
790 RBASRV---RECEIVE BUFFER ADDRESS SERVICE  
862 RCVA--ROUTINE TO HANDLE FIRST DDCMP CHARACTER  
892 RCVB--ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD  
931 RCVC--ROUTINE TO HANDLE SECOND CHARACTER OF COUNT FIELD, SELECT AND FINAL  
950 RCVD--ROUTINE TO HANDLE RESPONSE FIELD FOR NUMBERED MESSAGES  
974 RCVE--ROUTINE TO HANDLE N FIELD OF NUMBERED MESSAGE  
987 RCVF--ROUTINE TO IGNORE ADDRESS  
992 RCVG--ROUTINE TO IGNORE CMC1  
997 RCVH--ROUTINE TO HANDLE CMC2 AND TO DISPATCH NUMBERED AND UNNUMBERED TYPES

1056	RCVK01--ROUTINE TO HANDLE FIRST BYTE ODD RECEIVE
1063	RCVK0--PROCESS ODD CHARACTER
1093	RCVKE--HANDLE EVEN BYTES
1140	RCV1--STORE UNNUMBERED MESSAGE TYPE
1146	RCVJ--ROUTINE TO HANDLE SUBTYPE FIELD, SELECT AND FINAL
1151	RCVR--UNNUMBERED MESSAGE RESPONSE FIELD
1161	RCVQ--UNNUMBERED MESSAGE--NUMBER FIELD
1167	RCVL--PROCESS CRC3
1192	RCVM--PROCESS CRC4--END OF DATA MESSAGE
1211	EM2--PROCESS RLD MESSAGE
1251	TMTUA--TRANSMITTER DISPATCH ROUTINE
1257	TMTA--FIRST CHARACTER OF HEADER
1304	TMTB--OUTPUT FIRST CHAR OF COUNT
1330	TMTC--OUTPUT SECOND CHAR OF COUNT
1347	TMTD--RESPONSE FIELD--NUMBERED MESSAGE
1367	TMTL--NUMBER FIELD--NUMBERED MESSAGE
1376	TMTF--NUMBERED MSG ADDRESS FIELD
1389	TMTI--NUMBERED MSG HEADER EOM
1399	IMTM--ROUTINE TO OUTPUT DATA CHARACTERS
1454	TMTI--SEND UNNUMBERED TYPE FIELD
1460	TMTJ--SEND SUB-TYPE FIELD
1467	TMTK--OUTPUT RESPONSE FIELD (UNNUMB MSG)
1475	TMTL--UNNUMB MSG NUMBER FIELD
1493	TMTM--UNNUMB MSG--STATION ADDRESS
1509	TIMSRV--TIMEOUT ROUTINE--SENDS REP
1570	SNACK--ROUTINE TO SEND AN ACK
1627	REP HANDLER
1636	START HANDLER
1649	STACK HANDLER
1685	NXMERR ---NON EXISTANT MEMORY HANDLER
1692	SELQSY--ROUTINE TO CHECK SELECT AND QSYNC AND DIDDLE LINE STATUS WORD

5	
6	
7	.TITLE DMC-11 MICROPROCESSOR INSTRUCTIONS
8	.SBTTL MACRO DEFINITIONS
9	;
10	.SBTTL REVISION 00
11	.SBTTL FEBRUARY 25, 1975
12	.SBTTL
13	.SBTTL REVISION 01
14	.SBTTL MARCH 10, 1975
15	.SBTTL NEW CSR BOARD CHANGES
16	.SBTTL
17	.SBTTL HARVEY M. SCHLESINGER
18	;
19	.SBTTL COPYRIGHT 1975 DIGITAL EQUIPMENT CORPORATION
	;



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258          .SBTTL INPUT/OUTPUT ASSIGNMENTS
259          ;IBUS ASSIGNMENTS
260          INCON=0+100000          ;IN CONTROL CSR
261          MAIN=20+100000         ;MAINTAINENCE REGISTER
262          OCON=40+100000         ;OUT CONTROL CSR
263          UBADDR=60+100000       ;UNUSED
264          PORT1=100+100000       ;CSR4
265          PORT2=120+100000       ;CSR5
266          PORT3=140+100000       ;CSR6
267          PORT4=160+100000       ;CSR7
268          NPR=200+100000         ;NPR CONTROL
269          UBRM=220+100000        ;BR(INTERRUPT)CONTROL
270          INDATA1=0              ;INPUT DATA LOW BYTE
271          INDATA2=20             ;INPUT DATA HIGH BYTE
272          IOBA1=140              ;OUTPUT BA LOW BYTE
273          IOBA2=160              ;OUTPUT BA HIGH BYTE
274          IIBA1=100              ;INPUT BA LOW BYTE
275          IIBA2=120              ;INPUT BA HIGH BYTE
276          RCVDAT=200             ;RECEIVE DATA
277          TMTCON=220             ;TMTR CONTROL
278          RCVCON=240             ;RCVR CONTROL
279          MODEM=260              ;MODEM CONTROL
280          SYNREG=300             ;SYN REGISTER
281          LNOSWE=320             ;LINE NUMBER SWITCH
282          BMS73=340              ;BMS73 ADDRESS
283          LUMAIN=360             ;LINE UNIT MAINTAINENCE
284          ;OBUS ASSIGNMENTS
285          ;EXTENDED OBUS
286          OINCON=0              ;IN CONTROL CSR
287          OMAIN=1                ;MAINT
288          OCON=2                 ;OUT CONTROL CSR
289          OUBADD=3               ;UNUSED
290          OPORT1=4               ;CSR4
291          OPORT2=5               ;CSR5
292          OPORT3=6               ;CSR6
293          OPORT4=7               ;CSR7
294          ONPR=10                ;NPR CONTROL
295          OBR=11                 ;BR CONTROL
296          ;UNEXTENDED OBUS
297          OUTDA1=2                ;OUTPUT DATA LOW BYTE
298          OUTDA2=3                ;OUTPUT DATA HIGH BYTE
299          OBA1=6                  ;OUTPUT BA LOW BYTE
300          OBA2=7                  ;OUTPUT BA HIGH BYTE
301          IBA1=4                  ;INPUT BA LOW BYTE
302          IBA2=5                  ;INPUT BA HIGH BYTE
303          TMTDAT=10              ;TMTR DATA
304          OTMCO=11                ;TMTR CONTROL
305          ORCVCO=12               ;RCVR CONTROL
306          OMODEM=13              ;MODEM CONTROL
307          SYNC=14                ;SYN REGISTER
308          OLUMAR=17              ;LINE UNIT MAINT.

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310          .SBTTL PROTOCOL DEPENDANT MACROS
311          ;
312          ;
313          ;
314          ;
315          ;
316          ;
317          ;
318          ;
319          ;
320          ;
321          ;
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340          ;
341          ;
342          ;
343          ;
344          ;
345          ;
346          ;
347          ;
348          ;
349          ;
350          177777          MICPC=177777 ;INIT MICRO PC
351          ;

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353  
354 000000  
355 000000

.SBTTL DMC11 DDCMP MICRO CODE ASSEMBLED FOR USE WITH THE M8201 LINE UNIT  
LOW=0  
\$LOW=0

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.TITLE DMC11 DDCMP PROTOCOL IMPLEMENTATION  
.IDENT /V0001/  
.SBTTL VERSION 00A FEBRUARY 26,1975  
.SBTTL  
.SBTTL HARVEY M. SCHLESINGER  
.SBTTL  
.SBTTL COPYRIGHT 1975, DIGITAL EQUIPMENT CORPORATION  
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.SBTTL RELEASE ON OCTOBER 13, 1976

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381 .SBTTL MICROPROCESSOR MAIN MEMORY ASSIGNMENTS
382 ;ALLOCATION OF MICROPROCESSOR MAIN MEMORY
383 NAKSR=0 ;NAKS RECD--DYNAMIC
384 NAKST=NAKSR+1 ;NAKS TMED--DYNAMIC
385 REPSR=NAKST+1 ;REPS RECD--DYNAMIC
386 REPST=REPSR+1 ;REPS TMED--DYNAMIC
387 NP=REPST+3 ;CONSTANT 0
388 NTLR=NP+1 ;NAKS=MSG NO BUFFERS CUMUL.
389 NHDR=NTLR+1 ;NAKS=MSG HEADER BAD
390 NDATR=NHDR+1 ;NAKS=DATA BAD
391 NTL5=NDATR+1 ;NAK SENT --NO BUFFERS
392 NHDS=NTL5+1 ;NAK SENT BAD HEADER
393 NDATS=NHDS+1 ;NAK SENT BAD DATA
394 REPCS=NDATS+1 ;REPS SENT CUMUL
395 REPCR=REPCS+1 ;REPS RECD CUMUL
396 BASE=REPCR+1 ;CORE TABLE BASE ADDRESS
397 SRC=BASE+3 ;START OF INPUT CHAIN--NEXT RECV DONE
398 ERC=SRC+1 ;END OF INPUT CHAIN
399 LRC=ERC+1 ;LAST POINTER RECV
400 RCL1=LRC+1 ;RECEIVE LINK #1
401 RCL2=RCL1+5 ; " " #2
402 RCL3=RCL2+5 ; " " #3
403 RCL4=RCL3+5
404 RCL5=RCL4+5
405 RCL6=RCL5+5
406 RCL7=RCL6+5
407 STC=RCL7+5 ;START OF OUTPUT CHAIN---NEXT TMT DONE
408 LTC=STC+1 ;LAST TRANSMITTED
409 ETC=LTC+1 ;END OF TRANSMIT CHAIN
410 TML1=ETC+1 ;TRANSMIT LINK #1
411 TML2=TML1+6 ; " " #2
412 TML3=TML2+6 ; " " #3
413 TML4=TML3+6
414 TML5=TML4+6
415 TML6=TML5+6
416 TML7=TML6+6
417 TML8=TML7+6
418 T=TML8+6 ;TYPE FIELD
419 ST=T+1 ;SUBTYPE FIELD
420 ISP17=ST+1 ;MSG ACKED IMAGE
421 IMG10=ISP17+1 ;IMAGE OF BIT 1 OF SP10
422 IMG11=IMG10+1 ;IMAGE OF SP11
423 IMG12=IMG11+1 ;IMAGE OF SP12
424 IMG17=IMG12+1 ;IMAGE OF SP17
425 PRST=IMG17+1 ;PORT STATE
426 TYPTAB=PRST+1 ;TYPE TABLE---
427 ;72 TYPE TABLE REP
428 ;73 " " NAK
429 TYPSTI=TYPTAB+2 ;74 " " START
430 ;75 " " STACK
431 ;
432 ;
433 OSTATE=TYPSTI+3 ;OLD STATE POINTER
434 ISP11=OSTATE+1 ;SP11 IMAGE
435 ISP12=ISP11+1 ;SP12 IMAGE
436 INCONS=ISP12+1 ;IN CONTROL CSR IMAGE
```

```
437 RTHRS=INCONS+1 ;RECV THRESHOLD LINK
438 NXTINT=240 ;NEXT INTERRUPT POSITION
439 NXTSP=NXTINT+1 ;END OF INTERRUPT CHAIN
440 INTSTK=NXTSP+1 ;STACK OF INTERRUPTS
441 MMEND=400 ;MAIN MEMORY END
```

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443          .SBTTL SCRATCH PAD ASSIGNMENTS
444          SP0=0 ;SP0---SCRATCH REGISTER
445          SP1=1 ;SP1---PORT STATUS WORD
446          ;BIT ASSIGNMENTS
447          ;BIT0---INIT MODE
448          ;BIT1---SEC STATION SELECT(UNUSED)
449          ;BIT2---NO BUFFER ASSIGNED IN BOOT MODE
450          ;BIT3---DLE RECEIVED WHILE NOT IN MAINT MODE
451          ;BIT4---INTERRUPT PENDING
452          ;BIT6---DISCONNECT ERROR
453          ;BIT7---BOOT MODE
454          SP2=2 ;SP2---TRANSMIT STATE POINTER
455          SP3=3 ;SP3---RECEIVE STATE POINTER
456          SP4=4 ;SP4---END RECV ADDRESS
457          SP5=5 ;SP5---END RECEIVE ADDRESS
458          SP6=6 ;SP6---END TRANSMIT ADDRESS
459          SP7=7 ;SP7---END TRANSMIT ADDRESS
460          SP10=10 ;SP10---LINE STATUS WORD
461          ;BIT ASSIGNMENTS
462          ;BIT0---UNNUMB PENDING
463          ;BIT1---MESSAGE IN PROGRESS
464          ;BIT2---LINE HAS GONE IDLE
465          ;BIT3---START RECEIVED
466          ;BIT4---CLEAR ACTIVE ON END
467          ;BIT5---START MODE
468          ;BIT6---HALF DUPLEX
469          ;BIT7---OK TO SEND
470          SP11=11 ;SP11---R FIELD
471          SP12=12 ;SP12---N FIELD
472          SP13=13 ;SP13---TYPE
473          SP14=14 ;SP14---RECEIVE LINK IMAGE
474          SP15=15 ;SP15---TIMER ENTRY---NUMBER OF ONE SECOND TICKS
475          SP16=16 ;SP16---POINTER TO TMT LINK COPY IN MAIN MEM
476          SP17=17 ;SP17---LAST MESSAGE ACKNOWLEDGED

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478          .SBTTL INIT--INITIALIZATION ROUTINE
479          ;ZERO5 MAIN MEMORY
480          ;LOOP8 WAITING FOR RECEIVE DATA(BOOT?)
481          ;OR FOR RQI TO BE SET
482          ;WILL ACCEPT ONLY BASE FORMAT. ALL OTHERS WILL RETURN A PROCEDURE ERROR
483          ;
484          ;AT INITIALIZATION --- THE HARDWARE CLEARS THE BR AND MAR
485          ;=12322
486          @12322 @12322          INIT: SP BR,SELB,SP0 ;CLEAR SP0
487          (1) @12322 @03220          MICPC=MICPC+1
488          (1) @12324 @00001          <MOVE!SPX1BR!SELB!SP0> ;PAGE ONE TRANSFER ADDRESS
489          (1) @12324 @03226          SP BR,SELB,SP3
490          (1) @12326 @00002          MICPC=MICPC+1
491          (1) @12326 @03223          <MOVE!SPX1BR!SELB!SP3> ;CLEAR SP17
492          (1) @12326 @03237          SP BR,SELB,SP17
493          (1) @12330 @00003          MICPC=MICPC+1
494          (1) @12330 @01200          <MOVE!WROUTX1BR!<SEL1!OINCON> OUT BR,<SEL1!OINCON> ;ZERO THE IN CONTROL CSR
495          (1) @12332 @00004          MICPC=MICPC+1
496          (1) @12332 @01202          <MOVE!WROUTX1BR!<SEL1!OOCON> OUT BR,<SEL1!OOCON> ;ZERO THE OUT CONTROL CSR
497          (1) @12334 @00005          MICPC=MICPC+1
498          (1) @12334 @00370          SP IMM,370,SP10
499          (1) @12334 @00370          <MOVE!SPX1IMM!370!SP10> ;WRITE 5 ONE BITS TO THE HIGH ORDER
500          (1) @12336 @00006          SP BR,AA,SP10 ;BITS OF SP10
501          (1) @12336 @03130          MICPC=MICPC+1 ;SHIFT SP10 LEFT SETTING CARRY THE
502          (1) @12336 @03130          <MOVE!SPX1BR!AA!SP10>
503          (1) @12340 @00007          MEMINC BR,ADDC!SP3 ;FIRST 5 TIMES THRU THE LOOP
504          (1) @12340 @07642          MICPC=MICPC+1 ;WRITE A ONE TO THE FIRST 5 MEMORY
505          (1) @12340 @07642          <MOVE!WRMEM!INCMAR!BR!<ADDC!SP3>>
506          (1) @12342 @00010          SP BR,INCA,SP0 ;LOCATIONS AND ZERO THE REST
507          (1) @12342 @03060          MICPC=MICPC+1 ;INCREMENT COUNTER
508          (1) @12344 @00011          <MOVE!SPX1BR!INCA!SP0>
509          (1) @12344 @00011          Z 108 ;ALL DONE
510          (1) @12344 @00011          MICPC=MICPC+1
511          (1) @12344 @01413          <JUMP!ZCOND!<108-INIT!3000*4>!<108-INIT!777/2>>
512          (1) @12346 @00012          ALWAYS 56 ;KEEP GOING
513          (1) @12346 @00012          MICPC=MICPC+1
514          (1) @12346 @012350          <JUMP!ZCOND!<58-INIT!3000*4>!<58-INIT!777/2>>
515          (1) @12350 @00013          SPBR IMM,1,SP1 ;WRITE A 1 TO THE BR AND SP1
516          (1) @12350 @03401          MICPC=MICPC+1
517          (1) @12350 @03401          <MOVE!SPBRX!IMM!1!SP1>
518          (1) @12352 @00014          SP BR,SELB,SP11 ;WRITE A 1 TO SP11
519          (1) @12352 @03231          MICPC=MICPC+1
520          (1) @12352 @03231          <MOVE!SPX1BR!SELB!SP11>
521          (1) @12354 @00015          SP BR,SELB,SP12 ;WRITE A 1 TO SP12
522          (1) @12354 @03232          MICPC=MICPC+1
523          (1) @12354 @03232          <MOVE!SPX1BR!SELB!SP12>
524          (1) @12356 @00016          LOMA IMM,PRST ;POINT MAR TO UNNUM MSG SKELETON
525          (1) @12356 @10162          MICPC=MICPC+1
526          (1) @12356 @10162          <MOVE!LDMAR!IMM!<PRST!377>>

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504 012360          PSTAT1 NIDLE2          ;WRITE PORT IDLE STATE
(1) 012360          MEMINC IMM,<<NIDLE2=INIT&777/2>>
(2) 012360 000017  MICPC=MICPC+1
(2) 012360 016520  <MOVE!WRHEM!INCMAR!IMM1<<NIDLE2=INIT&777/2>>>
505 012362          BRWRT IMM,226          ;WRITE SYNC TO MEMORY
(1) 012362 000020  MICPC=MICPC+1
(1) 012362 000020  <MOVE!WRTEBR!IMM1<226>>
506 012364          OUTPUT BR,SELB1SYNC      ;LOAD THE SYNC REGISTER
(1) 012364 000021  MICPC=MICPC+1
(1) 012364 002234  <MOVE!WROUT!BR!<SELB1SYNC>>
507 012366          MEMINC IMM,3            ;REP
(1) 012366 000022  MICPC=MICPC+1
(1) 012366 016403  <MOVE!WRHEM!INCMAR!IMM1<3>>
508 012370          MEM IMM,2              ;NAK
(1) 012370 000023  MICPC=MICPC+1
(1) 012370 002402  <MOVE!WRHEM!IMM1<2>>
509 012372          SP MEMX1INCMAR,SELB,SP15  ;SET STARTING COUNT
(1) 012372 000024  MICPC=MICPC+1
(1) 012372 057235  <MOVE!SPX!MEMX1!INCMAR!SELB!SP15>
510 012374          MEMINC IMM,6            ;START
(1) 012374 000025  MICPC=MICPC+1
(1) 012374 016406  <MOVE!WRHEM!INCMAR!IMM1<6>>
511 012376          MEMINC IMM,7            ;STACK
(1) 012376 000026  MICPC=MICPC+1
(1) 012376 016407  <MOVE!WRHEM!INCMAR!IMM1<7>>
512 012400          MEMINC IMM,1            ;ACK
(1) 012400 000027  MICPC=MICPC+1
(1) 012400 016401  <MOVE!WRHEM!INCMAR!IMM1<1>>
513 012402          LDMA IMM,STC            ;LOAD ADDRESS OF LAST TMT CHAIN
(1) 012402 000030  MICPC=MICPC+1
(1) 012402 010070  <MOVE!LDMAR!IMM1<STC&377>>
514 012404          MEMINC IMM,TML1         ;STORE ADDRESS OF FIRST TMT LINK
(1) 012404 000031  MICPC=MICPC+1
(1) 012404 016473  <MOVE!WRHEM!INCMAR!IMM1<TML1>>
515 012406          MEMINC IMM,TML1
(1) 012406 000032  MICPC=MICPC+1
(1) 012406 016473  <MOVE!WRHEM!INCMAR!IMM1<TML1>>
516 012410          MEMINC IMM,TML1
(1) 012410 000033  MICPC=MICPC+1
(1) 012410 016473  <MOVE!WRHEM!INCMAR!IMM1<TML1>>
517 012412          LDMA IMM,SRC            ;LOAD ADDRESS OF LAST RECV CHAIN
(1) 012412 000034  MICPC=MICPC+1
(1) 012412 010022  <MOVE!LDMAR!IMM1<SRC&377>>
518 012414          MEMINC IMM,RCL1         ;SET UP ADDRESS OF FIRST RECV LINK
(1) 012414 000035  MICPC=MICPC+1
(1) 012414 016425  <MOVE!WRHEM!INCMAR!IMM1<RCL1>>
519 012416          MEMINC IMM,RCL1
(1) 012416 000036  MICPC=MICPC+1
(1) 012416 016425  <MOVE!WRHEM!INCMAR!IMM1<RCL1>>
520 012420          MEMINC IMM,RCL1
(1) 012420 000037  MICPC=MICPC+1
(1) 012420 016425  <MOVE!WRHEM!INCMAR!IMM1<RCL1>>
521 012422          LDMA IMM,NXTINT        ;ADDRESS OF NEXT INTERRUPT POINTER TO MAR
(1) 012422 000040  MICPC=MICPC+1
(1) 012422 010240  <MOVE!LDMAR!IMM1<NXTINT&377>>
522 012424          MEMINC IMM,INTSTK      ;INITIALIZE NEXT INTERRUPT POINTER

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(1) 012424 000041  MICPC=MICPC+1
(1) 012424 016042  <MOVE!WRHEM!INCMAR!IMM1<INTSTK>>
523 012426          MEM IMM,INTSTK          ;INITIALIZE INSERTION POINTER
(1) 012426 000042  MICPC=MICPC+1
(1) 012426 002042  <MOVE!WRHEM!IMM1<INTSTK>>
524 012430          BRWRT IMM,200          ;WRITE THE RUN BIT TO THE BR
(1) 012430 000043  MICPC=MICPC+1
(1) 012430 000000  <MOVE!WRTEBR!IMM1<200>>
525 012432          OUT BR,<SELB!OMAIN>      ;WRITE THE RUN BIT TO MAINT CSR
(1) 012432 000044  MICPC=MICPC+1
(1) 012432 001221  <MOVE!WROUT!BR!<SELB!OMAIN>>
526 012432          ;FALL INTO IDLE LOOP

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533  
534  
535  
536  
537  
538 012434  
(1) 000045  
(1) 012434 060610  
539 012436  
(1) 000046  
(1) 012436 112400  
540 012440  
(1) 000047  
(1) 012440 112000  
541 012442  
(1) 000050  
(1) 012442 100452  
542  
543 012444  
(1) 000051  
(1) 012444 063222  
544 012446  
(1) 000052  
(1) 012446 020640  
545 012450  
(1) 000053  
(1) 012450 167203  
546 012452  
(1) 000054  
(1) 012452 010162  
547 012454  
(1) 000055  
(1) 012454 140620

```
.SBTTL IDLE--PROGRAM IDLE LOOP
;PROGRAM IDLE LOOP
;DISPATCHES TO APPROPRIATE SERVICE ROUTINES
;USES STATE POINTERS FOR TMT,RCV,CSR ACTIVITY
;
IDLE: BRWRT BR,<SELA:SP10> ;READ TRANSMIT STATUS WORD FROM SP10 TO BR
      MICPC=MICPC+1
      <MOVE>WRTBRIBRI:<SELA:SP10>>
      BR1 TMTDA ;IF DATA TO SEND-- BRANCH
      MICPC=MICPC+1
      <JUMP>IBR1CONI:<TMTDA=INIT63000*4>I<TMTDA=INIT6777/2>>
      BR0 TMTDA ;IF DATA TO SEND-- BRANCH
      MICPC=MICPC+1
      <JUMP>IBR0CONI:<TMTDA=INIT63000*4>I<TMTDA=INIT6777/2>>
      ALWAYS I1
      MICPC=MICPC+1
      <JUMP>ALCONDI<I1=INIT63000*4>I<I1=INIT6777/2>>
;
XEXIT: SP BR,SELB,SP2
      MICPC=MICPC+1
      <MOVE>ISPIBRI:SELB:SP2>
I1: BRWRT IBUS,RCVCON ;READ LINE UNIT RECEIVE CONTROL WORD
      MICPC=MICPC+1
      <MOVE>WRTBRIBRI:<RCVCON>>
      BR4 BR,SELA,SP3:PAGE1 ;BRANCH BASED UPON RCV STATE
      MICPC=MICPC+1
      <JUMP>IBR4CONI:BRI:SELA:SP3:PAGE1>
I2: LDMA IMM,PRST ;ADDRESS POINT STATE
      MICPC=MICPC+1
      <MOVE>ILDMMARI:IMM:<PRST6377>>
      ALWAYS MEMX,SELB,0 ;INDEX
      MICPC=MICPC+1
      <JUMP>ALCONDI:MEMX:SELB:0>
```

549  
550 012456  
(1) 012456  
(2) 000056  
(2) 012456 002520  
551 012460  
(1) 000057  
(1) 012460 010017  
552 012462  
(1) 000060  
(1) 012462 136504  
553 012464  
(1) 000061  
(1) 012464 136520  
554 012466  
(1) 000062  
(1) 012466 122560  
555 012470  
(1) 000063  
(1) 012470 123000  
556 012472  
(1) 000064  
(1) 012472 002500  
557 012474  
(1) 000065  
(1) 012474 001260  
558 012476  
(1) 000066  
(1) 012476 002520  
559 012500  
(1) 000067  
(1) 012500 002233  
560 012502  
(1) 000070  
(1) 012502 040620  
561 012504  
(1) 000071  
(1) 012504 103100  
562 012506  
(1) 000072  
(1) 012506 010153  
563 012510  
(1) 000073  
(1) 012510 016406  
564 012512  
(1) 000074  
(1) 012512 002700  
565 012514  
(1) 000075  
(1) 012514 003161  
566 012516  
(1) 000076  
(1) 012516 000641  
567 012520  
(1) 000077  
(1) 012520 110733

```
.SBTTL BASERV--- BASE SERVICE ROUTINE
BASERV: PSTATE NIDLE2
      MEM IMM,<<NIDLE2=INIT6777/2>>
      MICPC=MICPC+1
      <MOVE>WRTMEM:IMM:<<NIDLE2=INIT6777/2>>>
      LDMA IMM,BASE ;CLEAR TO MAR SO IT POINTS TO BASE POINT
      MICPC=MICPC+1
      <MOVE>ILDMMARI:IMM:<BASE6377>>
      MEMINC IBUS,PORT1 ;READ CSR4
      MICPC=MICPC+1
      <MOVE>WRTMEM:INCMMAR:IBUS:<PORT1>>
      MEMINC IBUS,PORT2 ;READ CSR5
      MICPC=MICPC+1
      <MOVE>WRTMEM:INCMMAR:IBUS:<PORT2>>
      MEM IBUS,PORT4
      MICPC=MICPC+1
      <MOVE>WRTMEM:IBUS:<PORT4>>
      SP IBUS,INCON,SP0 ;READ INPUT CONTROL CSR
      MICPC=MICPC+1
      <MOVE>ISPIBRI:IBUS:INCON:SP0>
      BRWRT IMM,100 ;CLEAR THE BR
      MICPC=MICPC+1
      <MOVE>WRTBR:IMM:<100>>
      OUT BR,<AANDB:OINCON> ;CLEAR THE INCONTROL CSR
      MICPC=MICPC+1
      <MOVE>WROUT:IBRI:<AANDB:OINCON>>
      BRWRT IMM,120 ;MASK FOR HDX AND DTR
      MICPC=MICPC+1
      <MOVE>WRTBR:IMM:<120>>
      OUTPUT BR,<SELB:OIMODEM>
      MICPC=MICPC+1
      <MOVE>WROUT:IBRI:<SELB:OIMODEM>>
      BRWRT MEMX,SELB ;READ SEL6
      MICPC=MICPC+1
      <MOVE>WRTBR:MEMX:<SELB>>
      BR4 RESUME ;IF SET RESUME
      MICPC=MICPC+1
      <JUMP>IBR4CONI:<RESUME=INIT63000*4>I<RESUME=INIT6777/2>>
      LDMA IMM,T ;LOAD ADDRESS OF TYPE FIELD
      MICPC=MICPC+1
      <MOVE>ILDMMARI:IMM:<T6377>>
      MEMINC IMM,6 ;WRITE START TYPE TO MEMORY
      MICPC=MICPC+1
      <MOVE>WRTMEM:INCMMAR:IMM:<6>>
      MEM IMM,300 ;WRITE SELECT AND FINAL TO MEMORY
      MICPC=MICPC+1
      <MOVE>WRTMEM:IMM:<300>>
      SP BR,DECA,SP1 ;TURN OFF INIT MODE
      MICPC=MICPC+1
      <MOVE>ISPIBRI:DECA:SP1>
BS1: BRWRT IMM,241 ;SET OK TO SEND,STARTMODE AND UNNUM PENDING
      MICPC=MICPC+1
      <MOVE>WRTBR:IMM:<241>>
      ALWAYS SA3
      MICPC=MICPC+1
      <JUMP>ALCONDI:<SA3=INIT63000*4>I<SA3=INIT6777/2>>
```

```

568 012522      000100
(1) 012522 003004
569 012524      000101
(1) 012524 003070
570
571 012526      000102
(1) 012526 010017
572 012530      000103
(1) 012530 000736
573 012532      000104
(1) 012532 110902
574 012534      000105
(1) 012534 010156
575 012536      000106
(1) 012536 043330
576 012540      000107
(1) 012540 057231
577 012542      000110
(1) 012542 057232
578 012544      000111
(1) 012544 043237
579 012546      000112
(1) 012546 003170
580
581 012550      000113
(1) 012550 000520
582 012552      000114
(1) 012552 000114
583
584 012554      000115
(1) 012554 003161
585 012556      000116
(1) 012556 000600
586 012560      000117
(1) 012560 110733

RESUME: SP      IMM,SP4,4          ;SET UP SP4 FOR COUNTING NPKS
MICPC=MICPC+1
<MOVE>SPX:IMM:SP4:4>
SP      BR,INCA,SP10          ;SET UNNUM MESSAGE PENDING TO
MICPC=MICPC+1
<MOVE>SPX:BR:INCA:SP10>
LDMA   IMM,BASE              ;TRICK TRANSMITTER CODE
MICPC=MICPC+1                ;ADDRESS BASE TABLE ADDRESS
<MOVE>LDMAR:IMM:<BASE&377>>
STATE  FUDGE                 ;SET TMTR STATE TO ENTER TABLE UPDATE
MICPC=MICPC+1
<MOVE>WRTBR:IMM:<FUDGE-INIT&777/2>>
ALWAYS TB0                   ;GO SET UP NXT BITS AND ADDRESS OF BASE FOR NPRS
MICPC=MICPC+1
<JUMP>ALCONDI:<TB0-INIT&3000*4>:<TB0-INIT&777/2>>
BS2:   LDMA   IMM,IMG10
MICPC=MICPC+1
<MOVE>LDMAR:IMM:<IMG10&377>>
SP      MEMX,AORB,SP10        ;RESTORE BIT 1 OF SP10
MICPC=MICPC+1
<MOVE>SPX:MEMX:AORB:SP10>
SP      MEMX:INCMAR,SELB,SP11 ;RESTORE SP11
MICPC=MICPC+1
<MOVE>SPX:MEMX:INCMAR:SELB:SP11>
SP      MEMX:INCMAR,SELB,SP12 ;RESTORE SP12
MICPC=MICPC+1
<MOVE>SPX:MEMX:INCMAR:SELB:SP12>
SP      MEMX,SELB,SP17        ;RESTORE SP17
MICPC=MICPC+1
<MOVE>SPX:MEMX:SELB:SP17>
SP      BR,DECA,SP10         ;TURN OFF UNNUM MESSAGE PENDING AND
MICPC=MICPC+1
<MOVE>SPX:BR:DECA:SP10>
STATE  NIDLE2                ;ZERO THE BRG
MICPC=MICPC+1                ;PORT STATUS
<MOVE>WRTBR:IMM:<NIDLE2-INIT&777/2>>
SP      BR,SELB,SP13         ;SAVE IN SP13 - NOTE THAT STATUS READ INTO
MICPC=MICPC+1
<MOVE>SPX:BR:SELB:SP13>
SP      BR,DECA,SP10         ;RAM WAS TABLE UPDATE WHICH SAVED STATUS IN SP13
MICPC=MICPC+1
<MOVE>SPX:BR:DECA:SP10>
STATE  NIDLE2                ;CLEAR INIT MODE
MICPC=MICPC+1
<MOVE>SPX:BR:DECA:SP10>
BRWRT  IMM,200               ;SET OK TO SEND
MICPC=MICPC+1
<MOVE>WRTBR:IMM:<200>>
ALWAYS SA3
MICPC=MICPC+1
<JUMP>ALCONDI:<SA3-INIT&3000*4>:<SA3-INIT&777/2>>

```

```

588
589 012562      000120
(1) 012562 000601
594 012564      000121
(1) 012564 103220
596 012566      000122
(1) 012566 123400
597 012570      000123
(1) 012570 001620
598 012572      000124
(1) 012572 103155
599
600
601 012574      000125
(1) 012574 003001
606 012576      000126
(1) 012576 102731
608 012600      000127
(1) 012600 123620
609 012602      000130
(1) 012602 113245
614 012604      000131
(1) 012604 023060
615 012606      000132
(1) 012606 000520
616 012610      000133
(1) 012610 103150
617 012612      000134
(1) 012612 000610
618 012614      000135
(1) 012614 001020
619 012616      000136
(1) 012616 103045
620 012620      000137
(1) 012620 000521
621 012622      000140
(1) 012622 102945
622 012624      000141
(1) 012624 000141

NIDLE2: .SBTTL NIDLE2---NO CSR ACTIVITY STATE
BRWRT  BR,SELB:SP1          ;READ PORT STATUS WORD
MICPC=MICPC+1
<MOVE>WRTBR:BR:SELB:SP1>
BR4    OUTINT
MICPC=MICPC+1
<JUMP>BR4CONI:<OUTINT-INIT&3000*4>:<OUTINT-INIT&777/2>>
SPBR   IBUS,INCON,SP0      ;READ INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE>SPBRX:IBUS:INCON:SP0>
BRSHFT ;SHIFT IT RIGHT
MICPC=MICPC+1
<MOVE>SHFTBR:WRTBR:SELB>
BR4    INWAT1              ;IF ROI SET -- BRANCH
MICPC=MICPC+1
<JUMP>BR4CONI:<INWAT1-INIT&3000*4>:<INWAT1-INIT&777/2>>
;TO RE-READ THE IN CNTRL REGISTER TO AVOID
;A RACE IN MICRO-P READ/UNIBUS WRITE
;READ PORT STATUS
NIDLE6: BRWRT  BR,SELB:SP1
MICPC=MICPC+1
<MOVE>WRTBR:BR:SELB:SP1>
BR0    106
MICPC=MICPC+1
<JUMP>BR0CONI:<106-INIT&3000*4>:<106-INIT&777/2>>
SPBR   IBUS,UB0R,SP0      ;TIMER EXPIRES?
MICPC=MICPC+1
<MOVE>SPBRX:IBUS:UB0R:SP0>
BR4    TIMSRV
MICPC=MICPC+1
<JUMP>BR4CONI:<TIMSRV-INIT&3000*4>:<TIMSRV-INIT&777/2>>
SPBR   IBUS,MODEM,SP0     ;READ MODEM CONTROL CSR
MICPC=MICPC+1
<MOVE>SPBRX:IBUS:MODEM:SP0>
BRWRT  BR,AA:SP0          ;SHIFT IT LEFT
MICPC=MICPC+1
<MOVE>WRTBR:BR:AA:SP0>
BR4    SETDSR              ;IF DSR SET, CLEAR FLAG
MICPC=MICPC+1
<JUMP>BR4CONI:<SETDSR-INIT&3000*4>:<SETDSR-INIT&777/2>>
BRWRT  BR,SELB:SP10       ;READ LINE STATUS WORD
MICPC=MICPC+1
<MOVE>WRTBR:BR:SELB:SP10>
BRSHFT
MICPC=MICPC+1
BR4    IDLE                 ;START MODE
MICPC=MICPC+1
<JUMP>BR4CONI:<IDLE-INIT&3000*4>:<IDLE-INIT&777/2>>
BRWRT  BR,AA:SP1         ;READ PORT STATUS WORD
MICPC=MICPC+1
<MOVE>WRTBR:BR:AA:SP1>
BR1    IDLE                 ;INIT MODE
MICPC=MICPC+1
<JUMP>BR1CONI:<IDLE-INIT&3000*4>:<IDLE-INIT&777/2>>
BR7    IDLE                 ;DISCONNECT ERROR ALREADY SENT
MICPC=MICPC+1

```

(1) 012624 103445  
623 012626 000142  
(1) 012626 123420  
624 012630 000143  
(1) 012630 000400  
625 012632 000144  
(1) 012632 103045  
626 012634 000145  
(1) 012634 000500  
627 012636 000146  
(1) 012636 063301  
628 012640 000147  
(1) 012640 114671  
629 012642 000150  
(1) 012642 000677  
630 012644 000151  
(1) 012644 100652

```
<JUMP!BR7CON!<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>  
SPBR IBUS,MAIN,SP0 ;READ THE MAINT REGISTER  
MICPC=MICPC+1  
<MOVE!SPBRX!IBUS!MAIN!SP0>  
BRWRT BR,ADDISP0 ;SHIFT LEFT  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR!<ADU!SP0>>  
BF4 IDLE ;LU LOOP -- EXIT  
MICPC=MICPC+1  
<JUMP!BR4CON!<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>  
BRWRT IMM,100 ;WRITE DISCONNECT ERROR  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<100>>  
SP BR,AORB,SP1 ;FLAG ERROR RECORDED  
MICPC=MICPC+1  
<MOVE!SPX!BR!AORB!SP1>  
ALWAYS ERRX ;MAKE A CONTROL OUT  
MICPC=MICPC+1  
<JUMP!ALCONDI!<ERRX-INIT63000*4>!<ERRX-INIT6777/2>>  
SETDSR: BRWRT IMM,277 ;CLEAR DISCONNECT ERROR FLAG  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<277>>  
ALWAYS CLRIDL  
MICPC=MICPC+1  
<JUMP!ALCONDI!<CLRIDL-INIT63000*4>!<CLRIDL-INIT6777/2>>
```

637  
638 012646 000152  
(1) 012646 123400  
639 012650 000153  
(1) 012650 060520  
640 012652 000154  
(1) 012652 103557  
641  
642 012654 000155  
(1) 012654 123400  
643 012656 000156  
(1) 012656 103566  
644 012660 000157  
(1) 012660 062555  
645 012662 000160  
(1) 012662 060520  
646 012664 000161  
(1) 012664 117454  
647 012666 000162  
(1) 012666 062552  
648 012670 000163  
(1) 012670 060600  
649 012672 000164  
(1) 012672 061300  
650 012674 000165  
(1) 012674 100445  
651  
652 012676 000166  
(1) 012676 001620  
653 012700 000167  
(1) 012700 103125  
658 012702 000170  
(1) 012702 000171  
(1) 012702 123400  
659 012704 000171  
(1) 012704 102605  
660 012706 000172  
(1) 012706 102177

```
.SBTTL INWAIT---WAIT FOR RQI TO CLEAR  
INWAIT: SPBR IBUS,INCON,SP0 ;READ INPUT CONTROL CSR  
MICPC=MICPC+1  
<MOVE!SPBRX!IBUS!INCON!SP0>  
BRWRT BR,<AA!SP0> ;SHIFT IT LEFT  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR!<AA!SP0>>  
BR7 NIDLE3 ;INTERRUPT ENABLE HAS BEEN SET  
MICPC=MICPC+1  
<JUMP!BR7CON!<NIDLE3-INIT63000*4>!<NIDLE3-INIT6777/2>>  
INWAIT1: SPBR IBUS,INCON,SP0 ;READ THE INPUT CONTROL CSR  
MICPC=MICPC+1  
<MOVE!SPBRX!IBUS!INCON!SP0>  
BR7 INWAIT2 ;READY IN STILL SET  
MICPC=MICPC+1  
<JUMP!BR7CON!<INWAIT2-INIT63000*4>!<INWAIT2-INIT6777/2>>  
NIDLE3: PSTATE INWAIT1 ;UPDATE STATE TO INPUT  
MEM IMM,<<INWAIT1-INIT6777/2>>  
MICPC=MICPC+1  
<MOVE!WRMEM!IMM!<<INWAIT1-INIT6777/2>>>  
BRWRT BR,AA!SP0 ;SHIFT CSR LEFT  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR,<AA!SP0>>  
BR7 ININT  
MICPC=MICPC+1  
<JUMP!BR7CON!<ININT-INIT63000*4>!<ININT-INIT6777/2>>  
PSTATE INWAIT1 ;UPDATE STATE POINTER TO NO INTERRUPT GENERATED  
MEM IMM,<<INWAIT-INIT6777/2>>  
MICPC=MICPC+1  
<MOVE!WRMEM!IMM!<<INWAIT-INIT6777/2>>>  
NIDLE4: BRWRT IMM,200  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<200>>  
OUT BR,AORB!OINCON ;SET THE RDYI  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<AORB!OINCON>>  
ALWAYS IDLE  
MICPC=MICPC+1  
<JUMP!ALCONDI!<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>  
INWAIT2: BRSHFT ;SHIFT THE BR RIGHT  
MICPC=MICPC+1  
<MOVE!SHFTBR!WRTEBR!SELB>  
BR4 NIDLE6 ;RQI SET--- GO AWAY  
MICPC=MICPC+1  
<JUMP!BR4CON!<NIDLE6-INIT63000*4>!<NIDLE6-INIT6777/2>>  
INSRV: SPBR IBUS,INCON,SP0 ;READ THE INPUT CONTROL CSR  
MICPC=MICPC+1  
<MOVE!SPBRX!IBUS!INCON!SP0>  
GR0 308 ;--SENSE OR BASE  
MICPC=MICPC+1  
<JUMP!BR1CON!<308-INIT63000*4>!<308-INIT6777/2>>  
BR0 106 ;CNTL I  
MICPC=MICPC+1  
<JUMP!BR0CON!<106-INIT63000*4>!<106-INIT6777/2>>
```

```

061 012710          BRSHFT                      ;MUST BE BA/CC-SHIFT FOR IN OR OUT
(1) 012710 000173  <MICPC=MICPC+1
(1) 012710 001620  <MOVE<SHFTBR<INWTEBR<SELB>
062 012712          BR1 155
(1) 012712 000174  <MICPC=MICPC+1
(1) 012712 102601  <JUMP<BR<CON<158-INIT<3000*4>1<158-INIT<777/2>>
063 012714          PSTATE TBASRV                ;TRANSMITTER
(1) 012714          MEM IMM,<<TBASRV-INIT<777/2>>
(2) 000175  <MICPC=MICPC+1
(2) 012714 002703  <MOVE<WRMEM<IMM<<TBASRV-INIT<777/2>>>
064 012716          ALWAYS 206
(1) 012716 000176  <MICPC=MICPC+1
(1) 012716 100602  <JUMP<ALCONDI<206-INIT<3000*4>1<206-INIT<777/2>>
065 012720          106: PSTATE CTLSRV
(1) 012720          MEM IMM,<<CTLSRV-INIT<777/2>>
(2) 000177  <MICPC=MICPC+1
(2) 012720 002661  <MOVE<WRMEM<IMM<<CTLSRV-INIT<777/2>>>
066 012722          ALWAYS 206
(1) 012722 100602  <MICPC=MICPC+1
(1) 012722 100602  <JUMP<ALCONDI<206-INIT<3000*4>1<206-INIT<777/2>>
067 012724          158: PSTATE RBASRV
(1) 012724          MEM IMM,<<RBASRV-INIT<777/2>>
(2) 000201  <MICPC=MICPC+1
(2) 012724 002726  <MOVE<WRMEM<IMM<<RBASRV-INIT<777/2>>>
068 012726          206: BRWRT BR,SELA:SP1          ;INIT MODE
(1) 012726 000202  <MICPC=MICPC+1
(1) 012726 000601  <MOVE<WTEBR<BRI<SELA:SP1>>
069 012730          BR0 PROCER                      ;IF INIT MODE--ERROR
(1) 012730 000203  <MICPC=MICPC+1
(1) 012730 102211  <JUMP<BR<CON<PROCER-INIT<3000*4>1<PROCER-INIT<777/2>>
070 012732          ALWAYS IDLE
(1) 012732 000204  <MICPC=MICPC+1
(1) 012732 100445  <JUMP<ALCONDI<IDLE-INIT<3000*4>1<IDLE-INIT<777/2>>
079 012734          306: BR0 356                      ;IF BASE---PROCESS
(1) 012734 000205  <MICPC=MICPC+1
(1) 012734 102207  <JUMP<BR<CON<356-INIT<3000*4>1<356-INIT<777/2>>
080 012736          ALWAYS PROCER
(1) 012736 000206  <MICPC=MICPC+1
(1) 012736 100611  <JUMP<ALCONDI<PROCER-INIT<3000*4>1<PROCER-INIT<777/2>>
081 012740          356: BRWRT BR,SELA:SP1          ;INIT MODE?
(1) 012740 000207  <MICPC=MICPC+1
(1) 012740 000601  <MOVE<WTEBR<BRI<SELA:SP1>>
082 012742          BR0 BASSRV
(1) 012742 000210  <MICPC=MICPC+1
(1) 012742 102056  <JUMP<BR<CON<BASSRV-INIT<3000*4>1<BASSRV-INIT<777/2>>
084 012744          PROCER: BRWRT IMM,100          ;CLEAR INPUT CONTROL CSR
(1) 012744 000211  <MICPC=MICPC+1
(1) 012744 000500  <MOVE<WTEBR<IMM<100>>
085 012746          OUT BR,AANDB<OINCON          ;
(1) 012746 000212  <MICPC=MICPC+1
(1) 012746 001260  <MOVE<WROUT<IBR<AANDB<OINCON>>
086 012750          LDMA IMM,<<RTHRS+3>>          ;ADDRESS ERROR LINK
(1) 012750 000213  <MICPC=MICPC+1
(1) 012750 010177  <MOVE<LDMA<IMM<<RTHRS+3>>6377>>
087 012752          MEMINC IMM,2
(1) 012752 000214  <MICPC=MICPC+1
  
```

```

(1) 012752 016402  <MOVE<WRMEM<INCMAR<IMM<2>>
088 012754          MEM IMM,0
(1) 012754 000215  <MICPC=MICPC+1
(1) 012754 002400  <MOVE<WRMEM<IMM<0>>
089 012756          OUTPUT MEMX,SELB<IOMODEM          ;CLEAR DATA TERMINAL READY
(1) 012756 000216  <MICPC=MICPC+1
(1) 012756 042233  <MOVE<WROUT<MEMX<SELB<IOMODEM>>
090 012760          ALWAYS RCEXX                      ;POST THE ERROR - FATAL
(1) 012760 000217  <MICPC=MICPC+1
(1) 012760 114527  <JUMP<ALCONDI<RCEXX-INIT<3000*4>1<RCEXX-INIT<777/2>>
  
```

692  
693 #12762  
694 C12762  
(1) #12762  
(2) #00220  
(2) #12762 #02654  
700  
701 #12764  
(1) #00221  
(1) #12764 #10240  
702 #12766  
(1) #00222  
(1) #12766 #00220  
703 #12770  
(1) #00223  
(1) #12770 #123040  
704 #12772  
(1) #00224  
(1) #12772 #05302  
705 #12774  
(1) #00225  
(1) #12774 #00220  
706 #12776  
(1) #00226  
(1) #12776 #074520  
707  
708  
709 #13000  
(1) #00227  
(1) #13000 #05224  
710 #13002  
(1) #00230  
(1) #13002 #05225  
711 #13004  
(1) #00231  
(1) #13004 #05227  
712 #13006  
(1) #00232  
(1) #13006 #55226  
713  
714 #13010  
(1) #00233  
(1) #13010 #03760  
715  
721 #13012  
723 #13012  
(1) #00234  
(1) #13012 #10240  
724 #13014  
(1) #00235  
(1) #13014 #043220  
725 #13016  
(1) #00236  
(1) #13016 #02642  
726 #13020  
(1) #00237

```
.SBTTL OUTINT---SET UP OUTPUT INTERRUPT (RDY0)
OUTINT: PSTATE OUTWAIT ;PORT STATUS TO WAITING FOR OUT
MEM IMM,<<OUTWAIT-INIT&777/2>>
NICPC=NICPC+1
<MOVE!WMMEM!IMM!<<OUTWAIT-INIT&777/2>>>
;COMPLETION
LDMA IMM,NXTINT ;ADDRESS OF NEXT INTERRUPT POINTER
NICPC=NICPC+1
<MOVE!LDMAR!IMM!<NXTINT&377>>
LDMA MEMX,SELB ;NEXT INTERRUPT
NICPC=NICPC+1
<MOVE!LDMAR!MEMX!<SELB>>
SP IBUS,0CON,SP0 ;READ THE OUTPUT CONTROL CSR
NICPC=NICPC+1
<MOVE!SFX!IBUS!0CON!SP0>
OUT <MEMX!INCMAR,<<AORB!0CON>> ;WRITE THE OUT CONTROL CSR
NICPC=NICPC+1
<MOVE!WROUTX!MEMX!INCMAR!<AORB!0CON>>
LDMA MEMX,SELB ;ADDRESS LINK
NICPC=NICPC+1
<MOVE!LDMAR!MEMX!<SELB>>
BRWRT <BR!INCMAR,<<AA!SP0>> ;KICK PAST LINK STATUS BYTE
NICPC=NICPC+1
<MOVE!WRTBR!BR!INCMAR!<AA!SP0>>
;SHIFT CSR0 IMAGE LEFT
;***DO NOT CHANGE BR UNTIL BR7***
OUT <MEMX!INCMAR,<<SELB!OPORT1>> ;WRITE LOW BYTE OF BA TO CSR
NICPC=NICPC+1
<MOVE!WROUTX!MEMX!INCMAR!<SELB!OPORT1>>
OUT <MEMX!INCMAR,<<SELB!OPORT2>> ;WRITE HIGH BYTE OF BA TO CSR
NICPC=NICPC+1
<MOVE!WROUTX!MEMX!INCMAR!<SELB!OPORT2>>
OUT <MEMX!INCMAR,<<SELB!OPORT4>> ;WRITE HIGH BYTE OF COUNT TO CSR
NICPC=NICPC+1
<MOVE!WROUTX!MEMX!INCMAR!<SELB!OPORT4>>
OUT <MEMX!INCMAR,<<SELB!OPORT3>> ;WRITE THE LOW BYTE OF COUNT
NICPC=NICPC+1
<MOVE!WROUTX!MEMX!INCMAR!<SELB!OPORT3>>
BR7 PE1 ;***HERE IS BR7***
NICPC=NICPC+1 ;INTERRUPT ENABLE IS SET
<JUMP!BR7CON!<PE1-INIT&3000*4>!<PE1-INIT&777/2>>
;GENERATE AN INTERRUPT
PINT2: LDMA IMM,NXTINT ;ADDRESS NEXT INTERRUPT QUEUE
NICPC=NICPC+1
<MOVE!LDMAR!IMM!<NXTINT&377>>
SP MEMX,SELB,SP0 ;COPY ADDRESS FOR NEXT INT TO SP0
NICPC=NICPC+1
<MOVE!SFX!MEMX!SELB!SP0>
MEM IMM,INTSTK ;ASSUME WRAP AROUND CASE
NICPC=NICPC+1
<MOVE!WMMEM!IMM!<INTSTK>>
BRWRT IMM,<<MMEND-2>> ;ADDRESS OF LAST INT IN STACK
NICPC=NICPC+1
```

(1) #13020 #00776  
727 #13022 #00240  
(1) #13022 #00360  
728 #13024  
(1) #00241  
(1) #13024 #101644  
729 #13026  
(1) #00242  
(1) #13026 #00402  
730 #13030  
(1) #00243  
(1) #13030 #02400  
731 #13032  
(1) #00244  
(1) #13032 #043220  
732 #13034  
(1) #00245  
(1) #13034 #10241  
733 #13036  
(1) #00246  
(1) #13036 #00360  
734 #13040  
(1) #00247  
(1) #13040 #101651  
735 #13042  
(1) #00250  
(1) #13042 #100445  
736 #13044  
(1) #00251  
(1) #13044 #00757  
737 #13046  
(1) #00252  
(1) #13046 #03261  
738 #13050  
(1) #00253  
(1) #13050 #100445

```
<MOVE!WRTBR!IMM!<<MMEND-2>>>
CMP BR,SP0 ;SHOULD WE WRAP
NICPC=NICPC+1
<SUBTC!BR!SP0>
Z SS ;YES--BRANCH
NICPC=NICPC+1
<JUMP!ZCOND!<58-INIT&3000*4>!<58-INIT&777/2>>
BRWRT IMM,2 ;OFFSET FOR NEXT POINTER
NICPC=NICPC+1
<MOVE!WRTBR!IMM!<2>>
MEM BR,ADD!SP0 ;UPDATE POINTER
NICPC=NICPC+1
<MOVE!WMMEM!BR!<ADD!SP0>>
56: SP MEMX,SELB,SP0 ;COPY POINTER TO SP0
NICPC=NICPC+1
<MOVE!SFX!MEMX!SELB!SP0>
LDMA IMM,NXTSP ;PICK UP START OF IN QUEUE
NICPC=NICPC+1
<MOVE!LDMAR!IMM!<NXTSP&377>>
CMP MEMX,SP0 ;COMPARE TO END
NICPC=NICPC+1
<SUBTC!MEMX!SP0>
Z 108 ;IF EQUAL--CLEAR INT PENDING
NICPC=NICPC+1
<JUMP!ZCOND!<108-INIT&3000*4>!<108-INIT&777/2>>
ALWAYS IDLE
NICPC=NICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
108: BRWRT IMM,357 ;MASK TO CLEAR INT PENDING
NICPC=NICPC+1
<MOVE!WRTBR!IMM!<357>>
CLRIDL: SP BR,AAADB,SP1
NICPC=NICPC+1
<MOVE!SFX!BR!AAADB!SP1>
ALWAYS IDLE
NICPC=NICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
```

740  
741 013052 000254  
(1) 013052 123440  
742 013054  
(1) 000255  
(1) 013054 103525  
743 013056  
(1) 000256  
(1) 013056 300500  
744 013060  
(1) 000257  
(1) 013060 961262  
745 013062  
(1) 000260  
(1) 013062 100674

```
.SBTTL OUTWAI--WAIT FOR RDY0 TO GO AWAY
OUTWAI: SPBR IBUS,OCON,SP0 ;READ OUTPUT CONTROL CSR
MICPC=MICPC+1
<MOVEISPBRX:IBUS:OCON:SP0>
BR7 NIDLE6 ;RDY0 SET --GET OUT
MICPC=MICPC+1
<JUMP:BR7CON:INIDLE6-INIT63000*4>I<NIDLE6-INIT6777/2>>
BRWRTE IMM,100 ;CLEAR CONTROL BITS
MICPC=MICPC+1
<MOVE:WTEBR:IMM:100>
OUT BR,OCON:IAANDB
MICPC=MICPC+1
<MOVE:WROUT:IBR:OCON:IAANDB>
ALWAYS INS13
MICPC=MICPC+1
<JUMP:ALCONDI<INS13-INIT63000*4>I<INS13-INIT6777/2>>
```

747  
748 013064 000261  
(1) 013064 123560  
749 013066  
(1) 000262  
(1) 013066 301620  
750 013070  
(1) 000263  
(1) 013070 102755  
751 013072  
(1) 000264  
(1) 013072 300500  
752 013074  
(1) 000265  
(1) 013074 062233  
753 013076  
(1) 000266  
(1) 013076 300600  
754 013100  
(1) 000267  
(1) 013100 062276  
755 013102  
(1) 000270  
(1) 013102 123000  
756 013104  
(1) 000271  
(1) 013104 900500  
757 013106  
(1) 000272  
(1) 013106 061260  
758 013112  
(1) 000273  
(1) 013112 010162  
759 013112  
(2) 000274  
(2) 013112 302520  
760 013114  
(1) 000275  
(1) 013114 100445  
761  
762 013116  
(1) 000276  
(1) 013116 000600  
763 013120  
(1) 000277  
(1) 013120 063301  
764 013122  
(1) 000300  
(1) 013122 000604  
765 013124  
(1) 000301  
(1) 013124 063230  
766 013126  
(1) 000302

```
.SBTTL CTLSRV--CNTL I SERVICE
CTLSRV: SPBR IBUS,PORT4,SP0 ;TO SP0
MICPC=MICPC+1
<MOVE:SPBRX:IBUS:PORT4:SP0>
BRSHFT
MICPC=MICPC+1
<MOVE:SHFTBR:WRTEBR:SELB>
BR1 HDSEL ;IF SET IS HALF DUPLEX
MICPC=MICPC+1
<JUMP:BR1CON:HDSEL-INIT63000*4>I<HDSEL-INIT6777/2>>
BRWRTE IMM,100 ;MASK FOR DTR
MICPC=MICPC+1
<MOVE:WRTEBR:IMM:100>
OUTPUT BR,SELB:IOMODEM ;TURN OFF HALF-DUPLEX
MICPC=MICPC+1
<MOVE:WROUT:IBR:SELB:IOMODEM>
INS11: BRWRTE DP,<SELB:IOMODEM> ;RESTORE THE CNTL WORD
MICPC=MICPC+1
<MOVE:WRTEBR:DP:SELB:IOMODEM>
BR0 CBOOT ;IF SET IS BOOT
MICPC=MICPC+1
<JUMP:BR0CON:CBOOT-INIT63000*4>I<CBOOT-INIT6777/2>>
INS12: SP IBUS,INCON,SP0 ;READ THE INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE:SPX:IBUS:INCON:SP0>
BRWRTE IMM,100 ;ZERO THE BR REGISTER EXCEPT INT ENABLE
MICPC=MICPC+1
<MOVE:WRTEBR:IMM:100>
OUT BR,<AANDB:IOINCON> ;CLEAR IN CONTROL CSR
MICPC=MICPC+1
<MOVE:WROUT:IBR:AANDB:IOINCON>
LDMA IMM,PRST ;ADDRESS PORT STATE
MICPC=MICPC+1
<MOVE:LDMA:IMM:PRST>
INS13: PSTATE NIDLE2
MEM IMM,<<NIDLE2-INIT6777/2>>
MICPC=MICPC+1
<MOVE:WMMEM:IMM:<<NIDLE2-INIT6777/2>>>
ALWAYS IDLE
MICPC=MICPC+1
<JUMP:ALCONDI<IDLE-INIT63000*4>I<IDLE-INIT6777/2>>
;
CBOOT: BRWRTE IMM,200 ;MASK FOR BOOT MODE
MICPC=MICPC+1
<MOVE:WRTEBR:IMM:200>
SP BR,AOR,SP1 ;IN PORT STATUS WORD
MICPC=MICPC+1
<MOVE:SPX:IBR:AOR:SP1>
BRWRTE IMM,204 ;MASK FOR OK TO SEND AND LINE IDLE
MICPC=MICPC+1
<MOVE:WRTEBR:IMM:204>
SP BR,SELB,SP10 ;IN LINE STATUS
MICPC=MICPC+1
<MOVE:SPX:IBR:SELB:SP10>
ALWAYS INS12
MICPC=MICPC+1
```

(1) 013126 100670

<JUMP:ALCOND1<INS12-INIT63000\*4>1<INS12-INIT6777/2>>

768  
769 013130 000303  
(1) 013130 010072  
770 013132 000304  
(1) 013132 053220  
771 013134 000305  
(1) 013134 016401  
772 013136 000306  
(1) 013136 211506  
773  
774 013140 000307  
(1) 013140 136500  
775 013142 000310  
(1) 013142 136520  
776 013144 000311  
(1) 013144 136560  
777 013146 000312  
(1) 013146 136540  
778 013150 000313  
(1) 013150 063000  
779 013152 000314  
(1) 013152 000553  
780 013154 000315  
(1) 013154 010072  
781 013156 000316  
(1) 013156 000360  
782 013160 000317  
(1) 013160 101724  
783 013162 000320  
(1) 013162 002600  
784 013164 000321  
(1) 013164 000402  
785 013166 000322  
(1) 013166 003310  
786 013170 000323  
(1) 013170 100670  
787 013172 000324  
(1) 013172 002471

```
      .SBTTL TBASRV--TRANSMITTER BUFFER ADDRESS SERVICE
TBASRV: LDMA  IMM,ETC ;GET POINTER TO END OF TMT CHAIN
        MICPC=MICPC+1
        <MOVE:LDNAR:IMM1<ETC6377>>
        LDMA  MEMX,<SELB:SPX:SP0> ;FIND THE LINK
        MICPC=MICPC+1
        <MOVE:LDNAR:MEMX1<SELB:SPX:SP0>>
        MEMINC IMM,1 ;BUFFER ASSIGNED IN IN LINK FLAGS
        MICPC=MICPC+1
        <MOVE:W:MEM:INCMAR:IMM1<1>>
        BRWRT <IMM:INCMAR>,6 ;POINT PAST NUMBER FIELD
        MICPC=MICPC+1
        <MOVE:WRT:BR:IMM:INCMAR1<6>> ;SET BR FOR ADDITION TO SP0
        MEMINC IBUS,PORT1
        MICPC=MICPC+1
        <MOVE:W:MEM:INCMAR:IBUS1<PORT1>>
        MEMINC IBUS,PORT2
        MICPC=MICPC+1
        <MOVE:W:MEM:INCMAR:IBUS1<PORT2>>
        MEMINC IBUS,PORT4
        MICPC=MICPC+1
        <MOVE:W:MEM:INCMAR:IBUS1<PORT4>>
        MEMINC IBUS,PORT3
        MICPC=MICPC+1
        <MOVE:W:MEM:INCMAR:IBUS1<PORT3>>
        SP BR,ADD,SP0 ;OFFSET TO NEXT TRANSMIT LINK
        MICPC=MICPC+1
        <MOVE:SPX:BR:ADD:SP0>
        BRWRT IMM,T ;LOAD BR WITH ADDRESS OF CHAIN END
        MICPC=MICPC+1
        <MOVE:WRT:BR:IMM1<T>>
        LDMA  IMM,ETC
        MICPC=MICPC+1
        <MOVE:LDNAR:IMM1<ETC6377>>
        CMP BR,SP0 ;END OF CHAIN?
        MICPC=MICPC+1
        <SUBT:IBR:SP0>
        Z 200 ;IF YES==BRANCH
        MICPC=MICPC+1
        <JUMP:ZCOND1<200-INIT63000*4>1<200-INIT6777/2>>
        MEM BR,SEL:SP0 ;UPDATE THE END POINTER IN MEMORY
        MICPC=MICPC+1
        <MOVE:W:MEM:BR1<SEL:SP0>>
106: BRWRT IMM,2 ;NUMBERED MSG PENDING MASK
        MICPC=MICPC+1
        <MOVE:WRT:BR:IMM1<2>>
        SP BR,AORB,SP10 ;UPDATE LINE STATUS
        MICPC=MICPC+1
        <MOVE:SPX:BR:AORB:SP10>
        ALWAYS INS12
        MICPC=MICPC+1
        <JUMP:ALCOND1<INS12-INIT63000*4>1<INS12-INIT6777/2>>
206: MEM IMM,TM1 ;WRAP IT AROUND
        MICPC=MICPC+1
        <MOVE:W:MEM:IMM1<TM1>>
```



788 013174  
(1) 000325  
(1) 013174 100721

ALWAYS 108 ;CONTINUE PROCESSING  
NICPC=NICPC+1  
<JUMPIALCONDI<108-INIT&3000\*4>1<108-INIT&777/2>>

790 013176  
(1) 000326  
(1) 013176 010023  
792 013200  
(1) 000327  
(1) 013200 053220  
793 013202  
(1) 000330  
(1) 013202 016401  
794 013204  
(1) 000331  
(1) 013204 136500  
795 013206  
(1) 000332  
(1) 013206 136520  
796 013210  
(1) 000333  
(1) 013210 136560  
797 013212  
(1) 000334  
(1) 013212 136540  
798  
799 013214  
(1) 000335  
(1) 013214 210023  
800 013216  
(1) 000336  
(1) 013216 002425  
801 013220  
(1) 000337  
(1) 013220 000463  
802 013222  
(1) 000340  
(1) 013222 000360  
803 013224  
(1) 000341  
(1) 013224 010670  
804 013226  
(1) 000342  
(1) 013226 000405  
805 013230  
(1) 000343  
(1) 013230 262400  
806 013232  
(1) 000344  
(1) 013232 100670  
807 013234  
(1) 000345  
(1) 013234 000717  
808 013236  
(1) 000346  
(1) 013236 063670  
809 013240  
(1) 000347  
(1) 013240 000400

RBASRV: ;SBTTL RBASRV--RECEIVE BUFFER ADDRESS SERVICE  
LDMA IMM,ERC ;ADDRESS END OF RECEIVE CHAIN  
NICPC=NICPC+1  
<MOVEI LDWAR:IMM1<ERC&377>>  
LDMA MEMX,<SELBISPI&SP0> ;GET THE POINTER TO LINK  
NICPC=NICPC+1  
<MOVEI LDWAR:MEMX1<SELBISPI&SP0>>  
MEMINC IMM,1  
NICPC=NICPC+1  
<MOVEI WRMEM:INCMAR:IMM1<1>>  
MEMINC IBUS,PORT1  
NICPC=NICPC+1  
<MOVEI WRMEM:INCMAR:IBUS1<PORT1>>  
MEMINC IBUS,PORT2  
NICPC=NICPC+1  
<MOVEI WRMEM:INCMAR:IBUS1<PORT2>>  
MEMINC IBUS,PORT4  
NICPC=NICPC+1  
<MOVEI WRMEM:INCMAR:IBUS1<PORT4>>  
MEMINC IBUS,PORT3  
NICPC=NICPC+1  
<MOVEI WRMEM:INCMAR:IBUS1<PORT3>>  
;;;NOTE INVERTED ORDER OF PORT 3 AND PORT 4  
LDMA IMM,ERC  
NICPC=NICPC+1  
<MOVEI LDWAR:IMM1<ERC&377>>  
MEM IMM,RCL1 ;ASSUME WRAP AROUND CASE  
NICPC=NICPC+1  
<MOVEI WRMEM:IMM1<RCL1>>  
BRWRT IMM,RCL7 ;GET ADDRESS OF END OF CHAIN AREA  
NICPC=NICPC+1  
<MOVEI WRTEBR:IMM1<RCL7>>  
CMP BR,SP0 ;CHECK FOR END  
NICPC=NICPC+1  
<SUBTCI BR:SP0>  
Z INS12 ;IF EQUAL BRANCH  
NICPC=NICPC+1  
<JUMPIALCONDI<INS12-INIT&3000\*4>1<INS12-INIT&777/2>>  
BRWRT IMM,5 ;CALCULATE ADDRESS OF NEXT LINK  
NICPC=NICPC+1  
<MOVEI WRTEBR:IMM1<5>>  
MEM BR,ADDISP0 ;..  
NICPC=NICPC+1  
<MOVEI WRMEM:IBR1<ADDISP0>>  
ALWAYS INS12 ;EXIT  
NICPC=NICPC+1  
<JUMPIALCONDI<INS12-INIT&3000\*4>1<INS12-INIT&777/2>>  
RA1: BRWRT IMM,317 ;MASK TO CLEAR START MODE AND CLR ACTIVE  
NICPC=NICPC+1  
<MOVEI WRTEBR:IMM1<317>>  
SPBR BR,AAANDB,SP10 ;CLEAR BIT IN LINE STATUS WORD  
NICPC=NICPC+1  
<MOVEI SPBR:IBR1AANDB:SP10>  
RA3: BRWRT IMM,0 ;CLEAR BR  
NICPC=NICPC+1  
<MOVEI WRTEBR:IMM1<0>>

810 013242  
(1) 000350  
(1) 013242 063233  
811 013244  
(1) 000351  
(1) 013244 000424  
812 013246  
(1) 000352  
(1) 013246 104422  
813  
814 013250  
(1) 000353  
(1) 013250 000402  
815 013252  
(1) 000354  
(1) 013252 114671  
816

```
SP BR,SELB,SP13 ;SET NUMB MESSAGE TYPE IN SP13
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP13>
STATE RCVB ;CHANGE RECEIVE STATE POINTER TO STATE B
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<RCVB-INIT&777/2>>
ALWAYS REXIT
MICPC=MICPC+1
<JUMPIALCONDI<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
;
RTHRES: BRWRTE IMM,2
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<2>>
ALWAYS ERRXX
MICPC=MICPC+1
<JUMPIALCONDI<ERRXX-INIT&3000*4>!<ERRXX-INIT&777/2>>
;
```

830 013254  
(1) 000355  
(1) 013254 000500  
831 013256  
(1) 000356  
(1) 013256 063310  
832 013260  
(1) 000357  
(1) 013260 100666  
833  
834 013262  
(1) 000360  
(1) 013262 000700  
835 013264  
(1) 000361  
(1) 013264 123220  
836 013266  
(1) 000362  
(1) 013266 061311  
841 013270  
(1) 000363  
(1) 013270 100634  
843  
844 013272  
(1) 000364  
(1) 013272 002730  
845  
846 013274  
(1) 000365  
(1) 013274 000402  
847 013276  
(1) 000366  
(1) 013276 061231  
848 013300  
(1) 000367  
(1) 013300 120620  
849 013302  
(1) 000370  
(1) 013302 132767  
850 013304  
(1) 000371  
(1) 013304 154620  
851 013306  
(1) 000372  
(1) 013306 120620  
852 013310  
(1) 000373  
(1) 013310 103364  
853 013312  
(1) 000374  
(1) 013312 114733  
854  
855 013314  
(1) 000375  
(1) 013314 170630  
856 013316

```
HDEL: BRWRTE IMM,100 ;HD MASK TO BR
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<100>>
SP BR,AORB,SP10 ;UPDATE PORT STATUS WORD
MICPC=MICPC+1
<MOVE!SPX!BR!AORB!SP10>
ALWAYS IN511
MICPC=MICPC+1
<JUMPIALCONDI<INS11-INIT&3000*4>!<INS11-INIT&777/2>>
;
PEI: BRWRTE IMM,300 ;MASK FOR INTERRUPT AND VECTOR THROUGH X04
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<300>>
SP IBUS,UBBR,SP0 ;READ BR CONTROL REG
MICPC=MICPC+1
<MOVE!SPX!IBUS!UBBR!SP0>
OUT BR,<AORB!OBR> ;INTERRUPT
MICPC=MICPC+1
<MOVE!WROUTX!BR!<AORB!OBR>>
ALWAYS PINT2
MICPC=MICPC+1
<JUMPIALCONDI<PINT2-INIT&3000*4>!<PINT2-INIT&777/2>>
;
HALTED: MEMADR EM6
MICPC=MICPC+1
<MOVE!WRMEM!<EM6-INIT&777/2>>
;FALL INTO ACLOW
;CAUSE AN AC LOW
ACLOW: BRWRTE IMM,2
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<2>>
OUT BR,<SELB!OBR>
MICPC=MICPC+1
<MOVE!WROUTX!BR!<SELB!OBR>>
;WAIT FOR IT TO COMPLETE
5S: BRWRTE IBUS,UBBR
MICPC=MICPC+1
<MOVE!WRTEBR!IBUS!<UBBR>>
BR1 5S
MICPC=MICPC+1
<JUMPIBR1CONI<5S-INIT&3000*4>!<5S-INIT&777/2>>
;ALWAY MEMX,SELB,PAGE3
MICPC=MICPC+1
<JUMPIALCONDI<MEMX!SELB!PAGE3>
;READ BR CONTROL REG
CKTIME: BRWRTE IBUS,UBBR
MICPC=MICPC+1
<MOVE!WRTEBR!IBUS!<UBBR>>
BR4 HALTED
MICPC=MICPC+1
<JUMPIBR4CONI<HALTED-INIT&3000*4>!<HALTED-INIT&777/2>>
ALWAYS EM1
MICPC=MICPC+1
<JUMPIALCONDI<EM1-INIT&3000*4>!<EM1-INIT&777/2>>
;
TRUI: BRWRTE IBUS,NPR
MICPC=MICPC+1
<MOVE!WRTEBR!IBUS!<NPR>>
BR0 IDLE
```

(1) 000376  
(1) 013316 102045  
857 013320  
(1) 000377  
(1) 013320 114760  
858

MICPC=MICPC+1  
<JUMP:BR0CONI<IDLE-INIT&3000\*4>!<IDLE-INIT&777/2>>  
ALWAYS EC2  
MICPC=MICPC+1  
<JUMPIALCOND!<EC2-INIT&3000\*4>!<EC2-INIT&777/2>>

860 013322  
861 000377  
862  
863  
864  
865  
866 013322  
(1) 000400  
(1) 013322 023200  
867 013324  
(1) 000401  
(1) 013324 060601  
868 013326  
(1) 000402  
(1) 013326 106012  
869 013330  
(1) 000403  
(1) 013330 107412  
870 013332  
(1) 000404  
(1) 013332 000601  
871 013334  
(1) 000405  
(1) 013334 060360  
872 013336  
(1) 000406  
(1) 013336 107445  
873 013340  
(1) 000407  
(1) 013340 000405  
874 013342  
(1) 000410  
(1) 013342 000360  
875 013344  
(1) 000411  
(1) 013344 105421  
876 013346  
(1) 000412  
(1) 013346 000620  
877 013350  
(1) 000413  
(1) 013350 060360  
878 013352  
(1) 000414  
(1) 013352 105762  
879 013354  
(1) 000415  
(1) 013354 002212  
880 013356  
(1) 000416  
(1) 013356 000757  
881 013360  
(1) 000417  
(1) 013360 063274  
882 013362  
(1) 000418

RCVA:  
RCVA: SP IBUS,RCVDAT,SP0 ;READ RECEIVE CHARACTER TO SP0  
MICPC=MICPC+1  
<MOVE:SPXIBUS:RCVDAT:SP0>  
BRWRT BR,SELA:SP1 ;READ PORT STATUS WORD  
MICPC=MICPC+1  
<MOVE:WRTBR:BR:SELA:SP1>  
BR0 50 ;IF INIT MODE---ONLY BOOT OK  
MICPC=MICPC+1  
<JUMPIBR0CONI<50-INIT&3000\*4>!<50-INIT&777/2>>  
BR7 50 ;IF BOOT MODE---ONLY BOOT OK  
MICPC=MICPC+1  
<JUMPIBR7CONI<50-INIT&3000\*4>!<50-INIT&777/2>>  
BRWRT IMM,201 ;SOH TO BR  
MICPC=MICPC+1  
<MOVE:WRTBR:IMM:201>  
CMP BR,SP0 ;COMPARE BR TO SP0  
MICPC=MICPC+1  
<SUBTC:BR:SP0>  
Z RA1 ;IF EQUAL-IS NUMBERED MESSAGE  
MICPC=MICPC+1  
<JUMPIZCONDI<RA1-INIT&3000\*4>!<RA1-INIT&777/2>>  
BRWRT IMM,5 ;ENQ TO BR  
MICPC=MICPC+1  
<MOVE:WRTBR:IMM:5>  
CMP BR,SP0 ;COMPARE ENQ TO SP0  
MICPC=MICPC+1  
<SUBTC:BR:SP0>  
Z RA2 ;IF EQUAL-IS UNNUMBERED MESSAGE  
MICPC=MICPC+1  
<JUMPIZCONDI<RA2-INIT&3000\*4>!<RA2-INIT&777/2>>  
50: BRWRT IMM,220 ;DLE TO BR  
MICPC=MICPC+1  
<MOVE:WRTBR:IMM:220>  
CMP BR,SP0 ;COMPARE DLE TO SP0  
MICPC=MICPC+1  
<SUBTC:BR:SP0>  
Z BOOT ;IF EQUAL IS BOOT  
MICPC=MICPC+1  
<JUMPIZCONDI<BOOT-INIT&3000\*4>!<BOOT-INIT&777/2>>  
FLUSH: OUTPUT IMM,<200:ORCVCO> ;FLUSH THE INPUT SILO  
MICPC=MICPC+1  
<MOVE:WROUT:IMM:<200:ORCVCO>>  
BRWRT IMM,357 ;MASK TO CLEAR--CLEAR ACTIVE  
MICPC=MICPC+1  
<MOVE:WRTBR:IMM:357>  
SP BR,AANDR,SP10 ;IN LINE STATUS WORD  
MICPC=MICPC+1  
<MOVE:SP:XIBR:AANDR:SP10>  
ALWAYS RM1 ;SET STATE TO RCVA AND RETURN TO IDLE  
MICPC=MICPC+1

(1) 013362 114662  
003 013364  
(1) 030421  
(1) 013364 000700  
008 013366  
(1) 000422  
(1) 013366 063223  
009 013370  
(1) 000423  
(1) 013370 100445

RA2: <JUMPIALCONDI<RM1-INIT&3000\*4>1<RM1-INIT&777/2>>  
STATE RCVI ;CHANGE RECEIVE STATE TO 1  
MICPC=MICPC+1  
<MOVE!WRTEBRIIMMI<RCVI-INIT&777/2>>  
REXIT: SP BR,SELB,SP3  
MICPC=MICPC+1  
<MOVE!SPXIBRISELB!SP3>  
ALWAYS IDLE  
MICPC=MICPC+1  
<JUMPIALCONDI<IDLE-INIT&3000\*4>1<IDLE-INIT&777/2>>

092  
093  
094  
095  
096 013372  
097 013372  
(1) 000424  
(1) 013372 023204  
098 013374  
(1) 000425  
(1) 013374 010024  
099 013376  
(1) 000426  
(1) 013376 053234  
000  
001 013400  
(1) 000427  
(1) 013400 054620  
002 013402  
(1) 000430  
(1) 013402 106042  
003 013404  
(1) 000431  
(1) 013404 000601  
004 013406  
(1) 000432  
(1) 013406 107440  
005 013410  
(1) 000433  
(1) 013410 010153  
006 013412  
(1) 000434  
(1) 013412 016402  
007 013414  
(1) 000435  
(1) 013414 002710  
008 013416  
(1) 000436  
(1) 013416 010012  
009 013420  
(1) 000437  
(1) 013420 104557  
010 013422  
(1) 000440  
(1) 013422 000104  
011 013424  
(1) 002441  
(1) 013424 003301  
012 013426  
(1) 000442  
(1) 013426 000462  
013 013430  
(1) 000443  
(1) 013430 063223  
014 013432  
(1) 000444

.SBTTL RCVB--ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD  
;ENTERED FROM IDLE LOOP  
;STORES COUNT FIELD AND SETS UP RCVI AS NEXT STATE  
;  
RCVB: SP IBUS,RCVDAT,SP4 ;READ CHARACTER TO SP4  
MICPC=MICPC+1  
<MOVE!SPXIBUS!RCVDAT!SP4>  
LDNA IMM,LRC ;LOAD ADDRESS OF START OF RECV CHAIN  
MICPC=MICPC+1  
<MOVE!LDNARIIMMI<LRC&377>>  
SP MEMX!LDNAR,SELB,SP14 ;COPY POINTER TO SP14  
MICPC=MICPC+1  
<MOVE!SPXIMEMX!LDNAR!SELB!SP14>  
;AND LOAD MAR WITH ADDRESS OF CURRENT BA  
BRWRTE MEMX,INCMAR!SELB ;READ FLAGS BYTE  
MICPC=MICPC+1  
<MOVE!WRTEBRIIMMI<INCMAR!SELB>>  
;RCV BUFFER ASSIGNED---CONTINUE  
BR0 RB1  
MICPC=MICPC+1  
<JUMPIBR7CONI<RB3-INIT&3000\*4>1<RB3-INIT&777/2>>  
BRWRTE BR,SELA!SP1 ;READ STATUS BYTE  
MICPC=MICPC+1  
<MOVE!WRTEBRIIMMI<SELA!SP1>>  
;MAINT MODE  
BR7 RB3  
MICPC=MICPC+1  
<JUMPIBR7CONI<RB3-INIT&3000\*4>1<RB3-INIT&777/2>>  
LDNA IMM,T ;ERROR--LOAD TYPE FIELD ADDRESS IN MAR  
MICPC=MICPC+1  
<MOVE!LDNARIIMMI<T&377>>  
MEMINC IMM,2 ;LOAD NAK TYPE  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IMMI<2>>  
;LOAD SUB-TYPE NO BUFFERS  
MEM IMM,310  
MICPC=MICPC+1  
<MOVE!WRMEM!IMMI<310>>  
LDNA IMM,NTLS  
MICPC=MICPC+1  
<MOVE!LDNARIIMMI<NTLS&377>>  
ALWAYS RH5 ;BRANCH TO SEND NAK ROUTINE  
MICPC=MICPC+1  
<JUMPIALCONDI<RH5-INIT&3000\*4>1<RH5-INIT&777/2>>  
BRWRTE IMM,4 ;MASK FOR NO BUFFER AVAILABLE  
MICPC=MICPC+1  
<MOVE!WRTEBRIIMMI<4>>  
SP BR,AORB,SP1 ;SET THE FLAG  
MICPC=MICPC+1  
<MOVE!SPXIBRI!AORB!SP1>  
RB3: STATE RCVI  
MICPC=MICPC+1  
<MOVE!WRTEBRIIMMI<RCVC-INIT&777/2>>  
RB0: SP BR,SELB,SP3  
MICPC=MICPC+1  
<MOVE!SPXIBRI!SELB!SP3>  
OUTPUT <MEMX!INCMAR>,SELB!OBA1 ;OUTPUT LOW ORDER BYTE OF ADDRESS  
MICPC=MICPC+1

(1) 013432 056226  
915 013434 200445  
(1) 013434 056227  
916 013436  
(1) 000446  
(1) 013436 123220  
917 013440  
(1) 000447  
(1) 013440 000501  
918 013442  
(1) 000450  
(1) 013442 063260  
919 013444  
(1) 000451  
(1) 013444 003305  
920  
921  
922 013446  
(1) 000452  
(1) 013446 040665  
923 013450  
(1) 000453  
(1) 013450 001020  
924 013452  
(1) 000454  
(1) 013452 001020  
925 013454  
(1) 000455  
(1) 013454 001020  
926 013456  
(1) 000456  
(1) 013456 001020  
927 013460  
(1) 000457  
(1) 013460 061311  
928 013462  
(1) 000460  
(1) 013462 100445  
929 013464  
(1) 000461  
(1) 013464 100454

```
<MOVE!WROUT!MEMX!INCMAR!<SELB!OBA1>>  
OUTPUT MEMX!INCMAR,<SELB!OBA2>;OUTPUT HIGH BYTE OF ADDRESS  
MICPC=MICPC+1  
<MOVE!WROUT!MEMX!INCMAR!<SELB!OBA2>>  
SP IBUS,UBBR,SP0 ;READ THE BUS REQ REGISTER  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!UBBR!SP0>  
BRWRT IMM,101 ;MASK OFF ALL BUT HXM AND VEC4 BITS  
MICPC=MICPC+1  
<MOVE!WRTBR!IMM!<101>>  
SP BR, AANDB,SP0 ;AND SAVE IN SP0  
MICPC=MICPC+1  
<MOVE!SPX!BR!AANDB!SP0>  
SP IMM,300,SP5 ;MASK TO ISOLATE EX, MEM BITS  
MICPC=MICPC+1  
<MOVE!SPX!IMM!300!SP5>  
  
BRWRT MEMX,AANDB!SP5 ;NOTE THIS REALLY WRITES A 305 BUT THE  
MICPC=MICPC+1 ;5 GETS SHIFTED OUT  
<MOVE!WRTBR!MEMX!<AANDB!SP5>> ;MASK ALL BUT EX, MEM BITS  
BRSHFT ;SHIFT THEM INTO THE CORRECT POSITION  
MICPC=MICPC+1  
<MOVE!SHFTBR!WRTBR!SELB>  
BRSHFT  
MICPC=MICPC+1  
<MOVE!SHFTBR!WRTBR!SELB>  
BRSHFT  
MICPC=MICPC+1  
<MOVE!SHFTBR!WRTBR!SELB>  
BRSHFT  
MICPC=MICPC+1  
<MOVE!SHFTBR!WRTBR!SELB>  
BRSHFT  
MICPC=MICPC+1  
OUT BR,AORBIOR ;WRITE EX MEM BITS OUT  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<AORBIOR>>  
ALWAYS IDLE  
MICPC=MICPC+1  
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>  
RB2: ALWAYS I2  
MICPC=MICPC+1  
<JUMP!ALCOND!<I2-INIT&3000*4>!<I2-INIT&777/2>>
```

931  
932  
933  
934  
935  
936 013466  
(1) 000462  
(1) 013466 114470  
937 013470  
(1) 000463  
(1) 013470 070214  
938 013472  
(1) 000464  
(1) 013472 074001  
939 013474  
(1) 000465  
(1) 013474 015620  
940 013476  
(1) 000466  
(1) 013476 106475  
941 013500  
(1) 000467  
(1) 013500 014477  
942 013502  
(1) 000470  
(1) 013502 057220  
943 013504  
(1) 000471  
(1) 013504 060660  
944 013506  
(1) 000472  
(1) 013506 060305  
945 013510  
(1) 000473  
(1) 013510 115116  
946 013512  
(1) 000474  
(1) 013512 115513  
947 013514  
(1) 000475  
(1) 013514 000477  
948 013516  
(1) 000476  
(1) 013516 104422

```
.SBTTL RCVC--ROUTINE TO HANDLE SECOND CHARACTER OF COUNT FIELD, SELECT AND FINA  
;ENTERED FROM IDLE LOOP  
;INTERPRETS SELECT AND FINAL  
;CHECKS FOR COUNT TOO LARGE  
;  
RCVC: ALWAYS SELQSY ;"CALL" SELECT/QSYNC SUBROUTINE  
MICPC=MICPC+1  
<JUMP!ALCOND!<SELQSY-INIT&3000*4>!<SELQSY-INIT&777/2>>  
LDMA BR,<SEL!SP14> ;LOAD ADDRESS OF CURRENT COUNT  
MICPC=MICPC+1  
<MOVE!LDMAR!BR!<SEL!SP14>>  
BRWRT BR,INCMAR,SEL!SP1 ;READ STATUS BYTE  
MICPC=MICPC+1  
<MOVE!WRTBR!BR!INCMAR!<SEL!SP1>>  
BRWRT SHFTBR!INCMAR,SELB ;SHIFT IT RIGHT  
MICPC=MICPC+1  
<MOVE!WRTBR!SHFTBR!INCMAR!<SELB>>  
BR1 RCS ;NO BUFFER ASSIGNED IN MAINT MODE  
MICPC=MICPC+1  
<JUMP!BRCON!<RCS-INIT&3000*4>!<RCS-INIT&777/2>>  
BRWRT IMM!INCMAR,77 ;MASK FOR COUNT BITS  
MICPC=MICPC+1  
<MOVE!WRTBR!IMM!INCMAR!<77>>  
SP MEMX!INCMAR,SELB,SP0 ;COPY HIGH BYTE OF COUNT TO SP0  
MICPC=MICPC+1  
<MOVE!SPX!MEMX!INCMAR!SELB!SP0>  
BRWRT BR,AANDB!SP0 ;MASK TO BR  
MICPC=MICPC+1  
<MOVE!WRTBR!BR!<AANDB!SP0>>  
CMP BR,SP5 ;COMPARE HIGH ORDER BITS OF COUNT  
MICPC=MICPC+1  
<SUBTC!BR!SP5>  
C RCFATL ;IF CARRY--TOO BIG ERROR  
MICPC=MICPC+1  
<JUMP!ICOND!<RCFATL-INIT&3000*4>!<RCFATL-INIT&777/2>>  
Z RCLW ;IF EQUAL COMPARE LOW ORDER BITS OF COUNT  
MICPC=MICPC+1  
<JUMP!ICOND!<RCLW-INIT&3000*4>!<RCLW-INIT&777/2>>  
RC5: STATE RCVD ;SET NEXT STATE TO D  
MICPC=MICPC+1  
<MOVE!WRTBR!IMM!<RCVD-INIT&777/2>>  
ALWAYS REXIT  
MICPC=MICPC+1  
<JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
```

950  
951  
952 013520 000477  
(1) 013520 063164  
953 013522 000500  
(1) 013522 105102  
954 013524 000501  
(1) 013524 063165  
955 013526 000502  
(1) 013526 000523  
956 013530 000503  
(1) 013530 063223  
957 013532 000504  
(1) 013532 023600  
958 013534 000505  
(1) 013534 060757  
959 013536 000506  
(1) 013536 107510  
960 013540 000507  
(1) 013540 100445  
961 013542 000510  
(1) 013542 000510  
962 013544 000511  
(1) 013544 103445  
963 013546 000512  
(1) 013546 060610  
964 013550 000513  
(1) 013550 001620  
965 013552 000514  
(1) 013552 103045  
966 013554 000515  
(1) 013554 010155  
967 013556 000516  
(1) 013556 062600  
968 013560 000517  
(1) 013560 010403  
969  
970 013562 000520  
(1)

```

.SBTTL RCVD--ROUTINE TO HANDLE RESPONSE FIELD FOR NUMBERED MESSAGES
;
RCVD: SP BR,DECA,SP4 ;DECREMENT LOW BYTE OF COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP4>
      C RD3 ;NO OVERFLOW
      MICPC=MICPC+1
      <JUMP!CONDI!<RD3-INIT&3000*4>!<RD3-INIT&777/2>>
      SP BR,DECA,SP5 ;OVERFLOW - DECREMENT HIGH BYTE
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP5>
RD3: STATE RCVE
      MICPC=MICPC+1
      <MOVE!WFTBR!IMM!<RCVE-INIT&777/2>>
RD2: SP BR,SELB,SP3 ;SAVE THE STATE
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP3>
      SPBR IBUS,RCVDAT,SP0 ;INPUT THE CHARACTER
      MICPC=MICPC+1
      <MOVE!SPBRX!IBUS!RCVDAT!SP0>
      BRWRT BR,SUB!SP17 ;COMPARE NEW R TO LAST R
      MICPC=MICPC+1
      <MOVE!WRTBR!BR!<SUB!SP17>>
      BR7 106 ;IF NEW IS GREATER---PROCESS
      MICPC=MICPC+1
      <JUMP!BR7CON!<106-INIT&3000*4>!<106-INIT&777/2>>
      ALWAYS IDLE
      MICPC=MICPC+1
106: <JUMP!ALCONDI!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
      BRWRT BR,SEL!SP1 ;READ STATUS BYTE
      MICPC=MICPC+1
      <MOVE!WRTBR!BR!<SEL!SP1>>
      BR7 IDLE ;MAINT. MODE - GET OUT
      MICPC=MICPC+1
      <JUMP!BR7CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
      BRWRT BR,SEL!SP10
      MICPC=MICPC+1
      <MOVE!WRTBR!BR!<SEL!SP10>>
      BRSHFT
      MICPC=MICPC+1
      <MOVE!SHFTBR!WRTBR!SELB>
      BR4 IDLE
      MICPC=MICPC+1
      <JUMP!BR4CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
      LDMA IMM,ISP17 ;ADDRESS LAST ACKED IMAGE
      MICPC=MICPC+1
      <MOVE!LDMAR!IMM!<ISP17&377>>
      MEM BR,SEL!SP0 ;COPY THE CHAR
      MICPC=MICPC+1
      <MOVE!WPMEM!BR!<SEL!SP0>>
RD5: BRWRT IMM,REPST!LDMAR ;SET UP COUNT FOR TIMER
      MICPC=MICPC+1
      <MOVE!WFTBR!IMM!<REPST!LDMAR>>
      MEM IMM,1 ;****DEPENDENT ON REPST = 2
      MICPC=MICPC+1 ;RESET REP THRESHOLD

```

(1) 013562 002401  
971 013564 000521  
(1) 013564 063235  
972 013566 000522  
(1) 013566 100445

```

      <MOVE!WPMEM!IMM!<1>>
      SP BR,SELB,SP15 ;RESET THE COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP15>
      ALWAYS IDLE
      MICPC=MICPC+1
      <JUMP!ALCONDI!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

```

974  
975  
976 013570 000523  
(1) 013570 060601  
977 013572 000524  
(1) 013572 107713  
978 013574 000525  
(1) 013574 020600  
979 013576 000526  
(1) 013576 060371  
980 013600 000527  
(1) 013600 105532  
981 013602 000530  
(1) 013602 063173  
982 013604 000531  
(1) 013604 104533  
983 013606 000532  
(1) 013606 063071  
984 013610 000533  
(1) 013610 000535  
985 013612 000534  
(1) 013612 104422

```
.SBTTL RCVE--ROUTINE TO HANDLE N FIELD OF NUMBERED MESSAGE
;
RCVE: BRWRT BR,SELA:SP1 ;READ THE STATUS BYTE
      MICPC=MICPC+1
      <MOVEIWRTEBRIBR!<SELA:SP1>>
      BR7 RCVQ
      MICPC=MICPC+1
      <JUMPIBR7CON!<RCVQ-INIT&3000*4>!<RCVQ-INIT&777/2>>
      BRWRT IBUS,RCVDAT ;INPUT THE CHARACTER
      MICPC=MICPC+1
      <MOVEIWRTEBRIBUS!<RCVDAT>>
      CMP BR,SP11
      MICPC=MICPC+1
      <SUBTCIBR!SP11>
      Z 55
      MICPC=MICPC+1
      <JUMPIZCOND!<55-INIT&3000*4>!<55-INIT&777/2>>
      SP BR,DECA,SP13 ;FORCE MSG TYPE TO -1
      MICPC=MICPC+1
      <MOVEISPXIBRIDECA!SP13>
      ALWAYS RE2
      MICPC=MICPC+1
      <JUMPIALCOND!<RE2-INIT&3000*4>!<RE2-INIT&777/2>>
      SP BR,INCA,SP11 ;UPDATE R FIELD
      MICPC=MICPC+1
      <MOVEISPXIBRIDECA!SP11>
      RE2: STATE RCVF ;NEXT RECEIVE STATE IS F
           MICPC=MICPC+1
           <MOVEIWRTEBRIMM!<RCVF-INIT&777/2>>
           ALWAYS REXIT
           MICPC=MICPC+1
           <JUMPIALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
```

987  
988 013614 000535  
(1) 013614 000540  
989 013616 000536  
(1) 013616 020200  
990 013620 000537  
(1) 013620 104422  
991  
992  
993  
994 013622 000540  
(1) 013622 000542  
995 013624 000541  
(1) 013624 104536

```
.SBTTL RCVF--ROUTINE TO IGNORE ADDRESS
;
RCVF: STATE RCVG
      MICPC=MICPC+1
      <MOVEIWRTEBRIMMI!<RCVG-INIT&777/2>>
      RCVF1: NOP IBUS,RCVDAT,0 ;INPUT CHARACTER - AND DISCARD
            MICPC=MICPC+1
            <IBUS!RCVDAT!0>
            ALWAYS REXIT
            MICPC=MICPC+1
            <JUMPIALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
            ;
            .SBTTL RCVG--ROUTINE TO IGNORE CRC1
            ;
            RCVG: STATE RCVH ;NEXT STATE IS RCVH
                  MICPC=MICPC+1
                  <MOVEIWRTEBRIMMI!<RCVH-INIT&777/2>>
                  ALWAYS RCVF1
                  MICPC=MICPC+1
                  <JUMPIALCOND!<RCVF1-INIT&3000*4>!<RCVF1-INIT&777/2>>
```

```

997
998
999 013626
1000 013626
(1) 000542
(1) 013626 023200
1001 013634
(1) 000543
(1) 013630 020640
1002 013632
(1) 000544
(1) 013632 116167
1003 013634
(1) 000545
(1) 013634 000001
1004 013635
(1) 000546
(1) 013636 107751
1005 013640
(1) 000547
(1) 013640 000610
1006 013642
(1) 000550
(1) 013642 001620
1007 013644
(1) 000551
(1) 013644 117315
1008 013646
(1) 000552
(1) 013646 010153
1009 013650
(1) 000553
(1) 013650 016402
1010 013652
(1) 000554
(1) 013652 016701
1011 013654
(1) 000555
(1) 013654 002617
1012 013656
(1) 000556
(1) 013656 010013
1013 013660
(1) 000557
(1) 013660 043220
1014 013662
(1) 000560
(1) 013662 062460
1015 013664
(1) 000561
(1) 013664 010001
1016 013666
(1) 000562
(1) 013666 040620
1017 013670
(1) 000563

```

```

.SBTTL RCVH--ROUTINE TO HANDLE CRC2 AND TO DISPATCH NUMBERED AND UNNUMBERED TYP
;
RCVH:
SP IBUS,RCVDAT,SP0 ;GET CHAR IN SP0
MICPC=MICPC+1
<MOVE!SPX!IBUS!RCVDAT!SP0>
BRWRT E IBUS,RCVCON ;READ RECVR CONTROL REGISTER
MICPC=MICPC+1
<MOVE!WRTBR!IBUS!<RCVCON>>
BR0 TDON1 ;IF BCC MATCH SET CRC IS GOOD
MICPC=MICPC+1
<JUMP!BR0CON!<TDON1-INIT63000*4>!<TDON1-INIT6777/2>>
BRWRT E BR,SELA!SP1 ;READ STATUS BYTE
MICPC=MICPC+1
<MOVE!WRTBR!BR!<SELA!SP1>>
BR7 RHX ;MAINT MODE
MICPC=MICPC+1
<JUMP!BR7CON!<RHX-INIT63000*4>!<RHX-INIT6777/2>>
BRWRT E DP,<SELA!SP10> ;READ PORT STATUS WORD TO BR
MICPC=MICPC+1
<MOVE!WRTBR!DP!<SELA!SP10>>
BRSHFT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTBR!SELB>
BR4 SNAK1 ;IF START MODE--PROCEED TO RESEND START
MICPC=MICPC+1
<JUMP!BR4CON!<SNAK1-INIT63000*4>!<SNAK1-INIT6777/2>>
LDNA IMM,7 ;ELSE BCC ERROR--LOAD ADDRESS OF TYPE FI
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<T6377>>
MEMINC IMM,2 ;WRITE NAK TYPE
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IMM!<2>>
MEMINC IMM,301 ;WRITE HEADER BCC ERROR SUBTYPE
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IMM!<301>>
MEM BR,SELA!SP17 ;RESTORE LAST ACKED IMAGE
MICPC=MICPC+1
<MOVE!WRMEM!BR!<SELA!SP17>>
LDNA IMM,NHDS ;ADDRESS CUM ERROR COUNTER
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<NHDS6377>>
RHS: SP MEMX,SELB,SP0 ;WRITE IT TO SP0
MICPC=MICPC+1
<MOVE!SPX!MEMX!SELB!SP0>
MEM BR,INCA!SP0 ;INCREMENT IT
MICPC=MICPC+1
<MOVE!WRMEM!BR!<INCA!SP0>>
LDNA IMM,NAKST ;ADDRESS NAKS TMTED DYNAMIC
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<NAKST6377>>
BRWRT E MEMX,SELB ;WRITE IT TO BR
MICPC=MICPC+1
<MOVE!WRTBR!MEMX!<SELB>>
BRSHFTB ;SHIFT IT RIGHT
MICPC=MICPC+1

```

```

(1) 013670 061620
1018 013672
(1) 000564
(1) 013672 002620
1019 013674
(1) 000565
(1) 013674 116204
1020 013676
(1) 000566
(1) 013676 114712
1021 013700
(1) 000567
(1) 013700 000573
1022 013702
(1) 000570
(1) 013702 115505
1023 013704
(1) 000571
(1) 013704 000400
(1) 000572
(1) 013706 003223
1024 013710
(1) 000573
(1) 013710 000610
1025 013712
(1) 000574
(1) 013712 117040
1026 013714
(1) 000575
(1) 013714 001620
1027 013716
(1) 000576
(1) 013716 107204
1028 013720
(1) 000577
(1) 013720 010103
1029 013722
(1) 000600
(1) 013722 054373
1030 013724
(1) 000601
(1) 013724 115404
1031 013726
(1) 000602
(1) 013726 054373
1032 013730
(1) 000603
(1) 013730 115443
1033 013732
(1) 000604
(1) 013732 010103
1034 013734
(1) 000605
(1) 013734 054373
1035 013736
(1) 000606

```

```

<MOVE!SHFTBR!SELB!BR>
MEM BR,SELB ;UPDATE IT
MICPC=MICPC+1
<MOVE!WRMEM!BR!<SELB>>
BR0 NTHRES ;BRANCH IF THRESHOLD EXCEEDED
MICPC=MICPC+1
<JUMP!BR0CON!<NTHRES-INIT63000*4>!<NTHRES-INIT6777/2>>
ALWAYS SNAK
MICPC=MICPC+1
<JUMP!ALCONDI!<SNAK-INIT63000*4>!<SNAK-INIT6777/2>>
BRWRT E DP,<DECA!SP13> ;LOAD TYPE RECEIVED--DECREMENTING
MICPC=MICPC+1
<MOVE!WRTBR!DP!<DECA!SP13>>
Z RH1 ;IF ALUOUT IS ALL ONES IS NUMBERED MSG
MICPC=MICPC+1
<JUMP!ZCONDI!<RH1-INIT63000*4>!<RH1-INIT6777/2>>
RSTATE RCVA
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<RCVA-INIT6777/2>>
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP3>
BRWRT E DP,<SELA!SP10> ;LOAD LINE STATUS WORD IN BR
MICPC=MICPC+1
<MOVE!WRTBR!DP!<SELA!SP10>>
BR4 FLUSH1
MICPC=MICPC+1
<JUMP!BR4CON!<FLUSH1-INIT63000*4>!<FLUSH1-INIT6777/2>>
BRSHFT ;SHIFT RIGHT
CG1: MICPC=MICPC+1
<MOVE!SHFTBR!WRTBR!SELB>
BR4 10S
MICPC=MICPC+1
<JUMP!BR4CON!<10S-INIT63000*4>!<10S-INIT6777/2>>
LDNA IMM,TYPAB ;ADDRESS TYPE TABLE
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<TYPAB6377>>
CMP <MEMX!INCMAR>,SP13
MICPC=MICPC+1
<SUBTC!MEMX!INCMAR!SP13>
Z REP
MICPC=MICPC+1
<JUMP!ZCONDI!<REP-INIT63000*4>!<REP-INIT6777/2>>
CMP <MEMX!INCMAR>,SP13
MICPC=MICPC+1
<SUBTC!MEMX!INCMAR!SP13>
Z NAK
MICPC=MICPC+1
<JUMP!ZCONDI!<NAK-INIT63000*4>!<NAK-INIT6777/2>>
LDNA IMM,TYPST ;SET POINTER TO START TYPE
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<TYPST6377>>
CMP <MEMX!INCMAR>,SP13
MICPC=MICPC+1
<SUBTC!MEMX!INCMAR!SP13>
Z START
MICPC=MICPC+1

```



```

(1) 013736 115413 <JUMP:IZCOND!<START-INIT&3000*4>!<START-INIT&777/2>>
1036 ;STACK TYPE
1037 013740 CMP <MEMX!INCMAR>,SP13
(1) 013740 000607 MICPC=MICPC+1
(1) 013740 054373 <SUBTCIMEMX!INCMAR!SP13>
1038 013742 Z STACK
(1) 013742 000610 MICPC=MICPC+1
(1) 013742 115425 <JUMP:IZCOND!<STACK-INIT&3000*4>!<STACK-INIT&777/2>>
1039 013744 CMP <MEMX!INCMAR>,SP13 ;ACK TYPE
(1) 013744 000611 MICPC=MICPC+1
(1) 013744 054373 <SUBTCIMEMX!INCMAR!SP13>
1040 013746 Z ACK
(1) 013746 000612 MICPC=MICPC+1
(1) 013746 105620 <JUMP:IZCOND!<ACK-INIT&3000*4>!<ACK-INIT&777/2>>
1041 013750 ALWAYS IDLE ;OTHERWISE IGNORE--MUST BE OBS MSG
(1) 013750 000613 MICPC=MICPC+1
(1) 013750 100445 <JUMP:ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
1043 RCVCK: SPBR IBUS,RCVCON,SP0 ;READ RCVR CONTROL CSR
(1) 013752 000614 MICPC=MICPC+1
(1) 013752 023640 <MOVE!SPBR!IBUS!RCVCON!SP0>
1044 013754 BRWRT BR,ADD!SP0 ;SHIFT LEFT
(1) 013754 000615 MICPC=MICPC+1
(1) 013754 060400 <MOVE!WRTEBR!BR!<ADD!SP0>>
1045 013756 BR7 I1
(1) 013756 000616 MICPC=MICPC+1
(1) 013756 103452 <JUMP:BR7CON!<I1-INIT&3000*4>!<I1-INIT&777/2>>
1046 013760 ALWAYS TA1
(1) 013760 000617 MICPC=MICPC+1
(1) 013760 110405 <JUMP:ALCOND!<TA1-INIT&3000*4>!<TA1-INIT&777/2>>
1047 013762 ACK: BRWRT BR,AA!SP10 ;READ LINE STATUS-SHIFTING LEFT
(1) 013762 000620 MICPC=MICPC+1
(1) 013762 060530 <MOVE!WRTEBR!BR!<AA!SP10>>
1048 013764 BR4 58 ;IF START RECD -- CLEAR START MODE
(1) 013764 000621 MICPC=MICPC+1
(1) 013764 107223 <JUMP:BR4CON!<58-INIT&3000*4>!<58-INIT&777/2>>
1049 013766 ALWAYS IDLE
(1) 013766 000622 MICPC=MICPC+1
(1) 013766 100445 <JUMP:ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
1050 013770 SS: BRWRT IMM,327 ;CLEAR START MODE
(1) 013770 000623 MICPC=MICPC+1
(1) 013770 000727 <MOVE!WRTEBR!IMM!<327>>
1051 013772 SP BR,AA&NB,SP10 ;IN LINE STATUS
(1) 013772 000624 MICPC=MICPC+1
(1) 013772 063270 <MOVE!SPX!BR!AA&NB!SP10>
1052 013774 ALWAYS RD5
(1) 013774 000625 MICPC=MICPC+1
(1) 013774 104517 <JUMP:ALCOND!<RD5-INIT&3000*4>!<RD5-INIT&777/2>>

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1055 ;*****TIME CRITICAL CODE-- CHANGE WITH GREAT CARE*****
1056 .SBTTL RCVK01--ROUTINE TO HANDLE FIRST BYTE ODD RECEIVE
1057 013776 RCVK01: SPBR IBUS,NPR,SP0 ;READ NPR REGISTER
(1) 013776 000626 MICPC=MICPC+1
(1) 013776 123600 <MOVE!SPBR!IBUS!NPR!SP0>
1058 014000 BR0 IDLE
(1) 014000 000627 MICPC=MICPC+1
(1) 014000 102045 <JUMP:BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
1059 014002 BRWRT IMM,200 ;MASK FOR C0(BYTE TRANSFER)
(1) 014002 000630 MICPC=MICPC+1
(1) 014002 200600 <MOVE!WRTEBR!IMM!<200>>
1060 014004 OUT BR,<AORB!ONPR> ;TURN ON C0
(1) 014004 000631 MICPC=MICPC+1
(1) 014004 061310 <MOVE!WROUT!BR!<AORB!ONPR>>
1061 014006 STATE RKE1
(1) 014006 000632 MICPC=MICPC+1
(1) 014006 000670 <MOVE!WRTEBR!IMM!<RKE1-INIT&777/2>>
1062 014010 ALWAYS RCVK02
(1) 014010 100633 MICPC=MICPC+1
(1) 014010 104637 <JUMP:ALCOND!<RCVK02-INIT&3000*4>!<RCVK02-INIT&777/2>>
1063 .SBTTL RCVK0--PROCESS ODD CHARACTER
1072 014012 RCVK0: SPBR IBUS,NPR,SP0 ;IS AN NPR GOING
(1) 014012 000634 MICPC=MICPC+1
(1) 014012 123600 <MOVE!SPBR!IBUS!NPR!SP0>
1073 014014 BR0 IDLE ;IF SO --- GET OUT
(1) 014014 000635 MICPC=MICPC+1
(1) 014014 102045 <JUMP:BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
1074 014016 STATE RCVKE
(1) 014016 000636 MICPC=MICPC+1
(1) 014016 200645 <MOVE!WRTEBR!IMM!<RCVKE-INIT&777/2>>
1075 014020 RCVK02: SP BR,SELB,SP3 ;SET STATE
(1) 014020 000637 MICPC=MICPC+1
(1) 014020 063223 <MOVE!SPX!BR!SELB!SP3>
1076 014022 OUTPUT IBUS,RCVDAT!OUTDA2 ;OUTPUT A CHAR
(1) 014022 000640 MICPC=MICPC+1
(1) 014022 027203 <MOVE!WROUT!IBUS!<RCVDAT!OUTDA2>>
1077 014024 RK2:
1079 014024 RK8: BRWRT IMM,21 ;SET OUT NPR (C1) AND NPR REQ
(1) 014024 000641 MICPC=MICPC+1
(1) 014024 000421 <MOVE!WRTEBR!IMM!<21>>
1080 014026 SP IBUS,NPR,SP0 ;READ NPR REGISTER
(1) 014026 000642 MICPC=MICPC+1
(1) 014026 123200 <MOVE!SPX!IBUS!NPR!SP0>
1081 014030 OUT BR,<AORB!ONPR> ;WRITE NPR REGISTER
(1) 014030 000643 MICPC=MICPC+1
(1) 014030 061310 <MOVE!WROUT!BR!<AORB!ONPR>>
1082 014032 ALWAYS IDLE
(1) 014032 000644 MICPC=MICPC+1
(1) 014032 100445 <JUMP:ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

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1093  
1094 014034  
(1) 000645  
(1) 014034 120600  
1099 014036  
(1) 000646  
(1) 014036 102045  
1101 014040  
(1) 000647  
(1) 014040 023140  
1102 014042  
(1) 000650  
(1) 014042 062066  
1103 014044  
(1) 000651  
(1) 014044 063164  
1104 014046  
(1) 000652  
(1) 014046 105255  
1105 014050  
(1) 000653  
(1) 014050 063165  
1106 014052  
(1) 000654  
(1) 014052 105721  
1107 014054  
(1) 000655  
(1) 014054 023140  
1108 014056  
(1) 000656  
(1) 014056 062066  
1109 014060  
(1) 000657  
(1) 014060 115030  
1110 014062  
(1) 000660  
(1) 014062 023200  
1111 014064  
(1) 000661  
(1) 014064 062202  
1112 014066  
(1) 000662  
(1) 014066 063164  
1113 014070  
(1) 000663  
(1) 014070 105266  
1114 014072  
(1) 000664  
(1) 014072 063165  
1115 014074  
(1) 000665  
(1) 014074 111765  
1125 014076  
(1) 000666  
(1) 014076 000634  
1126 014100

```

RCVKE: .SBTTL RCVKE--HANDLE EVEN BYTES
        BRWRT IBUS,NPR                ;READ NPR CONTROL REGISTER
        MICPC=MICPC+1
        <MOVEIWBRI:IBUSI<NPR>>
        BR0 IDLE
        MICPC=MICPC+1
        <JUMPIBR0CONI<IDLE=INIT&3000*4>I<IDLE=INIT&777/2>>
RK5:    SP IBUS,I0BA1,SP0             ;READ LOW BYTE OF BA TO SP
        MICPC=MICPC+1
        <MOVEISPX:IBUS:I0BA1:SP0>
        OUTPUT DP,<INCA:I0BA1>        ;WRITE INCREMENTED BA
        MICPC=MICPC+1
        <MOVEIWROUT:DP:I<INCA:I0BA1>>
RK50:   SP BR,DECA,SP4                ;DECREMENT CHARACTER COUNT
        MICPC=MICPC+1
        <MOVEISPX:IBRI:DECA:SP4>
        C 106                          ;NO OVERFLOW
        MICPC=MICPC+1
        <JUMPICOND:I<106=INIT&3000*4>I<106=INIT&777/2>>
        SP BR,DECA,SP5                ;OVERFLOW - DECREMENT HIGH BYTE
        MICPC=MICPC+1
        <MOVEISPX:IBRI:DECA:SP5>
        Z RL3                           ;BYTE COUNT ZERO
        MICPC=MICPC+1
        <JUMPIZCOND:I<RL3=INIT&3000*4>I<RL3=INIT&777/2>>
106:    SP IBUS,I0BA1,SP0             ;READ INCREMENTED BA
        MICPC=MICPC+1
        <MOVEISPX:IBUS:I0BA1:SP0>
        OUTPUT DP,<INCA:I0BA1>        ;WRITE INCREMENTED BA
        MICPC=MICPC+1
        <MOVEIWROUT:DP:I<INCA:I0BA1>>
        C ICB22                          ;IF CARRY INC BA HIGH
        MICPC=MICPC+1
        <JUMPICOND:I<ICB22=INIT&3000*4>I<ICB22=INIT&777/2>>
RK9:    SP IBUS,RCVDAT,SP0            ;READ CHAR AND SAVE IN SP0
        MICPC=MICPC+1
        <MOVEISPX:IBUS:RCVDAT:SP0>
RK3:    OUTPUT BR,SELA:OUTDA1          ;WRITE THE CHARACTER
        MICPC=MICPC+1
        <MOVEIWROUT:BR:I<SELA:OUTDA1>>
        SP BR,DECA,SP4                ;DECREMENT THE COUNT OF BYTES
        MICPC=MICPC+1
        <MOVEISPX:IBRI:DECA:SP4>
        C RK6                            ;NO OVERFLOW
        MICPC=MICPC+1
        <JUMPICOND:I<RK6=INIT&3000*4>I<RK6=INIT&777/2>>
        SP BR,DECA,SP5                ;DECREMENT HIGH BYTE OF COUNT
        MICPC=MICPC+1
        <MOVEISPX:IBRI:DECA:SP5>
        Z RL4                           ;BYTE COUNT ZERO
        MICPC=MICPC+1
        <JUMPIZCOND:I<RL4=INIT&3000*4>I<RL4=INIT&777/2>>
RK6:    STATE RCVKO
        MICPC=MICPC+1
        <MOVEIWBRI:IMMI<RCVKO=INIT&777/2>>
        ALWAYS REXIT

```

(1) 000667  
(1) 014100 104422  
1128  
1129 014102  
(1) 000670  
(1) 014102 123200  
1130 014104  
(1) 000671  
(1) 014104 000577  
1131 014106  
(1) 000672  
(1) 014106 061270  
1132 014110  
(1) 000673  
(1) 014110 104651  
1133  
1134  
1135 014112  
(1) 000674  
(1) 014112 023200  
1136 014114  
(1) 000675  
(1) 014114 060601  
1137 014116  
(1) 000676  
(1) 014116 117600  
1138 014120  
(1) 000677  
(1) 014120 104661

```

        MICPC=MICPC+1
        <JUMPIALCONDI<REXIT=INIT&3000*4>I<REXIT=INIT&777/2>>
        ;
RKE1:   SP IBUS,NPR,SP0               ;READ NPR REGISTER
        MICPC=MICPC+1
        <MOVEISPX:IBUS:INPR:SP0>
        BRWRT IMM,177                  ;MASK FOR ALL BUT C0
        MICPC=MICPC+1
        <MOVEIWBRI:IMMI<177>>
        OUT BR,<AANDB:INPR>            ;TURN OFF ALL BUT C0
        MICPC=MICPC+1
        <MOVEIWROUT:IBRI:<AANDB:INPR>>
        ALWAYS REXIT
        MICPC=MICPC+1
        <JUMPIALCONDI<RK50=INIT&3000*4>I<RK50=INIT&777/2>>
;*****END OF TIME CRITICAL PATH*****
RCVKE0: SP IBUS,RCVDAT,SP0            ;READ CHARACTER AND SAVE IN SP0
        MICPC=MICPC+1
        <MOVEISPX:IBUS:RCVDAT:SP0>
        BRWRT BR,SELA:SP1              ;READ STATUS BYTE
        MICPC=MICPC+1
        <MOVEIWBRI:IBRI:<SELA:SP1>>
        BR7 PASWRD                      ;MAINT MODE - SEE IF RLD MESSAGE
        MICPC=MICPC+1
        <JUMPIBR7CONI<PASWRD=INIT&3000*4>I<PASWRD=INIT&777/2>>
        ALWAYS RK3                       ;OTHERWISE PROCESS NORMALLY
        MICPC=MICPC+1
        <JUMPIALCONDI<RK3=INIT&3000*4>I<RK3=INIT&777/2>>

```

1140  
1141 014122  
(1) 000700  
(1) 014122 023213  
1142 014124  
(1) 000701  
(1) 014124 000703  
1143 014126  
(1) 000702  
(1) 214126 104422  
1144

```
.SBTTL RCVI--STORE UNNUMBERED MESSAGE TYPE
RCVI: SP IBUS,RCVDAT,SP13 ;STORE UNNUMBERED TYPE
      MICPC=MICPC+1
      <MOVE!SPX!IRUS!RCVDAT!SP13>
      STATE RCVJ ;NEXT STATE IS J
      MICPC=MICPC+1
      <MOVE!WRTE!R!IMM!<RCVJ-INIT6777/2>>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP!ALCOND!<REXIT-INIT63000+4>!<REXIT-INIT6777/2>>
      ;
```

1146  
1147 014130  
(1) 000703  
(1) 014130 114470  
1148 014132  
(1) 000704  
(1) 014132 000706  
1149 014134  
(1) 000705  
(1) 014134 104422

```
.SBTTL RCVJ--ROUTINE TO HANDLE SUBTYPE FIELD,SELECT AND FINAL
RCVJ: ALWAYS SELOS ;"CALL" SELECT AND @SYNC SUBROUTINE
      MICPC=MICPC+1
      <JUMP!ALCOND!<SELOS-INIT63000+4>!<SELOS-INIT6777/2>>
      STATE RCVR ;NEXT STATE IS N
      MICPC=MICPC+1
      <MOVE!WRTE!R!IMM!<RCVJ-INIT6777/2>>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP!ALCOND!<REXIT-INIT63000+4>!<REXIT-INIT6777/2>>
      ;
```

1151  
1152  
1153  
1154 014136  
(1) 000706  
(1) 014130 000403  
1155 014140  
(1) 000707  
(1) 014140 060353  
1156 014142  
(1) 000710  
(1) 014142 000713  
1157  
1158 014144  
(1)  
(1) 014144 000711  
(1) 014144 105136  
1159 014146  
(1) 000712  
(1) 014146 104503

```
.SBTTL RCVR--UNNUMBERED MESSAGE RESPONSE FIELD
;ENTERED FROM IDLE LOOP
;
RCVR:  HRWRTE IMM,3                ;REP MESSAGE TYPE TO BR
        MICPC=MICPC+1
        <MOVE!WRTEBR!IMM!<3>>
        NOP BR,SUB,SP13          ;IS TYPE ACK OR NAK
        MICPC=MICPC+1
        <BR!SUB!SP13>
        STATE RCVO                ;NEXT STATE IS RCVO
        MICPC=MICPC+1
        <MOVE!WRTEBR!IMM!<RCVO-INIT&777/2>>
        ;***NOTE THIS INSTR DOES NOT CLOCK "C"
        C RCVF1                    ;IF NOT IGNORE
        MICPC=MICPC+1
        <JUMP!COND!<RCVF1-INIT&3000*4>!<RCVF1-INIT&777/2>>
        ALWAYS RD2                ;DO RANGE CHECKS
        MICPC=MICPC+1
        <JUMP!ALCOND!<RD2-INIT&3000*4>!<RD2-INIT&777/2>>
```

1161  
1162  
1163  
1164 014154  
(1) 000713  
(1) 014150 000535  
1165 014152  
(1) 000714  
(1) 014152 104536

```
.SBTTL RCVO--UNNUMBERED MESSAGE--NUMBER FIELD
;ENTER FROM IDLE
;
RCVO:  STATE RCVF                    ;NEXT STATE IS ADDRESS
        MICPC=MICPC+1
        <MOVE!WRTEBR!IMM!<RCVF-INIT&777/2>>
        ALWAYS RCVF1
        MICPC=MICPC+1
        <JUMP!ALCOND!<RCVF1-INIT&3000*4>!<RCVF1-INIT&777/2>>
```

```

1167      ,SBTTL RCVL--PROCESS CRC3
1168      ;ENTERED FROM IDLE LOOP
1169      RCVL: SPBR IBUS,NPR,SP0 ;READ NPR CONTROL
(1)      MICPC=MICPC+1
(1)      <MOVE!SPBRX!IBUS!NPR!SP0>
1174      BR0 IDLE
(1)      MICPC=MICPC+1
(1)      <JUMP!BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
1176      RL2: BRWRT IMM,177 ;MASK TO TURN OFF C0
(1)      MICPC=MICPC+1
(1)      <MOVE!WRTEBR!IMM!<177>>
1177      OUT BR, AANDB!ONPR
(1)      MICPC=MICPC+1
1178      RL3: <MOVE!WROUTX!BR!<AANDB!ONPR>>
(1)      SPBR IBUS,IOBA1,SP0 ;READ LOW ORDER BYTE OF ADDRESS
(1)      MICPC=MICPC+1
1179      <MOVE!SPBRX!IBUS!IOBA1!SP0>
(1)      OUTPUT BR,INCA!OBA1 ;INCREMENT THE LOW ORDER BYTE
(1)      MICPC=MICPC+1
1180      <MOVE!WROUT!BR!<INCA!OBA1>>
(1)      SP IBUS,IOBA2,SP0 ;READ HIGH BYTE
(1)      MICPC=MICPC+1
1181      <MOVE!SPX!IBUS!IOBA2!SP0>
(1)      OUTPUT BR,AC!OBA2 ;ADD CARRY TO HIGH BYTE
(1)      MICPC=MICPC+1
1182      <MOVE!WROUT!BR!<AC!OBA2>>
1183      ;
1183      STATE RCVM
(1)      MICPC=MICPC+1
(1)      <MOVE!WRTEBR!IMM!<RCVM-INIT&777/2>>
1184      ALWAYS RCVF1
(1)      MICPC=MICPC+1
(1)      <JUMP!ALCOND!<RCVF1-INIT&3000*4>!<RCVF1-INIT&777/2>>
1185      ;
1190      ;

```

```

1192      ,SBTTL RCVM--PROCESS CRC4--END OF DATA MESSAGE
1193      ;ENTERED FROM IDLE LOOP
1194      ;IF CRC CORRECT -- QUEUE INTERRUPT AND UPDATE RESPONSE
1195      ;
1196      ;IF CRC WRONG SEND NAK
1197      RCVM: BRWRT IBUS,UBBR ;READ UNIBUS BR REGISTER
(1)      MICPC=MICPC+1
(1)      <MOVE!WRTEBR!IBUS!<UBBR>>
1198      BR0 NXMERR ;NON-EXISTANT MEMORY
(1)      MICPC=MICPC+1
(1)      <JUMP!BR0CON!<NXMERR-INIT&3000*4>!<NXMERR-INIT&777/2>>
1199      SP IBUS,RCV DAT,SP0 ;READ CRC CHARACTER
(1)      MICPC=MICPC+1
(1)      <MOVE!SPX!IBUS!RCV DAT!SP0>
1200      BRWRT IBUS,RCVCON ;READ RECEIVER CONTROL REGISTER
(1)      MICPC=MICPC+1
(1)      <MOVE!WRTEBR!IBUS!<RCVCON>>
1201      BR0 RCVM1 ;IF CRC GOOD -- PROCESS
(1)      MICPC=MICPC+1
(1)      <JUMP!BR0CON!<RCVM1-INIT&3000*4>!<RCVM1-INIT&777/2>>
1202      BRWRT BR,SELA!SP1 ;READ STATUS BYTE
(1)      MICPC=MICPC+1
(1)      <MOVE!WRTEBR!BR!<SELA!SP1>>
1203      BR7 RHX ;CRC ERROR IN BOOT MODE - FLUSH
(1)      MICPC=MICPC+1
(1)      <JUMP!BR7CON!<RHX-INIT&3000*4>!<RHX-INIT&777/2>>
1204      LDMA IMM,T ;ELSE SEND NAK --DATA ERROR
(1)      MICPC=MICPC+1
(1)      <MOVE!LDMAR!IMM!<T&377>>
1205      MEMINC IMM,2 ;NAK TYPE
(1)      MICPC=MICPC+1
(1)      <MOVE!WRMEM!INC MAR!IMM!<2>>
1206      MEMINC IMM,302 ;DATA ERROR SUBTYPE
(1)      MICPC=MICPC+1
(1)      <MOVE!WRMEM!INC MAR!IMM!<302>>
1207      LDMA IMM,NDATS
(1)      MICPC=MICPC+1
(1)      <MOVE!LDMAR!IMM!<NDATS&377>>
1208      ALWAYS RH5 ;SEND NAK
(1)      MICPC=MICPC+1
(1)      <JUMP!ALCOND!<RH5-INIT&3000*4>!<RH5-INIT&777/2>>
1209      ;
1210      RCVM0: LDMA IMM,<<RTHRS+3>> ;POINT TO ERROR WORD
(1)      MICPC=MICPC+1
(1)      <MOVE!LDMAR!IMM!<<RTHRS+3>&377>>
1211      BRWRT IMM,10 ;MAINT MESSAGE ERROR
(1)      MICPC=MICPC+1
(1)      <MOVE!WRTEBR!IMM!<10>>
1212      ALWAYS RCEXY ;GIVE FATAL ERROR
(1)      MICPC=MICPC+1
(1)      <JUMP!ALCOND!<RCEXY-INIT&3000*4>!<RCEXY-INIT&777/2>>

```

1214  
1215  
1216  
1217  
1218 #14236  
(1) 000746  
(1) #14236 020600  
1219 #14240  
(1) 000747  
(1) #14240 060376  
1220 #14242  
(1) 000750  
(1) #14242 105757  
1221  
1222 #14244  
(1) 000751  
(1) #14244 060521  
1223 #14246  
(1) 000752  
(1) #14246 107354  
1224 #14250  
(1) 000753  
(1) #14250 104415  
1225 #14252  
(1) 000754  
(1) #14252 000563  
1226 #14254  
(1) 000755  
(1) #14254 063261  
1227 #14256  
(1) 000756  
(1) #14256 104415  
1228  
1229 #14260  
(1) 000757  
(1) #14260 063164  
1230 #14262  
(1) 000760  
(1) #14262 115720  
1231 #14264  
(1) 000761  
(1) #14264 100145

.SBTTL EM2--PROCESS RLD MESSAGE  
;ENTERED FROM IDLE LOOP  
;IF RLD PASSWORD CHECKS TRIGGER THE BOOT ROM  
EM2: BRWRT E IBUS,RCVDAT ;READ THE CHAR  
MICPC=MICPC+1  
<MOVE!WRTEBR!IBUS!<RCVDAT>>  
CMP BR,SP16 ;IS IT A MATCH  
MICPC=MICPC+1  
<SUBTC!BR!SP16>  
Z  
MICPC=MICPC+1  
<JUMP!ZCOND!<EM3-INIT&3000\*4>!<EM3-INIT&777/2>>  
;FALL INTO RHX  
RHX: BRWRT E BR,AA!SP1 ;READ STATUS BYTE SHIFTED LEFT  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR!<AA!SP1>>  
BR4 100 ;DLE RECEIVED IN NORMAL MODE  
MICPC=MICPC+1  
<JUMP!BR4CON!<100-INIT&3000\*4>!<100-INIT&777/2>>  
ALWAYS FLUSH ;ALREADY IN MAINT MODE  
MICPC=MICPC+1  
<JUMP!ALCOND!<FLUSH-INIT&3000\*4>!<FLUSH-INIT&777/2>>  
10S: BRWRT E IMM,163 ;MASK TO CLEAR ALL MAINT RELATED BITS  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<163>>  
SP BR,AA!NDB,SP1 ;CLEAR THEM  
MICPC=MICPC+1  
<MOVE!SPX!BR!<AA!NDB!SP1>  
ALWAYS FLUSH  
MICPC=MICPC+1  
<JUMP!ALCOND!<FLUSH-INIT&3000\*4>!<FLUSH-INIT&777/2>>  
EM3: SP BR,DECA,SP4 ;DECREMENT CHARACTER COUNT BY ONE  
MICPC=MICPC+1  
<MOVE!SPX!BR!<DECA!SP4>  
Z EMTRIG ;TRIGGER AC LOW  
MICPC=MICPC+1  
<JUMP!ZCOND!<EMTRIG-INIT&3000\*4>!<EMTRIG-INIT&777/2>>  
ALWAYS IDLE  
MICPC=MICPC+1  
<JUMP!ALCOND!<IDLE-INIT&3000\*4>!<IDLE-INIT&777/2>>

1233  
1234 #14266  
(1) 000762  
(1) #14266 060601  
1235 #14270  
(1) 000763  
(1) #14270 103747  
1236 #14272  
(1) 000764  
(1) #14272 000610  
1237 #14274  
(1) 000765  
(1) #14274 063301  
1238 #14276  
(1) 000766  
(1) #14276 100747  
1239 #14300  
(1) 000767  
(1) #14300 000404  
1240 #14302  
(1) 000770  
(1) #14302 123200  
1241 #14304  
(1) 000771  
(1) #14304 061010  
1242 #14306  
(1) 000772  
(1) #14306 110753  
1243 #14310  
(1) 000773  
(1) #14310 000404  
1244 #14312  
(1) 000774  
(1) #14312 123220  
1245 #14314  
(1) 000775  
(1) #14314 061011  
1246 #14316  
(1) 000776  
(1) #14316 114767  
1247 #14320  
(1) 000777  
(1) #14320 000000

BOOT: BRWRT E BR,SELA!SP1 ;SEE IF IN MAINT. MODE  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR!<SELA!SP1>>  
BR7 RA3 ;BRANCH IF SO AND TREAT DLE LIKE NUM. MSG.  
MICPC=MICPC+1  
<JUMP!BR7CON!<RA3-INIT&3000\*4>!<RA3-INIT&777/2>>  
BRWRT E IMM,210 ;MASK TO SET MAINT MODE AND DLE RECV'D  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<210>>  
SP BR,AORB,SP1 ;SET THE BITS  
MICPC=MICPC+1  
<MOVE!SPX!BR!<AORB!SP1>  
ALWAYS RA3 ;TREAT LIKE NUMBERED MESSAGE  
MICPC=MICPC+1  
<JUMP!ALCOND!<RA3-INIT&3000\*4>!<RA3-INIT&777/2>>  
RESEXT: BRWRT E IMM,4 ;ADD TO MXT BITS  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<4>>  
SP IBUS,NPR,SP0  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!NPR!SP0>  
OUT BR,ADD!ONPR ;DO IT  
MICPC=MICPC+1  
<MOVE!WROUTX!BR!<ADD!ONPR>>  
ALWAYS RES1  
MICPC=MICPC+1  
<JUMP!ALCOND!<RES1-INIT&3000\*4>!<RES1-INIT&777/2>>  
TABMXT: BRWRT E IMM,4 ;INCREMENT MXT  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<4>>  
SP IBUS,UBBR,SP0 ;READ BR CONTROL  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!UBBR!SP0>  
OUT BR,ADD!OBR  
MICPC=MICPC+1  
<MOVE!WROUTX!BR!<ADD!OBR>>  
ALWAYS ECX  
MICPC=MICPC+1  
<JUMP!ALCOND!<ECX-INIT&3000\*4>!<ECX-INIT&777/2>>  
\$ZERO  
MICPC=MICPC+1  
000000

1249 014322  
1250 002777  
1251  
1252  
1253 014322  
(1) 01000  
(1) 014322 020620  
1254 014324  
(1) 001001  
(1) 014324 173202  
1255 014326  
(1) 001002  
(1) 014326 103452

```

      ,=INIT+2000
      MICPC=777
      .SBTTL TMTDA--TRANSMITTER DISPATCH ROUTINE
      ;
TMTDA: BRWRTE IBUS,TMTCON ;READ TRANSMITTER CONTROL REGISTER
      MICPC=MICPC+1
      <MOVE!WRTEBRI!IBUS!<TMTCON>>
      ,BR4 DP,SELA,<21PAGE2> ;IF READY PROCEED
      MICPC=MICPC+1
      <JUMP! BR4CON!DP!SELA!21PAGE2>
      ALWAYS I1 ;ELSE IDLE
      MICPC=MICPC+1
      <JUMP!ALCONDI!<I1-INIT+3000*4>!<I1-INIT+777/2>>

```

1257  
1258  
1259 014330  
(1) 001003  
(1) 014330 060530  
1260 014332  
(1) 001004  
(1) 014332 107614  
1261 014334  
(1) 001005  
(1) 014334 060610  
1262 014336  
(1) 001006  
(1) 014336 112031  
1263 014340  
(1) 001007  
(1) 014340 001620  
1264 014342  
(1) 001010  
(1) 014342 103052  
1265 014344  
(1) 001011  
(1) 014344 112431  
1266  
1267 014346  
(1) 001012  
(1) 014346 002453  
(1) 001013  
(1) 014350 063222  
1268 014352  
(1) 001014  
(1) 014352 060601  
1269 014354  
(1) 001015  
(1) 014354 113427  
1270 014356  
(1) 001016  
(1) 014356 060610  
1271 014360  
(1) 001017  
(1) 014360 112023  
1272 014362  
(1) 001022  
(1) 014362 000001  
1273 014364  
(1) 001021  
(1) 014364 062230  
1274 014366  
(1) 001022  
(1) 014366 100452  
1275 014370  
(1) 001023  
(1) 014370 002000  
(1) 001021  
(1) 014372 063222  
1276 014374

```

      .SBTTL TMTA--FIRST CHARACTER OF HEADER
      ;
TMTA: BRWRTE BR,AA!SP10 ;SHIFT LEFT
      MICPC=MICPC+1
      <MOVE!WRTEBRI!BR!<AA!SP10>>
      BR7 RCVCCK
      MICPC=MICPC+1
      <JUMP!BR7CON!<RCVCCK-INIT+3000*4>!<RCVCCK-INIT+777/2>>
TMTA: BRWRTE BR,SELA!SP10 ;REREAD STATUS
      MICPC=MICPC+1
      <MOVE!WRTEBRI!BR!<SELA!SP10>>
      BR0 NUMSYN ;IF UNNUMBPENDING -- SEND IT
      MICPC=MICPC+1
      <JUMP!BR0CON!<NUMSYN-INIT+3000*4>!<NUMSYN-INIT+777/2>>
      BRSHFT
      MICPC=MICPC+1
      <MOVE!SHFTBRI!WRTEBRI!SELB>
      BR4 I1 ;IF START MODE--EXIT
      MICPC=MICPC+1
      <JUMP!BR4CON!<I1-INIT+3000*4>!<I1-INIT+777/2>>
      BR1 NUMSYN ;IF LINE HAS GONE IDLE SEND SYN
      MICPC=MICPC+1
      <JUMP!BR1CON!<NUMSYN-INIT+3000*4>!<NUMSYN-INIT+777/2>>
      ;ELSE--START TO SEND MESSAGE
TMTXT: TSTATE TMTB
      MICPC=MICPC+1
      <MOVE!WRTEBRI!IMM!<TMTB-INIT+777/2>>
      MICPC=MICPC+1
      <MOVE!SPX!BRI!SELB!SP2>
      BRWRTE BR,SELA!SP1 ;ARE WE IN BOOT MODE
      MICPC=MICPC+1
      <MOVE!WRTEBRI!BRI!<SELA!SP1>>
      BR7 TMTBT ;IF SO SEND DLE
      MICPC=MICPC+1
      <JUMP!BR7CON!<TMTBT-INIT+3000*4>!<TMTBT-INIT+777/2>>
      BRWRTE BR,<SELA!SP10> ;UNNUMB MESSAGE?
      MICPC=MICPC+1
      <MOVE!WRTEBRI!BRI!<SELA!SP10>>
      BR0 TMTUN ;IF SO --BRANCH
      MICPC=MICPC+1
      <JUMP!BR0CON!<TMTUN-INIT+3000*4>!<TMTUN-INIT+777/2>>
      BRWRTE IMM,201 ;ELSE STORE SOH
      MICPC=MICPC+1
      <MOVE!WRTEBRI!IMM!<201>>
TMTA5: OUTPUT BR,<SELB!TMTDAT> ;IN TMT SILO
      MICPC=MICPC+1
      <MOVE!WROUT!BRI!<SELB!TMTDAT>>
      ALWAYS I1
      MICPC=MICPC+1
      <JUMP!ALCONDI!<I1-INIT+3000*4>!<I1-INIT+777/2>>
TMTUN: TSTATE TMTI
      MICPC=MICPC+1
      <MOVE!WRTEBRI!IMM!<TMTI-INIT+777/2>>
      MICPC=MICPC+1
      <MOVE!SPX!BRI!SELB!SP2>
      BRWRTE IMM,5 ;END TO BR

```

(1) 014374 001025  
(1) 014376 000405  
1277 014376 001026  
(1) 014376 110421  
1278 014400 001027  
(1) 014400 000620  
1279 014402 001030  
(1) 014402 110421  
1280 014404 001031  
(1) 014494 000610  
1282 014406 001032  
(1) 014406 113434  
1283 014410 001033  
(1) 014410 100452  
1284 014412 001034  
(1) 014412 020660  
1285 014414 001035  
(1) 014414 001020  
1286 014416 001036  
(1) 014416 103052  
1287 014420 001037  
(1) 014422 000773  
1288 014422 001040  
(1) 014422 003270  
1289 014424 001041  
(1) 014424 000445  
(1) 014426 001042  
(1) 014426 003222  
1294 014430 001043  
(1) 014430 000410  
1296 014432 001044  
(1) 014432 003226  
1297 014434 001045  
(1) 014434 003166  
1298 014436 001046  
(1) 014436 111412  
1299 014440 001047  
(1) 014440 000401

```
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<5>>  
ALWAYS TMTA5  
MICPC=MICPC+1  
<JUMP!ALCONDI<TMTA5-INIT&3000*4>!<TMTA5-INIT&777/2>>  
TMTBT: BRWRTE IMM,270 ;WRITE A DLE TO BR  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<220>>  
ALWAYS TMTA5 ;SEND IT  
MICPC=MICPC+1  
<JUMP!ALCONDI<TMTA5-INIT&3000*4>!<TMTA5-INIT&777/2>>  
; NUMSYN: BRWRTE BR,<SELA!SP10> ;READ LINE STATUS WORD  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR!<SELA!SP10>>  
BR7 58 ;IF OK TO SEND--PROCEED  
MICPC=MICPC+1  
<JUMP!BR7CONI<58-INIT&3000*4>!<58-INIT&777/2>>  
ALWAYS I1 ;ELSE--IDLE  
MICPC=MICPC+1  
<JUMP!ALCONDI<I1-INIT&3000*4>!<I1-INIT&777/2>>  
58: BRWRTE IBUS,MODEM ;ARE WE STILL SENDING?  
MICPC=MICPC+1  
<MOVE!WRTEBR!IBUS!<MODEM>>  
BRSHFT  
MICPC=MICPC+1  
<MOVE!SHFTBR!WRTEBR!SELB>  
BR4 I1 ;RTS SET? IF SO WE ARE--STALL  
MICPC=MICPC+1  
<JUMP!BR4CONI<I1-INIT&3000*4>!<I1-INIT&777/2>>  
BRWRTE IMM,373 ;MASK TO TURN OFFLINE IDLE  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<373>>  
SP BR,AANDB,SP10 ;IN LINE STATUS WORD  
MICPC=MICPC+1  
<MOVE!SPX!BR!AANDB!SP10>  
TSTATE TMTA1  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<TMTA1-INIT&777/2>>  
MICPC=MICPC+1  
<MOVE!SPX!BR!SELB!SP2>  
BRWRTE IMM,10  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<10>>  
SP BR,SELB,SP6 ;STORE IN SP6  
MICPC=MICPC+1  
<MOVE!SPX!BR!SELB!SP6>  
TMTA1: SP BR,DECA,SP6 ;DECREMENT SYN COUNT  
MICPC=MICPC+1  
<MOVE!SPX!BR!DECA!SP6>  
Z TMTXT  
MICPC=MICPC+1  
<JUMP!ZCONDI<TMTXT-INIT&3000*4>!<TMTXT-INIT&777/2>>  
BRWRTE IMM,1 ;MASK FOR SON  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<1>>
```

1300 014442 001050  
(1) 014442 002231  
1301 014444 001051  
(1) 014444 000626  
1302 014446 001052  
(1) 014446 110421

```
OUTPUT BR,SELB!OTMTCO ;WRITE IT TO TMTR CONTROL  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<SELB!OTMTCO>>  
BRWRTE IMM,226 ;SYNC CHAR  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<226>>  
ALWAYS TMTA5  
MICPC=MICPC+1  
<JUMP!ALCONDI<TMTA5-INIT&3000*4>!<TMTA5-INIT&777/2>>
```



1304  
1305  
1306 014450 001053  
(1) 014450 123600  
1307 014452 001054  
(1) 014452 102045  
1308 014454 001055  
(1) 014454 010071  
1309 014456 001056  
(1) 014456 053236  
1310 014460 001057  
(1) 014460 016403  
1311 014462 001060  
(1) 014462 070612  
1312 014464 001061  
(1) 014464 000500  
1313 014466 001062  
(1) 014466 063222  
1314 014470 001063  
(1) 014470 056224  
1315 014472 001064  
(1) 014472 056225  
1316 014474 001065  
(1) 014474 043227  
1317  
1318 014476 001066  
(1) 014476 003300  
1319 014500 001067  
(1) 014500 054660  
1320 014502 001070  
(1) 014502 001620  
1321 014504 001071  
(1) 014504 001620  
1322 014506 001072  
(1) 014506 001620  
1323 014510 001073  
(1) 014510 001620  
1324 014512 001074  
(1) 001074

```

.SBTTL TMTB--OUTPUT FIRST CHAR OF COUNT
;
TMTB: SPBR IBUS,NPR,SP0 ;READ BR CONTROL REG
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!NPR!SP0>
SR0 IDLE ;NPR GOING--GET OUT
MICPC=MICPC+1
LDMA IMM,LTC ;GETPOINTER TO NEXT TMT LINK
MICPC=MICPC+1
<MOVE!LDMA!IMM!<LTC&377>>
LDMA MEMX,SELB!SP!SP16 ;POINT TO THE LINK
MICPC=MICPC+1
<MOVE!LDMA!MEMX!<SELB!SP!SP16>>
MEMINC IMM,3 ;WRITE MSG TMTD TO FLAGS
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IMM!<3>>
MEMINC DP,SELA!SP12 ;PICK UP MSGNO
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!DP!<SELA!SP12>>
STATE TMTC ;ADDRESS TMTR STATE
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TMTC-INIT&777/2>>
TE0: SP BR,SELB,SP2 ;UPDATE IT
MICPC=MICPC+1
<MOVE!SPX!IBR!<SELB!SP2>
OUTPUT <MEMX!INCMAR>,SELB!IBA1 ;WRITE LOW BYTE OF ADDRESS
MICPC=MICPC+1
<MOVE!WROUT!MEMX!INCMAR!<SELB!IBA1>>
OUTPUT <MEMX!INCMAR>,SELB!IBA2 ;WRITE HIGH BYTE OF ADDRESS
MICPC=MICPC+1
<MOVE!WROUT!MEMX!INCMAR!<SELB!IBA2>>
SP MEMX,SELB,SP7 ;HIGH BYTE OF COUNT TO SP7
MICPC=MICPC+1
<MOVE!SPX!MEMX!SELB!SP7>
;WAIT TO MASK OFF MEM EXT. BITS
SP IMM,300,SP0 ;MASK FOR MXI
MICPC=MICPC+1
<MOVE!SPX!IMM!300!SP0>
BRWRT MEMX!INCMAR,AAADB!SP0 ;TURN OFF CC2
MICPC=MICPC+1
<MOVE!WRTEBR!MEMX!INCMAR!<AAADB!SP0>>
BRSHFT ;SHIFT BITS INTO CORRECT POSITION
MICPC=MICPC+1
<MOVE!SHFTBR!WRTEBR!SELB>
BRSHFT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTEBR!SELB>
BRSHFT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTEBR!SELB>
BRSHFT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTEBR!SELB>
BRSHFT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTEBR!SELB>
OUT BR,SELB!ONPR
MICPC=MICPC+1

```

(1) 014512 001230  
1325 014514 001075  
(1) 014514 057626  
1326 014516 001076  
(1) 014516 062230  
1327 014520 001077  
(1) 014520 100445  
1328

```

<MOVE!WROUT!IBR!<SELB!ONPR>>
SPBR MEMX!INCMAR,SELB,SP6 ;LOW BYTE OF COUNT TO SP6
MICPC=MICPC+1
<MOVE!SPBRX!MEMX!INCMAR!SELB!SP6>
OUTPUT BR,SELB!TMTDAT ;WRITE IT TO TMTR SILO
MICPC=MICPC+1
<MOVE!WROUT!IBR!<SELB!TMTDAT>>
ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000+4>!<IDLE-INIT&777/2>>
;

```

```

1330          ,SBTTL TMTC--OUTPUT SECOND CHAR OF COUNT
1331          ;
1332 014522    TMTC: BRWRTI IMM,77          ;MASK TO CLEAR NXT BITS
                MICPC=MICPC+1
                <MOVEIWRTEBRIIMM1<77>>
1333 014524    SPBR BR,ANDB,SP7          ;CLEAR THEM
                MICPC=MICPC+1
                <MOVEISPBRXIBRIANDBISP7>
1334 014526    OUTPUT DP,<SELB:TMTDAT>    ;WRITE TO TMT SILO
                MICPC=MICPC+1
                <MOVEIWROUTIDPI<SELB:TMTDAT>>
1335 014530    LDMA IMM,LTC              ;POINT TO TMT BUFFER
                MICPC=MICPC+1
                <MOVEILDMAIRIMM1<LTC&377>>
1336 014532    BRWRTI IMM,6              ;OFFSET TO NEXT LINK
                MICPC=MICPC+1
                <MOVEIWRTEBRIIMM1<6>>
1337 014534    MEM BP,ADDISP16           ;UPDATE THE POINTER
                MICPC=MICPC+1
                <MOVEIWRMEMIBRI<ADDISP16>>
1338 014536    BRWRTI IMM,TML0           ;GET WRAPAROUND ADDRESS
                MICPC=MICPC+1
                <MOVEIWRTEBRIIMM1<TML0>>
1339 014540    CMP BR,SP16               ;WRAPAORUND
                MICPC=MICPC+1
                <SUBTCIBRISP16>
1340 014542    Z 100
                MICPC=MICPC+1
                <JUMPIZCONDI<100-INIT&3000*4>1<100-INIT&777/2>>
1341 014544    50: STATE TMTD
                MICPC=MICPC+1
                <MOVEIWRTEBRIIMM1<TMTD-INIT&777/2>>
1342 014546    ALWAYS XEXIT
                MICPC=MICPC+1
                <JUMPIALCONDI<XEXIT-INIT&3000*4>1<XEXIT-INIT&777/2>>
1343 014550    100: MEM IMM,TML1         ;GO BACK TO FIRST LINK
                MICPC=MICPC+1
                <MOVEIWRMEMIBRIIMM1<TML1>>
1344 014552    ALWAYS 50
                MICPC=MICPC+1
                <JUMPIALCONDI<50-INIT&3000*4>1<50-INIT&777/2>>
1345          ;
  
```

```

1347          ,SBTTL TMTD--RESPONSE FIELD-NUMBERED MESSAGE
1348 014554    TMTD: STATE TMTD
                MICPC=MICPC+1
                <MOVEIWRTEBRIIMM1<TMTD-INIT&777/2>>
1349 014556    SP BR,DECA,SP6           ;ADJUSRT COUNT FOR TWO'S COMPLEMENT
                MICPC=MICPC+1
                <MOVEISPXIBRIDECAISP6>
1350 014560    C TD2                    ;NO OVERFLOW
                MICPC=MICPC+1
                <JUMPICCONDI<TD2-INIT&3000*4>1<TD2-INIT&777/2>>
1351 014562    SP BR,DECA,SP7           ;DECREMENT HIGH BYTE OF COUNT
                MICPC=MICPC+1
                <MOVEISPXIBRIDECAISP7>
1352 014564    TD2: LDMA IMM,ISP11      ;RESP FIELD ADDR TO MAR
                MICPC=MICPC+1
                <MOVEILDMAIRIMM1<ISP11&377>>
  
```

1363 014566  
(1) 001122  
(1) 014566 110606

ALWAYS TJ1  
MICPC=MICPC+1  
<JUMP!ALCOND!<TJ1-INIT&3000\*4>!<TJ1-INIT&777/2>>

1367  
1368 014573  
1369 014570  
(1) 014570 001123  
(1) 014570 123000  
1370 014572  
(1) 014572 001124  
(1) 014572 102052  
1371 014574  
(1) 014574 001125  
(1) 014574 000612  
1372 014576  
(1) 014576 001126  
(1) 014576 062230  
1373 014600  
(1) 014600 001127  
(1) 014600 000531  
1374 014602  
(1) 014602 001130  
(1) 014602 110573

.SBTTL TMTE--NUMBER FIELD--NUMBERED MESSAGE  
TMTE: SPBR IBUS,NPR,SP0 ;READ NPR CONTROL REGISTER  
MICPC=MICPC+1  
<MOVE!SPBR!IBUS!NPR!SP0>  
BR0 I1 ;BUSY = GET OUT  
MICPC=MICPC+1  
<JUMP!BR@CONI<I1-INIT&3000\*4>!<I1-INIT&777/2>>  
BRWRT BR,SELAISP12  
MICPC=MICPC+1  
<MOVE!WRTEBR!<SELAISP12>>  
OUTPUT BR,<SELB!TMTDAT> ;WRITE IT TO THE SILO  
MICPC=MICPC+1  
<MOVE!WROUTIBRI<SELB!TMTDAT>>  
STATE TMTF  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMMI<TMTF-INIT&777/2>>  
ALWAYS TH3  
MICPC=MICPC+1  
<JUMP!ALCOND!<TH3-INIT&3000\*4>!<TH3-INIT&777/2>>

1376  
1377  
1378 014604  
(1) 001131  
(1) 014601 000535  
1379 014606  
(1) 001132  
(1) 014606 063222  
1380 014610  
(1) 001133  
(1) 014610 000401  
1386 014612  
(1) 001134  
(1) 014612 110421

```
.SBTTL TMTF--NUMBERED MSG ADDRESS FIELD
?
TMTF: STATE TF1
      MICPC=MICPC+1
      <MOVE!WRTEBRIIMM!<TF1-INIT&777/2>>
TF2:  SP BR,SELB,SP2
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP2>
      BRWRT IMM,1 ;LOAD ADDRESS
      MICPC=MICPC+1
      <MOVE!WRTEBRIIMM!<1>>
      ALWAYS TMTA5
      MICPC=MICPC+1
      <JUMP!ALCONDI<TMTA5-INIT&3000*4>!<TMTA5-INIT&777/2>>
```

1389  
1390 014614  
(1) 001135  
(1) 014614 000402  
1391 014616  
(1) 001136  
(1) 014616 062231  
1392 014620  
(1) 001137  
(1) 014620 062230  
1393 014622  
(1) 001140  
(1) 014622 020500  
1394 014624  
(1) 001141  
(1) 014624 112155  
1395 014626  
(1) 001142  
(1) 014626 000544  
1396 014630  
(1) 001143  
(1) 014630 100451

```
.SBTTL TF1-NUMBERED MSG HEADER EOM
TF1: BRWRT IMM,2 ;EOM MASK TO BR
      MICPC=MICPC+1
      <MOVE!WRTEBRIIMM!<2>>
      OUTPUT BR,<SELB!OTMTCO> ;UPDATE TMR CONTROL REGISTER
      MICPC=MICPC+1
      <MOVE!WROUTIBRI<SELB!OTMTCO>>
      OUTPUT BR,<SELB!TMDAT> ;OUTPUT A GARBAGE CHAR
      MICPC=MICPC+1
      <MOVE!WROUTIBRI<SELB!TMDAT>>
      BRWRT IBUS,IIBA1 ;READ LOW ORDER FROM INBA
      MICPC=MICPC+1
      <MOVE!WRTEBRIIBUS!<IIBA1>>
      BR0 TMTF1 ;IF ODD BYTE--BRANCH
      MICPC=MICPC+1
      <JUMP!BRCONI<TMTF1-INIT&3000*4>!<TMTF1-INIT&777/2>>
      STATE TMTH
      MICPC=MICPC+1
      <MOVE!WRTEBRIIMM!<TMTH-INIT&777/2>>
      ALWAYS XEXIT
      MICPC=MICPC+1
      <JUMP!ALCONDI<XEXIT-INIT&3000*4>!<XEXIT-INIT&777/2>>
```

1398  
1399  
1400  
1401 014632  
(1) 001144  
(1) 014632 123600  
1405 014634  
(1) 001145  
(1) 014634 102052  
1406 014636  
(1) 001146  
(1) 014636 022010  
1407 014640  
(1) 001147  
(1) 014640 023100  
1408 014642  
(1) 001150  
(1) 014642 062064  
1409 014644  
(1) 001151  
(1) 014644 063160  
1410 014646  
(1) 001152  
(1) 014646 111155  
1411 014650  
(1) 001153  
(1) 014650 063167  
1412 014652  
(1) 001154  
(1) 014652 115402  
1413 014654  
1418 014654  
(1) 001155  
(1) 014654 000557  
1419 014656  
(1) 001156  
(1) 014656 100451  
1420 014660  
1422 014660  
(1) 001157  
(1) 014660 123600  
1423 014662  
(1) 001160  
(1) 014662 102052  
1425 014664  
(1) 001161  
(1) 014664 022030  
1426 014666  
(1) 001162  
(1) 014666 023100  
1427 014670  
(1) 001163  
(1) 014670 062064  
1428 014672  
(1) 001164  
(1) 014672 111372

```

;*****TIME CRITICAL PATH--MODIFY WITH GREAT CARE
;SBTTL TMTH--ROUTINE TO OUTPUT DATA CHARACTERS
;
TMTH: SPBR IBUS,NPR,SP0 ;READ NPR CONTROL
      MICPC=MICPC+1
      <MOVE!SPBRX!IBUS!NPR!SP0>
      BR0 I1 ;IF NPR IN PROGRESS --BRANCH
      MICPC=MICPC+1
      <JUMP!BR0CON!<I1-INIT63000*4>!<I1-INIT6777/2>>
56: OUTPUT IBUS,<INDAT1!TMTDAT> ;WRITE THE EVEN CHAR TO TMT SILO
      MICPC=MICPC+1
      <MOVE!WROUT!IBUS!<INDAT1!TMTDAT>>
      SP IBUS,IIB1,SP0 ;READ LOW BYTE OF BA TO SP
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!IIB1!SP0>
      OUTPUT BR,<INCA!IBA1> ;OUTPUT INCREMENTED BA
      MICPC=MICPC+1
      <MOVE!WROUT!IBR!<INCA!IBA1>>
      SP BR,DECA,SP6 ;DECREMENT CHARACTER COUNT
      MICPC=MICPC+1
      <MOVE!SPX!IBR!DECA!SP6>
      C TH6 ;NO OVERFLOW
      MICPC=MICPC+1
      <JUMP!CCOND!<TH6-INIT63000*4>!<TH6-INIT6777/2>>
      SP BR,DECA,SP7 ;DECREMENT HIGH BYTE OF COUNT
      MICPC=MICPC+1
      <MOVE!SPX!IBR!DECA!SP7>
      Z HEH1 ;BYTE COUNT ZERO
      MICPC=MICPC+1
      <JUMP!ZCOND!<HEH1-INIT63000*4>!<HEH1-INIT6777/2>>
TH6:
TMTF1: STATE TMTHO
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<TMTHO-INIT6777/2>>
      ALWAYS XEXIT
      MICPC=MICPC+1
      <JUMP!ALCOND!<XEXIT-INIT63000*4>!<XEXIT-INIT6777/2>>
TMTHO: SPBR IBUS,NPR,SP0 ;NPR BUSY
      MICPC=MICPC+1
      <MOVE!SPBRX!IBUS!NPR!SP0>
      BR0 I1
      MICPC=MICPC+1
      <JUMP!BR0CON!<I1-INIT63000*4>!<I1-INIT6777/2>>
TH9: OUTPUT IBUS,<INDAT2!TMTDAT> ;ODD CHAR TO SILO
      MICPC=MICPC+1
      <MOVE!WROUT!IBUS!<INDAT2!TMTDAT>>
      SP IBUS,IIB1,SP0 ;READ LOW BYTE TO BA
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!IIB1!SP0>
      OUTPUT BR,<INCA!IBA1> ;OUTPUT THE INCREMENTED BA
      MICPC=MICPC+1
      <MOVE!WROUT!IBR!<INCA!IBA1>>
      C HOINCH
      MICPC=MICPC+1
      <JUMP!CCOND!<HOINCH-INIT63000*4>!<HOINCH-INIT6777/2>>

```

1429 014674  
(1) 001165  
(1) 014674 063160  
1430 014676  
(1) 001166  
(1) 014676 111171  
1431 014700  
(1) 001167  
(1) 014700 063167  
1432 014702  
(1) 001170  
(1) 014702 115402  
1433 014704  
(1) 001171  
(1) 014704 123600  
1437 014706  
(1) 001172  
(1) 014706 060544  
1438 014710  
(1) 001173  
(1) 014710 063222  
1439 014712  
(1) 001174  
(1) 014712 000557  
1440 014714  
(1) 001175  
(1) 014714 063260  
1441 014716  
(1) 001176  
(1) 014716 000401  
1449 014720  
(1) 001177  
(1) 014720 124643  
1451  
1452

```

TH0: SP BR,DECA,SP6 ;DECREMENT CHARACTERCOUNT
      MICPC=MICPC+1
      <MOVE!SPX!IBR!DECA!SP6>
      C TH7 ;NO OVERFLOW
      MICPC=MICPC+1
      <JUMP!CCOND!<TH7-INIT63000*4>!<TH7-INIT6777/2>>
      SP BR,DECA,SP7 ;DECREMENT HIGH BYTE OF COUNT
      MICPC=MICPC+1
      <MOVE!SPX!IBR!DECA!SP7>
      Z HEH1 ;BYTE COUNT ZERO
      MICPC=MICPC+1
      <JUMP!ZCOND!<HEH1-INIT63000*4>!<HEH1-INIT6777/2>>
TH7: SPBR IBUS,NPR,SP0 ;READ NPR REGISTER
      MICPC=MICPC+1
      <MOVE!SPBRX!IBUS!NPR!SP0>
      STATE TMTH
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<TMTH-INIT6777/2>>
TH3: SP BR,SELB,SP2 ;SAVE TSTATE
      MICPC=MICPC+1
      <MOVE!SPX!IBR!SELB!SP2>
TH3X: BRWRTE IMM,157 ;CLEAR C0 AND C1
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<157>>
      SP BR,AAADB,SP0 ;CLEAR THE BITS
      MICPC=MICPC+1
      <MOVE!SPX!IBR!AAADB!SP0>
      BRWRTE IMM,1 ;WRITE NPR BITS TO BR
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<1>>
      ALWAYS RK7
      MICPC=MICPC+1
      <JUMP!ALCOND!<RK7-INIT63000*4>!<RK7-INIT6777/2>>
;*****END TIME CRITICAL PATH*****
;

```

1454  
1455 014722 001200  
(1) 014722 010153  
1456 014724 001201  
(1) 014724 043226  
1457 014726 001202  
(1) 014726 000004  
1458 014730 001203  
(1) 014730 110606  
1459  
1460  
1461 014732 001204  
(1) 014732 010154  
1462 014734 001205  
(1) 014734 000610  
1463 014736 001206  
(1) 014736 042230  
1464 014740 001207  
(1) 014740 100451  
1465

```

.SBTL TMTI--SEND UNNUMBERED TYPE FIELD
TMTI: LDMA IMM,T ;ADDRESS OF TYPE FIELD TO MAR
      MICPC=MICPC+1
      <MOVE!LDMAR!IMM!<T&377>>
      SP MEMX,SELB,SP6 ;COPY IT TO SP6
      MICPC=MICPC+1
      <MOVE!SPX!MEMX!SELB!SP6>
      STATE TMTJ
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<TMTJ-INIT&777/2>>
      ALWAYS TJ1
      MICPC=MICPC+1
      <JUMPIALCOND!<TJ1-INIT&3000*4>!<TJ1-INIT&777/2>>
      ;
.SBTL TMTJ--SEND SUB-TYPE FIELD
TMTJ: LDMA IMM,ST ;ADDRESS OF SUB-TYPE FIELD TO MAR
      MICPC=MICPC+1
      <MOVE!LDMAR!IMM!<ST&377>>
      STATE TMTK
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<TMTK-INIT&777/2>>
TJ1: OUTPUT MEMX,SELB:TMTDAT
      MICPC=MICPC+1
      <MOVE!WROUT!MEMX!<SELB!TMTDAT>>
      ALWAYS XEXIT
      MICPC=MICPC+1
      <JUMPIALCOND!<XEXIT-INIT&3000*4>!<XEXIT-INIT&777/2>>
      ;

```

1467  
1468  
1469 014742 001210  
(1) 014742 000403  
1474 014744 001211  
(1) 014744 060346  
1471 014746 001212  
(1) 014746 000616  
(1) 014750 001213  
(1) 014750 063222  
1472 014752 001214  
(1) 014752 111223  
1473 014754 001215  
(1) 014754 110521  
1474  
1475  
1476 014756 001216  
(1) 014756 000627  
(1) 014760 001217  
(1) 014760 063222  
1477 014762 001220  
(1) 014762 000403  
1478 014764 001221  
(1) 014764 060366  
1479 014766 001222  
(1) 014766 111625  
1480 014770 001223  
(1) 014770 000400  
1481 014772 001224  
(1) 014772 110421  
1482  
1483 014774 001225  
(1) 014774 060572  
1489 014776 001226  
(1) 014776 110421  
1491

```

.SBTL TMTK--OUTPUT RESPONSE FIELD (UNNUMB MSG)
TMTK: BRWRTE IMM,3 ;WRITE A 3 TO BR
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<3>>
      NOP BR,SUB,SP6 ;IF TYPE LESS THAN 3
      MICPC=MICPC+1
      <BR!SUB!SP6>
      TSTATE TMTL
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<TMTL-INIT&777/2>>
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP2>
      C TMTL0
      MICPC=MICPC+1
      <JUMPIALCOND!<TMTL0-INIT&3000*4>!<TMTL0-INIT&777/2>>
      ALWAYS TD2
      MICPC=MICPC+1
      <JUMPIALCOND!<TD2-INIT&3000*4>!<TD2-INIT&777/2>>
      ;
.SBTL TMTL--UNNUMB MSG NUMBER FIELD
TMTL: TSTATE TMTM
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<TMTM-INIT&777/2>>
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP2>
      BRWRTE IMM,3
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<3>>
      CMP BR,SP6 ;IS MESSAGE REP
      MICPC=MICPC+1
      <SUBTC!BR!SP6>
      Z TMTL1 ;YES
      MICPC=MICPC+1
      <JUMPIALCOND!<TMTL1-INIT&3000*4>!<TMTL1-INIT&777/2>>
TMTL0: BRWRTE IMM,0 ;ADDRESS CONTRAT OF ZERO
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<0>>
      ALWAYS TMTA5
      MICPC=MICPC+1
      <JUMPIALCOND!<TMTA5-INIT&3000*4>!<TMTA5-INIT&777/2>>
      ;
TMTL1: BRWRTE BR,DECA!SP12 ;WRITE A RESPONSE
      MICPC=MICPC+1
      <MOVE!WRTEBR!BR!<DECA!SP12>>
      ALWAYS TMTA5
      MICPC=MICPC+1
      <JUMPIALCOND!<TMTA5-INIT&3000*4>!<TMTA5-INIT&777/2>>
      ;

```

1493  
1494 015000 001227  
(1) 015000 000631  
1495 015002 001230  
(1) 015002 110532  
1496 015004 001231  
(1) 015004 000402  
1497 015006 001232  
(1) 015006 062231  
1498 015010 001233  
(1) 015010 062230  
1499 015012 001234  
(1) 015012 000404  
1500 015014 001235  
(1) 015014 063710  
1501 015016 001236  
(1) 015016 060530  
1502 015020 001237  
(1) 015020 113643  
1503 015022 001240  
(1) 015022 000776  
1504 015024 001241  
(1) 015024 063270  
1505 015026 001242  
(1) 015026 110734  
1506 015030 001243  
(1) 015030 000576  
1507 015032 001244  
(1) 015032 110641

```
.SBTTL TMTM--UNNUMB MSG--STATION ADDRESS
STATE TNEOM
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TNEOM-INIT&777/2>>
ALWAYS TF2
MICPC=MICPC+1
<JUMP!ALCOND!<TF2-INIT&3000*4>!<TF2-INIT&777/2>>
TNEOM: BRWRT IMM,2 ;END OF MESSAGE TO BR
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<2>>
OUTPUT BR,<SELB!OTMTCO>
MICPC=MICPC+1
<MOVE!WROUT!BR!<SELB!OTMTCO>> ;OUTPUT A GARBAGE CHARACTER
OUTPUT BR,<SELB!TMTDAT>
MICPC=MICPC+1
<MOVE!WROUT!BR!<SELB!TMTDAT>>
BRWRT IMM,4 ;SET UP LINE HAS GONE IDLE MASK
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<4>>
SPBR BR,AORB,SP10 ;UPDATE LINE STATUS WORD
MICPC=MICPC+1
<MOVE!SPBRX!BR!AORB!SP10>
BRWRT BR,AA!SP10 ;SHIFT STATUS LEFT
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<AA!SP10>>
BR7 108 ;IF HDX SET---BRANCH TO CLEAR OK TO SEND
MICPC=MICPC+1
<JUMP!BR7CON!<108-INIT&3000*4>!<108-INIT&777/2>>
BRWRT IMM,376 ;MASK TO TURN OFF UNNUMB PENDING
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<376>>
SP BR,AA!SP10 ;MASK TO LINE STATUS WORD
MICPC=MICPC+1
<MOVE!SPX!BR!AA!SP10>
ALWAYS TEOM2
MICPC=MICPC+1
<JUMP!ALCOND!<TEOM2-INIT&3000*4>!<TEOM2-INIT&777/2>>
BRWRT IMM,176 ;CLEAR OK TO SEND AND UNNUMB PENDING
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<176>>
ALWAYS 56
MICPC=MICPC+1
<JUMP!ALCOND!<56-INIT&3000*4>!<56-INIT&777/2>>
```

1509  
1510  
1511  
1512 015034 001245  
(1) 015034 123220  
1513 015036 001246  
(1) 015036 000577  
1514  
1515  
1516  
1517  
1518 015040 001247  
(1) 015040 061271  
1519 015042 001250  
(1) 015042 060601  
1520 015044 001251  
(1) 015044 103445  
1521 015046 001252  
(1) 015046 063175  
1522 015050 001253  
(1) 015050 111662  
1523 015052 001254  
(1) 015052 060610  
1524 015054 001255  
(1) 015054 116737  
1525 015056 001256  
(1) 015056 116337  
1526 015060 001257  
(1) 015060 001620  
1527 015062 001260  
(1) 015062 103045  
1528 015064 001261  
(1) 015064 110727  
1529 015066 001262  
(1) 015066 000402  
1531 015070 001263  
(1) 015070 103235  
1532 015072 001264  
(1) 015072 060610

```
.SBTTL TIMSRV--TIMEOUT ROUTINE--SENDS REP
;
;ENABLE LSB
TIMSRV: SP IBUS,UBBR,SP0 ;READ UNIBUS BR REGISTER
MICPC=MICPC+1
<MOVE!SPX!IBUS!UBBR!SP0>
BRWRT IMM,177 ;MASK OFF BR REQ
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<177>>
;RESET TIMER---SLICK MOVE
;SINCE TIMER IS RESET BY WRITING
;A 1 AND THE EXPIRATION LOOKS
;LIKE 1--VOILA
;AND THE BIT ON
OUT BR,<AA!NDB!OBR>
MICPC=MICPC+1
<MOVE!WROUT!BR!<AA!NDB!OBR>>
BRWRT BR,SELA!SP1 ;READ STATUS BYTE
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<SELA!SP1>>
BR7 IDLE ;IF IN MAINT. MODE DISABLE TIMER
MICPC=MICPC+1
<JUMP!BR7CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
SP BR,DECA,SP15 ;DECREMENT THE COUNTER
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP15>
Z 208 ;IF ALL ONES HAS EXPIRED
MICPC=MICPC+1
<JUMP!ZCOND!<208-INIT&3000*4>!<208-INIT&777/2>>
BRWRT BR,SELA!SP10 ;READ LINE STATUS
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<SELA!SP10>>
BR1 TABUPD ;NUMBERED MESSAGE IN PROGRESS
MICPC=MICPC+1
<JUMP!BR1CON!<TABUPD-INIT&3000*4>!<TABUPD-INIT&777/2>>
BR0 TABUPD ;UNNUMBMSGIN PROGRESS
MICPC=MICPC+1
<JUMP!BR0CON!<TABUPD-INIT&3000*4>!<TABUPD-INIT&777/2>>
BRSHFT
MICPC=MICPC+1
<MOVE!SHFT!BR!WRTEBR!SELB>
BR4 IDLE ;START MODE
MICPC=MICPC+1
<JUMP!BR4CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
ALWAYS SNDACK ;ELSE SEND ACK
MICPC=MICPC+1
<JUMP!ALCOND!<SNDACK-INIT&3000*4>!<SNDACK-INIT&777/2>>
TIME1:
208: BRWRT IMM,2 ;
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<2>>
SP BR,SELB,SP15 ;RESET THE TIMER TICK COUNT
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP15>
BRWRT BR,<SELB!SP10> ;READ LINE STATUS WORD
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<SELB!SP10>>
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1533 015074 001265      BRSFHT
(1) 015074 001265      MICPC=MICPC+1
1534 015076 001266      <MOVEISHFTBR|WRTEBR|SELB>
(1) 015076 001266      BR4 BS1 ;IF IN START MODE--BRANCH
1535 015100 001267      MICPC=MICPC+1
(1) 015100 001267      <JUMP|BR4CON|<BS1-INIT&3000*4>|<BS1-INIT&777/2>>
1536 015102 001270      BRWRTE BR,DECA|SP12 ;GET LAST NUMBER SENT
(1) 015102 001270      MICPC=MICPC+1
1537 015104 001271      <MOVE|WRTEBR|BR1|<DECA|SP12>>
(1) 015104 001271      CNP BR,SP17 ;COMPARE TO LAST ACKED
1538 015106 001272      MICPC=MICPC+1
(1) 015106 001272      <SUBTC|BR1|SP17>
1539 015110 001273      Z 106 ;IF EQ --SEND ACK
(1) 015110 001273      MICPC=MICPC+1
1540 015112 001274      <JUMP|ZCOND|<106-INIT&3000*4>|<106-INIT&777/2>>
(1) 015112 001274      LDMA IMM,T ;LOAD ADDRESS OF TYPE FIELD IN UNNUMB SK
1541 015114 001275      MICPC=MICPC+1
(1) 015114 001275      <MOVE|LDMAR|IMM|<T&377>>
1542 015116 001276      MEMINC IMM,3 ;LOAD REP TYPE
(1) 015116 001276      MICPC=MICPC+1
1543 015120 001277      <MOVE|WRMEM|INCMAR|IMM|<3>>
(1) 015120 001277      MEMINC IMM,300 ;ZERO THE SUB-TYPE
1544 015122 001278      <MOVE|WRMEM|INCMAR|IMM|<300>>
(1) 015122 001278      LDMA IMM,REPCS ;CUMULATIVE REPS RECD
1545 015124 001279      MICPC=MICPC+1
(1) 015124 001279      <MOVE|LDMAR|IMM|<REPCS&377>>
1546 015126 001280      SP MEMX,SELB,SP0 ;COPY IT TO SP0
(1) 015126 001280      MICPC=MICPC+1
1547 015130 001281      <MOVE|SPX|MEMX|SELB|SP0>
(1) 015130 001281      MEM BR,INCA|SP0 ;INCREMENT IT
1548 015132 001282      MICPC=MICPC+1
(1) 015132 001282      <MOVE|WRMEM|BR1|<INCA|SP0>>
1549 015134 001283      LDMA IMM,REPST ;ADDRESS DYNAMIC REP COUNTER
(1) 015134 001283      MICPC=MICPC+1
1550 015136 001284      <MOVE|LDMAR|IMM|<REPST&377>>
(1) 015136 001284      BRWRTE MEMX,SELB ;COPY IT TO THE BR
1551 015140 001285      MICPC=MICPC+1
(1) 015140 001285      <MOVE|WRTEBR|MEMX|<SELB>>
1552 015142 001286      BSHFTB
(1) 015142 001286      MICPC=MICPC+1
1553 015144 001287      <MOVE|SHFTBR|SELB|BR>
(1) 015144 001287      MEM BR,SELB
1554 015146 001288      MICPC=MICPC+1
(1) 015146 001288      <MOVE|WRMEM|BR1|<SELB>>
1555 015148 001289      BR0 RTHRES
(1) 015148 001289      MICPC=MICPC+1
1556 015150 001290      <JUMP|BR0CON|<RTHRES-INIT&3000*4>|<RTHRES-INIT&777/2>>
(1) 015150 001290      BRWRTE IMM,201 ;MASK FOR OK TO SEND
1557 015152 001291      MICPC=MICPC+1
(1) 015152 001291      <MOVE|WRTEBR|IMM|<201>>
1558 015154 001292      SP BR,AORB,SP10 ;OR IT IN
(1) 015154 001292      MICPC=MICPC+1
1559 015156 001293      <MOVE|SPX|BR1|AORB|SP10>
(1) 015156 001293      ALWAYS IDLE
1560 015158 001294      MICPC=MICPC+1

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(1) 015144 100445      <JUMP|ALCOND|<IDLE-INIT&3000*4>|<IDLE-INIT&777/2>>
1552 015146 001294      .DSABLE LSB
1553 015148 001295      ;

```



1555 015142  
(1) 001310  
(1) 015142 120620  
1556 015144  
(1) 001311  
(1) 015144 116063  
1557 015146  
(1) 001312  
(1) 015146 000402  
1558 015150  
(1) 001313  
(1) 015150 002231  
1559 015152  
(1) 001314  
(1) 015152 002230  
1560 015154  
(1) 001315  
(1) 015154 000601  
1561 015150  
(1) 001316  
(1) 015156 113755  
1562 015160  
(1) 001317  
(1) 015160 003072  
1563 015162  
(1) 001320  
(1) 015162 010071  
1564 015164  
(1) 001321  
(1) 015164 002220  
1565 015166  
(1) 001322  
(1) 015166 000620  
1566 015170  
(1) 001323  
(1) 015170 112334  
1567 015172  
(1) 001324  
(1) 015172 000775  
1568 015174  
(1) 001325  
(1) 015174 003670  
1569 015176  
(1) 001326  
(1) 015176 112334  
1570  
1571 015200  
(1) 001327  
(1) 015200 010153  
1572 015202  
(1) 001330  
(1) 015202 016401  
1573 015204  
(1) 001331  
(1) 015204 000405  
1574 015206

TEOM: BRWRTI IBUS,UBBR  
MICPC=MICPC+1  
<MOVE!WRTEBRI!IBUS!<UBBR>>  
BR0 NXMERR ;NON-EXISTANT MEMORY  
MICPC=MICPC+1  
<JUMP!BR0CONI!<NXMERR-INIT63000\*4>!<NXMERR-INIT6777/2>>  
BRWRTI IMM,2 ;EOM TO BR  
MICPC=MICPC+1  
<MOVE!WRTEBRI!IMM!<2>>  
OUTPUT BR,<SELB!OTMTCO> ;WRITE TMR CONTROL  
MICPC=MICPC+1  
<MOVE!WROUT!BRI!<SELB!OTMTCO>>  
OUTPUT BR,<SELB!TMTDAT> ;WRITE GARBAGE DATA  
MICPC=MICPC+1  
<MOVE!WROUT!BRI!<SELB!TMTDAT>>  
BRWRTI BR,SELA!SP1 ;CHECK FOR BOOT MODE  
MICPC=MICPC+1  
<MOVE!WRTEBRI!BRI!<SELA!SP1>>  
BR7 BTEOM ;---IF SET IS MAINT MSG  
MICPC=MICPC+1  
<JUMP!BR7CONI!<BTEOM-INIT63000\*4>!<BTEOM-INIT6777/2>>  
SP BR,INCA,SP12 ;INCREMENT THE MESSAGE NUMBER  
MICPC=MICPC+1  
<MOVE!SPXIBRI!INCA!SP12>  
TEOM1: LDMA IMM,LTC ;ADDRESS LAST TMT LINK  
MICPC=MICPC+1  
<MOVE!LDMAR!IMM!<LTC6377>>  
LDMA MEMX,SELB  
MICPC=MICPC+1  
<MOVE!LDMAR!MEMX!<SELB>>  
BRWRTI MEMX,SELB  
MICPC=MICPC+1  
<MOVE!WRTEBRI!MEMX!<SELB>>  
BR0 TEOM2  
MICPC=MICPC+1  
<JUMP!BR0CONI!<TEOM2-INIT63000\*4>!<TEOM2-INIT6777/2>>  
TEOM3: BRWRTI IMM,375 ;TURN OFF MESSAGE PENDING  
MICPC=MICPC+1  
<MOVE!WRTEBRI!IMM!<375>>  
SPBR BR,AAAND,SP10 ;  
MICPC=MICPC+1  
<MOVE!SPBRX!BRI!AAAND!SP10>  
BR0 TEOM2 ;IF UNNUMB PENDING--GO AWAY  
MICPC=MICPC+1  
<JUMP!BR0CONI!<TEOM2-INIT63000\*4>!<TEOM2-INIT6777/2>>  
,SBTTL SNDACK--ROUTINE TO SEND AN ACK  
SNDACK: LDMA IMM,T  
MICPC=MICPC+1  
<MOVE!LDMAR!IMM!<T6377>>  
MEMINC IMM,1  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IMM!<1>>  
BRWRTI IMM,5  
MICPC=MICPC+1  
<MOVE!WRTEBRI!IMM!<5>>  
SA2: MEMINC IMM,300

(1) 001332  
(1) 015206 016700  
1575 015210  
(1) 001333  
(1) 015210 003310  
1576  
1577 015212  
(1) 001334  
(1) 015212 000403  
1578 015214  
(1) 001335  
(1) 015214 100451  
1579 015216  
(1) 001336  
(1) 015216 120600  
1580 015220  
(1) 001337  
(1) 015220 102045  
1581 015222  
(1) 001340  
(1) 015222 000604  
1582 015224  
(1) 001341  
(1) 015224 103505  
1583 015226  
(1) 001342  
(1) 015226 003600  
1584 015230  
(1) 001343  
(1) 015230 003620  
1585 015232  
(1) 001344  
(1) 015232 000402  
1586 015234  
(1) 001345  
(1) 015234 003004  
1587 015236  
(1) 001346  
(1) 015236 002300  
1588 015240  
(1) 001347  
(1) 015240 002004  
1589 015242  
(1) 001350  
(1) 015242 002320  
1594 015244  
(1) 001351  
(1) 015244 002105  
1591 015246  
(1) 001352  
(1) 015246 105367  
1592 015250  
(1) 001353  
(1) 015250 123200  
1593 015252  
(1) 001354

MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IMM!<300>>  
SA3: SP BR,AORB,SP10  
MICPC=MICPC+1  
<MOVE!SPXIBRI!AORB!SP10>  
; STATE TMTA  
TEOM2: MICPC=MICPC+1  
<MOVE!WRTEBRI!IMM!<TMTA-INIT6777/2>>  
ALWAYS XEXIT  
MICPC=MICPC+1  
<JUMP!ALCONDI!<XEXIT-INIT63000\*4>!<XEXIT-INIT6777/2>>  
FUDGE: BRWRTI IBUS,NPR ;READ NPR CONTROL  
MICPC=MICPC+1  
<MOVE!WRTEBRI!IBUS!<NPR>>  
BR0 IDLE ;IF NPR GOING---LEAVE  
MICPC=MICPC+1  
<JUMP!BR0CONI!<IDLE-INIT63000\*4>!<IDLE-INIT6777/2>>  
BRWRTI BR!LDMAR,SELA!SP4 ;LOAD THE MAR  
MICPC=MICPC+1  
<MOVE!WRTEBRI!BRI!LDMAR!<SELA!SP4>>  
BR7 BS2 ;IF SET - READ BACK ALL 200  
MICPC=MICPC+1  
<JUMP!BR7CONI!<BS2-INIT63000\*4>!<BS2-INIT6777/2>>  
MEMINC IBUS,INDAT1 ;OTHERWISE RESTORE TWO BYTES  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IBUS!<INDAT1>>  
MEMINC IBUS,INDAT2 ;..  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IBUS!<INDAT2>>  
BRWRTI IMM,2 ;UPDATE---UNIBUS ADDRESS  
MICPC=MICPC+1  
<MOVE!WRTEBRI!IMM!<2>>  
SP BR,ADD,SP4 ;UPDATE NPR COUNTER  
MICPC=MICPC+1  
<MOVE!SPXIBRI!ADD!SP4>  
SP IBUS,IRA1,SP0 ;UPDATE ADDRESS LOW  
MICPC=MICPC+1  
<MOVE!SPXIBUS!IRA1!SP0>  
OUTPUT BR,ADD!IBA1  
MICPC=MICPC+1  
<MOVE!WROUT!BRI!<ADD!IBA1>>  
SP IBUS,IBA2,SP0 ;READ HIGH ADDRESS  
MICPC=MICPC+1  
<MOVE!SPXIBUS!IBA2!SP0>  
OUTPUT BR,AC!IBA2 ;UPDATE HIGH  
MICPC=MICPC+1  
<MOVE!WROUT!BRI!<AC!IBA2>>  
C RESEXT ;IF CARRY---UPDATE MXT  
MICPC=MICPC+1  
<JUMP!CCONDI!<RESEXT-INIT63000\*4>!<RESEXT-INIT6777/2>>  
RES1: SP IBUS,NPR,SP0 ;READ NPR REGISTER  
MICPC=MICPC+1  
<MOVE!SPXIBUS!NPR!SP0>  
ALWAYS TH3X  
MICPC=MICPC+1  
<GO DO ANOTHER NPR

(1) 015252 112574  
1594 015254 001355  
(1) 015254 000774  
1595 015256 001356  
(1) 015256 003270  
1596 015260 001357  
(1) 015260 003233  
1597  
1598 015262 001360  
(1) 015262 010070  
1599 015264 001361  
(1) 015264 043220  
1600 015266 001362  
(1) 015266 000431  
(1) 015270 001363  
(1) 015270 003222  
1601 015272 001364  
(1) 015272 114534  
1602 015274 001365  
(1) 015274 000715  
(1) 015276 001366  
(1) 015276 003223  
1603 015300 001367  
(1) 015300 123200  
1610 015302 000621  
(1) 015302 001370  
(1) 015302 000621  
1611 015304 001371  
(1) 015304 104643  
1613 015306 001372  
(1) 015306 023120  
1614 015310 001373  
(1) 015310 002065  
1615 015312 001374  
(1) 015312 111376  
1616 015314 001375  
(1) 015314 110565  
1617  
1618 015316 001376  
(1) 015316 123200  
1619 015320

<JUMPIALCONDI<TH3X-INIT&3000\*4>1<TH3X-INIT&777/2>>  
BRWRT IMM,374 ;MASK FOR CLEAR MSG PENDING  
MICPC=MICPC+1  
<MOVE!WRTEBRI!MM1<374>>  
SP BR, AANDB, SP10 ;TURN THEM OFF IN LINE STATUS WORD  
MICPC=MICPC+1  
<MOVE!SPXIBRI!AANDB!SP10>  
SP BR, SELB, SP13 ;STORE UNRECOGNIZABLE VALUE INTO SP13  
MICPC=MICPC+1  
<MOVE!SPXIBRI!SELB!SP13>  
LDMA IMM,STC ;SO "RH3" WILL EXIT BACK TO IDLE LOOP  
MICPC=MICPC+1 ;ADDRESS START OF TMT CHAIN  
<MOVE!LDMAR!MM1<STC&377>>  
SP MEMX, SELB, SP0 ;COPY LINK ADDRESS  
MICPC=MICPC+1  
<MOVE!SPX!MEMX!SELB!SP0>  
TSTATE NUMSYN ;CHANGE XMIT STATE TO LINE IS IDLE  
MICPC=MICPC+1  
<MOVE!WRTEBRI!MM1<NUMSYN-INIT&777/2>>  
MICPC=MICPC+1  
<MOVE!SPX!BR!SELB!SP2>  
ALWAYS TDON2 ;POST A DONE  
MICPC=MICPC+1  
<JUMPIALCONDI<TDON2-INIT&3000\*4>1<TDON2-INIT&777/2>>  
RSTATE RCVL  
MICPC=MICPC+1  
<MOVE!WRTEBRI!MM1<RCVL-INIT&777/2>>  
MICPC=MICPC+1  
<MOVE!SPX!BR!SELB!SP3>  
SP IBUS, NPR, SP0 ;READ NPR CONTROL REGISTER  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!NPR!SP0>  
BRWRT IMM,221  
MICPC=MICPC+1  
<MOVE!WRTEBRI!MM1<221>>  
ALWAYS RK7  
MICPC=MICPC+1  
<JUMPIALCONDI<RK7-INIT&3000\*4>1<RK7-INIT&777/2>>  
HOINCH: SP IBUS, IIBA2, SP0  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!IIBA2!SP0>  
OUTPUT BR, INCA!IBA2 ;OUTPUT INCREMENTED BA  
MICPC=MICPC+1  
<MOVE!WROUTIBRI!INCA!IBA2>  
C 56 ;INCREMENT BYTEW COUNT  
MICPC=MICPC+1  
<JUMPIALCONDI<56-INIT&3000\*4>1<56-INIT&777/2>>  
ALWAYS TH8  
MICPC=MICPC+1  
<JUMPIALCONDI<TH8-INIT&3000\*4>1<TH8-INIT&777/2>>  
;INCREMENT MXT BITS  
56: SP IBUS, NPR, SP0 ;READ NPR REG IWITH CURRENT MXT BITS  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!NPR!SP0>  
BRWRT IMM,4 ;WRITE BIT TO ADD

(1) 015320 001377  
(1) 015320 000404  
1620 015322 001400  
(1) 015322 001400  
1621 015324 001403  
(1) 015324 001403  
(1) 015324 110565  
1622  
1623 015326 001402  
(1) 015326 000710  
1624 015330 001403  
(1) 015330 100451  
1625

MICPC=MICPC+1  
<MOVE!WRTEBRI!MM1<4>>  
OUT BR, <ADD!ONPR> ;TURN ON PROPER MXT BITS  
MICPC=MICPC+1  
<MOVE!WROUTIBRI!<ADD!ONPR>>  
ALWAYS TH8  
MICPC=MICPC+1  
<JUMPIALCONDI<TH8-INIT&3000\*4>1<TH8-INIT&777/2>>  
; STATE TEOM  
HEH1: MICPC=MICPC+1  
<MOVE!WRTEBRI!MM1<TEOM-INIT&777/2>>  
ALWAYS XEXIT  
MICPC=MICPC+1  
<JUMPIALCONDI<XEXIT-INIT&3000\*4>1<XEXIT-INIT&777/2>>  
;

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1627      ,SBTTL REP HANDLER
1628 015332 REP: LDMA IMM,REPCR ;LOAD MAR ADDRESS WITH POINTER TO REPS RECC
(1) 001404 MICPC=MICPC+1
(1) 015332 010016 <MOVE!LDMAR!IMM!<REPCR&377>>
1629 015334 SP HEXX,SELB,SP0 ;READ NUMBER OF REPS RECD
(1) 001405 MICPC=MICPC+1
(1) 015334 043220 <MOVE!SP!MEMX!SELB!SP0>
1630 015336 MEM DP,<INCA!SP0> ;INCREMNT R&PS RECD
(1) 001406 MICPC=MICPC+1
(1) 015336 002460 <MOVE!WRMEM!DP!<INCA!SP0>>
1631 015340 LDMA IMM,T ;LOAD ADDRESS OF TYPE FIELD
(1) 001407 MICPC=MICPC+1
(1) 015340 040153 <MOVE!LDMAR!IMM!<T&377>>
1632 015342 MEMINC IMM,2 ;LOAD NAK TYPE
(1) 001410 MICPC=MICPC+1
(1) 015342 016402 <MOVE!WRMEM!INCMAR!IMM!<2>>
1633 015344 MEMINC IMM,303 ;LOAD REP RESPONSE SUB-TYPE
(1) 001411 MICPC=MICPC+1
(1) 015344 016703 <MOVE!WRMEM!INCMAR!IMM!<303>>
1634 015346 ALWAYS SNAK ;SEND AN UNNUMB MSG
(1) 001412 MICPC=MICPC+1
(1) 015346 114712 <JUMP!ALCOND!<SNAK-INIT&3000*4>!<SNAK-INIT&777/2>>
1635
1636 J
1637 015350 START: ,SBTTL START HANDLER
(1) 001413 BRWRT DP,<SELA!SP10> ;READ LINE STATUS WORD
(1) 015350 000610 MICPC=MICPC+1
1638 015352 <MOVE!WRTEBR!DP!<SELA!SP10>>
(1) 001414 BRSHFT ;GET START MODE BIT IN TESTABLE POSITION
(1) 015352 001620 MICPC=MICPC+1
1639 015351 <MOVE!SHFTBR!WRTEBR!SELB>
(1) 001415 BR4 109 ;IF IN START MODE SET STACK
(1) 015351 117021 MICPC=MICPC+1
1640 <JUMP!BR4CONI!<106-INIT&3000*4>!<106-INIT&777/2>>
1641 015356 LDMA IMM,<<RTHRS+3>> ;ELSE SET UP START ERROR
(1) 001416 MICPC=MICPC+1
(1) 015356 010177 <MOVE!LDMAR!IMM!<<RTHRS+3>&377>>
1642 015360 BRWRT IMM,200
(1) 001417 MICPC=MICPC+1
(1) 015360 000600 <MOVE!WRTEBR!IMM!<200>>
1643 015362 ALWAYS RCEXY
(1) 001420 MICPC=MICPC+1
(1) 015362 114525 <JUMP!ALCOND!<RCEXY-INIT&3000*4>!<RCEXY-INIT&777/2>>
1644 015364 106: LDMA IMM,T ;SET UP ADDRESS OF TYPE FIELD
(1) 001421 MICPC=MICPC+1
(1) 015364 010153 <MOVE!LDMAR!IMM!<T&377>>
1645 015366 MEMINC IMM,7 ;WRITE STACK TYPE
(1) 001422 MICPC=MICPC+1
(1) 015366 016407 <MOVE!WRMEM!INCMAR!IMM!<7>>
1646 015370 BRWRT IMM,11 ;SET START RECD AND UNNUMB PENDING
(1) 001423 MICPC=MICPC+1
(1) 015370 000411 <MOVE!WRTEBR!IMM!<11>>
1647 015372 ALWAYS SA2 ;SEND THE UNNUMBERED MESSAGE
(1) 001424 MICPC=MICPC+1
(1) 015372 110732 <JUMP!ALCOND!<SA2-INIT&3000*4>!<SA2-INIT&777/2>>
1648 J

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1649      ,SBTTL STACK HANDLER
1650 015374 STACK: BRWRT IMM,327 ;MASK TO CLEAR START MODE
(1) 001425 MICPC=MICPC+1
(1) 015374 020727 <MOVE!WRTEBR!IMM!<327>>
1651 015376 SP BR,AANDB,SP10 ;CLEAR START MODE
(1) 001426 MICPC=MICPC+1
(1) 015376 003270 <MOVE!SP!BR!AANDB!SP10>
1652 015401 ALWAYS TIME1 ;RESET TIMER AND IDLE
(1) 001427 MICPC=MICPC+1
(1) 015401 110662 <JUMP!ALCOND!<TIME1-INIT&3000*4>!<TIME1-INIT&777/2>>

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1654 015402 001430  
(1) 015402 023160  
1655 015404 001431  
(1) 015404 062067  
1656 015406 001432  
(1) 015406 115034  
1657 015410 001433  
(1) 015410 104660  
1658 015412 001434  
(1) 015412 123220  
1660 015414 001435  
(1) 015414 000404  
1661 015416 001436  
(1) 015416 061011  
1662 015420 001437  
(1) 015420 104660  
1663 015422 001440  
(1) 015422 003200  
1664 015424 001441  
(1) 015424 062212  
1665 015426 001442  
(1) 015426 104575  
1666 015430 001443  
(1) 015430 010070  
1667 015432 001444  
(1) 015432 057220  
1668 015434 001445  
(1) 015434 062000  
1669 015436 001446  
(1) 015436 060477  
1670 015440 001447  
(1) 015440 063232  
1671 015442 001450  
(1) 015442 000406  
1672 015444 001451  
(1) 015444 063310

ICBA22: SP IBUS,IOBA2,SP0 ;READTHEHIGH ORDERBITS OF BA TO SP0  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!IOBA2!SP0>  
OUTPUT DP,<INCA!IOBA2> ;OUTPUT THE INCREMENTED COUNT  
MICPC=MICPC+1  
<MOVE!WROUT!DP!<INCA!IOBA2>>  
C 58 ;IF CARRY SET INCREMENT THE NXTBITS  
MICPC=MICPC+1  
<JUMP!COND!<58-INIT&3000\*4>!<58-INIT&777/2>>  
ALWAYS RK9  
MICPC=MICPC+1  
<JUMP!ALCOND!<RK9-INIT&3000\*4>!<RK9-INIT&777/2>>  
?  
58: SP IBUS,UBBR,SP0  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!UBBR!SP0>  
BRWRTE IMM,4  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<4>>  
OUT BR,<ADD!OBR>  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<ADD!OBR>>  
ALWAYS RK9  
MICPC=MICPC+1  
<JUMP!ALCOND!<RK9-INIT&3000\*4>!<RK9-INIT&777/2>>  
FLUSH1: SP IMM,200,SP0 ;FLUSH THE RECVR  
MICPC=MICPC+1  
<MOVE!SPX!IMM!200!SP0>  
OUTPUT BR,<SELA!ORCVC0>  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<SELA!ORCVC0>>  
ALWAYS CG1  
MICPC=MICPC+1  
<JUMP!ALCOND!<CG1-INIT&3000\*4>!<CG1-INIT&777/2>>  
NAK: LDMA IMM,STC ;ADDRESS START OF TMT CHAIN  
MICPC=MICPC+1  
<MOVE!LDMAR!IMM!<STC&377>>  
SP MEMX!INCMAR,SELB,SP0 ;COPY IT TO SP0  
MICPC=MICPC+1  
<MOVE!SPX!MEMX!INCMAR!SELB!SP0>  
MEM BR,SELA!SP0 ;COPY START OF CHAIN  
MICPC=MICPC+1  
<MOVE!WRMEM!BR!<SELA!SP0>>  
BRWRTE BR,INCA!SP17 ;GETLASTMESSAGE ACKED  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR!<INCA!SP17>>  
SP BR,SELB,SP12 ;COPY TO CURRENT NUMBER  
MICPC=MICPC+1  
<MOVE!SPX!BR!SELB!SP12>  
BRWRTE IMM,6 ;WRITE NUMBERED MSG PENDING  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<6>>  
; AND LINE HAS COME IDLE  
SP BR,AORB,SP10 ;SET IT IN LINE STATUS WORD  
MICPC=MICPC+1  
<MOVE!SPX!BR!AORB!SP10>

1674 015446 001452  
(1) 015446 063235  
1675 015450 001453  
(1) 015450 110720  
1676 015452 001454  
(1) 015452 000415  
1677 015454 001455  
(1) 015454 123220  
1678 015456 001456  
(1) 015456 063260  
1679 015460 001457  
(1) 015460 000600  
1680 015462 001461  
(1) 015462 061311  
1681 015464 001461  
(1) 015464 123000  
1682 015466 001462  
(1) 015466 100563  
1683

SP BR,SELB,SP15 ;RESET TIMER COUNT  
MICPC=MICPC+1  
<MOVE!SPX!BR!SELB!SP15>  
ALWAYS TEOM1  
MICPC=MICPC+1  
<JUMP!ALCOND!<TEOM1-INIT&3000\*4>!<TEOM1-INIT&777/2>>  
ININT: BRWRTE IMM,15 ;MASK FOR TURN OFF ALB BUT EXT MEM BITS + NXM  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<15>>  
SP IBUS,UBBR,SP0 ;READ BR CONTROL REGISTER  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!UBBR!SP0>  
SP BR,AANDB,SP0 ;MASK OFF VECTOR TO X04  
MICPC=MICPC+1  
<MOVE!SPX!BR!AANDB!SP0>  
BRWRTE IMM,200 ;MASK FOR INTERRUPT  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<200>>  
OUT BR,AORB!OBR ;INTERRUPT  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<AORB!OBR>>  
SP IBUS,INCON,SP0 ;RESTORE INPUT CONTROLCSR  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!INCON!SP0>  
ALWAYS NIDLE4  
MICPC=MICPC+1  
<JUMP!ALCOND!<NIDLE4-INIT&3000\*4>!<NIDLE4-INIT&777/2>>  
?

```

1665
1686 @15470
(1) @01463
(1) @15470 @010177
1687 @15472
(1) @01464
(1) @15472 @016401
1688 @15474
(1) @01465
(1) @15474 @02400
1689 @15476
(1) @01466
(1) @15476 @03230
1690 @15500
(1) @01467
(1) @15500 114527

```

```

.SBTTL NXMERR ---NON EXISTANT MEMORY HANDLER
NXMERR: LDMA IMM,<<RTHRS+3>> ;ADDRESS ERROR LINK
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<<RTHRS+3>>@377>>
MEMINC IMM,1
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IMM!<1>>
NEM IMM,0 ;NXM ERROR BIT
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<0>>
SP MEMX,SELB,SP10 ;CLEAR STATUS
MICPC=MICPC+1
<MOVE!SPX!MEMX!SELB!SP10>
ALWAYS RCXXX
MICPC=MICPC+1
<JUMP!ALCOND!<RCXXX-INIT@3000*4>!<RCXXX-INIT@777/2>>

```

```

1692
1693
1694 @15502
(1) @01470
(1) @15502 @23605
1695 @15504
(1) @01471
(1) @15504 117477
1696 @15506
(1) @01472
(1) @15506 @060525
1697 @15510
(1) @01473
(1) @15510 117502
1698 @15512
(1) @01474
(1) @15512 @00477
1699 @15514
(1) @01475
(1) @15514 @63665
1700 @15516
(1) @01476
(1) @15516 164463
1701
1702 @15520
(1) @01477
(1) @15520 @00600
1703 @15522
(1) @01500
(1) @15522 @63310
1704 @15524
(1) @01501
(1) @15524 114472
1705 @15526
(1) @01502
(1) @15526 @00420
1706 @15530
(1) @01503
(1) @15530 @63310
1707 @15532
(1) @01504
(1) @15532 114474

```

```

.SBTTL SELQSY--ROUTINETOCHECK SELECT AND QSYNC AND DIDDLE LINE STATUS WORD
;USES SP5, ALWAYS CALLED BY FIRST INSTR IN A RSTATE
SELQSY: SPBR IBUS,RCVDAT,SP5 ;READCHARACTERINTO SP5 AND THE BR
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!RCVDAT!SP5>
BR7 155 ;SELECT SET?--BRANCH
MICPC=MICPC+1
<JUMP!BR7CON!<155-INIT@3000*4>!<155-INIT@777/2>>
55: BRWRTE BR,AA!SP5 ;SHIFTBR LEFT
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<AA!SP5>>
BR7 208 ;FINAL SET?
MICPC=MICPC+1
<JUMP!BR7CON!<208-INIT@3000*4>!<208-INIT@777/2>>
105: BRWRTE IMM,77 ;MASK TO BR
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<77>>
SPBR BR,AA!SP5 ;TURN OFF SELECTANDFINAL
MICPC=MICPC+1
<MOVE!SPBRX!BRI!AA!SP5>
ALWAYS BR,INCA,SP3!PAGE1
MICPC=MICPC+1
<JUMP!ALCOND!BR!INCA!SP3!PAGE1>
;
155: BRWRTE IMM,200 ;SET OK TO SEND
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<200>>
SP BR,AORB,SP10 ;IN LINE STATUS WORD
MICPC=MICPC+1
<MOVE!SPX!BR!AORB!SP10>
ALWAYS 55
MICPC=MICPC+1
<JUMP!ALCOND!<55-INIT@3000*4>!<55-INIT@777/2>>
205: BRWRTE IMM,20 ;SETCLEARACTIVE
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<20>>
SP BR,AORB,SP10 ;IN LINE STATUS WORD
MICPC=MICPC+1
<MOVE!SPX!BR!AORB!SP10>
ALWAYS 105
MICPC=MICPC+1
<JUMP!ALCOND!<105-INIT@3000*4>!<105-INIT@777/2>>

```

1709  
1710 115534  
(1) 001505  
(1) 015534 020540  
1711 015536  
(1) 001506  
(1) 015536 116111  
1716 015549  
(1) 001507  
(1) 015540 000074  
1717 015542  
(1) 001510  
(1) 015542 104422  
1718  
1719 015544  
(1) 001511  
(1) 015544 000626  
1720 015546  
(1) 001512  
(1) 015546 104422  
1721  
1722 015550  
(1) 001513  
(1) 015550 040364  
1723 015552  
(1) 001514  
(1) 015552 115116  
1724 015554  
(1) 001515  
(1) 015554 104475  
1725 015556  
(1) 001516  
(1) 015556 010153  
1726 015560  
(1) 001517  
(1) 015560 010402  
1727 015562  
(1) 001520  
(1) 015562 002711  
1728 015564  
(1) 001521  
(1) 015564 010175  
1729 015566  
(1) 001522  
(1) 015566 036540  
1730 015570  
(1) 001523  
(1) 015570 036560  
1731 015572  
(1) 001524  
(1) 015572 000420  
1732 015574  
(1) 001525  
(1) 015574 016400  
1733 015576  
(1) 001526

```

;FUGITIVE RECEIVE ROUTINES---DON'T FIT IN PAGE
RH1: BRWRT IBUS,IOBA1 ;READ LOW BYTE OF IN BA
      MICPC=MICPC+1
      <MOVE>WRTEBRI<IBUS1<IOBA1>>
      BR0 RCYODD ;IF SET IS ODD TRANSFER
      MICPC=MICPC+1
      <JUMP>BR7CONI<RCYODD-INIT&3000*4>|<RCYODD-INIT&777/2>>
      STATE RCVKE0
      MICPC=MICPC+1
      <MOVE>WRTEBRI<IMM1<RCVKE0-INIT&777/2>>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP>ALCONDI<REXIT-INIT&3000*4>|<REXIT-INIT&777/2>>
;
RCYODD: STATE RCVK01
        MICPC=MICPC+1
        <MOVE>WRTEBRI<IMM1<RCVK01-INIT&777/2>>
        ALWAYS REXIT
        MICPC=MICPC+1
        <JUMP>ALCONDI<REXIT-INIT&3000*4>|<REXIT-INIT&777/2>>
;
RCLOW: CMP MEMX,SP4 ;COMPARE LOW ORDER BITS OF COUNT
        MICPC=MICPC+1
        <SUBTC>MEMX<ISP4>
        C RCFATL ;CARRY--TOO BIG
        MICPC=MICPC+1
        <JUMP>C<CONDI<RCFATL-INIT&3000*4>|<RCFATL-INIT&777/2>>
        ALWAYS RCS ;ELSE CONTINUE
        MICPC=MICPC+1
        <JUMP>ALCONDI<RCS-INIT&3000*4>|<RCS-INIT&777/2>>
;
RCFATL: LDMA IMM,1
        MICPC=MICPC+1
        <MOVE>LDMAR<IMM1<T&377>>
        MEMINC IMM,2
        MICPC=MICPC+1
        <MOVE>MEM<INCMAR<IMM1<2>>
        MEM IMM,311
        MICPC=MICPC+1
        <MOVE>MEM<IMM1<311>>
        LDMA IMM,<<RTHR&+1>> ;ADDRESS ERROR LINK
        MICPC=MICPC+1
        <MOVE>LDMAR<IMM1<<RTHR&+1>>&377>>
        MEMINC IBUS,IOBA1
        MICPC=MICPC+1
        <MOVE>MEM<INCMAR<IBUS1<IOBA1>>
        MEMINC IBUS,IOBA2
        MICPC=MICPC+1
        <MOVE>MEM<INCMAR<IBUS1<IOBA2>>
        BRWRT IMM,20
        MICPC=MICPC+1
        <MOVE>WRTEBRI<IMM1<20>>
;
RCEXY: MEMINC IMM,0
        MICPC=MICPC+1
        <MOVE>MEM<INCMAR<IMM1<0>>
        MEM BR,SELB
        MICPC=MICPC+1

```

(1) 015576 062620  
1734 015600  
(1) 001527  
(1) 015600 002212  
1735 015602  
(1) 001530  
(1) 015602 003001  
1736 015604  
(1) 001531  
(1) 015604 114674  
1737  
1738 015606  
(1) 001532  
(1) 015606 040757  
1739 015610  
(1) 001533  
(1) 015610 187567  
1740 015612  
(1) 001534  
(1) 015612 070200  
1741 015614  
(1) 001535  
(1) 015614 002400  
1742 015616  
(1) 001536  
(1) 015616 010070  
1743 015620  
(1) 001537  
(1) 015620 002473  
1744 015622  
(1) 001540  
(1) 015622 000545  
1745 015624  
(1) 001541  
(1) 015624 000360  
1746 015626  
(1) 001542  
(1) 015626 115545  
1747 015630  
(1) 001543  
(1) 015630 000406  
1748 015632  
(1) 001544  
(1) 015632 062400  
1749 015634  
(1) 001545  
(1) 015634 010241  
1750 015636  
(1) 001546  
(1) 015636 053223  
1751  
1752 015640  
(1) 001547  
(1) 015640 016600  
1753 015642  
(1) 001550

```

;
RCEXX: <MOVE>MEM<IBUS1<SELB>>
        OUTPUT IMM,<2001ORCVCO> ;FLUSH THE INPUT SILO
        MICPC=MICPC+1
        <MOVE>WROUT<IMM1<2001ORCVCO>>
        SP IMM,1,SP1 ;SET INIT MODE IN PORT STATUS WORD
        MICPC=MICPC+1
        <MOVE>SP<IMM1<1SP1>
        ALWAYS NTRS1
        MICPC=MICPC+1
        <JUMP>ALCONDI<NTRS1-INIT&3000*4>|<NTRS1-INIT&777/2>>
;
TDON3: BRWRT MEMX,SUB1SP17 ;COMPARE RESPONSE TO MSG NO
        MICPC=MICPC+1
        <MOVE>WRTEBRI<MEMX1<SUB1SP17>>
        BR7 RH3 ;IF NEGATIVE EXIT
        MICPC=MICPC+1
        <JUMP>BR7CONI<RH3-INIT&3000*4>|<RH3-INIT&777/2>>
;
TDON2: LDMA BR,SELA1SP0 ;ADDRESS THE TRANSMI LINK
        MICPC=MICPC+1
        <MOVE>LDMAR<IBRI<SELA1SP0>>
        MEM IMM,0
        MICPC=MICPC+1
        <MOVE>MEM<IMM1<0>>
        LDMA IMM,STC
        MICPC=MICPC+1
        <MOVE>LDMAR<IMM1<STC&377>>
        MEM IMM,TML1 ;ASSUME WRAPAROUND
        MICPC=MICPC+1
        <MOVE>MEM<IMM1<TML1>>
        BRWRT IMM,TML0 ;WRAPAROUND?
        MICPC=MICPC+1
        <MOVE>WRTEBRI<IMM1<TML0>>
        CMP BR,SP0
        MICPC=MICPC+1
        <SUBTC>IBRI<SP0>
        Z TDON4 ;YES
        MICPC=MICPC+1
        <JUMP>Z<CONDI<TDON4-INIT&3000*4>|<TDON4-INIT&777/2>>
        BRWRT IMM,6 ;OFFSET FOR NEXT TMT LINK
        MICPC=MICPC+1
        <MOVE>WRTEBRI<IMM1<6>>
        MEM BR,ADD1SP0 ;UPDATE THE POINTER
        MICPC=MICPC+1
        <MOVE>WRTEBRI<IBRI<ADD1SP0>>
;
IDON4: LDMA IMM,NXTSP ;ADDRESS DONE LINK
        MICPC=MICPC+1
        <MOVE>LDMAR<IMM1<NXTSP&377>>
        LDMA MEMX,SELB1SP1SP3 ;ADDRESS THE LINK,COPYING
        MICPC=MICPC+1
        <MOVE>LDMAR<MEMX1<SELB1SP1SP3>>
;
        MEMINC IMM,200 ;WRITE THE INTERRUPT TYPE
        MICPC=MICPC+1
        <MOVE>MEM<INCMAR<IMM1<200>>
        MEM BR,INCA1SP0 ;COPY ACTUAL LINK ADDRESS
        MICPC=MICPC+1

```

```

(1) 015642 062460 <MOVE!WRMEMIBRI<INCA!SP0>>
1754 015644 LDMA IMM,NXTSP ;ADDRESS PTR INT STACK
(1) 001551 MICPC=MICPC+1
(1) 015644 010241 <MOVE!LDMAR!IMM!<NXTSP&377>>
1755 015646 MEM IMM,INTSTK ;ASSUME WRAP AROUND
(1) 001552 MICPC=MICPC+1
(1) 015646 002642 <MOVE!WRMEM!IMM!<INTSTK>>
1756 015650 BRWRTE IMM,<<MMEND-2>> ;ADDRESS END OF INT STACK
(1) 001553 MICPC=MICPC+1
(1) 015650 000776 <MOVE!WRTEBRI!IMM!<<MMEND-2>>>
1757 015652 CMP BR,SP3 ;WRAP AROUND?
(1) 001554 MICPC=MICPC+1
(1) 015652 002363 <SUBTC!BRI!SP3>
1758 015654 Z TDON40 ;YES---BRANCH
(1) 001555 MICPC=MICPC+1
(1) 015654 115560 <JUMP!ZCOND!<TDON40-INIT&3000+4>!<TDON40-INIT&777/2>>
1759 015656 BRWRTE IMM,2 ;OFFSET TO NEXT PAIR
(1) 001556 MICPC=MICPC+1
(1) 015656 000402 <MOVE!WRTEBRI!IMM!<2>>
1760 015660 MEM BR,ADD!SP3 ;UPDATE POINTER
(1) 001557 MICPC=MICPC+1
(1) 015660 002403 <MOVE!WRMEMIBRI<ADD!SP3>>
1761 015662 TDON40: BRWRTE IMM,20 ;WRITE INTERRUPT PENDING
(1) 001560 MICPC=MICPC+1
(1) 015662 000420 <MOVE!WRTEBRI!IMM!<20>>
1762 015664 SP BR,AORB,SP1 ;IN PORT STATUS WORD
(1) 001561 MICPC=MICPC+1
(1) 015664 003301 <MOVE!SP!IBRI!AORB!SP1>
1763 015666 LDMA IMM,ETC ;ADDRESS NEXT EMPTY PTR
(1) 001562 MICPC=MICPC+1
(1) 015666 010072 <MOVE!LDMAR!IMM!<ETC&377>>
1764 015670 SP MEMX,SELB,SP0 ;COPY IT TO SP0
(1) 001563 MICPC=MICPC+1
(1) 015670 043220 <MOVE!SP!IMEMX!SELB!SP0>
1765 015672 LDMA IMM,STC ;GET NEXT DONE PTR
(1) 001564 MICPC=MICPC+1
(1) 015672 010070 <MOVE!LDMAR!IMM!<STC&377>>
1766 015674 CMP MEMX,SP0 ;IDENTICAL?
(1) 001565 MICPC=MICPC+1
(1) 015674 040360 <SUBTC!MEMX!SP0>
1767 015676 Z RH3 ;FINISH PROCESSING HEADER
(1) 001566 MICPC=MICPC+1
(1) 015676 105567 <JUMP!ZCOND!<RH3-INIT&3000+4>!<RH3-INIT&777/2>>
1768
1769 015700 TDON1: LDMA IMM,ISP17 ;GET LAST ACKED
(1) 001567 MICPC=MICPC+1
(1) 015700 010155 <MOVE!LDMAR!IMM!<ISP17&377>>
1770 015702 SP MEMX,SELB,SP17 ;STORE IT IN SP17
(1) 001570 MICPC=MICPC+1
(1) 015702 043237 <MOVE!SP!IMEMX!SELB!SP17>
1771 015704 LDMA IMM,STC ;GET START OF TMT CHAIN
(1) 001571 MICPC=MICPC+1
(1) 015704 010070 <MOVE!LDMAR!IMM!<STC&377>>
1772 015706 LDMA MEMX,SELB!SPBRX!SP0 ;ADDRESS THE LINK
(1) 001572 MICPC=MICPC+1
(1) 015706 053620 <MOVE!LDMAR!MEMX!<SELB!SPBRX!SP0>>

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1773 015710 BRWRTE MEMX!INCHAR,SELB ;GET THE FLAGS
(1) 001573 MICPC=MICPC+1
(1) 015710 054020 <MOVE!WRTEBRI!MEMX!INCHAR!<SELB>>
1774 015712 BR1 TDON3 ;IF BUFFER ASSIGNED PROCEED
(1) 001574 MICPC=MICPC+1
(1) 015712 116532 <JUMP!BRI!CON!<TDON3-INIT&3000+4>!<TDON3-INIT&777/2>>
1775 015714 ALWAYS RH3 ;ELSE---EXIT
(1) 001575 MICPC=MICPC+1
(1) 015714 104567 <JUMP!ALCOND!<RH3-INIT&3000+4>!<RH3-INIT&777/2>>
1776
1777 015716 OVRUN: BRWRTE IMM,4
(1) 001576 MICPC=MICPC+1
(1) 015716 000404 <MOVE!WRTEBRI!IMM!<4>>
1778 015720 ALWAYS NTR00
(1) 001577 MICPC=MICPC+1
(1) 015720 114671 <JUMP!ALCOND!<NTR00-INIT&3000+4>!<NTR00-INIT&777/2>>
1779
1780 ; INPUTS:
1781 ; SP0 = RECEIVE CHARACTER
1782
1783 015722 PASWRD: SP IBUS,LNOSW,SP16 ;READ PASSWD SWITCH
(1) 001600 MICPC=MICPC+1
(1) 015722 023336 <MOVE!SP!IBUS!LNOSW!SP16>
1784 015724 Z 105 ;IF ALL ONES NO RLD ENABLED
(1) 001601 MICPC=MICPC+1
(1) 015724 115605 <JUMP!ZCOND!<105-INIT&3000+4>!<105-INIT&777/2>>
1785 015726 BRWRTE IMM,6 ;CHECK FOR ENTER MOP MODE
(1) 001602 MICPC=MICPC+1
(1) 015726 000406 <MOVE!WRTEBRI!IMM!<6>>
1786 015730 CMP BR,SP0
(1) 001603 MICPC=MICPC+1
(1) 015730 000360 <SUBTC!BRI!SP0>
1787 015732 Z 205 ;IF EQUAL ENTER MOP
(1) 001604 MICPC=MICPC+1
(1) 015732 115613 <JUMP!ZCOND!<205-INIT&3000+4>!<205-INIT&777/2>>
1788 015734 105: BRWRTE BR,SELA!SP1 ;READ STATUS BYTE
(1) 001605 MICPC=MICPC+1
(1) 015734 000001 <MOVE!WRTEBRI!BRI!<SELA!SP1>>
1789 015736 BRSHFT ;SHIFT IT RIGHT
(1) 001606 MICPC=MICPC+1
(1) 015736 001620 <MOVE!SHFTBRI!WRTEBRI!SELB>
1790 015740 BFI RHX ;MESSAGE WITH NO BUFFER ASSIGNED
(1) 001607 MICPC=MICPC+1
(1) 015740 106751 <JUMP!BRI!CON!<RHX-INIT&3000+4>!<RHX-INIT&777/2>>
1791 015742 BRSHFT ;SHIFT RIGHT AGAIN
(1) 001610 MICPC=MICPC+1
(1) 015742 001620 <MOVE!SHFTBRI!WRTEBRI!SELB>
1792 015744 BFI RCV00 ;DLE RECEIVED IN NORMAL MODE
(1) 001611 MICPC=MICPC+1
(1) 015744 106743 <JUMP!BFI!CON!<RCV00-INIT&3000+4>!<RCV00-INIT&777/2>>
1793 015746 ALWAYS RK3 ;HANDLE MAINT MODE MESSAGE
(1) 001612 MICPC=MICPC+1
(1) 015746 104001 <JUMP!ALCOND!<RK3-INIT&3000+4>!<RK3-INIT&777/2>>
1794 015750 205: SP BR,DECA!SP4 ;COUNT FOR NUMB OF COMPARES
(1) 001613 MICPC=MICPC+1
(1) 015750 003164 <MOVE!SP!BR!DECA!SP4>

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1795 015752 STATE EM2
(1) 001614 MICPC=MICPC+1
(1) 015752 009746 <MOVE!WTEBR!IMM!<EM2-INIT6777/2>>
1796 015754 ALWAYS REXIT
(1) 001615 MICPC=MICPC+1
(1) 015754 104422 <JUMPIALCONDI<REXIT-INIT63000*4>|<REXIT-INIT6777/2>>
1797 015756 HCYM1: LDMA IMM,ISP11 ;ADDRESS SP11 IMAGE
(1) 001616 MICPC=MICPC+1
(1) 015755 013171 <MOVE!LDMAR!IMM!<ISP114377>>
1798 015760 MEM BR,DECA!SP11 ;COPY SP11
(1) 001617 MICPC=MICPC+1
(1) 015760 062571 <MOVE!WRMEM!BRI<DECA!SP11>>
1799 015762 LDMA IMM,NXTSP
(1) 001620 MICPC=MICPC+1
(1) 015762 010241 <MOVE!LDMAR!IMM!<NXTSP6377>>
1800 015764 SP MEMX!LDMAR,SELB,SP3 ;COPY TO SP3
(1) 001621 MICPC=MICPC+1
(1) 015764 053223 <MOVE!SPX!MEMX!LDMAR!SELB!SP3>
1801 015766 MEMINC IMM,204 ;RECEIVE DONE IMAGE
(1) 001622 MICPC=MICPC+1
(1) 015766 016604 <MOVE!WRMEM!INCMAR!IMM!<204>>
1802 015770 MEM BR!LDMAR,SELA!SP14 ;COPY LINK ADDRESS TO NEXT INTE
(1) 001623 MICPC=MICPC+1
(1) 015770 072614 <MOVE!WPMEM!BRI!LDMAR!<SELA!SP14>>
1803 015772 MEMINC IMM,0 ;ZERO THE FLAGS
(1) 001624 MICPC=MICPC+1
(1) 015772 016400 <MOVE!WRMEM!INCMAR!IMM!<0>>
1804 015774 SP IBUS,IOBA1,SP4 ;GET BEGIN ADDRESS LOW
(1) 001625 MICPC=MICPC+1
(1) 015774 023144 <MOVE!SPX!IBUS!IOBA1!SP4>
1805 015776 SP IBUS,IOBA2,SP5 ;AND HIGH BYTE
(1) 001626 MICPC=MICPC+1
(1) 015776 023165 <MOVE!SPX!IBUS!IOBA2!SP5>
1806 016000 SP MEMX!INCMAR,SUB,SP4 ;SUBTRACT TO GET COUNT
(1) 001627 MICPC=MICPC+1
(1) 016000 057344 <MOVE!SPX!MEMX!INCMAR!SUB!SP4>
1807 016002 C 108 ;IF CARRY SET THEN NO CARRY!
(1) 001630 MICPC=MICPC+1
(1) 016002 115232 <JUMPICCONDI<108-INIT63000*4>|<108-INIT6777/2>>
1808 016004 SP BR,DECA,SP5 ;DECREMENT HIGH BYTE OF ADDRESS
(1) 001631 MICPC=MICPC+1
(1) 016004 063165 <MOVE!SPX!BRI!DECA!SP5>
1809 016006 SP MEMX!INCMAR,SUB,SP5 ;SUBTRACT FOR COUNT
(1) 001632 MICPC=MICPC+1
(1) 016006 057345 <MOVE!SPX!MEMX!INCMAR!SUB!SP5>
1810 016010 MEMINC BR,SELA!SP5 ;COPY TO MEMORY LINK
(1) 001633 MICPC=MICPC+1
(1) 016010 076605 <MOVE!WRMEM!INCMAR!BRI!SELA!SP5>
1811 016012 MEMINC BR,SELA!SP4
(1) 001634 MICPC=MICPC+1
(1) 016012 076604 <MOVE!WRMEM!INCMAR!BRI!SELA!SP4>
1812 016014 BRWRT IMM,2
(1) 001635 MICPC=MICPC+1
(1) 016014 000402 <MOVE!WTEBR!IMM!<2>>
1813 016016 LDMA IMM,NXTSP ;ADDRESS NEXT INT STACK
(1) 001636 MICPC=MICPC+1

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(1) 016016 010241 <MOVE!LDMAR!IMM!<NXTSP6377>>
1814 016020 MEM BR,ADD!SP3
(1) 001637 MICPC=MICPC+1
(1) 016020 062403 <MOVE!WRMEM!BRI!<ADD!SP3>>
1815 016022 BRWRT IMM,<<MMEND-2>> ;ADDRESSEND OF INT STACK
(1) 001640 MICPC=MICPC+1
(1) 016022 060776 <MOVE!WTEBR!IMM!<<MMEND-2>>>
1816 016024 CMP BR,SP3 ;WRAP AROUND
(1) 001641 MICPC=MICPC+1
(1) 016024 060363 <SUBTC!BRI!SP3>
1817 016026 Z RMIFLP ;IFYES-- BRANCH
(1) 001642 MICPC=MICPC+1
(1) 016026 115644 <JUMPIZCONDI<RMIFLP-INIT63000*4>|<RMIFLP-INIT6777/2>>
1818 016030 ALWAYS RMX1
(1) 001643 MICPC=MICPC+1
(1) 016030 114645 <JUMPIALCONDI<RMX1-INIT63000*4>|<RMX1-INIT6777/2>>
1819 016032 RMIFLP: MEM IMM,INTSTK
(1) 001644 MICPC=MICPC+1
(1) 016032 002642 <MOVE!WRMEM!IMM!<INTSTK>>
1820 016034 RMX1:
(1) 001645 LDMA IMM,LRC
(1) 016034 010024 <MOVE!LDMAR!IMM!<LRC6377>>
1822 016036 BRWRT IMM,5 ;INDEX TO NEXT BUFFER
(1) 001646 MICPC=MICPC+1
(1) 016036 000405 <MOVE!WTEBR!IMM!<5>>
1823 016040 SP BR,ADD,SP14 ;UPDATE COPY OF POINTER
(1) 001647 MICPC=MICPC+1
(1) 016040 063014 <MOVE!SPX!BRI!ADD!SP14>
1824 016042 BRWRT IMM,STC ;ADDRESS OF WRAP AROUND POINT
(1) 001650 MICPC=MICPC+1
(1) 016042 000470 <MOVE!WTEBR!IMM!<STC>>
1825 016044 CMP BR,SP14 ;WRAPAROUND?
(1) 001651 MICPC=MICPC+1
(1) 016044 060374 <SUBTC!BRI!SP14>
1826 016046 Z RMFLIP ;IF YES---BRANCH
(1) 001652 MICPC=MICPC+1
(1) 016046 115655 <JUMPIZCONDI<RMFLIP-INIT63000*4>|<RMFLIP-INIT6777/2>>
1827 016050 MEM BR,SELA!SP14 ;ELSE UPDATE THE POINTER
(1) 001653 MICPC=MICPC+1
(1) 016050 062614 <MOVE!WRMEM!BRI!SELA!SP14>
1828 016052 ALWAYS RMX
(1) 001654 MICPC=MICPC+1
(1) 016052 114656 <JUMPIALCONDI<RMX-INIT63000*4>|<RMX-INIT6777/2>>
1829 016054 RMFLIP: MEM IMM,RCL1 ;POINT TO FIRST LINK
(1) 001655 MICPC=MICPC+1
(1) 016054 000425 <MOVE!WRMEM!IMM!<RCL1>>
1830 016056 RMX: BRWRT IMM,20 ;MASK FOR INTERRUPT PENDING
(1) 001656 MICPC=MICPC+1
(1) 016056 000420 <MOVE!WTEBR!IMM!<20>>
1831 016060 SP DP,AORB,SP1 ;UPDATE PORT STATUS WORD
(1) 001657 MICPC=MICPC+1
(1) 016060 063331 <MOVE!SPX!DP!AORB!SP1>
1832 016062 BRWRT DP,<SELA!SP10> ;READ LINE STATUS WORD
(1) 001660 MICPC=MICPC+1
(1) 016062 060614 <MOVE!WTEBR!DP!<SELA!SP10>>

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1833 016964 001661  
 (1) 016964 107015  
 1834 016966 001662  
 (1) 016966 000400  
 1835 016971 001663  
 (1) 016971 104422  
 1836 016972 001664  
 (1) 016972 010154  
 1837 016973 001665  
 (1) 016973 043020  
 1838 016975 001666  
 (1) 016975 000400  
 1839 016100 001667  
 (1) 016100 117176  
 1840 016102 001670  
 (1) 016102 000401  
 1841 016104 001671  
 (1) 016104 010177  
 1843 016106 001672  
 (1) 016106 010400  
 1844 016110 001673  
 (1) 016110 062620  
 1845 016112 001674  
 (1) 016112 010241  
 1846 016114 001675  
 (1) 016114 053220  
 1847 016116 001676  
 (1) 016116 016601  
 1848 016120 001677  
 (1) 016120 002574  
 1849 016122 001700  
 (1) 016122 010241  
 1850 016124 001701  
 (1) 016124 002642  
 1851 016126 001702  
 (1) 016126 000776  
 1852 016133 001703

BR4 FLUSH ;IF CLEAR ACTIVE SET---FLUSH  
 MICPC=MICPC+1  
 <JUMP!BR4CONI<FLUSH-INIT&3000\*4>!<FLUSH-INIT&777/2>>  
 RM1: STATE RCVA  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!MM!<RCVA-INIT&777/2>>  
 ALWAYS REXIT  
 MICPC=MICPC+1  
 <JUMP!ALCONO!<REXIT-INIT&3000\*4>!<REXIT-INIT&777/2>>  
 NTHRS: LDMA IMM,ST  
 MICPC=MICPC+1  
 <MOVE!LDMA!IMM!<ST&377>>  
 SPBR MEMX,SELB,SP0  
 MICPC=MICPC+1  
 <MOVE!SPBR!MEMX!SELB!SP0>  
 BRWRTE BR,ADD!SP0 ;SHIFT LEFT  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!BR!<ADD!SP0>>  
 BR4 OVRUN  
 MICPC=MICPC+1  
 <JUMP!BR4CONI!<OVRUN-INIT&3000\*4>!<OVRUN-INIT&777/2>>  
 BRWRTE IMM,1  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!IMM!<1>>  
 ERRX:  
 NTRS0: LDMA IMM,<<RTHRS+3>>  
 MICPC=MICPC+1  
 <MOVE!LDMA!IMM!<<RTHRS+3>&377>>  
 MEMINC IMM,0  
 MICPC=MICPC+1  
 <MOVE!WRMEM!INCMAR!IMM!<0>>  
 MEM BR,SELB  
 MICPC=MICPC+1  
 <MOVE!WRMEM!BR!<SELB>>  
 NTRS1: LDMA IMM,NXTSP  
 MICPC=MICPC+1  
 <MOVE!LDMA!IMM!<NXTSP&377>>  
 LDMA MEMX,SELB!SPX!SP0  
 MICPC=MICPC+1  
 <MOVE!LDMA!MEMX!<SELB!SPX!SP0>>  
 MEMINC IMM,201  
 MICPC=MICPC+1  
 <MOVE!WRMEM!INCMAR!IMM!<201>>  
 MEM IMM,<<RTHRS>>  
 MICPC=MICPC+1  
 <MOVE!WRMEM!IMM!<<RTHRS>>>  
 LDMA IMM,NXTSP  
 MICPC=MICPC+1  
 <MOVE!LDMA!IMM!<NXTSP&377>>  
 MEM IMM,INTSTK ;ASSUME QUEUE WRAP AROUND  
 MICPC=MICPC+1  
 <MOVE!WRMEM!IMM!<INTSTK>>  
 BRWRTE IMM,<<MMEND-2>>  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!IMM!<<MMEND-2>>>  
 CMP BR,SP0

(1) 001703  
 (1) 016130 000360  
 1853 016132 001704  
 (1) 016132 115707  
 1854 016134 001705  
 (1) 016134 000402  
 1855 016136 001706  
 (1) 016136 062400  
 1856 016140 001707  
 (1) 016140 000420  
 1857 016142 001710  
 (1) 016142 063701  
 1858 016144 001711  
 (1) 016144 110342  
 1859 016146 001712  
 (1) 016146 010171  
 1860 016150 001713  
 (1) 016150 043231  
 1861 016152 001714  
 (1) 016152 063071  
 1862 016154 001715  
 (1) 016154 000401  
 1863 016156 001716  
 (1) 016156 063310  
 1864 016160 001717  
 (1) 016160 104415  
 1865  
 1866 016162 001720  
 (1) 016162 000424  
 1867 016164 001721  
 (1) 016164 062226  
 1868 016166 001722  
 (1) 016166 000400  
 1869 016170 001723  
 (1) 016170 062227  
 1874 016172 001724  
 (1) 016172 227340  
 1871 016174 001725

MICPC=MICPC+1  
 <SUBT!BR!SP0>  
 Z NTRS2 ;IT DID WRAP AROUND  
 MICPC=MICPC+1  
 <JUMP!ZCONDI!<NTRS2-INIT&3000\*4>!<NTRS2-INIT&777/2>>  
 BRWRTE IMM,2 ;OFFSET TO NEXT PAIR  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!IMM!<2>>  
 MEM BR,ADD!SP0 ;UPDATE QUEUE POINTER  
 MICPC=MICPC+1  
 <MOVE!WRMEM!BR!<ADD!SP0>>  
 NTRS2: BRWRTE IMM,20  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!IMM!<20>>  
 SPBR BR,AORB,SP1  
 MICPC=MICPC+1  
 <MOVE!SPBR!BR!<AORB!SP1>  
 BR0 TAB1 ;FLAGGED BY ERROR TYPE  
 MICPC=MICPC+1  
 <JUMP!BR0CONI!<TAB1-INIT&3000\*4>!<TAB1-INIT&777/2>>  
 SNAK: LDMA IMM,ISP11  
 MICPC=MICPC+1  
 <MOVE!LDMA!IMM!<ISP11&377>>  
 SP MEMX,SELB,SP11  
 MICPC=MICPC+1  
 <MOVE!SPX!MEMX!SELB!SP11>  
 SP BR,INCA,SP11 ;INCREMENT MSG EXPECTED  
 MICPC=MICPC+1  
 <MOVE!SPX!BR!INCA!SP11>  
 SNAK1: BRWRTE IMM,1 ;UNNUMB PENING BIT TO BR  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!IMM!<1>>  
 SNAK2: SP BR,AORB,SP10 ;UPDATE LINE STATUS WORD  
 MICPC=MICPC+1  
 <MOVE!SPX!BR!<AORB!SP10>  
 ALWAYS FLUSH  
 MICPC=MICPC+1  
 <JUMP!ALCONO!<FLUSH-INIT&3000\*4>!<FLUSH-INIT&777/2>>  
 ;  
 EMTRIG: BRWRTE IMM,24  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!IMM!<24>>  
 OUTPUT BR,<SELB!OBA1>  
 MICPC=MICPC+1  
 <MOVE!WROUT!BR!<SELB!OBA1>>  
 BRWRTE IMM,0  
 MICPC=MICPC+1  
 <MOVE!WRTEBRI!IMM!<0>>  
 OUTPUT BR,<SELB!OBA2>  
 MICPC=MICPC+1  
 <MOVE!WROUT!BR!<SELB!OBA2>>  
 SPBR 1BUS,0M073,SP0 ;READ 0M073 ADDRESS---  
 MICPC=MICPC+1  
 <MOVE!SPBRX!1BUS!0M073!SP0>  
 OUTPUT BR,SELB!OUTDA1 ;SET UP LOW BYTE OF ADDRESS  
 MICPC=MICPC+1

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(1) 016174 062222 <MOVE!WROUT!BR!<SELB!OUTDA1>>
1072 016176 001726 BRWRITE IMM,366 ;HIGH BYTE BASE FOR ROM BOOT
(1) 001726 MICPC=MICPC+1
(1) 016176 000766 <MOVE!WRTEBR!IMM!<366>>
1073 016200 001727 OUTPUT BR,SELB!OUTDA2 ;
(1) 001727 MICPC=MICPC+1
(1) 016200 062223 <MOVE!WROUT!BR!<SELB!OUTDA2>>
1074 016202 001730 BRWRITE IMM,21 ;MASK FOR TIMER AND ALSO TO START NPR
(1) 001730 MICPC=MICPC+1
(1) 016202 000421 <MOVE!WRTEBR!IMM!<21>>
1075 016204 001731 OUT BR,<SELB!OBR>
(1) 001731 MICPC=MICPC+1
(1) 016204 061231 <MOVE!WROUT!BR!<SELB!OBR>>
1076 016206 001732 OUT BR,<SELB!ONPR>
(1) 001732 MICPC=MICPC+1
(1) 016206 061230 <MOVE!WROUT!BR!<SELB!ONPR>>
1077 016210 001733 BRWRITE IBUS,NPR ;READ NPR CONTROL
(1) 001733 MICPC=MICPC+1
(1) 016210 120600 <MOVE!WRTEBR!IBUS!<NPR>>
1078 016212 001734 BR0 CKTIME
(1) 001734 MICPC=MICPC+1
(1) 016212 102372 <JUMP!BR0CON!<CKTIME-INIT&3000*4>!<CKTIME-INIT&777/2>>
1079 016214 001735 MEMADR RM1 ;IF NPR DONE
(1) 001735 MICPC=MICPC+1
(1) 016214 002062 <MOVE!WRMEM!<RM1-INIT&777/2>>
1080 016216 001736 ALWAYS ACLOW
(1) 001736 MICPC=MICPC+1
(1) 016216 100765 <JUMP!ALCONDI<ACLOW-INIT&3000*4>!<ACLOW-INIT&777/2>>
1081 016220 001737 TABUPD: SPBR IBUS,RCVCON,SP0 ;READ RECEIVER CONTROL REG
(1) 001737 MICPC=MICPC+1
(1) 016220 023640 <MOVE!SPBR!IBUS!RCVCON!SP0>
1082 016222 001740 BRWRITE BR,ADD!SP0 ;SHIFT LEFT
(1) 001740 MICPC=MICPC+1
(1) 016222 060400 <MOVE!WRTEBR!BR!<ADD!SP0>>
1083 016224 001741 BR7 IDLE ;RECEIVE ACTIVE--IDLE
(1) 001741 MICPC=MICPC+1
(1) 016224 103445 <JUMP!BR7CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
1084 016226 001742 TAB1: LDMA IMM,IMG10
(1) 001742 MICPC=MICPC+1
(1) 016226 012156 <MOVE!LDMA!IMM!<IMG10&377>>
1085 016230 001743 BRWRITE IMM,2
(1) 001743 MICPC=MICPC+1
(1) 016230 000402 <MOVE!WRTEBR!IMM!<2>>
1086 016232 001744 MEMINC BR,AAANDB!SP10 ;SAVE BIT 1 OF SP10
(1) 001744 MICPC=MICPC+1
(1) 016232 076670 <MOVE!WRMEM!INCMAR!BR!<AAANDB!SP10>>
1087 016234 001745 MEMINC BR,SELA!SP11 ;SAVE SP11
(1) 001745 MICPC=MICPC+1
(1) 016234 076611 <MOVE!WRMEM!INCMAR!BR!<SELA!SP11>>
1088 016236 001746 MEMINC BR,SELA!SP12 ;SAVE SP12
(1) 001746 MICPC=MICPC+1
(1) 016236 076612 <MOVE!WRMEM!INCMAR!BR!<SELA!SP12>>
1089 016240 001747 MEMINC BR,SELA!SP17 ;SAVE SP17
(1) 001747 MICPC=MICPC+1
(1) 016240 076617 <MOVE!WRMEM!INCMAR!BR!<SELA!SP17>>
1090 ;

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1091 016242 001750 STATE RB2 ;NOTE: THE BRG CANNOT BE CHANGED FROM THIS
(1) 001750 MICPC=MICPC+1
(1) 016242 000461 <MOVE!WRTEBR!IMM!<RB2-INIT&777/2>>
1092 000461 ;POINT UNTIL THE BRANCH TO RB0
1093 016244 001751 CMP BR,SP3
(1) 001751 MICPC=MICPC+1
(1) 016244 060363 <SUBTC!BR!SP3>
1094 016246 001752 Z IDLE
(1) 001752 MICPC=MICPC+1
(1) 016246 101445 <JUMP!ZCONDI<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
1095 ;
1096 016250 001753 SP MEMX,SELB,SP13
(1) 001753 MICPC=MICPC+1
(1) 016250 043233 <MOVE!SPX!MEMX!SELB!SP13>
1097 016252 001754 PSTATE TBU1 ;NEW PORT STATE ADDRESS
(1) 001754 MICPC=MICPC+1
(2) 016252 002775 <MOVE!WRMEM!IMM!<TBU1-INIT&777/2>>
1098 016254 001755 SP IMM,4,SP4 ;INITIALIZE COUNT
(1) 001755 MICPC=MICPC+1
(1) 016254 000004 <MOVE!SPX!IMM!4!SP4>
1099 ;
1100 ;NOTE: FIRST 6 RAM LOCATIONS ARE NOT WRITTEN
1101 016256 001756 LDMA IMM,BASE ;TO CORE TABLE.
(1) 001756 MICPC=MICPC+1 ;MAR NOW POINTS TO BASE
(1) 016256 010017 <MOVE!LDMA!IMM!<BASE&377>>
1102 016260 001757 ALWAYS RB0 ;THE BRG MUST BE PRESET TO STATE RB2
(1) 001757 MICPC=MICPC+1
(1) 016260 104443 <JUMP!ALCONDI<RB0-INIT&3000*4>!<RB0-INIT&777/2>>
1103 016262 001760 BRWRITE IMM,2 ;INCREMENT COUNT/TEST
(1) 001760 MICPC=MICPC+1
(1) 016262 000402 <MOVE!WRTEBR!IMM!<2>>
1104 016264 001761 SP BR,ADD,SP4
(1) 001761 MICPC=MICPC+1
(1) 016264 063004 <MOVE!SPX!BR!ADD!SP4>
1105 016266 001762 SP IBUS,IOBA1,SP0 ;POINT TO NEXT ADDRESS
(1) 001762 MICPC=MICPC+1
(1) 016266 023140 <MOVE!SPX!IBUS!IOBA1!SP0>
1106 016270 001763 OUTPUT BR,ADD!IOBA1
(1) 001763 MICPC=MICPC+1
(1) 016270 062006 <MOVE!WROUT!BR!<ADD!IOBA1>>
1107 016272 001764 SP IBUS,IOBA2,SP0
(1) 001764 MICPC=MICPC+1
(1) 016272 023160 <MOVE!SPX!IBUS!IOBA2!SP0>
1108 016274 001765 OUTPUT BR,AC!IOBA2
(1) 001765 MICPC=MICPC+1
(1) 016274 062107 <MOVE!WROUT!BR!<AC!IOBA2>>
1109 016276 001766 C TABMXT
(1) 001766 MICPC=MICPC+1
(1) 016276 145373 <JUMP!CCONDI<TABMXT-INIT&3000*4>!<TABMXT-INIT&777/2>>
1110 ;
1111 016300 001767 ECX: BRWRITE BR!LDMA,SELA!SP4 ;READ COUNTER
(1) 001767 MICPC=MICPC+1
(1) 016300 070604 <MOVE!WRTEBR!BR!LDMA!<SELA!SP4>>
1112 016302 001770 BR7 206 ;ALL DONE
(1) 001770 MICPC=MICPC+1

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(1) 016302 117774 <JUMP!BR7CON!<208-INIT63000*4>1<206-INIT6777/2>>
1913 016304 001771 OUTPUT MEMX!INCMAR,SELB!OUTDA1 ;STORE COUNTS OF ERRORS
(1) 016304 001771 MICPC=MICPC+1
(1) 016304 056222 <MOVE!WROUT!MEMX!INCMAR!<SELB!OUTDA1>>
1914 016306 001772 OUTPUT MEMX!INCMAR,SELB!OUTDA2
(1) 016306 001772 MICPC=MICPC+1
(1) 016306 056223 <MOVE!WROUT!MEMX!INCMAR!<SELB!OUTDA2>>
1915 016311 001773 ALWAYS RK8
(1) 016311 001773 MICPC=MICPC+1
(1) 016311 104641 <JUMP!ALCOND!<RK8-INIT63000*4>1<RK8-INIT6777/2>>
1916
1917 016312 206: LDMA IMM,PRST
(1) 016312 001774 MICPC=MICPC+1
(1) 016312 010162 <MOVE!LDHAR!IMM!<PRST6377>>
1918 016314 MEM BR,SELA!SP13
(1) 016314 001775 MICPC=MICPC+1
(1) 016314 062613 <MOVE!WFMEM!BR!<SELA!SP13>>
1919 016316 ALWAYS RM1
(1) 016316 001776 MICPC=MICPC+1
(1) 016316 114662 <JUMP!ALCOND!<RM1-INIT63000*4>1<RM1-INIT6777/2>>
1920 016320 $ZERO
(1) 016320 001777 MICPC=MICPC+1
(1) 016320 002000 000000
1921 002001 .END
```

. ARS. 016322 000

ERRORS DETECTED: 0

,DDCMP/CRF/DS:CRF\_DMCNEW,LOW,DDCNEW  
RUN-TIME: 5 8 0 SECONDS  
RUN-TIME RATIO: 70/13=5.1  
CORE USED: 6K (11 PAGES)

1608

01400

```
1609 02800
1670 016322 02900 HIMAP: ;HIGH SPEED (LOCAL) MICRO-CODE
```

6	MACRO DEFINITIONS
8	REVISION 00
9	FEBRUARY 25, 1975
10	
11	REVISION 01
12	MARCH 18, 1975
13	NEW CSR BOARD CHANGES
14	
15	HARVEY M. SCHLESINGER
17	COPYRIGHT 1975 DIGITAL EQUIPMENT CORPORATION
69	MICRO INSTRUCTION DEFINITIONS
70	BRANCH INSTRUCTIONS
113	INDEXED BRANCH INSTRUCTIONS
149	MOVE INSTRUCTIONS
257	INPUT/OUTPUT ASSIGNMENTS
309	PROTOCOL DEPENDANT MACROS
352	DMC11 DDCMP MICRO CODE ASSEMBLED FOR USE WITH THE M0201 LINE UNIT
359	VERSION 00A FEBRUARY 26, 1975
360	
361	HARVEY M. SCHLESINGER
362	
363	COPYRIGHT 1975, DIGITAL EQUIPMENT CORPORATION
364	
365	VERSION 00B MARCH 17, 1975
366	CSR AND MICROPROCESSOR CHANGES
367	
368	
369	VERSION 00C NOVEMBER 6, 1975
370	RETRANSMISSION CHANGES
371	
372	VERSION 00D DECEMBER 3, 1975
373	TRANSMIT DONE CHANGES
374	
375	THE LATEST MODIFICATIONS WERE ADDED ON:
377	NOVEMBER 16, 1976
442	MICROPROCESSOR MAIN MEMORY ASSIGNMENTS
477	SCRATCH PAD ASSIGNMENTS
534	INIT--INITIALIZATION ROUTINE
565	IDLE--PROGRAM IDLE LOOP
602	BASSRV--- BASE SERVICE ROUTINE
643	NIDLE2---NO CSR ACTIVITY STATE
693	INWAIT---WAIT FOR ROI TO CLEAR
741	OUTINT---SET UP OUTPUT INTERRUPT (RDY0)
753	OUTWAI---WAIT FOR RDY0 TO GO AWAY
773	CTLSRV---CNTL I SERVICE
793	TBASRV---TRANSMITTER BUFFER ADDRESS SERVICE
859	RBASRV---RECEIVE BUFFER ADDRESS SERVICE
896	RCVA---ROUTINE TO HANDLE FIRST DDCMP CHARACTER
933	RCVB---ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD
954	RCVC---ROUTINE TO HANDLE SECOND CHARACTER OF COUNT FIELD, SELECT AND FINAL
975	RCVD---ROUTINE TO HANDLE RESPONSE FIELD FOR NUMBERED MESSAGES
983	RCVE---ROUTINE TO HANDLE N FIELD OF NUMBERED MESSAGE
926	RCVF---ROUTINE TO IGNORE ADDRESS
1066	RCVG---ROUTINE TO IGNORE CRC1
1079	RCVH---ROUTINE TO HANDLE CRC2 AND TO DISPATCH NUMBERED AND UNNUMBERED TYPES
1066	RCVK01---ROUTINE TO HANDLE FIRST BYTE ODD RECEIVE
1079	RCVK0---PROCESS ODD CHARACTER

1096	RCVKE--HANDLE EVEN BYTES
1146	RCVIL--STORE UNNUMBERED MESSAGE TYPE
1152	RCVJ--ROUTINE TO HANDLE SUBTYPE FIELD, SELECT AND FINAL
1166	RCVR--UNNUMBERED MESSAGE RESPONSE FIELD
1176	RCVQ--UNNUMBERED MESSAGE--NUMBER FIELD
1182	RCVL--PROCESS CRC3
1204	RCVM--PROCESS CRC4--END OF DATA MESSAGE
1226	E*2--PROCESS RLD MESSAGE
1246	NXMR--NON EXISTANT MEMORY HANDLER
1295	TMDA--TRANSMITTER DISPATCH ROUTINE
1301	TMA--FIRST CHARACTER OF HEADER
1373	TMTB--OUTPUT FIRST CHAR OF COUNT
1404	TMTC--OUTPUT SECOND CHAR OF COUNT
1424	TMD--RESPONSE FIELD--NUMBERED MESSAGE
1438	TMTF--NUMBER FIELD--NUMBERED MESSAGE
1447	TMTF--NUMBERED MSG ADDRESS FIELD
1460	TF1--NUMBERED MSG HEADER EOM
1470	TMTH--ROUTINE TO OUTPUT DATA CHARACTERS
1527	TMTI--SEND UNNUMBERED TYPE FIELD
1533	TMTJ--SEND SUB-TYPE FIELD
1538	TMTK--OUTPUT RESPONSE FIELD (UNNUMB MSG)
1546	TMTL--UNNUMB MSG NUMBER FIELD
1564	TMTM--UNNUMB MSG--STATION ADDRESS
1580	TMSRV--TIMEOUT ROUTINE--SENDS REP
1646	SNDACK--ROUTINE TO SEND AN ACK
1713	REP HANDLER
1722	START HANDLER
1735	STACK HANDLER

```
5 .TITLE DMC-11 MICROPROCESSOR INSTRUCTIONS
6 .SBTTL MACRO DEFINITIONS
7 ;
8 .SBTTL REVISION 00
9 .SBTTL FEBRUARY 25, 1975
10 .SBTTL
11 .SBTTL REVISION 01
12 .SBTTL MARCH 18, 1975
13 .SBTTL NEW CSR BOARD CHANGES
14 .SBTTL
15 .SBTTL HARVEY M. SCHLESINGER
16 ;
17 .SBTTL COPYRIGHT 1975 DIGITAL EQUIPMENT CORPORATION
18 ;
```

```
20 000000 NEW=0
21 ;MICROPROCESSOR INSTRUCTION WORD DEFINITIONS
22 000000 MOVE=0 ;OPCODE MOVE
23 100000 JUMP=100000 ;OPCODE JUMP
24 200000 IBUS=200000 ;SOURCE IBUS
25 000000 IMM=0 ;SOURCE IMMEDIATE
26 040000 MEMX=400000 ;SOURCE MEMORY
27 060000 BRX=600000 ;SOURCE BR
28 350000 BR=600000 ;SOURCE BR
29
30 060000 DP=600000 ;SOURCE BR
31 010000 LDMAR=100000 ;MA-LOAD MAR LO
32 014000 INCMAR=140000 ;MA-INCREMENT MAR
33 000400 WRTEBR=400 ;DEST-WRITE BR
34 001000 WROUTX=1000 ;DEST-EXTENDED IBUS
35 001400 SHFTBR=1400 ;DEST-SHIFT BR LEFT
36 002000 WROUT=2000 ;DEST-WRITE OUTPUT
37 002400 WRMEM=2400 ;DEST-WRITE MEMORY
38 003000 SPX=3000 ;DEST-WRITE SP
39 003400 SPBRX=3400 ;DEST-WRITE SP AND BR
40 ;FUNCTIONS
41 000200 SELA=200 ;FUNCTION-SELECT A
42 000220 SELB=220 ;FUNCTION-SELECT B
43 000240 AORNB=240 ;FUNCTION-A OR NOT B
44 000260 AANDB=260 ;FUNCTION A AND B
45 000300 AORB=300 ;FUNCTION-A OR B
46 000320 AXORB=320 ;FUNCTION A XOR B
47 000340 SUB=340 ;SUBTRACT
48 000360 SUBTC=360 ;FUNCTION- TWOS COMPLEMENT SUBTRACT
49 000000 ADD=0 ;ADD A+B
50 000020 ADDC=20 ;A+B+CARRY
51 000040 SUBC=40 ;A-B-C
52 000060 INCA=60 ;INCREMENT A
53 000100 AC=100 ;A PLUS CARRY
54 000120 AA=120 ;A PLUS A
55 000140 AAC=140 ;A PLUS A PLUS C
56 000160 DECA=160 ;DECREMENT A
57
58 004000 PAGE1=4000
59 010000 PAGE2=10000
60 014000 PAGE3=14000
61 001000 CCOND=1000 ;CONDITION C
62 001400 ZCOND=1400 ;CONDITION Z
63 000400 ALCOND=400 ;ALWAYS
64 002000 BP0CON=2000 ;CONDITION BR0
65 002400 BR1CON=2400 ;CONDITION BR1
66 003000 BR4CON=3000 ;CONDITION BR4
67 003400 BR7CON=3400 ;CONDITION BR7
```



```
309          ;SBTTL PROTOCOL DEPENDANT MACROS
316          ;
323          ;
328          ;
332          ;
336          ;
342          ;
348          ;
349          177777      MICPC=177777      ;INIT MICRO PC
350
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352          ;SBTTL DMC11 DDCMP MICRO CODE ASSEMBLED FOR USE WITH THE M8201 LINE UNIT
353          1J2000      LOW=0
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.TITLE DMC11 DDCMP PROTOCOL IMPLEMENTATION  
.SBTTL VERSION 00A FEBRUARY 26,1975  
.SBTTL  
.SBTTL HARVEY M. SCHLESINGER  
.SBTTL  
.SBTTL COPYRIGHT 1975, DIGITAL EQUIPMENT CORPORATION  
.SBTTL  
.SBTTL VERSION 00B MARCH 17,1975  
.SBTTL CSR AND MICROPROCESSOR CHANGES  
.SBTTL  
.SBTTL VERSION 00C NOVEMBER 6, 1975  
.SBTTL RETRANSMISSION CHANGES  
.SBTTL  
.SBTTL VERSION 00D DECEMBER 3,1975  
.SBTTL TRANSMIT DONE CHANGES  
.SBTTL  
.SBTTL THE LATEST MODIFICATIONS WERE ADDED ON:  
.SBTTL NOVEMBER 16, 1976

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.SBTTL MICROPROCESSOR MAIN MEMORY ASSIGNMENTS  
;ALLOCATION OF MICROPROCESSOR MAIN MEMORY  
NAKSR=0 ;NAKS RECD--DYNAMIC  
NAKST=NAKSR+1 ;NAKS TMED--DYNAMIC  
REPSR=NAKST+1 ;REPS RECD--DYNAMIC  
REPST=REPSR+1 ;REPS TMED--DYNAMIC  
NP=REPST+3 ;CONSTANT 0  
NTR=NP+1 ;NAKS-MSG NO BUFFERS CUMUL.  
NHDR=NTR+1 ;NAKS-MSG HEADER BAD  
NDATR=NHDR+1 ;NAKS-DATA BAD  
NTLS=NDATR+1 ;NAK SENT --NO BUFFERS  
NHDS=NTLS+1 ;NAK SENT BAD HEADER  
NDATS=NHDS+1 ;NAK SENT BAD DATA  
REPCS=NDATS+1 ;REPS SENT CUMUL  
REPCR=REPCS+1 ;REPS RECD CUMUL  
BASE=REPCR+1 ;CORE TABLE BASE ADDRESS  
SRC=BASE+3 ;START OF INPUT CHAIN--NEXT RECV DONE  
ERC=SRC+1 ;END OF INPUT CHAIN  
RCL1=ERC+1 ;RECEIVE LINK #1  
RCL2=RCL1+5 ; " " #2  
RCL3=RCL2+5 ; " " #3  
RCL4=RCL3+5  
RCL5=RCL4+5  
RCL6=RCL5+5  
RCL7=RCL6+5  
STC=RCL7+5 ;START OF OUTPUT CHAIN--NEXT TMT DONE  
ETC=STC+1 ;END OF TRANSMIT CHAIN  
TML1=ETC+1 ;TRANSMIT LINK #1  
TML2=TML1+6 ; " " #2  
TML3=TML2+6 ; " " #3  
TML4=TML3+6  
TML5=TML4+6  
TML6=TML5+6  
TML7=TML6+6  
TML8=TML7+6  
T=TML8+6 ;TYPE FIELD  
ST=T+1 ;SUBTYPE FIELD  
ISP17=ST+1 ;MSG ACKED IMAGE  
IMG10=ISP17+1 ;IMAGE OF BIT 1 OF SP10  
IMG11=IMG10+1 ;IMAGE OF SP11  
IMG12=IMG11+1 ;IMAGE OF SP12  
IMG14=IMG12+1 ;IMAGE OF SP14  
IMG16=IMG14+1 ;IMAGE OF SP16  
IMG17=IMG16+1 ;IMAGE OF SP17  
TYPTAB=IMG17+1 ;TYPE TABLE--  
;72 TYPE TABLE REP  
;73 " " NAK  
TYPST=TYPTAB+2 ;74 " " START  
;75 " " STACK  
;  
;  
BC=TYPS17+3 ;RECEIVE BYTE COUNT  
ISP11=BC+2 ;SP11 IMAGE  
ISP12=ISP11+1 ;SP12 IMAGE  
INCONS=ISP12+1 ;IN CONTROL CSR IMAGE  
MTHRS=INCONS+1 ;RECV THRESHOLD LINK



```
433 ;ALL LOCATIONS FROM 200 ON ARE NOT WRITTEN OUT DURING A TABLE UPDATE
434
435 TABST=210 ;TABLE UPDATE STATE
436 PRTST=TABST+1 ;PORT STATE
437 NXTINT=240 ;NEXT INTERRUPT POSITION
438 NXTSP=NXTINT+1 ;END OF INTERRUPT CHAIN
439 INTSTK=NXTSP+1 ;STACK OF INTERRUPTS
440 MMEND=400 ;MAIN MEMORY END
```

```
442 .SBTTL SCRATCH PAD ASSIGNMENTS
443 SP0=0 ;SP0---SCRATCH REGISTER
444 SP1=1 ;SP1---PORT STATUS WORD
445 ;BIT ASSIGNMENTS
446 ;BIT0---INIT MODE
447 ;BIT1---SEC STATION SELECT(UNUSED)
448 ;BIT2---NO BUFFER ASSIGNED IN BOOT MODE
449 ;BIT3---DLE RECEIVED WHILE NOT IN MAINT MODE
450 ;BIT4---INTERRUPT PENDING
451 ;BIT6---DISCONNECT ERROR
452 ;BIT7---BOOT MODE
453 SP2=2 ;SP2---TRANSMIT STATE POINTER
454 SP3=3 ;SP3---RECEIVE STATE POINTER
455 SP4=4 ;SP4---END RECV ADDRESS
456 SP5=5 ;SP5---END RECEIVE ADDRESS
457 SP6=6 ;SP6---END TRANSMIT ADDRESS
458 SP7=7 ;SP7---END TRANSMIT ADDRESS
459 SP10=10 ;SP10---LINE STATUS WORD
460 ;BIT ASSIGNMENTS
461 ;BIT0---UNNUMB PENDING
462 ;BIT1---MESSAGE IN PROGRESS
463 ;BIT2---LINE HAS GONE IDLE
464 ;BIT3---START RECEIVED
465 ;BIT4---CLEAR ACTIVE ON END
466 ;BIT5---START MODE
467 ;BIT6---HALF DUPLEX
468 ;BIT7---OK TO SEND
469 SP11=11 ;SP11---R FIELD
470 SP12=12 ;SP12---M FIELD
471 SP13=13 ;SP13---TYPE
472 SP14=14 ;SP14---RECEIVE LINK IMAGE
473 SP15=15 ;SP15---TIMER ENTRY---NUMBER OF ONE SECOND TICKS
474 SP16=16 ;SP16---POINTER TO TMT LINK COPY IN MAIN MEM
475 SP17=17 ;SP17---LAST MESSAGE ACKNOWLEDGED
```

```

477 .SBTTL INIT--INITIALIZATION ROUTINE
478 ;ZEROS MAIN MEMORY
479 ;LOOPS WAITING FOR RECEIVE DATA(BOOT?)
480 ;OK FOR ROI TO BE SET
481 ;WILL ACCEPT ONLY BASE FORMAT. ALL OTHERS WILL RETURN A PROCEDURE ERROR
482 ;
483 ;AT INITIALIZATION --- THE HARDWARE CLEARS THE BR AND MAR
484 .=16322
485 #16322 016322
(1) 000000
(1) #16322 063220
486 #16324
(1) 000001
(1) #16324 063223
487 #16326
(1) 000002
(1) #16326 063237
488 #16330
(1) 000003
(1) #16330 061200
489 #16332
(1) 000004
(1) #16332 061202
490 #16334
(1) 000005
(1) #16334 003370
491
492 #16336
(1) 000006
(1) #16336 063130
493
494 #16340
(1) 000007
(1) #16340 076423
495
496 #16342
(1) 000010
(1) #16342 063060
497 #16344
(1) 000011
(1) #16344 101413
498 #16346
(1) 000012
(1) #16346 100400
499 #16350
(1) 000013
(1) #16350 003401
500 #16352
(1) 000014
(1) #16352 063231
501 #16354
(1) 000015
(1) #16354 063232
502 #16356
(1) 000016
(1) #16356 010162

```

```

INIT: SP BR,SELB,SP0 ;CLEAR SP0
MICPC=MICPC+1
<MOVE:SPX:BR:SELB:SP0>
SP BR,SELB,SP3 ;PAGE ONE TRANSFER ADDRESS
MICPC=MICPC+1
<MOVE:SPX:BR:SELB:SP3>
SP BR,SELB,SP17 ;CLEAR SP17
MICPC=MICPC+1
<MOVE:SPX:BR:SELB:SP17>
OUT BR,<SEL:IOINCON> ;ZERO THE IN CONTROL CSR
MICPC=MICPC+1
<MOVE:WROUT:BR:<SEL:IOINCON>>
OUT BR,<SEL:IOOCON> ;ZERO THE OUT CONTROL CSR
MICPC=MICPC+1
<MOVE:WROUT:BR:<SEL:IOOCON>>
SP IMM,370,SP10 ;WRITE 5 ONE BITS TO THE HIGH ORDER
MICPC=MICPC+1
<MOVE:SPX:IMM:370:SP10>
;BITS OF SP10
55: SP BR,AA,SP10 ;SHIFT SP10 LEFT SETTING CARRY THE
MICPC=MICPC+1
<MOVE:SPX:BR:AA:SP10>
;FIRST 5 TIMES THRU THE LOOP
;WRITE A ONE TO THE FIRST 5 MEMORY
MEMINC BR,ADDC:SP3
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:BR:ADDC:SP3>
;LOCATIONS AND ZERO THE REST
;INCREMENT COUNTER
SP BR,INCA,SP0
MICPC=MICPC+1
<MOVE:SPX:BR:INCA:SP0>
Z 106 ;ALL DONE
MICPC=MICPC+1
<JUMP:ZCOND:<106-INIT:3000*4>:<106-INIT:777/2>>
ALWAYS 55 ;KEEP GOING
MICPC=MICPC+1
<JUMP:ALCOND:<56-INIT:3000*4>:<56-INIT:777/2>>
106: SPBR IMM,1,SP1 ;WRITE A 1 TO THE BR AND SP1
MICPC=MICPC+1
<MOVE:SPBRX:IMM:1:SP1>
SP BR,SELB,SP11 ;WRITE A 1 TO SP11
MICPC=MICPC+1
<MOVE:SPX:BR:SELB:SP11>
SP BR,SELB,SP12 ;WRITE A 1 TO SP12
MICPC=MICPC+1
<MOVE:SPX:BR:SELB:SP12>
LDMA IMM,TYP TAB ;POINT MAR TO TYPE TABLE
MICPC=MICPC+1
<MOVE:LDMA:IMM:<TYP TAB:377>>

```

```

503 #16360
(1) 000017
(1) #16360 000626
504 #16362
(1) 000020
(1) #16362 062234
505 #16364
(1) 000021
(1) #16364 016403
506 #16366
(1) 000022
(1) #16366 002402
507 #16370
(1) 000023
(1) #16370 057235
508 #16372
(1) 000024
(1) #16372 016406
509 #16374
(1) 000025
(1) #16374 016407
510 #16376
(1) 000026
(1) #16376 016401
511 #16400
(1) 000027
(1) #16400 010210
512 #16402
(1) 000030
(2) #16402 016460
513 #16404
(1) 000031
(2) #16404 016533
514 #16406
(1) 000032
(1) #16406 010057
515 #16410
(1) 000033
(1) #16410 016471
516 #16412
(1) 000034
(1) #16412 002471
517 #16414
(1) 000035
(1) #16414 043236
518 #16416
(1) 000036
(1) #16416 010022
519 #16420
(1) 000037
(1) #16420 016424
520 #16422
(1) 000040
(1) #16422 002424

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BRWRT IMM,226 ;WRITE SYNC TO MEMORY
MICPC=MICPC+1
<MOVE:WRTE:BR:IMM:<226>>
OUTPUT BR,SELB:SYNC ;LOAD THE SYNC REGISTER
MICPC=MICPC+1
<MOVE:WROUT:BR:<SELB:SYNC>>
MEMINC IMM,3 ;REP
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM:<3>>
MEM IMM,2 ;NAK
MICPC=MICPC+1
<MOVE:WRMEM:IMM:<2>>
SP MEMX:INCMAR,SELB,SP15 ;SET STARTING COUNT
MICPC=MICPC+1
<MOVE:SPX:MEMX:INCMAR:SELB:SP15>
MEMINC IMM,6 ;START
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM:<6>>
MEMINC IMM,7 ;STACK
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM:<7>>
MEMINC IMM,1 ;ACK
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM:<1>>
LDMA IMM,TABST ;POINT TO TABLE UPDATE STATE
MICPC=MICPC+1
<MOVE:LDMA:IMM:<TABST:377>>
PSTATI I3 ;INITIALIZE IT
MEMINC IMM,<<I3-INIT:777/2>>
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM:<<I3-INIT:777/2>>>
PSTATI NIDLE2 ;INITIALIZE PORT STATUS
MEMINC IMM,<<NIDLE2-INIT:777/2>>
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM:<<NIDLE2-INIT:777/2>>>
LDMA IMM,STC ;LOAD ADDRESS OF LAST TMT CHAIN
MICPC=MICPC+1
<MOVE:LDMA:IMM:<STC:377>>
MEMINC IMM,TML1 ;STORE ADDRESS OF FIRST TMT LINK
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM:<TML1>>
MEM IMM,TML1
MICPC=MICPC+1
<MOVE:WRMEM:IMM:<TML1>>
SP MEMX,SELB,SP16 ;INITIALIZE LAST XMIT POINTER
MICPC=MICPC+1
<MOVE:SPX:MEMX:SELB:SP16>
LDMA IMM,SRC ;LOAD ADDRESS OF LAST RECV CHAIN
MICPC=MICPC+1
<MOVE:LDMA:IMM:<SRC:377>>
MEMINC IMM,RCL1 ;SET UP ADDRESS OF FIRST RECV LINK
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM:<RCL1>>
MEM IMM,RCL1
MICPC=MICPC+1
<MOVE:WRMEM:IMM:<RCL1>>

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521 010424 SP MEMX,SELB,SP14
(1) 000041 MICPC=NICPC+1
(1) 016424 043234 <MOVE!SP!MEMX!SELB!SP14>
522 010426 LDMA IMM,INTINT ;ADDRESS OF NEXT INTERRUPT POINTER TO MAR
(1) 000042 MICPC=NICPC+1
(1) 016426 010240 <MOVE!LDMA!IMM!<NXTINT&377>>
523 016430 MEMINC IMM,INTSTK ;INITIALIZE NEXT INTERRUPT POINTER
(1) 000043 MICPC=NICPC+1
(1) 016430 016642 <MOVE!WRMEM!INCMAR!IMM!<INTSTK>>
524 016432 MEM IMM,INTSTK ;INITIALIZE INSERTION POINTER
(1) 000044 MICPC=NICPC+1
(1) 016432 002642 <MOVE!WRMEM!IMM!<INTSTK>>
525 016434 BRWRT IMM,200 ;WRITE THE RUN BIT TO THE BR
(1) 000045 MICPC=NICPC+1
(1) 016434 000600 <MOVE!WRTEBR!IMM!<200>>
526 016436 OUT BR,<SELB!OMAIN> ;WRITE THE RUN BIT TO MAINT CSR
(1) 000046 MICPC=NICPC+1
(1) 016436 061221 <MOVE!ROUTX!BR!<SELB!OMAIN>>
527 ;FALL INTO IDLE LOOP
529 016440 ALWAYS TEOM2
(1) 000047 MICPC=NICPC+1
(1) 016440 110740 <JUMPIALCONDI<TEOM2-INIT&3000+4>!<TEOM2-INIT&777/2>>
530
531 016442 REXIT: SP BR,SELB,SP3
(1) 000050 MICPC=NICPC+1
(1) 016442 063223 <MOVE!SPX!BR!SELB!SP3>

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534 ;SBTTL IDLE--PROGRAM IDLE LOOP
535 ;PROGRAM IDLE LOOP
536 ;DISPATCHES TO APPROPRIATE SERVICE ROUTINES
537 ;USES STATE POINTERS FOR TMT,RCV,CSR ACTIVITY
538
539 016444 IDLE: BRWRT BR,<SELA!SP10> ;READ TRANSMIT STATUS WORD FROM SP10 TO BR
(1) 000051 MICPC=NICPC+1
(1) 016444 060610 <MOVE!WRTEBR!BR!<SELA!SP10>>
540 BR1 TMTDA ;IF DATA TO SEND-- BRANCH
(1) 000052 MICPC=NICPC+1
(1) 016446 112400 <JUMPIBRCONI<TMTDA-INIT&3000+4>!<TMTDA-INIT&777/2>>
541 016450 BR0 TMTDA ;IF DATA TO SEND-- BRANCH
(1) 000053 MICPC=NICPC+1
(1) 016450 112000 <JUMPIBRCONI<TMTDA-INIT&3000+4>!<TMTDA-INIT&777/2>>
547 016452 I1: BRWRT IBUS,RCVCON ;READ LINE UNIT RECEIVE CONTROL WORD
(1) 000054 MICPC=NICPC+1
(1) 016452 020640 <MOVE!WRTEBR!IBUS!<RCVCON>>
548 016454 ,BR4 BR,SELA,SP3!PAGE1 ;BRANCH BASED UPON RCV STATE
(1) 000055 MICPC=NICPC+1
(1) 016454 167203 <JUMPIBRACONIBR!SELA!SP3!PAGE1>
549 016456 I2: LDMA IMM,TABST ;POINT TO TABLE UPDATE STATE
(1) 000056 MICPC=NICPC+1
(1) 016456 010210 <MOVE!LDMA!IMM!<TABST&377>>
550 010460 ,ALWAY MEMX,SELB,0
(1) 000057 MICPC=NICPC+1
(1) 016460 140620 <JUMPIALCONDI<MEMX!SELB!0>
551 016462 I3: STATE TMTA+2 ;GET IDLE TRANSMIT STATE + 1
(1) 000060 MICPC=NICPC+1
(1) 016462 000404 <MOVE!WRTEBR!IMM!<TMTA+2-INIT&777/2>>
554 016464 NOP BR,SUB,SP2 ;SUBTRACT FROM CURRENT STATE
(1) 000061 MICPC=NICPC+1
(1) 016464 060342 <BRISUB!SP2>
555 016466 C TMTDA ;NON-IDLE STATE
(1) 000062 MICPC=NICPC+1
(1) 016466 111000 <JUMPICONDI<TMTDA-INIT&3000+4>!<TMTDA-INIT&777/2>>
557 016470 IDLE0: SPBR IBUS,UBBR,SP0 ;TIMER EXPIRES?
(1) 000063 MICPC=NICPC+1
(1) 016470 123620 <MOVE!SPBR!IBUS!UBBR!SP0>
558 010472 BR4 TIMSRV
(1) 000064 MICPC=NICPC+1
(1) 016472 113255 <JUMPIBRACONI<TIMSRV-INIT&3000+4>!<TIMSRV-INIT&777/2>>
559 010474 SP IBUS,RCVCON,SP0 ;READ THE RECEIVE CONTROL REGISTER
(1) 000065 MICPC=NICPC+1
(1) 016474 023240 <MOVE!SPX!IBUS!RCVCON!SP0>
560 016476 BRWRT BR,AA!SP0 ;SHIFT IT LEFT
(1) 000066 MICPC=NICPC+1
(1) 016476 060520 <MOVE!WRTEBR!BR!<AA!SP0>>
561 010500 BR7 I1 ;RECEIVE ACTIVE, DON'T DO PORT STATUS
(1) 000067 MICPC=NICPC+1
(1) 016500 103454 <JUMPIBR7CONI<I1-INIT&3000+4>!<I1-INIT&777/2>>
562 010502 LDMA IMM,PRST ;ADDRESS PORT STATE
(1) 000070 MICPC=NICPC+1
(1) 016502 010211 <MOVE!LDMA!IMM!<PRST&377>>
563 010504 ,ALWAY MEMX,SELB,0 ;INDEX
(1) 000071 MICPC=NICPC+1

```

(1) 016504 140620

<JUMP:ALCOND:MEMX:SELB10>

565  
 566 016500  
 (1) 016506  
 (2) 000072  
 (2) 016506 002533  
 567 016510  
 (1) 000073  
 (1) 016510 010017  
 568 016512  
 (1) 000074  
 (1) 016512 136500  
 569 016514  
 (1) 000075  
 (1) 016514 136520  
 570 016516  
 (1) 000076  
 (1) 016516 122560  
 571 016520  
 (1) 000077  
 (1) 016520 123000  
 572 016522  
 (1) 000100  
 (1) 016522 000500  
 573 016524  
 (1) 000101  
 (1) 016524 061260  
 574 016526  
 (1) 000102  
 (1) 016526 002133  
 575 016530  
 (1) 000103  
 (1) 016530 040620  
 576 016532  
 (1) 000104  
 (1) 016532 103113  
 577 016534  
 (1) 000105  
 (1) 016534 010151  
 578 016536  
 (1) 000106  
 (1) 016536 016406  
 579 016540  
 (1) 000107  
 (1) 016540 002700  
 580 016542  
 (1) 000110  
 (1) 016542 003161  
 581 016544  
 (1) 000111  
 (1) 016544 000641  
 582 016546  
 (1) 000112  
 (1) 016546 110737  
 583 016550  
 (1) 000113  
 (1) 016550 003204

```

.SBTTL BASSRV---- BASE SERVICE ROUTINE
BASSRV: PSTATE NIDLE2
MEM IMM,<<NIDLE2-INIT&777/2>>
MICPC=MICPC+1
<MOVE:WRMEM:IMM1<<NIDLE2-INIT&777/2>>>
LDMA IMM,BASE ;CLEAR TO MAR SO IT POINTS TO BASE POINT
MICPC=MICPC+1
<MOVE:LDMAR:IMM1<BASE&377>>
MEMINC IBUS,PORT1 ;READ CSR4
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IBUS1<PORT1>>
MEMINC IBUS,PORT2 ;READ CSR5
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IBUS1<PORT2>>
MEM IBUS,PORT4
MICPC=MICPC+1
<MOVE:WRMEM:IBUS1<PORT4>>
SP IBUS,INCON,SP0 ;READ INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE:SPX:IBUS:INCON:SP0>
BRWRT IMM,100 ;CLEAR THE BR
MICPC=MICPC+1
<MOVE:WRTBR:IMM1<100>>
OUT BR,<<AANDB:IOINCON>> ;CLEAR THE INCONTROL CSR
MICPC=MICPC+1
<MOVE:WROUTX:BR1<AANDB:IOINCON>>
OUTPUT IMM,<<120:OMODEM>> ;MASK FOR HDX AND DTR
MICPC=MICPC+1
<MOVE:WROUT:IMM1<120:OMODEM>>
BRWRT MEMX,SELB ;READ SEL6
MICPC=MICPC+1
<MOVE:WRTBR:MEMX1<SEL6>>
BR4 RESUME ;IF SET RESUME
MICPC=MICPC+1
<JUMP:BR4CON1<RESUME-INIT&3000*4>1<RESUME-INIT&777/2>>
LDMA IMM,T ;LOAD ADDRESS OF TYPE FIELD
MICPC=MICPC+1
<MOVE:LDMAR:IMM1<T&377>>
MEMINC IMM,6 ;WRITE START TYPE TO MEMORY
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM1<6>>
MEM IMM,300 ;WRITE SELECT AND FINAL TO MEMORY
MICPC=MICPC+1
<MOVE:WRMEM:IMM1<300>>
SP BR,DECA,SP1 ;TURN OFF INIT MODE
MICPC=MICPC+1
<MOVE:SPX:BR:DECA:SP1>
BRWRT IMM,241 ;SET OK TO SEND,STARTMODE AND UNNUM PENDING
MICPC=MICPC+1
<MOVE:WRTBR:IMM1<241>>
ALWAYS SA3
MICPC=MICPC+1
<JUMP:ALCOND1<SA3-INIT&3000*4>1<SA3-INIT&777/2>>
RESUME: SP IMM,SP4,4 ;SET UP SP4 FOR COUNTING NPRS
MICPC=MICPC+1
<MOVE:SPX:IMM1:SP4:4>

```

```

584 016552          SP      BR,INCA,SP10          ;SET UNNUMB MESSAGE PENDING TO
(1) 016552 000114 MICPC=MICPC+1
(1) 016552 003070 <MOVE:SPXIBR:INCA:SP10>
585                                     ;TRICK TRANSMITTER CODE
586 016554          LDMA   IMM,BASE          ;ADDRESS BASE TABLE ADDRESS
(1) 016554 000115 MICPC=MICPC+1
(1) 016554 010017 <MOVE:LDMAR:IMM:BASE6377>
587 016556          STATE  FUDGE          ;SET TMTR STATE TO ENTER TABLE UPDATE
(1) 016556 000116 MICPC=MICPC+1
(1) 016556 000743 <MOVE:WRTEBR:IMM:FDGE=INIT&777/2>
588 016560          ALWAYS  T80          ;GO SET UP MXT BITS AND ADDRESS OF BASE FOR NPRS
(1) 016560 000117 MICPC=MICPC+1
(1) 016560 112455 <JUMP:ALCONDI:T80=INIT&3000*4:1:T80=INIT&777/2>
BS2: 589 016562          LDMA   IMM,IMG10
(1) 016562 000120 MICPC=MICPC+1
(1) 016562 010154 <MOVE:LDMAR:IMM:IMG10&377>
590 016564          SP      MEMX:INCMAR,AORB,SP10      ;RESTORE BIT 1 OF SP10
(1) 016564 000121 MICPC=MICPC+1
(1) 016564 057310 <MOVE:SPX:MEMX:INCMAR:AORB:SP10>
591 016566          SP      MEMX:INCMAR,SELB,SP11      ;RESTORE SP11
(1) 016566 000122 MICPC=MICPC+1
(1) 016566 057231 <MOVE:SPX:MEMX:INCMAR:SELB:SP11>
592 016570          SP      MEMX:INCMAR,SELB,SP12      ;RESTORE SP12
(1) 016570 000123 MICPC=MICPC+1
(1) 016570 057232 <MOVE:SPX:MEMX:INCMAR:SELB:SP12>
593 016572          SP      MEMX:INCMAR,SELB,SP14      ;RESTORE SP14
(1) 016572 000124 MICPC=MICPC+1
(1) 016572 057234 <MOVE:SPX:MEMX:INCMAR:SELB:SP14>
594 016574          SP      MEMX:INCMAR,SELB,SP16      ;RESTORE SP16
(1) 016574 000125 MICPC=MICPC+1
(1) 016574 057236 <MOVE:SPX:MEMX:INCMAR:SELB:SP16>
595 016576          SP      MEMX,SELB,SP17          ;RESTORE SP17
(1) 016576 000126 MICPC=MICPC+1
(1) 016576 043237 <MOVE:SPX:MEMX:SELB:SP17>
596 016600          SP      BR,DECA,SP10          ;TURN OFF UNNUM MESSAGE PENDING AND
(1) 016600 000127 MICPC=MICPC+1
(1) 016600 003170 <MOVE:SPXIBR:DECA:SP10>
597                                     ;ZERO THE BRG
598 016602          SP      BR,DECA,SP1          ;CLEAR INIT MODE
(1) 016602 000130 MICPC=MICPC+1
(1) 016602 003161 <MOVE:SPXIBR:DECA:SP1>
599 016604          BRWRTE IMM,200          ;SET OK TO SEND
(1) 016604 000131 MICPC=MICPC+1
(1) 016604 000600 <MOVE:WRTEBR:IMM:200>
600 016606          ALWAYS  SA3
(1) 016606 000132 MICPC=MICPC+1
(1) 016606 110737 <JUMP:ALCONDI:SA3=INIT&3000*4:1:SA3=INIT&777/2>

```

```

602          .SBTTL  NIDLE2---NO CSR ACTIVITY STATE
603 016610          NIDLE2: BRWRTE BR,SELA:SP1          ;READ PORT STATUS WORD
(1) 016610 000133 MICPC=MICPC+1
(1) 016610 000601 <MOVE:WRTEBR:BR:SELA:SP1>
605 016612          BR4   NIDLE5          ;INTERRUPT PENDING?---BRANCH
(1) 016612 000134 MICPC=MICPC+1
(1) 016612 103141 <JUMP:BR4CONI:NIDLE5=INIT&3000*4:1:NIDLE5=INIT&777/2>
610 016614          SPBR  IBUS,INCON,SP0          ;READ INPUT CONTROL CSR
(1) 016614 000135 MICPC=MICPC+1
(1) 016614 123400 <MOVE:SPBRX:IBUS:INCON:SP0>
611 016616          BRSHFT          ;SHIFT IT RIGHT
(1) 016616 000136 MICPC=MICPC+1
(1) 016616 001620 <MOVE:SHFTBR:WRTEBR:SELB>
612 016620          BR4   INWAT1          ;IF RQI SET -- BRANCH
(1) 016620 000137 MICPC=MICPC+1
(1) 016620 103146 <JUMP:BR4CONI:INWAT1=INIT&3000*4:1:INWAT1=INIT&777/2>
613                                     ;TO RE-READ THE IN CNTRL REGISTER TO AVOID
614                                     ;A RACE IN MICRO-P READ/UNIBUS WRITE
616 016622          ALWAYS  IDLE
(1) 016622 000140 MICPC=MICPC+1
(1) 016622 100451 <JUMP:ALCONDI:IDLE=INIT&3000*4:1:IDLE=INIT&777/2>
618 016624          NIDLE6:
639 016624          NIDLE5: PSTATE  OUTINT          ;SET STATE FOR INTERRUPT PROCESSING
(1) 016624          MEM   IMM,<<OUTINT=INIT&777/2>>
(2) 016624 000141 MICPC=MICPC+1
(2) 016624 002614 <MOVE:WRMEM:IMM:<<OUTINT=INIT&777/2>>
640 016626          ALWAYS  IDLE
(1) 016626 000142 MICPC=MICPC+1
(1) 016626 100451 <JUMP:ALCONDI:IDLE=INIT&3000*4:1:IDLE=INIT&777/2>

```

643 016633  
644 016633 000143  
(1) 016630 123400  
645 016632  
(1) 000144  
(1) 016632 060520  
646 016631  
(1) 000145  
(1) 016634 103550  
647  
648 016636  
(1) 000146  
(1) 016636 123400  
649 016640  
(1) 000147  
(1) 016640 103557  
650 016642  
(1) 016642  
(2) 000150  
(2) 016642 002546  
651 016644  
(1) 000151  
(1) 016644 060520  
652 016646  
(1) 000152  
(1) 016646 117460  
653 016650  
(1) 016650  
(2) 000153  
(2) 016650 002543  
654 016652  
(1) 000154  
(1) 016652 060600  
655 016654  
(1) 000155  
(1) 016654 061300  
656 016656  
(1) 000156  
(1) 016656 100451  
657  
658 016660  
(1) 000157  
(1) 016660 001620  
663 016662  
(1) 000160  
(1) 016662 103051  
664 016664  
(1) 016664  
(2) 000161  
(2) 016664 002563  
665 016666  
(1) 000162  
(1) 016666 100451  
667 016670  
(1) 000163

```
.SBTTL INWAIT---WAIT FOR ROI TO CLEAR
INWAIT: SPBR IBUS,INCON,SP0 ;READ INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!INCON!SP0>
BRWRT BR,<AA!SP0> ;SHIFT IT LEFT
MICPC=MICPC+1
<MOVE!WRTEBR!BRI<AA!SP0>>
BR7 NIDLE3 ;INTERRUPT ENABLE HAS BEEN SET
MICPC=MICPC+1
<JUMP!BR7CON!<NIDLE3-INIT63000*4>!<NIDLE3-INIT6777/2>>

INWAIT1: SPBR IBUS,INCON,SP0 ;READ THE INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!INCON!SP0>
BR7 INWAIT2 ;READY IN STILL SET
MICPC=MICPC+1
<JUMP!BR7CON!<INWAIT2-INIT63000*4>!<INWAIT2-INIT6777/2>>
NIDLE3: PSTATE INWAIT ;UPDATE STATE TO INPUT
MEM IMM,<<INWAIT1-INIT6777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<INWAIT1-INIT6777/2>>>
BRWRT BR,AA!SP0 ;SHIFT CSR LEFT
MICPC=MICPC+1
<MOVE!WRTEBR!BRI<AA!SP0>>
BR7 ININT
MICPC=MICPC+4
<JUMP!BR7CON!<ININT-INIT63000*4>!<ININT-INIT6777/2>>
PSTATE INWAIT ;UPDATE STATE POINTER TO NO INTERRUPT GENERATED
MEM IMM,<<INWAIT-INIT6777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<INWAIT-INIT6777/2>>>
NIDLE4: BRWRT IMM,200
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<200>>
OUT BR,AORB!OINCON ;SET THE RDYI
MICPC=MICPC+1
<MOVE!WROUT!BRI<AORB!OINCON>>
ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>

INWAIT2: BRSHFT ;SHIFT THE BR RIGHT
MICPC=MICPC+1
<MOVE!SHFT!BRI!WRTEBR!SELB>
BR4 IDLE
MICPC=MICPC+1
<JUMP!BR4CON!<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>
PSTATE INSRV ;SET NEXT STATE TO INPUT SERVICE
MEM IMM,<<INSRV-INIT6777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<INSRV-INIT6777/2>>>
ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>
INSRV: SPBR IBUS,INCON,SP0 ;READ THE INPUT CONTROL CSR
MICPC=MICPC+1
```

(1) 016670 123400  
668 016672  
(1) 000164  
(1) 016672 102000  
669 016674  
(1) 000165  
(1) 016674 132172  
670 016676  
(1) 000166  
(1) 016676 001620  
671 016700  
(1) 000167  
(1) 016700 102574  
672 016702  
(1) 016702  
(2) 000170  
(2) 016702 002700  
673 016704  
(1) 000171  
(1) 016704 100575  
674 016706  
(1) 016706  
(2) 000172  
(2) 016706 002057  
675 016710  
(1) 000173  
(1) 016710 100575  
676 016712  
(1) 016712  
(2) 000174  
(2) 016712 002721  
677 016714  
(1) 000175  
(1) 016714 060601  
678 016716  
(1) 000176  
(1) 016716 102201  
679 016720  
(1) 000177  
(1) 016720 100451  
680 016722  
(1) 000200  
(1) 016722 102211  
681 016724  
(1) 016724  
(2) 000201  
(2) 016724 002533  
682 016726  
(1) 000202  
(1) 016726 000530  
683 016730  
(1) 000203  
(1) 016730 061260  
694 016732  
(1) 000204  
(1) 016732 010177

```
<MOVE!SPBRX!IBUS!INCON!SP0>
BR1 300 ;--SENSE OR BASE
MICPC=MICPC+1
<JUMP!BRI!CON!<300-INIT63000*4>!<300-INIT6777/2>>
BR0 100 ;CNTL I
MICPC=MICPC+1
<JUMP!BR0CON!<100-INIT63000*4>!<100-INIT6777/2>>
BRSHFT ;MUST BE BA/CC-SHIFT FOR IN OR OUT
MICPC=MICPC+1
<MOVE!SHFT!BRI!WRTEBR!SELB>
BR1 150
MICPC=MICPC+1
<JUMP!BRI!CON!<150-INIT63000*4>!<150-INIT6777/2>>
PSTATE TBASRV ;TRANSMITTER
MEM IMM,<<TBASRV-INIT6777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<TBASRV-INIT6777/2>>>
ALWAYS 200
MICPC=MICPC+1
<JUMP!ALCOND!<200-INIT63000*4>!<200-INIT6777/2>>
100: PSTATE CTLSRV
MEM IMM,<<CTLSRV-INIT6777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<CTLSRV-INIT6777/2>>>
ALWAYS 200
MICPC=MICPC+1
<JUMP!ALCOND!<200-INIT63000*4>!<200-INIT6777/2>>
150: PSTATE RBASRV
MEM IMM,<<RBASRV-INIT6777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<RBASRV-INIT6777/2>>>
200: BRWRT BR,SELA!SP1 ;INIT MODE
MICPC=MICPC+1
<MOVE!WRTEBR!BRI<SELA!SP1>>
BR0 PROCER ;IF INIT MODE--ERROR
MICPC=MICPC+1
<JUMP!BR0CON!<PROCER-INIT63000*4>!<PROCER-INIT6777/2>>
ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>
300: BR0 INSRV1 ;IF BASE---PROCESS
MICPC=MICPC+1
<JUMP!BR0CON!<INSRV1-INIT63000*4>!<INSRV1-INIT6777/2>>
PPOCER: PSTATE NIDLE2 ;RESET PORT STATUS
MEM IMM,<<NIDLE2-INIT6777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<NIDLE2-INIT6777/2>>>
BRWRT IMM,100 ;CLEAR INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<100>>
OUT BR,ANARB!OINCON ;
MICPC=MICPC+1
<MOVE!WROUT!BRI<ANARB!OINCON>>
LONA IMM,<<+THRS+3>> ;ADDRESS ERROR LINK
MICPC=MICPC+1
<MOVE!LONAR!IMM!<<+THRS+3>>+377>>
```

685 016734  
(1) 000205  
(1) 016734 016402  
686 016735  
(1) 000206  
(1) 016736 002400  
687 016740  
(1) 000207  
(1) 016740 042233  
689 016742  
(1) 000210  
(1) 016742 114524  
689 016744  
(1) 000211  
(1) 016744 060601  
690 016746  
(1) 000212  
(1) 016746 13072  
691 016750  
(1) 000213  
(1) 016750 100601

```
MEMINC IMM,2
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IMM!<2>>
MEM IMM,0
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<0>>
OUTPUT MEMX,SELB!OMODEM ;CLEAR DATA TERMINAL READY
MICPC=MICPC+1
<MOVE!WROUT!MEMX!<SELB!OMODEM>>
ALWAYS RCXXX ;POST THE ERROR - FATAL
MICPC=MICPC+1
<JUMPIALCONDI!<RCXXX-INIT&3000*4>!<RCXXX-INIT&777/2>>
INSRV1: BRWRTE BR,SELB!SP1 ;INIT MODE?
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<SELB!SP1>>
BR0 BASSRV
MICPC=MICPC+1
<JUMPIBR0CONI!<BASSRV-INIT&3000*4>!<BASSRV-INIT&777/2>>
ALWAYS PROCER ;NO - PROCEDURE ERROR
MICPC=MICPC+1
<JUMPIALCONDI!<PROCER-INIT&3000*4>!<PROCER-INIT&777/2>>
```

693  
694 016752  
696 016752  
(1) 016752  
(2) 000214  
(2) 016752 002631  
701  
702 016754  
(1) 000215  
(1) 016754 010240  
703 016756  
(1) 000216  
(1) 016756 050220  
704 016760  
(1) 000217  
(1) 016760 123040  
705 016762  
(1) 000220  
(1) 016762 055302  
706 016764  
(1) 000221  
(1) 016764 050220  
707 016766  
(1) 000222  
(1) 016766 074520  
708  
709  
710 016770  
(1) 000223  
(1) 016770 055224  
711 016772  
(1) 000224  
(1) 016772 055225  
712 016774  
(1) 000225  
(1) 016774 055227  
713 016776  
(1) 000226  
(1) 016776 055226  
714  
715 017000  
(1) 000227  
(1) 017000 103757  
716  
718 017002  
(1) 000230  
(1) 017002 100451  
719 017004  
(1) 017004  
(2) 000231  
(2) 017004 000652  
724 017006  
(1) 000232  
(1) 017006 010240  
725 017010  
(1) 000233

```
.SBTTL OUTINT---SET UP OUTPUT INTERRUPT (RDYO)
OUTINT:
PSTATE PINT2
MEM IMM,<<PINT2-INIT&777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<PINT2-INIT&777/2>>>
;COMPLETION
LDMA IMM,NXTINT ;ADDRESS OF NEXT INTERRUPT POINTER
MICPC=MICPC+1
<MOVE!LDMA!IMM!<NXTINT&377>>
LDMA MEMX,SELB ;NEXT INTERRUPT
MICPC=MICPC+1
<MOVE!LDMA!MEMX!<SELB>>
SP IBUS,OCON,SP0 ;READ THE OUTPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!SPX!IBUS!OCON!SP0>
OUT <MEMX!INCMAR>,<AORB!OCON> ;WRITE THE OUT CONTROL CSR
MICPC=MICPC+1
<MOVE!WROUT!MEMX!INCMAR!<AORB!OCON>>
LDMA MEMX,SELB ;ADDRESS LINK
MICPC=MICPC+1
<MOVE!LDMA!MEMX!<SELB>>
BRWRTE <BR!INCMAR>,<AA!SP0> ;KICK PAST LINK STATUS BYTE
MICPC=MICPC+1
<MOVE!WRTEBR!BR!INCMAR!<AA!SP0>>
;SHIFT CSR0 IMAGE LEFT
;***DO NOT CHANGE BR UNTIL BR7***
OUT <MEMX!INCMAR>,<SELB!OPORT1> ;WRITE LOW BYTE OF BA TO CSR
MICPC=MICPC+1
<MOVE!WROUT!MEMX!INCMAR!<SELB!OPORT1>>
OUT <MEMX!INCMAR>,<SELB!OPORT2> ;WRITE HIGH BYTE OF BA TO CSR
MICPC=MICPC+1
<MOVE!WROUT!MEMX!INCMAR!<SELB!OPORT2>>
OUT <MEMX!INCMAR>,<SELB!OPORT4> ;WRITE HIGH BYTE OF COUNT TO CSR
MICPC=MICPC+1
<MOVE!WROUT!MEMX!INCMAR!<SELB!OPORT4>>
OUT <MEMX!INCMAR>,<SELB!OPORT3> ;WRITE THE LOW BYTE OF COUNT
MICPC=MICPC+1
<MOVE!WROUT!MEMX!INCMAR!<SELB!OPORT3>>
;***HERE IS BR7***
BR7 PE1 ;INTERRUPT ENABLE IS SET
MICPC=MICPC+1
<JUMPIBR7CONI!<PE1-INIT&3000*4>!<PE1-INIT&777/2>>
;GENERATE AN INTERRUPT
ALWAYS IDLE
MICPC=MICPC+1
<JUMPIALCONDI!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
PINT2: PSTATE OUTWAIT
MEM IMM,<<OUTWAIT-INIT&777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<OUTWAIT-INIT&777/2>>>
LDMA IMM,NXTINT ;ADDRESS NEXT INTERRUPT QUEUE
MICPC=MICPC+1
<MOVE!LDMA!IMM!<NXTINT&377>>
SP MEMX,SELB,SP0 ;COPY ADDRESS FOR NEXT INT TO SP0
MICPC=MICPC+1
```

(1) 017010 043220  
 726 017012 000234  
 (1) 017012 002642  
 727 017014 000235  
 (1) 017014 000776  
 728 017016 000236  
 (1) 017016 003360  
 729 017020 000237  
 (1) 017020 101642  
 730 017022 000240  
 (1) 017022 000402  
 731 017024 000241  
 (1) 017024 062400  
 732 017026 000242  
 (1) 017026 043220  
 733 017030 000243  
 (1) 017030 010241  
 734 017032 000244  
 (1) 017032 040360  
 735 017034 000245  
 (1) 017034 101647  
 736 017036 000246  
 (1) 017036 100451  
 737 017040 000247  
 (1) 017040 000757  
 738 017042 000250  
 (1) 017042 063261  
 739 017044 000251  
 (1) 017044 100451

```

<MOVE:SPX:MEMX:SELB:SP0>
MEM IMM,INTSTK ;ASSUME WRAP AROUND CASE
MICPC=MICPC+1
<MOVE:WRMEM:IMM:<INTSTK>>
BRWRT IMM,<<MMEND-2>> ;ADDRESS OF LAST INT IN STACK
MICPC=MICPC+1
<MOVE:WRTBR:IMM:<<MMEND-2>>>
CMP BR,SP0 ;SHOULD WE WRAP
MICPC=MICPC+1
<SUBTC:BR:SP0>
Z 5 ;YES--BRANCH
MICPC=MICPC+1
<JUMP:ZCOND:<56-INIT&3000*4>:<56-INIT&777/2>>
RRWRT IMM,2 ;OFFSET FOR NEXT POINTER
MICPC=MICPC+1
<MOVE:WRTBR:IMM:<2>>
MEM BR,ADDISP0 ;UPDATE POINTER
MICPC=MICPC+1
<MOVE:WRMEM:BR:ADDISP0>
SP MEMX,SELB,SP0 ;COPY POINTER TO SP0
MICPC=MICPC+1
<MOVE:SPX:MEMX:SELB:SP0>
LDMA IMM,NXTSP ;PICK UP START OF IN QUEUE
MICPC=MICPC+1
<MOVE:LDMA:IMM:<NXTSP&377>>
CMP MEMX,SP0 ;COMPARE TO END
MICPC=MICPC+1
<SUBTC:MEMX:SP0>
Z 100 ;IF EQUAL--CLEAR INT PENDING
MICPC=MICPC+1
<JUMP:ZCOND:<100-INIT&3000*4>:<100-INIT&777/2>>
ALWAYS IDLE
MICPC=MICPC+1
<JUMP:ALCOND:<IDLE-INIT&3000*4>:<IDLE-INIT&777/2>>
100: BRWRT IMM,357 ;MASK TO CLEAR INT PENDING
MICPC=MICPC+1
<MOVE:WRTBR:IMM:<357>>
CLRIDL: SP BR,ANDB,SP1
MICPC=MICPC+1
<MOVE:SPX:BR:ANDB:SP1>
ALWAYS IDLE
MICPC=MICPC+1
<JUMP:ALCOND:<IDLE-INIT&3000*4>:<IDLE-INIT&777/2>>

```

741  
 742 017046 000252  
 (1) 017046 123440  
 747 017050 000253  
 (1) 017050 103451  
 749 017052 000254  
 (1) 017052 000500  
 750 017054 000255  
 (1) 017054 061262  
 751 017056 000256  
 (1) 017056 100671

```

.SBTL OUTWAI--WAIT FOR RDYO TO GO AWAY
OUTWAI: SPBR IBUS,OCON,SP0 ;READ OUTPUT CONTROL CSR
MICPC=MICPC+1
<MOVE:SPBRX:IBUS:OCON:SP0>
BR7 IDLE
MICPC=MICPC+1
<JUMP:BR7CON:<IDLE-INIT&3000*4>:<IDLE-INIT&777/2>>
BRWRT IMM,100 ;CLEAR CONTROL BITS
MICPC=MICPC+1
<MOVE:WRTBR:IMM:<100>>
OUT BR,OOCON:AAADB
MICPC=MICPC+1
<MOVE:WROUTX:BR:OOCON:AAADB>
ALWAYS INS13
MICPC=MICPC+1
<JUMP:ALCOND:<INS13-INIT&3000*4>:<INS13-INIT&777/2>>

```



```

753
754 017060
(1) 000257
(1) 017060 123560
755 017062
(1) 000260
(1) 017062 001620
756 017064
(1) 000261
(1) 017064 102754
757 017066
(1) 000262
(1) 017066 002113
758 017070
(1) 000263
(1) 017070 000600
759 017072
(1) 000264
(1) 017072 102273
760 017074
(1) 000265
(1) 017074 123000
761 017076
(1) 000266
(1) 017076 000500
762 017100
(1) 000267
(1) 017100 001260
763 017102
(1) 000270
(1) 017102 010211
764 017104
(1) 000271
(2) 000271
(2) 017104 002533
765 017106
(1) 000272
(1) 017106 100451
766
767 017110
(1) 000273
(1) 017110 000600
768 017112
(1) 000274
(1) 017112 003301
769 017114
(1) 000275
(1) 017114 000604
770 017116
(1) 000276
(1) 017116 003230
771 017120
(1) 000277
(1) 017120 100665

```

```

.SBTTL CTLSRV--CNTL I SERVICE
CTLSRV: SPBR IBUS,PORT4,SP0 ;TO SP0
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!PORT4!SP0>
BRSHFT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTEBR!SELB>
BR1 HDSEL ;IF SET IS HALF DUPLEX
MICPC=MICPC+1
<JUMP!BRICONI!<HDSSEL-INIT&3000*4>!<HDSSEL-INIT&777/2>>
OUTPUT IMM,<100!MODEM> ;MASK DTR, TURN OFF HDX
MICPC=MICPC+1
<MOVE!WROUT!IMM!<100!MODEM>>
INS11: BRWRTE DP,<SELA!SP0> ;RESTORE THE CNTL WORD
MICPC=MICPC+1
<MOVE!WRTEBR!DP!<SELA!SP0>>
BR0 CBOOT ;IF SET IS BOOT
MICPC=MICPC+1
<JUMP!BR0CONI!<CBOOT-INIT&3000*4>!<CBOOT-INIT&777/2>>
INS12: SP IBUS,INCON,SP0 ;READ THE INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!SPX!IBUS!INCON!SP0>
BRWRTE IMM,100 ;ZERO THE BR REGISTER EXCEPT INT ENABLE
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<100>>
OUT BR,<AANDB!OINCON> ;CLEAR IN CONTROL CSR
MICPC=MICPC+1
<MOVE!WROUTX!IBR!<AANDB!OINCON>>
LDMA IMM,PRST ;ADDRESS PORT STATE
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<PRST&377>>
INS13: PSTATE NIDLE2
MEM IMM,<<NIDLE2-INIT&777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<NIDLE2-INIT&777/2>>>
ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCONDI!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
)
CBOOT: BRWRTE IMM,200 ;MASK FOR BOOT MODE
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<200>>
SP BR,AORB,SP1 ;IN PORT STATUS WORD
MICPC=MICPC+1
<MOVE!SPX!IBR!AORB!SP1>
BRWRTE IMM,204 ;MASK FOR OK TO SEND AND LINE IDLE
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<204>>
SP BR,SELB,SP10 ;IN LINE STATUS
MICPC=MICPC+1
<MOVE!SPX!IBR!SELB!SP10>
ALWAYS INS12
MICPC=MICPC+1
<JUMP!ALCONDI!<INS12-INIT&3000*4>!<INS12-INIT&777/2>>

```

```

773
774 017122
(1) 000300
(1) 017122 010070
775 017124
(1) 000301
(1) 017124 003220
776 017126
(1) 000302
(1) 017126 016401
777 017130
(1) 000303
(1) 017130 014543
778
779 017132
(1) 000304
(1) 017132 136500
780 017134
(1) 000305
(1) 017134 136520
781 017136
(1) 000306
(1) 017136 136560
782 017140
(1) 000307
(1) 017140 136540
783 017142
(1) 000310
(1) 017142 010070
784 017144
(1) 000311
(1) 017144 002471
785 017146
(1) 000312
(1) 017146 000360
786 017150
(1) 000313
(1) 017150 017116
787 017152
(1) 000314
(1) 017152 000406
788 017154
(1) 000315
(1) 017154 002400
789 017156
(1) 000316
(1) 017156 000402
790 017160
(1) 000317
(1) 017160 003310
791 017162
(1) 000320
(1) 017162 100665

```

```

.SBTTL TBASRV--TRANSMITTER BUFFER ADDRESS SERVICE
TBASRV: LDMA IMM,ETC ;GET POINTER TO END OF TMT CHAIN
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<ETC&377>>
LDMA MEMX,<SELB!SPX!SP0> ;FIND THE LINK
MICPC=MICPC+1
<MOVE!LDMAR!MEMX!<SELB!SPX!SP0>>
MEMINC IMM,1 ;BUFFER ASSIGNED IN IN LINK FLAGS
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IMM!<1>>
BRWRTE <IMM!INCMAR>,TML0 ;POINT PAST NUMBER FIELD
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!INCMAR!<TML0>>
;SET BR FOR ADDITION TO SP0
MEMINC IBUS,PORT1
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IBUS!<PORT1>>
MEMINC IBUS,PORT2
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IBUS!<PORT2>>
MEMINC IBUS,PORT4
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IBUS!<PORT4>>
MEMINC IBUS,PORT3
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IBUS!<PORT3>>
LDMA IMM,ETC
MICPC=MICPC+1
<MOVE!LDMAR!IMM!<ETC&377>>
MEM IMM,TML1 ;ASSUME QUEUE WRAP AROUND
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<TML1>>
CNP BR,SP0 ;END OF CHAIN?
MICPC=MICPC+1
<SUBTC!IBR!SP0>
Z 104 ;IF YES--BRANCH
MICPC=MICPC+1
<JUMP!ZCONDI!<104-INIT&3000*4>!<104-INIT&777/2>>
BRWRTE IMM,6 ;QUEUE ENTRY LENGTH
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<6>>
MEM BR,ADD!SP0 ;UPDATE THE END POINTER IN MEMORY
MICPC=MICPC+1
<MOVE!WRMEM!IBR!<ADD!SP0>>
126: BRWRTE IMM,2 ;NUMBERED MSG PENDING MASK
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<2>>
SP BR,AORB,SP10 ;UPDATE LINE STATUS
MICPC=MICPC+1
<MOVE!SPX!IBR!AORB!SP10>
ALWAYS INS12
MICPC=MICPC+1
<JUMP!ALCONDI!<INS12-INIT&3000*4>!<INS12-INIT&777/2>>

```

793  
794 017164  
(1) 000321  
(1) 017164 010023  
795 017166  
(1) 000322  
(1) 017166 053220  
796 017170  
(1) 000323  
(1) 017170 016401  
797 017172  
(1) 000324  
(1) 017172 136500  
798 017174  
(1) 000325  
(1) 017174 136520  
799 017176  
(1) 000326  
(1) 017176 136500  
800 017200  
(1) 000327  
(1) 017200 136540  
801  
802 017202  
(1) 000330  
(1) 017202 010023  
803 017204  
(1) 000331  
(1) 017204 002424  
804 017206  
(1) 000332  
(1) 017206 000462  
805 017210  
(1) 000333  
(1) 017210 000360  
806 017212  
(1) 000334  
(1) 017212 010665  
807 017214  
(1) 000335  
(1) 017214 000405  
808 017216  
(1) 000336  
(1) 017216 002400  
809 017220  
(1) 000337  
(1) 017220 100065  
810 017222  
(1) 000340  
(1) 017222 000717  
811 017224  
(1) 000341  
(1) 017224 003070  
812 017226  
(1) 000342  
(1) 017226 000400

.SBTTL RBASRV--RECEIVE BUFFER ADDRESS SERVICE  
RDMA IMM,ERC ;ADDRESS END OF RECEIVE CHAIN  
RBASRV: LDMA IMM,ERC  
MICPC=MICPC+1  
<MOVE!LDMA!IMM!<ERC&377>>  
LDMA MEMX,<SELB!SPX!SP0> ;GET THE POINTER TO LINK  
MICPC=MICPC+1  
<MOVE!LDMA!MEMX!<SELB!SPX!SP0>>  
MEMINC IMM,1  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IMM!<1>>  
MEMINC IBUS,PORT1  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IBUS!<PORT1>>  
MEMINC IBUS,PORT2  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IBUS!<PORT2>>  
MEMINC IBUS,PORT4  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IBUS!<PORT4>>  
MEMINC IBUS,PORT3  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!IBUS!<PORT3>>  
;;;NOTE INVERTED ORDER OF PORT 3 AND PORT4  
LDMA IMM,ERC  
MICPC=MICPC+1  
<MOVE!LDMA!IMM!<ERC&377>>  
MEM IMM,RCL1 ;ASSUME WRAP AROUND CASE  
MICPC=MICPC+1  
<MOVE!WRMEM!IMM!<RCL1>>  
BRWRT IMM,RCL7 ;GET ADDRESS OF END OF CAHIN AREA  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<RCL7>>  
CMF BR,SP0 ;CHECK FOR END  
MICPC=MICPC+1  
<SUBTC!BR!SP0>  
Z IMM,12 ;IF EQUAL BRANCH  
MICPC=MICPC+1  
<JUMPIALCONDI!<INS12-INIT&3000\*4>!<INS12-INIT&777/2>>  
BRWRT IMM,5 ;CALCULATE ADDRESS OF NEXT LINK  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<5>>  
MEM BR,ADD!SP0 ;..  
MICPC=MICPC+1  
<MOVE!WRMEM!BR!<ADD!SP0>>  
ALWAYS IMM,12 ;EXIT  
MICPC=MICPC+1  
<JUMPIALCONDI!<INS12-INIT&3000\*4>!<INS12-INIT&777/2>>  
RA1: BRWRT IMM,317 ;MASK TO CLEAR START MODE AND CLR ACTIVE  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<317>>  
SPBR BR,ANDB,SP10 ;CLEAR BIT IN LINE STATUS WORD  
MICPC=MICPC+1  
<MOVE!SPBR!BR!<ANDB!SP10>>  
RA3: BRWRT IMM,0 ;CLEAR BR  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<0>>

813 017230  
(1) 000343  
(1) 017230 063233  
814 017232  
(1) 000344  
(1) 017232 000424  
815 017234  
(1) 000345  
(1) 017234 100450  
816  
818 017236  
(1) 000346  
(1) 017236 060530  
819 017240  
(1) 000347  
(1) 017240 103351  
820 017242  
(1) 000350  
(1) 017242 100451  
821 017244  
(1) 000351  
(1) 017244 000727  
822 017246  
(1) 000352  
(1) 017246 063270  
823 017250  
(1) 000353  
(1) 017250 104507

SP BR,SELB,SP13 ;SET NUMB MESSAGE TYPE IN SP13  
MICPC=MICPC+1  
<MOVE!SPX!BR!<SELB!SP13>>  
STATE RCVB ;CHANGE RECEIVE STATE POINTER TO STATE B  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<RCVB-INIT&777/2>>  
ALWAYS REXIT  
MICPC=MICPC+1  
<JUMPIALCONDI!<REXIT-INIT&3000\*4>!<REXIT-INIT&777/2>>  
J  
ACK: BRWRT BR,AA!SP10 ;READ LINE STATUS SHIFTING LEFT  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR!<AA!SP10>>  
BR4 58 ;IF START RECD--CLEAR START MODE  
MICPC=MICPC+1  
<JUMPIALCONDI!<58-INIT&3000\*4>!<58-INIT&777/2>>  
ALWAYS IDLE  
MICPC=MICPC+1  
<JUMPIALCONDI!<IDLE-INIT&3000\*4>!<IDLE-INIT&777/2>>  
58: BRWRT IMM,327 ;CLEAR START MODE  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<327>>  
SP BR,ANDB,SP10 ;IN LINE STATUS  
MICPC=MICPC+1  
<MOVE!SPX!BR!<ANDB!SP10>>  
ALWAYS RDS  
MICPC=MICPC+1  
<JUMPIALCONDI!<RDS-INIT&3000\*4>!<RDS-INIT&777/2>>

826 117252  
 (1) 000354  
 (1) 017252 000500  
 827 017254  
 (1) 000355  
 (1) 017254 003310  
 828 017256  
 (1) 000356  
 (1) 017256 102663  
 829  
 830 017260  
 (1) 000357  
 (1) 017260 002700  
 831 017262  
 (1) 000360  
 (1) 017262 123220  
 832 017264  
 (1) 000361  
 (1) 017264 001311  
 834 017266  
 (1) 000362  
 (1) 017266 100451  
 839  
 840 017270  
 (1) 000363  
 (1) 017270 002722  
 841  
 842 017272  
 (1) 000364  
 (1) 017272 000402  
 843 017274  
 (1) 000365  
 (1) 017274 001231  
 844 017276  
 (1) 000366  
 (1) 017276 120620  
 845 017300  
 (1) 000367  
 (1) 017300 002766  
 846 017302  
 (1) 000370  
 (1) 017302 154620  
 847 017304  
 (1) 000371  
 (1) 017304 120620  
 848 017306  
 (1) 000372  
 (1) 017306 103363  
 849 017310  
 (1) 000373  
 (1) 017310 114725  
 850  
 851 017312  
 (1) 000374  
 (1) 017312 120600  
 852 017314

```

H0SEL: BRWRTE IMM,100 ;HD MASK TO BR
        MICPC=MICPC+1
        <MOVE!WRTEBR!IMM!<100>>
        SP BR,AORB,SP10 ;UPDATE PORI STATUS WORD
        MICPC=MICPC+1
        <MOVE!SPXIBR!AORB!SP10>
        ALWAYS INS11
        MICPC=MICPC+1
        <JUMP!ALCONDI<INS11-INIT&3000*4>!<INS11-INIT&777/2>>
        ;
PE1: BRWRTE IMM,300 ;MASK FOR INTERRUPT AND VECTOR THROUGH X04
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<300>>
      SP IBUS,UBBR,SP0 ;READ BR CONTROL REG
      MICPC=MICPC+1
      <MOVE!SPXIBUS!UBBR!SP0>
      OUT BR,<AORB!OBR> ;INTERRUPT
      MICPC=MICPC+1
      <MOVE!WROUTX!BR!<AORB!OBR>>
      ALWAYS IDLE
      MICPC=MICPC+1
      <JUMP!ALCONDI<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
      ;
HALTED: MEMADR EM6
        MICPC=MICPC+1
        <MOVE!WRMEM!<EM6-INIT&777/2>>
        ;FALL INTO ACLOW
        ;CAUSE AN AC LOW
ACLOW: BRWRTE IMM,2
        MICPC=MICPC+1
        <MOVE!WRTEBR!IMM!<2>>
        OUT BR,<SELB!OBR>
        MICPC=MICPC+1
        <MOVE!WROUTX!BR!<SELB!OBR>>
5s: BRWRTE IBUS,UBBR ;WAIT FOR IT TO COMPLETE
     MICPC=MICPC+1
     <MOVE!WRTEBR!IBUS!<UBBR>>
     BR1 56
     MICPC=MICPC+1
     <JUMP!BR1CON!<5s-INIT&3000*4>!<5s-INIT&777/2>>
     ,ALWAY MEMX,SELB,PAGE3
     MICPC=MICPC+1
     <JUMP!ALCONDI<MEMX!SELB!PAGE3>
CKTIME: BRWRTE IBUS,UBBR ;READ BR CONTROL REG
        MICPC=MICPC+1
        <MOVE!WRTEBR!IBUS!<UBBR>>
        BR4 HALTED
        MICPC=MICPC+1
        <JUMP!BR4CON!<HALTED-INIT&3000*4>!<HALTED-INIT&777/2>>
        ALWAYS EM1
        MICPC=MICPC+1
        <JUMP!ALCONDI<EM1-INIT&3000*4>!<EM1-INIT&777/2>>
        ;
TBU1: BRWRTE IBUS,NPR
      MICPC=MICPC+1
      <MOVE!WRTEBR!IBUS!<NPR>>
      BR0 IDLE
  
```

(1) 000375  
 (1) 017314 102051  
 853 017316  
 (1) 000376  
 (1) 017316 114752  
 854 017320  
 (1) 000377  
 (1) 017320 002000  
 855

```

MICPC=MICPC+1
<JUMP!BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
ALWAYS EC2
MICPC=MICPC+1
<JUMP!ALCONDI<EC2-INIT&3000*4>!<EC2-INIT&777/2>>
SZERO
MICPC=MICPC+1
000000
  
```

```

857      017322      .=INIT+1000
858      000377      MICPC=377
859      .SBITL RCVA--ROUTINE TO HANDLE FIRST DDCMP CHARACTER
860      ;ENTERED FROM IDLE LOOP
861      ;DETERMINES IF MESSAGE TYPE IS NUMBERED, UNNUMBERED OR BOOT
862      ;SETS UP APPROPRIATE STATES FOR REST OF MESSAGE.
863      RCVA:      SP      IBUS,RCVDAT,SP0      ;READ RECEIVE CHARACTER TO SP0
(1)      000400      MICPC=MICPC+1
(1)      017322      <MOVE!SPX!IBUS!RCVDAT!SP0>
864      017324      BRWRT BR,SEL!ISP1      ;READ PORT STATUS WORD
(1)      000401      MICPC=MICPC+1
(1)      017324      <MOVE!WRTEBR!BRI<SEL!ISP1>>
865      017326      BR0      55      ;IF INIT MODE---ONLY BOOT OK
(1)      000402      MICPC=MICPC+1
(1)      017326      <JUMP!BR0!CON!<55-INIT&3000*4>!<55-INIT&777/2>>
866      017330      BR7      55      ;IF BOOT MODE---ONLY BOOT OK
(1)      000403      MICPC=MICPC+1
(1)      017330      <JUMP!BR7!CON!<55-INIT&3000*4>!<55-INIT&777/2>>
867      017332      BRWRT IMM,201      ;SOH TO BR
(1)      000404      MICPC=MICPC+1
(1)      017332      <MOVE!WRTEBR!IMM!<201>>
868      017334      CMP      BR,SP0      ;COMPARE BR TO SP0
(1)      000405      MICPC=MICPC+1
(1)      017334      <SUBTC!BR!SP0>
869      017336      Z      RA1      ;IF EQUAL--IS NUMBERED MESSAGE
(1)      000406      MICPC=MICPC+1
(1)      017336      <JUMP!Z!CONDI<RA1-INIT&3000*4>!<RA1-INIT&777/2>>
870      017340      BRWRT IMM,5      ;ENQ TO BR
(1)      000407      MICPC=MICPC+1
(1)      017340      <MOVE!WRTEBR!IMM!<5>>
871      017342      CMP      BR,SP0      ;COMPARE ENQ TO SP0
(1)      000410      MICPC=MICPC+1
(1)      017342      <SUBTC!BR!SP0>
872      017344      Z      RA2      ;IF EQUAL--IS UNNUMBERED MESSAGE
(1)      000411      MICPC=MICPC+1
(1)      017344      <JUMP!Z!CONDI<RA2-INIT&3000*4>!<RA2-INIT&777/2>>
873      017346      BRWRT IMM,220      ;DLE TO BR
(1)      000412      MICPC=MICPC+1
(1)      017346      <MOVE!WRTEBR!IMM!<220>>
874      017350      CMP      BR,SP0      ;COMPARE DLE TO SP0
(1)      000413      MICPC=MICPC+1
(1)      017350      <SUBTC!BR!SP0>
875      017352      Z      BOOT      ;IF EQUAL IS BOOT
(1)      000414      MICPC=MICPC+1
(1)      017352      <JUMP!Z!CONDI<BOOT-INIT&3000*4>!<BOOT-INIT&777/2>>
876      017354      FLUSH:      OUTPUT IMM,<200!ORCVCO>      ;FLUSH INPUT SILO
(1)      000415      MICPC=MICPC+1
(1)      017354      <MOVE!WRROUT!IMM!<200!ORCVCO>>
877      ;(LOW ORDER BITS READ ONLY)
878      017356      BRWRT IMM,357      ;MASK TO CLEAR--CLEAR ACTIVE
(1)      000416      MICPC=MICPC+1
(1)      017356      <MOVE!WRTEBR!IMM!<357>>
879      017360      SP      BR,AANDB,SP10      ;IN LINE STATUS WORD
(1)      000417      MICPC=MICPC+1
(1)      017360      <MOVE!SPX!BRI!AANDB!SP10>
884      017362      RM1:      STATE RCVA

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(1)      000420      MICPC=MICPC+1
(1)      017362      <MOVE!WRTEBR!IMM!<RCVA-INIT&777/2>>
885      017364      ALWAYS REXIT
(1)      000421      MICPC=MICPC+1
(1)      017364      <JUMP!ALCONDI<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
887      017366      RA2:      STATE RCVI      ;CHANGE RECEIVE STATE TO 1
(1)      000422      MICPC=MICPC+1
(1)      017366      <MOVE!WRTEBR!IMM!<RCVI-INIT&777/2>>
889      017370      ALWAYS REXIT
(1)      000423      MICPC=MICPC+1
(1)      017370      <JUMP!ALCONDI<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

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896 .SBTTL RCVB--ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD
897 ;ENTERED FROM IDLE LOOP
898 ;STORES COUNT FIELD AND SETS UP RCVC AS NEXT STATE
899 ;
900 RCVB: SP IBUS,RCVDAT,SP4 ;READ CHARACTER TO SP4
(1) MICPC=NICPC+1
(1) <MOVE!SPX!IBUS!RCVDAT!SP4>
901 LDMA BR,<SEL!SP14> ;LOAD MAR WITH ADDRESS OF CURRENT BA
(1) MICPC=NICPC+1
(1) <MOVE!LDMAR!BRI!<SEL!SP14>>
902 BRWRT MEMX,INCMAR!SELB ;READ FLAGS BYTE
(1) MICPC=NICPC+1
(1) <MOVE!WRTEBRI!MEMX!<INCMAR!SELB>>
903 SR0 RB1 ;RCV BUFFER ASSIGNED---CONTINUE
(1) MICPC=NICPC+1
(1) <JUMP!BROCON!<RB1-INIT!3000*4>!<RB1-INIT!777/2>>
904 BRWRT BR,SEL!SP1 ;READ STATUS BYTE
(1) MICPC=NICPC+1
(1) <MOVE!WRTEBRI!BRI!<SEL!SP1>>
905 BRT RB3 ;MAINT MODE
(1) MICPC=NICPC+1
(1) <JUMP!BROCON!<RB3-INIT!3000*4>!<RB3-INIT!777/2>>
906 LDMA IMM,T ;ERROR--LOAD TYPE FIELD ADDRESS IN MAR
(1) MICPC=NICPC+1
(1) <MOVE!LDMAR!IMM!<T!377>>
907 MEMINC IMM,2 ;LOAD NAK TYPE
(1) MICPC=NICPC+1
(1) <MOVE!WRMEM!INCMAR!IMM!<2>>
908 MEM IMM,310 ;LOAD SUB-TYPE NO BUFFERS
(1) MICPC=NICPC+1
(1) <MOVE!WRMEM!IMM!<310>>
909 LDMA IMM,NTLS
(1) MICPC=NICPC+1
(1) <MOVE!LDMAR!IMM!<R!T!LS!377>>
910 ALWAYS RH5 ;BRANCH TO SEND NAK ROUTINE
(1) MICPC=NICPC+1
(1) <JUMP!ALCONDI!<RH5-INIT!3000*4>!<RH5-INIT!777/2>>
911 BRWRT IMM,4 ;MASK FOR NO BUFFER AVAILABLE
(1) MICPC=NICPC+1
(1) <MOVE!WRTEBRI!IMM!<4>>
912 SP BR,AORB,SP1 ;SET THE FLAG
(1) MICPC=NICPC+1
(1) <MOVE!SPX!BRI!AORB!SP1>
913 STATE RCVC
(1) MICPC=NICPC+1
(1) <MOVE!WRTEBRI!IMM!<RCVC-INIT!777/2>>
914 SP BR,SELB,SP3
(1) MICPC=NICPC+1
(1) <MOVE!SPX!BRI!SELB!SP3>
915 OUTPUT <MEMX!INCMAR,<SELB!OBA1> ;OUTPUT LOW ORDER BYTE OF ADDRESS
(1) MICPC=NICPC+1
(1) <MOVE!WROUT!MEMX!INCMAR!<SELB!OBA1>>
916 OUTPUT MEMX,INCMAR,<SELB!OBA2> ;OUTPUT HIGH BYTE OF ADDRESS
(1) MICPC=NICPC+1
(1) <MOVE!WROUT!MEMX!INCMAR!<SELB!OBA2>>
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918 SP UBBR,SP0 ;READ THE BUS REQ REGISTER
(1) MICPC=NICPC+1
(1) <MOVE!SPX!IBUS!UBBR!SP0>
919 BRWRT IMM,101 ;MASK OFF ALL BUT NXM AND VEC4 BITS
(1) MICPC=NICPC+1
(1) <MOVE!WRTEBRI!IMM!<101>>
920 SP BR,AANDB,SP0 ;AND SAVE IN SP0
(1) MICPC=NICPC+1
(1) <MOVE!SPX!BRI!AANDB!SP0>
921 SP IMM,300,SP5 ;MASK TO ISOLATE EX. MEM BITS
(1) MICPC=NICPC+1
(1) <MOVE!SPX!IMM!300!SP5>
922 ;NOTE THIS REALLY WRITES A 305 BUT THE
923 ;5 GETS SHIFTED OUT
924 BRWRT MEMX,AANDB!SP5 ;MASK ALL BUT EX. MEM BITS
(1) MICPC=NICPC+1
(1) <MOVE!WRTEBRI!MEMX!<AANDB!SP5>>
925 BRSHFT ;SHIFT THEM INTO THE CORRECT POSITION
(1) MICPC=NICPC+1
(1) <MOVE!SHFTBRI!WRTEBRI!SELB>
926 LRSHT
(1) MICPC=NICPC+1
(1) <MOVE!SHFTBRI!WRTEBRI!SELB>
927 BRSHFT
(1) MICPC=NICPC+1
(1) <MOVE!SHFTBRI!WRTEBRI!SELB>
928 BRSHFT
(1) MICPC=NICPC+1
(1) <MOVE!SHFTBRI!WRTEBRI!SELB>
929 OUT BR,AORB!OBR ;WRITE EX MEM BITS OUT
(1) MICPC=NICPC+1
(1) <MOVE!WROUTX!BRI!<AORB!OBR>>
930 ALWAYS IDLE
(1) MICPC=NICPC+1
(1) <JUMP!ALCONDI!<IDLE-INIT!3000*4>!<IDLE-INIT!777/2>>
931 ALWAYS I2
(1) MICPC=NICPC+1
(1) <JUMP!ALCONDI!<I2-INIT!3000*4>!<I2-INIT!777/2>>
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938 017464  
939 017464  
(1) 000461  
(1) 017464 023205  
944 017466  
(1) 000462  
(1) 017466 000600  
945 017470  
(1) 000463  
(1) 017470 000605  
946 017472  
(1) 000464  
(1) 017472 063310  
947 017474  
(1) 000465  
(1) 017474 010167  
948 017476  
(1) 000466  
(1) 017476 076004  
949 017500  
(1) 000467  
(1) 017500 076605  
951 017502  
(1) 000470  
(1) 017502 060472  
952 017504  
(1) 000471  
(1) 017504 100450

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.SBTT: RCVC--ROUTINE TO HANDLE SECOND CHARACTER OF COUNT FIELD, SELECT AND FINAL
;ENTERED FROM IDLE LOOP
;INTERPRETS SELECT AND FINAL
;CHECKS FOR COUNT TOO LARGE
;
RCVC:
SP      IBUS,RCVDAT,SP5      ;GET CHARACTER
NICPC=MICPC+1
<MOVE!SPX!IBUS!RCVDAT!SP5>
BRWRTI IMM,200              ;SEPARATE SELECT BIT FROM COUNT
NICPC=MICPC+1
<MOVE!WRTEBRI!IMM!<200>>
BRWRTI BR,AANDB!SP5
NICPC=MICPC+1
<MOVE!WRTEBRI!BR!<AANDB!SP5>>
SP      BR,AORB,SP10
NICPC=MICPC+1
<MOVE!SPX!BR!AORB!SP10>
LDMA   IMM,BC              ;LOAD MAR TO BYTE COUNT
NICPC=MICPC+1
<MOVE!LDMAR!IMM!<BC&377>>
MEMINC BR,SELA!SP4        ;SAVE LOW BYTE
NICPC=MICPC+1
<MOVE!WRMEM!INCMAR!BR!<SELA!SP4>>
MEMINC BR,SELA!SP5        ;AND NOW HIGH BYTE
NICPC=MICPC+1
<MOVE!WRMEM!INCMAR!BR!<SELA!SP5>>
RC5:   STATE RCVD          ;SET NEXT STATE TO D
NICPC=MICPC+1
<MOVE!WRTEBRI!IMM!<RCVD=INIT&777/2>>
ALWAYS REXIT
NICPC=MICPC+1
<JUMPI!ALCONDI!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
```

954  
955  
956 017506  
(1) 000472  
(1) 017506 000513  
957 017510  
(1) 000473  
(1) 017510 063223  
958 017512  
(1) 000474  
(1) 017512 023600  
959 017514  
(1) 000475  
(1) 017514 060757  
960 017516  
(1) 000476  
(1) 017516 107500  
961 017520  
(1) 000477  
(1) 017520 100451  
962 017522  
(1) 000500  
(1) 017522 060601  
963 017524  
(1) 000501  
(1) 017524 103451  
964 017526  
(1) 000502  
(1) 017526 060610  
965 017530  
(1) 000503  
(1) 017530 061620  
966 017532  
(1) 000504  
(1) 017532 103051  
967 017534  
(1) 000505  
(1) 017534 010153  
968 017536  
(1) 000506  
(1) 017536 062600  
969 017540  
(1) 000507  
(1) 017540 010403  
970  
971 017542  
(1) 000510  
(1) 017542 022401  
972 017544  
(1) 000511  
(1) 017544 063235  
973 017546  
(1) 000512  
(1) 017546 100451

```
.SBTT: RCVD--ROUTINE TO HANDLE RESPONSE FIELD FOR NUMBERED MESSAGES
;
RCVD:  STATE RCVE
NICPC=MICPC+1
<MOVE!WRTEBRI!IMM!<RCVE-INIT&777/2>>
RD2:   SP      BR,SELB,SP3      ;SAVE THE STATE
NICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP3>
SPBR   IBUS,RCVDAT,SP0      ;INPUT THE CHARACTER
NICPC=MICPC+1
<MOVE!SPBRX!IBUS!RCVDAT!SP0>
BRWRTI BR,SUB!SP17          ;COMPARE NEW R TO LAST R
NICPC=MICPC+1
<MOVE!WRTEBRI!BR!<SUB!SP17>>
BR7    108
NICPC=MICPC+1
<JUMPI!BR7CONI!<108-INIT&3000*4>!<108-INIT&777/2>>
ALWAYS IDLE
NICPC=MICPC+1
<JUMPI!ALCONDI!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
108:   BRWRTI BR,SELA!SP1      ;READ STATUS BYTE
NICPC=MICPC+1
<MOVE!WRTEBRI!BR!<SELA!SP1>>
BR7    IDLE                  ;MAINT. MODE - GET OUT
NICPC=MICPC+1
<JUMPI!BR7CONI!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
BRWRTI BR,SELA!SP10
NICPC=MICPC+1
<MOVE!WRTEBRI!BR!<SELA!SP10>>
BRSHFT
NICPC=MICPC+1
<MOVE!SHFTBRI!WRTEBRI!SELB>
BR4    IDLE
NICPC=MICPC+1
<JUMPI!BR4CONI!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
LDMA   IMM,ISP17            ;ADDRESS LAST ACKED IMAGE
NICPC=MICPC+1
<MOVE!LDMAR!IMM!<ISP17&377>>
MEM     BR,SELA!SP0        ;COPY THE CHAR
NICPC=MICPC+1
<MOVE!WRMEM!BR!<SELA!SP0>>
RD5:   BRWRTI IMM!LDMAR,REPST  ;SET UP COUNT FOR TIMER
NICPC=MICPC+1
<MOVE!WRTEBRI!IMM!LDMAR!<REPST>>
MEM     IMM,1                ;***DEPENDENT ON REPST = 2
NICPC=MICPC+1
<MOVE!WRMEM!IMM!<1>>
SP      BR,SELB,SP15        ;RESET THE COUNT
NICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP15>
ALWAYS IDLE
NICPC=MICPC+1
<JUMPI!ALCONDI!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
```

975  
976  
977 017550 000513  
(1) 017550 000601  
978 017552 000514  
(1) 017552 107703  
979 017554 000515  
(1) 017554 020600  
980 017556 000516  
(1) 017556 000371  
981 017560 000517  
(1) 017560 105522  
982 017562 000520  
(1) 017562 003173  
983 017564 000521  
(1) 017564 104523  
984 017566 000522  
(1) 017566 003071  
985 017570 000523  
(1) 017570 000525  
986 017572 000524  
(1) 017572 100450

```
.SBTTL RCVE--ROUTINE TO HANDLE N FIELD OF NUMBERED MESSAGE
;
RCVE: BRWRITE BR,SELA!SP1 ;READ THE STATUS BYTE
      MICPC=MICPC+1
      <MOVE!WRTEBR!BR!<SELA!SP1>>
      BR7 RCYQ
      MICPC=MICPC+1
      <JUMP!BP7CONI!<RCYQ-INIT&3000*4>!<RCYQ-INIT&777/2>>
      BRWRITE IBUS,RCVDAT ;INPUT THE CHARACTER
      MICPC=MICPC+1
      <MOVE!WRTEBR!IBUS!<RCVDAT>>
      CMP BR,SP11
      MICPC=MICPC+1
      <SUBTC!BR!SP11>
      Z S6
      MICPC=MICPC+1
      <JUMP!ZCOND!<S6-INIT&3000*4>!<S6-INIT&777/2>>
      SP BR,DECA,SP13 ;FORCE MSG TYPE TO -1
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP13>
      ALWAYS RE2
      MICPC=MICPC+1
      <JUMP!ALCONDI!<RE2-INIT&3000*4>!<RE2-INIT&777/2>>
56: SP BR,INCA,SP11 ;UPDATE R FIELD
      MICPC=MICPC+1
      <MOVE!SPX!BR!INCA!SP11>
RE2: STATE RCVF ;NEXT RECEIVE STATE IS F
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<RCVF-INIT&777/2>>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP!ALCONDI!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
```

988  
989 017574 000525  
(1) 017574 003164  
990 017576 000526  
(1) 017576 125130  
991 017600 000527  
(1) 017600 003165  
992 017602 000530  
(1) 017602 000533  
993 017604 000531  
(1) 017604 020200  
994 017606 000532  
(1) 017606 100450  
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998 017610 000533  
(1) 017610 000535  
999 017612 000534  
(1) 017612 104531

```
.SBTTL RCVF--ROUTINE TO IGNORE ADDRESS
RCVF: SP BR,DECA,SP4 ;DECREMENT LOW BYTE OF COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP4>
      C RCVF0 ;NO OVERFLOW
      MICPC=MICPC+1
      <JUMP!CCONDI!<RCVF0-INIT&3000*4>!<RCVF0-INIT&777/2>>
      SP BR,DECA,SP5 ;OVERFLOW - DECREMENT HIGH BYTE
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP5>
RCVF0: STATE RCVG
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<RCVG-INIT&777/2>>
RCVF1: NOP IBUS,RCVDAT,0 ;INPUT CHARACTER - AND DISCARD
      MICPC=MICPC+1
      <IBUS!RCVDAT!0>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP!ALCONDI!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
;
.SBTTL RCVG--ROUTINE TO IGNORE CRC1
;
RCVG: STATE RCVH ;NEXT STATE IS RCVH
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<RCVH-INIT&777/2>>
      ALWAYS RCVF1
      MICPC=MICPC+1
      <JUMP!ALCONDI!<RCVF1-INIT&3000*4>!<RCVF1-INIT&777/2>>
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1003 017614  
1004 017614  
(1) 000535  
(1) 017614 023200  
1005 017616  
(1) 000536  
(1) 017616 020640  
1006 017620  
(1) 000537  
(1) 017620 116165  
1007 017622  
(1) 000540  
(1) 017622 060601  
1008 017624  
(1) 000541  
(1) 017624 107740  
1009 017626  
(1) 000542  
(1) 017626 060610  
1010 017630  
(1) 000543  
(1) 017630 020620  
1011 017632  
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(1) 017632 117307  
1012 017634  
(1) 000545  
(1) 017634 012151  
1013 017636  
(1) 000546  
(1) 017636 016402  
1014 017640  
(1) 000547  
(1) 017640 016701  
1015 017642  
(1) 000550  
(1) 017642 062617  
1016 017644  
(1) 000551  
(1) 017644 010013  
1017 017646  
(1) 000552  
(1) 017646 043220  
1018 017650  
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(1) 017650 062460  
1019 017652  
(1) 000554  
(1) 017652 010001  
1020 017654  
(1) 000555  
(1) 017654 040620  
1021 017656  
(1) 000556

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.SBTL RCVH--ROUTINE TO HANDLE CRC2 AND TO DISPATCH NUMBERED AND UNNUMBERED TYP
;
RCVH:
SP      IBUS,RCVDAT,SP0          ;GET CHAR IN SP0
MICPC=MICPC+1
<MOVEI SPX1IBUSIRCVDAT:SP0>
BRWRT IBUS,RCVCON              ;READ RECVR CONTROL REGISTER
MICPC=MICPC+1
<MOVEI WRTBRIBRI<RCVCON>>
BR0   TDON1                    ;IF BCC MATCH SET CRC IS GOOD
MICPC=MICPC+1
<JUMPI BR0CONI<TDON1-INIT&3000*4>I<TDON1-INIT&777/2>>
BRWRT BR,SELA:SP1              ;READ STATUS BYTE
MICPC=MICPC+1
<MOVEI WRTBRIBRI<SELA:SP1>>
BR7   RHX                      ;MAINT MODE
MICPC=MICPC+1
<JUMPI BR7CONI<RHX-INIT&3000*4>I<RHX-INIT&777/2>>
BRWRT DP,<SELA:SP10>           ;READ PORT STATUS WORD TO BR
MICPC=MICPC+1
<MOVEI WRTBRIBRI<SELA:SP10>>
BRSHFT
MICPC=MICPC+1
<MOVEI SHFTBRI<WRTBRIBRI>>
BR4   SNAK1                    ;IF START MODE--PROCEED TO RESEND START
MICPC=MICPC+1
<JUMPI BR4CONI<SNAK1-INIT&3000*4>I<SNAK1-INIT&777/2>>
LDMA  IMM,T                    ;ELSE BCC ERROR--LOAD ADDRESS OF TYPE FI
MICPC=MICPC+1
<MOVEI LDMA:IMM<T&377>>
MEMINC IMM,2                   ;WRITE NAK TYPE
MICPC=MICPC+1
<MOVEI WRMEMI<INCMAR:IMM<2>>>
MEMINC IMM,301                ;WRITE HEADER BCC ERROR SUBTYPE
MICPC=MICPC+1
<MOVEI WRMEMI<INCMAR:IMM<301>>>
MEM  BR,SELA:SP17             ;RESTORE LAST ACKED IMAGE
MICPC=MICPC+1
LDMA  IMM,NHDS                 ;ADDRESS CUM ERROR COUNTER
MICPC=MICPC+1
<MOVEI LDMA:IMM<NHDS&377>>
RHS:  SP      MEMX,SELB,SP0    ;WRITE IT TO SP0
MICPC=MICPC+1
<MOVEI SPX1MEMX:SELB:SP0>
MEM  BR,INCA:SP0              ;INCREMENT IT
MICPC=MICPC+1
<MOVEI WRMEMI<BRI<INCA:SP0>>>
LDMA  IMM,NAKST                ;ADDRESS NAKS TMED DYNAMIC
MICPC=MICPC+1
<MOVEI LDMA:IMM<NAKST&377>>
BRWRT MEMX,SELB                ;WRITE IT TO BR
MICPC=MICPC+1
<MOVEI WRTBRIMEMX:SELB>>
BRSHFTB                        ;SHIFT IT RIGHT
MICPC=MICPC+1

```

(1) 017656 061620  
1022 017660  
(1) 000557  
(1) 017660 062620  
1023 017662  
(1) 000560  
(1) 017662 116256  
1024 017664  
(1) 000561  
(1) 017664 114704  
1025 017666  
(1) 000562  
(1) 017666 060573  
1026 017670  
(1) 000563  
(1) 017670 115467  
1027 017672  
(1) 000564  
(1) 017672 020400  
(1) 000565  
(1) 017674 063223  
1028 017676  
(1) 000566  
(1) 017676 060610  
1034 017700  
(1) 000567  
(1) 017700 062212  
1036 017702  
(1) 000570  
(1) 017702 0201620  
1037 017704  
(1) 000571  
(1) 017704 107177  
1038 017706  
(1) 000572  
(1) 017706 010162  
1039 017710  
(1) 000573  
(1) 017710 054373  
1040 017712  
(1) 000574  
(1) 017712 115411  
1041 017714  
(1) 000575  
(1) 017714 054373  
1042 017716  
(1) 000576  
(1) 017716 115445  
1043 017720  
(1) 000577  
(1) 017720 013164  
1044 017722  
(1) 000600  
(1) 017722 054373  
1045 017724  
(1) 000601

```

<MOVEI SHFTBRI<SELB:BR>>
MEM  BR,SELB                  ;UPDATE IT
MICPC=MICPC+1
<MOVEI WRMEMI<SELB>>
BR0   NTHRES                   ;BRANCH IF THRESHOLD EXCEEDED0
MICPC=MICPC+1
<JUMPI BR0CONI<NTHRES-INIT&3000*4>I<NTHRES-INIT&777/2>>
ALWAYS SNAK
MICPC=MICPC+1
<JUMPI ALCONDI<SNAK-INIT&3000*4>I<SNAK-INIT&777/2>>
BRWRT DP,<DECA:SP13>          ;LOAD TYPE RECEIVED--DECREMENTING
MICPC=MICPC+1
<MOVEI WRTBRIBRI<DECA:SP13>>
Z     RHI                      ;IF ALUOUT IS ALL ONES IS NUMBERED MSG
MICPC=MICPC+1
<JUMPI ZCONDI<RHI-INIT&3000*4>I<RHI-INIT&777/2>>
RSTATB RCVA
MICPC=MICPC+1
<MOVEI WRTBRIBRI<RCVA-INIT&777/2>>
MICPC=MICPC+1
<MOVEI SPX1BRI<SELB:SP3>>
BRWRT DP,<SELA:SP10>          ;LOAD LINE STATUS WORD IN BR
MICPC=MICPC+1
<MOVEI WRTBRIBRI<SELA:SP10>>
OUTPUT IMM,<200:ORCVC0>
MICPC=MICPC+1
<MOVEI WROUT:IMM<200:ORCVC0>>
BRSHFT                        ;SHIFT RIGHT
MICPC=MICPC+1
<MOVEI SHFTBRI<WRTBRIBRI>>
BR4   108
MICPC=MICPC+1
<JUMPI BR4CONI<108-INIT&3000*4>I<108-INIT&777/2>>
LDMA  IMM,TYPSTAB              ;ADDRESS TYPE TABLE
MICPC=MICPC+1
<MOVEI LDMA:IMM<TYPSTAB&377>>
CMP   <MEMX:INCMAR>,SP13
MICPC=MICPC+1
<SUBTC:MEMX:INCMAR:SP13>
Z     REP
MICPC=MICPC+1
<JUMPI ZCONDI<REP-INIT&3000*4>I<REP-INIT&777/2>>
CMP   <MEMX:INCMAR>,SP13
MICPC=MICPC+1
<SUBTC:MEMX:INCMAR:SP13>
Z     NAK
MICPC=MICPC+1
LDMA  IMM,TYPSTT              ;SET POINTER TO START TYPE
MICPC=MICPC+1
<MOVEI LDMA:IMM<TYPSTT&377>>
CMP   <MEMX:INCMAR>,SP13
MICPC=MICPC+1
<SUBTC:MEMX:INCMAR:SP13>
Z     START
MICPC=MICPC+1

```



```
(1) 017724 115420 <JUMPIZCOND!<START-INIT&3000*4>!<START-INIT&777/2>>
1046
1047 017726 CMP <MEMX!INCMAR>,SP13 ;STACK TYPE
(1) 000602 MICPC=MICPC+1
(1) 017726 054373 <SUBTC!MEMX!INCMAR!SP13>
1048 017730 Z STACK
(1) 000603 MICPC=MICPC+1
(1) 017730 115432 <JUMPIZCOND!<STACK-INIT&3000*4>!<STACK-INIT&777/2>>
1049 017732 CMP <MEMX!INCMAR>,SP13 ;ACK TYPE
(1) 000604 MICPC=MICPC+1
1050 017734 <SUBTC!MEMX!INCMAR!SP13>
(1) 000605 Z ACK
(1) 017734 101746 MICPC=MICPC+1
(1) 017736 <JUMPIZCOND!<ACK-INIT&3000*4>!<ACK-INIT&777/2>>
1051 017736 ALWAYS IDLE ;OTHERWISE IGNORE--MUST BE OBS MSG
(1) 000606 MICPC=MICPC+1
(1) 017736 100451 <JUMPIALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
```

```
1065 ;*****TIME CRITICAL CODE-- CHANGE WITH GREAT CARE*****
1066 .SBTTL RCVK01--ROUTINE TO HANDLE FIRST BYTE ODD RECEIVE
1067 017740 RCVK01: SPBR IBUS,NPR,SP0 ;READ NPR REGISTER
(1) 000607 MICPC=MICPC+1
(1) 017740 123000 <MOVE!SPBR!IBUS!NPR!SP0>
1068 017742 BR0 IDLE
(1) 000610 MICPC=MICPC+1
(1) 017742 102051 <JUMPIBR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
1069 017744 BRWRT IMM,200 ;MASK FOR C0(BYTE TRANSFER)
(1) 000611 MICPC=MICPC+1
(1) 017744 000600 <MOVE!WRTEBR!IMM!<200>>
1071 017746 SP BR,AORB,SP0
(1) 000612 MICPC=MICPC+1
(1) 017746 063300 <MOVE!SPX!BR!AORB!SP0>
1076 017750 STATE RKE1
(1) 000613 MICPC=MICPC+1
(1) 017750 000653 <MOVE!WRTEBR!IMM!<RKE1-INIT&777/2>>
1077 017752 ALWAYS RCVK02
(1) 000614 MICPC=MICPC+1
(1) 017752 104620 <JUMPIALCOND!<RCVK02-INIT&3000*4>!<RCVK02-INIT&777/2>>
1078 .SBTTL RCVK0--PROCESS ODD CHARACTER
1079 017754 RCVK0: SPBR IBUS,NPR,SP0 ;IS AN NPR GOING
(1) 000615 MICPC=MICPC+1
(1) 017754 123000 <MOVE!SPBR!IBUS!NPR!SP0>
1081 017756 BR0 RK66 ;IF SO, REITERATE ODD AND EXIT
(1) 000616 MICPC=MICPC+1
(1) 017756 106247 <JUMPIBR0CON!<RK66-INIT&3000*4>!<RK66-INIT&777/2>>
1086 017760 STATE RCVKE
(1) 000617 MICPC=MICPC+1
(1) 017760 000625 <MOVE!WRTEBR!IMM!<RCVKE-INIT&777/2>>
1087 017762 RCVK02: SP BR,SELB,SP3 ;SET STATE
(1) 000620 MICPC=MICPC+1
(1) 017762 063223 <MOVE!SPX!BR!SELB!SP3>
1088 017764 OUTPUT IBUS,RCVDAT!OUTDA2 ;OUTPUT A CHAR
(1) 000621 MICPC=MICPC+1
(1) 017764 022203 <MOVE!WROUT!IBUS!<RCVDAT!OUTDA2>>
1089 017766 RR0: BRWRT IMM,21 ;SET OUT NPR (C1) AND NPR REQ
(1) 000622 MICPC=MICPC+1
(1) 017766 000421 <MOVE!WRTEBR!IMM!<21>>
1093 017770 RK7: OUT BR,<AORB!ONPR> ;WRITE NPR REGISTER
(1) 000623 MICPC=MICPC+1
(1) 017770 001310 <MOVE!WROUT!BR!<AORB!ONPR>>
1094 017772 ALWAYS IDLE
(1) 000624 MICPC=MICPC+1
(1) 017772 100451 <JUMPIALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
```

```

1096
1097 017774
(1) 017774 000625
(1) 017774 120000
1099 017776
(1) 017776 000626
(1) 017776 107251
1104 020000
(1) 020000 000627
(1) 020000 023140
1105 020002
(1) 020002 000630
(1) 020002 062066
1106 020004
(1) 020004 000631
(1) 020004 063164
1107 020006
(1) 020006 000632
(1) 020006 105235
1108 020010
(1) 020010 000633
(1) 020010 063165
1109 020012
(1) 020012 000634
(1) 020012 105711
1110 020014
(1) 020014 000635
(1) 020014 022202
1111 020016
(1) 020016 000636
(1) 020016 023140
1112 020020
(1) 020020 000637
(1) 020020 062066
1113 020022
(1) 020022 000640
(1) 020022 115035
1114 020024
(1) 020024 000641
(1) 020024 063164
1115 020026
(1) 020026 000642
(1) 020026 105245
1116 020030
(1) 020030 000643
(1) 020030 063165
1117 020032
(1) 020032 000644
(1) 020032 111772
1119 020034
(1) 020034 000645
(1) 020034 020040
1120 020036
(1) 020036 000646
(1) 020036 107215
1121 020040
RCVKE: SBTTL RCVKE--HANDLE EVEN BYTES
BRWRT IBUS,NPR ;READ NPR CONTROL REGISTER
MICPC=MICPC+1
<MOVEIWBREBRI<NPR>>
BR4 Rk4 ;IF RECV NPR--BRANCH
MICPC=MICPC+1
<JUMPIBRACONDI<Rk4-INIT63000*4>!<Rk4-INIT6777/2>>
RK5: SP IBUS,IOBA1,SP0 ;READ LOW BYTE OF BA TO SP
MICPC=MICPC+1
<MOVEISPX:IBUS:IOBA1:SP0>
OUTPUT DP,<INCA:IOBA1> ;WRITE INCREMENTED BA
MICPC=MICPC+1
<MOVEIWROUT:DP:<INCA:IOBA1>>
RK50: SP BR,DECA,SP4 ;DECREMENT CHARACTER COUNT
MICPC=MICPC+1
<MOVEISPX:IBR:DECA:SP4>
C 105 ;NO OVERFLOW
MICPC=MICPC+1
<JUMPICCONDI<105-INIT63000*4>!<105-INIT6777/2>>
SP BR,DECA,SP5 ;OVERFLOW - DECREMENT HIGH BYTE
MICPC=MICPC+1
<MOVEISPX:IBR:DECA:SP5>
Z RL3 ;BYTE COUNT ZERO
MICPC=MICPC+1
<JUMPIZCONDI<RL3-INIT63000*4>!<RL3-INIT6777/2>>
106: OUTPUT IBUS,<RCVDAT:IOUDA1> ;READ CHARACTER AND WRITE IT
MICPC=MICPC+1
<MOVEIWROUT:IBUS:<RCVDAT:IOUDA1>>
SP IBUS,IOBA1,SP0 ;READ INCREMENTED BA
MICPC=MICPC+1
<MOVEISPX:IBUS:IOBA1:SP0>
OUTPUT DP,<INCA:IOBA1> ;WRITE INCREMENTED BA
MICPC=MICPC+1
<MOVEIWROUT:DP:<INCA:IOBA1>>
C ICBA22 ;IF CARRY INC BA HIGH
MICPC=MICPC+1
<JUMPICCONDI<ICBA22-INIT63000*4>!<ICBA22-INIT6777/2>>
RK3: SP BR,DECA,SP4 ;DECREMENT THE COUNT OF BYTES
MICPC=MICPC+1
<MOVEISPX:IBR:DECA:SP4>
C Rk6 ;NO OVERFLOW
MICPC=MICPC+1
<JUMPICCONDI<Rk6-INIT63000*4>!<Rk6-INIT6777/2>>
SP BR,DECA,SP5 ;DECREMENT HIGH BYTE OF COUNT
MICPC=MICPC+1
<MOVEISPX:IBR:DECA:SP5>
Z RL4 ;BYTE COUNT ZERO
MICPC=MICPC+1
<JUMPIZCONDI<RL4-INIT63000*4>!<RL4-INIT6777/2>>
RK6: BRWRT IBUS,RCVCON ;READ RECEIVER CONTROL REGISTER
MICPC=MICPC+1
<MOVEIWBREBRI<RCVCON>>
BR4 RCVKO ;IF ANOTHER CHARACTER--PROCESS
MICPC=MICPC+1
<JUMPIBRACONDI<RCVCO-INIT63000*4>!<RCVCO-INIT6777/2>>
RK66: STATE RCVKO

```

```

(1) 000647
(1) 020040 000615
1122 020042
(1) 000650
(1) 020042 100450
1123 020044
(1) 000651
(1) 020044 107251
1124 020046
(1) 000652
(1) 020046 104627
1130
1131 020050
(1) 000653
(1) 020050 123200
1133 020052
(1) 000654
(1) 020052 102251
1135 020054
(1) 000655
(1) 020054 000577
1136 020056
(1) 000656
(1) 020056 061270
1137 020060
(1) 000657
(1) 020060 104631
1138
1139
1140 020062
(1) 000660
(1) 020062 023200
1141 020064
(1) 000661
(1) 020064 062202
1142 020066
(1) 000662
(1) 020066 060001
1143 020070
(1) 000663
(1) 020070 117576
1144 020072
(1) 000664
(1) 020072 104641
MICPC=MICPC+1
<MOVEIWBREBRI<IMM:<RCVCO-INIT6777/2>>
ALWAYS REXIT
MICPC=MICPC+1
<JUMPIALCONDI<REXIT-INIT63000*4>!<REXIT-INIT6777/2>>
RK4: BR0 IDLE
MICPC=MICPC+1
<JUMPIBR0CONDI<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>
ALWAYS RK5 ;IF NO NPR --PROCESS
MICPC=MICPC+1
<JUMPIALCONDI<RK5-INIT63000*4>!<RK5-INIT6777/2>>
RKE1: SP IBUS,NPR,SP0 ;READ NPR REGISTER
MICPC=MICPC+1
<MOVEISPX:IBUS:NPR:SP0>
BR0 IDLE ;NPR STILL IN PROGRESS
MICPC=MICPC+1
<JUMPIBR0CONDI<IDLE-INIT63000*4>!<IDLE-INIT6777/2>>
BRWRT IMM,177 ;MASK FOR ALL BUT C0
MICPC=MICPC+1
<MOVEIWBREBRI<IMM:<177>>
OUT BR,<AANDB:IONPR> ;TURN OFF ALL BUT C0
MICPC=MICPC+1
<MOVEIWROUT:IBR:<AANDB:IONPR>>
ALWAYS RK50
MICPC=MICPC+1
<JUMPIALCONDI<RK50-INIT63000*4>!<RK50-INIT6777/2>>
;*****END OF TIME CRITICAL PATH*****
RCVKE0: SP IBUS,RCVDAT,SP0 ;READ CHARACTER AND SAVE IN SP0
MICPC=MICPC+1
<MOVEISPX:IBUS:RCVDAT:SP0>
OUTPUT BR,<SELA:IOUDA1> ;SEND NONSENSE CHARACTER
MICPC=MICPC+1
<MOVEIWROUT:IBR:<SELA:IOUDA1>>
BRWRT BR,SELA:SP1 ;READ STATUS BYTE
MICPC=MICPC+1
<MOVEIWBREBRI<IBR:<SELA:SP1>>
BR7 PASWRD ;MAINT MODE - SEE IF RLD MESSAGE
MICPC=MICPC+1
<JUMPIBR7CONDI<PASWRD-INIT63000*4>!<PASWRD-INIT6777/2>>
ALWAYS RK3 ;OTHERWISE PROCESS NORMALLY
MICPC=MICPC+1
<JUMPIALCONDI<RK3-INIT63000*4>!<RK3-INIT6777/2>>

```

1146  
1147 020074 000665  
(1) 020074 073213  
1148 020076 000666  
(1) 020076 000670  
1149 020100 000667  
(1) 020100 100450  
1150

```
.SBTTL RCVI--STORE UNNUMBERED MESSAGE TYPE
RCVI:  SP      IBUS,RCVDAT,SP13      ;STORE UNNUMBERED TYPE
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!RCVDAT!SP13>
      STATE  RCVJ      ;NEXT STATE IS J
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<RCVJ-INIT&777/2>>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
      ;
```

1152  
1153 020102  
1158 020102 000670  
(1) 020102 023205  
1159 020104 000671  
(1) 020104 000600  
1160 020106 000672  
(1) 020106 000665  
1161 020110 000673  
(1) 020110 003310  
1163 020112 000674  
(1) 020112 000676  
1164 020114 000675  
(1) 020114 100450

```
.SBTTL RCVJ--ROUTINE TO HANDLE SUBTYPE FIELD,SELECT AND FINAL
RCVJ:  SP      IBUS,RCVDAT,SP5      ;GET CHARACTER
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!RCVDAT!SP5>
      BRWRE  IMM,200      ;CONDITIONALLY SET BIT
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<200>>
      BRWRE  BR,AANDB!SP5
      MICPC=MICPC+1
      <MOVE!WRTEBR!BRI!<AANDB!SP5>>
      SP      BR,AORB,SP10
      MICPC=MICPC+1
      <MOVE!SPX!BRI!AORB!SP10>
      STATE  RCVR      ;NEXT STATE IS N
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<RCVJ-INIT&777/2>>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
      ;
```

1166  
1167  
1168  
1169 020116 000676  
(1) 020116 000403  
1170 020120 000677  
(1) 020120 060353  
1171 020122 000700  
(1) 020122 000703  
1172  
1173 020124  
(1) 000701  
(1) 020124 105131  
1174 020126  
(1) 000702  
(1) 020126 104473

```
.SBTTL RCVR--UNNUMBERED MESSAGE RESPONSE FIELD
;ENTERED FROM IDLE LOOP
;
RCVR: BRWRTI IMM,3 ;REP MESSAGE TYPE TO BR
      MICPC=MICPC+1
      <MOVE!WRTEBRIIMM1<3>>
      NOP BR,SUB,SP13 ;IS TYPE ACK OR NAK
      MICPC=MICPC+1
      <BRISUB!SP13>
      STATE RCVO ;NEXT STATE IS RCVO
      MICPC=MICPC+1
      <MOVE!WRTEBRIIMM1<RCVO-INIT6777/2>>
      ;**NOTE THIS INSTR DOES NOT CLOCK "C"
      ;IF NOT IGNORE
      C RCVF1
      MICPC=MICPC+1
      <JUMPICOND!<RCVF1-INIT63000*4>!<RCVF1-INIT6777/2>>
      ALWAYS RD2 ;DO RANGE CHECKS
      MICPC=MICPC+1
      <JUMPIALCOND!<RD2-INIT63000*4>!<RD2-INIT6777/2>>
```

1176  
1177  
1178  
1179 020130 000703  
(1) 020130 000525  
1180 020132 000704  
(1) 020132 104531

```
.SBTTL RCVO--UNNUMBERED MESSAGE--NUMBER FIELD
;ENTER FROM IDLE
;
RCVO: STATE RCVF ;NEXT STATE IS ADDRESS
      MICPC=MICPC+1
      <MOVE!WRTEBRIIMM1<RCVF-INIT6777/2>>
      ALWAYS RCVF1
      MICPC=MICPC+1
      <JUMPIALCOND!<RCVF1-INIT63000*4>!<RCVF1-INIT6777/2>>
```

```

1182      .SBTTL RCVL--PROCESS CRC3
1183      ;ENTERED FROM IDLE LOOP
1184      RCVL: SPBR IBUS,NPR,SP0      ;READ NPR CONTROL
           MICPC=MICPC+1
           <MOVE!SPBR!IBUS!NPR!SP0>
           BR4 RL1      ;RCV NPR BRANCH
           MICPC=MICPC+1
           <JUMP!BR4CON!<RL1-INIT&3000*4>!<RL1-INIT&777/2>>
1191      RL2: BRWRT IMM,176      ;MASK TO TURN OFF C0
           MICPC=MICPC+1
           <MOVE!WRTBR!IMM!<176>>
           OUT BR,AAANDBI0NPR
           MICPC=MICPC+1
           <MOVE!WROUTX!BR!<AAANDBI0NPR>>
1193      ;
1194      RL3: NOP IBUS,RCV DAT,0      ;INPUT CHARACTER AND DISCARD
           MICPC=MICPC+1
           <IBUS!RCV DAT!0>
           STATE RCVM
           MICPC=MICPC+1
           <MOVE!WRTBR!IMM!<RCVM-INIT&777/2>>
1195      ALWAYS REXIT
           MICPC=MICPC+1
           <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
1197      ;
1199      RL1: BR0 IDLE      ;NPR GOING --GET OUT
           MICPC=MICPC+1
           <JUMP!BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
           ALWAYS RL2
           MICPC=MICPC+1
           <JUMP!ALCOND!<RL2-INIT&3000*4>!<RL2-INIT&777/2>>
           ;
1200      ;
1201      ;
1202      ;

```

```

1204      .SBTTL RCVM--PROCESS CRC4--END OF DATA MESSAGE
1205      ;ENTERED FROM IDLE LOOP
1206      ;IF CRC CORRECT -- QUEUE INTERRUPT AND UPDATE RESPONSE
1207      ;
1208      ;IF CRC WRONG SEND NAK
1209      RCVM: BRWRT IBUS,UBRR      ;READ UNIBUS BR REGISTER
           MICPC=MICPC+1
           <MOVE!WRTBR!IBUS!<UBRR>>
           BR0 NXMERR      ;NON-EXISTANT MEMORY
           MICPC=MICPC+1
           <JUMP!BR0CON!<NXMERR-INIT&3000*4>!<NXMERR-INIT&777/2>>
           SP IBUS,RCV DAT,SP0      ;READ CRC CHARACTER
           MICPC=MICPC+1
           <MOVE!SP!IBUS!RCV DAT!SP0>
           BRWRT IBUS,RCV COM      ;READ RECEIVER CONTROL REGISTER
           MICPC=MICPC+1
           <MOVE!WRTBR!IBUS!<RCV COM>>
           BR0 RCVM1      ;IF CRC GOOD -- PROCESS
           MICPC=MICPC+1
           <JUMP!BR0CON!<RCVM1-INIT&3000*4>!<RCVM1-INIT&777/2>>
           BRWRT BR,SELAI SP1      ;READ STATUS BYTE
           MICPC=MICPC+1
           <MOVE!WRTBR!BR!<SELAI SP1>>
           BR7 RHX      ;CRC ERROR IN BOOT MODE - FLUSH
           MICPC=MICPC+1
           <JUMP!BR7CON!<RHX-INIT&3000*4>!<RHX-INIT&777/2>>
           LDMA IMM,1      ;ELSE SEND NAK --DATA ERROR
           MICPC=MICPC+1
           <MOVE!LDMA!IMM!<T&377>>
           MEMINC IMM,2      ;NAK TYPE
           MICPC=MICPC+1
           <MOVE!WRMEM!INCHAR!IMM!<2>>
           MEMINC IMM,302      ;DATA ERROR SUBTYPE
           MICPC=MICPC+1
           <MOVE!WRMEM!INCHAR!IMM!<302>>
           LDMA IMM,NDATS
           MICPC=MICPC+1
           <MOVE!LDMA!IMM!<NDATS&377>>
           ALWAYS RRS      ;SEND NAK
           MICPC=MICPC+1
           <JUMP!ALCOND!<RRS-INIT&3000*4>!<RRS-INIT&777/2>>
           ;
1221      ;
1222      RCVM0: LDMA IMM,<<RTHRS+3>>      ;POINT TO ERROR WORD
           MICPC=MICPC+1
           <MOVE!LDMA!IMM!<<RTHRS+3>&377>>
           BRWRT IMM,10      ;MAINT MESSAGE ERROR
           MICPC=MICPC+1
           <MOVE!WRTBR!IMM!<10>>
           ALWAYS RCEXY      ;GIVE FATAL ERROR
           MICPC=MICPC+1
           <JUMP!ALCOND!<RCEXY-INIT&3000*4>!<RCEXY-INIT&777/2>>
           ;
1223      ;
1224      ;
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1226      ;
1227      ;
1228      ;
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1231      ;
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1500      ;

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1226  
1227  
1228  
1229  
1230 #20214  
(1) 000735  
(1) #20214 020000  
1231 #20216  
(1) 000736  
(1) #20216 060373  
1232 #20220  
(1) #00737  
(1) #20220 105746  
1233  
1234 #20222  
(1) 000740  
(1) #20222 060521  
1235 #20224  
(1) 000741  
(1) #20224 107343  
1236 #20226  
(1) 000742  
(1) #20226 104415  
1237 #20230  
(1) 000743  
(1) #20230 000563  
1238 #20232  
(1) 000744  
(1) #20232 063261  
1239 #20234  
(1) 000745  
(1) #20234 104415  
1240  
1241 #20236  
(1) 000746  
(1) #20236 063164  
1242 #20240  
(1) 000747  
(1) #20240 115712  
1243 #20242  
(1) 000750  
(1) #20242 104451

```

.SBTTL EM2--PROCESS RLD MESSAGE
;ENTERED FROM IDLE LOOP
;IF RLD PASSWORD CHECKS TRIGGER THE BOOT ROM

EM2: BRWRT# IBUS,RCVDAT          ;READ THE CHAR
      MICPC=MICPC+1
      <MOVE!WRT#BRI!IBUS!<RCVDAT>>
      CMP BR,SP13              ;IS IT A MATCH
      MICPC=MICPC+1
      <SUBT!BRI!SP13>
      Z LM3
      MICPC=MICPC+1
      <JUMP!ZCOND1<EM3-INIT&3000*4>!<EM3-INIT&777/2>>

RHX: BRWRT# BR,AA!SP1          ;FALL INTO RHX
      MICPC=MICPC+1            ;READ STATUS BYTE SHIFTED LEFT
      <MOVE!WRT#BRI!BRI!<AA!SP1>>
      BR4 106                  ;DLE RECEIVED IN NORMAL MODE
      MICPC=MICPC+1
      <JUMP!BR4CON1<106-INIT&3000*4>!<106-INIT&777/2>>
      ALWAYS FLUSH            ;ALREADY IN MAINT MODE
      MICPC=MICPC+1
      <JUMP!ALCOND1<FLUSH-INIT&3000*4>!<FLUSH-INIT&777/2>>

106: BRWRT# IMM,163            ;MASK TO CLEAR ALL MAINT RELATED BITS
      MICPC=MICPC+1
      <MOVE!WRT#BRI!IMM!<163>>
      SP BR,AA&NB,SP1         ;CLEAR THEM
      MICPC=MICPC+1
      <MOVE!SPX!BRI!AA&NB!SP1>
      ALWAYS FLUSH
      MICPC=MICPC+1
      <JUMP!ALCOND1<FLUSH-INIT&3000*4>!<FLUSH-INIT&777/2>>

EM3: SP BR,DECA,SP4           ;DECREMENT CHARACTER COUNT BY ONE
      MICPC=MICPC+1
      <MOVE!SPX!BRI!DECA!SP4>
      Z EMTRIG                 ;TRIGGER AC LOW
      MICPC=MICPC+1
      <JUMP!ZCOND1<EMTRIG-INIT&3000*4>!<EMTRIG-INIT&777/2>>
      ALWAYS IDLE
      MICPC=MICPC+1
      <JUMP!ALCOND1<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

```

1246  
1247 #20244  
(1) 000751  
(1) #20244 210177  
1248 #20246  
(1) 000752  
(1) #20246 016401  
1249 #20250  
(1) 000753  
(1) #20250 002400  
1250 #20252  
(1) 000754  
(1) #20252 043230  
1251 #20254  
(1) 000755  
(1) #20254 114524

```

.SBTTL NXMERR ---NON EXISTANT MEMORY HANDLER
NXMERR: LDMA IMM,<<RTHRS+3>> ;ADDRESS ERROR LINK
        MICPC=MICPC+1
        <MOVE!LDMA!IMM!<<RTHRS+3>>6377>>
        MEMINC IMM,1
        MICPC=MICPC+1
        <MOVE!WRT#MEM!INCMA!IMM!<1>>
        MEM IMM,0              ;NXM ERROR BIT
        MICPC=MICPC+1
        <MOVE!WRT#MEM!IMM!<0>>
        SP MEMX,SELB,SP10     ;CLEAR STATUS
        MICPC=MICPC+1
        <MOVE!SPX!MEMX!SELB!SP10>
        ALWAYS RCEXX
        MICPC=MICPC+1
        <JUMP!ALCOND1<RCEXX-INIT&3000*4>!<RCEXX-INIT&777/2>>

```

1273  
 1274 020256 000756  
 (1) 020256 060601  
 1275 020263 000757  
 (1) 020260 103742  
 1276 020262 000760  
 (1) 020262 000610  
 1277 020264 000761  
 (1) 020264 063301  
 1278 020266 000762  
 (1) 020266 100742  
 1279 020270 000763  
 (1) 020270 000404  
 1280 020272 000764  
 (1) 020272 063000  
 1281 020274 000765  
 (1) 020274 110601  
 1282 020276 000766  
 (1) 020276 000404  
 1283 020300 000767  
 (1) 020300 123220  
 1284 020302 000770  
 (1) 020302 061011  
 1285 020304 000771  
 (1) 020304 114761  
 1286  
 1287 020306 000772  
 (1) 020306 000402  
 1288 020310 000773  
 (1) 020310 114603  
 1291 020312 000774  
 (2) 020312 000000  
 (1) 020314 000775  
 (2) 020314 000000  
 (1) 020316 000776  
 (2) 020316 000000  
 (1) 020318 000777  
 (2) 020320 000000

```

;
BOOT: BRWRT BR, SELAISP1 ;SEE IF IN MAINT. MODE
      MICPC=MICPC+1
      <MOVEI WPTBR I BR I <SELAISP1>>
      BR7 RA3 ;BRANCH IF SO AND TREAT DLE LIKE NUM. MSG.
      MICPC=MICPC+1
      <JUMPI BR7CON I <RA3-INIT&3000*4> I <RA3-INIT&777/2>>
      BRWRT IMM, 210 ;MASK TO SET MAINT MODE AND DLE RCV'D
      MICPC=MICPC+1
      <MOVEI WPTBR I IMM I <210>>
      SP BR, AORB, SP1 ;SET THE BITS
      MICPC=MICPC+1
      <MOVEI SPX I BR I AORB I SP1>
      ALWAYS RA3 ;TREAT LIKE NUMBERED MESSAGE
      MICPC=MICPC+1
      <JUMPI ALCONDI I <RA3-INIT&3000*4> I <RA3-INIT&777/2>>
RESEXT: BRWRT IMM, 4 ;ADD TO MXT BITS
        MICPC=MICPC+1
        <MOVEI WRTBR I IMM I <4>>
        SP BR, ADD, SP0
        MICPC=MICPC+1
        <MOVEI SPX I BR I ADD I SP0>
        ALWAYS TH3X
        MICPC=MICPC+1
        <JUMPI ALCONDI I <TH3X-INIT&3000*4> I <TH3X-INIT&777/2>>
TABMXT: BRWRT IMM, 4 ;INCREMENT MXT
        MICPC=MICPC+1
        <MOVEI WRTBR I IMM I <4>>
        SP IBUS, UBBR, SP0 ;READ BR CONTROL
        MICPC=MICPC+1
        <MOVEI SPX I IBUS I UBBR I SP0>
        OUT BR, ADD I OBR
        MICPC=MICPC+1
        <MOVEI WROUTX I BR I <ADD I OBR>>
        ALWAYS ECX
        MICPC=MICPC+1
        <JUMPI ALCONDI I <ECX-INIT&3000*4> I <ECX-INIT&777/2>>
;
RTHRES: BRWRT IMM, 2
        MICPC=MICPC+1
        <MOVEI WRTBR I IMM I <2>>
        ALWAYS ERRXX
        MICPC=MICPC+1
        <JUMPI ALCONDI I <ERRXX-INIT&3000*4> I <ERRXX-INIT&777/2>>
        ZERO
        MICPC=MICPC+1
        000000
        ZERO
        MICPC=MICPC+1
        000000
        ZERO
        MICPC=MICPC+1
        000000
        ZERO
        MICPC=MICPC+1
        000000
        ZERO
        MICPC=MICPC+1
        000000

```

1293 020322  
 1294 000777  
 1295  
 1296  
 1297 020322 001000  
 (1) 020322 020020  
 1298 020324 001001  
 (1) 020324 173202  
 1299 020326 001002  
 (1) 020326 100454

```

.=INIT+2000
MICPC=777
.SBTTL TMTDA--TRANSMITTER DISPATCH ROUTINE
;
TMTDA: BRWRT IBUS, TMTCON ;READ TRANSMITTER CONTROL REGISTER
        MICPC=MICPC+1
        <MOVEI WRTBR I IBUS I <TMTCON>>
        BR4 DP, SELA, <2 I PAGE2> ;IF READY PROCEED
        MICPC=MICPC+1
        <JUMPI BR4CON I DP I SELA I 2 I PAGE2>
        ALWAYS I1 ;ELSE IDLE
        MICPC=MICPC+1
        <JUMPI ALCONDI I <I1-INIT&3000*4> I <I1-INIT&777/2>>

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```

1301
1302
1303 #20330
1309 #20330
(1) #20330 #20330
(1) #20330 #20332
1310 #20332
(1) #20332 #1004
(1) #20332 #12007
1311 #20334
(1) #20334 #01005
(1) #20334 #01620
1312 #20336
(1) #20336 #01006
(1) #20336 #10063
1318 #20340
(1) #20340 #01007
(1) #20340 #00610
1319 #20342
(1) #20342 #01010
(1) #20342 #13412
1320 #20344
(1) #20344 #01011
(1) #20344 #10054
1321 #20346
(1) #20346 #01012
(1) #20346 #20060
1322 #20350
(1) #20350 #01013
(1) #20350 #01620
1323 #20352
(1) #20352 #01014
(1) #20352 #10054
1324 #20354
(1) #20354 #01015
(1) #20354 #00773
1325 #20356
(1) #20356 #01016
(1) #20356 #03270
1326 #20360
(1) #20360 #01017
(1) #20360 #00424
(1) #20360 #01020
(1) #20362 #03222
1327 #20364
(1) #20364 #01021
(1) #20364 #000412
1328 #20366
(1) #20366 #01022
(1) #20366 #03226
1329 #20370
(1) #20370 #10054
1330 #20372
(1) #20372 #01024
(1) #20372 #03166

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.SBTL TMTA--FIRST CHARACTER OF HEADER
TMTA:
BRWRT BR,SELA:SP10 ;REREAD STATUS
MICPC=MICPC+1
<MOVEIWBTR:BR:SELA:SP10>
BR0 NUMSYN ;IF UNNUMBPENDING -- SEND IT
MICPC=MICPC+1
<JUMPIBROCON:NUMSYN-INIT&3000*4>:NUMSYN-INIT&777/2>
BRSHFT
MICPC=MICPC+1
<MOVEISHT:BR:WRTEBR:SELB>
SP4 IDLE0 ;IF START MODE--EXIT
MICPC=MICPC+1
<JUMPIBROCON:IDLE0-INIT&3000*4>:IDLE0-INIT&777/2>
NUMSYN: BRWRT BR,<SELA:SP10> ;READ LINE STATUS WORD
MICPC=MICPC+1
<MOVEIWBTR:BR:SELA:SP10>
BR7 55 ;IF OK TO SEND--PROCEED
MICPC=MICPC+1
<JUMPIBROCON:55-INIT&3000*4>:55-INIT&777/2>
ALWAYS I1 ;ELSE--IDLE
MICPC=MICPC+1
<JUMPIALCONDI:I1-INIT&3000*4>:I1-INIT&777/2>
55: BRWRT IBUS,MODEM ;ARE WE STILL SENDING?
MICPC=MICPC+1
<MOVEIWBTR:IBUS:MODEM>
BRSHFT
MICPC=MICPC+1
<MOVEISHT:BR:WRTEBR:SELB>
BR4 I1 ;RTS SET? IF SO WE ARE--STALL
MICPC=MICPC+1
<JUMPIBROCON:I1-INIT&3000*4>:I1-INIT&777/2>
BRWRT IMM,373 ;MASK TO TURN OFFLINE IDLE
MICPC=MICPC+1
<MOVEIWBTR:IMM:373>
SP BR,AANDB,SP10 ;IN LINE STATUS WORD
MICPC=MICPC+1
<MOVEIWBTR:IMM:AANDB:SP10>
TSTATE TMTA1
MICPC=MICPC+1
<MOVEIWBTR:IMM:TMTA1-INIT&777/2>
MICPC=MICPC+1
<MOVEIWBTR:IMM:12>
BRWRT IMM,12
MICPC=MICPC+1
<MOVEIWBTR:IMM:12>
SP BR,SELB,SP6 ;STORE IN SP6
MICPC=MICPC+1
<MOVEIWBTR:IMM:SELB:SP6>
ALWAYS I1 ;BACK TO IDLE LOOP
MICPC=MICPC+1
<JUMPIALCONDI:I1-INIT&3000*4>:I1-INIT&777/2>
TMTA1: SP BR,DECA,SP6 ;DECREMENT SYN COUNT
MICPC=MICPC+1
<MOVEIWBTR:IMM:DECA:SP6>

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1331 #20374
(1) #20374 #01025
(1) #20374 #11432
1332 #20376
(1) #20376 #01026
(1) #20376 #02011
1333 #20400
(1) #20400 #01027
(1) #20400 #00626
1334 #20402
(1) #20402 #01030
(1) #20402 #02230
1335 #20404
(1) #20404 #01031
(1) #20404 #10054
1337 #20406
(1) #20406 #01032
(1) #20406 #00610
1338 #20410
(1) #20410 #01033
(1) #20410 #12043
1339 #20412
(1) #20412 #01034
(1) #20412 #00451
(1) #20412 #01035
(1) #20414 #03222
1340 #20416
(1) #20416 #01036
(1) #20416 #00601
1341 #20420
(1) #20420 #01037
(1) #20420 #13447
1342 #20422
(1) #20422 #01038
(1) #20422 #00601
1343 #20424
(1) #20424 #01041
(1) #20424 #02230
1344 #20426
(1) #20426 #01042
(1) #20426 #10054
1345 #20430
(1) #20430 #01043
(1) #20430 #00610
(1) #20432 #01044
(1) #20432 #03222
1346 #20434
(1) #20434 #01045
(1) #20434 #00605
1347 #20436
(1) #20436 #01046
(1) #20436 #10041
1348 #20440
(1) #20440 #01047
(1) #20440 #00620
1349 #20442

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```

Z TMTXT
MICPC=MICPC+1
<JUMPIZCONDI:TMTXT-INIT&3000*4>:TMTXT-INIT&777/2>
OUTPUT IMM,<110TMTCO> ;WRITE SOM TO TMR CONTRL
MICPC=MICPC+1
<MOVEIWBTR:IMM:110TMTCO>
BRWRT IMM,226 ;SYNC CHAR
MICPC=MICPC+1
<MOVEIWBTR:IMM:226>
OUTPUT BR,<SELB:TMTDAT> ;SEND THE CHARACTER
MICPC=MICPC+1
<MOVEIWBTR:IMM:SELB:TMTDAT>
ALWAYS I1
MICPC=MICPC+1
<JUMPIALCONDI:I1-INIT&3000*4>:I1-INIT&777/2>
TMTXT: BRWRT BR,<SELA:SP10> ;UNNUMB MESSAGE?
MICPC=MICPC+1
<MOVEIWBTR:BR:SELA:SP10>
BR0 TMTUN ;IF SO --BRANCH
MICPC=MICPC+1
<JUMPIBROCON:TMTUN-INIT&3000*4>:TMTUN-INIT&777/2>
TSTATE TMTB
MICPC=MICPC+1
<MOVEIWBTR:IMM:TMTB-INIT&777/2>
MICPC=MICPC+1
<MOVEIWBTR:IMM:201> ;ARE WE IN BOOT MODE
BRWRT BR,SELA:SP1
MICPC=MICPC+1
BR7 TMTBT ;IF SO SEND DLE
MICPC=MICPC+1
<JUMPIBROCON:TMTBT-INIT&3000*4>:TMTBT-INIT&777/2>
BRWRT IMM,201 ;ELSE STORE SOM
MICPC=MICPC+1
<MOVEIWBTR:IMM:201>
TMTA5: OUTPUT BR,<SELB:TMTDAT> ;IN TMT SILO
MICPC=MICPC+1
<MOVEIWBTR:IMM:SELB:TMTDAT>
ALWAYS I1
MICPC=MICPC+1
<JUMPIALCONDI:I1-INIT&3000*4>:I1-INIT&777/2>
TMTUN: TSTATE TMTI
MICPC=MICPC+1
<MOVEIWBTR:IMM:TMTI-INIT&777/2>
MICPC=MICPC+1
<MOVEIWBTR:IMM:5> ;END TO BR
BRWRT IMM,5
MICPC=MICPC+1
<MOVEIWBTR:IMM:5>
ALWAYS TMTA5
MICPC=MICPC+1
<JUMPIALCONDI:TMTA5-INIT&3000*4>:TMTA5-INIT&777/2>
TMTBT: BRWRT IMM,220 ;WRITE A DLE TO BR
MICPC=MICPC+1
<MOVEIWBTR:IMM:220>
ALWAYS TMTA5 ;SEND IT

```



(1) #1850  
(1) #20442 112441

MICPC=MICPC+1  
<JUMP:ALCOND1<TMTA5-INIT63000\*4>1<TMTA5-INIT6777/2>>

1373  
1374  
1375 #20444 021051  
(1) #20444 070216  
1376 #20446 001052  
(1) #20446 016403  
1377 #20450 001053  
(1) #20450 076612  
1378 #20452 021054  
(1) #20452 000476  
1379 #20454 001055  
(1) #20454 063222  
1380 #20456 001056  
(1) #20456 056224  
1381 #20460 001057  
(1) #20460 056225  
1382 #20462 001060  
(1) #20462 043227  
1383  
1384 #20464 001061  
(1) #20464 123200  
1385 #20466 001062  
(1) #20466 000620  
1386 #20470 021063  
(1) #20470 063260  
1387 #20472 001064  
(1) #20472 003306  
1388 #20474 001065  
(1) #20474 054666  
1389 #20476 001066  
(1) #20476 042230  
1390 #20500 001067  
(1) #20500 001620  
1391 #20502 001070  
(1) #20502 001620  
1392 #20504 001071  
(1) #20504 041624  
1393 #20506 001072

```

;SFTL TMTB--OUTPUT FIRST CHAR OF COUNT
;
TMTB: LDWA BR, SELA1SP16 ;GET POINTER TO NEXT TMT LINK
      MICPC=MICPC+1
      <MOVE:LDMAR:BR:SELA1SP16>
      MEMINC IMM,3 ;WRITE MSG TMTB TO FLAGS
      MICPC=MICPC+1
      <MOVE:HRMEM:INCMAR:IMM:3>
      MEMINC BR, SELA1SP12 ;PICK UP MSGNO
      MICPC=MICPC+1
      <MOVE:HRMEM:INCMAR:BR:SELA1SP12>
      STATE TMTC ;ADDRESS TMTR STATE
      MICPC=MICPC+1
      <MOVE:WRTEBR:IMM:TMTC-INIT6777/2>
      SP BR, SELB, SP2 ;UPDATE IT
      MICPC=MICPC+1
      <MOVE:SPX:BR:SELB:SP2>
      OUTPUT <MEMX:INCMAR>, SELB:IBA1 ;WRITE LOW BYTE OF ADDRESS
      MICPC=MICPC+1
      <MOVE:WROUT:MEMX:INCMAR:SELB:IBA1>
      OUTPUT <MEMX:INCMAR>, SELB:IBA2 ;WRITE HIGH BYTE OF ADDRESS
      MICPC=MICPC+1
      <MOVE:WROUT:MEMX:INCMAR:SELB:IBA2>
      SP MEMX, SELB, SP7 ;HIGH BYTE OF COUNT TO SP7
      MICPC=MICPC+1
      <MOVE:SPX:MEMX:SELB:SP7>
      ;WAIT TO MASK OFF MEM EXT. BITS
      SP IBUS, NPR, SP0
      MICPC=MICPC+1
      <MOVE:SPX:IBUS:INPR:SP0>
      BRWRT IMM, 220
      MICPC=MICPC+1
      <MOVE:WRTEBR:IMM:220>
      SP BR, AANDB, SP0
      MICPC=MICPC+1
      <MOVE:SPX:BR:AANDB:SP0>
      SP IMM, 300, SP6 ;MASK FOR HXT
      MICPC=MICPC+1
      <MOVE:SPX:IMM:300:SP6>
      BRWRT MEMX:INCMAR, AANDB:SP6 ;TURN OFF CC2
      MICPC=MICPC+1
      <MOVE:WRTEBR:MEMX:INCMAR:AANDB:SP6>
      OUTPUT MEMX, SELB:TMTDAT ;ALSO WRITE COUNT TO TMTR SILO
      MICPC=MICPC+1
      <MOVE:WROUT:MEMX:SELB:TMTDAT>
      BRSHFT ;SHIFT BITS INTO CORRECT POSITION
      MICPC=MICPC+1
      <MOVE:SHFT:BR:WRTEBR:SELB>
      BRSHFT
      MICPC=MICPC+1
      <MOVE:SHFT:BR:WRTEBR:SELB>
      BRSHFT
      MICPC=MICPC+1
      <MOVE:SHFT:BR:WRTEBR:SELB>
      BRSHFT
      MICPC=MICPC+1
      <MOVE:SHFT:BR:WRTEBR:SELB>
      BRSHFT
      MICPC=MICPC+1

```

(1) 020506 001020  
1394 020510 001073  
(1) 020510 001310  
1395 020512 001074  
(1) 020512 043020  
1400 020514 001075  
(1) 020514 100454  
1402

```
<MOVE>SHFTBR<WRITEBR>SELB>  
OUT BR,AORBIONPR  
NICPC=NICPC+1  
<MOVE>WRROUTX<BR><AORBIONPR>  
SPBR MEMX,SELB,SP6 ;LOWBYTE OF COUNT TO SP6  
NICPC=NICPC+1  
<MOVE>SPBRX<MEMX>SELB<SP6>  
ALWAYS I1  
NICPC=NICPC+1  
<JUMP>IALCOND<I1-INIT<3000*4>><I1-INIT<777/2>>  
;
```

1404  
1405  
1406 020516 001076  
(1) 020516 000477  
1407 020520 001077  
(1) 020520 003067  
1408 020522 001100  
(1) 020522 002230  
1409 020524 001101  
(1) 020524 000543  
1410 020526 001102  
(1) 020526 000376  
1411 020530 001103  
(1) 020530 111511  
1412 020532 000406  
(1) 020532 001104  
1413 020534 000406  
(1) 020534 001105  
(1) 020534 003016  
1414 020536  
1420 020536 001106  
(1) 020536 000514  
(1) 020536 001107  
(1) 020540 003222  
1421 020542 001110  
(1) 020542 100454  
1423 020544 001111  
(1) 020544 000471  
1424 020546 001112  
(1) 020546 003236  
1425 020550 001113  
(1) 020550 110506  
1426

```
.SBTTL TMTB--OUTPUT SECOND CHAR OF COUNT  
;  
TMTB: BRWRITE IMM,77 ;MASK TO CLEAR NXT BITS  
NICPC=NICPC+1  
<MOVE>WRTEBR<IMM><77>  
SPBR BR,AANDB,SP7 ;CLEAR THEM  
NICPC=NICPC+1  
<MOVE>SPBRX<BR><AANDB><SP7>  
OUTPUT DP,<SELB><TMTDAT> ;WRITE TO TMT SILO  
NICPC=NICPC+1  
<MOVE>WRROUT<DP><SELB><TMTDAT>  
BRWRITE IMM,TML8 ;GET WRAPAROUND ADDRESS  
NICPC=NICPC+1  
<MOVE>WRTEBR<IMM><TML8>  
CMP BR,SP16 ;WRAPAORUND  
NICPC=NICPC+1  
<SUBT><BR><SP16>  
Z 100  
NICPC=NICPC+1  
<JUMP>ZCOND<I1-INIT<3000*4>><I1-INIT<777/2>>  
BRWRITE IMM,6 ;OFFSET TO NEXT LINK  
NICPC=NICPC+1  
<MOVE>WRTEBR<IMM><6>  
SP BR,ADD,SP16 ;UPDATE THE POINTER  
NICPC=NICPC+1  
<MOVE>SPX<BR><ADD><SP16>  
50:  
TSTATE TMTD  
NICPC=NICPC+1  
<MOVE>WRTEBR<IMM><TMTD-INIT<777/2>>  
NICPC=NICPC+1  
<MOVE>SPX<BR><SELB><SP2>  
ALWAYS I1 ;***OCTOBER 29, 1976  
NICPC=NICPC+1  
<JUMP>IALCOND<I1-INIT<3000*4>><I1-INIT<777/2>>  
100:  
BRWRITE IMM,TML1 ;GO BACK TO FIRST LINK  
NICPC=NICPC+1  
<MOVE>WRTEBR<IMM><TML1>  
SP BR,SELB,SP16  
NICPC=NICPC+1  
<MOVE>SPX<BR><SELB><SP16>  
ALWAYS 50  
NICPC=NICPC+1  
<JUMP>IALCOND<I1-INIT<3000*4>><I1-INIT<777/2>>  
;
```

1428  
1429 020552 001114  
(1) 020552 000524  
1430 020554 001115  
(1) 020554 003166  
1431 020556 001116  
(1) 020556 111120  
1432 020560 001117  
(1) 020560 003167  
1433 020562 001120  
(1) 020562 010171  
1434 020564 001121  
(1) 020564 042230  
1435 020566 001122  
(1) 020566 003222  
1436 020570 001123  
(1) 020570 100454

```
.SBTTL TMD--RESPONSE FIELD-NUMBERED MESSAGE
STATE TMT
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TMT-INIT&777/2>>
SP BR,DECA,SP6 ;ADJUSRT COUNT FOR TWO'S COMPLEMENT
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP6>
C ID2 ;NO OVERFLOW
MICPC=MICPC+1
<JUMP!CCOND!<TD2-INIT&3000*4>!<TD2-INIT&777/2>>
SP BR,DECA,SP7 ;DECREMENT HIGH BYTE OF COUNT
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP7>
LDMA IMM,ISP11 ;RESP FIELD ADDR TO MAR
MICPC=MICPC+1
<MOVE!DMAR!IMM!<ISP11&377>>
TD2: OUTPUT MEMX,SELB!TMDAT ;WRITE IT TO SILO
MICPC=MICPC+1
<MOVE!WROUT!MEMX!<SELB!TMDAT>>
XEXIT2: SP BR,SELB,SP2
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP2>
ALWAYS I1
MICPC=MICPC+1
<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
```

1438  
1439 020572  
1440 020572 001124  
(1) 020572 123000  
1441 020574 001125  
(1) 020574 102054  
1442 020576 001126  
(1) 020576 000612  
1443 020600 001127  
(1) 020600 002230  
1444 020602 001130  
(1) 020602 000532  
1445 020604 001131  
(1) 020604 110600

```
.SBTTL TMT--NUMBER FIELD--NUMBERED MESSAGE
TMT: SPBR IBUS,NPR,SP0 ;READ NPR CONTROL REGISTER
MICPC=MICPC+1
<MOVE!SPBR!IBUS!NPR!SP0>
SR0 I1 ;BUSY - GET OUT
MICPC=MICPC+1
<JUMP!BRCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
BRWTE BR,SEL1!SP12
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<SEL1!SP12>>
OUTPUT BR,<SELB!TMDAT> ;WRITE IT TO THE SILO
MICPC=MICPC+1
<MOVE!WROUT!BR!<SELB!TMDAT>>
STATE TMTF
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TMTF-INIT&777/2>>
ALWAYS TH3
MICPC=MICPC+1
<JUMP!ALCOND!<TH3-INIT&3000*4>!<TH3-INIT&777/2>>
```

1447  
1448  
1449 020606  
(1) 001132  
(1) 020606 000537  
1450 020610  
(1) 001133  
(1) 020610 063222  
1451 020612  
(1) 001134  
(1) 020612 000401  
1453 020614  
(1) 001135  
(1) 020614 062230  
1454 020616  
(1) 001136  
(1) 020616 100454

```
.SBTTL TMTF--NUMBERED MSG ADDRESS FIELD
?
TMTF: STATE TF1
      MICPC=MICPC+1
      <MOVEIWRITEBRIIMMI<TF1-INIT6777/2>>
TF2:  SP BR,SELB,SP2
      MICPC=MICPC+1
      <MOVEISPIXIBRISELBISP2>
      BRWRT IMM,1 ;LOAD ADDRESS
      MICPC=MICPC+1
TF3:  <MOVEIWRITEBRIIMMI<1>>
      OUTPUT BR,<SELBITMTDAT>
      MICPC=MICPC+1
      <MOVEIWRROUTIBRI<SELBITMTDAT>>
      ALWAYS I1
      MICPC=MICPC+1
      <JUMPIALCONDI<I1-INIT63000+4>I<I1-INIT6777/2>>
```

1460  
1461 020620  
(1) 001137  
(1) 020620 100402  
1462 020622  
(1) 001140  
(1) 020622 062231  
1463 020624  
(1) 001141  
(1) 020624 062230  
1464 020626  
(1) 001142  
(1) 020626 022500  
1465 020630  
(1) 001143  
(1) 020630 112162  
1466 020632  
(1) 001144  
(1) 020632 000546  
1467 020634  
(1) 001145  
(1) 020634 110563

```
.SBTTL TF1-NUMBERED MSG HEADER EOM
TF1: BRWRT IMM,2 ;EOM MASK TO BR
      MICPC=MICPC+1
      <MOVEIWRITEBRIIMMI<2>>
      OUTPUT BR,<SELBIOTMTCO> ;UPDATE TMTF CONTROL REGISTER
      MICPC=MICPC+1
      <MOVEIWRROUTIBRI<SELBIOTMTCO>>
      OUTPUT BR,<SELBITMTDAT> ;OUTPUT A GARBAGE CHAR
      MICPC=MICPC+1
      <MOVEIWRROUTIBRI<SELBITMTDAT>>
      BRWRT IBUS,IIBA1 ;READ LOW ORDER FROM INBA
      MICPC=MICPC+1
      <MOVEIWRITEBRIIBUSI<IIBA1>>
      BRG TMTF1 ;IF ODD BITS--BRANCH
      MICPC=MICPC+1
      <JUMPIBRCONI<TMTF1-INIT63000+4>I<TMTF1-INIT6777/2>>
      STATE TMTF
      MICPC=MICPC+1
      <MOVEIWRITEBRIIMMI<TMTF-INIT6777/2>>
      ALWAYS XEXIT
      MICPC=MICPC+1
      <JUMPIALCONDI<XEXIT-INIT63000+4>I<XEXIT-INIT6777/2>>
```

1469  
1470  
1471  
1472 020636  
(1) 001146  
(1) 020636 123000  
1474 020640  
(1) 001147  
(1) 020640 113151  
1476 020642  
(1) 001150  
(1) 020642 182054  
1477 020644  
(1) 001151  
(1) 020644 022010  
1478 020646  
(1) 001152  
(1) 020646 023100  
1479 020650  
(1) 001153  
(1) 020650 002064  
1480 020652  
(1) 001154  
(1) 020652 063166  
1481 020654  
(1) 001155  
(1) 020654 111160  
1482 020656  
(1) 001156  
(1) 020656 063167  
1483 020660  
(1) 001157  
(1) 020660 115407  
1484 020662  
1486 020662  
(1) 001160  
(1) 020662 020020  
1487 020664  
(1) 001161  
(1) 020664 113165  
1489 020666  
(1) 001162  
(1) 020666 000505  
1494 020670  
(1) 001163  
(1) 020670 063222  
1495 020672  
(1) 001164  
(1) 020672 100454  
1497 020674  
1502 020674  
(1) 001165  
(1) 020674 022030  
1503 020676  
(1) 001166  
(1) 020676 023100

```
*****TIME CRITICAL PATH--MODIFY WITH GREAT CARE
;SBTTL TMT--ROUTINE TO OUTPUT DATA CHARACTERS
;
TMT: SPBR IBUS,NPR,SP0 ;READ NPR CONTROL
      MICPC=MICPC+1
      <MOVE!SPBRX!IBUS!NPR!SP0>
      BR4 5S ;IF RECV NPR --PROCESS
      MICPC=MICPC+1
      <JUMP!BR4CON!<5S-INIT&3000*4>!<5S-INIT&777/2>>
      BR0 I1 ;IF NPR IN PROGRESS --BRANCH
      MICPC=MICPC+1
      <JUMP!BR0CON!<I1-INIT&3000*4>!<I1-INIT&777/2>>
55: OUTPUT IBUS,<INDAT1!TMTDAT> ;WRITE THE EVEN CHAR TO TMT SILO
      MICPC=MICPC+1
      <MOVE!WROUT!IBUS!<INDAT1!TMTDAT>>
      SP IBUS,IIBA1,SP0 ;READ LOW BYTE OF BA TO SP
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!IIBA1!SP0>
      OUTPUT BR,<INCA!IIBA1> ;OUTPUT INCREMENTED BA
      MICPC=MICPC+1
      <MOVE!WROUT!BR!<INCA!IIBA1>>
      SP BR,DECA,SP6 ;DECREMENT CHARACTER COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP6>
      C TH6 ;NO OVERFLOW
      MICPC=MICPC+1
      <JUMP!CCOND!<TH6-INIT&3000*4>!<TH6-INIT&777/2>>
      SP BR,DECA,SP7 ;DECREMENT HIGH BYTE OF COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP7>
      Z HEH1 ;BYTE COUNT ZERO
      MICPC=MICPC+1
      <JUMP!ZCOND!<HEH1-INIT&3000*4>!<HEH1-INIT&777/2>>
TH6: BRWRT IBUS,TMTCON ;READ TMT CONTROL CSR
      MICPC=MICPC+1
      <MOVE!WRTBR!IBUS!<TMTCON>>
      BR4 TH9 ;IF MORE ROOM IN SILO--BRANCH
      MICPC=MICPC+1
      <JUMP!BR4CON!<TH9-INIT&3000*4>!<TH9-INIT&777/2>>
TMTF1: STATE TMT0
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<TMT0-INIT&777/2>>
XEXIT: SP BR,SELB,SP2 ;STORE NEW TRANSMIT STATE
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP2>
      ALWAYS I1
      MICPC=MICPC+1
      <JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
TMT0: OUTPUT IBUS,<INDAT2!TMTDAT> ;ODD CHAR TO SILO
      MICPC=MICPC+1
      <MOVE!WROUT!IBUS!<INDAT2!TMTDAT>>
      SP IBUS,IIBA1,SP0 ;READ LOW BYTE TO BA
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!IIBA1!SP0>
```

1504 020700  
(1) 001167  
(1) 020700 062064  
1505 020702  
(1) 001170  
(1) 020702 113377  
1506 020704  
(1) 001171  
(1) 020704 063166  
1507 020706  
(1) 001172  
(1) 020706 111175  
1508 020710  
(1) 001173  
(1) 020710 063167  
1509 020712  
(1) 001174  
(1) 020712 115407  
1510 020714  
(1) 001175  
(1) 020714 123000  
1512 020716  
(1) 001176  
(1) 020716 112205  
1514 020720  
(1) 001177  
(1) 020720 000546  
1515 020722  
(1) 001200  
(1) 020722 063222  
1516 020724  
(1) 001201  
(1) 020724 000556  
1517 020726  
(1) 001202  
(1) 020726 063260  
1518 020730  
(1) 001203  
(1) 020730 161070  
1519 020732  
(1) 001204  
(1) 020732 100454  
1521 020734  
(1) 001205  
(1) 020734 000575  
(1) 001206  
(1) 020736 063222  
1522 020740  
(1) 001207  
(1) 020740 100454  
1524  
1525

```
OUTPUT BR,<INCA!IIBA1> ;OUTPUT THE INCREMENTED BA
      MICPC=MICPC+1
      <MOVE!WROUT!BR!<INCA!IIBA1>>
      C HOINCH
      MICPC=MICPC+1
      <JUMP!CCOND!<HOINCH-INIT&3000*4>!<HOINCH-INIT&777/2>>
TH8: SP BR,DECA,SP6 ;DECREMENT CHARACTERCOUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP6>
      C TH7 ;NO OVERFLOW
      MICPC=MICPC+1
      <JUMP!CCOND!<TH7-INIT&3000*4>!<TH7-INIT&777/2>>
      SP BR,DECA,SP7 ;DECREMENT HIGH BYTE OF COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP7>
      Z HEH1 ;BYTE COUNT ZERO
      MICPC=MICPC+1
      <JUMP!ZCOND!<HEH1-INIT&3000*4>!<HEH1-INIT&777/2>>
TH7: SPBR IBUS,NPR,SP0 ;READ NPR REGISTER
      MICPC=MICPC+1
      <MOVE!SPBRX!IBUS!NPR!SP0>
      BR0 TH2 ;IF NPR BUSY WAIT TO GO
      MICPC=MICPC+1
      <JUMP!BR0CON!<TH2-INIT&3000*4>!<TH2-INIT&777/2>>
      STATE TMT
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<TMT-INIT&777/2>>
TH3: SP BR,SELB,SP2 ;SAVE TSTATE
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP2>
TH3X: BRWRT IMM,156 ;CLEAR C0 AND C1
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<156>>
      SP BR,AANDB,SP0 ;CLEAR THE BITS
      MICPC=MICPC+1
      <MOVE!SPX!BR!AANDB!SP0>
      OUT BR,<INCA!ONPR>
      MICPC=MICPC+1
      <MOVE!WROUTX!BR!<INCA!ONPR>>
      ALWAYS I1
      MICPC=MICPC+1
      <JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
TH2: TSTATE TH7
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<TH7-INIT&777/2>>
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP2>
      ALWAYS I1
      MICPC=MICPC+1
      <JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
*****END TIME CRITICAL PATH*****
```

1527  
 1528 020742 001210  
 (1) 020742 010151  
 1529 020744 001211  
 (1) 020744 043226  
 1530 020746 001212  
 (1) 020746 002614  
 1531 020750 001213  
 (1) 020750 110521  
 1532  
 1533  
 1534 020752 001214  
 (1) 020752 010152  
 1535 020754 001215  
 (1) 020754 000617  
 1536 020756 001216  
 (1) 020756 110521

```

.SBTL TMTI--SEND UNNUMBERED TYPE FIELD
TMTI: LDMA IMM,T ;ADDRESS OF TYPE FIELD TO MAR
      MICPC=MICPC+1
      <MOVEI,LDMAR,IMM1<T&377>>
      SP MEMX,SELB,SP6 ;COPY IT TO SP6
      MICPC=MICPC+1
      <MOVEISFXIMEMXISELBISP6>
      STATE TMTJ
      MICPC=MICPC+1
      <MOVEI,WRTEBR,IMM1<TMTJ-INIT&777/2>>
      ALWAYS TD3
      MICPC=MICPC+1
      <JUMPI,ALCOND1<TD3-INIT&3000*4>!<TD3-INIT&777/2>>
      ;
.SBTL TMTJ--SEND SUB-TYPE FIELD
TMTJ: LDMA IMM,ST ;ADDRESS OF SUB-TYPE FIELD TO MAR
      MICPC=MICPC+1
      <MOVEI,LDMAR,IMM1<ST&377>>
      STATE TMTK
      MICPC=MICPC+1
      <MOVEI,WRTEBR,IMM1<TMTK-INIT&777/2>>
      ALWAYS TD3
      MICPC=MICPC+1
      <JUMPI,ALCOND1<TD3-INIT&3000*4>!<TD3-INIT&777/2>>
      ;

```

1538  
 1539  
 1540 020760 001217  
 (1) 020760 000403  
 1541 020762 001220  
 (1) 020762 060346  
 1542 020764 001221  
 (1) 020764 000625  
 (1) 020764 001222  
 (1) 020766 060322  
 1543 020770 001223  
 (1) 020770 111232  
 1544 020772 001224  
 (1) 020772 110520  
 1545  
 1546  
 1547 020774 001225  
 (1) 020774 000637  
 (1) 020774 001226  
 (1) 020776 060322  
 1548 021000 001227  
 (1) 021000 000403  
 1549 021002 001230  
 (1) 021002 000366  
 1550 021004 001231  
 (1) 021004 111635  
 1551 021006 001232  
 (1) 021006 000400  
 1556 021010 001233  
 (1) 021010 062230  
 1557 021012 001234  
 (1) 021012 102454  
 1559  
 1560 021014 001235  
 (1) 021014 060572  
 1561 021016 001236  
 (1) 021016 112441  
 1562

```

.SBTL TMTK--OUTPUT RESPONSE FIELD (UNNUMB MSG)
TMTK: BRWRTE IMM,3 ;WRITE A 3 TO BR
      MICPC=MICPC+1
      <MOVEI,WRTEBR,IMM1<3>>
      NOP BR,SUR,SP6 ;IF TYPE LESS THAN 3
      MICPC=MICPC+1
      <BRISUBISP6>
      TSTATE TMTL
      MICPC=MICPC+1
      <MOVEI,WRTEBR,IMM1<TMTL-INIT&777/2>>
      MICPC=MICPC+1
      <MOVEISPXIBRISELBISP2>
      C TMTL0
      MICPC=MICPC+1
      <JUMPI,COND1<TMTL0-INIT&3000*4>!<TMTL0-INIT&777/2>>
      ALWAYS TD2
      MICPC=MICPC+1
      <JUMPI,ALCOND1<TD2-INIT&3000*4>!<TD2-INIT&777/2>>
      ;
.SBTL TMTL--UNNUMB MSG NUMBER FIELD
TMTL: TSTATE TMTM
      MICPC=MICPC+1
      <MOVEI,WRTEBR,IMM1<TMTM-INIT&777/2>>
      MICPC=MICPC+1
      <MOVEISPXIBRISELBISP2>
      BRWRTE IMM,3
      MICPC=MICPC+1
      <MOVEI,WRTEBR,IMM1<3>>
      CMP BR,SP6 ;IS MESSAGE REP
      MICPC=MICPC+1
      <SUBTC,IBRISP6>
      Z TMTL1 ;YES
      MICPC=MICPC+1
      <JUMPI,COND1<TMTL1-INIT&3000*4>!<TMTL1-INIT&777/2>>
      BRWRTE IMM,0 ;ADDRESS CONTNAT OF ZERO
      MICPC=MICPC+1
      <MOVEI,WRTEBR,IMM1<0>>
      OUTPUT BR,<SELB,TMTDAT> ;SEND IT OUT
      MICPC=MICPC+1
      <MOVEI,ROUT,IBRI<SELB,TMTDAT>>
      ALWAYS I1 ;BACK TO IDLE LOOP
      MICPC=MICPC+1
      <JUMPI,ALCOND1<I1-INIT&3000*4>!<I1-INIT&777/2>>
      ;
TMTL1: BRWRTE BR,DECA:SP12 ;WRITE A RESPONSE
      MICPC=MICPC+1
      <MOVEI,WRTEBR,IBRI<DECA:SP12>>
      ALWAYS TMTA5
      MICPC=MICPC+1
      <JUMPI,ALCOND1<TMTA5-INIT&3000*4>!<TMTA5-INIT&777/2>>
      ;

```

1564  
1565 021020  
(1) 001237  
(1) 021020 000041  
1566 021022  
(1) 001240  
(1) 021022 110533  
1567 021024  
(1) 001241  
(1) 021024 000402  
1568 021026  
(1) 001242  
(1) 021026 002231  
1569 021030  
(1) 001243  
(1) 021030 002230  
1570 021032  
(1) 001244  
(1) 021032 000404  
1571 021034  
(1) 001245  
(1) 021034 003710  
1572 021036  
(1) 001246  
(1) 021036 000530  
1573 021040  
(1) 001247  
(1) 021040 113653  
1574 021042  
(1) 001250  
(1) 021042 000776  
1575 021044  
(1) 001251  
(1) 021044 003270  
1576 021046  
(1) 001252  
(1) 021046 110740  
1577 021050  
(1) 001253  
(1) 021050 000576  
1578 021052  
(1) 001254  
(1) 021052 110651

```
.SBTTL TMTM--UNNUMB MSG--STATION ADDRESS
STATE TNEOM
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<TNEOM-INIT&777/2>>
ALWAYS TF2
NICPC=MICPC+1
<JUMPIALCOND1<TF2-INIT&3000*4>1<TF2-INIT&777/2>>
TNEOM: BRWRTI IMM,2 ;END OF MESSAGE TO BR
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<2>>
OUTPUT BR,<SELB10TMTCO>
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<SELB10TMTCO>> ;OUTPUT A GARBAGE CHARACTER
OUTPUT BR,<SELB1TMTDAT>
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<SELB1TMTDAT>> ;SET UP LINE HAS GONE IDLE MASK
BRWRTI IMM,4
NICPC=MICPC+1
SPBR BR,AORB,SP10 ;UPDATE LINE STATUS WORD
NICPC=MICPC+1
<MOVEISPBR:BR:AORB:SP10>
BRWRTI BR,AA:SP10 ;SHIFT STATUS LEFT
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<AA:SP10>>
BR7 108 ;IF HDX SET---BRANCH TO CLEAR OK TO SEND
NICPC=MICPC+1
<JUMPIBR7CON1<108-INIT&3000*4>1<108-INIT&777/2>>
BRWRTI IMM,376 ;MASK TO TURN OFF UNNUMB PENDING
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<376>>
SP BR,AA:ND:SP10 ;MASK TO LINE STATUS WORD
NICPC=MICPC+1
<MOVEISPX:BR:AA:ND:SP10>
ALWAYS TEOM2
NICPC=MICPC+1
<JUMPIALCOND1<TEOM2-INIT&3000*4>1<TEOM2-INIT&777/2>>
TNEOM2: BRWRTI IMM,176 ;CLEAR OK TO SEND AND UNNUMB PENDING
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<176>>
ALWAYS 58
NICPC=MICPC+1
<JUMPIALCOND1<58-INIT&3000*4>1<58-INIT&777/2>>
```

1580  
1581  
1582  
1583 021054  
(1) 001255  
(1) 021054 000577  
1584  
1585  
1586  
1587  
1588 021056  
(1) 001256  
(1) 021056 001271  
1589 021060  
(1) 001257  
(1) 021060 000601  
1590 021062  
(1) 001260  
(1) 021062 102051  
1591 021064  
(1) 001261  
(1) 021064 103451  
1592 021066  
(1) 001262  
(1) 021066 003175  
1593 021070  
(1) 001263  
(1) 021070 111670  
1594 021072  
(1) 001264  
(1) 021072 000010  
1595 021074  
(1) 001265  
(1) 021074 116731  
1596 021076  
(1) 001266  
(1) 021076 116331  
1597 021100  
(1) 001267  
(1) 021100 100451  
1598 021102  
(1) 001270  
1599 021102  
(1) 001270  
(1) 021102 000402  
1600 021104  
(1) 001271  
(1) 021104 003235  
1601 021106  
(1) 001272  
(1) 021106 000001  
1602 021110  
(1) 001273  
(1) 021110 003710  
1603 021112  
(1) 001274  
(1) 021112 001020

```
.SBTTL TIMSRV--TIMEOUT ROUTINE--SENDS REP
;
;ENABLE LSB
TIMSRV: BRWRTI IMM,177 ;MASK OFF BR REQ
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<177>>
;RESET TIMER---SLICK MOVE
;SINCE TIMER IS RESET BY WRITING
;A 1 AND THE EXPIRATION LOOKS
;LIKE 1--VOILA
;AND THE BIT ON
OUT BR,<AANDBIOBR>
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<AANDBIOBR>>
BRWRTI BR,SELA:SP1 ;READ STATUS BYTE
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<SELA:SP1>>
BR0 IDLE
NICPC=MICPC+1
<JUMPIBRCON1<IDLE-INIT&3000*4>1<IDLE-INIT&777/2>>
BR7 IDLE ;IF IN MAINT. MODE DISABLE TIMER
NICPC=MICPC+1
<JUMPIBR7CON1<IDLE-INIT&3000*4>1<IDLE-INIT&777/2>>
SP BR,DECA,SP15 ;DECREMENT THE COUNTER
NICPC=MICPC+1
<MOVEISPX:BR:DECA:SP15>
Z 208 ;IF ALL ONES HAS EXPIRED
NICPC=MICPC+1
<JUMPIZCOND1<208-INIT&3000*4>1<208-INIT&777/2>>
BRWRTI BR,SELA:SP10 ;READ LINE STATUS
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<SELA:SP10>>
BR TABUPD ;NUMBERED MESSAGE IN PROGRESS
NICPC=MICPC+1
<JUMPIBR1CON1<TABUPD-INIT&3000*4>1<TABUPD-INIT&777/2>>
BR0 TABUPD ;UNNUMBMSG IN PROGRESS
NICPC=MICPC+1
<JUMPIBR0CON1<TABUPD-INIT&3000*4>1<TABUPD-INIT&777/2>>
ALWAYS IDLE ;ELSE BACK TO IDLE LOOP
NICPC=MICPC+1
<JUMPIALCOND1<IDLE-INIT&3000*4>1<IDLE-INIT&777/2>>
TIME1:
208: BRWRTI IMM,2 ;
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<2>>
SP BR,SELA,SP15 ;RESET THE TIMER TICK COUNT
NICPC=MICPC+1
<MOVEISPX:BR:SELA:SP15>
BRWRTI IMM,201 ;SEI OK TO SEND AND
NICPC=MICPC+1
<MOVEIWRITEBR:IMM1<201>>
SPBR BR,AORB,SP10 ;UNNUM MSG PENDING
NICPC=MICPC+1
<MOVEISPBR:BR:AORB:SP10>
BR SHFT
NICPC=MICPC+1
<MOVEISHFT:BR:SHFT:SP10>
```

```

1609 021114 BR4 BS1 ;IF IN START MODE--BRANCH
(1) 021114 MICPC=MICPC+1
(1) 021114 <JUMP!BR4CON1<BS1-INIT63000*4>1<BS1-INIT6777/2>>
1610 021116 BRWRTE BR,DECA1SP12 ;GET LAST NUMBER SENT
(1) 021116 MICPC=MICPC+1
(1) 021116 <MOVE!WRTEBRIBRI<DECA1SP12>>
1611 021120 CMP BR,SP17 ;COMPARE TO LAST ACKED
(1) 021120 MICPC=MICPC+1
(1) 021120 <SUBTC!BR1SP17>
1612 021122 Z SNDACK ;IF EQ --SEND ACK
(1) 021122 MICPC=MICPC+1
(1) 021122 <JUMP!ZCOND1<SNDACK-INIT63000*4>1<SNDACK-INIT6777/2>>
1613 021124 LDMA IMM,T ;LOAD ADDRESS OF TYPE FIELD IN UNNUMB SK
(1) 021124 MICPC=MICPC+1
(1) 021124 <MOVE!LDMAR!IMM1<T6377>>
1614 021126 MEMINC IMM,3 ;LOAD REP TYPE
(1) 021126 MICPC=MICPC+1
(1) 021126 <MOVE!WRMEM!INCMAR!IMM1<3>>
1615 021130 MEMINC IMM,300 ;ZERO THE SUB-TYPE
(1) 021130 MICPC=MICPC+1
(1) 021130 <MOVE!WRMEM!INCMAR!IMM1<300>>
1616 021132 LDMA IMM,REPCS ;CUMULATIVE REPS RECD
(1) 021132 MICPC=MICPC+1
(1) 021132 <MOVE!LDMAR!IMM1<REPCS6377>>
1617 021134 SP MEMX,SELB,SP0 ;COPY IT TO SP0
(1) 021134 MICPC=MICPC+1
(1) 021134 <MOVE!SP!MEMX!SELB!SP0>
1618 021136 MEM BR,INCA!SP0 ;INCREMENT IT
(1) 021136 MICPC=MICPC+1
(1) 021136 <MOVE!WRMEM!BR!<INCA!SP0>>
1619 021140 LDMA IMM,REPST ;ADDRESS DYNAMIC REP COUNTER
(1) 021140 MICPC=MICPC+1
(1) 021140 <MOVE!LDMAR!IMM1<REPST6377>>
1620 021142 BRWRTE MEMX,SELB ;COPY IT TO THE BR
(1) 021142 MICPC=MICPC+1
(1) 021142 <MOVE!WRTEBR!MEMX!<SELB>>
1621 021144 BSHFTB
(1) 021144 MICPC=MICPC+1
(1) 021144 <MOVE!SHFTBR!SELB!BR>
1622 021146 MEM BR,SELB
(1) 021146 MICPC=MICPC+1
(1) 021146 <MOVE!WRMEM!BR!<SELB>>
1623 021150 BR0 RTHRES
(1) 021150 MICPC=MICPC+1
(1) 021150 <JUMP!BR0CON1<RTHRES-INIT63000*4>1<RTHRES-INIT6777/2>>
1620 021152 ALWAYS IDLE
(1) 021152 MICPC=MICPC+1
(1) 021152 <JUMP!ALCOND1<IDLE-INIT63000*4>1<IDLE-INIT6777/2>>
1629 .DSABLE LSB
1630 ;

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1632 021154 BRWRTE IBUS,UBBR
(1) 021154 MICPC=MICPC+1
(1) 021154 <MOVE!WRTEBR!IBUS!<UBBR>>
1633 021156 BR0 NXMERR ;NON-EXISTANT MEMORY
(1) 021156 MICPC=MICPC+1
(1) 021156 <JUMP!BR0CON1<NXMERR-INIT63000*4>1<NXMERR-INIT6777/2>>
1634 021160 BRWRTE IMM,2 ;EOM TO BR
(1) 021160 MICPC=MICPC+1
(1) 021160 <MOVE!WRTEBR!IMM1<2>>
1635 021162 OUTPUT BR,<SELB!OTMTCO> ;WRITE TMR CONTROL
(1) 021162 MICPC=MICPC+1
(1) 021162 <MOVE!WROUT!BR!<SELB!OTMTCO>>
1636 021164 OUTPUT BR,<SELB!TMTDAT> ;WRITE GARBAGE DATA
(1) 021164 MICPC=MICPC+1
(1) 021164 <MOVE!WROUT!BR!<SELB!TMTDAT>>
1637 021166 BRWRTE BR,SELA!SP1 ;CHECK FOR BOOT MODE
(1) 021166 MICPC=MICPC+1
(1) 021166 <MOVE!WRTEBR!BR!<SELA!SP1>>
1638 021170 BR7 BTEOM ;---IF SET IS MAINT MSG
(1) 021170 MICPC=MICPC+1
(1) 021170 <JUMP!BR7CON1<BTEOM-INIT63000*4>1<BTEOM-INIT6777/2>>
1639 021172 SP BR,INCA,SP12 ;INCREMENT THE MESSAGE NUMBER
(1) 021172 MICPC=MICPC+1
(1) 021172 <MOVE!SP!BR!INCA!SP12>
1640 021174 LDMA BR,SELA!SP16 ;ADDRESS LAST TMT LINK
(1) 021174 MICPC=MICPC+1
(1) 021174 <MOVE!LDMAR!BR!<SELA!SP16>>
1641 021176 BRWRTE MEMX,SELB
(1) 021176 MICPC=MICPC+1
(1) 021176 <MOVE!WRTEBR!MEMX!<SELB>>
1642 021200 BR0 TEOM2
(1) 021200 MICPC=MICPC+1
(1) 021200 <JUMP!BR0CON1<TEOM2-INIT63000*4>1<TEOM2-INIT6777/2>>
1643 021202 BRWRTE IMM,375 ;TURN OFF MESSAGE PENDING
(1) 021202 MICPC=MICPC+1
(1) 021202 <MOVE!WRTEBR!IMM1<375>>
1644 021204 SPBR BR,AAADB,SP10 ;
(1) 021204 MICPC=MICPC+1
(1) 021204 <MOVE!SPBR!BR!AAADB!SP10>
1645 021206 BR0 TEOM2 ;IF UNNUMB PENDING--GO AWAY
(1) 021206 MICPC=MICPC+1
(1) 021206 <JUMP!BR0CON1<TEOM2-INIT63000*4>1<TEOM2-INIT6777/2>>
1646 .SBTTL SNDACK--ROUTINE TO SEND AN ACK
1647 021210 LDMA IMM,T
(1) 021210 MICPC=MICPC+1
(1) 021210 <MOVE!LDMAR!IMM1<T6377>>
1648 021212 MEMINC IMM,1
(1) 021212 MICPC=MICPC+1
(1) 021212 <MOVE!WRMEM!INCMAR!IMM1<1>>
1649 021214 BRWRTE IMM,5
(1) 021214 MICPC=MICPC+1
(1) 021214 <MOVE!WRTEBR!IMM1<5>>
1650 021216 MEMINC IMM,300
(1) 021216 MICPC=MICPC+1
(1) 021216 <MOVE!WRMEM!INCMAR!IMM1<300>>
1651 021220 SP BR,AADB,SP10

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(1) 001337  
(1) 021220 003310  
1652  
1658 021222  
(1) 001340  
(1) 021222 000403  
(1) 001341  
(1) 021224 003222  
1659 021226  
(1) 001342  
(1) 021226 100454  
1661 021230  
(1) 001343  
(1) 021230 120000  
1662 021232  
(1) 001344  
(1) 021232 102051  
1663 021234  
(1) 001345  
(1) 021234 070004  
1664 021236  
(1) 001346  
(1) 021236 103520  
1665 021240  
(1) 001347  
(1) 021240 030400  
1666 021242  
(1) 001350  
(1) 021242 030420  
1667 021244  
(1) 001351  
(1) 021244 000402  
1668 021246  
(1) 001352  
(1) 021246 003004  
1669 021250  
(1) 001353  
(1) 021250 023100  
1670 021252  
(1) 001354  
(1) 021252 002004  
1671 021254  
(1) 001355  
(1) 021254 023120  
1672 021256  
(1) 001356  
(1) 021256 002105  
1673 021260  
(1) 001357  
(1) 021260 123200  
1674 021262  
(1) 001360  
(1) 021262 105363  
1675 021264  
(1) 001361  
(1) 021264 110001

MICPC=MICPC+1  
<MOVE:SPX:BR:IAORBI:SP10>  
TEOM2: TSTATE TMTA  
MICPC=MICPC+1  
<MOVE:WPTEBRI:IMM1<TMTA-INIT&777/2>>  
MICPC=MICPC+1  
<MOVE:SPX:BR:SELB:SP2>  
ALWAYS I1  
MICPC=MICPC+1  
<JUMPIALCONDI<I1-INIT&3000\*4>I<I1-INIT&777/2>>  
FUDGE: BRWRT IBUS,NPR ;READ NPR CONTROL  
MICPC=MICPC+1  
<MOVE:WRTBRI:IBUS1<NPR>>  
BR0 IDLE ;IF NPR GOING---LEAVE  
MICPC=MICPC+1  
<JUMPIBROCONI<IDLE-INIT&3000\*4>I<IDLE-INIT&777/2>>  
BRWRT BR:LDMAR,SELB:SP4 ;LOAD THE MAR  
MICPC=MICPC+1  
<MOVE:WRTBRI:BR:LDMAR1<SELB:SP4>>  
BR7 BS2 ;IF SET - READ BACK ALL 200  
MICPC=MICPC+1  
<JUMPIB7CONI<BS2-INIT&3000\*4>I<BS2-INIT&777/2>>  
MEMINC IBUS,INDAT1 ;OTHERWISE RESTORE TWO BYTES  
MICPC=MICPC+1  
<MOVE:WRMEM:INCMAR:IBUS1<INDAT1>>  
MEMINC IBUS,INDAT2 ;..  
MICPC=MICPC+1  
<MOVE:WRMEM:INCMAR:IBUS1<INDAT2>>  
BRWRT IMM,2 ;UPDATE---UNIBUS ADDRESS  
MICPC=MICPC+1  
<MOVE:WRTBRI:IMM1<2>>  
SP BR,ADD,SP4 ;UPDATE NPR COUNTER  
MICPC=MICPC+1  
<MOVE:SPX:BR:ADD:SP4>  
SP IBUS,IIBA1,SP0 ;UPDATE ADDRESS LOW  
MICPC=MICPC+1  
<MOVE:SPX:IBUS1:IIBA1:SP0>  
OUTPUT BR,ADD:IIBA1  
MICPC=MICPC+1  
<MOVE:WROUT:BR1<ADD:IIBA1>>  
SP IBUS,IIBA2,SP0 ;READ HIGH ADDRESS  
MICPC=MICPC+1  
<MOVE:SPX:IBUS1:IIBA2:SP0>  
OUTPUT BR,AC:IIBA2 ;UPDATE HIGH  
MICPC=MICPC+1  
<MOVE:WROUT:BR1<AC:IIBA2>>  
SP IBUS,NPR,SP0 ;READ NPR REGISTER  
MICPC=MICPC+1  
<MOVE:SPX:IBUS:NPR:SP0>  
C RESEXT ;IF CARRY---UPDATE MXT  
MICPC=MICPC+1  
<JUMPICONDI<RESEXT-INIT&3000\*4>I<RESEXT-INIT&777/2>>  
ALWAYS TH3X ;GO DO ANOTHER NPR  
MICPC=MICPC+1  
<JUMPIALCONDI<TH3X-INIT&3000\*4>I<TH3X-INIT&777/2>>

1676 021206 001362  
(1) 021266 000774  
1677 021270  
(1) 001363  
(1) 021270 003270  
1678 021272  
(1) 001364  
(1) 021272 003233  
1679  
1680 021274  
(1) 001365  
(1) 021274 010067  
1681 021276  
(1) 001366  
(1) 021276 003220  
1686 021300  
(1) 001367  
(1) 021300 000403  
(1) 001370  
(1) 021302 003222  
1688 021304  
(1) 001371  
(1) 021304 111532  
1689 021306  
(1) 001372  
(1) 021306 000705  
(1) 001373  
(1) 021310 003223  
1690 021312  
(1) 001374  
(1) 021312 123200  
1691 021314  
(1) 001375  
(1) 021314 000021  
1692 021316  
(1) 001376  
(1) 021316 100023  
1693 021320  
(1) 001377  
(1) 021320 023120  
1694 021322  
(1) 001400  
(1) 021322 002065  
1695 021324  
(1) 001401  
(1) 021324 115003  
1696 021326  
(1) 001402  
(1) 021326 110071  
1697  
1698 021330  
(1) 001403  
(1) 021330 123200  
1699 021332  
(1) 001404

BTEOM: BRWRT IMM,374 ;MASK FOR CLEAR MSG PENDING  
MICPC=MICPC+1  
<MOVE:WRTBRI:IMM1<374>>  
SP BR,ANDB,SP10 ;TURN THEM OFF IN LINE STATUS WORD  
MICPC=MICPC+1  
<MOVE:SPX:BR:IAANDB:SP10>  
SP BR,SELB,SP13 ;STORE UNRECOGNIZABLE VALUE INTO SP13  
MICPC=MICPC+1  
<MOVE:SPX:BR:SELB:SP13>  
;SO "RH3" WILL EXIT BACK TO IDLE LOOP  
;ADDRESS START OF TMT CHAIN  
LDMA IMM,STC  
MICPC=MICPC+1  
<MOVE:LDMA:IMM1<STC&377>>  
SP MEMX,SELB,SP0 ;COPY LINK ADDRESS  
MICPC=MICPC+1  
<MOVE:SPX:MEMX:SELB:SP0>  
TSTATE TMTA ;CHANGE XMIT STATE TO LINE IS IDLE  
MICPC=MICPC+1  
<MOVE:WRTBRI:IMM1<TMTA-INIT&777/2>>  
MICPC=MICPC+1  
<MOVE:SPX:BR:SELB:SP2>  
ALWAYS TDON2 ;POST A DONE  
MICPC=MICPC+1  
<JUMPIALCONDI<TDON2-INIT&3000\*4>I<TDON2-INIT&777/2>>  
RL4: RSTATE RCVL  
MICPC=MICPC+1  
<MOVE:WRTBRI:IMM1<RCVL-INIT&777/2>>  
MICPC=MICPC+1  
<MOVE:SPX:BR:SELB:SP3>  
SP IBUS,NPR,SP0 ;READ NPR CONTROL REGISTER  
MICPC=MICPC+1  
<MOVE:SPX:IBUS:NPR:SP0>  
BRWRT IMM,221  
MICPC=MICPC+1  
<MOVE:WRTBRI:IMM1<221>>  
ALWAYS RK7  
MICPC=MICPC+1  
<JUMPIALCONDI<RK7-INIT&3000\*4>I<RK7-INIT&777/2>>  
HOINCH: SP IBUS,IIBA2,SP0  
MICPC=MICPC+1  
<MOVE:SPX:IBUS:IIBA2:SP0>  
OUTPUT BR,INCA:IIBA2 ;OUTPUT INCREMENTED BA  
MICPC=MICPC+1  
<MOVE:WROUT:BR1<INCA:IIBA2>>  
C 55 ;INCREMENT BYTEW COUNT  
MICPC=MICPC+1  
<JUMPICONDI<55-INIT&3000\*4>I<55-INIT&777/2>>  
ALWAYS TH0  
MICPC=MICPC+1  
<JUMPIALCONDI<TH0-INIT&3000\*4>I<TH0-INIT&777/2>>  
;INCREMENT MXT BITS  
55: SP IBUS,NPR,SP0 ;READ NPR REG WITH CURRENT MXT BITS  
MICPC=MICPC+1  
<MOVE:SPX:IBUS:NPR:SP0>  
BRWRT IMM,4 ;WRITE BIT TO ADD  
MICPC=MICPC+1

(1) 021332 001403  
1700 021334  
(1) 001405  
(1) 021334 001010  
1701 021336  
(1) 001406  
(1) 021336 112571  
1702  
1704 021340  
(1) 001407  
(1) 021340 000715  
1705 021342  
(1) 001410  
(1) 021342 110563  
1707

```
<MOVE:WRTEBR:IMM1<4>>  
OUT BR,<ADDITIONPR> ;TURN ON PROPER MIT BITS  
MICPC=MICPC+1  
<MOVE:WROUTX:BR1<ADDITIONPR>>  
ALWAYS TH8  
MICPC=MICPC+1  
<JUMP:ALCOND1<TH8-INIT63000*4>1<TH8-INIT6777/2>>  
;  
HEH1: STATE TEOM  
MICPC=MICPC+1  
<MOVE:WRTEBR:IMM1<TEOM-INIT6777/2>>  
ALWAYS XEXIT  
MICPC=MICPC+1  
<JUMP:ALCOND1<XEXIT-INIT63000*4>1<XEXIT-INIT6777/2>>  
;
```

1713  
1714 021344  
(1) 001411  
(1) 021344 010016  
1715 021346  
(1) 001412  
(1) 021346 043220  
1716 021350  
(1) 001413  
(1) 021350 002460  
1717 021352  
(1) 001414  
(1) 021352 010151  
1718 021354  
(1) 001415  
(1) 021354 016402  
1719 021356  
(1) 001416  
(1) 021356 016703  
1720 021360  
(1) 001417  
(1) 021360 114704  
1721  
1722  
1723 021362  
(1) 001420  
(1) 021362 060010  
1724 021364  
(1) 001421  
(1) 021364 010120  
1725 021366  
(1) 001422  
(1) 021366 117026  
1726  
1727 021370  
(1) 001423  
(1) 021370 010177  
1728 021372  
(1) 001424  
(1) 021372 000000  
1729 021374  
(1) 001425  
(1) 021374 111522  
1730 021376  
(1) 001426  
(1) 021376 010151  
1731 021400  
(1) 001427  
(1) 021400 016407  
1732 021402  
(1) 001430  
(1) 021402 000011  
1733 021404  
(1) 001431  
(1) 021404 110736  
1734

```
.SBTTL REP HANDLER  
REP: LDMA IMM,REPCR ;LOAD MAR ADDRESS WITH POINTER TO REPS RECD  
MICPC=MICPC+1  
<MOVE:LDMAR:IMM1<REPCR6377>>  
SP MEMX,SEL0,SP0 ;READ NUMBER OF REPS RECD  
MICPC=MICPC+1  
<MOVE:SPX:MEMX:SELB:SP0>  
MEM DP,<INCA:SP0> ;INCREMNT REPS RECD  
MICPC=MICPC+1  
<MOVE:INRMEM:DP1<INCA:SP0>>  
LDMA IMM,T ;LOAD ADDRESS OF TYPE FIELD  
MICPC=MICPC+1  
<MOVE:LDMAR:IMM1<T6377>>  
MEMINC IMM,2 ;LOAD NAK TYPE  
MICPC=MICPC+1  
<MOVE:INRMEM:INCMAR:IMM1<2>>  
MEMINC IMM,303 ;LOAD REP RESPONSE SUB-TYPE  
MICPC=MICPC+1  
<MOVE:INRMEM:INCMAR:IMM1<303>>  
ALWAYS SNAK ;SEND AN UNNUMB MSG  
MICPC=MICPC+1  
<JUMP:ALCOND1<SNAK-INIT63000*4>1<SNAK-INIT6777/2>>  
;  
.SBTTL START HANDLER  
START: BRWRT DP,<SEL:ISP10> ;READ LINE STATUS WORD  
MICPC=MICPC+1  
<MOVE:WRTEBR:DP1<SEL:ISP10>>  
BPSHFT ;GET START MODE BIT IN TESTABLE POSITION  
MICPC=MICPC+1  
<MOVE:SHFTBR:WRTEBR:SEL0>  
BR4 100 ;IF IN START MODE SET STACK  
MICPC=MICPC+1  
<JUMP:BP4CON1<100-INIT63000*4>1<100-INIT6777/2>>  
;EL6E SET UP START ERROR  
LDMA IMM,<<RTHR8+3>>  
MICPC=MICPC+1  
<MOVE:LDMAR:IMM1<<RTHR8+3>6377>>  
BRWRT IMM,200  
MICPC=MICPC+1  
<MOVE:WRTEBR:IMM1<200>>  
ALWAYS RCEXY  
MICPC=MICPC+1  
<JUMP:ALCOND1<RCEXY-INIT63000*4>1<RCEXY-INIT6777/2>>  
100: LDMA IMM,T ;SET UP ADDRESS OF TYPE FIELD  
MICPC=MICPC+1  
<MOVE:LDMAR:IMM1<T6377>>  
MEMINC IMM,7 ;WRITE STACK TYPE  
MICPC=MICPC+1  
<MOVE:INRMEM:INCMAR:IMM1<7>>  
BRWRT IMM,11 ;SET START RECD AND UNNUMB PENDING  
MICPC=MICPC+1  
<MOVE:WRTEBR:IMM1<11>>  
ALWAYS SA2 ;SEND THE UNNUMBERED MESSAGE  
MICPC=MICPC+1  
<JUMP:ALCOND1<SA2-INIT63000*4>1<SA2-INIT6777/2>>  
;
```

1735  
1736 J21406 001432  
(1) 021406 000727  
1737 021410 001433  
(1) 021410 003270  
1738 021412 001434  
(1) 021412 110670

STACK: SBTTL STACK HANDLER  
BRWRTB IMM,327 ;MASK TO CLEAR START MODE  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<327>>  
SP BR,AANDB,SP10 ;CLEAR START MODE  
MICPC=MICPC+1  
<MOVE!SPX!BR!AANDB!SP10>  
ALWAYS TIME1 ;RESET TIMER AND IDLE  
MICPC=MICPC+1  
<JUMP!ALCONDI<TIME1-INIT&3000\*4>!<TIME1-INIT&777/2>>

1740 021414 001435  
(1) 021414 023160  
1741 021416 001436  
(1) 021416 002067  
1742 021420 001437  
(1) 021420 115041  
1743 021422 001440  
(1) 021422 104641  
1744  
1745 021424 001441  
(1) 021424 123220  
1746 021426 001442  
(1) 021426 000404  
1747 021430 001443  
(1) 021430 001011  
1748 021432 001444  
(1) 021432 104641  
1753 021434 001445  
(1) 021434 001011  
1754 021436 001446  
(1) 021436 003220  
1755 021440 001447  
(1) 021440 002160  
1756 021442 001450  
(1) 021442 002067  
1757 021444 001451  
(1) 021444 003236  
1758 021446 001452  
(1) 021446 000477  
1759 021450 001453  
(1) 021450 003232  
1760 021452 001454  
(1) 021452 000406  
1761  
1762 021454 001455  
(1) 021454 003310  
1763 021456 001456  
(1) 021456 003235

ICBA22: SP IBUS,IOBA2,SP0 ;READTHEHIGH ORDERBITS OF BA TO SP0  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!IOBA2!SP0>  
OUTPUT DP,<INCA!IOBA2> ;OUTPUT THE INCREMENTED COUNT  
MICPC=MICPC+1  
<MOVE!WROUT!DP!<INCA!IOBA2>>  
C SS ;IF CARRY SET INCREMENT THE NMTBITS  
MICPC=MICPC+1  
<JUMP!ALCONDI<SS-INIT&3000\*4>!<SS-INIT&777/2>>  
ALWAYS RK3  
MICPC=MICPC+1  
<JUMP!ALCONDI<RK3-INIT&3000\*4>!<RK3-INIT&777/2>>  
}  
55: SP IBUS,UBBR,SP0  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!UBBR!SP0>  
BRWRTB IMM,4  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<4>>  
OUT BR,<ADD!OBR>  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<ADD!OBR>>  
ALWAYS RK3  
MICPC=MICPC+1  
<JUMP!ALCONDI<RK3-INIT&3000\*4>!<RK3-INIT&777/2>>  
NAK: LDMA IMM,NDATR ;CUMMULATIVE NAK COUNTER  
MICPC=MICPC+1  
<MOVE!LDHAR!IMM!<NDATR&377>>  
SP MEMX,SELB,SP0 ;READ IT  
MICPC=MICPC+1  
<MOVE!SPX!MEMX!SELB!SP0>  
MEM MEMX,INCA!SP0 ;INCREMENT THE COUNTER  
MICPC=MICPC+1  
<MOVE!WRMEM!MEMX!<INCA!SP0>>  
LDMA IMM,STC ;ADDRESS START OF IMT CHAIN  
MICPC=MICPC+1  
<MOVE!LDHAR!IMM!<STC&377>>  
SP MEMX,SELB,SP16 ;COPY START OF CHAIN TO LAST XMIT POINTER  
MICPC=MICPC+1  
<MOVE!SPX!MEMX!SELB!SP16>  
BRWRTB BR,INCA!SP17 ;GETLASTMESSAGE ACKED  
MICPC=MICPC+1  
<MOVE!WRTEBR!BR!<INCA!SP17>>  
SP BR,SELB,SP12 ;COPY TO CURRENT NUMBER  
MICPC=MICPC+1  
<MOVE!SPX!BR!SELB!SP12>  
BRWRTB IMM,6 ;WRITE NUMBERED MSG PENDING  
MICPC=MICPC+1  
<MOVE!WRTEBR!IMM!<6>>  
SP BR,AORB,SP10 ; AND LINE HAS GONE IDLE  
MICPC=MICPC+1 ;SET IT IN LINE STATUS WORD  
<MOVE!SPX!BR!AORB!SP10>  
SP BR,SELB,SP15 ;RESET TIMER COUNT  
MICPC=MICPC+1  
<MOVE!SPX!BR!SELB!SP15>

```

1764 021460 ALWAYS TEOM1
(1) 021460 001457 MICPC=MICPC+1
(1) 021460 110725 <JUMP:ALCONDI<TEOM1-INIT&3000*4>|<TEOM1-INIT&777/2>>
1765 021462 ININT: BRWRT IMM,15 ;MASK FOR TURN OFF ALL BUT EXT MEM BITS + NXM
(1) 021462 001460 MICPC=MICPC+1
(1) 021462 000415 <MOVE:WRTEBRI:IMM1<15>>
1766 021464 SP IBUS,UBBR,SP0 ;READ BR CONTROL REGISTER
(1) 021464 001461 MICPC=MICPC+1
(1) 021464 123220 <MOVE:SPX:IBUS:UBBR:SP0>
1767 021466 SP BR,ANDB,SP0 ;MASK OFF VECTOR TO X04
(1) 021466 001462 MICPC=MICPC+1
(1) 021466 003260 <MOVE:SPX:IBR:ANDB:SP0>
1768 021470 BRWRT IMM,200 ;MASK FOR INTERRUPT
(1) 021470 001463 MICPC=MICPC+1
(1) 021470 000600 <MOVE:WRTEBRI:IMM1<200>>
1769 021472 OUT BR,AORB:OBR ;INTERRUPT
(1) 021472 001464 MICPC=MICPC+1
(1) 021472 001311 <MOVE:WROUT:IBR:<AORB:OBR>>
1770 021474 SP IBUS,INCON,SP0 ;RESTORE INPUT CONTROL CSK
(1) 021474 001465 MICPC=MICPC+1
(1) 021474 123000 <MOVE:SPX:IBUS:INCON:SP0>
1771 021476 ALWAYS NIDLE4
(1) 021476 001466 MICPC=MICPC+1
(1) 021476 100554 <JUMP:ALCONDI<NIDLE4-INIT&3000*4>|<NIDLE4-INIT&777/2>>
1772 ;

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1783 ;FUGITIVE RECEIVE ROUTINES---DON'T FIT IN PAGE
1784 021500 RH1: BRWRT IMM,77
(1) 021500 001467 MICPC=MICPC+1
(1) 021500 000477 <MOVE:WRTEBRI:IMM1<77>>
1785 021502 SP BR,ANDB,SP5
(1) 021502 001470 MICPC=MICPC+1
(1) 021502 003265 <MOVE:SPX:IBR:ANDB:SP5>
1786 021504 LDMA BR,<INCA:SP14> ;LOAD ADDRESS OF CURRENT COUNT
(1) 021504 001471 MICPC=MICPC+1
(1) 021504 000074 <MOVE:LDMA:BR:<INCA:SP14>>
1787 021506 SP BR:INCMAR,SELB,SP0 ;SAVE MASK
(1) 021506 001472 MICPC=MICPC+1
(1) 021506 007220 <MOVE:SPX:IBR:INCMAR:SELB:SP0>
1788 021510 BRWRT BR:INCMAR,SELA:SP1 ;READ STATUS BYTE
(1) 021510 001473 MICPC=MICPC+1
(1) 021510 004001 <MOVE:WRTEBRI:BR:INCMAR:<SELA:SP1>>
1789 021512 BRSHFT ;SHIFT IT RIGHT
(1) 021512 001474 MICPC=MICPC+1
(1) 021512 001020 <MOVE:SHFT:BR:WRTEBRI:SELB>
1790 021514 BR1 RH2 ;NO BUFFER ASSIGNED IN MAINT MODE
(1) 021514 001475 MICPC=MICPC+1
(1) 021514 116502 <JUMP:BR1:CONI<RH2-INIT&3000*4>|<RH2-INIT&777/2>>
1791 021516 BRWRT MEMX:INCMAR,ANDB:SP0 ;GET HIGH BYTE COUNT BITS
(1) 021516 001476 MICPC=MICPC+1
(1) 021516 004660 <MOVE:WRTEBRI:MEMX:INCMAR:<ANDB:SP0>>
1792 021520 CMP BR,SP5 ;COMPARE HIGH ORDER BITS OF COUNT
(1) 021520 001477 MICPC=MICPC+1
(1) 021520 000365 <SUBTC:BR:SP5>
1793 021522 C RCFATL ;IF CARRY--TOO BIG ERROR
(1) 021522 001500 MICPC=MICPC+1
(1) 021522 115113 <JUMP:ICCOND:<RCFATL-INIT&3000*4>|<RCFATL-INIT&777/2>>
1794 021524 Z RCLOW ;IF EQUAL COMPARE LOW ORDER BITS OF COUNT
(1) 021524 115110 MICPC=MICPC+1
(1) 021524 115110 <JUMP:Z:COND:<RCLOW-INIT&3000*4>|<RCLOW-INIT&777/2>>
1795 021526 RH2: BRWRT IBUS,IOBA1 ;READ LOW BYTE OF IN BA
(1) 021526 001502 MICPC=MICPC+1
(1) 021526 000540 <MOVE:WRTEBRI:IBUS:<IOBA1>>
1796 021530 BR0 RCVODD ;IF SET IS ODD TRANSFER
(1) 021530 001503 MICPC=MICPC+1
(1) 021530 116106 <JUMP:BR0:CONI<RCVODD-INIT&3000*4>|<RCVODD-INIT&777/2>>
1801 021532 STATE RCVKE0
(1) 021532 001504 MICPC=MICPC+1
(1) 021532 000660 <MOVE:WRTEBRI:IMM1<RCVKE0-INIT&777/2>>
1802 021534 ALWAYS REXIT
(1) 021534 001505 MICPC=MICPC+1
(1) 021534 100450 <JUMP:ALCONDI<REXIT-INIT&3000*4>|<REXIT-INIT&777/2>>
1803 ;
1804 RCVODD: STATE RCVK01
(1) 021536 001506 MICPC=MICPC+1
(1) 021536 000037 <MOVE:WRTEBRI:IMM1<RCVK01-INIT&777/2>>
1805 021540 ALWAYS REXIT
(1) 021540 001507 MICPC=MICPC+1
(1) 021540 100450 <JUMP:ALCONDI<REXIT-INIT&3000*4>|<REXIT-INIT&777/2>>
1806 ;
1807 RCLOW: CMP MEMX,SP4 ;COMPARE LOW ORDER BITS OF COUNT
(1) 021542 001511 MICPC=MICPC+1

```

```

(1) 021542 040364
1808 021544
(1) 021544 115113
1809 021546
(1) 021546 114502
1810 021550
(1) 021553 010151
1811 021552
(1) 021554 016402
1812 021554
(1) 021554 0202711
1813 021556
(1) 021560 010175
1814 021560
(1) 021562 036540
1815 021562
(1) 021562 036560
1816 021564
(1) 021564 000420
1817 021566
(1) 021566 016400
1818 021570
(1) 021570 062620
1819 021572
(1) 021572 022212
1820 021574
(1) 021574 003002
1821 021576
(1) 021576 003001
1822 021600
(1) 021600 114666
1823 021602
(1) 021602 040757
1824 021604
(1) 021604 107562
1825 021606
(1) 021606 270200
1826 021610

```

```

<SUBTCI MEMX1SP4>
C RCFATL ;CARRY--TOO BIG
MICPC=MICPC+1
<JUMP:ICOND1<RCFATL-INIT63000*4>1<RCFATL-INIT6777/2>>
ALWAYS RH2 ;ELSE CONTINUE
MICPC=MICPC+1
<JUMP:ALCOND1<RH2-INIT63000*4>1<RH2-INIT6777/2>>
RCFATL: LDMA IMM,T
MICPC=MICPC+1
<MOVE:LDMAR:IMM1<T6377>>
MEMINC IMM,2
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM1<2>>
MEM IMM,311
MICPC=MICPC+1
LDMA IMM,<<RTHRS+1>> ;ADDRESS ERROR LINK
MICPC=MICPC+1
<MOVE:LDMAR:IMM1<<RTHRS+1>6377>>
MEMINC IBUS,IOBA1
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IBUS1<IOBA1>>
MEMINC IBUS,IOBA2
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IBUS1<IOBA2>>
BRWRT IMM,20
MICPC=MICPC+1
<MOVE:WRTEBR:IMM1<20>>
RCEXY: MEMINC IMM,0
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM1<0>>
MEM BR,SELB
MICPC=MICPC+1
<MOVE:WRMEM:BR1<SELB>>
RCEXX: OUTPUT IMM,<2001ORCYCO> ;FLUSH INPUT SILO
MICPC=MICPC+1
<MOVE:WROUT:IMM1<2001ORCYCO>>
SP IMM,SP2,2 ;INHIBIT FURTHER TRANSMISSIONS
MICPC=MICPC+1
<MOVE:SPX:IMM1SP212>
SP IMM,1,SP1 ;SET INIT MODE IN PORT STATUS WORD
MICPC=MICPC+1
<MOVE:SPX:IMM11:SP1>
ALWAYS NTRS1
MICPC=MICPC+1
<JUMP:ALCOND1<NTRS1-INIT63000*4>1<NTRS1-INIT6777/2>>
TDON3: BRWRT MEMX,SUB1SP17 ;COMPARE RESPONSE TO MSG NO
MICPC=MICPC+1
<MOVE:WRTEBR:MEMX1<SUB1SP17>>
BR7 RH3 ;IF NEGATIVE EXIT
MICPC=MICPC+1
<JUMP:BR7CON1<RH3-INIT63000*4>1<RH3-INIT6777/2>>
TDON2: LDMA BR,SELB1SP0 ;ADDRESS THE TRANSMITLINK
MICPC=MICPC+1
<MOVE:LDMAR:BR1<SELB1SP0>>
MEM IMM,0 ;TURN OF ASSIGNEDAND TMTED BITS IN FLAG

```

```

(1) 021610 002400
1827 021612
(1) 021612 010067
1828 021614
(1) 021614 002471
1829 021616
(1) 021616 000543
1830 021620
(1) 021620 060360
1831 021622
(1) 021622 115543
1832 021624
(1) 021624 000406
1833 021626
(1) 021626 062400
1834 021630
(1) 021630 010241
1835 021632
(1) 021632 053223
1836
1837 021634
(1) 021634 016600
1838 021636
(1) 021636 020460
1839 021640
(1) 021640 010241
1840 021642
(1) 021642 002642
1841 021644
(1) 021644 000776
1842 021646
(1) 021646 060363
1843 021650
(1) 021652 115556
1844 021652
(1) 021652 000402
1845 021654
(1) 021654

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```

MICPC=MICPC+1
<MOVE:WRMEM:IMM1<0>>
LDMA IMM,STC
MICPC=MICPC+1
<MOVE:LDMAR:IMM1<STC6377>>
MEM IMM,TML1 ;ASSUME WRAPAROUND
MICPC=MICPC+1
<MOVE:WRMEM:IMM1<TML1>>
BRWRT IMM,TML8 ;WRAPAROUND?
MICPC=MICPC+1
<MOVE:WRTEBR:IMM1<TML8>>
CMP BR,SP0
MICPC=MICPC+1
<SUBTC:BR1SP0>
Z TDON4 ;YES
MICPC=MICPC+1
<JUMP:ZCOND1<TDON4-INIT63000*4>1<TDON4-INIT6777/2>>
BRWRT IMM,6 ;OFFSET FOR NEXT TML LINK
MICPC=MICPC+1
<MOVE:WRTEBR:IMM1<6>>
MEM BR,ADD1SP0 ;UPDATE THE POINTER
MICPC=MICPC+1
<MOVE:WRMEM:BR1<ADD1SP0>>
TDON4: LDMA IMM,NXTSP ;ADDRESS DONE LINK
MICPC=MICPC+1
<MOVE:LDMAR:IMM1<NXTSP6377>>
LDMA MEMX,SELB1SP3 ;ADDRESS THE LINK,COPYING
MICPC=MICPC+1
<MOVE:LDMAR:MEMX1<SELB1SP3>>
MEMINC IMM,200 ;ITS ADDRESS TO SP0
MICPC=MICPC+1
<MOVE:WRMEM:INCMAR:IMM1<200>>
MEM BR,INCA1SP0 ;COPY ACTUAL LINK ADDRESS
MICPC=MICPC+1
LDMA IMM,NXTSP ;ADDRESS PTR INT STACK
MICPC=MICPC+1
<MOVE:LDMAR:IMM1<NXTSP6377>>
MEM IMM,INTSTK ;ASSUME WRAP AROUND
MICPC=MICPC+1
<MOVE:WRMEM:IMM1<INTSTK>>
BRWRT IMM,<<NHEND-2>> ;ADDRESS END OF INT STACK
MICPC=MICPC+1
<MOVE:WRTEBR:IMM1<<NHEND-2>>>
CMP BR,SP3 ;WRAPAROUND?
MICPC=MICPC+1
<SUBTC:BR1SP3>
Z TDON40 ;YES---BRANCH
MICPC=MICPC+1
<JUMP:ZCOND1<TDON40-INIT63000*4>1<TDON40-INIT6777/2>>
BRWRT IMM,2 ;OFFSET TO NEXT PAIR
MICPC=MICPC+1
<MOVE:WRTEBR:IMM1<2>>
MEM BR,ADD1SP3 ;UPDATE POINTER
MICPC=MICPC+1

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(1) 021654 002403  
1046 021656 001556  
(1) 021656 000420  
1047 021660 001557  
(1) 021660 003301  
1048 021662 001560  
(1) 021662 010070  
1049 021664 001561  
(1) 021664 043220  
1050 021666 010067  
(1) 021670 001562  
1051 021670 040360  
(1) 021670 001563  
(1) 021670 040360  
1052 021672 001564  
(1) 021672 105562  
1053  
1054 021674 001565  
(1) 021674 010153  
1055 021676 001566  
(1) 021676 043237  
1056 021700 001567  
(1) 021700 010067  
1057 021702 001570  
(1) 021702 053020  
1058 021704 001571  
(1) 021704 054020  
1059 021706 001572  
(1) 021706 116530  
1060 021710 001573  
(1) 021710 104562  
1061  
1062 021712 001574  
(1) 021712 000404  
1063 021714 001575  
(1) 021714 114663  
1064  
1065  
1066  
1067  
1068 021716

```
<MOVE>WHEM:BR1<ADDISP3>>
BRWRT0 IMM,20 ;WRITE INTERRUPT PENDING
MICPC=MICPC+1
<MOVE>WRT0:BR1<20>>
SP BR,AOR0,SP1 ;IN PORT STATUS WORD
MICPC=MICPC+1
<MOVE>ISP1:BR1AOR0:SP1>
LDMA IMM,ETC ;ADDRESS NEXT EMPTY PTR
MICPC=MICPC+1
<MOVE>LDMAR:IMM1<ETC&377>>
SP MEMX,SELB,SP0 ;COPY IT TO SP0
MICPC=MICPC+1
<MOVE>ISP1:MEMX:SELB:SP0>
LDMA IMM,STC ;GET NEXT DONE PTR
MICPC=MICPC+1
<MOVE>LDMAR:IMM1<STC&377>>
CMP MEMX,SP0 ;IDENTICAL?
MICPC=MICPC+1
<SUBTC>MEMX:SP0>
Z RH3 ;FINISH PROCESSING HEADER
MICPC=MICPC+1
<JUMP>ZCOND1<RH3-INIT&3000*4>1<RH3-INIT&777/2>>

TDON1: LDMA IMM,ISP17 ;GET LAST ACKED
MICPC=MICPC+1
<MOVE>LDMAR:IMM1<ISP17&377>>
SP MEMX,SELB,SP17 ;STORE IT IN SP17
MICPC=MICPC+1
<MOVE>ISP1:MEMX:SELB:SP17>
LDMA IMM,STC ;GET START OF TMT CHAIN
MICPC=MICPC+1
<MOVE>LDMAR:IMM1<STC&377>>
LDMA MEMX,SELB:SPBRX:SP0 ;ADDRESS THE LINK
MICPC=MICPC+1
<MOVE>LDMAR:MEMX1<SELB:SPBRX:SP0>>
BRWRT0 MEMX:INCMAR,6SELB ;GET THE FLAGS
MICPC=MICPC+1
<MOVE>WRT0:MEMX:INCMAR1<SELB>>
BR1 TDON3 ;IF BUFFER ASSIGNED PROCEED
MICPC=MICPC+1
<JUMP>BR1CON1<TDON3-INIT&3000*4>1<TDON3-INIT&777/2>>
ALWAYS RH3 ;ELSE---EXIT
MICPC=MICPC+1
<JUMP>ALCOND1<RH3-INIT&3000*4>1<RH3-INIT&777/2>>

OVRUN: BRWRT0 IMM,4
MICPC=MICPC+1
<MOVE>WRT0:BR1<4>>
ALWAYS NTR00
MICPC=MICPC+1
<JUMP>ALCOND1<NTR00-INIT&3000*4>1<NTR00-INIT&777/2>>

; INPUTS:
; SP0 = RECEIVE CHARACTER

PASWRD: SP IBUS,LNOSW,SP13 ;READ PASSWD SWITCH
```

(1) 001576  
(1) 021716 023333  
1069 021720 001577  
(1) 021720 115603  
1070 021722 001600  
(1) 021722 000406  
1071 021724 001601  
(1) 021724 060360  
1072 021726 001602  
(1) 021726 115611  
1073 021730 001603  
(1) 021730 060601  
1074 021732 001604  
(1) 021732 001620  
1075 021734 126740  
(1) 021736 001605  
(1) 021736 001620  
1076 021738 001606  
(1) 021738 001620  
1077 021740 001607  
(1) 021740 106732  
1078 021742 001610  
(1) 021742 104641  
1079 021744 001611  
(1) 021744 063164  
1080 021746 001612  
(1) 021746 000735  
1081 021750 001613  
(1) 021750 100450  
1082  
1083  
1084  
1085 021752 001614  
(1) 021752 010001  
1086 021754 001615  
(1) 021754 002401  
1087 021756 001616  
(1) 021756 010167  
1088 021760 001617  
(1) 021760 057224

```
MICPC=MICPC+1
<MOVE>ISP1:IBUS:LNOSW:SP13>
Z 108 ;IF ALL ONES NO RLD ENABLED
MICPC=MICPC+1
<JUMP>ZCOND1<108-INIT&3000*4>1<108-INIT&777/2>>
BRWRT0 IMM,6 ;CHECK FOR ENTER MOP MODE
MICPC=MICPC+1
<MOVE>WRT0:BR1<6>>
CMP BR,SP0
MICPC=MICPC+1
<SUBTC>BR:SP0>
Z 208 ;IF EQUAL ENTER MOP
MICPC=MICPC+1
<JUMP>ZCOND1<208-INIT&3000*4>1<208-INIT&777/2>>
BRWRT0 BR,SELB:SP1 ;READ STATUS BYTE
MICPC=MICPC+1
<MOVE>WRT0:BR1<SELB:SP1>>
BRSHFT ;SHIFT IT RIGHT
MICPC=MICPC+1
<MOVE>SHFT:BR1:WRT0:SELB>
BR1 RHX ;MESSAGE WITH NO BUFFER ASSIGNED
MICPC=MICPC+1
<JUMP>BR1CON1<RHX-INIT&3000*4>1<RHX-INIT&777/2>>
BRSHFT ;SHIFT RIGHT AGAIN
MICPC=MICPC+1
<MOVE>SHFT:BR1:WRT0:SELB>
BR1 RCV00 ;DLR RECEIVED IN NORMAL MODE
MICPC=MICPC+1
<JUMP>BR1CON1<RCV00-INIT&3000*4>1<RCV00-INIT&777/2>>
ALWAYS RK3 ;HANDLE MAINT MODE MESSAGE
MICPC=MICPC+1
<JUMP>ALCOND1<RK3-INIT&3000*4>1<RK3-INIT&777/2>>
206: SP BR,DECA,SP4 ;COUNT FOR NUMB OF COMPARES
MICPC=MICPC+1
<MOVE>ISP1:BR1:DECA:SP4>
STATE EM2
MICPC=MICPC+1
<MOVE>WRT0:BR1:EM2<EM2-INIT&777/2>>
ALWAYS REXIT
MICPC=MICPC+1
<JUMP>ALCOND1<REXIT-INIT&3000*4>1<REXIT-INIT&777/2>>

;
; .ENABL LSB
;
; RCV01: LDMA IMM,NAKST ;RESET NAKS SENT
MICPC=MICPC+1
<MOVE>LDMAR:IMM1<NAKST&377>>
MEM IMM,1 ;..
MICPC=MICPC+1
<MOVE>WHEM:IMM1<1>>
LDMA IMM,HC ;ADDRESS ORIGINAL RCV BYTE COUNT
MICPC=MICPC+1
<MOVE>LDMAR:IMM1<HC&377>>
SP MEMX:INCMAR,SELB,SP4 ;MOVE BYTE COUNT TO SP4
MICPC=MICPC+1
<MOVE>ISP1:MEMX:INCMAR:SELB:SP4>
```

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1889 021764 SP MEMX,INCMAR,SELB,SP5 ;AND SP5
(1) 021764 001020 MICPC=MICPC+1
(1) 021764 057225 <MOVE:SPX:MEMX:INCMAR:SELB:SP5>
1890 021764 MEM BR,DECA:SP11 ;COPY SP11 FROM MEMORY
(1) 021764 001021 MICPC=MICPC+1
(1) 021764 002571 <MOVE:WPMEM:BR:DECA:SP11>
1891 021766 LDMA IMM,NXTSP
(1) 021766 001022 MICPC=MICPC+1
(1) 021766 010241 <MOVE:LDMAR:IMM:NXTSP<377>>
1892 021770 SP MEMX,LDMAR,SELB,SP3 ;COPY TO SP3
(1) 021770 001023 MICPC=MICPC+1
(1) 021770 053223 <MOVE:SPX:MEMX:LDMAR:SELB:SP3>
1893 021772 MEMINC IMM,204 ;RECEIVE DONE IMAGE
(1) 021772 001024 MICPC=MICPC+1
(1) 021772 016004 <MOVE:WRMEM:INCMAR:IMM:204>
1894 021774 MEM BR,LDMAR,SELA:SP14 ;COPY LINK ADDRESS TO NEXT INTER
(1) 021774 001025 MICPC=MICPC+1
(1) 021774 002014 <MOVE:WRMEM:BR:LDMAR:SELA:SP14>
1895 021776 MEMINC IMM,0 ;ZERO THE FLAGS
(1) 021776 001026 MICPC=MICPC+1
(1) 021776 016000 <MOVE:WRMEM:INCMAR:IMM:0>
1896 022000 SP IMM,INCMAR,SP0,300 ;WRITE A 300 TO SP0
(1) 022000 001027 MICPC=MICPC+1
(1) 022000 0017300 <MOVE:SPX:IMM:INCMAR:SP0:300>
1897 022002 BRWRT IMM,INCMAR,2 ;PREPARE TO ADDRESS NEXT
(1) 022002 001030 MICPC=MICPC+1
(1) 022002 014002 <MOVE:WRTEBR:IMM:INCMAR:2>
1898 ;INTERRUPT STACK AND INCREMENT
1899 ;THE MAR
1900 022004 MEM MEMX,AANDB:SP0 ;MASK OFF ORIGINAL HIGH BYTE
(1) 022004 001031 MICPC=MICPC+1
(1) 022004 042060 <MOVE:WRMEM:MEMX:AANDB:SP0>
1901 ;OF COUNT SAVING EXTENDED MEM BITS
1902 022006 MEMINC MEMX,AORB:SP5 ;COPY TO MEMORY LINK
(1) 022006 001032 MICPC=MICPC+1
(1) 022006 056705 <MOVE:WRMEM:INCMAR:MEMX:AORB:SP5>
1903 022010 MEMINC BR,SELA:SP4
(1) 022010 001033 MICPC=MICPC+1
(1) 022010 007004 <MOVE:WRMEM:INCMAR:BR:SELA:SP4>
1904 022012 LDMA IMM,NXTSP ;ADDRESS NEXT INT STACK
(1) 022012 001034 MICPC=MICPC+1
(1) 022012 010241 <MOVE:LDMAR:IMM:NXTSP<377>>
1945 022014 MEM BR,ADD:SP3
(1) 022014 001035 MICPC=MICPC+1
(1) 022014 002403 <MOVE:WRMEM:BR:ADD:SP3>
1906 022016 BRWRT IMM,<<MMEND-2>> ;ADDRESSEND OF INT STACK
(1) 022016 001036 MICPC=MICPC+1
(1) 022016 000776 <MOVE:WRTEBR:IMM:<<MMEND-2>>>
1907 022020 CMP BR,SP3 ;WRAP AROUND
(1) 022020 001037 MICPC=MICPC+1
(1) 022020 060303 <SUBTC:BR:SP3>
1908 022022 Z 406 ;IF YES-- BRANCH
(1) 022022 001040 MICPC=MICPC+1
(1) 022022 115051 <JUMP:ZCOND:406-INIT&3000*4>:1<406-INIT&777/2>>
1909 206:
1910 022024 BRWRT IMM,5 ;INDEX TO NEXT BUFFER

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(1) 022024 001041 MICPC=MICPC+1
(1) 022024 000405 <MOVE:WRTEBR:IMM:5>>
1911 022026 SP BR,ADD,SP14 ;UPDATE COPY OF POINTER
(1) 022026 001042 MICPC=MICPC+1
(1) 022026 003014 <MOVE:SPX:BR:ADD:SP14>
1912 022030 BRWRT IMM,STC ;ADDRESS OF WRAP AROUND POINT
(1) 022030 001043 MICPC=MICPC+1
(1) 022030 000467 <MOVE:WRTEBR:IMM:STC>
1913 022032 CMP BR,SP14 ;WRAP AROUND?
(1) 022032 001044 MICPC=MICPC+1
(1) 022032 000374 <SUBTC:BR:SP14>
1914 022034 Z 506 ;IF YES---BRANCH
(1) 022034 001045 MICPC=MICPC+1
(1) 022034 115053 <JUMP:ZCOND:506-INIT&3000*4>:1<506-INIT&777/2>>
1915 022036 BRWRT IMM,20 ;MASK FOR INTERRUPT PENDING
(1) 022036 001046 MICPC=MICPC+1
(1) 022036 000420 <MOVE:WRTEBR:IMM:20>
1916 022040 SP DP,AORB,SP1 ;UPDATE PORT STATUS WORD
(1) 022040 001047 MICPC=MICPC+1
(1) 022040 003301 <MOVE:SPX:DP:AORB:SP1>
1924 022042 ALWAYS FLUSH
(1) 022042 001050 MICPC=MICPC+1
(1) 022042 104415 <JUMP:ALCOND:FLUSH-INIT&3000*4>:1<FLUSH-INIT&777/2>>
1926 022044 MEM IMM,INTSTK ;POINT TO START OF INTERRUPT STACK
(1) 022044 001051 MICPC=MICPC+1
(1) 022044 002042 <MOVE:WRMEM:IMM:INTSTK>
1927 022046 ALWAYS 206
(1) 022046 001052 MICPC=MICPC+1
(1) 022046 114041 <JUMP:ALCOND:206-INIT&3000*4>:1<206-INIT&777/2>>
1928 022050 BRWRT IMM,RCL1 ;POINT TO START OF RECEIVE QUEUE
(1) 022050 001053 MICPC=MICPC+1
(1) 022050 000424 <MOVE:WRTEBR:IMM:RCL1>
1929 022052 SP BR,SELB,SP14
(1) 022052 001054 MICPC=MICPC+1
(1) 022052 003234 <MOVE:SPX:BR:SELB:SP14>
1930 022054 ALWAYS 306
(1) 022054 001055 MICPC=MICPC+1
(1) 022054 114046 <JUMP:ALCOND:306-INIT&3000*4>:1<306-INIT&777/2>>
1931 ;DSABL LSB
1932 022056 LDMA IMM,ST
(1) 022056 001056 MICPC=MICPC+1
(1) 022056 010152 <MOVE:LDMAR:IMM:ST<377>>
1933 022060 SP6R MEMX,SELB,SP0
(1) 022060 001057 MICPC=MICPC+1
(1) 022060 003020 <MOVE:SP6R:MEMX:SELB:SP0>
1934 022062 BRWRT BR,ADD:SP0 ;SHIFT LEFT
(1) 022062 001060 MICPC=MICPC+1
(1) 022062 000400 <MOVE:WRTEBR:BR:ADD:SP0>
1935 022064 BR4 OVRUN
(1) 022064 001061 MICPC=MICPC+1
(1) 022064 117174 <JUMP:BR4COND:OVRUN-INIT&3000*4>:1<OVRUN-INIT&777/2>>
1936 022066 BRWRT IMM,1
(1) 022066 001062 MICPC=MICPC+1
(1) 022066 000401 <MOVE:WRTEBR:IMM:1>
1937 022070 BRXX:
1938 022070 NTHRS: LDMA IMM,<<RTHRS+3>>

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(1) 022071 001663 MICPC=MICPC+1
(1) 022072 010177 <MOVE:LDNAR:IMM1<<RTHRS+3>&377>>
1939 022072 FEMINC IMM,0
(1) 022072 001664 MICPC=MICPC+1
(1) 022072 016400 <MOVE:WFMEM:INCMAR:IMM1<0>>
1940 022071 MEM BR,SELB
(1) 022071 001665 MICPC=MICPC+1
(1) 022071 002620 <MOVE:WMMEM:BR1<SELB>>
1941 022076 NTRS1: LDNA IMM,NXTSP
(1) 022076 001666 MICPC=MICPC+1
(1) 022076 010241 <MOVE:LDNAR:IMM1<NXTSP&377>>
1942 022100 LDNA MEMX,SELB:SPX:SP0
(1) 022100 001667 MICPC=MICPC+1
(1) 022100 053220 <MOVE:LDNAR:MEMX1<SELB:SPX:SP0>>
1943 022102 MEMINC IMM,201
(1) 022102 001670 MICPC=MICPC+1
(1) 022102 016601 <MOVE:WMMEM:INCMAR:IMM1<201>>
1944 022104 MEM IMM,<<RTHRS>>
(1) 022104 001671 MICPC=MICPC+1
(1) 022104 002574 <MOVE:WFMEM:IMM1<<RTHRS>>>
1945 022106 LDNA IMM,NXTSP
(1) 022106 001672 MICPC=MICPC+1
(1) 022106 010241 <MOVE:LDNAR:IMM1<NXTSP&377>>
1946 022110 MEM IMM,INTSTK ;ASSUME QUEUE WRAP AROUND
(1) 022110 001673 MICPC=MICPC+1
(1) 022110 002642 <MOVE:WMMEM:IMM1<INTSTK>>
1947 022112 BRWRTS IMM,<<MMEND-2>>
(1) 022112 001674 MICPC=MICPC+1
(1) 022112 000776 <MOVE:WRTB:BR:IMM1<<MMEND-2>>>
1948 022114 CMP BR,SP0
(1) 022114 001675 MICPC=MICPC+1
1949 022116 <SUBTC:HR:SP0>
(1) 022116 001676 Z NTRS2 ;IT DID WRAP AROUND
(1) 022116 115701 MICPC=MICPC+1
1950 022120 <JUMP:ZCOND:<NTRS2-INIT&3000*4>1<NTRS2-INIT&777/2>>
(1) 022120 001677 BRWRTS IMM,2 ;OFFSET TO NEXT PAIR
(1) 022120 000402 MICPC=MICPC+1
1951 022122 <MOVE:WRTB:BR:IMM1<2>>
(1) 022122 001700 MEM BR,ADD:SP0 ;UPDATE QUEUE POINTER
(1) 022122 002400 MICPC=MICPC+1
1952 022124 <MOVE:WMMEM:BR1<ADD:SP0>>
(1) 022124 001701 BRWRTS IMM,20
(1) 022124 000420 MICPC=MICPC+1
1953 022126 <MOVE:WRTB:BR:IMM1<20>>
(1) 022126 001702 SPBR BR,AORB,SP1
(1) 022126 003701 MICPC=MICPC+1
1954 022130 <MOVE:SPBR:BR:AORB:SP1>
(1) 022130 001703 BR0 TAB1 ;FLAGGED BY ERROR TYPE
(1) 022130 116333 MICPC=MICPC+1
1955 022132 <JUMP:BR0:CON1<TAB1-INIT&3000*4>1<TAB1-INIT&777/2>>
(1) 022132 001704 LDNA IMM,ISP11
(1) 022132 010171 SNAK: MICPC=MICPC+1
1956 022134 <MOVE:LDNAR:IMM1<ISP11&377>>
(1) 022134 001705 SP MEMX,SELB,SP11
(1) 022134 003231 MICPC=MICPC+1
<MOVE:SPX:MEMX:SELB:SP11>

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1957 022136 001706 SP BR,INCA,SP11 ;INCREMENT MSG EXPECTED
(1) 022136 003071 MICPC=MICPC+1
1958 022140 SNAK1: <MOVE:SPX:BR:INCA:SP11>
(1) 022140 001707 BRWRTS IMM,1 ;UNNUMB PENDING BIT TO BR
(1) 022140 000401 MICPC=MICPC+1
1959 022142 SNAK2: <MOVE:WRTB:BR:IMM1<1>>
(1) 022142 001710 SP BR,AORB,SP10 ;UPDATE LINE STATUS WORD
(1) 022142 003310 MICPC=MICPC+1
1960 022144 <MOVE:SPX:BR:AORB:SP10>
(1) 022144 001711 ALWAYS FLUSH
(1) 022144 104415 MICPC=MICPC+1
<JUMP:ALCOND1<FLUSH-INIT&3000*4>1<FLUSH-INIT&777/2>>
;
EMTRIG: BRWRTS IMM,24
(1) 022146 001712 MICPC=MICPC+1
(1) 022146 000424 <MOVE:WRTB:BR:IMM1<24>>
1963 022150 OUTPUT BR,<SELB:OBA1>
(1) 022150 001713 MICPC=MICPC+1
(1) 022150 002226 <MOVE:WROUT:BR1<SELB:OBA1>>
1964 022152 BRWRTS IMM,0
(1) 022152 001714 MICPC=MICPC+1
(1) 022152 000400 <MOVE:WRTB:BR:IMM1<0>>
1965 022154 OUTPUT BR,<SELB:OBA2>
(1) 022154 001715 MICPC=MICPC+1
(1) 022154 002227 <MOVE:WROUT:BR1<SELB:OBA2>>
1966 022156 SPBR IBUS,BM873,SP0 ;READ BM873 ADDRESS---
(1) 022156 001716 MICPC=MICPC+1
(1) 022156 003740 <MOVE:SPBR:IBUS:BM873:SP0>
1967 022160 OUTPUT BR,SELB:OUTDA1 ;SET UP LOW BYTE OF ADDRESS
(1) 022160 001717 MICPC=MICPC+1
(1) 022160 002222 <MOVE:WROUT:BR1<SELB:OUTDA1>>
1968 022162 BRWRTS IMM,366 ;HIGH BYTE BASE FOR ROM BOOT
(1) 022162 001720 MICPC=MICPC+1
(1) 022162 000766 <MOVE:WRTB:BR:IMM1<366>>
1969 022164 OUTPUT BR,SELB:OUTDA2 ;
(1) 022164 001721 MICPC=MICPC+1
(1) 022164 002223 <MOVE:WROUT:BR1<SELB:OUTDA2>>
1970 022166 EM6: BRWRTS IMM,21 ;MASK FOR TIMER AND ALSO TO START NPR
(1) 022166 001722 MICPC=MICPC+1
(1) 022166 000421 <MOVE:WRTB:BR:IMM1<21>>
1971 022170 OUT BR,<SELB:OBR>
(1) 022170 001723 MICPC=MICPC+1
(1) 022170 001231 <MOVE:WROUT:BR1<SELB:OBR>>
1972 022172 OUT BR,<SELB:ONPR>
(1) 022172 001724 MICPC=MICPC+1
(1) 022172 001230 <MOVE:WROUT:BR1<SELB:ONPR>>
1973 022174 EM1: BRWRTS IBUS,NPR ;READ NPR CONTROL
(1) 022174 001725 MICPC=MICPC+1
(1) 022174 120600 <MOVE:WRTB:BR:IBUS1<NPR>>
1974 022176 BR0 CTIME
(1) 022176 001726 MICPC=MICPC+1
(1) 022176 102371 <JUMP:BR0:CON1<CKTIME-INIT&3000*4>1<CKTIME-INIT&777/2>>
1975 022200 MEMADR R#1 ;IF NPR DONE
(1) 022200 001727 MICPC=MICPC+1
(1) 022200 002420 <MOVE:WMMEM:R#1<R#1-INIT&777/2>>
1976 022202 ALWAYS ACLOA

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(1) 001730  
(1) 022202 100764  
1977 022204  
(1) 001731  
(1) 022204 023640  
1978 022206  
(1) 001732  
(1) 022206 060400  
1979 022210  
(1) 001733  
(1) 022210 103451  
1980 022212  
(1) 001734  
(1) 022212 010154  
1981 022214  
(1) 001735  
(1) 022214 000402  
1982 022216  
(1) 001736  
(1) 022216 076670  
1983 022220  
(1) 001737  
(1) 022220 076011  
1984 022222  
(1) 001740  
(1) 022222 076012  
1985 022224  
(1) 001741  
(1) 022224 076014  
1986 022226  
(1) 001742  
(1) 022226 076016  
1987 022230  
(1) 001743  
(1) 022230 076017  
1988  
1989 022232  
(1) 001744  
(1) 022232 000460  
1990 022234  
(1) 001745  
(1) 022234 010210  
1991 022236  
(1) 001746  
(2) 022236 002774  
1992 022240  
(1) 001747  
(1) 022240 003004  
1993  
1994  
1995 022242  
(1) 001750  
(1) 022242 010017  
1996 022244  
(1) 001751

MICPC=MICPC+1  
<JUMPIALCONDI<ACLOW=INIT&3000\*4>!<ACLOW=INIT&777/2>>  
TABUPD: SPBR IBUS,RCVCON,SP0 ;READ RECEIVER CONTROL REG  
MICPC=MICPC+1  
<MOVE!SPBR!IBUS!RCVCON!SP0>  
BRWRT BR,ADD!SP0 ;SHIFT LEFT  
MICPC=MICPC+1  
<MOVE!WTEBR!BR!<ADD!SP0>>  
BR7 IDLE ;RECEIVE ACTIVE--IDLE  
MICPC=MICPC+1  
<JUMPIBR7CON!<IDLE=INIT&3000\*4>!<IDLE=INIT&777/2>>  
TAB1: LDMA IMM,IMG10  
MICPC=MICPC+1  
<MOVE!LDMA!IMM!<IMG10&377>>  
BRWRT IMM,2  
MICPC=MICPC+1  
<MOVE!WTEBR!IMM!<2>>  
MEMINC BR,AAAND!SP10 ;SAVE BIT 1 OF SP10  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!BR!<AAAND!SP10>>  
MEMINC BR,SELA!SP11 ;SAVE SP11  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!BR!<SELA!SP11>>  
MEMINC BR,SELA!SP12 ;SAVE SP12  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!BR!<SELA!SP12>>  
MEMINC BR,SELA!SP14 ;SAVE SP14  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!BR!<SELA!SP14>>  
MEMINC BR,SELA!SP16 ;SAVE SP16  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!BR!<SELA!SP16>>  
MEMINC BR,SELA!SP17 ;SAVE SP17  
MICPC=MICPC+1  
<MOVE!WRMEM!INCMAR!BR!<SELA!SP17>>  
;MAR NOW POINTS TO BASE  
STATE RB2 ;DO NOT CHANGE BR UNTIL RB0  
MICPC=MICPC+1  
<MOVE!WTEBR!IMM!<RB2=INIT&777/2>>  
LDMA IMM,TABST ;POINT TO TABLE UPDATE STATE  
MICPC=MICPC+1  
<MOVE!LDMA!IMM!<TABST&377>>  
PSTATE TBU1 ;NEW PORT STATE ADDRESS  
MEM IMM,<<TBU1=INIT&777/2>>  
MICPC=MICPC+1  
<MOVE!WRMEM!IMM!<<TBU1=INIT&777/2>>>  
SP IMM,4,SP4 ;INITIALIZE COUNT  
MICPC=MICPC+1  
<MOVE!SPX!IMM!4!SP4>  
;NOTE: FIRST 6 RAM LOCATIONS ARE NOT WRITTEN  
;TO COKE TABLE.  
LDMA IMM,BASE  
MICPC=MICPC+1  
<MOVE!LDMA!IMM!<BASE&377>>  
ALWAYS RB0  
MICPC=MICPC+1

(1) 022244 104442  
1997 022246  
(1) 001752  
(1) 022246 000402  
1998 022250  
(1) 001753  
(1) 022250 063004  
1999 022252  
(1) 001754  
(1) 022252 023140  
2000 022254  
(1) 001755  
(1) 022254 002006  
2001 022256  
(1) 001756  
(1) 022256 023160  
2002 022260  
(1) 001757  
(1) 022260 002107  
2003 022262  
(1) 001760  
(1) 022262 105366  
2004 022264  
(1) 001761  
(1) 022264 000001  
2005 022266  
(1) 001762  
(1) 022266 116374  
2006  
2007 022270  
(1) 001763  
(1) 022270 070004  
2008 022272  
(1) 001764  
(1) 022272 117371  
2009 022274  
(1) 001765  
(1) 022274 050222  
2010 022276  
(1) 001766  
(1) 022276 050223  
2012 022300  
(1) 001767  
(1) 022300 123200  
2014 022302  
(1) 001770  
(1) 022302 100022  
2015 022304  
(1) 001771  
(1) 022304 010210  
2016 022306  
(1) 001772  
(2) 022306 002460  
2017 022310  
(1) 001773

<JUMPIALCONDI<RB0=INIT&3000\*4>!<RB0=INIT&777/2>>  
EC2: BRWRT IMM,2 ;INCREMENT COUNT/TEST  
MICPC=MICPC+1  
<MOVE!WTEBR!IMM!<2>>  
SP BR,ADD,SP4  
MICPC=MICPC+1  
<MOVE!SPX!BR!ADD!SP4>  
SP IBUS,IOBA1,SP0 ;POINT TO NEXT ADDRESS  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!IOBA1!SP0>  
OUTPUT BR,ADD!IOBA1  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<ADD!IOBA1>>  
SP IBUS,IOBA2,SP0  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!IOBA2!SP0>  
OUTPUT BR,AC!IOBA2  
MICPC=MICPC+1  
<MOVE!WROUT!BR!<AC!IOBA2>>  
C TABMXT  
MICPC=MICPC+1  
<JUMPIALCONDI<TABMXT=INIT&3000\*4>!<TABMXT=INIT&777/2>>  
ECX: BRWRT BR,SELA!SP1 ;READ PORT STATUS  
MICPC=MICPC+1  
<MOVE!WTEBR!BR!<SELA!SP1>>  
BR0 308 ;INIT MODE, WRITE OUT 200 BYTES  
MICPC=MICPC+1  
<JUMPIBR0CON!<308=INIT&3000\*4>!<308=INIT&777/2>>  
;OTHERWISE ONLY WRITE OUT ERROR COUNTERS  
BRWRT BR!LDMA,SELA!SP4 ;READ COUNTER  
MICPC=MICPC+1  
<MOVE!WTEBR!BR!LDMA!<SELA!SP4>>  
BR4 208 ;ALL DONE  
MICPC=MICPC+1  
<JUMPIBR4CON!<208=INIT&3000\*4>!<208=INIT&777/2>>  
10S: OUTPUT MEMX!INCMAR,SELB!OUTDA1 ;STORE COUNTS OF ERRORS  
MICPC=MICPC+1  
<MOVE!WROUT!MEMX!INCMAR!<SELB!OUTDA1>>  
OUTPUT MEMX!INCMAR,SELB!OUTDA2  
MICPC=MICPC+1  
<MOVE!WROUT!MEMX!INCMAR!<SELB!OUTDA2>>  
SP IBUS,NPR,SP0  
MICPC=MICPC+1  
<MOVE!SPX!IBUS!NPR!SP0>  
ALWAYS RB8  
MICPC=MICPC+1  
<JUMPIALCONDI<RB8=INIT&3000\*4>!<RB8=INIT&777/2>>  
20S: LDMA IMM,TABST  
MICPC=MICPC+1  
<MOVE!LDMA!IMM!<TABST&377>>  
PSTATE I3  
MEM IMM,<<I3=INIT&777/2>>  
MICPC=MICPC+1  
<MOVE!WRMEM!IMM!<<I3=INIT&777/2>>>  
ALWAYS RM1  
MICPC=MICPC+1

(1) 022310 104420  
2018 022312  
(1) 001774  
(1) 022312 070604  
2019 022314  
(1) 001775  
(1) 022314 117771  
2020 022316  
(1) 001776  
(1) 022316 114765  
2021 022320  
(1) 001777  
(1) 022320 000000  
2022  
2023 000001

30\$: <JUMP:ALCOND!<RM1-INIT63000\*4>!<RM1-INIT677//2>>  
BRWRT BRILDMAR,SELAI5P4 ;READ COUNTER  
MICPC=MICPC+1  
<MOVE!WPTEBRIBR!LDMAR!<SELAI5P4>>  
BR7 20\$ ;ALL DONE  
MICPC=MICPC+1  
<JUMP!BR7CON!<206-INIT63000\*4>!<206-INIT677//2>>  
ALWAYS 10\$ ;KEEP GOING  
MICPC=MICPC+1  
<JUMP:ALCOND!<106-INIT63000\*4>!<106-INIT677//2>>  
\$ZERO  
MICPC=MICPC+1  
000000  
;  
;END

. Abs. 022322 000

ERRORS DETECTED: 0

,DDCMP/CRF/DS:CRF\_DMCHGH,HIL0W,DUCHGH  
RUN-TIME: 5 0 0 SECONDS  
RUN-TIME RATIO: 68/13=4.9  
COPE USED: 6K (11 PAGES)

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03000

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1685 022322 012737 000001 001226  
1686 022332 012737 022760 001216  
1687  
1688 022336 005737 022360  
1689 022342 001002  
1690 022344 104402 022362  
1691 022350 012737 177777 022360  
1692 022356 104400  
1693 022360 000000  
1694 022362 005377 055104 046504  
(1) 022445 377 042012 041515  
(1) 022473 377 031462 032055  
(1) 022530 005015 031462 032055  
(1) 022566 005015 031462 032055  
(1) 022612 005377 046504 030503  
(1) 022640 031377 026463 034463  
(1) 022675 015 031012 026463  
(1) 022733 015 031012 026463  
(1) 022745 015 031012 026463  
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1708 022760 012737 000002 001226  
1709 022766 012737 023052 001216  
1710  
1711 022774 044737 027012  
1712 023000 012737 100000 001306  
1713 023006 001120  
1714 023010 005000  
1715 023012 013702 012320  
1716 023015 012711 002100

02800

\*\*\*\*\* TEST 1 \*\*\*\*\*  
;THIS IS A SPECIAL TEST WHICH IS ONLY EXECUTED ONE TIME,  
;THE FIRST PASS AFTER THE DIAGNOSTIC IS LOADED. IT TYPES ON  
;THE CONSOLE THE PART NUMBERS OF THE CROMS WHICH THIS  
;REVISION SUPPORTS. TO FORCE A TYPE OUT PATCH LOCATION  
;ROMNUM: TO A ZERO.  
;\*\*\*\*\*  
; TEST 1  
;-----  
TST1: MOV R1,TSTNO  
MOV #TST2,NEXT  
;R1 CONTAINS BASE DMC11 ADDRESS  
;FIRST TIME HERET  
;SKIP IF NOT  
;TYPE PART NUMBERS  
;SET FLAG TO ONLY TYPE ONCE  
1\$: MOV #-1,ROMNUM  
SCOPE  
ROMNUM: 0  
ROM1: .ASCII <377><12>/DZDMG-C SUPPORTS THE FOLLOWING CROM PART NUMBERS:/  
.ASCII <377><12>/DMC11-AR (M8200-1A)/  
.ASCII <377>/23-414A9/<15><12>/23-415A9/<15><12>/23-416A9/  
.ASCII <15><12>/23-417A9/<15><12>/23-418A9/<15><12>/23-419A9/  
.ASCII <15><12>/23-420A9/<15><12>/23-421A9/  
.ASCII <377><12>/DMC11-AL (M8200-1B)/  
.ASCII <377>/23-392A9/<15><12>/23-393A9/<15><12>/23-394A9/  
.ASCII <15><12>/23-395A9/<15><12>/23-396A9/<15><12>/23-397A9/  
.ASCII <15><12>/23-398A9/  
.ASCIZ <15><12>/23-399A9/  
;EVEN

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1708 022760 012737 000002 001226  
1709 022766 012737 023052 001216  
1710  
1711 022774 044737 027012  
1712 023000 012737 100000 001306  
1713 023006 001120  
1714 023010 005000  
1715 023012 013702 012320  
1716 023015 012711 002100

\*\*\*\*\* TEST 2 \*\*\*\*\*  
;THIS IS A SPECIAL TEST WHICH WILL RUN ON A KMC (DMC WITH  
;WRITABLE CONTROL STORE) TO LOAD THE CROM WITH THE DDCMP  
;MICRO-CODE. FIRST BE SURE BIT1 OF STAT3 IS SET UP AS FOLLOWS  
;1=LOCAL HIGH SPEED CODE, 0=REMOTE LOW SPEED CODE THE STATUS  
;OF STAT3 BIT1 DETERMINES WHICH MICRO-CODE WILL  
;BE LOADED IN THE KMC. LOOP ON THIS TEST FOR A FEW SECONDS  
;TO LOAD THE KMC.  
;\*\*\*\*\*  
; TEST 2  
;-----  
TST2: MOV R2,TSTNO  
MOV #TST3,NEXT  
;R1 CONTAINS BASE DMC11 ADDRESS  
;CHECK FOR HI OR LO  
;BE SURE DMC HAS CROM  
;SKIP IF NO CROM  
;R0=CROM ADDRESS  
;R2 POINTS TO ROMMAP  
1\$: MOV #BIT10,(R1)  
;SET R0M0

```

1717 023022 010061 000004      MOV     R0,4(R1)      ;LOAD CROM ADDRESS
1718 023020 012261 000006      MOV     (R2)+,6(R1)  ;LOAD WORD TO BE WRITTEN
1719 023032 052711 020000      BIS     #BIT13,(R1)  ;WRITE IT!
1720 023036 005200                INC     R0            ;NEXT ADDRESS
1721 023040 022700 002000      CMP     #2000,R0     ;DONE YET?
1722 023044 001304                BNE    18            ;BR IF NO
1723 023046 005011                CLR     (R1)         ;CLEAR SEL0
1724 023050 104400                29:   SCOPE         ;SCOPE THIS TEST
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1735 023052 012737 000003 001226      TST3:  MOV     #3,ISTNO
1736 023060 012737 023166 001216      MOV     #TST4,NEXT
1737
1738 023066 104412                MSTRCLR          ;MASTER CLEAR DMC11 ADDRESS
1739 023070 104412                MSTRCLR          ;MASTER CLEAR DMC11
1740 023072 013701 001404                MOV     DMC5R,R1  ;R1 = DMC BASE ADDRESS
1741 023076 005011                CLR     (R1)      ;CLEAR SEL0
1742 023100 012705 052525                MOV     #52525,R5 ;START WITH 125
1743 023104 010561 000004                MOV     R5,4(R1)  ;PORT4_125
1744 023110 104414                ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1745 023112 120520                120500          ;BR - PORT4
1746 023114 104414                ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1747 023116 001620                061620          ;BR RSH_BR, SHIFT BR RIGHT
1748 023120 104414                ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1749 023122 061225                061225          ;PORT5_BR
1750 023124 006005                ROR     R5        ;R5 = "EXPECTED"
1751 023126 116104 000005                MOV     5(R1),R4  ;R4 = "FOUND"
1752 023132 120504                CMP     R5,R4     ;DID BR SHIFT RIGHT ONCE?
1753 023134 001401                BEQ    18         ;BR IF YES
1754 023136 104012                HLT    12         ;BR RIGHT SHIFT ERROR
1755 023140
1756 023140 104414                18:   ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1757 023142 061620                061620          ;BR RSH_BR, SHFT BR RIGHT AGAIN
1758 023144 104414                ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1759 023146 061225                061225          ;PORT5_BR
1760 023150 006005                ROR     R5        ;R5 = "EXPECTED"
1761 023152 116104 000005                MOV     5(R1),R4  ;R4 = "FOUND"
1762 023156 120504                CMP     R5,R4     ;DID BR SHIFT RIGHT?
1763 023160 001401                BEQ    28         ;BR IF YES
1764 023162 104012                HLT    12         ;BR RIGHT SHIFT ERROR
1765 023164 104400                28:   SCOPE         ;SCOPE THIS TEST
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;***** TEST 4 *****
;CROM READ TEST
;THIS TEST READS EACH ROM LOCATION AND COMPARES
;IT TO A SOFTWARE DUPLICATE OF THE CROM, THIS TEST
;ALSO TESTS THE JUMP(I) MICRO-PROCESSOR INSTRUCTION.

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1799 023166 012737 000004 001226      TST4:  MOV     #4,TSTNO
1800 023174 012737 023362 001216      MOV     #TST5,NEXT
1801 023202 012737 023240 001220      MOV     #18,LOCK
1802
1803 023210 104412                MSTRCLR          ;R1 CONTAINS BASE DMC11 ADDRESS
1804 023212 032737 100000 001366                BIT     #BIT15,STAT1 ;MASTER CLEAR DMC11
1805 023220 001057                BNE    48         ;IS IT RAM OR ROM
1806 023222 044737 027012                JSP    PC,MAPCK   ;SKIP TEST IF CROM
1807 023226 005011                CLR     (R1)      ;CHECK FOR HI OR LO
1808 023230 013700 012320                MOV     ROMMAP,R0 ;CLEAR RUN
1809 023234 005002                CLR     R2        ;R0 POINTS TO SOFTWARE ROM MAP
1810 023236 005003                CLR     R3        ;R2 CONTAINS ROM ADDRESS BITS 0-7
1811 023240 042737 014377 023260                BIC    #14377,28  ;R3 CONTAINS ROM ADDRESS BITS 8-9 IN BITS 11&12
1812 023246 050237 023260                BIS    R2,28     ;CLEAR ADDRESS FIELDS OF INSTRUCTION
1813 023252 001337 023260                BIS    R3,28     ;ADD BITS 0-7 TO INSTRUCTION
1814 023256 104414                ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1815 023260 100400                28:   100400          ;JUMP(I) TO ROM ADDRESS IN R2 & R3
1816 023262 112711 002000                MOV     #BIT10,(R1) ;SET ROM0
1817 023266 011005                MOV     (R0),R5   ;PUT "EXPECTED" IN R5
1818 023270 016104 000006                MOV     6(R1),R4  ;PUT "FOUND" IN R4
1819 023274 005004                CMP     R5,R4     ;COMPARE ROM CONTENTS TO SOFT DUP
1820 023276 001414                BEQ    36         ;BR IF OK
1821 023300 010337 001252                MOV     R3,TEMP3  ;PUT ROM ADDRESS IN TEMP3
1822 023304 000241                CLC                    ;FOR ERROR TYPEOUT
1823 023306 006037 001252                ROR     TEMP3
1824 023312 006037 001252                ROR     TEMP3
1825 023314 006037 001252                ROR     TEMP3
1826 023322 050237 001252                BIS    R2,TEMP3  ;TEMP3 NOW CONTAINS CORRECT ADDRESS
1827 023326 104404                HLT    4          ;ROM READ ERROR
1828 023330 104401                35:   SCOP1         ;LOOP 10 18 IF SW09=1

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1829 023332 005720          TST (R0)+      ;BUMP SOFT POINTER
1830 023333 005232          INC R2         ;BUMP ROM ADDRESS
1831 023330 022702 000400  CMP #400,R2   ;IS R2 TO MAX YET?
1832 023342 001336          BNE 10        ;BR IF NO
1833 023344 005002          CLR R2       ;YES, RESE1 R2 TO 0
1834 023346 002703 004000  ADD #4000,R3  ;INC TO NEXT PAGE OF ROM
1835 023352 022703 020000  CMP #20000,R3 ;DONE YET?
1836 023356 001336          BNE 10        ;BR IF NO
1837 023360 104100          4S: SCOPE    ;SCOPE THIS TEST
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1849 023362 012737 000005 001226  IST5: MOV #5,TSTNO
1850 023370 012737 023556 001216  MOV #TST6,NEXT
1851 023376 012737 023422 001220  MOV #1$,LOCK
1852
1853 023404 104412          MSTCLR       ;R1 CONTAINS BASE DMC11 ADDRESS
1854 023406 032737 100000 001366  BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
1855 023414 001057          BNE 08+2     ;IS IT CRAM?
1856 023416 004737 027012  JSR PC,MAPCK ;SKIP TEST IF YES
1857
1858 023422 004737 026656          1S: JSR PC,CLRALL ;CHECK FOR HI OR LO
1859 023426 104414          ROMCLK      ;CLEAR ALL CONDITIONS
1860 023430 100400          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1861 023432 104414          ROMCLK      ;START AT ROM PC=0
1862 023434 114377          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1863 023436 004737 026750  JSR PC,ROMDAT ;JUMP TO ROM PC OF 1777
1864 023442 000002          Z           ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1865 023444 020504          CMP R5,R4   ;INDEX
1866 023446 001401          BEQ 20      ;ARE NEW PC CONTENTS CORRECT?
1867 023450 104006          HLT 6       ;BR IF YES
1868 023452 104401          SCOPE1     ;ERROR, CHOM PC IS WRONG
1869 023454 012737 023462 001220  MOV #3$,LOCK ;LOOP TO 1$ IF SW09=1
1870
1871 023462 004737 026656          3S: JSR PC,CLRALL ;NEW SCOPE1
1872 023466 104414          ROMCLK      ;CLEAR ALL CONDITIONS
1873 023470 100403          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1874 023472 104414          ROMCLK      ;START AT ROM PC=3
1875 023474 100000          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1876 023476 004737 026750  JSR PC,ROMDAT ;JUMP TO ROM PC OF 0
1877 023502 000000          JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1878 023504 020504          CMP R5,R4   ;INDEX
1879 023506 001401          BEQ 40      ;ARE NEW PC CONTENTS CORRECT?
1880 023510 104006          HLT 6       ;BR IF YES
1881 023512 104401          SCOPE1     ;ERROR, CHOM PC IS WRONG
1882 023514 012737 023522 001220  MOV #5$,LOCK ;LOOP TO 3$ IF SW09=1
1883 023522          5S:          ;NEW SCOPE1
1884 023522 004737 026656          JSR PC,CLRALL ;CLEAR ALL CONDITIONS

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1885 023526 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1886 123530 100406          ROMCLK      ;START AT ROM PC=0
1887 023532 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1888 023534 104125          ROMCLK      ;JUMP TO ROM PC OF 525
1889 023536 004737 026750  JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1890 023542 000016          16         ;INDEX
1891 023544 020504          CMP R5,R4   ;ARE NEW ROM PC CONTENTS CORRECT?
1892 023546 001401          BEQ 60      ;BR IF YES
1893 023550 104006          HLT 6       ;ERROR, CHOM PC IS WRONG
1894 023552 104401          SCOPE1     ;LOOP TO 5$ IF SW09=1
1895 023554 104400          6S: SCOPE    ;NEW SCOPE1
1896
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1906 023556 012737 000006 001226  TST6: MOV #6,TSTNO
1907 023564 012737 023736 001216  MOV #TST7,NEXT
1908 023572 012737 023616 001220  MOV #1$,LOCK
1909
1910 023600 104412          MSTCLR       ;R1 CONTAINS BASE DMC11 ADDRESS
1911 023602 032737 100000 001366  BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
1912 023610 001051          BNE 08+2     ;IS IT CRAM?
1913 023612 004737 027012  JSR PC,MAPCK ;SKIP TEST IF YES
1914
1915 023616 104414          1S: JSR PC,CLRALL ;CHECK FOR HI OR LO
1916 023620 100400          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1917 023622 104414          ROMCLK      ;START AT ROM PC=0
1918 023624 114777          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1919 023626 004737 026750  JSR PC,ROMDAT ;JUMP TO ROM PC OF 1777
1920 023632 003776          JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1921 023634 020504          CMP R5,R4   ;INDEX
1922 023636 001401          BEQ 20      ;ARE NEW PC CONTENTS CORRECT?
1923 023640 104006          HLT 6       ;BR IF YES
1924 023642 104401          SCOPE1     ;ERROR, CHOM PC IS WRONG
1925 023644 012737 023652 001220  MOV #3$,LOCK ;LOOP TO 3$ IF SW09=1
1926
1927 023652 104414          3S:          ;NEW SCOPE1
1928 023654 100403          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1929 023656 104414          ROMCLK      ;START AT ROM PC=3
1930 023660 100000          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1931 023662 004737 026750  JSR PC,ROMDAT ;JUMP TO ROM PC OF 0
1932 023664 000000          JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1933 023666 020504          CMP R5,R4   ;INDEX
1934 023668 001401          BEQ 40      ;ARE NEW PC CONTENTS CORRECT?
1935 023670 104006          HLT 6       ;BR IF YES
1936 023672 104401          SCOPE1     ;ERROR, CHOM PC IS WRONG
1937 023674 012737 023706 001220  MOV #5$,LOCK ;LOOP TO 5$ IF SW09=1
1938
1939 023706          5S:          ;NEW SCOPE1
1940 023706 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1941 023710 100406          ROMCLK      ;START AT ROM PC=6

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1941 023712 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304.
1942 023714 104525 ;JUMP TO ROM PC OF 525
1943 023716 004737 026750 JSR PC,ROMDAT ;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1944 023722 001252 ;INDEX
1945 023724 020504 CMP R5,R4 ;ARE NEW ROM PC CONTENTS CORRECT?
1946 023726 001401 BEQ 66 ;BR IF YES
1947 023730 104006 HLT 6 ;ERROR, CROM PC IS WRONG
1948 023732 104401 68: SCOP1 ;LOOP TO 55 IF SW59=1
1949 023734 104400 SCOPE ;SCOPE THIS TEST
1950
1951
1952 ;***** TEST 7 *****
1953 ;*CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
1954 ;*SET THE C BIT, PERFORM THE JUMP INSTRUCTION,
1955 ;*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
1956 ;*****
1957
1958 ; TEST 7
1959 ;-----
1960 023736 012737 000007 001220 TST7: MOV #7,TSTNO
1961 023744 012737 024132 001216 MOV #TST10,NEXT
1962 023752 012737 023776 001220 MOV #10,LOCK
1963
1964 023760 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
1965 023762 032737 100000 001366 ;MASTER CLEAR DMC11
1966 023770 001057 BIT #BIT15,STAT1 ;IS IT CRAM?
1967 023772 004737 027012 BNE 66+2 ;SKIP TEST IF YES
1968 023776 JSR PC,MAPCK ;CHECK FOR HI OR LO
1969 023776 004737 026724 16: JSR PC,SETC ;SET THE C BIT*
1970 024002 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1971 024004 100400 ;START AT ROM PC=0
1972 024006 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1973 024010 115377 1143771<400*2> ;JUMP TO ROM PC OF 1777
1974 024012 004737 026750 JSR PC,ROMDAT ;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1975 024016 003776 ;INDEX
1976 024020 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
1977 024022 001401 BEQ 28 ;BR IF YES
1978 024024 104006 HLT 6 ;ERROR, CROM PC IS WRONG
1979 024026 104401 25: SCOP1 ;LOOP TO 16 IF SW09=1
1980 024030 012737 024036 001220 MOV #30,LOCK ;NEW SCOP1
1981 024036 35:
1982 024036 004737 026724 JSR PC,SETC ;SET THE C BIT*
1983 024042 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1984 024044 100403 ;START AT ROM PC=3
1985 024046 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1986 024050 101000 1000001<400*2> ;JUMP TO ROM PC OF 0
1987 024052 004737 026750 JSR PC,ROMDAT ;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1988 024056 000000 ;INDEX
1989 024060 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
1990 024062 001401 BEQ 48 ;BR IF YES
1991 024064 104006 HLT 6 ;ERROR, CROM PC IS WRONG
1992 024066 104401 45: SCOP1 ;LOOP TO 35 IF SW09=1
1993 024070 012737 024076 001220 MOV #50,LOCK ;NEW SCOP1
1994 024076 55:
1995 024076 004737 026724 JSR PC,SETC ;SET THE C BIT*
1996 024102 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
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1997 024104 100406 ;START AT ROM PC=6
1998 024106 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1999 024110 105125 1041251<400*2> ;JUMP TO ROM PC OF 525
2000 024112 004737 026750 JSR PC,ROMDAT ;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2001 024116 001252 ;INDEX
2002 024120 020504 CMP R5,R4 ;ARE NEW ROM PC CONTENTS CORRECT?
2003 024122 001401 BEQ 66 ;BR IF YES
2004 024124 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2005 024126 104401 65: SCOP1 ;LOOP TO 55 IF SW59=1
2006 024130 104400 SCOPE ;SCOPE THIS TEST
2007
2008
2009 ;***** TEST 10 *****
2010 ;*CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
2011 ;*SET THE Z BIT, PERFORM THE JUMP INSTRUCTION,
2012 ;*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
2013 ;*****
2014
2015 ; TEST 10
2016 ;-----
2017 024132 012737 000010 001226 TST10: MOV #10,TSTNO
2018 024140 012737 024326 001216 MOV #TST11,NEXT
2019 024146 012737 024172 001220 MOV #10,LOCK
2020
2021 024154 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2022 024156 032737 100000 001366 ;MASTER CLEAR DMC11
2023 024164 001057 BIT #BIT15,STAT1 ;IS IT CRAM?
2024 024166 004737 027012 BNE 66+2 ;SKIP TEST IF YES
2025 024172 JSR PC,MAPCK ;CHECK FOR HI OR LO
2026 024172 004737 026742 18: JSR PC,SETZ ;SET THE Z BIT*
2027 024176 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2028 024200 100400 ;START AT ROM PC=0
2029 024202 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2030 024204 115777 1143771<400*3> ;JUMP TO ROM PC OF 1777
2031 024206 004737 026750 JSR PC,ROMDAT ;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2032 024212 003776 ;INDEX
2033 024214 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2034 024216 001401 BEQ 28 ;BR IF YES
2035 024220 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2036 024222 104401 28: SCOP1 ;LOOP TO 16 IF SW09=1
2037 024224 012737 024232 001220 MOV #30,LOCK ;NEW SCOP1
2038 024232 38:
2039 024232 004737 026742 JSR PC,SETZ ;SET THE Z BIT*
2040 024236 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2041 024240 100403 ;START AT ROM PC=3
2042 024242 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2043 024244 101400 1000001<400*3> ;JUMP TO ROM PC OF 0
2044 024246 004737 026750 JSR PC,ROMDAT ;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2045 024252 000000 ;INDEX
2046 024254 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2047 024256 001401 BEQ 48 ;BR IF YES
2048 024260 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2049 024262 104401 45: SCOP1 ;LOOP TO 35 IF SW09=1
2050 024264 012737 024272 001220 MOV #50,LOCK ;NEW SCOP1
2051 024272 55:
2052 024272 004737 026742 JSR PC,SETZ ;SET THE Z BIT*
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2053 024276 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304.
2054 024300 100400 100400 ;START AT ROM PC=6
2055 024302 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2056 024304 105525 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2057 024306 004737 026750 JSR PC,ROMDAT ;JUMP TO ROM PC OF 525
2058 024312 001252 ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2059 024314 020504 ;INDEX
2060 024316 001401 CMP R5,R4 ;ARE NEW ROM PC CONTENTS CORRECT?
2061 024320 100400 BEQ 68 ;BR IF YES
2062 024322 104401 HLT 6 ;ERROR, CROM PC IS WRONG
2063 024324 104400 65: SCOPI ;LOOP TO 56 IF SW59=1
SCOPE ;SCOPE THIS TEST

;***** TEST 11 *****
;CROM TEST OF JUMP(I) ON BR0 SET MICRO-PROCESSOR INSTRUCTION.
;SET THE BR0 BIT, PERFORM THE JUMP INSTRUCTION.
;VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
;*****

; TEST 11
;-----
2074 024326 012737 000011 001226 TST11: MOV #11,TSTNO
2075 024334 012737 024522 001216 MOV #TST12,NEXT
2076 024342 012737 024366 001220 MOV #16,LOCK

2077 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2078 024350 104412 BIT ;MASTER CLEAR DMC11
2079 024352 032737 100000 001366 BIT #BIT15,STAT1 ;IS IT CRAM?
2080 024360 001057 BNE 68+2 ;SKIP TEST IF YES
2081 024362 004737 027012 JSR PC,MAPCK ;CHECK FOR HI OR LO

2082 024366 18: JSR PC,SETBR0 ;SET THE BR0 BIT
2083 024366 004737 026674 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2084 024372 104414 100400 ;START AT ROM PC=0
2085 024374 100400 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2086 024376 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2087 024400 116377 114377;<400*4> ;JUMP TO ROM PC OF 1777
2088 024402 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2089 024406 003776 ;INDEX
2090 024410 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2091 024412 001401 BEQ 28 ;BR IF YES
2092 024414 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2093 024416 104401 28: SCOPI ;LOOP TO 16 IF SW09=1
2094 024420 012737 024426 001220 MOV #38,LOCK ;NEW SCOPI
2095 024426 38: JSR PC,SETBR0 ;SET THE BR0 BIT
2096 024426 004737 026674 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2097 024432 104414 100403 ;START AT ROM PC=3
2098 024434 100403 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2099 024436 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2100 024440 102000 100000;<400*4> ;JUMP TO ROM PC OF 0
2101 024442 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2102 024446 000000 ;INDEX
2103 024450 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2104 024452 001401 BEQ 48 ;BR IF YES
2105 024454 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2106 024456 104401 48: SCOPI ;LOOP TO 36 IF SW09=1
2107 024460 012737 024466 001220 MOV #58,LOCK ;NEW SCOPI
2108 024466 58:

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2109 024466 004737 026674 JSR PC,SETBR0 ;SET THE BR0 BIT
2110 024472 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2111 024474 100406 100400 ;START AT ROM PC=6
2112 024476 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2113 024500 106125 104125;<400*4> ;JUMP TO ROM PC OF 525
2114 024502 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2115 024506 001252 ;INDEX
2116 024510 020504 CMP R5,R4 ;ARE NEW ROM PC CONTENTS CORRECT?
2117 024512 001401 BEQ 68 ;BR IF YES
2118 024514 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2119 024516 104401 68: SCOPI ;LOOP TO 58 IF SW59=1
2120 024520 104400 SCOPE ;SCOPE THIS TEST
2121
2122
2123 ;***** TEST 12 *****
2124 ;CROM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
2125 ;SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION.
2126 ;VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
2127 ;*****
2128
2129 ; TEST 12
2130 ;-----
2131 024522 012737 000012 001226 TST12: MOV #12,TSTNO
2132 024530 012737 024716 001216 MOV #TST13,NEXT
2133 024536 012737 024562 001220 MOV #18,LOCK

2134 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2135 024544 104412 BIT ;MASTER CLEAR DMC11
2136 024546 032737 100000 001366 BIT #BIT15,STAT1 ;IS IT CRAM?
2137 024554 001057 BNE 68+2 ;SKIP TEST IF YES
2138 024556 004737 027012 JSR PC,MAPCK ;CHECK FOR HI OR LO

2139 024562 18: JSR PC,SETBR1 ;SET THE BR1 BIT
2140 024562 004737 026702 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2141 024566 104414 100400 ;START AT ROM PC=0
2142 024570 100400 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2143 024572 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2144 024574 116777 114377;<400*5> ;JUMP TO ROM PC OF 1777
2145 024576 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2146 024602 003776 ;INDEX
2147 024604 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2148 024606 001401 BEQ 28 ;BR IF YES
2149 024610 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2150 024612 104401 28: SCOPI ;LOOP TO 16 IF SW09=1
2151 024614 012737 024622 001220 MOV #38,LOCK ;NEW SCOPI
2152 024622 38: JSR PC,SETBR1 ;SET THE BR1 BIT
2153 024622 004737 026702 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2154 024626 104414 100403 ;START AT ROM PC=3
2155 024630 100403 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2156 024632 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2157 024634 102400 100000;<400*5> ;JUMP TO ROM PC OF 0
2158 024636 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2159 024642 000000 ;INDEX
2160 024644 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2161 024646 001401 BEQ 48 ;BR IF YES
2162 024650 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2163 024652 104401 48: SCOPI ;LOOP TO 36 IF SW09=1
2164 024654 012737 024662 001220 MOV #56,LOCK ;NEW SCOPI

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2165 024662          56:
2166 024662 004737 026702      JSR   PC,SETBR1      ;SET THE BR1 BIT
2167 024666 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2168 024670 100400          100400 ;START AT ROM PC=6
2169 024672 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2170 024674 106525          104125<400*5> ;JUMP TO ROM PC OF 525
2171 024676 004737 026750      JSR   PC,ROMDAT      ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2172 024702 001252          1252 ;INDEX
2173 024704 020504          CMP   R5,R4          ;ARE NEW ROM PC CONTENTS CORRECT?
2174 024706 001401          BEQ  6                ;BR IF YES
2175 024710 104006          HLT  6                ;ERROR, CROM PC IS WRONG
2176 024712 104401          68: SCOPI           ;LOOP TO 56 IF SW59=1
2177 024714 104400          SCOPE ;SCOPE THIS TEST
2178
2179
2180 ;***** TEST 13 *****
2181 ;*CROM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
2182 ;*SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
2183 ;*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
2184 ;*****
2185
2186 ; TEST 13
2187 ;-----
2188 024716 012737 000013 001226      TST13: MOV   #13,TSTNO
2189 024724 012737 025112 001216      MOV   #TST14,NEXT
2190 024732 012737 024756 001220      MOV   #13,LOCK
2191
2192 024740 104412          MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2193 024742 032737 100000 001366      BIT   #BIT15,STAT1 ;MASTER CLEAR DMC11
2194 024750 001057          BNE  68+2            ;IS IT CRAM?
2195 024752 004737 027012          JSR   PC,MAPCK       ;SKIP TEST IF YES
2196 024756
2197 024756 004737 026710          16: JSR   PC,SETBR4      ;SET THE BR4 BIT
2198 024762 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2199 024764 100400          100400 ;START AT ROM PC=6
2200 024766 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2201 024770 117377          114377<400*6> ;JUMP TO ROM PC OF 1777
2202 024772 004737 026750      JSR   PC,ROMDAT      ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2203 024776 003776          3776 ;INDEX
2204 025000 020504          CMP   R5,R4          ;ARE NEW PC CONTENTS CORRECT?
2205 025002 001401          BEQ  28              ;BR IF YES
2206 025004 104006          HLT  6                ;ERROR, CROM PC IS WRONG
2207 025006 104401          28: SCOPI           ;LOOP TO 16 IF SW09=1
2208 025010 012737 025016 001220      MOV   #38,LOCK      ;NEW SCOPI
2209 025016
2210 025016 004737 026710          38: JSR   PC,SETBR4      ;SET THE BR4 BIT
2211 025022 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2212 025024 100403          100403 ;START AT ROM PC=3
2213 025026 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2214 025030 103009          100000<400*6> ;JUMP TO ROM PC OF 0
2215 025032 004737 026750      JSR   PC,ROMDAT      ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2216 025036 000000          0 ;INDEX
2217 025040 020504          CMP   R5,R4          ;ARE NEW PC CONTENTS CORRECT?
2218 025042 001401          BEQ  48              ;BR IF YES
2219 025044 104006          HLT  6                ;ERROR, CROM PC IS WRONG
2220 025046 104401          48: SCOPI           ;LOOP TO 36 IF SW09=1

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2221 025050 012737 025056 001220      MOV   #58,LOCK      ;NEW SCOPI
2222 025056
2223 025056 004737 026710          58: JSR   PC,SETBR4      ;SET THE BR4 BIT
2224 025062 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2225 025064 100406          100406 ;START AT ROM PC=6
2226 025066 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2227 025070 107125          104125<400*6> ;JUMP TO ROM PC OF 525
2228 025072 004737 026750      JSR   PC,ROMDAT      ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2229 025076 001252          1252 ;INDEX
2230 025100 020504          CMP   R5,R4          ;ARE NEW ROM PC CONTENTS CORRECT?
2231 025102 001401          BEQ  68              ;BR IF YES
2232 025104 104006          HLT  6                ;ERROR, CROM PC IS WRONG
2233 025106 104401          68: SCOPI           ;LOOP TO 56 IF SW59=1
2234 025110 104400          SCOPE ;SCOPE THIS TEST
2235
2236
2237 ;***** TEST 14 *****
2238 ;*CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
2239 ;*SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,
2240 ;*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
2241 ;*****
2242
2243 ; TEST 14
2244 ;-----
2245 025112 012737 000014 001226      TST14: MOV   #14,TSTNO
2246 025120 012737 025306 001216      MOV   #TST15,NEXT
2247 025126 012737 025152 001220      MOV   #15,LOCK
2248
2249 025134 104412          MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2250 025136 032737 100000 001366      BIT   #BIT15,STAT1 ;MASTER CLEAR DMC11
2251 025144 001057          BNE  68+2            ;IS IT CRAM?
2252 025146 004737 027012          JSR   PC,MAPCK       ;SKIP TEST IF YES
2253 025152
2254 025152 004737 026716          16: JSR   PC,SETBR7      ;SET THE BR7 BIT
2255 025156 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2256 025160 100400          100400 ;START AT ROM PC=6
2257 025162 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2258 025164 117777          114377<400*7> ;JUMP TO ROM PC OF 1777
2259 025166 004737 026750      JSR   PC,ROMDAT      ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2260 025172 003776          3776 ;INDEX
2261 025174 020504          CMP   R5,R4          ;ARE NEW PC CONTENTS CORRECT?
2262 025176 001401          BEQ  28              ;BR IF YES
2263 025200 104006          HLT  6                ;ERROR, CROM PC IS WRONG
2264 025202 104401          28: SCOPI           ;LOOP TO 16 IF SW09=1
2265 025204 012737 025212 001220      MOV   #38,LOCK      ;NEW SCOPI
2266 025212
2267 025212 004737 026716          38: JSR   PC,SETBR7      ;SET THE BR7 BIT
2268 025216 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2269 025220 100403          100403 ;START AT ROM PC=3
2270 025222 104414          ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2271 025224 103009          100000<400*7> ;JUMP TO ROM PC OF 0
2272 025226 004737 026750      JSR   PC,ROMDAT      ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2273 025232 000000          0 ;INDEX
2274 025234 020504          CMP   R5,R4          ;ARE NEW PC CONTENTS CORRECT?
2275 025236 001401          BEQ  48              ;BR IF YES
2276 025240 104006          HLT  6                ;ERROR, CROM PC IS WRONG

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2277 425242 104401
2278 425244 012737 025252 001220 48: SCOP1 ;LOOP TO 38 IF SW09=1
2279 025252 MOV #58,LOCK ;NEW SCOP1
2280 425252 004737 026716 58: JSR PC,SETR7 ;SET THE BR7 BIT
2281 425256 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2282 425260 100406 100406 ;START AT ROM PC=6
2283 425262 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2284 025264 107525 1041251<400*7> ;JUMP TO ROM PC OF 525
2285 425266 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2286 425272 001252 1252 ;INDEX
2287 425274 020504 CMP R5,R4 ;ARE NEW ROM PC CONTENTS CORRECT?
2288 425276 001401 BEQ 6 ;BR IF YES
2289 025300 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2290 425302 104401 68: SCOP1 ;LOOP TO 58 IF SW59=1
2291 025304 104400 SCOPE ;SCOPE THIS TEST
2292
2293
2294
2295 ;***** TEST 15 *****
2296 ;*CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
2297 ;*CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION,
2298 ;*VERIFY THAT THE JUMP DID NOT OCCUR BY READING
2299 ;*THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
2300 ;*****
2301
2302 ; TEST 15
2303 425306 012737 000015 001220 TST15: MOV #15,TSTNO
2304 425314 012737 025502 001216 MOV #TST16,NEXT
2305 425322 012737 025346 001220 MOV #18,LOCK
2306
2307 425330 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2308 425332 032737 100000 001366 BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
2309 425340 001057 BNE 6+2 ;IS IT CRAM?
2310 425342 004737 027012 JSR PC,MAPCK ;SKIP TEST IF YES
2311 025346 18: ;CHECK FOR HI OR LO
2312 425346 004737 026656 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2313 425352 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2314 425354 100406 100406 ;START AT ROM PC=0
2315 425356 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2316 425360 115377 1143771<400*2> ;JUMP TO ROM PC OF 1777
2317 425362 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2318 425366 000002 2 ;INDEX
2319 425370 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2320 425372 001401 BEQ 28 ;BR IF YES
2321 425374 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2322 425376 104401 28: SCOP1 ;LOOP TO 16 IF SW09=1
2323 425400 012737 025406 001220 MOV #38,LOCK ;NEW SCOP1
2324 425406 38:
2325 425406 004737 026656 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2326 425412 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2327 425414 100403 100403 ;START AT ROM PC=3
2328 425416 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2329 425420 101000 1000001<400*2> ;JUMP TO ROM PC OF 0
2330 425422 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2331 425426 000010 10 ;INDEX
2332 425430 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?

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2333 425432 001401 BEQ 48 ;BR IF YES
2334 425434 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2335 425436 104401 48: SCOP1 ;LOOP TO 38 IF SW09=1
2336 425440 012737 025446 001220 MOV #58,LOCK ;NEW SCOP1
2337 025446 58:
2338 425446 004737 026656 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2339 425452 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2340 425454 100406 100406 ;START AT ROM PC=6
2341 425456 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2342 425460 105125 1041251<400*2> ;JUMP TO ROM PC OF 525
2343 425462 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2344 425466 000016 16 ;INDEX
2345 425470 020504 CMP R5,R4 ;ARE NEW ROM PC CONTENTS CORRECT?
2346 425472 001401 BEQ 68 ;BR IF YES
2347 425474 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2348 425476 104401 68: SCOP1 ;LOOP TO 58 IF SW59=1
2349 425500 104400 SCOPE ;SCOPE THIS TEST
2350
2351
2352
2353 ;***** TEST 16 *****
2354 ;*CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
2355 ;*CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,
2356 ;*VERIFY THAT THE JUMP DID NOT OCCUR BY READING
2357 ;*THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
2358 ;*****
2359
2360 ; TEST 16
2361 025502 012737 000016 001220 TST16: MOV #16,TSTNO
2362 425510 012737 025676 001216 MOV #TST17,NEXT
2363 425516 012737 025542 001220 MOV #18,LOCK
2364
2365 425524 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2366 425526 032737 100000 001366 BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
2367 425530 001057 BNE 6+2 ;IS IT CRAM?
2368 425536 004737 027012 JSR PC,MAPCK ;SKIP TEST IF YES
2369 425542 18: ;CHECK FOR HI OR LO
2370 425542 004737 026656 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2371 425546 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2372 425550 100406 100406 ;START AT ROM PC=0
2373 425552 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2374 425554 115777 1143771<400*3> ;JUMP TO ROM PC OF 1777
2375 425556 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2376 425562 000002 2 ;INDEX
2377 425564 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2378 425566 001401 BEQ 28 ;BR IF YES
2379 425570 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2380 425572 104401 28: SCOP1 ;LOOP TO 16 IF SW09=1
2381 425574 012737 025602 001220 MOV #38,LOCK ;NEW SCOP1
2382 425602 38:
2383 425602 004737 026656 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2384 425606 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2385 425610 100403 100403 ;START AT ROM PC=3
2386 425612 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2387 425614 101000 1000001<400*3> ;JUMP TO ROM PC OF 0
2388 425616 004737 026750 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA

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2389 025622 000010          10          ;INDEX
2390 025624 020504          CMP          R5,R4      ;ARE NEW PC CONTENTS CORRECT?
2391 025626 001401          BEQ          48          ;BR IF YES
2392 025630 104006          HLT          6          ;ERROR, CROM PC IS WRONG
2393 025632 104401          SCOPI       6          ;LOOP TO 36 IF SW09=1
2394 025634 012737 025642 001220 48:      MOV          #58,LOCK   ;NEW SCOPI
2395 025642
2396 025642 004737 026656 58:      JSR          PC,CLRALL  ;CLEAR ALL CONDITIONS
2397 025646 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2398 025650 100406          100406      ;START AT ROM PC=6
2399 025652 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2400 025654 105525          1041251<400*3> ;JUMP TO ROM PC OF 525
2401 025656 004737 026750 JSR          PC,ROMDAT  ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2402 025662 000016          16          ;INDEX
2403 025664 020504          CMP          R5,R4      ;ARE NEW ROM PC CONTENTS CORRECT?
2404 025666 001401          BEQ          68          ;BR IF YES
2405 025670 104006          HLT          6          ;ERROR, CROM PC IS WRONG
2406 025672 104401          SCOPI       6          ;LOOP TO 56 IF SW59=1
2407 025674 104400          SCOPE      ;SCOPE THIS TEST
2408
2409
2410
2411 ;***** TEST 17 *****
2412 ;*CROM TEST OF JUMP(I) ON BR0 SET MICRO-PROCESSOR INSTRUCTION.
2413 ;*CLEAR THE BR0 BIT, PERFORM THE JUMP INSTRUCTION,
2414 ;*VERIFY THAT THE JUMP DID NOT OCCUR BY READING
2415 ;*THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
2416 ;*****
2417 ; TEST 17
2418 ;-----
2419 025676 012737 000017 001226 TST17:    MOV          #17,TSTNO
2420 025704 012737 026072 001216      MOV          #TST20,NEXT
2421 025712 012737 025736 001220      MOV          #18,LOCK
2422
2423 025720 104412          MSTCLR     ;R1 CONTAINS BASE DMC11 ADDRESS
2424 025722 032737 100000 001366      BIT          #BIT15,STAT1 ;MASTER CLEAR DMC11
2425 025730 001057          BNE          68+2      ;IS IT CROM?
2426 025732 004737 027012          JSR          PC,MAPCK  ;SKIP TEST IF YES
2427 025736
2428 025736 004737 026656 18:      JSR          PC,CLRALL  ;CLEAR ALL CONDITIONS
2429 025742 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2430 025744 100400          100400      ;START AT ROM PC=6
2431 025746 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2432 025750 116377          1143771<400*4> ;JUMP TO ROM PC OF 1777
2433 025752 004737 026750 JSR          PC,ROMDAT  ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2434 025756 000002          2          ;INDEX
2435 025760 020504          CMP          R5,R4      ;ARE NEW PC CONTENTS CORRECT?
2436 025762 001401          BEQ          28          ;BR IF YES
2437 025764 104006          HLT          6          ;ERROR, CROM PC IS WRONG
2438 025766 104401          SCOPI       6          ;LOOP TO 18 IF SW09=1
2439 025770 012737 025776 001220 28:      MOV          #38,LOCK   ;NEW SCOPI
2440 025776
2441 025776 004737 026656 38:      JSR          PC,CLRALL  ;CLEAR ALL CONDITIONS
2442 026002 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2443 026004 100403          100403      ;START AT ROM PC=3
2444 026006 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

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2445 026010 102000          1000001<400*4> ;JUMP TO ROM PC OF 0
2446 026012 004737 026750 JSR          PC,ROMDAT  ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2447 026016 000010          10          ;INDEX
2448 026020 022504          CMP          R5,R4      ;ARE NEW PC CONTENTS CORRECT?
2449 026022 001401          BEQ          48          ;BR IF YES
2450 026024 104006          HLT          6          ;ERROR, CROM PC IS WRONG
2451 026026 104401          SCOPI       6          ;LOOP TO 36 IF SW09=1
2452 026030 012737 026036 001220 48:      MOV          #56,LOCK   ;NEW SCOPI
2453 026036
2454 026036 004737 026656 56:      JSR          PC,CLRALL  ;CLEAR ALL CONDITIONS
2455 026042 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2456 026044 100406          100406      ;START AT ROM PC=6
2457 026046 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2458 026050 106125          1041251<400*4> ;JUMP TO ROM PC OF 525
2459 026052 004737 026750 JSR          PC,ROMDAT  ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2460 026056 000016          16          ;INDEX
2461 026060 020504          CMP          R5,R4      ;ARE NEW ROM PC CONTENTS CORRECT?
2462 026062 001401          BEQ          68          ;BR IF YES
2463 026064 104006          HLT          6          ;ERROR, CROM PC IS WRONG
2464 026066 104401          SCOPI       6          ;LOOP TO 56 IF SW59=1
2465 026070 104400          SCOPE      ;SCOPE THIS TEST
2466
2467
2468 ;***** TEST 20 *****
2469 ;*CROM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
2470 ;*CLEAR THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,
2471 ;*VERIFY THAT THE JUMP DID NOT OCCUR BY READING
2472 ;*THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
2473 ;*****
2474 ; TEST 20
2475 ;-----
2476
2477 026072 012737 000020 001220 TST20:    MOV          #20,TSTNO
2478 026100 012737 026266 001216      MOV          #TST21,NEXT
2479 026106 012737 026132 001220      MOV          #16,LOCK
2480
2481 026114 104412          MSTCLR     ;R1 CONTAINS BASE DMC11 ADDRESS
2482 026116 032737 100000 001366      BIT          #BIT15,STAT1 ;MASTER CLEAR DMC11
2483 026120 001057          BNE          68+2      ;IS IT CROM?
2484 026126 004737 027012          JSR          PC,MAPCK  ;SKIP TEST IF YES
2485 026132
2486 026132 004737 026656 18:      JSR          PC,CLRALL  ;CLEAR ALL CONDITIONS
2487 026136 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2488 026140 100400          100400      ;START AT ROM PC=6
2489 026142 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2490 026144 116777          1143771<400*5> ;JUMP TO ROM PC OF 1777
2491 026146 004737 026750 JSR          PC,ROMDAT  ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2492 026152 000002          2          ;INDEX
2493 026154 020504          CMP          R5,R4      ;ARE NEW PC CONTENTS CORRECT?
2494 026156 001401          BEQ          28          ;BR IF YES
2495 026160 104006          HLT          6          ;ERROR, CROM PC IS WRONG
2496 026162 104401          SCOPI       6          ;LOOP TO 18 IF SW09=1
2497 026164 012737 026172 001220 28:      MOV          #38,LOCK   ;NEW SCOPI
2498 026172
2499 026172 004737 026656 38:      JSR          PC,CLRALL  ;CLEAR ALL CONDITIONS
2500 026176 104414          ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

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2501 026200 100403 ;START AT ROM PC=3
2502 026202 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2503 026204 102400 ;START AT ROM PC=0
2504 026206 004737 026750 ;JUMP TO ROM PC OF 0
2505 026210 000010 ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2506 026214 020504 ;INDEX
2507 026216 001401 ;ARE NEW PC CONTENTS CORRECT?
2508 026220 104006 ;BR IF YES
2509 026222 104401 ;ERROR, CROM PC IS WRONG
2510 026224 012737 026232 001220 ;LOOP TO 36 IF SW09=1
2511 026232 ;NEW SCOPI
2512 026232 004737 026656 ;CLEAR ALL CONDITIONS
2513 026236 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2514 026240 100406 ;START AT ROM PC=6
2515 026242 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2516 026244 106525 ;START AT ROM PC=6
2517 026246 004737 026750 ;JUMP TO ROM PC OF 525
2518 026252 000016 ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2519 026254 020504 ;INDEX
2520 026256 001401 ;ARE NEW ROM PC CONTENTS CORRECT?
2521 026260 104006 ;BR IF YES
2522 026262 104401 ;ERROR, CROM PC IS WRONG
2523 026264 104400 ;LOOP TO 56 IF SW59=1
2524 ;SCOPE THIS TEST
2525
2526 ;***** TEST 21 *****
2527 ;CROM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
2528 ;CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
2529 ;VERIFY THAT THE JUMP DID NOT OCCUR BY READING
2530 ;THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
2531 ;*****
2532
2533 ; TEST 21
2534 ;-----
2535 026266 012737 000021 001226 TST21: MOV #21,TSTNO
2536 026274 012737 026462 001216 MOV #TST2,NEXT
2537 026302 012737 026326 001220 MOV #18,LOCK
2538
2539 026310 104412 ;R1 CONTAINS BASE DMC11 ADDRESS
2540 026312 032737 100000 001366 ;MASTER CLEAR DMC11
2541 026320 001057 ;IS IT CRAM?
2542 026322 004737 027012 ;SKIP TEST IF YES
2543 026326 ;CHECK FOR HI OR LO
2544 026326 004737 026656 ;CLEAR ALL CONDITIONS
2545 026332 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2546 026334 100400 ;START AT ROM PC=0
2547 026336 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2548 026340 117377 ;JUMP TO ROM PC OF 1777
2549 026342 004737 026750 ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2550 026346 000002 ;INDEX
2551 026350 020504 ;ARE NEW PC CONTENTS CORRECT?
2552 026352 001401 ;BR IF YES
2553 026354 104006 ;ERROR, CROM PC IS WRONG
2554 026356 104401 ;LOOP TO 16 IF SW09=1
2555 026360 012737 026366 001220 ;NEW SCOPI
2556 026366 ;SCOPE
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2557 026366 004737 026656 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2558 026372 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2559 026374 100403 ;START AT ROM PC=3
2560 026376 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2561 026400 103000 ;START AT ROM PC=0
2562 026402 004737 026750 ;JUMP TO ROM PC OF 0
2563 026406 000010 ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2564 026410 020504 ;INDEX
2565 026412 001401 ;ARE NEW PC CONTENTS CORRECT?
2566 026414 104006 ;BR IF YES
2567 026416 104401 ;ERROR, CROM PC IS WRONG
2568 026420 012737 026426 001220 ;LOOP TO 30 IF SW09=1
2569 026426 ;NEW SCOPI
2570 026426 009137 020050 ;CLEAR ALL CONDITIONS
2571 026432 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2572 026434 100406 ;START AT ROM PC=6
2573 026436 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2574 026440 107125 ;JUMP TO ROM PC OF 525
2575 026442 004737 026750 ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2576 026446 000016 ;INDEX
2577 026450 020504 ;ARE NEW ROM PC CONTENTS CORRECT?
2578 026452 001401 ;BR IF YES
2579 026454 104006 ;ERROR, CROM PC IS WRONG
2580 026456 104401 ;LOOP TO 55 IF SW59=1
2581 026460 104400 ;SCOPE THIS TEST
2582
2583 ;***** TEST 22 *****
2584 ;CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
2585 ;CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,
2586 ;VERIFY THAT THE JUMP DID NOT OCCUR BY READING
2587 ;THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
2588 ;*****
2589
2590 ; TEST 22
2591 ;-----
2592
2593 026462 012737 000022 001226 IST22: MOV #22,TSTNO
2594 026470 012737 003364 001216 MOV #EOP,NEXT
2595 026476 012737 026522 001220 MOV #18,LOCK
2596
2597 026504 104412 ;R1 CONTAINS BASE DMC11 ADDRESS
2598 026506 032737 100000 001366 ;MASTER CLEAR DMC11
2599 026514 001057 ;IS IT CRAM?
2600 026516 004737 027012 ;SKIP TEST IF YES
2601 026522 ;CHECK FOR HI OR LO
2602 026522 004737 026656 ;CLEAR ALL CONDITIONS
2603 026526 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2604 026530 100400 ;START AT ROM PC=0
2605 026532 104414 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2606 026534 117777 ;JUMP TO ROM PC OF 1777
2607 026536 004737 026750 ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2608 026542 000002 ;INDEX
2609 026544 020504 ;ARE NEW PC CONTENTS CORRECT?
2610 026546 001401 ;BR IF YES
2611 026550 104006 ;ERROR, CROM PC IS WRONG
2612 026552 104401 ;LOOP TO 16 IF SW09=1
2613 ;SCOPE
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2613 026554 012737 026562 001220      MOV     #3,LOCK      ;NEW SCOPI
2614 026562
2615 026562 004737 026656      35:    JSR     PC,CLRALL   ;CLEAR ALL CONDITIONS
2616 026566 104414      ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2617 026570 100403      100403 ;START AT ROM PC=3
2618 026572 104414      ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2619 026574 103400      1000001<400*7> ;JUMP TO ROM PC OF 0
2620 026576 004737 026750      JSR     PC,ROMDAT   ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2621 126602 000010      10      ;INDEX
2622 026604 020504      CMP     R5,R4      ;ARE NEW PC CONTENTS CORRECT?
2623 026606 001401      BEQ     48          ;BR IF YES
2624 026610 104006      HLT     6           ;ERROR, CROM PC IS WRONG
2625 026612 104401      45:    SCOP1 ;LOOP TO 35 IF SW09=1
2626 026614 012737 026622 001220      MOV     #5,LOCK      ;NEW SCOPI
2627 026622
2628 026622 004737 026656      55:    JSR     PC,CLRALL   ;CLEAR ALL CONDITIONS
2629 026626 104414      ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2630 026630 100406      100406 ;START AT ROM PC=6
2631 026632 104414      ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2632 026634 107525      1041251<400*7> ;JUMP TO ROM PC OF 525
2633 026636 004737 026750      JSR     PC,ROMDAT   ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2634 026642 000016      16      ;INDEX
2635 026644 020504      CMP     R5,R4      ;ARE NEW ROM PC CONTENTS CORRECT?
2636 026646 001401      BEQ     68          ;BR IF YES
2637 026650 104006      HLT     6           ;ERROR, CROM PC IS WRONG
2638 026652 104401      65:    SCOP1 ;LOOP TO 55 IF SW59=1
2639 026654 104400      SCOPE  ;SCOPE THIS TEST

2640 00300
2641 00400
2642 00500 ;SUBROUTINES
2643 00600 ;-----
2644 00700
2645 026656 CLRALL: ;THIS SUBROUTINE CLEARS THE C&Z BITS AND THE BR
2646 00900
2647 01000
2648 026656 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2649 026660 000400 ;BR_0
2650 026662 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2651 026664 003220 053220 ;SP(0)-BR
2652 026666 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2653 026670 000400 060400 ;BR_SP(0)+BR
2654 026672 000207
2655 01700
2656 01800
2657 026674 SETBR0: ;THIS SUBROUTINE SETS BR0 BIT
2658 02100
2659 02200
2660 026674 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2661 026675 000401 000401 ;BR_001
2662 026700 000207
2663 02600
2664 02700
2665 026702 SETBR1: ;THIS SUBROUTINE SETS BR1 BIT
2666 02900
2667 03000
2668 026702 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
  
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2669 026704 000402 03200 020402 ;BR_002
2670 026706 000207 03300
2671 03400
2672 03500
2673 026710 SETBR4: ;THIS SUBROUTINE SETS BR4 BIT
2674 03600
2675 03700
2676 026710 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2677 026712 000420 04000 000420 ;BR_020
2678 026714 000207 04100
2679 04200
2680 04300
2681 026716 SETBR7: ;THIS SUBROUTINE SETS BR7 BIT
2682 04400
2683 04500
2684 026716 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2685 026720 000600 04800 000600 ;BR_200
2686 026722 000207 04900
2687 05000
2688 05100
2689 026724 SETC: ;THIS SUBROUTINE SETS THE C BIT
2690 05200
2691 05300
2692 05400
2693 026724 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2694 026726 000777 05600 000777 ;BR_377
2695 026730 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2696 026732 003220 05800 053220 ;SP(0)-BR
2697 026734 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2698 026736 000400 06000 060400 ;BR_SP(0)+BR
2699 000207 06100
2700 06200
2701 026742 SETZ: ;THIS SUBROUTINE SETS THE Z BIT
2702 06300
2703 06400
2704 026742 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2705 026744 000777 06800 000777 ;BR_377
2706 026746 000207 06900
2707 07000
2708 07100
2709 026750 ROMDAT: ;THIS SUBROUTINE LOADS R5 WITH EXPECTED ROM CONTENTS
2710 07200 ;AND LOADS R4 WITH ACTUAL ROM CONTENTS
2711 07300
2712 07400
2713 026750 017600 000000 MOV     0(SP),R0 ;INDEX FOR COMPARE
2714 026754 002716 000002 AND     #2,(SP) ;ADJUST STACK
2715 026760 012711 002000 MOV     #BIT10,(R1) ;SET ROM0
2716 026764 016005 007900 MOV     LOMAP(R0),R5 ;PUT EXPECTED IN R5 (LOSPEED)
2717 026770 032737 000002 001372 BIT     #BIT1,STAT3 ;LOW OR HIGH SPEED?
2718 026776 001402 001000 BEQ     18          ;BR IF LOW SPEED
2719 027000 016005 016322 MOV     HIMAP(R0),R5 ;PUT EXPECTED IN R5 (HISPEED)
2720 027004 016104 000006 1S:    MOV     6(R1),R4 ;PUT "FOUND" IN R4
2721 027010 000207 HTS     PC ;RETURN
2722 02500
2723 027012 MAPCK:
2724 02700 ;THIS SUBROUTINE CHECKS THE STATUS TABLE AND LOADS
  
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```
2725          08800          ;THE ROMMAP POINTER TO POINT TO EITHER THE HIGH OR
2726          08900          ;LOW SPEED MICRO-CODE.
2727          09000
2728 027012 012737 012322 012320 09100      MOV  #L0MAP,ROMMAP    ;LOAD POINTER TO LOW SPEED
2729 027020 032737 000002 001372 09200      BIT  #BIT1,STAT3     ;CHECK STATUS TABLE
2730 027026 001403          09300      BEQ  16               ;BR IF LOW SPEED
2731 027030 012737 016322 012320 09400      MOV  #H1MAP,ROMMAP    ;LOAD POINTER TO HIGH SPEED
2732 027036 000207          09500      RTS   PC              ;RETURN
2733          09600
2734          00300
027040 041777 040522 020115 00400      EM1:  .ASCIZ <37>/CRAM DATA ERROR/
027061 377 051103 046501 00500      EM2:  .ASCIZ <37>/CRAM DUAL ADDRESSING ERROR/
027115 377 051103 046517 00600      EM3:  .ASCIZ <37>/CRAM DATA ERROR/
027136 045377 046525 020120 00700      EM4:  .ASCIZ <37>/JUMP ERROR/
027152 047777 052104 042440 00800      EM5:  .ASCIZ <37>/ODT ERROR IN IBUS* REG10/
027204 044777 050117 046440 00900      EM7:  .ASCIZ <37>/IOP MAR TEST/
027222 041377 020122 044522 01000      EM10: .ASCIZ <37>/BR RIGHT SHIFT TEST/
027247 377 042522 042503 01100      EM11: .ASCIZ <37>/RECEIVE DATA ERROR/
027273 377 051106 042505 01200      EM12: .ASCIZ <37>/FREE RUNNING ERROR/
027317 377 047503 052116 01300      EM13: .ASCIZ <37>/CONTROL OUT ERROR/
          01400
027342 042777 050130 041505 01500      DH1:  .ASCIZ <37>/EXPECTED FOUND ADDRESS/
027374 042777 050130 041505 01600      DH2:  .ASCIZ <37>/EXPECTED FOUND/
027415 377 051440 046105 01700      DH3:  .ASCIZ <37>/SEL4 SEL6/
          01800
          01900
          02000      DT1:  3
027436 000003          02100      .BYTE 6,4
027440 006 004 02200      SAVR2
027442 001264          02300      .BYTE 6,4
027444 006 004 02400      SAVR4
027446 001270          02500      .BYTE 4,2
027450 004 002 02600      SAVR0
027452 001260          02700      DT2:  3
027454 000003          02800      .BYTE 6,4
027456 006 004 02900      SAVR5
027460 001272          03000      .BYTE 6,4
027462 006 004 03100      SAVR4
027464 001270          03200      .BYTE 4,2
027466 004 002 03300      SAVR2
027470 001264          03400      DT3:  3
027472 000003          03500      .BYTE 6,4
027474 006 004 03600      SAVR5
027476 001272          03700      .BYTE 6,4
027500 006 004 03800      SAVR4
027502 001270          03900      .BYTE 4,2
027504 004 002 04000      TEMP3
027506 001252          04100      DT4:  2
027510 000002          04200      .BYTE 3,7
027512 003 007 04300      SAVR5
027514 001272          04400      .BYTE 3,2
027516 003 002 04500      SAVR4
027520 001270          04600      DT5:  2
027522 000002          04700      .BYTE 6,4
027524 006 004 04800      SAVR5
027526 001272          04900      .BYTE 6,2
027530 006 002 05000
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027532 001270          05100      SAVR4
027534 000003          05200      DT7:  3
027536 003 010 05300      .BYTE 3,10
027540 001272          05400      SAVR5
027542 003 004 05500      .BYTE 3,4
027544 001270          05600      SAVR4
027546 004 002 05700      .BYTE 4,2
027550 001264          05800      SAVR2
027552 000003          05900      DT10: 3
027554 003 007 06000      .BYTE 3,7
027556 001272          06100      SAVR5
027560 003 004 06200      .BYTE 3,4
027562 001270          06300      SAVR4
027564 006 002 06400      .BYTE 5,2
027566 001252          06500      TEMP3
027570 000002          06600      DT11: 2
027572 006 004 06700      .BYTE 6,4
027574 001252          06800      TEMP3
027576 006 002 06900      .BYTE 6,2
027600 001254          07000      TEMP4
          07100      .ERRTAB:
          07200      0
          07300      0
          07400      0
          07500      EM1
027612 027342          07600      DH1  ;HLT  1
027614 027436          07700      DT1
027616 027061          07800      EM2
027620 027342          07900      DH1  ;HLT  2
027622 027436          08000      DT1
027624 027040          08100      EM1
027626 027342          08200      DH1  ;HLT  3
027630 027454          08300      DT2
027632 027115          08400      EM3
027634 027342          08500      DH1  ;HLT  4
027636 027472          08600      DT3
027640 027136          08700      EM4
027642 027374          08800      DH2  ;HLT  5
027644 027510          08900      DT4
027646 027136          09000      EM4
027650 027374          09100      DH2  ;HLT  6
027652 027522          09200      DT5
027654 027152          09300      EM5
027656 027374          09400      DH2  ;HLT  7
027660 027510          09500      DT4
027662 004000          09600      0
027664 000000          09700      0
027666 000000          09800      0
027670 027204          09900      EM7
027672 027342          10000      DH1  ;HLT  11
027674 027534          10100      LT7
027676 027222          10200      L410
027700 027374          10300      DH2  ;HLT  12
027702 027510          10400      DT4
027704 027247          10500      L411
```













DMEND	1#	725																
DMFRNT	1#																	
HLI	75#	1754	1764	1827	1867	1880	1893	1923	1935	1947	1978	1991	2004	2035	2048			
		2061	2092	2105	2118	2149	2162	2175	2206	2219	2232	2263	2276	2289	2321	2334		
		2347	2379	2392	2405	2437	2450	2463	2495	2508	2521	2553	2566	2579	2611	2624		
		2637																
SAUTO	1#	547																
SBRSSH	1#	1725																
SBUFFE	1#	1199																
SCOMF	1#																	
SCRAM	1#	1694																
SCYCLE	1#	1271																
SEOF	1#	725																
SFINI	1#	2640																
SGETPA	1#																	
SHEADE	1#																	
SJUMP	1#	1830	1896	1950	2007	2064	2121	2178	2235	2292	2350	2400	2466	2524	2582			
SMARHI	1#																	
SNOCK	1#																	
SMSG	1#	1187																
SPFAIL	1#	1103																
SQUEST	1#	1381	1394	1403	1482	1491												
SRANCL	1#	1131																
SRCCLK	1#	1134	1137	1174	1179	1744	1746	1748	1755	1758	1814	1859	1861	1872	1874			
		1885	1887	1915	1917	1927	1929	1939	1941	1970	1972	1983	1985	1996	1998	2027		
		2029	2040	2042	2053	2055	2084	2086	2097	2099	2110	2112	2141	2143	2154	2156		
		2167	2169	2198	2200	2211	2213	2224	2226	2255	2257	2268	2270	2281	2283	2313		
		2315	2326	2328	2339	2341	2371	2373	2384	2386	2397	2399	2429	2431	2442	2444		
		2455	2457	2487	2489	2500	2502	2513	2515	2545	2547	2558	2560	2571	2573	2603		
		2605	2616	2618	2629	2631	2648	2650	2652	2660	2668	2676	2684	2692	2694	2696		
		2704																
SROMNU	1#	1673																
SROMRD	1#	1766																
SSCOPE	1#	775																
SSIMBC	1#																	
SSOFTC	1#	1207																
STRPDE	1#	215	217	219	221	223	225	227	229	231	233	235	237	239	241			
		243																
STSTN	1#	1683	1706	1733	1797	1847	1904	1950	2015	2072	2129	2186	2243	2301	2359			
		2417	2475	2533	2591													
SVARIA	1#	134																
SXZ	1#	1673	1681	1694	1704	1725	1731	1766	1795	1838	1845	1896	1902	1950	1956			
		2007	2013	2064	2070	2121	2127	2178	2184	2235	2241	2292	2299	2350	2357	2408		
		2415	2466	2473	2524	2531	2582	2589										

. ABS. 027734 000

ERRORS DETECTED: 0

DZDMG,DZDMG/SOL/CRF\_IPLUTL,DZDMG  
 RUN-TIME: 10 13 1 SECONDS  
 RUN-TIME RATIO: 167/24=6.8  
 CORE USED: 21K (41 PAGES)