IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZKWC-C-D

PRODUCT NAME: KW11W LOGIC TEST

DATE CREATED: SEPTEMBER 1, 1974

MAINTAINER: IPC CUSTOM SYSTEMS

AUTHOR: RAYMOND BALDWIN

AH

MEMORY STORAGE - 00000 - 012000 OCTAL

LOADING PROCEDURE - (PAPER TAPE SUPPLIED) LOADED USING NORAML
BINARY PROCEDURE.

STARTING PROCEDURE:
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STARTING ADDRESS 200:

FOR NON-STANDARD VECTORS, DEVICE ADDRESSES & PRIORITY INTERRUPT
LEVELS, THE PROGRAM WILL ASK THE FOLLOWING QUESTIONS TO WHICH
THE OPERATOR MUST RESPOND:

FIRST DEVICE ADDRESS - (6 CHARACTERS)
FIRST INT. VECTOR - (3 CHARACTERS)
PRIORITY INT. LEVEL - (INPUT INT. LEVEL OF DEVICE 4-7)
PDP-11 (A)=05,10,20 (B)=35,40 (C)=45,50

IF AN ERROR IS ENCOUNTERED WHILE INPUTING THE DEVICE ADDRESS
OR INT. VECTOR, THE OPERATOR MAY TYPE A RUB OUT AND REPEAT
ENTIRE LINE INPUTING. WHEN LINE IS COMPLETE OR IF NO CHANGES
(FROM STANDARD DEVICE) THE OPERATOR MUST TERMINATE THE LINE
WITH A CARRIAGE RETURN.

STARTING ADDRESS 1000:
****

DIRECT STARTING OR RESTARTING OF LOGIC TEST.

STARTING ADDRESS 220:
****

DIRECT STARTING OR RESTARTING OF DELAY ADJUSTMENT TEST.

STARTING ADDRESS 240:
****

DIRECT STARTING OR RESTARTING OF DYNAMIC SYSTEM TEST.

LOGIC TEST OPERATING PROCEDURE AND DESCRIPTION
****

THE LOGIC TEST CONSISTS OF 44 SUB TESTS EACH CONTAINING AN ERROR ROUTINE. LOGIC TEST SHOULD BE STARTED WITH ALL CONSOLE (PDP-11) SWITCHES DOWN. IF AN ERROR IS ENCOUNTERED, THE TELETYPE WILL REPORT WITH FAILING TEST AND HALT. TO LOOP ON A FAILURE CONSOLE SWITCH REGISTER, BIT 14 IS RAISED AND THE TEST IS LOOPED BY DEPRESSING THE CONTINUE KEY. TO INHIBIT THE ERROR TYPING RAISE SWITCH REGISTER BIT 13.

LOGIC TEST REQUIREMENTS:
****

TO RUN THE LOGIC TEST, THE SUPPLIED TEST PLUG MUST BE CONNECTED TO THE MODULE CONNECTOR. THE T3 DELAY MUST EXCEED T2 BY 50 MICRO-SECONDS. THE ADJUSTMENT OF T1 MUST BE SET AT A MINIMUM.

LOGIC TEST ERROR REPORTS.
****

TEST	FAILURE
T1	STATUS AND CONTROL REG. NOT CLEAR UPON INITIALIZE.
T2	INT. ENABLE BIT 6 OF CSR NOT SET.
T3	INT. ENABLE BIT 6 OF CSR NOT CLEAR.
T4	AN ILLEGAL INT. IS PRESENT FROM THE MODULE.
T5	AN ILLEGAL INT. IS PRESENT AFTER A DELAY TIME OUT.
T6	STATUS REGISTER NOT CLEAR AFTER DELAY TIME OUT.
T7	STATUS REGISTER WAS AFFECTED BY A CLEAR FLAGS INSTRUCTION.
T8	FAILED TO MONITOR A T2 FLAG.
T9	ALARM RECEIVED BIT 14 OF CSR SET WITHOUT AN EXT. ENABLE.
T10	ALARM RECIEVE FLAG FAILED TO SET AFTER ENABLING THE EXTERNAL WORLD.
T11	T2 FLAG FAILED TO CLEAR.
T12	RECIEVE FLAG FAILED TO CLEAR.
T13	SHORT LOOP (T1) FAILED TO CLEAR.
T14	T2 FLAG SET SHOULD HAVE BEEN TERMINATED BY THE LOCK FLOP UPON THE SHORT LOOP GENERATED IN T13.
T15	RECEIVE FLAG WAS SET UPON A SHORT LOOP WITHOUT THE EXTERNAL ENABLE.
T16	LOCK FLOP FAILED TO CLEAR UPON ENABLING THE EXTERNAL WORLD AND WAITING 5M.SEC. FOR CLEAR ERROR.
T17	NO ERROR CHECKING, CONDITIONING FOR T18, T19, AND T20.
T18	T1 FLAG FAILED TO CLEAR.
T19	T2 FLAG FAILED TO CLEAR.
T20	RECEIVE FLAG FAILED TO CLEAR.
T21	RECEIVE FLAG FAILED TO SET UPON A TIME OUT OF T3.
T22	ALARM REC. FLAG FAILED TO CLEAR.
T23	ENABLE FLOP NOT CLEARED AN ALARM OUT.
T24	A T2 FLAG FAILED TO RAISE AN INT. AT VECTOR 350.
T25	SHORT LOOP FLAG FAILED TO RAISE AN INT. AT VECTOR 350.

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T26     ALARM REC. FLAG FAILED TO RAISE AN INT. AT VECTOR 352.
T27     SHORT LOOP "LOCK" FAILED TO TERMINATE T3.
T28     SHORT LOOP "LOCK" FAILED TO TERMINATE T2.
T29     THE CLEARING OF "LOCK" DIDNOT RELEASE T2 TO THE
        BUS (REFER TO T26,T27, &T28).
T30     SHORT LOOP " LOCK"FAILED TO LOCK PULSING OF TIMER.
T31     INITIALIZE FAILED TO CLEAR SHORT LOOP FLAG.
T32     INITIALIZE FAILED TO CLEAR RECEIVE FLAG.
T33     INITIALIZE FAILED TO CLEAR THE LOCK FLOP.
T34     INITIALIZE FAILED TO TERMINATE T3.
T35     INITIALIZE FAILED TO TERMINATE T2.
T36     INCORRECT STATUS IN EXTERNAL STATUS REG.
T37     STATUS OF ECSR CHANGED UPON A RESET INSTRUCTION.
T38     SWITCH BUS INSTRUCTION FAILED TO CHANGE THE EXTERNAL
        STATUS REGISTER.
T39     THE LATCH FAILED TO PREVENT A 2ND BUS SWITCHING
        (REFER TO T38).
T40     BUS FAILED TO SWITCH TO 2ND LATCH.
T41     TERMINATION OF T3 FAILED TO RELEASE THE LATCH.
T42     A SWITCH BUS COMMAND FAILED TO CHANGE THE BUS STATUS.
T43     A RESET INSTRUCTION FAILED TO CLEAR THE LATCH.
T44     MANUAL ENABLE INPUT FAILED.
**********************************
T38S    TEST FOLLOWED BY AN "S" DENOTES SUBTEST.
T40S    WHICH IS A FAILURE OF THE EXTERNAL STATUS
T41S    REGISTER (STATUS READ IS INCORRECT).
T43S
```

ALL TESTS MUST BE SUCCESSFULLY COMPLETED BEFORE THE NEXT TEST MAY BE EXECUTED.

UPON SUCCESSFUL COMPLETION OF THE LOGIC TEST, THE TELETYPE WILL PRINT "PASS".

FOR SCOPING ERRORS, SWITCH REGISTER BIT 7 MAY BE RAISED TO INCREASE THE TEST REPEATIBILITY RATE.

DELAY ADJUSTMENT TESTS.
****

THE OPERATOR MUST RESPOND TO THE QUESTION, "(1) WATCHDOG, (2)
WARNING & SHORT LOOP" BY TYPING A 1 OR A 2 FOR DESIRED
ADJUSTMENT LOOP TO BE RUN.

DYNAMIC SYSTEM TEST.
****

THIS TEST IS INTENDED AS AN EXCERSER WHICH SHOULD BE RUN ONLY AFTER
COMPLETING THE LOGIC TEST.

THE TEST EXERCISES THE INTERRUPT LOGIC, EXTERNAL STATUS AND
DELAYS.

THE TIMER IS PRIMED BY PULSING THE DELAYS AND ENABLING THE
INTERRUPT. THE ONLY LEGAL INTERRUPTS ARE THOSE FROM THE T2
DELAY. AFTER EACH LEGAL INTERRUPT, THE EXTERNAL STATUS IS
SWITCHED AND TESTED FOR A CORRECT STATUS READING.

A "PASS" IS PRINTED AFTER 100 SUCCESSFUL INTERRUPTS.
POSSIBLE ERRORS REPORTED ARE:

1. SHORT LOOP FLAG SET
2. EXTERNAL STATUS BAD
3. ILLEGAL INTERRUPT

TO EXIT ANY TEST, RAISE CONSOLE SWITCH REGISTER,BIT 00,
THE PROGRAM WILL THEN OUTPUT THE HEADER, MAKE SURE THAT
THE SWITCH IS LOWERED BEFORE ENTERING A NEW TEST.

****
END

```
                                .TITLE WATCH DOG TIMER
                                .ENABL AMA ABS

                        ;
                        ;
                        ;LOGIC TEST FOR WATCH DOG TIMER (HARDWARE MONITOR)
                        ;FOR PDP-11 SYSTEMS.
                        ;THE WATCH DOG TIMER MUST BE PULSED FROM THE
                        ;COMPUTER PROGRAM WITHIN A SPECIFIED TIME TO
                        ;INHIBIT THE TIMER FROM TIMING OUT.  UPON A TIME
                        ;OUT CONDITION THE WATCH DOG WILL POST AN
                        ;INTERRUPT ALLOWING THE PROCESSOR A CHANCE TO
                        ;RECOVER BEFORE A SECOND TIME OUT CONDITION
                        ;OCCURS ISSUING AN "ALARM OUT" TO THE EXTERNAL
                        ;WORLD.  THE WARNING INTERRUPT IS SENSED AT
                        ;BIT 07 OF THE CONTROLL AND STATUS REGISTER.
                        ;THE TIMER ALSO HAS A "SHORT LOOP" PROTECTION WHICH
                        ;GUARDS AGAINST A PROGRAM FAILURE THAT MAYBE PULSING THE
                        ;TIMER BEFORE A SPECIFIED INTERVAL.  THE SHORT LOOP WILL
                        ;POST AN INTERRUPT ALSO AT VECTOR (XXX) WHENEVER PULSED
                        ;TWICE WITHIN A SPECIFIED TIME INTERVAL.  THE SHORT LOOP
                        ;INTERRUPT IS SENSED IN THE STATUS REGISTER BY BIT 14.
                        ;THE RECEIVE CIRCUIT ALLOWS FOR AN INTERRUPT (VECTOR XXX) TO BE
                        ;POSTED WHEN AN "ALARM SIGNAL" IS RECEIVED FROM THE
                        ;EXTERNAL WORLD.  THE RECEIVE INTERRUPT IS SENSED AT
                        ;BIT 7 OF THE STATUS REGISTER.

                        ;
                        ;FOR TEST PURPOSES THE "ALARM OUT" SIGNAL IS
                        ;JUMPERED TO THE ALARM RECEIVE WITH A SUPPLIED
                        ;TEST PATCH.
                                ;
                                ;
                                ;DIGITAL EQUIPMENT CORP.
                                ;INDUSTRIAL PRODUCTS GROUP
                                ;WATCH DOG TIMER LOGIC TEST
                                ;MAINDEC-11-DZKWC-C
                                ;AUTHOR: RAY,BALDWIN
                                ;MAINTAINER: IPG:CUSTOM SYSTEMS
                                ;COPYRIGHT:DIGITAL 1973
                                ;
                                ;
 177776                         PS=177776
 177562                         TKB=177562              ;TELETYPE READER BUFFER
 177560                         TKS=177560              ;TELETYPE READER STATUS
 177566                         TYDB=177566             ;TELETYPE PRINTER BUFFER
 177564                         TYSR=177564             ;TELTYPE PRINTER STATUS
 172400                         CSR=172400              ;CONTROLL AND STATUS-WATCHDOG
 172402                         CINT=172402             ;INTERRUPT CLR INSTRUCTION
 172404                         ECSR=172404             ;EXTERNAL CSR
 172406                         SWBU=172406             ;SWITCH BUS
 177570                         SR=177570               ;SWITCH REGISTER
 104000                         NULL=104000
 000240                         NOP=240
```

G1

WATCH.SRC

```
                000000          HLT=0
                000000          R0=%0
                000001          R1=%1
                000002          R2=%2                   ;SUBROUTINE RETAIN
                000003          R3=%3                   ;TELTYPE ROUTINE RETAIN
                000004          R4=%4                   ;TIME CONTROL ROUTINES
                000005          R5=%5                   ;ERROR PRINT & SCOPE MODE
                000006          SP=%6
                000007          PC=%7
                                ;LOAD TRAP CATCHER
```

```
                        000020                  .=8
                                                .REPT   10
                                                .+2
                                                HLT                     ;TRAPPED TO PREVIOUS VECTOR
                                                .ENDR
                                                ;
                        000004                  .=4
000004  007466                                  TOBE            ;TIME OUT BUSS ERROR
000006  000340                                  340             ;PROCESSOR STATUS
                        000030                  .=30
000030  010430                                  NULPRT
000032  000340                                  340
                                                ;
                                                ;
                                                ;
                        000350                  .=350                   ;WATCH DOG INTERRUPT
000350  007362                                  WADG
000352  000340                                  340                     ;SET PROCESSOR STATUS BACK TO 7
000354  007372                                  RECF                    ;RECEIVE FLAG VECTOR
000356  000340                                  340
                                                ;
                                                ;
                                                ;
                        000500                  .=500
000500  172400                  XCSR:   CSR
000502  172402                  XCINT:  CINT
000504  172404                  XECSR:  ECSR
000506  172406                  XSWBU:  SWBU
000510  000300                  PRIV:   300     ;PRIORITY LEVEL
                                                ;
                                                ;
                        000600                  .=600
000600  000000                  STACK:  0                       ;STACK LOCATOR
                        000200                  .=200
000200  012706  000600                          MOV     #STACK,SP
000204  004537  007510                          JSR     R5,ADDMO        ;ASK FOR VECTORS AND ADDRESSES
000210  000137  007060                          JMP     HEADER          ;PRINT HEADER AND TAKE COMMANDS
                                                ;
                        000220                  .=220
000220  012706  000600                          MOV     #STACK,SP
000224  000137  006220                          JMP     DELAY           ;DIRECT ENTRY TO DELAY TEST
                                                ;
                        000240                  .=240
000240  012706  000600                          MOV     #STACK,SP
000244  000137  006436                          JMP     DYMAN           ;DIRECT ENTRY TO DYMANIC TEST
                                                ;
                        001000                  .=1000
001000  012706  000600          LOGIC:  MOV     #STACK-SP       ;INITIALIZE STACK
001004  104000                          NULL
001006  000005                          RESET
001010  104000                          NULL
001012  000137  001016                  JMP     TEST            ;
                                                ;
```

I1

```
                                        ;
                                        ;*****************************************************************
                                        ;                LOGIC TEST
                                        ;*****************************************************************(
001016  012737  010617  007334  TEST:   MOV     #LT,MES         ;SET REGISTER 3 FOR OUTCODE
001024  004337  007210                  JSR     R3,PRINT        ;PRINT "LOGIC TEST"
                                        ;
                                        ;
                                        ;TEST THAT ALL STATUS BITS ARE CLEARED IN THE CSR
                                        ;
                                        ;
001030  004137  007402          T1:     JSR     R1,CHECK
001034  012737  000340  177776          MOV     #340,PS
001042  012737  001030  010570          MOV     #T1,LOOP
001050  032777  177777  177422          BIT     #177777,@XCSR           ;TEST ALL BITS OF STATUS REG
001056  001414                          BEQ     T2
001060  004537  010520                  JSR     R5,ERROR
001064  012737  010634  007334          MOV     #EE1,MES
001072  004337  007210                  JSR     R3,PRINT
001076  004537  010536                  JSR     R5,SCOPE
001102  000000                          HLT             ;STATUS REG NOT CLEAR
001104  000137  001030                  JMP     T1
                                        ;
                                        ;TEST THAT INTERRUPT ENABLE (BIT 6 OF CSR) CAN
                                        ;BE SET AND CLEARED .
                                        ;
001110  004137  007402          T2:     JSR     R1,CHECK
001114  012737  001110  010570          MOV     #T2,LOOP
001122  012777  000100  177350          MOV     #100,@XCSR
001130  032777  000100  177342          BIT     #100,@XCSR              ;TEST THAT INT,EN, IS SET IN THE CSR
001136  001014                          BNE     T3
001140  004537  010520                  JSR     R5,ERROR
001144  012737  010640  007334          MOV     #EE2,MES
001152  004337  007210                  JSR     R3,PRINT
001156  004537  010536                  JSR     R5,SCOPE
001162  000000                          HLT             ;INT, EN, BIT FAILED TO SET
001164  000137  001110                  JMP     T2
                                        ;
                                        ;
                                        ;
001170  004137  007402          T3:     JSR     R1,CHECK
001174  012737  001170  010570          MOV     #T3,LOOP
001202  005077  177272                  CLR     @XCSR
001206  032777  000100  177264          BIT     #100,@XCSR              ;CHECK THAT INT ENABLE CLEARED
001214  001414                          BEQ     T4
001216  004537  010520                  JSR     R5,ERROR
001222  012737  010644  007334          MOV     #EE3,MES
001230  004337  007210                  JSR     R3,PRINT
001234  004537  010536                  JSR     R5,SCOPE
001240  000000                          HLT                     ;INT.ENABLE FAILED TO CLEAR
001242  000137  001170                  JMP     T3
                                        ;
                                        ;EX
                                        ;ENABLE PROCESSOR INTERRUPT AND CHECK FOR ILLEGAL
```

J1

```
                                                ;INTERRUPTS OF WATCH DOG TIMER
                                                ;
001246  004137  007402          T4:   JSR     R1,CHECK
001252  012737  001246  013570        MOV     #T4,LOOP
001260  012704  001322              MOV     #AA1,R4         ;SET UP INT RETURN
001264  012705  001322              MOV     #AA1,R5
001270  052777  000100  177202      BIS     #100,@XCSR              ;ENABLE INT
001276  013737  000510  177776      MOV     PRIV,PS         ;SET PROCESSOR STATUS TO PRIV
001304  000240                      NOP
001306  000240                      NOP                     ;WAIT FOR INTERRUPT
001310  012737  000340  177776      MOV     #340,PS         ;NO INTERRUPT SO GO
001316  000137  001352              JMP     T5
001322  004537  010520          AA1:  JSR     R5,ERROR        ;CHECK FOR ERROR PRINTOUT
001326  012737  010650  007304      MOV     #EE4,MES        ;PRINT ERROR MESSAGE
```

K1

```
                                ;PRINT ERROR 1
                                ;CHECK FOR SCOPE LOOP
                                ;STAY HERE
                                ;RUN TEST OVER ON KEY "COUNT"
                                ;
                                ;
                                ;WAIT FOR POSSIBLE TIME OUT OF DELAYS AND CHECK AGAIN
                                ;FOR ILLEGAL WATCHDOG INTERRUPTS
                                ;
001352  004137  007402      T5: JSR     R1,CHECK
001356  012737  000340  177776  MOV     #340,PS         ;SET PROCESSOR STATUS TO 7
001364  004237  010350          JSR     R2,TOUT         ;WAIT . FOR TIME OUTS
001370  012704  001432          MOV     #AA2,R4         ;SET INT RETURN
001374  012705  001432          MOV     #AA2,R5
001400  013737  000510  177776  MOV     PRIV,PS         ;P.S. TO PRIV
001406  000240                  NOP                     ;WAIT FOR INT
001410  000240                  NOP
001412  012737  000340  177776  MOV     #340,PS         ;SET STATUS TO 7
001420  042777  000100  177052  BIC     #100,@XCSR
001426  000137  001462          JMP     T6              ;GO ON
001432  004537  010520      AA2: JSR     R5,ERROR        ;CHECK FOR ERROR PRINT
001436  012737  010654  007324  MOV     #EE5,MES        ;PRINT ERROR MESSAGE
001444  004337  007210          JSR     R3,PRINT        ;PRINT ERROR 1A
001450  004537  010536          JSR     R5,SCOPE
001454  000000                  HLT                     ;ILLEGAL INT AFTER TIME OUT
001456  000137  001352          JMP     T5
                                ;
                                ;
                                ;READ THE STATUS WORD TO CHECK THAT ALL BITS ARE
                                ;CLEAR AT THIS TIME.
                                ;
001462  004137  007402      T6: JSR     R1,CHECK
001466  012737  001462  010570  MOV     #T6,LOOP        ;SET FOR SCOPE LOOP RUN
001474  032777  177777  176776  BIT     #177777,@XCSR   ;CHECK STATUS REGISTER
001502  001414                  BEQ     T7              ;IF 0 GO TO TEST 7
001504  004537  010520          JSR     R5,ERROR
001510  012737  010668  007324  MOV     #EE6,MES
001516  004337  007210          JSR     R3,PRINT        ;PRINT ERROR2
001522  004537  010536          JSR     R5,SCOPE        ;CHECK FOR SCOPE LOOP
001526  000000                  HLT                     ;STAY HERE
001530  000137  001462          JMP     T6              ;RECYCLE
                                ;
                                ;
                                ;GENERATE A CLEAR COMMAND AND CHECK
                                ;THAT STATUS WAS UNAFFECTED
                                ;
001534  004137  007402      T7: JSR     R1,CHECK
001540  012737  001534  010570  MOV     #T7,LOOP        ;SET UP FOR SCOPE LOOP RUN
001546  005777  176730          TST     @XCINT          ;CLR TO FLAGS SHORT LOOP,SECOND CHANCE
001552  004237  010350          JSR     R2,TOUT
001556  032777  177777  176714  BIT     #177777,@XCSR
001564  001414                  BEQ     T8              ;ALL CLEAR GO TO TEST 8
001566  004537  010520          JSR     R5,ERROR
```

```
                                        MOV     #EE7,MES        ;PRINT ERROR 3
                                        JSR     R3,PRINT
                                        JSR     R5,SCOPE        ;CHECK FOR SCOPE LOOP
                                        HLT
                                        JMP     T7              ;RECYCLE TEST
                                        ;
                                        ;
                                        ;
                                        ;PULSE TIMER AND CHECK FOR SECOND CHANCE (T2) TO TIME
                                        ;OUT
                                        ;
001616  004137  007402          T8:     JSR     R1,CHECK
001622  012737  001616  013570          MOV     #T8,LOOP
001630  012737  000340  177776          MOV     #340,PS
001636  012777  000001  176634          MOV     #1,@XCSR        ;PULSE TIMER
001644  004237  010350                  JSR     R2,TOUT
001650  105777  176624                  TSTB    @XCSR           ;TEST THAT T2 TIMED OUT
001654  100414                          BMI     T9
001656  004537  010520                  JSR     R5,ERROR
001662  012737  010670  007304          MOV     #EE8,MES
001670  004337  007210                  JSR     R3,PRINT
001674  004537  010536                  JSR     R5,SCOPE
001700  000000                          HLT
001702  000137  001616                  JMP     T8              ;T2 FAILED TO TIME OUT
                                        ;
                                        ;CHECK THAT ALARM RECEIVE (BIT 14) IS NOT SET
                                        ;ENABLE FLOP=0
                                        ;
001706  004137  007402          T9:     JSR     R1,CHECK
001712  032777  040000  176568          BIT     #040000,@XCSR
001720  001414                          BEQ     T10
001722  004537  010520                  JSR     R5,ERROR
001726  012737  010674  007304          MOV     #EE9,MES
001734  004337  007210                  JSR     R3,PRINT
001740  004537  010536                  JSR     R5,SCOPE
001744  000000                          HLT                     ;REC.SET WITHOUT ENABLE
001746  000137  001706                  JMP     T9
                                        ;
                                        ;
                                        ;
                                        ;ENABLE ALARM OUT AND CHECK THAT ALARM RECEIVE
                                        ;WILL SET
                                        ;
001752  004137  007402          T10:    JSR     R1,CHECK
001756  012737  001616  013570          MOV     #T8,LOOP
001764  012777  000002  176536          MOV     #2,@XCSR
001772  004237  007342                  JSR     R2,WAITX
001776  032777  040000  176474          BIT     #040000,@XCSR           ;TEST BIT 14
002004  001014                          BNE     T11
002006  004537  010520                  JSR     R5,ERROR
002012  012737  010700  007304          MOV     #EE10,MES
002020  004337  007210                  JSR     R3,PRINT
002024  004537  010536                  JSR     R5,SCOPE
```

M1

```
 297  002030  000000                          HLT                             ;RECEIVE FLAG FAILED TO
 298  002032  000137  001616                  JMP     T8                      ;SET,CHECK THAT T3 TIMED OUT
 299                                          ;
 300                                          ;
 301                                          ;TEST THAT T2 FLAG IS CLEARED BY (164882)CINT
 302                                          ;
 303  002036  004137  007402          T11:    JSR     R1,CHECK
 304  002042  012737  002036  013578          MOV     #T11,LOOP
 305  002050  005777  176426                  TST     @XCINT
 306  002054  105777  176420                  TSTB    @XCSR
 307  002060  100014                          BPL     T12
 308  002062  004537  010520                  JSR     R5,ERROR
 309  002066  012737  010705  007304          MOV     #EE11,MES
 310  002074  004337  007210                  JSR     R3,PRINT
 311  002100  004537  010536                  JSR     R5,SCOPE
 312  002104  000000                          HLT                     ;T2 NOT CLEARED BY CINT(164882)
 313  002106  000137  002036                  JMP     T11
 314                                          ;
 315                                          ;CHECK THAT RECIEVE FLAG WAS CLEARED BY CLEAR REC FLAG (BIT 8 OF CSR)
 316                                          ;
 317  002112  004137  007402          T12:    JSR     R1,CHECK
 318  002116  012737  002036  013578          MOV     #T11,LOOP
 319  002124  012777  000400  176346          MOV     #000400,@XCSR           ;CLEAR RECIEVE FLAG
 320  002132  032777  040000  176340          BIT     #040000,@XCSR           ;TEST RECIEVE FLAG
 321  002140  001414                          BEQ     T13
 322  002142  004537  010520                  JSR     R5,ERROR
 323  002146  012737  010712  007304          MOV     #EE12,MES
 324  002154  004337  007210                  JSR     R3,PRINT
 325  002160  004537  010536                  JSR     R5,SCOPE
 326  002164  000000                          HLT                             ;RECEIVE FLG FAILED TO CLR
 327  002166  000137  002112                  JMP     T12
 328                                          ;
 329                                          ;
 330                                          ;ISSUE TWO SUCCESSIVE PULSES TO THE TIMER AND MONITOR BIT 15
 331                                          ;OF THE CSR FOR A SHORT LOOP FLAG
 332  002172  004137  007402          T13:    JSR     R1,CHECK
 333  002176  012737  000340  177776          MOV     #340,PS         ;SET STATUS TO SEVEN
 334  002204  012737  002474  013578          MOV     #THW,LOOP       ;SET FOR SCOPE LOOP
 335  002212  005277  176262                  INC     @XCSR           ;HIT TIMER TWICE
 336  002216  005277  176256                  INC     @XCSR
 337  002222  005777  176252                  TST     @XCSR           ;BIT 15 SHOULD BE SET
```

```
 339
 340  002226  100004                        BPL     .+12
 341  002230  004237  010350                JSR     R2,TOUT         ;GO WAIT FOR TIMEOUT BEFORE PROCEEDING
 342  002234  000137  002270                JMP     T14
 343  002240  004537  010520                JSR     R5,ERROR        ;CHECK FOR ERROR PRINT
 344  002244  012737  010717  007304        MOV     #EE13,MES       ;PRINT ERROR 13
 345  002252  004337  007210                JSR     R3,PRINT
 346  002256  004537  010536                JSR     R5,SCOPE
 347  002262  000000                        HLT             ;SHORT LOOP FLAG FAILED TO SET
 348  002264  000137  002474                JMP     THW
 349                                        ;
 350                                        ;
 351                                        ;TEST BIT 7 (2ND CHANCE) .  BIT 7 SHOULD NOT BE SE
 352                                        ;TERMINATED BY LOCK
 353                                        ;
 354  002270  004137  007402        T14:    JSR     R1,CHECK
 355  002274  105777  176200                TSTB    @XCSR           ;TEST BIT 7
 356  002300  100014                        BPL     T15             ;CONTINUE TO TEST
 357  002302  004537  010520                JSR     R5,ERROR
 358  002306  012737  010724  007304        MOV     #EE14,MES
 359  002314  004337  007210                JSR     R3,PRINT
 360  002320  004537  010536                JSR     R5,SCOPE
 361  002324  000000                        HLT             ;T2 (2ND CHANCE) FLAG SET,CHECK LOCK FLOP
 362  002326  000137  002474                JMP     THW             ;LOOP TO TEST 13 ON KEY "CONT"
 363                                        ;
 364                                        ;WAIT 5 M,SEC AND TEST THAT THE ENABLE FLOP PREVRENTED
 365                                        ;THE WATCH DOG OUT SIGNAL FROM SETTING THE RECEIVE FLAG
 366                                        ;
 367                                        ;
 368  002332  004137  007402        T15:    JSR     R1,CHECK
 369  002336  012737  000340  177776        MOV     #340,PS
 370  002344  004237  007342                JSR     R2,WAITX        ;WAIT FOR POSSIBLE TIME OUT OFT4
 371  002350  032777  040000  176122        BIT     #BM7800,@XCSR   ;TEST THAT REC.DIDNT SET
 372  002356  001414                        BEQ     T16
 373  002360  004537  010520                JSR     R5,ERROR
 374  002364  012737  010731  007304        MOV     #EE15,MES
 375  002372  004337  007210                JSR     R3,PRINT
 376  002376  004537  010536                JSR     R5,SCOPE
 377  002402  000000                        HLT             ;REC. FLAG SET WITHOUT AN ENABLE
 378  002404  000137  002474                JMP     THW             ;LOOP ON TEST 13
 379                                        ;
 380                                        ;
 381                                        ;ENABLE THE EXTERNAL WORLD AND WAIT 5 M.SEC
 382                                        ;FOR THE LOCK FLOP TO BE CLEARED BY CLEAR ERROR
 383                                        ;SIGNAL. TEST THAT LOCK FLOP WAS CLEARED BY RESETTING
 384                                        ;THE 2ND, CHANCE FLAG (T2).
 385                                        ;
 386  002410  004137  007402        T16:    JSR     R1,CHECK
 387  002414  012777  000002  176056        MOV     #2,@XCSR        ;ENABLE THE EXTERNAL WORLD
 388  002422  004237  007342                JSR     R2,WAITX        ;WAIT FOR CLEAR ERROR
 389  002426  005277  176046                INC     @XCSR           ;SET T2 FLAG AGAIN
 390  002432  004237  010350                JSR     R2,TOUT         ;TIME OUT DELAYS
 391  002436  105777  176036                TSTB    @XCSR
 392  002442  100431                        BMI     T17             ;RE CLR AND PROCEED
```

```
  393  002444  004537  010520                JSR     R5,ERROR
  394  002450  012737  010736  007324        MOV     #EE16,MES
  395  002456  004337  007210                JSR     R3,PRINT
  396  002462  004537  010536                JSR     R5,SCOPE
  397  002466  000000                        HLT                     ;LOCK FLOP NOT CLEARED BY
  398  002470  000137  002474                JMP     THW             ;CLEAR ERROR
  399  002474  012777  000002  175776  THW:  MOV     #2,@XCSR        ;CLEAR LOCK FOR RECYCLE
  400  002502  004237  007342                JSR     R2,WAITX
  421  002506  005777  175770                TST     @XCINT          ;CLEAR FLAGS SHORT LOOP,SECOND CHANCE
  402  002512  012777  000400  175760        MOV     #000400,@XCSR           ;CLEAR RECIEVE FLAG
  403  002520  000005                        RESET
  404  002522  000137  002172                JMP     T13
  405                                        ;
  406                                        ;
  407                                        ;WITH RECEIVE AND SHORT LOOP FLAG SET PULSE TIMER
  408                                        ;AND WAIT FOR TIME OUT OF T2 THEN ISSUE AN CLEAR INSTRUCTION
  409                                        ;AND CHECK THAT ALL FLAGS ARE CLEARED.
```

C2

```
 411                                                    ;
 412  002526  004137  007402          T19:    JSR     R1,CHECK
 413  002532  012737  000340  177776          MOV     #340,PS
 414  002540  012737  002526  010570          MOV     #T17,LOOP       ;LOOP TEST9
 415  002546  005777  175730                  TST     @XCINT          ;CLEAR INTERRUPT FLAGS, SHORT LOOP,SECOND CHANCE
 416  002552  012777  000400  175720          MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
 417                                          ;TEST SHORT LOOP INTERRUPT FLAG FOR BEING CLEARED
 418                                                    ;
 419  002560  004137  007402          T18:    JSR     R1,CHECK
 420  002564  005777  175710                  TST@    @XCSR           ;TEST BIT 15 OF CSR
 421  002570  100014                          BPL     T19             ;OK GO ON
 422  002572  004537  010520                  JSR     R5,ERROR        ;CHECK FOR REPORT OF ERROR
 423  002576  012737  010750  007304          MOV     #EE18,MES       ;SET ERROR PRINT
 424  002604  004337  007210                  JSR     R3,PRINT
 425  002610  004537  010536                  JSR     R5,SCOPE
 426  002614  000000                          HLT                     ;SHORT LOOP FLAG FAILED TO CLEAR
 427  002616  000137  002526                  JMP     T17             ;LOOP TO TEST 17 ON KEY "CONT"
 428                                                    ;
 429                                          ;TEST WARNING FLAG (BIT 7) FOR BEING CLEAR
 430                                                    ;
 431  002622  004137  007402          T19:    JSR     R1,CHECK
 432  002626  105777  175646                  TSTB    @XCSR           ;TEST BIT 07 OF CSR
 433  002632  100014                          BPL     T20
 434  002634  004537  010520                  JSR     R5,ERROR        ;CHECK FOR ERROR REPORT
 435  002640  012737  010755  007304          MOV     #EE19,MES       ;SET ERROR PRINT
 436  002646  004337  007210                  JSR     R3,PRINT
 437  002652  004537  010536                  JSR     R5,SCOPE
 438  002656  000000                          HLT
 439  002660  000137  002526                  JMP     T17             ;LOOP TO TEST 17 ON KEY "CONT"
 440                                                    ;
 441                                          ;TEST ALARM RECEIVE (BIT 14) FOR BEING CLEAR
 442                                                    ;
 443  002664  004137  007402          T20:    JSR     R1,CHECK
 444  002670  032777  040000  175632          BIT     #040000,@XCSR           ;TEST BIT 14 OF CSR
 445  002676  001414                          BEQ     T21
 446  002700  004537  010520                  JSR     R5,ERROR        ;CHECK FOR ERROR REPORT
 447  002704  012737  010762  007304          MOV     #EE20,MES       ;SET PRINT ERROR T20
 448  002712  004337  007210                  JSR     R3,PRINT
 449  002716  004537  010536                  JSR     R5,SCOPE
 450  002722  000000                          HLT                     ;BIT 14 OF CSR FAILED TO A CLR
 451  002724  000137  000017                  JMP     17              ;LOOP TO TEST 17 ON CONT
 452                                                    ;
 453                                          ;ENABLE ALARM OUT SIGNAL (PROGRAM CONTROL) AND TEST
 454                                          ;THAT TIME OUT OF T3 WILL SET ALARM RECEIVE FLOP (BIT 14)
 455                                          ;THE ALARM RECEIVE SIGNAL MUST BE CONNECTED TO THE ALARM OUT
 456                                          ;AND THE PROGRAM CONTROLLED "RESET" STRAP MUST BE CONNECTED
 457                                                    ;
 458  002730  004137  007402          T21:    JSR     R1,CHECK
 459  002734  012737  002730  010570          MOV     #T21,LOOP
 460  002742  012737  000340  177776          MOV     #340,PS
 461  002750  012777  000003  175522          MOV     #3,@XCSR                ;START TIMER AND ENABLE "ALARM OUT"
 462  002756  004237  010350                  JSR     R2,TOUT                 ;TIME OUT DELAYS
 463  002762  032777  040000  175510          BIT     #040000,@XCSR           ;CHECK BIT 14 FOR BEING SET
 464  002770  001402                          BEQ     .+6
```

```
  465  002772  000137  003026                    JMP     T22
  466  002776  004537  010520                    JSR     R5,ERROR
  467  003002  012737  010767  007304            MOV     #EE21,MES       ;SET ERROR PRINTOUT
  468  003010  004337  007210                    JSR     R3,PRINT
  469  003014  004537  010536                    JSR     R5,SCOPE
  470  003020  000000                            HLT                     ;RECEIVE ALARM FLOP FAILED TO SET
  471  003022  000137  002730                    JMP     T21             ;LOOP ON TEST 21
  472                                             ;
  473                                             ;
  474                                             ;CLEAR INTERRUPT FLAGS AND CHECK THAT "ALARM RECEIVE"
  475                                             ;FLAG WAS CLEARED
  476                                             ;
  477  003026  004137  007402          T221:      JSR     R1,CHECK
  478  003032  012777  000340  175440            MOV     #340,@XCSR
  479  003040  012737  003026  010570            MOV     #T22,LOOP       ;SET SCOPE RETURN
  480  003046  012777  000400  175424            MOV     #000400,@XCSR   ;CLEAR ALARM RECEIVE FLAG
  481  003054  032777  040000  175416            BIT     #040000,@XCSR           ;TEST BIT 14 FOR BEING CLEAR
  482  003062  001414                            BEQ     T23             ;FLAG CLEAR GO ON
```

```
                                                ;
003064  004537  010520                          JSR     R5,ERROR
003070  012737  010774  007304                  MOV     #EE22,MES
003076  004337  007210                          JSR     R3,PRINT
003102  004537  010536                          JSR     R5,SCOPE
003106  000000                                  HLT                     ;BIT 14 OF CSR FAILED TO CLEAR
003110  000137  003026                          JMP     T22
                                                ;
                                                ;CHECK "LOCKOUT" FEATURE OF "ALARM OUT" AFTER AN ALARM
                                                ;OUT SIGNAL HAS BEEN GENERATED.
                                                ;
003114  004137  007402            T23:          JSR     R1,CHECK
003120  012737  000340  177776                  MOV     #340,PS
003126  012737  003114  010570                  MOV     #T23,LOOP
003134  012777  000001  175336                  MOV     #1,@XCSR                ;START TIMING
003142  004237  010350                          JSR     R2,TOUT         ;TIME OUT DELAYS
003146  004237  007342                          JSR     R2,WAITX        ;WAIT FOR REC TO @SET
003152  032777  040000  175320                  BIT     #040000,@XCSR           ;TEST THAT LOCK OUT PREVENTED
003160  001414                                  BEQ     T24             ;BIT 14 FROM BEING SET
003162  004537  010520                          JSR     R5,ERROR
003166  012737  011001  007304                  MOV     #EE23,MES
003174  004337  007210                          JSR     R3,PRINT
003200  004537  010536                          JSR     R5,SCOPE
003204  000000                                  HLT                     ;CLEAR ERROR FAILED TO ENABLE FLOP
003206  000137  003114                          JMP     T23             ;ALARM OUT SIGNAL
                                                ;
                                                ;DROP PROCESSOR STATUS TO 6 AND CHECK THAT WARNING FLAG WILL GIVE AN
                                                ;INTERRUPT AT VECTOR 170
                                                ;
003212  005777  175264            T24:          TST     @XCINT          ;CLEAR SHORT LOOP, SECOND CHANCE
003216  012777  000400  175254                  MOV     #000400,@XCSR           ;CLEAR RECEIVE FLAG
003224  004137  007402                          JSR     R1,CHECK
003230  012704  003330                          MOV     #T25,R4         ;SET INTERRUPT RETURN
003234  012705  007440                          MOV     #WRNG,R5        ;SET FOR INTERRUPT AT WRONG VECTOR
003240  012737  003212  010570                  MOV     #T24,LOOP
003246  012777  000101  175224                  MOV     #101,@XCSR
003254  004237  010350                          JSR     R2,TOUT
003260  013737  000510  177776                  MOV     @PRIV,PS        ;SET STATUS TO PRIV
003266  000240                                  NOP                     ;WAIT FOR INTERRUPT
003270  000240                                  NOP                     ;
003272  012737  000340  177776                  MOV     #340,PS         ;SHOULD HAVE INTERRUPTED
003300  004537  010520                          JSR     R5,ERROR        ;SET STATUS BACK TO SEVEN
003304  012737  011006  007304                  MOV     #EE24,MES
003312  004337  007210                          JSR     R3,PRINT
003316  004537  010536                          JSR     R5,SCOPE
003322  000000                                  HLT                     ;WARNING FLAG (BIT 07) FAILED
003324  000137  003212                          JMP     T24             ;TO PRODUCE AN INTERRUPT
                                                ;
                                                ;CLEAR FLAGS AND SET THE SHORT LOOP
                                                ;FLAG TO CHECK FOR AN INTERRUPT
                                                ;
                                                ;
```

F2

```
537
538  003330  004137  007402          T25:    ;
539  003334  000005                  JSR     R1,CHECK
540  003336  005777  175140          RESET
541  003342  012704  003446          TST     @XCINT          ;CLEAR INTERRUPTS
542  003346  012705  007440          MOV     #AA4,R4         ;SET INTERRUPT RETURN
543  003352  012737  003330  013570  MOV     #WRNG,R5        ;SETFOR WRONG VECTOR
544  003360  013737  000516  177776  MOV     #T25,LOOP       ;SET SCOPE MODE
545  003366  052777  000102  175104  MOV     PRIV,PS         ;GET STATUS DOWN TO PRIV
546  003374  005277  175100          BIS     #102,@XCSR      ;INT.EN +EXT.EN
547  003400  005277  175074          INC     @XCSR           ;SET SHORT LOOP
548  003404  000240                  INC     @XCSR
549  003406  000240                  NOP                     ;SHOULD INT HERE
550  003410  012737  000340  177776  NOP
551  003416  004537  010520          MOV     #340,PS         ;NO INT.GET STATUS BACK UP
552  003422  012737  011013  007304  JSR     R5,ERROR
553  003430  004337  007210          MOV     #EE25,MES       ;SET ERROR PRINT
554  003434  004537  010536          JSR     R3,PRINT
555  003440  000000                  JSR     R5,SCOPE
556  003442  000137  003330          HLT                     ;SHORT LOOP FLAG FAILED TO RAISE A
557  003446  004237  007342  AA4:    JMP     T25             ;INTERRUPT
558  003452  005777  175024          JSR     R2,WAITX                ;WAIT FOR TIME OUT CLR ERROR
559  003456  012777  000400  175014  TST     @XCINT          ;CLEAR FLAGS SHORT LOOP, SECOND CHANCE
560  003464  000137  003470          MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
561                                  JMP     T26
562                                  ;
563                                  ;CHECK FOR ALARM RECEIVE FLAG TO GENERATE AN INTERRUPT
564                                  ;BY CLEARING THE WARNING FLAG BEFORE THE RECEIVE
565                                  ;FLAG IS SET, T3>T2 BY AT LEAST 50 MIRCO. SEC.
566  003470  004137  007402          ;
567  003474  012737  000340  177776  T26:    JSR     R1,CHECK
568  003502  012705  003626          MOV     #340,PS         ;SET PROCESSOR STATUS TO 7
569  003506  012704  007440          MOV     #AA5,R5         ;SET INTERRUPT RETURN
570  003512  012737  003446  013570  MOV     #WRNG,R4        ;SET FOR WRONG VECTOR
571  003520  012777  000003  174752  MOV     #AA4,LOOP       ;SET SCOPE
572  003526  105777  174746          MOV     #3,@XCSR                ;START TIMING, ENABLE ALARM OUT
573  003532  100375                  TSTB    @XCSR                   ;WAIT FOR WARNING
574  003534  005777  174742          BPL     .-4
575  003540  032777  040000  174732  TST     @XCINT                  ;CLEAR BIT 7 OF CSR
576  003546  001774                  BIT     #040000,@XCSR           ;WAIT FOR ALARM RECEIVE FLAG
577  003550  052777  000100  174722  BEQ     .-6
578  003556  013737  000516  177776  BIS     #100,@XCSR              ;ENABLE INT.-2L
579  003564  000240                  MOV     PRIV,PS         ;SET STATUS TO PRIV
580  003566  000240                  NOP                     ;SHOULD INT. HERE
581  003570  012737  000340  177776  NOP
582  003576  004537  010520          MOV     #340,PS         ;FAILED TO INT. SET STATUS TO 7
583  003602  012737  011020  007304  JSR     R5,ERROR        ;CHECK FOR ERROR REPORT
584  003610  004337  007210          MOV     #EE26,MES       ;
585  003614  004537  010536          JSR     R3,PRINT
586  003620  000000                  JSR     R5,SCOPE        ;CHECK FOR SCOPE ROUTINE
587  003622  000137  003446          HLT
588  003626  004237  010350  AA5:    JMP     AA4             ;CLR FLAGSBEFORE LOOP
589  003632  012777  000400  174640  JSR     R2,TOUT         ;CLEAR POSSIBILITY OF SHORT LOOP
590  003640  000137  003644          MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
                                     JMP     T27                     ;T 27
```

(2)

```
                                                        ;
                                                        ;
                                                        ;CHECK LOCK OUT OF SHORT LOOP BY FIRST CAUSING A
                                                        ;SHORT LOOP FLAG THEN READING STATUS OF RECEIVE TO CHECK
                                                        ;THAT T3 HAS BEEN TERMINATED
                                                        ;
003644  004137  007402          T29:    JSR     R1,CHECK
003650  012737  003626  013570          MOV     #AA5,LOOP
003656  012737  000340  177776          MOV     #340,PS
003664  005777  174612                  TST     @XCINT
003670  005077  174604                  CLR     @XCSR
003674  012777  000003  174576          MOV     #3,@XCSR        ;SET SHORT LOOP
003702  005277  174572                  INC     @XCSR
003706  004237  007342                  JSR     R2,WAITX        ;5,MILLI.SEC,CLEAR LOCK  AND ENABLE
003712  032777  040000  174560          BIT     #040000,@XCSR
003720  001014                          BNE     T28
003722  004537  010520                  JSR     R5,ERROR
003726  012737  011025  007334          MOV     #EE27,MES
003734  004337  007210                  JSR     R3,PRINT
003740  004537  010536                  JSR     R5,SCOPE
003744  000000                          HLT                     ;SHORT LOOP LOCK FAILED TO TERMINATE T3
003746  000137  003626                  JMP     AA5
                                                        ;
                                                        ;TEST THAT T2 WAS TERMINATED BY A SHORT LOOP LOCK BY
                                                        ;TESTING STATUS OF T2
                                                        ;
003752  004137  007402          T28:    JSR     R1,CHECK
003756  012737  003752  013570          MOV     #T28,LOOP
003764  004237  010350                  JSR     R2,TOUT
003770  012777  000400  174532          MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
003776  005777  174506                  TST     @XCINT          ;CLR FLAGS SHORT LOOP, SECOND CHANCE
004002  012777  000003  174470          MOV     #3,@XCSR        ;EXT EN, SET S.LOOP
004010  005277  174464                  INC     @XCSR
004014  105777  174460                  TSTB    @XCSR           ;TEST BIT 7
004020  100014                          BPL     T29
004022  004537  010520                  JSR     R5,ERROR
004026  012737  011032  007334          MOV     #EE28,MES
004034  004337  007210                  JSR     R3,PRINT
004040  004337  010536                  JSR     R3,SCOPE
004044  000000                          HLT                     ;LOCK FAILED TO TERMINATE T2
004046  000137  003752                  JMP     T28             ;LOOP ONTEST 28
                                                        ;
                                                        ;
                                                        ;WAIT 5 MILLI SEC, FOR CLEAR ERROR TO RELEASE
                                                        ;THE LOCK FLOP AND PASS T2 TO BUS
                                                        ;
                                                        ;
004052  004137  007402          T29:    JSR     R1,CHECK
004056  004237  007342                  JSR     R2,WAITX
004062  105777  174412                  TSTB    @XCSR
004066  100414                          BMI     T30
004070  004537  010520                  JSR     R5,ERROR
004074  012737  011037  007334          MOV     #EE29,MES
004102  004337  007210                  JSR     R3,PRINT
```

```
 645  004106  004537  010536                    JSR     R5,SCOPE
 646  004112  000006                            HLT                     ;LOCK DIDN'T RELEASE T2 TO BUS
 647  004114  000137  003792                    JMP     T28             ;LOOP ON TEST 28
 648                                             ;
 649                                             ;
 650                                             ;
 651                                             ;CHECK THAT LOCK FROM SHORT LOOP FLAG
 652                                             ;LOCKS PULSE ING OF TIMER BY ATTEMPING TO SET SHORT
 653                                             ;LOOP FLAG AFTER A PREVIOUS SHORT LOOP
 654                                             ;
 655  004120  004137  007402          T38:       JSR     R1,CHECK
 656  004124  012737  000340  177776              MOV     @340,PS
 657  004132  012737  004120  013570              MOV     @T38,LOOP
 658  004140  005777  174336                    TST     @XCINT          ;CLEAR FLAGS SHORT LOOP,SECOND CHANCE
 659  004144  005277  174338                    INC     @XCSR
 660  004150  005277  174324                    INC     @XCSR
 661  004154  005777  174322                    TST     @XCINT          ;CLR FLAGS SHORT LOOP,SECOND CHANCE
 662  004160  005277  174314                    INC     @XCSR
 663  004164  005277  174310                    INC     @XCSR
 664  004170  005777  174304                    TST     @XCSR
 665  004174  100014                            BPL     PTR
 666  004176  004537  010520                    JSR     R5,ERROR
 667  004202  012737  011044  007304            MOV     @EE38,MES
 668  004210  004337  007210                    JSR     R3,PRINT
 669  004214  004537  010536                    JSR     R5,SCOPE
 670  004220  000000                            HLT                     ;SHORT LOOP LOCK FAILED TO LOCK TIMER
 671  004222  000137  004120                    JMP     T38             ;LOOP ON TEST 38
 672                                             ;
 673  004226  012777  000002  174244  PTR:      MOV     @2,@XCSR
 674  004234  004237  007342                    JSR     R2,WAITX        ;CLR ERROR
 675  004240  005777  174236                    TST     @XCINT          ;CLEAR FLAGS SHORT LOOP,SECOND CHANCE
 676                                             ;
 677                                             ;
 678                                             ;GENERATE A SHORT LOOP COMMAND AND CHECK THAT INITIALIZE
 679                                             ;WILL CLEAR THE SHORT LOOP FLAG.
 680                                             ;
 681                                             ;
 682  004244  004137  007402          T31:       JSR     R1,CHECK
 683  004250  012737  004244  013570              MOV     @T31,LOOP
 684  004256  005277  174216                    INC     @XCSR           ;SET A SHORT LOOP
 685  004262  005277  174212                    INC     @XCSR
 686  004266  000005                            RESET
 687  004270  005777  174204                    TST     @XCSR           ;TEST SHORT LOOP FLAG FOR CLEAR
 688  004274  100014                            BPL     T32
 689  004276  004537  010520                    JSR     R5,ERROR
 690  004302  012737  011051  007304            MOV     @EE31,MES
 691  004310  004337  007210                    JSR     R3,PRINT
 692  004314  004537  010536                    JSR     R5,SCOPE
 693  004320  000000                            HLT                     ;INITIALIZE FAILED TO CLEAR SHORT
 694  004322  000137  004244                    JMP     T31             ;LOOP FLAG
 695                                             ;
 696                                             ;ENABLE THE EXTERNAL WORLD AND ALLOW THE RECIEVE
 697                                             ;FLAG TO SET THEN CHECK THAT THE INITIALIZE
 698                                             ;CLEARED RECEIVE FLAG.
```

I2

```
                                                ;
000326  004137  007462          T32:  JSR     R1,CHECK
000332  012737  004326  013570        MOV     #T32,LOOP
000340  012777  000002  174132        MOV     #2,@XCSR
000346  004237  007342                JSR     R2,WAITX        ;5,MILLI SEC SET REC
000352  000005                        RESET
000354  032777  040000  174116        BIT     #040000,@XCSR           ;TEST RECIEVE FLAG
000362  001414                        BEQ     T33
000364  004537  010520                JSR     R5,ERROR
000370  012737  011056  007304        MOV     #EE32,MES
000376  004337  007210                JSR     R3,PRINT
000402  004537  010536                JSR     R5,SCOPE
000406  000000                        HLT                     ;INITIALIZE FAILED TO CLEAR REC
000410  000137  004326                JMP     T32             ;FLAG
                                                ;
                                                ;
                                                ;TEST THAT INITIALIZE WILL CLEAR THE LOCK FLOP
                                                ;BY SETTING A SHORT LOOP FLAG AND ISSUEING A RESET INSTR
                                                ;UCTION, TEST THAT THE LOCK FLOP IS CLEARED BY SETTING
                                                ;A 2ND SHORT LOOP FLAG.
                                                ;
                                                ;
                                                ;
000414  004137  007462          T33:  JSR     R1,CHECK
000420  012737  004414  013570        MOV     #T33,LOOP
000426  005277  174046                INC     @XCSR
000432  005277  174042                INC     @XCSR
000436  000005                        RESET                   ;ATTEMPT TO CLEAR SHORT LOOP
000440  005277  174034                INC     @XCSR
000444  005277  174030                INC     @XCSR
000450  005777  174024                TST     @XCSR           ;TEST SHOT LOOP
000454  100414                        BMI     PTX1
000456  004537  010520                JSR     R5,ERROR
000462  012737  011063  007304        MOV     #EE33,MES
000470  004337  007210                JSR     R3,PRINT
000474  004537  010536                JSR     R5,SCOPE
000500  000000                        HLT                     ;INITIALIZE FAILED TO CLEAR LOCK
000502  000137  004414                JMP     T33
000506  012777  000002  173764  PTX1: MOV     #2,@XCSR
000514  004237  007342                JSR     R2,WAITX                ;WAIT 5,M.S. FOR ERROR TO CLR
                                                ;
                                                ;PULSE TIMER AND ISSUE A RESET INSTRUCTION, WAIT 5,MILLI
                                                ;WITH EXTERNAL ENABLE SETAND TEST RECEIVE FLAG TO
                                                ;CHECK THAT INITIALIZE TERMINATED T3.
                                                ;
000520  004137  007462          T34:  JSR     R1,CHECK
000524  012737  004520  013570        MOV     #T34,LOOP
000532  012777  000001  173748        MOV     #1,@XCSR        ;PULSE TIMER & EX. EN SET
000540  000005                        RESET
000542  012777  000002  173738        MOV     #2,@XCSR
000550  004237  007342                JSR     R2,WAITX        ;WAIT 5, MILLI SEC FOR T4
000554  032777  040000  173716        BIT     #040000,@XCSR   ;TEST RECEIVE FLAG
000562  001020                        BNE     PTX2
000564  004237  010350                JSR     R2,TOUT
```

```
                                        TST     @XCINT
                                        JSR     R5,ERROR
                                        MOV     #EE34,MES
                                        JSR     R3,PRINT
                                        JSR     R5,SCOPE
                                        HLT                     ;INITIALIZE FAILED TO TERMINATE
                                        JMP     T34             ;T3
                        PTX21:          JSR     R2,TOUT
                                        TST     @XCINT          ;CLEAR SHORT LOOP,SECOND CHANCE
                                        MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
                                        ;
                                        ;PULSE TIMER AND ISSUE A RESET  INSTRUCTION
                                        ;WAIT FOR POSSIBLE TIME-OUT OF T2 THEN READ
                                        ;STATUS OF T2 TO TEST THAT INITIALIZE
                                        ;TERMINATED T2.
                                        ;
                        T35:            JSR     R1,CHECK
                                        MOV     #T35,LOOP
                                        MOV     #3,@XCSR
                                        RESET
                                        JSR     R2,TOUT         ;WAIT FOR DELAYS TO TIME OUT
                                        TSTB    @XCSR           ;TEST BIT 7
                                        BPL     PTX3
                                        TST     @XCINT          ;CLEAR FLAGS
                                        JSR     R5,ERROR
                                        MOV     #EE35,MES
                                        JSR     R3,PRINT
                                        JSR     R5,SCOPE
                                        HLT                     ;INITIALIZE FAILED TO TERMINATE T2
                                        JMP     T35
                        PTX3:           TST     @XCINT          ;CLEAR FLAGS SHORT LOOP, SECOND CHANCE
                                        MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
                                        ;
                                        ;TEST STATUS A&B AND TEST THAT BITS 7 & 15 ARE COMPLEMENTS
                                        ;15=1 AND 7=0 FROM A RESET CONDITION
                                        ;
                        T36:            JSR     R1,CHECK
                                        RESET
                                        MOV     #340,PS
                                        MOV     #T36,LOOP
                                        TST     @XECSR          ;CHECK BIT 15 OFECSR
                                        BPL     TILT
                                        TSTB    @XECSR          ;CHECK BIT 7 OF EXT CSR 15=1
                                        BMI     TILT            ;REPORT ERROR BOTH SAME
                                        JMP     T37             ;OK 15=1  7=0
                        TILT:           NOP
                                        JSR     R5,ERROR
                                        MOV     #EE36,MES
                                        JSR     R3,PRINT
                                        JSR     R5,SCOPE
                                        HLT             ;INCORECT STATUS IN EXT. CSR
                                        JMP     T36
                                        ;
                                        ;ISSUE A RESET INSTRUCTION AND TEST THAT STATUS
```

K2

```
                                                ;OF THE EXT. CSR DOESNT CHANGE (NEUTRAL-POSITION)!
                                                ;
005040  004167  007402          T39:  JSR     R1,CHECK
005044  017737  173434  005724        MOV     @XECSR,PPL              ;SAVE EXT STATUS
005052  012737  005040  010570        MOV     #T37,LOOP
                                      RESET
005060  000005                        JSR     R2,WAITX                ;WAIT FO RELAY
005062  004237  007342                ADD     @XECSR,PPL      ;TEST FOR STATUS CHANGE
005066  067737  173412  005724        BPL     T38
005074  100014                        JSR     R5,ERROR
005076  004537  010520                MOV     #EE37,MES
005102  012737  011107  007304        JSR     R3,PRINT
005110  004337  007210                JSR     R5,SCOPE
005114  004537  010536                HLT                     ;RESET INSTRUCTION CHANGED STATUS
005120  000000                        JMP     T39             ;OF EXT CSR
005122  000137  005040                ;
                                      ;
                                      ;WITH LATCH IN NEUTRAL POSITION SWITCH BUSS AND
                                      ;CHECK FOR CHANGE OF STATUS IN EXT. CSR
                                      ;
005126  004167  007402          T38:  JSR     R1,CHECK
                                      RESET
005132  000005                        MOV     #T38,LOOP
005134  012737  005126  010570        MOV     #EE385,MES
005142  012737  011157  007304        MOV     @XECSR,PPL      ;SAVE EXT. STATUS
005150  017737  173330  005724        INC     @XSW3U          ;SWITCH BUSS
005156  005277  173324                JSR     R2,WAITX
005162  004237  007342                JSR     R3,OPP          ;CHECK THAT BITS ARE OF OPPOSITE
005166  004337  006100                ADD     @XECSR,PPL      ;POLARITY
005172  067737  173306  005724        BMI     T39
005200  100414                        JSR     R5,ERROR
005202  004537  010520                MOV     #EE38,MES
005206  012737  011114  007304        JSR     R3,PRINT
005214  004337  007210                JSR     R5,SCOPE
005220  004537  010536                HLT                     ;SWITCHING BUSS FAILED
005224  000000                        JMP     T38
005226  000137  005126                ;
                                      ;
                                      ;WITH BUS SWITCH'D CHECK THAT LATCH WILL DE-ENERGIZE RELAY ON
                                      ;A SECOND SWITCHING OF THE BUS
                                      ;TEST THAT STATUS CHANGED (NEUTRAL POSITION)
                                      ;
                                      ;
005232  004167  007402          T39:  JSR     R1,CHECK
005236  012737  005232  010570        MOV     #T39,LOOP
005244  017737  173234  005724        MOV     @XECSR,PPL      ;SAVE EXT STATUS
005252  005277  173230                INC     @XSW3U          ;ATTEMPT TO SWITCH BUSS
005256  004237  007342                JSR     R2,WAITX        ;WAIT FOR RELAY
005262  067737  173216  005724        ADD     @XECSR,PPL      ;WAS BUSS STATUS CHANGED
005270  100414                        BMI     T40
005272  004537  010520                JSR     R5,ERROR
005276  012737  011121  007304        MOV     #EE39,MES
005304  004337  007210                JSR     R3,PRINT
005310  004537  010536                JSR     R5,SCOPE
```

```
000314  000000                          HLT                     ;LATCH FAILED TO PREVENT BUSS CHANGE
000316  240137  000232                  JMP     T39
                                        ;
                                        ;ISSUE A SWITCH BUS COMMAND AND CHECK THAT STATUS
                                        ;A & B CHANGED TO NEXT LATCH
                                        ;
                                        ;
000322  004137  007402          T40:    JSR     R1,CHECK
000326  012737  000322  013570          MOV     #T40,LOOP
000334  017737  173144  000724          MOV     @XECSR,PPL
000342  005277  173140                  INC     @XSWBU          ;SWITCH BUS
000346  004237  007342                  JSR     R2,WAITX                ;5 MILLI SEC FOR RELAY
000352  012737  011165  007304          MOV     #EE40S,MES
000360  004337  006100                  JSR     R3,OPP                  ;TEST FOR POL.CHANGE
000364  067737  173114  000724          ADD     @XECSR,PPL              ;TEST THAT STATUS CHANGED
000372  100414                          BMI     T41
000374  004537  010520                  JSR     R5,ERROR
000400  012737  011126  007304          MOV     #EE40,MES
000406  004337  007210                  JSR     R3,PRINT
000412  004537  010536                  JSR     R5,SCOPE
000416  000000                          HLT                     ;BUS FAILED TO SWITCH TO 2ND LATCH
000420  000137  000322                  JMP     T40
                                        ;
                                        ;
                                        ;
                                        ;ENABLE EXTERNALWORLD AND ALLOW DELAYS TO TIME
                                        ;OUT TO CHECK THAT TERMINATION OF T3 WILL RELEASE THE LATCH
                                        ;
                                        ;
000424  004137  007402          T41:    JSR     R1,CHECK
000430  012737  000322  013570          MOV     #T40,LOOP
000436  017737  173042  000724          MOV     @XECSR,PPL      ;SAVE STATUS A&B
000444  012777  000003  173026          MOV     #3,@XCSR                ;ALLOW FOR CLEAR ERROR
000452  004237  010350                  JSR     R2,TOUT         ;TIME OUT ALLDELAYS
000456  004237  007342                  JSR     R2,WAITX        ;5 MILLI.SEC FOR RELAYS
000462  012737  011173  007304          MOV     #EE41S,MES      ;SET SUBTEST PRINT
000470  004337  006100                  JSR     R3,OPP          ;SUBTEST
000474  067737  173004  000724          ADD     @XECSR,PPL
000502  100414                          BMI     T42             ;IF STATUS CHANGED GO ON
000504  004537  010520                  JSR     R5,ERROR        ;
000510  012737  011133  007304          MOV     #EE41,MES
000516  004337  007210                  JSR     R3,PRINT
000522  004537  010536                  JSR     R5,SCOPE
000526  000000                          HLT                     ;BUSS FAILED TO SWITCH TO SECOND LATCH
000530  000137  000424                  JMP     T41
                                        ;
                                        ;
                                        ;
                                        ;ISSUE A SECOND SWITCH BUSS COMAND AND CHECK THAT SWBU (164056)
                                        ;WILL SWITCH BUS
                                        ;
000534  004137  007402          T42:    JSR     R1,CHECK
000540  012737  000534  013570          MOV     #T42,LOOP
000546  017737  172732  000724          MOV     @XECSR,PPL
```

M2

```
 915  005554  005277  172726                 INC     @XSWBU          ;ATTEMPT TO SWITCH BUSS
 916  005560  004237  007342                 JSR     R2,WAITX        ;5 MILLI SEC FOR RELAY
 917  005564  067737  172714  005724         ADD     @XECSR,PPL      ;DID STATUS CHANGE
 918  005572  100414                         BMI     T43             ;IF MINUS STATUS CHANGED
 919  005574  004537  010520                 JSR     R5,ERROR
 920  005600  012737  011140  007304         MOV     #EE42,MES
 921  005606  004337  007210                 JSR     R3,PRINT
 922  005612  004537  010536                 JSR     R5,SCOPE
 923  005616  000000                         HLT                     ;LATCH FAILED TO PREVENT BUSS FROM
 924  005620  000137  005534                 JMP     T42             ;SWITCHING
 925                                         ;
 926                                         ;
 927                                         ;ISSUE A "RESET" INSTRUCTION AND TEST THAT
 928                                         ;LATCH  GETS CLEARED
 929                                         ;
 930  005624  004137  007402         T43:    JSR     R1,CHECK
 931  005630  012737  005624  010570         MOV     #T43,LOOP
 932  005636  017737  172642  005724         MOV     @XECSR,PPL              ;SAVE STATUS
 933  005644  012737  011201  007304         MOV     #EE43S,MES              ;SET SUBTEST PRINT
 934  005652  000005                         RESET                   ;CLEAR LATCH
 935  005654  004237  007342                 JSR     R2,WAITX        ;WAIT FOR RELAY
 936  005660  004337  006100                 JSR     R3,OPP
 937  005664  067737  172614  005724         ADD     @XECSR,PPL      ;TEST FOR STATUS CHANGE
 938  005672  100415                         BMI     T44             ;IF MINUS STATUS CHANGED
 939  005674  004537  010520                 JSR     R5,ERROR
 940  005700  012737  011145  007304         MOV     #EE43,MES
 941  005706  004337  007210                 JSR     R3,PRINT
 942  005712  004537  010536                 JSR     R5,SCOPE
 943  005716  000000                         HLT                     ;RESET FAILED TO RELEASE LATCH
 944  005720  000137  005624                 JMP     T43
 945                                         ;
 946                                         ;
 947                                         ;
 948  005724  000000                 PPL:    0                       ;TEST DATA POINT
 949                                         ;
 950                                         ;
 951                                         ;TEST THAT "MANUAL" EXTERNAL ENABLE CIRCUITRY FUNCTIONS
 952                                         ;BY SETTING THE ENABLE FLOP FROM A SWITCHING OF THE BUS
 953                                         ;(VIA TEST CONNECTOR)
 954                                         ;
 955  005726  004137  007402         T44:    JSR     R1,CHECK
 956  005732  012737  005726  010570         MOV     #T44,LOOP
 957  005740  012777  000003  172532         MOV     #3,@XCSR
 958  005746  004237  010350                 JSR     R2,TOUT         ;CLEAR ANY ERROR CONDITIONS
 959  005752  005777  172524                 TST     @XCINT          ;CLEAR FLAGS SHORT LOOP,SECOND CHANCE
 960  005756  012777  000400  172514         MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
 961  005764  005277  172516                 INC     @XSWBU
 962  005770  004237  007342                 JSR     R2,WAITX        ;SWITCH BUSS WAIT FOR RELAY
 963  005774  005277  172500                 INC     @XCSR           ;GENERATE A SHORT LOOP ERROR,RECEIVE FLAG SHOULD
 964  006000  005277  172474                 INC     @XCSR           ;GET SET WITH EXTERNAL ENABLE SET BY SWITCH BUS COMMAND
 965  006004  004237  007342                 JSR     R2,WAITX
 966  006010  032777  040000  172462         BIT     #40000,@XCSR
 967  006016  001014                         BNE     INIT
 968  006020  004537  010520                 JSR     R5,ERROR
```

A3

```
  969  000824  012737  211152  007304          MOV     #EE44,MES
  970  000832  004337  007210                  JSR     R3,PRINT
  971  000836  004537  010536                  JSR     R5,SCOPE
  972  000842  000000                          HLT             ;MANUAL ENABLE INPUT CIRCUITRY FAILED
  973  000844  000137  005726                  JMP     T44
  974                                          ;
  975                                          ;
  976                                          ;
  977
  978                                          ;INITIALIZE THE WORLD AND PRINT PASS FOR EACH
  979                                          ;PASS OF TEST CHECK TELETYPE FOR COMMAND INSTRUCTIONS
  980                                          ;
  981  000850  000005          INIT:   RESET                   ;INITIALIZE WORLD
  982  000852  012737  211233  007304          MOV     #PASS,MES       ;SET PASS PRINT
  983  000860  004337  007210                  JSR     R3,PRINT        ;
  984  000864  004137  007402                  JSR     R1,CHECK        ;CHECK FOR TELTYPE COMMANDS
  985  000870  012706  000600                  MOV     #STACK,SP
  986  000874  000137  001030                  JMP     T1
  987                                          ;
  988                                          ;
  989                                          ;SUBROUTINE TO TEST THAT STATUS A&B ARE OF ADJACENT
  990                                          ;POLARITY, THIS ROUTINE IS USED AS A SUBTEST.
  991                                          ;
  992  001000  005777  172400          OPP:    TST     @XECSR          ;TEST BIT 15 OF ESCR
  993  001004  100004                          BPL     .+12
  994  001006  105777  172372                  TSTB    @XECSR          ;BIT 15=1 TEST BIT 7
  995  001012  100405                          BMI     .+14            ;REPORT A&B SAME
  996  001014  000203                          RTS     R3
  997  001016  105777  172362                  TSTB    @XECSR  ;15=1 7=0
  998  001022  100001                          BPL     .+4     ;REPORT BOTH SAME
  999  001024  000203                          RTS     R3
 1000  001026  004537  010520                  JSR     R5,ERROR
 1001  001032  000240                          NOP
 1002  001034  000240                          NOP
 1003  001036  000240                          NOP
 1004  001040  004337  007210                  JSR     R3,PRINT
 1005  001044  004537  010536                  JSR     R5,SCOPE
 1006  001050  000000                          HLT
 1007  001052  000177  002412                  JMP     @LOOP           ;LOOP ON FAILING TEST
 1008  001056  000203                          RTS     R3              ;OK 15=1 7=0
 1009  001060  105777  172320                  TSTB    @XECSR          ;15=0 TEST 7
 1010  001064  100001                          BPL     .+4             ;REPORT BOTH SAME
 1011  001066  000203                          RTS     R3              ;OK 15=0 7=1
 1012  001070  004537  010520                  JSR     R5,ERROR        ;CHECK FOR ERROR REPORT
 1013  001074  000240                          NOP
 1014  001076  000240                          NOP
 1015  001100  000240                          NOP
 1016  001102  004237  007210                  JSR     R2,PRINT
 1017  001106  004537  010536                  JSR     R5,SCOPE
 1018  001112  000000                          HLT
 1019  001114  000177  002350                  JMP     @LOOP           ;LOOP ON FAILING TEST
 1020                                          ;
 1021                                          ;
 1022                                          ;
```

B3

```
1024
1025                                                    ;
1026                                                    ;
1027                                                    ;*****************************************
1028                                                    ;DELAY ADJJSTMENT TEST
1029                                                    ;*****************************************
1030  000220  012737  000340  177776  DELAY1: MOV     #340,PS          ;KEEP STATUS AT 7 FOR ENTIRE TEST
1031  000226  104000                        NULL
1032  000230  000005                        RESET
1033  000232  104000                        NULL
1034  000234  012737  011277  007394        MOV     #DELTST,MES      ;PRINT "DELAY ADJUST TEST"
1035  000242  004337  007210                JSR     R3,PRINT
1036  000246  012737  011327  007394  LREP1: MOV     #ASK,MES         ;ASK FOR DELAY 1, 2
1037  000254  004337  007210                JSR     R3,PRINT
1038  000260  004137  007306                JSR     R1,REC           ;RECIEVE ONE CHARACTER FROM TELE
1039  000264  004337  007172                JSR     R3,ECHO          ;ECHO CHARACTER
1040  000270  023727  007176  000261        CMP     WLD,#261
1041  000276  001413                        BEQ     D1               ;RUN DELAY 1 (RECEIVE) TIMING TEST
1042  000300  023727  007176  000262        CMP     WLD,#262
1043  000306  001432                        BEQ     D2               ;RUN DELAY 2 (WARNING & S.L.) TIMING TEST
1044  000310  012737  011402  007394        MOV     #QU,MES          ;PRINT A ?
1045  000316  004337  007210                JSR     R3,PRINT
1046  000322  000137  000246                JMP     LREP             ;REPEAT LINE
1047                                                    ;
1048                                                    ;
1049  000326  012737  000340  177776  D1:    MOV     #340,PS
1050  000334  012777  000400  172136        MOV     #000400,@XCSR    ;CLEAR RECEIVE FLAG
1051  000342  012777  000003  172130        MOV     #3,@XCSR         ;PULSE WORNING FLAG DELAY
1052  000350  032777  040000  172122        BIT     #040000,@XCSR    ;MONITOR BIT 14
1053  000356  001774                        BEQ     .-6
1054  000360  004237  010350                JSR     R2,TOUT          ;WAIT APPROX 10.-6 SEC
1055  000364  004137  007402                JSR     R1,CHECK
1056  000370  000137  000326                JMP     D1
1057                                                    ;RUN WARNING FLAG & SHORT LOOP DELAY TIMING TESTS
1058                                                    ;
1059  000374  012737  000340  177776  D2:    MOV     #340,PS
1060  000402  005777  172074                TST     @XCINT           ;CLEAR FLAG
1061  000406  012777  000001  172064        MOV     #1,@XCSR         ;PULSE ALARM DELAY
1062  000414  105777  172060                TSTB    @XCSR            ;TEST BIT 7
1063  000420  100375                        BPL     .-4
1064  000422  004237  007342                JSR     R2,WAITX
1065  000426  004137  007402                JSR     R1,CHECK         ;CHECK FOR TELETYPE COMMANDS
1066  000432  000137  000374                JMP     D2               ;RECYCLE
1067                                                    ;
1068                                                    ;
```

```
1070                                                    ;
1071                                                    ;
1072                                                    ;.....................................................
1073                                                    ;DYNAMIC SYSTEM TEST
1074                                                    ;.....................................................
1075                                                    ;
1076                                                    ;
1077  000436  012737  011463  007334  DYNAMI:  MOV     #DYTST,MES
1078  000444  004337  007210                  JSR     R3,PRINT
1079  000450  104000                          NULL
1080  000452  000005                          RESET
1081  000454  004137  007402          DYX:    JSR     R1,CHECK
1082  000460  017737  172020  007056          MOV     @XECSR,SIRE     ;SAVE STATUS
1083  000466  012737  000340  177776          MOV     #340,PS         ;SET STATUS
1084  000474  012704  000562                  MOV     #HORN,R4        ;SET INT. RETURN
1085  000500  012705  000562                  MOV     #HORN,R5
1086  000504  012737  000120  007054          MOV     #120,COUNT      ;SET COUNTER FOR 100 PASSES
1087  000512  012777  000103  171700  PTI:    MOV     #103,@XCSR      ;START TIMING, ENABLE ALARM OUT
1088  000520  013737  000510  177776          MOV     @RIV,PS         ;STATUS=6
1089  000526  000240                          NOP
1090  000530  000137  000526                  JMP     .-2             ;STAY HERE WAIT FOR INTERRUPT
1091  000534  012737  011502  007334  HERE:   MOV     #SLF,MES        ;SHORT LOOP FLAG SET
1092  000542  004337  007210                  JSR     R3,PRINT
1093  000546  004237  010350                  JSR     R2,TOUT         ;TIME OUT DELAYS
1094  000552  005777  171724                  TST     @XCINT          ;CLEAR FLAGS
1095  000556  000137  000512                  JMP     PT              ;RECYCLE TEST
1096  000562  005777  171712          HORN:   TST     @XCSR           ;FIND WHO GAVE INTERRUPT
1097  000566  100762                          BMI     HERE
1098  000570  105777  171704                  TSTB    @XCSR           ;CHECK BIT 7
1099  000574  100407                          BMI     OKK             ;ALL RIGHT GO
1100  000576  032777  040000  171674          BIT     #040000,@XCSR   ;NOT BIT 7 SO TRY 14
1101  000604  001505                          BEQ     ERR             ;ILLEGAL INT.
1102  000606  105777  171666                  TSTB    @XCSR
1103  000612  100375                          BPL     .-4
1104  000614  032777  040000  171656  OKK:    BIT     #040000,@XCSR   ;BIT 7=1 WAIT FOR 14
1105  000622  001774                          BEQ     .-6
1106  000624  005777  171652                  TST     @XCINT          ;CLEAR FLAGS SHORT LOOP, SECOND CHANCE
1107  000630  012777  000400  171642          MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
1108  000636  005277  171644                  INC     @XSWBU          ;SWITCH BUS
1109  000642  004237  007342                  JSR     R2,WAITX
1110  000646  067737  171632  007056          ADD     @XECSR,SIRE
1111  000654  100410                          BMI     CLST            ;BR IF STATUS CHANGED
1112  000656  104000                          NULL
1113  000660  012737  011532  007334          MOV     #BBS,MES        ;REPORT EXT. STATUS BAD
1114  000666  004337  007210                  JSR     R3,PRINT
1115  000672  000137  000454                  JMP     DYX
1116  000676  017737  171602  007056  CLST:   MOV     @XECSR,SIRE
1117  000704  000005                          RESET                   ;CLEAR LATCH
1118  000706  004237  007342                  JSR     R2,WAITX
1119  000712  067737  171566  007056          ADD     @XECSR,SIRE
1120  000720  100410                          BMI     TIKE
1121  000722  104000                          NULL
1122  000724  012737  011532  007334          MOV     #BBS,MES
1123  000732  004337  007210                  JSR     R3,PRINT
```

```
1124   000736  000137  000454          JMP     DYX
1125   000742  005337  007054  TIME:   DEC     COUNT
1126   000746  001404                  BEQ     .+12            ;BRANCH WHEN DONE
1127   000750  004137  007402          JSR     R1,CHECK
1128   000754  000137  000512          JMP     PT
1129   000760  012737  000340  177776  MOV     #340,PS
1130   000766  104000                  NULL
1131   000770  012737  011233  007304  MOV     #PASS,MES
1132   000776  004337  007210          JSR     R3,PRINT
1133   007002  104000                  NULL
1134   007004  004237  010350          JSR     R2,TOUT
1135   007010  004237  010350          JSR     R2,TOUT
1136   007014  000137  000454          JMP     DYX
1137   007020  012737  011527  007304  ERR:    MOV     #IINT,MES
1138   007026  004337  007210          JSR     R3,PRINT
1139   007032  004237  010350          JSR     R2,TOUT
1140   007036  005777  171440          TST     @XCINT          ;CLEAR SHORT LOOP,SECOND CHANCE
1141   007042  012777  000400  171430  MOV     #000400,@XCSR   ;CLEAR RECEIVE FLAG
1142   007050  000137  000512          JMP     PT
1143   007054  000000          COUNT:  0
1144   007056  000000          SIRE:   0
1145                                   ;
1146                                   ;
1147                                   ;
1148                                   ;PRINT HEADER ROUTINE AND RECIEVE TELETYPE COMMANDS
1149                                   ;TO SPECIFY DESIRED TESTS
1150                                   ;
1151   007060  005037  177562  HEADER: CLR     TKB             ;CLEAR DONE OF READER STATUS
1152   007064  012737  011405  007304  MOV     #HEAD,MES
1153   007072  004337  007210          JSR     R3,PRINT        ;ASK FOR DESIRED TEST
1154   007076  004137  007306          JSR     R1,REC          ;RECIEVE ONE CHARACTER
1155   007102  004337  007172          JSR     R3,ECHO         ;ECHO TELEREADER CHARACTER
1156   007106  023727  007170  000261  CMP     HLD,#261        ;TEST A=LOGIC TEST
1157   007114  001417                  BEQ     TA
1158   007116  023727  007170  000262  CMP     HLD,#262        ;TEST B=TIME DELAY TEST
1159   007124  001415                  BEQ     TB
1160   007126  023727  007170  000263  CMP     HLD,#263        ;TEST C=SYSTEM STATUS TEST
1161   007134  001413                  BEQ     TC
1162   007136  012737  011402  007304  MOV     #QU,MES         ;TYPE ?
1163   007144  004337  007210          JSR     R3,PRINT
1164   007150  000137  007060          JMP     HEADER          ;ILLEGAL CHARACTER TRY AGAIN
1165   007154  000137  001000          TA:     JMP     LOGIC   ;LOGIC TEST
1166   007160  000137  006220          TB:     JMP     DELAY   ;DELAY TIME LOOP
1167   007164  000137  006436          TC:     JMP     DYMAN   ;DYNAMIC TEST
1168   007170  000000          HLD:    0                       ;HOLD TEST DESIRED
```

```
1170                                                    ;
1171                                                    ;ECHO CHARACTER IN TELETYPE BUFFER REGISTER
1172  007172  013737  177562  177566  ECHO:   MOV     TKB,TYDB        ;READER BUFFER TO PRINTER BUFFER
1173  007200  105737  177564                  TSTB    TYSR            ;TEST PRINTER STATUS
1174  007204  100375                          BPL     .-4
1175  007206  000203                          RTS     R3
1176                                                    ;PRINT DATA SPECIFIED BY LEADING ADDRESS IN REGISTER 4
1177                                                    ;UNTIL TERMINATED BY (0)
1178  007210  104000                  PRINT:  NULL
1179  007212  013704  007304                  MOV     MES,R4
1180  007216  112437  007302                  MOVB    (R4)+,DBUF
1181  007222  122737  000100  007302          CMPB    #100,DBUF
1182  007230  001422                          BEQ     DONE
1183  007232  122737  000045  007302          CMPB    #45,DBUF
1184  007240  001004                          BNE     OUT
1185  007242  004237  010466                  JSR     R2,LFCR
1186  007246  000137  007216                  JMP     PRINT+6
1187  007252  004537  007260          OUT:    JSR     R5,PRT
1188  007256  000757                          BR      PRINT+6
1189                                                    ;
1190  007260  113737  007302  177566  PRT:    MOVB    DBUF,TYDB
1191  007266  105737  177564                  TSTB    TYSR
1192  007272  100375                          BPL     .-4
1193  007274  000205                          RTS     R5
1194  007276  104000                  DONE:   NULL
1195  007300  000203                          RTS     R3
1196  007302  000000                  DBUF:   0
1197  007304  000000                  MES:    0
1198                                                    ;
1199                                                    ;
1200                                                    ;RECEIVE ONE CHARACTER FROM TELETYPE READER
1201                                                    ;BUFFER AND STORE IN LOC. "HLD"
1202                                                    ;
1203  007306  105737  177560          REC:    TSTB    TKS             ;WAIT FOR KEYBOARD
1204  007312  100375                          BPL     .-4
1205  007314  013737  177562  007170          MOV     TKB,HLD         ;MOV DATA TO LOC. HLD
1206  007322  000201                          RTS     R1
1207                                                    ;
1208                                                    ;
1209                                                    ;5 MILLI-SEC LOOP
1210
1211  007324  012737  001750  010426  WAIT:   MOV     #1750,TIMI
1212  007332  005337  010426                  DEC     TIMI
1213  007336  001375                          BNE     .-4
1214  007340  000202                          RTS     R2
1215                                                    ;
1216                                                    ;WAIT 5 MILLI SEC.
1217                                                    ;
1218  007342  013737  007360  010426  WAITX:  MOV     SPEED,TIMI      ;LOAD FOR 5 MILLISEC
1219  007350  005337  010426                  DEC     TIMI
1220  007354  001375                          BNE     .-4
1221  007356  000202                          RTS     R2
1222  007360  177777                  SPEED:  177777          ;5 MILLI SEC CONST
1223                                                    ;
```

F3

```
1224                                                    ;
1225                                                    ;RETURN FROM SHORT LOOP & WARNING INTERRUPTS
1226                                                    ;
1227  007362  012706  000600          WAOG:   MOV     #STACK,SP       ;FORCE INTERRUPT RETURN OF SHORTLOOP & WARNING
1228  007366  010467                          MOV     R4,PC
1229  007370  000000                          HLT                     ;SHOULD NEVER GET HERE
1230                                                    ;
1231                                                    ;RETURN FROM RECIEVE FLAG INTERRUPTS
1232  007372  012706  000600          RECF:   MOV     #STACK,SP
1233  007376  010567                          MOV     R5,PC           ;FORCE INT RET OF REC
1234  007400  000000                          HLT
1235                                                    ;
1236                                                    ;
1237                                                    ;
1238                                                    ;
1239                                                    ;
1240                                                    ;CHECK FOR COMMANDS TO MONITOR
1241                                                    ;TEST REQUIRED
1242                                                    ;
1243                                                    ;
1244  007402  032737  000001  177570  CHECK:  BIT     #1,SR
1245  007410  001001                          BNE     .+4
1246  007412  000201                          RTS     R1
1247  007414  012777  000003  171056          MOV     #3,@XCSR
1248  007422  004237  010410                  JSR     R2,TOUT1
1249  007426  000005                          RESET
1250  007430  005777  171046                  TST     @XCINT          ;CLEAR FLAGS
1251  007434  000137  007060                  JMP     HEADER
1252                                                    ;
1253                                                    ;
1254                                                    ;
1255                                                    ;
1256                                                    ;WHEN VECTORS 170 & 174 ARE INCORRECTLY ASSERTED
1257                                                    ;ENTER ROUTINE, REPORT ERROR AND RETURN TO FAILING TEST
1258                                                    ;
1259                                                    ;
1260  007440  012737  011241  007334  WRNG:   MOV     #WRONG,MES
1261  007446  004337  007210                  JSR     R3,PRINT
1262  007452  005726                          TST     (SP)+
1263  007454  012776  000340  000020          MOV     #340,@(SP)      ;SET RETURN STATUS TO 7
1264  007462  005746                          TST     -(SP)
1265  007464  000002                          RTI                     ;RETURN TO FAILING TEST
1266                                                    ;
1267                                                    ;BUSS TIME-OUT ERROR SUBROUTINE
1268                                                    ;
1269                                                    ;
1270  007466  004537  010520          TOBE:   JSR     R5,ERROR
1271  007472  012737  011207  007334          MOV     #TOER,MES       ;REPORT TIME OUT ERROR
1272  007500  004337  007210                  JSR     R3,PRINT
1273  007504  000240                          NOP
1274  007506  000002                          RTI
1275                                                    ;
1276                                                    ;
1277                                                    ;SUBROUTINE FOR INPUTTING ADDRESSES AND VECTORS
```

```
1278                                                    ;
1279                                                    ;
1280   007510  012737  011576  007304  ADDMOD: MOV     #ASK1,MES       ;ASK FOR "FIRST DEVICE ADD"
1281   007516  004337  007210                  JSR     R3,PRINT
1282   007522  005037  010334                  CLR     ADDRES
1283   007526  004137  007306          MOD:    JSR     R1,REC          ;REC A CHARACTER
1284   007532  004337  007172                  JSR     R3,ECHO
1285   007536  022737  000215  007170          CMP     #215,HLD        ;TEST FOR A C.R.
1286   007544  001416                          BEQ     SET
1287   007546  006337  010334                  ASL     ADDRES
1288   007552  006337  010334                  ASL     ADDRES
1289   007556  006337  010334                  ASL     ADDRES
1290   007562  042737  177770  007170          BIC     #177770,HLD
1291   007570  063737  007170  010334          ADD     HLD,ADDRES
1292   007576  000137  007526                  JMP     MOD
1293   007602  005737  010334          SET:    TST     ADDRES
1294   007606  001425                          BEQ     STRB
1295   007610  013737  010334  003500          MOV     ADDRES,XCSR     ;SET DEVICE ADDRESS
1296   007616  062737  000002  010334          ADD     #2,ADDRES
1297   007624  013737  010334  003502          MOV     ADDRES,XCINT
1298   007632  062737  000002  010334          ADD     #2,ADDRES
1299   007640  013737  010334  003504          MOV     ADDRES,XECSR
1300   007646  062737  000002  010334          ADD     #2,ADDRES
1301   007654  013737  010334  003506          MOV     ADDRES,XSWBU
1302   007662  000240          STRB:   NOP
1303   007664  012737  011625  007304          MOV     #ASK2,MES       ;ASK FIRST INT. VECTOR
1304   007672  004337  007210                  JSR     R3,PRINT
1305   007676  005037  010336                  CLR     VADDR           ;CLR VECTOR ADDRESS
1306   007702  004137  007306          MODA:   JSR     R1,REC
1307   007706  004337  007172                  JSR     R3,ECHO
1308   007712  022737  000215  007170          CMP     #215,HLD        ;TEST FOR C.R.
1309   007720  001416                          BEQ     SETA
1310   007722  006337  010336                  ASL     VADDR
1311   007726  006337  010336                  ASL     VADDR
1312   007732  006337  010336                  ASL     VADDR
1313   007736  042737  177770  007170          BIC     #177770,HLD
1314   007744  063737  007170  010336          ADD     HLD,VADDR
1315   007752  000137  007702                  JMP     MODA
1316   007756  005737  010336          SETA:   TST     VADDR
1317   007762  001438                          BEQ     STRBA
1318   007764  042737  177000  010336          BIC     #177000,VADDR
1319   007772  012777  007362  003336          MOV     #WAOS,@VADDR
1320   010000  062737  000002  010336          ADD     #2,VADDR
1321   010006  012777  000340  003322          MOV     #340,@VADDR
1322   010014  062737  000002  010336          ADD     #2,VADDR
1323   010022  012777  007372  003336          MOV     #RECF,@VADDR
1324   010030  062737  000002  010336          ADD     #2,VADDR
1325   010036  012777  000340  003272          MOV     #340,@VADDR
1326   010044  012737  011651  007304  STRBA:  MOV     #ASK3,MES       ;ASK FOR VECTOR LEVEL
1327   010052  004337  007210                  JSR     R3,PRINT
1328   010056  004137  007306                  JSR     R1,REC          ;REC ONE CHARACTERS
1329   010062  004337  007172                  JSR     R3,ECHO
1330   010066  022737  000215  007170          CMP     #215,HLD
1331   010074  001407                          BEQ     .+20
```

#3

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1332  010076  022737  000264  007170          CMP     #264,HLD        ;CHECK FOR A 4
1333  010104  001004                          BNE     .+12
1334  010106  012737  000140  003510          MOV     #140,PRIV       ;SET PRIORITY AT 3
1335  010114  000437                          BR      PROTIM
1336  010116  022737  000265  007170          CMP     #265,HLD
1337  010124  001004                          BNE     .+12
1338  010126  012737  000200  003510          MOV     #200,PRIV
1339  010134  000427                          BR      PROTIM
1340  010136  022737  000266  007170          CMP     #266,HLD
1341  010144  001004                          BNE     .+12
1342  010146  012737  000240  003510          MOV     #240,PRIV
1343  010154  000417                          BR      PROTIM
1344  010156  022737  000267  007170          CMP     #267,HLD
1345  010164  001004                          BNE     .+12
1346  010166  012737  000300  003510          MOV     #300,PRIV
1347  010174  000407                          BR      PROTIM
1348  010176  012737  011402  007304          MOV     #QU,*ES
1349  010204  004337  007210                  JSR     R3,PRINT
1350  010210  000137  010044                  JMP     STRBA           ;TRY AGAIN
1351  010214  012737  011677  007304  PROTIM: MOV     #ASK4,*ES
1352  010222  004337  007210                  JSR     R3,PRINT
1353  010226  004137  007306                  JSR     R1,REC
1354  010232  004337  007172                  JSR     R3,ECHO
1355  010236  022737  000301  007170          CMP     #301,HLD
1356  010244  001004                          BNE     .+12
1357  010246  012737  001500  007360          MOV     #1500,SPEED
1358  010254  000417                          BR      KA
1359  010256  022737  000302  007170          CMP     #302,HLD
1360  010264  001004                          BNE     .+12
1361  010266  012737  003000  007360          MOV     #3000,SPEED
1362  010274  000407                          BR      KA
1363  010276  022737  000303  007170          CMP     #303,HLD
1364  010304  001004                          BNE     .+12
1365  010306  012737  006000  007360          MOV     #6000,SPEED
1366  010314  000205                  KAI     RTS     R5
1367  010316  012737  011402  007304          MOV     #QJ,*ES
1368  010324  004337  007210                  JSR     R3,PRINT
1369  010330  000137  010214                  JMP     PROTIM
1370
1371                                          ;
1372  010334  000000                  ADDRES: 0
1373  010336  000000                  VADDR:  0
```

I3

```
1375                                                    ;
1376  010340  012706  000600          TIMEX:  MOV     #STACK,SP       ;REINITIALIZE THE STACK
1377  010344  011467                          MOV     (R4),PC         ;FORCE RETURN FROM INTERRUPT
1378  010346  000000                          HLT                     ;SHOULD NEVER GET HERE
1379                                                    ;
1380                                                    ;RUN DELAY TIME OUTS,TOTAL TIME AS PER
1381                                                    ;PROCESSOR TIME 85=4SEC,& 40=3 SEC&
1382                                                    ;
1383                                                    ;
1384  010350  105737  177570          TOUT:   TSTB    SR
1385  010354  000415                          BR      TOUT1           ;CHANGE TO BPL TO RUN A FAST MODE FOR
1386  010356  012737  000012  010424          MOV     #12,CNTIM       ;T1,T2,T3<50 MILLI-SEC
1387  010364  013737  007360  010426  RA:     MOV     SPEED,TIMI      ;50 MILLI SEC. WORTH
1388  010372  005337  010426                  DEC     TIMI
1389  010376  001375                          BNE     .-4
1390  010400  005337  010424                  DEC     CNTIM
1391  010404  001367                          BNE     RA
1392  010406  000202                          RTS     R2              ;GO WHEN DONE
1393                                                    ;RUN LONG TIME OUT FOR ALL DELAYS HERE
1394  010410  012737  000005  010426  TOUT1: MOV     #5,TIMI         ;SET COUNT TIME
1395  010416  004437  010572                  JSR     R4,TIME
1396  010422  000202                          RTS     R2
1397  010424  000000                  CNTIM:  0
1398  010426  000000                  TIMI:   0
1399                                                    ;
1400                                                    ;
1401  010430  000240                  NULPRT: NOP
1402  010432  105737  177564                  TSTB    TYSR
1403  010436  100375                          BPL     .-4
1404  010440  005037  177566                  CLR     TYDB
1405  010444  105737  177564                  TSTB    TYSR
1406  010450  100375                          BPL     .-4
1407  010452  005037  177566                  CLR     TYDB
1408  010456  105737  177564                  TSTB    TYSR
1409  010462  100375                          BPL     .-4
1410  010464  000002                          RTI
1411                                                    ;
1412                                                    ;
1413  010466  012737  000215  177566  LFCR:   MOV     #215,TYDB       ;CARRIAGE RET.
1414  010474  105737  177564                  TSTB    TYSR
1415  010500  100375                          BPL     .-4
1416  010502  012737  000212  177566          MOV     #212,TYDB
1417  010510  105737  177564                  TSTB    TYSR
1418  010514  100375                          BPL     .-4
1419  010516  000202                          RTS     R2
1420                                                    ;
1421                                                    ;
1422                                                    ;
1423                                                    ;CHECK FOR ERROR PRINT OUT (BIT 13 OF SWITCH REG.)
1424  010520  032737  020000  177570  ERROR:  BIT     #20000,SR
1425  010526  001402                          BEQ     .+6             ;IF BIT 13=0 PRINT ERROR
1426  010530  062705  000012                  ADD     #12,R5          ;ADD VALUE TO OMIT ERROR PRINT
1427  010534  000205                          RTS     R5
1428                                                    ;
```

```
1429                                                    ;CHECK FOR SCOPE LOOP (BIT 14 OF SWITCH REG.)
1430  010536  013737  177570  013566  SCOPE:  MOV     SR,ESTAT
1431  010544  032737  040000  013566          BIT     #040000,ESTAT   ;TEST BIT 14 OF SWITCH REGISTER
1432  010552  001404                          BEQ     .+12            ;IF BIT 14=1 RUN SCOPE
1433  010554  012706  000600                  MOV     #STACK,SP
1434  010560  013727  010570                  MOV     LOOP,PC         ;FORCE RETURN TO TEST
1435  010564  000205                          RTS     R5              ;RETURN AND HLT
1436  010566  000000          ESTAT:  0
1437  010570  000000          LOOP:   0
1438                                                    ;
1439                                                    ;RUN TIME INCREMENTS IN VALUES STORED IN TIMI
1440  010572  005037  010614          TIME:   CLR     XES
1441  010576  005237  010614                  INC     XES             ;COUNT LOOP
1442  010602  001375                          BNE     .-4             ; *
1443  010604  005337  010426                  DEC     TIMI            ;NUMBER OF COUNT LOOPS
1444  010610  001372                          BNE     .-12
1445  010612  000204                          RTS     R4
1446  010614  000000          XES:    0
1447                                                    ;MESSAGES
1448  010616     000                          .BYTE
1449  010617     045  047514  044527  LTI:    .ASCII  /%LOGIC TEST%0/
      010624  020103  042524  052123
      010632  040045
1450  010634  030524  040045          EEI:    .ASCII  /T1%9/
1451
1452  010640  031124  040045          EE2:    .ASCII  /T2%9/
1453
1454  010644  031524  040045          EE3:    .ASCII  /T3%9/
1455
1456  010650  032124  040045          EE4:    .ASCII  /T4%9/
1457
1458  010654  032524  040045          EE5:    .ASCII  /T5%9/
1459
1460  010660  033124  040045          EE6:    .ASCII  /T6%9/
1461
1462  010664  033524  040045          EE7:    .ASCII  /T7%9/
1463
1464  010670  034124  040045          EE8:    .ASCII  /T8%9/
1465
1466  010674  034524  040045          EE9:    .ASCII  /T9%9/
1467
1468  010700  030524  022460     188  EEI0:   .ASCII  /T10%0/
1469
1470  010705     124  030461  042045  EE11:   .ASCII  /T11%0/
1471
1472  010712  030524  022462     188  EEI2:   .ASCII  /T12%0/
1473
1474  010717     124  031461  042045  EEI3:   .ASCII  /T13%0/
1475
1476  010724  030524  022464     188  EEI4:   .ASCII  /T14%0/
1477
1478  010731     124  032461  042045  EEI5:   .ASCII  /T15%0/
1479
1480  010736  030524  022466     188  EEI6:   .ASCII  /T16%0/
```

```
1481
1482  010743     124  033461  040045  EE17:   .ASCII  /T17X0/
1483
1484  010750  030524  022470     100  EE18:   .ASCII  /T18X0/
1485
1486  010755     124  034461  040045  EE19:   .ASCII  /T19X0/
1487
1488  010762  031124  022460     100  EE20:   .ASCII  /T20X0/
1489
1490  010767     124  030462  040045  EE21:   .ASCII  /T21X0/
1491
1492  010774  031124  022462     100  EE22:   .ASCII  /T22X0/
1493
1494  011001     124  031462  040045  EE23:   .ASCII  /T23X0/
1495
1496  011006  031124  022464     100  EE24:   .ASCII  /T24X0/
1497
1498  011013     124  032462  040045  EE25:   .ASCII  /T25X0/
1499
1500  011020  031124  022466     100  EE26:   .ASCII  /T26X0/
1501
1502  011025     124  033462  040045  EE27:   .ASCII  /T27X0/
1503
1504  011032  031124  022470     100  EE28:   .ASCII  /T28X0/
1505
1506  011037     124  034462  040045  EE29:   .ASCII  /T29X0/
1507
1508  011044  031524  022460     100  EE30:   .ASCII  /T30X0/
1509
1510  011051     124  030463  040045  EE31:   .ASCII  /T31X0/
1511
1512  011056  031524  022462     100  EE32:   .ASCII  /T32X0/
1513
1514  011063     124  031463  040045  EE33:   .ASCII  /T33X0/
1515
1516  011070  031524  022464     100  EE34:   .ASCII  /T34X0/
1517
1518  011075     124  032463  040045  EE35:   .ASCII  /T35X0/
1519
1520  011102  031524  022466     100  EE36:   .ASCII  /T36X0/
1521
1522  011107     124  033463  040045  EE37:   .ASCII  /T37X0/
1523
1524  011114  031524  022470     100  EE38:   .ASCII  /T38X0/
1525
1526  011121     124  034463  040045  EE39:   .ASCII  /T39X0/
1527
1528  011126  032124  022460     100  EE40:   .ASCII  /T40X0/
1529
1530  011133     124  030464  040045  EE41:   .ASCII  /T41X0/
1531
1532  011140  032124  022462     100  EE42:   .ASCII  /T42X0/
1533
1534  011145     124  031464  040045  EE43:   .ASCII  /T43X0/
```

L3

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 1535
 1536  011152  032124  022464     188  EE441:  .ASCII  /T44%0/
 1537
 1538  011157     124  034863  022523  EE385:  .ASCII  /T385%0/
       011164     188
 1539
 1540  011165     124  030864  022523  EE405:  .ASCII  /T405%0/
       011172     188
 1541
 1542  011173     124  030464  022523  EE415:  .ASCII  /T415%0/
       011200     188
 1543
 1544  011201     124  030464  022523  EE435:  .ASCII  /T415%0/
       011206     188
 1545
 1546  011207     102  051525  042440  TOER:   .ASCII  /BUS ERROR TIME-OUT%0/
       011214  051122  051117  052040
       011222  046511  026505  052517
       011230  022524     188
 1547
 1548  011233     120  051501  022523  PASS:   .ASCII  /PASS%0/
       011240     188
 1549
 1550  011241     124  040522  053120  WRONG:  .ASCII  /TRAPPED TO WRONG INT. VECTOR%0/
       011246  042105  052040  020117
       011254  051127  047117  020107
       011262  047111  027124  053040
       011270  041505  047524  022522
       011276     188
 1551
 1552  011277     045  042504  040514  DELTST: .ASCII  /%DELAY ADJUSTMENT TEST%0/
       011304  020131  042101  052512
       011312  052123  042515  053116
       011320  052040  051505  022524
       011326     188
 1553
 1554  011327     104  046105  054501  ASR:    .ASCII  /DELAY:(1)WATCHDOG,(2)WARNING & SHORT LOOP%0/
       011334  024072  024461  040527
       011342  041524  042110  043517
       011350  024056  024462  040527
       011356  047122  047111  020107
       011364  020046  044123  051117
       011372  020124  047514  053117
       011400  040045
 1555
 1556  011402  022477     188          QUI     .ASCII  /?%0/
 1557
 1558  011405     045  047514  044507  HEAD:   .ASCII  /%LOGIC TEST(1),DELAY TEST(2),DYNAMIC TEST(3)%0/
       011412  020103  042524  052123
       011420  030450  026051  042504
       011426  040514  020131  042524
       011434  052123  031050  026051
       011442  054504  040516  044515
       011450  020103  042524  052123
```

143

```
                011456  031458  722451      138
 1559
 1560           011463     045  054524  043516  DYTST:  .ASCII  /%DYNAMIC TEST%0/
                011470  244515  220103  042524
                011476  052123  040045
 1561
 1562           011502  044123  051117  023124  SLF:    .ASCII  /SHORT LOOP FLAG SET%0/
                011510  047514  050117  043040
                011516  040514  020107  042523
                011524  022524     100
 1563
 1564           011527     111  046114  043505  IINT:   .ASCII  /ILLEGAL INTERRUPT%0/
                011534  046101  044440  052116
                011542  051105  052522  052120
                011550  040045
 1565
 1566           011552  054105  027124  052502  BBS:    .ASCII  /EXT.BUS STATUS BAD%0/
                011560  020123  052123  052101
                011566  051525  041040  042101
                011574  040045
 1567
 1568           011576  043045  051111  052123  ASK1:   .ASCII  /%FIRST DEVICE ADDRESS=0/
                011604  042040  053105  041511
                011612  020105  042101  051124
                011620  051505  036523     100
 1569
 1570           011625     045  044506  051522  ASK2:   .ASCII  /%FIRST INT. VECTOR=0/
                011632  020124  047111  027124
                011640  053040  041505  047524
                011646  036522     100
 1571
 1572           011651     045  051120  047511  ASK3:   .ASCII  /%PRIORITY INT. LEVEL=0/
                011656  044522  054524  044440
                011664  052116  020056  042514
                011672  042526  036514     100
 1573           011677     045  042120  020520  ASK4:   .ASCII  /%PDP-11 (A)=05,10,20 (B)=35,40 (C)=45,50 0/
                011704  030461  024040  024501
                011712  030075  026065  033061
                011720  031054  020060  041050
                011726  036451  032463  032054
                011734  020060  041450  036451
                011742  032464  032454  020060
                011750     100
 1574
 1575                   011752                  .EVEN
 1576                   000001                  .END
```

A4

```
AA1     001322          AA2     001432          AA4     003446          AA5     003626
ADDMO   007510          ADDRES  013334          ASK     011327          ASK1    011576
ASK2    011625          ASK3    011651          ASK4    011677          BBS     011592
CHECK   007402          CINT  = 172402          CLST    006676          CNTIM   010424
COUNT   007054          CSR   = 172410          DBUF    007332          DELAY   006220
DELTST  011277          DONE    007276          DYMAN   006436          DYTST   011463
DYX     006454          D1      006326          D2      006374          ECHO    007172
ECSR  = 172404          EE1     013634          EE10    010730          EE11    010705
EE12    010712          EE13    010717          EE14    010724          EE15    010731
EE16    010736          EE17    010743          EE18    010750          EE19    010755
EE2     010640          EE20    010762          EE21    010767          EE22    010774
EF23    011001          EE24    011006          EE25    011013          EE26    011020
EE27    011025          EE28    011032          EE29    011037          EE3     010644
EE30    011044          EE31    011051          EE32    011056          EE33    011063
EE34    011070          EE35    011075          EE36    011102          EE37    011107
EE38    011114          EE38S   011157          EE39    011121          EE4     010650
EE40    011126          EE40S   011165          EE41    011133          EE41S   011173
EE42    011140          EE43    011145          EE43S   011201          EE44    011152
EE5     010654          EE6     010660          EE7     010664          EE8     010670
EE9     010674          ERR     007020          ERROR   010520          ESTAT   010566
HEAD    011405          HEADER  007060          HERE    006534          HLD     007170
HLT   = 000000          HORN    006562          IINT    011527          INIT    006050
KA      010314          LFCR    013466          LOGIC   001030          LOOP    010570
LREP    006246          LT      013617          MES     007304          MOD     007520
MODA    007702          NOP   = 000240          NULL  = 104000          NULPRT  010430
OKK     006614          OPP     006130          OUT     007252          PASS    011233
PC    =%000007          PPL     005724          PRINT   007210          PRIV    000510
PROTIM  010214          PRT     007260          PS    = 177776          PT      006512
PTR     004226          PTX1    004536          PTX2    004624          PTX3    004732
QU      011402          RA      013364          REC     007306          RECF    007372
R0    =%000000          R1    =%000001          R2    =%000002          R3    =%000003
R4    =%000004          R5    =%000005          SCOPE   010536          SET     007602
SETA    007756          SIRE    007056          SLP     011532          SP    =%000006
SPEED   007360          SR    = 177570          STACK   000620          STRB    007662
STRBA   010044          SWBU  = 172406          TA      007154          TB      007160
TC      007164          TEST    001016          TIME    010572          TIME    006742
TILT    005006          TIME    010572          TIMEX   010340          TIMI    010426
TKB   = 177562          TKS   = 177560          TOBE    007466          TOER    011207
TOUT    010350          TOUT1   010410          TYDB  = 177566          TYSR  = 177564
T1      001030          T10     001752          T11     002030          T12     002112
T13     002172          T14     002270          T15     002332          T16     002410
T17     002526          T18     002560          T19     002622          T2      001110
T20     002664          T21     002730          T22     003020          T23     003114
T24     003212          T25     003330          T26     003470          T27     003644
T28     003752          T29     004052          T3      001170          T30     004120
T31     004244          T32     004326          T33     004414          T34     004520
T35     004642          T36     004744          T37     005040          T38     005126
T39     005232          T4      001246          T40     005322          T41     005424
T42     005534          T43     005624          T44     005720          T5      001352
T6      001462          T7      001534          T8      001610          T9      001706
VADDR   010336          WAIT    007324          WAITX   007342          WADG    007362
WRNG    007440          WRONG   011241          XCINT   000502          XCSR    000500
XECSR   000504          XES     010614          XSWBU   000506          .     = 011752
```

ERRORS DETECTED: 0

*WATCH,WATCH=WATCH.SRC
RUN-TIME: 4 9 8 SECONDS
CORE USED: 4K

C4