

## IDENTIFICATION

PRODUCT CODE:           MAINDEC-11-DZKCC-A-D  
PRODUCT NAME:           BASIC W/R AND MICRO-PROCESSOR TESTS  
DATE:                    MAY 1977  
MAINTAINER:             DIAGNOSTICS  
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1. ABSTRACT

The function of the KMC11 diagnostics is to verify that the option operates according to specifications. The diagnostics verify that there are no malfunctions and that all operations of the KMC11 are correct in its environment.

Parameters must be set up to alert the diagnostics to the KMC11 configuration. These parameters are contained in the STATUS TABLE and are generated in two ways: 1) Manual Input - the operator answers questions. 2) Autosizing - the program determines the parameters automatically.

DZKCC tests the KMC11 micro-processor (MB204). It performs write/read tests on the KMC unibus registers, checks the micro-processor operation, checks out Main Memory, scratch pad memory, the ALU functions as well as interrupts and NPR operation. DZKCC performs no tests on the line unit or any CRAM dependent tests. It will run on KMC11's containing CRAM (IOP). It does not require a line unit to run.

Currently there are four off line diagnostics that are to be run in sequence to insure that if an error should occur it will be detected at an early stage.

NOTE: Additional diagnostics may be added in the future.

The four diagnostics are:

1. DZKCC [REV] Basic W/R and Micro-processor tests
2. DZKCD [REV] Jump and memory tests (Heat test tape)
3. DZKCE [REV] DDCHP Line unit tests
4. DZKCF [REV] BITSTUFF Line unit tests
5. DZKCA [REV] KMC11 CPU MICRO-DIAGNOSTICS.

2. REQUIREMENTS

2.1 EQUIPMENT

Any PDP11 family CPU (except an LSI-11) with minimum 8k memory  
ASR 33 (or equivalent)  
KMC11-AN IOP (MB204)

2.2 STORAGE

Program will use all 8K of memory except where ABL and BOOTSTRAP LOADER reside. Locations 2100 thru 2300; contain the "STATUS TABLE" information which is generated at start of diagnostics by manual input (questions) or automatically (auto-sizing). This area is an overlay area and should not be altered by the operator.

3. LOADING PROCEEDURE

3.1 METHOD

All programs are in absolute format and are loaded using the ABSOLUTE LOADER. NOTE: if the diagnostics are on a media such as DISK, MAGTAPE, DECTAPE, or CASSETTE; follow instructions for the monitor which has been provided on that specific media.

ABSOLUTE LOADER starting address #500

MEMORY \* SIZE

4k	17
8k	37
12k	57
16k	77
20k	117
24k	137
28k	157

- 3.1.1 Place address of ABS loader into switch register.  
(also place 'HALT' SW up)
- 3.1.2 Depress 'LOAD ADDRESS' key on console and release.
- 3.1.3 Depress 'START KEY' on console and release (program should now be loading into CPU)

STARTING PROCEDURE

- a. Set switch register to 000200
- b. Depress 'LOAD ADDRESS' key and release
- c. Set SWR to zero for 'AUTO SIZING' or SWR bit0=1 for manual input (questions) or SWR bit7=1 to use existing parameters set up by a previous start or a previously run KMC11 diagnostic.
- d. Depress 'START KEY' and release. The program will type Maindec Name and program name (if this was the first start up of the program) and also the following:

MAP OF KMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
002100	160010	045310	177777	000000
002110	160020	045320	177777	000000

The program will type 'R' and proceed to run the diagnostic. The above is only an example. This would indicate the status table starting at add. 2100 in the program. In this example the table contains the information and status of two KMC11'S. THE STATUS TABLE MUST BE VERIFIED BY THE USER IF AUTO SIZING IS DONE. For information of status table see section 8.4 for help.

If the diagnostic was started with SW00=1 indicating manual parameter input then the following shows an example of the questions asked and some example answers:

HOW MANY KMC11'S TO BE TESTED?1

01

CSR ADDRESS?160010

VECTOR ADDRESS?310

BR PRIORITY LEVEL? (4,5,6,7)?5

WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF

M8202 TYPE "2"?1

IS THE LOOP BACK CONNECTOR ON?Y

SWITCH PAC#1 (DOCHP LINE#)?377

SWITCH PAC#2 (BMB73 BOOT ADD)?377

Following the questions the status map is printed out as described above, the information in the map reflects the answers to the questions. If the diagnostic was started with SW00=0 and SW07=0 (AUTO-SIZING) then no questions are asked and only the status-map is printed out. If AUTO-SIZING is used the status information must be verified to be correct (match the hardware). If it does not match the hardware the diagnostic must be restarted with SW00=1 and the questions answered.

4.1 CONTROL SWITCH SETTINGS

SW15 Set: Halt on error  
 SW14 Set: Loop on current test  
 SW13 Set: Inhibit error print out  
 SW12 Set: Inhibit type out abell on error.  
 SW11 Set: Inhibit iterations. (quick pass)  
 SW10 Set: Escape to next test on error  
 SW9 Set: Loop with current data  
 SW8 Set: Catch error and loop on it  
 SW7 Set: Use previous status table.  
 SW6 Set: Halt in ROMCLK routine before clocking  
 micro-processor  
 SW5 Set: Reserved  
 SW4 Set: Reserved  
 SW3 Set: Reselect KMC11's desired active  
 SW2 Set: Lock on selected test  
 SW1 Set: Restart program at selected test  
 SW0 Set: Build new status table from questions. (If SW07=0  
 and SW00=0 a new status table is built by  
 auto-sizing)

Switch 06 and 08-15 are dynamic and can be changed as needed while the diagnostic is running. Switches 00-03 and switch 07 are static, and are used only on starting or restarting the diagnostic.

4.1.2 SWITCH REGISTER OPTIONS (at start up)

- SW 01 RESTART PROGRAM AT SELECTED TEST. It is strongly suggested that at least one pass has been made before trying to select a test, the reason being is that the program has to clear areas and set up parameters. When this switch is used the diagnostic will ask TEST NO.? Answer by typing the number of the test desired and carriage return to begin execution at the selected test.
- SW 02 LOCK ON SELECTED TEST. This switch when used with SW01 will cause the program to constantly loop on the selected test. Hitting any key on the console will let it advance to the next test and loop until a key is hit again. If SW02=0 when SW01 is used. The program will begin at the selected test and continue normal operations.
- SW 03 RESELECT KMC11'S DESIRED ACTIVE. Please note that a message is typed out for setting the switch register equal to KMC11's active. This means if the system has four KMC11s; bits 00,01,02,03 will be set in loc 'KMACTV' from the switch register. Using this switch(SW00) alters that location; therefore if four KMC11s are in the system ~~###DO NOT###~~ set switches greater than SW 03 in the up position. This would be a fatal error. do not select more active KMC11s than there is information on in the status table.

METHOD: A: Load address 200  
 B: Start with SW 00=1  
 C: Program will type message  
 D: Set a switch for each KMC desired active.  
 EXAMPLE: If you have 4 KMC's but only want to run the first and the last set SWR bits 0 and 3 = 1. PRESS CONTINUE  
 E: Number (IF VALID) will be in data lights (excluding 11/05)  
 F: Set with any other switch settings desired. PRESS CONTINUE.

### 4.1.3 DYNAMIC SWITCHES

#### ERROR SWITCHES

1. SW 12 Delete print out/bell on error
2. SW 13 Delete error printout.
3. SW 15 Halt on the error.
4. SW 08 Goto beginning of the test(on error).
5. SW 10 Goto next test(on error).

#### SCOPE SWITCHES

1. SW06 Halt in ROMCLK routine before clocking micro-processor instruction. This allows the operator to scope a micro-processor instruction in the static state before it is clocked. Hit continue to resume running.
2. SW09 (if enabled by 'SCOPI') on an error; If an '#' is printed in front of the test no. (ex. #TEST NO. 10) SW09 is incorporated in that test and therefore SW09 is usually the best switch for the scope loop (SW14=0, SW10=0, SW09=1, SW08=0). If SW09 is not enabled; and there is a HARD error (constant); SW08 is best. (SW14=1,0, SW10=0, SW09=0, SW08=1). for intermittent errors; SW14=1 will loop on test regardless of error or not error. (SW14=1, SW10=0, SW09=0, SW08=1,0)
3. SW11 Inhibit iterations.
4. SW14 Loop on current test.

### 4.2 STARTING ADDRESS

Starting address is at 000200 there are no other starting addresses for the KMC11 diagnostics. (See Section 4.0)

NOTE: If address 000042 is non-zero the program assumes it is under ACT11 or XXDP control and will act accordingly after all available KMC11's are tested the program will return to 'XXDP' or 'ACT-11'.

### 5. OPERATING PROCEDURE

When program is initially started messages as described in section 4.0 will be printed, and program will begin running the diagnostic

## 5.2 PROGRAM AND/OR OPERATOR ACTION

The typical approach should be

1. Halt on error (via SW 15=1) when ever an error occurs.
2. Clear SW 15.
3. Set SW 14: (loop on this test)
4. Set SW 13: (inhibit error print out)

The TEST NUMBER and PC will be typed out and possibly an error message (this depends on the test) to give the operator an idea as to the source of the problem. If it is necessary to know more information concerning the error report; LOOK IN THE LISTING for that TEST NUMBER which was typed out and then NOTE THE PC of the ERROR REPORT this way the EXACT FUNCTION of the test CAN BE DETERMINED.

## 6. ERRORS

As described previously there will always be a TEST NUMBER and PC typed out at the time of an error (providing SW 13=0 and SW 12=0). in most cases additional information will be supplied in the the error message to give the operator an indication of the error.

### 6.2 ERROR RECOVERY

If for some reason the KMC11 should 'HANG THE BUS' (gain control of bus so that console manual functions are inhibited) an init or power down/up is necessary for operator to regain control of cpu. If this should happen; look in location 'STSTNM' (address 1202) for the number of the test that was running at the time of the catastrophic error. In this way the operator will have an idea as to what the KMC11 was doing at the time of the error.

## 7. RESTRICTIONS

### 7.1 STARTING RESTRICTIONS

See section 4. (PLEASE)

Status table should be verified regardless of how program was started. Also it is important to use this listing along with the information printed on the TTY to completely isolate problems.



7.2 OPERATING RESTRICTIONS

The first time a KMC11 diagnostic is loaded into core and run the STATUS TABLE must be set up. This is done by manual input (SM00=1) or by autosizing (SM00=0 and SM07=0). Thereafter however the status table need not be setup by subsequent restarts or even loading the next KMC diagnostic because the STATUS TABLE is overlaid. The current parameters in the STATUS TABLE are used when SM07=1 on start up.

7.3 HARDWARE CONFIGURATION RESTRICTIONS

KMC11 IOP(MB204)- Jumper W1 must be in,

8. MISCELLANEOUS

8.1 EXECUTION TIME

All KMC11 device diagnostics will give an 'END PASS' message (providing no errors and sw12=0) within 4 mins. This is assuming SM11=1 (DELETE ITERATIONS) is set to give the fastest possible execution. The actual execution time depends greatly on the POP11 CPU configuration and the amount of memory in the system.

8.2 PASS COMPLETE

NOTE: EVERY time the program is started; the tests will run as if SM11 (delete iterations) was up (=1). This is to 'VERIFY NO HARD ERRORS' as soon as possible. Therefore the first pass -EACH TIME PROGRAM IS STARTED- will be a 'QUICK PASS' until all KMC11's in system are tested. When the diagnostic has completed a pass the following is an example of the print out to be expected.

END PASS DZKCC CSR: 175000 VEC: 0300 PASSES: 000001  
ERRORS: 000000

NOTE: The pass count and error counts are cumulative for each KMC11 that is running, and are set to zero only when the diagnostic is started. Therefore after an overnight run for example, the total passes and errors for each KMC11 since the diagnostic was started are reflected in PASSES: and ERRORS:.

8.4 KEY LOCATIONS

- SLPADR (1206) Contains the address where program will return when iteration count is reached or if loop on test is asserted.
- NEXT (1442) Contains the address of the next test to be performed.
- STSTNM (1202) Contains the number of the test now being performed.
- RUN (1500) The bit in 'RUN' always points to the KMC11 currently being tested. EXAMPLE: (RUN) 1500/00000000100000 Means that KMC11 no.06 is the KMC11 now running.

KMC00-KMC17  
KMS00-KMS17  
(2100)-(2300)

These locations contain the information needed to test up to 16 (decimal) KMC11s sequentially. they contain the CSR VECTOR and STATUS concerning the configuration of each KMC11.

- KMACTV (1306) Each bit set in this location indicates that the associated KMC11 will be tested in turn. EXAMPLE: (KMACTV) 1470/000000000011111 means that KMC11 no. 00,01,02,03,04 will be tested. EXAMPLE: (KMACTV) 1470/000000000010001 Means that KMC11 no. 00,04 will be tested.
- KMCSR (2066) Contains the CSR of the current KMC11 under test.

8.4A 'STATUS TABLE' (2100-2300)

The table is filled by AUTO SIZING or by the manual parameter input (questions) as described previously. Also if desired by user; the locations may be altered by hand (toggled in) to suit the specific configuration.

The example status map shown below contains information for two KMC11'S. the table can contain up to 16 KMC11'S. Following the map is a description of the bits for each map entry

MAP OF KMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
002100	160010	045310	177777	000000
002110	160020	016320	000000	000000

Each map entry contains 4 words which contain the status information for 1 KMC11. The PC shows where in core memory the first of the 4 words is. In the example above the first KMC'S status is in locations, 2100, 2102, 2104, and 2106. The second KMC status is located at 2110, 2112, 2114, and 2116. The information contained in each 4 word entry is defined as follows:

- CSR:     Contains KMC11 CSR address
- STAT1:  BITS 00-08 IS KMC11 VECTOR ADDRESS  
           BIT14=1 TURNAROUND CONNECTOR IS ON  
           BIT14=0 NO TURNAROUND CONNECTOR  
           BIT13=0 LINE UNIT IS AN MB201  
           BIT13=1 LINE UNIT IS AN MB202  
           BIT12=1 NO LINE UNIT  
           BITS 09-11 IS KMC11 BR PRIORITY LEVEL
- STAT2:  LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)  
           HIGH BYTE IS SWITCH PAC#2 (BMB73 BOOT ADD)
- STAT3:  NOT USED

## 8.5 METHOD OF AUTO SIZING

## 8.5.1 FINDING THE CONTROL STATUS REGISTER.

The auto-sizing routine finds a KMC11 as follows: It starts at address 160000 and tests all address in increments of 10 up to and including address 167760. If the address does not time out, the following is done, the first CROM address is written to a 125252 then it is read back. If it contains a -1 or 125252 a KMC11 has been found, if not, the address is updated by 10 and the search continues. A -1 indicates a KMC11 with no CROM, and a 125252 indicates a KMC11 with CROM. Further tests are performed at this point to determine which line unit, if any, is installed, if a loop-back connector is installed and various switch settings on the line unit. THIS IS WHY THE STATUS TABLE MUST BE VERIFIED BY THE USER AND IF ANY OF THE INFORMATION DOES NOT AGREE WITH THE HARDWARE THE DIAGNOSTIC MUST BE RESTARTED AND THE QUESTIONS MUST BE ANSWERED. All KMC11's in the system will be found by the auto-sizer. If it does not find a KMC11 the diagnostic must be restarted and the questions answered.

## 8.5.2 FINDING THE VECTOR AND BR LEVEL

The vector area (address 300-776) is filled with the instruction IOT and '+2' (next address). The processor status is started at 7 and the KMC is programmed to interrupt. The PS is lowered by 1 until the KMC interrupts, a delay is made and if no interrupt occurs at PS level 3 (because of a bad KMC11) the program assumes vector address 300 at BR level 5 and the problem should be fixed in the diagnostic. Once the problem is fixed; the program should be re-setup again to get correct vector. If an interrupt occurred; the address to which the KMC11 interrupted to is picked up and reported as the vector. NOTE: if the vector reported is not the vector set up by you; there is a problem and AUTO SIZING should not be done.

## 8.5 SOFTWARE SWITCH REGISTER

If the diagnostic is run on an 11/04 or other CPU without a switch register then a software switch register is used to allow user the same switch options as described previously. If the hardware switch register does not exist or if one does and it contains all ones (177777) this software switch register is used.

## Control:

To obtain control at any allowable time during execution of the diagnostic the operator types a CTRL G on the console terminal keyboard. As soon as the CTRL G is recognized, by the diagnostic, the following message will be displayed:

SMR=XXXXXX NEW?

Where XXXXXX is the current contents of the software switch register in octal. The software control routine will then await operator action. At which time the operator is required to type one or more of the legal characters: 1) 0 - 7, 2) line feed(<LF>), 3) carriage return(<CR>), or 4) control-U (CTRL U). No check is made for legality. If the input character is not a <LF>, <CR>, or CTRL U it is assumed to be an octal digit.

To change the contents of the SSR the operator simply types the new desired value in octal - leading zeros need not be typed. And terminates the input string with a <CR> or <LF> depending on the program action desired as described below. The input value will be truncated to the last 6 digits typed. At least one digit must be typed on any given input string prior to the terminator before a change to the SSR will occur.

When the input string is terminated with a <CR> the diagnostic will continue execution from the point at which it was interrupted. If a <CR> is the only thing typed the program will continue without changing the SSR. The <LF> differs from the <CR> by restarting the program as if it were restarted at address 200.

If a CTRL U is typed at any point in the input string prior to the terminator the input value will be disregarded and the prompt displayed (SWR = XXXXXX NEW?).

To set the SSR for the starting switches, first load the diagnostic, then hit CTRL G, then start the diagnostic.

APT/ACT/XXDP/SLIDE

\*\*\*\*\*

THIS DIAGNOSTIC IS APT/ACT/XXDP/SLIDE COMPATIBLE USER WOULD BE ABLE TO RUN IT UNDER APT/ACT/XXDP ENVIRONMENT.

NOTE: FOR MANUFACTURING PURPOSE ONLY ITS DESCRIBED HOW TO RUN UNDER APT ENVIRONMENT.

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ETABLE SETTING FOR APT TO RUN UNDER APT

\*\*\*\*\*

FIRST PASS TIME:

LONGEST TEST TIME:

ADDITIONAL TEST TIME:

ALL THE ABOVE PARAMETERS ARE DEPENDENT ON PARTICULAR DIAGNOSTICS AND SHOULD BE LOADED AT THE TIME OF SETTING ETABLE. THERE IS NO DEFAULT TIME SET UP.

SOFTWARE ENVIRONMENT:001 ENVIRONMENT MODE:200

SWITCH 1:-SHOULD BE USED AS NORMAL SWITCH REGISTER.

SWITCH 2:-NOT USED.

CPU OPTIONS:-NOT USED.

MEMORY TYPE 1:-BITS<2:4>:=BITS <12:14> OF STAT1 OF DEV:0.

MAXIMUM ADDRESS:-BITS<17:19>:=BITS<12:14> OF STAT1 OF DEV:1

BITS<2:4>:=BITS <12:14> OF STAT1 OF DEV:2

BITS<10:12>:=BITS<12:14> OF STAT1 OF DEV:3

IN THE SAME MANNER

MEMORY TYPE 2 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE

4,5,6,7.

MEMORY TYPE 3 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE

8,9,10,11.

MEMORY TYPE 4 MAXIMUM ADDRESS:-GETS STAT1<12:14> OF DEVICE

12,13,14,15.

INTERRUPT VECTOR 1:FIRST DEVICE RECEIVE VECTOR.

REST OF THE DEVICE(KMC'S) VECTOR SHOULD BE SET UP SEQUENTIALLY  
IN INCREMENTS OF 10.

BUS PRIORITY:KMC'S PRIORITY(SHOULD BE SAME FOR ALL KMC'S UNDER  
TEST).

INTERRUPT VECTOR 2:NOT USED.

BUS PRIORITY:NOT USED.

BASE ADDRESS:FIRST DEVICE CSR ADDRESS.

REST SHOULD FOLLOW SEQUENTIALLY

IN INCREMENTS OF 10.

DEVICE MAP:AS DESCRIBED IN APT MANUAL.

CONTROLLER SPECIFIC CODE 1:-NO. OF DEVICES UNDER TEST.

CONTROLLER SPECIFIC CODE 2:-NOT USED.

DEVICE DESCRIPTOR WORD 0:STAT2 OF FIRST DEVICE.

. .

. .

TO

. .

. .

DEVICE DESCRIPTOR WORD 15:STAT2 OF 16TH DEVICE.(KMC)

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DOCUMENT  
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MAINDEC-11-DZKCC-A  
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- 2225 \*\*\*\*\* TEST 1 \*\*\*\*\*  
VERIFY THAT REFERENCING UNIBUS DEVICE REGISTERS  
DOES NOT CAUSE A TIME OUT TRAP
- 2256 \*\*\*\*\* TEST 2 \*\*\*\*\*  
VERIFY THAT RUN CAN BE CLEARED
- 2275 \*\*\*\*\* TEST 3 \*\*\*\*\*  
UNIBUS REGISTER WORD DUAL ADDRESSING TEST  
LOAD ALL REGISTERS WITH INCREMENTING PATTERN  
READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING
- 2318 \*\*\*\*\* TEST \*\*\*\*\*  
CONTROL STATUS REGISTER WRITE/RE... TEST  
SET BIT0, VERIFY BIT0 WAS SET  
CLEAR BIT0, VERIFY BIT0 WAS CLEARED
- 2350 \*\*\*\*\* TEST 5 \*\*\*\*\*  
CONTROL STATUS REGISTER WRITE/READ TEST  
SET BIT1, VERIFY BIT1 WAS SET  
CLEAR BIT1, VERIFY BIT1 WAS CLEARED
- 2382 \*\*\*\*\* TEST 6 \*\*\*\*\*
- 2383 CONTROL STATUS REGISTER WRITE/READ TEST  
SET BIT2, VERIFY BIT2 WAS SET  
CLEAR BIT2, VERIFY BIT2 WAS CLEARED
- 2414 \*\*\*\*\* TEST 7 \*\*\*\*\*  
CONTROL STATUS REGISTER WRITE/READ TEST  
SET BITS, VERIFY BITS WAS SET  
CLEAR BITS, VERIFY BITS WAS CLEARED
- 2446 \*\*\*\*\* TEST 10 \*\*\*\*\*  
CONTROL STATUS REGISTER WRITE/READ TEST  
SET BIT6, VERIFY BIT6 WAS SET  
CLEAR BIT6, VERIFY BIT6 WAS CLEARED

2478 \*\*\*\*\* TEST 11 \*\*\*\*\*  
CONTROL STATUS REGISTER WRITE/READ TEST  
SET BIT7, VERIFY BIT7 WAS SET  
CLEAR BIT7, VERIFY BIT7 WAS CLEARED

2510 \*\*\*\*\* TEST 12 \*\*\*\*\*  
CONTROL STATUS REGISTER WRITE/READ TEST  
SET BIT9, VERIFY BIT9 WAS SET  
CLEAR BIT9, VERIFY BIT9 WAS CLEARED

2542 \*\*\*\*\* TEST 13 \*\*\*\*\*  
CONTROL STATUS REGISTER WRITE/READ TEST  
SET BIT11, VERIFY BIT11 WAS SET  
CLEAR BIT11, VERIFY BIT11 WAS CLEARED

2574 \*\*\*\*\* TEST 14 \*\*\*\*\*  
CONTROL STATUS REGISTER WRITE/READ TEST  
SET BIT12, VERIFY BIT12 WAS SET  
CLEAR BIT12, VERIFY BIT12 WAS CLEARED

2606 \*\*\*\*\* TEST 15 \*\*\*\*\*

2607 CONTROL OUT REGISTER WRITE/READ TEST  
SET BIT0, VERIFY BIT0 WAS SET  
CLEAR BIT0, VERIFY BIT0 WAS CLEARED

2638 \*\*\*\*\* TEST 16 \*\*\*\*\*  
CONTROL OUT REGISTER WRITE/READ TEST  
SET BIT1, VERIFY BIT1 WAS SET  
CLEAR BIT1, VERIFY BIT1 WAS CLEARED

2670 \*\*\*\*\* TEST 17 \*\*\*\*\*  
CONTROL OUT REGISTER WRITE/READ TEST  
SET BIT2, VERIFY BIT2 WAS SET  
CLEAR BIT2, VERIFY BIT2 WAS CLEARED

2702 \*\*\*\*\* TEST 20 \*\*\*\*\*  
CONTROL OUT REGISTER WRITE/READ TEST  
SET BIT6, VERIFY BIT6 WAS SET  
CLEAR BIT6, VERIFY BIT6 WAS CLEARED

2734 \*\*\*\*\* TEST 21 \*\*\*\*\*  
CONTROL OUT REGISTER WRITE/READ TEST  
SET BIT7, VERIFY BIT7 WAS SET  
CLEAR BIT7, VERIFY BIT7 WAS CLEARED

2766 \*\*\*\*\* TEST 22 \*\*\*\*\*  
CONTROL OUT REGISTER WRITE/READ TEST  
SET BIT12, VERIFY BIT12 WAS SET  
CLEAR BIT12, VERIFY BIT12 WAS CLEARED

2798 \*\*\*\*\* TEST 23 \*\*\*\*\*  
CONTROL OUT REGISTER WRITE/READ TEST  
SET BIT13, VERIFY BIT13 WAS SET  
CLEAR BIT13, VERIFY BIT13 WAS CLEARED

2830 \*\*\*\*\* TEST 24 \*\*\*\*\*

2831 PORT4 REGISTER WRITE/READ TEST  
FLOAT A ONE THROUGH PORT4 REGISTER  
FLOAT A ZERO THROUGH PORT4 REGISTER

2874 \*\*\*\*\* TEST 25 \*\*\*\*\*  
PORT6 REGISTER WRITE/READ TEST  
FLOAT A ONE THROUGH PORT6 REGISTER  
FLOAT A ZERO THROUGH PORT6 REGISTER

2918 \*\*\*\*\* TEST 26 \*\*\*\*\*  
UNIBUS REGISTER BYTE DATA ADDRESSING TEST  
LOAD ALL REGISTERS WITH INCREASING PATTERN  
READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING

2961 \*\*\*\*\* TEST 27 \*\*\*\*\*  
MAINTENANCE INSTRUCTION REGISTER TEST  
VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'  
AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A BUS RESET.

3003 \*\*\*\*\* TEST 30 \*\*\*\*\*  
MAINTENANCE INSTRUCTION REGISTER TEST  
VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'  
AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A MASTER RESET.

3045 \*\*\*\*\* TEST 31 \*\*\*\*\*  
MICRO PROCESSOR TEST  
LOAD 10P06 WITH A MICRO-PROCESSOR INSTRUCTION, CLOCK IT  
VERIFY INSTRUCTION EXECUTED PROPERLY  
INSTRUCTION SHOULD MOVE IBUS#4 TO IBUS#5, IBUS#4 IS ALL 1'S  
AND IBUS#5 IS ALL 0'S. RESULT SHOULD BE ALL 1'S IN SEL4

3074 \*\*\*\*\* TEST 32 \*\*\*\*\*  
MICRO PROCESSOR IBUS# REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS# REGISTER 0  
FLOAT A 0 THROUGH IBUS# REGISTER 0

3131 \*\*\*\*\* TEST 33 \*\*\*\*\*  
MICRO PROCESSOR IBUS# REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS# REGISTER 2  
FLOAT A 0 THROUGH IBUS# REGISTER 2

3188 \*\*\*\*\* TEST 34 \*\*\*\*\*  
MICRO PROCESSOR IBUS# REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS# REGISTER 4  
FLOAT A 0 THROUGH IBUS# REGISTER 4

- 3241 \*\*\*\*\* TEST 35 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 5  
FLOAT A 0 THROUGH IBUS REGISTER 5
  
- 3294 \*\*\*\*\* TEST 36 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 10  
FLOAT A 0 THROUGH IBUS REGISTER 10
  
- 3351 \*\*\*\*\* TEST 37 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 11  
FLOAT A 0 THROUGH IBUS REGISTER 11
  
- 3410 \*\*\*\*\* TEST 40 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 0  
FLOAT A 0 THROUGH IBUS REGISTER 0
  
- 3463 \*\*\*\*\* TEST 41 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 1  
FLOAT A 0 THROUGH IBUS REGISTER 1
  
- 3516 \*\*\*\*\* TEST 42 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 2  
FLOAT A 0 THROUGH IBUS REGISTER 2
  
- 3569 \*\*\*\*\* TEST 43 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 3  
FLOAT A 0 THROUGH IBUS REGISTER 3
  
- 3622 \*\*\*\*\* TEST 44 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 4  
FLOAT A 0 THROUGH IBUS REGISTER 4
  
- 3675 \*\*\*\*\* TEST 45 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 5  
FLOAT A 0 THROUGH IBUS REGISTER 5
  
- 3728 \*\*\*\*\* TEST 46 \*\*\*\*\*  
MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
FLOAT A 1 THROUGH IBUS REGISTER 6  
FLOAT A 0 THROUGH IBUS REGISTER 6

3781 \*\*\*\*\* TEST 47 \*\*\*\*\*  
 MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST

3783 FLOAT A 1 THROUGH IBUS REGISTER 7  
 FLOAT A 0 THROUGH IBUS REGISTER 7

3834 \*\*\*\*\* TEST 50 \*\*\*\*\*  
 MICRO PROCESSOR IBUS DUAL ADDRESS TEST  
 WRITE ALL IBUS REGISTERS WITH INCREMENTING PATTERN  
 READ ALL IBUS REGISTERS TO VERIFY CORRECT ADDRESSING

3897 \*\*\*\*\* TEST 51 \*\*\*\*\*  
 MICRO PROCESSOR BR REGISTER TEST  
 FLOAT A 1 THROUGH THE BR  
 FLOAT A 0 THROUGH THE BR

3949 \*\*\*\*\* TEST 52 \*\*\*\*\*  
 SCRATCH PAD TEST

3951 FLOAT A 1 THROUGH EACH SCRATCH PAD LOCATION  
 FLOAT A 0 THROUGH EACH SCRATCH PAD LOCATION

4016 \*\*\*\*\* TEST 53 \*\*\*\*\*  
 SCRATCH PAD DUAL ADDRESSING TEST  
 WRITE AN INCREMENTING PATTERN IN ALL SP LOCATIONS  
 READ ALL SP LOCATIONS TO VERIFY CORRECT ADDRESSING

4077 \*\*\*\*\* TEST 54 \*\*\*\*\*  
 INTERRUPT TEST  
 TEST THAT DEVICE CAN INTERRUPT TO VECTOR A

4108 \*\*\*\*\* TEST 55 \*\*\*\*\*  
 INTERRUPT TEST  
 TEST THAT DEVICE CAN INTERRUPT TO VECTOR B

4138 \*\*\*\*\* TEST 56 \*\*\*\*\*  
 PRIORITY INTERRUPT TESTS  
 SET PS TO ALL BR LEVELS EQUAL OR GREATER THAN  
 THE KMC11 LEVEL, VERIFY THAT KMC11 DOES NOT INTERRUPT

4178 \*\*\*\*\* TEST 57 \*\*\*\*\*  
 PRIORITY INTERRUPT TESTS  
 SET PS TO ALL BR LEVELS LESS THAN THE KMC11 LEVEL  
 VERIFY THAT THE KMC11 WILL INTERRUPT

4224 \*\*\*\*\* TEST 60 \*\*\*\*\*  
 NPR TEST  
 TEST OF DAT0, 1 WORD FROM UPROC TO 11 MEMORY

- 4259 \*\*\*\*\* TEST 61 \*\*\*\*\*  
 NPR TEST  
 TEST OF DAT1, 1 WORD FROM 11 MEMORY TO UPROC
- 4297 \*\*\*\*\* TEST 62 \*\*\*\*\*  
 NPR TEST  
 TEST OF DAT0B, 1 BYTE FROM UPROC TO 11 MEMORY
- 4331 \*\*\*\*\* TEST 63 \*\*\*\*\*  
 TEST OF EA BITS 16 AND 17  
 DO A DAT0 TO AN ADDRESS USING OUT BA BITS 16 AND 17  
 VERIFY CORRECT RESULTS
- 4372 \*\*\*\*\* TEST 64 \*\*\*\*\*  
 TEST OF EA BITS 16 AND 17  
 DO A DAT1 USING IN BA BITS 16 AND 17  
 VERIFY CORRECT RESULTS
- 4410 \*\*\*\*\* TEST 65 \*\*\*\*\*  
 NPR NON-EXISTENT MEMORY TEST  
 DO A DAT0 TO A NON-EXISTENT ADDRESS  
 VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
- 4447 \*\*\*\*\* TEST 66 \*\*\*\*\*  
 NPR NON-EXISTENT MEMORY TEST  
 DO A DAT1 FROM A NON-EXISTENT ADDRESS  
 VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
- 4484 \*\*\*\*\* TEST 67 \*\*\*\*\*  
 NPR TEST  
 USING DAT0, NPR A BINARY COUNT (0-377 )  
 FROM MICRO-PROCESSOR TO ALL AVAILABLE MEMORY
- 4546 \*\*\*\*\* TEST 70 \*\*\*\*\*  
 ALU C BIT TEST  
 TEST THAT AN ADD OF 377 AND 377 WILL SET THE C BIT
- 4586 \*\*\*\*\* TEST 71 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION SEL B WITH C BIT CLEARED  
 ALU FUNCTION (B) CODE=11  
 LOAD MAIN MEM AND SP WITH B WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS
- 4637 \*\*\*\*\* TEST 72 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION SEL A WITH C BIT CLEARED  
 ALU FUNCTION (A) CODE=10  
 LOAD MAIN MEM AND SP WITH B WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS

```

4688 ***** TEST 73 *****
ALU TEST
TEST OF ALU FUNCTION A OR NOTB WITH C BIT CLEARED
ALU FUNCTION (A OR NOTB) CODE=12
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4739 ***** TEST 74 *****
ALU TEST
TEST OF ALU FUNCTION A AND B WITH C BIT CLEARED
ALU FUNCTION (A AND B) CODE=13
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4790 ***** TEST 75 *****
4791 ALU TEST
TEST OF ALU FUNCTION A OR B WITH C BIT CLEARED
ALU FUNCTION (A OR B) CODE=14
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4841 ***** TEST 76 *****
ALU TEST
TEST OF ALU FUNCTION A XOR B WITH C BIT CLEARED
ALU FUNCTION (A XOR B) CODE=15
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4892 ***** TEST 77 *****
ALU TEST
TEST OF ALU FUNCTION ADD WITH C BIT CLEARED
ALU FUNCTION (A PLUS B) CODE=00
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4943 ***** TEST 100 *****
ALU TEST
TEST OF ALU FUNCTION 2A W/C WITH C BIT CLEARED
ALU FUNCTION (A PLUS A PLUS C) CODE=6
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

4994 ***** TEST 101 *****
ALU TEST
TEST OF ALU FUNCTION SUB WITH C BIT CLEARED
ALU FUNCTION (A-B) CODE=16
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

```

5045 \*\*\*\*\* TEST 102 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION ADD W/C WITH C BIT CLEARED  
 ALU FUNCTION (A PLUS B PLUS C) CODE=01  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS

5096 \*\*\*\*\* TEST 103 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION SUB W/C WITH C BIT CLEARED  
 ALU FUNCTION (A-B-C) CODE=2  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS

5147 \*\*\*\*\* TEST 104 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION INC A WITH C BIT CLEARED  
 ALU FUNCTION (A PLUS 1) CODE=3  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS

5198 \*\*\*\*\* TEST 105 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION 2A WITH C BIT CLEARED  
 ALU FUNCTION (A PLUS A) CODE=5  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS

5249 \*\*\*\*\* TEST 106 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION A PLUS C WITH C BIT CLEARED  
 ALU FUNCTION (A PLUS C) CODE=4  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS

5300 \*\*\*\*\* TEST 107 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION SUB WITH C BIT CLEARED  
 ALU FUNCTION (A-B) CODE=1  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS

5351 \*\*\*\*\* TEST 110 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION A WITH C BIT CLEARED  
 ALU FUNCTION (A) CODE=7  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS



5402 \*\*\*\*\* TEST 111 \*\*\*\*\*  
ALU TEST  
TEST OF ALU FUNCTION SEL B WITH C BIT SET  
ALU FUNCTION (B) CODE=11  
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA

5407 PERFORM THE FUNCTION, VERIFY THE RESULTS

5453 \*\*\*\*\* TEST 112 \*\*\*\*\*  
ALU TEST  
TEST OF ALU FUNCTION SEL A WITH C BIT SET  
ALU FUNCTION (A) CODE=10  
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
PERFORM THE FUNCTION, VERIFY THE RESULTS

5504 \*\*\*\*\* TEST 113 \*\*\*\*\*  
ALU TEST  
TEST OF ALU FUNCTION A OR NOTB WITH C BIT SET  
ALU FUNCTION (A OR NOTB) CODE=12  
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
PERFORM THE FUNCTION, VERIFY THE RESULTS

5555 \*\*\*\*\* TEST 114 \*\*\*\*\*  
ALU TEST  
TEST OF ALU FUNCTION A AND B WITH C BIT SET  
ALU FUNCTION (A AND B) CODE=13  
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
PERFORM THE FUNCTION, VERIFY THE RESULTS

5606 \*\*\*\*\* TEST 115 \*\*\*\*\*  
ALU TEST  
TEST OF ALU FUNCTION A OR B WITH C BIT SET  
ALU FUNCTION (A OR B) CODE=14  
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
PERFORM THE FUNCTION, VERIFY THE RESULTS

5657 \*\*\*\*\* TEST 116 \*\*\*\*\*  
ALU TEST  
TEST OF ALU FUNCTION A XOR B WITH C BIT SET  
ALU FUNCTION (A XOR B) CODE=15  
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
PERFORM THE FUNCTION, VERIFY THE RESULTS

5708 \*\*\*\*\* TEST 117 \*\*\*\*\*  
ALU TEST  
TEST OF ALU FUNCTION ADD WITH C BIT SET  
ALU FUNCTION (A PLUS B) CODE=00  
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
PERFORM THE FUNCTION, VERIFY THE RESULTS

```

5759 ***** TEST 120 *****
ALU TEST
TEST OF ALU FUNCTION 2A W/C WITH C BIT SET
ALU FUNCTION (A PLUS A PLUS C) CODE=5
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5810 ***** TEST 121 *****
ALU TEST
TEST OF ALU FUNCTION SUB WITH C BIT SET
ALU FUNCTION (A-B) CODE=16
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5961 ***** TEST 122 *****
ALU TEST
TEST OF ALU FUNCTION ADD W/C WITH C BIT SET
ALU FUNCTION (A PLUS B PLUS C) CODE=01
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5912 ***** TEST 123 *****
ALU TEST
TEST OF ALU FUNCTION SUB W/C WITH C BIT SET
ALU FUNCTION (A-B-C) CODE=2
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

5963 ***** TEST 124 *****
ALU TEST
TEST OF ALU FUNCTION INC A WITH C BIT SET
ALU FUNCTION (A PLUS 1) CODE=3

5967 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

6014 ***** TEST 125 *****
ALU TEST
TEST OF ALU FUNCTION 2A WITH C BIT SET
ALU FUNCTION (A PLUS A) CODE=5
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

6065 ***** TEST 126 *****
ALU TEST
TEST OF ALU FUNCTION A PLUS C WITH C BIT SET
ALU FUNCTION (A PLUS C) CODE=4
LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
PERFORM THE FUNCTION, VERIFY THE RESULTS

```

- 6116 \*\*\*\*\* TEST 127 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT SET  
 ALU FUNCTION (A-B-1) CODE=17  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS
  
- 6167 \*\*\*\*\* TEST 130 \*\*\*\*\*  
 ALU TEST  
 TEST OF ALU FUNCTION DEC A WITH C BIT SET  
 ALU FUNCTION (A-1) CODE=7  
 LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
 PERFORM THE FUNCTION, VERIFY THE RESULTS
  
- 6218 \*\*\*\*\* TEST 131 \*\*\*\*\*  
 TEST OF PROGRAM CLOCK BIT  
 DO A MASTER CLEAR, VERIFY THAT PROGRAM CLOCK IS SET  
 WRITE PROGRAM CLOCK BIT TO A ONE, VERIFY THAT IT CLEARS,  
 AND THEN SETS SOME TIME LATER
  
- 6269 \*\*\*\*\* TEST 132 \*\*\*\*\*  
 FORCE POWER FAIL TEST  
 SET FORCE POWER FAIL BIT VERIFY THAT PROCESSOR TRAPS TO 24  
 GOING DOWN AND COMING UP, VERIFY ALSO THAT BUS INIT WAS  
 BLOCKED FROM GETTING TO THE I/OC DURING THE POWER FAIL
  
- 6317 \*\*\*\*\* TEST 133 \*\*\*\*\*  
 MICRO-PROCESSOR NOISE TEST  
 WRITE ALL ZERO'S THEN ALL ONE'S THEN A DATA PATTERN  
 TO THE I/OB\* AND I/OB REGISTERS AND TO THE SP AND MAIN MEM  
 THEN GO BACK AND READ THE DATA PATTERNS TO VERIFY THAT  
 READING AND WRITING OF OTHER LOCATIONS AND REGISTERS  
 DID NOT CHANGE THE DATA.

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```
.TITLE MAINDEC-11-DZKCC-A
*COPYRIGHT (C) 1976
*DIGITAL EQUIPMENT CORP.
*RAYNARD, MASS. 01754
*
*PROGRAM BY DINESH GORADIA
*
*THIS PROGRAM WAS ASSEMBLED USING THE POP-11 MAINDEC SYSMAC
*PACKAGE (MAINDEC-11-DZGAC-C3), JAN 19, 1977.
*
```

```
MAINDEC-11-DZKCC-A BASIC KNC11 CONTROLLER TEST
COPYRIGHT 1976, DIGITAL EQUIPMENT CORP., RAYNARD, MASS. 01754
```

```
STARTING PROCEDURE
LOAD PROGRAM
LOAD ADDRESS 000200
SAB=0 AUTOSIZE KNC11
SAD=1 USE CURRENT KNC11 PARAMETERS
SAO=1 INPUT NEW KNC11 PARAMETERS
PRESS START
PROGRAM WILL TYPE "MAINDEC-11-DZKCC-A BASIC KNC11 CONTROLLER TEST"
PROGRAM WILL TYPE STATUS MAP
PROGRAM WILL TYPE "P" TO INDICATE THAT TESTING HAS STARTED
AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
AND THEN RESUME TESTING
SUBSEQUENT RESTARTS WILL NOT TYPE PROGRAM TITLE
```

.SBTTL BASIC DEFINITIONS

```
001200 :#INITIAL ADDRESS OF THE STACK POINTER ### 1200 ###
STACK= 1200
.EQUIV ENT,ERROR ;;BASIC DEFINITION OF ERROR CALL
.EQUIV TOT,SCOPE ;;BASIC DEFINITION OF SCOPE CALL
```

:#MISCELLANEOUS DEFINITIONS

```
000011 HT= 11 ;;CODE FOR HORIZONTAL TAB
000012 LF= 12 ;;CODE FOR LINE FEED
000015 CR= 15 ;;CODE FOR CARRIAGE RETURN
000200 CRLF= 200 ;;CODE FOR CARRIAGE RETURN-LINE FEED
177776 PS= 177776 ;;PROCESSOR STATUS WORD
.EQUIV PS,PSM
177774 $TKLMT= 177774 ;;STACK LIMIT REGISTER
177772 PIR0= 177772 ;;PROGRAM INTERRUPT REQUEST REGISTER
177570 DSUR= 177570 ;;HARDWARE SWITCH REGISTER
177570 DOISP= 177570 ;;HARDWARE DISPLAY REGISTER
```

:#GENERAL PURPOSE REGISTER DEFINITIONS

```
000000 R0= %0 ;;GENERAL REGISTER
000001 R1= %1 ;;GENERAL REGISTER
000002 R2= %2 ;;GENERAL REGISTER
```



113 000100  
114 000040  
115 000020  
116 000010  
117 000004  
118 000002  
119 000001  
120  
121  
122  
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126  
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129  
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131  
132 000004  
133 000010  
134 000014  
135 000014  
136 000014  
137 000020  
138 000024  
139 000030  
140 000034  
141 000060  
142 000064  
143 000240  
144  
145  
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151 005746  
152 005726  
153 010046  
154 012600  
155 024646  
156 022626  
157  
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160

BIT06= 100  
BIT05= 40  
BIT04= 20  
BIT03= 10  
BIT02= 4  
BIT01= 2  
BIT0= 1  
EQUIV BIT09, BIT9  
EQUIV BIT08, BIT8  
EQUIV BIT07, BIT7  
EQUIV BIT06, BIT6  
EQUIV BIT05, BIT5  
EQUIV BIT04, BIT4  
EQUIV BIT03, BIT3  
EQUIV BIT02, BIT2  
EQUIV BIT01, BIT1  
EQUIV BIT00, BIT0

: BASIC "CPU" TRAP VECTOR ADDRESSES  
ERRVEC= 4 : TIME OUT AND OTHER ERRORS  
RESVEC= 10 : RESERVED AND ILLEGAL INSTRUCTIONS  
TRITVEC= 14 : TRAP INSTRUCTION  
BPTVEC= 14 : BREAKPOINT TRAP (BPT)  
IOTVEC= 20 : INPUT/OUTPUT TRAP (IOT) #SCOPE##  
PWRVEC= 24 : POWER FAIL  
ENTVEC= 30 : EMULATOR TRAP (ENT) #ERROR##  
TRAPVEC= 34 : TRAP TRAP  
TKVEC= 60 : TTY KEYBOARD VECTOR  
TPVEC= 64 : TTY PRINTER VECTOR  
PIROVEC= 240 : PROGRAM INTERRUPT REQUEST VECTOR

: INSTRUCTION DEFINITIONS

PUSHSP=5746 : DECREMENT PROCESSOR STACK 1 WORD  
POPSP=5726 : INCREMENT PROCESSOR STACK 1 WORD  
PUSHRD=10046 : SAVE RD ON STACK  
POPRD=12600 : RESTORE RD FROM STACK  
PUSHCS=24646 : DECREMENT STACK TWICE  
POP2SP=22626 : INCREMENT STACK TWICE  
.EQUIV ENT,HLT : BASIC DEFINITION OF ERROR CALL

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(2)  
(2)  
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207

000000 000000 000000

000020 004134  
000022 000340  
000024 007126  
000026 000340  
000030 006512  
000032 000340  
000034 006414  
000036 000340

000040 000046  
000046 004070  
000052 000052  
000052 000000  
000040 000040

000174 000000  
000176 000000

000200 000137 002402

001000 005200 040515 047111  
(2) 001025 102 051501 041511

177570  
177570

\*\*\*\*\*  
-----  
: TRAPCATCHER FOR ILLEGAL INTERRUPTS  
: THE STANDARD "TRAP" CATCHER IS PLACED  
: BETWEEN ADDRESS 0 TO ADDRESS 776.  
: IT LOOKS LIKE "PC+2 HALT".  
-----  
\*\*\*\*\*

.=0  
WORD 0,0  
: STANDARD INTERRUPT VECTORS  
-----

.=20  
: SCOPE LOOP HANDLER.  
: SERVICE AT LEVEL 7.  
: POWER FAIL HANDLER  
: SERVICE AT LEVEL 7  
: ERROR HANDLER  
: SERVICE AT LEVEL 7  
: GENERAL HANDLER DISPATCH SERVICE  
: SERVICE AT LEVEL 7  
.SBTTL ACT11 HOOKS

\*\*\*\*\*  
: HOOKS REQUIRED BY ACT11  
: \$SVPC= ;SAVE PC  
: .=46 ;:1)SET LOC.46 TO ADDRESS OF SENDAD IN .SEOP  
: SENDAD  
: .=52 ;:2)SET LOC.52 TO ZERO  
: .WORD 0 ;: RESTORE PC  
: .=\$SVPC

.=174  
DISPREG: 0 ; SOFTWARE DISPLAY REGISTER  
SWREG: 0 ; SOFTWARE SWITCH REGISTER

.=200  
JMP .START ; GO TO START OF PROGRAM

.=1000  
MTITLE: .ASCII (200)<12>/MAINDEC-11-DZKCC-A/(200)  
.ASCII /BASIC KMC11 CONTROLLER TEST/(200)

DSWR = 177570  
DDISP = 177570





264  
265  
266  
267 001316  
268 001316 000000  
269 001320 000000  
270 001322 000000  
271 001324 000000  
272 001326 000000  
273 001330 000000  
274 001332 000000  
275 001334 000000  
276 001336  
277 001336 002  
278 001337 000  
279 001340 000000  
280 001342 000000  
281 001344 000000  
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288 001346 000  
289 001347 000  
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294 001350 000000  
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296 001352 000  
297 001353 000  
298 001354 000000  
299 001356 000  
300 001357 000  
301 001360 000000  
302 001362 000  
303 001363 000  
304 001364 000000  
305 001366 000000  
306 001370 000000  
307 001372 000000  
308 001374 000000  
309 001376 000000  
310 001400 000000  
311 001402 000000  
312 001404 000000  
313 001406 000000  
314 001410 000000  
315 001412 000000  
316 001414 000000  
317 001416 000000  
318 001420 000000  
319 001422 000000

```

*****
: EVEN
: APT MAILBOX
: MESSAGE TYPE CODE
: FATAL ERROR NUMBER
: TEST NUMBER
: PASS COUNT
: DEVICE COUNT
: I/O UNIT NUMBER
: MESSAGE ADDRESS
: MESSAGE LENGTH
: APT ENVIRONMENT TABLE
: ENVIRONMENT BYTE
: ENVIRONMENT MODE BITS
: APT SWITCH REGISTER
: USER SWITCHES
: CPU TYPE, OPTIONS
: BITS 15-11=CPU TYPE
: 11/01=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05
: 11/70=06, 100=07, 0=10
: BIT 10=REAL TIME CLOCK
: BIT 9=FLOATING POINT PROCESSOR
: BIT 8=MEMORY MANAGEMENT
: HIGH ADDRESS, H.S. BYTE
: MEM. TYPE, BLK#1
: MEM. TYPE BYTE — (HIGH BYTE)
: 900 MSEC CORE=001
: 700 MSEC BIPOLAR=002
: 500 MSEC NOS=003
: HIGH ADDRESS, BLK#1
: MEM. LAST ADDR. #3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE
: HIGH ADDRESS, H.S. BYTE
: MEM. TYPE, BLK#2
: MEM. LAST ADDRESS, BLK#2
: HIGH ADDRESS, H.S. BYTE
: MEM. TYPE, BLK#3
: MEM. LAST ADDRESS, BLK#3
: HIGH ADDRESS, H.S. BYTE
: MEM. TYPE, BLK#4
: MEM. LAST ADDRESS, BLK#4
: INTERRUPT VECTOR#1, BUS PRIORITY#1
: INTERRUPT VECTOR#2, BUS PRIORITY#2
: BASE ADDRESS OF EQUIPMENT UNDER TEST
: DEVICE #0
: CONTROLLER DESCRIPTION WORD#1
: CONTROLLER DESCRIPTION WORD#2
: DEVICE DESCRIPTOR WORD#0
: DEVICE DESCRIPTOR WORD#1
: DEVICE DESCRIPTOR WORD#2
: DEVICE DESCRIPTOR WORD#3
: DEVICE DESCRIPTOR WORD#4
: DEVICE DESCRIPTOR WORD#5
: DEVICE DESCRIPTOR WORD#6
: DEVICE DESCRIPTOR WORD#7
: DEVICE DESCRIPTOR WORD#8

```

360 001424 000000  
 361 001425 000000  
 362 001430 000000  
 363 001432 000000  
 364 001434 000000  
 365 001436 000000  
 366 001440 000000  
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 368 001442  
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ROOM9: .WORD ROOM9  
 ROOM10: .WORD ROOM10  
 ROOM11: .WORD ROOM11  
 ROOM12: .WORD ROOM12  
 ROOM13: .WORD ROOM13  
 ROOM14: .WORD ROOM14  
 ROOM15: .WORD ROOM15

SETEND:

PROGRAM CONTROL PARAMETERS

NEXT: .WORD 0 ; ADDRESS OF NEXT TEST TO BE EXECUTED  
 LOCK: .WORD 0 ; ADDRESS FOR LOCK CURRENT DATA

PROGRAM VARIABLES

STRTSM: .WORD 0 ; SWITCHES AT START OF PROGRAM  
 STAT: .WORD 0 ; KM STATUS WORD STORAGE  
 CLIX: .WORD 0  
 MASKX: .WORD 0  
 SAVSP: .WORD 0 ; STACK POINTER STORAGE  
 SAVPC: .WORD 0 ; PROGRAM COUNTER STORAGE  
 ZERO: .WORD 0  
 ONE: .WORD 1  
 NEM IN: .WORD 0 ; HIGHEST LOCATION FOR NPR'S  
 KRACTV: .BLKM 1 ; KNC11 SELECTED ACTIVE  
 KMINUM: .BLKM 1 ; OCTAL NUMBER OF KNC11'S  
 SAVACT: .BLKM 1 ; ORIGINAL ACTIVE DEVICES.  
 SAVNUM: .BLKM 1 ; WORKABLE NUMBER.  
 RUN: .WORD 0 ; POINTER TO RUNNING DEVICES  
 EVEN  
 CREAM: .WORD K11.MAP-6 ; TABLE POINTER  
 MILK: .WORD CNT.MAP-4 ; TABLE POINTER

PROGRAM CONTROL FLAGS

INIFLG: .BYTE 0 ; PROGRAM INITIALIZING FLAG  
 .EVEN  
 LOKFLG: .BYTE 0 ; LOCK ON CURRENT TEST FLAG  
 QV.FLG: .BYTE 0 ; QUICK VERIFY FLAG  
 ; ON FIRST PASS OF EACH KNC11 ITERATIONS WILL BE SUPPRES

.SBTTL ERROR POINTER TABLE

;\* THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.  
;\* THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN  
;\* LOCATION SITE#B. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.  
;\* NOTE1: IF SITE#B IS 0 THE ONLY PERTINENT DATA IS (SERRPC).  
;\* NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;\* EM ;; POINTS TO THE ERROR MESSAGE  
;\* DH ;; POINTS TO THE DATA HEADER  
;\* DT ;; POINTS TO THE DATA  
;\* DF ;; POINTS TO THE DATA FORMAT

SERRTB:  
:EVEN  
;\* DF ;; DOES NOT APPLY IN THIS DIAGNOSTIC.

365  
366  
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368  
369  
370  
371  
372  
373  
374  
375  
376  
377  
378  
379 001512  
380  
381  
382 001512 000000  
383 001514 000000  
384 001516 000000  
385 001520 035746  
386 001522 036632  
387 001524 037112  
388 001526 036013  
389 001530 036673  
390 001532 037124  
391 001534 036054  
392 001536 036731  
393 001540 037142  
394 001542 036102  
395 001544 036752  
396 001546 037194  
397 001550 036102  
398 001552 037014  
399 001554 037172  
400 001556 036143  
401 001560 036731  
402 001562 037210  
403 001564 036165  
404 001566 037055  
405 001570 037172  
406 001572 036207  
407 001574 000000  
408 001576 000000  
409 001600 036243  
410 001602 000000  
411 001604 000000  
412 001606 036307  
413 001610 036731  
414 001612 037142  
415 001614 036321  
416 001616 037055  
417 001620 037172  
418 001622 036343  
419 001624 037055  
420 001626 037172

DF  
0  
0  
EM1 ; ERROR 1  
DH1  
DT1  
EM2 ; ERROR 2  
DH2  
DT2  
EM3 ; ERROR 3  
DH3  
DT3  
EM4 ; ERROR 4  
DH4  
DT4  
EM5 ; ERROR 5  
DH5  
DT5  
EM6 ; ERROR 6  
DH6  
DT6  
EM7 ; ERROR 7  
DH7  
DT7  
EM10 ; ERROR 10  
DH10  
DT10  
EM11 ; ERROR 11  
DH11  
DT11  
EM12 ; ERROR 12  
DH12  
DT12  
EM13 ; ERROR 13  
DH13  
DT13  
EM14 ; ERROR 14  
DH14  
DT14

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001630 036355
001631 036731
001632 037210
001633 036731
001634 036731
001635 037154
001644 036413
001646 000000
001650 000000
001652 036443
001654 000000
001656 000000
001660 036307
001662 037055
001664 037172
001666 036471
001670 036731
001672 037222
001674 036524
001676 036731
001700 037142
001702 036471
001704 000000
001706 000000
001710 036573
001712 036731
001714 037142
002034
000024 000200
000044 002034
002034 000000
002036 001316
002040 000132
002042 000137
002044 000137
002046 000052
470
471

```

```

EM14
DH3 ; ERROR 15
DT6
EM15
DH4 ; ERROR 16
DT4
EM16
0 ; ERROR 17
0
EM17
0 ; ERROR 20
0
EM11
DH6 ; ERROR 21
DT5
EM20
DH3 ; ERROR 22
DT7
EM21
DH3 ; ERROR 23
DT3
EM20
0 ; ERROR 24
0
EM22
DH3 ; ERROR 25
DT3

```

```

.=2034
.SBTTL APT PARAMETER BLOCK

```

```

*****
SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
*****
.SX. : SAVE CURRENT LOCATION
.24 : SET POWER FAIL TO POINT TO START OF PROGRAM
200 : FOR APT START UP
.SX : POINT TO SET INDIRECT ADDRESS PTR.
.SX : POINT TO APT NUMBER BLOCK
.SX : RESET LOCATION COUNTER
*****
SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-POP11 DIAGNOSTIC
INTERFACE SPEC.

```

```

SAPTH0:
SHITS: .WORD 0 ; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
SMBOR: .WORD SMAIL ; ADDRESS OF APT MAILBOX (BITS 0-15)
STSTM: .WORD 90 ; RUN TIME OF LONGEST TEST
SPASTM: .WORD 95 ; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
SUNITH: .WORD 95 ; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
.SX : SETEND-SMAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)

```

```

472
473 ;KMC11 CONTROL INDICATORS FOR CURRENT KMC11 UNDER TEST
474 -----
475
476 002050 000000 STAT1: 0
477 002052 000000 STAT2: 0
478 002054 000000 STAT3: 0
479
480 ;KMC11 VECTOR AND REGISTER INDIRECT POINTERS
481 -----
482
483 002056 000000 KMRVEC: 0 ; POINTER TO KMC11 RECEIVER INTERRUPT VECTOR
484 002060 000000 KMRVL: 0 ; POINTER TO KMC11 RECEIVER INTERRUPT SERVICE PS
485 002062 000000 KMTVEC: 0 ; POINTER TO KMC11 TRANSMITTER INTERRUPT VECTOR
486 002064 000000 KMTVL: 0 ; POINTER TO KMC11 TRANSMITTER INTERRUPT SERVICE PS
487 002066 000000 KMCSSR: 0 ; POINTER TO KMC11 CONTROL STATUS REGISTER
488 002070 000000 KMCSSRH: 0 ; POINTER TO KMC11 CONTROL STATUS REGISTER HIGH BYTE.
489 002072 000000 KMCCTL: 0 ; POINTER TO KMC11 CONTROL OUT REGISTER
490 002074 000000 KMP04: 0 ; POINTER TO KMC11 PORT REGISTER(SEL 4)
491 002076 000000 KMP06: 0 ; POINTER TO KMC11 PORT REGISTER(SEL 6)
492
493 ;TEMP STORAGE
494 -----
495
496 ;TEMP: 0
497 ;.=. +40
498
499 ;KMC11 STATUS TABLE AND ADDRESS ASSIGNMENTS
500 -----
501
502 . =2100
503 002100 002100 KM.MAP:
504 002100 000001 KMC00: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 00
505 002102 000001 KMS100: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 00
506 002104 000001 KMS200: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 00
507 002106 000001 KMS300: .BLKW 1 ; 3RD STATUS WORD
508
509 002110 000001 KMC01: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 01
510 002112 000001 KMS101: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 01
511 002114 000001 KMS201: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 01
512 002116 000001 KMS301: .BLKW 1 ; 3RD STATUS WORD
513
514 002120 000001 KMC02: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 02
515 002122 000001 KMS102: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 02
516 002124 000001 KMS202: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 02
517 002126 000001 KMS302: .BLKW 1 ; 3RD STATUS WORD
518
519 002130 000001 KMC03: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 03
520 002132 000001 KMS103: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 03
521 002134 000001 KMS203: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 03
522 002136 000001 KMS303: .BLKW 1 ; 3RD STATUS WORD
523
524 002140 000001 KMC04: .BLKW 1 ; CONTROL STATUS REGISTER FOR KMC11 NUMBER 04
525 002142 000001 KMS104: .BLKW 1 ; VECTOR FOR KMC11 NUMBER 04
526 002144 000001 KMS204: .BLKW 1 ; DDCMP LINE# FOR KMC11 NUMBER 04
527 002146 000001 KMS304: .BLKW 1 ; 3RD STATUS WORD
    
```

569	002150	00001	KMCR05: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 05
570	002152	00001	KMS105: .BLKW	1	: VECTOR FOR KMC11 NUMBER 05
571	002154	00001	KMS205: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 05
572	002156	00001	KMS305: .BLKW	1	: 3RD STATUS WORD
573	002160	00001	KMCR06: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 06
574	002162	00001	KMS106: .BLKW	1	: VECTOR FOR KMC11 NUMBER 06
575	002164	00001	KMS206: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 06
576	002166	00001	KMS306: .BLKW	1	: 3RD STATUS WORD
577	002170	00001	KMCR07: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 07
578	002172	00001	KMS107: .BLKW	1	: VECTOR FOR KMC11 NUMBER 07
579	002174	00001	KMS207: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 07
580	002176	00001	KMS307: .BLKW	1	: 3RD STATUS WORD
581	002200	00001	KMCR10: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 10
582	002202	00001	KMS110: .BLKW	1	: VECTOR FOR KMC11 NUMBER 10
583	002204	00001	KMS210: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 10
584	002206	00001	KMS310: .BLKW	1	: 3RD STATUS WORD
585	002210	00001	KMCR11: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 11
586	002212	00001	KMS111: .BLKW	1	: VECTOR FOR KMC11 NUMBER 11
587	002214	00001	KMS211: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 11
588	002216	00001	KMS311: .BLKW	1	: 3RD STATUS WORD
589	002220	00001	KMCR12: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 12
590	002222	00001	KMS112: .BLKW	1	: VECTOR FOR KMC11 NUMBER 12
591	002224	00001	KMS212: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 12
592	002226	00001	KMS312: .BLKW	1	: 3RD STATUS WORD
593	002230	00001	KMCR13: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 13
594	002232	00001	KMS113: .BLKW	1	: VECTOR FOR KMC11 NUMBER 13
595	002234	00001	KMS213: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 13
596	002236	00001	KMS313: .BLKW	1	: 3RD STATUS WORD
597	002240	00001	KMCR14: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 14
598	002242	00001	KMS114: .BLKW	1	: VECTOR FOR KMC11 NUMBER 14
599	002244	00001	KMS214: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 14
600	002246	00001	KMS314: .BLKW	1	: 3RD STATUS WORD
601	002250	00001	KMCR15: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 15
602	002252	00001	KMS115: .BLKW	1	: VECTOR FOR KMC11 NUMBER 15
603	002254	00001	KMS215: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 15
604	002256	00001	KMS315: .BLKW	1	: 3RD STATUS WORD
605	002260	00001	KMCR16: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 16
606	002262	00001	KMS116: .BLKW	1	: VECTOR FOR KMC11 NUMBER 16
607	002264	00001	KMS216: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 16
608	002266	00001	KMS316: .BLKW	1	: 3RD STATUS WORD
609	002270	00001	KMCR17: .BLKW	1	: CONTROL STATUS REGISTER FOR KMC11 NUMBER 17
610	002272	00001	KMS117: .BLKW	1	: VECTOR FOR KMC11 NUMBER 17
611	002274	00001	KMS217: .BLKW	1	: DOOMP LINE# FOR KMC11 NUMBER 17
612	002276	00001	KMS317: .BLKW	1	: 3RD STATUS WORD

N03

DZKCC MACY11 27(1006) 12-MAY-77 18:34 PAGE 13  
DZKCC.P11 21-MAR-77 17:19 APT PARAMETER BLOCK  
584 002300 000000 KM.END: 0000F

PAGE: 0039

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002302 000000  
 002302 000000  
 002304 000000  
 002306 000000  
 002310 000000  
 002312 000000  
 002314 000000  
 002316 000000  
 002320 000000  
 002322 000000  
 002324 000000  
 002326 000000  
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 002354 000000  
 002356 000000  
 002360 000000  
 002362 000000  
 002364 000000  
 002366 000000  
 002370 000000  
 002372 000000  
 002374 000000  
 002376 000000  
 002400 000000

;KMC11 PASS COUNT AND ERROR COUNT TABLE

-----  
 CNT.MAP:  
 PACT00: 0 ;PASS COUNT FOR KMC11 NUMBER 00  
 ERCT00: 0 ;ERROR COUNT FOR KMC11 NUMBER 00  
 PACT01: 0 ;PASS COUNT FOR KMC11 NUMBER 01  
 ERCT01: 0 ;ERROR COUNT FOR KMC11 NUMBER 01  
 PACT02: 0 ;PASS COUNT FOR KMC11 NUMBER 02  
 ERCT02: 0 ;ERROR COUNT FOR KMC11 NUMBER 02  
 PACT03: 0 ;PASS COUNT FOR KMC11 NUMBER 03  
 ERCT03: 0 ;ERROR COUNT FOR KMC11 NUMBER 03  
 PACT04: 0 ;PASS COUNT FOR KMC11 NUMBER 04  
 ERCT04: 0 ;ERROR COUNT FOR KMC11 NUMBER 04  
 PACT05: 0 ;PASS COUNT FOR KMC11 NUMBER 05  
 ERCT05: 0 ;ERROR COUNT FOR KMC11 NUMBER 05  
 PACT06: 0 ;PASS COUNT FOR KMC11 NUMBER 06  
 ERCT06: 0 ;ERROR COUNT FOR KMC11 NUMBER 06  
 PACT07: 0 ;PASS COUNT FOR KMC11 NUMBER 07  
 ERCT07: 0 ;ERROR COUNT FOR KMC11 NUMBER 07  
 PACT10: 0 ;PASS COUNT FOR KMC11 NUMBER 10  
 ERCT10: 0 ;ERROR COUNT FOR KMC11 NUMBER 10  
 PACT11: 0 ;PASS COUNT FOR KMC11 NUMBER 11  
 ERCT11: 0 ;ERROR COUNT FOR KMC11 NUMBER 11  
 PACT12: 0 ;PASS COUNT FOR KMC11 NUMBER 12  
 ERCT12: 0 ;ERROR COUNT FOR KMC11 NUMBER 12  
 PACT13: 0 ;PASS COUNT FOR KMC11 NUMBER 13  
 ERCT13: 0 ;ERROR COUNT FOR KMC11 NUMBER 13  
 PACT14: 0 ;PASS COUNT FOR KMC11 NUMBER 14  
 ERCT14: 0 ;ERROR COUNT FOR KMC11 NUMBER 14  
 PACT15: 0 ;PASS COUNT FOR KMC11 NUMBER 15  
 ERCT15: 0 ;ERROR COUNT FOR KMC11 NUMBER 15  
 PACT16: 0 ;PASS COUNT FOR KMC11 NUMBER 16  
 ERCT16: 0 ;ERROR COUNT FOR KMC11 NUMBER 16  
 PACT17: 0 ;PASS COUNT FOR KMC11 NUMBER 17  
 ERCT17: 0 ;ERROR COUNT FOR KMC11 NUMBER 17



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FORMAT OF STATUS TABLE

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	CSR
I	C	O	N	T	R	O	L	I	R	E	G	I	S	T	E	R	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	*	I	*	I	*	I	*	I	*	I	*	I	*	I	*	I	STAT1
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	*	I	B	I	M	I	I	A	I	D	I	D	*	I	*	I	STAT2
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	*	STAT3

DEFINITION OF FORMAT

- CSR: CONTAINS KNC11 CSR ADDRESS
- STAT1: BITS 00-08 IS KNC11 VECTOR ADDRESS  
 BIT14=1 ??? TURNAROUND CONNECTOR IS ON  
 BIT14=0 NO TURNAROUND CONNECTOR  
 BIT13=0 LINE UNIT IS AN MBE01  
 BIT13=1 LINE UNIT IS AN MBE02  
 BIT12=1 NO LINE UNIT  
 BITS 09-11 IS KNC11 BR PRIORITY LEVEL
- STAT2: LOW BYTE IS SWITCH PAC#1 (DOCMP LINE NUMBER)  
 HIGH BYTE IS SWITCH PAC#2 (BNB73 BOOT ADD)
- STAT3: BIT0=1 DO FREE RUNNING TESTS ON KNC  
 (MUST BE SET TO A ONE MANUALLY (PROGRAMS G AND H ONLY))

```

6989
6990
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6999
7000 002402 012737 000340 177776 .START: MOV #340,PS ;LOCK OUT INTERRUPTS
7001 002410 012706 001200 MOV #STACK,SP ;SET UP STACK
7002 002414 012737 007126 000024 MOV #SP+100,2024 ;SET UP POWER FAIL VECTOR
7003 002422 013737 001472 001476 MOV R0 ;SAVE NUMBER OF DEVICES IN SYSTEM.
7004 002430 005037 011416 CLR SP ;CLEAR SOFT TIMEOUT FLAG
7005 002434 105037 001203 CLRB SE ;CLEAR ERROR FLAG
7006 002440 105037 001511 CLRB OV.FLG ;ZERO QUICK VERIFY FLAG
7007 002444 012737 002070 001502 MOV #N0N.MAP-10,CREAM ;GET MAP POINTER.
7008 002452 012737 002276 001504 MOV #C0N.MAP-4,MILK ;GET PASS COUNT MAP POINTER
7009 002460 012737 100000 001500 MOV #BIT15,RUN ;POINT POINTER TO FIRST DEVICE.
7010 002466 012700 002302 MOV #C0N.T.MAP,R0 ;PASS COUNT POINTER TO R0
7011 002472 005037 235: CLR (R0)+ ;CLEAR TABLE
7012 002474 002700 002402 CNP #C0N.T.MAP+100,R0 ;DONE YET?
7013 002500 001374 BNE 235 ;KEEP GOING
7014 002506 005037 001216 CLR #ERRPC ;CLEAR LAST ERROR POINTER
7015 002510 012737 000001 001202 MOV #1,STSTN ;SET UP FOR TEST 1
7016 002514 012737 002402 001206 MOV #.START,SLPADR ;SET UP FOR POWER FAIL BEFORE
7017 ;TESTING STARTS
7018 002522 132737 000001 001336 BITB #1,SENV ;IS IT RUNNING UNDER APT?
7019 002530 001404 BEQ 75 ;IF NOT CHECK FOR TYPE OF SWITCH REGISTER.
7020 002532 013737 001340 000176 MOV #SMREG,SMREG ;LOAD SOFTWARE SWITCH REG.
7021 002540 000423 BR 65+2 ;GO SET UP SOFTWARE SWITCH REG.
7022 002546 013737 000006 35: MOV #0,-(SP) ;SAVE CURRENT VECTORS
7023 002550 013737 000004 MOV #0,-(SP)
7024 002552 012737 002606 00LJ04 MOV #65,204 ;SET UP FOR TIMEOUT
7025 002560 012737 177570 001240 MOV #177570,SWR ;SET SWR TO HARD SWR ADDRESS
7026 002562 012737 177570 001242 MOV #177570,DISPLAY ;SET DISPLAY TO HARD SWR ADDRESS
7027 002574 022777 177777 176436 CNP #-1,2SMR ;REFERENCE HARDWARE SWITCH REGISTER
7028 002578 001402 BEQ 75 ;IF = -1 USE SOFT SWR ANYWAY
7029 002582 000407 BR 75 ;IF IT EXISTS AND NOT = -1 USE HARD SWR
7030 002606 022626 65: CNP (SP)+(SP)+ ;ADJUST STACK
7031 002610 012737 000176 001240 MOV #SMREG,SWR ;POINTER TO SOFT SWR
7032 002616 012737 000174 001242 MOV #0,SMREG,DISPLAY ;POINTER TO SOFT DISPLAY REG
7033 002624 012637 000004 75: MOV (SP)+,204 ;RESTORE VECTORS
7034 002630 012637 000006 MOV (SP)+,206
7035 002634 105737 001506 TSTB INIFLG ;HAS INITIALIZATION BEEN PERFORMED
7036 002640 001006 BNE 208 ;OR IF YES
7037 002642 022737 004070 000042 CNP #ENDADR,2042 ;IF ACT-11 AUTOMATIC MODE, DON'T TYPE ID
7038 002646 001402 BEQ 208
7039 002652 104401 001000 TYPE #TITLE ;TYPE TITLE MESSAGE
7040 002656 004737 011212 205: JSR #C,CKSWR ;CHECK FOR SOFT SWR
7041 002660 017737 176350 001446 MOV #SMR,STRTSW ;STORE STARTING SWITCHES
7042 002670 006737 000042 TST #042 ;IS IT RUNNING IN AUTO MODE?
7043 002674 001402 BEQ +6 ;OR IF NO
7044 002678 005037 001446 CLR STRTSW ;IF YES, CLEAR SWITCHES
7045 002702 022737 000001 001446 BIT #SM00,STRTSW ;IF SM00=1, QUESTIONS ARE ASKED.
7046 002710 001012 BNE 175 ;OR IF SM00=1
7047 002712 105737 001446 TSTB STRTSW ;BIT7=1??

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```

748 002716 100007 BPL 17S : BR IF SMO7=0
749 002720 005737 001470 TST KMACTV : ARE ANY DEVICES SELECTED?
750 002724 001027 BNE 16S : BR IF YES
751 002726 104401 010731 TYPE, NOACT : NO DEVICES SELECTED.
752 002730 000000 HALT : STOP THE SMO
753 002734 000776 BR : DISQUALIFY CONTINUE SWITCH
754 002736 105737 001336 17S: TSTB SENV : IS IT UNDER APT DUMP MODE?
755 002740 001405 BEQ 27S : YES, CHECK IF APT SIZED IT?
756 002744 132737 0000C1 001336 BITB B1,SENV : IS IT UNDER Q,V OR ALM MODE?
757 002752 001012 BNE 30S : YES, NEEDS ONLY APT SIZING.
758 002754 000405 BR 33S : NO, NEEDS REGULAR AUTO.SIZE.
759 002756 105737 001337 27S: TSTB SENVM : IS IT SIZED BY APT?
760 002762 100405 BHI 30S : YES, NEEDS ONLY APT SIZING.
761 002764 002737 000001 001446 BIC RSMO0,STRSM : SIZE ONLY IN AUTO MODE.
762 002772 004737 012110 33S: JSR PC,AUTO.SIZE : GO DO THE AUTO.SIZE.
763 002776 000405 BR 16S : GO PRINT THE MAP.
764 013000 004737 013510 30S: JSR PC,APT.SIZE : GO DO THE APT SIZING.
765 003004 105737 001506 16S: TSTB INIFLG : FIRST TIME?
766 013010 001410 BEQ 21S : BR IF YES
767 013012 105737 001446 TSTB STRSM : IF USING SAME PARAMETERS DONT TYPE MAP
768 013016 100431 BHI 1S : IS
769 013020 032737 000006 001446 BIT BIT1:BIT2,STRSM : IS TEST NO. OR LOCK SELECTED
770 013026 001403 BEQ 24S : IF NO THEN TYPE STATUS
771 013030 000424 BR 1S : IF YES DO NOT TYPE STATUS
772 013032 105137 001506 21S: COMB INIFLG : SET FLAG
773 013036 104401 010077 24S: TYPE XHEAD : TYPE HEADER
774 013042 012704 002100 NOV R4,MAP,R4 : SET POINTER
775 013046 010437 001276 5S: NOV R4,STMP0 : SET ADDRESS
776 013052 012437 001300 NOV (R4)+,STMP1 : SET CTR
777 013056 001411 BEQ 1S : ALL DONE IF ZERO
778 013060 012437 001302 NOV (R4)+,STMP2 : SET STAT1
779 013064 012437 001304 NOV (R4)+,STMP3 : SET STAT2
780 013070 012437 001306 NOV (R4)+,STMP4 : SET STAT3
781 013074 104416 CONVRT : TYPE OUT STATUS MAP
782 013076 011060 XSTAT0 :
783 013100 000762 BR 5S :
784 013102 012700 002100 1S: NOV R0,MAP,R0 : R0 POINTS TO STATUS TABLE

```

```

*****
: #AUTO SIZE TEST
: #THIS TEST VERIFYS THAT THE KNC11S AND/OR KNC11S ARE AT THE CORRECT FLOATING
: #ADDRESSES FOR YOUR SYS. IF THIS TEST FAILS, IT IS NOT A HARDWARE ERROR.
: #CHECK THE ADDRESSES OF ALL FLOATING DEVICES (DT,DH,DO,DU,DUP,LK,DNC,DZ,KNC).
: #IF THERE ARE NO OTHER FLOATING DEVICES BEFORE THE KNC11, THE FIRST
: # KNC11 IS 760110. NO DEVICE SHOULD EVER BE AT
: #ADDRESS 760000.
*****

```

```

795 003106 012746 000004 NOV R04,-(SP) : SAVE LOC 4
796 013112 012746 000006 NOV R06,-(SP) : SAVE LOC 6
797 013116 000007 CLR R08 : CLEAR VEC+2
798 013122 000007 CLR STMP2 : CLEAR FLAG
800 013126 011060 000006 AUSTRT: NOV (R0),KNC5R : GET NEXT KNC CSR
801 013132 011510 BEQ ALDONE : BR IF DONE
802 013136 012746 000240 2S: NOV SMODEV,R04 : SET UP FOR TIMEOUT
803 013142 012700 000010 3S: NOV R10,R3 : R3 IS COUNT OF DEVICES BEFORE KNC

```

INITIALIZATION AND START UP.

804	003146	012702	003342	4S:	MOV	#DEVTAB,R2	:R2 IS DEVICE TABLE POINTER
805	003152	012701	160010		MOV	#160010,R1	:START WITH ADDRESS 160010
806	003158	005711		FLOAT:	TST	(R1)	:CHECK ADDRESS IN R1
807	003164	111204			MOVB	(R2),R4	:IF NO TIMEOUT, GET NEXT ADDRESS
808	003162	060401			ADD	R4,R1	:IN R1
809	003164	005201			INC	R1	
810	003166	040401			BIC	R4,R1	
811	003170	005703			TST	R3	:ANY MORE DEVICES TO CHECK FOR?
812	003172	001371			BNE	FLOAT	:BR IF YES
813	003174	012737	003244	000004	MOV	#ERR,004	:OK ONLY KMC'S ARE LEFT, SET UP FOR TIMEOUT
814	003208	005711		FY:	TST	(R1)	:CHECK KMC ADDRESS
815	003209	020137	002066		CHP	R1,KMCSR	:DOES IT MATCH
816	003210	001403			BEQ	OK	:BR IF YES
817	003212	062701	000010		ADD	#10,R1	:GET NEXT KMC ADDRESS
818	003216	000771			BR	FY	:DO IT AGAIN
819	003220	062700	000010	OK:	ADD	#10,R0	:SKIP TO NEXT KMC CSR
820	003224	062701	000010		ADD	#10,R1	:GET NEXT KMC ADDRESS
821	003230	011037	002066		MOV	(R0),KMCSR	:GET NEXT KMC CSR
822	003234	001447			BEQ	ALDONE	:BRANCH IF ALL DONE.
823	003236	000761			BR	FY	:DO IT AGAIN.
824	003240	122443		NODEV:	CHPB	(R2)+,-(R3)	:ON TIMEOUT, INC R2, DEC R3
825	003242	000002			RTI		:BLAOR
826	003244	005737	001302	ERR:	TST	\$TMP2	:CHECK FLAG IF = 0 TYPE HEADER
827	003250	001014			BNE	IS	:SKIP HEADER
828	003252	104401			TYPE		:TYPEOUT HEADER MESSAGE
829	003254	010762			CONERR		:CONFIGURATION ERROR!!!!
830	003256	012737	003244	001460	MOV	#ERR,\$AVPC	:SAVE PC FOR TYPEOUT
831	003254	104417			CONVRT		:TYPE OUT ERROR PC
832	003256	003322			ERRPC		
833	003270	104401			TYPE		:TYPE REST OF HEADER
834	003272	011027			CHERR		
835	003274	012737	177777	001302	MOV	#-1,\$TMP2	:SET FLAG SO IT ONLY GETS TYPED ONCE
836	003302	010137	001264	1S:	MOV	R1,\$REG1	:SAVE R1 FOR TYPEOUT
837	003306	104416			CONVRT		
838	003310	003330			CONTAB		:TYPE CSR VALUES
839	003312	104401		3S:	TYPE		
840	003314	011050			KMCH		
841	003316	022626		4S:	CHP	(SP)+,(SP)+	:ADJUST STACK
842	003320	000737			BR	OK	:BR TO GET OUT
843	003322	000001		ERRPC:	1		
844	003324	006	002		.BYTE	6,2	
845	003326	001460			\$AVPC		
846	003330	000002		CONTAB:	2		
847	003332	006	004		.BYTE	6,4	
848	003334	001264			\$REG1		
849	003336	006	002		.BYTE	6,2	
850	003340	002066			KMCSR		
851	003342	007		DEVTAB:	.BYTE	7	:DJ
852	003343	017			.BYTE	17	:DH
853	003344	007			.BYTE	7	:DD
854	003345	007			.BYTE	7	:DU
855	003346	007			.BYTE	7	:DUP
856	003347	007			.BYTE	7	:LK
857	003350	007			.BYTE	7	:DMC
858	003351	007			.BYTE	7	:DZ
859	003352	007			.BYTE	7	:KMC

860	003354	003354									
861	003354	012637	000006								
862	003354	012637	000004								
863	003354	032737	000010	001446							
864	003372	001422									
865	003374	104401	010017								
866	003400	005000									
867	003402	000000									
868	003404	027737	175630	001474							
869	003412	101404									
870	003414	104401	007672								
871	003420	000000									
872	003422	000776									
873	003424	017737	175610	001470	25:						
874	003432	013700	001470								
875	003436	000000									
876	003440	012700	000300		35:						
877	003444	012701	000302								
878	003450	010120			45:						
879	003452	005021									
880	003454	022021									
881	003456	022700	001000								
882	003462	001372									
883											
884											
885											
886											
887											
888	003464	012706	001200								
889	003470	013746	000006								
890	003474	013746	000004								
891	003500	005000									
892	003502	012737	003546	000004							
893	003510	005037	000006								
894	003514	005720			65:						
895	003516	022700	157776								
896	003522	001374									
897	003524	162700	007776								
898	003530	010037	001466		75:						
899	003534	012637	000004								
900	003540	012637	000006								
901	003544	000413									
902	003546	022626			25:						
903	003550	162700	000004								
904	003554	162700	007776								
905	003560	022700	030000								
906	003564	001361									
907	003566	012700	037400								
908	003572	000756									
909	003574	012737	000340	177776	105:						
910	003602	032737	000004	001446							
911	003610	001406									
912	003612	104401	007716								
913	003616	012737	000240	004146							
914	003624	000403									
915	003626	013737	004360	004146	15:						

```

EVEN
ADDONE:
15:  MOV      (SP)+,2#6      ;RESTORE LOC 6
      MOV      (SP)+,2#4      ;RESTORE LOC 4
      BIT      #SM03,STRSM    ;SELECT SPECIFIC DEVICES??
      BEQ     35              ;BR IF NO.
      TYPE    MNEW           ;TYPE THE MESSAGE.
      CLR     R0              ;ZERO DATA LIGHTS
      HALT                    ;WAIT FOR USER TO TELL WHAT DEVICES TO RUN
      CMP     #SMR,SAYACT    ;IS THE NUMBER VALID?
      BLOS   25              ;BR IF NUMBER IS OK.
      TYPE    ,MERR3        ;TELL USER OF INVALID NUMBER.
      HALT                    ;STOP EVERYTHING.
      BR     -2              ;RESTART THE PROGRAM AGAIN.
25:  MOV      #SMR,KMACTV    ;GET NEW DEVICE PATTERN
      MOV      KMACTV,R0     ;SHOW THE USER WHAT HE SELECTED.
      HALT                    ;CONTINUE DYNAMIC SWITCHES.
35:  MOV      #300,R0        ;PREPARE TO CLEAR THE FLOATING
      MOV      #302,R1        ;VECTOR AREA. 300-776
      MOV      R1,(R0)+      ;START PUTTING "PC+2 - HALT"
      CLR     (R1)+          ;IN VECTOR AREA.
      CMP     (R0)+,(R1)+    ;POP POINTERS
      CMP     #1000,R0       ;ALL DONE??
      BNE    45              ;BR IF NO.
45:  BNE

;TEST START AND RESTART
-----
.BEGIN: MOV      #STACK,SP  ;SET UP STACK
      MOV      2#6,-(SP)    ;SAVE LOC 6
      MOV      2#4,-(SP)    ;SAVE LOC 4
      CLR     R0            ;START AT 0
      MOV      #25,2#4      ;SET UP FOR TIME OUT
      CLR     2#6          ;TO AUTOSIZE MEMORY
85:  TST     (R0)+          ;CHECK ADDRESS IN R0
      CMP     #157776,R0    ;IS IT AT LEAST 28K
      BNE    65            ;BR IF NO
      SUB     #7776,R0      ;SAVE 2K FOR MONITORS
87:  MOV     R0,HEALTH      ;STORE MEMORY LIMIT
      MOV     (SP)+,2#4     ;RESTORE LOC 4
      MOV     (SP)+,2#6     ;RESTORE LOC 6
      BR     105           ;CONTINUE
25:  CMP     (SP)+,(SP)+    ;ADJUST STACK
      SUB     #4,R0         ;GET LAST GOOD ADDRESS
      SUB     #7776,R0      ;SAVE 2K FOR MONITORS
      CMP     #30000,R0     ;IS IT OK?
      BNE    75            ;BR IF NO
      MOV     #37400,R0     ;IF OK DON'T SAVE 2K
      BR     75

105: MOV     #340,PS        ;LOCK OUT INTERRUPTS
      BIT     #BIT2,STRSM  ;CHECK FOR LOCK ON TEST
      BEQ    15            ;BR IF NO LOCK DESIRED.
      TYPE    #LOCK        ;TYPE LOCK SELECTED.
      MOV     #NOP,TTST    ;SET UP TO LOCK
      BR     35           ;CONTINUE ALONG.
15:  MOV     #AW,TTST      ;PREPARE NORMAL SCOPE ROUTINE

```

H04

DZKCC MACY11 27(1006) 12-MAY-77 18:34 PAGE 20  
DZKCC.P11 21-MAR-77 17:19

PROGRAM INITIALIZATION AND START UP.

PAGE: 0046

916	003634	012737	011460	001206	3\$:	MOV	#CYCLE,\$LPADR	; START AT "CYCLE" FIND WHICH DEVICE TO TEST
917	003642	032737	000002	001446	4\$:	BIT	#SW01,STRTSW	; IS TEST NO. SELECTED?
918	003650	001002				BNE	\$S	; BR IF YES
919	003652	104401	007642			TYPE	MR	; TYPE R
920	003656	000177	175324		5\$:	JMP	\$LPADR	; START TESTING



```

977 004102 011460
978 004104 000001
979 004106 006 002
980 004110 002066
981 004112 000001
982 004114 004 002
983 004116 002056
984 004120 000001
985 004122 006 002
986 004124 001324
987 004126 000001
988 004130 006 002
989 004132 001212
990
991
992
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996
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998
999
1000
1001
1002
1003
1004
1005
1006 004134
1007 004134 005037 001216
1008 004140 023716 013734
1009 004144 001413
1010 004146 000406
1011 004150 105777 175070
1012 004154 100067
1013 004156 017766 175064 177776
1014 004164 032777 040000 175046
1015 004172 001060
1016
1017 004174 000416
1018
1019 004176 015746 000004
1020 004202 012737 004222 000004
1021 004210 005737 177060
1022 004214 012637 000004
1023 004220 000436
1024 004222 022626
1025 004224 012637 000004
1026 004230 000441
1027 004232
1028 004232 105737 001203
1029 004236 001404
1030 004240 105037 001203
1031 004244 005037 001310
1032 004250 032777 004000 174762

```

```

SRTNAD: .WORD CYCLE
XCSR: 1
      .BYTE 6,2
      KMCSR
XVEC: 1
      .BYTE 4,2
      KMRVEC
XPASS: 1
      .BYTE 6,2
      SPASS
XERR: 1
      .BYTE 6,2
      SERTTL

```

;;SCOPE LOOP AND INTERATION HANDLER

.SBTTL SCOPE HANDLER ROUTINE

```

*****
;THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
;AND LOAD THE TEST NUMBER(STSTN) INTO THE DISPLAY REG.(DISPLAY<7:0>).
;AND LOAD THE ERROR FLAG (SEFLG) INTO DISPLAY<15:08>
;THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
;SM14=1 LOOP ON TEST
;SM11=1 INHIBIT ITERATIONS
;CALL
; SCOPE ;;SCOPE=IOT
;SCOPE:
CLR SEFLG ; CLEAR LAST ERROR PC
CHP TST1+2,(SP) ; IS THIS TEST #1?
REQ SXTSTR ; IF SO DON'T LOOP.
BR IS
TTST: TSTB STICKS ; KEYBOARD DONE?
      BPL SOVER ; IF NO DON'T WAIT.
      MOV STICKB,-2(SP)
IS: BIT BIT14,SSMR ; LOOP ON PRESENT TEST?
      BNE SOVER ; YES IF SM14=1
;#####START OF CODE FOR THE XOR TESTER#####
SXTSTR: BR 65 ; IF RUNNING ON THE "XOR" TESTER CHANGE
      ; THIS INSTRUCTION TO A "NOP" (NOP=240)
      ; SAVE THE CONTENTS OF THE ERROR VECTOR
      ; SET FOR TIMEOUT
      ; TIME OUT ON XOR?
      ; RESTORE THE ERROR VECTOR
      ; GO TO THE NEXT TEST
      ; CLEAR THE STACK AFTER A TIME OUT
      ; RESTORE THE ERROR VECTOR
      ; LOOP ON THE PRESENT TEST
      ;#####END OF CODE FOR THE XOR TESTER#####
65: TSTB SEFLG ; HAS AN ERROR OCCURRED?
      BEQ 25 ; IF NO
45: CLRB SEFLG ; ZERO THE ERROR FLAG
      CLR STICKS ; CLEAR THE NUMBER OF ITERATIONS TO MAKE
      BIT11,SSMR ; INHIBIT ITERATIONS?

```





1089	004434	122737	000001	001336		CMPB	#APTENV,SENV	::RUNNING IN APT MODE
1090	004442	001011				BNE	62S	::NO GO CHECK FOR APT CONSOLE
1091	004444	132737	000100	001337		BITB	#APTSPOOL,SENV	::SPOOL MESSAGE TO APT
1092	004453	001405				BEQ	62S	::NO GO CHECK FOR CONSOLE
1093	004454	010037	004464			MOV	RO,61S	::SETUP MESSAGE ADDRESS FOR APT
1094	004460	004737	004704			JSR	PC,SATY3	::SPOOL MESSAGE TO APT
1095	004464	000000					0	::MESSAGE ADDRESS
1096	004466	132737	000040	001337	61S:	.WORD	0	::APT CONSOLE SUPPRESSED
1097	004474	001003			62S:	BITB	#APTCSUP,SENV	::YES,SKIP TYPE OUT
1098	004476	112046			2S:	MOV	(RO)+,-(SP)	::PUSH CHARACTER TO BE TYPED ONTO STACK
1099	004500	001005				BNE	4S	::OR IF IT IS THE TERMINATOR
1100	004502	005726				TST	(SP)+	::IF TERMINATOR POP IT OFF THE STACK
1101	004504	012600			60S:	MOV	(SP)+,RO	::RESTORE RO
1102	004506	062716	000002		3S:	ADD	#2,(SP)	::ADJUST RETURN PC
1103	004512	000002				RTI		::RETURN
1104	004514	122716	000011		4S:	CMPB	#HT,(SP)	::BRANCH IF <HT>
1105	004520	001430				BEQ	8S	::BRANCH IF NOT <CRLF>
1106	004522	122716	000200			CMPB	#CRLF,(SP)	::BRANCH IF NOT <CRLF>
1107	004526	001006				BNE	5S	::POP <CR><LF> EQUIV
1108	004530	005726				TST	(SP)+	::TYPE A CR AND LF
1109	004532	104401				TYPE		::CLEAR CHARACTER COUNT
1110	004534	001313				SCRLF		::GET NEXT CHARACTER
1111	004536	105037	004672			CLRB	#SCHARCNT	::DO TYPE THIS CHARACTER
1112	004542	000755				BR	2S	::IS IT TIME FOR FILLER CHARS.?
1113	004544	004737	004626		5S:	JSR	PC,STYPEC	::IF NO GO GET NEXT CHAR.
1114	004550	123726	001256		6S:	CMPB	#FILLC,(SP)+	::GET # OF FILLER CHARS. NEEDED
1115	004554	001350				BNE	2S	::AND THE NULL CHAR.
1116	004556	013746	001254			MOV	#NULL,-(SP)	::DOES A NULL NEED TO BE TYPED?
1117								::OR IF NO--GO POP THE NULL OFF OF STACK
1118	004562	105366	000001		7S:	DECB	1,(SP)	::GO TYPE A NULL
1119	004566	002770				BLT	6S	::DO NOT COUNT AS A COUNT
1120	004570	004737	004626			JSR	PC,STYPEC	::LOOP
1121	004574	105337	004672			DECB	#SCHARCNT	
1122	004600	000770				BR	7S	
1123								
1124								
1125								
1126	004602	112716	000040		8S:	MOV	#1,(SP)	::REPLACE TAB WITH SPACE
1127	004606	004737	004626		9S:	JSR	PC,STYPEC	::TYPE A SPACE
1128	004612	132737	000007	004672		BITB	#7,SCHARCNT	::BRANCH IF NOT AT
1129	004620	001372				BNE	9S	::TAB STOP
1130	004622	005726				TST	(SP)+	::POP SPACE OFF STACK
1131	004624	000724				BR	2S	::GET NEXT CHARACTER
1132	004626	105777	174416		STYPEC:	TSTB	#STPS	::WAIT UNTIL PRINTER IS READY
1133	004632	100375				BPL	STYPEC	
1134	004634	116677	000002	174410		MOV	2,(SP) #STPB	::LOAD CHAR TO BE TYPED INTO DATA REG.
1135	004642	122766	000015	000002		CMPB	#CR,2(SP)	::IS CHARACTER A CARRIAGE RETURN?
1136	004650	001003				BNE	1S	::BRANCH IF NO
1137	004652	105037	004672			CLRB	#SCHARCNT	::YES--CLEAR CHARACTER COUNT
1138	004656	000406				BR	STYPEX	::EXIT
1139	004660	122766	000012	000002	1S:	CMF	#LF,2(SP)	::IS CHARACTER A LINE FEED?
1140	004666	001402				BEQ	STYPEX	::BRANCH IF YES
1141	004670	105227				INCB	(PC)+	::COUNT THE CHARACTER
1142	004672	000000				SCHARCNT:	.WORD	::CHARACTER COUNT STORAGE
1143	004674	000207				STYPEX:	RTS	
1144							PC	

APT COMMUNICATIONS ROUTINE

.SBTTL APT COMMUNICATIONS ROUTINE

```

1145
1146
1147
1148 004676 112737 000001 005142 SATY1: MOVB #1,SFFLG ;; TO REPORT FATAL ERROR
1149 004704 112737 000001 005140 SATY3: MOVB #1,SFFLG ;; TO TYPE A MESSAGE
1150 004712 000403 BR SATYC
1151 004714 112737 000001 005142 SATY4: MOVB #1,SFFLG ;; TO ONLY REPORT FATAL ERROR
1152 004722 SATYC:
1153 004722 010046 MOV R0,-(SP) ;; PUSH R0 ON STACK
1154 004724 010146 MOV R1,-(SP) ;; PUSH R1 ON STACK
1155 004726 105737 005140 TSTB SFFLG ;; SHOULD TYPE A MESSAGE?
1156 004732 001450 BEQ SS ;; IF NOT: BR
1157 004734 122737 000001 001336 CNPB #APTENV,SENV ;; OPERATING UNDER APT?
1158 004742 001031 BNE SS ;; IF NOT: BR
1159 004744 132737 000100 001337 BITB #APTSPOOL,SENVH ;; SHOULD SPOOL MESSAGES?
1160 004752 001425 BEQ SS ;; IF NOT: BR
1161 004754 017600 000004 MOV #4(SP),R0 ;; GET MESSAGE ADDR.
1162 004760 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDR.
1163 004766 005737 001316 1S: TST #MSGTYPE ;; SEE IF DONE W/ LAST XMISSION?
1164 004772 001375 BNE SS ;; IF NOT: WAIT
1165 004774 010037 001332 MOV R0,#MSGAD ;; PUT ADDR IN MAILBOX
1166 005000 105720 2S: TSTB (R0)+ ;; FIND END OF MESSAGE
1167 005002 001375 BNE SS
1168 005004 163700 001332 SUB #MSGAD,R0 ;; SUB START OF MESSAGE
1169 005010 006200 RSR R0 ;; GET MESSAGE LENGTH IN WORDS
1170 005012 010037 001334 MOV R0,#MSGLGTY ;; PUT LENGTH IN MAILBOX
1171 005016 012737 000004 001316 MOV #4,#MSGTYPE ;; TELL APT TO TAKE MSG.
1172 005024 000413 BR SS
1173 005026 017637 000004 005052 3S: MOV #4(SP),4S ;; PUT MSG ADDR IN JSR LINKAGE
1174 005034 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDRESS
1175 005042 013746 177776 004414 MOV #177776,-(SP) ;; PUSH 177776 ON STACK
1176 005046 004737 JSR PC,#TYPE ;; CALL TYPE MACRO
1177 005052 000000 4S: .WORD 0
1178 005054 5S:
1179 005054 105737 005142 10S: TSTB SFFLG ;; SHOULD REPORT FATAL ERROR?
1180 005060 001416 BEQ SS ;; IF NOT: BR
1181 005062 005737 001336 TST SENV ;; RUNNING UNDER APT?
1182 005066 001413 BEQ SS ;; IF NOT: BR
1183 005070 005737 001316 11S: TST #MSGTYPE ;; FINISHED LAST MESSAGE?
1184 005074 001375 BNE SS ;; IF NOT: WAIT
1185 005076 017637 000004 001320 MOV #4(SP),#FATAL ;; GET ERROR #
1186 005104 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDR.
1187 005112 005237 001316 12S: INC #MSGTYPE ;; TELL APT TO TAKE ERROR
1188 005116 105037 005142 CLRB SFFLG ;; CLEAR FATAL FLAG
1189 005122 105037 005141 CLRB SLFLG ;; CLEAR LOG FLAG
1190 005126 105037 005140 CLRB SFFLG ;; CLEAR MESSAGE FLAG
1191 005132 012601 MOV (SP)+,R1 ;; POP STACK INTO R1
1192 005134 012600 MOV (SP)+,R0 ;; POP STACK INTO R0
1193 005136 000207 RTS PC ;; RETURN
1194 005140 000 SMFLG: .BYTE 0 ;; MESSG. FLAG
1195 005141 000 SLFLG: .BYTE 0 ;; LOG FLAG
1196 005142 000 SFFLG: .BYTE 0 ;; FATAL FLAG
1197 005144 .EVEN
1198 000200 APTSIZE=200
1199 000001 APTENV=001
1200 000100 APTSPOOL=100

```

APT COMMUNICATIONS ROUTINE

APTCSUP=040

.SBTTL TTY INPUT ROUTINE

\*\*\*\*\*

.ENABL LSB

.DSABL LSB

\*\*\*\*\*

\*THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY

\*CALL:

\* RDCHR INPUT A SINGLE CHARACTER FROM THE TTY  
\* RETURN HERE CHARACTER IS ON THE STACK  
\* WITH PARITY BIT STRIPPED OFF

1201  
1202  
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1254  
1255  
1256

000040  
005144 011646  
005146 016666 000004 000002  
005154 105777 174064  
005150 100375  
005162 117766 174060 000004  
005170 042766 177600 000004  
005176 026627 000004 000023  
005204 001013  
005206 105777 174032  
005212 100375  
005214 117746 174026  
005220 042716 177600  
005224 022627 000021  
005230 001366  
005232 000750  
005234 026627 000004 000140  
005242 002407  
005244 026627 000004 000175  
005252 003003  
005254 042766 000040 000004  
005262 000002

SRDCHR: MOV (SP), -(SP)  
MOV 4(SP), 2(SP)  
1\$: TSTB 25TKS  
BR 1\$  
NOVB 25TKB, 4(SP)  
BIC 81C(177), 4(SP)  
CMP 4(SP), 023  
BNE 2\$  
TSTB 25TKS  
BR 2\$  
NOVB 25TKB, -(SP)  
BIC 81C(177), (SP)  
CMP (SP)+, 021  
BNE 3\$  
CMP 4(SP), 0140  
BLT 4\$  
CMP 4(SP), 0175  
BGT 4\$  
BIC 040, 4(SP)  
RTY  
4\$:

PUSH DOWN THE PC  
SAVE THE PS  
WAIT FOR  
A CHARACTER  
READ THE TTY  
GET RID OF JUNK IF ANY  
IS IT A CONTROL-5?  
BRANCH IF NO  
WAIT FOR A CHARACTER  
LOOP UNTIL ITS THERE  
GET CHARACTER  
MAKE IT 7-BIT ASCII  
IS IT A CONTROL-0?  
IF NOT DISCARD IT  
YES, RESUME  
IS IT UPPER CASE?  
BRANCH IF YES  
IS IT A SPECIAL CHAR?  
BRANCH IF YES  
MAKE IT UPPER CASE  
GO BACK TO USER

\*\*\*\*\*

\*THIS ROUTINE WILL INPUT A STRING FROM THE TTY

\*CALL:

\* RDLIN INPUT A STRING FROM THE TTY  
\* RETURN HERE ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK  
\* TERMINATOR WILL BE A BYTE OF ALL 0'S

SRDLIN: MOV R3, -(SP)  
CLR -(SP)  
1\$: MOV #51TYIN, R3  
2\$: CMP #51TTYIN+7, R3  
BLOS 4\$  
RDCHR  
NOVB (SP)+, (R3)  
10\$: CMPB 0177, (R3)  
BNE 5\$

SAVE R3  
CLEAR THE RUBOUT KEY  
GET ADDRESS  
BUFFER FULL?  
BR IF YES  
GO READ ONE CHARACTER FROM THE TTY  
GET CHARACTER  
IS IT A RUBOUT  
BR IF NO

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1257 005314 005716 TST (SP) ; IS THIS THE FIRST RUBOUT?
1258 005316 001007 BNE 65 ; BR IF NO
1259 005320 112737 000134 005516 MOVB #' \, 95 ; TYPE A BACK SLASH
1260 005326 104401 005516 TYPE 95
1261 005332 012716 177777 MOV 1-1, (SP) ; SET THE RUBOUT KEY
1262 005336 005303 65: DEC R3 ; BACKUP BY ONE
1263 005340 020327 005520 CMP R3, #STTYIN ; STACK EMPTY?
1264 005344 103434 BLO 45 ; BR IF YES
1265 005346 111337 005516 MOVB (R3), 95 ; SETUP TO TYPEOUT THE DELETED CHAR.
1266 005352 104401 005516 TYPE 95 ; GO TYPE
1267 005356 000746 BR 25 ; GO READ ANOTHER CHAR.
1268 005360 005716 55: TST (SP) ; RUBOUT KEY SET?
1269 005362 001406 BEQ 75 ; BR IF NO
1270 005364 112737 000134 005516 MOVB #' \, 95 ; TYPE A BACK SLASH
1271 005372 104401 005516 TYPE 95
1272 005376 005016 CLR (SP) ; CLEAR THE RUBOUT KEY
1273 005400 122713 000025 75: CMPB 25, (R3) ; IS CHARACTER A CTRL U?
1274 005404 001003 BNE 85 ; BR IF NO
1275 005406 104401 005527 TYPE 1, $CNTLU ; TYPE A CONTROL "U"
1276 005412 000726 BR 15 ; GO START OVER
1277 005414 122713 000022 85: CMPB 22, (R3) ; IS CHARACTER A "1R"?
1278 005420 001011 BNE 35 ; BRANCH IF NO
1279 005422 105013 CLRB (R3) ; CLEAR THE CHARACTER
1280 005424 104401 001313 TYPE 1, $CLRF ; TYPE A "CR" & "LF"
1281 005430 104401 005520 TYPE 1, $TTYIN ; TYPE THE INPUT STRING
1282 005434 000717 BR 25 ; GO PICKUP ANOTHER CHARACTER
1283 005436 104401 001312 45: TYPE 1, $QUES ; TYPE A '?'
1284 005440 000712 BR 15 ; CLEAR THE BUFFER AND LOOP
1285 005444 111337 005516 35: MOVB (R3), 95 ; ECHO THE CHARACTER
1286 005450 104401 005516 TYPE 95
1287 005454 122723 000015 65: CMPB 15, (R3)+ ; CHECK FOR RETURN
1288 005460 001305 BNE 25 ; LOOP IF NOT RETURN
1289 005462 105063 177777 CLRB -1(R3) ; CLEAR RETURN (THE 15)
1290 005466 104401 001311 TYPE 1, $LF ; TYPE A LINE FEED
1291 005472 005726 TST (SP)+ ; CLEAR RUBOUT KEY FROM THE STACK
1292 005474 012603 MOV (SP)+, R3 ; RESTORE R3
1293 005476 011646 MOV (SP), -(SP) ; ADJUST THE STACK AND PUT ADDRESS OF THE
1294 005500 016666 000000 000000 MOV 4(SP), 2(SP) ; FIRST ASCII CHARACTER ON IT
1295 005506 012766 000000 000000 MOV #STTYIN, 4(SP)
1296 005514 000002 RTI ; RETURN
1297 005516 000 .BYTE 0 ; STORAGE FOR ASCII CHAR. TO TYPE
1298 005517 000 .BYTE 0 ; TERMINATOR
1299 005520 000007 $TTYIN: .BLKB 7 ; RESERVE 7 BYTES FOR TTY INPUT
1300 005527 136 006525 $CNTLU: .ASCIZ /1U/<15><12> ; CONTROL "U"
1301 005534 043536 005015 $CNTLG: .ASCIZ /1G/<15><12> ; CONTROL "G"
1302 005541 015 051127 $MSMR: .ASCIZ <15><12>/SMR = /
1303 005546 036440 000040 $MNEW: .ASCIZ / NEW = /
1304 005552 020040 042516 020127 .EVEN
1305 005560 020075 000 .SBTTL READ AN OCTAL NUMBER FROM THE TTY
1306 005564
1307
1308
1309 ;*****
1310 ;THIS ROUTINE WILL READ AN OCTAL (ASCII) NUMBER FROM THE TTY AND
1311 ;CHANGE IT TO BINARY.
1312 ;THE INPUT CHARACTERS WILL BE CHECKED TO INSURED THEY ARE LEGAL

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1313 ;#OCTAL DIGITS. IF AN ILLEGAL CHARACTER IS READ A "*" WILL BE TYPED
1314 ;#FOLLOWED BY A CARRIAGE RETURN-LINE FEED, THE COMPLETE NUMBER MUST
1315 ;#THEN BE RETYPED. THE INPUT IS TERMINATED BY TYPING A CARRIAGE RETURN.
1316 ;#CALL:
1317 ;*          RDOCT          ;; READ AN OCTAL NUMBER
1318 ;*          RETURN HERE   ;; LOW ORDER BITS ARE ON TOP OF THE STACK
1319 ;*                                     ;; HIGH ORDER BITS ARE IN SHIOCT
1320
1321 005564 011646 000004 000002 SRDOCT: MOV      (SP), -(SP)          ;; PROVIDE SPACE FOR THE
1322 005566 016666          MOV      4(SP), 2(SP)        ;; INPUT NUMBER
1323 005574 010046          MOV      R0, -(SP)          ;; PUSH R0 ON STACK
1324 005576 010146          MOV      R1, -(SP)          ;; PUSH R1 ON STACK
1325 005600 010246          MOV      R2, -(SP)          ;; PUSH R2 ON STACK
1326 005602 104403          15:  RDLIN          ;; READ AN ASCII LINE
1327 005604 012600          MOV      (SP)+, R0        ;; GET ADDRESS OF 1ST CHARACTER
1328 005606 010037 005712  MOV      R0, 55          ;; AND SAVE IT
1329 005612 005001          CLR      R1              ;; CLEAR DATA WORD
1330 005614 005002          CLR      R2
1331 005616 112046          25:  MOVWB   (R0)+, -(SP)      ;; PICKUP THIS CHARACTER
1332 005620 001420          BEQ      35              ;; IF ZERO GET OUT
1333 005622 122716 000350  CMPB    #'0', (SP)        ;; MAKE SURE THIS CHARACTER
1334 005626 003026          BGT      45              ;; IS AN OCTAL DIGIT
1335 005630 122716 001000  CMPB    #'7', (SP)
1336 005634 002000          BGT      45
1337 005636 002000          R1              ;; #2
1338 005640 002000          R2              ;; #4
1339 005642 002000          R1              ;; #8
1340 005644 002000          R2
1341 005646 002000          R1
1342 005650 00610F          R2
1343 005652 042716          ROL      #107, (SP)      ;; STRIP THE ASCII JUNK
1344 005656 062601          BIC      (SP)+, R1        ;; ADD IN THIS DIGIT
1345 005660 000756          ADD     25              ;; LOOP
1346 005662 005726          BR       35              ;; CLEAN TERMINATOR FROM STACK
1347 005664 010166 000012  TST     (SP)+            ;; SAVE THE RESULT
1348 005670 010237 005722  MOV     R1, 12(SP)
1349 005674 012602          MOV     R2, SHIOCT
1350 005676 012601          MOV     (SP)+, R2
1351 005700 012600          MOV     (SP)+, R1
1352 005702 000002          MOV     (SP)+, R0
1353 005704 005726          RTI
1354 005706 105010          45:  TST     (SP)+            ;; CLEAN PARTIAL FROM STACK
1355 005710 104401          CLRB   (R0)              ;; SET A TERMINATOR
1356 005712 000000          TYPE   0                 ;; TYPE UP THRU THE BAD CHAR.
1357 005714 104401 001312  55:  .WORD  0
1358 005720 000730          TYPE   'QUES            ;; "?" "CR" & "LF"
1359 005722 000000          BR     15                 ;; TRY AGAIN
SHIOCT: .WORD  0          ;; HIGH ORDER BITS GO HERE
-----
INPUT OCTAL NUMBER ROUTINE
$INPUT: MOV     R5, -(SP)          ;; SAVE REGISTER R5.
MOV     2(SP), R5          ;; GET FIRST PARAMETER ADDRESS.
MOV     (R5)+, WHAT        ;; GET MESSAGE ADDRESS.
MOV     (R5)+, LOLIM       ;; GET LOW LIMIT FOR THE #
MOV     (R5)+, HILIM       ;; GET HIGH LIMIT FOR THE #.
    
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1369 005746 012537 006054      MOV      (RS)+,WHERE      ; GET ADDRESS OF INBUFFER.
1370 005752 112537 006056      MOV      (RS)+,LOBITS    ; GET LOWMASK BITS.
1371 005756 112537 006057      MOV      (RS)+,AORCNT    ; GET # OF #'S TO BE GENERATED.
1372 005760 010566 000002      MOV      RS,2(SP)        ; SAVE THE RETURN ADDRESS.
                                INLP1:  TYPE      ; TYPE THE MESSAGE.
                                WHAT:   .WORD      0
1373 005764 104401 000000      RDOCT
1374 005770 000000      RDOCT
1375 005772 104404 000000      RDOCT
1376 005774 021637 006052      CMP      (SP),HILIM      ; READ OCTAL # FROM KEYBOARD.
1377 005000 003003 000000      BGT      25              ; IS IT IN HIGH LIMIT?
1378 005002 021637 006050      CMP      (SP),LOLIM      ; BRANCH IF NO.
1379 005006 002005 000000      BGE      35              ; IS IT MORE THAN LOW LIMIT.
1380 006010 104401 001312      25:      TYPE      .SOLUS      ; BRANCH IF YES.
1381 006014 104401 001313      TYPE      .SCLF         ; TYPE (CR), (LF)
1382 006020 000762 000000      BR
1383 006022 013705 006054      35:      MOV      WHERE,RS        ; GET BUFFER ADDRESS.
1384 006026 011625 000002      45:      MOV      (SP),RS+        ; SAVE THE # IN RIGHT PLACE.
1385 006030 002716 000002      ADD      RS,(SP)         ; NEXT SEQUENTIAL NUMBER.
1386 006034 105337 006057      DECB    AORCNT          ; COUNT BY 1.
1387 006040 001372 000000      BNE      45              ; BRANCH IF NOT DONE.
1388 006042 005726 000000      TST     (SP)+           ; POP THE STACK POINTER.
1389 006044 012505 000000      MOV     (SP)+,RS        ; POP THE REG.5
1390 006046 000002 000000      RTI
1391 006050 000000 000000      LOLIM:  .WORD      0
1392 006052 000000 000000      HILIM:  .WORD      0
1393 006054 000000 000000      WHERE:  .WORD      0
1394 006056 000000 000000      LOBITS: .BYTE      0
1395 006057 000000 000000      AORCNT: .BYTE      0
1396
1397
1398
1399
1400 006060 013716 001442      .ADVANCE: MOV      NEXT,(SP) ; CRUNCH STACK WITH ADDRESS OF SCOPE CALL
1401 006064 005037 001444      CLR      LOCK           ; RESET TIGHT LOOP ADDRESS
1402 006070 000002 000000      RTI                    ; CHECK TO SEE IF OLD TEST GETS REPEATED
1403
1404      ;SAVE PC OF TEST THAT FAILED AND RO-RS
1405
1406
1407 006072 016637 000004 001460 .SAVOS: MOV      4(SP),SAVPC ;SAVE R7 (PC)
1408
1409      ;SAVE RO-RS
1410
1411 006100 010537 001274      SVOS:  MOV      R5,AREG5 ;SAVE R5
1412 006104 010437 001272      MOV      R3,AREG3 ;SAVE R3
1413 006110 010337 001270      MOV      R2,AREG2 ;SAVE R2
1414 006114 010237 001266      MOV      R1,AREG1 ;SAVE R1
1415 006120 010137 001264      MOV      R0,AREG0 ;SAVE R0
1416 006124 010037 001262      MOV      R0,AREG0 ;SAVE R0
1417 006130 000002 000000      RTI                    ;LEAVE.
1418
1419      ;RESTORE RO-RS
1420
1421 006132 013700 001262      .RESOS: MOV      AREG0,R0 ;RESTORE R0
1422 006136 013701 001264      MOV      AREG1,R1 ;RESTORE R1
1423 006142 013702 001266      MOV      AREG2,R2 ;RESTORE R2
1424 006146 013703 001270      MOV      AREG3,R3 ;RESTORE R3

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1425	006152	013704	001272	MOV	\$REG4, R4	:RESTORE R4
1426	006156	013705	001274	MOV	\$REG5, R5	:RESTORE R5
1427	006162	000002		RTI		:LEAVE
1428						
1429						
1430						:CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
1431						-----
1432	006164	104401	001313	CONVR:	TYPE	SCALE
1433	006170	010046		CONVRT:	MOV	R0, -(R0)
1434	006172	010146			MOV	R1, -(R0)
1435	006174	010346			MOV	R2, -(R0)
1436	006176	010446			MOV	R3, -(R0)
1437	006200	010546			MOV	R5, -(R0)
1438	006202	017601	000012		MOV	R12(R0), R1
1439	006206	062766	000002		ROD	R0, 12(R0)
1440	006214	012137	006406		MOV	(R1)+, MROCNT
1441	006220	112137	006410	19:	MOVSB	(R1)+, CHARCNT
1442	006224	112137	006411		MOVSB	(R1)+, SPACNT
1443	006230	013137	006412		MOV	R3(R1)+, BINMRO
1444	006234	122737	000003	006410	CHPB	R3, CHARCNT
1445	006240	001003			BNE	ZS
1446	006244	042737	177400	006412	BIC	#177400, BINMRO
1447	006248	013704	006412	29:	MOV	BINMRO, R2
1448	006250	113705	006410		MOVSB	CHARCNT, R5
1449	006252	012700	011106		MOV	#TEMP, R0
1450	006256	010403		39:	MOV	R2, R3
1451	006270	042703	177770		BIC	#177770, R3
1452	006274	062703	000060		ROD	R060, R3
1453	006300	110320			MOVSB	R3, (R0)+
1454	006302	000241			CLC	
1455	006304	006004			ROR	R2
1456	006306	000241			CLC	
1457	006310	006004			ROR	R2
1458	006312	000241			CLC	
1459	006314	006004			ROR	R2
1460	006316	005305			DEC	CHARCNT
1461	006320	001362			BNE	CHARCNT
1462	006322	012703	011150		MOV	#DATA, R3
1463	006326	114023		49:	MOVSB	-(R0), (R3)+
1464	006330	105337	006410		DECSB	CHARCNT
1465	006334	001374			BNE	CHARCNT
1466	006336	105737	006411		TSTB	SPACNT
1467	006340	001405			BEO	SPACNT
1468	006344	112723	000040	59:	MOVSB	SPACNT, (R3)+
1469	006350	105337	006411		DECSB	SPACNT
1470	006354	001373			BNE	SPACNT
1471	006356	105013		69:	CLRB	(R3)
1472	006360	104401	011150		TYPE	#DATA
1473	006364	005337	006406		DEC	CHARCNT
1474	006370	001313			BNE	CHARCNT
1475	006372	012605			MOV	(R0)+, R0
1476	006374	012604			MOV	(R0)+, R0
1477	006376	012603			MOV	(R0)+, R0
1478	006400	012601			MOV	(R0)+, R0
1479	006402	012600			MOV	(R0)+, R0
1480	006404	000002			RTI	



1481 006406 000000  
1482 006410 000000  
1483 006411 000000  
1484 006412 000000

WRCNT: 0  
CHRCNT: 0  
SPACNT=CHRCNT+1  
BINWRD: 0

: TRAP DISPATCH SERVICE  
: ARGUMENT OF TRAP IS EXTRACTED  
: AND USED AS OFFSET TO OBTAIN POINTER  
: TO SELECTED SUBROUTINE

.SBTTL TRAP DECODER

\*\*\*\*\*  
: THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION  
: AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS  
: OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL  
: GO TO THAT ROUTINE.

1500 006414 010046  
1501 006416 016600 000002  
1502 006422 005740  
1503 006424 111000  
1504 006426 006300  
1505 006430 016000 006450  
1506 006434 000200

STRAP: MOV R0, -(SP) ;: SAVE R0  
MOV 2(SP), R0 ;: GET TRAP ADDRESS  
TST -(R0) ;: BACKUP BY 2  
MOV R0, (R0), R0 ;: GET RIGHT BYTE OF TRAP  
ASL R0 ;: POSITION FOR INDEXING  
MOV STRAP(R0), R0 ;: INDEX TO TABLE  
RTS R0 ;: GO TO ROUTINE

:: THIS IS USE TO HANDLE THE "GETPRI" MACRO

1511 006436 011646  
1512 006440 016666 000004 000002  
1513 006446 000002

STRAP2: MOV (SP), -(SP) ;: MOVE THE PC DOWN  
MOV 4(SP), 2(SP) ;: MOVE THE PSM DOWN  
RTI ;: RESTORE THE PSM

.SBTTL TRAP TABLE

: THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED  
: BY THE "TRAP" INSTRUCTION.

1521  
1522 006450 006436  
1523 006452 004414  
1524  
1525  
1526 006454 005144  
1527 006456 005264  
1528 006458 005384  
1529 006460 005504  
1530 006462 005624  
1531 006464 005744  
1532 006470 007262  
1533 006472 007382  
1534 006474 007502  
1535 006476 007622  
1536 006478 007742  
1537 006480 007862  
1538 006482 007982  
1539 006484 008102  
1540 006486 008222  
1541 006488 008342  
1542 006490 008462  
1543 006492 008582  
1544 006494 008702  
1545 006496 008822  
1546 006498 008942  
1547 006500 009062

ROUTINE  
STRPAD: WORD STRAP2 ;: CALL=TYPE TRAP+1(10W101) TTY TYPEOUT ROUTINE  
STYPE ;: CALL=TYPE  
SROCHR ;: CALL=SROCHR TRAP+2(10W102) TTY TYPEIN CHARACTER ROUTINE  
SROLIN ;: CALL=SROLIN TRAP+3(10W103) TTY TYPEIN STRING ROUTINE  
SROCT ;: CALL=SROCT TRAP+4(10W104) SEND AN OCTAL NUMBER FROM TTY  
SROST ;: CALL=SROST TRAP+5(10W105) CALL TO LOOP ON CURRENT DATA HANDLER  
SROV ;: CALL=SROV TRAP+6(10W106)  
SROV ;: CALL=SROV TRAP+7(10W107) CALL TO REGISTER SOME ROUTINE  
SROV ;: CALL=SROV TRAP+8(10W108) CALL TO REGISTER RESTORE ROUTINE  
SROV ;: CALL=SROV TRAP+9(10W109)  
SROV ;: CALL=SROV TRAP+10(10W110) CALL TO ISSUE A MASTER CLEAR  
SROV ;: CALL=SROV TRAP+11(10W111) CALL TO DELAY  
SROV ;: CALL=SROV TRAP+12(10W112) CALL TO CLOCK ROM ONCE  
SROV ;: CALL=SROV TRAP+13(10W113) CALL TO CLOCK DATA  
SROV ;: CALL=SROV TRAP+14(10W114) CALL TO DELAY A CLOCK TICK

1537	006502	005724			SINPUT	::CALL=INPUT	TRAP+15(104415)	CALL TO OCTAL & INPUT ROUTINE
1538	006504	006164			.CNVRT	::CALL=CNVRT	TRAP+16(104416)	CALL TO .....
1539	006506	006170			.CNVRT	::CALL=CNVRT	TRAP+17(104417)	CALL TO .....
1540	006510	006060			.ADVANCE	::CALL=ADVANCE	TRAP+20(104420)	CALL TO ADVANCE TO NEXT TEST
1541								
1542								
1543								
1544								
1545								
1546								
1547	006512	004737	011212		SERROR:	JSR	PC,CKSWR	CHECK FOR SOFT SWR
1548	006516	032777	010000	172514		BIT	BSW12,BSWR	BELL ON ERROR?
1549	006524	001406				BEG	XBX	BR IF NO BELL
1550	006526	105777	172516			TSTB	BSSTPS	TTY READY.
1551	006532	100003				BPL	XBX	DON'T WAIT IF TTY NOT READY.
1552	006534	112777	000207	172510		MOVB	BS207,BSSTPB	PUSH A BELL AT THE TTY.
1553	006542	032777	020000	172470	XBX:	BIT	BSW13,BSWR	DELETE ERROR PRINT OUT?
1554	006550	001107				BNE	HALTS	BR IF NO PRINT OUT WANTED.
1555	006552	021637	001216			CHP	(SP),SERRPC	WAS THIS ERROR FOUND LAST TIME?
1556	006554	001407				BEG	IS	BR IF YES
1557	006560	011637	001216			MOV	(SP),SERRPC	RECORD BEING HERE
1558	006564	105037	001203			CLRB	SERFLG	PREPARE HEADER
1559	006570	104406			IS:	SAVOS		SAVE ALL PROC REGISTERS
1560	006572	011605				MOV	(SP),R5	GET THE PC OF ERROR
1561	006574	162705	000002			SUB	R5,R5	GET ADDRESS OF TRAP CALL
1562	006580	011504				MOV	(R5),R7	GET ERROR INSTRUCTION
1563	006602	110437	001214			MOVB	R7,BSITENB	COPY ERROR & FOR APT HANDLING
1564	006606	006304				RSI	R7	HALT BY TWO
1565	006610	061504				ROO	(R5),R7	DOUBLE IT
1566	006612	006304				RSI	R7	HALT AGAIN
1567	006614	042704	177001			BIC	BS177001,R7	CLEAR JUNK
1568	006620	042704	001512			ROO	BS000001,R7	GET COUNTER
1569	006624	012437	006740			MOV	(R7)+,ERRMSG	GET ERROR MESSAGE
1570	006630	012437	006752			MOV	(R7)+,DATAHD	GET DATA HEADER
1571	006634	011437	006764			MOV	(R7)+,DATATB	GET DATA TABLE
1572	006640	105737	001203			TSTB	SERFLG	TYPE MESSAGE
1573	006644	001403				BEG	TYPMSG	BR IF YES
1574	006646	005737	006764			TST	DATATB	DOES DATA TABLE EXIST?
1575	006652	001040				BNE	TYPDAT	BR IF YES.
1576	006654	104401	001313		TYPMSG:	TYPE	,SCRLF	
1577	006660	104401	001313			TYPE	,SCRLF	
1578	006664	005737	001444			TST	LOCK	
1579	006670	001402				BEG	IS	
1580	006672	104401	010015			TYPE	,NASTEX	
1581	006676	104401	010003		IS:	TYPE	,NTSTN	
1582	006702	104417	007120			CHVRT	,XTSTN	SHOW IT
1583	006706	104401	010072			TYPE	,ERRPC	TYPE PC.
1584	006712	104417	007112			CHVRT	,ERTABO	SHOW IT
1585	006716	104401	001313			TYPE	,SCRLF	GIVE A CR/LF
1586	006722	112737	177777	001203		MOVB	B-1,SERFLG	NO MORE HEADER UNLESS NO DATA TABLE.
1587	006730	005737	006740			TST	ERRMSG	IS THERE AN ERROR MESSAGE?
1588	006734	001402				BEG	WRKO.FM	BR IF NO.
1589	006736	104401				TYPE		ERROR MESSAGE
1590	006740	000000			ERRMSG: 0			
1591	006742				WRKO.FM:			
1592	006742	005737	006752			TST	DATATB	DATA HEADER?



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1649 007176 000776          BR      .-2          ;;HANG UP
1650
1651
1652          ;;*****
1653          :POWER UP ROUTINE
1654 007200 012737 007316 000024 $PMRUP: MOV      $SILLUP,$PMRVEC  ;;SET FOR FAST DOWN
1655 007206 013705 007322          $SSAVR6,$SP  ;;GET SP
1656 007212 005037 007322          CLR      $SSAVR6  ;;WAIT LOOP FOR THE TTY
1657 007216 005237 007322          IS:    INC      $SSAVR6  ;;WAIT FOR THE INC
1658 007222 001375          BNE     IS        ;;OF WORD
1659 007224 104401 007562          TYPE   ,MFAIL
1660 007230 104417 007324          CHVRT  ,PFTAB
1661 007234 105037 001203          CLRAB  $ERRFLG  ;;CLEAR ERROR FLAG.
1662 007240 005037 001216          CLR    $ERRPC  ;;CLEAR LAST ERROR PC
1663 007244 013701 002066          MOV    $KNCSTR,$R1  ;;RESTORE DEVICE ADDRESS
1664 007250 005011          CLR    ($R1)      ;;CLEAR THE CSR.
1665 007252 104410          MSTCLR
1666 007254 012677 171760          MOV    ($SP)+,$R2  ;;POP STACK INTO $R2
1667 007260 012605          MOV    ($SP)+,$R3  ;;POP STACK INTO $R3
1668 007262 012604          MOV    ($SP)+,$R4  ;;POP STACK INTO $R4
1669 007264 012603          MOV    ($SP)+,$R5  ;;POP STACK INTO $R5
1670 007266 012602          MOV    ($SP)+,$R6  ;;POP STACK INTO $R6
1671 007270 012601          MOV    ($SP)+,$R7  ;;POP STACK INTO $R7
1672 007272 012600          MOV    ($SP)+,$R8  ;;POP STACK INTO $R8
1673 007274 012737 007126 000024          MOV    $KNDON,$PMRVEC  ;;SET UP THE POWER DOWN VECTOR
1674 007302 012737 000340 000026          MOV    $340,$PMRVEC+2  ;;PTR0:
1675 007310 104401          TYPE   ,MFAIL  ;;REPORT THE POWER FAILURE
1676 007312 007562          $PMRNG: .WORD  MFAIL  ;;POWER FAIL MESSAGE POINTER
1677 007314 000002          RTI
1678 007316 000000          $SILLUP: HALT
1679 007320 000776          BR      .-2
1680 007322 000000          $SSAVR6: 0  ;;PUT THE SP HERE
1681
1682 007324 000001          PFTAB: 1
1683 007326 003 002          .BYTE  3,2
1684 007330 001202          $15TNM
1685
1686 007332          .DELAY:
1687 007332 012777 000020 172534          MOV    #20,$KMP04
1688 007340 104412          ROMCLK 121111  ;;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1689 007344 121111          IS:    ;;POKE CLOCK DELAY BIT
1690 007344 104412          ROMCLK 121224  ;;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1691 007346 121224          BIT    #BIT4,$KMP04  ;;PORT4=IBUS#11
1692 007350 032777 000020 172516          BEQ    IS        ;;IS CLOCK BIT SET?
1693 007356 001772          IS:    BR      IF NO
1694 007360 000002          RTI
1695
1696 007362          .MSTCLR:
1697 007362 152777 000100 172500          B1SB  #BIT6,$KMCSTRH  ;;SET MASTER CLEAR
1698 007370 142777 000300 172472          B1CB  #BIT6!BIT7,$KMCSTRH  ;;CLEAR MASTER CLEAR AND RUN
1699 007376 000002          RTI  ;;RETURN
1700
1701 007400          .ROMCLK:
1702 007400 152777 000002 172462          B1SB  #BIT1,$KMCSTRH  ;;SET ROMI
1703 007406 013677 172464          MOV    #1($SP)+,$KMP06  ;;LOAD INSTRUCTION IN SEL6
1704 007412 062746 000002          ADD    #2,-($SP)  ;;ADJUST STACK

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POWER DOWN AND UP ROUTINES

1705	007416	032777	000100	171614		BTF	#SM06,ASHR	HALT IF SM06 =1
1706	007424	001401				BEQ	15	OR IF SM06 =0
1707	007426	000000				HALT		HALT BEFORE CLOCKING INSTRUCTION
1708	007430	152777	000003	172432	1S:	BTSB	#BIT1!BIT0,AKMSAH	CLOCK INSTRUCTION
1709	007436	142777	000007	172424		BICB	#BIT2!BIT1!BIT0,AKMSRH	CLEAR ROM0, ROM1, STEP
1710	007444	000002				RTI		
1711								
1712	007446							
1713	007446	013637	011106			MOV	2(SP)+TEMP	PUT TICK COUNT IN TEMP
1714	007452	062746	000002			ADD	2,-(SP)	ADJUST STACK
1715	007456	152777	000020	172404	1S:	BTSB	#BIT4,AKMSRH	SET STEP LU
1716	007464	027777	000020	172374		CMF	AKMSRH,AKMSRH	WASTE TIME
1717	007472	142777	000020	172370		BICB	#BIT4,AKMSRH	CLEAR STEP LU
1718	007500	005337	011106			DEC	TEMP	DEC TICK COUNT
1719	007504	001364				BNE	15	OR IF NOT DONE
1720	007506	000002				RTI		RETURN
1721	007510	000001			3S:		.BLKM 1	
1722								
1723	007512							
1724	007512	013637	011106			MOV	2(SP)+TEMP	MOVE COUNT TO TEMP
1725	007516	062746	000002			ADD	2,-(SP)	ADJUST STACK
1726	007522				1S:			
1727	007522	104412				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1728	007524	021364				OR	PORT4+IBUS# REG11	
1729	007526	032777	000002	172340		BTF	#2,AKMPO4	IS ROM CLOCK BIT CLEAR?
1730	007534	001772				BNE	15	OR IF YES
1731	007536				2S:			
1732	007536	104412				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1733	007540	021364				OR	PORT4+IBUS# REG11	
1734	007542	032777	000002	172324		BTF	#2,AKMPO4	IS ROM CLOCK BIT SET?
1735	007550	001372				BNE	25	OR IF YES
1736	007552	005337	011106			DEC	TEMP	DEC COUNT
1737	007556	001361				BNE	15	OR IF NOT DONE
1738	007560	000002				RTI		RETURN
1739								
1740	007562	050200	051127	043040		MPFAIL:	.ASC12	<200>/MPR FAILED, RESTART AT TEST /
(2)	007620	042600	042116	050040		MPASS:	.ASC14	<200>/END PASS DZXCC /
(2)	007642	051200	000			MP:	.ASC12	<200>/ /
(2)	007645	200	047516	042040		MPNO:	.ASC14	<200>/NO DEVICES PRESENT./
(2)	007672	044600	051516	043126		MPNO3:	.ASC12	<200>/INSUFFICIENT DATA! /
(2)	007716	046200	041517	040113		MPLOCK:	.ASC12	<200>/LOCK ON SELECTED TEST /
(2)	007736	100	041129	040029		MPNO:	.ASC14	/ /
(2)	007753	126	041606	040072		MPVEX:	.ASC12	/VEC: /
(2)	007761	120	051601	042523		MPASX:	.ASC12	/PASSES: /
(2)	007772	051106	047522	051522		MPERR:	.ASC12	/ERRORS: /
(2)	010006	124	051506	020124		MPSTN:	.ASC14	/TEST NO: /
(2)	010015	063	000			MPWSTK:	.ASC14	/ /
(2)	010017	200	042523	020124		MPMEM:	.ASC12	<200>/SET SWITCH REG TO KMC11'S DESIRED ACTIVE. /
(2)	010072	041520	020072	000		MPERRPC:	.ASC12	/PC: /
(2)	010077	200	020040	020040		MPHEAD:	.ASC11	<200>/ /
(2)	010126	020200	020040	020040			.ASC11	<200>/ /
(2)	010175	200	020040				.ASC11	<200>/ PC CSR STAT1 STAT2 STAT3 /
(2)	010247	200	026455				.ASC12	<200>/ /
(2)	010223	200	047510			NUM:	.ASC12	<200>/HOW MANY KMC11'S TO BE TESTED? /
(2)	010263	200	051503				.ASC12	<200>/CSR ADDRESS? /
(2)	010401	200	042526				.ASC12	<200>/VECTOR ADDRESS? /

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POWER DOWN AND UP ROUTINES

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(2) 010422 041200 020122 051120 PRIO: .ASCIZ <200>/BR PRIORITY LEVEL? (4,5,6,7)?/
(2) 010461 200 044127 041511 MODU: .ASCIZ <200>/WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202 TYP
(2) 010573 200 053523 052111 LINE: .ASCIZ <200>/SWITCH PAC#1 (OCCUP LINE #)?/
(2) 010631 200 053523 052111 BR: .ASCIZ <200>/SWITCH PAC#2 (.Y873 BOOT ADD)?/
(2) 010671 200 051511 052040 CONN: .ASCIZ <200>/IS THE LOOP BALK CONNECTOR ON?/
(2) 010731 200 047516 042040 NOACT: .ASCIZ <200>/NO DEVICES ARE SELECTED/
(2) 010762 100200 046513 030503 CONERR: .ASCIZ <200><200>/KMC11 AT NONSTANDARD ADDRESS PC: /
(2) 011027 200 054105 042520 CNERR: .ASCIZ <210>/EXPECTED FOUND/
(2) 011050 024040 046513 024503 KMCN: .ASCIZ / (KMC) /
(2) 011060 000005 .EVEN
(2) 011062 006 003 XSTATQ: 5
1741 011064 001276 .BYTE 6,3
1742 011066 006 003 $TMP0
1743 011070 001300 .BYTE 6,3
1744 011072 006 003 $TMP1
1745 011074 001302 .BYTE 6,3
1746 011076 006 003 $TMP2
1747 011100 001304 .BYTE 6,3
1748 011102 006 002 $TMP3
1749 011104 001306 .BYTE 6,2
1750 $TMP4
1751 .EVEN
1752 ;BUFFERS FOR INPUT-OUTPUT
1753
1754
1755 011106 000000 TEMP: 0
1756 011150 .=. +40
1757 011150 000000 MDATA: 0
1758 011212 .=. +40
1759
1760
1761 ;ROUTINE USED TO CHANGE SOFTWARE SWITCH
1762 ;REGISTER USING THE CONSOLE TERMINAL
1763 -----
1764
1765 011212 022737 000176 001240 CKSWR: CMP #SMREG, SWR ; IS THE SOFT SWR BEING USED?
1766 011220 001075 BNE CKSWRS ; BR IF NO
1767 011222 132737 000001 001336 BITB #1, SWW ; IS IT RUNNING UNDER APT?
1768 011230 001071 BNE CKSWRS ; EXIT IF YES.
1769 011232 022777 000007 170006 CMP #7, #STKB ; WAS CTRL G TYPED? (7 BIT ASCII)
1770 011240 001404 BEQ IS ; BR IF YES
1771 011242 022777 000207 167776 CMP #207, #STKB ; WAS CTRL G TYPED? (8 BIT ASCII)
1772 011250 001061 BNE CKSWRS ; BR IF NO
1773 011252 010246 IS: MOV R2, -(SP) ; STORE R2
1774 011254 010346 MOV R3, -(SP) ; STORE R3
1775 011256 010446 MOV R4, -(SP) ; STORE R4
1776 011260 012737 177777 011416 MOV #-1, SWFLG ; SET SOFT TYPE OUT FLAG
1777 011262 005002 CKSWR1: CLR R2 ; CLEAR NEW SWR CONTENTS
1778 011270 012704 177777 MOV #-1, R4 ; SET FLAG TO ALL ONES
1779 011274 104401 005541 TYPE SWR ; TYPE "SWR"
1780 011300 104417 CKSWR2: CHVRT ; TYPE OUT PRESENT CONTENTS
1781 011302 011452 SOFTSW ; OF SOFT SWITCH REGISTER
1782 011304 104401 CKSWR3: TYPE SWNEW ; TYPE "NEW"
1783 011310 004737 CKSWR4: JSR PC, INCHAR ; GET RESPONSE
1784 011314 022703 000015 CMP #15, R3 ; WAS IT A CR?
1785 011320 001424 BEQ SS ; BR IF YES

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011460 005737 001470
011464 001004
011466 101401 010731
011472 000000
011474 000776
011476 000241
011500 006137 001500
011504 005537 001500
011510 002737 000004 001504
011516 002737 000010 001502
011524 002737 002300 001502
011532 001006
011534 012737 002100 001502
011542 012737 002302 001504
011550 033737 001500 001470
011556 001747
011560 013700 001502
011564 013702 001504
011570 012037 002056
011574 011037 002056
011600 042737 177000 002056
011606 012037 002050
011612 012037 002052
011616 012037 002054
011622 012237 001324
011626 012237 001212
011632 012700 000002
011636 013737 002056 002070
011644 005237 002070
011650 013737 002070 002072
011656 005237 002072
011662 013737 002072 002074
011670 000037 002074
011674 013737 002074 002076
011702 000037 002076
011706 013737 002056 002060
011714 000037 002060
011720 013737 002060 002062
011726 000037 002062
011732 013737 002062 002064
011740 000037 002064
011744 032737 000002 001446
011752 001447
011754
005737 000042
    
```

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ROUTINE USED TO "CYCLE" THROUGH UP TO 16 KMC11'S
THIS ROUTINE SETS UP THE CONTROL ADDRESS FOR THE DIAGNOSTIC
AND RUNS THE SPECIFIED KMC11'S. THIS ROUTINE MUST
BE RUN FIRST BEFORE ENTERING THE DIAGNOSTIC FOR THE
SETUP NECESSARY.

CYCLE: TST      KMACTV      ;ARE ANY KMC11'S TO BE TESTED?
        IS
        BNE
        TYPE      ,NOACT
        HALT
        BR
        CLC      .-2
        ROL
        RDC      RUN
        RDO      RUN
        RDO      #4,MILK
        RDO      #10,CREAM
        RDO      #01,MAP+200,CREAM
        CHP
        BNE
        MOV      #01,MAP,CREAM
        MOV      #CNT.MAP,MILK
        BIT
        BEQ
        MOV      CREAM,R0
        MOV      MILK,R2
        MOV      (R0)+,KMC1R
        MOV      (R0)+,KMAVEC
        BIC      #177000,KMAVEC
        MOV      (R0)+,STAT1
        MOV      (R0)+,STAT2
        MOV      (R0)+,STAT3
        MOV      (R2)+,PASS
        MOV      (R2)+,BERTTL
        MOV      #2,R0
        MOV      KMC1R,KMCSRH
        INC      KMCSRH
        MOV      KMCSRH,KMCTL
        INC      KMCTL
        MOV      KMCTL,KMPO4
        RDO      R0,KMPO4
        MOV      KMPO4,KMPO6
        RDC      R0,KMPO6

        ;KEEP GOING; NOT ALL TESTED FOR.
        ;RESET ADDRESS POINTER.
        ;RESET PASS COUNT POINTER
        ;IS THIS ONE ACTIVE?
        ;BR IF NO
        ;GET ADDRESS POINTER
        ;GET PASS COUNT POINTER
        ;LOAD SYSTEM CTRL. REG
        ;LOAD VECTOR
        ;CLEAR UNANTED BITS
        ;LOAD STAT1
        ;LOAD STAT2
        ;LOAD STAT3
        ;LOAD PASS COUNT
        ;LOAD ERROR COUNT
        ;SAVE CORE THIS WAY!

        ;PTY LVL
        ;TX VEC
        ;TX LVL

        ;IS TEST NO. SELECTED
        ;BR IF NO

        4S: TST      #SW01,STRTSW
        BEQ      7S
        TST      #42
    
```



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1879 011760 001044 BNE 7$ ;BR IF YES
1880 011762 104401 001313 TYPE ,SCLF
1881 011766 104415 INPUT
1882 011770 010003 MTSTN
1883 011772 000001 I
1884 011774 001000 I000
1885 011776 001202 $STNM
1886 012000 000 .BYTE
1887 012001 001 .BYTE
1888 012002 012700 013732 MOV #TST1,RO
1889 012006 022710 SS: CMP (PC)+,(RO) ;CMP FIRST WORD TO 12737
1890 012010 012737 MOV (PC)+,2(PC)+
1891 012012 001020 BNE 6$ ;BR IF NOT SAME
1892 012014 023760 001202 000002 CMP $STNM,2(RO) ;DOES $STNM MATCH?
1893 012022 001014 BNE 6$ ;BR IF NO
1894 012024 022760 001202 000004 CMP #STNM,4(RO) ;IS LAST WORD OK?
1895 012032 001010 BNE 6$ ;BR IF NO
1896 012034 010037 001206 MOV RO,$LPADR ;IT IS A LEGAL TEST SO DO IT
1897 012040 104401 007642 TYPE BR
1898 012044 042737 000002 001446 BIC #SMD1,STRSM
1899 012052 000412 BR 8$
1900 012054 005720 SS: TST (RO)+ ;POP RO
1901 012056 020027 034670 CMP RO,#LAST+10 ;AT END YET?
1902 012062 001351 BNE 5$ ;BR IF NO
1903 012064 104401 001312 TYPE $QUES ;YES ILLEGAL TEST NO.
1904 012070 000731 BR 4$ ;TRY AGAIN
1905
1906 012072 012737 013732 001206 7$: MOV #TST1,$LPADR ;PREPARE $LPADR ADDRESS
1907 012100 013701 002066 8$: MOV KMC11,R1 ;R1 = BASE KMC11 ADDRESS
1908 012104 000177 167076 JMP $LPADR ;GO START TESTING.
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:ROUTINE USED TO "AUTO SIZE" THE KMC11
:CSR AND VECTOR.
:NOTE: THE CSR MAY BE ANY WHERE IN THE FLOATING
:ADDRESS RANGE (16000:16400)
:AND THE VECTOR MAY BE ANY WHERE IN THE
:FLOATING VECTOR RANGE (300:770)

```

AUTO.SIZE:

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1919 012110 CSRMAP: RESET ;INSURE A BUS INIT.
1920 012110 000005 MOV #KN.MAP,R2 ;LOAD MAP POINTER.
1921 012112 012702 002100 CLR (R2)+ ;ZERO ENTIRE MAP
1922 012116 005022 IS: CMP #KN.END,R2 ;ALL DONE?
1923 012120 022702 002300 BNE 1$ ;BR IF NO
1924 012124 001374 CLR KNUM ;SET OCTAL NUMBER OF KMC11'S TO 0
1925 012126 005037 001472 MOV #KN.MAP,R2 ;R2 POINTS TO KMC MAP
1926 012132 012702 002100 CLR KMACTV ;CLEAR ACTIVE
1927 012136 005037 001470 BIT #SMD0,STRSM ;QUESTIONS?
1928 012142 032737 000001 001446 BNE .+6 ;BR IF YES
1929 012150 001002 JMP 7$ ;IF NO SKIP QUESTIONS
1930 012152 000137 012532 001306 MOV #1,$TMP4 ;START WITH 1
1931 012156 012737 000001 INPUT
1932 012164 104415 NUM
1933 012166 010323 I
1934 012170 000001 I

```

1935	012172	000020			16.		
1936	012174	001302			STMP2		
1937	012176	000			.BYTE	0	
1938	012177	001			.BYTE	1	
1939	012200	013737	001302	001472	MOV	STMP2,KMINUM	;KMINUM = HOW MANY
1940	012206	104401	001313	12S:	TYPE	,SCLF	;TYPE WHICH KMC IS BEING DONE
1941	012212	104416			CONVRT		;STMP4 IS WHICH KMC
1942	012214	013164			WHICH		
1943	012216	005237	001306		INC	STMP4	
1944	012218	104415			INPUT		
1945	012219	010363			CSR		
1946	012220	160000			160000		
1947	012220	164000			164000		
1948	012220	001304			STMP3		
1949	012224	000			.BYTE	0	
1950	012226	001			.BYTE	1	
1951	012226	013722	001304		MOV	STMP3,(R2)+	;STORE CSR IN MAP
1952	012226	104415			INPUT		
1953	012227	010401			VEC		
1954	012228	000000			0		
1955	012230	000776			776		
1956	012232	001304			STMP3		
1957	012234	000			.BYTE	0	
1958	012234	001			.BYTE	1	
1959	012236	013712	001304		MOV	STMP3,(R2)	;STORE VECTOR IN MAP
1960	012232	104401		10S:	TYPE		
1961	012234	010422			PRI0		;ASK WHAT BK LEVEL
1962	012236	004737	013456		JSR	PC,INTTY	;GET RESPONSE
1963	012272	022703	000024		CMP	#24,R3	
1964	012276	101014			BHI	50S	;BR IF LESS THAN 4
1965	012300	022703	000027		CMP	#27,R3	
1966	012304	103411			BLO	50S	;BR IF GREATER THAN 7
1967	012306	012704	000011		MOV	#11,R4	;R4 = NUMBER OF SHIFTS
1968	012312	005303			ASL	R3	;SHIFT R3 LEFT
1969	012314	005304			DEC	R4	;DEC SHIFT COUNT
1970	012316	001375			UNE	-4	;BR IF NOT DONE
1971	012320	042703	170777		BIC	#170777,R3	;BIC UNWANTED BITS
1972	012324	050312			BIS	R3,(R2)	;PUT BR LEVEL IN STATUS MAP
1973	012326	000403			BR	8S	;CONTINUE
1974	012330	104401		50S:	TYPE		
1975	012332	001312			SQUES		;RESPONSE IS OUT OF LIMITS
1976	012334	000752			BR	10S	;TRY AGAIN
1977	012336			8S:			
1978	012336			9S:			
1979	012336	104401		16S:	TYPE		
1980	012340	010461			MODU		;ASK WHICH LINE UNIT
1981	012342	004737	013456		JSR	PC,INTTY	;GET REPLY
1982	012346	022703	000021		CMP	#21,R3	; "1"
1983	012352	001417			BEQ	30S	
1984	012354	022703	000022		CMP	#22,R3	; "2"
1985	012360	001412			BEQ	31S	
1986	012362	022703	000116		CMP	#116,R3	; "N"
1987	012366	001403			BEQ	32S	
1988	012370	104401			TYPE		
1989	012372	001312			SQUES		;IF NOT A 1,2 OR N TYPE "?"
1990	012374	000760			BR	16S	;TRY AGAIN

POWER DOWN AND UP ROUTINES

```

1991 012376 052722 010000 32S: BIS #BIT12,(R2)+ ;SET BIT 12 IN STAT2 IF NO LU
1992 012402 022222          CMP (R2)+,(R2)+ ;POP OVER STAT2 AND STAT3
1993 012404 000445          BR 33S
1994 012406 052712 020000 31S: BIS #BIT13,(R2) ;SET BIT 13 IN STAT2 IF M8202
1995 012412 104401          TYPE
1996 012414 010671          CONN ;ASK IF LOOP-BACK IS ON
1997 012416 004737 013456 JSR PC,INTTY ;GET REPLY
1998 012422 022703 000131 CMP #131,R3 ;Y
1999 012424 001406          BEQ 17S
2000 012430 022703 000116 CMP #116,R3 ;N
2001 012434 001406          BEQ 18S
2002 012436 104401          TYPE
2003 012440 001312          SQUES ;IF NOT Y OR N TYPE ""
2004 012442 000763          BR 30S ;TRY AGAIN
2005 012444 052722 040000 17S: BIS #BIT14,(R2)+ ;TURNAROUND IS CONNECTED
2006 012450 000402          BR 19S
2007 012452 042722 040000 18S: BIC #BIT14,(R2)+ ;NO TURNAROUND
2008 012456          19S:
2009 012456 104415          INPUT
2010 012460 010573          LINE
2011 012462 000000          0
2012 012464 000377          377
2013 012466 0C1304          STMP3
2014 012470 000          .BYTE 0
2015 012471 001          .BYTE 1
2016 012472 113722 001304 MOVB STMP3,(R2)+ ;STORE SWITCH PAC IN MAP
2017 012476 104415          INPUT
2018 012500 010631          BR 0
2019 012502 000000          0
2020 012504 000377          377
2021 012506 0C1304          STMP3
2022 012510 000          .BYTE 0
2023 012511 001          .BYTE 1
2024 012512 113722 001304 MOVB STMP3,(R2)+ ;STORE SWITCH PAC IN MAP
2025 012516 052722          TST (R2)+ ;POP OVER STAT3
2026 012520 005337 001302 33S: DEC STMP2 ;DEC KMC COUNT
2027 012524 001230          BNE 12S ;BR IF MORE TO DO
2028 012526 000137 013064 JMP 13S ;CONTINUE
2029 012532 012701 160000 7S: MOV #160000,R1 ;SET FOR FIRST ADDRESS TO BE TESTED
2030 012536 012737 013156 000004 MOV #65,204 ;SET FOR NON-EXISTANT DEVICE TIME OUT
2031 012544 005011          CLR (R1) ;CLEAR SEL0
2032 012546 005711          TST (R1) ;IF KMC11 KMC SR S/B 0
2033 012550 001135          BNE 3S ;IF NO DEV ; TRAP TO 4. IF NO BIT 8 THEN NO KMC11
2034 012552 005061 000006 CLR 6(R1) ;CLEAR SEL6
2035 012556 005761 000006 TST 6(R1) ;IF KMC11 THEN KMC11 S/B =0!
2036 012562 001130          BNE 3S ;BR IF NOT KMC11
2037 012564 012711 002000 MOV #BIT10,(R1) ;SET ROM0
2038 012570 005061 000004 CLR 4(R1) ;CLEAR SEL4
2039 012574 012761 125252 000006 MOV #125252,6(R1) ;WRITE THIS TO SEL6
2040 012602 052711 020000 BIS #BIT13,(R1) ;WRITE IT!
2041 012606 022761 125252 000004 CMP #125252,4(R1) ;WAS IT WRITTEN?
2042 012614 001113          BNE 3S ;IF NO IT IS NOT CRAM
2043 ;AT THIS POINT IT IS ASSUMED THAT R1 HOLDS A KMC11 CSR ADDRESS.
2044 012616 21S:
2045 012616 010122 22S: MOV R1,(R2)+ ;STORE CSR IN CORE TABLE.
2046 012620 012711 001000 15S: MOV #BIT9,(R1) ;CLEAR LINE UNIT LOOP

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2047	012624	005061	000004		CLR	4(R1)	;	CLEAR PORT4	
2048	012630	012761	122113	000006	MOV	0122113,6(R1)	;	LOAD INSTRUCTION (CLR DTR)	
2049	012636	002711	000400		BIS	0018, (R1)	;	CLOCK INSTRUCTION	
2050	012642	012761	001254	000006	MOV	001254,6(R1)	;	LOAD INSTRUCTION	
2051	012648	002711	000400		BIS	0018, (R1)	;	CLOCK INSTRUCTION	
2052	012654	012761	000377	000004	CMPB	0377,4(R1)	;	IS IT ALL ONES?	
2053	012660	001003			BNE	+10	;	BR IF NO	
2054	012666	002712	010000		BIS	00112,(R2)	;	IF YES, NO LINE UNIT, SET STATUS BIT	
2055	012672	000436			BR	205			
2056	012678	002761	000002	000004	BIT	0011,4(R1)	;	IS SWITCH A ONE?	
2057	012700	001403			SEQ	+10	;	BR IF #0201	
2058	012706	002712	060000		BIS	00113!0114,(R2)	;	#0202 ASSUME CONNECTOR	
2059	012712	000437			BR	205	;	CONNECTOR (ON)	
2060	012718	002761	000010	000004	BIT	0013,4(R1)	;	IS HWDY SET	
2061	012724	001023			BNE	205	;	BR IF #0201 NO CONNECTOR (ON LINE)	
2062	012730	012761	000100	000004	MOV	0016,4(R1)	;	LOAD PORT4	
2063	012736	012761	122113	000006	MOV	0122113,6(R1)	;	LOAD INSTRUCTION	
2064	012742	002711	000400		BIS	0018, (R1)	;	CLOCK INSTRUCTION (SET DTR)	
2065	012748	012761	001254	000006	MOV	001254,6(R1)	;	LOAD INSTRUCTION	
2066	012754	002711	000400		BIS	0018, (R1)	;	CLOCK INSTRUCTION (READ MODEM REG)	
2067	012760	002761	000010	000004	BIT	0013,4(R1)	;	IS HWDY SET NOW?	
2068	012766	001402			BEQ	205	;	BR IF NO CONNECTOR	
2069	012772	002712	040000		BIS	00114,(R2)	;	SET STATUS BIT FOR CONNECTOR	
2070	012778	005728			TST	(R2)+	;	POP POINTER	
2071	012784	012761	021324	000006	205:	MOV	0021324,6(R1)	;	PUT INSTRUCTION IN PORT6
2072	012790	012711	001400		MOV	00119!0118, (R1)	;	PORT4+LU IS	
2073	013002	156122	000004		BISB	4(R1),(R2)+	;	STORE DDCP LINE # IN TABLE	
2074	013008	012761	021344	000006	MOV	0021344,6(R1)	;	PORT6+INSTRUCTION	
2075	013014	012711	001400		MOV	00118!0119, (R1)	;	CLOCK INSTR.	
2076	013020	156122	000004		BISB	4(R1),(R2)+	;	STORE #073 ADD IN TABLE	
2077	013026	005722			TST	(R2)+	;	POP OVER STAT3	
2078	013032	005011			CLR	(R1)	;	CLEAR N0M1	
2079	013038	005237	001472		INC	K0NUM	;	UPDATE DEVICE COUNTER	
2080	013044	002737	000020	001472	CMP	020,K0NUM	;	ARE MAX. NO. OF DEV FOUND?	
2081	013050	001410			BEQ	135	;	YES DON'T LOOK FOR ANY MORE.	
2082	013056	005011			CLR	(R1)	;	CLEAR BIT 10	
2083	013062	005061	000006		35:	CLR	6(R1)	;	CLEAR SEL 6
2084	013068	002701	000010		145:	ADD	010,R1	;	UPDATE CSR POINTER ADDRESS
2085	013074	022701	164000		CMP	0164000,R1			
2086	013080	001230			BNE	25	;	BR IF MORE ADDRESS TO CHECK.	
2087	013086	005037	001470		135:	CLR	K0ACTV		
2088	013092	005737	001472		TST	K0NUM	;	WERE ANY K0C11'S FOUND AT ALL?	
2089	013098	001423			BEQ	55	;	ERROR AUTO SIZER FOUND NO K0C11'S IN THIS SYS.	
2090	013104	013701	001472		MOV	K0NUM,R1			
2091	013110	010137	001476		MOV	R1,SAVNUM	;	SAVE NUMBER OF DEVICES	
2092	013116	000241			45:	CLC			
2093	013122	005137	001470		ROL	K0ACTV	;	GENERATE ACTIVE REGISTER OF DEVICES.	
2094	013128	005237	001470		INC	K0ACTV	;	SET THE BIT	
2095	013134	005301			DEC	R1			
2096	013140	001371			BNE	45	;	BR IF MORE TO GENERATE	
2097	013146	012737	000006	000004	MOV	06,004	;	RESTORE TRAP VECTOR	
2098	013152	013737	001470	001474	MOV	K0ACTV,SAVACT	;	SAVE ACTIVE REGISTER	
2099	013158	000137	013172		JMP	VECMAP	;	GO FIND THE VECTOR NOW.	
2100	013164	104401	007645		55:	TYPE	HERR2	;	NOTIFY OPR THAT NO K0C11'S FOUND.
2101	013170	005000			CLR	R0	;	MAKE DATA LIGHTS ZERO	
2102	013176	000000			HALT		;	STOP THE SHOW	

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2103 013154 000776          BR      -2          ;DISABLE CONT. SW.
2104 013156 012716 013052 6S:  MOV      014S,(SP) ;ENTERED BY NON-EXISTANT TIME-OUT.
2105 013162 000002          RTI          ;RETURN TO MAINSTREAM
2106
2107 013164 000001          WHICH: 1
2108 013166      002      002      .BYTE      2,2
2109 013170 001306          STMP4
2110
2111 013172 032737 000001 001446 VECMAP: BIT      @SM00,STRTSW
2112 013200 001114          BNE      5S
2113 013202 012737 000340 000022          MOV      @340,@022 ;SET IOT TRAP PRIO TO 7
2114 013210 012737 013364 000020          MOV      @4S,@020 ;SET IOT TRAP VECTOR
2115 013216 012702 002100          MOV      @K1.MAP,R2 ;K1: SOFTWARE POINTER
2116 013222 012700 000300          MOV      @300,R0 ;FLOATING VECTORS START HERE.
2117 013224 012701 000302          MOV      @302,R1 ;PC OF IOT INSTR.
2118 013226 010120          1S:  MOV      R1,(R0)+ ;START FILLING VECTOR AREA
2119 013234 012721 000004          MOV      @4,(R1)+ ;WITH .+2; IOT
2120 013240 022021          CMP      (R0)+,(R1)+ ;ADD 2 TO RD +R1
2121 013242 020127 001000          CMP      R1,@1000
2122 013246 101771          BLOS    1S ;BR IF MORE TO FILL
2123 013250 013737 001470 001276 2S:  MOV      @KACTV,STMP0 ;STORE TEMPORALLY
2124 013254 016037 001276          ROR      STMP0 ;BRING OUT A BIT
2125 013262 103063          BCC     5S ;BR IF ALL DONE
2126 013264 012704 000012          MOV      @12,R4 ;R4 IS INDEX REGISTER
2127 013270 016437 013442 177776          MOV      @R4,R4 ;SET PS TO 7
2128 013276 011201          MOV      @R4,R1
2129 013300 012761 000200 000004          MOV      @200,4(R1)
2130 013306 012711 001000          MOV      @10,(R1) ;SET BOM1
2131 013312 012761 121111 000006          MOV      @121111,6(R1) ;PUT INSTRUCTION IN PORT6
2132 013320 012711 001400          MOV      @121111,6(R1) ;FORCE AN INTERRUPT
2133 013324 105200          7S:  INCB    RD ;STILL
2134 013326 001376          SUB     -2 ;FOR TIME TO INTERRUPT
2135 013330 162704 000002          SUB     @2,R4 ;GET NEXT LOWEST PS LEVEL
2136 013334 001404          BNE     7S ;BR IF R4 = 0
2137 013336 016437 013442 177776          MOV      @R4,R4 ;MOVE NEXT LOWER LEVEL IN F.
2138 013344 000767          BR     7S ;BR TO DELAY
2139 013346 052762 005300 000002 6S:  BIT      @300,2(R2) ;NO INTERRUPT ASSUME 300 AT LEVEL 5 AND FIX KMC1! LATER
2140 013354 005011          3S:  CLR      (R1) ;CLEAR BOM1
2141 013356 062702 000010          ADD     @10,R2 ;POP SOFTWARE POINTER
2142 013362 000735          BR     2S ;KEEP GOING
2143 013364 051662 000002          BIT      (SP),2(R2) ;GET VECTOR ADDRESS
2144 013370 042762 000007 000002 4S:  BIC     @7,2(R2) ;SET VECTOR ADDRESS
2145 013376 016405 013444          MOV      @R4,R5 ;CLEAR JUNK
2146 013402 006305          RSL     R5 ;GET BR LEVEL OF KMC11
2147 013404 006305          RSL     R5 ;SHIFT LEVEL 4 PLACES
2148 013406 006305          RSL     R5 ;TO THE LEFT FOR THE
2149 013410 006305          RSL     R5 ;STATUS TABLE
2150 013412 042705 170777          BIC     @170777,R5 ;CLEAR UNWANTED BITS
2151 013416 050562 000002          BIT      @5,2(R2) ;PUT BR LEVEL IN STATUS TABLE
2152 013422 022626          CMP      (SP)+,(SP)+ ;POP IOT JUNK OFF STACK
2153 013424 012716 013354          MOV      @3S,(SP) ;SET FOR RETURN
2154 013430 000002          RTI
2155 013432 012737 004134 000020 5S:  MOV      @SSCOPE,@020 ;RESTORE SCOPE VECTOR
2156 013440 000207          RTS      PC ;ALL DONE WITH "AUTO SIZING"
2157
2158 013442 000000          BRLVL: PRO ;LEVEL 0

```

POWER DOWN AND UP ROUTINES

2159	013444	000000		PRO	;	LEVEL 0	
2160	013446	000200		PR4	;	LEVEL 4	
2161	013450	000240		PR5	;	LEVEL 5	
2162	013452	000300		PR6	;	LEVEL 6	
2163	013454	000340		PR7	;	LEVEL 7	
2164							
2165							
2166	013456	105777	165562	INTTY: TSTB	2STKS		;WAIT FOR DONE
2167	013462	100375		BPL	-4		
2168	013464	017703	165556	MOV	2STKB,R3		;PUT CHAR IN R3
2169	013470	105777	165554	TSTB	2STPS		;WAIT UNTIL PRINTER IS READY
2170	013474	100375		BPL	-4		
2171	013476	010377	165550	MOV	R3 2STPS		;ECHO CHAR
2172	013502	042703	000240	BIC	#BIT7:BITS,R3		;MASK OFF LOWER CASE
2173	013506	000207		RTS	PC		;RETURN
2174							
2175	013510			APT.SIZE:			
2176	013510	000005		RESET			
2177	013512	010046		MOV	R0,-(SP)		.....PUSH R0 ON STACK
2178	013514	010146		MOV	R1,-(SP)		.....PUSH R1 ON STACK
2179	013516	010246		MOV	R2,-(SP)		.....PUSH R2 ON STACK
2180	013520	010346		MOV	R3,-(SP)		.....PUSH R3 ON STACK
2181	013520	005037	013724	CLR	VECTR		.....CLEAR THE LOCAL VARIABLE
2182	013520	005137	013730	CLR	PRIORITY		.....CLEAR UP LOCAL VARIABLE
2183	013520	013700	001376	MOV	DDOXM,R0		.....GET THE DEVICE COUNT
2184	013536	010037	001476	MOV	R0,DDOXM		.....SAVE THE NO. OF DEVICES
2185	013542	012701	001346	MOV	DDOXM,R1		.....GET EXTRA INFO, BITS POINTER
2186	013546	013737	001372	MOV	DDOXM,R2		.....GET BASE CSR ADDRESS
2187	013554	113737	001366	MOV	DDOXM,R3		.....GET THE VECTOR
2188	013562	113737	001367	MOV	DDOXM,R1		.....GET THE PRIORITY
2189	013570	013737	001374	MOV	DDOXM,R0		.....SAVE THE IOP'S SELECTED ACTIVE
2190	013576	013737	001470	MOV	DDOXM,R0		.....SAVE THE ACTIVE REGISTER
2191	013604	012702	001402	MOV	DDOXM,R0		.....GET ADDRESS OF FIRST DEVICE DESCRIPTOR WORD
2192	013610	012703	002100	MOV	DDOXM,R3		.....GET POINTER TO DEVICE MAP
2193	013614	005023		CLR	(R3)+		.....CLEAR DEVICE MAP
2194	013616	022713	002300	CMP	DDOXM,R3		.....IS WHOLE DEV MAP CLEARED?
2195	013622	003774		BGT	3\$		.....NO, THEN GO ON
2196	013624	012703	002100	MOV	DDOXM,R3		.....RESTORE DEV MAP POINTER.
2197	013630	013723	013726	MOV	BASE,(R3)+		.....LOAD CSR ADDRESS
2198	013634	112163	000001	MOV	(R1)+,1(R3)		.....GET EXTRA INFO, BITS
2199	013640	006213		ASR	(R3)		.....SET IT IN RIGHT POSITION.
2200	013642	006213		ASR	(R3)		.....SET IT IN RIGHT POSITION.
2201	013644	053713	013730	BIS	PRIORITY,(R3)		.....SET PRIORITY IN STAT1
2202	013650	006313		ASL	(R3)		.....SET THEM IN RIGHT POSITION
2203	013652	006313		ASL	(R3)		.....
2204	013654	006313		ASL	(R3)		.....
2205	013656	006313		ASL	(R3)		.....
2206	013660	053723	013724	BIS	VECTR,(R3)+		.....GET THE VECTOR IN STAT1.
2207	013664	012223		MOV	(R2)+,(R3)+		.....GET THE STAT2 FROM DDOXM
2208	013666	005723		TST	(R3)+		.....SKIP OVER STAT3
2209	013670	005300		DEC	R0		.....COUNT BY 1
2210	013672	001407		BEQ	2\$		.....ALL DONE?
2211	013674	062737	000010	ADD	#10,BASE		.....INCREMENT BASE CSR ADDRESS BY 10
2212	013702	062737	000010	ADD	#10,VECTR		.....INCREMENT VECTOR ADDRESS BY 10
2213	013710	000747		BR	1\$		.....SET THE NEXT MAP ENTRY
2214	013712						

```

2215 013712 012603      MOV      (SP)+,R3      ;; POP STACK INTO R3
2216 013714 012602      MOV      (SP)+,R2      ;; POP STACK INTO R2
2217 013716 012601      MOV      (SP)+,R1      ;; POP STACK INTO R1
2218 013720 012600      MOV      (SP)+,R0      ;; POP STACK INTO R0
2219 013722 000207      RTS       PC           ;; RETURN
2220 013724 000000      VECTR:   .WORD      0
2221 013726 000000      BASE:    .WORD      0
2222 013730 000000      PRTY:    .WORD      0

```

```

***** TEST 1 *****
*VERIFY THAT REFERENCING UNIBUS DEVICE REGISTERS
*DOES NOT CAUSE A TIME OUT TRAP
*****

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```

; TEST 1
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2233 013732 000004      ;*****
2234 013734 012737 000001 001202 1ST1: SCOPE      ;LOAD THE NO. OF THIS TEST
2235 013742 012737 014042 001442      MOV      #1,ST1M      ;POINT TO THE START OF NEXT TEST.
2236 013750 012737 014002 001444      MOV      #1$,LOCK     ;ADDRESS FOR LOCK ON DATA.
2237                                ;R1 CONTAINS BASE KMC11 ADDRESS
2238 013756 013701 002066      MOV      KMC11,R1     ;R1 CONTAINS BASE KMC11 ADDRESS
2239 013762 012700 000004      MOV      #4,R0        ;4 REGISTERS TO BE TESTED
2240 013766 012737 014034 000004      MOV      #4,4         ;SET UP TIME-OUT TRAP
2241 013774 012737 000340 000006      MOV      #340,6       ;LEVEL 7
2242 014002 005711 1$: TST      (R1)      ;REFERENCE DEVICE REGISTER
2243 014004 000240      NOP
2244 014006 104405      SCOPI
2245 014010 062701 000002      ADD      #2,R1        ;SM09=1?
2246 014014 005300      DEC      R0           ;NEXT REGISTER
2247 014016 001371      BNE     1$           ;DEC REGISTER COUNT
2248 014020 012737 000006 000004      MOV      #6,4        ;BR IF NOT LAST REGISTER
2249 014026 005037 000006      CLR      6           ;RESTORE LOC 4
2250 014032 104420      ADVANCE 6           ;RESTORE LOC 6
2251 014034 011632 2$: MOV      (SP),R2     ;ADVANCE TO NEXT TEST
2252 014036 104001      ERROR   1           ;GET PC OF TRAP
2253 014040 000002      RTI              ;TIME-OUT ERROR

```

```

***** TEST 2 *****
*VERIFY THAT RUN CAN BE CLEARED
*****

```

```

; TEST 2
-----

```

```

2263 014042 000004      ;*****
2264 014044 012737 000002 001202 1ST2: SCOPE      ;LOAD THE NO. OF THIS TEST
2265 014052 012737 014072 001442      MOV      #2,ST2M      ;POINT TO THE START OF NEXT TEST.
2266                                ;R1 CONTAINS BASE KMC11 ADDRESS
2267 014060 005011      CLR      (R1)        ;CLEAR KMC11
2268 014062 005005      CLR      R5         ;CLEAR "EXPECTED"
2269 014064 011104      MOV      (R1),R4     ;PUT KMC11 IN "FOUND"
2270 014066 001401      BEQ     1$         ;BR IF CLEARED

```

2271 014070 104002  
2272 014072

15: ERROR 2 ;ERROR KMCSR NOT CLEARED

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2326

014072 000004  
014074 012737 000003 001202  
014102 012737 014222 001442  
014110 012737 014124 001444  
  
014116 104410  
014120 012700 000001  
014124 005011  
014126 010005  
014130 010011  
014132 011104  
014134 020504  
014136 001401  
014140 104002  
014142 104405  
014144 005721  
014146 005200  
014150 022700 000005  
014154 001363  
014156 013701 002066  
014162 012700 000001  
014166 012737 014174 001444  
014174 010005  
014176 011104  
014200 020504  
014202 001401  
014204 104002  
014206 104405  
014210 005721  
014212 005200  
014214 022700 000005  
014220 001365

\*\*\*\*\* TEST 3 \*\*\*\*\*  
#UNIBUS REGISTER WORD DUAL ADDRESSING TEST  
#LOAD ALL REGISTERS WITH INCREMENTING PATTERN  
#READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING  
\*\*\*\*\*

TEST 3

1ST3: SCOPE  
MOV #3,ST3NH ; LOAD THE NO. OF THIS TEST  
MOV #ST34,NEXT ; POINT TO THE START OF NEXT TEST.  
MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.  
  
R1 CONTAINS BASE KMC11 ADDRESS  
MASTER CLEAR KMC11  
START PATTERN AT 1  
CLEAR REGISTER  
PUT DATA IN "EXPECTED"  
WRITE KMC REGISTER WITH PATTERN  
READ KMC REGISTER INTO "FOUND"  
IS DATA CORRECT  
BR IF YES  
DATA ERROR  
SCOPE 1  
NEXT REGISTER  
INCREMENT DATA PATTERN  
LAST REGISTER?  
BR IF NO  
BASE KMC11 ADDRESS TO R1  
RESTART PATTERN AT 1  
NEW SCOPE 1  
PUT DATA IN "EXPECTED"  
READ KMC REGISTER INTO "FOUND"  
IS DATA CORRECT  
BR IF YES  
DUAL ADDRESSING ERROR  
SCOPE 1  
NEXT REGISTER  
INCREMENT PATTERN  
LAST REGISTER?  
BR IF NO

\*\*\*\*\* TEST 4 \*\*\*\*\*  
#CONTROL STATUS REGISTER WRITE/READ TEST  
#SET BIT0, VERIFY BIT0 WAS SET  
#CLEAR BIT0, VERIFY BIT0 WAS CLEARED  
\*\*\*\*\*

TEST 4

\*\*\*\*\*



KMC11 UNIBUS REGISTER TESTS

```

2327 014222 000004          TST4: SCOPE
2328 014224 012737 000004 001202  MOV    #4,STSTNM          ; LOAD THE NO. OF THIS TEST
2329 014232 012737 014320 001442  MOV    #TST5,NEXT        ; POINT TO THE START OF NEXT TEST.
2330 014240 012737 014250 001444  MOV    #18,LOCK          ; ADDRESS FOR LOCK ON DATA.
2331 014246 104410          MSTCLR          ; MASTER CLEAR KMC11
2332 014250 013701 002066          15:  MOV    KMC1R,R1          ; PUT REGISTER ADDRESS IN R1
2333 014254 012705 000001          MOV    #BIT0,R5          ; PUT DATA IN "EXPECTED"
2334 014260 010511          MOV    R5,(R1)          ; WRITE BIT 0
2335 014262 011104          MOV    (R1),R4          ; READ CONTROL STATUS REGISTER
2336 014264 020504          CMP    R5,R4            ; IS DATA CORRECT
2337 014266 001401          BEQ    #0,2             ; BR IF YES
2338 014270 104002          ERROR 2                ; DATA ERROR
2339 014272 104405          25:  SCOPI
2340 014274 012737 014302 001444  MOV    #35,LOCK          ; NEW SCOPI
2341 014302 042711 000001          35:  BIC    #BIT0,(R1)        ; CLEAR BIT 0
2342 014306 005005          CLR    R5                ; CLEAR "EXPECTED"
2343 014310 011104          MOV    (R1),R4          ; READ CONTROL STATUS REGISTER
2344 014312 001402          BEQ    #4,2             ; BR IF ZERO
2345 014314 104002          ERROR 2                ; DATA ERROR BIT0 NOT CLEARED
2346 014316 104405          45:  SCOPI
2347 014320

```

```

***** TEST 5 *****
*CONTROL STATUS REGISTER WRITE/READ TEST
*SET BIT1, VERIFY BIT1 WAS SET
*CLEAR BIT1, VERIFY BIT1 WAS CLEARED
*****

```

TEST 5

```

2351
2352
2353
2354
2355
2356
2357
2358
2359 014320 000004          TST5: SCOPE
2360 014322 012737 000005 001202  MOV    #5,STSTNM          ; LOAD THE NO. OF THIS TEST
2361 014330 012737 014316 001442  MOV    #TST6,NEXT        ; POINT TO THE START OF NEXT TEST.
2362 014336 012737 014346 001444  MOV    #18,LOCK          ; ADDRESS FOR LOCK ON DATA.
2363 014344 104410          MSTCLR          ; MASTER CLEAR KMC11
2364 014346 013701 002066          15:  MOV    KMC1R,R1          ; PUT REGISTER ADDRESS IN R1
2365 014352 012705 000002          MOV    #BIT1,R5          ; PUT DATA IN "EXPECTED"
2366 014356 010511          MOV    R5,(R1)          ; WRITE BIT 1
2367 014360 011104          MOV    (R1),R4          ; READ CONTROL STATUS REGISTER
2368 014362 020504          CMP    R5,R4            ; IS DATA CORRECT
2369 014364 001401          BEQ    #0,2             ; BR IF YES
2370 014366 104002          ERROR 2                ; DATA ERROR
2371 014370 104405          25:  SCOPI
2372 014372 012737 014400 001444  MOV    #35,LOCK          ; NEW SCOPI
2373 014400 042711 000002          35:  BIC    #BIT1,(R1)        ; CLEAR BIT 1
2374 014404 005005          CLR    R5                ; CLEAR "EXPECTED"
2375 014406 011104          MOV    (R1),R4          ; READ CONTROL STATUS REGISTER
2376 014410 001402          BEQ    #4,2             ; BR IF ZERO
2377 014412 104002          ERROR 2                ; DATA ERROR BIT1 NOT CLEARED
2378 014414 104405          45:  SCOPI
2379 014416

```

```

***** TEST 6 *****

```

\*\*\*\*\*  
: #CONTROL STATUS REGISTER WRITE/READ TEST  
: #SET BIT2, VERIFY BIT2 WAS SET  
: #CLEAR BIT2, VERIFY BIT2 WAS CLEARED  
: \*\*\*\*\*

TEST 6

2383  
2384  
2385  
2386  
2387  
2388  
2389  
2390  
2391 014416 000004  
2392 014420 012737 000006 001202  
2393 014426 012737 014514 001442  
2394 014434 012737 014444 001444  
2395 014442 104410  
2396 014444 013701 002066  
2397 014450 012705 000004  
2398 014452 010511  
2399 014456 011104  
2400 014460 020504  
2401 014462 001401  
2402 014464 104002  
2403 014466 104405  
2404 014470 012737 014476 001444  
2405 014476 042711 000004  
2406 014500 005005  
2407 014504 011104  
2408 014506 001402  
2409 014510 104002  
2410 014512 104405  
2411 014514

\*\*\*\*\*  
: TEST 6  
: \*\*\*\*\*  
: SCOPE  
: MOV #6,STSTNM ; LOAD THE NO. OF THIS TEST  
: MOV #1ST7,NEXT ; POINT TO THE START OF NEXT TEST.  
: MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.  
: MSTCLR ; MASTER CLEAR KMC11  
15: MOV KMC5R,R1 ; PUT REGISTER ADDRESS IN R1  
: MOV #BIT2,R5 ; PUT DATA IN "EXPECTED"  
: MOV R5,(R1) ; WRITE BIT 2  
: MOV (R1),R4 ; READ CONTROL STATUS REGISTER  
: CMP R5,R4 ; IS DATA CORRECT  
: BEQ 25 ; BR IF YES  
: ERROR 2 ; DATA ERROR  
25: SCOPE ; SMO9 UP?  
: MOV #35,LOCK ; NEW SCOPE  
35: BIC #BIT2,(R1) ; CLEAR BIT 2  
: CLR R5 ; CLEAR "EXPECTED"  
: MOV (R1),R4 ; READ CONTROL STATUS REGISTER  
: BEQ 45 ; BR IF ZERO  
: ERROR 2 ; DATA ERROR BIT2 NOT CLEARED  
45: SCOPE ; SMO9 UP?  
: \*\*\*\*\*

\*\*\*\*\* TEST 7 \*\*\*\*\*  
: #CONTROL STATUS REGISTER WRITE/READ TEST  
: #SET BITS, VERIFY BITS WAS SET  
: #CLEAR BITS, VERIFY BITS WAS CLEARED  
: \*\*\*\*\*

TEST 7

2412  
2413  
2414  
2415  
2416  
2417  
2418  
2419  
2420  
2421  
2422  
2423 014514 000004  
2424 014516 012737 000007 001202  
2425 014524 012737 014612 001442  
2426 014532 012737 014542 001444  
2427 014540 104410  
2428 014542 013701 002066  
2429 014546 012705 000040  
2430 014550 010511  
2431 014554 011104  
2432 014556 020504  
2433 014560 001401  
2434 014562 104002  
2435 014564 104405  
2436 014566 012737 014574 001444  
2437 014574 042711 000040  
2438 014600 005005

\*\*\*\*\*  
: TEST 7  
: \*\*\*\*\*  
: SCOPE  
: MOV #7,STSTNM ; LOAD THE NO. OF THIS TEST  
: MOV #1ST10,NEXT ; POINT TO THE START OF NEXT TEST.  
: MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.  
: MSTCLR ; MASTER CLEAR KMC11  
15: MOV KMC5R,R1 ; PUT REGISTER ADDRESS IN R1  
: MOV #BIT5,R5 ; PUT DATA IN "EXPECTED"  
: MOV R5,(R1) ; WRITE BIT 5  
: MOV (R1),R4 ; READ CONTROL STATUS REGISTER  
: CMP R5,R4 ; IS DATA CORRECT  
: BEQ 25 ; BR IF YES  
: ERROR 2 ; DATA ERROR  
25: SCOPE ; SMO9 UP?  
: MOV #35,LOCK ; NEW SCOPE  
35: BIC #BIT5,(R1) ; CLEAR BIT 5  
: CLR R5 ; CLEAR "EXPECTED"  
: \*\*\*\*\*

KMC11 UNIBUS REGISTER TESTS

2439 014602 011104  
2440 014604 001402  
2441 014606 104002  
2442 014610 104405  
2443 014612

MOV (R1),R4 ; READ CONTROL STATUS REGISTER  
BEQ 48 ; BR IF ZERO  
ERROR 2 ; DATA ERROR BITS NOT CLEARED  
SCOPI ; SMO9 UP?

48:

\*\*\*\*\* TEST 10 \*\*\*\*\*  
\*CONTROL STATUS REGISTER WRITE/READ TEST  
\*SET BIT6, VERIFY BIT6 WAS SET  
\*CLEAR BIT6, VERIFY BIT6 WAS CLEARED  
\*\*\*\*\*

TEST 10

2444 014612 000004  
2445 014614 012737 000010 001202  
2446 014622 012737 014710 001442  
2447 014630 012737 014640 001444  
2448 014636 104410  
2449 014640 013701 002066  
2450 014644 012705 000100  
2451 014650 010511  
2452 014652 011104  
2453 014654 020504  
2454 014656 001401  
2455 014660 104002  
2456 014662 104405  
2457 014664 012737 014672 001444  
2458 014672 042711 000100  
2459 014676 005005  
2460 014700 011104  
2461 014702 001402  
2462 014704 104002  
2463 014706 104405  
2464 014710

\*\*\*\*\*  
↑ST10: SCOPE ;  
MOV #10,STSTNM ; LOAD THE NO. OF THIS TEST  
MOV #ST11,NEXT ; POINT TO THE START OF NEXT TEST.  
MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.  
NSTCLR ; MASTER CLEAR KMC11  
18: MOV KNCSR,R1 ; PUT REGISTER ADDRESS IN R1  
MOV #BIT6,RS ; PUT DATA IN "EXPECTED"  
MOV RS,(R1) ; WRITE BIT 6  
MOV (R1),R4 ; READ CONTROL STATUS REGISTER  
CMP RS,R4 ; IS DATA CORRECT  
BEQ 28 ; BR IF YES  
ERROR 2 ; DATA ERROR  
SCOPI ; SMO9 UP?  
28: MOV #28,LOCK ; NEW SCOPI  
38: BIC #BIT6,(R1) ; CLEAR BIT 6  
CLR RS ; CLEAR "EXPECTED"  
MOV (R1),R4 ; READ CONTROL STATUS REGISTER  
BEQ 48 ; BR IF ZERO  
ERROR 2 ; DATA ERROR BIT6 NOT CLEARED  
SCOPI ; SMO9 UP?  
48:

\*\*\*\*\* TEST 11 \*\*\*\*\*  
\*CONTROL STATUS REGISTER WRITE/READ TEST  
\*SET BIT7, VERIFY BIT7 WAS SET  
\*CLEAR BIT7, VERIFY BIT7 WAS CLEARED  
\*\*\*\*\*

TEST 11

2465 014710 000004  
2466 014712 012737 000011 001202  
2467 014720 012737 015006 001442  
2468 014726 012737 014736 001444  
2469 014734 104410  
2470 014736 013701 002066  
2471 014742 012705 000200  
2472 014746 010511

\*\*\*\*\*  
↑ST11: SCOPE ;  
MOV #11,STSTNM ; LOAD THE NO. OF THIS TEST  
MOV #ST12,NEXT ; POINT TO THE START OF NEXT TEST.  
MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.  
NSTCLR ; MASTER CLEAR KMC11  
18: MOV KNCSR,R1 ; PUT REGISTER ADDRESS IN R1  
MOV #BIT7,RS ; PUT DATA IN "EXPECTED"  
MOV RS,(R1) ; WRITE BIT 7



KNC11 UNIBUS REGISTER TESTS

2570	015176	104002		
2571	015200	104405		
2572	015202			
2573				
2574				
2575				
2576				
2577				
2578				
2579				
2580				
2581				
2582				
2583	015202	000004		
2584	015204	012737	000014	001202
2585	015212	012737	015300	001442
2586	015220	012737	015230	001444
2587	015226	104410		
2588	015230	013701	002066	
2589	015234	012705	010000	
2590	015240	010511		
2591	015242	011104		
2592	015244	020504		
2593	015246	001401		
2594	015248	104002		
2595	015250	104405		
2596	015254	012737	015262	001444
2597	015262	042711	010000	
2598	015266	005005		
2599	015270	011104		
2600	015272	001402		
2601	015274	104002		
2602	015276	104405		
2603	015300			
2604				
2605				
2606				

```

TST13: SCOPE
        MOV      #13,STSTNM      ; LOAD THE NO. OF THIS TEST
        MOV      @STST14,NEXT    ; POINT TO THE START OF NEXT TEST.
        MOV      @R1,LOCK       ; ADDRESS FOR LOCK ON DATA.
        NSTCLR
15:     MOV      #KNC11,R1       ; MASTER CLEAR KNC11
        MOV      @R1,R5         ; PUT REGISTER ADDRESS IN R1
        MOV      #0,R5          ; PUT DATA IN "EXPECTED"
        MOV      (R1),R4        ; WRITE BIT 11
        MOV      (R1),R4        ; READ CONTROL STATUS REGISTER
        CMP      R5,R4          ; IS DATA CORRECT
        BEQ      25          ; BR IF YES
        ERROR   2              ; DATA ERROR
        SCOP1  25             ; SNOOZ UP
        MOV      #R35,LOCK
35:     BIC      @BIT11,(R1)     ; CLEAR BIT 11
        CLR      R5            ; CLEAR "EXPECTED"
        MOV      (R1),R4        ; READ CONTROL STATUS REGISTER
        BEQ      45            ; BR IF ZERO
        ERROR   2              ; DATA ERROR BIT11 NOT CLEARED
        SCOP1  45             ; SNOOZ UP
45:

```

```

;***** TEST 14 *****
;CONTROL STATUS REGISTER WRITE/READ TEST
;SET BIT12, VERIFY BIT12 WAS SET
;CLEAR BIT12, VERIFY BIT12 WAS CLEARED
;*****

```

TEST 14

2583	015202	000004		
2584	015204	012737	000014	001202
2585	015212	012737	015300	001442
2586	015220	012737	015230	001444
2587	015226	104410		
2588	015230	013701	002066	
2589	015234	012705	010000	
2590	015240	010511		
2591	015242	011104		
2592	015244	020504		
2593	015246	001401		
2594	015248	104002		
2595	015250	104405		
2596	015254	012737	015262	001444
2597	015262	042711	010000	
2598	015266	005005		
2599	015270	011104		
2600	015272	001402		
2601	015274	104002		
2602	015276	104405		
2603	015300			
2604				
2605				
2606				

```

TST14: SCOPE
        MOV      #14,STSTNM      ; LOAD THE NO. OF THIS TEST
        MOV      @STST15,NEXT    ; POINT TO THE START OF NEXT TEST.
        MOV      @R1,LOCK       ; ADDRESS FOR LOCK ON DATA.
        NSTCLR
15:     MOV      #KNC11,R1       ; MASTER CLEAR KNC11
        MOV      @R1,R5         ; PUT REGISTER ADDRESS IN R1
        MOV      #0,R5          ; PUT DATA IN "EXPECTED"
        MOV      (R1),R4        ; WRITE BIT 12
        MOV      (R1),R4        ; READ CONTROL STATUS REGISTER
        CMP      R5,R4          ; IS DATA CORRECT
        BEQ      25          ; BR IF YES
        ERROR   2              ; DATA ERROR
        SCOP1  25             ; SNOOZ UP
        MOV      #R35,LOCK
25:     BIC      @BIT12,(R1)     ; CLEAR BIT 12
        CLR      R5            ; CLEAR "EXPECTED"
        MOV      (R1),R4        ; READ CONTROL STATUS REGISTER
        BEQ      45            ; BR IF ZERO
        ERROR   2              ; DATA ERROR BIT12 NOT CLEARED
        SCOP1  45             ; SNOOZ UP
45:

```

```

;***** TEST 15 *****

```

KMC11 UNIBUS REGISTER TESTS

2607  
2608  
2609  
2610  
2611  
2612  
2613  
2614  
2615  
2616  
2617  
2618  
2619  
2620  
2621  
2622  
2623  
2624  
2625  
2626  
2627  
2628  
2629  
2630  
2631  
2632  
2633  
2634  
2635  
2636  
2637  
2638  
2639  
2640  
2641  
2642  
2643  
2644  
2645  
2646  
2647  
2648  
2649  
2650  
2651  
2652  
2653  
2654  
2655  
2656  
2657  
2658  
2659  
2660  
2661  
2662

```
015300 000004
015302 012737 000015 001202
015310 012737 015376 001442
015316 012737 015326 001444
015324 104410
015326 013701 002072
015332 012705 000001
015336 010511
015340 011104
015342 020504
015344 001401
015346 104002
015350 104405
015352 012737 015360 001444
015360 042711 000001
015364 005005
015366 011104
015370 001402
015372 104002
015374 104405
015376
```

```
*CONTROL OUT REGISTER WRITE/READ TEST
*SET BIT0, VERIFY BIT0 WAS SET
*CLEAR BIT0, VERIFY BIT0 WAS CLEARED
*****
```

TEST 15

```
*****
TST15: SCOPE
MOV #15,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST16,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
1$: MOV KMC1L,R1 ; PUT REGISTER ADDRESS IN R1
MOV #BIT0,R5 ; PUT DATA IN "EXPECTED"
MOV R5,(R1) ; WRITE BIT 0
MOV (R1),R4 ; READ CONTROL OUT REGISTER
CMP R5,R4 ; IS DATA CORRECT
BEQ 2$ ; BR IF YES
ERROR 2 ; DATA ERROR
SCOPI ; SNO9 UP?
2$: MOV #3$,LOCK ; NEW SCOPI
BIC #BIT0,(R1) ; CLEAR BIT 0
CLR R5 ; CLEAR "EXPECTED"
MOV (R1),R4 ; READ CONTROL OUT REGISTER
BEQ 4$ ; BR IF ZERO
ERROR 2 ; DATA ERROR BIT0 NOT CLEARED
SCOPI ; SNO9 UP?
4$:
```

```
***** TEST 16 *****
*CONTROL OUT REGISTER WRITE/READ TEST
*SET BIT1, VERIFY BIT1 WAS SET
*CLEAR BIT1, VERIFY BIT1 WAS CLEARED
*****
```

TEST 16

```
*****
TST16: SCOPE
MOV #16,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST17,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
MSTCLR ; MASTER CLEAR KMC11
1$: MOV KMC1L,R1 ; PUT REGISTER ADDRESS IN R1
MOV #BIT1,R5 ; PUT DATA IN "EXPECTED"
MOV R5,(R1) ; WRITE BIT 1
MOV (R1),R4 ; READ CONTROL OUT REGISTER
CMP R5,R4 ; IS DATA CORRECT
BEQ 2$ ; BR IF YES
ERROR 2 ; DATA ERROR
SCOPI ; SNO9 UP?
2$: MOV #3$,LOCK ; NEW SCOPI
BIC #BIT1,(R1) ; CLEAR BIT 1
CLR R5 ; CLEAR "EXPECTED"
```



```

2719 015632 011104      MOV      (R1),R4      ; READ CONTROL OUT REGISTER
2720 015634 020504      CMP      R5,R4       ; IS DATA CORRECT
2721 015636 001401      BEQ     28           ; BR IF YES
2722 015640 104002      ERROR   2           ; DATA ERROR
2723 015642 104405      SCOPI   ; SMO9 UP?
2724 015644 012737 015652 001444 28:  MOV     #35,LOCK     ; NEW SCOPI
2725 015652 042711 000100 38:  BIC     #BIT6,(R1)   ; CLEAR BIT 6
2726 015656 005005      CLR     R5          ; CLEAR "EXPECTED"
2727 015660 011104      MOV     (R1),R4     ; READ CONTROL OUT REGISTER
2728 015662 001402      BEQ     48           ; BR IF ZERO
2729 015664 104002      ERROR   2           ; DATA ERROR BIT6 NOT CLEARED
2730 015666 104405      SCOPI   ; SMO9 UP?
2731 015670      48:

```

```

;***** TEST 21 *****
;CONTROL OUT REGISTER WRITE/READ TEST
;SET BIT7, VERIFY BIT7 WAS SET
;CLEAR BIT7, VERIFY BIT7 WAS CLEARED
;*****

```

TEST 21

```

2740      ;
2741      ;-----
2742      ;*****
2743 015670 000004      *T21: SCOPE
2744 015672 012737 000021 001202  MOV     #21,STSTNM ; LOAD THE NO. OF THIS TEST
2745 015700 012737 015766 001442  MOV     #T22,NEXT  ; POINT TO THE START OF NEXT TEST.
2746 015706 012737 015716 001444  MOV     #18,LOCK   ; ADDRESS FOR LOCK ON DATA.
2747 015714 104410      HSTCLR ; MASTER CLEAR KMC11
2748 015716 013701 002072      18:  MOV     KMC1L,R1   ; PUT REGISTER ADDRESS IN R1
2749 015722 012705 000200  MOV     #BIT7,R5   ; PUT DATA IN "EXPECTED"
2750 015726 010511      MOV     R5,(R1)   ; WRITE BIT 7
2751 015730 011104      MOV     (R1),R4   ; READ CONTROL OUT REGISTER
2752 015732 020504      CMP     R5,R4     ; IS DATA CORRECT?
2753 015734 001401      BEQ     28        ; BR IF YES
2754 015736 104002      ERROR   2        ; DATA ERROR
2755 015740 104405      SCOPI   ; SMO9 UP?
2756 015742 012737 015750 001444 28:  MOV     #35,LOCK   ; NEW SCOPI
2757 015750 042711 000200 38:  BIC     #BIT7,(R1) ; CLEAR BIT 7
2758 015754 005005      CLR     R5        ; CLEAR "EXPECTED"
2759 015756 011104      MOV     (R1),R4   ; READ CONTROL OUT REGISTER
2760 015760 001402      BEQ     48        ; BR IF ZERO
2761 015762 104002      ERROR   2        ; DATA ERROR BIT7 NOT CLEARED
2762 015764 104405      SCOPI   ; SMO9 UP?
2763      48:

```

```

;***** TEST 22 *****
;CONTROL OUT REGISTER WRITE/READ TEST
;SET BIT12, VERIFY BIT12 WAS SET
;CLEAR BIT12, VERIFY BIT12 WAS CLEARED
;*****

```

TEST 22

```

2764
2765
2766
2767
2768
2769
2770
2771
2772
2773
2774 ;*****

```



KMC11 UNIBUS REGISTER TESTS

2775	015766	000004		
2776	015770	012737	000022	001202
2777	015776	012737	016064	001442
2778	016004	012737	016014	001444
2779	016012	104410		
2780	016014	013701	002072	
2781	016020	012705	010000	
2782	016024	010511		
2783	016026	011104		
2784	016030	020504		
2785	016032	001401		
2786	016034	104002		
2787	016036	104405		
2788	016040	012737	016046	001444
2789	016046	042711	010000	
2790	016052	005005		
2791	016054	011104		
2792	016056	001402		
2793	016060	104002		
2794	016062	104405		
2795	016064			

```

TST22: SCOPE
MOV #22,STSTNM
MOV #TST23,NEXT
MOV #18,LOCK
MSTCLR
1S: MOV KMC1L,R1
MOV #BIT12,RS
MOV RS,(R1)
MOV (R1),R4
CMP RS,R4
BEQ ERROR
EOR R4,R4
SCOPI
MOV #38,LOCK
BIC #BIT12,(R1)
CLR RS
MOV (R1),R4
BEQ 4S
ERROR 2
SCOPI
4S:

```

```

: LOAD THE NO. OF THIS TEST
: POINT TO THE START OF NEXT TEST.
: ADDRESS FOR LOCK ON DATA.
: MASTER CLEAR KMC11
: PUT REGISTER ADDRESS IN R1
: PUT DATA IN "EXPECTED"
: WRITE BIT 12
: READ CONTROL OUT REGISTER
: IS DATA CORRECT
: OR IF YES
: DATA ERROR
: STOP UP?
: NEW SCOPI
: CLEAR BIT 12
: CLEAR "EXPECTED"
: READ CONTROL OUT REGISTER
: OR IF ZERO
: DATA ERROR BIT12 NOT CLEARED
: STOP UP?

```

```

:***** TEST 23 *****
:CONTROL OUT REGISTER WRITE/READ TEST
:SET BIT13, VERIFY BIT13 WAS SET
:CLEAR BIT13, VERIFY BIT13 WAS CLEARED
:*****

```

TEST 23

2807	016064	000004		
2808	016066	012737	000023	001202
2809	016074	012737	016162	001442
2810	016102	012737	016112	001444
2811	016110	104410		
2812	016112	013701	002072	
2813	016116	012705	020000	
2814	016122	010511		
2815	016124	011104		
2816	016126	020504		
2817	016130	001401		
2818	016132	104002		
2819	016134	104405		
2820	016136	012737	016144	001444
2821	016144	042711	020000	
2822	016150	005005		
2823	016152	011104		
2824	016154	001402		
2825	016156	104002		
2826	016160	104405		
2827	016162			
2828				
2829				
2830				

```

TST23: SCOPE
MOV #23,STSTNM
MOV #TST24,NEXT
MOV #18,LOCK
MSTCLR
1S: MOV KMC1L,R1
MOV #BIT13,RS
MOV RS,(R1)
MOV (R1),R4
CMP RS,R4
BEQ ERROR
EOR R4,R4
SCOPI
MOV #38,LOCK
BIC #BIT13,(R1)
CLR RS
MOV (R1),R4
BEQ 4S
ERROR 2
SCOPI
4S:

```

```

: LOAD THE NO. OF THIS TEST
: POINT TO THE START OF NEXT TEST.
: ADDRESS FOR LOCK ON DATA.
: MASTER CLEAR KMC11
: PUT REGISTER ADDRESS IN R1
: PUT DATA IN "EXPECTED"
: WRITE BIT 13
: READ CONTROL OUT REGISTER
: IS DATA CORRECT
: OR IF YES
: DATA ERROR
: STOP UP?
: NEW SCOPI
: CLEAR BIT 13
: CLEAR "EXPECTED"
: READ CONTROL OUT REGISTER
: OR IF ZERO
: DATA ERROR BIT13 NOT CLEARED
: STOP UP?

```

```

:***** TEST 24 *****

```

KNC11 UNIBUS REGISTER TESTS

2831  
2832  
2833  
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2886

016162 000004  
016164 012737 000024 001202  
016172 012737 016306 001442  
016200 012737 016220 001444  
016206 104410  
016210 013701 002074  
016214 012700 000001  
016220  
016220 010005  
016220 010511  
016224 011104  
016226 020504  
016230 001401  
016232 104002  
016234 104405  
016236 000241  
016240 006100  
016242 001366  
016244 012737 016256 001444  
016246 012700 000001  
016256  
016256 005100  
016260 010005  
016262 010511  
016264 011104  
016266 020504  
016270 001401  
016272 104002  
016274 104405  
016276 005100  
016300 000241  
016302 006100  
016304 001364

```

: #PORT4 REGISTER WRITE/READ TEST
: #FLOAT A ONE THROUGH PORT4 REGISTER
: #FLOAT A ZERO THROUGH PORT4 REGISTER
: *****
:
: TEST 24
: -----
: *****
:
: ST24: SCOPE
: MOV #24,STSTNM ; LOAD THE NO. OF THIS TEST
: MOV #ST25,NEXT ; POINT TO THE START OF NEXT TEST.
: MOV #648,LOCK ; ADDRESS FOR LOCK ON DATA.
: *****
: MSTCLR ; MASTER CLEAR KNC11
: MOV KMP04,R1 ; PUT REGISTER ADDRESS IN R1
: MOV #1,R0 ; START WITH BIT0
:
: 648:
: MOV R0,R5 ; PUT "EXPECTED" IN R5
: MOV R5,(R1) ; WRITE PORT4 REGISTER
: MOV (R1),R4 ; READ PORT4 REGISTER
: CMP R5,R4 ; COMPARE EXPECTED AND FOUND
: BEQ 658 ; BR IF OK
: ERROR 2 ; WRITE/READ ERROR
: 658: SCOP1 ; LOOP TO 648 IF S109=1
: CLC ; CLEAR CARRY
: ROL R0 ; SHIFT TO NEXT BIT
: BNE 648 ; BR IF NOT DONE YET?
: MOV #668,LOCK ; NEW SCOP1
: MOV #1,R0 ; START WITH BIT0
:
: 668:
: COM R0 ; CHANGE TO A FLOATING ZERO
: MOV R0,R5 ; PUT "EXPECTED" IN R5
: MOV R5,(R1) ; WRITE PORT4 REGISTER
: MOV (R1),R4 ; READ PORT4 REGISTER
: CMP R5,R4 ; COMPARE EXPECTED AND FOUND
: BEQ 678 ; BR IF OK
: ERROR 2 ; WRITE/READ ERROR
: 678: SCOP1 ; LOOP TO 668 IF S109=1
: COM R0 ; CHANGE BACK TO A FLOATING ONE
: CLC ; CLEAR CARRY
: ROL R0 ; SHIFT TO NEXT BIT
: BNE 668 ; BR IF NOT DONE YET?

```

```

: ***** TEST 25 *****
: #PORT6 REGISTER WRITE/READ TEST
: #FLOAT A ONE THROUGH PORT6 REGISTER
: #FLOAT A ZERO THROUGH PORT6 REGISTER
: *****
:
: TEST 25
: -----
: *****
:
: ST25: SCOPE
: MOV #25,STSTNM ; LOAD THE NO. OF THIS TEST
: MOV #ST26,NEXT ; POINT TO THE START OF NEXT TEST.
: MOV #648,LOCK ; ADDRESS FOR LOCK ON DATA.

```

KNC11 UNIBUS REGISTER TESTS

2887	016332	104410		
2888	016334	013701	002076	
2889	016340	012700	000001	
2890	016344			
2891	016344	010005		
2892	016346	010511		
2893	016346	011104		
2894	016348	020504		
2895	016354	001401		
2896	016356	104002		
2897	016356	104405		
2898	016362	000241		
2899	016364	006100		
2900	016366	001366		
2901	016370	012737	016402	001444
2902	016376	012700	000001	
2903	016402			
2904	016402	005100		
2905	016404	010005		
2906	016406	010511		
2907	016410	011104		
2908	016412	020504		
2909	016414	001401		
2910	016416	104002		
2911	016420	104405		
2912	016422	005100		
2913	016424	000241		
2914	016426	006100		
2915	016430	001366		

```

MSTCLR ;MASTER CLEAR KNC11
MOV KMP06,R1 ;PUT REGISTER ADDRESS IN R1
MOV #1,R0 ;START WITH BIT0

64S: MOV R0,RS ;PUT "EXPECTED" IN RS
MOV RS,(R1) ;WRITE PORT6 REGISTER
MOV (R1),R4 ;READ PORT6 REGISTER
CMP RS,R4 ;COMPARE EXPECTED AND FOUND
BEQ 65S ;BR IF OK
ERROR 2 ;WRITE/READ ERROR
LOOP TO 64S IF SMO9=1

65S: SCOP1 ;CLEAR CARRY
CLC ;SHIFT TO NEXT BIT
ROL R0 ;BR IF NOT DONE YET?
BNE 64S ;NEW SCOP1
MOV #66S,LOCK ;START WITH BIT0
MOV #1,R0

66S: COM R0 ;CHANGE TO A FLOATING ZERO
MOV R0,RS ;PUT "EXPECTED" IN RS
MOV RS,(R1) ;WRITE PORT6 REGISTER
MOV (R1),R4 ;READ PORT6 REGISTER
CMP RS,R4 ;COMPARE EXPECTED AND FOUND
BEQ 67S ;BR IF OK
ERROR 2 ;WRITE/READ ERROR
LOOP TO 66S IF SMO9=1

67S: COM R0 ;CHANGE BACK TO A FLOATING ONE
CLC ;CLEAR CARRY
ROL R0 ;SHIFT TO NEXT BIT
BNE 66S ;BR IF NOT DONE YET?

```

```

***** TEST 26 *****
UNIBUS REGISTER BYTE DUAL ADDRESSING TEST
LOAD ALL REGISTERS WITH INCREMENTING PATTERN
READ BACK ALL REGISTERS TO VERIFY CORRECT ADDRESSING
*****

```

TEST 26

2916	016432	000004		
2917	016434	012737	000026	001202
2918	016442	012737	016562	001442
2919	016450	012737	016464	001444
2920	016456	104410		
2921	016460	012700	000001	
2922	016464	105011		
2923	016466	110005		
2924	016470	110011		
2925	016472	111104		
2926	016474	020504		
2927	016476	001401		
2928	016500	104002		
2929	016502	104405		
2930	016504	105721		

```

tst26: SCOP1 ;*****
MOV #26,STSTN1 ;LOAD THE NO. OF THIS TEST
MOV #STST27,NEXT ;POINT TO THE START OF NEXT TEST.
MOV #18,LOCK ;ADDRESS FOR LOCK ON DATA.

15: MSTCLR ;R1 CONTAINS BASE KNC11 ADDRESS
MOV #1,R0 ;MASTER CLEAR KNC11
CLRB (R1) ;START PATTERN AT 1
MOV R0,RS ;CLEAR REGISTER
MOV (R1),R4 ;PUT DATA IN "EXPECTED"
MOV R0,(R1) ;WRITE KNC REGIS. R1 WITH PATTERN
MOV (R1),R4 ;READ KNC REGISTER INTO "FOUND"
CMP RS,R4 ;IS DATA CORRECT
BEQ 25 ;BR IF YES
ERROR 2 ;DATA ERROR
SCOP1 ;SMO9=1?
TSTB (R1)+ ;NEXT REGISTER

```

2943	016506	005200			INC	R0	INCREMENT DATA PATTERN
2944	016510	022700			CHP	#11,R0	LAST REGISTER?
2945	016514	001363	000011		BNE	18	BR IF NO
2946	016516	013701	002066		MOV	KMCSR,R1	BASE KMC11 ADDRESS TO R1
2947	016522	012700	000001		MOV	#1,R0	RESTART PATTERN AT 1
2948	016526	012737	016534	001444	MOV	#38,LOCK	NEW SCOPE
2949	016534	110005		35:	MOV	R0,R5	PUT DATA IN "EXPECTED"
2950	016536	111104			MOV	(R1),R4	READ KMC REGISTER INTO "FOUND"
2951	016540	020504			CHP	R5,R4	IS DATA CORRECT
2952	016542	001401			BEQ	48	BR IF YES
2953	016544	104002			ERROR	2	DUAL ADDRESSING ERROR
2954	016546	104405		45:	SCOPE		SMD9=1
2955	016550	105721			TSTB	(R1)+	NEXT REGISTER
2956	016552	005200			INC	R0	INCREMENT PATTERN
2957	016554	022700	000011		CHP	#11,R0	LAST REGISTER?
2958	016560	001365			BNE	38	BR IF NO

\*\*\*\*\* TEST 27 \*\*\*\*\*  
 MAINTENANCE INSTRUCTION REGISTER TEST  
 VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'  
 AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A BUS RESET.  
 \*\*\*\*\*

TEST 27

2970	016562	000004			TST27:	SCOPE	*****
2971	016564	012737	000027	001202	MOV	#27,\$STSNM	: LOAD THE NO. OF THIS TEST
2972	016572	012737	016722	001442	MOV	#TST30,NEXT	: POINT TO THE START OF NEXT TEST.
2973	016600	012737	016616	001444	MOV	#18,LOCK	: ADDRESS FOR LOCK ON DATA.
2974							: R1 CONTAINS BASE KMC11 ADDRESS
2975	016606	104410			MCCLR		MASTER CLEAR KMC11
2976	016610	012711	003000		MOV	#BIT9:BIT10,(R1)	: SELF IS NOW THE IR
2977	016614	005005			CLR	R5	PUT "EXPECTED" IN R5
2978	016616	010561	000006		MOV	R5,6(R1)	CLEAR THE IR
2979	016622	016104	000006		MOV	6(R1),R4	READ THE IR
2980	016626	020504			CHP	R5,R4	IS IT CLEARED?
2981	016630	001401			BEQ	28	BR IF YES
2982	016632	104023			ERROR	23	ERROR IR IS NOT CLEAR
2983	016634	104405		25:	SCOPE		LOOP TO 18 IF SMD9=1
2984	016636	012737	016650	001444	MOV	#38,LOCK	NEW SCOPE
2985	016644	012705	177777		MOV	#1,R5	PUT "EXPECTED" IN R5
2986	016650	010561	000006		MOV	R5,6(R1)	WRITE ALL ONES TO THE IR
2987	016654	016104	000006		MOV	6(R1),R4	READ THE IR
2988	016660	020504			CHP	R5,R4	IS IT ALL ONES?
2989	016662	001401			BEQ	48	BR IF YES
2990	016664	104023			ERROR	23	ERROR IR IS NOT = ALL ONES
2991	016666	104405		45:	SCOPE		LOOP TO 35 IF SMD9=1
2992	016670	012737	016700	001444	MOV	#58,LOCK	NEW SCOPE
2993	016676	005005			CLR	R5	PUT "EXPECTED" IN R5
2994	016700	000005			RESET		BUS RESET
2995	016702	012711	003000		MOV	#BIT9:BIT10,(R1)	: SELF IS IR
2996	016706	016104	000006		MOV	6(R1),R4	READ THE IR
2997	016712	020504			CHP	R5,R4	IS IT CLEARED?
2998	016714	001401			BEQ	68	BR IF YES

2999 016716 104023  
3000 016720 104405  
3001  
3002  
3003  
3004  
3005  
3006  
3007  
3008  
3009  
3010  
3011  
3012 016722 000004  
3013 016724 012737 000030 001202  
3014 016732 012737 017064 001442  
3015 016740 012737 016756 001444  
3016  
3017 016746 104410  
3018 016750 012711 003000  
3019 016754 005005  
3020 016756 010561 000006  
3021 016762 016104 000006  
3022 016766 020504  
3023 016770 001401  
3024 016772 104023  
3025 016774 104405  
3026 016776 012737 017010 001444  
3027 017004 012705 177777  
3028 017010 010561 000006  
3029 017014 016104 000006  
3030 017020 020504  
3031 017022 001401  
3032 017024 104023  
3033 017026 104405  
3034 017030 012737 017040 001444  
3035 017036 005005  
3036 017040 052711 040000  
3037 017071 012711 003000  
3038 017080 016104 000006  
3039 017084 020504  
3040 017086 001401  
3041 017060 104023  
3042 017062 104405  
3043  
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3051  
3052  
3053  
3054

65: ERROR 23 ;ERROR, IR IS NOT CLEARED  
SCOPI ;LOOP TO 55 IF SMO9=1

\*\*\*\*\* TEST 30 \*\*\*\*\*  
#MAINTENANCE INSTRUCTION REGISTER TEST  
#VERIFY THAT THE MAINT IR CAN BE WRITTEN TO ALL ZEROS'  
#AND ALL ONES'. VERIFY THAT IT IS CLEARED ON A MASTER RESET.  
\*\*\*\*\*

TEST 30

-----  
:\*\*\*\*\*  
:†ST30: SCOPE  
:MOV #30,STSTNM ; LOAD THE NO. OF THIS TEST  
:MOV #STST31,NEXT ; POINT TO THE START OF NEXT TEST.  
:MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.  
:R1 CONTAINS BASE KMC11 ADDRESS  
:MASTER CLEAR KMC11  
:SEL6 IS NOW THE IR  
:PUT "EXPECTED" IN RS  
15: CLR R5 ; CLEAR THE IR  
:MOV R5,6(R1) ; READ THE IR  
:CMP R5,R4 ; AS IT CLEARED?  
:BEQ 25 ; BR IF YES  
:ERROR 23 ; ERROR IR IS NOT CLEAR  
:SCOPI ; LOOP TO 15 IF SMO9=1  
:MOV #35,LOCK ; NEW SCOPE  
:MOV #-1,R5 ; PUT "EXPECTED" IN RS  
35: MOV R5,6(R1) ; WRITE ALL ONES TO THE IR  
:MOV R5,R4 ; READ THE IR  
:CMP R5,R4 ; IS IT ALL ONES?  
:BEQ 45 ; BR IF YES  
:ERROR 23 ; ERROR IR IS NOT = ALL ONES  
45: SCOPI ; LOOP TO 35 IF SMO9=1  
:MOV #55,LOCK ; NEW SCOPE  
:CLR R5 ; PUT "EXPECTED" IN RS  
55: BIS #BIT14,(R1) ; MASTER CLEAR  
:MOV #BIT9:BIT10,(R1) ; SEL6 IS IR  
:MOV R5,R4 ; READ THE IR  
:CMP R5,R4 ; IS IT CLEARED?  
:BEQ 65 ; BR IF YES  
:ERROR 23 ; ERROR, IR IS NOT CLEARED  
65: SCOPI ; LOOP TO 55 IF SMO9=1  
:\*\*\*\*\*

\*\*\*\*\* TEST 31 \*\*\*\*\*  
#MICRO PROCESSOR TEST  
#LOAD KMP06 WITH A MICRO-PROCESSOR INSTRUCTION, CLOCK IT  
#VERIFY INSTRUCTION EXECUTED PROPERLY  
#INSTRUCTION SHOULD MOVE IBUS#4 TO IBUS#5, IBUS#4 IS ALL 1'S  
#AND IBUS#5 IS ALL 0'S. RESULT SHOULD BE ALL 1'S IN SEL4  
\*\*\*\*\*

TEST 31

```

3055 :*****
3056 017064 000004 1ST31: SCOPE
3057 017066 012737 000031 001202 MOV #31,STSNM ; LOAD THE NO. OF THIS TEST
3058 017074 012737 017150 001442 MOV #1ST32,NEXT ; POINT TO THE START OF NEXT TEST.
3059 ; R1 CONTAINS BASE KMC11 ADDRESS
3060 017102 104410 MSTCLR ; MASTER CLEAR KMC11
3061 017104 012761 000377 000004 MOV #377,4(R1) ; PORT4 HI-BYTE=0'S LO-BYTE=1'S
3062 017112 012711 001000 MOV #BIT9,(R1) ; SET ROMI
3063 017116 012761 121105 000006 MOV #121105,6(R1) ; INSTRUCTION TO PORT6
3064 017124 052711 C31400 BIS #BIT8:BIT9,(R1) ; CLK INSTRUCTION, MOVE IBUS#4 TO IBUS#5
3065 017130 000240 NOP
3066 017132 012705 177777 MOV #-1,R5 ; PUT "EXPECTED" IN R5
3067 017136 016104 000004 MOV 4(R1),R4 ; PUT "FOUND" INTO R4
3068 017142 020504 CNP R5,R4 ; IS DATA CORRECT
3069 017144 001401 BEQ 1$ ; OR IF YES
3070 017146 104003 ERROR 3 ; ERROR
3071 017150
3072
3073
3074 :***** TEST 32 *****
3075 ; MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
3076 ; FLOAT A I THROUGH IBUS* REGISTER 0
3077 ; FLOAT A 0 THROUGH IBUS* REGISTER 0
3078 :*****
3079
3080 ; TEST 32
3081 :-----
3082 :*****
3083 017150 000004 1ST32: SCOPE
3084 017152 012737 000032 001202 MOV #32,STSNM ; LOAD THE NO. OF THIS TEST
3085 017160 012737 017350 001442 MOV #1ST33,NEXT ; POINT TO THE START OF NEXT TEST.
3086 017166 012737 017206 001444 MOV #64$,LOCK ; ADDRESS FOR LOCK ON DATA.
3087 ; R1 CONTAINS BASE KMC11 ADDRESS
3088 017174 104410 MSTCLR ; MASTER CLEAR KMC11
3089 017176 012702 000000 MOV #0,R2 ; SAVE REGISTER ADDRESS FOR TYPEOUT
3090 017202 012700 000001 MOV #1,R0 ; START WITH BIT 0
3091 017206
3092 017206 010061 000004 64$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4
3093 017212 042761 000030 000004 BIC #30,4(R1) ; CLEAR UNWANTED BITS
3094 017220 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3095 017222 121100 121100:0 MOV DATA TO IBUS* REGISTER 0
3096 017224 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3097 017226 121005 121005:(0#20) READ FROM IBUS* REGISTER 0
3098 017230 010005 MOV R0,R5 ; PUT EXPECTED IN R5
3099 017232 042705 000030 BIC #30,R5 ; CLEAR UNWANTED BITS
3100 017236 116104 000005 MOV# 5(R1),R4 ; PUT "FOUND" INTO R4
3101 017242 120504 CNPB R5,R4 ; DATA CORRECT?
3102 017244 001401 BEQ 65$ ; OR IF YES
3103 017246 104004 ERROR 4 ; ERROR
3104 017250 104405 65$: SCOP1 ; SMO#-1?
3105 017252 000241 CLC ; CLEAR CARRY
3106 017254 106100 ROL# R0 ; SHIFT BIT IN R0
3107 017256 001353 BNE 64$ ; IF R0=0 THEN DONE
3108 017260 012737 017274 001444 MOV #67$,LOCK ; NEW SCOP1
3109 017266 012700 000001 MOV #1,R0 ; START WITH BIT 0
3110 017272 005100 69$: COM R0 ; CHANGE TO FLOATING ZERO

```

```

3111 017274          67$:
3112 017274 010061 000004      MOV    R0,4(R1)      ;PUT PATTERN INTO PORT4
3113 017300 042761 000030 000004      BIC    #30,4(R1)    ;CLEAR UNWANTED BITS
3114 017306 104412          ROMCLK  ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3115 017310 121100          121100!0      MOV    DATA TO IBUS* REGISTER 0
3116 017312 104412          ROMCLK  ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3117 017314 121005!<0#20>      READ FROM IBUS* REGISTER 0
3118 017316 010005          MOV    R0,R5        ;PUT EXPECTED IN R5
3119 017320 042705 000030      BIC    #30,R5       ;CLEAR UNWANTED BITS
3120 017324 116104 000005      MOV    S(R1),R4     ;PUT "FOUND" INTO R4
3121 017330 120504          CMP    R5,R4        ;DATA CORRECT?
3122 017332 001401          BEQ    #68$        ;BR IF YES
3123 017334 104004          ERROR  4           ;ERROR
3124 017336 104405          68$: SCOP1      ;SND=1?
3125 017340 005100          COM    R0           ;CHANGE TO FLOATING 1
3126 017342 000241          CLC                    ;CLEAR CARRY
3127 017344 106100          ROL    R0           ;SHIFT BIT IN R0
3128 017346 001351          BNE    #69$        ;IF R0=0 THEN DONE
3129
3130
3131          ;***** TEST 33 *****
3132          ;MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
3133          ;*FLOAT A 1 THROUGH IBUS* REGISTER 2
3134          ;*FLOAT A 0 THROUGH IBUS* REGISTER 2
3135          ;*****
3136
3137          ; TEST 33
3138          ;-----
3139          ;*****
3140 017350 000004      ;T33: SCOP
3141 017352 012737 000033 001202      MOV    #33,$ST33M   ;LOAD THE NO. OF THIS TEST
3142 017350 012737 017550 001442      MOV    $T33M,NEXT   ;POINT TO THE START OF NEXT TEST.
3143 017366 012737 017406 001444      MOV    #64$,$LOCK   ;ADDRESS FOR LOCK ON DATA.
3144          ;R1 CONTAINS BASE JMC11 ADDRESS
3145 017374 104410          MSTCLR ;MASTER CLEAR JMC11
3146 017376 012702 000002      MOV    #2,R2        ;SAVE REGISTER ADDRESS FOR TYPEOUT
3147 017402 012700 000001      MOV    #1,R0        ;START WITH BIT 0
3148 017406
3149 017406 010061 000004      64$: MOV    R0,4(R1)    ;PUT PATTERN INTO PORT4
3150 017412 042761 000070 000004      BIC    #70,4(R1)   ;CLEAR UNWANTED BITS
3151 017420 104412          ROMCLK  ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3152 017422 121102          121102!2      MOV    DATA TO IBUS* REGISTER 2
3153 017424 104412          ROMCLK  ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3154 017426 121005!<2#20>      READ FROM IBUS* REGISTER 2
3155 017430 010005          MOV    R0,R5        ;PUT EXPECTED IN R5
3156 017432 042705 000070      BIC    #70,R5       ;CLEAR UNWANTED BITS
3157 017436 116104 000005      MOV    S(R1),R4     ;PUT "FOUND" INTO R4
3158 017442 120504          CMP    R5,R4        ;DATA CORRECT?
3159 017444 001401          BEQ    #65$        ;BR IF YES
3160 017446 104004          ERROR  4           ;ERROR
3161 017450 104405          65$: SCOP1      ;SND=1?
3162 017452 000241          CLC                    ;CLEAR CARRY
3163 017454 106100          ROL    R0           ;SHIFT BIT IN R0
3164 017456 001353          BNE    #64$        ;IF R0=0 THEN DONE
3165 017460 012737 017474 001444      MOV    #67$,$LOCK   ;NEW SCOP1
3166 017466 012700 000001      MOV    #1,R0        ;START WITH BIT 0

```

```

3167 017472 005100 69$: COM R0 ;CHANGE TO FLOATING ZERO
3168 017474 000004 67$: MOV R0,4(R1) ;PUT PATTERN INTO PORT4
3169 017474 010061 000004 000004 BIC #70,4(R1) ;CLEAR UNWANTED BITS
3170 017500 042761 000070 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3171 017506 104412 121100:2 ;MOV DATA TO IBUS* REGISTER 2
3172 017510 121102 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3173 017512 104412 121005:(2*20) ;READ FROM IBUS* REGISTER 2
3174 017514 121055 MOV R0,R5 ;PUT EXPECTED IN R5
3175 017516 010005 BIC #70,R5 ;CLEAR UNWANTED BITS
3176 017520 042705 000070 000005 MOV# 5(R1),R4 ;PUT "FOUND" INTO R4
3177 017524 116104 CMPE R5,R4 ;DATA CORRECT?
3178 017530 120504 BEQ EE ;BR IF YES
3179 017532 001401 ERROR 4 ;ERROR
3180 017534 104004 68$: SCOPI ;SHOW=1?
3181 017536 104405 COM R0 ;CHANGE TO FLOATING 1
3182 017540 005100 CLC ;CLEAR CARRY
3183 017542 000241 ROLB R0 ;SHIFT BIT IN R0
3184 017544 106100 BNE 69$ ;IF R0=0 THEN DONE
3185 017546 001351

```

```

***** TEST 34 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
#FLOAT A 1 THROUGH IBUS* REGISTER 4
#FLOAT A 0 THROUGH IBUS* REGISTER 4
*****

```

TEST 34

```

3197 017550 000004 1$T34: SCOPE ;*****
3198 017552 012737 000034 001202 MOV #34,$TSTNM ;LOAD THE NO. OF THIS TEST
3199 017560 012737 017724 001442 MOV #1$T35,NEXT ;POINT TO THE START OF NEXT TEST.
3200 017566 012737 017606 001444 MOV #64$,$LOCK ;ADDRESS FOR LOCK ON DATA.
3201 017574 104410 ;R1 CONTAINS BASE KMC11 ADDRESS
3202 017576 012702 000004 ;MASTER CLEAR KMC11
3203 017602 012700 000001 ;SAVE REGISTER ADDRESS FOR TYPEOUT
3204 017606 010061 000004 64$: MOV R0,4(R1) ;START WITH BIT 0
3205 017612 104412 ROMCLK ;PUT PATTERN INTO PORT4
3206 017614 121104 121100:4 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3207 017616 104412 ROMCLK ;MOV DATA TO IBUS* REGISTER 4
3208 017620 121105:(4*20) ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3209 017622 010005 MOV R0,R5 ;READ FROM IBUS* REGISTER 4
3210 017624 116104 000005 MOV# 5(R1),R4 ;PUT EXPECTED IN R5
3211 017630 120504 CMPE R5,R4 ;PUT "FOUND" INTO R4
3212 017632 001401 BEQ 65$ ;DATA CORRECT?
3213 017634 104004 ERROR 4 ;BR IF YES
3214 017636 104405 65$: SCOPI ;ERROR
3215 017640 000241 CLC ;SHOW=1?
3216 017642 106100 ROLB R0 ;CLEAR CARRY
3217 017644 001350 BNE 64$ ;SHIFT BIT IN R0
3218 017646 012737 000001 001444 MOV #67$,$LOCK ;IF R0=0 THEN DONE
3219 017654 012700 000001 ;NEW SCOPI
3220 017660 005100 69$: COM R0 ;START WITH BIT 0
3221 ;CHANGE TO FLOATING ZERO
3222

```



```

3223 017662
3224 017663 010061 000004
3225 017666 104412
3226 017670 121104
3227 017672 104412
3228 017674 121105
3229 017676 010005
3230 017700 116104 000005
3231 017704 120504
3232 017706 001401
3233 017710 104004
3234 017712 104405
3235 017714 005100
3236 017716 000241
3237 017720 106100
3238 017722 001356
3239
3240
3241
3242
3243
3244
3245
3246
3247
3248
3249
3250 017724 000004
3251 017726 012737 000035 001202
3252 017734 012737 020100 001442
3253 017742 012737 017762 001444
3254
3255 017750 104410
3256 017752 012702 000005
3257 017756 012700 000001
3258 017762
3259 017762 010061 000004
3260 017766 104412
3261 017770 121105
3262 017772 104412
3263 017774 121125
3264 017776 010005
3265 020000 116104 000005
3266 020004 120504
3267 020006 001401
3268 020010 104004
3269 020012 104405
3270 020014 000241
3271 020016 106100
3272 020020 001360
3273 020022 012737 020036 001444
3274 020020 012700 000001
3275 020024 005100
3276 020026
3277 020026 010061 000004
3278 020042 104412

```

```

67$: MOV RO,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121100!4 ; MOV DATA TO IBUS* REGISTER 4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121005!(4*20) ; READ FROM IBUS* REGISTER 4
MOV RO,R5 ; PUT EXPECTED IN R5
MOVSB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 68$ ; BR IF YES
ERROR 4 ; ERROR
68$: SCOPI ; SMO=1?
COM RO ; CHANGE TO FLOATING 1
CLC ; CLEAR CARRY
ROLB RO ; SHIFT BIT IN RO
BNE 69$ ; IF RO=0 THEN DONE

```

```

***** TEST 35 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
#FLOAT A 1 THROUGH IBUS* REGISTER 5
#FLOAT A 0 THROUGH IBUS* REGISTER 5
*****

```

TEST 35

```

*****
TST35: SCOPE ;
MOV #35,$TSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST36,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #64$,$LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
; MASTER CLEAR KMC11
; SAVE REGISTER ADDRESS FOR TYPEOUT
; START WITH BIT 0
64$: MOV RO,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121100!5 ; MOV DATA TO IBUS* REGISTER 5
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121005!(5*20) ; READ FROM IBUS* REGISTER 5
MOV RO,R5 ; PUT EXPECTED IN R5
MOVSB 5(R1),R4 ; PUT "FOUND" INTO R4
CMPB R5,R4 ; DATA CORRECT?
BEQ 65$ ; BR IF YES
ERROR 4 ; ERROR
65$: SCOPI ; SMO=1?
CLC ; CLEAR CARRY
ROLB RO ; SHIFT BIT IN RO
BNE 64$ ; IF RO=0 THEN DONE
MOV #67$,$LOCK ; NEW SCOPI
MOV #1,$RO ; START WITH BIT 0
69$: COM RO ; CHANGE TO FLOATING ZERO
67$: MOV RO,4(R1) ; PUT PATTERN INTO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

KMC11 MICRO PROCESSOR IBUS\* TESTS

```

3279 020044 121105          121100:5          ;MOV DATA TO IBUS* REGISTER 5
3280 020046 104412          ROMCLK           ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3281 020050 121125          121005:(5*20)   ;READ FROM IBUS* REGISTER 5
3282 020052 010005          MOV            R0,R5 ;PUT EXPECTED IN R5
3283 020054 116104 000005      MOVB          5(R1),R4 ;PUT "FOUND" INTO R4
3284 020056 120504          CMPB          R5,R4  ;DATA CORRECT?
3285 020058 001401          BEQ           68$   ;BR IF YES
3286 020060 104004          ERROR         4     ;ERROR
3287 020066 104405          68$: SCOP1      ;SMD9=1?
3288 020070 005100          COM           R0    ;CHANGE TO FLOATING 1
3289 020072 000241          CLC           ;CLEAR CARRY
3290 020074 106100          ROLB          R0    ;SHIFT BIT IN R0
3291 020076 001356          BNE           69$   ;IF R0=0 THEN DONE
3292
3293
3294
3295
3296
3297
3298
3299
3300
3301
3302
3303
3304 020100 000004          ;***** TEST 36 *****
3305 020102 012737 000036 001202 ;*MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
3306 020110 012737 020300 001442 ;*FLOAT A 1 THROUGH IBUS* REGISTER 10
3307 020116 012737 020136 001444 ;*FLOAT A 0 THROUGH IBUS* REGISTER 10
3308
3309
3310
3311
3312
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3324
3325
3326
3327
3328
3329
3330
3331
3332
3333
3334

```

```

:***** TEST 36 *****
:*MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
:*FLOAT A 1 THROUGH IBUS* REGISTER 10
:*FLOAT A 0 THROUGH IBUS* REGISTER 10
:*****

```

TEST 36

```

:*****
:TEST 36:
:*****
MOV            R36,STSTM          ; LOAD THE NO. OF THIS TEST
MOV            R51,ST37,NEXT     ; POINT TO THE START OF NEXT TEST.
MOV            R64$,LOCK         ; ADDRESS FOR LOCK ON DATA.
;R1 CONTAINS BASE KMC11 ADDRESS
MASTER CLEAR KMC11
SAVE REGISTER ADDRESS FOR TIMEOUT
START WITH BIT 0

MOV            R0,4(R1)          ; PUT PATTERN INTO PORT4
BIC            R141,4(R1)        ; CLEAR UNWANTED BITS
ROMCLK        ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121100:10      ; MOV DATA TO IBUS* REGISTER 10
ROMCLK        ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121005:(10*20) ; READ FROM IBUS* REGISTER 10
MOV            R0,R5            ; PUT EXPECTED IN R5
BIC            R141,R5          ; CLEAR UNWANTED BITS
MOVB          5(R1),R4          ; PUT "FOUND" INTO R4
CMPB          R5,R4            ; DATA CORRECT?
BEQ           65$              ; BR IF YES
ERROR         4                ; ERROR
65$: SCOP1      ; SMD9=1?
CLC           ; CLEAR CARRY
ROLB          R0                ; SHIFT BIT IN R0
BNE           64$              ; IF R0=0 THEN DONE
MOV            R67$,LOCK        ; NEW SCOP1
MOV            R1,R0            ; START WITH BIT 0
69$: COM           R0           ; CHANGE TO FLOATING ZERO
67$: MOV            R0,4(R1)     ; PUT PATTERN INTO PORT4
BIC            R141,4(R1)       ; CLEAR UNWANTED BITS
ROMCLK        ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

KMC11 MICRO PROCESSOR IBUS\* TESTS

3335	020240	121110			121100!10		MOV DATA TO IBUS* REGISTER 10
3336	020242	104412			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3337	020244	121205			121005!<10*20>		READ FROM IBUS* REGISTER 10
3338	020246	010005			MOV R0,R5		PUT EXPECTED IN R5
3339	020250	042705	000141		BIC #141,R5		CLEAR UNWANTED BITS
3340	020254	116104	000005		MOVB 5(R1),R4		PUT "FOUND" INTO R4
3341	020250	120504			CMPS R5,R4		DATA CORRECT?
3342	020252	001401			BEQ 65\$		BR IF YES
3343	020254	104004			ERROR 4		ERROR
3344	020256	104405			SCOPI		SND=1?
3345	020270	005100			COM R0		CHANGE TO FLOATING 1
3346	020272	000241			CLC		CLEAR CARRY
3347	020274	106100			ROLB R0		SHIFT BIT IN R0
3348	020276	001351			BNE 67\$		IF R0=0 THEN DONE

```

***** TEST 37 *****
MICRO PROCESSOR IBUS* REGISTER WRITE/READ TEST
#FLOAT A 1 THROUGH IBUS* REGISTER 11
#FLOAT A 0 THROUGH IBUS* REGISTER 11
*****

```

TEST 37

3350	020300	000004			TEST37: SCOPE		*****
3351	020302	012737	000037	001202	MOV #37,\$STNM		; LOAD THE NO. OF THIS TEST
3352	020310	012737	020510	001442	MOV #ST40,NEXT		; POINT TO THE START OF NEXT TEST.
3353	020316	012737	020336	001444	MOV #67\$,\$LOCK		; ADDRESS FOR LOCK ON DATA.
3354							; R1 CONTAINS BASE KMC11 ADDRESS
3355	020324	104410			STCLR		MASTER CLEAR KMC11
3356	020326	012702	000011		MOV #11,R2		SAVE REGISTER ADDRESS FOR TYPEOUT
3357	020332	012700	000001		MOV #1,R0		START WITH BIT 0
3358							
3359							
3360							
3361							
3362							
3363							
3364							
3365	020336	010061	000004		MOV R0,4(R1)		; PUT PATTERN INTO PORT4
3366	020342	042761	000262	000004	BIC #262,4(R1)		CLEAR UNWANTED BITS
3367	020348	104412			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3368	020352	121111			121100!11		MOV DATA TO IBUS* REGISTER 11
3369	020354	104412			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3370	020356	121225			121005!<11*20>		READ FROM IBUS* REGISTER 11
3371	020360	010005			MOV R0,R5		PUT EXPECTED IN R5
3372	020362	042705	000262		BIC #262,R5		CLEAR UNWANTED BITS
3373	020366	052705	000020		BIS #20,R5		ADD THESE BITS
3374	020372	116104	000005		MOVB 5(R1),R4		PUT "FOUND" INTO R4
3375	020376	120504			CMPS R5,R4		DATA CORRECT?
3376	020400	001401			BEQ 65\$		BR IF YES
3377	020402	104004			ERROR 4		ERROR
3378	020404	104405			SCOPI		SND=1?
3379	020406	000241			CLC		CLEAR CARRY
3380	020410	106100			ROLB R0		SHIFT BIT IN R0
3381	020412	001351			BNE 64\$		IF R0=0 THEN DONE
3382	020414	012737	020430	001444	MOV #67\$,\$LOCK		NEW SCOPI
3383	020422	012700	000001		MOV #1,R0		START WITH BIT 0
3384	020426	005100			COM R0		CHANGE TO FLOATING ZERO
3385	020430						
3386	020430	010061	000004		MOV R0,4(R1)		; PUT PATTERN INTO PORT4

3391	020434	042761	000262	000004	BIC	#262,4(R1)	; CLEAR UNWANTED BITS
3392	020442	104412			ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3393	020444	121111			121100!11		; MOV DATA TO IBUS* REGISTER 11
3394	020446	104412			ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3395	020450	121225			121005!<11*20>		; READ FROM IBUS* REGISTER 11
3396	020452	010005			MOV	R0,RS	; PUT EXPECTED IN RS
3397	020454	042761	000262		BIC	#262,RS	; CLEAR UNWANTED BITS
3398	020460	052705	000020		BIS	#20,RS	; SET THESE BITS
3399	020464	116104	000005		MOV#	5(R1),R4	; PUT "FOUND" INTO R4
3400	020470	120504			CMPB	RS,R4	; DATA CORRECT?
3401	020472	001401			BEQ	68\$	; BR IF YES
3402	020474	104004			ERROR	4	; ERROR
3403	020476	104405		68\$:	SCOP1		; SMO=1?
3404	020500	005100			COM	R0	; CHANGE TO FLOATING 1
3405	020502	000241			CLC		; CLEAR CARRY
3406	020504	106100			ROLB	R0	; SHIFT BIT IN R0
3407	020506	001347			BNE	69\$	; IF R0=0 THEN DONE

\*\*\*\*\* TEST 40 \*\*\*\*\*  
 ; MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
 ; FLOAT A 1 THROUGH IBUS REGISTER 0  
 ; FLOAT A 0 THROUGH IBUS REGISTER 0  
 ;\*\*\*\*\*

TEST 40

3418					*****		
3419	020510	000004			↑ST40: SCOPE		
3420	020512	012737	000040	001202	MOV	#40,STSTNM	; LOAD THE NO. OF THIS TEST
3421	020520	012737	020664	001442	MOV	#TST41,NEXT	; POINT TO THE START OF NEXT TEST.
3422	020526	012737	020546	001444	MOV	#64\$,LOCK	; ADDRESS FOR LOCK ON DATA.
3423							; R1 CONTAINS BASE KMC11 ADDRESS
3424	020534	104410			MSTCLR		; MASTER CLEAR KMC11
3425	020536	012702	000000		MOV	#0,R2	; SAVE REGISTER ADDRESS FOR TYPEOUT
3426	020542	012700	000001		MOV	#1,R0	; START WITH BIT 0
3427	020546						
3428	020546	010061	000004		MOV	R0,4(R1)	; PUT PATTERN INTO PORT4
3429	020552	104412			ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3430	020554	122100			122100!0		; MOV DATA TO IBUS REGISTER 0
3431	020556	104412			ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3432	020560	021005			21005!<0#20>		; READ FROM IBUS REGISTER 0
3433	020562	010005			MOV	R0,RS	; PUT EXPECTED IN RS
3434	020574	116104	000005		MOV#	5(R1),R4	; PUT "FOUND" INTO R4
3435	020570	120504			CMPB	RS,R4	; DATA CORRECT?
3436	020572	001401			BEQ	65\$	; BR IF YES
3437	020574	104005			ERROR	5	; ERROR
3438	020576	104405		65\$:	SCOP1		; SMO=1?
3439	020600	000241			CLC		; CLEAR CARRY
3440	020602	106100			ROLB	R0	; SHIFT BIT IN R0
3441	020604	001360			BNE	64\$	; IF R0=0 THEN DONE
3442	020606	012737	020622	001444	MOV	#67\$,LOCK	; NEW SCOP1
3443	020614	012700	000001		MOV	#1,R0	; START WITH BIT 0
3444	020620	005100			COM	R0	; CHANGE TO FLOATING ZERO
3445	020622						
3446	020622	010061	000004		MOV	R0,4(R1)	; PUT PATTERN INTO PORT4

3447	020626	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3448	020630	122100		122100!0		:MOV DATA TO IBUS REGISTER 0
3449	020632	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3450	020634	021005		21005!<0#20>		:READ FROM IBUS REGISTER 0
3451	020636	010005		MOV	RO,RS	:PUT EXPECTED IN RS
3452	020640	116104	000005	MOV#	5(R1),R4	:PUT "FOUND" INTO R4
3453	020644	120504		CMPS	RS,R4	:DATA CORRECT?
3454	020646	001401		BEG	68\$	:BR IF YES
3455	020648	104005		ERROR	5	:ERROR
3456	020650	104405		SCOPI		:SHOW=1?
3457	020654	005100		COM	RO	:CHANGE TO FLOATING 1
3458	020656	000241		CLC		:CLEAR CARRY
3459	020660	106100		ROLB	RO	:SHIFT BIT IN RO
3460	020662	001356		BNE	69\$	:IF RO=0 THEN DONE

\*\*\*\*\* TEST 41 \*\*\*\*\*  
 :MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
 :FLOAT A 1 THROUGH IBUS REGISTER 1  
 :FLOAT A 0 THROUGH IBUS REGISTER 1  
 :\*\*\*\*\*

TEST 41

3471						:*****
3472	020664	000004		TEST41: SCOPE		
3473	020666	012737	000041	MOV	#41,STSTNM	:LOAD THE NO. OF THIS TEST
3474	020674	012737	021040	MOV	#ST42,NEXT	:POINT TO THE START OF NEXT TEST.
3475	020702	012737	020722	MOV	#64\$,LOCK	:ADDRESS FOR LOCK ON DATA.
3476						:R1 CONTAINS BASE KMC11 ADDRESS
3477	020710	104410		INSTCLR		:MASTER CLEAR KMC11
3478	020712	012702	000001	MOV	#1,R2	:SAVE REGISTER ADDRESS FOR TYPEOUT
3479	020716	012700	000001	MOV	#1,R0	:START WITH BIT 0
3480	020722			64\$:		
3481	020722	010061	000004	MOV	RO,4(R1)	:PUT PATTERN INTO PORT4
3482	020726	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3483	020730	122101		122100!1		:MOV DATA TO IBUS REGISTER 1
3484	020732	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3485	020734	021025		21005!<1#20>		:READ FROM IBUS REGISTER 1
3486	020736	010005		MOV	RO,RS	:PUT EXPECTED IN RS
3487	020740	116104	000005	MOV#	5(R1),R4	:PUT "FOUND" INTO R4
3488	020744	120504		CMPS	RS,R4	:DATA CORRECT?
3489	020746	001401		BEG	65\$	:BR IF YES
3490	020750	104005		ERROR	5	:ERROR
3491	020752	104405		SCOPI		:SHOW=1?
3492	020754	000241		CLC		:CLEAR CARRY
3493	020756	106100		ROLB	RO	:SHIFT BIT IN RO
3494	020760	001350		BNE	64\$	:IF RO=0 THEN DONE
3495	020762	012737	020776	MOV	#67\$,LOCK	:NEW SCOPI
3496	020770	012700	000001	MOV	#1,R0	:START WITH BIT 0
3497	020774	005100		69\$: COM	RO	:CHANGE TO FLOATING ZERO
3498	020776			67\$:		
3499	020776	010061	000004	MOV	RO,4(R1)	:PUT PATTERN INTO PORT4
3500	021002	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3501	021004	122101		122100!1		:MOV DATA TO IBUS REGISTER 1
3502	021006	104412		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

3503 021010 021025
3504 021012 010005
3505 021014 116104 000005
3506 021016 120504
3507 021018 001401
3508 021020 104005
3509 021022 104405
3510 021024 005100
3511 021026 000241
3512 021028 106100
3513 021030 001356
3514
3515
3516
3517
3518
3519

```

```

21005!(1#20)
MOV R0,R5
MOV 5(R1),R4
CPSB R5,R4
BC 648
ERROR 5
SCOPI
COM R0
CLC
ROLB R0
BNE 698

```

```

: READ FROM IBUS REGISTER 1
: PUT EXPECTED IN R5
: PUT "FOUND" INTO R4
: DATA CORRECT?
: BR IF YES
: ERROR
: SLO?=?
: CHANGE TO FLOATING 1
: CLEAR CARRY
: SHIFT BIT IN R0
: IF R0=0 THEN DONE

```

```

: ***** TEST 42 *****
: #MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
: #FLOAT A 1 THROUGH IBUS REGISTER 2
: #FLOAT A 0 THROUGH IBUS REGISTER 2
: *****

```

TEST 42

```

3520 021040 000004
3521 021042 012737 000042 001202
3522 021044 012737 021214 001442
3523 021046 012737 021076 001444
3524
3525
3526
3527
3528 021064 104410
3529 021066 012732 000002
3530 021072 012700 000001
3531 021076 010061 000004
3532 021102 104412
3533 021104 122102
3534 021106 104412
3535 021110 021045
3536 021112 010005
3537 021114 116104 000005
3538 021120 120504
3539 021122 001401
3540 021124 104005
3541 021126 104405
3542 021128 000241
3543 021130 106100
3544 021132 001260
3545 021134 012737 021152 001444
3546 021136 012700 000001
3547 021138 005100
3548 021140 010061 000004
3549 021142 104412
3550 021144 122102
3551 021146 104412
3552 021148 021045
3553 021150 010005
3554 021152 116104 000005
3555
3556
3557
3558

```

```

: *****
: TEST 42
: *****
: #1ST42: SCOPE
: MOV #42,STSTN# : LOAD THE NO. OF THIS TEST
: MOV #1ST43,NEXT : POINT TO THE START OF NEXT TEST.
: MOV #648,LOCK : ADDRESS FOR LOCK ON DATA.
: #R1 CONTAINS BASE KMC11 ADDRESS
: #MASTER CLEAR KMC11
: #SAVE REGISTER ADDRESS FOR TYPEOUT
: #START WITH BIT 0
:
: #648:
: MOV R0,4(R1) : PUT PATTERN INTO PORT4
: ROMCLK : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: 122100!2 : MOV DATA TO IBUS REGISTER 2
: ROMCLK : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: 21005!(2#20)
: MOV R0,R5 : READ FROM IBUS REGISTER 2
: MOV 5(R1),R4 : PUT EXPECTED IN R5
: CPSB R5,R4 : PUT "FOUND" INTO R4
: BC 658 : DATA CORRECT?
: ERROR : BR IF YES
: SCOPI : ERROR
: CLC : SLO?=?
: ROLB R0 : CLEAR CARRY
: BNE 648 : SHIFT BIT IN R0
: MOV #678,LOCK : IF R0=0 THEN DONE
: MOV #1,R0 : NEW SCOPI
: COM R0 : START WITH BIT 0
:
: #698:
: MOV R0,4(R1) : PUT PATTERN INTO PORT4
: ROMCLK : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: 122100!2 : MOV DATA TO IBUS REGISTER 2
: ROMCLK : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: 21005!(2#20)
: MOV R0,R5 : READ FROM IBUS REGISTER 2
: MOV 5(R1),R4 : PUT EXPECTED IN R5
: MOV 5(R1),R4 : PUT "FOUND" INTO R4

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3559 021174 120504  
3560 021176 001401  
3561 021200 104005  
3562 021202 104405  
3563 021204 005100  
3564 021206 000241  
3565 021210 106100  
3566 021212 001356  
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3578 021214 000004  
3579 021216 012737 000043 001202  
3580 021224 012737 021370 001442  
3581 021232 012737 021252 001444  
3582  
3583 021240 104410  
3584 021242 012702 000003  
3585 021246 012700 000001  
3586 021250  
3587 021252 010061 000004  
3588 021254 104412  
3589 021256 122103  
3590 021258 104412  
3591 021254 021055  
3592 021256 010005  
3593 021270 116104 000005  
3594 021274 120504  
3595 021276 001401  
3596 021300 104005  
3597 021302 104405  
3598 021304 000241  
3599 021306 106100  
3600 021310 001360  
3601 021312 012737 021326 001444  
3602 021320 012700 000001  
3603 021324 005100  
3604 021326  
3605 021326 010061 000004  
3606 021328 104412  
3607 021334 122103  
3608 021336 104412  
3609 021340 021055  
3610 021342 010005  
3611 021344 116104 000005  
3612 021350 120504  
3613 021352 001401  
3614 021354 104005

685: CMPB RS,R4  
BEQ 685  
ERROR 5  
SCOPI  
COM R0  
CLC  
ROLB R0  
BNE 695

: DATA CORRECT?  
: BR IF YES  
: ERROR  
: S409=1?  
: CHANGE T. FLOATING 1  
: CLEAR CARRY  
: SHIFT BIT IN R0  
: IF R0=0 THEN DONE

\*\*\*\*\* TEST 43 \*\*\*\*\*  
: MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
: FLOAT A 1 THROUGH IBUS REGISTER 3  
: FLOAT A 0 THROUGH IBUS REGISTER 3  
\*\*\*\*\*

TEST 43

\*\*\*\*\*

1ST43: SCOPE  
MOV #43,\$STSNH ; LOAD THE NO. OF THIS TEST  
MOV \$TST44,NEXT ; POINT TO THE START OF NEXT TEST.  
MOV #64,\$LOCK ; ADDRESS FOR LOCK ON DATA.

: R1 CONTAINS BASE KMC11 ADDRESS  
: MASTER CLEAR KMC11  
: SAVE REGISTER ADDRESS FOR TYPEOUT  
: START WITH BIT 0

645: MOV R0,4(R1) ; PUT PATTERN INTO PORT4  
RONCLK ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
122100!3 ; MOV DATA TO IBUS REGISTER 3  
RONCLK ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
21005!(3\*20) ; READ FROM IBUS REGISTER 3

: PUT EXPECTED IN R5  
: PUT "FOUND" INTO R4  
: DATA CORRECT?  
: BR IF YES  
: ERROR

655: SCOPI  
CLC  
ROLB R0  
BNE 645  
MOV #67,\$LOCK  
MOV #1,R0  
COM R0

: S409=1?  
: CLEAR CARRY  
: SHIFT BIT IN R0  
: IF R0=0 THEN DONE  
: NEW SCOPI  
: START WITH BIT 0  
: CHANGE TO FLOATING ZERO

695: MOV R0,4(R1) ; PUT PATTERN INTO PORT4  
RONCLK ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
122100!3 ; MOV DATA TO IBUS REGISTER 3  
RONCLK ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
21005!(3\*20) ; READ FROM IBUS REGISTER 3

: PUT EXPECTED IN R5  
: PUT "FOUND" INTO R4  
: DATA CORRECT?  
: BR IF YES  
: ERROR

KMC11 MICRO PROCESSOR IBUS TESTS

3615 021356 104405  
3616 021360 005100  
3617 021362 000241  
3618 021364 106100  
3619 021366 001356

68\$: SCOP1 ;SMD9=1?  
COM RO ;CHANGE TO FLOATING 1  
CLC ;CLEAR CARRY  
ROLB RO ;SHIFT BIT IN RO  
BNE 69\$ ;IF RO=0 THEN DONE

\*\*\*\*\* TEST 44 \*\*\*\*\*  
\*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
\*FLOAT A 1 THROUGH IBUS REGISTER 4  
\*FLOAT A 0 REGISTER 4  
\*\*\*\*\*

TEST 44

3631 021370 000004  
3632 021372 012737 000044 001202  
3633 021400 012737 021544 001442  
3634 021406 012737 021426 001444

\*\*\*\*\*  
TST44: SCOPE ; LOAD THE NO. OF THIS TEST  
MOV #44,STSTNM ; POINT TO THE START OF NEXT TEST.  
MOV #TST45,NEXT ; ADDRESS FOR LOCK ON DATA.  
MOV #64\$,LOCK ; RI CONTAINS BASE KMC11 ADDRESS  
; MASTER CLEAR KMC11  
; SAVE REGISTER ADDRESS FOR TYPEOUT  
; START WITH BIT 0

3636 021414 104410  
3637 021416 012702 000004  
3638 021422 012700 000001

64\$: NOV RO,4(R1) ; PUT PATTERN INTO PORT4  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
122100!4 ; NOV DATA TO IBUS REGISTER 4  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
21005!(4\*20) ; READ FROM IBUS REGISTER 4  
NOV RO,R5 ; PUT EXPECTED IN R5  
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4  
CMPB R5,R4 ; DATA CORRECT?  
BEQ 65\$ ; BR IF YES  
ERROR 5 ; ERROR

3640 021426 010061 000004  
3641 021432 104412  
3642 021434 122104  
3643 021436 104412  
3644 021440 021105  
3645 021442 010005

65\$: SCOP1 ;SMD9=1?  
CLC ;CLEAR CARRY  
ROLB RO ;SHIFT BIT IN RO  
BNE 64\$ ;IF RO=0 THEN DONE  
MOV #67\$,LOCK ;NEW SCOP1  
MOV #1,R0 ;START WITH BIT 0  
69\$: COM RO ;CHANGE TO FLOATING ZERO  
67\$:

3646 021444 116104 000005  
3647 021450 120504  
3648 021452 001401  
3649 021454 104005  
3650 021456 104405  
3651 021460 000241  
3652 021462 106100  
3653 021464 001360  
3654 021466 012737 021502 001444  
3655 021474 012700 000001  
3656 021500 005100  
3657 021502

NOV RO,4(R1) ; PUT PATTERN INTO PORT4  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
122100!4 ; NOV DATA TO IBUS REGISTER 4  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
21005!(4\*20) ; READ FROM IBUS REGISTER 4  
NOV RO,R5 ; PUT EXPECTED IN R5  
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4  
CMPB R5,R4 ; DATA CORRECT?  
BEQ 68\$ ; BR IF YES  
ERROR 5 ; ERROR

3658 021502 010061 000004  
3659 021506 104412  
3660 021510 122104  
3661 021512 104412  
3662 021514 021105  
3663 021516 010005  
3664 021520 116104 000005  
3665 021524 120504  
3666 021526 001401  
3667 021530 104005  
3668 021532 104405  
3669 021534 005100  
3670 021536 000241

68\$: SCOP1 ;SMD9=1?  
COM RO ;CHANGE TO FLOATING 1  
CLC ;CLEAR CARRY



```

3671 021540 106100          ROLB  RO          ;SHIFT BIT IN RO
3672 021542 001356          BNE   69$         ;IF RO=0 THEN DONE
3673
3674
3675          ;***** TEST 45 *****
3676          ;MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST
3677          ;FLOAT A 1 THROUGH IBUS REGISTER 5
3678          ;FLOAT A 0 THROUGH IBUS REGISTER 5
3679          ;*****
3680
3681          ; TEST 45
3682          ;-----
3683          ;*****
3684 021544 000004          1$T45: SCOPE
3685 021546 012737 000045 001202  MOV   #45,BSTNM          ; LOAD THE NO. OF THIS TEST
3686 021554 012737 021720 001442  MOV   #15146,NEXT       ; POINT TO THE START OF NEXT TEST.
3687 021562 012737 021602 001444  MOV   #64$,LOCK        ; ADDRESS FOR LOCK ON DATA.
3688                                     ; RI CONTAINS BASE KMC11 ADDRESS
3689 021570 104410          MSTCLR          ;MASTER CLEAR KMC11
3690 021572 012702 000005  MOV   #5,R2          ;SAVE REGISTER ADDRESS FOR TYPEOUT
3691 021576 012700 000001  MOV   #1,R0          ;START WITH BIT 0
3692 021602
3693 021602 010061 000004          64$: MOV   RO,4(R1)        ; PUT PATTERN INTO PORT4
3694 021606 104412          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3695 021610 122105          122100!5        ;MOV DATA TO IBUS REGISTER 5
3696 021612 104412          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3697 021614 021125          21005!(5*20)    ;READ FROM IBUS REGISTER 5
3698 021616 010005          MOV   RO,R5        ;PUT EXPECTED IN R5
3699 021620 116104 000005  MOVB  S(R1),R4     ;PUT "FOUND" INTO R4
3700 021624 120504          CHPB  R5,R4        ;DATA CORRECT?
3701 021626 001401          BEQ   65$         ;OR IF YES
3702 021630 104005          ERROR 5          ;ERROR
3703 021632 104405          65$: SCOP1          ;STOP!
3704 021634 000241          CLC           ;CLEAR CARRY
3705 021636 106100          ROLB  RO          ;SHIFT BIT IN RO
3706 021640 001360          BNE   64$         ;IF RO=0 THEN DONE
3707 021642 012737 021656 001444  MOV   #67$,LOCK     ;NEW SCOP1
3708 021650 012700 000001  MOV   #1,R0        ;START WITH BIT 0
3709 021654 005100          69$: COM   RO          ;CHANGE TO FLOATING ZERO
3710 021656
3711 021656 010061 000004          67$: MOV   RO,4(R1)        ; PUT PATTERN INTO PORT4
3712 021662 104412          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3713 021664 122105          122100!5        ;MOV DATA TO IBUS REGISTER 5
3714 021666 104412          ROMCLK          ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3715 021670 021125          21005!(5*20)    ;READ FROM IBUS REGISTER 5
3716 021672 010005          MOV   RO,R5        ;PUT EXPECTED IN R5
3717 021674 116104 000005  MOVB  S(R1),R4     ;PUT "FOUND" INTO R4
3718 021700 120504          CHPB  R5,R4        ;DATA CORRECT?
3719 021702 001401          BEQ   68$         ;OR IF YES
3720 021704 104005          ERROR 5          ;ERROR
3721 021706 104405          68$: SCOP1          ;STOP!
3722 021710 005100          COM   RO          ;CHANGE TO FLOATING 1
3723 021712 000241          CLC           ;CLEAR CARRY
3724 021714 106100          ROLB  RO          ;SHIFT BIT IN RO
3725 021716 001356          BNE   69$         ;IF RO=0 THEN DONE
3726

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021720 000004  
021722 012737 000046 001202  
021730 012737 022074 001442  
021736 012737 021756 001444  
  
021744 104410  
021746 012702 000006  
021752 012700 000001  
  
021756 010061 000004  
021762 104412  
021764 122106  
021766 104412  
021770 021145  
021772 010005  
021774 116104 000005  
022000 120504  
022002 001401  
022004 104005  
022006 104405  
022010 000241  
022012 106100  
022014 001360  
022016 012737 022032 001444  
022024 012700 000001  
022030 005100  
022032 010061 000004  
022036 104412  
022040 122106  
022042 104412  
022044 021145  
022046 010005  
022050 116104 000005  
022054 120504  
022056 001401  
022060 104005  
022062 104405  
022064 005100  
022066 000241  
022070 106100  
022072 001356

\*\*\*\*\* TEST 46 \*\*\*\*\*  
\*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST  
\*FLOAT A 1 THROUGH IBUS REGISTER 6  
\*FLOAT A 0 THROUGH IBUS REGISTER 6  
\*\*\*\*\*

TEST 46

-----  
\*\*\*\*\*  
TST46: SCOPE  
MOV #46,STSTN ; LOAD THE NO. OF THIS TEST  
MOV #TST47,NEXT ; POINT TO THE START OF NEXT TEST.  
MOV #64\$,LOCK ; ADDRESS FOR LOCK ON DATA.  
; R1 CONTAINS BASE KMC11 ADDRESS  
MSTCLR ; MASTER CLEAR KMC11  
MOV #6,R2 ; SAVE REGISTER ADDRESS FOR TYPEOUT  
MOV #1,R0 ; START WITH BIT 0  
  
64\$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
122100!6 ; MOV DATA TO IBUS REGISTER 6  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
21005!(6+20) ; READ FROM IBUS REGISTER 6  
MOV R0,R5 ; PUT EXPECTED IN R5  
MOVB S(R1),R4 ; PUT "FOUND" INTO R4  
CMPB R5,R4 ; DATA CORRECT?  
BEQ 65\$ ; BR IF YES  
ERROR ; ERROR  
SNO4=1 ;  
CLC ; CLEAR CARRY  
ROLB R0 ; SHIFT BIT IN R0  
BNE 64\$ ; IF R0=0 THEN DONE  
MOV #67\$,LOCK ; NEW SCOPE  
MOV #1,R0 ; START WITH BIT 0  
69\$: COM R0 ; CHANGE TO FLOATING ZERO  
67\$: MOV R0,4(R1) ; PUT PATTERN INTO PORT4  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
122100!6 ; MOV DATA TO IBUS REGISTER 6  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
21005!(6+20) ; READ FROM IBUS REGISTER 6  
MOV R0,R5 ; PUT EXPECTED IN R5  
MOVB S(R1),R4 ; PUT "FOUND" INTO R4  
CMPB R5,R4 ; DATA CORRECT?  
BEQ 68\$ ; BR IF YES  
ERROR ; ERROR  
SNO4=1 ;  
COM R0 ; CHANGE TO FLOATING 1  
CLC ; CLEAR CARRY  
ROLB R0 ; SHIFT BIT IN R0  
BNE 69\$ ; IF R0=0 THEN DONE

\*\*\*\*\* TEST 47 \*\*\*\*\*  
\*MICRO PROCESSOR IBUS REGISTER WRITE/READ TEST

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022074 000004  
022076 012737 000047 001202  
022104 012737 022250 001442  
022112 012737 022132 001444  
022120 104410  
022122 012702 000007  
022126 012700 000001  
022132 010061 000004  
022136 104412  
022140 122107  
022146 104412  
022154 210051(7\*20)  
022156 010005  
022162 116104 000005  
022166 120504  
022168 001401  
022170 104405  
022172 104405  
022174 000241  
022176 106100  
022178 001360  
022172 012737 022206 001444  
022200 012700 000001  
022204 005100  
022206 010061 000004  
022212 104412  
022214 122107  
022216 104412  
022220 021165  
022222 010005  
022224 116104 000005  
022230 120504  
022232 001401  
022234 104405  
022236 104405  
022240 005100  
022242 000241  
022244 106100  
022246 001356

```
*****  
: #FLOAT A 1 THROUGH IBUS REGISTER 7  
: #FLOAT A 0 THROUGH IBUS REGISTER 7  
: *****  
: TEST 47  
: -----  
: *****  
†ST47: SCOPE  
MOV #47,STSTNM ; LOAD THE NO. OF THIS TEST  
MOV #TST50,NEXT ; POINT TO THE START OF NEXT TEST.  
MOV #64$,LOCK ; ADDRESS FOR LOCK ON DATA.  
; RI CONTAINS BASE KMC11 ADDRESS  
MSTCLR ; MASTER CLEAR KMC11  
MOV #7,R2 ; SAVE REGISTER ADDRESS FOR TYPEOUT  
MOV #1,R0 ; START WITH BIT 0  
64$:  
MOV R0,(R1) ; PUT PATTERN INTO PORT4  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
122100? ; MOV DATA TO IBUS REGISTER 7  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
210051(7*20) ; READ FROM IBUS REGISTER 7  
MOV R0,R5 ; PUT EXPECTED IN R5  
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4  
CMPB R5,R4 ; DATA CORRECT?  
BEQ 65$ ; BR IF YES  
ERROR ;  
SND9=1? ;  
CLC ; CLEAR CARRY  
ROLB R0 ; SHIFT BIT IN R0  
BNE 64$ ; IF R0=0 THEN DONE  
65$:  
MOV #67$,LOCK ; NEW SCOPE  
MOV #1,R0 ; START WITH BIT 0  
COM R0 ; CHANGE TO FLOATING ZERO  
67$:  
MOV R0,(R1) ; PUT PATTERN INTO PORT4  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
122100? ; MOV DATA TO IBUS REGISTER 7  
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
210051(7*20) ; READ FROM IBUS REGISTER 7  
MOV R0,R5 ; PUT EXPECTED IN R5  
MOVB 5(R1),R4 ; PUT "FOUND" INTO R4  
CMPB R5,R4 ; DATA CORRECT?  
BEQ 68$ ; BR IF YES  
ERROR ;  
SND9=1? ;  
COM R0 ; CHANGE TO FLOATING 1  
CLC ; CLEAR CARRY  
ROLB R0 ; SHIFT BIT IN R0  
BNE 69$ ; IF R0=0 THEN DONE  
68$:  
COM R0 ;  
CLC ;  
ROLB R0 ;  
BNE 69$ ;  
69$:  
COM R0 ;  
CLC ;  
ROLB R0 ;  
BNE 69$ ;
```

```
***** TEST 50 *****  
: #MICRO PROCESSOR IBUS DUAL ADDRESS TEST  
: #WRITE ALL IBUS REGISTERS WITH INCREMENTING PATTERN  
: #READ ALL IBUS REGISTERS TO VERIFY CORRECT ADDRESSING  
: *****
```

```

3839
3840
3841
3842
3843 022250 000004
3844 022252 012737 000050 001202
3845 022250 012737 022476 001442
3846 022256 012737 022304 001444
3847
3848 022274 104410
3849 022276 012700 000001
3850 022302 005002
3851 022304 010203
3852 022306 010061 000004
3853 022312 042737 000017 022326
3854 022320 050337 022326
3855 022324 104412
3856 022326 122100
3857 022330 006303
3858 022332 006303
3859 022334 006303
3860 022336 006303
3861 022340 042737 000360 022354
3862 022346 050337 022354
3863 022352 104412
3864 022354 021005
3865 022356 110005
3866 022360 116104 000005
3867 022364 120504
3868 022366 001401
3869 022370 104005
3870 022372 104405
3871 022374 005200
3872 022376 005202
3873 022400 022702 000010
3874 022404 001337
3875 022406 012737 022424 001444
3876 022414 012700 000001
3877 022420 005002
3878 022422 005003
3879 022424 042737 000360 022440
3880 022432 050337 022440
3881 022436 104412
3882 022440 021005
3883 022442 010005
3884 022444 116104 000005
3885 022450 120504
3886 022452 001401
3887 022454 104005
3888 022456 104405
3889 022460 005200
3890 022462 005202
3891 022464 062703 000020
3892 022470 022702 000010
3893 022474 001353
3894

```

```

; TEST 50
; *****
; STS0: SCOPE
; MOV #50,STSTNM ; LOAD THE NO. OF THIS TEST
; MOV #STST1,NEXT ; POINT TO THE START OF NEXT TEST.
; MOV #IS,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
; MASTER CLEAR KMC11
; START WITH A ONE
; R2 CONTAINS ADDRESS OF REGISTER
; R3 REGISTER ADDRESS
; WRITE DATA TO PORT4
; CLEAR ADDRESS FIELD OF INSTRUCTION
; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; MOVE DATA TO IBUS REGISTER
; SHIFT ADDRESS
; 4 TIMES TO GET
; IT TO BITS 4-7
; OF NEXT INSTRUCTION
; CLEAR ADDRESS FIELD
; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; READ FROM IBUS REGISTER
; PUT "EXPECTED" IN R5
; PUT "FOUND" IN R4
; IS DATA CORRECT?
; BR IF YES
; DATA ERROR
; SMO#1?
; INCREMENT PATTERN
; INCREMENT REGISTER ADDRESS
; #7+1,R2 ;LAST ADDRESS DONE?
; BR IF NO
; NEW SCOPI
; RESTART PATTERN TO 1
; RESTART AT ADDRESS 0
; RESTART AT ADDRESS 0
; CLEAR ADDRESS FIELD OF INSTRUCTION
; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; READ FROM IBUS REGISTER
; PUT "EXPECTED" IN R5
; PUT "FOUND" IN R5
; DATA CORRECT?
; BR IF YES
; DATA ADDRESSING ERROR
; SMO#1?
; INCREMENT PATTERN
; NEXT ADDRESS
; ADD 1 TO ADDRESS IN R3(SHIFTED 4 TIMES)
; #7+1,R2 ;LAST ADDRESS DONE?
; BR IF NO

```

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022476 000004  
022500 012737 000051 001202  
022506 012737 022646 001442  
022514 012737 022530 001444  
  
022522 104410  
022524 012700 000001  
022530  
022530 010061 000004  
022534 104412  
022536 120500  
022540 104412  
022542 061225  
022544 010005  
022546 116104 000005  
022550 120504  
022552 001401  
022554 104006  
022556 104405  
022560 000241  
022564 106100  
022566 001350  
022570 012737 022604 001444  
022576 012700 000001  
022602 005100  
022604  
022604 010061 000004  
022610 104412  
022612 120500  
022614 104412  
022616 061225  
022620 010005  
022624 116104 000005  
022626 120504  
022630 001401  
022632 104006  
022634 104405  
022636 005100  
022640 000241  
022642 106100  
022644 001350

\*\*\*\*\* TEST 51 \*\*\*\*\*  
:MICRO PROCESSOR BR REGISTER TEST  
:#FLOAT A 1 THROUGH THE BR  
:#FLOAT A 0 THROUGH THE BR  
:\*\*\*\*\*

TEST 51

.....  
TST51: SCOPE  
MOV #51, STSTNM ; LOAD THE NO. OF THIS TEST  
MOV #TST52, NEXT ; POINT TO THE START OF NEXT TEST.  
MOV #648, LOCK ; ADDRESS FOR LOCK ON DATA.  
; R1 CONTAINS BASE KMC11 ADDRESS  
; MASTER CLEAR KMC11  
; START PATTERN WITH BIT0  
648: MSTRCLR  
MOV #1, R0  
MOV R0, 4(R1) ; WRITE PATTERN IN PORT4  
RONCLK ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
120500 ; MOVE DATA TO THE BR REGISTER  
RONCLK ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
061225 ; MOVE BR TO PORT 5  
MOV R0, R5 ; PUT "EXPECTED" IN R5  
MOVB 5(R1), R4 ; PUT "FOUND" IN R4  
CMPB R5, R4 ; DATA CONNECT?  
BEQ 658 ; BR IF YES  
ERROR 6 ; DATA ERROR  
658: SCOP1  
CLC ; CLEAR CARRY  
ROLB R0 ; SHIFT BIT IN R0  
BNE 648 ; DONE IF NO=0  
MOV #675, LOCK ; NEW SCOP1  
MOV #1, R0 ; START PATTERN WITH BIT0  
698: COM R0 ; CHANGE TO FLOATING ZERO  
675: MOV R0, 4(R1) ; WRITE PATTERN IN PORT4  
RONCLK ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
120500 ; MOVE DATA TO THE BR REGISTER  
RONCLK ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
061225 ; MOVE BR TO PORT 5  
MOV R0, R5 ; PUT "EXPECTED" IN R5  
MOVB 5(R1), R4 ; PUT "FOUND" IN R4  
CMPB R5, R4 ; DATA CONNECT?  
BEQ 688 ; BR IF YES  
ERROR 6 ; DATA ERROR  
688: COM R0 ; CHANGE BACK TO A ONE  
CLC ; CLEAR CARRY  
ROLB R0 ; SHIFT BIT IN R0  
BNE 698 ; DONE IF RO=0

\*\*\*\*\* TEST 52 \*\*\*\*\*  
:SCRATCH PAD TEST





```

4063 023302 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4064 023304 061225 ;MOV BR TO PORT5
4065 023306 010005 MOV RO,R5 ;PUT "EXPECTED" IN R5
4066 023310 116104 0000G5 MOVB 5(R1),R4 ;PUT "FOUND" IN R4
4067 023314 120504 CMPB R5,R4 ;DATA CORRECT?
4068 023316 001401 BEQ 7$ ;BR IF YES
4069 023320 104007 ERROR 7 ;SP ADDRESSING ERROR
4070 023322 104405 7$: SCOPI ;S409=1?
4071 023324 005200 INC RO ;INCREMENT PATTERN
4072 023326 005203 INC R3 ;NEXT ADDRESS
4073 023330 022703 000020 CMP #20,R3 ;LAST ADDRESS DONE?
4074 023334 001352 BNE 5$ ;BR IF NO
4075
4076
4077
4078
4079
4080
4081
4082
4083
4084

```

```

***** TEST 54 *****
*INTERRUPT TEST
*TEST THAT DEVICE CAN INTERRUPT TO VECTOR A
*****

```

TEST 54

```

4085 023336 000004 7$T54: SCOPE ;*****
4086 023340 012737 000054 001202 MOV #54,$T5TMM ; LOAD THE NO. OF THIS TEST
4087 023346 012737 023432 001442 MOV #T5T55,NEXT ; POINT TO THE START OF NEXT TEST.
4088 ;R1 CONTAINS BASE KMC11 ADDRESS
4089 023354 000005 RESET ;BUS RESET
4090 023356 005011 CLR (R1) ;CLEAR RUN
4091 023360 004537 035516 JSR R5,GETVEC ;SET UP VECTORS
4092 023364 023426 3$ ;X00
4093 023366 023424 2$ ;X04
4094 023370 340 340 ;LEVEL 7
4095 023372 012737 000340 177776 1$: MOV #340,PS ;PS = LEVEL 7
4096 023400 012761 000200 000004 MOV #200,4(R1) ;WRITE PORT4
4097 023406 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4098 023410 121111 121111 ;SET BR R0 IN [BUS# REG 1]
4099 023412 005037 177776 CLR PS ;ALLOW INTERRUPT
4100 023416 000240 NOP
4101 023420 104010 ERROR 10 ;NO INTERRUPT
4102 023422 000403 BR 4$ 4$
4103 023424 104011 2$: ERROR 11 ;WRONG VECTOR
4104 023426 012706 001200 3$: MOV #STACK,SP ;RESET STACK
4105 023432 4$:
4106
4107
4108
4109
4110
4111
4112
4113
4114
4115

```

```

***** TEST 55 *****
*INTERRUPT TEST
*TEST THAT DEVICE CAN INTERRUPT TO VECTOR B
*****

```

TEST 55

```

4116 023432 000004 7$T55: SCOPE ;*****
4117 023434 012737 000055 001202 MOV #55,$T5TMM ; LOAD THE NO. OF THIS TEST
4118 023442 012737 023524 001442 MOV #T5T56,NEXT ; POINT TO THE START OF NEXT TEST.

```



```

4119
4120 023450 104410          MSTCLR
4121 023452 004537 03551F    JSR    R5,SETVEC
4122 023454 023516          2$
4123 023456 023520          3$
4124 023458          340          340
4125 023464 012737 000340 177776 1$: MOV    #340,PS
4126 023472 012761 000300 000074    MOV    #300,4(R1)
4127 023500 104412          ROMCLK
4128 023502 121111          121111
4129 023504 005037 177776    CLR    PS
4130 023510 000240          NOP
4131 023512 104010          ERROR  10
4132 023514 000403          BR     4$
4133 023516 104011          2$: ERROR  11
4134 023520 01270E 001200    3$: MOV    #STACK,SP
4135 023524          4$:

```

```

:R1 CONTAINS BASE KMC11 ADDRESS
:MASTER CLEAR KMC11
:SET UP VECTORS
:XXD
:XX4
:LEVEL 7
:PS = LEVEL 7
:WRITE PORT4
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:SET BR R0 IN I2US* REG 11
:ALLOW INTERRUPT
:NO INTERRUPT
:WRONG VECTOR
:RESET STACK

```

```

:***** TEST 56 *****
: *PRIORITY INTERRUPT TESTS
: *SET PS TO ALL BR LEVELS EQUAL OR GREATER THAN
: *THE KMC11 LEVEL, VERIFY THAT KMC11 DOES NOT INTERRUPT
:*****

```

TEST 56

```

4147 023524 000004          1$T56: SCOPE
4148 023526 012737 000056 001202    MOV    #56,$STSTM
4149 023534 012737 023646 001442    MOV    #T57,NEXT
4150
4151 023542 104410          MSTCLR
4152 023544 012702 000340          MOV    #340,R2
4153 023550 010237 177776          MOV    R2,PS
4154 023554 013700 002050          MOV    STAT1,R0
4155 023560 006200          ASR   R0
4156 023562 006200          ASR   R0
4157 023564 006200          ASR   R0
4158 023566 006200          ASR   R0
4159 023570 042700 177437          BIC   #177437,R0
4160 023574 004537 035516          JSR   R5,SETVEC
4161 023600 023642          2$
4162 023602 023642          2$
4163 023604          340          340
4164 023606 012761 000200 000004 4$: MOV    #200,4(R1)
4165 023614 104412          ROMCLK
4166 023616 121111          121111
4167 023620 010237 177776    5$: MOV    R2,PS
4168 023624 000240          NOP
4169 023626 020002          CMP   R0,R2
4170 023630 001403          BEQ  1$
4171 023632 162702 000040          SUB   #40,R2
4172 023636 000770          BR   5$
4173 023640 104420          1$: ADVANCE
4174 023642 104020          2$: ERROR  20

```

```

: LOAD THE NO. OF THIS TEST
: POINT TO THE START OF NEXT TEST.
:R1 CONTAINS BASE KMC11 ADDRESS
:MASTER CLEAR KMC11
:PUT LEVEL 7 IN R2
:SET PRIORITY TO 7
:GET BR LEVEL OF KMC11
:SHIFT R0 4 TIMES
:TO GET PROPER LEVEL
: CLEAR UNWANTED BITS
:SET UP VECTORS
:A VECTOR
:B VECTOR
:PRIORITY 7
:LOAD PORT4
:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
:SET BR REQUEST
:PUT LEVEL IN R2 IN PS
: IS PRESENT PS LEVEL = TO KMC LEVEL
: BR IF YES
:NO GET NEXT LOWER LEVEL IN R2
:AND CONTINUE WITH TEST
: ADVANCE LOOP
:ERROR UNEXPECTED INTERRUPT

```

4175 023644 000002

RTI

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4183

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4185

4186

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4229

4230

\*\*\*\*\* TEST 57 \*\*\*\*\*  
\*PRIORITY INTERRUPT TESTS  
\*SET PS TO ALL BR LEVELS LESS THAN THE KMC11 LEVEL  
\*VERIFY THAT THE KMC11 WILL INTERRUPT  
\*\*\*\*\*

TEST 57

\*\*\*\*\*  
TST57: SCOPE ; LOAD THE NO. OF THIS TEST  
MOV #57,STSNM ; POINT TO THE START OF NEXT TEST.  
MOV #T560,NEXT ; R1 CONTAINS BASE KMC11 ADDRESS  
MSTCLR ; MASTER CLEAR KMC11  
MOV #340,R2 ; PUT LEVEL 7 IN R2  
MOV R2,PS ; SET PRIORITY TO 7  
MOV STAT1,R0 ; GET BR LEVEL OF KMC11  
RSR R0 ; SHIFT R0 4 TIMES  
RSR R0 ; TO GET PROPER LEVEL  
RSR R0  
RSR R0  
BIC #177437,R0 ; CLEAR UNWANTED BITS  
MOV R0,R2 ; PUT KMC LEVEL IN R2  
SUB #40,R2 ; GET NEXT LOWER LEVEL IN R2  
JSR RS,SETVEC ; SET UP VECTORS  
; A VECTOR  
; B VECTOR  
; PRIORITY 7  
; LOAD PORT4  
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
; SET BR REQUEST  
MOV R2,PS ; PUT LEVEL IN R2 IN PS  
NOP  
ERROR 10 ; ERROR, NO INTERRUPT  
CMP #140,R2 ; IS IT DOWN TO LEVEL 3 YET?  
BEQ 15 ; YES, KMC DID NOT INTERRUPT, ERROR  
SUB #40,R2 ; PUT NEXT LOWER LEVEL IN R2  
BR 48 ; CONTINUE TEST  
ADVANCE ; ADVANCE LOOP  
MOV #68,(SP) ; SET UP FOR RTI  
RTI  
ERROR 11 ; ERROR, WRONG VECTOR  
MOV #68,(SP) ; SET UP FOR RTI  
RTI

\*\*\*\*\* TEST 60 \*\*\*\*\*  
\*NPR TEST  
\*TEST OF DATO, 1 WORD FROM UPROC TO 11 MEMORY  
\*\*\*\*\*

TEST 60

```

4231 024014 000004
4232 024016 012737 000060 001202
4233 024024 012737 024122 001442
4234
4235 024030 000005
4236 024032 005011
4237 024036 005061 000004
4238 024040 004537 035540
4239 024044 000000
4240 024048 177777
4241 024052 024120
4242 024056 024116
4243 024060 005037 024116 000004
4244 024064 012761 000021 000004
4245 024068 104412
4246 024072 121110
4247 024074 000240
4248 024076 012705 177777
4249 024100 013704 024116
4250 024106 020504
4251 024110 001401
4252 024112 104012
4253 024114 104420
4254 024116 000000
4255 024120 000000

```

```

*****
†ST60: SCOPE
MOV #60,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #ST61,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
RESET
BUS RESET
CLR (R1) ; CLEAR RUM
CLR 4(R1) ; CLR PORT4
JSR RS,NRSET ; SET UP IBUS REG 0-7
0 ; IN DATA
-1 ; OUT DATA
; IN BA
; OUT BA
CLR 28 ; CLEAR 28
MOV #21,4(R1) ; WRITE PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121110 ; SET NPR BITS IN IBUS* REG 11
NOP
MOV #1,RS ; PUT "EXPECTED" IN RS
MOV #2,RA ; PUT "FOUND" IN RA
CMP #5,RA ; DATA CORRECT?
BNC IF YES ; OR IF YES
ERROR NPR FAILED ; ERROR NPR FAILED
ADVANCE 12 ; ADVANCE LOOP
; OUT BA
; IN BA
45: 0
35: 0
36: 0

```

```

***** TEST 61 *****
#NPR TEST
*TEST OF DATA, 1 WORD FROM 11 MEMORY TO UPROC
*****

```

TEST 61

```

4267 024122 000004
4268 024124 012737 000061 001202
4269 024132 012737 024240 001442
4270
4271 024140 104410
4272 024142 005061 000004
4273 024146 004537 035540
4274 024152 000000
4275 024154 177777
4276 024158 024236
4277 024160 024234
4278 024162 012737 177777 024236
4279 024170 012761 000001 000004
4280 024176 104412
4281 024200 121110
4282 024202 000240
4283 024204 012705 177777
4284 024210 104412
4285 024212 021004
4286 024214 104412

```

```

*****
†ST61: SCOPE
MOV #61,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #ST62,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR 4(R1) ; CLR PORT4
JSR RS,NRSET ; SET UP IBUS REG 0-7
0 ; IN DATA
-1 ; OUT DATA
; IN BA
; OUT BA
MOV #1,35 ; PUT DATA IN 35
MOV #1,4(R1) ; WRITE PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121110 ; SET NPR BITS IN IBUS* REG 11
NOP
MOV #1,RS ; PUT "EXPECTED" IN RS
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
021004 ; MOVE IN DATA LOW BYTE TO PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

```

```

4297 024216 021025
4298 024220 016104 000004
4299 024224 020504
4300 024228 001401
4301 024230 104012
4302 024232 104420
4303 024234 000000
4304 024236 000000

```

```

021025
MOV 4(R1),R4
CMP R5,R4
BEQ 48
ERROR 12
ADVANCE
45: 0
25: 0
35: 0

```

```

MOVE IN DATA HIGH BYTE TO PORTS
PUT "FOUND" IN R4
DATA CORRECT?
OR IF YES
ERROR NPR FAILED
ADVANCE LOOP
OUT BA
IN BA

```

```

***** TEST 62 *****
NPR TEST
*TEST OF DATOB, 1 BYTE FROM UPROC TO 11 MEMORY
*****

```

TEST 62

```

4305 024240 000004
4306 024242 012737 000062 001202
4307 024250 012737 024344 001442
4308
4309 024256 104410
4310 024260 005061 000004
4311 024264 004537 035540
4312 024270 000000
4313 024272 177777
4314 024274 024342
4315 024276 024341
4316 024300 005037 024340
4317 024304 012761 000221 000004
4318 024312 104412
4319 024314 121110
4320 024316 000240
4321 024320 012705 177400
4322 024324 013704 024340
4323 024330 020504
4324 024332 001401
4325 024334 104012
4326 024336 104420
4327 024340 000000
4328 024342 000000
4329
4330
4331
4332
4333
4334
4335
4336
4337
4338
4339

```

```

TST62: SCOPE
MOV #62,$STSTM ; LOAD THE NO. OF THIS TEST
MOV #TST63,NEXT ; POINT TO THE START OF NEXT TEST.
NSTCLR ; R1 CONTAINS BASE KMC11 ADDRESS
CLR 4(R1) ; MASTER CLEAR KMC11
JSR R5,NPRSET ; CLR PORT4
0 ; SET UP IBUS REG 0-7
-1 ; IN DATA
-2 ; OUT DATA
-3 ; IN BA
-4 ; OUT BA
CLR 25 ; CLEAR 25
MOV #221,4(R1) ; WRITE PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121110 ; SET NPR BITS IN IBUS* REG 11
NOP
MOV #177400,R5 ; PUT "EVALUATED" IN R5
MOV 25,R4 ; PUT "FOUND" IN R4
CMP R5,R4 ; DATA CORRECT?
BEQ 48 ; OR IF YES
ERROR 12 ; ERROR NPR FAILED
ADVANCE ; ADVANCE LOOP
45: 0 ; OUT BA
25: 0 ; IN BA
35: 0

```

```

***** TEST 63 *****
*TEST OF EA BITS 16 AND 17
*DO A DATO TO AN ADDRESS USING OUT BA BITS 16 AND 17
*VERIFY CORRECT RESULTS
*****

```

TEST 63

```

4340 024344 000004
4341 024346 012737 000063 001202
4342 024354 012737 024502 001442

```

```

TST63: SCOPE
MOV #63,$STSTM ; LOAD THE NO. OF THIS TEST
MOV #TST64,NEXT ; POINT TO THE START OF NEXT TEST.

```

```


```

4343						MSTCLR			:R1 CONTAINS BASE KMC11 ADDRESS
4344	024362	104410				MOV	KMP04, 18		:MASTER CLEAR KMC11
4345	024364	013737	002074	024412		MOV	KMP04, 28		:USE SEL4 FOR ADDRESS
4346	024372	013737	002074	024410		JSR	RS, NPASET		:USE SEL4 FOR ADDRESS
4347	024400	004537	035540			0			:LOAD BA AND DATA
4348	024404	000000				125252			:IN DATA
4349	024406	125252				0			:OUT DATA
4350	024410	000000			2S:	0			:IN BA
4351	024412	000000			1S:	0			:OUT BA
4352	024414	012761	000014	000004		MOV	#14, 4(R1)		:LOAD SEL4 WITH OUT BA16 AND 17
4353	024420	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4354	024424	121111				121111			:SET OUTBA 16 AND 17
4355	024426	012761	000021	000004		MOV	#21, 4(R1)		:LOAD SEL4
4356	024434	012761	121110	000006		MOV	#121110, 6(R1)		:PUT INSTRUCTION IN SEL6
4357	024442	012711	003000			MOV	#BIT9:BIT10, (R1)		:SET CROM1 AND CROM0!!
4358	024446	052711	000400			BIS	#BIT8, (R1)		:CLOCK IT!
4359	024452	000240				NOP			:WAIT FOR NPR
4360	024454	012705	121110			MOV	#121110, R5		:PUT "EXPECTED" IN R5
4361	024460	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4362	024462	021044				021044			:MOVE OUT DATA L8 TO SEL4
4363	024464	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4364	024466	021065				021065			:MOVE OUT DATA H8 TO SEL5
4365	024470	016104	000004			MOV	4(R1), R4		:PUT "FOUND" IN R4
4366	024474	020504				CHP	RS, R4		:CORRECT RESULTS ?
4367	024476	001401				BEQ	35		:OR IF YES
4368	024500	104012				ERROR	12		:ERROR BA 16 AND 17 FAILED
4369	024502				3S:				

\*\*\*\*\* TEST 64 \*\*\*\*\*  
 : \*TEST OF EA BITS 16 AND 17  
 : \*DO A DATA USING IN BA BITS 16 AND 17  
 : \*VERIFY CORRECT RESULTS  
 : \*\*\*\*\*

TEST 64  
 :-----

4381	024502	000004				1ST64: SCOPE			: *****
4382	024504	012737	000064	001202		MOV	#64, 8STNH		: LOAD THE NO. OF THIS TEST
4383	024512	012737	024626	001442		MOV	#7ST65, NEXT		: POINT TO THE START OF NEXT TEST.
4384									:R1 CONTAINS BASE KMC11 ADDRESS
4385	024520	104410				MSTCLR			:MASTER CLEAR KMC11
4386	024522	013737	002074	024550		MOV	KMP04, 18		:USE SEL4 FOR ADDRESS
4387	024530	013737	002074	024546		MOV	KMP04, 28		:USE SEL4 FOR ADDRESS
4388	024536	004537	035540			JSR	RS, NPASET		:LOAD BA AND DATA
4389	024542	000000				0			:IN DATA
4390	024544	125252				125252			:OUT DATA
4391	024546	000000			2S:	0			:IN BA
4392	024550	000000			1S:	0			:OUT BA
4393	024562	012761	000015	000004		MOV	#15, 4(R1)		:LOAD SEL4
4394	024560	012761	121110	000006		MOV	#121110, 6(R1)		:PUT INSTRUCTION IN SEL6
4395	024566	012711	003000			MOV	#BIT9:BIT10, (R1)		:SET CROM1 AND CROM0!!
4396	024572	052711	000400			BIS	#BIT8, (R1)		:CLOCK IT!
4397	024576	000240				NOP			:WAIT FOR NPR
4398	024600	012705	121110			MOV	#121110, R5		:PUT "EXPECTED" IN R5

4399	024604	104412			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4400	024606	021004			021004		: MOVE IN DATA LB TO SEL4
4401	024610	104412			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4402	024612	021025			021025		: MOVE IN DATA HB TO SEL5
4403	024614	016104	000004		MOV	4(R1),R4	: PUT "FOUND" IN R4
4404	024620	020504			CMF	R5,R4	: CORRECT RESULTS ?
4405	024622	001401			BEG	38	: BR IF YES
4406	024624	104012			ERROR	12	: ERROR BA 16 AND 17 FAILED
4407	024626						

35:

```

***** TEST 65 *****
#NPR NON-EXISTENT MEMORY TEST
#DO A DATO TO A NON-EXISTENT ADDRESS
#VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
*****

```

TEST 65

4418					TEST65:	SCOPE		
4419	024626	000004			MOV	#65,STSTMM	: LOAD THE NO. OF THIS TEST	
4420	024630	012737	000065	001202	MOV	#1ST66,NEXT	: POINT TO THE START OF NEXT TEST.	
4421	024636	012737	024736	001442			: R1 CONTAINS BASE KMC11 ADDRESS	
4422					MSTCLR		: MASTER CLEAR KMC11	
4423	024644	104410			TSR	R5,NRSET	: LOAD IBUS REGISTERS 0-7	
4424	024646	004537	035540		0		: IN DATA	
4425	024652	000000			0		: OUT DATA	
4426	024654	000000			0		: IN BA	
4427	024656	177320			177320		: OUT BA	
4428	024660	177320			177320		: SET OUT BA BITS 16+17 IN PORT4	
4429	024662	012761	000014	000004	MOV	#14,4(R1)	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304	
4430	024670	104412			ROMCLK		: SET OUTBA 16 AND 17	
4431	024672	121111			121111		: SET NPR REQUEST BITS IN PORT4	
4432	024674	012761	000021	000004	MOV	#21,4(R1)	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304	
4433	024702	104412			ROMCLK		: NOV IBUS# 4 TO IBUS# 10	
4434	024704	121110			121110			
4435	024706	000240			MOV			
4436	024710	104412			ROMCLK		: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304	
4437	024712	121225			121225		: NOV IBUS#11 TO IBUS#5	
4438	024714	012705	000001		MOV	#1,R5	: PUT "EXPECTED" IN R5	
4439	024720	116104	000005		MOV#	5(R1),R4	: PUT "FOUND" IN R4	
4440	024724	042704	177776		BIC	#177776,R4	: CLEAR UNWANTED BITS	
4441	024730	020504			CMF	R5,R4	: DATA CORRECT?	
4442	024732	001401			BEG	18	: BR IF YES	
4443	024734	104012			ERROR	12	: ERROR NON-EXISTENT MEM BIT FAILED TO SET	
4444	024736							

15:

```

***** TEST 66 *****
#NPR NON-EXISTENT MEMORY TEST
#DO A DATI FROM A NON-EXISTENT ADDRESS
#VERIFY THAT THE NON-EXISTENT BIT SET IN IBUS REG 11
*****

```

TEST 66

4445  
4446  
4447  
4448  
4449  
4450  
4451  
4452  
4453  
4454

```

#455
#456 024736 000074
#457 024740 012737 000066 001202
#458 024746 012737 025044 001442
#459
#460 024754 104410
#461 024756 004537 035540
#462 024762 000000
#463 024764 000000
#464 024766 177320
#465 024770 177320
#466 024772 005061 000004
#467 024776 104412
#468 025000 121111
#469 025002 012761 000015 000004
#470 025010 104412
#471 025012 121110
#472 025014 000240
#473 025016 104412
#474 025020 121225
#475 025022 012705 000001
#476 025026 116104 000005
#477 025032 042704 177776
#478 025036 020504
#479 025040 001401
#480 025042 104012
#481 025044
#482
#483
#484
#485
#486
#487
#488
#489
#490
#491
#492
#493 025044 000004
#494 025046 012737 000067 001202
#495 025054 012737 000003 001310
#496 025062 012737 025244 001442
#497
#498 025070 104410
#499 025072 005037 025242
#500 025076 005000
#501 025100 012702 037234
#502 025104 010037 025134
#503 025110 010237 025140
#504 025114 032702 000001
#505 025120 001402
#506 025122 000337 025134
#507 025126 004537 035540
#508 025132 000000
#509 025134 000000
#510

```

```

*****
TST66: SCOPE
MOV #66,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #TST67,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
JSR R5,NPRSET ; LOAD NPR REGISTERS 0-7
0 ; IN DATA
0 ; OUT DATA
177320 ; IN BA
177320 ; OUT BA
CLR 4(R1)
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121111 ; CLEAR NON-EXISTENT BIT
MOV #15,4(R1) ; SET NPR REQUEST BITS IN PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121110 ; MOV IBUS# 4 TO IBUS# 10
NOP
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
121225 ; MOV IBUS#11 TO IBUS#5
MOV #1,R5 ; PUT "EXPECTED" IN R5
MOVB 5(R1),R4 ; PUT "FOUND" IN R4
BIC #17776,R4 ; CLEAR UNWANTED BITS
CMP R5,R4 ; DATA CORRECT?
BEQ 1$ ; BR IF YES
ERROR 12 ; ERROR NON-EXISTENT MEM BIT FAILED TO SET
1$:

```

```

***** TEST 67 *****
#NPR TEST
#USING DAT0, NPR A BINARY COUNT (0-377 )
#FROM MICRO-PROCESSOR TO ALL AVAILABLE MEMORY
*****

```

TEST 67

```

*****
TST67: SCOPE
MOV #67,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #83,$TIMES ; LOAD ITERATION COUNT
MOV #TST70,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR 5$ ; START FLAG AT 0
CLR R0 ; DATA
MOV #CORMAX,R2 ; ADDRESS
1$:
MOV R0,2$ ; LOAD DATA
MOV R2,4$ ; LOAD BA
BIT #810,R2 ; IS BA 000?
EQ 4$ ; BR IF NO
SWAB 2$ ; IF 000 PUT DATA IN HI-BYTE
JSR R5,NPRSET ; LOAD NPR REGISTERS
0 ; IN DATA
0 ; OUT DATA
2$:

```

```

4511 025136 006000
4512 025140 000000
4513 025140 105012
4514 025140 012761 000221 000004
4515 025140 104412
4516 025140 121110
4517 025140 000240
4518 025140 010005
4519 025140 111204
4520 025140 120504
4521 025140 001401
4522 025140 104021
4523 025140 104405
4524 025140 005200
4525 025140 012700 177400
4526 025140 005737 025242
4527 025140 001402
4528 025140 005700
4529 025140 001412
4530 025140 005202
4531 025140 023702 001466
4532 025140 001330
4533 025140 012702 037234
4534 025140 012737 177777 025242
4535 025140 000722
4536 025140 104420
4537 025242 000000
4538
4539
4540
4541
4542
4543
4544
4545
4546
4547
4548
4549
4550
4551
4552
4553
4554
4555
4556
4557
4558
4559
4560
4561
4562
4563
4564
4565
4566

```

```

45: 0
0
CLR B (R2)
MOV #221,4(R1)
ROMCLK
121110
NOP
MOV R0,R5
MOV B (R2),R4
CMP B R3,R4
BEQ 3$
ERROR 21
35: SCOPE1
INC R0
BIC #177400,R0
TST 5$
BEQ 6$
TST R0
BEQ 7$
65: INC R2
CMP MEM LIM,R2
BNE 1$
MOV #CORMAX,R2
MOV #-1,5$
75: ADVANCE
55: 0
: MEM1
: MEM0
: MEM2 1K
: MEM3 1K
: ***** TEST 70 *****
: HALU C BIT TEST
: *TEST THAT AN ADD OF 377 AND 377 WILL SET THE C BI?
: *****
: TEST 70
: -----
: *****
: TST70: SCOPE
MOV #70,STSTM ; LOAD THE NO. OF THIS TEST
MOV #TST71,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
: R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
JSR PC,MEMLD ; LOAD MAINMEM DATA
TDATA ; POINTER TO DATA
JSR PC,SPLD ; LOAD SP DATA
TDATA ; POINTER TO DATA
1$: ROMCLK
010000 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; MAR+0

```

```

: IN BA
: OUT BA
: CLEAR MEMORY LOCATION
: LOAD PORT4
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: DO THE NPR
: PUT "EXPECTED" IN R5
: PUT "FOUND" IN R4
: IS DATA CORRECT?
: BR IF YES
: ERROR, DATA INCORRECT
: NEXT CHARACTER
: USE ONLY LOW BYTE
: HAS MAX MEMORY BEEN REACHED YET?
: BR IF NO
: DONE PATTERN?
: BR IF YES
: INC BA
: REACHED MEMORY LIMIT YET?
: BR IF NOT
: RESTART BA AT FIRST ADDRESS
: SET FLAG TO END TEST AT END OF DATA PATTERN
: CONTINUE
: ADVANCE LOOP
: THIS LOCATION IS A FLAG. IT STARTS AT 0
: AND IS SET TO -1 WHEN LAST MEMORY ADDRESS
: IS USED, TEST IS THEN ENDED WHEN PATTERN IS FINISHED

```



```

4567 025312 104412
4568 025314 054400
4569 025316 104412
4570 025318 040401
4571 025320 104412
4572 025322 061224
4573 025324 012705 000001
4574 025326 016104 000004
4575 025328 120504
4576 025330 001401
4577 025332 104015
4578 025334 104405
4579 025336 104420
4580 025338 377 000
4581 025340 000 000
4582 025356 000 000
4583
4584
4585
4586
4587
4588
4589
4590
4591
4592
4593
4594
4595
4596
4597 025360 000004
4598 025362 012737 000071 001202
4599 025370 012737 025536 001442
4600 025376 012737 025430 001444
4601
4602 025404 104410
4603 025406 005000
4604 025410 012702 025526
4605 025414 004737 035602
4606 025420 035726
4607 025422 004737 035636
4608 025426 035736
4609 025430 004737 035702
4610 025434 042737 000017 025450
4611 025442 050037 025450
4612 025446 104412
4613 025450 010000
4614 025452 042737 000017 025466
4615 025460 050037 025466
4616 025464 104412
4617 025466 040620
4618 025470 104412
4619 025472 061224
4620 025474 111205
4621 025476 116104 000004
4622 025502 120504

```

```

ROMCLK
054400!<0*20>
ROMCLK
040401!<1*20>
ROMCLK
61224
MOV 81,R5
MOV 4(R1),R4
CMPB R5,R4
BEQ 28
ERROR 15
SCOPI
ADVANCE
TDATA: .BYTE -1,0,0,0,0,0,0,0
.EVEN

```

```

NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
ADD 377 AND 377, TO SET C BIT
NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
ADD 0 AND 0 AND THE C BIT
NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
PUT RESULTS IN PORT4
PUT "EXPECTED" IN R5
PUT "FOUND" IN R4
DATA CORRECT?
BR IF YES
ERROR C BIT NOT SET
SMO=1?
ADVANCE LOOP

```

```

***** TEST 71 *****
*ALU TEST
*TEST OF ALU FUNCTION SEL B WITH C BIT CLEARED
*ALU FUNCTION (B) CODE=11
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 71

```

*****
TST71: SCOPE
MOV 871,STSTIM ; LOAD THE NO. OF THIS TEST
MOV 8TST72,NEXT ; POINT TO THE START OF NEXT TEST.
MOV 8IS,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEN + SP ADDRESS
MOV R5,R2 ; POINTER TO CORRECT DATA
JSR PC,NEHD ; LOAD 8 WORDS OF MAIN MEMORY
MENDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
JSR PC,CLRC ; CLEAR C BIT!
BIC 81,28 ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,28 ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MAIN
BIC 817,38 ; CLEAR ADDRESS OF INSTRUCTION
BIS R0,38 ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040400!<11*20> ; BR + SEL B
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE BR TO PORT4
MOV8 (R2),R5 ; PUT "EXPECTED" IN R5
MOV8 4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?

```

```

#623 025504 001401 BEQ 4$ : BR IF YES
#624 025506 104015 ERROR 15 : ALU ERROR
#625 025510 104405 SCOPI 4$ : SMO9=1?
#626 025512 005202 INC R2 : NEXT DATA
#627 025514 005200 INC R0 : NEXT ADDRESS
#628 025516 022700 000010 CMP #10,R0 : DONE YET?
#629 025522 001342 BNE 1$ : BR IF NO
#630 025524 104420 ADVANCE : ADVANCE LOOP
#631 025526 000 377 000 5$: .BYTE 0,-1,0,-1,125,252,125,252
#632 025531 377 125 252
#633 025534 125 252

```

.EVEN

```

***** TEST 72 *****
*ALU TEST
*TEST OF ALU FUNCTION SEL A WITH C BIT CLEARED
*ALU FUNCTION (A) CODE=10
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 72

```

#644 025536 000004 tst72: SCOPE
#645 025540 012737 000072 001202 MOV #72,BSTNM : LOAD THE NO. OF THIS TEST
#646 025546 012737 025714 001442 MOV #TST73,NEXT : POINT TO THE START OF NEXT TEST.
#647 025554 012737 025606 001444 MOV #1$,LOCK : ADDRESS FOR LOCK ON DATA.
#648 025562 104410 NSTCLR : R1 CONTAINS BASE KNC11 ADDRESS
#649 025564 005000 CLR R0 : MASTER CLEAR KNC11
#650 025566 012702 025704 MOV #5$,R2 : MEM + SP ADDRESS
#651 025572 004737 035602 JSR PC,NEALD : POINTER TO CORRECT DATA
#652 025576 035726 MENDAT : LOAD 8 WORDS OF MAIN MEMORY
#653 025580 004737 035636 JSR PC,SPLD : POINTER TO DATA
#654 025584 025736 SPDAT : LOAD 8 WORDS OF SP
#655 025586 004737 035702 1$: JSR PC,CLAC : POINTER TO DATA
#656 025592 012737 000017 025626 BIC #17,$S : CLEAR C BIT!
#657 025594 000017 025626 BIC #0,$S : CLEAR ADDRESS FIELD OF INSTRUCTION
#658 025596 104412 ROMCLK : ADD ADDRESS TO INSTRUCTION
#659 025598 010000 2$: 010000 : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
#660 025600 012737 000017 025644 BIC #17,$S : LOAD MEM
#661 025602 050007 025644 BIC #0,$S : CLEAR ADDRESS OF INSTRUCTION
#662 025604 104412 ROMCLK : ADD ADDRESS TO INSTRUCTION
#663 025606 061224 3$: 061224 : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
#664 025608 040600 BR + SEL A
#665 025610 104412 ROMCLK : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
#666 025612 061224 MOVE BR TO PORT4
#667 025614 111205 MOVB (R2),R5 : PUT "EXPECTED" IN R5
#668 025616 116104 000004 MOVB 4(R1),R4 : PUT "FOUND" IN R4
#669 025618 120504 CMPB R5,R4 : DATA CORRECT?
#670 025620 001401 BEQ 4$ : BR IF YES
#671 025622 104015 ERROR 15 : ALU ERROR
#672 025624 104405 SCOPI 4$ : SMO9=1?
#673 025626 005202 INC R2 : NEXT DATA
#674 025628 005200 INC R0 : NEXT ADDRESS

```

```

4679 025704 022700 000010      CMP    #10,R0      :DONE YET?
4680 025700 001342      BNE    1$         :BR IF NO
4681 025702 104420      ADVANCE          :ADVANCE LOOP
4682 025704      000      000      377 5$: .BYTE 0,0,-1,-1,125,125,252,252
4683 025707      377      125      125
4684 025712      252      252

```

.EVEN

\*\*\*\*\* TEST 73 \*\*\*\*\*

```

:ALU TEST
:TEST OF ALU FUNCTION A OR NOTB WITH C BIT CLEARED
:ALU FUNCTION (A OR NOTB) CODE=12
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

TEST 73

```

4698
4699
4700 025714 000004      1$T73: SCOPE
4701 025716 012737 000073 001202      MOV    #73,$ST7M      :LOAD THE NO. OF THIS TEST
4702 025724 012737 026072 001442      MOV    #ST74,NEXT    :POINT TO THE START OF NEXT TEST.
4703 025732 012737 025764 001444      MOV    #1$,LOCK      :ADDRESS FOR LOCK ON DATA.
4704 025740 104410      R1 CONTAINS BASE KMC11 ADDRESS
4705 025742 005000      MSTRCLR          :MASTER CLEAR KMC11
4706 025744 012702 026062      CLR    R0         :MEM + SP ADDRESS
4707 025750 004737 035602      MOV    #5$,R2      :POINTER TO CORRECT DATA
4708 025754 035726      JSR    PC,NEARLD  :LOAD 8 WORDS OF MAIN MEMORY
4709 025756 004737 035636      MENDAT          :POINTER TO DATA
4710 025762 035736      JSR    PC,SPLD    :LOAD 8 WORDS OF SP
4711 025764 004737 035702 1$: SPDAT          :POINTER TO DATA
4712 025770 042737 000017 026004      JSR    PC,CLRC    :CLEAR C BIT!
4713 025776 050037 026004      BIC    #17,2$     :CLEAR ADDRESS FIELD OF INSTRUCTION
4714 026002 104412      BIS    R0,2$     :ADD ADDRESS TO INSTRUCTION
4715 026004 010000      ROMCLK          :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4716 026006 042737 000017 026022 2$: 010000          :LOAD MEM
4717 026014 050037 026022      BIC    #17,3$     :CLEAR ADDRESS OF INSTRUCTION
4718 026020 104412      BIS    R0,3$     :ADD ADDRESS TO INSTRUCTION
4719 026022 040640      ROMCLK          :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4720 026024 104412      ROMCLK          :BR + A OR NOTB
4721 026026 061224      ROMCLK          :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4722 026030 111205      61224          :MOVE BR TO PORT4
4723 026032 116104 000004      MOVB   (R2),R5    :PUT "EXPECTED" IN R5
4724 026036 120504      MOVB   4(R1),R4   :PUT "FOUND" IN R4
4725 026040 001401      CMPB   R5,R4      :DATA CORRECT?
4726 026042 104015      BEQ    4$         :BR IF YES
4727 026044 104405      ERROR   1$       :ALU ERROR
4728 026046 005212      SCOPI          :SMD9=1?
4729 026050 005200      INC    R2         :NEXT DATA
4730 026052 022700 000010      INC    R0         :NEXT ADDRESS
4731 026056 001342      CMP    #10,R0     :DONE YET?
4732 026060 104420      BNE    1$         :BR IF NO
4733 026062      377      000      377 5$: .BYTE -1,0 -1,-1,-1,125,252,-1
4734 026065      377      377      125

```

4735 026070 252 377

.EVEN

\*\*\*\*\* TEST 74 \*\*\*\*\*  
\*ALU TEST  
\*TEST OF ALU FUNCTION A AND B WITH C BIT CLEARED  
\*ALU FUNCTION (A AND B) CODE=13  
\*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
\*PERFORM THE FUNCTION, VERIFY THE RESULTS  
\*\*\*\*\*

TEST 74

```

*****
TST74: SCOPE
MOV #74,STSTM          ; LOAD THE NO. OF THIS TEST
MOV #TST75,NEXT        ; POINT TO THE START OF NEXT TEST.
MOV #18,LOCK           ; ADDRESS FOR LOCK ON DATA.

; R1 CONTAINS BASE KMC11 ADDRESS
; MASTER CLEAR KMC11
; MEM + SP ADDRESS
; POINTER TO CORRECT DATA
; LOAD 8 WORDS OF MAIN MEMORY
; POINTER TO DATA
; LOAD 8 WORDS OF SP
; POINTER TO DATA
1$: JSR PC,CLRC         ; CLEAR C BIT!
    BIC #17,28         ; CLEAR ADDRESS FIELD OF INSTRUCTION
    BIS #0,28          ; ADD ADDRESS TO INSTRUCTION
    ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
    ; LOAD MEM
    ; CLEAR ADDRESS OF INSTRUCTION
    ; ADD ADDRESS TO INSTRUCTION
    ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
    ; R2 = A AND B
    ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
    ; MOVE BR TO PORT4
    ; PUT -EXPECTED- IN R5
    ; PUT -FOUND- IN R4
    ; DATA CORRECT?
    ; BR IF YES
    ; ALU ERROR
    ; STOP-1?
    ; NEXT DATA
    ; NEXT ADDRESS
    ; DONE YET?
    ; BR IF NO
    ; ADVANCE LOOP
2$: ROMCLK 010000
    BIC #17,38         ; CLEAR ADDRESS OF INSTRUCTION
    BIS #0,38          ; ADD ADDRESS TO INSTRUCTION
    ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
    ; MOVE BR TO PORT4
    ; PUT -EXPECTED- IN R5
    ; PUT -FOUND- IN R4
    ; DATA CORRECT?
    ; BR IF YES
    ; ALU ERROR
    ; STOP-1?
    ; NEXT DATA
    ; NEXT ADDRESS
    ; DONE YET?
    ; BR IF NO
    ; ADVANCE LOOP
3$: ROMCLK 040400!(<13*20>)
    MOV #61224,R5      ; (R2),R5
    MOV #4(R1),R4      ; 4(R1),R4
    CMP #R5,R4         ; R5,R4
    BEQ #48            ; 48
    ; ERROR
    ; 15
    ; SCOPI
    ; INC R2
    ; INC R0
    ; CMP #10,R0
    ; BNE 15
    ; ADVANCE
5$: .BYTE 0,0,0,-1,125,0,0,252

;*****

```

4787  
4788  
4789  
4790

.EVEN

\*\*\*\*\* TEST 75 \*\*\*\*\*

```

4791
4792
4793
4794
4795
4796
4797
4798
4799
4800
4801 026250 000004
4802 026252 012737 000075 001202
4803 026254 012737 026426 001442
4804 026256 012737 026320 001444
4805
4806 026274 104410
4807 026276 005000
4808 026300 012702 026416
4809 026304 004737 035602
4810 026310 035726
4811 026312 004737 035636
4812 026316 035736
4813 026320 004737 035702
4814 026324 042737 000017 026340
4815 026332 050037 026340
4816 026336 104412
4817 026340 010000
4818 026342 042737 000017 026356
4819 026350 050037 026356
4820 026354 104412
4821 026356 040700
4822 026360 104412
4823 026362 061224
4824 026364 111205
4825 026366 116104 000004
4826 026372 120504
4827 026374 001401
4828 026376 104015
4829 026400 104405
4830 026402 005202
4831 026404 005200
4832 026406 022700 000010
4833 026412 001342
4834 026414 104420
4835 026416 000 377 377
4836 026421 377 125 377
4837 026424 377 252

```

```

: *ALU TEST
: *TEST OF ALU FUNCTION A OR B WITH C BIT CLEARED
: *ALU FUNCTION (A OR B) CODE=14
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

TEST 75

```

: *****
: TST75: SCOPE
: MOV #75,STSTNM ; LOAD THE NO. OF THIS TEST
: MOV #TST76,NEXT ; POINT TO THE START OF NEXT TEST.
: MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.
: R1 CONTAINS BASE KMC11 ADDRESS
: MSTRCLR ; MASTER CLEAR KMC11
: CLR RO ; MEM + SP ADDRESS
: MOV #58,R2 ; POINTER TO CONNECT DATA
: JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
: MEMDAT ; POINTER TO DATA
: JSR PC,SPLD ; LOAD 8 WORDS OF SP
: SPDAT ; POINTER TO DATA
: JSR PC,CLRC ; CLEAR C BIT!
: BIC #17,25 ; CLEAR ADDRESS FIELD OF INSTRUCTION
: BIS RO,25 ; ADD ADDRESS TO INSTRUCTION
: ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: O10000 ; LOAD RAR
: BIC #17,35 ; CLEAR ADDRESS OF INSTRUCTION
: BIS RO,35 ; ADD ADDRESS TO INSTRUCTION
: ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: O40400:(14*20) ; BR = A OR B
: ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: 61224 ; MOVE BR TO PORT4
: MOVB (R2),R5 ; PUT "EXPECTED" IN R5
: MOVB 4(R1),R4 ; PUT "FOUND" IN R4
: CNPB R5,R4 ; DATA CORREC.?
: BEQ 48 ; BR IF YES
: ERROR 15 ; ALU ERROR
: SCOP1 ; SMO=1?
: INC R2 ; NEXT DATA
: INC RO ; NEXT ADDRESS
: CNP #10,RO ; DONE YET?
: BNE 18 ; BR IF NO
: ADVANCE ; ADVANCE LOOP
: .BYTE 0,-1,-1,-1,125,-1,-1,252

```

\*\*\*\*\* TEST 76 \*\*\*\*\*

```

4841
4842 : *ALU TEST
4843 : *TEST OF ALU FUNCTION A XOR B WITH C BIT CLEARED
4844 : *ALU FUNCTION (A XOR B) CODE=15
4845 : *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
4846 : *PERFORM THE FUNCTION, VERIFY THE RESULTS

```

```

4847
4848
4849
4850
4851
4852 026426 000004
4853 026430 012737 000076 001202
4854 026436 012737 026604 001442
4855 026444 012737 026476 001444
4856
4857 026452 104410
4858 026454 005000
4859 026456 012702 026574
4860 026462 004737 035602
4861 026466 035726
4862 026470 004737 035636
4863 026474 035736
4864 026476 004737 035702
4865 026502 042737 000017 026516
4866 026510 050037 026516
4867 026514 104412
4868 026516 010000
4869 026520 042737 000017 026534
4870 026526 050037 026534
4871 026532 104412
4872 026534 040720
4873 026536 104412
4874 026540 061224
4875 026542 111205
4876 026544 116104 000004
4877 026550 120504
4878 026552 001401
4879 026554 104015
4880 026556 104405
4881 026560 005202
4882 026562 005200
4883 026564 022700 000010
4884 026570 001342
4885 026572 104420
4886 026574 000 377 377
4887 026577 000 000 377
4888 026602 377 000
4889
4890
4891
4892
4893
4894
4895
4896
4897
4898
4899
4900
4901
4902

```

TEST 76

```

*****
:
: TEST 76
:-----
*****
15: SCOPE
MOV #76, $STSTM ; LOAD THE NO. OF THIS TEST
MOV #ST77, NEXT ; POINT TO THE START OF NEXT TEST.
MOV #15, LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
; MASTER CLEAR KMC11
; MEM + SP ADDRESS
; POINTER TO CORRECT DATA
; LOAD 8 WORDS OF MAIN MEMORY
; POINTER TO DATA
; LOAD 8 WORDS OF SP
; POINTER TO DATA
; CLEAR C BIT!
; CLEAR ADDRESS FIELD OF INSTRUCTION
; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
25: ROMCLK 010000
; LOCK NAR
; CLEAR ADDRESS OF INSTRUCTION
; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
35: ROMCLK 040400! (15*20)
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; MOVE BR TO PORT4
; PUT "EXPECTED" IN R5
; PUT "FOUND" IN R4
; DATA CORRECT?
; BR IF YES
; ALU ERROR
45: SCOPE1
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10, R0 ; DONE YET?
BNE 15 ; BR IF NO
ADVANCE ; ADVANCE LOOP
55: .BYTE 0, -1, -1, 0, 0, -1, -1, 0
;
; .EVEN

```

TEST 77

```

*****
:
: *ALU TEST
: *TEST OF ALU FUNCTION ADD WITH C BIT CLEARED
: *ALU FUNCTION (A PLUS B) CODE=00
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
:
: *****

```

TEST 77

```

*****
:
:
: *****

```

```

4903 026604 000004          TST77: SCOPE
4904 026606 012737 000077 001202  MOV      #77,$STSTM          ; LOAD THE NO. OF THIS TEST
4905 026614 012737 026762 001442  MOV      $TST100,NEXT      ; POINT TO THE START OF NEXT TEST.
4906 026622 012737 026654 001444  MOV      #18,LOCK          ; ADDRESS FOR LOCK ON DATA.
4907                                     ; R1 CONTAINS BASE KMC11 ADDRESS
4908 026630 104410          MSTCLR  MASTER CLEAR KMC11
4909 026632 005000          CLR      R0                ; MEM + SP ADDRESS
4910 026634 012702 026752          MOV      #53,R2           ; POINTER TO CORRECT DATA
4911 026640 004737 035602          JSR      PC,NEMLD         ; LOAD 8 WORDS OF MAIN MEMORY
4912 026644 035726          MENDAT  POINTER TO DATA
4913 026646 004737 035636          JSR      PC,SPLD          ; LOAD 8 WORDS OF SP
4914 026648 035736          SPOAT   POINTER TO DATA
4915 026654 004737 035702 15:      JSR      PC,CLRC          ; CLEAR C BIT!
4916 026660 026737 000017 026674  BIC      #17,25           ; CLEAR ADDRESS FIELD OF INSTRUCTION
4917 026666 050037 026674          BIS      R0,25           ; ADD ADDRESS TO INSTRUCTION
4918 026672 104412          ROMCLK  NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4919 026674 010000          010000 25:      LOAD MAR
4920 026676 026737 000017 026712  BIC      #17,35           ; CLEAR ADDRESS OF INSTRUCTION
4921 026704 050037 026712          BIS      R0,35           ; ADD ADDRESS TO INSTRUCTION
4922 026710 104412          ROMCLK  NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4923 026712 040400          040400! <00#20> 35:      BR + ADD
4924 026714 104412          ROMCLK  NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4925 026716 061224          61224          MOVE    BR TO PORT4
4926 026720 111205          MOV8    (R2),R5           ; PUT "EXPECTED" IN R5
4927 026722 116104 000004          MOV8    4(R1),R4         ; PUT "FOUND" IN R4
4928 026726 120504          CMP8    R5,R4           ; DATA CORRECT?
4929 026730 001401          BEQ     #45              ; BR IF YES
4930 026732 104415          ERROR  15              ; ALU ERROR
4931 026734 104405          SCOPE  45:      SMOV=1?
4932 026736 005202          INC     R2              ; NEXT DATA
4933 026740 005200          INC     R3              ; NEXT ADDRESS
4934 026742 022700 000010          CMP     #10,R0          ; DONE YET?
4935 026746 001342          BNE     #58              ; BR IF NO
4936 026750 104420          ADVANCE ; ADVANCE LOOP
4937 026752          000          377          377 58:      .BYTE 0,-1,-1,376,252,-1,-1,124
4938 026756          376          377
4939 026760          377          124
4940                                     .EVEN

```

```

***** TEST 100 *****
;ALU TEST
;TEST OF ALU FUNCTION 2A W/C WITH C BIT CLEARED
;ALU FUNCTION (A PLUS A PLUS C) CODE=6
;LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
;PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

```

TEST 100
*****
;TST100: SCOPE
MOV      #100,$STSTM          ; LOAD 100
MOV      $TST101,NEXT        ; POINT
MOV      #18,LOCK            ; ADDRESS
;R1 CONTAINS BASE

```

4959	027006	104410				MSTCLR		MASTER CLEAR KMC11
4960	027010	005000				CLR	R0	MEM + SP ADDRESS
4961	027012	012702	027130			MOV	R55,R2	POINTER TO CORRECT DATA
4962	027016	004737	035602			JSR	PC, MEMLD	LOAD 8 WORDS OF MAIN MEMORY
4963	027022	035726				MEMDAT		POINTER TO DATA
4964	027024	004737	035636			JSR	PC, SPLD	LOAD 8 WORDS OF SP
4965	027030	035736				SPORT		POINTER TO DATA
4966	027032	004737	035702			JSR	PC, CLRC	CLEAR C BIT!
4967	027036	042737	000017	027052	18:	BIC	R0, 28	CLEAR ADDRESS FIELD OF INSTRUCTION
4968	027044	050037	027052			BIS	R0, 28	ADD ADDRESS TO INSTRUCTION
4969	027050	104412				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4970	027052	010000			25:	010000		LOAD MEM
4971	027054	042737	000017	027070		BIC	R0, 38	CLEAR ADDRESS OF INSTRUCTION
4972	027062	050037	027070			BIS	R0, 38	ADD ADDRESS TO INSTRUCTION
4973	027066	104412				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4974	027070	040540			35:	040540 (<6420>		MEM + SP A/C
4975	027072	104412				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4976	027074	061224				MOV	R0, R0	MOVE R0 TO PORTA
4977	027076	111205				MOV	(R2), R5	PUT "EXPECTED" IN R5
4978	027100	116104	000004			MOV	4(R1), R4	PUT "FOUND" IN R4
4979	027104	120504				CHP	R5, R4	DATA CORRECT?
4980	027106	001401				BEQ	R5, R4	BR IF YES
4981	027110	104415				ERROR	R5	ALU ERROR
4982	027112	104405			45:	SCOPE		SCOPE-1!
4983	027114	005202				INC	R0	NEXT DATA
4984	027116	005200				INC	R0	NEXT ADDRESS
4985	027120	022700	000110			CHP	R10, R0	DONE YET?
4986	027124	001342				BNE	R5	BR IF NO
4987	027126	104420				ADVANCE		ADVANCE LOOP
4988	027130	000	100	376	58:	.BYTE	0,0,376,376,252,252,124,124	
4989	027133	376	252	252				
4990	027136	124	124					
4991						.EVEN		
4992								
4993								
4994								
4995								
4996								
4997								
4998								
4999								
5000								
5001								
5002								
5003								
5004								
5005	027140	000004				TEST101: SCOPE		
5006	027142	012737	000101	001202		MOV	#101, R1STNUM	LOAD THE NO. OF THIS TEST
5007	027150	012737	027316	001442		MOV	#1ST102, NEXT	POINT TO THE START OF NEXT TEST.
5008	027156	012737	027210	001444		MOV	#18, LOCK	ADDRESS FOR LOCK ON DATA.
5009								R1 CONTAINS BASE KMC11 ADDRESS
5010	027164	104410				MSTCLR		MASTER CLEAR KMC11
5011	027166	005000				CLR	R0	MEM + SP ADDRESS
5012	027170	012702	027306			MOV	R55,R2	POINTER TO CORRECT DATA
5013	027174	004737	035602			JSR	PC, MEMLD	LOAD 8 WORDS OF MAIN MEMORY
5014	027200	035726				MEMDAT		POINTER TO DATA



5015	027202	004737	035636			JSR	PC, SPLD	LOAD 8 WORDS OF SP
5016	027206	035736				SPDAT		POINTER TO DATA
5017	027210	004737	035702	15:		JSR	PC, CLRC	CLEAR C BIT!
5018	027214	042737	000017	027230		BIC	R17, 25	CLEAR ADDRESS FIELD OF INSTRUCTION
5019	027222	050037	027230			BIS	R0, 25	ADD ADDRESS TO INSTRUCTION
5020	027226	104412				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5021	027230	010000		25:		010000		LOAD RAR
5022	027238	042737	000017	027246		BIC	R17, 35	CLEAR ADDRESS OF INSTRUCTION
5023	027240	050037	027246			BIS	R0, 35	ADD ADDRESS TO INSTRUCTION
5024	027244	104412				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5025	027246	040740		35:		040740! (16*20)		BR + SUB
5026	027250	104412				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5027	027252	061224				61224		MOVE BR TO PORT4
5028	027254	111205				NOVB	(R2), R5	PUT "EXPECTED" IN R5
5029	027256	116104	000004			NOVB	4(R1), R4	PUT "FOUND" IN R4
5030	027258	120504				CMPB	R5, R4	DATA CORRECT?
5031	027264	001401				BFC	46	BR IF YES
5032	027266	104015				ERROR	15	ALL ERROR
5033	027270	104405		45:		SCOPI		SUB-1?
5034	027272	005202				INC	R2	NEXT DATA
5035	027274	005200				INC	R0	NEXT ADDRESS
5036	027276	022700	000010			CMF	R10, R0	DONE YET?
5037	027302	001342				BNE	15	BR IF NO
5038	027304	104420				ADVANCE		ADVANCE LOOP
5039	027306	000	001	377	55:	.BYTE	0, 1, -1, 0, 0, 253, 125, 0	
5040	027311	000	000	253				
5041	027314	125	000					
5042								.EVEN

```

***** TEST 102 *****
:ALU TEST
:TEST OF ALU FUNCTION ADD W/C WITH C BIT CLEARED
:ALU FUNCTION (A PLUS B PLUS C) CODE=01
:LOAD MAIN MEN AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

TEST 102

5056	027316	000004				TEST102: SCOPE		
5057	027320	012737	000102	001202		MOV	R102, RSTIM	LOAD THE NO. OF THIS TEST
5058	027326	012737	027474	001049		MOV	RST103, NEXT	POINT TO THE START OF NEXT TEST.
5059	027334	012737	027366	001444		MOV	R18, LOCK	ADDRESS FOR LOCK ON DATA.
5060								R1 CONTAINS BASE KMC11 ADDRESS
5061	027342	104410				INSTCLR		MASTER CLEAR KMC11
5062	027344	005000				CLR	R0	MEN + SP ADDRESS
5063	027346	012702	027464			MOV	R65, R2	POINTER TO CORRECT DATA
5064	027352	004737	035602			JSR	PC, MENLD	LOAD 8 WORDS OF MAIN MEMORY
5065	027356	035736				MEMDAT		POINTER TO DATA
5066	027360	004737	035636			JSR	PC, SPLD	LOAD 8 WORDS OF SP
5067	027364	035736				SPDAT		POINTER TO DATA
5068	027366	004737	035702	027406	15:	JSR	PC, CLRC	CLEAR C BIT!
5069	027372	042737	000017			BIC	R17, 25	CLEAR ADDRESS FIELD OF INSTRUCTION
5070	027400	050037	027406			BIS	R0, 25	ADD ADDRESS TO INSTRUCTION

5071	027404	104412					ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5072	027406	010000			2S:		010000		:LOAD MAIN
5073	027410	042737	000017	027424			BIC	#17,3S	:CLEAR ADDRESS OF INSTRUCTION
5074	027416	050037	027424				BIS	RD,3S	:ADD ADDRESS TO INSTRUCTION
5075	027422	104412					ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5076	027424	040420			3S:		040420	(01#20)	:M/C
5077	027426	104412					ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5078	027430	061224					61224		:MOVE IN TO PORT4
5079	027432	111205					MOV	(R2),R5	:PUT "EXPECTED" IN R5
5080	027434	116104	0000G4				MOV	4(R1),R4	:PUT "FOUND" IN R4
5081	027440	130504					CMP	R5,R4	:DATA CORRECT?
5082	027442	001401					BEQ		:BR IF YES
5083	027444	104015					ERROR	IS	:ALU ERROR
5084	027446	104405			4S:		SCOPI		:SCOPI
5085	027450	005202					INC	R2	:NEXT DATA
5086	027452	005200					INC	RD	:NEXT ADDRESS
5087	027454	022700	000010				CMP	#10,R0	:DONE YET?
5088	027460	001342					BNE	IS	:BR IF NO
5089	027462	104420					ADVANCE		:ADVANCE LOOP
5090	027464	000	377	377	5S:		.BYTE	0,-1,-1,376,252,-1,-1,124	
5091	027467	376	252	377					
5092	027472	377	124						
5093									:.EVEN

```

***** TEST 103 *****
: *ALU TEST
: *TEST OF ALU FUNCTION SUB W/C WITH C BIT CLEARED
: *ALU FUNCTION (A-B-C) CODE=2
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

```

: TEST 103
: *****
: *****
TST103: SCOPE
MOV #103,STSTM ; LOAD THE NO. OF THIS TEST
MOV #STSTM,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #IS,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
: *MASTER CLEAR KMC11
: *MEM + SP ADDRESS
: *POINTER TO CORRECT DATA
: *LOAD 8 WORDS OF MAIN MEMORY
: *POINTER TO DATA
: *LOAD 8 WORDS OF SP
: *POINTER TO DATA
: *CLEAR C BIT!
: *CLEAR ADDRESS FIELD OF INSTRUCTION
: *ADD ADDRESS TO INSTRUCTION
: *NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: *LOAD MAIN
: *CLEAR ADDRESS OF INSTRUCTION
: *ADD ADDRESS TO INSTRUCTION
: *NEXT WORD IS INSTRUCTION ROMCLK PC=5304

```

5107	027474	000004					SCOPE		
5108	027476	012737	000103	001202			MOV	#103,STSTM	
5109	027504	012737	027652	001442			MOV	#STSTM,NEXT	
5110	027512	012737	027544	001444			MOV	#IS,LOCK	
5111									
5112	027520	104410					MSTCLR		
5113	027522	005000					CLR	R0	
5114	027524	012702	027642				MOV	#SS,R2	
5115	027530	004737	035602				JSR	PC,NEMLD	
5116	027534	035726					MEMDAT		
5117	027536	004737	035636				JSR	PC,SPLD	
5118	027542	035736					SPDAT		
5119	027544	004737	035702		1S:		JSR	PC,CLRC	
5120	027550	042737	000017	027564			BIC	#17,2S	
5121	027556	050037	027564				BIS	RD,2S	
5122	027562	104412					ROMCLK		
5123	027564	010000			2S:		010000		
5124	027566	042737	000017	027602			BIC	#17,3S	
5125	027574	050037	027602				BIS	RD,3S	
5126	027600	104412					ROMCLK		

5127	027602	040440		3\$:	040400!(<2*20)		BR + SUB W/C
5128	027604	104412			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5129	027606	061224			61224		:MOVE BR TO PORT4
5130	027610	111205			MOVB (R2),R5		:PUT "EXPECTED" IN R5
5131	027612	116104	000004		MOVB 4(R1),R4		:PUT "FOUND" IN R4
5132	027616	120504			CMPB R5,R4		:DATA CORRECT?
5133	027620	001401			BEQ 4\$		:BR IF YES
5134	027622	104015			ERROR 15		:ALU ERROR
5135	027624	104405		4\$:	SCOPI		:SHOW=1?
5136	027626	005202			INC R2		:NEXT DATA
5137	027630	005200			INC R0		:NEXT ADDRESS
5138	027632	022700	000010		CMP #10,R0		:DONE YET?
5139	027636	001342			BNE 1\$		:BR IF NO
5140	027640	104420			ADVANCE		:ADVANCE LOOP
5141	027642	377	000	376	.BYTE -1,0,376,-1,-1,252,124,-1		
5142	027645	377	377	252			
5143	027650	124	377				
5144					.EVEN		

```

***** TEST 104 *****
#ALU TEST
#TEST OF ALU FUNCTION INC A WITH C BIT CLEARED
#ALU FUNCTION (A PLUS 1) CODE=3
#LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
#PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

```

; TEST 104
-----

```

5157					ST10:	SCOPE		*****
5158	027652	000004			MOV #104,STSTNM			:LOAD THE NO. OF THIS TEST
5159	027654	012737	000104	001202	MOV #ST105,NEXT			:POINT TO THE START OF NEXT TEST.
5160	027662	012737	030030	001442	MOV #1\$,LOCK			:ADDRESS FOR LOCK ON DATA.
5161	027670	012737	027722	001444				:R1 CONTAINS BASE KMC11 ADDRESS
5162					MSTCLR			:MASTER CLEAR KMC11
5163	027676	104410			CLR R0			:MEM + SP ADDRESS
5164	027700	005000			MOV #5\$,R2			:POINTER TO CORRECT DATA
5165	027702	012702	030020		JSR PC,NEMLD			:LOAD 8 WORDS OF MAIN MEMORY
5166	027706	004737	035602		MEMDAT			:POINTER TO DATA
5167	027712	035726			JSR PC,SPLD			:LOAD 8 WORDS OF SP
5168	027714	004737	035636		SPDAT			:POINTER TO DATA
5169	027720	035736			JSR PC,CLRC			:CLEAR C BIT!
5170	027722	004737	035702		BIC #17,2\$			:CLEAR ADDRESS FIELD OF INSTRUCTION
5171	027726	042737	000017	027742	BIS R0,2\$			:ADD ADDRESS TO INSTRUCTION
5172	027734	050037	027742		ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5173	027740	104412			010000			:LOAD MAR
5174	027742	010000			BIC #17,3\$			:CLEAR ADDRESS OF INSTRUCTION
5175	027744	042737	000017	027760	BIS R0,3\$			:ADD ADDRESS TO INSTRUCTION
5176	027752	050037	027760		ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5177	027756	104412			040400!(<3*20)			:BR + INC A
5178	027760	104460		3\$:	ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5179	027762	104412			61224			:MOVE BR TO PORT4
5180	027764	061224			MOVB (R2),R5			:PUT "EXPECTED" IN R5
5181	027766	111205			MOVB 4(R1),R4			:PUT "FOUND" IN R4
5182	027770	116104	000004					

```

5183 027774 120504          CMPB   R5,R4          :DATA CORRECT?
5184 027776 001401          BEQ    4$            :BR IF YES
5185 030000 104015          ERROR  15           :ALU ERROR
5186 030002 104405          4$: SCOPI           :SMO9=1?
5187 030004 005202          INC    R2           :NEXT DATA
5188 030006 005200          INC    R0           :NEXT ADDRESS
5189 030010 022700 000010        CMP    #10,R0       :DONE YET?
5190 030014 001342          BNE    1$           :BR IF NO
5191 030016 104420          ADVANCE :ADVANCE LOOP
5192 030020 001 001 000 5$: .BYTE 1,1,0,0,126,126,253,253
5193 030023 000 126 126
5194 030026 253 253
5195
5196 .EVEN
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```

:***** TEST 105 *****
:ALU TEST
:TEST OF ALU FUNCTION 2A WITH C BIT CLEARED
:ALU FUNCTION (A PLUS A) CODE=5
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

TEST 105

```

5209 030030 000604          †ST105: SCOPE
5210 030032 012737 000105 001202  MOV    #105,STSTNM :LOAD THE NO. OF THIS TEST
5211 030040 012737 030206 001442  MOV    #ST106,NEXT :POINT TO THE START OF NEXT TEST.
5212 030046 012737 030100 001444  MOV    #1$,LOCK :ADDRESS FOR LOCK ON DATA.
5213
5214 030054 104410          MSTCLR :R1 CONTAINS BASE KMC11 ADDRESS
5215 030056 005000          CLR    R0           :MASTER CLEAR KMC11
5216 030060 012702 030176  MOV    #5$,R2       :MEM + SP ADDRESS
5217 030064 004737 035602  JSR    PC,MEMLD     :POINTER TO CORRECT DATA
5218 030070 035726          MEMDAT :LOAD 8 WORDS OF MAIN MEMORY
5219 030072 004737 035636  JSR    PC,SPLD     :POINTER TO DATA
5220 030076 035736          SPDAT  :LOAD 8 WORDS OF SP
5221 030100 004737 035702  JSR    PC,CLRC     :POINTER TO DATA
5222 030104 042737 000017 030120  BIC    #17,2$      :CLEAR C BIT!
5223 030112 050037 030120          BIS    R0,2$      :CLEAR ADDRESS FIELD OF INSTRUCTION
5224 030116 104412          ROMCLK :ADD ADDRESS TO INSTRUCTION
5225 030120 010000          #10000 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5226 030122 042737 000017 030136  BIC    #17,3$     :LOAD MAR
5227 030130 050037 030136          BIS    R0,3$     :CLEAR ADDRESS OF INSTRUCTION
5228 030134 104412          ROMCLK :ADD ADDRESS TO INSTRUCTION
5229 030136 040520          #40400!(5*20) :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5230 030140 104412          ROMCLK :BR + 2A
5231 030142 061224          61224 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5232 030144 111205          MOVB   (R2),R5     :MOVE BR TO PORT4
5233 030146 116104          MOVB   4(R1),R4    :PUT "EXPECTED" IN R5
5234 030150 120504          CMPB   R5,R4      :PUT "FOUND" IN R4
5235 030154 001401          BEQ    4$         :DATA CORRECT?
5236 030156 104015          ERROR  15         :BR IF YES
5237 030160 104405          4$: SCOPI         :ALU ERROR
5238 030162 005202          INC    R2         :SMO9=1?
                    :NEXT DATA

```

```

5239 030164 005200          INC      R0          ;NEXT ADDRESS
5240 030166 022700 000010  CMP      #10,R0     ;DONE YET?
5241 030172 001342          BNE     1$          ;BR IF NO
5242 030174 104420          ADVANCE ;ADVANCE LOOP
5243 030176 000      000    376 5$: .BYTE 0,0,376,376,252,252,124,124
5244 030201 376      252    252
5245 030204 124      124

```

.EVEN

```

: ***** TEST 106 *****
: #ALU TEST
: #TEST OF ALU FUNCTION A PLUS C WITH C BIT CLEARED
: #ALU FUNCTION (A PLUS C) CODE=4
: #LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: #PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

TEST 106

```

5256 030206 000004          ;*****
5257 030210 012737 000106 001202 ;TEST106: SCOPE
5258 030216 012737 030364 001442 ;MOV      #106,$STNM ;LOAD THE NO. OF THIS TEST
5259 030224 012737 030256 001444 ;MOV      #1$,$NEXT ;POINT TO THE START OF NEXT TEST.
5260 ;MOV      #1$,$LOCK ;ADDRESS FOR LOCK ON DATA.
5261 ;R1 CONTAINS BASE KMC11 ADDRESS
5262 030232 104410          ;MASTER CLEAR KMC11
5263 030234 005000          CLR      R0          ;MEM + SP ADDRESS
5264 030236 012702 030354 ;MOV      #5$,$R2     ;POINTER TO CORRECT DATA
5265 030242 004737 035602 ;JSR     PC,$MEMLO ;LOAD 8 WORDS OF MAIN MEMORY
5266 030246 035726          ;MENDAT ;POINTER TO DATA
5267 030250 004737 035636 ;JSR     PC,$PLD     ;LOAD 8 WORDS OF SP
5268 030254 035736          ;SPOAT ;POINTER TO DATA
5269 030256 004737 035702 1$: ;JSR     PC,$CLRC   ;CLEAR C BIT!
5270 030262 012737 000017 030276 ;BIC     #17,$2$    ;CLEAR ADDRESS FIELD OF INSTRUCTION
5271 030274 050037 030276          ;BIS     R0,$2$    ;ADD ADDRESS TO INSTRUCTION
5272 030276 010000          ;ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5273 030300 012737 000017 030314 2$: ;BIC     #17,$3$    ;LOAD MAR
5274 030306 050037 030314          ;BIS     R0,$3$    ;CLEAR ADDRESS OF INSTRUCTION
5275 030312 104412          ;ROMCLK ;ADD ADDRESS TO INSTRUCTION
5276 030314 040500          ;D40400(4#20) ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5277 030316 104412          ;ROMCLK ;BR + A PLUS C
5278 030320 061224          ;61224 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5279 030322 111205          ;MOV     (R2),R5    ;MOVE BR TO PORT4
5280 030324 116104 000004 ;MOV     4(R1),R4   ;PUT "EXPECTED" IN R5
5281 030330 120504          ;CMPB   R5,R4      ;PUT "FOUND" IN R4
5282 030332 001401          ;BEQ    4$         ;DATA CORRECT?
5283 030334 104015          ;ERROR  1$        ;BR IF YES
5284 030336 104405          ;SCOPI  1$        ;ALU ERROR
5285 030340 005202          ;INC    R2         ;SMOS=1?
5286 030342 005200          ;INC    R0         ;NEXT DATA
5287 030344 022700 000010  ;CMP     #10,R0     ;NEXT ADDRESS
5288 030350 001342          ;BNE   1$         ;DONE YET?
5289 030352 104420          ;ADVANCE ;BR IF NO
5290 030354 000      000    377 5$: .BYTE 0,0,-1,-1,125,125,252,252 ;ADVANCE LOOP

```

5295 030357 377 125 125  
5296 030362 252 252  
5297  
5298  
5299  
5300  
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5302  
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\*\*\*\*\* TEST 107 \*\*\*\*\*  
\*ALU TEST  
\*TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT CLEAR!  
\*ALU FUNCTION (A-B-1) CODE=17  
\*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
\*PERFORM THE FUNCTION, VERIFY THE RESULTS  
\*\*\*\*\*

TEST 107

030364 000004  
030366 012737 000107 001202  
030374 012737 030542 001442  
030402 012737 030434 001444  
  
030410 104410  
030412 005000  
030414 012702 030532  
030420 004737 035602  
030422 035726  
030424 004737 035636  
030428 035736  
030434 004737 035702  
030440 012737 000017 030454  
030446 050037 030454  
030450 104412  
030454 012737 000017 030472  
030456 050037 030472  
030470 104412  
030472 040760  
030474 104412  
030476 061224  
  
030500 111205  
030502 116104 000004  
030504 120504  
030510 001401  
030512 104015  
030514 104406  
030516 005202  
030520 005200  
030522 022700 000010  
030524 001342  
030530 104420  
030532 377 000 376  
030534 377 377 252  
030540 124 377

\*\*\*\*\*  
TEST107: SCOPE  
MOV #107,STNUM ; LOAD THE NO. OF THIS TEST  
MOV #ST110,NEXT ; POINT TO THE START OF NEXT TEST.  
MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.  
  
; RI CONTAINS BIZE KMC11 ADDRESS  
RSTCLR ; MASTER CLEAR KMC11  
CLR RO ; R0 = SP ADDRESS  
MOV #55,R2 ; POINTER TO CORRECT DATA  
JSR PC,HEMLD ; LOAD 8 WORDS OF MAIN MEMORY  
MEMDAT ; POINTER TO DATA  
JSR PC,SPLD ; LOAD 8 WORDS OF SP  
SPDAT ; POINTER TO DATA  
JSR PC,CLRC ; CLEAR C BIT!  
BYC #17,28 ; CLEAR ADDRESS FIELD OF INSTRUCTION  
BIS RO,28 ; ADD ADDRESS TO INSTRUCTION  
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
ROMCLK 010000 ; LOAD R0  
; CLEAR ADDRESS OF INSTRUCTION  
BIC #17,38 ; ADD ADDRESS TO INSTRUCTION  
BIS RO,38 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
ROMCLK 040760<17420> ; R0 = 2'S COMP SUB  
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304  
ROMCLK 061224 ; MOVE R0 TO PORT4  
MOV# (R0),R5 ; PUT "EXPECTED" IN R5  
MOV# 4(R0),R4 ; PUT "FOUND" IN R4  
CPS# R5,R4 ; DATA CORRECT?  
BEQ #5 ; BR IF YES  
ERROR 15 ; ALL ERROR  
SCOP1 509-1 ;  
INC R2 ; NEXT DATA  
INC RO ; NEXT ADDRESS  
CMP #10,RO ; DONE YET?  
BNE 15 ; BR IF NO  
ADVANCE ; ADVANCE LOOP  
; .BYTE -1,0,376,-1,-1,252,124,-1  
\*\*\*\*\*

.EVEN

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5351
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5360
5361
5362 030542 000004
5363 030544 012737 000110 001202
5364 030552 012737 030720 001442
5365 030560 012737 030612 001444
5366
5367 030566 104410
5368 030570 005000
5369 030572 012702 030710
5370 030576 004737 035602
5371 030602 035726
5372 030604 004737 035636
5373 030610 035736
5374 030612 004737 035702
5375 030616 042737 000017
5376 030624 050037 030632
5377 030630 104412
5378 030632 010000
5379 030634 042737 000017 030451
5380 030642 050037 030650
5381 030646 104412
5382 030650 040560
5383 030652 104412
5384 030654 061224
5385 030656 111205
5386 030660 116104 000004
5387 030664 120504
5388 030666 001401
5389 030670 104015
5390 030672 104405
5391 030674 005202
5392 030676 005200
5393 030700 022700 000010
5394 030704 001342
5395 030706 104420
5396 030710 377 377 376
5397 030713 376 124 124
5398 030716 251 251
5399
5400
5401
5402
5403
5404
5405
5406

```

```

***** TEST 110 *****
*ALU TEST
*TEST OF A U FUNCTION DEC A WITH C BIT CLEARED
*ALU FUNCTION (A-1) CODE=7
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 110

```

-----
*****
TST110: SCOPE
MOV #110,$STNM ; LOAD THE NO. OF THIS TEST
MOV #TST111,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #55,R2 ; POINTER TO CONNECT DATA
JSR PC,MEMLD ; LOAD 8 WORDS OF MAIN MEMORY
MEMDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPORT ; POINTER TO DATA
JSR PC,LRC ; CLEAR C BIT!
BIC #17,R2 ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R0,R2 ; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; LOAD MEM
BIC #17,R2 ; CLEAR ADDRESS OF INSTRUCTION
BIS R0,R2 ; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
040560:(?x20) ; RR = DEC A
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
61224 ; MOVE RR TO PORT4
MOV# (R2) R5 ; PUT "EXPECTED" IN R5
MOV# 4(R1),R4 ; PUT "FOUND" IN R4
CMP# R5,R4 ; DATA CORRECT?
BEQ 48 ; BR IF YES
ERROR 15 ; ALU ERROR
45: SCOP1 ; SMOA=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE 15 ; BR IF NO
ADVANCE ; ADVANCE LOOP
55: .BYTE -1,-1,376,376,124,124,251,251
.EVEN

```

```

***** TEST 111 *****
*ALU TEST
*TEST OF ALU FUNCTION SEL B WITH C BIT SET
*ALU FUNCTION (B) CODE=11
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA

```

```

5407
5408
5409
5410
5411
5412
5413 030720 000004
5414 030722 012737 000111 001202
5415 030730 012737 031076 001442
5416 030736 012737 030770 001444
5417
5418 030744 104410
5419 030746 005000
5420 030750 012702 031066
5421 030754 004737 035602
5422 030760 035726
5423 030762 004737 035636
5424 030766 035736
5425 030770 004737 035714
5426 030774 042737 000017 031010
5427 031002 050037 031010
5428 031006 104412
5429 031010 010000
5430 031012 042737 000017 031026
5431 031020 050037 031026
5432 031024 104412
5433 031026 040620
5434 031030 104412
5435 031032 061224
5436 031034 111205
5437 031036 116104 000004
5438 031042 120504
5439 031044 031401
5440 031046 104015
5441 031050 104405
5442 031052 005202
5443 031054 005200
5444 031056 022700 000010
5445 031062 001342
5446 031064 104420
5447 031066 000 377 000
5448 031071 377 125 252
5449 031074 125 252
5450
5451
5452
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5454
5455
5456
5457
5458
5459
5460
5461
5462

```

```

; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****
; TEST 111
; -----
; *****
TST111: SCOPE
MOV      #111,STSTNM      ; LOAD THE NO. OF THIS TEST
MOV      #TST112,NEXT    ; POINT TO THE START OF NEXT TEST.
MOV      #1$,LOCK        ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR  MASTER CLEAR KMC11
CLR      R0              ; MEM + SP ADDRESS
MOV      #5$,R2         ; POINTER TO CONNECT DATA
JSR      PC,MEHL0       ; LOAD # WORDS OF MAIN MEMORY
MEMDAT  ; POINTER TO DATA
JSR      PC,SPLO        ; LOAD # WORDS OF SP
SPDAT   ; POINTER TO DATA
JSR      PC,SETC        ; SET C BIT!
BIC      #17,2$         ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS      R0,2$          ; ADD ADDRESS TO INSTRUCTION
ROMCLK  010000          ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; LOAD MMR
BIC      #17,3$         ; CLEAR ADDRESS OF INSTRUCTION
BIS      R0,3$          ; ADD ADDRESS TO INSTRUCTION
ROMCLK  040620<11*20> ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; BR + SEL #
ROMCLK  61224           ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; MOVE BR TO PORT4
MOVW    (R2),R5         ; PUT "EXPECTED" IN R5
MOVW    4(R1),R4        ; PUT "FOUND" IN R4
CMPB    R5,R4          ; DATA CONNECT?
BEQ     4$              ; BR IF YES
ERR0R   15              ; ALU ERROR
SCOPI   15              ; SUD=1?
INC     R2              ; NEXT DATA
INC     R0              ; NEXT ADDRESS
CMP     #10,R0         ; DONE YET?
BNE     1$              ; BR IF NO
ADVANCE ; ADVANCE LOOP
.BYTE  0,-1,0,-1,125,252,125,252
; .EVEN

```

```

***** TEST 112 *****
; ALU TEST
; TEST OF ALU FUNCTION SEL A WITH C BIT SET
; ALU FUNCTION (A) CODE=10
; LOAD MAIN MEM AND SP WITH # WORDS OF DATA
; *PERFORM THE FUNCTION, VERIFY THE RESULTS
; *****
; TEST 112
; -----

```



```

5463
5464 031076 000004
5465 031100 012737 000112 001202
5466 031106 012737 031254 001442
5467 031114 012737 031146 001444
5468
5469 031122 104410 MSTCLR
5470 031124 005000 CLR R0
5471 031126 012702 031244 MOV #55,R2
5472 031132 004737 035602 JSR PC,MEMLD
5473 031136 035726 MEMDAT
5474 031140 004737 035636 JSR PC,SPLD
5475 031144 035736 SPOAT
5476 031146 004737 035714 JSR PC,SETC
5477 031152 042737 000017 031166 BIC #17,25
5478 031160 050037 031166 BIS R0,25
5479 031164 104412 ROMCLK
5480 031166 010000 25:
5481 031170 042737 000017 031204 BIC #17,35
5482 031176 050037 031204 BIS R0,35
5483 031202 104412 ROMCLK
5484 031204 040600 35:
5485 031206 104412 ROMCLK
5486 031210 061224
5487 031212 111205 MOV# (R2),R5
5488 031214 116104 000004 MOV# 4(R1),R4
5489 031220 120504 CMB# R5,R4
5490 031222 001401 BEQ #5
5491 031224 104015 ERROR 15
5492 031226 104405 45: SCOPE
5493 031230 005202 INC R2
5494 031232 005200 INC R0
5495 031234 022700 000010 CMP #10,R0
5496 031240 001342 BNE 15
5497 031242 104420 ADVANCE
5498 031244 000 000 377 55: .BYTE 0,0,-1,-1,125,125,252,252
5499 031247 377 125 125
5500 031252 252 252
5501 .EVEN
5502
5503
5504
5505
5506
5507
5508
5509
5510
5511
5512
5513
5514
5515 031254 000004
5516 031256 012737 000113 001202
5517 031264 012737 031432 001442
5518 031272 012737 031324 001444

```

```

*****
†ST112: SCOPE
MOV #112,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #†ST113,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.
R1 CONTAINS BASE KMC11 ADDRESS
MASTER CLEAR KMC11
MEM + SP ADDRESS
POINTER TO CONNECT DATA
LOAD 8 WORDS OF MAIN MEMORY
POINTER TO DATA
LOAD 8 WORDS OF SP
POINTER TO DATA
SET C BIT!
CLEAR ADDRESS FIELD OF INSTRUCTION
ADD ADDRESS TO INSTRUCTION
NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
LOAD NR
CLEAR ADDRESS OF INSTRUCTION
ADD ADDRESS TO INSTRUCTION
NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
BR + SEL A
NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
MOVE BR TO PORT4
PUT "EXPECTED" IN R5
PUT "FOUND" IN R4
DATA CONNECT?
BR IF YES
ALU ERROR
SM09=1?
NEXT DATA
NEXT ADDRESS
DONE YET?
BR IF NO
ADVANCE LOOP

```

```

***** TEST 113 *****
*ALU TEST
*TEST OF ALU FUNCTION A OR NOTB WITH C BIT SET
*ALU FUNCTION (A OR NOTB) CODE=12
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 113

```

*****
†ST113: SCOPE
MOV #113,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #†ST114,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.

```

```

9519 031300 104410
9520 031302 005000
9521 031304 012702 031422
9522 031310 004737 035602
9523 031314 035726
9524 031316 004737 035636
9525 031322 035736
9526 031324 004737 035714
9527 031330 004737 000017 031344 1S:
9528 031336 050037 031344
9529 031342 104412
9530 031344 010000
9531 031346 042737 000017 031362 2S:
9532 031354 050037 031362
9533 031360 104412
9534 031362 040640 3S:
9535 031364 104412
9536 031366 061224
9537 031370 111205
9538 031372 116104 000004
9539 031376 120504
9540 031400 301401
9541 031402 104015
9542 031404 104405 4S:
9543 031406 005202
9544 031410 005200
9545 031412 022700 000010
9546 031416 001342
9547 031420 104420
9548 031422 377 000 377 5S:
9549 031425 377 125
9550 031430 252 377
9551 031432
9552
9553
9554
9555
9556
9557
9558
9559
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9562
9563
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9567
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9571
9572
9573
9574

```

```

MSTCLR
CLR RO
MOV #55,R2
JSR PC,NEMLD
MEMDAT
JSR PC,SPLD
SPOAT
JSR PC,SETC
BIC #17,25 031344
BIS RO,25
ROMCLK 010000 2S:
O10000
BIC #17,35 031362
BIS RO,35
ROMCLK 040640! (12*20) 3S:
ROMCLK 61224
MOV8 (R2),R5
MOV8 4(R1),R4
CMPB R5,R4
BEQ 45
ERROR 15 4S:
SCOPI
INC R2
INC RO
CMP #10,RO
BNE 15
ADVANCE
.BYTE -1,0,-1,-1,-1,125,252,-1 5S:

```

```

R1 CONTAINS BASE KMC11 ADDRESS
MASTER CLEAR KMC11
MEM + SP ADDRESS
POINTER TO CORRECT DATA
LOAD 8 WORDS OF MAIN MEMORY
POINTER TO DATA
LOAD 8 WORDS OF SP
POINTER TO DATA
SET C BIT!
CLEAR ADDRESS FIELD OF INSTRUCTION
ADD ADDRESS TO INSTRUCTION
NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
LOAD MAR
CLEAR ADDRESS OF INSTRUCTION
ADD ADDRESS TO INSTRUCTION
NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
BR = A OR NOTB
NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
MOVE BR TO PORT4
PUT "EXPECTED" IN R5
PUT "FOUND" IN R4
DATA CORRECT?
BR IF YES
ALU ERROR
SUM=1?
NEXT DATA
NEXT ADDRESS
DONE YET?
BR IF NO
ADVANCE LOOP

```

```

***** TEST 114 *****
:ALU TEST
:TEST OF ALU FUNCTION A AND B WITH C BIT SET
:ALU FUNCTION (A AND B) CODE=13
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

```

TEST 114
-----
:*****
†ST114: SCOPE
MOV #114,$STNM ; LOAD THE NO. OF THIS TEST
MOV #ST115,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.
:R1 CONTAINS BASE KMC11 ADDRESS
:MASTER CLEAR KMC11
:MEM + SP ADDRESS
:POINTER TO CORRECT DATA
:LOAD 8 WORDS OF MAIN MEMORY

```

```

9566 031432 000004
9567 031434 012737 000114 001202
9568 031442 012737 031610 001442
9569 031450 012737 031502 001444
9570
9571 031456 104410
9572 031460 005000
9573 031462 012702 031600
9574 031466 004737 035602

```

```

5573 031472 035726
5574 031474 047737 035636
5575 031480 035726
5576 031480 047737 035714
5577 031480 047737 000017 031522
5578 031480 047737 000017 031522
5579 031514 060037 031522
5580 031514 104412
5581 031514 010000
5582 031514 047737 000017 031540
5583 031514 060037 031540
5584 031514 104412
5585 031514 040660
5586 031514 104412
5587 031514 061224
5588 031514 111205
5589 031514 16104 000004
5590 031514 120504
5591 031514 001401
5592 031514 104015
5593 031514 104405
5594 031514 005202
5595 031514 005200
5596 031570 022700 000010
5597 031574 001342
5598 031574 001342
5599 031576 104420
5600 031600 000 000 000 55:
5601 031603 377 125 000
5602 031606 000 252

```

```

MEMDAT
JSR PC,SPLD
SPDAT
JSR PC,SETC
BIC #17,25
BIS R0,25
ROMCLK 010000
BIC #17,35
BIS R0,35
ROMCLK 040400! <13*20>
ROMCLK 61224
MOV8 (R2),R5
MOV8 4(R1),R4
CMP8 R5,R4
BEQ 45
ERROR 15
SCOPI
INC R2
INC R0
CMP #10,R0
BNE 15
ADVANCE
.BYTE 0,0,0,-1,125,0,0,252

```

```

: POINTER TO DATA
: LOAD 8 WORDS OF SP
: POINTER TO DATA
: SET C BIT!
: CLEAR ADDRESS FIELD OF INSTRUCTION
: ADD ADDRESS TO INSTRUCTION
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: LOAD MAR
: CLEAR ADDRESS OF INSTRUCTION
: ADD ADDRESS TO INSTRUCTION
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: BR + A AND B
: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
: MOVE BR TO PORT4
: PUT "EXPECTED" IN R5
: PUT "FOUND" IN R4
: DATA CORRECT?
: BR IF YES
: ALU ERROR
: SMO9=1?
: NEXT DATA
: NEXT ADDRESS
: DONE YET?
: BR IF NO
: ADVANCE LOOP

```

.EVEN

```

: ***** TEST 115 *****
: *ALU TEST
: *TEST OF ALU FUNCTION A OR B WITH C BIT SET
: *ALU FUNCTION (A OR B) CODE=14
: *LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: *PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

TEST 115

```

5617 031610 000004
5618 031612 012737 000115 001202
5619 031620 012737 031766 001442
5620 031626 012737 031660 001444
5621
5622 031634 104410
5623 031636 005000
5624 031640 012702 031756
5625 031644 004737 035602
5626 031650 035726
5627 031652 004737 035636
5628 031656 035736
5629 031660 004737 035714
5630 031664 042737 000017 031700

```

```

†ST115: SCOPE
MOV #115,STSTNM
MOV #TST116,NEXT
MOV #1$,LOCK
MSTCLR
CLR R0
MOV #5$,R2
JSR PC,MEMLD
MEMDAT
JSR PC,SPLD
SPDAT
JSR PC,SETC
BIC #17,25

```

```

: LOAD THE NO. OF THIS TEST
: POINT TO THE START OF NEXT TEST.
: ADDRESS FOR LOCK ON DATA.
: R1 CONTAINS BASE KMC11 ADDRESS
: MASTER CLEAR KMC11
: MEM + SP ADDRESS
: POINTER TO CORRECT DATA
: LOAD 8 WORDS OF MAIN MEMORY
: POINTER TO DATA
: LOAD 8 WORDS OF SP
: POINTER TO DATA
: SET C BIT!
: CLEAR ADDRESS FIELD OF INSTRUCTION

```

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K.C.P11 21-MAR-77 17:19 KMC11 ALU TESTS

5631	031672	050037	031700		BIS	RO,25	ADD ADDRESS TO INSTRUCTION
5632	031676	104412			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5633	031700	010000		25:	010000		LOAD MAR
5634	031702	042737	000017	031716	BIC	#17,35	CLEAR ADDRESS OF INSTRUCTION
5635	031710	050037	031715		BIS	RO,35	ADD ADDRESS TO INSTRUCTION
5636	031714	104412			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5637	031715	040700		35:	040700:(14*20)		BR - A OR B
5638	031720	104412			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5639	031722	061224			61224		MOVE BR TO PORT4
5640	031724	111205			MOV#	(R2),R5	PUT "EXPECTED" IN R5
5641	031726	116104	000004		MOV#	4(R1),R4	PUT "FOUND" IN R4
5642	031732	120504			CHPB	R5,R4	DATA CORRECT?
5643	031734	001401			BEG	45	BR IF YES
5644	031736	104C15			ERROR	15	ALU ERROR
5645	031740	104405		45:	SCOPI		SID=1?
5646	031742	005202			INC	R2	NEXT DATA
5647	031744	005200			INC	RO	NEXT ADDRESS
5648	031746	022700	000010		CMP	#10,RO	DONE YET?
5649	031752	001342			BNE	15	BR IF NO
5650	031754	104420			ADVANCE		ADVANCE LOOP
5651	031756	000	377	377	.BYTE	0,-1,-1,-1,125,-1,-1,252	
5652	031761	377	125	377			
5653	031764	377	252				

.EVEN

```

***** TEST 116 *****
#ALU TEST
#TEST OF ALU FUNCTION A XOR B WITH C BIT SET
#ALU FUNCTION (A XOR B) CODE=15
#LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
#PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 116

```

*****
TST116: SCOPE
MOV #116,STSTM ; LOAD THE NO. OF THIS TEST
MOV #TST117,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
; MASTER CLEAR KMC11
; MEM + SP ADDRESS
; POINTER TO CORRECT DATA
; LOAD 8 WORDS OF MAIN MEMORY
; POINTER TO DATA
; LOAD 8 WORDS OF SP
; POINTER TO DATA
; SET C BIT!
; CLEAR ADDRESS FIELD OF INSTRUCTION
; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; LOAD MAR
; CLEAR ADDRESS OF INSTRUCTION
; ADD ADDRESS TO INSTRUCTION

```

5668	031766	000004			SCOPE		
5669	031770	012737	000116	001202	MOV	#116,STSTM	
5670	031776	012737	032144	001442	MOV	#TST117,NEXT	
5671	032004	012737	032036	001444	MOV	#15,LOCK	
5672							
5673	032012	104410			STCLR		
5674	032014	005000			CLR	RO	
5675	032016	012702	032134		MOV	#55,R2	
5676	032022	004737	035602		JSR	PC,MEMLO	
5677	032026	025726			MEMDAT		
5678	032030	004737	035636		JSR	PC,SPLD	
5679	032034	025726			SPDAT		
5680	032036	004737	035714		JSR	PC,SETC	15:
5681	032042	042737	000017	032056	BIC	#17,25	
5682	032060	050037	032056		BIS	RO,25	
5683	032054	104412			ROMCLK		
5684	032056	010000			010000		25:
5685	032060	042727	000017	032074	BIC	#17,35	
5686	032066	050037	032074		BIS	RO,35	

```

5687 032072 104412 ROMCLK NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5688 032074 040720 35: 040400!<15*20> BR + A XOR B
5689 032076 104412 ROMCLK NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5690 032100 061224 61224 MOVE BR TO PORT4
5691 032102 111205 MOVB (R2),R5 PUT "EXPECTED" IN R5
5692 032104 116104 000004 MOVB 4(R1),R4 PUT "FOUND" IN R4
5693 032110 120504 CMPS RS,R4 DATA CONNECT?
5694 032112 001401 BEQ 48 BR IF YES
5695 032114 104015 ERROR 15 ALU ERROR
5696 032116 104405 45: SCOP1 509=1?
5697 032120 005202 INC R2 NEXT DATA
5698 032122 005200 INC R0 NEXT ADDRESS
5699 032124 022700 000010 CMP #10,R0 DONE YET?
5700 032130 001342 BNE 18 BR IF NO
5701 032132 104420 ADVANCE ADVANCE LOOP
5702 032134 000 377 377 55: .BYTE 0,-1,-1,0,0,-1,-1,0
5703 032137 000 000 377
5704 032142 377 000
5705 .EVEN
5706
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5718

```

```

***** TEST 117 *****
: ALU TEST
: TEST OF ALU FUNCTION ADD WITH C BIT SET
: ADD FUNCTION (A PLUS B) CODE=00
: LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
: PERFORM THE FUNCTION, VERIFY THE RESULTS
: *****

```

: TEST 117

```

5719 032144 000004 000117 001202 15:117: SCOPE
5720 032146 012737 032322 001442 MOV #117,SYSTEM ; LOAD THE NO. OF THIS TEST
5721 032154 012737 032214 001444 MOV #SYSTEM,NEXT ; POINT TO THE START OF NEXT TEST.
5722 032162 012737 032214 001444 MOV #SYSTEM,LOCK ; ADDRESS FOR LOCK ON DATA.
5723 ; R1 CONTAINS THE KMC11 ADDRESS
5724 032170 104410 NSTCLR ; MASTER CLEAR KMC11
5725 032172 005000 CLR R0 ; R0 = SP ADDRESS
5726 032174 012702 032312 MOV #58,R2 ; POINTER TO CORRECT DATA
5727 032180 004737 035602 JSR PC,READ ; LOAD 8 WORDS OF MAIN MEMORY
5728 032184 025725 ; POINTER TO DATA
5729 032186 001742 035636 JSR PC,SPLD ; LOAD 8 WORDS OF SP
5730 032188 025725 ; POINTER TO DATA
5731 032194 004737 025714 032234 15: JSR PC,SETC ; SET C BIT!
5732 032196 012737 000017 032234 BIT #17,25 ; CLEAR ADDRESS FIELD OF INSTRUCTION
5733 032198 025725 032234 ADD #17,25 ; ADD ADDRESS TO INSTRUCTION
5734 032200 104412 ROMCLK NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5735 032202 010000 25: LOAD R0
5736 032204 000017 032252 BIT #17,35 ; CLEAR ADDRESS OF INSTRUCTION
5737 032206 025725 032252 ADD #17,35 ; ADD ADDRESS TO INSTRUCTION
5738 032208 104412 ROMCLK NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5739 032210 040400!<00*20> BR + 000
5740 032212 104412 ROMCLK NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5741 032214 61224 MOVE BR TO PORT4
5742 032216 111205 MOVB (R2),R5 ; PUT "EXPECTED" IN R5

```

```

5743 032262 116104 000004      MOVB 4(R1),R4      : PUT "FOUND" IN R4
5744 032266 120504      CMPB  R5,R4      : DATA CORRECT?
5745 032270 001401      BEQ   4$         : BR IF YES
5746 032272 104015      ERROR 15        : ALU ERROR
5747 032274 104405      SCOPI          : SW09=1?
5748 032276 005202      INC   R2         : NEXT DATA
5749 032300 005200      INC   R0         : NEXT ADDRESS
5750 032302 022700 000010      CMP  #10,R0      : DONE YET?
5751 032306 001342      BNE  1$         : BR IF NO
5752 032310 104420      ADVANCE        : ADVANCE LOOP
5753 032312      000      377      377 5$: .BYTE 0,-1,-1,376,252,-1,-1,124
5754 032315      376      252      377
5755 032320      377      124
5756
5757 .EVEN
5758
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5770
5771
5772
5773
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```

```

:***** TEST 120 *****
:ALU TEST
:TEST OF ALU FUNCTION 2A W/C WITH C BIT SET
:ALU FUNCTION (A PLUS A PLUS C) CODE=6
:LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
:PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****

```

TEST 120

```

5770 032322 000004      :*****
5771 032324 012737 000120 001202 1$T120: SCOPE      : LOAD THE NO. OF THIS TEST
5772 032332 012737 032500 001442      MOV  #120,$STNUM  : POINT TO THE START OF NEXT TEST.
5773 032340 012737 032372 001444      MOV  #1$T121,NEXT : ADDRESS FOR LOCK ON DATA.
5774                                MOV  #18,LOCK     : R1 CONTAINS BASE KMC11 ADDRESS
5775                                MSTCLR          : MASTER CLEAR KMC11
5776 032350 005000      CLR   R0         : R0 = SP ADDRESS
5777 032352 012702 332470      MOV  #55,R2      : POINTER TO CORRECT DATA
5778 032356 004737 035602      JSR  PC,NEMLD   : LOAD 8 WORDS OF MAIN MEMORY
5779 032362 035726      MENDAT        : POINTER TO DATA
5780 032364 004737 035636      JSR  PC,$PLD    : LOAD 8 WORDS OF SP
5781 032370 035736      SPDAT        : POINTER TO DATA
5782 032372 004737 035714      JSR  PC,SETC    : SET C BIT!
5783 032376 012737 000017 032412 1$: BIC  #17,2$    : CLEAR ADDRESS FIELD OF INSTRUCTION
5784 032404 050037 032412      BIS  R0,2$     : ADD ADDRESS TO INSTRUCTION
5785 032410 104412      ROMCLK        : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5786 032412 010000      010000      : LOAD R0
5787 032414 012737 000017 032430 2$: BIC  #17,3$    : CLEAR ADDRESS OF INSTRUCTION
5788 032422 050037 032430      BIS  R0,3$     : ADD ADDRESS TO INSTRUCTION
5789 032426 104412      ROMCLK        : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5790 032430 040540      040540!(6*20) : BR + 2A W/C
5791 032432 104412      ROMCLK        : NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5792 032434 061224      61224        : MOVE R0 TO PORT4
5793 032436 111205      MOVB (R2),R5   : PUT "EXPECTED" IN R5
5794 032440 116104 000004      MOVB 4(R1),R4  : PUT "FOUND" IN R4
5795 032444 120504      CMPB  R5,R4    : DATA CORRECT?
5796 032446 001401      BEQ   4$         : BR IF YES
5797 032450 104015      ERROR 15        : ALU ERROR
5798 032452 104405      SCOPI          : SW09=1?

```

```

5799 032454 005202          INC      R2          :NEXT DATA
5800 032456 005200          INC      R0          :NEXT ADDRESS
5801 032460 022700 000010    CMP      #10,R0     :DONE YET?
5802 032464 001342          BNE     #5          :BR IF NO
5803 032466 104420          ADVANCE          :ADVANCE LOOP
5804 032470          001      377 55:  .BYTE 1,1,-1,-1,253,253,125,125
5805 032473          377      253
5806 032476          125      125
5807                                     .EVEN
5808
5809
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5820

```

```

***** TEST 121 *****
*ALU TEST
*TEST OF ALU FUNCTION SUB WITH C BIT SET
*ALU FUNCTION (A-B) CODE=16
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 121

```

5821 032500 000004          :*****
5822 032502 012737 000121 001202 1ST121: SCOPE
5823 032510 012737 032556 001442      MOV     #121,STSNM   :LOAD THE NO. OF THIS TEST
5824 032516 012737 032550 001444      MOV     #1ST122,NEXT :POINT TO THE START OF NEXT TEST.
5825                                     MOV     #1$,LOCK     :ADDRESS FOR LOCK ON DATA.
5826 032524 104410          :R1 CONTAINS BASE KMC11 ADDRESS
5827 032526 005000          :MASTER CLEAR KMC11
5828 032530 012702 032646      CLR     R0          :MEM + SP ADDRESS
5829 032534 004737 035602      MOV     #5$,R2     :POINTER TO CORRECT DATA
5830 032540 035726          JSR     PC, MEMLD   :LOAD 8 WORDS OF MAIN MEMORY
5831 032542 004737 035636      MEMDAT          :POINTER TO DATA
5832 032546 035736          JSR     PC, SPLD   :LOAD 8 WORDS OF SP
5833 032550 004737 035714      SPDAT          :POINTER TO DATA
5834 032554 042737 000017 032570 1$:  BIC     #17,25     :SET C BIT!
5835 032562 050037 032570      BIS     R0,25     :CLEAR ADDRESS FIELD OF INSTRUCTION
5836 032566 104412          ROMCLK          :ADD ADDRESS TO INSTRUCTION
5837 032570 010000          :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5838 032572 042737 000017 032606 2$:  BIC     #17,35     :LOAD MEM
5839 032600 050037 032606      BIS     R0,35     :CLEAR ADDRESS OF INSTRUCTION
5840 032604 104412          :ADD ADDRESS TO INSTRUCTION
5841 032606 040740 032606 3$:  ROMCLK          :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5842 032610 104412          :BR + SUB
5843 032612 061224          :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5844 032614 111205          :MOVE BR TO PORT4
5845 032616 116104 000004      MOVB   (R2),R5     :PUT "EXPECTED" IN R5
5846 032622 120504          MOVB   4(R1),R4    :PUT "FOUND" IN R4
5847 032624 001401          CMPB   R5,R4      :DATA CORRECT?
5848 032626 104015          BEQ    #4         :BR IF YES
5849 032630 104405          ERROR   #15     :ALU ERROR
5850 032632 005202          SCOPI          :SMO9=1*
5851 032634 005200          INC     R2        :NEXT DATA
5852 032636 022700 000010    INC     R0        :NEXT ADDRESS
5853 032642 001342          CMP     #10,R0   :DONE YET?
5854 032644 104420          BNE    #5        :BR IF NO
                    ADVANCE          :ADVANCE LOOP

```

5855 032646 000 001 377 58: .BYTE 0,1,-1,0,0,253,125,0  
5856 032651 000 000 253  
5857 032654 125 000  
5858 .EVEN

\*\*\*\*\* TEST 122 \*\*\*\*\*  
\*ALU TEST  
\*TEST OF ALU FUNCTION ADD M/C WITH C BIT SET  
\*ALU FUNCTION (A PLUS B PLUS C) CODE=01  
\*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA  
\*PERFORM THE FUNCTION, VERIFY THE RESULTS  
\*\*\*\*\*

TEST 122

5872 032656 000004  
5873 032660 012737 000122 001202  
5874 032666 012737 033034 001442  
5875 032674 012737 032726 001444  
5876  
5877 032702 104410  
5878 032704 005000  
5879 032706 012702 033024  
5880 032712 004737 035602  
5881 032716 035726  
5882 032720 004737 035636  
5883 032724 035736  
5884 032726 004737 035714 18:  
5885 032732 042737 000017 032746  
5886 032740 050037 032746  
5887 032744 104412  
5888 032746 010000 28:  
5889 032750 042737 000017 032764  
5890 032756 050037 032764  
5891 032762 104412 38:  
5892 032764 040420  
5893 032766 104412  
5894 032770 061224  
5895 032772 111205  
5896 032774 116104 000004  
5897 033000 120504  
5898 033002 001401  
5899 033004 104015  
5900 033006 104405 48:  
5901 033010 005202  
5902 033012 005200  
5903 033014 022700 000010  
5904 033020 071342  
5905 033022 104420  
5906 033024 001 000 000 58:  
5907 033027 377 253 000  
5908 033032 000 125  
5909 .EVEN  
5910

\*\*\*\*\*  
TST122: SCOPE  
MOV R122,STSTNM ; LOAD THE NO. OF THIS TEST  
MOV R123,NEXT ; POINT TO THE START OF NEXT TEST.  
MOV R18,LOCK ; ADDRESS FOR LOCK ON DATA.  
; R1 CONTAINS BASE KNC11 ADDRESS  
MSTCLR ; MASTER CLEAR KNC11  
CLR R0 ; MEM + SP ADDRESS  
MOV R55,R2 ; POINTER TO CORRECT DATA  
JSR PC,NEFLD ; LOAD 8 WORDS OF MAIN MEMORY  
MENDAT ; POINTER TO DATA  
JSR PC,SPLD ; LOAD 8 WORDS OF SP  
SPOAT ; POINTER TO DATA  
JSR PC,SETC ; SET C BIT!  
BIC R17,R28 ; CLEAR ADDRESS FIELD OF INSTRUCTION  
BIS R0,R28 ; ADD ADDRESS TO INSTRUCTION  
RONCLK PC=5304 ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
LOAD R0 ; LOAD R0  
BIC R17,R28 ; CLEAR ADDRESS OF INSTRUCTION  
BIS R0,R28 ; ADD ADDRESS TO INSTRUCTION  
RONCLK PC=5304 ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
R0 = ADD M/C ; R0 = ADD M/C  
RONCLK PC=5304 ; NEXT WORD IS INSTRUCTION, RONCLK PC=5304  
MOVE R0 TO PORT4 ; MOVE R0 TO PORT4  
PUT "EXPECTED" IN R5 ; PUT "EXPECTED" IN R5  
PUT "FOUND" IN R4 ; PUT "FOUND" IN R4  
DATA CORRECT? ; DATA CORRECT?  
BR IF YES ; BR IF YES  
ALU ERROR ; ALU ERROR  
STOP? ; STOP?  
NEXT DATA ; NEXT DATA  
NEXT ADDRESS ; NEXT ADDRESS  
DONE YET? ; DONE YET?  
BR IF NO ; BR IF NO  
ADVANCE LOOP ; ADVANCE LOOP  
58: .BYTE 1,0,0,-1,253,0,0,125



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5923 033034 000004
5924 033036 012737 000123 001202
5925 033044 012737 033212 001442
5926 033052 012737 033104 001444
5927
5928 033060 104410
5929 033062 005000
5930 033064 012702 033202
5931 033070 004737 035602
5932 033074 035726
5933 033076 004737 035636
5934 033102 035736
5935 033104 004737 035714
5936 033110 042737 000017 033124
5937 033116 050037 033124
5938 033122 104412
5939 033124 010000
5940 033126 042737 000017 033142
5941 033134 050037 033142
5942 033140 104412
5943 033142 040440
5944 033144 104412
5945 033146 061224
5946 033150 111205
5947 033152 116104 000004
5948 033156 120504
5949 033160 001401
5950 033162 104015
5951 033164 104405
5952 033166 005202
5953 033170 005200
5954 033172 022700 000010
5955 033176 001342
5956 033200 104420
5957 033202 000 001 377
5958 033205 000 000 253
5959 033210 125 000
5960
5961
5962
5963
5964
5965
5966

```

```

***** TEST 123 *****
*ALU TEST
*TEST OF ALU FUNCTION SUB W/C WITH C BIT SET
*ALU FUNCTION (A-B-C) CODE=2
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

TEST 123
-----
*****
†ST123: SCOPE
MOV #123,STSTNM ; LOAD THE NO. OF THIS TEST
MOV #ST124,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #1$,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
; MASTER CLEAR KMC11
; MEM + SP ADDRESS
; POINTER TO CORRECT DATA
; LOAD 8 WORDS OF MAIN MEMORY
; POINTER TO DATA
; LOAD 8 WORDS OF SP
; POINTER TO DATA
1$: JSR PC,SETC ; SET C BIT!
BIC #17,2$ ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS #0,2$ ; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2$: ROMCLK 010000 ; LOAD RAR
BIC #17,3$ ; CLEAR ADDRESS OF INSTRUCTION
BIS #0,3$ ; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3$: ROMCLK 040400!(<2*20>) ; BR + SUB W/C
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; MOVE BR TO PORT4
; PUT "EXPECTED" IN R5
; PUT "FOUND" IN R4
; DATA CORRECT?
; BR IF YES
; ALU ERROR
4$: SCOPI ; SMO=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE 1$ ; BR IF NO
; ADVANCE LOOP
5$: .BYTE 0,1,-1,0,0,253,125,0
.EVEN

```

```

***** TEST 124 *****
*ALU TEST
*TEST OF ALU FUNCTION INC A WITH C BIT SET
*ALU FUNCTION (A PLUS 1) CODE=3

```

```

5967 ;#LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
5968 ;#PERFORM THE FUNCTION, VERIFY THE RESULTS
5969 ;:*****~*****
5970
5971 ; TEST 124
5972 -----
5973 ;:*****~*****
5974 033212 000004 TST124: SCOPE
5975 033214 012737 000124 001202 MOV #124,STSTNM ; LOAD THE NO. OF THIS TEST
5976 033222 012737 033370 001442 MOV #TST125,NEXT ; POINT TO THE START OF NEXT TEST.
5977 033230 012737 033262 001444 MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.
5978 ; R1 CONTAINS BASE KMC11 ADDRESS
5979 033236 104410 MSTCLR ; MASTER CLEAR KMC11
5980 033240 005000 CLR R0 ; MEM + SP ADDRESS
5981 033242 012702 033360 MOV #55,R2 ; POINTER TO CONNECT DATA
5982 033246 004737 035602 JSR PC,MEMLO ; LOAD 8 WORDS OF MAIN MEMORY
5983 033252 035726 MEMDAT ; POINTER TO DATA
5984 033254 004737 035636 JSR PC,SPLD ; LOAD 8 WORDS OF SP
5985 033260 035736 SPDAT ; POINTER TO DATA
5986 033262 004737 035714 JSR PC,SETC ; SET C BIT!
5987 033266 042737 000017 033302 15: BIC #17,25 ; CLEAR ADDRESS FIELD OF INSTRUCTION
5988 033274 050037 033302 BIS R0,25 ; ADD ADDRESS TO INSTRUCTION
5989 033300 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5990 033302 010000 25: 010000 ; LOAD NAR
5991 033304 042737 000017 033320 BIC #17,35 ; CLEAR ADDRESS OF INSTRUCTION
5992 033312 050037 033320 BIS R0,35 ; ADD ADDRESS TO INSTRUCTION
5993 033316 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5994 033320 040460 35: 040460 (<3>20) ; BR + INC A
5995 033322 104412 ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
5996 033324 061224 61224 ; MOVE BR TO PORT4
5997 033326 111205 MOVB (R2),R5 ; PUT "EXPECTED" IN R5
5998 033330 116104 000004 MOVB 4(R1),R4 ; PUT "FOUND" IN R4
5999 033334 120504 CNPB R5,R4 ; DATA CORRECT?
6000 033336 001401 BEQ 45 ; BR IF YES
6001 033340 104015 ERROR 15 ; ALU ERROR
6002 033342 104405 45: SCOPE 5009=1 ; NEXT DATA
6003 033344 005202 INC R2 ; NEXT ADDRESS
6004 033346 005200 INC R0 ; NEXT ADDRESS
6005 033350 022700 000010 CNP #10,R0 ; DONE YET?
6006 033354 001342 BNE 15 ; BR IF NO
6007 033356 104420 ADVANCE ; ADVANCE LOOP
6008 033360 001 001 000 55: .BYTE 1,1,0,0,126,126,253,253
6009 033363 007 126 126
6010 033366 253 253
6011 ;.EVEN
6012
6013 ;*****~***** TEST 125 *****~*****
6014 ;#ALU TEST
6015 ;#TEST OF ALU FUNCTION 2A WITH C BIT SET
6016 ;#ALU FUNCTION (A PLUS A) CODE=5
6017 ;#LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
6018 ;#PERFORM THE FUNCTION, VERIFY THE RESULTS
6019 ;:*****~*****
6020
6021 ; TEST 125
6022

```

```

6023
6024
6025 033370 000004
6026 033372 012737 000125 001202
6027 033400 012737 033546 001442
6028 033406 012737 033440 001444
6029
6030 033414 104410
6031 033416 005000
6032 033420 012702 033536
6033 033424 004737 035602
6034 033430 035726
6035 033432 004737 035636
6036 033436 035736
6037 033440 004737 035714
6038 033444 042737 000017 033460 15:
6039 033452 050037 033460
6040 033456 104412
6041 033460 010000
6042 033462 042737 000017 033476 25:
6043 033470 050037 033476
6044 033474 104412
6045 033476 040520
6046 033500 104412
6047 033502 061224
6048 033504 111205
6049 033506 116104 000004
6050 033512 120504
6051 033514 001401
6052 033516 104015
6053 033520 104405
6054 033522 005202
6055 033524 005200
6056 033526 022700 000010
6057 033532 001342
6058 033534 104420
6059 033536 000 000 376
6060 033541 376 252
6061 033544 124 124
6062 .EVEN
6063
6064
6065
6066
6067
6068
6069
6070
6071
6072
6073
6074
6075
6076 033546 000004
6077 033550 012737 000126 001202
6078 033556 012737 033724 001442

```

```

:*****
TST125: SCOPE
MOV #125,$STSNM ; LOAD THE NO. OF THIS TEST
MOV #TST126,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #18,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KNC11 ADDRESS
MSTCLR ; MASTER CLEAR KNC11
CLR R0 ; R0 ← SP ADDRESS
MOV #58,R2 ; POINTER TO CONNECT DATA
JSR PC,MEHLD ; LOAD 8 WORDS OF MAIN MEMORY
MENDAT ; POINTER TO DATA
JSR PC,SPLD ; LOAD 8 WORDS OF SP
SPDAT ; POINTER TO DATA
JSR PC,SETC ; SET C BIT!
BIC #17,25 ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS #0,25 ; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
ROMCLK 010000 ; LOAD MM
BIC #17,38 ; CLEAR ADDRESS OF INSTRUCTION
BIS #0,38 ; ADD ADDRESS TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
ROMCLK 040400!(5*20) ; BR ← 2A
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
MOV #2A ; MOVE BR TO PORT4
MOV #R2,R5 ; PUT "EXPECTED" IN R5
MOV #4(R1),R4 ; PUT "FOUND" IN R4
CMPB R5,R4 ; DATA CORRECT?
BEQ #4 ; BR IF YES
ERROR #15 ; ALU ERROR
SCOPI #1 ; SMO=1?
INC R2 ; NEXT DATA
INC R0 ; NEXT ADDRESS
CMP #10,R0 ; DONE YET?
BNE #18 ; BR IF NO
ADVANCE ; ADVANCE LOOP
.BYTE 0,0,376,376,252,252,124,124
55:

```

```

:***** TEST 126 *****
*ALU TEST
*TEST OF ALU FUNCTION A PLUS C WITH C BIT SET
*ALU FUNCTION (A PLUS C) CODE=4
*LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
*PERFORM THE FUNCTION, VERIFY THE RESULTS
:*****
; TEST 126
:*****
TST126: SCOPE
MOV #126,$STSNM ; LOAD THE NO. OF THIS TEST
MOV #TST127,NEXT ; POINT TO THE START OF NEXT TEST.

```

6079	033564	012737	033616	001444	MOV	#15,LOCK				R1 CONTAINS BASE KMC11 ADDRESS
6080										MASTER CLEAR KMC11
6081	033572	104410			MSTCLR					MEM + SP ADDRESS
6082	033574	005000			CLR	R0				POINTER TO CORRECT DATA
6083	033576	012702	033714		MOV	#55,R2				LOAD 8 WORDS OF MAIN MEMORY
6084	033578	004737	035602		JSR	PC,NEALD				POINTER TO DATA
6085	033578	035726			MEMDAT					LOAD 8 WORDS OF SP
6086	033570	004737	035636		JSR	PC,SPLD				POINTER TO DATA
6087	033514	035736			SPDAT					SET C BIT!
6088	033516	004737	035714	15:	JSR	PC,SETC				CLEAR ADDRESS FIELD OF INSTRUCTION
6089	033522	042737	000017	033636	BIC	#17,25				ADD ADDRESS TO INSTRUCTION
6090	033630	050037	033636		BIS	R0,25				NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6091	033634	104412			ROMCLK					LOAD WBR
6092	033636	010000			D10000					CLEAR ADDRESS OF INSTRUCTION
6093	033640	042737	000017	033654	BIC	#17,35				ADD ADDRESS TO INSTRUCTION
6094	033646	050037	033654		BIS	R0,35				NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6095	033652	104412			ROMCLK					BR + A PLUS C
6096	033654	040500			040500:(4#20)					NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6097	033656	104412			ROMCLK					MOVE BR TO PORT4
6098	033660	061224			61224					PUT "EXPECTED" IN R5
6099	033662	111205			MOV8	(R2),R4				PUT "FOUND" IN R4
6100	033664	116104	000004		MOV8	4(R1),R4				DATA CORRECT?
6101	033670	120504			CHP8	R5,R4				BR IF YES
6102	033672	001401			BEG	48				ALU ERROR
6103	033674	104015			ERROR	15				SND=1?
6104	033676	104405			SCOPI					NEXT DATA
6105	033700	005202			INC	R2				NEXT ADDRESS
6106	033702	005200			INC	R0				DONE YET?
6107	033704	022700	000010		CHP	#10,R0				BR IF NO
6108	033710	001342			BNE	15				ADVANCE LOOP
6109	033712	104420			ADVANCE					
6110	033714	001	001	000	.BYTE	1,1,0,0,126,126,253,253				
6111	033717	000	126	126						
6112	033722	253	253							

.EVEN

```

***** TEST 127 *****
#ALU TEST
#TEST OF ALU FUNCTION 2'S COMP SUB WITH C BIT SET
#ALU FUNCTION (A-B-1) CODE=17
#LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
#PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 127

```

*****
TST127: SCOPE
MOV #127,$STNM ; LOAD THE NO. OF THIS TEST
MOV #TST130,NEXT ; POINT TO THE START OF NEXT TEST.
MOV #15,LOCK ; ADDRESS FOR LOCK ON DATA.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCLR ; MASTER CLEAR KMC11
CLR R0 ; MEM + SP ADDRESS
MOV #55,R2 ; POINTER TO CORRECT DATA

```

6135	033760	004737	035602				JSR	PC, MEMLD	LOAD 8 WORDS OF MAIN MEMORY
6136	033764	035726					MEMDAT		POINTER TO DATA
6137	033766	004737	035636				JSR	PC, SPLD	LOAD 8 WORDS OF SP
6138	033772	035736					SPOAT		POINTER TO DATA
6139	033774	004737	035714	1S:			JSR	PC, SETC	SET C BIT!
6140	034000	042737	000017	034014			BIC	#17, 2S	CLEAR ADDRESS FIELD OF INSTRUCTION
6141	034006	050037	034014				BIS	RO, 2S	ADD ADDRESS TO INSTRUCTION
6142	034012	104412					ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6143	034014	010000					010000		LOAD MEM
6144	034016	042737	000017	034032	2S:		BIC	#17, 3S	CLEAR ADDRESS OF INSTRUCTION
6145	034024	050037	034032				BIS	RO, 3S	ADD ADDRESS TO INSTRUCTION
6146	034030	104412					ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6147	034032	040760			3S:		040400!	(17#20)	BR + 2'S COMP SUB
6148	034034	104412					ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6149	034036	061224					61224		MOVE BR TO PORT4
6150	034040	111205					MOV8	(R2), R5	PUT "EXPECTED" IN R5
6151	034042	116104	000004				MOV8	4(R1), R4	PUT "FOUND" IN R4
6152	034046	120504					CHPB	R5, R4	DATA CONNECT?
6153	034050	001401					BEO	4S, R4	BR IF YES
6154	034052	104015					ERROR	15	ALU ERROR
6155	034054	104405			4S:		SCOPI		SMD=1?
6156	034056	005202					INC	R2	NEXT DATA
6157	034060	005200					INC	RO	NEXT ADDRESS
6158	034062	022700	000010				CHP	#10, RO	DONE YET?
6159	034066	001342					BNE	1S	BR IF NO
6160	034070	104420					ADVANCE		ADVANCE LOOP
6161	034072	377	000	376	5S:		.BYTE	-1, 0, 376, -1, -1, 252, 124, -1	
6162	034075	377	377	252					
6163	034100	124	377						
6164									.EVEN

```

***** TEST 130 *****
#ALU TEST
#TEST OF ALU FUNCTION DEC A WITH C BIT SET
#ALU FUNCTION (A-1) CODE=7
#LOAD MAIN MEM AND SP WITH 8 WORDS OF DATA
#PERFORM THE FUNCTION, VERIFY THE RESULTS
*****

```

TEST 130

6178	034102	000001					ST130: SCOPE		*****
6179	034104	012737	000130	001202			MOV	#130, STSTNH	LOAD THE NO. OF THIS TEST
6180	034112	012737	034260	001442			MOV	#ST131, NEXT	POINT TO THE START OF NEXT TEST.
6181	034120	012737	034152	001444			MOV	#1S, LOCK	ADDRESS FOR LOCK ON DATA.
6182									R1 CONTAINS BASE KMC11 ADDRESS
6183	034126	104410					MSTCLR		MASTER CLEAR KMC11
6184	034130	005000					CLR	RO	MEM + SP ADDRESS
6185	034132	012702	034250				MOV	#5S, R2	POINTER TO CONNECT DATA
6186	034136	004737	035602				JSR	PC, MEMLD	LOAD 8 WORDS OF MAIN MEMORY
6187	034142	035726					MEMDAT		POINTER TO DATA
6188	034144	004737	035636				JSR	PC, SPLD	LOAD 8 WORDS OF SP
6189	034150	035736					SPDAT		POINTER TO DATA
6190	034152	004737	035714	1S:			JSR	PC, SETC	SET C BIT!

6191	034156	012737	000017	034172	BIC	#17,25	;	CLEAR ADDRESS FIELD OF INSTRUCTION
6192	034172	050037	034172		BIS	RO,25	;	ADD ADDRESS TO INSTRUCTION
6193	034170	104412			ROMCLK		;	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6194	034172	010000			LOAD		;	LOAD M00
6195	034174	012737	000017	034210	BIC	#17,35	;	CLEAR ADDRESS OF INSTRUCTION
6196	034202	050037	034210		BIS	RO,35	;	ADD ADDRESS TO INSTRUCTION
6197	034206	104412			ROMCLK		;	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6198	034210	040560			040400!	<7*20>	;	BR + DEC A
6199	034212	104412			ROMCLK		;	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6200	034214	061224			MOV	BR TO PORT4	;	MOVE BR TO PORT4
6201	034216	111205			MOV	(R2),R5	;	PUT "EXPECTED" IN R5
6202	034220	116104	000004		MOV	4(R1),R4	;	PUT "FOUND" IN R4
6203	034224	120504			CMP	R5,R4	;	DATA CORRECT?
6204	034226	001401			BEQ	15	;	BR IF YES
6205	034230	104015			ERROR	15	;	ALU ERROR
6206	034232	104405			SCOPI		;	SHOW I?
6207	034234	005202			INC	R2	;	NEXT DATA
6208	034236	005200			INC	RO	;	NEXT ADDRESS
6209	034240	022700	000010		CMP	#10,RO	;	DONE YET?
6210	034244	001342			BNE	15	;	BR IF NO
6211	034246	104420			ADVANCE		;	ADVANCE LOOP
6212	034250	377	377	376	.BYTE	-1,-1,376,376,124,124,251,251	;	
6213	034253	376		124			;	
6214	034256	251		251			;	
6215							;	.EVEN

\*\*\*\*\* TEST 131 \*\*\*\*\*  
 \*TEST OF PROGRAM CLOCK BIT  
 \*ADD A MASTER CLEAR, VERIFY THAT PROGRAM CLOCK IS SET  
 \*WRITE PROGRAM CLOCK BIT TO A ONE, VERIFY THAT IT CLEARS,  
 \*AND THEN SETS SOME TIME LATER  
 \*\*\*\*\*

TEST 131

6228	034260	000004			TEST131: SCOPE		;	LOAD THE NO. OF THIS TEST
6229	034262	012737	000131	001202	MOV	#131,\$STMP	;	POINT TO THE START OF NEXT TEST.
6230	034270	012737	034466	001442	MOV	\$ST132,NEXT	;	R1 CONTAINS BASE KMC11 ADDRESS
6231					MSTCLR		;	MASTER CLEAR KMC11
6232	034276	104410			CLR	TEMP	;	PREFARE FOR
6233	034200	005037	011106		CLR	\$TMP0	;	DELAY
6234	034204	005037	001376		MOV	#11,R2	;	SAVE FOR TYPEOUT
6235	034210	012702	000011		ROMCLK		;	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6236	034214	104412			PORT4+LUI		;	PORT4+LUI
6237	034216	121224			MOV	4(R1),R4	;	PUT "FOUND" IN R4
6238	034220	016104	000004		BIC	#357,R4	;	CLEAR UNWANTED BITS
6239	034224	042704	000357		MOV	#20,R5	;	PUT "EXPECTED" IN R5
6240	034220	012705	000020		CMP	R5,R4	;	IS PGM CLOCK SET?
6241	034224	120504			BEQ	15	;	
6242	034226	001401			ERROR	16	;	ERROR, PGM CLOCK IS NOT SET
6243	034240	104016			MOV	#20,4(R1)	;	LOAD PORT 4
6244	034242	012761	000020	000004	BISB	#811,1(R1)	;	SET ROMI
6245	034250	152761	000002	000001	MOV	#121111,6(R1)	;	SEL6 + INSTRUCTION
6246	034256	012761	121111	000006			;	

6277	034364	152761	000003	000001	BISB	#BIT11,BIT0,1(R1)	SET CLOCK BIT
6278	034372	012761	121224	000006	MOV	#121224,6(R1)	LOAD NEXT INSTRUCTION
6279	034400	152761	000003	000001	BISB	#BIT11,BIT0,1(R1)	READ CLOCK BIT
6280	034406	142761	000003	000001	BICB	#BIT11,BIT0,1(R1)	CLEAR PAINT BITS
6281	034414	016104	000004		MOV	4(R1),R4	PUT "FOUND" IN R4
6282	034420	005005			CLR	R5	PUT "EXPECTED" IN R5
6283	034426	120504			CMPB	R5,R4	IS PGM CLOCK CLEAR?
6284	034426	001401			BEG	25	
6285	034426	104016			ERROR	16	;ERROR, PGM CLOCK IS NOT CLEAR
6286	034430			25:			
6287	034430	104412			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6288	034430	121224			121224		PORT4+LUI1
6289	034434	122761	000020	000004	CMPB	#20,4(R1)	IS PGM CLOCK SET?
6290	034442	001411			BEG	35	BR IF YES
6291	034444	005237	011106		INC	TEMP	INCREMENT DELAY
6292	034450	005537	001276	001276	ADC	\$TMP0	INCREMENT DELAY
6293	034454	022737	000006	001276	CMP	#6,\$TMP0	IS DELAY DONE
6294	034462	001362			BNE	25	BR IF NO
6295	034464	104016			ERROR	16	;ERROR PGM CLOCK NOT SET
6296	034466			35:			

```

***** TEST 132 *****
#FORCE POWER FAIL TEST
#SET FORCE POWER FAIL BIT VERIFY THAT PROCESSOR TRAPS TO 24
#GOING DOWN AND COMING UP. VERIFY ALSO THAT BUS INIT WAS
#BLOCKED FROM GETTING TO THE KMC DURING THE POWER FAIL
*****

```

TEST 132

```

*****
TST132: SCOPE
MOV #122,$STNMY ; LOAD THE NO. OF THIS TEST
MOV #TST133,NEXT ; POINT TO THE START OF NEXT TEST.
; R1 CONTAINS BASE KMC11 ADDRESS
MSTCL11 ; MASTER CLEAR KMC11
CLR TEMP ; PREPARE FOR DELAY
MOV #2#24,-(SP) ; STORE POWER FAIL ADDRESS
MOV #15,#2#24 ; SET UP FOR FORCE POWER FAIL
MOV #2,4(R1) ; LOAD PORT4
MOV #BIT9,(R1) ; SET R0M1
MOV #121111,6(R1) ; LOAD INSTRUCTION
MOV #BIT9,BIT8,(R1) ; CLOCK INSTRUCTION
55: INC TEMP ; WAIT FOR POWER FAIL
BNE 55 ; BR IF DELAY NOT DONE
ERROR 17 ; ERROR, NO POWER FAIL
BR 45
6295: MOV #35,#2#24 ; POWER UP ADDRESS
6296: MOV SP,25 ; STORE STACK
6297: HALT ; WAIT FOR POWER UP SEQUENCE
6298: 0 ;
6299: 35: MOV 25,SP ; RESTORE STACK
6300: POP2SP ; POP STACK TWICE
6301: MOV (SP)+,#2#24 ; RESTORE TRUE POWER FAIL ADDRESS
6302: CMP #SPWRDN,#2#24 ; IS IT CORRECT?

```

```

6303 034630 001406 BEQ 45 ;BR IF YES
6304 034622 104017 ERROR 17 ;ERROR STACK IS INCORRECT
6305 034624 012737 007126 000024 MOV #SPWRD,SP ;RESTORE TRUE POWER FAIL ADDRESS
6306 034632 012706 001200 MOV #STACK,SP ;RESTORE STACK
6307 034636 012711 003000 45: MOV #BIT9:BIT10,(R1) ;SEL6 = MAINT IR
6308 034642 012705 121111 MOV #121111,R5 ;RS = EXPECTED
6309 034646 016104 000004 MOV 4(R1),R4 ;R4 = FOUND
6310 034652 020504 CMP R5,R4 ;MAINT IR SHOULD = 12111
6311 034654 001401 BEQ +4 ;BR IF OK
6312 034656 104025 ERROR 25 ;IF = 0 THEN BUS INIT WAS
;NOT BLOCKED FROM CLEARING
;THE KMC-11

```

```

***** TEST 133 *****
;MICRO-PROCESSOR NOISE TEST
;WRITE ALL ZERO'S THEN ALL ONE'S THEN A DATA PATTERN
;TO THE IBUS* AND IBUS REGISTERS AND TO THE SP AND MAIN MEM
;THEN GO BACK AND READ THE DATA PATTERNS TO VERIFY THAT
;READING AND WRITING OF OTHER LOCATIONS AND REGISTERS
;DID NOT CHANGE THE DATA.
*****

```

TEST 133

```

6329 034660 000004 ;*****
6330 034662 012737 000133 001202 †ST133: SCOPE
6331 034670 012737 003662 001442 MOV #133,$STNM ; LOAD THE NO. OF THIS TEST
MOV #SEOP,NEXT ; POINT TO THE END OF PASS HANDLER.
6332 ;R1 CONTAINS BASE KMC11 ADDRESS
6333 034676 104110 MSTCLR ;MASTER CLEAR KMC11
6334 034700 005002 CLR R2 ;R2 IS INDEX REGISTER
6335 034702 042737 000017 034726 15: BIC #17,25 ;CLEAR ADDRESS FIELD
6336 034710 156237 035502 034726 BISB 305(R2),25 ;ADD IBUS* REG ADDRESS TO INSTRUCTION
6337 034716 116261 035510 000004 MOVB 315(R2),4(R1) ;LOAD PORT4
6338 034724 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6339 034726 121100 25: WRITE IBUS* REGISTER
6340 034730 005202 INC R2 ;INC INDEX REGISTER
6341 034732 022702 000005 CMP #5,R2 ;DONE YET?
6342 034736 001361 BNE 15 ;BR IF NO
6343 034740 005002 CLR R2 ;R2 IS IBUS REGISTER ADDRESS
6344 034742 042737 000017 035006 35: BIC #17,45 ;CLEAR ADDRESS FIELD OF INSTRUCTIONS
6345 034750 042737 000017 035020 BIC #17,55
6346 034756 042737 000017 035030 BIC #17,65
6347 034764 050237 035006 ;ADD IBUS REG ADDRESS TO INSTRUCTION
6348 034770 050237 035020 BIS R2,45
6349 034774 050237 035030 BIS R2,55
6350 035000 105061 000004 CLR R2 ;CLEAR PORT4
6351 035004 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6352 035006 122100 45: WRITE 0 TO IBUS REG
6353 035010 112761 000377 000304 MOVB #377,4(R1) ;LOAD PORT4
6354 035016 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6355 035020 122100 55: WRITE ALL ONES TO IBUS REG
6356 035022 110261 000004 MOVB R2,4(R1) ;LOAD PORT4
6357 035026 104412 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6358 035030 122100 65: WRITE ITS OWN ADDRESS TO IBUS REG

```



6359	035132	005202				INC	R2		:NEXT ADDRESS
6360	035134	022702	000010			CMP	#10,R2		:DONE YET?
6361	035040	001340				BNE	3\$		:BR IF NO
6362	035042	005002				CLR	R2		:START AT SP ADDRESS 0
6363	035044	042737	000017	035110	75:	BIC	#17,8\$		:CLEAR ADDRESS FIELD
6364	035052	042737	000017	035122		BIC	#17,9\$		
6365	035060	042737	000017	035132		BIC	#17,10\$		
6366	035066	050237	035110			BIS	R2,8\$		:ADD ADDRESS TO INSTRUCTION
6367	035072	050237	035122			BIS	R2,9\$		
6368	035076	050237	035132			BIS	R2,10\$		
6369	035102	105061	000004			CLRB	4(R1)		:CLEAR PORT4
6370	035106	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6371	035110	123100			85:	123100			:WRITE ZERO TO SP
6372	035112	112761	000377	000004		MOVB	#377,4(R1)		:LOAD PORT4
6373	035120	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6374	035122	123100			95:	123100			:WRITE ALL ONES TO SP
6375	035124	110261	000004			MOVB	R2,4(R1)		:LOAD PORT4
6376	035130	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6377	035132	123100			105:	123100			:WRITE SP ADDRESS TO ITSELF
6378	035134	005202				INC	R2		:NEXT SP ADDRESS
6379	035136	022702	000020			CMP	#20,R2		:DONE YET?
6380	035142	001340				BNE	7\$		:BR IF NO
6381	035144	005002				CLR	R2		:R2 = MAIN MEM ADDRESS
6382	035146	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6383	035150	010000				010000			:MAR + 0
6384	035152	105061	000004		115:	CLRB	4(R1)		:CLEAR PORT4
6385	035156	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6386	035160	122500				122500			:WRITE ZEROS TO MEM
6387	035162	112761	000377	000004		MOVB	#377,4(R1)		:LOAD PORT4
6388	035170	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6389	035172	122500				122500			:WRITE ONES TO MEM
6390	035174	110261	000004			MOVB	R2,4(R1)		:LOAD PORT4
6391	035200	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6392	035202	136500				136500			:WRITE TO MEM IT OWN ADDRESS
6393	035204	105202				INC	R2		:NEXT MEM ADDRESS
6394	035206	022702	001000			CMP	#1000,R2		:DONE YET?
6395	035212	001357				BNE	11\$		:BR IF NO
6396									
6397									:NOW GO BACK AND READ EVERYTHING
6398									
6399	035214	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6400	035216	010000				010000			:MAR+0
6401	035220	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6402	035222	004000				4000			:MAR HI + 0 (KMC ONLY)
6403	035224	005000				CLR	R0		:R0 IS INDEX REGISTER
6404	035226	042737	000360	035264	125:	BIC	#360,13\$		:CLEAR ADDRESS FIELD
6405	035234	116002	035502			MOVB	30\$(R0),R2		:R2 = IBUS* ADDRESS
6406	035240	010203				MOV	R2,R3		:PUT IBUS* ADDRESS IN R3
6407	035242	006303				ASL	R3		:SHIFT ADDRESS TO BITS 4-7
6408	035244	006303				ASL	R3		
6409	035246	006303				ASL	R3		
6410	035250	006303				ASL	R3		
6411	035252	050337	035264			BIS	R3,13\$		:ADD ADDRESS TO INSTRUCTION
6412	035256	116005	035510			MOVB	31\$(R0),R5		:R5 = "EXPECTED"
6413	035262	104412				ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6414	035264	121004			135:	121004			:PORT4 + IBUS* REGISTER

6415	035266	016104	000004		MOV	4(R1),R4		:R4 = "FOUND"
6416	035272	120504			CMPB	R5,R4		:IBUS# CONTENTS OK?
6417	035274	001401			BEG	+4		:BR IF YES
6418	035276	104004			ERROR	4		:IBUS# DATA ERROR
6419	035300	005200			INC	R0		:INC COUNTER
6420	035302	022700	000005		CMP	#5,R0		:DONE YET?
6421	035306	001347			BNE	12\$		:BR IF NO
6422	035310	005002			CLR	R2		:R2 = IBUS REG ADDRESS
6423	035312	042737	000360	035342	14\$:	BIC	#360,15\$	:CLEAR ADDRESS FIELD OF INSTRUCTION
6424	035320	010203			MOV	R2,R3		:R3 = IBUS ADDRESS
6425	035322	006303			ASL	R3		:SHIFT ADDRESS TO BITS 4-7
6426	035324	006303			ASL	R3		
6427	035326	006303			ASL	R3		
6428	035330	006303			ASL	R3		
6429	035332	050337	035342		BIS	R3,15\$		:ADD ADDRESS TO INSTRUCTION
6430	035336	010205			MOV	R2,R5		:R5 = "EXPECTED"
6431	035340	104412			ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6432	035342	021004		15\$:	PORT4	* IBUS REG		
6433	035344	016104	000004		MOV	4(R1),R4		:R4 = "FOUND"
6434	035350	120504			CMPB	R5,R4		:IBUS CONTENTS OK?
6435	035352	001401			BEG	+4		:BR IF YES
6436	035354	104005			ERROR	5		:IBUS DATA ERROR
6437	035356	015202			INC	R2		:NEXT IBUS REGISTER
6438	035360	022702	000010		CMP	#10,R2		:DONE YET?
6439	035364	001352			BNE	14\$		:BR IF NO
6440	035366	005002			CLR	R2		:R2 = SP ADDRESS
6441	035370	042737	000017	035404	16\$:	BIC	#17,17\$	:CLEAR ADDRESS FIELD OF INSTRUCTION
6442	035376	050237	035404		BIS	R2,17\$		:ADD ADDRESS TO INSTRUCTION
6443	035402	104412			ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6444	035404	040600		17\$:	BR	* SP		
6445	035406	010205			MOV	R2,R5		:R5 = "EXPECTED"
6446	035410	104412			ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6447	035412	061224			PORT4	* BR		
6448	035414	016104	000004		MOV	4(R1),R4		:R4 = "FOUND"
6449	035420	120504			CMPB	R5,R4		:SP CONTENTS OK?
6450	035422	001401			BEG	+4		:BR IF YES
6451	035424	104007			ERROR	7		:SP DATA ERROR
6452	035426	005202			INC	R2		:NEXT SP LOCATION
6453	035430	022702	000020		CMP	#20,R2		:DONE YET?
6454	035434	001355			BNE	16\$		:BR IF NO
6455	035436	005002			CLR	R2		:R2 = MEMORY ADDRESS
6456	035440	104412			ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6457	035442	010000			RRR	* 0		
6458	035444	104412			ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6459	035446	004000			RRR	#1 * 0 (KMC ONLY)		
6460	035450	010205		18\$:	MOV	R2,R5		:R5 = "EXPECTED"
6461	035452	104412			ROMCLK			:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6462	035454	055224			PORT4	* MAIN MEM		
6463	035456	016104	000004		MOV	4(R1),R4		:R4 = "FOUND"
6464	035462	120504			CMPB	R5,R4		:MAIN MEM CONTENTS OK?
6465	035464	001401			BEG	+4		:BR IF YES
6466	035466	104013			ERROR	13		:MAIN MEM DATA ERROR
6467	035470	005202			INC	R2		:NEXT MEM ADDRESS
6468	035472	022702	001000		CMP	#1000,R2		:DONE YET?
6469	035476	001364			BNE	18\$		:BR IF NO
6470	035500	104420			ADVANCE			:ADVANCE LOOP

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```

6471 035502 000 002 003 30S: .BYTE 0,2,3,5,10
6472 035505 005 010
6473 035510 035510
6474 035510 001 003 004 31S: .BYTE 1,3,4,6,10
6475 035513 006 010
6476 035516 .EVEN
6477
6478
6479
6480
6481
6482 035516
6483
6484
6485 035516 012577 144334
6486 035522 012577 144334
6487 035526 112577 144326
6488 035532 112577 144326
6489 035536 000205
6490
6491
6492 035540
6493
6494
6495
6496 035540 010246
6497 035542 005002
6498 035544 112561 000004
6499 035550 042737 000017 035564
6500 035556 050237 035564
6501 035562 104412
6502 035564 122100
6503 035566 005202
6504 035570 022702 000010
6505 035574 001363
6506 035576 012602
6507 035600 000205
6508
6509
6510 035602
6511
6512
6513
6514 035602 013605
6515 035604 062746 000002
6516 035610 012704 000010
6517 035614 104412
6518 035616 010000
6519 035620 112577 144250
6520 035624 104412
6521 035626 136500
6522 035630 005304
6523 035632 001372
6524 035634 000207
6525
6526
    
```

; SUBROUTINES

SETVEC: ; THIS SUBROUTINE LOADS THE VECTORS AND VECTOR LEVELS

```

MOV (R5)+, 2(KHVEC) ; LOAD BASE VECTOR
MOV (R5)+, 2(KHTEC) ; LOAD VECTOR + 2
MOVB (R5)+, 2(KHRLVL) ; LOAD VECTOR + 4
MOVB (R5)+, 2(KHRTLVL) ; LOAD VECTOR + 6
RTS R5 ; RETURN
    
```

NPRSET: ; THIS SUBROUTINE LOADS IBUS REGISTERS 0-7  
 ; WITH NPR INFORMATION (INBA, OUTBA, OUT DATA)

```

MOV R2, -(SP) ; SAVE R2
CLR R2 ; START AT IBUS REG 0
MOVB (R5)+, 4(R1) ; LOAD PORT4
BIC #17, R2 ; CLEAR ADDRESS FIELD OF INSTRUCTION
BIS R2, 28 ; ADD ADDRESS TO INSTRUCTION
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1S: 122100 ; MOVE PORT4 TO IBUS REG
2S: ; NEXT ADDRESS
INC R2 ; ALL DONE?
CMP #10, R2 ; BR IF NO
BNE 1S ; RESTORE R2
MOV (SP)+, R2 ; RETURN
RTS R5
    
```

MEMLD: ; THIS SUBROUTINE LOADS THE FIRST 8 LOCATIONS OF MAIN  
 ; MEMORY WITH THIS DATA: 0, -1, 0, -1, 125, 252, 125, 252

```

MOV 2(SP)+, R5 ; PUT POINTER TO DATA IN R5
ADD #2, -(SP) ; ADJUST STACK
MOV #10, R4 ; DO 8 LOADS
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
010000 ; MAR ( 0
1S: MOVB (R5)+, 2(KMP04) ; LOAD PORT4
ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
136500 ; MOV DATA TO MEM, AUTO INC MAR
DEC R4 ; DECREMENT COUNT
BNE 1S ; BR IF NOT DONE
RTS PC ; RETURN
    
```

```

6527 035636          SPLD:
6528                ; THIS SUBROUTINE LOADS THE FIRST 8 SCRATCH PAD
6529                ; LOCATIONS WITH: 0,0,-1,-1,125,125,252,252
6530
6531 035636 013605      MOV    @ (SP)+,R5      ; PUT POINTER TO DATA IN R5
6532 035640 062746      ADD    #2,-(SP)      ; ADJUST STACK
6533 035644 005004      CLR    R4            ; START AT SP ADDRESS 0
6534 035646 112577      MOVB  (R5)+,@KMP04   ; LOAD PORT4 WITH DATA
6535 035652 042737      BIC   #17,25        ; CLEAR ADDRESS FIELD OF INSTRUCTION
6536 035660 050437      BIS   R4,25        ; ADD ADDRESS TO INSTRUCTION
6537 035664 104412      ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6538 035666 123100      25: 123100      ; MOVE DATA TO SP
6539 035670 005204      INC   R4            ; INCREMENT COUNT
6540 035672 022704      CMP   #10,R4       ; DONE YET?
6541 035676 001363      BNE  IS            ; BR IF NO
6542 035700 000207      RTS   PC           ; RETURN
6543
6544
6545 035702          CLRC:
6546                ; THIS SUBROUTINE CLEARS THE MICRO PROCESSOR C BIT
6547
6548 035702 104412      ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6549 035704 010000      010000      ; MAR=0
6550 035706 104412      ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6551 035710 040400      040400! (<0*20) ; CLEAR C BIT
6552 035712 000207      RTS   PC           ; RETURN
6553
6554
6555 035714          SETC:
6556                ; THIS SUBROUTINE SETS THE MICRO PROCESSOR C BIT
6557
6558 035714 104412      ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6559 035716 010003      010003      ; MAR=3
6560 035720 104412      ROMCLK ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
6561 035722 040403      040403! (<0*20) ; SET C BIT
6562 035724 000207      RTS   PC           ; RETURN
6563
6564
6565 035726          MEMDAT: .BYTE 0,-1,0,-1,125,252,125,252
6566 035731          377      125      252
6567 035734          125      252
6568 035736          000      000      377 SPDAT: .BYTE 0,0,-1,-1,125,125,252,252
6569 035741          377      125      125
6570 035744          252      252
6571
6572 035746          .EVEN
036013          052500 044516 052502 EM1: .ASCIZ (<200>/UNABLE REGISTER ADDRESSING TIME-OUT/
036013          200 047125 041111 EM2: .ASCIZ (<200>/MIRBUS REGISTER WRITE/READ TEST/
036054          046600 041511 047522 EM3: .ASCIZ (<200>/MIRRO PROCESSOR TEST/
036102          046600 041511 047522 EM4: .ASCIZ (<200>/MIRRO PROCESSOR WRITE/READ TEST/
036143          200 051102 051040 EM5: .ASCIZ (<200>/MAR REGISTER TEST/
036165          200 041523 040522 EM6: .ASCIZ (<200>/SCRATCH PAD TEST/
036207          200 042504 044526 EM7: .ASCIZ (<200>/DEVICE FAILED TO INTERRUPT/
036243          200 042504 044526 EM10: .ASCIZ (<200>/DEVICE INTERRUPTED TO WRONG VECTOR/
036307          200 050116 020122 EM11: .ASCIZ (<200>/MAR TEST/
036321          200 040515 047111 EM12: .ASCIZ (<200>/MAIN MEMORY TEST/
036343          200 040515 020122 EM13: .ASCIZ (<200>/MAR TEST/
    
```

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036355	200	046101	020125	EM14:	.ASCIZ	<200>/ALU TEST/		
036367	200	051120	043517	EM15:	.ASCIZ	<200>/PROGRAM CLOCK TEST/		
036413	200	047506	041522	EM16:	.ASCIZ	<200>/FORCE POWER FAIL ERROR/		
036443	200	047125	054105	EM17:	.ASCIZ	<200>/UNEXPECTED INTERRUPT/		
036471	200	046513	030503	EM20:	.ASCIZ	<200>/KMC11 CONFIGURATION ERROR/		
036524	046600	044501	052116	EM21:	.ASCIZ	<200>/MAINTENANCE INSTRUCTION REGISTER TEST/		
036573	200	047520	042527	EM22:	.ASCIZ	<200>/POWER FAIL INITIALIZE FAILURE/		
036632	051200	043505	051511	DH1:	.ASCIZ	<200>/REGISTER	TRAPPED FROM/	
036673	200	054105	042520	DH2:	.ASCIZ	<200>/EXPECTED	FOUND	REGISTER/
036731	200	054105	042520	DH3:	.ASCIZ	<200>/EXPECTED	FOUND/	
036752	042600	050130	041505	DH4:	.ASCIZ	<200>/EXPECTED	FOUND	IBUS# REGISTER/
037014	042600	050130	041505	DH5:	.ASCIZ	<200>/EXPECTED	FOUND	IBUS REGISTER/
037055	200	054105	042520	DH6:	.ASCIZ	<200>/EXPECTED	FOUND	ADDRESS/
								.EVEN
037112	000002			DT1:	2			
037114	006	015			.BYTE	6,15		
037116	001264				\$REG1			
037120	006	002			.BYTE	6,2		
037122	001266				\$REG2			
037124	000003			DT2:	3			
037126	006	004			.BYTE	6,4		
037130	001274				\$REG3			
037132	006	004			.BYTE	6,4		
037134	001272				\$REG4			
037136	006	002			.BYTE	6,2		
037140	001254				\$REG1			
037142	000002			DT3:	2			
037144	006	004			.BYTE	6,4		
037146	001274				\$REG3			
037150	006	002			.BYTE	6,2		
037152	001272				\$REG4			
037154	000003			DT4:	3			
037156	003	007			.BYTE	3,7		
037160	001274				\$REG5			
037162	003	011			.BYTE	3,11		
037164	001272				\$REG4			
037166	002	002			.BYTE	2,2		
037170	001266				\$REG2			
037172	000003			DT5:	3			
037174	003	007			.BYTE	3,7		
037176	001274				\$REG5			
037200	003	007			.BYTE	3,7		
037202	001272				\$REG4			
037204	006	002			.BYTE	6,2		
037206	001266				\$REG2			
037210	000002			DT6:	2			
037212	003	007			.BYTE	3,7		
037214	001274				\$REG5			
037216	003	002			.BYTE	3,2		
037220	001272				\$REG4			
037222	000002			DT7:	2			
037224	006	004			.BYTE	6,4		
037226	001264				\$REG1			
037230	006	002			.BYTE	6,2		

H12

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037232 002066  
037234 000001

KMCSR  
CORMAX:  
.END







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DZKCC.P11 21-MAR-77 17:19 CROSS REFERENCE TABLE -- USER SYMBOLS

CORMAX	037234	4501	4533	6572#					
CR	= 000015	44#	1135	1145					
CREAM	001502	354#	707*	1841*	1842	1844*	1848		
CRLF	= 000200	45#	1106	1145					
CSR	010363	1740#	1945						
CSMAP	012112	1921#							
CYCLE	011460	916	977	1832#					
DATABP	006764	1571*	1574	1596	1599#				
DATAFL	= 104413	1535#							
DATAHD	006752	1570*	1592	1595#					
DDISP	= 177570	51#	207#	236					
DELAY	= 104411	1533#							
DEVTAB	003342	804	851#						
DH1	036632	386	6572#						
DH2	036673	389	6572#						
DH3	036731	392	401	413	422	437	440	446	6572#
DH4	036752	395	425	6572#					
DH5	037014	398	6572#						
DH6	037055	404	416	419	434	6572#			
DISPLA	001242	236#	726*	732*	1044*				
DISPRE	000174	197#	732						
DSMR	= 177570	50#	206#	235					
DT1	037112	387	6572#						
DT2	037124	390	6572#						
DT3	037142	393	414	441	447	6572#			
DT4	037154	396	426	6572#					
DT5	037172	399	405	417	420	435	6572#		
DT6	037210	402	423	6572#					
DT7	037222	438	6572#						
DZONE	= #####	382							U
DZONG	= #####	382							U
EHTVEC	= 000030	139#							
EM1	035746	385	6572#						
EM10	036243	409	6572#						
EM11	036307	412	433	6572#					
EM12	036321	415	6572#						
EM13	036347	418	6572#						
EM14	03635E	421	6572#						
EM15	036367	424	6572#						
EM16	036413	427	6572#						
EM17	036443	430	6572#						
EM2	036013	388	6572#						
EM20	036471	436	442	6572#					
EM21	036524	439	6572#						
EM22	036573	445	6572#						
EM3	036054	391	6572#						
EM4	036102	394	397	6572#					
EM5	036143	400	6572#						
EM6	036165	403	6572#						
EM7	036207	406	6572#						
ERCT00	002304	591#							
ERCT01	002310	594#							
ERCT02	002314	597#							
ERCT03	002320	600#							
ERCT04	002324	603#							
ERCT05	002330	606#							







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CROSS REFERENCE TABLE -- USER SYMBOLS

NOACT	010731	751	1740*	1834																		
MODEV	003240	802	824*																			
MARSET	035540	4239	4273	4311	4347	4388	4424	4461	4508	6492*												
NUM	010323	1740*	1933																			
OK	003220	816	819*	842																		
ONE	001464																					
PACT00	002302	590*																				
PACT01	002306	593*																				
PACT02	002312	596*																				
PACT03	002316	599*																				
PACT04	002322	602*																				
PACT05	002326	605*																				
PACT06	002332	608*																				
PACT07	002336	611*																				
PACT10	002342	614*																				
PACT11	002346	617*																				
PACT12	002352	620*																				
PACT13	002356	623*																				
PACT14	002362	626*																				
PACT15	002366	629*																				
PACT16	002372	632*																				
PACT17	002376	635*																				
PARBIT=	040000	159*																				
PERFOR=	004537	159*																				
PFTAB	007324	1659	1681*																			
PIRQ =	177772	49*																				
PIRQVE=	000240	143*																				
POFRD =	012600	154*	1614																			
POP1SP=	005726	152*																				
POP2SP=	022626	156*	6300																			
PRI0	010422	1740*	1961																			
PRIORITY	013730	2182*	2188*	2201	2222*																	
PR0 =	000000	66*	2158	2159																		
PR1 =	000040	67*																				
PR2 =	000100	68*																				
PR3 =	000140	69*																				
PR4 =	000200	70*	2160																			
PR5 =	000240	71*	2161																			
PR6 =	000300	72*	2162																			
PR7 =	000340	73*	178	180	182	184	2163															
PS =	177776	46*	47	700*	909*	2127*	2137*	4095*	4099*	4125*	4129*	4153*	4167*	4193*								
		4209*																				
PSM =	177776	47*																				
PUSHRO=	010046	153*	1611																			
PUSHIS=	005746	151*																				
PUSH2S=	024646	155*																				
PARVEC=	000024	138*	1637*	1638*	1647*	1653*	1672*	1673*														
QV.FLG	001511	362*	706*	956*																		
ROCHR =	104402	1253	1526*																			
ROLIN =	104403	1326	1527*																			
ROOCT =	104404	1375	1528*																			
RESREG	006766	1597	1600*																			
RESVEC=	000010	133*																				
RES05 =	104407	1531*	1600																			
ROMCLK=	104412	1534*	1687	1690	1727	1732	3094	3096	3114	3116	3151	3153	3171	3173								
		3207	3209	3225	3227	3260	3262	3278	3280	3314	3316	3334	3336	3371	3371							





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TST121	032500	5772	5821#
TST122	032656	5823	5872#
TST123	033034	5874	5923#
TST124	033212	5925	5974#
TST125	033370	5976	6025#
TST126	033546	6027	6076#
TST127	033724	6078	6127#
TST13	015104	2521	2551#
TST130	034102	6129	6178#
TST131	034260	6180	6228#
TST132	034466	6230	6279#
TST133	034660	6281	6329#
TST134	##### U	6331	6572
TST14	015202	2553	2583#
TST15	015300	2585	2615#
TST16	015376	2617	2647#
TST17	015474	2649	2679#
TST2	014042	2235	2263#
TST20	015572	2681	2711#
TST21	015670	2713	2743#
TST22	015766	2745	2775#
TST23	016064	2777	2807#
TST24	016162	2809	2839#
TST25	016306	2841	2883#
TST26	016432	2885	2927#
TST27	016562	2929	2970#
TST3	014072	2265	2284#
TST30	016722	2972	3012#
TST31	017064	3014	3056#
TST32	017150	3058	3083#
TST33	017350	3085	3140#
TST34	017550	3142	3197#
TST35	017724	3199	3250#
TST36	020100	3252	3303#
TST37	020300	3305	3360#
TST4	014222	2286	2327#
TST40	020510	3362	3419#
TST41	020664	3421	3472#
TST42	021040	3474	3525#
TST43	021214	3527	3578#
TST44	021370	3580	3631#
TST45	021544	3633	3684#
TST46	021720	3686	3737#
TST47	022074	3739	3790#
TST5	014320	2329	2359#
TST50	022250	3792	3843#
TST51	022476	3845	3906#
TST52	022646	3908	3958#
TST53	023114	3960	4025#
TST54	023336	4027	4085#
TST55	023432	4087	4116#
TST56	023524	4118	4147#
TST57	023646	4149	4187#
TST6	014416	2361	2391#
TST60	024014	4189	4232#
TST61	024122	4234	4267#







CROSS REFERENCE TABLE -- USER SYMBOLS

SERFLG	001203	218#	705*	937*	999	1028	1030*	1051	1558*	1572	1586*	1660*		
SERMAX	001215	224#	1051											
SERPAR	006512	181	1547#											
SERAPC	001216	225#	714*	958*	1007*	1555	1557*	1661*						
SERATB	001512	379#	1568											
SERTTL	001212	222#	949	989	1615*	1857*								
SETABL	001336	276#												
SETEND	001442	329#	470											
SFATAL	001380	269#	1185*											
SFFLG	005142	1148#	1151*	1179	1188*	1196#								
SFILLC	001256	243#	1114	1145										
SFILLS	001255	242#	1145											
SGADR	001220	226#												
SJDDAT	001224	228#												
SGET42	004060	968#												
SCTSAR=	##### U	1525												
SHD =	000000	11												
SHIBTS	002034	465#												
SHIOCT	005722	1348#	1359#											
SHCNT	001204	219#	1036*	1037	1039*	1050								
SILLUP	007316	1637	1653	1677#										
SINPUT	005724	1364#	1537											
SINTAG	001235	233#												
SITEMB	001214	223#	1563*	1603										
SLF	001314	261#	1145	1290	1300	1360								
SLFLG	005141	1189#	1195#											
SLPADR	001206	220#	716*	916*	920	1043*	1045	1050	1620*	1622	1896*	1906*	1908	
SLPERR	001210	221#												
SPADR1	001350	294#												
SPADR2	001354	298#												
SPADR3	001360	301#												
SPADR4	001364	304#												
SPAIL	001316	267#	466	470	1042	1089								
SPANS1	001346	288#	2185											
SPANS2	001352	295#												
SPANS3	001356	299#												
SPANS4	001362	302#												
SPBADR	002036	466#												
SPFLG	005140	1149#	1155	1190*	1194#									
SPHEX	005552	1304#	1782											
SPSGAD	001332	274#	1165*	1168										
SPSGLC	001334	275#	1170*											
SPSCTY	001316	268#	1163	1171*	1183	1187*								
SPSMR	005541	1302#	1779											
SPYYP1	001347	289#												
SPYYP2	001353	297#												
SPYYP3	001357	300#												
SPYYP4	001363	303#												
SPXCNT	004362	1040	1050#											
SN =	000133	1#	2223	2228	2230	2238#	2254	2258	2260	2267#	2273	2279	2281	2289
		2290#	2316	2322	2324	2331	2332#	2348	2354	2356	2363	2364#	2380	2386
		2388	2395	2396#	2412	2418	2420	2427	2428#	2444	2450	2452	2459	2460#
		2476	2482	2484	2491	2492#	2508	2514	2515	2523	2524#	2540	2546	2548
		2555	2556#	2572	2578	2580	2587	2598#	2604	2610	2612	2619	2620	2636
		2642	2644	2651	2652#	2668	2674	2676	2683	2684#	2700	2706	2708	2715
		2716#	2732	2738	2740	2747	2748#	2764	2770	2772	2779	2780#	2796	2802

CROSS REFERENCE TABLE -- USER SYMBOLS

2804	2811	2812	2828	2834	2836	2843	2844	2872	2878	2880	2887	2888
2916	2922	2924	2932	2933	2939	2943	2967	2975	2976	3001	3007	3009
3017	3018	3043	3051	3053	3060	3065	3072	3078	3080	3088	3089	3123
3135	3137	3145	3146	3188	3189	3194	3202	3203	3239	3245	3247	3255
3256	3292	3298	3300	3308	3309	3349	3355	3357	3365	3366	3408	3414
3416	3424	3425	3461	3467	3469	3477	3478	3514	3520	3522	3530	3531
3567	3573	3575	3583	3734	3620	3626	3628	3636	3637	3673	3679	3681
3689	3690	3726	3732	3734	3742	3743	3779	3785	3787	3795	3796	3836
3838	3840	3848	3849	3849	3901	3903	3911	3912	3947	3953	3955	3963
3964	4014	4020	4022	4030	4031	4075	4080	4082	4089	4091	4106	4111
4113	4120	4121	4136	4142	4144	4151	4152	4176	4182	4184	4191	4192
4222	4227	4229	4236	4238	4257	4262	4264	4271	4272	4295	4300	4302
4309	4310	4323	4326	4347	4344	4345	4370	4376	4378	4385	4386	4408
4414	4416	4423	4424	4425	4451	4453	4460	4461	4482	4488	4490	4498
4499	4544	4549	4551	4559	4560	4584	4582	4594	4602	4603	4635	4643
4645	4653	4654	4686	4694	4696	4704	4705	4737	4745	4747	4755	4756
4788	4796	4798	4806	4807	4839	4847	4849	4857	4858	4890	4898	4900
4908	4909	4941	4949	4950	4951	4959	4960	4992	5000	5001	5002	5010
5011	5043	5051	5052	5053	5061	5062	5094	5102	5103	5104	5112	5113
5145	5153	5154	5155	5163	5164	5188	5204	5205	5206	5214	5215	5247
5255	5256	5257	5265	5286	5295	5306	5307	5308	5316	5317	5349	5357
5358	5359	5367	5368	5400	5418	5409	5410	5418	5419	5451	5459	5460
5461	5469	5470	5503	5510	5511	5512	5520	5521	5553	5561	5562	5563
5571	5572	5604	5612	5613	5614	5622	5623	5655	5663	5664	5666	5673
5674	5706	5714	5715	5716	5724	5725	5757	5765	5766	5767	5775	5776
5808	5816	5817	5818	5826	5827	5859	5867	5868	5869	5877	5878	5910
5918	5919	5920	5928	5929	5961	5969	5970	5971	5979	5980	6012	6020
6021	6022	6030	6031	6063	6071	6072	6073	6081	6082	6114	6122	6123
6124	6132	6133	6165	6173	6174	6175	6183	6184	6216	6223	6224	6225
6232	6233	6267	6274	6275	6276	6283	6284	6315	6324	6325	6326	6333
6334	6572											
241	1116	1145										
2232	2262	2283	2326	2358	2390	2422	2454	2486	2518	2550	2582	2614
2646	2678	2710	2742	2774	2806	2838	2870	2902	2934	3011	3055	3082
3139	3196	3249	3302	3359	3418	3471	3524	3577	3630	3683	3736	3789
3842	3905	3957	4024	4084	4115	4146	4186	4231	4286	4304	4339	4380
4418	4455	4492	4553	4596	4647	4698	4749	4800	4851	4902	4953	5004
5055	5106	5157	5208	5259	5310	5361	5412	5463	5514	5565	5616	5667
5718	5769	5820	5871	5922	5973	6024	6075	6126	6177	6227	6278	6328
SOVER	004334											
SPASS	001324											
SPASTH	002042											
SPARDN	007126											
SPARNG	007312											
SPARLP	007200											
SOLES	001312											
SROCHR	005144											
SRODEC	#####											
SROLIN	005264											
SRODOCT	005564											
SROSZ	= 000007											
SREGAD	001260											
SREGO	001262											
SREG1	001264											
SREG2	001266											
SREG3	001270											

SMULL 001254  
SMWTST= 000000

SOVER 004334  
SPASS 001324  
SPASTH 002042  
SPARDN 007126  
SPARNG 007312  
SPARLP 007200  
SOLES 001312  
SROCHR 005144  
SRODEC= ##### U  
SROLIN 005264  
SRODOCT 005564  
SROSZ = 000007  
SREGAD 001260  
SREGO 001262  
SREG1 001264  
SREG2 001266  
SREG3 001270





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CROSS REFERENCE TABLE -- USER SYMBOLS

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.SAVDS	006072	1407#	1530		
.SCOP1	004364	1055#	1529		
.START	002402	201	700#	716	1799
.TIMER	007512	1536	1723#		
.\$ASTA=	***** U	1149	1152		
.\$X =	002034	454#	459		





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DZKCC.P11 21-MAR-77 17:19 CROSS REFERENCE TABLE -- MACRO NAMES

TYPNUM	1448														
TYPOCS	1448														
TYPOCT	1448														
TYPTXT	1448														
SAD01	18	2223													
SAD02	18	2254													
SAD03	18	2273	2916												
SAD04	18	2316	2348	2380	2412	2444	2476	2508	2540	2572	2604	2636	2668	2700	2732
	2764	2796													
SALU	18	4584	4635	4686	4737	4788	4839	4890	4941	4992	5043	5094	5145	5196	5247
	5298	5349	5400	5451	5502	5553	5604	5655	5706	5757	5808	5859	5910	5961	6012
	6063	6114	6165												
SALUD	18	4544													
SALTO	18	785													
SBR	18	3912	3929												
SBUFFE	18	1752													
SCOMP	18	6238	6251												
SCYCLE	18	1823													
SEOP	18	921													
SERTBL	18	381													
SFINI	18	6572													
SFLOAT	18	3090	3109	3147	3166	3204	3221	3257	3274	3310	3329	3367	3387	3426	3443
	3479	3496	3532	3549	3585	3602	3638	3655	3691	3708	3744	3761	3797	3814	
SGETPA	18														
SHEADE	18	11													
SINTR	18	4075	4106												
SIR	18	2959	3001												
SMARHI	18	6401	6458												
SMENFL	18														
SMEND	18														
SMEN1	18														
SMEN2	18														
SMEN3	18														
SMOCK	18														
SMSC	18	1740													
SNOISE	18	6315													
SNPABI	18	4482													
SNPR1	18	4222	4257	4295											
SNPR2	18	4329	4370												
SNPR3	18	4408	4445												
SPASEN	18	935													
SPFAIL	18	1630													
SPOMER	18	6267													
SPRIO	18	4136	4176												
SPROC1	18	3043													
SPROC2	18	3072	3129	3186	3239	3292	3349	3408	3461	3514	3567	3620	3673	3726	3779
SPROC3	18	3832													
SPROC4	18	3895													
SPROCS	18														
SQUEST	18	1932	1944	1952	2009	2017									
SRANCL	18	1684													
SRCLK	18	1687	1690	1727	1732	3094	3096	3114	3116	3151	3153	3171	3173	3207	3209
	3225	3227	3260	3262	3278	3280	3314	3316	3334	3336	3371	3373	3392	3394	3429
	3431	3447	3449	3482	3484	3500	3502	3535	3537	3553	3555	3588	3590	3606	3608
	3641	3643	3659	3661	3694	3696	3712	3714	3747	3749	3765	3767	3800	3802	3818
	3820	3855	3863	3881	3915	3917	3933	3935	3969	3973	3975	3992	3996	3998	4037

CROSS REFERENCE TABLE -- MACRO NAMES

	4041	4043	4061	4063	4097	4127	4165	4207	4246	4280	4284	4286	4318	4353	4361
	4363	4399	4401	4430	4433	4436	4467	4470	4473	4515	4565	4567	4569	4571	4512
	4616	4618	4663	4667	4669	4714	4718	4720	4765	4769	4771	4816	4820	4822	4867
	4871	4873	4918	4923	4924	4969	4973	4975	5020	5024	5026	5071	5075	5077	5122
	5126	5128	5173	5177	5179	5224	5228	5230	5275	5279	5281	5326	5330	5332	5377
	5381	5383	5428	5432	5434	5479	5483	5485	5530	5534	5536	5581	5585	5587	5632
	5636	5638	5683	5687	5689	5734	5738	5740	5785	5789	5791	5836	5840	5812	5887
	5891	5893	5938	5942	5944	5989	5993	5995	6040	6044	6046	6091	6095	6097	6142
	6146	6148	6193	6197	6199	6236	6257	6338	6351	6354	6357	6370	6373	6376	6382
	6385	6388	6391	6399	6401	6413	6431	6443	6446	6456	6458	6461	6501	6517	6520
	6537	6548	6550	6558	6560										
SSOVAR	1#	331													
SSCAD0	1#	1007													
SSCAD1	1#	1046													
SSIMBC	1#														
SSOFTC	1#	1760													
SSPF	1#	3965	3987												
SSP1	1#	3947													
SSP2	1#	4014													
STIMER	1#	6216													
STSTN	1#	2230	2260	2281	2324	2356	2388	2420	2452	2484	2516	2548	2580	2612	2644
	2676	2708	2740	2772	2804	2836	2880	2924	2967	3009	3053	3080	3137	3194	3247
	3300	3357	3416	3469	3522	3575	3628	3681	3734	3787	3840	3903	3955	4022	4082
	4113	4144	4184	4229	4284	4302	4337	4378	4416	4453	4490	4551	4594	4645	4696
	4747	4798	4849	4900	4951	5002	5053	5104	5155	5206	5257	5308	5359	5410	5461
	5512	5563	5614	5665	5716	5767	5818	5869	5920	5971	6022	6073	6124	6175	6225
	6276	6326													
SLPAD0	1#	1658													
SVARIA	1#	203													
SWRFLT	1#	2845	2858	2889	2902										
SWR46	1#	2828	2872												
WXZ	1#	2223	2228	2254	2258	2273	2279	2316	2322	2348	2354	2380	2386	2412	2418
	2444	2450	2476	2482	2508	2514	2540	2546	2572	2578	2604	2610	2636	2642	2668
	2674	2700	2706	2732	2738	2764	2770	2796	2802	2828	2834	2872	2878	2916	2922
	2959	2965	3001	3007	3043	3051	3072	3078	3129	3135	3186	3192	3239	3245	3292
	3298	3349	3355	3408	3414	3461	3467	3514	3520	3567	3573	3620	3626	3673	3679
	3726	3732	3779	3785	3832	3838	3895	3901	3947	3953	4014	4020	4075	4080	4106
	4111	4136	4142	4176	4182	4222	4227	4257	4262	4296	4300	4329	4335	4370	4376
	4408	4414	4445	4451	4482	4488	4544	4549	4584	4592	4635	4643	4686	4694	4737
	4745	4788	4796	4839	4847	4890	4898	4941	4949	4992	5000	5043	5051	5094	5102
	5145	5153	5196	5204	5247	5255	5298	5306	5349	5357	5400	5408	5451	5453	5502
	5510	5553	5561	5604	5612	5655	5663	5706	5714	5757	5765	5808	5816	5859	5867
	5910	5918	5961	5969	6012	6020	6063	6071	6114	6122	6165	6173	6216	6223	6267
	6274	6315	6324												
SSCHRE	208#	247	248	249	250	251	252								
SSCHTM	208#	253	254	255	256	257									
SSESCA	144#														
SSNEWT	144#	2232	2262	2283	2326	2358	2390	2422	2454	2486	2518	2550	2582	2614	2646
	2678	2710	2742	2774	2806	2838	2882	2926	2969	3011	3055	3082	3139	3196	3249
	3302	3359	3418	3471	3524	3577	3630	3683	3736	3789	3842	3905	3957	4024	4084
	4115	4146	4186	4231	4266	4304	4339	4380	4418	4455	4492	4553	4596	4647	4698
	4749	4800	4851	4902	4953	5004	5055	5106	5157	5208	5259	5310	5361	5412	5463
	5514	5565	5616	5667	5718	5769	5820	5871	5922	5973	6024	6075	6126	6177	6227
	6278	6328													
SSSCOP	1#	990													
SSSET	1515#	1526	1527	1528	1529	1530	1531	1532	1533	1534	1535	1536	1537	1538	1539

DZKCC MACY11 27(1006) 12-MAY-77 18:34 PAGE 147  
DZKCC.P11 21-MAR-77 17:19 CROSS REFERENCE TABLE -- MACRO NAMES

SSKIP	1540	
.EQUAT	1448	
.HEADE	18	34
.SETUP	18	
.SACT1	18	185
.SAPT8	18	2638
.SAPTH	18	449
.SAPTY	18	1145
.SCATC	18	
.SCMTR	18	208
.SEOP	18	927
.SERRO	18	
.SERRT	18	
.SPOWE	18	1633
.SRDOC	18	1307
.SREAO	18	1204
.SSCOP	18	994
.STRAP	18	1492
.STYPE	18	1066
.STYPO	18	

. ARS. 037234 000

ERRORS DETECTED: 0  
DEFAULT GLOBALS GENERATED: 0

DZKCC,DZKCC/SOL/CRF+DZKCC.MAC,DZKCC.P11  
RUN-TIME: 34 32 2 SECONDS  
RUN-TIME RATIO: 116/69=1.6  
CORE USED: 49K (98 PAGES)