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2.0 OPERATING INSTRUCTIONS

2.1 LOADING AND STARTING PROCEDURES

2.1.1 LOADING

USE NORMAL PROCEDURES FOR LOADING ABSOLUTE BINARY TAPES.

2.1.2 NORMAL START

THIS IS THE PROCEDURE FOR NORMAL PROGRAM RUNNING (I.E., STARTING WITH TEST 1 AND EXECUTING ENTIRE DIAGNOSTIC).

LOAD ADDRESS = 200
START

2.1.3 SUBTEST START

THIS IS THE PROCEDURE FOR STARTING AT A SUBTEST OTHER THAN 1.

1. LOAD \$TESTN (IN MAILBOX SECTION) WITH THE NUMBER OF SUBTEST MINUS ONE (IN OCTAL) FOR EXAMPLE, TO START AT SUBTEST 100, \$TESTN=77.
2. LOAD STARTING ADDRESS OF SUBTEST IN LOC. 216
3. LOAD ADDRESS = ADDRESS OF SUBTEST
START

2.2 SPECIAL ENVIRONMENTS

THIS PROGRAM IS WRITTEN TO COMPLY WITH ALL THE REQUIREMENTS OF THE APT INTERFACE SPECIFICATION. IT WILL RUN UNDER APT IN EITHER QUICK VERIFY, PROGRAM OR RUN-TIME MODES.

THIS PROGRAM IS WRITTEN TO COMPLY WITH ALL OF THE REQUIREMENTS OF PROGRAMS TO RUN UNDER THE ACT11 MONITOR.

2.3 PROGRAM OPTIONS

THIS PROGRAM IS INTENDED TO BE A BASIC PROCESSOR TEST. IT IS INTENDED TO BE THE LOWEST LEVEL DIAGNOSTIC RUN. IT PROVIDES FOR NO SELECTABLE OPTIONS.

IN ORDER THAT THE TEST BE RUNNABLE ON A PROCESSOR WITHOUT A TELETYPE, IT IS POSSIBLE TO SUPPRESS THE END OF PASS MESSAGE. IF NO TELETYPE IS AVAILABLE, ALTER THE BYTE, SENVM, WHICH IS LOCATED IN THE APT MAILBOX. SETTING SENVM TO 40(8) WILL

SUPPRESS ALL CONSOLE OUTPUT.
THE EXACT LOCATION OF THIS BYTE CAN BE FOUND IN THE SYMBOL
TABLE AT THE END OF THE LISTING.

2.4 EXECUTION TIMES

THE DIAGNOSTIC COMPLETES ONE PASS IN LESS THAN 1 SEC.
THE PROGRAM WILL RUN CONTINUOUSLY UNTIL EXTERNALLY HALTED.

3.0 ERROR INFORMATION

3.1 ERROR TYPES

THERE ARE TWO BASIC TYPES OF ERRORS IN THE DIAGNOSTIC.

3.1.1 FUNCTIONAL ERRORS

THESE ARE ERRORS WHICH REPRESENT A MALFUNCTION OF AN
INSTRUCTION OR SEQUENCE OF INSTRUCTION. (E.G. THE PROPER
CONDITION CODE NOT SET OR IMPROPER RESULT OF AN ARITHMETIC
OR LOGICAL OPERATION).

3.1.2 SEQUENCE ERRORS

THE RESULT OF A TESTS BEING EXECUTED OUT OF SEQUENCE. (E.G.
WILD MACHINE OR IMPROPER BRANCH OR JUMP).

3.2 ERROR REPORTING PROCEDURES

THE DIAGNOSTIC RESPONDS TO THE DETECTION OF ALL ERRORS BY
STORING CERTAIN INFORMATION IN MEMORY AND HALTING THE PROCESSOR.
THE INFORMATION STORED IN MEMORY CAN BE USED BY THE OPERATOR
TO IDENTIFY THE ERROR DETECTED.

CERTAIN FAILURES WILL CAUSE THE PROESSOR TO HANG.
THIS TYPE OF FAILURE IS INDICATED IF THE PROGRAM
DOES NOT PRINT ITS END OF PASS INDICATION WITHIN A REASONABLE
AMOUNT OF TIME. (FIRST MESSAGE SHOULD APPEAR WITHIN 1 SEC.)

3.3 ERROR DESCRIPTOR INFORMATION

THE DIAGNOSTIC MAILBOX HOLDS THE ERROR INFORMATION NECESSARY
TO IDENTIFY THE DETECTED ERROR. THIS INFORMATION HAS BEEN
DESIGNED FOR COMPLIANCE WITH THE APT TO DIAGNOSTIC INTERFACE
SPECIFICATION. IT IS THE PRIMARY MEDIUM FOR IDENTIFYING ERRORS.

3.2.1 SMSGTYP

ALWAYS CONTAIN THE NUMBER OF SUCCESSFUL PASSES COMPLETED.
\$PASS IS RESET WITH EVERY RETART FROM LOC. 200.

ADDITIONALLY, THE MESSAGE END OF DGKAA IS PRINTED ON THE CONSOLE
TELETYPE AFTER THE FIRST PASS AND FOLLOWING EVERY 400TH PASS
THEREAFTER.

IF NO TELETYPE IS AVAILABLE, THE CONSOLE OUTPUT MUST BE SUPPRESSED.
(SEE SECTION 2.3)

5.0 TROUBLE SHOOTING

WHEN THE PROGRAM DISCOVERS A FAULT IT WILL HALT. TO DETERMINE
THE CAUSE OF THE HALT, THE DIAGNOSTIC PROVIDES ERROR INFORMATION.
THIS INFORMATION IS STORED IN THE APT MAILBOX AND IS THE PRIMARY
SOURCE OF ERROR IDENTIFICATION.

UPON FINDING AN ERROR, THE FOLLOWING PROCEDURE SHOULD AID IN ISOLATING
THE FAULT.

5.1 CHECK THE MAILBOX

1. \$MSGTY THIS LOCATION SHOULD CONTAIN A 1. IF THE PROCESSOR
HALTS AND THIS LOCATION IS ZERO, THEN THE PROCESSOR HAS COME
TO AN UNEXPECTED HALT. FIRST SUSPECT A TRAP. CHECK THE
PC AND IF A TRAP CHECK R6 AND THE STACK FOR THE LOCATION OF
THE FAILING INSTRUCTION.
2. \$FATAL THIS LOCATION IS USED TO HOLD THE NUMBER OF THE ERROR WHICH HAS
DETECTED. EACH ERROR BEING CHECKED BY THE DIAGNOSTIC IS ASSIGNED
A UNIQUE NUMBER WHICH IS STORED IN \$FATAL WHEN THAT ERROR IS DETECTED.

WHEN AN ERROR IS DETECTED, CHECK THE LISTING TO SEE THAT THE ERROR
NUMBER STORED IN \$FATAL IS ONE WHICH IS DETECTED IN THE
TEST WHOSE NUMBER IS IN \$TESTN. IF THERE IS A DISAGREEMENT THEN
THE ERROR BEING REPORTED IS A SEQUENCE ERROR. \$TESTN CONTAINS
ONE MORE THAN THE LAST TEST WHICH WAS SUCCESSFULLY COMPLETED.

3. \$TESTN THIS LOCATION IS USED TO INDICATE THE NUMBER OF THE
TEST WHICH WAS BEING EXECUTED WHEN THE FAULT WAS DETECTED.
\$TESTN IS USED IN CONJUNCTION WITH \$FATAL TO DISTINGUISH
BETWEEN SEQUENCE AND FUNCTIONAL ERRORS. (SEE 2. THIS SECTION)
4. \$PASS THIS LOCATION IS USED TO INDICATE THE NUMBER OF SUCCESSFUL
PASSES WHICH THE DIAGNOSTIC HAS COMPLETED. THIS WILL GIVE AN
INDICATION THAT THE DIAGNOSTIC HAS NOT JUST BEEN HUNG IN A LOOP
IF NOT TELETYPE IS AVAILABLE TO REPORT THE PRINTED PROGRESS
REPORTS.

IF AN ERROR HAS BEEN DETECTED \$PASS WILL SHOW WHETHER IT
WAS A HARD ERROR DISCOVERED DURING THE FIRST TRY OR WHETHER
IT WAS INTERMITTANT OR DEVELOPED DURING THE RUNNING OF THE
DIAGNOSTIC.

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409
410
411
412
413
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000500

000240
000007
000006
177776
177564
177566

00040C

5.2 SCOPING

WHILE THIS DIAGNOSTIC IS PRIMARILY INTENDED TO BE A FAULT DETECTION PROGRAM, PROVISIONS ARE MADE TO ASSIST A TECHNICIAN WHO MIGHT WANT TO USE THE PROGRAM AS A TROUBLE SHOOTING TEST.

THE PROCEDURE FOR SCOPING A SUBTEST INVOLVES MODIFYING SEVERAL MEMORY LOCATIONS IN THE TEST ITSELF. THE PHILOSOPHY IS TO PROVIDE A SCOPING LOOP WHICH WILL INCLUDE THE CODE WHERE THE ERROR WAS DETECTED. THE LOOP IS SET UP SO THAT THE LOOP WILL NOT BE TERMINATED SHOULD THE ERROR INTERMITTANTLY DISAPPEAR.

THE PROCEDURE IS AS FOLLOWS:

1. DETERMINE WHICH ERROR IS TO BE SCOPED. USE \$FATAL AND \$TESTN FOR THIS (SEE ABOVE)
2. LOCATE THE ERROR ROUTINE IN THE LISTING.
3. CLEAR THE RIGHT BYTE OF THE CONDITIONAL BRANCH INSTRUCTION ASSOCIATED WITH THE ERROR. (THIS IS MARKED WITH <===='S IN THE LISTING.)
4. REPLACE THE INSTRUCTION FOLLOWING <MOV #XXX, -(R2)> WITH THE SCOPING BRANCH PROVIDED IN THE LISTING COMMENTS.
5. RESTART THE PROGRAM. THE PROGRAM MAY BE RESTARTED FROM THE BEGINNING OR FROM THE SUBTEST (SEE 2.0).

6.0 LISTING

```

%
.TITLE MAINDEC-11-DGKAA 11/04 CPU TEST
.ENABLE ABS
STBOT=500
.NLIST CND,MC,MD
.LIST ME
SCOPE=NOP
R7=%7
R6=%6
PS=177776
TPS=177564
TPB=177566
.MCALL .SAPTHDR .SAPTBLs .SACT11
.SBTTL ACT11 HOOKS
;*****
;HOOKS REQUIRED BY ACT11
$SVPC= ;SAVE PC

```

415 000046 000046
 416 000046 015264
 417 000052 000052
 418 000052 000000
 419 000400 000400
 420 000300 000300
 421
 422
 423
 424
 425 000300 000000
 426 000300 000000
 427 000302 000000
 428 000304 000000
 429 000306 000000
 430 000310 000000
 431 000312 000000
 432 000314 000000
 433 000316 000000
 434 000320 000
 435 000320 000
 436 000321 000
 437 000322 000000
 438 000324 000000
 439 000326 000000
 440
 441
 442
 443
 444
 445
 446 000330
 447
 448
 449
 450
 451
 452
 453 000330 000330
 454 000024 000024
 455 000200 000200
 456 000044 000044
 457 000044 000330
 458 000330 000330
 459
 460
 461
 462
 463 000330
 464 000330 000000
 465 000332 000300
 466 000334 000002
 467 000336 000002
 468 000340 000000
 469 000342 000014
 470 000370 000370

.=46
 \$ENDAD ;; 1)SET LOC.46 TO ADDRESS OF \$ENDAD IN BE F
 .=52
 .WORD 0 ;; 2)SET LOC.52 TO ZERO
 .=\$\$VPC ;; RESTORE PC
 .=300

.SBTTL APT MAILBOX-ETABLE

.EVEN
 \$MAIL: ;; APT MAILBOX
 \$MSGTY: .WORD AMSGTY ;; MESSAGE TYPE CODE
 \$FATAL: .WORD AFATAL ;; FATAL ERROR NUMBER
 \$TESTN: .WORD ATESTN ;; TEST NUMBER
 \$PASS: .WORD APASS ;; PASS COUNT
 \$DEVCT: .WORD ADEVCT ;; DEVICE COUNT
 \$UNIT: .WORD AUNIT ;; I/O UNIT NUMBER
 \$MSGAD: .WORD AMSGAD ;; MESSAGE ADDRESS
 \$MSGLG: .WORD AMSGLG ;; MESSAGE LENGTH
 \$ETABLE: ;; APT ENVIRONMENT TABLE
 \$ENV: .BYTE AENV ;; ENVIRONMENT BYTE
 \$ENVM: .BYTE AENVM ;; ENVIRONMENT MODE BITS
 \$\$WREG: .WORD ASWREG ;; APT SWITCH REGISTER
 \$USWR: .WORD AUSWR ;; USER SWITCHES
 \$CPUOP: .WORD ACPUOP ;; CPU TYPE, OPTIONS
 *
 * BIT 15-11=CPU TYPE
 * 11/04=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05
 * 11/70=06, PDQ=07, Q=10
 * BIT 10=REAL TIME CLOCK
 * BIT 9=FLOATING POINT PROCESSOR
 * BIT 8=MEMORY MANAGEMENT

\$ETEND:
 .MEXIT
 .SBTTL APT PARAMETER BLOCK

;;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT

.\$X= ;; SAVE CURRENT LOCATION
 =24 ;; SET POWER FAIL TO POINT TO START OF PROGRAM
 200 FOR APT START UP
 =44 ;; POINT TO APT INDIRECT ADDRESS PNTR.
 \$APTHDR ;; POINT TO APT HEADER BLOCK
 =.\$X ;; RESET LOCATION COUNTER

;;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
 ;;INTERFACE SPEC.

\$APTHD:
 \$HIBTS: .WORD 0 ;; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
 \$MBADR: .WORD \$MAIL ;; ADDRESS OF APT MAILBOX (BITS 0-15)
 \$STMT: .WORD 2 ;; RUN TIM OF LONGEST TEST
 \$PASTM: .WORD 2 ;; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
 \$SUNIYM: .WORD 0 ;; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
 .WORD \$ETEND-\$MAIL/2 ;; LENGTH MAILBOX-ETABLE(WORDS)
 .=370

```

471 003370 000000 000000 000000
472 000376 000000 000000 000000
473 000404 000001 000001 177777
474      00050C
475
476
477      000500
478      000200
479 000200 000167 000274
480
481 000204 012706 000500
482 000210 012702 000304
483 000214 000137
484 000216 000000
485
486      000500
487      000302
488      000304
489 000500 012737 015426 000024
490 000506 012737 000000 000306
491 000514 012737 177777 015310
492 000522 012706 000500
493 000526 012702 000304
494 000532 012737 000000 000304
495 000540 012737 000000 000302
496 000546 012737 000000 000300

```

```

          0.0.0.0.0.0
          1,1,-1
          .=500
:*****
:SET UP STARTING ADDRESS
          .SX=
          .=200
          JMP      START
          MOV      #STBOT,R6      ;SET STACK POINTER
          MOV      #STESTN,R2    ;SET MAILBOX POINTER
          JMP      @PC)+         ;JUMP TO SUBTEST
          0                      ;ADDR. OF SUBTEST GOES HERE

          .=.SX
          $ERROR=$FATAL
          $STSTNM=$TESTN
START:   MOV      #PWRDN,@#24    ;SET UP FOR POWER FAIL
          MOV      #0,@#$PASS    ;CLEAR PASS COUNT
          MOV      #-1,@#PASSPT ;SET PRINT COUNTER
RESTRT:  MOV      #STBOT,R6     ;INITIALIZE STACK POINTER
          MOV      #STESTN,R2   ;SET UP POINTER TO MESSAGE TYPE
          MOV      #0,@#$STSTNM ;CLEAR TEST NUMBER
          MOV      #0,@#$ERROR  ;CLEAR ERROR NUMBER
          MOV      #0,@#$MSGTY  ;CLEAR MESSAGE TYPE(FOR APT)

```

```

-97
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439
500 000554 005212
501 000556 022712 000001
502 000562 001024
503 000564 000257
504 000566 001401
505 000570 000404
506
507
508
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510 000572
511 000572 012742 000001
512 000576 005242
513 000600 000000
514 000602
515 000602 001004
516
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520 000604 012742 000002
521 000610 005242
522 000612 000000
523 000614 000264
524 000616 001001
525 000620 000404
526
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530 000622
531 000622 012742 000003
532 000626 005242
533 000630 000000
534 000632
535 000632 001404
536
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540 000634 012742 000004
541 000640 005242
542 000642 000000
543

```

```

;*****
;TEST 1 CHECK BRANCHES ON Z BIT
;*****
TST1: INC (R2) ;UPDATE TEST NUMBER
      CMP #1,(R2) ;SEQUENCE ERROR?
      BNE TST2-10 ;BR TO ERROR HALT ON SEQ ERROR
      CCC ;CLEAR ALL CONDITION CODES
      BEQ BR1 ;SHOULD BRANCH
      BR BR2 ;BAD BRANCH OF Z-BIT
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; BRANCH INSTRUCTION AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; FOLLOWING W/ 774 <====
      ;
BR1: MOV #1,-(R2) ;MOVE TO MAILBOX # ***** 1 *****
     INC -(R2) ;SET MSGTYP TO FATAL ERROR
     HALT ;SHOULD HAVE BRANCHED: Z=0
BR2: BNE BR3
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; CONDITIONAL BRANCH INST. AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; WHICH FOLLOWS W/ 770 <====
      ;
BR3: MOV #2,-(R2) ;MOVE TO MAILBOX # ***** 2 *****
     INC -(R2) ;SET MSGTYP TO FATAL ERROR
     HALT
     SEZ
     BNE BR4
     BR BR5
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; BRANCH INSTRUCTION AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; FOLLOWING W/ 760 <====
      ;
BR4: MOV #3,-(R2) ;MOVE TO MAILBOX # ***** 3 *****
     INC -(R2) ;SET MSGTYP TO FATAL ERROR
     HALT ;SHOULD NOT HAVE BRANCHED HERE ON Z=1
BR5: BEQ TST2
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; CONDITIONAL BRANCH INST. AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; WHICH FOLLOWS W/ 754 <====
      ;
      ; MOVE TO MAILBOX # ***** 4 *****
      ; SET MSGTYP TO FATAL ERROR
      ; SHOULD HAVE BRANCHED ON Z=1
      ; OR SEQUENCE ERROR

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SBTTL DATA PATH TESTS

THE DATA PATH TESTS ARE USED TO VERIFY THAT VARIOUS
DATA PATTERNS CAN BE SUCCESSFULLY MOVED THROUGH THE DATA PATHS
MOVE AND COMPARE MODE 2,3 INSTRUCTIONS ARE USED TO PASS AND
TEST VARIOUS DATA PATTERNS IN THE DATA PATHS.

THE TEST EXERCISES THE INTERNAL DATA PATHS, THE UNIBUS
DATA TRANSCIEVERS, AND AMUX CONTROL FOR ALU AND UBUS INPUTS.
IF THESE TESTS FAIL, EXAMINE THE TARGET LOCATION (LOC. 0)
TO SEE WHICH BITS OF THE DATA PATH ARE FAILING. IF THIS PROVIDES
INCONCLUSIVE DATA, TRY TO CHECK MODE 3 IR DECODE BY RUNNING
JUST THE MICROCODE AND IR DECODE TESTS FOR THE MOVE AND COMPARE
INSTRUCTIONS.

TEST 2 TEST OF ZEROES IN THE DATA PATH

```
TST2:  INC      (R2)          ; UPDATE TEST NUMBER
      CMP      #2,(R2)      ; SEQUENCE ERROR?
      BNE     TST3-10      ; BR TO ERROR HALT ON SEQ ERROR
      MOV     #0, @#0      ; MOVE ZEROES THRU ADDRESS LINES, DATA
                          ; LINES AND INTERNAL PATHS
      TST     @#0          ; SUCCESSFUL?
      BEQ     TST3

      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; CONDITIONAL BRANCH INST. AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; WHICH FOLLOWS W/ 772 <====

      MOV     #5, -(R2)    ; MOVE TO MAILBOX # ***** 5 *****
      INC     -(R2)        ; SET MSGTYP TO FATAL ERROR
      HALT                    ; DATA INCORRECT
                          ; OR SEQUENCE ERROR
```

TEST 3 TEST OF PATTERN 125252 IN DATA PATH

```
TST3:  INC      (R2)          ; UPDATE TEST NUMBER
      CMP      #3,(R2)      ; SEQUENCE ERROR?
      BNE     TST4-10      ; BR TO ERROR HALT ON SEQ ERROR
      MOV     #125252, @#0  ; MOVE ALTERNATING ONES AND ZEROES
                          ; THRU DATA PATHS
      CMP     #125252, @#0  ; SUCCESSFUL
      BEQ     TST4

      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ; CONDITIONAL BRANCH INST. AND <====
      ; REPLACE THE MOVE INSTRUCTION <====
      ; WHICH FOLLOWS W/ 771 <====

      MOV     #6, -(R2)    ; MOVE TO MAILBOX # ***** 6 *****
      INC     -(R2)        ; SET MSGTYP TO FATAL ERROR
      HALT                    ; DATA INCORRECT
                          ; OR SEQUENCE ERROR
```

TEST 4 TEST OF PATTERN 052525 IN DATA PATH

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MAINDEC-11-DGKAA 11:04 CPU TEST MACY11 27(732) 06-OCT-76 14:01 PAGE 169
DGKAA.P11 T4 TEST OF PATTERN 052525 IN DATA PATH

```
600 000736 005212          TST4:  INC      (R2)          ;UPDATE TEST NUMBER
601 000740 022712 000004    CMP      #4,(R2)        ;SEQUENCE ERROR?
602 000744 001007          BNE     TST5-10        ;BR TO ERROR HALT ON SEQ ERROR
603 000746 012737 052525 000000  MOV     #052525,0#0    ;MOVE ALTERNATING ZEROES AND ONES
604                                ;THRU DATA PATH
605 000754 022737 052525 000000  CMP     #052525,0#0    ;SUCCESSFUL?
606 000762 001404          BEQ     TST5
607                                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
608                                ;          CONDITIONAL BRANCH INST. AND <====
609                                ;          REPLACE THE MOVE INSTRUCTION <====
610                                ;          WHICH FOLLOWS W/ 771 <====
611 000764 012742 000007    MOV     #7, -(R2)      ;MOVE TO MAILBOX # ***** 7 *****
612 000770 005242          INC     -(R2)         ;SET MSGTYP TO FATAL ERROR
613 000772 000000          HALT                    ;DATA INCORRECT
614                                ; OR SEQUENCE ERROR
615
616 ;*****
617 ;TEST 5 TEST OF ALL ONES IN DATA PATH
618 ;*****
619 000774 005212          TST5:  INC      (R2)          ;UPDATE TEST NUMBER
620 000776 022712 000005    CMP     #5,(R2)        ;SEQUENCE ERROR?
621 001002 001007          BNE     TST6-10        ;BR TO ERROR HALT ON SEQ ERROR
622 001004 012737 177777 000000  MOV     #177777,0#0    ;MOVE ONES THRU DATA PATH
623 001012 022737 177777 000000  CMP     #177777,0#0    ;SUCCESSFUL
624 001020 001404          BEQ     TST6
625                                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
626                                ;          CONDITIONAL BRANCH INST. AND <====
627                                ;          REPLACE THE MOVE INSTRUCTION <====
628                                ;          WHICH FOLLOWS W/ 771 <====
629 001022 012742 000010    MOV     #10, -(R2)     ;MOVE TO MAILBOX # ***** 10 *****
630 001026 005242          INC     -(R2)         ;SET MSGTYP TO FATAL ERROR
631 001030 000000          HALT                    ;DATA INCORRECT
632                                ; OR SEQUENCE ERROR
```

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 SBTTL SCRATCH PAD TESTS

THE SCRATCH PAD TESTS ARE USED TO VERIFY THAT VARIOUS DATA PATTERNS CAN BE SUCCESSFULLY HELD IN THE SCRATCH PAD CIRCUITRY. MOVE AND COMPARE INSTRUCTIONS ARE USED TO TEST THAT RO CAN HOLD VARIOUS DATA PATTERNS. EACH DATA PATTERN IS MOVED AND TESTED IN A SMALL LOOP CONVENIENT FOR SCOPING. THE SUCCESSFUL COMPLETION OF THESE TESTS SHOULD VERIFY THE CIRCUITRY EXTERNAL TO THE SCRATCH PAD ITSELF.

THE REMAINDER OF THE GENERAL REGISTERS ARE TESTED BY MOVING A BIT INTO BIT 0 OF THE REGISTER AND SHIFTING IT LEFT ONE BIT AT A TIME INTO THE CARRY BIT. THE RESULT IS THEN CHECKED TO INSURE THAT NO BITS WERE PICKED.

AT THIS POINT ALL OF THE GENERAL REGISTERS HAVE BEEN EXERCISED AS WELL AS REGISTER 11. REGISTERS 10 AND 12 HAVE BEEN ACCESSED BY THE INSTRUCTIONS. REGISTERS 13,14,AND 17 WILL BE TESTED LATER IN THE MICROCODE TESTS.

IF THE PATTERN TESTS WITH REGISTER 0 FAIL CHECK THE RESULTANT DATA FOR A CLUE TO A FAULT IN THE EXTERNAL CIRCUITRY. IF THE PATTERN TESTS WITH RO ARE SUCCESSFUL BUT THE TESTS WITH THE OTHER REGISTERS FAIL, SUSPECT THE REGISTER SELECT LINES AND THEN THE SCRATCH PAD ITSELF.

 TEST 6 TEST IF RO CAN HOLD ALL ZEROES

```
TST6:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #6,(R2)    ;SEQUENCE ERROR?
        BNE     TST7-10    ;BR TO ERROR HALT ON SEQ ERROR
        MOV      #0,RO      ;MOVE ZEROES TO RO
        TST     RO         ;SUCCESSFUL?
        BEQ     TST7
```

```
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;          CONDITIONAL BRANCH INST. AND <====
;          REPLACE THE MOVE INSTRUCTION <====
;          WHICH FOLLOWS W/ 774 <====
```

```
        MOV      #11,-(R2) ;MOVE TO MAILBOX # ***** 11 *****
        INC     -(R2)      ;SET MSGTYP TO FATAL ERROR
        HALT                    ;RO NOT 0
; OR SEQUENCE ERROR
```

 TEST 7 TEST IF RO CAN HOLD ONES AND ZEROES

```
TST7:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #7,(R2)    ;SEQUENCE ERROR?
        BNE     TST10-10    ;BR TO ERROR HALT ON SEQ ERROR
        MOV      #125252,RO ;MOVE ALTERNATING ONES AND ZEROES TO RO
        CMP     RO,#125252  ;SUCCESSFUL?
        BEQ     TST10
```

```
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
;          CONDITIONAL BRANCH INST. AND <====
;          REPLACE THE MOVE INSTRUCTION <====
```

```

689
690 001104 012742 000012      MOV      #12,-(R2)      ; MOVE TO MAILBOX # ***** 12 *****
691 001110 005242              INC      -(R2)         ; SET MSGTYP TO FATAL ERROR
692 001112 000000              HALT                    ; RO NOT 125252
693                                     ; OR SEQUENCE ERROR
694
695 ;*****
696 ;TEST 10      TEST IF RO CAN HOLD ZEROES AND ONES
697 ;*****
698 001114 005212              TST10: INC      (R2)          ; UPDATE TEST NUMBER
699 001116 022712 000010      CMP      #10,(R2)      ; SEQUENCE ERROR?
700 001122 001005              BNE     TST11-10       ; BR TO ERROR HALT ON SEQ ERROR
701 001124 012700 052525      MOV      #052525,RO    ; MOVE ALTERNATING ZEROES AND ONES TO RO
702 001130 020027 052525      CMP      RO,#052525    ; SUCCESSFUL?
703 001134 001404              BEQ     TST11
704                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
705                                     ; CONDITIONAL BRANCH INST. AND <====
706                                     ; REPLACE THE MOVE INSTRUCTION <====
707                                     ; WHICH FOLLOWS W/ 773 <====
708 001136 012742 000013      MOV      #13,-(R2)      ; MOVE TO MAILBOX # ***** 13 *****
709 001142 005242              INC      -(R2)         ; SET MSGTYP TO FATAL ERROR
710 001144 000000              HALT                    ; RO NOT 52525
711                                     ; OR SEQUENCE ERROR
712
713 ;*****
714 ;TEST 11      TEST IF RO CAN HOLD ALL ONES
715 ;*****
716 001146 005212              TST11: INC      (R2)          ; UPDATE TEST NUMBER
717 001150 022712 000011      CMP      #11,(R2)      ; SEQUENCE ERROR?
718 001154 001005              BNE     TST12-10       ; BR TO ERROR HALT ON SEQ ERROR
719 001156 012700 177777      MOV      #177777,RO    ; MOVE ALL ONES TO RO
720 001162 020027 177777      CMP      RO,#177777    ; SUCCESSFUL?
721 001166 001404              BEQ     TST12
722                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
723                                     ; CONDITIONAL BRANCH INST. AND <====
724                                     ; REPLACE THE MOVE INSTRUCTION <====
725                                     ; WHICH FOLLOWS W/ 773 <====
726 001170 012742 000014      MOV      #14,-(R2)      ; MOVE TO MAILBOX # ***** 14 *****
727 001174 005242              INC      -(R2)         ; SET MSGTYP TO FATAL ERROR
728 001176 000000              HALT                    ; RO NOT 177777
729                                     ; OR SEQUENCE ERROR
730
731 ;*****
732 ;TEST 12      TEST IF R1 CAN HOLD A ONE IN ALL BITS
733 ;*****
734 001200 005212              TST12: INC      (R2)          ; UPDATE TEST NUMBER
735 001202 022712 000012      CMP      #12,(R2)      ; SEQUENCE ERROR?
736 001206 001006              BNE     TST13-10       ; BR TO ERROR HALT ON SEQ ERROR
737 001210 012701 000001      MOV      #1,R1         ; SET BIT 0
738 001214 000241              CLC                    ; CLEAR C-BIT
739 001216 006101              REG1: ROL      R1        ; ROTATE 1 POSITION
740 001220 103376              BCC     REG1           ; ALL DONE
741 001222 001404              BEQ     TST13
742                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
743                                     ; CONDITIONAL BRANCH INST. AND <====
744                                     ; REPLACE THE MOVE INSTRUCTION <====

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745
746 001224 012742 000015      MOV    #15,-(R2)      ; MOVE TO MAILBOX # ***** 15 *****
747 001230 005242              INC    -(R2)          ; SET MSGTYP TO FATAL ERROR
748 001232 000000              HALT                   ; FAILURE WITH R1
749                                  ; OR SEQUENCE ERROR
750
751 ;*****
752 ;TEST 13      TEST IF R2 CAN HOLD A ONE IN ALL BITS
753 ;*****
754 001234 005212      TST13: INC    (R2)          ; UPDATE TEST NUMBER
755 001236 022712      CMP    #13,(R2)       ; SEQUENCE ERROR?
756 001242 001006      BNE   REG2A-14        ; BR TO ERROR HALT ON SEQ ERROR
757 001244 012702      MOV    #1,R2          ; SET BIT 0
758 001250 000241      CLC                   ; CLEAR C-BIT
759 001252 006102      REG2: ROL    R2        ; ROTATE 1 POSITION
760 001254 103376      BCC   REG2            ; ALL DONE
761 001256 001406      BEQ   REG2A          ;
762
763 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
764 ; BRANCH INSTRUCTION AND <====
765 ; REPLACE THE MOVE INSTRUCTION <====
766 ; FOLLOWING W/ 771 <====
766 001260 012702 000304      MOV    $TESTN,R2     ; RESTORE POINTER
767 001264 012742 000016      MOV    #16,-(R2)     ; MOVE TO MAILBOX # ***** 16 *****
768 001270 005242              INC    -(R2)          ; SET MSGTYP TO FATAL ERROR
769 001272 000000              HALT                   ; FAILURE WITH R2
770 001274 012702 000304      REG2A: MOV   $TESTN,R2 ; RESTORE POINTER
771 ;*****
772 ;TEST 14      TEST IF R3 CAN HOLD A ONE IN ALL BITS
773 ;*****
774 001300 005212      TST14: INC    (R2)          ; UPDATE TEST NUMBER
775 001302 022712      CMP    #14,(R2)       ; SEQUENCE ERROR?
776 001306 001006      BNE   TST15-10        ; BR TO ERROR HALT ON SEQ ERROR
777 001310 012703 000001      MOV    #1,R3          ; SET BIT 0
778 001314 000241      CLC                   ; CLEAR C-BIT
779 001316 006103      REG3: ROL    R3        ; ROTATE 1 POSITION
780 001320 103376      BCC   REG3            ; ALL DONE
781 001322 001404      BEQ   TST15          ;
782
783 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
784 ; CONDITIONAL BRANCH INST. AND <====
785 ; REPLACE THE MOVE INSTRUCTION <====
786 ; WHICH FOLLOWS W/ 772 <====
786 001324 012742 000017      MOV    #17,-(R2)     ; MOVE TO MAILBOX # ***** 17 *****
787 001330 005242              INC    -(R2)          ; SET MSGTYP TO FATAL ERROR
788 001332 000000              HALT                   ; FAILURE WITH R3
789                                  ; OR SEQUENCE ERROR
790
791 ;*****
792 ;TEST 15      TEST IF R4 CAN HOLD A ONE IN ALL BITS
793 ;*****
794 001334 005212      TST15: INC    (R2)          ; UPDATE TEST NUMBER
795 001336 022712      CMP    #15,(R2)       ; SEQUENCE ERROR?
796 001342 001006      BNE   TST16-10        ; BR TO ERROR HALT ON SEQ ERROR
797 001344 012704 000001      MOV    #1,R4          ; SET BIT 0
798 001350 000241      CLC                   ; CLEAR C-BIT
799 001352 006104      REG4: ROL    R4        ; ROTATE 1 POSITION
800 001354 103376      BCC   REG4            ; ALL DONE

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801 001356 001404
802
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806 001360 012742 000020
807 001364 005242
808 001366 000000
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810
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BEG TST16

MOV #20, -(R2)
INC -(R2)
HALT

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 772 <====
: MOVE TO MAILBOX # ***** 20 *****
: SET MSGTYP TO FATAL ERROR
: FAILURE WITH R4
: OR SEQUENCE ERROR

: TEST 16 TEST IF R5 CAN HOLD A ONE IN ALL BITS

814 001370 005212
815 001372 022712 000016
816 001376 001006
817 001400 012705 000001
818 001404 000241
819 001406 006105
820 001410 103376
821 001412 001404
822

TST16: INC (R2)
CMP #16, (R2)
BNE TST17-10
MOV #1, R5
CLC
REG5: ROL R5
BCC REG5
BEG TST17

: UPDATE TEST NUMBER
: SEQUENCE ERROR?
: BR TO ERROR HALT ON SEQ ERROR
: SET BIT 0
: CLEAR C-BIT
: ROTATE 1 POSITION
: ALL DONE

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 772 <====
: MOVE TO MAILBOX # ***** 21 *****
: SET MSGTYP TO FATAL ERROR
: FAILURE WITH R5
: OR SEQUENCE ERROR

: TEST 17 TEST IF R6 CAN HOLD A ONE IN ALL BITS

834 001424 005212
835 001426 022712 000017
836 001432 001006
837 001434 012706 000001
838 001440 000241
839 001442 006106
840 001444 103376
841 001446 001404
842
843
844

TST17: INC (R2)
CMP #17, (R2)
BNE TST20-10
MOV #1, R6
CLC
REG6: ROL R6
BCC REG6
BEG TST20

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 772 <====
: MOVE TO MAILBOX # ***** 22 *****
: SET MSGTYP TO FATAL ERROR
: FAILURE WITH R6
: OR SEQUENCE ERROR

846 001450 012742 000022
847 001454 005242
848 001456 000000
849
850

MOV #22, -(R2)
INC -(R2)
HALT

002

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*****
SBTTL PSW TESTS

THE PSW TESTS ARE USED TO VERIFY THAT VARIOUS DATA
PATTERNS CAN BE SUCCESSFULLY HELD IN THE PSE AND THAT THE
PSW ADDRESSING LOGIC IS FUNCTIONING. MOVE AND COMPARE INSTRUCTIONS
ARE USED TO TEST THAT THE PSE CAN HOLD VARIOUS DATA PATTERNS.
EACH DATA PATTERN IS MOVED AND TESTED IN A SMALL LOOP CONVENIENT FOR
SCOPING.
THE PSW REGISTER ITSELF IS TESTED AS WELL AS THE ADDRESS
SELECT CIRCUITRY. THE AMUX INPUTS TO THE PSW MUX ARE TESTED. THE
CC INPUTS ARE TESTED LATER IN THE MICROCODE TESTS. SETTING OF
THE T-BIT BY THE TEST PATTERNS IS PURPOSELY AVOIDED; TESTING OF THE
T-BIT TRAP CIRCUITRY IS LEFT FOR THE TRAP TEST.

*****
TEST 20 TEST IF PSW WILL HOLD ZEROES
*****
TST20: INC (R2) ;UPDATE TEST NUMBER
CMP #20,(R2) ;SEQUENCE ERROR?
BNE TST21-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #STBOT,R6
MOV #0,#PS ;SET PSW TO ZERO
TST #PS ;SUCCESSFUL
BEQ TST21

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====

MOV #23,-(R2) ;MOVE TO MAILBOX # ***** 23 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;PSW NOT 0
; OR SEQUENCE ERROR

*****
TEST 21 TEST IF PSW WILL HOLD ONES AND ZEROES
*****
TST21: INC (R2) ;UPDATE TEST NUMBER
CMP #21,(R2) ;SEQUENCE ERROR?
BNE TST22-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #252,#PS ;MOVE ALT. ONES AND ZEROES TO PSW
CMP #PS,#252 ;SUCCESSFUL?
BEQ TST22

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====

MOV #24,-(R2) ;MOVE TO MAILBOX # ***** 24 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;PSW NOT 252
; OR SEQUENCE ERROR

*****
TEST 22 TEST IF PSW (EXCEPT T-BIT) WILL HOLD ZEROES AND ONES
*****

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000020
000500 177776
000000 177776
001404
000023
000000
000021
000252 177776 000252
001404
000024
000000

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995
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998
999 001764 012742 000031      MOV      #31, -(R2)
1000 001770 005242      INC      -(R2)
1001 001772 000000      HALT
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 761
; MOVE TO MAILBOX # ***** 31 *****
; SET MSGTYP TO FATAL ERROR
; BIT 0 NOT SET
; OR SEQUENCE ERROR
; *****
; TEST 26      LEFT SHIFT FROM BIT 0 TO C-BIT
; *****
1007 001774 005212      †ST26:  INC      (R2)      ; UPDATE TEST NUMBER
1008 001776 022712 000026      CMP      #26, (R2)      ; SEQUENCE ERROR?
1009 002002 001010      BNE     TST27-10      ; BR TO ERROR HALT ON SEQ ERROR
1010 002004 012737 000001 000000      MOV      #1, @#0      ; SET BIT 0
1011 002012 000241      CLC
1012 002014 006137 000000      SHL:    ROL      @#0      ; CLEAR C-BIT
1013 002020 103375      BCC     SHL           ; SHIFT LEFT ONE POSITION
1014 002022 001404      BEQ     TST27         ; BRANCH IF C-BIT NOT SET
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 770
; MOVE TO MAILBOX # ***** 32 *****
; SET MSGTYP TO FATAL ERROR
; LEFT SHIFTING LOGIC FAILED
; OR SEQUENCE ERROR
; *****
; TEST 27      SHIFT BIT 15 TO BIT 14
; *****
1027 002034 005212      †ST27:  INC      (R2)      ; UPDATE TEST NUMBER
1028 002036 022712 000027      CMP      #27, (R2)      ; SEQUENCE ERROR?
1029 002042 001012      BNE     TST30-10      ; BR TO ERROR HALT ON SEQ ERROR
1030 002044 012737 100000 000000      MOV      #100000, @#0   ; SET BIT 15
1031 002052 000241      CLC      ; CLEAR CARRY
1032 002054 006037 000000      ROR      @#0           ; SHIFT BIT 15 TO BIT 14
1033 002060 022737 040000 000000      CMP      #40000, @#0    ; SUCCESSFUL
1034 002066 001404      BEQ
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 766
; MOVE TO MAILBOX # ***** 33 *****
; SET MSGTYP TO FATAL ERROR
; BIT 14 NOT SET
; OR SEQUENCE ERROR
; *****
; TEST 30      RIGHT SHIFT FROM BIT 15 TO C-BIT
; *****
1047 002100 005212      †ST30:  INC      (R2)      ; UPDATE TEST NUMBER
1048 002102 022712 000030      CMP      #30, (R2)      ; SEQUENCE ERROR?
1049 002106 001010      BNE     TST31-10      ; BR TO ERROR HALT ON SEQ ERROR
1050 002110 012737 100000 000000      MOV      #100000, @#0   ; SET BIT 15

```

```

:051 002116 000241
:052 002120 006037 000000
:053 002124 103375
:054 002126 001404
:055
:056
:057
:058
:059 002130 012742 000034
:060 002134 005242
:061 002136 000000
:062

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```

S-M: CLC
ROR 380
BCC SHR
BEQ TST31

MOV #34 -(R2)
INC -(R2)
HLT

```

```

: CLEAR C-BIT
: ROTATE RIGHT ONE POSITION
: BRANCH IF C-BIT CLEAR

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
: CONDITIONAL BRANCH INST. AND (====
: REPLACE THE MOVE INSTRUCTION (====
: WHICH FOLLOWS W/ 770 (====

: MOVE TO MAILBOX # ***** 34 *****
: SET MSGTYP TO FATAL ERROR
: RIGHT SHIFT LOGIC FAILED
: OR SEQUENCE ERROR

```

SETL CONDITION CODE TEST

```

*****
THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE Z-BIT.
THE Z-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
BEQ AND BNE ARE TESTED FOR PROPER EXECUTION. THEN THE Z-BIT IS
SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
AGAIN FOR PROPER OPERATION.
THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
USED IN THE TEST ARE VERIFIED HERE.
*****

```

TEST 31 TEST BRANCHES AROUND Z-BIT

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002140 005212
002142 022712 000031
002146 001014
002150 000257
002152 000264
002154 001001
002156 001404
002160
002160 012742 000035
002164 005242
002166 000000
002170 000277
002172 000244
002174 001401
002176 001004
002200
002200 012742 000036
002204 005242
002206 000000

```

```

*****
TST31: INC (R2) ;UPDATE TEST NUMBER
CMP #31,(R2) ;SEQUENCE ERROR?
BNE TST32-10 ;BR TO ERROR HALT ON SEQ ERROR
;FIRST WITH Z-BIT ON
CCC ;CC=0100: JUST Z-BIT
SEZ
BNE BRZ1 ;CHECK OPPOSITE CONDITION
BEQ BRZ2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 774 <====
BRZ1: MOV #35,-(R2) ;MOVE TO MAILBOX # ***** 35 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ Z=1
;CHECK WITH Z-BIT OFF
BRZ2: SCC ;CC=1011: ALL BUT Z-BIT
CLZ
BEQ BRZ3
BNE TST32
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====
BRZ3: MOV #36,-(R2) ;MOVE TO MAILBOX # ***** 36 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ Z=0
; OR SEQUENCE ERROR

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002210 005212
002212 022712 000032
002216 001014
002220 000257
002222 000270
002224 1000C1
002226 100404
002230 012742 000037
002234 005242
002236 000000
002240 000277
002242 000250
002244 100401
002246 100004
002250 012742 000040
002254 005242
002256 000000

```

*****
THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE N-BIT.
THE N-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
BMI AND BPL ARE TESTED FOR PROPER EXECUTION. THEN THE N-BIT IS
SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
AGAIN FOR PROPER OPERATION.
THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
USED IN THE TEST ARE VERIFIED HERE.
*****
TEST 32 TEST BRANCHES AROUND N-BIT
*****
TST32: INC (R2) ;UPDATE TEST NUMBER
CMP #32,(R2) ;SEQUENCE ERROR?
BNE TST33-10 ;BR TO ERROR HALT ON SEQ ERROR
;FIRST WITH N-BIT ON
CCC ;CC=1000: JUST N-BIT
SEN
BPL BRN1 ;CHECK OPPOSITE CONDITION
BMI BRN2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 774 <====
BRN1: MOV #37,-(R2) ;MOVE TO MAILBOX # ***** 37 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ N=1
;CHECK WITH N-BIT OFF
BRN2: SCC ;CC=0111
CLN
BMI BRN3 ;CHECK OPPOSITE CONDITION
BPL TST33
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====
BRN3: MOV #40,-(R2) ;MOVE TO MAILBOX # ***** 40 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ N=0
; OR SEQUENCE ERROR

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1199
1200
1201
1202
1203
1204

002260 005212
002262 022712 000033
002266 001014
002270 000257
002272 000262
002274 102001
002276 102404
002300
002300 012742 000041
002304 005242
002306 000000
002310 000277
002312 000242
002314 102401
002316 102004
002320
002320 012742 000042
002324 005242
002326 000000

```
*****
THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE V-BIT.
THE V-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
BVS AND BVC ARE TESTED FOR PROPER EXECUTION. THEN THE V-BIT IS
SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
AGAIN FOR PROPER OPERATION.
THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
USED IN THE TEST ARE VERIFIED HERE.
*****
TEST 33 TEST BRANCHES AROUND V-BIT
*****
TST33: INC (R2) ;UPDATE TEST NUMBER
CMP #33,(R2) ;SEQUENCE ERROR?
BNE TST34-10 ;BR TO ERROR HALT ON SEQ ERROR
;FIRST WITH V-BIT ON
;CC=0010: JUST V-BIT
CCC ;CC=0010: JUST V-BIT
SEV
BVC BRV1 ;CHECK OPPOSITE CONDITION
BVS BRV2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 774 <====
BRV1: MOV #41,-(R2) ;MOVE TO MAILBOX # ***** 41 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ V=1
;CHECK WITH V-BIT OFF
BRV2: SCC ;CC=1101: ALL BVT V-BIT
CLV
BVS BRV3 ;CHECK OPPOSITE CONDITION
BVC TST34
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====
BRV3: MOV #42,-(R2) ;MOVE TO MAILBOX # ***** 42 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ V=0
; OR SEQUENCE ERROR
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002330 005212
002332 022712 000034
002336 001014
002340 000257
002342 000261
002344 103001
002346 103404
002350
002350 012742 000043
002354 005242
002356 000000
002360 000277
002362 000242
002364 102401
002366 100404
002370
002370 012742 000044
002374 005242
002376 000000

```
*****
: THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE C-BIT.
: THE C-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
: BCS AND BCC ARE TESTED FOR PROPER EXECUTION. THEN THE C-BIT IS
: SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
: AGAIN FOR PROPER OPERATION.
: THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
: CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
: BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
: LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
: USED IN THE TEST ARE VERIFIED HERE.
*****
: TEST 34 TEST BRANCHES AROUND C-BIT
*****
TST34: INC (R2) ;UPDATE TEST NUMBER
CMP #34,(R2) ;SEQUENCE ERROR?
BNE TST35-10 ;BR TO ERROR HALT ON SEQ ERROR
;FIRST WITH C-BIT ON
CC ;CC=0001: JUST C-BIT
SEC ;CHECK OPPOSITE CONDITION
BCC BRC1
BCS BRC2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 774 <====
BRC1: MOV #43,-(R2) ;MOVE TO MAILBOX # ***** 43 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ C=1
;CHECK WITH V-BIT OFF
BRC2: SCC ;CC=1110
CLV ;CHECK OPPOSITE CONDITION
BVS BRC3
BMI TST35
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====
BRC3: MOV #44,-(R2) ;MOVE TO MAILBOX # ***** 44 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;IMPROPER BR W/ C=0
; OR SEQUENCE ERROR
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;SBTTL MICROCODE TESTS

THE MICROCODE TESTS ARE USED TO VERIFY THE MICROPROGRAMM
FLOW. THE GOAL OF THESE TESTS IS TO EXERCISE EVERY POSSIBLE
BRANCH IN THE MICROPROGRAM FLOW.

THE TEST EXERCISES EVERY BRANCH IN THE MICROCODE BY
TESTING AT LEAST ONE INSTRUCTION FROM EVERY CLASS OF INSTRUCTION IN
ALL POSSIBLE MODES. FOR EXAMPLE, TO TEST THE SINGLE OPERAND INSTRUCTIONS,
AT LEAST ONE SINGLE OPERAND INSTRUCTION IS VERIFIED IN ALL UNIQUE
ADDRESSING MODES. BYTE MODES ARE ALSO TESTED. AS EACH NEW
MODE IS INTRODUCED THE SAME INSTRUCTION IS TRIED AND TESTED IN
A SMALL LOOP CONVENIENT FOR SCOPING. THE TEST IS SET UP USING
ONLY INSTRUCTIONS AND ADDRESSING MODES WHICH HAVE BEEN PREVIOUSLY
VERIFIED.

IF THESE TESTS FAIL, CHECK THE RESULTS FOR A CLUE TO THE
FAULT.

THE CLR INSTRUCTION IS USED TO INTRODUCE EACH ADDRESSING
MODE WITH THE SINGLE OPERAND INSTRUCTION. FOLLOWING THE SEQUENCE CHECK,
THE CLR INSTRUCTION IS EXECUTED AND A BRANCH TEST IS EXECUTED WHICH
CHECKS THAT THE Z-BIT WAS PROPERLY SET. THIS SMALL TEST IS SELF-SUFFICIENT
AND CAN BE SCOPE TO TROUBLE SHOOT ALL OF THE IR DECODE LOGIC AND
MICROCODE FOR SOP INSTRUCTIONS WITH MODE 0. FOLLOWING THIS TEST
SEVERAL OTHER SOP INSTRUCTIONS ARE INTRODUCED WITH MODE 0. THESE
INSTRUCTIONS MAINPULATE DATA AND SERVE TO CHECK THE DATA RESULTS
OF THE SOP INSTRUCTIONS IN THIS TEST. THE DATA IN THIS TEST IS
OPERATED ON BY EACH INSTRUCTION WITHOUT REINITIALIZING.

;TEST 35 TEST MODE 0 USING SOP INST.

TST35: INC (R2) ;UPDATE TEST NUMBER
CMP #35,(R2) ;SEQUENCE ERROR?
BNE TST36-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R0 ;TRY THE CLEAR INST.
BEQ SOPOA

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 776 <====

MOV #45,-(R2) ;MOVE TO MAILBOX # ***** 45 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLR DID NOT SET Z-BIT
SOPOA: INC R0 ;TRY THE INCREMENT INST.
NEG R0 ;TRY THE NEGATE INST.
BMI SOPOB

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====

002400 005212
002402 022712 000035
002406 001017
002410 005000
002412 001404

002414 012742 000045
002420 005242
002422 000000
002424 005200
002426 005400
002430 100404


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1310 002432 012742 000046          MOV    #46,-(R2)          ; REPLACE THE MOVE INSTRUCTION <====
1311 002436 005242          INC    -(R2)             ; WHICH FOLLOWS W/ 767 <====
1312 002440 000000          HALT                    ; MOVE TO MAILBOX # ***** 46 *****
1313 002442 005100          COM    R0                ; SET MSGTYP TO FATAL ERROR
1314 002444 001404          BFG    TST36             ; NEGATE DID NOT SET N-BIT
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1319 002446 012742 000047          MOV    #47,-(R2)          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
1320 002452 005242          INC    -(R2)             ; CONDITIONAL BRANCH INST. AND <====
1321 002454 000000          HALT                    ; REPLACE THE MOVE INSTRUCTION <====
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1337 002456 005212          TST36: INC    (R2)          ; *****
1338 002460 022712 000036          CMP    #36,(R2)          ; THIS TEST INTRODUCES THE REMAINING SOP INSTRUCTIONS AND TESTS
1339 002464 001020          BNE    TST37-10         ; THEM IN MODE 0. THE PURPOSE IS TO PROVIDE A BASELINE OF
1340 002466 005000          CLR    R0                ; INSTRUCTIONS FOR USE IN THE SUBSEQUENT TESTS. SINCE THE MICROCODE FOR
1341 002470 005300          DEC    R0                ; THESE INSTRUCTIONS IS IDENTICAL TO THAT ALREADY TESTED, ANY TROUBLE
1342 002472 100404          BMI    SOPOC             ; SHOOTING EFFORTS SHOULD BE AIMED AT THE ACTUAL IR DECODE AND ALU
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1347 002474 012742 000050          MOV    #50,-(R2)          ; FUNCTIONING.
1348 002500 005242          INC    -(R2)             ; *****
1349 002502 000000          HALT                    ; TEST 36 TEST REMAINDER OF SOP INSTS IN MODE 0
1350 002504 000261          SEC                    ; *****
1351 002506 005500          ADC    R0                ; TST36: INC    (R2)          ; UPDATE TEST NUMBER
1352 002510 001006          BNE    SOPOD             ; SEQUENCE ERROR?
1353 002512 000261          SEC                    ; BR TO ERROR HALT ON SEQ ERROR
1354 002514 005600          SBC    R0                ; INITIALIZE
1355 002516 100003          BPL    SOPOD             ; TRY DECREMENT INST.
1356 002520 005400          NEG    R0                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
1357 002522 005300          DEC    R0                ; CONDITIONAL BRANCH INST. AND <====
1358 002524 001404          BEQ    TST37             ; REPLACE THE MOVE INSTRUCTION <====
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1363 002526          SOPOD:                  ; WHICH FOLLOWS W/ 775 <====
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N02

MAINDEC-11-DGKAA 11/04 CPU TEST MACY11 27(732) 06-OCT-76 14:01 PAGE 185
DGKAAA.P11 T36 TEST REMAINDER OF SOP INSTS IN MODE 0

1364 002526 012742 200051
1365 002532 005242
1366 002534 000000
1367

MOV #51 -(R2)
INC -(R2)
HALT

; MOVE TO MAILBOX # ***** 51 *****
; SET MSGTYP TO FATAL ERROR
; CUMMULATIVE RESULT OF ADC,SBC,NEG AND DEC INSTS. FAILE
; OR SEQUENCE ERROR

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002536 005212
002540 022712 000037
002544 001012
002546 :05C00
002550 001404

002552 012742 000052
002556 005242
002560 000000
002562 105100
002564 100002
002566 105200
002570 001404

002572 012742 000053
002572 005242
002576 000000

```
*****
: THIS TEST INTRODUCES THE BYTE CONTROL LOGIC OF THE PROCESSOR.
: THE MODE 0 BYTE MICROCODE IS TESTED. THE METHOD AND SEQUENCE
: OF TESTING IS THE SAME AS THAT USED IN THE SOP MODE 0 TESTS.
*****
: TEST 37 TEST MODE 0 EVEN BYTE USING SOP INST
*****
: ST37: INC (R2) ; UPDATE TEST NUMBER
: CMP #37,(R2) ; SEQUENCE ERROR?
: BNE TST40-10 ; BR TO ERROR HALT ON SEQ ERROR
: CLRB R0 ; TRY CLEARING EVEN BYTE OF REGISTER
: BEQ SOPBOA
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
: CONDITIONAL BRANCH INST. AND (====
: REPLACE THE MOVE INSTRUCTION (====
: WHICH FOLLOWS W/ 776 (====
: MOV #52,-(R2) ; MOVE TO MAILBOX # ***** 52 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; CLRB DID NOT SET Z-BIT
SOPBOA: COMB R0 ; TRY SETTING EVEN BYTE OF REGISTER
: BPL SOPBOB
: INCB R0 ; TRY INCREMENTING EVEN BYTE OF REGISTER>>
: BEQ TST40
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
: CONDITIONAL BRANCH INST. AND (====
: REPLACE THE MOVE INSTRUCTION (====
: WHICH FOLLOWS W/ 766 (====
: MOV #53,-(R2) ; MOVE TO MAILBOX # ***** 53 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; TEST CUMMULATIVE RESULT OF ABOVE BYTE INST.
: OR SEQUENCE ERROR
*****
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002602 005212
 002604 022712 000040
 002610 001014
 002612 005000
 002614 005010
 002616 001404
 012742 000054
 002624 005242
 002626 000000
 002630 005310
 002632 100003
 002634 000261
 002636 005510
 002640 001404
 002642
 002644 012742 000055
 002646 005242
 002650 000000

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*****
: THIS TEST USES THE CLR INSTRUCTION TO INTRODUCE AND TEST
: SINGLE OPERAND MODE 1 INSTRUCTIONS. AGAIN, THE CLR INSTRUCTION
: IS USED TO INTRODUCE THE MICROCODE AND TO TEST THAT THE PROPER
: CONDITION CODES ARE SET. OTHER SOP INSTRUCTIONS ARE USED TO MANIPULATE
: COMMON DATA TO VERIFY THAT THE CORRECT DATA IS PRODUCED.
*****
: TEST 40 TEST MODE 1 USING SOP INST.
*****
: ST40: INC (R2) ; UPDATE TEST NUMBER
: CMP #40,(R2) ; SEQUENCE ERROR?
: BNE TST41-10 ; BR TO ERROR HALT ON SEQ ERROR
: CLR R0 ; INITIALIZE R0
: CLR (R0) ; TRY CLEAR INST W/MODE 1
: BEQ SOP1A
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 775 <====
:
: MOV #54, -(R2) ; MOVE TO MAILBOX # ***** 54 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; CLR DID NOT SET Z-BIT
:
: SOP1A: DEC (R0) ; TRY DECREMENT INST W/MODE 1
: BPL SOP1B
: SEC ; INITIALIZE CARRY
: ADC (R0) ; TRY ADD-CARRY W/MODE 1
: BEQ TST41
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 764 <====
:
: SOP1B: MOV #55, -(R2) ; MOVE TO MAILBOX # ***** 55 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; TEST CUMULATIVE RESULT OF ABOVE INST
: OR SEQUENCE ERROR
    
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*****
THIS TEST VERIFIES THE BYTE INSTRUCTION MICROCODE FOR MODE 1
SINGLE OPERAND INSTRUCTIONS.
THIS IS THE FIRST PLACE THE SIGN EXTEND LOGIC IS EXERCISED
AND VERIFIED.
*****
TEST 41      TEST MODE 1 EVEN BYTE USING SOP INST
*****
TST41:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #41,(R2)     ;SEQUENCE ERROR?
        BNE     TST42-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0           ;INITIALIZE R0
        CLR     (R0)        ;INITIALIZE LOC. 0
        COM     (R0)
        CLRB   (R0)        ;TRY TO CLEAR BYTE 0
        BEQ    SOPB1A
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
        ;           CONDITIONAL BRANCH INST. AND
        ;           REPLACE THE MOVE INSTRUCTION
        ;           WHICH FOLLOWS W/ 773
        ;           <====
        ;           <====
        ;           <====
        ;           <====
        MOV     #56,-(R2)    ;MOVE TO MAILBOX # ***** 56 *****
        INC     -(R2)
        HALT
SOPB1A:  INC     (R0)        ;SET MSGTYP TO FATAL ERROR
        BPL   SOPB1B       ;CLRB DID NOT SET Z-BIT
        NEGB  (R0)        ;INCREMENT TO TEST WORD
        BPL   SOPB1B
        INCB  (R0)
        BEQ   TST42
        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
        ;           CONDITIONAL BRANCH INST. AND
        ;           REPLACE THE MOVE INSTRUCTION
        ;           WHICH FOLLOWS W/ 761
        ;           <====
        ;           <====
        ;           <====
        ;           <====
SOPB1B:  MOV     #57,-(R2)    ;MOVE TO MAILBOX # ***** 57 *****
        INC     -(R2)
        HALT
        ;SET MSGTYP TO FATAL ERROR
        ;CHECK CUMMULATIVE RESULT OF ABOVE INST
        ;OR SEQUENCE ERROR

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002652 005212
002654 022712 000041
002660 001017
002662 005000
002664 005010
002666 005110
002670 105410
002672 001404

002674 012742 000056
002700 005242
002702 000000
002704 005210
002706 100004
002710 105410
002712 100002
002714 105210
002716 001404

002720
002720 012742 000057
002724 005242
002726 000000

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THIS TEST VERIFIES THAT SINGLE OPERAND BYTE INSTRUCTIONS WILL
FUNCTION CORRECTLY FOR ODD BYTES.
THIS IS THE FIRST TIME THAT ADDRESS LINE 0 HAS BEEN
EXERCISED. CHECKS ARE MADE THAT THE PROPER BYTE IS MODIFIED AND
THE CONDITION CODES ARE CHECKED. IT IS ALSO VERIFIED THAT THE UNADDRESSED
BYTE IS NOT ALTERED BY THE INSTRUCTION.

TEST 42 TEST MODE 1 ODD BYTE USING SOP INST

002730 005212
002732 022712 000042
002736 001021
002740 005000
002742 005010
002744 005110
002746 005200
002750 105010
002752 001404

TST42: INC (R2) ; UPDATE TEST NUMBER
CMP #42,(R2) ; SEQUENCE ERROR?
BNE TST43-10 ; BR TO ERROR HALT ON SEQ ERROR
CLR R0 ; INITIALIZE R0
CLR (R0) ; INITIALIZE LOC. 0
COM (R0)
INC R0 ; R0=ODD BYTE
CLRB (R0) ; TRY TO CLEAR BYTE 1
BEQ SOPB1C

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
CONDITIONAL BRANCH INST. AND <====
REPLACE THE MOVE INSTRUCTION <====
WHICH FOLLOWS W/ 772 <====

002754 012742 000060
002760 005242
002762 000000
002764 005300
002766 005210
002770 005200
002772 105410
002774 100002
002776 105210
003000 001404

MOV #60,-(R2) ; MOVE TO MAILBOX # ***** 60 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CLRB DID NOT SET Z-BIT
SOPB1C: DEC R0 ; R0=WORD ADDR.
INC (R0) ; INCREMENT TO TEST WORD
INC R0 ; R0=ODD BYTE
NEGB (R0) ; TRY TO NEGATE BYTE 1
BPL SOPB1D
INCB (R0) ; TRY TO INCREMENT BYTE 1
BEQ TST43

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
CONDITIONAL BRANCH INST. AND <====
REPLACE THE MOVE INSTRUCTION <====
WHICH FOLLOWS W/ 757 <====

003002
003002 012742 000061
003006 005242
003010 000000

SOPB1D: MOV #61,-(R2) ; MOVE TO MAILBOX # ***** 61 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; TEST CUMMULATIVE RESULT OF ABOVE INST.
; OR SEQUENCE ERROR

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003012 005212
003014 022712 000043
003020 001023
003022 005000
003024 105100
003026 005200
003030 005010
003032 005110
003034 005020
003036 001404

003040 012742 000062
003044 005242
003046 000000
003050 005300
003052 005300
003054 005120
003056 100004
003060 005300
003062 005300
003064 005220
003066 001404

003070 012742 000063
003074 005242
003076 000000

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*****
:
: THIS TEST VERIFIES MODE 2 SINGLE-OPERAND INSTRUCTIONS. PREVIOUSLY
: TESTED INSTRUCTIONS ARE USED TO SET A POINTER IN RO TO LOC. 400.
: LOC. 400 IS INITIALIZED TO -1 BEFORE A CLR MODE 2 IS EXECUTED.
: THEN RO IS DECREMENTED BY TWO TO AGAIN POINT TO 400 BEFORE EACH
: OF SEVERAL MODE 2 INSTRUCTIONS ARE USED TO VERIFY THE DATA RESULTS OF
: THE TEST. THIS PROCEDURE ALSO VERIFIES THE PROPER INCREMENTING OF THE
: REGISTER.
:
: *****
: TEST 43 TEST MODE 2 USING SOP INST.
: *****
: ST43: INC (R2) ; UPDATE TEST NUMBER
: CMP #43,(R2) ; SEQUENCE ERROR?
: BNE TST44-10 ; BR TO ERROR HALT ON SEQ ERROR
: CLR RO ; SET RO=400
: COMB RO
: INC RO
: CLR (RO) ; CLEAR 400
: COM (RO) ; INITIALIZE: 400=-1
: CLR (RO)+ ; TRY CLEARING WITH MODE 2
: BEQ SOPZA
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
: CONDITIONAL BRANCH INST. AND (====
: REPLACE THE MOVE INSTRUCTION (====
: WHICH FOLLOWS W/ 771 (====
:
: MOV #62,-(R2) ; MOVE TO MAILBOX # ***** 62 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; CLR INST DID NOT SET Z-BIT
:
: SOPZA: DEC RO ; RESET RO
: DEC RO
: COM (RO)+ ; TRY COMPLEMENTING WITH MODE 2
: BPL SOP2B
: DEC RO ; RESET RO
: DEC RO
: INC (RO)+ ; TRY INCREMENTING WITH MODE 2
: BEQ TST44
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
: CONDITIONAL BRANCH INST. AND (====
: REPLACE THE MOVE INSTRUCTION (====
: WHICH FOLLOWS W/ 755 (====
:
: SOP2B: MOV #63,-(R2) ; MOVE TO MAILBOX # ***** 63 *****
: INC -(R2) ; SET MSGTYP TO FATAL ERROR
: HALT ; CHECK CUMULATIVE RESULT OF ABOVE INST
: ; OR SEQUENCE ERROR
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003100 005212
003102 022712 000044
003106 001022
003110 005000
003112 105100
003114 005200
003116 005010
003120 005110
003122 105020
003124 001404

003126 012742 000064
003132 005242
003134 000000
003136 005300
003140 005210
003142 105420
003144 100003
003146 005300
003150 105220
003152 001404

003154
003154 012742 000065
003160 005242
003162 000000

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*****
: THIS TEST VERIFIES MODE 2 SINGLE OPERAND INSTRUCTIONS WHICH
: ADDRESS EVEN BYTES.  R0 IS SET TO 400 AND USED TO INITIALIZE LOCATION
: 400 TO -1.  CLRB INSTRUCTION IS THEN EXECUTED ON BYTE 400 WITH
: MODE 2.
: R0 IS THEN DECREMENTED BEFORE EACH OF SEVERAL MODE 2 INSTRUCTIONS
: WHICH ARE USED TO VERIFY THE DATA RESULTS OF THE TEST.  THIS PROCEDURE ALSO
: VERIFIES THE PROPER INCREMENTING OF THE REGISTER.
*****
: TEST 44          TEST MODE 2 EVEN BYTE USING SOP INST.
*****
TST44:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #44,(R2)     ;SEQUENCE ERROR?
        BNE     TST45-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0           ;SET R0=400
        COMB   R0
        INC    R0
        CLR    (R0)         ;CLEAR 400
        COM    (R0)         ;INITIALIZE: 400=-1
        CLRB  (R0)+        ;TRY TO CLEAT 400 W/MODE 2
        BEQ    SOPB2A
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
:          CONDITIONAL BRANCH INST. AND <====
:          REPLACE THE MOVE INSTRUCTION <====
:          WHICH FOLLOWS W/ 771 <====
        MOV     #64,-(R2)    ;MOVE TO MAILBOX # ***** 64 *****
        INC    -(R2)
        HALT
SOPB2A: DEC     R0          ;RESULT R0=400
        INC    (R0)
        NEGB  (R0)+
        BPL   SOPB2B
        DEC   R0           ;RESET R0=400
        INCB  (R0)+        ;TRY INCREMENT OF EVEN BYTE
        BEQ   TST45
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
:          CONDITIONAL BRANCH INST. AND <====
:          REPLACE THE MOVE INSTRUCTION <====
:          WHICH FOLLOWS W/ 756 <====
SOPB2B: MOV     #65,-(R2)    ;MOVE TO MAILBOX # ***** 65 *****
        INC    -(R2)
        HALT
: TEST CUMMULATIVE RESULT OF ABOVE INST.
: OR SEQUENCE ERROR
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003164 005212
003166 022712 000045
003172 001025
003174 005000
003176 105100
003200 005200
003202 005010
003204 005110
003206 005200
003210 105020
003212 001404

003214 012742 000066
003220 005242
003222 000000
003224 005300
003226 005300
003230 005220
003232 005300
003234 105420
003236 100003
003240 005300
003242 105220
003244 001404

003246 012742 000067
003246 005242
003252 000000
    
```

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*****
THIS TEST FOLLOWS THE SAME PROCEDURE DESCRIBED IN THE PREVIOUS
TEST.  HERE, THE BYTE INSTRUCTION IS USED TO ADDRESS AN ODD BYTE.
*****
TEST 45  TEST MODE 2 ODD BYTE USING SOP INST.
*****
ST45:  INC      (R2)          ;UPDATE TEST NUMBER
      CMP      #45,(R2)     ;SEQUENCE ERROR?
      SNE     TST46-1C     ;BR TO ERROR HALT ON SEQ ERROR.
      CLR     RO           ;SET RO=400
      COMB   RO
      INC     RO
      CLR     (RO)        ;CLEAR LOC 400
      COM     (RO)        ;INITIALIZE: 400=-1
      INC     RO          ;RO=ODD BYTE
      CLRB   (RO)+       ;TRY TO CLEAR ODD BYTE
      BEQ    SOPB2C
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ;          CONDITIONAL BRANCH INST. AND <====
      ;          REPLACE THE MOVE INSTRUCTION <====
      ;          WHICH FOLLOWS W/ 770 <====
      MOV     #66,-(R2)   ;MOVE TO MAILBOX # ***** 66 *****
      INC     -(R2)
      HALT
SOPB2C: DEC     RO
      DEC     RO
      INC     (RO)+       ;INCREMENT WORD
      DEC     RO          ;POINT TO ODD BYTE
      NEGB   (RO)+       ;TRY TO NEGATE ODD BYTE
      BPL    SOPB2D
      DEC     RO
      INCB   (RO)+       ;RESET RO TO ODD BYTE
      BEQ    TST46       ;TRY TO INCREMENT ODD BYTE
      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
      ;          CONDITIONAL BRANCH INST. AND <====
      ;          REPLACE THE MOVE INSTRUCTION <====
      ;          WHICH FOLLOWS W/ 753 <====
SOPB2D: MOV     #67,-(R2) ;MOVE TO MAILBOX # ***** 67 *****
      INC     -(R2)
      HALT
      ;SET MSGTYP TO FATAL ERROR
      ;TEST CUMMULATIVE RESULT OF ABOVE INST.
      ; OR SEQUENCE ERROR
    
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003256 005212
003260 022712 000046
003264 001020
003266 005000
003270 105100
003272 005200
003274 005010
003276 005030
003300 001404

003302 012742 000070
003306 005242
003310 000000
003312 005300
003314 005300
003316 005130
003320 100002
003322 005230
003324 001404

003326
003326 012742 000071
003332 005242
003334 000000

```
*****
: THIS TEST VERIFIES MODE 3 SINGLE OPERAND INSTRUCTIONS. IT
: USES LOCATION 0 AS ITS TARGET DATA. A TABLE LOCATED AT LOC. 400
: THRU 402 IS USED TO SUPPLY THE ADDRESS OF LOCATION 0 TO THE
: INSTRUCTIONS UNDER TEST.
: RO IS SET TO 400, THE START OF THE ADDRESS TABLE, AND A CLR
: INSTRUCTION IS EXECUTED WITH MODE 3 TO CLEAR LOC. 0. THEN RO
: IS DECREMENTED BY TWO AND TWO OTHER MODE 3 INSTRUCTIONS OPERATE ON
: LOC. 0 TO VERIFY THE DATA RESULTS OF THE TEST. THE PROPER INCREMENTING
: OF THE REGISTER IS ALSO VERIFIED IN THIS MANNER.
: IF A FAILURE IS DETECTED BE SURE TO VERIFY THAT THE TABLE
: (LOC. 400-402) HAS THE PROPER VALUES (0).
*****
: TEST 46 TEST MODE 3 USING SOP INST.
*****
TST46: INC (R2) ;UPDATE TEST NUMBER
CMP #46,(R2) ;SEQUENCE ERROR?
BNE TST47-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;SET RO=400
COMB RO
INC RO
CLR (RO) ;CLEAR LOC 400
CLR @ (RO)+ ;TRY TO CLEAR LOC 0 USING MODE 3
BEQ SOP3A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
MOV #70,-(R2) ;MOVE TO MAILBOX # ***** 70 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLR DID NOT SET Z-BIT
SOP3A: DEC RO ;RESET RO=400
DEC RO
COM @ (RO)+ ;TRY TO COMPLEMENT LOC 0 OF MODE 3
BPL SOP3B
INC @ (RO)+ ;TRY TO INCREMENT LOC 0 W/MODE 3
BEQ TST47
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 <====
SOP3B: MOV #71,-(R2) ;MOVE TO MAILBOX # ***** 71 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CUMMULATIVE RESULT OF ABOVE INST FAILED
; OR SEQUENCE ERROR
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003336 005212
003340 022712
003344 001026
003346 005004
003350 105104
003352 005204
003354 005000
003356 005010
003360 005110
003362 105034
003364 001404

003366 012742
003372 005242
003374 000000
003376 005304
003400 005304
003402 005234
003404 100006
003406 105434
003410 100004
003412 005304
003414 005304
003416 105234
003420 001404

003422 012742
003426 005242
003430 000000

000047

000072

000073

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*****
: THIS TEST VERIFIES MODE 3 SINGLE OPERAND BYTE INSTRUCTIONS
: WHICH ADDRESS EVEN BYTES. AGAIN, THE TARGET LOCATION 0 IS USED
: AND THE SAME TABLE AT 400 IS EMPLOYED.
: AFTER POINTING R4 TO THE TABLE (400) AND SETTING LOCATION
: 0 TO -1, A CLRB INSTRUCTION IS USED TO CLEAR BYTE 0.
: SEVERAL OTHER MODE 3 INSTRUCTIONS ARE THEN USED WITH THE TABLE
: TO VERIFY THE DATA RESULTS AND THE PROPER INCREMENTING OF THE REGISTER.
: IF A FAILURE IS DETECTED, BE SURE THAT THE TABLE (LOCATION 400-402) HAS
: THE PROPER VALUES (0).
*****
: TEST 47 TEST MODE 3 EVEN BYTE USING SOP INST.
*****
†ST47: INC (R2) ;UPDATE TEST NUMBER
CMP #47,(R2) ;SEQUENCE ERROR?
BNE TST50-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R4 ;SET R4=400
COMB R4
INC R4
CLR R0 ;INITIALIZE LOC. 0=-1
CLR (R0)
COM (R0)
CLRB @R4+ ;TRY TO CLEAR EVEN BYTE
BEQ SOPB3A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====
MOV #72,-(R2) ;MOVE TO MAILBOX # ***** 72 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLRB DID NOT SET Z-BIT
SOPB3A: DEC R4 ;RESET POINTER
DEC R4
INC @R4+ ;TRY INCREMENTING WORD
BPL SOPB3B
NEGB @R4+ ;TRY TO NEGATE EVEN BYTE
BPL SOPB3B
DEC R4
DEC R4
INCB @R4+ ;TRY TO INCREMENT EVEN BYTE
BEQ TST50
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 752 <====
SOPB3B: MOV #73,-(R2) ;MOVE TO MAILBOX # ***** 73 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CUMMULATIVE RESULT OF ABOVE INST FAILED
; OR SEQUENCE ERROR
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003432 005212
003434 022712 000050
003440 001024
003442 005000
003444 105100
003446 005200
003450 005030
003452 005130
003454 105030
003456 001404

003460 012742 000074
003464 005242
003466 000000
003470 005300
003472 005300
003474 005300
003476 005300
003500 005230
003502 105430
003504 100002
003506 10523C
003510 001404

003512
003512 012742 000075
003516 005242
003520 000000

```
*****
THIS TEST VERIFIES MODE 3 SINGLE OPERAND BYTE INSTRUCTIONS
WHICH ADDRESS ODD BYTES. THE TARGET IS BYTE 1. A TABLE AT
LOC. 400-406 IS USED. RO SERVES AS THE TABLE POINTER.
RO IS INITIALIZED TO 400. LOC. 0 IS SET TO -1 USING THE
FIRST TWO TABLE ENTRIES. A CLRB MODE 3 IS EXECUTED ON BYTE 1 USING
TABLE ADDRESS AT 404. RO IS DECREMENTED TO 402 AND SEVERAL SOP
MODE 3 INSTRUCTIONS ARE USED TO VERIFY DATA RESULTS AND PROPER
REGISTER INCREMENTING.
THE TABLE (400-406) SHOULD CONTAIN 0,0,1,1 BEFORE AND
AFTER THE TEST IS RUN.
*****
TEST 50 TEST MODE 3 ODD BYTE USING SOP INST.
*****
TST50: INC (R2) ;UPDATE TEST NUMBER
CMP #50,(R2) ;SEQUENCE ERROR?
BNE TST51-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;SET RO=400
COMB RO
INC RO
CLR @ (RO)+ ;INITIALIZE
COM @ (RO)+ ;LOC 0=-1 RO=404
CLRB @ (RO)+ ;TRY TO CLEAR ODD BYTE
BEQ SOPB3C
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 771
MOV #74,-(R2) ;MOVE TO MAILBOX # ***** 74 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLRB DID NOT SET Z-BIT
SOPB3C: DEC RO ;RESET RO
DEC RO
DEC RO ;POINT TO EVEN BYTE ADDR.
DEC RO
INC @ (RO)+ ;INCREMENT WORD
NEGB @ (RO)+ ;TRY TO NEGATE ODD BYTE
BPL SOPB3D
INCB @ (RO)+ ;TRY TO INCREMENT ODD BYTE
BEQ TST51
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 754
SOPB3D: MOV #75,-(R2) ;MOVE TO MAILBOX # ***** 75 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CUMMULATIVE RESULT OF ABOVE INSTS FAILED
; OR SEQUENCE ERROR
*****
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1827 003522 005212
1828 003524 022712 000051
1829 003530 001021
1830 003532 005000
1831 003534 105100
1832 003536 005200
1833 003540 005040
1834 003542 001404
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1839 003544 012742 000076
1840 003550 005242
1841 003552 000000
1842 003554 005200
1843 003556 005200
1844 003560 005140
1845 003562 100004
1846 003564 005200
1847 003566 005200
1848 003570 005240
1849 003572 001404
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1854 003574
1855 003574 012742 000077
1856 003600 005242
1857 003602 000000
1858

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;*****
;TEST 51 TEST MODE 4 USING SOP INSTS
;*****
TST51: INC (R2) ;UPDATE TEST NUMBER
CMP #51,(R2) ;SEQUENCE ERROR?
BNE TST52-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;SET RO=400
COMB RO
INC RO
CLR -(RO) ;TRY TO CLEAR USING MODE 4
BEQ SOP4A

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 773 <====

MOV #76,-(R2) ;MOVE TO MAILBOX # ***** 76 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLR DID NOT SET Z-BIT
SOP4A: INC RO ;RESET RO
INC RO
COM -(RO) ;TRY TO COMPLEMENT USING MODE 4
BPL SOP4B
INC RO ;MOVE POINTER
INC RO
INC -(RO)
BEQ TST52

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 757 <====

SOP4B: MOV #77,-(R2) ;MOVE TO MAILBOX # ***** 77 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CHECK CUMMULATIVE RESULT OF ABOVE INST.
; OR SEQUENCE ERROR

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003604 005212
003606 022712 000052
003612 001017
003614 005000
003616 005020
003620 105400
003622 005050
003624 001404

003626 012742 000100
003632 005242
003634 000000
003636 005200
003640 005200
003642 005150
003644 100002
003646 005250
003650 001404

003652
003652 012742 000101
003656 005242
003660 000000

```
*****
: THIS TEST VERIFIES MODE 5 SINGLE OPERAND INSTRUCTIONS. I-
: USES LOCATION 0 AS ITS TARGET DATA. A TABLE LOCATED AT LOC. 372
: THRU 374 IS USED TO SUPPLY THE ADDRESS OF LOCATION 0 TO THE
: INSTRUCTIONS UNDER TEST
: RO IS SET TO 376, (THE START OF THE ADDRESS TABLE) +2,
: AND A CLR INSTRUCTION IS EXECUTED WITH MODE 3 TO CLEAR
: LOC. 0. THEN RO IS INCREMENTED BY TWO AND TWO OTHER MODE 3
: INSTRUCTIONS OPERATE ON LOC. 0 TO VERIFY THE DATA RESULTS OF
: THE TEST. THE PROPER DECREMENTING OF THE REGISTER IS ALSO
: VERIFIED IN THIS MANNER.
: IF A FAILURE IS DETECTED BE SURE TO VERIFY THAT THE TABLE
: (LOC. 372 THRU 374) HAS THE PROPER VALUES (0).
*****
: TEST 52 TEST MODE 5 USING SOP INSTS
*****
: ST52: INC (R2) ;UPDATE TEST NUMBER
: CMP #52,(R2) ;SEQUENCE ERROR?
: BNE TST53-10 ;BR TO ERROR HALT ON SEQ ERROR
: CLR RO ;SET RO=376
: CLR (RO)+
: NEGB RO
: CLR @-(RO) ;TRY TO CLEAR LOC 0 W/MODE 5
: BEQ SOP5A
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 773 <====
: ; MOVE TO MAILBOX # ***** 100 *****
: ; SET MSGTYP TO FATAL ERROR
: ; CLR DID NOT SET Z-BIT
: ; RESET RO
: ; TRY TO COMPLEMENT LOC. 0 W/MODE 5
: ; TRY TO INCREMENT LOC. 0 W/MODE 5
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 761 <====
: ; MOVE TO MAILBOX # ***** 101 *****
: ; SET MSGTYP TO FATAL ERROR
: ; TEST CUMMULATIVE RESULT OF ABOVE INSTS
: ; OR SEQUENCE ERROR
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003662 005212
003664 022712 000053
003670 001020
003672 005000
003674 105100
003676 005200
003700 005060 177400
003704 001404

003706 012742 000102
003712 005242
003714 000000
003716 005160 177400
003722 100003
003724 005260 177400
003730 001404

003732
003732 012742 000103
003736 005242
003740 000000

```
*****
:
: THIS TEST VERIFIES MODE 6 SINGLE OPERAND INSTRUCTIONS. IT
: USES LOCATION 0 AS ITS TARGET DATA. RO IS SET TO 400 USING
: PREVIOUSLY TESTED INSTRUCTIONS AND A MODE 6 CLR INSTRUCTION IS
: EXECUTED ON LOC. 0 USING RO AND A -400 OFFSET. COM AND INC
: INSTRUCTIONS ARE THEN USED TO VERIFY THE DATA.
:
: *****
: TEST 53 TEST MODE 6 USING SOP INSTS
: *****
TST53: INC (R2) ;UPDATE TEST NUMBER
      CMP #53,(R2) ;SEQUENCE ERROR?
      BNE TST54-10 ;BR TO ERROR HALT ON SEQ ERROR
      CLR RO ;SET RO=400
      COMB RO
      INC RO
      CLR -400(RO) ;TRY TO CLEAR LOCATION 0 W/MODE 6
      BEQ SOP6A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====
      MOV #102,-(R2) ;MOVE TO MAILBOX # ***** 102 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;CLR DID NOT SET Z-BIT
SOP6A: COM -400(RO) ;TRY TO COMPLEMENT LOCATION 0 W/MODE 6
      BPL SOP6B
      INC -400(RO) ;TRY TO INCREMENT LOCATION 0 W/MODE 6
      BEQ TST54
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 <====
SOP6B: MOV #103,-(R2) ;MOVE TO MAILBOX # ***** 103 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;TEST CUMMULATIVE RESULT OF ABOVE INSTS
; OR SEQUENCE ERROR
;
```

```

*****
THIS TEST VERIFIES MODE 7 SINGLE OPERAND INSTRUCTIONS. IT USES
THE POINTER TO LOC. 0 WHICH IS STORED AT LOC. 402.
RD IS SET TO 400 AND A MODE 7 CLR INSTRUCTION IS
EXECUTED WITH A +2 OFFSET TO CLEAR LOC. 0.
SEVERAL OTHER MODE 7 INSTRUCTIONS ARE THEN USED ON THE COMMON
LOCATION TO VERIFY THE DATA RESULTS.
*****

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TEST 54 TEST MODE 7 USING SOP INST.

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003742 005212
003744 022712 000054
003750 001020
003752 005000
003754 105100
003756 005200
003760 005070 000002
003764 001404

012742 000104
005242
000000
005170 000002
100003
005270 000002
001404

004012
004012 012742 000105
004016 005242
004020 005000

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ST54: INC (R2) ;UPDATE TEST NUMBER
CMP #54,(R2) ;SEQUENCE ERROR?
BNE TST55-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RD ;SET RD=400
COMB RD
INC RD
CLR RD ;TRY TO CLEAR LOC. 0 W/MODE 7
BEQ SOP7A

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 772 <====

SOP7A: MOV #104, -(R2) ;MOVE TO MAILBOX # ***** 104 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLR DID NOT SET Z-BIT
COM #2,(RD) ;TRY TO COMPLEMENT LOC. 0 W/MODE 7
BPL SOP7B
INC #2,(RD) ;TRY TO INCREMENT LOC. 0 W/MODE 7
BEQ TST55

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 <====

SOP7B: MOV #105, -(R2) ;MOVE TO MAILBOX # ***** 105 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;TEST CUMMULATIVE RESULT OF ABOVE INSTS.
; OR SEQUENCE ERROR

```



```

1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001 004022 005212
2002 004024 022712 000055
2003 004030 001017
2004 004032 005027
2005 004034 177777
2006 004036 001404
2007
2008
2009
2010
2011 004040 012742 000106
2012 004044 005242
2013 004046 000000
2014 004050 005237 004034
2015 004054 005467 177754
2016 004060 100003
2017 004062 005277 000012
2018 004066 001405
2019
2020
2021
2022
2023 004070
2024 004070 012742 000107
2025 004074 005242
2026 004076 000000
2027
2028 004100 004034
    
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```

*****
: THIS TEST VERIFIES PROGRAM COUNTER ADDRESSING WITH SOP
: INSTRUCTIONS. CLR MODE 77 IS USED TO CLEAR THE LOCATION FOLLOWING THE
: INSTRUCTION (SOPX). THEN SINGLE OPERAND INSTRUCTIONS WITH MODES 37, 67, AND
: 77, USING INDIRECT POINTER SOPXAD ARE USED TO VERIFY THE DATA RESULTS
: OF THESE INSTRUCTIONS.
*****
: TEST 55 TEST SOP INSTRUCTIONS MODES 2,3,6,7 WITH REGISTER 7
*****
↑ST55: INC (R2) ;UPDATE TEST NUMBER
: CMP #55,(R2) ;SEQUENCE ERROR?
: BNE SOPB ;BR TO ERROR HALT ON SEQ ERROR
: CLR (R7)+ ;CLEAR NEXT LOCATION: (SOPX)
SOPX: -1 ;USE MODE 27
: BEQ SOPA
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 775 <====
: MOVE TO MAILBOX # ***** 106 *****
: SET MSGTYP TO FATAL ERROR
: CLR DID NOT SET Z-BIT
SOPA: INC @SOPX ;INC SOPX W/MODE 37
: NEG SOPX ;NEGATE SOPX W/MODE 67
: BPL SOPB
: INC SOPXAD ;INC SOPX W/MODE 77
: BEQ TST56
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 761 <====
SOPB: MOV #107,-(R2) ;MOVE TO MAILBOX # ***** 107 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;INC DID NOT SET Z-BIT
: OR SEQUENCE ERROR
SOPXAD: SOPX ;INDIRECT ADDRESS OF SOPX
    
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2058
2059
2060

004102 005212
004104 022712 000056
004110 001010
004112 005000
004114 000277
004116 000244
004120 005700
004122 102403
004124 100402
004126 103401
004130 001404

004132 012742 000110
004136 005242
004140 000000

: THIS TEST VERIFIES SINGLE OPERAND NON-MODIFYING INSTRUCTIONS
: USING MODE 0. R0 IS SET TO ZERO AND THE CONDITION CODES ARE SET
: TO THE COMPLEMENT OF THAT EXPECTED BY THE INSTRUCTION. A TST INSTRUCTION
: IS EXECUTED AND CONDITIONAL BRANCHES ARE USED TO TEST THE CONDITION
: CODES.

: TEST 56 TEST MODE 0 SOP NON-MODIFYING

*ST56: INC (R2) ; UPDATE TEST NUMBER
CMP #56,(R2) ; SEQUENCE ERROR?
BNE TST57-10 ; BR TO ERROR HALT ON SEQ ERROR
CLR R0 ; INITIALIZE R0=0
SCC ; SET CC=1011
CLZ
TST R0 ; TRY TST W/ MODE 0
BVS SNMOA ; CHECK THAT CC=0100
BMI SNMOA
BCS SNMOA
BEQ TST57

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 770 <====

SNMOA: MOV #110,-(R2) ; MOVE TO MAILBOX * ***** 110 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CONDITION CODES NOT SET PROPERLY
; OR SEQUENCE ERROR

2061
2062
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2090
2091
2092

004142 005212
004144 022712 000057
004150 001010
004152 005000
004154 105100
004156 000277
004160 000250
004152 105700
004164 102402
004166 101401
004170 100404

004172 012742 000111
004176 005242
004200 000000

```
*****
: THIS TEST VERIFIES SINGLE OPERAND NON-MODIFYING BYTE INSTRUCTIONS WITH MODE L
: RO IS SET TO 377 AND COMPLEMENT OF THE EXPECTED CONDITION CODES
: IS LOADED IN PSW. A TSTB INSTRUCTION IS EXECUTED AND THE RESULTS
: ARE CHECKED WITH SEVERAL CONDITIONAL BRANCH INSTRUCTIONS.
: THIS VERIFIES THAT THE PROPER BYTE WAS TESTED.
*****
: TEST 57 TEST MODE 0 EVEN BYTE W/ SOP NON-MODIFYING
*****
†ST57: INC (R2) ;UPDATE TEST NUMBER
CMP #57,(R2) ;SEQUENCE ERROR?
BNE TST60-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RC ;INITIALIZE
COMB RO ;RO=377
SCC ;SET CC=0111
CLN
TSTB RO ;TRY TST EVEN BYTE
BVS SNMBOA ;CHECK CC=1000
BLOS SNMBOA
BMI TST60
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====
SNMBOA: MOV #111,-(R2) ;MOVE TO MAILBOX # ***** 111 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CONDITION CODES NOT SET PROPERLY
; OR SEQUENCE ERROR
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2097
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2100
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2103
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2105
2106
2107
2108
2109
2110
2111
2112
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2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125

004202 005212
004204 022712 000060
004210 001011
004212 005000
004214 005010
004216 000277
004220 000244
004222 005710
004224 102403
004226 103402
004230 100401
004232 001404

004234 012742 000112
004234 005242
004242 000000

```
*****
THIS TEST VERIFIES SINGLE OPERAND INSTRUCTIONS WITH MODE 1.
RO IS USED TO POINT TO AND CLEAR LOC. 0. THE COMPLEMENT OF THE
EXPECTED CONDITION CODES ARE LOADED IN THE PSW. A TST INSTRUCTION
IS THEN EXECUTED ON LOC. 0 USING RO AND CONDITIONAL BRANCHES TEST
THE RESULTS.
*****
TEST 60 TEST MODE 1 SOP NON-MODIFYING
*****
TST60: INC (R2) ;UPDATE TEST NUMBER
CMP #60,(R2) ;SEQUENCE ERROR?
BNE TST61-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;POINT TO LOC 0
CLR (RO) ;CLEAR LOC 0
SCC ;INITIALIZE
CLZ ;CC=1011
TST (RO) ;TRY TST W/ MODE 1
BVS SNM1A ;CHECK CC=0100
BCS SNM1A
BMI SNM1A
BEQ TST61

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 767 (====

SNM1A: MOV #112,-(R2) ;MOVE TO MAILBOX # ***** 112 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CC'S NOT SET PROPERLY
; OR SEQUENCE ERROR
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2126
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2161
2162
2163
2164
2165
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2167
2168
2169
2170
2171
2172
2173
2174

004244 005212
004246 C22712
004252 001026
004254 005000
004256 005010
004260 105110
004262 000277
004264 000250
004266 105710
004270 102402
004272 101401
004274 100404

004276
004276 012742
004302 005242
004304 000000
004306 005000
004310 005200
004312 000277
004314 000244
004316 105710
004320 102403
004322 103402
004324 100401
004326 001404

004330
004330 012742
004334 005242
004336 000000

000061

000113

000114

```
*****
:
: THIS TEST SETS LOCATION 0 TO 377 AND THEN USES R0 TO TEST
: THE EVEN BYTE AND THE ODD BYTE USING SOP BYTE INSTRUCTIONS WITH MODE 1.
: AGAIN, CONDITIONAL BRANCHES ARE USED TO VERIFY THE SETTING OF THE
: PROPER CONDITION CODE BITS.
:
: *****
: TEST 61 TEST MODE 1 BYTE INST. NON-MODIFYING
: *****
TST61: INC (R2) ; UPDATE TEST NUMBER
CMP #61,(R2) ; SEQUENCE ERROR?
BNE TST62-10 ; BR TO ERROR HALT ON SEQ ERROR
CLR R0 ; POINT TO LOC 0
CLR (R0) ; CLEAR LOC 0
COMB (R0) ; COMPLEMENT BYTE 0
SCC ; SET CC=0111
CLN
TSTB (R0) ; TRY TST ON EVEN BYTE
BVS SNMB1A
BLOS SNMB1A
BMI SNMB1B
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====
SNMB1A: MOV #113,-(R2) ; MOVE TO MAILBOX # ***** 113 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CC'S NOT CORRECT
SNMB1B: CLR R0
INC R0
; SET CC=1011
CLZ
TSTB (R0) ; TRY TO TST AN ODD BYTE
BVS SNMB1C
BCS SNMB1C
BMI SNMB1C
BEQ TST62
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 752 <====
SNMB1C: MOV #114,-(R2) ; MOVE TO MAILBOX # ***** 114 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CC'S NOT CORRECT
; OR SEQUENCE ERROR
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2175
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2178
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2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216

004340 005212
004342 022712 000062
004346 001020
004350 005000
004352 005010
004354 000277
004356 000244
004360 005720
004362 102403
004364 103402
004366 100401
004370 001404

004372
004376 012742 000115
004400 000000
004402 005300
004404 005300
004406 001404

004410 012742 000116
004414 005242
004416 000000

```
*****
: THIS TEST VERIFIES THE SINGLE-OPERAND NON-MODIFYING INSTRUCTIONS
: USING MODE 2. IT USES THE IDENTICAL PROCEDURE EMPLOYED IN THE
: MODE 1 TESTS. ADDITIONALLY, THE REGISTER IS CHECKED TO ASSURE THAT
: IT IS INCREMENTED PROPERLY.
*****
: TEST 62 TEST MODE 2 WITH SOP NON-MODIFYING
*****
: ST62: INC (R2) ;UPDATE TEST NUMBER
: CMP #62,(R2) ;SEQUENCE ERROR?
: BNE TST63-10 ;BR TO ERROR HALT ON SEQ ERROR
: CLR RO ;INITIALIZE RO=0
: CLR (RO) ;CLEAR LOC 0
: SCC ;SET CC=1011
: CLZ
: TST (RO)+ ;TRY TST W/ MODE 2
: BVS SNM2A ;CHECK CC=0100
: BCS SNM2A
: BMI SNM2A
: BEQ SNM2B
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
: CONDITIONAL BRANCH INST. AND (====
: REPLACE THE MOVE INSTRUCTION (====
: WHICH FOLLOWS W/ 767 (====
: SNM2A: MOV #115,-(R2) ;MOVE TO MAILBOX # ***** 115 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;CC'S NOT CORRECT
: SNM2B: DEC RO ;RESET RO
: DEC RO
: BEQ TST63
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
: CONDITIONAL BRANCH INST. AND (====
: REPLACE THE MOVE INSTRUCTION (====
: WHICH FOLLOWS W/ 760 (====
: SNM2A: MOV #116,-(R2) ;MOVE TO MAILBOX # ***** 116 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;MODE 2 DID NOT INC REQ CORRECTLY
: OR SEQUENCE ERROR
```

2217
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2222
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2234
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2236
2237
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2240
2241
2242
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2244
2245
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2249
2250
2251
2252
2253
2254
2255
2256
2257
2258
2259
2260
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2264
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2269
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2271
2272

004420 005212
004422 022712 000063
004426 001742
004430 005000
004432 005010
004434 105110
004436 000277
004440 000250
004442 105720
004444 102402
004446 101401
004450 100404

004452 012742 000117
004456 005242
004460 000000
004462 005300
004464 001404

004466 012742 000120
004472 005242
004474 000000
004476 005200
004500 000277
004502 000244
004504 105720
004506 102403
004510 103402
004512 100401
004514 001404

004516 012742 000121
004522 005242

```

*****
THIS TEST VERIFIES MODE 2 SINGLE OPERAND NON-MODIFYING BYTE
INSTRUCTIONS IT USES R0 TO POINT TO LOC. 0. WITH LOCATION 0
SET TO 377, THE EVEN AND ODD BYTE IS TESTED WITH TSTB INSTRUCTIONS
TO VERIFY THE CORRECT CC ARE SET. THE REGISTER IS CHECKED FOR
PROPER INCREMENTING.
*****
TEST 63          TEST MODE 2 - BYTE W/ SOP NON-MODIFYING
*****
TST63:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #63,(R2)     ;SEQUENCE ERROR?
        BNE     TST64-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0           ;CLEAR R0
        CLR     (R0)         ;CLEAR LOC 0
        COMB   (R0)         ;SET LOC 0=377
        SCC     ;           ;SET CC=0111
        CLN
        TSTB   (R0)+        ;TRY TST OF EVEN BYTE
        BVS    SNMB2A
        BLOS   SNMB2A
        BMI    SNMB2B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===
; CONDITIONAL BRANCH INST. AND <===
; REPLACE THE MOVE INSTRUCTION <===
; WHICH FOLLOWS W/ 767 <===

SNMB2A:  MOV     #117, -(R2)   ;MOVE TO MAILBOX # ***** 117 *****
        INC     -(R2)
        HALT
SNMB2B:  DEC     R0           ;SET MSGTYP TO FATAL ERROR
        BEQ    SNMB2C        ;CC'S NOT SET CORRECTLY
        ;       ;DECREMENT R0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===
; CONDITIONAL BRANCH INST. AND <===
; REPLACE THE MOVE INSTRUCTION <===
; WHICH FOLLOWS W/ 761 <===

SNMB2C:  MOV     #120, -(R2)  ;MOVE TO MAILBOX # ***** 120 *****
        INC     -(R2)
        HALT
        INC     R0           ;SET MSGTYP TO FATAL ERROR
        SCC     ;           ;MODE 2 DID NOT INC REG CORRECTLY
        CLZ
        TSTB   (R0)+        ;POINT TO ODD BYTE
        BVS    SNMB2D        ;SET CC=1011
        BCS    SNMB2D
        BMI    SNMB2D
        BEQ    SNMB2E

; TRY TST OF ODD BYTE
; CHECK CC'S=0100

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===
; CONDITI. AL BRANCH INST. AND <===
; REPLACE THE MOVE INSTRUCTION <===
; WHICH FOLLOWS W/ 745 <===

SNMB2D:  MOV     #121, -(R2)  ;MOVE TO MAILBOX # ***** 121 *****
        INC     -(R2)
        ;       ;SET MSGTYP TO FATAL ERROR
    
```

J04

2273 004524 000000
2274 004526 005300
2275 004530 005300
2276 004532 001404
2277
2278
2279
2280
2281 004534 012742 000122
2282 004540 005242
2283 004542 000000
2284

SNMB2E: HALT
DEC R0
DEC R0
BEG TST64

MOV #122, -(R2)
INC -(R2)
HALT

;CC'S NOT CORRECT

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 736
; MOVE TO MAILBOX # ***** 122 *****
; SET MSGTYP TO FATAL ERROR
; RD DID NOT INCREMENT PROPERLY
; OR SEQUENCE ERROR


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2285
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2296 004544 005212
2297 004546 022712 000064
2298 004552 001022
2299 004554 005000
2300 004556 005010
2301 004560 105100
2302 004562 005300
2303 004564 000277
2304 004566 000244
2305 004570 005730
2306 004572 102403
2307 004574 103402
2308 004576 100401
2309 004600 001404
2310
2311
2312
2313
2314 004602
2315 004602 012742 000123
2316 004606 005242
2317 004610 000000
2318 004612 005300
2319 004614 105100
2320 004616 001404
2321
2322
2323
2324
2325 004620 012742 000124
2326 004624 005242
2327 004626 000000
2328

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```

*****
: THIS TEST VERIFIES MODE 3 SINGLE OPERAND NON-MODIFYING INSTRUCTIONS.
: A POINTER IN A TABLE AT LOC. 376 IS USED TO TEST LOCATION 0.
: THE CC'S AND THE REGISTER ARE CHECKED FOLLOWING THE
: TST MODE 3 INSTRUCTION.
*****
: TEST 64 TEST MODE 3 W/ SOP NON-MODIFYING INSTS
*****
TST64: INC (R2) ;UPDATE TEST NUMBER
CMP #64,(R2) ;SEQUENCE ERROR?
BNE TST65-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;RO=0
CLR (RO) ;CLEAR LOC 0
COMB RO ;RO=376
DEC RO
SCC ;SET CC=1011
CLZ
TST 2(RO)+ ;TRY TST W/ MODE 3
BVS SNM3A ;CHECK CC=0100
BCS SNM3A
BMI SNM3A
BEQ SNM3B

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 765 <====

SNM3A: MOV #123,-(R2) ;MOVE TO MAILBOX # ***** 123 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CC'S NOT CORRECT

SNM3B: DEC RO ;RO=377
COMB RO ;RO=0
BEQ TST65

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 756 <====

MOV #124,-(R2) ;MOVE TO MAILBOX # ***** 124 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;MODE 3 DID NOT INC REG CORRECTLY
; OR SEQUENCE ERROR

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004630 005212
004632 022712 000065
004636 001036
004640 005000
004642 005010
004644 105110
004646 105100
004650 005200
004652 005720
004654 000277
004656 000250
004660 105730
004662 102402
004664 101401
004666 100404

004670
004670 012742 000125
004674 005242
004676 000000
004700 000277
004702 000244
004704 105730
004706 102403
004710 103402
004712 100401
004714 001404

004716
004716 012742 000126
004722 005242
004724 000000
004726 005720
004730 005710
004732 100404

```
*****
: THIS TEST VERIFIES SOP NON-MODIFYING BYTE INSTRUCTIONS MODE 3
: LOC. 0 IS SET TO 377. TABLE AT LOC. 402-404 IS USED TO TEST
: BYTE 0 AND BYTE 1. THE REGISTER IS CHECKED FOR PROPER INCREMENTING AND
: THE CC'S ARE VERIFIED.
: THE TABLE AT LOC. 402-404 SHOULD CONTAIN 0 AND 1 BEFORE AND
: AFTER THE TEST IS RUN.
*****
: TEST 65 TEST MODE 3 - BYTES W/ SOP NON-MODIFYING INSTS.
*****
TST65: INC (R2) ; UPDATE TEST NUMBER
CMP #65,(R2) ; SEQUENCE ERROR?
BNE TST66-10 ; BR TO ERROR HALT ON SEQ ERROR
CLR RO ; RO=0
CLR (RO) ; CLEAR LOC 0
COMB (RO) ; LOC. 0 =377
COMB RO
INC RO
TST (RO)+ ; RO=402
SCC ; CC=0111
CLN
TSTB @ (RO)+ ; TRY TST OF EVEN BYTE
BVS SNMB3A ; CHECK CC=1000
BLOS SNMB3A
BMI SNMB3B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 764 <====

SNMB3A: MOV #125,-(R2) ; MOVE TO MAILBOX # ***** 125 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CC'S NOT CORRECT
SNMB3B: SCC ; SET CC=1011
CLZ
TSTB @ (RO)+ ; TRY TST OF ODD BYTE
BVS SNMB3C ; CHECK CC=0100
BCS SNMB3C
BMI SNMB3C
BEQ SNMB3D

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 751 <====

SNMB3C: MOV #126,-(R2) ; MOVE TO MAILBOX # ***** 126 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CC'S NOT CORRECT
SNMB3D: TST (RO)+ ; RO=410
TST (RO)
BMI TST66

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
```

```

2385
2386
2387 004734 012742 000127      MOV      #127, -(R2)      ; REPLACE THE MOVE INSTRUCTION <====
2388 004740 005242      INC      -(R2)          ; WHICH FOLLOWS W/ 742 <====
2389 004742 000000      HALT                    ; MOVE TO MAILBOX # ***** 127 *****
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2402 004744 005212      INC      (R2)           ; UPDATE TEST NUMBER
2403 004746 022712 000066      CMP      #66, (R2)      ; SEQUENCE ERROR?
2404 004752 001017      BNE      TST67-10       ; BR TO ERROR HALT ON SEQ ERROR
2405 004754 005000      CLR      RO             ; RO=0
2406 004756 005010      CLR      (RO)           ; LOC 0=0
2407 004760 005120      COM      (RO)+          ; LOC 0=-1
2408 004762 000277      SCC                    ; SET CC=1011
2409 004764 000244      CLZ
2410 004766 005740      TST      -(RO)          ; TRY TST W/ MODE 4
2411 004770 102402      BVS      SNM4A          ; CHECK CC=0100
2412 004772 101401      BLOS     SNM4A
2413 004774 100404      BMI      SNM4B
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2418 004776
2419 004776 012742 000130      SNM4A: MOV      #130, -(R2)    ; MOVE TO MAILBOX # ***** 130 *****
2420 005002 005242      INC      -(R2)          ; SET MSGTYP TO FATAL ERROR
2421 005004 000000      HALT                    ; CC'S NOT CORRECT
2422 005006 005700      SNM4B: TST      RO
2423 005010 001404      BEQ      TST67
2424
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2428 005012 012742 000131      MOV      #131, -(R2)    ; MOVE TO MAILBOX # ***** 131 *****
2429 005016 005242      INC      -(R2)          ; SET MSGTYP TO FATAL ERROR
2430 005020 000000      HALT                    ; TST MODE 4 DID NOT DEC RO CORRECTLY
2431

```

THIS TEST VERIFIES MODE 4 SOP NON-MODIFYING INSTRUCTIONS.
LOC. 0 IS SET TO -1 AND THE CC'S ARE SET TO THE COMPLEMENT OF THE
EXPECTED RESULTS. RO AND SET TO 2 AND A TST MODE 4 IS EXECUTED.
THE CC'S ARE CHECKED WITH CONDITIONAL BRANCH INSTRUCTIONS AND THE REGISTER
IS CHECKED FOR PROPER DECREMENTING.

TEST 66 TEST MODE 4 W/ SOP NON-MODIFYING INSTS

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
CONDITIONAL BRANCH INST. AND <====
REPLACE THE MOVE INSTRUCTION <====
WHICH FOLLOWS W/ 767 <====

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
CONDITIONAL BRANCH INST. AND <====
REPLACE THE MOVE INSTRUCTION <====
WHICH FOLLOWS W/ 761 <====

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005022 005212
005024 022712 000067
005030 001022
005032 005000
005034 005010
005036 005110
005040 105100
005042 005200
005044 000277
005046 000250
005050 005750
005052 102402
005054 101401
005056 100404

005060
005060 012742 000132
005064 005242
005066 000000
005070 005200
005072 105100
005074 001404

005076 012742 000133
005102 005242
005104 000000

```
*****
THIS TEST VERIFIES MODE 5 SOP NON-MODIFYING INSTRUCTIONS.
IT USES A POINTER AT LOC. 376 TO TEST LOC. 0. RO IS SET
TO 400. A TST MODE 5 INSTRUCTION IS EXECUTED AND THE CC'S CHECKED.
RO IS CHECKED TO INSURE PROPER DECREMENTING.
*****
TEST 67 TEST MODE 5 W/ SOP NON-MODIFYING INSTS
*****
TST67: INC (R2) ;UPDATE TEST NUMBER
CMP #67,(R2) ;SEQUENCE ERROR?
BNE TST70-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;RO=0
CLR (RO) ;LOC 0=0
COM (RO) ;LOC 0=-1
COMB RO ;RO=377
INC RO ;RO=400
SCC ;SET CC=0111
CLN
TST 2-(RO) ;TRY TST W/ MODE 5
BVS SNMSA ;CHECK CC=1000
BLOS SNMSA
BMI SNMSB

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 765 (====

SNMSA: MOV #132,-(R2) ;MOVE TO MAILBOX # ***** 132 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CC'S NOT SET PROPERLY
SNMSB: INC RO ;RO=377
COMB RO ;RO=0
BEQ TST70

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 756 (====

MOV #133,-(R2) ;MOVE TO MAILBOX # ***** 133 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;MODE 5 DID NOT DEC RO CORRECTLY
; OR SEQUENCE ERROR
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TEST MODE 6 W

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THIS TEST VERIFIES MODE 7 SOP NON-MODIFYING INSTRUCTIONS.
IT USES A POINTER TO LOC. 0 STORED AT LOC. 400 TO TST LOC. 0.
RO IS SET TO 377 AND LOC. 0 IS TESTED THRU THE POINTER AT 400 USING
RO AND AN OFFSET OF 1.

TEST 71 TEST MODE 7 W/ SOP NON-MODIFYING INSTS.

005170 005212
005172 022712 000071
005176 001021
005200 005000
005202 005010
005204 005110
005206 105100
005210 000277
005212 000250
005214 005770 000001
005220 102402
005222 101401
005224 100404

TST71: INC (R2) ;UPDATE TEST NUMBER
CMP #71,(R2) ;SEQUENCE ERROR?
BNE TST72-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR RO ;RO=0
CLR (RO) ;LOC 0=0
COM (RO) ;LOC 0=-1
COMB RO ;RO=377
SCC ;CC=0111
CLN
TST 21(RO) ;TRY TST W/ MODE 7
BVS SNM7A ;CHECK CC=1000
BLOS SNM7A
BMI SNM7B

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 765 <====

005226
005226 012742 000136
005232 005242
005234 000000
005236 105100
005240 001404

SNM7A: MOV #136,-(R2) ;MOVE TO MAILBOX # ***** 136 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CC'S NOT CORRECT
SNM7B: COMB RO ;RO=0
SEQ TST72

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 757 <====

005242 012742 000137
005246 005242
005250 000000

MOV #137,-(R2) ;MOVE TO MAILBOX # ***** 137 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;TST MODE 7 INCORRECTLY CHANGED RC
; OR SEQUENCE ERROR

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005252 005212
005254 022712 000072
005260 001006
005262 005000
005264 005100
005266 005004
005270 060004
005272 005204
005274 001404

005276 012742 000140
005302 005242
005304 000000

005306 005212
005310 022712 000073
005314 001006
005316 005000
005320 005004
005322 005100
005324 010004
005326 005204
005330 001404

005332 012742 000141
005336 005242
005340 000000

```
*****
THIS TEST VERIFIES MODE 0 DOUBLE OPERAND INSTRUCTIONS. IT SETS
DATA IN R0 AND R4 AND USES THE ADD INSTRUCTION TO TEST THE DCP
MICROCODE.
*****
TEST 72      TEST MODE 0 DOUBLE-OPERAND (DOP) INSTS.
*****
ST72:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #72,(R2)     ;SEQUENCE ERROR?
        BNE     TST73-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0           ;R0=0
        COM     R0           ;R0=-1
        CLR     R4           ;R4=0
        ADD     R0,R4        ;TRY ADD: R4=-1
        INC     R4           ;R4=0
        BEQ     TST73
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
;         CONDITIONAL BRANCH INST. AND  <====
;         REPLACE THE MOVE INSTRUCTION  <====
;         WHICH FOLLOWS W/ 772         <====
        MOV     #140,-(R2)    ;MOVE TO MAILBOX # ***** 140 *****
        INC     -(R2)
        HALT
; SET MSGTYP TO FATAL ERROR
; ADD INST. FAILED W/ MODE 0
; OR SEQUENCE ERROR
*****
THIS TEST VERIFIES THE MOVE INSTRUCTION WITH MODE 0 TO MODE 0.
THIS TEST IS NECESSARY BECAUSE THIS PARTICULAR INSTRUCTION UTILIZES UNIQUE
MICROCODE.
*****
TEST 73      MOV MODE 0 TO MODE 0
*****
ST73:  INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #73,(R2)     ;SEQUENCE ERROR?
        BNE     TST74-10     ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0           ;R0=0
        CLR     R4           ;R4=0
        COM     R0           ;R0=-1
        MOV     R0,R4        ;TRY MOVE -1 TO R4
        INC     R4           ;INC R4
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
;         CONDITIONAL BRANCH INST. AND  <====
;         REPLACE THE MOVE INSTRUCTION  <====
;         WHICH FOLLOWS W/ 772         <====
        MOV     #141,-(R2)    ;MOVE TO MAILBOX # ***** 141 *****
        INC     -(R2)
        HALT
; SET MSGTYP TO FATAL ERROR
; MOVE FAILED MODE 0 TO MODE 0
; OR SEQUENCE ERROR
*****
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005342 005212
005344 022712 000074
005350 001051
005352 005000
005354 010004
005356 001404

005360 012742 000142
005364 005242
005366 000000
005370 005200
005372 005100
005374 005104
005376 040004
005400 005304
005402 001404

005404 012742 000143
005410 005242
005412 000000
005414 050004
005416 005204
005420 005204
005422 001404

005424 012742 000144
005430 005242
005432 000000
005434 005000
005436 105100
005440 005004
005442 005104
005444 040004
005446 060004
005450 005204

```
*****
THIS TEST QUICKLY VERIFIES THE REMAINING DOP MODIFYING INSTRUCTIONS
WITH MODE 0 TO PROVIDE A BASELINE FOR SUBSEQUENT TESTS.
SINGLE OPERAND INSTRUCTIONS ARE USED TO SET UP DATA IN R0 AND R4
BEFORE EACH OF THE SEVERAL DOP MODIFYING INSTRUCTIONS ARE USED AND
VERIFIED.
*****
TEST 74 TEST ALL THE DOP INSTRUCTIONS W/ SOURCE MODE 0
*****
ST74: INC (R2) ;UPDATE TEST NUMBER
CMP #74,(R2) ;SEQUENCE ERROR?
BNE TST75-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R0 ;R0=0
MOV R0,R4 ;TRY MOVE MODE 0,0
BEQ DOP0A

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 775 <====

MOV #142,-(R2) ;MOVE TO MAILBOX # ***** 142 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;Z-BIT NOT SET
DOP0A: INC R0 ;R0=1
COM R0 ;R0=177776
COM R4 ;R4=177777
BIC R0,R4 ;TRY BIC: R4=1
DEC R4 ;R4=0
BEQ DOP0B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 763 <====

MOV #143,-(R2) ;MOVE TO MAILBOX # ***** 143 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;BIC CLEAR RESULT INCORRECT
DOP0B: BIS R0,R4 ;TRY BIS: R4=177777
INC R4 ;R4=0
INC R4 ;R4=0
BEQ DOP0C

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 753 <====

MOV #144,-(R2) ;MOVE TO MAILBOX # ***** 144 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;RESULT OF BIS INCORRECT
DOP0C: CLR R0 ;R0=0
COMB R0 ;R0=377
CLR R4 ;R4=0
COM R4 ;R4=177777
COM R4 ;R4=177400
BIC R0,R4 ;TRY ADD: R4=177777
ADD R0,R4 ;R4=0
INC R4
```


2670	005452	001404	
2671			
2672			
2673			
2674			
2675	005454	012742	000145
2676	005460	005242	
2677	005462	000000	
2678	005464	160004	
2679	005466	105404	
2680	005470	005204	
2681	005472	001404	
2682			
2683			
2684			
2685			
2686	005474	012742	000146
2687	005500	005242	
2688	005502	000000	
2689			

	BEQ	DOP0D	
	MOV	#145 -(R2)	
	INC	-(R2)	
	HALT		
DOP0D:	SUB	R0,R4	
	NEGB	R4	
	INC	R4	
	BEQ	TST75	

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 737
;=====
; MOVE TO MAILBOX # ***** 145 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF ADD INCORRECT
; 177401=R4
; R4=177777
; RD=0

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 727
;=====
; MOVE TO MAILBOX # ***** 146 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF SUB INCORRECT
; OR SEQUENCE ERROR

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005504 005212
005506 022712 000075
005512 001042
005514 005000
005516 005004
005520 005204
005522 020400
005524 003004

005526 012742 000147
005532 005242
005534 000000
005536 020004
005540 002404

005542 012742 000150
005546 005242
005550 000000
005552 005200
005554 020400
005556 001404

005560 012742 000151
005564 005242
005566 000000
005570 005000
005572 005100
005574 005004
005576 030004
005600 001404

005602 012742 000152
005606 005242
005610 000000

```
*****
: THIS TEST VERIFIES MODE 0 DOP NON-MODIFYING INSTRUCTIONS.
: R0 AND R4 ARE PRESET TO 0 AND 1 RESPECTIVELY. COMPARE INSTRUCTIONS ARE
: THEN EXECUTED AND CHECKED. FIRST R4 IS COMPARED TO R0 THEN R0 TO R4.
*****
: TEST 75 TEST DOP NON-MODIFYING INST. W/ SOURCE MODE 0
*****
: ST75: INC (R2) ; UPDATE TEST NUMBER
: CMP #75,(R2) ; SEQUENCE ERROR?
: BNE TST76-10 ; BR TO ERROR HALT ON SEQ ERROR
: CLR R0 ; R0=0
: CLR R4 ; R4=0
: INC R4 ; R4=1
: CMP R4,R0 ; TRY COMPARE R4 TO R0
: BGT DNM1
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 773 <====
: MOVE TO MAILBOX # ***** 147 *****
: SET MSGTYP TO FATAL ERROR
: CC'S NOT CORRECT FOR CMP
: TRY COMPARE R0 TO R4
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 765 <====
: MOVE TO MAILBOX # ***** 150 *****
: SET MSGTYP TO FATAL ERROR
: CC'S NOT CORRECT FOR CMP
: R4=0
: TRY COMPARE R4=1 TO R0=1
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 756 <====
: MOVE TO MAILBOX # ***** 151 *****
: SET MSGTYP TO FATAL ERROR
: CC'S NOT CORRECT (Z=1) FOR CMP
: R0=0
: R0=177777
: R4=0
: TRY BIT R0 TO R4
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 745 <====
: MOVE TO MAILBOX # ***** 152 *****
: SET MSGTYP TO FATAL ERROR
: CC'S NOT CORRECT FOR BIT
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2746 005612 005304          ONM4:  D&C      R4          ;R4=177777
2747 005614 030004          BIT      RD,R4    ;TRY BIT AGAIN
2748 005616 100404          BMI      TST76
2749          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
2750          ;          CONDITIONAL BRANCH INST. AND <====
2751          ;          REPLACE THE MOVE INSTRUCTION <====
2752          ;          WHICH FOLLOWS W/ 736 <====
2753 005620 0.2742 000153    MOV      #153,-(R2) ;MOVE TO MAILBOX # ***** 153 *****
2754 005624 005242          INC      -(R2)     ;SET MSGTYP TO FATAL ERROR
2755 005626 000000          HALT          ;CC'S NOT CORRECT FOR BIT
2756          ;          OR SEQUENCE ERROR
2757
2758 :*****
2759 :
2760 :          THIS TEST VERIFIES MODE 1 DOP INSTRUCTIONS.  RD IS SET TO -1
2761 :AND LOC 0 TO 1.  R4 IS THEN CLEARED AND USED TO POINT TO LOC 0.
2762 :IN THE ADD MODE 1 INSTRUCTION, LOC 0 IS ADDED TO RD AND THE
2763 :RESULTS VERIFIED.
2764 :
2765 :*****
2766 :TEST 76          TEST MODE 1 W/ DOP INST.
2767 :*****
2768 005630 005212          ST76:  INC      (R2)          ;UPDATE TEST NUMBER
2769 005632 022712 000076    CMP      #76,(R2)    ;SEQUENCE ERROR?
2770 005636 001007          BNE     TST77-10    ;BR TO ERROR HALT ON SEQ ERRCR
2771 005640 005000          CLR     RD          ;RD=0
2772 005642 005100          COM     RD          ;RD=177777
2773 005644 005004          CLR     R4          ;R4=0
2774 005646 005014          CLR     (R4)        ;LOC 0=0
2775 005650 005214          INC     (R4)        ;LOC 0=1
2776 005652 061400          ADD     (R4),RD     ;TRY ADD SOURCE MODE 1
2777 005654 001404          BEQ     TST77
2778          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
2779          ;          CONDITIONAL BRANCH INST. AND <====
2780          ;          REPLACE THE MOVE INSTRUCTION <====
2781          ;          WHICH FOLLOWS W/ 771 <====
2782 005656 012742 000154    MOV      #154,-(R2) ;MOVE TO MAILBOX # ***** 154 *****
2783 005662 005242          INC     -(R2)     ;SET MSGTYP TO FATAL ERROR
2784 005664 000000          HALT          ;RESULT OF ADD INCORRECT
2785          ;          OR SEQUENCE ERROR

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2796 005666 005212
2797 005670 022712 000077
2798 005674 001007
2799 005676 005000
2800 005700 005010
2801 005702 005110
2802 005704 005004
2803 005706 151004
2804 005710 105104
2805 005712 001404
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2810 005714 012742 000155
2811 005720 005242
2812 005722 000000
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*****
: THIS TEST VERIFIES MODE 1 DOP BYTE INSTRUCTIONS WHICH ADDRESS
: EVEN BYTES. LOC. 0 IS SET TO -1 AND R4 IS CLEARED. THEN R4 IS
: SET TO -1 USING A BISB THRU R0 WITH MODE 1.
*****
: TEST 77 TEST MODE 1 - EVEN BYTE W/ DOP INSTS.
*****
TST77: INC (R2) ;UPDATE TEST NUMBER
CMP #77,(R2) ;SEQUENCE ERROR?
SNE TST100-10 ;BR TO ERROR HALT ON SEQ ERROR
CLR R0 ;R0=0
CLR (R0) ;LOC. 0=0
COM (R0) ;LOC. 0=177777
CLR R4 ;R4=0
BISB (R0),R4 ;TRY MODE 1- EVEN BYTE W/ DOP
CCMB R4 ;R4=0
BEQ TST100

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====
; MOVE TO MAILBOX # ***** 155 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF BISB IS INCORRECT
; OR SEQUENCE ERROR

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2825 005724 005212
2826 005726 022712 000100
2827 005732 001007
2828 005734 005000
2829 005736 005010
2830 005740 005110
2831 005742 005004
2832 005744 105104
2833 005746 121004
2834 005750 001404
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2839 005752 012742 000156
2840 005756 005242
2841 005760 000000
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:*****
:
:   THIS TEST VERIFIES MODE 1 DOP NON-MODIFYING INSTRUCTIONS
: WHICH ADDRESS EVEN BYTES.  LOC. 0 IS SET TO -1 AND R0 IS CLEARED
: AND USED AS THE ADDRESSING REGISTER.  R4 IS SET TO 377 AND A
: MODE 1,0 CMPB INSTRUCTION IS USED THE RESULTS VERIFIED.
:*****
:TEST 100      TEST MODE 1 - EVEN BYTE W/ DOP NON-MODIFYING INST.
:*****
TST100: INC      (R2)          ;UPDATE TEST NUMBER
        CMP      #100,(R2)   ;SEQUENCE ERROR?
        BNE     TST101-10   ;BR TO ERROR HALT ON SEQ ERROR
        CLR     R0          ;R0=0
        CLR     (R0)        ;LOC 0=0
        COM     (R0)        ;LOC 0=177777
        CLR     R4          ;R4=0
        COMB    R4          ;R4=377
        CMPB   (R0),R4     ;TRY MODE 1 - EVEN BYTE W/ DOP NON-MODIFYING
        BEQ     TST101
:
:   TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
:             CONDITIONAL BRANCH INST. AND <====
:             REPLACE THE MOVE INSTRUCTION <====
:             WHICH FOLLOWS W/ 771 <====
:MOVE TO MAILBOX # ***** 156 *****
:SET MSGTYP TO FATAL ERROR
:RESULT OF CMPB INCORRECT
: OR SEQUENCE ERROR

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005762 005212
005764 022712 000101
005770 001020
005772 005000
005774 005010
005776 105110
006000 005110
006002 005004
006004 005104
006006 111004
006010 005704
006012 001404

006014 012742 000157
006020 005242
006022 000000
006024 005110
006026 111004
006030 100404

006032 012742 000160
006036 005242
006040 000000

```
*****
: THIS TEST VERIFIES MODE 1,0 MOVB INSTRUCTIONS
: WHICH ADDRESS EVEN BYTES. LOC. 0 IS SET TO 177400, R0 IS CLEARED AND
: R4 IS SET TO -1. MOVB ARE USED TO MOVE BYTE 0 TO R4. THIS
: VERIFIES THAT THE PROPER BYTE WAS SELECTED AND THAT THE SIGN-X-TEND
: FUNCTION WITH MODE 0.
: THEN LOC. 0 IS COMPLEMENTED AND THE SAME PROCEDURE EXERCISES
: THE LOGIC FOR COMPLEMENTARY DATA.
: THIS TEST EXERCISES UNIQUE MICROCODE.
*****
: TEST 101 TEST MOV INSTRUCTION MODE 1,0 EVEN BYTE
*****
TST101: INC (R2) ;UPDATE TEST NUMBER
: CMP #101,(R2) ;SEQUENCE ERROR?
: BNE TST102-10 ;BR TO ERROR HALT ON SEQ ERROR
: CLR R0 ;R0=0
: CLR (R0) ;LOC 0=0
: COMB (R0) ;LOC 0=177400
: COM (R0)
: CLR R4 ;R4=0
: COM R4 ;R4=177777
: MOVB (R0),R4 ;R4=0
: TST R4 ;CHECK SIGN OF WORD
: BEQ DOP1
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 767 <====
: MOV #157,-(R2) ;MOVE TO MAILBOX # ***** 157 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;MOVB SHOULD SIGN X-TEND
DOP1: COM (R0) ;LOC 0=177777
: MOVB (R0),R4 ;DO MOVB W/ EVEN BYTE
: BMI TST102
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 760 <====
: MOV #160,-(R2) ;MOVE TO MAILBOX # ***** 160 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;MOVB SHOULD SIGN X-TEND
: OR SEQUENCE ERROR
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2899 006042 005212
2900 006044 022712 0001C2
2901 006050 001010
2902 006052 005000
2903 006054 005010
2904 006056 005004
2905 006060 005204
2906 006062 105114
2907 006064 151410
2908 006066 005210
2909 006070 001404
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2914 006072 012742 000161
2915 006076 005242
2916 006100 000000
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*****
: THIS TEST VERIFIES MODE 1 DOP INSTRUCTIONS WHICH REFERENCE
: ODD BYTES. LOC. 0 IS SET TO 177400. R0 IS SET TO 0 AND R4 IS
: SET TO 1. THE BISB INSTRUCTION USES THE DATA IN BYTE 1 TO SET BYTE 0.
: THE RESULT IS CHECKED BY INCREMENTING THE WORD (LOC. 0) TO ZERO.
*****
: TEST 102 TEST MODE 1-ODD BYTE W/ DOP INSTS.
*****
†ST102: INC (R2) ; UPDATE TEST NUMBER
CMP #102,(R2) ; SEQUENCE ERROR?
BNE TST103-10 ; BR TO ERROR HALT ON SEQ ERROR
CLR R0 ; R0=0
CLR (R0) ; LOC. 0=0
CLR R4 ; R4=0
INC R4 ; R4=1
COMB (R4) ; LOC. 0=177400
BISB (R4),(R0) ; TRY TO BIS LOW ORDER BITS W/ MODE 1
INC (R0) ; CHECK RESULT
BEQ TST103

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <== =
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W' 770 <====
; MOVE TO MAILBOX # ***** 161 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF BISB INCORRECT
; OR SEQUENCE ERROR

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006102 005212
006104 022712 000103
006110 001015
006112 005000
006114 005010
006116 005110
006120 012004
006122 005204
006124 001404

006126 012742 000162
006132 005242
006134 000000
006136 005300
006140 005300
006142 001404

006144 012742 000163
006150 005242
006152 000000

TST103: INC (R2)
CMP #103,(R2)
BNE TST104-10
CLR RO
CLR (RO)
COM (RO)
MOV (RO)+,R4
INC R4
BEQ DOP2

DOP2: RO
DEC RO
BEQ TST104

MOV #162,-(R2)
INC -(R2)
HALT
RO
DEC RO
BEQ TST104

MOV #163,-(R2)
INC -(R2)
HALT

: THIS TEST VERIFIES MODE 2 DOP INSTRUCTIONS. LOC. 0 IS SET TO -1.
: RO IS CLEARED AND USED AS THE MODE 2 ADDRESSING REGISTER TO MOVE LOC. 0
: TO R7. THE DATA RESULTS ARE VERIFIED AND THE INCREMENTING OF THE REGISTER
: IS CHECKED.

: TEST 103 TEST MODE 2 W/ DOP INSTS.

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 772 <====
: MOVE TO MAILBOX # ***** 162 *****
: SET MSGTYP TO FATAL ERROR
: RESULT OF MOV INST INCORRECT
: TEST RO AFTER MODE 2

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 763 <====
: MOVE TO MAILBOX # ***** 163 *****
: SET MSGTYP TO FATAL ERROR
: REGISTER NOT INCREMENTED IN MODE 2
: OR SEQUENCE ERROR


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2969 006154 005212
2970 006156 022712 000104
2971 006162 001016
2972 006164 005000
2973 006166 010010
2974 006170 005110
2975 006172 142010
2976 006174 105737 000001
2977 006200 001404
2978
2979
2980
2981
2982 006202 012742 000164
2983 006206 005242
2984 006210 000000
2985 006212 105137 000000
2986 006216 001404
2987
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2989
2990
2991 006220 012742 000165
2992 006224 005242
2993 006226 000000
2994

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*****
: THIS TEST VERIFIES MODE 2 DOP BYTE INSTRUCTIONS WHICH ADDRESS
: EVEN BYTES. LOC. 0 IS SET TO -1. RO IS CLEARED AND USED AS THE
: ADDRESSING REGISTER IN A TEST WHICH TRIES TO CLEAR BYTE 1 USING
: BYTE 0 DATA AND A BICB. UNIQUE IN THIS TEST IS USE OF THE
: SAME ADDRESSING REGISTER FOR BOTH SOURCE AND DESTINATION. THE SOURCE AND
: DESTINATION IS CHECKED TO INSURE PROPER FUNCTIONING.
*****
: TEST 104 TEST MODE 2 - EVEN BYTE W/ DOP INST.
*****
TST104: INC (R2) ;UPDATE TEST NUMBER
: CMP #104,(R2) ;SEQUENCE ERROR?
: BNE TST105-10 ;BR TO ERROR HALT ON SEQ ERROR
: CLR RO ;RO=0
: MOV RO,(RO) ;LOC. 0=0
: COM (RO) ;LOC. 0=177777
: BICB (RO)+,(RO) ;TRY TO CLEAR BYTE 1 FROM BYTE 0 W/ BICB
: TSTB @#1 ;CHECK RESULT
: BEQ DOPB2A
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 771 <====
: MOVE TO MAILBOX # ***** 164 *****
: SET MSGTYP TO FATAL ERROR
: BICB DESTINATION INCORRECT
: DOPB2A: COMB @#0 ;CHECK BICB SOURCE
: BEQ TST105
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 762 <====
: MOVE TO MAILBOX # ***** 165 *****
: SET MSGTYP TO FATAL ERROR
: BICB SOURCE INCORRECTLY CHANGED
: OR SEQUENCE ERROR

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2995
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006230 005212
006232 022712 000105
006236 001017
006240 005000
006242 005004
006244 005010
006246 005110
006250 105120
006252 112004
006254 005204
006256 001404

012742 000166
006264 005242
006266 000000
006270 005740
006272 005700
006274 001404

012742 000167
006302 005242
006304 000000

THIS TEST VERIFIES MODE 2 DOP BYTE INSTRUCTIONS WHICH REFERENCE
ODD BYTES. R0 IS SET TO 1, LOC. 0 IS SET TO 177400, AND R4 IS CLEARED.
A MODE 2 MOV B USES R0 TO MOVE BYTE 1 TO R4. AN INCREMENT
IS USED TO CHECK THAT THE PROPER BYTE WAS MOVED AND SIGN X-TENDED.

TEST 105 TEST MODE 2 - ODD BYTE W/ DOP INST.

ST105: INC (R2) ; UPDATE TEST NUMBER
CMP #105, (R2) ; SEQUENCE ERROR?
BNE TST106-10 ; BR TO ERROR HALT ON SEQ ERROR
CLR R0 ; R0=0
CLR R4 ; R4=0
CLR (R0) ; LOC. 0=0
COM (R0) ; LOC. 0=177777
COMB (R0)+ ; LOC 0=177400; R0=1
MOVB (R0)+, R4 ; TRY DOP MODE 2 W/ ODD BYTE
INC R4 ; CHECK RESULT OF MOV B
BEQ DOPB2B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 770 <====
; MOVE TO MAILBOX # ***** 166 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF MOV B INCORRECT
DOPB2B: TST -(R0) ; BUMP R0 DOWN BY 2
TST R0 ; CHECK R0
BEQ TST106

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 761 <====
; MOVE TO MAILBOX # ***** 167 *****
; SET MSGTYP TO FATAL ERROR
; MODE 2 BYTE DID NOT INCREMENT REG. CORRECTLY
; OR SEQUENCE ERROR

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006306 005212
006310 022712 000106
006314 001011
006316 012737 052525 000000
006324 012700 125252
006330 053700 000000
006334 005200
006336 001404

006340 012742 000170
006344 005242
006346 000000

006350 005212
006352 022712 000107
006356 001011
006360 012737 052652 000000
006366 005000
006370 153700 000000
006374 022700 000252
006400 001404

006402 012742 000171
006406 005242
006410 000000

: THIS TEST VERIFIES MODE 3 DOUBLE-OPERAND INSTRUCTIONS.
: LOC. 0 IS LOADED WITH ALTERNATING ZEROES AND ONES; AND RO IS LOADED
: WITH ALTERNATING ONES AND ZEROES. A MODE 3 BIS IS USED TO SET RO
: TO -1 BY USING LOC. 0 AS THE SOURCE TO BIS THE ZEROES IN RO. THE
: RESULT IS TESTED BY INCREMENTING RO AND CHECKING FOR ZERO.

: TEST 106 TEST MODE 3 W/ DOP INSTS.

↑ST106: INC (R2) ; UPDATE TEST NUMBER
CMP #106, (R2) ; SEQUENCE ERROR?
BNE TST107-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #052525, @#0 ; MOVE 52525 TO LOC. 0
MOV #125252, RO ; SET ALT. ONE AND ZERO IN RO
BIS @#0, RO ; TRY TO SET ALL OTHER BITS W/ MODE 3
INC RO ; TEST RESULT
BEQ TST107

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 767 <====
MOV #170, -(R2) ; MOVE TO MAILBOX # ***** 170 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; BIS W/ MODE 3 INCORRECT RESULT
; OR SEQUENCE ERROR

: THIS TEST VERIFIES MODE 3 DOUBLE OPERAND BYTE INSTRUCTIONS WHICH
: ADDRESS EVEN BYTES. BYTE 0 IS SET TO ALTERNATING 1'S AND 0'S; BYTE 1,
: ALTERNATING 0'S AND 1'S. RO IS CLEARED AND A BISB IS USED TO
: SET THE LOW BYTE OF RO TO 252.

: TEST 107 TEST MODE 3 - EVEN BYTE W/ DOP INSTS.

↑ST107: INC (R2) ; UPDATE TEST NUMBER
CMP #107, (R2) ; SEQUENCE ERROR?
BNE TST110-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #52652, @#0 ; MOVE 1'S AND 0' PATTERN TO LOC. 0
CLR RO ; RO=0
BISB @#0, RO ; TRY RO=252 W/ MODE 3 - EVEN BYTE
CMP #252, RO ; BISB W/ EVEN BYTE SUCCESSFUL?
BEQ TST110

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 767 <====
MOV #171, -(R2) ; MOVE TO MAILBOX # ***** 171 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; BISB W/ MODE 3 - EVEN BYTE FAILED
; OR SEQUENCE ERROR

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3141
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3143
3144

006412 005212
006414 022712 000110
006420 001011
006422 012737 052652 000000
006430 005000
006432 153700 000001
006436 022700 000125
006442 001404

006444 012742 000172
006450 005242
006452 000000

005212 000111
001015
006536
006536
006536
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006536
001411

THIS TEST VERIFIES MODE 3 DOUBLE OPERAND BYTE INSTRUCTIONS
WHICH ADDRESS ODD BYTES. THE SAME PROCEDURE USED IN PREVIOUS
TEST IS USED HERE. THIS TIME BYTE 1 IS USED AS THE SOURCE BYTE.
THE EXPECTED RESULT IS: RO = 125.

TEST 110 TEST MODE 3 - ODD BYTE W/ DOP INSTS.

TST110: INC (R2) ; UPDATE TEST NUMBER
CMP #110, (R2) ; SEQUENCE ERROR?
BNE TST111-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #52652, @#0 ; MOVE 1'S AND 0'S PATTERN TO LOC 0
CLR RO ; RO=0
BISB @#1, RO ; TRY RO=152 W/ MODE 3 - ODD BYTE
CMP #125, RO ; RO=125?
BEQ TST111

; TO SCOPE. CLEAR THE RIGHT BYTE OF THIS /====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====
MOV #172, -(R2) ; MOVE TO MAILBOX # ***** 172 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; BISB W/ MODE 3 - ODD BYTE FAILED
; OR SEQUENCE ERROR

THIS TEST VERIFIES MODE 4 DOUBLE OPERAND INSTRUCTIONS.
THE TEST USES MODE 4 ADDRESSING WITH REGISTER 0 TO MOVE THRU A
TABLE OF OPERANDS. THE TABLE OF OPERANDS AND THE WORK LOCATION IS
STORED FOLLOWING THE TEST CODE. A SERIES OF 5 DOP INSTRUCTIONS UTILIZES
THE DATA IN THE TABLE TO CYCLE THE WORK LOCATION THRU A SET OF
VALUE. THE DATA HAS BEEN CHOSEN TO INSURE THAT NO SINGLE ERROR WILL
GO UNDETECTED. WORD AND BYTE INSTRUCTION ACCESSING BOTH EVEN AND
ODD ADDRESSES ARE USED IN THE TEST. THE LISTING SHOWS THE
EXPECTED INTERMEDIATE RESULT AS EACH INSTRUCTION IS EXECUTED.

TEST 111 TEST MODE 4 W/ DOP INSTS.

TST111: INC (R2) ; UPDATE TEST NUMBER
CMP #111, (R2) ; SEQUENCE ERROR?
BNE DOP4 ; BR TO ERROR HALT ON SEQ ERROR
MOV #TBL1, RO ; INITIALIZE RO
MOV -(RO), @#TBL1 ; TBL1=125252
ADD -(RO), @#TBL1 ; TBL1=000377
BICB -(RO), @#TBL1 ; TBL1=000252
BISB -(RO), @#TBL1+1 ; TBL1=125252
CMP -(RO), @#TBL1 ; CHECK RESULT
BEQ TST112

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====

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006516
006516 012742 000173
006522 005242
006524 000000

006526 125252
006530 052652
006532 053125
006534 125252
006536 000000

TBL1: 0

THIS TEST VERIFIES MODE 5 DOUBLE OPERAND INSTRUCTIONS.
THE TEST USES AN ADDRESS TABLE STORED FOLLOWING THE TEST CODE.
THIS TABLE IS SIMPLY A TABLE OF ADDRESS POINTERS WHICH ADDRESS
THE DATA TABLE USED IN THE PREVIOUS TEST. THE TEST IS IDENTICAL TO
THE PREVIOUS TEST EXCEPT THE DATA IS REFERENCED USING THIS ADDRESS
TABLE AND MODE 5 ADDRESSING. (SEE PREVIOUS TEST).

TEST 112 TEST MODE 5 W/ DOP INSTS.

TST112: INC (R2) ; UPDATE TEST NUMBER
CMP #112, (R2) ; SEQUENCE ERROR?
BNE DOP5 ; BR TO ERROR HALT ON SEQ ERROR
MOV #TBL2+2, R0 ; INITIALIZE R0
MOV @-(R0), @#TBL1 ; TBL1=125252
ADD @-(R0), @#TBL1 ; TBL1=000377
BICB @-(R0), @#TBL1 ; TBL1=000252
BISB @-(R0), @#TBL1+1 ; TBL1=125252
CMP @-(R0), @#TBL1 ; CHECK RESULT
BEQ TST113

DOP5:
MOV #174, -(R2)
INC -(R2)
HALT

TBL1-10
TBL1-6
TBL1-5
TBL1-4
TBL2: TBL1-2

WHICH FOLLOWS W/ 763
; MOVE TO MAILBOX # ***** 173 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF MODE 4 INSTS. INCORRECT
; OR SEQUENCE ERROR

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 763 <====
; MOVE TO MAILBOX # ***** 174 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF MODE 5 INSTS. INCORRECT
; OR SEQUENCE ERROR

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3249

006624 005212
006626 022712 000113
006632 001022
006634 012700 006532
006640 016037 000002 006536
006646 066037 000000 006536
006654 146037 177777 006536
006662 156037 177776 006537
006670 026037 177774 006536
006676 001404

006700 012742 000175
006704 005242
006706 000000

THIS TEST VERIFIES MODE 6 DOUBLE OPERAND INSTRUCTIONS.
IT USES THE SAME DATA AS THAT USED IN THE MODE 4 TESTS.
THIS TIME THE DATA IS ACCESSED USING MODE 6. RO IS SET
TO POINT TO THE MIDDLE OF THE TABLE. THE TABLE IS ACCESSED FROM
BOTTOM TO TOP BY VARYING THE OFFSET IN THE MODE 6 INSTRUCTIONS.
THE DATA RESULTS ARE IDENTICAL TO THOSE EXPECTED IN THE MODE 4
TESTS.

TEST 113 TEST MODE 6 W/ DOP INSTS.

TST113: INC (R2) ; UPDATE TEST NUMBER
CMP #113 (R2) ; SEQUENCE ERROR?
BNE TST114-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #TBL1-4,RO ; INITIALIZE RO
MOV 2(RO),@#TBL1 ; TBL1=125252
ADD 0(RO),@#TBL1 ; TBL1=000377
BICB -1(RO),@#TBL1 ; TBL1=000252
BISB -2(RO),@#TBL1+1 ; TBL1=125252
CMP -4(RO),@#TBL1 ; CHECK RESULT
BEQ TST114

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
CONDITIONAL BRANCH INST. AND <====
REPLACE THE MOVE INSTRUCTION <====
WHICH FOLLOWS W/ 756 <====
MOVE TO MAILBOX # ***** 175 *****
SET MSGTYP TO FATAL ERROR
RESULT OF MODE 6 INSTS. INCORRECT
OR SEQUENCE ERROR

THIS TEST VERIFIES MODE 7 DOUBLE OPERAND INSTRUCTIONS.
THIS TEST USES THE SAME ADDRESS TABLE AND DATA TABLE USED BY
THE MODE 5 TESTS. THIS TIME THE DATA IS ACCESSED USING MODE 7.
RO IS SET TO POINT TO THE MIDDLE OF THE ADDRESS TABLE IN THE MODE 5
TEST. THE TABLE IS ACCESSED FROM BOTTOM TO TOP BY VARYING THE OFFSET
IN THE MODE 7 INSTRUCTIONS. THE DATA RESULTS ARE IDENTICAL TO
THOSE EXPECTED IN THE MODE 5 TESTS.

TEST 114 TEST MODE 7 W/ DOP INSTS.

TST114: INC (R2) ; UPDATE TEST NUMBER
CMP #114 (R2) ; SEQUENCE ERROR?
BNE TST115-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #TBL2-4,RO ; INITIALIZE RO
MOV @4(RO),@#TBL1 ; TBL1=125252
ADD @2(RO),@#TBL1 ; TBL1=000377
BICB @0(RO),@#TBL1 ; TBL1=000252
BISB @-2(RO),@#TBL1+1 ; TBL1=125252
CMP @-4(RO),@#TBL1 ; CHECK RESULT
BEQ TST115

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3250 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3251 ; CONDITIONAL BRANCH INST. AND <====
3252 ; REPLACE THE MOVE INSTRUCTION <====
3253 ; WHICH FOLLOWS W/ 756 <====
3254 006764 012742 000176 MOV #176, -(R2) ; MOVE TO MAILBOX # ***** 176 *****
3255 006770 005242 INC -(R2) ; SET MSGTYP TO FATAL ERROR
3256 006772 000000 HALT ; RESULT OF MODE 7 INSTS INCORRECT
; OR SEQUENCE ERROR
3258
3259 *****
3260
3261 THIS TEST VERIFIES THE ROTATE MODE 0 INSTRUCTIONS.
3262 ; RO IS LOADED WITH A DATA PATTERN, THE C-BIT IS LOADED, AND
3263 ; AN ROL INSTRUCTION IS EXECUTED WITH MODE 0. THE OPERATION IS CHECKED
3264 ; BY TESTING THE RESULTING DATA AND THE STATE OF THE C AND V BITS.
3265 ; NEXT, THE SAME PROCEDURE IS EXECUTED TO TEST MODE 0 BYTE INSTRUCTIONS.
3266
3267 *****
3268 ; TEST 115 TEST ROTATE INSTRUCTIONS OF MODE 0
3269 ; *****
3270 006774 005212 ST115: INC (R2) ; UPDATE TEST NUMBER
3271 006776 022712 000115 CMP #115, (R2) ; SEQUENCE ERROR?
3272 007002 001026 BNE TST116-10 ; BR TO ERROR HALT ON SEQ ERROR
3273 007004 012700 125252 MOV #125252, RO ; INITIALIZE DATA
3274 007010 000261 SEC ; SET C-BIT
3275 007012 006100 ROL RO ; TRY ROL W/ MODE 0
3276 007014 102004 BVC ROTOA ; CC=0011
3277 007016 103003 BCC ROTOA
3278 007020 022700 052525 CMP #052525, RO ; CHECK DATA
3279 007024 001404 BEQ ROTOB
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====
3284 ROTOA: MOV #177, -(R2) ; MOVE TO MAILBOX # ***** 177 *****
3285 007026 012742 000177 INC -(R2) ; SET MSGTYP TO FATAL ERROR
3286 007032 005242 HALT ; ROL MODE 0 FAILED
3287 007034 000000 ROTOB: MOV #125252, RO ; INITIALIZE DATA
3288 007036 012700 125252 SEC ; SET C-BIT
3289 007042 000261 ROLB RO ; TRY ROL W/ MODE 0 EVEN BYTE
3290 007044 106100 BVC ROTOC ; CC=0011
3291 007046 102004 BCC ROTOC
3292 007050 103003 BCC ROTOC
3293 007052 022700 125125 CMP #125125, RO ; CHECK DATA
3294 007056 001404 BEQ TST116
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 752 <====
3298 ROTOC: MOV #200, -(R2) ; MOVE TO MAILBOX # ***** 200 *****
3299 007060 012742 000200 INC -(R2) ; SET MSGTYP TO FATAL ERROR
3300 007060 005242 HALT ; ROLB MODE 0 FAILED
3301 007064 005242 ; OR SEQUENCE ERROR
3302 007066 000000
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3317 007070 005212
3318 007072 022712 000116
3319 007076 001051
3320 007100 005000
3321 007102 012710 052525
3322 007106 000241
3323 007110 006110
3324 007112 102005
3325 007114 103404
3326 007116 023727 000000 125252
3327 007124 001404
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3332 007126
3333 007126 012742 000201
3334 007132 005242
3335 007134 000000
3336 007136 000261
3337 007140 012710 125252
3338 007144 106110
3339 007146 102005
3340 007150 103004
3341 007152 022737 125125 000000
3342 007160 001404
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3345
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3347 007162
3348 007162 012742 000202
3349 007166 005242
3350 007170 000000
3351 007172 012710 125252
3352 007176 005000
3353 007200 005200
3354 007202 000261
3355 007204 106110
3356 007206 102005
3357 007210 103004
3358 007212 022737 052652 000000
3359 007220 001404

```

*****
: THIS TEST VERIFIES THE ROTATE MODE 1 INSTRUCTIONS.
: THE DATA TO BE ROTATED IS IN LOC 0. R0 IS USED AS THE
: ADDRESSING REGISTER. THE C-BIT IS LOADED AND AN ROL IS EXECUTED.
: THE RESULTS ARE CHECKED BY COMPARING THE DATA RESULTS AND TESTING
: THE C AND V BITS. THIS PROCEDURE IS THEN REPEATED TWICE MORE
: TO TEST THE BYTE ROTATES. FIRST ON BYTE 0, THEN ON BYTE 1.
*****
: TEST 116 TEST ROTATE INSTRUCTIONS W/ MODE 1
*****
TST116: INC (R2) ;UPDATE TEST NUMBER
        CMP #116,(R2) ;SEQUENCE ERROR?
        BNE TST117-10 ;BR TO ERROR HALT ON SEQ ERROR
        CLR R0 ;POINT TO LOC. 0
        MOV #52525,(R0) ;INITIALIZE DATA
        CLC ;CLEAR C-BIT
        ROL (R0) ;TRY ROL W/ MODE 1
        BVC ROT1A ;CC=1010
        BCS ROT1A
        CMP #0,#125252 ;CHECK RESULT
        BEQ ROT1B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====

ROT1A: MOV #201,-(R2) ;MOVE TO MAILBOX # ***** 201 *****
        INC -(R2) ;SET MSGTYP TO FATAL ERROR
        HALT ;ROL MODE 1 FAILED

ROT1B: SEC
        MOV #125252,(R0) ;INITIALIZE DATA
        ROLB (R0) ;TRY ROLB W/ MODE 1 EVEN BYTE
        BVC ROT1C ;CC=1011
        BCC ROT1C
        CMP #125125,#0 ;TEST RESULT
        BEQ ROT1D

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 747 <====

ROT1C: MOV #202,-(R2) ;MOVE TO MAILBOX # ***** 202 *****
        INC -(R2) ;SET MSGTYP TO FATAL ERROR
        HALT ;ROLB W/ MODE 1 EVEN BYTE FAILED

ROT1D: MOV #125252,(R0)
        CLR R0 ;POINT TO ODD BYTE
        INC R0
        SEC ;SET C-BIT
        ROLB (R0) ;TRY ROLB W/ MODE 1 ODD BYTE
        BVC ROT1E ;CC=0011
        BCC ROT1E
        CMP #052652,#0 ;CHECK DATA
        BEQ TST117

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TEST ROTATE INSTRUCTIONS W/ MODE 1

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007222 012742 000203
007222 005242
007226 005242
007230 000000

007232 005212
007234 022712 000117
007240 001057
007242 005000
007244 012710 173737
007250 000241
007252 006120
007254 103007
007256 022737 167676 000000
007264 001003
007266 005300
007270 005300
007272 001404

007274
007274 012742 000204
007300 005242
007302 000000
007304 005000
007306 012710 004040
007312 000241
007314 106120
007316 103406
007320 022737 004100 000000
007326 001002
007330 005300
007332 001404

007334
007334 012742 000205

ROT1E:
MOV #203, -(R2)
INC -(R2)
HALT

TST117: INC (R2)
CMP #117, (R2)
BNE TST120-10
CLR R0
MOV #173737, (R0)
CLC
ROL (R0)+
BCC ROT2A
CMP #167676, @#0
BNE ROT2A
DEC R0
DEC R0
BEQ ROT2B

ROT2A:
MOV #204, -(R2)
INC -(R2)
HALT

ROT2B:
CLR R0
MOV #4040, (R0)
CLC
ROLB (R0)+
BCS ROT2C
CMP #4100, @#0
BNE ROT2C
DEC R0
BEQ ROT2D

ROT2C:
MOV #205, -(R2)

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 727 <====

: MOVE TO MAILBOX # ***** 203 *****
: SET MSGTYP TO FATAL ERROR
: ROLB W/ MODE 1 ODD BYTE FAILED
: OR SEQUENCE ERROR

: *****
: THIS TEST VERIFIES MODE 2 ROTATE INSTRUCTIONS.
: THE SAME PROCEDURE AS IN THE OTHER ROTATE TESTS ARE USED. R0
: IS USED AS THE ADDRESSING REGISTER AND IS CHECKED FOR PPOPER
: INCREMENTING. BYTE INSTRUCTIONS ARE ALSO CHECKED.
: *****
: TEST 117 TEST ROTATE INSTRUCTIONS W/ MODE 2
: *****
: UPDATE TEST NUMBER
: SEQUENCE ERROR?
: BR TO ERROR HALT ON SEQ ERROR
: POINT TO LOC 0
: INITIALIZE DATA
: CLEAR C-BIT
: TRY ROL W/ MODE 2
: CHECK C-BIT
: CHECK DATA
: BRANCH IF RESULT INCORRECT
: TEST R0

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 763 <====

: MOVE TO MAILBOX # ***** 204 *****
: SET MSGTYP TO FATAL ERROR
: ROL W/ MODE 2 FAILED
: POINT TO LOC 0
: INITIALIZE DATA
: CLEAR C-BIT
: TRY ROLB W/ MODE 2 EVEN BYTE
: CHECK C-BIT
: CHECK DATA
: BRANCH IF DATA INCORRECT
: CHECK R0

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 743 <====

: MOVE TO MAILBOX # ***** 205 *****

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007410 005212
007412 022712 000120
007416 001051
007420 012737 052525 000000
007426 000261
007430 006137 000000
007434 103404
007436 022737 125253 000000
007444 001404

007446
007446 012742 000207
007452 005242
007454 000000
007456 012737 125252 000000
007464 000241
007466 106137 000000
007472 103004
007474 023727 000000 125124
007502 001404

007504
007504 012742 000210
007510 005242
007512 000000
007514 012737 125252 000000
007522 000261
007524 106137 000001
007530 103004
007532 022737 052652 000000
007540 001404

007542
007542 012742 000211
007546 005242
007550 000000

```
*****
THIS TEST VERIFIES MODE 3 ROTATE INSTRUCTIONS.
THIS TEST USES THE SAME PROCEDURES AS IN THE OTHER ROTATE
TESTS. THE DATA IS STORED IN LOC. 0 AND IS ADDRESSED USING
MODE 37. BYTE ADDRESSING IS ALSO CHECKED FOR EVEN AND ODD BYTES.
*****
TEST 120 TEST ROTATE INSTRUCTIONS /W MODE 3
*****
TST120: INC (R2) ;UPDATE TEST NUMBER
CMP #120,(R2) ;SEQUENCE ERROR?
BNE TST121-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #52525,a#0 ;INITIALIZE DATA IN LOC 0
SEC ;SET C-BIT
ROL a#0 ;TRO ROL W/ MODE 3
BCS ROT3A ;CHECK C-BIT
CMP #125253,a#0 ;CHECK DATA
BEQ ROT3B

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====

ROT3A: MOV #207,-(R2) ;MOVE TO MAILBOX # ***** 207 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;ROL W/ MODE 3 FAILED
ROT3B: MOV #125252,a#0 ;INITIALIZE DATA
CLC ;CLEAR C-BIT
ROLB a#0 ;TRY ROL W/ MODE 3 EVEN BYTE
BCC ROT3C ;CHECK C-BIT
CMP a#0,#125124 ;CHECK DATA
BEQ ROT3D

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 746 <====

ROT3C: MOV #210,-(R2) ;MOVE TO MAILBOX # ***** 210 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;ROL W/ MODE 3 EVEN BYTE FAILED
ROT3D: MOV #125252,a#0 ;INITIALIZE DATA IN LOC. 0
SEC ;SET C-BIT
ROLB a#1 ;TRY ROL W/ MODE 3 ODD BYTE
BCC ROT3E ;CHECK C-BIT
CMP #052652,a#0 ;CHECK DATA
BEQ TST121

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 727 <====

ROT3E: MOV #211,-(R2) ;MOVE TO MAILBOX # ***** 211 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;ROL W/ MODE 3 ODD BYTE FAILED
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LU6

3494

; OR SEQUENCE ERROR

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3507 007552 005212
3508 007554 022712 000121
3509 007560 001016
3510 007562 012737 070707 000000
3511 007570 012700 000002
3512 007574 000261
3513 007576 006140
3514 007600 103406
3515 007602 022737 161617 000000
3516 007610 001002
3517 007612 005700
3518 007614 001404
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3521
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3523 007616
3524 007616 012742 000212
3525 007622 005242
3526 007624 000000
3527
3528
3529
3530
3531
3532
3533
3534
3535
3536
3537
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3540
3541
3542 007626 005212
3543 007630 022712 000122
3544 007634 001021
3545 007636 012737 007710 000000
3546 007644 012700 000002
3547 007650 012767 107070 000032
3548 007656 000241
3549 007660 006150
3550 007662 103006

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;*****
;
; THIS TEST VERIFIES MODE 4 ROTATE INSTRUCTIONS. THE DATA IS
; STORED IN LOC. 0. RO IS SET TO 2 AND THE CARRY IS SET. AN ROL MODE 4
; IS USED TO ROTATE LOCATION 0 USING RO. THE DATA IS CHECKED
; AND THE C AND V BITS ARE TESTED. THE PROPER DECREMENTING OF
; RO IS VERIFIED.
;*****
; TEST 121 TEST MODE 4 W/ ROTATE INSTRUCTIONS
;*****
TST121: INC (R2) ; UPDATE TEST NUMBER
; SEQUENCE ERROR?
CMP #121,(R2) ; BR TO ERROR HALT ON SEQ ERROR
BNE TST122-10 ; INITIALIZE DATA IN LOC. 0
MOV #070707,@#0 ; INITIALIZE RO AS PCINTER
MOV #2,RO ; SET C-BIT
SEC ; TRY ROL W/ MODE 4
ROL -(RO) ; CHECK C-BIT
BCS ROT4 ; CHECK DATA
CMP #161617,@#0 ; BRANCH IF DATA INCORRECT
BNE ROT4 ; CHECK MODE 4 REGISTER
TST RO
BEQ TST122
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 762 <====
;
ROT4: MOV #212,-(R2) ; MOVE TO MAILBOX # ***** 212 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; ROL MODE 4 FAILED
; OR SEQUENCE ERROR
;*****
;
; THIS TEST VERIFIES MODE 5 ROTATE INSTRUCTIONS.
; THE DATA IS STORED IN A WORK LOCATION (ROTX) AT THE END OF THE
; TEST CODE. LOC. 0 IS LOADED WITH THE ADDRESS OF THE DATA (ROTX).
; RO IS SET TO 2. THE CARRY IS CLEARED AND A MODE 5 ROL
; IS EXECUTED USING RO AS AN ADDRESSING REGISTER. THE DATA IS
; CHECKED, THE C AND V BITS TESTED, AND RO CHECKED FOR PROPER
; DECREMENTING.
;*****
; TEST 122 TEST MODE 5 W/ ROTATE INSTRUCTIONS
;*****
TST122: INC (R2) ; UPDATE TEST NUMBER
; SEQUENCE ERROR?
CMP #122,(R2) ; BR TO ERROR HALT ON SEQ ERROR
BNE ROT5 ; MOVE POINTER TO LOC. 0
MOV #ROTX,@#0 ; SET MODE 5 REG. TO LOC. 0
MOV #2,RO ; INITIALIZE DATA
MOV #107070,ROTX ; CLEAR C-BIT
CLC ; TRY ROL W/ MODE 5
ROL @-(RO) ; CHECK C-BIT
BCC ROT5

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3605 007760 005212
3606 007762 022712 000124
3607 007766 001016
3608 007770 012737 052525 007710
3609 007776 012737 007710 010034
3610 010004 000241
3611 010006 006177 000022
3612 010012 103404
3613 010014 023727 007710 125252
3614 010022 001405
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3619 010024
3620 010024 012742 000215
3621 010030 005242
3622 010032 000000
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3624 010034 000000
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3637 010036 005212
3638 010040 022712 000125
3639 010044 001013
3640 010046 012700 177400
3641 010052 000300
3642 010054 100404
3643
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3647 010056 012742 000216
3648 010062 005242
3649 010064 000000

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*****
: THIS TEST VERIFIES MODE 7 ROTATE INSTRUCTIONS.
: THE DATA IS SET IN LOC. ROTX. (SEE PREVIOUS TEST). THE ROL INSTRUCTION
: ADDRESSES IT INDIRECTLY USING MODE 7 AND INDIRECT ADDRESS LOCATION
: (ROTXAD) FOLLOWING THE TEST CODE.
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*****
TEST 124 TEST MODE 7 W/ ROTATE INSTRUCTIONS
*****

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†TST124: INC (R2) ; UPDATE TEST NUMBER
CMP #124,(R2) ; SEQUENCE ERROR?
BNE ROT7 ; BR TO ERROR HALT ON SEQ ERROR
MOV #52525,2#ROTX ; INITIALIZE DATA
MOV #ROTX,2#ROTXAD ; INITIALIZE ADDRESS POINTER
CLC ; CLEAR C-BIT
ROL 2#ROTXAD ; TRY ROL W/ MODE 7
BCS ROT7 ; CHECK C-BIT
CMP 2#ROTX,#125252 ; CHECK DATA
BEG TST125

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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 762 (====

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ROT7: MOV #215,-(R2) ; MOVE TO MAILBOX # ***** 215 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; ROL W/ MODE 7 FAILED
; OR SEQUENCE ERROR

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ROTXAD: 0

```

*****
: THIS TEST VERIFIES MODE 0 SWAB INSTRUCTION. RO IS SET TO
: 177400. A SWAB MODE 0 IS EXECUTED AND THE CONDITIONAL BRANCH
: IS USED TO CHECK THE SIGN OF THE RESULT. ALSO, A COMPARISON
: IS MADE TO CHECK THE DATA RESULTS.
*****

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```

*****
TEST 125 TEST MODE 0 W/ SWAB INST.
*****

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†TST125: INC (R2) ; UPDATE TEST NUMBER
CMP #125,(R2) ; SEQUENCE ERROR?
BNE TST126-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #177400,RO ; MOVE TEST PATTERN TO RO
SWAB RO ; TRY SWAB MODE 0
BMI 580

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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 774 (====

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MOV #216,-(R2) ; MOVE TO MAILBOX # ***** 216 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; SWAB DID NOT SET CC'S CORRECT

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3650 010066 022700 000377
3651 010072 001404
3652
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3656 010074 012742 000217
3657 010100 005242
3658 010102 000000
3659

SBC: CMP #377, RD
BEQ TST126

MOV #217, -(R2)
INC -(R2)
HALT

;CHECK RESULT
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS w/ 765 <====
: MOVE TO MAILBOX # ***** 217 *****
: SET MSGTYP TO FATAL ERROR
: RESULT OF SWAB MODE G FAILED
: OR SEQUENCE ERROR

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010104	005212		
010106	022712	000126	
010112	001011		
010114	012737	125652	000000
010122	005000		
010124	000310		
010126	022737	125253	000000
010134	001404		
010136	012742	000220	
010142	005242		
010144	000000		
010146	005212		
010150	022712	000127	
010154	001020		
010156	012737	125152	000000
010164	005000		
010166	000320		
010170	022737	065252	000000
010176	001404		
010200	012742	000221	
010204	005242		
010206	000000		
010210	162700	000002	
010214	001404		

 THIS TEST VERIFIES MODE 1 SWAB INSTRUCTION. THE TEST
 PATTERN IS MOVED TO LOC 0. R0 IS CLEARED AND USED AS THE ADDRESSING
 REGISTER IN THE MODE 1 SWAB. THE DATA RESULTS ARE CHECKED WITH
 A COMPARE.

 TEST 126 TEST MODE 1 W/ SWAB INST

 †TST126: INC (R2) ; UPDATE TEST NUMBER
 CMP #126,(R2) ; SEQUENCE ERROR?
 BNE TST127-10 ; BR TO ERROR HALT ON SEQ ERROR
 MOV #125652,R#0 ; MOVE TEST PATTERN TO LOC. 0
 CLR R0 ; R0=0
 SWAB (R0) ; TRY SWAB MODE 1
 CMP #125253,R#0 ; CHECK RESULT
 BEQ TST127
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
 ; CONDITIONAL BRANCH INST. AND <====
 ; REPLACE THE MOVE INSTRUCTION <====
 ; WHICH FOLLOWS W/ 767 <====
 MOV #220,-(R2) ; MOVE TO MAILBOX # ***** 220 *****
 INC -(R2) ; SET MSGTYP TO FATAL ERROR
 HALT ; RESULT OF SWAB MODE 1 FAILED
 ; OR SEQUENCE ERROR

 THIS TEST VERIFIES MODE 2 SWAB INSTRUCTION. THE TEST
 PATTERN IS MOVED TO LOC 0. R0 IS CLEARED AND USED AS THE MODE
 2 ADDRESSING REGISTER. THE RESULTS ARE CHECKED WITH A COMPARE.
 R0 IS CHECKED FOR PROPER DECREMENTING.

 TEST 127 TEST MODE 2 W/ SWAB INST

 †TST127: INC (R2) ; UPDATE TEST NUMBER
 CMP #127,(R2) ; SEQUENCE ERROR?
 BNE TST130-10 ; BR TO ERROR HALT ON SEQ ERROR
 MOV #125152,R#0 ; MOVE TEST PATTERN TO LOC. 0
 CLR R0 ; R0=0
 SWAB (R0)+ ; TRY SWAB MODE 2
 CMP #65252,R#0 ; CHECK RESULT
 BEQ SB2
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
 ; CONDITIONAL BRANCH INST. AND <====
 ; REPLACE THE MOVE INSTRUCTION <====
 ; WHICH FOLLOWS W/ 767 <====
 MOV #221,-(R2) ; MOVE TO MAILBOX # ***** 221 *****
 INC -(R2) ; SET MSGTYP TO FATAL ERROR
 HALT ; RESULT OF SWAB MODE 0 FAILED
 SB2: SUB #2,R0 ; CHECK EFFECT OF REG.
 BEQ TST130

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3716
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3720 010216 012742 000222          MOV      #222, -(R2)
3721 010222 005242          INC      -(R2)
3722 010224 000000          HALT
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
: CONDITIONAL BRANCH INST. AND
: REPLACE THE MOVE INSTRUCTION
: WHICH FOLLOWS W/ 760
: MOVE TO MAILBOX # ***** 222 *****
: SET MSGTYP TO FATAL ERROR
: REGISTER VALUE INCORRECT
: OR SEQUENCE ERROR

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: *****
: THIS TEST VERIFIES MODE 3 SWAB INSTRUCTION. THE TEST
: PATTERN IS MOVED TO LOC 0. A MODE 3 SWAB INSTRUCTION IS EXECUTED
: USING R7 AS THE ADDRESSING REGISTER. A COMPARE VERIFIES THE
: DATA RESULTS.
: *****

```

```

3736 010226 005212          TEST 130  TEST MODE 3 W/SWAB INST.
3737 010230 022712 000130      TST130: INC      (R2)
3738 010234 001011          CMP      #130, (R2)
3739 010236 012737 000377 000000  BNE     TST131-10
3740 010244 000337 000000      MOV     #377, @#0
3741 010250 022737 177400 000000  SWAB   @#0
3742 010256 001404          CMP     #177400, @#0
: UPDATE TEST NUMBER
: SEQUENCE ERROR?
: BR TO ERROR HALT ON SEQ ERROR
: MOVE TEST PATTERN TO LOC. 0
: TRY SWAB W/ MODE 3
: CHECK RESULT

```

```

3743
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3747 010260 012742 000223          MOV      #223, -(R2)
3748 010264 005242          INC      -(R2)
3749 010266 000000          HALT
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
: CONDITIONAL BRANCH INST. AND
: REPLACE THE MOVE INSTRUCTION
: WHICH FOLLOWS W/ 767
: MOVE TO MAILBOX # ***** 223 *****
: SET MSGTYP TO FATAL ERROR
: RESULT OF SWAB INCORRECT
: OR SEQUENCE ERROR

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010270 005212
010272 022712 000131
010276 001020
010300 012737 125652 000000
010306 012700 000002
010312 000340
010314 022737 125253 000000
010322 001404

010324 012742 000224
010330 005242
010332 000000
010334 005700
010336 001404

010340 012742 000225
010344 005242
010346 000000

```
*****
: THIS TEST VERIFIES MODE 4 SWAB INSTRUCTIONS. THE DATA
: IS MOVED TO LOC 0. R0 IS SET TO 2 AND USED AS THE MODE 4 ADDRESSING
: REGISTER. THE DATA IS CHECKED WITH A COMPARE AND R0 IS CHECKED
: FOR PROPER DECREMENTING.
*****
: TEST 131 TEST MODE 4 W/ SWAB INST
*****
TST131: INC (R2) ; UPDATE TEST NUMBER
CMP #131,(R2) ; SEQUENCE ERROR?
BNE TST132-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #125652,0#0 ; MOVE TEST PATTERN TO LOC. 0
MOV #2,R0 ; SET UP REGISTER POINTER
SWAB -(R0) ; TRY SWAB MODE 4
CMP #125253,0#0 ; CHECK RESULT
BEQ SB4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 766 <====
MOV #224,-(R2) ; MOVE TO MAILBOX # ***** 224 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; RESULT OF SWAB INCORRECT
SB4: TST R0 ; CHECK EFFECT ON REG.
BEQ TST132

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 760 <====
MOV #225,-(R2) ; MOVE TO MAILBOX # ***** 225 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; REGISTER VALUE INCORRECT
; OR SEQUENCE ERROR
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3802 010350 005212
3803 010352 022712 000132
3804 010356 001021
3805 010360 012700 010436
3806 010364 012767 125125 000040
3807 010372 000350
3808 010374 022767 052652 000030
3809 010402 001404
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3814 010404 012742 000226
3815 010410 005242
3816 010412 000000
3817 010414 020027 010434
3818 010420 001406
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3823 010422
3824 010422 012742 000227
3825 010426 005242
3826 010430 000000
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3828 010432 000000
3829 010434 010432
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```

*****
THIS TEST VERIFIES MODE 5 SWAB INSTRUCTION. THE TEST USES
TWO LOCATIONS FOLLOWING THE TEST CODE. SB5X HOLDS THE DATA;
SB5XAD IS A POINTER TO THE DATA LOCATION. THE DATA IS MOVED TO
SB5X AND RO IS SET TO TWO PLUS THE ADDRESS OF SB5XAD FOLLOWING
THE MODE 5 SWAB SB5X IS CHECKED FOR THE PROPER DATA. RO IS
CHECKED TO SEE THAT IT WAS DECREMENTED PROPERLY.
*****
TEST 132 TEST MODE 5 W/ SWAB INST.
*****
TST132: INC (R2) ; UPDATE TEST NUMBER
CMP #132, (R2) ; SEQUENCE ERROR?
BNE SB5 ; BR TO ERROR HALT ON SEQ ERROR
MOV #SB5XAD+2, RO ; SET UP POINTER TO WORK LOCATION
MOV #125125, SB5X ; MOVE PATTERN TO WORK LOCATION
SWAB @-(RO) ; TRY SWAB MODE 5
CMP #52652, SB5X ; CHECK RESULT
BEQ SB5A
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 766 (====
; MOVE TO MAILBOX # ***** 226 *****
; SET MSGTYP TO FATAL ERROR
; RESULT OF SWAB INCORRECT
; CHECK RESULT OF REG.
SB5A: CMP RO, #SB5XAD
BEQ TST133
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 757 (====
SB5: MOV #227, -(R2) ; MOVE TO MAILBOX # ***** 227 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; REGISTER VALUE INCORRECT
; OR SEQUENCE ERROR
; WORK LOCATION
SB5X: 0
SB5XAD: SB5X

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010436 005212
010440 022712 000133
010444 001013
010446 012767 125125 000030
010454 012700 010476
010460 000360 000006
010464 022760 052652 000006
010472 001405

010474
010474 012742 000230
010500 005242
010502 000000

010504 000000

```
*****
: THIS TEST VERIFIES MODE 6 SWAB INSTRUCTION. THIS TEST
: USES A WORK LOCATION (SB6X) FOLLOWING THE TEST CODE. TEST DATA
: IS LOADED INTO THE WORK LOCATION. R0, THE ADDRESSING REGISTER
: IS LOADED WITH 6 LESS THEN THE ADDRESS OF THE WORK LOCATION.
: THE MODE 6 SWAB IS EXECUTED WITH A +6 OFFSET. THE DATA IS
: VERIFIED WITH A COMPARE.
*****
: TEST 133 TEST MODE 6 W/ SWAB INST.
*****
TST133: INC (R2) ;UPDATE TEST NUMBER
CMP #133,(R2) ;SEQUENCE ERROR?
BNE SB6 ;BR TO ERROR HALT ON SEQ ERROR
MOV #125125,SB6X ;MOVE PATTERN TO WORK LOCATION
MOV #SB6X-6,R0 ;MOVE OFFSET POINTER TO R0
SWAB 6(R0) ;TRY SWAB W/ MODE 6
CMP #52652,6(R0) ;CHECK RESULT
BEQ TST134

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====

SB6: MOV #230,-(R2) ;MOVE TO MAILBOX # ***** 230 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;RESULT OF SWAB INCORRECT
; OR SEQUENCE ERROR
SB6X: 0 ;WORK LOCATION
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010506 005212
010510 022712 000134
010514 001013
010516 012767 177400 000030
010524 012700 010464
010530 000370 000072
010534 027027 000072 000377
010542 001406

010544
010544 012742 000231
010550 005242
010552 000900

010554 000000
010556 010554

```
*****
:
: THIS TEST VERIFIES MODE 7 SWAB INSTRUCTION. THIS TEST
: USES TWO LOCATIONS FOLLOWING THE TEST CODE: A WORK LOCATION
: (SB7X) AND A POINTER TO THE WORK LOCATION (SB7XAD). DATA IS MOVED
: TO THE WORK LOCATION. RO IS LOADED WITH 72 LESS THAN THE ADDRESS
: OF THE ADDRESS POINTER. THE DATA IS SWAB'ED USING A MODE 7
: INSTRUCTION WITH AN OFFSET OF +72. THE DATA IS VERIFIED WITH A
: COMPARE.
:
: *****
: TEST 134 TEST MODE 7 W/ SWAB INST.
: *****
TST134: INC (R2) ; UPDATE TEST NUMBER
        CMP #134,(R2) ; SEQUENCE ERROR?
        BNE SB7 ; BR TO ERROR HALT ON SEQ ERROR
        MOV #177400,SB7X ; MOVE PATTERN TO WORK LOCATION
        MOV #SB7XAD-72,RO ; MOVE OFFSET POINTER TO RO
        SWAB @72(RO) ; TRY SWAB MODE 7
        CMP @72(RO),#377 ; CHECK RESULTS
        BEQ TST135
;
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 765 <====
;
SB7: MOV #231,-(R2) ; MOVE TO MAILBOX # ***** 231 *****
      INC -(R2) ; SET MSGTYP TO FATAL ERROR
      HALT ; RESULT OF SWAB INCORRECT
; OR SEQUENCE ERROR
SB7X: 0 ; WORK LOCATION
SB7XAD: SB7X ; POINTER TO WORK LOCATION
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THIS TEST VERIFIES ALL LEGAL MODES OF THE JMP INSTRUCTION.
BECAUSE OF THE NATURE OF THE INSTRUCTION UNDER TEST, THIS TEST
UTILIZES SEVERAL DIFFERENT TECHNIQUES. THE CODE IS NOT EXECUTED
IN A LINEAR FASHION. THE DIFFERENT MODES ARE EXECUTED IN ORDER
FROM 1-7; HOWEVER, THE CODE IS ARRANGED SO THAT CONTROL LEAP
FROGS THRU THE TEST CODE. THE ORDER OF APPEARANCE OF THE CODE
IS:

- JMP MODE 1
- JMP MODE 3
- JMP MODE 2
- JMP MODE 4
- JMP MODE 6
- JMP MODE 5
- JMP MODE 7

AN INTERNAL SEQUENCE TEST (JMPSEQ) IS USED TO INSURE THAT THE
JUMPS ARE OCCURRING IN THE PROGRAMMED SEQUENCE.
THE TEST IS MADE UP OF SEVERAL BLOCKS OF CODE. EACH CODE
BEGINS WITH A LABEL WHICH INDICATES THE MODE BEING EXECUTED IN
THAT BLOCK. A SIMPLE PROCEDURE IS FOLLOWED IN EACH BLOCK. FOR
EXAMPLE THE CODE BEGINNING AT JMP3 WILL FIRST COMPARE THE RESULTS
OF THE PREVIOUS MODE 2 JUMP. (ANY REGISTER CHANGES ARE VERIFIED
AND THE SEQUENCE CHECK IS MADE). THEN THE REGISTERS ARE SETUP
FOR A MODE 3 JUMP TO THE NEXT TEST BLOCK (HERE, JMP4), THE SEQUENCE
CHECKER IS UPDATED AND THE JUMP IS EXECUTED.

IF A FAILURE OCCURS, THE SEQUENCE CHECKER WILL ASSIST IN
DETERMINING JUST WHICH MODE FAILED. IF THE SEQUENCE IS CORRECT
THEN THE ERROR DETECTED WAS A MODE FAILURE (E.G. FAILURE OF THE
REGISTER TO BE INCREMENTED IN MODE 2 JUMP.)

TEST 135 TEST THE JMP INSTRUCTION IN ALL MODES

```

TST135: INC      (R2)           ;UPDATE TEST NUMBER
          CMP      #135, (R2)   ;SEQUENCE ERROR?
          BNE     JMPCK+6      ;BR TO ERROR HALT ON SEQ ERROR
          CLR     JMPSEQ       ;ESTABLISH A SEQUENCE CHECKER
          MOV     #JMP2, R0     ;SET R0=JUMP TARGET
          JMP     (R0)         ;TRY JMP MODE 1
JMP3:    CMP     #.+2, R0      ;CHECK RESULT OF MODE 2 JUMP
          BEQ     JMP3A

          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
          ;          CONDITIONAL BRANCH INST. AND <====
          ;          REPLACE THE MOVE INSTRUCTION <====
          ;          WHICH FOLLOWS W/ 770 <====
          MOV     #232, -(R2)   ;MOVE TO MAILBOX # ***** 232 *****
          INC     -(R2)        ;SET MSGTYP TO FATAL ERROR
          HALT    .            ;REGISTER VALUE AFTER JMP MODE 2 INCORRECT
JMP3A:   CMP     JMPSEQ, #1    ;MAKE SURE JUMPS ARE IN SEQUENCE: JMPSEQ=1?
          BEQ     JMP3B

          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
          ;          CONDITIONAL BRANCH INST. AND <====
          ;          REPLACE THE MOVE INSTRUCTION <====
          ;          WHICH FOLLOWS W/ 760 <====

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010560 005212
010562 022712 000135
010566 001150
010570 005067 000326
010574 012700 010654
010600 000110
010602 022700 010604
010606 001404

010610 012742 000232
010614 005242
010616 000000
010620 026727 000276 000001
010626 001404

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MOV     #232, -(R2)
INC     -(R2)
HALT    .
JMP3A:  CMP     JMPSEQ, #1
BEQ     JMP3B

```

3953	010630	012742	000233		MOV	#233, -(R2)	; MOVE TO MAILBOX # ***** 233 *****
3954	010634	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
3955	010636	000000			HALT		; SHOULD BE HERE FROM JMP MODE 2 ONLY
3956	010640	012700	010652	JMP3B:	MOV	#IIMP4, R0	; POINT R0 TO INDIRECT JMP ADDR.
3957	010644	005267	000252		INC	JMPSEQ	; UPDATE SEQUENCE CHECKER
3958	010650	000130			JMP	2(R0)+	; TRY JMP MODE 3
3959	010652	010704		IIMP4:	JMP4		; ADDRESS INDIRECT JUMP
3960							
3961	010654	005767	000242	JMP2:	TST	JMPSEQ	; CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=0?
3962	010660	001404			BEQ	JMP2A	
3963							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3964							CONDITIONAL BRANCH INST. AND <====
3965							REPLACE THE MOVE INSTRUCTION <====
3966							WHICH FOLLOWS W/ 743 <====
3967	010662	012742	000234		MOV	#234, -(R2)	; MOVE TO MAILBOX # ***** 234 *****
3968	010666	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
3969	010670	000000			HALT		; SHOULD BE HERE FROM JMP MODE 1 ONLY
3970	010672	005267	000224	JMP2A:	INC	JMPSEQ	; UPDATE SEQUENCE CHECKER
3971	010676	012700	010602		MOV	#JMP3, R0	; SET R0=JUMP TARGET
3972	010702	000120			JMP	(R0)+	; TRY A JUMP MODE 2 TO "JMP3"
3973	010704	022700	010654	JMP4:	CMP	#IIMP4+2, R0	; CHECK RESULT OF REGISTER IN MODE 3 JUMP
3974	010710	001404			BEQ	JMP4A	
3975							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3976							CONDITIONAL BRANCH INST. AND <====
3977							REPLACE THE MOVE INSTRUCTION <====
3978							WHICH FOLLOWS W/ 727 <====
3979	010712	012742	000235		MOV	#235, -(R2)	; MOVE TO MAILBOX # ***** 235 *****
3980	010716	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
3981	010720	000000			HALT		; REGISTER VALUE AFTER MODE 3 JUMP INCORRECT
3982	010722	022767	000002 000172	JMP4A:	CMP	#2, JMPSEQ	; CHECK JUMP SEQUENCE: JMPSEQ=2?
3983	010730	001404			BEQ	JMP4B	
3984							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3985							CONDITIONAL BRANCH INST. AND <====
3986							REPLACE THE MOVE INSTRUCTION <====
3987							WHICH FOLLOWS W/ 717 <====
3988	010732	012742	000236		MOV	#236, -(R2)	; MOVE TO MAILBOX # ***** 236 *****
3989	010736	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
3990	010740	000000			HALT		; SHOULD BE ONLY FROM MODE 3 JUMP
3991	010742	012700	011012	JMP4B:	MOV	#JMP5+2, R0	; SET UP POINTER TO JUMP TARGET
3992	010746	005267	000150		INC	JMPSEQ	; UPDATE SEQUENCE CHECKER
3993	010752	000140			JMP	-(R0)	; TRY JUMP MODE 4 TO "JMP4"
3994							
3995	010754	022767	000004 000140	JMP6:	CMP	#4, JMPSEQ	; CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=4?
3996	010762	001404			BEQ	JMP6A	
3997							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
3998							CONDITIONAL BRANCH INST. AND <====
3999							REPLACE THE MOVE INSTRUCTION <====
4000							WHICH FOLLOWS W/ 702 <====
4001	010764	012742	000237		MOV	#237, -(R2)	; MOVE TO MAILBOX # ***** 237 *****
4002	010770	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR
4003	010772	000000			HALT		; SHOULD BE HERE ONLY FROM MODE 5 JUMP
4004	010774	012700	011442	JMP6A:	MOV	#JMP7+376, R0	; SET UP OFFSET POINTER TO JUMP TARGET
4005	011000	005267	000116		INC	JMPSEQ	; UPDATE JUMP SEQUENCE
4006	011004	000160	177402		JMP	-376(R0)	; TRY MODE 6 JUMP
4007							
4008	011010	022767	000003 000104	JMP5:	CMP	#3, JMPSEQ	; CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=3?


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4009 011016 001404          BEQ      JMP5A
4010
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4014 011020 012742 000240      MOV      #240,-(R2)
4015 011024 005242          INC      -(R2)
4016 011026 000000          HALT
4017 011030 012700 011044      JMP5A:  MOV      #IIMP5+2,R0
4018 011034 005267 000062          INC      JMPSEQ
4019 011040 000150          JMP      @-(R0)
4020 011042 010754          IIMP5:  JMP6
4021
4022 011044 022767 000005 000050  JMP7:  CMP      #5,JMPSEQ
4023 011052 001404          BEQ      JMP7A
4024
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4028 011054 012742 000241      MOV      #241,-(R2)
4029 011060 005242          INC      -(R2)
4030 011062 000000          HALT
4031 011064 012700 011110      JMP7A:  MOV      #IIMP+10,R0
4032 011070 005267 000026          INC      JMPSEQ
4033 011074 000170 177770          JMP      @-10(R0)
4034 011100 011102          IIMP:  JMPCK
4035
4036 011102 026727 000014 000006  JMPCK:  CMP      JMPSEQ,#6
4037 011110 001405          BEQ      TST136
4038
4039
4040
4041
4042 011112 012742 000242      MOV      #242,-(R2)
4043 011116 005242          INC      -(R2)
4044 011120 000000          HALT
4045
4046 011122 000000          JMPSEQ: 0

```

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 664 <====
; MOVE TO MAILBOX # ***** 240 *****
; SET MSGTYP TO FATAL ERROR
; SHOULD ONLY BE HERE FROM MODE 4 JUMP
; SET UP POINTER TO INDIRECT JUMP ADDR.
; UPDATE JUMP SEQUENCE
; TRY JUMP MODE 5 TO "JMP6"
; INDIRECT ADDRESS POINTER
; CHECK JUMPS IN SEQUENCE: JMPSEQ=5?
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 646 <====
; MOVE TO MAILBOX # ***** 241 *****
; SET MSGTYP TO FATAL ERROR
; SHOULD ONLY BE HERE FROM MODE 6 JUMP
; SET UP OFFSET POINTER TO INDIRECT ADDR.
; UPDATE JUMP SEQUENCE
; TRY MODE 7 JUMP
; INDIRECT ADDRESS
; CHECK JUMPS IN SEQUENCE: JMPSEQ
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 627 <====
; MOVE TO MAILBOX # ***** 242 *****
; SET MSGTYP TO FATAL ERROR
; SHOULD ONLY BE HERE FROM MODE 6 JUMP
; OR SEQUENCE ERROR

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011126 022712 000136
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011134 000402
011136 000137 011572
011142 012706 000500
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011152 005037 011552
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011160 005101
011162 004110
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011164 012742 000243
011170 005242
011172 000000
011174 022737 000001 011552
011202 001014
011204 020127 011336
011210 001011
011212 022706 000476
011216 001006
011220 022716 125252
011224 001003
011226 022700 011176
011232 001404
011234
011234 012742 000244
011240 005242

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*****
:
: THIS TEST VERIFIES ALL LEGAL MODES OF THE JSR INSTRUCTION.
: THE CONCEPT OF LEAP FROGGING AND SEQUENCE CHECKING (JSRSEQ) IS
: IDENTICAL TO THAT USED IN JMP TEST (SEE PREVIOUS TEST). EACH
: BLOCK OF CODE VERIFIES THE PREVIOUS JSR BY CHECKING THE SEQUENCE,
: CHECKING THAT THE PC WAS SAVED IN THE SPECIFIED REGISTER, CHECKING
: THAT THE SP WAS DECREMENTED, CHECKING THAT THE REGISTER WAS
: SAVED ON THE STACK, AND FINALLY CHECKING THAT ANY MODE ADDRESS
: REGISTER ALTERATIONS (E.G. INCREMENT REGISTER IN MODE 2) WERE
: SUCCESSFUL. R1 IS USED AS THE REGISTER IN ALL JSR INSTRUCTIONS.
: IF A FAILURE OCCURS, THE SEQUENCE CHECKER WILL ASSIST IN
: DETERMINING JUST WHICH MODE FAILED. IF THE SEQUENCE IS CORRECT
: THEN THE ERROR DETECTED WAS A FUNCTIONAL FAILURE (E.G., INCORRECT
: REGISTER SAVED).
:
: *****
: TEST 136 TEST JSR INSTRUCTION W/ ALL MODES
: *****
: ST136: INC (R2) ;UPDATE TEST NUMBER
: CMP #136,(R2) ;SEQUENCE ERROR?
: BNE JSR0 ;BR TO ERROR HALT ON SEQ ERROR
: BR JSR1
: JSR0: JMP @#JSRCK1
:
: JSR1: MOV #STBOT,R6 ;SET STACK POINTER
: MOV #JSR2,R0 ;SET TARGET ADDRESS
: CLR @#JSRSEQ ;INITIALIZE SEQUENCE CHECKER
: CLR R1 ;INITIALIZE R1
: COM R1
: JSR R1,(R0) ;TRY JSR MODE 1
: ; TO SCOPE: REPLACE THE MOVE INSTRUCTION <===
: ; FOLLOWING W/ 774 <===
:
: JSR1A: MOV #243,-(R2) ;MOVE TO MAILBOX # ***** 243 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;JSR MODE 1 FAILED
:
: JSR3: CMP #1,@#JSRSEQ ;CHECK SEQUENCE: JSRSEQ=1?
: BNE JSR3A ;BRANCH IF OUT OF SEQUENCE
: CMP R1,#JSR4 ;PROPER PC SAVED?
: BNE JSR3A ;BRANCH IF PC WRONG
: CMP #STBOT-2,R6 ;STACK POINTER DECREMENTED?
: BNE JSR3A ;BRANCH IF SP WRONG
: CMP #125252,(R6) ;REG SAVED ON STACK?
: BNE JSR3A ;BRANCH IF REG. NOT SAVED
: CMP #JSR3+2,R0 ;MODE 2 INCREMENT CORRECT?
: BEQ JSR3B
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===
: ; CONDITIONAL BRANCH INST. AND <===
: ; REPLACE THE MOVE INSTRUCTION <===
: ; WHICH FOLLOWS W/ 740 <===
:
: JSR3A: MOV #244,-(R2) ;MOVE TO MAILBOX # ***** 244 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
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4103 011242 000000          HALT          ;JSR MODE 3 MALFUNCTIONED
4104 011244 005237 011552 JSR3B: INC      @#JSRSEQ ;UPDATE SEQUENCE CHECKER
4105 011250 004137 011336 JSR      R1,@#JSR4 ;TRY JSR MODE 4
4106
4107 011254 005737 011552 JSR2:  TST      @#JSRSEQ ;CHECK SEQUENCE: JSRSEQ=0?
4108 011260 001011          BNE      JSR2A ;BRANCH IF OUT OF SEQUENCE
4109 011262 020127 011164 CMP      R1,#JSR1A ;PROPER PC SAVED?
4110 011266 001006          BNE      JSR2A ;BRANCH IF PC WRONG
4111 011270 022706 000476 CMP      #STBOT-2,R6 ;R6 DECREMENT?
4112 011274 001003          BNE      JSR2A ;BRANCH IF R6 IS INCORRECT
4113 011276 021627 177777 CMP      (R6), #-1 ;REGISTER SAVED?
4114 011302 001404          BEQ      JSR2B
4115
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4119 011304          JSR2A:
4120 011304 012742 000245 MOV      #245,-(R2) ;MOVE TO MAILBOX # ***** 245 *****
4121 011310 005242          INC      -(R2) ;SET MSGTYP TO FATAL ERROR
4122 011312 000000          HALT     ;JSR MODE 1 MALFUNCTIONED
4123 011314 012706 000500 JSR2B: MOV      #STBOT,R6 ;INITIALIZE R6
4124 011320 012701 125252 MOV      #125252,R1 ;INITIALIZE R1
4125 011324 005237 011552 INC      @#JSRSEQ ;UPDATE SEQUENCE CHECKER
4126 011330 012700 011174 MOV      #JSR3,R0 ;SET TARGET ADDRESS
4127 011334 004120          JSR      R1,(R0)+ ;TRY JSR MODE 2
4128
4129 011336 022737 000002 011552 JSR4:  CMP      #2,@#JSRSEQ ;CHECK SEQUENCE: JSRSEQ=2?
4130 011344 001003          BNE      JSR4A ;BRANCH IF OUT OF SEQUENCE
4131 011346 022701 011254 CMP      #JSR2,R1 ;PROPER PC SAVED?
4132 011352 001404          BEQ      JSR4B
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4137 011354          JSR4A:
4138 011354 012742 000246 MOV      #246,-(R2) ;MOVE TO MAILBOX # ***** 246 *****
4139 011360 005242          INC      -(R2) ;SET MSGTYP TO FATAL ERROR
4140 011362 000000          HALT     ;JSR MODE 3 MALFUNCTIONED
4141 011364 005237 011552 JSR4B: INC      @#JSRSEQ ;UPDATE SEQUENCE CHECKER
4142 011370 012700 011444 MOV      #JSR5+2,R0 ;SET TARGET ADDRESS
4143 011374 004140          JSR      R1,-(R0) ;TRY JSR MODE 4
4144
4145 011376 022767 000004 000146 JSR6:  CMP      #4,JSRSEQ ;CHECK SEQUENCE: JSRSEQ=4?
4146 011404 001006          BNE      JSR6A ;BRANCH IF OUT OF SEQUENCE
4147 011406 022701 011510 CMP      #JSR7,R1 ;PROPER PC SAVED?
4148 011412 001003          BNE      JSR6A ;BRANCH IF PC WRONG
4149 011414 022700 011546 CMP      #JSR6AD,R0 ;MODE 5 REGISTER CORRECT?
4150 011420 001404          BEQ      JSR6B
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4155 011422          JSR6A:
4156 011422 012742 000247 MOV      #247,-(R2) ;MOVE TO MAILBOX # ***** 247 *****
4157 011426 005242          INC      -(R2) ;SET MSGTYP TO FATAL ERROR
4158 011430 000000          HALT     ;JSR MODE 5 FAILED

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4159 011432 005237 011552 JSR6B: INC 0#JSRSEQ ;UPDATE SEQUENCE CHECKER
4160 011436 004167 003046 JSR R1,JSR7 ;TRY JSR MODE 6
4161 011442 022767 000003 000102 JSR5: CMP #3,JSRSEQ ;CHECK SEQUENCE: JSRSEQ=3?
4162 011450 001006 BNE JSR5A ;BRANCH IF OUT OF SEQUENCE
4163 011452 022701 011376 CMP #JSR6,R1 ;PROPER PC SAVED?
4164 011456 001003 BNE JSR5A ;BRANCH IF PC WRONG
4165 011460 022700 011442 CMP #JSR5,R0 ;CHECK MODE 4 REGISTER
4166 011464 001404 BEQ JSR5B
4167 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4168 : CONDITIONAL BRANCH INST. AND <====
4169 : REPLACE THE MOVE INSTRUCTION <====
4170 : WHICH FOLLOWS W/ 623 <====
4171 011466 JSR5A:
4172 011466 012742 000250 MOV #250,-(R2) ;MOVE TO MAILBOX # ***** 250 *****
4173 011472 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4174 011474 000000 HALT ;JSR MODE 4 MALFUNCTIONED
4175 011476 005237 011552 JSR5B: INC 0#JSRSEQ ;UPDATE SEQUENCE CHECKER
4176 011502 012700 011550 MOV #JSR6AD+2,R0 ;POINT R0 TO TARGET ADDRESS
4177 011506 004150 JSR R1,0-(R0) ;TRY JSR MODE 5
4178
4179 011510 022737 000005 011552 JSR7: CMP #5,0#JSRSEQ ;CHECK SEQUENCE: JSRSEQ=5?
4180 011516 001003 BNE JSR7A ;BRANCH IF OUT OF SEQUENCE
4181 011520 022701 011442 CMP #JSR5,R1 ;PROPER PC SAVED?
4182 011524 001404 BEQ JSR7B
4183 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4184 : CONDITIONAL BRANCH INST. AND <====
4185 : REPLACE THE MOVE INSTRUCTION <====
4186 : WHICH FOLLOWS W/ 603 <====
4187 011526 JSR7A:
4188 011526 012742 000251 MOV #251,-(R2) ;MOVE TO MAILBOX # ***** 251 *****
4189 011532 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4190 011534 000000 HALT ;JSR MODE 6 FAILED
4191 011536 005237 011552 JSR7B: INC 0#JSRSEQ ;UPDATE SEQUENCE CHECKER
4192 011542 004177 000002 JSR R1,0JSRCKAD ;TRY JSR MODE 7
4193
4194 011546 011376 JSR6AD: JSR6 ;MODE 5 TARGET ADDRESS
4195 011550 011554 JSRCKAD: JSRCK ;MODE 7 TARGET ADDRESS
4196 011552 000000 JSRSEQ: 0 ;SEQUENCE CHECKER
4197
4198 011554 022767 000006 177770 JSRCK: CMP #6,JSRSEQ ;CHECK SEQUENCE: JSRSEQ=6?
4199 011562 001003 BNE JSRCK1 ;BRANCH IF OUT OF SEQUENCE
4200 011564 022701 011546 CMP #JSR6AD,R1 ;PROPER PC SAVED?
4201 011570 001404 BEQ TST137
4202 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4203 : CONDITIONAL BRANCH INST. AND <====
4204 : REPLACE THE MOVE INSTRUCTION <====
4205 : WHICH FOLLOWS W/ 561 <====
4206 011572 JSRCK1:
4207 011572 012742 000252 MOV #252,-(R2) ;MOVE TO MAILBOX # ***** 252 *****
4208 011576 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4209 011600 000000 HALT ;JSR MODE 7 MALFUNCTIONED
4210 ; OR SEQUENCE ERROR
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4212 ;*****
4213 ;
4214 ;

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011602 005212
011604 022712 000137
011610 001016
011612 012706 000500
011616 012746 052525
011622 012700 011640
011626 000200

011630 012742 000253
011634 005242
011636 000000
011640 022700 052525
011644 001404

011646 012742 000254
011652 005242
011654 000000
  
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: THIS TEST VERIFIES THE RTS INSTRUCTION. THE STACK POINTER
: IS INITIALIZED AND A TEST PATTERN STORED ON STACK. R0 IS LOADED
: WITH RETURN ADDRESS. AN RTS IS EXECUTED, AND, AT THE TARGET
: ADDRESS, A CHECK IS MADE THAT R0 WAS PROPERLY RESTORED FROM THE
: STACK.
: *****
: TEST 137 TEST RTS INSTRUCTION
: *****
TST137: INC (R2) ; UPDATE TEST NUMBER
CMP #137,(R2) ; SEQUENCE ERROR?
BNE TST140-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #STBOT,R6 ; INITIALIZE STACK POINTER
MOV #52525,-(R6) ; INITIALIZE TOP OF STACK
MOV #RTS1,R0 ; INITIALIZE RETURN REGISTER
RTS R0 ; TRY RTS THROUGH R0
; TO SCOPE: REPLACE THE MOVE INSTRUCTION (<====
; FOLLOWING W/ 770 (<====
MOV #253,-(R2) ; MOVE TO MAILBOX # ***** 253 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; RTS FAILED
RTS1: CMP #52525,R0 ; CHECK THAT R0 RESTORED FROM STACK
BEQ TST140
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (<====
; CONDITIONAL BRANCH INST. AND (<====
; REPLACE THE MOVE INSTRUCTION (<====
; WHICH FOLLOWS W/ 762 (<====
MOV #254,-(R2) ; MOVE TO MAILBOX # ***** 254 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; RTS MALFUNCTIONED
; OR SEQUENCE ERROR
  
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011656 005212
011660 022712 000140
011664 001022
011666 000277
011670 000251
011672 012700 100000
011676 101402
011700 102401
011702 100404

011704
011704 012742 000255
011710 005242
011712 000000

011714 000277
011716 000244
011720 012700 000000
011724 101002
011726 102401
011730 100004

011732
011732 012742 000256
011736 005242
011740 000000

011742 005212

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*****
THESE NEXT FOUR TESTS VERIFY THE FUNCTIONING OF A GROUP
OF FOUR INSTRUCTIONS. THE GROUP CONSISTS OF THE INSTRUCTIONS:
MOV, BIC, BIT, AND BIS. THESE INSTRUCTIONS ARE SIMILAR IN THE
WAY THEY EFFECT THE C AND V BITS. THEY ALL LEAVE THE V-BIT
CLEAR AND THE C-BIT UNAFFECTED.
THE TEST PROCEDURE IS AS FOLLOWS: THE N, Z, AND V BITS
ARE LOADED WITH THE COMPLEMENT OF THE EXPECTED RESULTS, THE C-BIT
IS LOADED WITH THE DESIRED RESULT. THE INSTRUCTION IS EXECUTED
WITH DIFFERENT DATA PATTERNS AND THE RESULTS ARE VERIFIED WITH
A SERIES OF CONDITIONAL BRANCH INSTRUCTIONS. THE DATA IS CHOSEN
TO PRODUCT ALL POSSIBLE COMBINATIONS OF THE C AND V BITS.
*****
TEST 140 TEST MOV INSTRUCTION
*****
TST140: INC (R2) ;UPDATE TEST NUMBER
CMP #140, (R2) ;SEQUENCE ERROR?
BNE TST141-10 ;BR TO ERROR HALT ON SEQ ERROR
SCC ;CC=0110
+CLN!CLC
MOV #100000, R0 ;CC=1000
BLOS MOV1
BVS MOV1
BMI MOV2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 771 <====
MOV1: MOV #255, -(R2) ;MOVE TO MAILBOX # ***** 255 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;MOV DID NOT SET CC'S CORRECTLY
MOV2: SCC ;CC=1011
CLZ ;CC=0101
MOV #0, R0 ;C OR Z = 0?
BHI MOV3 ;V=1?
BVS MOV3
BPL TST141
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 756 <====
MOV3: MOV #256, -(R2) ;MOVE TO MAILBOX # ***** 256 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;MOV DID NOT SET CC'S CORRECTLY
; OR SEQUENCE ERROR
*****
;TEST 141 TEST BIT INSTRUCTION
*****
TST141: INC (R2) ;UPDATE TEST NUMBER
*****

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4301 011744 022712 000141      CMP      #141,(R2)      ;SEQUENCE ERROR?
4302 011750 001024      BNE     TST142-10     ;BR TO ERROR HALT ON SEG ERROR
4303 011752 012700 100001      MOV     #100001,R0
4304 011756 000277      SCC
4305 011760 000251      +CLN!CLC             ;CC=0110
4306 011762 032700 100000      BIT     #100000,R0    ;CC=1000
4307 011766 101402      BLOS   BIT1
4308 011770 102401      BVS    BIT1
4309 011772 100404      BMI    BIT2
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4314 011774
4315 011774 012742 000257      BIT1:  MOV     #257,-(R2) ;MOVE TO MAILBOX # ***** 257 *****
4316 012000 005242      INC     -(R2)         ;SET MSGTYP TO FATAL ERROR
4317 012002 000000      HALT    ;BIT DID NOT SET CC'S CORRECTLY
4318
4319 012004 000277      BIT2:  SCC
4320 012006 000244      CLZ
4321 012010 032700 077776      BIT     #77776,R0    ;CC=0101
4322 012014 101002      BHI    BIT3
4323 012016 102401      BVS    BIT3
4324 012020 100004      BPL    TST142
4325
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4329 012022      BIT3:
4330 012022 012742 000260      MOV     #260,-(R2)   ;MOVE TO MAILBOX # ***** 260 *****
4331 012026 005242      INC     -(R2)         ;SET MSGTYP TO FATAL ERROR
4332 012030 000000      HALT    ;BIT DID NOT SET CC'S CORRECTLY
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4338 012032 005212      ;*****
4339 012034 022712 000142      ;TEST 142 TEST BIC INSTRUCTION
4340 012040 001024      ;*****
4341 012042 012700 177777      TST142: INC     (R2)      ;UPDATE TEST NUMBER
4342 012046 000277      CMP     #142,(R2)    ;SEQUENCE ERROR?
4343 012050 000251      BNE     TST143-10    ;BR TO ERROR HALT ON SEG ERROR
4344 012052 042700 077777      MOV     #177777,R0
4345 012056 101402      SCC
4346 012060 102401      +CLN!CLC             ;CC=0110
4347 012062 100404      BIC     #77777,R0    ;CC=1000
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4352 012064      BIC1:
4353 012064 012742 000261      MOV     #261,-(R2)   ;MOVE TO MAILBOX # ***** 261 *****
4354 012070 005242      INC     -(R2)         ;SET MSGTYP TO FATAL ERROR
4355 012072 000000      HALT    ;BIC DID NOT SET CC'S CORRECTLY
4356 012074 000277      BIC2:  SCC             ;CC=1011

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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 767 (====

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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 754 (====

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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
; CONDITIONAL BRANCH INST. AND (====
; REPLACE THE MOVE INSTRUCTION (====
; WHICH FOLLOWS W/ 767 (====

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012214 005212
012216 022712 000144
012222 001037
012224 012700 077777
012230 000257
012232 000264
012234 005200
012236 101402
012240 100001
012242 102404

012244
012244 012742 000265
012250 005242
012252 000000
012254 052700 077777
012260 000261
012262 000244
012264 005200
012266 100403
012270 102402
012272 103001
012274 001404

012276
012276 012742 000266
012302 005242
012304 000000

012306 000277
012310 000241
012312 005200
012314 101402
012316 100401
012320 100004

```
*****
: THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE INC AND
: DEC INSTRUCTIONS. THESE INSTRUCTIONS BOTH EFFECT THE C AND V
: BITS THE SAME; THE C-BIT IS LEFT UNCHANGED AND THE V-BIT IS DEPENDENT
: UPON THE DATA RESULTS. THE SAME PROCEDURE IS USED. THE CONDITION
: CODE BITS ARE INITIALIZED, THE INSTRUCTION IS EXECUTED AND THE
: RESULTS ARE VERIFIED WITH A SERIES OF CONDITIONAL BRANCH INSTRUCTIONS.
: THIS PROCEDURE IS REPEATED WITH SEVERAL DATA PATTERNS TO PRODUCE
: DIFFERENT COMBINATIONS OF THE C AND V BITS.
*****
: TEST 144 TEST INC INSTRUCTION
*****
TST144: INC (R2) ;UPDATE TEST NUMBER
CMP #144,(R2) ;SEQUENCE ERROR?
BNE TST145-10 ;BR TO ERROR HALT ON SEQ ERROR
MOV #077777,R0 ;RO=077777
CCC ;CC=0100
SEZ ;
INC R0 ;CC=1010 RO=10000
BLOS INC1
BPL INC1
BVS INC2
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 770
INC1: MOV #265,-(R2) ;MOVE TO MAILBOX # ***** 265 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;INC DID NOT SET CC'S CORRECTLY
INC2: BIS #77777,R0 ;RO=177777
SEC ;CC=1011
CLZ ;
INC R0 ;CC=0101 RC=0
BMI INC3
BVS INC3
BCC INC3
BEQ INC4
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 753
INC3: MOV #266,-(R2) ;MOVE TO MAILBOX # ***** 266 *****
INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;INC DID NOT SET CC'S CORRECTLY
INC4: SCC ;CC=1110
CLC
INC R0 ;CC=0000 RO=1
BLOS INCS
BMI INCS
BPL TST145
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4471 012322
4472 012322 012742 000267
4473 012326 005242
4474 012330 000000
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4480 012332 005212
4481 012334 022712 000145
4482 012340 001051
4483 012342 012700 000002
4484 012346 000277
4485 012350 005300
4486 012352 100403
4487 012354 001402
4488 012356 102401
4489 012360 103404
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4494 012362
4495 012362 012742 000270
4496 012366 005242
4497 012370 000000
4498 012372 000261
4499 012374 000244
4500 012376 005300
4501 012400 101002
4502 012402 100401
4503 012404 102004
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4508 012406
4509 012406 012742 000271
4510 012412 005242
4511 012414 000000
4512 012416 000277
4513 012420 000251
4514 012422 005300
4515 012424 101402
4516 012426 102401
4517 012430 100404
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4522 012432

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; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 741
=====

INC5:
MOV #267, -(R2) ; MOVE TO MAILBOX # ***** 267 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; INC DID NOT SET CC'S CORRECTLY
; OR SEQUENCE ERROR

;*****
;TEST 145 TEST DEC INSTRUCTION
;*****
†ST145: INC (R2) ; UPDATE TEST NUMBER
CMP #145, (R2) ; SEQUENCE ERROR?
BNE TST146-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #2, R0 ; R0=2
SCC ; CC=1111
DEC R0 ; CC=0001 R0=1
BMI DEC1
BEQ DEC1
BVS DEC1
BCS DEC2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 770
=====

DEC1:
MOV #270, -(R2) ; MOVE TO MAILBOX # ***** 270 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; DEC DID NOT SET CC'S CORRECTLY
DEC2:
SEC ; CC=1011
CLZ
DEC R0 ; CC=0101 R0=0
BMI DEC3
BVI DEC3
BVC DEC4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 756
=====

DEC3:
MOV #271, -(R2) ; MOVE TO MAILBOX # ***** 271 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; DEC DID NOT SET CC'S CORRECTLY
DEC4:
SCC ; CC=0110
+CLN:CLC
DEC R0 ; CC=1000 R0=17777
BLOS DEC5
BVS DEC5
BMI DEC6

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
; CONDITIONAL BRANCH INST. AND
; REPLACE THE MOVE INSTRUCTION
; WHICH FOLLOWS W/ 744
=====

DEC5:

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4523 012432 012742 000272      MOV      #272, -(R2)      ;MOVE TO MAILBOX # ***** 272 *****
4524 012436 005242      INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4525 012440 000000      HALT                    ;DEC DID NOT SET CC'S CORRECTLY
4526 012442 042700 077777      DEC6:  BIC      #77777, R0 ;RO=100000
4527 012446 000277      SCC                                ;CC=0101
4528 012450 000252      +CLN!CLV
4529 012452 005300      DEC      R0              ;CC=1011  R0=77777
4530 012454 100403      BMI     DEC7             ;CC=0011
4531 012456 001402      BEQ     DEC7
4532 012460 102001      BVC     DEC7
4533 012462 103404      BCS     TST146
4534
4535      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  (====
4536      ;          CONDITIONAL BRANCH INST. AND  (====
4537      ;          REPLACE THE MOVE INSTRUCTION  (====
4538      ;          WHICH FOLLOWS W/ 727        (====
4539 012464      DEC7:
4539 012464 012742 000273      MOV      #273, -(R2)      ;MOVE TO MAILBOX # ***** 273 *****
4540 012470 005242      INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4541 012472 000000      HALT                    ;DEC DID NOT SET CC'S CORRECTLY
4542
4543      ; OR SEQUENCE ERROR

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012474 005212
012476 022712 000146
012502 001007
012504 000277
012506 000244
012510 005000
012512 100403
012514 102402
012516 103401
012520 001404

012522
012522 012742 000274
012526 005242
012530 000000

012532 005212
012534 022712 000147
012540 001022
012542 000277
012544 000244
012546 005700
012550 100403
012552 102402
012554 103401
012556 001404

012560
012560 012742 000275
012564 005242
012566 000000
012570 005300
012572 000277

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*****;*****
:
: THESE NEXT THREE TESTS VERIFY THE FUNCTIONING OF THE CLR,
: TST, AND SWAB INSTRUCTIONS. THESE THREE INSTRUCTIONS ALL LEAVE
: THE C AND V BITS CLEARED. AGAIN, THE CONDITION CODES ARE PRESET,
: THE INSTRUCTION EXECUTED AND THE RESULTS CHECKED WITH CONDITIONAL
: BRANCH INSTRUCTIONS. THE PROCEDURE IS REPEATED TO PRODUCE OTHER
: COMBINATIONS OF CONDITION CODES.
:
: *****
: TEST 146 TEST CLR INSTRUCTION
: *****
TST146: INC (R2) ;UPDATE TEST NUMBER
        CMP #146,(R2) ;SEQUENCE ERROR?
        BNE TST147-10 ;BR TO ERROR HALT ON SEQ ERROR
        SCC ;CC=1011
        CLZ
        CLR RO ;CC=0100 RO=0
        BMI CLR1
        BVS CLR1
        BCS CLR1
        BEQ TST147
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 771 <====
:
CLR1: MOV #274,-(R2) ;MOVE TO MAILBOX # ***** 274 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;CLR DID NOT SET CC'S CORRECTLY
: ; OR SEQUENCE ERROR
:
: *****
: TEST 147 TEST TST INSTRUCTION
: *****
TST147: INC (R2) ;UPDATE TEST NUMBER
        CMP #147,(R2) ;SEQUENCE ERROR?
        BNE TST150-10 ;BR TO ERROR HALT ON SEQ ERROR
        SCC ;CC=1011
        CLZ
        TST RO ;CC=0100
        BMI TEST1
        BVS TEST1
        BCS TEST1
        BEQ TEST2
:
: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 771 <====
:
TEST1: MOV #275,-(R2) ;MOVE TO MAILBOX # ***** 275 *****
      INC -(R2) ;SET MSGTYP TO FATAL ERROR
      HALT ;TEST DID NOT SET CC'S CORRECTLY
TEST2: DEC RO ;MAKE RO NEGATIVE
      SCC ;CC=0111
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4600 012574 000250          CLN
4601 012576 005700          TST      RO      ;CC=1000
4602 012600 101402          BLOS    TEST3
4603 012602 102401          BVS     TEST3
4604 012604 100404          BMI     TST150
4605
4606                      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4607                      ; CONDITIONAL BRANCH INST. AND <====
4608                      ; REPLACE THE MOVE INSTRUCTION <====
4609                      ; WHICH FOLLOWS W/ 756 <====
4610 012606 012742 000276    TEST3:  MOV     #276, -(R2) ;MOVE TO MAILBOX # ***** 276 *****
4611 012612 005242          INC     -(R2)      ;SET MSGTYP TO FATAL ERROR
4612 012614 000000          HALT                    ;TEST DID NOT SET CC'S CORRECTLY
4613                      ; OR SEQUENCE ERROR
4614
4615                      ;*****
4616                      ;TEST 150      TEST SWAB INSTRUCTION
4617                      ;*****
4618 012616 005212          TST150: INC     (R2)      ;UPDATE TEST NUMBER
4619 012620 022712 000150    CMP     #150, (R2)    ;SEQUENCE ERROR?
4620 012624 001023          BNE    TST151-10    ;BR TO ERROR HALT ON SEQ ERROR
4621 012626 012700 170000    MOV     #170000, RO  ;RO=170000
4622 012632 000277          SCC                    ;CC=0111
4623 012634 000250          CLN
4624 012636 000300          SWAB   RO           ;CC=1000  RO=360
4625 012640 101402          BLOS   SWB1
4626 012642 102401          BVS    SWB1
4627 012644 100404          BMI    SWB2
4628
4629                      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4630                      ; CONDITIONAL BRANCH INST. AND <====
4631                      ; REPLACE THE MOVE INSTRUCTION <====
4632                      ; WHICH FOLLOWS W/ 77C <====
4633 012646 012742 000277    SWB1:  MOV     #277, -(R2) ;MOVE TO MAILBOX # ***** 277 *****
4634 012652 005242          INC     -(R2)      ;SET MSGTYP TO FATAL ERROR
4635 012654 000000          HALT                    ;SWAB DID NOT SET CC'S CORRECTLY
4636 012656 000277          SWB2:  SCC                    ;CC=1011
4637 012660 000244          CLZ
4638 012662 000300          SWAB   RO           ;CC=0100  RO=170000
4639 012664 102403          BVS    SWB3
4640 012666 103402          BCS    SWB3
4641 012670 100401          BMI    SWB3
4642 012672 001404          BEQ    TST151
4643
4644                      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4645                      ; CONDITIONAL BRANCH INST. AND <====
4646                      ; REPLACE THE MOVE INSTRUCTION <====
4647                      ; WHICH FOLLOWS W/ 755 <====
4648 012674 012742 000300    SWB3:  MOV     #300, -(R2) ;MOVE TO MAILBOX # ***** 300 *****
4649 012700 005242          INC     -(R2)      ;SET MSGTYP TO FATAL ERROR
4650 012702 000000          HALT
4651

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012704 005212
012706 022712 000151
012712 001062
012714 012700 040000
012720 000277
012722 062700 030000
012726 101402
012730 102401
012732 100004

012734
012734 012742 000301
012740 005242
012742 000000
012744 000264

012746 062700 010000
012752 101402
012754 102001
012756 100404

012760
012760 012742 000302
012764 005242
012766 000000
012770 000257
012772 000270
012774 062700 100000
013000 101002
013002 102001
013004 100004

013006

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*****
: THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE ADD AND
: ADC INSTRUCTIONS. BOTH OF THESE INSTRUCTIONS HANDLE THE C AND
: V BITS IDENTICALLY. THE PROCEDURE IS TO PRESET THE CONDITION
: CODES, EXECUTE THE INSTRUCTION WITH A PARTICULAR SET OF DATA, AND
: THEN CHECK THE RESULTS BY EXECUTING A SERIES OF CONDITIONAL
: BRANCHES. THIS PROCEDURE IS REPEATED SEVERAL TIMES WITH DIFFERENT
: DATA TO PRODUCE EVERY COMBINATION OF C AND V BITS.
*****
: TEST 151 TEST ADD INSTRUCTION
*****
: ST151: INC (R2) ;UPDATE TEST NUMBER
: CMP #151,(R2) ;SEQUENCE ERROR?
: BNE TST152-10 ;BR TO ERROR HALT ON SEQ ERROR
: MOV #40000,R0 ;RO=40000
: SCC ;CC=1111
: ADD #30000,R0 ;CC=0000 RO=70000
: BLOS ADD1
: BVS ADD1
: BPL ADD2
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 770 <====
:
: ADD1: MOV #301,-(R2) ;MOVE TO MAILBOX # ***** 301 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;ADD DID NOT SET CC'S CORRECTLY
: ADD2: SEZ ;CC=0100
: ;
: ADD #10000,R0 ;CC=1010 40=100000
: BLOS ADD3
: BVC ADD3
: BMI ADD4
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 756 <====
:
: ADD3: MOV #302,-(R2) ;MOVE TO MAILBOX # ***** 302 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;ADD DID NOT SET CC'S CORRECTLY
: ADD4: CCC ;CC=1000
: SEN
: ADD #100000,R0 ;CC=0111 RO=0
: BHI ADD5
: BVC ADD5
: BPL ADD6
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 743 <====
:
: ADD5:
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4708 013006 012742 000303      MOV      #303, -(R2)      ;MOVE TO MAILBOX # ***** 303 *****
4709 013012 005242              INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4710 013014 000000              HALT                    ;ADD DID NOT SET CC'S CORRECTLY
4711 013016 062700 177777      ADD6:   ADD      #177777, R0 ;CC=1000 RO=177777
4712 013022 101402              BLOS    ADD7
4713 013024 102401              BVS     ADD7
4714 013026 100404              BMI     ADD8
4715                                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4716                                ;          CONDITIONAL BRANCH INST. AND <====
4717                                ;          REPLACE THE MOVE INSTRUCTION <====
4718                                ;          WHICH FOLLOWS W/ 732 <====
4719 013030
4720 013030 012742 000304      ADD7:   MOV      #304, -(R2) ;MOVE TO MAILBOX # ***** 304 *****
4721 013034 005242              INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4722 013036 000000              HALT                    ;ADD DID NOT SET CC'S CORRECTLY
4723 013040 000277      ADD8:   SCC
4724 013042 000245              +CLC!CLZ                ;CC=1010
4725 013044 062700 000001      ADD     #1, R0          ;CC=0101 R=0
4726 013050 102403              BVS     ADD9
4727 013052 103002              BCC     ADD9
4728 013054 100401              BMI     ADD9
4729 013056 001404              BEQ     TST152
4730                                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4731                                ;          CONDITIONAL BRANCH INST. AND <====
4732                                ;          REPLACE THE MOVE INSTRUCTION <====
4733                                ;          WHICH FOLLOWS W/ 716 <====
4734 013060
4735 013060 012742 000305      ADD9:   MOV      #305, -(R2) ;MOVE TO MAILBOX # ***** 305 *****
4736 013064 005242              INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4737 013066 000000              HALT                    ;ADD DID NOT SET CC'S CORRECTLY
4738                                ; OR SEQUENCE ERROR
4739
4740 ;*****
4741 ;TEST 152 TEST ADC INSTRUCTION
4742 ;*****
4743 013070 005212      TST152: INC      (R2)          ;UPDATE TEST NUMBER
4744 013072 022712 000152      CMP     #152, (R2)      ;SEQUENCE ERROR?
4745 013076 001037              BNE     TST153-10      ;BR TO ERROR HALT ON SEQ ERROR
4746 013100 012700 077777      MOV     #077777, R0
4747 013104 000277              SCC
4748 013106 000252              +CLN!CLV                ;CC=0101
4749 013110 005500              ADC     R0              ;CC=1010
4750 013112 101402              BLOS    ADC1
4751 013114 102001              BVC     ADC1
4752 013116 100404              BMI     ADC2
4753                                ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4754                                ;          CONDITIONAL BRANCH INST. AND <====
4755                                ;          REPLACE THE MOVE INSTRUCTION <====
4756                                ;          WHICH FOLLOWS W/ 770 <====
4757 013120
4758 013120 012742 000306      ADC1:   MOV      #306, -(R2) ;MOVE TO MAILBOX # ***** 306 *****
4759 013124 005242              INC      -(R2)          ;SET MSGTYP TO FATAL ERROR
4760 013126 000000              HALT                    ;ADC DID NOT SET CC'S CORRECTLY
4761 013130 052700 077777      ADC2:   BIS      #77777, R0
4762 013134 000277              SCC
4763 013136 000244              CLZ

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4764 013140 005500          ADC      R0          ;CC=0101  RO=0
4765 013142 101002          BHI      ADC3
4766 013144 102401          BVS      ADC3
4767 013146 100004          BPL      ADC4
4768                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4769                                     ; CONDITIONAL BRANCH INST. AND <====
4770                                     ; REPLACE THE MOVE INSTRUCTION <====
4771                                     ; WHICH FOLLOWS W/ 754 <====
4772 013150          ADC3:  MOV      #307, -(R2) ;MOVE TO MAILBOX # ***** 307 *****
4773 013150 012742 000307    INC      -(R2) ;SET MSGTYP TO FATAL ERROR
4774 013154 005242          HALT    ;ADC DID NOT SET CC'S CORRECTLY
4775 013156 000000          SCC
4776 013160 000277          ADC4:  +CLZ!CLC ;CC=1010
4777 013162 000245          ADC      R0          ;CC=0100
4778 013164 005500          BVS      ADC5
4779 013166 102403          BCS      ADC5
4780 013170 103402          BMI      ADC5
4781 013172 100401          BEQ      TST153
4782 013174 001404
4783                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4784                                     ; CONDITIONAL BRANCH INST. AND <====
4785                                     ; REPLACE THE MOVE INSTRUCTION <====
4786                                     ; WHICH FOLLOWS W/ 741 <====
4787 013176          ADC5:  MOV      #310, -(R2) ;MOVE TO MAILBOX # ***** 310 *****
4788 013176 012742 000310    INC      -(R2) ;SET MSGTYP TO FATAL ERROR
4789 013202 005242          HALT    ;ADC DID NOT SET CC'S CORRECTLY
4790 013204 000000          ; OR SEQUENCE ERROR
4791

```


THESE NEXT THREE TESTS VERIFY THE FUNCTIONING OF THE NEG,
 CMP, AND COM INSTRUCTIONS. EACH OF THESE INSTRUCTIONS GENERATE
 THE C AND V BITS IDENTICALLY. THE CONDITION CODES ARE PRESET
 THE INSTRUCTIONS EXECUTED, AND THE RESULTS CHECKED WITH A SERIES
 OF CONDITIONAL BRANCH INSTRUCTIONS. THIS PROCEDURE IS REPEATED
 SEVERAL TIMES WITH DIFFERENT DATA IN ORDER TO GENERATE DIFFERENT
 COMBINATIONS OF THE C AND V BITS.

TEST 153 TEST NEG INSTRUCTION

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*****
TEST153: INC      (R2)          ;UPDATE TEST NUMBER
          CMP      #153,(R2)   ;SEQUENCE ERROR?
          BNE     TST154-10   ;BR TO ERROR HALT ON SEQ ERROR
          MOV     #1,R0
          SCC
          +CLN!CLC           ;CC=0110
          NEG     RO          ;CC=1001 RO=177777
          BCC     NEG1
          BVS     NEG1
          BEQ     NEG1
          BMI     NEG2
          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
          ; CONDITIONAL BRANCH INST. AND (====
          ; REPLACE THE MOVE INSTRUCTION (====
          ; WHICH FOLLOWS W/ 767 (====

          NEG1: MOV     #311,-(R2) ;MOVE TO MAILBOX # ***** 311 *****
          INC     -(R2)          ;SET MSGTYP TO FATAL ERROR
          HALT
          NEG2: BIC     #77777,R0 ;NEG DID NOT SET CC'S CORRECTLY
          CCC
          SEZ
          NEG     RO          ;CC=0100
          BVC     NEG3
          BCC     NEG3
          BEQ     NEG3
          BMI     NEG4
          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====
          ; CONDITIONAL BRANCH INST. AND (====
          ; REPLACE THE MOVE INSTRUCTION (====
          ; WHICH FOLLOWS W/ 752 (====

          NEG3: MOV     #312,-(R2) ;MOVE TO MAILBOX # ***** 312 *****
          INC     -(R2)          ;SET MSGTYP TO FATAL ERROR
          HALT
          NEG4: CLR     RO
          SCC
          CLZ
          NEG     RO          ;CC=0100 RO=0
          BVS     NEG5
          BCS     NEG5
          BNE     NEG5
  
```

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4848 013320 100004
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4851
4852
4853 013322
4854 013322 012742 000313
4855 013326 005242
4856 013330 000000
4857
4858
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4862 013332 005212
4863 013334 022712 000154
4864 013340 001060
4865 013342 012700 000005
4866 013346 000257
4867 013350 000271
4868 013352 022700 000005
4869 013356 101002
4870 013360 102401
4871 013362 100004
4872
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4876 013364
4877 013364 012742 000314
4878 013370 005242
4879 013372 000000
4880 013374 012700 100000
4881 013400 000277
4882 013402 000242
4883 013404 020027 077777
4884 013410 101402
4885 013412 102001
4886 013414 100004
4887
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4891 013416
4892 013416 012742 000315
4893 013422 005242
4894 013424 000000
4895 013426 052700 040000
4896 013432 000257
4897 013434 000264
4898 013436 022700 040000
4899 013442 102003
4900 013444 103002
4901 013446 001401
4902 013450 100404
4903

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BPL TST154
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 736 <====

NEG5:
MOV #313, -(R2) ; MOVE TO MAILBOX # ***** 313 *****
INC -R2 ; SET MSGTYP TO FATAL ERROR
HALT ; NEG DID NOT SET CC'S CORRECTLY
; OR SEQUENCE ERROR

;*****
;TEST 154 TEST CMP INSTRUCTION
;*****
*ST154: INC (R2) ; UPDATE TEST NUMBER
CMP #154, (R2) ; SEQUENCE ERROR?
BNE TST155-10 ; BR TO ERROR HALT ON SEQ ERROR
MOV #5, R0
CCC ; CC=1010
+SEN!SEC
CMP #5, R0 ; CC=0101
BHI CMP1
BVS CMP1
BPL CMP2

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====

CMP1:
MOV #314, -(R2) ; MOVE TO MAILBOX # ***** 314 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CMP DID NOT SET CC'S CORRECTLY

CMP2:
MOV #100000, R0
SCC ; CC=1101
CLV
CMP R0, #77777 ; CC=0010
BLOS CMP3
BVC CMP3
BPL CMP4

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 752 <====

CMP3:
MOV #315, -(R2) ; MOVE TO MAILBOX # ***** 315 *****
INC -(R2) ; SET MSGTYP TO FATAL ERROR
HALT ; CMP DID NOT SET CC'S CORRECTLY

CMP4:
BIS #40000, R0 ; RO=140000
CCC ; CC=0100
SEZ
CMP #40000, R0 ; CC=1011
BVC CMP5
BCC CMP5
BEQ CMP5
BMI CMP6

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====

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4907 013453 012742 000316  CMPS:  MO. #316, -(R2)  :MOVE TO MAILBOX # ***** 316 *****
4908 013454 005242  :INC -(R2)  :SET MSGTYP TO FATAL ERROR
4909 013455 000000  :HALT  :CMP DID NOT SET CC'S CORRECTLY
4910 013456 042700 040000  CMPB:  BIC #40000,R0
4911 013457 000277  :SCC :CC=1111
4912 013458 022700 177777  CMP  # -1,R0 :CC=0000
4913 013470 101402  BLOS CMP?
4914 013474 102401  BVS CMP?
4915 013476 100004  BPL TST155
4916
4917 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4918 : CONDITIONAL BRANCH INST. AND <====
4919 : REPLACE THE MOVE INSTRUCTION <====
4920 : WHICH FOLLOWS W/ 720 <====
4921 013502 012742 000317  CMP7:  MOV #317, -(R2)  :MOVE TO MAILBOX # ***** 317 *****
4922 013502 005242  :INC -(R2)  :SET MSGTYP TO FATAL ERROR
4923 013506 000000  :HALT  :CMP DID NOT SET CC'S CORRECTLY
4924 013510  :OR SEQUENCE ERROR
4925
4926 *****
4927 :TEST 155 TEST COM INSTRUCTION
4928 *****
4929
4930 013512 005212 000155  TST155: INC (R2)  :UPDATE TEST NUMBER
4931 013514 022712  :CMP #155,(R2)  :SEQUENCE ERROR?
4932 013520 001010  :BNE TST156-10 :BR TO ERROR HALT ON SEQ ERROR
4933 013522 012700 177777  :MOV # -1,R0
4934 013526 000257  :CCC :CC=1010
4935 013530 000265  +SEC!SEZ
4936 013532 005100  :COM R0 :CC=0101
4937 013534 101002  :BHI COM1
4938 013536 102401  :BVS COM1
4939 013540 100004  :BPL TST156
4940
4941 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
4942 : CONDITIONAL BRANCH INST. AND <====
4943 : REPLACE THE MOVE INSTRUCTION <====
4944 : WHICH FOLLOWS W/ 770 <====
4945 013542 012742 000320  COM1:  MOV #320, -(R2)  :MOVE TO MAILBOX # ***** 320 *****
4946 013542 005242  :INC -(R2)  :SET MSGTYP TO FATAL ERROR
4947 013550 000000  :HALT  :COM DID NOT SET CC'S CORRECTLY
4948 :OR SEQUENCE ERROR
4949

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CGARPP

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*****
THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE SUB
AND SBC INSTRUCTIONS. BOTH OF THESE INSTRUCTIONS HANDLE THE
C AND V BITS IDENTICALLY. THE PROCEDURE IS TO PRESET THE CONDITION
CODES, EXECUTE THE INSTRUCTION WITH A PARTICULAR SET OF DATA, AND
THEN CHECK THE RESULTS BY EXECUTING A SERIES OF CONDITIONAL
BRANCHES. THIS PROCEDURE IS REPEATED SEVERAL TIMES WITH DIFFERENT
DATA PATTERNS TO PROVIDE EVERY COMBINATION OF THE C AND V BITS.
*****
TEST 156      TEST SUB INSTRUCTION
*****
ST156: INC      (R2)          ;UPDATE TEST NUMBER
          CMP      #156,(R2)   ;SEQUENCE ERROR?
          BNE     TST157-10    ;BR TO ERROR HALT ON SEQ ERROR
          MOV     #125252,R0
          CCC
          +SEN!SEC          ;CC=1010
          SUB     #125252,R0   ;CC=0101  RO=0
          BHI     SUB1
          BVS     SUB1
          BPL     SUB2
          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
          ;          CONDITIONAL BRANCH INST. AND   <====
          ;          REPLACE THE MOVE INSTRUCTION  <====
          ;          WHICH FOLLOWS W/ 767          <====
SUB1: MOV     #321,-(R2)      ;MOVE TO MAILBOX # ***** 321 *****
          INC     -(R2)
          HALT
          ;SET MSGTYP TO FATAL ERROR
          ;SUB DID NOT SET CC'S CORRECTLY
SUB2: BIS     #100000,R0
          SCC
          ;CC=1101
          CLV
          SUB     #77777,R0   ;CC=0010  RO=1
          BLOS   SUB3
          BVC     SUB3
          BPL     SUB4
          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
          ;          CONDITIONAL BRANCH INST. AND   <====
          ;          REPLACE THE MOVE INSTRUCTION  <====
          ;          WHICH FOLLOWS W/ 752          <====
SUB3: MOV     #322,-(R2)      ;MOVE TO MAILBOX # ***** 322 *****
          INC     -(R2)
          HALT
          ;SET MSGTYP TO FATAL ERROR
SUB4: COM     R0
          SCC
          ;RO=177777
          ;CC=11111
          SUB     #100000,R0   ;CC=0000  RO=77777
          BLOS   SUB5
          BVS     SUB5
          BPL     SUB6
          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  <====
          ;          CONDITIONAL BRANCH INST. AND   <====

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013552 005212
013554 022712 000156
013560 001055
013562 012700 125252
013566 000257
013570 000271
013572 162700 125252
013576 101002
013600 102401
013602 100004
013604
013604 012742 000321
013610 005242
013612 000000
013614 052700 100000
013620 000277
013622 000242
013624 162700 077777
013630 101402
013632 102001
013634 100004
013636
013636 012742 000322
013642 005242
013644 000000
013646 005100
013650 000277
013652 162700 100000
013656 101402
013660 102401
013662 100004

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5006                                     :                                     (=====
5007                                     :                                     (=====
5008 013664                               SUB5:                                     (=====
5009 013664 012742 000323                MOV      #323, -(R2)                ; MOVE TO MAILBOX # ***** 323 *****
5010 013670 005242                        INC      -(R2)                    ; SET MSGTYP TO FATAL ERROR
5011 013672 000000                        HALT                                     ; SUB DID NOT SET CC'S CORRECTLY
5012 013674 000257                               SUB6:                ; CC=0100
5013 013676 000264                               SEZ                                     ;
5014 013700 162700 140000                SUB      #140000, R0                ; CC=1011
5015 013704 102003                        BVC     SUB7
5016 013706 103002                        BCC     SUB7
5017 013710 001401                        BEQ     SUB7
5018 013712 100404                        BMI     TST157
5019                                     :                                     (=====
5020                                     : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
5021                                     : CONDITIONAL BRANCH INST. AND (=====
5022                                     : REPLACE THE MOVE INSTRUCTION (=====
5023                                     : WHICH FOLLOWS W/ 737 (=====
5024 013714                               SUB7:                                     (=====
5025 013714 012742 000324                MOV      #324, -(R2)                ; MOVE TO MAILBOX # ***** 324 *****
5026 013720 005242                        INC      -(R2)                    ; SET MSGTYP TO FATAL ERROR
5027 013722 000000                        HALT                                     ;
5028 ;*****
5029 ;TEST 157 TEST SBC INSTRUCTION
5030 ;*****
5031 013724 005212                               TST157: INC      (R2)                ; UPDATE TEST NUMBER
5032 013726 022712 000157                CMP      #157, (R2)                ; SEQUENCE ERROR?
5033 013732 001053                        BNE     TST160-10                ; BR TO ERROR HALT ON SEQ ERROR
5034 013734 012700 000001                MOV      #1, R0
5035 013740 000277                               SCC                                     ; CC=1011
5036 013742 000244                               CLZ
5037 013744 005600                        SBC     R0                        ; CC=0100 R=0
5038 013746 103403                        BCS     SBC1
5039 013750 102402                        BVS     SBC1
5040 013752 100401                        BMI     SBC1
5041 013754 001404                        BEQ     SBC2
5042                                     :                                     (=====
5043                                     : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
5044                                     : CONDITIONAL BRANCH INST. AND (=====
5045                                     : REPLACE THE MOVE INSTRUCTION (=====
5046                                     : WHICH FOLLOWS W/ 767 (=====
5047 013756                               SBC1:                                     (=====
5048 013756 012742 000325                MOV      #325, -(R2)                ; MOVE TO MAILBOX # ***** 325 *****
5049 013762 005242                        INC      -(R2)                    ; SET MSGTYP TO FATAL ERROR
5050 013764 000000                        HALT                                     ; SBC DID NOT SET CC'S CORRECTLY
5051 013766 000277                               SBC2:                ; CC=1010
5052 013770 000245                               SCC
5053 013772 005600                               +CLZ!CLC
5054 013774 103403                        SBC     R0                        ; CC=0100 R=0
5055 013776 102402                        BCS     SBC3
5056 014000 100401                        BVS     SBC3
5057 014002 001404                        BMI     SBC3
5058                                     :                                     (=====
5059                                     : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
5060                                     : CONDITIONAL BRANCH INST. AND (=====
5061                                     : REPLACE THE MOVE INSTRUCTION (=====
5061 014004                               SBC3:                ; WHICH FOLLOWS W/ 754 (=====

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000000.P11 T15 TEST SBC INSTRUCTION

5062	014004	012742	000326	MOV	#326, -(R2)	; MOVE TO MAILBOX # ***** 326 *****	
5063	014010	005242		INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
5064	014012	000000		HALT		; SBC DID NOT SET CC'S CORRECTLY	
5065	014014	000277		SBC4: SCC		; CC=0111	
5066	014016	000250		CLN			
5067	014020	005600		SBC	RO	; CC=1001 RO=177777	
5068	014022	103003		SBC	SBC5		
5069	014024	102402		BVS	SBC5		
5070	014026	001401		SEQ	SBC5		
5071	014030	100404		BMI	SBC6		
5072						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
5073						CONDITIONAL BRANCH INST. AND	<=====
5074						REPLACE THE MOVE INSTRUCTION	<=====
5075						WHICH FOLLOWS W/ 741	<=====
5076	014032			SBC5: MOV	#327, -(R2)	; MOVE TO MAILBOX # ***** 327 *****	
5077	014032	012742	000327	INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
5078	014036	005242		HALT		; SBC DID NOT SET CC'S CORRECTLY	
5079	014040	000000		SBC6: BIC	#777777, RO	; RO=100000	
5080	014042	042700	077777	SCC		; CC=1101	
5081	014046	000277		CLV			
5082	014050	000242		SBC	RO	; CC=0010	
5083	014052	005600		BLOS	SBC7		
5084	014054	101402		BVC	SBC7		
5085	014056	102001		BPL	TST160		
5086	014060	100004				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
5087						CONDITIONAL BRANCH INST. AND	<=====
5088						REPLACE THE MOVE INSTRUCTION	<=====
5089						WHICH FOLLOWS W/ 725	<=====
5090							
5091	014062			SBC7: MOV	#330, -(R2)	; MOVE TO MAILBOX # ***** 330 *****	
5092	014062	012742	000330	INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
5093	014066	005242		HALT		; SBC DID NOT SET CC'S CORRECTLY	
5094	014070	000300				; OR SEQUENCE ERROR	
5095							
5096							

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014072 005212
014074 022712 000160
014100 001053
014102 012700 144000
014106 000257
014110 000266
014112 006100
014114 103003
014116 102402
014120 001401
014122 100404

014124
014124 012742 000331
014130 005242
014132 000000
014134 000277
014136 000243
014140 006100
014142 103003
014144 102002
014146 001401
014150 100004

014152
014152 012742 000332
014156 005242
014160 000000
014162 000277
014164 000250
014166 006100
014170 101402
014172 102401
014174 100004

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*****
:
: THESE NEXT FOUR TESTS VERIFY THE FUNCTIONING OF THE ROL
: ROR, ASL AND ASR INSTRUCTIONS. SPECIAL DATA PATTERNS ARE LOADED
: AND ROTATED SEVERAL TIMES FOR EACH TEST. THE CONDITION CODES
: ARE PRESET BEFORE EACH ROTATION AND THE CONDITION CODES ARE
: CHECKED AFTER EACH ROTATION. THE FINAL CHECK IN EACH TEST IS
: TO VERIFY THE COMMULATIVE DATA RESULT. THE DATA PATTERNS HAVE
: BEEN SELECTED TO PRODUCE ALL COMBINATIONS OF THE C AND V BITS.
:
: *****
: TEST 160 TEST ROL INSTRUCTION
: *****
: TEST160: INC (R2) ;UPDATE TEST NUMBER
: CMP #160,(R2) ;SEQUENCE ERROR?
: BNE TST161-10 ;BR TO ERROR HALT ON SEQ ERROR
: MOV #144000,R0 ;RO=144000
: CCC ;CC=0110
: +SEZ!SEV
: ROL R0 ;CC=1001 RO=110000
: BCC ROL1
: BVS ROL1
: BEQ ROL1
: BMI ROL2
:
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 767 <====
:
: ROL1: MOV #331, -(R2) ;MOVE TO MAILBOX # ***** 331 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT
: ROL2: SCC ;CC=1100
: +CLV!CLC
: ROL R0 ;CC=0011 RO=020000
: BCC ROL3
: BVC ROL3
: BEQ ROL3
: BPL ROL4
:
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
: ; REPLACE THE MOVE INSTRUCTION <====
: ; WHICH FOLLOWS W/ 754 <====
:
: ROL3: MOV #332, -(R2) ;MOVE TO MAILBOX # ***** 332 *****
: INC -(R2) ;SET MSGTYP TO FATAL ERROR
: HALT ;ROL DID NOT SET CC'S CORRECTLY
: ROL4: SCC ;CC=0111
: CLN
: ROL R0 ;CC=0000 RO=040001
: BLOS ROL5
: BVS ROL5
: BPL ROL6
:
: ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: ; CONDITIONAL BRANCH INST. AND <====
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5153                                     :
5154                                     :
5155 014176                                ROL5:
5156 014176 012742 000333                MOV    #333, -(R2)      ; MOVE TO MAILBOX # ***** 333 *****
5157 014202 005242                        INC    -(R2)           ; SET MSGTYP TO FATAL ERROR
5158 014204 000000                        HALT                                     ; ROL DID NOT SET CC'S CORRECTLY
5159 014206 000257                                ROL6: CCC           ; CC=0101
5160 014210 000265                        +SEZ!SEC
5161 014212 006100                        ROL    RO             ; CC=1010  RO=100003
5162 014214 101405                        BLOS   ROL7
5163 014216 102004                        BVC    ROL7
5164 014220 100003                        BPL    ROL7
5165 014222 022700 100003                CMP    #100003, RO
5166 014226 001404                        BEQ    TST161
5167                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5168                                     ; CONDITIONAL BRANCH INST. AND <====
5169                                     ; REPLACE THE MOVE INSTRUCTION <====
5170                                     ; WHICH FOLLOWS W/ 742 <====
5171 014230                                ROL7:
5172 014230 012742 000334                MOV    #334, -(R2)      ; MOVE TO MAILBOX # ***** 334 *****
5173 014234 005242                        INC    -(R2)           ; SET MSGTYP TO FATAL ERROR
5174 014236 000000                        HALT                                     ; ROL MALFUNCTIONED
5175                                     ; OR SEQUENCE ERROR
5176
5177 ;*****
5178 ;TEST 161 TEST ROR INSTRUCTION
5179 ;*****
5180 014240 005212                                TST161: INC (R2)      ; UPDATE TEST NUMBER
5181 014242 022712 000161                CMP    #161, (R2)      ; SEQUENCE ERROR?
5182 014246 001051                                BNE    TST162-10      ; BR TO ERROR HALT ON SEQ ERROR
5183 014250 012700 000023                MOV    #23, RO        ; RO=23
5184 014254 000277                                SCC                                     ; CC=0111
5185 014256 000250                                CLN
5186 014260 006000                                ROR    RO             ; CC=1001  RO=100011
5187 014262 102403                                BVS   ROR1
5188 014264 103002                                BCC   ROR1
5189 014266 001401                                BEQ   ROR1
5190 014270 100404                                BMI   ROR2
5191                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5192                                     ; CONDITIONAL BRANCH INST. AND <====
5193                                     ; REPLACE THE MOVE INSTRUCTION <====
5194                                     ; WHICH FOLLOWS W/ 767 <====
5195 014272                                ROR1:
5196 014272 012742 000335                MOV    #335, -(R2)      ; MOVE TO MAILBOX # ***** 335 *****
5197 014276 005242                        INC    -(R2)           ; SET MSGTYP TO FATAL ERROR
5198 014300 000000                        HALT                                     ; ROR DID NOT SET CC'S CORRECTLY
5199 014302 000257                                ROR2: CCC           ; CC=1100
5200 014304 000274                        +SEN!SEZ
5201 014306 006000                                ROR    RO             ; CC=0011  RO=040004
5202 014310 102003                        BVC    ROR3
5203 014312 103002                        BCC    ROR3
5204 014314 001401                        BEQ    ROR3
5205 014316 100004                        BPL    ROR4
5206                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5207                                     ; CONDITIONAL BRANCH INST. AND <====
5208                                     ; REPLACE THE MOVE INSTRUCTION <====

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5209
5210 014320 ROR3: ; WHICH FOLLOWS W/ 754 =====
5211 014320 012742 000336 MOV #336,-(R2) ;MOVE TO MAILBOX # ***** 336 *****
5212 014324 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
5213 014326 000000 HALT ;ROR DID NOT SET CC'S CORRECTLY
5214 014330 000277 ROR4: SCC ;CC=1110
5215 014332 000241 CLC
5216 014334 006000 ROR RO ;CC=0000 RO=020002
5217 014336 101403 BLOS ROR5
5218 014340 102402 BVS ROR5
5219 014342 001401 BEQ ROR5
5220 014344 100004 BPL ROR5
5221 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (<====
5222 ; CONDITIONAL BRANCH INST. AND (<====
5223 ; REPLACE THE MOVE INSTRUCTION (<====
5224 ; WHICH FOLLOWS W/ 741 (<====
5225 014346 ROR5:
5226 014346 012742 000337 MOV #337,-(R2) ;MOVE TO MAILBOX # ***** 337 *****
5227 014352 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
5228 014354 000000 HALT ;ROR DID NOT SET CC'S CORRECTLY
5229 014356 000257 ROR6: CCC ;CC=0101
5230 014360 000265 +SEC!SEZ
5231 014362 006000 ROR RO ;CC=1010 RO=110001
5232 014364 101402 BLOS ROR7
5233 014366 102001 BVC ROR7
5234 014370 100404 BMI TST162
5235 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (<====
5236 ; CONDITIONAL BRANCH INST. AND (<====
5237 ; REPLACE THE MOVE INSTRUCTION (<====
5238 ; WHICH FOLLOWS W/ 727 (<====
5239 014372 ROR7:
5240 014372 012742 000340 MOV #340,-(R2) ;MOVE TO MAILBOX # ***** 340 *****
5241 014376 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
5242 014400 000000 HALT ;ROR DID NOT PRODUCE CORRECT RESULTS
5243 ; OR SEQUENCE ERROR
5244
5245 ;*****
5246 ;TEST 162 TEST ASL INSTRUCTION
5247 ;*****
5248 014402 005212 RST162: INC (R2) ;UPDATE TEST NUMBER
5249 014404 022712 000162 CMP #162,(R2) ;SEQUENCE ERROR?
5250 014410 001054 BNE TST163-10 ;BR TO ERROR HALT ON SEQ ERROR
5251 014412 012700 144000 MOV #144000,R0 ;RO=14000
5252 014416 000257 CCC ;CC=0110
5253 014420 000271 +SEN!SEC
5254 014422 006300 ASL RO ;CC=1001 RO=110000
5255 014424 103003 BCC ASL1
5256 014426 102402 BVS ASL1
5257 014430 001401 BEQ ASL1
5258 014432 100404 BMI ASL2
5259 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (<====
5260 ; CONDITIONAL BRANCH INST. AND (<====
5261 ; REPLACE THE MOVE INSTRUCTION (<====
5262 ; WHICH FOLLOWS W/ 767 (<====
5263 014434 ASL1:
5264 014434 012742 000341 MOV #341,-(R2) ;MOVE TO MAILBOX # ***** 341 *****

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5265 014440 005242      INC      -(R2)      ;SET MSGTYP TO FATAL ERKOR
5266 014442 000000      HALT
5267 014444 000277      ASL2:   SCC          ;CC=1100
5268 014446 000243      +CLV!CLC
5269 014450 006300      ASL     R0          ;CC=0011  R0=020000
5270 014452 103003      BCC     ASL3
5271 014454 102002      BVC     ASL3
5272 014456 001401      BEQ     ASL3
5273 014460 100004      BPL     ASL4
5274
5275      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5276      ;          CONDITIONAL BRANCH INST. AND <====
5277      ;          REPLACE THE MOVE INSTRUCTION <====
5278      ;          WHICH FOLLOWS W/ 754 <====
5278 014462      ASL3:
5279 014462 012742 000342      MOV     #342, -(R2) ;MOVE TO MAILBOX # ***** 342 *****
5280 014466 005242      INC     -(R2)      ;SET MSGTYP TO FATAL ERROR
5281 014470 000000      HALT      ;ASL DID NOT SET CC'S CORRECTLY
5282 014472 000277      ASL4:   SCC          ;CC=0111
5283 014474 000250      CLN
5284 014476 006300      ASL     R0          ;CC=0000  R0=040000
5285 014500 101402      BLOS   ASL5
5286 014502 102401      BVS     ASL5
5287 014504 100004      BPL     ASL6
5288
5289      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5290      ;          CONDITIONAL BRANCH INST. AND <====
5291      ;          REPLACE THE MOVE INSTRUCTION <====
5292      ;          WHICH FOLLOWS W/ 742 <====
5292 014506      ASL5:
5293 014506 012742 000343      MOV     #343, -(R2) ;MOVE TO MAILBOX # ***** 343 *****
5294 014512 005242      INC     -(R2)      ;SET MSGTYP TO FATAL ERROR
5295 014514 000000      HALT      ;ASL DID NOT SET CC'S CORRECTLY
5296 014516 000257      ASL6:   CCC          ;CC=0101
5297 014520 000265      +SEZ!SEC
5298 014522 006300      ASL     R0          ;CC=1010  R0=100000
5299 014524 103406      BCS     ASL7
5300 014526 001405      BEQ     ASL7
5301 014530 102004      BVC     ASL7
5302 014532 100003      BPL     ASL7
5303 014534 022700 100000      CMP     #100000, R0
5304 014540 001404      BEQ     TST163
5305
5306      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
5307      ;          CONDITIONAL BRANCH INST. AND <====
5308      ;          REPLACE THE MOVE INSTRUCTION <====
5309      ;          WHICH FOLLOWS W/ 724 <====
5309 014542      ASL7:
5310 014542 012742 000344      MOV     #344, -(R2) ;MOVE TO MAILBOX # ***** 344 *****
5311 014546 005242      INC     -(R2)      ;SET MSGTYP TO FATAL ERROR
5312 014550 000000      HALT      ;ASL MALFUNCTIONED
5313      ; OR SEQUENCE ERROR
5314
5315      ;*****
5316      ;TEST 163 TEST ASR INSTRUCTION
5317      ;*****
5318 014552 005212      TST163: INC     (R2)      ;UPDATE TEST NUMBER
5319 014554 022712 000163      CMP     #163, (R2)  ;SEQUENCE ERROR?
5320 014560 001060      BNE     TST164-10  ;BR TO ERROR HALT ON SEQ ERROR

```

5321	014562	012700	100023		MOV	#100023,RO		;RO=100023	
5322	014566	000277			SCC			;CC=0110	
5323	014570	000250			CLN				
5324	014572	006200			ASR	RO		;CC=1001	RP=140011
5325	014574	102403			BVS	ASR1			
5326	014576	103002			BCC	ASR1			
5327	014600	001401			BEQ	ASR1			
5328	014602	100404			BMI	ASR2			
5329									
5330									
5331									
5332									
5333	014604			ASR1:					
5334	014604	012742	000345		MOV	#345, -(R2)		;MOVE TO MAILBOX #	***** 345 *****
5335	014610	005242			INC	-(R2)		;SET MSGTYP TO FATAL ERROR	
5336	014612	000000			HALT			;ASR DID NOT SET CC'S CORRECTLY	
5337	014614	042700	100000	ASR2:	BIC	#100000,RO		;RO=40011	
5338	014620	000277			SCC			;CC=1100	
5339	014622	000243			+CLV!CLC				
5340	014624	006200			ASR	RO		;CC=0011	RO=020004
5341	014626	102003			BVC	ASR3			
5342	014630	103002			BCC	ASR3			
5343	014632	001401			BEQ	ASR3			
5344	014634	100004			BPL	ASR4			
5345									
5346									
5347									
5348									
5349	014636			ASR3:					
5350	014636	012742	000346		MOV	#346, -(R2)		;MOVE TO MAILBOX #	***** 346 *****
5351	014642	005242			INC	-(R2)		;SET MSGTYP TO FATAL ERROR	
5352	014644	000000			HALT			;ASR DID NOT SET CC'S CORRECTLY	
5353	014646	000277		ASR4:	SCC			;CC=1111	
5354									
5355	014650	006200			ASR	RO		;CC=0000	RO=C10002
5356	014652	101403			BLOS	ASR5			
5357	014654	102402			BVS	ASR5			
5358	014656	001401			BEQ	ASR5			
5359	014660	100004			BPL	ASR6			
5360									
5361									
5362									
5363									
5364	014662			ASR5:					
5365	014662	012742	000347		MOV	#347, -(R2)		;MOVE TO MAILBOX #	***** 347 *****
5366	014666	005242			INC	-(R2)		;SET MSGTYP TO FATAL ERROR	
5367	014670	000000			HALT			;ASR DID NOT SET CC'S CORRECTLY	
5368	014672	052700	100000	ASR6:	BIS	#100300,RO		;RO=110002	
5369	014676	000257			CCC			;CC=0101	
5370	014700	000265			+SEZ!SEC				
5371	014702	006200			ASR	RO		;C=1010	RO=144001
5372	014704	101406			BLOS	ASR7			
5373	014706	102005			BVC	ASR7			
5374	014710	100004			BPL	ASR7			
5375	014712	001403			BEQ	ASR7			
5376	014714	022700	144001		CMF	#144001,RO		;CHECK RESULT OF ASR'S	

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 767 <====

```

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 752 <====

```

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
; CONDITIONAL BRANCH INST. AND <====
; REPLACE THE MOVE INSTRUCTION <====
; WHICH FOLLOWS W/ 740 <====

```

5377 014720 001404
5378
5379
5380
5381
5382 014722
5383 014722 012742 000350
5384 014726 005242
5385 014730 000000
5386
5387
5388

BEO TST164

ASR7:

MOV *350, -(R2)
INC -(R2)
HALT

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
: CONDITIONAL BRANCH INST. AND <====
: REPLACE THE MOVE INSTRUCTION <====
: WHICH FOLLOWS W/ 720 <====

: MOVE TO MAILBOX # ***** 350 *****
: SET MSGTYP TO FATAL ERROR
: ASR DID NOT FUNCTION CORRECTLY
: OR SEQUENCE ERROR

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5444

014732 005212
014734 022712 000164
014740 001062
014742 012700 015332
014746 012704 015370
014752 012767 000015 000142
014760 012067 000110
014764 012401
014766 012767 177777 000074
014774 012703 000016
015000 005267 000064
015004 032701 100000
015010 013705 177776
015014 042705 177773
015020 000165 015024
015024 000167 000020
015030 012767 015124 000042
015036 012767 015106 000040
015044 000167 000014
015050 012767 015106 000022
015056 012767 015124 000020
015064 006101

015066 012737
015070 000000
015072 177776
015074 000000
015076 000137
015100 000000

THIS TEST VERIFIES THE CONTENTS OF THE BRANCH ROM. THE TEST
EXECUTES EVERY POSSIBLE BRANCH WITH EVERY POSSIBLE CONDITION
CODE COMBINATION.
THE ROUTINE USES TWO TABLES. THE BRANCH TABLE HOLDS ALL THE
POSSIBLE BRANCH INSTRUCTIONS. THE OTHER TABLE (YNTAB) HOLDS BIT MAPS FOR
EACH BRANCH. A ONE IN THE BIT MAP INDICATES THAT THE CORRESPONDING
BRANCH INSTRUCTION SHOULD BRANCH FOR THE CONDITION CODE SETTING WHICH
CORRESPONDS TO THE BIT POSITION WITHIN THE MAP. FOR EXAMPLE IF THE LEFT
MOST BIT IS A ONE THEN THE CORRESPONDING BRANCH INSTRUCTION SHOULD BRANCH
WHEN THE CONDITION CODES ARE 0.
THE ROUTINE CONSISTS OF NESTED LOOPS: THE OUTER LOOP SETS UP
ALL THE POSSIBLE BRANCH INSTRUCTIONS. THE INNER LOOP SETS UP EVERY POSSIBLE
CONDITION CODE FOR EACH BRANCH.
THE BIT MAP IS USED TO SET THE ADDRESS LOCATION IN TWO
JUMP MODE 3 INSTRUCTIONS. THE ADDRESSES ARE CHANGED TO ALLOW THE
PROGRAM TO CONTINUE OR JUMP TO AN ERROR ROUTINE DEPENDING UPON
WHETHER IT HANDLED THE BRANCH INSTRUCTION CORRECTLY.
AT ANY ERROR HALT, LOCATION, BRH, HOLDS THE BRANCH INSTRUCTION
UNDER TEST AND LOCATION, CC, HOLDS THE VALUE OF THE CONDITION CODES
AT THE TIME THE BRANCH WAS EXECUTED.

TEST 164 TEST THE BRANCH ROM

TST164: INC (R2) ;UPDATE TEST NUMBER
CMP #164,(R2) ;SEQUENCE ERROR?
BNE ER ;BR TO ERROR HALT ON SEQ ERROR
SETUP: MOV #BRTAB,R0 ;INITIALIZE BRANCH TABLE POINTER
MOV #YNTAB,R4 ;INITIALIZE YES/NO BRANCH MAP POINTER
MOV #15,BRCT ;INITIALIZE BRANCH TABLE COUNT
SETBR: MOV (R0)+,BRH ;GET NEXT BRANCH INST.
MOV (R4)+,R1 ;GET NEXT BRANCH MAP
MOV #-1,CC ;INITIALIZE CONDITION CODE VALUE
MOV #16,R3 ;INITIALIZE CONDITION CODE COUNT
SETCC: INC CC ;SET FOR NEXT CC VALUE
BIT #100000,R1 ;SEE IF SHOULD BR W/ THESE CC'S
MOV @#177776,R5 ;SIMULATE A JNE
BIC #177773,R5 ; (JUMP NOT EQUAL)
JMP .+4(R5) ; TO SET2BR
JMP SET2BR
MOV #CONT,NBR ;SET TO CONTINUE IF NO BRANCH
MOV #ER,YBR ;SET TO REPORT ERROR IF BRANCH
JMP AROUND ;GO AROUNDND OPPOSITE CONDITION
SET2BR: MOV #ER,NBR ;SET TO REPORT ERROR IF NO BRANCH
MOV #CONT,YBR ;SET TO CONTINUE IF BRANCH
AROUND: ROL R1 ;UPDATE BIT MAP

MOV (PC)+,@(PC)+ ;SET CONDITION CODE
CC: 0 ;NEW CC VALUE GOES HERE
BRH: 0 ;BRANCH INST. GOES HERE
JMP @ (PC)+ ;THIS JUMP IF NO BRANCH
NBR: 0 ;WHERE TO GO IF NO BRANCH OCCURS

```

5445 015102 000137
5446 015104 000000
5447 015106 012702 000304
5448 015112 012742 000351
5449 015116 005242
5450 015120 000000
5451 015122 000000
5452 015124 005303
5453 015126 013705 177776
5454 015132 042705 177773
5455 015136 000165 015142
5456 015142 000167 177632
5457 015146 005367 177750
5458 015152 013705 177776
5459 015156 042705 177773
5460 015162 000165 015166
5461 015166 000167 177566

```

```

YBR:
ER:
BRCT:
CCNT:

```

```

@ (PC)+
MOV #TESTN,R2
MOV #351,-(R2)
INC -(R2)
HALT
DEC R3
MOV @#177776,R5
BIC #177773,R5
JMP .+4(R5)
SETCC
DEC BRCT
MOV @#177776,R5
BIC #177773,R5
JMP .+4(R5)
SETBR

```

```

: THIS JUMP IF BRANCH OCCURS
: WHERE TO GO IF BRANCH OCCURS
: RESTORE POINTER
: MOVE TO MAILBOX # ***** 351 *****
: SET MSGTYP TO FATAL ERROR
:
: CC'S DONE?
: SIMULATE A JNE
: (JUMP NOT EQUAL)
: TO SETCC
:
: BR'S DONE?
: SIMULATE A JNE
: (JUMP NOT EQUAL)
: TO SETBR

```

```

5462
5463
5464
5465 015172 005212
5466 015174 022712 000165
5467 015200 001037
5468 015202 005237 000306
5469 015206 105267 000076
5470 015212 001020
5471 015214 132767 000040 163077
5472 015222 001014
5473 015224 023727 000042 015264
5474 015232 001410
5475 015234 012700 015312
5476 015240 105737 177564
5477 015244 100375
5478 015246 112037 177566
5479 015250 001372
5480 015254 013700 000042
5481 015260 001405
5482 015262 000005
5483 015264 004710
5484 015266 000240
5485 015270 000240
5486 015272 000240
5487 015274 000167 163222
5488 015300
5489 015300 012742 000352
5490 015304 005242
5491 015306 000000
5492 015310 177777
5493 015312 047105 020104 043117
5494 015320 042040 045507 040501
5495 015326 005015 000
    
```

```

:*****
:TEST 165      END OF PASS SEQUENCE
:*****
↑ST165: INC      (R2)          ;UPDATE TEST NUMBER
      CMP      #165,(R2)     ;SEQUENCE ERROR?
      BNE     EOP1         ;BR TO ERROR HALT ON SEQ EFROR
      INC     @#SPASS
      INCB    PASSPT       ;SHOULD PRINT THIS PASS?
      BNE     ACT         ;NO
      BITB   #40,$ENVM     ;WILL APT ALLOW PRINTING?
      BNE     ACT         ;NO
      CMP     @#42,#SENDAD ;UNDER ACT AUTO ACCEPT?
      BEQ     ACT         ;IF SO SKIP PRINTOUT
      MOV     #MSG,RO      ;GET MSG ADDR.
      TSTB   @#TPS        ;TTY READY
      BPL     WAIT        ;NO WAIT
      MOVB   (RO)+,@#TPB  ;PRINT CHARACTER
      BNE     WAIT        ;NEXT IF NOT DONE.
      MOV     @#42,RO     ;CHECK ACT
      BEQ     GOAGIN      ;KEEP GOING
      RESET
      JSR     PC,(RO)     ;ACT HOOKS
      NOP
      NOP
      NOP
      GOAGIN: JMP     RESTRT ;DO NEXT PASS
      EOP1:
      MOV     #352,-(R2)   ;MOVE TO MAILBOX # ***** 352 *****
      INC     -(R2)       ;SET MSGTYP TO FATAL ERROR
      HALT
      PASSPT: -1
      MSG:   .ASCIZ  .END OF DGKAA.<15><12>
    
```

```

5486      015332      .EVEN
5497
5498 015332 000402      BR      .+6
5499 015334 001002      BNE     .+6
5500 015336 001402      BEQ     .+6
5501 015340 002002      BGE     .+6
5502 015342 002402      BLT     .+6
5503 015344 003002      BGT     .+6
5504 015346 003402      BLE     .+6
5505 015350 100002      BPL     .+6
5506 015352 100402      BMI     .+6
5507 015354 101002      BHI     .+6
5508 015356 101402      BLOS    .+6
5509 015360 102002      BVC     .+6
5510 015362 102402      BVS     .+6
5511 015364 103002      BCC     .+6
5512 015366 103402      BCS     .+6
5513
5514      000002      .RADIX 2
5515 015370 177777      YNTAB: 1111111111111111      ;BR
5516 015372 170360      1111000011110000      ;BNE: Z=0
5517 015374 007417      0000111100001111      ;BEQ: Z=1
5518 015376 146063      1100110000110011      ;BGE: N XOR V =0
5519 015400 031714      0011001111001100      ;BLT: N XOR V =1
5520 015402 140060      1100000000110000      ;BGT: Z+(N XOR V) =0
5521 015404 037717      0011111111001111      ;BLE: Z+(N XOR V) =1
5522
5523 015406 177400      1111111100000000      ;BPL: N=0
5524 015410 000377      0000000011111111      ;BMI: N=1
5525 015412 120240      1010000010100000      ;BHI: C+Z=0
5526 015414 057537      0101111101011111      ;BLOS: C+Z=1
5527 015416 146314      1100110011001100      ;BVC: V=0
5528 015420 031463      0011001100110011      ;BVS: V=1
5529 015422 125252      1010101010101010      ;BCC: C=0
5530 015424 052525      0101010101010101      ;BCS: C=1
5531
5532      000010      .RADIX 8
5533 015426 012737 015436 000024 PWRDN: MOV      #PWRUP, @#24      ;SET UP FOR A POWER UP
5534 015434 000000      HALT
5535
5536 015436 012737 015426 000024 PWRUP: MOV      #PWRDN, @#24      ;SET UP FOR A POWER FAIL
5537 015444 012706 000500      MOV      #STBOT, R6      ;SET UP STACK POINTER
5538 015450 132767 000040 162643 BITB     #40, SENVM      ;SHOULD PRINT?
5539 015456 001010      BNE      PWR2      ;IF NOT: BR
5540 015460 012700 015504      MOV      #PFMES, R0      ;GET POWER FAIL MESSG.
5541 015464 105737 177564 WATE:   TSTB     @#TPS      ;TTY READY?
5542 015470 100375      BPL      WATE      ;IF NOT: BR
5543 015472 112037 177566      MOVB     (R0)+, @#TPB      ;PRINT NEXT CHAR.
5544 015476 001372      BNE      WATE      ;IF NOT DONE: BR
5545 015500 000137 000500 PWR2:   JMP      @#START      ;START PROGRAM AGAIN
5546
5547 015504 006412 047520 042527 PFMES: .ASCIZ (<12><15>).POWER FAILURE.<12><15>
5548 015512 020122 040506 046111
5549 015520 051125 005105 000015
5550
5551      000001      .END

```


RBASE =	000000	424			
ACDW1 =	000000	424			
ACDW2 =	000000	424			
ACPUOP =	000000	424	439		
ACT	015254	5470	5472	5474	5490#
ROC1	013120	4750	4751	4757#	
ROC2	013130	4752	4761#		
ROC3	013150	4765	4766	4772#	
ROC4	013160	4767	4776#		
ROC5	013176	4779	4780	4781	4787#
ROOM0 =	000000	424			
ROOM1 =	000000	424			
ROOM10 =	000000	424			
ROOM11 =	000000	424			
ROOM12 =	000000	424			
ROOM13 =	000000	424			
ROOM14 =	000000	424			
ROOM15 =	000000	424			
ROOM2 =	000000	424			
ROOM3 =	000000	424			
ROOM4 =	000000	424			
ROOM5 =	000000	424			
ROOM6 =	000000	424			
ROOM7 =	000000	424			
ROOM8 =	000000	424			
ROOM9 =	000000	424			
ADD1	012734	4672	4673	4679#	
ADD2	012744	4674	4683#		
ADD3	012760	4686	4687	4693#	
ADD4	012770	4688	4697#		
ADD5	013006	4700	4701	4707#	
ADD6	013016	4702	4711#		
ADD7	013030	4712	4713	4719#	
ADD8	013040	4714	4723#		
ADD9	013060	4726	4727	4728	4734#
ADEVCT =	000000	424	430		
ADEVN =	000000	424			
RENV =	000000	424	435		
RENVM =	000000	424	436		
AFATAL =	000000	424	427		
AMADR1 =	000000	424			
AMADR2 =	000000	424			
AMADR3 =	000000	424			
AMADR4 =	000000	424			
AMAMS1 =	000000	424			
AMAMS2 =	000000	424			
AMAMS3 =	000000	424			
AMAMS4 =	000000	424			
AMSGAD =	000000	424	432		
AMSGLG =	000000	424	433		
AMSGTY =	000000	424	426		
AMTYP1 =	000000	424			
AMTYP2 =	000000	424			
AMTYP3 =	000000	424			
AMTYP4 =	000000	424			
APASS =	000000	424	429		

APRIOR=	000000	424				
AROUND	015064	5434	5437#			
ASL1	014434	5255	5256	5257	5262#	
ASL2	014444	5258	5267#			
ASL3	014462	5270	5271	5272	5278#	
ASL4	014472	5273	5282#			
ASL5	014506	5285	5286	5292#		
ASL6	014516	5287	5296#			
ASL7	014542	5299	5300	5301	5302	5309#
ASR1	014604	5325	5326	5327	5333#	
ASR2	014614	5328	5337#			
ASR3	014636	5341	5342	5343	5349#	
ASR4	014646	5344	5353#			
ASR5	014662	5356	5357	5358	5364#	
ASR6	014672	5359	5368#			
ASR7	014722	5372	5373	5374	5375	5382#
ASUREG=	000000	424	437			
ATESTN=	000000	424	428			
AUNIT =	000000	424	431			
AUSMR =	000000	424	438			
AVECT1=	000000	424				
AVECT2=	000000	424				
BIC1	012064	4345	4346	4352#		
BIC2	012074	4347	4356#			
BIC3	012112	4359	4360	4366#		
BIS1	012154	4382	4383	4384	4390#	
BIS2	012164	4385	4394#			
BIS3	012204	4397	4398	4399	4405#	
BIT1	011774	4307	4308	4314#		
BIT2	012004	4309	4319#			
BIT3	012022	4322	4323	4329#		
BRC1	015122	5421#	5451#	5457#		
BRC2	002350	1228	1234#			
BRC3	002360	1229	1239#			
BR4	015074	5422#	5442#			
BRN1	002230	1134	1140#			
BRN2	002240	1135	1145#			
BRN3	002250	1147	1153#			
BRTAB	015332	5419	5498#			
BRV1	002300	1181	1187#			
BRV2	002310	1182	1192#			
BRV3	002320	1194	1200#			
BRZ1	002160	1087	1093#			
BRZ2	002170	1088	1098#			
BRZ3	002200	1100	1106#			
BR1	000572	504	510#			
BR2	000602	505	514#			
BR3	000614	515	523#			
BR4	000622	524	530#			
BRS	000632	525	534#			
CC	015070	5424#	5426#	5440#		
CLR1	012522	4563	4564	4565	4571#	
CMP1	013364	4869	4870	4876#		
CMP2	013374	4871	4880#			
CMP3	013416	4884	4885	4891#		

R0L6	014206	5150	5159*												
R0L7	014230	5162	5163	5164	5171*										
R0R1	014272	5187	5188	5189	5195*										
R0R2	014302	5190	5199*												
R0R3	014320	5202	5203	5204	5210*										
R0R4	014330	5205	5214*												
R0R5	014346	5217	5218	5219	5225*										
R0R6	014356	5220	5229*												
R0R7	014372	5232	5233	5239*											
ROT X	007710	3545	3547*	3551	3564*	3579*	3581*	3585	3598*	3609	3613				
ROTXAO	010034	3609*	3611*	3624*											
ROTOA	007026	3276	3277	3284*											
ROTOB	007036	3279	3288*												
ROTOC	007060	3291	3292	3299*											
ROTA A	007126	3324	3325	3332*											
ROTA B	007136	3327	3336*												
ROTA C	007162	3339	3340	3347*											
ROTA D	007172	3342	3351*												
ROTA E	007222	3356	3357	3364*											
ROTA F	007274	3387	3389	3397*											
ROTB	007304	3392	3401*												
ROTC	007334	3405	3407	3414*											
ROTD	007344	3409	3418*												
ROTE	007400	3423	3425	3433*											
ROTA G	007446	3455	3462*												
ROTA H	007456	3457	3466*												
ROTA I	007504	3469	3476*												
ROTA J	007514	3471	3480*												
ROTA K	007542	3483	3490*												
RCT4	007616	3514	3516	3523*											
ROTS	007700	3544	3550	3552-	3559*										
ROTB	007750	3582	3589*												
PCT7	010024	3607	3612	3619*											
RTS1	011640	4228	4235*												
PD	=:000000	665*	666	683*	684	701*	702	719*	720	1294*	1303*	1304*	1313*	1340*	
		1341*	1351*	1354*	1356*	1357*	1381*	1390*	1392*	1418*	1419*	1428*	1431*	1456*	
		1457*	1458*	1459*	1468*	1470*	1472*	1500*	1501*	1502*	1503*	1504*	1513*	1514*	
		1515*	1516*	1518*	1546*	1547*	1548*	1549*	1550*	1551*	1560*	1561*	1562*	1564*	
		1565*	1566*	1594*	1595*	1596*	1597*	1598*	1599*	1608*	1609*	1610*	1612*	1613*	
		1636*	1637*	1638*	1639*	1640*	1641*	1642*	1651*	1652*	1653*	1654*	1655*	1657*	
		1658*	1690*	1691*	1692*	1693*	1694*	1703*	1704*	1705*	1707*	1740*	1741*	1742*	
		1791*	1792*	1793*	1794*	1795*	1796*	1805*	1806*	1807*	1808*	1809*	1810*	1812*	
		1830*	1831*	1832*	1833*	1842*	1843*	1844*	1846*	1847*	1848*	1881*	1882*	1883*	
		1894*	1893*	1894*	1895*	1897*	1923*	1924*	1925*	1926*	1935*	1937*	1964*	1965*	
		1966*	1967*	1976*	1978*	2044*	2047	2076*	2077*	2080	2108*	2109*	2112	2140*	
		2141*	2142*	2145	2157*	2158*	2161	2189*	2190*	2193	2206*	2207*	2232*	2233*	
		2234*	2237	2249*	2258*	2258*	2261	2275*	2275*	2299*	2300*	2301*	2302*	2318*	
		2319*	2345*	2346*	2347*	2348*	2349*	2350	2353	2367	2380	2381	2405*	2406*	
		2407*	2410	2422	2446*	2447*	2448*	2449*	2450*	2453	2465*	2466*	2490*	2491*	
		2492*	2493*	2496	2508*	2532*	2533*	2534*	2535*	2538	2550*	2573*	2574*	2576	
		2600*	2602*	2603	2629*	2630	2639*	2640*	2642	2652	2663*	2664*	2667	2668	
		2678	2703*	2706	2715	2724*	2725	2734*	2735*	2737	2747	2771*	2772*	2776*	
		2799*	2800*	2801*	2803	2828*	2829*	2830*	2833	2861*	2862*	2863*	2864*	2867	
		2877*	2878	2902*	2903*	2907*	2908*	2932*	2933*	2934*	2935	2945*	2946*	2972*	
		2973*	2974*	2975*	3008*	3010*	3011*	3012*	3013	3023	3024	3050*	3051*	3052*	
		3077*	3078*	3079	3104*	3105*	3106	3135*	3136	3137	3138	3139	3140	3173*	

R1 =:000001
R2 =:000002

3174	3175	3176	3177	3178	3211*	3212	3213	3214	3215	3216	3243*	3244
3245	3246	3247	3248	3273*	3275*	3278	3288*	3290*	3293	3320*	332.*	3323*
3337*	3338*	3351*	3352*	3353*	3355*	3383*	3384*	3386*	3390*	3391*	3401*	3402*
3404*	3408*	3419*	3419*	3420*	3422*	3426*	3427*	3511*	3513*	3517	3546*	3549*
3553	3640*	3641*	3650	3675*	3676*	3703*	3704*	3714*	3767*	3768*	3778	3805*
3807*	3817	3848*	3849*	3850	3881*	3882*	3883	3936*	3937	3938	3956*	3958
3971*	3972	3973	3991*	3993	4004*	4006	4017*	4019	4031*	4033	4074*	4078
4094	4126*	4127	4142*	4143	4149	4165	4176*	4177	4228*	4229*	4235	4268*
4283*	4303*	4306	4321	4341*	4344*	4358*	4378*	4381*	4396*	4429*	4432*	4444*
4447*	4463*	4483*	4485*	4500*	4514*	4526*	4529*	4562*	4585	4598*	4601	4621*
4624*	4638*	4669*	4671*	4685*	4699*	4711*	4725*	4746*	4749*	4761*	4764*	4778*
4809*	4812*	4825*	4828*	4841*	4844*	4865*	4868	4880*	4883	4895*	4898	491.*
4913	4933*	4936*	4967*	4970*	4982*	4985*	4997*	5000*	5014*	5034*	5037*	5052*
5067*	5080*	5083*	5114*	5117*	5132*	5147*	5161*	5165	5183*	5186*	5201*	5216*
5231*	5251*	5254*	5269*	5284*	5298*	5303	5321*	5324*	5337*	5340*	5355*	5368*
5371*	5376	5419*	5422	5475*	5478	5480*	5483	5540*	5543			
737*	739*	4076*	4077*	4078*	4088	4105*	4109	4124*	4127*	4131	4143*	4147
4160*	4163	4177*	4181	4192*	4200	5423*	5427	5437*				
482*	493*	500*	501	511*	512*	520*	521*	531*	532*	540*	541*	562*
563	573*	574*	581*	582	592*	593*	600*	601	611*	612*	619*	620
629*	630*	661*	662	672*	673*	680*	681	690*	691*	698*	699	708*
709*	716*	717	726*	727*	734*	735	746*	747*	754*	755	757*	759*
766*	767*	768*	770*	774*	775	786*	787*	794*	795	806*	807*	814*
815	826*	827*	834*	835	846*	847*	870*	871	881*	882*	889*	890
899*	900*	907*	908	917*	918*	925*	926	935*	936*	958*	959	970*
971*	978*	979	989*	990*	999*	1000*	1007*	1008	1019*	1020*	1027*	1028
1039*	1040*	1047*	1048	1059*	1060*	1081*	1082	1094*	1095*	1107*	1108*	1128*
1129	1141*	1142*	1154*	1155*	1175*	1176	1188*	1189*	1201*	1202*	1222*	1223
1235*	1236*	1248*	1249*	1291*	1292	1300*	1301*	1310*	1311*	1319*	1320*	1337*
1338	1347*	1348*	1364*	1365*	1378*	1379	1387*	1388*	1399*	1400*	1415*	1416
1425*	1426*	1438*	1439*	1453*	1454	1465*	1466*	1479*	1480*	1497*	1498	1510*
1511*	1525*	1526*	1543*	1544	1557*	1558*	1573*	1574*	1591*	1592	1605*	1606*
1620*	1621*	1633*	1634	1648*	1649*	1665*	1666*	1687*	1688	1700*	1701*	1714*
1715*	1734*	1735	1749*	1750*	1767*	1768*	1788*	1789	1802*	1803*	1819*	1820*
1827*	1828	1839*	1840*	1855*	1856*	1878*	1879	1890*	1891*	1904*	1905*	1920*
1921	1932*	1933*	1944*	1945*	1961*	1962	1973*	1974*	1985*	1986*	2001*	2002
2011*	2012*	2024*	2025*	2041*	2042	2057*	2058*	2073*	2074	2089*	2090*	2105*
2106	2122*	2123*	2137*	2138	2154*	2155*	2171*	2172*	2186*	2187	2203*	2204*
2213*	2214*	2229*	2230	2246*	2247*	2255*	2256*	2271*	2272*	2281*	2282*	2296*
2297	2315*	2316*	2325*	2326*	2342*	2343	2362*	2363*	2377*	2378*	2387*	2388*
2402*	2403	2419*	2420*	2428*	2429*	2443*	2444	2462*	2463*	2472*	2473*	2487*
2488	2505*	2506*	2514*	2515*	2529*	2530	2547*	2548*	2556*	2557*	2570*	2571
2583*	2584*	2597*	2598	2610*	2611*	2626*	2627	2636*	2637*	2649*	2650*	2660*
2661*	2675*	2676*	2686*	2687*	2700*	2701	2712*	2713*	2721*	2722*	2731*	2732*
2743*	2744*	2753*	2754*	2768*	2769	2782*	2783*	2796*	2797	2810*	2811*	2825*
2826	2839*	2840*	2858*	2859	2874*	2875*	2884*	2885*	2899*	2900	2914*	2915*
2929*	2930	2942*	2943*	2952*	2953*	2969*	2970	2982*	2983*	2991*	2992*	3005*
3006	3020*	3021*	3030*	3031*	3046*	3047	3058*	3059*	3073*	3074	3085*	3086*
3100*	3101	3112*	3113*	3132*	3133	3147*	3148*	3170*	3171	3185*	3186*	3208*
3209	3222*	3223*	3240*	3241	3254*	3255*	3270*	3271	3285*	3286*	3300*	3301*
3317*	3318	3333*	3334*	3348*	3349*	3365*	3366*	3380*	3381	3398*	3399*	3415*
3416*	3434*	3435*	3449*	3450	3463*	3464*	3477*	3478*	3491*	3492*	3507*	3508
3524*	3525*	3542*	3543	3560*	3561*	3576*	3577	3590*	3591*	3605*	3606	3620*
3621*	3637*	3638	3647*	3648*	3656*	3657*	3671*	3672	3683*	3684*	3699*	3700
3711*	3712*	3720*	3721*	3736*	3737	3747*	3748*	3763*	3764	3775*	3776*	3784*
3785*	3802*	3803	3814*	3815*	3824*	3825*	3844*	3845	3857*	3858*	3877*	3878

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SNM81C	004330	2162	2163	2164	2170#
SNM82A	004452	2238	2239	2245#	
SNM82B	004462	2240	2249#		
SNM82C	004476	2250	2258#		
SNM82D	004516	2262	2263	2264	2270#
SNM82E	004526	2265	2274#		
SNM83A	004670	2354	2355	2361#	
SNM83B	004700	2356	2365#		
SNM83C	004716	2368	2369	2370	2376#
SNM83D	004726	2371	2380#		
SNM20A	004132	2048	2049	2050	2056#
SNM1A	004234	2113	2114	2115	2121#
SNM2A	004372	2194	2195	2196	2202#
SNM2B	004402	2197	2206#		
SNM3A	004602	2306	2307	2308	2314#
SNM3B	004612	2309	2318#		
SNM4A	004776	2411	2412	2418#	
SNM4B	005006	2413	2422#		
SNM5A	005060	2454	2455	2461#	
SNM5B	005070	2456	2465#		
SNM6A	005144	2497	2498	2504#	
SNM6B	005154	2499	2508#		
SNM7A	005226	2539	2540	2546#	
SNM7B	005236	2541	2550#		
SOPA	004050	2006	2014#		
SOPB	004070	2003	2016	2023#	
SOPB0A	002562	1382	1390#		
SOPB0B	002572	1391	1398#		
SOPB1A	002704	1460	1468#		
SOPB1B	002720	1469	1471	1478#	
SOPB1C	002764	1505	1513#		
SOPB1D	003002	1517	1524#		
SOPB2A	003136	1600	1608#		
SOPB2B	003154	1611	1619#		
SOPB2C	003224	1643	1651#		
SOPB2D	003246	1656	1664#		
SOPB3A	003376	1744	1752#		
SOPB3B	003422	1755	1757	1766#	
SOPB3C	003470	1797	1805#		
SOPB7C	003512	1811	1818#		
SOPY	004034	2005#	2014#	2015*	2028
SOPYX0	004100	2017*	2028#		
SOP24	003050	1552	1560#		
SOP0A	002424	1295	1303#		
SOP0B	002442	1305	1313#		
SOP0C	002504	1342	1350#		
SOP0D	002526	1352	1355	1363#	
SOP1A	002630	1420	1428#		
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TST132	010350	3765	3779	3802#
TST133	010436	3818	3844#	
TST134	010506	3851	3877#	
TST135	010560	3884	3932#	
TST136	011124	4037	4067#	
TST137	011602	4201	4223#	
TST14	001300	774#		
TST140	011656	4225	4236	4263#
TST141	011742	4265	4286	4300#
TST142	012032	4302	4324	4338#
TST143	012122	4340	4361	4375#
TST144	012214	4377	4400	4426#
TST145	012332	4428	4466	4480#
TST146	012474	4482	4533	4557#
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TST15	001334	776	781	794#
TST150	012616	4582	4604	4618#
TST151	012704	4620	4642	4666#
TST152	013070	4668	4729	4743#
TST153	013206	4745	4782	4806#
TST154	013332	4808	4848	4862#
TST155	013512	4864	4916	4930#
TST156	013552	4932	4939	4964#
TST157	013724	4966	5018	5031#
TST16	001370	796	801	814#
TST160	014072	5033	5086	5111#
TST161	014240	5113	5166	5180#
TST162	014402	5182	5234	5248#
TST163	014552	5250	5304	5318#
TST164	014732	5320	5377	5416#
TST165	015172	5465#		
TST17	001424	816	821	834#
TST2	000644	502	535	562#
TST20	001460	836	841	870#
TST21	001520	872	876	889#
TST22	001556	891	894	907#
TST23	001614	909	912	925#
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TST25	001716	960	965	978#
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TST32	002210	1083	1101	1128#
TST33	002260	1130	1148	1175#
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TST35	002400	1224	1242	1291#
TST36	002456	1293	1314	1337#
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TST4	000736	583	587	600#
TST40	002602	1380	1393	1415#
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1007#

TST44 003100
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TST46 003256
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TST54 003742
TST55 004022
TST56 004102
TST57 004142
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TST60 004202
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YNTAB 015370
SAPTHD 000330
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1593 1614 1633#
1635 1659 1687#
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502 506 619#
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1829 1849 1878#
1880 1898 1920#
1922 1938 1961#
1963 1979 2001#
2018 2041#
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621 624 661#
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2107 2116 2137#
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663 667 660#
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5476# 5477 5479
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5433# 5436# 5446#
5420 5515#
457 463#
439#
430#
416 5473 5483#
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398# 511 512# 520 521# 531 532# 540 541# 573 574# 592 593#
611 612# 629 630# 672 673# 690 691# 708 709# 726 727# 746
747# 767 768# 786 787# 806 807# 826 827# 846 847# 881 882#
899 900# 917 918# 935 936# 970 971# 989 990# 999 1000# 1019
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1767 1768# 1802 1803# 1819 1820# 1839 1840# 1855 1856# 1890 1891# 1904
1905# 1932 1933# 1944 1945# 1973 1974# 1985 1986# 2011 2012# 2024 2025#
2057 2058# 2089 2090# 2122 2123# 2154 2155# 2171 2172# 2203 2204# 2213
2214# 2246 2247# 2255 2256# 2271 2272# 2281 2282# 2315 2316# 2325 2326#
2362 2363# 2377 2378# 2387 2388# 2419 2420# 2428 2429# 2462 2463# 2472
2473# 2505 2506# 2514 2515# 2547 2548# 2556 2557# 2583 2584# 2610 2611#

2636	2637	2649	2650	2660	2661	2675	2676	2686	2687	2712	2713	2721
2722	2731	2732	2743	2744	2753	2754	2782	2783	2810	2811	2839	2840
2874	2875	2884	2885	2914	2915	2942	2943	2952	2953	2982	2983	2991
2992	3020	3021	3030	3031	3058	3059	3085	3086	3112	3113	3147	3148
3185	3186	3222	3223	3254	3255	3285	3286	3300	3301	3333	3334	3349
3349	3365	3366	3398	3399	3415	3416	3434	3435	3453	3464	3477	3478
3491	3492	3524	3525	3560	3561	3590	3591	3620	3621	3647	3648	3656
3657	3683	3684	3711	3712	3720	3721	3747	3748	3775	3776	3784	3785
3814	3815	3824	3825	3857	3858	3890	3891	3944	3945	3953	3954	3967
3968	3979	3980	3988	3989	4001	4002	4014	4015	4028	4029	4042	4043
4082	4083	4101	4102	4120	4121	4138	4139	4156	4157	4172	4173	4188
4189	4207	4208	4232	4233	4241	4242	4277	4278	4292	4293	4315	4316
4330	4331	4353	4354	4367	4368	4391	4392	4406	4407	4441	4442	4457
4458	4472	4473	4495	4496	4509	4510	4523	4524	4539	4540	4572	4573
4595	4596	4610	4611	4633	4634	4648	4649	4680	4681	4694	4695	4708
4709	4720	4721	4735	4736	4758	4759	4773	4774	4788	4789	4822	4823
4838	4839	4854	4855	4877	4878	4892	4893	4908	4909	4922	4923	4945
4946	4979	4980	4994	4995	5009	5010	5024	5025	5047	5048	5062	5063
5077	5078	5092	5093	5127	5128	5142	5143	5156	5157	5172	5173	5196
5197	5211	5212	5226	5227	5240	5241	5264	5265	5279	5280	5293	5294
5310	5311	5334	5335	5350	5351	5365	5366	5383	5384	5448	5449	5489
5490	487	495*										
	434											
	446	469										
	427	487										
	464											
	425	465	469									
	465											
	432											
	433											
	426	496*										
	429	490*	5468*									
	467											
	414	419										
	398											
	437											
	428	482	488	493	766	770	5447					
	398	497	503	535	559	565	568	578	584	587	597	603
	616	622	624	658	664	667	677	683	685	695	701	703
	719	721	731	737	741	751	757	771	777	781	791	797
	811	817	821	831	837	841	867	873	876	886	892	894
	910	912	922	928	930	955	961	965	975	981	984	994
	1010	1014	1024	1030	1034	1044	1050	1054	1078	1084	1101	1125
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	1375	1381	1393	1412	1418	1432	1450	1456	1473	1494	1500	1519
	1546	1567	1588	1594	1614	1630	1636	1659	1684	1690	1708	1731
	1761	1785	1791	1813	1824	1830	1849	1875	1881	1898	1917	1923
	1958	1964	1979	1998	2004	2018	2038	2044	2051	2070	2076	2083
	2108	2116	2134	2140	2165	2183	2189	2208	2226	2232	2276	2293
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	2526	2532	2551	2567	2573	2578	2594	2600	2605	2623	2629	2681
	2703	2748	2765	2771	2777	2793	2799	2805	2822	2828	2834	2855
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MACY11 27032
CROSS REFERENCE TABLE -- USER SYMBOLS

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3702	3715	3733	3739	3742	3760	3766	3779	3799	3805	3818	3841	3847
3851	3874	3880	3884	3929	3935	4037	4064	4070	4201	4220	4226	4236
4260	4266	4286	4297	4303	4324	4335	4341	4361	4372	4378	4400	4423
4429	4466	4477	4483	4533	4554	4560	4566	4577	4593	4604	4615	4621
4642	4663	4669	4729	4740	4746	4782	4803	4809	4848	4859	4865	4916
4927	4933	4939	4961	4967	5018	5028	5034	5086	5108	5114	5166	5177
5183	5234	5245	5251	5304	5315	5321	5377	5413	5419	5462	5468	
466												
488	494*											
431												
468												
438												
503	518	538	565	571	584	590	603	609	622	627	664	670
683	688	701	706	719	724	737	744	757	777	784	797	804
817	824	837	844	873	879	892	897	910	915	928	933	961
968	981	987	997	1010	1017	1030	1037	1050	1057	1084	1091	1104
1131	1138	1151	1178	1185	1198	1225	1232	1245	1294	1298	1308	1317
1340	1345	1361	1381	1385	1396	1418	1423	1435	1456	1463	1476	1500
1508	1522	1546	1555	1570	1594	1603	1617	1636	1646	1662	1690	1698
1711	1737	1747	1764	1791	1800	1816	1830	1837	1852	1881	1888	1901
1923	1930	1941	1964	1971	1982	2004	2009	2021	2044	2054	2076	2086
2108	2119	2140	2151	2168	2189	2200	2211	2232	2243	2253	2268	2279
2299	2312	2323	2345	2359	2374	2385	2405	2416	2426	2446	2459	2470
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3211	3220	3243	3252	3273	3282	3297	3320	3330	3345	3362	3383	3395
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3782	3805	3812	3821	3847	3854	3880	3887	3935	3942	3951	3965	3977
3986	3999	4012	4026	4040	4070	4098	4117	4135	4153	4169	4185	4204
4226	4239	4266	4274	4289	4303	4312	4327	4341	4350	4364	4378	4388
4403	4429	4438	4454	4469	4483	4492	4506	4520	4536	4560	4569	4583
4592	4607	4621	4630	4645	4669	4677	4691	4705	4717	4732	4746	4755
4770	4785	4809	4819	4835	4851	4865	4874	4889	4905	4919	4933	4942
4967	4976	4991	5006	5021	5034	5044	5059	5074	5089	5114	5124	5139
5153	5169	5183	5193	5208	5223	5237	5251	5261	5276	5290	5307	5321
5331	5347	5362	5380	5419	5468							
518	538	571	590	609	627	670	688	706	724	744	784	804
824	844	879	897	915	933	968	987	997	1017	1037	1057	1091
1104	1138	1151	1185	1198	1232	1245	1298	1308	1317	1345	1361	1385
1396	1423	1435	1463	1476	1508	1522	1555	1570	1603	1617	1646	1662
1698	1711	1747	1764	1800	1816	1837	1852	1888	1901	1930	1941	1971
1982	2009	2021	2054	2086	2119	2151	2168	2200	2211	2243	2253	2268
2279	2312	2323	2359	2374	2385	2416	2426	2459	2470	2502	2512	2544
2554	2581	2608	2634	2647	2658	2673	2684	2710	2719	2729	2741	2751
2780	2808	2837	2872	2882	2912	2940	2950	2980	2989	3018	3028	3056
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3745	3773	3782	3812	3821	3854	3887	3942	3951	3965	3977	3986	3999
4012	4026	4040	4098	4117	4135	4153	4169	4185	4204	4239	4274	4289
4312	4327	4350	4364	4388	4403	4438	4454	4469	4492	4506	4520	4536
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 SUNIT 000312
 SUNIT 000340
 SUSAR 000324
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	1101	1135	1148	1182	1195	1229	1242	1295	1305	1314	1342	1358	1382	1393	1420
	1432	1460	1473	1505	1519	1552	1567	1600	1614	1643	1659	1695	1708	1744	1761
	1797	1813	1834	1849	1885	1898	1927	1938	1968	1979	2006	2018	2051	2083	2116
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	2456	2467	2499	2509	2541	2551	2578	2605	2631	2644	2655	2670	2681	2707	2716
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	3809	3818	3851	3884	3939	3948	3962	3974	3983	3996	4009	4023	4037	4081	4095
	4114	4132	4150	4166	4182	4201	4232	4236	4271	4286	4309	4324	4347	4361	4385
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	5258	5273	5287	5304	5328	5344	5359	5377	5448	5488					
ESCAPE	1														
SET PRI	1														
SET SLIP	1														
JMP	5387	5428	5453	5458											
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	5347	5362	5380												
MULT	1														
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POP	1														
PUSH	1														
REPORT	1														
SET PRI	1														
SETUP	1														
SKIP	1														
SLASH	1														
STARS	1														
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		599	616	618	634	658	660	677	679	695	697	713	715	731	733

CROSS REFERENCE TABLE -- NAMES

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1065	1078	1080	1112	1125	1127	1159	1172	1174	1206	1219	1221	1253	1271	1275
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SWSU
 TYPBIN
 TYPDEC
 TYPNAM
 TYPNUM
 TYPOCS
 TYPOCT
 TYPTXT
 SSERCO

398	511	520	531	540	573	592	611	629	672	690	708	726	746	767
786	806	826	846	881	899	917	935	970	989	999	1019	1039	1059	1094
1107	1141	1154	1188	1201	1235	1248	1300	1310	1319	1347	1364	1387	1399	1425
1438	1465	1479	1510	1525	1557	1573	1605	1620	1648	1665	1700	1714	1749	1767
1802	1819	1839	1855	1890	1904	1932	1944	1973	1985	2011	2024	2057	2089	2122
2154	2171	2203	2213	2246	2255	2271	2281	2315	2325	2362	2377	2387	2419	2428
2462	2472	2505	2514	2547	2556	2583	2583	2610	2636	2649	2675	2686	2712	2721
2731	2743	2753	2782	2810	2839	2874	2884	2914	2942	2952	2982	2991	3020	3030
3058	3085	3112	3147	3185	3222	3254	3285	3300	3333	3348	3365	3398	3415	3434
3463	3477	3491	3524	3560	3590	3620	3647	3656	3683	3711	3720	3747	3775	3784
3814	3824	3857	3890	3944	3953	3967	3979	3988	4001	4014	4028	4042	4082	4101
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4406	4441	4457	4472	4495	4509	4523	4539	4572	4595	4610	4633	4648	4680	4694
4708	4720	4735	4758	4773	4788	4822	4838	4854	4877	4892	4908	4922	4945	4979
4994	5009	5024	5047	5062	5077	5092	5127	5142	5156	5172	5196	5211	5226	5240
5264	5279	5293	5310	5334	5350	5365	5383	5448	5489					
398	511	520	531	540	573	592	611	629	672	690	708	726	746	767
786	806	826	846	881	899	917	935	970	989	999	1019	1039	1059	1094
1107	1141	1154	1188	1201	1235	1248	1300	1310	1319	1347	1364	1387	1399	1425
1438	1465	1479	1510	1525	1557	1573	1605	1620	1648	1665	1700	1714	1749	1767
1802	1819	1839	1855	1890	1904	1932	1944	1973	1985	2011	2024	2057	2089	2122
2154	2171	2203	2213	2246	2255	2271	2281	2315	2325	2362	2377	2387	2419	2428
2462	2472	2505	2514	2547	2556	2583	2610	2636	2649	2660	2675	2686	2712	2721
2731	2743	2753	2782	2810	2839	2874	2884	2914	2942	2952	2982	2991	3020	3030
3058	3085	3112	3147	3185	3222	3254	3285	3300	3333	3348	3365	3398	3415	3434
3463	3477	3491	3524	3560	3590	3620	3647	3656	3683	3711	3720	3747	3775	3784
3814	3824	3857	3890	3944	3953	3967	3979	3988	4001	4014	4028	4042	4082	4101
4120	4138	4156	4172	4188	4207	4232	4241	4277	4292	4315	4330	4353	4367	4391

SSERNJ

SPC
SRAND
SRDOE
SRDOC
SREAD
SRZK
SSAVE
SSB2D
SSB2C
SSCOP
SSIZE
SSUPP
STAPP
STYPB
STYPD
STYPE
STYPO
S40CA
S40C

Table with columns for symbols (e.g., B000, B001, B002) and corresponding numerical values. The table is organized into rows and columns, with some symbols appearing multiple times. The values are integers ranging from approximately 100 to 5500.

S.S	1182	1194	1241	2048	2081	2113	2146	2162	2194	2238	2262	2306	2354	2368	2411
	2454	2497	2539	4270	4285	4308	4323	4346	4360	4383	4399	4435	4449	4488	4516
	4564	4587	4603	4626	4639	4673	4713	4726	4766	4779	4814	4845	4870	4915	4938
	4972	5002	5039	5054	5069	5119	5149	5187	5218	5256	5286	5325	5357	5510	
CCC	503	1085	1132	1179	1226	4430	4697	4826	4866	4896	4934	4968	5012	5115	5159
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	3610	4267	4305	4343	4380	4462	4513	4724	4777	4811	5051	5131	5215	5268	5339
CLY	1146	2079	2144	2236	2352	2452	2495	2537	4267	4305	4343	4380	4395	4513	4528
	4600	4623	4748	4811	5066	5146	5185	5283	5323						
CLR	1294	1340	1418	1419	1456	1457	1500	1501	1546	1549	1551	1594	1597	1636	1639
	1690	1693	1694	1737	1740	1741	1791	1794	1830	1833	1881	1882	1884	1923	1926
	1964	1967	2004	2044	2076	2108	2109	2140	2141	2157	2189	2190	2232	2233	2299
	2300	2345	2346	2405	2406	2446	2447	2490	2491	2532	2533	2573	2575	2600	2601
	2629	2663	2665	2703	2704	2734	2736	2771	2773	2774	2799	2800	2802	2828	2829
	2831	2861	2862	2865	2902	2903	2904	2932	2933	2972	3008	3009	3010	3077	3104
	3320	3352	3383	3401	3418	3675	3703	3935	4075	4076	4378	4562	4841		
CLRB	1381	1459	1504	1599	1642	1743	1796								
CLV	1193	1240	4528	4748	4882	4984	5082	5131	5268	5339					
CLZ	1099	2046	2111	2160	2192	2260	2304	2366	2409	4282	4320	4357	4446	4499	4561
	4584	4637	4724	4763	4777	4843	5036	5051							
CMP	501	563	582	586	601	605	620	623	662	681	684	699	702	717	720
	735	755	775	795	815	835	871	890	893	908	911	926	929	959	964
	979	993	1008	1028	1033	1048	1082	1129	1176	1223	1292	1338	1379	1416	1454
	1498	1544	1592	1634	1688	1735	1789	1828	1879	1921	1962	2002	2042	2074	2106
	2138	2187	2230	2297	2343	2403	2444	2488	2530	2571	2598	2627	2701	2706	2715
	2725	2769	2797	2826	2859	2900	2930	2970	3006	3047	3074	3079	3101	3106	3133
	3140	3171	3178	3209	3216	3241	3248	3271	3278	3293	3318	3326	3341	3358	3381
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ROR	1032	1052	5186	5201	5216	5231									
RTS	4229														
SBC	1354	5037	5052	5067	5083										
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	2652	2655	2663	2670	2678	2681	2707	2715	2716	2724	2726	2734	2738	2746	2748
	2777	2805	2834	2869	2877	2879	2909	2937	2945	2947	2977	2985	2986	3015	3023

3325	3353	3380	3407	3441	3479	3517	3554	3592	3629	3667	3704	3742	3780	3817	3855	3893	3931	3969	4007	4045	4083	4121	4159	4197	4235	4273	4311	4349	4387	4425	4463	4501	4539	4577	4615	4653	4691	4729	4767	4805	4843	4881	4919	4957	4995	5033	5071	5109	5147	5185	5223	5261	5299	5337	5375	5413	5451	5489	5527	5565	5603	5641	5679	5717	5755	5793	5831	5869	5907	5945	5983	6021	6059	6097	6135	6173	6211	6249	6287	6325	6363	6401	6439	6477	6515	6553	6591	6629	6667	6705	6743	6781	6819	6857	6895	6933	6971	7009	7047	7085	7123	7161	7199	7237	7275	7313	7351	7389	7427	7465	7503	7541	7579	7617	7655	7693	7731	7769	7807	7845	7883	7921	7959	7997	8035	8073	8111	8149	8187	8225	8263	8301	8339	8377	8415	8453	8491	8529	8567	8605	8643	8681	8719	8757	8795	8833	8871	8909	8947	8985	9023	9061	9099	9137	9175	9213	9251	9289	9327	9365	9403	9441	9479	9517	9555	9593	9631	9669	9707	9745	9783	9821	9859	9897	9935	9973
3326	3354	3381	3408	3442	3480	3518	3555	3593	3630	3668	3705	3743	3781	3818	3856	3894	3932	3970	4008	4046	4084	4122	4160	4198	4236	4274	4312	4350	4388	4426	4464	4502	4540	4578	4616	4654	4692	4730	4768	4806	4844	4882	4920	4958	4996	5034	5072	5110	5148	5186	5224	5262	5300	5338	5376	5414	5452	5490	5528	5566	5604	5642	5680	5718	5756	5794	5832	5870	5908	5946	5984	6022	6060	6098	6136	6174	6212	6250	6288	6326	6364	6402	6440	6478	6516	6554	6592	6630	6668	6706	6744	6782	6820	6858	6896	6934	6972	7010	7048	7086	7124	7162	7200	7238	7276	7314	7352	7390	7428	7466	7504	7542	7580	7618	7656	7694	7732	7770	7808	7846	7884	7922	7960	7998	8036	8074	8112	8150	8188	8226	8264	8302	8340	8378	8416	8454	8492	8530	8568	8606	8644	8682	8720	8758	8796	8834	8872	8910	8948	8986	9024	9062	9100	9138	9176	9214	9252	9290	9328	9366	9404	9442	9480	9518	9556	9594	9632	9670	9708	9746	9784	9822	9860	9898	9936	9974

LIST

734	737	744	747	754	757	768	774	777	784	787	794	797	804	807
814	817	824	827	834	837	844	847	870	873	879	882	889	892	897
900	907	910	915	918	925	928	933	936	958	961	968	971	978	981
987	990	997	1000	1007	1010	1017	1020	1027	1030	1037	1040	1047	1050	1057
1060	1081	1084	1091	1095	1104	1108	1128	1131	1138	1142	1151	1155	1175	1178
1185	1189	1198	1202	1222	1225	1232	1236	1245	1249	1291	1294	1298	1301	1308
1311	1317	1320	1337	1340	1345	1348	1361	1365	1378	1381	1385	1388	1396	1400
1415	1416	1423	1426	1435	1439	1453	1456	1463	1466	1476	1480	1497	1500	1508
1511	1522	1526	1543	1546	1555	1558	1570	1574	1591	1594	1603	1606	1617	1621
1633	1636	1646	1649	1662	1666	1687	1690	1698	1701	1711	1715	1734	1737	1747
1750	1764	1768	1789	1791	1800	1803	1816	1820	1827	1830	1837	1840	1852	1856
1878	1881	1888	1891	1901	1905	1920	1923	1930	1933	1941	1945	1961	1964	1971
1974	1982	1986	2001	2004	2009	2012	2021	2025	2041	2044	2054	2058	2073	2076
2086	2090	2105	2108	2119	2123	2137	2140	2151	2155	2168	2172	2186	2189	2200
2204	2211	2214	2229	2232	2243	2247	2253	2256	2268	2272	2279	2282	2296	2299
2312	2316	2323	2326	2342	2345	2359	2363	2374	2378	2385	2388	2402	2405	2416
2420	2426	2429	2443	2446	2459	2463	2470	2473	2487	2490	2502	2506	2512	2515
2529	2532	2544	2548	2554	2557	2570	2573	2581	2584	2597	2600	2608	2611	2626
2629	2634	2637	2647	2650	2658	2661	2673	2676	2684	2687	2700	2703	2710	2713
2719	2722	2729	2732	2741	2744	2751	2754	2768	2771	2780	2783	2796	2799	2808
2811	2825	2828	2837	2840	2858	2861	2872	2875	2882	2885	2899	2902	2912	2915
2929	2932	2940	2943	2950	2953	2969	2972	2980	2983	2989	2992	3005	3008	3018
3021	3028	3031	3046	3049	3056	3059	3073	3076	3083	3086	3100	3103	3110	3113
3132	3135	3144	3148	3170	3173	3182	3186	3208	3211	3220	3223	3240	3243	3252
3255	3270	3273	3282	3286	3297	3301	3317	3320	3330	3334	3345	3349	3362	3366
3380	3383	3395	3399	3412	3416	3431	3435	3449	3452	3460	3464	3474	3478	3488
3492	3507	3510	3521	3525	3542	3545	3557	3561	3576	3579	3587	3591	3605	3608
3617	3621	3637	3640	3645	3648	3654	3657	3671	3674	3681	3684	3699	3702	3709
3712	3718	3721	3736	3739	3745	3748	3763	3766	3773	3776	3782	3785	3802	3805
3812	3815	3821	3825	3844	3847	3854	3858	3877	3880	3887	3891	3932	3935	3942
3945	3951	3954	3965	3968	3977	3980	3986	3989	3999	4002	4012	4015	4026	4029
4040	4043	4067	4070	4083	4098	4102	4117	4121	4135	4139	4153	4157	4169	4173
4185	4199	4204	4208	4223	4226	4233	4239	4242	4263	4266	4274	4278	4289	4293
4300	4303	4312	4316	4327	4331	4338	4341	4350	4354	4364	4368	4375	4378	4388
4392	4403	4407	4426	4429	4438	4442	4454	4458	4469	4473	4480	4483	4492	4496
4506	4510	4520	4524	4536	4540	4557	4560	4569	4573	4580	4583	4592	4596	4607
4611	4618	4621	4630	4634	4645	4649	4666	4669	4677	4681	4691	4695	4705	4709
4717	4721	4732	4736	4743	4746	4755	4759	4770	4774	4785	4789	4806	4809	4819
4823	4835	4839	4851	4855	4862	4865	4874	4878	4889	4893	4905	4909	4919	4923
4930	4933	4942	4946	4964	4967	4976	4980	4991	4995	5006	5010	5021	5025	5031
5034	5044	5048	5059	5063	5074	5078	5089	5093	5111	5114	5124	5128	5139	5143
5153	5157	5169	5173	5180	5183	5193	5197	5208	5212	5223	5227	5237	5241	5248
5251	5261	5265	5276	5280	5280	5294	5307	5311	5318	5321	5331	5335	5347	5351
5362	5366	5380	5384	5416	5419	5449	5465	5468	5490					

MACRO
MCALL
MEXIT
MIS*

1	398	401	409	424	500	503	512	518	521	532	538	541	562	565
409														
447														
1	398	401	409	424	500	503	512	518	521	532	538	541	562	565
571	574	581	584	590	593	600	603	609	612	619	622	627	630	661
664	670	673	680	683	688	691	698	701	706	709	716	719	724	727
734	737	744	747	754	757	768	774	777	784	787	794	797	804	807
814	817	824	827	834	837	844	847	870	873	879	882	889	892	897
900	907	910	915	918	925	928	933	936	958	961	968	971	978	981
987	990	997	1000	1007	1010	1017	1020	1027	1030	1037	1040	1047	1050	1057
1060	1081	1084	1091	1095	1104	1108	1128	1131	1138	1142	1151	1155	1175	1178
1185	1189	1198	1202	1222	1225	1232	1236	1245	1249	1291	1294	1298	1301	1308

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

* DOKRAA.SEG/SOL/CRF PAGES IN NL: 700 DS:ERFD=S*SMAC.CC.DG:RAA.P11
RUN-TIME: 61 BY 12 SECONDS
RUN-TIME RATIO: 527/158=3.3
CORE USED: 33K (65 PAGES)