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IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DEKBH-A-D
PRODUCT NAME:	PDP-11/70 DIAGNOSTIC/BOOTSTRAP (M9301-YC) PATTERN
DATE CREATED:	21-JULY-75
MAINTAINER:	DIAGNOSTIC ENGINEERING
AUTHOR:	DALE A. ROLOGER

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        1)      ABSTRACT
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                THIS PROGRAM IS THE ROM DIAGNOSTIC/BOOTSTRAP FOR THE M9301-YC
                IT IS MEANT TO BE FOR THE PDP-11/70 ONLY, AND WILL FAIL ON ALL
                OTHER PDP-11 PROCESSORS.

                THE DIAGNOSTIC PORTION OF THE PROGRAM WILL TEST THE BASIC CPU,
                INCLUDING: THE BRANCHES, THE REGISTERS, ALL ADDRESSING MODES,
                AND MOST OF THE INSTRUCTIONS IN THE PDP-11 REPERTOIRE.  IT WILL
                THEN SET THE STACK POINTER TO KERNEL D-SPACE P.A.R. 7, CHECK
                AND TURN ON, IF REQUESTED, MEMORY MANAGEMENT AND THE UNIBUS MAP,
                AND CHECK MEMORY FROM VIRTUAL ADDRESS 1000 TO 157776.  AFTER
                MAIN MEMORY HAS BEEN VERIFIED, WITH THE CACHE OFF, THE CACHE
                MEMORY WILL BE TESTED TO VERIFY THAT "HITS" OCCUR PROPERLY.
                THEN MAIN MEMORY WILL BE SCANNED AGAIN TO INSURE THAT THE CACHE
                IS WORKING PROPERLY THROUGHOUT THE 28K OF MEMORY TO BE USED IN
                THE "BOOT" OPERATION.

                IF ONE OF THE CACHE MEMORY TESTS FAILS, THE OPERATOR CAN ATTEMPT
                TO "BOOT" THE SYSTEM ANYWAY BY PRESSING "CONTINUE".  THIS WILL
                CAUSE THE PROGRAM TO FORCE "MISSES" IN BOTH GROUPS OF THE CACHE
                BEFORE GOING TO THE BOOTSTRAP SECTION OF THE PROGRAM.

                THE BOOTSTRAP PORTION OF THE PROGRAM LOOKS AT THE LOWER BYTE OF
                THE SWITCH REGISTER TO DETERMINE WHICH ONE OF 9 DEVICES AND WHICH
                DRIVE NUMBER TO ATTEMPT THE "BOOT" FROM.  SWITCHES <02 : 00>
                SELECT THE DRIVE NUMBER (0 - 7), AND SWITCHES <06 : 03> SELECT
                THE DEVICE CODE (1 - 11).  IF THE LOWER BYTE OF THE SWITCH REGIS-
                TER IS ZERO, THE PROGRAM WILL READ THE SET OF SWITCHES ON THE
                M9301-YC TO DETERMINE THE DEVICE AND DRIVE NUMBER.  THESE SWITCHES
                CAN BE SET BY FIELD SERVICE TO SELECT A "DEFAULT BOOT" DEVICE.

                IF THE BOOTSTRAP OPERATION FAILS AS A RESULT OF A HARDWARE ERROR
                IN THE PERIPHERAL DEVICE THE PROGRAM WILL DO A "RESET" INSTRUC-
                TION AND JUMP BACK TO THE TEST THAT SETS UP AND TURNS ON MEMORY
                MANAGEMENT AND TESTS MEMORY.  THEN THE PROGRAM WILL ATTEMPT TO
                "BOOT" AGAIN.

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        2)      STARTING PROCEDURE
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            2.1   SWITCH SETTINGS

                THE LOWER BYTE OF THE SWITCH REGISTER SHOULD BE SET TO HAVE
                THE DRIVE NUMBER (0 - 7) IN SWITCHES <02 : 00>, AND THE DEVICE
                CODE (1 - 11) IN SWITCHES <06 : 03>.

                THE UPPER BYTE OF THE SWITCH REGISTER SHOULD BE SET TO HAVE
                THE BANK NUMBER OF THE 32K BLOCK OF MEMORY TO BE USED FOR THE
                BOOTSTRAP OPERATION (0 - 17) IN SWITCHES <15 : 12>.

                THE DEVICE CODES ARE AS FOLLOWS:
                1)    TM11/TU10    MAGNETIC TAPE, TM11
                2)    TC11/TU56    DECTAPE, TC11-G
                3)    RK11/RK05    DECPACK DIS CARTRIDGE, RK11-D
                4)    RP11/RP03    DISK PACK, RP11-C
                5)    RESERVED FOR FUTURE DEVICE
                6)    RH70/TU16    MAGNETIC TAPE SYSTEM, TMU16
                7)    RH70/RP04    DISK PACK, RHP04
                10)   RH70/RS04    FIXED HEAD DISK, RHS04 (OR RHS03)
                11)   RX11/RX01    DISKETTE

                THE MEMORY BLOCKS ARE AS FOLLOWS:
                0)    PHYSICAL MEMORY 0 - 28K
                1)    PHYSICAL MEMORY 32K - 60K
                2)    PHYSICAL MEMORY 64K - 92K
                3)    PHYSICAL MEMORY 96K - 124K
                4)    PHYSICAL MEMORY 128K - 156K
                .
                .
                13)   PHYSICAL MEMORY 256K - 284K
                .
                .
                14)   PHYSICAL MEMORY 384K - 412K
                15)   PHYSICAL MEMORY 416K - 444K
                16)   PHYSICAL MEMORY 448K - 476K
                17)   PHYSICAL MEMORY 480K - 508K
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            2.2   STARTING ADDRESSES

                THE NORMAL STARTING ADDRESS FOR THIS PROGRAM IS 177765000.

                IF THE DIAGNOSTIC PORTION OF THIS PROGRAM FAILS AND THE OPERATOR
                WANTS TO ATTEMPT TO "BOOT" ANYWAY, HE MUST FOLLOW THESE STEPS:

                1)  SET UP MEMORY MANAGEMENT IF "BOOTING" INTO OTHER THAN
                    THE LOWER 28K OF MEMORY.

                2A) IF DEVICE IS ON MASSBUS:
                    SET STACK POINTER TO A VALID ADDRESS AND LOAD THAT ADDRESS
                    WITH THE MEMORY BANK NUMBER HE WOULD PUT INTO SWITCHES <15:12>.

                2B) IF DEVICE IS ON UNIBUS:
                    SET UP UNIBUS MAP REGISTERS 0 THRU 6 TO MAP TO SAME MEMORY
                    AS MEMORY MANAGEMENT.

                3)  DEPOSIT ADDRESS 173000 INTO THE PC.

                4)  SET THE DEVICE CODE AND DRIVE NUMBER IN THE LOWER BYTE OF
                    THE SWITCH REGISTER.

                5)  PRESS CONTINUE.

                EXAMPLES:
                A) RP04 -- SET STACK POINTER TO 40000
                           LOAD 000000 INTO ADDRESS 40000
                           LOAD 173000 INTO THE PC (17777707)
                           SET 000070 INTO SWITCHES  (RP04  DRIVE 0)
                           PRESS "CONTINUE"

                B) RK05 -- LOAD 173000 INTO THE PC (17777707)
                           SET 000030 INTO SWITCHES  (RK05  DRIVE 0)
                           PRESS "CONTINUE"

            2.3   OPERATOR ACTION

                IF THE DIAGNOSTIC PORTION OF THE ROM FAILS RECORD THE PC OF
                THE "HALT" INSTRUCTION AND REFER TO THE LISTING TO FIND OUT WHAT
                PORTION OF THE MACHINE FAILED.

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3) ERRORS

3.1 LIST OF ERROR HALTS INDEXED BY THE ADDRESS DISPLAYED

ADDRESS DISPLAYED	TEST NUMBER AND SUBSYSTEM UNDER TEST
17765004	TEST 1 BRANCH TEST
17765020	TEST 2 BRANCH TEST
17765036	TEST 3 BRANCH TEST
17765052	TEST 4 BRANCH TEST
17765066	TEST 5 BRANCH TEST
17765076	TEST 6 BRANCH TEST
17765134	TEST 7 REGISTER DATA PATH TEST
17765146	TEST 10 BRANCH TEST
17765166	TEST 11 CPU INSTRUCTION TEST
17765204	TEST 12 CPU INSTRUCTION TEST
17765214	TEST 13 CPU INSTRUCTION TEST
17765222	TEST 14 "COM" INSTRUCTION TEST
17765236	TEST 14 CPU INSTRUCTION TEST
17765260	TEST 15 CPU INSTRUCTION TEST
17765270	TEST 16 BRANCH TEST
17765312	TEST 16 CPU INSTRUCTION TEST
17765346	TEST 17 CPU INSTRUCTION TEST
17765360	TEST 20 CPU INSTRUCTION TEST
17765374	TEST 20 CPU INSTRUCTION TEST
17765450	TEST 21 KERNEL P.A.R. TEST
17765474	TEST 22 KERNEL P.D.R. TEST
17765510	TEST 23 "JSR" TEST
17765520	TEST 23 "JSR" TEST
17765530	TEST 23 "RTS" TEST
17765542	TEST 23 "RTI" TEST
17765550	TEST 23 "JMP" TEST
17765760	TEST 25 MAIN MEMORY DATA COMPARE ERROR
17766000	TEST 25 MAIN MEMORY PARITY ERROR NO RECOVERY POSSIBLE FROM THIS ERROR
17773644	TEST 26 CACHE MEMORY DATA COMPARE ERROR
17773654	TEST 26 CACHE MEMORY NO "HIT" PRESSING "CONTINUE" HERE WILL CAUSE "BOOT" ATTEMPT FORCING "MISSES"
17773736	TEST 27 CACHE MEMORY DATA COMPARE ERROR
17773746	TEST 27 CACHE MEMORY NO "HIT" PRESSING "CONTINUE" HERE WILL CAUSE "BOOT" ATTEMPT FORCING "MISSES"
17773764	TEST 25 OR 26 CACHE MEMORY PARITY ERROR PRESSING "CONTINUE" HERE WILL CASUE "BOOT" ATTEMPT FORCING "MISSES"

3.2 ERROR RECOVERY

MOST OF THE ABOVE ERROR HALTS ARE "HARD" FAILURES, WHICH MEANS THAT THERE IS NO RECOVERY FROM THEM. ESPECIALLY THE TWO (2) MAIN

MEMORY HALTS ARE NOT RECOVERABLE. YOUR BEST BET IS TO TRY TO
"BOOT" INTO ANOTHER 32K BANK OF MEMORY IF IT APPEARS TO
BE A MAIN MEMORY FAILURE.

IF THE PROCESSOR HALTS IN ONE OF THE TWO CACHE TESTS THE ERROR
CAN BE RECOVERED FROM. BY PRESSING "CONTINUE" THE PROGRAM WILL
EITHER ATTEMPT TO FINISH THE TEST (IF AT EITHER: 17773644 OR
17773736) OR FORCE "MISSES" IN BOTH GROUPS OF THE CACHE AND
ATTEMPT TO "BOOT" THE SYSTEM MONITOR WITH THE CACHE FULLY
DISABLED (IF AT EITHER: 17773654, 17773740, OR 17773704).

4) EXECUTION TIME

THE RUN TIME FOR THIS PROGRAM IS APPROXIMATELY 3 SECONDS.

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.END

ERRORS DETECTED: 0

*,DEKBHA/NL:SEQ/NL:LOC/NL:BIN/NL:SYM=DEKBHA.MAN
RUN-TIME: 0 1 0 SECONDS
CORE USED: 4K

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                        .TITLE  PDP-11/70 DIAGNOSTIC/BOOTSTRAP (M9301-YC) PATTERN
                        ;* COPYRIGHT (C) JUNE 21,1979
                        ;* DIGITAL EQUIPMENT CORPORATION
                        ;* MAYNARD, MASS. 01754
                        ;*
                        ;* PROGRAMMER DALE A. ROEDGER
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;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
;*
;*      TO INITIATE THE DIAGNOSTIC/BOOTSTRAP PROGRAM IN THE M93Ø1-YC
;*      THE OPERATOR MUST: LOAD ADDRESS 17765ØØØ, SELECT THE DESIRED
;*      DEVICE CODE, DRIVE NUMBER, AND MEMORY BLOCK VIA THE SWITCH
;*      REGISTER, AND THEN PRESS "START".  AFTER THE PROGRAM HAS
;*      VERIFIED THE C.P.U., CACHE, AND THE 28K BLOCK OF MEMORY
;*      SELECTED TO BE USED (APPROXIMATELY 3 SECONDS) THE PERIPHERAL
;*      DEVICE WILL "BOOT" THE SYSTEM MONITOR.
;*
;*      THE DRIVE NUMBER DESIRED (Ø - 7) MUST BE IN THE SWITCH REGISTER,
;*      SWITCHES <Ø2 : ØØ>.
;*
;*      THE CODE FOR THE DESIRED DEVICE (1 - 11) MUST BE IN THE SWITCH
;*      REGISTER, SWITCHES <Ø7 : Ø3>.
;*
;*      THE DEVICE CODES AND DEVICE NAMES ARE AS FOLLOWS:
;*      1)      TM11/TU1Ø       MAGNETIC TAPE, TM11
;*      2)      TC11/TU56       DECTAPE, TC11-C
;*      3)      RK11/RKØ5       DECPACK DISK CARTRIDGE, RK11-D
;*      4)      RP11/RPØ3       DISK PACK, RP11-C
;*      5)      RESERVED
;*      6)      RH7Ø/TU16       MAGNETIC TAPE SYSTEM, TWU16
;*      7)      RH7Ø/RPØ4       DISK PACK, RWPØ4
;*      1Ø)     RH7Ø/RSØ4       FIXED HEAD DISK, RWSØ4 (OR RWSØ3)
;*      11)     RX11/RXØ1       DISKETTE
;*
;*      THE 32K MEMORY BLOCK NUMBER (Ø - 17) IN WHICH TO "BOOT" THE
;*      SYSTEM MUST BE IN THE SWITCH REGISTER, SWITCHES <15 : 12>.
;*      MEMORY BLOCK Ø CORRESPONDS TO PHYSICAL Ø - 28K.
;*      MEMORY BLOCK 1 CORRESPONDS TO PHYSICAL 32K - 6ØK.
;*      MEMORY BLOCK 2 CORRESPONDS TO PHYSICAL 64K - 92K.
;*      .
;*      .
;*      MEMORY BLOCK 16 CORRESPONDS TO PHYSICAL 448K - 476K.
;*      MEMORY BLOCK 17 CORRESPONDS TO PHYSICAL 48ØK - 5Ø8K.
;*
;*      IF THE DIAGNOSTIC PORTION OF THE PROGRAM FAILS AND YOU WANT
;*      TO TRY TO BOOT ANYWAY, THEN YOU MUST LOAD ADDRESS 17773ØØØ,
;*      SELECT THE DRIVE NUMBER AND DEVICE CODE AS BEFORE.  NOW YOU
;*      MUST SET UP MEMORY MANAGEMENT IF YOU WISH TO "BOOT" INTO
;*      OTHER THAN THE LOWER 28K OF MEMORY, AND FOLLOW THE PROCEDURES
;*      LISTED BELOW FOR YOUR PERIPHERAL DEVICE.
;*
;*      1)  IF THE DEVICE IS ON THE MASS BUS:
;*      THE STACK POINTER (R6) MUST BE SETUP AND THE WORD THAT IT POINTS
;*      TO MUST CONTAIN THE BLOCK NUMBER OF THE 32K BOUNDARY THAT YOU
;*      WISH TO BOOT INTO.
;*
;*      2)  IF THE DEVICE IS ON THE UNIBUS:
;*      YOU MUST SET UP THE UNIBUS MAP IN ADDITION TO MEMORY MANAGEMENT.
;*
;*****************************************************************************
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                                        ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                        ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                        ;*
                                        ;*      IF THIS PROGRAM FAILS IN AN UNCONTROLLED MANNER IT MIGHT
                                        ;*      BE DUE TO AN UNEXPECTED TRAP TO LOCATION 000004.  IF THIS IS
                                        ;*      SUSPECTED THEN LOAD A "000006" INTO ADDRESS 000004 AND A
                                        ;*      "000000" INTO LOCATION 000006.  THIS WILL CAUSE ALL TRAPS TO
                                        ;*      LOCATION 000004 TO HALT WITH 00000010 IN THE ADDRESS LIGHTS SO
                                        ;*      THAT THE OPERATOR CAN EXAMINE THE CPU ERROR REGISTER AT
                                        ;*      LOCATION 17777766.
                                        ;*
                                        ;*      THE BITS IN THE CPU ERROR REGISTER ARE DEFINED AS FOLLOWS:
                                        ;*      BIT02   = RED ZONE STACK LIMIT
                                        ;*      BIT03   = YELLOW ZONE STACK LIMIT
                                        ;*      BIT04   = UNIBUS TIME-OUT
                                        ;*      BIT05   = NON-EXISTANT MEMORY (CACHE)
                                        ;*      BIT06   = ODD ADDRESS ERROR
                                        ;*      BIT07   = ILLEGAL HALT
                                        ;*
                                        ;^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
                                        ;^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^


                                        ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                        ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                        ;*
                                        ;*      NOTE:   IN THE COMMENT FIELD OF THE BRANCHES THAT ARE BEING
                                        ;*              TESTED, JUST PRECEEDING THE ROM ADDRESS INVOLVED, IS
                                        ;*              A SYMBOL USED TO INDICATE WHETHER TO TAKE THE BRANCH
                                        ;*              UNDER TEST OR TO FALL THROUGH TO THE NEXT INSTRUCTION.
                                        ;*              A "V" INDICATES THAT THE BRANCH SHOULD NOT BE TAKEN,
                                        ;*              AND THE NEXT INSTRUCTION SHOULD BE EXECUTED.  A "*"
                                        ;*              INDICATES THAT THE BRANCH SHOULD BE EXECUTED, UNLESS
                                        ;*              AN ERROR CONDITION OCCURS.
                                        ;*
                                        ;^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
                                        ;^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^


                165000                          . = BASE1
                                        ;;*****************************************************************
                                                .SBTTL  TEST1   THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
                                        ;*
                                        ;*      THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
                                        ;*      THIS TEST IS ENTERED AND THEY SHOULD REMAIN THAT WAY UPON
                                        ;*      THE COMPLETION OF THIS TEST.
                                        ;*
                                        ;;*****************************************************************
    165000                              TST1:
    165000      000401                          BR      TST2            ; * 326 BRANCH ALWAYS
    165002      000000                          HALT
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                        ;;*****************************************************************
                        .SBTTL  TEST2   TEST "SUB", MODE "B", AND "BMI","BVS","BHI","BLOS"
                        ;*
                        ;*      THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
                        ;*      THIS TEST IS ENTERED.  UPON COMPLETION OF THIS TEST THE "SP"
                        ;*      (R6) SHOULD BE ZERO AND ONLY THE "Z" FLIP-FLOP WILL BE SET.
                        ;*
                        ;;*****************************************************************
165004                  TST2:
165004  005006                  CLR     SP              ;N=0,Z=1;V=0,C=0,SP=000000
165006  100403                  BMI     1$              ; V 324 BRANCH IF N=1
165010  102402                  BVS     1$              ; V 324 BRANCH IF V=1
165012  101001                  BHI     1$              ; V 321 BRANCH IF Z AND C ARE BOTH 0
165014  101401                  BLOS    TST3            ; * 329 BRANCH IF (Z XOR C)=1
165016  000000          1$:     HALT
                        ;;*****************************************************************
                        .SBTTL  TEST3   TEST "DEC", MODE "B", AND "BPL","BEQ","BGE","BGT","BLE"
                        ;*
                        ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                        ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                        ;*      R3 = ? R4 = ? R5 = ? SP = 000000
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                        ;*      N = 1, Z = 0, V = 0, AND C = 0
                        ;*      THE REGISTERS AFFECTED BY THE TEST ARE:
                        ;*      SP = 177777
                        ;*
                        ;;*****************************************************************
165020                  TST3:
165020  005306                  DEC     SP              ;N=1,Z=0;V=0,C=0,SP=177777
165022  100004                  BPL     1$              ; V 321 BRANCH IF N=0
165024  001403                  BEQ     1$              ; V 324 BRANCH IF Z=1
165026  002002                  BGE     1$              ; V 322 BRANCH IF (N XOR V)=0
165030  003001                  BGT     1$              ; V 322 BRANCH IF Z AND (N XOR V) ARE BOTH 0
165032  003401                  BLE     TST4            ; * 326 BRANCH IF [Z OR (N XOR V)]=1
165034  000000          1$:     HALT
                        ;;*****************************************************************
                        .SBTTL  TEST4   TEST "ROR", MODE "B", AND "BVC","BHIS","BHI","BNE"
                        ;*
                        ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 1, Z = 0, V = 0, AND C = 0,
                        ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                        ;*      R3 = ? R4 = ? R5 = ? SP = 177777
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                        ;*      N = 0, Z = 0, V = 1, AND C = 1
                        ;*      THE REGISTERS AFFECTED BY THE TEST ARE:
                        ;*      SP = 077777
                        ;*
                        ;;*****************************************************************
165036                  TST4:
165036  006006                  ROR     SP              ;N=0,Z=0;V=1,C=1,SP=077777
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                                        BVC     15              ; V 321 BRANCH IF V=0
                                        BHIS    15              . V 321 BRANCH IF C=0
                                        BHI     15              ; V 321 BRANCH IF C AND Z ARE BOTH 0
                                        BNE     TST5            . = 328 BRANCH IF Z=0
                                15:     HALT

                                ;!=====================================================================
                                        .SBTTL  TEST5   TEST "BHI", "BLT", AND "BLOS"
                                ;=
                                ;=      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                                ;=      N = 0, Z = 0, V = 1, AND C = 1.
                                ;=      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                                ;=      R3 = ? R4 = ? R5 = ? SP = 077777
                                ;=      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                                ;=      N = 1, Z = 1, V = 1, AND C = 1
                                ;=      THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.
                                ;=
                                ;!=====================================================================
                                TST5:
                                        SEZ                     ;N=0,Z=1;V=1,C=1
                                        BHI     15              ; V 321 BRANCH IF Z AND C ARE BOTH 0
                                        SEN                     ;N=1,Z=1;V=1,C=1
                                        BLT     15              ; V 324 BRANCH IF (N XOR V)=1
                                        BLOS    TST6            ; = 325 BRANCH IF (Z OR C)=1
                                15:     HALT                    ;STOP HERE IF A BRANCH FAILED

                                ;!=====================================================================
                                        .SBTTL  TEST6   TEST "BLE" AND "BGT"
                                ;=
                                ;=      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                                ;=      N = 1, Z = 1, V = 1, AND C = 1.
                                ;=      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                                ;=      R3 = ? R4 = ? R5 = ? SP = 077777
                                ;=      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                                ;=      N = 1, Z = 0, V = 1, AND C = 1
                                ;=      THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.
                                ;=
                                ;!=====================================================================
                                TST6:
                                        CLZ                     ;N=1,Z=0;V=1,C=1
                                        BLE     15              ; V 324 BRANCH IF [Z OR (N XOR V)]=1
                                        BGT     TST7            ; = 328 BRANCH IF Z AND (N XOR V) ARE BOTH 0
                                15:     HALT                    ;STOP HERE IF A BRANCH FAILED

                                ;!=====================================================================
                                        .SBTTL  TEST7   TEST REGISTER DATA PATH AND MODES "2", "3", "6"
                                ;=
                                ;=      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;=      N = 1, Z = 0, V = 1, AND C = 1.
                                ;=      THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
                                ;=      R3 = ?, R4 = ?, R5 = ?, SP = 077777.
                                ;=      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;=      N = 0, Z = 1, V = 0, AND C = 0.
                                ;=      THE REGISTERS ARE LEFT AS FOLLOWS:
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                                        ;*      R0 = 125252, R1 = 000000, R2 = 125252, R3 = 125252
                                        ;*      R4 = 125252, R5 = 125252, SP = 125252, AND MAPL00 = 125252
                                        ;*
                                        ;;*****************************************************************
                                        TST7:
 165076  012706  125252                          MOV     #125252,SP      ;N=1,Z=0;V=0,C=1,SP=125252
 165102  010600                                  MOV     SP,R0           ;N=1,Z=0;V=0,C=1,R0=125252
 165104  010001                                  MOV     R0,R1           ;N=1,Z=0;V=0,C=1,R1=125252
 165106  010102                                  MOV     R1,R2           ;N=1,Z=0,V=0,C=1,R2=125252
 165110  010203                                  MOV     R2,R3           ;N=1,Z=0,V=0,C=1,R3=125252
 165112  010304                                  MOV     R3,R4           ;N=1,Z=0;V=0,C=1,R4=125252
 165114  010405                                  MOV     R4,R5           ;N=1,Z=0;V=0,C=1,R5=125252
 165116  010537                                  MOV     R5,@(PC)+       ;N=1,Z=0;V=0,C=1
 165120  170200                 ;NOMAP:  .WORD   MAPL0                   ;MAPL0=125252
 165122  167701  177772                 SUB     @#NOMAP,R1              ;N=0,Z=1,V=0,C=0, AND R1=000000
 165126  002401                         BLT     1$                      ; V 324 BRANCH IF (N XOR V)=1
 165130  001401                         BEQ     TST10                   ; * 326 BRANCH IF Z=1
 165132  000000                 1$:     HALT
                                        ;;*****************************************************************
                                                .SBTTL  TEST10  TEST "ROL", "BCC", "BLT", AND MODE "6"
                                        ;*
                                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                                        ;*      R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
                                        ;*      MAPL00 = 125252
                                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                        ;*      N = 0, Z = 0, V = 1, AND C = 1,
                                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                                        ;*      MAPL00 WHICH SHOULD NOW EQUAL 052524,
                                        ;*
                                        ;;*****************************************************************
 165134                                 TST10:
 165134  006167  003040                          ROL     MAPL0           ;N=0,Z=0;V=1,C=1, AND MAPL00 = 052524
 165140  103001                                  BCC     1$              ; V 321 BRANCH IF C=0
 165142  002401                                  BLT     TST11           ; * 326 BRANCH IF (N XOR V)=1
 165144  000000                 1$:     HALT
                                        ;;*****************************************************************
                                                .SBTTL  TEST11  TEST "ADD", "INC", "COM", AND "BCS", "BLE"
                                        ;*
                                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                        ;*      N = 0, Z = 0, V = 1, AND C = 1,
                                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                                        ;*      R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252
                                        ;*      MAPL00 = 052524,
                                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                        ;*      N = 0, Z = 1, V = 0, AND C = 0,
                                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                                        ;*      R3 WHICH NOW EQUALS 000000, AND R1 WHICH IS ALSO 000000
                                        ;*
                                        ;;*****************************************************************
 165146                                 TST11:
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```
                                                        ;(MAPL00 = 052524) + (R3 = 125252)
165146  060703  013020          ADD     MAPL0,R3        ;N=1,Z=0,V=0,C=0, AND R3=177776
165152  005203                  INC     R3              ;N=1,Z=0,V=0,C=0, AND R3=177777
165154  005103                  COM     R3              ;N=0,Z=1,V=0,C=1, AND R3 = 000000
165156  060301                  ADD     R3,R1           ;N=0,Z=1,V=0,C=0, AND R1 = 000000
165160  103401                  BCS     1$              ; V 324 BRANCH IF C=1
165162  003401                  BLE     TST12           ; + 326 BRANCH IF (Z OR (N XOR V))=1
165164  000000          1$:     HALT

                        ;;=====================================================================
                                .SBTTL  TEST12  TEST "ROR", "BIS", "ADD", AND "BLO", "BGE"
                        ;+
                        ;+      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;+      N = 0, Z = 1, V = 0, AND C = 0.
                        ;+      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                        ;+      R3 = 000000, R4 = 125252, R5 = 125252, SP = 125252.
                        ;+      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;+      N = 0, Z = 1, V = 0, AND C = 0.
                        ;+      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;+      R3 WHICH SHOULD BE MODIFIED BACK TO 000000, AND
                        ;+      R4 WHICH SHOULD NOW EQUAL 052525
                        ;+
                        ;;=====================================================================
165166                  TST12:
165166  006004                  ROR     R4              ;N=0,Z=0,V=1,C=0, AND R4 = 052525
165170  050403                  BIS     R4,R3           ;N=0,Z=0,V=0,C=0, AND R3 = 052525
165172  060503                  ADD     R5,R3           ;N=1,Z=0,V=0,C=0, AND R3 = 177777
165174  005203                  INC     R3              ;N=0,Z=1,V=0,C=0, AND R3 = 000000
165176  103401                  BLO     1$              ; V 324 BRANCH IF C=1
165200  002001                  BGE     TST13           ; + 328 BRANCH IF (N XOR V)=0
165202  000000          1$:     HALT

                        ;;=====================================================================
                                .SBTTL  TEST13  TEST "DEC" AND "BLOS", "BLT"
                        ;+
                        ;+      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;+      N = 0, Z = 1, V = 0, AND C = 0.
                        ;+      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                        ;+      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                        ;+      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;+      N = 1, Z = 0, V = 0, AND C = 0.
                        ;+      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;+      R1 WHICH SHOULD NOW EQUAL 177777
                        ;+
                        ;;=====================================================================
165204                  TST13:
165204  005301                  DEC     R1              ;N=1,Z=0,V=0,C=0,R1=177777
165206  101401                  BLOS    1$              ; V 324 BRANCH IF (Z OR C)=1
165210  002401                  BLT     TST14           ; + 326 BRANCH IF (N XOR V)=1
165212  000000          1$:     HALT

                        ;;=====================================================================
                                .SBTTL  TEST14  TEST "COM", "BIC", AND "BGT", "BGE", "BLE"
                        ;+
```

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                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 1, Z = 0, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = 125252, R1 = 177777, R2 = 125252
                                ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 0, V = 1, AND C = 1.
                                ;*      THE REGISTER  ARE LEFT UNCHANGED EXCEPT FOR
                                ;*      R0 WHICH SHOULD NOW EQUAL 052525, AND
                                ;*      R1 WHICH SHOULD NOW EQUAL 052524
                                ;*
                                ;;*****************************************************************
165214                          TST14:
165214  005100                          COM     R0              ;N=0,Z=0,V=0,C=1, AND R0 = 052525
165216  101401                          BLOS    2$              ; * 325 BRANCH IF (Z OR C)=1
165220  000000                          HALT                    ;STOP HERE IF BRANCH FAILED
165222  040001                  2$:     BIC     R0,R1           ;N=1,Z=0,V=0,C=1, AND R1 = 125252
165224  060101                          ADD     R1,R1           ;N=0,Z=0,V=1,C=1, AND R1 = 052524
165226  003002                          BGT     1$              ; V 322 BRANCH IF Z AND (N XOR V) ARE BOTH 0
165230  002001                          BGE     1$              ; V 322 BRANCH IF (N XOR V)=0
165232  003401                          BLE     TST15           ; * 326 BRANCH IF [Z OR (N XOR V)]=1
165234  000000                  1$:     HALT
                                ;;*****************************************************************
                                        .SBTTL  TEST15  TEST "ADC", "CMP", "BIT", AND "BNE","BGT","BEQ"
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 0, V = 1, AND C = 1.
                                ;*      THE REGISTERS ARE: R0 = 052525, R1 = 052524, R2 = 125252
                                ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE NOW:
                                ;*      R0 = 052525, R1 = 000000, R2 = 125252, R3 = 000000
                                ;*      R4 = 052525, R5 = 052525, SP = 125252.
                                ;*
                                ;;*****************************************************************
165236                          TST15:
165236  005501                          ADC     R1              ;N=0,Z=0,V=0,C=0, AND R1 = 052525
165240  020401                          CMP     R4,R1           ;N=0,Z=1;V=0,C=0
165242  001005                          BNE     1$              ; V 322 BRANCH IF Z=0
                                                                ;R1 = 052525  R5 = 125252
165244  030105                          BIT     R1,R5           ;N=0,Z=1;V=0,C=0
165246  003003                          BGT     1$              ; V 322 BRANCH IF Z AND (N XOR V) ARE BOTH 0
165250  005105                          COM     R5              ;N=0,Z=0,V=0,C=1, AND R5 = 052525
165252  160501                          SUB     R5,R1           ;N=0,Z=1;V=0,C=0, AND R1 = 000000
165254  001401                          BEQ     TST16           ; * 326 BRANCH IF Z=1
165256  000000                  1$:     HALT
                                ;;*****************************************************************
                                        .SBTTL  TEST16  TEST "MOVB", "SOB", "CLR", "TST" AND "BPL", "BNE"
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = 052525, R1 = 000000, R2 = 125252
```

B2

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                                        ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
                                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                        ;*      R0 IS DECREMENTED BY A SOB INSTRUCTION TO 000000
                                        ;*      R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000000
                                        ;*
                                        ;;=====================================================================
165260                                  TST16:
165260  112700  177401                          MOVB    #177401,R0      ;N=0,Z=0,V=0,C=0, AND R0 = 000001
165264  100001                                  BPL     2$              ; = 328 BRANCH IF N=0
165266  000000                          1$:     HALT                    ;STOP IF "BPL" FAILED
165270  077002                          2$:     SOB     R0,1$           ;DO NOT LOOP SINCE (R0 - 1) = 0
165272  005001                                  CLR     R1              ;N=0, Z=1, V=0, C=0, AND R1 = 000000
165274  005201                          3$:     INC     R1              ;INCREMENT 64K TIMES (Z == 16)
165276  077002                                  SOB     R0,3$           ;LOOP BACK TO "INC" 64K TIMES
165300  005700                                  TST     R0              ;N=0,Z=1,V=0,C=0, AND R0 = 000000
165302  001002                                  BNE     4$              ; V 322 BRANCH IF Z=0
165304  005701                                  TST     R1              ;N=0,Z=1,V=0,C=0, AND R1 = 000000
165306  001401                                  BEQ     TST17           ; = 326 BRANCH IF Z=1
165310  000000                          4$:     HALT
                                        ;;=====================================================================
                                                .SBTTL  TEST17  TEST "ASR", "ASL"
                                        ;*
                                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
                                        ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
                                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                        ;*      N = 0, Z = 0, V = 0, AND C = 0.
                                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                                        ;*      R0 WHICH IS NOW EQUAL TO 000000,
                                        ;*      R1 WHICH IS NOW 000001, AND
                                        ;*      R2 WHICH IS NOW 000000.
                                        ;*
                                        ;;=====================================================================
165312                                  TST17:
165312  012700  100000                          MOV     #100000,R0      ;R0=100000
165316  005201                                  INC     R1              ;R1=000001
165320  012702  000020                          MOV     #^D16,R2        ;SET COUNTER TO 16 DECIMAL
165324  006200                          1$:     ASR     R0              ;RIGHT SHIFT R0, SIGN EXTEND (16 TIMES)
165326  005500                                  ADC     R0              ;ADD CARRY (0 UNTIL LAST TIME)
165330  006301                                  ASL     R1              ;LEFT SHIFT R1 (16 TIMES)
165332  005501                                  ADC     R1              ;ADD CARRY (0 UNTIL LAST TIME)
165334  077203                                  SOB     R2,1$           ;LOOP BACK 16 DECIMAL TIMES
                                                                        ;AT THE END OF THE LOOP
                                                                        ;R0 = 000000  AND  R1 = 000001
165336  060001                                  ADD     R0,R1           ;N=0,Z=0,V=0,C=0  R1=000001, R0=000000
165340  003401                                  BLE     2$              ; V 324 BRANCH IF [Z OR (N XOR V)]=1
165342  003001                                  BGT     TST20           ; = 320 BRANCH IF Z AND (N XOR V) ARE BOTH 0
165344  000000                          2$:     HALT
                                        ;;=====================================================================
                                                .SBTTL  TEST20  TEST ASH, AND SWAB
```

```
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 0, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = 000000, R1 = 000001, R2 = 000000
                                ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 1.
                                ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                                ;*      R1 WHICH SHOULD NOW EQUAL 000000
                                ;*
                                ;!*****************************************************************
165346                          TST20:
165346  072127  000007                ASH     #7,R1           ;LEFT SHIFT BITS INTO BIT7
                                                                ;N=0,Z=0,V=0,C=0, AND R1 = 000200
165352  105701                        TSTB    R1              ;LOWER BYTE SHOULD BE NEGATIVE
                                                                ;N=1,Z=0,V=0,C=0
165354  100401                        BMI     1$              ; * 325 BRANCH IF N=1
165356  000000                        HALT                    ;"ASH" MUST HAVE FAILED
165360  000301                1$:     SWAB    R1              ;SWITCH BYTES OF R1, R1 = 000000
                                                                ;N=1,Z=0,V=0,C=0
165362  072127  177761                ASH     #-#D15,R1       ;RIGHT SHIFT R1 15 PLACES SIGN EXTEND
                                                                ;N=1,Z=0,V=0,C=0, R1 = 177777
165366  005201                        INC     R1              ;N=0,Z=1,V=0,C=1, R1 = 000000
165370  001401                        BEQ     TST21           ; * 326 BRANCH IF Z=1
165372  000000                        HALT                    ;EITHER "SWAB" OR "ASH" FAILED

                                ;!*****************************************************************
                                        .SBTTL  TEST21  TEST 16 KERNEL P.A.R.'S
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 1.
                                ;*      THE REGISTERS ARE: R0 = 000000, R1 = 000000, R2 = 000000
                                ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                ;*      THE REGISTERS NOW EQUAL:
                                ;*      R0 = 172400, R1 = 000000, R2 = 000000, R3 = 000000
                                ;*      R4 = 052525, R5 = 125252, SP = 125252.
                                ;*      ALL KERNEL P.A.R.'S = 125252.
                                ;*
                                ;!*****************************************************************
165374                          TST21:
165374  012700  172340                MOV     #KIPAR0,R0      ;FIRST "PAR" TO BE CHECKED
165400  012701  000020                MOV     #-#D16,R1       ;DO KIPAR0 THRU KDPAR7
165404  005105                        COM     R5              ;R5=125252
165406  010420                1$:     MOV     R4,(R0)+        ;PAR=052525
165410  020460  177776                CMP     R4,-2(R0)       ;DID IT LOAD PROPERLY?
165414  001014                        BNE     2$              ; V BRANCH IF NO  R0 = PAR + 2
165416  105140                        COMB    -(R0)           ;COMPLEMENT HIGH BYTE  PAR=125125
165420  120510                        CMPB    R5,(R0)         ;CHECK THE HIGH BYTE
165422  001011                        BNE     2$              ; V BRANCH IF BAD  R0 = PAR + 1
165424  120440                        CMPB    R4,-(R0)        ;CHECK THE LOW BYTE DIDN'T CHANGE
165426  001007                        BNE     2$              ; V BRANCH IF IT CHANGED  R0 = PAR
165430  105110                        COMB    (R0)            ;COMPLEMENT THE LOW BYTE  PAR=125252
```

```
                                        CMPB    R5,(R0)+        ;CHECK THE LOW BYTE
                                        BNE     2$              ; V BRANCH IF BAD  R0 = PAR + 1
                                        CMPB    R5,(R0)+        ;CHECK THE HIGH BYTE
                                        BNE     2$              ; V BRANCH IF IT FAILED  R0 = PAR + 2
                                        SOB     R1,1$           ;LOOP UNTIL KDPAR7 HAS BEEN TESTED
                                        BR      TST22           ; = BRANCH TO NEXT TEST
                                2$:     HALT                    ;A P.A.R. FAILED TO HOLD THE RIGHT DATA
                                                                ;CHECK R0 FOR THE ADDRESS


                                ;;======================================================================
                                        .SBTTL  TEST22  TEST AND LOAD KIPDR'S
                                ;=
                                ;=      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;=      N = 0, Z = 1, V = 0, AND C = 0.
                                ;=      THE REGISTERS ARE: R0 = 172300, R1 = 000000, R2 = 000000
                                ;=      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                                ;=      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;=      N = 0, Z = 1, V = 0, AND C = 0.
                                ;=      THE REGISTERS THAT ARE MODIFIED ARE:
                                ;=      R0 = 172300, R1 = 000000, R2 = 077406
                                ;=      ALL KERNEL I-SPACE P.D.R.'S (172300 - 172316) = 077406
                                ;=
                                ;;======================================================================
                                TST22:
                                        MOV     #KIPDR7+2,R0    ;START WITH LAST "PDR"
                                        MOV     #^D8,R1         ;DO KIPDR7 THRU KIPDR0
                                        MOV     #077406,R2      ;PATTERN TO TEST "PDR'S"
                                1$:     MOV     R2,-(R0)        ;LOAD "PDR" UNDER TEST
                                        CMP     (R0),R2         ;SEE IF THE DATA LOADED IS CORRECT
                                        BEQ     2$              ;BRANCH IF THE DATA MATCHES
                                        HALT                    ;A "PDR" HAS FAILED
                                                                ;R0 HAS THE ADDRESS OF THE BAD "PDR"
                                                                ;R2 HAS THE EXPECTED DATA
                                2$:     SOB     R1,1$           ;LOOP UNTIL ALL EIGHT "PDR'S" HAVE BEEN
                                                                ;TESTED


                                ;;======================================================================
                                        .SBTTL  TEST23  TEST "JSR", "RTS", "RTI", & "JMP"
                                ;=
                                ;=      THIS TEST FIRST SETS THE STACK POINTER TO "KDPAR7" (172376),
                                ;=      AND THEN VERIFIES THAT "JSR", "RTS", "RTI", AND "JMP"
                                ;=      ALL WORK PROPERLY.
                                ;=
                                ;=      ON ENTRY TO THIS TEST THE STACK POINTER "SP" IS INITIALIZED
                                ;=      TO 172376 AND IS LEFT THAT WAY ON EXIT.
                                ;=
                                ;;======================================================================
                                TST23:

                                        MOV     #KDPAR7,SP      ;SET UP THE STACK POINTER
                                        JSR     PC,1$           ;TRY TO JSR TO 1$
                                100$:   HALT                    ;THE "JSR" MUST HAVE FAILED
                                1$:     CMP     #100$,(SP)      ;WAS THE CORRECT ADDRESS PUSHED?
```

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                        001401                  BEQ     2$              ;BRANCH IF YES
                        000000                  HALT                    ;WRONG THING PUSHED ON STACK
165530          012716  165530          2$:     MOV     #3$,(SP)        ;CHANGE THE ADDRESS ON THE STACK
                        000207                  RTS     PC              ;TRY TO RETURN TO 3$
                        000000                  HALT                    ;DID NOT RETURN PROPERLY
                        005046          3$:     CLR     -(SP)           ;PUSH A ZERO ON THE STACK
165542          012746  165542                  MOV     #4$,-(SP)       ;PUSH THE RETURN ADDRESS ON STACK
                        000002                  RTI                     ;SEE IF AN "RTI" WORKS
                        000000                  HALT                    ;THE "RTI" FAILED
165550          000137  165550          4$:     JMP     @#5$            ;TRY TO "JMP"
                        000000                  HALT                    ;THE "JMP" FAILED
165550                                  5$:                             ;ADDRESS TO "JMP" TO

                                        ;;**************************************************************************
                                                .SBTTL  TEST24  LOAD AND TURN ON MEMORY MANAGEMENT AND THE UNIBUS MAP
                                        ;*
                                        ;*      THIS TEST IS ONLY EXECUTED IF THE UPPER 4 BITS <15:12> OF
                                        ;*      THE SWITCH REGISTER ARE NON-ZERO.  THE TEST WILL LOAD MEMORY
                                        ;*      MANAGEMENT TO RELOCATE TO THE 32K BLOCK NUMBER SPECIFIED.
                                        ;*      IT WILL ALSO SET UP THE UNIBUS MAP REGISTERS 0 THRU 6 TO
                                        ;*      RELOCATE THE UNIBUS ADDRESSES CORRECTLY. (IE. IF BITS <15:12>
                                        ;*      SPECIFY BLOCK NUMBER 3, THEN YOU WANT TO BOOT INTO
                                        ;*      MEMORY FROM 96K TO 128K.  THE KIPAR'S WILL BE LOADED AS FOLLOWS:
                                        ;*      KIPAR0 = 000000, KIPAR1 = 000200, KIPAR2 = 000400, KIPAR3 = 000600
                                        ;*      KIPAR4 = 007000, KIPAR5 = 007200, KIPAR6 = 007400.)
                                        ;*      KIPAR7 WILL ALWAYS EQUAL 177600.
                                        ;*      THE UNIBUS MAP REGISTERS WILL THEN BE SET AS FOLLOWS:
                                        ;*      MAPL0 = 000000, MAPH0 = 03, MAPL1 = 020000, MAPH1 = 03,
                                        ;*      MAPL2 = 040000, MAPH2 = 03, MAPL3 = 060000, MAPH3 = 03,
                                        ;*      MAPL4 = 100000, MAPH4 = 03, MAPL5 = 120000, MAPH5 = 03,
                                        ;*      MAPL6 = 140000, MAPH6 = 03.
                                        ;*
                                        ;;**************************************************************************
165558                                  TST24:
165558          013702  177570                  MOV     @#SWR,R2        ;READ THE SWITCH REGISTER
165554          001002                  BNE     10$                     ;SKIP THE NEXT INSTRUCTION IF NOT ZERO
165556          013702  173024                  MOV     @#173024,R2     ;READ THE SWITCHES ON THE M9301
165562          072227  177770          10$:    ASH     #-2,R2          ;RIGHT SHIFT BITS <15:12> 2 PLACES
165566          042702  141777                  BIC     #^C03#000,R2    ;LEAVE ONLY BITS <13:10> IN R2
165572          001433                  BEQ     TST25                   ;GO TO NEXT TEST IF R2 IS ZERO NOW
                                        ;*
                                        ;*      THIS NEXT PORTION OF CODE WILL BE RUN ONLY IF YOU ARE
                                        ;*      BOOTING INTO MEMORY OTHER THAN PHYSICAL 0 TO 28K.
                                        ;*
165574          012703  172340                  MOV     #KIPAR0,R3      ;ADDRESS OF FIRST "PAR" TO LOAD
165600          012701  000007                  MOV     #^D7,R1         ;LOAD KIPAR0 THRU KIPAR6
165604          010223          15$:    MOV     R2,(R3)+                ;LOAD THE KERNEL I-SPACE P.A.R.'S
165606          062702  000200                  ADD     #200,R2         ;MAKE R2 POINT TO NEXT 4K BLOCK
165612          077104                  SOB     R1,15$                  ;LOOP UNTIL KIPAR6 HAS BEEN LOADED
165614          012710  177600                  MOV     #177600,(R0)    ;MAP KIPAR7 TO I/O PAGE
                                        ;*
                                        ;*      NOW LOAD THE UNIBUS MAP TO REFERENCE THE SAME MEMORY
                                        ;*      AS MEMORY MANAGEMENT DOES.
```

```
                                        ;*
165622  012227  177760                  ASH     #-#D10,R2       ;RIGHT SHIFT R2 10 PLACES
165624  005003                          CLR     R3              ;START WITH R3 = 000000
165626  012700  170200                  MOV     #MAPL0,R0       ;ADDRESS OF FIRST MAP REGISTER
165632  012701  000007                  MOV     #*D7,R1         ;PREPARE TO LOAD SEVEN MAP REGISTERS
165636  010320                  2$:     MOV     R3,(R0)+        ;LOAD LOWER 16 BITS OF THE MAP REGISTER
165640  010220                          MOV     R2,(R0)+        ;LOAD UPPER 6 BITS OF THE MAP REGISTER
165642  062703  020000                  ADD     #20000,R3       ;POINT TO THE NEXT 4K BLOCK
165646  077105                          SOB     R1,2$           ;LOOP UNTIL SEVEN MAP REGS ARE LOADED
                                        
165650  012737  000060  172516          MOV     #60,@#MMR3      ;ENABLE 22-BIT MAPPING AND UNIBUS MAP
165656  005237  177572                  INC     @#MMR0          ;TURN ON FULL RELOCATION
                                        
                                        
                                        ;;*****************************************************************
                                        .SBTTL  TEST25  TEST MAIN MEMORY FROM VIRTUAL 1000 TO 20K
                                        ;*
                                        ;*      THIS TEST WILL TEST MAIN MEMORY WITH THE CACHE DISABLED, FROM
                                        ;*      VIRTUAL ADDRESS 001000 TO 157776.  IF THE DATA DOES NOT COMPARE
                                        ;*      PROPERLY THE TEST WILL HALT AT EITHER 165748 OR 165796. IF A
                                        ;*      PARITY ERROR OCCURS THE TEST WILL HALT AT ADDRESS 165776, WITH
                                        ;*      THE PC + 2 ON THE STACK WHICH IS IN THE KERNEL D-SPACE P.A.R.'S.
                                        ;*
                                        ;*      IN THIS TEST THE REGISTERS ARE INITIALIZED AS FOLLOWS:
                                        ;*      R0 = 001000, R1 = DATA READ, R2 = 007400, R3 = 001000
                                        ;*      R4 = 007400, R5 = 177746 (CONTROL REG.) SP = 172376
                                        ;*
                                        ;;*****************************************************************
165662                                  TST25:
165662  010216                          MOV     R2,(SP)         ;SAVE R2 FOR THE UPPER SIX BITS
                                                                ;OF THE UNIBUS DEVICE'S BUS ADDRESS
                                                                ;IN ADDRESS 17772376 (KDPAR7)
                                        
165664  012737  165776  000114          MOV     #PARHLT,@#114   ;SET UP PARITY VECTOR
165672  005037  000116                  CLR     @#116           ;SET PROCESSOR STATUS WORD TO ZERO
165676  012705  177746                  MOV     #177746,R5      ;CACHE CONTROL REGISTER ADDRESS
165702  012715  000014                  MOV     #MISS,(R5)      ;FORCE MISS BOTH GROUPS
165706  012702  007400                  MOV     #7400,R2        ;COUNT STORAGE
165712  012703  001000                  MOV     #1000,R3        ;FIRST ADDRESS STORAGE
165716  010204                          MOV     R2,R4           ;SETUP COUNTER
165720  010300                          MOV     R3,R0           ;SETUP FIRST ADDRESS
165722  010020                  1$:     MOV     R0,(R0)+        ;LOAD EACH ADDRESS WITH ITS
                                                                ;OWN ADDRESS
165724  077402                          SOB     R4,1$           ;LOOP UNTIL DONE
165726  010204                          MOV     R2,R4           ;SETUP COUNTER AND FIRST ADDRESS
165730  010300                          MOV     R3,R0           ;SET STARTING ADDRESS IN R0
165732  011001                  2$:     MOV     (R0),R1         ;GET THE DATA
165734  020001                          CMP     R0,R1           ;IS IT CORRECT?
165736  001401                          BEQ     3$              ;BRANCH IF YES
165740  000000                          HALT                    ;R0=ADDRESS, R1=DATA
165742  005120                  3$:     COM     (R0)+           ;COMPLEMENT DATA AND INCREMENT ADDRESS
165744  077406                          SOB     R4,2$           ;LOOP UNTIL DONE
165746  014001                  4$:     MOV     -(R0),R1        ;READ THE DATA (IT SHOULD NOW BE THE
                                                                ;COMPLEMENT OF THE ADDRESS)
```

```
 669  165758  005101                        COM     R1              ;COMPLEMENT BEFORE CHECKING
 670  165752  020001                        CMP     R0,R1           ;IS THE DATA CORRECT?
 671  165754  001401                        BEQ     5$              ;BRANCH IF YES
 672  165756  000000                        HALT                    ;R0=ADDRESS R1=-DATA
 673  165760  077206                5$:     SOB     R2,4$           ;LOOP UNTIL DONE
 674  165762  012737  173762  000114        MOV     #CONT,@#114     ;SET PARITY VECTOR TO CODE THAT
 675                                                                ;WILL TRY TO CONTINUE AND BOOT
 676                                                                ;IF THE CACHE FAILS.
 677  165770  005046                        CLR     -(SP)           ;SET THE CYCLE FLAG TO ZERO
 678  165772  000137  173030                JMP     @#TST26         ;JUMP TO SECOND HALF OF THE ROM
 679  165776  000000            PAEHLT:     HALT                    ;HALTING HERE MEANS A PARITY ERROR
 680
```

```
                                          .SBTTL  BOOTSTRAP ENTRY POINT IS AT 17773000
                                          ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                          ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                          ;*
                                          ;*      THE REGISTER USAGE DURING THE BOOTSTRAP IS GENERALLY AS FOLLOWS:
                                          ;*
                                          ;*      R0 = THE DRIVE NUMBER RIGHT JUSTIFIED (0 - 7)
                                          ;*      R1 = THE ADDRESS OF THE MAIN CONTROL AND STATUS REGISTER
                                          ;*      R2 = THE DRIVE NUMBER POSITIONED FOR LOADING INTO DEVICE
                                          ;*      R3 = POINTER TO THE FUNCTION TABLE
                                          ;*      R4 = INDEX NUMBER TO GET THRU THE TABLES FOR THE CORRECT INFORMATION
                                          ;*
                                          ;*
                                          ;*      AFTER A SUCCESSFUL BOOT THE REGISTERS ARE AS FOLLOWS:
                                          ;*
                                          ;*      R0 = THE DRIVE NUMBER RIGHT JUSTIFIED (0 - 7)
                                          ;*      R1 = THE ADDRESS OF THE MAIN COMMAND AND STATUS REGISTER
                                          ;*
                                          ;''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''
                                          ;''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''''


        173000                                    . = BASE2
173000  000405                            BOOT:   BR      START           ;BRANCH TO START OF BOOT STRAP

                                          .SBTTL  CODE TO WAIT FOR TU10 TO COME ON LINE

173002  032761  000001  177776            WAIT:   BIT     #TUN,-2(R1)     ;IS THE SELECTED DRIVE ON LINE
173010  001774                                    BEQ     WAIT            ;WAIT FOR BIT TO BE SET BY DRIVE
173012  000430                                    BR      TU102           ;BRANCH TO CONTINUE BOOTING FROM TU10


                                          .SBTTL  THIS IS THE CODE TO READ THE SWITCH REGISTER AND DECODE IT

173014  113700  177570                    START:  MOVB    @#SWR,R0        ;READ SWITCH REGISTER INTO R0
173020  001003                                    BNE     1$              ;BRANCH TO DECODE IF THE LOWER
                                                                          ;BYTE IS NOT ZERO
173022  012700                                    MOV     (PC)+,R0        ;IF SWITCH REGISTER IS ZERO
                                                                          ;THEN READ SWITCHES ON THE M9301
                                                                          ;TO DETERMINE DEVICE TYPE AND NO.
173024  000000                                    .WORD   0               ;THIS WORD WILL BE ASSEMBLED AT 773024
173026  006200                                    ASR     R0              ;RIGHT SHIFT R0 ONE PLACE
173030  010004                            1$:     MOV     R0,R4           ;COPY DEVICE AND UNIT NUMBER
173032  042704  177407                            BIC     #^C000370,R4    ;LEAVE DEVICE NUMBER IN R4
173036  072427  177776                            ASH     #-2,R4          ;SHIFT R4 RIGHT 2 PLACES TO BE 2 - 76
173042  005744                                    TST     -(R4)           ;ADJUST R4 TO INDEX THRU TABLE (0 - 74)
173044  042700  177770                            BIC     #^C7,R0         ;LEAVE UNIT NUMBER IN R0
173050  010002                                    MOV     R0,R2           ;COPY UNIT NUMBER INTO R2
173052  000302                                    SWAB    R2              ;PUT UNIT NUMBER IN UPPER BYTE OF R2
173054  016401  173520                            MOV     CSRPTN(R4),R1   ;LOAD MAIN CSR ADDRESS INTO R1
173060  016403  173542                            MOV     CMDPTN(R4),R3   ;LOAD POINTER TO FUNCTION TABLE
173064  000174  173564                            JMP     @ADDR$(R4)      ;JUMP TO START OF PARTICULAR BOOT
```

I2

```
                                        .SBTTL  THIS IS THE START OF THE TM11/TU10 BOOT STRAP (MAGNETIC TAPE, TM11)
                                                ;COMMAND REGISTER ADDRESS IS 172522

173070  010211                  TU10:   MOV     R2,(R1)         ;LOAD UNIT NUMBER INTO C.S.R.
173072  000743                          BR      WAIT            ;GO WAIT FOR SELECTED DRIVE TO COME ONLINE
173074  052311                  TU102:  BIS     (R3)+,(R1)      ;'OR' REWIND COMMAND INTO C.S.R.
                                                                ;THIS COMMAND ALSO SETS 800 BPI 9 CHAN.
173076  105711                  1$:     TSTB    (R1)            ;SEE IF THE REWIND IS COMPLETE
173100  100376                          BPL     1$              ;WAIT FOR BIT 07 OF C.S.R. TO BE SET
173102  012761  177777  000002          MOV     #-1,2(R1)       ;SET RECORD COUNTER TO SKIP ONE RECORD
173110  112311                          MOVB    (R3)+,(R1)      ;LOAD SPACE FORWARD COMMAND INTO C.S.R.
173112  105711                  2$:     TSTB    (R1)            ;SEE IF THE SPACE IS COMPLETE
173114  100376                          BPL     2$              ;WAIT FOR BIT 07 OF C.S.R. TO BE SET
173116  005711                          TST     (R1)            ;CHECK THE ERROR FLAG FOR THE TM11/TU10
173120  100563                          BMI     AGAIN           ;RE-TRY BOOT IF THERE WAS AN ERROR
173122  000417                          BR      CMNSGO          ;BRANCH TO COMMON READ CODE IF NO ERRORS


                                        .SBTTL  THIS IS THE START OF THE TC11/TU56 BOOT STRAP (DECTAPE, TC11-G)
                                                ;COMMAND REGISTER ADDRESS IS 177342

173124  010211                  TU56:   MOV     R2,(R1)         ;LOAD UNIT NUMBER INTO C.S.R.
173126  052311                          BIS     (R3)+,(R1)      ;'OR' REWIND COMMAND INTO C.S.R.
173130  005711                  1$:     TST     (R1)            ;SEE IF ERROR BIT IS SET
173132  100376                          BPL     1$              ;WAIT UNTIL BIT 15 OF C.S.R. IS SET
173134  005761  177776                  TST     -2(R1)          ;IS THE ERROR 'END ZONE'
173140  100153                          BPL     AGAIN           ;BRANCH IF NOT 'END ZONE'
173142  010211                          MOV     R2,(R1)         ;RE-LOAD DRIVE NUMBER AND CLEAR REVERSE BIT
173144  000406                          BR      CMNSGO          ;BRANCH TO COMMON READ CODE


                                        .SBTTL  THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECPACK DISK CARTRIDGE, RK11-D)
                                                ;COMMAND REGISTER ADDRESS IS 177404

173146  072227  000005          RK05:   ASH     #5,R2           ;LEFT SHIFT UNIT NUMBER 5 PLACES
173152  010261  000006                  MOV     R2,6(R1)        ;LOAD UNIT NUMBER INTO DEVICE
173156  000401                          BR      CMNSGO          ;BRANCH TO COMMON READ CODE


                                        .SBTTL  THIS IS THE START OF THE RP11/RP03 BOOT STRAP (DISK PACK, RP11-C)
                                                ;COMMAND REGISTER ADDRESS IS 176714

173160  010211                  RP03:   MOV     R2,(R1)         ;LOAD THE UNIT NUMBER INTO THE COMMAND REG.


                                        .SBTTL  THIS IS THE START OF THE COMMON READ CODE

173162  012761  177000  000002  CMNSGO: MOV     #-512.,2(R1)    ;LOAD WORD COUNT OF 512 WORDS
173170  111311                          MOVB    (R3),(R1)       ;LOAD READ FUNCTION INTO C.S.R.
173172  105711                  1$:     TSTB    (R1)            ;SEE IF FUNCTION IS COMPLETE
173174  100376                          BPL     1$              ;WAIT UNTIL BIT 07 OF C.S.R. IS SET
173176  005711                          TST     (R1)            ;WERE THERE ANY ERRORS ON THE TRANSFER
173200  100007                          BPL     2$              ;IF NO ERRORS BRANCH TO SEC. BOOT
173202  022704  000012                  CMP     #12,R4          ;IS THIS THE RH70/TU10?
```

```
789  173206  001130                          BNE     AGAIN           ;BRANCH IF NOT TO TRY AGAIN
790  173210  022761  001000  000014          CMP     #FCL,14(R1)     ;WAS ERROR A FRAME COUNT ERROR?
791  173216  001124                          BNE     AGAIN           ;BRANCH IF NOT TO TRY AGAIN
792  173220  005011                  2$:     CLR     (R1)            ;CLEAR COMMAND REGISTER THIS WILL STOP
793                                                                  ;THE DECTAPE MOTION IF DEVICE WAS TU56
794  173222  005007                          CLR     PC              ;START SECONDARY BOOT AT VIRTUAL ZERO
795
796  173224  165000                          .WORD   165000          ;VECTOR TO THE START OF M9301 BOOTSTRAP
797  173226  000340                          .WORD   000340          ;PROCESSOR STATUS TO ASSUME AT BOOT TIME
798
799
800                                  .SBTTL  THIS IS THE START OF THE RH70/TU16 BOOT STRAP (MAGNETIC TAPE SYSTEM, TMU16)
801                                          ;COMMAND REGISTER ADDRESS IS 172440
802
803  173230  010002                  TU16:   MOV     R0,R2           ;COPY UNIT NUMBER INTO R2
804  173232  052702  001300                  BIS     #001300,R2      ;'OR' 800 BPI & FORMAT, WITH SLAVE NUMBER
805  173236  010201  000032                  MOV     R2,32(R1)       ;LOAD UNIT NUMBER
806  173242  032761  010000  000012  1$:     BIT     #MOL,12(R1)     ;IS THE MEDIUM ON LINE
807  173250  001774                          BEQ     1$              ;WAIT FOR BIT 12 OF DRIVE STATUS REG
808  173252  112311                          MOVB    (R3)+,(R1)      ;ISSUE REWIND COMMAND
809  173254  105761  000012          2$:     TSTB    12(R1)          ;IS DRIVE READY BIT SET YET?
810  173260  100375                          BPL     2$              ;WAIT FOR DRIVE READY BIT
811  173262  112311                          MOVB    (R3)+,(R1)      ;ISSUE DRIVE CLEAR COMMAND
812  173264  105761  000012          3$:     TSTB    12(R1)          ;IS DRIVE READY BIT SET?
813  173270  100375                          BPL     3$              ;WAIT UNTIL BIT 07 IS SET
814  173272  012761  177777  000006          MOV     #-1,6(R1)       ;SET SKIP COUNT TO 1 RECORD
815  173300  112311                          MOVB    (R3)+,(R1)      ;ISSUE SPACE FORWARD COMMAND
816  173302  105761  000012          4$:     TSTB    12(R1)          ;HAS THE DRIVE FINISHED THE SPACE?
817  173306  100375                          BPL     4$              ;WAIT UNTIL BIT 07 IS SET
818  173310  011661  000034                  MOV     (SP),34(R1)     ;LOAD UPPER 6 BITS OF BUS ADDRESS
819  173314  000415                          BR      CMNSRH          ;GO JOIN COMMON RH70 CODE
820
821
822                                  .SBTTL  THIS IS THE START OF THE RH70/RP04 BOOT STRAP (DISK PACK, RHP04)
823                                          ;COMMAND REGISTER ADDRESS IS 176700
824
825  173316  110061  000010          RP04:   MOVB    R0,10(R1)       ;SELECT UNIT NUMBER TO BOOT FROM
826  173322  112311                          MOVB    (R3)+,(R1)      ;ISSUE READ-IN PRESET COMMAND
827  173324  012761  014000  000032          MOV     #14000,32(R1)   ;SET FMT22 & ECC INHIBIT BITS
828  173332  011661  000050                  MOV     (SP),50(R1)     ;LOAD UPPER 6 BITS OF BUS ADDRESS
829  173336  000404                          BR      CMNSRH          ;GO JOIN THE COMMON RH70 CODE
830
831
832                                  .SBTTL  THIS IS THE START OF THE RH70/RS04 BOOT STRAP (FIXED HEAD DISK, RHS04)
833                                          ;COMMAND REGISTER ADDRESS IS 172040
834
835  173340  110061  000010          RS04:   MOVB    R0,10(R1)       ;LOAD THE DRIVE NUMBER TO BOOT FROM
836  173344  011661  000030                  MOV     (SP),30(R1)     ;LOAD UPPER  6 BITS OF BUS ADDRESS
837
838
839                                  .SBTTL  THIS IS THE START OF THE COMMON RH-70 CODE
840
841  173350  016161  000010  000016  CMNSRH: MOV     10(R1),10(R1)   ;TURN OFF ANY ACTIVE ATTENTION FLAGS
842  173356  000701                          BR      CMNSCO          ;BRANCH TO COMMON READ CODE
```

```
                                .SBTTL  THIS IS THE START OF THE RX11/RX01 BOOT STRAP (FLOPPY DISK)
                                        ;COMMAND REGISTER ADDRESS IS 177170

173360  042700  000006    RX01:   BIC     #6,R0           ;MAKE SURE UNIT NUMBER IS ZERO OR ONE
173364  001401                    BEQ     1$              ;SKIP NEXT INST IF UNIT NUMBER IS ZERO
173366  005203                    INC     R3              ;POINT TO UNIT ONE'S READ COMMAND
173370  132711  000040    1$:     BITB    #40,(R1)        ;IS THE "DONE" BIT SET?
173374  001775                    BEQ     1$              ;WAIT UNTIL THE DONE BIT IS SET
173376  111311                    MOVB    (R3),(R1)       ;LOAD THE READ COMMAND
173400  012702  000002            MOV     #2,R2           ;LOAD LOOP COUNT INTO R2
173404  105711                2$: TSTB    (R1)            ;IS THE "TR" BIT SET?
173406  100376                    BPL     2$              ;WAIT UNTIL BIT 07 OF RXCS IS SET
173410  112761  000001  000002    MOVB    #1,2(R1)        ;LOAD SECTOR NUMBER OR TRACK ADDRESS
173416  077206                    SOB     R2,2$           ;LOOP BACK TO LOAD SECTOR NUMBER
173420  032711  100040    3$:     BIT     #100040,(R1)    ;CHECK FOR "ERROR" OR "DONE"
173424  001775                    BEQ     3$              ;WAIT UNTIL BIT 15 OR BIT 05 OF RXCS IS SET
173426  100420                    BMI     AGAIN           ;BRANCH TO TRY AGAIN IF ERROR
173430  112711  000003            MOVB    #3,(R1)         ;LOAD "EMPTY BUFFER" COMMAND INTO RXCS
173434  105711                4$: TSTB    (R1)            ;IS 'TR' BIT SET?
173436  100376                    BPL     4$              ;WAIT UNTIL BIT 07 OF RXCS IS SET
173440  116122  000002            MOVB    2(R1),(R2)+     ;STORE DATA (R2 STARTS AT 0 & GOES TO 177)
173444  105702                    TSTB    R2              ;IS BIT 07 OF MEMORY ADDRESS SET?
173446  100372                    BPL     4$              ;BRANCH IF NOT 128 BYTES YET
173450  005007                    CLR     PC              ;START SECONDARY BOOT AT VIRTUAL ZERO


                                .SBTTL  THIS IS THE START RESERVED FOR A FUTURE DEVICE

173452  000000    FUTDEV: HALT                            ;THERE IS NO BOOT YET
173454  000000            .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
173456  000000            .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
173460  000000            .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
173462  000000            .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
173464  000000            .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION
173466  000000            .WORD   000000                  ;RESERVED FOR FUTURE BOOT EXPANSION


173470  000005    AGAIN:  RESET                           ;CLEAR THE WORLD AFTER ERROR
173472  000137  165550    JMP     @#TST24                 ;GO SETUP MEMORY MANAGEMENT AND TEST
                                                        ;MAIN MEMORY AND THE CACHE AGAIN.
```

L2

```
                                .SBTTL  FUNCTION CODES FOR THE ALL OF THE DEVICES

173476  200017          TU16S:  .WORD   00001/          ;REWIND SELECTED DRIVE AND SET 800 BPI
173500      011                 .BYTE   011             ;SPACE FORWARD COMMAND FOR TU16
173501      003                 .BYTE   003             ;READ COMMAND FOR TU16

173502  004003          TU56S:  .WORD   004003          ;SEARCH FOR BLOCK 0, REVERSE DIRECTION
173504                  RK05S:
173504      005         RP03S:  .BYTE   005             ;READ COMMAND FOR TU56, RK05, RP03

173505      007         TU16S:  .BYTE   007             ;REWIND SELECTED DRIVE
173506      011                 .BYTE   011             ;DRIVE CLEAR COMMAND
173507      031                 .BYTE   031             ;SPACE FORWARD
173510      071                 .BYTE   071             ;READ FORWARD

173511      021         RP04S:  .BYTE   021             ;READ-IN PRESET
173512      071         RS04S:  .BYTE   071             ;READ COMMAND FOR RP04 & RS04

173513      007         RX01S:  .BYTE   007             ;READ SECTOR COMMAND FOR DRIVE ZERO
173514      027                 .BYTE   027             ;READ SECTOR COMMAND FOR DRIVE ONE

173515      000         FUTDES: .BYTE   0               ;SPACE FOR FUTURE DEVICE COMMAND
173516  000000                  .WORD   0               ;SPACE FOR MORE COMMANDS
```

```
                                .SBTTL  COMMAND AND STATUS REGISTER ADDRESS TABLE

173520  172522  CSRPTR: .WORD   172522          ;THIS IS THE C.S.R. ADDRESS FOR TU18
173522  177342          .WORD   177342          ;THIS IS THE C.S.R. ADDRESS FOR THE TU56
173524  177404          .WORD   177404          ;THIS IS THE C.S.R. ADDRESS FOR THE RK05
173526  176714          .WORD   176714          ;THIS IS THE C.S.R. ADDRESS FOR THE RP03
173530  000000          .WORD   0               ;THIS IS THE C.S.R. ADDRESS OF A FUTURE DEVICE
173532  172440          .WORD   172440          ;THIS IS THE C.S.R. ADDRESS FOR THE RH70/TU16
173534  176700          .WORD   176700          ;THIS IS THE C.S.R. ADDRESS FOR THE RH70/RP04
173536  172040          .WORD   172040          ;THIS IS THE C.S.R. ADDRESS FOR THE RH70/RS04
173540  177170          .WORD   177170          ;THIS IS THE C.S.R. ADDRESS FOR RX11/RX01

                                .SBTTL  FUNCTION POINTER TABLE

173542  173476  CMDPTR: .WORD   TU18$          ;POINTER TO FUNCTION TABLE FOR THE TU18
173544  173502          .WORD   TU56$          ;POINTER TO FUNCTION TABLE FOR THE TU56
173546  173534          .WORD   RK05$          ;POINTER TO FUNCTION TABLE FOR THE RK05
173550  173564          .WORD   RP03$          ;POINTER TO FUNCTION TABLE FOR THE RP03
173552  173615          .WORD   FUTDE$         ;POINTER TO FUNCTION TABLE FOR A FUTURE DEVICE
173554  173505          .WORD   TU16$          ;POINTER TO FUNCTION TABLE FOR THE RH70/TU16
173556  173511          .WORD   RP04$          ;POINTER TO FUNCTION TABLE FOR THE RH70/RP04
173560  173512          .WORD   RS04$          ;POINTER TO FUNCTION TABLE FOR THE RH70/RS04
173562  173513          .WORD   RX01$          ;POINTER TO FUNCTION TABLE FOR THE RX01

                                .SBTTL  STARTING ADDRESS TABLE

173564  173670  ADDRS:  .WORD   TU18           ;STARTING ADDRESS FOR THE TM11/TU18
173566  173124          .WORD   TU56           ;STARTING ADDRESS FOR THE TC11/TU56
173570  173146          .WORD   RK05           ;STARTING ADDRESS FOR THE RK11/RK05
173572  173160          .WORD   RP03           ;STARTING ADDRESS FOR THE RP11/RP03
173574  173452          .WORD   FUTDEV         ;STARTING ADDRESS FOR A FUTURE DEVICE
173576  173230          .WORD   TU16           ;STARTING ADDRESS FOR THE RH70/TU16
173600  173316          .WORD   RP04           ;STARTING ADDRESS FOR THE RH70/RP04
173602  173342          .WORD   RS04           ;STARTING ADDRESS FOR THE RH70/RS04
173604  173362          .WORD   RX01           ;STARTING ADDRESS FOR THE RX11/RX01
```

```
                                  .SBTTL  CACHE MEMORY DIAGNOSTIC TESTS

                                  ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                  ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                  ;*
                                  ;*      THE FOLLOWING TWO TESTS ARE CACHE MEMORY TESTS, IF EITHER OF
                                  ;*      THEM FAILS TO RUN SUCCESSFULLY THEY WILL COME TO A HALT
                                  ;*      IN THE M9301 ROM.  IF YOU DESIRE TO TRY TO BOOT YOUR SYSTEM, OR
                                  ;*      DIAGNOSTIC ANYWAY, YOU CAN PRESS "CONTINUE" AND THE PROGRAM
                                  ;*      WILL FORCE MISSES IN BOTH GROUPS OF THE CACHE AND GO TO THE
                                  ;*      BOOT STRAP THAT HAS BEEN SELECTED.
                                  ;*
                                  ;^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^
                                  ;^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^^

              173606                      . = BASE2 + 606

                                  ;;*********************************************************************
                                          .SBTTL  TEST26  TEST CACHE DATA MEMORY
                                  ;*
                                  ;*      THIS TEST WILL CHECK THE DATA MEMORY IN THE CACHE, FIRST GROUP
                                  ;*      0 AND THEN GROUP 1.  IT LOADS 052525 INTO AN ADDRESS COMPLEMENTS
                                  ;*      IT TWICE AND THEN READS THE DATA, THEN IT CHECKS TO INSURE THAT
                                  ;*      THE DATA WAS A HIT.  THEN THE SEQUENCE IS REPEATED ON THE SAME
                                  ;*      ADDRESS WITH 125252 AS THE DATA.  ALL CACHE MEMORY DATA LOCATIONS
                                  ;*      ARE TESTED IN THIS WAY.
                                  ;*      IF EITHER GROUP FAILS AND THE OPERATOR PRESSES CONTINUE THE
                                  ;*      PROGRAM WILL TRY TO BOOT WITH THE CACHE DISABLED.
                                  ;*
                                  ;*      THE REGISTERS ARE INITIALIZED AS FOLLOWS FOR THIS TEST:
                                  ;*      R0 = 1000 (ADDRESS) R1 = 2 (COUNT), R2 = 1000 (COUNT)
                                  ;*      R3 = 1000 (COUNT), R4 = 125252 (PATTERN) R5 = 177746 (CONTROL REG)
                                  ;*      SP = 172374 (FLAG OF ZERO PUSHED ON STACK)
                                  ;*
                                  ;;*********************************************************************
       173606                     TST26:
       173606  012704  125252             MOV     #125252,R4      ;SET UP R4 FOR THIS TEST
       173612  012715  000030             MOV     #GRPE,(R5)      ;FORCE REPLACE GROUP 0 AND FORCE MISS GROUP 1
       173616  010302             1$:     MOV     R3,R2           ;SET COUNT TO CONTENTS OF R3
       173620  010200                     MOV     R2,R0           ;SET STARTING ADDRESS INTO R0
       173622  012701  000002     2$:     MOV     #2,R1           ;USE 2 PATTERNS IN DATA MEMORY
       173626  005104             3$:     COM     R4              ;COMPLEMENT DATA IN R4
       173630  010410                     MOV     R4,(R0)         ;WRITE THE TEST PATTERN
       173632  005110                     COM     (R0)            ;DOUBLE COMPLEMENT DATA AND
       173634  005110                     COM     (R0)            ;MAKE SURE DATA IS IN THE CACHE
       173636  021004                     CMP     (R0),R4         ;COMPARE DATA & SET BIT 0 IN HIT/MISS REG.
       173640  001401                     BEQ     5$              ;BRANCH IF DATA MATCHES
       173642  000000                     HALT                    ;DATA DIDN'T MATCH R0 = ADDRESS
       173644  036037  177752     5$:     BIT     @#177752        ;WAS THE LAST MEMORY REFERENCE A HIT?
       173650  103402                     BCS     4$              ;BRANCH IF YES
       173652  000000                     HALT                    ;CACHE FAILED TO HIT R0 = ADDRESS
       173654  000444                     BR      BOOTMISS        ;ABORT REST OF TEST IF "CONTINUE" PRESSED
       173656  077115             4$:     SOB     R1,3$           ;GO BACK ONE TIME TO TRY COMPLEMENT DATA
```

```
1002  173660  005720                  TST     (R0)+           ;MOVE TO NEXT ADDRESS
1003  173662  077221                  SOB     R2,2$           ;BRANCH IF NOT DONE
1004  173664  012715  030044          MOV     #GRP1,(R5)      ;FORCE REPLACE GROUP 1 AND FORCE MISS GROUP 0
1005  173670  005116                  COM     (SP)            ;COMPLEMENT THE CYCLE FLAG
1006  173672  001351                  BNE     1$              ;LOOP IF NOT DONE
1007
1008                          ;!*****************************************************************
1009                                  .SBTTL  TEST2/  TEST VIRTUAL 28K WITH CACHE ON
1010                          ;*
1011                          ;*      THIS TEST CHECKS VIRTUAL MEMORY FROM 001000 THRU 157776
1012                          ;*      TO INSURE THAT YOU CAN GET HITS ALL THE WAY UP THROUGH MAIN
1013                          ;*      MEMORY.  IT STARTS WITH GROUP 1 ENABLED, THEN TESTS GROUP 0, AND
1014                          ;*      FINALLY CHECKS MEMORY WITH BOTH GROUPS ENABLED.  IF ANY OF
1015                          ;*      THE THREE PASSES FAIL THE TEST WILL HALT AT "CONT + 2".  THEN
1016                          ;*      IF THE OPERATOR PRESSES "CONTINUE", THE PROGRAM WILL TRY TO
1017                          ;*      BOOT WITH THE CACHE DISABLED.
1018                          ;*
1019                          ;*      UPON ENTRY THE REGISTERS WILL BE SET UP AS FOLLOWS:
1020                          ;*      R0 = 001000 (ADDRESS), R1 = 3 (PASS COUNT), R2 = 67400 (MEMORY COUNTER),
1021                          ;*      R3 = 1000 (FIRST ADDRESS), R4 = 67400 (MEMORY COUNTER),
1022                          ;*      R5 = 177746 (CONTROL REG.), SP = 172374 (POINTING TO CODE FOR CONTROL REG)
1023                          ;*
1024                          ;*      UPON COMPLETION OF THIS TEST MAIN MEMORY FROM VIRTUAL ADDRESS
1025                          ;*      001000 THRU 157776 WILL CONTAIN ITS OWN VIRTUAL ADDRESS.
1026                          ;*
1027                          ;!*****************************************************************
1028  173674                  TST27:
1029  173674  012702  067400          MOV     #67400,R2       ;COUNT STORAGE (28K - 1000 BYTES)
1030  173700  010300                  MOV     R3,R0           ;FIRST ADDRESS IS 1000 OCTAL
1031  173702  010204                  MOV     R2,R4           ;SETUP COUNTER
1032  173704  010020          1$:     MOV     R0,(R0)+        ;FILL MEMORY WITH ADDRESSES
1033  173706  077402                  SOB     R4,1$           ;LOOP UNTIL DONE
1034  173710  012716  000030          MOV     #GRP0,(SP)      ;LOAD CODE TO FORCE GROUP 0 ONTO STACK
1035  173714  012701  000003          MOV     #3,R1           ;SET PASS COUNT TO THREE
1036  173720  010300          2$:     MOV     R3,R0           ;FIRST ADDRESS
1037  173722  010204                  MOV     R2,R4           ;COUNTER
1038  173724  005110          3$:     COM     (R0)            ;DOUBLE COMPLEMENT DATA AND
1039  173726  005110                  COM     (R0)            ;MAKE SURE IT IS IN THE CACHE,
1040  173730  020020                  CMP     R0,(R0)+        ;COMPARE DATA, AND SET BIT 0 IN HIT/MISS REG
1041                                                          ;ALSO POINT TO NEXT ADDRESS
1042  173732  001401                  BEQ     5$              ;BRANCH IF DATA MATCHES
1043  173734  000000                  HALT                    ;DATA DIDN'T MATCH R0 = ADDRESS + 2
1044  173736  006037  177752  5$:     ROR     @#177752        ;WAS THE LAST MEMORY REFERENCE A HIT?
1045  173742  103402                  BCS     4$              ;BRANCH IF YES
1046  173744  000000                  HALT                    ;HIT FAILED TO OCCUR R0 = ADDRESS + 2
1047  173746  000407                  BR      BOOTMISS        ;ABORT REST OF TEST IF "CONTINUE" PRESSED
1048  173750  077413          4$:     SOB     R4,3$           ;LOOP UNTIL DONE
1049  173752  011615                  MOV     (SP),(R5)       ;FORCE MISS GRP1 ON PASS 2, FULLY
1050                                                          ;ENABLE CACHE ON PASS THREE,
1051  173754  005016                  CLR     (SP)            ;GET READY TO FULLY ENABLE CACHE ON PASS 3
1052  173756  077120                  SOB     R1,2$           ;RUN THREE PASSES THRU THIS TEST
1053  173760  000404                  BR      JUMP            ;GO TO BOOT STRAP CODE
1054
1055
```

C3

```
.056  173762  000000                  CONT:   HALT                    ;STOP HERE IF THERE IS A CACHE ERROR
.057  173764  022626                          CMP     (SP)+,(SP)+     ;ADJUST STACK POINTER AFTER ABORT
.058  173766                          BOOTMISS:
.059  173766  012715  000014                  MOV     #MISS,(R5)      ;FORCE MISSES IN BOTH GROUPS OF CACHE
.060  173772  005726                  JUMP:   TST     (SP)+           ;POINT TO UPPER SIX BITS OF BUS ADDRESS
                                                                      ;THAT DATA IS IN ADDRESS 1772376 (KUPAR7)
.062  173774  000137  173000                  JMP     @#BOOT          ;GO TO BOOT STRAP ENTRY POINT
.063
.064
.065          000001                  .END
```

```
ADDRS   173564          733     938#
AGAIN   173478          750     762     789     791     861     883#
BASE1 = 165000#           1#    116
BASE2 = 173000#           1#    784     964
BOOT    173000          785#   1002
BOOTMI  173766         1000    1047    1058#
CMDPTR  173542          732     920#
CMNSGO  173162          791     764     772     782#    842
CMNSRH  173358#         819     829     841#
CONT    173762          674    1056#
CSRPTR  173520          731     914#
DISPLA= 177570#           1#
FCE   = 001000#           1#    798
FUTDEV  173452         8748    942
FUTDES  173515         9008    938
GRP0  = 000030            1#    986    1034
GRP1  = 000044            1#   1004
INDMAP  165120#         250#    251
JUMP    173772         1053    1060#
KDPAR0= 172360#           1#
KDPAR7= 172376            1#    557
KIPAR0= 172340            1#    495     686
KIPAR7= 172356            1#
KIPDR0= 172300#           1#
KIPDR7= 172316            1#    551
MAPLP = 170200#           1#    250     271*    292     618
MISS  = 000014            1#    691    1059
MMR0  = 177572            1#    620*
MMR3  = 172516            1#    625*
MOL   = 010000#           1#    806
\     = 000003          1178    118     119     124     129#    138     151     136     146#    147     148     158     168#
                         169     178     188     189#    198     191     208     209#    218     211     228     227#    228
                         229     248     256#    257     258     269     276#    277     278     289     300#    301     302
                         313     323#    324     325     335     342#    343     344     355     367#    368     369     388
                         393#    394     395     485     420#    421     422     434     451#    492     493     403     479#
                         483     481     493     516#    517     518     520     544#    545     546     554     575#    576
                         577     594     629#    638     631     642     706#    707     708     783     1000#   1007    1018
                        1027
PAEHLT  169776          648     679#
PC    =%000007          249*    558*    564*    719     794*    868*
RK05    173140          770#    948
RK05S   173504          894#    928
RP03    173160#         778#    941
RP03S   173504          895#    929
RP04    173320          825#    944
RP04S   173511          982#    932
RS04    173340          835#    945
RS04S   173512          983#    933
RX01    173360#         848#    946
RX01S   173513          985#    934
R0    =%000000          243*    244     357*    368     487*    418*    413*    414     436*    439*    448*    440     495*
                        498*    499     501*    502     504     506*    507     509     531*    534*    535     606*    608*
                        611*    618*    628*    621*    655*    656*    668*    661     662     665*    667     670     710*
                        719*    723*    724     728*    729     803     825     838     848*    908*    991*    992*    993*
```

```
                        994    1002   1030*  1332*  1036*  1038*  1039*  1040
R1      =%000001        244*    245    251*   295*   337*   368*   361*   382*   383    386    389*   411*   412*
                        410     437*   441*   442*   446*   465*   467    471*   473*   475*   496*   511*   532*
                        540*    607*   610*   619*   623*   661*   662    667*   669*   670    709    731*   739*
                        741*    743    745*   746*   747    749    757*   758*   759    761    763*   771*   778*
                        782*    783*   784    786    790    792*   805*   806    808*   809    811*   812    814*
                        815*    816    818*   825*   826*   827*   828*   835*   836*   841*   851    853*   855
                        857*    859    862*   863    865    989*   1001*  1035*  1052*
R2      =%000002        245*    246    438*   443*   533*   534    535    596*   598*   599*   608*   608    609*
                        616*    621    644    652*   654    659    673*   729*   738*   739    757    763    778*
                        771     776    803*   804*   805    854*   858*   869*   866    987*   988    1003*  1029*
                        1031    1037
R3      =%000003        246*    247    292*   293*   294*   295    316*   317*   318*   617*   620    622*   653*
                        655     660    732*   741    746    758    783    808    811    819    826    858*   853
                        987     1038   1036
R4      =%000004        247*    248    315*   316    383    498    499    504    654*   658*   659*   800*   724*
                        725*    726*   727    731    732    733    788    989*   998*   991    994    1031*  1033*
                        1037*   1048*
R5      =%000005        248*    249    317    386    388*   389    497*   502    507    509    658*   691*   986*
                        1004*   1049*  1059*
SP      =%000006        139*    168*   182*   242*   243    557*   508    563*   566*   567*   644*   677*   818
                        828     836    1005*  1034*  1049   1051*  1057   1060
START   173014          785     7108
SWR     = 177572          18    996     716
TST1    165000          1258
TST10   165134          253     2708
TST11   165146          273     2908
TST12   165166          297     3148
TST13   165204          328     3368
TST14   165214          339     3568
TST15   165236          364     3818
TST16   165268          398     4208
TST17   165312          417     4358
TST2    165004          126     1378
TST20   165346          448     4648
TST21   165374          476     4948
TST22   165458          512     5388
TST23   165476          5558
TST24   165558          5958    884
TST25   165662          681     6438
TST26   173606          678     9848
TST27   173674          1028#
TST3    165020          143     1598
TST4    165036          165     1818
TST5    165052          186     2018
TST6    165066          206     2218
TST7    165076          224     2418
TUR     = 000001          1#    709
TU10    173076          739#    938
TU105   173476          889#    926
TU132   173074          711     7418
TU16    173238          883#    943
TU165   173586          897#    951
TU56    173124          757#    939
```

```
TU56S   173582          8#38    927
WAIT    173082          7898    918     748
STN     = 000038          18    117     1268    129     1388    143     146     1688    165     168     1828    186     189
                        2028    206     289     2228    224     227     2428    253     256     2718    273     276     2918
                        297     308     3158    328     323     3378    339     342     3578    364     367     3828    398
                        393     4078    417     428     4368    448     491     4698    476     479     4958    912     916
                        5318    944     5568    975     5968    681     629     6448    966     9858    1888    10298
.       = 174888        1168    7848    9648
```

```
ADC     382  440  442
ADD     292  295  317  361  446  689  622
ASH     465  473  599  616  726  770
ASL     441
ASR     439  723
BCC     272
BCS     296  998 1045
BEQ     162  293  390  417  476  536  561  681  683  6/1  718  887  849  892  868
        995 1042
BGE     163  320  303
BGT     164  224  302  387  448
BHI     142  185  283
BHIS    184
BIC     300  680  725  728  848
BIS     316  741  758  884
BIT     386  789  886  859
BIPB    851
BLE     165  223  297  304  447
BLO     319
BLOS    143  286  338  358
BLT     285  252  273  339
BMI     140  469  750  861
BNE     186  384  415  588  583  585  588  918  597  717  789  791 1886
BPL     161  488  744  748  760  762  785  787  818  813  817  896  804  867
BR      126  912  785  711  748  751  764  772  819  829  842 1888 1847 1893
BVC     183
BVS     141
CLR     139  411  586  617  649  677  792  794  808 1851
CLZ     222
CMP     383  499  535  508  662  678  788  798  994 1848 1857
CMPB    582  584  587  589
COM     294  357  388  497  665  669  998  992  993 1885 1838 1839
COMB    581  586
DEC     160  337
HALT    127  144  166  187  287  225  254  274  298  321  348  359  385  391  489
        418  449  470  477  513  537  559  582  585  589  571  664  672  679  874
        996  999 1043 1046 1056
INC     293  318  412  437  475  626  858
JMP     570  678  733  884 1862
JSR     558
MOV     242  243  244  245  246  247  248  249  436  438  495  498  498  931  932
        533  534  557  563  567  596  598  686  687  688  611  618  619  628  621
        625  644  648  658  651  652  653  654  655  656  659  668  661  667  674
        719  724  729  731  732  739  745  757  703  771  778  782  883  885  814
        818  827  828  836  841  854  985  986  987  988  989  991 1884 1829 1838
       1831 1832 1834 1835 1836 1837 1849 1859
MOVB    487  716  746  783  888  811  815  825  826  839  853  857  862  865
RESET   883
ROL     271
ROR     182  315  997 1844
RTI     568
RTS     564
SEN     284
SEZ     282
```

```
$DB      410   413   443   911   948   618   623   658   666   673   858  1881  1883  1833  1848
        1852
$UB      251   389
$WAB     471   738
TST      414   416   727   749   759   761   786  1882  1883
TSTB     467   743   747   784   889   812   816   855   863   866
.BYTE    898   891   895   897   898   899   988   982   983   989   986   988
.DSABL     1
.ENABL     1
.END    1865
.ENDC    118   125   127   138   137   144   147   159   166   169   181   187   198   281   287
         218   221   225   228   241   254   257   278   274   277   298   298   381   314   321
         324   336   348   343   356   365   368   381   391   394   486   418   421   435   449
         452   464   477   488   494   513   517   538   545   555   576   595   682   638   643
         967   984  1889  1828
.EQUIV     1
.IF      117   124   126   129   136   143   146   158   165   168   183   186   189   288   284
         289   228   224   227   248   253   256   269   273   276   289   297   388   313   328
         323   335   339   342   355   364   367   388   398   393   485   417   428   434   448
         451   463   476   479   493   512   516   529   544   554   575   594   681   629   642
         966   983  1888  1827
.IFF     117   124   126   129   136   143   146   158   165   168   188   186   189   288   284
         289   228   224   227   248   253   256   269   273   276   289   297   388   313   328
         323   335   339   342   355   364   367   388   398   393   485   417   428   434   448
         451   463   476   479   493   512   516   529   544   554   575   594   681   629   642
         966   983  1888  1827
.IIF     117   118   119   124   129   138   131   136   146   147   148   158   168   169   178
         188   189   198   191   288   289   218   211   228   227   228   229   248   256   257
         258   269   276   277   278   289   388   381   382   313   323   324   325   335   342
         343   344   355   367   368   369   388   393   394   395   485   428   421   422   434
         451   452   453   463   479   488   481   493   516   517   518   529   544   545   546
         554   575   576   577   594   629   638   631   642   966   967   968   983  1888  1889
        1818  1827
.LIST      1    77    96   188   112   117   126   129   138   148   168   166   182   189   282
         289   222   227   242   256   271   276   291   388   315   323   337   342   397   367
         382   393   487   428   436   451   465   478   495   516   531   544   556   575   596
         629   644   683   788   951   961   966   985  1888  1829
.MACRO     1   117   129   146   168   189   289   227   256   276   388   323   342   367   393
         428   451   479   516   544   575   628   966  1888
.NLIST     1    77    96   188   112   117   126   129   138   148   168   168   182   189   282
         289   222   227   242   256   271   276   291   388   315   323   337   342   397   367
         382   393   487   428   436   451   465   479   495   516   531   544   556   575   596
         629   644   683   788   951   961   966   985  1888  1829
.PAGE      1    21    75   681   886   911   948
.REPT     77    96   188   112   683   788   875   951   961
.SBTTL   118   138   147   169   198   218   228   297   277   381   324   343   368   394   421
         452   488   517   545   576   638   682   787   714   738   754   767   775   788   888
         822   832   839   845   872   887   912   924   936   949   967  1889
.TITLE    13
.WORD    258   722   796   797   875   876   877   878   879   888   889   893   989   914   915
         916   917   918   919   928   921   922   926   927   928   929   938   931   932   933
         934   938   939   948   941   942   943   944   945   946
```

ERRORS DETECTED: 0

*DEKBHA,DEKBHA.LIS/SOL/CRF=DEKBHA.P11
RUN-TIME: 10 15 2 SECONDS
CORE USED: 9K

K