

KW11-W

LOGIC TEST
MD-11-DZKWC-C

EP DZKWC-C DL
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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-JZKWC-C-D
PRODUCT NAME: KW11W LOGIC TEST
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MAINTAINER: IPG CUSTOM SYSTEMS
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MEMORY STORAGE - 00000 - 012000 OCTAL

LOADING PROCEDURE - (PAPER TAPE SUPPLIED) LOADED USING NORMAL
BINARY PROCEDURE.

STARTING PROCEDURE:

STARTING ADDRESS 2001

FOR NON-STANDARD VECTORS, DEVICE ADDRESSES & PRIORITY INTERRUPT
LEVELS, THE PROGRAM WILL ASK THE FOLLOWING QUESTIONS TO WHICH
THE OPERATOR MUST RESPOND:

FIRST DEVICE ADDRESS - (6 CHARACTERS)
FIRST INT. VECTOR - (3 CHARACTERS)
PRIORITY INT. LEVEL - (INPUT INT. LEVEL OF DEVICE 4-7)
PDP-11 (A)=05,10,20 (B)=35,40 (C)=45,50

IF AN ERROR IS ENCOUNTERED WHILE INPUTTING THE DEVICE ADDRESS
OR INT. VECTOR, THE OPERATOR MAY TYPE A RUB OUT AND REPEAT
ENTIRE LINE INPUTTING. WHEN LINE IS COMPLETE OR IF NO CHANGES
(FROM STANDARD DEVICE) THE OPERATOR MUST TERMINATE THE LINE
WITH A CARRIAGE RETURN.

STARTING ADDRESS 10001

DIRECT STARTING OR RESTARTING OF LOGIC TEST.

STARTING ADDRESS 2201

DIRECT STARTING OR RESTARTING OF DELAY ADJUSTMENT TEST.

STARTING ADDRESS 2401

DIRECT STARTING OR RESTARTING OF DYNAMIC SYSTEM TEST.

LOGIC TEST OPERATING PROCEDURE AND DESCRIPTION

THE LOGIC TEST CONSISTS OF 44 SUB TESTS EACH CONTAINING AN ERROR ROUTINE. LOGIC TEST SHOULD BE STARTED WITH ALL CONSOLE (PDP-11) SWITCHES DOWN. IF AN ERROR IS ENCOUNTERED, THE TELETYPE WILL REPORT WITH FAILING TEST AND HALT, TO LOOP ON A FAILURE CONSOLE SWITCH REGISTER, BIT 14 IS RAISED AND THE TEST IS LOOPEO BY DEPRESSING THE CONTINUE KEY, TO INHIBIT THE ERROR TYPING RAISE SWITCH REGISTER BIT 13.

LOGIC TEST REQUIREMENTS:

TO RUN THE LOGIC TEST, THE SUPPLIED TEST PLUG MUST BE CONNECTED TO THE MODULE CONNECTOR, THE T3 DELAY MUST EXCEED T2 BY 50 MICRO-SECONDS, THE ADJUSTMENT OF T1 MUST BE SET AT A MINIMUM.

LOGIC TEST ERROR REPORTS.

TEST	FAILURE
----	-----
T1	STATUS AND CONTROL REG, NOT CLEAR UPON INITIALIZE,
T2	INT, ENABLE BIT 6 OF CSR NOT SET,
T3	INT, ENABLE BIT 6 OF CSR NOT CLEAR,
T4	AN ILLEGAL INT, IS PRESENT FROM THE MODULE,
T5	AN ILLEGAL INT, IS PRESENT AFTER A DELAY TIME OUT,
T6	STATUS REGISTER NOT CLEAR AFTER DELAY TIME OUT,
T7	STATUS REGISTER WAS AFFECTED BY A CLEAR FLAGS INSTRUCTION,
T8	FAILED TO MONITOR A T2 FLAG,
T9	ALARM RECEIVED BIT 14 OF CSR SET WITHOUT AN EXT, ENALBE,
T10	ALARM RECIEVE FLAG FAILED TO SET AFTER ENABLING THE EXTER NAL WORLD,
T11	T2 FLAG FAILED TO CLEAR,
T12	RECIEVE FLAG FAILED TO CLEAR,
T13	SHORT LOOP (T1) FAILED TO CLEAR,
T14	T2 FLAG SET SHOULD HAVE BEEN TEMINATED BY THE LOCK FLOP UPON THE SHORT LOOP GENERATED IN T13,
T15	RECEIVE FLAG WAS SET UPON A SHORT LOOP WITHOUT THE EXTERNAL ENABLE,
T16	LOCK FLOP FAILED TO CLEAR JPON ENABLING THE EXTERNAL WORLD AND WAITING 5M,SEC, FOR CLEAR ERROR,
T17	NO ERROR CHECKING, CONDITIONING FOR T18, T19, AND T20,
T18	T1 FLAG FAILED TO CLEAR,
T19	T2 FLAG FAILED TO CLEAR,
T20	RECEIVE FLAG FAILED TO CLEAR,
T21	RECEIVE FLAG FAILED TO SET UPON A TIME OUT OF T3,
T22	ALARM REC, FLAG FAILED TO CLEAR,
T23	ENABLE FLOP NOT CLEARED AN ALARM OUT,
T24	A T2 FLAG FAILED TO RAISE AN INT, AT VECTOR 350,
T25	SHORT LOOP FLAG FAILED TO RAISE AN INT, AT VECTOR 350,

T26 ALARM REC, FLAG FAILED TO RAISE AN INT, AT VECTOR 358,
 T27 SHORT LOOP "LOCK" FAILED TO TERMINATE T3,
 T28 SHORT LOOP "LOCK" FAILED TO TERMINATE T2,
 T29 THE CLEARING OF "LOCK" DIDNOT RELEASE T2 TO THE
 BUS (REFER TO T26,T27, &T28),
 T30 SHORT LOOP " LOCK"FAILED TO LOCK PULSING OF TIMER,
 T31 INITIALIZE FAILED TO CLEAR SHORT LOOP FLAG,
 T32 INITIALIZE FAILED TO CLEAR RECEIVE FLAG,
 T33 INITIALIZE FAILED TO CLEAR THE LOCK FLOP,
 T34 INITIALIZE FAILED TO TERMINATE T3,
 T35 INITIALIZE FAILED TO TERMINATE T2,
 T36 INCORRECT STATUS IN EXTERNAL STATUS REG,
 T37 STATUS OF ECSR CHANGED UPON A RESET INSTRUCTION,
 T38 SWITCH BUS INSTRUCTION FAILED TO CHANGE THE EXTERNAL
 STATUS REGISTER,
 T39 THE LATCH FAILED TO PREVENT A 2ND BUS SWITCHING
 (REFER TO T38),
 T40 BUS FAILED TO SWITCH TO 2ND LATCH,
 T41 TERMINATION OF T3 FAILED TO RELEASE THE LATCH,
 T42 A SWITCH BUS COMMAND FAILED TO CHANGE THE BUS STATUS,
 T43 A RESET INSTRUCTION FAILED TO CLEAR THE LATCH,
 T44 MANUAL ENABLE INPUT FAILED,
,
 T38S TEST FOLLOWED BY AN "S" DEVOTES SUBTEST,
 T40S WHICH IS A FAILURE OF THE EXTERNAL STATUS
 T41S REGISTER (STATUS READ IS INCORRECT),
 T43S

ALL TESTS MUST BE SUCCESSFULLY COMPLETED BEFORE THE NEXT TEST MAY
BE EXECUTED,

UPON SUCCESSFUL COMPLETION OF THE LOGIC TEST, THE TELETYPE WILL
PRINT "PASS".

FOR SCOPING ERRORS, SWITCH REGISTER BIT 7 MAY BE RAISED TO INCREASE
THE TEST REPEATABILITY RATE,

DELAY ADJUSTMENT TESTS,

THE OPERATOR MUST RESPOND TO THE QUESTION, "(1) WATCHDOG, (2) WARNING & SHORT LOOP" BY TYPING A 1 OR A 2 FOR DESIRED ADJUSTMENT LOOP TO BE RUN,

DYNAMIC SYSTEM TEST,

THIS TEST IS INTENDED AS AN EXERCISER WHICH SHOULD BE RUN ONLY AFTER COMPLETING THE LOGIC TEST,

THE TEST EXERCISES THE INTERRUPT LOGIC, EXTERNAL STATUS AND DELAYS,

THE TIMER IS PRIMED BY PULSING THE DELAYS AND ENABLING THE INTERRUPT, THE ONLY LEGAL INTERRUPTS ARE THOSE FROM THE T2 DELAY, AFTER EACH LEGAL INTERRUPT, THE EXTERNAL STATUS IS SWITCHED AND TESTED FOR A CORRECT STATUS READING,

A "PASS" IS PRINTED AFTER 100 SUCCESSFUL INTERRUPTS, POSSIBLE ERRORS REPORTED ARE:

1. SHORT LOOP FLAG SET
2. EXTERNAL STATUS BAD
3. ILLEGAL INTERRUPT

TO EXIT ANY TEST, RAISE CONSOLE SWITCH REGISTER, BIT 00, THE PROGRAM WILL THEN OUTPUT THE HEADER, MAKE SURE THAT THE SWITCH IS LOWERED BEFORE ENTERING A NEW TEST,

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.TITLE WATCH DOG TIMER
.ENABL A4A A3S

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;
;LOGIC TEST FOR WATCH DOG TIMER (HARDWARE MONITOR)
;FOR PDP-11 SYSTEMS,
;THE WATCH DOG TIMER MUST BE PULSED FROM THE
;COMPUTER PROGRAM WITHIN A SPECIFIED TIME TO
;INHIBIT THE TIMER FROM TIMING OUT. UPON A TIME
;OUT CONDITION THE WATCH DOG WILL POST AN
;INTERRUPT ALLOWING THE PROCESSOR A CHANCE TO
;RECOVER BEFORE A SECOND TIME OUT CONDITION
;OCCURS ISSUING AN "ALARM OUT" TO THE EXTERNAL
;WORLD. THE WARNING INTERRUPT IS SENSED AT
;BIT 07 OF THE CONTROL AND STATUS REGISTER.
;THE TIMER ALSO HAS A "SHORT LOOP" PROTECTION WHICH
;GUARDS AGAINST A PROGRAM FAILURE THAT MAYBE PULSING THE
;TIMER BEFORE A SPECIFIED INTERVAL. THE SHORT LOOP WILL
;POST AN INTERRUPT ALSO AT VECTOR (XXX) WHENEVER PULSED
;TWICE WITHIN A SPECIFIED TIME INTERVAL. THE SHORT LOOP
;INTERRUPT IS SENSED IN THE STATUS REGISTER BY BIT 14.
;THE RECEIVE CIRCUIT ALLOWS FOR AN INTERRUPT (VECTOR XXX) TO BE
;POSTED WHEN AN "ALARM SIGNAL" IS RECEIVED FROM THE
;EXTERNAL WORLD. THE RECEIVE INTERRUPT IS SENSED AT
;BIT 7 OF THE STATUS REGISTER.

;
;FOR TEST PURPOSES THE "ALARM OUT" SIGNAL IS
;JUMPED TO THE ALARM RECEIVE WITH A SUPPLIED
;TEST PATCH.

;
;
;DIGITAL EQUIPMENT CORP.
;INDUSTRIAL PRODUCTS GROUP
;WATCH DOG TIMER LOGIC TEST
;MAINDEC-11-DEKWC-C
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;MAINTAINER: IPGICUSTOM SYSTEMS
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177776
177562
177560
177566
177564
172400
172402
172404
172406
177570
104000
000240

PS=177776
TKB=177562
TKS=177560
TYDB=177566
TYSR=177564
CSR=172400
CINT=172402
ECSR=172404
SWBU=172406
SR=177570
NULL=104000
NOP=240

;TELETYPE READER BUFFER
;TELETYPE READER STATUS
;TELETYPE PRINTER BUFFER
;TELETYPE PRINTER STATUS
;CONTROL AND STATUS-WATCHDOG
;INTERRUPT CLR INSTRUCTION
;EXTERNAL CSR
;SWITCH BUS
;SWITCH REGISTER

61

55	000000	HLT=0	
56	000000	R0=X0	
57	000001	R1=X1	
58	000002	R2=X2	;SUBROUTINE RETAIN
59	000003	R3=X3	;TELETYPE ROUTINE RETAIN
60	000004	R4=X4	;TIME CONTROL ROUTINES
61	000005	R5=X5	;ERROR PRINT & SCOPE MODE
62	000006	SP=X6	
63	000007	PC=X7	
64		ILOAD TRAP CATCHER	

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66
67          000000
68
69          .=0
70          .REPT      100
71          .+2
72          HLT
73          .ENDR
74          ;TRAPPED TO PREVIOUS VECTOR
75
76          .=4
77          TOBE
78          340
79          ;TIME OUT BUSS ERROR
80          ;PROCESSOR STATUS
81
82          .=30
83          NULPRY
84          340
85
86          ;
87          ;
88          ;
89          ;
90          .=350
91          WAOG
92          340
93          ;WATCH DOG INTERRUPT
94          RECF
95          340
96          ;SET PROCESSOR STATUS BACK TO 7
97          ;RECEIVE FLAG VECTOR
98
99          ;
100         .=500
101         XCSR: CSR
102         XCINT: CINT
103         XECSR: ECSR
104         XSWBU: SWBU
105         PRIV: 300
106         ;PRIORITY LEVEL
107
108         .=600
109         STACK: 0
110         ;STACK LOCATOR
111         .=200
112         MOV      #STACK,SP
113         JSR      R5,AJDMO
114         JMP      HEADER
115         ;ASK FOR VECTORS AND ADDRESSES
116         ;PRINT HEADER AND TAKE COMMANDS
117
118         .=220
119         MOV      #STACK,SP
120         JMP      DELAY
121         ;DIRECT ENTRY TO DELAY TEST
122
123         .=240
124         MOV      #STACK,SP
125         JMP      DYMAN
126         ;DIRECT ENTRY TO DYMANIC TEST
127
128         .=1000
129         LOGIC: MOV      #STACK,SP
130         ;INITIALIZE STACK
131         NULL
132         RESET
133         NULL
134         JMP      TEST
135         ;
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124 001016 012737 010617 007324 TESTI MOV #LT,MES ;SET REGISTER 3 FOR OUTCODE
125 001024 004337 007210 JSR R3,PRINT ;PRINT "LOGIC TEST"
126
127
128
129
130
131 001030 004137 007402 T1i JSR R1,CHECK
132 001034 012737 000340 177776 MOV #340,PS
133 001042 012737 001030 010570 MOV #T1,LOOP
134 001050 032777 177777 177422 BIT #177777,@XCSR ;TEST ALL BITS OF STATUS REG
135 001056 001414 BEQ T2
136 001060 004537 010520 JSR R5,ERROR
137 001064 012737 010634 007324 MOV #EE1,MES
138 001072 004337 007210 JSR R3,PRINT
139 001076 004537 010536 JSR R5,SCOPE
140 001102 000000 HLT ;STATUS REG NOT CLEAR
141 001104 000137 001030 JMP T1
142
143
144
145
146 001110 004137 007402 T2i JSR R1,CHECK
147 001114 012737 001110 010570 MOV #T2,LOOP
148 001122 012777 000100 177350 MOV #100,@XCSR
149 001130 032777 000100 177342 BIT #100,@XCSR ;TEST THAT INT,EN, IS SET IN THE CSR
150 001136 001014 BNE T3
151 001140 004537 010520 JSR R5,ERROR
152 001144 012737 010640 007324 MOV #EE2,MES
153 001152 004337 007210 JSR R3,PRINT
154 001156 004537 010536 JSR R5,SCOPE
155 001162 000000 HLT ;INT, EN, BIT FAILED TO SET
156 001164 000137 001110 JMP T2
157
158
159
160 001170 004137 007402 T3i JSR R1,CHECK
161 001174 012737 001170 010570 MOV #T3,LOOP
162 001202 005077 177272 CLR @XCSR
163 001206 032777 000100 177264 BIT #100,@XCSR ;CHECK THAT INT ENABLE CLEARED
164 001214 001414 BEQ T4
165 001216 004537 010520 JSR R5,ERROR
166 001222 012737 010644 007324 MOV #EE3,MES
167 001230 004337 007210 JSR R3,PRINT
168 001234 004537 010536 JSR R5,SCOPE
169 001240 000000 HLT ;INT.ENABLE FAILED TO CLEAR
170 001242 000137 001170 JMP T3
171
172
173
    IEX
    IENABLE PROCESSOR INTERRUPT AND CHECK FOR ILLEGAL
    
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					; INTERRUPTS OF WATCH DOG TIMER	
174						
175						
176	001246	004137	007402		JSR	R1,CHECK
177	001252	012737	001246	010570	MOV	#T4,LOOP
178	001260	012704	001322		MOV	#AAA1,R4
179	001264	012709	001322		MOV	#AAA1,R5
180	001270	052777	000100	177202	BIS	#100,#XCSR
181	001276	013737	000510	177776	MOV	PRIV,PS
182	001304	000240			NOP	
183	001306	000240			NOP	
184	001310	012737	000340	177776	MOV	#340,PS
185	001316	000137	001352		JMP	T5
186	001322	004537	010520		JSR	R5,ERROR
187	001326	012737	010650	007304	MOV	#EE4,MES

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189
190 001334 004337 007210 JSR R3,PRINT ;PRINT ERROR 1
191 001340 004537 010536 JSR R5,SCOPE ;CHECK FOR SCOPE LOOP
192 001344 000000 HLT ;STAY HERE
193 001346 000137 001246 JMP T4 ;RUN TEST OVER ON KEY "COUNT"
194
195
196 ;WAIT FOR POSSIBLE TIME OUT OF DELAYS AND CHECK AGAIN
197 ;FOR ILLEGAL WATCHDOG INTERRUPTS
198
199 001352 004137 007402 JSR R1,CHECK T5i
200 001356 012737 000340 177776 MOV #340,PS ;SET PROCESSOR STATUS TO 7
201 001364 004237 010350 JSR R2,TOUT ;WAIT FOR TIME OUTS
202 001370 012704 001432 MOV #AA2,R4 ;SET INT RETURN
203 001374 012705 001432 MOV #AA2,R5
204 001400 013737 000510 177776 MOV PRIV,PS ;P.S. TO PRIV
205 001406 000240 NOP ;WAIT FOR INT
206 001410 000240 NOP
207 001412 012737 000340 177776 MOV #340,PS ;SET STATUS TO 7
208 001420 042777 000100 177052 BIC #100,0XC5R
209 001426 000137 001462 JMP T6 ;GO ON
210 001432 004537 010520 AA2i JSR R5,ERROR ;CHECK FOR ERROR PRINT
211 001436 012737 010654 007304 MOV #EE5,MES ;PRINT ERROR MESSAGE
212 001444 004337 007210 JSR R3,PRINT ;PRINT ERROR 1A
213 001450 004537 010536 JSR R5,SCOPE
214 001454 000000 HLT ;ILLEGAL INT AFTER TIME OUT
215 001456 000137 001352 JMP T5
216
217
218 ;READ THE STATUS WORD TO CHECK THAT ALL BITS ARE
219 ;CLEAR AT THIS TIME.
220
221 001462 004137 007402 JSR R1,CHECK T6i
222 001466 012737 001462 010570 MOV #T6,LOOP ;SET FOR SCOPE LOOP RUN
223 001474 032777 177777 176776 BIT #177777,0XC5R ;CHECK STATUS REGISTER
224 001502 001414 BEQ T7 ;IF 0 GO TO TEST 7
225 001504 004537 010520 JSR R5,ERROR
226 001510 012737 010660 007304 MOV #EE6,MES
227 001516 004337 007210 JSR R3,PRINT ;PRINT ERROR2
228 001522 004537 010536 JSR R5,SCOPE ;CHECK FOR SCOPE LOOP
229 001526 000000 HLT ;STAY HERE
230 001530 000137 001462 JMP T6 ;RECYCLE
231
232
233 ;GENERATE A CLEAR COMMAND AND CHECK
234 ;THAT STATUS WAS UNAFFECTED
235
236 001534 004137 007402 JSR R1,CHECK T7i
237 001540 012737 001534 010570 MOV #T7,LOOP ;SET UP FOR SCOPE LOOP RUN
238 001546 005777 176730 TST 0XC1V ;CLR TO FLAGS SHORT LOOP,SECOND CHANCE
239 001552 004237 010350 JSR R2,TOUT
240 001556 032777 177777 176714 BIT #177777,0XC5R
241 001564 001414 BEQ T8 ;ALL CLEAR GO TO TEST 8
242 001566 004537 010520 JSR R5,ERROR

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243 001572 012737 010664 007304      MOV      #EE7,MES      ;PRINT ERROR 3
244 001600 004337 007210                JSR      R3,PRINT
245 001604 004537 010536                JSR      R5,SCOPE      ;CHECK FOR SCOPE LOOP
246 001610 000000                HLT
247 001612 000137 001534                JMP      T7            ;RECYCLE TEST?
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254 001616 004137 007402                JSR      R1,CHECK      ;PULSE TIMER AND CHECK FOR SECOND CHANCE (T2) TO TIME
255 001622 012737 001616 013570      T0i      MOV      #T0,LOOP      ;OUT
256 001630 012737 000340 177776      MOV      #340,PS
257 001636 012777 000001 176634      MOV      #1,@XCSR      ;PULSE TIMER
258 001644 004237 010350                JSR      R2,TOUT
259 001650 105777 176624                TSTB    @XCSR          ;TEST THAT T2 TIMED OUT
260 001654 100414                BMI     T9
261 001656 004537 010520                JSR      R5,ERROR
262 001662 012737 010670 007304      MOV      #EE8,MES
263 001670 004337 007210                JSR      R3,PRINT
264 001674 004537 010536                JSR      R5,SCOPE
265 001700 000000                HLT
266 001702 000137 001616                JMP      T8            ;T2 FAILED TO TIME OUT
267
268
269
270
271 001706 004137 007402                JSR      R1,CHECK      ;CHECK THAT ALARM RECEIVE (BIT 14) IS NOT SET
272 001712 032777 040000 176560      T9i      BIT     #040000,@XCSR  ;ENABLE FLOP=0
273 001720 001414                BEQ     T10
274 001722 004537 010520                JSR      R5,ERROR
275 001726 012737 010674 007304      MOV      #EE9,MES
276 001734 004337 007210                JSR      R3,PRINT
277 001740 004537 010536                JSR      R5,SCOPE
278 001744 000000                HLT
279 001746 000137 001706                JMP      T9            ;REC.SET WITHOUT ENABLE
280
281
282
283
284
285
286
287 001752 004137 007402                JSR      R1,CHECK      ;ENABLE ALARM OUT AND CHECK THAT ALARM RECEIVE
288 001756 012737 001616 013570      T10i     MOV      #T0,LOOP      ;WILL SET
289 001764 012777 000002 176506      MOV      #2,@XCSR
290 001772 004237 007342                JSR      R2,WAITX
291 001776 032777 040000 176474      BIT     #040000,@XCSR  ;TEST BIT 14
292 002004 001014                BNE     T11
293 002006 004537 010520                JSR      R5,ERROR
294 002012 012737 010700 007304      MOV      #EE10,MES
295 002020 004337 007210                JSR      R3,PRINT
296 002024 004537 010536                JSR      R5,SCOPE

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M1

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297 002030 000000          HLT
298 002032 000137 001616  JMP      T8          ;RECEIVE FLAG FAILED TO
299                               |          ;SET,CHECK THAT T3 TIMED OUT
300                               |
301                               |
302                               |
303 002036 004137 007402          JSR      R1,CHECK
304 002042 012737 002036 010570 T11:    MOV      @T11,LOOP
305 002050 005777 176420          TST      @XCINT
306 002054 105777 176420          TSTB    @XCSR
307 002060 100014          BPL     T12
308 002062 004537 010520          JSR      R5,ERROR
309 002066 012737 010705 007304  MOV      @EE11,MES
310 002074 004337 007210          JSR      R3,PRINT
311 002100 004537 010536          JSR      R5,SCOPE
312 002104 000000          HLT
313 002106 000137 002036  JMP      T11          ;T2 NOT CLEARED BY CINT(164002)
314                               |
315                               |
316                               |
317 002112 004137 007402          JSR      R1,CHECK
318 002116 012737 002036 010570 T12:    MOV      @T11,LOOP
319 002124 012777 000400 176346  MOV      @000400,@XCSR          ;CLEAR RECIEVE FLAG
320 002132 032777 040000 176340  BIT      @040000,@XCSR          ;TEST RECIEVE FLAG
321 002140 001414          BEQ     T13
322 002142 004537 010520          JSR      R5,ERROR
323 002146 012737 010712 007304  MOV      @EE12,MES
324 002154 004337 007210          JSR      R3,PRINT
325 002160 004537 010536          JSR      R5,SCOPE
326 002164 000000          HLT
327 002166 000137 002112  JMP      T12          ;RECEIVE FLG FAILED TO CLR
328                               |
329                               |
330                               |
331                               |
332 002172 004137 007402          JSR      R1,CHECK
333 002176 012737 000340 177776 T13:    MOV      @340,PS          ;SET STATUS TO SEVEN
334 002204 012737 002474 010570  MOV      @TMM,LOOP          ;SET FOR SCOPE LOOP
335 002212 005277 176262          INC      @XCSR          ;HIT TIMER TWICE
336 002216 005277 176256          INC      @XCSR
337 002222 005777 176252          TST      @XCSR          ;BIT 15 SHOULD BE SET
    
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339
340 002226 100004      BPL      ,012
341 002230 004237 010350  JSR      R2,TOUT      ;GO WAIT FOR TIMEOUT BEFORE PROCEEDING
342 002234 000137 002270  JMP      T14
343 002240 004537 010520  JSR      R5,ERROR     ;CHECK FOR ERROR PRINT
344 002244 012737 010717 007324  MOV      @EE13,MES    ;PRINT ERROR 13
345 002252 004337 007210  JSR      R3,PRINT
346 002256 004537 010536  JSR      R5,SCOPE
347 002262 000000      HLT
348 002264 000137 002474  JMP      THW          ;SHORT LOOP FLAG FAILED TO SET
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351
352
353
354 002270 004137 007402      T14:  JSR      R1,CHECK
355 002274 105777 176200  TSTB    @XCSR        ;TEST BIT 7
356 002300 100014      BPL      T15          ;CONTINUE TO TEST
357 002302 004537 010520  JSR      R5,ERROR
358 002306 012737 010724 007324  MOV      @EE14,MES
359 002314 004337 007210  JSR      R3,PRINT
360 002320 004537 010536  JSR      R5,SCOPE
361 002324 000000      HLT
362 002326 000137 002474  JMP      THW          ;T2 (2ND CHANCE) FLAG SET,CHECK LOCK FLOP
363
364
365
366
367
368
369 002332 004137 007402      T15:  JSR      R1,CHECK
370 002336 012737 000340 177776  MOV      @340,PS
371 002344 004237 007342  JSR      R2,WAITX     ;WAIT FOR POSSIBLE TIME OUT OF T4
372 002350 032777 040000 176122  BIT     @040000,@XCSR ;TEST THAT REC.DIDNT SET
373 002356 001414      BEQ     T16
374 002360 004537 010520  JSR      R5,ERROR
375 002364 012737 010731 007324  MOV      @EE15,MES
376 002372 004337 007210  JSR      R3,PRINT
377 002376 004537 010536  JSR      R5,SCOPE
378 002402 000000      HLT
379 002404 000137 002474  JMP      THW          ;REC. FLAG SET WITHOUT AN ENABLE
380
381
382
383
384
385
386 002410 004137 007402      T16:  JSR      R1,CHECK
387 002414 012777 000002 176056  MOV      @2,@XCSR     ;ENABLE THE EXTERNAL WORLD
388 002422 004237 007342  JSR      R2,WAITX     ;WAIT FOR CLEAR ERROR
389 002426 005277 176046  INC     @XCSR        ;SET T2 FLAG AGAIN
390 002432 004237 010350  JSR      R2,TOUT     ;TIME OUT DELAYS
391 002436 105777 176036  TSTB    @XCSR
392 002442 100431      BMI     T17          ;RE CLR AND PROCEED

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B2


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393 002444 004537 010520      JSR    R5,ERROR
394 002450 012737 010736 007304  MOV    @EE10,MES
395 002456 004337 007210      JSR    R3,PRINT
396 002462 004537 010536      JSR    R5,SCOPE
397 002466 000000      WLT
398 002470 000137 002474      JMP    THW
399 002474 012777 000002 175776 THW1  MOV    @2,@XCSR      ;LOCK FLOP NOT CLEARED BY
400 002502 004237 007342      JSR    R2,WAITX      ;CLEAR ERROR
401 002506 005777 175770      TST    @XCINT        ;CLEAR LOCK FOR RECYCLE
402 002512 012777 000400 175760  MOV    @000400,@XCSR ;CLEAR FLAGS SHORT LOOP,SECOND CHANCE
403 002520 000005      RESET              ;CLEAR RECIEVE FLAG
404 002522 000137 002172      JMP    T13
405
406
407
408
409

```

;WITH RECEIVE AND SHORT LOOP FLAG SET PULSE TIMER
 ;AND WAIT FOR TIME OUT OF T2 THEN ISSUE AN CLEAR INSTRUCTION
 ;AND CHECK THAT ALL FLAGS ARE CLEARED.

```

411
412 002526 004137 007402          T19: JSR    R1,CHECK
413 002532 012737 000340 177776   MOV    #340,PS
414 002540 012737 002526 010570   MOV    #T17,LOOP      ;LOOP TESTS
415 002546 005777 175730          TST    @XCINT         ;CLEAR INTERRUPT FLAGS, SHORT LOOP,SECOND CHANCE
416 002552 012777 000400 175720   MOV    @000400,@XCSR  ;CLEAR RECEIVE FLAG
417                                ITEST SHORT LOOP INTERRUPT FLAG FOR BEING CLEARED
418
419 002560 004137 007402          T10: JSR    R1,CHECK
420 002564 005777 175710          TST    @XCSR         ;TEST BIT 15 OF CSR
421 002570 100014                    BPL    T19           ;OK GO ON
422 002572 004537 010520          JSR    R5,ERROR      ;CHECK FOR REPORT OF ERROR
423 002576 012737 010750 007304   MOV    @EE19,MES     ;SET ERROR PRINT
424 002604 004337 007210          JSR    R3,PRINT
425 002610 004537 010536          JSR    R5,SCOPE
426 002614 000000                    HLT
427 002616 000137 002526          JMP    T17           ;SHORT LOOP FLAG FAILED TO CLEAR
428                                ;LOOP TO TEST 17 ON KEY "CONT"
429                                ITEST WARNING FLAG (BIT 7) FOR BEING CLEAR
430
431 002622 004137 007402          T19: JSR    R1,CHECK
432 002626 105777 175646          TSTB   @XCSR         ;TEST BIT 07 OF CSR
433 002632 100014                    BPL    T20
434 002634 004537 010520          JSR    R5,ERROR      ;CHECK FOR ERROR REPORT
435 002640 012737 010755 007304   MOV    @EE19,MES     ;SET ERROR PRINT
436 002646 004337 007210          JSR    R3,PRINT
437 002652 004537 010536          JSR    R5,SCOPE
438 002656 000000                    HLT
439 002660 000137 002526          JMP    T17           ;LOOP TO TEST 17 ON KEY "CONT"
440                                ITEST ALARM RECEIVE (BIT 14) FOR BEING CLEAR
441
442
443 002664 004137 007402          T20: JSR    R1,CHECK
444 002670 032777 040000 175602   BIT    @040000,@XCSR  ;TEST BIT 14 OF CSR
445 002676 001414                    BEQ    T21
446 002700 004537 010520          JSR    R5,ERROR      ;CHECK FOR ERROR REPORT
447 002704 012737 010762 007304   MOV    @EE20,MES     ;SET PRINT ERROR T20
448 002712 004337 007210          JSR    R3,PRINT
449 002716 004537 010536          JSR    R5,SCOPE
450 002722 000000                    HLT
451 002724 000137 000017          JMP    17            ;BIT 14 OF CSR FAILED TO A CLR
452                                ;LOOP TO TEST 17 ON CONT
453                                IENABLE ALARM OUT SIGNAL (PROGRAM CONTROL) AND TEST
454                                ;THAT TIME OUT OF T3 WILL SET ALARM RECEIVE FLOP (BIT 14)
455                                ;THE ALARM RECEIVE SIGNAL MUST BE CONNECTED TO THE ALARM OUT
456                                ;AND THE PROGRAM CONTROLLED "RESET" STRAP MUST BE CONNECTED
457
458 002730 004137 007402          T21: JSR    R1,CHECK
459 002734 012737 002730 010570   MOV    #T21,LOOP
460 002742 012737 000340 177776   MOV    #340,PS
461 002750 012777 000003 175522   MOV    #3,@XCSR      ;START TIMER AND ENABLE "ALARM OUT"
462 002756 004137 010350          JSR    R2,TOUT       ;TIME OUT DELAYS
463 002762 032777 040000 175510   BIT    @040000,@XCSR ;CHECK BIT 14 FOR BEING SET
464 002770 001402                    BEQ    .+6
  
```

D2

465	002772	000137	003026			JMP	T22	
466	002776	004537	010520			JSR	R9,ERROR	
467	003002	012737	010767	007384		MOV	#EE21,MES	;SET ERROR PRINTOUT
468	003010	004337	007210			JSR	R3,PRINT	
469	003014	004537	010536			JSR	R9,SCOPE	
470	003020	000000				HLT		;RECEIVE ALARM FLOP FAILED TO SET
471	003022	000137	002730			JMP	T21	;LOOP ON TEST 21
472								
473								
474								
475								
476								
477	003026	004137	007402		T221	JSR	R1,CHECK	
478	003032	012777	000340	175440		MOV	#340,0XCSR	
479	003040	012737	003026	013570		MOV	#T22,LOOP	;SET SCOPE RETURN
480	003046	012777	000400	175424		MOV	#000400,0XCSR	;CLEAR ALARM RECEIVE FLAG
481	003054	032777	040000	175416		BIT	#040000,0XCSR	;TEST BIT 14 FOR BEING CLEAR
482	003062	001414				BEO	T23	;FLAG CLEAR GO ON

WATCH.SRC

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484
485 003064 004537 010520 JSR R5,ERROR
486 003070 012737 010774 007384 MOV #EE22,MES
487 003076 004337 007210 JSR R3,PRINT
488 003102 004537 010536 JSR R5,SCOPE
489 003106 000000 HLT ;BIT 14 OF CSR FAILED TO CLEAR
490 003110 000137 003026 JMP T22
491
492 ;CHECK "LOCKOUT" FEATURE OF "ALARM OUT" AFTER AN ALARM
493 ;OUT SIGNAL HAS BEEN GENERATED.
494
495 003114 004137 007402 T23: JSR R1,CHECK
496 003120 012737 000340 177776 MOV #340,PS
497 003126 012737 003114 010570 MOV #T23,LOOP
498 003134 012777 000001 175336 MOV #1,0XCSR ;START TIMING
499 003142 004237 010350 JSR R2,TOUT ;TIME OUT DELAYS
500 003146 004237 007342 JSR R2,WAITX ;WAIT FOR REC TO *SET
501 003152 032777 040000 175320 BIT #040000,0XCSR ;TEST THAT LOCK OUT PREVENTED
502 003160 001414 BEO T24 ;BIT 14 FROM BEING SET
503 003162 004537 010520 JSR R5,ERROR
504 003166 012737 011001 007384 MOV #EE23,MES
505 003174 004337 007210 JSR R3,PRINT
506 003200 004537 010536 JSR R5,SCOPE
507 003204 000000 HLT ;CLEAR ERROR FAILED TO ENABLE FLOP
508 003206 000137 003114 JMP T23 ;ALARM OUT SIGNAL
509
510 ;DROP PROCESSOR STATUS TO 6 AND CHECK THAT WARNING FLAG WILL GIVE AN
511 ;INTERRUPT AT VECTOR 170
512
513 003212 005777 175264 T24: TST 0XCINT ;CLEAR SHORT LOOP, SECOND CHANCE
514 003216 012777 000400 175254 MOV #000400,0XCSR ;CLEAR RECEIVE FLAG
515 003224 004137 007402 JSR R1,CHECK
516 003230 012704 003330 MOV #T25,R4 ;SET INTERRUPT RETURN
517 003234 012705 007440 MOV #WRNG,R5 ;SET FOR INTERRUPT AT WRONG VECTOR
518 003240 012737 003212 010570 MOV #T24,LOOP
519 003246 012777 000101 175224 MOV #101,0XCSR
520 003254 004237 010350 JSR R2,TOUT
521 003260 013737 000510 177776 MOV PRIV,PS ;SET STATUS TO PRIV
522 003266 000240 NOP ;WAIT FOR INTERRUPT
523 003270 000240 NOP
524 003272 012737 000340 177776 MOV #340,PS ;SHOULD HAVE INTERRUPTED
525 003300 004537 010520 JSR R5,ERROR ;SET STATUS BACK TO SEVEN
526 003304 012737 011006 007384 MOV #EE24,MES
527 003312 004337 007210 JSR R3,PRINT
528 003316 004537 010536 JSR R5,SCOPE
529 003322 000000 HLT ;WARNING FLAG (BIT 07) FAILED
530 003324 000137 003212 JMP T24 ;TO PRODUCE AN INTERRUPT
531
532 ;CLEAR FLAGS AND SET THE SHORT LOOP
533 ;FLAG TO CHECK FOR AN INTERRUPT
534
535

```

F2

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537
538 003330 004137 007402          T29I  JSR    R1,CHECK
539 003334 000005                RESET
540 003336 005777 175140          TST    @XCIVT          ;CLEAR INTERRUPTS
541 003342 012704 003446          MOV    @AA4,R4        ;SET INTERRUPT RETURN
542 003346 012709 007440          MOV    @WRNG,R5      ;SETFOR WRONG VECTOR
543 003352 012737 003330 018570  MOV    @T29,LOOP     ;SET SCOPE MODE
544 003360 013737 000510 177776  MOV    PRIV,PS       ;GET STATUS DOWN TO PRIV
545 003366 052777 000102 175104  BIS    @102,@XCSR    ;INT.EN +EXT.EN
546 003374 005277 175100          INC    @XCSR         ;SET SHORT LOOP
547 003400 005277 175074          INC    @XCSR
548 003404 000240                NOP                    ;SHOULD INT? HERE
549 003406 000240                NOP
550 003410 012737 000340 177776  MOV    @340,PS       ;NO INT,GET STATUS BACK UP
551 003416 004537 010520          JSR    R5,ERROR
552 003422 012737 011013 007304  MOV    @EE25,MES     ;SET ERROR PRINT
553 003430 004337 007210          JSR    R3,PRINT
554 003434 004537 010536          JSR    R5,SCOPE
555 003440 000000                HLT                    ;SHORT LOOP FLAG FAILED TO RAISE A
556 003442 000137 003330          JMP    T29           ;INTERRUPT
557 003446 004237 007342          AA4I JSR    R2,WAITX     ;WAIT FOR TIME OUT CLR ERROR
558 003452 005777 175024          TST    @XCIVT        ;CLEAR FLAGS SHORT LOOP, SECOND CHANCE
559 003456 012777 000400 175014  MOV    @000400,@XCSR ;CLEAR RECEIVE FLAG
560 003464 000137 003470          JMP    T26
561
562          ;CHECK FOR ALARM RECEIVE FLAG TO GENERATE AN INTERRUPT
563          ;BY CLEARING THE WARNING FLAG BEFORE THE RECEIVE
564          ;FLAG IS SET, T3>T2 BY AT LEAST 50 MIRCO. SEC.
565
566 003470 004137 007402          T26I JSR    R1,CHECK
567 003474 012737 000340 177776  MOV    @340,PS       ;SET PROCESSOR STATUS TO 7
568 003502 012709 003626          MOV    @AA5,R5      ;SET INTERRUPT RETURN
569 003506 012704 007440          MOV    @WRNG,R4      ;SET FOR WRONG VECTOR
570 003512 012737 003446 018570  MOV    @AA4,LOOP     ;SET SCOPE
571 003520 012777 000003 174792  MOV    @3,@XCSR      ;START TIMING, ENABLE ALARM OUT
572 003526 105777 174746          TSTB   @XCSR         ;WAIT FOR WARNING
573 003532 100375                BPL    ,=4
574 003534 005777 174742          TST    @XCIVT        ;CLEAR BIT 7 OF CSR
575 003540 032777 040000 174732  BIT    @040000,@XCSR ;WAIT FOR ALARM RECEIVE FLAG
576 003546 001774                BEQ    ,=6
577 003550 052777 000100 174722  BIS    @100,@XCSR    ;ENABLE INT.-2L
578 003556 013737 000510 177776  MOV    PRIV,PS       ;SET STATUS TO PRIV
579 003564 000240                NOP                    ;SHOULD INT? HERE
580 003566 000240                NOP
581 003570 012737 000340 177776  MOV    @340,PS       ;FAILED TO INT. SET STATUS TO 7
582 003576 004537 010520          JSR    R5,ERROR      ;CHECK FOR ERROR REPORT
583 003602 012737 011020 007304  MOV    @EE25,MES
584 003610 004337 007210          JSR    R3,PRINT
585 003614 004537 010536          JSR    R5,SCOPE
586 003620 000000                HLT                    ;CHECK FOR SCOPE ROUTINE
587 003622 000137 003446          JMP    AA4
588 003626 004237 010350          AA9I JSR    R2,TOUT       ;CLR FLAGS BEFORE LOOP
589 003632 012777 000400 174640  MOV    @000400,@XCSR ;CLEAR POSSIBILITY OF SHORT LOOP
590 003640 000137 003644          JMP    T27           ;CLEAR RECEIVE FLAG
                    ;T 27

```


591						
592						
593						ICHECK LOCK OUT OF SHORT LOOP BY FIRST CAUSING A
594						ISHORT LOOP FLAG THEN READING STATUS OF RECEIVE TO CHECK
595						THAT T3 HAS BEEN TERMINATED
596						
597	003644	004137	007402	T291	JSR	R1,CHECK
598	003650	012737	003626	010570	MOV	#AA5,LOOP
599	003656	012737	000340	177776	MOV	#340,PS
600	003664	005777	174612		TST	#XCINT
601	003670	005077	174604		CLR	#XCSR
602	003674	012777	000003	174576	MOV	#3,#XCSR ;SET SHORT LOOP
603	003702	005277	174572		INC	#XCSR
604	003706	004237	007342		JSR	R2,WAITX ;5,MILLI.SEC.CLEAR LOCK AND ENABLE
605	003712	032777	040000	174560	BIT	#040000,#XCSR
606	003720	001014			BNE	T20
607	003722	004537	010520		JSR	R5,ERROR
608	003726	012737	011025	007304	MOV	#EE27,MES
609	003734	004337	007210		JSR	R3,PRINT
610	003740	004537	010536		JSR	R5,SCOPE
611	003744	000000			HLT	;SHORT LOOP LOCK FAILED TO TERMINATE T3
612	003746	000137	003626		JMP	AA5
613						
614						ITEST THAT T2 WAS TERMINATED BY A SHORT LOOP LOCK BY
615						TESTING STATUS OF T2
616						
617	003752	004137	007402	T201	JSR	R1,CHECK
618	003756	012737	003752	010570	MOV	#T20,LOOP
619	003764	004237	010350		JSR	R2,TOUT
620	003770	012777	000400	174502	MOV	#000400,#XCSR ;CLEAR RECEIVE FLAG
621	003776	005777	174500		TST	#XCINT ;CLR FLAGS SHORT LOOP, SECOND CHANCE
622	004002	012777	000003	174470	MOV	#3,#XCSR ;EXT EN, SET S.LOOP
623	004010	005277	174464		INC	#XCSR
624	004014	105777	174460		TSTB	#XCSR ;TEST BIT 9
625	004020	100014			BPL	T20
626	004022	004537	010520		JSR	R5,ERROR
627	004026	012737	011032	007304	MOV	#EE20,MES
628	004034	004337	007210		JSR	R3,PRINT
629	004040	004337	010536		JSR	R3,SCOPE
630	004044	000000			HLT	;LOCK FAILED TO TERMINATE T2
631	004046	000137	003752		JMP	T20 ;LOOP ONTEST 20
632						
633						
634						IWAIT 5 MILLI SEC. FOR CLEAR ERROR TO RELEASE
635						THE LOCK FLOP AND PASS T2 TO BUS
636						
637						
638	004052	004137	007402	T201	JSR	R1,CHECK
639	004056	004237	007342		JSR	R2,WAITX
640	004062	105777	174412		TSTB	#XCSR
641	004066	100414			BMI	T30
642	004070	004537	010520		JSR	R5,ERROR
643	004074	012737	011037	007304	MOV	#EE29,MES
644	004102	004337	007210		JSR	R3,PRINT

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645 004106 004537 010536      JSR    R5,SCOPE
646 004112 000000              HLT
647 004114 000137 003752      JMP    T20                ;LOCK DIDNT RELEASE T2 TO BUS
648                                ;LOOP ON TEST 20
649                                ;
650                                ;
651                                ;CHECK THAT LOCK FROM SHORT LOOP FLAG
652                                ;LOCKS PULSE ING OF TIMER BY ATTEMPTING TO SET SHORT
653                                ;LOOP FLAG AFTER A PREVIOUS SHORT LOOP
654                                ;
655 004120 004137 007402      JSR    R1,CHECK          T30:
656 004124 012737 000340 177776  MOV    #340,PS
657 004132 012737 004120 013570  MOV    #T30,LOOP
658 004140 005777 174336      TST    @XCIN             ;CLEAR FLAGS SHORT LOOP,SECOND CHANCE
659 004144 005277 174330      INC    @XCSR
660 004150 005277 174324      INC    @XCSR
661 004154 005777 174322      TST    @XCIN             ;CLR FLAGS SHORT LOOP,SECOND CHANCE
662 004160 005277 174314      INC    @XCSR
663 004164 005277 174310      INC    @XCSR
664 004170 005777 174304      TST    @XCSR
665 004174 100014              BPL    PTR
666 004176 004537 010520      JSR    R5,ERROR
667 004202 012737 011044 007304  MOV    @EE30,MES
668 004210 004337 007210      JSR    R3,PRINT
669 004214 004537 010536      JSR    R5,SCOPE
670 004220 000000              HLT
671 004222 000137 004120      JMP    T30                ;SHORT LOOP LOCK FAILED TO LOCK TIMER
672                                ;LOOP ON TEST 30
673 004226 012777 000002 174244  PTR:  MOV    #2,@XCSR
674 004234 004237 007342      JSR    R2,WAITX          ;CLR ERROR
675 004240 005777 174236      TST    @XCIN             ;CLEAR FLAGS SHORT LOOP,SECOND CHANCE
676                                ;
677                                ;
678                                ;GENERATE A SHORT LOOP COMMAND AND CHECK THAT INITIALIZE
679                                ;WILL CLEAR THE SHORT LOOP FLAG,
680                                ;
681                                ;
682 004244 004137 007402      JSR    R1,CHECK          T31:
683 004250 012737 004244 013570  MOV    #T31,LOOP
684 004256 005277 174216      INC    @XCSR             ;SET A SHORT LOOP
685 004262 005277 174212      INC    @XCSR
686 004266 000005              RESET
687 004270 005777 174204      TST    @XCSR             ;TEST SHORT LOOP FLAG FOR CLEAR
688 004274 100014              BPL    T32
689 004276 004537 010520      JSR    R5,ERROR
690 004302 012737 011051 007304  MOV    @EE31,MES
691 004310 004337 007210      JSR    R3,PRINT
692 004314 004537 010536      JSR    R5,SCOPE
693 004320 000000              HLT
694 004322 000137 004244      JMP    T31                ;INITIALIZE FAILED TO CLEAR SHORT
695                                ;LOOP FLAG
696                                ;
697                                ;ENABLE THE EXTERNAL WORLD AND ALLOW THE RECIEVE
698                                ;FLAG TO SET THEN CHECK THAT THE INITIALIZE
699                                ;CLEARED RECEIVE FLAG.

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699
700 004326 004137 007402          T321 JSR    R1,CHECK
701 004332 012737 004326 010570 MOV    @T32,LOOP
702 004340 012777 000002 174132 MOV    @2,@XCSR
703 004346 004237 007342 JSR    R2,WAITX          ;5.MILLI SEC SET REC
704 004352 000005 RESET
705 004354 032777 040000 174116 BIT    @040000,@XCSR          ;TEST RECIEVE FLAG
706 004362 001414 BEO    T33
707 004364 004537 010520 JSR    R5,ERROR
708 004370 012737 011056 007304 MOV    @EE32,MES
709 004376 004337 007210 JSR    R3,PRINT
710 004402 004537 010536 JSR    R5,SCOPE
711 004406 000000 HLT
712 004410 000137 004326 JMP    T32          ;INITIALIZE FAILED TO CLEAR REC
713                                     ;FLAG
714
715                                     ;
716                                     ;TEST THAT INITIALIZE WILL CLEAR THE LOCK FLOP
717                                     ;BY SETTING A SHORT LOOP FLAG AND ISSUEING A RESET INSTR
718                                     ;-UCTION, TEST THAT THE LOCK FLOP IS CLEARED BY SETTING
719                                     ;A 2ND SHORT LOOP FLAG.
720                                     ;
721                                     ;
722 004414 004137 007402          T331 JSR    R1,CHECK
723 004420 012737 004414 010570 MOV    @T33,LOOP
724 004426 005277 174046 INC     @XCSR
725 004432 005277 174042 INC     @XCSR
726 004436 000005 RESET          ;ATTEMPT TO CLEAR SHORT LOOP
727 004440 005277 174034 INC     @XCSR
728 004444 005277 174030 INC     @XCSR
729 004450 005777 174024 TST    @XCSR          ;TEST SHOT LOOP
730 004454 100414 BHI    PTX1
731 004456 004537 010520 JSR    R5,ERROR
732 004462 012737 011063 007304 MOV    @EE33,MES
733 004470 004337 007210 JSR    R3,PRINT
734 004474 004537 010536 JSR    R5,SCOPE
735 004500 000000 HLT          ;INITIALIZE FAILED TO CLEAR LOCK
736 004502 000137 004414 JMP    T33
737 004506 012777 000002 173764 PTX11 MOV    @2,@XCSR
738 004514 004237 007342 JSR    R2,WAITX          ;WAIT 5.M.S. FOR ERROR TO CLR
739                                     ;
740                                     ;PULSE TIMER AND ISSUE A RESET INSTRUCTION, WAIT 5.MILLI
741                                     ;WITH EXTERNAL ENABLE SETAND TEST RECEIVE FLAG TO
742                                     ;CHECK THAT INITIALIZE TERMINATED T3,
743                                     ;
744 004520 004137 007402          T341 JSR    R1,CHECK
745 004524 012737 004520 010570 MOV    @T34,LOOP
746 004532 012777 000001 173740 MOV    @1,@XCSR          ;PULSE TIMER & EX. CN SET
747 004540 000005 RESET
748 004542 012777 000002 173730 MOV    @2,@XCSR
749 004550 004237 007342 JSR    R2,WAITX          ;WAIT 5. MILLI SEC FOR T4
750 004554 032777 040000 173716 BIT    @040000,@XCSR          ;TEST RECEIVE FLAG
751 004562 001020 BNE    PTX2
752 004564 004237 010350 JSR    R2,TOUT
    
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753 004570 005777 173706          TST    @XCINT
754 004574 004537 010520          JSR    R5,ERROR
755 004600 012737 011070 007304  MOV    @EE34,MES
756 004606 004337 007210          JSR    R3,PRINT
757 004612 004537 010536          JSR    R5,SCOPE
758 004616 000000                      HLT
759 004620 000137 004520          JMP    T34 ;INITIALIZE FAILED TO TERMINATE
760 004624 004237 010350          JSR    R2,TOUT ;TS
761 004630 005777 173646          TST    @XCINT ;CLEAR SHORT LOOP,SECOND CHANCE
762 004634 012777 000400 173636  MOV    @000400,@XCSR ;CLEAR RECEIVE FLAG
763
764 ;
765 ;PULSE TIMER AND ISSUE A RESET INSTRUCTION
766 ;WAIT FOR POSSIBLE TIME-OUT OF T2 THEN READ
767 ;STATUS OF T2 TO TEST THAT INITIALIZE
768 ;TERMINATED T2.
769 004642 004137 007402          JSR    R1,CHECK
770 004646 012737 004642 010570 3391  MOV    @T35,LOOP
771 004654 012777 000003 173616  MOV    @3,@XCSR
772 004662 000005                      RESET
773 004664 004237 010350          JSR    R2,TOUT ;WAIT FOR DELAYS TO TIME OUT
774 004670 105777 173604          TSTB  @XCSR ;TEST BIT 9
775 004674 100016                      BPL    PTX3
776 004676 005777 173600          TST    @XCINT ;CLEAR FLAGS
777 004702 004537 010520          JSR    R5,ERROR
778 004706 012737 011075 007304  MOV    @EE35,MES
779 004714 004337 007210          JSR    R3,PRINT
780 004720 004537 010536          JSR    R5,SCOPE
781 004724 000000                      HLT
782 004726 000137 004642          JMP    T35 ;INITIALIZE FAILED TO TERMINATE T2
783 004732 005777 173544          TST    @XCINT ;CLEAR FLAGS SHORT LOOP, SECOND CHANCE
784 004736 012777 000400 173534  MOV    @000400,@XCSR ;CLEAR RECEIVE FLAG
785
786 ;
787 ;TEST STATUS A&B AND TEST THAT BITS 9 & 15 ARE COMPLEMENTS
788 ;15=1 AND 9=0 FROM A RESET CONDITION
789 004744 004137 007402          JSR    R1,CHECK
790 004750 000005                      RESET
791 004752 012737 000340 177776  MOV    @340,@PS
792 004760 012737 004744 010570  MOV    @T36,LOOP
793 004766 005777 173512          TST    @XECR ;CHECK BIT 15 OF ECSR
794 004772 100005                      BPL    TILT
795 004774 105777 173504          TSTB  @XECR ;CHECK BIT 7 OF EXT CSR 15=1
796 005000 100402                      BMI    TILT ;REPORT ERROR BOTH SAME
797 005002 000137 005040          JMP    T37 ;OK 15=1 7=0
798 005006 000240          TILT: NOP
799 005010 004537 010520          JSR    R5,ERROR
800 005014 012737 011102 007304  MOV    @EE36,MES
801 005022 004337 007210          JSR    R3,PRINT
802 005026 004537 010536          JSR    R5,SCOPE
803 005032 000000                      HLT ;INCORECT STATUS IN EXT. CSR
804 005034 000137 004744          JMP    T36
805
806 ;ISSUE A RESET INSTRUCTION AND TEST THAT STATUS

```

K2


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007
008
009 005040 004137 007402          T39: JSR      R1,CHECK
010 005044 017737 173434 005724    MOV      @XECR,PPL          ;SAVE EXT STATUS
011 005052 012737 005040 010570    MOV      @T37,LOOP
012 005060 000005                RESET
013 005062 004237 007342          JSR      R2,WAITX          ;WAIT FO RELAY
014 005066 067737 173412 005724    ADD      @XECR,PPL          ;TEST FOR STATUS CHANGE
015 005074 100014                BPL      T30
016 005076 004537 010520          JSR      R5,ERROR
017 005102 012737 011107 007304    MOV      @EE37,MES
018 005110 004337 007210          JSR      R3,PRINT
019 005114 004537 010536          JSR      R5,SCOPE
020 005120 000000                HLT
021 005122 000137 005040          JMP      T37                ;RESET INSTRUCTION CHANGED STATUS
022                                     ;OF EXT CSR
023
024
025                                     ;WITH LATCH IN NEUTRAL POSITION SWITCH BUSS AND
026                                     ;CHECK FOR CHANGE OF STATUS IN EXT, CSR
027 005126 004137 007402          T30: JSR      R1,CHECK
028 005132 000005                RESET
029 005134 012737 005126 010570    MOV      @T30,LOOP
030 005142 012737 011157 007304    MOV      @EE30,MES
031 005150 017737 173330 005724    MOV      @XECR,PPL          ;SAVE EXT, STATUS
032 005156 005277 173324          INC      @XSWBU            ;SWITCH BUSS
033 005162 004237 007342          JSR      R2,WAITX
034 005166 004337 006100          JSR      R3,OPP            ;CHECK THAT BITS ARE OF OPPOSITE
035 005172 067737 173306 005724    ADD      @XECR,PPL          ;POLARITY
036 005200 100414                BMI     T30
037 005202 004537 010520          JSR      R5,ERROR
038 005206 012737 011114 007304    MOV      @EE30,MES
039 005214 004337 007210          JSR      R3,PRINT
040 005220 004537 010536          JSR      R5,SCOPE
041 005224 000000                HLT
042 005226 000137 005126          JMP      T30                ;SWITCHING BUSS FAILED
043
044
045                                     ;WITH BUS SWITCH'D CHECK THAT LATCH WILL DE-ENERGIE RELAY ON
046                                     ;A SECOND SWITCHING OF THE BUS
047                                     ;TEST THAT STATUS CHANGED (NEUTRAL POSITION)
048
049
050 005232 004137 007402          T39: JSR      R1,CHECK
051 005236 012737 005232 010570    MOV      @T39,LOOP
052 005244 017737 173234 005724    MOV      @XECR,PPL          ;SAVE EXT STATUS
053 005252 005277 173230          INC      @XSWBU            ;ATTEMPT TO SWITCH BUSS
054 005256 004237 007342          JSR      R2,WAITX          ;WAIT FOR RELAY
055 005262 067737 173216 005724    ADD      @XECR,PPL          ;WAS BUSS STATUS CHANGED
056 005270 100414                BMI     T40
057 005272 004537 010520          JSR      R5,ERROR
058 005276 012737 011121 007304    MOV      @EE39,MES
059 005304 004337 007210          JSR      R3,PRINT
060 005310 004537 010536          JSR      R5,SCOPE

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861 005314 000000          HLT           ;LATCH FAILED TO PREVENT BUSS CHANGE
862 005316 000137 005232  JMP           T39
863                                     ;
864                                     ;ISSUE A SWITCH BUS COMMAND AND CHECK THAT STATUS
865                                     ;A & B CHANGED TO NEXT LATCH
866                                     ;
867                                     ;
868 005322 004137 007402          T40: JSR           R1,CHECK
869 005326 012737 005322 010570  MOV           #T40,LOOP
870 005334 017737 173144 005724  MOV           @XCSR,PPL
871 005342 005277 173140          INC           @XSWBU           ;SWITCH BUS
872 005346 004237 007342          JSR           R2,WAITX       ;5 MILLI SEC FOR RELAY
873 005352 012737 011165 007304  MOV           @EE40,MES
874 005360 004337 006100          JSR           R3,OPP         ;TEST FOR POL.CHANGE
875 005364 067737 173114 005724  ADD           @XCSR,PPL     ;TEST THAT STATUS CHANGED
876 005372 100414          BHI           T41
877 005374 004537 010520          JSR           R5,ERROR
878 005400 012737 011126 007304  MOV           @EE40,MES
879 005406 004337 007210          JSR           R3,PRINT
880 005412 004537 010536          JSR           R5,SCOPE
881 005416 000000          HLT
882 005420 000137 005322          JMP           T40           ;BUS FAILED TO SWITCH TO 2ND LATCH
883                                     ;
884                                     ;
885                                     ;
886                                     ;ENABLE EXTERNALWORLD AND ALLOW DELAYS TO TIME
887                                     ;OUT TO CHECK THAT TERMINATION OF T3 WILL RELEASE THE LATCH
888                                     ;
889                                     ;
890 005424 004137 007402          T41: JSR           R1,CHECK
891 005430 012737 005322 010570  MOV           #T40,LOOP
892 005436 017737 173042 005724  MOV           @XCSR,PPL     ;SAVE STATUS A&B
893 005444 012777 000003 173026  MOV           #3,@XCSR     ;ALLOW FOR CLEAR ERROR
894 005452 004237 010350          JSR           R2,TOUT        ;TIME OUT ALLDELAYS
895 005456 004237 007342          JSR           R2,WAITX       ;5 MILLI.SEC FOR RELAYS
896 005462 012737 011173 007304  MOV           @EE41,MES     ;SET SUBTEST PRINT
897 005470 004337 006100          JSR           R3,OPP         ;SUBTEST
898 005474 067737 173004 005724  ADD           @XCSR,PPL
899 005502 100414          BHI           T42           ;IF STATUS CHANGED GO ON
900 005504 004537 010520          JSR           R5,ERROR
901 005510 012737 011133 007304  MOV           @EE41,MES
902 005516 004337 007210          JSR           R3,PRINT
903 005522 004537 010536          JSR           R5,SCOPE
904 005526 000000          HLT
905 005530 000137 005424          JMP           T41
906                                     ;
907                                     ;
908                                     ;
909                                     ;ISSUE A SECOND SWITCH BUSS COMAND AND CHECK THAT SWBU (164006)
910                                     ;WILL SWITCH BUS
911                                     ;
912 005534 004137 007402          T42: JSR           R1,CHECK
913 005540 012737 005534 010570  MOV           #T42,LOOP
914 005546 017737 172732 005724  MOV           @XCSR,PPL
  
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MZ


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915 005554 005277 172720      INC      0XSW3U      ;ATTEMPT TO SWITCH BUSS
916 005560 004237 007342      JSR      R2, WAITX  ;5 MILLI SEC FOR RELAY
917 005564 067737 172714 005724  ADD      0XCSR, PPL ;DID STATUS CHANGE
918 005572 100414      BMI     T43        ;IF MINUS STATUS CHANGED
919 005574 004537 010520      JSR      R5, ERROR
920 005600 012737 011140 007304  MOV      @EE42, MES
921 005606 004337 007210      JSR      R3, PRINT
922 005612 004537 010536      JSR      R5, SCOPE
923 005616 000000      HLT
924 005620 000137 005534      JMP      T42        ;LATCH FAILED TO PREVENT BUSS FROM
925                                ;SWITCHING
926                                ;
927                                ;ISSUE A "RESET" INSTRUCTION AND TEST THAT
928                                ;LATCH GETS CLEARED
929                                ;
930 005624 004137 007402      JSR      R1, CHECK  T43I
931 005630 012737 005624 013570  MOV      @T43, LOOP
932 005636 017737 172642 005724  MOV      0XCSR, PPL      ;SAVE STATUS
933 005644 012737 011201 007304  MOV      @EE43S, MES    ;SET SUBTEST PRINT
934 005652 000005      RESET          ;CLEAR LATCH
935 005654 004237 007342      JSR      R2, WAITX  ;WAIT FOR RELAY
936 005660 004337 006100      JSR      R3, OPP
937 005664 067737 172614 005724  ADD      0XCSR, PPL    ;TEST FOR STATUS CHANGE
938 005672 100415      BMI     T44        ;IF MINUS STATUS CHANGED
939 005674 004537 010520      JSR      R5, ERROR
940 005700 012737 011145 007304  MOV      @EE43, MES
941 005706 004337 007210      JSR      R3, PRINT
942 005712 004537 010536      JSR      R5, SCOPE
943 005716 000000      HLT          ;RESET FAILED TO RELEASE LATCH
944 005720 000137 005624      JMP      T43
945                                ;
946                                ;
947                                ;
948 005724 000000      PPLI          ;TEST DATA POINT
949                                ;
950                                ;
951                                ;TEST THAT "MANUAL" EXTERNAL ENABLE CIRCUITRY FUNCTIONS
952                                ;BY SETTING THE ENABLE FLOP FROM A SWITCHING OF THE BUS
953                                ;(VIA TEST CONNECTOR)
954                                ;
955 005726 004137 007402      JSR      R1, CHECK  T44I
956 005732 012737 005726 013570  MOV      @T44, LOOP
957 005740 012777 000003 172532  MOV      @3, 0XCSR
958 005746 004237 010350      JSR      R2, TOUT    ;CLEAR ANY ERROR CONDITIONS
959 005752 005777 172524      TST     0XCIVT      ;CLEAR FLAGS SHORT LOOP, SECOND CHANCE
960 005756 012777 000400 172514  MOV      @000400, 0XCSR ;CLEAR RECEIVE FLAG
961 005764 005277 172516      INC      0XSW3U
962 005770 004237 007342      JSR      R2, WAITX  ;SWITCH BUSS WAIT FOR RELAY
963 005774 005277 172500      INC      0XCSR      ;GENERATE A SHORT LOOP ERROR, RECEIVE FLAG SHOULD
964 006000 005277 172474      INC      0XCSR      ;GET SET WITH EXTERNAL ENABLE SET BY SWITCH BUS COMMAND
965 006004 004237 007342      JSR      R2, WAITX
966 006010 032777 040000 172462  BIT     @40000, 0XCSR
967 006016 001014      BNE     INIT
968 006020 004537 010520      JSR      R5, ERROR
    
```

A3


```

969 006024 012737 011152 007304      MOV      @EE44, MES
970 006032 004337 007210              JSR      R3, PRINT
971 006036 004537 010536              JSR      R5, SCOPE
972 006042 000000              HLT
973 006044 000137 005726              JMP      T44      ;MANUAL ENABLE INPUT CIRCUITRY FAILED
974
975
976
977
978
979
980
981 006050 000005 011233 007304      INI TI  RESET
982 006052 012737 011233 007304      MOV      @PASS, MES      ;INITIALIZE WORLD
983 006060 004337 007210              JSR      R3, PRINT      ;SET PASS PRINT
984 006064 004137 007402              JSR      R1, CHECK      ;CHECK FOR TELTYPE COMMANDS
985 006070 012706 000600              MOV      @STACK, SP
986 006074 000137 001030              JMP      T1
987
988
989
990
991
992 006100 005777 172400      OPPI  TST      @XCSR      ;TEST BIT 15 OF ESCR
993 006104 100004              BPL      ,+12
994 006106 105777 172372      TSTB    @XCSR      ;BIT 15=1 TEST BIT 7
995 006112 100405              BMI     ,+14      ;REPORT A&B SAME
996 006114 000203              RTS      R3
997 006116 105777 172362      TSTB    @XCSR      ;15=1 7=0
998 006122 100001              BPL      ,+4      ;REPORT BOTH SAME
999 006124 000203              RTS      R3
1000 006126 004537 010520      JSR      R5, ERROR
1001 006132 000240              NOP
1002 006134 000240              NOP
1003 006136 000240              NOP
1004 006140 004337 007210      JSR      R3, PRINT
1005 006144 004537 010536      JSR      R5, SCOPE
1006 006150 000000              HLT
1007 006152 000177 002412      JMP      @LOOP      ;LOOP ON FAILING TEST
1008 006156 000203              RTS      R3      ;OK 15=1 7=0
1009 006160 105777 172320      TSTB    @XCSR      ;15=0 TEST 7
1010 006164 100001              BPL      ,+4      ;REPORT BOTH SAME
1011 006166 000203              RTS      R3      ;OK 15=0 7=1
1012 006170 004537 010520      JSR      R5, ERROR      ;CHECK FOR ERROR REPORT
1013 006174 000240              NOP
1014 006176 000240              NOP
1015 006200 000240              NOP
1016 006202 004237 007210      JSR      R2, PRINT
1017 006206 004537 010536      JSR      R5, SCOPE
1018 006212 000000              HLT
1019 006214 000177 002350      JMP      @LOOP      ;LOOP ON FAILING TEST
1020
1021
1022

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1024
1025
1026
1027
1028
1029
1030 006220 012737 000340 177776 DELAY1 MOV 0340,PS ;KEEP STATUS AT 7 FOR ENTIRE TEST
1031 006226 104000 NULL
1032 006230 000005 RESET
1033 006232 104000 NULL
1034 006234 012737 011277 007304 MOV 0DELYST,MES ;PRINT "DELAY ADJUST TEST"
1035 006242 004337 007210 JSR R3,PRINT
1036 006246 012737 011327 007304 LREPI MOV 0ASK,MES ;ASK FOR DELAY 1, 2
1037 006254 004337 007210 JSR R3,PRINT
1038 006260 004137 007306 JSR R1,REC ;RECIEVE ONE CHARACTER FROM TELE
1039 006264 004337 007172 JSR R3,ECHO ;ECHO CHARACTER
1040 006270 023727 007170 003261 CMP HLD,0261
1041 006276 001413 BEQ 01 ;RUN DELAY 1 (RECEIVE) TIMING TEST
1042 006300 023727 007170 003262 CMP HLD,0262
1043 006306 001432 BEQ 02 ;RUN DELAY 2 (WARNING & S.L.) TIMING TEST
1044 006310 012737 011402 007304 MOV 0QU,MES ;PRINT A ?
1045 006316 004337 007210 JSR R3,PRINT
1046 006322 000137 006246 JMP LREP ;REPEAT LINE
1047
1048
1049 006326 012737 000340 177776 01i MOV 0340,PS
1050 006334 012777 000400 172136 MOV 0000400,0XCSR ;CLEAR RECEIVE FLAG
1051 006342 012777 000003 172130 MOV 03,0XCSR ;PULSE WARNING FLAG DELAY
1052 006350 032777 040000 172122 BIT 0040000,0XCSR ;MONITOR BIT 14
1053 006356 001774 BEQ ,=6
1054 006360 004237 010350 JSR R2,TOUT ;WAIT APPROX 10.-6 SEC
1055 006364 004137 007402 JSR R1,CHECK
1056 006370 000137 006326 JMP 01
1057 ;RUN WARNING FLAG & SHORT LOOP DELAY TIMING TESTS
1058
1059 006374 012737 000340 177776 02i MOV 0340,PS
1060 006402 005777 172074 TST 0XCINT ;CLEAR FLAG
1061 006406 012777 000001 172064 MOV 01,0XCSR ;PULSE ALARM DELAY
1062 006414 105777 172060 TSTB 0XCSR ;TEST BIT 9
1063 006420 100375 BPL ,=4
1064 006422 004237 007342 JSR R2,WAITX
1065 006426 004137 007402 JSR R1,CHECK ;CHECK FOR TELETYPE COMMANDS
1066 006432 000137 006374 JMP 02 ;RECYCLE
1067
1068

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1070
1071
1072
1073
1074
1075
1076
1077 006436 012737 011463 007304 DYNAMI MOV 0DVTST,MES
1078 006444 004337 007210 JSR R3,PRINT
1079 006450 104000 NULL
1080 006452 000005 RESET
1081 006454 004137 007402 DYXI JSR R1,CHECK
1082 006460 017737 172020 007056 MOV 0XCSR,SIRE ;SAVE STATUS
1083 006466 012737 000340 177776 MOV 0340,PS ;SET STATUS
1084 006474 012704 006562 MOV 0MOR4,R4 ;SET INT. RETURN
1085 006500 012705 006562 MOV 0MOR4,R5
1086 006504 012737 000120 007054 MOV 0120,COUNT ;SET COUNTER FOR 100 PASSES
1087 006512 012777 000103 171760 PTI MOV 0103,0XCSR ;START TIMING, ENABLE ALARM OUT
1088 006520 013737 000510 177776 MOV PRIV,PS ;STATUS=6
1089 006526 000240 NOP
1090 006530 000137 006526 JMP 02 ;STAY HERE WAIT FOR INTERRUPT
1091 006534 012737 011502 007304 HEREI MOV 0SLF,MES ;SHORT LOOP FLAG SET
1092 006542 004337 007210 JSR R3,PRINT
1093 006546 004237 010350 JSR R2,TOUT ;TIME OUT DELAYS
1094 006552 005777 171724 TST 0XCINT ;CLEAR FLAGS
1095 006556 000137 006512 JMP 07 ;RECYCLE TEST
1096 006562 005777 171712 HORN1 TST 0XCSR ;FIND WHO GAVE INTERRUPT
1097 006566 100702 BHI HERE
1098 006570 105777 171704 TSTB 0XCSR ;CHECK BIT 7
1099 006574 100407 BHI OKK ;ALL RIGHT GO
1100 006576 032777 040000 171674 BIT 004000,0XCSR ;NOT BIT 7 SO TRY 14
1101 006604 001505 BEQ ERR ;ILLEGAL INT.
1102 006606 105777 171666 TSTB 0XCSR
1103 006612 100375 BPL 04
1104 006614 032777 040000 171656 OKKI BIT 040000,0XCSR ;BIT 7=1 WAIT FOR 14
1105 006622 001774 BEQ 06
1106 006624 005777 171652 TST 0XCINT ;CLEAR FLAGS SHORT LOOP, SECOND CHANCE
1107 006630 012777 000400 171642 MOV 000400,0XCSR ;CLEAR RECEIVE FLAG
1108 006636 005277 171644 INC 0XSW3U ;SWITCH BUS
1109 006642 004237 007342 JSR R2,WAITX
1110 006646 067737 171632 007056 ADD 0XCSR,SIRE
1111 006654 100410 BHI CLST ;BR IF STATUS CHANGED
1112 006656 104000 NULL
1113 006660 012737 011552 007304 MOV 0BBS,MES ;REPORT EXT. STATUS BAD
1114 006666 004337 007210 JSR R3,PRINT
1115 006672 000137 006454 JMP DYX
1116 006676 017737 171602 007056 CLSTI MOV 0XCSR,SIRE
1117 006704 000005 RESET ;CLEAR LATCH
1118 006706 004237 007342 JSR R2,WAITX
1119 006712 067737 171566 007056 ADD 0XCSR,SIRE
1120 006720 100410 BHI T1KE
1121 006722 104000 NULL
1122 006724 012737 011552 007304 MOV 0BBS,MES
1123 006732 004337 007210 JSR R3,PRINT
    
```

DS


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1124 006736 000137 006454          JMP      DYX
1125 006742 005337 007054          TIMEI  DEC      COUNT
1126 006746 001404          BEQ      ,+12          ;BRANCH WHEN DONE
1127 006750 004137 007402          JSR      R1,CHECK
1128 006754 000137 006512          JMP      PT
1129 006760 012737 000340 177776          MOV      #340,PS
1130 006766 104000          NULL
1131 006770 012737 011233 007304          MOV      #PASS,MES
1132 006776 004337 007210          JSR      R3,PRINT
1133 007002 104000          NULL
1134 007004 004237 010350          JSR      R2,TOUT
1135 007010 004237 010350          JSR      R2,TOUT
1136 007014 000137 006454          JMP      DYX
1137 007020 012737 011527 007304  ERR:  MOV      #IINT,MES
1138 007026 004337 007210          JSR      R3,PRINT
1139 007032 004237 010350          JSR      R2,TOUT
1140 007036 005777 171440          TST      @XCINT          ;CLEAR SHORT LOOP,SECOND CHANCE
1141 007042 012777 000400 171430          MOV      @000400,@XCSR  ;CLEAR RECEIVE FLAG
1142 007050 000137 006512          JMP      PT
1143 007054 000000          COUNTI 0
1144 007056 000000          SIREI   0
1145          |
1146          |
1147          |
1148          |PRINT HEADER ROUTINE AND RECIEVE TELETYPE COMMANDS
1149          |TO SPECIFY DESIRED TESTS
1150          |
1151 007060 005037 177562          HEADER: CLR      TKB          ;CLEAR DONE OF READER STATUS
1152 007064 012737 011405 007304          MOV      @HEAD,MES
1153 007072 004337 007210          JSR      R3,PRINT          ;ASK FOR DESIRED TEST
1154 007076 004137 007306          JSR      R1,REC          ;RECIEVE ONE CHARACTER
1155 007102 004337 007172          JSR      R3,ECHO          ;ECHO TELEREADER CHARACTER
1156 007106 023727 007170 000261          CMP      #LD,#261          ;TEST A=LOGIC TEST
1157 007114 001417          BEQ      TA
1158 007116 023727 007170 000262          CMP      #LD,#262          ;TEST B=TIME DELAY TEST
1159 007124 001415          BEQ      TB
1160 007126 023727 007170 000263          CMP      #LD,#263          ;TEST C=SYSTEM STATUS TEST
1161 007134 001413          BEQ      TC
1162 007136 012737 011402 007304          MOV      #QU,MES          ;TYPE ?
1163 007144 004337 007210          JSR      R3,PRINT
1164 007150 000137 007060          JMP      HEADER          ;ILLEGAL CHARACTER TRY AGAIN
1165 007154 000137 001000          TAI    JMP      LOGIC          ;LOGIC TEST
1166 007160 000137 006220          TBI    JMP      DELAY          ;DELAY TIME LOOP
1167 007164 000137 006436          TCI    JMP      DYMAN          ;DYNAMIC TEST?
1168 007170 000000          HLDI   0          ;HOLD TEST DESIRED
  
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1170
1171
1172 007172 013737 177562 177566 ECHOI  I
1173 007200 105737 177564          MOV   TK8, TYDB      ;READER BUFFER TO PRINTER BUFFER
1174 007204 100375          TSTB  TYSR          ;TEST PRINTER STATUS
1175 007206 000203          BPL   ,=4
1176          RTS   R3
1177          IPRINT DATA SPECIFIED BY LEADING ADDRESS IN REGISTER 4
1178          UNTIL TERMINATED BY (0)
1179 007210 104030          PRINTI NULL
1180 007212 013704 007304          MOV   #0, R4
1181 007216 112437 007302          MOVB (R4), DBUF
1182 007222 122737 000100 007302          CPB  0100, DBUF
1183 007230 001422          BEQ  DONE
1184 007232 122737 000045 007302          CPB  045, DBUF
1185 007240 001004          BNE  OUT
1186 007242 004237 010466          JSR  R2, LPCR
1187 007246 000137 007216          JMP  PRINT=6
1188 007252 004537 007260          OUTI JSR  R5, PRT
1189 007256 000757          BR   PRINT=6
1190
1191 007260 113737 007302 177566 PR9I  I
1192 007266 105737 177564          MOVB DBUF, TYDB
1193 007272 100375          TSTB  TYSR
1194 007274 000205          BPL   ,=4
1195 007276 104000          DONEI NULL
1196 007300 000203          RTS   R3
1197 007302 000000          DBUFI 0
1198 007304 000000          MESI 0
1199
1200          I
1201          IRECEIVE ONE CHARACTER FROM TELETYPE READER
1202          IBUFFER AND STORE IN LOC. "HLD"
1203          I
1204 007306 105737 177560          RECI  TSTB  TK8          ;WAIT FOR KEYBOARD
1205 007312 100375          BPL   ,=4
1206 007314 013737 177562 007170          MOV   TK8, HLD      ;MOV DATA TO LOC. HLD
1207 007322 000201          RTS   R1
1208          I
1209          I 15 MILLI-SEC LOOP
1210          I
1211 007324 012737 001750 010426 WAITI MOV   01750, TIM1
1212 007332 005337 010426          DEC   TIM1
1213 007336 001375          BNE   ,=4
1214 007340 000202          RTS   R2
1215          I
1216          IWAIT 9 MILLI SEC.
1217          I
1218 007342 013737 007360 010426 WAITXI MOV   SPEED, TIM1    ;LOAD FOR 9 MILLI SEC
1219 007350 005337 010426          DEC   TIM1
1220 007354 001375          BNE   ,=4
1221 007356 000202          RTS   R2
1222 007360 177777          SPEEDI 177777      ; 15 MILLI SEC CONST?
1223          I
  
```



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1224 |
1225 | RETURN FROM SHORT LOOP & WARNING INTERRUPTS
1226 |
1227 007362 012706 000600 WAOGI MOV @STACK,SP ;FORCE INTERRUPT RETURN OF SHORTLOOP & WARNING
1228 007366 010407 MOV R4,PC
1229 007370 000000 HLT ;SHOULD NEVER GET HERE
1230 |
1231 | RETURN FROM RECIEVE FLAG INTERRUPTS
1232 007372 012706 000600 RECFI MOV @STACK,SP
1233 007376 010507 MOV R5,PC ;FORCE INT RET OF REC
1234 007400 000000 HLT
1235 |
1236 |
1237 |
1238 |
1239 |
1240 | CHECK FOR COMMANDS TO MONITOR
1241 | TEST REQUIRED
1242 |
1243 |
1244 007402 032737 000001 177570 CHECKI BIT @1,SR
1245 007410 001001 BNE ,+4
1246 007412 000201 RTS R1
1247 007414 012777 000003 171056 MOV @3,@XCSR
1248 007422 004237 010410 JSR @2,@OUT1
1249 007426 000005 RESET
1250 007430 005777 171046 TST @XCINT ;CLEAR FLAGS
1251 007434 000137 007060 JMP HEADER
1252 |
1253 |
1254 |
1255 |
1256 | WHEN VECTORS 170 & 174 ARE INCORRECTLY ASSERTED
1257 | ENTER ROUTINE, REPORT ERROR AND RETURN TO FAILING TEST
1258 |
1259 |
1260 007440 012737 011241 007304 WRNGI MOV @WRONG,MES
1261 007446 004337 007210 JSR @3,PRINT
1262 007452 005726 TST (SP)+
1263 007454 012776 000340 000020 MOV @340,@(SP) ;SET RETURN STATUS TO 7
1264 007462 005746 TST -(SP)
1265 007464 000002 RTI ;RETURN TO FAILING TEST
1266 |
1267 | BUSS TIME-OUT ERROR SUBROUTINE
1268 |
1269 |
1270 007466 004537 010520 TOBEI JSR @5,ERROR
1271 007472 012737 011207 007304 MOV @TOER,MES ;REPORT TIME OUT ERROR
1272 007500 004337 007210 JSR @3,PRINT
1273 007504 000240 NOP
1274 007506 000002 RTI
1275 |
1276 |
1277 | SUBROUTINE FOR INPUTTING ADDRESSES AND VECTORS

```

63

1278						I			
1279						I			
1280	007510	012737	011576	007304	ADDMOI	MOV	#ASK1, MES		:ASK FOR "FIRST DEVICE ADD"
1281	007516	004337	007210			JSR	R3, PRINT		
1282	007522	005037	010334			CLR	ADDRS		
1283	007526	004137	007306		MODI	JSR	R1, REC		:REC A CHARACTER
1284	007532	004337	007172			JSR	R3, ECHO		
1285	007536	022737	000215	007170		CHP	#215, HLD		:TEST FOR A C.R.
1286	007544	001416				BEO	SET		
1287	007546	006337	010334			ASL	ADDRS		
1288	007552	006337	010334			ASL	ADDRS		
1289	007556	006337	010334			ASL	ADDRS		
1290	007562	042737	177770	007170		BIC	#177770, HLD		
1291	007570	063737	007170	010334		ADD	HLD, ADDR		
1292	007576	000137	007526			JMP	#0		
1293	007602	005737	010334		SEYI	TSY	ADDRS		
1294	007606	001425				BEO	STRB		
1295	007610	013737	010334	002500		MOV	ADDRS, XCSR		:SET DEVICE ADDRESS
1296	007616	062737	000002	010334		ADD	#2, ADDR		
1297	007624	013737	010334	002502		MOV	ADDRS, XCINT		
1298	007632	062737	000002	010334		ADD	#2, ADDR		
1299	007640	013737	010334	002504		MOV	ADDRS, XECSR		
1300	007646	062737	000002	010334		ADD	#2, ADDR		
1301	007654	013737	010334	000505		MOV	ADDRS, XSHBU		
1302	007662	000240			STRBI	NOP			
1303	007664	012737	011625	007304		MOV	#ASK2, MES		:ASK FIRST INT. VECTOR
1304	007672	004337	007210			JSR	R3, PRINT		
1305	007676	005037	010336			CLR	VADDR		:CLR VECTOR ADDRESS
1306	007702	004137	007306		MODAI	JSR	R1, REC		
1307	007706	004337	007172			JSR	R3, ECHO		
1308	007712	022737	000215	007170		CHP	#215, HLD		:TEST FOR C.R.
1309	007720	001416				BEO	SETA		
1310	007722	006337	010336			ASL	VADDR		
1311	007726	006337	010336			ASL	VADDR		
1312	007732	006337	010336			ASL	VADDR		
1313	007736	042737	177770	007170		BIC	#177770, HLD		
1314	007744	063737	007170	010336		ADD	HLD, VADDR		
1315	007752	000137	007702			JMP	#0		
1316	007756	005737	010336		SEYAI	TSY	VADDR		
1317	007762	001430				BEO	STRBA		
1318	007764	042737	177000	010336		BIC	#177000, VADDR		
1319	007772	012777	007362	003336		MOV	#A00, #VADDR		
1320	010000	062737	000002	010336		ADD	#2, VADDR		
1321	010006	012777	000340	003322		MOV	#340, #VADDR		
1322	010014	062737	000002	010336		ADD	#2, VADDR		
1323	010022	012777	067372	003306		MOV	#REC, #VADDR		
1324	010030	062737	000002	010336		ADD	#2, VADDR		
1325	010036	012777	000340	002272		MOV	#340, #VADDR		
1326	010044	012737	011651	007304	STRBAI	MOV	#ASK3, MES		:ASK FOR VECTOR LEVEL
1327	010052	004337	007210			JSR	R3, PRINT		
1328	010056	004137	007306			JSR	R1, REC		:REC ONE CHARACTERS
1329	010062	004337	007172			JSR	R3, ECHO		
1330	010066	022737	000215	007170		CHP	#215, HLD		
1331	010074	001407				BEO	, +20		

A3

1332	010076	022737	000264	007170		CMP	0264,HL0		;CHECK FOR A 4
1333	010104	001004				BNE	,+12		
1334	010106	012737	000140	003510		MOV	0140,PRIV		;SET PRIORITY AT 3
1335	010114	000437				BR	PROTIM		
1336	010116	022737	000265	007170		CMP	0265,HL0		
1337	010124	001004				BNE	,+12		
1338	010126	012737	000200	003510		MOV	0200,PRIV		
1339	010134	000427				BR	PROTIM		
1340	010136	022737	000266	007170		CMP	0266,HL0		
1341	010144	001004				BNE	,+12		
1342	010146	012737	000240	003510		MOV	0240,PRIV		
1343	010154	000417				BR	PROTIM		
1344	010156	022737	000267	007170		CMP	0267,HL0		
1345	010164	001004				BNE	,+12		
1346	010166	012737	000300	003510		MOV	0300,PRIV		
1347	010174	000407				BR	PROTIM		
1348	010176	012737	011402	007304		MOV	00J,YES		
1349	010204	004337	007210			JSR	R3,PRINT		
1350	010210	000137	010044			JMP	STRBA		;TRY AGAIN
1351	010214	012737	011677	007304	PROTIM	MOV	0ASK4,YES		
1352	010222	004337	007210			JSR	R3,PRINT		
1353	010226	004137	007306			JSR	R1,REC		
1354	010232	004337	007172			JSR	R3,ECHO		
1355	010236	022737	000301	007170		CMP	0301,HL0		
1356	010244	001004				BNE	,+12		
1357	010246	012737	001500	007360		MOV	01500,SPEED		
1358	010254	000417				BR	KA		
1359	010256	022737	000302	007170		CMP	0302,HL0		
1360	010264	001004				BNE	,+12		
1361	010266	012737	003000	007360		MOV	03000,SPEED		
1362	010274	000407				BR	KA		
1363	010276	022737	000303	007170		CMP	0303,HL0		
1364	010304	001004				BNE	,+12		
1365	010306	012737	006000	007360	KA	MOV	06000,SPEED		
1366	010314	000205				RTS	R5		
1367	010316	012737	011402	007304		MOV	00J,YES		
1368	010324	004337	007210			JSR	R3,PRINT		
1369	010330	000137	010214			JMP	PROTIM		
1370									
1371									
1372	010334	000000			ADDRESS	0			
1373	010336	000000			VADDRESS	0			

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1375
1376 010340 012706 000000          TIMEXI  MOV      #STACK,SP      ;REINITIALIZE THE STACK
1377 010344 011407                    MOV      (R4),PC        ;FORCE RETURN FROM INTERRUPT
1378 010346 000000                    HLT                          ;SHOULD NEVER GET HERE
1379
1380
1381                    ;RUN DELAY TIME OUTS,TOTAL TIME AS PER
1382                    ;PROCESSOR TIME 05=4SEC,+ 40=3 SEC+
1383
1384 010350 105737 177570          TOUTI  TSTB      SR
1385 010354 000415                    BR       TOUT1           ;CHANGE TO BPL TO RUN A FAST MODE FOR
1386 010356 012737 000012 010424    MOV      #12,CNTIM      ;T1,T2,T3<90 MILLI-SEC
1387 010364 013737 007360 010426    RA:    MOV      SPEED,TIMI ;90 MILLI SEC. WORTH
1388 010372 005337 010426                    DEC      TIMI
1389 010376 001375                    BNE     ,=4
1390 010400 005337 010424                    DEC      CNTIM
1391 010404 001367                    BNE     RA
1392 010406 000202                    RTS      R2              ;GO WHEN DONE
1393
1394 010410 012737 000005 010426    TOUT1: MOV      #5,TIMI      ;RUN LONG TIME OUT FOR ALL DELAYS WERE
1395 010416 004437 010572                    JSR     R4,TIME         ;SET COUNT TIME
1396 010422 000202                    RTS      R2
1397 010424 000000          CNTIMI 0
1398 010426 000000          TIMI1  0
1399
1400
1401 010430 000240          NULPRTI NOP
1402 010432 105737 177564          TSTB     TYSR
1403 010436 100375                    BPL     ,=4
1404 010440 005037 177566          CLR      TYDB
1405 010444 105737 177564          TSTB     TYSR
1406 010450 100375                    BPL     ,=4
1407 010452 005037 177566          CLR      TYDB
1408 010456 105737 177564          TSTB     TYSR
1409 010462 100375                    BPL     ,=4
1410 010464 000002          RTI
1411
1412
1413 010466 012737 000215 177566    LFCRI  MOV      #215,TYDB     ;CARRIAGE RET.
1414 010474 105737 177564          TSTB     TYSR
1415 010500 100375                    BPL     ,=4
1416 010502 012737 000212 177566    MOV      #212,TYDB
1417 010510 105737 177564          TSTB     TYSR
1418 010514 100375                    BPL     ,=4
1419 010516 000202                    RTS      R2
1420
1421
1422
1423                    ;CHECK FOR ERROR PRINT OUT (BIT 13 OF SWITCH REG.)
1424 010520 032737 020000 177570    ERRORI BIT      #20000,SR
1425 010526 001402                    BEQ     ,=6             ;IF BIT 13=0 PRINT ERROR
1426 010530 062705 000012          ADD      #12,R5         ;ADD VALUE TO OMIT ERROR PRINT
1427 010534 000205                    RTS      R5
1428

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1429                                     ;CHECK FOR SCOPE LOOP (BIT 14 OF SWITCH REG.)
1430 010536 013737 177570 010566 SCOPEI MOV SR,ESTAT
1431 010544 032737 040000 010566 BIT 0040000,ESTAT ;TEST BIT 14 OF SWITCH REGISTER
1432 010552 001404 BEQ ,+12 ;IF BIT 14=1 RUN SCOPE
1433 010554 012706 000600 MOV @STACK,SP
1434 010560 013707 010570 MOV LOOP,PC ;FORCE RETURN TO TEST
1435 010564 000205 RTS R5 ;RETURN AND WLT
1436 010566 000000 ESTATI 0
1437 010570 000000 LOOPI 0
1438                                     ;
1439                                     ;RUN TIME INCREMENTS IN VALUES STORED IN TIMEI
1440 010572 005037 010614 TIMEI CLR YES
1441 010576 005237 010614 INC YES ;COUNT LOOP
1442 010602 001375 BNE ,+4 ;
1443 010604 005337 010426 DEC TIMEI ;NUMBER OF COUNT LOOPS
1444 010610 001372 BNE ,+12
1445 010612 000204 RTS R4
1446 010614 000000 XESI 0
1447                                     ;MESSAGES
1448 010616 000 BYTE
1449 010617 045 047514 044507 LYI .ASCII /XLOGIC TESTX0/
010624 020103 042524 052123
010632 040045
1450 010634 030524 040045 EE1I .ASCII /T1X0/
1451
1452 010640 031124 040045 EE2I .ASCII /T2X0/
1453
1454 010644 031524 040045 EE3I .ASCII /T3X0/
1455
1456 010650 032124 040045 EE4I .ASCII /T4X0/
1457
1458 010654 032524 040045 EE5I .ASCII /T5X0/
1459
1460 010660 033124 040045 EE6I .ASCII /T6X0/
1461
1462 010664 033524 040045 EE7I .ASCII /T7X0/
1463
1464 010670 034124 040045 EE8I .ASCII /T8X0/
1465
1466 010674 034524 040045 EE9I .ASCII /T9X0/
1467
1468 010700 030524 022460 100 EE10I .ASCII /T10X0/
1469
1470 010705 124 030461 040045 EE11I .ASCII /T11X0/
1471
1472 010712 030524 022462 100 EE12I .ASCII /T12X0/
1473
1474 010717 124 031461 040045 EE13I .ASCII /T13X0/
1475
1476 010724 030524 022464 100 EE14I .ASCII /T14X0/
1477
1478 010731 124 032461 040045 EE15I .ASCII /T15X0/
1479
1480 010736 030524 022466 100 EE16I .ASCII /T16X0/

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1481							
1482	010743	124	033461	040045	EE171	.ASCII	/T17X0/
1483							
1484	010750	030524	022470	100	EE181	.ASCII	/T18X0/
1485							
1486	010755	124	034461	040045	EE191	.ASCII	/T19X0/
1487							
1488	010762	031124	022460	100	EE201	.ASCII	/T20X0/
1489							
1490	010767	124	030462	040045	EE211	.ASCII	/T21X0/
1491							
1492	010774	031124	022462	100	EE221	.ASCII	/T22X0/
1493							
1494	011001	124	031462	040045	EE231	.ASCII	/T23X0/
1495							
1496	011006	031124	022464	100	EE241	.ASCII	/T24X0/
1497							
1498	011013	124	032462	040045	EE251	.ASCII	/T25X0/
1499							
1500	011020	031124	022466	100	EE261	.ASCII	/T26X0/
1501							
1502	011025	124	033462	040045	EE271	.ASCII	/T27X0/
1503							
1504	011032	031124	022470	100	EE281	.ASCII	/T28X0/
1505							
1506	011037	124	034462	040045	EE291	.ASCII	/T29X0/
1507							
1508	011044	031524	022460	100	EE301	.ASCII	/T30X0/
1509							
1510	011051	124	030463	040045	EE311	.ASCII	/T31X0/
1511							
1512	011056	031524	022462	100	EE321	.ASCII	/T32X0/
1513							
1514	011063	124	031463	040045	EE331	.ASCII	/T33X0/
1515							
1516	011070	031524	022464	100	EE341	.ASCII	/T34X0/
1517							
1518	011075	124	032463	040045	EE351	.ASCII	/T35X0/
1519							
1520	011102	031524	022466	100	EE361	.ASCII	/T36X0/
1521							
1522	011107	124	033463	040045	EE371	.ASCII	/T37X0/
1523							
1524	011114	031524	022470	100	EE381	.ASCII	/T38X0/
1525							
1526	011121	124	034463	040045	EE391	.ASCII	/T39X0/
1527							
1528	011126	032124	022460	100	EE401	.ASCII	/T40X0/
1529							
1530	011133	124	030464	040045	EE411	.ASCII	/T41X0/
1531							
1532	011140	032124	022462	100	EE421	.ASCII	/T42X0/
1533							
1534	011145	124	031464	040045	EE431	.ASCII	/T43X0/

1535							
1536	011152	032124	022464	100	EE44I	.ASCII	/T44X0/
1537							
1538	011157	124	034063	022523	EE38SI	.ASCII	/T38SX0/
	011164	100					
1539							
1540	011165	124	030064	022523	EE40SI	.ASCII	/T40SX0/
	011172	100					
1541							
1542	011173	124	030464	022523	EE41SI	.ASCII	/T41SX0/
	011200	100					
1543							
1544	011201	124	030464	022523	EE43SI	.ASCII	/T41SX0/
	011206	100					
1545							
1546	011207	102	051525	042440	TOERI	.ASCII	/BUS ERROR TIME-OUTX0/
	011214	051122	051117	052040			
	011222	046511	026505	052517			
	011230	022524	100				
1547							
1548	011233	120	051501	022523	PASSI	.ASCII	/PASSX0/
	011240	100					
1549							
1550	011241	124	040522	050120	WRONGI	.ASCII	/TRAPPED TO WRONG INT. VECTORX0/
	011246	042105	052040	020117			
	011254	051127	047117	020107			
	011262	047111	027124	053040			
	011270	041505	047524	022522			
	011276	100					
1551							
1552	011277	045	042504	040514	DELTSTI	.ASCII	/XDELAY ADJUSTMENT TESTX0/
	011304	020131	042101	052512			
	011312	052123	042515	050116			
	011320	052040	051505	022524			
	011326	100					
1553							
1554	011327	104	046105	054501	ASRI	.ASCII	/DELAY:(1)WATCHDOG,(2)WARNING & SHORT LOOPX0/
	011334	024072	024461	040527			
	011342	041524	042110	043517			
	011350	024056	024462	040527			
	011356	047122	047111	020107			
	011364	020046	044123	051117			
	011372	020124	047514	050117			
	011400	040045					
1555							
1556	011402	022477	100		QUI	.ASCII	/?X0/
1557							
1558	011405	045	047514	044507	HEADI	.ASCII	/XLOGIC TEST(1),DELAY TEST(2),DYNAMIC TEST(3)X0/
	011412	020103	042524	052123			
	011420	030450	026051	042504			
	011426	040514	020131	042524			
	011434	052123	031050	026051			
	011442	054504	040516	044515			
	011450	020103	042524	052123			


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1559 011456 031450 222451 100
1560 011463 045 054524 040516 DYSTI .ASCII /XDYNAMIC TESTX0/
      011470 044515 020103 042524
      011476 052123 040045
1561 011502 044123 051117 020124 SLPI .ASCII /SHORT LOOP FLAG SETX0/
1562 011510 047514 050117 043040
      011516 040514 020107 042523
      011524 022524 100
1563 011527 111 040114 043505 IINTI .ASCII /ILLEGAL INTERRUPTX0/
1564 011534 046101 044440 052116
      011542 051105 052522 052120
      011550 040045
1565 011552 054105 027124 052502 RBSI .ASCII /EXT.BUS STATUS BADX0/
1566 011560 020123 052123 052101
      011566 051525 041040 042101
      011574 040045
1567 011576 043045 051111 052123 ASK1I .ASCII /XFIRST DEVICE ADDRESS=0/
1568 011604 042040 053105 041511
      011612 020105 042101 051104
      011620 051505 036523 100
1569 011625 045 044506 051522 ASK2I .ASCII /XFIRST INT. VECTOR=0/
1570 011632 020124 047111 027124
      011640 053040 041505 047524
      011646 036522 100
1571 011651 045 051120 047511 ASK3I .ASCII /XPRIORITY INT. LEVEL=0/
1572 011656 044522 054524 044440
      011664 052116 020056 042514
      011672 042526 036514 100
1573 011677 045 042120 020520 ASK4I .ASCII /XPD=11 (A)=05,10,20 (B)=35,40 (C)=45,50 0/
      011704 030461 024040 024501
      011712 030075 026065 030061
      011720 031054 020060 041050
      011726 036451 032463 032054
      011734 020060 041450 036451
      011742 032464 032454 020060
      011750 100
1574
1575 011752 .EVEN
1576 000001 .END

```

A4

AA1	001322	AA2	001432	AA4	003446	AA5	003626
ADDMD	007510	ADDRES	010334	ASK	011327	ASK1	011576
ASK2	011625	ASK3	011691	ASK4	011677	BBS	011592
CHECK	007402	CINT	= 172402	CLST	006676	CNTIM	010424
COUNT	007054	CSR	= 172400	DBUF	007302	DELAY	006220
DELTST	011277	DONE	007276	DYMAN	006436	DYTSY	011463
DYX	006494	D1	006326	D2	006374	ECHO	007172
ECSR	= 172404	EE1	010634	EE10	010700	EE11	010705
EE12	010712	EE13	010717	EE14	010724	EE15	010731
EE16	010736	EE17	010743	EE18	010750	EE19	010755
EE2	010640	EE20	010762	EE21	010767	EE22	010794
EE23	011001	EE24	011006	EE25	011013	EE26	011020
EE27	011029	EE28	011032	EE29	011037	EE3	010644
EE30	011044	EE31	011091	EE32	011056	EE33	011063
EE34	011070	EE35	011075	EE36	011102	EE37	011107
EE38	011114	EE38S	011197	EE39	011121	EE4	010650
EE40	011126	EE40S	011165	EE41	011133	EE41S	011173
EE42	011140	EE43	011145	EE43S	011201	EE44	011192
EE5	010654	EE6	010660	EE7	010664	EE8	010670
EE9	010674	ERR	007020	ERROR	010520	ESTAT	010566
HEAD	011405	HEADER	007000	HERE	006534	HLD	007170
HL7	= 000000	HORN	006502	IINT	011527	INIT	006090
KA	010314	LFCR	010406	LOGIC	001000	LOOP	010570
LREP	006246	LY	010617	MES	007304	MOD	007526
MODA	007702	NOP	= 000240	NULL	= 104000	NULPRT	010430
OKK	006614	OPP	006100	OUT	007252	PASS	011233
PC	=X000007	PPL	005724	PRINT	007210	PRIV	000510
PROTIM	010214	PRT	007260	PS	= 177776	PT	006512
PTR	004226	PTX1	004506	PTX2	004624	PTX3	004732
QU	011402	RA	010364	REC	007306	RECF	007372
R0	=X000000	R1	=X000001	R2	=X000002	R3	=X000003
R4	=X000004	R5	=X000005	SCOPE	010536	SET	007602
SEYA	007756	SIRE	007056	SLF	011502	SP	=X000006
SPEED	007360	SR	= 177570	STACK	000600	STRB	007662
STRBA	010044	SWBU	= 172406	TA	007154	T0	007160
TC	007164	TEST	001016	THW	002474	TIKE	006742
TILT	005006	TIME	010572	TIMEX	010340	TIMI	010426
TK0	= 177562	TKS	= 177560	TOBE	007466	TOER	011207
TOUT	010350	TOUT1	010410	TYDB	= 177566	TYSR	= 177564
T1	001030	T10	001792	T11	002036	T12	002112
T13	002172	T14	002270	T15	002332	T16	002410
T17	002526	T18	002560	T19	002622	T2	001110
T20	002664	T21	002730	T22	003026	T23	003114
T24	003212	T25	003330	T26	003470	T27	003644
T28	003752	T29	004092	T3	001170	T30	004120
T31	004244	T32	004326	T33	004414	T34	004520
T35	004642	T36	004744	T37	005040	T38	005126
T39	005232	T4	001246	T40	005322	T41	005424
T42	005534	T43	005624	T44	005726	T5	001392
T6	001462	T7	001534	T8	001616	T9	001706
VADDR	010336	WAIT	007324	WAITX	007342	WAOG	007362
WRNG	007440	WRONG	011241	XCINT	000502	XCSR	000500
XCSR	000504	XES	010614	XSWBU	000500	.	= 011752

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WATCH, SRC SYMBOL TABLE

ERRORS DETECTED: 0

WATCH, WATCH, WATCH, SRC
RUN-TIME: 4 9 0 SECONDS
CORE USED: 4K

C4