

DQ11

INTERRUPT LOGIC TEST
MD-11-DZDQC-C

EP-DZDQC-C-DL-A

NOV 1976

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDQC-C-D
PRODUCT NAME: DQ11 INTERRUPT LOGIC TESTS
DATE: 21 JUNE 1976
MAINTAINER: DIAGNOSTIC GROUP

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1. ABSTRACT

THE FUNCTION OF THE DQ11 DIAGNOSTICS ARE TO VERIFY THAT THE OPTION OPERATES ACCORDING TO SPECIFICATIONS.

THIS TEST CHECKS ALL POSSIBLE INTERRUPTS VERIFYING THAT AN INTERRUPT OCCURS WHEN IT SHOULD AND THAT ONE DOESN'T HAPPEN WHEN IT SHOULDN'T.
ALSO THAT THE INTERRUPTS OCCUR TO THE CORRECT VECTOR.
BASIC NPR FUNCTIONS ARE ALSO INCLUDED IN THIS TEST.

CURRENTLY THERE ARE SEVEN OFF LINE DIAGNOSTICS THAT ARE TO BE RUN IN SEQUENCE TO INSURE THAT IF AN ERROR SHOULD OCCUR IT WILL BE DETECTED AT AN EARLY STAGE AND INSURING THAT DIAGNOSIS OF ERROR WILL BE IMMEDIATE TO PROBLEM.
NOTE: ADDITIONAL DIAGNOSTICS MAY BE ADDED IN THE FUTURE.

THE SEVEN DIAGNOSTICS ARE:

1. DZDQA [REV] BASIS R/W TEST #1
2. DZDQB [REV] BASIS R/W TEST #2
3. DZDQC [REV] BASIC NPR AND INTERRUPT TEST
4. DZDQD [REV] RECEIVER TRANSMITTER EXERCISER TEST
5. DZDQE [REV] MISC. RX AND TX TESTS. PLUS BCC TESTS.
6. DZDQF [REV] CHARACTER DETECT TESTS.
7. DZDQH [REV] CHARACTER LENGTH AND INTERRUPT TESTS.

THERE IS ALSO AN ONLINE TEST TO BE DISCUSSED LATER.

1. DZDQG [REV] ONLINE TEST. (ITEP OVERLAY)

AND A PARAMETER INPUT PROGRAM IS AVAILABLE

1. DZDQG [REV] DQ11 TRIAL PROGRAM (PARAMETER INPUT)

2. REQUIREMENTS

2.1 EQUIPMENT

ANY PDP11 FAMILY CPU (WITH MINIMUM 4K MEMORY)-WITH
OR WITHOUT A HARDWARE SWITCH REGISTER (LOC. 177570)
ASR 33 (OR EQUIVALENT)
DQ11
SYNC MODEM (ONLY REQUIRED FOR ONLINE TEST)

2.2 STORAGE

PROGRAM WILL LOAD AND RUN
IN 4K OF MEMORY.

LOCATION 1400 THRU 1600 ARE ESPECIALLY TO BE NOTED AND TO BE UNTOUCHED BY OPERATOR AFTER DQ11 TRIAL PROGRAM HAS BEEN EXECUTED. OR AFTER THE "AUTO SIZING" HAS BEEN DONE.

3. LOADING PROCEEDURE

3.1 METHOD

ALL PROGRAMS ARE IN ABSOLUTE FORMAT AND ARE LOADED USING THE ABSOLUTE LOADER.

ABSOLUTE LOADER STARTING ADDRESS *500

MEMORY *
SIZE

4K	17
8K	37
12K	57
16K	77
20K	117
24K	137
28K	157

3.1.1 LOAD THE ADDRESS OF ABS. LOADER (LOC.XXX500)

3.1.2 THEN START

4. STARTING PROCEEDURE

A. LOAD LOC. 200

B. SET SWR TO ZERO FOR "AUTO SIZING" OR LEAVE
LEAVE SWR BIT 7=1 TO USE EXISTING PARAMETERS SET UP
BY DQ11 TRIAL PROGRAM OR A PREVIOUSLY RUN DQ11 DIAGNOSTIC
THAT USED THE "AUTO SIZING".
****REFER TO SECTION 4.1 FOR SOFTWARE SWITCH REGISTER OPERATION
AND OPTIONS.****

NOTE: THE SOFTWARE SWITCH REGISTER IS LOCATED AT LOC.176
SOFTWARE DISPLAY REGISTER IS LOCATED AT LOC.174

C. THEN START

THE PROGRAM WILL TYPE MAINDEC NAME AND PROGRAM NAME
IF THIS WAS THE FIRST START UP OF THE PROGRAM) AND ALSO
THE FOLLOWING:

"MAP OF DQ11 STATUS"
1400 160010
1402 152300
1404 160020
1406 150310

THE ABOVE IS ONLY AN EXAMPLE!

THIS WOULD INDICATE THE STATUS TABLE STARTING AT ADD.
1400 IN THE PROGRAM. THE STATUS TABLE MUST BE VERIFIED BY THE
USER IF AUTO SIZING IS DONE. FOR INFORMATION OF STATUS
TABLE SEE SECTION 8.4 FOR HELP.

****IF THE SOFTWARE SWITCH REGISTER IS SELECTED THEN THE FOLLOWING
WILL BE TYPED AFTER THE PROGRAM IDENTIFIES ITSELF:
SWR=XXXXXX NEW= (REFER TO SECTION 4.1 FOR OPERATOR'S OPTION)****
NOTE: IF USING THE SOFTWARE SWITCH REGISTER WHEN A HARDWARE
SWITCH REGISTER IS AVAILABLE THE PROGRAM WILL NOT
TYPE OUT THE TITLE.

THE PROGRAM WILL TYPE "R"
AND PROCEED TO RUN THE DIAGNOSTIC

4.1 CONTROL SWITCH SETTINGS

IF THE DIAGNOSTIC IS RUN ON A CPU WITHOUT A SWITCH
REGISTER THEN A SOFTWARE SWITCH REGISTER IS USED WHICH ALLOWS
THE USER THE SAME SWITCH OPTIONS AS THE HARDWARE SWITCH REGISTER.
IF THE HARDWARE SWITCH REGISTER DOES NOT EXIST OR IF ONE DOES
AND IT CONTAINS ALL ONES (177777) THEN THE SOFTWARE SWITCH
REGISTER (LOC. 176) IS USED.

CONTROL:

THIS PROGRAM ALSO SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH
REGISTER (LOC. 176) FROM THE TTY. THIS CAN BE ACCOMPLISHED BY
DOING THE FOLLOWING:

- 1) TYPE CONTROL G (<↑G>); THIS WILL ALLOW THE TTY TO ENTER DATA INTO
LOC. 176 AT SELECTED POINTS WITHIN THE PROGRAM.
- 2) THE MACHINE WILL THEN TYPE: SWR=XXXXXXNEW= (XXXXXX IS THE OCTAL CONTENTS
OF THE SOFTWARE SWITCH REGISTER.)
- 3) AFTER THE "NEW=" HAS BEEN TYPED THEN THE OPERATOR CAN DO ONE
OF THE FOLLOWING AT THE TTY:
 - A) TYPE A NUMBER TO BE LOADED INTO LOC. 176 FOLLOWED BY A <CR>.
(ONLY NUMBERS BETWEEN 0-7 WILL BE ACCEPTED AND ONLY 6 NUMBERS
WILL BE ALLOWED)
IF A <CR> IS THE FIRST KEY DEPRESSED THE SOFTWARE SWITCH
REGISTER CONTENTS WILL NOT BE CHANGED.
 - B) IF A CONTROL U (<↑U>) IS DEPRESSED THEN THE PROGRAM WILL SEND YOU
BACK TO STEP 2.

SW 15	SET: HALT ON ERROR
SW 14	SET: LOOP ON CURRENT TEST
SW 13	SET: INHIBIT ERROR PRINT OUT
SW 12	SET: INHIBIT TYPE OUT/BELL ON ERROR.
SW 11	SET: INHIBIT ITERATIONS

SW 10 SET: ESCAPE TO NEXT TEST
 SW 09 SET: LOOP WITH CURRENT DATA
 SW 08 SET: CATCH ERROR AND LOOP ON IT
 SW 07 SET: USE PREVIOUS STATUS TABLE. CLR-DO AUTO SIZE.
 SW 06 SET:
 SW 05 SET:
 SW 04 SET:
 SW 03 SET:
 SW 02 SET: LOCK ON SELECTED TEST
 SW 01 SET: RESTART PROGRAM AT SELECTED TEST
 SW 00 SET: RESELECT DQ11'S DESIRED ACTIVE.

4.1.2 SWITCH REGISTER RESTRICTIONS

SW 00 RESELECT DQ11'S DESIRED ACTIVE.
 PLEASE NOTE THAT A MESSAGE IS TYPED
 OUT FOR SWITCH REGISTER BEING EQUAL TO DQ11'S
 ACTIVE. THIS MEANS IF THE SYSTEM HAS
 FOUR DQ11S; BITS 00,01,02,03 WILL
 BE SET IN LOC "DQACTV". USING THIS
 SWITCH ALTERS THAT LOCATION; THEREFORE
 IF FOUR DQ11S ARE IN THE SYSTEM
 DO NOT SET SWITCHS GREATER THAN
 SW 03 IN THE UP POSITION. THIS WOULD BE
 A FATAL ERROR. DO NOT SELECT MORE ACTIVE
 DQ11S THAN HAS BEEN GIVEN INFORMATION
 ABOUT IN TRIAL PROGRAM.

METHOD: A: LOAD ADDRESS 200
 B: START WITH SW 00=1
 C: PROGRAM WILL TYPE MESSAGE
 D: CONTINUE THE BINARY NUMBER OF DQ11S DESIRED ACTIVE
 EXAMPLE: 1=1 DQ11; 3=2 DQ11; 7=3 DQ11; 17=4 DQ11 37=5 DQ11 ETC.
 E: NUMBER (IF VALID) WILL BE IN DATA LIGHTS (EXCLUDING 11/05, 11/04, 11/34)
 F: CONTINUE WITH ANY OTHER SWITCH SETTINGS DESIRED.

SW 01 IT IS STRONGLY SUGGESTED THAT
 AT LEAST ONE PASS HAS BEEN MADE
 BEFORE TRYING TO SELECT A TEST
 THAT IS NOT IN THE ORDER OF SEQUENCE
 THE REASON BEING IS THAT THE
 PROGRAM HAS TO CLEAR AREAS AND SET
 UP PARAMETERS. ALSO WHEN A TEST IS
 SELECTED ALWAYS START AT THE VERY
 BEGINNING OF THAT TEST.

SW 09 LOOP ON CURRENT DATA:
 THIS SWITCH WILL ONLY WORK IF
 CALL "SCOPI" IS IN THAT TEST.
 THE REASON BEING THAT MOST TESTS
 DEAL WITH BLOCKS OF DIFFERENT DATA
 TO BE SENT OR RECEIVED ALL AT ONCE
 THUS IN BLOCK DATA; ONE PATTERN CANN'T BE SINGLED OUT.

4.1.3 SWITCH REGISTER PRIORITYS

ERROR SWITCHES

1. SW 12 DELETE PRINT OUT/BELL ON ERROR.
2. SW 13 DELETE ERROR PRINTOUT.
3. SW 15 HALT ON THE ERROR.
4. SW 08 GOTO BEGINNING OF THE TEST.
5. SW 10 GOTO NEXT TEST ON ERROR.

****HLT (ERROR) ROUTINE SUPPORTS <↑G> OPERATION****

SCOPE SWITCHES

1. SW 09 (IF ENABLED BY "SCOPI")
2. SW 14
3. SW 11

****SCOPE ROUTINE WILL SUPPORT <↑G> OPERATION****

4.2 STARTING ADDRESS

STARTING ADDRESS IS AT 000200
THERE ARE NO OTHER STARTING ADDRESSES
FOR THE DQ11 DIAGNOSTICS PREVIOUSLY MENTIONED

NOTE: IF ADDRESS 000042 IS NON-ZERO
THE PROGRAM ASSUMES IT IS UNDER
ACT11 OR DDP CONTROL AND WILL ACT ACCORDINGLY
AFTER *ALL* AVAILABLE DQ11'S ARE TESTED
THE PROGRAM WILL RETURN TO "DDP2" OR "ACT-11".

5. OPERATING PROCEDURE

WHEN PROGRAM IS INITIALLY STARTED MESSAGES AS DESCRIBED IN SECTION
FOUR WILL BE PRINTED.

AND PROGRAM WILL BEGIN RUNNING THE
DIAGNOSTIC

5.2 PROGRAM AND/OR OPERATOR ACTION

THE TYPICAL APPROACH SHOULD BE

1. HALT ON ERROR (VIA SW 15=1)
WHEN EVER AN ERROR OCCURS
2. CLEAR SW 15
3. SET SW 14: (LOOP ON THIS TEST)
4. SET SW 13: (INHIBIT ERROR PRINT OUT)

THE TEST NUMBER AND PC WILL BE TYPED OUT AND
POSSIBLY AN ERROR MESSAGE (THIS DEPENDS ON THE TEST)
TO GIVE THE OPERATOR AN IDEA AS TO THE SOURCE OF THE
PROBLEM. IF IT IS NECESSARY TO KNOW MORE INFORMATION
CONCERNING THE ERROR REPORT; LOOK IN THE LISTING
FOR THAT TEST NUMBER WHICH WAS TYPED OUT
AND THEN NOTE THE PC OF THE ERROR REPORT
THIS WAY THE EXACT FUNCTIONING OF THE TEST

CAN BE INTERPEDITED

6. ERRORS

AS DESCRIBED PREVIOUSLY THERE WILL ALWAYS BE A TEST NUMBER AND PC TYPED OUT AT THE TIME OF AN ERROR (PROVIDING SW 13=0 AND SW 12=0). IN MOST CASES ADDITIONAL INFORMATION WILL BE SUPPLIED THE THE ERROR MESSAGE WHICH IS TO GIVE THE OPERATOR AN INDICATION OF THE ERROR.

6.2 ERROR RECOVERY

IF FOR SOME REASON THE DQ11 SHOULD "HANG THE BUS" (GAIN CONTROL OF BUS SO THAT CONSOLE MANUAL FUNCTIONS ARE INHIBITED) AN INIT OR POWER DOWN/UP IS NECESSARY FOR OPERATOR TO REGAIN CONTROL OF CPU. IF THIS SHOULD HAPPEN; LOOK IN LOCATION "TSTNO" (ADDRESS 1222) FOR THE NUMBER OF THE TEST THAT WAS RUNNING AT THE TIME OF THE CATASTROPHIC ERROR. IN THIS WAY THE OPERATOR WILL HAVE AN IDEA AS TO WHAT THE DQ11 WAS DOING AT THE TIME OF THE ERROR.

6.3 ****HALT RECOVERY WHEN USING SOFTWARE SWITCH REGISTER****

IF THE SOFTWARE SWITCH REGISTER IS TO BE CHANGED AFTER A HALT THE THE OPERATOR IS REQUIRED TO TYPE A <↑G> BEFORE DEPRESSING CONTINUE. THE FOLLOWING WILL BE TYPED:
SWR=XXXXXX NEW= (REFER TO SECTION 4.1 FOR OPERATOR OPTION)

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

SEE SECTION 4. (PLEASE)

7.2 OPERATING RESTRICTIONS

DQ11 TRIAL PROGRAM MUST BE RUN PRIOR TO THE FIRST AND ONLY THE FIRST RUNNING OF ANY DQ11 DIAGNOSTIC
NOTE: IF NO PROGRAM OTHER THAN A DQ11 DIAGNOSTIC WAS LOADED AFTER DQ11 TRIAL OR IF CORE MEMORY HAS NOT BEEN CHANGED; OR IF THERE IS NO DQ11 CONFIGURATION CHANGES; THE DQ11 TRIAL PROGRAM NEED NEVER BE RUN AGAIN. HOWEVER IF ANY OF THE ABOVE HAVE BEEN VIOLATED THE DQ11 TRIAL PROGRAM MUST BE RUN AGAIN BEFORE RUNNING THE DIAGNOSTICS
NOTE: AN ALTERNATIVE TO THE ABOVE IS ATTEMPTING THE "AUTO SIZING" WHEN PROGRAM IS INITIALLY STARTED WITH SW07=0.

8. MISCELLANEOUS

DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 9
 DZDQCC.P11

8.1 EXECUTION TIME

8.2 PASS COMPLETE

WHEN THE DIAGNOSTIC HAS COMPLETED
 A PASS THE FOLLOWING IS AN EXAMPLE
 OF THE PRINT OUT TO BE EXPECTED.

END PASS DZDQC-C CSR: 160000 VEC: 300 PASSES: 000001 ERRORS: 000000

NOTE: THE NUMBERS FOR CSR AND VEC ARE
 NOT NECESSARILY THE VALUES FOR THE DEVICE
 THEY ARE ONLY FOR THIS EXAMPLE.

8.3 TST1 (MINI MONITOR)

THE VERY FIRST "TEST" (TST1)
 IS *NOT* A TEST OF THE DQ11 HARDWARE
 IT IS A MINI-MONITOR USED TO CYCLE DQ11 IN THE
 SYSTEM THROUGH THE DIAGNOSTIC.

REMEMBER: TST1 IS NOT A TEST OF DQ11 HARDWARE!!!!!!!

8.4 KEY LOCATIONS

RETURN (1210) CONTAINS THE ADDRESS WHERE PROGRAM WILL
 RETURN WHEN ITERATION COUNT IS REACHED
 OR IF LOOP ON TEST IS ASSERTED.

NEXT (1212) CONTAINS THE ADDRESS OF THE NEXT TEST
 TO BE PERFORMED.

TSTNO (1222) CONTAINS THE NUMBER OF THE TEST NOW
 BEING PERFORMED.

RUN (1272) THE BIT IN "RUN" ALWAYS POINTS ONE
 PAST THE DQ11 CURRENTLY BEING TESTED.

EXAMPLE:

(RUN) 1272/0000000001000000

MEANS THAT DQ11 NO.05 IS THE DQ11 NOW
 RUNNING.

DQCR00-DQCR17
 DQST00-DQST17
 (1400)-(1476)

THESE LOCATIONS CONTAIN THE INFORMATION
 NEEDED TO TEST UP TO 16 (DECIMAL) DQ11S
 SEQUENTIALY. THEY CONTAIN THE CSR, VECTOR
 AND STATUS CONCERNING THE CONFIGURATION
 OF EACH DQ11.

DQACTV (1500)

EACH BIT SET IN THIS LOCATION INDICATES
 THAT THE ASSOCIATED DQ11 WILL BE TESTED
 IN TURN.

EXAMPLE:

(DQACTV) 1500/000000000000111111

MEANS THAT DQ11 NO. 00,01,02,03,04
 WILL BE TESTED.

EXAMPLE:

(DQACTV) 1500/00000000000010001

MEANS THAT DQ11 NO. 00,04

DQCSR (1506) WILL BE TESTED.
 CONTAINS THE RECEIVER CSR OF THE
 CURRENT DQ11 UNDER TEST.
 DQSTAT (1510) CONTAINS THE STATUS OF THE CURRENT
 DQ11 UNDER TEST.
 BIT 15 SET: TWO SYNC CHARS/ONE SYNC CHAR
 BIT 14 SET: TEST JUMPER INSTALLED/NOT INSTALLED
 BIT 13 SET: BB OPTION INSTALLED/NOT INSTALLED
 BIT 12 SET: BA OPTION INSTALLED/NOT INSTALLED
 BIT 11 SET: ACTIVE ON FIRST NON-SYNC/ACTIVE AFTER NO. OF SYNC
 BIT 10 SET: AB OPTION INSTALLED/NOT INSTALLED
 BIT 09 SET: ODD VRC/EVEN VRC
 BIT 00-08 VECTOR "A" OF DEVICE

8.5 *** METHOD OF AUTO SIZING ***

8.5.1 FINDING THE CONTROL STATUS REGISTER.

WHEN LOOKING FOR THE CSR IT IS NECESSARY TO TAKE CARE
 THAT WHEN A CSR IS FOUND THAT IT IS INDEED A DQ11. THAT
 IS THE METHOD OF MY MADNESS FOR THIS ROUTINE.
 AN ATTEMPT TO CLEAR THE MISC. REGISTER IS TRIED
 IF A TIME-OUT TRAP OCCURES POINTERS ARE UPDATED
 AND ATTEMPTED AGAIN. IF NO TIME-OUT; THE RECEIVER "ACTIVE BIT" (BIT 12)
 IS SET AND A *COMPARE* FOR BOTH SYNC1 AND SYNC 2 IS DONE
 AT THE MISC. REGISTER. IF THEY ARE THERE THIS IS
 A DQ11. THE INFORMATION IS STORED AWAY.

8.5.2 ONE SYNC BIT OR TWO?

SINCE TOO MUCH HARDWARE MUST BE TURNED ON TO SENSE THE
 PRESENTS OF ONE SYNC OR TWO. THE PROGRAM ASSUMES TWO SYNC
 CHARS. NOTE: THIS ASSUMPTION MAY BE ALTERED AFTER AUTO SIZING
 BY ALTERING BIT 15 IN APPRIOATE DQSTXX: LOCATION.

8.5.3 "BB" OPTION INSTALLED?

TO SENSE FOR THE "BB" OPTION THE PROGRAM SELECTS THE
 CHARACTER DET. REGISTER AND THE LOADS IN ALL 1'S; IF
 ANY ONE OR COMBINATION OF BITS ARE SET THE BB OPTION
 IS ASSUMED TO EXIST.

8.5.4 "AB" OPTION INSTALLED?

TO SENSE FOR THE "AB" OPTION THE PROGRAM SELECTS THE
 POLYNOMIAL REGISTER AND WRITES ALL 1'S INTO IT; IF ANY
 ONE OR COMBINATION OF BITS ARE SET THE AB OPTION IS ASSUMED
 TO EXIST.

8.5.5 "BA" OPTION INSTALLED?

TO SENSE FOR "BA" OPTION REQUEST TO SEND AND DATA TERMINAL
 READY ARE SET; IF EITHER ONE OR BOTH ARE SET THE PROGRAM
 ASSUMES THE BA OPTION EXISTES

8.5.6 JUMPER ON END OF CABLE?

THE PROGRAM CHECKS TO SEE IF EITHER OR BOTH CLEAR TO SEND AND CARRIER ARE SET; IF SO THE PROGRAM ASSUMES THE TEST JUMPER IS ON THE END OF THE CABLE.

8.5.7 ACTIVE ON FIRST NON-SYNC?

SINCE TOO MUCH HARDWARE MUST BE TURNED ON TO SENSE FOR WHEN THE DQ11 GOES ACTIVE THE PROGRAM ASSUMES "ACTIVE ON FIRST NON-SYNC". NOTE: THIS CAN BE CHANGED BY ALTERING BIT 11 IN THE APPRIOATE DQSTXX: AFTER AUTO SIZING

8.5.8 SET FOR ODD OR EVEN PARITY?

AS ABOVE TOO MUCH HARDWARE IS NEED TO SENSE WHICH PARITY WAS SELECTED. SO THE PROGRAM ASSEMES ODD PARITY. NOTE: THIS CAN BE CHANGED BY ALTERING BIT 9 IN APPRIO-ATE DQSTXX: LOCATION. AFTER AUTO SIZING

8.5.9 FINDING THE VECTOR.

THE PROGRAM SETS "PRIMARY DONE", "SECONDAY DONE", AND "INTERUPT ENABLE" AND LOOKS FOR AN INTERUPT. IF IT INTERUPTS IT IS PICKED UP AND STORED AWAY. IF NO INTERUPT OCCURES THE PROGRAM ASSUMES VECTOR =300. THIS PROBLEM WILL BE FIXED IN ONE OF THE DIAGNOSTICS AND *AUTO SIZING* SHOULD BE REDONE TO GET THE CORRECT VECTOR.

9. PROGRAM DESCRIPTION
CONTAINED WITHIN LISTING
10. LISTING
FOLLOWING

532
531
530
529
528
527
526
525
524
523
522
521
520
519
518
517
516
515
514
513
512
511
510
509
508
507
506
505
504
503
502
501
500

177320

NON.EX=177320
.ENABLE AMA

;MAINDEC-11-DZDQC-C/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST
;COPYRIGHT 1975, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754

;REVISED 21-JUNE-76 BY S. CARPENTER
;A)SUPPORTS SOFTWARE SWITCH REGISTER
;B)SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH REGISTER
;BY <↑G>.
;STARTING PROCEDURE
;LOAD PROGRAM
;LOAD ADDRESS 000200
;PRESS START
;PROGRAM WILL TYPE "MAINDEC-11-DZDQC-C/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST"
;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
;AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
;AND THEN RESUME TESTING

;SWITCH REGISTER OPTIONS

100000
040000
020000
010000
004000
002000
001000
000400
000100
000040
000020
000010
000004
000002
000001

SW15=100000 ;=1,HALT ON ERROR
SW14=40000 ;=1,LOOP ON CURRENT TEST
SW13=20000 ;=1,INHIBIT ERROR TYPEOUT
SW12=10000 ;=1,DELETE TYPEOUT/BELL ON ERROR.
SW11=4000 ;=1,INHIBIT ITERATIONS
SW10=2000 ;=1,ESCAPE TO NEXT TEST ON ERROR
SW09=1000 ;=1,LOOP WITH CURRENT DATA
SW08=400 ;=1,LOOP ON ERROR
SW06=100
SW05=40
SW04=20
SW03=10
SW02=4
SW01=2
SW00=1

;LOCK ON TEST SELECT
;RESTART PROGRAM AT SELECTED TEST
;RESELECT DQ11 DESIRED ACTIVE
;NOTE: THIS MUST NOT EXCEED ORIGINAL COUNT

```

570
571
572           ;REGISTER DEFINITIONS
573
574           000000      R0=%0           ;GENERAL REGISTER
575           000001      R1=%1           ;GENERAL REGISTER
576           000002      R2=%2           ;GENERAL REGISTER
577           000003      R3=%3           ;GENERAL REGISTER
578           000004      R4=%4           ;GENERAL REGISTER
579           000005      R5=%5           ;GENERAL REGISTER
580           000006      SP=%6          ;PROCESSOR STACK POINTER
581           000007      PC=%7          ;PROGRAM COUNTER
582
583           ;LOCATION EQUIVALENCIES
584
585           177570      DSWR= 177570    ;HARDWARE SWITCH REGISTER LOC.
586           177570      DLIGHTS=177570 ;HARDWARE DISPLAY REGISTER LOC.
587           177776      PS=177776     ;PROCESSOR STATUS WORD
588           001200      STACK=1200     ;START OF PROCESSOR STACK
589
590           ;INSTRUCTION DEFINITIONS
591
592           005746      PUSH1SP=5746    ;DECREMENT PROCESSOR STACK 1 WORD
593           005726      POP1SP=5726     ;INCREMENT PROCESSOR STACK 1 WORD
594           010046      PUSHRO=10046    ;SAVE R0 ON STACK
595           012600      POPFO=12600     ;RESTORE R0 FROM STACK
596           024646      PUSH2SP=24646  ;DECREMENT STACK TWICE
597           022626      POP2SP=22626   ;INCREMENT STACK TWICE
598           .EQUIV EMT,HLT ;BASIC DEFINITION OF ERROR CALL
599
600
601           100000      BIT15=100000
602           040000      BIT14=40000
603           020000      BIT13=20000
604           010000      BIT12=10000
605           004000      BIT11=4000
606           002000      BIT10=2000
607           001000      BIT9=1000
608           000400      BIT8=400
609           000200      BIT7=200
610           000100      BIT6=100
611           000040      BIT5=40
612           000020      BIT4=20
613           000010      BIT3=10
614           000004      BIT2=4
615           000002      BIT1=2
616           000001      BIT0=1
617
618           ;DQ11 OPTIONAL DEFINITIONS
619
620
621           002000      ABBIT=2000
622           004000      ACTBIT=4000
623           010000      BABIT=10000
624           020000      BBBIT=20000
625           040000      JUMBIT=40000

```

626 001000 ODDBIT=1000
 627 100000 SYNBIT=100000

;DQ11 SECONDARY REGISTER DEFINATIONS

630	000000	RXBA.P=0	;RECEIVER BUS ADDRESS PRIMARY.
631	000001	RXWC.P=1	;RECEIVER WORD COUNT PRIMARY.
632	000002	TXBA.P=2	;TRANSMITTER BUS ADDRESS PRIMARY.
633	000003	TXWC.P=3	;TRANSMITTER BUS ADDRESS PRIMARY.
634	000004	RXBA.S=4	;RECEIVER BUS ADDRESS SECONDARY.
635	000005	RXWC.S=5	;RECEIVER WORD COUNT SECONDARY.
636	000006	TXBA.S=6	;TRANSMITTER BUS ADDRESS SECONDARY.
637	000007	TXWC.S=7	;TRANSMITTER WORD COUNT SECONDARY.
640			
641	000010	CHARDT=10	;CHARACTER DETECT REGISTER.
642	000011	SYNC.=11	;SYNC REGISTER.
643	000012	MISC.=12	;MISCELLANEOUS REGISTER.
644	000013	TX.MUX=13	;TRANSMITTER MUX REGISTER.
645	000014	SEQ.=14	;SEQUENCE REGISTER.
646	000015	RX.BCC=15	;RECEIVER BCC REGISTER.
647	000016	TX.BCC=16	;TRANSMITTER BCC REGISTER.
648	000017	POLY.=17	;POLYNOMIAL REGISTER.
649			
650			

707	000154	000156	.+2	:UNEXPECTED TRAP TO THIS LOCATION
708	000156	000000	HALT	:EXAMINE STACK TO FIND CAUSE
709	000160	000162	.+2	:UNEXPECTED TRAP TO THIS LOCATION
710	000162	000000	HALT	:EXAMINE STACK TO FIND CAUSE
711	000164	000166	.+2	:UNEXPECTED TRAP TO THIS LOCATION
712	000166	000000	HALT	:EXAMINE STACK TO FIND CAUSE
713	000170	000172	.+2	:UNEXPECTED TRAP TO THIS LOCATION
714	000172	000000	HALT	:EXAMINE STACK TO FIND CAUSE
715	000174	000176	.+2	:UNEXPECTED TRAP TO THIS LOCATION
716	000176	000000	HALT	:EXAMINE STACK TO FIND CAUSE
717	000200	000202	.+2	:UNEXPECTED TRAP TO THIS LOCATION
718	000202	000000	HALT	:EXAMINE STACK TO FIND CAUSE
719	000204	000206	.+2	:UNEXPECTED TRAP TO THIS LOCATION
720	000206	000000	HALT	:EXAMINE STACK TO FIND CAUSE
721	000210	000212	.+2	:UNEXPECTED TRAP TO THIS LOCATION
722	000212	000000	HALT	:EXAMINE STACK TO FIND CAUSE
723	000214	000216	.+2	:UNEXPECTED TRAP TO THIS LOCATION
724	000216	000000	HALT	:EXAMINE STACK TO FIND CAUSE
725	000220	000222	.+2	:UNEXPECTED TRAP TO THIS LOCATION
726	000222	000000	HALT	:EXAMINE STACK TO FIND CAUSE
727	000224	000226	.+2	:UNEXPECTED TRAP TO THIS LOCATION
728	000226	000000	HALT	:EXAMINE STACK TO FIND CAUSE
729	000230	000232	.+2	:UNEXPECTED TRAP TO THIS LOCATION
730	000232	000000	HALT	:EXAMINE STACK TO FIND CAUSE
731	000234	000236	.+2	:UNEXPECTED TRAP TO THIS LOCATION
732	000236	000000	HALT	:EXAMINE STACK TO FIND CAUSE
733	000240	000242	.+2	:UNEXPECTED TRAP TO THIS LOCATION
734	000242	000000	HALT	:EXAMINE STACK TO FIND CAUSE
735	000244	000246	.+2	:UNEXPECTED TRAP TO THIS LOCATION
736	000246	000000	HALT	:EXAMINE STACK TO FIND CAUSE
737	000250	000252	.+2	:UNEXPECTED TRAP TO THIS LOCATION
738	000252	000000	HALT	:EXAMINE STACK TO FIND CAUSE
739	000254	000256	.+2	:UNEXPECTED TRAP TO THIS LOCATION
740	000256	000000	HALT	:EXAMINE STACK TO FIND CAUSE
741	000260	000262	.+2	:UNEXPECTED TRAP TO THIS LOCATION
742	000262	000000	HALT	:EXAMINE STACK TO FIND CAUSE
743	000264	000266	.+2	:UNEXPECTED TRAP TO THIS LOCATION
744	000266	000000	HALT	:EXAMINE STACK TO FIND CAUSE
745	000270	000272	.+2	:UNEXPECTED TRAP TO THIS LOCATION
746	000272	000000	HALT	:EXAMINE STACK TO FIND CAUSE
747	000274	000276	.+2	:UNEXPECTED TRAP TO THIS LOCATION
748	000276	000000	HALT	:EXAMINE STACK TO FIND CAUSE
749	000300	000302	.+2	:UNEXPECTED TRAP TO THIS LOCATION
750	000302	000000	HALT	:EXAMINE STACK TO FIND CAUSE
751	000304	000306	.+2	:UNEXPECTED TRAP TO THIS LOCATION
752	000306	000000	HALT	:EXAMINE STACK TO FIND CAUSE
753	000310	000312	.+2	:UNEXPECTED TRAP TO THIS LOCATION
754	000312	000000	HALT	:EXAMINE STACK TO FIND CAUSE
755	000314	000316	.+2	:UNEXPECTED TRAP TO THIS LOCATION
756	000316	000000	HALT	:EXAMINE STACK TO FIND CAUSE
757	000320	000322	.+2	:UNEXPECTED TRAP TO THIS LOCATION
758	000322	000000	HALT	:EXAMINE STACK TO FIND CAUSE
759	000324	000326	.+2	:UNEXPECTED TRAP TO THIS LOCATION
760	000326	000000	HALT	:EXAMINE STACK TO FIND CAUSE
761	000330	000332	.+2	:UNEXPECTED TRAP TO THIS LOCATION
762	000332	000000	HALT	:EXAMINE STACK TO FIND CAUSE

763	000334	000336	.+2	:UNEXPECTED TRAP TO THIS LOCATION
764	000336	000000	HALT	:EXAMINE STACK TO FIND CAUSE
765	000340	000342	.+2	:UNEXPECTED TRAP TO THIS LOCATION
766	000342	000000	HALT	:EXAMINE STACK TO FIND CAUSE
767	000344	000346	.+2	:UNEXPECTED TRAP TO THIS LOCATION
768	000346	000000	HALT	:EXAMINE STACK TO FIND CAUSE
769	000350	000352	.+2	:UNEXPECTED TRAP TO THIS LOCATION
770	000352	000000	HALT	:EXAMINE STACK TO FIND CAUSE
771	000354	000356	.+2	:UNEXPECTED TRAP TO THIS LOCATION
772	000356	000000	HALT	:EXAMINE STACK TO FIND CAUSE
773	000360	000362	.+2	:UNEXPECTED TRAP TO THIS LOCATION
774	000362	000000	HALT	:EXAMINE STACK TO FIND CAUSE
775	000364	000366	.+2	:UNEXPECTED TRAP TO THIS LOCATION
776	000366	000000	HALT	:EXAMINE STACK TO FIND CAUSE
777	000370	000372	.+2	:UNEXPECTED TRAP TO THIS LOCATION
778	000372	000000	HALT	:EXAMINE STACK TO FIND CAUSE
779	000374	000376	.+2	:UNEXPECTED TRAP TO THIS LOCATION
780	000376	000000	HALT	:EXAMINE STACK TO FIND CAUSE
781	000400	000402	.+2	:UNEXPECTED TRAP TO THIS LOCATION
782	000402	000000	HALT	:EXAMINE STACK TO FIND CAUSE
783	000404	000406	.+2	:UNEXPECTED TRAP TO THIS LOCATION
784	000406	000000	HALT	:EXAMINE STACK TO FIND CAUSE
785	000410	000412	.+2	:UNEXPECTED TRAP TO THIS LOCATION
786	000412	000000	HALT	:EXAMINE STACK TO FIND CAUSE
787	000414	000416	.+2	:UNEXPECTED TRAP TO THIS LOCATION
788	000416	000000	HALT	:EXAMINE STACK TO FIND CAUSE
789	000420	000422	.+2	:UNEXPECTED TRAP TO THIS LOCATION
790	000422	000000	HALT	:EXAMINE STACK TO FIND CAUSE
791	000424	000426	.+2	:UNEXPECTED TRAP TO THIS LOCATION
792	000426	000000	HALT	:EXAMINE STACK TO FIND CAUSE
793	000430	000432	.+2	:UNEXPECTED TRAP TO THIS LOCATION
794	000432	000000	HALT	:EXAMINE STACK TO FIND CAUSE
795	000434	000436	.+2	:UNEXPECTED TRAP TO THIS LOCATION
796	000436	000000	HALT	:EXAMINE STACK TO FIND CAUSE
797	000440	000442	.+2	:UNEXPECTED TRAP TO THIS LOCATION
798	000442	000000	HALT	:EXAMINE STACK TO FIND CAUSE
799	000444	000446	.+2	:UNEXPECTED TRAP TO THIS LOCATION
800	000446	000000	HALT	:EXAMINE STACK TO FIND CAUSE
801	000450	000452	.+2	:UNEXPECTED TRAP TO THIS LOCATION
802	000452	000000	HALT	:EXAMINE STACK TO FIND CAUSE
803	000454	000456	.+2	:UNEXPECTED TRAP TO THIS LOCATION
804	000456	000000	HALT	:EXAMINE STACK TO FIND CAUSE
805	000460	000462	.+2	:UNEXPECTED TRAP TO THIS LOCATION
806	000462	000000	HALT	:EXAMINE STACK TO FIND CAUSE
807	000464	000466	.+2	:UNEXPECTED TRAP TO THIS LOCATION
808	000466	000000	HALT	:EXAMINE STACK TO FIND CAUSE
809	000470	000472	.+2	:UNEXPECTED TRAP TO THIS LOCATION
810	000472	000000	HALT	:EXAMINE STACK TO FIND CAUSE
811	000474	000476	.+2	:UNEXPECTED TRAP TO THIS LOCATION
812	000476	000000	HALT	:EXAMINE STACK TO FIND CAUSE
813	000500	000502	.+2	:UNEXPECTED TRAP TO THIS LOCATION
814	000502	000000	HALT	:EXAMINE STACK TO FIND CAUSE
815	000504	000506	.+2	:UNEXPECTED TRAP TO THIS LOCATION
816	000506	000000	HALT	:EXAMINE STACK TO FIND CAUSE
817	000510	000512	.+2	:UNEXPECTED TRAP TO THIS LOCATION
818	000512	000000	HALT	:EXAMINE STACK TO FIND CAUSE

019	000514	000516	.+2	: UNEXPECTED TRAP TO THIS LOCATION
020	000516	000000	HALT	: EXAMINE STACK TO FIND CAUSE
021	000520	000522	.+2	: UNEXPECTED TRAP TO THIS LOCATION
022	000522	000000	HALT	: EXAMINE STACK TO FIND CAUSE
023	000524	000526	.+2	: UNEXPECTED TRAP TO THIS LOCATION
024	000526	000000	HALT	: EXAMINE STACK TO FIND CAUSE
025	000530	000532	.+2	: UNEXPECTED TRAP TO THIS LOCATION
026	000532	000000	HALT	: EXAMINE STACK TO FIND CAUSE
027	000534	000536	.+2	: UNEXPECTED TRAP TO THIS LOCATION
028	000536	000000	HALT	: EXAMINE STACK TO FIND CAUSE
029	000540	000542	.+2	: UNEXPECTED TRAP TO THIS LOCATION
030	000542	000000	HALT	: EXAMINE STACK TO FIND CAUSE
031	000544	000546	.+2	: UNEXPECTED TRAP TO THIS LOCATION
032	000546	000000	HALT	: EXAMINE STACK TO FIND CAUSE
033	000550	000552	.+2	: UNEXPECTED TRAP TO THIS LOCATION
034	000552	000000	HALT	: EXAMINE STACK TO FIND CAUSE
035	000554	000556	.+2	: UNEXPECTED TRAP TO THIS LOCATION
036	000556	000000	HALT	: EXAMINE STACK TO FIND CAUSE
037	000560	000562	.+2	: UNEXPECTED TRAP TO THIS LOCATION
038	000562	000000	HALT	: EXAMINE STACK TO FIND CAUSE
039	000564	000566	.+2	: UNEXPECTED TRAP TO THIS LOCATION
040	000566	000000	HALT	: EXAMINE STACK TO FIND CAUSE
041	000570	000572	.+2	: UNEXPECTED TRAP TO THIS LOCATION
042	000572	000000	HALT	: EXAMINE STACK TO FIND CAUSE
043	000574	000576	.+2	: UNEXPECTED TRAP TO THIS LOCATION
044	000576	000000	HALT	: EXAMINE STACK TO FIND CAUSE
045	000600	000602	.+2	: UNEXPECTED TRAP TO THIS LOCATION
046	000602	000000	HALT	: EXAMINE STACK TO FIND CAUSE
047	000604	000606	.+2	: UNEXPECTED TRAP TO THIS LOCATION
048	000606	000000	HALT	: EXAMINE STACK TO FIND CAUSE
049	000610	000612	.+2	: UNEXPECTED TRAP TO THIS LOCATION
050	000612	000000	HALT	: EXAMINE STACK TO FIND CAUSE
051	000614	000616	.+2	: UNEXPECTED TRAP TO THIS LOCATION
052	000616	000000	HALT	: EXAMINE STACK TO FIND CAUSE
053	000620	000622	.+2	: UNEXPECTED TRAP TO THIS LOCATION
054	000622	000000	HALT	: EXAMINE STACK TO FIND CAUSE
055	000624	000626	.+2	: UNEXPECTED TRAP TO THIS LOCATION
056	000626	000000	HALT	: EXAMINE STACK TO FIND CAUSE
057	000630	000632	.+2	: UNEXPECTED TRAP TO THIS LOCATION
058	000632	000000	HALT	: EXAMINE STACK TO FIND CAUSE
059	000634	000636	.+2	: UNEXPECTED TRAP TO THIS LOCATION
060	000636	000000	HALT	: EXAMINE STACK TO FIND CAUSE
061	000640	000642	.+2	: UNEXPECTED TRAP TO THIS LOCATION
062	000642	000000	HALT	: EXAMINE STACK TO FIND CAUSE
063	000644	000646	.+2	: UNEXPECTED TRAP TO THIS LOCATION
064	000646	000000	HALT	: EXAMINE STACK TO FIND CAUSE
065	000650	000652	.+2	: UNEXPECTED TRAP TO THIS LOCATION
066	000652	000000	HALT	: EXAMINE STACK TO FIND CAUSE
067	000654	000656	.+2	: UNEXPECTED TRAP TO THIS LOCATION
068	000656	000000	HALT	: EXAMINE STACK TO FIND CAUSE
069	000660	000662	.+2	: UNEXPECTED TRAP TO THIS LOCATION
070	000662	000000	HALT	: EXAMINE STACK TO FIND CAUSE
071	000664	000666	.+2	: UNEXPECTED TRAP TO THIS LOCATION
072	000666	000000	HALT	: EXAMINE STACK TO FIND CAUSE
073	000670	000672	.+2	: UNEXPECTED TRAP TO THIS LOCATION
074	000672	000000	HALT	: EXAMINE STACK TO FIND CAUSE

875	000674	000676	.+2	:UNEXPECTED TRAP TO THIS LOCATION
876	000676	000000	HALT	:EXAMINE STACK TO FIND CAUSE
877	000700	000702	.+2	:UNEXPECTED TRAP TO THIS LOCATION
878	000702	000000	HALT	:EXAMINE STACK TO FIND CAUSE
879	000704	000706	.+2	:UNEXPECTED TRAP TO THIS LOCATION
880	000706	000000	HALT	:EXAMINE STACK TO FIND CAUSE
881	000710	000712	.+2	:UNEXPECTED TRAP TO THIS LOCATION
882	000712	000000	HALT	:EXAMINE STACK TO FIND CAUSE
883	000714	000716	.+2	:UNEXPECTED TRAP TO THIS LOCATION
884	000716	000000	HALT	:EXAMINE STACK TO FIND CAUSE
885	000720	000722	.+2	:UNEXPECTED TRAP TO THIS LOCATION
886	000722	000000	HALT	:EXAMINE STACK TO FIND CAUSE
887	000724	000726	.+2	:UNEXPECTED TRAP TO THIS LOCATION
888	000726	000000	HALT	:EXAMINE STACK TO FIND CAUSE
889	000730	000732	.+2	:UNEXPECTED TRAP TO THIS LOCATION
890	000732	000000	HALT	:EXAMINE STACK TO FIND CAUSE
891	000734	000736	.+2	:UNEXPECTED TRAP TO THIS LOCATION
892	000736	000000	HALT	:EXAMINE STACK TO FIND CAUSE
893	000740	000742	.+2	:UNEXPECTED TRAP TO THIS LOCATION
894	000742	000000	HALT	:EXAMINE STACK TO FIND CAUSE
895	000744	000746	.+2	:UNEXPECTED TRAP TO THIS LOCATION
896	000746	000000	HALT	:EXAMINE STACK TO FIND CAUSE
897	000750	000752	.+2	:UNEXPECTED TRAP TO THIS LOCATION
898	000752	000000	HALT	:EXAMINE STACK TO FIND CAUSE
899	000754	000756	.+2	:UNEXPECTED TRAP TO THIS LOCATION
900	000756	000000	HALT	:EXAMINE STACK TO FIND CAUSE
901	000760	000762	.+2	:UNEXPECTED TRAP TO THIS LOCATION
902	000762	000000	HALT	:EXAMINE STACK TO FIND CAUSE
903	000764	000766	.+2	:UNEXPECTED TRAP TO THIS LOCATION
904	000766	000000	HALT	:EXAMINE STACK TO FIND CAUSE
905	000770	000772	.+2	:UNEXPECTED TRAP TO THIS LOCATION
906	000772	000000	HALT	:EXAMINE STACK TO FIND CAUSE
907	000774	000776	.+2	:UNEXPECTED TRAP TO THIS LOCATION
908	000776	000000	HALT	:EXAMINE STACK TO FIND CAUSE

```

909                                     ;STANDARD INTERRUPT VECTORS
910
911                                     . =24
912 000024 000024 .PFail                    ;POWER FAIL HANDLER
913 000026 014564 340                     ;SERVICE AT LEVEL 7
914 000030 014234 .HLT                     ;ERROR HANDLER
915 000032 000340 340                     ;SERVICE AT LEVEL 7
916 000034 014202 .TRPSRV                 ;GENERAL HANDLER DISPATCH SERVICE
917 000036 000340 340                     ;SERVICE AT LEVEL 7
918
919                                     . =46
920 000046 012762 LOGICAL                  ;ACT HOOKS
921
922                                     . =52
923 000052 000000 .WORD 0
924
925 ;THIS ROUTINE TRIES TO FORCE THE RECEIVER TO INTERRUPT
926 ;TO ITS VECTOR WHERE IT WILL PICK UP THE STATUS LOCATION
927 ;FOR ITS NEW PC; AND PICK UP AN IOT INSTRUCTION FOR ITS
928 ;NEW PS. WHEN THE NEW PC IS FETCHED AN IOT INSTRUCTION IS
929 ;EXECUTED, TRAPPING TO LOCATION 20 WHERE A ROUTINE IS EXECUTED
930 ;TO TAKE THE PC FROM THE STACK AND USE IT AS THE VECTOR ADDRESS
931                                     . =56
932
933 VECMAP:
934 1$: MOV R1,(R0)+ ;START FILLING THE VECTOR AREA
935     MOV #4,(R1)+ ;WITH +2; IOT (4)
936     CMP (R0)+,(R1)+ ;UPDATE THE POINTERS
937     CMP R1,#1000 ;IS ALL FLOATING VECTOR AREA DONE
938     BLOS 1$ ;BR IF NOT ALL DONE
939     MOV #4$,$#20 ;SET FOR IOT TRAP BY DQ11
940     MOV DQACTV,TEMP1 ;GET THE ACTIVE DQ11 S
941     ROR TEMP1 ;ARE YOU ACTIVE.. DQ11
942     BCC 5$ ;IF CARRY CLEAR.. NO MORE DQ11S
943     CLR PS ;CLEAR PS
944     TST (R2)+ ;PUT POINTER TO STATUS TABLE
945     MOV #340,$-2(R2) ;TRY AND SET PRI/SEC DONE AND IE
946     INCB R0 ;DELAY.....
947     BNE .-2 ;.....DELAY
948     MOVB #300,(R2) ;NO INTERRUPT ASSUME 300 FIX IN TEST C
949     TST (R2)+ ;UPDATE POINTERS
950     BR 2$ ;GO DO IT AGAIN
951     BIS (SP),(R2) ;ENTERD BY IOT TRAP BY DQ11
952     BIC #7,(R2) ;CLEAR UNWANTED BITS
953     CMP (SP)+,(SP)+ ;POP IOT JUNK OFF STACK
954     MOV #3$, (SP) ;SET RETURN PC ON STACK
955     RTI ;GO HOME
956     RTS PC ;ALL SIZING IS DONE
957
958 ;****SOFTWARE SWITCH REGISTER****
959 . =174
960 DISPREG: 0 ;SOFTWARE DISPLAY REGISTER
961 SWREG: 0 ;SOFTWARE SWITCH REGISTER
962
963 ;PROGRAM START
964
965                                     . =200
966 000200 000137 001512 JMP .START ;GO TO START OF PROGRAM
    
```

965		000220		.=220					
966	000220	012702	001400	CSRMAP:	MOV	#1400,R2	:	CLEAR ALL STATUS TABLE	
967	000224	005022			CLR	(R2)+	:	DO CLEAR	
968	000226	022702	001512		CMP	#1512,R2	:	ALL TABLE DONE	
969	000232	001374			BNE	.-6	:	BR IF MORE TO GO	
970	000234	005037	001504		CLR	DQNUM	:	SET NUMBER OF DQ11S TO 0	
971	000240	012702	001400		MOV	#1400,R2	:	SET TABLE POINTER	
972	000244	012701	160000		MOV	#160000,R1	:	GET FIRST FLOATING ADDRESS	
973	000250	012737	000614	000004	MOV	#5\$,2#4	:	SET FOR TIME OUT TRAP--NO DEVICE--	
974	000256	112761	000012	000005	1\$:	MOVB	#12,5(R1)	:	TRY AND SEL MISC REGISTER
975	000264	005061	000006		CLR	6(R1)	:	TRY AND CLEAR MISC REG	
976	000270	012711	010000		MOV	#10000,(R1)	:	TRY AND SET RX ACTIVE	
977	000274	022761	030000	000006	CMP	#30000,6(R1)	:	LOOK FOR SYNC 1 AND SYNC 2	
978	000302	001071			BNE	2\$:	THIS IS NOT A DQ11 IF I BRANCH	
979	000304	010122			MOV	R1,(R2)+	:	NOW THIS IS A DQ11 --STORE CSR	
980	000306	052712	100000		BIS	#SYNBIT,(R2)	:	SET FOR TWO SYNC CHARS	
981	000312	005011			CLR	(R1)	:	CLEAR DQ ACTIVE BIT	
982	000314	112761	000010	000005	MOVB	#10,5(R1)	:	SEL CHAR DET REGISTER	
983	000322	012761	177777	000006	MOV	#-1,6(R1)	:	WRITE INTO CHAR DET REG	
984	000330	005761	000006		TST	6(R1)	:	WAS THE REGISTER WRITTEN?	
985	000334	001402			BEQ	.-+6	:	APPARENTLY NO BB OPTION.	
986	000336	052712	020000		BIS	#BBBIT,(R2)	:	SET FOR BB OPTION	
987	000342	112761	000017	000005	MOVB	#17,5(R1)	:	SEL POLYNO. REGISTER	
988	000350	012761	177777	000006	MOV	#-1,6(R1)	:	WRITE POLYNO. REGISTER	
989	000356	005761	000006		TST	6(R1)	:	WAS REG WRITTEN??	
990	000362	001402			BEQ	.-+6	:	BR IF NO AB OPTION	
991	000364	052712	002000		BIS	#ABBIT,(R2)	:	SET FOR AB OPTION	
992	000370	012761	001400	000002	MOV	#1400,2(R1)	:	TRY TO SET DTR. RS.	
993	000376	032761	001400	000002	BIT	#1400,2(R1)	:	DID ANY OF THEM SET	
994	000404	001402			BEQ	.-+6	:	BR IF NO BA OPTION	
995	000406	052712	010000		BIS	#BABIT,(R2)	:	SET FOR BA OPTION	
996	000412	032761	030000	000002	BIT	#30000,2(R1)	:	DID CS. CO. SET	
997	000420	001402			BEQ	.-+6	:	BR IF NO JUMPER	
998	000422	052712	040000		BIS	#JUMBIT,(R2)	:	SET FOR JUMPER	
999	000426	052712	004000		BIS	#ACTBIT,(R2)	:	SET FOR ACTIVE ON FIRST NON-SYNC	
1000	000432	052712	001000		BIS	#ODDBIT,(R2)	:	SET FOR ODD VRC.....	
1001	000436	005722			TST	(R2)+	:	POP POINTER	
1002	000440	005011			CLR	(R1)	:	CLEAR RCSR	
1003	000442	005061	000002		CLR	2(R1)	:	CLEAR TCSR	
1004	000446	005061	000002		CLR	2(R1)	:	CLEAR AGAIN	
1005	000452	005061	000004		CLR	4(R1)	:	CLEAR ERROR REG	
1006	000456	005061	000006		CLR	6(R1)	:	CLEAR SEC REG	
1007	000462	005237	001504		INC	DQNUM	:	UPDATE NUMBER OF DQ11S	
1008	000466	062701	000010	2\$:	ADD	#10,R1	:	UPDATE CSR POINTER BY 10 (8)	
1009	000472	022701	164000		CMP	#164000,R1	:	HAVE ALL FLOATING ADDRESSES BEEN CHECKED??	
1010	000476	001267			BNE	1\$:	BR IF NOT ALL DONE	
1011	000500	005037	001500		CLR	DQACTV	:	ZERO ACTIVE DQ11S	
1012	000504	005737	001504		TST	DQNUM	:	WERE ANY DQ11S FOUND	
1013	000510	001434			BEQ	4\$:	HEY BUDDY. NO DQ11S FOUND IN SYSTEM	
1014	000512	013701	001504		MOV	DQNUM,R1	:	SAVE NUMBER OF DQ11S	
1015	000516	010137	001276		MOV	R1,SAVNUM	:	SAVE NUMBER FOR ACT11	
1016	000522	000241		3\$:	CLC		:	CLEAR CARRY	
1017	000524	006137	001500		ROL	DQACTV	:	+++++ ACTIVE ADDRESS	
1018	000530	005237	001500		INC	DQACTV	:	SET BIT 0	
1019	000534	005301			DEC	R1	:	DEC NUMBER OF DQ11S	
1020	000536	001371			BNE	3\$:	BR IF MORE TO GO	

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 DZDQCC.P11 ROUTINES USED FOR AUTO SIZING.

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1021 000540 012737 000006 000004      MOV      #6,J#4      ;RESET TIME OUT VECTOR
1022 000546 013737 001500 001502      MOV      DQACTV,SAVACT ;SAVE ACTIVE
1023 000554 012737 000340 000022      MOV      #340,J#22   ;SET IOT TRAP PRIO: TO 7
1024 000562 012702 001400          MOV      #1400,R2    ;SET TABLE POINTER
1025 000566 012700 000300          MOV      #300,R0     ;SET VECTOR START
1026 000572 012701 000302          MOV      #302,R1     ;SET VECTOR+2 START
1027 000576 000137 000056          JMP      VECMAP      ;GO FIND THE VECTORS
1028 000602 104402          4$:      TYPE        ;TYPE MESSAGE
1029 000604 015125          MERR2     ;I DIDN'T FIND ANY DQ11S. DON'T USE AUTO SIZE.
1030 000606 005000          CLR      R0         ;
1031 000610 000000          HALT      ;HOW CAN I TEST NO DQ11S
1032 000612 000776          BR       -2         ;DON'T LET OPR HIT CONT. SW
1033 000614 012716 000466          5$:      MOV      #2$, (SP) ;ENTERED BY TIME OUT TRAP
1034 000620 000002          RTI         ;GO HOME.
1035
1036
1037          ;=1000
1038 001000 005377 040515 047111  MTITLE: .ASCIZ <377><12>/MAINDEC-11-DZDQC-C/<377>/DQ11 INTERRUPT AND NPR LOGIC TEST/<37
1039 001006 042504 026503 030461
1040 001014 042055 042132 041521
1041 001022 041455 042377 030521
1042 001030 020061 047111 042524
1043 001036 051122 050125 020124
1044 001044 047101 020104 050116
1045 001052 020122 047514 044507
1046 001060 020103 042524 052123
1047 001066 000377
1048
1049          ;=1200
1050          ;INDIRECT POINTERS
1051
1052 001200 177570  SWR:      177570      ;SWITCH REGISTER POINTER
1053 001202 177570  LIGHTS:   177570     ;DISPLAY REGISTER POINTER
1054 001204 177560  TKCSR:   177560     ;TELETYPE KEYBOARD CONTROL REGISTER
1055 001206 177562  TKDBR:   177562     ;TELETYPE KEYBOARD DATA BUFFER
1056 001210 177564  TPCSR:   177564     ;TELEPRINTER CONTROL REGISTER
1057 001212 177566  TPDBR:   177566     ;TELEPRINTER DATA BUFFER
1058
1059          ;PROGRAM CONTROL PARAMETERS
1060
1061 001214 000000  RETURN:  0          ;SCOPE ADDRESS FOR LOOP ON TEST
1062 001216 000000  NEXT:    0          ;ADDRESS OF NEXT TEST TO BE EXECUTED
1063 001220 000000  LOCK:    0          ;ADDRESS FOR LOCK ON CURRENT DATA
1064 001222 000003  ICOUNT:  3          ;NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE EXECUTED
1065 001224 000000  LPCNT:   0          ;NUMBER OF ITERATIONS COMPLETED
1066 001226 000000  TSTNO:   0          ;NUMBER OF TEST IN PROGRESS
1067 001230 000000  PASCNT:  0          ;NUMBER OF PASSES COMPLETED
1068 001232 000000  ERRCNT:  0          ;TOTAL NUMBER OF ERRORS
1069 001234 000000  LSTERR:  0          ;PC OF LAST ERROR CALL
1070
1071          ;PROGRAM VARIABLES
1072
1073 001236 000000  CHAR1:   0
1074 001240 000000  CHAR2:   0
1075 001242 000000  CHAR3:   0
1076 001244 000000  TEMP1:   0          ;TEMPORARY STORAGE

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DZDQCC.P11 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

1077	001246	000000	TEMP2:	0	: TEMPORARY STORAGE
1078	001250	000000	TEMP3:	00	: TEMPORARY STORAGE
1079	001252	000000	TEMP4:	00	: TEMPORARY STORAGE
1080	001254	000000	TEMP5:	00	: TEMPORARY STORAGE
1081	001256	000000	SAVR0:	00	: R0 STORAGE
1082	001260	000000	SAVR1:	00	: R1 STORAGE
1083	001262	000000	SAVR2:	00	: R2 STORAGE
1084	001264	000000	SAVR3:	00	: R3 STORAGE
1085	001266	000000	SAVR4:	00	: R4 STORAGE
1086	001270	000000	SAVR5:	00	: R5 STORAGE
1087	001272	000000	SAVSP:	00	: STACK POINTER STORAGE
1088	001274	000000	SAVPC:	00	: PROGRAM COUNTER STORAGE
1089	001276	000000	SAVNUM:	0	
1090	001300	000001	CREAM:	.BLKW 1	
1091	001302	000000	RUNFLG:	0	
1092	001304	000000	RUN:	0	
1093	001306	000000	RUNCNT:	0	

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1097 001310 000
1098 001311 000
1099 001312 000
1100 001313 000
1101 000000
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1103
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1109 001314
1110 104400
1111 001314 013025
1112 104401
1113 001316 013150
1114 104402
1115 001320 013170
1116 104403
1117 001322 013276
1118 104404
1119 001324 013414
1120 104405
1121 001326 013446
1122 104406
1123 001330 013662
1124 104407
1125 001332 013722
1126 104410
1127 001334 013754
1128 104411
1129 001336 013760
1130 104412
1131 001340 015620
1132 104413
1133 001342 015636
1134 104414
1135 001344 014662
1136 104415
1137 001346 014736
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1144 001350 000000
1145 001352 000000
1146 001354 000000
1147 001356 000000
1148 001360 000000
1149 001362 000000

;PROGRAM CONTROL FLAGS
INIFLG: .BYTE 0 ;PROGRAM INITIALIZATION FLAG
STFLG: .BYTE 0 ;TEST START FLAG
ERRFLG: .BYTE 0 ;ERROR OCCURED FLAG
LOKFLG: .BYTE 0 ;LOCK ON CURRENT TEST FLAG
SY=0

;DEFINITIONS FOR TRAP SUBROUTINE CALLS
;POINTERS TO SUBROUTINES CAN BE FOUND
;IN THE TABLE IMMEDIATLY FOLLOWING THE DEFINITIONS

;*****
;*****
;TRPTAB:
SCOPE=TRAP+0 ;CALL TO SCOPE LOOP AND ITERATION HANDLER
SCOPE
SCOPI=TRAP+1 ;CALL TO LOOP ON CURRENT DATA HANDLER
SCOPI
TYPE=TRAP+2 ;CALL TO TELETYPE OUTPUT ROUTINE
TYPE
INSTR=TRAP+3 ;CALL TO ASCII STRING INPUT ROUTINE
INSTR
INSTER=TRAP+4 ;CALL TO INPUT ERROR HANDLER
INSTER
PARAM=TRAP+5 ;CALL TO NUMERICAL DATA INPUT ROUTINE
PARAM
SAVOS=TRAP+6 ;CALL TO REGISTER SAVE ROUTINE
SAVOS
RESOS=TRAP+7 ;CALL TO REGISTER RESTORE ROUTINE
RESOS
CONVRT=TRAP+10 ;CALL TO DATA OUTPUT ROUTINE
CONVRT
CNVRT=TRAP+11 ;CALL TO DATA OUTPUT ROUNTINE WITHOUT CR/LF.
CNVRT
MSTCLR=TRAP+12 ;CALL TO ISSUE MASTER CLEAR
MSTCLR
MEMCLR=TRAP+13 ;CALL TO CLEAR ALL SCRATCH PAD MEMORIES
MEMCLR
CKSWR=TRAP+14 ;CALL TO ALLOW SWREG TO BE LOADED FROM TTY
CKSWR
CNTLU=TRAP+15 ;CALL TO ALLOW LOADING OF SWREG FROM TTY
CNTLU

;*****
;*****

;DQ11 VECTOR AND REGISTER INDIRECT POINTERS
DQAVEC: 0 ;POINTER TO DQ11 RECEIVER INTERRUPT VECTOR
DQRLVL: 0 ;POINTER TO DQ11 RECEIVER INTERRUPT SERVICE PS
DQTVEC: 0 ;POINTER TO DQ11 TRANSMITTER INTERRUPT VECTOR
DQTLVL: 0 ;POINTER TO DQ11 TRANSMITTER INTERRUPT SERVICE PS
DQRC SR: 0 ;POINTER TO DQ11 RECEIVER CONTROL REGISTER
DQRC SH: 0 ;POINTER TO HIGH BYTE OF DQ11 RECEIVER CONTROL REGISTER
    
```


M02

DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 26
 DZDQCC.P11 PROGRAM INITIALIZATION AND START UP.

1206	001512	012737	000340	177776	.START:	MOV	#340,PS	;LOCK OUT INTERRUPTS
1207	001520	012706	001200			MOV	#STACK,SP	;SET UP STACK
1208	001524	012737	014564	000024		MOV	#.PFAIL,@#24	;SET UP POWER FAIL VECTOR
1209	001532	013737	001504	001276		MOV	DQNUM,SAVNUM	
1210	001540	105037	001311			CLRB	STFLG	;CLEAR START FLAG
1211	001544	005037	001230			CLR	PASCNT	;CLEAR PASS COUNT
1212	001550	105037	001312			CLRB	ERRFLG	;CLEAR ERROR FLAG
1213	001554	005037	001302			CLR	RUNFLG	
1214	001560	012737	001400	001300		MOV	#1400,CREAM	
1215	001566	005037	001232			CLR	ERRCNT	;CLEAR ERROR COUNT
1216	001572	005037	001234			CLR	LSTERR	;CLEAR LAST ERROR POINTER
1217	001576	012737	000001	001226		MOV	#1,TSTNO	;SET UP FOR TEST 1
1218	001604	012737	001512	001214		MOV	#.START,RETURN	;SET UP FOR POWER FAIL BEFORE
1219								;TESTING STARTS
1220	001612	105737	001310			TSTB	INIFLG	;HAS INITIALIZATION BEEN PERFORMED
1221	001616	001075				BNE	12\$	
1222	001620	104402	001000			TYPE	.MTITLE	;TYPE TITLE MESSAGE
1223	001624	105137	001310			COMB	INIFLG	;IF NOT SET FLAG AND DO
1224								
1225	001630	012737	177570	001200		MOV	#DSWR,SWR	;MOV HARDWARE SWR TO SWR
1226	001636	012737	177570	001202		MOV	#DLIGHTS,LIGHTS	;MOV DISPLAY LIGHTS TO LIGHTS
1227	001644	013746	000006			MOV	@#6,-(SP)	;SAVE VECTORS
1228	001650	013746	000004			MOV	@#4,-(SP)	
1229	001654	012737	001674	000004		MOV	#64\$,@#4	;SET UP FOR TIMEOUT
1230	001662	022777	177777	177310		CMP	#-1,@SWR	;REFERENCE HARDWARE SWITCH REGISTER
1231	001670	001402				BEQ	65\$	
1232	001672	000407				BR	66\$	
1233	001674	022526			64\$:	CMP	(SP)+,(SP)+	;ADJUST STACK
1234	001676	012737	000176	001200	65\$:	MOV	#SWREG,SWR	;POINT TO SOFTWARE SWITCH REG
1235	001704	012737	000174	001202		MOV	#DISPREG,LIGHTS	;POINT TO SOFT DISPLAY REG
1236	001712	012637	000004		66\$:	MOV	(SP)+,@#4	;RESTORE VECTORS
1237	001716	012637	000006			MOV	(SP)+,@#6	
1238	001722	005737	000042			TST	@#42	;UNDER MONITOR
1239	001726	001005				BNE	67\$	
1240	001730	022737	000176	001200		CMP	#SWREG,SWR	;IS SWREG USED
1241	001736	001001				BNE	67\$	
1242	001740	104415				CNTLU		
1243	001742	105777	177232		67\$:	TSTB	@SWR	
1244	001746	100402				BMI	+.6	
1245	001750	004737	000220			JSR	PC,CSRMAP	
1246	001754	104402	015412			TYPE	.XHEAD	
1247	001760	012737	001400	001244		MOV	#1400,TEMP1	
1248	001766	017737	177252	001246		MOV	@TEMP1,TEMP2	
1249	001774	001406				BEQ	+.16	
1250	001776	104410				CONVRT		
1251	002000	015440				XSTATQ		
1252	002002	062737	000002	001244		ADD	#2,TEMP1	
1253	002010	000766				BR	.-22	
1254	002012	032777	000001	177160	12\$:	BIT	#SW00,@SWR	
1255	002020	001424				BEQ	1\$	
1256	002022	104402				TYPE		
1257	002024	015333				MNEW		
1258	002026	005000				CLR	RG	
1259	002030	000000				HALT		
1260	002032	104414				CKSWR		
1261	002034	027737	177140	001502		CMP	@SWR,SAVACT	

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1262 002042 101404 BLOS 11$
1263 002044 104402 TYPE
1264 002046 015174 MERR3
1265 002050 000000 HALT
1266 002052 000776 BR -2
1267 002054 017737 177120 001500 11$: MOV @SWR,DQACTV
1268 002062 013700 001500 MOV DQACTV,R0
1269 002066 000000 HALT
1270 002070 104414 CKSWR
1271 002072 012700 000300 1$: MOV #300,R0
1272 002076 012701 000302 MOV #302,R1
1273 002102 010120 2$: MOV R1,(R0)+
1274 002104 005021 CLR (R1)+
1275 002106 022021 CMP (R0)+,(R1)+
1276 002110 022700 001000 CMP #1000,R0
1277 002114 001372 BNE 2$
1278
1279 ;TEST START AND RESTART
1280
1281 002116 012737 000340 177776 .BEGIN: MOV #340,PS ;LOCK OUT INTERRUPTS
1282 002124 012706 001200 MOV #STACK,SP ;SET UP STACK
1283 002130 005737 000042 TST @#42 ;IS PROGRAM UNDER MONITOR CONTROL
1284 002134 001040 BNE 3$
1285 002136 104414 CKSWR ;CHECK FOR <↑G>
1286 002140 032777 000004 177032 BIT #BIT2,@SWR ;CHECK FOR LOCK ON TEST
1287 002146 001411 BEQ 1$
1288 002150 104402 015232 TYPE .MLOCK
1289 002154 012737 000240 013046 MOV #NOP,TTST
1290 002162 012737 000240 013050 MOV #NOP,TTST+2 ;SET UP TO LOCK
1291 002170 000406 BR 2$
1292 002172 013737 013144 013046 1$: MOV BRW,TTST
1293 002200 013737 013146 013050 MOV BRX,TTST+2 ;LOCK NOT SELECTED. SET UP FOR NORMAL SCOPE LOOP
1294 002206 032777 000002 176764 2$: BIT #SW01,@SWR ;IF SW01=1, GET STARTING PC
1295 002214 001410 BEQ 3$
1296 002216 104403 INSTR
1297 002220 015220 MTSTPC
1298 002222 104405 PARAM
1299 002224 002254 TST1
1300 002226 012442 TLAST
1301 002230 000207 RETURN
1302 002232 001 .BYTE 1
1303 002233 001 .BYTE 1
1304 002234 000403 BR 4$
1305 002236 012737 002254 001214 3$: MOV #TST1,RETURN ;START AT TEST 1
1306 002244 104402 015122 4$: TYPE MR ;TYPE R
1307 002250 000177 176740 JMP @RETURN ;START TESTING
1308
1309 ; TEST 1
1310 002254 012737 000001 001226 *TST1: MOV #1,TSTNO
1311 002262 012737 002644 001214 MOV #TST2,RETURN
1312 002270 012737 002644 001216 MOV #TST2,NEXT
1313 002276 105737 001302 TSTB RUNFLG ;IS THIS MY FIRST TIME HERE?
1314 002302 001010 BNE 1$ ;BR IF FLAG IS SET
1315 002304 012737 000001 001304 MOV #BIT0,RUN ;SET RUN POINTER.
1316 002312 012737 000020 001306 MOV #16,RUNCNT ;SET FOR MAX OF 16 DQ11'S PER SYSTEM
1317 002320 105137 001302 COMB RUNFLG ;SET RUN FLAG

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1318	002324	033737	001304	001500	18:	BIT	RUN,DQACTV	: FIND AN ACTIVE DQ11 TO TEST.
1319	002332	001032				BNE	38	: BR IF I FOUND ONE TO TEST.
1320	002337	005737	001500			TST	DQACTV	: FIND OUT IF THERE ARE NO DQ11 ACTIVE.
1321	002340	001423				BEG	28	: BR TO FATAL ERROR. WHY AM I HERE IF NO ACTIVE DQ11'S???
1322	002342	000257				CCC		: CLEAR ALL THE CONDITION CODES OF CPU
1323	002344	006137	001304			ROL	RUN	: UPDATE RUN POINTER
1324	002350	062737	000004	001300		ADD	#4,CREAM	: UPDATE ADDRESS POINTER.
1325	002356	005337	001306			DEC	RUNCNT	: DEC NUMBER OF TIMES I LOOKED AT ACTIVE.
1326	002364	001360				BNE	18	: BR AND KEEP LOOKING.
1327	002374	012737	000020	001306		MOV	#16,RUNCNT	: START RESTORING MY POINTERS.
1328	002372	012737	001400	001300		MOV	#1400,CREAM	: RESTORE ADDRESS POINTER
1329	002400	012737	000001	001304		MOV	#1,RUN	: RESTORE RUN POINTER.
1330	002406	000746				BR	18	: KEEP ON TESTING.
1331	002410	104402			28:	TYPE		: ALERT OPERATOR OF FATAL ERROR
1332	002412	015125				MERR2		: NO DQ11 ACTIVE. WHY AM I HERE???
1333	002414	000000				HALT		: YOU MUST RELOAD DQ11 DIAGNOSTIC!!
1334	002416	000776				BR	.-2	: STICK HERE ON CONT.
1335	002420	000257			38:	CCC		: CLEAR CPU COND. CODES
1336	002422	006137	001304			ROL	RUN	: UPDATE RUN. ACTIVE DQ11 FOUND.
1337	002426	017737	176646	001506		MOV	#CREAM,DQCSR	: PLACE ADDRESS OF DQ11 AT DQCSR
1338	002434	062737	000002	001300		ADD	#2,CREAM	: UPDATE ADDRESS POINTER
1339	002442	017737	176632	001510		MOV	#CREAM,DQSTAT	: PLACE STATUS OF DQ11 AT DQSTAT
1340	002450	062737	000002	001300		ADD	#2,CREAM	: UPDATE ADDRESS POINTER
1341	002456	013737	001506	001360		MOV	DQCSR,DQCSR	
1342	002464	013737	001510	001350		MOV	DQSTAT,DQVEC	
1343	002472	042737	177007	001350		BIC	#177007,DQVEC	
1344	002500	013737	001350	001350		MOV	DQVEC,DQRLVL	: GENERATE ADDRESS OF RECEIVER INTERRUPT SERVICE PS
1345	002506	062737	000002	001354		ADD	#2,DQRLVL	
1346	002514	013737	001352	001354		MOV	DQRLVL,DQTEC	: GENERATE ADDRESS OF TRANSMITTER INTERRUPT VECTOR
1347	002522	062737	000002	001354		ADD	#2,DQTEC	
1348	002530	013737	001354	001356		MOV	DQTEC,DQTLVL	: GENERATE ADDRESS OF TRANSMITTER INTERRUPT SERVICE PS
1349	002536	062737	000002	001356		ADD	#2,DQTLVL	
1350	002544	013737	001360	001362		MOV	DQCSR,DQCSH	
1351	002552	005237	001362			INC	DQCSH	: GENERATE ADDRESS OF HIGH BYTE
1352	002556	013737	001360	001364		MOV	DQCSR,DQCSR	: GENERATE ADDRESS OF TRANSMITTER CONTROL REGISTER
1353	002564	062737	000002	001364		ADD	#2,DQCSR	
1354	002572	013737	001364	001366		MOV	DQCSR,DQERR	: GENERATE ADDRESS OF ERROR REGISTER
1355	002580	062737	000002	001366		ADD	#2,DQERR	
1356	002606	013737	001366	001370		MOV	DQERR,DQREG	: GENERATE ADDRESS OF HIGH BYTE OF ERROR REGISTER
1357	002614	005237	001370			INC	DQREG	
1358	002620	013737	001370	001372		MOV	DQREG,DQSEC	: GENERATE ADDRESS OF SECONDARY REGISTER
1359	002626	005237	001372			INC	DQSEC	
1360	002632	013737	001372	001374		MOV	DQSEC,DQSECH	: GENERATE ADDRESS OF HIGH BYTE
1361	002640	005237	001374			INC	DQSECH	

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:STEP MODE VERIFICATION AND CLOCK LOSS TEST
:SET STEP MODE
:SET RECEIVER GO
:SET TRANSMITTER GO
:EXPECTED RESULTS (AFTER DELAY)
:TRANSMITTER CLOCK LOSS = 1
:RECEIVER CLOCK LOSS = 1
:****NOTE: AS THE "CLOCK UP" OCCURS
:AN "NPR" SHOULD BE EXECUTED.
:THEREFORE IF THE DQ11 IS GOING TO "HANG"
:THE BUS DUE TO NPR'S THIS IS THE
:FIRST TEST IT WILL HAPPEN IN!!****

: TEST 2

002644 012737 000002 001226
002652 012737 000010 001222
002660 012737 003014 001216
002666 012737 000340 177776
002674 104413
002676 104412
002700 005037 001244
002704 012727 000010 001246
002712 112777 000012 176450
002720 012777 000002 176444
002726 012777 010001 176424
002734 012777 000001 176422
002742 005277 176424
002746 005377 176420
002752 005237 001244
002756 001375
002760 042777 010000 176372
002766 005337 001246
002772 001367
002774 012705 000003
003000 117704 176362
003004 020504
003006 001401
003010 104013
003012 104400

TST2: MOV #2,TSTNO
MOV #10,ICOUNT
MOV #TST3,NEXT
MOV #340,PS
MEMCLR ;LOCK OUT INTERRUPTS
MSTCLR ;CLEAR MEMORY
CLR TEMP1 ;INIT DQ11
MOV #10,TEMP2 ;ZERO DELAY COUNTER
MOVB #12,DQREG ;DELAY 9 X 65535 TIMES
MOV #BIT1,DQSEC ;SELECT MISC REG
MOV #BIT12+BIT0,DQRCR ;SET AUTO STEP
MOV #BIT0,DQTCR ;SET RX GO!!
MOV #BIT0,DQTCR ;SET TX GO!!
INC DQSEC ;CLOCK UP!!
DEC DQSEC ;CLOCK DN!!
INC TEMP1 ;DO THE DELAY....
BNE 15 ;DELAY
BIC #BIT12,DQRCR ;CLEAR RX ACTIVE
DEC TEMP2 ;DELAY:.....
BNE 15 ;DELAY
MOV #3,R5 ;SET FOR EXPECTED
MOVB DQERR,R4 ;READ THE DQERR REGISTER (SEL4)
CMP R5,R4 ;CLOCK LOSS WORKING??
BEQ 25 ;BR IF YES.
HLT 13 ;TX AND RX CLOCK LOSS ERROR
15: SCOPE ;SCOPE THIS TEST.
:TEST LOOP VERIFICATION
:SET STEP MODE AND TEST LOOP
:SET RECEIVER GO
:SET TRANSMITTER GO
:EXPECTED RESULTS (AFTER DELAY)
:TRANSMITTER CLOCK LOSS=0
:RECEIVER CLOCK LOSS=0
25:

: TEST 3

003014 012737 000003 001226
003022 012737 000010 001222
003030 012737 003142 001216
003036 104413
003040 012737 000340 177776

TST3: MOV #3,TSTNO
MOV #10,ICOUNT
MOV #TST4,NEXT
MEMCLR
MOV #340,PS ;SET PS =7 LOCK OUT INTERRUPTS

1418	003046	104412			MSTCLR		:INIT DQ11
1419	003050	005037	001244		CLR	TEMP1	:SET DELAY COUNTER TO 0
1420	003054	012737	000010	001246	MOV	#10,TEMP2	:SET FOR 8 X 65535 TIME DELAY
1421	003062	112777	000012	176300	MOVB	#12,DQREG	:SELECT MISC REGISTER
1422	003070	012777	000012	176274	MOV	#BIT1+BIT3,DQSEC	:SET TESTLOOP AND AUTO/STEP
1423	003076	012777	000001	176254	MOV	#BIT0,DQRCR	:SET RX GO.
1424	003104	012777	000001	176252	MOV	#BIT0,DGTCSR	:SET TX GO.
1425	003112	005237	001244		INC	TEMP1	:D
1426	003116	001375			SNE	1\$:E
1427	003120	005337	001246		DEC	TEMP2	:L
1428	003124	001372			BNE	1\$:A
1429							:Y
1430	003126	005005			CLR	R5	:SET EXPECTED
1431	003130	117704	176232		MOVB	DQERR,R4	:GET ACTUAL
1432	003134	001401			BEQ	2\$:BR IF LOW BYTE OF DQERR IS 0
1433	003136	104013			HLT	13	:DQ11 ERROR REG NOT 0
1434	003140	104400			2\$: SCOPE		:SCOPE THIS TEST.

E03

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: INDIVIDUAL INTERRUPT ENABLE TESTS
: SET SELECTED INTERRUPT ENABLE
: VERIFY THAT NO INTERRUPT OCCURS

: INTERRUPT LOGIC TEST
: SET CHARACTER DETECT INTERRUPT ENABLE
: VERIFY THAT NO INTERRUPT OCCURS

: TEST 4

:*****

003142 012737 000004 001226
003150 012737 003226 001216
003156 104412
003160 004737 016042
003164 003206
003166 003212
003170 052777 000020 176162
003176 005037 177776
003202 000240
003204 000403
003206 104003
003210 000401
003212 104002
003214 012706 001200
003220 004737 016074
003224 104400

TST4: MOV #4,TSTNO
MOV #TST5,NEXT
MSTCLR
JSR PC,SETV
1\$
2\$
BIS #BIT4,DQRCR
CLR PS
NOP
BR 3\$
1\$: HLT 3
BR 3\$
2\$: HLT 2
3\$: MOV #STACK,SP
JSR PC,RECAT
4\$: SCOPE

: CLEAR INTERFACE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 1\$
: TRANSMITTER WILL INTERRUPT TO 2\$
: SET CHARACTER DETECT INTERRUPT ENABL
: SET PROCESSOR PRIORITY TO 0
: WINDOW FOR INTERRUPTS
: UNEXPECTED RECEIVER INTERRUPT
: UNEXPECTED TRANSMITTER INTERRUPT
: RESTORE STACK
: RESTORE TRAPCATCHER
: CHECK FOR ITERATIONS, LOOP

: INTERRUPT LOGIC TEST
: SET RECEIVE DONE INTERRUPT ENABLE
: VERIFY THAT NO INTERRUPT OCCURS

: TEST 5

:*****

003226 012737 000005 001226
003234 012737 003312 001216
003242 104412
003244 004737 016042
003250 003272
003252 003276
003254 052777 000040 176076
003262 005037 177776
003266 000240
003270 000403
003272 104003
003274 000401
003276 104002
003300 012706 001200
003304 004737 016074
003310 104400

TST5: MOV #5,TSTNO
MOV #TST6,NEXT
MSTCLR
JSR PC,SETV
1\$
2\$
BIS #BITS,DQRCR
CLR PS
NOP
BR 3\$
1\$: HLT 3
BR 3\$
2\$: HLT 2
3\$: MOV #STACK,SP
JSR PC,RECAT
4\$: SCOPE

: CLEAR INTERFACE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 1\$
: TRANSMITTER WILL INTERRUPT TO 2\$
: SET RECEIVE DONE INTERRUPT ENABL
: SET PROCESSOR PRIORITY TO 0
: WINDOW FOR INTERRUPTS
: UNEXPECTED RECEIVER INTERRUPT
: UNEXPECTED TRANSMITTER INTERRUPT
: RESTORE STACK
: RESTORE TRAPCATCHER
: CHECK FOR ITERATIONS, LOOP

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABLE
: VERIFY THAT NO INTERRUPT OCCURS

: TEST 6

```

1491
1492 003312 012737 000006 001226 *****
1493 003320 012737 003376 001216 TST6: MOV #6,TSTNO
1494 003326 104412 MSTCLR ;CLEAR INTERFACE
1495 003330 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1496 003334 003356 1$ ;RECEIVER WILL INTERRUPT TO 1$
1497 003336 003362 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1498 003340 052777 000010 176016 BIS #BIT3,ADQTCR ;SET ERROR INTERRUPT ENABL
1499 003346 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1500 003352 000240 NOP ;WINDOW FOR INTERRUPTS
1501 003354 000403 BR 3$
1502 003356 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1503 003360 000401 BR 3$
1504 003362 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1505 003364 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
1506 003370 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1507 003374 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
1508
1509 ; INTERRUPT LOGIC TEST
1510 ; SET DATASET INTERRUPT ENABLE
1511 ; VERIFY THAT NO INTERRUPT OCCURS
1512
1513 ; TEST 7
1514 *****
1515 003376 012737 000007 001226 TST7: MOV #7,TSTNO
1516 003404 012737 003462 001216 MOV #TST10,NEXT
1517 003412 104412 MSTCLR ;CLEAR INTERFACE
1518 003414 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1519 003420 003442 1$ ;RECEIVER WILL INTERRUPT TO 1$
1520 003422 003446 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1521 003424 052777 000020 175732 BIS #BIT4,ADQTCR ;SET DATASET INTERRUPT ENABL
1522 003432 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1523 003436 000240 NOP ;WINDOW FOR INTERRUPTS
1524 003440 000403 BR 3$
1525 003442 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1526 003444 000401 BR 3$
1527 003446 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1528 003450 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
1529 003454 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1530 003460 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
1531
1532 ; INTERRUPT LOGIC TEST
1533 ; SET TRANSMIT DONE INTERRUPT ENABLE
1534 ; VERIFY THAT NO INTERRUPT OCCURS
1535
1536 ; TEST 10
1537 *****
1538 003462 012737 000010 001226 TST10: MOV #10,TSTNO
1539 003470 012737 003546 001216 MOV #TST11,NEXT
1540 003476 104412 MSTCLR ;CLEAR INTERFACE
1541 003500 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1542 003504 003526 1$ ;RECEIVER WILL INTERRUPT TO 1$
1543 003506 003532 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1544 003510 052777 000040 175646 BIS #BIT5,ADQTCR ;SET TRANSMIT DONE INTERRUPT ENABL
1545 003516 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1546 003522 000240 NOP ;WINDOW FOR INTERRUPTS

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1547 003524 000403 BR 3$
1548 003526 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1549 003530 000401 BR 3$
1550 003532 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1551 003534 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
1552 003540 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1553 003544 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
1554
1555 ; INDIVIDUAL INTERRUPT FLAG TESTS
1556 ; SET SELECTED INTERRUPT FLAG
1557 ; VERIFY THAT NO INTERRUPT OCCURS
1558
1559
1560 ; INTERRUPT LOGIC TEST
1561 ; SET RECEIVE DONE S INTERRUPT FLAG
1562 ; VERIFY THAT NO INTERRUPT OCCURS
1563
1564 : TEST 11
1565 :*****
1566 003546 012737 000011 001226 †ST11: MOV #11,TSTNO
1567 003554 012737 003632 001216 MOV #TST12,NEXT
1568 003562 104412 MSTCLR ;CLEAR INTERFACE
1569 003564 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1570 003570 003612 1$ ;RECEIVER WILL INTERRUPT TO 1$
1571 003572 003616 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1572 003574 052777 000100 175556 BIS #BIT6,JDQRCR ;SET RECEIVE DONE S INTERRUPT FLAG
1573 003602 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1574 003606 000240 NOP ;WINDOW FOR INTERRUPTS
1575 003610 000403 BR 3$
1576 003612 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1577 003614 000401 BR 3$
1578 003616 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1579 003620 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
1580 003624 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
1581 003630 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
1582
1583 ; INTERRUPT LOGIC TEST
1584 ; SET RECEIVE DONE P INTERRUPT FLAG
1585 ; VERIFY THAT NO INTERRUPT OCCURS
1586
1587 : TEST 12
1588 :*****
1589 003632 012737 000012 001226 †ST12: MOV #12,TSTNO
1590 003640 012737 003716 001216 MOV #TST13,NEXT
1591 003646 104412 MSTCLR ;CLEAR INTERFACE
1592 003650 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
1593 003654 003676 1$ ;RECEIVER WILL INTERRUPT TO 1$
1594 003656 003702 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
1595 003660 052777 000200 175472 BIS #BIT7,JDQRCR ;SET RECEIVE DONE P INTERRUPT FLAG
1596 003666 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
1597 003672 000240 NOP ;WINDOW FOR INTERRUPTS
1598 003674 000403 BR 3$
1599 003676 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
1600 003700 000401 BR 3$
1601 003702 104002 2$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
1602 003704 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK

```

```

1603 003710 004737 016074          JSR    PC,RECAT          ;RESTORE TRAPCATCHER
1604 003714 104400          4$:    SCOPE              ;CHECK FOR ITERATIONS, LOOP
1605
1606          ; INTERRUPT LOGIC TEST
1607          ; SET TRANSMIT DONE S INTERRUPT FLAG
1608          ; VERIFY THAT NO INTERRUPT OCCURS
1609
1610          ; TEST 13
1611          ;*****
1612 003716 012737 000013 001226  TST13: MOV    #13,TSTNO
1613 003724 012737 004002 001216      MOV    #TST14,NEXT
1614 003732 104412          MSTCLR
1615 003734 004737 016042          JSR    PC,SETV          ;CLEAR INTERFACE
1616 003740 003762          1$    ;SET UP INTERRUPT VECTORS
1617 003742 003766          2$    ;RECEIVER WILL INTERRUPT TO 1$
1618 003744 052777 000100 175412  BIS    #BIT6,ADQTCR    ;TRANSMITTER WILL INTERRUPT TO 2$
1619 003752 005037 177776          CLR    PS              ;SET TRANSMIT DONE S INTERRUPT FLAG
1620 003756 000240          NOP                    ;SET PROCESSOR PRIORITY TO 0
1621 003760 000403          BR     3$              ;WINDOW FOR INTERRUPTS
1622 003762 104003          1$:   HLT    3          ;UNEXPECTED RECEIVER INTERRUPT
1623 003764 000401          BR     3$
1624 003766 104002          2$:   HLT    2          ;UNEXPECTED TRANSMITTER INTERRUPT
1625 003770 012706 001200          3$:   MOV    #STACK,SP  ;RESTORE STACK
1626 003774 004737 016074          JSR    PC,RECAT        ;RESTORE TRAPCATCHER
1627 004000 104400          4$:   SCOPE              ;CHECK FOR ITERATIONS, LOOP
1628
1629          ; INTERRUPT LOGIC TEST
1630          ; SET RECEIVE DONE S INTERRUPT FLAG
1631          ; VERIFY THAT NO INTERRUPT OCCURS
1632
1633          ; TEST 14
1634          ;*****
1635 004002 012737 000014 001226  TST14: MOV    #14,TSTNO
1636 004010 012737 004066 001216      MOV    #TST15,NEXT
1637 004016 104412          MSTCLR
1638 004020 004737 016042          JSR    PC,SETV          ;CLEAR INTERFACE
1639 004024 004046          1$    ;SET UP INTERRUPT VECTORS
1640 004026 004052          2$    ;RECEIVER WILL INTERRUPT TO 1$
1641 004030 052777 000200 175326  BIS    #BIT7,ADQTCR    ;TRANSMITTER WILL INTERRUPT TO 2$
1642 004036 005037 177776          CLR    PS              ;SET RECEIVE DONE S INTERRUPT FLAG
1643 004042 000240          NOP                    ;SET PROCESSOR PRIORITY TO 0
1644 004044 000403          BR     3$              ;WINDOW FOR INTERRUPTS
1645 004046 104003          1$:   HLT    3          ;UNEXPECTED RECEIVER INTERRUPT
1646 004050 000401          BR     3$
1647 004052 104002          2$:   HLT    2          ;UNEXPECTED TRANSMITTER INTERRUPT
1648 004054 012706 001200          3$:   MOV    #STACK,SP  ;RESTORE STACK
1649 004060 004737 016074          JSR    PC,RECAT        ;RESTORE TRAPCATCHER
1650 004064 104400          4$:   SCOPE              ;CHECK FOR ITERATIONS, LOOP
1651
1652          ; INTERRUPT LOGIC TEST
1653          ; SET DATA SET INTERRUPT FLAG
1654          ; VERIFY THAT NO INTERRUPT OCCURS
1655
1656          ; TEST 15
1657          ;*****
1658 004066 012737 000015 001226  TST15: MOV    #15,TSTNO
    
```

```

1659 004074 012737 004152 001216      MOV      #TST16,NEXT
1660 004102 104412      MSTCLR
1661 004104 004737 016042      JSR      PC,SETV
1662 004110 004132      1$
1663 004112 004136      2$
1664 004114 052777 100000 175242      BIS      #BIT15,JDQTCR
1665 004122 005037 177776      CLR      PS
1666 004126 000240      NOP
1667 004130 000403      BR      3$
1668 004132 104003      1$: HLT      3
1669 004134 000401      BR      3$
1670 004136 104002      2$: HLT      2
1671 004140 012706 001200      3$: MOV      #STACK,SP
1672 004144 004737 016074      JSR      PC,RECAT
1673 004150 104400      4$: SCOPE

```

```

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1$
;TRANSMITTER WILL INTERRUPT TO 2$
;SET DATA SET INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;UNEXPECTED RECEIVER INTERRUPT
;UNEXPECTED TRANSMITTER INTERRUPT
;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET T CLOCK LOSS INTERRUPT FLAG
; VERIFY THAT NO INTERRUPT OCCURS

```

; TEST 16

```

1681 004152 012737 000016 001226  TST16: MOV      #16,TSTNO
1682 004160 012737 004236 001216      MOV      #TST17,NEXT
1683 004166 104412      MSTCLR
1684 004170 004737 016042      JSR      PC,SETV
1685 004174 004216      1$
1686 004176 004222      2$
1687 004200 052777 000001 175160      BIS      #BIT0,JDQERR
1688 004206 005037 177776      CLR      PS
1689 004212 000240      NOP
1690 004214 000403      BR      3$
1691 004216 104003      1$: HLT      3
1692 004220 000401      BR      3$
1693 004222 104002      2$: HLT      2
1694 004224 012706 001200      3$: MOV      #STACK,SP
1695 004230 004737 016074      JSR      PC,RECAT
1696 004234 104400      4$: SCOPE

```

```

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1$
;TRANSMITTER WILL INTERRUPT TO 2$
;SET T CLOCK LOSS INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;UNEXPECTED RECEIVER INTERRUPT
;UNEXPECTED TRANSMITTER INTERRUPT
;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET R CLOCK LOSS INTERRUPT FLAG
; VERIFY THAT NO INTERRUPT OCCURS

```

; TEST 17

```

1704 004236 012737 000017 001226  TST17: MOV      #17,TSTNO
1705 004244 012737 004322 001216      MOV      #TST20,NEXT
1706 004252 104412      MSTCLR
1707 004254 004737 016042      JSR      PC,SETV
1708 004260 004302      1$
1709 004262 004306      2$
1710 004264 052777 000002 175074      BIS      #BIT1,JDQERR
1711 004272 005037 177776      CLR      PS
1712 004276 000240      NOP
1713 004300 000403      BR      3$
1714 004302 104003      1$: HLT      3

```

```

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1$
;TRANSMITTER WILL INTERRUPT TO 2$
;SET R CLOCK LOSS INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;UNEXPECTED RECEIVER INTERRUPT

```

```

1715 004304 000401          BR      3$
1716 004306 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1717 004310 012706 001200        3$:    MOV      #STACK,SP ;RESTORE STACK
1718 004314 004737 016074          JSR      PC,RECAT ;RESTORE TRAPCATCHER
1719 004320 104400          4$:    SCOPE ;CHECK FOR ITERATIONS, LOOP
1720
1721          ; INTERRUPT LOGIC TEST
1722          ; SET T LATENCY INTERRUPT FLAG
1723          ; VERIFY THAT NO INTERRUPT OCCURS
1724
1725          ; TEST 20
1726          ; *****
1727 004322 012737 000020 001226 1727:  MOV      #20,TSTNO
1728 004330 012737 004406 001216 1728:  MOV      #TST21,NEXT
1729 004336 104412          MSTCLR ;CLEAR INTERFACE
1730 004340 004737 016042          JSR      PC,SETV ;SET UP INTERRUPT VECTORS
1731 004344 004366          1$:    ;RECEIVER WILL INTERRUPT TO 1$
1732 004346 004372          2$:    ;TRANSMITTER WILL INTERRUPT TO 2$
1733 004350 052777 000004 175010 1733:  BIS      #BIT2,JDQERR ;SET T LATENCY INTERRUPT FLAG
1734 004356 005037 177776          CLR      PS ;SET PROCESSOR PRIORITY TO 0
1735 004362 000240          NOP ;WINDOW FOR INTERRUPTS
1736 004364 000403          BR      3$
1737 004366 104003          1$:    HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1738 004370 000401          BR      3$
1739 004372 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1740 004374 012706 001200        3$:    MOV      #STACK,SP ;RESTORE STACK
1741 004400 004737 016074          JSR      PC,RECAT ;RESTORE TRAPCATCHER
1742 004404 104400          4$:    SCOPE ;CHECK FOR ITERATIONS, LOOP
1743
1744          ; INTERRUPT LOGIC TEST
1745          ; SET R LATENCY INTERRUPT FLAG
1746          ; VERIFY THAT NO INTERRUPT OCCURS
1747
1748          ; TEST 21
1749          ; *****
1750 004406 012737 000021 001226 1750:  MOV      #21,TSTNO
1751 004414 012737 004472 001216 1751:  MOV      #TST22,NEXT
1752 004422 104412          MSTCLR ;CLEAR INTERFACE
1753 004424 004737 016042          JSR      PC,SETV ;SET UP INTERRUPT VECTORS
1754 004430 004452          1$:    ;RECEIVER WILL INTERRUPT TO 1$
1755 004432 004456          2$:    ;TRANSMITTER WILL INTERRUPT TO 2$
1756 004434 052777 000010 174724 1756:  BIS      #BIT3,JDQERR ;SET R LATENCY INTERRUPT FLAG
1757 004442 005037 177776          CLR      PS ;SET PROCESSOR PRIORITY TO 0
1758 004446 000240          NOP ;WINDOW FOR INTERRUPTS
1759 004450 000403          BR      3$
1760 004452 104003          1$:    HLT      3          ;UNEXPECTED RECEIVER INTERRUPT
1761 004454 000401          BR      3$
1762 004456 104002          2$:    HLT      2          ;UNEXPECTED TRANSMITTER INTERRUPT
1763 004460 012706 001200        3$:    MOV      #STACK,SP ;RESTORE STACK
1764 004464 004737 016074          JSR      PC,RECAT ;RESTORE TRAPCATCHER
1765 004470 104400          4$:    SCOPE ;CHECK FOR ITERATIONS, LOOP
1766
1767          ; INTERRUPT LOGIC TEST
1768          ; SET T NON-EX MEM INTERRUPT FLAG
1769          ; VERIFY THAT NO INTERRUPT OCCURS
1770

```

```

1771      ; TEST 22
1772      ;*****
1773 004472 012737 000022 001226 TST22: MOV #22,TSTNO
1774 004500 012737 004556 001216      MOV #TST23,NEXT
1775 004506 104412      MSTCLR      ;CLEAR INTERFACE
1776 004510 004737 016042      JSR PC,SETV ;SET UP INTERRUPT VECTORS
1777 004514 004536      1$          ;RECEIVER WILL INTERRUPT TO 1$
1778 004516 004542      2$          ;TRANSMITTER WILL INTERRUPT TO 2$
1779 004520 052777 000020 174640      BIS #BIT4,ADQERR ;SET T NON-EX MEM INTERRUPT FLAG
1780 004526 005037 177776      CLR PS      ;SET PROCESSOR PRIORITY TO 0
1781 004532 000240      NOP        ;WINDOW FOR INTERRUPTS
1782 004534 000403      BR 3$
1783 004536 104003      1$: HLT 3      ;UNEXPECTED RECEIVER INTERRUPT
1784 004540 000401      BR 3$
1785 004542 104002      2$: HLT 2      ;UNEXPECTED TRANSMITTER INTERRUPT
1786 004544 012706 001200      3$: MOV #STACK,SP ;RESTORE STACK
1787 004550 004737 016074      JSR PC,RECAT ;RESTORE TRAPCATCHER
1788 004554 104400      4$: SCOPE    ;CHECK FOR ITERATIONS, LOOP
1789
1790      ; INTERRUPT LOGIC TEST
1791      ; SET R NON-EX MEM INTERRUPT FLAG
1792      ; VERIFY THAT NO INTERRUPT OCCURS
1793
1794      ; TEST 23
1795      ;*****
1796 004556 012737 000023 001226 TST23: MOV #23,TSTNO
1797 004564 012737 004642 001216      MOV #TST24,NEXT
1798 004572 104412      MSTCLR      ;CLEAR INTERFACE
1799 004574 004737 016042      JSR PC,SETV ;SET UP INTERRUPT VECTORS
1800 004600 004622      1$          ;RECEIVER WILL INTERRUPT TO 1$
1801 004602 004626      2$          ;TRANSMITTER WILL INTERRUPT TO 2$
1802 004604 052777 000040 174554      BIS #BIT5,ADQERR ;SET R NON-EX MEM INTERRUPT FLAG
1803 004612 005037 177776      CLR PS      ;SET PROCESSOR PRIORITY TO 0
1804 004616 000240      NOP        ;WINDOW FOR INTERRUPTS
1805 004620 000403      BR 3$
1806 004622 104003      1$: HLT 3      ;UNEXPECTED RECEIVER INTERRUPT
1807 004624 000401      BR 3$
1808 004626 104002      2$: HLT 2      ;UNEXPECTED TRANSMITTER INTERRUPT
1809 004630 012706 001200      3$: MOV #STACK,SP ;RESTORE STACK
1810 004634 004737 016074      JSR PC,RECAT ;RESTORE TRAPCATCHER
1811 004640 104400      4$: SCOPE    ;CHECK FOR ITERATIONS, LOOP
1812
1813      ; INTERRUPT LOGIC TEST
1814      ; SET R BCC ERROR INTERRUPT FLAG
1815      ; VERIFY THAT NO INTERRUPT OCCURS
1816
1817      ; TEST 24
1818      ;*****
1819 004642 012737 000024 001226 TST24: MOV #24,TSTNO
1820 004650 012737 004726 001216      MOV #TST25,NEXT
1821 004656 104412      MSTCLR      ;CLEAR INTERFACE
1822 004660 004737 016042      JSR PC,SETV ;SET UP INTERRUPT VECTORS
1823 004664 004706      1$          ;RECEIVER WILL INTERRUPT TO 1$
1824 004666 004712      2$          ;TRANSMITTER WILL INTERRUPT TO 2$
1825 004670 052777 000100 174470      BIS #BIT6,ADQERR ;SET R BCC ERROR INTERRUPT FLAG
1826 004676 005037 177776      CLR PS      ;SET PROCESSOR PRIORITY TO 0
    
```

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1827 004702 000240      NOP      ;WINDOW FOR INTERRUPTS
1828 004704 000403      BR       3$
1829 004706 104003      1$: HLT  3      ;UNEXPECTED RECEIVER INTERRUPT
1830 004710 000401      BR       3$
1831 004712 104002      2$: HLT  2      ;UNEXPECTED TRANSMITTER INTERRUPT
1832 004714 012706 001200  3$: MOV  #STACK, SP ;RESTORE STACK
1833 004720 004737 016074  JSR  PC, RECAT  ;RESTORE TRAPCATCHER
1834 004724 104400      4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
1835
1836      ; INTERRUPT LOGIC TEST
1837      ; SET R VRC ERROR INTERRUPT FLAG
1838      ; VERIFY THAT NO INTERRUPT OCCURS
1839
1840      ; TEST 25
1841      ; *****
1842 004726 012737 000025 001226  †TST25: MOV  #25, TSTNO
1843 004734 012737 005012 001216  MOV  #TST26, NEXT
1844 004742 104412      MSTCLR ; CLEAR INTERFACE
1845 004744 004737 016042  JSR  PC, SETV  ; SET UP INTERRUPT VECTORS
1846 004750 004772      1$    ; RECEIVER WILL INTERRUPT TO 1$
1847 004752 004776      2$    ; TRANSMITTER WILL INTERRUPT TO 2$
1848 004754 052777 000200 174404  BIS  #BIT7, JDQERR ; SET R VRC ERROR INTERRUPT FLAG
1849 004762 005037 177776  CLR  PS       ; SET PROCESSOR PRIORITY TO 0
1850 004766 000240      NOP    ; WINDOW FOR INTERRUPTS
1851 004770 000403      BR       3$
1852 004772 104003      1$: HLT  3      ; UNEXPECTED RECEIVER INTERRUPT
1853 004774 000401      BR       3$
1854 004776 104002      2$: HLT  2      ; UNEXPECTED TRANSMITTER INTERRUPT
1855 005000 012706 001200  3$: MOV  #STACK, SP ; RESTORE STACK
1856 005004 004737 016074  JSR  PC, RECAT  ; RESTORE TRAPCATCHER
1857 005010 104400      4$: SCOPE ; CHECK FOR ITERATIONS, LOOP
1858
1859      ; INDIVIDUAL INTERRUPT TESTS
1860      ; SET SELECTED INTERRUPT ENABLE AND FLAG
1861      ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT ADDRESS
1862
1863      ; INTERRUPT LOGIC TEST
1864      ; SET CHARACTER DETECT INTERRUPT ENABLE
1865      ; SET CHARACTER DETECT INTERRUPT FLAG
1866      ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
1867
1868      ; TEST 26
1869      ; *****
1870      ; *****
1871 005012 012737 000026 001226  †TST26: MOV  #26, TSTNO
1872 005020 012737 005102 001216  MOV  #TST27, NEXT
1873 005026 104412      MSTCLR ; CLEAR INTERFACE
1874 005030 004737 016042  JSR  PC, SETV  ; SET UP INTERRUPT VECTORS
1875 005034 005064      1$    ; RECEIVER WILL INTERRUPT TO 1$
1876 005036 005066      2$    ; TRANSMITTER WILL INTERRUPT TO 2$
1877 005040 052777 000020 174312  BIS  #BIT4, JDQRCR ; SET CHARACTER DETECT INTERRUPT ENABL
1878 005046 052777 100000 174304  BIS  #BIT15, JDQRCR ; SET CHARACTER DETECT INTERRUPT FLAG
1879 005054 005037 177776  CLR  PS       ; SET PROCESSOR PRIORITY TO 0
1880 005060 000240      NOP    ; WINDOW FOR INTERRUPTS
1881 005062 104000      HLT  0      ; RECEIVER DID NOT INTERRUPT
1882 005064 000401      1$: BR    3$    ; RECEIVER SHOULD INTERRUPT TO THIS LOCATION

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1939
1940
1941
1942
1943
1944
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1946
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;VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

; TEST 31
;*****

```

TST31:  MOV    #31,TSTNO
        MOV    #TST32,NEXT
        MSTCLR
        JSR    PC,SETV
        1$
        2$
        BIS    #BIT5,ADQTCR
        BIS    #BIT6,ADQTCR
        CLR    PS
        NOP
        HLT    1
        BR     3$
1$:     HLT    3
2$:     NOP
3$:     MOV    #STACK,SP
        JSR    PC,RECAT
4$:     SCOPE

```

```

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1$
;TRANSMITTER WILL INTERRUPT TO 2$
;SET TRANSMIT DONE INTERRUPT ENABL
;SET TRANSMIT DONE S INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;TRANSMITTER DID NOT INTERRUPT
;WITH TRANSMIT DONE INTERRUPT ENABL AND
;TRANSMIT DONE S INTERRUPT FLAG SET
;UNEXPECTED RECEIVER INTERRUPT
;TRANSMITTER SHOULD INTERRUPT TO HERE
;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET TRANSMIT DONE INTERRUPT ENABLE
; SET TRANSMIT DONE P INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

; TEST 32
;*****

```

TST32:  MOV    #32,TSTNO
        MOV    #TST33,NEXT
        MSTCLR
        JSR    PC,SETV
        1$
        2$
        BIS    #BIT5,ADQTCR
        BIS    #BIT7,ADQTCR
        CLR    PS
        NOP
        HLT    1
        BR     3$
1$:     HLT    3
2$:     NOP
3$:     MOV    #STACK,SP
        JSR    PC,RECAT
4$:     SCOPE

```

```

;CLEAR INTERFACE
;SET UP INTERRUPT VECTORS
;RECEIVER WILL INTERRUPT TO 1$
;TRANSMITTER WILL INTERRUPT TO 2$
;SET TRANSMIT DONE INTERRUPT ENABL
;SET TRANSMIT DONE P INTERRUPT FLAG
;SET PROCESSOR PRIORITY TO 0
;WINDOW FOR INTERRUPTS
;TRANSMITTER DID NOT INTERRUPT
;WITH TRANSMIT DONE INTERRUPT ENABL AND
;TRANSMIT DONE P INTERRUPT FLAG SET
;UNEXPECTED RECEIVER INTERRUPT
;TRANSMITTER SHOULD INTERRUPT TO HERE
;RESTORE STACK
;RESTORE TRAPCATCHER
;CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET ERROR INTERRUPT ENABLE
; SET T CLOCK LOSS INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

; TEST 33
;*****


```

00000000 005446 012737 000033 001226 TST33: MOV #33,TSTNO
00000000 005446 012737 005540 001216 MOV #TST34,NEXT
00000000 005446 104412 MSTCLR
00000000 005446 004737 016042 JSR PC,SETV
00000000 005446 005532 18 JSR
00000000 005446 005532 18 JSR
00000000 005446 052777 000010 173662 BIS #BIT3,SDQTCR
00000000 005446 052777 000001 173656 BIS #BIT0,SDQERR
00000000 005446 005037 177776 CLR PS
00000000 005446 000240 NOP
00000000 005446 104001 HLT 1
00000000 005446 000402 BR 3$
00000000 005522 104003 1$: HLT 3
00000000 005524 000240 2$: NOP
00000000 005526 012706 3$: MOV #STACK,SP
00000000 005526 004737 016074 JSR PC,RECAT
00000000 005536 104400 4$: SCOPE

```

```

: CLEAR INTERFACE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 1$
: TRANSMITTER WILL INTERRUPT TO 2$
: SET ERROR INTERRUPT ENABL
: SET T CLOCK LOSS INTERRUPT FLAG
: SET PROCESSOR PRIORITY TO 0
: WINDOW FOR INTERRUPTS
: TRANSMITTER DID NOT INTERRUPT
: WITH ERROR INTERRUPT ENABL AND
: T CLOCK LOSS INTERRUPT FLAG SET
: UNEXPECTED RECEIVER INTERRUPT
: TRANSMITTER SHOULD INTERRUPT TO HERE
: RESTORE STACK
: RESTORE TRAPCATCHER
: CHECK FOR ITERATIONS, LOOP

```

```

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABL
: SET R CLOCK LOSS INTERRUPT FLAG
: VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

```

: TEST 34
: *****

```

```

00000000 005540 012737 000034 001226 TST34: MOV #34,TSTNO
00000000 005545 012737 005632 001216 MOV #TST35,NEXT
00000000 005545 104412 MSTCLR
00000000 005545 004737 016042 JSR PC,SETV
00000000 005545 005614 18 JSR
00000000 005545 005614 18 JSR
00000000 005545 052777 000010 173570 BIS #BIT3,SDQTCR
00000000 005545 052777 000002 173564 BIS #BIT1,SDQERR
00000000 005545 005037 177776 CLR PS
00000000 005545 000240 NOP
00000000 005545 104001 HLT 1
00000000 005545 000402 BR 3$
00000000 005614 104003 1$: HLT 3
00000000 005616 000240 2$: NOP
00000000 005620 012706 3$: MOV #STACK,SP
00000000 005624 004737 016074 JSR PC,RECAT
00000000 005630 104400 4$: SCOPE

```

```

: CLEAR INTERFACE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 1$
: TRANSMITTER WILL INTERRUPT TO 2$
: SET ERROR INTERRUPT ENABL
: SET R CLOCK LOSS INTERRUPT FLAG
: SET PROCESSOR PRIORITY TO 0
: WINDOW FOR INTERRUPTS
: TRANSMITTER DID NOT INTERRUPT
: WITH ERROR INTERRUPT ENABL AND
: R CLOCK LOSS INTERRUPT FLAG SET
: UNEXPECTED RECEIVER INTERRUPT
: TRANSMITTER SHOULD INTERRUPT TO HERE
: RESTORE STACK
: RESTORE TRAPCATCHER
: CHECK FOR ITERATIONS, LOOP

```

```

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABL
: SET T LATENCY INTERRUPT FLAG
: VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

```

: TEST 35
: *****

```

```

00000000 005632 012737 000035 001226 TST35: MOV #35,TSTNO
00000000 005640 012737 005724 001216 MOV #TST36,NEXT
00000000 005646 104412 MSTCLR
00000000 005650 004737 016042 JSR PC,SETV

```

```

: CLEAR INTERFACE
: SET UP INTERRUPT VECTORS

```

```
005654 005706 16: HLT 3 :RECEIVER WILL INTERRUPT TO 1$
005655 005710 28: NOP :TRANSMITTER WILL INTERRUPT TO 2$
005656 052777 000010 173476 BIS #BIT3,JDQTCR :SET ERROR INTERRUPT ENABL
005657 052777 000004 173472 BIS #BIT2,JDQERR :SET T LATENCY INTERRUPT FLAG
005658 005037 177776 CLR PS :SET PROCESSOR PRIORITY TO 0
005659 000240 :WINDOW FOR INTERRUPTS
005700 104001 HLT 1 :TRANSMITTER DID NOT INTERRUPT
005702 000402 BR 3$ :WITH ERROR INTERRUPT ENABL AND
005703 104003 :T LATENCY INTERRUPT FLAG SET
005704 000240 16: HLT 3 :UNEXPECTED RECEIVER INTERRUPT
005706 000240 28: NOP :TRANSMITTER SHOULD INTERRUPT TO HERE
005710 012706 001200 38: MOV #STACK,SP :RESTORE STACK
005712 004737 016074 JSR PC,RECAT :RESTORE TRAPCATCHER
005716 104400 48: SCOPE :CHECK FOR ITERATIONS, LOOP
005722
```

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABLE
: SET R LATENCY INTERRUPT FLAG
: VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

: TEST 36
: *****

```
005724 012737 000036 001226 TST36: MOV #36,TSTNO
005732 012737 006016 001216 MOV #TST37,NEXT
005740 104412 MSTCLR
005742 004737 016042 JSR PC,SETV
005746 006000 16: HLT 3 :CLEAR INTERFACE
005750 006002 28: NOP :SET UP INTERRUPT VECTORS
005752 052777 000010 173404 BIS #BIT3,JDQTCR :RECEIVER WILL INTERRUPT TO 1$
005753 052777 000010 173400 BIS #BIT3,JDQERR :TRANSMITTER WILL INTERRUPT TO 2$
005754 005037 177776 CLR PS :SET ERROR INTERRUPT ENABL
005755 000240 :SET R LATENCY INTERRUPT FLAG
005756 104001 HLT 1 :SET PROCESSOR PRIORITY TO 0
005757 000402 BR 3$ :WINDOW FOR INTERRUPTS
006000 104003 16: HLT 3 :TRANSMITTER DID NOT INTERRUPT
006002 000240 28: NOP :WITH ERROR INTERRUPT ENABL AND
006004 012706 001200 38: MOV #STACK,SP :R LATENCY INTERRUPT FLAG SET
006010 004737 016074 JSR PC,RECAT :UNEXPECTED RECEIVER INTERRUPT
006014 104400 48: SCOPE :TRANSMITTER SHOULD INTERRUPT TO HERE
: RESTORE STACK
: RESTORE TRAPCATCHER
: CHECK FOR ITERATIONS, LOOP
```

: INTERRUPT LOGIC TEST
: SET ERROR INTERRUPT ENABLE
: SET T NON-EX MEM INTERRUPT FLAG
: VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

: TEST 37
: *****

```
006016 012737 000037 001226 TST37: MOV #37,TSTNO
006024 012737 006110 001216 MOV #TST40,NEXT
006032 104412 MSTCLR
006034 004737 016042 JSR PC,SETV
006040 006072 16: HLT 3 :CLEAR INTERFACE
006042 006074 28: NOP :SET UP INTERRUPT VECTORS
006044 052777 000010 173312 BIS #BIT3,JDQTCR :RECEIVER WILL INTERRUPT TO 1$
006052 052777 000020 173306 BIS #BIT4,JDQERR :TRANSMITTER WILL INTERRUPT TO 2$
: SET ERROR INTERRUPT ENABL
: SET T NON-EX MEM INTERRUPT FLAG
```

```

2107 006060 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
2108 006064 000240 NOP ;WINDOW FOR INTERRUPTS
2109 006066 104001 HLT 1 ;TRANSMITTER DID NOT INTERRUPT
2110 006070 000402 BR 3$ ;WITH ERROR INTERRUPT ENABL AND
2111 ; T NON-EX MEM INTERRUPT FLAG SET
2112 006072 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
2113 006074 000240 2$: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
2114 006076 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
2115 006102 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
2116 006106 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET ERROR INTERRUPT ENABLE
; SET R NON-EX MEM INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORPECT VECTOR

```

; TEST 40

```

2117 006110 012737 000040 001226 TST40: MOV #40,TSTNO
2118 006116 012737 006202 001216 MOV #TST41,NEXT
2119 006124 104412 MSTCLR ;CLEAR INTERFACE
2120 006126 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
2121 006132 006164 1$ ;RECEIVER WILL INTERRUPT TO 1$
2122 006134 006166 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
2123 006136 052777 000010 173220 BIS #BIT3,JDGTCSR ;SET ERROR INTERRUPT ENABL
2124 006144 052777 000040 173214 BIS #BIT5,JDGERR ;SET R NON-EX MEM INTERRUPT FLAG
2125 006152 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
2126 006156 000240 NOP ;WINDOW FOR INTERRUPTS
2127 006160 104001 HLT 1 ;TRANSMITTER DID NOT INTERRUPT
2128 006162 000402 BR 3$ ;WITH ERROR INTERRUPT ENABL AND
2129 ; R NON-EX MEM INTERRUPT FLAG SET
2130 006164 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
2131 006166 000240 2$: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
2132 006170 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
2133 006174 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
2134 006200 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP

```

```

; INTERRUPT LOGIC TEST
; SET ERROR INTERRUPT ENABLE
; SET R BCC ERROR INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR

```

; TEST 41

```

2135 006202 012737 000041 001226 TST41: MOV #41,TSTNO
2136 006210 012737 006274 001216 MOV #TST42,NEXT
2137 006216 104412 MSTCLR ;CLEAR INTERFACE
2138 006220 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
2139 006224 006256 1$ ;RECEIVER WILL INTERRUPT TO 1$
2140 006226 006260 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
2141 006230 052777 000010 173126 BIS #BIT3,JDGTCSR ;SET ERROR INTERRUPT ENABL
2142 006236 052777 000100 173122 BIS #BIT6,JDGERR ;SET R BCC ERROR INTERRUPT FLAG
2143 006244 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
2144 006250 000240 NOP ;WINDOW FOR INTERRUPTS
2145 006252 104001 HLT 1 ;TRANSMITTER DID NOT INTERRUPT
2146 006254 000402 BR 3$ ;WITH ERROR INTERRUPT ENABL AND

```

```

163          ;R BCC ERROR INTERUPT FLAG SET
164 006256 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
165 006260 000240 2$: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
166 006262 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
167 006266 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
168 006272 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
169
170          ; INTERRUPT LOGIC TEST
171          ; SET ERROR INTERRUPT ENABLE
172          ; SET R VRC ERROR INTERRUPT FLAG
173          ; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
174
175          ; TEST 42
176          ; *****
177 006274 012737 000042 001226 †TST42: MOV #42,TSTNO
178 006302 012737 006366 001216 MOV #TST43,NEXT
179 006310 104412 MSTCLR ; CLEAR INTERFACE
180 006312 004737 016042 JSR PC,SETV ; SET UP INTERRUPT VECTORS
181 006316 006350 1$: ; RECEIVER WILL INTERRUPT TO 1$
182 006320 006352 2$: ; TRANSMITTER WILL INTERRUPT TO 2$
183 006322 052777 000010 173034 BIS #BIT3,ADQTCR ; SET ERROR INTERRUPT ENABL
184 006330 052777 000200 173030 BIS #BIT7,ADQERR ; SET R VRC ERROR INTERRUPT FLAG
185 006336 005037 177776 CLR PS ; SET PROCESSOR PRIORITY TO 0
186 006342 000240 NOP ; WINDOW FOR INTERRUPTS
187 006344 104001 HLT 1 ; TRANSMITTER DID NOT INTERRUPT
188 006346 000402 BR 3$ ; WITH ERROR INTERRUPT ENABL AND
189          ; R VRC ERROR INTERRUPT FLAG SET
190 006350 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
191 006352 000240 2$: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
192 006354 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
193 006360 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
194 006364 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP
195
196          ; TEST THAT THE RECEIVER WILL INTERUPT
197          ; BEFORE THE TRANSMITTER WHEN
198          ; THEY ARE BOTH ENABLED AT THE
199          ; SAME TIME.
200
201          ; TEST 43
202          ; *****
203          ; *****
204 006366 012737 000043 001226 †TST43: MOV #43,TSTNO
205 006374 012737 006502 001216 MOV #TST44,NEXT
206 006402 104412 MSTCLR ; INIT DQ11
207 006404 004737 016042 JSR PC,SETV ; SET THE VECTORS
208 006410 006454 1$: ; THIS FOR RX
209 006412 006456 2$: ; THIS FOR TX
210 006414 012737 000340 177776 MOV #340,PS ; LOCK OUT INTERUPTS
211 006422 012777 000240 172734 MOV #240,ADQTCR ; SET TX PRI DONE AND IE
212 006430 012777 000240 172722 MOV #240,ADQRCR ; SET RX PRI DONE AND IE
213 006436 000240 NOP ; INTERRUPT YET.
214 006440 005037 177776 CLR PS ; ZERO PROC. STATUS
215 006444 000240 NOP ; WAIT ONE INSTR. TIME
216 006446 000240 NOP
217 006450 104001 HLT 1 ; TX AND RX FAILED TO INTERUPT
218 006452 104000 HLT 0

```


2275	006670	001401	BEQ	.+4	:BR IF YES
2276	006672	104000	HLT	0	:EITHER RX DID NOT INTERUPT; OR MORE THAN ONCE
2277	006674	104400	SCOPE		:SCOPE THE TEST
2278	006676	005100	1\$: COM	RO	:CHECK INTERUPT
2279	006700	001401	BEQ	.+4	:BR IF FIRST TIME HERE
2280	006702	104003	HLT	3	:RX INTERUPTED MORE THAN ONCE
2281	006704	000002	RTI		:GO BACK AND DELAY
2282	006706	104002	2\$: HLT	2	:UNEXPECTED TX INTERUPT
2283	006710	000002	RTI		:RETURN

:TEST TO SEE IF THE
:DQ11 TRANSMITTER WILL
:INTERUPT AT PS LEVEL
:OF 7 PRIORITY.

: TEST 46

:*****

2294	006712	012737	000046	001226	TST46: MOV	#46,TSTNO	
2295	006720	012737	007014	001216	MOV	#TST47,NEXT	
2296	006726	104412			MSTCLR		:INIT DQ11
2297	006730	004737	016042		JSR	PC,SETV	:SET VECTORS
2298	006734	006766			1\$:		:RX INTERUPTS TO 1\$
2299	006736	006772			2\$:		:TX INTERUPTS TO 2\$
2300	006740	012700	177777		MOV	#-1,RO	:SET CHECKER
2301	006744	012737	000340	177776	MOV	#340,PS	:SET PRIORITY
2302	006752	012777	000240	172404	MOV	#240,ADQTCR	:SET PRI DONE AND IE
2303	006760	000240			NOP		
2304	006762	000240			NOP		
2305	006764	000403			BR	3\$:CONTINUE TEST
2306	006766	104003			1\$: HLT	3	:UNEXPECTED RX INTERUPT
2307	006770	000002			RTI		:CONTINUE TEST
2308	006772	005100			2\$: COM	RO	:CHECK INTERUPT
2309	006774	012706	001200		3\$: MOV	#STACK,SP	:SET STACK POINTER
2310	007000	005700			TST	RO	:CHECK INTERUPT POINTER
2311	007002	001001			BNE	.+4	
2312	007004	104002			HLT	2	
2313	007006	005077	172352		CLR	ADQTCR	
2314	007012	104400			SCOPE		

:TEST TO SEE IF THE
:DQ11 TRANSMITTER WILL
:INTERUPT AT PS LEVEL
:OF 6 PRIORITY.

: TEST 47

:*****

2324	007014	012737	000047	001226	TST47: MOV	#47,TSTNO	
2325	007022	012737	007116	001216	MOV	#TST50,NEXT	
2326	007030	104412			MSTCLR		:INIT DQ11
2327	007032	004737	016042		JSR	PC,SETV	:SET VECTORS
2328	007036	007070			1\$:		:RX INTERUPTS TO 1\$
2329	007040	007074			2\$:		:TX INTERUPTS TO 2\$
2330	007042	012700	177777		MOV	#-1,RO	:SET CHECKER

```

2331 007046 012737 000300 177776      MOV      #300,PS      ;SET PRIORITY
2332 007054 012777 000240 172302      MOV      #240,SDQTCR ;SET PRI DONE AND IE
2333 007062 000240                NOP
2334 007064 000240                NOP
2335 007066 000403                BR       3$
2336 007070 104003                HLT     3            ;CONTINUE TEST
2337 007072 000002                RTI
2338 007074 005100                COM     R0          ;UNEXPECTED RX INTERUPT
2339 007076 012706 001200      2$:      MOV      #STACK,SP ;CONTINUE TEST
2340 007102 005700                TST     R0          ;CHECK INTERUPT
2341 007104 001001                BNE     .+4         ;SET STACK POINTER
2342 007106 104002                HLT     2
2343 007110 005077 172250      CLR     SDQTCR     ;CHECK INTERUPT POINTER
2344 007114 104400                SCOPE
2345
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```

;TEST TO SEE IF THE
;DQ11 TRANSMITTER WILL
;INTERUPT AT PS LEVEL
;OF 5 PRIORITY.

```

; TEST 50
*****
TST50: MOV      #50,TSTNO
      MOV      #TST51,NEXT
      MSTCLR
      JSR     PC,SETV      ;INIT DQ11
                          ;SET VECTORS
                          ;RX INTERUPTS TO 1$
                          ;TX INTERUPTS TO 2$
                          ;SET CHECKER
                          ;SET PRIORITY
                          ;SET PRI DONE AND IE
      BR       3$
1$:    HLT     3            ;CONTINUE TEST
      RTI
2$:    COM     R0          ;UNEXPECTED RX INTERUPT
3$:    MOV      #STACK,SP ;CONTINUE TEST
      TST     R0          ;CHECK INTERUPT
      BNE     .+4         ;SET STACK POINTER
      HLT     2          ;CHECK INTERUPT POINTER
      CLR     SDQTCR
      SCOPE
;TEST TO SEE IF THE
;DQ11 TRANSMITTER WILL
;INTERUPT AT PS LEVEL
;OF 4 PRIORITY.
; TEST 51
*****
TST51: MOV      #51,TSTNO
      MOV      #CHKBA,NEXT
      MSTCLR
                          ;INIT DQ11

```

```

2387 007236 004737 016042 JSR PC,SETV ;SET VECTORS
2388 007242 007274 1$ ;RX INTERRUPTS TO 1$
2389 007244 007300 2$ ;TX INTERRUPTS TO 2$
2390 007246 012700 177777 MOV #-1,RO ;SET CHECKER
2391 007252 012737 000200 177776 MOV #200,PS ;SET PRIORITY
2392 007260 012777 000240 172076 MOV #240,ADQTCR ;SET PRI DONE AND IE
2393 007266 000240 NOP ;
2394 007270 000240 NOP ;
2395 007272 000403 BR 3$ ;CONTINUE TEST
2396 007274 104003 1$: HLT 3 ;UNEXPECTED RX INTERRUPT
2397 007276 000002 RTI ;CONTINUE TEST
2398 007300 005100 2$: COM RO ;CHECK INTERRUPT
2399 007302 012706 001200 3$: MOV #STACK,SP ;SET STACK POINTER
2400 007306 005700 TST RO ;CHECK INTERRUPT POINTER
2401 007310 001401 BEQ +4 ;
2402 007312 104001 HLT 1 ;
2403 007314 005077 172044 CLR ADQTCR ;
2404 007320 104400 SCOPE ;
; IF THE DATA SET CONTROL OPTION IS INSTALLED,
; TEST 52 WILL BE EXECUTED
2412 007322 032737 010000 001510 CHKBA: BIT #BABIT,DQSTAT
2413 007330 001435 BEQ CHKCA1
; INTERRUPT LOGIC TEST
; SET DATA SET INTERRUPT ENABLE
; SET DATA SET INTERRUPT FLAG
; VERIFY THAT AN INTERRUPT OCCURS TO THE CORRECT VECTOR
; TEST 52
; *****
2422 007332 012737 000052 001226 TST52: MOV #52,TSTNO
2423 007340 012737 007426 001216 MOV #TST53,NEXT
2424 007346 104412 MSTCLR ;CLEAR INTERFACE
2425 007350 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
2426 007354 007406 1$ ;RECEIVE 3 WILL INTERRUPT TO 1$
2427 007356 007410 2$ ;TRANSMITTER WILL INTERRUPT TO 2$
2428 007360 052777 000030 171776 BIS #BIT4,ADQTCR ;SET DATA SET INTERRUPT ENABL
2429 007366 052777 100000 171770 BIS #BIT15,ADQTCR ;SET DATA SET INTERRUPT FLAG
2430 007374 005037 177776 CLR PS ;SET PROCESSOR PRIORITY TO 0
2431 007400 000240 NOP ;WINDOW FOR INTERRUPTS
2432 007402 104001 HLT 1 ;TRANSMITTER DID NOT INTERRUPT
2433 007404 000402 BR 3$ ;WITH DATA SET INTERRUPT ENABL AND
;DATA SET INTERRUPT FLAG SET
2435 007406 104003 1$: HLT 3 ;UNEXPECTED RECEIVER INTERRUPT
2436 007410 000240 2$: NOP ;TRANSMITTER SHOULD INTERRUPT TO HERE
2437 007412 012706 001200 3$: MOV #STACK,SP ;RESTORE STACK
2438 007416 004737 016074 JSR PC,RECAT ;RESTORE TRAPCATCHER
2439 007422 104400 4$: SCOPE ;CHECK FOR ITERATIONS, LOOP

```


2440 007424 000240 CHKCA1: NOP

: RECEIVER BASIC NPR LOGIC TEST (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT)
: EXPECTED RESULTS
: RECEIVER DONE INTERRUPT OCCURS
: RECEIVER DONE (PRIMARY) = 1
: RECEIVER GO = 0
: RECEIVER P/S = 1
: NO ERROR FLAGS ARE SET
:
: RECEIVER BUS ADDRESS (PRIMARY) = RBUFF+1
: RECEIVER CHARACTER COUNT (PRIMARY) = 0
: CONTENTS OF RBUFF = 0

: TEST 53

: *****

2456	007426	012737	000053	001226	TST53:	MOV	#53, TSTNO	
2457	007434	012737	007450	001214		MOV	#99\$, RETURN	
2458	007442	012737	007752	001216		MOV	#TST54, NEXT	
2459	007450	104413			99\$:	MEMCLR		
2460	007452	104412			1\$:	MSTCLR		
2461	007454	012737	000340	177776		MOV	#340, PS	; LOCK OUT INTERRUPTS
2462	007462	012737	000000	017170		MOV	#0, TBUFF	
2463	007470	004737	016024			JSR	PC, SETMNT	; SET MAINTENANCE MODE
2464	007474	004737	016042			JSR	PC, SETV	; SET UP INTERRUPT VECTORS
2465	007500	007576				3\$; RECEIVER WILL INTERRUPT TO 3\$
2466	007502	007600				4\$; TRANSMITTER WILL INTERRUPT TO 4\$
2467	007504	004737	016122			JSR	PC, SETBABC	; SELECT RECEIVER BUS ADDRESS (PRIMARY)
2468	007510	000	000		.BYTE	0, 0		; LOAD BUS ADDRESS
2469	007512	017166				RBUFF		; SELECT RECEIVER CHARACTER COUNT (PRIMARY)
2470	007514	177777				-1		; CHARACTER COUNT=1
2471	007516	012777	000040	171634		MOV	#BITS, DQRCR	; SET RECEIVER PRIMARY INTERRUPT ENABLE
2472	007524	052777	000001	171626		BIS	#BIT0, DQRCR	; SET RECEIVER GO
2473	007532	112777	000012	171630		MOVB	#12, DQREG	; SELECT MISCELLANEOUS REGISTER
2474	007540	052777	000020	171624		BIS	#BIT4, DQSEC	; FORCE RECEIVER INTERRUPT
2475	007546	005037	177776			CLR	PS	; ENABLE INTERRUPTS
2476	007552	012737	002000	001244		MOV	#2000, TEMP1	; SET UP DELAY
2477	007560	005337	001244		2\$:	DEC	TEMP1	; WAIT FOR INTERRUPTS AND NPPS
2478	007564	001375				BNE	2\$	
2479	007566	012737	000340	177776		MOV	#340, PS	; LOCK OUT INTERRUPTS
2480	007574	104000				HLT	0	; RECEIVER DID NOT INTERRUPT
2481	007576	000401			3\$:	BR	5\$	
2482	007600	104002			4\$:	HLT	2	; UNEXPECTED TRANSMITTER INTERRUPT
2483	007602	012706	001200		5\$:	MOV	#STACK, SP	; RESTORE PROCESSOR STACK
2484	007606	012705	000244			MOV	#244, R5	; (R5)=EXPECTED DATA IN RECEIVER CONTROL REGISTER
2485								; DONE (PRIMARY)=1, INTERRUPT ENEABLE=1,
2486								; P/S=1
2487	007612	017704	171542			MOV	DQRCR, R4	; (R4)=ACTUAL DATA IN RECEIVER CONTROL REGISTER
2488	007616	042704	177400			BIC	#177400, R4	; CLEAR UNWANTED BITS
2489	007622	020504				CMP	R5, R4	; ARE EXPECTED AND RECEIVED DATA THE SAME
2490	007624	001401				BEQ	6\$	
2491	007626	104004				HLT	4	; RECEIVER STATUS ERROR
2492	007630	005005			6\$:	CLR	R5	; (R5)=EXPECTED DATA IN ERROR REGISTER, 0
2493	007632	013703	001366			MOV	DQERR, R3	; ADDRESS OF ERROR REGISTER
2494	007636	117704	171524			MOVB	DQERR, R4	; (R4) TUAL DATA IN ERROR REGISTER
2495	007642	001401				BEQ	7\$	

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2496 007644 104006          HLT      6          ;ERROR FLAG(S) SET
2497 007646 112777 000000 171514 7$:  MOVB   #0, @DQREG ;SELECT RECEIVER BUS ADDRESS (PRIMARY)
2498 007654 012702 000000          MOV    #0, R2     ;ADDRESS OF RECEIVER BUS ADDRESS
2499                                ;SECONDARY REGISTER
2500 007660 013703 001372          MOV    DQSEC, R3 ;ADDRESS OF SECONDARY REGISTER
2501 007664 012705 017167          MOV    #RBUF+1, R5 ;(R5)=EXPECTED DATA IN
2502                                ;RECEIVER BUS ADDRESS (PRIMARY) REGISTER,
2503                                ;RBUF+1
2504 007670 017704 171476          MOV    @DQSEC, R4 ;(R4)=ACTUAL DATA IN RECEIVER
2505                                ;BUS ADDRESS REGISTER (PRIMARY)
2506 007674 020504          CMP    R5, R4     ;ARE EXPECTED AND RECEIVED DATA THE SAME
2507 007676 001401          BEQ    10$
2508 007700 104007          HLT    7          ;BUS ADDRESS ERROR
2509 007702 105277 171462          INCB  @DQREG     ;SELECT CHARACTER COUNT ADD.
2510 007706 005202          INC    R2        ;UPDATE POINTER
2511 007710 012705 000000          MOV    #0, R5     ;SET FOR EXPECTED.
2512 007714 017704 171452          MOV    @DQSEC, R4 ;READ THE ACTUAL.
2513 007720 020504          CMP    R5, R4     ;ARE THEY EQUAL?
2514 007722 001401          BEQ    11$
2515 007724 104010          HLT    10        ;BR IF YES
2516 007726 012705 000000          MOV    #0, R5     ;CHARACTER COUNT ERROR
2517 007732 012703 017166          MOV    #RBUF, R3 ;SET POINTER.
2518 007736 013704 017166          MOV    RBUF, R4
2519 007742 020504          CMP    R5, R4     ;EQUAL?
2520 007744 001401          BEQ    12$
2521 007746 104011          HLT    11        ;BR IF YES
2522 007750 104400          HLT    11
2523
2524                                ; TRANSMITTER BASIC NPR LOGIC TEST (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT
2525                                ; EXPECTED RESULTS
2526                                ;
2527                                ; TRANSMITTER DONE INTERRUPT OCCURS
2528                                ; TRANSMITTER DONE (PRIMARY) = 1
2529                                ; TRANSMITTER GO = 0
2530                                ; TRANSMITTER P/S = 1
2531                                ; NO ERROR FLAGS ARE SET
2532                                ;
2533                                ; TRANSMITTER BUS ADDRESS (PRIMARY) = TBUF+1
2534                                ; TRANSMITTER CHARACTER COUNT (PRIMARY) = 0
2535                                ; CONTENTS OF TRANSMITTER BUFFER = 52525
2536
2537                                ; TEST 54
2538                                ; *****
2538 007752 012737 000054 001226  TST54: MOV    #54, TSTNO
2539 007760 012737 007776 001214          MOV    #1$, RETURN
2540 007766 012737 010272 001216          MOV    #TST55, NEXT
2541 007774 104413          99$:  MEMCLR
2542 007776 104412          1$:  MSTCLR
2543 010000 012737 000340 177776          MOV    #340, PS   ;LOCK OUT INTERRUPTS
2544 010006 012737 052525 017170          MOV    #52525, TBUF
2545 010014 004737 016024          JSR    PC, SETMNT ;SET MAINTENANCE MODE
2546 010020 004737 016042          JSR    PC, SETV   ;SET UP INTERRUPT VECTORS
2547 010024 010110          3$:
2548 010026 010112          4$:
2549 010030 004737 016122          JSR    PC, SETBABC ;RECEIVER WILL INTERRUPT TO 3$
2550 010034 002000          .BYTE 2, 0       ;TRANSMITTER WILL INTERRUPT TO 4$
2551 010036 017170          TBUF           ;SELECT TRANSMITTER BUS ADDRESS (PRIMARY)
;LOAD BUS ADDRESS
;SELECT TRANSMITTER CHARACTER COUNT (PRIMARY)

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M04

DZDQC MACY11 27(732) 24-SEP-76 10:14 PAGE 52
 DZDQCC.P11 DQ11 INTERRUPT AND NPR LOGIC TESTS.

```

2608 :
2609 :
2610 :
2611 :
2612 :
2613 :
2614 :
2615 :
2616 :
2617 :
2618 :
2619 :
2620 010272 012737 000055 001226 ; TEST 55
2621 010300 012737 010704 001216 ;*****
2622 010306 104412 MSTCLR ;ISSUE A MASTER CLEAR.
2623 010310 004737 016006 JSR PC,SETLOP ;SET TEST LOOP
2624 010314 105077 171050 CLRB @DQREG ;SELECT RX BA PRI.
2625 010320 012777 017166 171044 MOV #RBUF,@DQSEC ;SET RX BA
2626 010326 105277 171036 INCB @DQREG ;SELECT RX WC PRI.
2627 010332 012777 177777 171032 MOV #-1,@DQSEC ;SET FOR ONE CHAR.
2628 010340 052777 010001 171012 BIS #BIT12+BIT0,@DQRCSR ;SET ACTIVE AND GO!!
2629 010346 012700 007000 MOV #7000,R0 ;SET FOR TIME OUT DELAY
2630 010352 005300 DEC R0 ;DELAY.....
2631 010354 001376 BNE .-2 ;DONE?
2632 010356 012705 000204 MOV #204,R5 ;SET EXPECTED. PRI. DONE AND P/S
2633 010362 017704 170772 MOV @DQRCSR,R4 ;READ RX CSR.
2634 010366 042704 177400 BIC #177400,R4 ;MASK UNWANTED BITS.
2635 010372 020405 CMP R4,R5 ;IS IT CORRECT?
2636 010374 001401 BEQ .+4 ;BR IF YES.
2637 010376 104004 HLT 4 ;RECEIVER STATUS ERROR.
2638 010400 005077 170754 CLR @DQRCSR ;CLEAR ALL BUT RX P/S
2639 010404 012737 000340 177776 MOV #340,PS ;LOCK OUT INTERRUPTS
2640 010412 012737 000000 017170 MOV #0,TBUFF
2641 010420 104413 1$: MEMCLR ;CLEAR INTERFACE MEMORIES
2642 010422 004737 016024 JSR PC,SETMNT ;SET MAINTENANCE MODE
2643 010426 004737 016042 JSR PC,SETV ;SET UP INTERRUPT VECTORS
2644 010432 010530 3$ ;RECEIVER WILL INTERRUPT TO 3$
2645 010434 010532 4$ ;TRANSMITTER WILL INTERRUPT TO 4$
2646 010436 004737 016122 JSR PC,SETBABC ;SELECT RECEIVER BUS ADDRESS (SECONDARY)
2647 010442 004 000 .BYTE 4,0 ;LOAD BUS ADDRESS
2648 010444 017166 RBUF ;SELECT RECEIVER CHARACTER COUNT (SECONDARY)
2649 010446 177777 -1 ;CHARACTER COUNT=1
2650 010450 012777 000040 170702 MOV #BITS,@DQRCSR ;SET RECEIVER SECONDARY INTERRUPT ENABLE
2651 010456 052777 000001 170674 BIS #BIT0,@DQRCSR ;SET RECEIVER GO
2652 010464 112777 000012 170676 MOVB #12,@DQREG ;SELECT MISCELLANEOUS REGISTER
2653 010472 052777 000020 170672 BIS #BIT4,@DQSEC ;FORCE RECEIVER INTERRUPT
2654 010500 005037 177776 CLR PS ;ENABLE INTERRUPTS
2655 010504 012737 002000 001244 MOV #2000,TEMP1 ;SET UP DELAY
2656 010512 005337 001244 2$: DEC TEMP1 ;WAIT FOR INTERRUPTS AND NPRS
2657 010515 001375 BNE 2$
2658 010518 012737 000340 177776 MOV #340,PS ;LOCK OUT INTERRUPTS
2659 010520 104000 HLT 0 ;RECEIVER DID NOT INTERRUPT
2660 010530 000401 3$: BR 5$
2661 010532 104002 4$: HLT 2 ;UNEXPECTED TRANSMITTER INTERRUPT
2662 010534 012706 001200 5$: MOV #STACK,SP ;RESTORE PROCESSOR STACK
2663 010540 012705 000140 MOV #140,R5 ;(R5)=EXPECTED DATA IN RECEIVER CONTROL REGISTER

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2664                                     ;DONE (SECONDARY)=1, INTERRUPT ENEABLE=1,
2665                                     ;P/S=1
2666 010544 017704 170610                MOV    JDQRCR,R4
2667 010550 042704 177400                BIC    #177400,R4
2668 010554 020504                       CMP    R5,R4
2669 010556 001401                       BEQ    6$
2670 010560 104004                       HLT    4
2671 010562 005005 6$:                  CLR    R5
2672 010564 013703 001366                MOV    DQERR,R3
2673 010570 117704 170572                MOVB   JDQERR,R4
2674 010574 001401                       BEQ    7$
2675 010576 104006                       HLT    6
2676 010600 112777 000004 170562 7$:    MOVB   #4,JDQREG
2677 010606 012702 000004                MOV    #4,R2
2678                                     ;ADDRESS OF RECEIVER BUS ADDRESS
2679 010612 013703 001372                MOV    DQSEC,R3
2680 010616 012705 017167                MOV    #RBUF+1,R5
2681                                     ;(R5)=EXPECTED DATA IN
2682                                     ;RECEIVER BUS ADDRESS (SECONDARY) REGISTER,
2683                                     ;RBUF+1
2684 010622 017704 170544                MOV    JDQSEC,R4
2685 010626 020504                       CMP    R5,R4
2686 010630 001401                       BEQ    10$
2687 010632 104007                       HLT    7
2688 010634 105277 170530 10$:         INCB   JDQREG
2689 010640 005202                       INC    R2
2690 010642 012705 000000                MOV    #0,R5
2691 010646 017704 170520                MOV    JDQSEC,R4
2692 010652 020504                       CMP    R5,R4
2693 010654 001401                       BEQ    11$
2694 010656 104010                       HLT    10
2695 010660 012705 000000 11$:         MOV    #0,R5
2696 010664 012703 017166                MOV    #RBUF,R3
2697 010670 013704 017166                MOV    RBUF,R4
2698 010674 020504                       CMP    R5,R4
2699 010676 001401                       BEQ    QZX
2700 010700 104011                       HLT    11
2701 010702 104400  QZX:                SCOPE
2702
2703                                     ; TRANSMITTER BASIC NPR LOGIC TEST (USING SECONDARY BUS ADDRESS AND CHARACTER COU
2704                                     ; EXPECTED RESULTS
2705                                     ; TRANSMITTER DONE INTERRUPT OCCURS
2706                                     ; TRANSMITTER DONE (SECONDARY) = 1
2707                                     ; TRANSMITTER GO = 0
2708                                     ; TRANSMITTER P/S = 1
2709                                     ; NO ERROR FLAGS ARE SET
2710
2711                                     ; TRANSMITTER BUS ADDRESS (SECONDARY) = TBUF+1
2712                                     ; TRANSMITTER CHARACTER COUNT (SECONDARY) = 0
2713                                     ; CONTENTS OF TRANSMITTER BUFFER = 177777
2714
2715                                     ; TEST 56
2716                                     ; *****
2717 010704 012737 000056 001226  †T56:  MOV    #56,TSTNO
2718 010712 012737 010730 001214        MOV    #1$,RETURN
2719 010720 012737 011330 001216        MOV    #TST57,NEXT

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7770	0110726	104413			MEMCLR				:ISS'IE A MEMORY CLEAR.
7771	0110730	104413			MSTCLR				:MASTER CLEAR,DQ11
7772	0110730	104413			MEMCLR				
7773	0110734	112777	000012	170426	MOVB	#12, @DQREG			:SELECT MISC.REG
7774	0110744	012777	004010	170422	MOV	#4010, @DQSEC			:SET FOR EIGHT BITS AND TEST LOOP
7775	0110754	112777	000002	170412	MOVB	#2, @DQREG			:SEL TX BA PRI.
7776	0110756	012777	017170	170406	MOV	#TBUFF, @DQSEC			:SET BUS ADDRESS
7777	0110764	105277	70400		INCB	@DQREG			:SELECT TX WC PRI.
7778	0110770	012777	177777	170374	MOV	#-1, @DQSEC			:SET FOR ONE CHAR.
7779	0110776	005277	170362		INC	@DQTCR			:SET TX GO!!
7780	0111000	012700	000010		MOV	#10, R0			:SET FOR TIME OUT.
7781	0111000	005300			DEC	R0			:DELAY
7782	0111010	001276			SNE	.-2			:BR IF MORE DELAY
7783	0111016	01705	000204		MOV	#204, R5			:SET FOR EXPECTED.
7784	0111016	01704	170342		MOV	@DQTCR, R4			:READ THE TX CSR
7785	0111022	020405			CMP	R4, R5			:EXPECTED=ACTUAL?
7786	0111022	001401			BEQ	+4			:BR IF YES
7787	0111030	104005			TLI				:TX STATUS REG ERROR
7788	0111030	005077	170330		CLR	@DQTCR			:CLEAR ALL BUT P/S BIT
7789	0111034	012737	000340	177776	MOV	#340, PS			:LOCK OUT INTERRUPTS
7790	0111044	012737	177777	017170	MOV	#177777, TBUFF			:SET CHARACTER
7791	0111050	104413			MEMCLR				:CLEAR INTERFACE MEMORIES
7792	0111056	004737	016006		JSR	PC, SETLOP			:SET MAINTENANCE MODE
7793	0111056	004737	016042		JSR	PC, SETV			:SET UP INTERRUPT VECTORS
7794	0111062	011146			JS				:RECEIVER WILL INTERRUPT TO 3\$
7795	0111064	011150			JS				:TRANSMITTER WILL INTERRUPT TO 4\$
7796	0111066	004737	016122		JSR	PC, SETBABC			:SELECT TRANSMITTER BUS ADDRESS (SECONDARY)
7797	0111072	006	000		.BYTE	6, 0			:LOAD BUS ADDRESS
7798	0111074	017170			TBUFF				:SELECT TRANSMITTER CHARACTER COUNT (SECONDARY)
7799	0111076	177777			-1				:CHARACTER COUNT=1
7800	0111100	012777	000340	170256	MOV	#BITS, @DQTCR			:SET TRANSMITTER SECONDARY INTERRUPT ENABLE
7801	0111106	052777	000001	170250	BIS	#BIT0, @DQTCR			:SET TRANSMITTER GO
7802	0111114	005037	177776		CLR	PS			:ENABLE INTERRUPTS
7803	0111120	012737	002000	001244	MOV	#2000, TEMP1			:SET UP DELAY
7804	0111126	005337	001244		DEC	TEMP1			:WAIT FOR INTERRUPTS AND NPRS
7805	0111132	01775			SNE	2\$			
7806	0111134	01737	000340	177776	MOV	#340, PS			:LOCK OUT INTERRUPTS
7807	0111142	104003			HLT	1			:TRANSMITTER DID NOT INTERRUPT
7808	0111144	000402			BR	5\$			
7809	0111146	104003			HLT	3			:UNEXPECTED RECEIVER INTERRUPT
7810	0111150	000240			NOP				
7811	0111150	012706	001200		MOV	#STACK, SP			:RESTORE PROCESSOR STACK
7812	0111156	012705	000140		MOV	#140, R5			: (R5)=EXPECTED DATA IN TRANSMITTER CONTROL REGIS
7813									: DONE (SECONDARY)=1, INTERRUPT ENAGBLE=1,
7814									: P/S=1
7815	0111162	017704	170176		MOV	@DQTCR, R4			: (R4)=ACTUAL DATA IN TRANSMITTER CONTROL REGISTE
7816	0111166	042704	177400		BIC	#177400, R4			:CLEAR UNWANTED BITS
7817	0111172	020504			CMP	R5, R4			:ARE EXPECTED AND RECEIVED DATA THE SAME
7818	0111174	001401			BEQ	6\$			
7819	0111176	104005			HLT	5\$:TRANSMITTER STATUS ERROR
7820	0111200	005005			CLR	R5			: (R5)=EXPECTED DATA IN ERROR REGISTER, 0
7821	0111202	013703	001366		MOV	DQERR, R3			:ADDRESS OF ERROR REGISTER
7822	0111206	117704	170154		MOVB	@DQERR, R4			: (R4)TUAL DATA IN ERROR REGISTER
7823	0111212	001401			BEQ	7\$			
7824	0111214	104006			HLT	6			:ERROR FLAG(S) SET
7825	0111216	112777	000006	170154	MOVB	#6, @DQREG			:SELECT TRANSMITTER B" ADDRESS (SECONDARY)

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011224 012702 000006      MOV      #6,R2          ;ADDRESS OF TRANSMITTER BUS ADDRESS
011230 013703 001372      MOV      DQSEC,R3      ;SECONDARY REGISTER
011234 012705 017171      MOV      #TBUF+1,R5    ;ADDRESS OF SECONDARY REGISTER
                                ;(R5)=EXPECTED DATA IN
                                ;TRANSMITTER BUS ADDRESS (SECONDARY) REGISTER,
                                ;TBUF+1
011240 017704 170126      MOV      @DQSEC,R4     ;(R4)=ACTUAL DATA IN TRANSMITTER
                                ;BUS ADDRESS REGISTER (SECONDARY)
                                ;ARE EXPECTED AND RECEIVED DATA THE SAME
011244 020504      CMP      R5,R4
011246 001401      BEQ     10$
011250 104007      HLT     7              ;BUS ADDRESS ERROR
011252 105277 170112      10$:    INCB   @DQREG
011254 005202      INC     R2
011256 012705 000000      MOV      #0,R5
011258 017704 170102      MOV      @DQSEC,R4
011260 020504      CMP      R5,R4
011262 001401      BEQ     11$
011264 104010      HLT     10            ;CHARACTER COUNT ERROR
011266 012705 177777      11$:    MOV      #177777,R5
011268 112777 000013 170060      MCRB   #13,@DQREG
011270 012702 000013      MOV      #13,R2
011272 017704 170052      MOV      @DQSEC,R4
011274 020504      CMP      R5,R4
011276 001401      BEQ     12$
011278 104012      HLT     12
011280 104400      12$:    SCOPE

```

```

;RECEIVER NON-EXISTANT MEMORY TIMEOUT TEST
;(USING PRIMARY BUS ADDRESS AND CHARACTER COUNT)
;EXPECTED RESULTS
;
;RECEIVER DONE INTERRUPT OCCURS
;RECEIVER DONE (PRIMARY) = 1
;RECEIVER CO = 0
;RECEIVER P/S = 1
;RECEIVER NON EXISTANT MEMORY ERROR FLAG = 1
;
;RECEIVER BUS ADDRESS (PRIMARY) = RBUF+1
;RECEIVER CHARACTER COUNT (PRIMARY) = 0

```

: TEST 57

```

011320 012737 000057 001226  ;*****
011322 012737 011362 001214  ;TST57: MOV      #57,TSTNO
011324 012737 011624 001216  MOV      #1$,RETURN
011326 012737 000340 177776  MOV      #TST60,NEXT
                                MOV      #340,P$
                                ;LOCK OUT INTERRUPTS
                                ;CLEAR INTERFACE MEMORIES
                                ;MASTER CLEAR INTERFACE
                                ;SET MAINTENANCE MODE
                                ;SET UP INTERRUPT VECTORS
                                ;RECEIVER WILL INTERRUPT TO 3$
                                ;TRANSMITTER WILL INTERRUPT TO 4$
011360 104413      1$:    MEMCLR
011362 104412      MSTCLR
011364 004737 016024      JSR     PC,SETMNT
011370 004737 016042      JSR     PC,SETV
011374 011472      3$:
011376 011474      4$:
011400 004737 016122      JSR     PC,SETBABC
011404 000000 140      .BYTE  0,140
011406 177320      NON.EX
011410 177777      -1
011412 012777 000040 167740      MOV      #BITS,@DQRCR
                                ;SET RECEIVER PRIMARY INTERRUPT ENABLE

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2883	011423	052777	000001	167732		BIS	#BIT0, DQRCR	: SET RECEIVER GO
2884	011426	112777	000012	167734		MOVB	#12, DQREG	: SELECT MISCELLANEOUS REGISTER
2885	011434	052777	000020	167730		BIS	#BIT4, DQSEC	: FORCE RECEIVER INTERRUPT
2886	011442	005037	177776			CLR	PS	: ENABLE INTERRUPTS
2887	011446	012737	002000	001244		MOV	#2000, TEMP1	: SET UP DELAY
2888	011454	005337	001244		2\$:	DEC	TEMP1	: WAIT FOR INTERRUPTS AND NPRS
2889	011460	001375				SNE	2\$	
2890	011462	012737	000340	177776		MOV	#340, PS	: LOCK OUT INTERRUPTS
2891	011470	104000				HLT	0	: RECEIVER DID NOT INTERRUPT
2892	011472	000401			3\$:	BR	5\$	
2893	011474	104002			4\$:	HLT	2	: UNEXPECTED TRANSMITTER INTERRUPT
2894	011476	012706	001200		5\$:	MOV	#STACK, SP	: RESTORE PROCESSOR STACK
2895	011502	012705	000244			MOV	#244, R5	: (R5)=EXPECTED DATA IN RECEIVER CONTROL REGISTER
2896								: DONE (PRIMARY)=1, INTERRUPT ENEABLE=1,
2897								: P/S=1
2898	011506	017704	167646			MOV	DQRCR, R4	: (R4)=ACTUAL DATA IN RECEIVER CONTROL REGISTER
2899	011512	042704	177400			BIC	#177400, R4	: CLEAR UNWANTED BITS
2900	011516	020504				CMP	R5, R4	: ARE EXPECTED AND RECEIVED DATA THE SAME
2901	011520	001401				BEQ	6\$	
2902	011522	104004				HLT	4	: RECEIVER STATUS ERROR
2903	011524	005005			6\$:	CLR	R5	: (R5)=EXPECTED DATA IN ERROR REGISTER, 0
2904	011526	013703	001366			MOV	DQERR, R3	: ADDRESS OF ERROR REGISTER
2905	011532	017704	167630			MOV	DQERR, R4	: (R4) TUAL DATA IN ERROR REGISTER
2906	011536	100401				BMI	7\$	
2907	011540	104006				HLT	6	: ERROR FLAG(S) NOT SET
2908	011542	112777	000000	167620	7\$:	MOVB	#0, DQREG	: SELECT RECEIVER BUS ADDRESS (PRIMARY)
2909	011550	012702	000000			MOV	#0, R2	: ADDRESS OF RECEIVER BUS ADDRESS
2910								: SECONDARY REGISTER
2911	011554	013703	001372			MOV	DQSEC, R3	: ADDRESS OF SECONDARY REGISTER
2912	011560	012705	177321			MOV	#NON.EX+1, R5	: (R5)=EXPECTED DATA IN
2913								: RECEIVER BUS ADDRESS (PRIMARY) REGISTER,
2914	011564	017704	167602			MOV	DQSEC, R4	: RBUFF+1
2915								: (R4)=ACTUAL DATA IN RECEIVER
2916	011570	020504				CMP	R5, R4	: BUS ADDRESS REGISTER (PRIMARY)
2917	011572	001401				BEQ	10\$: ARE EXPECTED AND RECEIVED DATA THE SAME
2918	011574	104007				HLT	7	: BUS ADDRESS ERROR
2919	011576	105277	167566		10\$:	INCB	DQREG	
2920	011602	005202				INC	R2	
2921	011604	012705	000000			MOV	#0, R5	
2922	011610	017704	167556			MOV	DQSEC, R4	
2923	011614	020504				CMP	R5, R4	
2924	011616	001401				BEQ	11\$	
2925	011620	104010				HLT	10	: CHARACTER COUNT ERROR
2926	011622	104400			11\$:	SCOPE		
2927								: TRANSMITTER NON-EXISTANT MEMORY TIMEOUT TEST
2928								: (USING PRIMARY BUS ADDRESS AND CHARACTER COUNT)
2929								: EXPECTED RESULTS
2930								: TRANSMITTER DONE INTERRUPT OCCURS
2931								: TRANSMITTER DONE (PRIMARY) = 1
2932								: TRANSMITTER GO = 0
2933								: TRANSMITTER P/S = 1
2934								: TRANSMITTER NON EXISTANT MEMORY ERROR FLAG = 1
2935								: TRANSMITTER BUS ADDRESS (PRIMARY) = TBUFF+1

E05

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DZDQCC.P11 DQ11 INTERRUPT AND NPR LOGIC TESTS.

TRANSMITTER CHARACTER COUNT (PRIMARY) = 0

```

:
: TEST 60
: *****
: ST60: MOV #60,TSTNO
: MOV #1$,RETURN
: MOV #TST61,NEXT
: MOV #340,PS
: LOCK OUT INTERRUPTS
: CLEAR INTERFACE MEMORIES
: MASTER CLEAR INTERFACE
: SET MAINTENANCE MODE
: SET UP INTERRUPT VECTORS
: RECEIVER WILL INTERRUPT TO 3$
: TRANSMITTER WILL INTERRUPT TO 4$
:
1$: MEMCLR
: MSTCLR
: JSR PC,SETMNT
: JSR PC,SETV
: 3$
: 4$
: JSR PC,SETBABC
: 2
: .BYTE 140
: NON.EX
: -1
: MOV #BITS,JDQTCR
: BIS #BIT0,JDQTCR
: CLR PS
: MOV #2000,TEMP1
: 2$: DEC TEMP1
: BNE 2$
: MOV #340,PS
: LOCK OUT INTERRUPTS
: TRANSMITTER DID NOT INTERRUPT
: 5$: HLT 3
: UNEXPECTED RECEIVER INTERRUPT
: 5$: MOV #STACK,SP
: MOV #244,R5
: RESTORE PROCESSOR STACK
: (R5)=EXPECTED DATA IN TRANSMITTER CONTROL REGIS
: DONE (PRIMARY)=1, INTERRUPT ENEABLE=1,
: P/S=1
: (R4)=ACTUAL DATA IN TRANSMITTER CONTROL REGISTE
: CLEAR UNWANTED BITS
: ARE EXPECTED AND RECEIVED DATA THE SAME
: 6$: HLT 5
: TRANSMITTER STATUS ERROR
: (R5)=EXPECTED DATA IN ERROR REGISTER, 0
: ADDRESS OF ERROR REGISTER
: (R4)TUAL DATA IN ERROR REGISTER
: 7$: HLT 6
: ERROR FLAG(S) NOT SET
: SELECT TRANSMITTER BUS ADDRESS (PRIMARY)
: ADDRESS OF TRANSMITTER BUS ADDRESS
: SECONDARY REGISTER
: ADDRESS OF SECONDARY REGISTER
: (R5)=EXPECTED DATA IN
: TRANSMITTER BUS ADDRESS (PRIMARY) REGISTER,
: TBUF+1
: (R4)=ACTUAL DATA IN TRANSMITTER
: BUS ADDRESS REGISTER (PRIMARY)
: ARE EXPECTED AND RECEIVED DATA THE SAME
: 10$: INCB JDQREG
: BUS ADDRESS ERROR

```

```

012064 005202          INC      R2
012066 012705 000000  MOV     #0,R5
012072 017704 167274  MOV     @DQSEC,R4
012076 020504          CMP     R5,R4
012100 001401          BEQ    11$
012102 104010          HLT    10 ; CHARACTER COUNT ERROR
012104 104400          11$: SCOPE

```

```

;RECEIVER P/S MASTER CLEAR TEST
;EXECUTE 1 NPR CYCLE TO FORCE RECEIVER P/S TO A 1
;ISSUE MASTER CLEAR
;VERIFY THAT RECEIVER P/S WAS CLEARED

```

; TEST 61

```

*****
012106 012737 000061 001226 TST61: MOV     #61,TSTNO
012114 012737 012140 001214  MOV     #1$,RETURN
012122 012737 012272 001216  MOV     #TST62,NEXT
012130 012737 000340 177776  MOV     #340,PS ; LOCK OUT INTERUPTS.
012136 104413          MEMCLR
012140 104412          1$: MSTCLR ; MASTER CLEAR INTERFACE
012142 004737 016024          JSR     PC,SETMNT ; SET MAINTENANCE MODE
012146 004737 016122          JSR     PC,SETBABC
012152 000000          .BYTE 0,0
012154 017166          RBUFF
012156 177777          -1
012160 052777 000001 167172  BIS     #BIT0,@DQRCR
012166 112777 000012 167174  MOVB   #12,@DQREG ; SELECT MISC REGISTER
012174 052777 000020 167170  BIS     #BIT4,@DQSEC ; FORCE RX NPR
012202 012737 002000 001244  MOV     #2000,TEMP1 ; SET FOR TIME OUT
012210 105777 167144          2$: TSTB  @DQRCR ; PRIMARY DONE UP
012214 100412          BMI   3$ ; BR IF PRI DONE SET.
012216 005337 001244          DEC   TEMP1 ; DELAY
012222 001372          BNE   2$ ; KEEP WAITING
012224 017704 167130          MOV   @DQRCR,R4 ; SAVE THE CSR
012230 042704 177400          BIC   #177400,R4 ; CLEAR UNWANTED BITS.
012234 012705 000204          MOV   #204,R5 ; SET EXPECTED.
012240 104004          HLT   4
012242 104412          3$: MSTCLR
012244 032777 000020 167106  BIT     #BIT4,@DQRCR
012252 001406          BEQ   4$
012254 005005          CLR   R5
012256 017704 167076          MOV   @DQRCR,R4
012262 042704 177400          BIC   #177400,R4
012266 104004          HLT   4
012270 104400          4$: SCOPE

```

```

;TRANSMITTER P/S MASTER CLEAR TEST
;EXECUTE 1 NPR CYCLE TO FORCE TRANSMITTER P/S TO A 1
;ISSUE MASTER CLEAR
;VERIFY THAT TRANSMITTER P/S WAS CLEARED

```

; TEST 62

```

*****
012272 012737 000062 001226 TST62: MOV     #62,TSTNO
012300 012737 012324 001214  MOV     #1$,RETURN

```

```

3000 012306 012737 012442 001216      MOV      #TST63,NEXT
3001 012314 012737 000340 177776      MOV      #340,PS                ;LOCK OUT INTERRUPTS.
3002 012322 104413                                MEMCLR
3003 012324 104412                                MSTCLR                ;MASTER CLEAR INTERFACE
3004 012326 004737 016024                                JSR      PC,SETMNT      ;SET MAINTENANCE MODE
3005 012332 004737 016122                                JSR      PC,SETBABC
3006 012336 002      000      .BYTE 2,0
3007 012340 017170                                TBUFF
3008 012342 177777                                -1
3009 012344 052777 000001 167012      BIS      #BIT0,DDQTCR
3010 012352 012737 002000 001244      MOV      #2000,TEMP1          ;SET FOR TIME OUT
3011 012360 105777 167000      2$:      TSTB      DDQTCR          ;PRIMARY DONE UP
3012 012364 100412                                BMI      3$                ;BR IF PRI DONE SET.
3013 012366 005337 001244                                DEC      TEMP1             ;DELAY
3014 012372 001372                                BNE      2$                ;KEEP WAITING
3015 012374 017704 166764                                MOV      DDQTCR,R4         ;SAVE THE CSR
3016 012400 042704 177400                                BIC      #177400,R4        ;CLEAR UNWANTED BITS.
3017 012404 012705 000204                                MOV      #204,R5          ;SET EXPECTED.
3018 012410 104005                                HLT      5
3019 012412 104412                                3$:      MSTCLR
3020 012414 032777 000020 166742      BIT      #BIT4,DDQTCR
3021 012422 001406                                BEQ      4$
3022 012424 005005                                CLR      R5
3023 012426 017704 166732                                MOV      DDQTCR,R4
3024 012432 042704 177400                                BIC      #177400,R4
3025 012436 104005                                HLT      5
3026 012440 104400                                4$:      SCOPE
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3055
; TRANSMITTER NPR DATA TEST (STEP MODE)
; EXECUTE 1 TRANSMITTER NPR CYCLE FOR EACH DATA PATTERN 0-177777
; VERIFY THAT TRANSMITTER BUFFER CONTAINS THE CORRECT DATA
; TEST 63
; *****
TST63: MOV      #63,TSTNO
      MOV      #1$,RETURN
      MOV      #10,ICOUNT
      MOV      #.EOP,NEXT
      MOV      #2$,LOCK
      MOV      #340,PS                ;LOCK OUT INTERRUPTS.
      MEMCLR                ;CLEAR ALL MEMORIES
      MSTCLR                ;INITIALIZE DEVICE
      CLR      ZDATA          ;CLEAR POINTER
      MOV      #0,R0
      MOV      DQSEC,R3
      MOV      #13,R2
      2$:      MSTCLR
      JSR      PC,SETSTP      ;SET FOR ERROR
      JSR      PC,SETBABC     ;SET FOR ERROR (TX MUX)
      .BYTE 2,0                ;GIVE ANOTHER MASTER CLEAR
      TBUFF
      -1
      MOV      ZDATA,R5
      MOV      R5,TBUFF        ;SET EXPECTED
      MOV      #BIT0,DDQTCR    ;LOAD CHARACTER
      MOV      #2000,TEMP1     ;SET TX GO.
      ;SET FOR DELAY

```

```

3056 012576 105777 166562      3$:  TSTB  @DQTCR      ;TX PRI DONE?
3057 012602 100404                BMI  4$          ;BR IF YES
3058 012604 005337 001244          DEC  TEMP1      ;DELAY
3059 012610 001372                BNE  3$          ;KEEP DELAYING
3060 012612 104003                HLT  3          ;TX PRI DONE FAILED TO SET
3061 012614 112777 000013 166546 4$:  MOVB  #13,@DQREG ;SELECT TX MUX REG.
3062 012622 017704 166544          MOV  @DQSEC,R4 ;READ MUX
3063 012626 020504                CMP  R5,R4      ;GOOD CHARACTER?
3064 012630 001401                BEQ  5$          ;BR IF GOOD
3065 012632 104012                HLT  12         ;DATA COMPARISON ERROR
3066 012634 104401                SCOPI           ;LOCK ON DATA (SW09=1)
3067 012636 005237 017172          INC  ZDATA      ;UPDATE CHARACTER
3068 012642 005300                DEC  R0          ;UPDATE COUNTER
3069 012644 001332                BNE  2$          ;GO DO MORE CHARACTERS
3070 012646 104400                6$:  SCOPE        ;SCOPE THIS TEST.
3071
3072
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3078 012650 005037 001234      .EOP: CLR  LSTERR     ;CLEAR LAST ERROR PC
3079 012654 005037 001312          CLR  ERRFLG    ;CLEAR ERROR FLAG
3080 012660 005237 001230          INC  PASCNT    ;UPDATE PASS COUNT
3081 012664 104402                TYPE
3082 012666 015100                MEPASS
3083 012670 104402                TYPE
3084 012672 015261                MCSRX
3085 012674 104411                CNVRT
3086 012676 013006                XCSR
3087 012700 104402                TYPE
3088 012702 015267                MVECX
3089 012704 104411                CNVRT
3090 012706 013014                XVEC
3091 012710 104402                TYPE
3092 012712 015275                MPASSX
3093 012714 104411                CNVRT
3094 012716 013022                XPASS
3095 012720 104402                TYPE
3096 012722 015306                MERRX
3097 012724 104411                CNVRT
3098 012726 013030                XERR
3099 012730 013777 001230 166244    MOV  PASCNT,@LIGHTS ;DISPLAY PASS COUNT
3100 012736 005337 001276          DEC  SAVNUM
3101 012742 001013                BNE  RESTR
3102 012744 013737 001504 001276    MOV  DQNUM,SAVNUM
3103 012752 013701 000042          MOV  @#42,R1
3104 012756 001405                BEQ  RESTR      ;CHECK FOR ACT-11 OR DDP
3105 012760 000005                RESET          ;IF NOT, CONTINUE TESTING
3106 012762
3107 012762 004711                LOGICAL: JSR  PC,(R1)
3108 012764 000240                NOP
3109 012766 000240                NOP
3110 012770 000240                NOP
3111 012772 104414                RESTRT: CKSWR

```

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 DZDQCC.P11 END OF PASS ROUTINE

3112	012774	012737	002254	001214		MOV	#TST1, RETURN
3113	013002	000137	002254			JMP	TST1
3114	013006	000001			XCSR:	1	
3115	013010	006	002			.BYTE	6,2
3116	013012	001360				DQRCSR	
3117	013014	000001			XVEC:	1	
3118	013016	003	002			.BYTE	3,2
3119	013020	001350				DQRVEC	
3120	013022	000001			XPASS:	1	
3121	013024	006	002			.BYTE	6,2
3122	013026	001230				PASCNT	
3123	013030	000001			XERR:	1	
3124	013032	006	002			.BYTE	6,2
3125	013034	001232				ERRCNT	
3126							
3127							
3128							
3129	013036	104414					
3130	013040	032777	040000	166132	.SCOPE:	CKSWR	
3131	013046	001407			TTST:	BIT	#BIT14, @SWR
3132	013050	000432				BEQ	1\$
3133	013052	105777	166126			BR	3\$
3134	013056	100027				TSTB	@TKCSR
3135	013060	017700	166122			BPL	3\$
3136	013064	000412				MOV	@TKDBR, R0
3137	013066	032777	004000	166104	1\$:	BR	2\$
3138	013074	001006				BIT	#SW11, @SWR
3139	013076	005237	001224			BNE	2\$
3140	013102	023737	001224	001222		INC	LPCNT
3141	013110	001012				CMP	LPCNT, ICOUNT
3142	013112	105037	001312		2\$:	BNE	3\$
3143	013116	005037	001224			CLRB	ERRFLG
3144	013122	012737	000012	001222		CLR	LPCNT
3145	013130	013737	001216	001214		MOV	#10., ICOUNT
3146	013136	013716	001214		3\$:	MOV	NEXT, RETURN
3147	013142	000002				MOV	RETURN, (SP)
3148	013144	001407			BRW:	RTI	
3149	013146	000432			BRX:	1407	
3150						432	
3151							
3152							
3153	013150	104414					
3154	013152	032777	001000	166020	.SCOPE1:	CKSWR	
3155	013160	001402				BIT	#SW09, @SWR
3156	013162	013716	001220			BEQ	1\$
3157	013166	000002			1\$:	MOV	LOCK, (SP)
3158						RTI	
3159							
3160							
3161	013170	010546			.TYPE:	MOV	R5, -(SP)
3162	013172	017605	000002			MOV	@2(SP), R5
3163	013176	062766	000002	000002		ADD	#2, 2(SP)
3164	013204	005737	014660		1\$:	TST	@#RDSW
3165	013210	001004				BNE	300\$
3166	013212	032777	010000	165760		BIT	#SW12, @SWR
3167	013220	001024				BNE	3\$

;SCOPE LOOP AND INTERATION HANDLER

;CHECK FOR FREEZE ON CURRENT DATA

;TELETYPE OUTPUT ROUTINE

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 DZDQCC.P11 GENERAL UTILITIES (TYPE OUT, ERROR, SCOPE, ETC.)

3168	013222	105715			300\$:	TSTB	(R5)
3169	013224	100014				BPL	2\$
3170	013226	105777	165756			TSTB	@TPCSR
3171	013232	100375				BPL	-4
3172	013234	012777	000015	165750		MOV	#15, @TPDDBR
3173	013242	105777	165742			TSTB	@TPCSR
3174	013246	100375				BPL	-4
3175	013250	012777	000012	165734		MOV	#12, @TPDDBR
3176	013256	105777	165726		2\$:	TSTB	@TPCSR
3177	013262	100375				BPL	2\$
3178	013264	112577	165722			MOVB	(R5)+, @TPDDBR
3179	013270	001345				BNE	1\$
3180	013272	012605			3\$:	MOV	(SP)+, R5
3181	013274	000002				RTI	

;ASCII STRING INPUT ROUTINE

3182							
3183							
3184							
3185	013276	010346			.INSTR:	MOV	R3, -(SP)
3186	013300	010446				MOV	R4, -(SP)
3187	013302	017637	000004	013320		MOV	@4(SP), .MSG
3188	013310	062766	000002	000004		ADD	#2, 4(SP)
3189	013316	104402			.INST1:	TYPE	
3190	013320	000000			.MSG:	0	
3191	013322	012704	015452			MOV	#INBUF, R4
3192	013326	012703	000007			MOV	#7, R3
3193	013332	105777	165646		1\$:	TSTB	@TKCSR
3194	013336	100375				BPL	1\$
3195	013340	117714	165642			MOVB	@TKDDBR, (R4)
3196	013344	142714	000200			BICB	#200, (R4)
3197	013350	121427	000025			CMPB	(R4), #25
3198	013354	001003				BNE	200\$
3199	013356	104402	015040			TYPE, MCRLF	
3200	013362	000755				BR	.INST1
3201	013364	122427	000015		200\$:	CMPB	(R4)+, #15
3202	013370	001423				BEQ	INSTR2
3203	013372	117777	165610	165612		MOVB	@TKDDBR, @TPDDBR
3204	013400	105777	165604		2\$:	TSTB	@TPCSR
3205	013404	100375				BPL	2\$
3206	013406	005303				DEC	R3
3207	013410	001350				BNE	1\$
3208	013412	000402				BR	.INSTG
3209	013414	010346			.INSTE:	MOV	R3, -(SP)
3210	013416	010446				MOV	R4, -(SP)
3211	013420	104402			.INSTG:	TYPE	
3212	013422	015034				MQM	
3213	013424	005737	014660			TST	@#RDSW
3214	013430	001402				BEQ	400\$
3215	013432	104402	015040			TYPE, MCRLF	
3216	013436	000727			400\$:	BR	.INST1
3217	013440	012604			INSTR2:	MOV	(SP)+, R4
3218	013442	012603				MOV	(SP)+, R3
3219	013444	000002				RTI	

;IS IT <↑G>

;CONVERT ASCII STRING TO OCTAL

3220							
3221							
3222							
3223	013446	010546			.PARAM:	MOV	R5, -(SP)

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 DZDQCC.P11 GENERAL UTILITIES (TYPE OUT,ERROR,SCOPE,ETC.)

3224	013450	010446		MOV	R4, -(SP)	
3225	013452	016605	000004	MOV	4(SP), R5	
3226	013456	012537	013652	MOV	(R5)+, LOLIM	
3227	013462	012537	013654	MOV	(R5)+, HILIM	
3228	013466	012537	013656	MOV	(R5)+, DEVADR	
3229	013472	112537	013660	MOVB	(R5)+, LOBITS	
3230	013476	112537	013661	MOVB	(R5)+, ADRCNT	
3231	013502	010566	000004	MOV	R5, 4(SP)	
3232	013506	005005		PARAM1: CLR	R5	
3233	013510	012704	015452	MOV	#INBUF, R4	
3234	013514	122714	000015	CMPB	#15, (R4)	
3235	013520	001420		BEQ	PARERR	
3236	013522	121427	000060	1\$: CMPB	(R4), #60	
3237	013526	002415		BLT	PARERR	
3238	013530	121427	000067	CMPB	(R4), #67	
3239	013534	003012		BGT	PARERR	
3240	013536	142714	000060	BICB	#60, (R4)	
3241	013542	152405		BISB	(R4)+, R5	
3242	013544	122714	000015	CMPB	#15, (R4)	
3243	013550	001414		BEQ	LIMITS	
3244	013552	006305		ASL	R5	
3245	013554	006305		ASL	R5	
3246	013556	006305		ASL	R5	
3247	013560	000760		BR	1\$	
3248	013562	122714	000015	PARERR: CMPB	#15, (R4)	; IS FIRST CHARACTER A <CR>
3249	013566	001003		BNE	120\$	
3250	013570	005737	014660	TST	#ARDSW	; IS CKSWR ROUTINE BEING USED
3251	013574	001023		BNE	PARTI	
3252	013576	104404		120\$: INSTER		
3253	013600	000742		BR	PARAM1	
3254						
3255						; TEST TO SEE IF NUMBER IS WITHIN LIMITS
3256						
3257	013602	020537	013654	LIMITS: CMP	R5, HILIM	
3258	013606	101365		BHI	PARERR	
3259	013610	020537	013652	CMP	R5, LOLIM	
3260	013614	103762		BLO	PARERR	
3261	013616	133705	013660	BITB	LOBITS, R5	
3262	013622	001357		BNE	PARERR	
3263						
3264						; STORE NUMBER AT SPECIFIED ADDRESS
3265						
3266	013624	013704	013656	1\$: MOV	DEVADR, R4	
3267	013630	010524		MOV	R5, (R4)+	
3268	013632	062705	000002	ADD	#2, R5	
3269	013636	105337	013661	DECB	ADRCNT	
3270	013642	001372		BNE	1\$	
3271	013644	012604		PARTI: MOV	(SP)+, R4	
3272	013646	012605		MOV	(SP)+, R5	
3273	013650	000002		RTI		
3274	013652	000000		LOLIM: 0		
3275	013654	000000		HILIM: 0		
3276	013656	000000		DEVADR: 0		
3277	013660	000000		LOBITS: 0		
3278		013661		ADRCNT=LOBITS+1		
3279						

```

3280                                     ;SAVE PC OF TEST THAT FAILED AND RO-R5
3281
3282 013662 016637 000004 001274 .SAV05: MOV     4(SP),SAVPC
3283
3284                                     ;SAVE RO-R5
3285
3286 013670 010537 001270          SV05:  MOV     R5,SAVR5
3287 013674 010437 001266          MOV     R4,SAVR4
3288 013700 010337 001264          MOV     R3,SAVR3
3289 013704 010237 001262          MOV     R2,SAVR2
3290 013710 010137 001260          MOV     R1,SAVR1
3291 013714 010037 001256          MOV     R0,SAVR0
3292 013720 000002          RTI
3293
3294                                     ;RESTORE RO-R5
3295
3296 013722 013700 001256          .RES05: MOV    SAVR0,R0
3297 013726 013701 001260          MOV    SAVR1,R1
3298 013732 013702 001262          MOV    SAVR2,R2
3299 013736 013703 001264          MOV    SAVR3,R3
3300 013742 013704 001266          MOV    SAVR4,R4
3301 013746 013705 001270          MOV    SAVR5,R5
3302 013752 000002          RTI
3303
3304                                     ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
3305
3306 013754 104402          .CONVR: TYPE
3307 013756 015040          MCRLF
3308 013760 010046          .CNVRT: MOV    R0,-(SP)
3309 013762 010146          MOV    R1,-(SP)
3310 013764 010346          MOV    R3,-(SP)
3311 013766 010446          MOV    R4,-(SP)
3312 013770 010546          MOV    R5,-(SP)
3313 013772 017601 000012          MOV    @12(SP),R1
3314 013776 013737 015514 001250          MOV    TEMP,TEMP3
3315 014004 062766 000002 000012          ADD    #2,12(SP)
3316 014012 012137 014174          MOV    (R1)+,WRDCNT
3317 014016 112137 014176          1$:  MOVB  (R1)+,CHRCNT
3318 014022 112137 014177          MOVB  (R1)+,SPACNT
3319 014026 013137 014200          MOV    @2(R1)+,BINWRD
3320 014032 013704 014200          2$:  MOV    BINWRD,R4
3321 014036 113705 014176          MOVB  CHRCNT,R5
3322 014042 012700 015514          MOV    #TEMP,R0
3323 014046 010403          3$:  MOV    R4,R3
3324 014050 042703 177770          BIC    #177770,R3
3325 014054 062703 000060          ADD    #060,R3
3326 014060 110320          MOVB  R3,(R0)+
3327 014062 000241          CLC
3328 014064 006004          ROR    R4
3329 014066 000241          CLC
3330 014070 006004          ROR    R4
3331 014072 000241          CLC
3332 014074 006004          ROR    R4
3333 014076 005305          DEC    R5
3334 014100 001362          BNE    3$
3335 014102 012703 015556          MOV    #MDATA,R3
  
```


3336	014106	114023		4\$:	MOVB	-(R0), (R3)+	
3337	014110	105337	014176		DECB	CHRCNT	
3338	014114	001374			BNE	4\$	
3339	014116	105737	014177		TSTB	SPACNT	
3340	014122	001405			BEQ	6\$	
3341	014124	112723	000040	5\$:	MOVB	#040, (R3)+	
3342	014130	105337	014177		DECB	SPACNT	
3343	014134	001373			BNE	5\$	
3344	014136	105013		6\$:	CLRB	(R3)	
3345	014140	104402			TYPE		
3346	014142	015556			MDATA		
3347	014144	005337	014174		DEC	WRDCNT	
3348	014150	001322			BNE	1\$	
3349	014152	013737	001250 015514		MOV	TEMP3, TEMP	
3350	014160	012605			MOV	(SP)+, R5	
3351	014162	012604			MOV	(SP)+, R4	
3352	014164	012603			MOV	(SP)+, R3	
3353	014166	012601			MOV	(SP)+, R1	
3354	014170	012600			MOV	(SP)+, R0	
3355	014172	000002			RTI		
3356	014174	000000			WRDCNT:	0	
3357	014176	000000			CHRCNT:	0	
3358		014177			SPACNT=	CHRCNT+1	
3359	014200	000000			BINWRD:	0	
3360							; TRAP DISPATCH SERVICE
3361							; ARGUMENT OF TRAP IS EXTRACTED
3362							; AND USED AS OFFSET TO OBTAIN POINTER
3363							; TO SELECTED SUBROUTINE
3364							
3365	014202	011646		.TRPSR:	MOV	(SP), -(SP)	; GET PC OF RETURN
3366	014204	162716	000002		SUB	#2, (SP)	; =PC OF TRAP
3367	014210	017616	000000		MOV	@(SP), (SP)	; GET TRAP
3368	014214	006316		TRPOK:	ASL	(SP)	; MULTIPLY TRAP ARG BY 2
3369	014216	042716	177001		BIC	#177001, (SP)	; CLEAR UNWANTED BITS
3370	014222	062716	001314		ADD	#.TRPTAB, (SP)	; POINTER TO SUBROUTINE ADDRESS
3371	014226	017616	000000		MOV	@(SP), (SP)	; SUBROUTINE ADDRESS
3372	014232	000136			JMP	@(SP)+	; GO TO SUBROUTINE
3373							
3374							; ERROR HANDLER
3375							
3376	014234	104414		.HLT:	CKSWR		
3377	014236	032777	010000 164734		BIT	#SW12, @SWR	
3378	014244	001406			BEQ	XBX	
3379	014246	105777	164736		TSTB	@TPCSR	
3380	014252	100003			BPL	XBX	
3381	014254	112777	000207 164730		MOVB	#207, @TPDBR	
3382	014262	032777	020000 164710	XBX:	BIT	#SW13, @SWR	
3383	014270	001074			BNE	HALTS	
3384	014272	021637	001234		CMP	(SP), LSTERR	
3385	014276	001404			BEQ	1\$	
3386	014300	011637	001234		MOV	(SP), LSTERR	
3387	014304	105037	001312		CLRB	ERRFLG	
3388	014310	104406		1\$:	SAVOS		
3389	014312	011605			MOV	(SP), R5	
3390	014314	162705	000002		SUB	#2, R5	
3391	014320	011504			MOV	(R5), R4	

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DZDQCC.P11 GENERAL UTILITIES (TYPE OUT, ERROR, SCOPE, ETC.)

3392	014322	006304			ASL	R4
3393	014324	061504			ADD	(R5),R4
3394	014326	006304			ASL	R4
3395	014330	042704	177001		BIC	#177001,R4
3396	014334	062704	016744		ADD	#.ERRTAB,R4
3397	014340	012437	014432		MOV	(R4)+,ERRMSG
3398	014344	012437	014444		MOV	(R4)+,DATAHD
3399	014350	011437	014456		MOV	(R4),DATABP
3400	014354	105737	001312		TSTB	ERRFLG
3401	014360	001403			BEQ	TYPMSG
3402	014362	005737	014456		TST	DATABP
3403	014366	001027			BNE	TYPDAT
3404	014370	104402			TYPMSG:	TYPE
3405	014372	015317			MTSTN	
3406	014374	104411			CNVRT	
3407	014376	014556			XTSTN	
3408	014400	104402			TYPE	
3409	014402	015405			MERRPC	
3410	014404	104411			CNVRT	
3411	014406	014550			ERTABO	
3412	014410	104402			TYPE	
3413	014412	015040			MCRLF	
3414	014414	112737	177777	001312	MOVB	#-1,ERRFLG
3415	014422	005737	014432		TST	ERRMSG
3416	014426	001402			BEQ	WRKO.FM
3417	014430	104402			TYPE	
3418	014432	000000			ERRMSG:	0
3419	014434				WRKO.FM:	
3420	014434	005737	014444		TST	DATAHD
3421	014440	001402			BEQ	TYPDAT
3422	014442	104402			TYPE	
3423	014444	000000			DATAHD:	0
3424	014446	005737	014456		TYPDAT:	TST
3425	014452	001402			BEQ	DATABP
3426	014454	104410			CONVRT	RESREG
3427	014456	000000			DATABP:	0
3428	014460	104407			RESREG:	RESOS
3429	014462	005777	164512		HALTS:	TST
3430	014466	100005			BPL	2SWR
3431	014470	010046			PUSHRO	EXITER
3432	014472	016600	000002		MOV	2(SP),R0
3433	014476	000000			HALT	
3434	014500	012600			POPPO	
3435	014502	104414			EXITER:	CKSWR
3436	014504	005237	001232		INC	ERRCNT
3437	014510	032777	000400	164462	BIT	#SW08,2SWR
3438	014516	001007			BNE	1\$
3439	014520	032777	002000	164452	BIT	#SW10,2SWR
3440	014526	001407			BEQ	2\$
3441	014530	013737	001216	001214	MOV	NEXT,RETURN
3442	014536	012706	001200		1\$:	MOV
3443	014542	000177	164446		JMP	#STACK,SP
3444	014546	000002			2\$:	RTI
3445	014550	000001			ERTABO:	1
3446	014552	006	002		.BYTE	6,2
3447	014554	001274			SAVPC	

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000777

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012706
001200
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001234
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4342
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005737
000042
001042
022737
000176
001200
001036
164300
105777
164300
017737
164274
013320
042737
177600
013320
122737
000007
013320
001021
104402
015010
005137
014660
104402
015014
104411
015002
104403
015023
104405
000000

XTSTN: 1
.BYTE 3,2
TSTNO
:ENTER HERE ON POWER FAILURE

.PFAIL:
MOV #RESTART,24 ;SET UP FOR POWER UP TRAP
HALT ;HALT ON POWER DOWN NORMAL
BR .
:PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED

RESTAR:
MOV #.PFAIL,24 ;SET UP FOR POWER FAILURE
MOV #STACK,SP
CLR TEMP
INC TEMP
BNE .-4
TYPE
MFAIL
CNVRT
PFTAB
CLR ERRFLG
CLR LSTERR
MSTCLR
MEMCLR
JMP @RETURN

PFTAB:
1
.BYTE 3,2
TSTNO

:CHECK SWITCH REGISTER ROUTINE. CHECKS FOR IG TO ALLOW CHANGING
:OF LOC.176.
:LOCATIONS USED:
RDSW: .WORD 0

.CKSWR: TST @#42
BNE OUT
CMP #SWREG,SWR ;SOFTWARE SWITCH REGISTER PRESENT
BNE OUT ;NO GET OUT
TSTB @TKCSR ;YES, WAIT FOR
BPL OUT ;READY, GET CHARACTER
MOV @TKDPR,.MSG ;AND STRIP OFF
BIC #177600,.MSG ;THE GARBAGE
CMPB #7,.MSG ;IS IT A (<IG>
BNE OUT
TYPE,SCNTG

.CNTLU: COM @RDSW
TYPE,SMWR
CNVRT,SWREG
INSTR,SMNEW
PARAM
0

014762	177777			177777	
014764	000176			SWREG	
014766	000	001		.BYTE	0,1
014770	104402	015040		TYPE, MCRLF	
014774	005037	014660		OUT: CLR	3#RDSW
015000	000002			RTI	
015002	000001			SWREGC: 1	
015004	000	002		.BYTE	6,2
015006	000176			SWREG	
015010	057377	000107		\$CNTG: .ASCIZ	<377>/IG/
015014	051777	051127	020075	\$MSWR: .ASCIZ	<377>/SWR= /
015022	000				
015023	040	047040	053505	\$MNEW: .ASCIZ	/ NEW= /
015030	020075	000			
	015034			.EVEN	
015034	020040	000077		MQM: .ASCIZ	/ ?/
015040	000377			MCRLF: .ASCIZ	<377>
015042	050377	051127	043040	MPFAIL: .ASCIZ	<377>/PWR FAILED. RESTART AT TEST /
015050	044501	042514	027104		
015056	051040	051505	040524		
015064	052122	040440	020124		
015074	042524	052123	000040		
015100	042777	042116	050040	MEPASS: .ASCIZ	<377>/END PASS DZDQC /
015106	051501	020123	055104		
015114	050504	020103	000040		
015122	051377	000		MR: .ASCIZ	<377>/R/
015122	0377	051120	043517	MERR2: .ASCIZ	<377>/PROGRAM INDICATES NO DEVICES PRESENT./
015122	040522	020115	047111		
015140	044504	040503	042524		
015146	020123	047516	042040		
015154	052105	041511	051505		
015162	050040	042522	042523		
015170	052116	000056			
015174	044777	051516	043125	MERR3: .ASCIZ	<377>/INSUFFICIENT DATA! /
015202	044506	044503	047105		
015210	020124	040504	040524		
015216	000041				
015220	052377	051505	020124	MTSTPC: .ASCIZ	<377>/TEST PC- /
015226	041520	000055			
015232	046377	041517	020113	MLOCK: .ASCIZ	<377>/LOCK ON SELECTED TEST /
015240	047117	051440	046105		
015244	041505	042524	020104		
015254	042524	052123	000		
015256	103	051123	020072	MCSRX: .ASCIZ	/CSR: /
015266	000				
015267	126	041505	020072	MVECX: .ASCIZ	/VEC: /
015274	000				
015275	120	051501	042523	MPASSX: .ASCIZ	/P : /
015302	035123	000040			
015306	051105	047522	051522	MERRX: .ASCIZ	/ERRORS: /
015314	020072	000			
015317	377	052377	051505	M...TN: .ASCIZ	<377><377> /TEST NO: /
015324	020124	047516	020072		
015332	000				
015333	377	042523	020124	MNEW: .ASCIZ	<377>/SET SWITCH REG TO DQ11'S DESIRED ACTIVE. /
015340	053523	052111	044103		

015346	051040	043505	052040		
015354	020117	050504	030461		
015362	051447	042040	051505		
015370	051111	042105	040440		
015376	052103	053111	027105		
015404	000				
015405	120	035103	000040	MERRPC:	.ASCIZ /PC: /
015412	046777	050101	047440	XHEAD:	.ASCIZ <377>/MAP OF DQ11 STATUS/<377>
015420	020106	050504	030461		
015426	051440	040524	052524		
015434	177523	000			
	015440			.EVEN	
015440	000002			XSTATQ:	2
015442	006	003		.BYTE	6,3
015444	001244			TEMP1	
015446	006	002		.BYTE	6,2
015450	001246			TEMP2	
				.EVEN	
				;BUFFERS FOR INPUT-OUTPUT	
015452	000000			INBUF:	0
	015514			= +40	
015514	000000			TEMP:	0
	015556			= +40	
015556	000000			MDATA:	0
	015620			= +40	
				;MASTER CLEAR DQ11 INTERFACE	
015620				.MSTCLR:	
015620	112777	000012	163542	MOVB	#12, DQREG
015626	012777	000040	163536	MOV	#BITS, DQSEC
015634	000002			RTI	
				;CLEAR INTERFACE MEMORIES	
015636				.MEMCLR:	
015636	105077	163526		CLRB	DQREG
015642	012700	000020		MOV	#16, R0
015646	152777	000020	163514	BISB	#BIT4, DQREG
015654	142777	000140	163506	BICB	#140, DQREG
015662	005077	163504		CLR	DQSEC
015666	105277	163476		INCB	DQREG
015672	005300			DEC	R0
015674	001364			BNE	1\$
015676	105077	163466		CLRB	DQREG
015702	105077	163454		CLRB	DQRC SH
015706	012700	000020		MOV	#16, R0
015712	112777	000010	163450	MOVB	#10, DQREG
015720	005077	163446		CLR	DQSEC
015724	112777	000014	163436	MOVB	#14, DQREG
015732	005077	163434		CLR	DQSEC
015736	105277	163420		INCB	DQRC SH
015742	005300			DEC	R0
015744	001362			BNE	2\$

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 DZDQCC.P11 GENERAL UTILITIES (TYPE OUT, ERROR, SCOPE, ETC.)

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3616 015746 105077 163410 CLRB 3DQRC5H
3617 015752 005077 163402 CLR 3DQRC5R
3618 015756 005077 163402 CLR 3DQTC5R
3619 015762 005077 163400 CLR 3DQERR
3620 015766 000002 RTI
;SET STEP MODE
3621 015770 112777 000012 163372 SETSTP: MOVB #12,3DQREG
3622 015776 052777 000002 163366 BIS #BIT1,3DQSEC
3623 016004 000207 RTS PC
;SET TEST LOOP
3624 016006 112777 000012 163354 SETLOP: MOVB #12,3DQREG
3625 016014 052777 000010 163350 BIS #BIT3,3DQSEC
3626 016022 000207 RTS PC
;SET MAINTENANCE MODE
3627 016024 112777 000012 163336 SETMNT: MOVB #12,3DQREG
3628 016032 052777 000012 163332 BIS #BIT1+BIT3,3DQSEC
3629 016040 000207 RTS PC
;SET INTERRUPT VECTORS
3630 016042 011605 SETV: MOV (SP),R5
3631 016044 012577 163300 MOV (R5)+,3DQRV5C
3632 016050 012777 000340 163274 MOV #340,3DQRLVL
3633 016056 012577 163272 MOV (R5)+,3DQTV5C
3634 016062 012777 000340 163266 MOV #340,3DQTLVL
3635 016070 010516 MOV R5,(SP)
3636 016072 000207 RTS PC
;RESTORE TRAPCATCHER
3637 016074 013777 001352 163246 RECAT: MOV DQRLVL,3DQRV5C
3638 016102 005077 163244 CLR 3DQRLVL
3639 016106 013777 001356 163240 MOV DQTLVL,3DQTV5C
3640 016114 005077 163236 CLR 3DQTLVL
3641 016120 000207 RTS PC
;SET UP BUS ADDRESS AND CHARACTER COUNTS
;FOR SELECTED FUNCTION
3642 016122 011605 SETBABC: MOV (SP),R5
3643 016124 112577 163240 MOVB (R5)+,3DQREG
3644 016130 152777 000020 163232 BISB #BIT4,3DQREG
3645 016136 152577 163226 BISB (R5)+,3DQREG
3646 016142 012577 163224 MOV (R5)+,3DQSEC
3647 016146 142777 000040 163214 BICB #BIT5,3DQREG
3648 016154 105277 163210 INCB 3DQREG
3649 016160 012577 163206 MOV (R5)+,3DQSEC
3650 016164 010516 MOV R5,(SP)
3651 016166 000207 RTS PC

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; TABLE OF ERROR MESSAGES

016170	042522	042503	053111	EM0:	.ASCIZ /RECEIVER DID NOT INTERRUPT/
016223	124	040522	051516	EM1:	.ASCIZ /TRANSMITTER DID NOT INTERRUPT/
016261	125	042516	050130	EM2:	.ASCIZ /UNEXPECTED TRANSMITTER INTERRUPT/
016322	047125	054105	042520	EM3:	.ASCIZ /UNEXPECTED RECEIVER INTERRUPT/
016360	042522	042503	053111	EM4:	.ASCIZ /RECEIVER STATUS ERROR/
016406	051124	047101	046523	EM5:	.ASCIZ /TRANSMITTER STATUS ERROR/
016437	105	051122	051117	EM6:	.ASCIZ /ERROR FLAG(S) SET/
016461	102	051525	040440	EM7:	.ASCIZ /BUS ADDRESS ERROR/
016503	103	040510	040522	EM10:	.ASCIZ /CHARACTER COUNT ERROR/
016531	122	041505	044505	EM11:	.ASCIZ /RECEIVED DATA ERROR/
016555	124	040522	051516	EM12:	.ASCIZ /TRANSMITTER BUFFER DATA ERROR/
016613	103	047514	045503	EM13:	.ASCIZ /CLOCK LOSS ERROR/

; TABLE OF DATA HEADERS

016634	042777	050130	041505	DH0:	.ASCIZ <377>/EXPECTED RECEIVED REG ADDRESS/
016675	377	054105	042520	DH1:	.ASCIZ <377>/EXPECTED RECEIVED SEC ADR SEC REG/
				.EVEN	

3676
 3677
 3678
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 3680
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 3682
 3683
 3684
 3685
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 3688
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 3696
 3697
 3698
 3699
 3700
 3701
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 3705
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 3709

; TABLE OF POINTERS FOR ERROR OUTPUT

.ERRTAB:EM0
 0
 0
 0
 EM1
 0
 0
 0
 EM2
 0
 0
 0
 EM3
 0
 0
 0
 EM4
 DH0
 DT0
 EMS
 DH0
 DT1
 EM6
 DH0
 DT4
 EM7
 DH1
 DT3
 EM10
 DH1
 DT3
 EM11
 DH0
 DT4
 EM12
 DH1

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 DZDQCC.P11 GENERAL UTILITIES (TYPE OUT, ERROR, SCOPE, ETC.)

3710	017044	017126			DT3
3711	017046	016613			EM13
3712	017050	016634			DHO
3713	017052	017110			DT2
3714					
3715					
3716					:DATA TABLES FOR ERROR OUTPUT
3717	017054	000003			DT0:
3718	017056	006	004		3
3719	017060	001270			.BYTE 6.4
3720	017062	006	004		SAVR5
3721	017064	001266			.BYTE 6.4
3722	017066	006	004		SAVR4
3723	017070	001360			.BYTE 6.4
3724	017072	000003			DQRCR
3725	017074	006	004		DT1:
3726	017076	001270			3
3727	017100	006	004		.BYTE 6.4
3728	017102	001266			SAVR5
3729	017104	006	004		.BYTE 6.4
3730	017106	001364			SAVR4
3731	017110	000003			.BYTE 6.4
3732	017112	003	007		DQTCR
3733	017114	001270			DT2:
3734	017116	003	007		3
3735	017120	001266			.BYTE 3.7
3736	017122	006	000		SAVR5
3737	017124	001366			.BYTE 3.7
3738	017126	000004			SAVR4
3739	017130	006	004		.BYTE 6.0
3740	017132	001270			DQERR
3741	017134	006	004		DT3:
3742	017136	001266			4
3743	017140	006	004		.BYTE 6.4
3744	017142	001372			SAVR5
3745	017144	002	000		.BYTE 6.4
3746	017146	001262			SAVR4
3747	017150	000003			.BYTE 6.4
3748	017152	006	004		DQSEC
3749	017154	001270			2.0
3750	017156	006	004		SAVR2
3751	017160	001266			DT4:
3752	017162	006	004		3
3753	017164	001264			.BYTE 6.4
3754	017166	000000			SAVR5
3755	017170	000000			.BYTE 6.4
3756	017172	000000			SAVR4
3757		000001			.BYTE 6.4
					SAVR3
					RBUFF: 0
					TBUFF: 0
					ZDATA: 0
					.END

LSTERR	001234	1069#	1216*	3078*	3384	3386*	3472*							
MCRLF	015040	3199	3215	3307	3413	3507	3520#							
MCSRX	015261	3084	3547#											
MDATA	015556	3335	3346	3585#										
MEMCLR=	104413	1132#	1382	1416	2459	2541	2641	2720	2722	2741	2821	2896	2963	3002
		3040	3474											
MEPASS	015100	3082	3526#											
MERRPC	015405	3409	3566#											
MERRX	015306	3096	3553#											
MERR2	015125	1029	1332	3530#										
MERR3	015174	1264	3537#											
MISC. =	000012	643#												
MLOCK	015232	1289	3543#											
MNEW	015333	1257	3558#											
MPASSX	015275	3092	3551#											
MPFAIL	015042	3468	3521#											
MQM	015034	3212	3519#											
MR	015122	1306	3529#											
MSTCLR=	104412	1130#	1383	1418	1448	1471	1494	1517	1540	1568	1591	1614	1637	1660
		1683	1706	1729	1752	1775	1798	1821	1844	1873	1897	1921	1945	1971
		1997	2023	2049	2075	2101	2127	2153	2179	2206	2235	2263	2296	2326
		2356	2386	2424	2460	2542	2622	2721	2822	2897	2964	2982	3003	3019
		3041	3046	3473										
MTITLE	001000	1038#	1222											
MTSTN	015317	3405	3555#											
MTSTPC	015220	1297	3541#											
MVECX	015267	3088	3549#											
NEXT	001216	1062#	1312*	1380*	1415*	1447*	1470*	1493*	1516*	1539*	1567*	1590*	1613*	1636*
		1659*	1682*	1705*	1728*	1751*	1774*	1797*	1820*	1843*	1872*	1896*	1920*	1944*
		1970*	1996*	2022*	2048*	2074*	2100*	2126*	2152*	2178*	2205*	2234*	2262*	2295*
		2325*	2355*	2385*	2423*	2458*	2540*	2621*	2719*	2819*	2894*	2961*	3000*	3037*
		3145	3441											
NON.EX=	177320	532#	2829	2861	2904	2935								
ODDBIT=	001000	626#	1000											
OUT	014774	3488	3490	3492	3496	3508#								
PARAM =	104405	1120#	1298	3502										
PARAM1	013506	3232#	3253											
PARERR	013562	3235	3237	3239	3248#	3258	3260	3262						
PARTI	013644	3251	3271#											
PASCNT	001230	1067#	1211*	3080*	3099	3122								
PC =%	000007	581#	953*	1245*	1449*	1460*	1472*	1483*	1495*	1506*	1518*	1529*	1541*	1552*
		1569*	1580*	1592*	1603*	1615*	1626*	1638*	1649*	1661*	1672*	1684*	1695*	1707*
		1718*	1730*	1741*	1753*	1764*	1776*	1787*	1799*	1810*	1822*	1833*	1845*	1856*
		1874*	1885*	1898*	1909*	1922*	1933*	1946*	1959*	1972*	1985*	1998*	2011*	2024*
		2037*	2050*	2063*	2076*	2089*	2102*	2115*	2128*	2141*	2154*	2167*	2180*	2193*
		2207*	2224*	2236*	2264*	2297*	2327*	2357*	2387*	2425*	2439*	2463*	2464*	2467*
		2545*	2546*	2549*	2623*	2642*	2643*	2646*	2742*	2743*	2746*	2823*	2824*	2927*
		2898*	2899*	2902*	2965*	2966*	3004*	3005*	3047*	3048*	3107*	3626*	3632*	3638*
		3648*	3656*	3670*										
PFTAB	014652	3470	3476#											
POLY. =	000017	648#												
POPPO	012600	595#	3434											
POP1SP=	005726	593#												
POP2SP=	022626	597#												
PS =	177776	587#	940*	1206*	1281*	1381*	1417*	1453*	1476*	1499*	1522*	1545*	1573*	1596*
		1619*	1642*	1665*	1688*	1711*	1734*	1757*	1780*	1803*	1826*	1849*	1879*	1903*

		1927*	1951*	1977*	2003*	2029*	2055*	2081*	2107*	2133*	2159*	2185*	2210*	2214*
		2239*	2243*	2267*	2271*	2301*	2331*	2361*	2391*	2430*	2461*	2475*	2479*	2543*
		2555*	2559*	2639*	2654*	2658*	2739*	2752*	2756*	2820*	2835*	2839*	2895*	2908*
		2912*	2962*	3001*	3039*									
		594#	3431											
		592#												
		596#												
PUSHRO=	010046	2699	2701#											
PUSH1S=	005746	2469	2501	2517	2518	2625	2648	2680	2696	2697	2968	3754#		
PUSH2S=	024646	3164	3213	3250	3484#	3498*	3508*							
QZX	010702	1460	1483	1506	1529	1552	1580	1603	1626	1649	1672	1695	1718	1741
RBUFF	017166	1764	1787	1810	1833	1856	1885	1909	1933	1959	1985	2011	2037	2063
RDSW	014660	2089	2115	2141	2167	2193	2224	2438	3652#					
RECAT	016074	3425	3428#											
		3455	3461#											
RESREG	014460	3101	3104	3111#										
RESTAR	014576	1124#	3428											
RESTR	012772	1061#	1218*	1305*	1307	1311*	2457*	2539*	2718*	2818*	2893*	2960*	2999*	3035*
RESOS =	104407	3112*	3145*	3146	3441*	3443	3475							
RETURN	001214	1092#	1315*	1318	1323*	1329*	1336*							
		1093#	1316*	1325*	1327*									
RUN	001304	1091#	1213*	1313	1317*									
RUNCNT	001306	632#												
RUNFLG	001302	636#												
RXBA.P=	000000	633#												
RXBA.S=	000004	637#												
RXWC.P=	000001	646#												
RXWC.S=	000005	574#	931*	933	943*	1025*	1030*	1258*	1268*	1271*	1273*	1275	1276	2241*
RX.BCC=	000015	2246	2252*	2269*	2274	2278*	2300*	2308*	2310	2330*	2338*	2340	2360*	2368*
RO	=%000000	2370	2390*	2398*	2400	2629*	2630*	2730*	2731*	3043*	3068*	3135*	3291	3296*
		3308	3322*	3326*	3336	3354*	3432*	3599*	3604*	3608*	3614*			
R1	=%000001	575#	931	932*	933	934	972*	974*	975*	976*	977	979	981*	982*
		983*	984	987*	988*	989	992*	993	996	1002*	1003*	1004*	1005*	1006*
		1008*	1009	1014*	1015	1019*	1026*	1272*	1273	1274*	1275	3103*	3107	3290
R2	=%000002	3297*	3309	3313*	3316	3317	3318	3319	3353*					
		576#	941	942*	945*	946	948*	949*	966*	967*	968	971*	979*	980*
		986*	991*	995*	998*	999*	1000*	1001	1024*	2242*	2244*	2270*	2272*	2498*
		2510*	2579*	2591*	2599*	2677*	2689*	2776*	2788*	2796*	2858*	2870*	2932*	2944*
R3	=%000003	3045#	3289	3298*										
		577#	2493*	2500*	2517*	2574*	2581*	2672*	2679*	2696*	2771*	2778*	2853*	2860*
		2927*	2934*	3044*	3185	3192*	3206*	3209	3218*	3288	3299*	3310	3323*	3324*
R4	=%000004	3325*	3326	3335*	3336*	3341*	3344*	3352*						
		578#	1398*	1399	1431*	2487*	2488*	2489	2494*	2504*	2506	2512*	2513	2518*
		2519	2568*	2569*	2570	2575*	2585*	2587	2593*	2594	2600*	2601	2633*	2634*
		2635	2666*	2667*	2668	2673*	2683*	2685	2691*	2692	2697*	2698	2734*	2735
		2765*	2766*	2767	2772*	2782*	2784	2790*	2791	2797*	2798	2847*	2849*	2849
		2854*	2864*	2866	2872*	2873	2921*	2922*	2923	2928*	2938*	2940	2946*	2947
		2978*	2979*	2986*	2987*	3015*	3016*	3023*	3024*	3062*	3063	3186	3191*	3195*
		3196*	3197	3201	3210	3217*	3224	3233*	3234	3236	3238	3240*	3241	3242
		3248	3266*	3267*	3271*	3287	3300*	3311	3320*	3323	3328*	3330*	3332*	3351*
		3391*	3392*	3393*	3394*	3395*	3396*	3397	3398	3399				
R5	=%000005	579#	1397*	1399	1430*	2484*	2489	2492*	2501*	2506	2511*	2513	2516*	2519
		2565*	2570	2573*	2582*	2587	2592*	2594	2597*	2601	2632*	2635	2663*	2668
		2671*	2680*	2685	2690*	2692	2695*	2698	2733*	2735	2762*	2767	2770*	2779*
		2784	2789*	2791	2794*	2798	2844*	2849	2852*	2861*	2866	2871*	2873	2918*
		2923	2926*	2935*	2940	2945*	2947	2980*	2985*	3017*	3022*	3052*	3053	3063

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DJNDCC.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

14-RT	0100	1112	3153 #	
RT-1	0100	1113	1206 #	1218
RT-2	0100	1114	3154 #	
RT-3	0100	1115	3155 #	
RT-4	0100	1116	3156 #	
RT-5	0100	1117	3157 #	
RT-6	0100	1118	3158 #	
RT-7	0100	1119	3159 #	
RT-8	0100	1120	3160 #	
RT-9	0100	1121	3161 #	

K07

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DZDQCC.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

.WORD 921 3484

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

*.DZDQCC.SEQ/SOL/CRF/PAGNUM/NL:TOC-UNIV.P11,DZDQCC.P11
RUN-TIME: 29 41 6 SECONDS
RUN-TIME RATIO: 140/78=1.7
CORE USED: 24K (47 PAGES)

