

# DL11-W

DIAGNOSTIC  
MD-11-DZDLD-A

EP-DZDLD-A-DL-A  
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This section of the document contains a grid of 100 small diagnostic charts or tables, arranged in 10 rows and 10 columns. Each cell contains technical data, likely related to the MD-11 aircraft diagnostic system. The data is organized into columns and rows, with some cells containing text and others containing numerical or graphical information. The overall layout is a structured grid of diagnostic information.

IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDLD-A  
PRODUCT NAME: DL11-M DIAGNOSTIC  
DATE CREATED: JUNE 11, 1976  
MAINTAINER: DIAGNOSTIC ENGINEERING (CC301)  
AUTHOR: DAN CASALETTO

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## 1.0 GENERAL INFORMATION

### 1.1 ABSTRACT

THIS DIAGNOSTIC IS A LOGIC TEST TO VERIFY THE OPERATION OF THE DL11-W SERIAL LINE/ REAL TIME CLOCK INTERFACE. THE PROGRAM WILL RUN WITHOUT ANY SPECIAL TEST FIXTURES BY DEFAULT. HOWEVER, A WRAP CABLE CAN BE USED AND TESTED BY OPTIO (BIT7 OF SWR).

THIS TEST OPERATES ON THE CONSOLE DL11-W SERIAL LINE AND CLOCK INTERFACES AS WELL AS UP TO FIFTEEN(15) ADDITIONAL DL11-W SERIAL LINE INTERFACES. THE DEFAULT ADDRESSES ARE:

A. CONSOLE - 177560 SERIAL LINE  
177546 CLOCK

B. OTHER SERIAL LINE - 776500 FIRST SERIAL LINE ADDRESS  
OF 15 CONSECUTIVE SERIAL  
LINE ADDRESSES

THIS PROGRAM IS DESIGNED TO RUN ON ANY PDP-11 WITH 8K OF MEMORY AND A DL11-W MODULE. IT CAN BE RUN UNDER XXDP APT, AND ACT MONITORS, AND ON PROCESSORS WITH NO HARDWARE SWITCH REGISTER, SOFTWARE SWITCH REGISTER = LOCATION 176

POWER FAILURE IS SUPPORTED FOR SYSTEMS WITH CORE MEMORY.

### 1.2 SYSTEM REQUIREMENTS

#### 1.2.1 EQUIPMENT

STANDARD 11 FAMILY COMPUTER WITH A CONSOLE OUTPUT DEVICE AND 8K OF MEMORY.

#### 1.2.2 STORAGE

THE PROGRAM USES MEMORY FROM 0000 TO 21510.

1.3 ASSUMPTIONS

- A. IF THE UNIT UNDER TEST (UUT) IS THE CONSOLE, THE PROGRAM WILL ASSUME THE REAL TIME CLOCK (RTC) IS ENABLED AND WILL TEST IT UNLESS THE TESTS ARE DISABLED BY BITS OF THE SMR.
- B. IF THE UUT IS NOT THE CONSOLE, THE RTC IS NOT TESTED FOR THAT DEVICE.
- C. THE PROGRAM WILL ASSUME THE ERROR FLAG BITS AND THE BREAK FUNCTION OF THE DL11-M ARE DISABLED AND WILL NOT TEST THESE FUNCTIONS UNLESS ENABLED BY BIT10 (FOR ERROR FLAGS) AND BIT8 (FOR BREAK) OF THE SMR.

2.0 OPERATING INSTRUCTIONS2.1 LOADING PROCEDURE

USE STANDARD PROCEDURE FOR PDP-11 ABSOLUTE BINARY FORMATTED TAPES.

2.2 STARTING PROCEDURE

LOAD THE SWITCH REGISTER WITH SETTING  
(SOFTWARE SWITCH REGISTER LOCATION = 176)

- A. START AT 200.  
AFTER CHECKING THE TRANSMITTER, THE PROGRAM WILL PRINT ITS IDENTIFICATION AND REPORT THE NUMBER OF DEVICES UNDER TEST (NUMBER IS OCTAL). "END PASS" IS PRINTED AFTER A FULL PASS HAS BEEN MADE ON ALL DEVICES UNDER TEST.
- B. START AT 204.  
THE "ECHO" TEST WILL BE EXECUTED. AN "\*" IS PRINTED AT THE BEGINNING OF THE TEST. THE ECHO TEST READS A CHARACTER FROM THE TERMINAL, WRITES THAT CHARACTER TO THE TERMINAL AND REPORTS ANY ERROR FLAGS SET IN THE RECEIVER BUFFER. A CONTROL-C HALTS THE TEST AND PRINTS "STOP" AT THE TERMINAL. CONTINUING RESTARTS THE ECHO TEST.
- C. START AT 210.  
THE TERMINAL OUTPUT TEST WILL BE EXECUTED. DEPRESSING ANY CHARACTER AT THE TERMINAL HALTS THE TEST. CONTINUING RESTARTS THE TEST. THE TEST OUTPUTS 32 CHARACTERS ON A LINE AND REPEATS THE PATTERN EVERY THREE LINES. THE PATTERN IS AS FOLLOWS (OCTAL CODE 040 --> 377):

!"#\$%&'()*+,-./0123456789:;<=>?	(OCTAL CODE)
abcdefghijklmnopqrstuvwxyz[\]^_`	(040 --> 077)
abcdefghijklmnopqrstuvwxyz{	(100 --> 137)
abcdefghijklmnopqrstuvwxyz{	(140 --> 177) [LOWER CASE ALPHA]

THIS BOTTOM LINE COULD BE THE FOLLOWING IF THE TERMINAL DOES NOT HAVE LOWER CASE:

E01

ABCDEFGHIJKLMNOPQRSTUVWXYZ[\

[UPPER CASE ALPHA]

SEQ 0004

## 2.3 OPERATING PROCEDURE

SEQ 0005

## 2.3.1 OPERATIONAL SWITCH SETTINGS

NOTE: IF NO HARDWARE SWITCH REGISTER IS AVAILABLE THE PROGRAM WILL AUTOMATICALLY USE THE CONTENTS OF LOCATION 176 AS THE SOFTWARE SWITCH REGISTER. THE USER SHOULD SET THIS LOCATION BEFORE STARTING THE PROGRAM. IF A HARDWARE SWITCH IS AVAILABLE AND A SOFTWARE SMR IS DESIRED, PUT ALL SWITCHES UP.

BIT15	- HALT ON ERROR
BIT14	- SCOPE LOOP
BIT13	- INHIBIT ERROR TIMEOUT
BIT12	- UNUSED
BIT11	- UNUSED
BIT10	- ENABLE ERROR FLAGS TESTS
BIT09	- LOOP ON ERROR
BIT08	- ENABLE BREAK FUNCTION TESTS
BIT07	- ENABLE DATA TEST WITH WRAP CABLE
BIT06	- INHIBIT RTC TESTS
BIT05	- ALLOW MANUAL SETTING OF "SDEVH" (DEVICE MAP)

BUILT INTO THE PROGRAM IS THE ABILITY TO DYNAMICALLY CHANGE THE CONTENTS OF SMREG DURING PROGRAM EXECUTION. BY STRIKING 1G (CNTRL G) ON CONSOLE TTY THE OPERATOR SETS A REQUEST FLAG TO CHANGE THE CONTENTS OF SMREG, WHICH IS PROCESSED IN KEY AREAS OF THE PROGRAM CODE (IE) ERROR ROUTINES, AFTER HALTS END OF PASS, AND OTHER APPLICABLE AREAS. BECAUSE THIS DIAGNOSTIC USES THE MAINTENANCE BIT OF THE SERIAL LINE, THE CONTROL-G SHOULD BE ISSUED DURING PROGRAM TIMEOUTS AT THAT TIME THE MAINTENANCE BIT IS SURE TO BE CLEAR.

IF A CONTROL-G IS DETECTED, UPON EXECUTION THE CONTENTS OF THE SMREG ARE DUMPED IN OCTAL ON THE CONSOLE TTY AND ANY CHANGES ARE REQUESTED

(IE) SMR=XXXXXX NEW=

POSSIBLE RESPONSES ARE:

1. <CR> IF NO CHANGES ARE TO BE MADE
2. 6 DIGITS 0-7 TO REPRESENT IN OCTAL THE NEW SWITCH REGISTER VALUE ;LAST DIGIT FOLLOWED BY <CR>.
3. 1U TO ALLOW REENTERING VALUE IF ERROR IS COMMITTED KEYING IN SMREG VALUE.

**2.3.2 RUNNING UNDER APT**

THE APT MAILBOX IS LOCATED AT LOCATION 500, TO ALLOW ADDITIONAL SERIAL LINE VECTOR ASSIGNMENTS TO THE 400 AREA OF MEMORY.

THE EXECUTION TIMES PROVIDED ARE FOR EXECUTION WITH AN 11/34 PROCESSOR, CORE MEMORY, AND 110 BAUD.

**2.3.3 RUN WITH ALTERNATE CONSOLE ADDRESS**

TO USE A CONSOLE ADDRESS OTHER THAN 177560, OR VECTOR OTHER THAN 60, THE OPERATOR MUST SUPPLY THE PROGRAM WITH THE CORRECT ADDRESSES BY INSERTING THEM AT THE TAG LABELED "CPCSR":

CPCSR: ADDRESS OF RECEIVER RCSR  
 CRBUF: ADDRESS OF RECEIVER BUFFER  
 CTCSS: ADDRESS OF TRANSMITTER CSR  
 CTBUF: ADDRESS OF TRANSMITTER BUFFER  
 CRVCT: ADDRESS OF RECEIVER VECTOR  
 CRPSW: ADDRESS OF ASSOCIATED PSW  
 CTVCT: ADDRESS OF TRANSMITTER VECTOR  
 CTPSW: ADDRESS OF ASSOCIATED PSW

**2.3.4 TESTING ADDITIONAL SERIAL LINES**

THIS PROGRAM WILL SUPPORT TESTING OF MULTIPLE SLU'S. IT REQUIRES THE ADDRESS OF THE FIRST ADDITIONAL RCSR (STORED AT "SBASE") AND ITS INTERRUPT VECTOR (STORED AT "SVECT1"); AND WILL BE ABLE TO ADDRESS ANY SLU STARTING AT THE SPECIFIED BASE ADDRESS UP TO 15 CONSECUTIVE DEVICES.

EXAMPLE: SBASE: 776500  
 SVECT1: 300

THE PROGRAM WILL BE ABLE TO TEST THE CONSOLE PLUS ANY ADDITIONAL DL11-W SLU'S WITHIN THE RANGE 776500 --> 776660

SBASE AND SVECT1 DEFAULT TO 776500 AND 300 RESPECTIVELY.

THE PROGRAM ASSOCIATES UNIT NUMBERS TO DEVICES AS FOLLOWS:  
(NUMBERS IN PARENTHESIS ARE OCTAL)

UNIT# 0 --> CONSOLE (ADDRESS STORED AT "CCSR")  
 UNIT# 1 --> BASE ADDRESS STORED AT "SBASE"  
 ASSOCIATED BASE VECTOR STORED AT "SVECT1"  
 UNIT# 2 --> BASE ADDRESS + (10)  
 BASE VECTOR + (10)  
 UNIT# 3 --> BASE ADDRESS + (20)  
 BASE VECTOR + (20)  
 UNIT# 4 --> BASE ADDRESS + (30)  
 BASE VECTOR + (30)

↓  
 UNIT#15 --> BASE ADDRESS + (160)  
 BASE VECTOR + (160)

STARTING AT LOCATION 200 AND HAVING BITS OF SWR CLEAR, THE PROGRAM WILL SELF  
 SIZE THE NUMBER OF DEVICES (STARTING AT THE BAS ADDRESS) AND  
 STORE A BIT MAP AT "SDEVH" (DEVICE MAP) TO INDICATE WHICH UNIT NUMBERS  
 ARE PRESENT AND WILL BE TESTED:

```

-----
| UNIT | UNIT | ..... | UNIT | UNIT | CONSOLE |
| 15  | 14  | ..... | 2   | 1   |          |
-----
    
```

A BIT MAP CAN BE ENTERED AT "SDEVH" PRIOR TO STARTING THE PROGRAM  
 SETTING BITS OF THE SWR INHIBITS THE SELF-SIZING AND DEVICE MAP  
 GENERATION, AND USES THE VALUE STORED BY THE OPERATOR.

EXAMPLE:

SWR = 000040            (BINARY 0 000 000 000 100 000)  
 SBASE: 776500  
 SVECT1: 300

SDEVH: 13            (BINARY - 0 000 000 000 001 011)

THE PROGRAM WILL TEST -  
 UNIT# 0 = CONSOLE  
 UNIT# 1 = 776500 ; 300  
 UNIT# 3 = 776520 ; 320

2.4 EXECUTION TIMES - (110 BAUD)

LONGEST SUBTEST TIME = 50 SECONDS  
 PASS TIME = 60 SECONDS  
 ADDITIONAL DEVICES = 55 SECONDS/DEVICE

3.0 ERROR REPORTING

IF A ROUTINE FAILS AND THE INHIBIT ERROR TYPEOUT (BIT13) OF THE SMR IS NOT SET, A PRINTOUT RESULTS IN THE FORM:

```
"(SOME ASCII MESSAGE)"
TEST#  ERR PC  RCSR  [ANY APPLICABLE DAT HEADINGS]
XXXXXX XXXXXX XXXXXX [ANY APPLICABLE DATA]
```

NOTE: "RCSR" IS DEPENDENT ON THE FAILURE  
 & THEREFORE COULD BE TCSR, RBUF, TBUF, OR LKS

WHERE "XXXXXX" IS AN OCTAL NUMBER.  
 THIS ERROR PRINTOUT OCCURS PROVIDED THE ERROR THAT EXISTS  
 WOULD NOT HINDER THE TYPEOUT. IN CASES WHERE IT IS NOT POSSIBLE  
 TO PRINT AN ERROR MESSAGE (I.E. FATAL CONSOLE TRANSMITTER  
 FAILURES), A HALT OCCURS AND THE PC CAN BE EXAMINED BY THE OPERATOR  
 TO FIND THE ERROR INFORMATION IN THE PROGRAM LISTING.

NOTE: FOR SOFTWARE SWITCH OPERATION, THE SWITCH REGISTER CAN  
 BE CHANGED BY TYPING A CONTROL-G AT THE CONSOLE DURING ERROR PRINTOUTS.  
 AFTER CONTINUING FROM THE ERROR HALT THE OLD SMR CONTENTS  
 IS DISPLAYED AND THE NEW CONTENTS CAN BE ENTERED.  
 IF ERROR HALTS ARE DISABLED, THE CONTROL-G RESPONSE OCCURS  
 IMMEDIATELY FOLLOWING THE TYPEOUT.

**4.0** SUBROUTINE ABSTRACTS**4.1** TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A BREAK POINT TRAP (000003). THUS AN ILLEGAL TRAP OR INTERRUPT CAUSES A TRAP THROUGH THE BPT VECTOR(14) WHICH POINTS TO THE "CATCH" ROUTINE.

THE "CATCH" ROUTINE REPORTS THE PC THAT CAUSED THE ORIGINAL TRAP AND THE LOCATION OF THE TRAP VECTOR (IF UNDER APT, AN ERROR IS INDICATED TO APT). AFTER REPORTING THE ERROR THE PROGRAM HALTS. THE PROGRAM MUST BE RESTARTED AT THIS POINT.

**4.2** WRPSM

THIS ROUTINE IS USED TO WRITE THE PSM BY POPPING VALUES FROM THE STACK. THIS METHOD IS USED TO BE COMPATIBLE WITH ALL 11 FAMILY PROCESSORS.

**4.3** SCOPE

THIS ROUTINE CALL IS PLACED BETWEEN EACH SUBTEST. IT RECORDS THE STARTING ADDRESS OF EACH SUBTEST AS IT IS BEING ENTERED AND UPDATES THE TEST NUMBER. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST AT WHICH THE SCOPE LOOP IS REQUESTED.

4.4 ERROR

THIS ROUTINE CALL IS PLACED WHEREEVER AN ERROR REPORT IS DESIRED. THE LOWER BYTE OF THIS CALL IS USED AS THE ERROR NUMBER AND AS A POINTER INTO THE ERROR TABLE. THIS ROUTINE REPORTS ERRORS TO APT USING "SAPTYPE" AND TYPES ERROR REPORTS TO THE CONSOLE USING "SERRTYPE".

4.5 SPWER

THIS ROUTINE SAVES ALL GENERAL REGISTERS DURING POWER-DOWN AND RESTORES THEM AT POWER-UP. IF A POWER FAILURE OCCURS "POWER" IS PRINTED AT THE CONSOLE AFTER POWER IS RESTORED.

4.6 CKSMR

THIS ROUTINE CALL IS USED TO DETECT THE RECEPTION OF A CONTROL-G FROM THE CONSOLE. THE CALL USES "SREAD" TO PERFORM THE CONTROL-G SEQUENCE OF DISPLAYING THE CONTENTS OF THE SOFTWARE SWITCH REGISTER AND THE ENTERING THE NEW CONTENTS FROM THE TERMINAL.

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.ENABLE ABS  
.LIST ME  
.NLIST MC,MD,CND

.MCALL .STYPE, .STYPC, .STRAP  
.MCALL .SETUP, .STARS, .PUSH, .POP, .SETUP, .EQUAT, .SERRTYP  
.MCALL .SAPTHR, .SAPTBL, .SACT11, .SSCOPE  
.MCALL .SCHTAG, .SEOP, .SREAD  
.SBTTL BASIC DEFINITIONS

001100

:#INITIAL ADDRESS OF THE STACK POINTER \*\*\* 1100 \*\*\*  
STACK= 1100  
.EQUIV EMT,ERROR ;;BASIC DEFINITION OF ERROR CALL  
.EQUIV IOT,SCOPE ;;BASIC DEFINITION OF SCOPE CALL

000011  
000012  
000015  
000200  
177776

:#MISCELLANEOUS DEFINITIONS  
HT= 11 ;;CODE FOR HORIZONTAL TAB  
LF= 12 ;;CODE FOR LINE FEED  
CR= 15 ;;CODE FOR CARRIAGE RETURN  
CRLF= 200 ;;CODE FOR CARRIAGE RETURN-LINE FEED  
PS= 177776 ;;PROCESSOR STATUS WORD  
.EQUIV PS,PSW

177774  
177772  
177570  
177570

STKLMT= 177774 ;;STACK LIMIT REGISTER  
PIRQ= 177772 ;;PROGRAM INTERRUPT REQUEST REGISTER  
DSMR= 177570 ;;HARDWARE SWITCH REGISTER  
DDISP= 177570 ;;HARDWARE DISPLAY REGISTER

000000  
000001  
000002  
000003  
000004  
000005  
000006  
000007

:#GENERAL PURPOSE REGISTER DEFINITIONS  
R0= %0 ;;GENERAL REGISTER  
R1= %1 ;;GENERAL REGISTER  
R2= %2 ;;GENERAL REGISTER  
R3= %3 ;;GENERAL REGISTER  
R4= %4 ;;GENERAL REGISTER  
R5= %5 ;;GENERAL REGISTER  
R6= %6 ;;GENERAL REGISTER  
R7= %7 ;;GENERAL REGISTER  
.EQUIV R6,SP ;;STACK POINTER  
.EQUIV R7,PC ;;PROGRAM COUNTER

000000  
000040  
000100  
000140  
000300  
000240  
000300  
000340

:#PRIORITY LEVEL DEFINITIONS  
PR0= 0 ;;PRIORITY LEVEL 0  
PR1= 40 ;;PRIORITY LEVEL 1  
PR2= 100 ;;PRIORITY LEVEL 2  
PR3= 140 ;;PRIORITY LEVEL 3  
PR4= 200 ;;PRIORITY LEVEL 4  
PR5= 240 ;;PRIORITY LEVEL 5  
PR6= 300 ;;PRIORITY LEVEL 6  
PR7= 340 ;;PRIORITY LEVEL 7

100000  
040000  
020000

:#"SWITCH REGISTER" SWITCH DEFINITIONS  
SW15= 100000  
SW14= 40000  
SW13= 20000

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000400  
000200  
000100  
000040  
000020  
000010  
000004  
000002  
000001

100000  
040000  
020000  
010000  
004000  
002000  
001000  
000400  
000200  
000100  
000040  
000020  
000010  
000004  
000002  
000001

SW12= 10000  
SW11= 4000  
SW10= 2000  
SW09= 1000  
SW08= 400  
SW07= 200  
SW06= 100  
SW05= 40  
SW04= 20  
SW03= 10  
SW02= 4  
SW01= 2  
SW00= 1  
.EQUIV SW09, SW9  
.EQUIV SW08, SW8  
.EQUIV SW07, SW7  
.EQUIV SW06, SW6  
.EQUIV SW05, SW5  
.EQUIV SW04, SW4  
.EQUIV SW03, SW3  
.EQUIV SW02, SW2  
.EQUIV SW01, SW1  
.EQUIV SW00, SW0

:#DATA BIT DEFINITIONS (BIT00 TO BIT15)

BIT15= 100000  
BIT14= 40000  
BIT13= 20000  
BIT12= 10000  
BIT11= 4000  
BIT10= 2000  
BIT09= 1000  
BIT08= 400  
BIT07= 200  
BIT06= 100  
BIT05= 40  
BIT04= 20  
BIT03= 10  
BIT02= 4  
BIT01= 2  
BIT00= 1  
.EQUIV BIT09, BIT9  
.EQUIV BIT08, BIT8  
.EQUIV BIT07, BIT7  
.EQUIV BIT06, BIT6  
.EQUIV BIT05, BIT5  
.EQUIV BIT04, BIT4  
.EQUIV BIT03, BIT3  
.EQUIV BIT02, BIT2  
.EQUIV BIT01, BIT1  
.EQUIV BIT00, BIT0

:#BASIC "CPU" TRAP VECTOR ADDRESSES

ERRVEC= 4  
RESVEC= 10  
TBITVEC=14  
::: TIME OUT AND OTHER ERRORS  
::: RESERVED AND ILLEGAL INSTRUCTIONS  
::: "T" BIT



```

154
155          000500
156          .SBTTL      =      500
157          .SBTTL      ACT11 HOOKS
158          ;;*****
159          ;HOOKS REQUIRED BY ACT11
160          $SVPC=      ;SAVE PC
161          =46
162          000046      SENDAD      ;;1)SET LOC.46 TO ADDRESS OF SENDAD IN .SEOP
163          011500
164          000052      =52
165          000000      .WORD      0      ;;2)SET LOC.52 TO ZERO
166          000500      =$SVPC      ;; RESTORE PC
167          .SBTTL      APT PARAMETER BLOCK
168          ;;*****
169          ;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
170          ;;*****
171          000500      .SX=      ;;SAVE CURRENT LOCATION
172          000024      =24      ;;SET POWER FAIL TO POINT TO START OF PROGRAM
173          000024      200      ;;FOR APT START UP
174          000044      =44      ;;POINT TO APT INDIRECT ADDRESS PNTR.
175          000044      $APTHDR    ;;POINT TO APT HEADER BLOCK
176          000500      =.SX      ;;RESET LOCATION COUNTER
177          ;;*****
178          ;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
179          ;INTERFACE SPEC.
180
181          $APTHD:
182          $HIBTS: .WORD      0      ;; TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
183          $MBAOR: .WORD      $MAIL   ;; ADDRESS OF APT MAILBOX (BITS 0-15)
184          $TSTM:  .WORD      50      ;; RUN TIM OF LONGEST TEST
185          $PASTM: .WORD      60      ;; RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
186          $UNITH: .WORD      55      ;; ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
187          .WORD      $ETEND-$MAIL/2 ;; LENGTH MAILBOX-ETABLE(WORDS)
188

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.SBTTL COMMON TAGS

\*\*\*\*\*  
: THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS  
: USED IN THE PROGRAM.

001000 001000  
001000 000000  
001002 000  
001003 000  
001004 000030  
001006 000000  
001010 000000  
001012 000000  
001014 000  
001015 001  
001016 000000  
001020 000000  
001022 000000  
001024 000000  
001026 000000  
001030 000000  
001032 000000  
001034 000  
001035 000  
001036 000000  
001040 177570  
001042 177570  
001044 177560  
001046 177562  
001050 177564  
001052 177566  
001054 000  
001055 002  
001056 012  
001057 000  
001060 000000  
001062 077  
001063 015  
001064 000012

SCHTAG: .=1000  
: .WORD 0  
\$TSTNM: .BYTE 000  
SERFLG: .BYTE 0000  
\$ICNT: .WORD 0000  
\$LPAOR: .WORD 0000  
\$LPERR: .WORD 0000  
\$ERTTL: .WORD 0000  
\$ITEMB: .BYTE 001  
\$ERMAX: .BYTE 1  
\$ERAPC: .WORD 0000  
\$GDAOR: .WORD 0000  
\$BDADR: .WORD 0000  
\$GDDAT: .WORD 0000  
\$BDDAT: .WORD 0000  
: .WORD 0000  
\$AUTOB: .BYTE 000  
\$INTAG: .BYTE 000  
: .WORD 0  
\$MR: .WORD D\$MR  
\$DISPLAY: .WORD DDISP  
\$TKS: 177560  
\$TKB: 177562  
\$TPS: 177564  
\$TPB: 177566  
\$NULL: .BYTE 0  
\$FILLS: .BYTE 2  
\$FILLC: .BYTE 12  
\$TFPLG: .BYTE 0  
\$ESCAPE: 0  
\$QUES: .ASCII /?/  
\$CRLF: .ASCII <15>  
\$LF: .ASCIZ <12>

:: START OF COMMON TAGS  
: CONTAINS THE TEST NUMBER  
: CONTAINS ERROR FLAG  
: CONTAINS SUBTEST ITERATION COUNT  
: CONTAINS SCOPE LOOP ADDRESS  
: CONTAINS SCOPE RETURN FOR ERRORS  
: CONTAINS TOTAL ERRORS DETECTED  
: CONTAINS ITEM CONTROL BYTE  
: CONTAINS MAX. ERRORS PER TEST  
: CONTAINS PC OF LAST ERROR INSTRUCTION  
: CONTAINS ADDRESS OF 'GOOD' DATA  
: CONTAINS ADDRESS OF 'BAD' DATA  
: CONTAINS 'GOOD' DATA  
: CONTAINS 'BAD' DATA  
: RESERVED--NOT TO BE USED  
: AUTOMATIC MODE INDICATOR  
: INTERRUPT MODE INDICATOR  
: ADDRESS OF SWITCH REGISTER  
: ADDRESS OF DISPLAY REGISTER  
: TTY KBD STATUS  
: TTY KBD BUFFER  
: TTY PRINTER STATUS REG. ADDRESS  
: TTY PRINTER BUFFER REG. ADDRESS  
: CONTAINS NULL CHARACTER FOR FILLS  
: CONTAINS # OF FILLER CHARACTERS REQUIRED  
: INSERT FILL CHARS. AFTER A "LINE FEED"  
: "TERMINAL AVAILABLE" FLAG (BIT<07>=0=YES)  
: ESCAPE ON ERROR ADDRESS  
: QUESTION MARK  
: CARRIAGE RETURN  
: LINE FEED

.SBTTL APT MAILBOX-ETABLE

\*\*\*\*\*

001066  
001066 000000  
001070 000000  
001072 000000  
001074 000000  
001076 000000  
001100 000000  
001102 000000  
001104 000000  
001106

APT MAILBOX  
\$MAIL: .WORD  
\$MSGTY: .WORD AMSGTY  
\$FATAL: .WORD AFATAL  
\$TESTN: .WORD ATESTN  
\$PASS: .WORD APASS  
\$DEVCT: .WORD ADEVCT  
\$UNIT: .WORD AUNIT  
\$MSGAD: .WORD AMSGAD  
\$MSGLG: .WORD AMSLG  
\$ETABLE: .WORD  
: MESSAGE TYPE CODE  
: FATAL ERROR NUMBER  
: TEST NUMBER  
: PASS COUNT  
: DEVICE COUNT  
: I/O UNIT NUMBER  
: MESSAGE ADDRESS  
: MESSAGE LENGTH  
: APT ENVIRONMENT TABLE

001106	000	SENV:	.BYTE	AENV	:: ENVIRONMENT BYTE
001107	000	SENVH:	.BYTE	AENVH	:: ENVIRONMENT MODE BITS
001110	000000	SSWREG:	.WORD	ASWREG	:: APT SWITCH REGISTER
001112	000000	SUSWR:	.WORD	AUSWR	:: USER SWITCHES
001114	000000	SCPUOP:	.WORD	ACPUOP	:: CPU TYPE, OPTIONS
		***			BITS 15-11=CPU TYPE
		***			11/04=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05
		***			11/70=06, P00=07, Q=10
		***			BIT 10=REAL TIME CLOCK
		***			BIT 9=FLOATING POINT PROCESSOR
		***			BIT 8=MEMORY MANAGEMENT
001116	000	SMAMS1:	.BYTE	AMAMS1	:: HIGH ADDRESS M.S. BYTE
001117	000	SMTYP1:	.BYTE	AMTYP1	:: MEM. TYPE, BLK#1
		***			MEM. TYPE BYTE -- (HIGH BYTE)
		***			900 NSEC CORE=001
		***			300 NSEC BIPOLAR=002
		***			500 NSEC MOS=003
001120	000000	SMADR1:	.WORD	AMADR1	:: HIGH ADDRESS, BLK#1
		***			MEM. LAST ADDR.=3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE
001122	000	SMAMS2:	.BYTE	AMAMS2	:: HIGH ADDRESS M.S. BYTE
001123	000	SMTYP2:	.BYTE	AMTYP2	:: MEM. TYPE, BLK#2
001124	000000	SMADR2:	.WORD	AMADR2	:: MEM. LAST ADDRESS, BLK#2
001126	000	SMAMS3:	.BYTE	AMAMS3	:: HIGH ADDRESS M.S. BYTE
001127	000	SMTYP3:	.BYTE	AMTYP3	:: MEM. TYPE, BLK#3
001130	000000	SMADR3:	.WORD	AMADR3	:: MEM. LAST ADDRESS, BLK#3
001132	000	SMAMS4:	.BYTE	AMAMS4	:: HIGH ADDRESS M.S. BYTE
001133	000	SMTYP4:	.BYTE	AMTYP4	:: MEM. TYPE, BLK#4
001134	000000	SMADR4:	.WORD	AMADR4	:: MEM. LAST ADDRESS, BLK#4
001136	000300	SVECT1:	.WORD	AVECT1	:: INTERRUPT VECTOR#1, BUS PRIORITY#1
001140	000000	SVECT2:	.WORD	AVECT2	:: INTERRUPT VECTOR#2, BUS PRIORITY#2
001142	176500	SBASE:	.WORD	ABASE	:: BASE ADDRESS OF EQUIPMENT UNDER TEST
001144	000000	SDEVH:	.WORD	ADEVH	:: DEVICE MAP
001146		SETEND:			
		.MEXIT			

.SBTTL ERROR POINTER TABLE

;#THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.  
 ;#THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN  
 ;#LOCATION SITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.  
 ;#NOTE1: IF SITEMB IS 0 THE ONLY PERTINENT DATA IS (SERRPC).  
 ;#NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;# EM ;:POINTS TO THE ERROR MESSAGE  
 ;# DH ;:POINTS TO THE DATA HEADER  
 ;# DT ;:POINTS TO THE DATA  
 ;# DF ;:POINTS TO THE DATA FORMAT

SERRTB:

.SERRTB:

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001146  
 001146 014614  
 001146 020575  
 001150 021340  
 001152 000000  
 001154  
 001156 014640  
 001160 020622  
 001162 021350  
 001164 000000  
 001166 014664  
 001170 020575  
 001172 021340  
 001174 000000  
 001176 014731  
 001200 020575  
 001202 021340  
 001204 000000  
 001206 014753  
 001210 020575  
 001212 021340  
 001214 000000  
 001216 015010  
 001220 020647  
 001222 021360  
 001224 000000  
 001226 015034  
 001230 020674  
 001232 021370  
 001234 000000  
 001236 015060  
 001240 020721  
 001242 021400  
 001244 000000

EM1  
 DH1  
 DT1  
 0  
 EM2  
 DH2  
 DT2  
 0  
 EM3  
 DH1  
 DT1  
 0  
 EM4  
 DH1  
 DT1  
 0  
 EM5  
 DH1  
 DT1  
 0  
 EM6  
 DH6  
 DT6  
 0  
 EM7  
 DH7  
 DT7  
 0  
 EM10  
 DH10  
 DT10  
 0

;"CAN NOT ACCESS TCSR"  
 ;"TEST# ERR PC TCSR"  
 ;STESTN,SERRPC,TCSR  
 ;"CAN NOT ACCESS TBUF"  
 ;"TEST# ERR PC TBUF"  
 ;STESTN,SERRPC,TBUF  
 ;"TCSR DONE NOT CLEARED WITH TBUF FULL"  
 ;"TEST# ERR PC TCSR"  
 ;STESTN,SERRPC,TCSR  
 ;"TCSR DONE NOT SET"  
 ;"TEST# ERR PC TCSR"  
 ;STESTN,SERRPC,TCSR  
 ;TCSR DONE NOT SET WITH RESET  
 ;"TEST# ERR PC TCSR"  
 ;STESTN,SERRPC,TCSR  
 ;"CAN NOT ACCESS RCSR"  
 ;"TEST# ERR PC RCSR"  
 ;STESTN,SERRPC,RCSR  
 ;"CAN NOT ACCESS RBUF"  
 ;"TEST# ERR PC RBUF"  
 ;STESTN,SERRPC,RBUF  
 ;"CAN NOT ACCESS LKS"  
 ;"TEST# ERR PC LKS"  
 ;STESTN,SERRPC,LKS

335					
336	001246	015103	EM11	;	"BIT0 OF TCSR NOT CLEAR AFTER RESET"
337	001250	020575	DH1	;	"TEST# ERR PC TCSR"
338	001252	021340	DT1	;	STESTN,SERRPC,TCSR
339	001254	000000	0		
340					
341	001256	015146	EM12	;	"CAN NOT SET BIT0 OF TCSR"
342	001260	020575	DH1	;	"TEST# ERR PC TCSR"
343	001262	021340	DT1	;	STESTN,SERRPC,TCSR
344	001264	000000	0		
345					
346	001266	015177	EM13	;	"CAN NOT CLEAR BIT0 OF TCSR"
347	001270	020575	DH1	;	"TEST# ERR PC TCSR"
348	001272	021340	DT1	;	STESTN,SERRPC,TCSR
349	001274	000000	0		
350					
351	001276	015232	EM14	;	"RESET DID NOT CLEAR BIT0 OF TCSR"
352	001300	020575	DH1	;	"TEST# ERR PC TCSR"
353	001302	021340	DT1	;	STESTN,SERRPC,TCSR
354	001304	000000	0		
355					
356	001306	015273	EM15	;	"BIT2 OF TCSR NOT CLEAR AFTER RESET"
357	001310	020575	DH1	;	"TEST# ERR PC TCSR"
358	001312	021340	DT1	;	STESTN,SERRPC,TCSR
359	001314	000000	0		
360					
361	001316	015336	EM16	;	"CAN NOT SET BIT2 OF TCSR"
362	001320	020575	DH1	;	"TEST# ERR PC TCSR"
363	001322	021340	DT1	;	STESTN,SERRPC,TCSR
364	001324	000000	0		
365					
366	001326	015367	EM17	;	"CAN NOT CLEAR BIT2 OF TCSR"
367	001330	020575	DH1	;	"TEST# ERR PC TCSR"
368	001332	021340	DT1	;	STESTN,SERRPC,TCSR
369	001334	000000	0		
370					
371	001336	015422	EM20	;	"RESET DID NOT CLEAR BIT2 OF TCSR"
372	001340	020575	DH1	;	"TEST# ERR PC TCSR"
373	001342	021340	DT1	;	STESTN,SERRPC,TCSR
374	001344	000000	0		
375					
376	001346	015463	EM21	;	"BIT6 OF TCSR NOT CLEAR AFTER RESET2"
377	001350	020575	DH1	;	"TEST# ERR PC TCSR"
378	001352	021340	DT1	;	STESTN,SERRPC,TCSR
379	001354	000000	0		
380					
381	001356	015527	EM22	;	"XMIT INTERRUPT WITH PRIORITY 7"
382	001360	020575	DH1	;	"TEST# ERR PC TCSR"
383	001362	021340	DT1	;	STESTN,SERRPC,TCSR
384	001364	000000	0		
385					
386	001366	015564	EM23	;	"CAN NOT SET BIT6 OF TCSR"
387	001370	020575	DH1	;	"TEST# ERR PC TCSR"
388	001372	021340	DT1	;	STESTN,SERRPC,TCSR
389	001374	000000	0		
390					

391	001376	015615	EM24	;"CAN NOT CLEAR BIT6 OF TCSR"
392	001400	020575	DH1	;"TEST# ERR PC TCSR"
393	001402	021340	DT1	;"STESTN,SERRPC,TCSR"
394	001404	000000	0	
396	001406	015650	EM25	;"RESET DID NOT CLEAR BIT6 OF TCSR"
397	001410	020575	DH1	;"TEST# ERR PC TCSR"
398	001412	021340	DT1	;"STESTN,SERRPC,TCSR"
399	001414	000000	0	
400				
401	001416	015711	EM26	;"BIT6 OF RCSR NOT CLEAR AFTER RESET"
402	001420	020647	DH6	;"TEST# ERR PC RCSR"
403	001422	021360	DT6	;"STESTN,SERRPC,RCSR"
404	001424	000000	0	
405				
406	001426	015754	EM27	;"RCVR INTERRUPT WITH PRIORITY 7"
407	001430	020647	DH6	;"TEST# ERR PC RCSR"
408	001432	021360	DT6	;"STESTN,SERRPC,RCSR"
409	001434	000000	0	
410				
411	001436	016013	EM30	;"CAN NOT SET BIT6 OF RCSR"
412	001440	020647	DH6	;"TEST# ERR PC RCSR"
413	001442	021360	DT6	;"STESTN,SERRPC,RCSR"
414	001444	000000	0	
415				
416	001446	016044	EM31	;"CAN NOT CLEAR BIT6 OF RCSR"
417	001450	020647	DH6	;"TEST# ERR PC RCSR"
418	001452	021360	DT6	;"STESTN,SERRPC,RCSR"
419	001454	000000	0	
420				
421	001456	016077	EM32	;"CAN NOT CLEAR BIT6 OF RCSR WITH RESET2"
422	001460	020647	DH6	;"TEST# ERR PC RCSR"
423	001462	021360	DT6	;"STESTN,SERRPC,RCSR"
424	001464	000000	0	
425				
426	001466	016145	EM33	;"BIT6 OF LKS NOT CLEAR AFTER RESET"
427	001470	020721	DH10	;"TEST# ERR PC LKS"
428	001472	021400	DT10	;"STESTN,SERRPC,LKS"
429	001474	000000	0	
430				
431	001476	016207	EM34	;"LKS INTERRUPT WITH PRIORITY 7"
432	001500	020721	DH10	;"TEST# ERR PC LKS"
433	001502	021400	DT10	;"STESTN,SERRPC,LKS"
434	001504	000000	0	
435				
436	001506	016245	EM35	;"CAN NOT SET BIT6 OF LKS"
437	001510	020721	DH10	;"TEST# ERR PC LKS"
438	001512	021400	DT10	;"STESTN,SERRPC,LKS"
439	001514	000000	0	
440				
441	001516	016275	EM36	;"CAN NOT CLEAR BIT6 OF LKS"
442	001520	020721	DH10	;"TEST# ERR PC LKS"
443	001522	021400	DT10	;"STESTN,SERRPC,LKS"
444	001524	000000	0	
445				
446	001526	016327	EM37	;"RESET DID NOT CLEAR BIT6 OF LKS"

447	001530	020721	DH10	:"TEST# ERR PC LKS"
448	001532	021400	DT10	:"STESTN, SERRPC, LKS"
449	001534	000000	0	
450				
451	001536	016367	EM40	:"DUAL ADDRESSING ERROR"
452	001540	020745	DH40	:"TEST# ERR PC GOOD BAD"
453	001542	021410	DT40	:"STESTN, SERRPC, RCSR, BDCSR"
454	001544	000000	0	
455				
456	001546	016415	EM41	:"BIT7 OF LKS NOT SET AFTER RESET2"
457	001550	020721	DH10	:"TEST# ERR PC LKS"
458	001552	021400	DT10	:"STESTN, SERRPC, LKS"
459	001554	000000	0	
460				
461	001556	016455	EM42	:"CAN NOT CLEAR BIT7 OF LKS"
462	001560	020721	DH10	:"TEST# ERR PC LKS"
463	001562	021400	DT10	:"STESTN, SERRPC, LKS"
464	001564	000000	0	
465				
466	001566	016507	EM43	:"BIT7 OF LKS DOES NOT SET"
467	001570	020721	DH10	:"TEST# ERR PC LKS"
468	001572	021400	DT10	:"STESTN, SERRPC, LKS"
469	001574	000000	0	
470				
471	001576	016540	EM44	:"RTC INTERRUPT AT PRIORITY 7"
472	001600	020721	DH10	:"TEST# ERR PC LKS"
473	001602	021400	DT10	:"STESTN, SERRPC, LKS"
474	001604	000000	0	
475				
476	001606	016574	EM45	:"RTC INTERRUPTS WHEN DISABLED"
477	001610	020721	DH10	:"TEST# ERR PC LKS"
478	001612	021400	DT10	:"STESTN, SERRPC, LKS"
479	001614	000000	0	
480				
481	001616	016631	EM46	:"RTC INTERRUPT DID NOT OCCUR"
482	001620	020721	DH10	:"TEST# ERR PC LKS"
483	001622	021400	DT10	:"STESTN, SERRPC, LKS"
484	001624	000000	0	
485				
486	001626	016631	EM47	:"RTC INTERRUPT DID NOT OCCUR"
487	001630	020721	DH10	:"TEST# ERR PC LKS"
488	001632	021400	DT10	:"STESTN, SERRPC, LKS"
489	001634	000000	0	
490				
491	001636	016665	EM50	:"RTC DOUBLE INTERRUPT"
492	001640	020721	DH10	:"TEST# ERR PC LKS"
493	001642	021400	DT10	:"STESTN, SERRPC, LKS"
494	001644	000000	0	
495				
496	001646	016712	EM51	:"RESET DID NOT CLEAR RTC INTERRUPT"
497	001650	020721	DH10	:"TEST# ERR PC LKS"
498	001652	021400	DT10	:"STESTN, SERRPC, LKS"
499	001654	000000	0	
500				
501	001656	016742	EM52	:"RTC INTERRUPT DID NOT CLEAR WITH BIT7 OF LKS"
502	001660	020721	DH10	:"TEST# ERR PC LKS"

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 DZDLDA.P11 ERROR POINTER TABLE

SEQ 0021

503	001662	021400	DT10	;STESTN,SERRPC,LKS
504	001664	000000	0	
505				
506	001666	017017	EM53	;"TEST# ERR PC LKS CNT1 CNT2"
507	001670	021001	DH53	;"TEST# ERR PC LKS CNT1 CNT2"
508	001672	021422	DT53	;"TEST# ERR PC LKS CNT1 CNT2"
509	001674	000000	0	;STESTN,SERRPC,LKS,FIRST,SECND
510				
511	001676	017043	EM54	;"XMIT INTERRUPTS WHEN DISABLED"
512	001700	020575	DH1	;"TEST# ERR PC TCSR"
513	001702	021340	DT1	;"TEST# ERR PC TCSR"
514	001704	000000	0	;STESTN,SERRPC,TCSR
515				
516	001706	017201	EM55	;"XMIT DID NOT INTERRUPT"
517	001710	020575	DH1	;"TEST# ERR PC TCSR"
518	001712	021340	DT1	;"TEST# ERR PC TCSR"
519	001714	000000	0	;STESTN,SERRPC,TCSR
520				
521	001716	017101	EM56	;"XMIT INTERRUPT AT PRIORITY 7"
522	001720	020575	DH1	;"TEST# ERR PC TCSR"
523	001722	021340	DT1	;"TEST# ERR PC TCSR"
524	001724	000000	0	;STESTN,SERRPC,TCSR
525				
526	001726	017137	EM57	;"XMIT INTERRUPTS WITH ENABLE CLEAR"
527	001730	020575	DH1	;"TEST# ERR PC TCSR"
528	001732	021340	DT1	;"TEST# ERR PC TCSR"
529	001734	000000	0	;STESTN,SERRPC,TCSR
530				
531	001736	017201	EM60	;"XMIT DID NOT INTERRUPT"
532	001740	020575	DH1	;"TEST# ERR PC TCSR"
533	001742	021340	DT1	;"TEST# ERR PC TCSR"
534	001744	000000	0	;STESTN,SERRPC,TCSR
535				
536	001746	017230	EM61	;"XMIT RE-INTERRUPTED"
537	001750	020575	DH1	;"TEST# ERR PC TCSR"
538	001752	021340	DT1	;"TEST# ERR PC TCSR"
539	001754	000000	0	;STESTN,SERRPC,TCSR
540				
541	001756	017254	EM62	;"LOADING 1BUF DID NOT CLEAR INTERRUPT"
542	001760	020575	DH1	;"TEST# ERR PC TCSR"
543	001762	021340	DT1	;"TEST# ERR PC TCSR"
544	001764	000000	0	;STESTN,SERRPC,TCSR
545				
546	001766	017321	EM63	;"RCVR ACTIVE NOT SET"
547	001770	020647	DH6	;"TEST# ERR PC RCSR"
548	001772	021360	DT6	;"TEST# ERR PC RCSR"
549	001774	000000	0	;STESTN,SERRPC,RCSR
550				
551	001776	017345	EM64	;"RECEIVER DONE NEVER SET"
552	002000	020647	DH6	;"TEST# ERR PC RCSR"
553	002002	021360	DT6	;"TEST# ERR PC RCSR"
554	002004	000000	0	;STESTN,SERRPC,RCSR
555				
556	002006	017371	EM65	;"RCVR ACTIVE NOT CLEARED WITH DONE SET2"
557	002010	020647	DH6	;"TEST# ERR PC RCSR"
558	002012	021360	DT6	;"TEST# ERR PC RCSR"

559	002014	000000	0	
560				
561	002016	017437	EM66	:"RESET DID NOT CLEAR RCVR DONE"
562	002020	020647	DH6	:"TEST# ERR PC RCSR"
563	002022	021360	DT6	:"STESTN, SERRPC, RCSR"
564	002024	000000	0	
565				
566	002026	017475	EM67	:"RDR ENABLE SET DID NOT CLEAR RCVR DONE"
567	002030	020647	DH6	:"TEST# ERR PC RCSR"
568	002032	021360	DT6	:"STESTN, SERRPC, RCSR"
569	002034	000000	0	
570				
571	002036	017540	EM70	:"READING RBUF DID NOT CLEAR RCVR DONE"
572	002040	020647	DH6	:"TEST# ERR PC RCSR"
573	002042	021360	DT6	:"STESTN, SERRPC, RCSR"
574	002044	000000	0	
575				
576	002046	017605	EM71	:"RCVR INTERRUPTS WITH ENABLE CLEAR"
577	002050	020647	DH6	:"TEST# ERR PC RCSR"
578	002052	021360	DT6	:"STESTN, SERRPC, RCSR"
579	002054	000000	0	
580				
581	002056	017754	EM72	:"RCVR DID NOT INTERRUPT"
582	002060	020647	DH6	:"TEST# ERR PC RCSR"
583	002062	021360	DT6	:"STESTN, SERRPC, RCSR"
584	002064	000000	0	
585				
586	002066	017647	EM73	:"RCVR INTERRUPTS AT PRIORITY 7"
587	002070	020647	DH6	:"TEST# ERR PC RCSR"
588	002072	021360	DT6	:"STESTN, SERRPC, RCSR"
589	002074	000000	0	
590				
591	002076	017705	EM74	:"RCVR INTERRUPT REQUEST PASSED WITH ENABLE CLEAR"
592	002100	020647	DH6	:"TEST# ERR PC RCSR"
593	002102	021360	DT6	:"STESTN, SERRPC, RCSR"
594	002104	000000	0	
595				
596	002106	017754	EM75	:"RCVR DID NOT INTERRUPT"
597	002110	020647	DH6	:"TEST# ERR PC RCSR"
598	002112	021360	DT6	:"STESTN, SERRPC, RCSR"
599	002114	000000	0	
600				
601	002116	020003	EM76	:"RECEIVER RE-INTERRUPTED"
602	002120	020647	DH6	:"TEST# ERR PC RCSR"
603	002122	021360	DT6	:"STESTN, SERRPC, RCSR"
604	002124	000000	0	
605				
606	002126	020027	EM77	:"READING RBUF DID NOT CLEAR INTERRUPT"
607	002130	020647	DH6	:"TEST# ERR PC RCSR"
608	002132	021360	DT6	:"STESTN, SERRPC, RCSR"
609	002134	000000	0	
610				
611	002136	020074	EM100	:"RESET DID NOT CLEAR RCVR INTERRUPT"
612	002140	020647	DH6	:"TEST# ERR PC RCSR"
613	002142	021360	DT6	:"STESTN, SERRPC, RCSR"
614	002144	000000	0	

615				
616				
617	002146	020137	EM101	;'OR' FLAG DID NOT SET"
618	002150	020647	DH6	
619	002152	021360	DT6	;STESTN,SERRPC,RCSR
620	002154	000000	0	
621				
622	002156	020165	EM102	;'ERROR' NOT SET WITH 'OR' FLAG"
623	002160	020647	DH6	;'TEST# ERR PC RCSR"
624	002162	021360	DT6	;STESTN,SERRPC,RCSR
625	002164	000000	0	
626				
627	002166	020224	EM103	;'BREAK DID NOT TRANSMIT ALL ZEROES"
628	002170	021046	DH103	;'TEST# ERR PC RCSR DATA"
629	002172	021436	DT103	;STESTN,SERRPC,RCSR,SDDAT
630	002174	000000	0	
631				
632	002176	020262	EM104	;'BREAK DID NOT SET FRAMING ERROR"
633	002200	020647	DH6	;'TEST# ERR PC RCSR"
634	002202	021360	DT6	;STESTN,SERRPC,RCSR
635	002204	000000	0	
636				
637	002206	020317	EM105	;'DATA COMPARE ERROR"
638	002210	021103	DH105	;'TEST# ERR PC RCSR GOOD BAD"
639	002212	021450	DT105	;STESTN,SERRPC,RCSR,GD,BD
640	002214	000000	0	
641				
642	002216	020342	EM106	;'DATA COMPARE ERROR WITH CABLE"
643	002220	021103	DH105	;'TEST# ERR PC RCSR GOOD BAD"
644	002222	021450	DT105	;STESTN,SERRPC,RCSR,GD,BD
645	002224	000000	0	
646				
647	002226	020400	EM107	;'TIMEOUT IN EXERCISER TEST"
648	002230	020647	DH6	;'TEST# ERR PC RCSR"
649	002232	021360	DT6	;STESTN,SERRPC,RCSR
650	002234	000000	0	
651				
652	002236	020432	EM110	;'INCORRECT RECEIVE COUNT"
653	002240	021147	DH110	;'TEST# ERR PC RCSR TRANS RCV"
654	002242	021464	DT110	;STESTN,SERRPC,RCSR,XMTCNT,RCVCNT
655	002244	000000	0	
656				
657	002246	020462	EM111	;'DATA COMPARE ERROR IN EXERCISER"
658	002250	021103	DH105	;'TEST# ERR PC RCSR GOOD BAD"
659	002252	021450	DT105	;STESTN,SERRPC,RCSR,GD,BD
660	002254	000000	0	
661				
662	002256	020522	EM112	;'TRAP CATCHER"
663	002260	021213	DH112	;'TEST# ERR PC RCSR OLDPC TRAP ADR"
664	002262	021500	DT112	;STESTN,SERRPC,RCSR,OLDPC,BDVECT
665	002264	000000	0	
666				
667	002266	020537	EM113	;'NO CLK INTERRUPT IN EXERCISER"
668	002270	020721	DH10	;'TEST# ERR PC LKS"
669	002272	021400	DT10	;STESTN,SERRPC,LKS
670	002274	000000	0	

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671
672 002275 000000      CTSTFL: .WORD 0          ;CONSOLE UNDER TEST FLAG
673 002300 000000      TMP1:  .WORD 0          ;TEMP LOCATION FOR TABLE OFFSETS
674 002302 000000      TMP2:  .WORD 0          ;TEMP LOCATION FOR DEVICE COUNT
675 002304 000000      TMP3:  .WORD 0          ;LOCATION FOR DEVICE MAP BIT TEST MASK
676                                     ;REGISTER AND VECTOR ADDRESSES FOR THE DL-11W UNDER TEST
677
678 002306 000000      RCSR:  .WORD 0
679 002310 000000      RBUF:  .WORD 0
680 002312 000000      TCSR:  .WORD 0
681 002314 000000      TBUF:  .WORD 0
682 002316 000000      RVECT: .WORD 0
683 002320 000000      RPSW:  .WORD 0
684 002322 000000      TVECT: .WORD 0
685 002324 000000      TPSW:  .WORD 0
686
687                                     ;CONSOLE REGISTER AND VECTOR ADDRESSES FOR THE DL-11W
688
689 002326 177560      CRCSR: 177560          ;ADDRESS OF RECEIVER COMMAND/STATUS REGISTER
690 002330 177562      CRBUF: 177562          ;ADDRESS OF RECEIVER BUFFER
691 002332 177564      CTCSR: 177564          ;ADDRESS OF TRANSMITTER COMMAND/STATUS REGISTER
692 002334 177566      CTBUF: 177566          ;ADDRESS OF TRANSMITTER BUFFER
693 002336 000060      CRVECT: 60            ;RECEIVER INTERRUPT VECTOR
694 002340 000062      CRPSW: 62
695 002342 000064      CTVECT: 64            ;TRANSMITTER INTERRUPT VECTOR
696 002344 000066      CTPSW: 66
697
698                                     ;REAL TIME CLOCK REGISTER AND VECTOR ADDRESSES
699 002346 177546      LKS:   .WORD 177546
700 002350 000100      RTCVT: .WORD 100
701 002352 000102      RTCPSW: .WORD 102
702
703 002354 000020      ADRTBL: .BLKW 20
704 002414 000020      VCTTBL: .BLKW 20
705
706
707                                     ;SUBROUTINE TO GENERATE DEVICE ADDRESS TABLE
708
709 002454 012702 002354      DEVADR: MOV      @ADRTBL,R2          ;POINT R2 TO THE DEVICE ADDRESS TABLE
710 002460 016700 176456      MOV      $BASE,R0          ;LOAD BASE DEVICE ADDRESS IN R0
711 002464 010001          MOV      R0,R1
712 002466 062701 000170      ADD      @170,R1          ;POINT R1 TO LAST DEVICE ADDRESS
713 002472 010022          MOV      R0,(R2)+          ;MOVE DEVICE ADDRESS TO TABLE
714 002474 062700 000010      ADD      @10,R0          ;POINT R0 TO NEXT DEVICE ADDRESS
715 002500 020001          CMP      R0,R1          ;FINISHED GENERATING TABLE?
716 002502 003773          BLE     1$              ;BR, IF LAST DEVICE ADDRESS NOT LOADED
717 002504 000207          RTS      PC
718
719
720
721 002506 005067 176356      START: CLR      $FATAL          ;CLEAR ERROR NO.
722 002512 005067 176350      CLR      $MSGTYP          ;CLEAR MESSAGE TYPE
723 002516 005067 176350      CLR      $TESTN          ;CLEAR TEST NO.
724 002522 005067 177550      CLR      CTSTFL          ;CLEAR CONSOLE UNDER TEST FLAG
725 002526 005067 176344      CLR      $DEVCT          ;CLEAR DEVICE COUNT
726 002532 005067 176342      CLR      $UNIT          ;CLEAR UNIT NUMBER

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727 002536 012737 000006 000004      MOV      #6,2#4      ;INITIALIZE TIMEOUT VECTORS TO TRAP
728 002544 012737 000003 000006      MOV      #3,2#6      ; CATCHER ROUTINE
729
730      .SBTTL INITIALIZE THE COMMON TAGS
731      ;;CLEAR THE COMMON TAGS (SCMTAG) AREA
732 002552 012706 001000      MOV      #SCMTAG,R6  ;;FIRST LOCATION TO BE CLEARED
733 002556 005026      CLR      (R6)+      ;;CLEAR MEMORY LOCATION
734 002560 022706 001040      CMP      #SWR,R6    ;;DONE?
735 002564 001374      BNE      #-6        ;;LOOP BACK IF NO
736 002566 012706 001000      MOV      #1000,SP   ;;SETUP THE STACK POINTER
737      ;;INITIALIZE A FEW VECTORS
738 002572 012737 012326 000020      MOV      #SSCOPE,2#IOTVEC ;;IOT VECTOR FOR SCOPE ROUTINE
739 002600 012737 000340 000022      MOV      #340,2#IOTVEC+2 ;;LEVEL 7
740 002606 012737 011632 000030      MOV      #ERROR,2#EMTVEC ;;EMT VECTOR FOR ERROR ROUTINE
741 002614 012737 000340 000032      MOV      #340,2#EMTVEC+2 ;;LEVEL 7
742 002622 012737 014232 000034      MOV      #STRAP,2#TRAPVEC ;;TRAP VECTOR FOR TRAP CALLS
743 002630 012737 000340 000036      MOV      #340,2#TRAPVEC+2;LEVEL 7
744 002636 012737 012150 000024      MOV      #SPWRDN,2#PWRVEC ;;POWER FAILURE VECTOR
745 002644 012737 000340 000026      MOV      #340,2#PWRVEC+2 ;;LEVEL 7
746 002652 016767 006602 006572      MOV      SENDCT,SEOPCT ;;SETUP END-OF-PROGRAM COUNTER
747 002660 005067 176174      CLR      SESCAPP    ;;CLEAR THE ESCAPE ON ERROR ADDRESS
748 002664 112767 000001 176123      MOVB    #1,SERMAX   ;;ALLOW ONE ERROR PER TEST
749 002672 012767 002672 176106      MOV      #.,SLPADR   ;;INITIALIZE THE LOOP ADDRESS FOR SCOPE
750 002700 012767 002700 176102      MOV      #.,SLPERR   ;;SETUP THE ERROR LOOP ADDRESS
751      ;;SIZE FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS
752      ;;EQUAL TO A "-1" SETUP FOR A SOFTWARE SWITCH REGISTER.
753 002706 013746 000004      MOV      2#ERRVEC,-(SP) ;;SAVE ERROR VECTOR
754 002712 012737 002746 000004      MOV      #64$,2#ERRVEC ;;SET UP ERROR VECTOR
755 002720 012767 177570 176112      MOV      #DSWR,SWR   ;;SETUP FOR A HARDWARE SWICH REGISTER
756 002726 012767 177570 176106      MOV      #DDISP,DISPLAY ;;AND A HARDWARE DISPLAY REGISTER
757 002734 022777 177777 176076      CMP      #-1,2#SWR  ;;TRY TO REFERENCE HARDWARE SWR
758 002742 001012      BNE      66$        ;;BRANCH IF NO TIMEOUT TRAP OCCURRED
759      ;;AND THE HARDWARE SWR IS NOT = -1
760 002744 000403      BR      65$        ;;BRANCH IF NO TIMEOUT
761 002746 012716 002754      64$: MOV      #65$, (SP)  ;;SET UP FOR TRAP RETURN
762 002752 000002      RTI
763 002754 012767 000176 176056      65$: MOV      #SWREG,SWR ;;POINT TO SOFTWARE SWR
764 002762 012767 000174 176052      MOV      #DISPREG,DISPLAY
765 002770 012637 000004      66$: MOV      (SP)+,2#ERRVEC ;;RESTORE ERROR VECTOR
766
767 002774 005067 176074      CLR      $PASS      ;;CLEAR PASS COUNT
768 003000 132767 000200 176101      BITB    #APTSIZE,$ENVM ;;TEST USER SIZE UNDER APT
769 003006 001403      BEQ     67$        ;;YES,USE NON-APT SWITCH
770 003010 012767 001110 176022      MOV     #SSWREG,SWR ;;NO,USE APT SWITCH REGISTER
771 003016      67$:
772 003016 132767 000001 176062      BITB    #BIT0,$ENV  ;;CHECK IF ON APT
773 003024 001404      BEQ     MANL      ;;BR IF NOT APT
774 003026 132767 000200 176053      BITB    #BIT7,$ENVM ;;DID APT SIZE
775 003034 001056      BNE     APTSZD    ;;BR, IF APT SIZED
776 003036 032777 000040 175774      MANL: BIT     #BITS,2#SWR ;;WAS "$DEVN" MANUALLY SET?
777 003044 001052      BNE     APTSZD    ;;IF YES, SKIP SELF-SIZING
778
779 003046 004767 177402      SIZE: JSR     PC,DEVADR ;;GENERATE DEVICE ADDRESS TABLE
780 003052 005067 177224      CLR     TMP2      ;;CLR TEMP LOCATION TO KEEP DEVICE COUNT
781 003056 005067 176062      CLR     $DEVN     ;;CLEAR DEVICE MAP
782 003062 013703 000004      MOV     2#4,R3    ;;SAVE TIMEOUT VECTOR
  
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783 003066 012737 003116 000004      MOV      #45,2#4      ;SET TIMEOUT POINTER
784 003074 016700 176042      MOV      $BASE,R0    ;LOAD BASE ADDRESS
785 003100 062700 000160      ADD      #160,R0     ;POINT R0 TO UNIT #15 (UNIT#0=CONSOLE)
786 003104 005710      3$:      TST      (R0)        ;CHECK FOR DEVICE EXISTANCE
787 003106 005267 176032      INC      $DEVN       ;INDICATE DEVICE EXISTANCE IN DEVICE MAP
788 003112 005267 177164      INC      TMP2        ;INCREMENT DEVICE COUNT
789 003116 012706 001000      4$:      MOV      #1000,SP    ;RESET STACK POINTER
790 003122 006367 176016      ASL     $DEVN       ;ADJUST DEVICE MAP FOR NEXT UNIT CHECK
791 003126 162700 000010      SLB     #10,R0      ;POINT R0 TO NEXT DEVICE NUMBER
792 003132 026700 176004      CMP     $BASE,R0    ;FINISHED SIZING?
793 003136 003762      BLE     3$          ;BR, IF BASE ADDRESS HAS NOT BEEN CHECKED
794 003140 016700 177162      MOV     CRCSR,R0    ;LOAD CONSOLE DEVICE ADDRESS
795 003144 012737 003164 000004      MOV     #55,2#4     ;SET UP TIMEOUT POINTER
796 003152 005710      TST     (R0)        ;TEST FOR CONSOLE EXISTANCE
797 003154 005267 175764      INC     $DEVN       ;INDICATE CONSOLE EXISTANCE IN DEVICE MAP
798 003160 005267 177116      INC     TMP2        ;INCREMENT DEVICE COUNT
799 003164 010337 000004      5$:      MOV     R3,2#4      ;RESTORE TIMEOUT VECTOR
800 003170 000415      BR      VCTADR      ;BR TO GENERATE VECTOR ADDRESS TABLE
801
802 003172 005067 177104      APTSZD: CLR     TMP2      ;CLEAR TEMP LOCATION TO KEEP DEVICE CNT
803 003176 016702 175742      MOV     $DEVN,R2    ;MOVE DEVICE MAP TO R2
804 003202 005702      TSTDVM: TST     R2      ;TEST MSB OF DEVICE MAP
805 003204 100002      BPL     1$          ;BR, IF MSB IS ZERO
806 003206 005267 177070      INC     TMP2        ;INCREMENT DEVICE COUNT, IF MSB=1
807 003212 006302      1$:      ASL     R2          ;SHIFT NEXT BIT INTO MSB POSITION
808 003214 001401      BEQ     DVADT       ;BR, IF NO OTHER BITS ARE SET IN $DEVN
809 003216 000771      BR      TSTDVM      ;CONTINUE CHECKING $DEVN, IF MORE BITS SET
810 003220 004767 177230      DVADT:  JSR     PC,DEVADR ;GENERATE DEVICE ADDRESS TABLE
811
812      ;GENERATE VECTOR ADDRESS TABLE
813
814 003224 012702 002414      VCTADR: MOV     #VCTTBL,R2 ;GET LOCATION OF VECTOR TABLE
815 003230 113700 001136      MOV     2#$VECT1,R0 ;COPY BASE VECTOR
816 003234 042700 177400      BIC     #177400,R0  ;CLEAR BYTE SIGN EXTENSION
817 003240 010001      MOV     R0,R1
818 003242 062701 000170      ADD     #170,R1
819 003246 010022      1$:      MOV     R0,(R2)+    ;POINT R1 TO LAST DEVICE VECTOR
820 003250 062700 000010      ADD     #10,R0      ;PUT VECTOR ADDRESS IN TABLE
821 003254 020001      CMP     R0,R1
822 003256 003773      BLE     1$          ;POINT R0 TO NEXT VECTOR ADDRESS
823
824      ;FINISHED GENERATING VECTOR TABLE?
825      ;BR, IF LAST VECTOR IS NOT LOADED
826
826 003260 016700 177016      ;MOVE DEVICE COUNT INTO DEVICE COUNT MESSAGE
827 003264 005001      MOV     TMP2,R0     ;COPY DEVICE COUNT INTO R0
828 003266 000300      CLR     R1          ;CLEAR AUXILIARY REGISTER
829 003270 006300      SWAB   R0          ;PUT DEVICE COUNT IN UPPER BYTE OF R0
830 003272 006300      ASL    R0          ;MOVE MSB OF COUNT INTO
831 003274 006300      ASL    R0          ;MSB OF R0
832 003276 106101      SHIFT: ASL    R0      ;PUT MSB OF COUNT INTO CARRY
833 003300 006300      ROLB   R1          ;MOVE MSB OF COUNT INTO R1
834 003302 106101      ASL    R0          ;MOVE NEXT BIT TO CARRY
835 003304 006300      ROLB   R1          ;MOVE INTO R1
836 003306 106101      ASL    R0          ;MOVE LAST BIT OF DIGIT
837 003310 062701 000060      ROLB   R1          ;INTO R1
838 003314 000301      ADD    #60,R1      ;CONVERT DIGIT TO ASCII
                        SWAB   R1      ;MOVE DIGIT TO UPPER BYTE

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839 003316 032701 000020 BIT #BIT4,R1 ;HAVE BOTH DIGITS BEEN MOVED TO R1?
840 003322 001764 BEQ SHIFT ;BR, IF NOT
841 003324 010167 015760 MOV R1,M2A ;MOVE DEVICE COUNT TO OUTPUT MESSAGE
842
843
844 003330 052767 000002 176746 BEGIN: BIS #BIT1,TMP3 ;SET UP BIT MASK TO TEST SDEVN FOR DEVICES EXCEPT CONSOL
845 003336 005067 176736 CLR TMP1 ;CLEAR LOCATION TO STORE TABLE OFFSETS
846 003342 032767 000001 175574 BIT #BIT0,SDEVN ;IS CONSOLE TO BE TESTED?
847 003350 001001 BNE TCONS ;BR, IF CONSOLE IS TO BE TESTED
848 003352 000414 BR TSTDEV ;BR, TO TEST OTHER DEVICES
849 003354 005267 176716 TCONS: INC CTSTFL ;INDICATE CONSOLE UNDER TEST
850 003360 012700 002326 MOV #CRCSR,R0 ;SET UP CONSOLE DEVICE ADDRESSES
851 003364 012701 002306 MOV #RCSR,R1 ;POINT R1 TO UUT ADDRESS TABLE
852 003370 012021 IS: MOV (R0)+,(R1)+ ;TRANSFER CONSOLE ADDRESSES
853 003372 022701 002324 CMP #TPSM,R1 ;FINISHED TRANSFER?
854 003376 002374 BGE IS ;BR, IF NOT
855 003400 000167 000122 JMP TST1 ;GO TEST CONSOLE INTERFACE
856
857 ;PREPARE ADDRESSES AND VECTORS FOR UUT
858 003404 036767 176674 175532 TSTDEV: BIT TMP3,SDEVN ;CHECK TO SEE IF DEVICE IS TO BE TESTED
859 003412 001010 BNE SETADR ;BR, IF YES
860 003414 006367 176664 ASL TMP3 ;SHIFT MASK TO CHECK NEXT SDEVN BIT
861 003420 062767 000002 176652 ADD #2,TMP1 ;INCREMENT TABLE INDEX
862 003426 005267 175446 INC $UNIT ;INCREMENT UNIT NUMBER
863 003432 000764 BR TSTDEV ;GO TEST NEXT BIT OF DEVICE MAP
864
865 003434 005267 175440 SETADR: INC $UNIT ;UPDATE UNIT NUMBER
866 003440 006367 176640 ASL TMP3 ;UPDATE DEVICE MAP TEST MASK
867 003444 016702 176630 MOV TMP1,R2 ;MOVE TABLE OFFSET TO R2
868 003450 062767 000002 176622 ADD #2,TMP1 ;UPDATE TABLE OFFSET FOR NEXT DEVICE
869 003456 016200 002354 MOV ADRTBL(R2),R0 ;PUT UUT ADDRESS INTO R0
870 003462 012701 002306 MOV #RCSR,R1 ;POINT R1 TO STORAGE AREA FOR UUT ADDRESSES
871 003466 010021 ADR: MOV R0,(R1)+ ;TRANSFER UUT ADDRESS
872 003470 062700 000002 ADD #2,R0 ;POINT TO NEXT UUT REGISTER
873 003474 030027 000006 BIT R0,#6 ;FINISHED TRANSFER?
874 003500 001372 BNE ADR ;BR, IF NOT
875
876 003502 016200 002414 VECT: MOV VCTTBL(R2),R0 ;PUT UUT VECTOR INTO R0
877 003506 010021 MOV R0,(R1)+ ;TRANSFER UUT VECTORS TO ACTIVE TABLE AREA
878 003510 062700 000002 ADD #2,R0 ;POINT TO NEXT VECTOR
879 003514 030027 000006 BIT R0,#6 ;FINISHED TRANSFER?
880 003520 001372 BNE VECT ;BR, IF NOT
881 003522 000167 000000 JMP TST1 ;GO TEST DEVICE
882
883

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884
885
886
887
888
889 003526 000004
890 003530 013703 000004
891 003534 012737 003550 000004
892 003542 005777 176544
893 003546 000412
894
895 003550 022626
896 003552 005767 176520
897 003556 001002
898 003560 104001
899 003562 000404
900 003564
901 003564 004767 006726
902 003570 000001
903 003572 000000
904 003574 010337 000004
905
906
907
908
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911 003600 000004
912 003602 013703 000004
913 003606 012737 003622 000004
914 003614 005777 176474
915 003620 000412
916
917 003622 022626
918 003624 005767 176446
919 003630 001002
920 003632 104002
921 003634 000404
922 003636
923 003636 004767 006654
924 003642 000002
925 003644 000000
926 003646 010337 000004

:*****
:TEST 1 TEST ABILITY TO REFERENCE TCSR
:*****
TST1: SCOPE
      MOV 2#4,R3 ;SAVE TIMEOUT VECTOR
      MOV 815,2#4 ;SET UP TIMEOUT VECTOR
      TST 2TCSR ;REFERENCE THE XMIT COMMAND/STATUS REG.
      BR 45 ;GO TO END OF TEST

15: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
     TST CTSTFL ;CHECK IF DEVICE IS CONSOLE
     BNE 25 ;IF YES, SKIP ERROR TYPEOUT
     ERROR 1 ;REPORT ERROR TO APT & TTY
     BR 45 ;BR TO END OF TEST

25: JSR PC,SATY4 ;: ONLY REPORT A FATAL ERROR
     ;: THE ERROR NUMBER (FROM APT LIST)

35: HALT
45: MOV R3,2#4 ;RESTORE TIMEOUT VECTOR

:*****
:TEST 2 TEST ABILITY TO REFERENCE TBUF
:*****
TST2: SCOPE
      MOV 2#4,R3 ;SAVE TIMEOUT VECTOR
      MOV 815,2#4 ;SET UP TIMEOUT VECTOR
      TST 2TBUF ;REFERENCE THE XMIT BUFFER
      BR 45 ;GO TO END OF TEST

15: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
     TST CTSTFL ;CHECK IF DEVICE IS CONSOLE
     BNE 25 ;IF YES, SKIP ERROR TYPEOUT
     ERROR 2 ;REPORT ERROR TO APT & TTY
     BR 45 ;BR TO END OF TEST

25: JSR PC,SATY4 ;: ONLY REPORT A FATAL ERROR
     ;: THE ERROR NUMBER (FROM APT LIST)

35: HALT
45: MOV R3,2#4 ;RESTORE TIMEOUT VECTOR
  
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927
928
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930
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932 003652 000004
933 003654 005077 176434
934 003660 105777 176426
935 003664 100016
936
937
938 003666 005077 176422
939 003672 105777 176414
940 003676 100011
941
942 003700 005767 176372
943 003704 001002
944 003706 104003
945 003710 000404
946 003712
947 003712 004767 006600
948 003716 000003
949 003720
950 003722 005000
951 003724 105777 176362
952 003730 100414
953 003732 005200
954 003734 001373
955
956 003736 005767 176334
957 003742 001002
958 003744 104004
959 003746 000405
960 003750
961 003750 004767 006542
962 003754 000004
963 003756 001000
964 003760 000415
965
966
967 003762 005737 000042
968 003766 001012
969 003770 005767 175100
970 003774 001007
971 003776 005767 175074
972 004002 001004
973 004004 104401
974 004006 021264
975 004010 104401
976 004012 021306

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```

*****
TEST 3 TEST THAT TCSR BIT7(DONE) CLEARS WHEN XBUF IS LOADED
*****
TST3: SCOPE
CLR @TBUF ;LOAD XBUF
TSTB @TCSR ;CHECK DONE
BPL 3$ ;BR IF CLEAR
;FILL SECOND BUFFER, BECAUSE REFRESH COULD CAUSE
; FIRST TEST TO FAIL
CLR @TBUF ;FILL DOUBLE BUFFER
TSTB @TCSR ;CHECK DONE
BPL 3$ ;BR IF CLEAR

TST CTSTFL ;CHECK IF DEVICE IS CONSOLE
BNE 1$ ;IF YES, SKIP ERROR TYPEOUT
ERROR 3 ;DONE NOT CLEARED WITH TBUF FULL
BR 3$ ;BR TO END OF TEST

1$: JSR PC,SATY4 ;ONLY REPORT A FATAL ERROR
3 ;THE ERROR NUMBER (FROM APT LIST)
2$: HALT ;TCSR "DONE" NOT CLEARED WITH TBUF FULL
3$: CLR R0 ;CLEAR TIMER
4$: TSTB @TCSR ;CHECK FOR XMIT DONE
BMI 6$ ;IF DONE SETS, BR TO NEXT TEST
INC R0 ;INCREMENT TIMER
BNE 4$ ;BR IF TIMER NOT DONE

TST CTSTFL ;CHECK IF DEVICE IS CONSOLE
BNE 5$
ERROR 4 ;TCSR "DONE" DOES NOT SET
BR 6$ ;BR TO END OF TEST

5$: JSR PC,SATY4 ;ONLY REPORT A FATAL ERROR
4 ;THE ERROR NUMBER (FROM APT LIST)
HALT 4
BR TST4 ;BR TO NEXT TEST, AND SKIP THE TYPEOUT THAT FOLLOWS
; BECAUSE OF THIS FAILURE

6$: TST @#42 ;UNDER ACT11?
BNE TST4 ;IF YES, SKIP IDENT. TYPEOUT
TST $PASS ;IS THIS THE FIRST PASS?
BNE TST4 ;IF NOT BR TO NEXT TEST & SKIP THE IDENTIFICATION TYPEOU
TST $DEVCT ;IS THIS THE FIRST SUBPASS?
BNE TST4 ;IF NOT, BR TO NEXT TEST
TYPE ;TYPE PROGRAM IDENTIFICATION
M1 ;TYPE NUMBER OF DEVICES UNDER TEST
TYPE M2

```

# E03

.MAIN. MACY11 27(732) 02-NOV-76 16:15 PAGE 21  
 DZDLDA.P11 T3 TEST THAT TCSR BIT7(DONE) CLEARS WHEN XBUF IS LOADED

SEQ 0030

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977
978
979
980
981
982 004014 000004
983 004016 005077 176272
984 004022 105777 176264
985 004026 100375
986 004030 005077 176260
987 004034 000240
988 004036 000005
989 004040 105777 176246
990 004044 100401
991
992 004046 104005
993
994
995
996
997
998
999 004050 000004
1000 004052 013703 000004
1001 004056 012737 004072 000004
1002 004064 005777 176216
1003 004070 000402
1004
1005 004072 022626
1006 004074 104006
1007 004076 010337 000004

:*****
:TEST 4 TEST THAT TCSR "DONE" SETS WITH RESET
:*****
TST4: SCOPE
1S: CLR JTBUF ;LOAD TRANSMIT BUFFER
TSTB JTCR ;WAIT FOR DONE
BPL 1S
CLR JTBUF ;LOAD SECOND BUFFER
NOP
RESET ;CLEAR DONE WITH RESET
TSTB JTCR ;CHECK FOR DONE SET
BMI TST5 ;BR TO NEXT TEST IF DONE SET
ERROR 5 ;TCSR "DONE" DOES NOT SET WITH RESET

:*****
:TEST 5 TEST ABILITY TO ACCESS RCSR
:*****
TST5: SCOPE
MOV J#4,R3 ;SAVE TIMEOUT VECTOR
MOV #1S,J#4 ;SET UP TIMEOUT VECTOR
TST JRCR ;ACCESS RCSR
BR ZS ;BR TO END OF TEST
1S: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
ERROR 6 ;CAN NOT ACCESS RCSR
2S: MOV R3,J#4 ;RESTORE TIMEOUT VECTOR
  
```

# F03

.MAIN. MACY11 27(732) 02-NOV-76 16:15 PAGE 22  
 DZDLDA.P11 TS TEST ABILITY TO ACCESS RCSR

SEQ 0031

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1008
1009
1010
1011
1012
1013 004102 000004
1014 004104 013703 000004
1015 004110 012737 004124 000004
1016 004116 005777 176166
1017 004122 000402
1018
1019 004124 022626
1020 004126 104007
1021 004130 010337 000004
1022
1023
1024
1025
1026
1027
1028 004134 000004
1029 004136 005767 176134
1030 004142 001420
1031 004144 032777 000100 174666
1032 004152 001014
1033 004154 013703 000004
1034 004160 012737 004174 000004
1035 004166 005777 176154
1036 004172 000402
1037
1038 004174 022626
1039 004176 104010
1040
1041 004200 010337 000004
1042

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```

*****
*TEST 6 TEST ABILITY TO ACCESS RBUF
*****
TST6: SCOPE
      MOV R3,R3 ;SAVE TIMEOUT VECTOR
      MOV R15,R3 ;SET UP TIMEOUT VECTOR
      TST RBUF ;ACCESS RBUF
      BR 2S ;BR TO END OF TEST

1S: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
     ERROR 7 ;CAN NOT ACCESS RBUF
2S: MOV R3,R3 ;RESTORE TIMEOUT VECTOR

*****
*TEST 7 TEST ABILITY TO ACCESS LKS
*****
TST7: SCOPE
      TST CTSTFL ;IS CONSOLE UNDER TEST?
      BEQ TST10 ;IF NOT, SKIP THIS TEST
      BIT #BIT6,DSMR ;ARE LINE CLOCK TESTS INHIBITED?
      BNE TST10 ;IF YES, SKIP THIS TEST
      MOV R3,R3 ;SAVE TIMEOUT VECTOR
      MOV R15,R3 ;SET UP TIMEOUT VECTOR
      TST LKS ;ACCESS LKS
      BR 2S ;NO TIMEOUT - BR TO END OF TEST

1S: CMP (SP)+,(SP)+ ;RESTORE SP AFTER TIMEOUT
     ERROR 10 ;CAN NOT ACCESS LKS
2S: MOV R3,R3 ;RESTORE TIMEOUT VECTOR

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1043
1044
1045
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1047
1048 004204 000004
1049 004206 032777 000400 174624
1050 004214 001462
1051 004216 000005
1052 004220 032777 000001 176064
1053 004226 001411
1054 004230 005767 176042
1055 004234 001002
1056 004236 104011
1057 004240 000404
1058 004242
1059 004242 004767 006250
1060 004246 000011
1061 004250 000000
1062
1063 004252 052777 000001 176032
1064 004260 032777 000001 176024
1065 004266 001001
1066
1067 004270 104012
1068
1069 004272 042777 000001 176012
1070 004300 032777 000001 176004
1071 004306 001411
1072 004310 005767 175762
1073 004314 001002
1074 004316 104013
1075 004320 000404
1076 004322
1077 004322 004767 006170
1078 004326 000013
1079 004330 000000
1080
1081 004332 052777 000001 175752
1082 004340 000005
1083 004342 032777 000001 175742
1084 004350 001404
1085 004352 042777 000001 175732
1086 004360 104014

*****
*TEST 10 TEST THAT BITO(BREAK BIT) CAN BE SET & CLEARED & RESET
*****
TST10: SCOPE
BIT #BIT0,@SMR ;IS BREAK FUNCTION ENABLED?
BEQ TST11 ;BR TO NEXT TEST, IF NOT
RESET ;CLEAR EVERYTHING
BIT #BIT0,@TCSR ;CHECK BIT0 OF TCSR CLEAR
BEQ 3$ ;BR IF CLEAR
TST CTSTFL
BNE 1$
ERROR 11 ;BIT0 WAS NOT CLEAR AFTER RESET
BR 3$

1$: JSR PC,@ATY4 ;: ONLY REPORT A FATAL ERROR
;: THE ERROR NUMBER (FROM APT LIST)
2$: HALT

3$: BIS #BIT0,@TCSR ;SET BIT0 IN TCSR
BIT #BIT0,@TCSR ;TEST BIT0 OF TCSR
BNE 4$ ;BR IF SET

ERROR 12 ;BIT0 OF TCSR WILL NOT SET

4$: BIC #BIT0,@TCSR ;CLEAR BIT0 OF TCSR
BIT #BIT0,@TCSR ;TEST BIT0 OF TCSR
BEQ 7$
TST CTSTFL
BNE 5$
ERROR 13 ;BIT0 OF TCSR WILL NOT CLEAR
BR 7$

5$: JSR PC,@ATY4 ;: ONLY REPORT A FATAL ERROR
;: THE ERROR NUMBER (FROM APT LIST)
6$: HALT

7$: BIS #BIT0,@TCSR ;SET BIT0 IN TCSR
RESET ;CLEAR BIT0 WITH RESET
BIT #BIT0,@TCSR ;TEST BIT0 CLEAR
BEQ TST11 ;BR IF CLEAR
BIC #BIT0,@TCSR ;CLEAR BIT0, TO PRINT ERROR
ERROR 14 ;RESET DID NOT CLEAR BIT0 OF TCSR

```

# H03

MAIN. MACY11 27(732)  
DZDLDA.P11 T10

02-NOV-76 16:15 PAGE 24  
TEST THAT BIT0(BREAK BIT) CAN BE SET & CLEARED & RESET

SEQ 0033

```

1087
1088
1089
1090          ::*****
1091          ::#TEST 11      TEST THAT BIT2(MAINT. BIT) CAN BE SET & RESET
1092          ::*****
1093          TST11: SCOPE
1094          RESET          ;CLEAR EVERYTHING
1095          BIT          #BIT2,@TCSR ;TEST FOR BIT2 OF TCSR CLEAR
1096          BEQ          3$          ;BR IF CLEAR
1097          TST          CTSTFL     ;CHECK IF DEVICE IS CONSOLE
1098          BNE          1$          ;IF YES, SKIP ERROR TYPEOUT
1099          ERROR       15          ;BIT2 OF TCSR NOT CLEAR AFTER RESET
1100          BR          3$
1101
1102          004410          1$:
1103          004410          004767 006102 JSR          PC,@ATY4          ;: ONLY REPORT A FATAL ERROR
1104          004414          000015          ;: THE ERROR NUMBER (FROM APT LIST)
1105          004416          000000          2$:
1106          HALT
1107          004420          052777 000004 175664 3$:
1108          004426          032777 000004 175656 BIS          #BIT2,@TCSR ;SET BIT2 OF TCSR
1109          004434          001001 BIT          #BIT2,@TCSR ;TEST FOR BIT2 SET
1110          ERROR       16          ;BR IF SET
1111          004436          104016 ERROR       16          ;BIT2 OF TCSR WILL NOT SET
1112
1113          004440          042777 000004 175644 4$:
1114          004446          032777 000004 175636 BIC          #BIT2,@TCSR ;CLEAR BIT2 OF TCSR
1115          004454          001411 BIT          #BIT2,@TCSR ;TEST BIT2 CLEAR
1116          BEQ          7$          ;BR IF CLEAR
1117          004456          005767 175614 TST          CTSTFL     ;CHECK IF DEVICE IS CONSOLE
1118          004462          001002 BNE          5$          ;IF YES, SKIP ERROR TYPEOUT
1119          004464          104017 ERROR       17
1120          004466          000404 BR          7$
1121          004470          004767 006022 5$:
1122          004470          004767 006022 JSR          PC,@ATY4          ;: ONLY REPORT A FATAL ERROR
1123          004474          000017          ;: THE ERROR NUMBER (FROM APT LIST)
1124          004476          000000          6$:
1125          HALT
1126          004500          052777 000004 175604 7$:
1127          004506          000005 BIS          #BIT2,@TCSR ;SET BIT2 OF TCSR
1128          004510          032777 000004 175574 RESET        ;CLEAR BIT2 WITH RESET
1129          004516          001404 BIT          #BIT2,@TCSR ;TEST FOR BIT2 CLEAR
1130          BEQ          TST12     ;IF CLEAR, GO TO NEXT TEST
1131          004520          042777 000004 175564 BIC          #BIT2,@TCSR ;CLEAR BIT2, TO PRINT ERROR
1132          004526          104020 ERROR       20
1133          ;RESET DID NOT CLEAR BIT2 OF TCSR

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1134
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1136
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1138
1139 004530 000004
1140 004532 000005
1141 004534 017703 175562
1142 004540 012777 004570 175554
1143 004546 004767 005016
1144 004552 000340
1145 004554 032777 000100 175530
1146 004562 001404
1147 004564 104021
1148
1149 004566 000402
1150
1151 004570 022626 15:
1152 004572 104022          CMP      (SP)+,(SP)+
1153
1154
1155 004574 052777 000100 175510 25:
1156 004602 032777 000100 175502          BIS      #BIT6,@TCSR
1157 004610 001001          BIT      #BIT6,@TCSR
1158
1159 004612 104023          BNE      35
1160
1161
1162 004614 042777 000100 175470 35:
1163 004622 032777 000100 175462          BIC      #BIT6,@TCSR
1164 004630 001401          BIT      #BIT6,@TCSR
1165 004632 104024          BEQ      45
1166
1167
1168 004634 052777 000100 175450 45:
1169 004642 000005          ERROR   23
1170 004644 032777 000100 175440          ;CANNOT SET BIT6 OF TCSR
1171 004652 001401          BIC      #BIT6,@TCSR
1172
1173 004654 104025          BIT      #BIT6,@TCSR
1174
1175 004656 010377 175440 55:          BEQ      55
          MOV      R3,@TVECT          ;SET BIT6 OF TCSR
          ;CLEAR BIT6 WITH RESET
          ;TEST BIT6 OF TCSR
          ;BR IF CLEAR
          ;CANNOT CLEAR BIT6 OF TCSR WITH RESET
          ;RESTORE XMIT VECTOR

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1176
1177
1178
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1181 004662 000004
1182 004664 000005
1183 004666 017703 175424
1184 004672 012777 004722 175416
1185 004700 004767 004664
1186 004704 000340
1187 004706 032777 000100 175372
1188 004714 001404
1189 004716 104026
1190
1191 004720 000402
1192
1193 004722 022626 1S:
1194 004724 104027
1195
1196
1197 004726 052777 000100 175352 2S:
1198 004734 032777 000100 175344
1199 004742 001001
1200
1201 004744 104030
1202
1203
1204 004746 042777 000100 175332 3S:
1205 004754 032777 000100 175324
1206 004762 001401
1207
1208 004764 104031
1209
1210
1211 004766 052777 000100 175312 4S:
1212 004774 000005
1213 004776 032777 000100 175302
1214 005004 001401
1215
1216 005006 104032
1217
1218 005010 010377 175302 5S:
1219

```

```

*****
;TEST 13 TEST THAT BIT6 OF RCSR CAN BE SET & RESET
*****
TST13: SCOPE
RESET ;CLEAR EVERYTHING
MOV @RVECT,R3 ;SAVE RECEIVE VECTOR
MOV #15,@RVECT ;SET UP INTERRUPT VECTOR FOR ERROR REPORT
JSR PC,@RPSW ;SET PSM TO PRIORITY=7
;WORD 340
BIT #BIT6,@RCSR ;TEST BIT6 OF RCSR
BEQ 25
ERROR 26
;BIT6 OF RCSR NOT CLEAR AFTER RESET
BR 25
1S: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 27
;RCVR INTERRUPT WITH PRIORITY=7
2S: BIS #BIT6,@RCSR ;SET BIT6 OF RCSR
BIT #BIT6,@RCSR ;TEST BIT6 OF RCSR
BNE 35 ;BR, IF SET
ERROR 30
;CANNOT SET BIT6 OF RCSR
3S: BIC #BIT6,@RCSR ;CLEAR BIT6 OF RCSR
BIT #BIT6,@RCSR ;TEST BIT6 OF RCSR
BEQ 45 ;BR, IF CLEAR
ERROR 31
;CANNOT CLEAR BIT6 OF RCSR
4S: BIS #BIT6,@RCSR ;SET BIT6 OF RCSR
RESET ;CLEAR BIT6 OF RCSR WITH RESET
BIT #BIT6,@RCSR ;TEST BIT6 OF RCSR
BEQ 55 ;BR, IF CLEAR
ERROR 32
;CANNOT CLEAR BIT6 OF RCSR WITH RESET
5S: MOV R3,@RVECT ;RESTORE RECEIVE VECTOR

```

# K03

```

1220
1221
1222
1223
1224 005014 000004
1225 005016 005767 175254
1226 005022 001460
1227 005024 032777 000100 174006
1228 005032 001054
1229 005034 000005
1230 005036 017703 175306
1231 005042 012777 005072 175300
1232 005050 004767 004514
1233 005054 000340
1234 005056 032777 000100 175262
1235 005064 001404
1236 005066 104033
1237
1238 005070 000402
1239
1240 005072 022626 1$:
1241 005074 104034 ERROR (SP)+,(SP)+
1242
1243
1244 005076 052777 000100 175242 2$:
1245 005104 032777 000100 175234 BIT #BIT6,2LKS
1246 005112 001001 BNE 35 ;SET BIT6 OF LKS
1247 ;TEST BIT6 OF LKS
1248 005114 104035 ERROR 35 ;BR IF SET
1249 ;CANNOT SET BIT6 OF LKS
1250
1251 005116 042777 000100 175222 3$:
1252 005124 032777 000100 175214 BIC #BIT6,2LKS
1253 005132 001401 BIT #BIT6,2LKS
1254 005134 104036 BEG 45 ;CLEAR BIT6 OF LKS
1255 ;TEST BIT6 OF LK
1256 005136 052777 000100 175202 4$:
1257 005144 000005 RESET 45 ;CANNOT CLEAR BIT6 OF LKS
1258 005146 032777 000100 175172 BIT #BIT6,2LKS ;SET BIT6 OF LKS
1259 005154 001401 BEG 55 ;CLEAR BIT6 OF LKS WITH RESET
1260 ;TEST BIT6 OF LKS
1261 ;BR IF CLEAR
1262
1263 005160 010377 175164 5$:
MOV R3,2RTCVT ;CANNOT CLEAR BIT6 OF LKS WITH RESET
;RESTORE LINE CLOCK VECTOR
  
```

```

1264
1265
1266
1267
1268
1269 005164 000004
1270 005166 013703 000004
1271 005172 013704 000006
1272 005176 012737 005250 000004
1273 005204 012737 000340 000006
1274 005212 000005
1275 005214 012700 000002
1276 005220 016767 175062 173574 1$:
1277 005226 040067 173570
1278 005232 026767 175050 173562
1279 005240 001415
1280 005242 052777 000100 173552
1281 005250 032777 000100 175030 2$:
1282 005256 001014
1283 005260 022706 001000
1284 005264 001003
1285 005266 042777 000100 173526
1286 005274 012706 001000 3$:
1287 005300 006300
1288 005302 005700
1289 005304 001345
1290 005306 000403
1291
1292 005310 012706 001000 4$:
1293 005314 104040
1294 005316 010337 000004
1295 005322 010437 000006 5$:

: *****
: *TEST 15 TEST THAT REGISTERS CAN NOT BE ADDRESSES AS ANYTHING BUT 17XXXX
: *****
TST15: SCOPE
MOV 2#4,R3 ;SAVE TIMEOUT VECTOR
MOV 2#6,R4 ;SAVE TIMEOUT PSW
MOV 2#2,2#4 ;SET UP TIMEOUT VECTOR
MOV 2#340,2#6 ;KEEP PRIO=7
RESET ;CLEAR EVERYTHING
MOV #BIT1,R0 ;SET UP BIT MASK
MOV RCSR,$BDADR ;MOVE GOOD RCSR ADDRESS INTO TEST ADDRESS
BIC R0,$BDADR ;CREATE BAD ADDRESS BY COMPLEMENTING ONE BIT
CMP RCSR,$BDADR ;ARE ADDRESSES IDENTICAL\
BEQ 3$ ;IF YES, DO NOT TEST THIS ADDRESS
BIS #BIT6,2$BDADR ;SET BIT6 USING BAD ADDRESS
BIT #BIT6,2$RCSR ;CHECK TO SEE IF GOOD ADDRESS CONTAINS BIT6
BNE 4$ ;BR IF SET ---> ERROR
CMP #1000,SP ;DID TEST CAUSE A TIMEOUT?
BNE 3$ ;IF YES, SKIP RESTORE OF MEMORY
BIC #BIT6,2$BDADR ;RESTORE ANY MEMORY LOCATION THAT WAS ALTERED
MOV #1000,SP ;RESTORE SP IN CASE A TIMEOUT OCCURRED
ASL R0 ;SHIFT BIT MASK TO NEXT POSITION
TST R0 ;COMPLEMENTED ALL BITS FROM 1 - 15?
BNE 1$ ;BR, IF NOT
BR 5$ ;BR TO NEXT TEST

;RESET STACK PIONTER
MOV #1000,SP
ERROR 40
MOV R3,2#4 ;RESTORE TIMEOUT VECTOR
MOV R4,2#6 ;RESTORE TIMEOUT PSW
  
```

# M03

.MAIN. MACY11 27(732)  
DZDLDA.P11 T15

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TEST THAT REGISTERS CAN NOT BE ADDRESSES AS ANYTHING BUT 17XXXX

SEQ 0038

```
1296
1297
1298
1299
1300
1301 005326 000004
1302 005330 005767 174742
1303 005334 001431
1304 005336 032777 000100 173474
1305 005344 001025
1306 005346 000005
1307 005350 000240
1308 005352 105777 174770 1S:
1309 005356 100401
1310 005360 104041
1311 005362 042777 000200 174756 2S:
1312 005370 032777 000200 174750
1313 005376 001401
1314
1315 005400 104042
1316
1317 005402 005000
1318 005404 105777 174736 3S:
1319 005410 100403
1320 005412 005200
1321 005414 001373
1322
1323 005416 104043
1324
```

```

*****
;TEST 16 TEST THAT BIT7 OF LKS SETS & CAN BE CLEARED
*****
TST16: SCOPE
TST CTSTFL ; IS CONSOLE UNDER TEST?
BEQ TST17 ; IF NOT, SKIP THIS TEST
BIT #BIT6, 2SWR ; ARE LINE CLOCK TESTS INHIBITED?
BNE TST17 ; IF YES, SKIP THIS TEST
RESET ; CLEAR EVERYTHING & SET BIT7 OF LKS
NOP
TSTB 2LKS ; TEST FOR BIT7 OF LKS
BMI 2S ; BR IF SET
ERROR 41 ; BIT7 OF LKS DID NOT SET WITH RESET
BIC #BIT7, 2LKS ; CLEAR BIT7 OF LKS
BIT #BIT7, 2LKS ; TEST BIT7 OF LKS
BEQ 3S
ERROR 42
; CAN NOT CLEAR BIT7 OF LKS
CLR R0 ; CLEAR TIMER
TSTB 2LKS ; TEST FOR BIT7 OF LKS
BMI TST17 ; BR IF SET
INC R0 ; INCREMENT TIMER
BNE CONT ; CONTINUE UNTIL TIME EXPIRES
ERROR 43 ; BIT7 OF LKS DOES NOT SET
```

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1325
1326
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1328
1329 005420 000004
1330 005422 005767 174650
1331 005426 001477
1332 005430 032777 000100 173402
1333 005436 001073
1334 005440 004767 004124
1335 005444 000340
1336 005446 017703 174676
1337 005452 012777 005514 174670
1338 005460 012777 000340 174664
1339 005466 052777 000100 174652
1340 005474 042777 000200 174644
1341 005502 105777 174640 15:
1342 005506 100375
1343 005510 000240
1344 005512 000402
1345
1346 005514 022626 25:
1347 005516 104044
1348
1349 005520 005077 174622 35:
1350 005524 012777 005552 174616
1351 005532 004767 004032
1352 005536 000240
1353 005540 105777 174602 205:
1354 005544 100375
1355 005546 000240
1356 005550 000402
1357
1358 005552 022626 45:
1359 005554 104045
1360
1361 005556 012777 005612 174564 55:
1362 005564 052777 000100 174554
1363 005572 042777 000200 174546
1364 005600 105777 174542 65:
1365 005604 100375
1366 005606 000240
1367
1368 005610 104046
1369
1370 005612 022626 75:
1371 005614 042777 000100 174524
1372 005622 010377 174522
1373
1374

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*****
: *TEST 17 TEST THAT THE REAL TIME CLOCK INTERRUPTS PROPERLY
*****
TST17: SCOPE
TST CTSTFL ; IS CONSOLE UNDER TEST?
BEQ TST20 ; IF NOT, SKIP THIS TEST
BIT #BIT6,JSWR ; ARE LINE CLOCK TESTS INHIBITED?
BNE TST20 ; IF YES, SKIP THIS TEST
JSR PC,WRPSW ; SET PSM TO PRIORITY 7
.WORD 340
MOV #25,RTCVT R3 ; SAVE LINE CLOCK VECTOR
MOV #340,RTCP SW ; SET RTC INTERRUPT VECTOR TO ERROR REPORT
BIS #BIT6,ALKS ; KEEP PRIORITY AT 7
BIC #BIT7,ALKS ; SET INTERRUPT ENABLE
TSTB ALKS ; CLEAR CLOCK DONE FLAG
BPL 15 ; WAIT FOR RTC DONE (INTERRUPT REQUEST)
NOP ; GIVE TIME FOR ANY INTERRUPTS
BR 35 ; BR, IF NO INTERRUPT OCCURS

25: CMP (SP)+,(SP)+ ; RESTORE SP AFTER INTERRUPT
ERROR 44 ; RTC INTERRUPTS AT PRIORITY 7

35: CLR ALKS ; DISABLE RTC INTERRUPTS & CLEAR DONE
MOV #45,RTCVT ; SET RTC INTERRUPT VECTOR FOR ERROR
JSR PC,WRPSW ; CHANGE PSM TO PRIORITY 5
.WORD 240
TSTB ALKS ; WAIT FOR DONE (INTERRUPT REQUEST)
BPL 205
NOP ; GIVE TIME FOR ANY INTERRUPT
BR 55 ; IF NO INTERRUPT - BR TO CONTINUE TEST

45: CMP (SP)+,(SP)+ ; RESTORE SP AFTER INTERRUPT
ERROR 45 ; RTC INTERRUPTS WITH INTERRUPTS DISABLED

55: MOV #75,RTCVT ; POINT RTC VECTOR TO END OF TEST
BIS #BIT6,ALKS ; ALLOW INTERRUPTS
BIC #BIT7,ALKS ; CLEAR CLOCK DONE FLAG
TSTB ALKS ; WAIT FOR RTC DONE
BPL 65
NOP ; GIVE TIME FOR INTERRUPT

65: ERROR 46 ; RTC INTERRUPT DID NOT OCCUR

75: CMP (SP)+,(SP)+ ; RESTORE SP AFTER INTERRUPT
BIC #BIT6,ALKS ; DISABLE INTERRUPTS
MOV R3,RTCVT ; RESTORE LINE CLOCK VECTOR

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1375  
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1400  
1401  
1402  
1403  
1404  
1405  
1406  
1407  
1408  
1409  
1410  
1411  
1412

005626 000004  
005630 005767 174442  
005634 001453  
005636 032777 000100 173174  
005644 001047  
005646 000005  
005650 017703 174474  
005654 012777 005724 174466  
005662 012777 000340 174462  
005670 004767 003674  
005674 000240  
005676 052777 000100 174442  
005704 042777 000200 174434  
005712 105777 174430  
005716 100375  
005720 000240  
005722 104047  
005724 022626  
005726 012777 005746 174414  
005734 004767 003630  
005740 000240  
005742 000240  
005744 000402  
005746 022626  
005750 104050  
005752 042777 000100 174366  
005760 010377 174364

```
*****  
: TEST 20 TEST RTC FOR DOUBLE INTERRUPTS  
*****  
TST20: SCOPE  
TST CTSTFL ; IS CONSOLE UNDER TEST?  
BEQ TST21 ; IF NOT, SKIP THIS TEST  
BIT #BIT6,PSW ; ARE LINE CLOCK TESTS INHIBITED?  
BNE TST21 ; IF YES, SKIP THIS TEST  
RESET ; CLEAR EVERYTHING  
MOV #R3,RTCVT ; SAVE LINE CLOCK VECTOR  
MOV #25,RTCVT ; SET UP RTC INTERRUPT VECTOR  
MOV #340,RTCPWM ; DISALLOW INTERRUPTS AFTER THE INTERRUPT  
JSR PC,RTCPWM ; SET PRIORITY TO 5  
; .WORD 240  
BIS #BIT6,ALKS ; ENABLE CLOCK INTERRUPTS  
BIC #BIT7,ALKS ; CLEAR CLOCK DONE FLAG  
1S: TSTB ALKS ; WAIT FOR DONE  
BPL 1S  
NOP ; GIVE TIME FOR ANY INTERRUPT  
ERROR 47 ; RTC INTERRUPT DID NOT OCCUR  
2S: CMP (SP)+,(SP)+ ; RESTORE SP AFTER INTERRUPT  
MOV #35,RTCVT ; POINT RTC VECTOR TO ERROR REPORT  
JSR PC,RTCPWM ; SET PSM TO PRIORITY 5  
; .WORD 240  
NOP ; GIVE SOME TIME FOR AN INTERRUPT  
BR 4S ; NO INTERRUPT - BR TO END OF TEST  
3S: CMP (SP)+,(SP)+ ; RESTORE SP AFTER INTERRUPT  
ERROR 50 ; INTERRUPT SEQUENCE DID NOT CLEAR  
; INTERRUPT REQUEST  
4S: BIC #BIT6,ALKS ; DISABLE CLOCK INTERRUPTS  
MOV R3,RTCVT ; RESTORE LINE CLOCK VECTOR
```

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1413
1414
1415
1416
1417
1418 005764 000004
1419 005766 005767 174304
1420 005772 001442
1421 005774 032777 000100 173036
1422 006002 001036
1423 006004 004767 003560
1424 006010 000340
1425 006012 017703 174332
1426 006016 012777 006070 174324
1427 006024 052777 000100 174314
1428 006032 042777 000200 174306
1429 006040 105777 174302 1$: TSTB 2LKS
1430 006044 100375
1431 006046 000005
1432 006050 004767 003514 JSR PC,WRPSW
1433 006054 000240 .WORD 240
1434 006056 000240
1435 006060 042777 000100 174260 NOP
1436 006066 000402 BIC #BIT6,2LKS
1437 BR 3$
1438 006070 022626 2$: CMP (SP)+,(SP)+
1439 006072 104051 ERROR 51
1440
1441 006074 010377 174250 3$: MOV R3,2RTCVT

```

```

:*****
:TEST 21 TEST THAT INTERRUPT CLEARS WITH RESET
:*****
:IS CONSOLE UNDER TEST?
:IF NOT, SKIP THIS TEST
:ARE LINE CLOCK TESTS INHIBITED?
:IF YES, SKIP THIS TEST
:SET PRIORITY TO 7
:SAVE LINE CLOCK VECTOR
:POINT RTC VECTOR TO ERROR REPORT
:ENABLE CLOCK INTERRUPTS
:CLEAR CLOCK DONE FLAG
:WAIT FOR DONE (INTERRUPT REQUEST)
:CLEAR PENDING INTERRUPT WITH RESET
:SET PRIORITY TO 5
:GIVE TIME FOR ANY INTERRUPT
:DISALLOW INTERRUPTS
:BR TO END OF TEST
:RESTORE SP AFTER INTERRUPT
:RESET DID NOT CLEAR INTERRUPT
:RESTORE LINE CLOCK VECTOR

```

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1442
1443
1444
1445
1446
1447 006100 000004
1448 006102 005767 174170
1449 006106 001444
1450 006110 032777 000100 172722
1451 006116 001040
1452 006120 004767 003444
1453 006124 000340
1454 006126 017703 174216
1455 006132 012777 006210 174210
1456 006140 052777 000100 174200
1457 006146 042777 000200 174172
1458 006154 105777 174166 1S: TSTB 2LKS
1459 006160 100375
1460 006162 042777 000200 174156
1461 006170 004767 003374
1462 006174 000240
1463 006176 000240
1464 006200 042777 000100 174140
1465 006206 000402
1466
1467
1468 006210 022626 2S: CMP (SP)+,(SP)+
1469 006212 104052 ERROR 52
1470
1471 006214 010377 174130 3S: MOV R3,2RTCVT

```

```

*****
*TEST 22 TEST THAT RTC INTERRUPT CLEARS BY CLEARING BIT7 OF LKS
*****
TST22: SCOPE
TST CTSTFL ;IS CONSOLE UNDER TEST?
BEQ TST23 ;IF NOT, SKIP THIS TEST
BIT 2,2SMR ;ARE LINE CLOCK TESTS INHIBITED?
BNE TST23 ;IF YES, SKIP THIS TEST
JSR PC,WRPSW ;SET PRIORITY TO 7
.WORD 340
MOV 2RTCVT,R3 ;SAVE LINE CLOCK VECTOR
MOV 2S,2RTCVT ;POINT RTC VECTOR TO ERROR REPORT
BIS 2,2LKS ;ENABLE CLOCK INTERRUPTS
BIC 2,2LKS ;CLEAR CLOCK DONE FLAG
TSTB 2LKS ;WAIT FOR DONE (INTERRUPT REQUEST)
BFL 1S
BIC 2,2LKS ;CLEAR DONE & INTERRUPT
JSR PC,WRPSW ;ALLOW INTERRUPTS
.WORD 240
NOP ;GIVE TIME FOR ANY INTERRUPT
BIC 2,2LKS ;DISALLOW INTERRUPTS
BR 3S ;BR TO END OF TEST

2S: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 52 ;CLEARING BIT7 OF LKS DID NOT CLEAR INTERRUPT

3S: MOV R3,2RTCVT ;RESTORE LINE CLOCK VECTOR

```

# E04

.MAIN. MACY11 27(732)  
DZDLDA.P11 T22

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TEST THAT RTC INTERRUPT CLEARS BY CLEARING BIT7 OF LKS

SEQ 0043

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1472
1473
1474
1475
1476
1477 006220 000004
1478 006222 005767 174050
1479 006226 001452
1480 006230 032777 000100 172602
1481 006236 001046
1482
1483 006240 005000
1484 006242 012701 177777
1485 006246 005002 1S:
1486 006250 005077 174072
1487 006254 105777 174066 2S:
1488 006260 100375
1489 006262 005077 174060
1490 006266 105777 174054 3S:
1491 006272 100003
1492 006274 005202
1493 006276 005077 174044
1494 006302 005200 4S:
1495 006304 001370
1496 006306 005201
1497 006310 001003
1498 006312 010267 000032
1499 006316 000753
1500 006320 016701 000024  CMPARE:
1501 006324 160201
1502 006326 100001
1503 006330 005401
1504 006332 020127 000000  TOLER:
1505 006336 003406
1506
1507 006340 010267 000006
1508 006344 104053
1509
1510 006346 000402
1511 006350 000000
1512 006352 000000

*****
*TEST 23 TEST CLOCK REPEATABILITY
*****
TST23: SCOPE
TST CTSTFL ; IS CONSOLE UNDER TEST?
BEQ TST24 ; IF NOT, SKIP THIS TEST
BIT #BIT6,2SWR ; ARE LINE CLOCK TESTS INHIBITED?
BNE TST24 ; IF YES, SKIP THIS TEST

CLR R0 ; CLEAR A TIMER
MOV #1,R1 ; SET A FLAG INDICATING FIRST PASS THRU THIS LOOP
1S: CLR R2 ; CLEAR CLOCK COUNTER
CLR #LKS ; CLEAR DONE
TSTB #LKS ; SYNC ON DONE
BPL 2S
CLR #LKS ; CLEAR DONE
3S: TSTB #LKS ; IS CLOCK DONE?
BPL 4S ; BR IF NOT, TO INCREMENT TIMER
INC R2 ; IF DONE, INCREMENT CLOCK COUNT
CLR R0 ; CLEAR DONE
4S: INC R0 ; INCREMENT TIMER
BNE 3S ; BR IF TIME REMAINS
INC R1 ; INCREMENT LOOP PASS FLAG
BNE CMPARE ; BR IF TWO PASSES HAVE BEEN MADE
MOV R2,FIRST ; IF NOT, STORE FIRST CLOCK COUNT
BR 1S ; DO LOOP AGAIN
CMPARE: MOV FIRST,R1 ; RECALL FIRST CLOCK COUNT
SUB R2,R1 ; CALCULATE DIFFERENCE OF TWO COUNTS
BPL TOLER ; IF POSITIVE, SKIP NEGATION OF DIFFERENCE
NEG R1 ; MAKE DIFFERENCE A POSITIVE NUMBER
TOLER: CMP R1,#0 ; COMPARE DIFFERENCE WITH DESIRED TOLERANCE
BLE TST24 ; BR, IF LOWER/EQUAL TO TOLERANCE

MOV R2,SECND ; STORE SECOND COUNT
ERROR 53 ; CLOCK REPEATABILITY ERROR

BR TST24
FIRST: .WORD 0
SECND: .WORD 0

```

```

1513
1514
1515
1516
1517
1518 006354 000004
1519 006356 042777 000100 173726
1520 006364 105777 173722
1521 006370 100375
1522 006372 017703 173724
1523 006376 012777 006420 173716
1524 006404 005077 173714
1525 006410 004767 003154
1526 006414 000140
1527 006416 000402
1528
1529 006420 022626 2S:
1530 006422 104054 ERROR 54
1531
1532 006424 012777 006444 173670 3S:
1533 006432 052777 000100 173652 MOV #45, @TVECT
1534 006440 000240 BIS #BIT6, @TCSR
1535
1536 006442 104055 ERROR 55
1537
1538 006444 042777 000100 173640 4S:
1539 006452 022626 CMP (SP)+, (SP)+
1540 006454 010377 173642 MOV R3, @TVECT
1541
  
```

```

*****
: TEST 24 TEST THAT XMIT INTERRUPTS ONLY WHEN ENABLED
*****
TST24: SCOPE
BIC #BIT6, @TCSR ; CLEAR TRANSMIT INTERRUPT ENABLE
1S: TSTB @TCSR ; WAIT FOR DONE
BPL 1S
MOV @TVECT, R3 ; SAVE XMIT VECTOR
MOV #25, @TVECT ; POINT XMIT VECTOR TO ERROR REPORT
CLR @TPSW
JSR PC, WPPSW ; SET PSW TO PRIORITY 3
WORD 140
BR 3S
2S: CMP (SP)+, (SP)+ ; RESTORE SP AFTER INTERRUPT
ERROR 54
3S: MOV #45, @TVECT ; XMIT INTERRUPTS WITH INTERRUPT ENABLE CLEAR
BIS #BIT6, @TCSR ; SET XMIT VECTOR TO END OF TEST
NOP ; ENABLE INTERRUPTS
ERROR 55 ; XMIT DID NOT INTERRUPT
4S: BIC #BIT6, @TCSR ; DISABLE INTERRUPTS
CMP (SP)+, (SP)+ ; RESTORE SP AFTER INTERRUPT
MOV R3, @TVECT ; RESTORE XMIT VECTOR
  
```

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1542
1543
1544
1545
1546 006460 000004
1547 006462 042777 000100 173622
1548 006470 004767 003074
1549 006474 000340
1550 006476 017703 173620
1551 006502 012777 006530 173612
1552 006510 105777 173576
1553 006514 100375
1554 006516 052777 000100 173566
1555 006524 000240
1556 006526 000402
1557
1558 006530 022626
1559 006532 104056
1560
1561 006534 042777 000100 173550
1562 006542 012777 006562 173552
1563 006550 004767 003014
1564 006554 000140
1565 006556 000240
1566 006560 000402
1567
1568 006562 022626
1569 006564 104057
1570
1571 006566 010377 173530

```

```

*****
: TEST 25 TEST THAT XMIT INTERRUPTS DO NOT OCCUR WHEN DISABLED
*****
TST25: SCOPE
      BIC  #BIT6,ATCSR ;DISABLE INTERRUPTS
      JSR  PC,WRPSW    ;SET PSM TO PRIORITY 7
              .WORD 340
      MOV  ATVECT,R3   ;SAVE XMIT VECTOR
      MOV  #25,ATVECT ;POINT XMIT VECTOR TO ERROR REPORT
1S:    TSTB ATCSR      ;WAIT FOR DONE
      BPL  1$
      BIS  #BIT6,ATCSR ;ENABLE INTERRUPT
      NOP
      BR   3$         ;CONTINUE TEST
2S:    CMP  (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
      ERROR 56
3S:    BIC  #BIT6,ATCSR ;XMIT INTERRUPTS AT PRIORITY=7
      MOV  #45,ATVECT  ;CLEAR INTERRUPT ENABLE
      JSR  PC,WRPSW    ;POINT XMIT VECTOR TO ERROR REPORT
              .WORD 140
      NOP
      BR   5$         ;BR TO END OF TEST-NO INTERRUPT
4S:    CMP  (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
      ERROR 57
5S:    MOV  R3,ATVECT  ;XMIT INTERRUPT OCCURES WITH BIT6 CLEAR
              ;RESTORE XMIT VECTOR

```

```

1572
1573
1574
1575
1576
1577 006572 000004
1578 006574 042777 000100 173510
1579 006602 017703 173514
1580 006606 012777 006642 173506
1581 006614 004767 002750
1582 006620 000140
1583 006622 105777 173464 1S: TSTB @TCSR ;WAIT FOR DONE
1584 006626 100375
1585 006630 052777 000100 173454
1586 006636 000240
1587
1588 006640 104060 ERROR 60
1589
1590 006642 022626 2S: CMP (SP)+,(SP)+ ;XMIT INTERRUPT DID NOT OCCUR
1591 006644 012777 006664 173450 MOV @-S,@TVECT ;RESTORE SP AFTER INTERRUPT
1592 006652 000240 NOP ;POINT XMIT VECTOR TO ERROR
1593 006654 042777 000100 173430 BIC @BIT6,@TCSR ;DISABLE INTERRUPTS
1594 006662 000402 BR 5S ;BR TO END OF TEST
1595
1596 006664 022626 4S: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
1597 006666 104061 ERROR 61
1598
1599 006670 010377 173426 5S: MOV R3,@TVECT ;XMIT RE-INTERRUPTED
;RESTORE XMIT VECTOR
1600
1601
1602
1603
1604 006674 000004
1605 006676 042777 000100 173406
1606 006704 004767 002660
1607 006710 000340
1608 006712 052777 000100 173372
1609 006720 017703 173376
1610 006724 012777 006770 173370
1611 006732 005077 173356
1612 006736 105777 173350 1S: TSTB @TCSR ;WAIT FOR DONE (INTERRUPT)
1613 006742 100375 BPL 1S
1614 006744 005077 173344 CLR @TBUF ;FILL SECOND BUFFER TO RESET INT.
1615 006750 004767 002614 JSR PC,@RPSW ;ALLOW INTERRUPTS
1616 006754 000140 .WORD 140
1617 006756 000240 NOP
1618 006760 042777 000100 173324 BIC @BIT6,@TCSR ;DISABLE INTERRUPTS
1619 006766 000402 BR 3S ;BR TO END OF TEST
1620
1621 006770 022626 2S: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
1622 006772 104062 ERROR 62
1623
1624 006774 010377 173322 3S: MOV R3,@TVECT ;LOADING TBUF DID NOT CLEAR INTERRUPT.
;RESTORE XMIT VECTOR
1625

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1626
1627
1628
1629
1630 007000 000004
1631 007002 000005
1632 007004 052777 000004 173300
1633 007012 005077 173276
1634 007016 005000
1635 007020 032777 004000 173260 WACTV:
1636 007026 001006
1637 007030 005200
1638 007032 001372
1639 007034 042777 000004 173250
1640
1641 007042 104063
1642
1643 007044 005000
1644 007046 105777 173234
1645 007052 100406
1646 007054 005200
1647 007056 001373
1648 007060 042777 000004 173224
1649 007066 104064
1650
1651
1652 007070 032777 004000 173210 3S:
1653 007076 001404
1654 007100 042777 004000 173200
1655 007106 104065
1656
1657
1658 007110 000005
1659 007112 105777 173170
1660 007116 001404
1661
1662 007120 042777 000004 173164
1663 007126 104066
1664
1665
1666 007130 042777 000004 173150 5S:
1667 007136 000400

```

```

*****
:TEST 30 TEST THAT RCVR ACTIVE (BIT11) OF RCSR SETS WHILE RECEIVING
*****
TST30: SCOPE
RESET
BIS #BIT2, @TCSR ;CLEAR EVERYTHING
CLR @TBUF ;SET MAINTENANCE WRAP
CLR RO ;LOAD TRANSMIT BUFFER
BIT #BIT11, @RCSR ;CLEAR A TIMER
BNE 2S ;TEST RCVR ACTIVE BIT
INC RO ;BR IF SET
BNE WACTV ;INCREMENT TIMER IF NOT SET
BIC #BIT2, @TCSR ;CONTINUE WAIT IF TIME REMAINS
;CLEAR MAINTENANCE BIT

ERROR 63 ;RCVR ACTIVE DID NOT SET WHILE RECEIVING

2S:
WDONE: CLR RO ;CLEAR TIMER
TSTB @RCSR ;CHECK FOR RECEIVER DONE
BMI 3S ;BR IF DONE
INC RO ;INCREMENT TIMER, IF NOT DONE
BNE WDONE ;CONTINUE WAIT IF TIME REMAINS
BIC #BIT2, @TCSR ;CLEAR MAINTENANCE BIT
ERROR 64 ;RECEIVER DONE NEVER SET

3S: BIT #BIT11, @RCSR ;CHECK FOR RCVR ACTIVE CLEAR
BEQ 4S ;BR IF CLEAR
BIC #BIT11, @RCSR ;CLEAR MAINTENANCE BIT
ERROR 65 ;RCVR ACTIVE DID NOT CLEAR WITH RCVR DONE

4S: RESET ;CLEAR DONE WITH RESET
TSTB @RCSR ;CHECK FOR DONE CLEAR
BEQ 5S

BIC #BIT2, @TCSR ;CLEAR MAINTENANCE BIT
ERROR 66 ;RESET DID NOT CLEAR RCVR DONE

5S: BIC #BIT2, @RCSR ;CLEAR MAINTENANCE BIT
BR TST31 ;BR TO NEXT TEST

```

# J04

```

1668
1669
1670
1671
1672
1673 007140 000004
1674 007142 000005
1675 007144 052777 000004 173140
1676 007152 005077 173136
1677 007156 105777 173124
1678 007162 100375
1679 007164 052777 000001 173114
1680 007172 105777 173110
1681 007176 001404
1682 007200 042777 000004 173104
1683 007206 104067
1684
1685
1686
1687
1688
1689
1690
1691 007210 000004
1692 007212 000005
1693 007214 052777 000004 173070
1694 007222 005077 173066
1695 007226 105777 173054
1696 007232 100375
1697 007234 017700 173050
1698 007240 042777 000004 173044
1699 007246 105777 173034
1700 007252 001401
1701 007254 104070
1702

:*****
:TEST 31 TEST THAT RDR ENABLE CLEARS RECEIVER DONE FLAG
:*****
TST31: SCOPE
        RESET
        BIS #BIT2,@TCSR ;CLEAR EVERYTHING
        CLR @TBUF ;SET MAINTENANCE WRAP
        TSTB @RCSR ;LOAD TRANSMITTER
        BPL IS ;WAIT FOR RECEIVER DONE
        BIS #BIT0,@RCSR ;CLEAR DONE BY SETTING RDR ENABLE
        TSTB @RCSR ;CHECK FOR DONE CLEAR
        BEQ TST32 ;BR, IF CLEAR TO NEXT TEST
        BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
        ERROR 67 ;SETTING RDR ENABLE DID NOT CLEAR RCVR DONE

:*****
:TEST 32 TEST THAT READING RBUF CLEARS RECEIVER DONE
:*****
TST32: SCOPE
        RESET
        BIS #BIT2,@TCSR ;CLEAR EVERYTHING
        CLR @TBUF ;SET MAINTENANCE WRAP
        TSTB @RCSR ;LOAD TRANSMITTER
        BPL IS ;WAIT FOR RECEIVER DONE
        MOV @RBUF,R0 ;READ RECEIVE BUFFER
        BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
        TSTB @RCSR ;CHECK FOR RECEIVE DONE CLEAR
        BEQ TST33 ;BR, IF CLEAR TO NEXT TEST
        ERROR 70 ;READING RBUF DID NOT CLEAR RCVR DONE
  
```

```

1703
1704
1705
1706
1707
1708 007256 000004
1709 007260 042777 000100 173024
1710 007266 042777 000100 173012
1711 007274 052777 000004 173010
1712 007302 017703 173010
1713 007306 012777 007350 173002
1714 007314 005077 173000
1715 007320 004767 002244
1716 007324 000140
1717 007326 005077 172762
1718 007332 105777 172750 15:
1719 007336 100375
1720 007340 042777 000004 172744
1721 007346 000405
1722 007350 042777 000004 172734 25:
1723 007356 022626
1724 007360 104071
1725
1726
1727 007362 012777 007412 172726 35:
1728 007370 052777 000100 172710
1729 007376 000240
1730 007400 042777 000004 172704
1731 007406 022626
1732 007410 104072
1733
1734
1735 007412 042777 000004 172672 45:
1736 007420 010377 172672
1737 007424 042777 000100 172654

```

```

*****
:TEST 33 TEST THAT RCVR INTERRUPTS ONLY WHEN ENABLED
*****
†ST33: SCOPE
BIC #BIT6,@TCSR ;DISABLE TRANSMIT INTERRUPTS
BIC #BIT6,@RCSR ;DISABLE RECEIVER INTERRUPTS
BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
MOV @RVECT,R3 ;SAVE RECEIVE VECTOR
MOV #25,@RVECT ;POINT RCY VECTOR TO ERROR REPORT
CLR @RPSW ;PSW VECTOR CLEAR
JSR PC,WPSW ;SET PSW TO PRIORITY 3
        .WORD 140
CLR @TBUF ;SEND A CHARACTER
TSTB @RCSR ;WAIT FOR RECEIVER DONE
BPL 15
BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
BR 35 ;CONTINUE TEST
BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 71 ;RECEIVER INTERRUPTS WITH INT. ENABLE CLEAR
35: MOV #45,@RVECT ;POINT RCY VECTOR TO END OF TEST
BIS #BIT6,@RCSR ;ENABLE RCY INTERRUPTS
NOP ;GIVE ANY INTERRUPTS TIME
BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 72 ;RCVR DID NOT INTERRUPT
45: BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
MOV R3,@RVECT ;RESTORE RECEIVE VECTOR
BIC #BIT6,@RCSR ;DISABLE INTERRUPTS

```

```

1738
1739
1740
1741
1742
1743 007432 000004
1744 007434 000005
1745 007436 052777 000004 172646
1746 007444 004767 002120
1747 007450 000340
1748 007452 017703 172640
1749 007456 012777 007514 172632
1750 007464 005077 172630
1751 007470 005077 172620
1752 007474 105777 172606 1S:
1753 007500 100375
1754 007502 052777 000100 172576
1755 007510 000240
1756 007512 000405
1757 007514 042777 000004 172570 2S:
1758 007522 022626
1759 007524 104073
1760
1761
1762 007526 042777 000100 172552 3S:
1763 007534 012777 007562 172554
1764 007542 004767 002022
1765 007546 000140
1766 007550 000240
1767 007552 042777 000004 172532
1768 007560 000405
1769
1770 007562 042777 000004 172522 4S:
1771 007570 022626
1772 007572 104074
1773
1774 007574 010377 172516 5S:

```

```

:*****
:TEST 34 TEST THAT RCVR INTERRUPTS DO NOT OCCUR WHEN DISABLED
:*****
TST34: SCOPE
RESET
BIS #BIT2,RTCSR ;CLEAR EVERYTHING
JSR PC,WRPSW ;SET MAINTENANCE WRAP
;SET PSM TO PRIORITY 7
.WORD 340
MOV R3,ARVECT ;SAVE RECEIVE VECTOR
MOV R25,ARVECT ;POINT RCVR VECTOR TO ERROR REPORT
CLR RPSW ;PSW VECTOR CLEAR
CLR RTBUF ;SEND A CHARACTER
TSTB RTCSR ;WAIT FOR RECEIVER DONE
BPL IS
BIS #BIT6,RTCSR ;ENABLE INTERRUPTS
NOP ;GIVE TIME FOR INTERRUPT
BR 3S ;CONTINUE TEST
BIC #BIT2,RTCSR ;CLEAR MAINTENANCE BIT
CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 73
;RCVR INTERRUPTS AT PRIORITY 7
BIC #BIT6,RTCSR ;CLEAR INTERRUPT ENABLE
MOV R45,ARVECT ;POINT RCVR VECTOR TO ERROR REPORT
JSR PC,WRPSW ;SET PSM TO PRIORITY 3
.WORD 140
NOP ;GIVE TIME FOR ANY INTERRUPT
BIC #BIT2,RTCSR ;CLEAR MAINTENANCE BIT
BR 5S ;BR TO END OF TEST, IF NO INTERRUPT
BIC #BIT2,RTCSR ;CLEAR MAINTENANCE BIT
CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 74
;RCVR INTERRUPT REQUEST PASSED WITH BIT6 CLEAR
MOV R3,ARVECT ;RESTORE RECEIVE VECTOR

```

```

1775
1776
1777
1778
1779
1780 007600 000004
1781 007602 000005
1782 007604 052777 000004 172500
1783 007612 017703 172500
1784 007616 012777 007670 172472
1785 007624 005077 172470
1786 007630 004767 001734
1787 007634 000140
1788 007636 005077 172452
1789 007642 105777 172440 1S:
1790 007646 100375
1791 007650 042777 000004 172434
1792 007656 052777 000100 172422
1793 007664 000240
1794
1795 007666 104075
1796
1797
1798 007670 022626
1799 007672 012777 007716 172416 2S:
1800 007700 000240
1801 007702 042777 000100 172376
1802 007710 010377 172402
1803 007714 000402
1804
1805 007716 022626 3S:
1806 007720 104076
1807
1808 007722 010377 172370 4S:

```

```

:*****
:TEST 35 TEST RECEIVER FOR DOUBLE INTERRUPTS
:*****
TST35: SCOPE
RESET ;CLEAR EVERYTHING
BIS #BIT2, @TCSR ;SET MAINTENANCE WRAP
MOV @RVECT, R3 ;SAVE RECEIVE VECTOR
MOV #2S, @RVECT ;POINT RCV VECTOR TO CONTINUE TEST
CLR @RPSW ;CLEAR PSM VECTOR
JSR PC, @RPSW ;SET PSM TO PRIORITY 3
.WORD 140
CLR @TBUF ;SEND A CHARACTER
TSTB @RCSR ;WAIT FOR RCVR DONE
BPL 1S
BIC #BIT2, @TCSR ;CLEAR MAINTENANCE BIT
BIS #BIT6, @RCSR ;ENABLE RCV INTERRUPTS
NOP ;GIVE SOME TIME

ERROR 75 ;RCVR INTERRUPT DID NOT OCCUR

CMP (SP)+, (SP)+ ;RESTORE SP AFTER INTERRUPT
MOV #3S, @RVECT ;POINT RCV VECTOR TO ERROR REPORT
NOP ;GIVE SOME TIME
BIC #BIT6, @RCSR ;CLEAR INTERRUPT ENABLE
MOV R3, @RVECT ;RESTORE RECEIVE VECTOR
BR 4S ;BR TO END OF TEST

CMP (SP)+, (SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 76 ;RECEIVER RE-INTERRUPTED
MOV R3, @RVECT ;RESTORE RECEIVE VECTOR

```

```

1809
1810
1811
1812
1813
1814 007726 000004
1815 007730 000005
1816 007732 004767 001632
1817 007736 000340
1818 007740 017703 172352
1819 007744 012777 010036 172344
1820 007752 005077 172342
1821 007756 052777 000100 172322
1822 007764 052777 000004 172320
1823 007772 005077 172316
1824 007776 105777 172304 15:
1825 010002 100375
1826 010004 042777 000004 172300
1827 010012 005077 172272
1828 010016 004767 001546
1829 010022 000140
1830 010024 000240
1831 010026 042777 000100 172252
1832 010034 000402
1833
1834 010036 022626 25:
1835 010040 104077
1836
1837 010042 010377 172250 35:
1838

```

```

*****
;TEST 36 TEST THAT RCVR INTERRUPT CLEARS BY READING RBUF
*****
↑ST36: SCOPE
RESET ;CLEAR EVERYTHING
JSR PC,WRPSW ;SET PSM PRIORITY TO 7
.WORD 340
MOV @RVECT,R3 ;SAVE RECEIVE VECTOR
MOV #25,@RVECT ;POINT RCV VECTOR TO ERROR REPORT
CLR @RPSW ;CLEAR PSM VECTOR
BIS #BIT6,@RCSR ;SET RCVR INTERRUPT ENABLE
BIS #BIT2,@TCSR ;SET MAINTENANCE WRAP
CLR @TBUF ;SEND A CHARACTER
15: TSTB @RCSR ;WAIT FOR DONE
BPL 15
BIC #BIT2,@TCSR ;CLEAR MAINTENANCE BIT
CLR @RBUF ;READ RBUF TO CLEAR PENDING INTERRUPT
JSR PC,WRPSW ;SET PSM TO PRIORITY 3
.WORD 140
NOP
1831 BIC #BIT6,@RCSR ;NO INTERRUPT-CLEAR INT. ENABLE
1832 BR 35
25: CMP (SP)+,(SF)+ ;RESTORE SP AFTER INTERRUPT
ERROR 77 ;READING RBUF DID NOT CLEAR INTERRUPT
35: MOV R3,@RVECT ;RESTORE RECEIVE VECTOR

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1839
1840
1841
1842
1843
1844 010046 000004
1845 010050 000005
1846 010052 004767 001512
1847 010056 000340
1848 010060 017703 172232
1849 010064 012777 010150 172224
1850 010072 005077 172222
1851 010076 052777 000100 172202
1852 010104 052777 000004 172200
1853 010112 012777 000377 172174
1854 010120 105777 172162
1855 010124 100375
1856 010126 000005
1857 010130 004767 001434
1858 010134 000140
1859 010136 000240
1860 010140 042777 000100 172140
1861 010146 000402
1862
1863
1864 010150 022626
1865 010152 104100
1866
1867 010154 010377 172136

:*****
:TEST 37 TEST THAT RESET CLEARS RECEIVE INTERRUPT
:*****
TST37: SCOPE
RESET ;CLEAR EVERYTHING
JSR PC,WRPSW ;SET PSM TO PRIORITY 7
.WORD 340
MOV @RVECT,R3 ;SAVE RECEIVE VECTOR
MOV @25,@RVECT ;POINT RCY VECTOR TO ERROR REPORT
CLR @RPSW ;CLEAR PSM VECTOR
BIS @BIT6,@RCSR ;SET RCY INTERRUPT ENABLE
BIS @BIT2,@TCSR ;SET MAINTENANCE WRAP
MOV @377,@TBUF ;SEND AN ALL 1'S CHARACTER
18: TSTB @RCSR ;WAIT FOR RCY DONE
BPL 18
RESET ;CLEAR RCY INTERRUPT & RBUF
JSR PC,WRPSW ;SET PSM TO PRIORITY 3
.WORD 140
NOP
BIC @BIT6,@RCSR ;NO INTERRUPT-CLEAR INT. ENABLE
BR 35 ;CONTINUE TEST

25: CMP (SP)+,(SP)+ ;RESTORE SP AFTER INTERRUPT
ERROR 100 ;RESET DID NOT CLEAR RCVR INTERRUPT

35: MOV R3,@RVECT ;RESTORE RECEIVE VECTOR
  
```

```

1868
1869
1870
1871
1872
1873 010160 000004
1874 010162 032777 002000 170650
1875 010170 001440
1876 010172 000005
1877 010174 052777 000004 172110
1878 010202 012700 000003
1879 010206 005077 172102 1S:
1880 010212 105777 172074 2S:
1881 010216 100375
1882 010220 005300
1883 010222 001371
1884 010224 032777 040000 172056
1885 010232 001004
1886 010234 042777 000004 172050
1887 010242 104101
1888
1889
1890 010244 032777 100000 172036 3S:
1891 010252 001004
1892 010254 042777 000004 172030
1893 010262 104102
1894
1895 010264 042777 000004 172020 4S:

```

```

*****
: TEST 40 TEST THAT THE "OR" ERROR (BIT14) & "ERROR" (BIT15) CAN BE SET
*****
TST40: SCOPE
BIT #BIT10,2SWR ; IS THIS TEST ENABLED
BEQ TST41 ; IF NOT ENABLED, BR TO NEXT TEST
RESET ; CLEAR EVERYTHING
BIS #BIT2,2TCSR ; SET MAINTENANCE WRAP
MOV #3,RO ; SET CHARACTER COUNT TO SEND 3 CHAR.
CLR 2TBUF ; LOAD TRANSMIT BUFFER
TSTB 2TCSR ; WAIT FOR TRANSMIT DONE
BPL 2S ;
DEC RO ; DECREMENT CHARACTER COUNT
BNE 1S ; BR IF ALL CHARACTERS NOT TRANSMITTED
BIT #BIT14,2RBUF ; TEST FOR "OR" ERROR FLAG
BNE 3S ; BR IF SET
BIC #BIT2,2TCSR ; CLEAR MAINTENANCE BIT
ERROR 101 ; "OR" ERROR FLAG DID NOT SET

3S: BIT #BIT15,2RBUF ; TEST "ERROR" FLAG
BNE 4S ; BR IF SET
PIC #BIT2,2TCSR ; CLEAR MAINTENANCE BIT
ERROR 102 ; "ERROR" FLAG DID NOT SET WITH "OR" FLAG

4S: BIC #BIT2,2TCSR ; CLEAR MAINTENANCE BIT

```

D05

.MAIN. MACY11 27(732)  
DZDLDA.P11 T40

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TEST THAT THE "OR" ERROR (BIT14) & "ERROR" (BIT15) CAN BE SET

SEQ 0055

```

1896
1897
1898
1899
1900
1901 010272 000004
1902 010274 032777 000400 170536
1903 010302 001444
1904 010304 000005
1905 010306 052777 000004 171776
1906 010314 012777 177777 171772
1907 010322 105777 171760 18:
1908 010326 100375
1909 010330 005077 171754
1910 010334 052777 000001 171750
1911 010342 005000
1912 010344 117767 171736 170454 28:
1913 010352 100406
1914 010354 075200
1915 010356 001372
1916
1917 010360 042777 000005 171724
1918 010366 104103
1919
1920 010370 105777 171714 CONT41:
1921 010374 001404
1922 010376 042777 000005 171706
1923
1924 010404 104103
1925
1926 010406 042777 000005 171676 38:

```

```

:*****
:TEST 41 TEST THAT BREAK TRANSMITS ALL ZEROES
:*****
TST41: SCOPE
BIT #BIT8, @SMR ; IS BREAK FUNCTION TEST ENABLED?
BEQ TST42 ; BR TO NEXT TEST, IF NOT ENABLED
RESET ; CLEAR EVERYTHING
BIS #BIT2, @TCSR ; SET MAINTENANCE WRAP
MOV @-1, @RBUF ; TRANSMIT ALL ONES TO RCVR
TSTB @RCSR ; WAIT FOR RCVR DONE
BPL 18
CLR @RBUF ; CLEAR DONE (LEAVING ALL ONES IN RBUF)
BIS #BIT0, @TCSR ; TRANSMIT BREAK
CLR @R ; CLEAR A TIMER
NOVB @RCSR, @DDAT ; WAIT FOR RCVR DONE
BMI CONT41 ; BR IF DONE
INC @R ; IF NOT, INCREMENT TIMER
BNE 28 ; BR IF TIME REMAINS

BIC #BIT0!BIT2, @TCSR ; CLEAR MAINTENANCE & BREAK BITS
ERROR 103 ; BREAK DID NOT TRANSMIT ANYTHING

CONT41: TSTB @RBUF ; CHECK RECEIVE BUFFER FOR ZERO
BEQ 38 ; BR IF ZERO
BIC #BIT0!BIT2, @TCSR ; CLEAR MAINTENANCE & BREAK BITS

ERROR 103 ; BREAK DID NOT TRANSMIT ALL ZEROES

BIC #BIT0!BIT2, @TCSR ; CLEAR MAINTENANCE & BREAK BITS

```

E05

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1927
1928
1929
1930
1931
1932 010414 000004
1933 010416 032777 002000 170414
1934 010424 001435
1935 010426 032777 000400 170404
1936 010434 001431
1937 010436 000005
1938 010440 052777 000004 171644
1939 010446 052777 000001 171636
1940 010454 005077 171634
1941 010460 105777 171626
1942 010464 100375
1943 010466 005077 171622
1944 010472 105777 171614
1945 010476 100375
1946 010500 042777 000005 171604
1947 010506 032777 020000 171574
1948 010514 001001
1949 010516 104104
1950
1951

```

```

*****
*TEST 42 TEST THAT "FR" ERROR CAN BE SET DURING BREAK
*****
TST42: SCOPE
BIT #BIT10, @SMR ; IS THE "TEST ERROR FLAGS" BIT SET
BEQ TST43 ; BR TO NEXT TEST, IF NOT SET
BIT #BIT8, @SMR ; IS BREAK FUNCTION ENABLED
BEQ TST43 ; BR TO NEXT TEST, IF NOT SET
RESET ; CLEAR EVERYTHING
BIS #BIT2, @TCSR ; SET MAINTENANCE WRAP
BIS #BIT0, @TCSR ; SEND BREAK
CLR @TBUF ; TRANSMIT A CHARACTER TO TIME BREAK
15: TSTB @TCSR ; WAIT FOR XMIT DONE
BPL 15
CLR @TBUF ; FILL SECOND BUFFER
25: TSTB @TCSR ; WAIT ONE CHARACTER TIME (DONE)
BPL 25
BIC #BIT0:BIT2, @TCSR ; CLEAR MAINTENANCE & BREAK BITS
BIT #BIT13, @RBUF ; CHECK FOR FRAMING ERROR FLAG
BNE TST43 ; BR, IF SET
ERROR 104 ; BREAK DID NOT SET FRAMING ERROR

```

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1956 *****
1957 *****
1958 *****
1959 *****
1960 *****
1961 *****
1962 *****
1963 *****
1964 *****
1965 *****
1966 *****
1967 *****
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1969 *****
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2005 *****
2006 *****

010520 000004 TST43: SCOPE
010522 000005 RESET ;CLEAR EVERYTHING
010524 005001 CLR R1 ;CLEAR REGISTER FOR TEST DATA
010526 052777 000004 171556 BIS #BIT2, JTCR ;SET MAINTENANCE WRAP
010534 010177 171554 1S: MOV R1, JTBUF ;XMIT A CHARACTER
010540 105777 171542 2S: TSTB JRCR ;WAIT FOR RECEIVER DONE
010544 100375 BPL 2S
010546 017702 171536 MOV JRBUFF, R2 ;GET RECEIVED CHARACTER
010552 020102 CMP R1, R2 ;COMPARE DATA
010554 001003 BNE 3S ;BR, IF NON-COMPARE
010556 105201 INCB R1 ;INCREMENT TEST DATA
010560 001411 BEQ 4S ;BR, IF FINISHED
010562 000764 BR 1S ;CONTINUE IF NOT
010564 010167 170234 3S: MOV R1, $GDDAT ;STORE THE EXPECTED DATA
010570 010267 170232 MOV R2, $RDDAT ;STORE RECEIVED DATA
010574 042777 000004 171510 BIC #BIT2, JTCR ;CLEAR MAINTENANCE BIT
010602 104105 ERROR 105 ;DATA COMPARE DATA
010604 042777 000004 171500 4S: BIC #BIT2, JTCR ;CLEAR MAINTENANCE BIT

*****
TEST 44 TEST DATA PATHS USING WRAP CABLE
*****
1983 *****
1984 *****
1985 *****
1986 *****
1987 *****
1988 *****
1989 *****
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2003 *****
2004 *****
2005 *****
2006 *****

010612 000004 TST44: SCOPE
010614 032777 000200 170216 BIT #BIT7, JSWR ;IS THIS TEST ENABLED
010622 001427 BEQ TST45 ;BR, IF NOT
010624 005001 CLR R1 ;CLEAR REGISTER FOR TEST DATA
010626 000005 RESET ;CLEAR EVERYTHING
010630 010177 171460 1S: MOV R1, JTBUF ;XMIT A CHARACTER
010634 005000 CLR R0 ;CLEAR A TIMER
010636 105777 171444 2S: TSTB JRCR ;WAIT FOR RECEIVER DONE
010642 100403 BMI 3S ;BR IF DONE
010644 005200 INC R0 ;INCREMENT TIMER IF NOT
010646 001373 BNE 2S ;BR IF TIME REMAINS
010650 104064 ERROR 64 ;RECEIVER DONE NOT SET
010652 017702 171432 3S: MOV JRBUFF, R2 ;GET RECEIVED CHARACTER
010656 020102 CMP R1, R2 ;COMPARE DATA
010660 001003 BNE 4S ;BR, IF NON-COMPARE
010662 105201 INCB R1 ;INCREMENT TEST DATA
010664 001406 BEQ TST45 ;BR, IF FINISHED
010666 000764 BR 1S ;CONTINUE IF NOT
010670 010167 170130 4S: MOV R1, $GDDAT ;STORE EXPECTED DATA
010674 010267 170126 MOV R2, $RDDAT ;STORE RECEIVED DATA
010700 104106 ERROR 106 ;DATA COMPARE ERROR WITH WRAP CABLE
    
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2055

010702 000004  
010704 000005  
010706 017703 171410  
010712 017704 171400  
010716 012777 011214 171376  
010724 005077 171374  
010730 012777 011250 171360  
010736 005077 171356  
010742 005767 171330  
010746 001416  
010750 032777 000100 170062  
010756 001012  
010760 017705 171364  
010764 012777 011264 171356  
010772 005077 171354  
010776 052777 000100 171342  
011004 052777 000004 171300  
011012 052777 000100 171272  
011020 052777 000100 171260  
011026 005067 000242  
011032 005067 000234  
011036 004767 000526  
011042 000140  
011044 005001  
011046 005000  
011050 012702 011300  
011054 005077 171234  
011060 005200  
011062 001376  
011064 032777 000100 171220  
011072 001402  
011074 000005  
011076 104107  
011100 026767 000170 000164  
011106 001402  
011110 000005  
011112 104110

\*\*\*\*\*  
:TEST 45 TEST DL11-W LOGIC BY EXERCISING THE XMIT, RECEIVE, & CLOCK (IF AVAILABLE)  
\*\*\*\*\*

15T45: SCOPE  
RESET  
MOV @TVECT,R3 ;CLEAR EVERYTHING  
MOV @RVECT,R4 ;SAVE XMIT VECTOR  
MOV @XMIT,@TVECT ;SAVE RECEIVE VECTOR  
CLR @TPSW ;POINT TRANSMIT VECTOR TO TRANSMIT ROUTINE  
MOV @RCV,@RVECT ;ALLOW INTERRUPTS AFTER XMIT INTERRUPT  
CLR @RPSW ;POINT RECEIVE VECTOR TO RECEIVE ROUTINE  
TST CTSTFL ;ALLOW INTERRUPTS AFTER RCVR INTERRUPT  
BEQ 15 ;IS CONSOLE UNDER TEST?  
BIT #BIT6,@SMR ;IF NOT SKIP CLOCK SET UP  
BNE 15 ;IF YES, ARE CLOCK TEST DISABLED?  
MOV @RTCVT,R5 ;IF YES, SKIP CLOCK SET UP  
MOV #CLK,@RTCVT ;SAVE CLOCK VECTOR  
CLR @RTCPSW ;POINT VECTOR TO CLOCK INTERRUPT ROUTINE  
BIS #BIT6,@LKS ;ALLOW INTERRUPTS AFTER CLOCK INTERRUPT  
BIS #BIT2,@TCSR ;ENABLE CLOCK INTERRUPTS  
BIS #BIT6,@TCSR ;SET MAINTENANCE WRAP  
BIS #BIT6,@RCR ;ENABLE TRANSMIT INTERRUPTS  
CLR XMITCNT ;ENABLE RECEIVE INTERRUPTS  
CLR RCVCNT ;CLEAR XMIT INTERRUPT COUNTER  
JSR PC,WRPSW ;CLEAR RCV INTERRUPT COUNTER  
WORD 140 ;SET PSM TO PRIORITY 3  
CLR R1 ;CLEAR A REGISTER FOR TEST DATA USE  
CLR R0 ;CLEAR TIMER  
MOV #BUF,R2 ;POINT R2 TO RECEIVE DATA STORAGE  
CLR @TBUF ;SEND FIRST CHARACTER  
INC R0 ;WAIT FOR INTERRUPTS  
BNE 25  
BIT #BIT6,@TCSR ;FINISHED ENTIRE TRANSMISSION  
BEQ 35 ;OR, IF INTERRUPTS ARE DISABLED (FINISHED)  
RESET ;CLEAR EVERYTHING  
ERROR 107 ;TRANSMIT INTERRUPT TIMEOUT IN MAIN. DATA TEST  
CMP XMITCNT,RCVCNT ;COMPARE THE NUMBER OF INTERRUPTS  
BEQ 45 ;OR, IF EQUAL  
RESET ;CLEAR EVERYTHING  
ERROR 110 ;RECEIVER DID NOT GET FULL TRANSMISSION  
IF RCVCNT=0, NO DATA RECEIVED  
IF RCVCNT?0, TEN (XMITCNT-RCVCNT)  
EQUALS THE NO, OF INTERRUPTS LOST.

15:

25:

35:

# H05

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TEST DL11-W LOGIC BY EXERCISING THE XMIT, RECEIVE, & CLOCK (IF AVAILABLE) SIMULTANEOUS

SEQ 0059

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2056
2057
2058 011114 005767 171156      4S:   TST      CTSTFL      ; IS CONSOLE UNDER TEST?
2059 011120 001410                BEQ      SS          ; IF NOT, SKIP CLOCK COUNT CHECK
2060 011122 032777 000100 167710    BIT      #BIT6, @SWR ; IF YES, ARE CLOCK TESTS DISABLED?
2061 011130 001004                BNE      SS          ; IF YES, SKIP CLOCK COUNT CHECK
2062 011132 005767 000140    TST      CLKCNT     ; CHECK FOR AT LEAST ONE CLOCK INTERRUPT
2063 011136 001001                BNE      SS          ; BR IF INTERRUPTS OCCURRED
2064
2065 011140 104113                ERROR    113        ; NO CLOCK INTERRUPTS IN EXERCISER
2066
2067 011142 000005                SS:   RESET
2068 011144 012700 011300    MOV      #BUF, R0   ; CLEAR EVERYTHING
2069 011150 005001                CLR      R1         ; LOAD RECEIVED DATA POINTER TO R0
2070 011152 022001                COMP:  CMP      (R0)+, R1 ; SET UP REGISTER FOR COMPARISON
2071 011154 001005                BNE      6S        ; COMPARE XMIT & RCV DATA
2072 011156 105201                INCB    R1         ; BR, IF NOT EQUAL
2073 011160 032701 000010    BIT      #BIT3, R1  ; INCREMENT COMPARE DATA
2074 011164 001372                BNE      COMP      ; FINISHED CHECKING RECEIVED DATA?
2075 011166 000405                BR      7S        ; BR, IF NOT FINISHED
2076
2077 011170 014067 167632    6S:   MOV      -(R0), @SDDAT ; STORE BAD DATA FOR ERROR REPORT
2078 011174 010167 167624    MOV      R1, @GDDAT ; STORE GOOD DATA FOR ERROR REPORT
2079 011200 104111                ERROR    111        ; DATA COMPARE ERROR IN EXERCISER
2080
2081 011202 010377 171114    7S:   MOV      R3, @TVECT ; RESTORE XMIT VECTOR
2082 011206 010477 171104    MOV      R4, @RVECT ; RESTORE RECEIVE VECTOR
2083 011212 000472                BR      ENDEV      ; BR TO END OF DEVICE TEST ROUTINE
2084
2085 011214 005267 000054    XMIT:  INC      XMITCNT ; INCREMENT XMIT INTERRUPT COUNTER
2086 011220 105201                INCB    R1         ; INCREMENT TEST DATA
2087 011222 032701 000040    BIT      #BITS, R1  ; SEND DATA PATTERN FROM 00 --> 37
2088 011226 001404                BEQ      XCONT     ; BR, IF MORE DATA TO BE SENT
2089 011230 042777 000100 171054    BIC      #BIT6, @TCSR ; CLEAR XMIT INTERRUPT ENABLE
2090 011236 000402                BR      XRET      ; RETURN, WITHOUT SENDING ANY MORE DATA
2091 011240 110177 171050    XCONT: MOVB    R1, @TBUF ; SEND NEW CHARACTER
2092 011244 005000                XRET:  CLR      R0   ; CLEAR TIMER
2093 011246 000002                RTI
2094
2095 011250 017722 171034    RCV:   MOV      @RBUF, (R2)+ ; STORE RECEIVED DATA
2096 011254 005267 000012    INC      RCVCNT    ; INCREMENT RCV INTERRUPT COUNTER
2097 011260 005000                CLR      R0         ; CLEAR TIMER
2098 011262 000002                RTI
2099
2100 011264 005267 000006    CLK:   INC      CLKCNT ; INCREMENT CLOCK INTERRUPT COUNT
2101 011270 000002                RTI
2102
2103 011272 000000                RCVCNT: .WORD    0
2104 011274 000000                XMITCNT: .WORD   0
2105 011276 000000                CLKCNT:  .WORD   0
2106 011300 000040                BUF:    .BLKW   40
2107

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.MAIN. MACY11 27(732)  
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TEST DL11-W LOGIC BY EXERCISING THE XMIT, RECEIVE, & CLOCK (IF AVAILABLE) SIMULTANEOUS

SEQ 0060

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2108
2109
2110 ;END OF DEVICE PASS ROUTINE
2111 011400 005067 167376 ENDEV: CLR $TSTNM ;CLEAR TEST NO. COUNT FOR SCOPE ROUTINE
2112 011404 005267 167466 INC $DEVCT ;INCREMENT DEVICE COUNTER
2113 011410 026767 170666 167460 CMP TMP2,$DEVCT ;ALL DEVICES TESTED
2114 011416 001404 BEQ SEOP ;BR. IF YES
2115 011420 005067 170652 CLR CTSTFL ;CLEAR CONSOLE UNDER TEST FLAG
2116 011424 000167 171754 JMP TSTDEV ;GO TEST NEXT DEVICE

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2117
2118
2119
2120 .SBTTL END OF PASS ROUTINE
2121
2122 ;*****
2123 ;#INCREMENT THE PASS NUMBER ($PASS)
2124 ;#IF THERES A MONITOR GO TO IT
2125 ;#IF THERE ISN'T JUMP TO GOAGIN

```

```

2126 SEOP:
2127 011430
2128 011430 000004 SCOPE
2129 011432 005067 167344 CLR $TSTNM ;ZERO THE TEST NUMBER
2130 011436 005267 167432 INC $PASS ;INCREMENT THE PASS NUMBER
2131 011442 042767 100000 167424 BIC #100000,$PASS ;DON'T ALLOW A NEG. NUMBER
2132 011450 005327 DEC (PC)+ ;LOOP?
2133 011452 000001 SEOPCT: .WORD 1
2134 011454 003015 BGT $DOAGN ;YES
2135 011456 012737 MOV (PC)+,$(PC)+ ;RESTORE COUNTER
2136 011460 000001 SENDCT: .WORD 1
2137 011462 011452 SEOPCT
2138 011464 104401 011520 TYPE .ENDMG ;TYPE "END PASS"
2139 011470 013700 000042 $GET42: MOV #42,R0 ;GET MONITOR ADDRESS
2140 011474 001405 BEQ $DOAGN ;BRANCH IF NO MONITOR
2141 011476 000005 RESET ;CLEAR THE WORLD
2142 011500 004710 SENDAD: JSR PC,(R0) ;GO TO MONITOR
2143 011502 000240 NOP ;SAVE ROOM
2144 011504 000240 NOP ;FOR
2145 011506 000240 NOP ;ACT11
2146 011510 $DOAGN:
2147 011510 000137 JMP @(PC)+ ;RETURN
2148 011512 011534 SRTNAD: .WORD GOAGIN
2149 011514 377 377 000 SENULL: .BYTE -1,-1,0 ;NULL CHARACTER STRING
2150 011520 011520 .EVEN
2151 011520 005015 047105 020104 ENDMG: .ASCIZ <CR><LF>/END PASS /
2152 011526 040520 051523 000040

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2153
2154 011534 005067 167336          GOAGIN: CLR      SDEVCT      ;CLEAR DEVICE COUNT
2155 011540 022767 000001 170534  CMP      #1,TMP2      ;IS THERE ONLY ONE DEVICE UNDER TEST?
2156 011546 001004          BNE      RSTRT      ;BR, IF NOT
2157 011550 012706 001000          MOV      #1000,SP    ;RESET STACK POINTER
2158 011554 000167 171746          JMP      TST1       ;GO DO ANOTHER PASS
2159
2160 011560 005067 167314          RSTRT: CLR      $UNIT    ;CLEAR UNIT NUMBER
2161 011564 000167 171540          JMP      BEGIN
2162
2163 011570 011646          WRPSW: MOV(SP),-(SP)   ;COPY RETURN PC
2164 011572 013616          MOV      2(SP),-(SP) ;MOVE NEW PSW TO STACK
2165 011574 062746 000002          ADD      #2,-(SP)   ;ADJUST JSR RETURN
2166 011600 000006          RTT              ;POP RETURN PC & NEW PSW
2167
2168          ;SUBROUTINE TO REPORT UNEXPECTED OR ERRONEOUS TRAPS OR INTERRUPTS
2169
2170 011602 012600          CATCH: MOV      (SP)+,R0 ;GET ADDRESS OF TRAP VECTOR + 4
2171 011604 162700 000004          SUB      #4,R0      ;ADJUST TO POINT TO TRAP ADDRESS
2172 011610 010067 000014          MOV      R0,BDVECT  ;STORE TRAP OR INTERRUPT ADDRESS
2173 011614 016667 000002 000004          MOV      2(SP),OLDPC ;GET PC WHERE TRAP OR INTERRUPT OCCURRED
2174 011622 104112          ERROR 112         ;REPORT ERROR
2175
2176 011624 000000          HALT              ;PROGRAM MUST BE RESTARTED AT THIS POINT
2177 011626 000000          OLDPC: .WORD     0
2178 011630 000000          BDVECT: .WORD    0
2179

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2222  
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011632  
011632 105267 167145  
011636 001775  
011640 016777 167136 167174  
011646 005267 167140  
011652 011667 167140  
011656 162767 000002 167132  
011664 117767 167126 167122  
011672 032777 020000 167140  
011700 001004  
011702 004767 000106  
011706 104401 001063  
011712  
011712 122767 000001 167166  
011720 001007  
011722 116767 167066 000004  
011730 004767 000562  
011734 000  
011735 000  
011736 000777  
011740 005777 167074  
011744 100001  
011746 000000  
011750 104406  
011752 032777 001000 167060  
011760 001402  
011762 016716 167022  
011766 005767 167066  
011772 001402  
011774 016716 167060  
012000  
012000 022737 011500 000042  
012006 001001  
012010 000000  
012012  
012012 000002

```
*****
: THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,
: SAVE THE ERROR ITEM NUMBER AND ADDRESS OF THE ERROR CALL
: AND GO TO SERRTYP ON ERROR
: THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
: SW15=1 HALT ON ERROR
: SW13=1 INHIBIT ERROR TYPEOUTS
: SW09=1 LOOP IN ERROR
: CALL
: ERROR N ;:ERROR=EMT AND N=ERROR ITEM NUMBER
*****
```

```
SERROR:
7S: INCB SERFLG ;SET THE ERROR FLAG
BEQ 7S ;DON'T LET FLAG GO TO ZERO
MOV $STNM,$DISP ;DISPLAY TEST NUMBER AND ERROR FLAG
INC SERTTL ;INCREMENT ERROR COUNT
MOV (SP),SERRPC ;GET ADDRESS OF ERROR INSTRUCTION
SUB #2,SERRPC
MOVB @SERRPC,$ITEMB ;STRIP AND SAVE THE ERROR ITEM CODE
BIT #BIT13,$SWR ;SKIP TYPEOUT IF SET
BNE 20S ;SKIP TYPEOUTS
JSR PC,SERRTYP ;GO TO USER ERROR ROUTINE
TYPE ,SCLF

20S: CMPB #APTENV,$ENV ;RUNNING IN APT MODE
BNE 2S ;NO, SKIP APT ERROR REPORT
MOVB $ITEMB,21S ;SET ITEM NUMBER AS ERROR NUMBER
JSR PC,$ATY4 ;REPORT FATAL ERROR TO APT

21S: .BYTE 0
.BYTE 0

22S: BR 22S ;APT ERROR LOOP
TST @SWR ;HALT ON ERROR
BPL 3S ;SKIP IF CONTINUE
HALT ;HALT ON ERROR!

3S: CKSWR ;TEST FOR CHANGE IN SOFT-SWR
BIT #BIT09,$SWR ;LOOP ON ERROR SWITCH SET?
BEQ 4S ;BR IF NO
MOV $LPERR,(SP) ;FUDGE RETURN FOR LOOPING
TST $ESCAPE ;CHECK FOR AN ESCAPE ADDRESS
BEQ 5S ;BR IF NONE
MOV $ESCAPE,(SP) ;FUDGE RETURN ADDRESS FOR ESCAPE

5S: CMP #SENDAD,@#42 ;ACT-11 AUTO-ACCEPT?
BNE 6S ;BR IF NO
HALT ;YES

6S: RTI ;RETURN
```

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.SBTTL ERROR MESSAGE TYPEOUT ROUTINE

```

;*****
;THIS ROUTINE USES THE "ITEM CONTROL BYTE" ($ITEMB) TO DETERMINE WHICH
;ERROR IS TO BE REPORTED. IT THEN OBTAINS, FROM THE "ERROR TABLE" ($ERRTB),
;AND REPORTS THE APPROPRIATE INFORMATION CONCERNING THE ERROR.

```

```

SERRTYP:
        TYPE      $SCRLF          ;; "CARRIAGE RETURN" & "LINE FEED"
        MOV       RO,-(SP)        ;; SAVE RO
        CLR       RO              ;; PICKUP THE ITEM INDEX
        BISB      @#$ITEMB,RO
        BNE       IS
        MOV       SERRPC,-(SP)    ;; IF ITEM NUMBER IS ZERO, JUST
        ;; TYPE THE PC OF THE ERROR
        ;; SAVE SERRPC FOR TYPEOUT
        ;; ERROR ADDRESS
        TYPCC     6$              ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
        BR        6$              ;; GET OUT
        IS:      DEC             ;; ADJUST THE INDEX SO THAT IT WILL
        ASL       RO              ;; WORK FOR THE ERROR TABLE
        ASL       RO
        ASL       RO
        ADD       #SERRTB,RO      ;; FORM TABLE POINTER
        MOV       (RO)+,2$        ;; PICKUP "ERROR MESSAGE" POINTER
        BEQ       3$              ;; SKIP TYPEOUT IF NO POINTER
        TYPE      0               ;; TYPE THE "ERROR MESSAGE"
        ;; "ERROR MESSAGE" POINTER GOES HERE
        2$:      $SCRLF          ;; "CARRIAGE RETURN" & "LINE FEED"
        MOV       (RO)+,4$        ;; PICKUP "DATA HEADER" POINTER
        BEQ       5$              ;; SKIP TYPEOUT IF 0
        TYPE      0               ;; TYPE THE "DATA HEADER"
        ;; "DATA HEADER" POINTER GOES HERE
        3$:      $SCRLF          ;; "CARRIAGE RETURN" & "LINE FEED"
        MOV       (RO),RO         ;; PICKUP "DATA TABLE" POINTER
        BNE       7$              ;; GO TYPE THE DATA
        4$:      MOV             ;; RESTORE RO
        (SP)+,RO
        TYPE      $SCRLF          ;; "CARRIAGE RETURN" & "LINE FEED"
        RTS       PC              ;; RETURN
        5$:      MOV             ;; SAVE @ (RO)+ FOR TYPEOUT
        @ (RO)+,-(SP)
        TYPCC     6$              ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
        TST       (RO)           ;; IS THERE ANOTHER NUMBER?
        BR        6$              ;; BR IF NO
        6$:      TYPE           ;; TYPE TWO(2) SPACES
        8$        8$              ;; LOOP
        .ASCIZ   / /              ;; TWO(2) SPACES
        .EVEN

```

```

012014      104401 001063
012020      010046
012022      005000
012024      153700 001014
012030      001004
012032      016746 166760
012036      104402
012040      000426
012042      005300
012044      006300
012046      006300
012050      006300
012052      062700 001146
012056      012067 000004
012062      001404
012064      104401
012066      000000
012070      104401 001063
012074      012067 000004
012100      001404
012102      104401
012104      000000
012106      104401 001063
012112      011000
012114      001004
012116      012600
012120      104401 001063
012124      000207
012126      013046
012130      104402
012132      005710
012134      001770
012136      104401 012144
012142      000771
012144      020040 000
012150

```

# M05

```

2279
2280 .SBTTL POWER DOWN AND UP ROUTINES
2281 ;;*****
2282 ;#POWER DOWN ROUTINE
2283 ;;*****
2284 012150 012737 012310 000024 $PWRDN: MOV $SILLUP, 2#PWRVEC ;SET FOR FAST UP
2285 012156 012737 000340 000026 MOV #340, 2#PWRVEC+2 ;PRIO:7
2286 012164 010046 MOV RO, -(SP) ;PUSH RO ON STACK
2287 012166 010146 MOV R1, -(SP) ;PUSH R1 ON STACK
2288 012170 010246 MOV R2, -(SP) ;PUSH R2 ON STACK
2289 012172 010346 MOV R3, -(SP) ;PUSH R3 ON STACK
2290 012174 010446 MOV R4, -(SP) ;PUSH R4 ON STACK
2291 012176 010546 MOV R5, -(SP) ;PUSH R5 ON STACK
2292 012200 017746 166634 MOV 2SWR, -(SP) ;PUSH 2SWR ON STACK
2293 012204 010667 000104 MOV SP, $SAVR6 ;SAVE SP
2294 012210 012737 012222 000024 MOV $PWRUP, 2#PWRVEC ;SET UP VECTOR
2295 012216 000000 HALT
2296 012220 000776 BR .-2 ;HANG UP
2297
2298
2299 ;;*****
2300 ;#POWER UP ROUTINE
2301 ;;*****
2302 012222 012737 012310 000024 $PWRUP: MOV $SILLUP, 2#PWRVEC ;SET FOR FAST DOWN
2303 012230 016706 000060 MOV $SAVR6, SP ;GET SP
2304 012234 012677 166600 MOV (SP)+, 2SWR ;POP STACK INTO 2SWR
2305 012240 012605 MOV (SP)+, R5 ;POP STACK INTO R5
2306 012242 012604 MOV (SP)+, R4 ;POP STACK INTO R4
2307 012244 012603 MOV (SP)+, R3 ;POP STACK INTO R3
2308 012246 012602 MOV (SP)+, R2 ;POP STACK INTO R2
2309 012250 012601 MOV (SP)+, R1 ;POP STACK INTO R1
2310 012252 012600 MOV (SP)+, RO ;POP STACK INTO RO
2311 012254 012737 012150 000024 MOV $PWRDN, 2#PWRVEC ;SET UP THE POWER DOWN VECTOR
2312 012262 012737 000340 000026 MOV #340, 2#PWRVEC+2 ;PRIO:7
2313 012270 005067 000020 CLR $SAVR6 ;WAIT LOOP FOR THE TTY
2314 012274 005267 000014 1$: INC $SAVR6 ;WAIT FOR THE INC
2315 012300 001375 BNE 1$ ;OF WORD
2316 012302 104401 TYPE ;REPORT THE POWER FAILURE
2317 012304 012316 SPWRMG: .WORD SPOWER ;POWER FAIL MESSAGE POINTER
2318 012306 000002 RTI
2319 012310 000000 $SILLUP: HALT ;THE POWER UP SEQUENCE WAS STARTED
2320 012312 000776 BR .-2 ;BEFORE THE POWER DOWN WAS COMPLETE
2321 012314 000000 $SAVR6: 0 ;PUT THE SP HERE
2322 012316 005015 047520 042527 $SPOWER: .ASCIZ <15><12>"POWER"
2323 012324 000122
2324

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.SBTTL SCOPE HANDLER ROUTINE

```

*****
: THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
: AND LOAD THE TEST NUMBER($STNM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
: AND LOAD THE ERROR FLAG ($ERFLG) INTO DISPLAY<15:08>
: THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
: *SW14=1      LOOP ON TEST
: *SW09=1      LOOP ON ERROR
: *CALL
: *          SCOPE          ;;SCOPE=IOT
  
```

```

SSCOPE:
1$: CKSWR          ;; TEST FOR CHANGE IN SOFT-SWR
   BIT          #BIT14,$SWR      ;; LOOP ON PRESENT TEST?
   BNE          $OVER           ;; YES IF SW14=1
: *****START OF CODE FOR THE XOR TESTER*****
$XTSTR: BR        6$           ;; IF RUNNING ON THE "XOR" TESTER CHANGE
                                ;; THIS INSTRUCTION TO A "NOP" (NOP=240)
                                ;; SAVE THE CONTENTS OF THE ERROR VECTOR
                                ;; SET FOR TIMEOUT
                                ;; TIME OUT ON XOR?
                                ;; RESTORE THE ERROR VECTOR
                                ;; GO TO THE NEXT TEST
                                ;; CLEAR THE STACK AFTER A TIME OUT
                                ;; RESTORE THE ERROR VECTOR
                                ;; LOOP ON THE PRESENT TEST
                                ;; TESTER*****
6$: *****END OF CODE FOR THE XOR TESTER*****
2$: TSTB          $ERFLG        ;; HAS AN ERROR OCCURRED?
   BEQ          $SVLAD         ;; BR IF NO
   BIT          #BIT09,$SWR     ;; LOOP ON ERROR?
   BEQ          4$            ;; BR IF NO
7$: MOV          $LPERR,$LPADR  ;; SET LOOP ADDRESS TO LAST SCOPE
   BR          $OVER
4$: CLRB          $ERFLG        ;; ZERO THE ERROR FLAG
$SVLAD: INCB      $STNM         ;; COUNT TEST NUMBERS
   MOVB        $STNM,$STESTN   ;; SET TEST NUMBER IN APT MAILBOX
   MOV         (SP),$LPADR     ;; SAVE SCOPE LOOP ADDRESS
   MOV         (SP),$LPERR     ;; SAVE ERROR LOOP ADDRESS
   CLR         $ESCAPE        ;; CLEAR THE ESCAPE FROM ERROR ADDRESS
   MOVB        #1,$SERMAX     ;; ONLY ALLOW ONE(1) ERROR ON NEXT TEST
$OVER: MOV        $STNM,$DISPLAY ;; DISPLAY TEST NUMBER
   MOV        $LPADR,(SP)     ;; FUDGE RETURN ADDRESS
   RTI                       ;; FIXES PS
  
```

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2371
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2376 012500 112767 000001 000236 SATY1: MOV  B1,SFFLG ;TO REPORT FATAL ERROR
2377 012506 112767 000001 000226 SATY3: MOV  B1,SMFLG ;TO TYPE A MESSAGE
2378 012514 000403          SATYC          ;
2379 012516 112767 000001 000220 SATY4: MOV  B1,SFFLG ;TO ONLY REPORT FATAL ERROR
2380 012524          SATYC          ;
2381 012524 010046          MOV  R0,-(SP) ;PUSH R0 ON STACK
2382 012526 010146          MOV  R1,-(SP) ;PUSH R1 ON STACK
2383 012530 105767 000206          TSTB SMFLG ;SHOULD TYPE A MESSAGE?
2384 012534 001450          BEQ   S$ ;IF NOT: BR
2385 012536 122767 000001 166342          CMPB 8APTENV,SENV ;OPERATING UNDER APT?
2386 012544 001031          BNE  S$ ;IF NOT: BR
2387 012546 132767 000100 166333          BITB 8APTPOOL,SENVH ;SHOULD SPOOL MESSAGE?
2388 012554 001425          BEQ   S$ ;IF NOT: BR
2389 012556 017600 000004          MOV  24(SP),R0 ;GET MESSAGE ADDRESS
2390 012562 062766 000002 000004          ADD  82,4(SP) ;BUMP RETURN ADDRESS
2391 012570 005767 166272          15: TST  SMSGTYPE ;SEE IF DONE W/ LAST XMISSION?
2392 012574 001375          BNE  15 ;IF NOT: WAIT
2393 012576 010067 166300          MOV  R0,SMSGAD ;PUT ADDRESS IN MAILBOX
2394 012602 105720          25: TSTB (R0)+ ;FIND END OF MESSAGE
2395 012604 001376          BNE  25
2396 012606 166700 166270          SUB  SMSGAD,R0 ;SUB START OF MESSAGE
2397 012612 006200          ASR  R0 ;GET MESSAGE LENGTH IN WORDS
2398 012614 010067 166264          MOV  R0,SMSG LGT ;PUT LENGTH IN MAILBOX
2399 012620 012767 000004 166240          MOV  84,SMSGTYPE ;TELL APT TO TAKE MESSAGE
2400 012626 000413          BR   S$
2401 012630 017667 000004 000016 35: MOV  24(SP),4$ ;PUT MSG ADDR IN JSR LINKAGE
2402 012636 062766 000002 000004          ADD  82,4(SP) ;BUMP RETURN ADDRESS
2403 012644 016746 165126          MOV  177776,-(SP) ;PUSH 177776 ON STACK
2404 012650 004767 000072          JSR  PC,STYPE ;CALL TYPE MACRO
2405 012654 000000          45: .WORD 0
2406 012656          55:
2407 012656 105767 000062          105: TSTB SFFLG ;SHOULD REPORT FATAL ERROR?
2408 012662 001413          BEQ  125 ;IF NOT: BR
2409 012664 005767 166216          TST  SENV ;RUNNING UNDER APT?
2410 012670 001410          BEQ  125 ;IF NOT: BR
2411 012672 005767 166170          115: TST  SMSGTYPE ;FINISHED LAST MESSAGE?
2412 012676 001375          BNE  115 ;IF NOT: WAIT
2413 012700 017667 000004 166162          MOV  24(SP),SFATAL ;GET ERROR #
2414 012706 005267 166154          INC  SMSGTYPE ;TELL APT TO TAKE ERROR
2415 012712 062766 000002 000004 125: ADD  82,4(SP) ;BUMP RETURN ADDRESS
2416 012720 105067 000020          CLRB SFFLG ;CLEAR FATAL FLAG
2417 012724 105067 000013          CLRB SLFLG ;CLEAR LOG FLAG
2418 012730 105067 000006          CLRB SMFLG ;CLEAR MESSAGE FLAG
2419 012734 012601          MOV  (SP)+,R1 ;POP STACK INTO R1
2420 012736 012600          MOV  (SP)+,R0 ;POP STACK INTO R1
2421 012740 000207          RTS  PC ;RETURN
2422 012742 000          SMFLG: .BYTE 0
2423 012743 000          SLFLG: .BYTE 0 ;LOG FLAG
2424 012744 000          SFFLG: .BYTE 0 ;FATAL FLAG
2425
2426 012746          .EVEN

```

C06

.MAIN. MACY11 27(732) 02-NOV-76 16:15 PAGE 58  
DZDLDA.P11 APT COMMUNICATIONS ROUTINE

SEQ 0067

7  
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000200  
000001  
000100  
000040

APTSIZE=200  
APTENV=001  
APTPOOL=100  
APTCSUP=040

012746  
012752  
012754  
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012762  
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012900

.SBTTL TYPE ROUTINE

\*\*\*\*\*  
\*ROUTINE TO TYPE ASCIZ MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.  
\*THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.  
\*NOTE1: SNULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.  
\*NOTE2: SFILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.  
\*NOTE3: SFILLC CONTAINS THE CHARACTER TO FILL AFTER.  
\*

\*CALL:  
\*1) USING A TRAP INSTRUCTION  
\* TYPE ,MESADR ;;MESADR IS FIRST ADDRESS OF AN ASCIZ STRING  
\*OR  
\* TYPE  
\* MESADR  
\*

012746 105767 166105  
012752 100002  
012754 000000  
012756 000430  
012760 010046  
012762 017600 000002  
012766 122767 000001 166112  
012774 001011  
012776 132767 000100 166103  
012778 001405  
012780 010067 000004  
012782 004767 177470  
012784 000000  
012786 132767 000040 166061  
012788 001003  
012790 112046  
012792 001005  
012794 005726  
012796 012600  
012798 062716 000002  
012800 000002  
012802 122716 000011  
012804 001430  
012806 122716 000200  
012808 001006  
012810 005726  
012812 104401  
012814 001063  
012816 105067 000130  
012818 000755  
012820 004767 000056  
012822 126726 165750  
012824 001350  
012826 016746 165740  
012828  
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STYPE: TSTB STPFLG  
BPL 1S  
HALT  
BR 3S  
1S: MOV RO, -(SP)  
MOV @2(SP), RO  
CMPB @APTENV, SENV  
BNE 62S  
BITB @APTSPool, SENVM  
BEQ 62S  
MOV RO, 61S  
JSR PC, SATY3  
61S: .WORD 0  
62S: BITB @APTCSUP, SENVM  
BNE 60S  
2S: MOVB (RO)+, -(SP)  
BNE 4S  
TST (SP)+  
60S: MOV (SP)+, RO  
3S: ADD @2, (SP)  
RTI  
4S: CMPB @HT, (SP)  
BEQ 8S  
CMPB @CRLF, (SP)  
BNE 5S  
TST (SP)+  
TYPE  
SCRLF  
CLRB SCHARCNT  
BR 2S  
5S: JSR PC, STYPEC  
6S: CMPB @FILLC, (SP)+  
BNE 2S  
MOV SNULL, -(SP)  
7S: DECB 1(SP)  
BLT 6S  
JSR PC, STYPEC

;; IS THERE A TERMINAL?  
;; BR IF YES  
;; HALT HERE IF NO TERMINAL  
;; LEAVE  
;; SAVE RO  
;; GET ADDRESS OF ASCIZ STRING  
;; RUNNING IN APT MODE  
;; NO GO CHECK FOR APT CONSOLE  
;; SPOOL MESSAGE TO APT  
;; NO GO CHECK FOR CONSOLE  
;; SETUP MESSAGE ADDRESS FOR APT  
;; SPOOL MESSAGE TO APT  
;; MESSAGE ADDRESS  
;; APT CONSOLE SUPPRESSED  
;; YES, SKIP TYPE OUT  
;; PUSH CHARACTER TO BE TYPED ONTO STACK  
;; BR IF IT ISN'T THE TERMINATOR  
;; IF TERMINATOR POP IT OFF THE STACK  
;; RESTORE RO  
;; ADJUST RETURN PC  
;; RETURN  
;; BRANCH IF <HT>  
;; BRANCH IF NOT <CRLF>  
;; POP <CR><LF> EQUIV  
;; TYPE A CR AND LF  
;; CLEAR CHARACTER COUNT  
;; GET NEXT CHARACTER  
;; GO TYPE THIS CHARACTER  
;; IS IT TIME FOR FILLER CHARS.?  
;; IF NO GO GET NEXT CHAR.  
;; GET # OF FILLER CHARS. NEEDED  
;; AND THE NULL CHAR.  
;; DOES A NULL NEED TO BE TYPED?  
;; BR IF NO--GO POP THE NULL OFF OF STACK  
;; GO TYPE A NULL

```

013126 105367 000072          DECB  $CHARCNT      ;; DO NOT COUNT AS A COUNT
013132 000770                BR      7$          ;; LOOP

; HORIZONTAL TAB PROCESSOR

013134 112716 000040          BS:   MOVB  8'(SP)      ;; REPLACE TAB WITH SPACE
013140 004767 000014          9$:   JSR  PC,$TYPEC   ;; TYPE A SPACE
013144 132767 000007 000052  BITB  8'$CHARCNT     ;; BRANCH IF NOT AT
013152 001372                BNE  9$            ;; TAB STOP
013154 005726                TST  (SP)+          ;; POP SPACE OFF STACK
013156 000724                BR   2$            ;; GET NEXT CHARACTER
013160 105777 165664          $TYPEC: TSTB 2$TPS    ;; WAIT UNTIL PRINTER IS READY
013164 100375                BPL  $TYPEC
013166 116677 000002 165656  MOVB  2(SP),2$TPB    ;; LOAD CHAR TO BE TYPED INTO DATA REG.
013174 122766 000015 000002  CMPB  8CR,2(SP)     ;; IS CHARACTER A CARRIAGE RETURN?
013202 001003                BNE  1$            ;; BRANCH IF NO
013204 105067 000014          CLRB  $CHARCNT     ;; YES--CLEAR CHARACTER COUNT
013210 000406                BR   $TYPEX        ;; EXIT
013212 122766 000012 000002  1$:   CMPB  8LF,2(SP)   ;; IS CHARACTER A LINE FEED?
013220 001402                BEQ  $TYPEX        ;; BRANCH IF YES
013222 105227                INCB  (PC)+        ;; COUNT THE CHARACTER
013224 000000          $CHARCNT: .WORD 0 ;; CHARACTER COUNT STORAGE
013226 000207          $TYPEX: RTS   PC

```

.SBTTL BINARY TO OCTAL (ASCII) AND TYPE

```

; *****
; THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 6-DIGIT
; OCTAL (ASCII) NUMBER AND TYPE IT.
; $TYPOS---ENTER HERE TO SETUP SUPPRESS ZEROS AND NUMBER OF DIGITS TO TYPE
; CALL:
;     MOV    NUM,-(SP)      ;; NUMBER TO BE TYPED
;     TYPOS  ;; CALL FOR TYPEOUT
;     .BYTE  N              ;; N=1 TO 6 FOR NUMBER OF DIGITS TO TYPE
;     .BYTE  M              ;; M=1 OR 0
;                               ;; 1=TYPE LEADING ZEROS
;                               ;; 0=SUPPRESS LEADING ZEROS

```

#STYPON---ENTER HERE TO TYPE OUT WITH THE SAME PARAMETERS AS THE LAST #TYPOS OR \$TYPOC

```

; CALL:
;     MOV    NUM,-(SP)      ;; NUMBER TO BE TYPED
;     TYPON  ;; CALL FOR TYPEOUT

```

#STYPOC---ENTER HERE FOR TYPEOUT OF A 16 BIT NUMBER

```

; CALL:
;     MOV    NUM,-(SP)      ;; NUMBER TO BE TYPED
;     TYPOC  ;; CALL FOR TYPEOUT

```

```

013230 017646 000000          $TYPOS: MOV  2(SP),-(SP)    ;; PICKUP THE MODE
013234 116667 000001 000211  MOVB  1(SP),8OFILL  ;; LOAD ZERO FILL SWITCH
013242 112667 000207          MOVB  (SP)+,8OMODE+1 ;; NUMBER OF DIGITS TO TYPE
013246 062716 000002          ADD   82,(SP)      ;; ADJUST RETURN ADDRESS
013252 000406                BR   $TYPON
013254 112767 000001 000171  $TYPOC: MOVB  81,8OFILL  ;; SET THE ZERO FILL SWITCH
013262 112767 000006 000165  MOVB  86,8OMODE+1  ;; SET FOR SIX(6) DIGITS

```

0544	013270	112767	000005	000154	STYPON: MOV	#5, SOCNT	:: SET THE ITERATION COUNT
0545	013276	010346			MOV	R3, -(SP)	:: SAVE R3
0546	013300	010446			MOV	R4, -(SP)	:: SAVE R4
0547	013302	010546			MOV	R5, -(SP)	:: SAVE R5
0548	013304	116704	000145		MOV	\$OMODE+1, R4	:: GET THE NUMBER OF DIGITS TO TYPE
0549	013310	005404			NEG	R4	
0550	013312	062704	000006		ADD	#6, R4	:: SUBTRACT IT FOR MAX. ALLOWED
0551	013316	110467	000132		MOV	R4, \$OMODE	:: SAVE IT FOR USE
0552	013322	116704	000125		MOV	\$OFILL, R4	:: GET THE ZERO FILL SWITCH
0553	013326	016605	000012		MOV	12(SP), R5	:: PICKUP THE INPUT NUMBER
0554	013332	005003			CLR	R3	:: CLEAR THE OUTPUT WORD
0555	013334	006105		15:	ROL	R5	:: ROTATE MSB INTO "C"
0556	013336	000404			BR	35	:: GO DO MSB
0557	013340	006105		25:	ROL	R5	:: FORM THIS DIGIT
0558	013342	006105			ROL	R5	
0559	013344	006105			ROL	R5	
0560	013346	010503			MOV	R5, R3	
0561	013350	006103		35:	ROL	R3	:: GET LSB OF THIS DIGIT
0562	013352	105367	000076		DECB	\$OMODE	:: TYPE THIS DIGIT?
0563	013356	100016			BPL	75	:: BR IF NO
0564	013360	042703	177770		BIC	#177770, R3	:: GET RID OF JUNK
0565	013364	001002			BNE	45	:: TEST FOR 0
0566	013366	005704			TST	R4	:: SUPPRESS THIS 0?
0567	013370	001403			BEQ	55	:: BR IF YES
0568	013372	005204		45:	INC	R4	:: DON'T SUPPRESS ANYMORE 0'S
0569	013374	052703	000060		BIS	#'0, R3	:: MAKE THIS DIGIT ASCII
0570	013400	052703	000040	55:	BIS	#' , R3	:: MAKE ASCII IF NOT ALREADY
0571	013404	110367	000040		MOV	R3, #5	:: SAVE FOR TYPING
0572	013410	104401	013450		TYPE	#5	:: GO TYPE THIS DIGIT
0573	013414	105367	000032	75:	DECB	\$OCNT	:: COUNT BY 1
0574	013420	003347			BGT	25	:: BR IF MORE TO DO
0575	013422	002402			BLT	65	:: BR IF DONE
0576	013424	005204			INC	R4	:: INSURE LAST DIGIT ISN'T A BLANK
0577	013426	000744			BR	25	:: GO DO THE LAST DIGIT
0578	013430	012605		65:	MOV	(SP)+, R5	:: RESTORE R5
0579	013432	012604			MOV	(SP)+, R4	:: RESTORE R4
0580	013434	012603			MOV	(SP)+, R3	:: RESTORE R3
0581	013436	016666	000002	000004	MOV	2(SP), 4(SP)	:: SET THE STACK FOR RETURNING
0582	013444	012616			MOV	(SP)+, (SP)	
0583	013446	000002			RTI		:: RETURN
0584	013450	000		85:	.BYTE	0	:: STORAGE FOR ASCII DIGIT
0585	013451	000			.BYTE	0	:: TERMINATOR FOR TYPE ROUTINE
0586	013452	000		SOCNT:	.BYTE	0	:: OCTAL DIGIT COUNTER
0587	013453	000		SOFILL:	.BYTE	0	:: ZERO FILL SWITCH
0588	013454	000000		SOMODE:	.WORD	0	:: NUMBER OF DIGITS TO TYPE
0589							



```

2646 013664 021627 000060      CMP      (SP),#60      ;; CHAR < 0?
2647 013670 002420      BLT      18$          ;; BRANCH IF YES
2648 013672 021627 000067      CMP      (SP),#67      ;; CHAR > 7?
2649 013676 003015      BGT      18$          ;; BRANCH IF YES
2650 013700 042726 000060      BIC      #60,(SP)+     ;; STRIP-OFF ASCII
2651 013704 005766 000002      TST      2(SP)        ;; IS THIS THE FIRST CHAR
2652 013710 001403      BEQ      17$          ;; BRANCH IF YES
2653 013712 006316      ASL      (SP)         ;; NO, SHIFT PRESENT
2654 013714 006316      ASL      (SP)         ;; CHAR OVER TO MAKE
2655 013716 006316      ASL      (SP)         ;; ROOM FOR NEW ONE.
2656 013720 005266 000002      17$: INC      2(SP)        ;; KEEP COUNT OF CHAR
2657 013724 056616 177776      BIS      -2(SP),(SP)  ;; SET IN NEW CHAR
2658 013730 000707      BR       7$           ;; GET THE NEXT ONE
2659 013732 104401 001062      18$: TYPE   $QUES     ;; TYPE ?(CR)(LF)
2660 013736 000720      BR       20$          ;; SIMULATE CONTROL-U
2661
2662
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2664
2665      ;; *****
2666      ;; THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY
2667      ;; *CALL:
2668      ;;      RDCHR          ;; INPUT A SINGLE CHARACTER FROM THE TTY
2669      ;;      RETURN HERE   ;; CHARACTER IS ON THE STACK
2670      ;;
2671
2672 013740 011646      SRDCHR: MOV      (SP),-(SP)  ;; PUSH DOWN THE PC
2673 013742 016666 000004 000002      MOV      4(SP),2(SP)    ;; SAVE THE PS
2674 013750 105777 165070      1$: TSTB   2$TKS        ;; WAIT FOR
2675 013754 100375      BPL      1$           ;; A CHARACTER
2676 013756 117766 165064 000004      MOVB   2$TKB,4(SP)     ;; READ THE TTY
2677 013764 042766 177600 000004      BIC      #1C(177),4(SP) ;; GET RID OF JUNK IF ANY
2678 013772 026627 000004 000023      CMP      4(SP),#23     ;; IS IT A CONTROL-5?
2679 014000 001013      BNE      3$           ;; BRANCH IF NO
2680 014002 105777 165036      2$: TSTB   2$TKS        ;; WAIT FOR A CHARACTER
2681 014006 100375      BPL      2$           ;; LOOP UNTIL ITS THERE
2682 014010 117746 165032      MOVB   2$TKB,-(SP)     ;; GET CHARACTER
2683 014014 042716 177600      BIC      #1C177,(SP)   ;; MAKE IT 7-BIT ASCII
2684 014020 022627 000021      CMP      (SP)+,#21     ;; IS IT A CONTROL-0?
2685 014024 001366      BNE      2$           ;; IF NOT DISCARD IT
2686 014026 000750      BR       1$           ;; YES, RESUME
2687 014030 026627 000004 000140      3$: CMP      4(SP),#140  ;; IS IT UPPER CASE?
2688 014036 002407      BLT      4$           ;; BRANCH IF YES
2689 014040 026627 000004 000175      CMP      4(SP),#175   ;; IS IT A SPECIAL CHAR?
2690 014046 003003      BGT      4$           ;; BRANCH IF YES
2691 014050 042766 000040 000004      BIC      #40,4(SP)    ;; MAKE IT UPPER CASE
2692 014056 000002      4$: RTI              ;; GO BACK TO USER
2693
2694      ;; *****
2695      ;; THIS ROUTINE WILL INPUT A STRING FROM THE TTY
2696      ;; *CALL:
2697      ;;      RDLIN          ;; INPUT A STRING FROM THE TTY
2698      ;;      RETURN HERE   ;; ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK
2699      ;;
2700      SRDLIN: MOV      R3,-(SP)  ;; SAVE R3
2701 014062 012703 014166      1$: MOV      #1TTYIN,R3  ;; GET ADDRESS
  
```

```

2702 014066 022703 014176      2S:  CMP      #STTYIN+8.,R3      ;; BUFFER FULL?
2703 014072 101405              BLOS     4S              ;; BR IF YES
2704 014074 104407              RDCMR                    ;; GO READ ONE CHARACTER FROM THE TTY
2705 014076 112613              MOV      (SP)+,(R3)      ;; GET CHARACTER
2706 014100 122713 000177      10S:  CMPB     #177,(R3)      ;; IS IT A RUBOUT
2707 014104 001003              BNE      3S              ;; SKIP IF NOT
2708 014106 104401 001062      4S:   TYPE     'QUES      ;; TYPE A '?'
2709 014112 000763              BR       1S              ;; CLEAR THE BUFFER AND LOOP
2710 014114 111367 000044      3S:   MOV      (R3),9S      ;; ECHO THE CHARACTER
2711 014120 104401 014164              TYPE     'S
2712 014124 122723 000015              CMPB     #15,(R3)+      ;; CHECK FOR RETURN
2713 014130 001356              BNE      2S              ;; LOOP IF NOT RETURN
2714 014132 105063 177777              CLRB     -1(R3)         ;; CLEAR RETURN (THE 15)
2715 014136 104401 001064              TYPE     'LF
2716 014142 012603              MOV      (SP)+,R3      ;; TYPE A LINE FEED
2717 014144 011646              MOV      (SP)-,(SP)     ;; RESTORE R3
2718 014146 016666 000004 000002      MOV      4(SP),2(SP)    ;; ADJUST THE STACK AND PUT ADDRESS OF THE
2719 014154 012766 014166 000004      MOV      #STTYIN,4(SP)  ;; FIRST ASCII CHARACTER ON IT
2720 014162 000002              RTI                    ;; RETURN
2721 014164 000              9S:   .BYTE    0              ;; STORAGE FOR ASCII CHAR. TO TYPE
2722 014165 000              .BYTE    0              ;; TERMINATOR
2723 014166 000010      STTYIN: .BLKB    8.      ;; RESERVE 8 BYTES FOR TTY INPUT
2724 014176 052536 005015 000      SCNTLU: .ASCIZ  /↑U/<15><12>  ;; CONTROL "U"
2725 014203 136 006507 000012      SCNTLG: .ASCIZ  /↑G/<15><12>  ;; CONTROL "G"
2726 014210 005015 053523 020122      SMSWR:  .ASCIZ  <15><12>/SWR = /
2727 014216 020075 000
2728 014221 040 047040 053505      SNEW:   .ASCIZ  / NEW = /
2729 014226 036440 000040
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.SBTTL TRAP DECODER

```

;*****
;THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
;AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
;OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
;GO TO THAT ROUTINE.
  
```

```

STRAP:  MOV    RD, -(SP)           ;; SAVE RD
        MOV    2(SP), RD          ;; GET TRAP ADDRESS
        TST   -(RD)              ;; BACKUP BY 2
        MOVB  (RD), RD           ;; GET RIGHT BYTE OF TRAP
        ASL   RD                 ;; POSITION FOR INDEXING
        MOV   STRPAD(RD), RD      ;; INDEX TO TABLE
        RTS   RD                 ;; GO TO ROUTINE
  
```

;; THIS IS USE TO HANDLE THE "GETPRI" MACRO

```

STRAP2: MOV    (SP), -(SP)        ;; MOVE THE PC DOWN
        MOV    4(SP), 2(SP)      ;; MOVE THE PSW DOWN
        RTI                               ;; RESTORE THE PSW
  
```

.SBTTL TRAP TABLE

```

;THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
;BY THE "TRAP" INSTRUCTION.
  
```

	ROUTINE		
STRPAD:	WORD	STRAP2	
	\$TYPE	;; CALL=TYPE	TRAP+1(104401) TTY TYPEOUT ROUTINE
	\$TYPOC	;; CALL=TYPOC	TRAP+2(104402) TYPE OCTAL NUMBER (WITH LEADING ZEROS)
	\$TYPOS	;; CALL=TYPOS	TRAP+3(104403) TYPE OCTAL NUMBER (NO LEADING ZEROS)
	\$TYPON	;; CALL=TYPON	TRAP+4(104404) TYPE OCTAL NUMBER (AS PER LAST CALL)
	SGTSWR	;; CALL=GTSWR	TRAP+5(104405) GET SOFT-SWR SETTING
	SCKSMR	;; CALL=CKSMR	TRAP+6(104406) TEST FOR CHANGE IN SOFT-SWR
	SRDCHR	;; CALL=RDCHR	TRAP+7(104407) TTY TYPEIN CHARACTER ROUTINE
	SRDLIN	;; CALL=ROLIN	TRAP+10(104410) TTY TYPEIN STRING ROUTINE

```

014232 010046
014234 016600 000002
014240 005740
014242 111000
014244 006300
014246 016000 014266
014252 000200
  
```

```

014254 011646
014256 016666 000004 000002
014264 000002
  
```

```

014266 014254
014270 012746
014272 013254
014274 013230
014276 013270
014300 013526
014302 013456
014304 013740
014306 014060
  
```

# K06

```
2775 .SBTTL ECHO TEST
2776 ;;*****
2777 ;*THIS ROUTINE WILL ECHO ANY CHARACTER TYPED
2778 ;*AT THE CONSOLE
2779 ;*THE TEST IS HALTED BY TYPING A CONTROL-C
2780 ;*TEST CAN BE RESTARTED AFTER HALTING BY JUST CONTINUING
2781 ;;*****
2782 ECHO:
2783 014310 000005 RESET ;CLEAR EVERYTHING
2784 014312 112777 000052 166014 MOVB #'* ,ACTBUF ;TRANSMIT PROMPT "*"
2785 014320 105777 166002 2S: TSTB ACTCSR ;WAIT FOR INPUT
2786 014324 100375 BPL 2S
2787 014326 117777 165776 166000 MOVB ACTBUF,ACTBUF ;ECHO INPUT
2788 014334 017700 165770 MOV ACTBUF,RO ;STORE INPUT
2789 014340 100023 BPL 5S ;BR IF "ERROR" NOT SET
2790 014342 052701 010000 BIS #BIT12,R1 ;SET PARITY ERROR TEST MASK
2791 014346 030100 BIT R1,RO ;CHECK FOR PARITY ERROR FLAG
2792 014350 001403 BEQ 3S ;BR IF NOT SET
2793 014352 004767 000056 JSR PC,MSG ;REPORT PARITY ERROR
2794 014356 014462 MPAR
2795 014360 006301 3S: ASL R1 ;SHIFT MASK TO TEST "FR" FLAG
2796 014362 030100 BIT R1,RO ;TEST FOR FRAMING ERROR FLAG
2797 014364 001403 BEQ 4S ;BR IF NOT SET
2798 014366 004767 000042 JSR PC,MSG ;REPORT FRAMING ERROR
2799 014372 014473 MFR
2800 014374 006301 4S: ASL R1 ;SHIFT MASK TO TEST "OR" FLAG
2801 014376 030100 BIT R1,RO ;TEST FOR OVERFLOW ERROR
2802 014400 001403 BEQ 5S ;BR IF NOT SET
2803 014402 004767 000026 JSR PC,MSG ;REPORT OVERFLOW ERROR
2804 014406 014505 MOR
2805 014410 042700 000200 5S: BIC #BIT7,RO ;CLEAR ANY PARITY BIT
2806 014414 022700 000003 CMP #3,RO ;WAS INPUT CONTROL-C
2807 014420 001337 BNE 2S ;BR IF NOT
2808 014422 004767 000006 JSR PC,MSG ;REPORT PROGRAM STOP
2809 014426 014520 MSTOP
2810 014430 000000 HALT ;END OF TEST HALT
2811 014432 000726 BR ECHO ;AFTER END OF TEST HALT
2812 ; PRESS CONTINUE TO RESTART ECHO TEST
2813
2814 014434 013600 MSG: MOV ACT(SP)+,RO ;PICK UP MESSAGE POINTER
2815 014436 062746 000002 ADD #2,-(SP) ;ADJUST RETURN PC
2816 014442 105777 165664 WAIT: TSTB ACTCSR ;WAIT FOR XMIT DONE
2817 014446 100375 BPL WAIT
2818 014450 112077 165660 MOVB (RO)+,ACTBUF ;SEND CHARACTER
2819 014454 105710 TSTB (RO) ;IS THIS END OF MESSAGE?
2820 014456 001371 BNE WAIT ;BR IF NOT
2821 014460 000207 RTS ;RETURN
2822
2823 014462 005015 040520 044522 MPAR: .ASCIZ <CR><LF>/PARITY/
2824 014470 054524 000
2825 014473 015 043012 040522 MFR: .ASCIZ <CR><LF>/FRAMING/
2826 014500 044515 043516 000
2827 014505 015 047412 042526 MOR: .ASCIZ <CR><LF>/OVERFLOW/
2828 014512 043122 047514 000127
2829 014520 005015 052123 050117 MSTOP: .ASCIZ <CR><LF>/STOP/
2830 014526 000
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014530

.EVEN

.SBTTL TERMINAL OUTPUT TEST

```

;*****
;THIS ROUTINE WILL OUTPUT ALL WRITABLE CHARACTERS FOR THE
;THE OCTAL CODE 040 --> 377
;32 CHARACTERS ARE PRINTED ON EACH LINE
;THE PATTERN IS REPEATED EVERY THREE LINES
;*****
    
```

```

OUTTST: MOV     #40,R1           ;LOAD FIRST WRITABLE CHARACTER
1$:     MOV     #40,R0           ;LOAD CHAR COUNT PER LINE
2$:     TSTB    @CTCSR           ;WAIT FOR DONE
        BPL     2$
        MOV     R1,@CTBUF        ;TRANSMIT A CHARACTER
        INCB   R1               ;INCREMENT CHARACTER CODE
        DEC    R0               ;DECREMENT CHAR COUNT
        BNE    2$              ;BR IF LINE NOT COMPLETE
        JSR    PC,MSG           ;SSUE CR,LINE FEED

        SCRLF
        TSTB   @CRCSR           ;ANY CHARACTER RECEIVED?
        BMI    3$              ;BR IF YES
        BIT    #BIT7,R1         ;FINISHED ONE PASS OF WRITABLE CHARACTERS?
        BNE    OUTTST          ;BR IF YES
        BR     1$              ;IF NOT WRITE NEXT LINE

3$:     CLR     @CRBUF          ;CLEAR RECEIVER
        HALT
        BR     OUTTST          ;RESTART TEST IF CONTINUED
    
```

```

014530 012701 000040
014534 012700 000040
014540 105777 165566
014544 100375
014546 010177 165562
014552 105201
014554 005300
014556 001370
014560 004767 177650
014564 001063
014566 105777 165534
014572 100404
014574 032701 000200
014600 001353
014602 000754
014604 005077 165520
014610 000000
014612 000746
    
```

2865						
2866						
2867	014614	040503	020116	047516	EM1:	.ASCIZ /CAN NOT ACCESS TCSR/
2868	014622	020124	041501	042503		
2869	014630	051523	052040	051503		
2870	014636	000122				
2871	014640	040503	020116	047516	EM2:	.ASCIZ /CAN NOT ACCESS TBUF/
2872	014646	020124	041501	042503		
2873	014654	051523	052040	052502		
2874	014662	000106				
2875	014664	041524	051123	042040	EM3:	.ASCIZ /TCSR DONE NOT CLEARED WITH TBUF FULL/
2876	014672	047117	020105	047516		
2877	014700	020124	046103	040505		
2878	014706	042522	020104	044527		
2879	014714	044124	052040	052502		
2880	014722	020106	052506	046114		
2881	014730	000				
2882	014731	124	051503	020122	EM4:	.ASCIZ /TCSR DONE NOT SET/
2883	014736	047504	042516	047040		
2884	014744	052117	051440	052105		
2885	014752	000				
2886	014753	124	051503	020122	EM5:	.ASCIZ /TCSR DONE NOT SET WITH RESET/
2887	014760	047504	042516	047040		
2888	014766	052117	051440	052105		
2889	014774	053440	052111	020110		
2890	015002	042522	042523	000124		
2891	015010	040503	020116	047516	EM6:	.ASCIZ /CAN NOT ACCESS RCSR/
2892	015016	020124	041501	042503		
2893	015024	051523	051040	051503		
2894	015032	000122				
2895	015034	040503	020116	047516	EM7:	.ASCIZ /CAN NOT ACCESS RBUF/
2896	015042	020124	041501	042503		
2897	015050	051523	051040	052502		
2898	015056	000106				
2899	015060	040503	020116	047516	EM10:	.ASCIZ /CAN NOT ACCESS LKS/
2900	015066	020124	041501	042503		
2901	015074	051523	046040	051513		
2902	015102	000				
2903	015103	102	052111	020060	EM11:	.ASCIZ /BITO OF TCSR NOT CLEAR AFTER RESET/
2904	015110	043117	052040	051503		
2905	015116	020122	047516	020124		
2906	015124	046103	040505	020122		
2907	015132	043101	042524	020122		
2908	015140	042522	042523	000124		
2909	015146	040503	020116	047516	EM12:	.ASCIZ /CAN NOT SET BITO OF TCSR/
2910	015154	020124	042523	020124		
2911	015162	044502	030124	047440		
2912	015170	020106	041524	051123		
2913	015176	000				
2914	015177	103	047101	047040	EM13:	.ASCIZ /CAN NOT CLEAR BITO OF TCSR/
2915	015204	052117	041440	042514		
2916	015212	051101	041040	052111		
2917	015220	020060	043117	052040		
2918	015226	051503	000122			
2919	015232	042522	042523	020124	EM14:	.ASCIZ /RESET DID NOT CLEAR BITO OF TCSR/
2920	015240	044504	020104	047516		

2921	015246	020124	046103	040505	
2922	015254	020122	044502	030124	
2923	015262	047440	020106	041524	
2924	015270	051123	000		
2925	015273	102	052111	020062	EM15: .ASCIZ /BIT2 OF TCSR NOT CLEAR AFTER RESET/
2926	015300	043117	052040	051503	
2927	015306	020122	047516	020124	
2928	015314	046103	040505	020122	
2929	015322	043101	042524	020122	
2930	015330	042522	042523	000124	
2931	015336	040503	020116	047516	EM16: .ASCIZ /CAN NOT SET BIT2 OF TCSR/
2932	015344	020124	042523	020124	
2933	015352	044502	031124	047440	
2934	015360	020106	041524	051123	
2935	015366	000			
2936	015367	103	047101	047040	EM17: .ASCIZ /CAN NOT CLEAR BIT2 OF TCSR/
2937	015374	052117	041440	042514	
2938	015402	051101	041040	052111	
2939	015410	020062	043117	052040	
2940	015416	051503	000122		
2941	015422	042522	042523	020124	EM20: .ASCIZ /RESET DID NOT CLEAR BIT2 OF TCSR/
2942	015430	044504	020104	047516	
2943	015436	020124	046103	040505	
2944	015444	020122	044502	031124	
2945	015452	047440	020106	041524	
2946	015460	051123	000		
2947	015463	102	052111	020066	EM21: .ASCIZ ;BIT6 OF TCSR NOT CLEAR AFTER RESET/
2948	015470	043117	052040	051503	
2949	015476	020122	047516	020124	
2950	015504	046103	040505	020122	
2951	015512	043101	042524	020122	
2952	015520	042522	042523	027524	
2953	015526	000			
2954	015527	130	044515	020124	EM22: .ASCIZ /XMIT INTERRUPT AT PRIORITY 7/
2955	015534	047111	042524	051122	
2956	015542	050125	020124	052101	
2957	015550	050040	044522	051117	
2958	015556	052111	020131	000067	
2959	015564	040503	020116	047516	EM23: .ASCIZ /CAN NOT SET BIT6 OF TCSR/
2960	015572	020124	042523	020124	
2961	015600	044502	033124	047440	
2962	015606	020106	041524	051123	
2963	015614	000			
2964	015615	103	047101	047040	EM24: .ASCIZ /CAN NOT CLEAR BIT6 OF TCSR/
2965	015622	052117	041440	042514	
2966	015630	051101	041040	052111	
2967	015636	020066	043117	052040	
2968	015644	051503	000122		
2969	015650	042522	042523	020124	EM25: .ASCIZ /RESET DID NOT CLEAR BIT6 OF TCSR/
2970	015656	044504	020104	047516	
2971	015664	020124	046103	040505	
2972	015672	020122	044502	033124	
2973	015700	047440	020106	041524	
2974	015706	051123	000		
2975	015711	102	052111	020066	EM26: .ASCIZ /BIT6 OF RCSR NOT CLEAR AFTER RESET/
2976	015716	043117	051040	051503	

2977	015724	020122	047516	020124	
2978	015732	046103	040505	020122	
2979	015740	043101	042524	020122	
2980	015746	042522	042523	000124	
2981	015754	041522	051126	044440	EM27: .ASCIZ /RCVR INTERRUPT WITH PRIORITY 7/
2982	015762	052116	051105	052522	
2983	015770	052120	053440	052111	
2984	015776	020110	051120	047511	
2985	016004	044522	054524	033440	
2986	016012	000			
2987	016013	103	047101	047040	EM30: .ASCIZ /CAN NOT SET BIT6 OF RCSR/
2988	016020	052117	051440	052105	
2989	016026	041040	052111	020066	
2990	016034	043117	051040	051503	
2991	016042	000122			
2992	016044	040503	020116	047516	EM31: .ASCIZ /CAN NOT CLEAR BIT6 OF RCSR/
2993	016052	020124	046103	040505	
2994	016060	020122	044502	033124	
2995	016066	047440	020106	041522	
2996	016074	051123	000		
2997	016077	103	047101	047040	EM32: .ASCIZ /CAN NOT CLEAR BIT6 OF RCSR WITH RESET/
2998	016104	052117	041440	042514	
2999	016112	051101	041040	052111	
3000	016120	020066	043117	051040	
3001	016128	051503	020122	044527	
3002	016134	044124	051040	051505	
3003	016142	052105	000		
3004	016145	102	052111	020066	EM33: .ASCIZ /BIT6 OF LKS NOT CLEAR AFTER RESET/
3005	016152	043117	046040	051513	
3006	016160	047040	052117	041440	
3007	016166	042514	051101	040440	
3008	016174	052106	051105	051040	
3009	016202	051505	052105	000	
3010	016207	114	051513	044440	EM34: .ASCIZ /LKS INTERRUPT WITH PRIORITY 7/
3011	016214	052116	051105	052522	
3012	016222	052120	053440	052111	
3013	016230	020110	051120	047511	
3014	016236	044522	054524	033440	
3015	016244	000			
3016	016245	103	047101	047040	EM35: .ASCIZ /CAN NOT SET BIT6 OF LKS/
3017	016252	052117	051440	052105	
3018	016260	041040	052111	020066	
3019	016266	043117	046040	051513	
3020	016274	000			
3021	016275	103	047101	047040	EM36: .ASCIZ /CAN NOT CLEAR BIT6 OF LKS/
3022	016302	052117	041440	042514	
3023	016310	051101	041040	052111	
3024	016316	020066	043117	046040	
3025	016324	051513	000		
3026	016327	122	051505	052105	EM37: .ASCIZ /RESET DID NOT CLEAR BIT6 OF LKS/
3027	016334	042040	042111	047040	
3028	016342	052117	041440	042514	
3029	016350	051101	041040	052111	
3030	016356	020066	043117	046040	
3031	016364	051513	000		
3032	016367	104	040525	020114	EM40: .ASCIZ /DUAL ADDRESSING ERROR/

3033	016374	042101	051104	051505	
3034	016402	044523	043516	042440	
3035	016410	051122	051117	000	
3036	016415	102	052111	020066	EM41: .ASCIZ /BIT6 OF LKS NOT SET AFTER RESET/
3037	016422	043117	046040	051513	
3038	016430	047040	052117	051440	
3039	016436	052105	040440	052106	
3040	016444	051105	051040	051505	
3041	016452	052105	000		
3042	016455	103	047101	047040	EM42: .ASCIZ /CAN NOT CLEAR BIT7 OF LKS/
3043	016462	052117	041440	042514	
3044	016470	051101	041040	052111	
3045	016476	020067	043117	046040	
3046	016504	051513	000		
3047	016507	102	052111	020067	EM43: .ASCIZ /BIT7 OF LKS DOES NOT SET/
3048	016514	043117	046040	051513	
3049	016522	042040	042517	020123	
3050	016530	047516	020124	042523	
3051	016536	000124			
3052	016540	052122	020103	047111	EM44: .ASCIZ /RTC INTERRUPT AT PRIORITY 7/
3053	016546	042524	051122	050125	
3054	016554	020124	052101	050040	
3055	016562	044522	051117	052111	
3056	016570	020131	000067		
3057	016574	052122	020103	047111	EM45: .ASCIZ /RTC INTERRUPTS WHEN DISABLED/
3058	016602	042524	051122	050125	
3059	016610	051524	053440	042510	
3060	016616	020116	044504	040523	
3061	016624	046102	042105	000	
3062	016631				EM47:
3063	016631	122	041524	044440	EM46: .ASCIZ /RTC INTERRUPT DID NOT OCCUR/
3064	016636	052116	051105	052522	
3065	016644	052120	042040	042111	
3066	016652	047040	052117	047440	
3067	016660	041503	051125	000	
3068	016665	122	041524	042040	EM50: .ASCIZ /RTC DOUBLE INTERRUPT/
3069	016672	052517	046102	020105	
3070	016700	047111	042524	051122	
3071	016706	050125	000124		
3072	016712	042522	042523	020124	EM51: .ASCIZ /RESET DID NOT INTERRUPT/
3073	016720	044504	020104	047516	
3074	016726	020124	047111	042524	
3075	016734	051122	050125	000124	
3076	016742	052122	020103	047111	EM52: .ASCIZ /RTC INTERRUPT DID NOT CLEAR WITH BIT7 OF LKS/
3077	016750	042524	051122	050125	
3078	016756	020124	044504	020104	
3079	016764	047516	020124	046103	
3080	016772	040505	020122	044527	
3081	017000	044124	041040	052111	
3082	017006	020067	043117	046040	
3083	017014	051513	000		
3084	017017	103	047514	045503	EM53: .ASCIZ /CLOCK REPEATABILITY/
3085	017024	051040	050105	040505	
3086	017032	040524	044502	044514	
3087	017040	054524	000		
3088	017043	130	044515	020124	EM54: .ASCIZ /XMIT INTERRUPTS WHEN DISABLED/

3089	017050	047111	042524	051122	
3090	017056	050125	051524	053440	
3091	017064	042510	020116	044504	
3092	017072	040523	046102	042105	
3093	017100	000			
3094	017101	130	044515	020124	EM56: .ASCIZ /XMIT INTERRUPTS AT PRIORITY 7/
3095	017106	047111	042524	051122	
3096	017114	050125	051524	040440	
3097	017122	020124	051120	047511	
3098	017130	044522	054524	033440	
3099	017136	000			
3100	017137	130	044515	020124	EM57: .ASCIZ /XMIT INTERRUPTS WITH ENABLE CLEAR/
3101	017144	047111	042524	051122	
3102	017152	050125	051524	053440	
3103	017160	052111	020110	047105	
3104	017166	041101	042514	041440	
3105	017174	042514	051101	000	
3106	017201				EM55:
3107	017201	130	044515	020124	EM60: .ASCIZ /XMIT DID NOT INTERRUPT/
3108	017206	044504	020104	047516	
3109	017214	020124	047111	042524	
3110	017222	051122	050125	000124	
3111	017230	046530	052111	051040	EM61: .ASCIZ /XMIT RE-INTERRUPTED/
3112	017236	026505	047111	042524	
3113	017244	051122	050125	042524	
3114	017252	000104			
3115	017254	047514	042101	047111	EM62: .ASCIZ /LOADING TBUF DID NOT CLEAR INTERRUPT/
3116	017262	020107	041124	043125	
3117	017270	042040	042111	047040	
3118	017276	052117	041440	042514	
3119	017284	051101	044440	052116	
3120	017312	051105	052522	052120	
3121	017320	000			
3122	017321	122	053103	020122	EM63: .ASCIZ /RCVR ACTIVE NOT SET/
3123	017326	041501	044524	042526	
3124	017334	047040	052117	051440	
3125	017342	052105	000		
3126	017345	122	053103	020122	EM64: .ASCIZ /RCVR DONE NEVER SET/
3127	017352	047504	042516	047040	
3128	017360	053105	051105	051440	
3129	017366	052105	000		
3130	017371	122	053103	020122	EM65: .ASCIZ /RCVR ACTIVE NOT CLEARED WITH DONE SET/
3131	017376	041501	044524	042526	
3132	017404	047040	052117	041440	
3133	017412	042514	051101	042105	
3134	017420	053440	052111	020110	
3135	017426	047504	042516	051440	
3136	017434	052105	000		
3137	017437	122	051505	052105	EM66: .ASCIZ /RESET DID NOT CLEAR RCVR DONE/
3138	017444	042040	042111	047040	
3139	017452	052117	041440	042514	
3140	017460	051101	051040	053103	
3141	017466	020122	047504	042516	
3142	017474	000			
3143	017475	122	051104	042440	EM67: .ASCIZ /RDR ENABLE DID NOT CLEAR RCVR DONE/
3144	017502	040516	046102	020105	

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SEQ 0082

3145	017510	044504	020104	047516	
3146	017516	020124	046103	040505	
3147	017524	020122	041522	051126	
3148	017532	042040	047117	000105	
3149	017540	042522	042101	047111	EM70: .ASCIZ /READING RBUF DID NOT CLEAR RCVR DONE/
3150	017546	020107	041122	043125	
3151	017554	042040	042111	047040	
3152	017562	052117	041440	042514	
3153	017570	051101	051040	053103	
3154	017576	020122	047504	042516	
3155	017604	000			
3156	017605	122	053103	020122	EM71: .ASCIZ /RCVR INTERRUPTS WITH ENABLE CLEAR/
3157	017612	047111	042524	051122	
3158	017620	050125	051524	053440	
3159	017626	052111	020110	047105	
3160	017634	041101	042514	041440	
3161	017642	042514	051101	000	
3162	017647	122	053103	020122	EM73: .ASCIZ /RCVR INTERRUPTS AT PRIORITY 7/
3163	017654	047111	042524	051122	
3164	017662	050125	051524	040440	
3165	017670	020124	051120	047511	
3166	017676	044522	054524	033440	
3167	017704	000			
3168	017705	122	053103	020122	EM74: .ASCIZ /RCVR INT RQST PASSED WITH ENABLE CLEAR/
3169	017712	047111	020124	050522	
3170	017720	052123	050040	051501	
3171	017726	042523	020104	044527	
3172	017734	044124	042440	040516	
3173	017742	046102	020105	046103	
3174	017750	040505	000122		
3175	017754				EM72:
3176	017754	041522	051126	042040	EM75: .ASCIZ /RCVR DID NOT INTERRUPT/
3177	017762	042111	047040	052117	
3178	017770	044440	052116	051105	
3179	017776	052522	052120	000	
3180	020003	122	053103	020122	EM76: .ASCIZ /RCVR RE-INTERRUPTED/
3181	020010	042522	044455	052116	
3182	020016	051105	052522	052120	
3183	020024	042105	000		
3184	020027	122	040505	044504	EM77: .ASCIZ /READING RBUF DID NOT CLEAR INTERRUPT/
3185	020034	043516	051040	052502	
3186	020042	020106	044504	020104	
3187	020050	047516	020124	046103	
3188	020056	040505	020122	047111	
3189	020064	042524	051122	050125	
3190	020072	000124			
3191	020074	042522	042523	020124	EM100: .ASCIZ /RESET DID NOT CLEAR RCVR INTERRUPT/
3192	020102	044504	020104	047516	
3193	020110	020124	046103	040505	
3194	020116	020122	041522	051126	
3195	020124	044440	052116	051105	
3196	020132	052522	052120	000	
3197	020137	047	051117	020047	EM101: .ASCIZ /'OR' FLAG DID NOT SET/
3198	020144	046106	043501	042040	
3199	020152	042111	047040	052117	
3200	020160	051440	052105	000	

3201	020165	047	051105	047522	EM102: .ASCIZ /'ERROR' NOT SET WITH 'OR' FLAG/
3202	020172	023522	047040	052117	
3203	020200	051440	052105	053440	
3204	020206	052111	020110	047447	
3205	020214	023522	043040	040514	
3206	020222	000107			
3207	020224	051102	040505	020113	EM103: .ASCIZ /BREAK DID NOT XMIT ALL ZEROES/
3208	020232	044504	020104	047516	
3209	020240	020124	046530	052111	
3210	020246	040440	046114	055040	
3211	020254	051105	042517	000123	
3212	020262	051102	040505	020113	EM104: .ASCIZ /BREAK DID NOT SET 'FR' ERROR/
3213	020270	044504	020104	047516	
3214	020276	020124	042523	020124	
3215	020304	043047	023522	042440	
3216	020312	051122	051117	000	
3217	020317	104	052101	020101	EM105: .ASCIZ /DATA COMPARE ERROR/
3218	020324	047503	050115	051101	
3219	020332	020105	051105	047522	
3220	020340	000122			
3221	020342	040504	040524	041440	EM106: .ASCIZ /DATA COMPARE ERROR WITH CABLE/
3222	020350	046517	040520	042522	
3223	020356	042440	051122	051117	
3224	020364	053440	052111	020110	
3225	020372	040503	046102	000105	
3226	020400	044524	042515	052517	EM107: .ASCIZ /TIMEOUT IN EXERCISER TEST/
3227	020406	020124	047111	042440	
3228	020414	042530	041522	051511	
3229	020422	051105	052040	051505	
3230	020430	000124			
3231	020432	047111	047503	051122	EM110: .ASCIZ /INCORRECT RECEIVE COUNT/
3232	020440	041505	020124	042522	
3233	020446	042503	053111	020105	
3234	020454	047503	047125	000124	
3235	020462	040504	040524	041440	EM111: .ASCIZ /DATA COMPARE ERROR IN EXERCISER/
3236	020470	046517	040520	042522	
3237	020476	042440	051122	051117	
3238	020504	044440	020116	054105	
3239	020512	051105	044503	042523	
3240	020520	000122			
3241	020522	051124	050101	041440	EM112: .ASCIZ /TRAP CATCHER/
3242	020530	052101	044103	051105	
3243	020536	000			
3244	020537	116	020117	046103	EM113: .ASCIZ /NO CLK INTERRUPT IN EXERCISER/
3245	020544	020113	047111	042524	
3246	020552	051122	050125	020124	
3247	020560	047111	042440	042530	
3248	020566	041522	051511	051105	
3249	020574	000			
3250					
3251	020575	124	051505	021524	DH1: .ASCIZ /TEST# ERROR# TCSR/
3252	020502	020040	042440	051122	
3253	020610	051117	020043	052040	
3254	020616	051503	000122		
3255	020622	042524	052123	020043	DH2: .ASCIZ /TEST# ERR PC TBUF/
3256	020630	020040	051105	020122	



3313						.EVEN	
3314	021306	005015			M2:	.ASCII	<CR><LF>
3315	021310	020040	042040	053105	M2A:	.ASCIZ	/ DEVICES UNDER TEST /
3316	021316	041511	051505	052440			
3317	021324	042116	051105	052040			
3318	021332	051505	020124	000040			
3319							
3320						.EVEN	
3321	021340	001072	001016	002312	DT1:	.WORD	STESTN,SERRPC,TCSR,0
3322	021346	000000					
3323	021350	001072	001016	002314	DT2:	.WORD	STESTN,SERRPC,TBUF,0
3324	021356	000000					
3325	021360	001072	001016	002306	DT6:	.WORD	STESTN,SERRPC,RCSR,0
3326	021366	000000					
3327	021370	001072	001016	002310	DT7:	.WORD	STESTN,SERRPC,RBUF,0
3328	021376	000000					
3329	021400	001072	001016	002346	DT10:	.WORD	STESTN,SERRPC,LKS,0
3330	021406	000000					
3331	021410	001072	001016	002306	DT40:	.WORD	STESTN,SERRPC,RCSR,\$B0ADR,0
3332	021416	001022	000000				
3333	021422	001072	001016	002346	DT53:	.WORD	STESTN,SERRPC,LKS,FIRST,SECND,0
3334	021430	006350	006352	000000			
3335	021436	001072	001016	002306	DT103:	.WORD	STESTN,SERRPC,RCSR,\$B0DAT,0
3336	021444	001026	000000				
3337	021450	001072	001016	002306	DT105:	.WORD	STESTN,SERRPC,RCSR,\$G0DAT,\$B0DAT,0
3338	021456	001024	001026	000000			
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3342	021506	011626	011630	000000			
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ACDM1 =	000000	234				
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ADDW1 =	000000	234				
ADDW10 =	000000	234				
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ADDW8 =	000000	234				
ADDW9 =	000000	234				
ADEVCT =	000000	234	240			
ADEVN =	000000	234	276			
ADR	003466	871#	874			
ADRTBL	002354	703#	709	869		
AENV =	000000	234	245			
AENVN =	000000	234	246			
AFATAL =	000000	234	237			
AMADR1 =	000000	234	262			
AMADR2 =	000000	234	266			
AMADR3 =	000000	234	269			
AMADR4 =	000000	234	272			
AMANS1 =	000000	234	256			
AMANS2 =	000000	234	264			
AMANS3 =	000000	234	267			
AMANS4 =	000000	234	270			
AMSGAD =	000000	234	242			
AMSGLC =	000000	234	243			
AMSGTY =	000000	234	236			
AMTYP1 =	000000	234	257			
AMTYP2 =	000000	234	265			
AMTYP3 =	000000	234	268			
AMTYP4 =	000000	234	271			
APASS =	000000	234	239			
APRIOR =	000000	234				
APTCSU =	000040	2430#	2463			
APTENV =	000001	2206	2385	2428#	2456	
APTSIZ =	000200	768	2427#			
APTSPO =	000100	2387	2429#	2458		
APTSZD	003172	775	777	802#		
ASWREG =	000000	234	247			
ATESTN =	000000	234	238			
AUNIT =	000000	234	241			
AUSMR =	000000	234	248			
AVECT1 =	000300	123#	234	273		
AVECT2 =	000000	234	274			
BDVECT	011630	2172#	2178#	3341		





EM14	015232	351	2919#
EM15	015273	356	2925#
EM16	015336	361	2931#
EM17	015367	366	2936#
EM2	014640	301	2871#
EM20	015422	371	2941#
EM21	015453	376	2947#
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EM23	015564	386	2959#
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EM26	015711	401	2975#
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EM30	016013	411	2987#
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EM33	016145	426	3004#
EM34	016207	431	3010#
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EM36	016275	441	3021#
EM37	016327	446	3026#
EM4	014731	311	2882#
EM40	016367	451	3032#
EM41	016415	456	3036#
EM42	016455	461	3042#
EM43	016507	466	3047#
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EM45	016574	476	3057#
EM46	016631	481	3063#
EM47	016631	486	3062#
EM5	014753	316	2886#
EM50	016665	491	3068#
EM51	016712	496	3072#
EM52	016742	501	3076#
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EM54	017043	511	3088#
EM55	017201	516	3106#
EM56	017101	521	3094#
EM57	017137	526	3100#
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EM60	017201	531	3107#
EM61	017230	536	3111#
EM62	017254	541	3115#
EM63	017321	546	3122#
EM64	017345	551	3126#
EM65	017371	556	3130#
EM66	017437	561	3137#
EM67	017475	566	3143#
EM7	015034	326	2895#
EM70	017540	571	3149#
EM71	017605	576	3156#
EM72	017754	581	3175#
EM73	017647	586	3162#
EM74	017705	591	3168#
EM75	017754	596	3176#











SMANS1	001116	256#																			
SMANS2	001122	264#																			
SMANS3	001126	267#																			
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SMADR	000502	183#																			
SMFLG	012742	2377#	2383	2418#	2422#																
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SMGLG	001104	243#	2398#																		
SMSTY	001066	236#	722#	2391	2399#	2411	2414#														
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SMTP2	001123	265#																			
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		1298#	1326#	1378#	1415#	1444#	1474#	1515#	1543#	1574#	1601#	1627#	1670#	1688#							
		1705#	1740#	1777#	1811#	1841#	1870#	1898#	1929#	1954#	1980#	2009#									
		2544#	2573#	2586#																	
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SOVER	012464	239#	767#	969	2130#	2131#	2149														
SPASS	001074	185#																			
SPASTH	000506	2317	2322#																		
SPOMER	012316	744	2284#	2311																	
SPMRDN	012150	2317#																			
SPMRNG	012304	2294	2302#																		
SPMRUP	012222	227#	2512	2659	2708	2724															
SOLES	001062	2672#	2772																		
SROCHR	013740	2774																			
SRODEC=	##### U	2700#	2773																		
SROLIN	014060	2774																			
SROOCT=	##### U	2693#																			
SROSZ =	000010	2148#																			
SRTNAD	011512	2774																			
SR2A =	##### U	2774																			
SSAVRE=	##### U	2293#	2303	2313#	2314#	2321#															
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SSCOPE	012326	144#	737	738	740	742	744	746	747	749	2129	2339	2596	2730							
SSETUP=	000137	144#																			
SSTUP =	177777	2349	2355	2361#																	
SSVLAD	012430	160#	165																		
SSVPC =	000500	125#	226	227	747	749	750	890	912	933	983	1000	1014	1029							
SSMR =	161000	1049	1093	1140	1182	1225	1270	1302	1330	1382	1419	1448	1478	1519							
		1547	1578	1605	1631	1674	1692	1709	1744	1781	1815	1845	1874	1902							
		1933	1958	1984	2013	2124	2130	2141	2147	2149	2332	2333	2334	2335							
		2340	2352	2354	2355	2356	2361	2364	2367	2370											
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		3341																			
STKB	001046	219#	2594	2605	2622	2676	2682														
STKS	001044	218#	2594	2603	2619	2643#	2674	2680													
STN =	000046	124#	886	890#	908	912#	929	933#	979	983#	996	1000#	1010	1014#							
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.EQUAT	10	90	12
.HEADE	10		
.KT11	10		
.SETUP	10	90	144
.SURNI	10		
.SACT1	10	100	156
.SAPT8	10	100	2310
.SAPTH	10	100	166
.SAPTY	10		
.SASTA	10		
.SCATC	10		
.SCHTA	10	110	189
.SDB20	10		
.SDB20	10		
.SDIV	10		
.SEOP	10	110	2120
.SERRO	10		
.SERRT	10	90	2231
.SMULT	10		
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.SRAND	10		
.SRDEE	10		
.SRDOC	10		
.SPREAD	10	110	2591
.SR2AZ	10		
.SSAVE	10		
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.SSCOP	10	100	2326
.SSIZE	10		
.SSUPR	10		
.STRAP	10	80	2733
.STYPB	10		
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.STYPE	10	80	2433
.STYPO	10	80	2512
.S40CA	10		
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 DZOLDA.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

SEQ 0099

ADD	712	714	785	818	820	837	861	868	872	878	2165	2253	2390	2402	2415
	2469	2540	2550	2630	2639	2815									
ASL	790	807	829	830	831	833	835	860	866	1287	2250	2251	2252	2653	2654
	2655	2745	2795	2800											
ASR	2397														
BEQ	769	773	808	840	1030	1050	1053	1071	1084	1095	1115	1129	1146	1164	1171
	1188	1206	1214	1226	1235	1253	1259	1279	1303	1313	1331	1383	1420	1449	1479
	1653	1660	1681	1700	1875	1903	1921	1934	1936	1969	1985	2001	2021	2042	2048
	2059	2088	2114	2140	2195	2218	2221	2255	2260	2273	2355	2357	2384	2388	2408
	2410	2459	2472	2507	2567	2610	2637	2652	2792	2797	2802				
BGE	854														
BGT	2134	2574	2649	2690											
BIC	816	1069	1085	1113	1131	1162	1204	1251	1277	1285	1311	1340	1363	1371	1393
	1411	1428	1435	1457	1460	1464	1519	1538	1547	1561	1578	1593	1605	1618	1639
	1648	1654	1662	1666	1682	1698	1709	1710	1720	1722	1730	1735	1737	1757	1762
	1767	1770	1791	1801	1826	1831	1860	1886	1892	1895	1917	1922	1926	1946	1973
	1976	2089	2131	2564	2606	2623	2650	2677	2683	2691	2805				
BIS	844	1063	1081	1107	1126	1155	1168	1197	1211	1244	1256	1280	1339	1362	1392
	1427	1456	1533	1554	1585	1608	1632	1675	1679	1693	1711	1728	1745	1754	1782
	1792	1821	1822	1851	1852	1877	1905	1910	1938	1939	1961	2027	2028	2029	2030
	2569	2570	2657	2790											
BISB	2242														
BIT	776	839	846	858	873	879	1031	1049	1052	1064	1070	1083	1094	1108	1114
	1128	1145	1156	1163	1170	1187	1198	1205	1213	1227	1234	1245	1252	1258	1281
	1304	1312	1332	1384	1421	1450	1480	1635	1652	1874	1884	1890	1902	1933	1935
	1947	1984	2022	2041	2060	2073	2087	2201	2217	2340	2356	2791	2796	2801	2858
BITB	768	772	774	2387	2458	2463	2495								
BLE	716	793	822	1505											
BLOS	2703														
BLT	2486	2575	2647	2688											
BMI	952	990	1309	1319	1645	1913	1991	2857							
BNE	735	758	775	777	847	859	874	880	897	919	943	954	957	968	970
	972	1032	1055	1065	1073	1098	1109	1118	1157	1199	1228	1246	1282	1284	1289
	1305	1321	1333	1385	1422	1451	1481	1495	1497	1636	1638	1647	1883	1885	1891
	1915	1948	1967	1993	1999	2023	2040	2061	2063	2071	2074	2156	2202	2207	2225
	2243	2265	2315	2341	2386	2392	2395	2412	2457	2464	2466	2474	2482	2496	2503
	2565	2602	2608	2628	2635	2642	2679	2685	2707	2713	2807	2820	2852	2859	
BPL	805	935	940	985	1342	1354	1365	1395	1430	1459	1488	1491	1502	1521	1553
	1584	1613	1678	1696	1719	1753	1790	1825	1855	1881	1908	1942	1945	1964	2214
	2451	2500	2563	2604	2620	2675	2681	2786	2789	2817	2848				
BPT	135														
BR	760	800	809	848	863	893	899	915	921	945	959	964	1003	1017	1036
	1057	1075	1100	1120	1149	1191	1238	1290	1344	1356	1405	1436	1465	1499	1510
	1527	1556	1566	1594	1619	1667	1721	1756	1768	1803	1832	1861	1970	2002	2075
	2083	2090	2212	2248	2275	2296	2320	2343	2349	2352	2359	2378	2400	2453	2479
	2489	2498	2505	2541	2556	2577	2631	2658	2660	2686	2709	2811	2860	2864	
CLR	721	722	723	724	725	726	733	747	767	780	781	802	827	845	933
	938	950	983	986	1317	1349	1483	1485	1486	1489	1493	1524	1611	1614	1633
	1634	1643	1676	1694	1714	1717	1750	1751	1785	1788	1820	1823	1827	1850	1879
	1909	1911	1940	1943	1960	1986	1989	2017	2019	2026	2031	2032	2035	2036	2038
	2069	2092	2097	2111	2115	2129	2154	2160	2241	2313	2365	2554	2617	2618	2862
	2360	2416	2417	2418	2478	2504	2714								
CLRB	715	734	757	792	821	853	895	917	1005	1019	1038	1151	1193	1240	1278
CMP	1283	1346	1358	1370	1400	1407	1438	1468	1504	1529	1539	1558	1568	1590	1596
	1621	1723	1731	1758	1771	1798	1805	1834	1864	1966	1998	2047	2070	2113	2155
	2224	2350	2601	2607	2627	2634	2646	2648	2678	2684	2687	2689	2702	2806	

# JOB

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 DZDLDA.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

SEQ 0100

CMPB	2206	2385	2456	2471	2473	2481	2502	2506	2609	2641	2706	2712			
DEC	1882	2132	2249	2851											
DECB	2485	2488	2562	2573											
EMT	16														
HALT	903	925	949	963	1061	1079	1105	1124	2176	2215	2226	2295	2319	2452	2810
	2863														
INC	787	788	797	798	806	849	862	865	953	1320	1492	1494	1496	1637	1646
	1914	1992	2039	2085	2096	2100	2112	2130	2197	2314	2414	2568	2576	2656	
INCB	1968	2000	2072	2086	2194	2361	2508	2850							
IOT	17														
JMP	151	152	153	855	881	2116	2147	2158	2161						
JSR	779	810	901	923	947	961	1059	1077	1103	1122	1143	1185	1232	1334	1351
	1390	1402	1423	1432	1452	1461	1525	1548	1563	1581	1606	1615	1715	1746	1764
	1786	1816	1828	1846	1857	2033	2142	2203	2209	2404	2461	2480	2487	2494	2645
	2793	2798	2803	2808	2853										
MOV	709	710	711	713	727	728	732	736	738	739	740	741	742	743	744
	745	746	749	750	753	754	755	756	761	763	764	765	770	782	783
	784	789	794	795	799	803	814	817	819	826	841	850	851	852	867
	869	870	871	876	877	890	891	904	912	913	926	1000	1001	1007	1014
	1015	1021	1033	1034	1041	1141	1142	1175	1183	1184	1218	1230	1231	1263	1270
	1271	1272	1273	1275	1276	1286	1292	1294	1295	1336	1337	1338	1350	1361	1372
	1387	1388	1389	1401	1412	1425	1426	1441	1454	1455	1471	1484	1498	1500	1507
	1522	1523	1532	1540	1550	1551	1562	1571	1579	1580	1591	1599	1609	1610	1624
	1697	1712	1713	1727	1736	1748	1749	1763	1774	1783	1784	1799	1802	1808	1818
	1819	1837	1848	1849	1853	1867	1878	1906	1962	1965	1971	1972	1988	1997	2003
	2004	2014	2015	2016	2018	2024	2025	2037	2068	2077	2078	2081	2082	2095	2135
	2139	2157	2163	2164	2170	2172	2173	2196	2198	2219	2222	2240	2245	2254	2259
	2264	2266	2270	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2302
	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2345	2346	2348	2351	2358
	2363	2364	2367	2368	2381	2382	2389	2393	2398	2399	2401	2403	2413	2419	2420
	2454	2455	2460	2468	2483	2537	2545	2546	2547	2553	2560	2578	2579	2580	2581
	2582	2614	2638	2643	2672	2673	2700	2701	2716	2717	2718	2719	2741	2742	2746
	2752	2753	2788	2814	2845	2846	2849								
MOVb	748	815	1912	2091	2200	2208	2362	2366	2376	2377	2379	2465	2493	2501	2538
	2539	2542	2543	2544	2548	2551	2552	2571	2605	2622	2676	2682	2705	2710	2744
	2784	2787	2818												
NEG	1503	2549													
NOP	987	1307	1343	1355	1366	1396	1404	1434	1463	1534	1555	1565	1586	1592	1617
	1729	1755	1766	1793	1800	1830	1859	2143	2144	2145					
RESET	988	1051	1082	1093	1127	1140	1169	1182	1212	1229	1257	1274	1306	1386	1431
	1631	1658	1674	1692	1744	1781	1815	1845	1856	1876	1904	1937	1959	1987	2013
	2043	2049	2067	2141	2783										
ROL	2555	2557	2558	2559	2561										
ROLB	832	834	836												
RTI	762	2093	2098	2101	2228	2318	2369	2470	2583	2644	2692	2720	2754		
RTS	717	2268	2421	2510	2747	2821									
RTT	2166														
SUB	791	1501	2171	2199	2396										
SWAB	828	838													
TRAP	2756	2765	2766	2767	2769	2771	2772	2773							
TST	786	796	804	892	896	914	918	942	956	967	969	971	1002	1016	1029
	1035	1054	1072	1097	1117	1225	1288	1302	1330	1382	1419	1448	1478	2020	2058
	2062	2213	2220	2272	2347	2391	2409	2411	2467	2475	2497	2566	2636	2651	2743
TSTB	934	939	951	984	989	1308	1318	1341	1353	1364	1394	1429	1458	1487	1490
	1520	1552	1583	1612	1644	1659	1677	1680	1695	1699	1718	1752	1789	1824	1854
	1880	1907	1920	1941	1944	1963	1990	2354	2383	2394	2407	2450	2499	2603	2619



	887	888	889	890	901	909	910	911	912	923	930	931	932	933	947
	961	980	981	982	983	997	998	999	1000	1011	1012	1013	1014	1026	1027
	1028	1029	1046	1047	1048	1049	1059	1077	1090	1091	1092	1093	1103	1122	1137
	1138	1139	1140	1179	1180	1181	1182	1222	1223	1224	1225	1267	1268	1269	1270
	1299	1300	1301	1302	1327	1328	1329	1330	1379	1380	1381	1382	1416	1417	1418
	1419	1445	1446	1447	1448	1475	1476	1477	1478	1516	1517	1518	1519	1544	1545
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	1672	1673	1674	1689	1690	1691	1692	1706	1707	1708	1709	1741	1742	1743	1744
	1778	1779	1780	1781	1812	1813	1814	1815	1842	1843	1844	1845	1871	1872	1873
	1874	1899	1900	1901	1902	1930	1931	1932	1933	1955	1956	1957	1958	1981	1982
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M08

.MAIN. MACY11 27(732) 02-NOV-76 16:15 PAGE 97  
DZDLDA.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

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