

DJ11

LOGIC TEST
MD-11-DZDJA-D

EP-DZDJA-D-DL-A

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FICHE 1 OF 1

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digital
MADE IN USA

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Category	Sub-Category	Count
Electronics	Smartphones	120
Electronics	Laptops	80
Electronics	Tablets	50
Electronics	Cameras	30
Electronics	Accessories	20
Home Goods	Kitchenware	90
Home Goods	Decor	60
Home Goods	Cleaning Supplies	40
Home Goods	Bedding	30
Home Goods	Furniture	20
Books & Media	Books	70
Books & Media	Movies	50
Books & Media	Music	30
Books & Media	Gaming	20
Books & Media	Stationery	10
Apparel	Clothing	100
Apparel	Footwear	60
Apparel	Accessories	40
Apparel	Hats	30
Apparel	Socks	20
Apparel	Underwear	10
Leisure	Travel	80
Leisure	Outdoor Gear	60
Leisure	Entertainment	40
Leisure	Leisure Wear	30
Leisure	Footwear	20
Leisure	Accessories	10

YTR-ML22-410A-1000-- Distribution to MEI-4, slot 134

/20110223-4-201001ES,2001(F900;2004),JMA2100DJ00,S,43423 Date 13-Oct-76 15:13:22 Monitor IPC-D 5070 [1A3] #START#

386672984828667895723-517898788562898823956-986-37958799018295789010345-228046-196-9PC+235562991233-5578971

XTC:MLB--10A. [ESE-- distribution to TESL--], slot 134

/3877023-1030000IES,20111003;200410JUL2100DJM0eSe43423 Date 13-Oct-76 15:13:22 Monitor IPC-D 5078 [1A3] #START#

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c01

The image displays a intricate geometric design, likely a woodcut or a digital print. It consists of a dense arrangement of small, black, diamond-shaped tiles. A series of sharp, V-shaped notches have been carved into the surface, creating a variety of polygonal shapes. On the left side, there are large, irregular notches. In the center, a prominent V-shaped cut creates a large triangular opening. To the right, another deep V-shaped cut is visible. The pattern is set against a plain white background.

-FTEB Version 6 (100344) Running on MTA1
+S237+ Date 09-185 TOM (460,2784) Job DZDJDG Sub. 23 Date 13-Oct-76 15:13:22 Monitor IPO-D 5073 (1A3) +START+
Request created: 13-Oct-76 14:51:19 X TO:ML21-4:DAVIES -- distribution to ML21-4, slot 134

File will be renamed to 10571 protection

D01

The image displays a dense, abstract pattern composed of numerous small, black, geometric shapes. These shapes include various types of squares, rectangles, and triangles, as well as more complex forms like stylized letters and arrows. The arrangement of these shapes creates a sense of depth and movement, with some elements appearing to overlap or be layered. The overall effect is reminiscent of a digital or abstract artwork, possibly a fractal or a complex algorithmic design.

LPTSP, Version 6 (100344) Running on MTA1
+START+ User DAVIES, TOM [400.2704] Job DZDJAD Seq. 23 Date 13-Oct-76 15:13:22 Monitor IPO-D 5073 [1A3] +START+
Request created: 13-Oct-76 14:51:19 XTO:ML21-4:DAVIES -- distribution to ML21-4, slot 134

EE366 95420-02E JADESEQT400522049 ICE 20130111 120915Z 15FEB100:11321MFR481.4E030500876L15:13:27
File will be REMAINED to 1057+ protection

MAINDE0-11-02DJA-0

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E01

.REM :

IDENTIFICATION

PRODUCT CODE: MAINDE0-11-02DJA-0-0
PRODUCT NAME: DJ11 LOGIC TESTS
PROGRAM DATE: MAY 1976
MAINTAINER: DIAGNOSTIC GROUP

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F01

MAINDEC-11-D2DJA-D
222780.F11

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MAINDEC-1A-D2DJA-D-D
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MAINDEC-11-DZDJB-D
DZDJB.D.P11

DJ11 LOGIC TESTS

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MAINDEC-11-DZDJB-D-D DJ11 LOGIC TESTS
DESCRIPTION

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1. ABSTRACT

THIS PROGRAM TESTS THE LOGIC OF THE DJ11 ASYNCHRONOUS MULTIPLEXER IN MAINTENANCE MODE. IT CHECKS THAT ALL THE CONTROL REGISTERS FUNCTION PROPERLY, THAT INTERRUPTS OCCURE AT THE RIGHT LEVEL, AND THAT DATA CAN BE TRANSMITTED AND RECEIVED CORRECTLY. THIS PROGRAM DOES NOT TEST THAT THE INPUT AND OUTPUT LEAD CONNECTIONS ARE FUNCTIONAL. (SEE MAINDEC-11-DZDJB, PROGRAMS 2 AND 3 FOR ON-LINE TESTING). THE PROGRAM SHOULD BE RUN FOR AT LEAST 2 PASSES WITH ALL SWITCHES DOWN.

2. REQUIREMENTS

2.1 EQUIPMENT

FDP-11 STANDARD COMPUTER WITH CONSOLE TELETYPE
OF TO 16 DJ11 ASYNCHRONOUS MULTIPLEXERS.

2.2 STORAGE

THIS PROGRAM USES ALL OF 8K, EXCEPT ABS LOADER.

2.3 PRELIMINARY PROGRAMS

NONE

3. LOADING PROCEDURE

USE STANDARD PROCEDURE FOR ABS TAPES.

4. STARTING PROCEDURE

4.1 CONTROL SWITCH SETTINGS

SEE 5.1 (ALL DOWN FOR WORST CASE TESTING)

4.2 STARTING ADDRESS

THE PROGRAM SHOULD ALWAYS BE STARTED AT 200. IT MAY BE RESTARTED AT 1000 AFTER ALL PARAMETERS HAVE BEEN SELECTED.

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DZDJ-A-D.P11

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MAINDEC-11-DZDJ-A-D-D DJ11 LOGIC TESTS
DESCRIPTION

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4.3 PROGRAM AND OPERATOR ACTION

- 1) LOAD PROGRAM INTO MEMORY USING ABS LOADER.
- 2) LOAD ADDRESS 200.
- 3) IF HARDWARE SWITCH REGISTER IS AVAILABLE, SET SWITCHES (SEE SEC. 5.1) ALL DOWN FOR WORST CASE, PRESS START.
- 4) IF SWITCH-LESS PROCESSOR SIMPLY PRESS START.
- 5) ENTER PARAMETERS (SEE SEC. 5.3) AS THEY ARE REQUESTED.
- 6) THE PROGRAM WILL LOOP AND BELL WILL RING ONCE EVERY PASS.
- 7) A MINIMUM OF TWO PASSES SHOULD ALWAYS BE RUN.

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

AT SA 200, ALL SWITCHES DOWN IS WORST CASE TESTING. EACH SUBTEST WILL BE LOOPED UPON UNTIL COMPLETION OF 16 PASSES OF THAT SUBTEST. THE BELL WILL RING UPON COMPLETION OF A PASS OF THE ENTIRE PROGRAM. ALTERNATE PASS WILL RUN WITH THE T-BIT SET.

THE SWITCH SETTINGS ARE:

SW<15> = 1 HALT ON ERROR
SW<14> = 1 SCOPE LOOP
SW<13> = 1 INHIBIT PRINTOUT
SW<12> = 1 INHIBIT TRACE TRAPPING
SW<11> = 1 INHIBIT ITERATIONS OF SUBTEST
SW<10> = 1 BELL ON ERROR
..... BELL ON PASS COMPLETE
SW<09> = 1 LOOP ON ERROR
SW<08> = 1 LOOP ON TEST IN SW<7:0>

THIS PROGRAM HAS BEEN MODIFIED TO RUN ON A PROCESSOR WITH OR WITHOUT A HARDWARE SWITCH REGISTER. WHEN FIRST EXECUTED THE PROGRAM TESTS THE EXISTENCE OF A HARDWARE SWITCH REGISTER. IF NOT FOUND A SOFTWARE SWITCH REGISTER LOCATION (SWREG=LOC. 176) IS DEFAULTED TO. IF THIS IS THE CASE, UPON EXECUTION THE CONTENTS OF THE SWREG ARE DUMPED IN OCTAL ON THE CONSOLE TTY AND ANY CHANGES ARE REQUESTED

(I.E.) SWR=XXXXXX NEW=

POSSIBLE RESPONSES ARE:

- 1: <CR> IF NO CHANGES ARE TO BE MADE.
- 2: 6 DIGITS 0-7 TO REPRESENT IN OCTAL THE NEW SWITCH REGISTER VALUE: LAST DIGIT FOLLOWED BY <CR>.
- 3: 1U TO ALLOW REENTERING VALUE IF ERROR IS

MAINDEC-11-22239-2
222392.F11

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COMMITTED KEYING IN SWREG VALUE.

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MAINDEC-11-DZDJIA-D-D
DESCRIPTION

5.3 PROGRAM AND OPERATOR ACTION

THE FOLLOWING REQUESTS ARE MADE TO THE OPERATOR AT THE BEGINNING OF THE PROGRAM. A DETAILED DESCRIPTION OF WHAT IS REQUIRED FOR EACH PARAMETER IS GIVEN BELOW.

- 1) "FIRST DJ11 ADDRESS: "
THE CSR ADDRESS OF THE FIRST DJ11 YOU WISH TO TEST. MUST BE BETWEEN 160000(8) AND 177777(8). THE DEFAULT (CARRIAGE RETURN) IS TO 160010(8). "P(PREVIOUS)" SELECTS THE ADDRESS PREVIOUSLY SELECTED.
- 2) "VECTOR ADDRESS: "
THE RECEIVER INTERRUPT VECTOR ADDRESS OF THE FIRST DJ11 YOU WISH TO TEST. MUST BE BETWEEN 300(8) AND 1000(8). THE DEFAULT (CARRIAGE RETURN) IS TO 300(8). "P(PREVIOUS)" SELECTS THE ADDRESS PREVIOUSLY SELECTED.
- 3) "NO. OF DJ11'S: "
THE NUMBER OF DJ11 UNITS YOU WISH TO TEST AT ONE TIME. MUST BE BETWEEN 1 AND 16. THE DEFAULT (CARRIAGE RETURN) IS TO 1. "P(PREVIOUS)" SELECTS THE NUMBER OF UNITS PREVIOUSLY SELECTED.
- 4) "STANDARD CONFIGURATION? "
"Y(ES)" OR DEFAULT (CARRIAGE RETURN) SELECTS 8 LEVEL CODE, NO PARITY. "N(NO)" CAUSES REQUESTS FOR CODE LEVEL AND PARITY ON ALL REQUESTED LINES IN GROUPS OF FOUR. "P(PREVIOUS)" SELECTS THE CODE LEVELS AND PARITIES PREVIOUSLY SELECTED.
- 5) "CHAR LENGTH: "
THE CODE LEVEL FOR THE LINE GROUP SPECIFIED. MUST BE 5, 6, 7, OR 8. THE DEFAULT (CARRIAGE RETURN) IS TO 8 LEVEL CODE.
- 6) "PARITY (NO, ODD, EVEN): "
THE TYPE OF PARITY SELECTED FOR THE LINE GROUP SPECIFIED. THE DEFAULT (CARRIAGE RETURN) IS TO NO PARITY.

6. ERRORS

6.1 ERROR PRINTOUT

THE FORMAT IS AS FOLLOWS:

ADR DJADR (R1) (R2) (R3) (R4)

WHERE:

ADR = ADDRESS OF ERROR HLT

DJADR = CSR ADDRESS OF DJ11 UNDER TEST

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305
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(RN) = CONTENTS OF GENERAL REGISTER "N". FROM NONE TO
FOUR OF THESE MAY BE TYPED DEPENDING ON THE NUMBER

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FOLLOWING THE HLT; E.G., HLT+3 WOULD TYPE (R1)
THRU (R3); HLT (BY ITSELF) WOULD STOP AFTER TYPING
ADR AND DJADR.

TO FIND THE FAILING TEST, LOOK AT THE LISTING ABOVE THE
ADDRESS TYPED. IN MOST CASES THE COMMENT BESIDE THE HLT
TELLS WHAT WAS BEING CHECKED AND WHAT WAS EXPECTED. ALSO, A
LIST OF THE PROBABLE FAILING LOGIC IS GIVEN IN THE COMMENTS
AT THE BEGINNING OF THE TEST.

6.2 ERROR RECOVERY

RESTART AT 200 OR 1000.

6.3 ERROR COUNTER

AN ERROR COUNT IS KEPT IN "ERRORS" (LOC 1202). IT CAN BE
CLEARED FROM THE CONSOLE, BY RESTARTING AT 200, OR BY
RELOADING THE PROGRAM.

7. RESTRICTIONS

IF MORE THAN ONE DJ11 IS TESTED AT A TIME, THE DEVICE
ADDRESSES AND THE VECTOR ADDRESSES MUST ALL BE CONTIGUOUS.

IF THIS PROGRAM IS RUN WITH A MONITOR, I.E. ACT11 OR DDP,
THE DEVICE ADDRESSES MUST FOLLOW THE FLOATING ADDRESS
CONVENTION. DJ11'S WILL BE FIRST, STARTING AT 160010.,

8. MISCELLANEOUS

8.1 EXECUTION TIME

DUE TO THE VARIOUS BAUD RATES AVAILABLE AND THE ABILITY TO
CHECK UP TO 8 DJ11'S AT ONCE, THE EXECUTION TIME CAN BE
ANYWHERE FROM 15 SECONDS TO THREE AND A HALF HOURS. THE
FOLLOWING TYPICAL TIMES ARE FOR ONE DJ11 WITH ALL LINES AT
THE SAME SPEED, 8 LEVEL CODE, 2 STOP BITS, AND NO PARITY ON
A PDP-11/20 WITHOUT TRACE TRAPPING. FOR MULTIPLE DJ11'S,
MULTIPLY THESE TIMES BY THE NUMBER OF UNITS SELECTED FOR
TEST.

BAUD RUN TIME

75 00:26:00
110 00:18:00
134.5 00:15:00

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DJ11 LOGIC TESTS

NO1
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363
364

150 00:13:00
300 00:05:30

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STOCK POINTERS

SEARCH IN UNITS OF 1000 METERS

A COUNT OF NUMBER OF PAGES COUNT IS KEPT IN "PASSED".
THIS COUNT CAN BE OBTAINED FROM THE CONSOLE.
INITIATING AT 200, CAN BY RELOADING THE PROGRAM.

POWER FAULT

THE TEST CAN BE POWER FAILED WITH NO ERRORS. TO USE, START
SOLARIS AS USUAL AND POWERDOWNS IT. ANY TIME THE
USER SHOULD TYPE "POWER" AND RESTART THE PROGRAM WITH NO
ERRORS.

PROGRAM DESCRIPTION

THIS PROGRAM TESTS THE LOGIC OF UP TO 16 DJ11 ASYNCHRONOUS DATA MULTIPLEXERS IN MAINTENANCE MODE. IT CHECKS THAT THE CONTROL REGISTERS FUNCTION PROPERLY, THAT INTERRUPTS OCCUR AT THE RIGHT PRIORITY LEVEL, AND THAT DATA CAN BE TRANSMITTED AND RECEIVED CORRECTLY. THE PROGRAM HAS MANY SUBTESTS (THE CODE BETWEEN 2 SCOPE STATEMENTS) WHICH ARE RUN 16 TIMES BEFORE CONTINUING TO THE NEXT. SW₁₁ ON A I-162000 EQUATES EACH SUBTEST TO BE RUN ONLY ONCE. SW₉ ON A I-162000 EQUATES LOOP ON ERROR. THE ADDRESS ICNT (LOC 18000) CONTAINS THE ITERATION COUNT IN THE LEFT BYTE AND THE TEST NUMBER IN THE RIGHT BYTE. ALL THE SUBTESTS SHOULD BE RUN SEQUENTIALLY BY STARTING AT 200 NOT BY STARTING AT THE BEGINNING OF THE SUBTEST. TO LOOP ON A PARTICULAR SUBTEST, PUT THE TEST NUMBER (SEE LISTING) IN THE RIGHT BYTE OF THE SWITCH REGISTER AND SW₉ ON A I. THIS TEST WILL BE LOOPED UPON UNTIL SW₉ IS PUT ON A 0 OR THE RIGHT BYTE IS CHANGED. THE TEST IS NON-EXISTANT, THE PROGRAM WILL BE RUN AS USUAL. IF MORE THAN ONE DJ11 IS SELECTED, ALL THE SUBTESTS ARE PERFORMED ON ONE UNIT AT A TIME. THE BELL WILL NOT GO UNTIL A PASS HAS BEEN MADE ON EACH OF THE DJ11'S SELECTED FOR TEST.

MAINDEC-11-02204-A-0

DD11 LOGIC TESTS
SWITCH SETTINGS

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CO2

TITLE MAINDEC-11-02204-A DD11 LOGIC TESTS
 ENABLE ABS
 ENABLE AMB
 COPYRIGHT 1972, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
 PROGRAM BY KEN CHAPMAN

	SWITCH	USE
SW15	100000	HALT ON ERROR
SW14	40000	LOOP ON TEST
SW13	20000	INHIBIT ERROR TYPEOUTS
SW12	10000	INHIBIT TRACE TRAP
SW11	4000	INHIBIT ITERATIONS
SW10	2000	O - BELL ON PASS COMPLETE
SW9	1000	L - BELL ON ERROR
SW8	400	LOOP ON ERROR
SW7	400	LOOP ON TEST IN SW7:0

DD11 REGISTER BIT ASSIGNMENTS:

CONTROL	STATUS REGISTER (CSR) XXXXX0
BIT0	RECEIVER ENABLE (READ/WRITE)
BIT1	HALF DUPLEX SELECT (READ/WRITE)
BIT2	MAINTENANCE (READ/WRITE)
BIT3	CLEAR MOS (WRITE ONLY)
BIT4	CLEAR MOS FLAG (READ ONLY)
BIT5	NOT USED
BIT6	RECEIVER INTERRUPT ENABLE (READ/WRITE)
BIT7	DONE (READ ONLY)
BIT8	MASTER TRANSMITTER SCAN ENABLE (READ/WRITE)
BIT9	NOT USED
BIT10	READ/WRITE BREAK REGISTER (READ/WRITE)
BIT11	NOT USED
BIT12	STATUS ENABLE (READ/WRITE)
BIT13	MI/FO OVERRUN (READ ONLY)
BIT14	MASTER TRANSMITTER INTERRUPT ENABLE (READ/WRITE)
BIT15	TRANSMITTER READY (READ ONLY)

RECEIVER BUFFER REGISTER (RBUF) XXXXX2 (READ ONLY)

BIT0-7	RECEIVED CHARACTER
BIT8-11	LINE NUMBER
BIT12	PARITY ERROR
BIT13	FRAMING ERROR
BIT14	UART OVERRUN ERROR
BIT15	CHARACTER PRESENT

TRANSMITTER CONTROL REGISTER (TCR) XXXXX4 (READ/WRITE)

BIT0-15 STOP THE SCANNER ON CORRESPONDING LINE

TRANSMITTER BUFFER (TBUF) XXXXX6

BIT0-7 TRANSMITTED CHARACTER (WRITE ONLY)

31110000000000000000000000000000

3111 LOGIC TESTS
3111 SPECIFICATIONS

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D02

3111 LINE NUMBER (READ ONLY)

BREAK CONTROL STATUS REGISTER (BCSR) XXXXX4 (BIT10 OF CSR SET) (READ/WRITE)

BIT0-15 TRANSMIT A BREAK ON CORRESPONDING LINE!

SCOPE= TRAP
TYPE= EMT
ID= 137776
DUMXNO=10000000000000000000000000000000

;MAX ALLOWED NUMBER OF DUMXES

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DJ11 SPECIFICATIONS

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EO2

516	000000	000000	000000	. = 0.0	:TRAP CATCHER IN LOCATIONS 0 THRU 776 :LOCATIONS 0 AND 2 CONTAIN "HALT" INSTRUCTIONS :LOCATIONS 4 THRU 56 CONTAIN ".+2" AND "HALT" IN EVERY VECTOR :LOCATIONS 56 THRU 776 CONTAIN ".+2" AND "IOT" IN EVERY VECTOR
	000046	000046		. = 46	SENDAD
	000174	000174		. = 174	
	000176	000000		DISPREG: 0	
	000176	000000		SWREG: 0	
	000200	000200		. = 200	
	000200	000137	001324	. = JMP 1000	SEGIN :200 ALWAYS IS THE STARTING ADDRESS
	001000	001000		. = JMP	RESTART
	001000	000137	002302		
	001200	001200		. = 1200	
	001200	000000		ICNT: 0	:ITERATION COUNT-LH, TEST NO.-RH
	001200	000000		ERRORS: 0	:ERROR COUNT REGISTER
	001204	000000	000000	PCNT: 0.0	:PASS COUNT REGISTER
	001210	160010		CSR: 160010	
	001210	160012		RBUF: 160012	:CONTROL STATUS REGISTER(DJ UNDER TEST)
	001212			TCR: 160012	:RECEIVER BUFFER REGISTER(DJ UNDER TEST)
	001214	160014		BCSR: 160014	:TRANSMITTER CONTROL REGISTER(DJ UNDER TEST)
	001216	160016		TBUF: 160016	:BREAK STATUS REGISTER(DJ UNDER TEST)
	001220	000300		RCVVEC: 300	:RECEIVER INTERRUPT VECTOR ADDRESS(DJ UNDER TEST)
	001220	000300		RCVLVL: 302	
	001224	000304		XMTVEC: 304	:TRANSMITTER INTERRUPT VECTOR ADDRESS(DJ UNDER TEST)
	001226	000306		XMTLVL: 306	
	001230	160010		DEVADR: 160010	
	001230	000300		VECADR: 300	:FIRST DEVICE ADDRESS(SELECTED)
	001230	000001		UNITS: 1	:FIRST VECTOR ADDRESS(SELECTED)
	001236	000040		LENGTH: .BLKB 40	:NUMBER OF UNITS TO BE TESTED
	001236	000004		PARITY: .BLKS 4	:TABLE OF CHARACTER LENGTHS (MASKS)
	001236	000000		TIMER: 0	:TABLE OF ODD PARITY FLAGS
	001236	000000			:USED TO SAVE RELATIVE TIMES
	001304	000000		DJUUT: 0	
	001304	000000		DJLEN: 00	:UNIT NUMBER OF DJ11 UNDER TEST
	001304	000000		DJPAR: 0	:CHAR MASK TABLE POINTER
	001304	160010		DEFADR: 160010	:UNIT FLAG (FOR ODD PARITY FLAG)
	001314	000300		DEFVEC: 300	:DEFAULT FIRST DEVICE ADDRESS
	001316	177570		SWR: 177570	:DEFAULT FIRST VECTOR ADDRESS
	001320	177570		DISPLAY: 177570	
	001322	177777		FTIME: -1	

MAINDEC-11-DZDJIA-D
DZDJIA.D.F11DJ11 LOGIC TESTS
SETUP AREA

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580	001324	012706	001200	BEGIN:	MOV	#ICNT.	SP	:SET UP STACK POINTER
	001330	004737	017710		JSR	PC.	SUSWRR	:CHECK FOR SWITCH REGISTER
	001334	012700	000014		MOV	#14, R0		
	001340	012720	015534		MOV	#YESRT	(R0)+	;TRACE TRAP VECTOR (14)
	001344	012720	000340		MOV	#340, (R0)+		
	001350	012720	017104		MOV	#IOTRAP, (R0)+		;IOT VECTOR (20)
	001354	012720	000340		MOV	#340, (R0)+		
	001360	012720	016744		MOV	#PDOWN\$, (R0)+		;POWER FAIL VECTOR (24)
	001364	012720	000340		MOV	#340, (R0)+		
	001370	012720	015774		MOV	#EMT\$, (R0)+		;EMT VECTOR (30)
	001374	012720	000340		MOV	#340, (R0)+		
	001400	012720	015632		MOV	#TRAPS, (R0)+		;TRAP VECTOR (34)
	001404	012720	000340		MOV	#340, (R0)+		
	001410	012737	001446	000010	MOV	#15, J#10		
	001416	006700			SXT	R0		:CHECK FOR PDP-11/40 OR 45
	001420	012737	000006	015534	MOV	#RTT, J#YESRT		
	001426	012737	000006	000006	MOV	#RTT, J#6		
	001434	012737	000400	177774	MOV	#400, J#177774		;SET UP STACK LIMIT TO 1000
	001442	005037	000006		CLR	J#6		
	001446	012737	000012	000010 1\$:	MOV	#12, J#10		
	001454	005037	001202		CLR	ERRORS		:CLEAR ERROR COUNTER
	001460	005037	001204		CLR	PCNT		:CLEAR PASS COUNTER
	001464	005037	001206		CLR	PCNT+2		
	001470	005737	000042		TST	J#42		:CHECK FOR ACT11 OR DDP PRESENT
	001474	001404			SEQ	GETADR		:BRANCH IF NONE
	001476	004737	017470		JSR	PC	AUTO	:GO TO SUBROUTINE TO "MAP" DJ11 ON THE SYS
	001502	000137	002302		JMP	RESTAR		:SKIP OPERATOR ACTION
-	599	001506	000004	017244	GETADR:	TYPE,	MSGADR	:TYPE "FIRST DJ11 ADDRESS"
	600	001512	004537	016216	JSR	RS,	READIN	:READ INPUT FROM TTY AND SAVE
	601	001516	001230		.WORD	DEVADR		:IN DEVADR
	602	001520	001372		BNE	GETADR		:BRANCH IF BAD INPUT
	603	001522	005737	001230	TST	DEVADR		
	604	001526	001003		BNE	J\$		
	605	001530	013737	001312	001230	MOV	DEFADR, DEVADR	
	606	001536	042737	000007	001230	BIC	#7, DEVADR	
	607	001544	022737	150000	001230	CMP	#1E0000, DEVADR	
	608	001552	101355		BHI	GETADR		
	610	001554	000004	017274	GETVEC:	TYPE,	MSGVEC	:TYPE "VECTOR ADDRESS:"
	611	001560	004537	016216	JSR	RS,	READIN	:READ INPUT FROM TTY AND SAVE
	612	001564	001232		.WORD	VECADR		:IN VECADR
	613	001566	001372		BNE	GETVEC		:BRANCH IF BAD INPUT
	614	001570	005737	001232	TST	VECADR		:CHECK FOR CR
	615	001574	001003		BNE	J\$		
	616	001576	012737	000300	001232	MOV	#300, VECADR	:SET TO FIRST FLOATING VECTOR
	617	001604	042737	000007	001232	BIC	#7, VECADR	:CLEAR TO MODULO 10
	618	001612	022737	000300	001232	CMP	#300, VECADR	:CHECK FOR LOW LIMIT
	619	001620	003355		BGT	GETVEC		
	620	001622	022737	001000	001232	CMP	#1000, VECADR	:CHECK FOR UPPER LIMIT
	621	001630	003751		BLE	GETVEC		
	622	001632	000004	017320	GETNUM:	TYPE,	MSGNUM	:TYPE "NUMBER OR UNITS:"
	623	001638	004737	016364	JSR	PC,READS		:READ INPUT FROM THE TTY
	624	001642	012702	016512	: CHECK STRING	FOR VALID DIGITS, TERMINATOR, AND 'P'		
					MOV	#INPUT,R2		:POINTS TO INPUT STRING

MAINDEC-11-DZDJJA-D
DZDJJA.D.P11DJ11 LOGIC TESTS
SETUP AREA

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626	001646	112201		MOV B (R2)+,R1	:LOAD 1ST CHAR	
	001650	001434		BEQ 1\$:BRANCH IF IMMEDIATE TERMINATOR	
	001652	122701	000120	CMPB #'P,R1	:CHECK FOR A P	
	001656	001443		BEQ CONFIG	:CONFIGURE MODE IF SO	
	001660	120127	000071	CMPB R1,#71	:MUST BE A VALID ASCII NUMBER	
	001664	101362		BHI GETNUM	:ELSE RETRY	
	001666	162701	000060	SUB #60,R1	:STRIP ASCII CODE	
	001672	003757		BLE GETNUM	:SHOULDN'T BE ZERO OR NEG	
				:1ST CHAR IS A VALID DIGIT, 1 THRU 9 - CHECK REST OF STRING		
	001674	105722		TSTB (R2)+	:2ND CHAR A TERMINATOR?	
	001676	001423		BEQ 3\$:YES - R1 HAS THE FINAL # OF UNITS	
	001700	105712		TSTB (R2)	:NO - NXT CHAR MUST BE THE TERMINATOR	
	001702	001353		BNE GETNUM	:ELSE RETRY.	
	001704	124827	000071	CMPB -(R2),#71	:CHECK 2ND CHAR FOR A VALID NUMBER	
	001710	101350		BHI GETNUM		
	001712	111203		MOV B (R2),R3	:MAKE IT MORE ACCESSIBLE	
	001714	162703	000060	SUB #60,R3	:STRIP ASCII CODE	
	001720	100744		SMI GETNUM	:SHOULDN'T BE NEGATIVE	
				:BOTH LOW AND HIGH ORDER DIGITS ARE OK - CONVERT DECIMAL VALUE.		
	001722	010146		MOV R1,-(SP)	:SAVE IT FOR LATER	
	001724	006301		ASL R1	:MULT HI ORDER BY 8	
	001726	006301		ASL R1		
	001730	006301		ASL R1		
	001732	006316		ASL (SP)	:MULTIPLY IT BY 2	
	001734	062601		ADD (SP)+,R1	:RESULT IS (HI ORD)*10.	
	001736	060301		ADD R3,R1	:NOW ADD IN THE LOW ORDER	
	001740	000402		BR 3\$		
	001742	012701	000001	1\$: MOV #1,R1	:LOAD DEFAULT VALUE HERE	
				3\$: R1 HAS THE CONVERTED VALUE - COMPARE AGAINST MAX ALLOWED.		
	001746	020127	000020	CMP R1,#DJMXNO	:TOO BIG?	
	001752	101327		BHI GETNUM	:YES - RETRY.	
	001754	010137	001234	MOV R1,UNITS	:VALUE OK - STORE RESULT	
	001760	012737	000100	MOV \$100,DJUUT	: "PRIME" UNIT UNDER TEST NUMBER	
	001766	000004	017343	CONFIG: TYPE,	TYPE "STANDARD CONFIG?"	
	001772	004737	016364	JSR PC, READS	:READ INPUT FROM TTY	
	001776	122737	000120	016512	CMPB *'P, INPUT	:CHECK FOR "P"
	002004	001536		BEQ RESTAR	:BRANCH IF PREVIOUS	
	002006	012700	000022	MOV #22, R0	:SET UP COUNTER	
	002012	012701	001236	MOV #LENGTH,R1	:POINT TO CHAR LEN TABLE	
	002016	005021		CLR (R1)+	:PUT CHAR MASK FOR 9 IN CHAR TABLE	
					:AND CLR PARITY TABLE	
	002020	005300		DEC R0	:COUNT DOWN	
	002022	001375		BNE 1\$:BRANCH IF NOT DONE	
	002024	105737	016512	TSTB INPUT	:CHECK FOR CR	
	002030	001524		BEQ RESTAR	:BRANCH IF DEFAULT	
	002032	122737	000131	016512	CMPB #131, INPUT	:CHECK FOR "Y"
	002040	001520		BEQ RESTAR	:BRANCH IF DEFAULT	
	002042	122737	000116	016512	CMPB #116, INPUT	:CHECK FOR "N"
	002050	001346		CONFIG	:BRANCH IF ILLEGAL ENTRY	
	002052	005000		CLR R0	:CLR UNIT COUNTER	
	002054	005001		CLR R1	:CLR LINE COUNTER	
	002056	012702	001236	MOV #LENGTH,R2	:SET UP POINTER TO CHAR MASK TABLE	
	002058	012703	001276	MOV #PARITY,R3	:SET UP POINTER TO PARITY TABLE	
	002060	012704	000001	MOV #1,R4	:SET UP MARKER	
691	002072	000004	017377	TYPLIN: TYPE,	TYPE "LINES "	
				MSGLIN		

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SETUP AREA

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682	002076	010105		MOV	R1,TTY	TYPE R1 IN OCTAL
683	002100	004737	015572	JSR	PC,PRINTS	AND SUPPRESS LEADING ZERO'S
684	002104	000004	017410	TYPE,	MSGDAS	TYPE A DASH (-)
685	002110	062701	000003	ADD	#3, R1	LAST LINE IN GROUP OF 4
686	002114	010105		MCV	R1,TTY	TYPE R1 IN OCTAL
687	002116	004737	015572	JSR	PC,PRINTS	AND SUPPRESS LEADING ZERO'S
688	002122	005201		INC	R1	FIRST LINE NEXT GROUP
689	002124	000004	017414	TYPE,	MSGLEN	TYPE "CHAR LENGTH:"
690	002130	004737	016512	JSR	PC, READS	READ FROM THE TTY
691	002134	105737	016512	TSTB	INPUT	CHECK FOR CR (DEFAULT)
692	002140	001421		BEQ	GETPAR	BRANCH IF DEFAULT
693	002142	105737	016513	TSTB	INPUT+1	CHECK FOR BAD DATA
694	002146	001366		BNE	GETLEN	BRANCH IF BAD
695	002150	162737	000060	SUB	#60, INPUT	CONVERT FROM ASCII
696	002156	112712	177777	MOVB	#-1, (R2)	SET UP MASK
697	002162	106312		ASLB	(R2)	CLEAR MASK BIT BY BIT
698	002164	103357		BCC	GETLEN	BAD INPUT, > 8
699	002166	105337	016512	DECB	INPUT	COUNT
700	002172	001373		BNE	2\$	BRANCH IF NOT DONE
701	002174	132712	000037	BITB	#37, (R2)	CHECK FOR 5 CHAR
702	002200	001351		BNE	GETLEN	BAD INPUT, < 5
703	002202	005202		INC	R2	INC TO NEXT LINE GROUP
704	002204	000004	017435	TYPE,	MSGPAR	TYPE "PARITY (NO, ODD, EVEN):"
705	002210	004737	016364	JSR	PC,READS	READ INPUT FROM TTY
706	002214	005737	016512	TST	INPUT	CHECK FOR CR
707	002220	001415		BEQ	3\$	BRANCH IF DEFAULT
708	002222	122737	000116	CMPB	#116, INPUT	CHECK FOR "N"
709	002230	001411		BEQ	3\$	BRANCH IF "NO"
710	002232	122737	000105	CMPB	#105, INPUT	CHECK FOR "E"
711	002240	001405		BEQ	3\$	BRANCH IF "EVEN"
712	002242	122737	000117	CMPB	#117, INPUT	CHECK FOR "O"
713	002250	001355		BNE	GETPAR	BRANCH IF NONE
714	002252	150413		BISB	R4, (R3)	SET THE ODD PARITY FLAG
715	002254	005203		INC	R3	UP DATE PARITY TABLE POINTER
716	002256	032701	000017	BIT	#17,R1	CHECK FOR NEXT UNIT
717	002262	001303		BNE	TYPLIN	BRANCH IF NOT
718	002264	012703	001276	MOV	#PARITY,R3	RESET PARITY TABLE POINTER
719	002270	006304		ASL	R4	FLAG TO NEXT UNIT
720	002272	005200		INC	R0	COUNT UNITS
721	002274	020037	001234	CMP	R0,UNITS	CHECK FOR LAST
722	002300	001274		BNE	TYPLIN	BRANCH IF MORE

723
 724 002302 000005 012706 001200 RESTAR: RESET :ISSUE RESET
 725 002304 005737 001322 MOV #ICNT, SP :SET UP STACK POINTER
 726 002310 001410 TST FTIME
 727 002314 001004 BEQ CLRVEC
 728 002316 00176 001315 CMP #SWREG, SWR
 729 002324 001004 BNE CLRVEC
 730 002326 004737 017770 JSR PC, CNTLU
 731 002332 005037 001322 CLR FTIME
 732 002336 012700 000300 CLRVEC: MOV #300, R0 :BEGINNING OF FLOATING VECTORS
 733 002342 005720 177776 1\$: TST (R0)+
 734 002344 010050 000004 MOV R0, -2(R0) :" +2"
 735 002350 012720 000004 MOV #IOT, (R0)+ ;"IOT"
 736 002354 022700 001000 CMP #1000, R0
 737 002360 001370 SNE 1\$
 738 002362 062737 000010 001210 ADD #10, CSR :UPDATE DEVICE ADDRESS TO NEXT UNIT
 739 002370 062737 000010 001220 ADD #10, RCVVEC :UPDATE DEVICE VECTOR ADDRESS
 740 002376 062737 000004 001306 ADD #4, DJLEN :MOVE CHAR TABLE POINTER
 741 002404 006337 001310 ASL DJPAR :UPDATE PARITY FLAG MARKER
 742 002410 023737 001304 001234 CMP DJUUT, UNITS
 743 002416 002416 BLT 2\$
 744 002420 005037 001304 CLR DJUUT
 745 002424 013737 001230 001210 MOV DEVADR, CSR
 746 002432 013737 001232 001220 MOV VECADR, RCVVEC
 747 002440 012737 001236 001306 MOV #LENGTH, DJLEN :INIT CHAR TABLE POINTER
 748 002446 012737 000001 001310 MOV #1, DJPAR :INIT PARITY FLAG MARKER
 749 002454 005237 001304 2\$: INC DJUUT
 750 002460 013701 001210 MOV CSR, R1 :SET UP ALL THE REGISTER ADDRESSES
 751 002464 062701 000002 ADD #2, R1 :ADD 2
 752 002470 010137 001212 MOV R1, RBUF :SET UP RECEIVER BUFFER
 753 002474 062701 000002 ADD #2, R1 :ADD 2
 754 002500 010137 001214 MOV R1, TCR :SET UP TRANSMITTER CONTROL REG
 755 : AND BREAK STATUS REG
 756 002504 062701 000002 ADD #2, R1 :ADD 2
 757 002510 010137 001216 MOV R1, TBUF :SET UP TRANSMITTER BUFFER
 758 002514 013701 001220 MOV RCVVEC, R1 :POINTER FOR VECTOR SETUP
 759 002520 005721 TST (R1)+ :INC R1
 760 002522 010137 001222 MOV R1, RCVLVL :SET INT LVL
 761 002526 005721 TST (R1)+ :INC R1
 762 002530 010137 001224 MOV R1, XMTVEC :TRANSMITTER VECTOR
 763 002534 005721 TST (R1)+ :INC R1
 764 002536 010137 001226 MOV R1, XMTLVL :XMT INT LVL ADR
 765 002542 005037 001200 CLR ICNT
 766 002546 005037 015770 CLR LAD
 767 002552 104400 SCOPE

MAINDEC-11-DZDJ-A-D
DZDJAD.P11 TST1: TEST IF CSR EXISTS

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770
771
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777 002554 012737 002612 000004 TST1: MOV #1$, @#4 ;SET UP TIME-OUT TRAP VECTOR
778 002562 012737 000340 000006 MOV #LEVEL7, @#6
779 002570 005777 176414 TST @CSR ;REFERENCE CSR (READ)
780 002574 005077 176410 CLR @CSR ;CLEAR CSR (WRITE)
781 002600 005577 176404 ADC @CSR ;CHECK CSR (READ AND WRITE)
782 002604 001405 BEQ 2$ ;BRANCH IF OK
783 002606 104000 HLT ;CSR NOT CLEARED
784
785 002610 000403 BR 2$ ;SKIP ISR
786
787 002612 012601 1$: MOV (SP)+, R1 ;SAVE RTI ADR FOR TYPING
788 002614 104001 HLT+1 ;CAN'T REFERENCE CSR!
789
790 002616 005726 TST (SP)+ ;FINISH CLEARING STACK
791 002620 012737 000006 000004 2$: MOV #5, @#4
792 002625 005037 000006 CLR @#6
793 002632 104400 SCOPE
794
795
796
797
798
799
800 002634 012777 000002 176346 TST2: MOV #BIT1, @CSR ;SET BIT1
801 002642 032777 000002 176340 BIT #BIT1, @CSR ;CHECK THAT BIT1 IS SET
802 002650 001001 BNE .+4 ;BRANCH IF OK
803 002652 104000 HLT ;CSR BIT1 FAILED TO SET
804
805 002654 032777 177775 176326 BIT #177775, @CSR ;CHECK THAT NO OTHER BIT SET
806 002662 001401 BEQ .+4 ;BRANCH IF OK
807 002664 104000 HLT ;EXTRA BIT SET IN CSR
808
809 002666 005077 176316 CLR @CSR ;CLEAR BIT1
810 002672 032777 000002 176310 BIT #BIT1, @CSR ;CHECK THAT BIT1 IS CLEARED
811 002700 001401 BEQ .+4 ;BRANCH IF OK
812 002702 104000 HLT ;CSR BIT1 FAILED TO CLEAR
813
814 002704 104400 SCOPE
815
816
817
818
819
820
821 002706 012777 000004 176274 TST3: MOV #BIT2, @CSR ;SET BIT2
822 002714 032777 000004 176266 BIT #BIT2, @CSR ;CHECK THAT BIT2 IS SET
823 002722 001001 BNE .+4 ;BRANCH IF OK
824 002724 104000 HLT ;CSR BIT2 FAILED TO SET
825

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K02

MAINDEC-11-DZDJJA-D
DZDJAD.P11 TST3: DJ11 LOGIC TESTS

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826 002726 032777 177773 176254 BIT #177773,0CSR ;CHECK THAT NO OTHER BIT SET
 827 002734 001401 BEQ .+4 ;BRANCH IF OK
 828 002736 104000 HLT
 829
 830 002740 005077 176244 CLR #CSR ;CLEAR BIT2
 831 002744 032777 000004 176236 BIT #BIT2,0CSR ;CHECK THAT BIT2 IS CLEARED
 832 002752 001401 BEQ .+4 ;BRANCH IF OK
 833 002754 104000 HLT ;CSR BIT2 FAILED TO CLEAR
 834
 835 002756 104400 SCOPE

836
 837 :*****
 838 :TEST 4: TEST THAT CSR BITS CAN BE SET AND CLEARED
 839 :PROBABLE FAULTY LOGIC: M7285 (D2-2) E4,E18, (D2-4) E47,E64
 840 :*****

841
 842 002760 012777 000100 176222 TST4: MOV #BIT6,0CSR ;SET BIT6
 843 002766 032777 000100 176214 BIT #BIT6,0CSR ;CHECK THAT BIT6 IS SET
 844 002774 001001 BNE .+4 ;BRANCH IF OK
 845 002776 104000 HLT ;CSR BIT6 FAILED TO SET
 846
 847 003000 032777 177677 176202 BIT #177677,0CSR ;CHECK THAT NO OTHER BIT SET
 848 003006 001401 BEQ .+4 ;BRANCH IF OK
 849 003010 104000 HLT ;EXTRA BIT SET IN CSR
 850
 851 003012 005077 176172 CLR #CSR ;CLEAR BIT6
 852 003016 032777 000100 176164 BIT #BIT6,0CSR ;CHECK THAT BIT6 IS CLEARED
 853 003024 001401 BEQ .+4 ;BRANCH IF OK
 854 003026 104000 HLT ;CSR BIT6 FAILED TO CLEAR
 855
 856 003030 104400 SCOPE

857
 858 :*****
 859 :TEST 5: TEST THAT CSR BITS CAN BE SET AND CLEARED
 860 :PROBABLE FAULTY LOGIC: M7285 (D2-2) E6,E18, (D2-4) E47,E31
 861 :*****

862
 863 003032 012777 000400 176150 TST5: MOV #BIT8,0CSR ;SET BIT8
 864 003040 032777 000400 176142 BIT #BIT8,0CSR ;CHECK THAT BIT8 IS SET
 865 003046 001001 BNE .+4 ;BRANCH IF OK
 866 003050 104000 HLT ;CSR BIT8 FAILED TO SET
 867
 868 003052 032777 177377 176130 BIT #177377,0CSR ;CHECK THAT NO OTHER BIT SET
 869 003060 001401 BEQ .+4 ;BRANCH IF OK
 870 003062 104000 HLT ;EXTRA BIT SET IN CSR
 871
 872 003064 005077 176120 CLR #CSR ;CLEAR BIT8
 873 003070 032777 000400 176112 BIT #BIT8,0CSR ;CHECK THAT BIT8 IS CLEARED
 874 003076 001401 BEQ .+4 ;BRANCH IF OK
 875 003100 104000 HLT ;CSR BIT8 FAILED TO CLEAR
 876
 877 003102 104400 SCOPE

878
 879 :*****
 880 :TEST 6: TEST THAT CSR BIT10 CAN BE SET AND CLEARED
 881 :PROBABLE FAULTY LOGIC: M7295 (D2-2) E30,E24, (D2-4) E47,E31

L02

MAINDEC-11-DZDJR-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 22
DZDJR.D.P11 TST6: TEST BIT10 OF CSR

M02

MAINDEC-11-DZDJAD-0 DJ11 LOGIC TESTS
DZDJAD.PII TST10: TEST BIT14 OF CSR

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938 003276 104000 HLT ;CSR BIT14 FAILED TO CLEAR
939

940 003300 104400 SCOPE

***** TEST 11: TEST THAT RECEIVER ENABLE (BIT0 OF THE CSR) CAN BE SET AND CLEARED, AND THAT CLEAR MOS (BIT3) IS WRITE ONLY.
PROBABLE FAULTY LOGIC: M7285 (D2-2) E26,E36,E7,E24. (D2-8) E17,E14,E15 *****

948	003302	012777	000004	175700	TST11:	MOV	#BIT2,	0CSR	:SET MAINTENANCE MODE (BIT2)
949	003310	005005				CLR	R5		:SET UP COUNTER
950	003312	052777	000010	175670		BIS	#BIT3,	0CSR	:SET CLEAR MOS (BIT3)
951	003320	017701	175664		1\$:	MOV	0CSR,	R1	:SAVE CSR
952	003324	032701	000010			SIT	#BIT3,	R1	:CHECK CLEAR MOS (BIT3)
953	003330	001401				BEQ	.+4		:BRANCH IF OK
954	003332	104001				HLT+1			:CLEAR MOS (BIT3) SET (WRITE-ONLY)
955									:R1 = CONTENTS OF CSR
956	003334	032701	000020			SIT	#BIT4,	R1	:CHECK CLEAR MOS FLAG
957	003340	001403				BEQ	2\$:BRANCH IF CLEARED
958	003342	105305				DECB	R5		:WAIT FOR MOS TO CLEAR
959	003344	001365				BNE	1\$:BRANCH IF MORE TIME
960	003346	104001				HLT+1			:CLEAR MOS FLAG (BIT4) FAILED TO CLEAR
961									:R1 = CONTENTS OF CSR
962	003350	022701	000004		2\$:	CMP	#BIT2,	R1	:CHECK THAT ONLY MAINTENANCE BIT SET
963	003354	001401				BEQ	.+4		:BRANCH IF OK
964	003356	104001				HLT+1			:CLEAR MOS CLEARED MAINTENANCE
965									:OR SET OTHER CSR BITS
966									:R1 = CONTENTS OF CSR
967	003360	052777	000001	175622		BIS	#BIT0,	0CSR	:SET RECEIVER ENABLE
968	003366	017701	175616			MOV	0CSR,	R1	:SAVE CSR
969	003372	032777	000001	175610		BIT	#BIT0,	0CSR	:CHECK THAT RECEIVER ENABLE SET
970	003400	001001				BNE	.+4		:BRANCH IF OK
971	003402	104001				HLT+1			:RECEIVER ENABLE FAILED TO SET
972									:R1 = CONTENTS OF CSR
973	003404	022777	000005	175576		CMP	#5,	0CSR	:CHECK REST OF CSR
974	003412	001401				BEQ	.+4		:BRANCH IF OK
975	003414	104001				HLT+1			:CSR ERROR
976									:R1 = CONTENTS OF CSR
977									:NOTE: IF THE TTY MODULE IS BEING USED AND DONE (BIT7) IS SET.
978									:THE ERROR COULD BE DUE TO MAINTENANCE OR CLEAR MOS NOT WORKING.
979	003416	042777	000001	175564		BIC	#BIT0,	0CSR	:CLEAR RECEIVER ENABLE
980	003424	017701	175560			MOV	0CSR,	R1	:SAVE CSR
981	003430	022777	000004	175552		CMP	#BIT2,	0CSR	:CHECK CSR
982	003436	001401				BEQ	.+4		:BRANCH IF OK
983	003440	104001				HLT+1			:RECEIVER ENABLE DIDN'T CLEAR
984									:OR OTHER CSR BIT SET
985									:R1 = CONTENTS OF CSR

SCOPE

TEST 12: TEST THAT CSR RESPONDS PROPERLY TO BYTE COMMANDS
PROBABLE FAULTY LOGIC: M7285 (D2-4) E47

MAINDEC-11-D2DJA-D
DEC2000.PII TST12: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 24

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995 003444 012777 052506 175536 TST12: MOV #052506, QCSR ;SET TEST NUMBER IN CSR
996 003452 017701 175532 052400 CLR B QCSR ;CLR EVEN BYTE
997 003456 017701 175526 MOV QCSR, R1 ;SAVE CSR
998 003462 022701 052400 CMP #052400, R1 ;CHECK CSR
999 003466 001401 BEQ .+4 ;BRANCH IF OK
0000 003470 104001 HLT+1 ;EVEN BYTE CLR FAILED ON CSR
R1 = CONTENTS OF CSR
0001 003472 012777 052506 175510 MOV #052506, QCSR ;SET TEST NUMBER IN CSR
0002 003500 005237 001210 INC CSR ;INC TO ODD BYTE
0003 003504 017701 175500 CLR B QCSR ;CLR ODD BYTE
0004 003510 005337 001210 DEC CSR ;RESTORE TO EVEN
0005 003514 017701 175470 MOV QCSR, R1 ;SAVE CSR
0006 003520 022701 000106 CMP #000106, R1 ;CHECK CSR
0007 003524 001401 BEQ .+4 ;BRANCH IF OK
0008 003526 104001 HLT+1 ;ODD BYTE CLR FAILED ON CSR
R1 = CONTENTS OF CSR

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0011 003530 104400 SCOPE

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;*****TEST 13: TEST THAT THE BIS AND BIC INSTRUCTIONS SET AND CLEAR R/W
;BITS OF CSR
;PROBABLE FAULTY LOGIC: M7285 (D2-4) E47
;*****

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1019 003532 005077 175452 TST13: CLR QCSR ;CLEAR THE CSR
1020 003536 017701 175446 MOV QCSR, R1 ;CHECK AND SAVE CSR
1021 003542 001401 BEQ .+4 ;BRANCH IF CLEARED OK
1022 003544 104001 HLT+1 ;RESET FAILED TO CLR CSR
1024 003546 052777 052506 175434 BIS #052506, QCSR ;SET ALL R/W BITS OF CSR
1025 003554 022777 052506 175426 CMP #052506, QCSR ;CHECK THAT THEY GOT SET
1026 003562 001401 BEQ .+4 ;BRANCH IF OK
1027 003564 104000 HLT ;REG FAILED CMP
1028 003566 042777 052506 175414 BIC #052506, QCSR ;CLEAR CSR
1029 003574 017701 175410 MOV QCSR, R1 ;CHECK AND SAVE CSR
1030 003600 001401 BEQ .+4 ;BRANCH IF CLEARED OK
1031 003602 104001 HLT+1 ;CLR FAILED TO CLR CSR
1034 003604 104400 SCOPE

```

```

1036 ;*****TEST 14: TEST BITS OF TCR FOR READ/WRITE CAPABILITY
1037 ;PROBABLE FAULTY LOGIC: M7285 (D2-2) ALL, (D2-3) E8,E20,E21,E43,E41
1038 ;*****

```

```

1041 003606 012777 177777 175400 TST14: MOV #177777, QTCR ;SET ALL BITS OF TCR
1042 003614 017701 175374 MOV QTCR, R1 ;CHECK AND SAVE TCR
1043 003620 022701 177777 CMP #177777, R1 ;CHECK THAT ALL THE BITS ARE SET
1044 003624 001401 BEQ .+4 ;BRANCH IF OK
1045 003626 104001 HLT+1 ;BIT(S) OF TCR FAILED TO SET
1047 003630 005077 175360 CLR QTCR ;CLEAR TCR
1048 003634 017701 175354 MOV QTCR, R1 ;CHECK THAT IT CLEARED AND SAVE
1049 003640 001401 BEQ .+4 ;BRANCH IF CLR

```

10363611-022294-0
TST14: TEST READ/WRITE BITS OF TOR
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003642	104001		HLT+1	:BIT(S) OF TOR FAILED TO CLEAR
003644	104400		SCOPE	

```
*****  
TEST 15: TEST THAT TOR RESPONDS PROPERLY TO BYTE COMMANDS  
PROBABLE FAULTY LOGIC: M7285 (D2-3) E41  
*****
```

003646	010000	100000	175040	TST15: MOV \$100000,STOR CLR R1 CLRB STOR MOV STOR, R1 CMP R1 BEO .+4 HLT+1	SET TEST NUMBER IN TOR CLR EVEN BYTE SAVE TOR CHECK TOR BRANCH IF OK EVEN BYTE CLR FAILED ON TOR R1 = CONTENTS OF TOR
003647	010000	100000	175040	MOV \$100000,STOR INC R1 CLRB STOR DEC STOR MOV STOR, R1 CMP R1 BEO .+4 HLT+1	SET TEST NUMBER IN TOR INC TO ODD BYTE CLR ODD BYTE RESTORE TO EVEN SAVE TOR CHECK TOR BRANCH IF OK ODD BYTE CLR FAILED ON TOR R1 = CONTENTS OF TOR
003648	104001				

003702	104400		SCOPE	
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```
*****  
TEST 16: TEST THAT THE BIS AND BIC INSTRUCTIONS SET AND CLEAR R/W  
BITS OF TOR  
PROBABLE FAULTY LOGIC: M7285 (D2-3) E41  
*****
```

003704	000000	100000	175050	TST16: CLR STOR MOV STOR, R1 BEO .+4 HLT+1	CLEAR THE TOR CHECK AND SAVE TOR BRANCH IF CLEARED OK RESET FAILED TO CLR TOR
003705	104000				
003706	000000	100000	175050	BIS \$100000; CMP \$100000; BEO .+4 HLT	STOR :SET ALL R/W BITS OF TOR STOR :CHECK THAT THEY GOT SET BRANCH IF OK REG FAILED CMP
003707	104000				
003708	000000	100000	175050	BIC \$100000; MOV STOR, R1 BEO .+4 HLT+1	STOR :CLEAR TOR STOR :CHECK AND SAVE TOR BRANCH IF CLEARED OK CLR FAILED TO CLR TOR
004006	107100	000000	001000	SCOPE MOV #1, TIMER MOV #1, LAD	INITIALIZE TIMER RESET LOOP ADDRESS
004010	010000	000000	001000		

```
*****  
TEST 17: TEST THAT TRANSMIT READY (BIT15 OF CSR) SETS AND CLEARS  
WHEN TOR0 IS SET AND CLEARED.
```

C03

SEARCHED-11-0220460 100% BASIC TESTS
INDEXED-11-0220460 100% BASIC TESTS

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ALSO CHECK THAT THE RIGHT LINE NO. (0) APPEARS IN TRUFF.
Y LOGIC: M7295 (D2-5) ALL, (D2-6) E23, E32, E33, E43, (D2-2) E3, E1

004054	012007	000400	175156	TST17:	MOV BIS MOV BMI INC BNE	#400, #100, #000, #000, #000, #000	0CSR #100, #000, #000, #000, #000, #000	:SET XMTR SCAN ENABLE :SET XMTR CONTROL BIT, LINE 0 :SET UP WAIT COUNTED :CHECK AND SAVE XMTR READY :BRANCH IF SET OK :WAIT A WHILE
004054	012007	175148		18:	HLT+1			:XMTR READY FAILED TO SET
004056	000416				BR	38		:SKIP LINE # CHECK ON ERROR
004060	050037	001303		ES:	BIS MOV CLR	#0, #000, #000	TCR, #000, #000	:SET UP TIMER :SAVE LINE NUMBER
004064	012720	175126			CMP BEC	#0, #000	TCR, #000	:CHECK THAT THE XMTR STOPPED ON LINE 0 :BRANCH IF OK
004070	106003				HLT+1			:WRONG LINE NUMBER APPEARED IN TBUF
004074	000030				MOV	#0		
004078	001401	000000			MOV	#0		
004102	104001				MOV	#0		
004104	012708	175100			MOV BMI	#000, #000	0CSR, #000	:CHECK AND SAVE XMTR READY :BRANCH IF OK
004110	104001				HLT+2			:READING THE TBUF CLEARED XMTR READY
004114	048007	000001	175078	198:	BIC MOV BPI	#0100, #000, #000	0CSR, #000, #000	:CLR XMTR CONTROL BIT, LINE 0 :CHECK AND SAVE XMTR READY :BRANCH IF OK
004116	012007	175082			HLT+1			:XMTR READY FAILED TO CLEAR WHEN : XMTR CONTROL FOR LINE 0 WAS CLEARED
004132	104400				SCOPE			

TEST EC: TEST THAT TRANSMIT READY (BIT15 OF CSR) SETS AND CLEARS
WHEN EACH TCR BIT IS SET AND CLEARED.
ALSO CHECK THAT THE RIGHT LINE NO. APPEARS IN TBUFF.
PROBABLE FAULTY LOGIC: M7285 (D2-5) ALL, (D2-6) E23, E32, E33, E49, (D2-8) E3, E1

D03

MAINDEO-11-022J4-D
DEC0300.RII TST20: TEST LOGIC TESTS
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004172	000414			R0	38		: SKIP LINE # CHECK ON ERROR
004173	000027	001300	E8:	BIS	R0	TIMER	: SET UP TIMER
004174	012706	174501		MOV	R0		: SAVE LINE NUMBER
004175	000300			SWAB	R0		
004176	020201			CMP	R0		
004177	001400			BEG	R0	R1	: CHECK THAT THE XMTR STOPPED ON RIGHT LINE
004178	104000			HLT+2	R0		: BRANCH IF OK
							: WRONG LINE NUMBER APPEARED IN TBUF
							: R1=LINE # (SHOULD BE)
							: R2=LINE # (TBUF)
004214	017703	174770		MOV	0CSR.	R3	: CHECK AND SAVE XMTR READY
004215	100401			BMI	R0		: BRANCH IF OK
004216	104003			HLT+3			: READING THE TBUF CLEARED XMTR READY
004221	040477	174764	E8:	BIS	R0	STOR	: CLR XMTR CONTROL BIT, EACH LINE
004220	017702	174765		MOV	0CSR.	R2	: CHECK AND SAVE XMTR READY
004224	100001			BPL	R0		: BRANCH IF OK
004226	104002			HLT+2	R0		: XMTR READY FAILED TO CLEAR WHEN XMTR CONTROL FOR LINE 0 LINE WAS CLEARED
							: R1 = LINE #
							: R2 = CONTENTS OF CSR
004240	005601			INC	R1		: INC LINE COUNTER TO NEXT LINE
004241	106604			HBL	R0		: SHIFT MARKER TO NEXT LINE
004244	103341			BSC	R0		: BRANCH IF NOT LAST LINE
004246	104400			SCOPE			

TEST 21: TEST THAT MASTER TRANSMIT SCAN ENABLE (CSR BIT 8) ON A 0
DISABLES TRANSMITTER READY (CSR BIT 15)
WHEN TCR BIT, LINE 0 IS SET.
PROBABLE FAULTY LOGIC: M7295 (02-6) E49,E23,E32,E33

004260	005077	174734	TST21:	CLR	0CSR		: CLEAR CONTROL STATUS
004277	000001	174732		BIS	\$0100,0CSR		: SET XMTR CONTROL BIT, LINE 0
013200	001300			MOV	TIMER,R0		: GET TIMER FROM PREVIOUS TEST
017701	174716		I8:	MOV	0CSR,R1		: CHECK AND SAVE XMTR READY
004278	100002			BPL	R0		: BRANCH IF NOT SET
004274	104001			HLT+1	R0		: XMTR READY SET WITHOUT
004276	000402			BRT	R0		: MASTER TRANS SCAN ENABLE
004300	005300		28:	DEC	R0		: WAIT A WHILE
004302	001371			BNE	I8		: AND CHECK AGAIN
004304	052777	000400	174676	I8:	BIS		: SET MASTER TRAN SCAN ENABLE
004312	005000			CLR	R0		
004314	017701	174670	48:	MOV	0CSR, R1		: CHECK AND SAVE XMTR READY
004320	100403			BMI	R0		
004324	005200			INC	R0		
004326	001373			BNE	R0		
004327	104001			HLT+1	R0		: TRAN READY NEVER CAME UP
							: TCR BIT WAS SET FIRST

MAINDEC-11-0000A-D
0000A-D.F11 TST21: D111 LOGIC TESTS
TEST MASTER TRANSMIT SCAN ENABLE MACY11 27(732) 21-SEP-76 13:43 PAGE 28

: THEN MASTER TRAN SCAN ENABLE

: CLEAR IT OUT

: CHECK AND SAVE TRAN READY

: BRANCH IF OK

: TRAN READY DIDN'T CLEAR.

004346 104400

SCOPE

:*****
: TEST 22: TEST THAT INTERRUPT DOES NOT OCCUR AT LEVEL 7
: PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

004360 012777 004434 174646

TST22: MOV #ISR22, @XMTVEC : SET UP XMTR INTERRUPT VECTOR

004360 042737 000340 174646

MOV #340, @XMTLVL : AT LEVEL 7

004360 052737 000340 177776

BIC #340, @#PS : CLEAR PS LEVEL

004360 012777 004434 177776

BIS #340, @#PS : SET PS TO LEVEL 7

004360 000340 174600

MOV #040400, @CSR : SET TRAN MASTER INT. ENABLE

004414 012777 000001 174600

MOV #BITO, @TCR : SET TRAN CONTROL BIT, LINE 0

004420 100375 174570

IS: BPL 1\$: WAIT

004420 000404

BR END22 : OK, BRANCH IF NO INTERRUPT

004424 104400

ISR22: HLT : SHOULDN'T HAVE INTERRUPTED AT LEVEL 7

004426 012716 004434

MOV RTI : MOVE NEW RTI ADR ONTO STACK

004432 000002

END22: HLT :*****

004434 012777 001226 174562

END22: MOV XMTLVL, @XMTVEC

004442 012777 000004 174556

MOV #IOT, @XMTLVL

004450 005077 174540

CLR @TCR

004454 005077 174530

CLR @CSR

004460 042737 000340 177776

BIC #340, @#PS

004466 104400

SCOPE :*****

: TEST 23: TEST THAT INTERRUPT DOES NOT OCCUR AT LEVEL 6
: PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
:*****

004470 012777 004544 174526

TST23: MOV #ISR23, @XMTVEC : SET UP XMTR INTERRUPT VECTOR

004476 012777 000340 174522

MOV #340, @XMTLVL : AT LEVEL 7

004504 042737 000340 177776

BIC #340, @#PS : CLEAR PS LEVEL

004512 052737 000300 177776

BIS #300, @#PS : SET PS TO LEVEL 6

004520 012777 040400 174462

MOV #040400, @CSR : SET TRAN MASTER INT. ENABLE

004526 012777 000001 174460

MOV #BITO, @TCR : SET TRAN CONTROL BIT, LINE 0

004534 012701 174450

IS: BPL 1\$: WAIT

004540 100375

BR END23 : OK, BRANCH IF NO INTERRUPT

004544 104400

ISR23: HLT : SHOULDN'T HAVE INTERRUPTED AT LEVEL 6

004546 012716 004554

MOV RTI : MOVE NEW RTI ADR ONTO STACK

004552 000002

MAINDEC-11-DZDJ-A-D MACY11 27(732) 21-SEP-76 13:43 PAGE 29
DZDJ-A.D.P11 TST23: TEST TRANSMIT INTERRUPT LEVEL

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1274 004554 013777 001226 174442 END23: MOV XMTLVL, @XMTVEC
1275 004562 012777 000004 174436 MOV #IOT, @XMTLVL
1276 004570 005077 174420 CLR @TCR
1277 004574 005077 174410 CLR @CSR
1278 004600 042737 000340 177776 BIC #340, @#PS
1279 004606 104400 SCOPE
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MAINDEC-11-DZDJA-D MACYII 27(732) 21-SEP-76 13:43 PAGE 30
 DZDJAD.P11 TST25: TEST TRANSMIT INTERRUPT LEVEL

```

1330 005014 013777 001226 174202 END25: MOV    XMTLVL, @XMTVEC
1331 005022 012777 000004 174176    MOV    #IOT,  @XMTLVL
1332 005030 005077 174160    CLR    @TCR
1333 005034 005077 174150    CLR    @CSR
1334 005040 042737 000340 177776    BIC    #340, @PS
1335
1336 005046 104400
  
```

SCOPE

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***** TEST 26: TEST THAT INTERRUPT OCCURS AT LEVEL 3
***** PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
*****
  
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005050 012777 005126 174146 TST26: MOV    #ISR26, @XMTVEC :SET UP XMTR INTERRUPT VECTOR
005056 012777 000340 174142    MOV    #340, @XMTLVL :AT LEVEL 7
005064 042737 000340 177776    BIC    #340, @PS :CLEAR PS LEVEL
005072 052737 000140 177776    SIS    #140, @PS :SET PS TO LEVEL 3
005100 012777 040400 174102    MOV    #040400, @CSR :SET TRAN MASTER INT. ENABLE
005106 012777 000001 174100    MOV    #BIT0, @TCR :SET TRAN CONTROL BIT, LINE 0
005114 017701 174070    1$:    MOV    @CSR, RI :WAIT
005120 100375
005122 104000
005124 000403    ISR26:    HLT
005126 012716 005134    END26:   BR    :SHOULD HAVE INTERRUPTED AT LEVEL 3
005132 000002
005134 013777 001226 174062 END26:   MOV    #END26, (SP) :CONTINUE
005142 012777 000004 174056    MOV    #IOT,  @XMTLVL
005150 005077 174040    CLR    @TCR
005154 005077 174030    CLR    @CSR
005160 042737 000340 177776    BIC    #340, @PS
  
```

SCOPE

```

***** TEST 27: TEST THAT INTERRUPT OCCURS AT LEVEL 2
***** PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
*****
  
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005170 012777 005246 174026 TST27: MOV    #ISR27, @XMTVEC :SET UP XMTR INTERRUPT VECTOR
005176 012777 000340 174022    MOV    #340, @XMTLVL :AT LEVEL 7
005204 042737 000340 177776    BIC    #340, @PS :CLEAR PS LEVEL
005212 052737 000100 177776    SIS    #100, @PS :SET PS TO LEVEL 2
005220 012777 040400 173762    MOV    #040400, @CSR :SET TRAN MASTER INT. ENABLE
005226 012777 000001 173760    MOV    #BIT0, @TCR :SET TRAN CONTROL BIT, LINE 0
005234 017701 173750    1$:    MOV    @CSR, RI :WAIT
005240 100375
005242 104000
005244 000403    ISR27:   HLT
005246 012716 005254    END27:   BR    :SHOULD HAVE INTERRUPTED AT LEVEL 2
005252 000002
  
```

SCOPE

MAINDEC-11-D2DJA-D
D2DJA.D.PII TST27: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 31

```

1386 005254 013777 001226 173742 END27: MOV    XMTLVL, @XMTVEC
1387 005262 012777 000004 173736 MOV    #IOT,  @XMTLVL
1388 005270 005077 173720 CLR    @TCR
1389 005274 005077 173710 CLR    @CSR
1390 005200 042737 000340 177776 BIC    #340, @PS
1391
1392 005306 104400

```

SCOPE

```

1393
1394
1395 ;*****
1396 ;TEST 30: TEST THAT INTERRUPT OCCURS AT LEVEL 1
1397 ;PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
1398 ;*****
1399

```

```

1400 005310 012777 005366 173706 TST30: MOV    #ISR30, @XMTVEC ;SET UP XMTR INTERRUPT VECTOR
1401 005316 012777 000340 173702 MOV    #340, @XMTLVL ;AT LEVEL 7
1402 005324 042737 000340 177776 BIC    #340, @PS ;CLEAR PS LEVEL
1403 005332 052737 000040 177776 SIS    #040, @PS ;SET PS TO LEVEL 1
1404 005340 012777 040400 173642 MOV    #040400, @CSR ;SET TRAN MASTER INT. ENABLE
1405 005346 012777 000001 173640 MOV    #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
1406 005354 017701 173630 1$:      MOV    @CSR, R1 ;WAIT
1407 005360 100375 BPL   1$                ;SHOULD HAVE INTERRUPTED AT LEVEL 1
1408 005362 104000 HLT
1409 005364 000403 BR    END30            ;CONTINUE
1410
1411 005366 012716 005374 ISR30: MOV    #END30, (SP) ;MOVE NEW RTI ADR ONTO STACK
1412 005372 000002

```

MAINDEC-11-DZDJA-D
DZDJDAD.PII TST31: DJ11 LOGIC TESTS
TEST TRANSMIT INTERRUPT LEVEL MACY11 27(732) 21-SEP-76 13:43 PAGE 32

```

1442 005514 013777 001226 173502 END31: MOV XMTLVL, @XMTVEC
1443 005522 012777 000004 173476 MOV #10T, @XMTLVL
1444 005530 005077 173460 CLR @TCR
1445 005534 005077 173450 CLR @CSR
1446 005540 042737 000340 177776 BIC #340, @PS
1447
1448 005546 104400 SCOPE
1449
1450 005550 005037 001302 CLR TIMER :INITIALIZE TIMER
1451 005554 012737 005562 015770 MOV #.+5, LAD ;RESET LOOP ADDRESS
***** TEST 32: TEST THAT LINE 0 CAN TRANSMIT AND
***** RECEIVE A CHARACTER. (377)
1452 1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
1453 2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
1454 3$: CHECKS THAT NO ERRORS IN FI/FO
1455 4$: CHECKS THAT RIGHT LINE # (0) IN FI/FO
1456 5$: CHECKS FOR RIGHT CHARACTER LENGTH
1457 6$: CHECKS THAT CORRECT DATA WAS RECEIVED
1458 7$: CHECKS THAT CHARACTER PRESENT CLEARS
1459 8$: CHECKS THAT DONE CLEARS
1460 PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES
***** INITIALIZE DEVICE "CSR" REGISTER
1461 005562 004737 015565 TST32: JSR PC, @#INITD SET:
1462 :BIT2 = MAINTENANCE
1463 :BIT3 = CLEAR MOS
1464 :BIT8 = MASTER XMTR SCAN ENB
1465 :WAIT FOR MOS TO CLEAR SET:
1466 :BIT0 = RECEIVER ENABLE
1467 005566 052777 000001 173420 LOP32: BIS #BIT0, @TCR :SET XMTR CONTROL BIT, LINE 0
1468 005574 017701 173410 MOV @CSR, R1 ;WAIT FOR XMTR READY
1469 005600 100375 BPL LOP32
1470 005602 012777 000377 173406 MOV #377, @TBUF :SEND A RUBOUT
1471 005610 005000 CLR R0 :CLEAR COUNTER
1472 005612 105305 DECB R5 :SHORT WAIT LOOP
1473 005614 001376 BNE 1$ :
1474 005616 105777 TSTB @CSR :WAIT FOR DONE
1475 005622 100405 BMI 2$ :BRANCH WHEN DONE
1476 005624 005200 INC R0 :TIME COUNTER
1477 005626 001371 BNE 1$ :BRANCH IF NOT TIME-OUT
1478 005630 017701 MOV @CSR, R1 :SAVE CSR
1479 005634 104001 HLT+1 :DONE NEVER CAME UP
1480 :R1 = CONTENTS OF CSR
1481 005636 050037 001302 2$: BIS R0, TIMER :SAVE TIMER
1482 005642 017701 173344 MOV @RBUF, R1 :READ THE FI/FO
1483 005646 100401 BMI .+4 :BRANCH IF CHARACTER READY
1484 005650 104001 HLT+1 :CHARACTER READY DIDN'T SET
1485 :R1 = CONTENTS OF RBUF
1486 005652 032701 070000 3$: BIT #70000, R1 :CHECK FOR ERROR BITS
1487 005656 001401 BEQ .+4 :BRANCH IF NONE

```

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MAINDEC-11-DZDJIA-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 33
DZDJAD.P11 TST32: TEST ALL OF LINE 0 TRANSMIT AND RECEIVE LOGIC

1498	005660	104001		HLT+1	:ERROR IN RECEIVED CHAR
1499					:R1 = CONTENTS OF RBUF
1500					:BIT14=UART OVERRUN
1501					:BIT13=FRAMING ERROR
1502					:BIT12=PARITY ERROR
1503	005662	010102		4\$: MOV R1, R2	:DUPLICATE DATA WORD
1504	005664	042702	170377	SIC #170377,R2	:MASK LINE#
1505	005670	000302		SWAB R2	:LINE # IN LOW BYTE
1506	005672	122702	000000	CMPB #0.. R2	:CHECK LINE #
1507	005676	001401		BEQ .+4	:BRANCH IF OK
1508	005700	104001		HLT+1	:WRONG LINE # RECEIVED
1509					:R1 = CONTENTS OF RBUF
1510					:BITS8-11 = LINE #
1511	005702	117702	173400	5\$: MOVS #DJLEN, R2	:GET MASK OF CHARACTER
1512	005706	130201		BITB R2, R1	:CHECK CHAR LENGTH.
1513	005710	001401		BEQ .+4	:BRANCH IF OK
1514	005712	104002		HLT+2	:WRONG CHARACTER LENGTH
1515					:R1=DATA FROM FI/FO
1516					:R2=MASK (BITS SET NOT EXPECTED)
1517	005714	105102		6\$: COMB R2	:REVERSE THE MASK
1518	005716	120102		CMPB R1, R2	:CHECK THE ACTURAL DATA
1519	005720	001401		BEQ .+4	:BRANCH IF OK
1520	005722	104002		HLT+2	:WRONG CHAR LEN OR DATA ERROR
1521					:R1=DATA FROM FI/FO (COMPLETE WORD)
1522					:R2=DATA (LOW BYTE) EXPECTED
1523	005724	017701	173262	7\$: MOV @RBUF, R1	:READ FI/FO
1524	005730	100001		BPL .+4	:BRANCH IF CHAR PRESENT NOT SET
1525	005732	104001		HLT+1	:CHARACTER PRESENT STAYED SET
1526					:R1 = CONTENTS OF RBUF
1527	005734	017701	173250	8\$: MOV @CSR, R1	:SAVE THE CSR
1528	005740	022701	100405	CMP #100405,R1	:CHECK THE CSR
1529	005744	001401		BEQ .+4	:BRANCH IF OK
1530	005746	104001		HLT+1	:DONE DIDN'T CLEAR OR OTHER CSR ERROR
1531					:R1 = CONTENTS OF CSR
1532	005750	005077	173240	CLR @TCR	:CLEAR TCR
1533	005754	005077	173230	CLR @CSR	:CLEAR CSR
1534	005760	104400		SCOPE	

1535 :*****
1536 :TEST 33: TEST THAT LINE 1 CAN TRANSMIT AND
1537 :RECEIVE A CHARACTER. (377)
1538 :1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
1539 :2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
1540 :3\$: CHECKS THAT NO ERRORS IN FI/FO
1541 :4\$: CHECKS THAT RIGHT LINE # (1) IN FI/FO
1542 :5\$: CHECKS FOR RIGHT CHARACTER LENGTH
1543 :6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
1544 :7\$: CHECKS THAT CHARACTER PRESENT CLEARS
1545 :8\$: CHECKS THAT DONE CLEARS
1546 :PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES
1547 :*****

1548 :INITIALIZE
1549 :DEVICE "CSR" REGISTER

1550 :SET:
1551 :TST33: JSR FC, @#INITD ;BIT2 = MAINTENANCE

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MAINDEC-11-DZDJAD.D
DZDJAD.P11 TST33: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 34

1554								:BIT3 = CLEAR MOS	
1555								;BIT8 = MASTER XMTR SCAN ENB	
1556									
1557								SET:	
1558								;BIT0 = RECEIVER ENABLE	
1559									
1560	005766	052777	000002	173220					
1561	005774	017701	173210		LOP33:	BIS	#BIT1,	@TCR	;SET XMTR CONTROL BIT, LINE 1
1562	006000	100375				MOV	0CSR,	R1	;WAIT FOR XMTR READY
1563	006002	012777	000377	173206		SPL	LOP33		
1564	006010	005000				MOV	#377,	@TBUF	;SEND A RUBOUT
1565	006012	105305				CLR	R0		;CLEAR COUNTER
1566	006014	001376				DECB	R5		;SHORT WAIT LOOP
1567	006016	105777	173166			BNE	1\$		
1568	006022	100405				TSTB	0CSR		;WAIT FOR DONE
1569	006024	005200				BMI	2\$;BRANCH WHEN DONE
1570	006026	001371				INC	R0		;TIME COUNTER
1571	006030	017701	173154			BNE	1\$;BRANCH IF NOT TIME-OUT
1572	006034	104001				MOV	0CSR,	R1	;SAVE CSR
1573						HLT+1			;DONE NEVER CAME UP
1574	006036	050037	001302		2\$:	BIS	R0,	TIMER	;R1 = CONTENTS OF CSR
1575	006042	017701	173144			MOV	0RBUF,	R1	;SAVE TIMER
1576	006046	100401				BMI	.+4		;READ THE FI/FO
1577	006050	104001				HLT+1			;BRANCH IF CHARACTER READY
1578									;CHARACTER READY DIDN'T SET
1579	006052	032701	070000		3\$:	BIT	#70000,	R1	;R1 = CONTENTS OF RBUF
1580	006056	001401				BEQ	.+4		;CHECK FOR ERROR BITS
1581	006060	104001				HLT+1			;BRANCH IF NONE
1582									;ERROR IN RECEIVED CHAR
1583									;R1 = CONTENTS OF RBUF
1584									;BIT14=UART OVERRUN
1585									;BIT13=FRAMING ERROR
1586	006062	010102			4\$:	MOV	R1,	R2	;BIT12=PARITY ERROR
1587	006064	042702	170377			BIC	#170377,R2		;DUPLICATE DATA WORD
1588	006070	000302				SWAB	R2		;MASK LINE#
1589	006072	122702	000001			CMPB	#1.,	R2	;LINE # IN LOW BYTE
1590	006076	001401				BEQ	.+4		;CHECK LINE #
1591	006100	104001				HLT+1			;BRANCH IF OK
1592									;WRONG LINE # RECEIVED
1593									;R1 = CONTENTS OF RBUF
1594	006102	117702	173200		5\$:	MOV	0DJLEN,	R2	;BITS8-11 = LINE #
1595	006106	130201				BITB	R2,	R1	;GET MASK OF CHARACTER
1596	006110	001401				BEQ	.+4		;CHECK CHAR LENGTH.
1597	006112	104002				HLT+2			;BRANCH IF OK
1598									;WRONG CHARACTER LENGTH
1599									;R1=DATA FROM FI/FO
1600	006114	105102			6\$:	COMB	R2		;R2=MASK (BITS SET NOT EXPECTED)
1601	006116	120102				CMPB	R1,		;REVERSE THE MASK
1602	006120	001401				BEQ	.+4		;CHECK THE ACTURAL DATA
1603	006122	104002				HLT+2			;BRANCH IF OK
1604									;WRONG CHAR LEN OR DATA ERROR
1605									;R1=DATA FROM FI/FO (COMPLETE WORD)
1606	006124	017701	173062		7\$:	MOV	0RBUF,	R1	;R2=DATA (LOW BYTE) EXPECTED
1607	006130	100001				BPL	.+4		;READ FI/FO
1608	006132	104001				HLT+1			;BRANCH IF CHAR PRESENT NOT SET
1609									;CHARACTER PRESENT STAYED SET
									;R1 = CONTENTS OF RBUF

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MAINDEC-11-DZDJA-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 35
DZDJA.D.P11 TST33: TEST ALL OF LINE 1 TRANSMIT AND RECEIVE LOGIC

```

1610 006134 017701 173050      9$:    MOV     @CSR, R1      ;SAVE THE CSR
1611 006140 022701 100405      CMP     #100405,R1    ;CHECK THE CSR
1612 006144 001401              BEQ     .+4        ;BRANCH IF OK
1613 006146 104001              HLT+1   .          ;DONE DIDN'T CLEAR OR OTHER CSR ERROR
1614 006150 005077 173040      CLR     @TCR       ;CLEAR TCR
1615 006154 005077 173030      CLR     @CSR       ;CLEAR CSR
1616 006160 104400

```

TEST 34: TEST THAT LINE 2 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2\$: CHECKS THAT CHAR PRESENT IS IN FI/F0
3\$: CHECKS THAT NO ERRORS IN FI/F0
4\$: CHECKS THAT RIGHT LINE # (2) IN FI/F0
5\$: CHECKS FOR RIGHT CHARACTER LENGTH
6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
7\$: CHECKS THAT CHARACTER PRESENT CLEARS
8\$: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

INITIALIZE
DEVICE "CSR" REGISTER

TST34: JSR PC, 3#INITD SET:
BIT2 = MAINTENANCE
BIT3 = CLEAR MOS
BIT0 = MASTER XMTB SCBN END

:WAIT FOR MOS TO CLEAR
;BITS = MASTER AFTER SCRN END
SET:
;BIT0 = RECEIVER ENABLE

1643	006166	052777	000004	173020		BIS	#BIT2.	STCR	SET XMTR CONTROL BIT, LINE 2
1644	006174	017701	173010		LOP34:	MOV	#CSR,	R1	WAIT FOR XMTR READY
1645	006200	100375				BPL	LOP34		
1646	006202	012777	000377	173006		MOV	#377,	BTBUF	SEND A RUBOUT
1647	006210	005000				CLR	RO		CLEAR COUNTER
1648	006212	105305			1\$:	DEC B	RS		SHORT WAIT LOOP
1649	006214	001376				BNE	1\$		
1650	006216	105777	172766			TSTB	#CSR		WAIT FOR DONE
1651	006222	100405				BMI	2\$		BRANCH WHEN DONE
1652	006224	005200				INC	RO		TIME COUNTER
1653	006226	001371				BNE	1\$		BRANCH IF NOT TIME-OUT
1654	006230	017701	172754			MOV	#CSR,	R1	SAVE CSR
1655	006234	104001				HLT+1			DONE NEVER CAME UP
1656									R1 = CONTENTS OF CSR
1657	006236	050037	001302		2\$:	BIS	RO,	TIMER	SAVE TIMER
1658	006242	017701	172744			MOV	#RBUF,	R1	READ THE FI/FO
1659	006246	100401				BMI	.+4		BRANCH IF CHARACTER READY
1660	006250	104001				HLT+1			CHARACTER READY DIDN'T SET
1661									R1 = CONTENTS OF RBUF
1662	006252	032701	070000		3\$:	BIT	#70000,	R1	CHECK FOR ERROR BITS
1663	006256	001401				BEQ	.+4		BRANCH IF NONE
1664	006260	104001				HLT+1			ERROR IN RECEIVED CHAR
1665									R1 = CONTENTS OF RBUF

M03

MAINDEC-11-DZDJAD-D
DZDJAD.PII TST34: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 36

1666						:BIT14=UART OVERRUN
1667						:BIT13=FRAMING ERROR
1668						:BIT12=PARITY ERROR
1669	006262	010102		4\$:	MOV R1, R2	:DUPLICATE DATA WORD
1670	006264	042702	170377		BIC #170377,R2	:MASK LINE#
1671	006270	000302			SWAB R2	:LINE # IN LOW BYTE
1672	006272	122702	000002		CMPB #2., R2	:CHECK LINE #
1673	006276	001401			BEQ .+4	:BRANCH IF OK
1674	006300	104001			HLT+1	:WRONG LINE # RECEIVED
1675						:R1 = CONTENTS OF RBUF
1676						:BITS8-11 = LINE #
1677	006302	117702	173000	5\$:	MOVB @DJLEN, R2	:GET MASK OF CHARACTER
1678	006306	130201			BITB R2, R1	:CHECK CHAR LENGTH.
1679	006310	001401			BEQ .+4	:BRANCH IF OK
1680	006312	104002			HLT+2	:WRONG CHARACTER LENGTH
1681						:R1=DATA FROM FI/FO
1682						:R2=MASK (BITS SET NOT EXPECTED)
1683	006314	105102		6\$:	COMB R2	:REVERSE THE MASK
1684	006316	120102			CMPB R1, R2	:CHECK THE ACTURAL DATA
1685	006320	001401			BEQ .+4	:BRANCH IF OK
1686	006322	104002			HLT+2	:WRONG CHAR LEN OR DATA ERROR
1687						:R1=DATA FROM FI/FO (COMPLETE WORD)
1688						:R2=DATA (LOW BYTE) EXPECTED
1689	006324	017701	1726EE	7\$:	MOV @RBUF, R1	:READ FI/FO
1690	006330	100001			BPL .+4	:BRANCH IF CHAR PRESENT NOT SET
1691	006332	104001			HLT+1	:CHARACTER PRESENT STAYED SET
1692						:R1 = CONTENTS OF RBUF
1693	006334	017701	172650	8\$:	MOV @CSR, R1	:SAVE THE CSR
1694	006340	022701	100405		CMP #100405,R1	:CHECK THE CSR
1695	006344	001401			BEQ .+4	:BRANCH IF OK
1696	006346	104001			HLT+1	:DONE DIDN'T CLEAR OR OTHER CSR ERROR
1697						:R1 = CONTENTS OF CSR
1698	006350	005077	172640		CLR @TCR	:CLEAR TCR
1699	006354	005077	172630		CLR @CSR	:CLEAR CSR
1700	006360	104400			SCOPE	
1701						
1702						*****
1703						TEST 35: TEST THAT LINE 3 CAN TRANSMIT AND
1704						RECEIVE A CHARACTER. (377)
1705				1\$:	CHECKS THAT DONE SETS IN REASONABLE TIME.	
1706				2\$:	CHECKS THAT CHAR PRESENT IS IN FI/FO	
1707				3\$:	CHECKS THAT NO ERRORS IN FI/FO	
1708				4\$:	CHECKS THAT RIGHT LINE # (3) IN FI/FO	
1709				5\$:	CHECKS FOR RIGHT CHARACTER LENGTH	
1710				6\$:	CHECKS THAT CORRECT DATA WAS RECEIVED	
1711				7\$:	CHECKS THAT CHARACTER PRESENT CLEARS	
1712				8\$:	CHECKS THAT DONE CLEARS	
1713					PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES	
1714					*****	
1715						
1716						
1717						
1718						
1719	006362	004737	015566		INITIALIZE DEVICE "CSR" REGISTER	
1720				TST35: JSR PC, @#INITD	SET: :BIT2 = MAINTENANCE :BIT3 = CLEAR MOS :BITS = MASTER XMTR SCAN ENB	
1721						

NO3

MAINDEC-11-D2DJA-D
D2DJA.D.PII TST35: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 37
TEST ALL OF LINE 3 TRANSMIT AND RECEIVE LOGIC

1722							:WAIT FOR MOS TO CLEAR		
1723									
1724								SET: ;BIT0 = RECEIVER ENABLE	
1725									
1726	006366	052777	000010	172620		BIS	#BIT3,	@TOR	;SET XMTR CONTROL BIT, LINE 3
1727	006374	017701	172610		LOP35:	MOV	#CSR,	R1	;WAIT FOR XMTR READY
1728	006400	100375				SPL	LOP35		
1729	006402	012777	000377	172606		MOV	#377,	@TBUF	;SEND A RUBOUT
1730	006410	005000				CLR	RO		;CLEAR COUNTER
1731	006412	105305				DECB	R5		;SHORT WAIT LOOP
1732	006414	001376				BNE	1\$		
1733	006416	105777	172566			TSTB	#CSR		;WAIT FOR DONE
1734	006422	100405				BMI	2\$;BRANCH WHEN DONE
1735	006424	005200				INC	RO		;TIME COUNTER
1736	006426	001371				BNE	1\$;BRANCH IF NOT TIME-OUT
1737	006430	017701	172554			MOV	#CSR,	R1	;SAVE CSR
1738	006434	104001				HLT+1			;DONE NEVER CAME UP
1739									R1 = CONTENTS OF CSR
1740	006436	050037	001302		2\$:	BIS	RO,	TIMER	;SAVE TIMER
1741	006442	017701	172544			MOV	#RBUF,	R1	;READ THE FI/FO
1742	006446	100401				BMI	.+4		;BRANCH IF CHARACTER READY
1743	006450	104001				HLT+1			;CHARACTER READY DIDN'T SET
1744									R1 = CONTENTS OF RBUF
1745	006452	032701	070000		3\$:	BIT	#70000,	R1	;CHECK FOR ERROR BITS
1746	006456	001401				BEQ	.+4		;BRANCH IF NONE
1747	006460	104001				HLT+1			;ERROR IN RECEIVED CHAR
1748									R1 = CONTENTS OF RBUF
1749									BIT14=UART OVERRUN
1750									BIT13=FRAMING ERROR
1751									BIT12=PARITY ERROR
1752	006462	010102			4\$:	MOV	R1,	R2	;DUPLICATE DATA WORD
1753	006464	042702	170377			BIC	#170377,R2		;MASK LINE#
1754	006470	000302				SWAB	R2		;LINE # IN LOW BYTE
1755	006472	122702	000003			CMPB	#3.,	R2	;CHECK LINE #
1756	006476	001401				BEQ	.+4		;BRANCH IF OK
1757	006500	104001				HLT+1			;WRONG LINE # RECEIVED
1758									R1 = CONTENTS OF RBUF
1759									BITS8-11 = LINE #
1760	006502	117702	172600		5\$:	MOV	#DJLEN,	R2	;GET MASK OF CHARACTER
1761	006506	130201				BITB	R2,	R1	;CHECK CHAR LENGTH.
1762	006510	001401				BEQ	.+4		;BRANCH IF OK
1763	006512	104002				HLT+2			;WRONG CHARACTER LENGTH
1764									R1=DATA FROM FI/FO
1765									R2=MASK (BITS SET NOT EXPECTED)
1766	006514	105102			6\$:	COMB	R2		;REVERSE THE MASK
1767	006516	120102				CMPB	R1,	R2	;CHECK THE ACTURAL DATA
1768	006520	001401				BEQ	.+4		;BRANCH IF OK
1769	006522	104002				HLT+2			;WRONG CHAR LEN OR DATA ERROR
1770									R1=DATA FROM FI/FO (COMPLETE WORD)
1771									R2=DATA (LOW BYTE) EXPECTED
1772	006524	017701	172462		7\$:	MOV	#RBUF,	R1	;READ FI/FO
1773	006530	100001				BPL	.+4		;BRANCH IF CHAR PRESENT NOT SET
1774	006532	104001				HLT+1			;CHARACTER PRESENT STAYED SET
1775									R1 = CONTENTS OF RBUF
1776	006534	017701	172450		8\$:	MOV	#CSR,	R1	;SAVE THE CSR
1777	006540	022701	100405			CMP	#100405,R1		;CHECK THE CSR

221520-11-0220A-D
TST36: ROM LOGIC TESTS MACYLL 27(732) 21-SEP-76 13:43 PAGE 39

006543	004401		B60	.+4	BRANCH IF OK
006546	004501		HLT+1		DONE DIDN'T CLEAR OR OTHER CSR ERROR
006549	005027	172430	CLEAR	RIOR	RI = CONTENTS OF CSR
006550	005027	172430	MOV#FF	DCSR	CLEAR TOR
006551	005027	172430	MOV#FF	DCSR	CLEAR CSR
006552	005027	015770	MOV	DLLEN	
				8.+6,	LAD

TEST 36: TEST THAT LINE 4 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
: CHECKS THAT DONE SETS IN REASONABLE TIME.
: CHECKS THAT CHAR PRESENT IS IN FIFO
: CHECKS THAT NO ERRORS IN FIFO
: CHECKS THAT RIGHT LINE 8 (4) IN FIFO
: CHECKS FOR RIGHT CHARACTER LENGTH
: CHECKS THAT CORRECT DATA WAS RECEIVED
: CHECKS THAT CHARACTER PRESENT CLEARS
: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; LART CARD 003 SERIES

006574	004737	015566	INITIALIZE DEVICE"CSR"REGISTER				
			TST36:	JSR	PC, S=INIT0		
					SET: :BIT0 = MAINTENANCE :BIT0 = CLEAR MOS :BIT0 = MASTER XMTR SCAN ENB		
					SET: :BIT0 = RECEIVER ENABLE		
006600	052777	000020	172405	LOP36:	BIS	BIT4, R1	SET XMTR CONTROL BIT, LINE 4
006600	017701	172376	172405		MOV	CSR	WAIT FOR XMTR READY
006600	100377	000377	172374		CLR	CSR	
006600	017701				MOV#0	CSR	
006600	105777				INC	CSR	
006600	005200				MOV#0	CSR	
006600	017701				MOV	CSR	
006600	104001				HLT+1	R1	
006600	050037	001000		BB:	BIS	RI, TIMER	
006600	017701	172302			MOV	RBUF, RI	
006600	050037				TRMI	.+4	
006600	017701				HLT+1		
006600	006701	070000		BB:	BIT	#70000, RI	
006600	017701				MOV	.+4	

:SET:
:BIT0 = CLEAR MOS
:BIT0 = MASTER XMTR SCAN ENB

SET:
:BIT0 = RECEIVER ENABLE

SET XMTR CONTROL BIT, LINE 4
WAIT FOR XMTR READY

SEND A RUBOUT
CLEAR COUNTER
SHORT WAIT LOOP

WAIT FOR DONE
BRANCH WHEN DONE
TIME COUNTER
BRANCH IF NOT TIME-OUT
SAVE CSR
DONE NEVER CAME UP
RI = CONTENTS OF CSR

SAVE TIMER
READ THE FIFO
BRANCH IF CHARACTER READY
CHARACTER READY DIDN'T SET
RI = CONTENTS OF RBUF

CHECK FOR ERROR BITS
BRANCH IF NONE
ERROR IN RECEIVED CHAR
RI = CONTENTS OF RBUF

D04

MAINCODE-11-02208-2 0011 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 40
TEST ALL OF LINE 5 TRANSMIT AND RECEIVE LOGIC

:WAIT FOR MOS TO CLEAR							
SET: ;BIT0 = RECEIVER ENABLE							
007000	052777	000040	172206				:SET XMTR CONTROL BIT, LINE 5
007006	017701	172176		L0P37:	BIS	#BITS.	:WAIT FOR XMTR READY
007013	100377				MOV	#05R	
007019	012677	000377	172174		BPL	L0P37	R1
007025	00650000				MOV	#377.	BTBUF
007026	105376			13:	CLR	R0	
007030	105777	172154			DECB	R5	
007034	100405				BNE	15	
007036	0065200				TSTB	#0CSR	
007040	001371				OMT	#0CSR	
007044	017701	172142			INC	R0	
007046	104001				BNE	15	
					MOV	#CSR.	R1
					HLT+1		
007050	050037	001302		23:	BIS	R0	
007054	017701	172132			MOV	BRBUF.	TIMER
007056	100401				BMI	.+4	
007058	104001				HLT+1		
007064	032701	070000		33:	BIT	#70000.	R1
007070	001401				NEQ	.+4	
007072	104001				HLT+1		
007074	010102			43:	MOV	R1	
007076	042702	170377			BIC	#170377.R2	
007104	000300				SHAB	R0	
007105	122702	000005			CMPB	#5..	R2
007110	001401				BEQ	.+4	
007112	104001				HLT+1		
007114	117702	172166		53:	MOVB	#DJLEN.	R2
007116	120201				BITB	R2.	R1
007118	001401				BEQ	.+4	
007124	104002				HLT+2		
007126	105102			63:	COMB	R2	
007130	120102				CMPB	RI.	R2
007132	001401				BEQ	.+4	
007134	104002				HLT+2		
007136	017701	172050		75:	MOV	BRBUF.	R1
007140	100001				BPL	.+4	
007144	104001				HLT+1		
007146	017701	172036		85:	MOV	#CSR.	R1
007150	022701	100405			CMP	#100405.R1	

E04

MAINDEC-11-DZDJR-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 41
DZDJR.D, TST37: TEST ALL OF LINE 5 TRANSMIT AND RECEIVE LOGIC

007156	001401		BEQ	.+4	:BRANCH IF OK				
007150	104001		HLT+1		:DONE DIDN'T CLEAR OR OTHER CSR ERROR				
007160	005022	172026	CLR	#TCSR	:R1 = CONTENTS OF CSR				
007166	005022	172016	CLR	#CSR	:CLEAR TCSR				
007172	104400		SCOPE		:CLEAR CSR				

TEST 40: TEST THAT LINE 6 CAN TRANSMIT AND RECEIVE A CHARACTER. (377)									
1\$:					CHECKS THAT DONE SETS IN REASONABLE TIME.				
2\$:					CHECKS THAT CHAR PRESENT IS IN FI/FO				
3\$:					CHECKS THAT NO ERRORS IN FI/FO				
4\$:					CHECKS THAT RIGHT LINE # (6) IN FI/FO				
5\$:					CHECKS FOR RIGHT CHARACTER LENGTH				
6\$:					CHECKS THAT CORRECT DATA WAS RECEIVED				
7\$:					CHECKS THAT CHARACTER PRESENT CLEARS				
8\$:					CHECKS THAT DONE CLEARS				
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD DOB SERIES									

INITIALIZE DEVICE "CSR" REGISTER									
007174	004737	015566	TST40:	JSR	PC,				
					S#INITD				
					SET: :BIT2 = MAINTENANCE :BIT3 = CLEAR MOS :BIT8 = MASTER XMTR SCAN ENB				
					SET: :BIT0 = RECEIVER ENABLE				
					WAIT FOR MOS TO CLEAR				
					:				
007200	052777	000100	172006	LOP40:	BIS	#BITS.	#TCSR	RI	:SET XMTR CONTROL BIT, LINE 6
007206	017701	171776			MOV	#CSR,	R1		:WAIT FOR XMTR READY
007210	100375				BPL	LOP40			
007214	012777	000377	171774		MOV	#377.	#TBUF		:SEND A RUBOUT
007222	005000				CLR	RO			:CLEAR COUNTER
007224	105305				DEC#	#5			:SHORT WAIT LOOP
007226	001376				BNE	1\$			
007230	105777	171754			TSTB	#CSR			:WAIT FOR DONE
007234	100405				BMI	2\$:BRANCH WHEN DONE
007236	005200				INC	RO			:TIME COUNTER
007240	001371				BNE	1\$:BRANCH IF NOT TIME-OUT
007242	017701	171742			MOV	#CSR,	R1		:SAVE CSR
007246	104001				HLT+1				:DONE NEVER CAME UP
									:R1 = CONTENTS OF CSR
007250	050037	001302		2\$:	BIS	RO.			:SAVE TIMER
007254	017701	171732			MOV	#RBUF,	R1		:READ THE FI/FO
007260	100401				BMI	.+4			:BRANCH IF CHARACTER READY
007262	104001				HLT+1				:CHARACTER READY DIDN'T SET
									:R1 = CONTENTS OF RBUF
007264	032701	070000		3\$:	BIT	#70000.	R1		:CHECK FOR ERROR BITS
007270	001401				BEQ	.+4			:BRANCH IF NONE
007272	104001				HLT+1				:ERROR IN RECEIVED CHAR
									:R1 = CONTENTS OF RBUF
									:BIT14=UART OVERRUN
									:BIT13=FRAMING ERROR

MARINDEC-11-0200A-D
0200A-D.F11 TST40: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 42
TEST ALL OF LINE 5 TRANSMIT AND RECEIVE LOGIC

0002							:BIT12=PARITY ERROR
0003	007324	010102		4\$: MOV	R1	R2	DUPLICATE DATA WORD
0004	007326	042703	170377	B1C	\$170377,R2		MASK LINE#
0005	007302	000306		SWAB	R2		LINE # IN LOW BYTE
0006	007304	122702	000006	CMPB	#6..	R2	CHECK LINE #
0007	007310	001401		BEQ	.+4		BRANCH IF OK
0008	007312	104001		HLT+1			WRONG LINE # RECEIVED
0009							R1 = CONTENTS OF RBUF
0010							BITS8-11 = LINE #
0011	007314	117702	171766	5\$: MOVB	00JLEN,	R2	GET MASK OF CHARACTER
0012	007320	130201		B1B	R2,	R1	CHECK CHAR LENGTH.
0013	007322	001401		BEQ	.+4		BRANCH IF OK
0014	007324	104002		HLT+2			WRONG CHARACTER LENGTH
0015							R1=DATA FROM FI/FO
0016							R2=MASK (BITS SET NOT EXPECTED)
0017	007326	105102		6\$: COMB	R2		REVERSE THE MASK
0018	007330	120102		CMPB	R1,	R2	CHECK THE ACTURAL DATA
0019	007332	001401		BEQ	.+4		BRANCH IF OK
0020	007334	104002		HLT+2			WRONG CHAR LEN OR DATA ERROR
0021							R1=DATA FROM FI/FO (COMPLETE WORD)
0022							R2=DATA (LOW BYTE) EXPECTED
0023	007336	017701	171650	7\$: MOV	0RBUF,	R1	READ FI/FO
0024	007342	100001		BPL	.+4		BRANCH IF CHAR PRESENT NOT SET
0025	007344	104001		HLT+1			CHARACTER PRESENT STAYED SET
0026							R1 = CONTENTS OF RBUF
0027	007346	017701	171636	8\$: MOV	0CSR,	R1	SAVE THE CSR
0028	007352	022701	100405	CMP	\$100405,R1		CHECK THE CSR
0029	007356	001401		BEQ	.+4		BRANCH IF OK
0030	007360	104001		HLT+1			DONE DIDN'T CLEAR OR OTHER CSR ERROR
0031							R1 = CONTENTS OF CSR
0032	007362	005077	171626	CLR	0TOR		CLEAR TCR
0033	007366	005077	171616	CLR	0CSR		CLEAR CSR
0034	007372	104400		SCOPE			

TEST 41: TEST THAT LINE 7 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3\$: CHECKS THAT NO ERRORS IN FI/FO
4\$: CHECKS THAT RIGHT LINE # (7) IN FI/FO
5\$: CHECKS FOR RIGHT CHARACTER LENGTH
6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
7\$: CHECKS THAT CHARACTER PRESENT CLEARS
8\$: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

INITIALIZE
DEVICE "CSR" REGISTER

007374 004737 015566 TST41: JSR PC, 0INITD

SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENS

:WAIT FOR MOS TO CLEAR

SET:

G04

MAINDEC-11-DZDJR-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 43
DZDJR.D.PII TST41: TEST ALL OF LINE 7 TRANSMIT AND RECEIVE LOGIC

								BIT0 = RECEIVER ENABLE
007400	052777	000200	171606	:				SET XMTR CONTROL BIT. LINE 7
007406	017701	171576		L0P41:	BIS	#BIT7.	BTCR	WAIT FOR XMTR READY
007412	100375				MOV	0CSR	R1	
007414	012777	000377	171574		BPL	L0P41		
007422	005000			1\$:	MOV	#377,	BTBUF	SEND A RUBOUT
007424	105305				CLR	RD		CLEAR COUNTER
007426	001376				DEC8	RD		SHORT WAIT LOOP
007430	105777	171554			SNE	1\$		
007434	100405				TSTB	0CSR		WAIT FOR DONE
007436	006200				BMI	RD		BRANCH WHEN DONE
007440	001371				INC	RD		TIME COUNTER
007444	017701	171542			BNE	1\$		BRANCH IF NOT TIME-OUT
007446	104001				MOV	0CSR,	R1	SAVE CSR
					HLT+1			DONE NEVER CAME UP
007450	050037	001302		23:	BIS	RD,	TIMER	R1 = CONTENTS OF CSR
007454	017701	171532			MOV	0RBUF,	R1	SAVE TIMER
007456	100401				BMI	.+4		READ THE FI/FO
007458	104001				HLT+1			BRANCH IF CHARACTER READY
007464	032701	070000		35:	BIT	#70000,	R1	CHARACTER READY DIDN'T SET
007470	001401				BEQ	.+4		R1 = CONTENTS OF RBUF
007472	104001				HLT+1			CHECK FOR ERROR BITS
								BRANCH IF NONE
007474	010102			45:	MOV	R1,	R2	ERROR IN RECEIVED CHAR
007478	042702	170377			0INR	#0377,R2		R1 = CONTENTS OF RBUF
007502	000302				0INR			BIT14=UART OVERRUN
007504	122702	000007			CMPS	#7..,	R2	BIT13=FRAMING ERROR
007510	001401				BEC	.+4		BIT12=PARITY ERROR
007512	104001				HLT+1			DUPLICATE DATA WORD
007514	117702	171566		55:	MOV	R1,	R2	MASK LINE#
007520	130201				0ITE	#0377,R2		LINE # IN LOW BYTE
007522	001401				BEQ	.+4		CHECK LINE #
007524	104002				HLT+2			BRANCH IF OK
007526	105102			65:	COMB	R2		WRONG LINE # RECEIVED
007528	120102				CMPS	R1,	R2	R1 = CONTENTS OF RBUF
007530	001401				BEC	.+4		BITS8-11 = LINE #
007534	104002				HLT+2			GET MASK OF CHARACTER
007536	017701	171450		75:	MOV	0RBUF,	R1	CHECK CHAR LENGTH.
007542	100001				BPL	.+4		BRANCH IF OK
007544	104001				HLT+1			WRONG CHARACTER LENGTH
007546	017701	171436		85:	MOV	0CSR,	R1	R1=DATA FROM FI/FO
007548	022701	100405			CMP	#100405,R1		R2=MASK (BITS SET NOT EXPECTED)
007550	001401				BEQ	.+4		REVERSE THE MASK
007552	104001				HLT+1			CHECK THE ACTURAL DATA
007554	017701	171436		95:	MOV	0CSR,	R1	BRANCH IF OK
007556	022701	100405			CMP			WRONG CHAR LEN OR DATA ERROR
007558	001401				BEQ			R1=DATA FROM FI/FO (COMPLETE WORD)
007560	104001				HLT+1			R2=DATA (LOW BYTE) EXPECTED
								READ FI/FO
								BRANCH IF CHAR PRESENT NOT SET
								CHARACTER PRESENT STAYED SET
								R1 = CONTENTS OF RBUF
								SAVE THE CSR
								CHECK THE CSR
								BRANCH IF OK
								DONE DIDN'T CLEAR OR OTHER CSR ERROR

MAINDEC-11-DZDJ-A-D MACY11 27(732) 21-SEP-76 13:43 PAGE 44
 TEST41: TEST ALL OF LINE 7 TRANSMIT AND RECEIVE LOGIC

007562	005077	171426	CLR	STCR	:R1 = CONTENTS OF CSR
007566	005077	171416	CLR	DCSR	:CLEAR TCR
007570	104400		SCOPE		:CLEAR CSR
007574	005237	001306	INC	DJLEN	
007580	012737	007606	MOV	*.+6, LAD	

 TEST 42: TEST THAT LINE 8 CAN TRANSMIT AND
 RECEIVE A CHARACTER. (377)
 1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
 2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
 3\$: CHECKS THAT NO ERRORS IN FI/FO
 4\$: CHECKS THAT RIGHT LINE # (8) IN FI/FO
 5\$: CHECKS FOR RIGHT CHARACTER LENGTH
 6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
 7\$: CHECKS THAT CHARACTER PRESENT CLEARS
 8\$: CHECKS THAT DONE CLEARS
 PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

INITIALIZE
 DEVICE "CSR" REGISTER

007606	004737	015566	TST42: JSR PC, 3#INITD	SET: :BIT2 = MAINTENANCE :BIT3 = CLEAR MOS :BIT3 = MASTER XMTR SCAN ENB
WAIT FOR MOS TO CLEAR				
007612	052777	000400	171374	LOP42: BIS #BIT8, STCR R1 :SET XMTR CONTROL BIT, LINE 8
007620	017701	171364	171374	MOV DCSR, R1 :WAIT FOR XMTR READY
007624	100375			BPL LOP42
007626	012777	000377	171362	MOV #377, RTBUF :SEND A RUBOUT
007634	005000			CLR RO :CLEAR COUNTER
007636	105305			DEC B R5 :SHORT WAIT LOOP
007640	001376			BNE 1\$
007642	105777	171342		TSTB 2CSR :WAIT FOR DONE
007646	100405			BMI 2\$:BRANCH WHEN DONE
007650	005200			INC RO :TIME COUNTER
007652	001371			BNE 1\$:BRANCH IF NOT TIME-OUT
007654	017701	171330		MOV DCSR, R1 :SAVE CSR
007660	104001			HLT+1 :DONE NEVER CAME UP
007662	050037	001302		R1 = CONTENTS OF CSR
007666	017701	171320	2\$: BIS RO, TIMER	SAVE TIMER
007672	100401		MOV 2RBUF, R1	READ THE FI/FO
007674	104001		BMI .+4	BRANCH IF CHARACTER READY
007676	032701	070000	HLT+1	CHARACTER READY DIDN'T SET
007702	001401		3\$: BIT BEQ .+4	R1 = CONTENTS OF RBUF
007704	104001		HLT+1	CHECK FOR ERROR BITS

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MAINDEC-11-DZDJIA-D 101
DZDJIA-D.FII TST42: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 45
TEST ALL OF LINE 9 TRANSMIT AND RECEIVE LOGIC

2170							
2171	007706	010102					
2172	007710	042702	170377	4\$:	MOV BIC SWAB CMPS BEQ HLT+1	R1 #170377,R2 R2 #8., R2 .+4	;BIT12=PARITY ERROR DUPLICATE DATA WORD MASK LINE# LINE # IN LOW BYTE CHECK LINE # BRANCH IF OK WRONG LINE # RECEIVED R1 = CONTENTS OF RBUF BITS8-11 = LINE # GET MASK OF CHARACTER CHECK CHAR LENGTH. BRANCH IF OK WRONG CHARACTER LENGTH R1=DATA FROM FI/FO R2=MASK (BITS SET NOT EXPECTED)
2173	007714	000302					
2174	007716	122702	000010				
2175	007722	001401					
2176	007724	104001					
2177							
2178	007726	117702	171354	5\$:	MOVB BITB BEQ HLT+2	SDJLEN, R2 R2, R1 .+4	
2179	007732	130201					
2180	007734	001401					
2181	007736	104002					
2182							
2183	007740	105102		6\$:	COMB CMPS BEQ HLT+2	R2 R1, R2 .+4	
2184	007742	120102					
2185	007744	001401					
2186	007746	104002					
2187							
2188	007750	017701	171235	7\$:	MOV BPL HLT+1	DRBUF, R1 .+4	
2189	007754	100001					
2190	007756	104001					
2191							
2192	007760	017701	171224	8\$:	MOV CMP BEQ HLT+1	DCSR, R1 #100405,R1 .+4	
2193	007764	022701	100405				
2194	007770	001401					
2195	007772	104001					
2196							
2197	007774	005077	171214		CLR CLR SCOPE	ATCR ACSR	
2198	010000	005077	171204				
2199	010004	104400					
2200							
2201							
2202							

TEST 43: TEST THAT LINE 9 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1S: CHECKS THAT DONE SETS IN REASONABLE TIME.
2S: CHECKS THAT CHAR PRESENT IS IN FI/FO
3S: CHECKS THAT NO ERRORS IN FI/FO
4S: CHECKS THAT RIGHT LINE # (9) IN FI/FO
5S: CHECKS FOR RIGHT CHARACTER LENGTH
6S: CHECKS THAT CORRECT DATA WAS RECEIVED
7S: CHECKS THAT CHARACTER PRESENT CLEARS
8S: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

INITIALIZE
DEVICE "CSR" REGISTER

010006 004737 015566

TST43: JSR PC, 0#INITD ;SET:
;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BIT8 = MASTER XMTB SCAN ENB

;WAIT FOR MOS TO CLEAR

MAINDEC-11-DZDJAD-D
DZDJAD.F11 TST43: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 46

2226								:BIT0 = RECEIVER ENABLE
2228	010012	052777	001000	171174				;SET XMTR CONTROL BIT. LINE 9
2229	010020	017701	171164		LOP43:	MOV #CSR,	ATCR R1	;WAIT FOR XMTR READY
2230	010024	100375				BPL LOP43		
2231	010026	012777	000377	171162		MOV #377,	ATBUF	;SEND A RUBOUT
2232	010034	005000				CLR RO		;CLEAR COUNTER
2233	010036	105305				DEC B R5		;SHORT WAIT LOOP
2234	010040	001376				SNE 1\$		
2235	010042	105777	171142			TSTB #CSR		;WAIT FOR DONE
2236	010046	100405				BMI 2\$;BRANCH WHEN DONE
2237	010050	005200				INC RO		;TIME COUNTER
2238	010052	001371				BNE 1\$;BRANCH IF NOT TIME-OUT
2239	010054	017701	171130			MOV #CSR, R1		;SAVE CSR
2240	010060	104001				HLT+1		;DONE NEVER CAME UP
2241	010062	050037	001302					R1 = CONTENTS OF CSR
2242	010066	017701	171120		2\$:	BIS RO,	TIMER	;SAVE TIMER
2243	010072	100401				MOV #RBUF, R1		;READ THE FI/FO
2244	010074	104001				BMI .+4		;BRANCH IF CHARACTER READY
2245						HLT+1		;CHARACTER READY DIDN'T SET
2246								R1 = CONTENTS OF RBUF
2247	010076	032701	070000		3\$:	BIT #70000, R1		;CHECK FOR ERROR BITS
2248	010102	001401				BEQ .+4		;BRANCH IF NONE
2249	010104	104001				HLT+1		;ERROR IN RECEIVED CHAR
2250								R1 = CONTENTS OF RBUF
2251								;BIT14=UART OVERRUN
2252								;BIT13=FRAMING ERROR
2253								;BIT12=PARITY ERROR
2254	010106	010102			4\$:	MOV R1,	R2	;DUPLICATE DATA WORD
2255	010110	042702	170377			BIC #170377, R2		;MASK LINE#
2256	010114	000302				SWAB R2		;LINE # IN LOW BYTE
2257	010116	122702	000011			CMPB #9., R2		;CHECK LINE #
2258	010122	001401				BEQ .+4		;BRANCH IF OK
2259	010124	104001				HLT+1		;WRONG LINE # RECEIVED
2260								R1 = CONTENTS OF RBUF
2261								;BITS8-11 = LINE #
2262	010126	117702	171154		5\$:	MOV B #DJLEN, R2		;GET MASK OF CHARACTER
2263	010132	130201				BITB R2.	R1	;CHECK CHAR LENGTH.
2264	010134	001401				BEQ .+4		;BRANCH IF OK
2265	010136	104002				HLT+2		;WRONG CHARACTER LENGTH
2266								R1=DATA FROM FI/FO
2267								R2=MASK (BITS SET NOT EXPECTED)
2268	010140	105102			6\$:	COMB R2		;REVERSE THE MASK
2269	010142	120102				CMPB R1,	R2	;CHECK THE ACTURAL DATA
2270	010144	001401				BEQ .+4		;BRANCH IF OK
2271	010146	104002				HLT+2		;WRONG CHAR LEN OR DATA ERROR
2272								R1=DATA FROM FI/FO (COMPLETE WORD)
2273								R2=DATA (LOW BYTE) EXPECTED
2274	010150	017701	171036		7\$:	MOV #RBUF, R1		;READ FI/FO
2275	010154	100001				BPL .+4		;BRANCH IF CHAR PRESENT NOT SET
2276	010156	104001				HLT+1		;CHARACTER PRESENT STAYED SET
2277								R1 = CONTENTS OF RBUF
2278	010160	017701	171024		8\$:	MOV #CSR, R1		;SAVE THE CSR
2279	010164	022701	100405			CMP #100405, R1		;CHECK THE CSR
2280	010170	001401				BEQ .+4		;BRANCH IF OK
2281	010172	104001				HLT+1		;DONE DIDN'T CLEAR OR OTHER CSR ERROR

K04

MAINDEC-11-DZDJ-A-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 47
DZDJ-A-D.F11 TST43: TEST ALL OF LINE 9 TRANSMIT AND RECEIVE LOGIC

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2283 010174 005077 171014           CLR      @TCR      :R1 = CONTENTS OF CSR
2284 010200 005077 171004           CLR      @CSR       ;CLEAR TCR
2285 010204 104400  SCOPE
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MAINDEC-11-DZDJJA-D MACY11 27(732) 21-SEP-76 13:43 PAGE 48
DZDJAD.P11 TST44: TEST ALL OF LINE 10 TRANSMIT AND RECEIVE LOGIC

2338	010310	042702	170377	B1C	#170377,R2	:MASK LINE#
2339	010314	000302		SWAB	R2	:LINE # IN LOW BYTE
2340	010316	122702	000012	CMPB	#10., R2	:CHECK LINE #
2341	010322	001401		BEQ	.+4	:BRANCH IF OK
2342	010324	104001		HLT+1		:WRONG LINE # RECEIVED
2343						:R1 = CONTENTS OF RBUF
2344						:BITS8-11 = LINE #
2345	010326	117702	170754	5\$: MOV	QDJLEN, R2	:GET MASK OF CHARACTER
2346	010332	130201		SITB	R2, R1	:CHECK CHAR LENGTH.
2347	010334	001401		BEQ	.+4	:BRANCH IF OK
2348	010336	104002		HLT+2		:WRONG CHARACTER LENGTH
2349						:R1=DATA FROM FI/FO
2350						:R2=MASK (BITS SET NOT EXPECTED)
2351	010340	105102		6\$: COMB	R2	:REVERSE THE MASK
2352	010342	120102		CMPB	R1,	:CHECK THE ACTURAL DATA
2353	010344	001401		BEQ	.+4	:BRANCH IF OK
2354	010346	104002		HLT+2		:WRONG CHAR LEN OR DATA ERROR
2355						:R1=DATA FROM FI/FO (COMPLETE WORD)
2356						:R2=DATA (LOW BYTE) EXPECTED
2357	010350	017701	170636	7\$: MOV	3RBUF, R1	:READ FI/FO
2358	010354	100001		BPL	.+4	:BRANCH IF CHAR PRESENT NOT SET
2359	010356	104001		HLT+1		:CHARACTER PRESENT STAYED SET
2360						:R1 = CONTENTS OF RBUF
2361	010360	017701	170624	8\$: MOV	3CSR, R1	:SAVE THE CSR
2362	010364	022701	100405	CMP	#100405,R1	:CHECK THE CSR
2363	010370	001401		BEQ	.+4	:BRANCH IF OK
2364	010372	104001		HLT+1		:DONE DIDN'T CLEAR OR OTHER CSR ERROR
2365						:R1 = CONTENTS OF CSR
2366	010374	005077	170614	CLR	3TOR	:CLEAR TCR
2367	010400	005077	170604	CLR	3CSR	:CLEAR CSR
2368	010404	104400		SCOPE		
2369						
2370						*****
2371						:TEST 45: TEST THAT LINE 11 CAN TRANSMIT AND
2372						RECEIVE A CHARACTER. (371)
2373				1\$:	CHECKS THAT DONE SETS IN REASONABLE TIME.	
2374				2\$:	CHECKS THAT CHAR PRESENT IS IN FI/FO	
2375				3\$:	CHECKS THAT NO ERRORS IN FI/FO	
2376				4\$:	CHECKS THAT RIGHT LINE # (11) IN FI/FO	
2377				5\$:	CHECKS FOR RIGHT CHARACTER LENGTH	
2378				6\$:	CHECKS THAT CORRECT DATA WAS RECEIVED	
2379				7\$:	CHECKS THAT CHARACTER PRESENT CLEARS	
2380				8\$:	CHECKS THAT DONE CLEARS	
2381					PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES	
2382					*****	
2383						
2384						
2385						
2386						
2387	010406	004737	015566		INITIALIZE DEVICE "CSR" REGISTER	SET: :BIT2 = MAINTENANCE
2388				TST45: JSR PC, 3#INITD		:BIT3 = CLEAR MOS
2389						:BIT8 = MASTER XMTR SCAN ENB
2390						
2391						SET: :BIT0 = RECEIVER ENABLE
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MAINDEC-11-DZDJ-A-D MACY11 27(732) 21-SEP-76 13:43 PAGE 49
 DZDJAD.P11 TST45: TEST ALL OF LINE 11 TRANSMIT AND RECEIVE LOGIC

2394	010412	052777	004000	170574		BIS	#BIT11, @TCR	SET XMTR CONTROL BIT, LINE 11
2395	010420	017701	170564		LOP45:	MOV	@CSR, R1	:WAIT FOR XMTR READY
2396	010424	100375				BPL	LOP45	
2397	010426	012777	000377	170562		MOV	#377, @TBUF	:SEND A RUBOUT
2398	010434	005000				CLR	R0	:CLEAR COUNTER
2399	010436	105305			1\$:	DECB	R5	:SHORT WAIT LOOP
2400	010440	001376				SNE	1\$	
2401	010442	105777	170542			TSTB	@CSR	:WAIT FOR DONE
2402	010446	100405				BMI	2\$:BRANCH WHEN DONE
2403	010450	005200				INC	R0	:TIME COUNTER
2404	010452	001371				BNE	1\$:BRANCH IF NOT TIME-OUT
2405	010454	017701	170530			MOV	@CSR, R1	:SAVE CSR
2406	010456	104001				HLT+1		:DONE NEVER CAME UP
2407								:R1 = CONTENTS OF CSR
2408	010462	050037	001302		2\$::	BIS	R0, TIMER	:SAVE TIMER
2409	010466	017701	170520			MOV	@RBUF, R1	:READ THE FI/FO
2410	010472	100401				BMI	.+4	:BRANCH IF CHARACTER READY
2411	010474	104001				HLT+1		:CHARACTER READY DIDN'T SET
2412								:R1 = CONTENTS OF RBUF
2413	010476	032701	070000		3\$::	BIT	#70000, R1	:CHECK FOR ERROR BITS
2414	010502	001401				BEQ	.+4	:BRANCH IF NONE
2415	010504	104001				HLT+1		:ERROR IN RECEIVED CHAR
2416								:R1 = CONTENTS OF RBUF
2417								:BIT14=UART OVERRUN
2418								:BIT13=FRAMING ERROR
2419								:BIT12=PARITY ERROR
2420	010506	010102			4\$::	MOV	R1, R2	:DUPLICATE DATA WORD
2421	010510	042702	170377			BIC	#170377, R2	:MASK LINE#
2422	010514	000302				SWAB	R2	:LINE # IN LOW BYTE
2423	010516	122702	000013			CMPB	#11., R2	:CHECK LINE #
2424	010522	001401				BEQ	.+4	:BRANCH IF OK
2425	010524	104001				HLT+1		:WRONG LINE # RECEIVED
2426								:R1 = CONTENTS OF RBUF
2427								:BITS8-11 = LINE #
2428	010526	117702	170554		5\$::	MOV B	@DJLEN, R2	:GET MASK OF CHARACTER
2429	010532	130201				BITB	R2, R1	:CHECK CHAR LENGTH.
2430	010534	001401				BEQ	.+4	:BRANCH IF OK
2431	010536	104002				HLT+2		:WRONG CHARACTER LENGTH
2432								:R1=DATA FROM FI/FO
2433								:R2=MASK (BITS SET NOT EXPECTED)
2434	010540	105102			6\$::	COMB	R2	:REVERSE THE MASK
2435	010542	120102				CMPB	R1, R2	:CHECK THE ACTURAL DATA
2436	010544	001401				BEQ	.+4	:BRANCH IF OK
2437	010546	104002				HLT+2		:WRONG CHAR LEN OR DATA ERROR
2438								:R1=DATA FROM FI/FO (COMPLETE WORD)
2439								:R2=DATA (LOW BYTE) EXPECTED
2440	010550	017701	170436		7\$::	MOV	@RBUF, R1	:READ FI/FO
2441	010554	100001				BPL	.+4	:BRANCH IF CHAR PRESENT NOT SET
2442	010556	104001				HLT+1		:CHARACTER PRESENT STAYED SET
2443								:R1 = CONTENTS OF RBUF
2444	010560	017701	170424		8\$::	MOV	@CSR, R1	:SAVE THE CSR
2445	010564	022701	100405			CMP	#100405, R1	:CHECK THE CSR
2446	010570	001401				BEQ	.+4	:BRANCH IF OK
2447	010572	104001				HLT+1		:DONE DIDN'T CLEAR OR OTHER CSR ERROR
2448								:R1 = CONTENTS OF CSR
2449	010574	005177	170414			CLR	@TCR	:CLEAR TCR

NO4

MAINDEC-11-DZDJAD-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 50
DZDJAD.FII TST45: TEST ALL OF LINE 11 TRANSMIT AND RECEIVE LOGIC

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2450 010600 005077 170404           CLR      @CSR          ;CLEAR CSR
2451 010604 104400
2452 010606 005237 001306           SCOPE    INC      DJLEN
2453 010612 012737 010620 015770   MOV      #.+6,    LAD

***** TEST 46: TEST THAT LINE 12 CAN TRANSMIT AND
***** RECEIVE A CHARACTER. (377)
1$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3$: CHECKS THAT NO ERRORS IN FI/FO
4$: CHECKS THAT RIGHT LINE # (12) IN FI/FO
5$: CHECKS FOR RIGHT CHARACTER LENGTH
6$: CHECKS THAT CORRECT DATA WAS RECEIVED
7$: CHECKS THAT CHARACTER PRESENT CLEARS
8$: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD DC3 SERIES
***** INITIALIZE DEVICE "CSR" REGISTER
:WAIT FOR MOS TO CLEAR
SET:
;BIT2 = MAINTENANCE
;BIT3 = CLEAR MOS
;BITS = MASTER XMTR SCAN ENB
SET:
;BIT0 = RECEIVER ENABLE
:SET XMTR CONTROL BIT, LINE 12
:WAIT FOR XMTR READY
:SEND A RUBOUT
:CLEAR COUNTER
:SHORT WAIT LOOP
:WAIT FOR DONE
:BRANCH WHEN DONE
:TIME COUNTER
:BRANCH IF NOT TIME-OUT
:SAVE CSR
:DONE NEVER CAME UP
:R1 = CONTENTS OF CSR
:SAVE TIMER
:READ THE FI/FO
:BRANCH IF CHARACTER READY
:CHARACTER READY DIDN'T SET
:R1 = CONTENTS OF RBUF
:CHECK FOR ERROR BITS
:BRANCH IF NONE
:ERROR IN RECEIVED CHAR
:R1 = CONTENTS OF RBUF
:BIT14=UART OVERRUN
:BIT13=FRAMING ERROR
:BIT12=PARITY ERROR
:DUPLICATE DATA WORD
:MOV      R1,    R2

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TEST46: 2011 LOGIC TESTS MACYLL 27(732) 21-SEP-76 13:43 PAGE 51

010768	010769	170377		BIC SWP0 CMP0 BEQ HLT+1	#170377, R2 R2 #12.. R2 .44 R1	MASK LINE# LINE # IN LOW BYTE CHECK LINE # BRANCH IF OK WRONG LINE # RECEIVED R1 = CONTENTS OF RBUF BITSS-11 = LINE # GET MASK OF CHARACTER CHECK CHAR LENGTH. BRANCH IF OK WRONG CHARACTER LENGTH R1=DATA FROM FI/FO R2=MASK (BITS SET NOT EXPECTED) REVERSE THE MASK CHECK THE ACTUAL DATA BRANCH IF OK WRONG CHAR LEN OR DATA ERROR R1=DATA FROM FI/FO (COMPLETE WORD) R2=DATA (LOW BYTE) EXPECTED
010769	010770	170378	58:	MOV0 BPL0 HLT+2	SOJLEN, R2 R2,.44 R1	GET MASK OF CHARACTER CHECK CHAR LENGTH. BRANCH IF OK WRONG CHARACTER LENGTH R1=DATA FROM FI/FO R2=MASK (BITS SET NOT EXPECTED)
010770	010771	170379	58:	COM0 CMP0 BEQ0 HLT+2	R2 R1,.44 R2	REVERSE THE MASK CHECK THE ACTUAL DATA BRANCH IF OK WRONG CHAR LEN OR DATA ERROR R1=DATA FROM FI/FO (COMPLETE WORD) R2=DATA (LOW BYTE) EXPECTED
010771	010772	170380	78:	MOV0 BPL0 HLT+1	SRBUF, R1 .44	READ FI/FO BRANCH IF CHAR PRESENT NOT SET CHARACTER PRESENT STAYED SET R1 = CONTENTS OF RBUF
010772	010773	170381	58:	MOV0 CMP0 BEQ0 HLT+1	SOCSR, R1 \$100400,R1 .44	SAVE THE CSR CHECK THE CSR BRANCH IF OK NONE DIDN'T CLEAR OR OTHER CSR ERROR R1 = CONTENTS OF CSR
010773	010774	170382	58:	CLR0 CLR0 SCOPE	BTOR SOCSR	CLEAR TCR CLEAR CSR
010774	010775	170383				
010775	010776	170384				

***** TEST 47: TEST THAT LINE 13 CAN TRANSMIT AND RECEIVE A CHARACTER. (377)
 1: CHECKS THAT DONE SETS IN REASONABLE TIME.
 2: CHECKS THAT CHAR PRESENT IS IN FI/FO
 3: CHECKS THAT NO ERRORS IN FI/FO
 4: CHECKS THAT RIGHT LINE # (13) IN FI/FO
 5: CHECKS FOR RIGHT CHARACTER LENGTH
 6: CHECKS THAT CORRECT DATA WAS RECEIVED
 7: CHECKS THAT CHARACTER PRESENT CLEARS
 8: CHECKS THAT DONE CLEARS
 PROBABLE FAULTY LOGIC: M7295 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

INITIALIZE DEVICE "CSR" REGISTER

011020 004737 015566

TEST47: JSR PC, &INIT0 SET:
 WAIT FOR MOS TO CLEAR
 SET:
 :BIT2 = MAINTENANCE
 :BIT3 = CLEAR MOS
 :BIT8 = MASTER XMTR SCAN ENG
 SET:
 :BIT0 = RECEIVER ENABLE

C05

MACY!! 27(732) 21-SEP-76 13:43 PAGE 52
 2223A-11-2223A-0
 2223A-11-2223A-0
 TST47: TEST ALL OF LINE 13 TRANSMIT AND RECEIVE LOGIC

011024	050037	000000	170162	L0P47:	BIS	\$BIT13, R1	SET XMTR CONTROL BIT, LINE 13
011036	011061	170152			MOV	\$CSR, R1	:WAIT FOR XMTR READY
011036	100377				BPL	L0P47	
011036	012777	000377	170150		MOV	\$377, R1	:SEND A RUBOUT
011036	005000				CLR		:CLEAR COUNTER
011036	105300				DEC8		:SHORT WAIT LOOP
011036	001327		170130		BNE		
011036	106777				TSTB	\$CSR	
011036	100400				SMI		
011036	001371				INC		
011036	012701		170116		BNE		
011036	104001				MOV	\$CSR, R1	
					HLT+1		
011074	050037	001302		18:	BIS	R0, TIMER	
011100	012701	170106			MOV	\$RBUF, R1	
011106	100400				SMI		
011106	104001				HLT+1		
011110	032701	070000		19:	BIT	\$70000, R1	
011110	001400				BEG		
011110	104001				HLT+1		
011120	010100		170377	48:	MOV	R1	
011120	00462700				SWP	\$170377, R0	
011120	000000		000015		CMP	R2	
011120	100400				MOV	\$13.., R2	
011120	104001				HLT+1		
011140	117702	170142		58:	MOV	R0, R2	
011140	000201				SWP	REGLEN, R2	
011140	001400				HLT+2		
011140	104002						
011150	105100			68:	COMB	R2	
011150	00001000				COMB	R1	
011150	101400				BEG		
011150	104002				HLT+2		
011160	017701	170024		78:	MOV	\$RBUF, R1	
011160	100001				SWP		
011160	104001				HLT+1		
011170	017701	170012		88:	MOV	\$CSR, R1	
011170	022701	100405			CMP		
011170	001400				BEG		
011170	104001				HLT+1		
011180	005077	170002			CLR	STOP	

DOS

MSANDER-11-02279-0
TEST LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 53
TEST LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 53

011212 005077 167772
011216 104400

CLR
SCOPE 8CSR :CLEAR CSR

TEST 50: TEST THAT LINE 14 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
16: CHECKS THAT DONE SETS IN REASONABLE TIME.
16: CHECKS THAT CHAR PRESENT IS IN FIFO
46: CHECKS THAT NO ERRORS IN FIFO
46: CHECKS THAT RIGHT LINE # (14) IN FIFO
16: CHECKS FOR RIGHT CHARACTER LENGTH
16: CHECKS THAT CORRECT DATA WAS RECEIVED
16: CHECKS THAT CHARACTER PRESENT CLEARS
16: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7285 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

INITIALIZE
DEVICE "CSR" REGISTER

TST50: JSR PC. S:INIT0 SET:
:SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT8 = MASTER XMTR SCAN ENB

:WAIT FOR MOS TO CLEAR
:SET:
:BIT0 = RECEIVER_ENABLE

011220 004737 015566
052777 040000 167762 LOP50: BIS #BIT14, R10 :SET XMTR CONTROL BIT, LINE 14
017701 167752 MOV 8CSR, R1 :WAIT FOR XMTR READY
100377 000377 167750 BPL LOP50 :
00065000 00065000 MOV #377, R1BUF :SEND A RUBOUT
00116721 00116721 CLR R0 :CLEAR COUNTER
00116722 00116722 DECB R0 :SHORT WAIT LOOP
000400 000400 BNE R0 :
00116723 00116723 TSTB R0 :WAIT FOR DONE
000400 000400 SMI R0 :BRANCH WHEN DONE
000400 000400 INC R0 :TIME COUNTER
00116724 00116724 BNE R0 :BRANCH IF NOT TIME-OUT
00116725 00116725 MOV 8CSR, R1 :SAVE CSR
00116726 00116726 HLT+1 R1 :DONE NEVER CAME UP
00116727 00116727 R1 :R1 = CONTENTS OF CSR
00116728 00116728 BIS R0 :SAVE TIMER
00116729 00116729 MOV R1BUF, R1 :READ THE FIFO
00116730 00116730 BMI .+4 :BRANCH IF CHARACTER READY
00116731 00116731 HLT+1 R1 :CHARACTER READY DIDN'T SET
00116732 00116732 R1 :R1 = CONTENTS OF RBUF
00116733 00116733 BIS R0 :CHECK FOR ERROR BITS
00116734 00116734 BEQ .+4 :BRANCH IF NONE
00116735 00116735 HLT+1 R1 :ERROR IN RECEIVED CHAR
00116736 00116736 R1 :R1 = CONTENTS OF RBUF
00116737 00116737 BIS R0 :BIT14=UART OVERRUN
00116738 00116738 BEQ .+4 :BIT13=FRAMING ERROR
00116739 00116739 HLT+1 R1 :BIT12=PARITY ERROR
00116740 00116740 R1 :DUPLICATE DATA WORD
00116741 00116741 SWAB R1, R2 :MASK LINE#
00116742 00116742 R2 :LINE # IN LOW BYTE

011220 010108 170377
011220 042700 000300
011220 000300

EO5

MAINDEC-11-DZDJIA-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 54
DZDJAD.P11 TST50: TEST ALL OF LINE 14 TRANSMIT AND RECEIVE LOGIC

011334	011330	132702	000016		CMPB	#14..	R2	:CHECK LINE #
011335	011334	001401			BEQ	.+4		:BRANCH IF OK
011336	011335	104001			HLT+1			:WRONG LINE # RECEIVED
011340	011340	117702	167742	5\$:	MOV#	00JLEN.	R2	:R1 = CONTENTS OF RBUF
011344	011340	130201			9ITB	R2,	R1	:BITS8-11 = LINE #
011346	011344	001401			BEQ	.+4		:GET MASK OF CHARACTER
011350	011346	104002			HLT+2			:CHECK CHAR LENGTH.
011352	011350	105100		6\$:	COMB	R2		:BRANCH IF OK
011354	011352	165100			CMPB	R1,	R2	:WRONG CHARACTER LENGTH
011356	011354	001401			BEQ	.+4		:R1=DATA FROM FI/FO
011360	011356	104002			HLT+2			:R2=MASK (BITS SET NOT EXPECTED)
011362	011360	017701	167624	7\$:	MOV	0RBUF,	R1	:REVERSE THE MASK
011364	011362	166001			SPL	.+4		:CHECK THE ACTUAL DATA
011370	011364	104001			HLT+1			:BRANCH IF OK
011372	011370	017701	167612	8\$:	MOV	0CSR,	R1	:WRONG CHAR LEN OR DATA ERROR
011374	011372	002701	100405		CMP	#100405,R1		:R1=DATA FROM FI/FO (COMPLETE WORD)
011404	011374	001401			BEQ	.+4		:R2=DATA (LOW BYTE) EXPECTED
011406	011404	104001			HLT+1			:READ FI/FO
011408	011406	005077	167602		CLR	0T0R		:BRANCH IF CHAR PRESENT NOT SET
011410	011408	005077	167572		CLR	0CSR		:CHARACTER PRESENT STAYED SET
					SCOPE			:R1 = CONTENTS OF RBUF

TEST 51: TEST THAT LINE 15 CAN TRANSMIT AND
RECEIVE A CHARACTER. (377)
1\$: CHECKS THAT DONE SETS IN REASONABLE TIME.
2\$: CHECKS THAT CHAR PRESENT IS IN FI/FO
3\$: CHECKS THAT NO ERRORS IN FI/FO
4\$: CHECKS THAT RIGHT LINE # (15) IN FI/FO
5\$: CHECKS FOR RIGHT CHARACTER LENGTH
6\$: CHECKS THAT CORRECT DATA WAS RECEIVED
7\$: CHECKS THAT CHARACTER PRESENT CLEARS
8\$: CHECKS THAT DONE CLEARS
PROBABLE FAULTY LOGIC: M7295 (D2-7) ALL; M7279 ALL; UART CARD D03 SERIES

INITIALIZE
DEVICE "CSR" REGISTER

011420 004737 015566
TST51: JSR PC, Q:INITD SET:
:BIT2 = MAINTENANCE
:BIT3 = CLEAR MOS
:BIT9 = MASTER XMTR SCAN ENB

:WAIT FOR MOS TO CLEAR
SET:
:BIT0 = RECEIVER ENABLE

011424 052777 100000 167562 LOP51: BIS #BIT15, 0T0R SET XMTR CONTROL BIT, LINE 15
011432 017701 167552 MOV 0CSR, R1 :WAIT FOR XMTR READY

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TEST ALL OF LINE 15 TRANSMIT AND RECEIVE LOGIC

2730	011436	100375		BPL	L0P51			
2731	011440	0:2777	000377 167550	MOV	#377.	ATBUF	:SEND A RUBOUT	
2732	011446	005000		CLR	R0		:CLEAR COUNTER	
2733	011450	105305		DEC8	R5		:SHORT WAIT LOOP	
2734	011452	001376		BNE	16			
2735	011454	105777	167530	TSTB	0CSR		:WAIT FOR DONE	
2736	011460	100405		BMI	28		:BRANCH WHEN DONE	
2737	011462	005200		INC	R0		:TIME COUNTER	
2738	011464	001371		SNE	16		:BRANCH IF NOT TIME-OUT	
2739	011466	017701	167516	MOV	0CSR.	R1	:SAVE CSR	
2740	011472	104001		HLT+1			:DONE NEVER CAME UP	
2741							:R1 = CONTENTS OF CSR	
2742	011474	050037	001302	BIS	R0	TIMER	:SAVE TIMER	
2743	011500	017701	167506	MOV	0RBUF.	R1	:READ THE FI/FO	
2744	011504	100401		BMI	.+4		:BRANCH IF CHARACTER READY	
2745	011506	104001		HLT+1			:CHARACTER READY DIDN'T SET	
2746							:R1 = CONTENTS OF RBUF	
2747	011510	032701	070000	BIT	\$70000.	R1	:CHECK FOR ERROR BITS	
2748	011514	001401		SEQ	.+4		:BRANCH IF NONE	
2749	011516	104001		HLT+1			:ERROR IN RECEIVED CHAR	
2750							:R1 = CONTENTS OF RBUF	
2751							:BIT14=UART OVERRUN	
2752							:BIT13=FRAMING ERROR	
2753							:BIT12=PARITY ERROR	
2754	011520	010102		MOV	R1,	R2	:DUPLICATE DATA WORD	
2755	011522	042702	170377	BIC	\$170377,R2		:MASK LINE#	
2756	011526	000302		SWAB	R2		:LINE # IN LOW BYTE	
2757	011530	122702	000017	CMPB	\$15..	R2	:CHECK LINE #	
2758	011534	001401		BEQ	.+4		:BRANCH IF OK	
2759	011536	104001		HLT+1			:WRONG LINE # RECEIVED	
2760							:R1 = CONTENTS OF RBUF	
2761							:BITS8-11 = LINE #	
2762	011540	117702	167542	5\$:	MOV8	0DJLEN.	R2	:GET MASK OF CHARACTER
2763	011544	130201		BITB	R2,	R1	:CHECK CHAR LENGTH.	
2764	011546	001401		BEQ	.+4		:BRANCH IF OK	
2765	011550	104002		HLT+2			:WRONG CHARACTER LENGTH	
2766							:R1=DATA FROM FI/FO	
2767							:R2=MASK (BITS SET NOT EXPECTED)	
2768	011552	105102		6\$:	COMB	R2		:REVERSE THE MASK
2769	011554	120102		CMPB	R1,	R2	:CHECK THE ACTURAL DATA	
2770	011556	001401		BEQ	.+4		:BRANCH IF OK	
2771	011560	104002		HLT+2			:WRONG CHAR LEN OR DATA ERROR	
2772							:R1=DATA FROM FI/FO (COMPLETE WORD)	
2773							:R2=DATA (LOW BYTE) EXPECTED	
2774	011562	017701	167424	7\$:	MOV	0RBUF.	R1	:READ FI/FO
2775	011566	100001		BPL	.+4		:BRANCH IF CHAR PRESENT NOT SET	
2776	011570	104001		HLT+1			:CHARACTER PRESENT STAYED SET	
2777							:R1 = CONTENTS OF RBUF	
2778	011572	017701	167412	8\$:	MOV	0CSR.	R1	:SAVE THE CSR
2779	011576	022701	100405	CMP	\$100405.R1		:CHECK THE CSR	
2780	011602	001401		BEQ	.+4		:BRANCH IF OK	
2781	011604	104001		HLT+1			:DONE DIDN'T CLEAR OR OTHER CSR ERROR	
2782							:R1 = CONTENTS OF CSR	
2783	011606	005077	167402	CLR	ATCR		:CLEAR TCR	
2784	011612	005077	167372	CLR	0CSR		:CLEAR CSR	
2785	011616	104400		SCOPE				

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2786	011620	162737	000003	001306	SUB	#3,	DJLEN	
2787	011626	005237	001302		INC	TIMER		:WORSE CASE TIME, ONE CHARACTER
2788	011632	013700	001302		MOV	TIMER, R0		:DUP TIMER
2789	011636	006200			ASR	R0		/2
2790	011640	006200			ASR	R0		/4
2791	011642	005200			INC	R0		+1
2792	011644	006137	001302		ROL	TIMER		:TIMER * 2
2793	011650	060037	001302		ADD	R0, TIMER		:2.25 TIMES ONE CHARACTER TIME
2794	011654	012737	011662	015770	MOV	#.46,	LAD	:RESET LOOP ADDRESS

TEST 52: TEST THAT CHARACTER PRESENT (BIT15) OF RBUF
IS CLEARED (BY CLEAR MOS).
PROBABLE FAULTY LOGIC: M7285 (D2-9) E17,E14,E15; M7279; M7280

INITIALIZE

011662	004737	015566		TST52: JSR PC,0\$INITD				
				SET:				
					BIT2 = MAINTENANCE			
					BIT3 = CLEAR MOS			
					BIT8 = TRANS SCAN ENABLE			
					WAIT FOR BIT4 = MOS CLEAR			
				SET:				
011666	012777	000001	167320		BIT0 = RECEIVER ENABLE			
011674	012704	000004			MOV #BIT0, @TCR		:TRANS CONTROL, LINE0	
011700	017701	167304		18:	MOV \$4,R4		:SET UP COUNTER	
011704	100375				MOV \$CSR,R1		:WAIT FOR TRANS READY	
011706	010477	167304			BPL 18			
011708	005304				MOV R4,@TBUF		:TRANSMIT COUNT	
011714	001371				DEC R4		:COUNT DOWN	
011716	105777	167266		28:	BNE 18			
011722	100375				TSTB \$CSR		:MAKE SURE DONE IS SET	
011724	052777	000010	167256		BPL 28			
011732	032777	000020	167250	38:	BIS \$BIT3,\$CSR		:CLEAR MOS	
011740	001374				BIT \$BIT4,\$CSR		:WAIT FOR CLRMOS TO FINISH	
011742	017701	167244			BNE 38			
011746	100001				MOV \$RBUF,R1		:CHECK RBUF AND SAVE	
011750	104001				BPL .+4			
011754	017701	167238			HLT+1			
011756	022701	100406			MOV \$CSR,R1		:SAVE CSR	
011760	001401				CMP \$100406,R1		:CHECK CSR	
011764	104001				BEQ .+4		:BRANCH IF OK	
					HLT+1		:CSR ERROR. POSSIBILITIES:	
							: (1) DONE DIDN'T CLEAR	
							: (2) TRANSMITTER UART DIDN'T CLR.	
							: R1=CONTENTS OF CSR	
011766	013700	001302		48:	MOV TIMER, R0		:SET UP TIMER	
011770	005304				DEC B		:SHORT WAIT LOOP	
011774	001374				BNE 48			

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0200A-D.P11 TST52: TEST LOGIC TESTS

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011706	017701	167206	MOV	\$CSR,R1	:SAVE CSR
012002	105701		TSTB	R1	:CHECK FOR DONE
012004	100001		BPL	.+4	:BRANCH IF OK
012006	104001		HLT+1		:DONE CAME UP!
012010	005300		DEC	R0	:MOS MUST NOT HAVE CLEARED
012012	001367		BNE	4\$:TIMER COUNT
012014	022701	100405	CMP	#100405.R1	:CHECK CSR
012020	001401		BEQ	.+4	:BRANCH IF OK
012022	104001		HLT+1		:CSR ERROR
012024	017701	167162	MOV	\$RBUF.R1	:CHECK RBUF
012030	100001		BPL	.+4	:BRANCH IF OK
012032	104001		HLT+1		:RBUF NOT EMPTY!
012034	005077	167154	CLR	\$TOR	
012040	005077	167144	CLR	\$CSR	
012044	104400		SCOPE		

 TEST 53: TEST THAT TRANSMITTER READY CLEARS WHEN TBUF IS LOADED
 NOTE: DUE TO THE DOUBLE BUFFERING BY THE UART, TWO CHARACTERS
 MUST BE LOADED TO INSURE SEEING TRANSMITTER READY CLEAR
 PROBABLE FAULTY LOGIC: M7285 (D2-6) E39, E23, E49

INITIALIZE DEVICE "CSR" REGISTER								
012046	004737	015556	TST53:	JSR	PC.			
				Q:INIT0	SET: :BIT0 = MAINTENANCE :BIT3 = CLEAR MOS :BIT8 = MASTER XMTR SCAN ENB			
					:WAIT FOR MOS TO CLEAR			
					SET: :BIT0 = RECEIVER ENABLE			
012052	052777	000001	167134	1\$:	BIS	#BIT0,	\$TOR	:TRANS CONTROL, LINE 0
012060	017701	167124			MOV	\$CSR,	R1	:WAIT FOR XMTR READY
012064	100375				BPL	1\$		
012066	012777	000001	167122	2\$:	MOV	\$1,	\$TBUF	:TRANSMIT A 1
012074	017701	167110			MOV	\$CSR,	R1	:WAIT FOR XMTR READY
012100	100375				BPL	2\$		
012102	012777	000002	167106		MOV	\$2,	\$TBUF	:TRANSMIT A 2
012110	017701	167074			MOV	\$CSR,	R1	:CHECK FOR XMTR READY
012114	100001				BPL	.+4		:BRANCH IF XMTR READY CLEARED
012116	104001				HLT+1			:TRANSMITTER READY FAILED TO CLEAR
012120	013700	001302		3\$:	MOV			:R1 = CONTENTS OF CSR
012124	105305				DEC B	TIME,	R0	:SET UP TIMER
012126	001376				BNE	R5		:SHORT WAIT LOOP
012130	017701	167054			MOV	3\$		
012134	000400				BR	\$CSR,	R1	:SAVE CSR FOR THE RECORD
								:NOP FOR TIMING

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TEST TRANSMIT READY

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2998	012136	005300		DEC	R0	:TIMER COUNT
2999	012140	001371		BNE	3\$:BRANCH IF MORE TIME
2900				CMP	#100605.R1	:CHECK CSR
2901	012142	022701	100605	BEQ	.+4	:BRANCH IF OK
2902	012146	001401		HLT+1		:DONE DIDN'T SET OR OTHER CSR ERROR
2903	012150	104001				:R1 = CONTENTS OF CSR
2904				MOV	@RBUF, R1	:CHECK RBUF FOR CHAR PRESENT
2905	012152	017701	167034	SMI	.+4	:BRANCH IF CHAR PRESENT
2906	012156	100401		HLT+1		:CHAR PRESENT MISSING
2907	012160	104001				:R1 = CONTENTS OF RBUF
2908				CMP	#100001.R1	:CHECK THE DATA
2909	012162	022701	100001	BEQ	.+4	:BRANCH IF OK
2910	012166	001401		HLT+1		:RECEIVER ERROR
2911	012170	104001				:R1 = CONTENTS OF RBUF
2912				MOV	@RBUF, R1	:CHECK RBUF FOR SECOND CHAR
2913	012172	017701	167014	SMI	.+4	:BRANCH IF CHAR PRESENT
2914	012176	100401		HLT+1		:CHAR PRESENT MISSING
2915	012200	104001				:R1 = CONTENTS OF RBUF
2916				CMP	#100002.R1	:CHECK THE DATA
2917	012202	022701	100002	BEQ	.+4	:BRANCH IF OK
2918	012206	001401		HLT+1		:RECEIVER ERROR
2919	012210	104001				:R1 = CONTENTS OF RBUF
2920				MOV	@RBUF, R1	:CHECK FOR NO MORE CHARACTERS
2921	012212	017701	166774	BPL	.+4	:BRANCH IF CHAR PRESENT CLEARED
2922	012216	100001		HLT+1		:CHAR PRESENT NOT CLEAR!
2923	012220	104001				:R1 = CONTENTS OF RBUF
2924				MOV	@CSR, R1	:SAVE CSR
2925	012222	017701	166762	CMP	#100405.R1	:CHECK CSR
2926	012226	022701	100405	BEG	.+4	:BRANCH IF OK
2927	012232	001401		HLT+1		:CSR ERROR
2928	012234	104001				:R1 = CONTENTS OF CSR
2929				CLR	@TCR	:CLEAR TCR
2930	012236	005077	166752	CLR	@CSR	:CLEAR CSR
2931	012240	005077	166742	SCOPE		
2932	012246	104400				

TEST 54: TEST THAT RECEIVER ENABLE ON A 0 INHIBITS DONE
AND CHARACTER PRESENT.
PROBABLE FAULTY LOGIC: M7285 (D2-7) E32, E15

941	012250	012777	000414	166732	TST54:	MOV	#414,	@CSR	:BIT2 = MAINTENANCE
942									:BIT3 = CLEAR MOS
943									:BIT8 = MASTER TRAN SCAN ENB
944	012256	032777	000020	166724	10\$:	BIT	#BIT4,	@CSR	:WAIT FOR MOS TO CLEAR
945	012264	001374				BNE	10\$		
946	012266	052777	0000L	166720	1\$:	BIS	#BIT0,	@TCR	:SET XMTR CONTROL BIT. LINE0
947	012274	017701	166710			MOV	@CSR,	R1	:WAIT FOR XMTR READY
948	012300	100375				BPL	1\$		
949	012302	012777	0002E2	166706		MOV	#252,	@TBUF	:SEND AN "
950	012310	013700	001302			MOV	TIMER,	R0	:SET UP TIMER
951	012314	105305			2\$:	DECB	R5		:SHORT WAIT LOOP
952	012316	001376				BNE	2\$		
953	012320	017701	166664			MOV	@CSR,	R1	:SAVE CSR FOR TYPING

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DZDJAD.P11 TST54: TEST RECEIVER ENABLE

2954	012324	105701		TSTB	R1	:CHECK FOR DONE
2955	012326	100002		BPL	3\$:BRANCH IF NOT SET
2956	012330	104001		HLT+1		:DONE SET WHEN RCV ENB CLR
2957						:R1=CONTENTS OF CSR
2958	012332	000402		BR	4\$	
2959	012334	005300	3\$:	DEC	RO	:TIMER COUNT
2960	012336	001366		BNE	2\$:BRANCH IF MORE TIMER
2961						
2962	012340	017701	166646	4\$:	MOV	:CHECK AND SAVE FI/FO
2963	012344	100001		BPL	.+4	:BRANCH IF OK
2964	012346	104001		HLT+1		:CHARACTER PRESENT IN FI/FO
2965						:R1=DATA FROM FI/FO
2966	012350	005277	166634	INC	QCSR	:SET RECEIVER ENABLE
2967	012354	017701	166630	5\$:	MOV	:SAVE CSR
2968	012360	105701		TSTB	R1	:CHECK FOR DONE
2969	012362	100403		BMI	6\$:BRANCH IF OK
2970	012364	105300		DECB	RO	:SHORT TIMER
2971	012366	001372		BNE	5\$	
2972	012370	104001		HLT+1		:DONE DIDN'T COME UP WHEN RECEIVER ENABLED
2973						:UART SHOULD HAVE HELD A CHARACTER
2974						:R1 = CONTENTS OF CSR
2975	012372	017701	166614	6\$:	MOV	:CHECK FOR CHARACTER PRESENT
2976	012376	100401		BMI	.+4	:BRANCH IF OK
2977	012400	104001		HLT+1		:CHARACTER PRESENT MISSING
2978						:R1 = CONTENTS OF RBUF
2979	012402	005077	166606	CLR	ATCR	:CLR TRANS CONTROL REG
2980						
2981	012406	104400		SCOPE		
2982						
2983						*****
2984						:TEST 55: TEST THAT HALF DUPLEX (BIT1) DISABLES THE RECEIVER UARTS.
2985						:PROBABLE FAULTY LOGIC: M7285 (D2-4) E32, E17, E22, (D2-2) E5, E1
2986						*****
2987						
2988	012410	004737	015556	TSTEE: JSR	PC,	Q#INITC :INITIALIZE
2989						:BIT1 = HALF DUPLEX
2990						:BIT2 = MAINTENANCE
2991						:BIT3 = CLEAR MOS
2992						:BIT8 = MASTER TRAN SCAN ENB
2993						:WAIT FOR MOS TO CLEAR
2994						:BIT0 = RECEIVER ENABLE
2995	012414	012777	000001	166572	1\$:	MOV #BIT0, ATCR :SET XMTR CONTROL BIT, LINE0
2996	012422	017701	166562		MOV QCSR, R1	:WAIT FOR XMTR READY
2997	012426	100375		BPL 1\$		
2998	012430	012777	000252	166560	MOV #252, ATBUF	:SEND AN "*"
2999	012436	013700	001302		MOV TIMER, RO	:SET UP TIMER
3000	012442	105305		DECB R5		:SHORT WAIT LOOP
3001	012444	001376		BNE 2\$		
3002	012446	017701	166536	MOV QCSR, R1		:SAVE CSR
3003	012452	105701		TSTB . R1		:CHECK FOR DONE
3004	012454	100002		BPL 3\$:BRANCH IF NOT SET
3005	012456	104001		HLT+1		:DONE SET WHEN HALF DUPLEX (BIT1) SET
3006						:R1=CONTENTS OF CSR
3007	012460	000402		BR 4\$		
3008	012462	005300		DEC RO		:TIMER COUNT
3009	012464	001366		BNE 2\$:BRANCH IF MORE TIMER

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DZDJAD.P11 TST55: DJ11 LOGIC TESTS
TEST HALF DUPLEX

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3010
3011 012466 017701 166520      4$:    MOV    @RBUF, R1      ;CHECK AND SAVE FI/FO
3012 012472 100001                BPL    .+4      ;BRANCH IF OK
3013 012474 104001                HLT+1   ;CHARACTER PRESENT IN FI/FO
3014                                     ;R1=DATA FROM FI/FO
3015 012476 042777 000002 166504    BIC    #BIT1, @CSR    ;CLEAR HALF DUPLEX BIT
3016 012504 000240                NOP
3017 012506 000240                NOP
3018 012510 000240                NOP
3019 012512 000240                NOP
3020 012514 017701 166472      5$:    MOV    @RBUF, R1      ;CHECK FOR CHAR PRESENT
3021 012520 100001                BPL    .+4      ;BRANCH IF CHAR NOT PRESENT
3022 012522 104001                HLT+1   ;CHAR PRESENT AFTER H/D CLEARED
3023                                     ;R1 = CONTENTS OF RBUF
3024 012524 005077 166464      CLR    @TCR      ;CLR TRANS CONTROL REG
3025
3026 012530 104400                SCOPE
3027
3028
3029
3030                                     ;*****TEST 56: TEST THAT RECEIVER INTERRUPT DOES NOT OCCUR AT LEVEL 5*****
3031                                     ;PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
3032                                     ;*****
3033
3034 012532 012777 012620 166460  TST56: MOV    #ISR56, @RCVVEC ;SET UP XMTR INTERRUPT VECTOR
3035 012540 012777 000340 166454    MOV    #340, @RCVLVL  ;AT LEVEL 7
3036 012546 042737 000340 177775    BIC    #340, @#PS    ;CLEAR PS LEVEL
3037 012554 052737 000240 177775    BIS    #240, @#PS    ;SET PS TO LEVEL 5
3038 012562 004737 015546                JSR    PC, @#INITB  ;SET:
3039                                     ;BIT2 = MAINTENANCE
3040                                     ;BIT3 = CLEAR MOS
3041                                     ;BIT6 = RECEIVER INTERRUPT ENABLE
3042                                     ;BIT8 = MASTER TRANS SCAN ENABLE
3043                                     ;WAIT FOR MOS TO CLEAR
3044                                     ;BIT0 = RECEIVER ENABLE
3045 012566 012777 000001 166420    1$:    MOV    #BIT0, @TCR  ;SET TRAN CONTROL BIT, LINE 0
3046 012574 017701 166410                MOV    @CSR, R1      ;WAIT
3047 012600 100375                BPL    1$ 
3048 012602 012777 000025 166406    2$:    MOV    #25, @TBUF   ;SEND #25
3049 012610 105777 166374                TSTB   @CSR
3050 012614 100375                BPL    2$ 
3051 012616 000404                BR    END56      ;OK, BRANCH IF NO INTERRUPT
3052
3053 012620 104000                ISR56: HLT
3054 012622 012716 012630          ISR56: MOV    #END56, (SP) ;SHOULDN'T HAVE INTERRUPTED AT LEVEL 5
3055 012626 000002                RTI
3056
3057 012630 017701 166356          END56: MOV    @RBUF, R1      ;READ THE CHARACTER
3058 012634 100401                BMI    .+4      ;BRANCH IF CHAR PRESENT
3059 012636 104001                HLT+1   ;CHAR PRESENT MISSING
3060                                     ;R1 = CONTENTS OF RBUF
3061 012640 022701 100025          CMP    #100025,R1    ;CHECK THE DATA
3062 012644 001401                BEQ    .+4      ;BRANCH IF OK
3063 012646 104001                HLT+1   ;RECEIVED DATA ERROR
3064                                     ;R1 = CONTENTS OF RBUF
3065 012650 013777 001222 166342    MOV    RCVLVL, @RCVVEC

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DZDJAD.P11 TST56: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 61

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3066 012656 012777 000004 166335      MOV    #IOT, @RCVLVL
3067 012664 005077 166324      CLR    @TCR
3068 012670 005077 166314      CLR    @CSR
3069 012674 042737 000340 177776      BIC    #340, @#PS
3070
3071 012702 104400          SCOPE
3072
3073
3074 :*****TEST 57: TEST THAT RECEIVER INTERRUPT OCCURES AT LEVEL 4*****
3075 :PROBABLE FAULTY LOGIC: M7821 WIRING, PROPER PRIORITY CHIP
3076 :*****TEST 57: TEST THAT RECEIVER INTERRUPT OCCURES AT LEVEL 4*****
3077
3078
3079 012704 012777 012774 166306  TST57: MOV    #ISR57, @RCVVEC ;SET UP XMTR INTERRUPT VECTOR
3080 012712 012777 000340 166302      MOV    #340, @RCVLVL ;AT LEVEL 7
3081 012720 042737 000340 177776      BIC    #340, @#PS ;CLEAR PS LEVEL
3082 012726 052737 000200 177776      BIS    #200, @#PS ;SET PS TO LEVEL 4
3083 012734 004737 015546      JSR    PC, @#INITB ;SET:
3084           ;BIT2 = MAINTENANCE
3085           ;BIT3 = CLEAR MOS
3086           ;BIT6 = RECEIVER INTERRUPT ENABLE
3087           ;BIT8 = MASTER TRANS SCAN ENABLE
3088           ;WAIT FOR MOS TO CLEAR
3089           ;BIT0 = RECEIVER ENABLE
3090 012740 012777 000001 166246      MOV    #BIT0, @TCR ;SET TRAN CONTROL BIT, LINE 0
3091 012746 017701 166236      1$:   MOV    @CSR, R1 ;WAIT
3092 012752 100375
3093 012754 012777 000025 166234      2$:   BPL    1$ ;SEND #25
3094 012762 105777 166222      TSTB   @CSR ;WAIT FOR DONE
3095 012766 100375      BPL    2$ ;SHOULD HAVE INTERRUPTED AT LEVEL 4
3096 012770 104000
3097 012772 000403      BR     END57 ;CONTINUE
3098
3099 012774 012716 013002      ISR57: MOV    #END57, (SP) ;MOVE NEW RTI ADR ONTO STACK
3100 013000 000002
3101
3102 013002 017701 166204      END57: MOV    @RBUF, R1 ;READ THE CHARACTER
3103 013006 100401      BMI    .+4 ;BRANCH IF CHAR PRESENT
3104 013010 104001      HLT    +1 ;CHAR PRESENT MISSING
3105
3106 013012 022701 100025      CMP    #100025,R1 ;R1 = CONTENTS OF RBUF
3107 013016 001401      BEQ    .+4 ;CHECK THE DATA
3108 013020 104001      HLT    +1 ;BRANCH IF OK
3109
3110 013022 013777 001222 166170      MOV    RCVLVL, @RCVVEC ;RECEIVED DATA ERROR
3111 013030 012777 000004 166164      MOV    #IOT, @RCVLVL ;R1 = CONTENTS OF RBUF
3112 013036 005077 166152      CLR    @TCR
3113 013042 005077 166142      CLR    @CSR
3114 013046 042737 000340 177776      BIC    #340, @#PS
3115
3116 013054 104400          SCOPE
3117
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3120
3121 :*****TEST 60: TEST FI/FO OVERRUN*****
3122 :THE FI/FO BUFFER SHOULD HOLD 64 CHARACTERS.

```

MOS

MAINDEC-11-DZDJAD-D
DZDJAD.F11 TST60: DJ11 LOGIC TESTS
TEST FI/FO OVERRUN

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3122 :PROBABLE FAULTY LOGIC: M7285 (D1-7) E32, E17, E22 (D2-2) E5, E1
3123 :*****
3124
3125      INITIALIZE
3126      DEVICE"CSR"REGISTER
3127 013056 004737 015566    TST60: JSR   PC,  @#INITD  SET:
3128          ;BIT2 = MAINTENANCE
3129          ;BIT3 = CLEAR MOS
3130          ;BIT8 = MASTER XMTR SCAN ENB
3131      :WAIT FOR MOS TO CLEAR
3132
3133      SET:
3134          ;BIT0 = RECEIVER ENABLE
3135 013062 012777 177777 166124    1$:    MOV    #177777, @TCR
3136 013070 012700 000100          MOV    #100,   R0
3137 013074 017701 166110          MOV    @CSR,   R1
3138 013100 100375          BPL    1$           ;SAVE AND WAIT FOR TRANS READY
3139 013102 000377 166110          SWAB   @TBUF
3140 013106 032701 020000          BIT    #BIT13, R1
3141 013112 001401          BEQ    .+4           ;CHECK FI/FO OVERRUN
3142 013114 104001          HLT+1
3143
3144 013116 005300          DEC    R0           ;TRANS CONTROL BIT, ALL LINES
3145 013120 001365          BNE    1$           ;SET UP COUNTER - 64. CHAR FI/FO BUFF
3146
3147 013122 013700 001302          2$:    MOV    TIMER,  R0
3148 013126 017701 166056          MOV    @CSR,   R1
3149 013132 100375          BPL    2$           ;WAIT FOR XMTR READY
3150 013134 105305          DECB   R5
3151 013136 001376          BNE    3$           ;SHORT WAIT LOOP
3152 013140 017701 166044          MOV    @CSR,   R1
3153 013144 100401          BMI    .+4           ;SAVE CSR FOR THE RECORD
3154 013146 104001          HLT+1
3155
3156 013150 005300          DEC    R0           ;BRANCH IF TRANS READY
3157 013152 001370          BNE    3$           ;TRANS READY MISTERIOUSLY DISAPPEARED
3158
3159      ;FI/FO SHOULD NOW BE FULL
3160
3161 013154 105701          TSTB   R1           ;R1=CONTENTS OF CSR
3162 013156 100401          BMI    .+4           ;CHECK THAT DONE IS SET
3163 013160 104001          HLT+1
3164
3165 013162 022701 100605          CMP    #100605,R1
3166 013166 001401          BEQ    .+4           ;CHECK THAT FI/FO NOT OVERRUN
3167 013170 104001          HLT+1
3168
3169      ;FI/FO OVERRUN SET
3170      ;OR SOME OTHER CSR ERROR
3171      ;R1=CONTENTS OF CSR
3172
3173      ;*****
3174      ;TEST 60A: TEST THAT FI/FO OVERRUN COMES UP WHEN 65TH CHARACTER
3175      ;IS RECEIVED WITHOUT READING FI/FO
3176      ;*****
3177 013172 000377 166020          T60A:  SWAB   @TBUF
3178 013176 013700 001302          MOV    TIMER, R0
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NOS

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DZDJAD.P11 TST60: DJ11 LOGIC TESTS
TEST FI/FO OVERRUN

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3178	013202	105305		11\$:	DECB	R5	;SHORT WAIT LOOP	
3179	013204	001376			BNE	11\$		
3180	013206	017701	165676		MOV	#CSR, R1	;SAVE CSR	
3181	013212	032701	020000		BIT	#BIT13,R1	;CHECK FI/FO OVERRUN	
3182	013216	001003			BNE	12\$;BRANCH WHEN SET	
3183	013220	005300			DEC	R0	;TIMER	
3184	013222	001367			SNE	11\$;BRANCH IF MORE TIME	
3185	013224	104001			HLT+1		;FI/FO OVERRUN DIDN'T COMEUP	
3186							;R1 = CONTENTS OF CSR	
3187	013226	022701	120605	12\$:	CMP	#120605,R1	;CHECK TOTAL CSR	
3188	013232	001401			BEQ	.+4	;BRANCH IF OK	
3189	013234	104001			HLT+1		;SOMETHING IN CSR FOULED UP	
3190							;R1=CONTENTS OF CSR	
3191								
3192							*****	
3193							TEST 60B: TEST THAT READING THE RECEIVER BUFFER CAUSES FI/FO	
3194							OVERRUN TO CLEAR.	
3195							NOTE: BECAUSE OF TIMING OF THE FI/FO, FI/FO OVERRUN CAN COME	
3196							BACK UP AFTER READING ONE CHARACTER, SO A SECOND MUST	
3197							BE READ TO INSURE THAT FI/FO OVERRUN IS CLEAR.	
3198							*****	
3199								
3200	013236	012700	000002	T60B:	MOV	#2,	SET UP COUNTER - 2 CHARACTERS	
3201	013242	017701	165744	21\$:	MOV	#RBUF, R1	;CHECK AND SAVE FIRST CHAR IN FI/FO	
3202	013246	100401			BMI	.+4	;BRANCH IF CHAR PRESENT	
3203	013250	104001			HLT+1		;CHARACTER PRESENT GONE!	
3204								
3205	013252	032701	070000		BIT	#070000,R1	;CHECK RECEIVER ERRORS	
3206	013256	001401			BEQ	.+4	;BRANCH IF OK	
3207	013260	104001			HLT+1		;RECEIVER ERROR	
3208							;R1=CONTENTS OF RBUF	
3209							;BIT14=UART OVERRUN	
3210							;BIT13=FRAMMING ERROR	
3211							;BIT12=PARITY ERROR	
3212								
3213	013262	010102			MOV	R1.	R2	;PUT LINE # IN R2
3214	013264	000302			SWAB	R2		
3215	013266	042702	177760		BIC	#177750,R2		
3216	013272	120102			CMPB	R1.	R2	;CHECK DATA (=LINE#)
3217	013274	001401			BEQ	.+4	;BRANCH IF OK	
3218	013276	104001			HLT+1		;WRONG DATA RECEIVED	
3219							;R1=FI/FO DATA	
3220							(DATA SHOULD=LINE#)	
3221	013300	005300		22\$:	DEC	R0		
3222	013302	001403			BEQ	24\$		
3223	013304	105305		23\$:	DECB	R5		
3224	013306	001376			BNE	23\$;SHORT WAIT LOOP - GIVE FI/FO TIME	
3225	013310	000754			BR	21\$		
3226							;GO READ ANOTHER	
3227	013312	017701	165672	24\$:	MOV	#CSR, R1		
3228	013316	022701	100605		CMP	#100605,R1		
3229	013322	001401			BEQ	.+4		
3230	013324	104001			HLT+1		;FI/FO OVERRUN DIDN'T CLR	
3231							;OR SOMEOTHER CSR PROBLEM	
3232								
3233								

SEARCHED - INDEXED - SERIALIZED - FILED

ANSWER

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B06

TEST 600:		TEST THAT FI/FO OVERRUN INTERRUPT DOESN'T OCCUR WHEN THE PROCESSOR IS AT LEVEL 5		
T600:	MOV	\$340,	R0	:CLEAR PSW
	MOV	\$340400,	R0	:SET PROCESSOR TO LEVEL 5
	MOV	\$340400, R1	SP	:SET UP RECEIVER INTERRUPT, VEC
	MOV	\$340400, R2	PCVVL	
	BIS	\$340400, R2	CSR	:SET STATUS ENABLE
	MOV	CSR, R1	R0	:SAVE CSR
	CMP	\$110605, R1	R0	:CHECK CSR
	BEQ	.	+	
	BLT+1	.	+	:CSR ERROR
	BLT+2	.	+	:CONTENTS OF CSR
	BLT+3	.	+	:SEND LINE *
	BLT+4	.	+	:WAIT FOR TRANSMITTER READY
308:	MOV	\$340400, R1	R0	
	MOV	\$340400, R1	R0	:SEND LINE *
	MOV	\$340400, R1	R0	:SAVE CSR
	BLT+5	.	+	:WAIT FOR FI/FO OVERRUN
	BLT+6	.	+	:SKIP ISR
328:	MOV	CSR, R1	R0	:SAVE CSR
	BLT+1	.	+	:INTERRUPT OCCURRED AT LEVEL 5
	POP	SPBUF	R0	:“POP” ONE CHARACTER
	MOV	\$340400, R0	SP1	:RESET RETURN ADDRESS
	RTI	.	+	:RETURN
348:	MOV	\$0	R0	:SET UP COUNTER - 2 CHARACTERS
	MOV	SPBUF, R1	R0	:READ ONE CHARACTER
	BLT+1	.	+	:BRANCH IF CHARACTER PRESENT
	BLT+2	.	+	
	BLT+3	\$70000, R1	R0	:CHECK ERRORS
	BLT+4	.	+	
	MOV	R1, R2	R0	:DUP DATA
	SWAP	R0, R1	R0	
	MOV	\$177760, R2	R0	:CLR ALL BUT LINE *
	MOV	\$0, R0	R0	:CHECK DATA
	BLT+5	.	+	
	BLT+6	.	+	
358:	DEC	R0	R0	:COUNT CHARACTERS
	BLT+7	.	+	:BRANCH IF DONE
	BLT+8	.	+	:SHORT WAIT LOOP
	BLT+9	.	+	
	BLT+10	.	+	:GO READ ANOTHER CHARACTER
368:	MOV	CSR, R1	R0	:SAVE CSR
	CMP	\$110605, R1	R0	:CHECK THAT FI/FO OVERRUN CLEARED
	BEQ	.	+	:BRANCH IF OK

MSINDEC-11-020JA-D
020JA-D.PII TSTSD: DIII LOGIC TESTS
TEST FI/FO OVERRUN

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013540	013540	104001		HLT+1			:FI/FO OVERRUN DIDN'T CLR OR SOMETHING CSR PROBLEM RI=CONTENTS OF CSR
***** TEST 600: TEST THAT FI/FO OVERRUN INTERRUPT OCCURS WHEN PROCESSOR IS AT LEVEL 4 *****							

013548	042737	000340	177776	T600:	BIC	#340,	:CLEAR PROCESSOR LEVEL
013550	052737	000200	177776		BIS	#200,	:SET PROCESSOR TO LEVEL 4
013552	012777	012642	165434		MOV	#4268,	:SET UP RECEIVER INTERRUPT VEC
013554	017701	165320			MOV	#0CSR,	:SAVE CSR
013556	022701	110600			CMP	#110605, RI	:CHECK CSR
013558	001701	104001			BEG	.+4	
					HLT+1		
013600	000377	165412		408:	SWBS	#TBUF	:SEND LINE #
013604	005777	165400			SWBS	#05	:WAIT FOR TRANSMITTER READY
013610	100376				SWBS	#05	
013612	000377	165400		418:	SWBS	#TBUF	:SEND LINE #
013616	017701	165366			MOV	#0CSR,	:SAVE CSR
013620	032701	020000			BEG	#BIT3, RI	:WAIT FOR FI/FO OVERRUN
013626	001779				HLT+1		
013630	104001						:INTERRUPT DIDN'T OCCURE WHEN OVERRUN SET
013632	052777	000010	165350		BIS	#BIT3, SOSR	:RI = CONTENTS OF CSR
013640	000464				SWBS	#55	:CLEAR MOS
							:SKIP TO THE END
013642	017701	165342		428:	MOV	#0CSR,	:SAVE CSR
013646	022701	160605			CMP	#130605, RI	:CHECK CSR
013650	001401				BEG	.+4	:BRANCH IF OK
013654	104001				HLT+1		:CSR ERROR
013656	012700	000101		438:	MOV	#101,	:RI = CONTENTS OF CSR
013658	017701	165324			SWBS	#RBUF, RI	:SET UP COUNTER - 65 CHARACTERS
013660	100401				BMI	.+4	:READ ONE CHARACTER
013670	104001				HLT+1		:BRANCH IF CHARACTER PRESENT
013672	032701	070000			BIT	#70000, RI	:CHECK ERRORS
013676	001401				BEG	.+4	
013700	104001				HLT+1		
013702	010102				MOV	RI, R2	:DUP DATA
013704	000309				SWBS	R2	
013706	042702	177760			SIC	#177760, R2	:CLR ALL BUT LINE #
013712	120102				CMPB	RI, R2	:CHECK DATA
013714	001401				BEG	.+4	
013716	104001				HLT+1		
013720	017701	165264			MOV	#0CSR, RI	:SAVE CSR
013724	005200				DEC	R0	
013726	001710				BEG	#448	
013728	032700	000100			CMP	#100, R0	:CHECK FOR FIRST CHAR READ
013732	001752				BEG	#438	:SKIP CSR CHECK ON FIRST CHAR
013736	022701	110605			CMP	#110605, RI	:CHECK CSR

D06

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 TST60: TEST FIFO OVERRUN

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013742	001401		BEQ	.+4		
013744	104001		HLT+1			
013746	000745		BR	43\$		
013750	022701	110405	44\$:	CMP	#110405,R1	:CHECK CSR
013754	001401		BEQ	.+4		:BRANCH IF OK
013756	104001		HLT+1			:DONE DIDN'T GO AWAY
						:OR OTHER CSR ERROR
013760	012701	165226		MOV	\$RBUF, R1	:READ A CHARACTER
013764	100001			\$PL	.+4	:BRANCH IF NO CHAR. PRES
013766	104001			HLT+1		:CHAR. PRESENT!
013770	013777	001222	165222	MOV	\$RVLVL, \$RCVVEC	
013776	012777	000004	165216	MOV	\$IOT, \$RCVVL	
014004	0012716	014012		MOV	\$45\$, (SP)	:RESET RETURN ADDRESS ON STACK
014010	0000008			BT		:RESTORE PSW
014014	005072	165176	45\$:	CLR	\$TCSR	
014018	005072	165166		CLR	\$OSR	
014022	042737	000340	177776	BIC	#340, \$APS	:LOWER PROCESSOR STATUS
014030	104400			SCOPE		

 :TEST 61: TEST THAT UART OVERRUN IS DETECTED ON ALL LINES
 :PROBABLE FAULTY LOGIC: M7295 (D2-2) E3, E1; M7279: M7280

014032	012777	000414	165150	TST61:	MOV	#414, \$CSR	:BIT2 = MAINTENANCE
014040	032777	000020	165142	10\$:	BIT	#BIT4, \$CSR	:BIT3 = CLEAR MOS
001374	006001				BNE	10\$:BIT8 = TRANS SCAN ENABLE
012777	000001	165134			CLR	R1	:WAIT FOR MOS TO CLEAR
017702	165124			LOP61:	MOV	\$1, \$CSR	:SET UP LINE COUNTER
100376					BPL	LOP61	:TRANS CONTROL LINE 0
012777	000001	165122			MOV	\$1,	:WAIT FOR TRANS READY
017702	165110			2\$:	BPL	\$CSR, R2	:SEND \$1
100375					MOV		:WAIT FOR TRANS READY
012777	000002	165106			BPL		:SEND \$2
013700	001302			3\$:	MOV	#2, TIMER, R0	:SET UP TIMER
105305					DEC	R5	:SHORT TIME LOOP
001376					BNE	3\$	
017702	165064				MOV	\$CSR, R2	:SAVE CSR FOR THE RECORD
000400					BR	.+2	:NOP FOR TIMING
005300					DEC	R0	:TIMER COUNT
001371					BNE	3\$	
005277	165052				INC	\$CSR	:SET RECEIVER ENABLE
017702	165046				MOV	\$CSR	:SAVE CSR
032702	000001				BIT	#BIT0, R2	:CHECK RECEIVER ENABLE
0014149					BNE	.+4	:BRANCH IF OK
014150	104002				HLT+2		:RECEIVER ENABLE FAILED TO SET

R1 = LINE #

E06

MAINDEC-11-D2DJA-0 DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 67
D2DJA.D.PII TST61: TEST RECEIVER UART OVERRUN ON ALL LINES

MAINDE0-11-D2DJA-D
D2DJAD.P11 TST62: DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 68

3458	014312	017701	164676	MOV	#BCSR, R1	:CHECK AND SAVE BCSR
3459	014316	022701	177777	CMP	#177777,R1	:CHECK THAT ALL THE BITS ARE SET
3460	014320	001401		BEQ	.+4	:BRANCH IF OK
3461	014324	104001		HLT+1		:BIT(S) OF BCSR FAILED TO SET
3462						
3463	014326	005077	164662	CLR	#BCSR	:CLEAR BCSR
3464	014332	017701	164556	MOV	#BCSR, R1	:CHECK THAT IT CLEARED AND SAVE
3465	014336	001401		BEQ	.+4	:BRANCH IF CLR
3466	014340	104001		HLT+1		:BIT(S) OF BCSR FAILED TO CLEAR
3467						
3468	014342	104400				SCOPE

 :TEST 63: TEST THAT LINE0 CAN TRANSMIT AND RECEIVE A BREAK
 ALSO CHECKS FRAMING ERROR(RBUF BIT13)
 ALSO CHECKS PARITY ERROR(RBUF BIT12)
 IF ODD PARITY IS SELECTED
 PROBABLE FAULTY LOGIC: M7285 (D2-2) E5, E1, (D2-3) E16, E2, E19, E35

3470	014344	004737	015536	TST63:	JSR	PC,	#INITA	:INITIALIZE
3471								:BIT2 = MAINTENANCE
3472								:BIT3 = CLEAR MOS
3473								:BIT10= R/W BCSR
3474								:WAIT FOR MOS TO CLEAR
3475								:BIT0 = RECEIVER ENABLE
3476								:SEND BREAKS, LINE 0
3477								:SET UP TIMER
3478								:SHORT WAIT LOOP
3479								
3480	014350	012777	000001	164636	1\$:	MOV	\$1, #CSR	
3481	014356	013700	001302			MOV	TIMER, R0	:SET UP TIMER
3482	014362	105305				DEC#	R5	
3483	014364	001376				BNE	1\$:SHORT WAIT LOOP
3484	014366	017701	164616			MOV	#CSR, R1	:SAVE CSR
3485	014372	105701				TSTB	R1	:CHECK FOR DONE
3486	014374	100404				BMI	2\$:BRANCH WHEN DONE
3487	014376	005200				INC	R0	:WAIT A WHILE
3488	014400	001370				BNE	1\$	
3489	014402	104001				HLT+1		:DONE NEVER CAME UP
3490	014404	000430			2\$:	BR	4\$:R1=CONTENTS OF CSR
3491	014406	022701	002205			CMP	#2205, R1	:CHECK REST OF CSR
3492	014412	001401				BEQ	.+4	:BRANCH IF OK
3493	014414	104001				HLT+1		:CSR ERROR
3494								:R1=CONTENTS OF CSR
3495								
3496	014416	017701	164570			MOV	#RBUF, R1	:GET DATA FROM FIFO
3497	014422	100401				BMI	.+4	:BRANCH IF OK
3498	014424	104001				HLT+1		:CHARACTER PRESENT NOT UP
3499								:R1=CONTENTS OF RBUF
3500								
3501	014426	032701	020000			BIT	*020000,R1	:CHECK FOR FRAMING ERROR
3502	014432	001001				BNE	.+4	:BRANCH IF OK
3503	014434	104001				HLT+1		:FRAMING ERROR NOT UP
3504								:R1=CONTENTS OF RBUF
3505								
3506	014436	133737	001310	001276		BITB	DJPAR, PARITY	:CHECK ODD PARITY FLAG
3507	014444	001404				BEQ	3\$:BRANCH IF NOT
3508	014446	032701	010000			BIT	*010000,R1	:CHECK PARITY ERROR
3509	014452	001005				BNE	4\$	

MAINDEC-11-D2DJA-D
D2DJA.D.FII TST63: DJ11 LOGIC TESTS
TEST BREAKS ON LINE 0

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3514	014454	104001		HLT+1		:ODD PARITY SHOULD CAUSE PARITY ERROR :R1=CONTENTS OF RBUF
3515	014456	032701	010000	3\$: BIT BEQ .+4	#010000,R1	:CHECK PARITY ERROR
3516	014462	001401		HLT+1		:BRANCH IF OK
3517	014464	104001				:EVEN PARITY OR NO PARITY
3518	014466	032701	040000	4\$: BIT BEQ .+4	#040000,R1	:SHOULDN'T CAUSE PARITY ERROR
3519	014472	001401		HLT+1		:R1=CONTENTS OF RBUF
3520	014474	104001				:CHECK UART OVERRUN
3521	014476	032701	007400	BIT BEQ .+4	#007400,R1	:BRANCH IF OK
3522	014502	001401		HLT+1		:UART OVERRUN SET!!
3523	014504	104001				:R1=CONTENTS OF RBUF
3524	014506	105701		TSTB BEQ .+4	R1	:CHECK LINE #
3525	014510	001401		HLT+1		:BRANCH IF OK
3526	014510	104001				:WRONG LINE# IN FIFO
3527	014514	017701	164472	MOV BPL .+4	RBUF, R1	:R1=CONTENTS OF RBUF
3528	014520	100001		HLT+1		:CHECK DATA
3529	014522	104001				:BRANCH IF OK
3530	014524	005077	164464	5\$: CLR DECB	BBCSR	:WRONG DATA RECEIVED
3531	014530	105305		BNE SS		:R1=CONTENTS OF RBUF
3532	014532	001376				:READ FIFO AGAIN
3533	014534	104400		SCOPE		:BRANCH IF OK

```
*****
:TEST 64: TEST THAT EACH LINE CAN TRANSMIT AND RECEIVE A BREAK
:ALSO CHECKS FRAMING ERROR(RBUF BIT13)
:ALSO CHECKS PARITY ERROR(RBUF BIT12)
:IF ODD PARITY IS SELECTED
:PROBABLE FAULTY LOGIC: M7295 (D2-2) E5, E1, (D2-3) E16, E2, E19, E36
*****
```

014536	004737	015536	TST64: JSR PC, SWINITA	INITIALIZE	
014542	005001			:BIT2 = MAINTENANCE	
014544	012704	000001		:BIT3 = CLEAR MOS	
014550	013700	001302		:BIT10 = R/W BCSR	
014554	050477	164434	LOP64: CLR R1	:WAIT FOR MOS TO CLEAR	
014560	105305		MOV \$:BIT0 = RECEIVER ENABLE	
014562	001376		DIS R4,	:SET UP LINE COUNTER	
014564	017702	164420	DECB R0	:SET UP LINE MARKER	
014570	105702		BNE 16	:SET UP TIMER	
014572	100404		MOV BCSR, R2	:SET BREAK CONTROL BIT, LINE # IN R1	
014574	005200		TSTB R2	:SHORT WAIT LOOP	
			BMI R2		
			INC R0		
				:SAVE CSR	
				:CHECK FOR DONE	
				:BRANCH WHEN DONE	
				:WAIT A WHILE	

H06

MAINDEC-11-D2DJA-D
D2DJA0.F11 TST64: D111 LOGIC TESTS
TEST BREAKS ON ALL LINES MACY11 27(732) 21-SEP-76 13:43 PAGE 70

3570	014576	001370		BNE	18		
	014600	104002		HLT+2			:DONE NEVER CAME UP
	014602	000433					:R1 = LINE #
	014604	022702	002205	28:	BR	48	:R2 = CONTENTS OF CSR
	014610	001401		CMP	#2205, R2		:CHECK REST OF CSR
	014612	104002		BEG	.+4		:BRANCH IF OK
				HLT+2			:CSR ERROR
							:R1 = LINE #
							:R2 = CONTENTS OF CSR
	014614	017702	164372	MOV	RBUF, R2		:GET DATA FROM FI/FO
	014616	100401		BR	.+4		:BRANCH IF OK
	014622	104002		HLT+2			:CHARACTER PRESENT NOT UP
							:R1 = LINE #
							:R2 = CONTENTS OF RBUF
	014624	032702	0E0000	BIT	#020000,R2		:CHECK FOR FRAMING ERROR
	014626	001001		BEG	.+4		:BRANCH IF OK
	014632	104002		HLT+2			:FRAMING ERROR NOT UP
							:R1 = LINE #
							:R2 = CONTENTS OF RBUF
	014634	010103		MOV	R1, R3		:GET LINE #
	014636	006203		BR	R3		:/4
	014640	006203		MOV	R1, R3		
	014642	133763	001310 001276	WTR	DJPAR,PARITY(3)		:CHECK ODD PARITY FLAG
	014644	001404		MOV	R3		:BRANCH IF NOT
	014646	032702	010000	MOV	#010000,R2		:CHECK PARITY ERROR
	014650	001005		HLT+2	48		:ODD PARITY SHOULD CAUSE PARITY ERROR
	014652	104002					:R1 = LINE #
							:R2 = CONTENTS OF RBUF
	014662	032702	010000	38:	BIT	#010000,R2	:CHECK PARITY ERROR
	014666	001401		BEG	48		:BRANCH IF OK
	014670	104002		HLT+2			:EVEN PARITY OR NO PARITY
							:SHOULDN'T CAUSE PARITY ERROR
							:R1 = LINE #
							:R2 = CONTENTS OF RBUF
	014672	032702	040000	48:	BIT	#040000,R2	:CHECK UART OVERRUN
	014676	001401		BEG	.+4		:BRANCH IF OK
	014700	104002		HLT+2			:UART OVERRUN SET!!
							:R1 = LINE #
							:R2 = CONTENTS OF RBUF
	014702	010203		MOV	R2, R3		:DUP DATA
	014704	000303		SWAB	R3		:LINE # IN LOW BYTE
	014706	042703	177760	BIC	#177760,R3		:MASK ALL BUT LINE #
	014712	020103		CMP	R1, R3		:CHECK FOR RIGHT LINE #
	014714	001401		BEG	.+4		:BRANCH IF OK
	014716	104002		HLT+2			:WRONG LINE# IN FI/FO
							:R1 = LINE #
							:R2 = CONTENTS OF RBUF
	014720	105702		TSTB	R2		:CHECK DATA

MAINDEC-11-DZDJAD-D MACY11 27(732) 21-SEP-76 13:43 PAGE 71
DZDJAD.F11 TST64: DJ11 LOGIC TESTS TEST BREAKS ON ALL LINES

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3626 014722 001401      BEQ    .+4      ;BRANCH IF OK
3627 014724 104002      HLT+2
3628
3629
3630 014726 017702 164260      MOV    @RBUF, R2      ;WRONG DATA RECEIVED
3631 014732 100001      BPL    .+4      ;R1 = LINE #
3632 014734 104002      HLT+2      ;R2 = CONTENTS OF RBUF
3633
3634
3635 014736 005077 164252      CLR    @BCSR      ;READ FI/FO AGAIN
3636 014742 005201      INC    R1      ;BRANCH IF OK
3637 014744 006304      ASL    R4      ;EXTRA CHAR IN FI/FO
3638 014746 103300      BCC    LOP64      ;R1 = LINE #
3639
3640 014750 005077 164234      CLR    @CSR      ;R2 = CONTENTS OF RBUF
3641 014754 104400      SCOPE
3642
3643 014756 012737 000002 015772      MOV    #2, TIMES
3644
3645 :*****TEST 65: TEST THAT RESET CLEARS ALL BUFFERS*****
3646 :NOTE: THE FI/FO BUFFER IS NOT COMPLETELY CLEARED
3647 :BY RESET; ONLY CHARACTER PRESENT IS CLEARED.
3648 :PROBABLE FAULTY LOGIC: M7285 (D2-8) E13
3649 :*****
3650
3651 014764 052737 000340 177776      TST65: BIS    #340,@PS      ;SET PROCESSOR TO LEVEL 7
3652 014772 012777 177777 164214      MOV    #177777,@TCR      ;SET ALL TCR BITS
3653 015000 012777 052507 164202      MOV    #052507,@CSR      ;SET ALL R/W BITS OF CSR
3654 015006 012777 177777 164200      MOV    #177777,@BCSR      ;SET ALL BREAK CONTROL BITS (SEND BREAKS)
3655
3656 :NOTE: ALL LINES SHOULD BE SENDING BREAKS, BUT NONE SHOULD BE RECEIVING
3657 :BECAUSE THE HALF DUPLEX BIT IS SET
3658 015014 012777 177777 164174      MOV    #177777,@TBUF      ;LOADING TRANS BUFF WHEN BREAK BIT SET
3659
3660 015022 000005
3661 015024 013737 001210 015034      RESET
3662 015032 013701      MOV    CSR,1$      ;CLEAR THE WORLD
3663 015034 000000      MOV    @((PC)+,R1)      ;CHECK CSR AND SAVE
3664 015036 001401      1$:      000000
3665 015040 104001      BEQ    .+4
3666
3667 015042 017701 164146      HLT+1
3668 015046 001401      MOV    @TCR,R1      ;CHECK TCR AND SAVE
3669 015050 104001      BEQ    .+4
3670
3671 015052 017701 164136      HLT+1
3672 015056 001401      MOV    @BCSR,R1      ;CHECK BCSR AND SAVE
3673 015060 104001      BEQ    .+4
3674
3675 015062 017701 164124      HLT+1
3676 015066 100001      MOV    @RBUF,R1      ;CHECK RBUF AND SAVE
3677 015070 104001      BPL    .+4
3678
3679 015072 017701 164120      HLT+1
3680 015076 001401      MOV    @TBUF,R1      ;CHECK TBUF AND SAVE
3681 015100 104001      BEQ    .+4

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J06

MAINDEC-11-DZDJAD-D DJ11 LOGIC TESTS
DZDJAD.PII TST65: TEST RESET

MACY11 27(732) 21-SEP-76 13:43 PAGE 72

3692
3693 015102 104400

SCOPE

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3686 ;***** TEST 66: SEND A BINARY COUNT PATTERN ON EACH LINE *****
3687 ;PROBABLE FAULTY LOGIC: COULD BE ALMOST ANYWHERE!
3688 ;*****
3689
3690
3691 015104 005001
3692 015106 012703 100000 TST66: CLR R1 :SET UP LINE COUNTER
3693 015112 005004 MOV #100000,R3 :SET UP RCV DATA
3694 015114 042737 000340 177776 CLR R4 :SET UP TRANS DATA
3695 015122 052737 000200 177775 BIC #340, @#PS :CLEAR PROCESSOR PRIORITY
3696 015130 012700 000001 MOV #200, @#PS :SET PRIORITY TO 4
3697 015134 012777 000010 164046 MOV #1, R0 :SET UP LINE MARKER
3698 015142 012777 010505 164040 MOV #10, @CSR :CLEAR MOS
3699
3700
3701
3702
3703 015150 032777 000020 164032 10$: BIT #BIT4, @CSR :WAIT FOR MOS TO CLEAR
3704 015156 001374 BNE 10$ :
3705 015160 012777 015274 164032 MOV #ISR66,@RCVVEC :SET UP RECEIVER INTERRUPT VECTOR
3706 015166 012777 000240 164026 MOV #240, @RCVLVL :
3707 015174 010077 164014 1$: MOV R0, @TOR :TRANS CONTROL, ONE LINE AT A TIME
3708 015200 005777 164004 2$: TST @CSR :WAIT FOR TRANS READY
3709 015204 100375 BPL 2$ :
3710 015206 010477 164004 MOV R4, @TBUF :SEND DATA
3711 015212 105204 INC B :BINARY COUNT
3712 015214 001371 BNE 2$ :
3713 015216 105703 3$: TSTB R3 :WAIT FOR RECEIVER DONE
3714 015220 001376 BNE 3$ :
3715 015222 017702 163762 MOV @CSR, R2 :SAVE CSR
3716 015226 022702 110505 CMP #110505,R2 :CHECK CSR
3717 015232 001401 BEQ .+4 :BRANCH IF OK
3718 015234 104002 HLT+2 :CSR ERROR
3719
3720
3721 015236 017702 163750 MOV @RBUF, R2 :R1=LINE #
3722 015242 100001 BPL .+4 :R2=CONTENTS OF CSR
3723 015244 104002 HLT+2 :CHECK CHARACTER PRESENT
3724 :BRANCH IF OK
3725 :CHARACTER PRESENT SET!!
3726 015246 062703 000400 ADD #400, R3 :R1=LINE #
3727 015252 005201 INC R1 :UPDATE LINE #
3728 015254 032701 000003 BIT #3, R1 :CHECK FOR FOURTH LINE
3729 015260 001002 BNE 4$ :BRANCH IF NOT
3730 015262 005237 001306 INC DJLEN :MOVE CHARACTER LENGTH POINTER
3731 015266 006300 4$: ASL R0 :UPDATE LINE MARKER
3732 015270 103341 BCC 1$ :BRANCH IF MORE
3733 015272 000417 BR ENDF6 :SKIP ISR
3734
3735 015274 017702 163712 ISR66: MOV @RBUF, R2 :READ FIRST DATA
3736 015300 100401 BMI 11$ :BRANCH IF CHARACTER PRESENT
3737 015302 104003 HLT+3 :INTERRUPT BUT NO CHAR PRESENT

```

K06

MAINDEC-11-DZDJIA-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 73
DZDJIA.D.PII TST66: TEST ALL DATA ON EACH LINE

MAINDEC-11-DZDJAD-D
DZDJAD.FIIDJ11 LOGIC TESTS
BELL AND SCOPE ROUTINE

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```

3794 015532 000000 .TBIT: 0 ;T BIT FLAG
3795
3796 015534 000002 YESRT: RTI ;RETURN FROM TRACE TRAP
3797
3798
3799
3800
3801
3802
3803
3804
3805
3806
3807
3808
3809
3810
3811
3812
3813
3814
3815
3816
3817 015536 012777 002014 163444 INITA: MOV #2014, @CSR SET ;BIT(S)2,3,10 THEN 0
3818 015544 000413 BR INITR
3819
3820 015546 012777 000514 163434 INITB: MOV #514, @CSR ;BIT(S)2,3,6,8 THEN 0
3821 015554 000407 BR INITR
3822
3823 015556 012777 000416 163424 INITC: MOV #416, @CSR ;BIT(S)1,2,3,9 THEN 0
3824 015564 000403 BR INITR
3825
3826 015566 012777 000414 163414 INITD: MOV #414, @CSR ;BIT(S)2,3,8 THEN 0
3827
3828 015574 005000 INITR: CLR R0
3829
3830 015576 005200 1$: INC R0 ;ANTIHANG
3831 015600 001004 BNE 2$ ;ROUTINE
3832
3833 015602 011600 MOV (SP), R0 ;RECORD SUBROUTINE CALL RETURN
3834 015604 162700 SUB #2, R0 ;FORM CALL ADDRESS FOR DISPLAY
3835
3836 015610 104000 HLT ;BIT#4 OF DEVICE CSR FAILED TO CLEAR
3837
3838 015612 032777 000020 163370 2$: BIT #BIT4, @CSR ;TEST HAS MOS CLEARED
3839 015620 001366 BNE 1$ ;NO BRANCHES
3840
3841 015622 052777 000001 163360 BIS #1, @CSR ;SET: BIT00 RECEIVE ENABLE
3842 015630 000207 RTS PC ;CONTINUE
3843
3844
3845 : $SCOPE SCOPE LOOP HANDLER
3846
3847 : THIS ROUTINE HANDLES THE ITERATIONS, LOOPING, ERROR
3848 : LOOPING, AND THE DISPLAYING OF THE TEST NUMBER.
3849

```

3850 ;"SCOPE" IS PLACED BETWEEN EACH SUBTEST IN THE TEST AND
 3851 ;RECORDS THE STARTING ADDRESS OF THE SUBTEST IN "LAD:"
 3852
 3853 015632 004737 017640 TRAPS: JSR PC, KBDINT
 3854 015636 032777 000400 163452 BIT #SW8,DSWR
 3855 015644 001404 BEQ 1\$
 3856 015646 127737 163444 001200 CMPB DSWR,ICNT
 3857 015654 001434 BEQ OVER\$
 3858 015656 032777 040000 163432 1\$: BIT #SW14,DSWR
 3859 015664 001026 BNE KITS
 3860 015666 032777 004000 163422 BIT #SW11,DSWR
 3861 015674 001012 BNE SVLADS\$
 3862 015676 105737 001201 TSTB ICNT+1
 3863 015702 001404 BEQ 2\$
 3864 015704 123737 015772 001201 CMPB TIMES,ICNT+1
 3865 015712 001013 BNE KITS
 3866 015714 112737 000001 001201 2\$: MOVB #1,ICNT+1
 3867 015722 105237 001200 SVLADS\$: INCB ICNT
 3868 015726 011637 015770 MOV (6),LAD
 3869 015732 013737 001200 001320 MOV ICNT,0#DISPLAY
 3870 015740 000002 RTI
 3871
 3872 015742 105237 001201 KITS: INCB ICNT+1
 3873 015746 013737 001200 OVER\$: MOV ICNT,0#DISPLAY
 3874 015754 105737 015770 TST LAD
 3875 015760 001760 BEQ SVLADS\$
 3876 015762 013716 015770 MOV LAD,(6)
 3877 015766 000002 RTI
 3878
 3879 015770 000000 LAD: 0
 3880 015772 000020 TIMES: 20
 ;LOOP ON SPEC. TEST?
 ;NO LOOP ON SPEC. TEST
 ;ON RIGHT TEST? *SW7-0*
 ;NOT RIGHT TEST
 ;LOOP ON TEST?
 ;LOOP ON TEST IS SET
 ;KILL ITERATIONS
 ;YES - KILL ITERATIONS
 ;FIRST ONE?
 ;BRANCH IF FIRST
 ;DONE?
 ;BRANCH IF NOT
 ;FIRST ITERATION
 ;COUNT TEST NUMBERS
 ;SAVE LOOP ADDRESS
 ;DISPLAY TEST NO. AND ITERATION COUNT
 ;RETURN
 ;INC THE ITERATION COUNT
 ;SET UP DISPLAY
 ;FIRST ONE?
 ;YES
 ;FUDGE RETURN ADDRESS
 ;FIXES PS
 ;LOOP ADDRESS
 ;RUN 20 TIMES

3891 ; ; \$HLT ERROR TYPEOUT HANDLER

3892 ; ; THIS ROUTINE PRINTS OUT ERROR MESSAGES STARTING WITH THE

3893 ; ; ADDRESS OF THE "HLT". IT ALSO COUNTS THE NUMBER OF ERRORS

3894 ; ; AND HAS THE CAPABILITY OF LOOPING ON ERROR, BELL ON ERROR,

3895 ; ; "HALT" ON ERROR, AND INHIBIT TYPEOUTS. AN OPTIONAL ARGUMENT

3896 ; ; (HLTCT\$) WILL BE PLACED IN "HLTCT\$:" FOR ADDITIONAL TYPEOUTS.

3897 ; ;

3898 ; ;

3899 ; ;

3900 015774 004737 017640 EMT\$: JSR PC, KBDINT

3901 016000 032777 002000 163310 BIT #SW10,0\$WR ;BELL ON ERROR?

3902 016006 001402 BEQ 1\$;NO - SKIP

3903 016010 000004 000007 TYPE BELL ;RING BELL

3904 016014 005237 001202 1\$: INC ERRORS ;COUNT THE NUMBER OF ERRORS

3905 016020 032777 020000 163270 BIT #SW13,0\$WR ;SKIP TYPEOUT IF SET

3906 016026 001026 BNE 2\$;SKIP TYPEOUTS

3907 016030 000004 016034 TYPE .+2 ;.ASCIZ <15><12>

3908 016040 011637 016144 MOV (6),HLTADR ;PUT ADDRESS OF INSTRUCTION ON STACK

3909 016044 162737 000002 016144 SUB #2,HLTADR ;FUDGE ADDRESS

3910 016052 117737 000066 016142 MOVB #HLTADR,HLTCT\$;GET HLT ARGUMENT

3911 016060 013705 016144 MOV HLTADR,TTY ;TYPE HLTADR IN OCTAL

3912 016064 004737 016562 JSR PC,PRINTR ;TYPE LEADING ZERO'S

3913 016070 000004 016074 TYPE .+2 ;.ASCIZ "

3914 016100 004737 016146 JSR PC,ERROR\$;GO TO USER ERROR ROUTINE

3915 016104 005777 163206 2\$: TST 0\$WR ;HALT ON ERROR

3916 016110 100001 BPL .+4 ;SKIP IF CONTINUE

3917 016112 000000 HALT ;HALT ON ERROR!

3918 016114 004737 017640 JSR PC,KBDINT ;CHECK FOR INHIBIT LOOP ON ERROR

3919 016120 032777 001000 163170 BIT #SW9,0\$WR ;SKIP IF LOOP ON ERROR

3920 016126 001001 BNE .+4 ;RETURN

3921 016130 000002 RTI ;CLEAR ITERATION COUNT

3922 016132 105037 001201 CLR B ICNT+1 ;LOOP ON TEST UNTIL NO ERRORS

3923 016136 000137 015742 JMP KITS\$;

3924 016142 000000 HLTCT\$: 0 ;HLT ARGUMENT

3925 016144 000000 HLTADR: 0 ;LAST HLT INSTRUCTION EXECUTED

3926 016146 ; ;

3927 016146 013705 001210 ; ;

3928 016152 004737 016562 JSR PC,PRINTR ;TYPE CSR IN OCTAL

3929 016156 042737 007700 016204 BIC #7700,2\$;TYPE LEADING ZERO'S

3930 016164 105337 016142 1\$: DECB HLTCT\$;

3931 016170 100411 BMI 3\$;

3932 016172 062737 000100 016204 ADD #100,2\$;

3933 016200 000004 017241 TYPE, SPACE ;

3934 016204 010005 2\$: MOV %0,TTY ;TYPE REGISTER X IN OCTAL

3935 016206 004737 016562 JSR %7,PRINTR ;

3936 016212 000764 BR 1\$;

3937 016214 000207 RTS PC ;

;SUBROUTINE TO SAVE INPUT AS OCTAL NUMBER

				016510	READIN: NOV		81. INHRE	READS	: GO READ TTY UNTIL CR
				020001	JSR		82. INHRE		: PUSH R1 ON STACK
				020002	CLR		83. - (6)		: PUSH R2 ON STACK
				020003	MOV		84. - (6)		: PUSH R3 ON STACK
				020004	MOV		85. - (6)		
				020005	MOV		86. - (6)		
				020006	MOV		87. - (6)		
				020007	CMPE		88. - (6)		
				020008	MOVB		89. - (6)		
				020009	MOVB		90. - (6)		
				02000A	MOVB		91. - (6)		
				02000B	MOVB		92. - (6)		
				02000C	MOVB		93. - (6)		
				02000D	MOVB		94. - (6)		
				02000E	MOVB		95. - (6)		
				02000F	MOVB		96. - (6)		
				020010	MOVB		97. - (6)		
				020011	MOVB		98. - (6)		
				020012	MOVB		99. - (6)		
				020013	MOVB		100. - (6)		
				020014	MOVB		101. - (6)		
				020015	MOVB		102. - (6)		
				020016	MOVB		103. - (6)		
				020017	MOVB		104. - (6)		
				020018	MOVB		105. - (6)		
				020019	MOVB		106. - (6)		
				02001A	MOVB		107. - (6)		
				02001B	MOVB		108. - (6)		
				02001C	MOVB		109. - (6)		
				02001D	MOVB		110. - (6)		
				02001E	MOVB		111. - (6)		
				02001F	MOVB		112. - (6)		
				020020	MOVB		113. - (6)		
				020021	MOVB		114. - (6)		
				020022	MOVB		115. - (6)		
				020023	MOVB		116. - (6)		
				020024	MOVB		117. - (6)		
				020025	MOVB		118. - (6)		
				020026	MOVB		119. - (6)		
				020027	MOVB		120. - (6)		
				020028	MOVB		121. - (6)		
				020029	MOVB		122. - (6)		
				02002A	MOVB		123. - (6)		
				02002B	MOVB		124. - (6)		
				02002C	MOVB		125. - (6)		
				02002D	MOVB		126. - (6)		
				02002E	MOVB		127. - (6)		
				02002F	MOVB		128. - (6)		
				020030	MOVB		129. - (6)		
				020031	MOVB		130. - (6)		
				020032	MOVB		131. - (6)		
				020033	MOVB		132. - (6)		
				020034	MOVB		133. - (6)		
				020035	MOVB		134. - (6)		
				020036	MOVB		135. - (6)		
				020037	MOVB		136. - (6)		
				020038	MOVB		137. - (6)		
				020039	MOVB		138. - (6)		
				02003A	MOVB		139. - (6)		
				02003B	MOVB		140. - (6)		
				02003C	MOVB		141. - (6)		
				02003D	MOVB		142. - (6)		
				02003E	MOVB		143. - (6)		
				02003F	MOVB		144. - (6)		
				020040	MOVB		145. - (6)		
				020041	MOVB		146. - (6)		
				020042	MOVB		147. - (6)		
				020043	MOVB		148. - (6)		
				020044	MOVB		149. - (6)		
				020045	MOVB		150. - (6)		
				020046	MOVB		151. - (6)		
				020047	MOVB		152. - (6)		
				020048	MOVB		153. - (6)		
				020049	MOVB		154. - (6)		
				02004A	MOVB		155. - (6)		
				02004B	MOVB		156. - (6)		
				02004C	MOVB		157. - (6)		
				02004D	MOVB		158. - (6)		
				02004E	MOVB		159. - (6)		
				02004F	MOVB		160. - (6)		
				020050	MOVB		161. - (6)		
				020051	MOVB		162. - (6)		
				020052	MOVB		163. - (6)		
				020053	MOVB		164. - (6)		
				020054	MOVB		165. - (6)		
				020055	MOVB		166. - (6)		
				020056	MOVB		167. - (6)		
				020057	MOVB		168. - (6)		
				020058	MOVB		169. - (6)		
				020059	MOVB		170. - (6)		
				02005A	MOVB		171. - (6)		
				02005B	MOVB		172. - (6)		
				02005C	MOVB		173. - (6)		
				02005D	MOVB		174. - (6)		
				02005E	MOVB		175. - (6)		
				02005F	MOVB		176. - (6)		
				020060	MOVB		177. - (6)		
				020061	MOVB		178. - (6)		
				020062	MOVB		179. - (6)		
				020063	MOVB		180. - (6)		
				020064	MOVB		181. - (6)		
				020065	MOVB		182. - (6)		
				020066	MOVB		183. - (6)		
				020067	MOVB		184. - (6)		
				020068	MOVB		185. - (6)		
				020069	MOVB		186. - (6)		
				02006A	MOVB		187. - (6)		
				02006B	MOVB		188. - (6)		
				02006C	MOVB		189. - (6)		
				02006D	MOVB		190. - (6)		
				02006E	MOVB		191. - (6)		
				02006F	MOVB		192. - (6)		
				020070	MOVB		193. - (6)		
				020071	MOVB		194. - (6)		
				020072	MOVB		195. - (6)		
				020073	MOVB		196. - (6)		
				020074	MOVB		197. - (6)		
				020075	MOVB		198. - (6)		
				020076	MOVB		199. - (6)		
				020077	MOVB		200. - (6)		
				020078	MOVB		201. - (6)		
				020079	MOVB		202. - (6)		
				02007A	MOVB		203. - (6)		
				02007B	MOVB		204. - (6)		
				02007C	MOVB		205. - (6)		
				02007D	MOVB		206. - (6)		
				02007E	MOVB		207. - (6)		
				02007F	MOVB		208. - (6)		
				020080	MOVB		209. - (6)		
				020081	MOVB		210. - (6)		
				020082	MOVB		211. - (6)		
				020083	MOVB		212. - (6)		
				020084	MOVB		213. - (6)		
				020085	MOVB		214. - (6)		
				020086	MOVB		215. - (6)		
				020087	MOVB		216. - (6)		
				020088	MOVB		217. - (6)		
				020089	MOVB		218. - (6)		
				02008A	MOVB		219. - (6)		
				02008B	MOVB		220. - (6)		
				02008C	MOVB		221. - (6)		
				02008D	MOVB		222. - (6)		
				02008E	MOVB		223. - (6)		
				02008F	MOVB		224. - (6)		
				020090	MOVB		225. - (6)		
				020091	MOVB		226. - (6)		
				020092	MOVB		227. - (6)		
				020093	MOVB		228. - (6)		
				020094	MOVB		229. - (6)		
				020095	MOVB		230. - (6)		
				020096	MOVB		231. - (6)		
				020097	MOVB		232. - (6)		
				020098	MOVB		233. - (6)		
				020099	MOVB		234. - (6)		
				02009A	MOVB		235. - (6)		
				02009B	MOVB		236. - (6)		
				02009C	MOVB		237. - (6)		
				02009D	MOVB		238. - (6)		
				02009E	MOVB		239. - (6)		
				02009F	MOVB		240. - (6)		
				0200A0	MOVB		241. - (6)		
				0200A1	MOVB		242. - (6)		
				0200A2	MOVB		243. - (6)		
				0200A3	MOVB		244. - (6)		
				0200A4	MOVB		245. - (6)		
				0200A5	MOVB		246. - (6)		
				0200A6	MOVB		247. - (6)		
				0200A7	MOVB		248. - (6)		
				0200A8	MOVB		249. - (6)		
				0200A9	MOVB		250. - (6)		
				0200AA	MOVB		251. - (6)		
				0200AB	MOVB		252. - (6)		
				0200AC	MOVB		253. - (6)		
				0200AD	MOVB		254. - (6)		
				0200AE	MOVB		255. - (6)		
				0200AF	MOVB		256. - (6)		
				0200B0	MOVB		257. - (6)		
				0200B1	MOVB		258. - (6)		
				0200B2	MOVB		259. - (6)		
				0200B3	MOVB		260. - (6)		
				0200B4	MOVB		261. - (6)		
				0200B5	MOVB		262. - (6)		
				0200B6	MOVB		263. - (6)		
				0200B7	MOVB		264. - (6)		
				0200B8	MOVB		265. - (6)		
				0200B9	MOVB		266. - (6)		
				0200BA	MOVB		267. - (6)		
				0200BB	MOVB		268. - (6)		
				0200BC	MOVB		269. - (6)		
				0200BD	MOVB		270. - (6)		
				0200BE	MOVB		271. - (6)		
			</						

C07

MAINDEC-11-0201A-0
0201A0.PII

BULL LOGIC TESTS TRY INPUT ROUTINE

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: OCTAL OCTAL TYPEOUT ROUTINE

: THIS ROUTINE IS USED TO TYPE AN OCTAL NUMBER ON THE TTY. IT WILL TYPE
 : ALL 8 CHARACTERS, SUPPRESS LEADING ZEROES, TYPE AN 16 BIT ADDRESS, OR TYPE
 : THE 16 BITS. IT IS CALLED VIA THE DUMP, SDUMP, DUMP16, OR BITYPE MACRO'S.

0165552	016737	170101 016720	BITYPS:	MOV #170101..PR	SET BIT FLAG AND 16. CHARACTER COUNT
			BR .PTIT	.PTIT	NOW TYPE IT IN BIT FORM
		000001 016720	PRINTR:	MOVB \$1..PR	SET ZERO FILL SWITCH
			BR .+	.+	SKIP
		016720 177772	PRINTS:	CLR .PR	SUPPRESS LEADING ZERO'S
			MOVB \$-6..PR+1		SET COUNT
		016722	.PTIT:	MOV R4,-(S)	SAVE R4
			MOV \$PR+2,R4	(4)	SET POINTER TO FIRST ASCII CHAR.
			CLRB (4)	.PRF	CLEAR FIRST BYTE
			CLRB (4)		ROTATE FIRST BIT
		000100 016720	.PRL:	CLRB (4)	CLEAR BYTE OF CHARACTER
			BITSET .PRF	\$100..PR	BIT TYPING MODE?
			ROL TT	.PRF	YES - SKIP 2 ROTATES
			ROL TT	(4)	ROTATE BIT INTO C
			ROL TT	(4)	PACK IT
			ROL TT	(4)	ROTATE BIT INTO C
			ROL TT	(4)	PACK IT
			ROL TT	(4)	ROTATE BIT INTO C
			ROL TT	(4)	IS IT ZERO?
		016720	.PRF:	INC	SKIP INC
		016720		SET FILL SWITCH	SET FILL SWITCH
		000060		CHECK FILL SWITCH	SKIP BITSET
		016721		MAKE INTO ASCII CHAR	MAKE INTO ASCII CHAR
		016722		INC COUNT	INC COUNT
		000060		REPEAT	REPEAT
		016722		EMPTY BUFFER?	EMPTY BUFFER?
			BR .PR+1		SKIP IF NOT
			BR .PR+2,R4		LOAD 1 ZERO
			MOV R4,(4)		NULL TERMINATOR
			TYPE IT		TYPE IT
			MOV R4,R4		RESTORE R4
			BLKW		RETURN
					COUNT, SWITCH, AND OUTPUT BUFFER

MAINDEC-11-02DJ9-D
02DJ9D.P11DJ11 LOGIC TESTS
POWER DOWN AND UP ROUTINES

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016740	016744	012777	017072	000126	PDOWN\$:	MOV	#ILLUF, \$PUVECS	SET FOR FAST UP
016741	016752	010077	000340	000125		MOV	#340, \$PUVECS+2	:PRIO:7
016753	016760	010046				MOV	R0,-(6)	PUSH R0 ON STACK
016762	010146					MOV	R1,-(6)	PUSH R1 ON STACK
016763	010246					MOV	R2,-(6)	PUSH R2 ON STACK
016764	010346					MOV	R3,-(6)	PUSH R3 ON STACK
016765	010446					MOV	R4,-(6)	PUSH R4 ON STACK
016770	010546					MOV	R5,-(6)	PUSH R5 ON STACK
016772	010646					MOV	\$SP, SAVR6	SAVE SP
016773	010637		017076	000072		MOV	\$PUPS, \$PUVECS	SET UP VECTOR
017000	012777		017010	000072		HALT		:WAIT FOR PF
017005	000000							
017010	013706	017076			PUPS:	MOV	.SAVR6, SP	GET SP
017014	005001				15:	CLD		:WAIT LOOP FOR THE TTY
017016	005201					INC		:WAIT FOR THE INC
017020	001326					BNE	16	:OF WORD
017022	012606					MOV	(6)+, R5	POP STACK INTO R5
017024	012604					MOV	(6)+, R4	POP STACK INTO R4
017026	012603					MOV	(6)+, R3	POP STACK INTO R3
017030	012602					MOV	(6)+, R2	POP STACK INTO R2
017032	012601					MOV	(6)+, R1	POP STACK INTO R1
017034	012600					MOV	(6)+, R0	POP STACK INTO R0
017036	016737	016744	000024			MOV	#PDOWN\$, #24	SET UP THE POWER DOWN VECTOR
017044	012737	000340	000026			MOV	#340, #26	:PRIO:7
017050	000004	017056				TYPE	+2	:ASCIZ <15><12>"POWER"
017056	000137	002304				JMP	AESTAR	:JMP TO USER ADDRESS
017072	000000				ILLUF:	HALT		:THE POWER UP SEQUENCE WAS STARTED
017074	000776					BR	.-2	:BEFORE THE POWER DOWN WAS COMPLETE
017076	000000					SAVR6:	0	:PUT THE SP HERE
017100	000024	000026				PUVECS:	24,26	:POWER UP VECTOR

MAINDEC-11-DZDJIA-D
DZDJIA.D.F11DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 81
POWER DOWN AND UP ROUTINES

 :IOT HANDLER. REENTERENT ROUTINE TO EITHER TYPE MESSAGES OR
 :INDICATE A FAULSE INTERRUPT OR TRAP.

017104	022715	001000	IOTRAP: CMP #1000, (SP)	:CHECK RETURN ADDRESS FOR FAULSE TRAP
017110	002407		BLT IOTS	:BRANCH IF "TYPE" COMMAND INTENDED
017112	162716	000004	SUB #4, (SP)	:GET VECTOR ADDRESS FROM RETURN ADDRESS
017114	012601		MOV (SP)+, R1	:PUT IN R1 FOR TYPING
017116	005706		TST (SP)+	:POP STACK
017118	011506		MOV (SP), R2	:SAVE RETURN ADDRESS FOR TYPING
017120	104002		HLT+2	:UNEXPECTED INTERRUPT OR TRAP

017126	000002		RTI	:R1 = VECTOR ADDRESS :R2 = RETURN PC :CONTINUE THE PROGRAM
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:MOCALL STYPE
 : STYPE MESSAGE TYPEOUT ROUTINE

:THIS ROUTINE IS USE TO TYPE ASCII MESSAGES ON THE TTY. THE
 :CALL CAN BE IN ONE OF 3 FORMS: 1) "TYPE ADR" - TYPES THE
 :MESSAGE STARTING IN LOCATION "ADR:" 2) "TYPE CHAR" - TYPES
 :THE ASCII "CHAR", AND 3) "PRINT <(15)<12>"MESSAGE">" - TYPES
 :THE MESSAGE WHICH IS INLINE ASCII.

017130	010546		IOTS: MOV TTY,-(6)	:SAVE TTY
017132	017605	000002	MOV #2(6),TTY	:GET ADDRESS TO BE TYPED
017134	032705	177400	BIT #177400,TTY	:IS IT A TYPING?
017142	001004		BNE 1\$:NO
017144	010537	017234	MOV TTY,.TYPE	:GET THE CHARACTER
017150	012705	017234	MOV #.TYPE.TTY	:FUDGE THE ADDRESS
017154	105715		TSTB (TTY)	:TERMINATOR?
017156	001406		BEO 2\$:GET OUT IF SO
017158	112537	177566	MOVE (TTY)+,2#177566	:LOAD AND TYPE THE CHARACTER
017160	105737	177564	TSTB 2#177564	:IS THE PRINTER READY
017162	100376		SPL -4	:WAIT UNTIL IT IS
017164	000770		BR .6	:GET THE NEXT CHARACTER
017174	017646	000002	2\$: MOV #2(6),-(6)	:SET ADDRESS TO BE TYPED
017200	062766	000002	ADD #2(6)	:ADD 2 TO THE ADDRESS
017206	022666	000002	CMP #6)+.2(6)	:IS IT .+2?
017212	001006		BNE 3\$:NO
017214	062705	000002	ADD #2.TTY	:ADD 2 TO THE ADDRESS
017220	042705	000001	BIC #1.TTY	:SHCK UP TO AN EVEN BYTE
017224	010566	000002	MOV TTY,2(6)	:RESTORE ADDRESS
017230	012605		MOV (6)+,TTY	:RESTORE TTY
017232	000002		RTI	:RETURN
017234	000000		.TYPE: 0	:CHARACTER TYPE LOCATION

017236	005015	000	RETURN: .ASCIZ <(15)<12>	
017241	0450	000040	SPACE: .ASCIZ "	
017244	005015	044506	MSGADR: .ASCIZ <(15)<12>"FIRST DJ11 ADDRESS: "	

017252	020124	045104	MSGVEC: .ASCIZ <(15)<12>"VECTOR ADDRESS: "	
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017260	040440	042104		
017262	061523	020072		
017264	005015	042526		
017302	051117	040440		
		042104		

MAINDEC-11-DDDJIA-D
DDDJAD.FIIDJ11 LOGIC TESTS
TYPE ROUTINE

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017310	042522	051523	020072	
017316	000040			
017320	005015	047516	020056	MSGNUM: .ASCIZ <15><12>"NO. OF DJ11'S: "
017326	043117	042040	030512	
017334	023461	035123	020040	
017343	0000			
017344	015	051412	040524	MSGCON: .ASCIZ <15><12>"STANDARD CONFIGURATION" "
017345	042116	051101	020104	
017346	051126	051116	043511	
017347	037516	051101	047511	
017348	051101	020040	047111	MSGLIN: .ASCIZ <15><12>"LINES "
017404	051500	046012		
017410	026440	000040		
017414	005015	044103	051101	MSGDAS: .ASCIZ " - "
017420	046005	047105	052107	MSGLEN: .ASCIZ <15><12>"CHAR LENGTH: "
017426	035110	020040	051101	
017435	015	050012	047101	
017440	052111	024131	026104	MSGPAR: .ASCIZ <15><12>"PARITY(0, ODD, EVEN): "
017450	020054	024112	024516	
017456	042440	000040		
017464	020072	000040		

.EVEN

;ROUTINE TO AUTOMATICALLY DETERMINE THE NUMBER OF DJ11'S ON THE SYSTEM
AND WHERE THEIR INTERRUPT VECTORS ARE.
THIS ROUTINE IS ONLY USED IF LOC 70 IS NOT ZERO, AS WHEN THE PROGRAM IS
BEING RUN UNDER ACT11 OR DDP MONITOR CONTROL.
NOTE: SOME OF THE LOGIC MUST BE FUNCTIONAL OR THIS ROUTINE WILL BOMB!

017470	012700	160000		
017474	012700	000001		
017500	012700	000002	000006	AUTO: MOV \$160000, RD
017504	00000001			SI, RD
017508	00000001			MOV SI, RD
017512	00000001			SETI, RD
017516	00000001			SET CARRY
017520	00000001			CHECK FOR ANY DJ11'S
017524	00000001			BRANCH IF IT TIMES OUT
017528	00000001			POINT TO NEXT DJ11 ADDRESS
017532	00000001			COUNT DJ11'S
017536	00000001			LOOK FOR MORE
017540	00000001			
017544	005308			BB: DEC RD
017548	100405			BRANCH IF DONE
017552	062700	000010		POINT TO FIRST DJ11
017556	010037	001200		SAVE FIRST DJ11 ADDRESS
017560	000761			GO COUNT DJ11'S
017564	005037	000006		BB: MOV RD, DEVAR
017568	007137	001234		BRANCH IF DONE
017572	001006			SAVE FIRST DJ11 ADDRESS
017576	104000			REPORT THAT NO DJ11'S WERE FOUND
017580	000137	015410		JMP DONE
017584	013746	000000		EXIT THIS PROGRAM

;ROUTINE TO DETERMINE VECTOR ADDRESSES

38: MOV \$SEC, -[SP] ;SAVE IOT VECTOR ON THE STACK

M31NDEC-11-0200JA-D
1200AC.FIIDUTY LOGIC TESTS
AUTOMATIC SYSTEM SIZER

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017620	012237	017624	000000		MOV	\$48	0\$20	:RESET IOT VECTOR
017620	001201	040400			MOV	DEVAOR, \$1		:SET FIRST DJ ADR
					MOV	\$40400, (R1)+		:SET OSR
017626	005721	000001			TST	\$1+		:BIT8 = TRANS SCAN ENABLE
017626	0000001				MOV	\$1, (R1)+		:BIT14 = TRANS INTERRUPT ENABLE
017626	0012637	000000			WAIT			:INC POINTER
017626	0000207				MOV	(SP)+, 0\$20		:SET TOR LINE 0
					RTS	PC		:WAIT FOR AN INTERRUPT
017634	162716	000010		48:	SUB	\$10, (SP)		:REPOSITION ADDRESS TO RVC VEC
017634	0011697	001232			MOV	(\$00), VPCADR		:SAVE FIRST VECTOR
017636	000002				MOV	(SP)+, (SP)+		:RESET STACK FROM IOT
					RTS	PC		:RETURN FROM INTERRUPT - RESTORE STATUS
017640	022737	000176	001316	KBDINT:	CMP	\$SWREG, SWR		
017646	001016				BNE	1\$		
017650	005037	017706			MOV	TMP1		
017650	113732	017706			MOV	177562, TMP1		
017650	148732	000200	017706		MOV	\$200, TMP1		
017650	148732	000007	017706		MOV	\$1, TMP1		
017700	004737	017770			RTS	PC, CNTLU		
017704	000207			18:	RTS	PC		
017706	000000				TMPI:	0		
017710	013746	000006			SUBWR:	MOV	6,-(SP)	
017714	013746	000004			MOV	4,-(SP)		
017720	012737	017740	000004		MOV	sis,4		
017726	022777	177777	161362		OMP	\$-1,0\$WR		
017734	001402				BNE	2\$		
017736	000407				BNE	3\$		
017740	022626			18:	CMP	(SP)+, (SP)+		
017742	012737	000176	001316	28:	MOV	\$SWREG, SWR		
017750	012737	000174	001320	38:	MOV	\$DISPREG, DISPLAY		
017756	012637	000004			MOV	(SP)+,4		
017762	012637	000006		38:	MOV	(SP)+,6		
017766	000207				RTS	PC		
017770	022737	000176	001316	CNTLU:	OMP	\$SWREG, SWR		
017776	001023				BNE	1\$		
020000	000004	020062			TYPE	SWREG		
020004	013705	000176			MOV	SWREG, TTY		:TYPE SWREG IN OCTAL
020010	004737	016562			JSR	PC, PRINTR		:TYPE LEADING ZERO'S
020014	000004	020052			TYPE	NEWIS		
020020	004537	016216			JSR	R5, READIN		
020024	017706				WORD	TMP1		
020026	001360				BNE	CNTLU		
020030	022737	000020	020050		COMP	\$20, CNT		
020036	001403				BEO	1\$		
020040	013777	017706	161250		MOV	TMP1, SWR		

MAINDEC-11-022034-0
1220340.F11 AUTOMATIC LOGIC TESTS
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020040	020046	000007	18:	R/S	PC
	020050	000000	CNT:	0	
	020052	020040	042516	036527	NEWIS: .ASCII " NEW= "
	020054	020040	053523	036522	SAREQ: .ASCII <15><12>"SWR= "
		000001			END

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MAINDEC-11-D2DJA-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 96
D2DJA-D.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

AUTO	017470	596	4158*	3458	3463*	3464	3484*	3538*	3563*	3635*	3655*	3671
BCSR	001214	542*	3457*	3893								
SEGIN	001224	530	571*									
SELL =	000007	496*	3772									
BITYPES	016552	4005*										
BITO =	000001	497*	967	969	979	1111	1133	1201	1219	1237	1255	1293
BIT1 =	000002	1377	1405	1433	1477	2912	2982	2946	2995	3045	3090	3398
BIT10 =	002000	498*	800	801	810	1560	3015					
BIT11 =	004000	507*	894	895	894	2311						
BIT12 =	010000	508*	2394									
BIT13 =	020000	509*	905	906	915	2479	3244					
BIT14 =	040000	510*	2552	3140	3191	3255	3312					
BIT15 =	100000	511*	926	927	936	2645	3410					
BIT16 =	000004	512*	2728									
BIT17 =	000010	499*	821	822	831	949	962	951	1643			
BIT18 =	000020	500*	950	952	1726	2923	3315					
BIT19 =	000040	501*	956	1811	2924	2944	3379	3703	3938			
BIT20 =	000100	502*	1894									
BIT21 =	000200	503*	842	843	852	1977						
BIT22 =	000400	504*	2060									
BIT23 =	001000	505*	863	864	873	2145						
BIT24 =	001224	506*	2228									
CLRVEC	002236	727	729	732*								
CNT	020050	3940*	3959*	4237	4242*							
CNTLU	017770	730	4208	4228*	4236							
CONFIG	001766	629	660*	675								
CSR	001210	539*	738*	745*	750	779	780*	781*	800*	801	805	810
		822	826	830*	831	842*	843	847	851*	852	863*	864
		873	884*	885	889	893*	894	905*	906	910	914*	915
		931	935*	936	948*	950*	951	967*	968	969	973	979*
		994*	995*	996	1001*	1002*	1003*	1004*	1005	1019*	1020	1024*
		1030	1110*	1113	1129	1134	1149*	1154	1174	1179	1200*	1203
		1220	1236*	1238	1249*	1264*	1266	1277*	1292*	1294	1305*	1320*
		1348*	1350	1361*	1376*	1378	1399*	1404*	1406	1417*	1432*	1434
		1484	1488	1527	1533*	1561	1567	1571	1610	1616*	1644	1650
		1699*	1727	1733	1737	1776	1792*	1812	1819	1822	1861	1867*
		1905	1944	1950*	1978	1984	1988	2027	2033*	2061	2067	2071
		2146	2152	2156	2195	2201*	2229	2235	2239	2278	2284*	2312
		2361	2367*	2395	2401	2405	2444	2450*	2480	2496	2499	2529
		2569	2573	2612	2618*	2646	2652	2656	2695	2701*	2729	2736
		2784*	2814	2820	2823*	2824	2830	2843	2860*	2893	2896	2899
		2931*	2941*	2944	2947	2953	2966*	2967	2996	3002	3015*	3046
		3091	3094	3113*	3137	3148	3152	3180	3227	3244*	3245	3251
		3287	3302	3308	3311	3316*	3319	3340	3365*	3376*	3379	3393
		3396*	3397	3403	3435*	3436	3446*	3456*	3498	3566	3540*	3654*
		3698*	3703	3708	3715	3758*	3817*	3820*	3823*	3826*	3939	3941*
DEFADR	001312	560*	605									
DEFVEC	001314	561*										
DEVADR	001230	550*	601	603	605*	606*	607	745	4172*	4195		
DISPLA	001320	564*	3869*	3873*	4222*							
DISPRE	000174	526*	4222									
DJLEN	001306	558*	740*	747*	1511	1594	1677	1760	1794*	1945	1929	2011
DJMXNO=	000020	2179	2262	2345	2428	2452*	2513	2596	2679	2762	2796*	3730*
DJPAR	001310	515*	655	741*	748*	3510	3596					
DTUUT	001204	559*	741*	748*	3510	3596	749*	3762				
		557*	658*	742	744*	749*						

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MAINDEC-11-DZDJR-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 87
DZDJR.D11 CROSS REFERENCE TABLE -- USER SYMBOLS

MAINDEC-11-DZDJAD-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 89
DZDJAD.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

		3941	3971	3972	3998*									
IOTRAP	017104	576	4077*											
IOTS	017130	4078	4097*											
I5R20	004424	1232	1242*											
I5R23	004544	1260	1270*											
I5R24	004564	1289	1298*											
I5R25	005006	1316	1327*											
I5R26	005126	1344	1355*											
I5R27	005246	1372	1383*											
I5R30	005366	1400	1411*											
I5R31	005506	1428	1439*											
I5R56	012620	3034	3053*											
I5R57	012774	3079	3099*											
I5R66	015274	3705	3735*											
KODINT	017640	3767	3853	3890	3909	4201*								
KITS	015742	3859	3865	3872*	3913									
LAD	015770	766*	1101*	1461*	1785*	2119*	2453*	2794*	3869*	3874	3876	3879*		
LENGTH	001236	553*	665	678	747									
LEVEL?	= 000340	513*	778											
LOOP32	005574	1478*	1479											
LOOP33	005774	1561*	1562											
LOOP34	006174	1644*	1645											
LOOP35	006374	1727*	1728											
LOOP36	006606	1812*	1813											
LOOP37	007006	1895*	1896											
LOOP40	007206	1978*	1979											
LOOP41	007406	2051*	2062											
LOOP42	007620	2146*	2147											
LOOP43	010020	2229*	2230											
LOOP44	010220	2312*	2313											
LOOP45	010420	2395*	2396											
LOOP46	010632	2480*	2481											
LOOP47	011032	2563*	2564											
LOOP50	011232	2646*	2647											
LOOP51	011432	2729*	2730											
LOOP61	014060	3383*	3384	3444										
LOOP64	014550	3562*	3638											
MSGADR	017244	599	4122*											
MSGCON	017343	660	4134*											
MSGDAS	017410	684	4141*											
MSGLEN	017414	689	4142*											
MSGLIN	017377	681	4139*											
MSGNUM	017320	622	4130*											
MSGPAR	017435	704	4145*											
MSGVEC	017274	610	4126*											
N = 000067		421*	770	794*	815*	836*	857*	878*	899*	920*	941*	969*	1012*	1035*
		1053*	1077*	1100*	1102	1141*	1192*	1226*	1254*	1290*	1310*	1339*	1366*	1394*
		1422*	1450*	1452	1535*	1618*	1701*	1784*	1786	1869*	1959*	2035*	2119*	2160*
		2203*	2286*	2369*	2452*	2454	2537*	2620*	2703*	2796*	2829*	2964*	3096*	3160*
		3028*	3073*	3118*	3370*	3450*	3469*	3545*	3543*	3644	3695*	3751*		
NEWIS	020052	4233	4244*											
OPEN	= 000000	514*												
OVERS	015746	3857	3873*											
PARITY	001276	554*	679	718	3510	3596								
PC	=%000007	495*	572*	596*	623*	661*	683*	687*	690*	705*	730*	1470*	1553*	1636*
		1719*	1804*	1887*	1970*	2053*	2139*	2221*	2304*	2387*	2472*	2555*	2638*	2721*

MAINDEC-11-DZDJAD.D
DZDJAD.PIIDJ11 LOGIC TESTS
CROSS REFERENCE TABLE -- USER SYMBOLS

MACY11 27(732)

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PONT	001204	2804*	2875*	2998*	3038*	3083*	3128*	3478*	3554*	3662	3767*	3842*	3953*	3890*
PDOWN\$	016744	3902*	3904*	3909*	3920*	3929*	3934*	3995*	4038*	4193*	4208*	4209*	4225*	4232*
PRINTR	016562	4240*	537*	592*	593*	3768*	3769*	3794						
PRINTS	016572	579	4040*	4062	3927	4007*	4232							
PS	= 177776	3902	3920	3927	4007*	4232								
PSTEMP	016362	693	687	4009*										
PUPS	017010	486*	1234*	1235*	1250*	1262*	1263*	1278*	1290*	1291*	1306*	1318*	1319*	1334*
PUVECS	017100	1346*	1347*	1362*	1374*	1375*	1390*	1402*	1403*	1418*	1430*	1431*	1446*	3036*
RSUF	001212	3037*	3069*	3081*	3082*	3114*	3240*	3241*	3299*	3300*	3366*	3652*	3694*	3695*
RCVLVL	001222	3961	3965*	3968*										
RCVVEC	001220	3961*	3965	3968*										
READIN	016216	4049	4052*											
READS	016364	4040*	4041*	4049*	4071*									
RESTAR	002302	540*	752*	1492	1523	1575	1606	1658	1689	1741	1772	1826	1857	1909
RETURN	017236	1940	1992	2023	2075	2106	2160	2191	2243	2274	2326	2357	2409	2440
RD	=%000000	2494	2525	2577	2608	2660	2691	2743	2774	2827	2855	2905	2913	2921
		2962	2975	3011	3020	3057	3102	3201	3261	3266	3325	3356	3405	3428
		3501	3535	3581	3630	3675	3721	3735	3750					
R1	=%000001	546*	760*	3035*	3065	3066*	3080*	3110	3111*	3243*	3360	3361*	3706*	3755
		3756*												
READIN	016216	545*	739*	746*	759	3034*	3065*	3079*	3110*	3242*	3301*	3360*	3705*	3755*
READS	016364	600	611	3933*	4234									
RESTAR	002302	623	651	690	705	3934	3970*	3764	3792	4065				
RETURN	017236	532	597	663	671	673	724*	3764						
		4120*												
		487*	573*	574*	575*	576*	577*	578*	579*	580*	581*	592*	593*	595*
		664*	668*	676*	720*	721	732*	733	734*	735*	736	1112*	1115*	1121
		1153*	1156*	1164	1202*	1207*	1211*	1214*	1481*	1486*	1491	1564*	1569*	1574
		1647*	1652*	1657	1730*	1735*	1740	1815*	1820*	1825	1898*	1903*	1909	1981*
		1986*	1991	2064*	2069*	2074	2149*	2154*	2159	2232*	2237*	2242	2315*	2320*
		2325	2398*	2403*	2408	2483*	2488*	2493	2566*	2571*	2576	2649*	2654*	2659
		2732*	2737*	2742	2788*	2789*	2790*	2791*	2793	2839*	2848*	2893*	2898*	2950*
		2959*	2970*	2999*	3009*	3136*	3144*	3147*	3156*	3177*	3193*	3200*	3221*	3265*
		3281*	3324*	3341*	3343	3389*	3394*	3495*	3491*	3562*	3569*	3696*	3707	3731*
		3784*	3828*	3830*	3833*	3834*	4042	4051*	4159*	4163	4165*	4171*	4172	
		488*	626*	628	630	632*	645	646*	647*	648*	650*	651*	653*	655
		657	665*	666*	677*	682	695*	686	688*	716	750*	751*	752	753*
		754	756*	757	758*	759	760	761	762	763	764	787*	951*	952
		956	962	968*	980*	996*	997	1005*	1006	1020*	1030*	1042*	1043	1048*
		1061*	1062	1070*	1071	1085*	1095*	1113*	1122*	1123*	1124*	1125	1134*	1150*
		1167	1186*	1203*	1212*	1220*	1238*	1266*	1294*	1322*	1350*	1378*	1406*	1434*
		1478*	1488*	1492*	1496	1503	1512	1519	1523*	1527*	1528	1561*	1571*	1575*
		1579	1586	1595	1601	1606*	1610*	1611	1644*	1654*	1658*	1662	1669	1678
		1684	1689*	1693*	1694	1727*	1737*	1741*	1745	1752	1761	1767	1772*	1776*
		1777	1812*	1822*	1826*	1830	1837	1846	1852	1857*	1861*	1862	1975*	1975*
		1909*	1913	1920	1929	1935	1940*	1944*	1945	1978*	1998*	1992*	1996	2003
		2012	2018	2023*	2027*	2028	2061*	2071*	2075*	2079	2086	2095	2101	2106*
		2110*	2111	2145*	2156*	2160*	2164	2171	2180	2196	2191*	2195*	2196	2229*
		2239*	2243*	2247	2254	2263	2269	2274*	2278*	2279	2312*	2322*	2326*	2330
		2337	2346	2352	2357*	2361*	2362	2395*	2405*	2409*	2413	2420	2429	2435
		2440*	2444*	2445	2480*	2490*	2494*	2498	2505	2514	2520	2525*	2529*	2530
		2563*	2573*	2577*	2581	2588	2597	2603	2608*	2612*	2613	2646*	2656*	2660*
		2664	2671	2680	2686	2691*	2695*	2696	2729*	2739*	2743*	2747	2754	2763
		2769	2774*	2778*	2779	2814*	2827*	2830*	2831	2843*	2844	2951	2955*	2993*
		2886*	2889*	2896*	2901	2905*	2909	2913*	2917	2921*	2925*	2926	2947*	2953*

MAINDEC-11-DZDJAD-D
DZDJAD.FII CROS

DJ11 LOGIC TESTS MACY11
S REFERENCE TABLE -- USER SYMBOLS

MACY11 27(732)

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~~REF ID: A11-02204-A-2~~ - 2011 LOGIC TESTS
CROSS REFERENCE TABLE -

MACY11 27(732) 21-SEP-76 13:43 PAGE 91
USER SYMBOLS

720	001216
720	001217
TIMER	001303
00	000000

MAINDEQ-11-0220A-D
0220A.D.FII CROSS REF

A-D DJ111 LOGIC TESTS MACY!
CROSS REFERENCE TABLE -- USER SYMBOLS

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MAINDEC-11-02202A-2
MACYII 27(732) 21-SEP-76 13:43 PAGE 93
CROSS REFERENCE TABLE -- USER SYMBOLS

0000000000000000	4014	4017	4032#
0000000000000000	4005#	4031	
0000000000000000	4011#	4070#	
0000000000000000	4000#	4101#	4102
0000000000000000	4005#	4006#	4103#

MAINDEC-11-DZDJR-D DJ11 LOGIC TESTS MACY11 27(732) 21-SEP-76 13:43 PAGE 95
DZDJR.D11 CROSS REFERENCE TABLE -- MACRO NAMES

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MAINDEC-11-0000A-D D11 LOGIC TESTS MACY11 27(732) 01-SEP-76 13:43 PAGE 96
0000A-D.F11 CROSS REFERENCE TABLE -- MACRO NAMES

F08

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

Conseil et est porté à croire que l'ordre de la Confédération n'a pas été rompu.

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2020-2021
2021-2022

3722
Cathartes aura - Common Vulture
Gyps fulvus - Steppe Vulture
Coragyps atratus - Turkey Buzzard
Aegypius monachus - Monk Vulture

Constitutive *Constitutive*
-*located in the cytosol* -*located in the nucleus*
-*located in the membrane* -*located in the nucleoplasm*

On the other hand, the more economic the model, the more it can be used to predict the future. This is because the model is based on the assumption that the economy is stable and predictable. The model also assumes that the economy is not subject to external factors such as political instability or natural disasters.

Consequently, the following conclusions can be drawn:

Collected from the same locality as the last specimen, but in a different place. The body is longer and more slender than in the last specimen, and the head is larger. The dorsal fin is situated further back than in the last specimen, and the pectoral fins are longer and more pointed. The scales are larger and more numerous.

Constitutive Constitutive
Growth Growth

A GENEALOGY OF THE HODGES

total station - £4000.
to station - £1000.

Journal of Health Politics, Policy and Law

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and it is the best way to do it.

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	8010	8011	8012	8013	8014	8015	8016	8017	8018	8019	8020	8021	8022	8023	8024	8025	8026	8027	8028	8029	8030	8031	8032	8033	8034	8035	8036	8037	8038	8039	8040	8041	8042	8043	8044	8045	8046	8047	8048	8049	8050	8051	8052	8053	8054	8055	8056	8057	8058	8059	8060	8061	8062	8063	8064	8065	8066	8067	8068	8069	8070	8071	8072	8073	8074	8075	8076	8077	8078	8079	8080	8081	8082	8083	8084	8085	8086	8087	8088	8089	8090	8091	8092	8093	8094	8095	8096	8097	8098	8099	80100	80101	80102	80103	80104	80105	80106	80107	80108	80109	80110	80111	80112	80113	80114	80115	80116	80117	80118	80119	80120	80121	80122	80123	80124	80125	80126	80127	80128	80129	80130	80131	80132	80133	80134	80135	80136	80137	80138	80139	80140	80141	80142	80143	80144	80145	80146	80147	80148	80149	80150	80151	80152	80

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 11-0224-0 D11 LOGIC TESTS CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

MOVE	3000	3001	3002	3003	3004	3005	3006	3007	3008	3009	3010	3011	3012	3013	3014	3015	3016	3017	3018	3019	3020	3021	3022	3023	3024	3025	3026	3027	3028	3029	3030	3031	3032	3033	3034	3035	3036	3037	3038	3039	3040	3041	3042	3043	3044	3045	3046	3047	3048	3049	3050	3051	3052	3053	3054	3055	3056	3057	3058	3059	3060	3061	3062	3063	3064	3065	3066	3067	3068	3069	3070	3071	3072	3073	3074	3075	3076	3077	3078	3079	3080	3081	3082	3083	3084	3085	3086	3087	3088	3089	3090	3091	3092	3093	3094	3095	3096	3097	3098	3099	3100	3101	3102	3103	3104	3105	3106	3107	3108	3109	3110	3111	3112	3113	3114	3115	3116	3117	3118	3119	3120	3121	3122	3123	3124	3125	3126	3127	3128	3129	3130	3131	3132	3133	3134	3135	3136	3137	3138	3139	3140	3141	3142	3143	3144	3145	3146	3147	3148	3149	3150	3151	3152	3153	3154	3155	3156	3157	3158	3159	3160	3161	3162	3163	3164	3165	3166	3167	3168	3169	3170	3171	3172	3173	3174	3175	3176	3177	3178	3179	3180	3181	3182	3183	3184	3185	3186	3187	3188	3189	3190	3191	3192	3193	3194	3195	3196	3197	3198	3199	3200	3201	3202	3203	3204	3205	3206	3207	3208	3209	3210	3211	3212	3213	3214	3215	3216	3217	3218	3219	3220	3221	3222	3223	3224	3225	3226	3227	3228	3229	3230	3231	3232	3233	3234	3235	3236	3237	3238	3239	3240	3241	3242	3243	3244	3245	3246	3247	3248	3249	3250	3251	3252	3253	3254	3255	3256	3257	3258	3259	3260	3261	3262	3263	3264	3265	3266	3267	3268	3269	3270	3271	3272	3273	3274	3275	3276	3277	3278	3279	3280	3281	3282	3283	3284	3285	3286	3287	3288	3289	3290	3291	3292	3293	3294	3295	3296	3297	3298	3299	3300	3301	3302	3303	3304	3305	3306	3307	3308	3309	3310	3311	3312	3313	3314	3315	3316	3317	3318	3319	3320	3321	3322	3323	3324	3325	3326	3327	3328	3329	3330	3331	3332	3333	3334	3335	3336	3337	3338	3339	3340	3341	3342	3343	3344	3345	3346	3347	3348	3349	3350	3351	3352	3353	3354	3355	3356	3357	3358	3359	3360	3361	3362	3363	3364	3365	3366	3367	3368	3369	3370	3371	3372	3373	3374	3375	3376	3377	3378	3379	3380	3381	3382	3383	3384	3385	3386	3387	3388	3389	3390	3391	3392	3393	3394	3395	3396	3397	3398	3399	3400	3401	3402	3403	3404	3405	3406	3407	3408	3409	3410	3411	3412	3413	3414	3415	3416	3417	3418	3419	3420	3421	3422	3423	3424	3425	3426	3427	3428	3429	3430	3431	3432	3433	3434	3435	3436	3437	3438	3439	3440	3441	3442	3443	3444	3445	3446	3447	3448	3449	3450	3451	3452	3453	3454	3455	3456	3457	3458	3459	3460	3461	3462	3463	3464	3465	3466	3467	3468	3469	3470	3471	3472	3473	3474	3475	3476	3477	3478	3479	3480	3481	3482	3483	3484	3485	3486	3487	3488	3489	3490	3491	3492	3493	3494	3495	3496	3497	3498	3499	3500	3501	3502	3503	3504	3505	3506	3507	3508	3509	3510	3511	3512	3513	3514	3515	3516	3517	3518	3519	3520	3521	3522	3523	3524	3525	3526	3527	3528	3529	3530	3531	3532	3533	3534	3535	3536	3537	3538	3539	3540	3541	3542	3543	3544	3545	3546	3547	3548	3549	3550	3551	3552	3553	3554	3555	3556	3557	3558	3559	3560	3561	3562	3563	3564	3565	3566	3567	3568	3569	3570	3571	3572	3573	3574	3575	3576	3577	3578	3579	3580	3581	3582	3583	3584	3585	3586	3587	3588	3589	3590	3591	3592	3593	3594	3595	3596	3597	3598	3599	3600	3601	3602	3603	3604	3605	3606	3607	3608	3609	3610	3611	3612	3613	3614	3615	3616	3617	3618	3619	3620	3621	3622	3623	3624	3625	3626	3627	3628	3629	3630	3631	3632	3633	3634	3635	3636	3637	3638	3639	3640	3641	3642	3643	3644	3645	3646	3647	3648	3649	3650	3651	3652	3653	3654	3655	3656	3657	3658	3659	3660	3661	3662	3663	3664	3665	3666	3667	3668	3669	3670	3671	3672	3673	3674	3675	3676	3677	3678	3679	3680	3681	3682	3683	3684	3685	3686	3687	3688	3689	3690	3691	3692	3693	3694	3695	3696	3697	3698	3699	3700	3701	3702	3703	3704	3705	3706	3707	3708	3709	3710	3711	3712	3713	3714	3715	3716	3717	3718	3719	3720	3721	3722	3723	3724	3725	3726	3727	3728	3729	3730	3731	3732	3733	3734	3735	3736	3737	3738	3739	3740	3741	3742	3743	3744	3745	3746	3747	3748	3749	3750	3751	3752	3753	3754	3755	3756	3757	3758	3759	3760	3761	3762	3763	3764	3765	3766	3767	3768	3769	3770	3771	3772	3773	3774	3775	3776	3777	3778	3779	3780	3781	3782	3783	3784	3785	3786	3787	3788	3789	3790	3791	3792	3793	3794	3795	3796	3797	3798	3799	3800	3801	3802	3803	3804	3805	3806	3807	3808	3809	3810	3811	3812	3813	3814	3815	3816	3817	3818	3819	3820	3821	3822	3823	3824	3825	3826	3827	3828	3829	3830	3831	3832	3833	3834	3835	3836	3837	3838	3839	3840	3841

MAINDEC-11-DZDJAD.D
DZDJAD.P11 CROS

-D DJ11 LOGIC TESTS MACY11 27
CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

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ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

5, DZDJD, SEC/SOL/CRF-5, DZDJD, MAC, DZDJD, P11

$$0.14 \times 0.02 = 0.0028$$

CORE USED: 33K (65 PAGES)

KOB

Spooler runtime 16 Seconds, 71 KCS, 416 disk reads, 3 disk writes, 97 pages