DH11

STATIC LOGIC TEST

MD-11-DZDHA-B

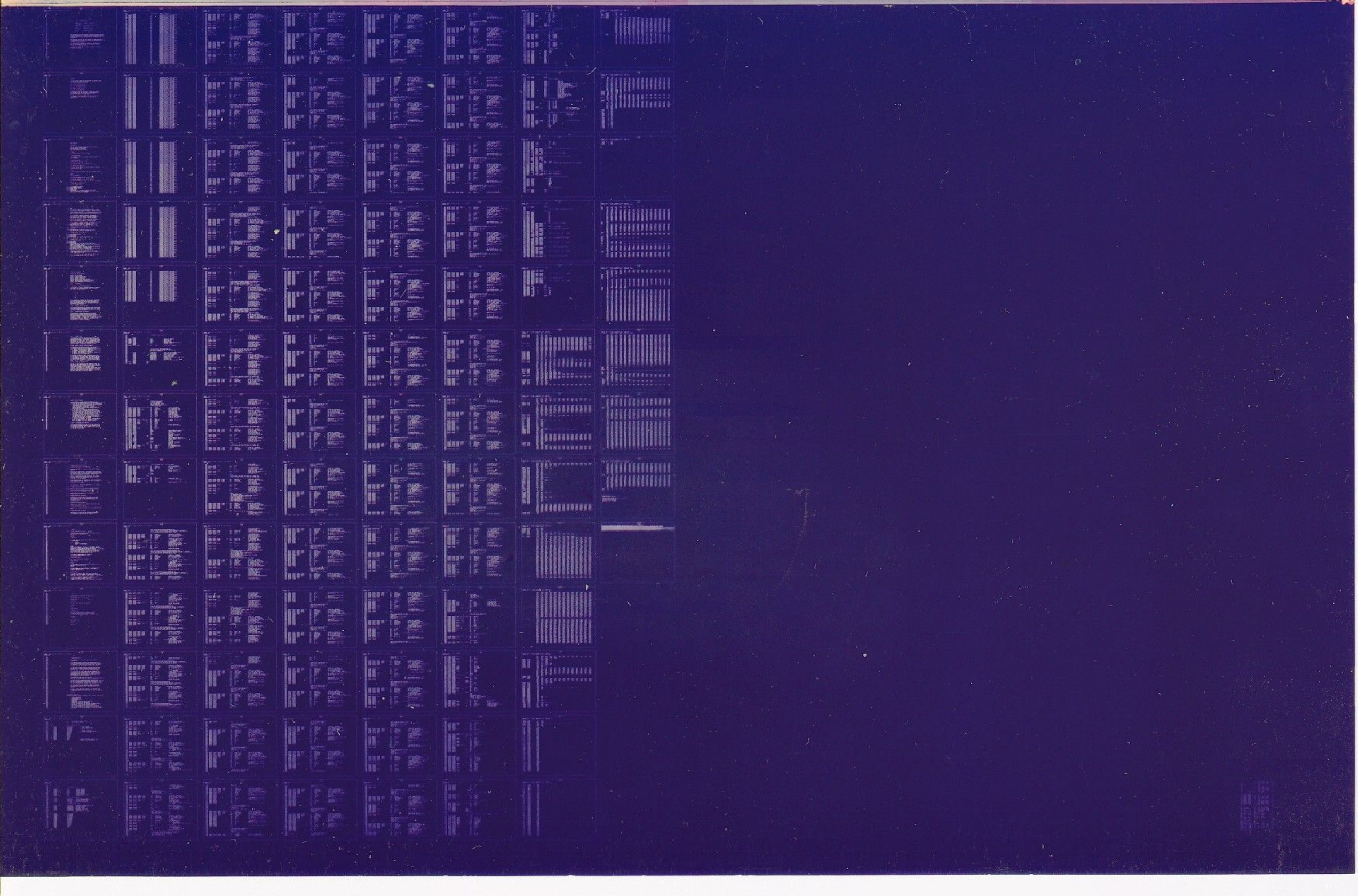
EP-DZDHA-B-DL-A

FICHE 1 OF 1

NOV 1976

digital

MADE IN U.S.A



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                                .REM !
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IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DZDHA-B-D
PRODUCT NAME:	DH11 STATIC LOGIC TEST
DATE:	APRIL 1976
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	MICHAEL DAVIS

1. ABSTRACT

THE DH11 STATIC LOGIC TEST IS DESIGNED TO PROVIDE A MEANS FOR TESTING THE CORRECT FUNCTION OF ALL READ/WRITE BITS IN THE FOLLOWING DH11 REGISTERS:

DH11 SYSTEM CONTROL REGISTER

DH11 LINE PARAMETER REGISTER

DH11 BREAK CONTROL REGISTER

DH11 SILO STATUS REGISTER

IN ADDITION, TESTS ARE PROVIDED TO CHECK THE FUNCTION OF THOSE BITS THAT ARE READ ONLY IN MAINTENANCE MODE. ALSO PROVIDED ARE TESTS OF REGISTER ADDRESSABILITY, AND OF THE FUNCTION OF MASTER CLEAR.

THE DIAGNOSTIC HAS BEEN WRITTEN SO THAT THE TESTING OF EACH FUNCTION IS CONTAINED IN AN INDIVIDUAL TEST LOOP.

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                                2.      REQUIREMENTS

                                2.1     EQUIPMENT

                                        PDP-11 FAMILY STANDARD COMPUTER WITH 8KW OF MEMORY
                                        ASR-33 TELETYPE OR EQUIVALENT
                                        DH11 ASYNCHRONOUS MULTIPLEXER
                                        DM11 MAINTENANCE CARD INSTALLED

                                2.2     STORAGE

                                        THE PROGRAM LOADS INTO 8KW OF MEMORY

                                3.      LOADING PROCEDURE

                                        THE STANDART PROCEDURE FOR LOADING ABSOLUTE BINARY TAPES
                                        IS TO BE USED

                                4.      STARTING PROCEDURE

                                4.1     CONTROL SWITCH SETTINGS

                                4.1.1   AFTER PROGRAM LOAD (INITIAL PROGRAM START)

                                        ALL CONSOLE SWITCHES DOWN

                                4.1.2   TO MODIFY DEVICE VECTOR AND CONTROL REGISTER ADDRESSES
                                        AFTER PROGRAM RESTART

                                        SW00=1

                                4.1.3   TO START PROGRAM AT SELECTED TEST AFTER PROGRAM RESTART

                                        SW01=1

                                4.2     STARTING ADDRESS

                                        THE STARTING ADDRESS FOR ALL TESTS IS 000200

                                        THE RESTART ADDRESS FOR ALL TESTS I 002000

                                        THE STARTING ADDRESS TO ENTER A SELECTED TEST IS 000200

                                4.3     PROGRAM AND/OR OPERATOR ACTION

                                4.3.1   INITIAL PROGRAM START

                                4.3.1.1 LOAD PROGRAM INTO MEMORY
                                4.3.1.2 LOAD ADDRESS 000200
                                4.3.1.3 CLEAR CONSOLE SWITCHES
                                4.3.1.4 PRESS START
                                4.3.1.5 THE PROGRAM WILL TYPE "DH11 STATIC LOGIC TEST"
                                        AND WILL THEN TYPE "VECTOR ADDRESS-" AND WAIT FOR AN
                                        INPUT FROM THE TELETYPE KEYBOARD.
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4.3 (CONT'D)

4.3.1.6 TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR
FOR THE DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

NOTE: WORDS IN ANGLE BRACKETS, I.E. <CARRIAGE RETURN> MEAN THAT
THE TELETYPE KEY WITH THE NAMED FUNCTION SHOULD BE STRUCK

IF AN INCORRECT ADDRESS IS ENTERED, THE PROGRAM
WILL TYPE "?" AND WILL REPEAT THE SECOND MESSAGE OF 4.3.1.5
4.3.1.7 THE PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-"
AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.1.8 TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER OF THE
DH11 TO BE TESTED FOLLOWED BY <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED, THE PROGRAM WILL TYPE
"?" AND WILL THEN REPEAT THE MESSAGE OF 4.3.1.7
4.3.1.9 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT IS
ABOUT TO START TESTING, AND THEN TESTING WILL BEGIN

4.3.2 PROGRAM RESTART WITH ALL SWITCHES DOWN

4.3.2.1 PERFORM 4.3.1.2 TO 4.3.1.5
4.3.2.2 THE PROGRAM WILL TYPE "DH11 STATIC LOGIC TEST"
AND WILL THEN CONTINUE AS DESCRIBED IN 4.3.1.9

4.3.3 PROGRAM RESTART WITH SW00=1

4.3.3.1 LOAD ADDRESS 000200
4.3.3.2 SET SW01=1
4.3.3.3 PRESS START
4.3.3.4 THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1.5 TO 4.3.1.9

4.3.4 PROGRAM RESTART WITH SW01=1

4.3.4.1 LOAD ADDRESS 000200
4.3.4.2 SET SW01=1
4.3.4.3 PRESS START
4.3.4.4 THE PROGRAM WILL TYPE "DH11 STATIC LOGIC TEST"
AND WILL THEN TYPE "TEST PC-" AND WILL WAIT FOR AN INPUT
FROM THE TELETYPE KEYBOARD
4.3.4.5 TYPE IN THE ADDRESS OF THE TEST AT WHICH THE PROGRAM IS TO
BE STARTED FOLLOWED BY <CARRIAGE RETURN>
4.3.4.6 THE PROGRAM WILL TYPE R TO INDICATE THAT IT HAS STARTED
AND WILL START TESTING AT THE SELECTED TEST.

NOTE: CARE MUST BE TAKEN WHEN THS FEATURE IS USED, SINCE
THERE IS NO PROTECTION AGAINST SELECTING AN ADDRESS THAT
IS IN THE MIDDLE OF A TEST

NOTE: IF IT IS DESIRED TO LOOP ON THE TEST THAT IS SELECTED
SET SW14=1 BEFORE ENTERING THE TEST ADDRESS

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                        5.      OPERATING PROCEDURE

                        5.1     OPERATIONAL SWITCH SETTINGS

                                SW15=1, HALT ON ERROR
                                SW14=1, LOOP ON CURRENT TEST
                                SW13=1, SUPPRESS ERROR TYPEOUT
                                SW11=1, INHIBIT ITERATIONS
                                SW10=1, ESCAPE TO NEXT TEST ON ERROR
                                SW09=1, FREEZE VARIABLE PARAMETER IN CURRENT TEST
                                SW01=1, START PROGRAM AT SELECTED TEST
                                SW00=1, CHANGE PARAMETERS AT PROGRAM RESTART

                        5.2     SUBROUTINE ABSTRACTS

                        5.2.1   TRAPCATCHER (LOCATIONS 000000-000776)

                                THIS ROUTINE IS USED TO INTERCEPT UNEXPECTED INTERRUPTS
                                AND TRAPS.  THE AREA FROM 000000-000776 IS LOADED
                                WITH THE FOLLOWING SEQUENCE

                                        002
                                        0
                                        ...
                                        772
                                        0
                                        776
                                        0

                                IF AN UNEXPECTED INTERRUPT OR TRAP OCCURS, THE PROGRAM
                                WILL HALT WITH THE PC 2 GREATER THAN THE ADDRESS TO
                                WHICH THE PROGRAM TRAPPED.  THE PROCESSOR STACK MAY
                                BE EXAMINED TO DETERMINE WHERE THE PROGRAM WAS WHEN THE
                                TRAP OR INTERRUPT OCCURED.

                        5.2.2   START   (PROGRAM INITIALIZATION)

                                THIS ROUTINE INITIALIZES ALL PROGRAM FLAGS AND COUNTERS,
                                TYPES THE PROGRAM TITLE MESSAGE, AND INPUTS THE VECTOR
                                AND CONTROL REGISTER ADDRESSES OF THE DH11 TO BE TESTED.

                        5.2.3   BEGIN   (PROGRAM START AND RESTART)

                                THIS ROUTINE IS ENTERED IMMEDIATLY AFTER "START"
                                AND EACH TIME A PROGRAM PASS HAS BEEN COMPLETED.
                                THE ROUTINE SETS UP THE PROCESSOR STACK AND STATUS WORD
                                AND THEN TRANSFERS CONTROL TO THE TEST AT WHICH
                                TESTING WILL BEGIN.  IF SW01=0 WHEN THIS ROUTINE IS ENTERD
                                TESTING WILL START AT T1 (TEST 1).  IF SW01=1 WHEN
                                THIS ROUTINE IS ENTERED, TESTING WILL START AT THE PC
                                ENTERED FROM THE TELETYPE KEYBOARD.
```

5.2.4 EOP (END OF PASS)

THIS ROUTINE IS ENTERED ONCE PER PASS AFTER ALL TESTS HAVE BEEN COMPLETED. THIS ROUTINE TYPES THE MAINDEC IDENTIFICATION CODE OF THE PROGRAM, CLEARS ERROR FLAGS AND UPDATES THE PASS COUNT. IF THE PROGRAM WAS LOADED UNDER ACT11 OR DDP, THE ROUTINE CHECKS FOR RETURN TO THE ACT11 OR DDP MONITOR. IF THE PROGRAM IS NOT UNDER MONITOR CONTROL, THE ROUTINE TRANSFERS TO BEGIN.

5.2.5 SCOPER (SCOPE LOOP AND ITERATION HANDLER)

THIS ROUTINE IS ENTERED EACH TIME A TEST IS COMPLETED. THE ROUTINE CHECKS FOR THE FOLLOWING UPON ENTRY

A) IF SW10=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE, AFTER CLEARING ERROR FLAGS.
B) IF SW11=1, THE ROUTINE WILL TRANSFER TO THE NEXT TEST SEQUENCE, AFTER CLEARING ERROR FLAGS.
C) IF SW14=1, THE ROUTINE WILL LOOP ON THE CURRENT TEST REGARDLESS OF THE ITERATION COUNT.

IF NONE OF THE ABOVE IS TRUE, THE ROUTINE WILL ADD 1 TO THE COUNT OF TEST ITERATIONS, AND COMPARE THIS VALUE TO THE NUMBER OF ITERATIONS THAT SHOULD BE PERFORMED. IF THESE NUMBERS ARE EQUAL, THE ROUTINE WILL TRANSFER TO THE NEXT TEST IN SEQUENCE. THE THE NUMBERS ARE NOT EQUAL, THE TEST CURRENTLY IN PROGRESS WILL BE REPEATED.

5.2.6 SCOP1R (FREEZE ON CURRENT DATA)

THE CALL TO THIS ROUTINE FOLLOWS IMMEDIATLY AFTER THE THE CALL TO THE ERROR HANDLER IN THOSE TESTS THAT HAVE VARIABLE PARAMETERS. THIS ROUTINE IS ALWAYS ENTERED IN THOSE TESTS, WHETHER OR NOT AN ERROR OCCURS.
IF SW09=1, THE ROUTINE WILL TRANSFER CONTROL BACK TO THE TEST AT A POINT WHICH WILL ALLOW REPEATING THE FUNCTION UNDER TEST CONTINUOUSLY WITH THE SAME DATA. IF THIS OPTION IS SELECTED, THE ROUTINE "SCOPER" IS NEVER ENTERED AND ITERATION COUNTS WILL NOT BE UPDATED.

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277
278                                5.2.7   ERRORS  (ERROR HANDLER)
279
280                                        THIS ROUTINE IS ENTERED UPON ERROR DETECTION ONLY.
281                                        WITH ALL CONSOLE SWITCHES DOWN, THE ROUTINE PROCEDES AS FOLLOWS:
282                                        A) THE PC OF THE INSTRUCTION THAT CALLED THE ERROR HANDLER
283                                           IS ACCESSED THRU THE STACK, AND THEN THE EMT INSTRUCTION
284                                           ITSELF IS FETCHED.  THE 8 LSB OF THE EMT
285                                           INSTRUCTION ARE THE ERROR CODE.  THIS CODE IS
286                                           USED TO ACCESS A TABLE OF ERROR MESSAGES AND ERROR
287                                           DATA STORAGE LOCATIONS.
288                                        B) IF THE TEST THAT FAILED DID NOT FAIL PREVIOUSLY
289                                           DURING THIS PASS,  A COMPLETE ERROR REPORT IS MADE
290                                           IF THE TEST THAT FAILED FAILED MOR THAT ONCE DURING
291                                           THE CURRENT PASS, ONLY THE DATA RELATING TO THE FAILUER
292                                           IS TYPED.  IF SW13=1, NO ERROR TYPEOUT IS MADE.
293                                        C) THE ROUTINE NOW CHECKS FOR HALT ON ERROR.  IF SW15=1
294                                           THE PROGRAM WILL HALT WITH THE PC OF THE CALL TO
295                                           THE ERROR ROUTINE IN R0.  IF SW15=0, THE PROGRAM WILL
296                                           NOT HALT, BUT WILL CHECK FOR ESCAPE TO NEXT TEST.
297                                        D) IF SW10=0, THE ROUTINE WILL RETURN
298                                           TO THE TEST IN PROGRESS.  IF SW10=1, THE ROUTINE WILL
299                                           ABORT THE CURRENT TEST, AND TRANSFER TO THE NEXT
300                                           TEST IN SEQUENCE, THRU THE ROUTINE "SCOPER".
301
302                                5.2.8   TRPSRV  (TRAP DECODE AND DISPATCH)
303
304                                        THIS ROUTINE DECODES THE 8 LSB OF THE TRAP INSTRUCTION
305                                        THAT CAUSED TH PROGRAM INTERRUPT, AND TRANSFERS CONTROL
306                                        TO THE ROUTINE THRU THE TABLE "TRPTAB" USING THE 8 LSB
307                                        OF THE TRAP INSTRUCTION AS  AN OFFSET TO THE POINTER TO
308                                        THE ROUTINE TO BE ENTERED.
309
```

5.3 PROGRAM AND OR OPERATOR ACTION

5.3.1 PROGRAM START WITH ALL SWITCHES DOWN

5.3.1.1 REFER TO SECTIONS 4.3.1 AND 4.3.2 FOR INITIAL PROGRAM BEHAVIOR.

5.3.1.2 AFTER "R" HAS BEEN TYPED BY THE PROGRAM, TEST EXECUTION WILL BEGIN. EACH TEST WILL BE REPEATED A SELECTED NUMBER OF ITERATIONS (SEE LISTING FOR EXACT NUMBER FOR EACH TEST) AND THEN THE PROGRAM WILL PROCEED TO THE NEXT TEST.

5.3.1.3 WHEN ALL ITERATIONS HAVE BEEN COMPLETED, THE PROGRAM WILL TYPE "DZDHA" AND THEN RESTART TESTING AT TEST 1 (LOCATION T1 IN THE PROGRAM).

5.3.1.4 IF AN ERROR OCCURS, THE PROGRAM WILL TYPE AN APPROPRIATE ERROR MESSAGE, AND THEN CONTINUE THE TEST IN PROGRESS.

5.3.2 PROGRAM START WITH SW00=1

THE PROGRAM WILL PERFORM AS DESCRIBED IN 4.3.1 AND 5.3.1

5.3.3 PROGRAM START WITH SW01=1

5.3.3.1 REFER TO SECTION 4.3.4 FOR INITIAL PROGRAM BEHAVIOR

5.3.3.2 TEST EXECUTION WILL START AT THE ADDRESS SPECIFIED AND WILL CONTINUE AS DESCRIBED IN 5.3.1.2

5.3.3.3 AFTER "DZDHA" HAS BEEN TYPED, THE PROGRAM WILL RESUME TESTING AT TEST 1

5.3.4 PROGRAM OPERATION WITH SW15=1

SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR, THE PROGRAM WILL HALT AFTER THE ERROR TYPEOUT, AND THE PC+2 OF THE CALL TO THE ERROR ROUTINE WILL BE DISPLAYED IN R0.

5.3.5 PROGRAM OPERATION WITH SW13=1

SAME AS 5.3.1 EXCEPT THAT NO ERROR TYPEOUTS WILL OCCUR

5.3.6 PROGRAM OPERATION WITH SW11=1

SAME AS 5.3.1 EXCEPT THAT EACH TEST WILL BE REPEATED ONCE ONLY

5.3.7 PROGRAM OPERATION WITH SW10=1

SAME AS 5.3.1, EXCEPT THAT IN THE CASE OF AN ERROR THE CURRENT TEST WILL BE ABORTED, AND THE PROGRAM WILL PROCEED TO THE NEXT TEST IN SEQUENCE.

5. (CONT'D)

5.3.6 PROGRAM OPERATION WITH SW14=1, OR SW09=1

THESE FUNCTIONS ARE NORMALLY USED FOR TROUBLE SHOOTING.
SEE SECTION 6.3 FOR THEIR USE.

6. ERRORS

6.1 ERROR HALTS

THE ERROR MESSAGE FORMAT FOR ALL ERROR TYPEOUTS
IS AS FOLLOWS

```
PC+2    MESSAGE
        HEADER (IF APPLICABLE)
        DATA   (IF APPLICABLE)
```

WHERE
PC+2 IS THE ADDRESS OF THE CALL TO THE ERROR HANDLER + 2
MESSAGE IS AN ASCII MESSAGE DESCRIBING (BRIEFLY) THE FAILURE
HEADER IS A DESCRIPTION OF THE DATA TO FOLLOW
DATA IS OCTAL INFORMATION RELATING TO THE CAUSE OF THE FAILURE
IF THE SAME ERROR OCCURS IN A GIVEN TEST ON THE SAME
PASS, AND IF DATA IS ASSOCIATED WITH THAT ERROR, ONLY
DATA IS TYPE ON SUCCEEDING ERROR TYPEOUTS

IF NO DATA IS ASSOCIATED WITH THE ERROR
THE COMPLETE ERROR MESSAGE IS TYPED.

6.1.1 ERROR DESCRIPTIONS

SEE LISTING FOR DETAILS OF ERRORS

6.2 ERROR RECOVERY

6.2.1 SW15=0

IF THE PROGRAM IS RUN WITH SW15=0, NO OPERATOT ACTION IS
REQUIRED TO CONTINUE TESTING

6.2.2 SW15=1

IF THE PROGRAM IS RUN WITH SW15=1, TO CONTINUE TESTING
AFTER THE PROGRAM HAS HALTED, PRESS THE PROCESSOR
CONSOLE CONTINUE SWITCH

6.3 SCOPE LOOPING

6.3.1 TO SCOPE ON A SPECIFIC TEST, SET SW14=1 AND SW13=1
THIS WILL CAUSE THE PROGRAM TO CONTINUOUSLY LOOP ON THE
SAME TEST, AND WILL CAUSE ALL ERROR TYPEOUTS TO BE INHIBITED

6.3.2 TO SCOPE ON A SPECIFIC VALUE OF A PARAMETER WITHIN
A TEST, SET SW09=1 TO FREEZE THE DATA
(SEE LISTING FOR THOSE TESTS THAT INCORPORATE THIS FEATURE)

6. (CONT'D)

6.3.3 PROGRAM START TO SCOPE LOOP ON SELECTED TEST

PERFORM SECTION 4.3.4 WITH SW14=1

7. RESTRICTIONS

7.1 STARTING

THE DH11 TEST CARD MUST BE INSTALLED

7.2 RUNNING

NONE

8. MISCELLANEOUS

8.1 EXECUTION TIME

THE TIME FOR ONE PASS OF THE PROGRAM (END OF TYPEOUT OF DZDHA TO END OF TYPEOUT OF DZDHA) IS GIVEN FOR VARIOUS PROCESSORS IN THE TABLE BELOW

PROCESSOR	TIME
PDP-11/05,10	
PDP-11/20	
PDP-11/40	
PDP-11/45	

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                                9.      PROGRAM DESCRIPTION

                                        THIS PROGRAM IS A LOW LEVEL TEST OF DH11 CONTROL
                                        REGISTERS.

                                        THE PROGRAM BEGINS BY CHECKING THE ADDRESSABILITY OF
                                        EACH DH11 REGISTER WITHOUT CONCERN FOR ANY DATA CONTENT.
                                        THE PURPOSE OF THESE TESTS IS TO VERFIY THAT THE ADDRESS
                                        SELECTORS FOR THE VARIOUS REGISTERS ARE FUNCTIONING.

                                        THE NEXT SET OF TESTS VERIFIES THAT EACH DH11 REGISTER
                                        CAN BE MASTER CLEARED, AFTER ALL READ/WRITE BITS HAVE
                                        BEEN SET TO 1.  THIS TEST DOES NOT VERIFY THAT ALL
                                        BITS HAVE BEEN SET, ONLY THAT THEY HAVE BEEN CLEARED.

                                        THE NEXT GROUP OF TESTS EXERCISES EACH READ/WRITE BIT
                                        IN THE DH11 SYSTEM CONTROL REGISTER, IN BOTH NORMAL AND
                                        MAINTENANCE MODES OF OPERATION.  IN NORMAL MODE, EACH
                                        READ/WRITE BIT IS SET AND CLEARED, AND READ ONLY BITS
                                        ARE CHECKED FOR READ ONLY FUNCTION.

                                        IN MAINTENANCE MODE, THE BITS THAT ARE
                                        READ ONLY IN NORMAL MODE ARE CHECKED FOR READ/WRITE OPERATION.

                                        THE NEXT GROUP OF TESTS CHECKS EACH READ/WRITE BIT
                                        OF THE DH11 LINE PARAMATER REGISTER, BREAK CONTROL REGISTER
                                        AND SILO STATUS REGISTER FOR READ/WRITE CAPABILITY. EACH
                                        BIT OF EACH REGISTER IS CHECKED IN AN INDIVIDUAL TEST LOOP.

                                        THE FINAL GROUP OF TESTS CHECKS CLEARING OF A SINGLE
                                        BIT IN EACH OF THE LINE PARAMETER, BREAK CONTROL AND
                                        SILO STATUS REGISTERS WITH ALL OTHER READ/WRITE BITS
                                        SET TO 1.

                                        AFTER ALL TESTS HAVE BEEN COMPLETED, THE PROGRAM TYPES
                                        "DZDHA" AND RESTARTS THE SEQUENCE OF TESTING JUST DESCRIBED.

                                10.     LISTING
                                        !

                                ;DH11 STATIC LOGIC TEST
                                ;COPYRIGHT 1972,1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754

                                        ;STARTING PROCEDURE
                                        ;LOAD PROGRAM
                                        ;LOAD ADDRESS 000200
                                        ;PRESS START
                                        ;PROGRAM WILL TYPE DH11 STATIC LOGIC TEST
                                        ;PROGRAM WILL TYPE "VECTOR ADDRESS-"
                                        ;TYPE IN THE ADDRESS OF THE RECEIVER INTERRUPT VECTOR
                                        ;FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>
                                        ;PROGRAM WILL TYPE "CONTROL REGISTER ADDRESS-"
                                        ;TYPE IN THE ADDRESS OF THE SYSTEM CONTROL REGISTER
                                        ;FOR THE DH11 TO BE TESTED, FOLLOWED BY <CARRIAGE RETURN>
                                        ;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
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                                        ;AT THE END OF A PASS, PROGRAM WILL TYPE " DZDHA "
                                        ;AND THEN RESUM TESTING


                                ;SWITCH REGISTER OPTIONS

        100000                  SW15=100000             ;=1,HALT ON ERROR
        040000                  SW14=40000              ;=1,LOOP ON CURRENT TEST
        020000                  SW13=20000              ;=1,INHIBIT ERROR TYPEOUT
        010000                  SW12=10000
        004000                  SW11=4000               ;=1,INHIBIT ITERATIONS
        002000                  SW10=2000               ;=1,ESCAPE TO NEXT TEST ON ERROR
        001000                  SW09=1000               ;=1,LOOP WITH CURRENT DATA
        000400                  SW08=400
        000100                  SW06=100
        000040                  SW05=40
        000020                  SW04=20
        000010                  SW03=10
        000004                  SW02=4
        000002                  SW01=2                  ;RESTART PROGRAM AT SELECTED TEST
        000001                  SW00=1                  ;RESELECT VECTOR AND CONTROL REGISTER
                                                        ;ADDRESS AFTER PROGRAM RESTART
```

```
                                ;REGISTER DEFINITIONS

000000                          R0=%0           ;GENERAL REGISTER
000001                          R1=%1           ;GENERAL REGISTER
000002                          R2=%2           ;GENERAL REGISTER
000003                          R3=%3           ;GENERAL REGISTER
000004                          R4=%4           ;GENERAL REGISTER
000005                          R5=%5           ;GENERAL REGISTER
000006                          SP=%6           ;PROCESSOR STACK POINTER
000007                          PC=%7           ;PROGRAM COUNTER

                                ;LOCATION EQUIVALENCIES

177570                          SWR=177570      ;CONSOLE SWITCH REGISTER
177570                          LIGHTS=177570   ;PDP-11/45 DISPLAY REGISTER
177776                          PS=177776       ;PROCESSOR STATUS WORD
021106                          STACK=ENDCOD+200;START OF PROCESSOR STACK

                                ;INSTRUCTION DEFINITIONS

005746                          PUSH1SP=5746    ;DECREMENT PROCESSOR STACK 1 WORD
005726                          POP1SP=5726     ;INCREMENT PROCESSOR STACK 1 WORD
010046                          PUSHR0=10046    ;SAVE R0 ON STACK
012600                          POPR0=12600     ;RESTORE R0 FROM STACK
024646                          PUSH2SP=24646   ;DECREMENT STACK TWICE
022626                          POP2SP=22626    ;INCREMENT STACK TWICE
                                .EQUIV  EMT,HLT ;BASIC DEFINITION OF ERROR CALL


100000                          BIT15=100000
040000                          BIT14=40000
020000                          BIT13=20000
010000                          BIT12=10000
004000                          BIT11=4000
002000                          BIT10=2000
001000                          BIT09=1000
000400                          BIT08=400
000200                          BIT07=200
000100                          BIT06=100
000040                          BIT05=40
000020                          BIT04=20
000010                          BIT03=10
000004                          BIT02=4
000002                          BIT01=2
000001                          BIT00=1
```

```
                                ;TRAPCATCAER FOR ILLEGAL INTERRUPTS
                        .=0
000000  000002          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000002  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000004  000006          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000006  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000010  000012          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000012  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000014  000016          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000016  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000020  000022          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000022  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000024  000026          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000026  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000030  000032          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000032  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000034  000036          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000036  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000040  000042          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000042  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000044  000046          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000046  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000050  000052          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000052  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000054  000056          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000056  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000060  000062          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000062  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000064  000066          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000066  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000070  000072          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000072  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000074  000076          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000076  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000100  000102          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000102  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000104  000106          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000106  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000110  000112          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000112  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000114  000116          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000116  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000120  000122          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000122  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000124  000126          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000126  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000130  000132          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000132  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000134  000136          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000136  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000140  000142          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000142  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000144  000146          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000146  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
000150  000152          .+2             ;UNEXPECTED TRAP TO THIS LOCATION
000152  000000          HALT            ;EXAMINE STACK TO FIND CAUSE
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   637  000154  000156                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   638  000156  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   639  000160  000162                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   640  000162  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   641  000164  000166                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   642  000166  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   643  000170  000172                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   644  000172  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   645  000174  000176                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   646  000176  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   647  000200  000202                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   648  000202  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   649  000204  000206                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   650  000206  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   651  000210  000212                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   652  000212  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   653  000214  000216                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   654  000216  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   655  000220  000222                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   656  000222  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   657  000224  000226                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   658  000226  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   659  000230  000232                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   660  000232  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   661  000234  000236                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   662  000236  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   663  000240  000242                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   664  000242  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   665  000244  000246                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   666  000246  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   667  000250  000252                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   668  000252  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   669  000254  000256                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   670  000256  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   671  000260  000262                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   672  000262  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   673  000264  000266                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   674  000266  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   675  000270  000272                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   676  000272  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   677  000274  000276                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   678  000276  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   679  000300  000302                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   680  000302  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   681  000304  000306                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   682  000306  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   683  000310  000312                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   684  000312  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   685  000314  000316                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   686  000316  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   687  000320  000322                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   688  000322  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   689  000324  000326                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   690  000326  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
   691  000330  000332                    .+2          ;UNEXPECTED TRAP TO THIS LOCATION
   692  000332  000000                    HALT         ;EXAMINE STACK TO FIND CAUSE
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693  000334  000336                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
694  000336  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
695  000340  000342                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
696  000342  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
697  000344  000346                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
698  000346  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
699  000350  000352                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
700  000352  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
701  000354  000356                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
702  000356  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
703  000360  000362                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
704  000362  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
705  000364  000366                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
706  000366  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
707  000370  000372                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
708  000372  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
709  000374  000376                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
710  000376  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
711  000400  000402                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
712  000402  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
713  000404  000406                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
714  000406  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
715  000410  000412                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
716  000412  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
717  000414  000416                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
718  000416  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
719  000420  000422                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
720  000422  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
721  000424  000426                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
722  000426  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
723  000430  000432                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
724  000432  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
725  000434  000436                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
726  000436  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
727  000440  000442                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
728  000442  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
729  000444  000446                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
730  000446  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
731  000450  000452                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
732  000452  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
733  000454  000456                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
734  000456  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
735  000460  000462                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
736  000462  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
737  000464  000466                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
738  000466  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
739  000470  000472                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
740  000472  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
741  000474  000476                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
742  000476  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
743  000500  000502                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
744  000502  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
745  000504  000506                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
746  000506  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
747  000510  000512                    .+2     ;UNEXPECTED TRAP TO THIS LOCATION
748  000512  000000                    HALT    ;EXAMINE STACK TO FIND CAUSE
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749  000514  000516                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
750  000516  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
751  000520  000522                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
752  000522  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
753  000524  000526                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
754  000526  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
755  000530  000532                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
756  000532  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
757  000534  000536                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
758  000536  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
759  000540  000542                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
760  000542  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
761  000544  000546                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
762  000546  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
763  000550  000552                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
764  000552  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
765  000554  000556                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
766  000556  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
767  000560  000562                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
768  000562  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
769  000564  000566                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
770  000566  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
771  000570  000572                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
772  000572  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
773  000574  000576                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
774  000576  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
775  000600  000602                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
776  000602  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
777  000604  000606                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
778  000606  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
779  000610  000612                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
780  000612  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
781  000614  000616                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
782  000616  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
783  000620  000622                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
784  000622  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
785  000624  000626                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
786  000626  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
787  000630  000632                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
788  000632  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
789  000634  000636                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
790  000636  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
791  000640  000642                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
792  000642  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
793  000644  000646                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
794  000646  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
795  000650  000652                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
796  000652  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
797  000654  000656                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
798  000656  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
799  000660  000662                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
800  000662  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
801  000664  000666                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
802  000666  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
803  000670  000672                    .+2         ;UNEXPECTED TRAP TO THIS LOCATION
804  000672  000000                    HALT        ;EXAMINE STACK TO FIND CAUSE
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  805  000674  000676                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  806  000676  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  807  000700  000702                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  808  000702  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  809  000704  000706                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  810  000706  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  811  000710  000712                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  812  000712  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  813  000714  000716                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  814  000716  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  815  000720  000722                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  816  000722  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  817  000724  000726                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  818  000726  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  819  000730  000732                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  820  000732  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  821  000734  000736                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  822  000736  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  823  000740  000742                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  824  000742  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  825  000744  000746                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  826  000746  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  827  000750  000752                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  828  000752  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  829  000754  000756                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  830  000756  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  831  000760  000762                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  832  000762  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  833  000764  000766                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  834  000766  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  835  000770  000772                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  836  000772  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
  837  000774  000776                    .+2             ;UNEXPECTED TRAP TO THIS LOCATION
  838  000776  000000                    HALT            ;EXAMINE STACK TO FIND CAUSE
```

```
                                        ;STANDARD INTERRUPT VECTORS


                    000024          .=24
000024  017502                      PFAIL                   ;POWER FAIL HANDLER
000026  000340                      340                     ;SERVICE AT LEVEL 7
000030  016346                      ERRORS                  ;ERROR HANDLER
000032  000340                      340                     ;SERVICE AT LEVEL 7
000034  016550                      TRPSRV                  ;GENERAL HANDLER DISPATCH SERVICE
000036  000340                      340                     ;SERVICE AT LEVEL 7
                    000200          .=200
000200  000167  000574              JMP     START           ;GO TO START OF PROGRAM


                                        ;DEFINITIONS FOR TRAP SUBROUTINE CALLS
                                        ;POINTERS TO SUBROUTINES CAN BE FOUND STARTING
                                        ;AT LOCATION "TRPTAB"

                    104400              SCOPE=TRAP+Y            ;SCOPE LOOP AND ITERATION HANDLER
                    104401              TYPE=TRAP+Y             ;TELETYPE OUTPUT ROUTINE
                    104402              OCTASC=TRAP+Y           ;OCTAL TO ASCII CONVERSION
                    104403              INSTR=TRAP+Y            ;INPUT ASCII STRING
                    104404              INSTER=TRAP+Y           ;STRING INPUT ERROR
                    104405              PARAM=TRAP+Y            ;CONVERT STRING TO OCTAL, CHECK LIMITS
                    104406              SAVDSP=TRAP+Y           ;SAVE R0-R5, PC
                    104407              RESDS=TRAP+Y            ;RESTORE R0-R5
                    104410              SCOPE1=TRAP+Y           ;CHECK FOR FREEZE ON CURRENT DATA
                    000046          .=46
000046  016214                      LOGICAL
                    000052          .=52
000052  040000                      40000
```

```
                    001000                  .=1000

                                            ;PROGRAM INITIALIZATION
                                            ;LOCK OUT INTERRUPTS
                                            ;SET UP PROCESSOR STACK
                                            ;SET UP POWER FAIL VECTOR
                                            ;CLEAR PROGRAM FLAGS AND COUNTS
                                            ;TYPE TITLE MESSAGE

001000  012767  000340  176770  START:  MOV     #340,PS         ;LOCK OUT INTERRUPTS
001006  012706  021106                  MOV     #STACK,SP       ;SET UP PROCESSOR STACK
001012  012737  017502  000024          MOV     #PFAIL,@#24     ;SET UP POWER FAIL TRAP
001020  005067  016452                  CLR     STFLG           ;CLEAR TEST START FLAG
001024  005067  016406                  CLR     PASCNT          ;CLEAR PASS COUNT
001030  005067  016404                  CLR     ERRCNT          ;CLEAR ERROR COUNT
001034  005067  016374                  CLR     ERRFLG          ;CLEAR ERROR FLAG
001040  005067  016370                  CLR     ERRFLG          ;CLEAR LAST ERROR PC
001044  104401  017646                  TYPE    ,MTITLE         ;TYPE TITLE MESSAGE
001050  005767  016420                  TST     INIFLG          ;CHECK INITIALIZATION FLAG
001054  001001                          BNE     VEC1            ;IF NOT 0, CHECK SWITCHES
                                                                ;FOR REINITIALIZATION
001056  000404                          BR      VEC2
001060  032767  000001  176502  VEC1:   BIT     #SW00,SWR       ;IF SW00=1, GET NEW VECTOR
001066  001445                          BEQ     BEGIN           ;AND CSR
001070  012701  000300          VEC2:   MOV     #300,R1
001074  012702  000302                  MOV     #302,R2
001100  012703  000004                  MOV     #4,R3
001104  010211                  1$:     MOV     R2,(R1)         ;RESTORE TRAPCATCHER
001106  005012                          CLR     (R2)            ;IN FLOATING VECTOR AREA
001110  060301                          ADD     R3,R1
001112  060302                          ADD     R3,R2
001114  020127  001000                  CMP     R1,#1000
001120  001371                          BNE     1$
001122  104403                          INSTR                   ;INPUT ADDRESS OF DEVICE VECTOR
001124  017703                          MVECTOR                 ;MESSAGE "VECTOR ADDRESS-"
001126  104405                          PARAM                   ;CONVERT STRING TO OCTAL
001130  000300                          300                     ;LOW LIMIT
001132  000770                          770                     ;HIGH  LIMIT
001134  017424                          DHRVEC                  ;LOCATIONS TO BE FILLED
001136     003                  .BYTE   3                       ;NUMBER OF LOCATIONS
001137     004                  .BYTE   4                       ;LSB MASK
001140  104403                          INSTR                   ;INPUT ADDRESS OF DEVICE CSR
001142  017725                          MREGAD                  ;MESSAGE "CONTROL REGISTER ADDRESS-"
001144  104405                          PARAM                   ;CONVERT STRING TO OCTAL
001146  000000                          0                       ;LOW LIMIT
001150  177776                          177776                  ;HIGH LIMIT
001152  017402                          DHSCR                   ;LOCATIONS TO BE FILLED
001154     007                  .BYTE   7                       ;NUMBER OF LOCATIONS
001155     010                  .BYTE   10                      ;LSB MASK
001156  016767  016236  016236          MOV     DHSSR,DHSLR     ;SET UP ADDRESS OF SILO
001164  005267  016232                  INC     DHSLR           ;STATUS REGISTER HIGH BYTE
001170  005767  016300                  TST     INIFLG          ;IF INITIALIZATION FLAG
001174  001002                          BNE     BEGIN           ;IS CLEARED
001176  005167  016272                  COM     INIFLG          ;SET IT

                                        ;PROGRAM START
```

```
                                                ;CHECK FOR PROGRAM START AT SELECTED ADDRESS

001202  012767  000340  176566  BEGIN:  MOV     #340,PS                 ;LOCK OUT INTERRUPTS
001210  012706  021106                  MOV     #STACK,SP               ;SET UP PROCESSOR STACK
001214  032767  000002  176346          BIT     #SW01,SWR               ;IF SW01=1
001222  001410                          BEQ     1$                      ;GET PC FOR PROGRAM START
001224  104403                          INSTR                           ;GET PC
001226  020071                          MTSTPC                          ;MESSAGE "TEST PC"
001230  104405                          PARAM                           ;CONVERT STRING TO OCTAL
001232  000000                          0
001234  017500                          17500
001236  000207                          RETURN
001240     001                  .BYTE   1
001241     001                  .BYTE   1
001242  000410                  BR      2$
001244  012767  001274  016170  1$:     MOV     #T1,RETURN              ;NORMAL START, TEST 1
001252  005767  016220                  TST     STFLG                   ;IF LOOPING, BYPASS TYPEOUT
001256  001004                          BNE     3$
001260  005167  016212                  COM     STFLG
001264  104401  020065          2$:     TYPE    ,MR                     ;TYPE "R" TO INDICATE START
001270  000177  016146          3$:     JMP     @RETURN                 ;START TESTING
```

```
                                        ;DH11 SYSTEM CONTROL REGISTER ADDRESSING TEST
                                        ;VERIFY THAT DH11 SYSTEM CONTROL REGISTER RESPONDS TO ADDRESSING
                                        ;IF DH11 SYSTEM CONTROL REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

001274  012767  000340  176474  T1:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001302  012767  000100  016140        MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001310  012767  001346  016126        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001316  012737  001340  000004        MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
001324  012737  000340  000006        MOV     #340,@#6
001332  005777  016044                TST     @DHSCR                  ;ADDRESS DH11 SYSTEM CONTROL
                                                                      ;REGISTER
001336  000406                        BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                      ;TO ADDRESSING
001340  016705  016036          1$:   MOV     DHSCR,R5                ;REGISTER DID NOT RESPOND
001344  104000                        HLT     0                       ;TIME OUT TRAP, DH11 SYSTEM CONTROL
                                                                      ;REGISTER DID NOT RESPOND
001346  012716  001354          2$:   MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
001352  000002                        RTI                             ;RETURN FROM TRAP
001354  012737  000006  000004  3$:   MOV     #6,@#4
001362  005037  000006                CLR     @#6                     ;RESTORE TRAP CATCHER
001366  104400                        SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;DH11 NEXT RECEIVED CHARACTER REGISTER ADDRESSING TEST
                                        ;VERIFY THAT DH11 NEXT RECEIVED CHARACTER REGISTER RESPONDS TO ADDRESSING
                                        ;IF DH11 NEXT RECEIVED CHARACTER REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

001370  012767  000340  176400  T2:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001376  012767  000100  016044        MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001404  012767  001442  016032        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001412  012737  001434  000004        MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
001420  012737  000340  000006        MOV     #340,@#6
001426  005777  015752                TST     @DHNRC                  ;ADDRESS DH11 NEXT RECEIVED CHARACTER
                                                                      ;REGISTER
001432  000406                        BR      3$                      ;NO TRAP, REGISTER RESPONDS
                                                                      ;TO ADDRESSING
001434  016705  015744          1$:   MOV     DHNRC,R5                ;REGISTER DID NOT RESPOND
001440  104000                        HLT     0                       ;TIME OUT TRAP, DH11 NEXT RECEIVED CHARACTER
                                                                      ;REGISTER DID NOT RESPOND
001442  012716  001450          2$:   MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
001446  000002                        RTI                             ;RETURN FROM TRAP
001450  012737  000006  000004  3$:   MOV     #6,@#4
001456  005037  000006                CLR     @#6                     ;RESTORE TRAP CATCHER
001462  104400                        SCOPE                           ;CHECK FOR ITERATIONS, LOOP

                                        ;DH  11 LINE PARAMETER REGISTER ADDRESSING TEST
                                        ;VERIFY THAT DH  11 LINE PARAMETER REGISTER RESPONDS TO ADDRESSING
                                        ;IF DH  11 LINE PARAMETER REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
                                        ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.

001464  012767  000340  176304  T3:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
001472  012767  000100  015750        MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
001500  012767  001536  015736        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
001506  012737  001530  000004        MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
```

```
1004  001514  012737  000340  000006          MOV     #340,@#6
1005  001522  005777  015660                  TST     @DHLPR                  ;ADDRESS DH  11 LINE PARAMETER
1006                                                                          ;REGISTER
1007  001526  000406                          BR      3$                      ;NO TRAP, REGISTER RESPONDS
1008                                                                          ;TO ADDRESSING
1009  001530  016705  015652          1$:     MOV     DHLPR,R5                ;REGISTER DID NOT RESPOND
1010  001534  104000                          HLT     0                       ;TIME OUT TRAP, DH  11 LINE PARAMETER
1011                                                                          ;REGISTER DID NOT RESPOND
1012  001536  012716  001544          2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
1013  001542  000002                          RTI                             ;RETURN FROM TRAP
1014  001544  012737  000006  000004  3$:     MOV     #6,@#4
1015  001552  005037  000006                  CLR     @#6                     ;RESTORE TRAP CATCHER
1016  001556  104400                          SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1017
1018                                          ;DH11 BUS ADDRESS REGISTER ADDRESSING TEST
1019                                          ;VERIFY THAT DH11 BUS ADDRESS REGISTER RESPONDS TO ADDRESSING
1020                                          ;IF DH11 BUS ADDRESS REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
1021                                          ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.
1022
1023  001560  012767  000340  176210  T4:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1024  001566  012767  000100  015654          MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
1025  001574  012767  001632  015642          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1026  001602  012737  001624  000004          MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
1027  001610  012737  000340  000006          MOV     #340,@#6
1028  001616  005777  015566                  TST     @DHBA                   ;ADDRESS DH11 BUS ADDRESS
1029                                                                          ;REGISTER
1030  001622  000406                          BR      3$                      ;NO TRAP, REGISTER RESPONDS
1031                                                                          ;TO ADDRESSING
1032  001624  016705  015560          1$:     MOV     DHBA,R5         ;REGISTER DID NOT RESPOND
1033  001630  104000                          HLT     0                       ;TIME OUT TRAP, DH11 BUS ADDRESS
1034                                                                          ;REGISTER DID NOT RESPOND
1035  001632  012716  001640          2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
1036  001636  000002                          RTI                             ;RETURN FROM TRAP
1037  001640  012737  000006  000004  3$:     MOV     #6,@#4
1038  001646  005037  000006                  CLR     @#6                     ;RESTORE TRAP CATCHER
1039  001652  104400                          SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1040
1041                                          ;DH11 BYTE COUNT REGISTER ADDRESSING TEST
1042                                          ;VERIFY THAT DH11 BYTE COUNT REGISTER RESPONDS TO ADDRESSING
1043                                          ;IF DH11 BYTE COUNT REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
1044                                          ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.
1045
1046  001654  012767  000340  176114  T5:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1047  001662  012767  000100  015560          MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
1048  001670  012767  001726  015546          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1049  001676  012737  001720  000004          MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
1050  001704  012737  000340  000006          MOV     #340,@#6
1051  001712  005777  015474                  TST     @DHBC                   ;ADDRESS DH11 BYTE COUNT
1052                                                                          ;REGISTER
1053  001716  000406                          BR      3$                      ;NO TRAP, REGISTER RESPONDS
1054                                                                          ;TO ADDRESSING
1055  001720  016705  015466          1$:     MOV     DHBC,R5         ;REGISTER DID NOT RESPOND
1056  001724  104000                          HLT     0                       ;TIME OUT TRAP, DH11 BYTE COUNT
1057                                                                          ;REGISTER DID NOT RESPOND
1058  001726  012716  001734          2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
1059  001732  000002                          RTI                             ;RETURN FROM TRAP
```

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1060  001734  012737  000006  000004  3$:     MOV     #6,@#4
1061  001742  005037  000006                  CLR     @#6                     ;RESTORE TRAP CATCHER
1062  001746  104400                          SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1063
1064                                          ;DH11 BREAK CONTROL REGISTER ADDRESSING TEST
1065                                          ;VERIFY THAT DH11 BREAK CONTROL REGISTER RESPONDS TO ADDRESSING
1066                                          ;IF DH11 BREAK CONTROL REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
1067                                          ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.
1068
1069  001750  012767  000340  176020  T6:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1070  001756  012767  000100  015464          MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
1071  001764  012767  002022  015452          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1072  001772  012737  002014  000004          MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
1073  002000  012737  000340  000006          MOV     #340,@#6
1074  002006  005777  015404                  TST     @DHBCR                  ;ADDRESS DH11 BREAK CONTROL
1075                                                                          ;REGISTER
1076  002012  000406                          BR      3$                      ;NO TRAP, REGISTER RESPONDS
1077                                                                          ;TO ADDRESSING
1078  002014  016705  015376          1$:     MOV     DHBCR,R5                ;REGISTER DID NOT RESPOND
1079  002020  104000                          HLT     0                       ;TIME OUT TRAP, DH11 BREAK CONTROL
1080                                                                          ;REGISTER DID NOT RESPOND
1081  002022  012716  002030          2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
1082  002026  000002                          RTI                             ;RETURN FROM TRAP
1083  002030  012737  000006  000004  3$:     MOV     #6,@#4
1084  002036  005037  000006                  CLR     @#6                     ;RESTORE TRAP CATCHER
1085  002042  104400                          SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1086
1087                                          ;BUS ACTIVE REGISTER ADDRESSING TEST
1088                                          ;VERIFY THAT BUS ACTIVE REGISTER RESPONDS TO ADDRESSING
1089                                          ;IF BUS ACTIVE REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
1090                                          ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.
1091
1092  002044  012767  000340  175724  T7:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1093  002052  012767  000100  015370          MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
1094  002060  012767  002116  015356          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1095  002066  012737  002110  000004          MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
1096  002074  012737  000340  000006          MOV     #340,@#6
1097  002102  005777  015306                  TST     @DHBAR                  ;ADDRESS BUS ACTIVE
1098                                                                          ;REGISTER
1099  002106  000406                          BR      3$                      ;NO TRAP, REGISTER RESPONDS
1100                                                                          ;TO ADDRESSING
1101  002110  016705  015300          1$:     MOV     DHBAR,R5                ;REGISTER DID NOT RESPOND
1102  002114  104000                          HLT     0                       ;TIME OUT TRAP, BUS ACTIVE
1103                                                                          ;REGISTER DID NOT RESPOND
1104  002116  012716  002124          2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
1105  002122  000002                          RTI                             ;RETURN FROM TRAP
1106  002124  012737  000006  000004  3$:     MOV     #6,@#4
1107  002132  005037  000006                  CLR     @#6                     ;RESTORE TRAP CATCHER
1108  002136  104400                          SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1109
1110                                          ;SILO STATUS REGISTER ADDRESSING TEST
1111                                          ;VERIFY THAT SILO STATUS REGISTER RESPONDS TO ADDRESSING
1112                                          ;IF SILO STATUS REGISTER DOES NOT RESPOND, A BUSS ERROR TRAP
1113                                          ;WILL OCCUR, AND AN ERROR MESSAGE WILL BE TYPED.
1114
1115  002140  012767  000340  175630  T10:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
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1116  002146  012767  000100  015274          MOV     #100,ICOUNT             ;SET UP FOR 100 ITERATIONS
1117  002154  012767  002212  015262          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1118  002162  012737  002204  000004          MOV     #1$,@#4                 ;SET UP TIME OUT TRAP
1119  002170  012737  000340  000006          MOV     #340,@#6
1120  002176  005777  015216                  TST     @DHSSR                  ;ADDRESS SILO STATUS
1121                                                                                  ;REGISTER
1122  002202  000406                          BR      3$                      ;NO TRAP, REGISTER RESPONDS
1123                                                                          ;TO ADDRESSING
1124  002204  016705  015210          1$:     MOV     DHSSR,R5                ;REGISTER DID NOT RESPOND
1125  002210  104000                          HLT     0                       ;TIME OUT TRAP, SILO STATUS
1126                                                                          ;REGISTER DID NOT RESPOND
1127  002212  012716  002220          2$:     MOV     #3$,(SP)                ;SET UP TO RETURN FROM TRAP
1128  002216  000002                          RTI                             ;RETURN FROM TRAP
1129  002220  012737  000006  000004  3$:     MOV     #6,@#4
1130  002226  005037  000006                  CLR     @#6                     ;RESTORE TRAP CATCHER
1131  002232  104400                          SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1132
1133
1134                                  ;MASTER CLEAR TEST
1135                                  ;SET SYSTEM CONTROL REGISTER TO 'CDATA'
1136                                  ;ISSUE MASTER CLEAR
1137                                  ;VERIFY THAT SYSTEM CONTROL WAS CLEARED
1138
1139  002234  012767  000340  175534  T11:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1140  002242  012767  004000  015200          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1141  002250  012767  002312  015166          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1142  002256  012777  173777  015116          MOV     #173777,@DHSCR          ;SET SYSTEM CONTROL REGISTER
1143                                                                          ;TO 173777
1144  002264  052777  004000  015110          BIS     #BIT11,@DHSCR           ;ISSUE MASTER CLEAR
1145  002272  017704  015104                  MOV     @DHSCR,R4               ;(R4)=ACTUAL DATA IN
1146                                                                          ;SYSTEM CONTROL REGISTER
1147  002276  005704                          TST     R4                              ;VERIFY THAT SYSTEM CONTROL REGISTER
1148                                                                          ;WAS CLEARED
1149  002300  001404                          BEQ     1$
1150  002302  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
1151                                                                          ;SYSTEM CONTROL REGISTER, 0
1152  002304  016703  015072                  MOV     DHSCR,R3                        ;GET REGISTER ADDRESS
1153  002310  104005                          HLT     5                       ;MASTER CLEAR FAILED
1154  002312  104400          1$:     SCOPE                                   ;CHECK FOR ITERATIONS, LOOP
1155
1156                                  ;MASTER CLEAR TEST
1157                                  ;SET LINE PARAMETER REGISTER TO 'CDATA'
1158                                  ;ISSUE MASTER CLEAR
1159                                  ;VERIFY THAT LINE PARAMETER WAS CLEARED
1160
1161  002314  012767  000340  175454  T12:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1162  002322  012767  004000  015120          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1163  002330  012767  002372  015106          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1164  002336  012777  177777  015042          MOV     #177777,@DHLPR          ;SET LINE PARAMETER REGISTER
1165                                                                          ;TO 177777
1166  002344  052777  004000  015030          BIS     #BIT11,@DHSCR           ;ISSUE MASTER CLEAR
1167  002352  017704  015030                  MOV     @DHLPR,R4               ;(R4)=ACTUAL DATA IN
1168                                                                          ;LINE PARAMETER REGISTER
1169  002356  005704                          TST     R4                              ;VERIFY THAT LINE PARAMETER REGISTER
1170                                                                          ;WAS CLEARED
1171  002360  001404                          BEQ     1$
```

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1172  002362  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
1173                                                                          ;LINE PARAMETER REGISTER, 0
1174  002364  016703  015016                  MOV     DHLPR,R3                        ;GET REGISTER ADDRESS
1175  002370  104005                          HLT     5                       ;MASTER CLEAR FAILED
1176  002372  104400                  1$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1177
1178                                          ;MASTER CLEAR TEST
1179                                          ;SET BREAK CONTROL REGISTER TO 'CDATA'
1180                                          ;ISSUE MASTER CLEAR
1181                                          ;VERIFY THAT BREAK CONTROL WAS CLEARED
1182
1183  002374  012767  000340  175374  T13:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1184  002402  012767  004000  015040          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1185  002410  012767  002452  015026          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1186  002416  012777  177777  014772          MOV     #177777,@DHBCR          ;SET BREAK CONTROL REGISTER
1187                                                                          ;TO 177777
1188  002424  052777  004000  014750          BIS     #BIT11,@DHSCR           ;ISSUE MASTER CLEAR
1189  002432  017704  014760                  MOV     @DHBCR,R4               ;(R4)=ACTUAL DATA IN
1190                                                                          ;BREAK CONTROL REGISTER
1191  002436  005704                          TST     R4                              ;VERIFY THAT BREAK CONTROL REGISTER
1192                                                                          ;WAS CLEARED
1193  002440  001404                          BEQ     1$
1194  002442  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
1195                                                                          ;BREAK CONTROL REGISTER, 0
1196  002444  016703  014746                  MOV     DHBCR,R3                        ;GET REGISTER ADDRESS
1197  002450  104005                          HLT     5                       ;MASTER CLEAR FAILED
1198  002452  104400                  1$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1199
1200                                          ;MASTER CLEAR TEST
1201                                          ;SET SILO STATUS REGISTER TO 'CDATA'
1202                                          ;ISSUE MASTER CLEAR
1203                                          ;VERIFY THAT SILO STATUS WAS CLEARED
1204
1205  002454  012767  000340  175314  T14:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1206  002462  012767  004000  014760          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1207  002470  012767  002536  014746          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1208  002476  012777  100077  014714          MOV     #100077,@DHSSR          ;SET SILO STATUS REGISTER
1209                                                                          ;TO 100077
1210  002504  052777  004000  014670          BIS     #BIT11,@DHSCR           ;ISSUE MASTER CLEAR
1211  002512  017704  014702                  MOV     @DHSSR,R4               ;(R4)=ACTUAL DATA IN
1212                                                                          ;SILO STATUS REGISTER
1213  002516  042704  077700                  BIC     #77700,R4                       ;CLEAR UNWANTED BITS
1214  002522  005704                          TST     R4                              ;VERIFY THAT SILO STATUS REGISTER
1215                                                                          ;WAS CLEARED
1216  002524  001404                          BEQ     1$
1217  002526  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
1218                                                                          ;SILO STATUS REGISTER, 0
1219  002530  016703  014664                  MOV     DHSSR,R3                        ;GET REGISTER ADDRESS
1220  002534  104005                          HLT     5                       ;MASTER CLEAR FAILED
1221  002536  104400                  1$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1222
1223                                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1224                                          ;SET LINE SELECT BIT 0 IN SYSTEM CONTROL REGISTER
1225                                          ;VERIFY THAT LINE SELECT BIT 0 WAS SET
1226                                          ;CLEAR LINE SELECT BIT 0
1227                                          ;VERITY THAT LINE SELECT BIT 0 WAS CLEARED
```

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1228
1229  002540  012767  000340  175230  T15:  MOV   #340,PS          ;DISABLE ALL INTERRUPTS
1230  002546  012767  004000  014674        MOV   #4000,ICOUNT     ;SET UP FOR 4000 ITERATIONS
1231  002554  012767  002624  014662        MOV   #2$,ESCAPE       ;SET UP TO ESCAPE TO NEXT TEST
1232  002562  016703  014614               MOV   DHSCR,R3         ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1233  002566  012713  000001               MOV   #BIT00,(R3)      ;SET LINE SELECT BIT 0
1234  002572  022713  000001               CMP   #BIT00,(R3)      ;VERIFY THAT LINE SELECT BIT 0 WAS SET
1235  002576  001404                        BEQ   1$
1236  002600  012705  000001               MOV   #BIT00,R5        ;(R5)= EXPECTED VALUE
1237                                                              ;IN SYSTEM CONTROL REGISTER
1238                                                              ;LINE SELECT BIT 0
1239  002604  011304                        MOV   (R3),R4          ;(R4)=ACTUAL DATA IN
1240                                                              ;SYSTEM CONTROL REGISTER
1241  002606  104001                        HLT   1                ;SYSTEM CONTROL REGISTER
1242                                                              ;WRITE/READ ERROR
1243  002610  042713  000001        1$:   BIC   #BIT00,(R3)      ;CLEAR LINE SELECT BIT 0
1244  002614  001403                        BEQ   2$
1245  002616  005005                        CLR   R5               ;(R5)=EXPECTED DATA IN
1246                                                              ;SYSTEM CONTROL REGISTER, 0
1247  002620  011304                        MOV   (R3),R4          ;(R4)=ACTUAL DATA IN
1248                                                              ;SYSTEM CONTROL REGISTER
1249  002622  104001                        HLT   1                ;SYSTEM CONTROL REGISTER
1250                                                              ;WRITE/READ ERROR
1251  002624  104400                  2$:   SCOPE                  ;CHECK FOR ITERATIONS, LOOP
1252
1253                                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1254                                        ;SET LINE SELECT BIT 1 IN SYSTEM CONTROL REGISTER
1255                                        ;VERIFY THAT LINE SELECT BIT 1 WAS SET
1256                                        ;CLEAR LINE SELECT BIT 1
1257                                        ;VERITY THAT LINE SELECT BIT 1 WAS CLEARED
1258
1259  002626  012767  000340  175142  T16:  MOV   #340,PS          ;DISABLE ALL INTERRUPTS
1260  002634  012767  004000  014606        MOV   #4000,ICOUNT     ;SET UP FOR 4000 ITERATIONS
1261  002642  012767  002712  014574        MOV   #2$,ESCAPE       ;SET UP TO ESCAPE TO NEXT TEST
1262  002650  016703  014526               MOV   DHSCR,R3         ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1263  002654  012713  000002               MOV   #BIT01,(R3)      ;SET LINE SELECT BIT 1
1264  002660  022713  000002               CMP   #BIT01,(R3)      ;VERIFY THAT LINE SELECT BIT 1 WAS SET
1265  002664  001404                        BEQ   1$
1266  002666  012705  000002               MOV   #BIT01,R5        ;(R5)= EXPECTED VALUE
1267                                                              ;IN SYSTEM CONTROL REGISTER
1268                                                              ;LINE SELECT BIT 1
1269  002672  011304                        MOV   (R3),R4          ;(R4)=ACTUAL DATA IN
1270                                                              ;SYSTEM CONTROL REGISTER
1271  002674  104001                        HLT   1                ;SYSTEM CONTROL REGISTER
1272                                                              ;WRITE/READ ERROR
1273  002676  042713  000002        1$:   BIC   #BIT01,(R3)      ;CLEAR LINE SELECT BIT 1
1274  002702  001403                        BEQ   2$
1275  002704  005005                        CLR   R5               ;(R5)=EXPECTED DATA IN
1276                                                              ;SYSTEM CONTROL REGISTER, 0
1277  002706  011304                        MOV   (R3),R4          ;(R4)=ACTUAL DATA IN
1278                                                              ;SYSTEM CONTROL REGISTER
1279  002710  104001                        HLT   1                ;SYSTEM CONTROL REGISTER
1280                                                              ;WRITE/READ ERROR
1281  002712  104400                  2$:   SCOPE                  ;CHECK FOR ITERATIONS, LOOP
1282
1283                                        ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
```

```
1284                                            ;SET LINE SELECT BIT 2 IN SYSTEM CONTROL REGISTER
1285                                            ;VERIFY THAT LINE SELECT BIT 2 WAS SET
1286                                            ;CLEAR LINE SELECT BIT 2
1287                                            ;VERITY THAT LINE SELECT BIT 2 WAS CLEARED
1288
1289  002714  012767  000340  175054  T17:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1290  002722  012767  004000  014520          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1291  002730  012767  003000  014506          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1292  002736  016703  014440                  MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1293  002742  012713  000004                  MOV     #BIT02,(R3)             ;SET LINE SELECT BIT 2
1294  002746  022713  000004                  CMP     #BIT02,(R3)             ;VERIFY THAT LINE SELECT BIT 2 WAS SET
1295  002752  001404                          BEQ     1$
1296  002754  012705  000004                  MOV     #BIT02,R5               ;(R5)= EXPECTED VALUE
1297                                                                           ;IN SYSTEM CONTROL REGISTER
1298                                                                           ;LINE SELECT BIT 2
1299  002760  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1300                                                                           ;SYSTEM CONTROL REGISTER
1301  002762  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1302                                                                           ;WRITE/READ ERROR
1303  002764  042713  000004          1$:     BIC     #BIT02,(R3)             ;CLEAR LINE SELECT BIT 2
1304  002770  001403                          BEQ     2$
1305  002772  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
1306                                                                           ;SYSTEM CONTROL REGISTER, 0
1307  002774  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1308                                                                           ;SYSTEM CONTROL REGISTER
1309  002776  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1310                                                                           ;WRITE/READ ERROR
1311  003000  104400                  2$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1312
1313                                            ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1314                                            ;SET LINE SELECT BIT 3 IN SYSTEM CONTROL REGISTER
1315                                            ;VERIFY THAT LINE SELECT BIT 3 WAS SET
1316                                            ;CLEAR LINE SELECT BIT 3
1317                                            ;VERITY THAT LINE SELECT BIT 3 WAS CLEARED
1318
1319  003002  012767  000340  174766  T20:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1320  003010  012767  004000  014432          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1321  003016  012767  003066  014420          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1322  003024  016703  014352                  MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1323  003030  012713  000010                  MOV     #BIT03,(R3)             ;SET LINE SELECT BIT 3
1324  003034  022713  000010                  CMP     #BIT03,(R3)             ;VERIFY THAT LINE SELECT BIT 3 WAS SET
1325  003040  001404                          BEQ     1$
1326  003042  012705  000010                  MOV     #BIT03,R5               ;(R5)= EXPECTED VALUE
1327                                                                           ;IN SYSTEM CONTROL REGISTER
1328                                                                           ;LINE SELECT BIT 3
1329  003046  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1330                                                                           ;SYSTEM CONTROL REGISTER
1331  003050  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1332                                                                           ;WRITE/READ ERROR
1333  003052  042713  000010          1$:     BIC     #BIT03,(R3)             ;CLEAR LINE SELECT BIT 3
1334  003056  001403                          BEQ     2$
1335  003060  005005                          CLR     R5                      ;(R5)=EXPECTED DATA IN
1336                                                                           ;SYSTEM CONTROL REGISTER, 0
1337  003062  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1338                                                                           ;SYSTEM CONTROL REGISTER
1339  003064  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
```

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1340                                                        ;WRITE/READ ERROR
1341  003066  104400                2$:     SCOPE           ;CHECK FOR ITERATIONS, LOOP
1342
1343                                ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1344                                ;SET MEMORY EXTENSION BIT 0 IN SYSTEM CONTROL REGISTER
1345                                ;VERIFY THAT MEMORY EXTENSION BIT 0 WAS SET
1346                                ;CLEAR MEMORY EXTENSION BIT 0
1347                                ;VERITY THAT MEMORY EXTENSION BIT 0 WAS CLEARED
1348
1349  003070  012767  000340  174700  T21:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
1350  003076  012767  004000  014344        MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
1351  003104  012767  003154  014332        MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1352  003112  016703  014264                MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1353  003116  012713  000020                MOV     #BIT04,(R3)     ;SET MEMORY EXTENSION BIT 0
1354  003122  022713  000020                CMP     #BIT04,(R3)     ;VERIFY THAT MEMORY EXTENSION BIT 0 WAS SET
1355  003126  001404                        BEQ     1$
1356  003130  012705  000020                MOV     #BIT04,R5       ;(R5)= EXPECTED VALUE
1357                                                                ;IN SYSTEM CONTROL REGISTER
1358                                                                ;MEMORY EXTENSION BIT 0
1359  003134  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
1360                                                                ;SYSTEM CONTROL REGISTER
1361  003136  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
1362                                                                ;WRITE/READ ERROR
1363  003140  042713  000020        1$:     BIC     #BIT04,(R3)     ;CLEAR MEMORY EXTENSION BIT 0
1364  003144  001403                        BEQ     2$
1365  003146  005005                        CLR     R5              ;(R5)=EXPECTED DATA IN
1366                                                                ;SYSTEM CONTROL REGISTER, 0
1367  003150  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
1368                                                                ;SYSTEM CONTROL REGISTER
1369  003152  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
1370                                                                ;WRITE/READ ERROR
1371  003154  104400                2$:     SCOPE           ;CHECK FOR ITERATIONS, LOOP
1372
1373                                ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1374                                ;SET MEMORY EXTENSION BIT 1 IN SYSTEM CONTROL REGISTER
1375                                ;VERIFY THAT MEMORY EXTENSION BIT 1 WAS SET
1376                                ;CLEAR MEMORY EXTENSION BIT 1
1377                                ;VERITY THAT MEMORY EXTENSION BIT 1 WAS CLEARED
1378
1379  003156  012767  000340  174612  T22:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
1380  003164  012767  004000  014256        MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
1381  003172  012767  003242  014244        MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1382  003200  016703  014176                MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1383  003204  012713  000040                MOV     #BIT05,(R3)     ;SET MEMORY EXTENSION BIT 1
1384  003210  022713  000040                CMP     #BIT05,(R3)     ;VERIFY THAT MEMORY EXTENSION BIT 1 WAS SET
1385  003214  001404                        BEQ     1$
1386  003216  012705  000040                MOV     #BIT05,R5       ;(R5)= EXPECTED VALUE
1387                                                                ;IN SYSTEM CONTROL REGISTER
1388                                                                ;MEMORY EXTENSION BIT 1
1389  003222  011304                        MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
1390                                                                ;SYSTEM CONTROL REGISTER
1391  003224  104001                        HLT     1               ;SYSTEM CONTROL REGISTER
1392                                                                ;WRITE/READ ERROR
1393  003226  042713  000040        1$:     BIC     #BIT05,(R3)     ;CLEAR MEMORY EXTENSION BIT 1
1394  003232  001403                        BEQ     2$
1395  003234  005005                        CLR     R5              ;(R5)=EXPECTED DATA IN
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1396
1397  003236  011304                          MOV     (R3),R4         ;SYSTEM CONTROL REGISTER, 0
1398                                                                  ;(R4)=ACTUAL DATA IN
1399  003240  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
1400                                                                  ;SYSTEM CONTROL REGISTER
1401  003242  104400                  2$:     SCOPE                   ;WRITE/READ ERROR
1402                                                                  ;CHECK FOR ITERATIONS, LOOP
1403                                  ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1404                                  ;SET RECEIVER INTERRUPT ENABLE IN SYSTEM CONTROL REGISTER
1405                                  ;VERIFY THAT RECEIVER INTERRUPT ENABLE WAS SET
1406                                  ;CLEAR RECEIVER INTERRUPT ENABLE
1407                                  ;VERITY THAT RECEIVER INTERRUPT ENABLE WAS CLEARED
1408
1409  003244  012767  000340  174524  T23:     MOV     #340,PS         ;DISABLE ALL INTERRUPTS
1410  003252  012767  004000  014170          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
1411  003260  012767  003330  014156          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1412  003266  016703  014110                  MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1413  003272  012713  000100                  MOV     #BIT06,(R3)     ;SET RECEIVER INTERRUPT ENABLE
1414  003276  022713  000100                  CMP     #BIT06,(R3)     ;VERIFY THAT RECEIVER INTERRUPT ENABLE WAS SET
1415  003302  001404                          BEQ     1$
1416  003304  012705  000100                  MOV     #BIT06,R5       ;(R5)= EXPECTED VALUE
1417                                                                  ;IN SYSTEM CONTROL REGISTER
1418                                                                  ;RECEIVER INTERRUPT ENABLE
1419  003310  011304                          MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
1420                                                                  ;SYSTEM CONTROL REGISTER
1421  003312  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
1422                                                                  ;WRITE/READ ERROR
1423  003314  042713  000100          1$:     BIC     #BIT06,(R3)     ;CLEAR RECEIVER INTERRUPT ENABLE
1424  003320  001403                          BEQ     2$
1425  003322  005005                          CLR     R5              ;(R5)=EXPECTED DATA IN
1426                                                                  ;SYSTEM CONTROL REGISTER, 0
1427  003324  011304                          MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
1428                                                                  ;SYSTEM CONTROL REGISTER
1429  003326  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
1430                                                                  ;WRITE/READ ERROR
1431  003330  104400                  2$:     SCOPE                   ;CHECK FOR ITERATIONS, LOOP
1432
1433                                  ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1434                                  ;SET MAINTENANCE MODE IN SYSTEM CONTROL REGISTER
1435                                  ;VERIFY THAT MAINTENANCE MODE WAS SET
1436                                  ;CLEAR MAINTENANCE MODE
1437                                  ;VERITY THAT MAINTENANCE MODE WAS CLEARED
1438
1439  003332  012767  000340  174436  T24:     MOV     #340,PS         ;DISABLE ALL INTERRUPTS
1440  003340  012767  004000  014102          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
1441  003346  012767  003416  014070          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1442  003354  016703  014022                  MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1443  003360  012713  001000                  MOV     #BIT09,(R3)     ;SET MAINTENANCE MODE
1444  003364  022713  001000                  CMP     #BIT09,(R3)     ;VERIFY THAT MAINTENANCE MODE WAS SET
1445  003370  001404                          BEQ     1$
1446  003372  012705  001000                  MOV     #BIT09,R5       ;(R5)= EXPECTED VALUE
1447                                                                  ;IN SYSTEM CONTROL REGISTER
1448                                                                  ;MAINTENANCE MODE
1449  003376  011304                          MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
1450                                                                  ;SYSTEM CONTROL REGISTER
1451  003400  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
```

F03


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1452
1453  003402  042713  001000          1$:     BIC     #BIT09,(R3)             ;WRITE/READ ERROR
1454  003406  001403                          BEQ     2$                      ;CLEAR MAINTENANCE MODE
1455  003410  005005                          CLR     R5
1456                                                                          ;(R5)=EXPECTED DATA IN
1457  003412  011304                          MOV     (R3),R4                 ;SYSTEM CONTROL REGISTER, 0
1458                                                                          ;(R4)=ACTUAL DATA IN
1459  003414  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1460                                                                          ;SYSTEM CONTROL REGISTER
1461  003416  104400                  2$:     SCOPE                           ;WRITE/READ ERROR
1462                                                                          ;CHECK FOR ITERATIONS, LOOP
1463                                  ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1464                                  ;SET SILO OVERFLOW INTERRUPT ENABLE IN SYSTEM CONTROL REGISTER
1465                                  ;VERIFY THAT SILO OVERFLOW INTERRUPT ENABLE WAS SET
1466                                  ;CLEAR SILO OVERFLOW INTERRUPT ENABLE
1467                                  ;VERITY THAT SILO OVERFLOW INTERRUPT ENABLE WAS CLEARED
1468
1469  003420  012767  000340  174350  T25:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1470  003426  012767  004000  014014          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1471  003434  012767  003504  014002          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1472  003442  016703  013734                  MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1473  003446  012713  010000                  MOV     #BIT12,(R3)             ;SET SILO OVERFLOW INTERRUPT ENABLE
1474  003452  022713  010000                  CMP     #BIT12,(R3)             ;VERIFY THAT SILO OVERFLOW INTERRUPT ENABLE WAS
1475  003456  001404                          BEQ     1$
1476  003460  012705  010000                  MOV     #BIT12,R5               ;(R5)= EXPECTED VALUE
1477                                                                          ;IN SYSTEM CONTROL REGISTER
1478                                                                          ;SILO OVERFLOW INTERRUPT ENABLE
1479  003464  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1480                                                                          ;SYSTEM CONTROL REGISTER
1481  003466  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1482                                                                          ;WRITE/READ ERROR
1483  003470  042713  010000          1$:     BIC     #BIT12,(R3)             ;CLEAR SILO OVERFLOW INTERRUPT ENABLE
1484  003474  001403                          BEQ     2$
1485  003476  005005                          CLR     R5
1486                                                                          ;(R5)=EXPECTED DATA IN
1487  003500  011304                          MOV     (R3),R4                 ;SYSTEM CONTROL REGISTER, 0
1488                                                                          ;(R4)=ACTUAL DATA IN
1489  003502  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1490                                                                          ;SYSTEM CONTROL REGISTER
1491  003504  104400                  2$:     SCOPE                           ;WRITE/READ ERROR
1492                                                                          ;CHECK FOR ITERATIONS, LOOP
1493                                  ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1494                                  ;SET TRANSMITTER INTERRUPT ENABLE IN SYSTEM CONTROL REGISTER
1495                                  ;VERIFY THAT TRANSMITTER INTERRUPT ENABLE WAS SET
1496                                  ;CLEAR TRANSMITTER INTERRUPT ENABLE
1497                                  ;VERITY THAT TRANSMITTER INTERRUPT ENABLE WAS CLEARED
1498
1499  003506  012767  000340  174262  T26:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1500  003514  012767  004000  013726          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1501  003522  012767  003572  013714          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1502  003530  016703  013646                  MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1503  003534  012713  020000                  MOV     #BIT13,(R3)             ;SET TRANSMITTER INTERRUPT ENABLE
1504  003540  022713  020000                  CMP     #BIT13,(R3)             ;VERIFY THAT TRANSMITTER INTERRUPT ENABLE WAS SE
1505  003544  001404                          BEQ     1$
1506  003546  012705  020000                  MOV     #BIT13,R5               ;(R5)= EXPECTED VALUE
1507                                                                          ;IN SYSTEM CONTROL REGISTER
```

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1508
1509  003552  011304                          MOV     (R3),R4         ;TRANSMITTER INTERRUPT ENABLE
1510                                                                  ;(R4)=ACTUAL DATA IN
1511  003554  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
1512                                                                  ;SYSTEM CONTROL REGISTER
1513  003556  042713  020000          1$:     BIC     #BIT13,(R3)     ;WRITE/READ ERROR
1514  003562  001403                          BEQ     2$              ;CLEAR TRANSMITTER INTERRUPT ENABLE
1515  003564  005005                          CLR     R5
1516                                                                  ;(R5)=EXPECTED DATA IN
1517  003566  011304                          MOV     (R3),R4         ;SYSTEM CONTROL REGISTER, 0
1518                                                                  ;(R4)=ACTUAL DATA IN
1519  003570  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
1520                                                                  ;SYSTEM CONTROL REGISTER
1521  003572  104400                  2$:     SCOPE                   ;WRITE/READ ERROR
1522                                                                  ;CHECK FOR ITERATIONS, LOOP
1523                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1524                          ;SET TRANSMITTER DONE IN SYSTEM CONTROL REGISTER
1525                          ;VERIFY THAT TRANSMITTER DONE WAS SET
1526                          ;CLEAR TRANSMITTER DONE
1527                          ;VERITY THAT TRANSMITTER DONE WAS CLEARED
1528
1529  003574  012767  000340  174174  T27:     MOV     #340,PS         ;DISABLE ALL INTERRUPTS
1530  003602  012767  004000  013640          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
1531  003610  012767  003660  013626          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1532  003616  016703  013560                  MOV     DHSCR,R3        ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1533  003622  012713  100000                  MOV     #BIT15,(R3)     ;SET TRANSMITTER DONE
1534  003626  022713  100000                  CMP     #BIT15,(R3)     ;VERIFY THAT TRANSMITTER DONE WAS SET
1535  003632  001404                          BEQ     1$
1536  003634  012705  100000                  MOV     #BIT15,R5       ;(R5)= EXPECTED VALUE
1537                                                                  ;IN SYSTEM CONTROL REGISTER
1538                                                                  ;TRANSMITTER DONE
1539  003640  011304                          MOV     (R3),R4         ;(R4)=ACTUAL DATA IN
1540                                                                  ;SYSTEM CONTROL REGISTER
1541  003642  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
1542                                                                  ;WRITE/READ ERROR
1543  003644  042713  100000          1$:     BIC     #BIT15,(R3)     ;CLEAR TRANSMITTER DONE
1544  003650  001403                          BEQ     2$
1545  003652  005005                          CLR     R5
1546                                                                  ;(R5)=EXPECTED DATA IN
1547  003654  011304                          MOV     (R3),R4         ;SYSTEM CONTROL REGISTER, 0
1548                                                                  ;(R4)=ACTUAL DATA IN
1549  003656  104001                          HLT     1               ;SYSTEM CONTROL REGISTER
1550                                                                  ;SYSTEM CONTROL REGISTER
1551  003660  104400                  2$:     SCOPE                   ;WRITE/READ ERROR
1552                                                                  ;CHECK FOR ITERATIONS, LOOP
1553                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1554                          ;VERIFY THAT CHARACTER AVAILABLE IS READ ONLY IN NORMAL MODE
1555
1556  003662  012767  000340  174106  T30:     MOV     #340,PS         ;DISABLE ALL INTERRUPTS
1557  003670  012767  004000  013552          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
1558  003676  012767  003734  013540          MOV     #1$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
1559  003704  012777  000200  013470          MOV     #BIT07,@DHSCR   ;ATTEMPT TO WRITE
1560                                                                  ;CHARACTER AVAILABLE IN
1561                                                                  ;SYSTEM CONTROL REGISTER
1562  003712  005777  013464                  TST     @DHSCR          ;WAS CHARACTER AVAILABLE SET
1563  003716  001406                          BEQ     1$
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1564  003720  005005                          CLR     R5                      ;(R5)=EXPECTED DATA
1565                                                                          ;IN SYSTEM CONTROL REGISTER, 0
1566  003722  017704  013454                  MOV     @DHSCR,R4               ;(R4)=ACTUAL DATA IN SYSTEM
1567                                                                          ;CONTROL REGISTER
1568  003726  016703  013450                  MOV     DHSCR,R3                ;ADDRESS OF SYSTEM CONTROL REGISTER
1569  003732  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1570                                                                          ;WRITE/READ ERROR
1571  003734  104400              1$:         SCOPE
1572
1573                                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1574                                          ;VERIFY THAT CLEAR      NON EXISTANT MEMORY IS READ ONLY IN NORMAL MODE
1575
1576  003736  012767  000340  174032  T31:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1577  003744  012767  004000  013476          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1578  003752  012767  004010  013464          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1579  003760  012777  000400  013414          MOV     #BIT08,@DHSCR           ;ATTEMPT TO WRITE
1580                                                                          ;CLEAR  NON EXISTANT MEMORY IN
1581                                                                          ;SYSTEM CONTROL REGISTER
1582  003766  005777  013410                  TST     @DHSCR                  ;WAS CLEAR      NON EXISTANT MEMORY SET
1583  003772  001406                          BEQ     1$
1584  003774  005005                          CLR     R5                      ;(R5)=EXPECTED DATA
1585                                                                          ;IN SYSTEM CONTROL REGISTER, 0
1586  003776  017704  013400                  MOV     @DHSCR,R4               ;(R4)=ACTUAL DATA IN SYSTEM
1587                                                                          ;CONTROL REGISTER
1588  004002  016703  013374                  MOV     DHSCR,R3                ;ADDRESS OF SYSTEM CONTROL REGISTER
1589  004006  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1590                                                                          ;WRITE/READ ERROR
1591  004010  104400              1$:         SCOPE
1592
1593                                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1594                                          ;VERIFY THAT NON EXISTANT MEMORY IS READ ONLY IN NORMAL MODE
1595
1596  004012  012767  000340  173756  T32:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1597  004020  012767  004000  013422          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1598  004026  012767  004064  013410          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1599  004034  012777  002000  013340          MOV     #BIT10,@DHSCR           ;ATTEMPT TO WRITE
1600                                                                          ;NON EXISTANT MEMORY IN
1601                                                                          ;SYSTEM CONTROL REGISTER
1602  004042  005777  013334                  TST     @DHSCR                  ;WAS NON EXISTANT MEMORY SET
1603  004046  001406                          BEQ     1$
1604  004050  005005                          CLR     R5                      ;(R5)=EXPECTED DATA
1605                                                                          ;IN SYSTEM CONTROL REGISTER, 0
1606  004052  017704  013324                  MOV     @DHSCR,R4               ;(R4)=ACTUAL DATA IN SYSTEM
1607                                                                          ;CONTROL REGISTER
1608  004056  016703  013320                  MOV     DHSCR,R3                ;ADDRESS OF SYSTEM CONTROL REGISTER
1609  004062  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1610                                                                          ;WRITE/READ ERROR
1611  004064  104400              1$:         SCOPE
1612
1613                                          ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1614                                          ;VERIFY THAT MASTER CLEAR IS READ ONLY IN NORMAL MODE
1615
1616  004066  012767  000340  173702  T33:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1617  004074  012767  004000  013346          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1618  004102  012767  004140  013334          MOV     #1$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1619  004110  012777  004000  013264          MOV     #BIT11,@DHSCR           ;ATTEMPT TO WRITE
```

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1620                                                                    ;MASTER CLEAR IN
1621                                                                    ;SYSTEM CONTROL REGISTER
1622  004116  005777  013260              TST     @DHSCR                ;WAS MASTER CLEAR SET
1623  004122  001406                      BEQ     1$
1624  004124  005005                      CLR     R5                    ;(R5)=EXPECTED DATA
1625                                                                    ;IN SYSTEM CONTROL REGISTER, 0
1626  004126  017704  013250              MOV     @DHSCR,R4             ;(R4)=ACTUAL DATA IN SYSTEM
1627                                                                    ;CONTROL REGISTER
1628  004132  016703  013244              MOV     DHSCR,R3              ;ADDRESS OF SYSTEM CONTROL REGISTER
1629  004136  104001                      HLT     1                     ;SYSTEM CONTROL REGISTER
1630                                                                    ;WRITE/READ ERROR
1631  004140  104400              1$:     SCOPE
1632
1633                                      ;SYSTEM CONTROL REGISTER WRITE/READ TEST (NORMAL MODE)
1634                                      ;VERIFY THAT SILO OVERFLOW IS READ ONLY IN NORMAL MODE
1635
1636  004142  012767  000340  173626  T34: MOV     #340,PS               ;DISABLE ALL INTERRUPTS
1637  004150  012767  004000  013272      MOV     #4000,ICOUNT          ;SET UP FOR 4000 ITERATIONS
1638  004156  012767  004214  013260      MOV     #1$,ESCAPE            ;SET UP TO ESCAPE TO NEXT TEST
1639  004164  012777  040000  013210      MOV     #BIT14,@DHSCR         ;ATTEMPT TO WRITE
1640                                                                    ;SILO OVERFLOW IN
1641                                                                    ;SYSTEM CONTROL REGISTER
1642  004172  005777  013204              TST     @DHSCR                ;WAS SILO OVERFLOW SET
1643  004176  001406                      BEQ     1$
1644  004200  005005                      CLR     R5                    ;(R5)=EXPECTED DATA
1645                                                                    ;IN SYSTEM CONTROL REGISTER, 0
1646  004202  017704  013174              MOV     @DHSCR,R4             ;(R4)=ACTUAL DATA IN SYSTEM
1647                                                                    ;CONTROL REGISTER
1648  004206  016703  013170              MOV     DHSCR,R3              ;ADDRESS OF SYSTEM CONTROL REGISTER
1649  004212  104001                      HLT     1                     ;SYSTEM CONTROL REGISTER
1650                                                                    ;WRITE/READ ERROR
1651  004214  104400              1$:     SCOPE
1652                                      ;SYSTEM CONTROL REGISTER WRITE/READ TEST (MAINTENANCE MODE)
1653                                      ;SET MAINTENANCE MODE
1654                                      ;SET CHARACTER AVAILABLE IN SYSTEM CONTROL REGISTER
1655                                      ;VERIFY THAT CHARACTER AVAILABLE WAS SET
1656                                      ;CLEAR MAINTENANCE MODE
1657                                      ;VERIFY THAT CHARACTER AVAILABLE CANNOT BE CLEARED
1658                                      ;SET MAINTENANCE MODE
1659                                      ;CLEAR CHARACTER AVAILABLE
1660                                      ;VERIFY THAT CHARACTER AVAILABLE WAS CLEARED
1661
1662  004216  012767  000340  173552  T35: MOV     #340,PS               ;DISABLE ALL INTERRUPTS
1663  004224  012767  004000  013216      MOV     #4000,ICOUNT          ;SET UP FOR 4000 ITERATIONS
1664  004232  012767  004344  013204      MOV     #3$,ESCAPE            ;SET UP TO ESCAPE TO NEXT TEST
1665  004240  016703  013136              MOV     DHSCR,R3              ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1666  004244  012713  001000              MOV     #BIT09,(R3)           ;SET MAINTENANCE MODE
1667  004250  052713  000200              BIS     #BIT07,(R3)           ;SET CHARACTER AVAILABLE
1668  004254  022713  001200              CMP     #BIT09+BIT07,(R3)     ;VERIFY THAT CHARACTER AVAILABLE
1669                                                                    ;AND MAINTENANCE MODE ARE SET
1670  004260  001404                      BEQ     1$
1671  004262  012705  001200              MOV     #BIT09+BIT07,R5 ;(R5)=EXPECTED DATA
1672                                                                    ;IN SYSTEM CONTROL REGISTER
1673                                                                    ;MAINTENANCE MODE AND CHARACTER AVAILABLE
1674  004266  011304                      MOV     (R3),R4               ;(R4)=ACTUAL DATA IN
1675                                                                    ;SYSTEM CONTROL REGISTER
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1676  004270  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1677                                                                          ;WRITE/READ ERROR
1678  004272  042713  001000          1$:     BIC     #BIT09,(R3)             ;CLEAR MAINTENANCE MODE
1679  004276  042713  000200                  BIC     #BIT07,(R3)             ;ATTEMPT TO CLEAR CHARACTER AVAILABLE
1680  004302  022713  000200                  CMP     #BIT07,(R3)             ;CHARACTER AVAILABLE SHOULD BE SET
1681  004306  001403                          BEQ     2$
1682  004310  012705  000200                  MOV     #BIT07,R5               ;(R5)=EXPECTED DATA IN
1683                                                                          ;SYSTEM CONTROL REGISTER
1684                                                                          ;CHARACTER AVAILABLE
1685  004314  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1686                                                                          ;WRITE/READ ERROR
1687  004316  052713  001000          2$:     BIS     #BIT09,(R3)             ;SET MAINTENANCE MODE
1688  004322  042713  000200                  BIC     #BIT07,(R3)             ;CLEAR CHARACTER AVAILABLE
1689  004326  022713  001000                  CMP     #BIT09,(R3)             ;EXPECT ONLY MAINTENANCE
1690                                                                          ;MODE TO BE SET
1691  004332  001404                          BEQ     3$
1692  004334  012705  001000                  MOV     #BIT09,R5               ;(R5)=EXPECTED DATA IN
1693                                                                          ;SYSTEM CONTROL REGISTER,
1694                                                                          ;MAINTENANCE MODE BIT
1695  004340  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1696                                                                          ;SYSTEM CONTROL REGISTER
1697  004342  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1698                                                                          ;WRITE/READ ERROR
1699  004344  104400                  3$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1700                                  ;SYSTEM CONTROL REGISTER WRITE/READ TEST (MAINTENANCE MODE)
1701                                  ;SET MAINTENANCE MODE
1702                                  ;SET NON EXISTANT MEMORY IN SYSTEM CONTROL REGISTER
1703                                  ;VERIFY THAT NON EXISTANT MEMORY WAS SET
1704                                  ;CLEAR MAINTENANCE MODE
1705                                  ;VERIFY THAT NON EXISTANT MEMORY CANNOT BE CLEARED
1706                                  ;SET MAINTENANCE MODE
1707                                  ;CLEAR NON EXISTANT MEMORY
1708                                  ;VERIFY THAT NON EXISTANT MEMORY WAS CLEARED
1709
1710  004346  012767  000340  173422  T36:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1711  004354  012767  004000  013066          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1712  004362  012767  004474  013054          MOV     #3$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1713  004370  016703  013006                  MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1714  004374  012713  001000                  MOV     #BIT09,(R3)             ;SET MAINTENANCE MODE
1715  004400  052713  002000                  BIS     #BIT10,(R3)             ;SET NON EXISTANT MEMORY
1716  004404  022713  003000                  CMP     #BIT09+BIT10,(R3)       ;VERIFY THAT NON EXISTANT MEMORY
1717                                                                          ;AND MAINTENANCE MODE ARE SET
1718  004410  001404                          BEQ     1$
1719  004412  012705  003000                  MOV     #BIT09+BIT10,R5 ;(R5)=EXPECTED DATA
1720                                                                          ;IN SYSTEM CONTROL REGISTER
1721                                                                          ;MAINTENANCE MODE AND NON EXISTANT MEMORY
1722  004416  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1723                                                                          ;SYSTEM CONTROL REGISTER
1724  004420  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1725                                                                          ;WRITE/READ ERROR
1726  004422  042713  001000          1$:     BIC     #BIT09,(R3)             ;CLEAR MAINTENANCE MODE
1727  004426  042713  002000                  BIC     #BIT10,(R3)             ;ATTEMPT TO CLEAR NON EXISTANT MEMORY
1728  004432  022713  002000                  CMP     #BIT10,(R3)             ;NON EXISTANT MEMORY SHOULD BE SET
1729  004436  001403                          BEQ     2$
1730  004440  012705  002000                  MOV     #BIT10,R5               ;(R5)=EXPECTED DATA IN
1731                                                                          ;SYSTEM CONTROL REGISTER
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1732
1733  004444  104001                          HLT     1                       ;NON EXISTANT MEMORY
1734                                                                          ;SYSTEM CONTROL REGISTER
1735  004446  052713  001000          2$:     BIS     #BIT09,(R3)             ;WRITE/READ ERROR
1736  004452  042713  002000          2$:     BIC     #BIT10,(R3)             ;SET MAINTENANCE MODE
1737  004456  022713  001000          2$:     CMP     #BIT09,(R3)             ;CLEAR NON EXISTANT MEMORY
1738                                                                          ;EXPECT ONLY MAINTENANCE
1739  004462  001404                          BEQ     3$                      ;MODE TO BE SET
1740  004464  012705  001000                  MOV     #BIT09,R5               ;(R5)=EXPECTED DATA IN
1741                                                                          ;SYSTEM CONTROL REGISTER,
1742                                                                          ;MAINTENANCE MODE BIT
1743  004470  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1744                                                                          ;SYSTEM CONTROL REGISTER
1745  004472  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1746                                                                          ;WRITE/READ ERROR
1747  004474  104400          3$:     SCOPE                                   ;CHECK FOR ITERATIONS, LOOP
1748                  ;SYSTEM CONTROL REGISTER WRITE/READ TEST (MAINTENANCE MODE)
1749                  ;SET MAINTENANCE MODE
1750                  ;SET SILO OVERFLOW IN SYSTEM CONTROL REGISTER
1751                  ;VERIFY THAT SILO OVERFLOW WAS SET
1752                  ;CLEAR MAINTENANCE MODE
1753                  ;VERIFY THAT SILO OVERFLOW CANNOT BE CLEARED
1754                  ;SET MAINTENANCE MODE
1755                  ;CLEAR SILO OVERFLOW
1756                  ;VERIFY THAT SILO OVERFLOW WAS CLEARED
1757
1758  004476  012767  000340  173272  T37:     MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1759  004504  012767  004000  012736          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1760  004512  012767  004624  012724          MOV     #3$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1761  004520  016703  012656                  MOV     DHSCR,R3                ;PUT ADDRESS OF SYSTEM CONTROL REGISTER IN R3
1762  004524  012713  001000                  MOV     #BIT09,(R3)             ;SET MAINTENANCE MODE
1763  004530  052713  040000                  BIS     #BIT14,(R3)             ;SET SILO OVERFLOW
1764  004534  022713  041000                  CMP     #BIT09+BIT14,(R3)       ;VERIFY THAT SILO OVERFLOW
1765                                                                          ;AND MAINTENANCE MODE ARE SET
1766  004540  001404                          BEQ     1$
1767  004542  012705  041000                  MOV     #BIT09+BIT14,R5 ;(R5)=EXPECTED DATA
1768                                                                          ;IN SYSTEM CONTROL REGISTER
1769                                                                          ;MAINTENANCE MODE AND SILO OVERFLOW
1770  004546  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1771                                                                          ;SYSTEM CONTROL REGISTER
1772  004550  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1773                                                                          ;WRITE/READ ERROR
1774  004552  042713  001000          1$:     BIC     #BIT09,(R3)             ;CLEAR MAINTENANCE MODE
1775  004556  042713  040000                  BIC     #BIT14,(R3)             ;ATTEMPT TO CLEAR SILO OVERFLOW
1776  004562  022713  040000                  CMP     #BIT14,(R3)             ;SILO OVERFLOW SHOULD BE SET
1777  004566  001403                          BEQ     2$
1778  004570  012705  040000                  MOV     #BIT14,R5               ;(R5)=EXPECTED DATA IN
1779                                                                          ;SYSTEM CONTROL REGISTER
1780                                                                          ;SILO OVERFLOW
1781  004574  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1782                                                                          ;WRITE/READ ERROR
1783  004576  052713  001000          2$:     BIS     #BIT09,(R3)             ;SET MAINTENANCE MODE
1784  004602  042713  040000                  BIC     #BIT14,(R3)             ;CLEAR SILO OVERFLOW
1785  004606  022713  001000                  CMP     #BIT09,(R3)             ;EXPECT ONLY MAINTENANCE
1786                                                                          ;MODE TO BE SET
1787  004612  001404                          BEQ     3$
```

```
1788  004614  012705  001000                  MOV     #BIT09,R5               ;(R5)=EXPECTED DATA IN
1789                                                                          ;SYSTEM CONTROL REGISTER,
1790                                                                          ;MAINTENANCE MODE BIT
1791  004620  011304                          MOV     (R3),R4                 ;(R4)=ACTUAL DATA IN
1792                                                                          ;SYSTEM CONTROL REGISTER
1793  004622  104001                          HLT     1                       ;SYSTEM CONTROL REGISTER
1794                                                                          ;WRITE/READ ERROR
1795  004624  104400                  3$:     SCOPE                           ;CHECK FOR ITERATIONS, LOOP
1796
1797                                          ;LINE PARAMETER REGISTER DATA TEST
1798                                          ;SET BIT 0 IN LINE PARAMETER TO 1
1799                                          ;VERIFY THAT BIT 0 WAS SET
1800                                          ;CLEAR BIT 0
1801                                          ;VERIFY THAT BIT 0 WAS CLEARED
1802
1803  004626  012767  000340  173142  T40:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1804  004634  012767  004000  012606          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1805  004642  012767  004714  012574          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1806  004650  012777  004000  012524          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1807  004656  016703  012524                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1808  004662  012705  000001                  MOV     #1,R5                   ;BIT 0 WILL BE SET IN LINE PARAMETER
1809  004666  010513                          MOV     R5,(R3)                 ;SET BIT 0
1810  004670  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1811  004672  020504                          CMP     R5,R4                   ;WAS BIT 0 SET
1812  004674  001401                          BEQ     1$
1813  004676  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1814  004700  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 0
1815  004702  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1816  004704  005704                          TST     R4                      ;WAS BIT 0 CLEARED
1817  004706  001402                          BEQ     2$
1818  004710  005005                          CLR     R5
1819  004712  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1820  004714  104400                  2$:     SCOPE
1821
1822                                          ;LINE PARAMETER REGISTER DATA TEST
1823                                          ;SET BIT 1 IN LINE PARAMETER TO 1
1824                                          ;VERIFY THAT BIT 1 WAS SET
1825                                          ;CLEAR BIT 1
1826                                          ;VERIFY THAT BIT 1 WAS CLEARED
1827
1828  004716  012767  000340  173052  T41:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1829  004724  012767  004000  012516          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1830  004732  012767  005004  012504          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1831  004740  012777  004000  012434          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1832  004746  016703  012434                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1833  004752  012705  000002                  MOV     #2,R5                   ;BIT 1 WILL BE SET IN LINE PARAMETER
1834  004756  010513                          MOV     R5,(R3)                 ;SET BIT 1
1835  004760  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1836  004762  020504                          CMP     R5,R4                   ;WAS BIT 1 SET
1837  004764  001401                          BEQ     1$
1838  004766  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1839  004770  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 1
1840  004772  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1841  004774  005704                          TST     R4                      ;WAS BIT 1 CLEARED
1842  004776  001402                          BEQ     2$
1843  005000  005005                          CLR     R5
```

```
1844  005002  104002                    HLT     2                       ;LINE PARAMETER REGISTER ERROR
1845  005004  104400            2$:     SCOPE
1846
1847                                    ;LINE PARAMETER REGISTER DATA TEST
1848                                    ;SET BIT 2 IN LINE PARAMETER TO 1
1849                                    ;VERIFY THAT BIT 2 WAS SET
1850                                    ;CLEAR BIT 2
1851                                    ;VERIFY THAT BIT 2 WAS CLEARED
1852
1853  005006  012767  000340  172762    T42:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1854  005014  012767  004000  012426            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1855  005022  012767  005074  012414            MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1856  005030  012777  004000  012344            MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1857  005036  016703  012344                    MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1858  005042  012705  000004                    MOV     #4,R5                   ;BIT 2 WILL BE SET IN LINE PARAMETER
1859  005046  010513                            MOV     R5,(R3)                 ;SET BIT 2
1860  005050  011304                            MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1861  005052  020504                            CMP     R5,R4                   ;WAS BIT 2 SET
1862  005054  001401                            BEQ     1$
1863  005056  104002                            HLT     2                       ;LINE PARAMETER REGISTER ERROR
1864  005060  040513            1$:     BIC     R5,(R3)                 ;CLEAR BIT 2
1865  005062  011304                            MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1866  005064  005704                            TST     R4                      ;WAS BIT 2 CLEARED
1867  005066  001402                            BEQ     2$
1868  005070  005005                            CLR     R5
1869  005072  104002                            HLT     2                       ;LINE PARAMETER REGISTER ERROR
1870  005074  104400            2$:     SCOPE
1871
1872                                    ;LINE PARAMETER REGISTER DATA TEST
1873                                    ;SET BIT 4 IN LINE PARAMETER TO 1
1874                                    ;VERIFY THAT BIT 4 WAS SET
1875                                    ;CLEAR BIT 4
1876                                    ;VERIFY THAT BIT 4 WAS CLEARED
1877
1878  005076  012767  000340  172672    T43:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1879  005104  012767  004000  012336            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1880  005112  012767  005164  012324            MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1881  005120  012777  004000  012254            MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1882  005126  016703  012254                    MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1883  005132  012705  000020                    MOV     #20,R5                  ;BIT 4 WILL BE SET IN LINE PARAMETER
1884  005136  010513                            MOV     R5,(R3)                 ;SET BIT 4
1885  005140  011304                            MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1886  005142  020504                            CMP     R5,R4                   ;WAS BIT 4 SET
1887  005144  001401                            BEQ     1$
1888  005146  104002                            HLT     2                       ;LINE PARAMETER REGISTER ERROR
1889  005150  040513            1$:     BIC     R5,(R3)                 ;CLEAR BIT 4
1890  005152  011304                            MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1891  005154  005704                            TST     R4                      ;WAS BIT 4 CLEARED
1892  005156  001402                            BEQ     2$
1893  005160  005005                            CLR     R5
1894  005162  104002                            HLT     2                       ;LINE PARAMETER REGISTER ERROR
1895  005164  104400            2$:     SCOPE
1896
1897                                    ;LINE PARAMETER REGISTER DATA TEST
1898                                    ;SET BIT 5 IN LINE PARAMETER TO 1
1899                                    ;VERIFY THAT BIT 5 WAS SET
```

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1900                                            ;CLEAR BIT 5
1901                                            ;VERIFY THAT BIT 5 WAS CLEARED
1902
1903  005166  012767  000340  172602  T44:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1904  005174  012767  004000  012246          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1905  005202  012767  005254  012234          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1906  005210  012777  004000  012164          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1907  005216  016703  012164                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1908  005222  012705  000040                  MOV     #40,R5                  ;BIT 5 WILL BE SET IN LINE PARAMETER
1909  005226  010513                          MOV     R5,(R3)                 ;SET BIT 5
1910  005230  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1911  005232  020504                          CMP     R5,R4                   ;WAS BIT 5 SET
1912  005234  001401                          BEQ     1$
1913  005236  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1914  005240  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 5
1915  005242  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1916  005244  005704                          TST     R4                      ;WAS BIT 5 CLEARED
1917  005246  001402                          BEQ     2$
1918  005250  005005                          CLR     R5
1919  005252  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1920  005254  104400                  2$:     SCOPE
1921
1922                                            ;LINE PARAMETER REGISTER DATA TEST
1923                                            ;SET BIT 6 IN LINE PARAMETER TO 1
1924                                            ;VERIFY THAT BIT 6 WAS SET
1925                                            ;CLEAR BIT 6
1926                                            ;VERIFY THAT BIT 6 WAS CLEARED
1927
1928  005256  012767  000340  172512  T45:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1929  005264  012767  004000  012156          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1930  005272  012767  005344  012144          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1931  005300  012777  004000  012074          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1932  005306  016703  012074                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1933  005312  012705  000100                  MOV     #100,R5                 ;BIT 6 WILL BE SET IN LINE PARAMETER
1934  005316  010513                          MOV     R5,(R3)                 ;SET BIT 6
1935  005320  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1936  005322  020504                          CMP     R5,R4                   ;WAS BIT 6 SET
1937  005324  001401                          BEQ     1$
1938  005326  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1939  005330  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 6
1940  005332  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1941  005334  005704                          TST     R4                      ;WAS BIT 6 CLEARED
1942  005336  001402                          BEQ     2$
1943  005340  005005                          CLR     R5
1944  005342  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
1945  005344  104400                  2$:     SCOPE
1946
1947                                            ;LINE PARAMETER REGISTER DATA TEST
1948                                            ;SET BIT 7 IN LINE PARAMETER TO 1
1949                                            ;VERIFY THAT BIT 7 WAS SET
1950                                            ;CLEAR BIT 7
1951                                            ;VERIFY THAT BIT 7 WAS CLEARED
1952
1953  005346  012767  000340  172422  T46:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1954  005354  012767  004000  012066          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1955  005362  012767  005434  012054          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
```

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1956  005370  012777  004000  012004      MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1957  005376  016703  012004              MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1958  005402  012705  000200              MOV     #200,R5                 ;BIT 7 WILL BE SET IN LINE PARAMETER
1959  005406  010513                      MOV     R5,(R3)                 ;SET BIT 7
1960  005410  011304                      MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1961  005412  020504                      CMP     R5,R4                   ;WAS BIT 7 SET
1962  005414  001401                      BEQ     1$
1963  005416  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
1964  005420  040513              1$:     BIC     R5,(R3)                 ;CLEAR BIT 7
1965  005422  011304                      MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1966  005424  005704                      TST     R4                      ;WAS BIT 7 CLEARED
1967  005426  001402                      BEQ     2$
1968  005430  005005                      CLR     R5
1969  005432  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
1970  005434  104400              2$:     SCOPE
1971
1972                                      ;LINE PARAMETER REGISTER DATA TEST
1973                                      ;SET BIT 10 IN LINE PARAMETER TO 1
1974                                      ;VERIFY THAT BIT 10 WAS SET
1975                                      ;CLEAR BIT 10
1976                                      ;VERIFY THAT BIT 10 WAS CLEARED
1977
1978  005436  012767  000340  172332  T47:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
1979  005444  012767  004000  011776      MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
1980  005452  012767  005524  011764      MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
1981  005460  012777  004000  011714      MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
1982  005466  016703  011714              MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
1983  005472  012705  000400              MOV     #400,R5                 ;BIT 10 WILL BE SET IN LINE PARAMETER
1984  005476  010513                      MOV     R5,(R3)                 ;SET BIT 10
1985  005500  011304                      MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
1986  005502  020504                      CMP     R5,R4                   ;WAS BIT 10 SET
1987  005504  001401                      BEQ     1$
1988  005506  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
1989  005510  040513              1$:     BIC     R5,(R3)                 ;CLEAR BIT 10
1990  005512  011304                      MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
1991  005514  005704                      TST     R4                      ;WAS BIT 10 CLEARED
1992  005516  001402                      BEQ     2$
1993  005520  005005                      CLR     R5
1994  005522  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERROR
1995  005524  104400              2$:     SCOPE
1996
1997                                      ;LINE PARAMETER REGISTER DATA TEST
1998                                      ;SET BIT 11 IN LINE PARAMETER TO 1
1999                                      ;VERIFY THAT BIT 11 WAS SET
2000                                      ;CLEAR BIT 11
2001                                      ;VERIFY THAT BIT 11 WAS CLEARED
2002
2003  005526  012767  000340  172242  T50:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2004  005534  012767  004000  011706      MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2005  005542  012767  005614  011674      MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2006  005550  012777  004000  011624      MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2007  005556  016703  011624              MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
2008  005562  012705  001000              MOV     #1000,R5                ;BIT 11 WILL BE SET IN LINE PARAMETER
2009  005566  010513                      MOV     R5,(R3)                 ;SET BIT 11
2010  005570  011304                      MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2011  005572  020504                      CMP     R5,R4                   ;WAS BIT 11 SET
```

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2012  005574  001401                          BEQ     1$
2013  005576  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2014  005600  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 11
2015  005602  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
2016  005604  005704                          TST     R4                      ;WAS BIT 11 CLEARED
2017  005606  001402                          BEQ     2$
2018  005610  005005                          CLR     R5
2019  005612  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2020  005614  104400                  2$:     SCOPE
2021
2022                                          ;LINE PARAMETER REGISTER DATA TEST
2023                                          ;SET BIT 12 IN LINE PARAMETER TO 1
2024                                          ;VERIFY THAT BIT 12 WAS SET
2025                                          ;CLEAR BIT 12
2026                                          ;VERIFY THAT BIT 12 WAS CLEARED
2027
2028  005616  012767  000340  172152  T51:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2029  005624  012767  004000  011616          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2030  005632  012767  005704  011604          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2031  005640  012777  004000  011534          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2032  005646  016703  011534                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
2033  005652  012705  002000                  MOV     #2000,R5                        ;BIT 12 WILL BE SET IN LINE PARAMETER
2034  005656  010513                          MOV     R5,(R3)                 ;SET BIT 12
2035  005660  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2036  005662  020504                          CMP     R5,R4                   ;WAS BIT 12 SET
2037  005664  001401                          BEQ     1$
2038  005666  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2039  005670  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 12
2040  005672  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
2041  005674  005704                          TST     R4                      ;WAS BIT 12 CLEARED
2042  005676  001402                          BEQ     2$
2043  005700  005005                          CLR     R5
2044  005702  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2045  005704  104400                  2$:     SCOPE
2046
2047                                          ;LINE PARAMETER REGISTER DATA TEST
2048                                          ;SET BIT 13 IN LINE PARAMETER TO 1
2049                                          ;VERIFY THAT BIT 13 WAS SET
2050                                          ;CLEAR BIT 13
2051                                          ;VERIFY THAT BIT 13 WAS CLEARED
2052
2053  005706  012767  000340  172062  T52:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2054  005714  012767  004000  011526          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2055  005722  012767  005774  011514          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2056  005730  012777  004000  011444          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2057  005736  016703  011444                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
2058  005742  012705  004000                  MOV     #4000,R5                        ;BIT 13 WILL BE SET IN LINE PARAMETER
2059  005746  010513                          MOV     R5,(R3)                 ;SET BIT 13
2060  005750  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2061  005752  020504                          CMP     R5,R4                   ;WAS BIT 13 SET
2062  005754  001401                          BEQ     1$
2063  005756  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2064  005760  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 13
2065  005762  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
2066  005764  005704                          TST     R4                      ;WAS BIT 13 CLEARED
2067  005766  001402                          BEQ     2$
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2068  005770  005005                        CLR     R5
2069  005772  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2070  005774  104400              2$:       SCOPE
2071
2072                                        ;LINE PARAMETER REGISTER DATA TEST
2073                                        ;SET BIT 14 IN LINE PARAMETER TO 1
2074                                        ;VERIFY THAT BIT 14 WAS SET
2075                                        ;CLEAR BIT 14
2076                                        ;VERIFY THAT BIT 14 WAS CLEARED
2077
2078  005776  012767  000340  171772  T53:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2079  006004  012767  004000  011436        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2080  006012  012767  006064  011424        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2081  006020  012777  004000  011354        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2082  006026  016703  011354                MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
2083  006032  012705  010000                MOV     #10000,R5                       ;BIT 14 WILL BE SET IN LINE PARAMETER
2084  006036  010513                        MOV     R5,(R3)                 ;SET BIT 14
2085  006040  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2086  006042  020504                        CMP     R5,R4                   ;WAS BIT 14 SET
2087  006044  001401                        BEQ     1$
2088  006046  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2089  006050  040513              1$:       BIC     R5,(R3)                 ;CLEAR BIT 14
2090  006052  011304                        MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
2091  006054  005704                        TST     R4                      ;WAS BIT 14 CLEARED
2092  006056  001402                        BEQ     2$
2093  006060  005005                        CLR     R5
2094  006062  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2095  006064  104400              2$:       SCOPE
2096
2097                                        ;LINE PARAMETER REGISTER DATA TEST
2098                                        ;SET BIT 15 IN LINE PARAMETER TO 1
2099                                        ;VERIFY THAT BIT 15 WAS SET
2100                                        ;CLEAR BIT 15
2101                                        ;VERIFY THAT BIT 15 WAS CLEARED
2102
2103  006066  012767  000340  171702  T54:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2104  006074  012767  004000  011346        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2105  006102  012767  006154  011334        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2106  006110  012777  004000  011264        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2107  006116  016703  011264                MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
2108  006122  012705  020000                MOV     #20000,R5                       ;BIT 15 WILL BE SET IN LINE PARAMETER
2109  006126  010513                        MOV     R5,(R3)                 ;SET BIT 15
2110  006130  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2111  006132  020504                        CMP     R5,R4                   ;WAS BIT 15 SET
2112  006134  001401                        BEQ     1$
2113  006136  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2114  006140  040513              1$:       BIC     R5,(R3)                 ;CLEAR BIT 15
2115  006142  011304                        MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
2116  006144  005704                        TST     R4                      ;WAS BIT 15 CLEARED
2117  006146  001402                        BEQ     2$
2118  006150  005005                        CLR     R5
2119  006152  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2120  006154  104400              2$:       SCOPE
2121
2122                                        ;LINE PARAMETER REGISTER DATA TEST
2123                                        ;SET BIT 16 IN LINE PARAMETER TO 1
```

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2124                                            ;VERIFY THAT BIT 16 WAS SET
2125                                            ;CLEAR BIT 16
2126                                            ;VERIFY THAT BIT 16 WAS CLEARED
2127
2128  006156  012767  000340  171612  T55:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2129  006164  012767  004000  011256          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2130  006172  012767  006244  011244          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2131  006200  012777  004000  011174          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2132  006206  016703  011174                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
2133  006212  012705  040000                  MOV     #40000,R5                       ;BIT 16 WILL BE SET IN LINE PARAMETER
2134  006216  010513                          MOV     R5,(R3)                 ;SET BIT 16
2135  006220  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2136  006222  020504                          CMP     R5,R4                   ;WAS BIT 16 SET
2137  006224  001401                          BEQ     1$
2138  006226  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2139  006230  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 16
2140  006232  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
2141  006234  005704                          TST     R4                      ;WAS BIT 16 CLEARED
2142  006236  001402                          BEQ     2$
2143  006240  005005                          CLR     R5
2144  006242  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2145  006244  104400                  2$:     SCOPE
2146
2147                                            ;LINE PARAMETER REGISTER DATA TEST
2148                                            ;SET BIT 17 IN LINE PARAMETER TO 1
2149                                            ;VERIFY THAT BIT 17 WAS SET
2150                                            ;CLEAR BIT 17
2151                                            ;VERIFY THAT BIT 17 WAS CLEARED
2152
2153  006246  012767  000340  171522  T56:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2154  006254  012767  004000  011166          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2155  006262  012767  006334  011154          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2156  006270  012777  004000  011104          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2157  006276  016703  011104                  MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
2158  006302  012705  100000                  MOV     #100000,R5                      ;BIT 17 WILL BE SET IN LINE PARAMETER
2159  006306  010513                          MOV     R5,(R3)                 ;SET BIT 17
2160  006310  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2161  006312  020504                          CMP     R5,R4                   ;WAS BIT 17 SET
2162  006314  001401                          BEQ     1$
2163  006316  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2164  006320  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 17
2165  006322  011304                          MOV     (R3),R4                 ;READ CONTENTS OF LINE PARAMETER
2166  006324  005704                          TST     R4                      ;WAS BIT 17 CLEARED
2167  006326  001402                          BEQ     2$
2168  006330  005005                          CLR     R5
2169  006332  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2170  006334  104400                  2$:     SCOPE
2171
2172                                            ;BREAK CONTROL REGISTER DATA TEST
2173                                            ;SET BIT 0 IN BREAK CONTROL TO 1
2174                                            ;VERIFY THAT BIT 0 WAS SET
2175                                            ;CLEAR BIT 0
2176                                            ;VERIFY THAT BIT 0 WAS CLEARED
2177
2178  006336  012767  000340  171432  T57:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2179  006344  012767  004000  011076          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
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2180  006352  012767  006424  011064          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2181  006360  012777  004000  011014          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2182  006366  016703  011024                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2183  006372  012705  000001                  MOV     #1,R5                   ;BIT 0 WILL BE SET IN BREAK CONTROL
2184  006376  010513                          MOV     R5,(R3)                 ;SET BIT 0
2185  006400  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2186  006402  020504                          CMP     R5,R4                   ;WAS BIT 0 SET
2187  006404  001401                          BEQ     1$
2188  006406  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2189  006410  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 0
2190  006412  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2191  006414  005704                          TST     R4                      ;WAS BIT 0 CLEARED
2192  006416  001402                          BEQ     2$
2193  006420  005005                          CLR     R5
2194  006422  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2195  006424  104400                  2$:     SCOPE
2196
2197                                          ;BREAK CONTROL REGISTER DATA TEST
2198                                          ;SET BIT 1 IN BREAK CONTROL TO 1
2199                                          ;VERIFY THAT BIT 1 WAS SET
2200                                          ;CLEAR BIT 1
2201                                          ;VERIFY THAT BIT 1 WAS CLEARED
2202
2203  006426  012767  000340  171342  T60:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2204  006434  012767  004000  011006          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2205  006442  012767  006514  010774          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2206  006450  012777  004000  010724          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2207  006456  016703  010734                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2208  006462  012705  000002                  MOV     #2,R5                   ;BIT 1 WILL BE SET IN BREAK CONTROL
2209  006466  010513                          MOV     R5,(R3)                 ;SET BIT 1
2210  006470  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2211  006472  020504                          CMP     R5,R4                   ;WAS BIT 1 SET
2212  006474  001401                          BEQ     1$
2213  006476  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2214  006500  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 1
2215  006502  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2216  006504  005704                          TST     R4                      ;WAS BIT 1 CLEARED
2217  006506  001402                          BEQ     2$
2218  006510  005005                          CLR     R5
2219  006512  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2220  006514  104400                  2$:     SCOPE
2221
2222                                          ;BREAK CONTROL REGISTER DATA TEST
2223                                          ;SET BIT 2 IN BREAK CONTROL TO 1
2224                                          ;VERIFY THAT BIT 2 WAS SET
2225                                          ;CLEAR BIT 2
2226                                          ;VERIFY THAT BIT 2 WAS CLEARED
2227
2228  006516  012767  000340  171252  T61:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2229  006524  012767  004000  010716          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2230  006532  012767  006604  010704          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2231  006540  012777  004000  010634          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2232  006546  016703  010644                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2233  006552  012705  000004                  MOV     #4,R5                   ;BIT 2 WILL BE SET IN BREAK CONTROL
2234  006556  010513                          MOV     R5,(R3)                 ;SET BIT 2
2235  006560  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
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2236  006562  020504                        CMP     R5,R4                   ;WAS BIT 2 SET
2237  006564  001401                        BEQ     1$
2238  006566  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2239  006570  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 2
2240  006572  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2241  006574  005704                        TST     R4                      ;WAS BIT 2 CLEARED
2242  006576  001402                        BEQ     2$
2243  006600  005005                        CLR     R5
2244  006602  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2245  006604  104400                2$:     SCOPE
2246
2247                                        ;BREAK CONTROL REGISTER DATA TEST
2248                                        ;SET BIT 3 IN BREAK CONTROL TO 1
2249                                        ;VERIFY THAT BIT 3 WAS SET
2250                                        ;CLEAR BIT 3
2251                                        ;VERIFY THAT BIT 3 WAS CLEARED
2252
2253  006606  012767  000340  171162 T62:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2254  006614  012767  004000  010626        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2255  006622  012767  006674  010614        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2256  006630  012777  004000  010544        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2257  006636  016703  010554                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2258  006642  012705  000010                MOV     #10,R5                  ;BIT 3 WILL BE SET IN BREAK CONTROL
2259  006646  010513                        MOV     R5,(R3)                 ;SET BIT 3
2260  006650  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2261  006652  020504                        CMP     R5,R4                   ;WAS BIT 3 SET
2262  006654  001401                        BEQ     1$
2263  006656  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2264  006660  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 3
2265  006662  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2266  006664  005704                        TST     R4                      ;WAS BIT 3 CLEARED
2267  006666  001402                        BEQ     2$
2268  006670  005005                        CLR     R5
2269  006672  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2270  006674  104400                2$:     SCOPE
2271
2272                                        ;BREAK CONTROL REGISTER DATA TEST
2273                                        ;SET BIT 4 IN BREAK CONTROL TO 1
2274                                        ;VERIFY THAT BIT 4 WAS SET
2275                                        ;CLEAR BIT 4
2276                                        ;VERIFY THAT BIT 4 WAS CLEARED
2277
2278  006676  012767  000340  171072 T63:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2279  006704  012767  004000  010536        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2280  006712  012767  006764  010524        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2281  006720  012777  004000  010454        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2282  006726  016703  010464                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2283  006732  012705  000020                MOV     #20,R5                  ;BIT 4 WILL BE SET IN BREAK CONTROL
2284  006736  010513                        MOV     R5,(R3)                 ;SET BIT 4
2285  006740  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2286  006742  020504                        CMP     R5,R4                   ;WAS BIT 4 SET
2287  006744  001401                        BEQ     1$
2288  006746  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2289  006750  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 4
2290  006752  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2291  006754  005704                        TST     R4                      ;WAS BIT 4 CLEARED
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2292  006756  001402                        BEQ     2$
2293  006760  005005                        CLR     R5
2294  006762  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2295  006764  104400              2$:       SCOPE
2296
2297                                        ;BREAK CONTROL REGISTER DATA TEST
2298                                        ;SET BIT 5 IN BREAK CONTROL TO 1
2299                                        ;VERIFY THAT BIT 5 WAS SET
2300                                        ;CLEAR BIT 5
2301                                        ;VERIFY THAT BIT 5 WAS CLEARED
2302
2303  006766  012767  000340  171002  T64:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2304  006774  012767  004000  010446        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2305  007002  012767  007054  010434        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2306  007010  012777  004000  010364        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2307  007016  016703  010374                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2308  007022  012705  000040                MOV     #40,R5                  ;BIT 5 WILL BE SET IN BREAK CONTROL
2309  007026  010513                        MOV     R5,(R3)                 ;SET BIT 5
2310  007030  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2311  007032  020504                        CMP     R5,R4                   ;WAS BIT 5 SET
2312  007034  001401                        BEQ     1$
2313  007036  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2314  007040  040513              1$:       BIC     R5,(R3)                 ;CLEAR BIT 5
2315  007042  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2316  007044  005704                        TST     R4                      ;WAS BIT 5 CLEARED
2317  007046  001402                        BEQ     2$
2318  007050  005005                        CLR     R5
2319  007052  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2320  007054  104400              2$:       SCOPE
2321
2322                                        ;BREAK CONTROL REGISTER DATA TEST
2323                                        ;SET BIT 6 IN BREAK CONTROL TO 1
2324                                        ;VERIFY THAT BIT 6 WAS SET
2325                                        ;CLEAR BIT 6
2326                                        ;VERIFY THAT BIT 6 WAS CLEARED
2327
2328  007056  012767  000340  170712  T65:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2329  007064  012767  004000  010356        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2330  007072  012767  007144  010344        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2331  007100  012777  004000  010274        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2332  007106  016703  010304                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2333  007112  012705  000100                MOV     #100,R5                 ;BIT 6 WILL BE SET IN BREAK CONTROL
2334  007116  010513                        MOV     R5,(R3)                 ;SET BIT 6
2335  007120  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2336  007122  020504                        CMP     R5,R4                   ;WAS BIT 6 SET
2337  007124  001401                        BEQ     1$
2338  007126  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2339  007130  040513              1$:       BIC     R5,(R3)                 ;CLEAR BIT 6
2340  007132  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2341  007134  005704                        TST     R4                      ;WAS BIT 6 CLEARED
2342  007136  001402                        BEQ     2$
2343  007140  005005                        CLR     R5
2344  007142  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2345  007144  104400              2$:       SCOPE
2346
2347                                        ;BREAK CONTROL REGISTER DATA TEST
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                                        ;SET BIT 7 IN BREAK CONTROL TO 1
                                        ;VERIFY THAT BIT 7 WAS SET
                                        ;CLEAR BIT 7
                                        ;VERIFY THAT BIT 7 WAS CLEARED
                                        
007146  012767  000340  170622  T66:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
007154  012767  004000  010266        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
007162  012767  007234  010254        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
007170  012777  004000  010204        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
007176  016703  010214                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
007202  012705  000200                MOV     #200,R5                 ;BIT 7 WILL BE SET IN BREAK CONTROL
007206  010513                        MOV     R5,(R3)                 ;SET BIT 7
007210  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
007212  020504                        CMP     R5,R4                   ;WAS BIT 7 SET
007214  001401                        BEQ     1$
007216  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
007220  040513                1$:   BIC     R5,(R3)                 ;CLEAR BIT 7
007222  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
007224  005704                        TST     R4                      ;WAS BIT 7 CLEARED
007226  001402                        BEQ     2$
007230  005005                        CLR     R5
007232  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
007234  104400                2$:   SCOPE
                                        
                                        ;BREAK CONTROL REGISTER DATA TEST
                                        ;SET BIT 10 IN BREAK CONTROL TO 1
                                        ;VERIFY THAT BIT 10 WAS SET
                                        ;CLEAR BIT 10
                                        ;VERIFY THAT BIT 10 WAS CLEARED
                                        
007236  012767  000340  170532  T67:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
007244  012767  004000  010176        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
007252  012767  007324  010164        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
007260  012777  004000  010114        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
007266  016703  010124                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
007272  012705  000400                MOV     #400,R5                 ;BIT 10 WILL BE SET IN BREAK CONTROL
007276  010513                        MOV     R5,(R3)                 ;SET BIT 10
007300  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
007302  020504                        CMP     R5,R4                   ;WAS BIT 10 SET
007304  001401                        BEQ     1$
007306  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
007310  040513                1$:   BIC     R5,(R3)                 ;CLEAR BIT 10
007312  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
007314  005704                        TST     R4                      ;WAS BIT 10 CLEARED
007316  001402                        BEQ     2$
007320  005005                        CLR     R5
007322  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
007324  104400                2$:   SCOPE
                                        
                                        ;BREAK CONTROL REGISTER DATA TEST
                                        ;SET BIT 11 IN BREAK CONTROL TO 1
                                        ;VERIFY THAT BIT 11 WAS SET
                                        ;CLEAR BIT 11
                                        ;VERIFY THAT BIT 11 WAS CLEARED
                                        
007326  012767  000340  170442  T70:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
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2404  007334  012767  004000  010106          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2405  007342  012767  007414  010074          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2406  007350  012777  004000  010024          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2407  007356  016703  010034                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2408  007362  012705  001000                  MOV     #1000,R5                        ;BIT 11 WILL BE SET IN BREAK CONTROL
2409  007366  010513                          MOV     R5,(R3)                 ;SET BIT 11
2410  007370  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2411  007372  020504                          CMP     R5,R4                   ;WAS BIT 11 SET
2412  007374  001401                          BEQ     1$
2413  007376  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2414  007400  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 11
2415  007402  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2416  007404  005704                          TST     R4                      ;WAS BIT 11 CLEARED
2417  007406  001402                          BEQ     2$
2418  007410  005005                          CLR     R5
2419  007412  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2420  007414  104400                  2$:     SCOPE
2421
2422                                          ;BREAK CONTROL REGISTER DATA TEST
2423                                          ;SET BIT 12 IN BREAK CONTROL TO 1
2424                                          ;VERIFY THAT BIT 12 WAS SET
2425                                          ;CLEAR BIT 12
2426                                          ;VERIFY THAT BIT 12 WAS CLEARED
2427
2428  007416  012767  000340  170352  T71:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2429  007424  012767  004000  010016          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2430  007432  012767  007504  010004          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2431  007440  012777  004000  007734          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2432  007446  016703  007744                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2433  007452  012705  002000                  MOV     #2000,R5                        ;BIT 12 WILL BE SET IN BREAK CONTROL
2434  007456  010513                          MOV     R5,(R3)                 ;SET BIT 12
2435  007460  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2436  007462  020504                          CMP     R5,R4                   ;WAS BIT 12 SET
2437  007464  001401                          BEQ     1$
2438  007466  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2439  007470  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 12
2440  007472  011304                          MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2441  007474  005704                          TST     R4                      ;WAS BIT 12 CLEARED
2442  007476  001402                          BEQ     2$
2443  007500  005005                          CLR     R5
2444  007502  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
2445  007504  104400                  2$:     SCOPE
2446
2447                                          ;BREAK CONTROL REGISTER DATA TEST
2448                                          ;SET BIT 13 IN BREAK CONTROL TO 1
2449                                          ;VERIFY THAT BIT 13 WAS SET
2450                                          ;CLEAR BIT 13
2451                                          ;VERIFY THAT BIT 13 WAS CLEARED
2452
2453  007506  012767  000340  170262  T72:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2454  007514  012767  004000  007726          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2455  007522  012767  007574  007714          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2456  007530  012777  004000  007644          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2457  007536  016703  007654                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2458  007542  012705  004000                  MOV     #4000,R5                        ;BIT 13 WILL BE SET IN BREAK CONTROL
2459  007546  010513                          MOV     R5,(R3)                 ;SET BIT 13
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2460  007550  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2461  007552  020504                        CMP     R5,R4                   ;WAS BIT 13 SET
2462  007554  001401                        BEQ     1$
2463  007556  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2464  007560  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 13
2465  007562  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2466  007564  005704                        TST     R4                      ;WAS BIT 13 CLEARED
2467  007566  001402                        BEQ     2$
2468  007570  005005                        CLR     R5
2469  007572  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2470  007574  104400                2$:     SCOPE
2471
2472                                        ;BREAK CONTROL REGISTER DATA TEST
2473                                        ;SET BIT 14 IN BREAK CONTROL TO 1
2474                                        ;VERIFY THAT BIT 14 WAS SET
2475                                        ;CLEAR BIT 14
2476                                        ;VERIFY THAT BIT 14 WAS CLEARED
2477
2478  007576  012767  000340  170172  T73:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2479  007604  012767  004000  007636        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2480  007612  012767  007664  007624        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2481  007620  012777  004000  007554        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2482  007626  016703  007564                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2483  007632  012705  010000                MOV     #10000,R5                       ;BIT 14 WILL BE SET IN BREAK CONTROL
2484  007636  010513                        MOV     R5,(R3)                 ;SET BIT 14
2485  007640  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2486  007642  020504                        CMP     R5,R4                   ;WAS BIT 14 SET
2487  007644  001401                        BEQ     1$
2488  007646  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2489  007650  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 14
2490  007652  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2491  007654  005704                        TST     R4                      ;WAS BIT 14 CLEARED
2492  007656  001402                        BEQ     2$
2493  007660  005005                        CLR     R5
2494  007662  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2495  007664  104400                2$:     SCOPE
2496
2497                                        ;BREAK CONTROL REGISTER DATA TEST
2498                                        ;SET BIT 15 IN BREAK CONTROL TO 1
2499                                        ;VERIFY THAT BIT 15 WAS SET
2500                                        ;CLEAR BIT 15
2501                                        ;VERIFY THAT BIT 15 WAS CLEARED
2502
2503  007666  012767  000340  170102  T74:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2504  007674  012767  004000  007546        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2505  007702  012767  007754  007534        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2506  007710  012777  004000  007464        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2507  007716  016703  007474                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2508  007722  012705  020000                MOV     #20000,R5                       ;BIT 15 WILL BE SET IN BREAK CONTROL
2509  007726  010513                        MOV     R5,(R3)                 ;SET BIT 15
2510  007730  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2511  007732  020504                        CMP     R5,R4                   ;WAS BIT 15 SET
2512  007734  001401                        BEQ     1$
2513  007736  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2514  007740  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 15
2515  007742  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
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2516  007744  005704                        TST     R4                      ;WAS BIT 15 CLEARED
2517  007746  001402                        BEQ     2$
2518  007750  005005                        CLR     R5
2519  007752  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2520  007754  104400              2$:       SCOPE
2521
2522                                        ;BREAK CONTROL REGISTER DATA TEST
2523                                        ;SET BIT 16 IN BREAK CONTROL TO 1
2524                                        ;VERIFY THAT BIT 16 WAS SET
2525                                        ;CLEAR BIT 16
2526                                        ;VERIFY THAT BIT 16 WAS CLEARED
2527
2528  007756  012767  000340  170012  T75:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2529  007764  012767  004000  007456        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2530  007772  012767  010044  007444        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2531  010000  012777  004000  007374        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2532  010006  016703  007404                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2533  010012  012705  040000                MOV     #40000,R5                       ;BIT 16 WILL BE SET IN BREAK CONTROL
2534  010016  010513                        MOV     R5,(R3)                 ;SET BIT 16
2535  010020  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2536  010022  020504                        CMP     R5,R4                   ;WAS BIT 16 SET
2537  010024  001401                        BEQ     1$
2538  010026  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2539  010030  040513              1$:       BIC     R5,(R3)                 ;CLEAR BIT 16
2540  010032  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2541  010034  005704                        TST     R4                      ;WAS BIT 16 CLEARED
2542  010036  001402                        BEQ     2$
2543  010040  005005                        CLR     R5
2544  010042  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2545  010044  104400              2$:       SCOPE
2546
2547                                        ;BREAK CONTROL REGISTER DATA TEST
2548                                        ;SET BIT 17 IN BREAK CONTROL TO 1
2549                                        ;VERIFY THAT BIT 17 WAS SET
2550                                        ;CLEAR BIT 17
2551                                        ;VERIFY THAT BIT 17 WAS CLEARED
2552
2553  010046  012767  000340  167722  T76:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2554  010054  012767  004000  007366        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2555  010062  012767  010134  007354        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2556  010070  012777  004000  007304        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2557  010076  016703  007314                MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
2558  010102  012705  100000                MOV     #100000,R5                      ;BIT 17 WILL BE SET IN BREAK CONTROL
2559  010106  010513                        MOV     R5,(R3)                 ;SET BIT 17
2560  010110  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
2561  010112  020504                        CMP     R5,R4                   ;WAS BIT 17 SET
2562  010114  001401                        BEQ     1$
2563  010116  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2564  010120  040513              1$:       BIC     R5,(R3)                 ;CLEAR BIT 17
2565  010122  011304                        MOV     (R3),R4                 ;READ CONTENTS OF BREAK CONTROL
2566  010124  005704                        TST     R4                      ;WAS BIT 17 CLEARED
2567  010126  001402                        BEQ     2$
2568  010130  005005                        CLR     R5
2569  010132  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
2570  010134  104400              2$:       SCOPE
2571
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2572                                            ;SILO STATUS REGISTER DATA TEST
2573                                            ;SET BIT 0 IN SILO STATUS TO 1
2574                                            ;VERIFY THAT BIT 0 WAS SET
2575                                            ;CLEAR BIT 0
2576                                            ;VERIFY THAT BIT 0 WAS CLEARED
2577
2578  010136  012767  000340  167632  T77:    MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2579  010144  012767  004000  007276          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2580  010152  012767  010234  007264          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2581  010160  012777  004000  007214          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2582  010166  016703  007226                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2583  010172  012705  000001                  MOV     #1,R5                   ;BIT 0 WILL BE SET IN SILO STATUS
2584  010176  010513                          MOV     R5,(R3)                 ;SET BIT 0
2585  010200  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2586  010202  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2587  010206  020504                          CMP     R5,R4                   ;WAS BIT 0 SET
2588  010210  001401                          BEQ     1$
2589  010212  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2590  010214  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 0
2591  010216  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2592  010220  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2593  010224  005704                          TST     R4                      ;WAS BIT 0 CLEARED
2594  010226  001402                          BEQ     2$
2595  010230  005005                          CLR     R5
2596  010232  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2597  010234  104400                  2$:     SCOPE
2598
2599                                            ;SILO STATUS REGISTER DATA TEST
2600                                            ;SET BIT 1 IN SILO STATUS TO 1
2601                                            ;VERIFY THAT BIT 1 WAS SET
2602                                            ;CLEAR BIT 1
2603                                            ;VERIFY THAT BIT 1 WAS CLEARED
2604
2605  010236  012767  000340  167532  T100:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2606  010244  012767  004000  007176          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2607  010252  012767  010334  007164          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2608  010260  012777  004000  007114          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2609  010266  016703  007126                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2610  010272  012705  000002                  MOV     #2,R5                   ;BIT 1 WILL BE SET IN SILO STATUS
2611  010276  010513                          MOV     R5,(R3)                 ;SET BIT 1
2612  010300  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2613  010302  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2614  010306  020504                          CMP     R5,R4                   ;WAS BIT 1 SET
2615  010310  001401                          BEQ     1$
2616  010312  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2617  010314  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 1
2618  010316  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2619  010320  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2620  010324  005704                          TST     R4                      ;WAS BIT 1 CLEARED
2621  010326  001402                          BEQ     2$
2622  010330  005005                          CLR     R5
2623  010332  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2624  010334  104400                  2$:     SCOPE
2625
2626                                            ;SILO STATUS REGISTER DATA TEST
2627                                            ;SET BIT 2 IN SILO STATUS TO 1
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2628                                            ;VERIFY THAT BIT 2 WAS SET
2629                                            ;CLEAR BIT 2
2630                                            ;VERIFY THAT BIT 2 WAS CLEARED
2631
2632  010336  012767  000340  167432  T101:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2633  010344  012767  004000  007076          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2634  010352  012767  010434  007064          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2635  010360  012777  004000  007014          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2636  010366  016703  007026                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2637  010372  012705  000004                  MOV     #4,R5                   ;BIT 2 WILL BE SET IN SILO STATUS
2638  010376  010513                          MOV     R5,(R3)                 ;SET BIT 2
2639  010400  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2640  010402  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2641  010406  020504                          CMP     R5,R4                   ;WAS BIT 2 SET
2642  010410  001401                          BEQ     1$
2643  010412  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2644  010414  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 2
2645  010416  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2646  010420  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2647  010424  005704                          TST     R4                      ;WAS BIT 2 CLEARED
2648  010426  001402                          BEQ     2$
2649  010430  005005                          CLR     R5
2650  010432  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2651  010434  104400                  2$:     SCOPE
2652
2653                                            ;SILO STATUS REGISTER DATA TEST
2654                                            ;SET BIT 3 IN SILO STATUS TO 1
2655                                            ;VERIFY THAT BIT 3 WAS SET
2656                                            ;CLEAR BIT 3
2657                                            ;VERIFY THAT BIT 3 WAS CLEARED
2658
2659  010436  012767  000340  167332  T102:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2660  010444  012767  004000  006776          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2661  010452  012767  010534  006764          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2662  010460  012777  004000  006714          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2663  010466  016703  006726                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2664  010472  012705  000010                  MOV     #10,R5                  ;BIT 3 WILL BE SET IN SILO STATUS
2665  010476  010513                          MOV     R5,(R3)                 ;SET BIT 3
2666  010500  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2667  010502  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2668  010506  020504                          CMP     R5,R4                   ;WAS BIT 3 SET
2669  010510  001401                          BEQ     1$
2670  010512  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2671  010514  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 3
2672  010516  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2673  010520  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2674  010524  005704                          TST     R4                      ;WAS BIT 3 CLEARED
2675  010526  001402                          BEQ     2$
2676  010530  005005                          CLR     R5
2677  010532  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2678  010534  104400                  2$:     SCOPE
2679
2680                                            ;SILO STATUS REGISTER DATA TEST
2681                                            ;SET BIT 4 IN SILO STATUS TO 1
2682                                            ;VERIFY THAT BIT 4 WAS SET
2683                                            ;CLEAR BIT 4
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                                        ;VERIFY THAT BIT 4 WAS CLEARED
                                        
010536  012767  000340  167232  T103: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
010544  012767  004000  006676        MOV     #4000.,ICOUNT           ;SET UP FOR 4000 ITERATIONS
010552  012767  010634  006664        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
010560  012777  004000  006614        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
010566  016703  006626                MOV     DHSCR,R3                ;SET UP POINTER TO SILO STATUS
010572  012705  000020                MOV     #20,R5                  ;BIT 4 WILL BE SET IN SILO STATUS
010576  010513                        MOV     R5,(R3)                 ;SET BIT 4
010600  011304                        MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
010602  042704  000700                BIC     #700,R4         ;CLEAR UNWANTED BITS
010606  020504                        CMP     R5,R4                   ;WAS BIT 4 SET
010610  001401                        BEQ     1$
010612  104004                        HLT     4                       ;SILO STATUS REGISTER ERROR
010614  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 4
010616  011304                        MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
010620  042704  000700                BIC     #700,R4         ;CLEAR UNWANTED BITS
010624  005704                        TST     R4                      ;WAS BIT 4 CLEARED
010626  001402                        BEQ     2$
010630  005005                        CLR     R5
010632  104004                        HLT     4                       ;SILO STATUS REGISTER ERROR
010634  104400                2$:     SCOPE
                                        
                                        ;SILO STATUS REGISTER DATA TEST
                                        ;SET BIT 5 IN SILO STATUS TO 1
                                        ;VERIFY THAT BIT 5 WAS SET
                                        ;CLEAR BIT 5
                                        ;VERIFY THAT BIT 5 WAS CLEARED
                                        
010636  012767  000340  167132  T104: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
010644  012767  004000  006576        MOV     #4000.,ICOUNT           ;SET UP FOR 4000 ITERATIONS
010652  012767  010734  006564        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
010660  012777  004000  006514        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
010666  016703  006526                MOV     DHSCR,R3                ;SET UP POINTER TO SILO STATUS
010672  012705  000040                MOV     #40,R5                  ;BIT 5 WILL BE SET IN SILO STATUS
010676  010513                        MOV     R5,(R3)                 ;SET BIT 5
010700  011304                        MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
010702  042704  000700                BIC     #700,R4         ;CLEAR UNWANTED BITS
010706  020504                        CMP     R5,R4                   ;WAS BIT 5 SET
010710  001401                        BEQ     1$
010712  104004                        HLT     4                       ;SILO STATUS REGISTER ERROR
010714  040513                1$:     BIC     R5,(R3)                 ;CLEAR BIT 5
010716  011304                        MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
010720  042704  000700                BIC     #700,R4         ;CLEAR UNWANTED BITS
010724  005704                        TST     R4                      ;WAS BIT 5 CLEARED
010726  001402                        BEQ     2$
010730  005005                        CLR     R5
010732  104004                        HLT     4                       ;SILO STATUS REGISTER ERROR
010734  104400                2$:     SCOPE
                                        
                                        ;SILO STATUS REGISTER DATA TEST
                                        ;SET BIT 17 IN SILO STATUS TO 1
                                        ;VERIFY THAT BIT 17 WAS SET
                                        ;CLEAR BIT 17
                                        ;VERIFY THAT BIT 17 WAS CLEARED
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2740  010736  012767  000340  167032  T105:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2741  010744  012767  004000  006476         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2742  010752  012767  011034  006464         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2743  010760  012777  004000  006414         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2744  010766  016703  006426                  MOV     DHSSR,R3                ;SET UP POINTER TO SILO STATUS
2745  010772  012705  100000                  MOV     #100000,R5                      ;BIT 17 WILL BE SET IN SILO STATUS
2746  010776  010513                          MOV     R5,(R3)                 ;SET BIT 17
2747  011000  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
2748  011002  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2749  011006  020504                          CMP     R5,R4                   ;WAS BIT 17 SET
2750  011010  001401                          BEQ     1$
2751  011012  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2752  011014  040513                  1$:     BIC     R5,(R3)                 ;CLEAR BIT 17
2753  011016  011304                          MOV     (R3),R4                 ;READ CONTENTS OF SILO STATUS
2754  011020  042704  000700                  BIC     #700,R4         ;CLEAR UNWANTED BITS
2755  011024  005704                          TST     R4                      ;WAS BIT 17 CLEARED
2756  011026  001402                          BEQ     2$
2757  011030  005005                          CLR     R5
2758  011032  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
2759  011034  104400                  2$:     SCOPE
2760
2761                                          ;LINE PARAMETER REGISTER DATA TEST
2762                                          ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2763                                          ;CLEAR BIT 0
2764                                          ;VERIFY THAT BIT 0 WAS CLEARED
2765                                          ;RESTORE BIT 0
2766                                          ;VERIFY THAT BIT 0 WAS SET
2767
2768  011036  012767  000340  166732  T106:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2769  011044  012767  004000  006376         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2770  011052  012767  011140  006364         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2771  011060  012777  004000  006314         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2772  011066  016703  006314                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2773  011072  012705  177766                  MOV     #177766,R5              ;(R5)=EXPECTED DATA
2774                                                                           ;IN LINE PARAMETER REGISTER, 177766
2775  011076  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2776                                                                           ;IN LINE PARAMETER REGISTER
2777  011102  042713  000001                  BIC     #1,(R3)         ;CLEAR BIT 0
2778  011106  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2779  011110  020504                          CMP     R5,R4                   ;WAS BIT 0 CLEARED
2780  011112  001401                          BEQ     1$
2781  011114  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2782  011116  052713  000001          1$:     BIS     #1,(R3)         ;SET BIT 0
2783  011122  011304                          MOV     (R3),R4
2784  011124  022704  177767                  CMP     #177767,R4              ;WAS BIT 0 SET
2785  011130  001403                          BEQ     2$
2786  011132  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2787                                                                           ;LINE PARAMETER REGISTER, 177767
2788  011136  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2789  011140  104400                  2$:     SCOPE
2790
2791                                          ;LINE PARAMETER REGISTER DATA TEST
2792                                          ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2793                                          ;CLEAR BIT 1
2794                                          ;VERIFY THAT BIT 1 WAS CLEARED
2795                                          ;RESTORE BIT 1
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2796                                            ;VERIFY THAT BIT 1 WAS SET
2797
2798  011142  012767  000340  166626  T107:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2799  011150  012767  004000  006272          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2800  011156  012767  011244  006260          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2801  011164  012777  004000  006210          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2802  011172  016703  006210                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2803  011176  012705  177765                  MOV     #177765,R5              ;(R5)=EXPECTED DATA
2804                                                                          ;IN LINE PARAMETER REGISTER, 177765
2805  011202  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2806                                                                          ;IN LINE PARAMETER REGISTER
2807  011206  042713  000002                  BIC     #2,(R3)         ;CLEAR BIT 1
2808  011212  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2809  011214  020504                          CMP     R5,R4                   ;WAS BIT 1 CLEARED
2810  011216  001401                          BEQ     1$
2811  011220  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2812  011222  052713  000002          1$:     BIS     #2,(R3)         ;SET BIT 1
2813  011226  011304                          MOV     (R3),R4
2814  011230  022704  177767                  CMP     #177767,R4              ;WAS BIT 1 SET
2815  011234  001403                          BEQ     2$
2816  011236  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2817                                                                          ;LINE PARAMETER REGISTER, 177767
2818  011242  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2819  011244  104400                  2$:     SCOPE
2820
2821                                            ;LINE PARAMETER REGISTER DATA TEST
2822                                            ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2823                                            ;CLEAR BIT 2
2824                                            ;VERIFY THAT BIT 2 WAS CLEARED
2825                                            ;RESTORE BIT 2
2826                                            ;VERIFY THAT BIT 2 WAS SET
2827
2828  011246  012767  000340  166522  T110:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2829  011254  012767  004000  006166          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2830  011262  012767  011350  006154          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2831  011270  012777  004000  006104          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2832  011276  016703  006104                  MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2833  011302  012705  177763                  MOV     #177763,R5              ;(R5)=EXPECTED DATA
2834                                                                          ;IN LINE PARAMETER REGISTER, 177763
2835  011306  012713  177767                  MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2836                                                                          ;IN LINE PARAMETER REGISTER
2837  011312  042713  000004                  BIC     #4,(R3)         ;CLEAR BIT 2
2838  011316  011304                          MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2839  011320  020504                          CMP     R5,R4                   ;WAS BIT 2 CLEARED
2840  011322  001401                          BEQ     1$
2841  011324  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2842  011326  052713  000004          1$:     BIS     #4,(R3)         ;SET BIT 2
2843  011332  011304                          MOV     (R3),R4
2844  011334  022704  177767                  CMP     #177767,R4              ;WAS BIT 2 SET
2845  011340  001403                          BEQ     2$
2846  011342  012705  177767                  MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2847                                                                          ;LINE PARAMETER REGISTER, 177767
2848  011346  104002                          HLT     2                       ;LINE PARAMETER REGISTER ERROR
2849  011350  104400                  2$:     SCOPE
2850
2851                                            ;LINE PARAMETER REGISTER DATA TEST
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                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
                                        ;CLEAR BIT 4
                                        ;VERIFY THAT BIT 4 WAS CLEARED
                                        ;RESTORE BIT 4
                                        ;VERIFY THAT BIT 4 WAS SET

011352  012767  000340  166416  T111: MOV     #340,PS           ;DISABLE ALL INTERRUPTS
011360  012767  004000  006062        MOV     #4000,ICOUNT      ;SET UP FOR 4000 ITERATIONS
011366  012767  011454  006050        MOV     #2$,ESCAPE        ;SET UP TO ESCAPE TO NEXT TEST
011374  012777  004000  006000        MOV     #BIT11,@DHSCR     ;MASTER CLEAR INTERFACE
011402  016703  006000                MOV     DHLPR,R3                  ;SET UP POINTER TO LINE PARAMETER
011406  012705  177747                MOV     #177747,R5        ;(R5)=EXPECTED DATA
                                                                ;IN LINE PARAMETER REGISTER, 177747
011412  012713  177767                MOV     #177767,(R3)      ;SET ALL READ/WRITE BITS
                                                                ;IN LINE PARAMETER REGISTER
011416  042713  000020                BIC     #20,(R3)          ;CLEAR BIT 4
011422  011304                        MOV     (R3),R4           ;GET CONTENTS OF LINE PARAMETER
011424  020504                        CMP     R5,R4             ;WAS BIT 4 CLEARED
011426  001401                        BEQ     1$
011430  104002                        HLT     2                 ;LINE PARAMETER REGISTER ERROR
011432  052713  000020          1$:   BIS     #20,(R3)          ;SET BIT 4
011436  011304                        MOV     (R3),R4
011440  022704  177767                CMP     #177767,R4        ;WAS BIT 4 SET
011444  001403                        BEQ     2$
011446  012705  177767                MOV     #177767,R5        ;(R5)=EXPECTED DATA IN
                                                                ;LINE PARAMETER REGISTER, 177767
011452  104002                        HLT     2                 ;LINE PARAMETER REGISTER ERROR
011454  104400                2$:   SCOPE

                                        ;LINE PARAMETER REGISTER DATA TEST
                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
                                        ;CLEAR BIT 5
                                        ;VERIFY THAT BIT 5 WAS CLEARED
                                        ;RESTORE BIT 5
                                        ;VERIFY THAT BIT 5 WAS SET

011456  012767  000340  166312  T112: MOV     #340,PS           ;DISABLE ALL INTERRUPTS
011464  012767  004000  005756        MOV     #4000,ICOUNT      ;SET UP FOR 4000 ITERATIONS
011472  012767  011560  005744        MOV     #2$,ESCAPE        ;SET UP TO ESCAPE TO NEXT TEST
011500  012777  004000  005674        MOV     #BIT11,@DHSCR     ;MASTER CLEAR INTERFACE
011506  016703  005674                MOV     DHLPR,R3                  ;SET UP POINTER TO LINE PARAMETER
011512  012705  177727                MOV     #177727,R5        ;(R5)=EXPECTED DATA
                                                                ;IN LINE PARAMETER REGISTER, 177727
011516  012713  177767                MOV     #177767,(R3)      ;SET ALL READ/WRITE BITS
                                                                ;IN LINE PARAMETER REGISTER
011522  042713  000040                BIC     #40,(R3)          ;CLEAR BIT 5
011526  011304                        MOV     (R3),R4           ;GET CONTENTS OF LINE PARAMETER
011530  020504                        CMP     R5,R4             ;WAS BIT 5 CLEARED
011532  001401                        BEQ     1$
011534  104002                        HLT     2                 ;LINE PARAMETER REGISTER ERROR
011536  052713  000040          1$:   BIS     #40,(R3)          ;SET BIT 5
011542  011304                        MOV     (R3),R4
011544  022704  177767                CMP     #177767,R4        ;WAS BIT 5 SET
011550  001403                        BEQ     2$
011552  012705  177767                MOV     #177767,R5        ;(R5)=EXPECTED DATA IN
                                                                ;LINE PARAMETER REGISTER, 177767
```

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2908  011556  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2909  011560  104400              2$:       SCOPE
2910
2911                                        ;LINE PARAMETER REGISTER DATA TEST
2912                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2913                                        ;CLEAR BIT 6
2914                                        ;VERIFY THAT BIT 6 WAS CLEARED
2915                                        ;RESTORE BIT 6
2916                                        ;VERIFY THAT BIT 6 WAS SET
2917
2918  011562  012767  000340  166206  T113: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2919  011570  012767  004000  005652        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2920  011576  012767  011664  005640        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2921  011604  012777  004000  005570        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2922  011612  016703  005570                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2923  011616  012705  177667                MOV     #177667,R5              ;(R5)=EXPECTED DATA
2924                                                                        ;IN LINE PARAMETER REGISTER, 177667
2925  011622  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2926                                                                        ;IN LINE PARAMETER REGISTER
2927  011626  042713  000100                BIC     #100,(R3)               ;CLEAR BIT 6
2928  011632  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2929  011634  020504                        CMP     R5,R4                   ;WAS BIT 6 CLEARED
2930  011636  001401                        BEQ     1$
2931  011640  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2932  011642  052713  000100        1$:     BIS     #100,(R3)               ;SET BIT 6
2933  011646  011304                        MOV     (R3),R4
2934  011650  022704  177767                CMP     #177767,R4              ;WAS BIT 6 SET
2935  011654  001403                        BEQ     2$
2936  011656  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
2937                                                                        ;LINE PARAMETER REGISTER, 177767
2938  011662  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2939  011664  104400              2$:       SCOPE
2940
2941                                        ;LINE PARAMETER REGISTER DATA TEST
2942                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
2943                                        ;CLEAR BIT 7
2944                                        ;VERIFY THAT BIT 7 WAS CLEARED
2945                                        ;RESTORE BIT 7
2946                                        ;VERIFY THAT BIT 7 WAS SET
2947
2948  011666  012767  000340  166102  T114: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
2949  011674  012767  004000  005546        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
2950  011702  012767  011770  005534        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
2951  011710  012777  004000  005464        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
2952  011716  016703  005464                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
2953  011722  012705  177567                MOV     #177567,R5              ;(R5)=EXPECTED DATA
2954                                                                        ;IN LINE PARAMETER REGISTER, 177567
2955  011726  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
2956                                                                        ;IN LINE PARAMETER REGISTER
2957  011732  042713  000200                BIC     #200,(R3)               ;CLEAR BIT 7
2958  011736  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
2959  011740  020504                        CMP     R5,R4                   ;WAS BIT 7 CLEARED
2960  011742  001401                        BEQ     1$
2961  011744  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
2962  011746  052713  000200        1$:     BIS     #200,(R3)               ;SET BIT 7
2963  011752  011304                        MOV     (R3),R4
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 2964  011754  022704  177767              CMP     #177767,R4              ;WAS BIT 7 SET
 2965  011760  001403                      BEQ     2$
 2966  011762  012705  177767              MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
 2967                                                                      ;LINE PARAMETER REGISTER, 177767
 2968  011766  104002                      HLT     2                       ;LINE PARAMETER REGISTER ERRCR
 2969  011770  104400            2$:       SCOPE
 2970
 2971                                      ;LINE PARAMETER REGISTER DATA TEST
 2972                                      ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
 2973                                      ;CLEAR BIT 10
 2974                                      ;VERIFY THAT BIT 10 WAS CLEARED
 2975                                      ;RESTORE BIT 10
 2976                                      ;VERIFY THAT BIT 10 WAS SET
 2977
 2978  011772  012767  000340  165776  T115: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
 2979  012000  012767  004000  005442        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
 2980  012006  012767  012074  005430        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
 2981  012014  012777  004000  005360        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
 2982  012022  016703  005360                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
 2983  012026  012705  177367                MOV     #177367,R5              ;(R5)=EXPECTED DATA
 2984                                                                      ;IN LINE PARAMETER REGISTER, 177367
 2985  012032  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
 2986                                                                      ;IN LINE PARAMETER REGISTER
 2987  012036  042713  000400                BIC     #400,(R3)               ;CLEAR BIT 10
 2988  012042  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
 2989  012044  020504                        CMP     R5,R4                   ;WAS BIT 10 CLEARED
 2990  012046  001401                        BEQ     1$
 2991  012050  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
 2992  012052  052713  000400          1$:   BIS     #400,(R3)               ;SET BIT 10
 2993  012056  011304                        MOV     (R3),R4
 2994  012060  022704  177767                CMP     #177767,R4              ;WAS BIT 10 SET
 2995  012064  001403                        BEQ     2$
 2996  012066  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
 2997                                                                      ;LINE PARAMETER REGISTER, 177767
 2998  012072  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
 2999  012074  104400            2$:       SCOPE
 3000
 3001                                      ;LINE PARAMETER REGISTER DATA TEST
 3002                                      ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
 3003                                      ;CLEAR BIT 11
 3004                                      ;VERIFY THAT BIT 11 WAS CLEARED
 3005                                      ;RESTORE BIT 11
 3006                                      ;VERIFY THAT BIT 11 WAS SET
 3007
 3008  012076  012767  000340  165672  T116: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
 3009  012104  012767  004000  005336        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
 3010  012112  012767  012200  005324        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
 3011  012120  012777  004000  005254        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
 3012  012126  016703  005254                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
 3013  012132  012705  176767                MOV     #176767,R5              ;(R5)=EXPECTED DATA
 3014                                                                      ;IN LINE PARAMETER REGISTER, 176767
 3015  012136  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
 3016                                                                      ;IN LINE PARAMETER REGISTER
 3017  012142  042713  001000                BIC     #1000,(R3)              ;CLEAR BIT 11
 3018  012146  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
 3019  012150  020504                        CMP     R5,R4                   ;WAS BIT 11 CLEARED
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3020  012152  001401                        BEQ     1$
3021  012154  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3022  012156  052713  001000          1$:   BIS     #1000,(R3)              ;SET BIT 11
3023  012162  011304                        MOV     (R3),R4
3024  012164  022704  177767                CMP     #177767,R4              ;WAS BIT 11 SET
3025  012170  001403                        BEQ     2$
3026  012172  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
3027                                                                        ;LINE PARAMETER REGISTER, 177767
3028  012176  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3029  012200  104400          2$:   SCOPE
3030
3031                                ;LINE PARAMETER REGISTER DATA TEST
3032                                ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
3033                                ;CLEAR BIT 12
3034                                ;VERIFY THAT BIT 12 WAS CLEARED
3035                                ;RESTORE BIT 12
3036                                ;VERIFY THAT BIT 12 WAS SET
3037
3038  012202  012767  000340  165566  T117:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3039  012210  012767  004000  005232        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3040  012216  012767  012304  005220        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3041  012224  012777  004000  005150        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3042  012232  016703  005150                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
3043  012236  012705  175767                MOV     #175767,R5              ;(R5)=EXPECTED DATA
3044                                                                        ;IN LINE PARAMETER REGISTER, 175767
3045  012242  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
3046                                                                        ;IN LINE PARAMETER REGISTER
3047  012246  042713  002000                BIC     #2000,(R3)              ;CLEAR BIT 12
3048  012252  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
3049  012254  020504                        CMP     R5,R4                   ;WAS BIT 12 CLEARED
3050  012256  001401                        BEQ     1$
3051  012260  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3052  012262  052713  002000          1$:   BIS     #2000,(R3)              ;SET BIT 12
3053  012266  011304                        MOV     (R3),R4
3054  012270  022704  177767                CMP     #177767,R4              ;WAS BIT 12 SET
3055  012274  001403                        BEQ     2$
3056  012276  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
3057                                                                        ;LINE PARAMETER REGISTER, 177767
3058  012302  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3059  012304  104400          2$:   SCOPE
3060
3061                                ;LINE PARAMETER REGISTER DATA TEST
3062                                ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
3063                                ;CLEAR BIT 13
3064                                ;VERIFY THAT BIT 13 WAS CLEARED
3065                                ;RESTORE BIT 13
3066                                ;VERIFY THAT BIT 13 WAS SET
3067
3068  012306  012767  000340  165462  T120:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3069  012314  012767  004000  005126        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3070  012322  012767  012410  005114        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3071  012330  012777  004000  005044        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3072  012336  016703  005044                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
3073  012342  012705  173767                MOV     #173767,R5              ;(R5)=EXPECTED DATA
3074                                                                        ;IN LINE PARAMETER REGISTER, 173767
3075  012346  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
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3076
3077  012352  042713  004000                BIC     #4000,(R3)              ;IN LINE PARAMETER REGISTER
3078  012356  011304                        MOV     (R3),R4                 ;CLEAR BIT 13
3079  012360  020504                        CMP     R5,R4                   ;GET CONTENTS OF LINE PARAMETER
3080  012362  001401                        BEQ     1$                      ;WAS BIT 13 CLEARED
3081  012364  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3082  012366  052713  004000          1$:   BIS     #4000,(R3)              ;SET BIT 13
3083  012372  011304                        MOV     (R3),R4
3084  012374  022704  177767                CMP     #177767,R4              ;WAS BIT 13 SET
3085  012400  001403                        BEQ     2$
3086  012402  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
3087                                                                        ;LINE PARAMETER REGISTER, 177767
3088  012406  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3089  012410  104400          2$:   SCOPE
3090
3091                                ;LINE PARAMETER REGISTER DATA TEST
3092                                ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
3093                                ;CLEAR BIT 14
3094                                ;VERIFY THAT BIT 14 WAS CLEARED
3095                                ;RESTORE BIT 14
3096                                ;VERIFY THAT BIT 14 WAS SET
3097
3098  012412  012767  000340  165356  T121:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3099  012420  012767  004000  005022        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3100  012426  012767  012514  005010        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3101  012434  012777  004000  004740        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3102  012442  016703  004740                MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
3103  012446  012705  167767                MOV     #167767,R5              ;(R5)=EXPECTED DATA
3104                                                                        ;IN LINE PARAMETER REGISTER, 167767
3105  012452  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
3106                                                                        ;IN LINE PARAMETER REGISTER
3107  012456  042713  010000                BIC     #10000,(R3)             ;CLEAR BIT 14
3108  012462  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
3109  012464  020504                        CMP     R5,R4                   ;WAS BIT 14 CLEARED
3110  012466  001401                        BEQ     1$
3111  012470  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3112  012472  052713  010000          1$:   BIS     #10000,(R3)             ;SET BIT 14
3113  012476  011304                        MOV     (R3),R4
3114  012500  022704  177767                CMP     #177767,R4              ;WAS BIT 14 SET
3115  012504  001403                        BEQ     2$
3116  012506  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
3117                                                                        ;LINE PARAMETER REGISTER, 177767
3118  012512  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3119  012514  104400          2$:   SCOPE
3120
3121                                ;LINE PARAMETER REGISTER DATA TEST
3122                                ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
3123                                ;CLEAR BIT 15
3124                                ;VERIFY THAT BIT 15 WAS CLEARED
3125                                ;RESTORE BIT 15
3126                                ;VERIFY THAT BIT 15 WAS SET
3127
3128  012516  012767  000340  165252  T122:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3129  012524  012767  004000  004716        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3130  012532  012767  012620  004704        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3131  012540  012777  004000  004634        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
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3132  012546  016703  004634                MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
3133  012552  012705  157767                MOV     #157767,R5              ;(R5)=EXPECTED DATA
3134                                                                          ;IN LINE PARAMETER REGISTER, 157767
3135  012556  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
3136                                                                          ;IN LINE PARAMETER REGISTER
3137  012562  042713  020000                BIC     #20000,(R3)             ;CLEAR BIT 15
3138  012566  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
3139  012570  020504                        CMP     R5,R4                   ;WAS BIT 15 CLEARED
3140  012572  001401                        BEQ     1$
3141  012574  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3142  012576  052713  020000          1$:   BIS     #20000,(R3)             ;SET BIT 15
3143  012602  011304                        MOV     (R3),R4
3144  012604  022704  177767                CMP     #177767,R4              ;WAS BIT 15 SET
3145  012610  001403                        BEQ     2$
3146  012612  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
3147                                                                          ;LINE PARAMETER REGISTER, 177767
3148  012616  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3149  012620  104400                2$:     SCOPE
3150
3151                                        ;LINE PARAMETER REGISTER DATA TEST
3152                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
3153                                        ;CLEAR BIT 16
3154                                        ;VERIFY THAT BIT 16 WAS CLEARED
3155                                        ;RESTORE BIT 16
3156                                        ;VERIFY THAT BIT 16 WAS SET
3157
3158  012622  012767  000340  165146  T123:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3159  012630  012767  004000  004612        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3160  012636  012767  012724  004600        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3161  012644  012777  004000  004530        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3162  012652  016703  004530                MOV     DHLPR,R3                ;SET UP POINTER TO LINE PARAMETER
3163  012656  012705  137767                MOV     #137767,R5              ;(R5)=EXPECTED DATA
3164                                                                          ;IN LINE PARAMETER REGISTER, 137767
3165  012662  012713  177767                MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
3166                                                                          ;IN LINE PARAMETER REGISTER
3167  012666  042713  040000                BIC     #40000,(R3)             ;CLEAR BIT 16
3168  012672  011304                        MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
3169  012674  020504                        CMP     R5,R4                   ;WAS BIT 16 CLEARED
3170  012676  001401                        BEQ     1$
3171  012700  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3172  012702  052713  040000          1$:   BIS     #40000,(R3)             ;SET BIT 16
3173  012706  011304                        MOV     (R3),R4
3174  012710  022704  177767                CMP     #177767,R4              ;WAS BIT 16 SET
3175  012714  001403                        BEQ     2$
3176  012716  012705  177767                MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
3177                                                                          ;LINE PARAMETER REGISTER, 177767
3178  012722  104002                        HLT     2                       ;LINE PARAMETER REGISTER ERROR
3179  012724  104400                2$:     SCOPE
3180
3181                                        ;LINE PARAMETER REGISTER DATA TEST
3182                                        ;SET ALL READ/WRITE BITS IN LINE PARAMETER REGISTER TO 1S
3183                                        ;CLEAR BIT 17
3184                                        ;VERIFY THAT BIT 17 WAS CLEARED
3185                                        ;RESTORE BIT 17
3186                                        ;VERIFY THAT BIT 17 WAS SET
3187
```

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3188  012726  012767  000340  165042  T124:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3189  012734  012767  004000  004506         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3190  012742  012767  013030  004474         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3191  012750  012777  004000  004424         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3192  012756  016703  004424                 MOV     DHLPR,R3                        ;SET UP POINTER TO LINE PARAMETER
3193  012762  012705  077767                 MOV     #77767,R5               ;(R5)=EXPECTED DATA
3194                                                                           ;IN LINE PARAMETER REGISTER, 77767
3195  012766  012713  177767                 MOV     #177767,(R3)            ;SET ALL READ/WRITE BITS
3196                                                                           ;IN LINE PARAMETER REGISTER
3197  012772  042713  100000                 BIC     #100000,(R3)            ;CLEAR BIT 17
3198  012776  011304                         MOV     (R3),R4                 ;GET CONTENTS OF LINE PARAMETER
3199  013000  020504                         CMP     R5,R4                   ;WAS BIT 17 CLEARED
3200  013002  001401                         BEQ     1$
3201  013004  104002                         HLT     2                       ;LINE PARAMETER REGISTER ERROR
3202  013006  052713  100000         1$:    BIS     #100000,(R3)            ;SET BIT 17
3203  013012  011304                         MOV     (R3),R4
3204  013014  022704  177767                 CMP     #177767,R4              ;WAS BIT 17 SET
3205  013020  001403                         BEQ     2$
3206  013022  012705  177767                 MOV     #177767,R5              ;(R5)=EXPECTED DATA IN
3207                                                                           ;LINE PARAMETER REGISTER, 177767
3208  013026  104002                         HLT     2                       ;LINE PARAMETER REGISTER ERROR
3209  013030  104400         2$:    SCOPE
3210
3211                                 ;BREAK CONTROL REGISTER DATA TEST
3212                                 ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3213                                 ;CLEAR BIT 0
3214                                 ;VERIFY THAT BIT 0 WAS CLEARED
3215                                 ;RESTORE BIT 0
3216                                 ;VERIFY THAT BIT 0 WAS SET
3217
3218  013032  012767  000340  164736  T125:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3219  013040  012767  004000  004402         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3220  013046  012767  013134  004370         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3221  013054  012777  004000  004320         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3222  013062  016703  004330                 MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3223  013066  012705  177776                 MOV     #177776,R5              ;(R5)=EXPECTED DATA
3224                                                                           ;IN BREAK CONTROL REGISTER, 177776
3225  013072  012713  177777                 MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3226                                                                           ;IN BREAK CONTROL REGISTER
3227  013076  042713  000001                 BIC     #1,(R3)         ;CLEAR BIT 0
3228  013102  011304                         MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3229  013104  020504                         CMP     R5,R4                   ;WAS BIT 0 CLEARED
3230  013106  001401                         BEQ     1$
3231  013110  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
3232  013112  052713  000001         1$:    BIS     #1,(R3)         ;SET BIT 0
3233  013116  011304                         MOV     (R3),R4
3234  013120  022704  177777                 CMP     #177777,R4              ;WAS BIT 0 SET
3235  013124  001403                         BEQ     2$
3236  013126  012705  177777                 MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3237                                                                           ;BREAK CONTROL REGISTER, 177777
3238  013132  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
3239  013134  104400         2$:    SCOPE
3240
3241                                 ;BREAK CONTROL REGISTER DATA TEST
3242                                 ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3243                                 ;CLEAR BIT 1
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                                        ;VERIFY THAT BIT 1 WAS CLEARED
                                        ;RESTORE BIT 1
                                        ;VERIFY THAT BIT 1 WAS SET

013136  012767  000340  164632  T126: MOV   #340,PS              ;DISABLE ALL INTERRUPTS
013144  012767  004000  004276        MOV   #4000,ICOUNT         ;SET UP FOR 4000 ITERATIONS
013152  012767  013240  004264        MOV   #2$,ESCAPE           ;SET UP TO ESCAPE TO NEXT TEST
013160  012777  004000  004214        MOV   #BIT11,@DHSCR        ;MASTER CLEAR INTERFACE
013166  016703  004224               MOV   DHBCR,R3                    ;SET UP POINTER TO BREAK CONTROL
013172  012705  177775               MOV   #177775,R5           ;(R5)=EXPECTED DATA
                                                                 ;IN BREAK CONTROL REGISTER, 177775
013176  012713  177777               MOV   #177777,(R3)         ;SET ALL READ/WRITE BITS
                                                                 ;IN BREAK CONTROL REGISTER
013202  042713  000002               BIC   #2,(R3)        ;CLEAR BIT 1
013206  011304                       MOV   (R3),R4                     CONTENTS OF BREAK CONTROL
013210  020504                       CMP   R5,R4                       BIT 1 CLEARED
013212  001401                       BEQ   1$
013214  104003                       HLT   3                           ; CONTROL REGISTER ERROR
013216  052713  000002         1$:   BIS   #2,(R3)        ;SET
013222  011304                       MOV   (R3),R4
013224  022704  177777               CMP   #177777,R4           ;WAS BIT 1 SET
013230  001403                       BEQ   2$
013232  012705  177777               MOV   #177777,R5           ;(R5)=EXPECTED DATA IN
                                                                 ;BREAK CONTROL REGISTER, 177777
013236  104003                       HLT   3                    ;BREAK CONTROL REGISTER ERROR
013240  104400         2$:   SCOPE

                                        ;BREAK CONTROL REGISTER DATA TEST
                                        ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
                                        ;CLEAR BIT 2
                                        ;VERIFY THAT BIT 2 WAS CLEARED
                                        ;RESTORE BIT 2
                                        ;VERIFY THAT BIT 2 WAS SET

013242  012767  000340  164526  T127: MOV   #340,PS              ;DISABLE ALL INTERRUPTS
013250  012767  004000  004172        MOV   #4000,ICOUNT         ;SET UP FOR 4000 ITERATIONS
013256  012767  013344  004160        MOV   #2$,ESCAPE           ;SET UP TO ESCAPE TO NEXT TEST
013264  012777  004000  004110        MOV   #BIT11,@DHSCR        ;MASTER CLEAR INTERFACE
013272  016703  004120               MOV   DHBCR,R3                    ;SET UP POINTER TO BREAK CONTROL
013276  012705  177773               MOV   #177773,R5           ;(R5)=EXPECTED DATA
                                                                 ;IN BREAK CONTROL REGISTER, 177773
013302  012713  177777               MOV   #177777,(R3)         ;SET ALL READ/WRITE BITS
                                                                 ;IN BREAK CONTROL REGISTER
013306  042713  000004               BIC   #4,(R3)        ;CLEAR BIT 2
013312  011304                       MOV   (R3),R4              ;GET CONTENTS OF BREAK CONTROL
013314  020504                       CMP   R5,R4                ;WAS BIT 2 CLEARED
013316  001401                       BEQ   1$
013320  104003                       HLT   3                    ;BREAK CONTROL REGISTER ERROR
013322  052713  000004         1$:   BIS   #4,(R3)        ;SET BIT 2
013326  011304                       MOV   (R3),R4
013330  022704  177777               CMP   #177777,R4           ;WAS BIT 2 SET
013334  001403                       BEQ   2$
013336  012705  177777               MOV   #177777,R5           ;(R5)=EXPECTED DATA IN
                                                                 ;BREAK CONTROL REGISTER, 177777
013342  104003                       HLT   3                    ;BREAK CONTROL REGISTER ERROR
013344  104400         2$:   SCOPE
```

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3300
3301                                            ;BREAK CONTROL REGISTER DATA TEST
3302                                            ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3303                                            ;CLEAR BIT 3
3304                                            ;VERIFY THAT BIT 3 WAS CLEARED
3305                                            ;RESTORE BIT 3
3306                                            ;VERIFY THAT BIT 3 WAS SET
3307
3308  013346  012767  000340  164422  T130:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
3309  013354  012767  004000  004066          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
3310  013362  012767  013450  004054          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
3311  013370  012777  004000  004004          MOV     #BIT11,@DHSCR   ;MASTER CLEAR INTERFACE
3312  013376  016703  004014                  MOV     DHBCR,R3                :SET UP POINTER TO BREAK CONTROL
3313  013402  012705  177767                  MOV     #177767,R5      ;(R5)=EXPECTED DATA
3314                                                                  ;IN BREAK CONTROL REGISTER, 177767
3315  013406  012713  177777                  MOV     #177777,(R3)    ;SET ALL READ/WRITE BITS
3316                                                                  ;IN BREAK CONTROL REGISTER
3317  013412  012713  000010                  BIC     #10,(R3)        ;CLEAR BIT 3
3318  013416  011304                          MOV     (R3),R4         ;GET CONTENTS OF BREAK CONTROL
3319  013420  020504                          CMP     R5,R4           ;WAS BIT 3 CLEARED
3320  013422  001401                          BEQ     1$
3321  013424  104003                          HLT     3               ;BREAK CONTROL REGISTER ERROR
3322  013426  052713  000010          1$:     BIS     #10,(R3)        ;SET BIT 3
3323  013432  011304                          MOV     (R3),R4
3324  013434  022704  177777                  CMP     #177777,R4      ;WAS BIT 3 SET
3325  013440  001403                          BEQ     2$
3326  013442  012705  177777                  MOV     #177777,R5      ;(R5)=EXPECTED DATA IN
3327                                                                  ;BREAK CONTROL REGISTER, 177777
3328  013446  104003                          HLT     3               ;BREAK CONTROL REGISTER ERROR
3329  013450  104400          2$:     SCOPE
3330
3331                                            ;BREAK CONTROL REGISTER DATA TEST
3332                                            ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3333                                            ;CLEAR BIT 4
3334                                            ;VERIFY THAT BIT 4 WAS CLEARED
3335                                            ;RESTORE BIT 4
3336                                            ;VERIFY THAT BIT 4 WAS SET
3337
3338  013452  012767  000340  164316  T131:   MOV     #340,PS         ;DISABLE ALL INTERRUPTS
3339  013460  012767  004000  003762          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
3340  013466  012767  013554  003750          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
3341  013474  012777  004000  003700          MOV     #BIT11,@DHSCR   ;MASTER CLEAR INTERFACE
3342  013502  016703  003710                  MOV     DHBCR,R3                :SET UP POINTER TO BREAK CONTROL
3343  013506  012705  177757                  MOV     #177757,R5      ;(R5)=EXPECTED DATA
3344                                                                  ;IN BREAK CONTROL REGISTER, 177757
3345  013512  012713  177777                  MOV     #177777,(R3)    ;SET ALL READ/WRITE BITS
3346                                                                  ;IN BREAK CONTROL REGISTER
3347  013516  042713  000020                  BIC     #20,(R3)        ;CLEAR BIT 4
3348  013522  011304                          MOV     (R3),R4         ;GET CONTENTS OF BREAK CONTROL
3349  013524  020504                          CMP     R5,R4           ;WAS BIT 4 CLEARED
3350  013526  001401                          BEQ     1$
3351  013530  104003                          HLT     3               ;BREAK CONTROL REGISTER ERROR
3352  013532  052713  000020          1$:     BIS     #20,(R3)        ;SET BIT 4
3353  013536  011304                          MOV     (R3),R4
3354  013540  022704  177777                  CMP     #177777,R4      ;WAS BIT 4 SET
3355  013544  001403                          BEQ     2$
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3356  013546  012705  177777                    MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3357                                                                              ;BREAK CONTROL REGISTER, 177777
3358  013552  104003                            HLT     3                       ;BREAK CONTROL REGISTER ERROR
3359  013554  104400                    2$:     SCOPE
3360
3361                                            ;BREAK CONTROL REGISTER DATA TEST
3362                                            ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3363                                            ;CLEAR BIT 5
3364                                            ;VERIFY THAT BIT 5 WAS CLEARED
3365                                            ;RESTORE BIT 5
3366                                            ;VERIFY THAT BIT 5 WAS SET
3367
3368  013556  012767  000340  164212    T132:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3369  013564  012767  004000  003656            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3370  013572  012767  013660  003644            MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3371  013600  012777  004000  003574            MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3372  013606  016703  003604                    MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3373  013612  012705  177737                    MOV     #177737,R5              ;(R5)=EXPECTED DATA
3374                                                                              ;IN BREAK CONTROL REGISTER, 177737
3375  013616  012713  177777                    MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3376                                                                              ;IN BREAK CONTROL REGISTER
3377  013622  042713  000040                    BIC     #40,(R3)                ;CLEAR BIT 5
3378  013626  011304                            MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3379  013630  020504                            CMP     R5,R4                   ;WAS BIT 5 CLEARED
3380  013632  001401                            BEQ     1$
3381  013634  104003                            HLT     3                       ;BREAK CONTROL REGISTER ERROR
3382  013636  052713  000040            1$:     BIS     #40,(R3)                ;SET BIT 5
3383  013642  011304                            MOV     (R3),R4
3384  013644  022704  177777                    CMP     #177777,R4              ;WAS BIT 5 SET
3385  013650  001403                            BEQ     2$
3386  013652  012705  177777                    MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3387                                                                              ;BREAK CONTROL REGISTER, 177777
3388  013656  104003                            HLT     3                       ;BREAK CONTROL REGISTER ERROR
3389  013660  104400                    2$:     SCOPE
3390
3391                                            ;BREAK CONTROL REGISTER DATA TEST
3392                                            ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3393                                            ;CLEAR BIT 6
3394                                            ;VERIFY THAT BIT 6 WAS CLEARED
3395                                            ;RESTORE BIT 6
3396                                            ;VERIFY THAT BIT 6 WAS SET
3397
3398  013662  012767  000340  164106    T133:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3399  013670  012767  004000  003552            MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3400  013676  012767  013764  003540            MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3401  013704  012777  004000  003470            MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3402  013712  016703  003500                    MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3403  013716  012705  177677                    MOV     #177677,R5              ;(R5)=EXPECTED DATA
3404                                                                              ;IN BREAK CONTROL REGISTER, 177677
3405  013722  012713  177777                    MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3406                                                                              ;IN BREAK CONTROL REGISTER
3407  013726  042713  000100                    BIC     #100,(R3)               ;CLEAR BIT 6
3408  013732  011304                            MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3409  013734  020504                            CMP     R5,R4                   ;WAS BIT 6 CLEARED
3410  013736  001401                            BEQ     1$
3411  013740  104003                            HLT     3                       ;BREAK CONTROL REGISTER ERROR
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3412  013742  052713  000100          1$:   BIS     #100,(R3)              ;SET BIT 6
3413  013746  011304                        MOV     (R3),R4
3414  013750  022704  177777                CMP     #177777,R4             ;WAS BIT 6 SET
3415  013754  001403                        BEQ     2$
3416  013756  012705  177777                MOV     #177777,R5             ;(R5)=EXPECTED DATA IN
3417                                                                         ;BREAK CONTROL REGISTER, 177777
3418  013762  104003                        HLT     3                      ;BREAK CONTROL REGISTER ERROR
3419  013764  104400                2$:     SCOPE
3420
3421                                        ;BREAK CONTROL REGISTER DATA TEST
3422                                        ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3423                                        ;CLEAR BIT 7
3424                                        ;VERIFY THAT BIT 7 WAS CLEARED
3425                                        ;RESTORE BIT 7
3426                                        ;VERIFY THAT BIT 7 WAS SET
3427
3428  013766  012767  000340  164002  T134: MOV     #340,PS                ;DISABLE ALL INTERRUPTS
3429  013774  012767  004000  003446        MOV     #4000,ICOUNT           ;SET UP FOR 4000 ITERATIONS
3430  014002  012767  014070  003434        MOV     #2$,ESCAPE             ;SET UP TO ESCAPE TO NEXT TEST
3431  014010  012777  004000  003364        MOV     #BIT11,@DHSCR          ;MASTER CLEAR INTERFACE
3432  014016  016703  003374                MOV     DHBCR,R3                       ;SET UP POINTER TO BREAK CONTROL
3433  014022  012705  177577                MOV     #177577,R5             ;(R5)=EXPECTED DATA
3434                                                                         ;IN BREAK CONTROL REGISTER, 177577
3435  014026  012713  177777                MOV     #177777,(R3)           ;SET ALL READ/WRITE BITS
3436                                                                         ;IN BREAK CONTROL REGISTER
3437  014032  042713  000200                BIC     #200,(R3)              ;CLEAR BIT 7
3438  014036  011304                        MOV     (R3),R4                ;GET CONTENTS OF BREAK CONTROL
3439  014040  020504                        CMP     R5,R4                  ;WAS BIT 7 CLEARED
3440  014042  001401                        BEQ     1$
3441  014044  104003                        HLT     3                      ;BREAK CONTROL REGISTER ERROR
3442  014046  052713  000200          1$:   BIS     #200,(R3)              ;SET BIT 7
3443  014052  011304                        MOV     (R3),R4
3444  014054  022704  177777                CMP     #177777,R4             ;WAS BIT 7 SET
3445  014060  001403                        BEQ     2$
3446  014062  012705  177777                MOV     #177777,R5             ;(R5)=EXPECTED DATA IN
3447                                                                         ;BREAK CONTROL REGISTER, 177777
3448  014066  104003                        HLT     3                      ;BREAK CONTROL REGISTER ERROR
3449  014070  104400                2$:     SCOPE
3450
3451                                        ;BREAK CONTROL REGISTER DATA TEST
3452                                        ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3453                                        ;CLEAR BIT 10
3454                                        ;VERIFY THAT BIT 10 WAS CLEARED
3455                                        ;RESTORE BIT 10
3456                                        ;VERIFY THAT BIT 10 WAS SET
3457
3458  014072  012767  000340  163676  T135: MOV     #340,PS                ;DISABLE ALL INTERRUPTS
3459  014100  012767  004000  003342        MOV     #4000,ICOUNT           ;SET UP FOR 4000 ITERATIONS
3460  014106  012767  014174  003330        MOV     #2$,ESCAPE             ;SET UP TO ESCAPE TO NEXT TEST
3461  014114  012777  004000  003260        MOV     #BIT11,@DHSCR          ;MASTER CLEAR INTERFACE
3462  014122  016703  003270                MOV     DHBCR,R3                       ;SET UP POINTER TO BREAK CONTROL
3463  014126  012705  177377                MOV     #177377,R5             ;(R5)=EXPECTED DATA
3464                                                                         ;IN BREAK CONTROL REGISTER, 177377
3465  014132  012713  177777                MOV     #177777,(R3)           ;SET ALL READ/WRITE BITS
3466                                                                         ;IN BREAK CONTROL REGISTER
3467  014136  042713  000400                BIC     #400,(R3)              ;CLEAR BIT 10
```

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3468  014142  011304                          MOV     (R3),R4         ;GET CONTENTS OF BREAK CONTROL
3469  014144  020504                          CMP     R5,R4           ;WAS BIT 10 CLEARED
3470  014146  001401                          BEQ     1$
3471  014150  104003                          HLT     3               ;BREAK CONTROL REGISTER ERROR
3472  014152  052713  000400          1$:     BIS     #400,(R3)       ;SET BIT 10
3473  014156  011304                          MOV     (R3),R4
3474  014160  022704  177777                  CMP     #177777,R4      ;WAS BIT 10 SET
3475  014164  001403                          BEQ     2$
3476  014166  012705  177777                  MOV     #177777,R5      ;(R5)=EXPECTED DATA IN
3477                                                                  ;BREAK CONTROL REGISTER, 177777
3478  014172  104003                          HLT     3               ;BREAK CONTROL REGISTER ERROR
3479  014174  104400          2$:     SCOPE
3480
3481                                  ;BREAK CONTROL REGISTER DATA TEST
3482                                  ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3483                                  ;CLEAR BIT 11
3484                                  ;VERIFY THAT BIT 11 WAS CLEARED
3485                                  ;RESTORE BIT 11
3486                                  ;VERIFY THAT BIT 11 WAS SET
3487
3488  014176  012767  000340  163572  T136:  MOV     #340,PS         ;DISABLE ALL INTERRUPTS
3489  014204  012767  004000  003236          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
3490  014212  012767  014300  003224          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
3491  014220  012777  004000  003154          MOV     #BIT11,@DHSCR   ;MASTER CLEAR INTERFACE
3492  014226  016703  003164                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
3493  014232  012705  176777                  MOV     #176777,R5      ;(R5)=EXPECTED DATA
3494                                                                  ;IN BREAK CONTROL REGISTER, 176777
3495  014236  012713  177777                  MOV     #177777,(R3)    ;SET ALL READ/WRITE BITS
3496                                                                  ;IN BREAK CONTROL REGISTER
3497  014242  042713  001000                  BIC     #1000,(R3)      ;CLEAR BIT 11
3498  014246  011304                          MOV     (R3),R4         ;GET CONTENTS OF BREAK CONTROL
3499  014250  020504                          CMP     R5,R4           ;WAS BIT 11 CLEARED
3500  014252  001401                          BEQ     1$
3501  014254  104003                          HLT     3               ;BREAK CONTROL REGISTER ERROR
3502  014256  052713  001000          1$:     BIS     #1000,(R3)      ;SET BIT 11
3503  014262  011304                          MOV     (R3),R4
3504  014264  022704  177777                  CMP     #177777,R4      ;WAS BIT 11 SET
3505  014270  001403                          BEQ     2$
3506  014272  012705  177777                  MOV     #177777,R5      ;(R5)=EXPECTED DATA IN
3507                                                                  ;BREAK CONTROL REGISTER, 177777
3508  014276  104003                          HLT     3               ;BREAK CONTROL REGISTER ERROR
3509  014300  104400          2$:     SCOPE
3510
3511                                  ;BREAK CONTROL REGISTER DATA TEST
3512                                  ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3513                                  ;CLEAR BIT 12
3514                                  ;VERIFY THAT BIT 12 WAS CLEARED
3515                                  ;RESTORE BIT 12
3516                                  ;VERIFY THAT BIT 12 WAS SET
3517
3518  014302  012767  000340  163466  T137:  MOV     #340,PS         ;DISABLE ALL INTERRUPTS
3519  014310  012767  004000  003132          MOV     #4000,ICOUNT    ;SET UP FOR 4000 ITERATIONS
3520  014316  012767  014404  003120          MOV     #2$,ESCAPE      ;SET UP TO ESCAPE TO NEXT TEST
3521  014324  012777  004000  003050          MOV     #BIT11,@DHSCR   ;MASTER CLEAR INTERFACE
3522  014332  016703  003060                  MOV     DHBCR,R3                ;SET UP POINTER TO BREAK CONTROL
3523  014336  012705  175777                  MOV     #175777,R5      ;(R5)=EXPECTED DATA
```

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3524
3525  014342  012713  177777                MOV     #177777,(R3)            ;IN BREAK CONTROL REGISTER, 175777
3526                                                                          ;SET ALL READ/WRITE BITS
3527  014346  042713  002000                BIC     #2000,(R3)              ;IN BREAK CONTROL REGISTER
3528  014352  011304                        MOV     (R3),R4                 ;CLEAR BIT 12
3529  014354  020504                        CMP     R5,R4                   ;GET CONTENTS OF BREAK CONTROL
3530  014356  001401                        BEQ     1$                      ;WAS BIT 12 CLEARED
3531  014360  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
3532  014362  052713  002000          1$:   BIS     #2000,(R3)              ;SET BIT 12
3533  014366  011304                        MOV     (R3),R4
3534  014370  022704  177777                CMP     #177777,R4              ;WAS BIT 12 SET
3535  014374  001403                        BEQ     2$
3536  014376  012705  177777                MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3537                                                                          ;BREAK CONTROL REGISTER, 177777
3538  014402  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
3539  014404  104400                  2$:   SCOPE
3540
3541                                        ;BREAK CONTROL REGISTER DATA TEST
3542                                        ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3543                                        ;CLEAR BIT 13
3544                                        ;VERIFY THAT BIT 13 WAS CLEARED
3545                                        ;RESTORE BIT 13
3546                                        ;VERIFY THAT BIT 13 WAS SET
3547
3548  014406  012767  000340  163362  T140:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3549  014414  012767  004000  003026        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3550  014422  012767  014510  003014        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3551  014430  012777  004000  002744        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3552  014436  016703  002754                MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3553  014442  012705  173777                MOV     #173777,R5              ;(R5)=EXPECTED DATA
3554                                                                          ;IN BREAK CONTROL REGISTER, 173777
3555  014446  012713  177777                MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3556                                                                          ;IN BREAK CONTROL REGISTER
3557  014452  042713  004000                BIC     #4000,(R3)              ;CLEAR BIT 13
3558  014456  011304                        MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3559  014460  020504                        CMP     R5,R4                   ;WAS BIT 13 CLEARED
3560  014462  001401                        BEQ     1$
3561  014464  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
3562  014466  052713  004000          1$:   BIS     #4000,(R3)              ;SET BIT 13
3563  014472  011304                        MOV     (R3),R4
3564  014474  022704  177777                CMP     #177777,R4              ;WAS BIT 13 SET
3565  014500  001403                        BEQ     2$
3566  014502  012705  177777                MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3567                                                                          ;BREAK CONTROL REGISTER, 177777
3568  014506  104003                        HLT     3                       ;BREAK CONTROL REGISTER ERROR
3569  014510  104400                  2$:   SCOPE
3570
3571                                        ;BREAK CONTROL REGISTER DATA TEST
3572                                        ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3573                                        ;CLEAR BIT 14
3574                                        ;VERIFY THAT BIT 14 WAS CLEARED
3575                                        ;RESTORE BIT 14
3576                                        ;VERIFY THAT BIT 14 WAS SET
3577
3578  014512  012767  000340  163256  T141:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3579  014520  012767  004000  002722        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
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3580  014526  012767  014614  002710          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3581  014534  012777  004000  002640          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3582  014542  016703  002650                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3583  014546  012705  167777                  MOV     #167777,R5              ;(R5)=EXPECTED DATA
3584                                                                          ;IN BREAK CONTROL REGISTER, 167777
3585  014552  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3586                                                                          ;IN BREAK CONTROL REGISTER
3587  014556  042713  010000                  BIC     #10000,(R3)             ;CLEAR BIT 14
3588  014562  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3589  014564  020504                          CMP     R5,R4                   ;WAS BIT 14 CLEARED
3590  014566  001401                          BEQ     1$
3591  014570  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3592  014572  052713  010000          1$:     BIS     #10000,(R3)             ;SET BIT 14
3593  014576  011304                          MOV     (R3),R4
3594  014600  022704  177777                  CMP     #177777,R4              ;WAS BIT 14 SET
3595  014604  001403                          BEQ     2$
3596  014606  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3597                                                                          ;BREAK CONTROL REGISTER, 177777
3598  014612  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3599  014614  104400          2$:     SCOPE
3600
3601                                  ;BREAK CONTROL REGISTER DATA TEST
3602                                  ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3603                                  ;CLEAR BIT 15
3604                                  ;VERIFY THAT BIT 15 WAS CLEARED
3605                                  ;RESTORE BIT 15
3606                                  ;VERIFY THAT BIT 15 WAS SET
3607
3608  014616  012767  000340  163152  T142:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3609  014624  012767  004000  002616          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3610  014632  012767  014720  002604          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3611  014640  012777  004000  002534          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3612  014646  016703  002544                  MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
3613  014652  012705  157777                  MOV     #157777,R5              ;(R5)=EXPECTED DATA
3614                                                                          ;IN BREAK CONTROL REGISTER, 157777
3615  014656  012713  177777                  MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
3616                                                                          ;IN BREAK CONTROL REGISTER
3617  014662  042713  020000                  BIC     #20000,(R3)             ;CLEAR BIT 15
3618  014666  011304                          MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
3619  014670  020504                          CMP     R5,R4                   ;WAS BIT 15 CLEARED
3620  014672  001401                          BEQ     1$
3621  014674  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3622  014676  052713  020000          1$:     BIS     #20000,(R3)             ;SET BIT 15
3623  014702  011304                          MOV     (R3),R4
3624  014704  022704  177777                  CMP     #177777,R4              ;WAS BIT 15 SET
3625  014710  001403                          BEQ     2$
3626  014712  012705  177777                  MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
3627                                                                          ;BREAK CONTROL REGISTER, 177777
3628  014716  104003                          HLT     3                       ;BREAK CONTROL REGISTER ERROR
3629  014720  104400          2$:     SCOPE
3630
3631                                  ;BREAK CONTROL REGISTER DATA TEST
3632                                  ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
3633                                  ;CLEAR BIT 16
3634                                  ;VERIFY THAT BIT 16 WAS CLEARED
3635                                  ;RESTORE BIT 16
```

```
                                                ;VERIFY THAT BIT 16 WAS SET
                                                
015722  012767  000340  163046  T143:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
015730  012767  004000  002512         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
015736  012767  015024  002500         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
015744  012777  004000  002430         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
015752  016703  002440                 MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
015756  012705  137777                 MOV     #137777,R5              ;(R5)=EXPECTED DATA
                                                                        ;IN BREAK CONTROL REGISTER, 137777
015762  012713  177777                 MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
                                                                        ;IN BREAK CONTROL REGISTER
015766  042713  040000                 BIC     #40000,(R3)             ;CLEAR BIT 16
015772  011304                         MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
015774  020504                         CMP     R5,R4                   ;WAS BIT 16 CLEARED
015776  001401                         BEQ     1$
015000  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
015002  052713  040000         1$:     BIS     #40000,(R3)             ;SET BIT 16
015006  011304                         MOV     (R3),R4
015010  022704  177777                 CMP     #177777,R4              ;WAS BIT 16 SET
015014  001403                         BEQ     2$
015016  012705  177777                 MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
                                                                        ;BREAK CONTROL REGISTER, 177777
015022  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
015024  104400         2$:     SCOPE
                                                
                                                ;BREAK CONTROL REGISTER DATA TEST
                                                ;SET ALL READ/WRITE BITS IN BREAK CONTROL REGISTER TO 1S
                                                ;CLEAR BIT 17
                                                ;VERIFY THAT BIT 17 WAS CLEARED
                                                ;RESTORE BIT 17
                                                ;VERIFY THAT BIT 17 WAS SET
                                                
015026  012767  000340  162742  T144:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
015034  012767  004000  002406         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
015042  012767  015130  002374         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
015050  012777  004000  002324         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
015056  016703  002334                 MOV     DHBCR,R3                        ;SET UP POINTER TO BREAK CONTROL
015062  012705  077777                 MOV     #77777,R5               ;(R5)=EXPECTED DATA
                                                                        ;IN BREAK CONTROL REGISTER, 77777
015066  012713  177777                 MOV     #177777,(R3)            ;SET ALL READ/WRITE BITS
                                                                        ;IN BREAK CONTROL REGISTER
015072  042713  100000                 BIC     #100000,(R3)            ;CLEAR BIT 17
015076  011304                         MOV     (R3),R4                 ;GET CONTENTS OF BREAK CONTROL
015100  020504                         CMP     R5,R4                   ;WAS BIT 17 CLEARED
015102  001401                         BEQ     1$
015104  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
015106  052713  100000         1$:     BIS     #100000,(R3)            ;SET BIT 17
015112  011304                         MOV     (R3),R4
015114  022704  177777                 CMP     #177777,R4              ;WAS BIT 17 SET
015120  001403                         BEQ     2$
015122  012705  177777                 MOV     #177777,R5              ;(R5)=EXPECTED DATA IN
                                                                        ;BREAK CONTROL REGISTER, 177777
015126  104003                         HLT     3                       ;BREAK CONTROL REGISTER ERROR
015130  104400         2$:     SCOPE
                                                
                                                ;SILO STATUS REGISTER DATA TEST
```

```
                                        ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
                                        ;CLEAR BIT 0
                                        ;VERIFY THAT BIT 0 WAS CLEARED
                                        ;RESTORE BIT 0
                                        ;VERIFY THAT BIT 0 WAS SET

015132  012767  000340  162636  T145:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
015140  012767  004000  002302         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
015146  012767  015244  002270         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
015154  012777  004000  002220         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
015162  016703  002232                 MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
015166  012705  100076                 MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
                                                                        ;IN SILO STATUS REGISTER, CLRBIT
015172  012713  100077                 MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
                                                                        ;IN SILO STATUS REGISTER
015176  042713  000001                 BIC     #1,(R3)         ;CLEAR BIT 0
015202  011304                         MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
015204  042704  077700                 BIC     #77700,R4               ;CLEAR UNWANTED BITS
015210  020504                         CMP     R5,R4                   ;WAS BIT 0 CLEARED
015212  001401                         BEQ     1$
015214  104004                         HLT     4                       ;SILO STATUS REGISTER ERROR
015216  052713  000001          1$:    BIS     #1,(R3)         ;SET BIT 0
015222  011304                         MOV     (R3),R4
015224  042704  077700                 BIC     #77700,R4               ;CLEAR UNWANTED BITS
015230  022704  100077                 CMP     #100077,R4              ;WAS BIT 0 SET
015234  001403                         BEQ     2$
015236  012705  100077                 MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
                                                                        ;SILO STATUS REGISTER, 100077
015242  104004                         HLT     4                       ;SILO STATUS REGISTER ERROR
015244  104400          2$:    SCOPE

                                        ;SILO STATUS REGISTER DATA TEST
                                        ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
                                        ;CLEAR BIT 1
                                        ;VERIFY THAT BIT 1 WAS CLEARED
                                        ;RESTORE BIT 1
                                        ;VERIFY THAT BIT 1 WAS SET

015246  012767  000340  162522  T146:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
015254  012767  004000  002166         MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
015262  012767  015360  002154         MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
015270  012777  004000  002104         MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
015276  016703  002116                 MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
015302  012705  100075                 MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
                                                                        ;IN SILO STATUS REGISTER, CLRBIT
015306  012713  100077                 MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
                                                                        ;IN SILO STATUS REGISTER
015312  042713  000002                 BIC     #2,(R3)         ;CLEAR BIT 1
015316  011304                         MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
015320  042704  077700                 BIC     #77700,R4               ;CLEAR UNWANTED BITS
015324  020504                         CMP     R5,R4                   ;WAS BIT 1 CLEARED
015326  001401                         BEQ     1$
015330  104004                         HLT     4                       ;SILO STATUS REGISTER ERROR
015332  052713  000002          1$:    BIS     #2,(R3)         ;SET BIT 1
015336  011304                         MOV     (R3),R4
015340  042704  077700                 BIC     #77700,R4               ;CLEAR UNWANTED BITS
```

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3748  015344  022704  100077              CMP     #100077,R4              ;WAS BIT 1 SET
3749  015350  001403                      BEQ     2$
3750  015352  012705  100077              MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3751                                                                        ;SILO STATUS REGISTER, 100077
3752  015356  104004                      HLT     4                       ;SILO STATUS REGISTER ERROR
3753  015360  104400              2$:     SCOPE
3754
3755                                      ;SILO STATUS REGISTER DATA TEST
3756                                      ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3757                                      ;CLEAR BIT 2
3758                                      ;VERIFY THAT BIT 2 WAS CLEARED
3759                                      ;RESTORE BIT 2
3760                                      ;VERIFY THAT BIT 2 WAS SET
3761
3762  015362  012767  000340  162406 T147: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3763  015370  012767  004000  002052      MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3764  015376  012767  015474  002040      MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3765  015404  012777  004000  001770      MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3766  015412  016703  002002              MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3767  015416  012705  100073              MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3768                                                                        ;IN SILO STATUS REGISTER, CLRBIT
3769  015422  012713  100077              MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3770                                                                        ;IN SILO STATUS REGISTER
3771  015426  042713  000004              BIC     #4,(R3)         ;CLEAR BIT 2
3772  015432  011304                      MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3773  015434  042704  077700              BIC     #77700,R4               ;CLEAR UNWANTED BITS
3774  015440  020504                      CMP     R5,R4                   ;WAS BIT 2 CLEARED
3775  015442  001401                      BEQ     1$
3776  015444  104004                      HLT     4                       ;SILO STATUS REGISTER ERROR
3777  015446  052713  000004      1$:     BIS     #4,(R3)         ;SET BIT 2
3778  015452  011304                      MOV     (R3),R4
3779  015454  042704  077700              BIC     #77700,R4               ;CLEAR UNWANTED BITS
3780  015460  022704  100077              CMP     #100077,R4              ;WAS BIT 2 SET
3781  015464  001403                      BEQ     2$
3782  015466  012705  100077              MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3783                                                                        ;SILO STATUS REGISTER, 100077
3784  015472  104004                      HLT     4                       ;SILO STATUS REGISTER ERROR
3785  015474  104400              2$:     SCOPE
3786
3787                                      ;SILO STATUS REGISTER DATA TEST
3788                                      ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3789                                      ;CLEAR BIT 3
3790                                      ;VERIFY THAT BIT 3 WAS CLEARED
3791                                      ;RESTORE BIT 3
3792                                      ;VERIFY THAT BIT 3 WAS SET
3793
3794  015476  012767  000340  162272 T150: MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3795  015504  012767  004000  001736      MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3796  015512  012767  015610  001724      MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3797  015520  012777  004000  001654      MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3798  015526  016703  001666              MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3799  015532  012705  100067              MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3800                                                                        ;IN SILO STATUS REGISTER, CLRBIT
3801  015536  012713  100077              MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3802                                                                        ;IN SILO STATUS REGISTER
3803  015542  042713  000010              BIC     #10,(R3)                ;CLEAR BIT 3
```

```
3804  015546  011304                        MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3805  015550  042704  077700                BIC     #77700,R4               ;CLEAR UNWANTED BITS
3806  015554  020504                        CMP     R5,R4                   ;WAS BIT 3 CLEARED
3807  015556  001401                        BEQ     1$
3808  015560  104004                        HLT     4                       ;SILO STATUS REGISTER ERROR
3809  015562  052713  000010        1$:     BIS     #10,(R3)                ;SET BIT 3
3810  015566  011304                        MOV     (R3),R4
3811  015570  042704  077700                BIC     #77700,R4               ;CLEAR UNWANTED BITS
3812  015574  022704  100077                CMP     #100077,R4              ;WAS BIT 3 SET
3813  015600  001403                        BEQ     2$
3814  015602  012705  100077                MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3815                                                                        ;SILO STATUS REGISTER, 100077
3816  015606  104004                        HLT     4                       ;SILO STATUS REGISTER ERROR
3817  015610  104400        2$:     SCOPE
3818
3819                                        ;SILO STATUS REGISTER DATA TEST
3820                                        ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3821                                        ;CLEAR BIT 4
3822                                        ;VERIFY THAT BIT 4 WAS CLEARED
3823                                        ;RESTORE BIT 4
3824                                        ;VERIFY THAT BIT 4 WAS SET
3825
3826  015612  012767  000340  162156  T151:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3827  015620  012767  004000  001622        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3828  015626  012767  015724  001610        MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3829  015634  012777  004000  001540        MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3830  015642  016703  001552                MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3831  015646  012705  100057                MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3832                                                                        ;IN SILO STATUS REGISTER, CLRBIT
3833  015652  012713  100077                MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3834                                                                        ;IN SILO STATUS REGISTER
3835  015656  042713  000020                BIC     #20,(R3)                ;CLEAR BIT 4
3836  015662  011304                        MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3837  015664  042704  077700                BIC     #77700,R4               ;CLEAR UNWANTED BITS
3838  015670  020504                        CMP     R5,R4                   ;WAS BIT 4 CLEARED
3839  015672  001401                        BEQ     1$
3840  015674  104004                        HLT     4                       ;SILO STATUS REGISTER ERROR
3841  015676  052713  000020        1$:     BIS     #20,(R3)                ;SET BIT 4
3842  015702  011304                        MOV     (R3),R4
3843  015704  042704  077700                BIC     #77700,R4               ;CLEAR UNWANTED BITS
3844  015710  022704  100077                CMP     #100077,R4              ;WAS BIT 4 SET
3845  015714  001403                        BEQ     2$
3846  015716  012705  100077                MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3847                                                                        ;SILO STATUS REGISTER, 100077
3848  015722  104004                        HLT     4                       ;SILO STATUS REGISTER ERROR
3849  015724  104400        2$:     SCOPE
3850
3851                                        ;SILO STATUS REGISTER DATA TEST
3852                                        ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3853                                        ;CLEAR BIT 5
3854                                        ;VERIFY THAT BIT 5 WAS CLEARED
3855                                        ;RESTORE BIT 5
3856                                        ;VERIFY THAT BIT 5 WAS SET
3857
3858  015726  012767  000340  162042  T152:  MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3859  015734  012767  004000  001506        MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
```

```
3860  015742  012767  016040  001474          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3861  015750  012777  004000  001424          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3862  015756  016703  001436                  MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3863  015762  012705  100037                  MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3864                                                                          ;IN SILO STATUS REGISTER, CLRBIT
3865  015766  012713  100077                  MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3866                                                                          ;IN SILO STATUS REGISTER
3867  015772  042713  000040                  BIC     #40,(R3)                ;CLEAR BIT 5
3868  015776  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3869  016000  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3870  016004  020504                          CMP     R5,R4                   ;WAS BIT 5 CLEARED
3871  016006  001401                          BEQ     1$
3872  016010  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3873  016012  052713  000040          1$:     BIS     #40,(R3)                ;SET BIT 5
3874  016016  011304                          MOV     (R3),R4
3875  016020  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3876  016024  022704  100077                  CMP     #100077,R4              ;WAS BIT 5 SET
3877  016030  001403                          BEQ     2$
3878  016032  012705  100077                  MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3879                                                                          ;SILO STATUS REGISTER, 100077
3880  016036  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3881  016040  104400          2$:     SCOPE
3882
3883                                  ;SILO STATUS REGISTER DATA TEST
3884                                  ;SET ALL READ/WRITE BITS IN SILO STATUS REGISTER TO 1S
3885                                  ;CLEAR BIT 17
3886                                  ;VERIFY THAT BIT 17 WAS CLEARED
3887                                  ;RESTORE BIT 17
3888                                  ;VERIFY THAT BIT 17 WAS SET
3889
3890  016042  012767  000340  161726  T153:   MOV     #340,PS                 ;DISABLE ALL INTERRUPTS
3891  016050  012767  004000  001372          MOV     #4000,ICOUNT            ;SET UP FOR 4000 ITERATIONS
3892  016056  012767  016154  001360          MOV     #2$,ESCAPE              ;SET UP TO ESCAPE TO NEXT TEST
3893  016064  012777  004000  001310          MOV     #BIT11,@DHSCR           ;MASTER CLEAR INTERFACE
3894  016072  016703  001322                  MOV     DHSSR,R3                        ;SET UP POINTER TO SILO STATUS
3895  016076  012705  000077                  MOV     #CLRBIT,R5              ;(R5)=EXPECTED DATA
3896                                                                          ;IN SILO STATUS REGISTER, CLRBIT
3897  016102  012713  100077                  MOV     #100077,(R3)            ;SET ALL READ/WRITE BITS
3898                                                                          ;IN SILO STATUS REGISTER
3899  016106  042713  100000                  BIC     #100000,(R3)            ;CLEAR BIT 17
3900  016112  011304                          MOV     (R3),R4                 ;GET CONTENTS OF SILO STATUS
3901  016114  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3902  016120  020504                          CMP     R5,R4                   ;WAS BIT 17 CLEARED
3903  016122  001401                          BEQ     1$
3904  016124  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3905  016126  052713  100000          1$:     BIS     #100000,(R3)            ;SET BIT 17
3906  016132  011304                          MOV     (R3),R4
3907  016134  042704  077700                  BIC     #77700,R4               ;CLEAR UNWANTED BITS
3908  016140  022704  100077                  CMP     #100077,R4              ;WAS BIT 17 SET
3909  016144  001403                          BEQ     2$
3910  016146  012705  100077                  MOV     #100077,R5              ;(R5)=EXPECTED DATA IN
3911                                                                          ;SILO STATUS REGISTER, 100077
3912  016152  104004                          HLT     4                       ;SILO STATUS REGISTER ERROR
3913  016154  104400          2$:     SCOPE
```

```
                                        ;END OF PASS
                                        ;TYPE NAME OF TEST
                                        ;UPDATE PASS COUNT
                                        ;CHECK FOR EXIT TO ACT-11
                                        ;RESTART TEST

016156  104401                  EOP:  TYPE                            ;TYPE NAME OF TEST
016160  020055                        MEPASS
016162  005067  001312                CLR     LAST                    ;CLEAR LAST ERROR PC
016166  005067  001242                CLR     ERRFLG                  ;CLEAR ERROR FLAG
016172  005267  001240                INC     PASCNT                  ;UPDATE PASS COUNT
016176  016767  001234  161364        MOV     PASCNT,LIGHTS           ;DISPLAY PASS COUNT
016204  013701  000042                MOV     @#42,R1                 ;CHECK FOR ACT-11 OR DDP
016210  001405                        BEQ     RESTRT                  ;IF NOT, CONTINUE TESTING
016212  000005                        RESET
016214  004711                LOGICAL:        JSR     PC,(R1)
016216  000240                        NOP
016220  000240                        NOP
016222  000240                        NOP
016224  000167  162752          RESTRT: JMP     BEGIN

                                        ;CHECK FOR LOOP ON CURRENT TEST
                                        ;CHECK FOR ITERATION SUPPRESSION

016230  032767  002000  161332  SCOPER: BIT     #SW10,SWR
016236  001030                        BNE     4$
016240  032767  040000  161322  1$:     BIT     #SW14,SWR
016246  001021                        BNE     3$
016250  032767  004000  161312        BIT     #SW11,SWR
016256  001006                        BNE     2$
016260  005267  001166                INC     LPCNT
016264  026767  001162  001156        CMP     LPCNT,ICOUNT
016272  001007                        BNE     3$
016274  005067  001152          2$:   CLR     LPCNT
016300  005067  001130                CLR     ERRFLG
016304  011667  001132                MOV     (SP),RETURN
016310  000002                        RTI
016312  016716  001124          3$:   MOV     RETURN,(SP)
016316  000002                        RTI
016320  005767  001110          4$:   TST     ERRFLG
016324  001745                        BEQ     1$
016326  000762                        BR      2$

                                        ;CHECK FOR FREEZE ON CURRENT DATA

016330  032767  001000  161232  SCOP1R: BIT     #SW09,SWR
016336  001402                        BEQ     1$
016340  016716  001102                MOV     FREEZ1,(SP)
016344  000002                  1$:   RTI

                                        ;ERROR HANDLER

016346  032767  020000  161214  ERRORS: BIT     #SW13,SWR
016354  001051                        BNE     HALTS
```

```
 3970  016356  021667  001116                        CMP     (SP),LAST
 3971  016362  001404                                BEQ     1$
 3972  016364  011667  001110                        MOV     (SP),LAST
 3973  016370  005067  001040                        CLR     ERRFLG
 3974  016374  104406                        1$:     SAVOSP
 3975  016376  011605                                MOV     (SP),R5
 3976  016400  162705  000002                        SUB     #2,R5
 3977  016404  011504                                MOV     (R5),R4
 3978  016406  006304                                ASL     R4
 3979  016410  006304                                ASL     R4
 3980  016412  042704  177001                        BIC     #177001,R4
 3981  016416  062704  020164                        ADD     #ERRTAB,R4
 3982  016422  012467  000034                        MOV     (R4)+,ERRMSG
 3983  016426  011467  000042                        MOV     (R4),DATABP
 3984  016432  005767  000776                        TST     ERRFLG
 3985  016436  001403                                BEQ     TYPMSG
 3986  016440  005767  000030                        TST     DATABP
 3987  016444  001007                                BNE     TYPDAT
 3988  016446  104402                    TYPMSG:     OCTASC
 3989  016450  016542                                ERTABO
 3990  016452  012767  000001  000754                MOV     #1,ERRFLG
 3991  016460  104401                                TYPE
 3992  016462  000000                    ERRMSG:     0
 3993  016464  005767  000004                TYPDAT: TST     DATABP
 3994  016470  001402                                BEQ     RESREG
 3995  016472  104402                                OCTASC
 3996  016474  000000                    DATABP:     0
 3997  016476  104407                    RESREG:     RESO5
 3998  016500  005767  161064                HALTS:  TST     SWR
 3999  016504  100005                                BPL     EXITER
 4000  016506  010046                                PUSHRO
 4001  016510  016600  000002                        MOV     2(SP),RO
 4002  016514  000000                                HALT
 4003  016516  012600                                POPRO
 4004  016520  005267  000714                EXITER: INC     ERRCNT
 4005  016524  032767  002000  161036                BIT     #SW10,SWR
 4006  016532  001402                                BEQ     1$
 4007  016534  016716  000704                        MOV     ESCAPE,(SP)
 4008  016540  000002                        1$:     RTI
 4009  016542  000001                    ERTABO:     1
 4010  016544     006     002                        .BYTE   6,2
 4011  016546  017472                                SAVPC
 4012                                               ;TRAP DISPATCH SERVICE
 4013                                               ;ARGUMENT OF TRAP IS EXTRACTED
 4014                                               ;AND USED AS OFFSET TO OBTAIN POINTER
 4015                                               ;TO SELECTED SUBROUTINE
 4016
 4017  016550  011646                    TRPSRV:     MOV     (SP),-(SP)      ;GET PC OF RETURN
 4018  016552  162716  000002                        SUB     #2,(SP)         ;=PC OF TRAP
 4019  016556  017616  000000                        MOV     @(SP),(SP)      ;GET TRP
 4020  016562  006316                    TRPOK:      ASL     (SP)            ;MULTIPLY TRAP ARG BY 2
 4021  016564  042716  177001                        BIC     #177001,(SP)    ;CLEAR UNWANTED BITS
 4022  016570  062716  020104                        ADD     #TRPTAB,(SP)    ;POINTER TO SUBROUTINE ADDRESS
 4023  016574  017616  000000                        MOV     @(SP),(SP)      ;SUBROUTINE ADDRESS
 4024  016600  000136                                JMP     @(SP)+          ;GO TO SUBROUTINE
 4025
```

```
4026                                                    ;TELETYPE OUTPUT ROUTINE
4027
4028  016602  017605  000000          TYPER:  MOV     @(SP),R5
4029  016606  062716  000002                  ADD     #2,(SP)
4030  016612  105777  000560          1$:     TSTB    @TPCSR
4031  016616  100375                          BPL     1$
4032  016620  105715                          TSTB    (R5)
4033  016622  001001                          BNE     2$
4034  016624  000002                          RTI
4035  016626  112577  000546          2$:     MOVB    (R5)+,@TPDBR
4036  016632  000767                          BR      1$
4037
4038                                                    ;ASCII STRING INPUT ROUTINE
4039
4040  016634  017667  000000  000006  INSTRG: MOV     @(SP),MSG
4041  016642  062716  000002                  ADD     #2,(SP)
4042  016646  104401                  INSTR1: TYPE
4043  016650  000000                  MSG:    0
4044  016652  012704  020126                  MOV     #INBUF,R4
4045  016656  012703  000007                  MOV     #7,R3
4046  016662  105777  000504          1$:     TSTB    @TKCSR
4047  016666  100375                          BPL     1$
4048  016670  117714  000500                  MOVB    @TKDBR,(R4)
4049  016674  142714  000200                  BICB    #200,(R4)
4050  016700  122427  000015                  CMPB    (R4)+,#15
4051  016704  001413                          BEQ     INSTR2
4052  016706  117777  000462  000464          MOVB    @TKDBR,@TPDBR
4053  016714  105777  000456          2$:     TSTB    @TPCSR
4054  016720  100375                          BPL     2$
4055  016722  005303                          DEC     R3
4056  016724  001356                          BNE     1$
4057  016726  104401                  INSTRE: TYPE
4058  016730  017761                          MQM
4059  016732  000745                          BR      INSTR1
4060  016734  000002                  INSTR2: RTI
4061
4062                                                    ;CONVERT ASCII STRING TO OCTAL
4063
4064  016736  011605                  PARAMS: MOV     (SP),R5
4065  016740  012567  000146                  MOV     (R5)+,LOLIM
4066  016744  012567  000144                  MOV     (R5)+,HILIM
4067  016750  012567  000142                  MOV     (R5)+,DEVADR
4068  016754  112567  000140                  MOVB    (R5)+,LOBITS
4069  016760  112567  000135                  MOVB    (R5)+,ADRCNT
4070  016764  010516                          MOV     R5,(SP)
4071  016766  005005                  PARAM1: CLR     R5
4072  016770  012704  020126                  MOV     #INBUF,R4
4073  016774  122714  000015                  CMPB    #15,(R4)
4074  017000  001420                          BEQ     PARERR
4075  017002  121427  000060          1$:     CMPB    (R4),#60
4076  017006  002415                          BLT     PARERR
4077  017010  121427  000067                  CMPB    (R4),#67
4078  017014  003012                          BGT     PARERR
4079  017016  142714  000060                  BICB    #60,(R4)
4080  017022  152405                          BISB    (R4)+,R5
4081  017024  122714  000015                  CMPB    #15,(R4)
```

```
4082  017030  001406                        BEQ     LIMITS
4083  017032  006305                        ASL     R5
4084  017034  006305                        ASL     R5
4085  017036  006305                        ASL     R5
4086  017040  000760                        BR      1$
4087  017042  104404              PARERR:   INSTER
4088  017044  000750                        BR      PARAM1
4089
4090                                        ;TEST TO SEE IF NUMBER IS WITHIN LIMITS
4091
4092  017046  020567  000042      LIMITS:   CMP     R5,HILIM
4093  017052  101373                        BHI     PARERR
4094  017054  020567  000032                CMP     R5,LOLIM
4095  017060  103770                        BLO     PARERR
4096  017062  136705  000032                BITB    LOBITS,R5
4097  017066  001365                        BNE     PARERR
4098
4099                                        ;STORE NUMBER AT SPECIFIED ADDRESS
4100
4101  017070  016704  000022                MOV     DEVADR,R4
4102  017074  010524              1$:       MOV     R5,(R4)+
4103  017076  062705  000002                ADD     #2,R5
4104  017102  105367  000013                DECB    ADRCNT
4105  017106  001372                        BNE     1$
4106  017110  000002                        RTI
4107  017112  000000              LOLIM:    0
4108  017114  000000              HILIM:    0
4109  017116  000000              DEVADR:   0
4110  017120  000000              LOBITS:   0
4111          017121              ADRCNT=LOBITS+1
4112
4113                                        ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
4114
4115  017122  104401              OCTASN:   TYPE
4116  017124  017765                        MCRLF
4117  017126  017601  000000                MOV     @(SP),R1
4118  017132  062716  000002                ADD     #2,(SP)
4119  017136  012167  000130                MOV     (R1)+,WRDCNT
4120  017142  112167  000126      1$:       MOVB    (R1)+,CHRCNT
4121  017146  112167  000123                MOVB    (R1)+,SPACNT
4122  017152  013167  000120                MOV     @(R1)+,BINWRD
4123  017156  016704  000114      2$:       MOV     BINWRD,R4
4124  017162  116705  000106                MOVB    CHRCNT,R5
4125  017166  012700  020140                MOV     #TEMP,R0
4126  017172  010403              3$:       MOV     R4,R3
4127  017174  042703  177770                BIC     #177770,R3
4128  017200  062703  000260                ADD     #260,R3
4129  017204  110320                        MOVB    R3,(R0)+
4130  017206  006204                        ASR     R4
4131  017210  006204                        ASR     R4
4132  017212  006204                        ASR     R4
4133  017214  005305                        DEC     R5
4134  017216  001365                        BNE     3$
4135  017220  012703  020152                MOV     #MDATA,R3
4136  017224  114023              4$:       MOVB    -(R0),(R3)+
4137  017226  105367  000042                DECB    CHRCNT
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4138  017232  001374                        BNE     4$
4139  017234  105767  000035                TSTB    SPACNT
4140  017240  001405                        BEQ     6$
4141  017242  112723  000240        5$:     MOVB    #240,(R3)+
4142  017246  105367  000023                DECB    SPACNT
4143  017252  001373                        BNE     5$
4144  017254  105013                6$:     CLRB    (R3)
4145  017256  104401                        TYPE
4146  017260  020152                        MDATA
4147  017262  005367  000004                DEC     WRDCNT
4148  017266  001325                        BNE     .$
4149  017270  000002                        RTI
4150  017272  000000                WRDCNT: 0
4151  017274  000000                CHRCNT: 0
4152          017275                SPACNT=CHRCNT+1
4153  017276  000000                BINWRD: 0
4154
4155                                        ;SAVE PC OF TEST THAT FAILED AND R0-R5
4156
4157  017300  016667  000004  000164 SVOSP: MOV     4(SP),SAVPC
4158
4159                                        ;SAVE R0-R5
4160
4161  017306  010567  000154        SVO5:   MOV     R5,SAVR5
4162  017312  010467  000146                MOV     R4,SAVR4
4163  017316  010367  000140                MOV     R3,SAVR3
4164  017322  010267  000132                MOV     R2,SAVR2
4165  017326  010167  000124                MOV     R1,SAVR1
4166  017332  010067  000116                MOV     R0,SAVR0
4167  017336  000002                        RTI
4168                                        ;RESTORE R0-R5
4169
4170  017340  016700  000110        RSO5:   MOV     SAVR0,R0
4171  017344  016701  000106                MOV     SAVR1,R1
4172  017350  016702  000104                MOV     SAVR2,R2
4173  017354  016703  000102                MOV     SAVR3,R3
4174  017360  016704  000100                MOV     SAVR4,R4
4175  017364  016705  000076                MOV     SAVR5,R5
4176  017370  000002                        RTI
4177                                        ;INDIRECT POINTERS
4178
4179  017372  177560                TKCSR:  177560
4180  017374  177562                TKDBR:  177562
4181  017376  177564                TPCSR:  177564
4182  017400  177566                TPDBR:  177566
4183  017402  000000                DHSCR:  0
4184  017404  000000                DHNRC:  0
4185  017406  000000                DHLPR:  0
4186  017410  000000                DHBA:   0
4187  017412  000000                DHBC:   0
4188  017414  000000                DHBAR:  0
4189  017416  000000                DHBCR:  0
4190  017420  000000                DHSSR:  0
4191  017422  000000                DHSLR:  0
4192  017424  000000                DHRVEC: 0
4193  017426  000000                DHRLVL: 0
```

```
                                DHTVEC: 0
                                DHTLVL: 0
                                        ;PROGRAM VARIABLES
                                ERRFLG: 0               ;ERROR FLAG
                                PASCNT: 0               ;PASS COUNT
                                ERRCNT: 0               ;ERROR COUNT
                                RETURN: 0               ;SCOPE RETURN ADDRESS FOR TEST LOOPING
                                ESCAPE: 0               ;ADDRESS FOR ERROR ESCAPE
                                FREEZ1: 0               ;DATA LOOPING RETURN ADDRESS
                                ICOUNT: 0               ;ITERATION COUNT FOR TEST IN PROGRESS
                                LPCNT:  0               ;NUMBER OF ITERATIONS THIS TEST
                                SAVR0:  0               ;R0 SAVE AREA
                                SAVR1:  0               ;R1 SAVE AREA
                                SAVR2:  0               ;R2 SAVE AREA
                                SAVR3:  0               ;R3 SAVE ARE
                                SAVR4:  0               ;R4 SAVE AREA
                                SAVR5:  0               ;R5 SAVE AREA
                                SAVSP:  0               ;STACK POINTER SAVE AREA
                                SAVPC:  0               ;CALLING ROUTINE SAVE AREA
                                INIFLG: 0               ;PROGRAM INITIALIZATION FLAG
                                STFLG:  0               ;PROGRAM START FLAG
                                LAST:   0               ;LAST ERROR PC
                                        ;ENTER HERE ON POWER FAILURE

017502  010046          PFAIL:  MOV     R0,-(SP)        ;SAVE R0-R5 ON PROCESSOR STACK
017504  010146                  MOV     R1,-(SP)
017506  010246                  MOV     R2,-(SP)
017510  010346                  MOV     R3,-(SP)
017512  010446                  MOV     R4,-(SP)
017514  010546                  MOV     R5,-(SP)
017516  016746  160302          MOV     24,-(SP)
017522  010667  177742          MOV     SP,SAVSP        ;SAVE STACK POINTER
017526  012767  017540  160270  MOV     #RESTART,24     ;SET UP FOR POWER UP TRAP
017534  000000                  HALT                    ;HALT ON POWER DOWN NORMAL
017536  000777                  BR      .

                                ;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED

017540  016706  177724  RESTAR: MOV     SAVSP,SP        ;RESTORE STACK POINTER
017544  012605                  MOV     (SP)+,R5        ;RESTORE R0-R5
017546  012604                  MOV     (SP)+,R4
017550  012603                  MOV     (SP)+,R3
017552  012602                  MOV     (SP)+,R2
017554  012601                  MOV     (SP)+,R1
017556  012600                  MOV     (SP)+,R0
017560  012767  017502  160236  MOV     #PFAIL,24       ;SET UP FOR POWER FAILURE
017566  012767  000340  160202  MOV     #340,PS
017574  012706  021106          MOV     #STACK,SP
017600  005067  000334          CLR     TEMP
017604  005267  000330          INC     TEMP
017610  001375                  BNE     .-4
017612  104402                  OCTASC
017614  017636                  PFTAB
017616  104401                  TYPE
```

```
 4250  017620  017770                              MPFAIL
 4251  017622  005067  177606                      CLR     ERRFLG
 4252  017626  005067  177646                      CLR     LAST
 4253  017632  000177  177604                      JMP     @RETURN
 4254  017636  000001                      PFTAB:  1
 4255  017640  000006  000002                      6,2
 4256  017644  000207                              RETURN
 4257  017646  005015  042012  030510  MTITLE: .ASCIZ  <15><12><12>/DH11 STATIC LOGIC TEST /<15><12>
 4258  017654  020061  052123  052101
 4259  017662  041511  046040  043517
 4260  017670  041511  052040  051505
 4261  017676  020124  005015     000
 4262  017703     015  053012  041505  MVECTO: .ASCIZ  <15><12>/VECTOR ADDRESS-/
 4263  017710  047524  020122  042101
 4264  017716  051104  051505  026523
 4265  017724     000
 4266  017725     015  041412  047117  MREGAD: .ASCIZ  <15><12>/CONTROL REGISTER ADDRESS-/
 4267  017732  051124  046117  051040
 4268  017740  043505  051511  042524
 4269  017746  020122  042101  051104
 4270  017754  051505  026523     000
 4271  017761     040  037440     000  MQM:    .ASCIZ  /  ?/
 4272  017765     015  000012          MCRLF:  .ASCIZ   <15><12>
 4273  017770  020040  047520  042527  MPFAIL: .ASCIZ  /  POWER FAILURE, PROGRAM RESTART AT TEST IN PROGRESS/
 4274  017776  020122  040506  046111
 4275  020004  051125  026105  050040
 4276  020012  047522  051107  046501
 4277  020020  051040  051505  040524
 4278  020026  052122  040440  020124
 4279  020034  042524  052123  044440
 4280  020042  020116  051120  043517
 4281  020050  042522  051523     000
 4282  020055     015  042012  042132  MEPASS: .ASCIZ  <15><12>/DZDHA/
 4283  020062  040510     000
 4284  020065     015  051012     000  MR:     .ASCIZ  <15><12>/R/
 4285  020071     015  052012  051505  MTSTPC: .ASCIZ  <15><12>/TEST PC-
 4286  020076  020124  041520  000055
 4287
 4288                                              ;TABLE OF POINTERS FOR TRAP DECODING
 4289
 4290  020104  016230                      TRPTAB: SCOPER
 4291  020106  016602                              TYPER
 4292  020110  017122                              OCTASN
 4293  020112  016634                              INSTRG
 4294  020114  016726                              INSTRE
 4295  020116  016736                              PARAMS
 4296  020120  017300                              SVOSP
 4297  020122  017340                              RSOS
 4298  020124  016330                              SCOP1R
 4299
 4300                                              ;BUFFERS FOR INPUT-OUTPUT
 4301
 4302  020126  000000                      INBUF:  0
 4303          020140                      .=.+10
 4304  020140  000000                      TEMP:   0
 4305          020152                      .=.+10
```

```
 4306  020152  000000                    MDATA:  0
 4307          020164                    .=.+10
 4308
 4309                                            ;TABLE OF POINTERS TO ERROR MESSAGES AND DATA
 4310
 4311  020164                            ERRTAB:
 4312  020164  020214                            EM0
 4313  020166  020672                            DT0
 4314  020170  020256                            EM1
 4315  020172  020670                            DT1
 4316  020174  020345                            EM2
 4317  020176  020670                            DT1
 4318  020200  020434                            EM3
 4319  020202  020670                            DT1
 4320  020204  020522                            EM4
 4321  020206  020670                            DT1
 4322  020210  020606                            EM5
 4323  020212  020670                            DT1
 4324  020214  042522  044507  052123  EM0:     .ASCII  /REGISTER DID NOT RESPOND/
 4325  020222  051105  042040  042111
 4326  020230  047040  052117  051040
 4327  020236  051505  047520  042116
 4328  020244  005015  042101  051104            .ASCIZ  <15><12>/ADDRESS/
 4329  020252  051505  000123
 4330  020256  054523  052123  046505  EM1:     .ASCII  /SYSTEM CONTROL REGISTER ERROR/
 4331  020264  041440  047117  051124
 4332  020272  046117  051040  043505
 4333  020300  051511  042524  020122
 4334  020306  051105  047522     122
 4335  020313     015  042412  050130            .ASCIZ  <15><12>/EXP     REC     ADDRESS/
 4336  020320  020040  020040  051040
 4337  020326  041505  020040  020040
 4338  020334  040440  042104  042522
 4339  020342  051523     000
 4340  020345     114  047111  020105  EM2:     .ASCII  /LINE PARAMETER REGISTER ERROR/
 4341  020352  040520  040522  042515
 4342  020360  042524  020122  042522
 4343  020366  044507  052123  051105
 4344  020374  042440  051122  051117
 4345  020402  005015  054105  020120            .ASCIZ  <15><12>/EXP     REC     ADDRESS/
 4346  020410  020040  020040  042522
 4347  020416  020103  020040  020040
 4348  020424  042101  051104  051505
 4349  020432  000123
 4350  020434  051102  040505  020113  EM3:     .ASCII  /BREAK CONTROL REGISTER ERROR/
 4351  020442  047503  052116  047522
 4352  020450  020114  042522  044507
 4353  020456  052123  051105  042440
 4354  020464  051122  051117
 4355  020470  005015  054105  020120            .ASCIZ  <15><12>/EXP     REC     ADDRESS/
 4356  020476  020040  020040  042522
 4357  020504  020103  020040  020040
 4358  020512  042101  051104  051505
 4359  020520  000123
 4360  020522  044523  047514  051440  EM4:     .ASCII  /SILO STATUS REGISTER ERROR/
 4361  020530  040524  052524  020123
```

```
 4362  020536  042522  044507  052123
 4363  020544  051105  042440  051122
 4364  020552  051117
 4365  020554  005015  054105  020120          .ASCIZ  <15><12>/EXP     REC     ADDRESS/
 4366  020562  020040  020040  042522
 4367  020570  020103  020040  020040
 4368  020576  042101  051104  051505
 4369  020604  000123
 4370  020606  040515  052123  051105  EMS:    .ASCII  /MASTER CLEAR ERROR/
 4371  020614  041440  042514  051101
 4372  020622  042440  051122  051117
 4373  020630  005015  054105  020120          .ASCIZ  <15><12>/EXP     REC     ADDRESS/
 4374  020636  020040  020040  042522
 4375  020644  020103  020040  020040
 4376  020652  042101  051104  051505
 4377  020660  000123
 4378                                  .EVEN
 4379  020662  000001                  DTO:    1
 4380  020664     006        000       .BYTE   6,0
 4381  020666  017466                          SAVR5
 4382  020670  000003                  DT1:    3
 4383  020672     006        002       .BYTE   6,2
 4384  020674  017466                          SAVR5
 4385  020676     006        002       .BYTE   6,2
 4386  020700  017464                          SAVR4
 4387  020702     006        000       .BYTE   6,0
 4388  020704  017462                          SAVR3
 4389  020706  000000                  ENDCOD: 0
 4390          000001                  .END
```

DZDHAB.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

```
ADRCNT= 017121           4069*  4104*  4111#
BEGIN   001202            894    923    929#  3935
BINWRD  017276           4122*  4123   4153#
BITC  = 000020           1796#  1821#  1846#  1871#  1896#  1921#  1946#  1971#  1996#  2021#  2046#  2071#  2096#
                         2121#  2146#  2171#  2196#  2221#  2246#  2271#  2296#  2321#  2346#  2371#  2396#  2421#
                         2446#  2471#  2496#  2521#  2546#  2571#  2598#  2625#  2652#  2679#  2706#  2733#  2760#
                         2790#  2820#  2850#  2880#  2910#  2940#  2970#  3000#  3030#  3060#  3090#  3120#  3150#
                         3180#  3210#  3240#  3270#  3300#  3330#  3360#  3390#  3420#  3450#  3480#  3510#  3540#
                         3570#  3600#  3630#  3660#  3690#  3722#  3754#  3786#  3818#  3850#  3882#  3914#
BITCLR= 000077           2760#  2790#  2820#  2850#  2880#  2910#  2940#  2970#  3000#  3030#  3060#  3090#  3120#
                         3150#  3180#  3210#  3240#  3270#  3300#  3330#  3360#  3390#  3420#  3450#  3480#  3510#
                         3540#  3570#  3600#  3630#  3660#  3690#  3722#  3754#  3786#  3818#  3850#  3882#
BITX  = 000000           1796#  1821#  1846#  1871#  1896#  1921#  1946#  1971#  1996#  2021#  2046#  2071#  2096#
                         2121#  2146#  2171#  2196#  2221#  2246#  2271#  2296#  2321#  2346#  2371#  2396#  2421#
                         2446#  2471#  2496#  2521#  2546#  2571#  2598#  2625#  2652#  2679#  2706#  2733#  2760#
                         2790#  2820#  2850#  2880#  2910#  2940#  2970#  3000#  3030#  3060#  3090#  3120#  3150#
                         3180#  3210#  3240#  3270#  3300#  3330#  3360#  3390#  3420#  3450#  3480#  3510#  3540#
                         3570#  3600#  3630#  3660#  3690#  3722#  3754#  3786#  3818#  3850#  3882#  3914#
BIT00 = 000001            580#  1233   1234   1236   1243
BIT01 = 000002            579#  1263   1264   1266   1273
BIT02 = 000004            578#  1293   1294   1296   1303
BIT03 = 000010            577#  1323   1324   1326   1333
BIT04 = 000020            576#  1353   1354   1356   1363
BIT05 = 000040            575#  1383   1384   1386   1393
BIT06 = 000100            574#  1413   1414   1416   1423
BIT07 = 000200            573#  1559   1667   1668   1671   1679   1680   1682   1688
BIT08 = 000400            572#  1579
BIT09 = 001000            571#  1443   1444   1446   1453   1666   1668   1671   1678   1687   1689   1692   1714
                         1716   1719   1726   1735   1737   1740   1762   1764   1767   1774   1783   1785   1788
BIT10 = 002000            570#  1599   1715   1716   1719   1727   1728   1730   1736
BIT11 = 004000            569#  1144   1166   1188   1210   1619   1806   1831   1856   1881   1906   1931   1956
                         1981   2006   2031   2056   2081   2106   2131   2156   2181   2206   2231   2256   2281
                         2306   2331   2356   2381   2406   2431   2456   2481   2506   2531   2556   2581   2606
                         2635   2662   2689   2716   2743   2771   2801   2831   2861   2891   2921   2951   2981
                         3011   3041   3071   3101   3131   3161   3191   3221   3251   3281   3311   3341   3371
                         3401   3431   3461   3491   3521   3551   3581   3611   3641   3671   3701   3733   3765
                         3797   3829   3861   3893
BIT12 = 010000            568#  1473   1474   1476   1483
BIT13 = 020000            567#  1503   1504   1506   1513
BIT14 = 040000            566#  1639   1763   1764   1767   1775   1776   1778   1784
BIT15 = 100000            565#  1533   1534   1536   1543
CBIT  = 000020           1796#  2171#  2571#  2760#  3210#  3690#
CCRBIT= 077777           2760#  2790#  2820#  2850#  2880#  2910#  2940#  2970#  3000#  3030#  3060#  3090#  3120#
                         3150#  3180#  3690#  3722#  3754#  3786#  3818#  3850#  3882#
CHRCNT  017274           4120*  4124   4137*  4151#  4152
CLRBIT= 000077           2760#  2790#  2820#  2850#  2880#  2910#  2940#  2970#  3000#  3030#  3060#  3090#  3120#
                         3150#  3180#  3210#  3240#  3270#  3300#  3330#  3360#  3390#  3420#  3450#  3480#  3510#
                         3540#  3570#  3600#  3630#  3660#  3690#  3703   3722#  3735   3754#  3767   3786#  3799
                         3818#  3831   3850#  3863   3882#  3895
DATABP  016474           3983*  3986   3993   3996#
DEVADR  017116           4067*  4101   4109#
DHBA    017410           1028   1032   4186#
DHBAR   017414           1097   1101   4188#
DHBC    017412           1051   1055   4187#
DHBCR   017416           1074   1078   1186*  1189   1196   2182   2207   2232   2257   2282   2307   2332   2357
                         2382   2407   2432   2457   2482   2507   2532   2557   3222   3252   3282   3312   3342
```

DZDHAB.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

```
                    3372    3402    3432    3462    3492    3522    3552    3582    3612    3642    3672    4189#
DHLPR   017406      1005    1009    1164*   1167    1174    1807    1832    1857    1882    1907    1932    1957    1982
                    2007    2032    2057    2082    2107    2132    2157    2772    2802    2832    2862    2892    2922
                    2952    2982    3012    3042    3072    3102    3132    3162    3192    4185#
DHNRC   017404       982     986    4184#
DHRLVL  017426      4193#
DHRVEC  017424       909    4192#
DHSCR   017402       917     959     963    1142*   1144*   1145    1152    1166*   1188*   1210*   1232    1262    1292
                    1322    1352    1382    1412    1442    1472    1502    1532    1559*   1562    1566    1568    1579*
                    1582    1586    1588    1599*   1602    1606    1608    1619*   1622    1626    1628    1639*   1642
                    1646    1648    1665    1713    1761    1806*   1831*   1856*   1881*   1906*   1931*   1956*   1981*
                    2006*   2031*   2056*   2081*   2106*   2131*   2156*   2181*   2206*   2231*   2256*   2281*   2306*
                    2331*   2356*   2381*   2406*   2431*   2456*   2481*   2506*   2531*   2556*   2581*   2608*   2635*
                    2662*   2689*   2716*   2743*   2771*   2801*   2831*   2861*   2891*   2921*   2951*   2981*   3011*
                    3041*   3071*   3101*   3131*   3161*   3191*   3221*   3251*   3281*   3311*   3341*   3371*   3401*
                    3431*   3461*   3491*   3521*   3551*   3581*   3611*   3641*   3671*   3701*   3733*   3765*   3797*
                    3829*   3861*   3892*   4183#
DHSLR   017422       920*    921*   4191#
DHSSR   017420       920    1120    1124    1208*   1211    1219    2582    2609    2636    2663    2690    2717    2744
                    3702    3734    3766    3798    3830    3862    3894    4190#
DHTLVL  017432      4195#
DHTVEC  017430      4194#
DTO     020662      4313    4379#
DT1     020670      4315    4317    4319    4321    4323    4382#
EM0     020214      4312    4324#
EM1     020256      4314    4330#
EM2     020345      4316    4340#
EM3     020434      4318    4350#
EM4     020522      4320    4360#
EM5     020606      4322    4370#
ENDCOD  020706       552    4389#
EOP     016156      3922#
ERRCNT  017440       885*    4004*   4200#
ERRFLG  017434       886*     887*   3925*   3950*   3955    3973*   3984    3990*   4198#   4251*
ERRMSG  016462      3982*   3992#
ERRORS  016346       845    3968#
ERRTAB  020164      3981    4311#
ERTABO  016542      3989    4009#
ESCAPE  017444       956*     979*   1002*   1025*   1048*   1071*   1094*   1117*   1141*   1163*   1185*   1207*   1231*
                    1261*   1291*   1321*   1351*   1381*   1411*   1441*   1471*   1501*   1531*   1558*   1578*   1598*
                    1618*   1638*   1664*   1712*   1760*   1805*   1830*   1855*   1880*   1905*   1930*   1955*   1980*
                    2005*   2030*   2055*   2080*   2105*   2130*   2155*   2180*   2205*   2230*   2255*   2280*   2305*
                    2330*   2355*   2380*   2405*   2430*   2455*   2480*   2505*   2530*   2555*   2580*   2607*   2634*
                    2661*   2688*   2715*   2742*   2770*   2800*   2830*   2860*   2890*   2920*   2950*   2980*   3010*
                    3040*   3070*   3100*   3130*   3160*   3190*   3220*   3250*   3280*   3310*   3340*   3370*   3400*
                    3430*   3460*   3490*   3520*   3550*   3580*   3610*   3640*   3670*   3700*   3732*   3764*   3796*
                    3828*   3860*   3892*   4007    4202#
EXITER  016520      3999    4004#
FREEZ1  017446      3963    4203#
HALTS   016500      3969    3998#
HILIM   017114      4066*   4092    4108#
ICOUNT  017450       955*    978*   1001*   1024*   1047*   1070*   1093*   1116*   1140*   1162*   1184*   1206*   1230*
                    1260*   1290*   1320*   1350*   1380*   1410*   1440*   1470*   1500*   1530*   1557*   1577*   1597*
                    1617*   1637*   1663*   1711*   1759*   1804*   1829*   1854*   1879*   1904*   1929*   1954*   1979*
                    2004*   2029*   2054*   2079*   2104*   2129*   2154*   2179*   2204*   2229*   2254*   2279*   2304*
                    2329*   2354*   2379*   2404*   2429*   2454*   2479*   2504*   2529*   2554*   2579*   2606*   2633*
```

```
                    2660*  2687*  2714*  2741*  2769*  2799*  2829*  2859*  2889*  2919*  2949*  2979*  3009*
                    3039*  3069*  3099*  3129*  3159*  3189*  3219*  3249*  3279*  3309*  3339*  3369*  3399*
                    3429*  3459*  3489*  3519*  3549*  3579*  3609*  3639*  3669*  3699*  3731*  3763*  3795*
                    3827*  3859*  3891*  3947   4204#
INBUF   020126      4044   4072   4302#
INIFLG  017474       889    922    924*  4214#
INSTER= 104404       862#  4087
INSTR = 104403       861#   904    912    933
INSTRE  016726      4057#  4294
INSTRG  016634      4040#  4293
INSTRI  016646      4042#  4059
INSTR2  016734      4051   4060#
LAST    017500      3924*  3970   3972*  4216#  4252*
LIGHTS= 177570       550#  3927*
LIMITS  017046      4082   4092#
LOBITS  017120      4068*  4096   4110#  4111
LOGICA  016214       868   3931#
LOLIM   017112      4065*  4094   4107#
LPCNT   017452      3946*  3947   3949*  4205#
MCRLF   017765      4116   4272#
MDATA   020152      4135   4146   4306#
MEPASS  020055      3923   4282#
MPFAIL  017770      4250   4273#
MQM     017761      4058   4271#
MR      020065       946   4284#
MREGAD  017725       913   4266#
MSG     016650      4040*  4043#
MTITLE  017646       888   4257#
MTSTPC  020071       934   4285#
MVECTO  017703       905   4262#
N     = 000001         1#
OCTASC= 104402       860#  3988   3995   4247
OCTASN  017122      4115#  4292
PARAM = 104405       863#   906    914    935
PARAMS  016736      4064#  4295
PARAM1  016766      4071#  4088
PARERR  017042      4074   4076   4078   4087#  4093   4095   4097
PASCNT  017436       884*  3926*  3927   4199#
PC    =%000007       545#  3931*
PFAIL   017502       843    882   4220#  4241
PFTAB   017636      4248   4254#
POPRO = 012600       559#  4003
POP1SP= 005726       557#
POP2SP= 022626       561#
PS    = 177776       551#   880*   929*   954*   977*  1000*  1023*  1046*  1069*  1092*  1115*  1139*  1161*
                    1183*  1205*  1229*  1259*  1289*  1319*  1349*  1379*  1409*  1439*  1469*  1499*  1529*
                    1556*  1576*  1596*  1616*  1636*  1662*  1710*  1758*  1803*  1828*  1853*  1878*  1903*
                    1928*  1953*  1978*  2003*  2028*  2053*  2078*  2103*  2128*  2153*  2178*  2203*  2228*
                    2253*  2278*  2303*  2328*  2353*  2378*  2403*  2428*  2453*  2478*  2503*  2528*  2553*
                    2578*  2605*  2632*  2659*  2686*  2713*  2740*  2768*  2798*  2828*  2858*  2888*  2918*
                    2948*  2978*  3008*  3038*  3068*  3098*  3128*  3158*  3188*  3218*  3248*  3278*  3308*
                    3338*  3368*  3398*  3428*  3458*  3488*  3518*  3548*  3578*  3608*  3638*  3668*  3698*
                    3730*  3762*  3794*  3826*  3858*  3890*  4242*
PUSHRO= 010046       558#  4000
PUSH1S= 005746       556#
PUSH2S= 024646       560#
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DZDHA8.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

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RESREG  016476          3994    3997#
RESTAR  017540          4228    4234#
RESTRT  016224          3929    3935#
RESOS = 104407           865#    3997
RETURN  017442           942*     947   3951*   3953   4201#   4253
RSOS    017340          4170#   4297
R0     =%000000          538#   4001*  4125*  4129*  4136   4166   4170*  4220   4240*
R1     =%000001          539#    895*   898*   900*   902   3928*  3931   4117*  4119   4120   4121   4122   4165
                        4171*   4221   4239*
R2     =%000002          540#    896*   898    899*   901*  4164   4172*  4222   4238*
R3     =%000003          541#    897*   900    901   1152*  1174*  1196*  1219*  1232*  1233*  1234   1239   1243*
                        1247    1262*  1263*  1264   1269   1273*  1277   1292*  1293*  1294   1299   1303*  1307
                        1322*   1323*  1324   1329   1333*  1337   1352*  1353*  1354   1359   1363*  1367   1382*
                        1383*   1384   1389   1393*  1397   1412*  1413*  1414   1419   1423*  1427   1442*  1443*
                        1444    1449   1453*  1457   1472*  1473*  1474   1479   1483*  1487   1502*  1503*  1504
                        1509    1513*  1517   1532*  1533*  1534   1539   1543*  1547   1568*  1588*  1608*  1628*
                        1648*   1665*  1666*  1667*  1668   1674   1678*  1679*  1680   1687*  1688*  1689   1695
                        1713*   1714*  1715*  1716   1722   1726*  1727*  1728   1735*  1736*  1737   1743   1761*
                        1762*   1763*  1764   1770   1774*  1775*  1776   1783*  1784*  1785   1791   1807*  1809*
                        1810    1814*  1815   1832*  1834*  1835   1839*  1840   1857*  1859*  1860   1864*  1865
                        1882*   1884*  1885   1889*  1890   1907*  1909*  1910   1914*  1915   1932*  1934*  1935
                        1939*   1940   1957*  1959*  1960   1964*  1965   1982*  1984*  1985   1989*  1990   2007*
                        2009*   2010   2014*  2015   2032*  2034*  2035   2039*  2040   2057*  2059*  2060   2064*
                        2065    2082*  2084*  2085   2089*  2090   2107*  2109*  2110   2114*  2115   2132*  2134*
                        2135    2139*  2140   2157*  2159*  2160   2164*  2165   2182*  2184*  2185   2189*  2190
                        2207*   2209*  2210   2214*  2215   2232*  2234*  2235   2239*  2240   2257*  2259*  2260
                        2264*   2265   2282*  2284*  2285   2289*  2290   2307*  2309*  2310   2314*  2315   2332*
                        2334*   2335   2339*  2340   2357*  2359*  2360   2364*  2365   2382*  2384*  2385   2389*
                        2390    2407*  2409*  2410   2414*  2415   2432*  2434*  2435   2439*  2440   2457*  2459*
                        2460    2464*  2465   2482*  2484*  2485   2489*  2490   2507*  2509*  2510   2514*  2515
                        2532*   2534*  2535   2539*  2540   2557*  2559*  2560   2564*  2565   2582*  2584*  2585
                        2590*   2591   2609*  2611*  2612   2617*  2618   2636*  2638*  2639   2644*  2645   2663*
                        2665*   2666   2671*  2672   2690*  2692*  2693   2698*  2699   2717*  2719*  2720   2725*
                        2726    2744*  2746*  2747   2752*  2753   2772*  2775*  2777*  2778   2782*  2783   2802*
                        2805*   2807*  2808   2812*  2813   2832*  2835*  2837*  2838   2842*  2843   2862*  2865*
                        2867*   2868   2872*  2873   2992*  2895*  2897*  2898   2902*  2903   2922*  2925*  2927*
                        2928    2932*  2933   2952*  2955*  2957*  2958   2962*  2963   2982*  2985*  2987*  2988
                        2992*   2993   3012*  3015*  3017*  3018   3022*  3023   3042*  3045*  3047*  3048   3052*
                        3053    3072*  3075*  3077*  3078   3082*  3083   3102*  3105*  3107*  3108   3112*  3113
                        3132*   3136*  3137*  3138   3142*  3143   3162*  3165*  3167*  3168   3172*  3173   3192*
                        3195*   3197*  3198   3202*  3203   3222*  3225*  3227*  3228   3232*  3233   3252*  3255*
                        3257*   3258   3262*  3263   3282*  3285*  3287*  3288   3292*  3293   3312*  3315*  3317*
                        3318    3322*  3323   3342*  3345*  3347*  3348   3352*  3353   3372*  3375*  3377*  3378
                        3382*   3383   3402*  3405*  3407*  3408   3412*  3413   3432*  3435*  3437*  3438   3442*
                        3443    3462*  3465*  3467*  3468   3472*  3473   3492*  3495*  3497*  3498   3502*  3503
                        3522*   3525*  3527*  3528   3532*  3533   3552*  3555*  3557*  3558   3562*  3563   3582*
                        3585*   3587*  3588   3592*  3593   3612*  3615*  3617*  3618   3622*  3623   3642*  3645*
                        3647*   3648   3652*  3653   3672*  3675*  3677*  3678   3682*  3683   3702*  3705*  3707*
                        3708    3713*  3714   3734*  3737*  3739*  3740   3745*  3746   3766*  3769*  3771*  3772
                        3777*   3778   3798*  3801*  3803*  3804   3809*  3810   3830*  3833*  3835*  3836   3841*
                        3842    3862*  3865*  3867*  3868   3873*  3874   3894*  3897*  3899*  3900   3905*  3906
                        4045*   4055*  4126*  4127*  4128*  4129   4135*  4136*  4141*  4144*  4163   4173*  4223
                        4237*
R4     =%000004          5428   1145*  1147   1167*  1169   1189*  1191   1211*  1213*  1214   1239*  1247*  1269*
                        1277*   1299*  1307*  1329*  1337*  1359*  1367*  1389*  1397*  1419*  1427*  1449*  1457*
                        1479*   1487*  1509*  1517*  1539*  1547*  1566*  1586*  1606*  1626*  1646*  1674*  1695*
```

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                1722*  1743*  1770*  1791*  1810*  1811   1815*  1816   1835*  1836   1840*  1841   1860*
                1861   1865*  1866   1885*  1886   1890*  1891   1910*  1911   1915*  1916   1935*  1936
                1940*  1941   1960*  1961   1965*  1966   1985*  1986   1990*  1991   2010*  2011   2015*
                2016   2035*  2036   2040*  2041   2060*  2061   2065*  2066   2085*  2086   2090*  2091
                2110*  2111   2115*  2116   2135*  2136   2140*  2141   2160*  2161   2165*  2166   2185*
                2186   2190*  2191   2210*  2211   2215*  2216   2235*  2236   2240*  2241   2260*  2261
                2265*  2266   2285*  2286   2290*  2291   2310*  2311   2315*  2316   2335*  2336   2340*
                2341   2360*  2361   2365*  2366   2385*  2386   2390*  2391   2410*  2411   2415*  2416
                2435*  2436   2440*  2441   2460*  2461   2465*  2466   2485*  2486   2490*  2491   2510*
                2511   2515*  2516   2535*  2536   2540*  2541   2560*  2561   2565*  2566   2585*  2586*
                2587   2591*  2592*  2593   2612*  2613*  2614   2618*  2619*  2620   2639*  2640*  2641
                2645*  2646*  2647   2666*  2667*  2668   2672*  2673*  2674   2693*  2694*  2695   2699*
                2700*  2701   2720*  2721*  2722   2726*  2727*  2728   2747*  2748*  2749   2753*  2754*
                2755   2778*  2779   2783*  2784   2808*  2809   2813*  2814   2838*  2839   2843*  2844
                2868*  2869   2873*  2874   2898*  2899   2903*  2904   2928*  2929   2933*  2934   2958*
                2959   2963*  2964   2988*  2989   2993*  2994   3018*  3019   3023*  3024   3048*  3049
                3053*  3054   3078*  3079   3083*  3084   3108*  3109   3113*  3114   3138*  3139   3143*
                3144   3168*  3169   3173*  3174   3198*  3199   3203*  3204   3228*  3229   3233*  3234
                3258*  3259   3263*  3264   3288*  3289   3293*  3294   3318*  3319   3323*  3324   3348*
                3349   3353*  3354   3378*  3379   3383*  3384   3408*  3409   3413*  3414   3438*  3439
                3443*  3444   3468*  3469   3473*  3474   3498*  3499   3503*  3504   3528*  3529   3533*
                3534   3558*  3559   3563*  3564   3588*  3589   3593*  3594   3618*  3619   3623*  3624
                3648*  3649   3653*  3654   3678*  3679   3683*  3684   3708*  3709*  3710   3714*  3715*
                3716   3740*  3741*  3742   3746*  3747*  3748   3772*  3773*  3774   3778*  3779*  3780
                3804*  3805*  3806   3810*  3811*  3812   3836*  3837*  3838   3842*  3843*  3844   3868*
                3869*  3870   3874*  3875*  3876   3900*  3901*  3902   3906*  3907*  3908   3977*  3978*
                3979*  3980*  3981*  3982   3983   4044*  4048*  4049*  4050   4072*  4073   4075   4077
                4079*  4080   4081   4101*  4102*  4123*  4126   4130*  4131*  4132*  4162   4174*  4224
                4236*
RS      =%000005  543*   963*   986*  1009*  1032*  1055*  1078*  1101*  1124*  1150*  1172*  1194*  1217*
                1236*  1245*  1266*  1275*  1296*  1305*  1326*  1335*  1356*  1365*  1386*  1395*  1416*
                1425*  1446*  1455*  1476*  1485*  1506*  1515*  1536*  1545*  1564*  1584*  1604*  1624*
                1644*  1671*  1682*  1692*  1719*  1730*  1740*  1767*  1778*  1788*  1808*  1809   1811
                1814   1818*  1833*  1834   1836   1839   1843*  1858*  1859   1861   1864   1868*  1883*
                1884   1886   1889   1893*  1908*  1909   1911   1914   1918*  1933*  1934   1936   1939
                1943*  1958*  1959   1961   1964   1968*  1983*  1984   1986   1989   1993*  2008*  2009
                2011   2014   2018*  2033*  2034   2036   2039   2043*  2058*  2059   2061   2064   2068*
                2083*  2084   2086   2089   2093*  2108*  2109   2111   2114   2118*  2133*  2134   2136
                2139   2143*  2158*  2159   2161   2164   2168*  2183*  2184   2186   2189   2193*  2208*
                2209   2211   2214   2218*  2233*  2234   2236   2239   2243*  2258*  2259   2261   2264
                2268*  2283*  2284   2286   2289   2293*  2308*  2309   2311   2314   2318*  2333*  2334
                2336   2339   2343*  2358*  2359   2361   2364   2368*  2383*  2384   2386   2389   2393*
                2408*  2409   2411   2414   2418*  2433*  2434   2436   2439   2443*  2458*  2459   2461
                2464   2468*  2483*  2484   2486   2489   2493*  2508*  2509   2511   2514   2518*  2533*
                2534   2536   2539   2543*  2558*  2559   2561   2564   2568*  2583*  2584   2587   2590
                2595*  2610*  2611   2614   2617   2622*  2637*  2638   2641   2644   2649*  2664*  2665
                2668   2671   2676*  2691*  2692   2695   2698   2703*  2718*  2719   2722   2725   2730*
                2745*  2746   2749   2752   2757*  2773*  2779   2786*  2803*  2809   2816*  2833*  2839
                2846*  2863*  2869   2876*  2893*  2899   2906*  2923*  2929   2936*  2953*  2959   2966*
                2983*  2989   2996*  3013*  3019   3026*  3043*  3049   3056*  3073*  3079   3086*  3103*
                3109   3116*  3133*  3139   3146*  3163*  3169   3176*  3193*  3199   3206*  3223*  3229
                3236*  3253*  3259   3266*  3283*  3289   3296*  3313*  3319   3326*  3343*  3349   3356*
                3373*  3379   3386*  3403*  3409   3416*  3433*  3439   3446*  3463*  3469   3476*  3493*
                3499   3506*  3523*  3529   3536*  3553*  3559   3566*  3583*  3589   3596*  3613*  3619
                3626*  3643*  3649   3656*  3673*  3679   3686*  3703*  3710   3718*  3735*  3742   3750*
                3767*  3774   3782*  3799*  3806   3814*  3831*  3838   3846*  3863*  3870   3878*  3895*
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                        3906    3910*   3975*   3976*   3977    4028*   4032    4035    4064*   4065    4066    4067    4068
                        4089    4070    4071*   4080*   4083*   4084*   4085*   4092    4094    4096    4102    4103*   4124*
                        4133*   4161    4175*   4225    4235*
SAVPC   017472          4011    4157*   4213#
SAVR0   017454          4166*   4170    4206#
SAVR1   017456          4165*   4171    4207#
SAVR2   017460          4164*   4172    4208#
SAVR3   017462          4163*   4173    4209#   4388
SAVR4   017464          4162*   4174    4210#   4386
SAVR5   017466          4161*   4175    4211#   4381    4384
SAVSP   017470          4212#   4227*   4234
SAVDSP= 104406           664#   3974
SCOPE = 104400           858#    970     993    1016    1039    1062    1085    1108    1131    1154    1176    1198    1221
                        1251    1281    1311    1341    1371    1401    1431    1461    1491    1521    1551    1571    1591
                        1611    1631    1651    1699    1747    1795    1820    1845    1870    1895    1920    1945    1970
                        1995    2020    2045    2070    2095    2120    2145    2170    2195    2220    2245    2270    2295
                        2320    2345    2370    2395    2420    2445    2470    2495    2520    2545    2570    2597    2624
                        2651    2678    2705    2732    2759    2789    2813    2849    2879    2909    2939    2969    2999
                        3029    3059    3089    3119    3149    3179    3209    3239    3269    3299    3329    3359    3389
                        3419    3449    3479    3509    3539    3569    3599    3629    3659    3689    3721    3753    3785
                        3817    3849    3881    3913
SCOPER  016230          3940#   4290
SCOPE1= 104410           866#
SCOP1R  016330          3961#   4298
SP     =%000006          544#    881*    930*    966*    989*   1012*   1035*   1058*   1081*   1104*   1127*   3951    3953*
                        3963*   3970    3972    3975    4001    4007*   4017*   4018*   4019*   4020*   4021*   4022*   4023*
                        4024    4028    4029*   4040    4041*   4064    4070*   4117    4118*   4157    4220*   4221*   4222*
                        4223*   4224*   4225*   4226*   4227    4234*   4235    4236    4237    4238    4239    4240    4243*
SPACNT= 017275          4121*   4139    4142*   4152#
STACK = 021106           552#    881     930    4243
START   001000           850     880#
STFLG   017476           883*    943     945*   4215#
SVOS    017306          4161#
SVOSP   017300          4157#   4296
SWR    = 177570          549#    893     931    3940    3942    3944    3961    3968    3998    4005
SW00   = 000001          532#    893
SW01   = 000002          531#    931
SW02   = 000004          530#
SW03   = 000010          529#
SW04   = 000020          528#
SW05   = 000040          527#
SW06   = 000100          526#
SW08   = 000400          525#
SW09   = 001000          524#   3961
SW10   = 002000          523#   3940    4005
SW11   = 004000          522#   3944
SW12   = 010000          521#
SW13   = 020000          520#   3968
SW14   = 040000          519#   3942
SW15   = 100000          518#
TEMP    020140          4125    4244*   4245*   4304#
TKCSR   017372          4046    4179#
TKDBR   017374          4048    4052    4180#
TPCSR   017376          4030    4053    4181#
TPDBR   017400          4035*   4052*   4182#
TRPOK   016562          4020#
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TRPSRV  016550            847   4017#
TRPTAB  020104           4022   4290#
TYPDAT  016464           3987   3993#
TYPE  = 104401            859#   888    946   3922   3991   4042   4057   4115   4145   4249
TYPER   016602           4028#  4291
TYPMSG  016446           3985   3988#
T1      001274            942    954#
T10     002140           1115#
T100    010236           2605#
T101    010336           2632#
T102    010436           2659#
T103    010536           2686#
T104    010636           2713#
T105    010736           2740#
T106    011036           2768#
T107    011142           2798#
T11     002234           1139#
T110    011246           2828#
T111    011352           2858#
T112    011456           2888#
T113    011562           2918#
T114    011666           2948#
T115    011772           2978#
T116    012076           3008#
T117    012202           3038#
T12     002314           1161#
T120    012306           3068#
T121    012412           3098#
T122    012516           3128#
T123    012622           3158#
T124    012726           3188#
T125    013032           3218#
T126    013136           3248#
T127    013242           3278#
T13     002374           1183#
T130    013346           3308#
T131    013452           3338#
T132    013556           3368#
T133    013662           3398#
T134    013766           3428#
T135    014072           3458#
T136    014176           3488#
T137    014302           3518#
T14     002454           1205#
T140    014406           3548#
T141    014512           3578#
T142    014616           3608#
T143    014722           3638#
T144    015026           3668#
T145    015132           3698#
T146    015246           3730#
T147    015362           3762#
T15     002540           1229#
T150    015476           3794#
T151    015612           3826#
T152    015726           3858#
```

DZDHAB.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

```
T153    016042          3890#
T16     002626          1259#
T17     002714          1289#
T2      001370           977#
T20     003002          1319#
T21     003070          1349#
T22     003156          1379#
T23     003244          1409#
T24     003332          1439#
T25     003420          1469#
T26     003506          1499#
T27     003574          1529#
T3      001464          1000#
T30     003662          1556#
T31     003736          1576#
T32     004012          1596#
T33     004066          1616#
T34     004142          1636#
T35     004216          1662#
T36     004346          1710#
T37     004476          1758#
T4      001560          1023#
T40     004626          1803#
T41     004716          1828#
T42     005006          1853#
T43     005076          1878#
T44     005166          1903#
T45     005256          1928#
T46     005346          1953#
T47     005436          1978#
T5      001654          1046#
T50     005526          2003#
T51     005616          2028#
T52     005706          2053#
T53     005776          2078#
T54     006066          2103#
T55     006156          2128#
T56     006246          2153#
T57     006336          2178#
T6      001750          1069#
T60     006426          2203#
T61     006516          2228#
T62     006606          2253#
T63     006676          2278#
T64     006766          2303#
T65     007056          2328#
T66     007146          2353#
T67     007236          2378#
T7      002044          1092#
T70     007326          2403#
T71     007416          2428#
T72     007506          2453#
T73     007576          2478#
T74     007666          2503#
T75     007756          2528#
T76     010046          2553#
```

DZDHAB.PFC CROSS REFERENCE TABLE -- USER SYMBOLS

```
CODEM1   871#   920
MLT      562#   964   987  1010  1033  1056  1079  1102  1125  1153  1175  1197  1220  1241  1249
        1271  1279  1301  1309  1331  1339  1361  1369  1391  1399  1421  1429  1451  1459  1481
        1489  1511  1519  1541  1549  1569  1589  1609  1629  1649  1676  1685  1697  1724  1733
        1745  1772  1781  1793  1813  1819  1838  1844  1863  1869  1888  1894  1913  1919  1938
        1944  1963  1969  1988  1994  2013  2019  2038  2044  2063  2069  2088  2094  2113  2119
        2138  2144  2163  2169  2188  2194  2213  2219  2238  2244  2263  2269  2288  2294  2313
        2319  2338  2344  2363  2369  2388  2394  2413  2419  2438  2444  2463  2469  2488  2494
        2513  2519  2538  2544  2563  2569  2589  2596  2616  2623  2643  2650  2670  2677  2697
        2704  2724  2731  2751  2758  2781  2788  2811  2818  2841  2848  2871  2878  2901  2908
        2931  2938  2961  2968  2991  2998  3021  3028  3051  3058  3081  3088  3111  3118  3141
        3148  3171  3178  3201  3208  3231  3238  3261  3268  3291  3298  3321  3328  3351  3358
        3381  3388  3411  3418  3441  3448  3471  3478  3501  3508  3531  3538  3561  3568  3591
        3598  3621  3628  3651  3658  3681  3688  3712  3720  3744  3752  3776  3784  3808  3816
        3840  3848  3872  3880  3904  3912
REGTS1   948#  1222  1252  1282  1312  1342  1372  1402  1432  1462  1492  1522
REGTS2   948#  1552  1572  1592  1612  1632
REGTS3   948#  1652  1700  1748
REGTS5   948#  1133  1155  1177  1199
REGTS6   948#  1796  1821  1846  1871  1896  1921  1946  1971  1996  2021  2046  2071  2096  2121
        2146  2171  2196  2221  2246  2271  2296  2321  2346  2371  2396  2421  2446  2471  2496
        2521  2546  2571  2598  2625  2652  2679  2706  2733
REGTS7   948#  2760  2790  2820  2850  2880  2910  2940  2970  3000  3030  3060  3090  3120  3150
        3180  3210  3240  3270  3300  3330  3360  3390  3420  3450  3480  3510  3540  3570  3600
        3630  3660  3690  3722  3754  3786  3818  3850  3882
RGADRS   948#   971   994  1017  1040  1063  1086  1109
TRPDEF     1#   858   859   860   861   862   863   864   865   866
TS         1#   954   977  1000  1023  1046  1069  1092  1115  1139  1161  1183  1205  1229  1259
        1289  1319  1349  1379  1409  1439  1469  1499  1529  1556  1576  1596  1616  1636  1662
        1710  1758  1803  1828  1853  1878  1903  1928  1953  1978  2003  2028  2053  2078  2103
        2128  2153  2178  2203  2228  2253  2278  2303  2328  2353  2378  2403  2428  2453  2478
        2503  2528  2553  2578  2605  2632  2659  2686  2713  2740  2768  2798  2828  2858  2888
        2918  2948  2978  3008  3038  3068  3098  3128  3158  3188  3218  3248  3278  3308  3338
        3368  3398  3428  3458  3488  3518  3548  3578  3608  3638  3668  3698  3730  3762  3794
        3826  3858  3890
.BUFFE     1#  4299
.CATCH     1#   581
.ENDCO     1#  4389
.EOP       1#  3915
.ERROR     1#  3965
.ERRTA     1#  4308
.HEADE     1#   496
.INSTR     1#  4037
.MSG       1#  4257
.OCTAS     1#  4112
.PARAM     1#  4061
.PFAIL     1#  4217
.POINT     1#  4177
.RESRE     1#  4168
.SAVRE     1#  4154
.SCOPE     1#  3936
.SCOPI     1#  3958
.SETVE     1#   839
.START     1#   871
.SYMBO     1#   515
.TRPDE     1#   853
```

```
.TRPSR      1#   4012
.TRPTA      1#   4287
.TYPER      1#   4025
.VARIA      1#   4196
```

DZDHAB.PFC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

```
ADD      900   901  3981  4022  4029  4041  4103  4118  4128
ASL     3978  3979  4020  4083  4084  4085
ASR     4130  4131  4132
BEQ      894   932  1149  1171  1193  1216  1235  1244  1265  1274  1295  1304  1325  1334  1355
        1364  1385  1394  1415  1424  1445  1454  1475  1484  1505  1514  1535  1544  1563  1583
        1603  1623  1643  1670  1681  1691  1718  1729  1739  1766  1777  1787  1812  1817  1837
        1842  1862  1867  1887  1892  1912  1917  1937  1942  1962  1967  1987  1992  2012  2017
        2037  2042  2062  2067  2087  2092  2112  2117  2137  2142  2162  2167  2187  2192  2212
        2217  2237  2242  2262  2267  2287  2292  2312  2317  2337  2342  2362  2367  2387  2392
        2412  2417  2437  2442  2462  2467  2487  2492  2512  2517  2537  2542  2562  2567  2588
        2594  2615  2621  2642  2648  2669  2675  2696  2702  2723  2729  2750  2756  2780  2785
        2810  2815  2840  2845  2870  2875  2900  2905  2930  2935  2960  2965  2990  2995  3020
        3025  3050  3055  3080  3085  3110  3115  3140  3145  3170  3175  3200  3205  3230  3235
        3260  3265  3290  3295  3320  3325  3350  3355  3380  3385  3410  3415  3440  3445  3470
        3475  3500  3505  3530  3535  3560  3565  3590  3595  3620  3625  3650  3655  3680  3685
        3711  3717  3743  3749  3775  3781  3807  3813  3839  3845  3871  3877  3903  3909  3929
        3956  3962  3971  3985  3994  4006  4051  4074  4082  4140
BGT     4078
BHI     4093
BIC     1213  1243  1273  1303  1333  1363  1393  1423  1453  1483  1513  1543  1678  1679  1688
        1726  1727  1736  1774  1775  1784  1814  1839  1864  1889  1914  1939  1964  1989  2014
        2039  2064  2089  2114  2139  2164  2189  2214  2239  2264  2289  2314  2339  2364  2389
        2414  2439  2464  2489  2514  2539  2564  2586  2590  2592  2613  2617  2619  2640  2644
        2646  2667  2671  2673  2694  2698  2700  2721  2725  2727  2748  2752  2754  2777  2807
        2837  2867  2897  2927  2957  2987  3017  3047  3077  3107  3137  3167  3197  3227  3257
        3287  3317  3347  3377  3407  3437  3467  3497  3527  3557  3587  3617  3647  3677  3707
        3709  3715  3739  3741  3747  3771  3773  3779  3803  3805  3811  3835  3837  3843  3867
        3869  3875  3899  3901  3907  3980  4021  4127
BICB    4049  4079
BIS     1144  1166  1188  1210  1667  1687  1715  1735  1763  1783  2782  2812  2842  2872  2902
        2932  2962  2992  3022  3052  3082  3112  3142  3172  3202  3232  3262  3292  3322  3352
        3382  3412  3442  3472  3502  3532  3562  3592  3622  3652  3682  3713  3745  3777  3809
        3841  3873  3905
BISB    4080
BIT      893   931  3940  3942  3944  3961  3968  4005
BITB    4096
BLO     4095
BLT     4076
BNE      890   903   923   944  3941  3943  3945  3948  3969  3987  4033  4056  4097  4105  4134
        4138  4143  4148  4246
BPL     3999  4031  4047  4054
BR       892   941   961   984  1007  1030  1053  1076  1099  1122  3957  4036  4059  4086  4088
        4230
CLR      883   884   885   886   887   899   969   992  1015  1038  1061  1084  1107  1130  1150
        1172  1194  1217  1245  1275  1305  1335  1365  1395  1425  1455  1485  1515  1545  1564
        1584  1604  1624  1644  1818  1843  1868  1893  1918  1943  1968  1993  2018  2043  2068
        2093  2118  2143  2168  2193  2218  2243  2268  2293  2318  2343  2368  2393  2418  2443
        2468  2493  2518  2543  2568  2595  2622  2649  2676  2703  2730  2757  3924  3925  3949
        3950  3973  4071  4244  4251  4252
CLRB    4144
CMP      902  1234  1264  1294  1324  1354  1384  1414  1444  1474  1504  1534  1668  1680  1689
        1716  1728  1737  1764  1776  1785  1811  1836  1861  1886  1911  1936  1961  1986  2011
        2036  2061  2086  2111  2136  2161  2186  2211  2236  2261  2286  2311  2336  2361  2386
        2411  2436  2461  2486  2511  2536  2561  2587  2614  2641  2668  2695  2722  2749  2779
        2784  2809  2814  2839  2844  2869  2874  2899  2904  2929  2934  2959  2964  2989  2994
        3019  3024  3049  3054  3079  3084  3109  3114  3139  3144  3169  3174  3199  3204  3229
```

DZDHAB.PFC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

```
        3234    3259    3264    3289    3294    3319    3324    3349    3354    3379    3384    3409    3414    3439    3444
        3469    3474    3499    3504    3529    3534    3559    3564    3589    3594    3619    3624    3649    3654    3679
        3684    3710    3716    3742    3748    3774    3780    3806    3812    3838    3844    3870    3876    3902    3908
        3947    3970    4092    4094
CMPB    4050    4073    4075    4077    4081
COM      924     945
DEC     4055    4133    4147
DECB    4104    4137    4142
EMT      562
HALT     584     586     588     590     592     594     596     598     600     602     604     606     608     610     612
         614     616     618     620     622     624     626     628     630     632     634     636     638     640     642
         644     646     648     650     652     654     656     658     660     662     664     666     668     670     672
         674     676     678     680     682     684     686     688     690     692     694     696     698     700     702
         704     706     708     710     712     714     716     718     720     722     724     726     728     730     732
         734     736     738     740     742     744     746     748     750     752     754     756     758     760     762
         764     766     768     770     772     774     776     778     780     782     784     786     788     790     792
         794     796     798     800     802     804     806     808     810     812     814     816     818     820     822
         824     826     828     830     832     834     836     838    4002    4229
INC      921    3926    3946    4004    4245
JMP      850     947    3935    4024    4253
JSR     3931
MOV      880     881     882     895     896     897     898     920     929     930     942     954     955     956     957
         958     963     966     968     977     978     979     980     981     986     989     991    1000    1001    1002
        1003    1004    1009    1012    1014    1023    1024    1025    1026    1027    1032    1035    1037    1046    1047
        1048    1049    1050    1055    1058    1060    1069    1070    1071    1072    1073    1078    1081    1083    1092
        1093    1094    1095    1096    1101    1104    1106    1115    1116    1117    1118    1119    1124    1127    1129
        1139    1140    1141    1142    1145    1152    1161    1162    1163    1164    1167    1174    1183    1184    1185
        1186    1189    1196    1205    1206    1207    1208    1211    1219    1229    1230    1231    1232    1233    1236
        1239    1247    1259    1260    1261    1262    1263    1266    1269    1277    1289    1290    1291    1292    1293
        1296    1299    1307    1319    1320    1321    1322    1323    1326    1329    1337    1349    1350    1351    1352
        1353    1356    1359    1367    1379    1380    1381    1382    1383    1386    1389    1397    1409    1410    1411
        1412    1413    1416    1419    1427    1439    1440    1441    1442    1443    1446    1449    1457    1469    1470
        1471    1472    1473    1476    1479    1487    1499    1500    1501    1502    1503    1506    1509    1517    1529
        1530    1531    1532    1533    1536    1539    1547    1556    1557    1558    1559    1566    1568    1576    1577
        1578    1579    1586    1588    1596    1597    1598    1599    1606    1608    1616    1617    1618    1619    1626
        1628    1636    1637    1638    1639    1646    1648    1662    1663    1664    1665    1666    1671    1674    1682
        1692    1695    1710    1711    1712    1713    1714    1719    1722    1730    1740    1743    1758    1759    1760
        1761    1762    1767    1770    1778    1788    1791    1803    1804    1805    1806    1807    1808    1809    1810
        1815    1828    1829    1830    1831    1832    1833    1834    1835    1840    1853    1854    1855    1856    1857
        1858    1859    1860    1865    1878    1879    1880    1881    1882    1883    1884    1885    1890    1903    1904
        1905    1906    1907    1908    1909    1910    1915    1928    1929    1930    1931    1932    1933    1934    1935
        1940    1953    1954    1955    1956    1957    1958    1959    1960    1965    1978    1979    1980    1981    1982
        1983    1984    1985    1990    2003    2004    2005    2006    2007    2008    2009    2010    2015    2028    2029
        2030    2031    2032    2033    2034    2035    2040    2053    2054    2055    2056    2057    2058    2059    2060
        2065    2078    2079    2080    2081    2082    2083    2084    2085    2090    2103    2104    2105    2106    2107
        2108    2109    2110    2115    2128    2129    2130    2131    2132    2133    2134    2135    2140    2153    2154
        2155    2156    2157    2158    2159    2160    2165    2178    2179    2180    2181    2182    2183    2184    2185
        2190    2203    2204    2205    2206    2207    2208    2209    2210    2215    2228    2229    2230    2231    2232
        2233    2234    2235    2240    2253    2254    2255    2256    2257    2258    2259    2260    2265    2278    2279
        2280    2281    2282    2283    2284    2285    2290    2303    2304    2305    2306    2307    2308    2309    2310
        2315    2328    2329    2330    2331    2332    2333    2334    2335    2340    2353    2354    2355    2356    2357
        2358    2359    2360    2365    2378    2379    2380    2381    2382    2383    2384    2385    2390    2403    2404
        2405    2406    2407    2408    2409    2410    2415    2428    2429    2430    2431    2432    2433    2434    2435
        2440    2453    2454    2455    2456    2457    2458    2459    2460    2465    2478    2479    2480    2481    2482
        2483    2484    2485    2490    2503    2504    2505    2506    2507    2508    2509    2510    2515    2528    2529
        2530    2531    2532    2533    2534    2535    2540    2553    2554    2555    2556    2557    2558    2559    2560
```

DZDHA8.PFC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

```
        2565  2578  2579  2580  2581  2582  2583  2584  2585  2591  2605  2606  2607  2608  2609
        2610  2611  2612  2618  2632  2633  2634  2635  2636  2637  2638  2639  2645  2659  2660
        2661  2662  2663  2664  2665  2666  2672  2686  2687  2688  2689  2690  2691  2692  2693
        2698  2713  2714  2715  2716  2717  2718  2719  2720  2726  2740  2741  2742  2743  2744
        2745  2746  2747  2753  2768  2769  2770  2771  2772  2773  2775  2778  2783  2786  2798
        2799  2800  2801  2802  2803  2805  2808  2813  2816  2828  2829  2830  2831  2832  2833
        2835  2838  2843  2846  2858  2859  2860  2861  2862  2863  2865  2868  2873  2876  2888
        2889  2890  2891  2892  2893  2895  2898  2903  2906  2918  2919  2920  2921  2922  2923
        2925  2928  2933  2936  2948  2949  2950  2951  2952  2953  2955  2958  2963  2966  2978
        2979  2980  2981  2982  2983  2985  2988  2993  2996  3008  3009  3010  3011  3012  3013
        3015  3018  3023  3026  3038  3039  3040  3041  3042  3043  3045  3048  3053  3056  3068
        3069  3070  3071  3072  3073  3075  3078  3083  3086  3098  3099  3100  3101  3102  3103
        3105  3108  3113  3116  3128  3129  3130  3131  3132  3133  3135  3138  3143  3146  3158
        3159  3160  3161  3162  3163  3165  3168  3173  3176  3188  3189  3190  3191  3192  3193
        3195  3198  3203  3206  3218  3219  3220  3221  3222  3223  3225  3228  3233  3236  3248
        3249  3250  3251  3252  3253  3255  3258  3263  3266  3278  3279  3280  3281  3282  3283
        3285  3288  3293  3296  3308  3309  3310  3311  3312  3313  3315  3318  3323  3326  3338
        3339  3340  3341  3342  3343  3345  3348  3353  3356  3368  3369  3370  3371  3372  3373
        3375  3378  3383  3386  3398  3399  3400  3401  3402  3403  3405  3408  3413  3416  3428
        3429  3430  3431  3432  3433  3435  3438  3443  3446  3458  3459  3460  3461  3462  3463
        3465  3468  3473  3476  3488  3489  3490  3491  3492  3493  3495  3498  3503  3506  3518
        3519  3520  3521  3522  3523  3525  3528  3533  3536  3548  3549  3550  3551  3552  3553
        3555  3558  3563  3566  3578  3579  3580  3581  3582  3583  3585  3588  3593  3596  3608
        3609  3610  3611  3612  3613  3615  3618  3623  3626  3638  3639  3640  3641  3642  3643
        3645  3648  3653  3656  3668  3669  3670  3671  3672  3673  3675  3678  3683  3686  3698
        3699  3700  3701  3702  3703  3705  3708  3714  3718  3730  3731  3732  3733  3734  3735
        3737  3740  3746  3750  3762  3763  3764  3765  3766  3767  3769  3772  3778  3782  3794
        3795  3796  3797  3798  3799  3801  3804  3810  3814  3826  3827  3828  3829  3830  3831
        3833  3836  3842  3846  3858  3859  3860  3861  3862  3863  3865  3868  3874  3878  3890
        3891  3892  3893  3894  3895  3897  3900  3906  3910  3927  3928  3951  3953  3963  3972
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        4243
MOVB    4035  4048  4052  4068  4069  4120  4121  4124  4129  4136  4141
NOP     3932  3933  3934
RESET   3930
RETURN   938  4256
RTI      967   990  1013  1036  1059  1082  1105  1128  3952  3954  3964  4008  4034  4060  4106
        4149  4167  4176
SUB     3976  4018
TRAP     858   859   860   861   862   863   864   865   866
TST      889   922   943   959   982  1005  1028  1051  1074  1097  1120  1147  1169  1191  1214
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        3986  3993  3998
TSTB    4030  4032  4046  4053  4139
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.END    4390
.ENDC    892   893   920   922   957   980  1003  1026  1049  1072  1095  1118  1142  1147  1164
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DZDHAB.PFC CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

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ERRORS DETECTED:  0
DEFAULT GLOBALS GENERATED:  0

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RUN-TIME RATIO: 129/69=1.8
CORE USED:  12K  (23 PAGES)
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JOB

Spooler runtime 16 Seconds, 70 KCS, 447 disk reads, 4 disk writes, 99 pages
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