

LPA/DMC-11

DIAGNOSTIC TEST 2
MD-11-DRLPM-A

EP-DRLPM-A-DL

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IDENTIFICATION

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1. ABSTRACT

This diagnostic is one of a series of diagnostics aimed at the the Ipa-11z system. please reference section 8.7 for a complete list.

The function of the m8200-yc diagnostics is to verify that the option operates according to specifications. The diagnostics verify that there are no malfunctions and the all operations of the m8200-yc are correct in its environment.

this diagnostic requires the user to recable the system, that is, the Ipa-11z i/o bus must join the unibus.

Parameters must be set up to alert the diagnostics to the m8200-yc configuration. These parameters are contained in the STATUS TABLE and are generated in two ways: 1) Manual Input - the operator answers questions. 2) Autosizing - the program determines the parameters automatically.

It performs jump tests on the micro-processor and verifies the control ROM of the MB200-yc. This diagnostic will not run on a KMC (MB204), however it is possible to load the KMC CRAM with the m8200-yc micro-code. See test 2 for details.

Currently there are two off line diagnostics that are to be run in sequence to insure that if an error should occur it will be detected at an early stage.

NOTE: Additional diagnostics may be added in the future.

The two diagnostics are:

1. DRLPL [REV] Basic W/R and Micro-processor tests
2. DRLPM [REV] Jump and CROM tests

2. REQUIREMENTS

2.1 EQUIPMENT

Any PDP11 family CPU (except an LSI-11) with minimum 8k memory ASR 33 (or equivalent)

2.2 STORAGE

Program will use all 8K of memory except where ABL and BOOTSTRAP LOADER reside. Locations 1500 thru 1640; contain the "STATUS TABLE" information which is generated at start of diagnostics by manual input (questions) or automatically (auto-sizing). This area is an overlay area and should not be altered by the operator.

3. LOADING PROCEDURE**3.1 METHOD**

All programs are in absolute format and are loaded using the ABSOLUTE LOADER. NOTE: if the diagnostics are on a media such as DISK, MAGTAPE, DECTAPE, or CASSETTE; follow instructions for the monitor which has been provided on that specific media.

ABSOLUTE LOADER starting address #500

MEMORY * SIZE

4k	17
8k	37
12k	57
16k	77
20k	117
24k	137
28k	157

- 3.1.1 Place address of ABS loader into switch register.
(also place 'HALT' SW up)
- 3.1.2 Depress 'LOAD ADDRESS' key on console and release.
- 3.1.3 Depress 'START KEY' on console and release (program should now be loading into CPU)

4. STARTING PROCEDURE

- a. Set switch register to 000200
- b. Depress 'LOAD ADDRESS' key and release
- c. Set SWR to zero for 'AUTO SIZING' or SWR bit0=1 for manual input (questions) or SWR bit7=1 to use existing parameters set up by a previous start or a previously run m8200-yc diagnostic.
- d. Depress 'START KEY' and release. The program will type Maindec Name and program name (if this was the first start up of the program) and also the following:

MAP OF M8200-YC STATUS

PC	CSR	STAT1	STAT2	STAT3
----	-----	-------	-------	-------

001500	160010	145310	177777	000000
--------	--------	--------	--------	--------

The program will type 'R' and proceed to run the diagnostic. The above is only an example. This would indicate the status table starting at add. 1500 in the program. In this example the table contains the information and status of an M8200-YC. THE STATUS TABLE MUST BE VERIFIED BY THE USER IF AUTO SIZING IS DONE. For information of status table see section 8.4 for help.

If the diagnostic was started with SW00=1 indicating manual parameter input then the following shows an example of the questions asked and some example answers:

HOW MANY M8200-YC'S TO BE TESTED?1

01

CSR ADDRESS?160010

VECTOR ADDRESS?310

BR PRIORITY LEVEL? (4,5,6,7)?5

FOLLOWING THE QUESTIONS THE STATUS MAP IS PRINTED OUT AS DESCRIBED ABOVE. THE INFORMATION IN THE MAP REFLECTS THE ANSWERS TO THE QUESTIONS. IF THE DIAGNOSTIC WAS STARTED WITH SW00=0 and SW07=0 (AUTO-SIZING) then no questions are asked and only the status-map is printed out. If AUTO-SIZING is used the status information must be verified to be correct (match the hardware). if it does not match the hardware the diagnostic must be restarted with SW00=1 and the questions answered.

4.1 CONTROL SWITCH SETTINGS

SW 15 Set: Halt on error
SW 14 Set: Loop on current test
SW 13 Set: Inhibit error print out
SW 12 Set: Inhibit type out/abell on error.
SW 11 Set: Inhibit iterations. (quick pass)
SW 10 Set: Escape to next test on error
SW 09 Set: Loop with current data
SW 08 Set: Catch error and loop on it
SW 07 Set: Use previous status table.
SW 06 Set: Halt in ROMCLK routine before clocking
micro-processor
SW 05 Set: Reserved
SW 04 Set: Reserved
SW 03 Set: Reselect m8200-uc's desired active
SW 02 Set: Lock on selected test
SW 01 Set: Restart program at selected test
SW 00 Set: Build new status table from questions. (If SW07=0
and SW00=0 a new status table is built by
auto-sizing)

Switch 06 and 08-15 are dynamic and can be changed as needed
while the diagnostic is running. Switches 00-03 and switch 07
are static, and are used only on starting or restarting the
diagnostic.

4.1.2 SWITCH REGISTER OPTIONS (at start up)

- SW 01 RESTART PROGRAM AT SELECTED TEST. It is strongly suggested that at least one pass has been made before trying to select a test, the reason being is that the program has to clear areas and set up parameters. When this switch is used the diagnostic will ask TEST NO.? Answer by typing the number of the test desired and carriage return to begin execution at the selected test.
- SW 02 LOCK ON SELECTED TEST. This switch when used with SW01 will cause the program to constantly loop on the selected test. Hitting any key on the console will let it advance to the next test and loop until a key is hit again. If SW02=0 when SW01 is used. The program will begin at the selected test and continue normal operations.
- SW 03 RESELECT M8200-YC'S DESIRED ACTIVE. Please note that a message is typed out for setting the switch register equal to m8200-yc's active. this means if the system has four m8200-yces; bits 00,01,02,03 will be set in loc 'DMACTV' from the switch register. Using this switch(SW00) alters that location; therefore if four m8200-yces are in the system ***DO NOT*** set switches greater than SW 03 in the up position. this would be a fatal error. do not select more active m8200-yc's than there is information on in the status table.
- METHOD: A: Load address 200
B: Start with SW 00=1
C: Program will type message
D: Set a switch for each m8200-yc desired active.
E: Number (IF VALID) will be in data lights
(excluding 11/05)
F: Set with any other switch settings desired.
PRESS CONTINUE.

4.1.3 DYNAMIC SWITCHES

ERROR SWITCHES

1. SW 12 Delete print out/bell on error.
2. SW 13 Delete error printout.
3. SW 15 Halt on the error.
4. SW 08 Goto beginning of the test(on error).
5. SW 10 Goto next test(on error).

SCOPE SWITCHES

1. SW06 Halt in ROMCLK routine before clocking micro-processor instruction. This allows the operator to scope a micro-processor instruction in the static state before it is clocked. Hit continue to resume running.
2. SW09 (if enabled by 'SCOP1') on an error: If an '*' is printed in front of the test no. (ex. *TEST NO. 10) SW09 is incorporated in that test and therefore SW09 is usually the best switch for the scope loop (SW14=0, SW10=0, SW09=1, SW08=0). If SW09 is not enabled; and there is a HARD error (constant): SW08 is best. (SW14=1,0, SW10=0, SW09=0, SW08=1). for intermittent errors; SW14=1 will loop on test regardless of error or not error. (SW14=1, SW10=0, SW09=0, SW08=1,0)
3. SW11 Inhibit iterations.
4. SW14 Loop on current test.

4.2 STARTING ADDRESS

Starting address is at 000200 there are no other starting addresses for the m8200-yc diagnostics. (See Section 4.0)

NOTE: If address 000042 is non-zero the program assumes it is under ACT11 or XXDP control and will act accordingly after all available m8200-yc's are tested the program will return to 'XXDP' or 'ACT-11'.

5. OPERATING PROCEDURE

When program is initially started messages as described in section 4.0 will be printed, and program will begin running the diagnostic

5.2 PROGRAM AND/OR OPERATOR ACTION

The typical approach should be

1. Halt on error (via SW 15=1) when ever an error occurs.
2. Clear SW 15.
3. Set SW 14: (loop on this test)
4. Set SW 13: (inhibit error print out)

The TEST NUMBER and PC will be typed out and possibly an error message (this depends on the test) to give the operator an idea as to the source of the problem. If it is necessary to know more information concerning the error report; LOOK IN THE LISTING for that TEST NUMBER which was typed out and then NOTE THE PC of the ERROR REPORT this way the EXACT FUNCTION of the test CAN BE DETERMINED.

6. ERRORS

As described previously there will always be a TEST NUMBER and PC typed out at the time of an error (providing SW 13=0 and SW 12=0). in most cases additional information will be supplied in the error message to give the operator an indication of the error.

6.2 ERROR RECOVERY

If for some reason the m8200-yc should 'HANG THE BUS' (gain control of bus so that console manual functions are inhibited) an init or power down/up is necessary for operator to regain control of cpu. If this should happen; look in location 'TSTNO' (address 1226) for the number of the test that was running at the time of the catastrophic error. In this way the operator will have an idea as to what the m8200-yc was doing at the time of the error.

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

See section 4. (PLEASE)
Status table should be verified regardless of how program was started. Also it is important to use this listing along with the information printed on the TTY to completely isolate problems.

7.2 OPERATING RESTRICTIONS

The first time a m8200-yc diagnostic is loaded into core and run the STATUS TABLE must be set up. This is done by manual input (SW00=1) or by autosizing (SW00=0 and SW07=0). Thereafter however the status table need not be setup by subsequent restarts or even loading the next m8200-yc diagnostic because the STATUS TABLE is overlayed. The current parameters in the STATUS TABLE are used when SW07=1 on start up.

m8200-yc must be on the unibus.

7.3 HARDWARE CONFIGURATION RESTRICTIONS

M8200-YC - Jumper W1 must be in, and switch 7 of E76 must be in the OFF position.

KMC(M8204)- Jumper W1 must be in.

8. MISCELLANEOUS

8.1 EXECUTION TIME

All m8200-yc device diagnostics will give an 'END PASS' message (providing no errors and sw12=0) within 4 mins. This is assuming SW11=1 (DELETE ITERATIONS) is set to give the fastest possible execution. The actual execution time depends greatly on the PDP11 CPU configuration and the amount of memory in the system.

8.2 PASS COMPLETE

NOTE: EVERY time the program is started; the tests will run as if SW11 (delete iterations) was up (=1). This is to 'VERIFY NO HARD ERRORS' as soon as possible. Therefore the first pass -EACH TIME PROGRAM IS STARTED- will be a 'QUICK PASS' until all m8200-yc's in system are tested. When the diagnostic has completed a pass the following is an example of the print out to be expected.

END PASS DZDMG CSR: 175000 VEC: 0300 PASSES: 000001
ERRORS: 000000

NOTE: The pass count and error counts are cumulative for each m8200-yc that is running, and are set to zero only when the diagnostic is started. Therefore after an overnight run for example, the total passes and errors for each M8200-YC since the diagnostic was started are reflected in PASSES: and ERRORS:.

8.4 KEY LOCATIONS

- RETURN (1214) Contains the address where program will return when iteration count is reached or if loop on test is asserted.
- NEXT (1216) Contains the address of the next test to be performed.
- TSTNO (1226) Contains the number of the test now being performed.
- RUN (1316) The bit in 'RUN' always points to the m8200-yc currently being tested. EXAMPLE: (RUN) 1302/0000000001000000 Means that m8200-yc no.06 is the m8200-yc now running.

DMCR00-DMCR17
DMST00-DMST17
(1500)-(1640)

These locations contain the information needed to test up to 16 (decimal) m8200-ycs sequentially. They contain the CSR, VECTOR and STATUS concerning the configuration of each m8200-yc.

- DMACTV (1306) Each bit set in this location indicates that the associated m8200-yc will be tested in turn. EXAMPLE: (DMACTV) 1276/0000000000011111 means that m8200-yc no. 00,01,02,03,04 will be tested. EXAMPLE: (DMACTV) 1276/00000000000010001 Means that m8200-yc no. 00,04 will be tested.
- DMCSR (1404) Contains the CSR of the current m8200-yc under test.

8.4A 'STATUS TABLE' (1500-1640)

The table is filled by AUTO SIZING or by the manual parameter input (questions) as described previously. Also if desired by user; the locations may be altered by hand (toggled in) to suit the specific configuration.

The example status map shown below contains information for two M8200-YC'S. the table can contain up to 16 M8200-YC'S. Following the map is a description of the bits for each map entry

MAP OF M8200-YC STATUS

PC	CSR	STAT1	STAT2	STAT3
--	--	---	---	---
001500	160010	145310	177777	000000

Each map entry contains 4 words which contain the status information for 1 M8200-YC. The PC shows where in core memory the first of the 4 words is. In the example above the first m8200-yc's status is in locations, 1500, 1502, 1504, and 1506. The second m8200-yc status is located at 1510, 1512, 1514, and 1516. The information contained in each 4 word entry is defined as follows:

CSR: Contains M8200-YC CSR address

STAT1: BITS 00-08 IS M8200-YC VECTOR ADDRESS
BIT15=1 MICRO-PROCESSOR HAS CRAM
BIT15=0 MICRO-PROCESSOR HAS CROM
BIT14=1 TURNAROUND CONNECTOR IS ON
BIT14=0 NO TURNAROUND CONNECTOR
BITS 09-11 IS M8200-YC BR PRIORITY LEVEL

STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)
HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)

stat3: bit0=1 perform free running tests on kmc
m8200-yc/lpa micro code version 3

8.5 METHOD OF AUTO SIZING

8.5.1 FINDING THE CONTROL STATUS REGISTER.

The auto-sizing routine finds a m8200-yc as follows: It starts at address 170440 and tests all address in increments of 10 up to and including address 170500. If the address does not time out, the following is done, the first CROM address is written to a 125252 then it is read back. If it contains a -1 or 125252 or 456 or 16520 a m8200-yc or KMC11 has been found, if not, the address is updated by 10 and the search continues. a 125252 indicates a KMC11 with CRAM. a 456 indicates a M8200-YC. THIS IS WHY THE STATUS TABLE MUST BE VERIFIED BY THE USER AND IF ANY OF THE INFORMATION DOES NOT AGREE WITH THE HARDWARE THE DIAGNOSTIC MUST BE RESTARTED AND THE QUESTIONS MUST BE ANSWERED. All m8200-yc's in the system will be found by the auto-sizer. If it does not find a m8200-yc the diagnostic must be restarted and the questions answered.

8.5.2 FINDING THE VECTOR AND BR LEVEL

The vector area (address 300-776) is filled with the instruction IOT and '.+2' (next address). The processor status is started at 7 and the DMC is programmed to interrupt. The PS is lowered by 1 until the DMC interrupts; a delay is made and if no interrupt occurs at PS level 3 (because of a bad m8200-yc) the program assumes vector address 300 at BR level 5 and the problem should be fixed in the diagnostic. Once the problem is fixed; the program should be re-setup again to get correct vector. If an interrupt occurred; the address to which the m8200-yc interrupted to is picked up and reported as the vector. NOTE! if the vector reported is not the vector set up by you; there is a problem and AUTO SIZING should not be done.

8.6 SOFTWARE SWITCH REGISTER

If the diagnostic is run on an 11/04 or other CPU without a switch register then a software switch register is used to allow user the same switch options as described previously. If the hardware switch register does not exist or if one does and it contains all ones (177777) this software switch register is used.

Control:

To obtain control at any allowable time during execution of the diagnostic the operator types a CTRL G on the console terminal keyboard. As soon as the CTRL G is recognized, by the diagnostic, the following message will be displayed:

SWR=XXXXXX NEW?

Where XXXXXX is the current contents of the software switch register in octal. The software control routine will then

await operator action. At which time the operator is required to type one or more of the legal characters: 1) 0 - 7, 2) line feed(<LF>), 3) carriage return(<CR>), or 4) control-U (CTRL U). No check is made for legality. If the input character is not a <LF>, <CR>, or CTRL U it is assumed to be an octal digit.

To change the contents of the SSR the operator simply types the new desired value in octal - leading zeros need not be typed. And terminates the input string with a <CR> or <LF> depending on the program action desired as described below. The input value will be truncated to the last 6 digits typed. At least one digit must be typed on any given input string prior to the terminator before a change to the SSR will occur.

When the input string is terminated with a <CR> the diagnostic will continue execution from the point at which it was interrupted. If a <CR> is the only thing typed the program will continue without changing the SSR. The <LF> differs from the <CR> by restarting the program as if it were restarted at address 200.

If a CTRL U is typed at any point in the input string prior to the terminator the input value will be disregarded and the prompt displayed (SWR = XXXXXX NEW?).

To set the SSR for the starting switches, first load the diagnostic, then hit CTRL G, then start the diagnostic.

8.7 lpa-11 (system) diagnostic summary

diagnostics for the lpa-11 are written at three levels: (1) total pdp-11 system, (2) lpa-11 system; and, (3) lpa-11 options.

level 1 is designed to isolate a failure to the lpa-11 system. all options on the pdp-11 are exercised.

level 2 diagnostics isolate a failure to the individual option within the lpa-11. the level 2 diagnostic is md-11-drlpa. when the user runs drlpa he can generally tell which option diagnostic (level 3) to run next. m8254 and m8200-yc errors may "look" alike and drlpa may not be able to distinguish between them. arbitration errors will not be detected by this diagnostic.

level three diagnostics aid in determining if the error was in fact on the option the drlpa specified. the user may "loop" on the error. within level three, there are two groups of diagnostics. the first group requires no "extra" work by the user in order to run. group "a" diagnostics do not check arbitration, and require extra time for execution. the second group (group "b") requires that the user reconfigure the pdp-11 system. this reconfiguration involves cabling the unibus to the

ipa's i/o bus.

the diagnostic for the m8254 falls into the group "b" category.

the lpa-11zz diagnostic kit will include:

<u>option</u>	<u>group</u>	<u>diag. #</u>	<u>diag. title</u>
lpa-11zz	level 2	md-11-dr1pa	lpa-11 system diag.
m8254	"b"	md-11-drm8a	m8254 (jpbm) diag.
salik	a	md-11-dr1pb	salik diag.
	b	md-11-dzaac	salik diag.
arilk	a	md-11-dr1pc	lpa/arilk diag. #1
	a	md-11-dr1pd	lpa/arilk diag. #2
	a	md-11-dr1pe	lpa/arilk diag. #3
	b	md-11-dzara	arilk diag. #1
	b	md-11-dzarb	arilk diag. #2
	b	md-11-dzarc	arilk diag. #3
drilk	a	md-11-dr1pf	lpa/drilk diag.
	b	md-11-dzdrg	drilk diag.
kwilk	a	md-11-dr1pg	lpa/kwilk diag.
	b	md-11-dzkwk	kwilk diag.
lps-11	a	md-11-dr1ph	lpa/lps-11 diag. #1
	a	md-11-dr1pi	lpa/lps-11 diag. #2
	a	md-11-dr1pj	lpa/lps-11 diag. #3
	b	md-11-dz1pc	lps-11 diag. #1
	b	md-11-dz1pd	lps-11 diag. #2
	b	md-11-dz1pi	lps-11 diag. #3
adilk	a	md-11-dr1pk	lpa/adilk diag.
	b	md-11-dzadl	adilk diag.
m8200-yc	b	md-11-dz1pl	lpa/m8200-yc basic micro-cpu r/w test
	<u>jmp+rom</u>	md-11-dz1pm	lpa/m8200-yc

D02
Page 16

SEQ 0016

read test

1
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```
;*MAINDEC-11-DRLPM-A LPA-M8200-YC CROM AND JUMP TESTS
;*COPYRIGHT 1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
;-----
;STARTING PROCEDURE
;LOAD PROGRAM
;LOAD ADDRESS 000200
;SWR=0 AUTOSIZE M8200-YC
;SW07=1 USE CURRENT M8200-YC PARAMETERS
;SW00=1 INPUT NEW M8200-YC PARAMETERS
;PRESS START
;PROGRAM WILL TYPE "MAINDEC-11-DRLPM-A LPA-M8200-YC CROM AND JUMP TESTS"
;PROGRAM WILL TYPE STATUS MAP
;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
;AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
;AND THEN RESUME TESTING
;SUBSEQUENT RESTARTS WILL NOT TYPE PROGRAM TITLE

;SWITCH REGISTER OPTIONS
;-----
100000 SW15=100000 :=1, HALT ON ERROR
040000 SW14=40000 :=1, LOOP ON CURRENT TEST
020000 SW13=20000 :=1, INHIBIT ERROR TYPEOUT
010000 SW12=10000 :=1, DELETE TYPEOUT/BELL ON ERROR.
004000 SW11=4000 :=1, INHIBIT ITERATIONS
002000 SW10=2000 :=1, ESCAPE TO nEXT TEST ON ERROR
001000 SW09=1000 :=1, LOOP WITH CURRENT DATA
000400 SW08=400 :=1, LOOP ON ERROR
000200 SW07=200 :=1, USE CURRENT M8200-YC PARAMETERS, =0, AUTOSIZE M8200-YC
000100 SW06=100 :=1, HALT BEFORE CLOCKING MICRO-PROCESSOR INSTRUCTION
000040 SW05=40
000020 SW04=20
000010 SW03=10 :RESELECT M8200-YC'S TO BE TESTED (ACTIVE)
000004 SW02=4 :LOCK ON TEST SELECT
000002 SW01=2 :RESTART PROGRAM AT SELECTED TEST
000001 SW00=1 :INPUT M8200-YC PARAMETERS
```

46
47
48 ;REGISTER DEFINITIONS
49 ;-----
50
51 000000 R0=%0 :GENERAL REGISTER
52 000001 R1=%1 :GENERAL REGISTER
53 000002 R2=%2 :GENERAL REGISTER
54 000003 R3=%3 :GENERAL REGISTER
55 000004 R4=%4 :GENERAL REGISTER
56 000005 R5=%5 :GENERAL REGISTER
57 000006 SP=%6 :PROCESSOR STACK POINTER
58 000007 PC=%7 :PROGRAM COUNTER
59
60 ;LOCATION EQUIVALENCIES
61 ;-----
62
63 177776 PS=177776 :PROCESSOR STATUS WORD
64 001200 STACK=1200 :START OF PROCESSOR STACK
65
66 ;INSTRUCTION DEFINITIONS
67 ;-----
68
69 005746 PUSH1SP=5746 :DECREMENT PROCESSOR STACK 1 WORD
70 005726 POP1SP=5726 :INCREMENT PROCESSOR STACK 1 WORD
71 010046 PUSHRO=10046 :SAVE RO ON STACK
72 012600 POPRO=12600 :RESTORE RO FROM STACK
73 024646 PUSH2SP=24646 :DECREMENT STACK TWICE
74 022626 POP2SP=22626 :INCREMENT STACK TWICE
75 .EQUIV EMT,HLT :BASIC DEFINITION OF ERROR CALL
76
77 ;BIT DEFINITIONS
78 ;-----
79
80 100000 BIT15=100000
81 040000 BIT14=40000
82 020000 BIT13=20000
83 010000 BIT12=10000
84 004000 BIT11=4000
85 002000 BIT10=2000
86 001000 BIT9=1000
87 000400 BIT8=400
88 000200 BIT7=200
89 000100 BIT6=100
90 000040 BIT5=40
91 000020 BIT4=20
92 000010 BIT3=10
93 000004 BIT2=4
94 000002 BIT1=2
95 000001 BIT0=1
96
97

```

98
99 ; ****
100 ;
101 ;-----; TRAPCATCAER FOR ILLEGAL INTERRUPTS
102 ;-----; THE STANDARD "TRAP CATCHER" IS PLACED
103 ;-----; BETWEEN ADDRESS 0 TO ADDRESS 776.
104 ;-----; IT LOOKS LIKE "PC+2 HALT".
105 ;
106 ; ****
107 ;
108 000000
109 .=0
110 ;-----; STANDARD INTERRUPT VECTORS
111 ;
112 .=24
113 000024 005346 PFAIL ;POWER FAIL HANDLER
114 000026 000340 340 ;SERVICE AT LEVEL 7
115 000030 004760 HLT ;ERROR HANDLER
116 000032 000340 340 ;SERVICE AT LEVEL 7
117 000034 004726 TRPSRV ;GENERAL HANDLER DISPATCH SERVICE
118 000036 000340 340 ;SERVICE AT LEVEL 7
119 000040
120 000040 000000 0 ;SAVE FOR ACT-11 OR XXDP
121 000042 000000 0 ;RETURN ADDRESS IF UNDER ACT-11 OR XXDP
122 000044 000000 0 ;SAVE FOR ACT-11 OR XXDP
123 000046 003532 SENDAD ;FOR USE WITH ACT-11 OR XXDP
124 000052 000000 0 ;ACT-11 PROGRAM CHARACTERISTICS
125
126
127 .=174
128 000174 000000 DISPREG:0 ;SOFTWARE DISPLAY REGISTER
129 000176 000000 SWREG: 0 ;SOFTWARE SWITCH REGISTER
130
131 000200 000137 002002 .=200
132 000200 000137 002002 JMP .START ;GO TO START OF PROGRAM
133
134
135 .=1000
136 001000 005377 040515 047111 MTITLE: .ASCII <377><12>/MAINDEC-11-DRLPM-A/<377>
137 (2) 001025 114 040520 046455 .ASCIZ /LPA-M8200-YC CROM AND JUMP TESTS/<377>
138
139 001200 .=1200
140 ;-----; INDIRECT POINTERS TO SWITCH REGISTER AND LIGHT DISPLAY
141
142 001200 177570 DISPLAY:177570
143 001202 177570 SWR: 177570

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DRLPM MACY11 27(654) 13-DEC-77 15:46 PAGE 4
 DRLPM.P11 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

SEQ 0020

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144
145 ;INDIRECT POINTERS TO TELETYPE VECTORS AND REGISTERS
146 ;-----
147
148 001204 177560 TKCSR: 177560 ;TELETYPE KEYBOARD CONTROL REGISTER
149 001206 177562 TKDBR: 177562 ;TELETYPE KEYBOARD DATA BUFFER
150 001210 177564 TPCSR: 177564 ;TELEPRINTER CONTROL REGISTER
151 001212 177566 TPDBR: 177566 ;TELEPRINTER DATA BUFFER

152
153 ;PROGRAM CONTROL PARAMETERS
154 ;-----
155
156 001214 000000 RETURN: 0 ;SCOPE ADDRESS FOR LOOP ON TEST
157 001216 000000 NEXT: 0 ;ADDRESS OF NEXT TEST TO BE EXECUTED
158 001220 000000 LOCK: 0 ;ADDRESS FOR LOCK ON CURRENT DATA
159 001222 000003 ICOUNT: 3 ;NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE EXECUTED
160 001224 000000 LPCNT: 0 ;NUMBER OF ITERATIONS COMPLETED
161 001226 000000 TSTNO: 0 ;NUMBER OF TEST IN PROGRESS
162 001230 000000 PASCNT: 0 ;NUMBER OF PASSES COMPLETED
163 001232 000000 ERRCNT: 0 ;TOTAL NUMBER OF ERRORS
164 001234 000000 LSTERR: 0 ;PC OF LAST ERROR CALL

165
166 ;PROGRAM VARIABLES
167 ;-----
168
169 001236 000000 STRTSW: 0 ;SWITCHES AT START OF PROGRAM
170 001240 000000 STAT: 0 ;DM STATUS WORD STORAGE
171 001242 000000 CLKX: 0
172 001244 000000 MASKX: 0
173 001246 000000 TEMP1: 0 ;TEMPORARY STORAGE
174 001250 000000 TEMP2: 0 ;TEMPORARY STORAGE
175 001252 000000 TEMP3: 0 ;TEMPORARY STORAGE
176 001254 000000 TEMP4: 0 ;TEMPORARY STORAGE
177 001256 000000 TEMP5: 0 ;TEMPORARY STORAGE
178 001260 000000 SAVR0: 0 ;R0 STORAGE
179 001262 000000 SAVR1: 0 ;R1 STORAGE
180 001264 000000 SAVR2: 0 ;R2 STORAGE
181 001266 000000 SAVR3: 0 ;R3 STORAGE
182 001270 000000 SAVR4: 0 ;R4 STORAGE
183 001272 000000 SAVR5: 0 ;R5 STORAGE
184 001274 000000 SAVSP: 0 ;STACK POINTER STORAGE
185 001276 000000 SAVPC: 0 ;PROGRAM COUNTER STORAGE
186 001300 000000 ZERO: 0
187 001302 000001 ONE: 1
188 001304 000000 MEMLIM: 0 ;HIGHEST LOCATION FOR NPR'S
189 001306 000001 DMACTV: .BLKW 1 ;M8200-YC'S SELECTED ACTIVE.
190 001310 000001 DMNUM: .BLKW 1 ;OCTAL NUMBER OF M8200-YC'S.
191 001312 000001 SAVACT: .BLKW 1 ;ORIGINAL ACTV DEVICES
192 001314 000001 SAVNUM: .BLKW 1 ;WORKABLE NUMBER
193 001316 000000 RUN: 0 ;pointer to running device.
194 ;EVEN
195 001320 001472 CREAM: DM.MAP-6 ;TABLE POINTER.
196 001322 001676 MILK: CNT.MAP-4 ;TABLE POINTER.

```

```

197
198 ;PROGRAM CONTROL FLAGS
199 ;-----
200
201 001324    000      INIFLG: .BYTE  0      ;PROGRAM INITIALIZATION FLAG
202 001325    000      ERRFLG: .BYTE  0      ;ERROR OCCURED FLAG
203 001326    000      LOKFLG: .BYTE  0      ;LOCK ON CURRENT TEST FLAG
204 001327    000      QV.FLG: .BYTE  0      ;QUICK VERIFY FLAG.
205                                     ;ON FIRST PASS OF EACH M8200-YC ITERATIONS WILL BE SUPPR
206 .EVEN
207
208 ;DEFINITIONS FOR TRAP SUBROUTINE CALLS
209 ;POINTERS TO SUBROUTINES CAN BE FOUND
210 ;IN THE TABLE IMMEDIATELY FOLLOWING THE DEFINITIONS
211
212 ;:*****-
213
214 001330    104400   ;TRPTAB:
215 001330    003606   SCOPE=TRAP+0      ;CALL TO SCOPE LOOP AND ITERATION HANDLER
216 001330    104401   .SCOPE
217 001332    003746   SCOP1=TRAP+1      ;CALL TO LOOP ON CURRENT DATA HANDLER
218 001332    104402   .SCOP1
219 001334    003776   TYPE=TRAP+2      ;CALL TO TELETYPE OUTPUT ROUTINE
220 001334    104403   .TYPE
221 001336    004060   INSTR=TRAP+3      ;CALL TO ASCII STRING INPUT ROUTINE
222 001336    104404   .INSTR
223 001340    004164   INSTER=TRAP+4      ;CALL TO INPUT ERROR HANDLER
224 001340    104405   .INSTER
225 001342    004204   PARAM=TRAP+5      ;CALL TO NUMERICAL DATA INPUT ROUTINE
226 001342    104406   .PARAM
227 001344    004404   SAV05=TRAP+6      ;CALL TO REGISTER SAVE ROUTINE
228 001344    104407   .SAV05
229 001346    004444   RES05=TRAP+7      ;CALL TO REGISTER RESTORE ROUTINE
230 001346    104410   .RES05
231 001350    004476   CONVRT=TRAP+10     ;CALL TO DATA OUTPUT ROUTINE
232 001350    104411   .CONVRT
233 001352    004502   CNVRT=TRAP+11     ;CALL TO DATA OUTPUT ROUNTINE WITHOUT CR/LF.
234 001352    104412   .CNVRT
235 001354    005476   MSTCLR=TRAP+12     ;CALL TO ISUE A MASTER CLEAR
236 001354    104413   .MSTCLR
237 001356    005446   DELAY=TRAP+13     ;CALL TO DELAY
238 001356    104414   .DELAY
239 001360    005514   ROMCLK=TRAP+14     ;CALL TO CLOCK ROM ONCE
240 001360    104415   .ROMCLK
241 001362    005562   DATACLK=TRAP+15     ;CALL TO CLK DATA
242 001362    104416   .DATACLK
243 001364    005626   TIMER=TRAP+16     ;CALL TO dELAY A CLOCK TICK
244
245 ;:*****-
246
247

```

J02

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 DRLPM.P11 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

SEQ 0022

```

248 ;M8200-YC CONTROL INDICATORS FOR CURRENT M8200-YC UNDER TEST
249 ;
250 ;
251 001366 000000 STAT1: 0
252 001370 000000 STAT2: 0
253 001372 000000 STAT3: 0
254 ;
255 ;M8200-YC VECTOR AND REGISTER INDIRECT POINTERS
256 ;
257 ;
258 001374 000000 DMRVEC: 0 :POINTER TO M8200-YC RECEIVER INTERRUPT VECTOR
259 001376 000000 DMRLVL: 0 :POINTER TO M8200-YC RECEIVER INTERRUPT SERVICE PS
260 001400 000000 DMTVEC: 0 :POINTER TO M8200-YC TRANSMITTER INTERRUPT VECTOR
261 001402 000000 DMTLVL: 0 :POINTER TO M8200-YC TRANSMITTER INTERRUPT SERVICE PS
262 001404 000000 DMCSR: 0 :POINTER TO M8200-YC CONTROL STATUS REGISTER
263 001406 000000 DMCSRH: 0 :POINTER TO M8200-YC CONTROL STATUS REGISTER HIGH BYTE.
264 001410 000000 DMCTL: 0 :POINTER TO M8200-YC CONTROL OUT REGISTER
265 001412 000000 DMP04: 0 :POINTER TO M8200-YC PORT REGISTER(SEL 4)
266 001414 000000 DMP06: 0 :POINTER TO M8200-YC PORT REGISTER(SEL 6)
267 ;
268 ;TEMP STORAGE
269 ;
270 001416 000000 TEMP: 0
271 001460 .=.+40
272 ;
273 ;
274 ;M8200-YC STATUS TABLE AND ADDRESS ASSIGNMENTS
275 ;
276 ;
277 001500 .=1500
278 001500 000001 DMCR00: .BLKW 1 :CONTROL STATUS REGISTER FOR M8200-YC NUMBER 00
279 001502 000001 DMS100: .BLKW 1 :VECTOR FOR M8200-YC NUMBER 00
280 001504 000001 DMS200: .BLKW 1 :DDCMP LINE# FOR M8200-YC NUMBER 00
281 001506 000001 DMS300: .BLKW 1 :3RD STATUS WORD
282 ;
283 001510 000001 DMCR01: .BLKW 1 :CONTROL STATUS REGISTER FOR M8200-YC NUMBER 01
284 001512 000001 DMS101: .BLKW 1 :VECTOR FOR M8200-YC NUMBER 01
285 001514 000001 DMS201: .BLKW 1 :DDCMP LINE# FOR M8200-YC NUMBER 01
286 001516 000001 DMS301: .BLKW 1 :3RD STATUS WORD
287 ;
288 001520 000001 DMCR02: .BLKW 1 :CONTROL STATUS REGISTER FOR M8200-YC NUMBER 02
289 001522 000001 DMS102: .BLKW 1 :VECTOR FOR M8200-YC NUMBER 02
290 001524 000001 DMS202: .BLKW 1 :DDCMP LINE# FOR M8200-YC NUMBER 02
291 001526 000001 DMS302: .BLKW 1 :3RD STATUS WORD
292 ;
293 001530 000001 DMCR03: .BLKW 1 :CONTROL STATUS REGISTER FOR M8200-YC NUMBER 03
294 001532 000001 DMS103: .BLKW 1 :VECTOR FOR M8200-YC NUMBER 03
295 001534 000001 DMS203: .BLKW 1 :DDCMP LINE# FOR M8200-YC NUMBER 03
296 001536 000001 DMS303: .BLKW 1 :3RD STATUS WORD
297 ;
298 001540 000001 DMCR04: .BLKW 1 :CONTROL STATUS REGISTER FOR M8200-YC NUMBER 04
299 001542 000001 DMS104: .BLKW 1 :VECTOR FOR M8200-YC NUMBER 04
300 001544 000001 DMS204: .BLKW 1 :DDCMP LINE# FOR M8200-YC NUMBER 04
301 ;

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 DRLPM.P11 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

SEQ 0023

302	001546	000001	DMS304: .BLKW	1	; 3RD STATUS WORD
303			DMCr05: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 05
304	001550	000001	DMS105: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 05
305	001552	000001	DMS205: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 05
306	001554	000001	DMS305: .BLKW	1	; 3RD STATUS WORD
307	001556	000001			
308			DMCR06: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 06
309	001560	000001	DMS106: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 06
310	001562	000001	DMS206: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 06
311	001564	000001	DMS306: .BLKW	1	; 3RD STATUS WORD
312	001566	000001			
313			DMCR07: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 07
314	001570	000001	DMS107: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 07
315	001572	000001	DMS207: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 07
316	001574	000001	DMS307: .BLKW	1	; 3RD STATUS WORD
317	001576	000001			
318			DMCR10: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 10
319	001600	000001	DMS110: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 10
320	001602	000001	DMS210: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 10
321	001604	000001	DMS310: .BLKW	1	; 3RD STATUS WORD
322	001606	000001			
323			DMCR11: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 11
324	001610	000001	DMS111: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 11
325	001612	000001	DMS211: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 11
326	001614	000001	DMS311: .BLKW	1	; 3RD STATUS WORD
327	001616	000001			
328			DMCr12: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 12
329	001620	000001	DMS112: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 12
330	001622	000001	DMS212: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 12
331	001624	000001	DMS312: .BLKW	1	; 3RD STATUS WORD
332	001626	000001			
333			DMCR13: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 13
334	001630	000001	DMS113: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 13
335	001632	000001	DMS213: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 13
336	001634	000001	DMS313: .BLKW	1	; 3RD STATUS WORD
337	001636	000001			
338			DMCR14: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 14
339	001640	000001	DMS114: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 14
340	001642	000001	DMS214: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 14
341	001644	000001	DMS314: .BLKW	1	; 3RD STATUS WORD
342	001646	000001			
343			DMCR15: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 15
344	001650	000001	DMS115: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 15
345	001652	000001	DMS215: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 15
346	001654	000001	DMS315: .BLKW	1	; 3RD STATUS WORD
347	001656	000001			
348			DMCR16: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 16
349	001660	000001	DMS116: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 16
350	001662	000001	DMS216: .BLKW	1	; DDCMP LINE# FOR M8200-YC NUMBER 16
351	001664	000001	DMS316: .BLKW	1	; 3RD STATUS WORD
352	001666	000001			
353			DMCr17: .BLKW	1	; CONTROL STATUS REGISTER FOR M8200-YC NUMBER 17
354	001670	000001	DMS117: .BLKW	1	; VECTOR FOR M8200-YC NUMBER 17
355	001672	000001			

L02

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DRLPM.P11 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

SEQ 0024

356 001674 000001
357 001676 000001
358
359 001700 000000

DMS217: .BLKW 1
DMS317: .BLKW 1
DM.END: 000000

;DDCMP LINE# FOR M8200-YC NUMBER 17
;3RD STATUS WORD

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 DRLPM.P11 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

SEQ 0025

```

360
361 ;M8200-YC PASS COUNT AND ERROR COUNT TABLE
362 ;
363 ;
364 001702 000000 CNT_MAP:
365 001702 000000 PACT00: 0 ;PASS COUNT FOR M8200-YC NUMBER 00
366 001704 000000 ERCT00: 0 ;ERROR COUNT FOR M8200-YC NUMBER 00
367
368 001706 000000 PACT01: 0 ;PASS COUNT FOR M8200-YC NUMBER 01
369 001710 000000 ERCT01: 0 ;ERROR COUNT FOR M8200-YC NUMBER 01
370
371 001712 000000 PACT02: 0 ;PASS COUNT FOR M8200-YC NUMBER 02
372 001714 000000 ERCT02: 0 ;ERROR COUNT FOR M8200-YC NUMBER 02
373
374 001716 000000 PACT03: 0 ;PASS COUNT FOR M8200-YC NUMBER 03
375 001720 000000 ERCT03: 0 ;ERROR COUNT FOR M8200-YC NUMBER 03
376
377 001722 000000 PACT04: 0 ;PASS COUNT FOR M8200-YC NUMBER 04
378 001724 000000 ERCT04: 0 ;ERROR COUNT FOR M8200-YC NUMBER 04
379
380 001726 000000 PACT05: 0 ;PASS COUNT FOR M8200-YC NUMBER 05
381 001730 000000 ERCT05: 0 ;ERROR COUNT FOR M8200-YC NUMBER 05
382
383 001732 000000 PACT06: 0 ;PASS COUNT FOR M8200-YC NUMBER 06
384 001734 000000 ERCT06: 0 ;ERROR COUNT FOR M8200-YC NUMBER 06
385
386 001736 000000 PACT07: 0 ;PASS COUNT FOR M8200-YC NUMBER 07
387 001740 000000 ERCT07: 0 ;ERROR COUNT FOR M8200-YC NUMBER 07
388
389 001742 000000 PACT10: 0 ;PASS COUNT FOR M8200-YC NUMBER 10
390 001744 000000 ERCT10: 0 ;ERROR COUNT FOR M8200-YC NUMBER 10
391
392 001746 000000 PACT11: 0 ;PASS COUNT FOR M8200-YC NUMBER 11
393 001750 000000 ERCT11: 0 ;ERROR COUNT FOR M8200-YC NUMBER 11
394
395 001752 000000 PACT12: 0 ;PASS COUNT FOR M8200-YC NUMBER 12
396 001754 000000 ERCT12: 0 ;ERROR COUNT FOR M8200-YC NUMBER 12
397
398 001756 000000 PACT13: 0 ;PASS COUNT FOR M8200-YC NUMBER 13
399 001760 000000 ERCT13: 0 ;ERROR COUNT FOR M8200-YC NUMBER 13
400
401 001762 000000 PACT14: 0 ;PASS COUNT FOR M8200-YC NUMBER 14
402 001764 000000 ERCT14: 0 ;ERROR COUNT FOR M8200-YC NUMBER 14
403
404 001766 000000 PACT15: 0 ;PASS COUNT FOR M8200-YC NUMBER 15
405 001770 000000 ERCT15: 0 ;ERROR COUNT FOR M8200-YC NUMBER 15
406
407 001772 000000 PACT16: 0 ;PASS COUNT FOR M8200-YC NUMBER 16
408 001774 000000 ERCT16: 0 ;ERROR COUNT FOR M8200-YC NUMBER 16
409
410 001776 000000 PACT17: 0 ;PASS COUNT FOR M8200-YC NUMBER 17
411 002000 000000 ERCT17: 0 ;ERROR COUNT FOR M8200-YC NUMBER 17
412

```

413

FORMAT OF STATUS TABLE

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CSR	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
	I	C	O	N	T	R	O	L	I	R	E	G	I	S	T	E
	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
STAT1	I	*	I	*	I	*	I	*	I	*	V	I	E	C	I	I
	I	*	I	*	I	*	I	*	I	*	I	I	I	T	O	R
	I	*	B	M	I	A	I	D	I	*	I	L	I	I	N	I
	I	*	I	I	I	I	I	I	I	*	I	I	I	I	E	I
STAT2	I	I	I	I	I	I	I	I	I	I	I	I	I	#	I	*
	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I
STAT3	I	I	I	I	I	I	I	I	I	I	I	I	I	*	I	*
	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I

DEFINITION OF FORMAT

CSR: CONTAINS M8200-YC CSR ADDRESS

STAT1: BITS 00-08 IS M8200-YC VECTOR ADDRESS
 BIT15=1 MICRO-PROCESSOR HAS CRAM
 BIT15=0 MICRO-PROCESSOR HAS CROM
 BIT14=1 ??? TURNAROUND CONNECTOR IS ON
 BIT14=0 NO TURNAROUND CONNECTOR
 BIT13=0 LINE UNIT IS AN M8201
 BIT13=1 LINE UNIT IS AN M8202
 BIT12=1 NO LINE UNIT
 BITS 09-11 IS M8200-YC BR PRIORITY LEVEL

STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)
 HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)

STAT3: BIT0=1 DO FREE RUNNING TESTS ON KMC
 (MUST BE SET TO A ONE MANUALLY [PROGRAM DZDMI ONLY])
 KMC MUST HAVE MICRO-CODE WRITTEN FROM RUNNING
 DZDMG TEST 2 FIRST
 BIT1=1 M8200-YC-AL LOCAL HIGH SPEED MICRO-CODE
 BIT1=0 M8200-YC-AR REMOTE LOW SPEED MICRO-CODE

B03

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DRLPM.P11 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

SEQ 0027

468
 469
 470
 471
 472
 473
 474
 475
 476 002002 012737 000340 177776 .START: MOV #340,PS
 477 002010 012706 001200 MOV #STACK,SP
 478 002014 012737 005346 000024 MOV \$PFAIL,2#24
 479 002022 012737 001310 001314 MOV DMNUM,SAVNUM
 480 002030 005037 010056 CLR SWFLG
 481 002034 105037 001325 CLRB ERRFLG
 482 002040 105037 001327 CLRB QV.FLG
 483 002044 012737 001470 001320 MOV SDM.MAP-10,CREAM
 484 002052 012737 001676 001322 MOV SCNT.MAP-4,MILK
 485 002060 012737 100000 001316 MOV \$BIT15,RUN
 486 002066 012700 001702 CLR SCNT.MAP,RO
 487 002072 005020 (RO)+ CLR (RO)+
 488 002074 022700 002002 CMP SCNT.MAP+100,RO
 489 002100 001374 BNE 23S
 490 002102 005037 001234 CLR LSTERR
 491 002106 012737 000001 001226 MOV \$1,TSTNO
 492 002114 012737 002002 001214 MOV \$.START,RETURN
 493
 494 002122 013746 000006 MOV @#6,-(SP)
 495 002126 013746 000004 MOV @#4,-(SP)
 496 002132 012737 002166 000004 MOV @#6,\$@#4
 497 002140 012737 177570 001202 MOV @177570,SWR
 498 002146 012737 177570 001200 MOV @177570,DISPLAY
 499 002154 022777 177777 177020 CMP #-1,JSWR
 500 002162 001402 BEQ 65+2
 501 002164 000407 BR 75
 502 002166 022626 65: CMP (SP)+,(SP)+
 503 002170 012737 000176 001202 MOV #SWREG,SWR
 504 002176 012737 000174 001200 MOV #DISPREG,DISPLAY
 505 002204 012637 000004 75: MOV (SP)+,@#4
 506 002210 012637 000006 MOV (SP)+,@#6
 507 002214 105737 001324 TSTB INIFLG
 508 002220 001012 BNE 20S
 509 002222 022737 003532 000042 CMP #SENDAD,2#42
 510 002230 001406 BEQ 20S
 511 002232 104402 001000 TYPE ,MTITLE
 512 002236 104402 023251 TYPE ,ROM1
 513 002242 104402 022454 TYPE ,MESWCH
 514 002246 004737 007646 20\$: JSR PC,CKSWR
 515 002252 017737 176724 001236 MOV #SWR,STRTSW
 516 002260 005737 000042 TST @#42
 517 002264 001402 BEQ +6
 518 002266 005037 001236 CLR STRTSW
 519 002272 032737 000001 001236 BIT #SW00,STRTSW
 520 002300 001012 BNE 17S
 521 002302 105737 001236 TSTB STRTSW
 :PROGRAM INITIALIZATION
 :LOCK OUT INTERRUPTS
 :SET UP PROCESSOR STACK
 :SET UP POWER FAIL VECTOR
 :CLEAR PROGRAM CONTROL FLAGS AND COUNTS
 :TYPE TITLE MESSAGE
 :LOCK OUT INTERRUPTS
 :SET UP STACK
 :SET UP POWER FAIL VECTOR
 :SAVE NUMBER OF DEVICES IN SYSTEM.
 :CLEAR SOFT TIMEOUT FLAG
 :CLEAR ERROR FLAG
 :ZERO QUICK VERIFY FLAG
 :GET MAP POINTER.
 :GET PASS COUNT MAP POINTER
 :POINT POINTER TO FIRST DEVICE.
 :PASS COUNT POINTER TO RO
 :CLEAR TABLE
 :DONE YET?
 :KEEP GOING
 :CLEAR LAST ERROR POINTER
 :SET UP FOR TEST 1
 :SET UP FOR POWER FAIL BEFORE
 :TESTING STARTS
 :SAVE CURRENT VECTORS
 :SET UP FOR TIMEOUT
 :SET SWR TO HARD SWR ADDRESS
 :SET DISPLAY TO HARD SWR ADDRESS
 :REFERENCE HARDWARE SWITCH REGISTER
 :IF = -1 USE SOFT SWR ANYWAY
 :IF IT EXISTS AND NOT = -1 USE HARD SWR
 :ADJUST STACK
 :POINTER TO SOFT SWR
 :POINTER TO SOFT DISPLAY REG
 :RESTORE VECTORS
 :HAS INITIALIZATION BEEN PERFORMED
 :BR IF YES
 :IF ACT-11 AUTOMATIC MODE, DON'T TYPE ID
 :TYPE TITLE MESSAGE
 :TYPE VERSION MESSAGE
 :TYPE SWITCH ? MESSAGE
 :CHECK FOR SOFT SWR
 :STORE STARTING SWITCHES
 :IS IT RUNNING IN AUTO MODE?
 :BR IF NO
 :IF YES, CLEAR SWITCHES
 :IF SW00=1, QUESTIONS ARE ASKED.
 :BR IF SW00=1
 :BIT?=1??

522	002306	100007		BPL	17S	BR IF SW07=0
523	002310	005737	001306	TST	DMACTV	ARE ANY DEVICES SELECTED?
524	002314	001006		BNE	16S	BR IF YES
525	002316	104402	007175	TYPE,	NOACT	NO DEVICES SELECTED.
526	002322	000000		HALT		STOP THE SHOW
527	002324	000776		BR	-2	DISQUALIFY CONTINUE SWITCH
528	002326	004737	010552	17S:	1SB	GO DO THE AUTO SIZE
529	002332	105737	001324	TSTB	INIFLG	FIRST TIME?
530	002336	001410		BEQ	21S	BR IF YES
531	002340	105737	001236	TSTB	STRTSW	IF USING SAME PARAMETERS DONT TYPE MAP
532	002344	100431		BMI	1S	
533	002346	032737	000006	BIT	#BIT1!BIT2,STRTSW	IS TEST NO. OR LOCK SELECTED
534	002354	001403	001236	BEQ	24S	IF NO THEN TYPE STATUS
535	002356	000424		BR	1S	IF YES DO NOT TYPE STATUS
536	002360	005137	001324	21S:	COM	SET FLAG
537	002364	104402	006237	24S:	TYPE	TYPE HEADER
538	002370	012704	001500	MOV	XHEAD	SET POINTER
539	002374	010437	001246	5S:	MOV	SET ADDRESS
540	002400	012437	001250	MOV	#DM.MAP,R4	SET CSR
541	002404	001411		BEQ	1S	ALL DONE IF ZERO
542	002406	012437	001252	MOV	(R4)+,TEMP3	SET STAT1
543	002412	012437	001254	MOV	(R4)+,TEMP4	SET STAT2
544	002416	012437	001256	MOV	(R4)+,TEMPS	SET STAT3
545	002422	104410		CONVRT		TYPE OUT STATUS MAP
546	002424	007514		XSTATQ		
547	002426	000762		BR	5S	
548	002430	012700	001500	MOV	#DM.mAP,RO	; RO POINTS TO STATUS TABLE
549						
550						*****
551						#AUTO SIZE TEST
552						*THIS TEST VERIFYS THAT THE MB200-YCS AND/OR KMC11S ARE AT THE CORRECT FLOATING
553						*ADDRESSES FOR YOUR SYSTEM. IF THIS TEST FAILS IT IS NOT A HARDWARE ERROR.
554						*CHECK THE ADDRESSES OF ALL FLOATING DEVICES (DJ,DH,DQ,DU,DUP,LK,DMC,DZ,KMC).
555						*IF THERE ARE NO OTHER FLOATING DEVICES BEFORE THE MB200-YC, THE FIRST
556						*MB200-YC ADDRESS IS 760070, KMC11 IS 760110. NO DEVICE SHOULD EVER BE AT
557						*ADDRESS 760000. THIS TEST MAY REQUIRE 2 OR MORE ATTEMPTS TO GET THE
558						*RIGHT ADDRESSES. AFTER YOU HAVE CHANGED THE ADDRESS TO WHAT IT TOLD
559						*YOU THE FIRST TIME, IT MAY COME BACK AND TELL YOU A DIFFERENT ADDRESS
560						*THE NEXT TIME YOU RUN IT. PLEASE HAVE PATIENCE, THE FINAL ADDRESS
561						*WILL BE CORRECT (AS LONG AS ALL DEVICES IN FRONT OF THE DMC'S ARE
562						*CORRECT).
563						*****
564						
565	002434	013746	000004	MOV	a#4,-(SP)	SAVE LOC 4
566	002440	013746	000006	MOV	a#6,-(SP)	SAVE LOC 6
567	002444	005037	000006	CLR	a#6	CLEAR VEC+2
568	002450	005037	001252	CLR	TEMP3	CLEAR FLAG
569	002454	005005		CLR	R5	R5=0=DMC, R5=-1=KMC
570	002456	011037	001404	AUSTRT:	MOV (R0),DMCSR	GET NEXT DMC CSR
571	002462	001564		BEQ	AUDONE	BR IF DONE
572	002464	005705		TST	R5	DMC OR KMC?
573	002466	001005		BNE	1S	BR IF KMC
574	002470	032760	100000 000002	BIT	#BIT15,2(R0)	CHECK FOR DMC CSR
575	002476	001061		BNE	SKIP	SKIP IF NOT DMC

576	002500	000404				BR	2S		ITS A DMC SO CONTINUE
577	002502	032760	100000	000002	1S:	BIT	#BIT15,2(R0)		CHECK FOR KMC CSR
578	002510	001454				BEQ	SKIP		SKIP IF NOT KMC
579	002512	012737	002704	000004	2S:	MOV	#NODEV,2#4		SET UP FOR TIMEOUT
580	002520	005705				TST	R5		DMC OR KMC?
581	002522	001003				BNE	3S		BR IF KMC
582	002524	012703	000006			MOV	#6,R3		R3 IS COUNT OF DEVICES BEFORE DMC
583	002530	000402				BR	4S		GO ON
584	002532	012703	000010		3S:	MOV	#10,R3		R3 IS COUNT OF DEVICES BEFORE KMC
585	002536	012702	003020		4S:	MOV	#DEVTAB,R2		R2 IS DEVICE TABLE PONTER
586	002542	012701	160010			MOV	#160010,R1		START WITH ADDRESS 160010
587	002546	005711			FLOAT:	TST	(R1)		CHECK ADDRESS IN R1
588	002550	111204				MOVB	(R2),R4		IF NO TIMEOUT, GET NEXT ADDRESS
589	002552	060401				ADD	R4,R1		IN R1
590	002554	005201				INC	R1		
591	002556	040401				BIC	R4,R1		
592	002560	005703				TST	R3		ANY MORE DEVICES TO CHECK FOR?
593	002562	001371				BNE	FLOAT		BR IF YES
594	002564	012737	002710	000004		MOV	#ERR,2#4		OK ONLY DMC'S ARE LEFT, SET UP FOR TIMEOUT
595	002572	010137	003032		FY:	MOV	R1,XLOC		SAVE FIRST DMC/KMC ADDRESS
596	002576	005705				TST	R5		DMC OR KMC?
597	002600	001005				BNE	1S		BR IF KMC
598	002602	032760	100000	000002		BIT	#BIT15,2(R0)		CHECK FOR DMC CSR
599	002610	001014				BNE	SKIP		SKIP IF NOT DMC
600	002612	000404				BR	2S		ITS A DMC SO CONTINUE
601	002614	032760	100000	000002	1S:	BIT	#BIT15,2(R0)		CHECK FOR KMC CSR
602	002622	001407				BEQ	SKIP		SKIP IF NOT KMC
603	002624	005711			2S:	TST	(R1)		CHECK DMC ADDRESS
604	002626	020137	001404			CMP	R1,DMCSR		DOES IT MATCH
605	002632	001411				BEQ	OK		BR IF YES
606	002634	062701	000010			ADD	#10,R1		GET NEXT DMC ADDRESS
607	002640	000756				BR	FY		DO IT AGAIN
608	002642	062700	000010		SKIP:	ADD	#10,R0		SKIP TO NEXT CSR IN TABLE
609	002646	011037	001404			MOV	(R0),DMCSR		GET NEXT CSR
610	002652	001470				BEQ	AUDONE		BR IF DONE
611	002654	000750				BR	FY		ELSE CONTINUE
612	002656	062700	000010		OK:	ADD	#10,R0		SKIP TO NEXT DMC CSR
613	002662	062737	000010	003032		ADD	#10,XLOC		UPDATE EXPECTED DMC/KMC ADDRESS
614	002670	011037	001404			MOV	(R0),DMCSR		GET NEXT DMC/KMC CSR
615	002674	001457				BEQ	AUDONE		BR IF DONE
616	002676	013701	003032			MOV	XLOC,R1		GET EXPECTED DMC/KMC ADDRESS
617	002702	000735				BR	FY		CONTINUE
618	002704	122243			NODEV:	CMPB	(R2)+,-(R3)		ON TIMEOUT, INC R2, DEC R3
619	002706	000002				RTI			RETURN
620	002710	005737	001252		ERR:	TST	TEMP3		CHECK FLAG IF = 0 TYPE HEADER
621	002714	001014				BNE	1S		SKIP HEADER
622	002716	104402				TYPE			TYPEOUT HEADER MESSAGE
623	002720	007244				CONERR			CONFIGURATION ERROR!!!!
624	002722	012737	002710	001276		MOV	#ERR,SAVPC		SAVE PC FOR TYPEOUT
625	002730	104411				CNVRT			TYPE OUT ERROR PC
626	002732	003000				ERRPC			
627	002734	104402				TYPE			TYPE REST OF HEADER
628	002736	007323				CNERR			
629	002740	012737	177777	001252		MOV	#-1,TEMP3		SET FLAG SO IT ONLY GETS TYPED ONCE

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DRLPM.P11 PROGRAM INITIALIZATION AND START UP.

SEQ 0031

630 002746 010137 001262	1\$: MOV CONVRT	R1,SAVR1	;SAVE R1 FOR TYPEOUT
631 002752 104410	CONTAB		
632 002754 003006	TST	RS	;TYPE CSR VALUES
633 002756 005705	BNE	3S	;DMC OR KMC ?
634 002760 001003	TYPE		;BR IF KMC
635 002762 104402	DMCM		
636 002764 007344	BR	4S	;CONTINUE
637 002766 000402	TYPE		
638 002770 104402	KMCM		
639 002772 007361	CMP	(SP)+,(SP)+	;ADJUST STACK
640 002774 022626	BR	OK	;BR TO GET OUT
641 002776 000727	ERRPC:	1	
642 003000 000001	.BYTE	6,2	
643 003002 006	SAVPC		
644 003004 001276	CONTAB:	2	
645 003006 000002	.BYTE	6,4	
646 003010 006	XLOC		
647 003012 003032	.BYTE	6,2	
648 003014 006	DMCSR		
649 003016 001404	.BYTE	7	
650 003020 007	DEVTAB:	7	:DJ
651 003021 017	.BYTE	17	:DH
652 003022 007	.BYTE	7	:DQ
653 003023 007	.BYTE	7	:DU
654 003024 007	.BYTE	7	:DUP
655 003025 00?	.BYTE	7	:LK
656 003026 007	.BYTE	7	:DMC
657 003027 007	.BYTE	7	:DZ
658 003030 007	.BYTE	7	:KMC
659 003032 .EVEN			
660 003032 000000	XLOC:	0	
661 003034 005705	AUDONE:	TST	DMC?
662 003036 001005	BNE	RS	;BR IF KMC AND ALL DONE
663 003040 012705 177777	MOV	#-1,RS	SET RS TO -1 (KMC)
664 003044 012700 001500	MOV	#DM.MAP,RO	RESET RO TO START OF TABLE
665 003050 000602	BR	AUSTRT	GO DO KMC'S
666 003052 012637 000006	MOV	(SP)+,@#6	RESTORE LOC 6
667 003056 012637 000004	MOV	(SP)+,@#4	RESTORE LOC 4
668 003062 032737 000010 001236	BIT	#SW03,STRTSW	SELECT SPECIFIC DEVICES??
669 003070 001422	BEQ	3S	;BR IF NO.
670 003072 104402 006154	TYPE	MNEW	TYPE THE MESSAGE.
671 003076 005000	CLR	RO	ZERO DATA LIGHTS
672 003100 000000	HALT		WAIT FOR USER TO TELL WHAT DEVICES TO RUN
673 003102 027737 176074 001312	CMP	@SWR,SAVACT	IS THE NUMBER VALID?
674 003110 101404	BLOS	2S	;BR IF NUMBER IS OK.
675 003112 104402 006015	TYPE	,MERR3	TELL USER OF INVALID NUMBER.
676 003116 000000	HALT		STOP EVERY THING.
677 003120 000776	BR	-2	RESTART THE PROGRAM AGAIN.
678 003122 017737 176054 001306 2\$:	MOV	@SWR,DMACTV	GET NEW DEVICE PATTERN
679 003130 013700 001306	MOV	DMACTV,RO	SHOW THE USER WHAT HE SELECTED.
680 003134 000000	HALT		CONTINUE DYNAMIC SWITCHES.
681 003136 012700 000300	MOV	#300,RO	PREPARE TO CLEAR THE FLOATING
682 003142 012701 000302	MOV	#302,R1	VECTOR AREA. 300-776
683 003146 010120	MOV	R1,(RO)+	START PUTTING "PC+2 - HALT"

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DRLPM.P11 PROGRAM INITIALIZATION AND START UP.

SEQ 0032

684	003150	005021		CLR	(R1)+	IN VECTOR AREA.
685	003152	022021		CMP	(R0)+, (R1)+	POP POINTERS
686	003154	022700	001000	CMP	#1000, R0	ALL DONE??
687	003160	001372		BNE	45	BR IF NO.
688						
689						; TEST START AND RESTART
690						;
691						
692	003162	012706	001200	.BEGIN:	MOV #STACK SP	SET UP STACK
693	003166	013746	000006		MOV @#6,-(SP)	SAVE LOC 6
694	003172	013746	000004		MOV @#4,-(SP)	SAVE LOC 4
695	003176	005000			CLR R0	START AT 0
696	003200	012737	003244	000004	MOV #28, #4	SET UP FOR TIME OUT
697	003206	005037	000006		CLR (R0)+	TO AUTOSIZE MEMORY
698	003212	005720			CMP #157776, R0	CHECK ADDRESS IN R0
699	003214	022700	157776		BNE 6S	IS IT AT LEAST 28K
700	003220	001374			SUB #7776, R0	BR IF NO
701	003222	162700	007776		MOV R0 MEMLIM	SAVE 2K FOR MONITORS
702	003226	010037	001304		MOV (SP)+, @#4	STORE MEMORY LIMIT
703	003232	012637	000004		MOV (SP)+, @#6	RESTORE LOC 4
704	003236	012637	000006		BR 10S	RESTORE LOC 6
705	003242	000413			CMP (SP)+, (SP)+	CONTINUE
706	003244	022626			SUB #4, R0	ADJUST STACK
707	003246	162700	000004		SUB #7776, R0	GET LAST GOOD ADDRESS
708	003252	162700	007776		CMP #30000, R0	SAVE 2K FOR MONITORS
709	003256	022700	030000		BNE 7S	IS IT 8K?
710	003262	001361			MOV #37400, R0	BR IF NO
711	003264	012700	037400		BR 7S	IF 8K DON'T SAVE 2K
712	003270	000756			MOV #340, PS	LOCK OUT INTERRUPTS
713	003272	012737	000340	177776	BIT #BIT2, STRTSW	CHECK FOR LOCK ON TEST
714	003300	032737	000004	001236	BEQ 1S	BR IF NO LOCK DESIRED.
715	003306	001411			TYPE .MLOCK	TYPE LOCK SELECTED.
716	003310	104402	006053		MOV \$NOP, TTST	ADJUST SCOPE ROUTINE.
717	003314	012737	000240	003622	MOV \$NOP, TTST+2	SET UP TO LOCK
718	003322	012737	000240	003624	BR 3S	CONTINUE ALONG.
719	003330	000406			MOV BRW, TTST	PREPARE NORMAL SCOPE ROUTINE
720	003332	013737	003740	003622	MOV BRX, TTST+2	LOCK NOT SELECTED, SET UP FOR NORMAL SCOPE LOOP
721	003340	013737	003742	003624	MOV #CYCLE, RETURN	START AT "CYCLE" FIND WHICH DEVICE TO TEST
722	003346	012737	010120	001214	BIT #SW01, STRTSW	IS TEST NO. SELECTED?
723	003354	032737	000002	001236	BNE 5S	BR IF YES
724	003362	001002			MR	TYPE R
725	003364	104402	005765		JMP @RETURN	START TESTING
726	003370	000177	175620			

727
 728
 729
 730
 731
 732
 733 003374 000005 .EOP: RESET ;END OF PASS
 734 003376 005037 001234 175560 LSTERR ;TYPE NAME OF TEST
 735 003402 105037 001325 CLRBL FRFLG ;UPDATE PASS COUNT
 736 003406 005237 001230 INC PASCNT ;CHECK FOR EXIT TO ACT-11
 737 003412 013777 001230 MOV PASCNT, ADISPLAY ;RESTART TEST
 738 003420 104402 005743 TYPE ,MEPASS
 739 003424 104402 006102 TYPE ,MCSSRX
 740 003430 104411 003556 CNVRT ,XCSR
 741 003434 104402 006110 TYPE ,MVECX
 742 003440 104411 003564 CNVRT ,XVEC
 743 003444 104402 006116 TYPE ,MPASSX
 744 003450 104411 003572 CNVRT ,XPASS
 745 003454 104402 006127 TYPE ,MERRX
 746 003460 104411 003600 CNVRT ,XERR
 747 003464 013700 001322 MOV MILK, R0 ;MAKE THE WORLD CLEAN AGAIN.
 748 003470 013720 001230 MOV PASCNT, (R0)+ ;CLEAR LAST ERROR PC
 749 003474 013720 001232 MOV ERRCNT, (R0)+ ;CLEAR ERROR FLAG
 750 003500 005337 001314 DEC SAVNUM ;UPDATE PASS COUNT
 751 003504 001017 BNE RESTRT ;DISPLAY PASS COUNT
 752 003506 112737 000377 001327 MOVB #377 QV. FLG ;TYPE END PASS
 753 003514 013737 001310 001314 MOV DMN, M SAVNUM ;TYPE CSR
 754 003522 013701 000042 MOV #442 R1 ;SHOW IT
 755 003526 001406 BEQ RESTRT ;TYPE VECTOR
 756 003530 000005 RESET ;SHOW IT
 757 003532 SENDAD: JSR PC, (R1) ;TYPE PASSES
 758 003532 004711 NOP ;SHOW ERRORS
 759 003534 000240 NOP ;SHOW IT
 760 003536 000240 NOP ;ARE ALL DEVICES TESTED?
 761 003540 000240 NOP ;BR IF NO
 762 003542 000240 NOP ;SET THE QUICK VERIFY FLAG.
 763 003544 012737 010120 001214 RESTRT: MOV #CYCLE, RETURN
 764 003552 000137 010120 JMP CYCLE ;RESTORE THE COUNT
 765 003556 000001 XCSR: 1 ;CHECK FOR ACT-11 OR DDP
 766 003560 006 002 BYTE 6,2 ;IF NOT, CONTINUE TESTING
 767 003562 001404 DMCSSR ;STOP THE SHOW--CLEAR THE WORLD
 768 003564 000001 XVEC: 1
 769 003566 004 002 BYTE 4,2
 770 003570 001374 DMRVEC
 771 003572 000001 XPASS: 1
 772 003574 006 002 BYTE 6,2
 773 003576 001230 PASCNT
 774 003600 000001 XERR: 1
 775 003602 006 002 BYTE 6,2
 776 003604 001232 ERRCNT ;SCOPE LOOP AND INTERATION HANDLER
 777
 778
 779
 780

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0034

781	003606	004737	007646	.SCOPE:	JSR	PC, CKSWR	CHECK FOR SOFT SWR
782	003612	010016			MOV	R0, (SP)	SAVE R0 ON THE STACK
783	003614	032777	040000 175360	TTST:	BIT	#BIT14, @SWR	"LOOP ON THIS TEST"?
784	003622	001407			BEQ	1S	BR IF NO. (IF LOCK SW01=1; THIS LOC =240)
785	003624	000437			BR	3S	GOTO 3S (IF LOCK SW01=1; THIS LOC =240)
786	003626	005737	003744		TST	DONE	WAS TKCSR DONE SET?
787	003632	001434			BEQ	3S	BR IF NO (LOCKED ON TEST)
788	003634	005037	003744		CLR	DONE	YES, CLEAR FLAG
789	003640	000415			BR	2S	GO TO NEXT TEST
790	003642	032777	004000 175332	1S:	BIT	#SW11, @SWR	DELETE ITERATION? (QUICK PASS)
791	003650	001011			BNE	2S	BR IF YES
792	003652	105737	001327		TSTB	QV.FLG	HAVE PASSES BEENCOMPLETED?
793	003656	001406			BEQ	2S	BR IF QUICK PASS.
794	003660	005237	001224		INC	LPCNT	UPDATE ITERATION COUNTER
795	003664	023737	001224	001222	CMP	LPCNT, ICOUNT	ARE ALL ITERATIONS DONE??
796	003672	101414			BLOS	3S	BR IF NOT YET
797	003674	105037	001325	2S:	CLR8	ERRFLG	PREPARE FOR NEW TEST
798	003700	005037	001224		CLR	LPCNT	START ICOUNTER AT 0
799	003704	005037	001220		CLR	LOCK	
800	003710	012737	000020	001222	MOV	#20, ICOUNT	RESET ITERATIONS
801	003716	013737	001216	001214	MOV	NEXT, RETURN	GET NEXT TEST
802	003724	011600		3S:	MOV	(SP), R0	POP R0 OFF OF THE STACK
803	003726	022626			POP2SP		FAKE AN "RTI"
804	003730	013701	001404		MOV	DMCSR, R1	R1 CONTAINS BASE M8200-YC ADDRESS
805	003734	000177	175254		JMP	@RETURN	GO DO THE TEST
806	003740	001407			BRW:	1407	
807	003742	000437			BRX:	437	
808	003744	000000			DONE:	0	
809							; CHECK FOR FREEZE ON CURRENT DATA
810							-----
811							
812							
813	003746	004737	007646	.SCOP1:	JSR	PC, CKSWR	CHECK FOR SOFT SWR
814	003752	032777	001000 175222		BIT	#SW09, @SWR	IS SW09=1(SET)?
815	003760	001405			BEQ	1S	BR IF NOT SET.
816	003762	005737	001220		TST	LOCK	
817	003766	001402			BEQ	1S	
818	003770	013716	001220	1S:	MOV	LOCK, (SP)	GOTO THE ADDRESS IN LOCK.
819	003774	000002			RTI		GO BACK.
820							
821							; TELETYPE OUTPUT ROUTINE
822							-----
823							
824	003776	010546		.TYPE:	MOV	R5, -(SP)	SAVE RS ON THE STACK.
825	004000	017605	000002		MOV	@2, (SP), RS	GET ADDRESS OF MESSAGE.
826	004004	062766	000002	4S:	ADD	#2, 2, (SP)	POP OVER ADDRESS.
827	004012	005737	010056		TST	SWFLG	SOFT SWR MESSAGE?
828	004016	001004			BNE	1S	IF YES TYPE IT OUT REGARDLESS OF SW12
829	004020	032777	010000 175154		BIT	#SW12, @SWR	INHIBIT ALL PRINT OUT??
830	004026	001012			BNE	3S	BR IF NO PRINT OUT WANTED (SW12=1)
831	004030	105715		1S:	TSTB	(RS)	IS NUMBER MINUS? (MSB=1(BIT7))
832	004032	100002			BPL	2S	BR IF NUMBER IS PLUS
833	004034	104402	005702		TYPE	MCRLF	TYPE A CR/LF!
834	004040	105777	175144	2S:	TSTB	@TPCSR	TTY READY?

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0035

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835 004044 100375          BPL   2$      ;BR IF NO.
836 004046 112577          MOVB  (R5)+, @TPDBR ;PRINT CURRENT CHAR.
837 004052 001357          BNE   4$      ;IF NOT ZERO KEEP PRINTING!
838 004054 012605          MOV   (SP)+, R5   ;END OF OUTPUT. RESTORE RS
839 004056 000002          RTI    ;GO HOME
840
841
842 004060 010346          .INSTR: MOV   R3, -(SP) ;SAVE R3 ON STACK
843 004062 010446          MOV   R4, -(SP) ;SAVE R4 ON STACK
844 004064 017637          000004 004102
845 004072 062766          000002 000004
846 004100 104402          .INST1: TYPE
847 004102 000000          .MSG:   C
848 004104 012704          MOV   #INBUF, R4
849 004110 012703          MOV   #7, R3
850 004114 105777          175064          1$:   TSTB  @TKCSR
851 004120 100375          BPL   1$      ;-----[REMOVED]
852 004122 117714          175060          MOV   @TKDBR, (R4)
853 004126 142714          000200          BICB  #200, (R4)
854 004132 122427          000015          CMPB  (R4)+, #15
855 004136 001417          BEQ   INSTR2
856 004140 105777          175044          2$:   TSTB  @TPCSR
857 004144 100375          BPL   2$      ;-----[REMOVED]
858 004146 017777          175034 175036          MOV   @TKDBR, @TPDBR
859 004154 005303
860 004156 001356
861 004160 012604
862 004162 012603
863 004164 104402          005676          .INSTE: TYPE
864 004170 010346          MOV   MQM
865 004172 010446          MOV   R3, -(SP)
866 004174 000741          MOV   R4, -(SP)
867 004176 012604          BR   .INST1
868 004200 012603          INSTR2: MOV   (SP)+, R4 ;RESTORE R4
869 004202 000002          MOV   (SP)+, R3 ;RESTORE R3
RTI
870
871 ;CONVERT ASCII STRING TO OCTAL
872 ;-----[REMOVED]
873
874 004204 010546          .PARAM: MOV   R5, -(SP)
875 004206 010446          MOV   R4, -(SP)
876 004210 016605          000004          MOV   4(SP), R5
877 004214 012537          004374          MOV   (R5)+, LOLIM
878 004220 012537          004376          MOV   (R5)+, HILIM
879 004224 012537          004400          MOV   (R5)+, DEVADR
880 004230 112537          004402          MOV   (R5)+, LOBITS
881 004234 112537          004403          MOV   (R5)+, ADRCNT
882 004240 010566          000004          MOV   R5, 4(SP)
883 004244 005005
884 004246 012704          007542          PARAM1: CLR   R5
885 004252 122714          000015          MOV   #INBUF, R4
886 004256 001420
887 004260 121427          000060          CMPB  #15, (R4)
888 004264 002415          BLT   PARERR
                                     1$:   BEQ   PARERR
                                     CMPB  (R4), #60
                                     RTI   PARERR
  
```

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0036

```

889 004266 121427 000067      CMPB   (R4), #67
890 004272 003012      BGT    PARERR
891 004274 142714 000060      BICB   #60, (R4)
892 004300 152405      BISB   (R4)+ R5
893 004302 122714 000015      CMPB   #15, (R4)
894 004306 001406      BEQ    LIMITS
895 004310 006305
896 004312 006305
897 004314 006305
898 004316 000760
899 004320 104404
900 004322 000750      PARERR: INSTER
                           BR     PARAM1

901
902 ; TEST TO SEE IF NUMBER IS WITHIN LIMITS
903 ;-----
904
905 004324 020537 004376      LIMITS: CMP    R5, HILIM
906 004330 101373      BHI    PARERR
907 004332 020537 004374      CMP    RS, LOLIM
908 004336 103770      BLO    PARERR
909 004340 133705 004402      BITB   LOBITS, R5
910 004344 001365      BNE    PARERR

911
912 ; STORE NUMBER AT SPECIFIED ADDRESS
913
914 004346 013704 004400      1$:   MOV    DEVADR, R4
915 004352 010524      MOV    R5, (R4)+
916 004354 062705 000002      ADD    #2, R5
917 004360 105337 004403      DECB   ADRCNT
918 004364 001372      BNE    1$           ; SP = R4 + 2
919 004366 012604      MOV    (SP)+, R4
920 004370 012605      MOV    (SP)+, R5
921 004372 000002      RTI
922 004374 000000      LOLIM: 0
923 004376 000000      HILIM: 0
924 004400 000000      DEVADR: 0
925 004402 000000      LOBITS: 0
926 004403            ADRCNT=LOBITS+1

927
928 ; SAVE PC OF TEST THAT FAILED AND R0-R5
929 ;-----
930
931 004404 016637 000004 001276 .SAV05: MOV    4(SP), SAVPC ; SAVE R7 (PC)
932
933 ; SAVE R0-R5
934
935 004412 010537 001272      SV05:  MOV    R5, SAVRS ; SAVE R5
936 004416 010437 001270      MOV    R4, SAVR4 ; SAVE R4
937 004422 010337 001266      MOV    R3, SAVR3 ; SAVE R3
938 004426 010237 001264      MOV    R2, SAVR2 ; SAVE R2
939 004432 010137 001262      MOV    R1, SAVR1 ; SAVE R1
940 004436 010037 001260      MOV    R0, SAVR0 ; SAVE R0
941 004442 000002            RTI    LEAVE.
942

```

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0037

```

943 ;RESTORE R0-R5
944
945 004444 013700 001260 .RES05: MOV SAVR0,R0 ;RESTORE R0
946 004450 013701 001262 MOV SAVR1,R1 ;RESTORE R1
947 004454 013702 001264 MOV SAVR2,R2 ;RESTORE R2
948 004460 013703 001266 MOV SAVR3,R3 ;RESTORE R3
949 004464 013704 001270 MOV SAVR4,R4 ;RESTORE R4
950 004470 013705 001272 MOV SAVR5,R5 ;RESTORE R5
951 004474 000002 RTI ,LEAVE

952 ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
953 ;-----
954
955
956 004476 104402 005702 .CONVR: TYPE MCRLF
957 004502 010046 .CNVRT: MOV R0,-(SP)
958 004504 010146 MOV R1,-(SP)
959 004506 010346 MOV R3,-(SP)
960 004510 010446 MOV R4,-(SP)
961 004512 010546 MOV R5,-(SP)
962 004514 017601 MOV @12(SP),R1
963 004520 062766 000012 ADD #2,12(SP)
964 004526 012137 004720 MOV (R1)+,WRDCNT
965 004532 112137 004722 1S: MOVB (R1)+,CHRCNT
966 004536 112137 004723 MOVB (R1)+,SPACNT
967 004542 013137 004724 MOV @1(R1)+,BINWRD
968 004546 122737 000003 004722 CMPB #3,CHRCNT
969 004554 001003 BNE 2S
970 004556 042737 177400 004724 BIC #177400,BINWRD
971 004564 013704 004724 2S: MOV BINWRD,R4
972 004570 113705 004722 MOVB CHRCNT,R5
973 004574 012700 001416 MOV #TEMP,R0
974 004600 010403 004722 3S: MOV R4,R3
975 004602 042703 177770 BIC #177770,R3
976 004606 062703 000060 ADD #060,R3
977 004612 110320 MOVB R3,(R0)+,CLC
978 004614 000241 ROR R4
979 004616 006004 CLC
980 004620 000241 ROR R4
981 004622 006004 CLC
982 004624 000241 ROR R4
983 004626 006004 CLC
984 004630 005305 ROR R4
985 004632 001362 DEC R5
986 004634 012703 007604 BNE 3S
987 004640 114023 004722 4S: MOVB #MDATA,R3
988 004642 105337 004722 DECB -(R0),(R3)+,CHRCNT
989 004646 001374 BNE 4S
990 004650 105737 004723 TSTB SPACNT
991 004654 001405 BEQ 6S
992 004656 112723 000040 MOVB #040,(R3)+,SPACNT
993 004662 105337 004723 DECB SPACNT
994 004666 001373 BNE 5S
995 004670 105013 CLR8 (R3)
996 004672 104402 007604 TYPE ,MDATA

```

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0038

997	004676	005337	004720		DEC	WRDCNT		
998	004702	001313			BNE	1\$		
999	004704	012605			MOV	(SP)+, R5		
1000	004706	012604			MOV	(SP)+, R4		
1001	004710	012603			MOV	(SP)+, R3		
1002	004712	012601			MOV	(SP)+, R1		
1003	004714	012600			MOV	(SP)+, R0		
1004	004716	000002			RTI			
1005	004720	000000			WRDCNT:	0		
1006	004722	000000			CHRCNT:	0		
1007	004723				SPACNT=	CHRCNT+1		
1008	004724	000000			BINWRD:	0		
1009								
1010								
1011								
1012								
1013								
1014								
1015								
1016	004726	011646			.TRPSR:	MOV	(SP)-(SP)	GET PC OF RETURN
1017	004730	162716	000002			SUB	#2,(SP)	=PC OF TRAP
1018	004734	017616	000000			MOV	0(SP),(SP)	GET TRP
1019	004740	006316				ASL	(SP)	MULTIPLY TRAP ARG BY 2
1020	004742	042716	177001			BIC	#177001,(SP)	CLEAR UNWANTED BITS
1021	004746	062716	001330			ADD	#.TRPTAB,(SP)	POINTER TO SUBROUTINE ADDRESS
1022	004752	017616	000000			MOV	0(SP),(SP)	SUBROUTINE ADDRESS
1023	004756	000136				JMP	0(SP)+	;GO TO SUBROUTINE
1024								
1025								
1026								
1027								
1028	004760	004737	007646		.HLT:	JSR	PC, CKSWR	CHECK FOR SOFT SWR
1029	004764	032777	010000	174210		BIT	#SW12,0SWR	BELL ON ERROR?
1030	004772	001406				BEQ	XBX	BR IF NO BELL
1031	004774	105777	174210			TSTB	0TPCSR	TTY READY.
1032	005000	100003				BPL	XBX	DON'T WAIT IF TTY NOT READY.
1033	005002	112777	000207	174202		MOVB	#207,0TPDBR	PUSH A BELL AT THE TTY
1034	005010	032777	020000	174164	XBX:	BIT	#SW13,0SWR	DELETE ERROR PRINT OUT?
1035	005016	001105				BNE	HALTS	BR IF NO PRINT OUT WANTED.
1036	005020	021637	001234			CMP	(SP),LSTERR	WAS THIS ERROR FOUND LAST TIME?
1037	005024	001404				BEQ	1\$	BR IF YES
1038	005026	011637	001234			MOV	(SP), LSTERR	RECORD BEING HERE
1039	005032	105037	001325			CLRB	ERRFLG	PREPARE HEADER
1040	005036	104406				SAVOS		SAVE ALL PROC REGISTERS
1041	005040	011605				MOV	(SP), R5	GET THE PC OF ERROR
1042	005042	162705	000002			SUB	#2, R5	GET ADDRESS OF TRAP CALL
1043	005046	011504				MOV	(R5), R4	GET HLT INSTRUCTION
1044	005050	006304				ASL	R4	MULT BY TWO
1045	005052	061504				ADD	(R5), R4	DOUBLE IT
1046	005054	006304				ASL	R4	MULT AGAIN
1047	005056	042704	177001			BIC	#177001, R4	CLEAR JUNK
1048	005062	062704	023544			ADD	#.ERRTAB, R4	GET POINTER
1049	005066	012437	005202			MOV	(R4)+, ERRMSG	GET ERROR MESSAGE
1050	005072	012437	005214			MOV	(R4)+, DATAHD	GET DATA HEADER

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DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0039

1051	005076	011437	005226	MOV	(R4), DATABP	:GET DATA TABLE
1052	005102	105737	001325	TSTB	ERRFLG	:TYPE HEADREER
1053	005106	001403		BEQ	TYPMMSG	:BR IF YES
1054	005110	005737	005226	TST	DATABP	:DOES DATA TABLE EXIST?
1055	005114	001040		BNE	TYPDAT	:BR IF YES.
1056	005116	104402	005702	TYPMMSG:	TYPE ,MCRLF	
1057	005122	104402	005702	TYPE	,MCRLF	
1058	005126	005737	001220	TST	'LOCK	
1059	005132	001402		BEQ	1S	
1060	005134	104402	006152	TYPE	,MASTEK	
1061	005140	104402	006140	1S:	TYPE ,MTSTN	
1062	005144	104411	005340	CNVRT	,XTSTN	:SHOW IT
1063	005150	104402	006232	TYPE	,MERRPC	:TYPE PC.
1064	005154	104411	005332	CNVRT	,ERTABO	:SHOW IT
1065	005160	104402	005702	TYPE	,MCRLF	:GIVE A CR/LF
1066	005164	112737	177777	001325	MOV8	:NO MORE HEADER UNLESS NO DATA TABLE.
1067	005172	005737	005202	TST	&1, ERRFLG	:IS THERE AN ERROR MESSAGE?
1068	005176	001402		BEQ	ERRMSG	:BR IF NO.
1069	005200	104402		TYPE	WRKO.FM	:TYPE
1070	005202	000000		ERRMSG:	0	:ERROR MESSAGE
1071	005204			WRKO.FM:		
1072	005204	005737	005214	TST	DATAHD	:DATA HEADER?
1073	005210	001402		BEQ	TYPDAT	:BR IF NO
1074	005212	104402		TYPE		:TYPE
1075	005214	000000		DATAHD:	0	:DATA HEADER
1076	005216	005737	005226	TYPDAT:	TST	:DATA TABLE?
1077	005222	001402		BEQ	RESREG	:BR IF NO.
1078	005224	104410		CONVRT		:SHOW
1079	005226	000000		DATABP:	0	:DATA TABLE
1080	005230	104407		RESREG:	RESOS	:RESTORE PROC REGISTERS
1081	005232	022737	003532	000042	HALTS:	:IF ACT-11 AUTOMATIC MODE, HALT!!
1082	005240	001403		CMP	#SENDAD, *	
1083	005242	005777	173734	BEQ	1S	
1084	005246	100005		TST	&SWR	:HALT ON ERROR?
1085	005250	010046		BPL	EXITER	:BR IF NO HALT ON ERROR
1086	005252	016600	000002	1S:	PUSHRO	:SAVE RO
1087	005256	000000		MOV	2(SP), RO	:SHOW ERROR PC IN DATA LIGHTS
1088	005260	012600		HALT		:HALT
1089	005262	005237	001232	POPRO		:GET RO
1090	005266	032777	000400	173706	EXITER:	:UPDATE ERROR COUNT
1091	005274	001007		INC	ERRCNT	:GOTO TOP OF TEST?
1092	005276	032777	002000	BIT	#SW08, &SWR	:BR IF YES
1093	005304	001411	173676	BNE	1S	:GOTO NEXT TEST?
1094	005306	013737	001216	BIT	#SW10, &SWR	:BR IF NO
1095	005314	012706	001200	BEQ	2S	:SET FOR NEXT TEST
1096	005320	013701	001404	1S:	MOV	:RESET SP
1097	005324	000177	173664	MOV	#STACK, SP	:SET UP R1
1098	005330	000002		JMP	DMCSR, R1	:GOTO SPECIFIED TEST
1099	005332	000001		RTI	&RETURN	:RETURN
1100	005334	006	002	ERTABO:	1	
1101	005336	001276		.BYTE	6,2	
1102	005340	000001		SAVPC		
1103	005342	003	002	XTSTN:	1	
1104	005344	001226		.BYTE	3,2	
				TSTNO		

1105 ;ENTER HERE ON POWER FAILURE
 1106 ;-----
 1107
 1108
 1109 005346 012737 005360 000024 .PFAIL:
 1110 005346 012737 005360 000024 MOV #PESTART,24 ;SET UP FOR POWER UP TRAP
 1111 005354 000000 000000 HALT ;HALT ON POWER DOWN NORMAL
 1112 005356 000777 BR
 1113
 1114 ;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
 1115
 1116 005360 012737 005346 000024 RESTAR:
 1117 005360 012737 005346 000024 MOV #PFAIL,24 ;SET UP FOR POWER FAILURE
 1118 005366 012706 001200 MOV #STACK_SP ;RESET THE STACK POINTER
 1119 005372 013701 001404 MOV DMCSR,R1 ;RESTORE R1
 1120 005376 005037 001416 CLR TEMP ;READY FOR TIMER
 1121 005402 005237 001416 INC TEMP ;PLUS ONE TO THE TIMER!
 1122 005406 001375 BNE -4 ;BR IF MORE TO GO
 1123 005410 104402 005705 TYPE ,MPFAIL ;TYPE THE MESSAGE
 1124 005414 104411 005440 CNVRT PFTAB ;TELL WHAT TEST TO RETURN TO.
 1125 005420 105037 001325 CLR8 ERRFLG ;START CLEAN
 1126 005424 005037 001234 CLR LSTERR ;CLEAR MAINT BITS
 1127 005430 005011 MSTCLR ;START CLEAN UP OF DEVICE
 1128 005432 104412 173554 JMP JRETURN ;START DOING THAT TEST AGAIN.
 1129 005434 000177 173554 PFTAB:
 1130 005440 000001 173554 .BYTE 1
 1131 005442 003 002 TSTNO 3,2
 1132 005444 001226 TSTNO 1
 1133
 1134 005446 012777 000020 173736 .DELAY:
 1135 005446 012777 000020 173736 MOV #20,ADMP04 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 1136 005454 104414 121111 ROMCLK 121111 ;POKE CLOCK DELAY BIT
 1137 005456 121111 1S:
 1138 005460 104414 ROMCLK 121224 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 1139 005460 121224 1S: PORT4+IBUS#11
 1140 005462 121224 BIT #BIT4,ADMP04 ;IS CLOCK BIT SET?
 1141 005464 032777 000020 173720 BEQ 1S ;BR IF NO
 1142 005472 001772 RTI
 1143 005474 000002 MSTCLR:
 1144
 1145 005476 152777 000100 173702 BISB #BIT6,ADMCSRH ;SET MASTER CLEAR
 1146 005504 142777 000300 173674 BICB #BIT6!BIT7,ADMCSRH ;CLEAR MASTER CLEAR AND RUN
 1147 005512 000002 RTI ;RETURN
 1148
 1149
 1150 005514 152777 000002 173664 ROMCLK:
 1151 005514 152777 000002 173664 BISB #BIT1,ADMCSRH ;SET ROMI
 1152 005522 013677 173666 MOV a(SP)+,ADMP06 ;LOAD INSTRUCTION IN SEL6
 1153 005526 062746 000002 ADD #2,-(SP) ;ADJUST STACK
 1154 005532 032777 000100 173442 BIT #SW06,a:WR ;HALT IF SW06 =1
 1155 005540 001401 BEQ 1S ;BR IF SW06 =0
 1156 005542 000000 HALT ;HALT BEFORE CLOCKING INSTRUCTION
 1157 005544 152777 000003 173634 1S: BISB #BIT1!BIT0,ADMCSRH ;CLOCK INSTRUCTION
 1158 005552 142777 000007 173626 BICB #BIT2!BIT1!BIT0,ADMCSRH ;CLEAR ROM0, ROMI, STEP

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0041

1159	005560	000002	RTI	
1160				
1161	005562		.DATACLK:	
1162	005562	013637 001416	MOV #2,-(SP)	;PUT TICK COUNT IN TEMP
1163	005566	062746 000002	ADD #BIT4,ADMCSR	;ADJUST STACK
1164	005572	152777 000020	15: BISB ADMCSR	;SET STEP LU
1165	005600	173600 173576	CMP ADMCSR	;WASTE TIME
1166	005606	142777 000020	BICB #BIT4,ADMCSR	;CLEAR STEP LU
1167	005614	173572	DEC TEMP	;DEC TICK COUNT
1168	005620	001416	BNE 15	;BR IF NOT DONE
1169	005622	000002	RTI	;RETURN
1170	005624	000001	.BLKW 1	
1171				
1172	005626		.TIMER:	
1173	005626	013637 001416	MOV #2,(SP)+ TEMP	;MOVE COUNT TO TEMP
1174	005632	062746 000002	ADD #2,-(SP)	;ADJUST STACK
1175	005636		15: ROMCLK 021364	;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1176	005636	104414	BIT #2,ADMPO4	;PORT4+IBUS# REG11
1177	005640	021364	BEQ 15	;IS PGM CLOCK BIT CLEAR?
1178	005642	032777 000002	25: ROMCLK 021364	;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1179	005650	173542	BIT #2,ADMPO4	;PORT4+IBUS# REG11
1180	005652	001772	BNE 25	;IS PGM CLOCK BIT SET?
1181	005652	104414	DEC TEMP	;BR IF YES
1182	005654	021364	BNE 15	;DEC COUNT
1183	005656	032777 000002	RTI	;BR IF NOT DONE
1184	005664	173526		;RETURN
1185	005666	001372		
1186	005672	001416		
1187	005674	000002		
1188				
1189	005676	020040 000077	MQM: .ASCIZ /*	
(2)	005702	005015 000	MCRLF: .ASCIZ <15><12>	
(2)	005705	377 053520 020122	MPFAIL: .ASCIZ <377>/PWR FAILED. RESTART AT TEST /	
(2)	005743	377 047105 020104	MEPASS: .ASCIZ <377>/END PASS DRLPM /	
(2)	005765	377 000122	MR: .ASCIZ <377>/R/	
(2)	005770	047377 020117	MERR2: .ASCIZ <377>/NO DEVICES PRESENT./	
(2)	006015	377 047111 052523	MERR3: .ASCIZ <377>/INSUFFICIENT DATA! /	
(2)	006041	377 042524 052123	MTSTPC: .ASCIZ <377>/TEST PC-/	
(2)	006053	377 047514 045503	MLOCK: .ASCIZ <377>/LOCK ON SELECTED TEST/	
(2)	006102	051503 035122	MCSRX: .ASCIZ /CSR:/	
(2)	006110	042526 035103	MVECX: .ASCIZ /VEC:/	
(2)	006116	040520 051523	MPASSX: .ASCIZ /PASSES:/	
(2)	006127	105 051122	MERRX: .ASCIZ /ERRORS:/	
(2)	006140	042524 052123	MTSTN: .ASCIZ /TEST NO:/	
(2)	006152	000052	MASTEK: .ASCIZ /*	
(2)	006154	051777 052105	MNEW: .ASCIZ <377>/SET SWITCH REG TO M8200-YC'S DESIRED ACTIVE./	
(2)	006232	041520 020072	MERRPC: .ASCIZ /PC:/	
(2)	006237	212 020040 020040	XHEAD: .ASCII <212>/ MAP OF M8200-YC STATUS/	
(2)	006301	377 020040 020040	.ASCII <377>/-----/	
(2)	006340	020212 050040	.ASCII <212>/ PC CSR STAT1 STAT2 STAT3/	
(2)	006412	026777 026455	.ASCII <377>/-----/	
(2)	006466	044377 053517	NUM: .ASCIZ <377>/HOW MANY M8200-YC'S TO BE TESTED?/	
(2)	006531	377 051503 020122	CSR: .ASCIZ <377>/CSR ADDRESS?/	
(2)	006547	042526 052103	VEC: .ASCIZ <377>/VECTOR ADDRESS?/	

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SEQ 0042

(2) 006570 041377 020122 051120 PRIO: .ASCIZ <377>/BR PRIORITY LEVEL? (4,5,6,7)?/
 (2) 006627 377 043111 042040 CRAM: .ASCIZ <377>/IF DMC HAS CRAM (M8204) TYPE "Y", IF CROM (M8200) TYPE "N" ?/
 (2) 006725 377 044127 041511 MODU: .ASCIZ <377>/WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202 TYP
 (2) 007037 377 053523 052111 LINE: .ASCIZ <377>/SWITCH PAC#1 (DDCMP LINE #)?/
 (2) 007075 377 053523 052111 BM: .ASCIZ <377>/SWITCH PAC#2 (BM873 BOOT ADD)?/
 (2) 007135 377 051511 052040 CONN: .ASCIZ <377>/IS THE LOOP BACK CONNECTOR ON?/
 (2) 007175 377 047516 042040 NOACT: .ASCIZ <377>/NO DEVICES ARE SELECTED/
 (2) 007226 005377 053523 036522 SWMES: .ASCIZ <377><12>/SWR= /
 (2) 007236 042516 037527 000040 SWMES1: .ASCIZ /NEW? /
 (2) 007244 177777 034115 030062 CONERR: .ASCIZ <377><377>/M8200-YC FOUND AT NON-STANDARD ADDRESS PC: /
 (2) 007323 377 054105 042520 CNERR: .ASCIZ <377>/EXPECTED FOUND/
 (2) 007344 024040 034115 030062 DMCM: .ASCIZ / (M8200-YC) /
 (2) 007361 040 045450 041515 KMCM: .ASCIZ / (KMC) /
 (2) 007371 377 034115 030062 SPEED: .ASCIZ <377>/M8200-YC-AR(REMOTE,LOW SPEED) OR M8200-YC-AL(LOCAL,HIGH SPEED) TYP
 (2) 007514 007514 .EVEN
 1190 007516 006 003 XSTATQ: 5
 1191 007520 001246 BYTE 6,3
 1192 007522 006 003 TEMP1
 1193 007524 001250 .BYTE 6,3
 1194 007526 006 003 TEMP2
 1195 007530 001252 .BYTE 6,3
 1196 007532 006 003 TEMP3
 1197 007534 001254 .BYTE 6,3
 1198 007536 006 002 TEMP4
 1199 007540 001256 .BYTE 6,2
 1200 .EVEN
 1201
 1202 ;BUFFERS FOR INPUT-OUTPUT
 1203
 1204 007542 000000 INBUF: 0
 1205 007604 .=.+40
 1206 007604 000000 MDATA: 0
 1207 .=.+40
 1208
 1209
 1210 ;ROUTINE USED TO CHANGE SOFTWARE SWITCH
 1211 ;REGISTER USING THE CONSOLE TERMINAL
 1212 ;-----
 1213
 1214 007646 022737 000176 001202 CKSWR: CMP #SWREG,SWR IS THE SOFT SWR BEING USED?
 1215 007654 001077 BNE CKSWRS BR IF NO
 1216 007656 105777 171322 TSTB @TKCSR IS DONE SET?
 1217 007662 100003 BPL 25 GO ON IF NOT SET
 1218 007664 012737 177777 003744 MOV #1,DONE IF DONE SET, SET FLAG
 1219 007672 022777 000007 171306 2\$: CMP #7,@TKDBR WAS CTRL G TYPED? (7 BIT ASCII)
 1220 007700 001404 BEQ 15 BR IF YES
 1221 007702 022777 000207 171276 CMP #207,@TKDBR WAS CTRL G TYPED? (8 BIT ASCII)
 1222 007710 001061 BNE CKSWRS BR IF NO
 1223 007712 010246 MOV R2,-(SP) STORE R2
 1224 007714 010346 MOV R3,-(SP) STORE R3
 1225 007716 010446 MOV R4,-(SP) STORE R4
 1226 007720 012737 177777 010056 MOV #1,SWFLG SET SOFT TYPE OUT FLAG
 1227 007726 005002 CKSWR1: CLR R2 CLEAR NEW SWR CONTENTS

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SEQ 0043

1228	007730	012704	177777		MOV	#-1,R4	SET FLAG TO ALL ONES
1229	007734	104402	007226		TYPE	,SWMES	TYPE "SWR= "
1230	007740	104411			CKSWR2:	CNVRT	TYPE OUT PRESENT CONTENTS
1231	007742	010112			SOFTSW		OF SOFT SWITCH REGISTER
1232	007744	104402	007236		CKSWR3:	TYPE	TYPE "NEW? "
1233	007750	004737	010060		CKSWR4:	JSR	GET RESPONSE
1234	007754	022703	000015			CMP	PC, INCHAR
1235	007760	001424				BEQ	#15,R3
1236	007762	022703	000012			CMP	55
1237	007765	001416				BEQ	#12,R3
1238	007770	022703	000025			CMP	45
1239	007774	001754				BEQ	#25,R3
1240	007776	022703	000007			CMP	CKSWR1
1241	010002	001762				BEQ	#7,R3
1242	010004	005004				CMP	CKSWR4
1243	010006	042703	177770			CLR	R4
1244	010012	006302				BIC	\$177770,R3
1245	010014	006302				ASL	R2
1246	010016	006302				ASL	R2
1247	010020	050302				ASL	R2
1248	010022	000752				BIS	R3,R2
1249	010024	012766	002002	000006	4S:	BR	CKSWR4
1250	010032	005704			5S:	MOV	#: START,6(SP)
1251	010034	001002				TST	R4
1252	010036	010277	171140			BNE	6S
1253	010042	005037	010056		6S:	MOV	R2, @SWR
1254	010046	012604				CLR	SWFLG
1255	010050	012603				MOV	(SP)+, R4
1256	010052	012602				MOV	(SP)+, R3
1257	010054	000207				MOV	(SP)+, R2
1258						CKSWR5:	RTS
1259	010056	000000				PC	
1260					SWFLG:	0	
1261	010060	105777	171120		INCHAR:	TSTB	@TKCSR
1262	010064	100375				BPL	-4
1263	010066	017703	171114			MOV	@TKDBR, R3
1264	010072	105777	171112			TSTB	@TPCSR
1265	010076	100375				BPL	-4
1266	010100	010377	171106			MOV	R3, @TPDBR
1267	010104	042703	000200			BIC	#BIT7,R3
1268	010110	000207				RTS	PC
1269					SOFTSW:	1	
1270	010112	000001		002		.BYTE	6,2
1271	010114	006				SWREG	
1272	010116	000176					

1273
 1274
 1275 ROUTINE USED TO "CYCLE" THROUGH UP TO 16 M8200-YC'S
 1276 THIS ROUTINE SETS UP THE CONTROL ADDRESS FOR THE DIAGNOSTIC
 1277 AND RUNS THE SPECIFIED M8200-YC'S. THIS ROUTINE *MUST*
 1278 BE RUN FIRST BEFORE ENTERING THE DIAGNOSTIC FOR THE
 1279 SETUP NECESSARY.
 1280
 1281
 1282 010120 005737 001306 CYCLE: TST DMACTV ; ARE ANY M8200-YC'S TO BE TESTED?
 1283 010124 001004 001004 BNE 1S ; BR IF OK.
 1284 010126 104402 007175 TYPE ,NOACT ; NO M8200-YC'S SELECTED!!
 1285 010132 000000 HALT ; STOP THE SHOW.
 1286 010134 000776 BR ; DISQUALIFY CONT. SW.
 1287 010136 000241 CLC ; CLEAR PROC. CARRY BIT.
 1288 010140 006137 001316 ROL ; UPDATE POINTER
 1289 010144 005537 001316 ADC ; CATCH CARRY FROM RUN
 1290 010150 062737 000004 001322 ADD ; UPDATE POINTER
 1291 010156 062737 000010 001320 ADD ; UPDATE ADDRESS POINTER.
 1292 010164 022737 001700 001320 CMP ; #DM.MAP+200, CREAM
 1293 010172 001006 BNE 2S ; KEEP GOING. NOT ALL TESTED FOR.
 1294 010174 012737 001500 001320 MOV ; RESET ADDRESS POINTER.
 1295 010202 012737 001702 001322 MOV ; RESET PASS COUNT POINTER
 1296 010210 033737 001316 001306 2S: BIT ; IS THIS ONE ACTIVE?
 1297 010216 001747 BEQ 1S ; BR IF NO
 1298 010220 013700 001320 MOV ; GET ADDRESS POINTER
 1299 010224 013702 001322 MOV ; GET PASS COUNT POINTER
 1300 010230 012037 001404 MOV ; LOAD SYSTEM CTRL. REG
 1301 010234 011037 001374 MOV ; LOAD VECTOR
 1302 010240 042737 177000 001374 BIC ; CLEAR UNWANTED BITS
 1303 010246 012037 001366 MOV ; LOAD STAT1
 1304 010252 012037 001370 MOV ; LOAD STAT2
 1305 010256 012037 001372 MOV ; LOAD STAT3
 1306 010262 012237 001230 MOV ; LOAD PASS COUNT
 1307 010266 012237 001232 MOV ; LOAD ERROR COUNT
 1308 010272 012700 000002 MOV ; SAVE CORE THIS WAY!
 1309 010276 013737 001404 001406 MOV ; DMRVEC, DMCSRH
 1310 010304 005237 001406 INC ; DMCSRH
 1311 010310 013737 001406 001410 MOV ; DMCSRH, DMCTL
 1312 010316 005237 001410 INC ; DMCTL
 1313 010322 013737 001410 001412 MOV ; DMCTL, DMP04
 1314 010330 060037 001412 ADD ; RO, DMP04
 1315 010334 013737 001412 001414 MOV ; DMP04, DMP06
 1316 010342 060037 001414 ADD ; RO, DMP06
 1317
 1318 010346 013737 001374 001376 MOV ; PTY LVL
 1319 010354 060037 001376 ADD ; RO, DMRLVL
 1320 010360 013737 001376 001400 MOV ; TX VEC
 1321 010366 060037 001400 ADD ; RO, DMTVEC
 1322 010372 013737 001400 001402 MOV ; DMTVEC, DMTLVL
 1323 010400 060037 001402 ADD ; RO, DMTLVL
 1324
 1325 010404 032737 000002 001236 BIT ; IS TEST NO. SELECTED
 1326 010412 001450 BEQ 7S ; BR IF NO

G04

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DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0045

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0046

```

1381 010614 000137 011322      JMP    ?$                ; IF NO SKIP QUESTIONS
1382 010620 012737 000001 001256  MOV    #1,TEMPS       ; START WITH 1
1383 010626 104403
1384 010630 006466
1385 010632 104405
1386 010634 000001
1387 010636 000020
1388 010640 001252
1389 010642 000
1390 010643 001
1391 010644 013737 001252 001310 12$:   MOV    TEMP3,DMNUM ; DMNUM = HOW MANY
1392 010652 104402 005702
1393 010656 104410
1394 010660 012054
1395 010662 005237 001256
1396 010666 104403
1397 010670 006531
1398 010672 104405
1399 010674 170440
1400 010676 170510
1401 010700 001254
1402 010702 000
1403 010703 001
1404 010704 013722 001254
1405 010710 104403
1406 010712 006547
1407 010714 104405
1408 010716 000000
1409 010720 000776
1410 010722 001254
1411 010724 000
1412 010725 001
1413 010726 013712 001254 10$:   MOV    TEMP4,(R2) ; STORE CSR IN MAP
1414 010732 104402
1415 010734 006570
1416 010736 004737 012340
1417 010742 022703 000024
1418 010746 101014
1419 010750 022703 000027
1420 010754 103411
1421 010756 012704 000011
1422 010762 006303
1423 010764 005304
1424 010766 001375
1425 010770 042703 170777
1426 010774 050312
1427 010776 000403
1428 011000 104402
1429 011002 005676
1430 011004 000752
1431 011006
1432 011006 000137 011300
1433 011012 104402
1434 011014 006627

      MOV    TYPE,PC_INTTY ; ASK WHAT BR LEVEL
      PRIO
      JSR    CMP #24,R3 ; GET RESPONSE
      BHI    50$           ; BR IF LESS THAN 4
      CMP    #27,R3
      BLO    50$           ; BR IF GREATER THAN 7
      MOV    #11,R4 ; R4 = NUMBER OF SHIFTS
      ASL    R3            ; SHIFT R3 LEFT
      DEC    R4            ; DEC SHIFT COUNT
      BNE    :-4           ; BR IF NOT DONE
      BIC    #170777,R3 ; BIC UNWANTED BITS
      BIS    R3,(R2)        ; PUT BR LEVEL IN STATUS MAP
      BR    8$             ; CONTINUE
      TYPE
      MQM
      BR    10$            ; RESPONSE IS OUT OF LIMITS
      8$:   JMP    33$          ; TRY AGAIN
      TYPE
      CRAM
      ; DOES DMC HAVE CRAM?
  
```

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DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0047

1435	011016	004737	012340	JSR	PC, INTTY	; GET REPLY
1436	011022	022703	000131	CMP	#131,R3	
1437	011026	001427		BEQ	9S	; YES
1438	011030	022703	000116	CMP	#116,R3	; NO
1439	011034	001403		BEQ	40S	; NOT A Y OR N
1440	011036	104402		TYPE		
1441	011040	005676		MQM		
1442	011042	000761		BR	8S	; TYPE "?"
1443	011044	104402		TYPE		; ASK AGAIN
1444	011046	007371		SPEED		
1445	011050	004737	012340	JSR	PC, INTTY	; M8200-YC-AR OR M8200-YC-AL?
1446	011054	022703	000122	CMP	#122,R3	; GET RESPONSE
1447	011060	001414		BEQ	16S	; IS IT R
1448	011062	022703	000114	CMP	#114,R3	; BR IF REMOTE
1449	011066	001403		BEQ	41S	; IS IT L
1450	011070	104402		TYPE		; BR IF LOCAL
1451	011072	005676		MQM		
1452	011074	000763		BR	40S	
1453	011076	052762	000002	000004	41S:	; TRY AGAIN
1454	011104	000402		BIS	#BIT1,4(R2)	; SET BIT1 IN STAT3
1455	011106	052712	100000		9S:	; CONTINUE
1456	011112	104402		BIS	#BIT15,(R2)	; SET BIT 15 IF CRAM
1457	011114	006725		16S:	TYPE	
1458	011116	004737	012340	MODU		; ASK WHICH LINE UNIT
1459	011122	022703	000021	JSR	PC, INTTY	; GET REPLY
1460	011126	001417		CMP	#21,R3	; "1"
1461	011130	022703	000022	BEQ	30S	
1462	011134	001412		CMP	#22,R3	; "2"
1463	011136	022703	000116	BEQ	31S	
1464	011142	001403		CMP	#116,R3	; "N"
1465	011144	104402		BEQ	32S	
1466	011146	005676		TYPE		
1467	011150	000760		MQM		
1468	011152	052722	010000	BR	16S	; IF NOT A 1,2 OR N TYPE "?"
1469	011156	022222		BIS	#BIT12,(R2)+	; TRY AGAIN
1470	011160	000447		CMP	(R2)+,(R2)+	; SET BIT 12 IN STAT2 IF NO LU
1471	011162	052712	020000	BR	33S	; POP OVER STAT2 AND STAT3
1472	011166	104402		BIS	#BIT13,(R2)	; SET BIT 13 IN STAT2 IF M8202
1473	011170	007135		30S:	TYPE	
1474	011172	004737	012340	CONN		; ASK IF LOOP-BACK IS ON
1475	011176	022703	000131	JSR	PC, INTTY	; GET REPLY
1476	011202	001406		CMP	#131,R3	; Y
1477	011204	022703	000116	BEQ	17S	
1478	011210	001406		CMP	#116,R3	; N
1479	011212	104402		BEQ	18S	
1480	011214	005676		TYPE		
1481	011216	000763		MQM		
1482	011220	052722	040000	BR	30S	; IF NOT Y OR N TYPE "?"
1483	011224	000402		BIS	#BIT14,(R2)+	; TRY AGAIN
1484	011226	042722	040000	BR	19S	; TURNAROUND IS CONNECTED
1485	011232			BIC	#BIT14,(R2)+	
1486	011232	104403		INSTR		
1487	011234	007037		LINE		
1488	011236	104405		PARAM		

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SEQ 0048

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1489 011240 000000          0
1490 011242 000377          377
1491 011244 001254          TEMP4
1492 011246 000           .BYTE
1493 011247 001           .BYTE
1494 011250 113722 001254   0
1495 011254 104403          MOVB
1496 011256 007075          INSTR
1497 011260 104405          BM
1498 011262 000000          PARAM
1499 011264 000377          0
1500 011266 001254          377
1501 011270 000           TEMP4
1502 011271 001           .BYTE
1503 011272 113722 001254   0
1504 011276 005722          MOVB
1505 011300            TST   (R2)+ ; STORE SWITCH PAC IN MAP
1506 011300 062702 000006          33$: ADD #6, R2
1507 011304 005337 001252          DEC TEMP3
1508 011310 001402          BEQ 34S
1509 011312 000137 010652          JMP 12S
1510 011316 000137 011754          JMP 13S
1511 011322 012701 170440          34$: MOV #170440, R1
1512 011326 012737 012046 000004  7S: MOV #65, @#4
1513 011334 005011            2S: CLR (R1)
1514 011336 005711            TST (R1)
1515 011340 001173            BNE 3S
1516 011342 005061 000006          CLR 6(R1)
1517 011346 000424            BR 21S
1518 011350 005761 000006          TST 6(R1)
1519 011354 001165            BNE 3S
1520 011356 012711 002000          MOV #BIT10, (R1)
1521 011362 005061 000004          CLR 4(R1)
1522 011366 012761 125252 000006  MOV #125252, 6(R1)
1523 011374 052711 020000          BIS #BIT13, (R1)
1524 011400 022761 125252 000004  CMP #125252, 4(R1)
1525 011406 001004            BNE 21S
1526 011410 052762 100000 000002  BIS #BIT15, 2(R2)
1527 011416 000431            BR 22S
1528 011420 012711 001000          21$: MOV #BIT9, (R1)
1529 011424 012761 100400 000006  MOV #100400, 6(R1)
1530 011432 012711 001400          MOV #BIT9!BIT8, (R1)
1531 011436 012711 002000          MOV #BIT10, (R1)
1532 011442 022761 000456 000006  CMP #456, 6(R1)
1533 011450 001411            BEQ 23S
1534 011452 022761 016520 000006  CMP #16520, 6(R1)
1535 011460 001410            BEQ 22S
1536 011462 022761 177777 000006  CMP #-1, 6(R1)
1537 011470 001404            BEQ 22S
1538 011472 000516            BR 3S
1539 011474 052762 000002 000006  23$: BIS #BIT1, 6(R2)
1540                      ; AT THIS POINT IT IS ASSUMED THAT R1 HOLDS A M8200-YC CSR ADDRESS.
1541 011502 010122            22$: MOV R1, (R2)+ ; STORE CSR IN CORE TABLE.
1542 011504 012711 001000            15$: MOV #BIT9, (R1) ; CLEAR LINE UNIT LOOP

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SEQ 0049

1543	011510	005061	000004		CLR	4(R1)	CLEAR PORT4
1544	011514	012761	122113	000006	MOV	#122113,6(R1)	LOAD INSTRUCTION (CLR DTR)
1545	011522	052711	000400		BIS	#BIT8,(R1)	CLOCK INSTRUCTION
1546	011526	012761	021264	000006	MOV	#021264,6(R1)	LOAD INSTRUCTION
1547	011534	052711	000400		BIS	#BIT8,(R1)	CLOCK INSTRUCTION
1548	011540	122761	000377	000004	CMPB	#377,4(R1)	IS IT ALL ONES?
1549	011546	001003			BNE	.+10	BR IF NO
1550	011550	052712	010000		BIS	#BIT12,(R2)	IF YES, NO LINE UNIT, SET STATUS BIT
1551	011554	000436			BR	20S	
1552	011556	032761	000002	000004	BIT	#BIT1,4(R1)	IS SWITCH A ONE?
1553	011564	001403			BEQ	.+10	BR IF M8201
1554	011566	052712	060000		BIS	#BIT13!BIT14,(r2)	M8202 ASSUME CONNECTOR
1555	011572	000427			BR	20S	CONNECTOR ON)
1556	011574	032761	000010	000004	BIT	#BIT3,4(R1)	IS MRDY SET
1557	011602	001023			BNE	20S	BR IF M8201 NO CONNECTOR (ON LINE)
1558	011604	012761	000100	000004	MOV	#BIT6,4(R1)	LOAD PORT4
1559	011612	012761	122113	000006	MOV	#122113,6(R1)	LOAD INSTRUCTION
1560	011620	052711	000400		BIS	#BIT8,(R1)	CLOCK INSTRUCTION(SET DTR)
1561	011624	012761	021264	000006	MOV	#021264,6(R1)	LOAD INSTRUCTION
1562	011632	052711	000400		BIS	#BIT8,(R1)	CLOCK INSTRUCTION(READ MODEM REG)
1563	011636	032761	000010	000004	BIT	#BIT3,4(R1)	IS MRDY SET NOW?
1564	011644	001402			BEQ	20S	BR IF NO CONNECTOR
1565	011646	052712	040000		BIS	#BIT14,(R2)	SET STATUS BIT FOR CONNECTOR
1566	011652	005722			TST	(R2)+	POP POINTER
1567	011654	012761	021324	000006	MOV	#021324,6(R1)	PUT INSTRUCTION IN PORT6
1568	011662	012711	001400		MOV	#BIT9!BIT8,(R1)	PORT4+LU 15
1569	011666	156122	000004		BISB	4(R1),(R2)+	STORE DDCMP LINE # IN TABLE
1570	011672	012761	021344	000006	MOV	#021344,6(R1)	PORT6+INSTRUCTION
1571	011700	012711	001400		MOV	#BIT8!BIT9,(R1)	CLOCK INSTR.
1572	011704	156122	000004		BISB	4(R1),(R2)+	STORE BM873 ADD IN TABLE
1573	011710	005722			TST	(R2)+	POP OVER STAT3
1574	011712	005011			CLR	(R1)	CLEAR ROMI
1575	011714	005237	001310		INC	DMNUM	UPDATE DEVICE COUNTER
1576	011720	022737	000020	001310	CMP	#20,DMNUM	ARE MAX. NO. OF DEV FOUND?
1577	011726	001412			BEQ	13S	YES DON'T LOOK FOR ANY MORE.
1578	011730	005011			3S:	CLR	CLEAR BIT 10
1579	011732	005061	000006		CLR	6(R1)	CLEAR SEL 6
1580	011736	062701	000010		14S:	ADD	UPDATE CSR POINTER ADDRESS
1581	011742	022701	170510		CMP	#170510,R1	
1582	011746	001402			BEQ	13S	BR IF DONE
1583	011750	000137	011334		JMP	2S	JUMP IF NOT
1584	011754	005037	001306		13S:	CLR	DMACTV
1585	011760	005737	001310		TST	DMNUM	WERE ANY M8200-YC'S FOUND AT ALL?
1586	011764	001423			BEQ	SS	ERROR AUTO SIZER FOUND NO M8200-YC'S IN THIS SYS.
1587	011766	013701	001310		MOV	DMNUM,R1	
1588	011772	010137	001314		MOV	R1,SAVNUM	SAVE NUMBER OF DEVICES
1589	011776	000241			4S:	CLC	
1590	012000	006137	001306		ROL	DMACTV	GENERATE ACTIVE REGISTER OF DEVICES.
1591	012004	005237	001306		INC	DMACTV	SET THE BIT
1592	012010	005301			DEC	R1	
1593	012012	001371			BNE	4S	BR IF MORE TO GENERATE
1594	012014	012737	000006	000004	MOV	#6,a#4	RESTORE TRAP VECTOR
1595	012022	013737	001306	001312	MOV	DMACTV,SAVACT	SAVE ACTIVE REGISTER
1596	012030	000137	012062		JMP	VECMAP	GO FIND THE VECTOR NOW.

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0050

1597	012034	104402	005770	SS:	TYPE	MERR2		
1598	012040	005000			CLR	R0	; NOTIFY OPR THAT NO M8200-YC'S FOUND.	
1599	012042	000000			HALT		; MAKE DATA LIGHTS ZERO	
1600	012044	000776			BR	-2	; STOP THE SHOW	
1601	012046	012716	011736	6S:	MOV	#14\$, (SP)	; DISABLE CONT. SW.	
1602	012052	000002			RTI		; ENTERED BY NON-EXISTANT TIME-OUT.	
1603							; RETURN TO MAINSTREAM	
1604	012054	000001		WHICH: 1				
1605	012056	002	002		.BYTE	2,2		
1606	012060	001256			TEMPS			
1607								
1608	012062	032737	000001	001236	VECMAP:	BIT	#SWOO, STRTSW	
1609	012070	001114			BNE	SS		
1610	012072	012737	000340	000022	MOV	#340, J#22	; SET IOT TRAP PRIO TO ?	
1611	012100	012737	012254	000020	MOV	#45, J#20	; SET IOT TRAP VECTOR	
1612	012106	012702	001500		MOV	#DM.MAP, R2	; SET SOFTWARE POINTER	
1613	012112	012700	000300		MOV	#300, R0	; FLOATING VECTORS START HERE.	
1614	012116	012701	000302		MOV	#302, R1	; PC OF IOT INSTR.	
1615	012122	010120		1S:	MOV	R1, (R0)+	; START FILLING VECTOR AREA	
1616	012124	012721	000004		MOV	#4, (R1)+	; WITH .+2; IOT	
1617	012130	022021			CMP	(R0)+ (R1)+	; ADD 2 TO R0 +R1	
1618	012132	020127	001000		CMP	R1, #1000		
1619	012136	101771			BLOS	1S		
1620	012140	013737	001306	001246	MOV	DMACTV, TEMP1	; BR IF MORE TO FILL	
1621	012146	006037	001246		ROR	TEMP1	; STORE TEMPORALLY	
1622	012152	103063			BCC	SS	; BR IF ALL DONE	
1623	012154	012704	000012		MOV	#12, R4	; R4 IS INDEX REGISTER	
1624	012160	016437	012324	177776	MOV	BRLVL(R4), PS	; SET PS TO 7	
1625	012166	011201			MOV	(R2), R1		
1626	012170	012761	000200	000004	MOV	#200, 4(R1)		
1627	012176	012711	001000		MOV	#BIT9, (R1)	; SET ROMI	
1628	012202	012761	121111	000006	MOV	#121111, 6(R1)	; PUT INSTRUCTION IN PORT6	
1629	012210	012711	001400		MOV	#BIT9:BIT8, (R1)	; FORCE AN INTERRUPT	
1630	012214	105200		7S:	INCB	RO	; STALL	
1631	012216	001376			BNE	-2	; FOR TIME TO INTERRUPT	
1632	012220	162704	000002		SUB	#2, R4	; GET NEXT LOWEST PS LEVEL	
1633	012224	001404			BEQ	6S	; BR IF R4 = 0	
1634	012226	016437	012324	177776	MOV	BRLVL(R4), PS	; MOVE NEXT LOWER LEVEL IN PS	
1635	012234	000767			BR	7S	; BR TO DELAY	
1636	012236	052762	005300	000002	6S:	BIS	#5300, 2(R2)	; NO INTERRUPT ASSUME 300 AT LEVEL 5 AND FIX M8200-YC LATE
1637	012244	005011		3S:	CLR	(R1)	; CLEAR ROMI	
1638	012246	062702	000010		ADD	#10, R2	; POP SOFTWARE POINTER	
1639	012252	000735			BR	2S	; KEEP GOING	
1640	012254	051662	000002	4S:	BIS	(SP), 2(R2)	; GET VECTOR ADDRESS	
1641	012260	042762	000007	000002	BIC	#7, 2(R2)	; CLEAR JUNK	
1642	012266	016405	012326		MOV	BRLVL+2(R4), R5	; GET BR LEVEL OF M8200-YC	
1643	012272	006305			ASL	RS	; SHIFT LEVEL 4 PLACES	
1644	012274	006305			ASL	RS	; TO THE LEFT FOR THE	
1645	012276	006305			ASL	RS	; STATUS TABLE	
1646	012300	006305			ASL	RS		
1647	012302	042705	170777		BIC	#170777, RS	; CLEAR UNWANTED BITS	
1648	012306	050562	000002		BIS	RS, 2(R2)	; PUT BR LEVEL IN STATUS TABLE	
1649	012312	022626			CMP	(SP)+ (SP)+	; POP IOT JUNK OFF STACK	
1650	012314	012716	012244		MOV	#3\$, (\$P)	; SET FOR RETURN	

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 DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0051

1651	012320	000002		RTI			
1652	012322	000207		SS:	RTS	PC	;ALL DONE WITH "AUTO SIZING"
1653				BRLVL:	0	;LEVEL 0	
1654	012324	000000			0	;LEVEL 0	
1655	012326	000000			200	;LEVEL 4	
1656	012330	000200			240	;LEVEL 5	
1657	012332	000240			300	;LEVEL 6	
1658	012334	000300			340	;LEVEL 7	
1659	012336	000340					
1660							
1661							
1662	012340	105777	166640	INTTY:	TSTB	ATKCSR	;WAIT FOR DONE
1663	012344	100375			BPL	-4	
1664	012346	017703	166634		MOV	ATKDBR,R3	;PUT CHAR IN R3
1665	012352	105777	166632		TSTB	ATPCSR	;WAIT UNTIL PRINTER IS READY
1666	012356	100375			BPL	-4	
1667	012360	010377	166626		MOV	R3,ATPD8R	;ECHO CHAR
1668	012364	042703	000240		BIC	#BIT7:BITS,R3	;MASK OFF LOWER CASE
1669	012370	000207			RTS	PC	;RETURN
1670							
1671							
1672	012372	000000		ROMMAP:	0		;POINTER TO HI OR LO SPEED MICRO-CODE
1673				LOMAP:			
1674	012374			HIMAP:			;MICRO-CODE
1675	012374						
1676							

1677
 1678
 1679
 1680 ;***** TEST 1 *****
 1681 ;THIS IS A SPECIAL TEST WHICH WILL RUN ON A KMC (DMC WITH
 1682 ;WRITTABLE CONTROL STORE) TO LOAD THE CRAM WITH THE DDCMP
 1683 ;MICRO-CODE. FIRST BE SURE BIT1 OF STAT3 IS SET UP AS FOLLOWS
 1684 ;1=LOCAL HIGH SPEED CODE, 0=REMOTE LOW SPEED CODE THE STATUS
 1685 ;OF STAT3 BIT1 DETERMINES WHICH MICRO-CODE WILL
 1686 ;BE LOADED IN THE KMC. LOOP ON THIS TEST FOR A FEW SECONDS
 1687 ;TO LOAD THE KMC.
 1688 ;*****
 1689
 1690 ; TEST 1
 1691-----
 1692 016376 012737 000001 001226 TST1:
 1693 016404 012737 016470 001216 MOV #1 TSTNO
 MOV #TST2,NEXT
 1694 016412 004737 022426 JSR PC,MAPCK
 1695 016416 032737 100000 BIT #BIT15,STAT1 ;R1 CONTAINS BASE M8200-YC ADDRESS
 1696 016424 001420 BEQ 2\$;CHECK FOR HI OR LO
 1697 016426 005000 CLR R0 ;BE SURE DMC HAS CRAM
 1698 016430 013702 MOV ROMMAP,R2 ;SKIP IF NO CRAM
 1699 016434 012711 002000 MOV #BIT10,(R1) ;R0=CRAM ADDRESS
 1700 016440 010061 000004 MOV R0,4(R1) ;R2 POINTS TO ROMMAP
 1701 016444 012261 000006 MOV (R2)+,6(R1) ;SET ROMO
 1702 016450 052711 020000 BIS #BIT13,(R1) ;LOAD CRAM ADDRESS
 1703 016454 005200 INC R0 ;LOAD WORD TO BE WRITTEN
 1704 016456 022700 002000 CMP #2000,R0 ;WRITE IT!
 1705 016462 001364 BNE 1\$;NEXT ADDRESS
 1706 016464 005011 CLR (R1) ;DONE YET?
 1707 016466 104400 SCOPE ;BR IF NO
 ;CLEAR SEL0
 1708 ;SCOPE THIS TEST
 1709
 1710
 1711 ;***** TEST 2 *****
 1712 ;TEST OF BR RIGHT SHIFT
 1713 ;VERIFY THAT A DEST OF BR RSH (011) OF A MICRO-INSTRUCTION
 1714 ;SHIFTS THE RESULTING BR DATA RIGHT ONCE.
 1715 ;*****
 1716
 1717 ; TEST 2
 1718-----
 1719 016470 012737 000002 001226 TST2:
 1720 016476 012737 016602 001216 MOV #2 TSTNO
 MOV #TST3,NEXT
 1721 016504 104412 MSTCLR ;R1 CONTAINS BASE M8200-YC ADDRESS
 1722 016506 013701 001404 MOV DMCSR,R1 ;MASTER CLEAR M8200-YC
 1723 016512 005011 CLR (R1) ;R1 = DMC BASE ADDRESS
 1724 016514 012705 MOV #52525,R5 ;CLEAR SEL0
 1725 016520 010561 000004 MOV R5,4(R1) ;START WITH 125
 1726 016524 104414 ROMCLK ;PORT4+125
 1727 016526 120500 120500 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 1728 016530 104414 ROMCLK ;BR + PORT4
 1729 016532 061620 061620 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 1730 ;BR RSH+BR, SHIFT BR RIGHT

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DRLPM.P11 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

SEQ 0053

1731 016534 104414	016536 061225	ROMCLK 061225	RS	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1732 016536 061225	006005	ROR	RS	PORTS-BR
1733 016540 006005	116104	MOV8	S(R1), R4	RS = "EXPECTED"
1734 016542 116104	120504	CMPB	R5, R4	R4 = "FOUND"
1735 016546 120504	001401	BEQ	19	DID BR SHIFT RIGHT ONCE?
1736 016550 001401	104012	HLT	12	BR IF YES
1737 016552 104012				BR RIGHT SHIFT ERROR
1738 016554 104414				
1739 016554 104414	061620	ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1740 016556 061620	104414	061620		BR RSH-BR, SHFT BR RIGHT AGAIN
1741 016560 104414	061225	ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1742 016562 061225	006005	061225		PORTS-BR
1743 016564 006005	116104	ROR	RS	RS = "EXPECTED"
1744 016566 116104	120504	MOV8	S(R1), R4	R4 = "FOUND"
1745 016572 120504	001401	CMPB	R5, R4	DID BR SHIFT RIGHT?
1746 016574 001401	104012	BEQ	25	BR IF YES
1747 016576 104012		HLT	12	BR RIGHT SHIFT ERROR
1748 016600 104400		SCOPE		SCOPE THIS TEST
1749				
1750				
1751				***** TEST 3 *****
1752				*CROM READ TEST
1753				*THIS TEST READS EACH ROM LOCATION AND COMPARES
1754				*IT TO A SOFTWARE DUPLICATE OF THE CROM. THIS TEST
1755				*ALSO TESTS THE JUMP(I) MICRO-PROCESSOR INSTRUCTION.
1756				*IF THIS TEST FAILS CHECK YOUR CROM PART NUMBERS.
1757				*DRLPM-A SUPPORTS THE FOLLOWING PART NUMBERS:
1758				*
1759				*M8200-YC-AR (M8200-YA)
1760				*****
1761				
1762				: TEST 3
1763				-----
1764 016602 012737 000003 001226	TST3:	MOV	#3, TSTNO	
1765 016610 012737 016776 001216		MOV	#T\$T4, NEXT	
1766 016616 012737 016654 001220		MOV	#1\$, LOCK	
1767				
1768 016624 104412		MSTCLR		R1 CONTAINS BASE M8200-YC ADDRESS
1769 016626 032737 100000 001366		BIT	#BIT15, STAT1	MASTER CLEAR M8200-YC
1770 016634 001057		BNE	4\$	IS IT RAM OR ROM
1771 016636 004737 022426		JSR	PC, MAPCK	SKIP TEST IF CRAM
1772 016642 005011		CLR	(R1)	CHECK FOR HI OR LO
1773 016644 013700 012372		MOV	ROMMAP, R0	CLEAR RUN
1774 016650 005002		CLR	R2	R0 POINTS TO SOFTWARE ROM MAP
1775 016652 005003		CLR	R3	R2 CONTAINS ROM ADDRESS BITS 0-7
1776 016654 042737 014377 016674	1S:	BIC	#14377, 2\$	R3 CONTAINS ROM ADDRESS BITS 8&9 IN BITS 11&12
1777 016662 050237 016674		BIS	R2, 2\$	CLEAR ADDRESS FIELDS OF INSTRUCTION
1778 016666 050337 016674		BIS	R3, 2\$	ADD BITS 0-7 TO INSTRUCTION
1779 016672 104414		ROMCLK		ADD BITS 11&12 TO INSTRUCTION
1780 016674 100400		100400		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1781 016676 012711 002000		MOV	#BIT10, (R1)	JUMP(I) TO ROM ADDRESS IN R2 & R3
1782 016702 011005		MOV	(R0), RS	SET ROM0
1783 016704 016104 000006		MOV	6(R1), R4	PUT "EXPECTED" IN RS
1784 016710 020504		CMP	RS, R4	PUT "FOUND" IN R4
				COMPARE ROM CONTENTS TO SOFT DUP

1785 016712 001414 BEQ 3S ;BR IF OK
 1786 016714 010337 001252 MOV R3, TEMP₃ ;PUT ROM ADDRESS IN TEMP3
 1787 016720 000241 CLC
 1788 016722 006037 001252 ROR TEMP₃
 1789 016726 006037 001252 ROR TEMP₃
 1790 016732 006037 001252 ROR TEMP₃
 1791 016736 050237 001252 BIS R2, TEMP₃ ;TEMP₃ NOW CONTAINS CORRECT ADDRESS
 1792 016742 104004 HLT 4 ;ROM READ ERROR
 1793 016744 104401 3S: SCOP1 (R0)+ ;LOOP TO 1S IF SW09=1
 1794 016746 005720 TST R2 ;BUMP SOFT POINTER
 1795 016750 005202 INC R2 ;BUMP ROM ADDRESS
 1796 016752 022702 000400 CMP #400, R2 ;IS R2 TO MAX YET?
 1797 016756 001336 BNE 1S ;BR IF NO
 1798 016760 005002 CLR R2 ;YES, RESET R2 TO 0
 1799 016762 062703 004000 ADD #4000, R3 ;INC TO NEXT PAGE OF ROM
 1800 016766 022703 020000 CMP #20000, R3 ;DONE YET?
 1801 016772 001330 BNE 1S ;BR IF NO
 1802 016774 104400 SCOPE ;SCOPE THIS TEST
 1803
 1804
 1805 ;***** TEST 4 *****
 1806 ;CROM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.
 1807 ;PERFORM THE JUMP INSTRUCTION
 1808 ;VERIFY THAT THE JUMP DID NOT OCCUR BY READING
 1809 ;THE CONTENTS OF THE NEW ROM PC (IT SHOULD INCREMENT BY ONE).
 1810 ;*****
 1811 ; TEST 4
 1812 ;-----
 1813
 1814 016776 012737 000004 001226 TST4: MOV #4, TSTNO
 1815 017004 012737 017172 001216 MOV #T\$T5, NEXT
 1816 017012 012737 017036 001220 MOV #1S, LOCK ;R1 CONTAINS BASE M8200-YC ADDRESS
 1817
 1818 017020 104412 MSTCLR ;MASTER CLEAR M8200-YC
 1819 017022 032737 100000 001366 BIT #BIT15, STAT1 ;IS IT CRAM?
 1820 017030 001057 BNE 6S+2 ;SKIP TEST IF YES
 1821 017032 004737 022426 JSR PC, MAPCK ;CHECK FOR HI OR LO
 1822 017036 004737 022272 1S: JSR PC, CLRALL ;CLEAR ALL CONDITIONS
 1823 017042 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 1824 017044 100400 100400 ;START AT ROM PC=0
 1825 017046 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 1826 017050 114377 114377!<400*0> ;JUMP TO ROM PC OF 1777
 1827 017052 004737 022364 JSR PC, ROMDAT ;RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 1828 017056 000002 2 ;INDEX
 1829 017060 020504 CMP RS, R4 ;ARE NEW PC CONTENTS CORRECT?
 1830 017062 001401 BEQ 2S ;BR IF YES
 1831 017064 104006 HLT 6 ;ERROR, CROM PC IS WRONG
 1832 017066 104401 2S: SCOP1 ;LOOP TO 1S IF SW09=1
 1833 017070 012737 017076 001220 3S: MOV #3S, LOCK ;NEW SCOP1
 1834 017076 004737 022272 JSR PC, CLRALL ;CLEAR ALL CONDITIONS
 1835 017076 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 1836 017076 004737 100403 100403 ;START AT ROM PC=3

DOS

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DRLPM.P11 CROM JUMP TESTS

SEQ 0055

1839	017106	104414				ROMCLK	100000! <400*0>	JUMP TO	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1840	017110	100000				JSR	PC,ROMDAT		ROM PC OF 0
1841	017112	004737	022364						R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1842	017116	000010				10			INDEX
1843	017120	020504				CMP	R5,R4		ARE NEW PC CONTENTS CORRECT?
1844	017122	001401				BEQ	45		BR IF YES
1845	017124	104006				HLT	6		ERROR, CROM PC IS WRONG
1846	017126	104401				SCOP1			LOOP TO 35 IF SW09=1
1847	017130	012737	017136	001220	45:	MOV	#5\$,LOCK		NEW SCOP1
1848	017136				55:	JSR	PC,CLRALL		CLEAR ALL CONDITIONS
1849	017136	004737	022272			ROMCLK	100406		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1850	017142	104414				ROMCLK	104125!	<400*0>	START AT ROM PC=6
1851	017144	100406				JSR	PC,ROMDAT		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1852	017146	104414				16			JUMP TO ROM PC OF 525
1853	017150	104125				CMP	R5,R4		R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1854	017152	004737	022364			BEQ	65		INDEX
1855	017156	000016				HLT	6		ARE NEW ROM PC CONTENTS CORRECT?
1856	017160	020504				SCOP1			BR IF YES
1857	017162	001401				SCOPE			ERROR, CROM PC IS WRONG
1858	017164	104006							LOOP TO 55 IF SW59=1
1859	017166	104401							,SCOPE THIS TEST
1860	017170	104400							
1861									
1862									
1863									***** TEST 5 *****
1864									*CROM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.
1865									*PERFORM THE JUMP INSTRUCTION
1866									*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
1867									*****
1868									
1869									: TEST 5
1870									-----
1871	017172	012737	000005	001226	TST5:	MOV	\$5,TSTNO		
1872	017200	012737	017352	001216		MOV	\$T\$T6,NEXT		
1873	017206	012737	017232	001220		MOV	\$1\$,LOCK		
1874									R1 CONTAINS BASE M8200-YC ADDRESS
1875	017214	104412				MSTCLR			MASTER CLEAR M8200-YC
1876	017216	032737	100000	001366		BIT	#BIT15,STAT1		IS IT CRAM?
1877	017224	001051				BNE	65+2		SKIP TEST IF YES
1878	017226	004737	022426			JSR	PC,MAPCK		CHECK FOR HI OR LO
1879	017232	104414							
1880	017234	100400				ROMCLK			NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1881	017236	104414				100400			START AT ROM PC=0
1882	017240	114777				ROMCLK			NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1883	017242	004737	022364			114377!	<400*1>		JUMP TO ROM PC OF 1777
1884	017242	004737				JSR	PC,ROMDAT		R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
1885	017246	003776				3776			INDEX
1886	017250	020504				CMP	R5,R4		ARE NEW PC CONTENTS CORRECT?
1887	017252	001401				BEQ	25		BR IF YES
1888	017254	104006				HLT	6		ERROR, CROM PC IS WRONG
1889	017256	104401				SCOP1			LOOP TO 15 IF SW09=1
1890	017260	012737	017266	001220	25:	MOV	#3\$,LOCK		NEW SCOP1
1891	017266				35:	ROMCLK			
1892	017266	104414							NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

1893 017270 100403
 1894 017272 104414
 1895 017274 100400
 1896 017276 004737 022364
 1897 017302 000000
 1898 017304 020504
 1899 017306 001401
 1900 017310 104006
 1901 017312 104401
 1902 017314 012737 017322 001220 4S:
 1903 017322 104414
 1904 017324 100406
 1905 017326 104414
 1906 017330 104525 022364
 1907 017332 004737
 1908 017336 001252
 1909 017340 020504
 1910 017342 001401
 1911 017344 104006
 1912 017346 104401
 1913 017350 104400
 1914 017352 012737 000006 001226 TST6:
 1925 017360 012737 017546 001216
 1926 017366 012737 017412 001220
 1927 017374 104412
 1928 017376 032737 100000 001366
 1929 017404 001057
 1930 017406 004737 022426
 1931 017412 004737 022340
 1932 017416 104414
 1933 017420 100400
 1934 017422 104414
 1935 017424 115377 022364
 1936 017426 004737
 1937 017432 003776
 1938 017434 020504
 1939 017436 001401
 1940 017440 104006
 1941 017442 104401
 1942 017444 012737 017452 001220 2S:
 1943 017452
 1944 017452

100403
 ROMCLK
 100000!<400*1> JUMP TO
 JSR PC,ROMDAT 0
 CMP R5, R4
 BEQ 4S
 HLT 6
 SCOP1
 MOV #5\$, LOCK

START AT ROM PC=3
 NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ROM PC OF 0
 R5=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 INDEX
 ARE NEW PC CONTENTS CORRECT?
 BR IF YES
 ERROR, CROM PC IS WRONG
 LOOP TO 3S IF SW09=1
 NEW SCOP1

ROMCLK
 100406
 ROMCLK
 104125!<400*1>
 JSR PC,ROMDAT 1252
 CMP R5, R4
 BEQ 6S
 HLT 6
 SCOP1
 SCOPE

NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 START AT ROM PC=6
 NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 JUMP TO ROM PC OF 525
 R5=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 INDEX
 ARE NEW ROM PC CONTENTS CORRECT?
 BR IF YES
 ERROR, CROM PC IS WRONG
 LOOP TO 5S IF SW59=1
 SCOPE THIS TEST

**** TEST 6 ****
 *CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
 *SET THE C BIT, PERFORM THE JUMP INSTRUCTION.
 *VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

TEST 6

MOV #6, TSTNO
 MOV #TST7, NEXT
 MOV #1\$, LOCK

MSTCLR
 BIT #BIT15, STAT1
 BNE 6S+2
 JSR PC, MAPCK

JSR PC, SETC ;SET THE C BIT

ROMCLK
 100400
 ROMCLK
 114377!<400*2>
 JSR PC,ROMDAT 3776
 CMP R5, R4
 BEQ 2S
 HLT 6
 SCOP1
 MOV #3\$, LOCK

R1 CONTAINS BASE M8200-YC ADDRESS
 MASTER CLEAR M8200-YC
 IS IT CRAM?
 SKIP TEST IF YES
 CHECK FOR HI OR LO

NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 START AT ROM PC=0
 NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 JUMP TO ROM PC OF 1777
 R5=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 INDEX
 ARE NEW PC CONTENTS CORRECT?
 BR IF YES
 ERROR, CROM PC IS WRONG
 LOOP TO 1S IF SW09=1
 NEW SCOP1

1947 017452 004737 022340
 1948 017456 104414
 1949 017460 100403
 1950 017462 104414
 1951 017464 101000
 1952 017466 004737 022364
 1953 017472 000000
 1954 017474 020504
 1955 017476 001401
 1956 017500 104006
 1957 017502 104401
 1958 017504 012737 017512 001220 4\$:
 1959 017512 004737 022340 5\$:
 1960 017512 004737 022340
 1961 017516 104414
 1962 017520 100406
 1963 017522 104414
 1964 017524 105125
 1965 017526 004737 022364
 1966 017532 001252
 1967 017534 020504
 1968 017536 001401
 1969 017540 104006
 1970 017542 104401
 1971 017544 104400
 1972
 1973
 1974 ;***** TEST 7 *****
 1975 ;CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
 1976 ;SET THE Z BIT, PERFORM THE JUMP INSTRUCTION.
 1977 ;VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
 1978 ;*****
 1979
 1980 ; TEST 7
 1981 -----
 1982 017546 012737 000007 001226 TST7:
 1983 017554 012737 017742 001216
 1984 017562 012737 017606 001220
 1985
 1986 017570 104412
 1987 017572 032737 100000 001366
 1988 017600 001057
 1989 017602 004737 022426
 1990 017606
 1991 017606 004737 022356 1\$:
 1992 017612 104414
 1993 017614 100400
 1994 017616 104414
 1995 017620 115777
 1996 017622 004737 022364
 1997 017626 003776
 1998 017630 020504
 1999 017632 001401
 2000 017634 104006

JSR PC,SETC ;SET THE C BIT
 ROMCLK 100403 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ROMCLK 100406 :START AT ROM PC=3
 ROMCLK 104125!<400*2> :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ROM CLK OF 0 :ROM PC OF 0
 JSR PC,ROMDAT R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
 0 INDEX
 CMP R5,R4 ARE NEW PC CONTENTS CORRECT?
 BEQ 4\$ BR IF YES
 HLT 6 ERROR, CROM PC IS WRONG
 SCOP1 LOOP TO 3\$ IF SW09=1
 MOV #5\$,LOCK NEW SCOP1
 JSR PC,SETC ;SET THE C BIT
 ROMCLK 100406 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ROMCLK 1252 :START AT ROM PC=6
 ROMCLK 104125!<400*2> :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 JSR PC,ROMDAT R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
 1252 INDEX
 CMP R5,R4 ARE NEW ROM PC CONTENTS CORRECT?
 BEQ 6\$ BR IF YES
 HLT 6 ERROR, CROM PC IS WRONG
 SCOP1 LOOP TO 5\$ IF SW59=1
 SCOPE SCOPE THIS TEST

;***** TEST 7 *****
 ;CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
 ;SET THE Z BIT, PERFORM THE JUMP INSTRUCTION.
 ;VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
 ;*****
 ; TEST 7

 MOV #7 TSTNO
 MOV #TST10 NEXT
 MOV #15,LOCK
 MSTCLR
 BIT #BIT15,STAT1 :R1 CONTAINS BASE M8200-YC ADDRESS
 BNE 6\$+2 :MASTER CLEAR M8200-YC
 JSR PC,MAPCK :IS IT CRAM?
 ;SKIP TEST IF YES
 ;CHECK FOR HI OR LO

JSR PC,SETZ ;SET THE Z BIT
 ROMCLK 100400 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ROMCLK 114377!<400*3> :START AT ROM PC=0
 ROM CLK OF 1777 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 JSR PC,ROMDAT R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
 3776 INDEX
 CMP R5,R4 ARE NEW PC CONTENTS CORRECT?
 BEQ 2\$ BR IF YES
 HLT 6 ERROR, CROM PC IS WRONG

G05

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SEQ 0058

2001	017636	104401			2S:	SCOP1		;LOOP TO 1S IF SW09=1
2002	017640	012737	017646	001220	3S:	MOV	#3\$,LOCK	;NEW SCOP1
2003	017646					JSR	PC,SETZ ;SET THE Z BIT'	
2004	017646	004737	022356			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2005	017652	104414				100403		START AT ROM PC=3
2006	017654	100403				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2007	017656	104414				100000!<400*3>	:JUMP TO	ROM PC OF 0
2008	017660	101400				JSR	PC,ROMDAT	;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2009	017662	004737	022364			O		INDEX
2010	017666	000000				CMP	R5,R4	ARE NEW PC CONTENTS CORRECT?
2011	017670	020504				BEQ	4S	BR IF YES
2012	017672	001401				HLT	6	ERROR, CROM PC IS WRONG
2013	017674	104006				SCOP1		;LOOP TO 3S IF SW09=1
2014	017676	104401			4S:	MOV	#5\$,LOCK	;NEW SCOP1
2015	017700	012737	017706	001220	5S:	JSR	PC,SETZ ;SET THE Z BIT'	
2016	017706		022356			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2017	017712	104414				100406		START AT ROM PC=6
2018	017714	100406				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2019	017716	104414				104125!<400*3>	:JUMP TO ROM PC OF 525	
2020	017720	105525				JSR	PC,ROMDAT	;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2021	017722	004737	022364			1252		INDEX
2022	017726	001252				CMP	R5,R4	ARE NEW ROM PC CONTENTS CORRECT?
2023	017730	020504				BEQ	6S	BR IF YES
2024	017732	001401				HLT	6	ERROR, CROM PC IS WRONG
2025	017734	104006				SCOP1		;LOOP TO 5S IF SW59=1
2026	017736	104401				SCOPE		;SCOPE THIS TEST
2027	017740	104400						
2028								
2029								
2030								
2031								***** TEST 10 *****
2032								*CROM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
2033								*SET THE BRO BIT, PERFORM THE JUMP INSTRUCTION
2034								*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
2035								*****
2036								
2037								; TEST 10
2038								-----
2039	017742	012737	000010	001226	TST10:	MOV	#10,TSTNO	
2040	017750	012737	020136	001216		MOV	#TST11,NEXT	
2041	017756	012737	020002	001220		MOV	#1\$,LOCK	
2042						MSTCLR		R1 CONTAINS BASE M8200-YC ADDRESS
2043	017764	104412				BIT	#BIT15,STAT1	MASTER CLEAR M8200-YC
2044	017766	032737	100000	001366		BNE	6S+2	IS IT CRAM?
2045	017774	001057				JSR	PC,MAPCK	SKIP TEST IF YES
2046	017776	004737	022426					CHECK FOR HI OR LO
2047	020002					JSR	PC,SETBRO	
2048	020002	004737	022310			ROMCLK		SET THE BRO BIT'
2049	020006	104414				100400		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2050	020010	100400				ROMCLK		START AT ROM PC=0
2051	020012	104414				114377!<400*4>		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2052	020014	116377				JSR	PC,ROMDAT	:JUMP TO ROM PC OF 1777
2053	020016	004737	022364			3776		;RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2054	020022	003776						INDEX

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SEQ 0059

2055	020024	020504			CMP	R5,R4	ARE NEW PC CONTENTS CORRECT?	
2056	020026	001401			BEQ	25	BR IF YES	
2057	020030	104006			HLT	6	ERROR, CROM PC IS WRONG	
2058	020032	104401			SCOP1		LOOP TO 1\$ IF SW09=1	
2059	020034	012737	020042	001220	MOV	#3\$,LOCK	NEW SCOP1	
2060	020042				JSR	PC,SETBRO	SET THE BRO BIT'	
2061	020042	004737	022310		ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304	
2062	020046	104414			100403		START AT ROM PC=3	
2063	020050	100403			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304	
2064	020052	104414			100000!<400*4>	JUMP TO	ROM PC OF 0	
2065	020054	102000			JSR	PC,ROMDAT	RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA	
2066	020056	004737	022364		0		INDEX	
2067	020062	000000			CMP	R5,R4	ARE NEW PC CONTENTS CORRECT?	
2068	020064	020504			BEQ	45	BR IF YES	
2069	020066	001401			HLT	6	ERROR, CROM PC IS WRONG	
2070	020070	104006			SCOP1		LOOP TO 3\$ IF SW09=1	
2071	020072	104401			MOV	#5\$,LOCK	NEW SCOP1	
2072	020074	012737	020102	001220	JSR	PC,SETBRO	SET THE BRO BIT'	
2073	020102				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304	
2074	020102	004737	022310		100406		START AT ROM PC=6	
2075	020106	104414			ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304	
2076	020110	100406			104125!<400*4>	JUMP TO ROM PC OF 525		
2077	020112	104414			JSR	PC,ROMDAT	RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA	
2078	020114	106125			1252		INDEX	
2079	020116	004737	022364		CMP	R5,R4	ARE NEW ROM PC CONTENTS CORRECT?	
2080	020122	001252			BEQ	65	BR IF YES	
2081	020124	020504			HLT	6	ERROR, CROM PC IS WRONG	
2082	020126	001401			SCOP1		LOOP TO 5\$ IF SW59=1	
2083	020130	104006			SCOPE		SCOPE THIS TEST	
2084	020132	104401						
2085	020134	104400						
2086								
2087								
2088							***** TEST 11 *****	
2089							*CROM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.	
2090							*SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION	
2091							*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC	
2092							*****	
2093								
2094							: TEST 11	
2095							-----	
2096	020136	012737	000011	001226	TST11:	MOV	#11,TSTNO	
2097	020144	012737	020332	001216		MOV	#TST12,NEXT	
2098	020152	012737	020176	001220		MOV	#15,LOCK	R1 CONTAINS BASE M8200-YC ADDRESS
2099						MSTCLR		MASTER CLEAR M8200-YC
2100	020160	104412				BIT	#BIT15,STAT1	IS IT CRAM?
2101	020162	032737	100000	001366		BNE	65+2	SKIP TEST IF YES
2102	020170	001057				JSR	PC,MAPCK	CHECK FOR HI OR LO
2103	020172	004737	022426					
2104	020176	004737	022316		1\$:	JSR	PC,SETBRI	SET THE BR1 BIT'
2105	020176	004737				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2106	020202	104414				100400		START AT ROM PC=0
2107	020204	100400				ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2108	020206	104414						

2109 020210 116777 114377!<400*5>
 2110 020212 004737 022364 JSR PC,ROMDAT :JUMP TO ROM PC OF 1777
 2111 020216 003776 3776 :RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
 2112 020220 020504 CMP R5,R4 :INDEX
 2113 020222 001401 BEQ 2\$:ARE NEW PC CONTENTS CORRECT?
 2114 020224 104006 HLT 6 :BR IF YES
 2115 020226 104401 SCOP1 :ERROR, CROM PC IS WRONG
 2116 020230 012737 020236 001220 2\$: MOV #3\$,LOCK :LOOP TO 1\$ IF SW09=1
 2117 020236 004737 022316 3\$: JSR PC,SETBR1 :NEW SCOP1
 2118 020242 104414 ROMCLK :SET THE BR1 BIT'
 2119 020244 100403 100403 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2120 020246 104414 ROMCLK :START AT ROM PC=3
 2121 020250 102400 100000!<400*5> :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2122 020252 004737 022364 JSR PC,ROMDAT :ROM PC OF 0
 2123 020256 000000 0 :RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
 2124 020260 020504 CMP R5,R4 :INDEX
 2125 020262 001401 BEQ 4\$:ARE NEW PC CONTENTS CORRECT?
 2126 020264 104006 HLT 6 :BR IF YES
 2127 020266 104401 SCOP1 :ERROR, CROM PC IS WRONG
 2128 020270 012737 020276 001220 4\$: MOV #5\$,LOCK :LOOP TO 3\$ IF SW09=1
 2129 020276 004737 022316 5\$: JSR PC,SETBR1 :NEW SCOP1
 2130 020302 104414 ROMCLK :SET THE BR1 BIT'
 2131 020304 100406 100406 :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2132 020306 104414 ROMCLK :START AT ROM PC=6
 2133 020310 106525 104125!<400*5> :NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2134 020312 004737 022364 JSR PC,ROMDAT :JUMP TO ROM PC OF 525
 2135 020316 001252 1252 :RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
 2136 020320 020504 CMP R5,R4 :INDEX
 2137 020322 001401 BEQ 6\$:ARE NEW ROM PC CONTENTS CORRECT?
 2138 020324 104006 HLT 6 :BR IF YES
 2139 020326 104401 SCOP1 :ERROR, CROM PC IS WRONG
 2140 020330 104400 SCOPE :LOOP TO 5\$ IF SW59=1
 2141 : :SCOPE THIS TEST
 2142 :
 2143 :
 2144 :
 2145 :***** TEST 12 *****
 2146 :*CROM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
 2147 :*SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION.
 2148 :*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
 2149 :*****
 2150 :
 2151 ; TEST 12
 2152 :-----
 2153 020332 012737 000012 001226 TST12: MOV #12,TSTNO :R1 CONTAINS BASE M8200-YC ADDRESS
 2154 020340 012737 020526 001216 MOV #TST13,NEXT :MASTER CLEAR M8200-YC
 2155 020346 012737 020372 001220 MOV #1\$,LOCK :IS IT CRAM?
 2156 :
 2157 020354 104412 MSTCLR :SKIP TEST IF YES
 2158 020356 032737 100000 001366 BIT #BIT15,STAT1 :CHECK FOR HI OR LO
 2159 020364 001057 BNE 6\$+2 :
 2160 020366 004737 022426 JSR PC,MAPCK :
 2161 020372 004737 022324 1\$: JSR PC,SETBR4 :SET THE BR4 BIT'

J05

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SEQ 0061

2163	020376	104414		ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2164	020400	100400		100400		START AT ROM PC=0
2165	020402	104414		ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2166	020404	117377		114377!<400*6>		JUMP TO ROM PC OF 1777
2167	020406	004737	022364	JSR PC,ROMDAT		RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2168	020412	003776		3776		INDEX
2169	020414	020504		CMP R5,R4		ARE NEW PC CONTENTS CORRECT?
2170	020416	001401		BEQ 2\$		BR IF YES
2171	020420	104006		HLT 6		ERROR, CROM PC IS WRONG
2172	020422	104401		SCOP1		LOOP TO 1\$ IF SW09=1
2173	020424	012737	020432 001220	MOV #3\$,LOCK		NEW SCOP1
2174	020432		3\$:	JSR PC,SETBR4		SET THE BR4 BIT'
2175	020432	004737	022324	ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2176	020436	104414		100403		START AT ROM PC=3
2177	020440	100403		ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2178	020442	104414		100000!<400*6>	JUMP TO	ROM PC OF 0
2179	020444	103000		JSR PC,ROMDAT		RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2180	020446	004737	022364	0		INDEX
2181	020452	000000		CMP R5,R4		ARE NEW PC CONTENTS CORRECT?
2182	020454	020504		BEQ 4\$		BR IF YES
2183	020456	001401		HLT 6		ERROR, CROM PC IS WRONG
2184	020460	104006		SCOP1		LOOP TO 3\$ IF SW09=1
2185	020462	104401		MOV #5\$,LOCK		NEW SCOP1
2186	020464	012737	020472 001220	JSR PC,SETBR4		SET THE BR4 BIT'
2187	020472		4\$: 5\$:	ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2188	020472	004737	022324	100406		START AT ROM PC=6
2189	020476	104414		ROMCLK		NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2190	020500	100406		104125!<400*6>	JUMP TO ROM PC OF 525	
2191	020502	104414		JSR PC,ROMDAT		RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2192	020504	107125		1252		INDEX
2193	020506	004737	022364	CMP R5,R4		ARE NEW ROM PC CONTENTS CORRECT?
2194	020512	001252		BEQ 6\$		BR IF YES
2195	020514	020504		HLT 6		ERROR, CROM PC IS WRONG
2196	020516	001401		SCOP1		LOOP TO 5\$ IF SW59=1
2197	020520	104006		SCOPE		SCOPE THIS TEST
2198	020522	104401				
2199	020524	104400				
2200						
2201						
2202						***** TEST 13 *****
2203						*CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
2204						*SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION.
2205						*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
2206						*****
2207						
2208						TEST 13
2209						-----
2210	020526	012737	000013 001226	TST13: MOV #13,TSTNO		
2211	020534	012737	020722 001216	MOV #TST14,NEXT		
2212	020542	012737	020566 001220	MOV #15,LOCK		
2213						R1 CONTAINS BASE M8200-YC ADDRESS
2214	020550	104412		MSTCLR		MASTER CLEAR M8200-YC
2215	020552	032737	100000 001366	BIT #BIT15,STAT1		IS IT CRAM?
2216	020560	001057		BNE 6\$+2		SKIP TEST IF YES

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SEQ 0062

2217	020562	004737	022426		JSR	PC,MAPCK	;CHECK FOR HI OR LO
2218	020566				JSR	PC,SETBR7	;SET THE BR7 BIT'
2219	020566	004737	022332		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2220	020572	104414			100400		START AT ROM PC=0
2221	020574	100400			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2222	020576	104414			114377!<400*7>		JUMP TO ROM PC OF 177?
2223	020600	117777			JSR	PC,ROMDAT	RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2224	020602	004737	022364		3776		INDEX
2225	020606	003776			CMP	R5,R4	ARE NEW PC CONTENTS CORRECT?
2226	020610	020504			BEQ	2\$	BR IF YES
2227	020612	001401			HLT	6	ERROR, CROM PC IS WRONG
2228	020614	104006			SCOP1		LOOP TO 1S IF SW09=1
2229	020616	104401			MOV	#3\$,LOCK	;NEW SCOP1
2230	020620	012737	020626	001220			
2231	020626				JSR	PC,SETBR7	;SET THE BR7 BIT'
2232	020626	004737	022332		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2233	020632	104414			100403		START AT ROM PC=3
2234	020634	100403			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2235	020636	104414			100000!<400*7>	JUMP TO	ROM PC OF 0
2236	020640	103400			JSR	PC,ROMDAT	RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2237	020642	004737	022364		0		INDEX
2238	020646	000000			CMP	R5,R4	ARE NEW PC CONTENTS CORRECT?
2239	020650	020504			BEQ	4\$	BR IF YES
2240	020652	001401			HLT	6	ERROR, CROM PC IS WRONG
2241	020654	104006			SCOP1		LOOP TO 3S IF SW09=1
2242	020656	104401			MOV	#5\$,LOCK	;NEW SCOP1
2243	020660	012737	020666	001220			
2244	020666	004737	022332		JSR	PC,SETBR7	;SET THE BR7 BIT'
2245	020672	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2246	020674	100406			100406		START AT ROM PC=6
2247	020676	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2248	020700	107525			104125!<400*7>	JUMP TO ROM PC OF 525	
2249	020702	004737	022364		JSR	PC,ROMDAT	RS=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2250	020706	001252			1252		INDEX
2251	020710	020504			CMP	R5,R4	ARE NEW ROM PC CONTENTS CORRECT?
2252	020712	001401			BEQ	6\$	BR IF YES
2253	020714	104006			HLT	6	ERROR, CROM PC IS WRONG
2254	020716	104401			SCOP1		LOOP TO 5S IF SW59=1
2255	020720	104400			SCOPE		;SCOPE THIS TEST
2256							
2257							
2258							
2259							***** TEST 14 *****
2260							*CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
2261							*CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION,
2262							*VERIFY THAT THE JUMP DID NOT OCCUR BY READING
2263							*THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
2264							*****
2265							
2266							
2267							
2268	020722	012737	000014	001226	TST14:	MOV	#14,TSTNO
2269	020730	012737	021116	001216		MOV	#T\$15,NEXT
2270	020736	012737	020762	001220		MOV	#1\$,LOCK

2271
 2272 020744 104412
 2273 020746 032737 100000 001366 MSTCLR
 2274 020754 001057 BNE #BIT15,STAT1
 2275 020756 004737 022426 JSR 6S+2
 2276 020762 004737 022272 JSR PC,MAPCK
 2277 020762 004737 022272 JSR PC,CLRALL
 2278 020766 104414 ROMCLK
 2279 020770 100400 100400
 2280 020772 104414 ROMCLK
 2281 020774 115377 114377!<400*2>
 2282 020776 004737 022364 JSR PC,ROMDAT
 2283 021002 000002 2
 2284 021004 020504 CMP R5,R4
 2285 021006 001401 BEQ 2S
 2286 021010 104006 HLT 6
 2287 021012 104401 SCOP1
 2288 021014 012737 021022 001220 MOV #3S,LOCK
 2289 021022 004737 022272 JSR PC,CLRALL
 2290 021026 104414 ROMCLK
 2292 021030 100403 100403
 2293 021032 104414 ROMCLK
 2294 021034 101000 100000!<400*2> :JUMP TO
 2295 021036 004737 022364 JSR PC,ROMDAT
 2296 021042 000010 10
 2297 021044 020504 CMP R5,R4
 2298 021046 001401 BEQ 4S
 2299 021050 104006 HLT 6
 2300 021052 104401 SCOP1
 2301 021054 012737 021062 001220 MOV #5S,LOCK
 2302 021062 004737 022272 JSR PC,CLRALL
 2303 021066 104414 ROMCLK
 2305 021070 100406 100406
 2306 021072 104414 ROMCLK
 2307 021074 105125 104125!<400*2>
 2308 021076 004737 022364 JSR PC,ROMDAT
 2309 021102 000016 16
 2310 021104 020504 CMP R5,R4
 2311 021106 001401 BEQ 6S
 2312 021110 104006 HLT 6
 2313 021112 104401 SCOP1
 2314 021114 104400 SCOPE
 2315
 2316
 2317 ;***** TEST 15 *****
 2318 ;CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
 2319 ;CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,
 2320 ;VERIFY THAT THE JUMP DID NOT OCCUR BY READING
 2321 ;THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
 2322 ;*****
 2323 ; TEST 15

2325 021116 012737 000015 001226 TST15: MOV #15,TSTNO
 2326 021124 012737 021312 001216 MOV #15,NEXT
 2327 021132 012737 021156 001220 MOV #15,LOCK
 2328
 2329
 2330 021140 104412 MSTCLR
 2331 021142 032737 100000 001366 BIT #BIT15,STAT1
 2332 021150 001057 BNE 65+2
 2333 021152 004737 JSR PC,MAPCK
 2334 021156 004737 15:
 2335 021158 004737 022272 TSR PC,CLRALL
 2336 021162 104414 ROMCLK PC,CLRALL
 2337 021164 100400 100400
 2338 021166 104414 ROMCLK
 2339 021170 115777 114377!<400*3>
 2340 021172 004737 022364 JSR PC,ROMDAT
 2341 021176 000002 2
 2342 021200 020504 CMP R5,R4
 2343 021202 001401 BEQ 25
 2344 021204 104006 HLT 6
 2345 021206 104401 SCOP1
 2346 021210 012737 021216 001220 25:
 2347 021216 004737 022272 35:
 2348 021216 004737 JSR PC,CLRALL
 2349 021222 104414 ROMCLK PC,CLRALL
 2350 021224 100403 100403
 2351 021226 104414 ROMCLK
 2352 021230 101400 100000!<400*3> ; JUMP TO
 2353 021232 004737 JSR PC,ROMDAT
 2354 021236 000010 10
 2355 021240 020504 CMP R5,R4
 2356 021242 001401 BEQ 45
 2357 021244 104006 HLT 6
 2358 021246 104401 SCOP1
 2359 021250 012737 021256 001220 45:
 2360 021256 004737 022272 55:
 2361 021256 004737 JSR PC,CLRALL
 2362 021262 104414 ROMCLK PC,CLRALL
 2363 021264 100406 100406
 2364 021266 104414 ROMCLK
 2365 021270 105525 104125!<400*3>
 2366 021272 004737 JSR PC,ROMDAT
 2367 021276 000016 16
 2368 021300 020504 CMP R5,R4
 2369 021302 001401 BEQ 65
 2370 021304 104006 HLT 6
 2371 021306 104401 SCOP1
 2372 021310 104400 SCOPE
 2373
 2374
 2375 ;***** TEST 16 *****
 2376 ;*CROM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
 2377 ;*CLEAR THE BRO BIT, PERFORM THE JUMP INSTRUCTION,
 2378 ;*VERIFY THAT THE JUMP DID NOT OCCUR BY READING

2379
 2380
 2381
 2382
 2383
 2384 021312 012737 000016 001226 TST16:
 2385 021320 012737 021506 001216
 2386 021326 012737 021352 001220
 2387
 2388 021334 104412
 2389 021336 032737 100000 001366
 2390 021344 001057
 2391 021346 004737 022426
 2392 021352 004737 022272
 2393 021356 104414 022364
 2394 021360 100400
 2395 021362 104414
 2396 021364 116377
 2397 021366 004737 021412 001220
 2398 021372 000002
 2399 021374 020504
 2400 021376 001401
 2401 021400 104006
 2402 021402 104401
 2403 021404 012737
 2404 021412 004737 022272
 2405 021416 104414
 2406 021420 100403
 2407 021422 104414
 2408 021424 102000
 2409 021426 004737 022364
 2410 021432 000010
 2411 021434 020504
 2412 021436 001401
 2413 021440 104006
 2414 021442 104401
 2415 021444 012737 021452 001220
 2416 021452 004737 022272
 2417 021456 104414
 2418 021460 100406
 2419 021462 104414
 2420 021464 106125
 2421 021466 004737 022364
 2422 021472 000016
 2423 021474 020504
 2424 021476 001401
 2425 021500 104006
 2426 021502 104401
 2427 021504 104400
 2428
 2429
 2430
 2431
 2432

;*THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
 ;*****
 ; TEST 16
 ;-----
 ;MOV #16,TSTNO
 ;MOV #TST17,NEXT
 ;MOV #1\$,LOCK
 ;MSTCLR
 ;BIT #BIT15,STAT1
 ;BNE 6\$+2
 ;JSR PC,MAPCK
 ;JSR PC,CLRALL
 ;ROMCLK 100400
 ;ROMCLK 114377!<400*4>
 ;JSR PC,ROMDAT
 ;2
 ;CMP R5,R4
 ;BEQ 2\$
 ;HLT 6
 ;SCOP1
 ;MOV #3\$,LOCK
 ;JSR PC,CLRALL
 ;ROMCLK 100403
 ;ROMCLK 100000!<400*4> :JUMP TO 0
 ;JSR PC,ROMDAT
 ;10
 ;CMP R5,R4
 ;BEQ 4\$
 ;HLT 6
 ;SCOP1
 ;MOV #5\$,LOCK
 ;JSR PC,CLRALL
 ;ROMCLK 100406
 ;ROMCLK 104125!<400*4>
 ;JSR PC,ROMDAT
 ;16
 ;CMP R5,R4
 ;BEQ 6\$
 ;HLT 6
 ;SCOP1
 ;SCOPE
 ;CLEAR ALL CONDITIONS
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;START AT ROM PC=0
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;JUMP TO ROM PC OF 1777
 ;R5=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 ;INDEX
 ;ARE NEW PC CONTENTS CORRECT?
 ;BR IF YES
 ;ERROR, CROM PC IS WRONG
 ;LOOP TO 1\$ IF SW09=1
 ;NEW SCOP1
 ;CLEAR ALL CONDITIONS
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;START AT ROM PC=3
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 ;INDEX
 ;ARE NEW PC CONTENTS CORRECT?
 ;BR IF YES
 ;ERROR, CROM PC IS WRONG
 ;LOOP TO 3\$ IF SW09=1
 ;NEW SCOP1
 ;CLEAR ALL CONDITIONS
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;START AT ROM PC=6
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;JUMP TO ROM PC OF 525
 ;RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 ;INDEX
 ;ARE NEW ROM PC CONTENTS CORRECT?
 ;BR IF YES
 ;ERROR, CROM PC IS WRONG
 ;LOOP TO 5\$ IF SW59=1
 ;SCOPE THIS TEST

2433
 2434
 2435
 2436
 2437
 2438
 2439
 2440
 2441 021506 012737 000017 001226 TST17:
 2442 021514 012737 021702 001216 MOV \$17,TSTNO
 2443 021522 012737 021546 001220 MOV \$TST20,NEXT
 2444 MOV \$1\$,LOCK
 2445
 2446 021530 104412 MSTCLR
 2447 021532 032737 100000 001366 BIT #BIT15,STAT1
 2448 021540 001057 BNE 6S+2
 2449 021542 004737 022426 JSR PC,MAPCK
 2450 021546 004737 022272 JSR PC,CLRALL
 2451 021552 104414 ROMCLK
 2452 021554 100400 100400
 2453 021556 104414 ROMCLK
 2454 021560 116777 114377!<400*5>
 2455 021562 004737 022364 JSR PC,ROMDAT
 2456 021566 000002 2
 2457 021570 020504 CMP R5,R4
 2458 021572 001401 BEQ 2S
 2459 021574 104006 HLT 6
 2460 021576 104401 SCOP1
 2461 021600 012737 021606 001220 2S: MOV #3S,LOCK
 2462 021606 004737 022272 3S: JSR PC,CLRALL
 2463 021612 104414 ROMCLK
 2464 021614 100403 100403
 2465 021616 104414 ROMCLK
 2466 021620 102400 100000!<400*5> JUMP TO
 2467 021622 004737 022364 JSR PC,ROMDAT
 2468 021626 000010 10
 2469 021630 020504 CMP R5,R4
 2470 021632 001401 BEQ 4S
 2471 021634 104006 HLT 6
 2472 021636 104401 SCOP1
 2473 021640 012737 021646 001220 4S: MOV #5S,LOCK
 2474 021646 004737 022272 5S: JSR PC,CLRALL
 2475 021652 104414 ROMCLK
 2476 021654 100406 100406
 2477 021656 104414 ROMCLK
 2478 021660 106525 104125!<400*5>
 2479 021662 004737 022364 JSR PC,ROMDAT
 2480 021666 000016 16
 2481 021670 020504 CMP R5,R4
 2482 021672 001401 BEQ 6S
 2483 021674 104006 HLT 6
 ; TEST 17
 ; **** TEST 17 ****
 ; CROM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
 ; CLEAR THE BR1 BIT. PERFORM THE JUMP INSTRUCTION,
 ; VERIFY THAT THE JUMP DID NOT OCCUR BY READING
 ; THE CONTENTS OF THE NEW ROM PC (IT SHOULD INCREMENT BY ONE).
 ; **** TEST 17 ****
 ; R1 CONTAINS BASE M8200-YC ADDRESS
 ; MASTER CLEAR M8200-YC
 ; IS IT CRAM?
 ; SKIP TEST IF YES
 ; CHECK FOR HI OR LO
 ; CLEAR ALL CONDITIONS
 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ; START AT ROM PC=0
 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ; JUMP TO ROM PC OF 1777
 ; RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 ; INDEX
 ; ARE NEW PC CONTENTS CORRECT?
 ; BR IF YES
 ; ERROR, CROM PC IS WRONG
 ; LOOP TO 1S IF SW09=1
 ; NEW SCOP1
 ; CLEAR ALL CONDITIONS
 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ; START AT ROM PC=3
 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ; ROM PC OF 0
 ; RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 ; INDEX
 ; ARE NEW PC CONTENTS CORRECT?
 ; BR IF YES
 ; ERROR, CROM PC IS WRONG
 ; LOOP TO 3S IF SW09=1
 ; NEW SCOP1
 ; CLEAR ALL CONDITIONS
 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ; START AT ROM PC=6
 ; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ; JUMP TO ROM PC OF 525
 ; RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 ; INDEX
 ; ARE NEW ROM PC CONTENTS CORRECT?
 ; BR IF YES
 ; ERROR, CROM PC IS WRONG

2487 021676 104401 6S: SCOP1 ;LOOP TO 5S IF SW59=1
 2488 021700 104400 SCOPE ;SCOPE THIS TEST

2489
 2490
 2491 ;***** TEST 20 *****
 2492 ;CROM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
 2493 ;CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
 2494 ;VERIFY THAT THE JUMP DID NOT OCCUR BY READING
 2495 ;THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
 2496 ;*****
 2497
 2498 ; TEST 20
 2499

2500 021702 012737 000020 001226	TST20:	MOV \$20,TSTNO	
2501 021710 012737 022076 001216		MOV \$TST21,NEXT	
2502 021716 012737 021742 001220		MOV \$1\$,LOCK	
2503			;R1 CONTAINS BASE M8200-YC ADDRESS
2504 021724 104412		MSTCLR	MASTER CLEAR M8200-YC
2505 021726 032737	100000 001366	BIT #BIT15,STAT1	IS IT CRAM?
2506 021734 001057		BNE 6S+2	SKIP TEST IF YES
2507 021736 004737	022426	JSR PC,MAPCK	CHECK FOR HI OR LO
2508 021742			
2509 021742 004737	022272	JSR PC,CLRALL	CLEAR ALL CONDITIONS
2510 021746 104414		ROMCLK	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2511 021750 100400		100400	START AT ROM PC=0
2512 021752 104414		ROMCLK	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2513 021754 117377		114377!<400*6>	JUMP TO ROM PC OF 1777
2514 021756 004737	022364	JSR PC,ROMDAT	RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
2515 021762 000002		2	INDEX
2516 021764 020504		CMP RS,R4	ARE NEW PC CONTENTS CORRECT?
2517 021766 001401		BEQ 2S	BR IF YES
2518 021770 104006		HLT 6	ERROR, CROM PC IS WRONG
2519 021772 104401		SCOP1	LOOP TO 1S IF SW09=1
2520 021774 012737	022002 001220	MOV #3\$,LOCK	NEW SCOP1
2521 022002 004737	022272	JSR PC,CLRALL	CLEAR ALL CONDITIONS
2522 022006 104414		ROMCLK	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2524 022010 100403		100403	START AT ROM PC=3
2525 022012 104414		ROMCLK	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2526 022014 103000		100000!<400*6>	JUMP TO ROM PC OF 0
2527 022016 004737	022364	JSR PC,ROMDAT	RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
2528 022022 000010		10	INDEX
2529 022024 020504		CMP RS,R4	ARE NEW PC CONTENTS CORRECT?
2530 022026 001401		BEQ 4S	BR IF YES
2531 022030 104006		HLT 6	ERROR, CROM PC IS WRONG
2532 022032 104401		SCOP1	LOOP TO 3S IF SW09=1
2533 022034 012737	022042 001220	MOV #5\$,LOCK	NEW SCOP1
2534 022042 004737	022272	JSR PC,CLRALL	CLEAR ALL CONDITIONS
2536 022046 104414		ROMCLK	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2537 022050 100406		100406	START AT ROM PC=6
2538 022052 104414		ROMCLK	NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2539 022054 107125		104125!<400*6>	JUMP TO ROM PC OF 525
2540 022056 004737	022364	JSR PC,ROMDAT	RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA

2541 022062 000016
 2542 022064 020504
 2543 022066 001401
 2544 022070 104006
 2545 022072 104401
 2546 022074 104400

6S:

16	CMP	R5,R4	: INDEX
	BEQ	6S	: ARE NEW ROM PC CONTENTS CORRECT?
	HLT	6	: BR IF YES
	SCOP1		: ERROR, CROM PC IS WRONG
	SCOPE		: LOOP TO 5S IF SW59=1
			: SCOPE THIS TEST

2547
 2548
 2549 :***** TEST 21 *****
 2550 :CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
 2551 :CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,
 2552 :VERIFY THAT THE JUMP DID NOT OCCUR BY READING
 2553 :THE CONTENTS OF THE NEW ROM PC (IT SHOULD INCREMENT BY ONE).
 2554 :*****
 2555
 2556 ; TEST 21
 2557
 2558 022076 012737 000021 001226 TST21:
 2559 022104 012737 003374 001216
 2560 022112 012737 022136 001220

MOV	#21	TSTNO	: R1 CONTAINS BASE M8200-YC ADDRESS
MOV	#	FOP NEXT	: MASTER CLEAR M8200-YC
MOV	#1\$	LOCK	: IS IT CRAM?

2561
 2562 022120 104412
 2563 022122 032737 100000 001366
 2564 022130 001057
 2565 022132 004737 022426

1S:

MSTCLR		#BIT15,STAT1	: SKIP TEST IF YES
BIT		6S+2	: CHECK FOR HI OR LO
BNE			
JSR		PC,MAPCK	

2566 022136 004737 022272
 2567 022142 104414
 2568 022144 100400
 2569 022144 100400
 2570 022146 104414
 2571 022150 117777
 2572 022152 004737 022364

JSR		PC,CLRALL	: CLEAR ALL CONDITIONS
ROMCLK		100400	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
ROMCLK		100400	: START AT ROM PC=0
114377!<400*7>			: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
JSR		PC,ROMDAT	: JUMP TO ROM PC OF 1777
2			: RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA

2573 022156 000002
 2574 022160 020504
 2575 022162 001401
 2576 022164 104006
 2577 022166 104401
 2578 022170 012737 022176 001220

CMP	R5,R4	: INDEX
BEQ	2S	: ARE NEW PC CONTENTS CORRECT?
HLT	6	: BR IF YES
SCOP1		: ERROR, CROM PC IS WRONG
MOV	#3\$,LOCK	: LOOP TO 1\$ IF SW09=1

2579 022176 004737 022272
 2580 022176 022272

JSR		PC,CLRALL	: NEW SCOP1
ROMCLK		100403	: CLEAR ALL CONDITIONS
ROMCLK		100403	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100000!<400*7>		JUMP TO ROM PC OF 0	: START AT ROM PC=3
JSR		PC,ROMDAT	: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
10			: RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA

2585 022212 004737 022364
 2586 022216 000010
 2587 022220 020504
 2588 022222 001401
 2589 022224 104006
 2590 022226 104401
 2591 022230 012737 022236 001220

CMP	R5,R4	: INDEX
BEQ	4S	: ARE NEW PC CONTENTS CORRECT?
HLT	6	: BR IF YES
SCOP1		: ERROR, CROM PC IS WRONG
MOV	#5\$,LOCK	: LOOP TO 3\$ IF SW09=1

2592 022236 004737 022272
 2593 022236 104414 4S:
 2594 022242 104414 5S:

JSR		PC,CLRALL	: NEW SCOP1
ROMCLK			: CLEAR ALL CONDITIONS
			: NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

2595 022244 100406
 2596 022246 104414
 2597 022250 107525
 2598 022252 004737 022364
 2599 022256 000016
 2600 022260 020504
 2601 022262 001401
 2602 022264 104006
 2603 022266 104401
 2604 022270 104400
 2605
 2606
 2607 ;SUBROUTINES
 2608 ;-----
 2609
 2610 022272 CLRALL:
 2611 ;THIS SUBROUTINE CLEARS THE C&Z BITS AND THE BR
 2612
 2613 022272 104414 ROMCLK
 2614 022274 000400 000400
 2615 022276 104414 ROMCLK
 2616 022300 063220 063220
 2617 022302 104414 ROMCLK
 2618 022304 060400 060400
 2619 022306 000207 RTS PC
 2620
 2621 022310 SETBRO:
 2622 ;THIS SUBROUTINE SETS BRO BIT
 2623
 2624 022310 104414 ROMCLK
 2625 022312 000401 000401
 2626 022314 000207 RTS PC
 2627
 2628
 2629
 2630 022316 SETBR1:
 2631 ;THIS SUBROUTINE SETS BR1 BIT
 2632
 2633 022316 104414 ROMCLK
 2634 022320 000402 000402
 2635 022322 000207 RTS PC
 2636
 2637
 2638 022324 SETBR4:
 2639 ;THIS SUBROUTINE SETS BR4 BIT
 2640
 2641 022324 104414 ROMCLK
 2642 022326 000420 000420
 2643 022330 000207 RTS PC
 2644
 2645
 2646 022332 SETBR7:
 2647 ;THIS SUBROUTINE SETS BR7 BIT
 2648

100406
 ROMCLK
 104125!<400*7>
 JSR PC,ROMDAT
 16
 CMP RS,R4
 BEQ 6S
 HLT 6
 SCOP1
 SCOPE

;START AT ROM PC=6
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;JUMP TO ROM PC OF 525
 ;RS=EXPECTED ROM DATA, R4=ACTUAL ROM DATA
 ;INDEX
 ;ARE NEW ROM PC CONTENTS CORRECT?
 ;BR IF YES
 ;ERROR, CROM PC IS WRONG
 ;LOOP TO 5S IF SW59=1
 ;SCOPE THIS TEST

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;BR+0
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;SP(0)+BR
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;BR+SP(0)+BR

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;BR+001

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;BR+002

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;BR+020

2649 022332 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2650 022334 000600 000600 ;BR+200
 2651 022336 000207 RTS PC

 2652
 2653
 2654 022340 SETC: ;THIS SUBROUTINE SETS THE C BIT

 2655 022340 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2658 022342 000777 000777 ;BR+377
 2659 022344 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2660 022346 063220 063220 ;SP(0)+BR
 2661 022350 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2662 022352 060400 060400 ;BR+SP(0)+BR
 2663 022354 000207 RTS PC

 2664
 2665
 2666 022356 SETZ: ;THIS SUBROUTINE SETS THE Z BIT

 2667 022356 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 2670 022360 000777 000777 ;BR+377
 2671 022362 000207 RTS PC

 2672
 2673
 2674 022364 ROMDAT: ;THIS SUBROUTINE LOADS R5 WITH EXPECTED ROM CONTENTS
 2675 ;AND LOADS R4 WITH ACTUAL ROM CONTENTS

 2678 022364 017600 000000 MOV A(SP),R0 ;INDEX FOR COMPARE
 2679 022370 062716 000002 ADD #2(SP) ;ADJUST STACK
 2680 022374 012711 002000 MOV #BIT10,(R1) ;SET ROM0
 2681 022400 016005 012374 MOV LOMAP(R0),RS ;PUT EXPECTED IN RS (LOSPEED)
 2682 022404 032737 000002 001372 BIT #BIT1,STAT3 ;LOW OR HIGH SPEED?
 2683 022412 001402 BEQ 1S ;BR IF LOW SPEED
 2684 022414 016005 012374 MOV HIMAP(R0),RS ;PUT EXPECTED IN RS (HISPEED)
 2685 022420 016104 000006 MOV 6(R1),R4 ;PUT "FOUND" IN R4
 2686 022424 000207 RTS PC ;RETURN

 2687
 2688 022426 MAPCK: ;THIS SUBROUTINE CHECKS THE STATUS TABLE AND LOADS
 2689 ;THE ROMMAP POINTER TO POINT TO EITHER THE HIGH OR
 2690 ;LOW SPEED MICRO-CODE.

 2693 022426 012737 012374 012372 MOV #LOMAP,ROMMAP ;LOAD POINTER TO LOW SPEED
 2694 022434 032737 000002 001372 BIT #BIT1,STAT3 ;CHECK STATUS TABLE
 2695 022442 001403 BEQ 1S ;BR IF LOW SPEED
 2696 022444 012737 012374 012372 MOV #HIMAP,ROMMAP ;LOAD POINTER TO HIGH SPEED
 2697 022452 000207 RTS PC ;RETURN

 2698
 2699 022454 020200 020040 020040 MESWCH: .ASCII <200># NOTE:#
 022467 200 047506 020122 .ASCII <200>#FOR THIS PROGRAM TO RUN PROPERLY, SWITCH#
 022540 033600 020054 043117 .ASCII <200>#7, OF THE VECTOR ADDRESS SWITCH PACK (E76),#
 022614 046600 051525 020124 .ASCII <200>#MUST BE ON. (M8200-YC BOARD)#<200>

022653	377	051103	046501	EM1:	.ASCIZ <377>/CRAM DATA ERROR/
022674	041777	040522	020115	EM2:	.ASCIZ <377>/CRAM DUAL ADDRESSING ERROR/
022730	041777	047522	020115	EM3:	.ASCIZ <377>/CROM DATA ERROR/
022751	377	052512	050115	EM4:	.ASCIZ <377>/JUMP ERROR/
022765	377	042117	020124	EM5:	.ASCIZ <377>/ODT ERROR IN IBUS* REG10/
023017	377	047511	020120	EM7:	.ASCIZ <377>/IOP MAR TEST/
023035	377	051102	051040	EM10:	.ASCIZ <377>/BR RIGHT SHIFT TEST/
023062	051377	041505	044505	EM11:	.ASCIZ <377>/RECEIVE DATA ERROR/
023106	043377	042522	020105	EM12:	.ASCIZ <377>/FREE RUNNING ERROR/
023132	041777	047117	051124	EM13:	.ASCIZ <377>/CONTROL OUT ERROR/
023155	377	054105	042520	DH1:	.ASCIZ <377>/EXPECTED FOUND ADDRESS/
023207	377	054105	042520	DH2:	.ASCIZ <377>/EXPECTED FOUND/
023230	020377	042523	032114	DH3:	.ASCIZ <377>/ SEL4 SEL6/
023251	377	042012	046122	ROM1:	.ASCII <377><12>/DRLPM-A SUPPORTS THE FOLLOWING CROM VERSIONS:/
023330	005377	050114	026501		.ASCIZ <377><12>/LPA- M8200-YC VERSION 4 MICRO CODE/<377><12>
.EVEN					
023400	000003			DT1:	3
023402	006	004			.BYTE 6,4
023404	001264				SAVR2
023406	006	004			.BYTE 6,4
023410	001270				SAVR4
023412	004	002			.BYTE 4,2
023414	001260				SAVRO
023416	000003				3
023420	006	004			.BYTE 6,4
023422	001272				SAVR5
023424	006	004			.BYTE 6,4
023426	001270				SAVR4
023430	004	002			.BYTE 4,2
023432	001264				SAVR2
023434	000003				3
023436	006	004			.BYTE 6,4
023440	001272				SAVR5
023442	006	004			.BYTE 6,4
023444	001270				SAVR4
023446	004	002			.BYTE 4,2
023450	001252				TEMP3
023452	000002				2
023454	003	007			.BYTE 3,7
023456	001272				SAVR5
023460	003	002			.BYTE 3,2
023462	001270				SAVR4
023464	000002				2
023466	006	004			.BYTE 6,4
023470	001272				SAVR5
023472	006	002			.BYTE 6,2
023474	001270				SAVR4
023476	000003				3
023500	003	010			.BYTE 3,10
023502	001272				SAVR5
023504	003	004			.BYTE 3,4

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 DRLPM.P11 SUBROUTINES

SEQ 0072

023506	001270		SAVR4	
023510	004	002	.BYTE	4,2
023512	001264		SAVR2	
023514	000003		3	
023516	003	007	.BYTE	3,7
023520	001272		SAVR5	
023522	003	004	.BYTE	3,4
023524	001270		SAVR4	
023526	006	002	.BYTE	6,2
023530	001252		TEMP3	
023532	000002		2	
023534	006	004	.BYTE	6,4
023536	001252		TEMP3	
023540	006	002	.BYTE	6,2
023542	001254		TEMP4	
 .ERRTAB:				
023544	000000		0	
023546	000000		0	
023550	000000		0	
023552	022653		EM1	
023554	023155		DH1	;HLT 1
023556	023400		DT1	
023560	022674		EM2	
023562	023155		DH1	;HLT 2
023564	023400		DT1	
023566	022653		EM1	
023570	023155		DH1	;HLT 3
023572	023416		DT2	
023574	022730		EM3	
023576	023155		DH1	;HLT 4
023600	023434		DT3	
023602	022751		EM4	
023604	023207		DH2	;HLT 5
023606	023452		DT4	
023610	022751		EM4	
023612	023207		DH2	;HLT 6
023614	023464		DT5	
023616	022765		EM5	
023620	023207		DH2	;HLT 7
023622	023452		DT4	
023624	000000		0	
023626	000000		0	
023630	000000		0	
023632	023017		EM7	
023634	023155		DH1	;HLT 11
023636	023476		DT7	
023640	023035		EM10	
023642	023207		DH2	;HLT 12
023644	023452		DT4	
023646	023062		EM11	
023650	023155		DH1	;HLT 13
023652	023514		DT10	
023654	023106		EM12	

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DRLPM.P11 SUBROUTINES

SEQ 0073

023656 000000 0 ;HLT 14
023660 000000 0
023662 023106 EM12
023664 023207 DH2 ;HLT 15
023666 023464 DT5
023670 023132 EM13
023672 023230 DH3 ;HLT 16
023674 023532 DT11

023676 000001 CORMAX:
.END

ADRCNT= 004403	AUDONE 003034	AUSTRT 002456	AUTO.S 010552
BINWRD 004724	BIT0 = 000001	BIT1 = 000002	BIT10 = 002000
BIT11 = 004000	BIT12 = 010000	BIT13 = 020000	BIT14 = 040000
BIT15 = 100000	BIT2 = 000004	BIT3 = 000010	BIT4 = 000020
BIT5 = 000040	BIT6 = 000100	BIT7 = 000200	BIT8 = 000400
BIT9 = 001000	BM 007075	BRLVL 012324	BRW 003740
BRX 003742	BUF1 ~ 012374	CHRCNT 004722	CKSWR 007646
CKSWR1 007726	CKSWR2 007740	CKSWR3 007744	CKSWR4 007750
CKSWR5 010054	CLKX 001242	CLRALL 022272	CNERR 007323
CNT.MA 001702	CNVRT = 104411	CONERR 007244	CONN 007135
CONTAB 003006	CONVRT= 104410	CORMAX 023676	CRAM 006627
CREAM 001320	CSR 006531	CSRMAP 010554	CYCLE 010120
DATABP 005226	DATACL= 104415	DATAHD 005214	DELAY = 104413
DEVADR 004400	DEVTAB 003020	DH1 023155	DH2 023207
DH3 023230	DISPLA 001200	DISPRE 000174	DMACTV 001306
DMCM 007344	DMCr00 001500	DMCR01 001510	DMCR02 001520
DMCR03 001530	DMCR04 001540	DMCR05 001550	DMCr06 001560
DMCr07 001570	DMCR10 001600	DMCR11 001610	DMCR12 001620
DMCR13 001630	DMCR14 001640	DMCr15 001650	DMCR16 001660
DMCR17 001670	DMCSR 001404	DMCSRH 001406	DMCTL 001410
DMNUM 001310	DMP04 001412	DMP06 001414	DMRLVL 001376
DMRVEC 001374	DMS100 001502	DMS101 001512	DMS102 001522
DMS103 001532	DMS104 001542	DMS105 001552	DMS106 001562
DMS107 001572	DMS110 001602	DMS111 001612	DMS112 001622
DMS113 001632	DMS114 001642	DMS115 001652	DMS116 001662
DMS117 001672	DMS200 001504	DMS201 001514	DMS202 001524
DMS203 001534	DMS204 001544	DMS205 001554	DMS206 001564
DMS207 001574	DMS210 001604	DMS211 001614	DMS212 001624
DMS213 001634	DMS214 001644	DMS215 001654	DMS216 001664
DMS217 001674	DMS300 001506	DMS301 001516	DMS302 001526
DMS303 001536	DMS304 001546	DMS305 001556	DMS306 001566
DMS307 001576	DMS310 001606	DMS311 001616	DMS312 001626
DMS313 001636	DMS314 001646	DMS315 001656	DMS316 001666
DMS317 001676	DMTLVL 001402	DMTVEC 001400	DM.END 001700
DM.MAP 001500	DONE 003744	DT1 023400	DT10 023514
DT11 023532	DT2 023416	DT3 023434	DT4 023452
DT5 023464	DT7 023476	EM1 022653	EM10 023035
EM11 023062	EM12 023106	EM13 023132	EM2 022674
EM3 022730	EM4 022751	EM5 022765	EM7 023017
ERCT00 001704	ERCT01 001710	ERCT02 001714	ERCT03 001720
ERCT04 001724	ERCT05 001730	ERCT06 001734	ERCT07 001740
ERCT10 001744	ERCT11 001750	ERCT12 001754	ERCT13 001760
ERCT14 001764	ERCT15 001770	ERCT16 001774	ERCT17 002000
ERR 002710	ERRCNT 001232	ERRFLG 001325	ERRMSG 005202
ERRPC 003000	ERTAB0 005332	EXIT = 000205	EXITER 005262
FLOAT 002546	FY 002576	HALTS 005232	HILIM 004376
HIMAP 012374	ICOUNT 001222	INBUF 007542	INCHAR 010060
INIFLG 001324	INSTER= 104404	INSTR = 104403	INSTR2 004176
INTTY 012340	KMCM 007361	LIMITS 004324	LINE 007037
LOBITS 004402	LOCK 001220	LOKFLG 001326	LOLIM 004374
LOMAP 012374	LPCNT 001224	LSTERR 001234	MAPCK 022426
MASKX 001244	MASTEK 006152	MCRLF 005702	MCSRX 006102
MDATA 007604	MEMLIM 001304	MEPASS 005743	MERRPC 006232
MERRX 006127	MERR2 005770	MERR3 006015	MESWCH 022454

MILK	001322	MLOCK	006053	MNEW	006154	MODU	006725
MPASSX	006116	MPFAIL	005705	MQM	005676	MR	005765
MRESET=	004000	MSTCLR=	104412	MTITLE	001000	MTSTM	006140
MTSTPC	006041	MVECX	006110	NEXT	001216	NOACT	007175
NODEV	002704	NUM	006466	OK	002656	ONE	001302
PACT00	001702	PACT01	001706	PACT02	001712	PACT03	001716
PACT04	001722	PACT05	001726	PACT06	001732	PACT07	001736
PACT10	001742	PACT11	001746	PACT12	001752	PACT13	001756
PACT14	001762	PACT15	001766	PACT16	001772	PACT17	001776
PARAM =	104405	PARAM1	004244	PARBIT=	040000	PARERR	004320
PASCNT	001230	PC	=%000007	PERFOR=	004537	PFTAB	005440
POPRO =	012600	POP1SP=	005726	POP2SP=	022626	PRI0	006570
PS	= 177776	PUSHRO=	010046	PUSH1S=	005746	PUSH2S=	024646
QV.FLG	001327	RESREG	005230	RESTAR	005360	RESTRRT	003544
RES05 =	104407	RETURN	001214	ROMCLK=	104414	ROMDAT	022364
ROMMAP	012372	ROM1	023251	RUN	001316	RO	=%000000
R1	=%000001	R2	=%000002	R3	=%000003	R4	=%000004
R5	=%000005	SAVACT	001312	SAVNUM	001314	SAVPC	001276
SAVRO	001260	SAVR1	001262	SAVR2	001264	SAVR3	001266
SAVR4	001270	SAVR5	001272	SAVSP	001274	SAV05 =	104406
SCOPE =	104400	SCOP1 =	104401	SETBRO	022310	SETBR1	022316
SETBR4	022324	SETBR7	022332	SETC	022340	SETZ	022356
SKIP	002642	SOFTSW	010112	SP	=%000006	SPACNT=	004723
SPEED	007371	STACK	= 001200	STAT	001240	STAT1	001366
STAT2	001370	STAT3	001372	STRTSW	001236	SV05	004412
SWFLG	010056	SWMES	007226	SWMES1	007236	SWR	001202
SWREG	000176	SW00	= 000001	SW01	= 000002	SW02	= 000004
SW03	= 000010	SW04	= 000020	SW05	= 000040	SW06	= 000100
SW07	= 000200	SW08	= 000400	SW09	= 001000	SW10	= 002000
SW11	= 004000	SW12	= 010000	SW13	= 020000	SW14	= 040000
SW15	= 100000	TEMP	001416	TEMP1	001246	TEMP2	001250
TEM _b 3	001252	TEMP4	001254	TEMPS	001256	TIMER	= 104416
TKCSR	001204	TKDBR	001206	TLAST	= 022076	TPCSR	001210
TPDBR	001212	TRPOK	004740	TSTNO	001226	TST1	016376
TST10	017742	TST11	020136	TST12	020332	TST13	020526
TST14	020722	TST15	021116	TST16	021312	TST17	021506
TST2	016470	TST20	021702	TST21	022076	TST3	016602
TST4	016776	TST5	017172	TST6	017352	TST7	017546
TTST	003622	TWOSYN=	010000	TYPDAT	005216	TYPE	= 104402
TYPMMSG	005116	VEC	006547	VECMAP	012062	WHICH	012054
WRDCNT	004720	WRKO.F	005204	XBX	005010	XCSR	003556
XERR	003600	XHEAD	006237	XLOC	003032	XPASS	003572
XSTATQ	007514	XTSTN	005340	XVEC	003564	ZERO	001300
SCRAP =	177777	SENDAD	003532	SN	= 000021	SS	= 000023
SY	= 000017	.BEGIN	003162	.CNVRT	004502	.CONVR	004476
.DATA.C	005562	.DELAY	005446	.EOP	003374	.ERRTA	023544
.HLT	004760	.INSTE	004164	.INSTR	004060	.INST1	004100
.MSG	004102	.MSTCL	005476	.PARAM	004204	.PFAIL	005346
.RES05	004444	.ROMCL	005514	.SAV05	004404	.SCOPE	003606
.SCOP1	003746	.START	002002	.TIMER	005626	.TRPSR	004726
.TRPTA	001330	.TYPE	003776	.	= 023676		

L06

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DRLPM.P11 SYMBOL TABLE

SEQ 0076

ERRORS DETECTED: 0

M06

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DRLPM.P11

SEQ 0077

*DRLPM,DRLPM/SOL=DRLPM.MAC,DRLPM
RUN-TIME: 12 15 0 SECONDS
CORE USED: 21K
EOF1DRLPMASEQ

00010000 780223

PDP10 411