

# LPA/KW11-K

DIAGNOSTIC TEST  
MD-11-DRLPG-A

EP-DRLPG-A-DL  
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FICHE 1 OF 2

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This image displays a grid of 100 small diagnostic test screens, arranged in 10 rows and 10 columns. Each screen shows a different set of data, including waveforms, numerical values, and status indicators. The screens are organized into several distinct sections:

- Top Row:** Displays various status and configuration parameters.
- Second Row:** Shows waveforms and data points, likely representing signal processing or timing.
- Third Row:** Contains numerical data and status indicators.
- Fourth Row:** Displays waveforms and data points, similar to the second row.
- Fifth Row:** Shows numerical data and status indicators.
- Sixth Row:** Displays waveforms and data points.
- Seventh Row:** Contains numerical data and status indicators.
- Eighth Row:** Shows waveforms and data points.
- Ninth Row:** Displays numerical data and status indicators.
- Tenth Row:** Shows waveforms and data points.

The overall layout is a systematic grid of diagnostic test results, likely used for troubleshooting or performance monitoring of the MD-11-DRLPG-A system.

# LPA/KW11-K

DIAGNOSTIC TEST  
MD-11-DRLPG-A

EP-DRLPG-A-DL  
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FICHE 2 OF 2

MAR 1978  
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MADE IN USA

This microfiche card contains a grid of frames. The leftmost column of frames contains text-based diagnostic data, including test results and error codes. The remaining frames in each row contain vertical bar patterns, which are likely graphical representations of test data or waveforms. The data is organized into approximately 12 rows and 6 columns of frames.

EOF1DRLPBASBQ411

00010000 780223  
\*\*\*\*\*

IdentPDP11/0400

7 HDR1DRLPGASEQ

00010000

780223  
SEQ 0001

Product Code: MAINDEC-11-DRLPG-A-D  
Product Name: LPA/KW11-K DIAGNOSTIC TEST  
Date Created: JANUARY 1978  
Maintainer: DIAGNOSTIC ENGINEERING

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1.0 ABSTRACT  
\*\*\*\*\*

This program allows the user to check out or debug the KW11K, DUAL REAL TIME CLOCK. The logic test is self contained and needs no external maintenance hardware or operator intervention.

Five special tests are included within this program to allow the user to check out and debug the external I/O signals. To run these tests a jumper wires is needed in order to loop output to an input.

THIS PROGRAM IS A MODIFIED VERSION OF "MD-11-DZKWK-A". IT WAS MODIFIED TO ENABLE THE OPERATOR TO CHECK OUT THE KW11K OPTION WHEN IT IS ON THE LPA11-KX I/O BUS. NO RECAPLING IS NEEDED. SOME TEST DONE IN THE ORIGINAL DIAGNOSTIC SUCH AS ARBRITRATION TEST, WERE DELETED AS THEY COULD NOT BE CHECKED. IF THIS DIAGNOSTIC DOESN'T FIND A SUSPECTED PROBLEM, YOU MAY HAVE TO RUN "MD-11-DZKWK-A". YOU SHOULD RUN "MD-11-DRLPA" BEFORE RUNNING THIS DIAGNOSTIC. PLEASE READ SECTION 10.

## 2.0 REQUIREMENTS \*\*\*\*\*

### 2.1 Equipment

1. PDP11 FAMILY COMPUTER with 16K of memory or more and I/O facilities (a switch register or TTY).
2. KW11K under test.
3. For external I/O signal tests a loopback wire (Jumper) is needed. Jumpers are 30 AWG jumper type 915.
4. LPA11-KX

### 2.2 Storage

This program occupies and uses only the lower 16K of memory.

### 3.0 LOADING PROCEDURE \*\*\*\*\*

#### 3.1 Method

Standards procedure for normal binary tapes should be followed.

1. Absolute loader must be in memory.
2. Place binary tape in reader.
3. Load address \*7500 (\* determined by location of loader).
4. Press "Start" (program will be loaded into memory).

The program can also be loaded by XXDP, ACT, or APT.

#### 3.2 Non-Standard Address, Vector, or Priority; or Use of Software Switch Register

This program is set to test a KW11K with a standard address, vector, and priority. If any of these are different on the KW11K you are testing, change the corresponding location in memory before starting this test.

<u>LOCATION</u>	<u>TAG</u>	<u>CURRENT CONTENTS</u>	<u>COMMENTS</u>
1254	\$BASE:	170404	::Base address of equipment :: under test
1250	\$VECT1:	000344	:: INTERRUPT Vector #1
1252	\$PRIOR:	000006	:: Bus priority - 1, #2
176	\$SWREG:	000000	:: Manual SWR.
	\$TPFLG:	.BYTE 0	:: "Terminal Available" :: Flag (Bit<0:7>=0=Yes)

#### NOTE

If no hardware Switch Register exists, you may set any bit in "SWREG" as you would have set it in the SWR.

#### 4.0 STARTING PROCEDURE \*\*\*\*\*

##### 4.1 Control Switch Settings

Starting at memory locations 200, 204, 210, 214, 220, 224, or 230 set all switches as desired. See Section 5.1.

##### 4.2 Starting Addresses

200 Start address for logic test.  
204 Restart address for logic test.  
210 Start address for "STP2 OUT", "SCHMITT TRIG 1" tests.  
214 Start address for "STP1 OUT", "SCHMITT TRIG 2" tests.  
220 Start address for "SCHMITT TRIG 3 IN", "ST3 OUT" tests.  
224 Starting address for "A EVENT OUT" test.  
230 Starting address for "B EVENT OUT" test.

##### 4.3 Program AND/OR Operator Action

1. Load program into core.
2. Set switch register to starting address.
3. Load address.
4. Set switches to desired settings - see section 5.1.
5. IF starting a special I/O signal test:  
MAKE WIRE LOOP CONNECTION.
6. Press Start.



## 5.0 OPERATING PROCEDURE

\*\*\*\*\*

## 5.1 Switch Register Function

## Switch use

-----

```

15 Halt on error
14 Loop on test
13 Inhibit error timeout (all tests)
13 Inhibit "*" timeout (special I/O signal tests)
11 Inhibit iterations (short pass)
10 Bell on error
9 Loop on error
8 Loop on test in SWR <7:0>

```

## 5.2 Scope Loops

If an error occurs and the user wishes to scope the error, he (or she) should set SW15=1 to halt on error, then when the program halts on error, SW15=0, set SW14=1. To loop on current test, set SW13=1 to inhibit error printout, and press continue on the CPU's console.

## NOTE

For each test in the listing, you will find a test description. In each description a probable SYNC Point is listed. These Points are listed AS A GUIDE in order for you to SYNC your scope to the Signals Being generated.

## 5.3 Program AND/OR Operator Action

## 5.3.1 Logic Test

The first pass through the program will be made with iterations inhibited. Successive passes will enable iterations if SW11=0. "END PASS" is printed out at the end of a pass.

If not inhibited by APT, the program will look for more KW11Ks to exercise, one pass will exercise all KW11Ks.

## 5.3.2 Special I/O Signal Tests

There are no "Short Passes". Each pass will iterate 65,324 times. A "\*" is typed at the end of a pass unless SW13=1.

## 6.0 ERRORS \*\*\*\*\*

### 6.1 Error Printout

Printout varies with the error detected. The error PC typed out is the actual location of the error call.

A halt at location "STYPE"+10 when running with no terminal indicates an error has occurred. To find out the number of the error, examine location "STSTNM". This is the item number of the error. To find out what the error typout would have been GOTO to the error pointer table beginning at location "SERRTB".

#### 6.1.1 Example

If we examined location "STSTNM" and found a 5 (101) we go to location "SERRTB" and look through the error pointer table until we found item 5. The information would look like:

;ITEM 5

```

EMS           ;CLOCK B SR DATA ERROR
DHS           ;ERRPC BSR WAS S/B
DTS           ;SERRPC,BSR,$BDDAT,$GDDAT
DFD           ;ALL NUMBERS ARE IN OCTAL FORM

```

To find out the information specified by DTS (SERRPC,BSR,\$GDDAT,\$BDDAT) follow these steps:

1. Look up the address of the label (i.e., SERRPC) in the symbol table which follows the listing.
2. Put this address in the witch register and depress the load address switch on the processor's console.
3. Now depress the Examine switch.
4. The data displayed in the data lights is the information that would have been printed for this label if you had a input/output terminal.

### 6.2 Non-Standard Error HALTS

A HALT MAY OCCUR IF THE PROGRAM DETECTS AN LPA11-KX ERROR. CHECK THE COMMENTS IN THE LISTING OPPOSITE THE PC HALT.

7.0 RESTRICTIONS  
\*\*\*\*\*

## 7.1

Jumper W2 must be installed if not jumpered on module.

## 7.2

Logic Test must be run before any special I/O Signal Test.

8.0 MISCELLANEOUS  
\*\*\*\*\*

## 8.1

After a power failure occurs, program execution will continue at the point where the power failure occurred after the program types "POWER".

## 8.2

This program is chainable under XXDP, ACT, or APT.

## 8.3 Execution Time

## 8.3.1 Logic Test

90 SECONDS iterations inhibited - no errors.

375 SECONDS with iterations - no errors.

## 8.3.2 Special I/O Signal Tests

1.0 Minutes No errors, SW13=0.

Execution times are approximate, as the various PDP-11 CPU's have varied instruction execution times.  
Times quoted were taken from a run on a PDP-11/34.

## 8.4 USER LINK TO I/O DEVICE

A SPECIAL USER LINK HAS BEEN PROVIDED IN ORDER FOR THE

OPERATOR TO EXAMINE OR MODIFY LOCATIONS ON THE LPA11-KX  
I/O BUS. (NOTE: THIS CANNOT BE DONE DIRECTLY.)

## PROCEDURE:

- 1) START THE PROCESSOR AT LOCATION SUTK:
- 2) THE DIALOG TO EXAMINE A LOCATION IS AS FOLLOWS:

```
E OR D      "E"  
DEVICE ADDR= "OCTAL ADDR"  
XXXXXX
```

WHERE XXXXXX IS THE CONTENTS OF THE SPECIFIED LOC.

- 3) THE DIALOG TO MODIFY A LOCATION IS AS FOLLOWS:

```
E OR D      "D"  
DATA=      "DATA TO BE DEPOSITED"
```

- 4) THE PROGRAM WILL STAY IN THIS LOOP UNTIL THE OPERATOR IS FINISHED. AT THIS TIME THE PROCESSOR SHOULD BE HALTED.

NOTE: THE OPERATORS RESPONSE IS ENCLOSED IN QUOTES.

## 9.0 PROGRAM DESCRIPTION

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### 9.1 Logic Tests

A complete description of each test is included withing the listing before each test.

### 9.2 Special External I/O Signal Tests

#### 9.2.1 LS210 "STP2 OUT" to "SCHMITT RIG 1 IN" Tests

This is a special section devoted for testing and providing scope loop capabilities for "STP2 OUT" L and "SCHMITT TRIG 1" IN.

When you load and start at location 210, program control is transferred here. "STP2 OUT" L pulses are generated by "LO STAT A HI" H + "BD10" H (Main. STP2).

Pin V ("STP2 OUT") is wired to pin LL (SCHMITT TRIG1) for this test. "STP2 OUT" pulses are received as "SCHMITT TRIG 1" pulses which set clock A's status register bit 15. If an error is detected, normal error reporting technique, and error switch register options are used. An "\*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins V and LL of J1 together.

Logic test (L + S 200) should be run first.

#### 9.2.2 LS214 "STP1 OUT" to "SCHMITT RIG 2" H Tests

This is a special test section devoted for testing and providing scope loop capabilities for "STP2 OUT" and "SCHMITT TRIG2" IN.

When you load and start at location 214, program control is transferred here. "STP1 OUT" L pulses are generated by "LD STAT A HI" + "BD12" H (mIn S ). Pin DD ("STP1 OUT") is wired to pin BB ("SCHMITT TRIG 2") for this test. "STP1 OUT" pulses are received as "SCHMITT RIG 2" pulses which will clear clock A's count register if mode 3 is selected. If an error is detected, normal error reporting technique, and error switch register options are used. An "\*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins DD and BB of J1 together.

Logic tests (L + S at 200) should be run first.

## 9.2.3 LS220 "SCHMITT TRIG 3" in, "ST3 OUT" Tests

This is a special section devoted for testing and providing scope LOOPS CAPABILITIES FOR "SCHMITT TRIG 3" AND "ST3 OUT".

When you load and start at location 220, program control is transferred here. "STP2" pulses are generated by "LD STAT A H," + "BD10" H (main STP2). Pin V ("STP2 OUT") is wired to pin T ("SCHMITT RIG 3"). "SCHMITT TRIG 3" pulses give us "ST3 OUT" pulses. Pin L ("ST3 OUT") is wired to pin LL ("SCHMITT RIG1"), and "SCHMITT RIG 1" will set clock A's status register bit 15.

If an error is detected, normal error reporting technique, and error switch register options are used. An "\*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins V to T of J1 together, as well as pins L to LL of J1 together.

Tests LS210 and LS214 should be run first.

## 9.2.4 LS224 "A EVENT OUT" Test

This is a special section devoted for testing and providing scope loop capabilities for "A EVENT OUT".

When you load and start at location 224, program control is transferred here. "A EVENT OUT" pulses are generated by clock A overflows. Pin VV ("A EVENT OUT") is wired to pin LL ("SCHMITT TRIG 1"). "SCHMITT TRIG 1" pulses will set clock A's CSR bit 15. If an error is detected, normal error reporting technique, and error switch register options are used. An "\*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins VV and LL of J1 together.

Test LS210 should be run first.

## 9.2.5 LS230 "B EVENT OUT" Test

This is a special section devoted for testing and providing scope loop capabilities for "B EVENT OUT".

When you load and start at location 230, program control is transferred here. "B EVENT OUT" pulses are generated by clock B overflows. Pin TT ("B EVENT OUT") is wired to pin LL ("SCHMITT TRIG 1"). "SCHMITT TRIG 1" pulses will set clock A's CSR bit 15. And error switch register options are used. An "\*" is typed after each 65,324 loops through the test. SW13=1 will inhibit this feature.

You must wire pins TT and LL of J1 together.

Test LS210 should be run first.

## 10.0 LPA11 (SYSTEM) DIAGNOSTIC SUMMARY

DIAGNOSTICS FOR THE LPA11 ARE WRITTEN AT THREE LEVELS: (1) TOTAL PDP-11 SYSTEM, (2) LPA11 SYSTEM; AND, (3) LPA11 OPTIONS.

LEVEL 1 IS DESIGNED TO ISOLATE A FAILURE TO THE LPA11 SYSTEM. ALL OPTIONS ON THE PDP-11 ARE EXERCISED.

LEVEL 2 DIAGNOSTICS ISOLATE A FAILURE TO THE INDIVIDUAL OPTION WITHIN THE LPA11. THE LEVEL 2 DIAGNOSTIC IS MD-11-DRLPA. WHEN THE USER RUNS DRLPA HE CAN GENERALLY TELL WHICH OPTION DIAGNOSTIC (LEVEL 3) TO RUN NEXT. MB254 AND MB200-YC ERRORS MAY "LOOK" ALIKE AND DRLPA MAY NOT BE ABLE TO DISTINGUISH BETWEEN THEM. ARBITRATION ERRORS WILL NOT BE DETECTED BY THIS DIAGNOSTIC.

LEVEL THREE DIAGNOSTICS AID IN DETERMINING IF THE ERROR WAS IN FACT ON THE OPTION THE DRLPA SPECIFIED. THE USER MAY "LOOP" ON THE ERROR. WITHIN LEVEL THREE, THERE ARE TWO GROUPS OF DIAGNOSTICS. THE FIRST GROUP REQUIRES NO "EXTRA" WORK BY THE USER IN ORDER TO RUN. GROUP "A" DIAGNOSTICS DO NOT CHECK ARBITRATION, AND REQUIRE EXTRA TIME FOR EXECUTION. THE SECOND GROUP (GROUP "B") REQUIRES THAT THE USER RECONFIGURE THE PDP-11 SYSTEM. THIS RECONFIGURATION INVOLVES CABLING THE UNIBUS TO THE LPA'S I/O BUS.

THE DIAGNOSTIC FOR THE MB254 FALLS INTO THE GROUP "B" CATAGORY.

## THE LPA11-KX DIAGNOSTIC KIT WILL INCLUDE:

<u>OPTION</u>	<u>GROUP</u>	<u>DIAG. #</u>	<u>DIAG. TITLE</u>
LPA11-KX	LEVEL 2	MD-11-DRLPA	LPA11-K SYSTEM DIAG.
M8254	"B"	MD-11-DRMBA	M8254 (JPBM) DIAG.
AA11-K	A	MD-11-DRLPB	AA11-K DIAG.
	B	MD-11-DZAAC	AA11-K DIAG.
AR11	A	MD-11-DRLPC	LPA/AR11 DIAG. #1
	A	MD-11-DRLPD	LPA/AR11 DIAG. #2
	A	MD-11-DRLPE	LPA/AR11 DIAG. #3
	B	MD-11-DZARA	AR11 DIAG. #1
	B	MD-11-DZARB	AR11 DIAG. #2
	B	MD-11-DZARC	AR11 DIAG. #3
DR11-K	A	MD-11-DRLPF	LPA/DR11-K DIAG.
	B	MD-11-DZDRG	DR11-K DIAG.
KW11-K	A	MD-11-DRLPG	LPA/KW11-K DIAG.
	B	MD-11-DZKWK	KW11-K DIAG.
LPS11	A	MD-11-DRLPH	LPA/LPS11 DIAG. #1
	A	MD-11-DRLPI	LPA/LPS11 DIAG. #2
	A	MD-11-DRLPJ	LPA/LPS11 DIAG. #3
	B	MD-11-DZLPC	LPS11 DIAG. #1
	B	MD-11-DZLPD	LPS11 DIAG. #2
	B	MD-11-DZLPI	LPS11 DIAG. #3
AD11-K	A	MD-11-DRLPK	LPA/AD11-K DIAG.
	B	MD-11-DZADL	AD11-K DIAG.
M8200-YC	B	MD-11-DZLPL	LPA/M8200-YC BASIC MICRO-CPU R/W TEST
	B	MD-11-DZLPM	LPA/M8200-YC JMP+ROM READ TEST



81	OPERATIONAL SWITCH SETTINGS
92	TRAP CATCHER
111	BASIC DEFINITIONS
234	ACT11 HOOKS
245	APT PARAMETER BLOCK
268	COMMON TAGS
316	APT MAILBOX-ETABLE
404	ERROR POINTER TABLE
630	PROGRAM START
633	INITIALIZE THE COMMON TAGS
735	*
736	* PHASE 1 CLOCKS A+B BASIC LOGIC TESTS.
737	*
740	T1 *TEST THE ADDRESSABILITY OF CLOCK ADDRESS
774	T2 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO
827	T3 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN TO A ZERO
867	T4 *TEST THAT CLOCK A'S STATUS CAN BE WRITTEN AND READ
916	T5 *TEST THAT CLOCK B'S STATUS REGISTER CAN BE WRITE/READ
955	T6 *TEST THAT CLOCK B'S BUFFER REGISTER CAN BE WRITE/READ
993	T7 *TEST THAT CLOCK A STATUS REGISTER BIT 15 CAN BE SET AND CLEARED
1049	T10 *TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED
1105	T11 *TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED
1161	T12 *TEST THAT CLOCK A STATUS REGISTER BIT 9 CAN BE SET AND CLEARED
1217	T13 *TEST THAT CLOCK A STATUS REGISTER BIT 8 CAN BE SET AND CLEARED
1273	T14 *TEST THAT CLOCK A STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
1329	T15 *TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
1385	T16 *TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
1441	T17 *TEST THAT CLOCK A STATUS REGISTER BIT 4 CAN BE SET AND CLEARED
1497	T20 *TEST THAT CLOCK A STATUS REGISTER BIT 2 CAN BE SET AND CLEARED
1553	T21 *TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
1609	T22 *TEST THAT CLOCK A STATUS REGISTER BIT 0 CAN BE SET AND CLEARED
1665	T23 *TEST THAT CLOCK A BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
1721	T24 *TEST THAT CLOCK A BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
1777	T25 *TEST THAT CLOCK A BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
1833	T26 *TEST THAT CLOCK A BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
1889	T27 *TEST THAT CLOCK A BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
1945	T30 *TEST THAT CLOCK A BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
2001	T31 *TEST THAT CLOCK A BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
2057	T32 *TEST THAT CLOCK A BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
2113	T33 *TEST THAT CLOCK A BUFFER REGISTER BIT 8 CAN BE SET AND CLEARED
2169	T34 *TEST THAT CLOCK A BUFFER REGISTER BIT 9 CAN BE SET AND CLEARED
2225	T35 *TEST THAT CLOCK A BUFFER REGISTER BIT 10 CAN BE SET AND CLEARED
2281	T36 *TEST THAT CLOCK A BUFFER REGISTER BIT 11 CAN BE SET AND CLEARED
2337	T37 *TEST THAT CLOCK A BUFFER REGISTER BIT 12 CAN BE SET AND CLEARED
2393	T40 *TEST THAT CLOCK A BUFFER REGISTER BIT 13 CAN BE SET AND CLEARED
2449	T41 *TEST THAT CLOCK A BUFFER REGISTER BIT 14 CAN BE SET AND CLEARED
2505	T42 *TEST THAT CLOCK A BUFFER REGISTER BIT 15 CAN BE SET AND CLEARED
2563	T43 *TEST THAT CLOCK B STATUS REGISTER BIT 11 CAN BE SET AND CLEARED
2620	T44 *TEST THAT CLOCK B STATUS REGISTER BIT 7 CAN BE SET AND CLEARED
2677	T45 *TEST THAT CLOCK B STATUS REGISTER BIT 6 CAN BE SET AND CLEARED
2734	T46 *TEST THAT CLOCK B STATUS REGISTER BIT 5 CAN BE SET AND CLEARED
2791	T47 *TEST THAT CLOCK B STATUS REGISTER BIT 4 CAN BE SET AND CLEARED
2848	T50 *TEST THAT CLOCK B STATUS REGISTER BIT 3 CAN BE SET AND CLEARED
2905	T51 *TEST THAT CLOCK B STATUS REGISTER BIT 2 CAN BE SET AND CLEARED

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2962	T52	*TEST THAT CLOCK B STATUS REGISTER BIT 1 CAN BE SET AND CLEARED
3019	T53	*TEST THAT CLOCK B STATUS REGISTER BIT 0 CAN BE SET AND CLEARED
3075	T54	*TEST THAT CLOCK B BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED
3131	T55	*TEST THAT CLOCK B BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED
3187	T56	*TEST THAT CLOCK B BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED
3243	T57	*TEST THAT CLOCK B BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED
3299	T60	*TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED
3355	T61	*TEST THAT CLOCK B BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED
3411	T62	*TEST THAT CLOCK B BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED
3467	T63	*TEST THAT CLOCK B BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED
3522	*	
3523	*	* PHASE 2 ADVANCED BASIC LOGIC TESTS
3524	*	
3527	T64	*TEST THAT CLOCK A'S COUNT REGISTER IS CLEAR
3573	T65	*TEST CLOCK A'S COUNT REGISTER WITH 125252 PATTERN
3624	T66	*TEST CLOCK A'S COUNT REGISTER WITH 052525 PATTERN
3676	T67	*TEST THAT CLOCK B'S COUNT REGISTER IS CLEAR
3723	T70	*TEST CLOCK B'S COUNT REGISTER WITH 125 PATTERN
3774	T71	*TEST CLOCK B'S COUNT REGISTER WITH 252 PATTERN
3826	T72	*TEST THE SETTING OF MAINTENANCE STP1 IN CLOCK A BIT 15 TO SET
3869	T73	*TEST THAT BIT00 IN CLOCK A STATUS REG. WILL SET WHEN BIT13 AND MAIN. STP1
3916	T74	*TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST
3976	T75	*TEST THE ABILITY OF CLOCK A TO COUNT FROM ZERO TO OVERFLOW USING M STP1'S
4057	*	
4058	*	* PHASE 3 CLOCK A COUNT FUNCTION TESTS
4059	*	
4062	T76	*TEST THAT CLOCK A OVERFLOW WILL OCCUR
4131	T77	*TEST IN CLOCK A THAT OVERFLOW IN MODE 0 CAUSE CLEARING OF "ENB CNTR" F/F
4210	T100	*TEST THE ABILITY OF CLOCK A TO COUNT AT 1MHZ RATE PART 1
4264	T101	*TEST THE ABILITY OF CLOCK A TO COUNT AT 100KHZ RATE PART 1
4318	T102	*TEST THE ABILITY OF CLOCK A TO COUNT AT 10KHZ RATE PART 1
4372	T103	*TEST THE ABILITY OF CLOCK A TO COUNT AT 1KHZ RATE PART 1
4426	T104	*TEST THE ABILITY OF CLOCK A TO COUNT AT 100HZ RATE PART 1
4480	T105	*TEST THE ABILITY OF CLOCK A TO COUNT AT LINE-FREQ RATE PART 1
4534	T106	*TEST THAT CLOCK A DOESN'T COUNT WHEN NO RATE IS SELECTED
4591	T107	*TEST THAT CLOCK A'S COUNT REG ISN'T LOADED WHEN CLOCK A IS ENABLED
4648	T110	*TEST THAT CLOCK A IN MODE 1 DOES NOT CLEAR ENABLE ON OVERFLOW
4700	T111	*TEST THAT A CLOCK A "BUFFER TO COUNT REG" DOESN'T TAKE PLACE ON A MODE 2 OVERFLOW
4765	T112	*TEST THAT CLOCK A MODE 2 + MAINTENANCE ST2 SET MODE FLG
4820	T113	*TEST THAT PATTERN 052525 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
4890	T114	*TEST THAT PATTERN 125252 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS
4962	T115	*TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 1 WHEN STP2 IS GENERATED
5011	T116	*TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 2 WHEN STP2 IS GENERATED
5061	T117	*TEST THAT MODE 3 + "STP2" CLEARS A'S COUNT REGISTER.
5111	T120	*TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER
5220	T121	*TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED
5278	*	
5279	*	* PHASE 4 CLOCK B COUNT FUNCTION TESTS
5280	*	
5283	T122	*TEST THAT CLOCK B WILL COUNT ONCE FIRST CLOCK B COUNT
5353	T123	*TEST THE ABILITY IF CLOCK B TO COUNT FROM ZERO TO OVERFLOW
5441	T124	*TEST THAT CLOCK B CAN GENERATE AN OVERFLOW
5519	T125	*TEST THE INIT. ABILITY OF CLOCK B'S COUNT REG.
5565	T126	*TEST THAT CLOCK B DOESN'T COUNT WHEN NO RATE IS SELECTED

5613	T127	*TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1
5671	T130	*TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1
5729	T131	*TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1
5787	T132	*TEST THE ABILITY OF CLOCK B TO COUNT AT 1KHZ PART 1
5845	T133	*TEST THE ABILITY OF CLOCK B TO COUNT AT 100HZ PART 1
5903	T134	*TEST THE ABILITY OF CLOCK B TO COUNT AT LINE-FREQ PART 1
5961	T135	*TEST THE "FEED B TO A" 24 BIT COUNTER FEATURE OF CLOCKS A + B
6038	*	
6039	*	* PHASE 6 CLOCK A+B ADVANCE TESTING
6040	*	
6044	T136	*TEST THAT THE TRAILING EDGE OF STP1 WILL INCR. COUNTER
6111	T137	*TEST CLOCK A'S 100KHZ DIVIDER
6223	T140	*TEST CLOCK A'S 10KHZ DIVIDER
6335	T141	*TEST CLOCK A'S 1KHZ DIVIDER
6447	T142	*TEST CLOCK A'S 100HZ DIVIDER
6560	T143	*TEST CLOCK B'S 100KHZ DIVIDER
6675	T144	*TEST CLOCK B'S 10KHZ DIVIDER
6790	T145	*TEST CLOCK B'S 1KHZ DIVIDER
6905	T146	*TEST CLOCK B'S 100HZ DIVIDER
7021		
7023		END OF PASS ROUTINE
7059	*	
7060	*	* SPECIAL I/O SIGNAL TESTS
7061	*	
7065	*	* "STP2 OUT" TO "SCHMITT TRIG 1 IN" TESTS
7161	.*	* "STP1 OUT" TO "SCHMITT TRIG 2" H TESTS
7263	*	* "SCHMITT TRIG 3" IN, "ST3 OUT" TESTS
7360	*	* "A EVENT OUT" TEST
7462	*	* "B EVENT OUT" TEST
7615		
7616		*SYSMAC ROUTINES
7617		
7619		BINARY TO OCTAL (ASCII) AND TYPE
7696		ERROR HANDLER ROUTINE
7746		ERROR MESSAGE TIMEOUT ROUTINE
7793		CONVERT BINARY TO DECIMAL AND TYPE ROUTINE
7860		SCOPE HANDLER ROUTINE
7925		READ AN OCTAL NUMBER FROM THE TTY
7963		TTY INPUT ROUTINE
8102		TYPE ROUTINE
8181		APT COMMUNICATIONS ROUTINE
8238		POWER DOWN AND UP ROUTINES
8281		TRAP DECODER
8304		TRAP TABLE

.REM I

LPA.MAC

WELCOME, THIS DIAGNOSTIC IS ONE IN A SERIES OF DIAGNOSTIC  
DESIGNED IN ORDER TO AID YOU IN TESTING THE LPA-11XX OPTION.  
I HOPE THAT YOU HAVE READ THE DOCUMENTATION SECTION OF THIS  
DIAGNOSTIC. IF YOU HAVE, YOU KNOW ABOUT ALL OF THE DIAGNOSTICS  
THAT ARE AVAILABLE FOR TESTING THE LPA SYSTEM.

GOOD LUCK !

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.GLOBL DRLPX2

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83

.REM !

THIS IS A LIST OF TESTS DELETED FROM THIS DIAGNOSTIC.  
THESE TEST COULD NOT BE DONE THROUGH THE LPA-11.

TEST THE LOW BYTE OPERATION OF CLOCK A'S STATUS REGISTER  
TEST THE HIGH BYTE OPERATION OF A'S STATUS REGISTER  
TEST THE LOW BYTE OPERATION OF B'S STATUS REGISTER  
TEST THE HIGH BYTE OPERATION OF B'S STATUS REGISTER  
TEST THAT INIT CLEARS STATUS REGISTER A  
TEST THAT INIT CLEARS BUFFER REGISTER A  
TEST THAT INIT CLEARS STATUS REGISTER B  
TEST THAT INIT CLEARS BUFFER REGISTER B  
TEST THAT A'S COUNT REGISTER IS CLEARED BY INIT  
TEST THAT CLOCK A WILL INTR. AND TO THE RIGHT VECTOR  
TEST THAT CLOCK A WILL INTR. WHEN CPU PSW = CLK INTR LEV -1  
TEST THAT CLOCK A WILL NOT INTR. WHEN CPU PSW = CLK INTR LEVEL  
TEST THAT STI WILL CAUSE CLOCK A TO INTER.  
TEST THAT CLOCK A OVERFLOW WILL CAUSE AN INTR.  
TEST THAT A CLOCK A COUNTER BUFFER WILL CAUSES AN INTR.  
TEST THAT CLOCK B WILL INTR. AND TO THE RIGHT VECTOR  
TEST THAT CLOCK B WILL INTR. WHEN CPU PSW=CLK INTR LEV -1  
TEST THAT CLOCK B WILL NOT INTR. WHEN CPU PSW=CLK INTR LEVEL  
TEST THAT A CLOCKS OVERFLOW WILL CAUSE AN INTR.  
TEST CLOCK A'S REPEATIBILITY AT 1MHZ RATE  
TEST CLOCK A'S REPEATIBILITY AT 100KHZ RATE  
TEST CLOCK A'S REPEATIBILITY AT 10KHZ RATE  
TEST CLOCK A'S REPEATIBILITY AT 1KHZ RATE  
TEST CLOCK A'S REPEATIBILITY AT 100HZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 1MHZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 100KHZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 10KHZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 1KHZ RATE  
TEST CLOCK B'S REPEATIBILITY AT 100HZ RATE  
TEST THAT "INIT" CLEARS B'S 100KHZ DIVIDE BY 10 CHIPS

.TITLE MAINDEC-11-DRLPG-A  
:\*COPYRIGHT (C) 1978  
:\*DIGITAL EQUIPMENT CORP.  
:\*MAYNARD, MASS. 01754  
:\*  
:\*PROGRAM BY EDWARD C. BADGER  
:\*  
:\*THIS PROGRAM WAS ASSEMBLED USING THE POP-11 MAINDEC SYSMAC  
:\*PACKAGE (MAINDEC-11-DZQAC-C2), SEPT 14, 1976.  
:\*

000001

\$TN=1  
.SBTTL OPERATIONAL SWITCH SETTINGS  
:\*  
:\* SWITCH USE  
:\* -----  
:\* 15 HALT ON ERROR

```

84      ;*      14      LOOP ON TEST
85      ;*      13      INHIBIT ERROR TYPEOUTS
86      ;*      11      INHIBIT ITERATIONS
87      ;*      10      BELL ON ERROR
88      ;*      9       LOOP ON ERROR
89      ;*      8       LOOP ON TEST IN SWR<7:0>
90      .SBTTL TRAP CATCHER
91
92      000000      .=0
93      ;*ALL UNUSED LOCATIONS FROM 4 - 776 CONTAIN A ".+2,HALT"
94      ;*SEQUENCE TO CATCH ILLEGAL TRAPS AND INTERRUPTS
95      ;*LOCATION 0 CONTAINS 0 TO CATCH IMPROPERLY LOADED VECTORS
96      000174      .=174
97      000174      000000      DISPREG: .WORD 0      ;; SOFTWARE DISPLAY REGISTER
98      000176      000000      SWREG:   .WORD 0      ;; SOFTWARE SWITCH REGISTER
99
100     000200      000137      001730      JMP      @#START      ;GO TO STARTING ADDRESS OF PROGRAM
101
102     000204      000137      002434      JMP      @#RSTART     ;GO TO RESTART ADDRESS.
103     000210      000137      023376      JMP      @#LS210      ;GO TO SPECIAL TEST #1.
104     000214      000137      023564      JMP      @#LS214      ;GO TO SPECIAL TEST #2.
105     000220      000137      024000      JMP      @#LS220      ;GO TO SPECIAL TEST #3.
106     000224      000137      024160      JMP      @#LS224      ;GO TO SPECIAL TEST #4.
107     000230      000137      024372      JMP      @#LS230      ;GO TO SPECIAL TEST #5.
108
109     .SBTTL BASIC DEFINITIONS
110
111     ;*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
112     001100      STACK= 1100
113     .EQUIV EMT,ERROR      ;; BASIC DEFINITION OF ERROR CALL
114     .EQUIV IOT,SCOPE      ;; BASIC DEFINITION OF SCOPE CALL
115
116     ;*MISCELLANEOUS DEFINITIONS
117     000011      HT= 11      ;; CODE FOR HORIZONTAL TAB
118     000012      LF= 12      ;; CODE FOR LINE FEED
119     000015      CR= 15      ;; CODE FOR CARRIAGE RETURN
120     000200      CRLF= 200    ;; CODE FOR CARRIAGE RETURN-LINE FEED
121     177776      PS= 177776   ;; PROCESSOR STATUS WORD
122     .EQUIV PS,PSW
123     177774      STKLMT= 177774 ;; STACK LIMIT REGISTER
124     177772      PIRQ= 177772  ;; PROGRAM INTERRUPT REQUEST REGISTER
125     177570      DSWR= 177570  ;; HARDWARE SWITCH REGISTER
126     177570      DDISP= 177570 ;; HARDWARE DISPLAY REGISTER
127
128     ;*GENERAL PURPOSE REGISTER DEFINITIONS
129     000000      R0= %0      ;; GENERAL REGISTER
130     000001      R1= %1      ;; GENERAL REGISTER
131     000002      R2= %2      ;; GENERAL REGISTER
132     000003      R3= %3      ;; GENERAL REGISTER
133     000004      R4= %4      ;; GENERAL REGISTER
134     000005      R5= %5      ;; GENERAL REGISTER
135     000006      R6= %6      ;; GENERAL REGISTER
136     000007      R7= %7      ;; GENERAL REGISTER
137     000006      SP= %6      ;; STACK POINTER

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138      000007      PC=      %7      ;;PROGRAM COUNTER
139
140      ;*PRIORITY LEVEL DEFINITIONS
141      000000      PR0=      0      ;;PRIORITY LEVEL 0
142      000040      PR1=      40     ;;PRIORITY LEVEL 1
143      000100      PR2=      100    ;;PRIORITY LEVEL 2
144      000140      PR3=      140    ;;PRIORITY LEVEL 3
145      000200      PR4=      200    ;;PRIORITY LEVEL 4
146      000240      PR5=      240    ;;PRIORITY LEVEL 5
147      000300      PR6=      300    ;;PRIORITY LEVEL 6
148      000340      PR7=      340    ;;PRIORITY LEVEL 7
149
150      ;*"SWITCH REGISTER" SWITCH DEFINITIONS
151      100000      SW15=     100000
152      040000      SW14=     40000
153      020000      SW13=     20000
154      010000      SW12=     10000
155      004000      SW11=     4000
156      002000      SW10=     2000
157      001000      SW09=     1000
158      000400      SW08=     400
159      000200      SW07=     200
160      000100      SW06=     100
161      000040      SW05=     40
162      000020      SW04=     20
163      000010      SW03=     10
164      000004      SW02=     4
165      000002      SW01=     2
166      000001      SW00=     1
167      .EQUIV     SW09,SW9
168      .EQUIV     SW08,SW8
169      .EQUIV     SW07,SW7
170      .EQUIV     SW06,SW6
171      .EQUIV     SW05,SW5
172      .EQUIV     SW04,SW4
173      .EQUIV     SW03,SW3
174      .EQUIV     SW02,SW2
175      .EQUIV     SW01,SW1
176      .EQUIV     SW00,SW0
177
178      ;*DATA BIT DEFINITIONS (BIT00 TO BIT15)
179      100000      BIT15=    100000
180      040000      BIT14=    40000
181      020000      BIT13=    20000
182      010000      BIT12=    10000
183      004000      BIT11=    4000
184      002000      BIT10=    2000
185      001000      BIT09=    1000
186      000400      BIT08=    400
187      000200      BIT07=    200
188      000100      BIT06=    100
189      000040      BIT05=    40
190      000020      BIT04=    20
191      000010      BIT03=    10

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000240  
  
170404  
000344  
000006  
  
000234  
000046  
023344  
000052  
000000  
000234  
001000

BIT02= 4  
BIT01= 2  
BIT00= 1  
.EQUIV BIT09,BIT9  
.EQUIV BIT08,BIT8  
.EQUIV BIT07,BIT7  
.EQUIV BIT06,BIT6  
.EQUIV BIT05,BIT5  
.EQUIV BIT04,BIT4  
.EQUIV BIT03,BIT3  
.EQUIV BIT02,BIT2  
.EQUIV BIT01,BIT1  
.EQUIV BIT00,BIT0

.\*BASIC "CPU" TRAP VECTOR ADDRESSES  
ERRVEC= 4 ;: TIME OUT AND OTHER ERRORS  
RESVEC= 10 ;: RESERVED AND ILLEGAL INSTRUCTIONS  
TBITVEC= 14 ;: "T" BIT  
TRTVEC= 14 ;: TRACE TRAP  
BPTVEC= 14 ;: BREAKPOINT TRAP (BPT)  
IOTVEC= 20 ;: INPUT/OUTPUT TRAP (IOT) \*\*SCOPE\*\*  
PWRVEC= 24 ;: POWER FAIL  
EMTVEC= 30 ;: EMULATOR TRAP (EMT) \*\*ERROR\*\*  
TRAPVEC= 34 ;: "TRAP" TRAP  
TKVEC= 60 ;: TTY KEYBOARD VECTOR  
TPVEC= 64 ;: TTY PRINTER VECTOR  
PIRQVEC= 240 ;: PROGRAM INTERRUPT REQUEST VECTOR

ABASE= 170404  
AVECT1= 344  
APRIOR= 6

.SBTTL ACT11 HOOKS

;;\*\*\*\*\*  
;HOOKS REQUIRED BY ACT11  
    \$SVPC=. ;SAVE PC  
    .=46  
    \$ENDAD ;;1)SET LOC.46 TO ADDRESS OF \$ENDAD IN .SEOP  
    .=52 ;;2)SET LOC.52 TO ZERO  
    .WORD 0  
    .= \$SVPC ;; RESTORE PC  
    .=1000

.SBTTL APT PARAMETER BLOCK

;;\*\*\*\*\*



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246
247
248      001000
249      000024
250 000024 000200
251      000044
252 000044 001000
253      001000
254
255
256
257
258 001000
259 001000 000000
260 001002 001202
261 001004 000002
262 001006 000120
263 001010 000120
264 001012 000052
265

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;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
;*****
.SX=.      ;SAVE CURRENT LOCATION
.=24      ;SET POWER FAIL TO POINT TO START OF PROGRAM
200       ;FOR APT START UP
.=44      ;POINT TO APT INDIRECT ADDRESS PNTR.
$APTHDR   ;POINT TO APT HEADER BLOCK
.=.SX     ;RESET LOCATION COUNTER
;*****
;SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
;INTERFACE SPEC.

```

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$APTHD:
$HIBTS: .WORD 0      ;TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
$MBADR: .WORD $MAIL  ;ADDRESS OF APT MAILBOX (BITS 0-15)
$STMT:  .WORD 2      ;RUN TIM OF LONGEST TEST
$PASTM: .WORD 120    ;RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
$UNITM: .WORD 120    ;ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
          .WORD      ;SETEND-$MAIL/2 ;;LENGTH MAILBOX-ETABLE(WORDS)

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267  
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269  
270  
271  
272  
273 001100  
274 001100 000000  
275 001102 000  
276 001103 000  
277 001104 000000  
278 001106 000000  
279 001110 000000  
280 001112 000000  
281 001114 000  
282 001115 001  
283 001116 000000  
284 001120 000000  
285 001122 000000  
286 001124 000000  
287 001126 000000  
288 001130 000000  
289 001132 000000  
290 001134 000  
291 001135 000  
292 001136 000000  
293 001140 177570  
294 001142 177570  
295 001144 177560  
296 001146 177562  
297 001150 177564  
298 001152 177566  
299 001154 000  
300 001155 002  
301 001156 012  
302 001157 000  
303 001160 000000  
304  
305 001162 000000  
306 001164 000000  
307 001166 000000  
308 001170 000000  
309 001172 177607 000377  
310 001176 077  
311 001177 015  
312 001200 000012  
313  
314  
315  
316  
317  
318 001202  
319 001202 000000

.SBTTL COMMON TAGS

\*\*\*\*\*  
; THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS  
; USED IN THE PROGRAM.

. =1100

SCMTAG: .WORD 0 ; ; START OF COMMON TAGS  
STSTNM: .BYTE 0 ; ; CONTAINS THE TEST NUMBER  
SERFLG: .BYTE 0 ; ; CONTAINS ERROR FLAG  
\$ICNT: .WORD 0 ; ; CONTAINS SUBTEST ITERATION COUNT  
\$LPADR: .WORD 0 ; ; CONTAINS SCOPE LOOP ADDRESS  
\$LPERR: .WORD 0 ; ; CONTAINS SCOPE RETURN FOR ERRORS  
\$ERTTL: .WORD 0 ; ; CONTAINS TOTAL ERRORS DETECTED  
\$ITEMB: .BYTE 0 ; ; CONTAINS ITEM CONTROL BYTE  
\$ERMAX: .BYTE 1 ; ; CONTAINS MAX. ERRORS PER TEST  
\$ERRPC: .WORD 0 ; ; CONTAINS PC OF LAST ERROR INSTRUCTION  
\$GDADR: .WORD 0 ; ; CONTAINS ADDRESS OF 'GOOD' DATA  
\$BDADR: .WORD 0 ; ; CONTAINS ADDRESS OF 'BAD' DATA  
\$GDDAT: .WORD 0 ; ; CONTAINS 'GOOD' DATA  
\$BDDAT: .WORD 0 ; ; CONTAINS 'BAD' DATA  
          .WORD 0 ; ; RESERVED--NOT TO BE USED  
          .WORD 0 ; ;  
\$AUTOB: .BYTE 0 ; ; AUTOMATIC MODE INDICATOR  
\$INTAG: .BYTE 0 ; ; INTERRUPT MODE INDICATOR  
          .WORD 0 ; ;  
\$SWR: .WORD DSWR ; ; ADDRESS OF SWITCH REGISTER  
\$DISPLAY: .WORD DDISP ; ; ADDRESS OF DISPLAY REGISTER  
\$TKS: 177560 ; ; TTY KBD STATUS  
\$TKB: 177562 ; ; TTY KBD BUFFER  
\$TPS: 177564 ; ; TTY PRINTER STATUS REG. ADDRESS  
\$TPB: 177566 ; ; TTY PRINTER BUFFER REG. ADDRESS  
\$NULL: .BYTE 0 ; ; CONTAINS NULL CHARACTER FOR FILLS  
\$FILLS: .BYTE 2 ; ; CONTAINS # OF FILLER CHARACTERS REQUIRED  
\$FILLC: .BYTE 12 ; ; INSERT FILL CHARS. AFTER A "LINE FEED"  
\$TPFLG: .BYTE 0 ; ; "TERMINAL AVAILABLE" FLAG (BIT<07>=0=YES)  
\$REGAD: .WORD 0 ; ; CONTAINS THE ADDRESS FROM WHICH (\$REGO) WAS OBTAINED  
\$REGO: .WORD 0 ; ; CONTAINS ((\$REGAD)+0)  
\$TMPO: .WORD 0 ; ; USER DEFINED  
\$TIMES: 0 ; ; MAX. NUMBER OF ITERATIONS  
\$ESCAPE: 0 ; ; ESCAPE ON ERROR ADDRESS  
\$BELL: .ASCIZ <207><377><377> ; ; CODE FOR BELL  
\$QUES: .ASCII /?/ ; ; QUESTION MARK  
\$CRLF: .ASCII <15> ; ; CARRIAGE RETURN  
\$LF: .ASCIZ <12> ; ; LINE FEED

\*\*\*\*\*  
.SBTTL APT MAILBOX-ETABLE

\*\*\*\*\*  
\$EVEN  
\$MAIL: ; ; APT MAILBOX  
\$MSGTY: .WORD AMSGTY ; ; MESSAGE TYPE CODE

320	001204	000000	\$FATAL: .WORD	AFATAL	:: FATAL ERROR NUMBER
321	001206	000000	\$TESTN: .WORD	ATESTN	:: TEST NUMBER
322	001210	000000	\$PASS: .WORD	APASS	:: PASS COUNT
323	001212	000000	\$DEVCT: .WORD	ADEVCT	:: DEVICE COUNT
324	001214	000000	\$UNIT: .WORD	AUNIT	:: I/O UNIT NUMBER
325	001216	000000	\$MSGAD: .WORD	AMSGAD	:: MESSAGE ADDRESS
326	001220	000000	\$MSGLG: .WORD	AMSGLG	:: MESSAGE LENGTH
327	001222		\$ETABLE:		:: APT ENVIRONMENT TABLE
328	001222	000	\$ENV: .BYTE	AENV	:: ENVIRONMENT BYTE
329	001223	000	\$ENVM: .BYTE	AENVM	:: ENVIRONMENT MODE BITS
330	001224	000000	\$SWREG: .WORD	ASWREG	:: APT SWITCH REGISTER
331	001226	000000	\$USWR: .WORD	AUSWR	:: USER SWITCHES
332	001230	000000	\$CPUOP: .WORD	ACPUOP	:: CPU TYPE, OPTIONS
333			::*		BITS 15-11=CPU TYPE
334			::*		11/04=01, 11/05=02, 11/20=03, 11/40=04, 11/45=05
335			::*		11/70=06, PDQ=07, Q=10
336			::*		BIT 10=REAL TIME CLOCK
337			::*		BIT 9=FLOATING POINT PROCESSOR
338			::*		BIT 8=MEMORY MANAGEMENT
339	001232	000	\$MAMS1: .BYTE	AMAMS1	:: HIGH ADDRESS M.S. BYTE
340	001233	000	\$MTYP1: .BYTE	AMTYP1	:: MEM. TYPE, BLK#1
341			::*		MEM. TYPE BYTE -- (HIGH BYTE)
342			::*		900 NSEC CORE=001
343			::*		300 NSEC BIPOLAR=002
344			::*		500 NSEC MOS=003
345	001234	000000	\$MADR1: .WORD	AMADR1	:: HIGH ADDRESS, BLK#1
346			::*		MEM. LAST ADDR.=3 BYTES, THIS WORD AND LOW OF "TYPE" ABOVE
347	001236	000	\$MAMS2: .BYTE	AMAMS2	:: HIGH ADDRESS M.S. BYTE
348	001237	000	\$MTYP2: .BYTE	AMTYP2	:: MEM. TYPE, BLK#2
349	001240	000000	\$MADR2: .WORD	AMADR2	:: MEM. LAST ADDRESS, BLK#2
350	001242	000	\$MAMS3: .BYTE	AMAMS3	:: HIGH ADDRESS M.S. BYTE
351	001243	000	\$MTYP3: .BYTE	AMTYP3	:: MEM. TYPE, BLK#3
352	001244	000000	\$MADR3: .WORD	AMADR3	:: MEM. LAST ADDRESS, BLK#3
353	001246	000	\$MAMS4: .BYTE	AMAMS4	:: HIGH ADDRESS M.S. BYTE
354	001247	000	\$MTYP4: .BYTE	AMTYP4	:: MEM. TYPE, BLK#4
355	001250	000000	\$MADR4: .WORD	AMADR4	:: MEM. LAST ADDRESS, BLK#4
356	001252	000344	\$VECT1: .WORD	AVECT1	:: INTERRUPT VECTOR#1 BUS PRIORITY#1
357	001254	000000	\$VECT2: .WORD	AVECT2	:: INTERRUPT VECTOR#2 BUS PRIORITY#2
358	001256	170404	\$BASE: .WORD	ABASE	:: BASE ADDRESS OF EQUIPMENT UNDER TEST
359	001260	000000	\$DEVN: .WORD	ADEVN	:: DEVICE MAP
360	001262	000000	\$CDW1: .WORD	ACDW1	:: CONTROLLER DESCRIPTION WORD#1
361	001264	000000	\$CDW2: .WORD	ACDW2	:: CONTROLLER DESCRIPTION WORD#2
362	001266	000000	\$DDW0: .WORD	ADDW0	:: DEVICE DESCRIPTOR WORD#0
363	001270	000000	\$DDW1: .WORD	ADDW1	:: DEVICE DESCRIPTOR WORD#1
364	001272	000000	\$DDW2: .WORD	ADDW2	:: DEVICE DESCRIPTOR WORD#2
365	001274	000000	\$DDW3: .WORD	ADDW3	:: DEVICE DESCRIPTOR WORD#3
366	001276	000000	\$DDW4: .WORD	ADDW4	:: DEVICE DESCRIPTOR WORD#4
367	001300	000000	\$DDW5: .WORD	ADDW5	:: DEVICE DESCRIPTOR WORD#5
368	001302	000000	\$DDW6: .WORD	ADDW6	:: DEVICE DESCRIPTOR WORD#6
369	001304	000000	\$DDW7: .WORD	ADDW7	:: DEVICE DESCRIPTOR WORD#7
370	001306	000000	\$DDW8: .WORD	ADDW8	:: DEVICE DESCRIPTOR WORD#8
371	001310	000000	\$DDW9: .WORD	ADDW9	:: DEVICE DESCRIPTOR WORD#9
372	001312	000000	\$DDW10: .WORD	ADDW10	:: DEVICE DESCRIPTOR WORD#10
373	001314	000000	\$DDW11: .WORD	ADDW11	:: DEVICE DESCRIPTOR WORD#11



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.SBTTL ERROR POINTER TABLE

;\*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.  
;\*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN  
;\*LOCATION \$ITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.  
;\*NOTE1: IF \$ITEMB IS 0 THE ONLY PERTINENT DATA IS (\$ERRPC).  
;\*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:

;\* EM ;: POINTS TO THE ERROR MESSAGE  
;\* DH ;: POINTS TO THE DATA HEADER  
;\* DT ;: POINTS TO THE DATA  
;\* DF ;: POINTS TO THE DATA FORMAT

\$ERRTB:

; ITEM 1  
EM1 ;: CLOCK A SR FUNCTION ERROR  
DH1 ;: ERRPC ASR WAS S/B  
DT1 ;: \$ERRPC, ASR, \$BDDAT, \$GDDAT  
DF0 ;: ALL NUMBERS ARE IN OCTAL FORM  
  
; ITEM 2  
EM2 ;: CLOCK A SR DATA ERROR  
DH1 ;: ERRPC ASR WAS S/B  
DT1 ;: \$ERRPC, ASR, \$BDDAT, \$GDDAT  
DF0 ;: ALL NUMBERS ARE IN OCTAL FORM  
  
; ITEM 3  
EM3 ;: CLOCK A BR DATA ERROR  
DH3 ;: ERRPC ABR WAS S/B  
DT3 ;: \$ERRPC, ABR, \$BDDAT, \$GDDAT  
DF0 ;: ALL NUMBERS ARE IN OCTAL FORM  
  
; ITEM 4  
EM4 ;: CLOCK A CR DATA ERROR  
DH4 ;: ERRPC ACR WAS S/B  
DT4 ;: \$ERRPC, ACR, \$BDDAT, \$GDDAT  
DF0 ;: ALL NUMBERS ARE IN OCTAL FORM  
  
; ITEM 5  
EM5 ;: CLOCK B SR DATA ERROR  
DH5 ;: ERRPC BSR WAS S/B  
DT5 ;: \$ERRPC, BSR, \$BDDAT, \$GDDAT  
DF0 ;: ALL NUMBERS ARE IN OCTAL FORM

001360  
  
001360 030112  
001362 030777  
001364 031612  
001366 032014  
  
001370 030145  
001372 030777  
001374 031612  
001376 032014  
  
001400 030174  
001402 031035  
001404 031624  
001406 032014  
  
001410 030223  
001412 031073  
001414 031636  
001416 032014  
  
001420 030252  
001422 031131  
001424 031650  
001426 032014

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457					
458					
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460	001430	030301			
461	001432	031167			
462	001434	031662			
463	001436	032014			
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468	001440	030330			
469	001442	031225			
470	001444	031674			
471	001446	032014			
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476	001450	030357			
477	001452	031263			
478					
479	001454	031706			
480	001456	032014			
481					
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485	001460	030404			
486	001462	031073			
487	001464	031636			
488	001466	032014			
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493	001470	030433			
494	001472	031422			
495	001474	031722			
496	001476	032014			
497					
498					
499					
500					
501	001500	032014			
502	001502	032014			
503	001504	032014			
504	001506	032014			
505					
506					
507					
508	001510	030473			
509	001512	031441			

```

;ITEM 6
EM6 ;CLOCK B BR DATA ERROR
DH6 ;ERRPC BBR WAS S/B
DT6 ;SERRPC, BBR, SBDDAT, SGDDAT
DFO ;ALL NUMBERS ARE IN OCTAL FORM

;ITEM 7
EM7 ;CLOCK B CR DATA ERROR
DH7 ;ERRPC BCR WAS S/B
DT7 ;SERRPC, BCR, SBDDAT, SGDDAT
DFO ;ALL NUMBERS ARE IN OCTAL FORM

;ITEM 10
EM10 ;DUAL ADDRESS ERROR
DH10 ;ERROR GOOD BAD GOOD DATA READ FROM
; PC ADDR ADDR DATA DUAL ADDRESS
;SERRPC, $GDADR, $BDADR, $GDDAT, $BDDAT
DFO ;ALL NUMBERS ARE IN OCTAL FORM

;ITEM 11
EM11 ;CLOCK A COUNT ERROR
DH4 ;ERRPC ACR WAS S/B
DT4 ;SERRPC, ACR, SBDDAT, SGDDAT
DFO ;ALL NUMBERS ARE IN OCTAL FORM

;ITEM 12
EM12 ;CLOCK A COUNT FUNCTION ERROR
DH12 ;ERRPC ASR
DT12 ;ERRPC, ASR
DFO ;ALL NUMBERS ARE IN OCTAL FORM

;ITEM 13
DFO ;ERROR 13 DOES NOT EXSIST.
DFO ;IT WOULD BE BAD LUCK.
DFO

;ITEM 14
EM14 ;CLOCK B COUNT FUNCTION ERROR
DH14 ;ERRPC BSR

```

510	001514	031730	DT14	;SERRPC, BSR
511	001516	032014	DF0	;ALL NUMBERS ARE IN OCTAL FORM
512				
513				
514				
515			; ITEM 15	
516	001520	030533	EM15	;CLOCK B COUNT ERROR
517	001522	031225	DH7	;ERRPC CSR WAS S/B
518	001524	031674	DT7	;SERRPC, BCR, SBDDAT, SGDDAT
519	001526	032014	DF0	;ALL NUMBERS ARE IN OCTAL FORM
520				
521				
522			; ITEM 16	
523				
524	001530	030562	EM16	;CLOCK A INTERRUPT ERROR
525	001532	031422	DH12	;ERRPC ASR
526	001534	031722	DT12	;SERRPC, ASR
527	001536	032014	DF0	;ALL NUMBERS ARE IN OCTAL FORM
528				
529				
530			; ITEM 17	
531				
532	001540	030615	EM17	;CLOCK B INTERRUPT ERROR
533	001542	031441	DH14	;ERRPC BSR
534	001544	031730	DT14	;SERRPC, BSR
535	001546	032014	DF0	
536				
537			; ITEM 20	
538				
539	001550	030650	EM20	;CLOCK A REPEATABILITY ERROR
540	001552	031457	DH20	;ERROR ASR 2ND CNT 1ST CNT
541	001554	031612	DT1	;SERRPC, ASR, SBDDAT, SGDDAT
542	001556	032014	DF0	;ALL NUMBERS ARE IN OCTAL FORM
543				
544				
545			; ITEM 21	
546				
547	001560	030404	EM11	;CLOCK A COUNT ERROR
548	001562	031073	DH4	;ERROR ASR 2ND CNT 1ST CNT
549	001564	031736	DT21	;SERRPC, ASR, SBDDAT, SGDDAT
550	001566	032014	DF0	;ALL NUMBERS ARE IN OCTAL FORM
551				
552				
553			; ITEM 22	
554				
555	001570	030404	EM11	;CLOCK A COUNT ERROR
556	001572	031073	DH4	;ERRPC ASR WAS S/B
557	001574	031750	DT22	;SERRPC, ACR, SBDDAT, STMPD
558	001576	032014	DF0	;ALL NUMBERS ARE IN OCTAL FORM
559				
560				
561			; ITEM 23	
562				
563	001600	030707	EM23	;CLOCK B REPEATABILITY ERROR

```

564 001602 031521          DH23          ;ERROR ASR 2NDCNT 1STCNT
565 001604 031612          DT1           ;$ERRPC, ASR, $BDDAT, $GDDAT
566 001606 032014          DFO           ;ALL NUMBERS ARE IN OCTAL FORM
567
568
569          ;ITEM 24
570
571 001610 030533          EM15          ;CLOCK B COUNT ERROR
572 001612 031225          DH7           ;ERRPC BCR WAS S/B
573 001614 031762          DT24          ;$ERRPC, BCR, $GDDAT, $TMPO
574 001616 032014          DFO           ;ALL NUMBERS ARE IN OCTAL FORM
575
576
577          ;ITEM 25
578
579 001620 030533          EM15          ;CLOCK B COUNT ERROR
580 001622 031225          DH7           ;ERRPC BCR WAS S/B
581 001624 031774          DT25          ;$ERRPC, BCR, $BDDAT, $TMPO
582 001626 032014          DFO           ;ALL NUMBERS ARE IN OCTAL FORM
583
584
585          ;ITEM 26
586
587 001630 030746          EM26          ;CLOCK ADDRESSING ERROR
588 001632 031563          DH26          ;ERRPC CLOCK ADDR.
589 001634 032006          DT26          ;$ERRPC, $TMPO
590 001636 032014          DFO           ;ALL NUMBERS ARE IN OCTAL FORM
591
592
593
594
595          ;ADDRESS OF KMC-11 OF LPA-11 THE ADDR FOR KMADD MAY BE
596          ;                          CHANGED BY THE USER TO REFLECT
597          ;                          A DIFFERENT KMC-11 ADDR. THE
598          ;                          REST OF THE ADDRESSES WILL
599          ;                          BE CHANGED BY THE PROGRAM.
600
601
602 001640          LPCI:
603 001640 170460          KMADD: .WORD 170460          ;BASE KMC ADDR. MAY BE PATCHED BY USER.
604
605 001642          LPMR:
606 001642 170461          KMAD1: .WORD 170460+1          ;>DO NOT <;KMC-CSR ADDR
607 001644          LPCO:
608 001644 170462          KMAD2: .WORD 170460+2          ;>PATCH <;
609 001646          LPSO:
610 001646 170463          KMAD3: .WORD 170460+3          ;>THIS AREA <
611 001650          LPADL:
612 001650 170464          KMAD4: .WORD 170460+4          ;
613 001652          LPADH:
614 001652 170465          KMAD5: .WORD 170460+5          ;>DO NOT <
615 001654          LPMS1:
616 001654 170466          KMAD6: .WORD 170460+6          ;>PATCH <
617 001656          LPMS2:

```



618	001656	170467	KMAD7: .WORD	170460+7	; >THIS AREA <
619					
620	001660	000344	VECTOR: .WORD	AVECT1&777	; BASE VECTOR OF KMC
621	001662	000350	VECTPS: .WORD	4+AVECT1&777	; VECOTR ADDR.+2
622					
623	001664	000004	VERSN: .WORD	4	; CURRENT VERSION NUMBER OF MICROCODE.
624					
625	001666	000000	.DVLS: .WORD	0	; /DEVICE LIST OF I/O ADDR. DEFINED
626	001670	000020	.BLKW	16.	; /BY INIT.
627					
628			.SBTTL	PROGRAM START	

```

629
630 001730
631
632
633 001730 012706 001100
634 001734 005026
635 001736 022706 001140
636 001742 001374
637 001744 012706 001100
638
639 001750 012737 025762 000020
640 001756 012737 000340 000022
641 001764 012737 025214 000030
642 001772 012737 000340 000032
643 002000 012737 030026 000034
644 002006 012737 000340 000036
645 002014 012737 027650 000024
646 002022 012737 000340 000026
647 002030 005037 001166
648 002034 005037 001170
649 002040 112737 000001 001115
650 002046 012737 002046 001106
651 002054 012737 002054 001110
652
653
654 002062 013746 000004
655 002066 012737 002122 000004
656 002074 012737 177570 001140
657 002102 012737 177570 001142
658 002110 022777 177777 177022
659 002116 001012
660
661 002120 000403
662 002122 012716 002130
663 002126 000002
664 002130 012737 000176 001140
665 002136 012737 000174 001142
666 002144 012637 000004
667
668 002150 005037 001210
669 002154 132737 000200 001223
670 002162 001403
671 002164 012737 001224 001140
672 002172
673 002172 005737 000042
674 002176 001015
675
676 002200 104401 002206
677 002204 000412
678
679 002232
680
681 002232 013737 001256 001326
682 002240 012737 000001 001212

```

```

START:
.SBTTL INITIALIZE THE COMMON TAGS
;;CLEAR THE COMMON TAGS ($CMTAG) AREA
MOV    $CMTAG,R6          ;;FIRST LOCATION TO BE CLEARED
CLR    (R6)+              ;;CLEAR MEMORY LOCATION
CMP    $SWR,R6           ;;DONE?
BNE    -6                 ;;LOOP BACK IF NO
MOV    $STACK,SP         ;;SETUP THE STACK POINTER
;;INITIALIZE A FEW VECTORS
MOV    $$SCOPE,$IOTVEC   ;;IOT VECTOR FOR SCOPE ROUTINE
MOV    $340,$IOTVEC+2    ;;LEVEL 7
MOV    $ERROR,$EMTVEC   ;;EMT VECTOR FOR ERROR ROUTINE
MOV    $340,$EMTVEC+2    ;;LEVEL 7
MOV    $TRAP,$TRAPVEC   ;;TRAP VECTOR FOR TRAP CALLS
MOV    $340,$TRAPVEC+2  ;;LEVEL 7
MOV    $SPWRDN,$PWRVEC  ;;POWER FAILURE VECTOR
MOV    $340,$PWRVEC+2   ;;LEVEL 7
CLR    $TIMES            ;;INITIALIZE NUMBER OF ITERATIONS
CLR    $ESCAPE          ;;CLEAR THE ESCAPE ON ERROR ADDRESS
MOVB  $1,$SERMAX        ;;ALLOW ONE ERROR PER TEST
MOV    $,$SLPADR        ;;INITIALIZE THE LOOP ADDRESS FOR SCOPE
MOV    $,$SLPERR        ;;SETUP THE ERROR LOOP ADDRESS
;;SIZE FOR A HARDWARE SWITCH REGISTER. IF NOT FOUND OR IT IS
;;EQUAL TO A "-1" SETUP FOR A SOFTWARE SWITCH REGISTER.
MOV    $ERRVEC,-(SP)    ;;SAVE ERROR VECTOR
MOV    $64,$ERRVEC     ;;SET UP ERROR VECTOR
MOV    $DSWR,$SWR      ;;SETUP FOR A HARDWARE SWICH REGISTER
MOV    $DDISP,$DISPLAY ;;AND A HARDWARE DISPLAY REGISTER
CMP    $-1,$SWR        ;;TRY TO REFERENCE HARDWARE SWR
BNE    66$             ;;BRANCH IF NO TIMEOUT TRAP OCCURRED
                        ;;AND THE HARDWARE SWR IS NOT = -1
BR     65$             ;;BRANCH IF NO TIMEOUT
MOV    $65$,(SP)      ;;SET UP FOR TRAP RETURN
RTI
65$: MOV    $SWREG,$SWR  ;;POINT TO $SOFTWARE SWR
MOV    $DISPREG,$DISPLAY
66$: MOV    (SP)+,$ERRVEC ;;RESTORE ERROR VECTOR
CLR    $PASS           ;;CLEAR PASS COUNT
BITB  $APTSIZE,$ENVM  ;;TEST USER SIZE UNDER APT
BEQ   67$             ;;YES,USE NON-APT SWITCH
MOV    $$SWREG,$SWR   ;;NO,USE APT SWITCH REGISTER
67$: TST    $42        ;;IF RUNNING UNDER ACT-
BNE    10$           ;;NO TYPEOUT.
TYPE  69$           ;;TYPE ASCIZ STRING
BR    68$           ;;GET OVER THE ASCIZ
69$: .ASCIZ <15><12><12>#MD-11-DRLPG-A#<15><12>
68$:
10$: MOV    $BASE,$ASR
MOV    $1,$DEVCT

```

```

683 002246 005037 001210 CLR $PASS
684
685
686 ; THIS SECTION OF CODE HANDLES INITIALIZING LPA-11 FUNCTIONS
687 ;
688
689 002252 010046 MOV RO,-(SP)
690 002254 010146 MOV R1,-(SP)
691 002256 013700 001640 MOV KMADD,RO ;GET KMC-11 ADDRESS.
692 002262 012701 001642 MOV #KMAD1,R1 ;GET ADDR. OF ADDR. LIST.
693
694 002266 005200 70$: INC RO ;UPDATE ADDR.
695 002270 010021 MOV RO,(1)+ ;WRITE ADDR.
696 002272 020127 001660 CMP R1,#KMAD7+2 ;DONE ALL ADDRESSES?
697 002276 001373 BNE 70$ ;NO - DO NEXT ADDR.
698 002300 005037 001666 CLR .DVL$ ;CLR ADDR. LIST.
699 002304 012601 MOV (SP)+,R1
700 002306 012600 MOV (SP)+,RO
701
702 LOOP:
703 002310 005000 1$: CLR RO ;DELAY SOME TIME SO THAT FIRST RESET
704 002312 005200 INC RO ;INSTR. WON'T CLOBBER TYPEOUT.
705 002314 001376 BNE 1$ ;NOW WE'RE GONNA FIX
706 002316 013700 001326 MOV ASR,RO ;ALL CLOCK ADDRESSES BASED ON ASR.
707 002322 062700 000002 ADD #2,RO
708 002326 010037 001330 MOV RO,ABR
709 002332 062700 000022 ADD #2,RO
710 002336 010037 001332 MOV RO,ACR
711 002342 062700 000002 ADD #2,RO
712 002346 010037 001334 MOV RO,BSR
713 002352 062700 000002 ADD #2,RO
714 002356 010037 001336 MOV RO,BBR
715 002362 062700 000002 ADD #2,RO
716 002366 010037 001340 MOV RO,BCR
717
718 002372 013700 001342 MOV AVECT,RO ;NOW FIX VECTOR ADDRESSES
719 002376 062700 000002 ADD #2,RO ;BASED ON AVECT.
720 002402 010037 001344 MOV RO,AVECP2
721 002406 062700 000016 ADD #16,RO
722 002412 010037 001346 MOV RO,BVECT
723 002416 062700 000002 ADD #2,RO
724 002422 010037 001350 MOV RO,BVECT2
725
726 002426 013737 001352 001354 RSTART: MOV APRITY,BPRITY ;FIX CLK B'S PRIORITY BASED ON A'S.
727 002434 012706 001100 MOV #STACK,SP
728 002440 012746 000340 MOV #340,-(SP) ;SET PROCESSOR PRIORITY TO 7.
729 002444 012746 002452 MOV #1$,-(SP)
730 002450 000002 RTI
731 002452 1$:
732
733 .SBTTL *
734 .SBTTL * PHASE 1 CLOCKS A+B BASIC LOGIC TESTS.
735 .SBTTL *

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002452 000240  
002454 012737 000050 001166  
002462 012737 002470 001106  
002470 112737 000001 001102  
002476 112737 000001 001206

```
*****
*TEST 1 *TEST THE ADDRESSABILITY OF CLOCK ADDRESS
*
*"BUS A17": "A04" = "DEVICE" H; "DEVICE" H + "TPO" H = "DEV ENABLE" H
*"DEV ENABLE" H + "TP1" H = "DEV ENB 2" H
*
* PROBABLE SYNC POINT FOR THIS TEST:: "BUS A17"
*
* CLOCK ADDRESS TEST. SCOPE FOR "DEV ENB 2" H AND WORK BACK
*
*****
```

```
†ST1: NOP
      MOV #50,$TIMES ;;DO 50 ITERATIONS
      MOV #15,$LPADR ;;SET SCOPE LOOP ADDRESS
1$:   MOVB #1,$STNM
      MOVB #1,$TESTN

; * MOV QASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
; * MOV QABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
; * MOV QACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
; * MOV QBSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
; * MOV QBBR,$BDDAT ;/READ DEVICE REG BBR,PUT DATA IN $BDDAT.
; * MOV QBCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
```

```
*****
*TEST 2 *TEST THAT CLOCK A BUFFER CAN BE WRITTEN INTO
*
*FOR LOADING DATA:
*
*(WE KNOW WE CAN ADDR. KW11), "BUS A01" L + "A02" H + "A03" H
*+"BUS C1" L="LD BUFF A" L
*"LD BUF A" L + BUFFERED DATA LOADS INTO MUX LATCH (NOTE WE KNOW
*BY NOW "TP1" L SHOULD BE GOOD).
*
* FOR READING DATA:
*
*BUS A01 L + (DATA IN H + EV ENABLE(1) H)=RD BUFF AL
*[BA01H*(DEPENDING ON WHICH DATA BITS READ) RD BUF AL]+BUFF A00:15
*+[DEV ENABLE*DATA IN L]=BUS DATA
*
*SINCE WE WONT LOOK FOR ANY SPECIFIC DATA BIT FAILURE,
*JUST THAT WE CAN WRITE INTO BUFFER + READ BACK,
*IF FAILED, KEY ON "LD BUFF A L" AND "RD BUFF A L"
```

```
790 ;*  
791 ;* PROBABLE SYNC POINT FOR THIS TEST:: "BUS A17" (2 OCCURANCES PER LOOP)  
792 ;*  
793 ;*  
794 ;*  
795 ;*****  
796 002564 000004 000050 001166 †ST2: SCOPE ; ;DO 50 ITERATIONS  
797 002566 012737 000050 001166 MOV #50,$TIMES ; ;DO 50 ITERATIONS  
798 ;WRITE INTO PRESET BUFFER.  
799 ;SET $GDDAT FOR ERROR TYPEOUT.  
800 ;READ THE PRESET BUFFER.  
801 002574 012737 001416 001124 MOV #1416,$GDDAT  
802 ;* MOV $GDDAT,$ABR ; / PUT DATA FROM $GDDAT TO DEVICE REG ABR  
803 ;* MOV $ABR,$BDDAT ; /READ DEVICE REG ABR,PUT DATA IN $BDDAT.  
804 002622 005737 001126 TST $BDDAT  
805 002626 001001 BNE IS ; IF ANY DATA WAS READ BACK, WE WILL  
806 ;BR PAST THE ERROR CALL.  
807  
808  
809  
810  
811
```

;;; \$ >> ERROR << \$

```
815 002630 104003 ERROR 3 ;UNABLE TO LOAD AND READ BACK  
816 ;FROM THE BUFFER REGISTER CLOCK A.  
817
```

;;; \$ >> ERROR << \$

```
821 002632 IS:
```

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```
*****
*TEST 3          *TEST THAT CLOCK A BUFFER CAN BE WRITTEN TO A ZERO
*
*THE LAST TEST WROTE 1'S INTO CLOCK A'S BUFFER. IN THIS
*TEST WE TRY TO WRITE ALL ZEROS.
*
*SIGNALS - SAME AS LAST TEST. SUSPECT F/F OR DATA GATE STUCK OPEN
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*
```

002632 000004  
002634 012737 000050 001166  
002642 005037 001124  
002666 005737 001126  
002672 001401

```
*****
*ST3: SCOPE
MOV #50,$TIMES ;;DO 50 ITERATIONS
CLR $GDDAT ;INDICATE WE EXPECT 0'S.
;CLEAR BUFFER REGISTER.
;READ CLOCK A'S BUFFER REGISTER
* MOV $GDDAT,$ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
* MOV $ABR,$BDDAT ;/READ DEVICE REG ABR,PUT DATA IN $BDDAT.
TST $BDDAT
BEQ IS ;SHOULD BE CLEAR - IF CLEAR - NEXT TEST.
```

;;; \$> ERROR <<\$

853  
854  
855

002674 104003 ERROR 3 ;CLEAR INTR. FAILED TO CLEAR CLOCK A'S  
;BUFFER REGISTER.

;;; \$> ERROR <<\$

859  
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871  
872  
873  
874  
875

002676

IS:

```
*****
*TEST 4          *TEST THAT CLOCK A'S STATUS CAN BE WRITTEN AND READ
*
*NOW THAT WE CAN WRITE INTO THE BUFFER REGISTER, WE'RE GOING TO TRY
*WRITING INTO THE STATUS REGISTER AND READ IT BACK.
*
*NEW SIGNALS: ["BA03" L + "BA02" L + "BA01" L]="LD STAT A" L
*             "DATA OUT LO" L + "DATA OUT HI" L + "LD STATA" L = "LD STAT A HI" H
*             + "LD STATA LO H"
*FOR READ BACK: "RD STATA" L
*
*NO ATTEMPT MADE TO VERIFY THAT CORRECT DATA CAME BACK, BUT
*JUST THAT SOME DATA CAME BACK.
*
```









804

MAINDEC-11-DRLPG-A  
DRLPG.P11 T7

MACY11 27(654) 15-DEC-77 08:29 PAGE 23  
\*TEST THAT CLOCK A STATUS REGISTER BIT 15 CAN BE SET AND CLEARED

SEQ 0040

1038 003202

25:



004

MAINDEC-11-DRLPG-A  
DRLPG.P11 T10

MACY11 27(654) 15-DEC-77 08:29 PAGE 25  
\*TEST THAT CLOCK A STATUS REGISTER BIT 14 CAN BE SET AND CLEARED

SEQ 0042

1093 003310

25:



F04

MAINDEC-11-DRLPG-A  
DRLPG.P11 T11

MACY11 27(654) 15-DEC-77 08:29 PAGE 27  
\*TEST THAT CLOCK A STATUS REGISTER BIT 13 CAN BE SET AND CLEARED

SEQ 0044

1148 003416

2S:



H04

MAINDEC-11-DRLPG-A  
DRLPG.P11 T12

MACY11 27(654) 15-DEC-77 08:29 PAGE 29  
\*TEST THAT CLOCK A STATUS REGISTER BIT 9 CAN BE SET AND CLEARED

SEQ 0046

1203 003524

2\$:





J04

MAINDEC-11-DRLPG-A  
DRLPG.P11 T13

MACY11 27(654) 15-DEC-77 08:29 PAGE 31  
\*TEST THAT CLOCK A STATUS REGISTER BIT 8 CAN BE SET AND CLEARED

SEQ 0048

1258 003632

25:



L04

MAINDEC-11-DRLPG-A  
DRLPG.P11 T14

MACY11 27(654) 15-DEC-77 08:29 PAGE 33  
\*TEST THAT CLOCK A STATUS REGISTER BIT 7 CAN BE SET AND CLEARED

SEQ 0050

1313 003740

2S:



N04

MAINDEC-11-DRLPG-A  
DRLPG.P11 T15

MACY11 27(654) 15-DEC-77 08:29 PAGE 35  
\*TEST THAT CLOCK A STATUS REGISTER BIT 6 CAN BE SET AND CLEARED

SEQ 0052

1368 004046

2S:



MAINDEC-11-DRLPG-A  
DRLPG.P11 T16

MACY11 27(654) 15-DEC-77 08:29 PAGE 37  
\*TEST THAT CLOCK A STATUS REGISTER BIT 5 CAN BE SET AND CLEARED

SEQ 0054

1423 004154

2\$:





E05

MAINDEC-11-DRLPG-A  
DRLPG.P11 T17

MACY11 27(654) 15-DEC-77 08:29 PAGE 39  
\*TEST THAT CLOCK A STATUS REGISTER BIT 3 CAN BE SET AND CLEARED

SEQ 0056

1478 004262

2\$:



G05

MAINDEC-11-DRLPG-A  
DRLPG.P11 T20

MACY11 27(654) 15-DEC-77 08:29 PAGE 41  
\*TEST THAT CLOCK A STATUS REGISTER BIT 2 CAN BE SET AND CLEARED

SEQ 0058

1533 004370

2\$:



MAINDEC-11-DRLPG-A  
DRLPG.P11 T21

MACY11 27(654) 15-DEC-77 08:29 PAGE 43  
\*TEST THAT CLOCK A STATUS REGISTER BIT 1 CAN BE SET AND CLEARED

SEQ 0060

1588 004476

25:



K05

MAINDEC-11-DRLPG-A  
DRLPG.P11 T22

MACY11 27(654) 15-DEC-77 08:29 PAGE 45  
\*TEST THAT CLOCK A STATUS REGISTER BIT 0 CAN BE SET AND CLEARED

SEQ 0062

1643 004604

25:





MAINDEC-11-DRLPG-A  
DRLPG.P11 T23

M05

MACY11 27(654) 15-DEC-77 08:29 PAGE 47  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED

SEQ 0064

1698 004712

25:



B06

MAINDEC-11-DRLPG-A  
DRLPG.P11 T24

MACY11 27(654) 15-DEC-77 08:29 PAGE 49  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED

SEQ 0066

1753 005020

25:



006

MAINDEC-11-DRLPG-A  
DRLPG.P11 T25

MACY11 27(654) 15-DEC-77 08:29 PAGE 51  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED

SEQ 0068

1808 005126

25:



F06

MAINDEC-11-DRLPG-A  
DRLPG.P11 T26

MACY11 27(654) 15-DEC-77 08:29 PAGE 53  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED

SEQ 0070

1863 005234

2\$:





MAINDEC-11-DRLPG-A  
DRLPG.P11 T27

MACY11 27(654) 15-DEC-77 08:29 PAGE 55  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED

H06

1918 005342

25:

SEQ 0072



J06

MAINDEC-11-DRLPG-A  
DRLPG.P11 T30

MACY11 27(654) 15-DEC-77 08:29 PAGE 57  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED

SEQ 0074

1973 005450

2\$:



L06

MAINDEC-11-DRLPG-A  
DRLPG.P11 T31

MACY11 27(654) 15-DEC-77 08:29 PAGE 59  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED

SEQ 0076

2028 005556

29:



N06

MAINDEC-11-DRLPG-A  
DRLPG.P11 T32

MACY11 27(654) 15-DEC-77 08:29 PAGE 61  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 7 CAN BE SET AND CLEARED

SEQ 0078

2083 005664

2\$:





C07

MAINDEC-11-DRLPG-A  
DRLPG.P11 T33

MACY11 27(654) 15-DEC-77 08:29 PAGE 63  
\*TEST THAT CLOCK A BUFFER REGISTER BIT B CAN BE SET AND CLEARED

SEQ 0080

2138 005772

25:



E07

MAINDEC-11-DRLPG-A  
DRLPG.P11 T34

MACY11 27(654) 15-DEC-77 08:29 PAGE 65  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 9 CAN BE SET AND CLEARED

SEQ 0082

2193 006100

2S:



GO7

MAINDEC-11-DRLPG-A  
DRLPG.P11 T35

MACY11 27(654) 15-DEC-77 08:29 PAGE 67  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 10 CAN BE SET AND CLEARED

SEQ 0084

2248 006206

25:



MAINDEC-11-DRLPG-A  
DRLPG.P11 T36

MACY11 27(654) 15-DEC-77 08:29 PAGE 69  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 11 CAN BE SET AND CLEARED

SEQ 0086

2303 006314

25:





K07

MAINDEC-11-DRLPG-A  
DRLPG.P11 T37

MACY11 27(654) 15-DEC-77 08:29 PAGE 71  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 12 CAN BE SET AND CLEARED

SEQ 0088

2358 006422

25:



M07

MAINDEC-11-DRLPG-A  
DRLPG.P11 T40

MACY11 27(654) 15-DEC-77 08:29 PAGE 73  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 13 CAN BE SET AND CLEARED

SEQ 0090

2413 006530

25:



B08

MAINDEC-11-DRLPG-A  
DRLPG.P11 T41

MACY11 27(654) 15-DEC-77 08:29 PAGE 75  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 14 CAN BE SET AND CLEARED

SEQ 0092

2468 006636

25:



MAINDEC-11-DRLPG-A  
DRLPG.P11 T42

MACY11 27(654) 15-DEC-77 08:29 PAGE 77  
\*TEST THAT CLOCK A BUFFER REGISTER BIT 15 CAN BE SET AND CLEARED

SEQ 0094

2523 006744  
2524  
2525

25:





F08

MAINDEC-11-DRLPG-A  
DRLPG.P11 T43

MACY11 27(654) 15-DEC-77 08:29 PAGE 79  
\*TEST THAT CLOCK B STATUS REGISTER BIT 11 CAN BE SET AND CLEARED

SEQ 0096

2580 007052  
2581

25:



H08

MAINDEC-11-DALPG-A  
DALPG.P11 T44

MACY11 27(654) 15-DEC-77 08:29 PAGE 81  
\*TEST THAT CLOCK B STATUS REGISTER BIT 7 CAN BE SET AND CLEARED

SEQ 0098

2636 007160  
2637

25:



J08

MAINDEC-11-DRLPG-A  
DRLPG.P11 T45

MACY11 27(654) 15-DEC-77 08:29 PAGE 83  
\*TEST THAT CLOCK B STATUS REGISTER BIT 6 CAN BE SET AND CLEARED

SEQ 0100

2692 007266  
2693

25:



MAINDEC-11-DRLPG-A  
DRLPG.P11 T46

MACY11 27(654) 15-DEC-77 08:29 PAGE 85  
\*TEST THAT CLOCK B STATUS REGISTER BIT 5 CAN BE SET AND CLEARED

SEQ 0102

2748 007374  
2749

25:





N08

M3INDEC-11-DRLPG-A  
DRLPG.P11 T47

MACY11 27(654) 15-DEC-77 08:29 PAGE 87  
\*TEST THAT CLOCK B STATUS REGISTER BIT 4 CAN BE SET AND CLEARED

SEQ 0104

2804 007502  
2805

2S:



C09

MAINDEC-11-DRLPG-A  
DRLPG.P11 T50

MACY11 27(654) 15-DEC-77 08:29 PAGE 89  
\*TEST THAT CLOCK B STATUS REGISTER BIT 3 CAN BE SET AND CLEARED

SEQ 0106

2860 007610  
2861

2\$:



MAINDEC-11-DRLPG-A  
DRLPG.P11 T51

MACY11 27(654) 15-DEC-77 08:29 PAGE 91  
\*TEST THAT CLOCK B STATUS REGISTER BIT 2 CAN BE SET AND CLEARED

SEQ 0108

2916 007716  
2917

25:



G09

MAINDEC-11-DRLPG-A  
DRLPG.P11 T52

MACY11 27(654) 15-DEC-77 08:29 PAGE 93  
\*TEST THAT CLOCK B STATUS REGISTER BIT 1 CAN BE SET AND CLEARED

SEQ 0110

2972 010024  
2973

25:





MAINDEC-11-DRLPG-A  
DRLPG.P11 T53

MACY11 27(654) 15-DEC-77 08:29 PAGE 95  
\*TEST THAT CLOCK B STATUS REGISTER BIT 0 CAN BE SET AND CLEARED

SEQ 0112

3028 010132

25:



K09

MAINDEC-11-DRLPG-A  
DRLPG.P11 TS4

MACY11 27(654) 15-DEC-77 08:29 PAGE 97  
\*TEST THAT CLOCK B BUFFER REGISTER BIT 0 CAN BE SET AND CLEARED

SEQ 0114

3083 010240

25:



MAINDEC-11-DRLPG-A  
DRLPG.P11 T55

MACY11 27(654) 15-DEC-77 08:29 PAGE 99  
\*TEST THAT CLOCK B BUFFER REGISTER BIT 1 CAN BE SET AND CLEARED

SEQ 0116

3138 010346

2\$:



M3INDEC-11-DRLPG-A  
DRLPG.P11 T56

MACY11 27(654) 15-DEC-77 08:29 PAGE 101  
\*TEST THAT CLOCK B BUFFER REGISTER BIT 2 CAN BE SET AND CLEARED

SEQ 0118

3193 010454

25:





D10

MAINDEC-11-DRLPG-A  
DRLPG.P11 T57

MACY11 27(654) 15-DEC-77 08:29 PAGE 103  
\*TEST THAT CLOCK B BUFFER REGISTER BIT 3 CAN BE SET AND CLEARED

SEQ 0120

3248 010562

2\$:



F10

MAINDEC-11-DRLPG-A  
DRLPG.P11 T60

MACY11 27(654) 15-DEC-77 08:29 PAGE 105  
\*TEST THAT CLOCK B BUFFER REGISTER BIT 4 CAN BE SET AND CLEARED

SEQ 0122

3303 010670

2\$:



H10

MAINDEC-11-DRLPG-A  
DRLPG.P11 T61

MACY11 27(654) 15-DEC-77 08:29 PAGE 107  
\*TEST THAT CLOCK B BUFFER REGISTER BIT 5 CAN BE SET AND CLEARED

SEQ 0124

3358 010776

25:



MAINDEC-11-DRLPG-A  
DRLPG.P11 T62

MACY11 27(654) 15-DEC-77 08:29 PAGE 109  
\*TEST THAT CLOCK B BUFFER REGISTER BIT 6 CAN BE SET AND CLEARED

SEQ 0126

3413 011104

25:













MAINLEC-11-DRLPG-A  
DRLPG.P11 T70

MACY11 27(654) 15-DEC-77 08:29 PAGE 115  
\*TEST CLOCK B'S COUNT REGISTER WITH 125 PATTERN

SEQ 0132

```

3684          ;*      MOV      $GDDAT, @BSR           ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
3685                                         ;LOAD THE BUFFER REGISTER WITH
3686                                         ;PATTERN 125. IT WILL BE
3687                                         ;TRANSFERRED TO THE COUNT REGISTER
3688                                         ;SINCE THIS IS MODE 0.
3689
3690 011546 012737 000125 001124          MOV      #125, $GDDAT           ;SET EXPECTED TO PATTERN IN CASE OF
3691                                         ;*      MOV      $GDDAT, @BBR           ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
3692                                         ;NEED OF ERROR TIMEOUT.
3693                                         ;READ THE COUNT REGISTER
3694
3695                                         ;*      MOV      @BCR, $BDDAT          ;/READ DEVICE REG BCR, PUT DATA IN $BDDAT.
3696                                         ;DID ALL THE BITS AND NO OTHER BITS
3697 011574 023737 001124 001126          CMP      $GDDAT, $BDDAT        ;COME THROUGH?
3698 011602 001401                         BEQ      1$                     ;BR IF YES TO NEXT TEST.
3699
3700
3701
3702

```

```

;;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR < $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

```

```

3706 011604 104007                         ERROR 7                          ;DATA ERROR CLOCK B - PATTERN "125"
3707                                         ;FAILED TO TRANSFER PROPERLY BETWEEN
3708                                         ;BUFFER AND COUNT REGISTERS.
3709
3710

```

```

;;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR < $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

```

```

3714 011606          1$:
3715          ;: *****
3716          ;*TEST 71          *TEST CLOCK B'S COUNT REGISTER WITH 252 PATTERN
3717          ;
3718          ;*
3719          ;*CLOCK B COUNT REGISTER BIT EXERCISE. ON FAILURE-SUSPECT INDIVIDUAL
3720          ;*F/FS OR GATES
3721          ;*
3722          ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 OCCURANCES PER PASS
3723          ;*
3724          ;*
3725          ;*
3726          ;: *****
3727          ;ST71: SCOPE *****
3728 011606 000004          MOV      #100, $TIMES           ;;DO 100 ITERATIONS
3729 011610 012737 000100 001166          ;SELECT MODE 0.
3730
3731          CLR      $GDDAT
3732 011616 005037 001124          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
3733          ;*      MOV      $GDDAT, @BSR           ;LOAD THE BUFFER REGISTER WITH
3734                                         ;PATTERN 252. IT WILL BE
3735                                         ;TRANSFERRED TO THE COUNT REGISTER
3736
3737

```

```

3738                                     ;SINCE THIS IS MODE 0.
3739
3740 011632 012737 000252 001124          MOV     #252,$GDDAT          ;SET EXPECTED TO PATTERN IN CASE OF
3741                                     ;*
3742                                     ;* MOV     $GDDAT,2BBR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
3743                                     ;NEED OF ERROR TIMEOUT.
3744                                     ;READ THE COUNT REGISTER
3745
3746                                     ;* MOV     2BCR,$BDDAT          ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
3747
3748 011660 023737 001124 001126          CMP     $GDDAT,$BDDAT      ;DID ALL THE BITS AND NO OTHER BITS
3749                                     ;COME THROUGH?
3750 011666 001401                          BEQ     1$                 ;BR IF YES TO NEXT TEST.
3751
3752

```

;;; \$ ERROR << \$

```

3756 011670 104007                          ERROR 7                   ;DATA ERROR CLOCK B - PATTERN "252"
3757                                     ;FAILED TO TRANSFER PROPERLY BETWEEN
3758                                     ;BUFFER AND COUNT REGISTERS.
3759
3760

```

;;; \$ ERROR << \$

```

3764 011672                                1$:
3765
3766                                     ;*****
3767                                     ;*TEST 72          *TEST THE SETTING OF MAINTENANCE STP1 IN CLOCK A BIT 15 TO SET
3768                                     ;*
3769                                     ;*NEW SIGNALS   GENERATION OF "STP1" BY "LD STAT A" H + "BD 12" H
3770                                     ;*
3771                                     ;* PROBABLE SYNC POINT FOR THIS TEST:: "DEVICE OUT" 2 PER PASS
3772                                     ;*
3773                                     ;*
3774                                     ;*****
3775

```

ST72: SCOPE

```

3776 011672 000004                          CLR     $GDDAT
3777
3778 011674 005037 001124                    ;* MOV     $GDDAT,2ASR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3779                                     ;*
3780                                     ;* MOV     2ASR,$GDDAT          ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
3781                                     ;MAKE SURE THE STATUS REGISTER IS CLEAR.
3782                                     ;SET MAINTENANCE STP1.
3783
3784 011720 012737 010000 001124              MOV     #BIT12,$GDDAT
3785
3786                                     ;* MOV     $GDDAT,2ASR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3787                                     ;DID BIT15 (STP1 FLAG) SET?
3788
3789                                     ;* MOV     2ASR,$BDDAT          ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
3790
3791

```





;;; \$> ERROR << \$

```

3849 012046 005037 001124 1$: CLR $GDDAT ;LEAVE SUBTEST WITH CLOCK CLEAR.
3850 012046 005037 001124 ;* MOV $GDDAT, @ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3851
3852
3853
3854
3855 ;: *****
3856 ;*TEST 74 *TEST THAT CLOCK A WILL INCREMENT - MODE 0 - RATE STP1 FIRST COUNT TEST
3857 ;*
3858 ;*COUNT TEST - THIS IS THE VERY FIST TIME THAT THE COUNTER
3859 ;*HAS BEEN ASKED TO INCREMENT! WHAT WE ARE GOING TO DO IS
3860 ;*CLEAR THE BUFFER, SELECT MODE 0, RATE OF STP1.
3861 ;*NEXT WILL GENERATE THE STP1 THROUGH MAINTENANCE MODE (WE'VE
3862 ;*DONE THIS BEFORE IN A PREVIOUS TEST TO SEE IF THE FLAG WOULD SET)
3863 ;*AND SEE IF THE COUNTER HAS INCREMENTED.
3864 ;*
3865 ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
3866 ;*
3867 ;*
3868 ;: *****
3869 012062 000004 †ST74: SCOPE
3870
3871 ;: CLEAR CLOCK A.
3872 ;: CLEAR BUFFER REGISTER.
3873 012064 005037 001124 CLR $GDDAT
3874 ;* MOV $GDDAT, @ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3875 ;* MOV $GDDAT, @ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
3876 ;: SELECT: MODE0! RATE "STP1" AND ENABLE
3877 ;: CLOCK A TO COUNT.
3878 ;: NOW GENERATE A MAINTENANCE STP1 - AT
3879 ;: THIS TIME THE CLOCK SHOULD COUNT ONCE.
3880
3881 012110 012737 000015 001124 MOV #15, $GDDAT
3882 ;* MOV $GDDAT, @ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3883 ;* MOV @ASR, $GDDAT ;/READ DEVICE REG ASR, PUT DATA IN $GDDAT.
3884 ;* BIS #BIT12, $GDDAT
3885
3886 012136 052737 010000 001124 ;* MOV $GDDAT, @ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
3887 ;* MOV #1, $GDDAT ;: FOR ERROR TYPEOUT (IF NEEDED) SET THE #1.
3888 ;: READ THE COUNT REGISTER - SHOULD=1.
3889
3890 012154 012737 000001 001124 ;* MOV @ACR, $BDDAT ;/READ DEVICE REG ACR, PUT DATA IN $BDDAT.
3891 ;* CMP $BDDAT, $GDDAT ;: DID THE COUNTER COUNT ONCE?
3892 ;* BEQ 1$ ;: IF YES - BR NEXT TEST.
3893
3894 012172 023737 001126 001124
3895 012200 001401
3896
3897

```

;;; \$> ERROR << \$

```

3901 012202 104011          ERROR 11          ;ERROR - COUNT A FAILED TO COUNT
3902                                     ;ONCE, WHEN ENABLED, MODE 0
3903                                     ;RATE "STP1" SEE ABOVE COMMENTS
3904                                     ;FOR COMPLETE DESCRIPTION AND LIST
3905                                     ;OF EVENTS.
3906
3907

```

::: \$> ERROR << \$

```

3911 012204          1$:
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3933 012204 000004
3934 012206 012737 000001 001166
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3936 012214 005037 001124
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3940 012220
3941 012220 005037 001356
3942
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3944
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3950
3951 012244 012737 000015 001356
3952
3953

```

```

*****
*TEST 75          *TEST THE ABILITY OF CLOCK A TO COUNT FROM ZERO TO OVERFLOW USING M STP1
*
*IN THIS TEST WE'LL COUNT THE COUNTER THROUGH EACH STEP
*FROM ZERO TO OVERFLOW USING MAINTENANCE "STP1" COUNTS.
*IT IS KNOWN THAT THE COUNTER WILL INCREMENT ONCE USING
*THE MAINTENANCE STP1 AND THAT THE COUNTER F/FS WILL
*PASS ALL DATA BITS.
*UNKNOWN IS THE ABILITY OF THE F/F'S TO PROPAGATE THEIR
*OVERFLOWS.
*
*IF IT IS DESIRED TO START THIS TEST AT A VALUE OTHER THAN
*ZERO, CHANGE THE SECOND INSTR. OF THIS TEST TO A VALUE TO BE
*LOADED INTO THE BUFFER TO THAT VALUE DESIRED.
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*****
ST75:  SCOPE
      MOV      #1,$TIMES          ;;DO 1 ITERATION
      CLR      $GDDAT ;START THE COUNTER FROM ZERO.
      ;NOTE: A VALUE OTHER THAN ZERO MAY BE
      ;PATCHED IN HERE IN ORDER THAT A COUNT
      ;MAY BE STARTED HIGHER.
      ;DISABLE CLOCK A.
      CLR      $TMDAT
      ;*      MOV      $TMDAT,$ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
      ;*      MOV      $GDDAT,$ABR     ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
      ;LOAD THE COUNTER BUFFER WITH VALUE.
      ;"1$" IS THE LOOP BACK POINT ON
      ;"LOOP ON TEST" (SW14=1) FEATURE. NOWMAL
      ;LOOP BACK POINT WILL BE "2$".
      MOV      #15,$TMDAT
      ;*      MOV      $TMDAT,$ASR     ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR

```

















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013262 000004  
013264 012737 000020 001166  
013272 005037 001124  
013316 012737 000011 001124  
013334 005000  
013336 005200  
013340 001376  
013352 005737 001126  
013356 001011  
013370 032737 000040 001126  
013376 001001  
013400 104012  
013402

```
;/#
*****
*TEST 103 *TEST THE ABILITY OF CLOCK A TO COUNT AT 1KHZ RATE PART 1
*THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
*IN RATE: 1KHZ PART 1
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*****
↑ST103: SCOPE
MOV #20,$TIMES ;;DO 20 ITERATIONS
; /MAKE SURE CLOCK IS CLEAR.
; /CLEAR THE BUFFER.
; /SELECT: MODE 0, RATE 1KHZ ; GO.
CLR $GDDAT
;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
;* MOV $GDDAT,$ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
MOV #1:10,$GDDAT
;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
CLR RO ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
INC RO ;/WILL AMOUNT TO 369MS ON A PDP-11/20
BNE 1$ ;/DID COUNTER INCREMENT AT ALL?
;* MOV $ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 2$ ;/IF YES - BR NEXT TEST.
; /COUNTER MAY HAVE HAD TIME TO OVERFLOW.
;* MOV $ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
BIT #BIT05,$BDDAT
; /AT HIGH RATE - SO WE'LL SEE IF "OVERFLOW"
; /F/F HAD SET.
; /BR IF YES NEXT TEST.
BNE 2$
;;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
013400 104012 ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO
; /COUNT RATE: 1KHZ.
;;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
2$:
```

4354 013402

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013402 000004  
013404 012737 000020 001166  
  
013412 005037 001124  
  
013436 012737 000013 001124  
  
013454 005000  
013456 005200  
013460 001376  
  
013472 005737 001126  
013476 001011  
  
013510 032737 000040 001126  
  
013516 001001

```
;/#
*****
*TEST 104 *TEST THE ABILITY OF CLOCK A TO COUNT AT 100HZ RATE PART 1
*THIS TEST IS DESIGNED TO TEST CLOCK A'S ABILITY TO COUNT
*IN RATE: 100HZ PART 1
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*****
TST104: SCOPE
MOV #20,$TIMES ;;DO 20 ITERATIONS
;;MAKE SURE CLOCK IS CLEAR.
;;CLEAR THE BUFFER.
;;SELECT: MODE 0, RATE 100HZ ; GO.
CLR $GDDAT
;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
;* MOV $GDDAT,$ABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
MOV #1!12,$GDDAT
;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
CLR RO ;/NOW WE'LL DO A LITTLE DELAY: THIS DELAY
1$: INC RO ;/WILL AMOUNT TO 369MS ON A PDP-11/20
BNE 1$ ;/DID COUNTER INCREMENT AT ALL?
;* MOV $ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST $BDDAT
BNE 2$ ;/IF YES - BR NEXT TEST.
;/COUNTER MAY HAVE HAD TIME TO oVERFLOW.
;* MOV $ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
BIT #BIT05,$BDDAT ;/AT HIGH RATE - SO WE'LL SEE IF "OVERFLOW"
;/F/F HAD SET.
BNE 2$ ;/BR IF YES NEXT TEST.
```

;;; \$> ERROR << \$

4401 013520 104012 ERROR 12 ;/ERROR CLOCK A COUNTER FAILED TO  
4402 ;/COUNT RATE: 100HZ.  
4403

;;; \$> ERROR << \$

4407 013522 2\$:



4462  
4463  
4464  
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4500  
4501  
4502  
4503  
4504

013642 000004  
013644 012737 000050 001166  
  
013652 005037 001124  
  
013676 005237 001124  
  
013712 005000  
013714 005200  
013716 001376  
  
013730 005737 001126  
013734 001010  
  
013746 032737 000040 001126  
013754 001401

```
*****
; *TEST 106      *TEST THAT CLOCK A DOESN'T COUNT WHEN NO RATE IS SELECTED
; *
; *WE KNOW THAT CLOCK A COUNTS AT ALL
; *ITS RATES, SO LETS BE SURE IT DOESNT
; *COUNT WHEN NO RATE IS SELECTED. ON
; *ERROR SUSPECT DUAL RATE SELECTION.
; *
; * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
; *
*****
```

```
TST106: SCOPE
MOV      #50,$TIMES      ;;DO 50 ITERATIONS
                           ;CLEAR CLOCK A.
                           ;ZERO ITS BUFFER.
                           ;TELL THE CLOCK TO GO!
                           ;
CLR      $GDDAT
; *      MOV      $GDDAT,$ASR      ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
; *      MOV      $GDDAT,$ABR      ; / PUT DATA FROM $GDDAT TO DEVICE REG ABR
INC      $GDDAT
; *      MOV      $GDDAT,$ASR      ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
                           ; NO RATE SELECTED.
                           ;
1$:      CLR      R0
INC      R0
BNE     1$
                           ; ANY COUNT OCCUR?
; *      MOV      @ASR,$BDDAT      ; /READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST     $BDDAT
BNE     2$
                           ; IF COUNTER HAS SOMETHING IN IT REPORT ERROR
; *      MOV      @ASR,$BDDAT      ; /READ DEVICE REG ASR,PUT DATA IN $BDDAT.
BIT     #BIT05,$BDDAT     ; IF THE OVERFLOW BIT SET THEN IT MUST
                           ; HAVE COUNTED.
BEQ     3$
```

;;; \$ ERROR << \$

013756 104012

```
2$:      ERROR      12
                           ; AH HA! ERROR CLOCK A COUNTED WHEN
                           ; ENABLED-BUT-NO-RATE SELECTED
                           ; BETTER FIND OUT HOW CAUSED SIGNAL:
                           ; "CLOCK A" L.
```

;;; \$ ERROR << \$

4508  
4509  
4510  
4511  
4512

4516 013760

3\$:

4517  
4518  
4519  
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4522  
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4561

013760 000004

```
*****  
*TEST 107 *TEST THAT CLOCK A'S COUNT REG ISN'T LOADED WHEN CLOCK A IS ENABLED  
*  
*IN THIS TEST WE'LL FIND OUT IF F/F "ENB CNTR A" WHEN SET,  
*INHIBITS LOADING OF CLOCK A'S COUNT REGISTER  
*THE LOADING OF THE COUNT REGISTER IS A FUNCTION OF:  
*"ENB CNTR (0)" H + "BUFFER LOAD" H  
*  
*  
* PROBABLE SYNC POINT FOR THIS TEST:: "RD STAT B"  
*  
*****  
↑ST107: SCOPE
```

```
;GENERATE A SYNC PULSE  
;CLEAR CLOCK A'S STATUS REG.  
;CLEAR CLOCK A'S BUFFER REG. NOTE  
;THIS WILL ALSO CAUSE ZEROS TO BE  
;LOADED INTO THE COUNT REG.
```

```
;* MOV QBSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
TST $BDDAT  
CLR $GDDAT  
;* MOV $GDDAT,QASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV $GDDAT,QABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
INC $GDDAT ;SET THE ENABLE F/F. THIS  
;* MOV $GDDAT,QASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;FROM BEING LOADED WHEN THE  
;BUFFER IS LOADED.  
014036 012737 177777 001124 MOV #177777,$GDDAT ;NOW LOAD THE BUFFER REG.  
;* MOV $GDDAT,QABR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR  
;TO THE COUNT REGISTER.  
;DID ANY BITS GET TRANSFERRED TO  
;THE COUNT REGISTER?  
;* MOV QACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
TST $BDDAT  
014064 005737 001126 BEQ IS ;BR IF NO - NEXT TEST.  
014070 001401
```

::: \$> ERROR << \$

4565 014072 104012 ERROR 12 ;ERROR CLOCK A BUFFER TO COUNT REG TRANSFER  
4566 ;OCCURRED EVEN THOUGH THE "ENB CNTR A" F/F  
4567 ;WAS SET.  
4568

::: \$> ERROR << \$



4624  
4625  
4626  
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4677

014216 000004

```

*****
*TEST 111      *TEST THAT A CLOCK A "BUFFER TO COUNT REG" DOESN'T TAKE PLACE ON A MODE
*
*THIS WILL BE THE FIRST TIME WE'VE DONE A MODE 2 OPERATION
*ON CLOCK A. THE FUNCTION OF THIS TEST WILL BE TO MAKE
*SURE A BUFFER TO COUNT REGISTER DOESN'T TAKE PLACE ON OVERFLOW
*THE COMBO THAT GAVE US BUFFER TO COUNT REG ON OVERFLOW BEFORE
*IS ["MODE A1 (0)" H + "A RELOAD" H]. WE'LL STILL BE GENERATING
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*
*"A RELOAD" H BUT SHOULD NOT GET."MODE A1 (0)" H AS THIS IS MODE 2.
*
*****
TST111: SCOPE

```

```

;MAKE SURE CLOCK A IS CLEAR.
;SET BUFFER + COUNT REG TO -1 FROM OVERFLOW.
;SET: MODE 2; RATE STP1: GO.
;CAUSE A MAINTENANCE STP1 - CLOCK ONCE.
;THIS SHOULD CAUSE AN OVERFLOW AND LEAVE
;THE COUNT REGISTER CLEAR AS A
;BUFFER TO COUNT REG. SHOULDN'T OCCUR.
;IS THE COUNT REG. CLEAR?

```

014220 005037 001124

CLR SGDDAT

014234 012737 177777 001124

```

;* MOV SGDDAT,ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
MOV #177777,SGDDAT

```

014252 012737 001015 001124

```

;* MOV SGDDAT,ABR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ABR
MOV #1015,SGDDAT

```

014300 052737 010000 001124

```

;* MOV SGDDAT,ASR ;/ PUT DATA FROM SGDDAT TO DEVICE REG ASR
;* MOV ASR,SGDDAT ;/READ DEVICE REG ASR,PUT DATA IN SGDDAT.
BIS #BIT12,SGDDAT

```

014326 005737 001126

```

;* MOV ASR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
TST $BDDAT

```

014332 001401

BEQ IS ;BR IF YES TO NEXT TEST.

;;; \$ >> ERROR << \$

014334 104012

ERROR 12

```

;ERROR THE CONTENTS OF THE BUFFER REG.
;GOT TRANSFERRED TO THE COUNT REG.
;(CLOCK A) ON OVERFLOW DOING A
;MODE 2 OPERATION.
;THERE'S AN OUTSIDE CHANCE THAT THE

```



```

4678 ;COUNT REG. NEVER GOES TO ZERO ON
4679 ;AN OVERFLOW - THIS IS THE FIRST TIME
4680 ;THAT WE WERE ABLE TO LOOK AT IT ON
4681 ;OVERFLOW BECAUSE MODES 0 + 1 CAUSED
4682 ;THAT AUTOMATIC BUFFER TO COUNT REG.
4683

```

::: \$ >> ERROR << \$

4687 014336 15:

```

4688
4689
4690
4691 ;*****
4692 ;*TEST 112 *TEST THAT CLOCK A MODE 2 + MAINTENANCE ST2 SET MODE FLG
4693 ;*
4694 ;*NOW WE'LL SEE IF CAN GENERATE A "CNTR TO BUFF" H SIGNAL.
4695 ;*TO DETECT IT, WE'RE GOING TO DEPEND ON IT SETTING THE MODE FLAG,
4696 ;*CLOCK A CSR BIT07. ["MODE A1 (0)" H + "ST2 (1)" H] + "TPO" L="CNTR TO BUFF" H.
4697 ;*BEING IN MODE 2, SHOULD GIVE US "MODE A1 (1)" H. WELL GET ST2 (1) H
4698 ;*BY GENERATING A MAINTENANCE "ST2". TPO COMES FROM THE INTERNAL
4699 ;*CLOCK PAGE.
4700 ;*
4701 ;* PROBABLE SYNC POINT FOR THIS TEST:: "RD STAT B"
4702 ;*
4703 ;*****

```

```

4704 014336 000004 TST112: SCOPE
4705
4706 ;GENERATE A SYNC PULSE
4707
4708 ;* MOV @BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
4709 014350 005737 001126 TST $BDDAT
4710 ;MAKE SURE CLOCK A'S STAT REG IS CLEAR.
4711 014354 005037 001124 CLR $GDDAT
4712
4713 ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
4714 ;SET MODE 2.
4715 ;GENERATE MAINTENANCE ST2.
4716 ;THE COMBO OF MODE 2 + ST2 SHOULD
4717 ;GET "CNTR TO BUFF" H WHICH SHOULD
4718 ;SET "MODE FLG" F/F.
4719 014370 012737 001000 001124 MOV #1000,$GDDAT
4720
4721 ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
4722
4723 ;* MOV @ASR,$GDDAT ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
4724 014416 052737 002000 001124 BIS #BIT10,$GDDAT
4725
4726 ;* MOV $GDDAT,@ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
4727 ;DID IT SET?
4728
4729 ;* MOV @ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
4730 014444 032737 000200 001126 BIT #BIT07,$BDDAT
4731 014452 001001 BNE 15 ;IF YES-BR TO NEXT TEST.

```

4732 ;;;SSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SS

4736 014454 104012 ERROR 12 ;ERROR - MODE 2 + ST2 DID NOT SET MODE FL.  
4737 ;;;SSSSSSSSSSSSSSSSSSSSSSSSSSSS>> ERROR <<SS

4741 014456 1S:  
4742  
4743 :;\*\*\*\*\*  
4744 :;\*TEST 113 \*TEST THAT PATTERN 052525 CAN BE XFERRED BETWEEN A'S COUNT-BUFFER REGS  
4745 :;\*  
4746 :;\*NOW WE'LL SHOT THE WORKS - WE KNOW FROM THE PREVIOUS TEST WE  
4747 :;\*CAN GENERATE "CNTR TO BUFF" H FROM MODE 2 + MAINTENANCE ST2, NOW  
4748 :;\*WE WELL TRY AND GENERATE A TRANSFER BETWEEN THE COUNTER AND BUFFER  
4749 :;\*USING A CB PAT PATTERN.  
4750 :;\*IF NO DATA PATTERN GETS TRANSFERRED, SUSPECT SIG "LD BUFFER"  
4751 :;\*TO BE STUCK LOW AT THE MUX INPUT FOR THE BUFFER OR  
4752 :;\*"CNTR TO BUFF" H NOT GETTING THROUGH TO THE LOAD INPUTS OF THE  
4753 :;\*BUFFER REGISTER.  
4754 :;\*IF JUST ONE OR A FEW BITS GETS MESSUED UP ON THE XFERR-  
4755 :;\*SUSPECT THE RESPECTIVE MUX OR ETCH BETWEEN THE COUNT REG  
4756 :;\*AND MUX. GOOD LUCK.  
4757 :;\*  
4758 :;\* PROBABLE SYNC POINT FOR THIS TEST:: "RD STAT B"  
4759 :;\*  
4760 :;\*  
4761 :;\*  
4762 :;\*\*\*\*\*  
4763 014456 000004 †ST113: SCOPE

```
4764 ;GENERATE A SYNC PULSE
4765 ;
4766 ;
4767 ;*      MOV      BSR, $BDDAT      ;/READ DEVICE REG BSR, PUT DATA IN $BDDAT.
4768 014470 005737 001126      TST      $BDDAT
4769 ;
4770 ;MAKE SURE CLOCK A IS CLEAR.
4771 ;PUT PATTERN 052525 INTO BUFFER REG.
4772 ;IT SHOULD GET XFERRED TO COUNT REG.
4773 ;SELECT: MODE 2, ENABLE.
4774 014474 005037 001124      CLR      $GDDAT      ;NOW GENERATE A MAINTENANCE ST2.
4775 ;
4776 ;*      MOV      $GDDAT, BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
4777 014510 012737 052525 001124      MOV      #052525, $GDDAT
4778 ;
4779 ;*      MOV      $GDDAT, ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
4780 014526 012737 001001 001124      MOV      #1001, $GDDAT
4781 ;
4782 ;*      MOV      $GDDAT, BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
4783 014544 005037 001124      CLR      $GDDAT
4784 ;
4785 ;*      MOV      $GDDAT, ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
```



```

4840                                     ; IT SHOULD GET XFERRED TO COUNT REG.
4841                                     ; SELECT: MODE 2, ENABLE.
4842                                     ; NOW GENERATE A MAINTENANCE ST2.
4843 014654 005037 001124          CLR      $GDDAT
4844
4845                                     ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR.
4846 014670 012737 125252 001124  ; *      MOV      $GDDAT, @ASR
4847                                     MOV      #125252, $GDDAT
4848                                     ; / PUT DATA FROM $GDDAT TO DEVICE REG ABR
4849 014706 012737 001001 001124  ; *      MOV      $GDDAT, @ABR
4850                                     MOV      #1001, $GDDAT
4851                                     ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
4852 014724 005037 001124          ; *      MOV      $GDDAT, @ASR
4853                                     CLR      $GDDAT
4854                                     ; / PUT DATA FROM $GDDAT TO DEVICE REG ABR
4855                                     ; *      MOV      $GDDAT, @ABR
4856                                     ; / READ DEVICE REG ASR, PUT DATA IN $GDDAT.
4857 014750 052737 002000 001124  ; *      MOV      @ASR, $GDDAT
4858                                     BIS      #BIT10, $GDDAT
4859                                     ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
4860 014766 012737 125252 001124  ; *      MOV      $GDDAT, @ASR
4861                                     MOV      #125252, $GDDAT
4862                                     ; RECORD $GDDAT (PATTERN) IN CASE WE
4863                                     ; NEED TO TYPE OUT AN ERROR.
4864                                     ; NOW READ BACK THE BUFFER REG.
4865 015004 023737 001126 001124  ; *      MOV      @ABR, $BDDAT
4866 015012 001401                                     CMP      $BDDAT, $GDDAT
4867                                     BEQ      1$

```

::: \$> ERROR << \$

```

4871 015014 104012          ERROR    12          ; ERROR FAILED TO XFERR 125252 PATTERN
4872                                     ; CORRECTLY FROM COUNT TO BUFFER REG.
4873                                     ; SEE INIT. COMMENT AS TO WHY
4874                                     ; IT MIGHT HAVE GONE SOUR.
4875

```

::: \$> ERROR << \$

```

4879 015016          1$:          P=P+1
4880 000012
4881
4882
4883
4884
4885
4886
4887
4888
4889
4890
4891
4892
4893

```

```

: *****
: *TEST 115 *TEST THAT A'S COUNT REGISTER ISN'T CLEARED IN MODE 1 WHEN STP2 IS GENER
: *
: *THIS TEST IS DESIGNED TO MAKE SURE THAT WE DON'T CLEAR THE COUNT
: *REGISTER IN MODE 1 WHEN AN STP2 IS GENERATED.
: *
: * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
: *
: *
: *****

```





```

5002 015260 012737 001400 001124      MOV      #1400,$GDDAT
5003
5004      ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
5005 015276 012737 177777 001124      MOV      #177777,$GDDAT
5006
5007      ;*      MOV      $GDDAT,@ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
5008
5009      ;*      MOV      @ASR,$GDDAT      ;/READ DEVICE REG ASR,PUT DATA IN $GDDAT.
5010 015324 052737 002000 001124      BIS      #BIT10,$GDDAT
5011
5012      ;*      MOV      $GDDAT,@ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
5013
5014      ;*      MOV      @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
5015 015352 005737 001126      TST     $BDDAT
5016 015356 001401      BEQ     1$      ;BR IF YES - NEXT TEST.
5017

```

;;; \$ > ERROR << \$

```

5021 015360 104012      ERROR 12      ;ERROR-CLOCK A-COUNT REGISTER FAILED TO
5022      ;CLEAR IN MODE 3 ON "STP2" PULSE.
5023

```

;;; \$ > ERROR << \$

```

5027 015362      1$:
5028
5029

```

```

5030      ; *****
5031      ; *TEST 120      *TEST THE AUTODECREMENT FEATURE OF CLOCK A'S BUFFER
5032
5033      ; *THIS IS GOING TO BE A BIGGIE-WITH TWO PARTS.
5034      ; *PART1:      WE'RE LOADING THE BUFFER WITH ALL ONES; MODE 0; RATE STP1
5035      ; *            WITH "AUTO INC (1)" SET (FOR FIRST TIME!). NOW WE'LL GENERATE
5036      ; *            THE THING TO WATCH FOR IS THE EXPLOSIVE COMBO OF
5037      ; *            "MODE A0 (0)" H + "MODE A1 (0)" H (MODE 0) + "AUTO INC (1)" H +
5038      ; *            "A OVERFLOW" ALL FEEDING THE DOWN COUNT SIDE OF THE 74193 CHIP.
5039      ; *            THE RESULTS SHOULD BE 177776.
5040      ; *PART2:      IF PART 1 WAS SUCCESSFUL WE'LL LOOK TO SEE IF
5041      ; *            THE COUNTER GOT LOADED WITH THE NEW VALUE 177776.
5042      ; *            THE HANG-UP HERE IS THAT "A OVERFLOW" FEEDS A ONE SHOT
5043      ; *            THAT GENERATES "A RELOAD" H. WE KNOW THAT WE CAN
5044      ; *            GET "A RELOAD" H BUT THE BIG TEST HERE IS SEEING IF THAT
5045      ; *            ONE SHOT SPITS OUT "A RELOAD" H TOO SOON TO CATCH THE BUFFER
5046      ; *            WITH ITS PANTS DOWN AS ITS DECREMENTING ITSELF.
5047
5048
5049      ; * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
5050      ; *****

```

```

5051
5052 015362 000004
5053
5054
5055

```

```

;ST120: SCOPE

```

```

;MAKE SURE CLOCK B IS CLEAR.
;MAKE SURE CLOCK A IS CLEAR.

```





```
5111 015542 1$: ;PART 2 DID NEW COUNT GET TRANSFERRED TO COUNT REGISTER?  
5112 ;  
5113 ;READ THE COUNT REGISTER  
5114 ;  
5115 015552 023727 001126 177776 ;* MOV $ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.  
5116 015552 023727 001126 177776 ;* CMP $BDDAT,#177776 ;DID NEW VALUE OF THE BUFFER  
5117 ; REGISTER GET PROPERLY LOADED INTO  
5118 ; THE COUNT REGISTER?  
5119 015560 001401 BEQ 2$ ;BR IF YES - NEXT TEST.  
5120  
; ; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

```
5124 015562 104012 ERROR 12 ;ERROR CLOCK A. NEW CONTENTS OF  
5125 ; BUFFER REGISTER FAILED TO BE PROPERLY  
5126 ; LOADED INTO COUNT REGISTER AFTER  
5127 ; AUTO DECREMENT.  
5128 ; SEE ABOVE COMMENTS FOR SEQUENCE OF EVENTS.  
5129  
; ; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
```

```
5133 015564 005037 001124 2$: CLR $GDDAT ;CLEAR AUTO INC OPTION.  
5134 015564 005037 001124  
5135 ;  
5136 ;* MOV $GDDAT,$BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
5137  
5138 ;*****  
5139 ;*TEST 121 *TEST THAT CLOCK A'S 1 MHZ CLK CAN BE DISABLED  
5140 ;*  
5141 ;*FOR THIS TEST, WE'LL TRY DISABLING THE 1 MHZ CLOCK. TO DO THIS,  
5142 ;*WE'LL SET THE "DISABLE OSC 1 MHZ" BIT 11 IN CLOCK B SR. THEN  
5143 ;*COUNTED OR OVERFLOWED, IF SO ERROR.  
5144 ;*THE UNKNOWN THING HERE IS BIT 11 SETTING THE DISABLE F/F THAT  
5145 ;*GATES WITH THE 1 MHZ FREQ TO PRODUCE "A 1 MHZ CLK" L  
5146 ;*  
5147 ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"  
5148 ;*  
5149 ;*****  
5150 015600 000004 $T121: SCOPE  
5151 015602 012737 000100 001166 MOV #100,$TIMES ;;DO 100 ITERATIONS  
5152  
5153 ;CLEAR CLOCK A.  
5154 ;SET THE "DISABLE OSC 1 MHZ" F/F.  
5155 ;CLEAR THE BUFFER + COUNT REGS.  
5156 ;START CLOCK: RATE 1 MHZ, MODE 0, GO.  
5157 015610 005037 001124 CLR $GDDAT  
5158 ;  
5159 ;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
5160 015624 012737 004000 001124 ;* MOV #BIT11,$GDDAT  
5161 ;* MOV $GDDAT,$BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
5162 015642 005037 001124 ;* CLR $GDDAT  
5163
```

```
5164
5165      015656  012737  000003  001124  ;*      MOV      $GDDAT,2ABR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ABR
5166      MOV      #3,$GDDAT
5167
5168      ;*      MOV      $GDDAT,2ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
5169      015674  005000      CLR      RD          ;SHORT DELAY. WE ALLOW THIS DELAY TO
5170      015676  105200      INCB    RD          ;OCCUR. IF THE 1 MHZ CLOCK IS DISABLED
5171      015700  100376      BPL     1$          ;NO CLOCKING OF CLOCK A WILL OCCUR.
5172                                     ;SEE SOMETHING IN THE COUNT REGISTERS
5173
5174      ;*      MOV      2ACR,$BDDAT     ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
5175      015712  005737  001126      TST     $BDDAT     ;DOES COUNT REG HAVE ANYTHING IN IT?
5176      015716  001007      BNE     2$          ;YES - REPORT ERROR!
5177
5178      ;*      MOV      2ASR,$BDDAT     ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
5179      015730  105737  001126      TSTB   $BDDAT     ;NO - BR NEXT TEST - NO ERROR.
5180      015734  100001      BPL     3$
5181
; ; ; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ > ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
5185      015736  104012      2$ :   ERROR    12          ;ERROR - UNABLE TO DISABLE 1 MHZ CLK
5186                                     ;USING "DISABLE OSC 1 MHZ" F/F
5187
; ; ; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ > ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
5191
5192      015740  005037  001124      3$ :   CLR      $GDDAT      ;CLEAR CLOCK A.
5193      ;*      MOV      $GDDAT,2ASR     ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
5194
```

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.SBTTL \*  
.SBTTL \* PHASE 4 CLOCK B COUNT FUNCTION TESTS  
.SBTTL \*

```

*****
*TEST 122      *TEST THAT CLOCK B WILL COUNT ONCE FIRST CLOCK B COUNT
*
*VERY FIRST TIME COUNTING WITH CLOCK B.
*WHAT WE'LL TRY AND DO IS COUNT IT FROM 0 TO 1.
*WE DO HAVE A PROBLEM HERE HOWEVER. WE CAN'T READ CLOCK B AS IT
*COUNTS AND THERE IS NO NICE WAY OF GENERATING A "CLOCK B" L PULSE.
*SO WE'RE GOING TO HAVE TO DO A COUPLE TRICKY THINGS: (1) DISABLE
*CLOCK A'S 1 MHZ CLOCK (WE DID THAT IN LAST TEST) SO THAT WE CAN
*GENERATE A MAINTENANCE 1 MHZ PULSE THROUGH CLOCK A (NEVER
*DID THAT BEFORE); (2) SET CLOCK B "FEED B TO A" BIT 05 (NEVER DID THAT
*BEFORE EITHER) SO THAT WE CAN ROUTE "A 1 MHZ" H TO MAKE
*"B 1 MHZ" L TO GIVE US "CLOCK B" L
    
```

\* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"

```

*****
*ST122: SCOPE
    
```

015754 000004

; CLEAR CLOCK B AND DISABLE 1MHZ OSC.

015756 012737 004000 001124

```

MOV    #BIT11,$GDDAT
;*    MOV    $GDDAT,$BSR
    
```

```

;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
; CLEAR B'S BUFFER + COUNT REGS.
; SELECT "FEED B TO A", RATE 1 MHZ, GO.
    
```

015774 005037 001124

```

CLR    $GDDAT
;*    MOV    $GDDAT,$BBR
    
```

```

;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
; CLOCK A'S 1 MHZ CLOCK.
; GENERATE A MAINTENANCE 1 MHZ PULSE..
; DID COUNTER COUNT?
    
```

016020 052737 000043 001124

```

;*    MOV    $BSR,$GDDAT
BIS    #BITS!BIT1!BIT0,$GDDAT
;*    MOV    $GDDAT,$BSR
    
```

;/ READ DEVICE REG BSR, PUT DATA IN \$GDDAT.

016046 052737 004000 001124

```

;*    MOV    $ASR,$GDDAT
BIS    #BIT11,$GDDAT
;*    MOV    $GDDAT,$ASR
    
```

;/ READ DEVICE REG ASR, PUT DATA IN \$GDDAT.

016074 005737 001126

```

;*    MOV    $BCR,$BDDAT
TST    $BDDAT
BNE    1$
    
```

;/ READ DEVICE REG BCR, PUT DATA IN \$BDDAT.

016100 001001

; BR IF YES TO NEXT TEST.

;;; \$ > ERROR < \$



```

5303
5304
5305          ;*      MOV      $GDDAT, @BBR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
5306                                     ;SELECT: "DISABLE OSC 1 MHZ"; "FEED B TO A";
5307                                     ;RATE 1 MHZ.
5308                                     ;GO. ENABL MUST BE SET AFTER "FEED B TO A"
5309 016162 012737 004042 001356          MOV      #4042, $TMDAT
5310
5311          ;*      MOV      $TMDAT, @BSR          ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
5312 016200 005237 001356          INC      $TMDAT
5313
5314          ;*      MOV      $TMDAT, @BSR          ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
5315
5316 016214          2$:          ;GENERATE A CLOCK PULSE.
5317                                     ;SHOULD CAUSE THE CLOCK TO
5318                                     ;INCREMENT ONCE.
5319
5320          ;*      MOV      @ASR, $TMDAT          ;/READ DEVICE REG ASR, PUT DATA IN $TMDAT.
5321 016224 052737 004000 001356          BIS      #BIT11, $TMDAT
5322
5323          ;*      MOV      $TMDAT, @ASR          ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
5324 016242 005237 001124          INC      $GDDAT          ;$GDDAT IS USED TO KEEP TRACK OF THE
5325                                     ;VALUE THE CLOCK SHOULD COUNT TO.
5326
5327
5328          ;*      MOV      @BCR, $BDDAT          ;/READ DEVICE REG BCR, PUT DATA IN $BDDAT.
5329
5330 016256 123737 001126 001124          CMPB    $BDDAT, $GDDAT  ;DID THE COUNT OCCUR CORRECTLY?
5331 016264 001402          BEQ      3$          ;IF YES - BR "3$".
5332

```

::: \$ >> ERROR << \$

```

5336 016256 104015          ERROR    15          ;ERROR CLOCK B FAILED TO UPCOUNT
5337                                     ;CORRECTLY - SEE COMMENTS AT SUB-TEST
5338                                     ;HEADING FOR MORE DETAILS.
5339

```

::: \$ >> ERROR << \$

```

5343 016270 000403          BR      4$
5344
5345 016272 105737 001124          3$:      TSTB    $GDDAT          ;DID WE ACHIEVE OVERFLOW YET?
5346 016276 001410          BEQ      5$          ;
5347
5348 016300 032777 040000 162632          4$:      BIT      #BIT14, @SWR          ;LOOP ON CURRENT COUNT?
5349 016306 001742          BEQ      2$          ;BR IF NO TO NEXT COUNT UPDATE.
5350 016310 162737 000001 001124          SUB     #1, $GDDAT          ;IF YES DECREMENT EXPECTED AND RELOAD.
5351 016316 000700          BR      1$          ;GO TO rELOAD POINT
5352
5353 016320          5$:          ;END SUBTEST.
5354
5355
5356

```

::: \*\*\*\*\*









```

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5481 016612 000004
5482 016614 012737 000100 001166
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5489 016622 005037 001124
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5491
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5494
5495
5496 016656 005237 001124
5497
5498
5499 016672 005000
5500 016674 105200
5501 016676 001376
5502
5503
5504
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5507 016710 005737 001126
5508 016714 001401
5509

; ; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ > ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

5513 016716 104014
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5515
5516

; ; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ > ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

5520 016720
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```

```

*****
*TEST 126 *TEST THAT CLOCK B DOESN'T COUNT WHEN NO RATE IS SELECTED
*****
TST126: SCOPE
      MOV #100,$TIMES ;;DO 100 ITERATIONS
           ;
           ;CLEAR CLOCK A.
           ;CLEAR CLOCK B.
           ;ZEROS TO BUFFER + COUNT REGS.
           ;ENABLE COUNTER TO COUNT - RATE - 0
           ;(NO RATE).
      CLR $GDDAT
           ;
           ;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
           ;* MOV $GDDAT,$BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
           ;* MOV $GDDAT,$BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
           ;
           ;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
           ;*   CLR RO ;/ DELAY FOR ANY COUNT THAT
           ;*   INCB RO ;/ COULD FALSELY OCCUR.
           ;*   BNE 1$ ;/ THIS DELAY APPROX. 369 MS ON A
           ;*      ;/ PDP 11/20.
           ;
           ;DID ANY COUNT OCCUR?
           ;* MOV $ACR,$BDDAT ;/ READ DEVICE REG ACR,PUT DATA IN $BDDAT.
           ;* TST $BDDAT
           ;* BEQ 2$ ;/ IF NO BR TO NEXT TEST.
    
```

;; \$ > ERROR << \$

ERROR - CLOCK B COUNTED WHEN ENABLED BUT NO RATE SELECTED. BETTER FIND OUT WHATS GENERATING "CLOCK B" L PULSES.

;; \$ > ERROR << \$

2\$:

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;/\*

```
*****
*TEST 127 *TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
*IN RATE: 1MHZ PART1
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"
*
```

```
*****
†ST127: SCOPE
```

```
016720 000004      ;/*
016722 012737 000020 001166    MOV     #20,$TIMES      ;;DO 20 ITERATIONS
                               ;/CLEAR CLOCK A.
016730 005037 001124          CLR     $GDDAT          ;/CLEAR CLOCK B.
                               ;/CLEAR THE BUFFER + COUNT REGS.
                               ;/SELECT: RATE: 1MHZ ; GO.
                               ;*
                               MOV     $GDDAT,$ASR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
                               ;*
                               MOV     $GDDAT,$BSR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
016764 012737 000003 001124    ;*
                               MOV     $GDDAT,$BBR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
                               MOV     #1!2,$GDDAT
                               ;*
                               MOV     $GDDAT,$BSR          ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
017002 005000          CLR     R0              ;/NOW WE'LL DO A LITTLE DELAY.
017004 005200 1$:        INC     R0              ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
017006 001376          BNE     1$             ;/ON A PDP-11/20.
                               ;/DID COUNTER COUNT AT ALL?
                               ;*
                               MOV     @BCR,$BDDAT          ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
                               TST     $BDCAT
                               BNE     2$             ;/BR IF YES - NEXT TEST.
                               ;*
                               MOV     @BSR,$BDDAT          ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
017036 105737 001126          TSTB   $BDDAT
                               ;/COUNT TO OVERFLOW - SO WE'LL SEE IF
                               ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
017042 100401          BMI     2$             ;/BR IF SET - NEXT TEST.
```

;;; \$ > ERROR << \$

```
5573 017044 104014          ERROR    14              ;/ERROR CLOCK B - COUNTER FAILED TO COUNT
5574                               ;/AT 1MHZ RATE.
5575
```

;;; \$ > ERROR << \$

N13

MAINDEC-11-DRLPG-A  
DRLPG.P11 T127

MACY11 27(654) 15-DEC-77 08:29 PAGE 152  
\*TEST THE ABILITY OF CLOCK B TO COUNT AT 1MHZ PART 1

SEQ 0169

5579 017046

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;/#

```

:*****
:*TEST 130      *TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1
:
:*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
:*IN RATE: 100KHZ      PART1
:*
:* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"
:*****
†ST130: SCOPE
MOV      #20,$TIMES      ;;DO 20 ITERATIONS
                               ;/CLEAR CLOCK A.
017046   000004          CLR      $GDDAT      ;/CLEAR CLOCK B.
017050   012737   000020 001166           ;/CLEAR THE BUFFER + COUNT REGS.
017056   005037   001124           ;/SELECT: RATE: 100KHZ ; GO.
; *   MOV      $GDDAT,$ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
; *   MOV      $GDDAT,$BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
; *   MOV      $GDDAT,$BBR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
017112   012737   000005 001124          MOV      #1!4,$GDDAT
; *   MOV      $GDDAT,$BSR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
017130   005000          CLR      R0      ;/NOW WE'LL DO A LITTLE DELAY.
017132   005200          1$: INC      R0      ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
017134   001376          BNE      1$      ;/ON A PDP-11/20.
                               ;/DID COUNTER COUNT AT ALL?
; *   MOV      $BCR,$BDDAT      ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
017146   005737   001126          TST     $BDDAT
017152   001010          BNE      2$      ;/BR IF YES - NEXT TEST.
; *   MOV      $BSR,$BDDAT      ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
017164   105737   001126          TSTB   $BDDAT
                               ;/COUNT TO OVERFLOW - SO WE'LL SEE IF
                               ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
017170   100401          BMI      2$      ;/BR IF SET - NEXT TEST.

```

;;;\$>> ERROR <<\$

017172 104014 ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT ;/AT 100KHZ RATE.

;;;\$>> ERROR <<\$

C14

MAINDEC-11-DRLPG-A  
DRLPG.P11 T130

MACY11 27(654) 15-DEC-77 08:29 PAGE 154  
\*TEST THE ABILITY OF CLOCK B TO COUNT AT 100KHZ PART 1

SEQ 0171

5636 017174

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017174 000004  
017176 012737 000020 001166  
  
017204 005037 001124  
  
  
  
  
  
  
  
  
  
  
  
  
017240 012737 000007 001124  
  
  
  
  
017256 005000  
017260 005200  
017262 001376  
  
  
  
  
  
  
017274 005737 001126  
017300 001010  
  
  
  
017312 105737 001126  
  
  
017316 100401

```
;/#  
*****  
*TEST 131 *TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1  
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT  
*IN RATE: 10KHZ PART1  
* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"  
*  
*****  
↑ST131: SCOPE  
MOV #20,$TIMES ;;DO 20 ITERATIONS  
;/CLEAR CLOCK A.  
CLR $GDDAT ;/CLEAR CLOCK B.  
;/CLEAR THE BUFFER + COUNT REGS.  
;/SELECT: RATE: 10KHZ ; GO.  
;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR  
;* MOV $GDDAT,$BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
;* MOV $GDDAT,$BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR  
MOV #16,$GDDAT  
;* MOV $GDDAT,$BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR  
CLR R0 ;/NOW WE'LL DO A LITTLE DELAY.  
1$: INC R0 ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.  
BNE 1$ ;/ON A PDP-11/20.  
;/DID COUNTER COUNT AT ALL?  
;* MOV $BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
TST $BDDAT  
BNE 2$ ;/BR IF YES - NEXT TEST.  
;* MOV $BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.  
TSTB $BDDAT  
;/COUNT TO OVERFLOW - SO WE'LL SEE IF  
;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.  
BMI 2$ ;/BR IF SET - NEXT TEST.
```

;;; \$>> ERROR <<\$

5687 017320 104014 ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT  
5688 ;/AT 10KHZ RATE.  
5689

;;; \$>> ERROR <<\$

E14

MAINDEC-11-DRLPG-A  
DRLPG.P11 T131

MACY11 27(654) 15-DEC-77 08:29 PAGE 156  
\*TEST THE ABILITY OF CLOCK B TO COUNT AT 10KHZ PART 1

SEQ 0173

5693 017322

25:





G14

MAINDEC-11-DRLPG-A  
DRLPG.P11 T132

MACY11 27(654) 15-DEC-77 08:29 PAGE 158  
\*TEST THE ABILITY OF CLOCK B TO COUNT AT 1KHZ PART 1

SEQ 0175

5750 017450

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```

; / *
*****
*TEST 133 *TEST THE ABILITY OF CLOCK B TO COUNT AT 100HZ PART 1
*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
*IN RATE: 100HZ PART1
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"
*
*****
ST133: SCOPE
MOV #20, $TIMES ; ; DO 20 ITERATIONS
; / CLEAR CLOCK A.
CLR $GDDAT ; / CLEAR CLOCK B.
; / CLEAR THE BUFFER + COUNT REGS.
; / SELECT: RATE: 100HZ ; GO.
* MOV $GDDAT, $ASR ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
* MOV $GDDAT, $BSR ; / PUT DATA FROM $GDDAT TO DEVICE REG BSR
* MOV $GDDAT, $BBR ; / PUT DATA FROM $GDDAT TO DEVICE REG BBR
MOV #11, $GDDAT
* MOV $GDDAT, $BSR ; / PUT DATA FROM $GDDAT TO DEVICE REG BSR
; / NOW WE'LL DO A LITTLE DELAY.
INC $R0 ; / THIS DELAY WILL AMOUNT TO APP. 269 MS.
BNE $R1 ; / ON A PDP-11/20.
; / DID COUNTER COUNT AT ALL?
* MOV $BCR, $BDDAT ; / READ DEVICE REG BCR, PUT DATA IN $BDDAT.
TST $BDDAT
BNE $R2 ; / BR IF YES - NEXT TEST.
* MOV $BSR, $BDDAT ; / READ DEVICE REG BSR, PUT DATA IN $BDDAT.
TSTB $BDDAT
; / COUNT TO OVERFLOW - SO WE'LL SEE IF
; / THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
BMI $R3 ; / BR IF SET - NEXT TEST.
***
ERROR << *****
ERROR 14 ; / ERROR CLOCK B - COUNTER FAILED TO COUNT
; / AT 100HZ RATE.
***

```

```

017450 000004
017452 012737 000020 001166
017460 005037 001124
017514 012737 000011 001124
017532 005000
017534 005200
017536 001376
017550 005737 001126
017554 001010
017566 105737 001126
017572 100401

```

\*\*\* \$ >> ERROR << \$

017574 104014 ERROR 14 ; / ERROR CLOCK B - COUNTER FAILED TO COUNT ; / AT 100HZ RATE.

\*\*\* \$ >> ERROR << \$

MAINDEC-11-DRLPG-A  
DRLPG.P11 T133

MACY11 27(654) 15-DEC-77 08:29 PAGE 160  
\*TEST THE ABILITY OF CLOCK B TO COUNT AT 100HZ PART 1

SEQ 0177

5807 017576

25:

```

5808 ;/*
5809
5810 ;*****
5811 ;*TEST 134 *TEST THE ABILITY OF CLOCK B TO COUNT AT LINE-FREQ PART 1
5812 ;*
5813 ;*THIS TEST IS DESIGNED TO TEST CLOCK B'S ABILITY TO COUNT
5814 ;*IN RATE: LINE-FREQ PART1
5815 ;*
5816 ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT A"
5817 ;*
5818 ;*
5819 ;*****
5820 017576 000004 ST134: SCOPE
5821 017600 012737 000020 001166 MOV #20,$TIMES ;;DO 20 ITERATIONS
5822
5823 ;/CLEAR CLOCK A.
5824 017606 005037 001124 CLR $GDDAT
5825 ;/CLEAR CLOCK B.
5826 ;/CLEAR THE BUFFER + COUNT REGS.
5827 ;/SELECT: RATE: LINE-FREQ ; GO.
5828
5829 ;* MOV $GDDAT,$ASR ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
5830 ;* MOV $GDDAT,$BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
5831 ;* MOV $GDDAT,$BBR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BBR
5832
5833 017642 012737 000017 001124 MOV #1!16,$GDDAT
5834 ;* MOV $GDDAT,$BSR ;/ PUT DATA FROM $GDDAT TO DEVICE REG BSR
5835
5836 017660 005000 ;/NOW WE'LL DO A LITTLE DELAY.
5837 017662 005200 1$: INC RO ;/THIS DELAY WILL AMOUNT TO APP. 269 MS.
5838 017664 001376 BNE 1$ ;/ON A PDP-11/20.
5839
5840 ;/DID COUNTER COUNT AT ALL?
5841
5842 ;* MOV $BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
5843 TST $BDDAT
5844 017676 005737 001126 BNE 2$ ;/BR IF YES - NEXT TEST.
5845 017702 001010
5846
5847 ;* MOV $BSR,$BDDAT ;/READ DEVICE REG BSR,PUT DATA IN $BDDAT.
5848 TSTB $BDDAT
5849 ;/COUNT TO overflow - SO WE'LL SEE IF
5850 017714 105737 001126 BMI 2$ ;/THE OVERFLOW F/F SET BEFORE WE CRY WOLF.
5851 ;/BR IF SET - NEXT TEST.
5852 017720 100401
5853
5854 ;; ;*****>> ERROR <<*****
5858 017722 104014 ERROR 14 ;/ERROR CLOCK B - COUNTER FAILED TO COUNT
5859 ;/AT LINE-FREQ RATE.
5860 ;; ;*****>> ERROR <<*****

```

5864 017724

2S:

5865  
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5868  
5869  
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5871  
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5873  
5874  
5875  
5876  
5877

```

*****
; *TEST 135      *TEST THE "FEED B TO A" 24 BIT COUNTER FEATURE OF CLOCKS A + B
; *
; *WE'RE GOING TO TEST CLOCKS A+B AS A 24 BIT COUNTER; THAT IS;
; *WE'RE GOINT TO TAKE THE OVERFLOW FROM CLOCK B AND FEED IT INTO
; *CLOCK A.
; *
; * PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF B"
; *
; *
*****
; ST135: SCOPE

```

5878 017724 000004

5879  
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5881  
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5915

```

; CLEAR CLOCK A.
; CLEAR CLOCK B.
; CLEAR A'S BUFFER + COUNT REGISTERS.
; PRESET B'S BUFFER + COUNT TO -1 FROM
; OVERFLOW.
; SELECT: "DISABLE OSC 1 MHZ"; RATE 1 MHZ;
; "FEED B TO A"
; SET ENABL. MUST BE SET AFTER "FEED B TO A".
; ENABLE CLOCK A; MODE 0; RATE 0.
; SIMULATE A 1 MHZ PULSE - THIS PULSE
; WILL CLOCK CLOCK B'S COUNTER
; REGISTER. AN OVERFLOW WILL
; OCCUR - THAT OVERFLOW SHOULD
; CLOCK CLOCK A'S COUNT REGISTER.
; DID CLOCK A'S COUNT REG GET CLOCKED?

```

5895 017726 005037 001124

CLR \$GDDAT

```

; * MOV $GDDAT, @ASR ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
; * MOV $GDDAT, @BSR ; / PUT DATA FROM $GDDAT TO DEVICE REG BSR
; * MOV $GDDAT, @ABR ; / PUT DATA FROM $GDDAT TO DEVICE REG ABR
; * MOV $GDDAT, @BBR ; / PUT DATA FROM $GDDAT TO DEVICE REG BBR
; * MOV $GDDAT, @BSR ; / PUT DATA FROM $GDDAT TO DEVICE REG BSR
; * INC $GDDAT
; * MOV $GDDAT, @BSR ; / PUT DATA FROM $GDDAT TO DEVICE REG BSR
; * MOV #1, $GDDAT
; * MOV $GDDAT, @ASR ; / PUT DATA FROM $GDDAT TO DEVICE REG ASR
; * MOV @ASR, $GDDAT ; / READ DEVICE REG ASR, PUT DATA IN $GDDAT.

```

5902 017762 012737 000377 001124

MOV \$GDDAT, @BBR  
MOV #4042, \$GDDAT

5905 020000 012737 004042 001124

5908 020016 005237 001124

MOV \$GDDAT, @BSR  
INC \$GDDAT

5911 020032 012737 000001 001124

MOV \$GDDAT, @BSR  
MOV #1, \$GDDAT

```

5916 020060 052737 004000 001124      BIS      #BIT11,$GDDAT
5917
5918                               ;*      MOV      $GDDAT,ASR      ;/ PUT DATA FROM $GDDAT TO DEVICE REG ASR
5919                               ;*
5920                               ;*      MOV      ACAR,$BDDAT    ;/READ DEVICE REG ACAR,PUT DATA IN $BDDAT.
5921 020106 005737 001126                TST      $BDDAT
5922
5923 020112 001001                        BNE      IS                      ;IF YES THEN BR NEXT TEST.
5924

```

::;\$>> ERROR <<\$

```

5928 020114 104014                        ERROR    14                      ;ERROR - UNABLE TO CLOCK CLOCKS A'S
5929                                          ;COUNT REGISTER WITH THE OVERFLOW
5930                                          ;FROM CLOCK B.
5931                                          ;THE MOST LOGICAL PLACE TO START
5932                                          ;WOULD BE "A CLOCK TIMING".
5933                                          ;"FEED B TO A (1)" H + "B OVERFLOW" H
5934                                          ;SHOULD BE COMING TOGETHER GOING
5935                                          ;INTO THE MUX - BEGING SELECTED AND
5936                                          ;COMING OUT OF THE MUX TO BECOME
5937                                          ;"CLOCK A" L.
5938

```

::;\$>> ERROR <<\$

```

5942 020116                               IS:
5943 .SBTTL *
5944 .SBTTL * PHASE 6 CLOCK A+B ADVANCE TESTING
5945 .SBTTL *
5946

```



6001 020226 104012  
6002  
6003  
6004  
6005

ERROR 12

;ST1 FAILED TO COUNT  
;CLOCK A'S COUNT REG. AFTER SETTING  
;'ENABL CNTR A' - SEE TEST HEADING  
;COMMENTS

:::\$>> ERROR <<\$

6009  
6010 020230  
6011  
6012

1\$:



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6064  
6065  
6066

;/#

```

*****
*TEST 137 *TEST CLOCK A'S 100KHZ DIVIDER
*
+IN THIS TEST WE'LL SEE IF THE 100KHZ DIVIDER WILL DIVIDE 1MHZ
+BY 10 TO GIVE US A 100KHZ CLK L PULSE.
+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
+PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100KHZ
+PULSES.
*THEN WE'LL GENERATE 9 MORE 1MHZ PULSES AND MAKE
*SURE THAT WE DON'T GET ANOTHER 100KHZ PULSE.
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*
*****

```

```

020230 000004
020232 012737 000020 001166

```

```

†ST137: SCOPE
MOV #20,$TIMES ;;DO 20 ITERATIONS
; /CLEAR CLOCK B.
; /CLEAR CLOCK A.
; /CLEAR A'S BUFFER + COUNT REGS.
; /DISABLE THE 1MHZ OSC.
; /ENABLE CNTR, RATE: 100KHZ ;MODE.

CLR $TMDAT
;* MOV $TMDAT,$BSR ; / PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV $TMDAT,$ASR ; / PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV $TMDAT,$ABR ; / PUT DATA FROM $TMDAT TO DEVICE REG ABR
020274 012737 004000 001356 MOV #BIT11,$TMDAT
;* MOV $TMDAT,$BSR ; / PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV $ASR,$TMDAT ; /READ DEVICE REG ASR,PUT DATA IN $TMDAT.
020322 052737 000405 001356 BIS #401!4,$TMDAT
;* MOV $TMDAT,$ASR ; / PUT DATA FROM $TMDAT TO DEVICE REG ASR
; /SET TO GENERATE ON 1MHZ PULSES
020340 012700 177766 MOV #-10.,R0
020344 1$: ; /GENERATE 1 1MHZ PULSE
; /HAS COUNTER ADVANCED ANY?
;* MOV $ASR,$TMDAT ; /READ DEVICE REG ASR,PUT DATA IN $TMDAT.
020354 052737 004000 001356 BIS #BIT11,$TMDAT
;* MOV $TMDAT,$ASR ; / PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV $ACR,$BDDAT ; /READ DEVICE REG ACR,PUT DATA IN $BDDAT.

```

```

6067 020402 005737 001126          TST      $BDDAT
6068 020406 001002                    BNE      10$
6069
6070
6071
6072
6073 020410 005200                    INC      RO
6074 020412 001354                    BNE      1$
6075
6076 020414 012737 000001 001124 10$:  MOV     #1,$GDDAT
6077
6078
6079
6080
6081
6082 020432 023737 001126 001124     CMP     $BDDAT,$GDDAT
6083 020440 001402                    BEQ     2$
6084

```

```

; /IF SO EXIT THIS LOOP.
; /NOTE: WHEN WE DISABLED THE 1 MHZ.
; /OSC., THE DIVIDER COULD HAVE
; /AND COUNT LEFT IN IT.
; /AFTER THIS LOOP, WE SHOULD BE SUNK.
; /DONE 10. 1MHZ PULSES?
; /IF NOT - DO ANOTHER.
; /SET FOR ERROR TYPEOUT IF NEEDED.
; /READ THE COUNTER.
; /READ DEVICE REG ACR, PUT DATA IN $BDDAT.
; /DID THE COUNTER ADVANCE ONCE?
; /IF YES - NEXT CHECK.

```

;;; \$ >> ERROR << \$

```

6088 020442 104012                    ERROR   12
6089
6090

```

```

; /ERROR - CLOCK A - 100KHZ - PULSE
; /NOT GENERATED WHEN 10 1MHZ PULSES

```

;;; \$ >> ERROR << \$

```

6094 020444 000430                    BR      4$
6095 020446 012700 000011              MOV     #9.,RO ; /GET THE NUMBER OF '1 MHZ' H PULSES
6096
6097 020452                                3$:
6098
6099
6100 020462 052737 004000 001356     ; *   MOV     @ASR,$TMDAT
6101                                BIS     #BIT11,$TMDAT ; /READ DEVICE REG ASR, PUT DATA IN $TMDAT.
6102                                ; *   MOV     $TMDAT,@ASR
6103 020500 005300                                DEC     RO
6104 020502 001363                                BNE     3$
6105
6106                                ; /PUT DATA FROM $TMDAT TO DEVICE REG ASR
6107                                ; /IN ORDER TO CHECK TO SEE THAT
6108                                ; /WE DON'T GENERATE ANOTHER 100KHZ PULSE.
6109 020514 023737 001126 001124     ; *   MOV     @ACR,$BDDAT
6110 020522 001401                                CMP     $BDDAT,$GDDAT
6111                                BEQ     4$
6112

```

```

; /GENERATE 9 1MHZ PULSES
; /READ DEVICE REG ASR, PUT DATA IN $TMDAT.
; /PUT DATA FROM $TMDAT TO DEVICE REG ASR
; /IN ORDER TO CHECK TO SEE THAT
; /WE DON'T GENERATE ANOTHER 100KHZ PULSE.
; /READ THE COUNTER
; /READ DEVICE REG ACR, PUT DATA IN $BDDAT.
; /WAS ANOTHER 100KHZ PULSE GENERATED?
; /NO-GO TO NEXT TEST!

```

;;; \$ >> ERROR << \$

```

6116 020524 104012                    ERROR   12
6117
6118
6119

```

```

; /ERROR CLOCK A WE SEEM TO HAVE
; /GENERATED A SECOND 100KHZ PULSE
; /ON ONLY 9 1MHZ PULSES.

```

;;; \$ >> ERROR << \$

MAINDEC-11-DRLPG-A  
DRLPG.P11 T137

MACY11 27(654) 15-DEC-77 08:29 PAGE 168  
\*TEST CLOCK A'S 100KHZ DIVIDER

SEQ 0185

6123 020526

4S:

6124  
6125  
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6177

020526 000004  
020530 012737 000020 001166  
  
020536 005037 001356  
  
020572 012737 004000 001356  
  
020620 052737 000407 001356  
  
020636 012700 177634  
020642  
  
020652 052737 004000 001356

```

; /*
*****
*TEST! 140 *TEST! CLOCK A'S 10KHZ DIVIDER
*
+IN THIS TEST WE'LL SEE IF THE 10KHZ DIVIDER WILL DIVIDE 100KHZ
+BY 10 TO GIVE US A 10KHZ CLK L PULSE.
+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 10KHZ
*PULSES.
*THEN WE'LL GENERATE 9 MORE 100KHZ PULSES AND MAKE
*SURE THAT WE DON'T GET ANOTHER 10KHZ PULSE.
*
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*****
†ST140: SCOPE
MOV #20,$TIMES ;;DO 20 ITERATIONS
;;CLEAR CLOCK B.
;;CLEAR CLOCK A.
;;CLEAR A'S BUFFER + COUNT REGS.
;;DISABLE THE 1MHZ OSC.
;;ENABLE CNTR, RATE: 10KHZ ;MODE.

CLR $TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV $TMDAT,@ABR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
MOV #BIT11,$TMDAT
;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #401!6,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;/SET TO GENERATE ON 1MHZ PULSES
MOV #-100.,R0
1$: ;/GENERATE 1 1MHZ PULSE
;/HAS COUNTER ADVANCED ANY?
;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS #BIT11,$TMDAT
;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;* MOV @ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.

```

```

6178 020700 005737 001126          TST     $BDDAT
6179 020704 001002                    BNE     10$
6180                                     ;/IF SO EXIT THIS LOOP.
6181                                     ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
6182                                     ;/OSC. THE DIVIDER COULD HAVE
6183                                     ;/AND COUNT LEFT IN IT.
6184 020706 005200          INC     RO
6185 020710 001354          BNE     1$
6186                                     ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
6187 020712 012737 000001 001124 10$:  MOV     #1,$GDDAT
6188                                     ;/SET FOR ERROR TYPEOUT IF NEEDED.
6189                                     ;/READ THE COUNTER.
6190                                     ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
6191                                     ;*
6192                                     ;/DID THE COUNTER ADVANCE ONCE?
6193 020730 023737 001126 001124      CMP     $BDDAT,$GDDAT
6194 020736 001402          BEQ     2$
6195                                     ;/IF YES - NEXT CHECK.

```

;;; \$ >> ERROR << \$

```

6199 020740 104012          ERROR 12
6200                                     ;/ERROR - CLOCK A - 10KHZ - PULSE
6201                                     ;/NOT GENERATED WHEN 10 100KHZ PULSES

```

;;; \$ >> ERROR << \$

```

6205 020742 000430          BR      4$
6206 020744 012700 000143      2$:  MOV     #99.,RO ;/GET THE NUMBER OF '1 MHZ' H PULSES
6207                                     ;/GENERATE 9 100KHZ PULSES
6208 020750          3$:
6209                                     ;*
6210                                     ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
6211 020760 052737 004000 001356      MOV     @ASR,$TMDAT
6212                                     ;/BIT 11, $TMDAT
6213                                     ;*
6214                                     ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6215 020776 005300          DEC     RO
6216 021000 001363          BNE     3$
6217                                     ;/INORDER TO CHECK TO SEE THAT
6218                                     ;/WE DON'T GENERATE ANOTHER 10KHZ PULSE.
6219                                     ;/READ THE COUNTER
6220 021012 023737 001126 001124      ;*
6221 021020 001401          MOV     @ACR,$BDDAT
6222                                     ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
6223                                     ;/WAS ANOTHER 10KHZ PULSE GENERATED?
6224                                     ;/NO-GO TO NEXT TEST!

```

;;; \$ >> ERROR << \$

```

6227 021022 104012          ERROR 12
6228                                     ;/ERROR CLOCK A WE SEEM TO HAVE
6229                                     ;/GENERATED A SECOND 10KHZ PULSE
6230                                     ;/ON ONLY 9 100KHZ PULSES.

```

;;; \$ >> ERROR << \$

MAINDEC-11-DRLPG-A  
DRLPG.P11 T140

MACY11 27(654) 15-DEC-77 08:29 PAGE 171  
\*TEST CLOCK A'S 10KHZ DIVIDER

SEQ 0188

6234 021024

4S:

6235  
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```

; /*
*****
*TEST 141      *TEST CLOCK A'S 1KHZ DIVIDER
*
+IN THIS TEST WE'LL SEE IF THE 1KHZ DIVIDER WILL DIVIDE 10KHZ
+BY 10 TO GIVE US A 1KHZ CLK L PULSE.
+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 1KHZ
*PULSES.
*THEN WE'LL GENERATE 9 MORE 10KHZ PULSES AND MAKE
*SURE THAT WE DON'T GET ANOTHER 1KHZ PULSE.
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*****
†ST141: SCOPE
MOV      #20,$TIMES      ;;DO 20 ITERATIONS
                ;/CLEAR CLOCK B.
                ;/CLEAR CLOCK A.
                ;/CLEAR A'S BUFFER + COUNT REGS.
                ;/DISABLE THE 1MHZ OSC.
                ;/ENABLE CNTR, RATE: 1KHZ ;MODE.

021024  000004      CLR      $TMDAT
021026  012737  000020  001166      ;* MOV      $TMDAT,$BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
                ;* MOV      $TMDAT,$ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
                ;* MOV      $TMDAT,$ABR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
021070  012737  004000  001356      ;* MOV      $TMDAT,$BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
                ;* MOV      $TMDAT,$ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
                ;* MOV      $TMDAT,$ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
                ;/SET TO GENERATE ON 1MHZ PULSES
021134  012700  176030      MOV      #-1000.,R0
021140                                1$:      ;/GENERATE 1 1MHZ PULSE
                ;/HAS COUNTER ADVANCED ANY?
                ;* MOV      $ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
                ;* BIS      #BIT11,$TMDAT
021150  052737  004000  001356      ;* MOV      $TMDAT,$ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
                ;* MOV      $ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.

```





MAINDEC-11-DRLPG-A  
DRLPG.P11 T141

MACY11 27(654) 15-DEC-77 08:29 PAGE 174  
\*TEST CLOCK A'S 1KHZ DIVIDER

J15

SEQ 0191

6345 021322

4S:

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6398  
6399

;/#

```

*****
*TEST 142      *TEST CLOCK A'S 100HZ DIVIDER
*
+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
+BY 10 TO GIVE US A 100HZ CLK L PULSE.
+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
+PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
+PULSES.
+THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
+SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
*
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
*****

```

```

021322 000004
021324 012737 000020 001166

```

```

ST142: SCOPE
MOV      #20,$TIMES      ;;DO 20 ITERATIONS
;/CLEAR CLOCK B.
;/CLEAR CLOCK A.
;/CLEAR A'S BUFFER + COUNT REGS.
;/DISABLE THE 1MHZ OSC.
;/ENABLE CNTR, RATE: 100HZ ;MODE.

```

```

021332 005037 001356

```

```

CLR      $TMDAT
;*      MOV      $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;*      MOV      $TMDAT,@ABR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR
021366 012737 004000 001356  MOV      #BIT11,$TMDAT
;*      MOV      $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
;*      MOV      @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
021414 052737 000413 001356  BIS      #401!12,$TMDAT
;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;/SET TO gENERATE ON 1MHZ PULSES
021432 012700 154360      MOV      #-10000.,RO

```

```

021436

```

```

1$:      ;/GENERATE 1 1MHZ PULSE
;/HAS COUNTER ADVANCED ANY?

```

```

021446 052737 004000 001356

```

```

;*      MOV      @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
BIS      #BIT11,$TMDAT
;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
;*      MOV      @ACR,$BDDAT      ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.

```

```

6400 021474 005737 001126 TST $BDDAT
6401 021500 001002 BNE 10$ ;/IF SO EXIT THIS LOOP.
6402 ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
6403 ;/OSC. THE DIVIDER COULD HAVE
6404 ;/AND COUNT LEFT IN IT.
6405 ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
6406 021502 005200 INC RO
6407 021504 001354 BNE 1$ ;/DONE 10000. 1MHZ PULSES?
6408 ;/IF NOT - DO ANOTHER.
6409 021506 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.
6410 ;/READ THE COUNTER.
6411 ;* MOV $ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
6412
6413
6414 021524 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
6415 021532 001402 BEQ 2$ ;/IF YES - NEXT CHECK.
6416
6417
  
```

;;; \$ > ERROR << \$

```

6421 021534 104012 ERROR 12 ;/ERROR - CLOCK A - 100HZ - PULSE
6422 ;/NOT GENERATED WHEN 10 1KHZ PULSES
6423
  
```

;;; \$ > ERROR << \$

```

6427 021536 000430 BR 4$
6428 021540 012700 023417 2$: MOV #9999.,RO ;/GET THE NUMBER OF '1 MHZ' H PULSES
6429 ;/GENERATE 9 1KHZ PULSES
6430 021544 3$:
6431 ;* MOV $ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
6432 021554 052737 004000 001356 BIS #BIT11,$TMDAT
6433 ;* MOV $TMDAT,$ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6434 ;/INORDER TO CHECK TO SEE THAT
6435 021572 005300 DEC RO ;/WE DON'T GENERATE ANOTHER 100HZ PULSE.
6436 021574 001363 BNE 3$ ;/READ THE COUNTER
6437
6438
6439 ;* MOV $ACR,$BDDAT ;/READ DEVICE REG ACR,PUT DATA IN $BDDAT.
6440 021606 023737 001126 001124 CMP $BDDAT,$GDDAT ;/WAS ANOTHER 100HZ PULSE GENERATED?
6441 021614 001401 BEQ 4$ ;/NO-GO TO NEXT TEST!
6442
6443
6444
6445
  
```

;;; \$ > ERROR << \$

```

6449 021616 104012 ERROR 12 ;/ERROR CLOCK A WE SEEM TO HAVE
6450 ;/GENERATED A SECOND 100HZ PULSE
6451 ;/ON ONLY 9 1KHZ PULSES.
6452
  
```

;;; \$ > ERROR << \$

6456 021620

4\$:

6457  
6458  
6459  
6460  
6461  
6462  
6463  
6464  
6465  
6466  
6467  
6468  
6469  
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6506  
6507

021620 000004  
021622 012737 000020 001166  
  
021630 005037 001356  
  
021664 012737 004040 001356  
  
021712 052737 000004 001356  
  
021730 005237 001356  
  
021744 012700 177766  
  
021750

```
*****  
*TEST 143 *TEST CLOCK B'S 100KHZ DIVIDER  
*  
*IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ  
*BY 10 TO GIVE US A 100HZ CLK L PULSE.  
*TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND  
*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ  
*PULSES.  
*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE  
*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.  
*  
* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"  
*  
*****  
TST143: SCOPE  
MOV #20,$TIMES ;;DO 20 ITERATIONS  
;  
;/CLEAR CLOCK B.  
;/CLEAR CLOCK A.  
;  
;/CLEAR B'S BUFFER + COUNT REGS.  
;/DISABLE THE 1MHZ OSC.  
;/RATE: 100KHZ  
;/ENABLE CLOCK B.  
CLR $TMDAT  
;* MOV $TMDAT,$BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
;* MOV $TMDAT,$ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
;* MOV $TMDAT,$BBR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR  
MOV #BIT11!BITS,$TMDAT  
;* MOV $TMDAT,$BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
;* MOV $BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.  
BIS #4,$TMDAT  
;* MOV $TMDAT,$BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
INC $TMDAT  
;* MOV $TMDAT,$BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR  
MOV #-10.,R0 ;/SET TO GENERATE 10. 1MHZ PULSES  
1$:  
;/GENERATE 1 1MHZ PULSE  
;/HAS THE COUNTER ADVANCED?
```

MAINDEC-11-DRLPG-A  
DRLPG.P11 T143

MACY11 27(654) 15-DEC-77 08:29 PAGE 178  
\*TEST CLOCK B'S 100KHZ DIVIDER

SEQ 0195

```

6508      ;*      MOV      @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
6509 021760 052737 004000 001356      BIS      #BIT11,$TMDAT
6510      ;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6511      ;*      MOV      @BCR,$BDDAT      ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6512      ;*      TST      $BDDAT
6513      ;*      BNE      10$
6514 022006 005737 001126
6515 022012 001002
6516      ;/EXIT LOOP IF SO.
6517      ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
6518      ;/      OSC. THE DIVIDER COULD HAVE
6519      ;/      HAD ANY COUNT IN IT.
6520      ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
6521 022014 005200      INC      RO      ;/DONE 10. 1MHZ PULSES?
6522 022016 001354      BNE      1$      ;/IF NOT - DO ANOTHER.
6523
6524 022020 012737 000001 001124 10$:  MOV      #1,$GDDAT      ;/SET FOR ERROR TYPEOUT IF NEEDED.
6525
6526      ;/READ THE COUNTER
6527
6528      ;*      MOV      @BCR,$BDDAT      ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6529
6530 022036 023737 001126 001124      CMP      $BDDAT,$GDDAT      ;/DID THE COUNTER ADVANCE ONCE?
6531 022044 001402      BEQ      2$      ;/IF YES - NEXT CHECK
6532

```

::;\$>> ERROR <<\$

```

6536 022046 104015      ERROR      15      ;/ERROR - CLOCK B - 100KHZ - PULSE
6537      ;/NOT GENERATED WHEN 10 1MHZ PULSE
6538      ;/WERE GENERATED.
6539

```

::;\$>> ERROR <<\$

```

6543 022050 000430      BR      4$
6544
6545 022052 012700 177767      2$:  MOV      #-9.,RO      ;/GET THE NUMBER OF "1 MHZ" H PULSES
6546      ;/NEED TO GIVE 9 1MHZ PULSES
6547 022056      3$:
6548
6549      ;*      MOV      @ASR,$TMDAT      ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
6550 022066 052737 004000 001356      BIS      #BIT11,$TMDAT
6551      ;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6552      ;/IN ORDER TO CHECK TO SEE THAT
6553 022104 005200      INC      RO
6554 022106 001363      BNE      3$      ;/WE DON'T GENERATE ANOTHER 100KHZ PULSE
6555
6556      ;*      MOV      @BCR,$BDDAT      ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6557      ;/WAS ANOTHER 100KHZ PULSE GENERATED?
6558 022120 023737 001126 001124      CMP      $BDDAT,$GDDAT
6559 022126 001401      BEQ      4$      ;/NO - GO TO NEXT CHECK.
6560
6561

```

::: \$ > ERROR << \$

6565 022130 104015 ERROR 15 ;/ERROR CLOCK B WE SEEM TO HAVE  
6566 ;/GENERATED A SECOND 100KHZ PULSE  
6567 ;/ON ONLY 9 1MHZ PULSES.  
6568

::: \$ > ERROR << \$

6572 022132 4S:  
6573 ;/\*\*\*\*\*  
6574 ;/TEST 144 \*TEST CLOCK B'S 10KHZ DIVIDER  
6575 ;/  
6576 ;/IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ  
6577 ;/BY 10 TO GIVE US A 100HZ CLK L PULSE.  
6578 ;/TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND  
6579 ;/PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ  
6580 ;/PULSES.  
6581 ;/THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE  
6582 ;/SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.  
6583 ;/  
6584 ;/  
6585 ;/PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"  
6586 ;/  
6587 ;/\*\*\*\*\*

6588  
6589 022132 000004  
6590 022134 012737 000020 001166 ST144: SCOPE  
6591 MOV #20,\$TIMES ;/DO 20 ITERATIONS  
6592 ;/CLEAR CLOCK B.  
6593 ;/CLEAR CLOCK A.  
6594 ;/  
6595 ;/CLEAR B'S BUFFER + COUNT REGS.  
6596 ;/DISABLE THE 1MHZ OSC.  
6597 ;/RATE: 10KHZ  
6598 ;/ENABLE CLOCK B.  
6599 022142 005037 001356 CLR \$TMDAT  
6600 ;/  
6601 ;/\* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR  
6602 ;/\* MOV \$TMDAT,@ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR  
6603 ;/\* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR  
6604 ;/\* MOV \$TMDAT,@BBR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BBR  
6605 022176 012737 004040 001356 MOV #BIT11!BITS,\$TMDAT  
6606 ;/\* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR  
6607 ;/\* MOV @BSR,\$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN \$TMDAT.  
6608 ;/\* BIS #6,\$TMDAT  
6609 ;/  
6610 ;/\* MOV \$TMDAT,@BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR  
6611 022224 052737 000006 001356 INC \$TMDAT  
6612 ;/  
6613 022242 005237 001356  
6614  
6615

```

6616        ;*      MOV      $TMDAT,$BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
6617 022256  012700  177634          MOV      #-100.,RO      ;/SET TO GENERATE 100. 1MHZ PULSES
6618
6619 022262          1$:                       ;/GENERATE 1 1MHZ PULSE
6620          ;/HAS THE COUNTER ADVANCED?
6621
6622        ;*      MOV      @ASR,$TMDAT        ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
6623 022272  052737  004000  001356  BIS      @BIT11,$TMDAT
6624
6625        ;*      MOV      $TMDAT,$ASR        ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6626        ;*      MOV      @BCR,$BDDAT       ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6627 022320  005737  001126          TST     $BDDAT
6628 022324  001002          BNE     10$
6629          ;/EXIT LOOP IF SO.
6630          ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
6631          ;/OSC., THE DIVIDER COULD HAVE
6632          ;/HAD ANY COUNT IN IT.
6633          ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
6634
6635 022326  005200          INC     RO            ;/DONE 100. 1MHZ PULSES?
6636 022330  001354          BNE     1$          ;/IF NOT - DO ANOTHER.
6637
6638 022332  012737  000001  001124  10$:   MOV     #1,$GDDAT    ;/SET FOR ERROR TYPEOUT IF NEEDED.
6639          ;/READ THE COUNTER
6640
6641        ;*      MOV      @BCR,$BDDAT       ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6642
6643 022350  023737  001126  001124          CMP     $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
6644 022356  001402          BEQ     2$          ;/IF YES - NEXT CHECK
6645
6646          ;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ > ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

```

```

6650 022360  104015          ERROR  15          ;/ERROR - CLOCK B - 10KHZ - PULSE
6651          ;/NOT GENERATED WHEN 10 100KHZ PULSE
6652          ;/WERE GENERATED.
6653
6654          ;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ > ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

```

```

6657 022362  000430          BR     4$
6658
6659 022364  012700  177635          2$:   MOV     #-99.,RO      ;/GET THE NUMBER OF "1 MHZ" H PULSES
6660          ;/NEED TO GIVE 9 100KHZ PULSES
6661 022370          3$:
6662
6663        ;*      MOV      @ASR,$TMDAT        ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
6664 022400  052737  004000  001356  BIS      @BIT11,$TMDAT
6665
6666        ;*      MOV      $TMDAT,$ASR        ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6667 022416  005200          INC     RO            ;/IN ORDER TO CHECK TO SEE THAT
6668 022420  001363          BNE     3$          ;/WE DON'T GENERATE ANOTHER 10KHZ PULSE
6669

```

```

6670
6671
6672 022432 023737 001126 001124 ;*   MOV   @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6673 022440 001401                CMP   $BDDAT,$GDDAT ;/WAS ANOTHER 10KHZ PULSE GENERATED?
6674                                BEQ   4$             ;/NO - GO TO NEXT CHECK.
6675

```

;;; \$>> ERROR << \$

```

6679 022442 104015                ERROR 15 ;/ERROR CLOCK B WE SEEM TO HAVE
6680                                ;/GENERATED A SECOND 10KHZ PULSE
6681                                ;/ON ONLY 9 100KHZ PULSES.
6682

```

;;; \$>> ERROR << \$

```

6686 022444                4$:
6687
6688 ;:*****
6689 ;:TEST 145      *TEST CLOCK B'S 1KHZ DIVIDER
6690 ;:
6691 ;:IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
6692 ;:BY 10 TO GIVE US A 100HZ CLK L PULSE.
6693 ;:TO DO THIS WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
6694 ;:PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
6695 ;:PULSES.
6696 ;:THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
6697 ;:SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
6698 ;:
6699 ;:
6700 ;:PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
6701 ;:
6702 ;:*****

```

```

6703 022444 000004                ST145: SCOPE
6704 022446 012737 000020 001166  MOV   #20,$TIMES ;;DO 20 ITERATIONS
6705 ;/CLEAR CLOCK B.
6706 ;/CLEAR CLOCK A.
6707
6708 ;/CLEAR B'S BUFFER + COUNT REGS.
6709 ;/DISABLE THE 1MHZ OSC.
6710 ;/RATE: 1KHZ
6711 ;/ENABLE CLOCK B.
6712
6713 022454 005037 001356  CLR   $TMDAT
6714 ;*   MOV   $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
6715 ;*   MOV   $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6716
6717 ;*   MOV   $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
6718 ;*   MOV   $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
6719
6720 022510 012737 004040 001356  MOV   #BIT11!BITS,$TMDAT
6721 ;*   MOV   $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
6722
6723

```



```

6724 ;* MOV @BSR,$TMDAT ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.
6725 022536 052737 000010 001356 BIS #10,$TMDAT
6726
6727 ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
6728 022554 005237 001356 INC $TMDAT
6729
6730 ;* MOV $TMDAT,@BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
6731 022570 012700 176030 MOV #-1000.,RO ;/SET TO GENERATE 1000. 1MHZ PULSES
6732
6733 022574 1$: ;/GENERATE 1 1MHZ PULSE
6734 ;/HAS THE COUNTER ADVANCED?
6735
6736 ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
6737 022604 052737 004000 001356 BIS #BIT11,$TMDAT
6738
6739 ;* MOV $TMDAT,@ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6740
6741 ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6742 022632 005737 001126 TST $BDDAT
6743 022636 001002 BNE 10$ ;/EXIT LOOP IF SO.
6744 ;/NOTE: WHEN WE DISABLED THE 1 MHZ.
6745 ;/ OSC. THE DIVIDER COULD HAVE
6746 ;/ HAD ANY COUNT IN IT.
6747 ;/AFTER THIS LOOP, WE SHOULD BE SUNK.
6748
6749 022640 005200 INC RO ;/DONE 1000. 1MHZ PULSES?
6750 022642 001354 BNE 1$ ;/IF NOT - DO ANOTHER.
6751
6752 022644 012737 000001 001124 10$: MOV #1,$GDDAT ;/SET FOR ERROR TYPEOUT IF NEEDED.
6753
6754 ;/READ THE COUNTER
6755
6756 ;* MOV @BCR,$BDDAT ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6757
6758 022662 023737 001126 001124 CMP $BDDAT,$GDDAT ;/DID THE COUNTER ADVANCE ONCE?
6759 022670 001402 BEQ 2$ ;/IF YES - NEXT CHECK
6760
    ;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

6764 022672 104015 ERROR 15 ;/ERROR - CLOCK B - 1KHZ - PULSE
6765 ;/NOT GENERATED WHEN 10 10KHZ PULSE
6766 ;/WERE GENERATED.
6767

    ;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

6771 022674 000430 BR 4$
6772
6773 022676 012700 176031 2$: MOV #-999.,RO ;/GET THE NUMBER OF "1 MHZ" H PULSES
6774 ;/NEED TO GIVE 9 10KHZ PULSES
6775 022702 3$:
6776
6777 ;* MOV @ASR,$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.
    
```

```

6778 022712 052737 004000 001356      BIS      #BIT11,$TMDAT
6779
6780      ;*      MOV      $TMDAT,$ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6781 022730 005200      INC      RO      ;/IN ORDER TO CHECK TO SEE THAT
6782 022732 001363      BNE      3$      ;/WE DON'T GENERATE ANOTHER 1KHZ PULSE
6783
6784
6785      ;*      MOV      @BCR,$BDDAT      ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.
6786 022744 023737 001126 001124      CMP      $BDDAT,$GDDAT      ;/WAS ANOTHER 1KHZ PULSE GENERATED?
6787 022752 001401      BEQ      4$      ;/NO - GO TO NEXT CHECK.
6788
6789

```

::;\$>> ERROR <<\$

```

6793 022754 104015      ERROR      15      ;/ERROR CLOCK B WE SEEM TO HAVE
6794      ;/GENERATED A SECOND 1KHZ PULSE
6795      ;/ON ONLY 9 10KHZ PULSES.
6796

```

::;\$>> ERROR <<\$

```

6800 022756      4$:
6801
6802      ;*****
6803      ;*TEST 146      *TEST CLOCK B'S 100HZ DIVIDER
6804      ;*
6805      ;+IN THIS TEST WE'LL SEE IF THE 100HZ DIVIDER WILL DIVIDE 1KHZ
6806      ;+BY 10 TO GIVE US A 100HZ CLK L PULSE.
6807      ;+TO DO THIS, WE'LL DISABLE THE REGULAR 1MHZ CLK PULSE AND
6808      ;*PULSES THAT IN TURN SHOULD DIVIDE BY TEN TO GIVE US ONE 100HZ
6809      ;*PULSES.
6810      ;*THEN WE'LL GENERATE 9 MORE 1KHZ PULSES AND MAKE
6811      ;*SURE THAT WE DON'T GET ANOTHER 100HZ PULSE.
6812      ;*
6813      ;*
6814      ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF A"
6815      ;*
6816      ;*****
6817 022756 000004      †ST146: SCOPE
6818 022760 012737 000020 001166      MOV      #20,$TIMES      ;/DO 20 ITERATIONS
6819
6820      ;/CLEAR CLOCK B.
6821      ;/CLEAR CLOCK A.
6822
6823      ;/CLEAR B'S BUFFER + COUNT REGS.
6824      ;/DISABLE THE 1MHZ OSC.
6825      ;/RATE: 100HZ
6826      ;/ENABLE CLOCK B.
6827 022766 005037 001356      CLR      $TMDAT
6828
6829      ;*      MOV      $TMDAT,@BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
6830      ;*      MOV      $TMDAT,@ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
6831

```



H16

```
6886  
6887 023210 012700 154361 2$:      MOV      #-9999.,RO      ;/GET THE NUMBER OF "1 MHZ" H PULSES  
6888                                           ;/NEED TO GIVE 9 1KHZ PULSES  
6889 023214                       3$:  
6890  
6891                               ;*      MOV      @ASR,$TMDAT    ;/READ DEVICE REG ASR,PUT DATA IN $TMDAT.  
6892 023224 052737 004000 001356  BIS      @BIT11,$TMDAT  
6893  
6894                               ;*      MOV      $TMDAT,@ASR    ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
6895 023242 005200                 INC      RO          ;/IN ORDER TO CHECK TO SEE THAT  
6896 023244 001363                 BNE      3$         ;/WE DON'T GENERATE ANOTHER 100HZ PULSE  
6897  
6898  
6899                               ;*      MOV      @BCR,$BDDAT    ;/READ DEVICE REG BCR,PUT DATA IN $BDDAT.  
6900 023256 023737 001126 001124  CMP      $BDDAT,$GDDAT ;/WAS ANOTHER 100HZ PULSE GENERATED?  
6901 023264 001401                 BEQ      4$         ;/NO - GO TO NEXT CHECK.  
6902  
6903
```

;;; \$ > ERROR << \$

```
6907 023266 104015                ERROR 15      ;/ERROR CLOCK B WE SEEM TO HAVE  
6908                                           ;/GENERATED A SECOND 100HZ PULSE  
6909                                           ;/ON ONLY 9 1KHZ PULSES.  
6910
```

;;; \$ > ERROR << \$

```
6914 023270                       4$:  
6915  
6916  
6917                               .SBTTL  
6918  
6919                               .SBTTL END OF PASS ROUTINE  
6920  
6921                               ;*****  
6922                               ;*INCREMENT THE PASS NUMBER ($PASS)  
6923                               ;*TYPE "END PASS"  
6924                               ;*IF THERES A MONITOR GO TO IT  
6925                               ;*IF THERE ISN'T JUMP TO LOOP  
6926                               ;*IF IT IS DESIRED TO HAVE A BELL INDICATE THE "END OF PASS" LOCATION  
6927                               ;*$SENDMG CAN BE CHANGED TO 7.  
6928  
6929                               $EOP:  
6930 023270 000240                 NOP  
6931 023272 005037 001102         CLR      $TSTNM    ;: ZERO THE TEST NUMBER  
6932 023276 005037 001166         CLR      $TIMES    ;: ZERO THE NUMBER OF ITERATIONS  
6933 023302 005237 001210         INC      $PASS     ;: INCREMENT THE PASS NUMBER  
6934 023306 042737 100000 001210  BIC      @100000,$PASS ;: DON'T ALLOW A NEG. NUMBER  
6935 023314 005327                 DEC      (PC)+     ;: LOOP?  
6936 023316 000001                 SEOPCT: .WORD 1  
6937 023320 003015                 BGT      $DOAGN    ;: YES  
6938 023322 012737                 MOV      (PC)+,@(PC)+ ;: RESTORE COUNTER  
6939 023324 000001                 SENDCT: .WORD 1
```

```

6940 023326 023316
6941 023330 104401 023363
6942 023334 013700 000042
6943 023340 001405
6944 023342 000005
6945 023344 004710
6946 023346 000240
6947 023350 000240
6948 023352 000240
6949 023354
6950 023354 000137
6951 023356 002310
6952 023360 377 377 000
6953 023363 015 042412 042116
6954 023370 050040 051501 000123
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6986 023376
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6988 023376 005037 001104
6989 023402 012737 177704 001210
6990
6991
6992
6993

$EO$CT
TYPE $SENDMG ;; TYPE "END PASS"
MOV $M42,RO ;; GET MONITOR ADDRESS
BEQ $DOAGN ;; BRANCH IF NO MONITOR
RESETE ;; CLEAR THE WORLD
SENDAD: JSR PC,(RO) ;; GO TO MONITOR
NOP ;; SAVE ROOM
NOP ;; FOR
NOP ;; ACT11

$DOAGN: JMP $PC)+ ;; RETURN
SRTNAD: .WORD LOOP
$ENULL: .BYTE -1,-1,0 ;; NULL CHARACTER STRING
$SENDMG: .ASCIZ <15><12>/END PASS/

.SBTTL *
.SBTTL * SPECIAL I/O SIGNAL TESTS
.SBTTL *

.SBTTL * "STP2 OUT" TO "SCHMITT TRIG 1 IN" TESTS
;*
;* THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
;* PROVIDING SCOPE LOOP CAPABILITIES FOR "STP2 OUT" L
;* AND "SCHMITT TRIG 1" IN.
;*
;* WHEN YOU LOAD AND START AT LOCATION 210, PROGRAM
;* CONTROL IS TRANSFERRED HERE. "STP2 OUT" L PULSES ARE
;* GENERATED BY "LO STAT A HI" H + "BD10" H (MAIN. STP2).
;* PIN V ("STP2 OUT") IS WIRED TO PIN LL (SCHMITT TRIG1) FOR
;* THIS TEST. "STP2 OUT" PULSES ARE RECEIVED AS "SCHMITT TRIG 1"
;* PULSES WHICH SET CLOCK A'S STATUS REGISTER BIT 15.
;* IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
;* AND ERROR SWITCH REGISTER OPTIONS ARE USED.
;* AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE
;* TEST. SW13=1 WILL INHIBIT THIS FEATURE.
;*
;* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"
;*
;* YOU MUST WIRE PINS DD AND LL OF J1 TOGETHER.
;*
;* LOGIC TEST (L + S 200) SHOULD BE RUN FIRST.
;*

LS210:
1$: CLR $ICNT ;/CLEAR ITERATION COUNT
MOV #-60.,$PASS ;/SET PASS COUNT.
;/NOTE: PASS COUNT USED ONLY
;/ TO DETECT 60 PASSES SO
;/ IT CAN GENERATE A CRLF.
;/ AFTER CRLF IT WILL BE ZEROED.

```

J16

```
6994                                     ; /CLEAR CLOCK A.  
6995 023410                             ; /CLEAR CLOCK B.  
6996 023410 005037 001356              CLR     $TMDAT  
6997                                     ;  
6998                                     ; *   MOV     $TMDAT, @ASR      ; / PUT DATA FROM $TMDAT TO DEVICE REG ASR  
6999                                     ; *   MOV     $TMDAT, @BSR      ; / PUT DATA FROM $TMDAT TO DEVICE REG BSR  
7000                                     ;  
7001                                     ;  
7002                                     ;  
7003                                     ; GENERATE AN "STP2 OUT" PULSE  
7004                                     ; AT THIS POINT YOU SHOULD  
7005                                     ; SEE AN OUTPUT AT PIN V.  
7006                                     ; PIN V SHOULD BE WIRED TO  
7007                                     ; PIN LL FOR "SCHMITT TRIG 1" IN.  
7008                                     ;  
7009                                     ; IS "ST1 FLAG" BIT 15 IN CLOCK  
7010                                     ; A'S CSR SET?  
7011                                     ;  
7012                                     ; *   MOV     @ASR, $TMDAT     ; /READ DEVICE REG ASR, PUT DATA IN $TMDAT.  
7013                                     ; *   MOV     @ASR, $TMDAT     ; /READ DEVICE REG ASR, PUT DATA IN $TMDAT.  
7014                                     ; *   MOV     @ASR, $TMDAT     ; /READ DEVICE REG ASR, PUT DATA IN $TMDAT.  
7015 023454 052737 002000 001356      BIS     #BIT10, $TMDAT  
7016                                     ; *   MOV     $TMDAT, @ASR     ; / PUT DATA FROM $TMDAT TO DEVICE REG ASR  
7017 023472 032737 100000 001356      BIT     #BIT15, $TMDAT  
7018                                     ; *   MOV     $TMDAT, @ASR     ; / PUT DATA FROM $TMDAT TO DEVICE REG ASR  
7019                                     ; *   MOV     $TMDAT, @ASR     ; BR IF YES TO 3$:  
7020                                     ;  
7021 023510 001001                       BNE    3$  
7022  
7023  
  
    ; ; ; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ >> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$  
  
7027  
7028 023512 104000                        ERROR                        ; ERROR "SCHMITT TRIG 1" IN NOT  
7029                                     ; RECEIVED. HAVE YOU WIRED IT RIGHT?  
7030  
  
    ; ; ; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ >> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$  
  
7034 023514                             3$:  
7035                                     ;  
7036 023514 032777 020000 155416      BIT     #BIT13, @SWR        ; /INHIBIT "*" TYPEOUT?  
7037 023522 001332                                BNE    2$                  ; /YES - IGNORE ANY UPDATES.  
7038                                     ;  
7039 023524 005237 001104              INC     $ICNT              ; /UPDATE COUNT.  
7040 023530 001327                                BNE    2$                  ; /IF NOT DONE 65,324 TIMES,  
7041                                     ; /DO IT AGAIN.  
7042                                     ;  
7043 023532 104401 023540              TYPE    ,65$                ; ; TYPE ASCIZ STRING  
7044 023536 000401                                BR     ,64$                ; ; GET OVER THE ASCIZ  
7045                                     ; ;  
7046 023542 ;:65$: .ASCIZ  ###  
7047 64$:
```

```

7048 023542 005237 001210      INC      $PASS      ;/DONE 60 PASSES?
7049 023546 100720              BMI      2$         ;/NO - NO NEED FOR CR,LF.
7050 023550 104401 023556      TYPE     67$       ;:TYPE ASCIZ STRING
7051 023554 000402              BR       66$       ;:GET OVER THE ASCIZ
7052                                ;:67$: .ASCIZ <15><12>##
7053 023562 000705              66$:      BR       1$
7054 023562 000705
7055
7056
7057 .SBTTL      ;*      "STP1 OUT" TO "SCHMITT TRIG 2" H TESTS
7058           ;*
7059           ;* THIS IS A SPECIAL TEST SECTION DEVOTED FOR TESTING AND
7060           ;* PROVIDING SCOPE LOOP CAPABILITIES FOR "STP1 OUT" AND
7061           ;* "SCHMITT TRIG2" IN.
7062           ;*
7063           ;* WHEN YOU LOAD AND START AT LOCATION 214, PROGRAM
7064           ;* CONTROL IS TRANSFERRED HERE. "STP1 OUT" L PULSES ARE
7065           ;* GENERATED BY "LD STAT A HI" + "BD12" H (MAIN ST1).
7066           ;* PIN DD ("STP1 OUT") IS WIRED TO PIN BB ("SCHMITT
7067           ;* TRIG 2") FOR THIS TEST. "STP1 OUT" PULSES ARE RECEIVED AS
7068           ;* "SCHMITT TRIG 2" PULSES WHICH WILL CLEAR CLOCK A'S
7069           ;* COUNT REGISTER IF MODE 3 IS SELECTED.
7070           ;* IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
7071           ;* AND ERROR SWITCH REGISTER OPTIONS ARE USED.
7072           ;* AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH
7073           ;* THE TEST. SW13=1 WILL INHIBIT THIS FEATURE.
7074           ;*
7075           ;*
7076           ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"
7077           ;*
7078           ;*
7079           ;* YOU MUST WIRE PINS DD AND BB OF J1 TOGETHER.
7080           ;*
7081           ;* LOGIC TESTS (L + S AT 200) SHOULD BE RUN FIRST.
7082           ;*
7083 023564      LS214:
7084
7085 023564 005037 001104      1$:      CLR      $ICNT      ;/CLEAR ITERATION COUNT
7086 023570 012737 177704 001210      MOV      #-60.,$PASS    ;/SET PASS COUNT.
7087                                     ;/NOTE: PASS COUNT USED ONLY
7088                                     ;/ TO DETECT 60 PASSES SO
7089                                     ;/ IT CAN GENERATE A CRLF.
7090                                     ;/ AFTER CRLF IT WILL BE ZEROED.
7091                                     ;/CLEAR CLOCK A.
7092 023576 005037 001356      2$:      CLR      $TMDAT    ;/CLEAR CLOCK B.
7093 023576
7094
7095           ;*      MOV      $TMDAT,ASR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
7096           ;*
7097           ;*      MOV      $TMDAT,BSR      ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
7098
7099           ;/LOAD ALL ONES TO CLK A'S BUFFER + COUNT REG.
7100           ;SELECT MODE 3.
7101           ;GENERATE A "STP1 OUT" PULSE.

```

```
7102                                     : AT THIS POINT WE SHOULD SEE AN  
7103                                     ; OUTPUT AT PIN DD. PIN DD SHOULD  
7104                                     ; BE WIRED TO PIN BB FOR  
7105                                     ; "SCHMITT TRIG 2" IN. THIS SHOULD  
7106                                     ; CAUSE AN "STP2" WHICH WILL CLEAR  
7107                                     ; CLOCK A'S COUNT REGISTER.  
7108 023622 012737 177777 001356      MOV    #-1,$TMDAT  
7109                                     ;*  
7110                                     ;/ PUT DATA FROM $TMDAT TO DEVICE REG ABR  
7111 023640 005037 001356              MOV    $TMDAT,$ABR  
7112 023644 012737 001400 001356      CLR    $TMDAT  
7113                                     ;*  
7114                                     ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
7115                                     ;*  
7116 023672 052737 010000 001356      MOV    $ASR,$TMDAT  
7117                                     ;/ READ DEVICE REG ASR, PUT DATA IN $TMDAT.  
7118                                     ;*  
7119                                     ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR  
7120                                     ; WAS THE COUNT REGISTER CLEARED?  
7121                                     ;*  
7122 023720 005737 001126              MOV    $ACR,$BDDAT  
7123                                     ;/ READ DEVICE REG ACR, PUT DATA IN $BDDAT.  
7124                                     ;*  
7125 023724 001401                     TST    $BDDAT  
7126                                     ; IF YES BR 3$.  
                                     ;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ >> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$  
  
7130 023726 104000                     ERROR                                     ; ERROR "SCHMITT TRIG 2" IN NOT  
7131                                     ; RECEIVED. HAVE YOU WIRED IT RIGHT?  
7132                                     ;; $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$ >> ERROR << $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$  
  
7136 023730                               3$:  
7137                                     ;*  
7138 023730 032777 020000 155202      BIT    #BIT13,$SWR                                     ; /INHIBIT "*" TYPEOUT?  
7139 023736 001317                                     BNE    2$                                     ; /YES - IGNORE ANY UPDATES.  
7140                                     ;*  
7141 023740 005237 001104              INC    $ICNT                                     ; /UPDATE COUNT.  
7142 023744 001314                                     BNE    2$                                     ; /IF NOT DONE 65,324 TIMES,  
7143                                     ; /DO IT AGAIN.  
7144                                     ;*  
7145 023746 104401 023754              TYPE   65$                                     ;; TYPE ASCIZ STRING  
7146 023752 000401                      BR     64$                                     ;; GET OVER THE ASCIZ  
7147                                     ;*  
7148 023756                               ;:65$:  
7149                                     ;:64$:  
7150 023756 005237 001210              INC    $PASS                                     ; /DONE 60 PASSES?  
7151 023762 100705                                     BMI    2$                                     ; /NO - NO NEED FOR CR,LF.  
7152 023764 104401 023772              TYPE   67$                                     ;; TYPE ASCIZ STRING  
7153 023770 000402                      BR     66$                                     ;; GET OVER THE ASCIZ  
7154                                     ;*  
7155 023776                               ;:67$:  
7156                                     ;:66$:
```



7156 023776 000672

BR 1\$

.SBTTL \* "SCHMITT TRIG 3" IN, "ST3 OUT" TESTS

```

;*
;*THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND
;*PROVIDING SCOPE LOOP CAPABILITIES FOR "SCHMITT TRIG 3"
;*AND "ST3 OUT".
;*
;*WHEN YOU LOAD AND START AT LOCATION 220, PROGRAM
;*CONTROL IS TRANSFERRED HERE. "STP2" PULSES ARE GENERATED
;*BY "LD STAT A H," + "BD10" H (MAIN STP2), PIN V ("STP2 OUT")
;*IS WIRED TO PIN T ("SCHMITT TRIG 3"), "SCHMITT TRIG 3" PULSES
;*GIVE US "ST3 OUT" PULSES. PIN L ("ST3 OUT") IS WIRED
;*TO PIN LL ("SCHMITT TRIG1"), AND "SCHMITT TRIG 1" WILL SET
;*CLOCK A'S STATUS REGISTER BIT 15.
;*IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIC.
;*AND ERROR SWITCH REGISTER OPTIONS ARE USED.
;*AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE
;*TEST. SW13=1 WILL INHIBIT THIS FEATURE.
;*

```

```

;*
;* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"
;*

```

```

;*YOU MUST WIRE PINS DD TO T OF J1 TOGETHER, AS WELL AS
;*PINS L TO BB OF J1 TOGETHER.
;*
;*TESTS LS210 AND LS214 SHOULD BE RUN FIRST.
;*

```

7186 024000

LS220:

7188 024000 005037 001104  
7189 024004 012737 177704 001210

1\$: CLR \$ICNT  
MOV #-60., \$PASS

```

;/CLEAR ITERATION COUNT
;/SET PASS COUNT.
;/NOTE: PASS COUNT USED ONLY
;/ TO DETECT 60 PASSES SO
;/ IT CAN GENERATE A CRLF.
;/ AFTER CRLF IT WILL BE ZEROED.
;/CLEAR CLOCK A.
;/CLEAR CLOCK B.

```

7195 024012  
7196 024012 005037 001356

2\$: CLR \$TMDAT

7198 ;\* MOV \$TMDAT, @ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR

7199 ;\* MOV \$TMDAT, @BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR

7200 ;\* ;/GENERATE A "STP2 OUT" PULSE.

7203 024036 005037 001356

CLR \$TMDAT

7205 ;\* MOV @ASR, \$TMDAT ;/READ DEVICE REG ASR, PUT DATA IN \$TMDAT.

7206 024052 052737 011000 001356 ;\* BIS #BIT12:BIT9, \$TMDAT

7207 ;\* MOV \$TMDAT, @ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR  
7208 ;\* ;/AT THIS POINT YOU SHOULD SEE AN



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7314  
7315  
7316  
7317

:(("A EVENT OUT") IS WIRED TO PIN LL ("SCHMITT TRIG 1"))  
:;"SCHMITT TRIG 1" PULSES WILL SET CLOCK A'S CSR BIT 15.  
:;"IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIQ.  
:;"AND ERROR SWITCH REGISTER OPTIONS ARE USED.  
:;"AN "\*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE TEST.  
:;"SW13=1 WILL INHIBIT THIS FEATURE.  
:;\*

:;\* PROBABLE SYNC POINT FOR THIS TEST:: "LD STAT B"  
:;\*

:;\* YOU MUST WIRE PINS VV AND BB OF J1 TOGETHER.  
:;\*

:;\* TEST LS210 SHOULD BE RUN FIRST.  
:;\*

024160 LS224:

024160 005037 001104 1\$: CLR \$ICNT  
024164 012737 177704 001210 MOV #-60.,\$PASS

:/CLEAR ITERATION COUNT  
:/SET PASS COUNT.  
:/NOTE: PASS COUNT USED ONLY  
/ TO DETECT 60 PASSES SO  
/ IT CAN GENERATE A CRLF.  
/ AFTER CRLF IT WILL BE ZEROED.  
:/CLEAR CLOCK A.  
:/CLEAR CLOCK B.

024172 005037 001356 2\$: CLR \$TMDAT

;\* MOV \$TMDAT,\$ASR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR  
;\* MOV \$TMDAT,\$BSR ;/ PUT DATA FROM \$TMDAT TO DEVICE REG BSR  
;/PRELOAD CLOCK A'S BUFFER + COUNT REGS.

024216 012737 177777 001356 MOV #-1,\$TMDAT

;/ PUT DATA FROM \$TMDAT TO DEVICE REG ABR  
;/RATE: 1MHZ, ENABLE COUNTER

024234 012737 001003 001356 MOV #1003,\$TMDAT

;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR  
;/HAS AN OVERFLOW OCCURRED?

024252 3\$:

024262 032737 000040 001356 ;\* MOV \$ASR,\$TMDAT  
BIT #BIT05,\$TMDAT ;/READ DEVICE REG ASR,PUT DATA IN \$TMDAT.

024300 001764 ;\* MOV \$TMDAT,\$ASR  
BEQ 3\$ ;/ PUT DATA FROM \$TMDAT TO DEVICE REG ASR

;/NO - THEN WAIT FOR IT.  
;/OVERFLOW SHOULD GO OUT AS  
;/ "A EVENT OUT" YOU SHOULD SEE  
;/ AN OUTPUT AT PIN VV.  
;/ THIS IN TURN IS BROUGHT  
;/ IN AS "SCHMITT TRIG 1" IN TO  
;/ SET CLOCK A'S CSR BIT 15.

```
7318  
7319  
7320  
7321  
7322 024312 105737 001126 ;* MOV @ASR,$BDDAT ;/DID CSR BIT 15 SET?  
7323 024316 100401 TSTB $BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.  
7324 BMI 4$ ;BR IF YES TO 4$
```

;;;\$>> ERROR <<\$

```
7328 024320 104000 ERROR ;ERROR "A EVENT OUT" PULSE  
7329 ;NOT DETECTED. HAVE YOU  
7330 ;WIRED IT RIGHT?  
7331
```

;;;\$>> ERROR <<\$

```
7335 024322 4$:  
7336  
7337 024322 032777 020000 154610 BIT #BIT13,@SWR ;/INHIBIT "*" TYPEOUT?  
7338 024330 001320 BNE 2$ ;/YES - IGNORE ANY UPDATES.  
7339  
7340 024332 005237 001104 INC $ICNT ;/UPDATE COUNT.  
7341 024336 001315 BNE 2$ ;/IF NOT DONE 65,324 TIMES,  
7342 ;/DO IT AGAIN.  
7343  
7344 024340 104401 024346 TYPE 65$ ;:TYPE ASCIZ STRING  
7345 024344 000401 BR 64$ ;:GET OVER THE ASCIZ  
7346 ;:65$: .ASCIZ ***  
7347 024350 64$:  
7348  
7349 024350 005237 001210 INC $PASS ;/DONE 60 PASSES?  
7350 024354 100706 BMI 2$ ;/NO - NO NEED FOR CR,LF.  
7351 024356 104401 024364 TYPE 67$ ;:TYPE ASCIZ STRING  
7352 024362 000402 BR 66$ ;:GET OVER THE ASCIZ  
7353 ;:67$: .ASCIZ <15><12>##  
7354 024370 66$:  
7355 024370 000673 BR 1$
```

```
7357 .SBTTL * "B EVENT OUT" TEST  
7358 ;*  
7359 ;*THIS IS A SPECIAL SECTION DEVOTED FOR TESTING AND  
7360 ;*PROVIDING SCOPE LOOP CAPABILITIES FOR "B EVENT OUT".  
7361 ;*  
7362 ;*WHEN YOU LOAD AND START AT LOCATION 230, PROGRAM  
7363 ;*CONTROL IS TRANSFERRED HERE. "B EVENT OUT" PULSES ARE  
7364 ;*GENERATED BY CLOCK B OVERFLOWS. PIN TT  
7365 ;*("B EVENT OUT") IS WIRED TO PIN LL ("SCHMITT TRIG 1")  
7366 ;*"SCHMITT TRIG 1" PULSES WILL SET CLOCK A'S CSR BIT 15.  
7367 ;*IF AN ERROR IS DETECTED, NORMAL ERROR REPORTING TECHNIQ.  
7368 ;*AND ERROR SWITCH REGISTER OPTIONS ARE USED.  
7369 ;*AN "*" IS TYPED AFTER EACH 65,324 LOOPS THROUGH THE TEST.  
7370 ;*SW13=1 WILL INHIBIT THIS FEATURE.  
7371
```

```

7372 ;*
7373 ;*
7374 ;* PROBABLE SYNC POINT FOR THIS TEST:: "LD BUFF B"
7375 ;*
7376 ;* YOU MUST WIRE PINS TT AND BB OF J1 TOGETHER.
7377 ;*
7378 ;* TEST LS210 SHOULD BE RUN FIRST.
7379 ;*
7380
7381 024372 LS230:
7382
7383 024372 005037 001104 1$: CLR $ICNT ;/CLEAR ITERATION COUNT
7384 024376 012737 177704 001210 MOV #-60.,$PASS ;/SET PASS COUNT.
7385 ;/NOTE: PASS COUNT USED ONLY
7386 ;/ TO DETECT 60 PASSES SO
7387 ;/ IT CAN GENERATE A CRLF.
7388 ;/ AFTER CRLF IT WILL BE ZEROED.
7389 ;/CLEAR CLOCK A.
7390 024404 2$: ;/CLEAR CLOCK B.
7391 024404 005037 001356 CLR $TMDAT
7392
7393 ;* MOV $TMDAT,$ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
7394 ;* MOV $TMDAT,$BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
7395 ;/PRELOAD CLOCK B'S BUFFER + COUNT REGS.
7396
7397 024430 012737 177777 001356 MOV #-1,$TMDAT
7398
7399 ;* MOV $TMDAT,$BBR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BBR
7400 024446 012737 001000 001356 MOV #1000,$TMDAT
7401 ;* MOV $TMDAT,$ASR ;/ PUT DATA FROM $TMDAT TO DEVICE REG ASR
7402 ;/RATE: 1MHZ, ENABLE COUNTER
7403 ;/HAS AN OVERFLOW OCCURRED?
7404
7405 024464 012737 000003 001356 MOV #3,$TMDAT
7406
7407 ;* MOV $TMDAT,$BSR ;/ PUT DATA FROM $TMDAT TO DEVICE REG BSR
7408 024502 3$: ;/READ DEVICE REG BSR,PUT DATA IN $TMDAT.
7409 ;* MOV $BSR,$TMDAT
7410 024512 032737 000200 001356 BIT #BIT07,$TMDAT
7411 024520 001770 BEQ 3$ ;/NO -THEN WAIT FOR IT.
7412 ;/OVERFLOW SHOULD GO OUT AS
7413 ;/"B EVENT OUT". YOU SHOULD SEE
7414 ;/AN OUTPUT AT PIN TT.
7415 ;/THIS IN TURN IS BROUGHT
7416 ;/IN AS "SCHMITT TRIG 1" IN TO
7417 ;/SET CLOCK A'S CSR BIT 15.
7418
7419 ;/DID CSR BIT 15 SET?
7420
7421
7422
7423
7424 ;* MOV $ASR,$BDDAT ;/READ DEVICE REG ASR,PUT DATA IN $BDDAT.
7425

```

F01

MAINDEC-11-DRLPG-A  
DRLPG.P11 \*

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"B EVENT OUT" TEST

SEQ 0212

7426 024532 105737 001126 TSTB \$BDDAT  
7427 024536 100401 BMI 4\$ ;BR IF YES TO 4\$  
7428

;;; \$> ERROR <<\$

7432 024540 104000 ERROR ;ERROR "B EVENT OUT" PULSE  
7433 ;NOT DETECTED. HAVE YOU  
7434 ;WIRED IT RIGHT?  
7435

;;; \$> ERROR <<\$

7439 024542 4\$:  
7440  
7441 024542 032777 020000 154370 BIT #BIT13, @SWR ;/INHIBIT "\*" TYPEOUT?  
7442 024550 001315 BNE 2\$ ;/YES - IGNORE ANY UPDATES.  
7443  
7444 024552 005237 001104 INC \$ICNT ;/UPDATE COUNT.  
7445 024556 001312 BNE 2\$ ;/IF NOT DONE 65,324 TIMES,  
7446 ;/DO IT AGAIN.  
7447

7448 024560 104401 024566 TYPE 65\$ ;;TYPE ASCIZ STRING  
7449 024564 000401 BR 64\$ ;;GET OVER THE ASCIZ  
7450  
7451 024570 64\$: .ASCIZ \*\*  
7452

7453 024570 005237 001210 INC \$PASS ;/DONE 60 PASSES?  
7454 024574 100703 BMI 2\$ ;/NO - NO NEED FOR CR, LF.  
7455 024576 104401 024604 TYPE 67\$ ;/TYPE ASCIZ STRING  
7456 024602 000402 BR 66\$ ;/GET OVER THE ASCIZ  
7457

7458 024610 66\$: .ASCIZ <15><12>##  
7459 024610 000670 BR 1\$  
7460

7461 ;\*ROUTINE TO HANDLE TRAPS TO IOC 4, 10 AND .  
7462 ;\*INTERRUPTS TO WRONG VECTORS.  
7463 ;\*.+2, IOTT(TRAPS) WERE PUT IN LOCATIONS 4-1000  
7464

7465  
7466  
7467 024612 IOTRD:  
7468 024612 011637 024762 MOV (R6), 2\$ ;GET WHERE WE TRAPPED TO.  
7469 024616 162737 000004 024762 SUB #4, 2\$ ;=WHERE R6 RETURN 10-4  
7470 024624 104401 024632 TYPE 65\$ ;/TYPE ASCIZ STRING  
7471 024630 000412 BR 64\$ ;/GET OVER THE ASCIZ  
7472 64\$: .ASCIZ <15><12>#ILLEGAL TRAP TO: #  
7473

7474  
7475 024656 013746 024762 MOV 2\$, -(SP) ;;SAVE 2\$ FOR TYPEOUT  
7476 024662 104402 TPOC ;/GO TYPE--OCTAL ASCII(ALL DIGITS)  
7477  
7478 024664 104401 024672 TYPE 67\$ ;/TYPE ASCIZ STRING  
7479 024670 000407 BR 66\$ ;/GET OVER THE ASCIZ

```

7480           ;;67$: .ASCIZ  # FROM LOC.: #
7481 024710    66$:
7482
7483 024710    062706 000004      ADD      #4,R6          ;POINT TO WHERE WE TRAPPED FROM.
7484
7485 024714    011637 024764      MOV      (R6),3$      ;PICK UP LOC
7486 024720    162737 000002 024764  SUB      #2,3$        ;FROM REAL ADDR.
7487 024726    013746 024764      MOV      3$,-(SP)    ;SAVE 3$ FOR TYPEOUT
7488 024732    104402      TYPOC          ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
7489
7490 024734    023727 024762 000004  CMP      2$,#4        ;DID WE TRAP TO LOC 4?
7491 024742    001405      BEQ      1$          ;IF SO - DON'T RETURN!
7492 024744    023727 024762 000010  CMP      2$,#10      ;DID WE TRAP TO LOC. 10?
7493 024752    001401      BEQ      1$          ;ID SO - DON'T RETURN!
7494 024754    000002      RTI              ;TRY RETURNING.
7495
7496
```

;;;\$>> ERROR <<\$

```

7500 024756    000000           1$: HALT          ;WE STOPPED HERE BECAUSE WE TRAPPED
7501 024760    000776           BR           1$      ;TO LOC 4 OR LOC 10. THIS IS A
7502                                     ;FATAL CONDITION THAT WE CAN NOT
7503                                     ;RECOVER FROM.
7504
7505
```

;;;\$>> ERROR <<\$

```

7509 024762    000000           2$: .WORD  0          ;USED BY IOTRAP TO STORE WHERE WE TRAPPED TO.
7510 024764    000000           3$: .WORD  0          ;USED BY IOTRAP TO STORE WHERE WE TRAPPED FROM.
7511                                     .SBTTL
7512                                     .SBTTL *SYSMAC ROUTINES
7513                                     .SBTTL
7514                                     .SBTTL
7515                                     .SBTTL BINARY TO OCTAL (ASCII) AND TYPE
7516
7517 *****
7518 *THIS ROUTINE IS USED TO cHANGE A 16-BIT BINARY NUMBER TO A 6-DIGIT
7519 *OCTAL (ASCII) NUMBER AND TYPE IT.
7520 *$TYPOS---ENTER HERE TO SETUP SUPPRESS ZEROS AND NUMBER OF DIGITS TO TYPE
7521 *CALL:
7522 *      MOV      NUM,-(SP)        ;;NUMBER TO BE TYPED
7523 *      TYPOS          ;;CALL FOR TYPEOUT
7524 *      .BYTE  N           ;;N=1 TO 6 FOR NUMBER OF DIGITS TO TYPE
7525 *      .BYTE  M           ;;M=1 OR 0
7526 *                                  ;;1=TYPE LEADING ZEROS
7527 *                                  ;;0=SUPPRESS LEADING ZEROS
7528 *
7529 *$TYPON----ENTER HERE TO tYPE OUT WITH THE SAME PARAMETERS AS THE LAST
7530 *$TYPOS OR $TYPOC
7531 *CALL:
7532 *      MOV      NUM,-(SP)        ;;NUMBER TO BE TYPED
7533 *      TYPON           ;;CALL FOR TYPEOUT
```





```

7588 025207 000
7589 025210 000
7590 025211 000
7591 025212 000000
7592
7593
7594
7595
7596
7597
7598
7599
7600
7601
7602
7603
7604
7605
7606 025214
7607 025214 104407
7608 025216 105237 001103
7609 025222 001775
7610 025224 013777 001102 153710
7611 025232 032777 002000 153700
7612 025240 001402
7613 025242 104401 001172
7614 025246 005237 001112
7615 025252 011637 001116
7616 025256 162737 000002 001116
7617 025264 117737 153626 001114
7618 025272 032777 020000 153640
7619 025300 001004
7620 025302 004737
7621 025306 104401 001177
7622 025312
7623 025312 122737 000001 001222
7624 025320 001007
7625 025322 113737 001114 025334
7626 025330 004737 027420
7627 025334 000
7628 025335 000
7629 025336 000777
7630 025340 005777 153574
7631 025344 100002
7632 025346 000000
7633 025350 104407
7634 025352 032777 001000 153560
7635 025360 001402
7636 025362 013716 001110
7637 025366 005737 001170
7638 025372 001402
7639 025374 013716 001170
7640 025400
7641 025400 000002

```

```

.SOCNT: .BYTE 0 ;; TERMINATOR FOR TYPE ROUTINE
.SOFILL: .BYTE 0 ;; OCTAL DIGIT COUNTER
.SOMODE: .WORD 0 ;; ZERO FILL SWITCH
.SBTTL: .SBTTL ERROR HANDLER ROUTINE ;; NUMBER OF DIGITS TO TYPE

```

```

*****
*THIS ROUTINE WILL INCREMENT THE ERROR FLAG AND THE ERROR COUNT,
*SAVE THE ERROR ITEM NUMBER AND THE ADDRESS OF THE ERROR CALL
*AND GO TO SERRTYP ON ERROR
*THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
*SW15=1 HALT ON ERROR
*SW13=1 INHIBIT ERROR TYPEOUTS
*SW10=1 BELL ON ERROR
*SW09=1 LOOP ON ERROR
*CALL
* ERROR N ;;ERROR=EMT AND N=ERROR ITEM NUMBER

```

```

SERROR:
7$: CKSWR ;; TEST FOR CHANGE IN SOFT-SWR
INCB ;; SET THE ERROR FLAG
BEQ 7$ DON'T LET THE FLAG GO TO ZERO
MOV STSNM, @DISPLAY ;; DISPLAY TEST NUMBER AND ERROR FLAG
BIT #BIT10, @SWR ;; BELL ON ERROR?
BEQ 1$ NO - SKIP
TYPE $BELL ;; RING BELL
INC $ERTTL ;; COUNT THE NUMBER OF ERRORS
MOV (SP), $ERRPC ;; GET ADDRESS OF ERROR INSTRUCTION
SUB #2, $ERRPC
MOVB @ERRPC, $ITEMB ;; STRIP AND SAVE THE ERROR ITEM CODE
BIT #BIT13, @SWR ;; SKIP TYPEOUT IF SET
BNE 20$ ;; SKIP TYPEOUTS
JSR PC, SERRTYP ;; GO TO USER ERROR ROUTINE
TYPE , $CRLF

20$: CMPB #APTEMV, $ENV ;; RUNNING IN APT MODE
BNE 2$ NO, SKIP APT ERROR REPORT
MOVB $ITEMB, 21$ ;; SET ITEM NUMBER AS ERROR NUMBER
JSR PC, SATY4 ;; REPORT FATAL ERROR TO APT

21$: .BYTE 0
.BYTE 0

22$: BR 22$ ;; APT ERROR LOOP
2$: TST @SWR ;; HALT ON ERROR
BPL 3$ SKIP IF CONTINUE
HALT ;; HALT ON ERROR!
CKSWR ;; TEST FOR CHANGE IN SOFT-SWR
BIT #BIT09, @SWR ;; LOOP ON ERROR SWITCH SET?
BEQ 4$ BR IF NO
MOV $LPERR, (SP) ;; FUDGE RETURN FOR LOOPING
TST $ESCAPE ;; CHECK FOR AN ESCAPE ADDRESS
BEQ 5$ BR IF NONE
MOV $ESCAPE, (SP) ;; FUDGE RETURN ADDRESS FOR ESCAPE

5$: RTI ;; RETURN

```

```

7642
7643
7644
7645
7646
7647
7648
7649 025402
7650 025402 104401 001177
7651 025406 010046
7652 025410 005000
7653 025412 153700 001114
7654 025416 001004
7655
7656 025420 013746 001116
7657
7658 025424 104402
7659 025426 000426
7660 025430 005300
7661 025432 006300
7662 025434 006300
7663 025436 006300
7664 025440 062700 001360
7665 025444 012037 025454
7666 025450 001404
7667 025452 104401
7668 025454 000000
7669 025456 104401 001177
7670 025462 012037 025472
7671 025466 001404
7672 025470 104401
7673 025472 000000
7674 025474 104401 001177
7675 025500 011000
7676 025502 001004
7677 025504 012600
7678 025506 104401 001177
7679 025512 000207
7680 025514
7681 025514 013046
7682 025516 104402
7683 025520 005710
7684 025522 001770
7685 025524 104401 025532
7686 025530 000771
7687 025532 020040 000
7688 025536
7689
7690
7691
7692
7693
7694
7695

```

.SBTTL ERROR MESSAGE TYPEOUT ROUTINE

```

*****
*THIS ROUTINE USES THE "ITEM CONTROL BYTE" ($ITEMB) TO DETERMINE WHICH
*ERROR IS TO BE REPORTED. IT THEN OBTAINS, FROM THE "ERROR TABLE" ($ERRTB),
*AND REPORTS THE APPROPRIATE INFORMATION CONCERNING THE ERROR.

```

```

SERRTYP:
      TYPE      $CRLF      ;; "CARRIAGE RETURN" & "LINE FEED"
      MOV      RO,-(SP)    ;; SAVE RO
      CLR      RO          ;; PICKUP THE ITEM INDEX
      BISB     @#$ITEMB,RO
      BNE      1$         ;; IF ITEM NUMBER IS ZERO, JUST
                          ;; TYPE THE PC OF THE ERROR
      MOV      $ERRPC,-(SP) ;; SAVE $ERRPC FOR TYPEOUT
                          ;; ERROR ADDRESS
                          ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
                          ;; GET OUT
                          ;; ADJUST THE INDEX SO THAT IT WILL
                          ;; WORK FOR THE ERROR TABLE
      TYPOC
      BR      6$
1$:   DEC      RO
      ASL     RO
      ASL     RO
      ASL     RO
      ADD     @$ERRTB,RO   ;; FORM TABLE POINTER
      MOV     (RO)+,2$    ;; PICKUP "ERROR MESSAGE" POINTER
      BEQ     3$         ;; SKIP TYPEOUT IF NO POINTER
      TYPE   1$         ;; TYPE THE "ERROR MESSAGE"
                          ;; "ERROR MESSAGE" POINTER GOES HERE
      TYPE   $CRLF      ;; "CARRIAGE RETURN" & "LINE FEED"
      MOV     (RO)+,4$    ;; PICKUP "DATA HEADER" POINTER
      BEQ     5$         ;; SKIP TYPEOUT IF 0
      TYPE   1$         ;; TYPE THE "DATA HEADER"
                          ;; "DATA HEADER" POINTER GOES HERE
      TYPE   $CRLF      ;; "CARRIAGE RETURN" & "LINE FEED"
      MOV     (RO),RO     ;; PICKUP "DATA TABLE" POINTER
      BNE     7$         ;; GO TYPE THE DATA
      MOV     (SP)+,RO    ;; RESTORE RO
      TYPE   $CRLF      ;; "CARRIAGE RETURN" & "LINE FEED"
      RTS     PC         ;; RETURN
      MOV     @2(RO)+,-(SP) ;; SAVE @2(RO)+ FOR TYPEOUT
      TYPOC
      TST     (RO)       ;; GO TYPE--OCTAL ASCII(ALL DIGITS)
                          ;; IS THERE ANOTHER NUMBER?
      BEQ     6$         ;; BR IF NO
      TYPE   2$         ;; TYPE TWO(2) SPACES
      BR     7$         ;; LOOP
8$:   .ASCIZ  / /       ;; TWO(2) SPACES
      .EVEN

```

.SBTTL CONVERT BINARY TO DECIMAL AND TYPE ROUTINE

```

*****
*THIS ROUTINE IS USED TO CHANGE A 16-BIT BINARY NUMBER TO A 5-DIGIT
*SIGNED DECIMAL (ASCII) NUMBER AND TYPE IT. DEPENDING ON WHETHER THE
*NUMBER IS POSITIVE OR NEGATIVE A SPACE OR A MINUS SIGN WILL BE TYPED
*BEFORE THE FIRST DIGIT OF THE NUMBER. LEADING ZEROS WILL ALWAYS BE

```

```

7696                                     ;*REPLACED WITH SPACES.
7697                                     ;*CALL:
7698                                     ;*      MOV      NUM,-(SP)          ;;PUT THE BINARY NUMBER ON THE STACK
7699                                     ;*      TYPDS                    ;;GO TO THE ROUTINE
7700
7701 025536                               $TYPDS:
7702 025536 010046                       MOV      R0,-(SP)          ;;PUSH R0 ON STACK
7703 025540 010146                       MOV      R1,-(SP)          ;;PUSH R1 ON STACK
7704 025542 010246                       MOV      R2,-(SP)          ;;PUSH R2 ON STACK
7705 025544 010346                       MOV      R3,-(SP)          ;;PUSH R3 ON STACK
7706 025546 010546                       MOV      R5,-(SP)          ;;PUSH R5 ON STACK
7707 025550 012746 020200                MOV      #20200,-(SP)     ;;SET BLANK SWITCH AND SIGN
7708 025554 016605 000020                MOV      20(SP),R5        ;;GET THE INPUT NUMBER
7709 025560 100004                       BPL      1$                ;;BR IF INPUT IS POS.
7710 025562 005405                       NEG      R5                ;;MAKE THE BINARY NUMBER POS.
7711 025564 112766 000055 000001        MOVVB    #'-,1(SP)        ;;MAKE THE ASCII NUMBER NEG.
7712 025572 005000                       1$:     CLR      R0                ;;ZERO THE CONSTANTS INDEX
7713 025574 012703 025752                MOV      #SDBLK,R3        ;;SETUP THE OUTPUT POINTER
7714 025600 112723 000040                MOVVB    #' ,(R3)+        ;;SET THE FIRST CHARACTER TO A BLANK
7715 025604 005002                       2$:     CLR      R2                ;;CLEAR THE BCD NUMBER
7716 025606 016001 025742                MOV      $DTBL(R0),R1     ;;GET THE CONSTANT
7717 025612 160105                       3$:     SUB      R1,R5                ;;FORM THIS BCD DIGIT
7718 025614 002402                       BLT     4$                ;;BR IF DONE
7719 025616 005202                       INC     R2                ;;INCREASE THE BCD DIGIT BY 1
7720 025620 000774                       BR      3$
7721 025622 060105                       4$:     ADD     R1,R5                ;;ADD BACK THE CONSTANT
7722 025624 005702                       TST     R2                ;;CHECK IF BCD DIGIT=0
7723 025626 001002                       BNE     5$                ;;FALL THROUGH IF 0
7724 025630 105716                       TSTB   (SP)                ;;STILL DOING LEADING 0'S?
7725 025632 100407                       BMI     7$                ;;BR IF YES
7726 025634 106316                       5$:     ASLB   (SP)                ;;MSD?
7727 025636 103003                       BCC     6$                ;;BR IF NO
7728 025640 116663 000001 177777        MOVVB    1(SP),-1(R3)     ;;YES--SET THE SIGN
7729 025646 052702 000060                BIS     #'0,R2            ;;MAKE THE BCD DIGIT ASCII
7730 025652 052702 000040                6$:     BIS     #' ,R2            ;;MAKE IT A SPACE IF NOT ALREADY A DIGIT
7731 025656 110223                       7$:     MOVVB  R2,(R3)+        ;;PUT THIS CHARACTER IN THE OUTPUT BUFFER
7732 025660 005720                       TST     (R0)+            ;;JUST INCREMENTING
7733 025662 020027 000010                CMP     R0,#10           ;;CHECK THE TABLE INDEX
7734 025666 002746                       BLT     2$                ;;GO DO THE NEXT DIGIT
7735 025670 003002                       BGT     8$                ;;GO TO EXIT
7736 025672 010502                       MOV     R5,R2            ;;GET THE LSD
7737 025674 000764                       BR      6$                ;;GO CHANGE TO ASCII
7738 025676 105726                       8$:     TSTB  (SP)+          ;;WAS THE LSD THE FIRST NON-ZERO?
7739 025700 100003                       BPL     9$                ;;BR IF NO
7740 025702 116663 177777 177776        MOVVB   -1(SP),-2(R3)    ;;YES--SET THE SIGN FOR TYPING
7741 025710 105013                       9$:     CLRB  (R3)            ;;SET THE TERMINATOR
7742 025712 012605                       MOV     (SP)+,R5        ;;POP STACK INTO R5
7743 025714 012603                       MOV     (SP)+,R3        ;;POP STACK INTO R3
7744 025716 012602                       MOV     (SP)+,R2        ;;POP STACK INTO R2
7745 025720 012601                       MOV     (SP)+,R1        ;;POP STACK INTO R1
7746 025722 012600                       MOV     (SP)+,R0        ;;POP STACK INTO R0
7747 025724 104401 025752                TYPE    $SDBLK           ;;NOW TYPE THE NUMBER
7748 025730 016666 000002 000004        MOV     2(SP),4(SP)     ;;ADJUST THE STACK
7749 025736 012616                       MOV     (SP)+,(SP)

```

```

7750 025740 000002          RTI          ;;RETURN TO uSER
7751 025742 023420          $DTBL: 10000.
7752 025744 001750          1000.
7753 025746 000144          100.
7754 025750 000012          10.
7755 025752 000004          $DBLK:  BLKW  4
7756                                     .SBTTL  SCOPE HANDLER ROUTINE
7757
7758                                     ;*****
7759                                     ;THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
7760                                     ;AND LOAD THE TEST NUMBER($STS:NM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
7761                                     ;AND LOAD THE ERROR FLAG ($ERFLG) INTO DISPLAY<15:08>
7762                                     ;THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
7763                                     ;SW14=1      LOOP ON TEST
7764                                     ;SW11=1      INHIBIT ITERATIONS
7765                                     ;SW09=1      LOOP ON ERROR
7766                                     ;SW08=1      LOOP ON TEST IN SWR<7:0>
7767                                     ;CALL
7768                                     ;*      SCOPE          ;;SCOPE=IOT
7769
7770 025762          $SCOPE:
7771 025762 104407          CKSWR
7772 025764 032777 040000 153146 1$:  BIT    #BIT14, $SWR      ;; TEST FOR CHANGE IN SOFT-SWR
7773 025772 001114          BNE    $OVER        ;; LOOP ON PRESENT TEST?
7774                                     ;*****START OF CODE FOR THE XOR TESTER*****
7775 025774 000416          $XTSTR: BR    6$      ;; YES IF SW14=1
7776                                     ; IF RUNNING ON THE "XOR" TESTER CHANGE
7777 025776 013746 000004          MOV    @#ERRVEC, -(SP) ;; THIS INSTRUCTION TO A "NOP" (NOP=240)
7778 026002 012737 026022 000004          MOV    #5$, @#ERRVEC ;; SAVE THE CONTENTS OF THE ERROR VECTOR
7779 026010 005737 177060          TST   @#177060      ;; SET FOR TIMEOUT
7780 026014 012637 000004          MOV    (SP)+, @#ERRVEC ;; TIME OUT ON XOR?
7781 026020 000463          BR    $SVLAD        ;; RESTORE THE ERROR VECTOR
7782 026022 022626          5$:  CMP    (SP)+, (SP)+ ;; GO TO THE NEXT TEST
7783 026024 012637 000004          MOV    (SP)+, @#ERRVEC ;; CLEAR THE STACK AFTER A TIME OUT
7784 026030 000423          BR    7$          ;; RESTORE THE ERROR VECTOR
7785 026032          6$: ; *****END OF CODE FOR THE XOR TESTER*****
7786 026032 032777 000400 153100          BIT    #BIT08, $SWR ;; LOOP ON SPEC. TEST?
7787 026040 001404          BEQ   2$          ;; BR IF NO
7788 026042 127737 153072 001102          CMPB  @SWR, $STNM  ;; ON THE RIGHT TEST? SWR<7:0>
7789 026050 001465          BEQ   $OVER        ;; BR IF YES
7790 026052 105737 001103          2$:  TSTB  $ERFLG      ;; HAS AN ERROR OCCURRED?
7791 026056 001421          BEQ   3$          ;; BR IF NO
7792 026060 123737 001115 001103          CMPB  $ERMAX, $ERFLG ;; MAX. ERRORS FOR THIS TEST OCCURRED?
7793 026066 101015          BHI   3$          ;; BR IF NO
7794 026070 032777 001000 153042          BIT    #BIT09, $SWR ;; LOOP ON ERROR?
7795 026076 001404          BEQ   4$          ;; BR IF NO
7796 026100 013737 001110 001106          7$:  MOV    $LPERR, $LPADR ;; SET LOOP ADDRESS TO LAST SCOPE
7797 026106 000446          BR    $OVER
7798 026110 105037 001103          4$:  CLRB  $ERFLG      ;; ZERO THE ERROR FLAG
7799 026114 005037 001166          CLR   $TIMES      ;; CLEAR THE NUMBER OF ITERATIONS TO MAKE
7800 026120 000415          BR    1$          ;; ESCAPE TO THE NEXT TEST
7801 026122 032777 004000 153010          3$:  BIT    #BIT11, $SWR ;; INHIBIT ITERATIONS?
7802 026130 001011          BNE   1$          ;; BR IF YES
7803 026132 005737 001210          TST   $PASS        ;; IF FIRST PASS OF PROGRAM

```

```

7804 026136 001406          BEQ      1$
7805 026140 005237 001104    INC      $ICNT          ;; INHIBIT ITERATIONS
7806 026144 023737 001166 001104    CMP      $TIMES,$ICNT  ;; INCREMENT ITERATION COUNT
7807 026152 002024          BGE      $OVER        ;; CHECK THE NUMBER OF ITERATIONS MADE
7808 026154 012737 000001 001104 1$:  MOV      #1,$ICNT     ;; BR IF MORE ITERATION REQUIRED
7809 026162 013737 026240 001166    MOV      $MXCNT,$TIMES  ;; REINITIALIZE THE ITERATION COUNTER
7810 026170 105237 001102          $SSVLAD: INCB     $STSTNM  ;; SET NUMBER OF ITERATIONS TO DO
7811 026174 113737 001102 001206    MOV      $STSTNM,$STSTNM  ;; COUNT TEST NUMBERS
7812 026202 011637 001106          MOV      (SP), $LPADR   ;; SET TEST NUMBER IN APT MAILBOX
7813 026206 011637 001110          MOV      (SP), $LPERR   ;; SAVE SCOPE LOOP ADDRESS
7814 026212 005037 001170          CLR      $ESCAPE      ;; SAVE ERROR LOOP ADDRESS
7815 026216 112737 000001 001115    MOV      #1,$ERMAX     ;; CLEAR THE ESCAPE FROM ERROR ADDRESS
7816 026224 013777 001102 152710  $OVER:  MOV      $STSTNM,$DISPLAY  ;; ONLY ALLOW ONE(I) ERROR ON NEXT TEST
7817 026232 013716 001106          MOV      $LPADR,(SP)   ;; DISPLAY TEST NUMBER
7818 026236 000002          RTI                    ;; FUDGE RETURN ADDRESS
7819 026240 000012          $MXCNT: 10.          ;; FIXES P5
7820          .SBTTL READ AN OCTAL NUMBER FROM THE TTY  ;; MAX. NUMBER OF ITERATIONS
7821
7822          ;; *****
7823          ;; *THIS ROUTINE WILL READ AN OCTAL (ASCII) NUMBER FROM THE TTY AND
7824          ;; *CHANGE IT TO BINARY.
7825          ;; *CALL:
7826          ;; *      RDOCT
7827          ;; *      RETURN HERE
7828          ;; *
7829          ;; *      READ AN OCTAL NUMBER
7830          ;; *      LOW ORDER BITS ARE ON TOP OF THE STACK
7831          ;; *      HIGH ORDER BITS ARE IN $HIOCT
7830 026242 011646          $RDOCT: MOV      (SP), -(SP)  ;; PROVIDE SPACE FOR THE
7831 026244 016666 000004 000002    MOV      4(SP), 2(SP)  ;; INPUT NUMBER
7832 026252 010046          MOV      R0, -(SP)    ;; PUSH R0 ON STACK
7833 026254 010146          MOV      R1, -(SP)    ;; PUSH R1 ON STACK
7834 026256 010246          MOV      R2, -(SP)    ;; PUSH R2 ON STACK
7835 026260 104411          1$:  RDLIN          ;; READ AN ASCII LINE
7836 026262 012600          MOV      (SP)+, R0    ;; GET ADDRESS OF 1ST CHARACTER
7837 026264 005001          CLR      R1          ;; CLEAR DATA WORD
7838 026266 005002          CLR      R2
7839 026270 112046          2$:  MOV      (R0)+, -(SP)  ;; PICKUP THIS CHARACTER
7840 026272 001412          BEQ      3$          ;; IF ZERO GET OUT
7841 026274 006301          ASL      R1          ;; *2
7842 026276 006102          ROL      R2
7843 026300 006301          ASL      R1          ;; *4
7844 026302 006102          ROL      R2
7845 026304 006301          ASL      R1          ;; *8
7846 026306 006102          ROL      R2
7847 026310 042716 177770          BIC      #1C7,(SP)    ;; STRIP THE ASCII JUNK
7848 026314 062601          ADD      (SP)+, R1    ;; ADD IN THIS DIGIT
7849 026316 000764          BR      2$          ;; LOOP
7850 026320 005726          3$:  TST      (SP)+      ;; CLEAN TERMINATOR FROM STACK
7851 026322 010166 000012          MOV      R1, 12(SP)  ;; SAVE THE RESULT
7852 026326 010237 026342          MOV      R2, $HIOCT
7853 026332 012602          MOV      (SP)+, R2
7854 026334 012601          MOV      (SP)+, R1
7855 026336 012600          MOV      (SP)+, R0
7856 026340 000002          RTI                    ;; RETURN
7857 026342 000000          $HIOCT: .WORD      0  ;; HIGH ORDER BITS GO HERE

```

```

7858 .SBTTL TTY INPUT ROUTINE
7859
7860 ;:*****
7861 .ENABL LSB
7862
7863 ;:*****
7864 ;*SOFTWARE SWITCH REGISTER CHANGE ROUTINE.
7865 ;*ROUTINE IS ENTERED FROM THE TRAP HANDLER, AND WILL
7866 ;*SERVICE THE TEST FOR CHANGE IN SOFTWARE SWITCH REGISTER TRAP CALL
7867 ;*WHEN OPERATING IN TTY FLAG MODE.
7868 026344 022737 000176 001140 $CKSWR: CMP #SWREG,SWR ;: IS THE SOFT-SWR SELECTED?
7869 026352 001074 BNE 15$ ;: BRANCH IF NO
7870 026354 105777 152564 TSTB @STKS ;: CHAR THERE?
7871 026360 100071 BPL 15$ ;: IF NO, DON'T WAIT AROUND
7872 026362 117746 152560 MOVB @STKB,-(SP) ;: SAVE THE CHAR
7873 026366 042716 177600 BIC #C177,(SP) ;: STRIP-OFF THE ASCII
7874 026372 022726 000007 CMP #7,(SP)+ ;: IS IT A CONTROL G?
7875 026376 001062 BNE 15$ ;: NO, RETURN TO USER
7876 026400 123727 001134 000001 CMPB $AUTOB,#1 ;: ARE WE RUNNING IN AUTO-MODE?
7877 026406 001456 BEQ 15$ ;: BRANCH IF YES
7878
7879 026410 104401 027071 $GTSWR: TYPE , $CNTLG ;: ECHO THE CONTROL-G (↑G)
7880 026414 104401 027076 TYPE $MSWR ;: TYPE CURRENT CONTENTS
7881 026420 013746 000176 MOV $WREG,-(SP) ;: SAVE SWREG FOR TYPEOUT
7882 026424 104402 TYPOC ;: GO TYPE--OCTAL ASCII(ALL DIGITS)
7883 026426 104401 027107 TYPE , $MN&W ;: PROMPT FOR NEW SWR
7884 026432 005046 19$: CLR -(SP) ;: CLEAR COUNTER
7885 026434 005046 CLR -(SP) ;: THE NEW SWR
7886 026436 105777 152502 7$: TSTB @STKS ;: CHAR THERE?
7887 026442 100375 BPL 7$ ;: IF NOT TRY AGAIN
7888
7889 026444 117746 152476 MOVB @STKB,-(SP) ;: PICK UP CHAR
7890 026450 042716 177600 BIC #C177,(SP) ;: MAKE IT 7-BIT ASCII
7891
7892
7893
7894 026454 021627 000025 9$: CMP (SP),#25 ;: IS IT A CONTROL-U?
7895 026460 001005 BNE 10$ ;: BRANCH IF NOT
7896 026462 104401 027064 TYPE , $CNTLU ;: YES, ECHO CONTROL-U (↑U)
7897 026466 062706 000006 20$: ADD #6,SP ;: IGNORE PREVIOUS INPUT
7898 026472 000757 BR 19$ ;: LET'S TRY IT AGAIN
7899
7900
7901 026474 021627 000015 10$: CMP (SP),#15 ;: IS IT A <CR>?
7902 026500 001022 BNE 16$ ;: BRANCH IF NO
7903 026502 005766 000004 TST 4(SP) ;: YES, IS IT THE FIRST CHAR?
7904 026506 001403 BEQ 11$ ;: BRANCH IF YES
7905 026510 016677 000002 152422 MOV 2(SP),@SWR ;: SAVE NEW SWR
7906 026516 062706 000006 11$: ADD #6,SP ;: CLEAR UP STACK
7907 026522 104401 001177 14$: TYPE , $CRLF ;: ECHO <CR> AND <LF>
7908 026526 123727 001135 000001 CMPB $INTAG,#1 ;: RE-ENABLE TTY KBD INTERRUPTS?
7909 026534 001003 BNE 15$ ;: BRANCH IF NOT
7910 026536 012777 000100 152400 MOV #100,@STKS ;: RE-ENABLE TTY KBD INTERRUPTS
7911 026544 000002 15$: RTI ;: RETURN

```

```

7912 026546 004737 027332      16$: JSR    PC,$TYPEC      ;; ECHO CHAR
7913 026552 021627 000060      CMP    (SP),#60          ;; CHAR < 0?
7914 026556 002420              BLT    18$              ;; BRANCH IF YES
7915 026560 021627 000067      CMP    (SP),#67          ;; CHAR > 7?
7916 026564 003015              BGT    18$              ;; BRANCH IF YES
7917 026566 042726 000060      BIC    #60,(SP)+        ;; STRIP-OFF ASCII
7918 026572 005766 000002      TST    2(SF)            ;; IS THIS THE FIRST CHAR
7919 026576 001403              BEQ    17$              ;; BRANCH IF YES
7920 026600 006316              ASL    (SP)              ;; NO, SHIFT PRESENT
7921 026602 006316              ASL    (SP)              ;; CHAR OVER TO MAKE
7922 026604 006316              ASL    (SP)              ;; ROOM FOR NEW ONE.
7923 026606 005266 000002      17$: INC    2(SP)          ;; KEEP COUNT OF CHAR
7924 026612 056616 177776      BIS    -2(SP),(SP)      ;; SET IN NEW CHAR
7925 026616 000707              BR     7$                ;; GET THE NEXT ONE
7926 026620 104401 001176      18$: TYPE $QUES          ;; TYPE ?<CR><LF>
7927 026624 000720              BR     20$              ;; SIMULATE CONTROL-U
7928
7929
7930
7931
7932
7933
7934
7935
7936
7937
7938
7939 026626 011646              $RDCHR: MOV    (SP),-(SP)  ;; PUSH DOWN THE PC
7940 026630 016666 000004 000002  MOV    4(SP),2(SP)      ;; SAVE THE PS
7941 026636 105777 152302      1$: TSTB   2$TKS         ;; WAIT FOR
7942 026642 100375              BPL    1$                ;; A CHARACTER
7943 026644 117766 152276 000004  MOVB   2$TKB,4(SP)      ;; READ THE TTY
7944 026652 042766 177600 000004  BIC    #1C<177>,4(SP)  ;; GET RID OF JUNK IF ANY
7945 026660 026627 000004 000023  CMP    4(SP),#23        ;; IS IT A CONTROL-S?
7946 026666 001013              BNE    3$                ;; BRANCH IF NO
7947 026670 105777 152250      2$: TSTB   2$TKS         ;; WAIT FOR A CHARACTER
7948 026674 100375              BPL    2$                ;; LOOP UNTIL ITS THERE
7949 026676 117746 152244  MOVB   2$TKB,-(SP)      ;; GET CHARACTER
7950 026702 042716 177600      BIC    #1C177,(SP)     ;; MAKE IT 7-BIT ASCII
7951 026706 022627 000021  CMP    (SP)+,#21        ;; IS IT A CONTROL-Q?
7952 026712 001366              BNE    2$                ;; IF NOT DISCARD IT
7953 026714 000750              BR     1$                ;; YES, RESUME
7954 026716 026627 000004 000140  3$: CMP    4(SP),#140     ;; IS IT UPPER CASE?
7955 026724 002407              BLT    4$                ;; BRANCH IF YES
7956 026726 026627 000004 000175  CMP    4(SP),#175       ;; IS IT A SPECIAL CHAR?
7957 026734 003003              BGT    4$                ;; BRANCH IF YES
7958 026736 042766 000040 000004  BIC    #40,4(SP)        ;; MAKE IT UPPER CASE
7959 026744 000002              4$: RTI                    ;; GO BACK TO USER
7960
7961
7962
7963
7964
7965

```

\*\*\*\*\*

THIS ROUTINE WILL INPUT A SINGLE CHARACTER FROM THE TTY

\*CALL: RDCHR RETURN HERE INPUT A SINGLE CHARACTER FROM THE TTY CHARACTER IS ON THE STACK WITH PARITY BIT STRIPPED OFF

\*\*\*\*\*

THIS ROUTINE WILL INPUT A STRING FROM THE TTY

\*CALL: RDLIN RETURN HERE INPUT A STRING FROM THE TTY ADDRESS OF FIRST CHARACTER WILL BE ON THE STACK TERMINATOR WILL BE A BYTE OF ALL 0'S

```

7966
7967 026746 010346
7968 026750 012703 027054
7969 026754 022703 027064
7970 026760 101405
7971 026762 104410
7972 026764 112613
7973 026766 122713 000177
7974 026772 001003
7975 026774 104401 001176
7976 027000 000763
7977 027002 111337 027052
7978 027006 104401 027052
7979 027012 122723 000015
7980 027016 001356
7981 027020 105063 177777
7982 027024 104401 001200
7983 027030 012603
7984 027032 011646
7985 027034 016666 000004 000002
7986 027042 012766 027054 000004
7987 027050 000002
7988 027052 000
7989 027053 000
7990 027054 000010
7991 027064 052536 005015 000
7992 027071 136 006507 000012
7993 027076 005015 053523 020122
7994 027104 020075 000
7995 027107 040 047040 053505
7996 027114 036440 000040

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```

$RDLIN: MOV R3, -(SP) ;: SAVE R3
1$: MOV #STTYIN, R3 ;: GET ADDRESS
2$: CMP #STTYIN+8., R3 ;: BUFFER FULL?
;: BLOS ;: BR IF YES
;: RDCHR ;: GO READ ONE CHARACTER FROM THE TTY
;: MOVB (SP)+, (R3) ;: GET CHARACTER
10$: CMPB #177, (R3) ;: IS IT A RUBOUT
;: BNE 3$ ;: SKIP IF NOT
4$: TYPE $QUES ;: TYPE A '?'
;: BR 1$ ;: CLEAR THE BUFFER AND LOOP
3$: MOVB (R3), 9$ ;: ECHO THE CHARACTER
;: TYPE 9$
;: CMPB #15, (R3)+ ;: CHECK FOR RETURN
;: BNE 2$ ;: LOOP IF NOT RETURN
;: CLRB -1(R3) ;: CLEAR RETURN (THE 15)
;: TYPE $LF ;: TYPE A LINE FEED
;: MOV (SP)+, R3 ;: RESTORE R3
;: MOV (SP), -(SP) ;: ADJUST THE STACK AND PUT ADDRESS OF THE
;: MOV 4(SP), 2(SP) ;: FIRST ASCII CHARACTER ON IT
;: MOV #STTYIN, 4(SP)
;: RTI ;: RETURN
9$: .BYTE 0 ;: STORAGE FOR ASCII CHAR. TO TYPE
;: .BYTE 0 ;: TERMINATOR
$TTYIN: .BLKB 8. ;: RESERVE 8 BYTES FOR TTY INPUT
$CNTLU: .ASCIZ /↑U/<15><12> ;: CONTROL "U"
$CNTLG: .ASCIZ /↑G/<15><12> ;: CONTROL "G"
$MSWR: .ASCIZ <15><12>/SWR = /
$MNEW: .ASCIZ / NEW = /

```

.SBTTL TYPE ROUTINE

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7999
8000 ;: *****
8001 ;: *ROUTINE TO TYPE ASCIZ MESSAGE. MESSAGE MUST TERMINATE WITH A 0 BYTE.
8002 ;: *THE ROUTINE WILL INSERT A NUMBER OF NULL CHARACTERS AFTER A LINE FEED.
8003 ;: *NOTE1: $NULL CONTAINS THE CHARACTER TO BE USED AS THE FILLER CHARACTER.
8004 ;: *NOTE2: $FILLS CONTAINS THE NUMBER OF FILLER CHARACTERS REQUIRED.
8005 ;: *NOTE3: $FILLC CONTAINS THE CHARACTER TO FILL AFTER.
8006 ;: *
8007 ;: *CALL:
8008 ;: *1) USING A TRAP INSTRUCTION ;: MESADR IS FIRST ADDRESS OF AN ASCIZ STRING
8009 ;: * TYPE ,MESADR
8010 ;: *OR
8011 ;: * TYPE
8012 ;: * MESADR
8013 ;: *
8014 027120 105737 001157 $TYPE: TSTB $TFPLG ;: IS THERE A TERMINAL?
8015 027124 100002 BPL 1$ ;: BR IF YES
8016 027126 000000 HALT ;: HALT HERE IF NO TERMINAL
8017 027130 000430 BR 3$ ;: LEAVE
8018 027132 010046 1$: MOV R0, -(SP) ;: SAVE R0
8019 027134 017600 000002 MOV @2(SP), R0 ;: GET ADDRESS OF ASCIZ STRING

```



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8020 027140 122737 000001 001222      CMPB  #APTENV,$ENVV      ;: RUNNING IN APT MODE
8021 027146 001011                    BNE   62$               ;: NO,GO CHECK FOR APT CONSOLE
8022 027150 132737 000100 001223      BITB  #APTSPOOL,$ENVM   ;: SPOOL MESSAGE TO APT
8023 027156 001405                    BEQ   62$               ;: NO,GO CHECK FOR CONSOLE
8024 027160 010037 027170              MOV   RO,61$           ;: SETUP MESSAGE ADDRESS FOR APT
8025 027164 004737 027410              JSR   PC,$ATY3         ;: SPOOL MESSAGE TO APT
8026 027170 000000                    .WORD 0                ;: MESSAGE ADDRESS
8027 027172 132737 000040 001223      61$: BITB  #APTCSUP,$ENVM ;: APT CONSOLE SUPPRESSED
8028 027200 001003                    BNE   60$               ;: YES,SKIP TYPE OUT
8029 027202 112046                    2$:  MOVB (RO)+,-(SP)   ;: PUSH CHARACTER TO BE TYPED ONTO STACK
8030 027204 001005                    BNE   4$                ;: BR IF IT ISN'T THE TERMINATOR
8031 027206 005726                    TST  (SP)+             ;: IF TERMINATOR POP IT OFF THE STACK
8032 027210 012600                    60$: MOV   (SP)+,RO    ;: RESTORE RO
8033 027212 062716 000002              3$:  ADD   #2,(SP)      ;: ADJUST RETURN PC
8034 027216 000002                    RTI                      ;: RETURN
8035 027220 122716 000011              4$:  CMPB  #HT,(SP)     ;: BRANCH IF <HT>
8036 027224 001430                    BEQ   8$                ;:
8037 027226 122716 000200              CMPB  #CRLF,(SP)      ;: ; BRANCH IF NOT <CRLF>
8038 027232 001006                    BNE   5$                ;:
8039 027234 005726                    TST  (SP)+             ;: POP <CR><LF> EQUIV
8040 027236 104401                    TYPE  $CRLF           ;: TYPE A CR AND LF
8041 027240 001177                    $CRLF
8042 027242 105037 027376              CLRB  $CHARCNT        ;: CLEAR CHARACTER COUNT
8043 027246 000755                    BR   2$                ;: GET NEXT CHARACTER
8044 027250 004737 027332              5$:  JSR   PC,$TYPEC    ;: GO TYPE THIS CHARACTER
8045 027254 123726 001156              6$:  CMPB  $FILLC,(SP)+ ;: IS IT TIME FOR FILLER CHARS.?
8046 027260 001350                    BNE   2$                ;: IF NO GO GET NEXT CHAR.
8047 027262 013746 001154              MOV   $NULL,-(SP)     ;: GET # OF FILLER CHARS. NEEDED
8048                                AND   THE NULL CHAR.
8049 027266 105366 000001              7$:  DECB  1(SP)        ;: DOES A NULL NEED TO BE TYPED?
8050 027272 002770                    BLT   6$                ;: BR IF NO--GO POP THE NULL OFF OF STACK
8051 027274 004737 027332              JSR   PC,$TYPEC    ;: GO TYPE A NULL
8052 027300 105337 027376              DECB  $CHARCNT       ;: DO NOT COUNT AS A COUNT
8053 027304 000770                    BR   7$                ;: LOOP
8054
8055                                ; HORIZONTAL TAB PROCESSOR
8056
8057 027306 112716 000040              8$:  MOVB  #' (SP)      ;: REPLACE TAB WITH SPACE
8058 027312 004737 027332              9$:  JSR   PC,$TYPEC    ;: TYPE A SPACE
8059 027316 132737 000007 027376      BITB  #',$CHARCNT     ;: BRANCH IF NOT AT
8060 027324 001372                    BNE   9$                ;: TAB STOP
8061 027326 005726                    TST  (SP)+             ;: POP SPACE OFF STACK
8062 027330 000724                    BR   2$                ;: GET NEXT CHARACTER
8063 027332 105777 151612              $TYPEC: TSTB  @STPS    ;: WAIT UNTIL PRINTER IS READY
8064 027336 100375                    BPL  $TYPEC           ;:
8065 027340 116677 000002 151604      MOVB  2(SP),@STPB     ;: LOAD CHAR TO BE TYPED INTO DATA REG.
8066 027346 122766 000015 000002      CMPB  #CR,2(SP)       ;: IS CHARACTER A CARRIAGE RETURN?
8067 027354 001003                    BNE   1$                ;: BRANCH IF NO
8068 027356 105037 027376              CLRB  $CHARCNT        ;: YES--CLEAR CHARACTER COUNT
8069 027362 000406                    BR   $TYPEX           ;: EXIT
8070 027364 122766 000012 000002      1$:  CMPB  #LF,2(SP)    ;: IS CHARACTER A LINE FEED?
8071 027372 001402                    BEQ   $TYPEX           ;: BRANCH IF YES
8072 027374 105227                    INCB  (PC)+            ;: COUNT THE CHARACTER
8073 027376 000000                    $CHARCNT: .WORD 0     ;: CHARACTER COUNT STORAGE

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8074 027400 000207 $TYPEX: RTS PC
8075
8076 .SBTTL APT COMMUNICATIONS ROUTINE
8077
8078 ;*****
8079 027402 112737 000001 027646 $ATY1: MOVB #1,$FFLG ;; TO REPORT FATAL ERROR
8080 027410 112737 000001 027644 $ATY3: MOVB #1,$MFLG ;; TO TYPE A MESSAGE
8081 027416 000403 BR $ATYC
8082 027420 112737 000001 027646 $ATY4: MOVB #1,$FFLG ;; TO ONLY REPORT FATAL ERROR
8083 027426 $ATYC:
8084 027426 010046 MOV R0,-(SP) ;; PUSH R0 ON STACK
8085 027430 010146 MOV R1,-(SP) ;; PUSH R1 ON STACK
8086 027432 105737 027644 TSTB $MFLG ;; SHOULD TYPE A MESSAGE?
8087 027436 001450 BEQ 5$ ;; IF NOT: BR
8088 027440 122737 000001 001222 CMPB #APTENV,$ENV ;; OPERATING UNDER APT?
8089 027446 001031 BNE 3$ ;; IF NOT: BR
8090 027450 132737 000100 001223 BITB #APTPOOL,$ENVM ;; SHOULD SPOOL MESSAGES?
8091 027456 001425 BEQ 3$ ;; IF NOT: BR
8092 027460 017600 000004 MOV #4(SP),R0 ;; GET MESSAGE ADDR.
8093 027464 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDR.
8094 027472 005737 001202 1$: TST $MSGTYPE ;; SEE IF DONE W/ LAST XMISSION?
8095 027476 001375 BNE 1$ ;; IF NOT: WAIT
8096 027500 010037 001216 MOV R0,$MSGAD ;; PUT ADDR IN MAILBOX
8097 027504 105720 2$: TSTB (R0)+ ;; FIND END OF MESSAGE
8098 027506 001376 BNE 2$
8099 027510 163700 001216 SUB $MSGAD,R0 ;; SUB START OF MESSAGE
8100 027514 006200 ASR R0 ;; GET MESSAGE LNTH IN WORDS
8101 027516 010037 001220 MOV R0,$MSG LGT ;; PUT LENGTH IN MAILBOX
8102 027522 012737 000004 001202 MOV #4,$MSGTYPE ;; TELL APT TO TAKE MSG.
8103 027530 000413 BR 5$
8104 027532 017637 000004 027556 3$: MOV #4(SP),4$ ;; PUT MSG ADDR IN JSR LINKAGE
8105 027540 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDRESS
8106 027546 013746 177776 MOV 177776,-(SP) ;; PUSH 177776 ON STACK
8107 027552 004737 027120 JSR PC,$TYPE ;; CALL TYPE MACRO
8108 027556 000000 4$: .WORD 0
8109 027560 5$:
8110 027560 105737 027646 10$: TSTB $FFLG ;; SHOULD REPORT FATAL ERROR?
8111 027564 001416 BEQ 12$ ;; IF NOT: BR
8112 027566 005737 001222 TST $ENV ;; RUNNING UNDER APT?
8113 027572 001413 BEQ 12$ ;; IF NOT: BR
8114 027574 005737 001202 11$: TST $MSGTYPE ;; FINISHED LAST MESSAGE?
8115 027600 001375 BNE 11$ ;; IF NOT: WAIT
8116 027602 017637 000004 001204 MOV #4(SP),$FATAL ;; GET ERROR #
8117 027610 062766 000002 000004 ADD #2,4(SP) ;; BUMP RETURN ADDR.
8118 027616 005237 001202 INC $MSGTYPE ;; TELL APT TO TAKE ERROR
8119 027622 105037 027646 12$: CLRB $FFLG ;; CLEAR FATAL FLAG
8120 027626 105037 027645 CLRB $LFLG ;; CLEAR LOG FLAG
8121 027632 105037 027644 CLRB $MFLG ;; CLEAR MESSAGE FLAG
8122 027636 012601 MOV (SP)+,R1 ;; POP STACK INTO R1
8123 027640 012600 MOV (SP)+,R0 ;; POP STACK INTO R0
8124 027642 000207 RTS PC ;; RETURN
8125 027644 000 $MFLG: .BYTE 0 ;; MESSG. FLAG
8126 027645 000 $LFLG: .BYTE 0 ;; LOG FLAG
8127 027646 000 $FFLG: .BYTE 0 ;; FATAL FLAG

```

8128 027650  
8129 000200  
8130 000001  
8131 000100  
8132 000040  
8133  
8134  
8135  
8136  
8137 027650 012737 030010 000024  
8138 027656 012737 000340 000026  
8139 027664 010046  
8140 027666 010146  
8141 027670 010246  
8142 027672 010346  
8143 027674 010446  
8144 027676 010546  
8145 027700 017746 151234  
8146 027704 010637 030014  
8147 027710 012737 027722 000024  
8148 027716 000000  
8149 027720 000776  
8150  
8151  
8152  
8153 027722 012737 030010 000024  
8154 027730 013706 030014  
8155 027734 005037 030014  
8156 027740 005237 030014  
8157 027744 001375  
8158 027746 012677 151166  
8159 027752 012605  
8160 027754 012604  
8161 027756 012603  
8162 027760 012602  
8163 027762 012601  
8164 027764 012600  
8165 027766 012737 027650 000024  
8166 027774 012737 000340 000026  
8167 030002 104401  
8168 030004 030016  
8169 030006 000002  
8170 030010 000000  
8171 030012 000776  
8172 030014 000000  
8173 030016 005015 047520 042527  
8174 030024 000122  
8175  
8176  
8177  
8178  
8179  
8180  
8181

```

.EVEN
APTSIZE=200
APTENV=001
APTSPool=100
APTC SUP=040
.SBTTL POWER DOWN AND UP ROUTINES

*****
: POWER DOWN ROUTINE
$PWRDN: MOV    $SILLUP, @#PWRVEC    ;; SET FOR FAST UP
        MOV    #340, @#PWRVEC+2  ;; PRIO:7
        MOV    RO, -(SP)          ;; PUSH RO ON STACK
        MOV    R1, -(SP)          ;; PUSH R1 ON STACK
        MOV    R2, -(SP)          ;; PUSH R2 ON STACK
        MOV    R3, -(SP)          ;; PUSH R3 ON STACK
        MOV    R4, -(SP)          ;; PUSH R4 ON STACK
        MOV    R5, -(SP)          ;; PUSH R5 ON STACK
        MOV    @SWR, -(SP)        ;; PUSH @SWR ON STACK
        MOV    SP, $SAVR6        ;; SAVE SP
        MOV    $PWRUP, @#PWRVEC  ;; SET UP VECTOR
        HALT
        BR     .-2                ;; HANG UP

*****
: POWER UP ROUTINE
$PWRUP: MOV    $SILLUP, @#PWRVEC  ;; SET FOR FAST DOWN
        MOV    $SAVR6, SP        ;; GET SP
        CLR    $SAVR6           ;; WAIT LOOP FOR THE TTY
1$:      INC    $SAVR6           ;; WAIT FOR THE INC
        BNE    1$              ;; OF WORD
        MOV    (SP)+, @SWR      ;; POP STACK INTO @SWR
        MOV    (SP)+, R5       ;; POP STACK INTO R5
        MOV    (SP)+, R4       ;; POP STACK INTO R4
        MOV    (SP)+, R3       ;; POP STACK INTO R3
        MOV    (SP)+, R2       ;; POP STACK INTO R2
        MOV    (SP)+, R1       ;; POP STACK INTO R1
        MOV    (SP)+, R0       ;; POP STACK INTO R0
        MOV    $PWRDN, @#PWRVEC ;; SET UP THE POWER DOWN VECTOR
        MOV    #340, @#PWRVEC+2 ;; PRIO:7
        TYPE   $POWER          ;; REPORT THE POWER FAILURE
        $PWRMG: .WORD $POWER  ;; POWER FAIL MESSAGE POINTER
        RTI
$SILLUP: HALT                  ;; THE POWER UP SEQUENCE WAS STARTED
        BR     .-2                ;; BEFORE THE POWER DOWN WAS COMPLETE
$SAVR6: 0                      ;; PUT THE SP HERE
$POWER:  .ASCIZ <15><12>"POWER"

.EVEN
.SBTTL TRAP DECODER

*****
: *THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE "TRAP" INSTRUCTION
: *AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
: *OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL

```

```

8182
8183
8184 030026 010046
8185 030030 016600 000002
8186 030034 005740
8187 030036 111000
8188 030040 006300
8189 030042 016000 030062
8190 030046 000200
8191
8192
8193
8194
8195 030050 011646
8196 030052 016666 000004 000002
8197 030060 000002
8198
8199
8200
8201
8202
8203
8204
8205
8206 030062 030050
8207 030064 027120
8208 030066 025012
8209 030070 024766
8210 030072 025026
8211 030074 025536
8212
8213 030076 026414
8214
8215 030100 026344
8216 030102 026626
8217 030104 026746
8218 030106 026242
8219 030110 024612
8220 030112 005015 046103 041517
8221 030120 040513 051440 020122
8222 030126 052506 041516 044524
8223 030134 047117 042440 051122
8224 030142 051117 000
8225 030145 015 041412 047514
8226 030152 045503 020101 051123
8227 030160 042040 052101 020101
8228 030166 051105 047522 000122
8229 030174 005015 046103 041517
8230 030202 040513 041040 020122
8231 030210 040504 040524 042440
8232 030216 051122 051117 000
8233 030223 015 041412 047514
8234 030230 045503 020101 051103
8235 030236 042040 052101 020101

```

;\*GO TO THAT ROUTINE.

```

$TRAP:  MOV    RO,-(SP)      ;;SAVE RO
        MOV    2(SP),RO     ;;GET TRAP ADDRESS
        TST   -(RO)        ;;BACKUP BY 2
        MOVB  (RO),RO      ;;GET RIGHT BYTE OF TRAP
        ASL   RO           ;;POSITION FOR INDEXING
        MOV   $TRPAD(RO),RO ;;INDEX TO TABLE
        RTS   RO           ;;GO TO ROUTINE

```

;;THIS IS USE TO HANDLE THE "GETPRI" MACRO

```

$TRAP2: MOV   (SP),-(SP)    ;;MOVE THE PC DOWN
        MOV   4(SP),2(SP)  ;;MOVE THE PSW DOWN
        RTI                      ;;RESTORE THE PSW

```

.SBTTL TRAP TABLE

;\*THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED  
;\*BY THE "TRAP" INSTRUCTION.

```

; ROUTINE
;-----
$TRPAD: .WORD  $TRAP2      TRAP+1(104401)  TTY TYPEOUT ROUTINE
        $TYPE   ;;CALL=TYPE   TRAP+2(104402)  TYPE OCTAL NUMBER (WITH LEADING ZEROS)
        $TYPOC  ;;CALL=TYPOC  TRAP+3(104403)  TYPE OCTAL NUMBER (NO LEADING ZEROS)
        $TYPOS  ;;CALL=TYPOS  TRAP+4(104404)  TYPE OCTAL NUMBER (AS PER LAST CALL)
        $TYPON  ;;CALL=TYPON  TRAP+5(104405)  TYPE DECIMAL NUMBER (WITH SIGN)
        $TYPDS  ;;CALL=TYPDS
        $GTSWR  ;;CALL=GTSWR  TRAP+6(104406)  GET SOFT-SWR SETTING
        $CKSWR  ;;CALL=CKSWR  TRAP+7(104407)  TEST FOR CHANGE IN SOFT-SWR
        $RDCHR  ;;CALL=RDCHR  TRAP+10(104410) TTY TYPEIN CHARACTER ROUTINE
        $RDLIN  ;;CALL=RDLIN  TRAP+11(104411) TTY TYPEIN STRING ROUTINE
        $RDOCT  ;;CALL=RDOCT  TRAP+12(104412) READ AN OCTAL NUMBER FROM TTY
        IOTRD  ;;CALL=IOTT   TRAP+13(104413)
        .ASCIZ <15><12>/CLOCKA SR FUNCTION ERROR/
EM1:
EM2: .ASCIZ <15><12>/CLOCKA SR DATA ERROR/
EM3: .ASCIZ <15><12>/CLOCKA BR DATA ERROR/
EM4: .ASCIZ <15><12>/CLOCKA CR DATA ERROR/

```

8236	030244	051105	047522	000122		
8237	030252	005015	046103	041517	EM5:	.ASCIZ <15><12>/CLOCKB SR DATA ERROR/
8238	030260	041113	051440	020122		
8239	030266	040504	040524	042440		
8240	030274	051122	051117	000		
8241	030301	015	041412	047514	EM6:	.ASCIZ <15><12>/CLOCKB BR DATA ERROR/
8242	030306	045503	020102	051102		
8243	030314	042040	052101	020101		
8244	030322	051105	047522	000122		
8245	030330	005015	046103	041517	EM7:	.ASCIZ <15><12>/CLOCKB CR DATA ERROR/
8246	030336	041113	041440	020122		
8247	030344	040504	040524	042440		
8248	030352	051122	051117	000		
8249	030357	015	042012	040525	EM10:	.ASCIZ <15><12>/DUAL ADDRESS ERROR/
8250	030364	020114	042101	051104		
8251	030372	051505	020123	051105		
8252	030400	047522	000122			
8253	030404	005015	046103	041517	EM11:	.ASCIZ <15><12>#CLOCK A COUNT ERROR #
8254	030412	020113	020101	047503		
8255	030420	047125	020124	051105		
8256	030426	047522	020122	000		
8257	030433	015	041412	047514	EM12:	.ASCIZ <15><12>#CLOCK A COUNT FUNCTION ERROR #
8258	030440	045503	040440	041440		
8259	030446	052517	052116	043040		
8260	030454	047125	052103	047511		
8261	030462	020116	051105	047522		
8262	030470	020122	000			
8263	030473	015	041412	047514	EM14:	.ASCIZ <15><12>#CLOCK B COUNT FUNCTION ERROR #
8264	030500	045503	041040	041440		
8265	030506	052517	052116	043040		
8266	030514	047125	052103	047511		
8267	030522	020116	051105	047522		
8268	030530	020122	000			
8269	030533	015	041412	047514	EM15:	.ASCIZ <15><12>#CLOCK B COUNT ERROR #
8270	030540	045503	041040	041440		
8271	030546	052517	052116	042440		
8272	030554	051122	051117	000040		
8273	030562	005015	046103	041517	EM16:	.ASCIZ <15><12>#CLOCK A INTERRUPT ERROR #
8274	030570	020113	020101	047111		
8275	030576	042524	051122	050125		
8276	030604	020124	051105	047522		
8277	030612	020122	000			
8278	030615	015	041412	047514	EM17:	.ASCIZ <15><12>#CLOCK B INTERRUPT ERROR #
8279	030622	045503	041040	044440		
8280	030630	052116	051105	052522		
8281	030636	052120	042440	051122		
8282	030644	051117	000040			
8283	030650	005015	046103	041517	EM20:	.ASCIZ <15><12>#CLOCK A REPEATABILITY ERROR #
8284	030656	020113	020101	042522		
8285	030664	042520	052101	041101		
8286	030672	046111	052111	020131		
8287	030700	051105	047522	020122		
8288	030706	000				
8289	030707	015	041412	047514	EM23:	.ASCIZ <15><12>#CLOCK B REPEATABILITY ERROR #

8290	030714	045503	041040	051040					
8291	030722	050105	040505	040524					
8292	030730	044502	044514	054524					
8293	030736	042440	051122	051117					
8294	030744	000040							
8295	030746	005015	046103	041517	EM26:	.ASCIZ	<15><12>	#CLOCK ADDRESSING ERROR#	
8296	030754	020113	042101	051104					
8297	030762	051505	044523	043516					
8298	030770	042440	051122	051117					
8299	030776	000							
8300									
8301	030777	015	042412	051122	DH1:	.ASCIZ	<15><12>	#ERRPC	ASR WAS S/B#
8302	031004	041520	020040	040440					
8303	031012	051123	020040	020040					
8304	031020	053440	051501	020040					
8305	031026	020040	051440	041057					
8306	031034	000							
8307	031035	015	042412	051122	DH3:	.ASCIZ	<15><12>	#ERRPC	ABR WAS S/B#
8308	031042	041520	020040	040440					
8309	031050	051102	020040	020040					
8310	031056	053440	051501	020040					
8311	031064	020040	051440	041057					
8312	031072	000							
8313	031073	015	042412	051122	DH4:	.ASCIZ	<15><12>	#ERRPC	ACR WAS S/B#
8314	031100	041520	020040	040440					
8315	031106	051103	020040	020040					
8316	031114	053440	051501	020040					
8317	031122	020040	051440	041057					
8318	031130	000							
8319	031131	015	042412	051122	DH5:	.ASCIZ	<15><12>	#ERRPC	BSR WAS S/B#
8320	031136	041520	020040	041040					
8321	031144	051123	020040	020040					
8322	031152	053440	051501	020040					
8323	031160	020040	051440	041057					
8324	031166	000							
8325	031167	015	042412	051122	DH6:	.ASCIZ	<15><12>	#ERRPC	BBR WAS S/B#
8326	031174	041520	020040	041040					
8327	031202	051102	020040	020040					
8328	031210	053440	051501	020040					
8329	031216	020040	051440	041057					
8330	031224	000							
8331	031225	015	042412	051122	DH7:	.ASCIZ	<15><12>	#ERRPC	BCR WAS S/B#
8332	031232	041520	020040	041040					
8333	031240	051103	020040	020040					
8334	031246	053440	051501	020040					
8335	031254	020040	051440	041057					
8336	031262	000							
8337	031263	015	042412	051122	DH10:	.ASCII	<15><12>	/ERROR	GOOD BAD GOOD DATA READ FROM/
8338	031270	051117	020040	043440					
8339	031276	047517	020104	020040					
8340	031304	041040	042101	020040					
8341	031312	020040	043440	047517					
8342	031320	020104	020040	042040					
8343	031326	052101	020101	042522					

PC	ADDR	ADDR	DATA	DUAL ADDRESS/
8344	031334	042101	043040	047522
8345	031342	115		
8346	031343	015	020012	050040
8347	031350	020103	020040	040440
8348	031356	042104	020122	020040
8349	031364	040440	042104	020122
8350	031372	020040	042040	052101
8351	031400	020101	020040	042040
8352	031406	040525	020114	042101
8353	031414	051104	051505	000123
8354	031422	005015	051105	050122
8355	031430	020103	020040	051501
8356	031436	020122	000	
8357	031441	015	042412	051122
8358	031446	041520	020040	041040
8359	031454	051123	000	
8360	031457	015	042412	051122
8361	031464	041520	020040	040440
8362	031472	051123	020040	020040
8363	031500	031040	042116	047103
8364	031506	020124	030440	052123
8365	031514	047103	020124	000
8366	031521	015	042412	051122
8367	031526	041520	020040	041040
8368	031534	051123	020040	020040
8369	031542	031040	042116	047103
8370	031550	020124	030440	052123
8371	031556	047103	020124	000
8372	031563	015	042412	051122
8373	031570	041520	020040	041440
8374	031576	047514	045503	040440
8375	031604	042104	027122	000
8376				
8377		031612		
8378				
8379	031612	001116	001326	001126
8380	031620	001124	000000	
8381	031624	001116	001330	001126
8382	031632	001124	000000	
8383	031636	001116	001332	001126
8384	031644	001124	000000	
8385	031650	001116	001334	001126
8386	031656	001124	000000	
8387	031662	001116	001336	001126
8388	031670	001124	000000	
8389	031674	001116	001340	001126
8390	031702	001124	000000	
8391	031706	001116	001120	001122
8392	031714	001124	001126	000000
8393	031722	001116	001326	000000
8394	031730	001116	001334	000000
8395	031736	001116	001332	001124
8396	031744	001164	000000	
8397	031750	001116	001332	001126

.ASCIZ <15><12>/ PC ADDR ADDR DATA DUAL ADDRESS/  
DH12: .ASCIZ <15><12>#ERRPC ASR #  
DH14: .ASCIZ <15><12>#ERRPC BSR#  
DH20: .ASCIZ <15><12>#ERRPC ASR 2NDCNT 1STCNT #  
DH23: .ASCIZ <15><12>#ERRPC BSR 2NDCNT 1STCNT #  
DH26: .ASCIZ <15><12>#ERRPC CLOCK ADDR. #  
.EVEN  
DT1: .WORD \$ERRPC, ASR, \$BDDAT, \$GDDAT, 0  
DT3: .WORD \$ERRPC, ABR, \$BDDAT, \$GDDAT, 0  
DT4: .WORD \$ERRPC, ACR, \$BDDAT, \$GDDAT, 0  
DT5: .WORD \$ERRPC, BSR, \$BDDAT, \$GDDAT, 0  
DT6: .WORD \$ERRPC, BBR, \$BDDAT, \$GDDAT, 0  
DT7: .WORD \$ERRPC, BCR, \$BDDAT, \$GDDAT, 0  
DT10: .WORD \$ERRPC, \$GDADR, \$BDADR, \$GDDAT, \$BDDAT, 0  
DT12: .WORD \$ERRPC, ASR, 0  
DT14: .WORD \$ERRPC, BSR, 0  
DT21: .WORD \$ERRPC, ACR, \$GDDAT, \$TMP0, 0  
DT22: .WORD \$ERRPC, ACR, \$BDDAT, \$TMP0, 0

```

8398 031756 001164 000000
8399 031762 001116 001340 001124 DT24: .WORD $ERRPC,BCR,$GDDAT,$TMPO,0
8400 031770 001164 000000
8401 031774 001116 001340 001126 DT25: .WORD $ERRPC,BCR,$BDDAT,$TMPO,0
8402 032002 001164 000000
8403 032006 001116 001164 000000 DT26: .WORD $ERRPC,$TMPO,0
8404
8405 032014 000000 000000 DFO: .WORD 0,0
8406
8407
8408
8409
8410
8411
8412
8413
8414
8415
8416
8417
8418
8419
8420
8421
8422
8423
8424
8425 032020
8426 032020 013746 000004 $LPAI: MOV 4,-(SP)
8427
8428 032024 000413 BR 31$
8429
8430
8431
8432
8433
8434
8435
8436
8437
8438
8439
8440
8441 032026 012737 032052 000004 MOV #30$,4
8442 032034 005237 170000 INC 170000
8443 032040 104401 032046 TYPE 65$
8444 032044 000401 BR 64$
8445
8446 032050 64$: .ASCIZ <7>##
8447 032050 000401 BR 31$
8448 032052 022626 30$: CMP (SP)+,(SP)+
8449 032054 012637 000004 31$: MOV (SP)+,4
8450 032060 005037 032676 CLR $AERR
8451 032064 004537 032700 JSR R5,$LOAD

```

```

;*
;*THIS SUB CODE IS USED TO INITIALIZE THE LPA-11
;*FIRST WE WILL LOAD MICROCODE INTO KMC-11
;*NEXT WE WILL INIT BOTH UPROCESSORS
;*THEN WE WILL LOAD DEVICE TABLE IN SLAVE UP.
;*THE ORDER OF LOAD IS DETERMINED BY THE USER.

```

```

;*
;* CALL= JSR R5,$LPAI ;ADDR. OF DEVICE ADDRESS.
;* .WORD 0
;* ROUTINES REQUIRED: .LOADLP
;* PROGRAMS REQUIRED: DRLPX2

```

```

;*
;* ;RETURNS WITH $AERR=1 IF SLAVE
;* ;MICRO SAYS AN ADDR. DOES NOT EXSIST. IN THE LIST.

```

```

;FIELD DOES NOT HAVE A BUS SWITCH TO
;WORRY ABOUT,SO WE WILL UNCONDITIONALLY
;BRANCH AROUND THE NEXT CODE THAT
;WORKS BASED ON A BUS SWITCH.
;CODE LEFT IN HERE FOR IN HOUSE
;PERSONAL WHO MAY PATCH THIS BRANCH
;INSTRUCTION TO A <NOP> OCTAL <240>
;IN ORDER TO RUN PROGRAM WITH A SWITCH.

```

```

;NOTE THIS "SWITCH" IS A PIECE OF INHOUSE
;TEST EQUIPMENT ONLY IT CONNECTS
;THE UNIBUS TO THE I/O BUS FOR
;CERTAIN TESTING.

```

```

;;TYPE ASCIZ STRING
;;GET OVER THE ASCIZ

```

```

;ALL THIS JUNK MUST BE REMOVED!!

```

```

;LOAD MICRO-CODE.

```



8452	032070	000000G			.WORD	DRLPX2		;FILE "DRLPX2.OBJ"
8453								
8454	032072	052777	040000	147540	BIS	#BIT14, @KMADO		;ISSUE KMC+DMC INIT.
8455								
8456	032100						1\$:	
8457								; "HANGS" HERE THEN KMC-11 ERROR.
8458	032100	010146			MOV	R1, -(SP)		
8459	032102	005001			CLR	R1		
8460	032104	005201			INC	R1	2\$:	;STALL FOR DMC-UP
8461	032106	001376			BNE	2\$		
8462	032110	012777	104000	147522	MOV	#BIT15!BIT11, @KMADO		;SET RUN, AND ENABLE ARBITRATION.
8463	032116	105201			INC	R1	25\$:	
8464	032120	001376			BNE	25\$		
8465								
8466	032122	032777	000040	147510	BIT	#BITS, @KMADO		;SLAVE READY? (READING IPBM SR)
8467	032130	001401			BEQ	3\$		;FATAL LPA-11 ERROR SLAVE NOT READY.
8468								
8469	032132	104000			ERROR			
8470								
8471	032134	012777	000004	147502	MOV	#4, @KMAD2	3\$:	;READ FAST PATH
8472	032142						4\$:	
8473	032142	004537	033610		JSR	R5, \$TOUT		; -TOUT-CHECK FOR TIMEOUT
8474								
8475	032146	104000			ERROR			; /TIME-OUT ERROR
8476								; /WE FAILED TO COMPLETE
8477								; /CURRENT OPERATION.
8478								; /CONTINUES IN THIS LOOP
8479								; /WOULD MAKE US "HANG" HERE
8480								
8481	032150	000774			BR	4\$		
8482								
8483								; /RETURNS HERE-FROM-TIMED OUT.
8484	032152	122777	000377	147464	CMPB	#377, @KMAD2		;WAIT TILL KMC DONE COMMAND.
8485	032160	001370			BNE	4\$		
8486	032162	122777	000377	147460	CMPB	#377, @KMAD4		; IF FAST PATH=377 THEN ERROR.
8487	032170	001001			BNE	35\$		
8488	032172	104000			ERROR			; IPBM ERROR (SLAVE SIDE)
8489								; YOU MUST RUN IPBM DIAGNOSTIC.
8490								
8491	032174	122777	000004	147446	CMPB	#4, @KMAD4	35\$:	; IS THIS THE CORRECT VERSION OF MICRO-CODE?
8492	032202	001543			BEQ	5\$		; YES-CONTINUE.
8493	032204	005227	177777		INC	#-1		
8494	032210	001140			BNE	5\$		
8495	032212	005227	177777		INC	#-1		
8496	032216	001135			BNE	5\$		
8497	032220	104401	032226		TYPE	,67\$		; ;TYPE ASCIZ STRING
8498	032224	000440			BR	66\$		; ;GET OVER THE ASCIZ
8499								; ;THIS PROGRAM WAS DESIGNED TO RUN WITH VERSION 4"
8500	032326						66\$:	
8501	032326	104401	032334		TYPE	,69\$		; ;TYPE ASCIZ STRING
8502	032332	000430			BR	68\$		; ;GET OVER THE ASCIZ
8503							69\$:	
8504	032414				.ASCIZ	<200>"MICRO-CODE. ANOTHER VERSION CODE WAS DETECTED."		
8505	032414	104401	032422		TYPE	,71\$		; ;TYPE ASCIZ STRING

```

8506 032420 000434          BR      70$          ;;GET OVER THE ASCIZ
8507          ;;71$: .ASCIZ <200>"THIS MAY OR MAYNOT CAUSE FALSE ERROR TO BE REPORTED."<200><200>
8508 032512          70$:
8509
8510 032512 112737 177777 032644 5$:  MOVB  #0-1,11$      ;DAC CODE FOR SLAVE.
8511 032520 012501          MOV   (5)+,R1      ;GET NEXT DEVICE ADDR.
8512 032522 021127 000000 6$:  CMP   (R1),#0      ;TERM REACHED?
8513 032526 001444          BEQ   10$
8514 032530 105237 032644          INCB  11$
8515 032534 1:3777 032644 147106  MOVB  11$,QKMA4    ;FIFO DATA
8516 032542 004737 032646          JSR   PC,20$      ;ISSUE SEND
8517 032546 112177 147076          MOVB  (R1)+,QKMA4 ;SEND LOW BYTE OF DEVICE ADDR TO SLAVE.
8518 032552 004737 032646          JSR   PC,20$      ;ISSUE SEND
8519 032556 112177 147066          MOVB  (R1)+,QKMA4 ;SEND HIGH BYTE OF DEVICE ADDR. TO SLAVE.
8520 032562 004737 032646          JSR   PC,20$
8521
8522 032566 032777 000002 147044 7$:  BIT   #BIT1,QKMA0  ;WAIT FOR FIFO DATA
8523 032574 001374          BNE   7$          ;=1 NO DATA. =0 DATA.
8524 032576 112777 000002 147040          MOVB  #2,QKMA2    ;READ FIFO.
8525
8526 032604          8$:
8527 032604 004537 033610          JSR   R5, $TOUT  ;--TOUT-CHECK FOR TIMEOUT
8528
8529 032610 104000          ERROR
8530
8531          ;/TIME-OUT ERROR
8532          ;/WE FAILED TO COMPLETE
8533          ;/CURRENT OPERATION.
8534          ;/CONTINUES IN THIS LOOP
8535          ;/WOULD MAKE US "HANG" HERE
8535 032612 000774          BR      8$
8536
8537          ;/RETURNS HERE-FROM-TIMED OUT.
8538 032614 122777 000377 147022  CMPB  #377,QKMA2  ;WAIT FOR READ.
8539 032622 001370          BNE   8$
8540 032624 105777 147020          TSTB  QKMA4
8541 032630 001734          BEQ   6$
8542
8543 032632 005237 032676          INC   $AERR
8544          ;WAS A ZERO RETURNED?
8545 032636 005041          CLR   -(1)
8546 032640 012601          MOV   (SP)+,R1   ;YES GET NEXT ADDR.
8547 032642 000205          RTS   R5         ;SLAVE WILL RETURN CODE 0 IF
8548          ;DEV PRESENT. ELSE
8549 032644 000000          10$:          ;EXIT $AERR=1 IF SLAVE GIVES ERROR.
8550          ;GET RID OF REFERENCE TO BAD ADDR.
8551          ;RETURN ALL ADDR. CHECKED.
8552 032646 112777 000003 146770 20$:  MOVB  #3,QKMA2    ;HOLDS DAC CODE PLUS OFFSET
8553 032654          21$:          ;TO SLAVES ADDR. TABLE.
8554 032654 004537 033610          JSR   R5, $TOUT  ;ISSUE FIFO WRITE
8555          ;--TOUT-CHECK FOR TIMEOUT
8556 032660 104000          ERROR
8557          ;/TIME-OUT ERROR
8558          ;/WE FAILED TO COMPLETE
8559          ;/CURRENT OPERATION.
          ;/CONTINUES IN THIS LOOP

```

```

8560 ;/WOULD MAKE US "HANG" HERE
8561
8562 032662 000774 BR 21$
8563
8564 ;/RETURNS HERE-FROM-TIMED OUT.
8565 032664 122777 000377 146752 CMPB #377, @KMAD2 ;KMC CODE WILL RETURN A "377"
8566 032672 001370 BNE 21$ ;WHEN DONE COMMAND.
8567 032674 000207 RTS PC
8568
8569 032676 000000 $AERR: .WORD 0 ;=0 IF ADDR. LIST OK,=1 IF BAD.
8570
8571 ;*
8572 ;*THIS SUB CODE USED TO LOAD MICRO-CODE INTO LPA-11.
8573 ;* CALL = JSR R5,$LOAD
8574 ;* .WORD XX ;ADDR. OF MICRO CODE.
8575 ;* ;RETURNS HERE
8576 ;* NOTE: MICRO CODE FILE MUST END IN -1 DATA.
8577 ;*
8578
8579 $LOAD: MOV R4, -(SP) ;SAVE R4.
8580 032702 010046 MOV RO, -(SP) ;SAVE RO.
8581 032704 012500 1$: MOV (5)+, RO ;GET PROG. ADDR.
8582 032706 005077 146726 CLR @KMAD0 ;CLEAR CSR
8583 032712 005077 146732 CLR @KMAD4 ;CLEAR CRAM ADDR.
8584 032716 052777 002000 146714 2$: BIS #2000, @KMAD0 ;SELECT CRAM.
8585 032724 012077 146724 MOV (0)+, @KMAD6 ;WRITE DATA.
8586 032730 052777 020000 146702 BIS #2000, @KMAD0 ;SET CRAM WRITE
8587 032736 005077 146676 CLR @KMAD0 ;DISABLE CRAM.
8588 032742 005277 146702 INC @KMAD4 ;UPDATE CRAM ADDR.
8589 032746 021027 177777 CMP (0), #-1 ;ALL DONE?
8590 032752 001361 BNE 2$ ;NO LOOP.
8591 032754 005077 146670 CLR @KMAD4 ;CLEAR CRAM ADDR.
8592 032760 016500 177776 MOV -2(5), RO ;GET MICRO CODE ADDR.
8593
8594 032764 052777 002000 146646 3$: BIS #2000, @KMAD0 ;SELECT CRAM
8595 032772 022077 146656 CMP (RO)+, @KMAD6 ;DATA OK?
8596 032776 001013 BNE 5$ ;NO - REPORT AN ERROR.
8597 033000 021027 177777 CMP (0), #-1 ;ALL DONE?
8598 033004 001405 BEQ 4$ ;YES - EXIT
8599 033006 005077 146626 CLR @KMAD0 ;NO - DESELECT CRAM.
8600 033012 005277 146632 INC @KMAD4 ;UPDATE CRAM ADDR.
8601 033016 000762 BR 3$
8602
8603 033020 012600 4$: MOV (SP)+, RO ;RESTORE RO
8604 033022 012604 MOV (SP)+, R4 ;RESTORE R4
8605 033024 000205 RTS R5 ;EXIT
8606
8607 033026 5$: ;COME HERE ON LOAD ERROR
8608 033026 005745 TST -(5)
8609 033030 105204 INCB R4 ;UPDATE ERROR COUNTER.
8610 033032 100324 BPL 1$ ;IF NOT TOO MANY, TRY AGAIN.
8611 033034 000000 HALT ;MICRO CODE LOAD ERROR.
8612 ;KMC-11 FAULT. YOU COULD TRY
8613 033036 000722 BR 1$ ;TO PRESS CONTINUE TO GIVE IT

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8614
8615
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8627 033040 010046
8628 033042 012500
8629 033044 052700 000340
8630 033050 004737 033322
8631 033054 010037 033146
8632 033060 010077 146564
8633 033064 112777 000005 146552
8634 033072 004737 033322
8635 033076 011537 033150
8636 033102 112577 146542
8637
8638 033106 112777 000005 146530
8639 033114 004737 033322
8640 033120 111537 033152
8641 033124 112577 146520
8642 033130 112777 000005 146506
8643 033136 004737 033322
8644 033142 012600
8645 033144 000205
8646 033146 000000
8647 033150 000000
8648 033152 000000
8649
8650
8651
8652
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8654
8655
8656
8657
8658
8659 033154 010046
8660 033156 012500
8661 033160 052700 000300
8662 033164 004737 033322
8663 033170 110077 146454
8664 033174 112777 000005 146442
8665 033202 004737 033322
8666 033206 010037 033316
8667 033212

```

```

; ANOTHER CHANCE, BUT I DOUBT
; THAT THAT WOULD WORK. SINCE I'VE
; ALREADY GIVEN IT 177 (OCTAL) CHANCES.
; TRY RUNNING THE KMC-11 DIAGNOSTIC.

; *THIS ROUTINE ISSUES A WRITE COMMAND TO THE LPA-11
; *
; * CALL = JSR R5,$TLKW
; * .WORD 0 ;OFFSET OF DEVICE ADDR.
; * .WORD 0 ;DATA TO BE WRITTEN
; *
$TLKW: MOV RO, -(SP) ;SAVE RO
MOV (5)+, RO ;GET DEVICE OFFSET
BIS #340, RO ;ADD WRITE CODE.
JSR PC,$LPW ;WAIT FOR FAST PATH READY
MOV RO, W1
MOV RO, @KMAD4
MOVB #5, @KMAD2 ;ISSUE FAST PATH WRITE
JSR PC,$LPW ;WAIT FOR RDY
MOV (5), W2
MOVB (5)+, @KMAD4 ;WRITE LOW BYTE DATA.
MOVB #5, @KMAD2 ;FP WRITE
JSR PC,$LPW
MOVB (5), W3
MOVB (5)+, @KMAD4 ;WRITE HIGH BYTE
JSR PC,$LPW
MOV (SP)+, RO
RTS R5 ;EXIT DONE.
W1: 0
W2: 0
W3: 0

; *THIS ROUTINE ISSUES A READ COMMAND TO THE LPA-11
; *
; * CALL = JSR R5,$TLKr
; * .WORD 0 ;OFFSET OF DEVICE
; * ;RETURNS HERE
; * *DATA IN WORD $DATR
; *
$TLKR: MOV RO, -(SP) ;SAVE RO
MOV (5)+, RO ;GET OFFSET
BIS #300, RO ;ADD READ CODE
JSR PC,$LPW ;WAIT TILL READY
MOVB RO, @KMAD4
MOVB #5, @KMAD2 ;ISSUE WRITE FP
JSR PC,$LPW
MOV RO, RD1
IS:

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8668 033212 004537 033610 JSR R5, $TOU1 ; -TOUT-CHECK FOR TIMEOUT
8669
8670 033216 104000 ERROR ; /TIME-OUT ERROR
8671 ; /WE FAILED TO COMPLETE
8672 ; /CURRENT OPERATION.
8673 ; /CONTINUES IN THIS LOOP
8674 ; /WOULD MAKE US "HANG" HERE
8675
8676 033220 000774 BR 1$
8677
8678 ; /RETURNS HERE-FROM-TIMED OUT.
8679 033222 032777 000040 146410 BIT #BITS, @KMADO ; FAST PATH GOT DATA?
8680 033230 001370 BNE 1$
8681 033232 112777 000004 146404 MOVB #4, @KMAD2 ; ISSUE FAST PATH READ
8682 033240 004737 033322 JSR PC, $LPW
8683 033244 117737 146400 033320 MOVB @KMAD4, $DATR ; GET LOW BYTE
8684 033252
8685 033252 004537 033610 JSR R5, $TOU1 ; -TOUT-CHECK FOR TIMEOUT
8686
8687 033256 104000 ERROR ; /TIME-OUT ERROR
8688 ; /WE FAILED TO COMPLETE
8689 ; /CURRENT OPERATION.
8690 ; /CONTINUES IN THIS LOOP
8691 ; /WOULD MAKE US "HANG" HERE
8692
8693 033260 000774 BR 2$
8694
8695 ; /RETURNS HERE-FROM-TIMED OUT.
8696 033262 032777 000040 146350 BIT #BITS, @KMADO ; FAST PATH READY?
8697 033270 001370 BNE 2$
8698 033272 112777 000004 146344 MOVB #4, @KMAD2 ; ISSUE FAST PATH READ
8699 033300 004737 033322 JSR PC, $LPW
8700 033304 117737 146340 033321 MOVB @KMAD4, $DATR+1 ; SAVE HIGH BYTE
8701 033312 012600 MOV (SP)+, R0
8702 033314 000205 RTS R5
8703 033316 000000
8704 033320 000000 RD1: 0
SDATR: .WORD 0
8705
8706 ; THIS ROUTINE WAITS FOR KMC-CODE TO BECOME READY AS WELL
8707 ; AS FAST PATH TO BE READ.
8708
8709 ; CALL = JSR PC, $LPW
8710
8711 ; IT WILL TIME OUT IF TOO MUCH TIME IS TAKEN BY
8712 ; THE MICRO-PROCESSORS AND REPORT AN ERROR, THEN HALT.
8713
8714
8715 033322 010146 SLPW: MOV R1, -(SP) ; SAVE R1
8716 033324 005001 CLR R1
8717 033326 122777 000377 146310 1$: CMPB #377, @KMAD2 ; FINISHED INSTRUCTION?
8718 033334 001403 BEQ 2$
8719 033336 005201 INC R1 ; TIME OUT?
8720 033340 001372 BNE 1$
8721 033342 000411 BR 10$

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8722
8723 033344 032777 000020 146266 2$: BIT #BIT4, QKMADD ;FAST PATH READ?
8724 033352 001403 BEQ 3$
8725 033354 005201 INC R1 ;NO - TIME OUT?
8726 033356 001372 BNE 2$
8727 033360 000402 BR 10$ ;YES - REPORT AN ERROR
8728
8729 033362 012601 3$: MOV (SP)+, R1 ;RESTORE R1
8730 033364 000207 RTS PC ;EXIT
8731
8732 033366 10$:
8733 033366 104401 033374 TYPE ,65$ ;:TYPE ASCIZ STRING
8734 033372 000407 BR ,64$ ;:GET OVER THE ASCIZ
8735 ;:65$: .ASCIZ <200>#LPA-11 FAULT#
8736 033412 64$:
8737
8738 033412 000000 11$: HALT ;LPA-11 FAULT RUN LPA-11
8739 033414 000776 BR 11$ ;DIAGNOSTICS.
8740
8741
8742
8743
8744 ;*
8745 ;*THIS ROUTINE PROVIDES THE LINKAGE FROM USER CODE TO
8746 ;*A DEVICE ADDRESS ON THE I/O BUSS FOR WRITE ONLY.
8747 ;*
8748 ;* FIRST WE WILL DETERMINE IF THE ADDRESS HAS BEEN USED
8749 ;* BEFORE. IF NOT WE HAVE TO INITIALIZE THE LPA WITH
8750 ;* THAT ADDRESS.
8751 ;* WHEN THE ADDR. IS KNOWN BY THE LPA, DO THE OUTPUT BY
8752 ;* $TLKW
8753 ;*
8754 033416 010046 $OUTLP: MOV R0, -(SP) ;SAVE R0
8755 033420 010146 MOV R1, -(SP) ;SAVE R1
8756
8757 033422 012700 001666 MOV #.DVLS, R0 ;PROGRAM DEFINED LIST.
8758 033426 005001 CLR R1
8759 033430 005710 1$: TST (0) ;TERMINATOR REACHED?
8760 033432 001421 BEQ 10$ ;YES NEXT STEP.
8761 033434 027520 000000 CMP @ (5), (0)+ ;MATCH WITH ADDR IN LIST?
8762 033440 001402 BEQ 2$
8763 033442 005201 INC R1
8764 033444 000771 BR 1$
8765
8766 033446 010137 033464 2$: MOV R1, 3$ ;SAVE OFFSET, DEVICE KNOWN.
8767 033452 005725 TST (5)+
8768 033454 013537 033466 MOV @ (5)+, 4$ ;GET DATA TO BE WRITTEN
8769 033460 004537 033040 JSR R5, $TLKW ;DO WRITE
8770 033464 000000 3$: .WORD 0 ;DEVICE OFFSET
8771 033466 000000 4$: .WORD 0 ;DATA TO BE WRITTEN.
8772 033470 012601 MOV (SP)+, R1
8773 033472 012600 MOV (SP)+, R0
8774 033474 000205 RTS R5
8775 033476 017520 000000 10$: MOV @ (5), (0)+ ;SAVE ADDR.

```

```

8776 033502 005010          CLR      (0)
8777 033504 004537 032020 JSR      R5,$LPAI
8778 033510 001666          .WORD   .DVLS
8779 033512 000755          BR       2$
8780
8781          ;*
8782          ;*THIS ROUTINE PROVIDES THE LINKAGE FROM USER CODE
8783          ;*TO A DEVICE ADDR. ON THE I/O BUSS FOR READ ONLY.
8784          ;*
8785          ;*FIRST WE WILL DETERMINE IF THE ADDRESS HAS BEEN
8786          ;*USED BEFORE. IF NOT, WE HAVE TO INITIALIZE THE LPA
8787          ;*WITH THE NEW ADDR.
8788          ;*WHEN THE ADDR IS KNOWN WE CAN DO OUTPUT THROUGH
8789          ;*$TLKR
8790          ;*
8791          ;*      CALL THROUGH      MOVEI   DATA,ADDR.
8792          ;*      WHICH EQUALS:
8793          ;*      JSR      R5,$INLP
8794          ;*      .WORD   XX      ADDR OF DEVICE
8795          ;*      .WORD   YY      ADDR TO $TORE READ DATA.
8796 033514 010046          $INLP:  MOV     RD,-(SP)      ;SAVE RD
8797 033516 010146          MOV     R1,-(SP)      ;SAVE R1
8798
8799 033520 012700 001666          MOV     #.DVLS,RD     ;PROG DEFINED ADDR. LIST.
8800 033524 005001          CLR     R1
8801 033526 005710          1$:   TST     (0)      ;EOL REACHED?
8802 033530 001420          BEQ     10$         ;YES - DEFINE NEW ADDR.
8803
8804 033532 027520 000000          CMP     @ (5), (0)+  ;ADDR. MATCH?
8805 033536 001402          BEQ     2$
8806 033540 005201          INC     R1
8807 033542 000771          BR      1$
8808
8809 033544 010137 033556          2$:   MOV     R1,3$      ;SAVE LIST OFFSET
8810 033550 005725          TST     (5)+
8811 033552 004537 033154          JSR     R5,$TLKR    ;GO READ DEVICE
8812          $OFS=.
8813 033556 000000          3$:   .WORD   0      ;OFFSET OF DEVICE
8814
8815 033560 013735 033320          MOV     $DATR,@ (5)+ ;STORE DATA.
8816 033564 012601          MOV     (SP)+,R1    ;RESTORE R1
8817 033566 012600          MOV     (SP)+,R0    ;RESTORE R2
8818 033570 000205          RTS     R5          ;EXIT
8819
8820 033572 017520 000000          10$:  MOV     @ (5), (0)+
8821 033576 005010          CLR     (0)
8822 033600 004537 032020          JSR     R5,$LPAI
8823 033604 001666          .WORD   .DVLS
8824 033606 000756          BR      2$
8825
8826          ;*
8827          ;*$STOUT ROUTINE USED TO WATCH IF
8828          ;*WE'RE IN A LOOP TOO-LONG
8829          ;*      CALL= JSR R5, $STOUT
8829          ;*      ERROR X ;RETURNS HERE ON TIMEOUT
    
```

```

8830                                     ;*
8831                                     ;*
8832                                     ;*
8833
8834 033610 020537 033644 $TOUT: CMP R5,$SAD ;SAME ADDR?
8835 033614 001405 BEQ 1$
8836 033616 010537 033644 MOV R5,$SAD ;NO-SAVE THIS ADDR.
8837 033622 005037 033646 CLR $CNT ;CLR CNT AT ADDR.
8838 033626 000403 BR 2$
8839 033630 005237 033646 1$: INC $CNT ;OVERFLOW?
8840 033634 100402 BMI 3$ ;YES-ERROR RETURN
8841 033636 062705 000004 2$: ADD #4,R5 ;NO-NON ERROR RETURN
8842 033642 000205 3$: RTS R5 ;RETURN.
8843
8844 033644 000000 $SAD: .WORD 0 ;CONTAINS LOOP ADDR.
8845 033646 000000 $CNT: .WORD 0 ;# OF TIMES AT ADDR.
8846
8847
8848 ;*
8849 ;* THIS ROUTINE REPLACES WHAT THE USER WOULD ORDINARILY
8850 ;* USE FOR A RESET. FIRST WE DO A RESET INSTRUCTION.
8851 ;* THEN WE CLR ".DVLST" WHICH FORCES US TO RESET BOTH THE
8852 ;* KMC AND DMC AS SOON AS A DEVICE IS REFERENCED.
8853 ;*
8854 ;* CALL=JSR PC,$RESET ;REPLACES "RESET INSTRUCTION
8855 ;* ;RETURNS HERE.
8856 033650 000005 $RESET: RESET ;RESET THE WORLD.
8857
8858 ;*
8859 033662 005737 032676 ;* MOV 2$,$1$ ;/READ DEVICE REG 2$,PUT DATA IN 1$.
8860 033666 001004 TST $AERR ;IF NO ERROR,LOOP
8861 033670 062737 000002 033704 BNE 10$ ;THERE WAS AN ERROR.
8862 ADD #2,2$ ;UPDATE DEVICE ADDR.
8863 ;YOU SEE ,WE HAVE TO PROTECT OUR SELF!
8864 ;IF 2$ CONTAINED A VALID ADDR,WE
8865 ;MUST KEEP TRYING UNTIL WE GENERATE
8866 ;AN INVALID ADDR.
8866 033676 000764 BR $RESET
8867 033700 10$:
8868 033700 000207 RTS PC
8869 033702 000000 1$: .WORD 0 ;JUNK LOC.
8870 033704 160000 2$: .WORD 160000 ;DUMB ADDR. FORCES INIT OF DMC/KMC.
8871
8872
8873 ;
8874 ;SDELAY- ROUTINE TO GIVE A MINOR DELAY.
8875 ; IS NOT TIME DEPENDENT CODE SENCE
8876 ; NOT USED TO GET SPECIFIC TIME BUT
8877 ; JUST A LITTLE DELAY.
8878 ;
8879 ;
8880 ; THAT IS UNLESS A REAL TIME CLOCK IS PRESENT!
8881 ; THEN WE'LL GENERATE A TIME BETWEEN 16MS TO 32 MS
8882 ;
8883 ;
8884 CALL= JSR PC, SDELAY
    
```



```

8884
8885 033706
8886 033706 005737 033770
8887 033712 100016
8888 033714 012737 000002 033760
8889 033722 052777 000115 000040
8890 033730 005037 177776
8891 033734 005737 033760
8892 033740 001375
8893 033742 005077 000022
8894
8895 033746 000207
8896 033750 105237 033760
8897 033754 001375
8898 033756 000207
8899
8900 033760 000000
8901
8902 033762 005337 033760
8903 033766 000002
8904 033770 000000
8905
8906
8907
8908
8909
8910
8911
8912
8913
8914
8915
8916 033772
8917 033772 005037 001666
8918 033776
8919 033776 104401 034004
8920 034002 000405
8921
8922 034016
8923 034016 105777 145122
8924 034022 100375
8925 034024 117737 145116 034146
8926 034032 104401 034146
8927 034036 142737 000240 034146
8928 034044 104412
8929 034046 012637 034144
8930 034052 123727 034146 000104
8931 034060 001411
8932
8933 034062 004537 033514
8934 034066 034144
8935 034070 034102
8936
8937 034072 013746 034102

;
SDELAY: TST RTCCSR ;CLOCK PRESENT?
        BPL 10$
        MOV #2,TIME
        BIS #115,RTCCSR ;START CLOCK
        CLR PS
1$: TST TIME
     BNE 1$
     CLR RTCCSR ;STOP CLOCK

10$: RTS PC
     INCB TIME
     BNE 10$
     RTS PC

TIME: .WORD 0

CLKINT: DEC TIME
        RTI

RTCCSR: .WORD 0 ;CLOCK CSR IF USED.

;
; *THIS MACRO ALLOWS THE OPERATOR TO TALK TO
; *ANY DEVICE ON THE I/O BUS
; *USER MUST START AT THIS ADDR.
; *HE MUST SAY EITHER "E" FOR EXAMINE, OR "D" FOR DEPOSIT.
; *"E" IS DEFAULT.
; *NEXT, HE MUST SUPPLY AN ADDR.
; *NOTE IF ADDR. IS NOT FOUND ON I/O BUS, A HALT
; *WILL OCCUR.

$UTK: CLR .DVLS
21$: TYPE 65$ ;;TYPE ASCIZ STRING
     BR 64$ ;;GET OVER THE ASCIZ
;;65$: .ASCIZ <200>#E OR D?#
64$:
1$: TSTB 2$TKS
     BPL 1$
     MOVB 2$TKB,20$ ;GET INPUT
     TYPE 20$ ;ECHO, NEXT MESSAGE.
     BICB #240,20$ ;STRIP PARITY, LC
     RDOCT ;GET ADDR.
     MOV (SP)+,14$
     CMPB 20$,#D ;DEPOSIT?
     BEQ 10$

2$: JSR R5,$INLP ;GET DATA
     .WORD 14$
     .WORD 5$

MOV 5$,-(SP) ;;SAVE 5$ FOR TYPEOUT
    
```

```

8938 034076 104402
8939 034100 000736
8940 034102 000000
8941
8942 034104
8943 034104 104401 034112
8944 034110 000404
8945
8946 034122
8947 034122 104412
8948 034124 012637 034142
8949
8950 034130 004537 033416
8951 034134 034144
8952 034136 034142
8953 034140 000716
8954
8955 034142 000000
8956 034144 000000
8957 034146 100001 042504 044526
8958 034154 042503 040440 042104
8959 034162 036522 000040
8960
8961
8962
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8965
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8967
8968
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8971
8972
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8977
8978
8979
8980
8981
8982
8983
8984 034166 012537 034176
8985 034172 004537 033514
8986 034176 000000
8987 034200 034274
8988 034202 113777 033556 145444
8989 034210 113777 033556 145440
8990 034216 013737 034176 034236
8991 034224 062737 000002 034236

```

```

TYPOC
BR 21$ ;;GO TYPE--OCTAL ASCII(ALL DIGITS)
5$: .WORD 0 ;LOOP.
10$: TYPE 67$ ;;TYPE ASCIZ STRING
BR 66$ ;;GET OVER THE ASCIZ
67$: .ASCIZ <200>#DATA= #
66$: RDOCT
MOV (SP)+,13$
11$: JSR R5,$OUTLP ;OUTPUT ROUTINE.
12$: .WORD 14$ ;DEVICE ADDR.
.WORD 13$ ;DATA
BR 21$
13$: .WORD 0
14$: .WORD 0
20$: .ASCIZ <1><200>#DEVICE ADDR= #

```

.EVEN

```

: THIS ROUTINE LOOKS THROUGH CURENT .DVLS FOR A/D ADDR.
: IF UNFOUND GENERATES IT. THIS ROUTINE'S WHOLE PURPOSE IS
: TO SET UP THE USER PROGRAM TO LINK TO FILE "DRLPX2" FOR
: SAMPLE TAKEING PURPOSES.
: TO TAKE SAMPLES, THE USER PROGRAM MUST SET UP
: A/D CSR IN BSEL 4 AND 5.
: (2) HE MUST CALL THIS ROUTINE:
: JSR R5,$SPUTS ;CALL SET UP ROUTINE.
: .WORD ADCSR ;ADDR. OF A/D CSR.
: ;RETURNS HERE ;KMC BSEL 3,6,7 PERMINENTLY SET UP
: ;(UNTILL ONE DOES A RESET)
:
: (3)THE USER MUST PUT CODE 006 INTO KMC REG 2 TO
: START CONVERSION CAUTION*DO WITH MOV B INSTR.!
: (4)MONITOR KMC REG 2 FOR CODE 377 (DRLPX2 IS DONE)
: (5)READ KMC REG 4,5 FOR A/D RESULT.
: (6) TO TAKE MORE SAMPLES, SIMPLY PUT A/D CSR INTO
: BSEL 4,5 AND CODE 6 INTO BSEL 2.

```

```

$SPUTS: MOV (5)+,1$ ;GET ADDR OF ADDR. OF A/D
JSR R5,$INLP
1$: .WORD 0
.WORD 10$
MOV $OFS,$KMA6
MOV $OFS,$KMA7
MOV 1$,2$
ADD #2,2$

```

8992	034232	004537	033514		JSR	R5,\$INLP
8993	034236	000000		2\$:	.WORD	0
8994	034240	034274			.WORD	10\$
8995	034242	113777	033556	145376	MOVB	\$OFS,@KMA03
8996	034250	152777	000340	145376	BISB	#340,@KMA06
8997	034256	152777	000300	145372	BISB	#300,@KMA07
8998	034264	152777	000300	145354	BISB	#300,@KMA03
8999	034272	000205			RTS	R5
9000	034274	000000		10\$:	.WORD	0
9001						
9002						
9003		000001			.END	



APRIOR= 000006  
APRITY 001352  
APTCSU= 000040  
APTENV= 000001  
APTSIZ= 000200  
APTSP0= 000100  
ASR 001326

222*	317													
397*	726													
8027	8132*													
7623	8020	8088	8130*											
669	8129*													
8022	8090	8131*												
383*	681*	706	759	869	891	908	1004	1006	1024	1026	1059	1061		
1079	1081	1114	1116	1134	1136	1169	1171	1189	1191	1224	1226	1244		
1246	1279	1281	1299	1301	1334	1336	1354	1356	1389	1391	1409	1411		
1444	1446	1464	1466	1499	1501	1519	1521	1554	1556	1574	1576	1609		
1611	1629	1631	3496	3542	3588	3781	3783	3788	3792	3827	3829	3832		
3834	3853	3876	3885	3887	3890	3944	3954	3959	3962	4017	4025	4027		
4030	4034	4051	4085	4097	4099	4102	4106	4164	4169	4181	4217	4222		
4234	4270	4275	4287	4323	4328	4340	4376	4381	4393	4429	4434	4446		
4483	4488	4500	4544	4549	4598	4604	4606	4609	4611	4653	4659	4661		
4664	4714	4722	4724	4727	4730	4777	4783	4788	4791	4846	4852	4857		
4860	4904	4910	4912	4915	4952	4958	4960	4963	5005	5010	5013	5074		
5083	5085	5088	5160	5169	5179	5195	5239	5242	5295	5321	5324	5383		
5396	5399	5452	5492	5499	5545	5602	5659	5716	5773	5830	5898	5914		
5916	5919	5980	5985	5988	6044	6051	6054	6062	6065	6100	6103	6155		
6162	6165	6173	6176	6211	6214	6266	6273	6276	6284	6287	6322	6325		
6377	6384	6387	6395	6398	6433	6436	6490	6509	6512	6550	6553	6604		
6623	6626	6664	6667	6718	6737	6740	6778	6781	6832	6851	6854	6892		
6895	6999	7013	7015	7018	7021	7096	7115	7117	7120	7199	7206	7209		
7221	7292	7304	7308	7311	7322	7394	7404	7426	8379	8393				

ASWREG= 000000  
ATESTN= 000000  
AUNIT = 000000  
#USWR = 000000  
AVECP2 001344  
AVECT 001342  
AVECT1= 000344  
AVECT2= 000000  
BBR 001336

317	330													
317	321													
317	324													
317	331													
392*	720*													
391*	718													
221*	317	356	620	621										
317	357													
388*	714*	767	965	967	3049	3051	3069	3071	3104	3106	3124	3126		
3159	3161	3179	3181	3214	3216	3234	3236	3269	3271	3289	3291	3324		
3326	3344	3346	3379	3381	3399	3401	3434	3436	3454	3456	3644	3693		
3743	5229	5306	5388	5457	5496	5549	5606	5663	5720	5777	5834	5905		
6492	6606	6720	6834	7401	8387									
389*	716*	769	3649	3697	3747	5244	5329	5417	5464	5560	5617	5674		
5731	5788	5845	6514	6529	6558	6628	6643	6672	6742	6757	6786	6856		
6871	6900	8389	8399	8401										

BCR 001340

204*	1606	1661	2991	3046	5234	5977								
194*	204	3834	4106	4611										
193*	203													
192*	202													
191*	201													
190*	200													
189*	199	4034	4181	4234	4287	4340	4393	4446	4500	7308				
188*	198													
187*	197	4051	4730	7414										
186*	196	7786												
185*	195	7634	7794											
203*	1551	1716	2935	3101	5234	8522								
184*	2211	4724	4788	4857	4912	4960	5010	7015	7611					

BIT0 = 000001  
BIT00 = 000001  
BIT01 = 000002  
BIT02 = 000004  
BIT03 = 000010  
BIT04 = 000020  
BIT05 = 000040  
BIT06 = 000100  
BIT07 = 000200  
BIT08 = 000400  
BIT09 = 001000  
BIT1 = 000002  
BIT10 = 002000

BIT11 = 004000	183#	2266	2543	5160	5221	5239	5296	5321	5396	5916	6046	6062	6100
	6157	6173	6211	6268	6284	6322	6379	6395	6433	6492	6509	6550	6606
BIT12 = 010000	6623	6664	6720	6737	6778	6834	6851	6892	7801	8462			
	182#	2321	3785	3829	3887	3959	4027	4099	4606	4661	5085	5985	7117
	7206												
BIT13 = 020000	181#	1111	2376	3824	7036	7138	7235	7337	7441	7618			
BIT14 = 040000	180#	1056	2431	3987	5348	7772	8454						
BIT15 = 100000	179#	1001	2486	7018	8462								
BIT2 = 000004	202#	1496	1771	2879	3156								
BIT3 = 000010	201#	1441	1826	2823	3211								
BIT4 = 000020	200#	1881	2767	3266	8723								
BIT5 = 000040	199#	1386	1936	2711	3321	5234	6492	6606	6720	6834	8466	8679	8696
BIT6 = 000100	198#	1331	1991	2655	3376								
BIT7 = 000200	197#	1276	2046	2599	3431								
BIT8 = 000400	196#	1221	2101	7112									
BIT9 = 001000	195#	1166	2156	7112	7206								
BPRITY 001354	398#	726*											
BPTVEC= 000014	211#												
BSR 001334	387#	712*	765	928	930	2546	2548	2566	2568	2602	2604	2622	2624
	2658	2660	2678	2680	2714	2716	2734	2736	2770	2772	2790	2792	2826
	2828	2846	2848	2882	2884	2902	2904	2938	2940	2958	2960	2994	2996
	3014	3016	3642	3685	3735	4540	4709	4768	4837	5072	5080	5137	5163
	5224	5234	5237	5299	5312	5315	5385	5391	5394	5401	5454	5494	5547
	5552	5565	5604	5609	5622	5661	5666	5679	5718	5723	5736	5775	5780
	5793	5832	5837	5850	5900	5908	5911	6042	6049	6153	6160	6264	6271
	6375	6382	6488	6495	6497	6500	6503	6602	6609	6611	6614	6617	6716
	6723	6725	6728	6731	6830	6837	6839	6842	6845	7001	7098	7201	7294
	7396	7411	7414	8385	8394								
BVECT 001346	394#	722*											
BVECT2 001350	395#	724*											
CKSWR = 104407	7607	7633	7771	8215#									
CLKINT 033762	8902#												
CR = 000015	119#	8066	8076										
CRLF = 000200	120#	8037	8076										
DDISP = 177570	126#	294	657										
DF0 032014	423	431	439	447	455	463	471	480	488	496	501	502	503
	504	511	519	527	535	542	550	558	566	574	582	590	8405#
DH1 030777	421	429	8301#										
DH10 031263	477	8337#											
DH12 031422	494	525	8354#										
DH14 031441	509	533	8357#										
DH20 031457	540	8360#											
DH23 031521	564	8366#											
DH26 031563	588	8372#											
DH3 031035	437	8307#											
DH4 031073	445	486	548	556	8313#								
DH5 031131	453	8319#											
DH6 031167	461	8325#											
DH7 031225	469	517	572	580	8331#								
DISPLA 001142	294#	657*	665*	7610*	7816*								
DISPRE 000174	97#	665											
DRLPX2= *****	14#	8452											
DSWR = 177570	125#	293	656										
DT1 031612	422	430	541	565	8379#								

G



LPADL	001650	611#													
LPCI	001640	602#													
LPCO	001644	607#													
LPMR	001642	605#													
LPMS1	001654	615#													
LPMS2	001656	617#													
LPSO	001646	609#													
LS210	023376	103	6986#												
LS214	023564	104	7083#												
LS220	024000	105	7186#												
LS224	024160	106	7279#												
LS230	024372	107	7381#												
P	= 000012	1644#	1699#	1754#	1809#	1864#	1919#	1974#	2029#	2084#	2139#	2194#	2249#	2304#	
		2359#	2414#	2469#	2524#	3029#	3084#	3139#	3194#	3249#	3304#	3359#	3414#	3469#	
		4811#	4880#												
PC	=%000007	138#	5458#	6935*	6938*	6945*	6950	7620*	7626*	7679*	7912*	8025*	8044*	8051*	
		8058#	8072*	8074*	8107*	8124*	8516*	8518*	8520*	8567*	8630*	8634*	8639*	8643*	
		8662*	8665*	8682*	8699*	8730*	8868*	8895*	8898*						
PIR0	= 177772	124#													
PIRQVE	= 000240	218#													
PRO	= 000000	141#													
PR1	= 000040	142#													
PR2	= 000100	143#													
PR3	= 000140	144#													
PR4	= 000200	145#													
PR5	= 000240	146#													
PR6	= 000300	147#													
PR7	= 000340	148#													
PS	= 177776	121#	122	8890*											
PSW	= 177776	122#													
PWRVEC	= 000024	213#	645*	646*	8137*	8138*	8147*	8153*	8165*	8166*					
RDCHR	= 104410	7971	8216#												
RDLIN	= 104411	7835	8217#												
RDOCT	= 104412	8218#	8928	8947											
RD1	033316	8666#	8703#												
RESVEC	= 000010	208#													
RSTART	002434	102	727#												
RTCCSR	033770	8886	8889#	8893*	8904#										
RO	=%000000	129#	689	691*	694*	695	700*	703*	704*	706*	707*	708	709*	710	
		711#	712	713*	714	715*	716	718*	719*	720	721*	722	723*	724	
		4169*	4170*	4222*	4223*	4275*	4276*	4328*	4329*	4381*	4382*	4434*	4435*	4489*	
		4490*	5169*	5170*	5499*	5500*	5553*	5554*	5610*	5611*	5667*	5668*	5724*	5725*	
		5781*	5782*	5838*	5839*	6056*	6073*	6095*	6103*	6167*	6184*	6206*	6214*	6278*	
		6295*	6317*	6325*	6389*	6406*	6428*	6436*	6503*	6521*	6545*	6553*	6617*	6635*	
		6659*	6667*	6731*	6749*	6773*	6781*	6845*	6863*	6887*	6895*	6942*	6945	7651	
		7652*	7653*	7660*	7661*	7662*	7663*	7664*	7665	7670	7675*	7677*	7681	7683	
		7702	7712*	7716	7732	7733	7746*	7832	7836*	7839	7855*	8018	8019*	8024	
		8029	8032*	8084	8092*	8096	8097	8099*	8100*	8101	8123*	8139	8164*	8184	
		8185*	8186	8187*	8188*	8189*	8190*	8580	8581*	8592*	8595	8603*	8627	8628*	
		8629*	8631	8632	8644*	8659	8660*	8661*	8663	8666	8701*	8754	8757*	8773*	
		8796	8799*	8817*											
R1	=%000001	130#	690	692*	696	699*	7703	7716*	7717	7721	7745*	7833	7837*	7841*	
		7843*	7845*	7848*	7851	7854*	8085	8122*	8140	8163*	8458	8459*	8460*	8463*	
		8511*	8512	8517	8519	8546*	8715	8716*	8719*	8725*	8729*	8755	8758*	8763*	



R2	=%000002	8766	8772*	8797	8800*	8806*	8809	8816*	7731	7736*	7744*	7834	7838*	7842*
		131*	7704	7715*	7719*	7722	7729*	7730*						
R3	=%000003	7844*	7846*	7852	7853*	8141	8162*							
		132*	7548	7557*	7563*	7564*	7567*	7572*	7573*	7574	7583*	7705	7713*	7714*
		7728*	7731*	7740*	7741*	7743*	7967	7968*	7969	7972*	7973	7977	7979	7981*
R4	=%000004	7983*	8142	8161*										
		133*	7549	7551*	7552*	7553*	7554	7555*	7569	7571*	7579*	7582*	8143	8160*
R5	=%000005	8579	8604*	8609*										
		134*	759*	761*	763*	765*	767*	769*	805*	807*	844*	846*	889*	891*
		908*	928*	930*	965*	967*	1004*	1006*	1024*	1026*	1059*	1061*	1079*	1081*
		1114*	1116*	1134*	1136*	1169*	1171*	1189*	1191*	1224*	1226*	1244*	1246*	1279*
		1281*	1299*	1301*	1334*	1336*	1354*	1356*	1389*	1391*	1409*	1411*	1444*	1446*
		1464*	1466*	1499*	1501*	1519*	1521*	1554*	1556*	1574*	1576*	1609*	1611*	1629*
		1631*	1664*	1666*	1684*	1686*	1719*	1721*	1739*	1741*	1774*	1776*	1794*	1796*
		1829*	1831*	1849*	1851*	1884*	1886*	1904*	1906*	1939*	1941*	1959*	1961*	1994*
		1996*	2014*	2016*	2049*	2051*	2069*	2071*	2104*	2106*	2124*	2126*	2159*	2161*
		2179*	2181*	2214*	2216*	2234*	2236*	2269*	2271*	2289*	2291*	2324*	2326*	2344*
		2346*	2379*	2381*	2399*	2401*	2434*	2436*	2454*	2456*	2489*	2491*	2509*	2511*
		2546*	2548*	2566*	2568*	2602*	2604*	2622*	2624*	2658*	2660*	2678*	2680*	2714*
		2716*	2734*	2736*	2770*	2772*	2790*	2792*	2826*	2828*	2846*	2848*	2882*	2884*
		2902*	2904*	2938*	2940*	2958*	2960*	2994*	2996*	3014*	3016*	3049*	3051*	3069*
		3071*	3104*	3106*	3124*	3126*	3159*	3161*	3179*	3181*	3214*	3216*	3234*	3236*
		3269*	3271*	3289*	3291*	3324*	3326*	3344*	3346*	3379*	3381*	3399*	3401*	3434*
		3436*	3454*	3456*	3496*	3498*	3503*	3542*	3548*	3550*	3588*	3598*	3600*	3642*
		3644*	3649*	3685*	3693*	3697*	3735*	3743*	3747*	3781*	3783*	3788*	3792*	3827*
		3829*	3832*	3834*	3853*	3876*	3878*	3885*	3887*	3890*	3894*	3944*	3946*	3954*
		3959*	3962*	3968*	4017*	4020*	4025*	4027*	4030*	4034*	4051*	4085*	4094*	4097*
		4099*	4102*	4106*	4123*	4164*	4166*	4169*	4175*	4181*	4217*	4219*	4222*	4228*
		4234*	4270*	4272*	4275*	4281*	4287*	4323*	4325*	4328*	4334*	4340*	4376*	4378*
		4381*	4387*	4393*	4429*	4431*	4434*	4440*	4446*	4483*	4485*	4488*	4495*	4500*
		4540*	4544*	4546*	4549*	4554*	4559*	4598*	4601*	4604*	4606*	4609*	4611*	4653*
		4656*	4659*	4661*	4664*	4666*	4709*	4714*	4722*	4724*	4727*	4730*	4768*	4777*
		4780*	4783*	4786*	4788*	4791*	4796*	4837*	4846*	4849*	4852*	4855*	4857*	4877*
		4865*	4904*	4907*	4910*	4912*	4915*	4917*	4952*	4955*	4958*	4960*	4963*	4965*
		5005*	5008*	5010*	5013*	5015*	5072*	5074*	5077*	5080*	5083*	5085*	5088*	5095*
		5116*	5137*	5160*	5163*	5166*	5169*	5175*	5179*	5195*	5224*	5229*	5234*	5237*
		5239*	5242*	5244*	5295*	5299*	5306*	5312*	5315*	5321*	5324*	5329*	5383*	5385*
		5388*	5391*	5394*	5396*	5399*	5401*	5417*	5452*	5454*	5457*	5464*	5492*	5494*
		5496*	5499*	5507*	5545*	5547*	5549*	5552*	5560*	5565*	5602*	5604*	5606*	5609*
		5617*	5622*	5659*	5661*	5663*	5666*	5674*	5679*	5716*	5718*	5720*	5723*	5731*
		5736*	5773*	5775*	5777*	5780*	5788*	5793*	5830*	5832*	5834*	5837*	5845*	5850*
		5898*	5900*	5902*	5905*	5908*	5911*	5914*	5916*	5919*	5921*	5980*	5983*	5985*
		5988*	5993*	6042*	6044*	6046*	6049*	6051*	6054*	6062*	6065*	6067*	6081*	6100*
		6103*	6109*	6153*	6155*	6157*	6160*	6162*	6165*	6173*	6176*	6178*	6192*	6211*
		6214*	6220*	6264*	6266*	6268*	6271*	6273*	6276*	6284*	6287*	6289*	6303*	6322*
		6325*	6331*	6375*	6377*	6379*	6382*	6384*	6387*	6395*	6398*	6400*	6414*	6433*
		6436*	6442*	6488*	6490*	6492*	6495*	6497*	6500*	6503*	6509*	6512*	6514*	6529*
		6550*	6553*	6558*	6602*	6604*	6606*	6609*	6611*	6614*	6617*	6623*	6626*	6628*
		6643*	6664*	6667*	6672*	6716*	6718*	6720*	6723*	6725*	6728*	6731*	6737*	6740*
		6742*	6757*	6778*	6781*	6786*	6830*	6832*	6834*	6837*	6839*	6842*	6845*	6851*
		6854*	6856*	6871*	6892*	6895*	6900*	6999*	7001*	7013*	7015*	7018*	7021*	7096*
		7098*	7111*	7115*	7117*	7120*	7123*	7199*	7201*	7206*	7209*	7221*	7292*	7294*
		7299*	7304*	7308*	7311*	7322*	7394*	7396*	7401*	7404*	7411*	7414*	7426*	7550
		7556*	7558*	7560*	7561*	7562*	7563	7581*	7706	7708*	7710*	7717*	7721*	7736

R6 =%000006  
R7 =%000007  
SDELAY 033706  
SP =%000006

7742*	8144	8159*	8451*	8473*	8527*	8547*	8554*	8605*	8645*	8668*	8685*	8702*
8769*	8774*	8777*	8811*	8818*	8822*	8834	8836	8841*	8842*	8859*	8933*	8950*
8985*	8992*	8999*										
135#	633*	634*	635	7468	7483*	7485						
136#												
8885#												
137#	637*	654*	662*	666	689*	690*	699	700	727*	728*	729*	7475*
7487*	7540*	7541	7542	7543*	7548*	7549*	7550*	7556	7581	7582	7583	7584*
7585*	7615	7636*	7639*	7651*	7656*	7677	7681*	7702*	7703*	7704*	7705*	7706*
7707*	7708	7711*	7724	7726*	7728	7738	7740	7742	7743	7744	7745	7746
7748*	7749*	7777*	7780	7782	7783	7812	7813	7817*	7830*	7831*	7832*	7833*
7834*	7836	7839*	7847*	7848	7850	7851*	7853	7854	7855	7872*	7873*	7874
7881*	7884*	7885*	7889*	7890*	7894	7897*	7901	7903	7905	7906*	7913	7915
7917*	7918	7920*	7921*	7922*	7923*	7924*	7939*	7940*	7943*	7944*	7945	7949*
7950*	7951	7954	7956	7958*	7967*	7972	7983	7984*	7985*	7986*	8018*	8019
8029*	8031	8032	8033*	8035	8037	8039	8045	8047*	8049*	8057*	8061	8065
8066	8070	8084*	8085*	8092	8093*	8104	8105*	8106*	8116	8117*	8122	8123
8139*	8140*	8141*	8142*	8143*	8144*	8145*	8146	8154*	8158	8159	8160	8161
8162	8163	8164	816*	8185	8195*	8196*	8426*	8448	8449	8458*	8546	8579*
8580*	8603	8604	8627*	8644	8659*	8701	8715*	8729	8754*	8755*	8772	8773
8796*	8797*	8816	8817	8929	8937*	8948						
112#	637	727										
100	630#											
123#												
293#	635	656*	658	664*	671*	3987	5348	7036	7138	7235	7337	7441
7611	7618	7630	7634	7772	7786	7788	7794	7801	7868	7905*	8145	8158*
98#	664	7868	7881									
176#												
166#	176											
165#	175											
164#	174											
163#	173											
162#	172											
161#	171											
160#	170											
159#	169											
158#	168											
157#	167											
175#												
156#												
155#												
154#												
153#												
152#												
151#												
174#												
173#												
172#												
171#												
170#												
169#												
168#												
167#												
209#												

STACK = 001100  
START 001730  
STKLMT= 177774  
SWR 001140  
SWREG 000176  
SW0 = 000001  
SW00 = 000001  
SW01 = 000002  
SW02 = 000004  
SW03 = 000010  
SW04 = 000020  
SW05 = 000040  
SW06 = 000100  
SW07 = 000200  
SW08 = 000400  
SW09 = 001000  
SW1 = 000002  
SW10 = 002000  
SW11 = 004000  
SW12 = 010000  
SW13 = 020000  
SW14 = 040000  
SW15 = 100000  
SW2 = 000004  
SW3 = 000010  
SW4 = 000020  
SW5 = 000040  
SW6 = 000100  
SW7 = 000200  
SW8 = 000400  
SW9 = 001000  
TBITVE= 000014

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TPVEC =	000064	217#				
TRAPVE =	000034	215#	643*	644*		
TRTVEC =	000014	210#				
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TST10	003202	1050#				
TST100	012702	4155#				
TST101	013022	4208#				
TST102	013142	4261#				
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TST107	013760	4531#				
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TST110	014074	4586#				
TST111	014216	4640#				
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TST117	015256	4994#				
TST12	003416	1160#				
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TST122	015754	5218#				
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TST15	003740	1325#				
TST16	004046	1380#				
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TST20	004262	1490#
TST21	004370	1545#
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TST4	002676	881#
TST40	006422	2370#
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TST42	006636	2480#
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TST5	002760	920#
TST50	007502	2817#
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TST52	007716	2929#
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TST56	010346	3150#
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TST60	010562	3260#
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TST62	010776	3370#
TST63	011104	3425#
TST64	011212	3486#
TST65	011272	3531#
TST66	011356	3581#
TST67	011442	3632#
TST7	003074	995#
TST70	011522	3678#
TST71	011606	3728#
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TST73	011756	3819#
TST74	012062	3869#
TST75	012204	3933#
TST76	012366	4011#
TST77	012534	4079#
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1994	1996	2010*	2014	2046*	2049	2051	2065*	2069	2101*	2104	2106	2120*
2124	2156*	2159	2161	2175*	2179	2211*	2214	2216	2230*	2234	2266*	2269*
2271	2285*	2289	2321*	2324	2326	2340*	2344	2376*	2379	2381	2395*	2399*
2431*	2434	2436	2450*	2454	2486*	2491	2491	2505*	2509	2543*	2546	2548
2562*	2566	2599*	2602*	2604	2618*	2622	2655*	2658	2660	2674*	2678	2711*
2714	2716	2730*	2734	2767*	2770	2772	2786*	2790	2823*	2826	2828	2842*
2846	2879*	2882	2884	2898*	2902	2935*	2938	2940	2954*	2958	2991*	2994
2996	3010*	3014	3046*	3049	3051	3065*	3069	3101*	3104	3106	3120*	3124
3156*	3159	3161	3175*	3179	3211*	3214	3216	3230*	3234	3266*	3269	3271
3285*	3289	3321*	3324	3326	3340*	3344	3376*	3379	3381	3395*	3399	3431*
3434	3436	3450*	3454	3493*	3496	3498	3499*	3539*	3542	3543*	3548	3551*
3585*	3588	3593*	3598	3601	3639*	3642	3644	3645*	3682*	3685	3690*	3693
3698	3732*	3735	3740*	3743	3748	3778*	3781	3783	3785*	3788	3824*	3827
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3946	3963*	3969	3984	3989*	4014*	4017*	4020	4022*	4025	4027*	4030	4082*
4085	4091*	4094*	4097	4099*	4102	4161*	4164	4166*	4169	4214*	4217	4219*
4222	4267*	4270	4272*	4275	4320*	4323	4325*	4328	4373*	4376	4378*	4381
4426*	4429	4431*	4434	4480*	4483	4485*	4488	4541*	4544	4546*	4549	4551*
4554	4595*	4598	4601*	4604	4650*	4653*	4656*	4659	4661*	4664	4711*	4714
4719*	4722	4724*	4727	4774*	4777*	4780	4783*	4786	4788*	4791*	4796	4843*
4846*	4849*	4852*	4855*	4857*	4860*	4865	4901*	4904*	4907*	4910	4912*	4915
4949*	4952*	4955*	4958	4960*	4963	5002*	5005*	5008	5010*	5013	5069*	5072
5074*	5077*	5080*	5083	5085*	5088	5091*	5134*	5137	5157*	5160*	5163*	5166*
5169	5192*	5195	5221*	5224	5226*	5229	5234*	5237	5239*	5242	5288*	5306
5324*	5330	5345	5350*	5380*	5383	5385*	5388*	5391*	5394	5396*	5399	5449*
5452*	5454*	5457	5460*	5489*	5492	5494	5496*	5499	5539*	5545*	5547	5549*
5552*	5596*	5602	5604	5609*	5609	5653*	5659	5661	5663*	5666	5710*	5716
5718	5720*	5723	5767*	5773	5775	5777*	5780	5824*	5830	5832	5834*	5837
5895*	5898	5900	5902*	5905*	5908*	5911*	5914	5916*	5919	5980*	5983	5985*
5988	5989*	5993	6076*	6082	6109	6187*	6193	6220*	6222*	6298*	6304	6409*
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\$GTSWR 026414												
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\$HIOTS 001000												
\$HIOT 026342												
\$ICNT 001104												
\$ILLUP 030010												
\$INLP 033514												
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78	79											
259#												
7852*	7857#											
277#	6988#	7039*	7085*	7141*	7188*	7238*	7281*	7340*	7383*	7444*	7805*	7806
7808*	7819											
8137	8153	8170#										
759	761	763	765	767	769	807	846	891	930	967	1006	1026
1061	1081	1116	1136	1171	1191	1226	1246	1281	1301	1336	1356	1391
1411	1446	1466	1501	1521	1556	1576	1611	1631	1666	1686	1721	1741
1776	1796	1831	1851	1886	1906	1941	1961	1996	2016	2051	2071	2106
2126	2161	2181	2216	2236	2271	2291	2326	2346	2381	2401	2436	2456
2491	2511	2548	2568	2604	2624	2660	2680	2716	2736	2772	2792	2828
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3216	3236	3271	3291	3326	3346	3381	3401	3436	3456	3503	3550	3600
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4051	4099	4106	4123	4175	4181	4228	4234	4281	4287	4334	4340	4387
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4730	4768	4788	4796	4837	4857	4865	4912	4917	4960	4965	5010	5015
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$GTSWR 026414
$HD = 000001
$HIOTS 001000
$HIOT 026342
$ICNT 001104

$ILLUP 030010
$INLP 033514

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	6178	6192	6211	6220	6273	6284	6289	6303	6322	6331	6384	6395	6400
	6414	6433	6442	6497	6509	6514	6529	6550	6558	6611	6623	6628	6643
	6664	6672	6725	6737	6742	6757	6778	6786	6839	6851	6856	6871	6892
	6900	7013	7015	7117	7123	7206	7221	7308	7322	7414	7426	8796#	8859
	8933	8985	8992										
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SITEMB	001114	281#	7617*	7625	7642	7653							
SLF	001200	312#	7642	7982	7991	8076							
SLFLG	027645	8120*	8126#										
SLOAD	032700	8451	8579#										
SLPADR	001106	278#	650*	752*	7796*	7812*	7817	7819					
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SLPW	033322	8630	8634	8639	8643	8662	8665	8682	8699	8715#			
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SMADR3	001244	352#											
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SMAMS1	001232	339#											
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SMFLG	027644	8080*	8086	8121*	8125#								
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SMSGAD	001216	325#	8096*	8099									
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SNULL	001154	299#	8047	8076									
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		987	1040#	1042	1095#	1097	1150#	1152	1205#	1207	1260#	1262	1315#
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		2085#	2087	2140#	2142	2195#	2197	2250#	2252	2305#	2307	2360#	2362
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\$OFS = 033556  
\$OMODE 025212  
\$OUTLP 033416

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1904	1939	1959	1994	2014	2049	2069	2104	2124	2159	2179	2214	2234		
2269	2289	2324	2344	2379	2399	2434	2454	2489	2509	2546	2566	2602		
2622	2658	2678	2714	2734	2770	2790	2826	2846	2882	2902	2938	2958		
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3344	3379	3399	3434	3454	3496	3498	3542	3548	3588	3598	3642	3644		
3685	3693	3735	3743	3781	3788	3827	3832	3853	3876	3878	3885	3890		
3944	3946	3954	3962	4017	4020	4025	4030	4085	4094	4097	4102	4164		
4166	4169	4217	4219	4222	4270	4272	4275	4323	4325	4328	4376	4378		
4381	4429	4431	4434	4483	4485	4488	4544	4546	4549	4554	4598	4601		
4604	4609	4653	4656	4659	4664	4714	4722	4727	4777	4780	4783	4786		
4791	4846	4849	4852	4855	4860	4904	4907	4910	4915	4952	4955	4958		
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5166	5169	5195	5224	5229	5237	5242	5295	5299	5306	5312	5315	5324		
5383	5385	5388	5391	5394	5399	5452	5454	5457	5492	5494	5496	5499		
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5718	5720	5723	5773	5775	5777	5780	5830	5832	5834	5837	5898	5900		
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6054	6065	6103	6153	6155	6157	6160	6165	6176	6214	6264	6266	6268		
6271	6276	6287	6325	6375	6377	6379	6382	6387	6398	6436	6488	6490		
6492	6495	6500	6503	6512	6553	6602	6604	6606	6609	6614	6617	6626		
6667	6716	6718	6720	6723	6728	6731	6740	6781	6830	6832	6834	6837		
6842	6845	6854	6895	6999	7001	7018	7021	7096	7098	7111	7115	7120		
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7773	7789	7797	7807	7816#										
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7349*	7384*	7453*	7803	7820										
262#														
8168	8173#													
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645	8137#	8165												
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310#	7642	7926	7975	7991	8076									
7939#	8216													
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5458	8856#	8866												
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\$PASTM 001006  
\$POWER 030016  
\$PUTS 034166  
\$PWRDN 027650  
\$PWARMG 030004  
\$PWRUP 027722  
\$QUES 001176  
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\$RDLIN 026746  
\$RDOCT 026242  
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\$REGAD 001160  
\$REGO 001162  
\$RESET 033650  
\$RTNAD 023356  
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\$SAD 033644  
\$SAVRE= \*\*\*\*\* U  
\$SAVR6 030014  
\$SCOPE 025762

\$SETUP= 000117  
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\$SVPC = 000234  
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7781	241											
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1931	2706	2762	2818	2874	2930	2986	3041	3096	3151	3206	3261	3316
2650	3426	3487	3532	3582	3633	3679	3729	3777	3820	3870	3934	4012
3371	4156	4209	4262	4315	4368	4421	4475	4532	4587	4641	4705	4764
4080	4895	4943	4995	5053	5151	5219	5286	5370	5444	5482	5536	5593
4833	5707	5764	5821	5879	5969	6031	6142	6253	6364	6476	6590	6704
5650	6924	6932	6944	6950	6952	7598	7599	7600	7601	7602	7611	7618
6818	7634	7642	7762	7763	7764	7765	7766	7772	7784	7786	7787	7790
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296#	7861	7870	7886	7910#	7941	7947	8923					
295#	8811											
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8627#	3941#	3944	3951#	3954	3959#	3962	4106	4606#	4609	5292#	5295	5296#
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7015#	7201	7203#	7206#	7209	7289#	7292	7294	7296#	7299	7301#	7304	7308
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1326#	1711#	1755	1766#	1810	1821#	1865	1876#	1920	1931#	1975	1986#	2030
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2041#	2426#	2470	2481#	2527	2538#	2583	2594#	2639	2650#	2695	2706#	2751
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\$TMPO 001164  
\$TN = 000147





ENDCOM

ERROR

ESCAPE  
GETPRI  
GETSWR  
MOVE I

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1892	1898	1912	1918	1947	1953	1967	1973	2002	2008	2022	2028	2057	2063	2077
2083	2112	2118	2132	2138	2167	2173	2187	2193	2222	2228	2242	2248	2277	2283
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2503	2517	2523	2554	2560	2574	2580	2610	2616	2630	2636	2666	2672	2686	2692
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2910	2946	2966	3002	3022	3057	3077	3112	3132	3167	3187	3222	3242	3277	3297
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2324	2344	2379	2399	2434	2454	2489	2509	2546	2566	2602	2622	2658	2678	2714
2734	2770	2790	2826	2846	2882	2902	2938	2958	2994	3014	3049	3069	3104	3124
3159	3179	3214	3234	3269	3289	3324	3344	3379	3399	3434	3454	3501	3548	3598
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4104	4120	4173	4179	4226	4232	4279	4285	4332	4338	4385	4391	4438	4444	4493
4498	4538	4557	4604	4609	4659	4664	4707	4722	4728	4766	4786	4794	4835	4855
4863	4910	4915	4958	4963	5008	5013	5083	5093	5114	5173	5177	5232	5237	5242
5319	5327	5394	5399	5415	5462	5505	5558	5563	5615	5620	5672	5677	5729	5734

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MOVEM	7204	7219	7306	7320	7411	7424	8857								
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	1222	1242	1277	1297	1332	1352	1387	1407	1442	1462	1497	1517	1552	1572	1607
	1627	1662	1682	1717	1737	1772	1792	1827	1847	1882	1902	1937	1957	1992	2012
	2047	2067	2102	2122	2157	2177	2212	2232	2267	2287	2322	2342	2377	2397	2432
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	3683	3691	3733	3741	3779	3786	3825	3830	3851	3874	3876	3893	3888	3942	3944
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	4220	4268	4270	4273	4321	4323	4326	4374	4376	4379	4427	4429	4432	4481	4483
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	4725	4775	4778	4781	4784	4789	4844	4847	4850	4853	4858	4902	4905	4908	4913
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	5161	5164	5167	5193	5222	5227	5235	5240	5293	5297	5304	5310	5313	5322	5381
	5383	5386	5389	5392	5397	5450	5452	5455	5490	5492	5494	5497	5543	5545	5547
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	5775	5778	5828	5830	5832	5835	5896	5898	5900	5903	5906	5909	5912	5917	5978
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POPSP2	226#														
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	2315	2370	2425	2480	2537	2593	2649	2705	2761	2817	2873	2929	2985	3040	3095
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.SCATC	30#	90
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.SINLP	28#	8781
.SMMAC	18#	
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.SRDOC	30#	7820
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ASL	7906	8033	8093	8105	8117	8841	8861	8991							
ASLB	7661	7662	7663	7841	7843	7845	7920	7921	7922	8188					
ASR	7726														
BCC	8100														
BEQ	7727														
	670	847	1007	1027	1062	1082	1117	1137	1172	1192	1227	1247	1282	1302	1337
	1357	1392	1412	1447	1467	1502	1522	1557	1577	1612	1632	1667	1687	1722	1742
	1777	1797	1832	1852	1887	1907	1942	1962	1997	2017	2052	2072	2107	2127	2162
	2182	2217	2237	2272	2292	2327	2347	2382	2402	2437	2457	2492	2512	2549	2569
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	3017	3052	3072	3107	3127	3162	3182	3217	3237	3272	3292	3327	3347	3382	3402
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	4560	4667	4797	4866	5016	5096	5119	5331	5346	5349	5419	5466	5508	5994	6083
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	8467	8492	8513	8541	8598	8718	8724	8760	8762	8802	8805	8835	8931		
BGE	7807														
BGT	6937	7577	7735	7916	7957										
BHI	7793														
BIC	6934	7567	7847	7873	7890	7917	7944	7950	7958						
BICB	8927														
BIS	3829	3887	3959	4027	4099	4606	4661	4724	4788	4857	4912	4960	5010	5085	5234
	5239	5321	5396	5916	5985	6051	6062	6100	6162	6173	6211	6273	6284	6322	6384
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BISB	7653	8996	8997	8998											
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BLOS	7970														
BLT	7578	7718	7734	7914	7955	8050									
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	8494	8496	8523	8539	8566	8590	8596	8680	8697	8720	8726	8860	8892	8897	
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	3010	3732	3778	3850	3873	3936	3941	4014	4082	4161	4169	4214	4222	4267	4275
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	7111	7884	7885	8155	8450	8459	8545	8582	8583	8587	8591	8599	8716	8758	8776
	7838	8821	8837	8890	8893	8917									
	8800	7798	7981	8042	8068	8119	8120	8121							
CLRB	7741	635	696	1006	1061	1116	1171	1226	1281	1336	1391	1446	1501	1556	1611
CMP	635	658	696	1006	1061	1116	1171	1226	1281	1336	1391	1446	1501	1556	1611
	1666	1721	1776	1831	1886	1941	1996	2051	2106	2161	2216	2271	2326	2381	2436
	2491	2548	2604	2660	2716	2772	2828	2884	2940	2996	3051	3106	3161	3216	3271
	3326	3381	3436	3551	3601	3698	3748	3894	3969	4123	4096	4865	5095	5116	5417
	5993	6082	6109	6193	6220	6304	6331	6415	6442	6530	6558	6644	6672	6758	6786
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	7954	7956	7969	8448	8512	8589	8595	8597	8761	8804	8834				
CMPB	5330	7623	7788	7792	7876	7908	7973	7979	8020	8035	8037	8045	8066	8070	8088
	8484	8486	8491	8538	8565	8717	8930								
DEC	6103	6214	6325	6436	6935	7660	8902								
DECB	7565	7576	8049	8052											
EMT	113														
HALT	96	7500	7632	8016	8148	8170	8611	8738							
INC	694	704	3963	4170	4223	4276	4329	4382	4435	4485	4490	4546	5312	5324	5391
	5496	5554	5611	5668	5725	5782	5839	5908	6073	6184	6295	6406	6500	6521	6553
	6614	6635	6667	6728	6749	6781	6842	6863	6895	6933	7039	7048	7141	7150	7238
	7247	7340	7349	7444	7453	7571	7579	7614	7719	7805	7923	8118	8156	8442	8460
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IOT	114							6950							
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JSR	759	761	763	765	767	769	805								
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	1389	1391	1409	1411	1444	1446	1464	1466	1499	1501	1519	1521	1554	1556	1574
	1576	1609	1611	1629	1631	1664	1666	1684	1686	1719	1721	1739	1741	1774	1776
	1794	1796	1829	1831	1849	1851	1884	1886	1904	1906	1939	1941	1959	1961	1994
	1996	2014	2016	2049	2051	2069	2071	2104	2106	2124	2126	2159	2161	2179	2181
	2214	2216	2234	2236	2269	2271	2289	2291	2324	2326	2344	2346	2379	2381	2399
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	4030	4034	4051	4085	4094	4097	4099	4102	4106	4123	4164	4166	4169	4175	4181
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DRLPG.P11

## CROSS REFERENCE TABLE

MOV

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8933	8950	8985	8992											
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657	662	664	665	666	671	681	682	689	690	691	692	695	699	700
706	708	710	712	714	716	718	720	722	724	726	727	728	729	751
752	797	802	837	882	884	921	923	958	960	996	1001	1051	1056	1106
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NEG NOP RESET	6944 7558 663 7679 8898	8999 5350 8208 807 1521	6946 7469 8209 846 1631	6947 7486 8210 891 1686	6948 7616 8211 930 1741	7717 8099 8213 967 1796	8099 8215 1026 1851 1906	7842 7844 7846 7911 7959	7844 7818 7856 7911 7959	7846 7846 7846 7911 7959	7846 7846 7846 7911 7959	7846 7846 7846 7911 7959	8034 8169 8818 8842	8197 8868	8903 8895	
ROL RTI RTS	8989 3989 8199 673	8999 5350 8208 807 1521	7469 8209 846 1631	7486 8210 891 1686	7616 8211 930 1741	7717 8099 8213 967 1796	8099 8215 1026 1851 1906	7842 7844 7846 7911 7959	7844 7818 7856 7911 7959	7846 7846 7846 7911 7959	7846 7846 7846 7911 7959	7846 7846 7846 7911 7959	8034 8169 8818 8842	8197 8868	8903 8895	
SUB TRAP TST	3181 4440 5560 7123 8094	3236 4495 5617 7569 8112	3291 4540 5674 7630 8114	3346 4559 5731 7637 8186	3401 4666 5788 7683 8608	3456 4709 5845 7722 8759	3503 4768 5921 7732 8767	3649 4837 6067 7779 8801	3792 4917 6178 7803 8810	3984 4965 6289 7850 8859	4175 5015 6400 7903 8886	4228 5175 6514 7918 8891	4281 5244 6628 8031 8891	4281 5244 6628 8031 8891	4334 5464 6742 8039 8895	4387 5507 6856 8061 8895
TSTB	5179 7870 310 309	5345 7886 311 312	5401 7941 8337 679	5565 7947 8337 6953	5622 8014 8337 7046	5679 8063 8337 7053	5736 8086 8337 7148	5793 8097 8337 7155	5850 8110 8337 7245	7221 8540 8337 7252	7322 8923 8337 7347	7426 8923 8337 7354	7426 8923 8337 7451	7724 8923 8337 7458	7738 8923 8337 7473	
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.DSABL .ENABL .END .ENDC	8126 7928 30 9003 73	8127 7928 7861 86	351 353 88	353 353 89	354 354 90	6952 7587 99	7587 7587 113	7588 7588 205	7589 7589 219	7590 7590 235	7627 7627 239	7628 7628 241	7988 7988 246	7989 7989 248	8125 8125 255	
	269 356 371 643 753 837 904 958 1018 1084 1142 1200 1258 1316 1372	273 357 372 645 772 838 911 959 1029 1087 1145 1203 1261 1317 1379	275 358 373 647 773 850 912 971 1032 1090 1148 1206 1262 1324 1380	303 359 374 648 795 853 919 974 1035 1093 1151 1207 1269 1325 1381	306 360 375 650 796 856 920 978 1038 1096 1152 1214 1270 1326 1382	307 361 376 652 797 859 921 981 1041 1097 1159 1215 1271 1327 1394	308 362 377 673 798 863 922 986 1042 1104 1160 1216 1272 1329 1397	309 363 378 679 812 864 934 987 1049 1105 1161 1217 1284 1342 1400	310 364 382 701 815 880 937 994 1050 1106 1162 1217 1287 1345 1403	314 365 402 739 818 881 941 995 1051 1107 1162 1229 1290 1348 1414	317 366 623 740 821 882 944 996 1052 1119 1177 1235 1293 1359 1417	339 367 629 749 824 883 949 997 1064 1122 1180 1238 1304 1362 1420	347 368 637 750 825 894 950 996 1067 1125 1183 1249 1307 1365 1423	350 369 638 751 835 897 956 996 1070 1128 1189 1252 1310 1368 1426	353 370 641 752 836 901 957 996 1073 1139 1197 1255 1313 1371 1427	

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CROSS REFERENCE TABLE

SEQ 0271

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ERRORS DETECTED: 0

G06

MAINDEC-11-DRLPG-A  
DRLPG.P11

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SEQ 0278

\*DRLPG,DRLPG/SOL/CRF=DRLPA.MAC,DRLPG  
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