M9301-YH

ROM BOOTSTRAP/TEST PROG

MD-11-DQM9A-A

EPDQM9A-A

FICHE 1 OF 1

JUN 1977

digital

MADE IN USA

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TABLE OF CONTENTS

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IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DQM9A-A-D
PRODUCT NAME:	PDP11/60,PDP11/70 ROM BOOTSTRAP/TEST PROGRAM
PROGRAM DATE:	JANUARY 1977
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	JIM KAPADIA

TABLE OF CONTENTS

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                                1.0  ABSTRACT

                THE M9301-Y-H IS DESIGNED TO PROVIDE BOOT STRAPPING CAPABILITIES
                FOR THE PDP 11/60 AND PDP 11/70 COMPUTERS.  IN ADDITION TO THAT
                THE M9301-Y-H ALSO INCLUDES ROUTINES THAT PROVIDE BASIC
                TESTS FOR THE CPU, MEMORY AND THE CACHE.

                THE BOOOTSTRAP/TEST PROGRAM HAS BEEN DESIGNED FOR FLEXIBILITY
                OF OPERATION.  ITS FUNCTIONS MAY BE INITIATED AUTOMATICALLY
                ON POWER-UP, OR BY DEPRESSING THE CONSOLE "BOOT" SWITCH
                OR BY A LOAD ADDRESS AND START SEQUENCE.

                A SET OF MICRO-SWITCHES ARE LOCATED ON THE M9301 MODULE.
                THEY ARE USED BY THE ROUTINES TO DETERMINE WHAT ACTION
                IS TO BE TAKEN.

                2.0  DEVICES SUPPORTED

                        1.  RK11/RK05 DISK
                        2.  RK611/RK06 DISK
                        3.  TC11/TU56 DECTAPE
                        4.  TM11/TU10 MAGTAPE
                        5.  RP11/RP03 DISK
                        6.  RH11/RP04 DISK
                        7.  RH11/TU16 MAGTAPE (800 BPI,NRZI)
                        8.  RH11/RS04 FIXED HEAD DISK
                        9.  RX11/RX01 DISKETTE
                        10. PC11 HIGH SPEED READER


                3.0  INITIATION

                THE BOOTSTRAP TEST PROGRAM CAN BE INITIATED IN ONE OF
                THE FOLLOWING WAYS:

                        1.  AUTOMATICALLY ON POWER UP
                        2.  DEPRESSING "BOOT" SWITCH ON THE CONSOLE
                        3.  LOAD ADDRESS AND START SEQUENCE FROM THE CONSOLE

                3.1  POWER-UP START

                3.1.1  PDP 11/6X

                ON THE PDP 11/6X THERE IS A THREE-POSITION SLIDE SWITCH
                (BOOT/RUN/HALT) ON THE CONSOLE.  IF THIS SWITCH IS LEFT
                IN THE "BOOT" POSITION AND POWER-UP OCCURS, AN AUTOMATIC
                BOOTING WILL OCCUR FROM THE PERIPHERAL SPECIFIED IN
                THE MICRO-SWITCHES (SEE SEC. 5.0).  UNIT 0 OF THE DEVICE
                WILL BE BOOTED.  THE TEST ROUTINES WILL BE EXECUTED
                PRIOR TO BOOTING DEPENDING ON THE SETTING OF MICRO-
                SWITCHES, SEE SEC. 5.0.

                3.1.2  PDP 11/70

                IF MICRO-SWITCH 1 ON THE M9301 MODULE IS ON, THEN
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AUTOMATIC BOOTSTRAPPING WILL OCCUR ON POWER UP.
THE BOOTING WILL BE DONE FROM THE DEVICE SPECIFIED
IN THE MICRO-SWITCHES. SEE SEC 5.0.

3.2 "BOOT" SWITCH

WHEN THE BOOT SWITCH ON THE CONSOLE IS DEPRESSED,
BOOTING WILL OCCUR FROM THE PERIPHERAL SELECTED IN
THE MICRO-SWITCHES, UNIT 0 WILL BE USED. THE TEST
ROUTINES WILL BE EXECUTED DEPENDING ON THE SETTING OF
MICRO-SWITCHES, SEE SEC. 5.0.

3.3 CONSOLE

THIS MODE OF OPERATION ALLOWS THE USER TO BOOT FROM
ANY DEVICE, ANY UNIT NUMBER; (INDICATED
IN THE CONSOLE SWITCH REGISTER). IF THE CONSOLE SWITCH REGISTER
IS CLEAR (ONLY THE LOW BYTE NEED TO BE CLEARED), THEN
THE BOOOTING WILL OCCUR FROM THE DEFAULT DEVICE SPECIFIED
IN THE MICRO-SWITCHES (SEE SEC 5.0). UNIT 0 OF THE
DEFAULT DEVICE WILL BE USED.

ON THE 11/6X, LOAD ADDRESS 773000.
ON THE 11/70, LOAD ADDRESS 17773000.

IF THE BOOTING IS TO BE DONE FROM THE DEFAULT DEVICE
SPECIFIED IN THE MICRO-SWITCHES, THEN CLEAR THE LO-BYTE
OF THE SWITCH REGISTER AND PRESS START.

IF THE BOOTING IS TO BE DONE FROM ANY DEVICE, THEN
SWREG<2=0> SHOULD CONTAIN THE DRIVE NUMBER AND
SWREG<6=3> SHOULD CONTAIN THE DEVICE CODE (SEE SEC 5.0).

AS BEFORE, THE DIAGNOSTIC TESTS WILL BE EXECUTED
(PRIOR TO BOOTING) DEPENDING ON THE POSITION OF
MICRO-SWITCHES, SEE SEC. 5.0.

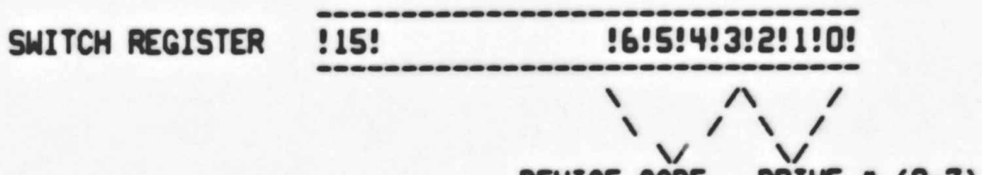
4.0 SWITCH REGISTER--DEVICE CODES, UNIT NUMBER

WHEN THE "LOAD ADDRESS, START" SEQUENCE DESCRIBED IN
SEC. 3.3 IS USED TO INITIATE THE BOOTSTRAP, THE
BOOTING WILL OCCUR EITHER FROM THE DEFAULT
DEVICE SPECIFIED IN THE MICRO-SWITCHES OR THE DEVICE,
UNIT SPECIFIED IN THE SWITCH REGISTER. THE PROCEDURE
IS TO LOAD ADDRESS, THEN LOAD THE SWITCH REGISTER PROPERLY
(SEE TABLE BELOW) AND PRESS START. (CONTROL, START FOR 11/60).

STARTING ADDRESS	
17773000	PDP 11/70
773000	PDP 11/6X

SWREG (LO BYTE)	FUNCTION
0	BOOT FROM DEFAULT DEVICE, DRIVE 0
NON-ZERO	BOOT FROM DEVICE AND DRIVE NUMBER

SPECIFIED IN THE SWITCH REGISTER.



DEVICE CODE (SWREG<6=3>)	DEVICE
0	USE THE DEVICE SPECIFIED IN MICRO-SWITCHES
1	TM11/TU10
2	TC11/TU56
3	RK11/RK05
4	RP11/RP03
5	RK611/RK06
6	RH11/TU16
7	RH11/RP04
10	RH11/RS04
11	RX11/RX01
12	PC11

5.0 MICRO-SWITCHES ON M9301, OPTION SELECTION

THERE IS A FLAT-PACK CONTAINING TEN MICRO-SWITCHES ON THE M9301. DEPENDING ON THE SETTING OF THESE MICRO-SWITCHES THE PROGRAM AND THE MACHINE TAKE DIFFERENT ACTIONS. (THE MICRO-SWITCHES CAN BE ADDRESSED AT UBA XX773024).

MICRO-SWITCHES	DESCRIPTION
10	USED TO SELECT PROCESSOR TYPE IF OFF, THEN 11/70 IF ON, THEN 11/60
09	IF OFF, DO NOT EXECUTE ANY TEST ROUTINES (CPU,CACHE,MEMORY) IF ON, EXECUTE TEST ROUTINES (NOTE: SEE MICRO-SWITCH 3). SEE SEC 6.0.
08	IF OFF, THE ROM BOOT STRAP PROGRAM WILL NOT CHECK THE CONSOLE SW REG BEFORE BOOTING. IF ON, THE ROM BOOT STRAP PROGRAM WILL CHECK THE CONSOLE SW REG AND WILL BOOT ACCORDINGLY.
07-04	DEVICE CODE, FOR SELECTING THE DEVICE TO BOOT FROM (NORMAL DEVICE).

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                                        03              IF OFF, EXECUTE MEMORY-MODIFYING
                                                        TESTS BEFORE BOOTING (SEE SEC 6.0)
                                                        (JSR,RTS,RTI,MEMORY TESTS, CACHE TESTS)
                                                        NOTE:  THIS MICRO-SWITCH IS LOOKED AT,
                                                        ONLY IF 9 IS ON.

                                        02              SWITCH SHOULD BE OFF FOR 11/60
                                                        SWITCH SHOULD BE ON FOR 11/70 IF
                                                        BOOT ON POWER UP IS TO BE USED.

                                        01              IF OFF, THE LOW ROM (XXX65000-XXX65776)
                                                        IS DISABLED
                                                        IF ON, THE LOW ROM IS ENABLED
                                                        NORMAL POSITION OF SW 01 IS ON.

MICRO-SWITCH OPTION 8 IS PROVIDED TO PROTECT THE USER AGAINST
UNINTENTIONAL OR NON-AUTHORIZED SETTING OF THE CONSOLE SWITCH
REGISTER.  NORMALLY, ON POWER-UP (SUBSEQUENT TO POWER-FAIL)
BOOTING WILL BE DONE FROM THE DEVICE CODE SPECIFIED IN THE
MICRO-SWITCHES (ON M9301 MODULE), PROVIDED THE CONSOLE SWITCH
REGISTER IS CLEAR.  IF THE CONSOLE SWITCH REGISTER IS NOT CLEAR,
THE PROGRAM WILL USE THE CODE SPECIFIED IN THE SWITCH REGISTER
FOR SELECTING THE DEVICE TO BOOT FROM.  IF THE MICRO-SWITCH
IS LEFT IN THE OFF POSITION, THE BOOT STRAP PROGRAM WILL NOT
SENSE THE CONSOLE SWITCH REGISTER; THUS ELIMINATING THE POSSIBILITY
OF ATTEMPTING TO BOOT FROM AN UNDESIRED OR NON-EXISTENT PERIPHERAL
IN CASE CONSOLE SWITCH REGISTER IS SET RANDOMLY.

6.0  TEST ROUTINES IN M9301-YH

THE M9301-YH HAS TESTS TO CHECK OUT THE CPU (INSTRUCTIONS),
CACHE AND MEMORY (UP TO 28K).  THERE ARE TWO TYPES OF TESTS.

        1.  NON-MEMORY MODIFYING TESTS
        2.  MEMORY-MODIFYING TESTS

THE CPU INSTRUCTION TESTS ARE NON-MEMORY MODIFYING
AND ARE EXECUTED PRIOR TO BOOTING IF MICRO-SWITCH
9 IS ON.  SEE SEC 5.0.

THE MEMORY-MODIFYING TESTS CONSTITUTES THE TESTS
FOR RTS,RTI,JSR INSTRUCTIONS, TESTS FOR THE CACHE
AND THE TESTS FOR THE MEMORY.  THESE TESTS
ARE EXECUTED PRIOR TO BOOTING IF MICRO-SWITCHES
9 IS ON AND MICRO-SWITCH 3 IS OFF.  SEE SEC. 5.0.

6.1  CPU TESTS

THIS SECTION CONSISTS OF SEVERAL SUB-TESTS
WHICH CHECK THE CPU DATA PATH AND CONTROL LOGIC
USING VARIOUS INSTRUCTIONS.

6.2  MAIN MEMORY TEST

THIS TEST CHECKS OUT THE MAIN MEMORY (UP TO 28K),
WITH THE CACHE DISABLED.  PARITY ERROR VECTOR HAS BEEN
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SET UP, HENCE PARITY ERRORS IF FOUND WILL BE DETECTED.

6.3 CACHE TEST

THIS SECTION HAS TESTS TO CHECK THE CACHE. THE TEST
CHECKS IF THE CACHE HITS CAN BE OBTAINED ALL THE WAY
THROUGH THE MEMORY. ALSO, THE DATA MEMORY OF THE CACHE
IS CHECKED. DIFFERENT TEST PARAMETERS ARE USED (WHERE NEEDED)
TO TEST THE PDP 11/60 AND THE PDP 11/70 CACHE.

7.0 ERROR RECOVERY AND RETRY:

7.1 ERRORS DURING BOOTING

IF A DEVICE ERROR IS DETECTED, WHILE TRYING TO BOOT,
A "RESET" WILL BE ISSUED AND THE BOOTSTRAP WILL TRY
AGAIN. THIS WOULD ALLOW DEVICES TO COME ON-LINE
(INTO LOAD POSITION) AFTER A POWER-UP SUBSEQUENT TO
POWER-FAIL.

7.2 ERRORS DURING TESTING

IF AN ERROR IS DETECTED DURING THE EXECUTION OF THE
TEST ROUTINES THE PROCESSOR WILL HALT, INDICATING TO
THE USER THAT A MALFUNCTION HAS BEEN DETECTED. THE
CONSOLE LIGHTS WILL INDICATE THE "PC" AT WHICH THE
"HALT" OCCURRED. MORE INFORMATION ABOUT THE FAILURE
CAN BE OBTAINED BY REFERENCING THE BOOTSTRAP/TEST
LISTINGS AT THE ERROR "PC".

IF AN ERROR OCCURS IN CACHE TESTS, THE USER HAS AN
OPTION TO CONTINUE AND BOOT BY PRESSING THE "CONTINUE"
SWITCH ON THE CONSOLE. HOWEVER, IN THE ABOVE CASE
CACHE MISSES WILL BE FORCED, TO PREVENT FURTHER
ERRORS FROM CACHE.
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                        165000                  . = BASE1
                                        ;:**********************************************************************
                                                .SBTTL  TEST1   THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
                                        ;*
                                        ;*      THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
                                        ;*      THIS TEST IS ENTERED AND THEY SHOULD REMAIN THAT WAY UPON
                                        ;*      THE COMPLETION OF THIS TEST.
                                        ;*
                                        ;:**********************************************************************
165000                                  TST1:

165000                                  DIAG:

165000  000401                                BR      TST2            ; * BRANCH ALWAYS
165002  000000                                HALT

                                        ;:**********************************************************************
                                                .SBTTL  TEST2   TEST "CLR", MODE "0", AND "BMI","BVS","BHI","BLOS"
                                        ;*
                                        ;*      THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN
                                        ;*      THIS TEST IS ENTERED.  UPON COMPLETION OF THIS TEST THE "SP"
                                        ;*      (R6) SHOULD BE ZERO AND ONLY THE "Z" FLIP-FLOP WILL BE SET.
                                        ;*
                                        ;:**********************************************************************
165004                                  TST2:

165004  005006                                CLR     SP              ;N=0,Z=1,V=0,C=0,SP=000000
165006  100403                                BMI     1$              ; V BRANCH IF N=1
165010  102402                                BVS     1$              ; V BRANCH IF V=1
165012  101001                                BHI     1$              ; V BRANCH IF Z AND C ARE BOTH 0
165014  101401                                BLOS    TST3            ; * BRANCH IF (Z XOR C)=1
165016  000000                          1$:   HALT

                                        ;:**********************************************************************
                                                .SBTTL  TEST3   TEST "DEC", MODE "0", AND "BPL","BEQ","BGE","BGT","BLE"
                                        ;*
                                        ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                        ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                                        ;*      R3 = ? R4 = ? R5 = ? SP = 000000
                                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                                        ;*      N = 1, Z = 0, V = 0, AND C = 0
                                        ;*      THE REGISTERS AFFECTED BY THE TEST ARE:
                                        ;*      SP = 177777
                                        ;*
                                        ;:**********************************************************************
165020                                  TST3:

165020  005306                                DEC     SP              ;N=1,Z=0,V=0,C=0,SP=177777
165022  100004                                BPL     1$              ; V BRANCH IF N=0
165024  001403                                BEQ     1$              ; V BRANCH IF Z=1
165026  002002                                BGE     1$              ; V BRANCH IF (N XOR V)=0
165030  003001                                BGT     1$              ; V BRANCH IF Z AND (N XOR V) ARE BOTH 0
165032  003401                                BLE     TST4            ; * BRANCH IF [Z OR (N XOR V)]=1
165034  000000                          1$:   HALT
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                                ;:*****************************************************************************
                                        .SBTTL  TEST4   TEST "ROR", MODE "0", AND "BVC","BHIS","BHI","BNE"
                                ;*
                                ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 1, Z = 0, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                                ;*      R3 = ? R4 = ? R5 = ? SP = 177777
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                                ;*      N = 0, Z = 0, V = 1, AND C = 1
                                ;*      THE REGISTERS AFFECTED BY THE TEST ARE:
                                ;*      SP = 077777
                                ;*
                                ;:*****************************************************************************
165036                          TST4:
165036  006006                        ROR     SP              ;N=0,Z=0,V=1,C=1,SP=077777
165040  102003                        BVC     1$              ; V BRANCH IF V=0
165042  103002                        BHIS    1$              ; V BRANCH IF C=0
165044  101001                        BHI     1$              ; V BRANCH IF C AND Z ARE BOTH 0
165046  001001                        BNE     TST5            ; * BRANCH IF Z=0
165050  000000                1$:     HALT
                                ;:*****************************************************************************
                                        .SBTTL  TEST5   TEST "BHI", "BLT", AND "BLOS"
                                ;*
                                ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 0, V = 1, AND C = 1.
                                ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                                ;*      R3 = ? R4 = ? R5 = ? SP = 077777
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                                ;*      N = 1, Z = 1, V = 1, AND C = 1
                                ;*      THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.
                                ;*
                                ;:*****************************************************************************
165052                          TST5:
165052  000264                        SEZ                     ;N=0,Z=1,V=1,C=1
165054  101003                        BHI     1$              ; V BRANCH IF Z AND C ARE BOTH 0
165056  000270                        SEN                     ;N=1,Z=1,V=1,C=1
165060  002401                        BLT     1$              ; V BRANCH IF (N XOR V)=1
165062  101401                        BLOS    TST6            ; * BRANCH IF (Z OR C)=1
165064  000000                1$:     HALT                    ;STOP HERE IF A BRANCH FAILED
                                ;:*****************************************************************************
                                        .SBTTL  TEST6   TEST "BLE" AND "BGT"
                                ;*
                                ;*      UPON ENTERING THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 1, Z = 1, V = 1, AND C = 1.
                                ;*      THE REGISTERS ARE: R0 = ?, R1 = ? R2 = ?
                                ;*      R3 = ? R4 = ? R5 = ? SP = 077777
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:
                                ;*      N = 1, Z = 0, V = 1, AND C = 1
                                ;*      THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.
                                ;*
                                ;:*****************************************************************************
165066                          TST6:
165066  000244                        CLZ                     ;N=1,Z=0,V=1,C=1
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                                TEST6   TEST "BLE" AND "BGT"

452  165070  003401                     BLE     1$                 ; V BRANCH IF [Z OR (N XOR V)]=1
453  165072  003001                     BGT     TST7               ; * BRANCH IF Z AND (N XOR V) ARE BOTH 0
454  165074  000000              1$:    HALT                       ;STOP HERE IF A BRANCH FAILED
455
456                             ;;*****************************************************************************
457                                     .SBTTL  TEST7   TEST REGISTER DATA PATH
458                             ;*
459                             ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
460                             ;*      N = 1, Z = 0, V = 1, AND C = 1.
461                             ;*      THE REGISTERS ARE: R0 = ?, R1 = ?, R2 = ?
462                             ;*      R3 = ?, R4 = ?, R5 = ?, SP = 077777.
463                             ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
464                             ;*      N = 0, Z = 1, V = 0, AND C = 0.
465                             ;*      THE REGISTERS ARE LEFT AS FOLLOWS:
466                             ;*      R0 = 125252, R1 = 000000, R2 = 125252, R3 = 125252
467                             ;*      R4 = 125252, R5 = 125252, AND SP = 125252
468                             ;*
469                             ;;*****************************************************************************
470  165076                     TST7:
471  165076  012706  125252             MOV     #125252,SP         ;N=1,Z=0,V=0,C=1,SP=125252
472  165102  010600                     MOV     SP,R0              ;N=1,Z=0,V=0,C=1,R0=125252
473  165104  010001                     MOV     R0,R1              ;N=1,Z=0,V=0,C=1,R1=125252
474  165106  010102                     MOV     R1,R2              ;N=1,Z=0,V=0,C=1,R2=125252
475  165110  010203                     MOV     R2,R3              ;N=1,Z=0,V=0,C=1,R3=125252
476  165112  010304                     MOV     R3,R4              ;N=1,Z=0,V=0,C=1,R4=125252
477  165114  010405                     MOV     R4,R5              ;N=1,Z=0,V=0,C=1,R5=125252
478  165116  160501                     SUB     R5,R1              ;N=0,Z=1,V=0,C=0, AND R1=000000
479  165120  002401                     BLT     1$                 ; V BRANCH IF (N XOR V)=1
480  165122  001401                     BEQ     TST10              ; * BRANCH IF Z=1
481  165124  000000              1$:    HALT
482
483                             ;;*****************************************************************************
484                                     .SBTTL  TEST10  TEST "ROL", "BCC", "BLT"
485                             ;*
486                             ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
487                             ;*      N = 0, Z = 1, V = 0, AND C = 0.
488                             ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252
489                             ;*      R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
490                             ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
491                             ;*      N = 0, Z = 0, V = 1, AND C = 1.
492                             ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
493                             ;*      R2 WHICH SHOULD NOW EQUAL 052524.
494                             ;*
495                             ;;*****************************************************************************
496  165126                     TST10:
497  165126  006102                     ROL     R2                 ;N=0,Z=0,V=1,C=1, AND R2 = 052524
498  165130  103001                     BCC     1$                 ; V BRANCH IF C=0
499  165132  002401                     BLT     TST11              ; * BRANCH IF (N XOR V)=1
500  165134  000000              1$:    HALT
501
502                             ;;*****************************************************************************
503                                     .SBTTL  TEST11  TEST "ADD", "INC", "COM", AND "BCS", "BLE"
504                             ;*
505                             ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
506                             ;*      N = 0, Z = 0, V = 1, AND C = 1.
507                             ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524
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                                TEST11  TEST "ADD", "INC", "COM", AND "BCS", "BLE"

                        ;*      R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R3 WHICH NOW EQUALS 000000, AND R1 WHICH IS ALSO 000000
                        ;*
                        ;;**************************************************************************
165136                  TST11:
                                                        ;(R2 = 052524) + (R3 = 125252)
165136  060203                  ADD     R2,R3           ;N=1,Z=0,V=0,C=0, AND R3=177776
165140  005203                  INC     R3              ;N=1,Z=0,V=0,C=0, AND R3=177777
165142  005103                  COM     R3              ;N=0,Z=1,V=0,C=1, AND R3 = 000000
165144  060301                  ADD     R3,R1           ;N=0,Z=1,V=0,C=0, AND R1 = 000000
165146  103401                  BCS     1$              ; V BRANCH IF C=1
165150  003401                  BLE     TST12           ; * BRANCH IF [Z OR (N XOR V)]=1
165152  000000          1$:     HALT

                        ;;**************************************************************************
                                .SBTTL  TEST12  TEST "ROR", "BIS", "ADD", AND "BLO", "BGE"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524
                        ;*      R3 = 000000, R4 = 125252, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R3 WHICH SHOULD BE MODIFIED BACK TO 000000, AND
                        ;*      R4 WHICH SHOULD NOW EQUAL 052525
                        ;*
                        ;;**************************************************************************
165154                  TST12:
165154  006004                  ROR     R4              ;N=0,Z=0,V=1,C=0, AND R4 = 052525
165156  050403                  BIS     R4,R3           ;N=0,Z=0,V=0,C=0, AND R3 = 052525
165160  060503                  ADD     R5,R3           ;N=1,Z=0,V=0,C=0, AND R3 = 177777
165162  005203                  INC     R3              ;N=0,Z=1,V=0,C=0, AND R3 = 000000
165164  103401                  BLO     1$              ; V BRANCH IF C=1
165166  002001                  BGE     TST13           ; * BRANCH IF (N XOR V)=0
165170  000000          1$:     HALT

                        ;;**************************************************************************
                                .SBTTL  TEST13  TEST "DEC" AND "BLOS", "BLT"
                        ;*
                        ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                        ;*      N = 0, Z = 1, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 052524
                        ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
                        ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                        ;*      N = 1, Z = 0, V = 0, AND C = 0.
                        ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                        ;*      R1 WHICH SHOULD NOW EQUAL 177777
                        ;*
                        ;;**************************************************************************
165172                  TST13:
165172  005301                  DEC     R1              ;N=1,Z=0,V=0,C=0,R1=177777
165174  101401                  BLOS    1$              ; V BRANCH IF (Z OR C)=1
```

```
                                TEST13  TEST "DEC" AND "BLOS", "BLT"

  564  165176  002401                     BLT     TST14           ; * BRANCH IF (N XOR V)=1
  565  165200  000000              1$:    HALT
  566
  567                                ;:**************************************************************************
  568                                        .SBTTL  TEST14  TEST "COM", "BIC", AND "BGT", "BGE", "BLE"
  569                                ;*
  570                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
  571                                ;*      N = 1, Z = 0, V = 0, AND C = 0.
  572                                ;*      THE REGISTERS ARE: R0 = 125252, R1 = 177777, R2 = 052524
  573                                ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
  574                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
  575                                ;*      N = 0, Z = 0, V = 1, AND C = 1.
  576                                ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
  577                                ;*      R0 WHICH SHOULD NOW EQUAL 052525, AND
  578                                ;*      R1 WHICH SHOULD NOW EQUAL 052524
  579                                ;*
  580                                ;:**************************************************************************
  581  165202                        TST14:
  582  165202  005100                     COM     R0              ;N=0,Z=0,V=0,C=1, AND R0 = 052525
  583  165204  101401                     BLOS    2$              ; * BRANCH IF (Z OR C)=1
  584  165206  000000                     HALT                    ;STOP HERE IF BRANCH FAILED
  585  165210  040001              2$:    BIC     R0,R1           ;N=1,Z=0,V=0,C=1, AND R1 = 125252
  586  165212  060101                     ADD     R1,R1           ;N=0,Z=0,V=1,C=1, AND R1 = 052524
  587  165214  003002                     BGT     1$              ; V BRANCH IF Z AND (N XOR V) ARE BOTH 0
  588  165216  002001                     BGE     1$              ; V BRANCH IF (N XOR V)=0
  589  165220  003401                     BLE     TST15           ; * BRANCH IF [Z OR (N XOR V)]=1
  590  165222  000000              1$:    HALT
  591
  592                                ;:**************************************************************************
  593                                        .SBTTL  TEST15  TEST "ADC", "CMP", "BIT", AND "BNE","BGT","BEQ"
  594                                ;*
  595                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
  596                                ;*      N = 0, Z = 0, V = 1, AND C = 1.
  597                                ;*      THE REGISTERS ARE: R0 = 052525, R1 = 052524, R2 = 052524
  598                                ;*      R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252.
  599                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
  600                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
  601                                ;*      THE REGISTERS ARE NOW:
  602                                ;*      R0 = 052525, R1 = 000000, R2 = 052524, R3 = 000000
  603                                ;*      R4 = 052525, R5 = 052525, SP = 125252.
  604                                ;*
  605                                ;:**************************************************************************
  606  165224                        TST15:
  607  165224  005501                     ADC     R1              ;N=0,Z=0,V=0,C=0, AND R1 = 052525
  608  165226  020401                     CMP     R4,R1           ;N=0,Z=1,V=0,C=0
  609  165230  001005                     BNE     1$              ; V BRANCH IF Z=0
  610                                                             ;R1 = 052525  R5 = 125252
  611  165232  030105                     BIT     R1,R5           ;N=0,Z=1,V=0,C=0
  612  165234  003003                     BGT     1$              ; V BRANCH IF Z AND (N XOR V) ARE BOTH 0
  613  165236  005105                     COM     R5              ;N=0,Z=0,V=0,C=1, AND R5 = 052525
  614  165240  160501                     SUB     R5,R1           ;N=0,Z=1,V=0,C=0, AND R1 = 000000
  615  165242  001401                     BEQ     TST16           ; * BRANCH IF Z=1
  616  165244  000000              1$:    HALT
  617
  618                                ;:**************************************************************************
  619                                        .SBTTL  TEST16  TEST "MOVB", "SOB", "CLR", "TST" AND "BPL", "BNE"
```

```
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = 052525, R1 = 000000, R2 = 052524
                                ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                ;*      R0 IS DECREMENTED BY A SOB INSTRUCTION TO 000000
                                ;*      R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000000
                                ;*
                                ;:**************************************************************************
165246                          TST16:
165246  112700  177401                MOVB    #177401,R0      ;N=0,Z=0,V=0,C=0, AND R0 = 000001
165252  100001                        BPL     2$              ; * BRANCH IF N=0
165254  000000                1$:     HALT                    ;STOP IF "BPL" FAILED
165256  077002                2$:     SOB     R0,1$           ;DO NOT LOOP SINCE (R0 - 1) = 0
165260  005001                        CLR     R1              ;N=0, Z=1, V=0, C=0, AND R1 = 000000
165262  005201                3$:     INC     R1              ;INCREMENT 64K TIMES (2 ** 16)
165264  077002                        SOB     R0,3$           ;LOOP BACK TO "INC" 64K TIMES
165266  005700                        TST     R0              ;N=0,Z=1,V=0,C=0, AND R0 = 000000
165270  001002                        BNE     4$              ; V BRANCH IF Z=0
165272  005701                        TST     R1              ;N=0,Z=1,V=0,C=0, AND R1 = 000000
165274  001401                        BEQ     TST17           ; * BRANCH IF Z=1
165276  000000                4$:     HALT
                                ;:**************************************************************************
                                        .SBTTL  TEST17  TEST "ASR", "ASL"
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = 000000, R1 = 000000, R2 = 052524
                                ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 0, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                                ;*      R0 WHICH IS NOW EQUAL TO 000000,
                                ;*      R1 WHICH IS NOW 000001, AND
                                ;*      R2 WHICH IS NOW 000000.
                                ;*
                                ;:**************************************************************************
165300                          TST17:
165300  012700  100000                MOV     #100000,R0      ;R0=100000
165304  005201                        INC     R1              ;R1=000001
165306  012702  000020                MOV     #^D16,R2        ;SET COUNTER TO 16 DECIMAL
165312  006200                1$:     ASR     R0              ;RIGHT SHIFT R0, SIGN EXTEND (16 TIMES)
165314  005500                        ADC     R0              ;ADD CARRY (0 UNTIL LAST TIME)
165316  006301                        ASL     R1              ;LEFT SHIFT R1 (16 TIMES)
165320  005501                        ADC     R1              ;ADD CARRY (0 UNTIL LAST TIME)
165322  077205                        SOB     R2,1$           ;LOOP BACK IS DECIMAL TIMES
                                                                ;AT THE END OF THE LOOP
                                                                ;R0 = 000000  AND  R1 = 000001
165324  060001                        ADD     R0,R1           ;N=0,Z=0,V=0,C=0  R1=000001, R0=000000
165326  003401                        BLE     2$              ; V BRANCH IF [Z OR (N XOR V)]=1
165330  003001                        BGT     TST20           ; * BRANCH IF Z AND (N XOR V) ARE BOTH 0
165332  000000                2$:     HALT
```

```
                                ;:*****************************************************************************
                                        .SBTTL  TEST20  TEST ASH, AND SWAB
                                ;*
                                ;*      WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 0, V = 0, AND C = 0.
                                ;*      THE REGISTERS ARE: R0 = 000000, R1 = 000001, R2 = 000000
                                ;*      R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252.
                                ;*      UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
                                ;*      N = 0, Z = 1, V = 0, AND C = 1.
                                ;*      THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
                                ;*      R1 WHICH SHOULD NOW EQUAL 000000
                                ;*
                                ;:*****************************************************************************
165334                          TST20:
165334  072127  000015                 ASH     #15,R1          ;LEFT SHIFT BIT0 INTO BIT15
                                                                ;N=1,Z=0,V=1,C=0, AND R1 = 100000
165340  000301                         SWAB    R1              ;SWITCH BYTES OF R1, R1 = 000200
                                                                ;N=1,Z=0,V=0,C=0
165342  072127  177770                 ASH     #-10,R1         ;RIGHT SHIFT R1 8 PLACES
                                                                ;N=0,Z=1,V=0,C=0, R1 = 000000
165346  001401                         BEQ     TST21           ;  * BRANCH IF Z=1
165350  000000                         HALT                    ;EITHER "SWAB" OR "ASH" FAILED

                                ;:*****************************************************************************
                                        .SBTTL  TEST21  TEST "JSR", "RTS", "RTI", & "JMP"
                                ;*
                                ;*      THIS TEST FIRST SETS THE STACK POINTER TO 776,
                                ;*      AND THEN VERIFIES THAT "JSR", "RTS", "RTI", AND "JMP"
                                ;*      ALL WORK PROPERLY.
                                ;*
                                ;*      ON ENTRY TO THIS TEST THE STACK POINTER "SP" IS INITIALIZED
                                ;*      TO 00776 AND IS LEFT THAT WAY ON EXIT.
                                ;*
                                ;:*****************************************************************************
165352                          TST21:

165352  032737  000400  173024         BIT     #400,@#173024   ;DO THE MEMORY-MODIFYING
                                                                ;GROUP OF TESTS?  (THIS TEST,
                                                                ;MEMORY TEST, CACHE TEST)
165360  001001                         BNE     11$             ;YES
165362  000571                         BR      JUMP0           ;SKIP, GO DIRECTLY TO BOOT
165364  012706  000776         11$:    MOV     #776,SP         ;SET UP THE STACK POINTER
165370  004767  000002                 JSR     PC,1$           ;TRY TO JSR TO 1$
165374  000000         10$:    HALT                    ;THE "JSR" MUST HAVE FAILED
165376  022716  165374          1$:    CMP     #10$,(SP)       ;WAS THE CORRECT ADDRESS PUSHED?
165402  001401                         BEQ     2$              ;BRANCH IF YES
165404  000000                         HALT                    ;WRONG THING PUSHED ON STACK
165406  012716  165416          2$:    MOV     #3$,(SP)        ;CHANGE THE ADDRESS ON THE STACK
165412  000207                         RTS     PC              ;TRY TO RETURN TO 3$
165414  000000                         HALT                    ;DID NOT RETURN PROPERLY
165416  005046          3$:    CLR     -(SP)           ;PUSH A ZERO ON THE STACK
165420  012746  165430                 MOV     #4$,-(SP)       ;PUSH THE RETURN ADDRESS ON STACK
165424  000002                         RTI                     ;SEE IF AN "RTI" WORKS
165426  000000                         HALT                    ;THE "RTI" FAILED
165430  000137  165436          4$:    JMP     @#5$            ;TRY TO "JMP"
165434  000000                         HALT                    ;THE "JMP" FAILED
```

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.MAIN.  MACY11 27(1006)  25-APR-77  08:26  PAGE 16
DQM90A.P11    13-APR-77 11:11          TEST21  TEST "JSR", "RTS", "RTI", & "JMP"

   732  165436                        5$:                             ;ADDRESS TO "JMP" TO
   733
   734
   735
   736
   737                                ;:*****************************************************************************
   738                                        .SBTTL  TEST22  TEST MAIN MEMORY FROM VIRTUAL 001000 TO LAST ADDR.
   739                                ;*
   740                                ;*      THIS TEST WILL TEST MAIN MEMORY WITH THE CACHE DISABLED, FROM
   741                                ;*      VIRTUAL ADDRESS 001000 TO LAST ADDR.  IF THE DATA DOES NOT COMPARE
   742                                ;*      PROPERLY THE TEST WILL HALT AT EITHER 165516 OR 165536. IF A
   743                                ;*      PARITY ERROR OCCURS THE TEST WILL HALT AT ADDRESS 165750, WITH
   744                                ;*      THE PC + 2 ON THE STACK WHICH IS IN THE KERNEL D-SPACE.
   745                                ;*
   746                                ;*      IN THIS TEST THE REGISTERS ARE INITIALIZED AS FOLLOWS:
   747                                ;*      R0 = 001000, R1 = DATA READ, R2 = 001000, R3 = 177746 (CACHE CONTROL REG.)
   748                                ;*      R4 = COUNT VALUE, R5 = LAST MEMORY ADDRESS SP = 000776
   749                                ;*
   750                                ;:*****************************************************************************
   751  165436                        TST22:
   752  165436  012700  165446               10$:    MOV     #10$,R0         ;SAVE RETURN ADDRESS
   753  165442  000137  173310               MOV     @#SIZE                  ;GO SIZE MEMORY, RETURN WITH R5 CONTAINING
   754                                                                        ;THE LAST MEMORY ADDRESS
   755  165446  012737  165750  000114      MOV     #CONT,@#114             ;SET UP PARITY VECTOR
   756  165454  005037  000116               CLR     @#116                   ;SET PROCESSOR STATUS WORD TO ZERO
   757  165460  012703  177746               MOV     #177746,R3              ;CACHE CONTROL REGISTER ADDRESS
   758  165464  012713  000014               MOV     #MISS,(R3)              ;FORCE MISS BOTH GROUPS
   759  165470  012702  001000               MOV     #1000,R2                ;FIRST ADDRESS STORAGE
   760  165474  010200                       MOV     R2,R0                   ;SETUP FIRST ADDRESS
   761  165476  010010               1$:     MOV     R0,(R0)                 ;LOAD EACH ADDRESS WITH ITS
   762                                                                        ;OWN ADDRESS
   763  165500  005720                       TST     (R0)+
   764  165502  020005                       CMP     R0,R5
   765  165504  101774                       BLOS    1$
   766  165506  010200                       MOV     R2,R0                   ;SET STARTING ADDRESS IN R0
   767  165510  011001               2$:     MOV     (R0),R1                 ;GET THE DATA
   768  165512  020001                       CMP     R0,R1                   ;IS IT CORRECT?
   769  165514  001401                       BEQ     3$                      ;BRANCH IF YES
   770  165516  000000                       HALT                            ;DATA ERROR ON READING MEMORY LOCATION
   771                                                                        ;R0=ADDRESS, R1=DATA RECEIVED, R0=DATA EXPECTED
   772  165520  005120               3$:     COM     (R0)+                   ;COMPLEMENT DATA AND INCREMENT ADDRESS
   773  165522  020005                       CMP     R0,R5
   774  165524  101771                       BLOS    2$
   775  165526  014001               4$:     MOV     -(R0),R1                ;READ THE DATA (IT SHOULD NOW BE THE
   776                                                                        ;COMPLEMENT OF THE ADDRESS)
   777  165530  005101                       COM     R1                      ;COMPLEMENT BEFORE CHECKING
   778  165532  020001                       CMP     R0,R1                   ;IS THE DATA CORRECT?
   779  165534  001401                       BEQ     5$                      ;BRANCH IF YES
   780  165536  000000                       HALT                            ;DATA ERROR ON READING MEMORY LOCATION
   781                                                                        ;R0=ADDRESS, R1=DATA RECEIVED, R0=DATA EXPECTED
   782  165540  020002               5$:     CMP     R0,R2
   783  165542  001371                       BNE     4$
```

```
                                .SBTTL  CACHE MEMORY DIAGNOSTIC TESTS

                                ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                ;*
                                ;*      THE FOLLOWING TWO TESTS ARE CACHE MEMORY TESTS, IF EITHER OF
                                ;*      THEM FAILS TO RUN SUCCESSFULLY THEY WILL COME TO A HALT
                                ;*      IN THE M9301 ROM.  IF YOU DESIRE TO TRY TO BOOT YOUR SYSTEM, OR
                                ;*      DIAGNOSTIC ANYWAY, YOU CAN PRESS "CONTINUE" AND THE PROGRAM
                                ;*      WILL FORCE MISSES IN THE CACHE AND GO TO THE
                                ;*      BOOT STRAP THAT HAS BEEN SELECTED.
                                ;*
                                ;†††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††
                                ;†††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††
                                ;;**********************************************************************
                                        .SBTTL  TEST23  TEST CACHE DATA MEMORY
                                ;*
                                ;*      THIS TEST WILL CHECK THE DATA MEMORY IN THE CACHE, ON THE PDP 11/60
                                        THERE IS ONLY ONE GROUP (1-K), ON PDP 11/60 THERE ARE
                                        TWO GROUPS, 1/2 K EACH.
                                ;*      THE TEST LOADS 052525 INTO AN ADDRESS COMPLEMENTS
                                ;*      IT TWICE AND THEN READS THE DATA, THEN IT CHECKS TO INSURE THAT
                                ;*      THE DATA WAS A HIT.  THEN THE SEQUENCE IS REPEATED ON THE SAME

                                ;*      ADDRESS WITH 125252 AS THE DATA.  ALL CACHE MEMORY DATA LOCATIONS
                                ;*      ARE TESTED IN THIS WAY.
                                ;*      IF EITHER GROUP FAILS AND THE OPERATOR PRESSES CONTINUE THE
                                ;*      PROGRAM WILL TRY TO BOOT WITH THE CACHE DISABLED.
                                ;*
                                ;*      THE REGISTERS ARE INITIALIZED AS FOLLOWS FOR THIS TEST:
                                ;*      R0 = 4000 (ADDRESS) R1 = 2 (COUNT), R2 = 1000 (COUNT)
                                ;*      R3 = 177746 (CONTROL REG.), R4 = 125252 (PATTERN) R5 = LAST MEMORY ADDRESS
                                ;*      SP = 000776 (FLAG OF ZERO PUSHED ON STACK)
                                ;*
                                ;;**********************************************************************
165544                          TST23:
165544  005016                          CLR     (SP)            ;SET THE CYCLE FLAG TO ZERO,PATTERN FLAG TO 0
165546  012704  125252                  MOV     #125252,R4      ;SET UP R4 FOR TEST
165552  012713  000030                  MOV     #GRP0,(R3)      ;FORCE REPLACE GROUP 0 AND FORCE MISS GROUP  1 (ON 11/70
                                                                ;FORCE MISS UPPER 1/2 K OF CACHE ON 11/60
165556  012700  004000                  MOV     #4000,R0        ;SET STARTING ADDRESS INTO R0
165562  012702  001000          1$:     MOV     #1000,R2                ;SET COUNT TO 1000 OCTAL
165566  005104                  3$:     COM     R4              ;COMPLEMENT DATA IN R4
165570  010410                          MOV     R4,(R0)         ;WRITE THE TEST PATTERN
165572  005110                          COM     (R0)            ;DOUBLE COMPLEMENT DATA AND
165574  005110                          COM     (R0)            ;MAKE SURE DATA IS IN THE CACHE
165576  021004                          CMP     (R0),R4         ;COMPARE DATA & SET BIT 0 IN HIT/MISS REG.
165600  001401                          BEQ     5$              ;BRANCH IF DATA MATCHES
165602  000000                          HALT                    ;CACHE DATA DIDN'T MATCH
                                                                ;R0=ADDRESS, R4=EXPECTED DATA
165604  006037  177752          5$:     ROR     @#177752        ;WAS THE LAST MEMORY REFERENCE A HIT?
165610  103402                          BCS     4$              ;BRANCH IF YES
165612  000000                          HALT                    ;CACHE FAILED TO HIT
                                                                ;R0=ADDRESS THAT WAS REFERENCED
```

```
                165614  000457                  BR      BOOTMISS        ;ABORT REST OF TEST IF "CONTINUE" PRESSED
                165616  105116          4$:     COMB    (SP)
                165620  001362                  BNE     3$
                165622  005720                  TST     (R0)+           ;MOVE TO NEXT ADDRESS
                165624  077220                  SOB     R2,3$           ;BRANCH IF NOT DONE
                165626  012713  000044          MOV     #GRP1,(R3)      ;FORCE REPLACE GROUP 1 AND FORCE MISS GROUP 0 (ON 11/70)
                                                                        ;FORCE MISS LOWER 1/2 K OF CACHE ON 11/60
                165632  012700  006000          MOV     #6000,R0
                165636  105166  000001          COMB    1(SP)           ;COMPLEMENT THE CYCLE FLAG
                165642  001347                  BNE     1$              ;LOOP IF NOT DONE

                ;;*******************************************************************************
                        .SBTTL  TEST24  TEST MEMORY WITH THE DATA CACHE ON
                ;*
                ;*      THIS TEST CHECKS VIRTUAL MEMORY FROM 001000 THRU LAST ADDRESS
                ;*      TO INSURE THAT YOU CAN GET HITS ALL THE WAY UP THROUGH MAIN
                ;*      MEMORY.  ON THE PDP 11/70, IT STARTS WITH GROUP 1 ENABLED, THEN TESTS
                ;*      GROUP 0, AND FINALLY CHECKS MEMORY WITH BOTH GROUPS ENABLED.
                ;*      ON THE PDP 11/60, THE TEST IS DONE WITH THE
                ;*      WHOLE CACHE ENABLED.
                ;*
                ;*      UPON ENTRY THE REGISTERS WILL BE SET UP AS FOLLOWS:
                ;*      R0 = 001000 (ADDRESS), R1 = 3 (PASS COUNT), R2 = (FIRST ADDRESS),
                ;*      R3 = 177746 (CONTROL REG.),
                ;*      R5 = (LAST MEMORY ADDRESS), SP = 776
                ;*
                ;*      UPON COMPLETION OF THIS TEST MAIN MEMORY FROM VIRTUAL ADDRESS
                ;*      001000 THRU LAST ADDRESS WILL CONTAIN ITS OWN VIRTUAL ADDRESS.
                ;*
                ;;*******************************************************************************
                TST24:
                165644  012702  001000          MOV     #1000,R2        ;SETUP FIRST ADDRESS
                165650  010200                  MOV     R2,R0           ;FIRST ADDRESS IS 1000 OCTAL
                165652  010010          1$:     MOV     R0,(R0)         ;FILL MEMORY WITH ADDRESSES
                165654  005720                  TST     (R0)+
                165656  020005                  CMP     R0,R5
                165660  101774                  BLOS    1$
                165662  012701  000003          MOV     #3,R1           ;SET PASS COUNT TO THREE
                165666  005016                  CLR     (SP)
                165670  032737  000002  173024  BIT     #2,@#173024     ;MICRO-SWITCH 2 INDICATES PDP 11/60 OR 11/70
                165676  001420                  BEQ     6$              ;IT IS PDP 11/60
                165700  012716  000030          MOV     #GRP0,(SP)      ;LOAD CODE TO FORCE GROUP 0 ONTO STACK
                165704  010200          2$:     MOV     R2,R0           ;FIRST ADDRESS
                165706  005110          3$:     COM     (R0)            ;DOUBLE COMPLEMENT DATA AND
                165710  005110                  COM     (R0)            ;MAKE SURE IT IS IN THE CACHE.
                165712  020010                  CMP     R0,(R0)         ;COMPARE DATA, AND SET BIT 0 IN HIT/MISS REG
                                                                        ;ALSO POINT TO NEXT ADDRESS
                165714  001401                  BEQ     5$              ;BRANCH IF DATA MATCHES
                165716  000000                  HALT                    ;DATA DIDN'T MATCH R0 = ADDRESS + 2
                165720  005720          5$:     TST     (R0)+
                165722  006037  177752          ROR     @#177752        ;WAS THE LAST MEMORY REFERENCE A HIT?
                165726  103402                  BCS     4$              ;BRANCH IF YES
                165730  000000                  HALT                    ;HIT FAILED TO OCCUR R0 = ADDRESS + 2
                165732  000410                  BR      BOOTMISS        ;ABORT REST OF TEST IF "CONTINUE" PRESSED
                165734  020005          4$:     CMP     R0,R5
                165736  101763                  BLOS    3$
```

```
                                        ;
                                        ;FORCE MISS GRP1 ON PASS 2, FULLY
                                        ;ENABLE CACHE ON PASS THREE. (11/70)
                                        ;ON 11/60, RUN EACH PASS WITH THE WHOLE
                                        ;CACHE ENABLED.
165742  005016          6$:     CLR     (SP)            ;GET READY TO FULLY ENABLE CACHE ON PASS 3
165744  077121          JUMPO:  SOB     R1,2$           ;RUN THREE PASSES THRU THIS TEST
165746  000404                  BR      JUMP            ;GO TO BOOT STRAP CODE
                                        ;
                                        ;
165750  000000          CONT:   HALT                    ;STOP HERE IF THERE IS A CACHE PARITY ERROR
                                        ;OR A MAIN MEMORY PARITY ERROR
                                        ;CHECK CCR, MEMORY REGISTER AND CPU REGISTER
                                        ;TO FIND WHICH ONE
165752  000402                  BR      JUMP
165754                  BOOTMISS:                       ;ENTER HERE IF ANY ERROR (EXCEPT PARITY) OCCURED IN CACH
165754  012713  000014          MOV     #MISS,(R3)      ;FORCE MISSES IN BOTH GROUPS OF CACHE
165760  000137  173112  JUMP:   JMP     @#CHKSWR        ;GO TO BOOT STRAP
```

BOOTSTRAP ENTRY POINT IS AT 17773000

```
                                .SBTTL  BOOTSTRAP ENTRY POINT IS AT 17773000
                                ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                ;VVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVVV
                                ;*
                                ;*      THE REGISTER USAGE DURING THE BOOTSTRAP IS GENERALLY AS FOLLOWS:
                                ;*
                                ;*      R0 = THE DRIVE NUMBER RIGHT JUSTIFIED (0 - 7)
                                ;*      R1 = THE ADDRESS OF THE MAIN CONTROL AND STATUS REGISTER
                                ;*      R2 = THE DRIVE NUMBER POSITIONED FOR LOADING INTO DEVICE
                                ;*      R3 = POINTER TO THE FUNCTION TABLE
                                ;*      R4 = INDEX NUMBER TO GET THRU THE TABLES FOR THE CORRECT INFORMATION
                                ;*      R5 = 100200 'ERROR' BIT AND 'READY' BIT
                                ;*
                                ;*
                                ;*      AFTER A SUCCESSFUL BOOT THE REGISTERS ARE AS FOLLOWS:
                                ;*
                                ;*      R0 = THE DRIVE NUMBER RIGHT JUSTIFIED (0 - 7)
                                ;*      R1 = THE ADDRESS OF THE MAIN COMMAND AND STATUS REGISTER
                                ;*
                                ;†††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††
                                ;†††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††††

          173000                            . = BASE2

173000  032737  000004  173024  BOOT:   BIT     #4,@#173024     ;SW OFF? SKIP TESTS (CPU, MEM, CACHE)?
173006  001041                          BNE     CHKSWR          ;IF YES, DONT EXECUTE ANY TESTS, GO
                                                                ;STRAIGHT TO THE BOOT
173010  000137  165000                  JMP     @#DIAG          ;GO DO THE TESTS

                                .SBTTL  THIS IS THE CODE TO READ THE SWITCH REGISTER AND SWITCHES

173014  113700  177570  START:  MOVB    @#SWR,R0        ;READ THE CONSOLE SWITCH REGISTER (LO BYTE)
173020  001005                  BNE     START2          ;IF NON-ZERO, GET THE DEVICE CODE FROM CONSOLE SWR
173022  012700          START1: MOV     (PC)+,R0        ;IF ZERO, READ THE MICRO-SWITCHES (AT 173024)
173024  000776                  .WORD   776             ;MICRO-SWITCH ADDRESS
173026  006200                  ASR     R0              ;SHIFT RIGHT CONTENTS OF MICRO-SWITCH AND
173030  042700  000007          BIC     #7,R0           ;MASK FOR COMMON PROCESSING
173034  010004          START2: MOV     R0,R4           ;COPY THE CONSOLE SWR OR MICRO-SWITCHES INTO R4
173036  042704  177607          BIC     #177607,R4      ;LEAVE DEVICE NUMBER IN R4 BITS <06:03>
173042  001004                  BNE     3$              ;IF DEVICE NUMBER WAS 0,
173044  013704  173024          MOV     @#173024,R4     ;READ THE MICRO-SWITCHES
173050  006204                  ASR     R4              ;SHIFT AND PROCESS
173052  000770                  BR      START2
173054  072427  177776  3$:     ASH     #-2,R4          ;SHIFT DEVICE NUMBER (IN R4) TO BITS <2=0>
173060  005744                  TST     -(R4)           ;ADJUST R4 TO INDEX THRU TABLE (0 - 74)
173062  042700  177770          BIC     #^C7,R0         ;LEAVE UNIT NUMBER IN R0 BITS <02 : 00>
173066  010002                  MOV     R0,R2           ;COPY UNIT NUMBER INTO R2
173070  000302                  SWAB    R2              ;PUT UNIT NUMBER IN UPPER BYTE OF R2
173072  012705  100200          MOV     #100200,R5      ;LOAD 'ERROR' AND 'READY' BITS INTO R5
173076  016401  173636          MOV     CSRPTR(R4),R1   ;LOAD MAIN CSR ADDRESS INTO R1
173102  016403  173662          MOV     CMDPTR(R4),R3   ;LOAD POINTER TO FUNCTION TABLE
173106  000174  173704          JMP     @ADDRS(R4)      ;JUMP TO START OF PARTICULAR BOOT
```

```
                                        THIS IS THE CODE TO READ THE SWITCH REGISTER AND SWITCHES

 969
 970
 971  173112  032737  000010  173024  CHKSWR: BIT     #10,@#173024    ;IS MICRO-SWITCH SET TO
 972                                                                  ;DISABLE LOOKING AT SWITCH REGISTER?
 973  173120  001340                          BNE     START1          ;IF OFF, DONT LOOK AT SWR
 974  173122  000734                          BR      START           ;IF ON, SENSE THE CONSOLE SWREG
 975
 976
 977                                  .SBTTL  THIS IS THE START OF THE TC11/TU56 BOOT STRAP (DECTAPE, TC11-G)
 978                                          ;COMMAND REGISTER ADDRESS IS 177342
 979
 980  173124  010211                  TU56:   MOV     R2,(R1)         ;LOAD UNIT NUMBER INTO C.S.R.
 981  173126  052311                          BIS     (R3)+,(R1)      ;'OR' REWIND COMMAND INTO C.S.R.
 982  173130  005711                  1$:     TST     (R1)            ;SEE IF ERROR BIT IS SET
 983  173132  100376                          BPL     1$              ;WAIT UNTIL BIT 15 OF C.S.R. IS SET
 984  173134  005761  177776                  TST     -2(R1)          ;IS THE ERROR  'END ZONE'
 985  173140  100017                          BPL     AGAIN           ;BRANCH IF NOT 'END ZONE'
 986  173142  000420                          BR      RP03
 987
 988
 989                                  .SBTTL  THIS IS THE START OF THE TM11/TU10 BOOT STRAP (MAGNETIC TAPE, TM11)
 990                                          ;COMMAND REGISTER ADDRESS IS 172522
 991
 992  173144  010211                  TU10:   MOV     R2,(R1)         ;LOAD UNIT NUMBER INTO C.S.R.
 993  173146  006061  177776          1$:     ROR     -2(R1)          ;IS THE SELECTED DRIVE ON LINE
 994  173152  103375                          BCC     1$              ;WAIT FOR BIT TO BE SET BY DRIVE
 995  173154  052311                          BIS     (R3)+,(R1)      ;'OR' REWIND COMMAND INTO C.S.R.
 996                                                                  ;THIS COMMAND ALSO SETS 800 BPI 9 CHAN.
 997  173156  105711                  2$:     TSTB    (R1)            ;SEE IF THE REWIND IS COMPLETE
 998  173160  100376                          BPL     2$              ;WAIT FOR READY BIT OF C.S.R. TO BE SET
 999  173162  012761  177777  000002          MOV     #-1,2(R1)       ;SET RECORD COUNTER TO SKIP ONE RECORD
1000  173170  112311                          MOVB    (R3)+,(R1)      ;LOAD SPACE FORWARD COMMAND INTO C.S.R.
1001  173172                          TU10A:
1002  173172  030511                  3$:     BIT     R5,(R1)         ;TEST FOR 'ERROR' AND 'READY' BITS
1003  173174  001776                          BEQ     3$              ;BRANCH IF NEITHER SET
1004  173176  100003                          BPL     CMNSGO          ;BRANCH TO COMMON READ IF NO ERRORS
1005
1006
1007                                  .SBTTL  CODE TO CLEAN UP WORLD AND TRY BOOTSTRAP AGAIN
1008
1009  173200  000005                  AGAIN:  RESET                   ;CLEAR ALL DEVICES AFTER ERROR
1010  173202  000743                          BR      CHKSWR          ;GO SET UP MEMORY MANAGEMENT AND UNIBUS MAP
1011                                                                  ;AND ATTEMPT TO BOOT AGAIN.
1012
1013                                  .SBTTL  THIS IS THE START OF THE RP11/RP03 BOOT STRAP (DISK PACK, RP11-C)
1014                                          ;COMMAND REGISTER ADDRESS IS 176714
1015
1016  173204  010211                  RP03:   MOV     R2,(R1)         ;LOAD THE UNIT NUMBER INTO THE COMMAND REG.
1017
1018
1019
1020                                  .SBTTL  THIS IS THE START OF THE COMMON READ CODE
1021
1022  173206  012761  177000  000002  CMNSGO: MOV     #-512.,2(R1)    ;LOAD WORD COUNT OF 256 WORDS
1023  173214  112302                          MOVB    (R3)+,R2        ;LOAD READ FUNCTION INTO LO BYTE
1024                                                                  ;& THEN LOAD READ FUNCTION INTO C.S.R.
```

```
1025                                                                    ;NOTE: THE ABOVE IS DONE BECAUSE RK611
1026                                                                    ;DOES NOT RECOGNIZE BYTE OPERATIONS
1027                                                                    ;ON THE BUS.
1028  173216  042711  000377                BIC     #377,(R1)         ;CLEAR OUT  LO BYTE OF THE C.S.R.
1029  173222  000402                        BR      CMN1
1030
1031
1032          173224                        .=BASE4                   ;ASSEMBLED AT 773224 & 773226
1033  173224  173000                        .WORD   173000            ;VECTOR TO THE START OF M9301 BOOTSTRAP
1034  173226  000340                        .WORD   000340            ;PROCESSOR STATUS TO ASSUME AT BOOT TIME
1035
1036  173230  050211                CMN1:   BIS     R2,(R1)           ;MOVE THE READ FUNCTION INTO C.S.R.
1037  173232  105711                GO1:    TSTB    (R1)              ;TEST FOR 'READY' BIT
1038  173234  100376                        BPL     GO1               ;WAIT UNTIL READY IS SET
1039  173236  005711                        TST     (R1)              ;TEST FOR ERROR BIT
1040  173240  100005                        BPL     CLRCS             ;NO ERROR
1041  173242  105713                        TSTB    (R3)              ;IS IT TU16?
1042  173244  001355                        BNE     AGAIN             ;NO
1043  173246  021361  000014                CMP     (R3),14(R1)       ;IF YES, WAS THE ERROR A FRAME COUNT EROR?
1044  173252  001352                        BNE     AGAIN             ;IF NOT, TRY TO BOOT AGAIN
1045
1046  173254  105011                CLRCS:  CLRB    (R1)              ;CLEAR COMMAND REGISTER. THIS WILL
1047                                                                  ;STOP DECTAPE MOTION IF DEVICE WAS
1048                                                                  ;TU56 - DON'T CLEAR HIGH BYTE
1049  173256  005007                        CLR     PC                ;START SECONDARY BOOT AT 0
1050
1051
1052                                .SBTTL  THIS IS THE START OF THE RKXX/RK06 BOOT STRAP (DISK DUMMY)
1053                                        ;COMMAND REGISTER ADDRESS IS 177400
1054
1055  173260  010061  000010        RK06:   MOV     R0,10(R1)         ;LOAD DRIVE NUMBER INTO DRIVE SELECT REG.
1056  173264  012711  000003                MOV     #3,(R1)           ;LOAD PACK ACKNOWLEDGE FUNCTION
1057  173270  000740                        BR      TU10A
```

```
                                        THIS IS THE START OF THE RH11/RP04 BOOT STRAP (DISK PACK, RWP04)

 1058                                   .SBTTL  THIS IS THE START OF THE RH11/RP04 BOOT STRAP (DISK PACK, RWP04)
 1059                                           ;COMMAND REGISTER ADDRESS IS 176700
 1060
 1061   173272  110061  000010          RP04:   MOVB    R0,10(R1)       ;SELECT UNIT NUMBER TO BOOT FROM
 1062   173276  112311                          MOVB    (R3)+,(R1)      ;ISSUE READ-IN PRESET COMMAND
 1063   173300  012761  014000  000032          MOV     #14000,32(R1)   ;SET FMT22 & ECC INHIBIT BITS
 1064   173306  000470                          BR      CMNSRH          ;GO JOIN THE COMMON RH70 CODE
```

```
                                        THIS IS THE START OF THE RH11/RP04 BOOT STRAP (DISK PACK, RWP04)

1065
1066
1067                                    .SBTTL  THIS IS THE MEMORY SIZING CODE
1068                                            ;ENTER WITH R0=RETURN ADDRESS
1069                                            ;EXIT  WITH R5=LAST MEMORY ADDRESS
1070
1071  173310  012705  160000        SIZE:   MOV     #160000,R5      ;SETUP MEMORY CHECK LIMIT (28K)
1072  173314  005037  000006                CLR     @#6             ;CLEAR LOC. 6 (TIMEOUT VEC.+2)
1073  173320  012737  173326  000004        MOV     #1$,@#4         ;SETUP TIMEOUT VECTOR
1074  173326  012706  000776        1$:     MOV     #776,SP         ;SETUP STACK POINTER
1075  173332  005745                TST     -(R5)           ;FIND LAST MEM. LOC.
1076  173334  010007                MOV     R0,PC           ;RETURN
1077
1078
1079                                    .SBTTL  THIS IS THE START OF THE RH11/TU16 BOOT STRAP (MAGNETIC TAPE SYSTEM, TWU16)
1080                                            ;COMMAND REGISTER ADDRESS IS 172440
1081
1082  173336  010061  000032        TU16:   MOV     R0,32(R1)       ;LOAD UNIT NUMBER INTO SLAVE SELECT REG.
1083  173342  052361  000032                BIS     (R3)+,32(R1)    ;MERGE IN FORMAT AND DENSITY BITS
1084  173346  032761  010000  000012  1$:   BIT     #MOL,12(R1)     ;IS THE MEDIUM ON LINE?
1085  173354  001774                BEQ     1$              ;WAIT FOR BIT 12 OF DRIVE STATUS REG
1086  173356  112311                MOVB    (R3)+,(R1)      ;ISSUE REWIND COMMAND
1087  173360  105761  000012        2$:     TSTB    12(R1)          ;IS DRIVE READY BIT SET YET?
1088  173364  100375                BPL     2$              ;WAIT FOR DRIVE READY BIT
1089  173366  112311                MOVB    (R3)+,(R1)      ;ISSUE DRIVE CLEAR COMMAND
1090  173370  105761  000012        3$:     TSTB    12(R1)          ;IS DRIVE READY BIT SET?
1091  173374  100375                BPL     3$              ;WAIT UNTIL BIT 07 IS SET
1092  173376  012761  177777  000006        MOV     #-1,6(R1)       ;SET SKIP COUNT TO 1 RECORD
1093  173404  112311                MOVB    (R3)+,(R1)      ;ISSUE SPACE FORWARD COMMAND
1094  173406  105761  000012        4$:     TSTB    12(R1)          ;HAS THE DRIVE FINISHED THE SPACE?
1095  173412  100375                BPL     4$              ;WAIT UNTIL BIT 07 IS SET
1096  173414  000425                BR      CMNSRH          ;GO JOIN COMMON RH70 CODE
1097
1098                                    .SBTTL  THIS IS THE START OF THE PC11 BOOTSTRAP (HIGH SPEED PAPER TAPE READER)
1099                                            ;THE STATUS REGISTER ADDRESS IS 177550
1100
1101  173416  012700  173424        PC11:   MOV     #1$,R0          ;SAVE RETURN PC
1102  173422  000732                BR      SIZE            ;GO SIZE MEMORY
1103                                            ;RETURN WITH R5=LAST ADDR.
1104  173424  010115        1$:     MOV     R1,(R5)
1105  173426  142705  000024                BICB    #24,R5          ;MASK FOR SPECIAL ADDRESS
1106  173432  010515                MOV     R5,(R5)         ;STORE OWN ADDRESS IN POINTER
1107  173434  011503        2$:     MOV     (R5),R3         ;GET BYTE POINTER
1108  173436  005211                INC     (R1)            ;ENABLE TAPE READER
1109  173440  105711        3$:     TSTB    (R1)            ;TEST DONE BIT
1110  173442  100376                BPL     3$              ;WAIT UNTIL READY
1111  173444  116113  000002        MOVB    2(R1),(R3)      ;STORE DATA AT BYTE POINTER
1112  173450  005215                INC     (R5)            ;BUMP POINTER
1113  173452  122703  000375        CMPB    #375,R3         ;STORED JUMP OFFSET?
1114  173456  001366                BNE     2$              ;BRANCH IF NOT YET
1115  173460  105223                INCB    (R3)+           ;YES, ALL DONE
1116  173462  000143                JMP     -(R3)           ;GO EXECUTE AS BRANCH
1117
1118
1119                                    .SBTTL  THIS IS THE START OF THE RH11/RS04 BOOT STRAP (FIXED HEAD DISK, RWS04)
1120                                            ;COMMAND REGISTER ADDRESS IS 172040
```

```
                        THIS IS THE START OF THE RH11/RS04 BOOT STRAP (FIXED HEAD DISK, RWS04)

  1121
  1122  173464  110061  000010          RS04:   MOVB    R0,10(R1)       ;LOAD THE DRIVE NUMBER TO BOOT FROM
  1123
```

```
                                        THIS IS THE START OF THE COMMON RH-70 CODE

                                .SBTTL  THIS IS THE START OF THE COMMON RH-70 CODE

173470  016161  000016  000016  CMNSRH: MOV     16(R1),16(R1)   ;TURN OFF ANY ACTIVE ATTENTION FLAGS
173476  000643                  CSRH1: -BR      CMNSGC          ;BRANCH TO COMMON READ CODE


                                .SBTTL  THIS IS THE START OF THE RX11/RX01 BOOT STRAP (FLOPPY DISK)
                                        ;COMMAND REGISTER ADDRESS IS 177170

173500  052705  000040          RX01:   BIS     #40,R5          ;ADD 'DONE' BIT TO 'ERROR' AND 'TR' BITS
173504  005700                          TST     R0              ;TEST UNIT NUMBER
173506  001401                          BEQ     1$              ;BRANCH IF UNIT 0 WAS SELECTED
173510  005723                          TST     (R3)+           ;ADD 2 TO FUNCTION CODE POINTER
173512  130511                  1$:     BITB    R5,(R1)         ;TEST FOR 'TR' AND 'DONE' BITS
173514  001776                          BEQ     1$              ;WAIT UNTIL ONE IS SET
173516  112311                          MOVB    (R3)+,(R1)      ;LOAD READ COMMAND FOR PROPER DRIVE
173520  012702  000002                  MOV     #2,R2           ;LOAD LOOP COUNT INTO R2
173524  105711                  2$:     TSTB    (R1)            ;TEST FOR THE 'TR' BIT
173526  100376                          BPL     2$              ;WAIT UNTIL IT IS SET
173530  112761  000001  000002          MOVB    #01,2(R1)       ;LOAD TRACK ADDRESS THEN SECTOR NUMBER
173536  077206                          SOB     R2,2$           ;LOOP BACK TO LOAD SECTOR NUMBER
173540  030511                  3$:     BIT     R5,(R1)         ;TEST FOR 'ERROR' 'TR' AND 'DONE' BITS
173542  001776                          BEQ     3$              ;WAIT FOR ONE OF THE BITS
173544  100615                          BMI     AGAIN           ;BRANCH TO RETRY BOOTSTRAP IF 'ERROR' BIT SET
173546  111311                          MOVB    (R3),(R1)       ;LOAD EMPTY BUFFER COMMAND FOR PROPER DRIVE
173550  130511                  4$:     BITB    R5,(R1)         ;TEST FOR 'TR' OR 'DONE' BITS
173552  001776                          BEQ     4$              ;WAIT FOR ONE OF THE BITS
173554  100003                          BPL     CHK240          ;BRANCH TO CHECK ADDRESS ZERO IF 'DONE' BIT
173556  116122  000002                  MOVB    2(R1),(R2)+     ;STORE DATA IN MEMORY (R2 GOES FROM 000 TO 177)
173562  000772                          BR      4$              ;GO GET NEXT BYTE
173564  022737  000240  000000  CHK240: CMP     #240,@#0        ;CHECK THE FIRST ADDRESS BOOTED
173572  001202                          BNE     AGAIN           ;BRANCH TO RETRY IF NOT A 'NOP'
173574  005007                          CLR     PC              ;START SECONDARY BOOT AT ADDRESS ZERO


                                .SBTTL  THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECPACK DISK CARTRIDGE, RK11-D)
                                        ;COMMAND REGISTER ADDRESS IS 177404

173576  072227  000005          RK05:   ASH     #5,R2           ;LEFT SHIFT UNIT NUMBER 5 PLACES
173602  010261  000006                  MOV     R2,6(R1)        ;LOAD UNIT NUMBER INTO DEVICE
173606  000733                          BR      CSRH1           ;BRANCH TO COMMON READ CODE
```

```
                        THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECPACK DISK CARTRIDGE, RK11-D)


                        .SBTTL  FUNCTION CODES FOR THE ALL OF THE DEVICES

173610  060017          TU10$:  .WORD   060017          ;REWIND SELECTED DRIVE AND SET 800 BPI
173612     011                  .BYTE   011             ;SPACE FORWARD COMMAND FOR TU10
173613     003                  .BYTE   003             ;READ COMMAND FOR TU10
                                                        ;PACK ACKNOWLEDGE FOR RK06
173614                  RK06$:
173614     021          RP04$:  .BYTE   021             ;READ-IN PRESET FOR RP04; READ FOR RK06
173615     071          RS04$:  .BYTE   071             ;READ COMMAND FOR RP04 & RS04

173616  004003          TU56$:  .WORD   004003          ;SEARCH FOR BLOCK 0, REVERSE DIRECTION
173620                  RK05$:
173620     005          RP03$:  .BYTE   005             ;READ COMMAND FOR TU56, RK05, RP03

173621     077                  .BYTE   077             ;THIS IS A FILLER-NON-ZERO BYTE
                                                        ;TO DISTINGUISH FROM THE (BYTE FOLLOWING
                                                        ;THE READ FORWARD COMMAND) IN TU16

173622  001300          TU16$:  .WORD   1300            ;FORMAT BITS FOR TU16, 800 BPI, NRZI
173624     007                  .BYTE   007             ;REWIND SELECTED DRIVE
173625     011                  .BYTE   011             ;DRIVE CLEAR COMMAND
173626     031                  .BYTE   031             ;SPACE FORWARD
173627     071                  .BYTE   071             ;READ FORWARD
173630  001000                  .WORD   1000            ;FRAME COUNT ERROR

                                .EVEN                   ;INSURE WORD BOUNDARY
173632     007          RX01$:  .BYTE   007             ;READ SECTOR COMMAND FOR DRIVE ZERO
173633     003                  .BYTE   003             ;EMPTY BUFFER COMMAND FOR DRIVE ZERO
173634     027                  .BYTE   027             ;READ SECTOR COMMAND FOR DRIVE ONE
173635     023                  .BYTE   023             ;EMPTY BUFFER COMMAND FOR DRIVE ONE
```

```
                                        FUNCTION CODES FOR THE ALL OF THE DEVICES

1197
1198
1199                                    .SBTTL  COMMAND AND STATUS REGISTER ADDRESS TABLE
1200   173636  172522                   CSRPTR: .WORD   172522          ;THIS IS THE C.S.R. ADDRESS FOR TU10
1201   173640  177342                           .WORD   177342          ;THIS IS THE C.S.R. ADDRESS FOR THE TU56
1202   173642  177404                           .WORD   177404          ;THIS IS THE C.S.R. ADDRESS FOR THE RK05
1203   173644  176714                           .WORD   176714          ;THIS IS THE C.S.R. ADDRESS FOR THE RP03
1204   173646  177440                           .WORD   177440          ;THIS IS THE C.S.R. ADDRESS FOR THE RK06
1205   173650  172440                           .WORD   172440          ;THIS IS THE C.S.R. ADDRESS FOR THE RH11/TU16
1206   173652  176700                           .WORD   176700          ;THIS IS THE C.S.R. ADDRESS FOR THE RH11/RP04
1207   173654  172040                           .WORD   172040          ;THIS IS THE C.S.R. ADDRESS FOR THE RH11/RS04
1208   173656  177170                           .WORD   177170          ;THIS IS THE C.S.R. ADDRESS FOR RX11/RX01
1209   173660  177550                           .WORD   177550          ;THIS IS THE C.S.R. ADDRESS FOR THE PC11
1210
1211                                    .SBTTL  FUNCTION POINTER TABLE
1212
1213   173662  173610                   CMDPTR: .WORD   TU10$           ;POINTER TO FUNCTION TABLE FOR THE TU10
1214   173664  173616                           .WORD   TU56$           ;POINTER TO FUNCTION TABLE FOR THE TU56
1215   173666  173620                           .WORD   RK05$           ;POINTER TO FUNCTION TABLE FOR THE RK05
1216   173670  173620                           .WORD   RP03$           ;POINTER TO FUNCTION TABLE FOR THE RP03
1217   173672  173614                           .WORD   RK06$           ;POINTER TO FUNCTION TABLE FOR THE RK06
1218   173674  173622                           .WORD   TU16$           ;POINTER TO FUNCTION TABLE FOR RH11/TU16
1219   173676  173614                           .WORD   RP04$           ;POINTER TO FUNCTION TABLE FOR THE RH70/RP04 OR RH11/RP0
1220   173700  173615                           .WORD   RS04$           ;POINTER TO FUNCTION TABLE FOR THE RH70/RS04 OR RH11/RP0
1221   173702  173632                           .WORD   RX01$           ;POINTER TO FUNCTION TABLE FOR THE RX01
1222
1223                                    .SBTTL  STARTING ADDRESS TABLE
1224
1225   173704  173144                   ADDRS:  .WORD   TU10            ;STARTING ADDRESS FOR THE TM11/TU10
1226   173706  173124                           .WORD   TU56            ;STARTING ADDRESS FOR THE TC11/TU56
1227   173710  173576                           .WORD   RK05            ;STARTING ADDRESS FOR THE RK11/RK05
1228   173712  173204                           .WORD   RP03            ;STARTING ADDRESS FOR THE RP11/RP03
1229   173714  173260                           .WORD   RK06            ;STARTING ADDRESS FOR THE RK06
1230   173716  173336                           .WORD   TU16            ;STARTING ADDRESS FOR THE RH70/TU16 (800 BPI NRZI)
1231   173720  173272                           .WORD   RP04            ;STARTING ADDRESS FOR THE RH70/RP04 OR RH11/RP04
1232   173722  173464                           .WORD   RS04            ;STARTING ADDRESS FOR THE RH70/RS04 OR RH11/RS04
1233   173724  173500                           .WORD   RX01            ;STARTING ADDRESS FOR THE RX11/RX01
1234   173726  173416                           .WORD   PC11            ;STARTING ADDRESS FOR THE PC11
1235   173730  000000                           .WORD   0               ;RESERVED
1236   173732  000000                           .WORD   0               ;RESERVED
1237           000001                           .END
```

CROSS REFERENCE TABLE -- USER SYMBOLS

```
ADDRS   173704              966    1225#
AGAIN   173200              985    1009#  1042   1044   1147   1155
BASE1 = 165000              328#    342
BASE2 = 173000              328#    936
BASE3 = 173002              328#
BASE4 = 173224              328#   1032
BIT6  = 000100              328#
BOOT    173000              938#
BOOTMI  165754              840     893    910#
CHKSUM  173112              912     939    971#   1010
CHK240  173564             1151    1154#
CLRCS   173254             1040    1046#
CMDPTR  173662              965    1213#
CMNSGO  173206             1004    1022#  1127
CMNSRH  17347C             1064    1096   1126#
CMN1    173230             1029    1036#
CONT    165750              755     905#
CSRPTR  173636              964    1200#
CSRH1   173476             1127#   1163
DIAG    165000              353#    941
DISPLA= 177570              328#
FCE   = 001000              328#
GO1     173232             1037#   1038
GRP0  = 000030              328#    824    881
GRP1  = 000044              328#    845
JUMP    165760              902     909    912#
JUMP0   165746              716     902#
KIPAR0= 172340              328#
KIPAR7= 172356              328#
KIPDR0= 172300              328#
KIPDR7= 172316              328#
MISS  = 000014              328#    758    911
MMR0  = 177572              328#
MOL   = 010000              328#   1084
N     = 000003              343#    344    345    350    358#   359    360    365    375#   376    377    387    397#
                            398     399    409    418#   419    420    429    438#   439    440    449    456#   457
                            458     469    483#   484    485    495    502#   503    504    514    525#   526    527
                            538     548#   549    550    560    567#   568    569    580    592#   593    594    605
                            618#    619    620    630    645#   646    647    659    676#   677    678    688    699#
                            700     701    709    737#   738    739    750    800#   801    802    820    851#   852
                            853     869
PC11    173416             1101#   1234
RK05    173576             1161#   1227
RK05S   173620             1177#   1215
RK06    173260             1055#   1229
RK06S   173614             1172#   1217
RP03    173204              986    1016#  1228
RP03S   173620             1178#   1216
RP04    173272             1061#   1231
RP04S   173614             1173#   1219
RS04    173464             1122#   1232
RS04S   173615             1174#   1220
RX01    173500             1133#   1233
RX01S   173632             1192#   1221
SIZE    173310              753    1071#  1102
START   173014              946#    974
```

```
START1  173022            948#    973
START2  173034            947     952#    957
SWR   = 177570            328#    946
TST1    165000            351#
TST10   165126            480     496#
TST11   165136            499     515#
TST12   165154            522     539#
TST13   165172            545     561#
TST14   165202            564     581#
TST15   165224            589     606#
TST16   165246            615     631#
TST17   165300            642     660#
TST2    165004            355     366#
TST20   165334            673     689#
TST21   165352            696     710#
TST22   165436            751#
TST23   165544            821#
TST24   165644            870#
TST3    165020            372     388#
TST4    165036            394     410#
TST5    165052            415     430#
TST6    165066            435     450#
TST7    165076            453     470#
TUR   = 000001            328#
TU10    173144            992#   1225
TU10A   173172           1001#   1057
TU10S   173610           1168#   1213
TU16    173336           1082#   1230
TU16S   173622           1184#   1218
TU56    173124            980#   1226
TU56S   173616           1176#   1214
STN   = 000025            328#    343     352#    355     358     367#    372     375     389#    394     397     411#    415
                          418     431#    435     438     451#    453     456     471#    480     483     497#    499     502
                          516#    522     525     540#    545     548     562#    564     567     582#    589     592     607#
                          615     618     632#    642     645     661#    673     676     690#    696     699     711#    737
                          752#    800     822#    851     871#
.     = 173734            342#    936#   1032#
```

CROSS REFERENCE TABLE -- MACRO NAMES

```
COMMEN    328#    788     914
ENDCOM    328#    798     932
MSG1      343#    345
MSG10     483#    485
MSG11     502#    504
MSG12     525#    527
MSG13     548#    550
MSG14     567#    569
MSG15     592#    594
MSG16     618#    620
MSG17     645#    647
MSG2      358#    360
MSG20     676#    678
MSG21     699#    701
MSG22     737#    739
MSG23     800#    802
MSG24     851#    853
MSG3      375#    377
MSG4      397#    399
MSG5      418#    420
MSG6      438#    440
MSG7      456#    458
NXTTST    328#    343     358     375     397     418     438     456     483     502     525     548     567     592     618
          645     676     699     737     800     851
SKIP      328#    355     372     394     415     435     453     480     499     522     545     564     589     615     642
          673     696
STARS     328#    343     350     358     365     375     387     397     409     418     429     438     449     456     469
          483     495     502     514     525     538     548     560     567     580     592     605     618     630     645
          659     676     688     699     709     737     750     800     820     851     869
$$NXT     328#    343     358     375     397     418     438     456     483     502     525     548     567     592     618
          645     676     699     737     800     851
$$SKIP    328#    355     372     394     415     435     453     480     499     522     545     564     589     615     642
          673     696
```

. ABS. 173734   000

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

```
,DSKZ:DQM9AA.SEQ/SOL/CRF=DQM9AA.P11
RUN-TIME: 2 3 .2 SECONDS
RUN-TIME RATIO: 43/5=7.3
CORE USED:  8K  (15 PAGES)
```