

**PDP11/34**

**BASIC INSTRUCTION TEST  
MD-11-DFKAA-B**

**EP-DFKAA-B-DL-A**

**NOV 1976**

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**FICHE 1 OF 2**

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11/34 CPU TEST  
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IDENTIFICATION

PRODUCT CODE:	MAINDEC-11-DFKAA-B
PRODUCT NAME:	POP-11/34 CPU TEST
DATE CREATED:	OCTOBER 1976
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR: REVISED BY:	GLENN JOHNSON MARY MCNALLY AUGUST 1976

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\* SUMMARY OF OPERATING INSTRUCTIONS \*  
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THE FOLLOWING PROCEDURE CAN BE USED TO RUN THIS DIAGNOSTIC  
IN A STANDARD CONFIGURATION WITH AT LEAST 4K OF MEMORY  
AND A TELETYPE. IF THE PROGRAM DOES NOT RUN SUCCESSFULLY  
CONSULT THE FOLLOWING DOCUMENT FOR ASSISTANCE.

OPERATING PROCEDURES:

1. LOAD THE PROGRAM USING NORMAL PROCEDURES
2. START THE PROGRAM AT LOCATION 200
3. PROGRAM SHOULD PRINT "END OF PASS" WITHIN  
THE 1ST SECOND AND REPEATABLY THEREAFTER  
AT APPROX. 10 SEC. INTERVALS UNTIL  
EXTERNALLY HALTED.
4. IF THE PROGRAM DOES NOT RUN AS DESCRIBED ABOVE,  
CONSULT THE FULL OPERATING INSTRUCTIONS WHICH  
FOLLOW.

79 1.0 GENERAL PROGRAM INFORMATION  
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1281.1 PROGRAM PURPOSE

THIS DIAGNOSTIC PROGRAM IS DESIGNED TO BE A COMPREHENSIVE CHECK OF THE PDP-11/34 BASIC INSTRUCTION SET. THE PROGRAM EXERCISES ALL OF THE PROCESSOR LOGIC AND MICROCODE FOR ALL INSTRUCTIONS EXCEPT THE TRAP AND MEMORY MANAGEMENT INSTRUCTIONS. THE PROGRAM DOES NOT TEST INSTRUCTIONS OR HARDWARE RELATED TO THE TRAP OR INTERRUPT MECHANISMS OF THE 11/34 (E.G. RTT, RTI, WAIT, RESET, TRAP, EMT).

1.2 SYSTEM REQUIREMENTS1.2.1 HARDWARE

PDP-11/34 PROCESSOR  
8K MEMORY -- THE PROGRAM USES LOCATIONS 0 - 26214

1.2.2 SOFTWARE

THIS PROGRAM IS WRITTEN TO BE RUN AS A STAND-ALONE PROGRAM. HOWEVER, THE PROGRAM IS DESIGNED TO RUN UNDER AUTOMATED PRODUCT TEST SYSTEM (APT) IN ALL THREE MODES.

THE PROGRAM CAN ALSO BE RUN UNDER THE ACT 11 MONITOR

1.3 RELATED DOCUMENTS AND STANDARDS

PDP-11/34 MICROCODE LISTING

PDP-11/34 ELECTRICAL SCHEMATICS

DIAGNOSTIC ENGINEERING PROJECT PLANFOR 11/34

DIAGNOSTIC ENGINEERING STANDARDS AND CONVENTIONS PROGRAMMING PRACTICES  
DOCUMENT NO. 175-003-009-00

APT INTERFACE SPECIFICATION, REVISION 9.

1.4 DIAGNOSTIC HIERARCHY PREREQUISITES

NONE

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1.5 FAILURE ASSUMPTIONS

NONE

2.0 OPERATING INSTRUCTIONS2.1 LOADING AND STARTING PROCEDURES2.1.1 LOADING

USE NORMAL PROCEDURES FOR LOADING ABSOLUTE BINARY TAPES.

2.1.2 NORMAL STARTTHIS IS THE PROCEDURE FOR NORMAL PROGRAM RUNNING (I.E.,  
STARTING WITH TEST 1 AND EXECUTING ENTIRE DIAGNOSTIC).LOAD ADDRESS = 200  
START2.1.3 SUBTEST START

THIS IS THE PROCEDURE FOR STARTING AT A SUBTEST OTHER THAN 1.

1. LOAD STESTN (IN MAILBOX SECTION) WITH THE NUMBER OF SUBTEST  
MINUS ONE (IN OCTAL) FOR EXAMPLE, TO START AT SUBTEST 100,  
STESTN=77.
2. LOAD STARTING ADDRESS OF SUBTEST IN LOC. 216
3. LOAD ADDRESS = 204
4. START

2.2 SPECIAL ENVIRONMENTSTHIS PROGRAM IS WRITTEN TO COMPLY WITH ALL THE REQUIREMENTS  
OF THE APT INTERFACE SPECIFICATION. IT WILL RUN UNDER APT  
IN EITHER QUICK VERIFY, PROGRAM OR RUN-TIME MODES.THIS PROGRAM IS WRITTEN TO COMPLY WITH ALL OF THE REQUIREMENTS  
OF PROGRAMS TO RUN UNDER THE ACT11 MONITOR.

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2.3 PROGRAM OPTIONS

THIS PROGRAM IS INTENDED TO BE A BASIC PROCESSOR TEST.  
IT IS INTENDED TO BE THE LOWEST LEVEL DIAGNOSTIC RUN.  
IT PROVIDES FOR NO SELECTABLE OPTIONS.

IN ORDER THAT THE TEST BE RUNNABLE ON A PROCESSOR WITHOUT A  
TELETYPE, IT IS POSSIBLE TO SUPPRESS THE END OF PASS MESSAGE.  
IF NO TELETYPE IS AVAILABLE, ALTER THE BYTE, SENVM, WHICH  
IS LOCATED IN THE APT MAILBOX. SETTING SENVM TO 40(8) WILL  
SUPPRESS ALL CONSOLE OUTPUT.  
THE EXACT LOCATION OF THIS BYTE CAN BE FOUND IN THE SYMBOL  
TABLE AT THE END OF THE LISTING.

2.4 EXECUTION TIMES

THE DIAGNOSTIC COMPLETES THE FIRST PASS IN LESS THAN 1 SEC.  
SUBSEQUENT PASSES REQUIRE APPROXIMATELY 10 SECS. EACH.  
THE PROGRAM WILL RUN CONTINUOUSLY UNTIL EXTERNALLY HALTED.

3.0 ERROR INFORMATION3.1 ERROR TYPES

THERE ARE TWO BASIC TYPES OF ERRORS IN THE DIAGNOSTIC.

3.1.1 FUNCTIONAL ERRORS

THESE ARE ERRORS WHICH REPRESENT A MALFUNCTION OF AN  
INSTRUCTION OR SEQUENCE OF INSTRUCTION. (E.G., THE PROPER  
CONDITION CODE NOT SET OR IMPROPER RESULT OF AN ARITHMETIC  
OR LOGICAL OPERATION).

3.1.2 SEQUENCE ERRORS

THE RESULT OF A TESTS BEING EXECUTED OUT OF SEQUENCE. (E.G.  
WILD MACHINE OR IMPROPER BRANCH OR JUMP).

3.2 ERROR REPORTING PROCEDURES

THE DIAGNOSTIC RESPONDS TO THE DETECTION OF ALL ERRORS BY  
STORING CERTAIN INFORMATION IN MEMORY AND HALTING THE PROCESSOR.  
THE INFORMATION STORED IN MEMORY CAN BE USED BY THE OPERATOR  
TO IDENTIFY THE ERROR DETECTED.

CERTAIN FAILURES WILL CAUSE THE PROCESSOR TO HANG.  
THIS TYPE OF FAILURE IS INDICATED IF THE PROGRAM

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DUES NOT PRINT ITS END OF PASS INDICATION WITHIN A REASONABLE  
AMOUNT OF TIME. (FIRST MESSAGE SHOULD APPEAR WITHIN 1 SEC.)

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3.3 ERROR DESCRIPTOR INFORMATION

THE DIAGNOSTIC MAILBOX HOLDS THE ERROR INFORMATION NECESSARY TO IDENTIFY THE DETECTED ERROR. THIS INFORMATION HAS BEEN DESIGNED FOR COMPLIANCE WITH THE APT TO DIAGNOSTIC INTERFACE SPECIFICATION. IT IS THE PRIMARY MEDIUM FOR IDENTIFYING ERRORS.

3.2.1 \$MSGTYP

THIS LOCATION IS INCREMENTED FROM ZERO TO ONE BEFORE THE PROGRAM COMES TO A PROGRAMMED HALT. IF THIS LOCATION IS NOT ONE, THEN THE DIAGNOSTIC HAS COME TO AN UNPROGRAMMED HALT. CHECK THE STACK AND PC FOR A CLUE TO THE CAUSE. SUSPECT A TRAP.

3.2.2 \$FATAL

THIS LOCATION IS LOADED WITH A NUMBER BEFORE A HALT IS EXECUTED. EACH PROGRAMMED HALT HAS A UNIQUE NUMBER ASSOCIATED WITH IT WHICH CAN BE USED TO IDENTIFY THE ERROR WHICH HAS BEEN DETECTED.

3.2.3 \$PASS

THIS LOCATION IS INCREMENTED FOR EVERY COMPLETE PASS OF THE DIAGNOSTIC. MONITORING THIS LOCATION WILL INDICATE WHETHER OR NOT THE PROGRAM IS HUNG. IT WILL ALSO INDICATE THE NUMBER OF SUCCESSFUL PASSES COMPLETED BEFORE THE ERROR HALT. A HIGH PASS COUNT MIGHT INDICATE THAT THE ERROR HALT IS ASSOCIATED WITH AN INTERMITTANT FAULT.

3.2.4 \$TESTN

THIS LOCATION IS INCREMENTED IN EACH NEW SUBTEST. THIS SHOULD INDICATE THE TEST BEING EXECUTED WHEN THE ERROR WAS DETECTED. THIS LOCATION IS ALSO USED TO DETECT A SEQUENCE ERROR.

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### 3.4      ERROR IDENTIFICATION

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BECAUSE OF THE OVERHEAD ASSOCIATED WITH EACH HALT IN AN APT COMPATIBLE PROGRAM THE SEQUENCE CHECK CODE WILL SHARE THE ERROR HALT OF FUNCTIONAL ERROR WITHIN EACH SUBTEST. TO DETERMINE WHICH ERROR IS BEING REPORTED, LOCATIONS \$FATAL AND \$TESTN ARE USED TOGETHER. WHEN AN ERROR HALT OCCURS, CHECK \$FATAL TO DETERMINE THE NUMBER OF THE ERROR DETECTED. NOW, CHECK THAT THE TEST NUMBER WHERE THIS ERROR IS DETECTED CORRESPONDS TO THE VALUE IN \$TESTN. IF THESE AGREE THE ERROR WAS A FUNCTIONAL ERROR AS DESCRIBED IN THE LISTINGS. IF THESE NUMBERS DO NOT AGREE, THEN A SEQUENCE ERROR WAS DETECTED. IN THIS CASE \$TESTN WILL CONTAIN ONE MORE THAN THE NUMBER OF THE LAST TEST SUCCESSFULLY COMPLETED. SEQUENCE ERRORS WHICH SHARE THE ERROR HALTS OF FUNCTIONAL ERRORS WILL ALWAYS BE REPORTED BY THE LAST HALT IN THE SUBTEST IN WHICH THEY WERE DISCOVERED.

### 4.0      PROGRESS REPORT

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AT THE END OF EACH SUCCESSFUL PASS (THE EQUIVALENT OF 400 (8) PROGRAM PASSES, EXCEPT THE FIRST PASS WHICH IS ONLY ONE PROGRAM PASS) THE PROGRAM INCREMENTS THE LOCATION \$PSS WHICH IS IN THE APT MAILBOX. THIS LOCATION WILL ALWAYS CONTAIN THE NUMBER OF SUCCESSFUL PASSES COMPLETED. \$PSS IS RESET WITH EVERY RESTART FROM LOC. 200.

ADDITIONALLY, THE MESSAGE END OF DFKAA IS PRINTED ON THE CONSOLE TELETYPE AFTER THE FIRST PASS AND FOLLOWING EVERY SUBSEQUENT PASS (400 PROGRAM LOOPS) THEREAFTER.

IF NO TELETYPE IS AVAILABLE, THE CONSOLE OUTPUT MUST BE SUPPRESSED. (SEE SECTION 2.3).

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5.0 TROUBLE SHOOTING

WHEN THE PROGRAM DISCOVERS A FAULT IT WILL HALT. TO DETERMINE THE CAUSE OF THE HALT, THE DIAGNOSTIC PROVIDES ERROR INFORMATION. THIS INFORMATION IS STORED IN THE APT MAILBOX AND IS THE PRIMARY SOURCE OF ERROR IDENTIFICATION.

UPON FINDING AN ERROR, THE FOLLOWING PROCEDURE SHOULD AID IN ISOLATING THE FAULT.

5.1 CHECK THE MAILBOX

1. \$MSGTY THIS LOCATION SHOULD CONTAIN A 1. IF THE PROCESSOR HALTS AND THIS LOCATION IS ZERO, THEN THE PROCESSOR HAS COME TO AN UNEXPECTED HALT. FIRST SUSPECT A TRAP. CHECK THE PC AND IF A TRAP CHECK R6 AND THE STACK FOR THE LOCATION OF THE FAILING INSTRUCTION.

2. \$FATAL THIS LOCATION IS USED TO HOLD THE NUMBER OF THE ERROR WHICH HAS DETECTED. EACH ERROR BEING CHECKED BY THE DIAGNOSTIC IS ASSIGNED A UNIQUE NUMBER WHICH IS STORED IN \$FATAL WHEN THAT ERROR IS DETECTED.

WHEN AN ERROR IS DETECTED, CHECK THE LISTING TO SEE THAT THE ERROR NUMBER STORED IN \$FATAL IS ONE WHICH IS DETECTED IN THE TEST WHOSE NUMBER IS IN \$TESTN. IF THERE IS A DISAGREEMENT THEN THE ERROR BEING REPORTED IS A SEQUENCE ERROR. \$TESTN CONTAINS ONE MORE THAN THE LAST TEST WHICH WAS SUCCESSFULLY COMPLETED.

3. \$TESTN THIS LOCATION IS USED TO INDICATE THE NUMBER OF THE TEST WHICH WAS BEING EXECUTED WHEN THE FAULT WAS DETECTED. \$TESTN IS USED IN CONJUNCTION WITH \$FATAL TO DISTINGUISH BETWEEN SEQUENCE AND FUNCTIONAL ERRORS. (SEE 2. THIS SECTION)

4. \$PSS THIS LOCATION IS USED TO INDICATE THE NUMBER OF SUCCESSFUL PASSES WHICH THE DIAGNOSTIC HAS COMPLETED. THIS WILL GIVE AN INDICATION THAT THE DIAGNOSTIC HAS NOT JUST BEEN HUNG IN A LOOP IF NOT TELETYPE IS AVAILABLE TO REPORT THE PRINTED PROGRESS REPORTS.

IF AN ERROR HAS BEEN DETECTED \$PSS WILL SHOW WHETHER IT WAS A HARD ERROR DISCOVERED DURING THE FIRST TRY OR WHETHER IT WAS INTERMITTANT OR DEVELOPED DURING THE RUNNING OF THE DIAGNOSTIC.

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371 WHILE THIS DIAGNOSTIC IS PRIMARILY INTENDED TO BE A FAULT DETECTION  
372 PROGRAM, PROVISIONS ARE MADE TO ASSIST A TECHNICIAN WHO MIGHT WANT  
373 TO USE THE PROGRAM AS A TROUBLE SHOOTING TEST.  
374  
375 THE PROCEDURE FOR SCOPING A SUBTEST INVOLVES MODIFYING SEVERAL  
376 MEMORY LOCATIONS IN THE TEST ITSELF. THE PHILOSOPHY IS TO PROVIDE  
377 A SCOPING LOOP WHICH WILL INCLUDE THE CODE WHERE THE ERROR WAS DETECTED.  
378 THE LOOP IS SET UP SO THAT THE LOOP WILL NOT BE TERMINATED SHOULD  
379 THE ERROR INTERMITTANTLY DISAPPEAR.  
380  
381 THE PROCEDURE IS AS FOLLOWS:  
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383 1. DETERMINE WHICH ERROR IS TO BE SCOPED. USE \$FATAL AND \$TESTN  
384 FOR THIS (SEE ABOVE)  
385  
386 2. LOCATE THE ERROR ROUTINE IN THE LISTING.  
387  
388 3. CLEAR THE RIGHT BYTE OF THE CONDITIONAL BRANCH INSTRUCTION  
389 ASSOCIATED WITH THE ERROR. (THIS IS MARKED WITH <===='S IN THE  
390 LISTING.)  
391  
392 4. REPLACE THE INSTRUCTION FOLLOWING (MOV #XXX,-(R2)) WITH THE  
393 SCOPING BRANCH PROVIDED IN THE LISTING COMMENTS.  
394  
395 5. RESTART THE PROGRAM. THE PROGRAM MAY BE RESTARTED FROM THE  
396 BEGINNING OR FROM THE SUBTEST (SEE 2.0).  
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398 6.0 LISTING  
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409 000240  
410 000007  
411 000006  
412 177776  
413 177564  
414 177566  
415 140000  
416 030000  
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422 .MCALL .SAPTHOR,.SAPTBLS,.SACT11  
.SBTTL ACT11 HOOKS  
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;HOOKS REQUIRED BY ACT11  
\$SVPC=. ;SAVE PC

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423      000046      .=46
424      000046      $SENDAD          ;;1)SET LOC.46 TO ADDRESS OF SENDAD IN .SEOP
425      000052      .=52
426      000052      .WORD 0          ;;2)SET LOC.52 TO ZERO
427      000400      .=$$VPC           ;; RESTORE PC
428      000300      .=300
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432      .SBTTL APT MAILBOX-ETABLE
433
434      000300      *****EVEN*****
435      000300      $MAIL:             ;;APT MAILBOX
436      000302      $MSGTY: .WORD AMSGY ;;MESSAGE TYPE CODE
437      000304      $FATAL: .WORD AFATAL ;;FATAL ERROR NUMBER
438      000306      $TESTN: .WORD ATESN ;;TEST NUMBER
439      000308      $PASS:  .WORD APASS  ;;PASS COUNT
440      000310      $DEVCT: .WORD ADEVCT ;;DEVICE COUNT
441      000312      $UNIT:  .WORD AUNIT  ;;I/O UNIT NUMBER
442      000314      $MSGAD: .WORD AMGAD ;;MESSAGE ADDRESS
443      000316      $MSGLG: .WORD AMGLG ;;MESSAGE LENGTH
444      000320      $TABLE:            ;;APT ENVIRONMENT TABLE
445      000321      $ENV:   .BYTE AENV   ;;ENVIRONMENT BYTE
446      000322      $ENV1:  .BYTE AENVM  ;;ENVIRONMENT MODE BITS
447      000324      $SWREG: .WORD ASWREG ;;APT SWITCH REGISTER
448      000326      $USR:   .WORD AUSWR ;;USER SWITCHES
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454      000330      $CPUOP: .WORD ACPUOP ;;CPU TYPE,OPTIONS
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459      000330      :*               11/04=01,11/05=02,11/20=03,11/40=04,11/45=05
460
461      000330      :*               11/70=06,PDQ=07,Q=10
462      000024      :*               BIT 10=REAL TIME CLOCK
463      000024      :*               BIT 9=FLOATING POINT PROCESSOR
464      000024      :*               BIT 8=MEMORY MANAGEMENT
465      000044      $ETEND:           ;;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
466      000044      .MEXIT
467      000044      .SBTTL APT PARAMETER BLOCK
468
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471      000330      *****SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT*****
472      000330      .SX=.             ;;SAVE CURRENT LOCATION
473      000330      .=24             ;;SET POWER FAIL TO POINT TO START OF PROGRAM
474      000330      200              ;;FOR APT START UP
475      000330      .=44             ;;POINT TO APT INDIRECT ADDRESS PNTR.
476      000330      $APTHDR:        ;;POINT TO APT HEADER BLOCK
477      000330      .=.SX            ;;RESET LOCATION COUNTER
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M01

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479 :SOME POINTERS TO CPU TRAP HANDLERS
480 ;*****
481 000004 =4
482 000004 026116 t04
483 000006 000000 0
484 000010 026126 T010
485 000012 000000 0
486 000014 026136 T014
487 000030 000030 =30
488 000030 026146 T030
489 000032 000000 0
490 000034 026156 T034
491 000036 000000 0
492 000114 =114
493 000114 026166 T0114
494 000116 000000 0
495 000244 =244
496 000244 026176 T0244
497 000246 000000 0
498 000250 026206 T0250
499 000252 000000 0
500

501 ;*****
502 ;DATA TABLE FOR USE IN ADDRESSING MODE TESTS
503 ;*****
504 000370 =370
505 000370 000000 000000 0,0,0,0,0,0
506 000376 000000 000000 000000
507 000404 000001 000001 177777 1,1,-1
508 000500 =500
509 ;*****
510 ;SET UP STARTING ADDRESS
511 000500 .SX=
512 000200 =200
513 000200 000167 000274 JMP START
514
515 000204 012706 000500 MOV #STBOT,R6 ;SET STACK POINTER
516 000210 012702 000304 MOV #TESTN,R2 ;SET MAILBOX POINTER
517 000214 000137 JMP @PC+ ;JUMP TO SUBTEST
518 000216 000000 O ;ADDR. OF SUBTEST GOES HERE
519
520 000500 =.SX
521 000302 SERROR=$FATAL
522 000304 $STSTNM=$TESTN -
523 000500 012737 026002 000024 START: MOV #PWRDN,@#24 ;SET UP FOR POWER FAIL
524 000506 012737 000000 000306 MOV #0,@$PASS ;CLEAR PASS COUNT
525 000514 012737 177777 025652 MOV #-1,@$PASSPT ;SET PRINT COUNTER
526 000522 012706 000500 RESTRT: MOV #STBOT,R6 ;INITIALIZE STACK POINTER
527 000526 012702 000304 MOV #TESTN,R2 ;SET UP POINTER TO MESSAGE TYPE
528 000532 012737 000000 000304 MOV #0,@$STSTNM ;CLEAR TEST NUMBER
529 000540 012737 000000 000302 MOV #0,@$ERROR ;CLEAR ERROR NUMBER
530 000546 012737 000000 000300 MOV #0,@$MSGTY ;CLEAR MESSAGE TYPE(FOR APT)

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NO1

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531
532 ;TEST 1 CHECK BRANCHES ON Z BIT
533 ;*****
534 000554 005212 000001 TST1: INC (R2) ;UPDATE TEST NUMBER
535 000556 022712 000001 CMP #1,(R2) ;SEQUENCE ERROR?
536 000562 001024 BNE TST2-10 ;BR TO ERROR HALT ON SEQ ERROR
537 000564 000257 CCC ;CLEAR ALL CONDITION CODES
538 000566 001401 BEQ BR1 ;SHOULD BRANCH
539 000570 000404 BR  BR2 ;BAD BRANCH OF Z-BIT
540 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
541 ;BRANCH INSTRUCTION AND <=====
542 ;REPLACE THE MOVE INSTRUCTION <=====
543 ;FOLLOWING W/ 774 <=====

544 000572 012742 000001 BR1: MOV *1,-(R2) ;MOVE TO MAILBOX * ***** 1 *****
545 000572 012742 000001 INC -(R2) ;SET MSGTYP TO FATAL ERROR
546 000576 005242 HALT ;SHOULD HAVE BRANCHED: Z=0
547 000600 000000
548 000602 001004 BR2: BNE BR3 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
549 ;CONDITIONAL BRANCH INST. AND <=====
550 ;REPLACE THE MOVE INSTRUCTION <=====
551 ;WHICH FOLLOWS W/ 770 <=====

552 000604 012742 000002 BR3: MOV *2,-(R2) ;MOVE TO MAILBOX * ***** 2 *****
553 000610 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
554 000612 000000 HALT ;
555 000614 000264 SEZ ;
556 000616 001001 BNE BR4 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
557 000620 000404 BR  BR5 ;BRANCH INSTRUCTION, AND <=====
558 ;REPLACE THE MOVE INSTRUCTION <=====
559 ;FOLLOWING W/ 760 <=====

560 000622 012742 000003 BR4: MOV *3,-(R2) ;MOVE TO MAILBOX * ***** 3 *****
561 000622 012742 000003 INC -(R2) ;SET MSGTYP TO FATAL ERROR
562 000626 005242 HALT ;SHOULD NOT HAVE BRANCHED HERE ON Z=1
563 000630 000000
564 000632 001404 BR5: BEQ TST2 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
565 ;CONDITIONAL BRANCH INST. AND <=====
566 ;REPLACE THE MOVE INSTRUCTION <=====
567 ;WHICH FOLLOWS W/ 754 <=====

568 000632 001404
569 000634 012742 000004 MOV *4,-(R2) ;MOVE TO MAILBOX * ***** 4 *****
570 000640 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
571 000642 000000 HALT ;SHOULD HAVE BRANCHED ON Z=1
572 ;OR SEQUENCE ERROR
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 SBTTL DATA PATH TESTS

THE DATA PATH TESTS ARE USED TO VERIFY THAT VARIOUS DATA PATTERNS CAN BE SUCCESSFULLY MOVED THROUGH THE DATA PATHS. MOVE AND COMPARE MODE 2,3 INSTRUCTIONS ARE USED TO PASS AND TEST VARIOUS DATA PATTERNS IN THE DATA PATHS.

THE TEST EXERCISES THE INTERNAL DATA PATHS, THE UNIBUS DATA TRANSCIEVERS, AND AMUX CONTROL FOR ALU AND UBUS INPUTS.

IF THESE TESTS FAIL, EXAMINE THE TARGET LOCATION (LOC. 0) TO SEE WHICH BITS OF THE DATA PATH ARE FAILING. IF THIS PROVIDES INCONCLUSIVE DATA, TRY TO CHECK MODE 3 IR DECODE BY RUNNING JUST THE MICROCODE AND IR DECODE TESTS FOR THE MOVE AND COMPARE INSTRUCTIONS.

 \*\*\*\*\*  
 TEST 2 TEST OF ZEROES IN THE DATA PATH

596 000644 005212	000002	TST2: INC (R2)	UPDATE TEST NUMBER
597 000646 022712		CMP #2-(R2)	SEQUENCE ERROR?
598 000652 001006		BNE TST3-10	BR TO ERROR HALT ON SEQ ERROR
599 000654 012737	000000 000000	MOV #0, #00	MOVE ZEROES THRU ADDRESS LINES, DATA
600			LINES AND INTERNAL PATHS
601 000662 005737	000000	TST #0	SUCCESSFUL?
602 000666 001404		BEQ TST3	
			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 772
607 000670 012742	000005	MOV #5-(R2)	MOVE TO MAILBOX * ***** 5 *****
608 000674 005242		INC -(R2)	SET MSGTYP TO FATAL ERROR
609 000676 000000		HALT	DATA INCORRECT ; OR SEQUENCE ERROR

 \*\*\*\*\*  
 TEST 3 TEST OF PATTERN 125252 IN DATA PATH

615 000700 005212	000003	TST3: INC (R2)	UPDATE TEST NUMBER
616 000702 022712		CMP #3-(R2)	SEQUENCE ERROR?
617 000706 001007		BNE TST4-10	BR TO ERROR HALT ON SEQ ERROR
618 000710 012737	125252 000000	MOV #125252, #00	MOVE ALTERNATING ONES AND ZEROES
619			THRU DATA PATHS
620 000716 022737	125252 000000	CMP #125252, #00	SUCCESSFUL
621 000724 001404		BEQ TST4	
			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 771
626 000726 012742	000006	MOV #6-(R2)	MOVE TO MAILBOX * ***** 6 *****
627 000732 005242		INC -(R2)	SET MSGTYP TO FATAL ERROR
628 000734 000000		HALT	DATA INCORRECT ; OR SEQUENCE ERROR

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DFKAA.B.P11 T3 TEST OF PATTERN 125252 IN DATA PATH

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630
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634 000736 005212 :***** TEST 4 TEST OF PATTERN 052525 IN DATA PATH *****
635 000740 022712 000004 TST4: INC   (R2)      ;UPDATE TEST NUMBER
636 000744 001007      CMP   #4,(R2)    ;SEQUENCE ERROR?
637 000746 012737 052525 000000 BNE   TST5-10   ;BR TO ERROR HALT ON SEQ ERROR
638                               MOV   #052525,0$0  ;MOVE ALTERNATING ZEROS AND ONES
639 000754 022737 052525 000000      CMP   #052525,0$0  ;THRU DATA PATH
640 000762 001404      BEQ   TST5    ;SUCCESSFUL?
641                               ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
642                               ; CONDITIONAL BRANCH INST. AND      <=====
643                               ; REPLACE THE MOVE INSTRUCTION      <=====
644                               ; WHICH FOLLOWS W/ 771      <=====
645 000764 012742 000007      MOV   #7,-(R2)   ;MOVE TO MAILBOX 8 ***** 7 *****
646 000770 005242      INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
647 000772 000000      HALT
648
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653 000774 005212 :***** TEST 5 TEST OF ALL ONES IN DATA PATH *****
654 000776 022712 000005 TST5: INC   (R2)      ;UPDATE TEST NUMBER
655 001002 001007      CMP   #5,(R2)    ;SEQUENCE ERROR?
656 001004 012737 177777 000000 BNE   TST6-10   ;BR TO ERROR HALT ON SEQ ERROR
657 001012 022737 177777 000000 MOV   #177777,0$0  ;MOVE ONES THRU DATA PATH
658 001020 001404      CMP   #177777,0$0  ;SUCCESSFUL
659                               BEQ   TST6    ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
660                               ; CONDITIONAL BRANCH INST. AND      <=====
661                               ; REPLACE THE MOVE INSTRUCTION      <=====
662                               ; WHICH FOLLOWS W/ 771      <=====
663 001022 012742 000010      MOV   #10,-(R2)  ;MOVE TO MAILBOX 8 ***** 10 *****
664 001026 005242      INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
665 001030 000000      HALT
666

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667  
 668 :\*\*\*\*\*  
 669 :SBTTL B-REGISTER TEST  
 670 :  
 671 : THE B-REGISTER SHIFTING LOGIC TESTS ARE USED TO TEST THAT THE  
 672 : B-REGISTER CAN HOLD VARIOUS DATA PATTERNS AND THAT THE ASSOCIATED  
 673 : LOGIC SUPPORTS THE SHIFTING FUNCTIONS WITHIN THE B-REGISTER AND C-BIT.  
 674 : A ONE IS SHIFTED THROUGH EVERY BIT IN THE B-REGISTER AND C-BIT IN  
 675 : BOTH DIRECTIONS.  
 676 : THE B-REGISTER ITSELF IS TESTED IN ITS ABILITY AS A BUFFER AND AS  
 677 : A SHIFT REGISTER. DATA IS ALSO PASSED THROUGH THE DATA PATH AND ALU.  
 678 : IF THESE TESTS FAIL, EXAMINE THE TARGET LOCATION (LOC. 0) TO SEE  
 679 : WHICH BITS OF THE B-REGISTER MAY BE FAILING. IF THIS PROVIDES  
 680 : INCONCLUSIVE DATA TRY TO CHECK THE MODE 3 IR DECODE BY RUNNING JUST  
 681 : THE MICROCODE AND IR DECODE TESTS FOR THE PARTICULAR INSTRUCTIONS.  
 682  
 683 :\*\*\*\*\*  
 684 :TEST 6 SHIFT BIT 0 TO BIT 1  
 685 :\*\*\*\*\*  
 686 001032 005212 000006 TST6: INC (R2) ;UPDATE TEST NUMBER  
 687 001034 022712 000006 CMP #6,(R2) ;SEQUENCE ERROR?  
 688 001040 0C1012 BNE TST7-10 ;BR TO ERROR HALT ON SEQ ERROR  
 689 001042 000241 CLC ;CLEAR CARRY BIT  
 690 001044 012737 000001 000000 MOV #1,3#0 ;LOAD A 1  
 691 001052 006137 000000 ROL #0 ;SHIFT LEFT  
 692 001056 022737 000002 000000 CMP #2,3#0 ;SUCCESSFUL  
 693 001064 001404 BEQ TST7 ;  
 694 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 695 ; CONDITIONAL BRANCH INST. AND <=====  
 696 ; REPLACE THE MOVE INSTRUCTION <=====  
 697 ; WHICH FOLLOWS W/ 766 <=====  
 698 001066 012742 000011 MOV #11,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 11 \*\*\*\*\*  
 699 001072 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 700 001074 000000 HALT ;BIT 1 NOT SET  
 701 ; OR SEQUENCE ERROR  
 702  
 703 :\*\*\*\*\*  
 704 :TEST 7 SHIFT CARRY INTO BIT 0  
 705 :\*\*\*\*\*  
 706 001076 005212 000007 TST7: INC (R2) ;UPDATE TEST NUMBER  
 707 001100 022712 000007 CMP #7,(R2) ;SEQUENCE ERROR?  
 708 001104 001017 BNE TST10-10 ;BR TO ERROR HALT ON SEQ ERROR  
 709 001106 012737 000000 000000 MOV #0,3#0 ;CLEAR LOCATION  
 710 001114 000261 SEC ;SET CARRY  
 711 001116 006137 000000 ROL #0 ;ROTATE CARRY BIT TO BIT 0  
 712 001122 103C14 BCC TST10 ;  
 713 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 714 ; CONDITIONAL BRANCH INST. AND <=====  
 715 ; REPLACE THE MOVE INSTRUCTION <=====  
 716 ; WHICH FOLLOWS W/ 771 <=====  
 717 001124 012742 000012 MOV #12,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 12 \*\*\*\*\*  
 718 001130 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 719 001132 000000 HALT ;CARRY CLEAR  
 720 ; OR SEQUENCE ERROR  
 721 001134 022737 000001 000000 CMP #1,3#0 ;BIT 0 SET  
 722 001142 001404 BEQ TST10 ;

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DFKAA.B.F11 T7 SHIFT CARRY INTO BIT 0

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723 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
724 ; CONDITIONAL BRANCH INST. AND      <=====
725 ; REPLACE THE MOVE INSTRUCTION      <=====
726 ; WHICH FOLLOWS W/ 761      <=====

727 001144 012742 000013          MOV    #13,-(R2)
728 001150 005242              INC    -(R2)
729 001152 000000              HALT
730
731
732 ;*****TEST 10 LEFT SHIFT FROM BIT 0 TO C-BIT*****
733 ;*****TEST 10 LEFT SHIFT FROM BIT 0 TO C-BIT*****
734 ;*****TEST 10 LEFT SHIFT FROM BIT 0 TO C-BIT*****
735 001154 005212          TST10: INC    (R2)
736 001156 022712 000010          CMP    #10,(R2)
737 001162 001014          BNE    TST11-10
738 001164 012737 000001 000000          MOV    #1,0#0
739 001172 012700 177757          MOV    #-21,R0
740 001176 000241          CLC
741 001200 005200          SHL:   INC    R0
742 001202 001404          BEQ    SHLE
743 001204 006137 000000          ROL    0#0
744 001210 103373          BCC    SHL
745 001212 001404          BEQ    TST11
746 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
747 ; CONDITIONAL BRANCH INST. AND      <=====
748 ; REPLACE THE MOVE INSTRUCTION      <=====
749 ; WHICH FOLLOWS W/ 764      <=====

750 001214 012742 000014          SHLE: MOV    #14,-(R2)
751 001220 005242              INC    -(R2)
752 001222 000000              HALT
753
754
755 ;*****TEST 11 SHIFT BIT 15 TO BIT 14*****
756 ;*****TEST 11 SHIFT BIT 15 TO BIT 14*****
757 ;*****TEST 11 SHIFT BIT 15 TO BIT 14*****
758 ;*****TEST 11 SHIFT BIT 15 TO BIT 14*****
759 001224 005212          TST11: INC    (R2)
760 001226 022712 000011          CMP    #11,(R2)
761 001232 001012          BNE    TST12-10
762 001234 012737 100000 000000          MOV    #100000,0#0
763 001242 000241          CLC
764 001244 006037 000000          ROR    0#0
765 001250 022737 040000 000000          CMP    #40000,0#0
766 001256 001404          BEQ    TST12
767 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
768 ; CONDITIONAL BRANCH INST. AND      <=====
769 ; REPLACE THE MOVE INSTRUCTION      <=====
770 ; WHICH FOLLOWS W/ 766      <=====

771 001260 012742 000015          MOV    #15,-(R2)
772 001264 005242              INC    -(R2)
773 001266 000000              HALT
774
775
776 ;*****TEST 12 RIGHT SHIFT FROM BIT 15 TO C-BIT*****
777 ;*****TEST 12 RIGHT SHIFT FROM BIT 15 TO C-BIT*****
778 ;*****TEST 12 RIGHT SHIFT FROM BIT 15 TO C-BIT*****

```

MAINDEC-11-DFKAA-8 11-34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 245  
 DFKAA8.P11 T12 RIGHT SHIFT FROM BIT 15 TO C-BIT

779 001270 005212		TST12: INC (R2)	UPDATE TEST NUMBER
780 001272 022712	000012	CMP #12 (R2)	SEQUENCE ERROR?
781 001276 001014		BNE TST13-10	BR TO ERROR HALT ON SEQ ERROR
782 001300 012737	100000 000000	MOV #100000,3#0	SET BIT 15
783 001306 012700	177757	MOV #-21,R0	SET BIT COUNTER
784 001312 000241		CLC	CLEAR C-BIT
785 001314 005200		INC R0	INCREMENT BIT COUNTER
786 001316 001404		BEQ SHRE	BR TO ERROR HALT IF BIT IS LOST
787 001320 006037	000000	ROR #0	ROTATE RIGHT ONE POSITION
788 001324 103373		BCC SHR	BRANCH IF C-BIT CLEAR
789 001326 001404		BEQ TST13	
790			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
791			CONDITIONAL BRANCH INST. AND
792			REPLACE THE MOVE INSTRUCTION
793			WHICH FOLLOWS W/ 764
794 001330		SHRE:	
795 001330 012742	000016	MOV #16 -(R2)	; MOVE TO MAILBOX # ***** 16 *****
796 001334 005242		INC -(R2)	; SET MSGTYP TO FATAL ERROR
797 001336 000000		HALT	; RIGHT SHIFT LOGIC FAILED
798			; OR SEQUENCE ERROR

799  
 800 :\*\*\*\*\*  
 801 .SBTTL SCRATCH PAD TESTS  
 802 :  
 803 THE SCRATCH PAD TESTS ARE USED TO VERIFY THAT VARIOUS  
 804 DATA PATTERNS CAN BE SUCCESSFULLY HELD IN THE SCRATCH PAD  
 805 CIRCUITRY. MOVE AND COMPARE INSTRUCTIONS ARE USED TO TEST THAT  
 806 R0 CAN HOLD VARIOUS DATA PATTERNS. EACH DATA PATTERN IS  
 807 MOVED AND TESTED IN A SMALL LOOP CONVENIENT FOR SCOPING. THE  
 808 SUCCESSFUL COMPLETION OF THESE TESTS SHOULD VERIFY THE CIRCUITRY EXTERNAL  
 809 TO THE SCRATCH PAD ITSELF.  
 810 THE REMAINDER OF THE GENERAL REGISTERS ARE TESTED BY MOVING  
 811 A BIT INTO BIT 0 OF THE REGISTER AND SHIFTING IT LEFT ONE  
 812 BIT AT A TIME INTO THE CARRY BIT. THE RESULT IS THEN CHECKED TO INSURE THAT  
 813 NO BITS WERE PICKED. THE PROCEDURE IS THEN REPEATED UNDER OPPOSITE  
 814 CONDITIONS. THE GENERAL REGISTER AND THE CARRY BIT ARE SET TO  
 815 ALL ONES, AND A ZERO IS SHIFTED LEFT FROM BIT 0 INTO THE CARRY BIT.  
 816 THE RESULT IS THEN CHECKED TO INSURE THAT NO ZEROES WERE PICKED.  
 817 AT THIS POINT ALL OF THE GENERAL REGISTERS HAVE BEEN EXERCISED  
 818 AS WELL AS REGISTER 11. REGISTERS 10 AND 12 HAVE BEEN ACCESSED BY  
 819 THE INSTRUCTIONS. REGISTERS 13,14,AND 17 WILL BE TESTED LATER IN THE  
 820 MICROCODE TESTS.  
 821 IF THE PATTERN TESTS WITH REGISTER 0 FAIL CHECK THE RESULTANT  
 822 DATA FOR A CLUE TO A FAULT IN THE EXTERNAL CIRCUITRY. IF THE  
 823 PATTERN TESTS WITH R0 ARE SUCCESSFUL BUT THE TESTS WITH THE OTHER  
 824 REGISTERS FAIL, SUSPECT THE REGISTER SELECT LINES AND THEN THE SCRATCH  
 825 PAD ITSELF.  
 826 :  
 827 :\*\*\*\*\*  
 828 :TEST 13 TEST IF R0 CAN HOLD ALL ZEROS  
 829 :\*\*\*\*\*  
 830 001340 005212 000013  
 831 001342 022712 000013  
 832 001346 001004 000000  
 833 001350 012700 000000  
 834 001354 005700 000000  
 835 001356 001404 000000  
 836 :  
 837 TST13: INC (R2) ;UPDATE TEST NUMBER  
 838 CMP #13, (R2) ;SEQUENCE ERROR?  
 839 BNE TST14-10 ;BR TO ERROR HALT ON SEQ ERROR  
 840 :  
 841 001360 012742 000017  
 842 001364 005242 000017  
 843 001366 000000 000000  
 844 :  
 845 MOV #17, -(R2) ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 846 INC -(R2) ;CONDITIONAL BRANCH INST. AND  
 847 HALT ;REPLACE THE MOVE INSTRUCTION  
 848 WHICH FOLLOWS W/ 774 <=====  
 849 :  
 850 :\*\*\*\*\*  
 851 :TEST 14 TEST IF R0 CAN HOLD ONES AND ZEROS  
 852 :\*\*\*\*\*  
 853 001370 005212 000014  
 854 001372 022712 000014  
 855 001376 001005 125252  
 856 001400 012700 125252  
 857 001404 020027 125252  
 858 001410 001404 000000  
 859 :  
 860 TST14: INC (R2) ;UPDATE TEST NUMBER  
 861 CMP #14, (R2) ;SEQUENCE ERROR?  
 862 BNE TST15-10 ;BR TO ERROR HALT ON SEQ ERROR  
 863 MOV #125252, R0 ;MOVE ALTERNATING ONES AND ZEROS TO R0  
 864 CMP R0, #125252 ;SUCCESSFUL?

```

855 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
856 ; CONDITIONAL BRANCH INST. AND <=====
857 ; REPLACE THE MOVE INSTRUCTION <=====
858 ; WHICH FOLLOWS W/ 773 <=====

859 001412 012742 000020           MOV    #20,-(R2)      ;MOVE TO MAILBOX # ***** 20 *****
860 001416 005242                 INC    -(R2)          ;SET MSGTYP TO FATAL ERROR
861 001420 000000                 HALT
862
863
864 ;***** TEST IS TEST IF RO CAN HOLD ZEROES AND ONES
865 ;***** TST15: INC (R2) ;UPDATE TEST NUMBER
866 ;***** CMP #15,(R2) ;SEQUENCE ERROR?
867 001422 005212 000015         BNE   TST16-10      ;BR TO ERROR HALT ON SEQ ERROR
868 001424 022712                 CMP    #15,(R2)
869 001430 001005                 BNE   TST16-10
870 001432 012700 052525         MOV    #052525,RO  ;MOVE ALTERNATING ZEROES AND ONES TO RO
871 001436 020027 052525         CMP    RO,#052525  ;SUCCESSFUL?
872 001442 001404                 BEQ   TST16
873
874 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
875 ; CONDITIONAL BRANCH INST. AND <=====
876 ; REPLACE THE MOVE INSTRUCTION <=====
877 ; WHICH FOLLOWS W/ 773 <=====

878 001444 012742 000021           MOV    #21,-(R2)      ;MOVE TO MAILBOX # ***** 21 *****
879 001450 005242                 INC    -(R2)          ;SET MSGTYP TO FATAL ERROR
880 001452 000000                 HALT
881
882 ;***** TEST 16 TEST IF RO CAN HOLD ALL ONES
883 ;***** TST16: INC (R2) ;UPDATE TEST NUMBER
884 ;***** CMP #16,(R2) ;SEQUENCE ERROR?
885 001454 005212 000016         BNE   TST17-10      ;BR TO ERROR HALT ON SEQ ERROR
886 001456 022712                 CMP    #16,(R2)
887 001462 001005                 BNE   TST17-10
888 001464 012700 177777         MOV    #177777,RO  ;MOVE ALL ONES TO RO
889 001470 020027 177777         CMP    RO,#177777  ;SUCCESSFUL?
890 001474 001404                 BEQ   TST17
891
892 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
893 ; CONDITIONAL BRANCH INST. AND <=====
894 ; REPLACE THE MOVE INSTRUCTION <=====
895 ; WHICH FOLLOWS W/ 773 <=====

896 001476 012742 000022           MOV    #22,-(R2)      ;MOVE TO MAILBOX # ***** 22 *****
897 001502 005242                 INC    -(R2)          ;SET MSGTYP TO FATAL ERROR
898 001504 000000                 HALT
899
900 ;***** TEST 17 TEST IF R1 CAN HOLD A ONE IN ALL BITS
901 ;***** TST17: INC (R2) ;UPDATE TEST NUMBER
902 ;***** CMP #17,(R2) ;SEQUENCE ERROR?
903 001506 005212 000017         BNE   TST20-10      ;BR TO ERROR HALT ON SEQ ERROR
904 001510 022712                 CMP    #17,(R2)
905 001514 001012                 BNE   TST20-10
906 001516 012701 000001         MOV    #1,R1          ;SET BIT 0
907 001522 012700 177757         MOV    #-21,RO        ;SET BIT COUNTER
908 001526 000241                 CLC
909 001530 005200                 REG1: INC    RO          ;CLEAR C-BIT
910 001532 001403                 BEQ   REG1E         ;INCREMENT BIT COUNTER
911
912 ; BR TO ERROR HALT IF BIT IS LOST

```

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DFKAAB.P11 T17 TEST IF R1 CAN HOLD A ONE IN ALL BITS

```

911 001534 006101          ROL   R1      ;ROTATE 1 POSITION
912 001536 103374          BCC   REG1    ;ALL DONE
913 001540 001404          BEQ   TST20   ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
914                                         ; CONDITIONAL BRANCH INST. AND <=====
915                                         ; REPLACE THE MOVE INSTRUCTION <=====
916                                         ; WHICH FOLLOWS W/ 766 <=====

918 001542               REG1E:    MOV   #23,-(R2) ;MOVE TO MAILBOX * ***** 23 *****
919 001542 012742 000023     INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
920 001546 005242           HALT
921 001550 000000           ;FAILURE WITH R1
922                                         ; OR SEQUENCE ERROR
923
924                                         ;*****TEST 20*****TEST IF R1 CAN HOLD A ZERO IN ALL BITS*****
925                                         ;*****TEST 20*****TEST IF R1 CAN HOLD A ZERO IN ALL BITS*****
926
927 001552 005212           TST20:   INC   (R2)    ;UPDATE TEST NUMBER
928 001554 022712 000020     CMP   #20,(R2) ;SEQUENCE ERROR?
929 001560 001014           BNE   TST21-10 ;BR TO ERROR HALT ON SEQ ERROR
930 001562 012701 177776     MOV   #-2,R1  ;SET ALL ONES IN R1 EXCEPT FOR BIT 0
931 001566 012700 177757     MOV   #-21,RO ;SET BIT COUNTER
932 001572 000261           SEC
933 001574 005200           REG1A:   INC   RO      ;INCREMENT COUNTER
934 001576 001405           BEQ   RIERR   ;BR TO ERROR HALT IF COUNTER=0
935 001600 006101           ROL   R1      ;ROTATE 1 POSITION
936 001602 103374           BCS   REG1A  ;CONTINUE UNTIL C-BIT IS CLEAR
937 001604 022701 177777     CMP   #-1,R1  ;CHECK DATA IN R1
938 001610 001404           BEQ   TST21   ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
939                                         ; CONDITIONAL BRANCH INST. AND <=====
940                                         ; REPLACE THE MOVE INSTRUCTION <=====
941                                         ; WHICH FOLLOWS W/ 764 <=====

943 001612               RIERR:    MOV   #24,-(R2) ;MOVE TO MAILBOX * ***** 24 *****
944 001612 012742 000024     INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
945 001616 005242           HALT
946 001620 000000           ;FAILURE WITH R1
947                                         ; OR SEQUENCE ERROR
948                                         ;*****TEST 21*****TEST IF R2 CAN HOLD A ONE IN ALL BITS*****
949                                         ;*****TEST 21*****TEST IF R2 CAN HOLD A ONE IN ALL BITS*****
950
951 001622 005212           TST21:   INC   (R2)    ;UPDATE TEST NUMBER
952 001624 022712 000021     CMP   #21,(R2) ;SEQUENCE ERROR?
953 001630 001012           BNE   REG2A-14 ;BR TO ERROR HALT ON SEQ ERROR
954 001632 012702 000001     MOV   #1,R2  ;SET BIT 0
955 001636 012700 177757     MOV   #-21,RO ;SET BIT COUNTER
956 001642 000241           CLC
957 001644 005200           REG2:   INC   RO      ;CLEAR C-BIT
958 001646 001403           BEQ   REG2A-14 ;INCREMENT BIT COUNTER
959 001650 006102           ROL   R2      ;BR TO ERROR HALT IF BIT IS LOST
960 001652 103374           BCC   REG2   ;ROTATE 1 POSITION
961 001654 001406           BEQ   REG2A  ;ALL DONE
962                                         ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
963                                         ; BRANCH INSTRUCTION AND <=====
964                                         ; REPLACE THE MOVE INSTRUCTION <=====
965                                         ; FOLLOWING W/ 771 <=====

966 001656 012702 000304     MOV   #TESTN,R2 ;RESTORE POINTER

```

## J02

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DFKAAB.P11 T21 TEST IF R2 CAN HOLD A ONE IN ALL BITS

```

967 001662 012742 000025           MOV    #25,-(R2)      ;MOVE TO MAILBOX * ***** 25 *****
968 001666 005242                  INC    -(R2)          ;SET MSGTYP TO FATAL ERROR
969 001670 000000                  HALT
970 001672 012702 000304           REG2A: MOV    #$TESTN,R2   ;FAILURE WITH R2
971                                         ;RESTORE POINTER
972                                         ;*****
973                                         ;TEST 22 TEST IF R2 CAN HOLD A ZERO IN ALL BITS
974                                         ;*****
975 001676 005212                  TST22: INC    (R2)        ;UPDATE TEST NUMBER
976 001700 022712 000022           CMP    #22,(R2)      ;SEQUENCE ERROR?
977 001704 001020                  BNE    TST23-10    ;BR TO ERROR HALT ON SEQ ERROR
978 001706 012702 177776           MOV    #-2,R2       ;SET ALL ONES IN R2 EXCEPT FOR BIT 0
979 001712 012700 177757           MOV    #-21,RO      ;SET BIT COUNTER
980 001716 000261                  SEC
981 001720 005200                  REG2B: INC    RO         ;INCREMENT BIT COUNTER
982 001722 001407                  BEQ    R2ERR       ;BR TO ERROR HALT IF COUNTER=0
983 001724 006102                  ROL    R2         ;ROTATE 1 POSITION
984 001726 103774                  BCS    REG2B       ;CONTINUE UNTIL C-BIT IS CLEAR
985 001730 022702 177777           CMP    #-1,R2       ;CHECK DATA IN R2
986 001734 001406                  BEQ    REG2C       ;RESTORE POINTER
987 001736 012702 000304           MOV    #$TESTN,R2
988 001742 012742 000026           R2ERR: MOV    #26,-(R2)      ;MOVE TO MAILBOX * ***** 26 *****
989 001746 005242                  INC    -(R2)          ;SET MSGTYP TO FATAL ERROR
990 001750 000000                  HALT
991 001752 012702 000304           REG2C: MOV    #$TESTN,R2   ;FAILURE WITH R2
992                                         ;RESTORE POINTER
993                                         ;*****
994                                         ;TEST 23 TEST IF R3 CAN HOLD A ONE IN ALL BITS
995                                         ;*****
996 001756 005212                  TST23: INC    (R2)        ;UPDATE TEST NUMBER
998 001760 022712 000023           CMP    #23,(R2)      ;SEQUENCE ERROR?
999 001764 001012                  BNE    TST24-10    ;BR TO ERROR HALT ON SEQ ERROR
1000 001766 012703 000001          MOV    #1,R3       ;SET BIT 0
1001 001772 012700 177757           MOV    #-21,RO      ;SET BIT COUNTER
1002 001776 000241                  CLC
1003 002000 005200                  REG3:  INC    RO         ;INCREMENT BIT COUNTER
1004 002002 001403                  BEQ    REG3E       ;BR TO ERROR HALT IF BIT IS LOST
1005 002004 006103                  ROL    R3         ;ROTATE 1 POSITION
1006 002006 103374                  BCC    REG3       ;ALL DONE
1007 002010 001404                  BEQ    TST24
1008                                         ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
1009                                         ; CONDITIONAL BRANCH INST. AND <=====
1010                                         ; REPLACE THE MOVE INSTRUCTION <=====
1011                                         ; WHICH FOLLOWS W/ 766 <=====
1012 002012 012742 000027           REG3E: MOV    #27,-(R2)      ;MOVE TO MAILBOX * ***** 27 *****
1013 002012 012742 000027           INC    -(R2)          ;SET MSGTYP TO FATAL ERROR
1014 002016 005242                  HALT
1015 002020 000000                  ;FAILURE WITH R3
1016                                         ; OR SEQUENCE ERROR
1017                                         ;*****
1018                                         ;TEST 24 TEST IF R3 CAN HOLD A ZERO IN ALL BITS
1019                                         ;*****
1020 1021 002022 005212 000024           TST24: INC    (R2)        ;UPDATE TEST NUMBER
1022 002024 022712 000024           CMP    #24,(R2)      ;SEQUENCE ERROR?

```

## K02

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 250  
 DFKAA8.P11 T24 TEST IF R3 CAN HOLD A ZERO IN ALL BITS

```

1023 002030 001014      BNE    TST25-10   ;BR TO ERROR HALT ON SEQ ERROR
1024 002032 012703 177776 MOV    #-2,R3   ;SET ALL ONES IN R3 EXCEPT FOR BIT 0
1025 002036 012700 177757 MOV    #-21,RO  ;SET BIT COUNTER
1026 002042 000261      SEC    C-BIT
1027 002044 005200      REG3A: INC    R0     ;INCREMENT BIT COUNTER
1028 002046 001405      BEQ    R3ERR  ;BR TO ERROR HALT IF COUNTER=0
1029 002050 006103      ROL    R3     ;ROTATE 1 POSITION
1030 002052 103774      BCS    REG3A  ;CONTINUE UNTIL C-BIT IS CLEAR
1031 002054 022703 177777 CMP    #-1,R3  ;CHECK DATA
1032 002060 001404      BEQ    TST25
1033                               ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
1034                               ; CONDITIONAL BRANCH INST. AND <=====
1035                               ; REPLACE THE MOVE INSTRUCTION <=====
1036                               ; WHICH FOLLOWS W/ 764 <=====

1037 002062      R3ERR: MOV    #30,-(R2) ;MOVE TO MAILBOX * ***** 30 *****
1038 002062 012742 000030 INC    -(R2)   ;SET MSGTYP TO FATAL ERROR
1039 002066 005242      HALT
1040 002070 000000
1041
1042
1043 :***** TEST 25 TEST IF R4 CAN HOLD A ONE IN ALL BITS *****
1044
1045 :***** TST25: INC (R2) ;UPDATE TEST NUMBER
1046 002072 005212      CMP    #25,(R2) ;SEQUENCE ERROR?
1047 002074 022712 000025 BNE    TST26-10 ;BR TO ERROR HALT ON SEQ ERROR
1048 002100 001012      MOV    #1,R4   ;SET BIT 0
1049 002102 012704 000001 MOV    #-21,RO ;SET BIT COUNTER
1050 002106 012700 177757 CLC
1051 002112 000241      REG4:  INC    R0     ;CLEAR C-BIT
1052 002114 005200      BEQ    REG4E  ;INCREMENT BIT COUNTER
1053 002116 001403      ROL    R4     ;BR TO ERROR HALT IF BIT IS LOST
1054 002120 006104      BCC    REG4   ;ROTATE 1 POSITION
1055 002122 103374      BEQ    TST26  ;ALL DONE
1056 002124 001404
1057                               ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
1058                               ; CONDITIONAL BRANCH INST. AND <=====
1059                               ; REPLACE THE MOVE INSTRUCTION <=====
1060                               ; WHICH FOLLOWS W/ 766 <=====

1061 002126      REG4E: MOV    #31,-(R2) ;MOVE TO MAILBOX * ***** 31 *****
1062 002126 012742 000031 INC    -(R2)   ;SET MSGTYP TO FATAL ERROR
1063 002132 005242      HALT
1064 002134 000000
1065
1066
1067 :***** TEST 26 TEST IF R4 CAN HOLD A ZERO IN ALL BITS *****
1068
1069 :***** TST26: INC (R2) ;UPDATE TEST NUMBER
1070 002136 005212      CMP    #26,(R2) ;SEQUENCE ERROR?
1071 002140 022712 000026 BNE    TST27-10 ;BR TO ERROR HALT ON SEQ ERROR
1072 002144 001014      MOV    #-2,R4   ;SET ALL ONES IN R4 EXCEPT FOR BIT 0
1073 002146 012704 177776 MOV    #-21,RO ;SET BIT COUNTER
1074 002152 012700 177757 SEC
1075 002156 000261      REG4A: INC    R0     ;INCREMENT BIT COUNTER
1076 002160 005200      BEQ    R4ERR  ;BR TO ERROR HALT IF COUNTER=0
1077 002162 001405      ROL    R4     ;ROTATE 1 POSITION
1078 002164 006104

```

## L02

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 DFKAA8.P11 T26 TEST IF R4 CAN HOLD A ZERO IN ALL BITS

```

1079 002166 103774      BCS   REG4A ;CONTINUE UNTIL C-BIT IS CLEAR
1080 002170 022704 177777    CMP   #-1,R4 ;CHECK DATA
1081 002174 001404      BEQ   TST27
1082
1083
1084
1085
1086 002176      R4ERR:    MOV   #32,-(R2)
1087 002176 012742 000032    INC   -(R2) ;MOVE TO MAILBOX # ***** 32 *****
1088 002202 005242      HALT
1089 002204 000000      ;SET MSGTYP TO FATAL ERROR
1090
1091
1092
1093
1094
1095
1096 002206 005212      TST27:   INC   (R2) ;TEST 27 TEST IF R5 CAN HOLD A ONE IN ALL BITS
1097 002210 022712 000027    CMP   #27,(R2) ;UPDATE TEST NUMBER
1098 002214 001012      BNE   TST30-10 ;SEQUENCE ERROR?
1099 002216 012705 000001    MOV   #1,R5 ;BR TO ERROR HALT ON SEQ ERROR
1100 002222 012700 177757    MOV   #-21,RO ;SET BIT 0
1101 002226 000241      CLC
1102 002230 005200      REG5:    INC   RO ;SET BIT COUNTER
1103 002232 001403      BEQ   REGSE ;INCREMENT BIT COUNTER
1104 002234 006105      ROL   RS ;BR TO ERROR HALT IF BIT IS LOST
1105 002236 103374      BCC   REGS ;ROTATE 1 POSITION
1106 002240 001404      BEQ   TST30 ;ALL DONE
1107
1108
1109
1110
1111 002242      REGSE:    MOV   #33,-(R2) ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
1112 002242 012742 000033    INC   -(R2) ;CONDITIONAL BRANCH INST. AND
1113 002246 005242      HALT
1114 002250 000000      ;REPLACE THE MOVE INSTRUCTION
1115
1116
1117
1118
1119
1120 002252 005212      TST30:   INC   (R2) ;TEST 30 TEST IF R5 CAN HOLD A ZERO IN ALL BITS
1121 002254 022712 000030    CMP   #30,(R2) ;UPDATE TEST NUMBER
1122 002260 001014      BNE   TST31-10 ;SEQUENCE ERROR?
1123 002262 012705 177776    MOV   #-2,R5 ;BR TO ERROR HALT ON SEQ ERROR
1124 002266 012700 177757    MOV   #-21,RO ;SET ALL ONES IN R5 EXCEPT FOR BIT 0
1125 002272 000261      SEC
1126 002274 005200      REG5A:   INC   RO ;SET BIT COUNTER
1127 002276 001405      BEQ   R5ERR ;INCREMENT BIT COUNTER
1128 002300 006105      ROL   RS ;BR TO ERROR HALT IF COUNTER=0
1129 002302 103774      BCS   REG5A ;ROTATE 1 POSITION
1130 002304 022705 177777    CMP   #-1,R5 ;CONTINUE UNTIL C-BIT IS C;EAR
1131 002310 001404      BEQ   TST31 ;CHECK DATA
1132
1133
1134
  ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
  ;CONDITIONAL BRANCH INST. AND
  ;REPLACE THE MOVE INSTRUCTION
  ;*****
```

## M02

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 252  
 DFKAA8.P11 T30 TEST IF R5 CAN HOLD A ZERO IN ALL BITS

1135 ; WHICH FOLLOWS W/ 754 <=====  
 1136 002312 012742 000034 RSERR:  
 1137 002312 005242 000034 MOV #34,-(R2) ; MOVE TO MAILBOX \* \*\*\*\*\* 34 \*\*\*\*\*  
 1138 002316 005242 HALT INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 1139 002220 000000 HALT ; FAILURE WITH R5  
 1140 ; OR SEQUENCE ERROR  
 1141 ;\*\*\*\*\*  
 1142 ;TEST 31 TEST IF R6 CAN HOLD A ONE IN ALL BITS  
 1143 ;\*\*\*\*\*  
 1144 TST31: INC (R2) ; UPDATE TEST NUMBER  
 1145 002322 005212 000031 CMP #31,(R2) ; SEQUENCE ERROR?  
 1146 002324 022712 000031 BNE TST32-10 ; BR TO ERROR HALT ON SEQ ERROR  
 1147 002330 001012 000001 MOV #1,R6  
 1148 002332 012706 000001 MOV #-21,RO ; SET BIT 0  
 1149 002336 012700 177757 CLC ; SET BIT COUNTER  
 1150 002342 000241 REG6: INC RO ; CLEAR C-BIT  
 1151 002344 005200 BEQ REG6E ; INCREMENT BIT COUNTER  
 1152 002346 001403 ROL R6 ; BR TO ERROR HALT IF BIT IS LOST  
 1153 002350 005106 BCC REG6 ; ROTATE 1 POSITION  
 1154 002352 103374 BEQ TST32 ; ALL DONE  
 1155 002354 001404 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 1156 ; CONDITIONAL BRANCH INST. AND <=====  
 1157 ; REPLACE THE MOVE INSTRUCTION <=====  
 1158 ; WHICH FOLLOWS W/ 766 <=====  
 1159 ;  
 1160 002356 012742 000035 REG6E:  
 1161 002356 012742 000035 MOV #35,-(R2) ; MOVE TO MAILBOX \* \*\*\*\*\* 35 \*\*\*\*\*  
 1162 002362 005242 HALT INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 1163 002364 000000 HALT ; FAILURE WITH R6  
 1164 ; OR SEQUENCE ERROR  
 1165 ;\*\*\*\*\*  
 1166 ;TEST 32 TEST IF R6 CAN HOLD A ZERO IN ALL BITS  
 1167 ;\*\*\*\*\*  
 1168 TST32: INC (R2) ; UPDATE TEST NUMBER  
 1169 002366 005212 000032 CMP #32,(R2) ; SEQUENCE ERROR?  
 1170 002370 022712 000032 BNE TST33-10 ; BR TO ERROR HALT ON SEQ ERROR  
 1171 002374 001014 000032 MOV #-2,R6 ; SET ALL ONES IN R6 EXCEPT FOR BIT 0  
 1172 002376 012706 177776 MOV #-21,RO ; SET BIT COUNTER  
 1173 002402 012700 177757 SEC ; SET C-BIT  
 1174 002406 000261 REG6A: INC RO ; INCREMENT BIT COUNT  
 1175 002410 005200 BEQ R6ERR ; BR TO ERROR HALT IF COUNTER=0  
 1176 002412 001405 ROL R6 ; ROTATE 1 POSITION  
 1177 002414 006106 BCS REG6A ; CONTINUE UNTIL C-BIT IS CLEAR  
 1178 002416 103374 BCS REG6A ; CHECK DATA  
 1179 002420 022706 177777 CMP #-1,R6  
 1180 002424 001404 BEQ TST33 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 1181 ; CONDITIONAL BRANCH INST. AND <=====  
 1182 ; REPLACE THE MOVE INSTRUCTION <=====  
 1183 ; WHICH FOLLOWS W/ 764 <=====  
 1184 ;  
 1185 002426 012742 000036 R6ERR:  
 1186 002426 012742 000036 MOV #36,-(R2) ; MOVE TO MAILBOX \* \*\*\*\*\* 36 \*\*\*\*\*  
 1187 002432 005242 HALT INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 1188 002434 000000 HALT ; FAILURE WITH R6  
 1189 ; OR SEQUENCE ERROR

N02

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1209 002436 005212
1210 002440 022712 000033
1211 002444 001010
1212 002446 012706 000500
1213 002452 012737 000000 177775
1214 002460 005737 177776
1215 002464 001404
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1220 002466 012742 000037
1221 002472 005242
1222 002474 000000
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1228 002476 005212
1229 002500 022712 000034
1230 002504 001007
1231 002506 012737 000252 177776
1232 002514 023727 177776 000252
1233 002522 001404
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1238 002524 012742 000040
1239 002530 005242
1240 002532 000000
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;*****SBTTL PSW TESTS*****
; THE PSW TESTS ARE USED TO VERIFY THAT VARIOUS DATA
; PATTERNS CAN BE SUCCESSFULLY HELD IN THE PSW AND THAT THE
; PSW ADDRESSING LOGIC IS FUNCTIONING. MOVE AND COMPARE INSTRUCTIONS
; ARE USED TO TEST THAT THE PSW CAN HOLD VARIOUS DATA PATTERNS.
; EACH DATA PATTERN IS MOVED AND TESTED IN A SMALL LOOP CONVENIENT FOR
; SCOPING.
; THE PSW REGISTER ITSELF IS TESTED AS WELL AS THE ADDRESS
; SELECT CIRCUITRY. THE AMUX INPUTS TO THE PSW MUX ARE TESTED. THE
; CC INPUTS ARE TESTED LATER IN THE MICROCODE TESTS. SETTING OF
; THE T-BIT BY THE TEST PATTERNS IS PURPOSELY AVOIDED; TESTING OF THE
; T-BIT TRAP CIRCUITRY IS LEFT FOR THE TRAP TEST.

;*****TEST 33 TEST IF PSW WILL HOLD ZEROS*****
;TST33: INC (R2) ;UPDATE TEST NUMBER
;       CMP #33, (R2) ;SEQUENCE ERROR?
;       BNE TST34-10 ;BR TO ERROR HALT ON SEQ ERROR
;       MOV #STBOT, R6
;       MOV #0, @PS
;       TST @PS
;       BEQ TST34 ;SET PSW TO ZERO
;                   ;SUCCESSFUL
;                   ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;                   ; CONDITIONAL BRANCH INST. AND
;                   ; REPLACE THE MOVE INSTRUCTION
;                   ; WHICH FOLLOWS W/ 770
;                   ;=====

;MOV      #37 -(R2) ;MOVE TO MAILBOX * ***** 37 *****
;INC      -(R2)    ;SET MSGTYP TO FATAL ERROR
;HALT
;                   ;PSW NOT 0
;                   ;OR SEQUENCE ERROR
;                   ;=====

;*****TEST 34 TEST IF PSW WILL HOLD ONES AND ZEROS*****
;TST34: INC (R2) ;UPDATE TEST NUMBER
;       CMP #34, (R2) ;SEQUENCE ERROR?
;       BNE TST35-10 ;BR TO ERROR HALT ON SEQ ERROR
;       MOV #252, @PS
;       CMP @PS, #252 ;MOVE ALT. ONES AND ZEROS TO PSW
;       BEQ TST35 ;SUCCESSFUL?
;                   ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;                   ; CONDITIONAL BRANCH INST. AND
;                   ; REPLACE THE MOVE INSTRUCTION
;                   ; WHICH FOLLOWS W/ 771
;                   ;=====

;MOV      #40 -(R2) ;MOVE TO MAILBOX * ***** 40 *****
;INC      -(R2)    ;SET MSGTYP TO FATAL ERROR
;HALT
;                   ;PSW NOT 252
;                   ;OR SEQUENCE ERROR
;                   ;=====

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DFKAA8.P11 T34 TEST IF PSW WILL HOLD ONES AND ZEROES

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1244 :***** TEST 35 TEST IF PSW (EXCEPT T-BIT) WILL HOLD ZEROES AND ONES *****
1245 :***** TEST IF PSW (EXCEPT T-BIT) WILL HOLD ZEROES AND ONES *****
1246 002534 005212      :TST35: INC   (R2)          :UPDATE TEST NUMBER
1247 002536 022712 000035    CMP   #35,(R2)        :SEQUENCE ERROR?
1248 002542 001007          SNE   TST36-10       :BR TO ERROR HALT ON SEQ ERROR
1249 002544 012737 000105 177776    MOV   #105,&PS      :MOVE ALT. ONES AND ZEROES TO PSW
1250 002552 023727 177776 000105    CMP   #PS,&105     :SUCCESSFUL?
1251 002560 001404          BEQ   TST36

1252 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
1253 : CONDITIONAL BRANCH INST. AND <=====
1254 : REPLACE THE MOVE INSTRUCTION <=====
1255 : WHICH FOLLOWS W/ 771 <=====

1256 002562 012742 000041      MOV   #41,-(R2)    :MOVE TO MAILBOX # ***** 41 *****
1257 002566 005242          INC   -(R2)         :SET MSGTYP TO FATAL ERROR
1258 002570 000000          HALT           :PSW NOT 105
1259 : OR SEQUENCE ERROR

1260
1261 :***** TEST 36 TEST IF PSW (EXCEPT T-BIT) WILL HOLD ALL ONES *****
1262 :***** TEST IF PSW (EXCEPT T-BIT) WILL HOLD ALL ONES *****
1263 :***** TEST IF PSW (EXCEPT T-BIT) WILL HOLD ALL ONES *****
1264 002572 005212      :TST36: INC   (R2)          :UPDATE TEST NUMBER
1265 002574 022712 000036    CMP   #36,(R2)        :SEQUENCE ERROR?
1266 002600 001007          BNE   TST37-10       :BR TO ERROR HALT ON SEQ ERROR
1267 002602 012737 000357 177776    MOV   #357,&PS      :MOVE ONES TO PSW
1268 002610 023727 177776 000357    CMP   #PS,&357     :SUCCESSFUL?
1269 002616 001404          BEQ   TST37

1270 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
1271 : CONDITIONAL BRANCH INST. AND <=====
1272 : REPLACE THE MOVE INSTRUCTION <=====
1273 : WHICH FOLLOWS W/ 771 <=====

1274 002620 012742 000042      MOV   #42,-(R2)    :MOVE TO MAILBOX # ***** 42 *****
1275 002624 005242          INC   -(R2)         :SET MSGTYP TO FATAL ERROR
1276 002626 000000          HALT           :PSW NOT 357
1277 : OR SEQUENCE ERROR

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MAINDEC-II-DFKAA-B 11 34 CPU TEST  
DFKAA8.P11 CONDITION CODE TEST

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1282 : THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE Z-BIT.  
1283 : THE Z-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS  
1284 : BEQ AND BNE ARE TESTED FOR PROPER EXECUTION. THEN THE Z-BIT IS  
1285 : SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED  
1286 : AGAIN FOR PROPER OPERATION.  
1287 : THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION  
1288 : CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL  
1289 : BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR  
1290 : LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY  
1291 : USED IN THE TEST ARE VERIFIED HERE.  
1292  
1293 : TEST 37 TEST BRANCHES AROUND Z-BIT  
1294 :  
1295 : TST37: INC (R2) ; UPDATE TEST NUMBER  
1296 002630 005212 000037 CMP #37,(R2) ; SEQUENCE ERROR?  
1297 002632 022712 BNE TST40-10 ; BR TO ERROR HALT ON SEQ ERROR  
1298 002636 001014  
1299  
1300 002640 000257  
1301 002642 0002E4  
1302 002644 001001  
1303 002646 001404  
1304  
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1307 : FIRST WITH Z-BIT ON  
1308 002650 012742 000043  
1309 002650 012742 000043  
1310 002654 005242  
1311 002656 000000  
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1313 002660 000277  
1314 002662 000244  
1315 002664 001401  
1316 002666 001004  
1317  
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1320 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
1321 002670 012742 000044  
1322 002670 012742 000044  
1323 002674 005242  
1324 002676 000000  
1325 : CONDITIONAL BRANCH INST. AND  
1326 : REPLACE THE MOVE INSTRUCTION  
1327 : WHICH FOLLOWS W/ 774  
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 1329 THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE N-BIT.  
 1330 :THE N-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS  
 1331 :BMI AND BPL ARE TESTED FOR PROPER EXECUTION. THEN THE N-BIT IS  
 1332 :SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED  
 1333 :AGAIN FOR PROPER OPERATION.  
 1334 THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION  
 1335 :CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL  
 1336 :BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR  
 1337 :LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY  
 1338 :USED IN THE TEST ARE VERIFIED HERE.  
 1339  
 1340 :\*\*\*\*\*  
 1341 :TEST 40 TEST BRANCHES AROUND N-BIT  
 1342 :\*\*\*\*\*  
 1343 002700 005212 000040  
 1344 002702 022712 000040  
 1345 002706 001014 000040  
 1346 TST40: INC (R2) ;UPDATE TEST NUMBER  
 1347 002710 000257  
 1348 002712 000270  
 1349 002714 100001  
 1350 002716 100404  
 1351 :CMP \$40,(R2) ;SEQUENCE ERROR  
 1352 :BNE TST41-10 ;BR TO ERROR HALT ON SEQ ERROR  
 1353 :FIRST WITH N-BIT ON  
 1354 :CCC ;CC=1000: JUST N-BIT  
 1355 :SEN ;CHECK OPPOSITE CONDITION  
 1356 :BPL BRN1 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 1357 :BPL BRN2 ;CONDITIONAL BRANCH INST. AND   
 1358 :BPL BRN3 ;REPLACE THE MOVE INSTRUCTION   
 1359 :HALT ;WHICH FOLLOWS W/ 774   
 1360 :\*\*\*\*\*  
 1361 :\*\*\*\*\*  
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 1363 :\*\*\*\*\*  
 1364 :\*\*\*\*\*  
 1365 :\*\*\*\*\*  
 1366 :\*\*\*\*\*  
 1367 :\*\*\*\*\*  
 1368 002720 012742 000045  
 1369 002724 005242 000045  
 1370 002726 000000 000045  
 1371 TST41: MOV \$45,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 45 \*\*\*\*\*  
 1372 :INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 1373 :HALT ;IMPROPER BR W/ N=1  
 1374 :CHECK WITH N-BIT OFF  
 1375 :SCC ;CC=0111  
 1376 :CLN ;CHECK OPPOSITE CONDITION  
 1377 :BPL BRN2 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 1378 :BPL BRN3 ;CONDITIONAL BRANCH INST. AND   
 1379 :BPL BRN1 ;REPLACE THE MOVE INSTRUCTION   
 1380 :BPL BRN4 ;WHICH FOLLOWS W/ 764   
 1381 :HALT ;\*\*\*\*\*  
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THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE V-BIT.  
 THE V-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS  
 BVS AND BVC ARE TESTED FOR PROPER EXECUTION. THEN THE V-BIT IS  
 SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED  
 AGAIN FOR PROPER OPERATION.

THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION  
 CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL  
 BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR  
 LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY  
 USED IN THE TEST ARE VERIFIED HERE.

TEST 41 TEST BRANCHES AROUND V-BIT

002750	005212		TST41:	INC (R2)	; UPDATE TEST NUMBER
002752	022712	000041		CMP #41, (R2)	; SEQUENCE ERROR?
002756	001014			BNE TST42-10	; BR TO ERROR HALT ON SEQ ERROR
002760	000257			CCC	; CC=0010: JUST V-BIT
002762	00C262			SEV	
002764	102001			BVC BRV1	; CHECK OPPOSITE CONDITION
002766	102404			BVS BRV2	
002770					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 774
002770	012742	000047	BRV1:	MOV #47, -(R2)	; MOVE TO MAILBOX # ***** 47 *****
002774	005242			INC -(R2)	; SET MSGTYP TO FATAL ERROR
002776	000000			HALT	; IMPROPER BR W/ V=1
003000	000277				
003002	000242		BRV2:	SCC	; CC=1101: ALL BVT V-BIT
003004	102401			CLV	
003006	102004			BVS BRV3	; CHECK OPPOSITE CONDITION
003010				BVC TST42	
003010	012742	000050	BRV3:	MOV #50, -(R2)	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 764
003014	005242			INC -(R2)	
003016	000000			HALT	
003018					
003019					

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1437 003020 005212
1438 003022 022712 000042
1439 003026 001014
1440 003030 000257
1441 003032 000261
1442 003034 103001
1443 003C36 103404
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1449 003040
1450 003040 012742 000051
1451 003044 005242
1452 003046 000000
1453
1454 003050 000277
1455 003052 000241
1456 003054 103401
1457 003056 100404
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1462 003060
1463 003060 012742 000052
1464 003064 005242
1465 003066 000000
1466

;***** THIS TEST CHECKS THE CONDITIONAL BRANCHES INVOLVING THE C-BIT.
;THE C-BIT IS SET WITH ALL OTHER CC BITS ZERO AND BOTH CONDITIONS
;BCS AND BCC ARE TESTED FOR PROPER EXECUTION. THEN THE C-BIT IS
;SET WITH ALL OTHER CC BITS CLEAR AND BOTH CONDITIONS ARE TESTED
;AGAIN FOR PROPER OPERATION.

;THIS TEST CHECKS THE OPERATION OF THE SET AND CLEAR CONDITION
;CODE INSTRUCTIONS AND CHECKS THE CIRCUITRY EXTERNAL TO THE CONDITIONAL
;BRANCH ROM. THE BRANCH MICROCODE FOR ALTERING THE PC AND FOR
;LEAVING THE PC UNALTERED IS TESTED. ONLY THOSE ROM ADDRESSES SPECIFICALLY
;USED IN THE TEST ARE VERIFIED HERE.

;***** TEST 42 TEST BRANCHES AROUND C-BIT *****
;***** TST42: INC (R2) :UPDATE TEST NUMBER
;           CMP #42,(R2) :SEQUENCE ERROR?
;           BNE TST43-10 :BR TO ERROR HALT ON SEQ ERROR
;           ;FIRST WITH C-BIT ON
;           CCC
;           SEC
;           BCC BRC1      ;CHECK OPPOSITE CONDITION
;           BCS BRC2
;           ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
;           ;CONDITIONAL BRANCH INST. AND <=====
;           ;REPLACE THE MOVE INSTRUCTION <=====
;           ;WHICH FOLLOWS W/ 774 <=====

;           BRC1:    MOV #51,-(R2) ;MOVE TO MAILBOX # ***** 51 *****
;           INC -(R2)   ;SET MSGTYP TO FATAL ERROR
;           HALT     ;IMPROPER BR W/ C=1
;           ;CHECK WITH C-BIT OFF
;           BRC2:    SCC
;           CLC
;           BCS BRC3      ;CHECK OPPOSITE CONDITION
;           BMI TST43
;           ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
;           ;CONDITIONAL BRANCH INST. AND <=====
;           ;REPLACE THE MOVE INSTRUCTION <=====
;           ;WHICH FOLLOWS W/ 764 <=====

;           BRC3:    MOV #52,-(R2) ;MOVE TO MAILBOX # ***** 52 *****
;           INC -(R2)   ;SET MSGTYP TO FATAL ERROR
;           HALT     ;IMPROPER BR W/ C=0
;           ;OR SEQUENCE ERROR

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1467  
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 1469 ;\*\*\*\*\*  
 1470 ;SBTTL MICROCODE TESTS  
 1471 ;  
 1472 ; THE MICROCODE TESTS ARE USED TO VERIFY THE MICROPROGRAMM  
 1473 ; FLOW. THE GOAL OF THESE TESTS IS TO EXERCISE EVERY POSSIBLE  
 1474 ; BRANCH IN THE MICROPROGRAM FLOW.  
 1475 ;  
 1476 ; THE TEST EXERCISES EVERY BRANCH IN THE MICROCODE BY  
 1477 ; TESTING AT LEAST ONE INSTRUCTION FROM EVERY CLASS OF INSTRUCTION IN  
 1478 ; ALL POSSIBLE MODES. FOR EXAMPLE, TO TEST THE SINGLE OPERAND INSTRUCTIONS,  
 1479 ; AT LEAST ONE SINGLE OPERAND INSTRUCTION IS VERIFIED IN ALL UNIQUE  
 1480 ; ADDRESSING MODES. BYTE MODES ARE ALSO TESTED. AS EACH NEW  
 1481 ; MODE IS INTRODUCED THE SAME INSTRUCTION IS TRIED AND TESTED IN  
 1482 ; A SMALL LOOP CONVENIENT FOR SCOPING. THE TEST IS SET UP USING  
 1483 ; ONLY INSTRUCTIONS AND ADDRESSING MODES WHICH HAVE BEEN PREVIOUSLY  
 1484 ; VERIFIED.  
 1485 ; IF THESE TESTS FAIL, CHECK THE RESULTS FOR A CLUE TO THE  
 1486 ; FAULT.  
 1487 ;\*\*\*\*\*  
 1488  
 1489  
 1490 ;\*\*\*\*\*  
 1491 ;  
 1492 ; THE CLR INSTRUCTION IS USED TO INTRODUCE EACH ADDRESSING  
 1493 ; MODE WITH THE SINGLE OPERAND INSTRUCTION. FOLLOWING THE SEQUENCE CHECK,  
 1494 ; THE CLR INSTRUCTION IS EXECUTED AND A BRANCH TEST IS EXECUTED WHICH  
 1495 ; CHECKS THAT THE Z-BIT WAS PROPERLY SET. THIS SMALL TEST IS SELF-SUFFICIENT  
 1496 ; AND CAN BE SCOPED TO TROUBLE SHOOT ALL OF THE IR DECODE LOGIC AND  
 1497 ; MICROCODE FOR SOP INSTRUCTIONS WITH MODE 0. FOLLOWING THIS TEST  
 1498 ; SEVERAL OTHER SOP INSTRUCTIONS ARE INTRODUCED WITH MODE 0. THESE  
 1499 ; INSTRUCTIONS MANIPULATE DATA AND SERVE TO CHECK THE DATA RESULTS  
 1500 ; OF THE SOP INSTRUCTIONS IN THIS TEST. THE DATA IN THIS TEST IS  
 1501 ; OPERATED ON BY EACH INSTRUCTION WITHOUT REINITIALIZING.  
 1502  
 1503 ;\*\*\*\*\*  
 1504 ; TEST 43 TEST MODE 0 USING SOP INST.  
 1505 ;\*\*\*\*\*  
 1506 003070 005212 000043  
 1507 003072 022712 TST43:  
 1508 003076 001020 INC (R2) ;UPDATE TEST NUMBER  
 1509 003100 005000 CMP #43, (R2) ;SEQUENCE ERROR?  
 1510 003102 001404 BNE TST44-10 ;BR TO ERROR HALT ON SEQ ERROR  
 1511 ; TRY THE CLEAR INST.  
 1512 ;  
 1513 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 1514 ; CONDITIONAL BRANCH INST. AND <=====  
 1515 003104 012742 000053 ; REPLACE THE MOVE INSTRUCTION <=====  
 1516 003110 005242 MOV #53,-(R2) ; WHICH FOLLOWS W/ 776 <=====  
 1517 003112 000000 INC -(R2)  
 1518 003114 005200 HALT  
 1519 003116 005100 INC RO  
 1520 003120 005200 COM RO  
 1521 003122 100404 INC RO  
 1522 ; TRY THE INCREMENT INST.  
 1523 ; TRY COMPLEMENT  
 1524 ;  
 1525 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 1526

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 1525  
 1526 003124 012742 000054 : MOV #54,-(R2) ; CONDITIONAL BRANCH INST. AND  
 1527 003130 005242 : INC -(R2) ; REPLACE THE MOVE INSTRUCTION  
 1528 003132 000000 : HALT ; WHICH FOLLOWS W/ 766  
 1529 003134 005100 : COM R0 ; MOVE TO MAILBOX # \*\*\*\*\* 54 \*\*\*\*\*  
 1530 003136 001404 : BEQ TST44 ; SET MSGTYP TO FATAL ERROR  
 1531 : SOPOB: ; NEGATE DID NOT SET N-BIT  
 1532 : TRY COMPLEMENT INST.  
 1533 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 1534 : CONDITIONAL BRANCH INST. AND  
 1535 003140 012742 000055 : INC #55,-(R2) ; REPLACE THE MOVE INSTRUCTION  
 1536 003144 005242 : HALT ; WHICH FOLLOWS W/ 760  
 1537 003145 000000 : ; SET MSGTYP TO FATAL ERROR  
 1538 : CUMMULATIVE RESULT OF CLR, INC, NEG AND COM INSTS. FAILED  
 1539 : OR SEQUENCE ERROR  
 1540  
 1541  
 1542  
 1543 :\*\*\*\*\* THIS TEST INTRODUCES THE REMAINING SOP INSTRUCTIONS AND TESTS  
 1544 : THEM IN MODE 0. THE PURPOSE IS TO PROVIDE A BASELINE OF  
 1545 : INSTRUCTIONS FOR USE IN THE SUBSEQUENT TESTS. SINCE THE MICROCODE FOR  
 1546 : THESE INSTRUCTIONS IS IDENTICAL TO THAT ALREADY TESTED, ANY TROUBLE  
 1547 : SHOOTING EFFORTS SHOULD BE AIMED AT THE ACTUAL IR DECODE AND ALU  
 1548 : FUNCTIONING.  
 1549  
 1550 :\*\*\*\*\* TEST 44 TEST REMAINDER OF SOP INSTS IN MODE 0\*\*\*\*\*  
 1551 :\*\*\*\*\*  
 1552 1553 003150 005212 : TST44: INC (R2) ; UPDATE TEST NUMBER  
 1554 003152 022712 000044 : CMP #44,(R2) ; SEQUENCE ERROR?  
 1555 003156 001021 : BNE TST45-10 ; BR TO ERROR HALT ON SEQ ERROR  
 1556 003160 005000 : CLR R0 ; INITIALIZE  
 1557 003162 005300 : DEC R0 ; TRY DECREMENT INST.  
 1558 003164 100404 : BMI SOPOC ;  
 1559 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 1560 : CONDITIONAL BRANCH INST. AND  
 1561 : REPLACE THE MOVE INSTRUCTION  
 1562 : WHICH FOLLOWS W/ 775  
 1563 003166 012742 000056 : MOV #56,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 56 \*\*\*\*\*  
 1564 003172 005242 : INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 1565 003174 000000 : HALT ; N-BIT NOT SET ON DEC  
 1566 003176 000261 : SEC ; INITIALIZE CARRY  
 1567 003200 005500 : ADC R0 ; TRY ADD CARRY INST  
 1568 003202 001007 : BNE SOPOD ;  
 1569 003204 000261 : SEC ; INITIALIZE CARRY  
 1570 003206 005600 : SBC R0 ; TRY SUBTRACT-CARRY INST  
 1571 003210 100004 : BPL SOPOD ;  
 1572 003212 005100 : COM R0 ;  
 1573 003214 005200 : INC R0 ;  
 1574 003216 005300 : DEC R0 ;  
 1575 003220 001404 : BEQ TST45 ;  
 1576 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 1577 : CONDITIONAL BRANCH INST. AND  
 1578 : REPLACE THE MOVE INSTRUCTION

MAINDEC-11-DFKAA-8 11 34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 261  
DFKAAB.P11 T44 TEST REMAINDER OF SOP INSTS IN MODE 0

1579  
1580 003222  
1581 003222 012742 000057  
1582 003226 005242  
1583 003230 000000  
1584

SCPOD:

MOV #57 -(R2)  
INC -(R2)  
HALT

; WHICH FOLLOWS W/ 757

&lt;=====

; MOVE TO MAILBOX # \*\*\*\*\* 57 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; CUMMULATIVE RESULT OF ADC,SBC,COM,INC AND DEC INSTS. F  
; OR SEQUENCE ERROR

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1585
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1595 003232 005212
1596 003234 022712 000045
1597 003240 001012
1598 003242 105000
1599 003244 001404

1600
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1602
1603
1604 003246 012742 000060
1605 003252 005242
1606 003254 000000
1607 003256 105100
1608 003260 100002
1609 003262 105200
1610 003264 001404

1611
1612
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1614
1615 003266 012742 000051
1616 003266 005242
1617 003272 000000
1618 003274 000000
1619

;***** THIS TEST INTRODUCES THE BYTE CONTROL LOGIC OF THE PROCESSOR.
;THE MODE 0 BYTE MICROCODE IS TESTED. THE METHOD AND SEQUENCE
;OF TESTING IS THE SAME AS THAT USED IN THE SOP MODE 0 TESTS.

;TEST 45 TEST MODE 0 EVEN BYTE USING SOP INST
;***** TST45: INC (R2) ;UPDATE TEST NUMBER
;           CMP #45, (R2) ;SEQUENCE ERROR?
;           BNE TST46-10 ;BR TO ERROR HALT ON SEG ERROR
;           CLR8 R0 ;TRY CLEARING EVEN BYTE OF REGISTER
;           BEQ SOPBOA
;           : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====)
;           : CONDITIONAL BRANCH INST. AND (====)
;           : REPLACE THE MOVE INSTRUCTION (====)
;           : WHICH FOLLOWS W/ 776 (====)
;           MOV #60,-(R2) ;MOVE TO MAILBOX # ***** 60 *****
;           INC -(R2) ;SET MSGTYP TO FATAL ERROR
;           HALT ;CLRB DID NOT SET Z-BIT
;           SOPBOA: COMB R0 ;TRY SETTING EVEN BYTE OF REGISTER
;           BPL SOPBOB
;           INCB R0 ;TRY INCREMENTING EVEN BYTE OF REGISTER>>
;           BEQ TST46
;           : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (====)
;           : CONDITIONAL BRANCH INST. AND (====)
;           : REPLACE THE MOVE INSTRUCTION (====)
;           : WHICH FOLLOWS W/ 766 (====)
;           SOPBOB: MOV #61,-(R2) ;MOVE TO MAILBOX # ***** 61 *****
;           INC -(R2) ;SET MSGTYP TO FATAL ERROR
;           HALT ;TEST CUMMULATIVE RESULT OF ABOVE BYTE INST.
;           ; OR SEQUENCE ERROR

```

## K03

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 263  
DFKAAB.P11 T45 TEST MODE 0 EVEN BYTE USING SOP INST

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1630
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1632 003276 C05212
1633 003300 022712 000046
1634 003304 001014
1635 003306 005000
1636 003310 005010
1637 003312 001404
1638
1639
1640
1641
1642 003314 012742 000062
1643 003320 005242
1644 003322 000000
1645 003324 005310
1646 003326 100003
1647 003330 000261
1648 003332 005510
1649 003334 001404
1650
1651
1652
1653
1654 003336 012742 000063
1655 003336 005242
1656 003342 000000
1657 003344 000000
1658

;***** THIS TEST USES THE CLR INSTRUCTION TO INTRODUCE AND TEST
;SINGLE OPERAND MODE 1 INSTRUCTIONS. AGAIN, THE CLR INSTRUCTION
;IS USED TO INTRODUCE THE MICROCODE AND TO TEST THAT THE PROPER
;CONDITION CODES ARE SET. OTHER SOP INSTRUCTIONS ARE USED TO MANIPULATE
;COMMON DATA TO VERIFY THAT THE CORRECT DATA IS PRODUCED.

;***** TEST 46 TEST MODE 1 USING SOP INST.

;***** TST46: INC (R2) ;UPDATE TEST NUMBER
;             CMP #46, (R2) ;SEQUENCE ERROR?
;             BNE TST47-10 ;BR TO ERROR HALT ON SEQ ERROR
;             CLR R0 ;INITIALIZE R0
;             CLR (R0) ;TRY CLEAR INST W/MODE 1
;             BEQ SOP1A ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;                           CONDITIONAL BRANCH INST. AND
;                           REPLACE THE MOVE INSTRUCTION
;                           WHICH FOLLOWS W/ 775 <=====
;             MOV #62, -(R2) ;MOVE TO MAILBOX # ***** 62 *****
;             INC -(R2) ;SET MSGTYP TO FATAL ERROR
;             HALT ;CLR DID NOT SET Z-BIT
;             DEC (R0) ;TRY DECREMENT INST W/MODE 1
;             BPL SOP1B ;INITIALIZE CARRY
;             SEC ;TRY ADD-CARRY W/MODE 1
;             ADC (R0) ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;                           CONDITIONAL BRANCH INST. AND
;                           REPLACE THE MOVE INSTRUCTION
;                           WHICH FOLLOWS W/ 764 <=====
;             BEQ TST47 ;MOVE TO MAILBOX # ***** 63 *****
;             MOV #63, -(R2) ;SET MSGTYP TO FATAL ERROR
;             INC -(R2) ;TEST CUMMULATIVE RESULT OF ABOVE INST
;             HALT ;OR SEQUENCE ERROR
;
```

1659  
 1660 \*\*\*\*\*  
 1661  
 1662 THIS TEST VERIFIES THE BYTE INSTRUCTION MICROCODE FOR MODE 1  
 1663 SINGLE OPERAND INSTRUCTIONS.  
 1664 THIS IS THE FIRST PLACE THE SIGN EXTEND LOGIC IS EXERCISED  
 1665 AND VERIFIED.  
 1666 \*\*\*\*\*  
 1667 TEST 47 TEST MODE 1 EVEN BYTE USING SOP INST  
 1668 \*\*\*\*\*  
 1669  
 1670 003346 005212 000047  
 1671 003350 022712 000047  
 1672 003354 001020  
 1673 003356 005000  
 1674 003360 005010  
 1675 003362 005110  
 1676 003364 105010  
 1677 003366 001404  
 1678  
 1679  
 1680  
 1681  
 1682 003370 012742 000064  
 1683 003374 005242  
 1684 003376 000000  
 1685 003400 005210  
 1686 003402 100005  
 1687 003404 105110  
 1688 003406 105210  
 1689 003410 100002  
 1690 003412 105210  
 1691 003414 001404  
 1692  
 1693  
 1694  
 1695  
 1696 003416 012742 000065  
 1697 003416 005242  
 1698 003422 000000  
 1699 003424 000000  
 1700  
 1701

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;*****  

;THIS TEST VERIFIES THE BYTE INSTRUCTION MICROCODE FOR MODE 1  

;SINGLE OPERAND INSTRUCTIONS.  

;THIS IS THE FIRST PLACE THE SIGN EXTEND LOGIC IS EXERCISED  

;AND VERIFIED.  

;*****  

;TEST 47 TEST MODE 1 EVEN BYTE USING SOP INST  

;*****  

;TST47: INC (R2) ;UPDATE TEST NUMBER  

;       CMP #47,(R2) ;SEQUENCE ERROR?  

;       BNE TST$0-10 ;BR TO ERROR HALT ON SEQ ERROR  

;       CLR R0 ;INITIALIZE R0  

;       CLR (R0) ;INITIALIZE LOC. 0  

;       COM (R0)  

;       CLRB (R0) ;TRY TO CLEAR BYTE 0  

;       BEQ SOPB1A ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  

;                      CONDITIONAL BRANCH INST. AND   

;                      REPLACE THE MOVE INSTRUCTION   

;                      WHICH FOLLOWS W/ 773 <=====  

;  

;MOV #64,-(R2) ;MOVE TO MAILBOX * ***** 64 *****  

;INC -(R2) ;SET MSGTYP TO FATAL ERROR  

;HALT ;CLRB DID NOT SET Z-BIT  

;SOPB1A: INC (R0) ;INCREMENT TO TEST WORD  

;        BPL SOPB1B ;COMPLEMENT: ODD BYTE = 376  

;        COMB (R0) ;INC: ODD BYTE = 377  

;        INCB (R0) ;INCREMENT ODD BYTE=0  

;        BPL SOPB1B ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  

;                      CONDITIONAL BRANCH INST. AND   

;                      REPLACE THE MOVE INSTRUCTION   

;                      WHICH FOLLOWS W/ 760 <=====  

;        INCB (R0)  

;        BEQ TST50  

;        TST50 ;MOVE TO MAILBOX * ***** 65 *****  

;        INC -(R2) ;SET MSGTYP TO FATAL ERROR  

;        HALT ;CHECK CUMMULATIVE RESULT OF ABOVE INST  

;              ; OR SEQUENCE ERROR
  
```

1702  
 1703 ;\*\*\*\*\*  
 1704 ;  
 1705 ; THIS TEST VERIFIES THAT SINGLE OPERAND BYTE INSTRUCTIONS WILL  
 1706 ; FUNCTION CORRECTLY FOR ODD BYTES.  
 1707 ; THIS IS THE FIRST TIME THAT ADDRESS LINE 0 HAS BEEN  
 1708 ; EXERCISED. CHECKS ARE MADE THAT THE PROPER BYTE IS MODIFIED AND  
 1709 ; THE CONDITION CODES ARE CHECKED. IT IS ALSO VERIFIED THAT THE UNADDRESSED  
 1710 ; BYTE IS NOT ALTERED BY THE INSTRUCTION.  
 1711  
 1712 ;\*\*\*\*\*  
 1713 ; TEST 50 TEST MODE 1 ODD BYTE USING SOP INST  
 1714 ;\*\*\*\*\*  
 1715 003426 005212 000050  
 1716 003430 022712  
 1717 003434 001022  
 1718 003436 005000  
 1719 003440 005010  
 1720 003442 005110  
 1721 003444 005200  
 1722 003446 105010  
 1723 003450 001404  
 1724  
 1725  
 1726  
 1727  
 1728 003452 012742 000066  
 1729 003456 005242  
 1730 003460 000000  
 1731 003462 005300  
 1732 003464 005210  
 1733 003466 005200  
 1734 003470 105110  
 1735 003472 105210  
 1736 003474 100002  
 1737 003476 105210  
 1738 003500 001404  
 1739  
 1740  
 1741  
 1742  
 1743 003502  
 1744 003502 012742 000067  
 1745 003506 005242  
 1746 003510 000000  
 1747

```

TST50: INC (R2) ;UPDATE TEST NUMBER
       CMP #50, (R2) ;SEQUENCE ERROR?
       BNE TST51-10 ;BR TO ERROR HALT ON SEQ ERROR
       CLR R0 ;INITIALIZE R0
       CLR (R0) ;INITIALIZE LOC. 0
       COM (R0)
       INC R0 ;R0=ODD BYTE
       CLRB (R0) ;TRY TO CLEAR BYTE 1
       BEQ SOPB1C ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====  

                   ; CONDITIONAL BRANCH INST. AND (=====  

                   ; REPLACE THE MOVE INSTRUCTION (=====  

                   ; WHICH FOLLOWS W/ 772 (=====  

MOV #66,-(R2) ;MOVE TO MAILBOX # ***** 66 *****  

INC -(R2) ;SET MSGTYP TO FATAL ERROR
HALT ;CLRB DID NOT SET Z-BIT
SOPB1C: DEC R0 ;R0=WORD ADDR.
         INC (R0) ;INCREMENT TO TEST WORD
         INC R0 ;R0=ODD BYTE
         COMB (R0) ;TRY TO COMPLEMENT BYTE 1
         INCB (R0)
         BPL SOPB1D ;TRY TO INCREMENT BYTE 1
         INCB (R0)
         BEQ TST51 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====  

                   ; CONDITIONAL BRANCH INST. AND (=====  

                   ; REPLACE THE MOVE INSTRUCTION (=====  

                   ; WHICH FOLLOWS W/ 756 (=====  

SOPB1D: MOV #67,-(R2) ;MOVE TO MAILBOX # ***** 67 *****  

       INC -(R2) ;SET MSGTYP TO FATAL ERROR
       HALT ;TEST CUMMULATIVE RESULT OF ABOVE INST.  

                   ; OR SEQUENCE ERROR
  
```

MAINDEC-11-DFKAA-5 11 34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 266  
DFKAA8.P11 750 TEST MODE 1 ODD BYTE USING SOP INST

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1748
1749
1750
1751      THIS TEST VERIFIES MODE 2 SINGLE-OPERAND INSTRUCTIONS. PREVIOUSLY
1752      TESTED INSTRUCTIONS ARE USED TO SET A POINTER IN R0 TO LOC. 400.
1753      LOC. 400 IS INITIALIZED TO -1 BEFORE A CLR MODE 2 IS EXECUTED.
1754      THEN R0 IS DECREMENTED BY TWO TO AGAIN POINT TO 400 BEFORE EACH
1755      OF SEVERAL MODE 2 INSTRUCTIONS ARE USED TO VERIFY THE DATA RESULTS OF
1756      THE TEST. THIS PROCEDURE ALSO VERIFIES THE PROPER INCREMENTING OF THE
1757      REGISTER.
1758
1759      ****
1760      TEST 51      TEST MODE 2 USING SOP INST.
1761      ****
1762 003512 005212      C0005:
1763 003514 022712      TST51: INC   (R2)      ;UPDATE TEST NUMBER
1764 003520 001023      CMP   #51,(R2)    ;SEQUENCE ERROR?
1765 003522 005000      BNE   TST52-10   ;BR TO ERROR HALT ON SEQ ERROR
1766 003524 10E100      CLR   R0        ;SET R0=400
1767 003526 00..00       COMB  R0
1768 003530 005010      INC   R0
1769 003532 005110      CLR   (R0)      ;CLEAR 400
1770 003534 005020      COM   (R0)      ;INITIALIZE: 400=-1
1771 003536 001404      CLR   (R0)+     ;TRY CLEARING WITH MODE 2
1772
1773
1774
1775      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
1776 003540 012742 000070      MOV   #70,-(R2)    ;CONDITIONAL BRANCH INST. AND      <=====
1777 003544 005242      INC   -(R2)      ;REPLACE THE MOVE INSTRUCTION      <=====
1778 003546 000000      HALT
1779 003550 0C5300      SOPZA: DEC   R0        ;WHICH FOLLOWS W/ 771      <=====
1780 003552 005300      DEC   R0
1781 003554 005120      COM   (R0)+     ;MOVE TO MAILBOX # ***** 70 *****
1782 003556 100004      BPL   SOP26      ;SET MSGTYP TO FATAL ERROR
1783 003560 005300      DEC   R0        ;CLR INST DID NOT SET Z-BIT
1784 003562 005300      DEC   R0        ;RESET R0
1785 003564 005220      INC   (R0)+     ;TRY COMPLEMENTING WITH MODE 2
1786 003566 001404      BEQ   TST52      ;TRY INCREMENTING WITH MODE 2
1787
1788
1789
1790      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
1791 003570 012742 000071      SOP2B: MOV   #71,-(R2)    ;CONDITIONAL BRANCH INST. AND      <=====
1792 003570 005242      INC   -(R2)      ;REPLACE THE MOVE INSTRUCTION      <=====
1793 003574 000000      HALT      ;WHICH FOLLOWS W/ 755      <=====
1794
1795      ;MOVE TO MAILBOX # ***** 71 *****
1796      ;SET MSGTYP TO FATAL ERROR
1797      ;CHECK CUMMULATIVE RESULT OF ABOVE INST
1798      ; OR SEQUENCE ERROR

```

MAINDEC-11-DFKAR-9 11 34 CPU TEST MACY!1 27(732) 01-OCT-76 15:03 PAGE 267  
DFKAR8.P11 T51 TEST MODE 2 USING SOP INST.

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1796
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1799      THIS TEST VERIFIES MODE 2 SINGLE OPERAND INSTRUCTIONS WHICH
1800      ADDRESS EVEN BYTES. R0 IS SET TO 400 AND USED TO INITIALIZE LOCATION
1801      400 TO -1. CLR8 INSTRUCTION IS THEN EXECUTED ON BYTE 400 WITH
1802      MODE 2.
1803      R0 IS THEN DECREMENTED BEFORE EACH OF SEVERAL MODE 2 INSTRUCTIONS
1804      WHICH ARE USED TO VERIFY THE DATA RESULTS OF THE TEST. THIS PROCEDURE ALSO
1805      VERIFIES THE PROPER INCREMENTING OF THE REGISTER.
1806
1807
1808      TEST 52      TEST MODE 2 EVEN BYTE USING SOP INST.
1809
1810      003600 005212 000052
1811      003602 022712
1812      003606 001023
1813      003610 005000
1814      003612 105100
1815      003614 005200
1816      003616 005010
1817      003620 005110
1818      003622 105020
1819      003624 001404
1820
1821
1822
1823
1824      003626 012742 000072
1825      003632 005242
1826      003634 000000
1827      003636 005300
1828      003640 005210
1829      003642 105110
1830      003644 105220
1831      003646 100003
1832      003650 005300
1833      003652 105220
1834      003654 001404
1835
1836
1837
1838
1839      003656 012742 000073
1840      003656 005242
1841      003662 000000
1842      003664 000000
1843

;***** THIS TEST VERIFIES MODE 2 SINGLE OPERAND INSTRUCTIONS WHICH
;ADDRESS EVEN BYTES. R0 IS SET TO 400 AND USED TO INITIALIZE LOCATION
;400 TO -1. CLR8 INSTRUCTION IS THEN EXECUTED ON BYTE 400 WITH
;MODE 2.

;R0 IS THEN DECREMENTED BEFORE EACH OF SEVERAL MODE 2 INSTRUCTIONS
;WHICH ARE USED TO VERIFY THE DATA RESULTS OF THE TEST. THIS PROCEDURE ALSO
;VERIFIES THE PROPER INCREMENTING OF THE REGISTER.

;TEST 52      TEST MODE 2 EVEN BYTE USING SOP INST.

;***** TEST 52: INC (R2)      :UPDATE TEST NUMBER
;                  CMP $52,(R2)    :SEQUENCE ERROR?
;                  BNE TST53-10   :BR TO ERROR HALT ON SEQ ERROR
;                  CLR R0          :SET R0=400
;                  COMB R0
;                  INC R0
;                  CLR (R0)        :CLEAR 400
;                  COM (R0)        :INITIALIZE: 400=-1
;                  CLR8 (R0)+     :TRY TO CLEAT 400 W/MODE 2
;                  BEQ SOPB2A       ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;                                         CONDITIONAL BRANCH INST. AND
;                                         REPLACE THE MOVE INSTRUCTION
;                                         WHICH FOLLOWS W/ 771
;                                         <=====

;***** SOPB2A: MOV #72-(R2)      :MOVE TO MAILBOX # ***** 72 *****
;                  INC -(R2)        :SET MSGTYP TO FATAL ERROR
;                  HALT             :CLR DID NOT SET Z-BIT
;                  DEC R0            :RESULT R0=400
;                  INC (R0)        :INC 400 TO TEST WORD
;                  COMB (R0)        ;TRY TO INC EVEN BYTE
;                  INCB (R0)+     ;RESET R0=400
;                  BPL SOPB2B       ;TRY INCREMENT OF EVEN BYTE
;                  DEC R0            ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;                                         CONDITIONAL BRANCH INST. AND
;                                         REPLACE THE MOVE INSTRUCTION
;                                         WHICH FOLLOWS W/ 755
;                                         <=====

;***** SOPB2B: MOV #73-(R2)      :MOVE TO MAILBOX # ***** 73 *****
;                  INC -(R2)        :SET MSGTYP TO FATAL ERROR
;                  HALT             ;TEST CUMMULATIVE RESULT OF ABOVE INST.
;                                         OR SEQUENCE ERROR
;                                         <=====
```

MAINDEC-11-DFKAA-B 11-34 CPU TEST MACY!1 27(732) 01-OCT-76 15:03 PAGE 268  
 DFKAA.B.PII T52 TEST MODE 2 EVEN BYTE USING SOP INST.

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THIS TEST FOLLOWS THE SAME PROCEDURE DESCRIBED IN THE PREVIOUS TEST. HERE, THE BYTE INSTRUCTION IS USED TO ADDRESS AN ODD BYTE.

TEST 53 TEST MODE 2 ODD BYTE USING SOP INST.

TST53: INC (R2) ;UPDATE TEST NUMBER

CMP #53 (R2) ;SEQUENCE ERROR?

BNE TST54-10 ;BR TO ERROR HALT ON SEQ ERROR.

CLR R0 ;SET R0=400

COMB R0

INC R0

CLR (R0) ;CLEAR LOC 400

COM (R0) ;INITIALIZE: 400=-1

INC R0 ;R0=ODD BYTE

CLRB (R0)+ ;TRY TO CLEAR ODD BYTE

BEO SOPB2C

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 770

MOV #74 -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 74 \*\*\*\*\*

INC -(R2) ;SET MSGTYP TO FATAL ERROR

HALT ;CLRB DID NOT SET Z-BIT

;R0=WORD ADDR.

SOPB2C: DEC R0

DEC R0

INC (R0)+ ;INCREMENT WORD

DEC R0 ;POINT TO ODD BYTE

COMB (R0) ;COMPLEMENT ODD BYTE

INC B (R0)+ ;TRY TO INCREMENT ODD BYTE

BPL SOPB2D

DEC R0 ;RESET R0 TO ODD BYTE

INC B (R0)+ ;TRY TO INCREMENT ODD BYTE

BEO TST54

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 752

MOV #75 -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 75 \*\*\*\*\*

INC -(R2) ;SET MSGTYP TO FATAL ERROR

HALT ;TEST CUMMULATIVE RESULT OF ABOVE INST.

; OR SEQUENCE ERROR

MAINDEC-11-DFKAA-3 11 34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 269  
 DFKAA8.P11 T53 TEST MODE 2 000 BYTE USING SOP INST.

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1891
1892
1893      THESE TESTS CHECK THE NEGATE INSTRUCTION IN ALL MODES. PREVIOUSLY
1894      TESTED SINGLE-OPERAND INSTRUCTIONS ARE USED TO TEST THE NEGATE INSTRUCTION.
1895
1896
1897      TEST 54      TEST MODE 0 USING NEGATE INSTRUCTION
1898
1899 003762 005212      000054
1900 003764 022712      TST54: INC   (R2) ;UPDATE TEST NUMBER
1901 003770 001035      CMP   #54,(R2) ;SEQUENCE ERROR?
1902 003772 005000      BNE   TST55-10 ;BR TO ERROR HALT ON SEQ ERROR
1903 003774 005200      CLR   R0
1904 003776 005400      INC   R0
1905 004000 100003      NEG   R0
1906 004002 001402      BPL   NEGO0
1907 004004 102401      BEQ   NEGO0
1908 004006 103404      BVS   NEGO0
1909                               BCS   NEGO1
1910
1911
1912
1913 004010 012742      NEGO0: MOV   #76,-(R2)
1914 004010 012742      INC   -(R2)
1915 004014 005242      HALT
1916 004016 000000
1917 004020 005200      NEGO1: INC   R0
1918 004022 001404      BEQ   NEGO2
1919
1920
1921
1922
1923
1924 004024 012742      NEGO2: MOV   #77,-(R2)
1925 004030 005242      INC   -(R2)
1926 004032 000000      HALT
1927
1928 004034 105100      NEGO2: COMB
1929 004036 105400      NEGB
1930 004040 100403      BMI   NEGO3
1931 004042 001402      BEQ   NEGO3
1932 004044 102401      BVS   NEGO3
1933 004046 103404      BCS   NEGO4
1934
1935
1936
1937
1938 004050 012742      NEGO3: MOV   #100,-(R2)
1939 004050 012742      INC   -(R2)
1940 004054 005242      HALT
1941 004056 000000
1942 004060 005300      NEGO4: DEC   R0
1943 004062 001404      BEQ   TST55
1944
1945
1946

```

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 771 (=====)

MOVE TO MAILBOX # \*\*\*\*\* 76 \*\*\*\*\*  
 SET MSGTYP TO FATAL ERROR  
 NEGATE DID NOT SET CC'S CORRECTLY

TEST DATA RESULT

MOVE TO MAILBOX # \*\*\*\*\* 77 \*\*\*\*\*  
 SET MSGTYP TO FATAL ERROR  
 DATA RESULT OF NEGATE INCORRECT

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 763 (=====)

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 751 (=====)

MOVE TO MAILBOX # \*\*\*\*\* 100 \*\*\*\*\*  
 SET MSGTYP TO FATAL ERROR  
 NEGB DID NOT SET CC'S CORRECTLY

TEST DATA RESULT

REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 751 (=====)

MAINDEC-11-DFKAAB-8 11 34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 270  
DFKAAB.PII T54 TEST MODE 0 USING NEGATE INSTRUCTION

1947								
1948	004064	012742	000101	MOV	*101 -(R2)	WHICH FOLLOWS W/ 743	'===='	
1949	004070	005242		INC	-(R2)	MOVE TO MAILBOX # ***** 101 *****		
1950	004072	000000		HALT		SET MSGTYP TO FATAL ERROR		
1951						DATA RESULT OF NEGB INCORRECT		
1952						OR SEQUENCE ERROR		
1953				***** TEST 55 TEST MODE I USING NEGATE INST. *****				
1954				*****				
1955	004074	005212		TST55:	INC (R2)	UPDATE TEST NUMBER		
1956	004076	022712	000055	CMP	*55 -(R2)	SEQUENCE ERROR?		
1957	004102	001040		BNE	TST56-10	BR TO ERROR HALT ON SEQ ERROR		
1958	004104	005000		CLR	R0	POINT TO LOC. 0		
1959	004106	005010		CLR	(R0)	CLEAR LOC. 0		
1960	004110	005210		INC	(R0)	LOC. 0=1		
1961	004112	005410		NEG	(R0)	TRY NEG. LOC. 0=-1		
1962	004114	100003		BPL	NEG10	:CC=1001		
1963	004116	001402		BEQ	NEG10			
1964	004120	102401		BVS	NEG10			
1965	004122	103404		BCS	NEG11			
1966						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<===='	
1967						CONDITIONAL BRANCH INST. AND		
1968						REPLACE THE MOVE INSTRUCTION		
1969						WHICH FOLLOWS W/ 770		
1970	004124			NEG10:				
1971	004124	012742	000102	MOV	*102 -(R2)	MOVE TO MAILBOX # ***** 102 *****		
1972	004130	005242		INC	-(R2)	SET MSGTYP TO FATAL ERROR		
1973	004132	000000		HALT		NEGB DID NOT SET CC'S CORRECTLY		
1974								
1975	004134	005237	000000	NEG11:	INC	000	TEST DATA RESULT	
1976	004140	001404		BEQ	NEG12			
1977						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<===='	
1978						CONDITIONAL BRANCH INST. AND		
1979						REPLACE THE MOVE INSTRUCTION		
1980						WHICH FOLLOWS W/ 761		
1981	004142	012742	000103	MOV	*103 -(R2)	MOVE TO MAILBOX # ***** 103 *****		
1982	004146	005242		INC	-(R2)	SET MSGTYP TO FATAL ERROR		
1983	004150	000000		HALT		DATA RESULT OF NEGB INCORRECT		
1984	004152	105110		COMB	(R0)			
1985	004154	105410		NEGB	(R0)	:LOC. 0=377		
1986	004156	100403		BMI	NEG13	TRY NEGB LOC. 0=1		
1987	004160	001402		BEQ	NEG13	:CC=0001?		
1988	004162	102401		BVS	NEG13			
1989	004164	103404		BCS	NEG14			
1990						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<===='	
1991						CONDITIONAL BRANCH INST. AND		
1992						REPLACE THE MOVE INSTRUCTION		
1993						WHICH FOLLOWS W/ 747		
1994	004166			NEG13:				
1995	004166	012742	000104	MOV	*104 -(R2)	MOVE TO MAILBOX # ***** 104 *****		
1996	004172	005242		INC	-(R2)	SET MSGTYP TO FATAL ERROR		
1997	004174	000000		HALT		NEGB DID NOT SET CC'S CORRECTLY		
1998	004176	005337	000000	NEG14:	DEC	000	TEST DATA RESULT	
1999	004202	001404		BEQ	TST56			
2000						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<===='	
2001						CONDITIONAL BRANCH INST. AND		
2002						REPLACE THE MOVE INSTRUCTION		

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MAINDEC-III-DFKAAB-8 11 34 CPU TEST MACY(11 271732) 01-OCT-76 15:03 PAGE 271  
DFKAAB.P11 TSS TEST MODE 1 USING NEGATE INST.

2003  
2004 004204 012742 000105  
2005 004210 005246  
2006 004212 000000  
2007

MOV #105,-(R2)  
INC -(R2)  
HALT

WHICH FOLLOWS W/ 740  
MOVE TO MAILBOX # \*\*\*\*\* 105 \*\*\*\*\*  
SET MSGTYP TO FATAL ERROR  
DATA RESULT OF NEGB INCORRECT  
OR SEQUENCE ERROR

MAINDEC-11-DFKAAB-9 11 34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 272  
 DFKAAB 711 TSS TEST MODE 1 USING NEGATE INST.

2008							
2009							
2010							
2011	004214	005212					
2012	004216	022712	000056				
2013	004222	001032					
2014	004224	005000					
2015	004226	005010					
2016	004230	005210					
2017	004232	005420					
2018	004234	100003					
2019	004236	001402					
2020	004240	102401					
2021	004242	103404					
2022							
2023							
2024							
2025							
2026	004244						
2027	004244	012742	000106				
2028	004250	005242					
2029	004252	000000					
2030	004254	105300					
2031	004256	105300					
2032	004260	105420					
2033	004262	105420					
2034	004264	105340					
2035	004266	005300					
2036	004270	001404					
2037							
2038							
2039							
2040							
2041	004272	012742	000107				
2042	004276	005242					
2043	004300	000000					
2044	004302	005337	000000				
2045	004306	001404					
2046							
2047							
2048							
2049							
2050	004310	012742	000110				
2051	004314	005242					
2052	004316	000000					
2053							

```

:***** TEST 56 TEST MODE 2 USING NEGATE INSTRUCTION *****
:TST56: INC (R2) :UPDATE TEST NUMBER
          CMP #56, (R2) :SEQUENCE ERROR?
          BNE TST57-10 :BR TO ERROR HALT ON SEQ ERROR
          CLR R0 :POINT TO LOC. 0
          CLR (R0) :CLEAR LOC. 0
          INC (R0) :LOC. 0=1
          NEG (R0)+ :TRY NEG.: LOC. 0=-1
          BPL NEG20 :CC=1001?
          BEQ NEG20 :
          BVS NEG20 :
          BCS NEG21 :

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
: CONDITIONAL BRANCH INST. AND (=====
: REPLACE THE MOVE INSTRUCTION (=====
: WHICH FOLLOWS W/ 770 (=====

NEG20: MOV #106,-(R2) :MOVE TO MAILBOX # ***** 106 *****
       INC -(R2) :SET MSGTYP TO FATAL ERROR
       HALT :NEGATE DID NOT SET CC'S CORRECTLY
       DEC8 RO :RO=LOC. 0
       DEC8 RO :
       NEG8 (R0)+ :BYTE 0=1 RO=1
       NEG8 (R0)+ :BYTE 1=1 RO=2
       DEC8 -(R0) :RO=1 LOC. 0=01
       DEC RO :RO=0
       BEQ NEG22 :

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
: CONDITIONAL BRANCH INST. AND (=====
: REPLACE THE MOVE INSTRUCTION (=====
: WHICH FOLLOWS W/ 755 (=====

MOV #107,-(R2) :MOVE TO MAILBOX # ***** 107 *****
INC -(R2) :SET MSGTYP TO FATAL ERROR
HALT :REGISTER NOT INCREMENTED CORRECTLY
DEC Q#0 :LOC. 0=0
BEQ TST57 :

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
: CONDITIONAL BRANCH INST. AND (=====
: REPLACE THE MOVE INSTRUCTION (=====
: WHICH FOLLOWS W/ 746 (=====

MOV #110,-(R2) :MOVE TO MAILBOX # ***** 110 *****
INC -(R2) :SET MSGTYP TO FATAL ERROR
HALT :NEG BYTE INSTRUCTIONS FAILED
      : OR SEQUENCE ERROR

```

2054  
 2055  
 2056  
 2057 THIS TEST VERIFIES MODE 3 SINGLE OPERAND INSTRUCTIONS. IT  
 2058 USES LOCATION 0 AS ITS TARGET DATA. A TABLE LOCATED AT LOC. 400  
 2059 THRU 402 IS USED TO SUPPLY THE ADDRESS OF LOCATION 0 TO THE  
 2060 INSTRUCTIONS UNDER TEST.  
 2061 RD IS SET TO 400, THE START OF THE ADDRESS TABLE, AND A CLR.  
 2062 INSTRUCTION IS EXECUTED WITH MODE 3 TO CLEAR LOC. 0. THEN RD  
 2063 IS DECREMENTED BY TWO AND TWO OTHER MODE 3 INSTRUCTIONS OPERATE ON  
 2064 LOC. 0 TO VERIFY THE DATA RESULTS OF THE TEST. THE PROPER INCREMENTING  
 2065 OF THE REGISTER IS ALSO VERIFIED IN THIS MANNER.  
 2066 IF A FAILURE IS DETECTED BE SURE TO VERIFY THAT THE TABLE  
 2067 (LOC. 400-402) HAS THE PROPER VALUES (0).  
 2068  
 2069 TEST 57 TEST MODE 3 USING SOP INST.  
 2070  
 2071 004320 005212 000057  
 2072 TST57: INC (R2) ;UPDATE TEST NUMBER  
 2073 004322 022712 CMP #57,(R2) ;SEQUENCE ERROR?  
 2074 004326 001020 BNE TST60-10 ;BR TO ERROR HALT ON SEQ ERROR  
 2075 004330 005000 CLR RO ;SET RO=400  
 2076 004332 105100 COMB RO  
 2077 004334 005200 INC RO  
 2078 004336 005010 CLR (RO) ;CLEAR LOC 400  
 2079 004340 005030 CLR @RO)+ ;TRY TO CLEAR LOC 0 USING MODE 3 ;RO=402  
 2080 004342 001404 BEQ SOP3A  
 2081 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 2082 ; CONDITIONAL BRANCH INST. AND <=====  
 2083 ; REPLACE THE MOVE INSTRUCTION <=====  
 2084 ; WHICH FOLLOWS W/ 772 <=====  
 2085 004344 012742 000111  
 2086 004350 005242 MOV #111,-(R2) ;MOVE TO MAILBOX & \*\*\*\*\* 111 \*\*\*\*\*  
 2087 004352 000000 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2088 004354 005300 HALT ;CLR DID NOT SET Z-BIT  
 2089 004356 005300  
 2090 004360 005130 DEC RO ;RESET RO=400  
 2091 004362 100002 DEC RO  
 2092 004364 005230 COM @RO)+ ;TRY TO COMPLEMENT LOC 0 OF MODE 3 ;RO=402  
 2093 004366 001404 BPL SOP3B  
 2094 ; TRY TO INCREMENT LOC 0 W/MODE 3 ;RO=404  
 2095 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 2096 ; CONDITIONAL BRANCH INST. AND <=====  
 2097 ; REPLACE THE MOVE INSTRUCTION <=====  
 2098 ; WHICH FOLLOWS W/ 760 <=====  
 2099 004370 012742 000112  
 2100 004374 005242 SOP3A: MOV #112,-(R2) ;MOVE TO MAILBOX & \*\*\*\*\* 112 \*\*\*\*\*  
 2101 004376 000000 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2102 HALT ;CUMMULATIVE RESULT OF ABOVE INST FAILED  
 ; OR SEQUENCE ERROR

2103  
 2104  
 2105  
 2106  
 2107 THIS TEST VERIFIES MODE 3 SINGLE OPERAND BYTE INSTRUCTIONS  
 2108 WHICH ADDRESS EVEN BYTES. AGAIN, THE TARGET LOCATION 0 IS USED  
 2109 AND THE SAME TABLE AT 400 IS EMPLOYED.  
 2110 AFTER POINTING R4 TO THE TABLE (400) AND SETTING LOCATION  
 2111 0 TO -1, A CLRB INSTRUCTION IS USED TO CLEAR BYTE 0.  
 2112 SEVERAL OTHER MODE 3 INSTRUCTIONS ARE THEN USED WITH THE TABLE  
 2113 TO VERIFY THE DATA RESULTS AND THE PROPER INCREMENTING OF THE REGISTER.  
 2114 IF A FAILURE IS DETECTED, BE SURE THAT THE TABLE (LOCATION 400-402) HAS  
 2115 THE PROPER VALUES (0).

2116 TEST 60 TEST MODE 3 EVEN BYTE USING SOP INST.  
 2117  
 2118

2119 004400 005212	000060	TST60: INC (R2)	; UPDATE TEST NUMBER
2120 004402 022712		CMP #60, (R2)	; SEQUENCE ERROR?
2121 004406 001026		BNE TST61-10	; BR TO ERROR HALT ON SEQ ERROR
2122 004410 005004		CLR R4	; SET R4=400
2123 004412 105104		COMB R4	
2124 004414 005204		INC R4	
2125 004416 005000		CLR R0	; INITIALIZE LOC. 0=-1
2126 004420 005010		CLR (R0)	
2127 004422 005110		COM (R0)	; LOC. 0=-1
2128 004424 105034		CLRB @R4)+	; TRY TO CLEAR EVEN BYTE ;LOC. 0=177400 R4=402
2129 004426 001404		BEQ SOPB3A	
2130			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
2131			CONDITIONAL BRANCH INST. AND <=====
2132			REPLACE THE MOVE INSTRUCTION <=====
2133			WHICH FOLLOWS W/ 770 <=====
2134 004430 012742 000113		MOV #113, -(R2)	; MOVE TO MAILBOX # ***** 113 *****
2135 004434 005242		INC -(R2)	; SET MSGTYP TO FATAL ERROR
2136 004436 000000		HALT	; CLRB DID NOT SET Z-BIT
2137 004440 005304		SOPB3A: DEC R4	; RESET POINTER R4=400
2138 004442 005304		DEC R4	
2139 004444 005234		INC @R4)+	; TRY INCREMENTING WORD LOC. 0=177401 R4=402
2140 004446 100006		BPL SOPB3B	
2141 004450 105434		NEGB @R4)+	; TRY TO NEGATE EVEN BYTE ;LOC. 0=-1 R4=404
2142 004452 100004		BPL SOPB3B	
2143 004454 005304		DEC R4	; R4=402
2144 004456 005304		DEC R4	
2145 004460 105234		INCB @R4)+	; TRY TO INCREMENT EVEN BYTE ;LOC. 0=17400
2146 004462 001404		BEQ TST61	
2147			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
2148			CONDITIONAL BRANCH INST. AND <=====
2149			REPLACE THE MOVE INSTRUCTION <=====
2150			WHICH FOLLOWS W/ 752 <=====
2151 004464		SOPB3B: MOV #114, -(R2)	; MOVE TO MAILBOX # ***** 114 *****
2152 004464 012742 000114		INC -(R2)	; SET MSGTYP TO FATAL ERROR
2153 004470 005242		HALT	; CUMMULATIVE RESULT OF ABOVE INST FAILED
2154 004472 000000			; OR SEQUENCE ERROR
2155			

J04

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2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173 004474 005212
2174 004476 022712 000061
2175 004502 001024
2176 004504 005000
2177 004506 105100
2178 004510 005200
2179 004512 005030
2180 004514 005130
2181 004516 105030
2182 004520 001404
2183
2184
2185
2186
2187 004522 012742 000115
2188 004526 005242
2189 004530 000000
2190 004532 005300
2191 004534 005300
2192 004536 005300
2193 004540 005300
2194 004542 005230
2195 004544 105430
2196 004546 100092
2197 004550 105230
2198 004552 001404
2199
2200
2201
2202
2203 004554 012742 000115
2204 004554 004554 000115
2205 004560 005242
2206 004562 000000
2207

;***** THIS TEST VERIFIES MODE 3 SINGLE OPERAND BYTE INSTRUCTIONS
;WHICH ADDRESS ODD BYTES. THE TARGET IS BYTE 1. A TABLE AT
;LOC. 400-406 IS USED. R0 SERVES AS THE TABLE POINTER.
;R0 IS INITIALIZED TO 400. LOC. 0 IS SET TO -1 USING THE
;FIRST TWO TABLE ENTRIES. A CLRB MODE 3 IS EXECUTED ON BYTE 1 USING
;TABLE ADDRESS AT 404. R0 IS DECREMENTED TO 402 AND SEVERAL SOP
;MODE 3 INSTRUCTIONS ARE USED TO VERIFY DATA RESULTS AND PROPER
;REGISTER INCREMENTING.
;THE TABLE (400-406) SHOULD CONTAIN 0,0,1,1 BEFORE AND
;AFTER THE TEST IS RUN.

;***** TEST 61 TEST MODE 3 ODD BYTE USING SOP INST.
;***** TST61: INC (R2) ;UPDATE TEST NUMBER
;              CMP #61,(R2) ;SEQUENCE ERROR?
;              BNE TST62-10 ;BR TO ERROR HALT ON SEQ ERROR
;              CLR R0 ;SET R0=400
;              COMB R0
;              INC R0
;              CLR @((R0)+) ;INITIALIZE
;              COM @((R0)+) ;LOC 0=-1 R0=404
;              CLRB @((R0)+) ;TRY TO CLEAR ODD BYTE LOC. 0=377 R0=406
;              BEQ SOPB3C ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
;                           CONDITIONAL BRANCH INST. AND <=====
;                           REPLACE THE MOVE INSTRUCTION <=====
;                           WHICH FOLLOWS W/ 771 <=====

;              MOV #115,-(R2) ;MOVE TO MAILBOX # ***** 115 *****
;              INC -(R2) ;SET MSGTYP TO FATAL ERROR
;              HALT ;CLRB DID NOT SET Z-BIT
;              DEC R0 ;RESET R0=402
;              DEC R0
;              DEC R0
;              DEC R0
;              INC @((R0)+) ;POINT TO EVEN BYTE ADDR.
;              NEGB @((R0)+)
;              BPL SOPB3D ;TRY TO NEGATE ODD BYTE LOC. 0=177400 R0=406
;              INCB @((R0)+) ;TRY TO INCREMENT ODD BYTE LOC.0=0 R0=410
;              BEQ TST62 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
;                           CONDITIONAL BRANCH INST. AND <=====
;                           REPLACE THE MOVE INSTRUCTION <=====
;                           WHICH FOLLOWS W/ 754 <=====

;              MOV #116,-(R2) ;MOVE TO MAILBOX # ***** 116 *****
;              INC -(R2) ;SET MSGTYP TO FATAL ERROR
;              HALT ;CUMMULATIVE RESULT OF ABOVE INSTS FAILED
;                   ; OR SEQUENCE ERROR

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## K04

MAINDEC-11-DFKF7-B 11.34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 276  
 DFKAAB.P11 T51 TEST MODE 3 ODD BYTE USING SOP INST.

```

2208
2209
2210
2211 004564 005212 ;***** TEST MODE 3 USING NEGATE INSTRUCTION *****
2212 004566 022712 000062 ;TEST 62
2213 004572 001054 TST62: INC (R2) ;UPDATE TEST NUMBER
2214 004574 005000 CMP #62, (R2) ;SEQUENCE ERROR?
2215 004576 105100 BNE TST63-10 ;BR TO ERROR HALT ON SEQ ERROR
2216 004600 005200 CLR R0 ;R0=400
2217 004602 005010 COMB RO
2218 004604 005004 INC RO
2219 004606 005014 CLR (R0) ;LOC. 400=0
2220 004610 005214 CLR R4 ;R4=0
2221 004612 005430 INC (R4) ;LOC. 0=0
2222 004614 100003 NEG @ (R0)+ ;TRY NEGATE LOC. 0=-1 RC=402
2223 004616 001402 BPL NEG30 ;CC=1001?
2224 004620 102401 BEQ NEG30
2225 004622 103404 BVS NEG30
2226
2227
2228
2229
2230 004624 012742 000117 BCS NEG31 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====>
2231 004624 012742 000117 NEG30: MOV #117, -(R2) ;CONDITIONAL BRANCH INST. AND <=====>
2232 004630 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR <=====>
2233 004632 000000 HALT ;NEG DID NOT SET CC'S CORRECTLY <=====>
2234 004634 005214 INC (R4) ;LOC. 0=0 <=====>
2235 004636 001404 BEQ NEG32 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====>
2236
2237
2238
2239
2240 004640 012742 000120 NEG32: MOV #120, -(R2) ;CONDITIONAL BRANCH INST. AND <=====>
2241 004644 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR <=====>
2242 004646 000000 HALT ;DATA RESULT OF NEG INCORRECT <=====>
2243 004650 105137 000001 COMB @#1 ;LOC 0=177400
2244 004654 005237 000000 INC @#0 ;LOC. 0=177401
2245 004660 105430 NEG8 @ (R0)+ ;TRY NEG8 LOC. 0=177777 RO=404
2246 004662 100404 BMI NEG33 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====>
2247
2248
2249
2250
2251 004664 012742 000121 NEG33: MOV #121, -(R2) ;CONDITIONAL BRANCH INST. AND <=====>
2252 004670 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR <=====>
2253 004672 000000 HALT ;NEG8 FAILED WITH EVEN BYTE <=====>
2254 004674 105430 NEGB @ (R0)+ ;TRY NEGB LOC.0=777 RO=406 <=====>
2255 004676 100004 BPL NEG34 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====>
2256
2257
2258
2259
2260 004700 012742 000122 NEG34: MOV #122, -(R2) ;CONDITIONAL BRANCH INST. AND <=====>
2261 004704 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR <=====>
2262 004706 000000 HALT ;NEG8 FAILED WITH ODD BYTE <=====>
2263 004710 105137 000001 COMB @#1 ;LOC. 0=177377 <=====>

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L04

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 277  
DFKAAB.P11 T62 TEST MODE 3 USING NEGATE INSTRUCTION

2264 004714 105237 000001	INC B	#1	;LOC. 0=177777
2265 004720 005214	INC	(R4)	;LOC. 0=0
2266 004722 001404	BEQ	TST63	
2267			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
2268			CONDITIONAL BRANCH INST. AND
2269			REPLACE THE MOVE INSTRUCTION
2270			WHICH FOLLOWS W/ 724
2271 004724 012742 000123	MOV	*123,-(R2)	;MOVE TO MAILBOX * ***** 123 *****
2272 004730 005242	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
2273 004732 000000	HALT		;DATA RESULT OF NEGB'S INCORRECT
2274			; OR SEQUENCE ERROR

2275  
 2276 \*\*\*\*\*  
 2277  
 2278 THIS TEST VERIFIES MODE 4 SINGLE OPERAND INSTRUCTIONS.  
 2279 ;R0 IS SET TO 400. A CLR INSTRUCTION IS EXECUTED IN MODE 4 TO CLEAR  
 2280 ;LOC. 376. R0 IS RESET TO 400 AND A COM INSTRUCTION USING MODE 4  
 2281 ;COMPLEMENTS LOC. 376.  
 2282 ;TWO INC INSTRUCTIONS AND A MODE 4 INSTRUCTION ARE EXECUTED  
 2283 ;TO COMPLETE THE TEST.  
 2284 \*\*\*\*\*  
 2285 ;TEST 63 TEST MODE 4 USING SOP INSTS  
 2286 \*\*\*\*\*  
 2287 004734 005212 000063  
 2288 004736 022712 000063  
 2289 004742 001021 000063  
 2290 004744 005000 000063  
 2291 004746 105100 000063  
 2292 004750 005200 000063  
 2293 004752 005040 000063  
 2294 004754 001404 000063  
 TST63: INC (R2) ;UPDATE TEST NUMBER  
       CMP #63, (R2) ;SEQUENCE ERROR?  
       BNE TST64-10 ;BR TO ERROR HALT ON SEQ ERROR  
       CLR R0 ;SET R0=400  
       COMB R0  
       INC R0  
       CLR -(R0) ;TRY TO CLEAR USING MODE 4  
       BEQ SOP4A ;  
                  ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
                  ; CONDITIONAL BRANCH INST. AND <=====  
                  ; REPLACE THE MOVE INSTRUCTION <=====  
                  ; WHICH FOLLOWS W/ 773 <=====  
 2295 004756 012742 000124  
 2296 004762 005242 000124  
 2297 004764 000000 000124  
 2298 004766 005200 000124  
 2299 004770 005200 000124  
 2300 004772 005140 000124  
 2301 004774 100004 000124  
 2302 004776 005200 000124  
 2303 005000 005200 000124  
 2304 005002 005240 000124  
 2305 005004 001404 000124  
 SOP4A: MOV #124, -(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 124 \*\*\*\*\*  
       INC -(R2) ;SET MSGTYP TO FATAL ERROR  
       HALT ;CLR DID NOT SET Z-BIT  
       INC R0 ;RESET R0  
       INC R0  
       COM -(R0) ;TRY TO COMPLEMENT USING MODE 4  
       BPL SOP4B ;  
       INC R0 ;MOVE POINTER  
       INC R0  
       INC -(R0) ;  
       BEQ TST64 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
                  ; CONDITIONAL BRANCH INST. AND <=====  
                  ; REPLACE THE MOVE INSTRUCTION <=====  
                  ; WHICH FOLLOWS W/ 757 <=====  
 2310 005006 012742 000125  
 2311 005008 005242 000125  
 2312 005012 005242 000125  
 2313 005014 000000 000125  
 SOP4B: MOV #125, -(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 125 \*\*\*\*\*  
       INC -(R2) ;SET MSGTYP TO FATAL ERROR  
       HALT ;CHECK CUMMULATIVE RESULT OF ABOVE INST.  
                  ; OR SEQUENCE ERROR

2319  
 2320 ;\*\*\*\*\*  
 2321  
 2322 THIS TEST VERIFIES MODE 5 SINGLE OPERAND INSTRUCTIONS. IT  
 2323 USES LOCATION 0 AS ITS TARGET DATA. A TABLE LOCATED AT LOC. 372  
 2324 THRU 374 IS USED TO SUPPLY THE ADDRESS OF LOCATION 0 TO THE  
 2325 INSTRUCTIONS UNDER TEST.  
 2326 RO IS SET TO 376, (THE START OF THE ADDRESS TABLE) +2,  
 2327 AND A CLR INSTRUCTION IS EXECUTED WITH MODE 3 TO CLEAR  
 2328 LOC. 0. THEN RO IS INCREMENTED BY TWO AND TWO OTHER MODE 3  
 2329 INSTRUCTIONS OPERATE ON LOC. 0 TO VERIFY THE DATA RESULTS OF  
 2330 THE TEST. THE PROPER DECREMENTING OF THE REGISTER IS ALSO  
 2331 VERIFIED IN THIS MANNER.  
 2332 IF A FAILURE IS DETECTED BE SURE TO VERIFY THAT THE TABLE  
 2333 (LOC. 372 THRU 374) HAS THE PROPER VALUES (0).  
 2334  
 2335 ;\*\*\*\*\*  
 2336 TEST 64 TEST MODE 5 USING SOP INSTS  
 2337 ;\*\*\*\*\*  
 2338 005016 005212 000064  
 2339 005020 022712  
 2340 005024 001017  
 2341 005026 005000  
 2342 005030 005020  
 2343 005032 105400  
 2344 005034 005050  
 2345 005036 0C1404  
 2346 ;TST64: INC (R2) ;UPDATE TEST NUMBER  
 2347 CMP #64, (R2) ;SEQUENCE ERROR?  
 2348 BNE TST65-10 ;BR TO ERROR HALT ON SEQ ERROR  
 2349 CLR RO ;SET RO=376  
 2350 NEG8 RO  
 2351 CLR (R0)+  
 2352 CLR @-(RO)  
 2353 BEQ SOP5A ;TRY TO CLEAR LOC 0 W/MODE 5  
 2354 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 2355 ; CONDITIONAL BRANCH INST. AND  
 2356 ; REPLACE THE MOVE INSTRUCTION  
 2357 ; WHICH FOLLOWS W/ 773  
 2358 005040 012742 000126  
 2359 MOV #126, -(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 126 \*\*\*\*\*  
 2360 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2361 HALT ;CLR DID NOT SET Z-BIT  
 2362 ;RESET RO  
 2363 005044 005242  
 2364 005046 000000  
 2365 005050 005200  
 2366 005052 005200  
 2367 005054 005150  
 2368 005056 100002  
 2369 005060 005250  
 2370 005062 001404  
 2371 ;SOP5A: INC RO  
 2372 INC RO  
 2373 COM @-(RO) ;TRY TO COMPLEMENT LOC. 0 W/MODE 5  
 2374 BPL SOP5B  
 2375 INC @-(RO) ;TRY TO INCREMENT LOC. 0 W/MODE 5  
 2376 BEQ TST65 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 2377 ; CONDITIONAL BRANCH INST. AND  
 2378 ; REPLACE THE MOVE INSTRUCTION  
 2379 ; WHICH FOLLOWS W/ 761  
 2380 005064 012742 000127  
 2381 ;SOP5B: MOV #127, -(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 127 \*\*\*\*\*  
 2382 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2383 HALT ;TEST CUMMULATIVE RESULT OF ABOVE INSTS  
 2384 ; OR SEQUENCE ERROR

THIS TEST VERIFIES MODE 6 SINGLE OPERAND INSTRUCTIONS. IT  
 USES LOCATION 0 AS ITS TARGET DATA. R0 IS SET TO 400 USING  
 PREVIOUSLY TESTED INSTRUCTIONS AND A MODE 6 CLR INSTRUCTION IS  
 EXECUTED ON LOC. 0 USING R0 AND A -400 OFFSET. COM AND INC  
 INSTRUCTIONS ARE THEN USED TO VERIFY THE DATA.  
  
 TEST 65 TEST MODE 6 USING SOP INSTS  
  
 TST65: INC (R2) ;UPDATE TEST NUMBER  
 CMP #65,(R2) ;SEQUENCE ERROR?  
 PNE TST65-10 ;BR TO ERROR HALT ON SEQ ERROR  
 CLR R0 ;SET R0=400  
 COMB R0  
 INC R0  
 CLR -400(R0) ;TRY TO CLEAR LOCATION 0 W/MODE 6  
 BEQ SOP6A ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND (=====)  
 ; REPLACE THE MOVE INSTRUCTION (=====)  
 ; WHICH FOLLOWS W/ 772 (=====)  
 MOV \*130,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 130 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;CLR DID NOT SET Z-BIT  
 SOP6A: COM -400(R0) ;TRY TO COMPLEMENT LOCATION 0 W/MODE 6  
 BPL SOP6B ;TRY TO INCREMENT LOCATION 0 W/MODE 6  
 INC -400(R0) ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 BEQ TST66 ; CONDITIONAL BRANCH INST. AND (=====)  
 ; REPLACE THE MOVE INSTRUCTION (=====)  
 ; WHICH FOLLOWS W/ 760 (=====)  
 MOV \*131,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 131 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;TEST CUMMULATIVE RESULT OF ABOVE INSTS  
 ; OR SEQUENCE ERROR (=====)

2408  
 2409  
 2410  
 2411  
 2412  
 2413  
 2414  
 2415  
 2416  
 2417  
 2418  
 2419  
 2420  
 2421 005154 005212 000066  
 2422 005156 022712  
 2423 005162 001021  
 2424 005164 005000  
 2425 005166 105100  
 2426 005170 005200  
 2427 005172 005210  
 2428 005174 005070 000002  
 2429 005200 001404

\*\*\*\*\*  
 THIS TEST VERIFIES MODE 7 SINGLE OPERAND INSTRUCTIONS. IT USES  
 THE POINTER TO LOC. 0 WHICH IS STORED AT LOC. 402.  
 R0 IS SET TO 400 AND A MODE 7 CLR INSTRUCTION IS  
 EXECUTED WITH A +2 OFFSET TO CLEAR LOC. 0.  
 SEVERAL OTHER MODE 7 INSTRUCTIONS ARE THEN USED ON THE COMMON  
 LOCATION TO VERIFY THE DATA RESULTS.

\*\*\*\*\*  
 TEST 66 TEST MODE 7 USING SOP INST.

\*\*\*\*\*  
 TST66: INC (R2) ;UPDATE TEST NUMBER  
 CMP #6E,(R2) ;SEQUENCE ERROR?  
 BNE TST67-10 ;BR TO ERROR HALT ON SEQ ERROR  
 CLR R0 ;SET R0=400

INC (R0) ;R0=1  
 CLR #2(R0) ;TRY TO CLEAR LOC. 0 W/MODE 7  
 BEQ SOP7A

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 771 <=====

MOV #132,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 132 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;CLR DID NOT SET Z-BIT  
 SOP7A: COM #2(P) ;TRY TO COMPLEMENT LOC. 0 W/MODE 7  
 BPL #8 ;TRY TO INCREMENT LOC. 0 W/MODE 7  
 INC #-(R0) ;TRY TO INCREMENT LOC. 0 W/MODE 7  
 BEQ TST67

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 757 <=====

SOP7B: MOV #133,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 133 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;TEST CUMMULATIVE RESULT OF ABOVE INSTS.  
 ; OR SEQUENCE ERROR

DOS

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DFKAA-B.P11 T56 TEST MODE ? USING SOP INST.

MAINDEC-11-DFKAA-9 11 34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 283  
DFKAA8.P11 T67 TEST MODE 4 WITH NEGATE INSTRUCTION

2492							
2493							
2494							
2495	005326	005212					
2496	005330	022712	000070				
2497	005334	001031					
2498	005336	005000					
2499	005340	005010					
2500	005342	105100					
2501	005344	005200					
2502	005346	005010					
2503	005350	005004					
2504	005352	005314					
2505	005354	005450					
2506	005356	100403					
2507	005360	001402					
2508	005362	102401					
2509	005364	103404					
2510							
2511							
2512							
2513							
2514	005366						
2515	005366	012742	000137				
2516	005372	005242					
2517	005374	000000					
2518	005376	005314					
2519	005400	001404					
2520							
2521							
2522							
2523							
2524	005402	012742	000140				
2525	005406	005242					
2526	005410	000000					
2527	005412	105100					
2528	005414	005300					
2529	005416	001404					
2530							
2531							
2532							
2533							
2534	005420	012742	000141				
2535	005424	005242					
2536	005426	000000					
2537							

\*\*\*\*\* TEST 70 TEST MODE 5 WITH NEGATE INSTRUCTION \*\*\*\*\*  
 TST70: INC (R2) ;UPDATE TEST NUMBER  
 CMP \$70,(R2) ;SEQUENCE ERROR?  
 BNE TST71-10 ;BR TO ERROR HALT ON SEQ ERROR  
 CLR R0 ;R0=0  
 CLR (R0) ;LOC. 0=0  
 COMB R0 ;R0=377  
 INC R0 ;R0=400  
 CLR (R0) ;SET 400 = 0  
 CLR R4 ;R4=0  
 DEC (R4) ;LOC. 0=177777  
 NEG @-(R0) ;TRY NEGATE: LOC. 0=1  
 BMI NEG50 ;CC=0001?  
 BEQ NEG50  
 BVS NEG50  
 BCS NEG51  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 764 <=====  
 NEG50:  
 MOV #137,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 137 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;NEG DID NOT SET CC'S CORRECTLY  
 NEG51:  
 DEC (R4) ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 BEQ NEG52 ;CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 756 <=====  
 ;MOVE TO MAILBOX # \*\*\*\*\* 140 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;DATA RESULT OF NEG INCORRECT  
 NEG52:  
 MOV #140,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 140 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;REGISTER NOT DECREMENTED PROPERLY  
 ; OR SEQUENCE ERROR.  
 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 747 <=====  
 ;MOVE TO MAILBOX # \*\*\*\*\* 141 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;REGISTER NOT DECREMENTED PROPERLY  
 ; OR SEQUENCE ERROR.

MAINDEC-11-DFKAAB.B 11:34 CPU TEST MACY!! 27(732) 01-OCT-76 15:03 PAGE 284  
DFKAAB.P11 T70 TEST MODE 5 WITH NEGATE INSTRUCTION

2538				*****	
2539				TEST 71 TEST MODE 6 WITH NEGATE	
2540				*****	
2541	005430	005212	000071	TST71: INC (R2)	UPDATE TEST NUMBER
2542	005432	022712		CMP #71, (R2)	SEQUENCE ERROR?
2543	005436	001022		BNE TST72-10	BR TO ERROR HALT ON SEQ ERROR
2544	005440	005000		CLR R0	R0=0
2545	005442	005004		CLR R4	R4=0
2546	005444	105100		COMB R0	R0=377
2547	005446	005014		CLR (R4)	LOC. 0=0
2548	005450	105024		CLRB (R4)+	LOC. 0=177777, R4=1
2549	005452	105114		COMB (R4)	LOC. 0=177400
2550	005454	005460	177401	NEG -377(R0)	LOC. 0=400
2551	005460	100403		BMI NEG60	CC=0001
2552	005462	001402		BEQ NEG60	
2553	005464	102401		BVS NEG60	
2554	005466	103404		BCS NEG61	
2555				;	TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
2556				;	CONDITIONAL BRANCH INST. AND
2557				;	REPLACE THE MOVE INSTRUCTION
2558				;	WHICH FOLLOWS W/ 764
2559	005470			NEG60:	<=====
2560	005470	012742	000142	MOV #142 -(R2)	MOVE TO MAILBOX # ***** 142 *****
2561	005474	005242		INC -(R2)	SET MSGTYP TO FATAL ERROR
2562	005476	000000		HALT	NEG DID NOT SET CC'S CORRECTLY
2563	005500	105314		NEG61: DECB (R4)	
2564	005502	001404		BEQ TST72	
2565				;	TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
2566				;	CONDITIONAL BRANCH INST. AND
2567				;	REPLACE THE MOVE INSTRUCTION
2568				;	WHICH FOLLOWS W/ 756
2569	005504	012742	000143	MOV #143 -(R2)	MOVE TO MAILBOX # ***** 143 *****
2570	005510	005242		INC -(R2)	SET MSGTYP TO FATAL ERROR
2571	005512	000000		HALT	DATA RESULT OF NEG INCORRECT
2572				;	OR SEQUENCE ERROR

## GOS

MAINDEC-11-DFKAA-B 11 34 CPU TEST MACYII 27(732) 01-OCT-76 15:03 PAGE 285  
 DFKAAB.P11 T1 TEST MODE 5 WITH NEGATE

```

2573
2574
2575
2576 005514 005212 :***** TEST 72 TEST MODE 7 W/ NEGATE *****
2577 005516 022712 000072 :***** TST72: INC (R2) :UPDATE TEST NUMBER *****
2578 005522 001024 :***** CMP #72,(R2) :SEQUENCE ERROR? *****
2579 005524 005000 :***** BNE TST73-10 :BR TO ERROR HALT ON SEQ ERROR *****
2580 005526 005010 :***** CLR R0 :R0=0 *****
2581 005530 005110 :***** CLR (R0) :LOC. 0=0 *****
2582 005532 105100 :***** COM (R0) :LOC. 0=177777 *****
2583 005534 105470 000005 :***** COMB R0 :R0=377 *****
2584 005540 100403 :***** NEGB $5(R0) :R0+5=404, 404=1, LOC. 0=777 *****
2585 005542 001402 :***** BMI NEG70 :CC=0001? *****
2586 005544 102401 :***** BEQ NEG70 *****
2587 005546 103404 :***** BVS NEG70 *****
2588 :***** BCS NEG71 :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS *****
2589 :***** :CONDITIONAL BRANCH INST. AND <===== *****
2590 :***** :REPLACE THE MOVE INSTRUCTION <===== *****
2591 :***** :WHICH FOLLOWS W/ 766 <===== *****
2592 005550
2593 005550 012742 000144 :***** NEG70: MOV #144,-(R2) :MOVE TO MAILBOX # ***** 144 *****
2594 005554 005242 :***** INC -(R2) :SET MSGTYP TO FATAL ERROR *****
2595 005556 000000 :***** HALT :NEG DID NOT SET CC'S CORRECTLY *****
2596 005560 105100 :***** COMB R0 :R0=0 *****
2597 005562 105120 :***** COMB (R0)+ :LOC. 0=400, R0=1 *****
2598 005564 105310 :***** DECB (R0) :LOC. 0=0 *****
2599 005566 005467 172206 :***** NEG 0 :USE NEG MODE 67 TO TST FOR ZERO *****
2600 005572 001404 :***** BEQ TST73 :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS *****
2601 :***** :CONDITIONAL BRANCH INST. AND <===== *****
2602 :***** :REPLACE THE MOVE INSTRUCTION <===== *****
2603 :***** :WHICH FOLLOWS W/ 754 <===== *****
2604
2605 005574 012742 000145 :***** MOV #145,-(R2) :MOVE TO MAILBOX # ***** 145 *****
2606 005600 005242 :***** INC -(R2) :SET MSGTYP TO FATAL ERROR *****
2607 005602 000000 :***** HALT :DATA RESULT OF NEG WAS INCORRECT *****
2608 :***** :OR SEQUENCE ERROR
  
```

2609  
 2610  
 2611  
 2612 :\*\*\*\*\*  
 2613 : THIS TEST VERIFIES PROGRAM COUNTER ADDRESSING WITH SOP  
 2614 : INSTRUCTIONS. CLR MODE 77 IS USED TO CLEAR THE LOCATION FOLLOWING THE  
 2615 : INSTRUCTION (SOPX). THEN SINGLE OPERAND INSTRUCTIONS WITH MODES 37, 67, AND  
 2616 : 77. USING INDIRECT POINTER SOPXAD ARE USED TO VERIFY THE DATA RESULTS  
 2617 : OF THESE INSTRUCTIONS.  
 2618 :\*\*\*\*\*  
 2619 :TEST 73 TEST SOP INSTRUCTIONS MODES 2,3,6,7 WITH REGISTER 7  
 2620 :\*\*\*\*\*  
 2621 005604 005212 000073  
 2622 005606 022712 000073  
 2623 005612 001017  
 2624 005614 005027  
 2625 005616 177777  
 2626 005620 001404  
 2627  
 2628  
 2629  
 2630  
 2631 005622 012742 000146  
 2632 005626 005242  
 2633 005630 000000  
 2634 005632 005237 005616  
 2635 005636 005467 177754  
 2636 005642 100003  
 2637 005644 005277 000012  
 2638 005650 001405  
 2639  
 2640  
 2641  
 2642  
 2643 005652  
 2644 005652 012742 000147  
 2645 005656 005242  
 2646 005660 000000  
 2647  
 2648 005662 005616

			TST?3:	INC (R2)	: UPDATE TEST NUMBER
				CMP #73, (R2)	: SEQUENCE ERROR?
				BNE SOPB	: BR TO ERROR HALT ON SEQ ERROR
			SOPX:	CLR (R7)+	: CLEAR NEXT LOCATION: (SOPX)
				-1	: USE MODE 27
				BEQ SOPA	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 775 <=====
				MOV #146, -(R2)	: MOVE TO MAILBOX # ***** 146 *****
				INC -(R2)	: SET MSGTYP TO FATAL ERROR
			SOPA:	HALT	: CLR DID NOT SET Z-BIT
				INC @SOPX	: INC SOPX W/MODE 37
				NEG SOPX	: NEGATE SOPX W/MODE 67
				BPL SOPB	
				INC @SOPXAD	: INC SOPX W/MODE 77
				BEQ TST74	: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 761 <=====
			SOPB:	MOV #147, -(R2)	: MOVE TO MAILBOX # ***** 147 ***** .
				INC -(R2)	: SET MSGTYP TO FATAL ERROR
				HALT	: INC DID NOT SET Z-BIT OR SEQUENCE ERROR
			SOPXAD:	SOPX	: INDIRECT ADDRESS OF SOPX

105

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DFKRAAB.P11 T73 TEST SOP INSTRUCTIONS MODES 2,3,6,7 WITH REGISTER 7

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2649
2650
2651
2652 **** THIS TEST VERIFIES SINGLE OPERAND NON-MODIFYING INSTRUCTIONS
2653 USING MODE 0. R0 IS SET TO ZERO AND THE CONDITION CODES ARE SET
2654 TO THE COMPLEMENT OF THAT EXPECTED BY THE INSTRUCTION. A TST INSTRUCTION
2655 IS EXECUTED AND CONDITIONAL BRANCHES ARE USED TO TEST THE CONDITION
2656 CODES.
2657
2658 **** TEST 74 TEST MODE 0 SOP NON-MODIFYING
2659
2660 ****
2661 005664 005212
2662 005666 022712 000074
2663 005672 001010
2664 005674 005000
2665 005676 000277
2666 005700 000244
2667 005702 005700
2668 005704 102403
2669 005706 100402
2670 005710 103401
2671 005712 001404
2672
2673
2674
2675
2676 005714
2677 005714 012742 000150
2678 005720 005242
2679 005722 000000
2680

TST74: INC      (R2)          ; UPDATE TEST NUMBER
       CMP      #74,(R2)        ; SEQUENCE ERROR?
       BNE      TST75-10       ; BR TO ERROR HALT ON SEQ ERROR
       CLR      R0              ; INITIALIZE R0=0
       SCC      R0              ; SET CC=1011
       CLZ
       TST      R0              ; TRY TST W/ MODE 0
       BVS      SNMOA           ; CHECK THAT CC=0100
       BMI      SNMOA
       BCS      SNMOA
       BEQ      TST75
                           ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
                           ; CONDITIONAL BRANCH INST. AND      <=====
                           ; REPLACE THE MOVE INSTRUCTION      <=====
                           ; WHICH FOLLOWS W/ ??0      <=====

SNMOA: MOV      #150,-(R2)    ; MOVE TO MAILBOX * ***** 150 *****
       INC      -(R2)          ; SET MSGTYP TO FATAL ERROR
       HALT

```

2681  
 2682  
 2683  
 2684  
 2685 THIS TEST VERIFIES SINGLE OPERAND NON-MODIFYING BYTE INSTRUCTIONS WITH MODE 0.  
 2686 : R0 IS SET TO 377 AND COMPLEMENT OF THE EXPECTED CONDITION CODES  
 2687 : IS LOADED IN PSW. A TSTB INSTRUCTION IS EXECUTED AND THE RESULTS  
 2688 : ARE CHECKED WITH SEVERAL CONDITIONAL BRANCH INSTRUCTIONS.  
 2689 : THIS VERIFIES THAT THE PROPER BYTE WAS TESTED.  
 2690  
 2691 TEST 75 TEST MODE 0 EVEN BYTE W/ SOP NON-MODIFYING  
 2692 :  
 2693 005724 005212 000075 TST75: INC (R2) ;UPDATE TEST NUMBER  
 2694 005726 022712 CMP #75,(R2) ;SEQUENCE ERROR?  
 2695 005732 001010 BNE TST76-10 ;BR TO ERROR HALT ON SEQ ERROR  
 2696 005734 005000 CLR R0 ;INITIALIZE  
 2697 005736 105100 COMB R0 ;R0=377  
 2698 005740 000277 SCC ;SET CC=0111  
 2699 005742 000250 CLN  
 2700 005744 105700 TSTB R0 ;TRY TST EVEN BYTE  
 2701 005746 102402 BVS SNMBOA ;CHECK CC=1000  
 2702 005750 101401 BLOS SNMBOA  
 2703 005752 100404 BMI TST76  
 2704 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 2705 : CONDITIONAL BRANCH INST. AND <=====  
 2706 : REPLACE THE MOVE INSTRUCTION <=====  
 2707 : WHICH FOLLOWS W/ 770 <=====  
 2708 005754 SNMBOA:  
 2709 005754 012742 000151 MOV #151,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 151 \*\*\*\*\*  
 2710 005760 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2711 005762 000000 HALT ;CONDITION CODES NOT SET PROPERLY  
 2712 : OR SEQUENCE ERROR

-5-

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2725 005764 005212
2726 005766 022712 000076
2727 005772 001011
2728 005774 005000
2729 005776 005010
2730 006000 000277
2731 006002 000244
2732 006004 005710
2733 006006 102403
2734 006010 103402
2735 006012 100401
2736 006014 001404
2737
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2741 006016
2742 006016 012742 000152
2743 006022 005242
2744 006024 000000
2745

***** THIS TEST VERIFIES SINGLE OPERAND INSTRUCTIONS WITH MODE 1.
;R0 IS USED TO POINT TO AND CLEAR LOC. 0. THE COMPLEMENT OF THE
;EXPECTED CONDITION CODES ARE LOADED IN THE PSW. A TST INSTRUCTION
;IS THEN EXECUTED ON LOC. 0 USING R0 AND CONDITIONAL BRANCHES TEST
;THE RESULTS.

***** TEST 76 TEST MODE 1 SOP NON-MODIFYING *****
TST76: INC (R2) ;UPDATE TEST NUMBER
       CMP #76,(R2) ;SEQUENCE ERROR?
       BNE TST77-10 ;BR TO ERROR HALT ON SEQ ERROR
       CLR R0 ;POINT TO LOC 0
       CLR (R0) ;CLEAR LOC 0
       SCC ;INITIALIZE
       CLZ ;CC=1011
       TST (R0) ;TRY TST W/ MODE 1
       BVS SNM1A ;CHECK CC=0100
       BCS SNM1A
       BMI SNM1A
       BEQ TST77 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
;: CONDITIONAL BRANCH INST. AND <=====
;: REPLACE THE MOVE INSTRUCTION <=====
;: WHICH FOLLOWS W/ 767 <=====

SNM1A:
       MOV #152,-(R2) ;MOVE TO MAILBOX * ***** 152 *****
       INC -(R2) ;SET MSGTYP TO FATAL ERROR
       HALT ;CC'S NOT SET PROPERLY
            ;OR SEQUENCE ERROR

```

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 DFKAA8.P11 T76 TEST MODE 1 SOP NON-MODIFYING

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2746
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2748
2749 ;*****
2750 ; THIS TEST SETS LOCATION 0 TO 377 AND THEN USES R0 TO TEST
2751 ; THE EVEN BYTE AND THE ODD BYTE USING SOP BYTE INSTRUCTIONS WITH MODE 1.
2752 ; AGAIN, CONDITIONAL BRANCHES ARE USED TO VERIFY THE SETTING OF THE
2753 ; PROPER CONDITION CODE BITS.
2754
2755 ;*****
2756 ; TEST 77 TEST MODE 1 BYTE INST. NON-MODIFYING
2757 ;*****
2758 006026 005212      TST77: INC   (R2)          ;UPDATE TEST NUMBER
2759 006030 022712      CMP   #77 (R2)        ;SEQUENCE ERROR?
2760 006034 001026      BNE   TST100-10     ;BR TO ERROR HALT ON SEQ ERROR
2761 006036 005000      CLR   R0             ;POINT TO LOC 0
2762 006040 005010      CLR   (R0)          ;CLEAR LOC 0
2763 006042 10510       COMB  (R0)          ;COMPLEMENT BYTE 0
2764 006044 000277      SCC   SNMB1A        ;SET CC=0111
2765 006046 000250      CLN   TST8            ;TRY TST ON EVEN BYTE
2766 006050 105710      BVS   SNMB1A        ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
2767 006052 102402      BLOS  SNMB1A        ;CONDITIONAL BRANCH INST. AND
2768 006054 101401      BMI   SNMB1B        ;REPLACE THE MOVE INSTRUCTION
2769 006056 100404      SNMB1B: MOV   #153,-(R2)    <=====
2770                                     INC   -(R2)          <=====
2771                                     HALT           <=====
2772                                     CLR   R0             <=====
2773                                     INC   RO             <=====
2774 006060 012742      SNMB1A: MOV   #153,-(R2)    ;MOVE TO MAILBOX * ***** 153 *****
2775 006064 005242      INC   -(R2)          ;SET MSGTYP TO FATAL ERROR
2776 006066 000000      HALT           ;CC'S NOT CORRECT
2777 006070 005000      SNMB1B: CLR   R0             ;SET CC=1011
2778 006072 005200      INC   RO             ;TRY TO TST AN ODD BYTE
2779 006074 000277      SCC   SNMB1C        ;CHECK CC=0100
2780 006076 000244      CLZ   TST8            ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
2781 006100 105710      BVS   SNMB1C        ;CONDITIONAL BRANCH INST. AND
2782 006102 102403      BCS   SNMB1C        ;REPLACE THE MOVE INSTRUCTION
2783 006104 103402      BMI   SNMB1C        <=====
2784 006106 100401      BEQ   TST100         <=====
2785 006110 001404      SNMB1C: MOV   #154,-(R2)    ;MOVE TO MAILBOX * ***** 154 *****
2786                                     INC   -(R2)          ;SET MSGTYP TO FATAL ERROR
2787                                     HALT           ;CC'S NOT CORRECT
2788                                     BEQ   TST100         ;OR SEQUENCE ERROR
2789                                     SNMB1C: MOV   #154,-(R2)    ;MOVE TO MAILBOX * ***** 154 *****
2790 006112 012742      INC   -(R2)          ;SET MSGTYP TO FATAL ERROR
2791 006112 005242      HALT           ;CC'S NOT CORRECT
2792 006116 000000
2793 006120 000000
2794

```

2795  
 2796 \*\*\*\*\*  
 2797  
 2798 THIS TEST VERIFIES THE SINGLE-OPERAND NON-MODIFYING INSTRUCTIONS  
 2799 USING MODE 2. IT USES THE IDENTICAL PROCEDURE EMPLOYED IN THE  
 2800 MODE 1 TESTS. ADDITIONALLY, THE REGISTER IS CHECKED TO ASSURE THAT  
 2801 IT IS INCREMENTED PROPERLY.  
 2802 \*\*\*\*\*  
 2803 TEST 100 TEST MODE 2 WITH S0P NON-MODIFYING  
 2804 \*\*\*\*\*  
 2805 006122 005212 TST100: INC (R2) ;UPDATE TEST NUMBER  
 2806 006124 022712 000100 CMP #100,(R2) ;SEQUENCE ERROR?  
 2807 006130 001020 BNE TST101-10 ;BR TO ERROR HALT ON SEQ ERROR  
 2808 006132 005000 CLR R0 ;INITIALIZE R0=0  
 2809 006134 005010 CLR (R0) ;CLEAR LOC 0  
 2810 006136 000277 SCC ;SET CC=1011  
 2811 006140 000244 CLZ  
 2812 006142 005720 TST (R0)+ ;TRY TST W/ MODE 2  
 2813 006144 102403 BVS SNM2A ;CHECK CC=0100  
 2814 006146 103402 BCS SNM2A  
 2815 006150 100401 BMI SNM2A  
 2816 006152 001404 BEQ SNM2B  
 2817  
 2818 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 2819 ; CONDITIONAL BRANCH INST. AND <=====  
 2820 ; REPLACE THE MOVE INSTRUCTION <=====  
 2821 ; WHICH FOLLOWS W/ 767 <=====  
 2822 006154 SNM2A:  
 2823 006154 012742 000155 MOV #155,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 155 \*\*\*\*\*  
 2824 006160 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2825 006162 000000 HALT ;CC'S NOT CORRECT  
 2826 006164 005300 SNM2B: DEC R0 ;RESET R0  
 2827 006166 005300 DEC R0  
 2828 006170 001404 BEQ TST101  
 2829  
 2830 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 2831 ; CONDITIONAL BRANCH INST. AND <=====  
 2832 ; REPLACE THE MOVE INSTRUCTION <=====  
 2833 ; WHICH FOLLOWS W/ 760 <=====  
 2834 006172 012742 000156 MOV #156,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 156 \*\*\*\*\*  
 2835 006176 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2836 006200 000000 HALT ;MODE 2 DID NOT INC REQ CORRECTLY  
 ; OR SEQUENCE ERROR

2837  
 2838 ;\*\*\*\*\*  
 2839  
 2840 THIS TEST VERIFIES MODE 2 SINGLE OPERAND NON-MODIFYING BYTE  
 2841 INSTRUCTIONS IT USES R0 TO POINT TO LOC. 0. WITH LOCATION 0  
 2842 SET TO 377, THE EVEN AND ODD BYTE IS TESTED WITH TSTB INSTRUCTIONS  
 2843 TO VERIFY THE CORRECT CC ARE SET. THE REGISTER IS CHECKED FOR  
 2844 PROPER INCREMENTING.  
 2845  
 2846 ;TEST 101 TEST MODE 2 - BYTE W/ SOP NON-MODIFYING  
 2847  
 2848 ;\*\*\*\*\*  
 2849 006202 005212 000101  
 2850 006204 022712 ;TST101: INC (R2) ;UPDATE TEST NUMBER  
 2851 006210 001042 CMP #101,(R2) ;SEQUENCE ERROR?  
 2852 006212 005000 BNE TST102-10 ;BR TO ERROR HALT ON SEQ ERROR  
 2853 006214 005010 CLR RO ;CLEAR R0  
 2854 006216 105110 CLR (R0) ;CLEAR LOC 0  
 2855 006220 000277 COMB (R0) ;SET LOC 0=377  
 2856 006222 000250 SCC SNMB2A ;SET CC=0111  
 2857 006224 105720 CLN TSTB (R0)+ ;TRY TST OF EVEN BYTE  
 2858 006226 102402 BVS SNMB2A  
 2859 006230 101401 BLOS SNMB2A  
 2860 006232 100404 BMI SNMB2B  
 2861 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 2862 ; CONDITIONAL BRANCH INST. AND <=====  
 2863 ; REPLACE THE MOVE INSTRUCTION <=====  
 2864 ; WHICH FOLLOWS W/ 767 <=====  
 2865 006234 012742 000157 SNMB2A:  
 2866 006234 012742 MOV #157,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 157 \*\*\*\*\*  
 2867 006240 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2868 006242 000000 HALT ;CC'S NOT SET CORRECTLY  
 2869 006244 005300 DEC RO ;DECREMENT R0  
 2870 006246 001404 BEQ SNMB2C  
 2871 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 2872 ; CONDITIONAL BRANCH INST. AND <=====  
 2873 ; REPLACE THE MOVE INSTRUCTION <=====  
 2874 ; WHICH FOLLOWS W/ 761 <=====  
 2875 006250 012742 000160 SNMB2C:  
 2876 006254 005242 MOV #160,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 160 \*\*\*\*\*  
 2877 006256 000000 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 2878 006260 005200 HALT ;MODE 2 DID NOT INC REG CORRECTLY  
 2879 006262 000277 INC RO ;POINT TO ODD BYTE  
 2880 006264 000244 SCC SNMB2D ;SET CC=1011  
 2881 006266 105720 CLZ TSTB (R0)+ ;TRY TST OF ODD BYTE  
 2882 006270 102403 BVS SNMB2D ;CHECK CC'S=0100  
 2883 006272 103402 BCS SNMB2D  
 2884 006274 100401 BMI SNMB2D  
 2885 006276 001404 BEQ SNMB2E  
 2886 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 2887 ; CONDITIONAL BRANCH INST. AND <=====  
 2888 ; REPLACE THE MOVE INSTRUCTION <=====  
 2889 ; WHICH FOLLOWS W/ 745 <=====  
 2890 006300 012742 000161 SNMB2D:  
 2891 006300 012742 MOV #161,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 161 \*\*\*\*\*  
 2892 006304 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR

MAINDEC-11-DFKAR-9 !1 34 CPU TEST MACY:1 27(732) 01-OCT-76 15:03 PAGE 293  
DFKAR5.P11 T101 TEST MODE 2 - BYTE W/ S0P NON-MODIFYING

2893 006306 000000  
2894 006310 005300  
2895 006312 005300  
2896 006314 001404  
2897  
2898  
2899  
2900  
2901 006316 C12742 000162  
2902 006322 005242  
2903 006324 000000  
2904

SNMB2E: HALT  
DEC RO  
DEC RO  
BEG TST102

MOV #162 -(R2)  
INC - R21  
HALT

;CC'S NOT CORRECT

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND  
: REPLACE THE MOVE INSTRUCTION  
: WHICH FOLLOWS W/ 736 (zzzz  
: MOVE TO MAILBOX # \*\*\*\*\* 162 \*\*\*\*\*  
: SET MSGTYP TO FATAL ERROR  
: R0 DID NOT INCREMENT PROPERLY  
: OR SEQUENCE ERROR

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 006326 005212  
 006330 022712 000102  
 006334 001022  
 006336 005000  
 006340 005010  
 006342 105100  
 006344 005300  
 006346 000277  
 006350 000244  
 006352 005730  
 006354 102403  
 006356 103402  
 006360 100401  
 006362 001404

 ; TEST 102 TEST MODE 3 W/ S0P NON-MODIFYING INSTS  
 TST102: INC (R2) ; UPDATE TEST NUMBER  
 CMP #102, (R2) ; SEQUENCE ERROR?  
 BNE TST103-10 ; BR TO ERROR HALT ON SEQ ERROR  
 CLR R0 ; R0=0  
 CLR (R0) ; CLEAR LOC 0  
 COMB R0 ; R0=376  
 DEC R0 ;  
 SCC ; SET CC=1011  
 CLZ ;  
 TST J(R0)+ ; TRY TST W/ MODE 3  
 BVS SNM3A ; CHECK CC=0100  
 BCS SNM3A  
 BMI SNM3A  
 BEQ SNM3B ;  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 765

&lt;=====

&lt;=====

&lt;=====

&lt;=====

 006364 012742 000163  
 006364 012742  
 005242  
 000000  
 006372 000000  
 005300  
 105100  
 001404

 SNM3A: MOV #163,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 163 \*\*\*\*\*  
 INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 HALT ; CC'S NOT CORRECT  
 SNM3B: DEC R0 ; R0=377  
 COMB R0 ; R0=0  
 BEQ TST103 ;  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 756

&lt;=====

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&lt;=====

&lt;=====

 MOV #164,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 164 \*\*\*\*\*  
 INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 HALT ; MODE 3 DID NOT INC REG CORRECTLY  
 ; OR SEQUENCE ERROR

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3004

THIS TEST VERIFIES SOP NON-MODIFYING BYTE INSTRUCTIONS MODE 3  
 LOC. 0 IS SET TO 377. TABLE AT LOC. 402-404 IS USED TO TEST  
 BYTE 0 AND BYTE 1. THE REGISTER IS CHECKED FOR PROPER INCREMENTING AND  
 THE CC'S ARE VERIFIED.  
 THE TABLE AT LOC. 402-404 SHOULD CONTAIN 0 AND 1 BEFORE AND  
 AFTER THE TEST IS RUN.

TEST 103 TEST MODE 3 - BYTES W/ SOP NON-MODIFYING INSTS.

TST103:	INC	(R2)	: UPDATE TEST NUMBER
	CMP	#103, (R2)	: SEQUENCE ERROR?
	BNE	TST104-10	: BR TO ERROR HALT ON SEQ ERROR
	CLR	R0	: R0=0
	CLR	(R0)	: CLEAR LOC 0
	COMB	(R0)	: LOC. 0 =377
	COMB	RO	
	INC	RO	
	TST	(R0)+	: R0=402
	SCC		: CC=0111
	CLN		
	TSTB	0(R0)+	: TRY TST OF EVEN BYTE
	BVS	SNMB3A	: CHECK CC=1000
	BLOS	SNMB3A	
	BMI	SNMB3B	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND       <===== REPLACE THE MOVE INSTRUCTION     <===== WHICH FOLLOWS W/ 764             <=====

SNMB3A:	MOV	\$165,-(R2)	: MOVE TO MAILBOX # ***** 165 *****
	INC	-(R2)	: SET MSGTYP TO FATAL ERROR
	HALT		: CC'S NOT CORRECT
SNMB3B:	SCC		: SET CC=1011
	CLZ		
	TSTB	0(R0)+	: TRY TST OF ODD BYTE
	BVS	SNMB3C	: CHECK CC=0100
	BCS	SNMB3C	
	BMI	SNMB3C	
	BEQ	SNMB3D	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND       <===== REPLACE THE MOVE INSTRUCTION     <===== WHICH FOLLOWS W/ 751             <=====

SNMB3C:	MOV	\$166,-(R2)	: MOVE TO MAILBOX # ***** 166 *****
	INC	-(R2)	: SET MSGTYP TO FATAL ERROR
	HALT		: CC'S NOT CORRECT
SNMB3D:	TST	(R0)+	: R0=410
	TST	(R0)	
	BMI	TST104	
			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND       <=====

3005  
 3006  
 3007 006516 012742 000167  
 3008 006522 005242  
 3009 006524 000000  
 3010  
 3011  
 3012  
 3013 THIS TEST VERIFIES MODE 4 SOP NON-MODIFYING INSTRUCTIONS.  
 3014 LOC. 0 IS SET TO -1 AND THE CC'S ARE SET TO THE COMPLEMENT OF THE  
 3015 EXPECTED RESULTS. R0 AND SET TO 2 AND A TST MODE 4 IS EXECUTED.  
 3016 THE CC'S ARE CHECKED WITH CONDITIONAL BRANCH INSTRUCTIONS AND THE REGISTER  
 3017 IS CHECKED FOR PROPER DECREMENTING.  
 3018  
 3019  
 3020 TEST 104 TEST MODE 4 W/ SOP NON-MODIFYING INSTS  
 3021  
 3022 006526 005212 000104  
 3023 006530 022712  
 3024 006534 001017  
 3025 006536 005000  
 3026 006540 005010  
 3027 006542 005120  
 3028 006544 000277  
 3029 006546 000244  
 3030 006550 005740  
 3031 006552 102402  
 3032 006554 101401  
 3033 006556 100404  
 3034  
 3035  
 3036  
 3037  
 3038 006560  
 3039 006560 012742 000170  
 3040 006564 005242  
 3041 006566 000000  
 3042 006570 005700  
 3043 006572 001404  
 3044  
 3045  
 3046  
 3047  
 3048 006574 012742 000171  
 3049 006600 005242  
 3050 006602 000000

SNM4A:  SNM4B:  MOV INC HALT  TST BEQ  MOV INC HALT	#167 -(R2) -(R2) HALT  R0 -(R0)+ SCC CLZ TST BYS BLOS BMI	;REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 742 ;MOVE TO MAILBOX # ***** 167 ***** ;SET MSGTYP TO FATAL ERROR ;TSTB DID NOT INCREMENT R0 CORRECTLY OR SEQUENCE ERROR ;***** ;THIS TEST VERIFIES MODE 4 SOP NON-MODIFYING INSTRUCTIONS. ;LOC. 0 IS SET TO -1 AND THE CC'S ARE SET TO THE COMPLEMENT OF THE ;EXPECTED RESULTS. R0 AND SET TO 2 AND A TST MODE 4 IS EXECUTED. ;THE CC'S ARE CHECKED WITH CONDITIONAL BRANCH INSTRUCTIONS AND THE REGISTER ;IS CHECKED FOR PROPER DECREMENTING. ;***** ;TEST 104 TEST MODE 4 W/ SOP NON-MODIFYING INSTS ;***** ;TST104: INC (R2) ;UPDATE TEST NUMBER ;CMP #104, (R2) ;SEQUENCE ERROR? ;BNE TST105-10 ;BR TO ERROR HALT ON SEQ ERROR ;CLR R0 ;R0=0 ;CLR (R0) ;LOC 0=0 ;COM (R0)+ ;LOC 0=-1 ;SCC ;SET CC=1011 ;CLZ ;TST -(R0) ;TRY TST W/ MODE 4 ;BVS SNM4A ;CHECK CC=0100 ;BLO SNM4A ;BMI SNM4B ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ;CONDITIONAL BRANCH INST. AND ;REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 767 ;***** ;SNM4A: MOV #170, -(R2) ;MOVE TO MAILBOX # ***** 170 ***** ;INC -(R2) ;SET MSGTYP TO FATAL ERROR ;HALT ;CC'S NOT CORRECT ;TST R0 ;BEQ TST105 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ;CONDITIONAL BRANCH INST. AND ;REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 761 ;***** ;SNM4B: MOV #171, -(R2) ;MOVE TO MAILBOX # ***** 171 ***** ;INC -(R2) ;SET MSGTYP TO FATAL ERROR ;HALT ;TST MODE 4 DID NOT DEC R0 CORRECTLY OR SEQUENCE ERROR
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THIS TEST VERIFIES MODE 5 SOP NON-MODIFYING INSTRUCTIONS.  
 IT USES A POINTER AT LOC. 376 TO TEST LOC. D. R0 IS SET  
 TO 400, A TST MODE 5 INSTRUCTION IS EXECUTED AND THE CC'S CHECKED.  
 R0 IS CHECKED TO INSURE PROPER DECREMENTING.

TEST 105 TEST MODE 5 W/ SOP NON-MODIFYING INSTS

TST105:	INC (R2)	; UPDATE TEST NUMBER
	CMP \$105,(R2)	; SEQUENCE ERROR?
	BNE TST106-10	; BR TO ERROR HALT ON SEQ ERROR
	CLR R0	; R0=0
	CLR (R0)	; LOC 0=0
	COM (R0)	; LOC 0=-1
	COMB R0	; R0=377
	INC R0	; R0=400
	SCC	; SET CC=0111
	CLN	
	TST 2-(R0)	; TRY TST W/ MODE 5
	BVS SNM5A	; CHECK CC=1000
	BLOS SNM5A	
	BMI SNM5B	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 765 <=====

SNM5A:	MOV #172,-(R2)	; MOVE TO MAILBOX # ***** 172 *****
	INC -(R2)	; SET MSGTYP TO FATAL ERROR
	HALT	; CC'S NOT SET PROPERLY
SNM5B:	INC R0	; R0=377
	COMB R0	; R0=0
	BEQ TST106	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND  
 REPLACE THE MOVE INSTRUCTION  
 WHICH FOLLOWS W/ 756 <=====

MOV #173,-(R2)	; MOVE TO MAILBOX # ***** 173 *****
INC -(R2)	; SET MSGTYP TO FATAL ERROR
HALT	; MODE 5 DID NOT DEC R0 CORRECTLY ; OR SEQUENCE ERROR

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3099      THIS TEST VERIFIES MODE 6 SOP NON-MODIFYING INSTRUCTIONS.
3100      ;R0 IS SET TO 377 AND A MODE 6 TST INSTRUCTION IS EXECUTED
3101      ;USING R0 AND AN OFFSET OF -377. THE CC'S ARE CHECKED AS WELL
3102      ;AS R0 TO INSURE IT WAS NOT ALTERED.
3103
3104
3105      TEST 106      TEST MODE 6 W/ SOP NON-MODIFYING INSTS
3106
3107 006670 005212      000106      TST106: INC    (R2)      ;UPDATE TEST NUMBER
3108 006672 022712      000106      CMP    *106,(R2)    ;SEQUENCE ERROR?
3109 006676 001021      000106      BNE    TST107-10   ;BR TO ERROR HALT ON SEQ ERROR
3110 006700 005000      000106      CL.R    R0          ;R0=0
3111 006702 005010      000106      C' R   (R0)        ;LOC 0=0
3112 006704 005110      000106      COM    (R0)        ;LOC 0=-1
3113 006706 105100      000106      COMB   R0          ;R0=377
3114 006710 000277      000106      SCC    CLN         ;SET CC=0111
3115 006712 000250      000106      CLN
3116 006714 005760      177401      TST    -377(R0)    ;TRY TST W/ MODE 6
3117 006720 102402      177401      BVS    SNM6A      ;CHECK CC=1000
3118 006722 101401      177401      BLOS   SNM6A
3119 006724 100404      177401      BMI    SNM6B
3120
3121
3122
3123      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
3124 006726 012742      000174      SNM6A: MOV    *174,-(R2)  ;CONDITIONAL BRANCH INST. AND
3125 006726 012742      000174      SNM6A: INC    -(R2)     ;REPLACE THE MOVE INSTRUCTION
3126 006732 005242      000174      SNM6A: HALT   R0          ;WHICH FOLLOWS W/ 765      <=====
3127 006734 000000      000174      SNM6B: COMB   R0          ;
3128 006736 105100      000174      SNM6B: BEQ    TST107   ;
3129 006740 001404      000174      SNM6B: HALT
3130
3131
3132
3133      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
3134 006742 012742      000175      MOV    *175,-(R2)  ;CONDITIONAL BRANCH INST. AND
3135 006746 005242      000175      MOV    *175,-(R2)  ;REPLACE THE MOVE INSTRUCTION
3136 006750 000000      000175      INC    -(R2)     ;WHICH FOLLOWS W/ 757      <=====
3137      ;MOVE TO MAILBOX # ***** 174 *****
3138      ;SET MSGTYP TO FATAL ERROR
3139      ;CC'S INCORRECT
3140      ;R0=0
3141
3142
3143
3144      ;MOVE TO MAILBOX # ***** 175 *****
3145      ;SET MSGTYP TO FATAL ERROR
3146      ;TST MODE 6 INCORRECTLY CHANGED RC
3147      ;OR SEQUENCE ERROR
  
```

MAINDEC-11-DFKAA-8 11:34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 299  
 DFKAA8.P11 T106 TEST MODE 6 W/ SOP NON-MODIFYING INSTS

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3138
3139
3140
3141      THIS TEST VERIFIES MODE 7 SOP NON-MODIFYING INSTRUCTIONS.
3142      IT USES A POINTER TO LOC. 0 STORED AT LOC. 400 TO TST LOC. 0.
3143      R0 IS SET TO 377 AND LOC. 0 IS TESTED THRU THE POINTER AT 400 USING
3144      R0 AND AN OFFSET OF 1.
3145
3146
3147      TEST 107    TEST MODE 7 W/ SOP NON-MODIFYING INSTS.
3148
3149 006752 005212      TST107: INC   (R2)      ;UPDATE TEST NUMBER
3150 006754 022712 000107    CMP   #107,(R2)   ;SEQUENCE ERROR?
3151 006760 001021    BNE   TST110-10  ;BR TO ERROR HALT ON SEQ ERROR
3152 006762 005000    CLR   R0          ;R0=0
3153 006764 005010    CLR   (R0)       ;LOC 0=0
3154 006766 005110    COM   (R0)       ;LOC 0=-1
3155 006770 105100    COMB  R0          ;R0=377
3156 006772 000277    SCC   CC          ;CC=0111
3157 006774 000250    CLN
3158 006776 005770 000001    TST   @1(R0)     ;TRY TST W/ MODE 7
3159 007002 102402    BVS   SNM7A      ;CHECK CC=1000
3160 007004 101401    BLOS  SNM7A
3161 007006 100404    BMI   SNM7B
3162
3163
3164
3165      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
3166 007010 012742 000176      SNM7A: MOV   #176,-(R2)  ;CONDITIONAL BRANCH INST. AND
3167 007010 012742 000176      SNM7A: INC   -(R2)      ;REPLACE THE MOVE INSTRUCTION
3168 007014 005242      SNM7A: HALT
3169 007016 000000      SNM7B: COMB  R0          ;WHICH FOLLOWS W/ 765      <=====
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3170 007020 105100      SNM7B: BEQ   TST110  ;MOVE TO MAILBOX * ***** 176 *****
3171 007022 001404      SNM7B: HALT
3172
3173
3174
3175      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
3176 007024 012742 000177      MOV   #177,-(R2)  ;CONDITIONAL BRANCH INST. AND
3177 007030 005242 000177      MOV   #177,-(R2)  ;REPLACE THE MOVE INSTRUCTION
3178 007032 000000      INC   -(R2)      ;WHICH FOLLOWS W/ 757      <=====
```

```

3179      ;MOVE TO MAILBOX * ***** 177 *****
3179      ;SET MSGTYP TO FATAL ERROR
3179      ;TST MODE 7 INCORRECTLY CHANGED RC
3179      ;OR SEQUENCE ERROR
```

MAINDEC-11-DFKAA-8 11 34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 300  
DFKAA8.P11 T10 TEST MODE ? W/ SOP NON-MODIFYING INSTS.

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3190
3181
3182
3183
3184      THIS TEST VERIFIES MODE 0 DOUBLE OPERAND INSTRUCTIONS. IT SETS
3185      DATA IN R0 AND R4 AND USES THE ADD INSTRUCTION TO TEST THE DOP
3186      MICROCODE.
3187
3188      TEST 110 TEST MODE 0 DOUBLE-OPERAND (DOP) INSTS.
3189
3190 007034 005212          tST110: INC   (R2)      ;UPDATE TEST NUMBER
3191 007036 022712 000110    CMP   #110,(R2)   ;SEQUENCE ERROR?
3192 007042 001006            BNE   TST111-10  ;BR TO ERROR HALT ON SEQ ERROR
3193 007044 005C00            CLR   R0           ;R0=0
3194 007046 005100            COM   R0           ;R0=-1
3195 007050 005004            CLR   R4           ;R4=0
3196 007052 060004            ADD   R0,R4       ;TRY ADD: R4=-1
3197 007054 005204            INC   R4           ;R4=0
3198 007056 001404            BEQ   TST111     ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
3199
3200
3201
3202
3203 007060 012742 000200    MOV   #200,-(R2)  ;MOVE TO MAILBOX * ***** 200 *****
3204 007064 005242            INC   -(R2)       ;SET MSGTYP TO FATAL ERROR
3205 007066 000700            HALT             ;ADD INST. FAILED W/ MODE 0
3206
3207
3208
3209
3210      THIS TEST VERIFIES THE MOVE INSTRUCTION WITH MODE 0 TO MODE 0.
3211      THIS TEST IS NECESSARY BECAUSE THIS PARTICULAR INSTRUCTION UTILIZES UNIQUE
3212      MICROCODE.
3213
3214
3215      TEST 111 MOV MODE 0 TO MODE 0
3216
3217 007070 005212          tST111: INC   (R2)      ;UPDATE TEST NUMBER
3218 007072 022712 000111    CMP   #111,(R2)   ;SEQUENCE ERROR?
3219 007076 001006            BNE   TST112-10  ;BR TO ERROR HALT ON SEQ ERROR
3220 007100 005000            CLR   R0           ;R0=0
3221 007102 005004            CLR   R4           ;R4=0
3222 007104 005100            COM   R0           ;R0=-1
3223 007106 010004            MOV   R0,R4       ;TRY MOVE -1 TO R4
3224 007110 005204            INC   R4           ;INC R4
3225 007112 001404            BEQ   TST112     ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
3226
3227
3228
3229
3230 007114 012742 000201    MOV   #201,-(R2)  ;MOVE TO MAILBOX * ***** 201 *****
3231 007120 005242            INC   -(R2)       ;SET MSGTYP TO FATAL ERROR
3232 007122 000000            HALT             ;MOVE FAILED MODE 0 TO MODE 0
3233
3234
3235

```

J06

THIS TEST VERIFIES THE SUBTRACT INSTRUCTION WITH MODE 0,0.  
 THIS TEST IS NECESSARY BECAUSE THIS PARTICULAR INSTRUCTION UTILIZES SOME  
 UNIQUE MICROCODE.

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TEST 112 TEST SUB MODE 0,0

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007124	005212		TST112: INC (R2)	UPDATE TEST NUMBER	<=====
007126	022712	000112	CMP #112 (R2)	SEQUENCE ERROR?	<=====
007132	001016		BNE TST113-10	BR TO ERROR HALT ON SEQ ERROR	<=====
007134	005000		CLR R0	R0=0	<=====
007136	005004		CLR R4	R4=0	<=====
007140	005204		INC R4	R4=1	<=====
007142	160400		SUB R4, R0	TRY SUB 0,0 R0=-1	<=====
007144	100003		BPL SUBO	CC=1001	<=====
007146	001402		BEQ SUBO		<=====
007150	102401		BVS SUBO		<=====
007152	103404		BCS SUBOA		<=====
007154	012742	000202	SUBO:	TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 770	<=====
007160	005242		MOV #202, -(R2)		<=====
007162	000000		INC -(R2)		<=====
007164	005200		HALT		<=====
007166	001404		SUBOA: INC RO	MOVE TO MAILBOX # ***** 202 ***** SET MSGTYP TO FATAL ERROR CONDITION CODE FAILED ON SUB	<=====
007170	012742	000203	BEQ TST113		<=====
007174	005242		MOV #203, -(R2)	TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 762	<=====
007176	000000		INC -(R2)	MOVE TO MAILBOX # ***** 203 ***** SET MSGTYP TO FATAL ERROR DATA RESULT OF SUB FAILED OR SEQUENCE ERROR	<=====

3273  
 3274 ;\*\*\*\*\*  
 3275  
 3276 THIS TEST QUICKLY VERIFIES THE REMAINING DOP MODIFYING INSTRUCTIONS  
 3277 WITH MODE 0,0 TO PROVIDE A BASELINE FOR SUBSEQUENT TESTS.  
 3278 SINGLE OPERAND INSTRUCTIONS ARE USED TO SET UP DATA IN R0 AND R4  
 3279 BEFORE EACH OF THE SEVERAL DOP MODIFYING INSTRUCTIONS ARE USED AND  
 3280 VERIFIED.  
 3281  
 3282 ;\*\*\*\*\*  
 3283 TEST 113 TEST ALL THE DOP INSTRUCTIONS W/ SOURCE MODE 0,0  
 3284 ;\*\*\*\*\*  
 3285 007200 005212 000113  
 3286 007202 022712 TST113:  
 3287 007206 001051 INC (R2) ;UPDATE TEST NUMBER  
 3288 007210 005000 CMP #113,(R2) ;SEQUENCE ERROR?  
 3289 007212 010004 BNE TST114-10 ;BR TO ERROR HALT ON SEQ ERROR  
 3290 007214 001404 CLR R0 ;R0=0  
 3291 ;TRY MOVE MODE 0,0  
 3292 BEQ DOP0A ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===== .  
 3293 ;CONDITIONAL BRANCH INST. AND <===== .  
 3294 ;REPLACE THE MOVE INSTRUCTION <===== .  
 3295 ;WHICH FOLLOWS W/ 775 <===== .  
 3296 007216 012742 000204  
 3297 007222 005242 MOV #204,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 204 \*\*\*\*\*  
 3298 007224 000000 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 3299 007226 005200 HALT ;Z-BIT NOT SET  
 3300 007230 005100 INC R0 ;R0=1  
 3301 007232 005104 COM R0 ;R0=177776  
 3302 007234 040004 COM R4 ;R4=177777  
 3303 007236 005304 BIC R0,R4 ;TRY BIC: R4=1  
 3304 007240 001404 DEC R4 ;R4=0  
 3305 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===== .  
 3306 ;CONDITIONAL BRANCH INST. AND <===== .  
 3307 ;REPLACE THE MOVE INSTRUCTION <===== .  
 3308 ;WHICH FOLLOWS W/ 763 <===== .  
 3309 007242 012742 000205  
 3310 007246 005242 MOV #205,-(R2) ;MOVE TO MAILBX # \*\*\*\*\* 205 \*\*\*\*\*  
 3311 007250 000000 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 3312 007252 050004 HALT ;BIC CLEAR RESULT INCORRECT  
 3313 007254 005204 BIS R0,R4 ;TRY BIS: R4=177777  
 3314 007256 005204 INC R4 ;R4=0  
 3315 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <===== .  
 3316 ;CONDITIONAL BRANCH INST. AND <===== .  
 3317 ;REPLACE THE MOVE INSTRUCTION <===== .  
 3318 ;WHICH FOLLOWS W/ 753 <===== .  
 3319 007262 012742 000206  
 3320 007266 005242 MOV #206,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 206 \*\*\*\*\*  
 3321 007270 000000 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 3322 007272 005000 HALT ;RESULT OF BIS INCORRECT  
 3323 007274 105100 CLR R0 ;R0=0  
 3324 007276 005004 COMB R0 ;R0=377  
 3325 007300 005104 CLR R4 ;R4=0  
 3326 007302 040004 COM R4 ;R4=177777  
 3327 007304 060004 BIC R0,R4 ;R4=177400  
 3328 007306 005204 ADD R0,R4 ;TRY ADD: R4=177777  
 3329 ;R4=0

L06

MAINDEC-11-DFKAA-8 11/34 CPJ TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 303  
DFKAA8.P11 T113 TEST ALL THE DOP INSTRUCTIONS W/ SOURCE MODE 0,0

3329	007310	001404		BEQ	DOPOD		
3330						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
3331						CONDITIONAL BRANCH INST. AND	<=====
3332						REPLACE THE MOVE INSTRUCTION	<=====
3333						WHICH FOLLOWS W/ 737	<=====
3334	007312	012742	000207		MOV	#207 -(R2)	
3335	007316	005242			INC	-(R2)	MOVE TO MAILBOX # ***** 207 *****
3336	007320	000000			HALT		SET MSGTYP TO FATAL ERROR
3337	007322	160004		DOPOD:	SUB	R0, R4	RESULT OF ADD INCORRECT
3338	007324	105404			NEGB	R4	177401=R4
3339	007326	005204			INC	R4	R4=177777
3340	007330	001404			BEQ	TST114	RD=0
3341							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
3342							CONDITIONAL BRANCH INST. AND
3343							REPLACE THE MOVE INSTRUCTION
3344							WHICH FOLLOWS W/ 727
3345	007332	012742	000210		MOV	#210 -(R2)	
3346	007336	005242			INC	-(R2)	MOVE TO MAILBOX # ***** 210 *****
3347	007340	000000			HALT		SET MSGTYP TO FATAL ERROR
3348							RESULT OF SUB INCORRECT
3349							OR SEQUENCE ERROR

MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 304  
DFKAAB.P11 T113 TEST ALL THE DOP INSTRUCTIONS W/ SOURCE MODE 0,0

-MOS

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3389
      **** THIS TEST VERIFIES MODE 0,X DOUBLE OPERAND INSTRUCTIONS. IT SETS
      DATA IN R0 AND LOCATION 0 AND OPERATES UPON IT USING DOP INSTRUCTIONS.

      **** TEST 114 TEST MODE 0,X DOUBLE-OPERAND INSTRUCTIONS
      ****

TST114: INC    (R2)          ; UPDATE TEST NUMBER
        CMP    #114, (R2)       ; SEQUENCE ERROR?
        BNE    TST115-10        ; BR TO ERROR HALT ON SEQ ERROR
        CLR    R0                ; R0=0
        CLR    (R0)              ; LOC. 0=0
        COMB   (R0)              ; LOC. 0=377
        INC    (R0)+             ; LOC. 0=400   R0=2
        NEG    R0                ; R0=-2
        ADD    R0, #0             ; TRY ADD 0,3; LOC. 0=376
        BMI    DOP03A            ; CC=0001?
        BEQ    DOP03A
        BVS    DOP03A
        BCS    DOP03B

        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
        ; CONDITIONAL BRANCH INST. AND                 <=====
        ; REPLACE THE MOVE INSTRUCTION                <=====
        ; WHICH FOLLOWS W/ 765                         <=====

DOP03A: MOV    #211, -(R2)     ; MOVE TO MAILBOX # ***** 211 *****
        INC    -(R2)              ; SET MSGTYP TO FATAL ERROR
        HALT
        DOP03B: COMB   #0           ; CC'S NOT SET CORRECTLY
        DEC    #0                  ; LOC. 0=1
        BEQ    TST115              ; LOC. 0=0

        ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
        ; CONDITIONAL BRANCH INST. AND                 <=====
        ; REPLACE THE MOVE INSTRUCTION                <=====
        ; WHICH FOLLOWS W/ 754                         <=====

MOV    #212, -(R2)     ; MOVE TO MAILBOX # ***** 212 *****
INC    -(R2)              ; SET MSGTYP TO FATAL ERROR
HALT

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3390 ;\*\*\*\*\*  
 3391  
 3392 THIS TEST VERIFIES MODE O,O DOP NON-MODIFYING INSTRUCTIONS.  
 3393 ;R0 AND R4 ARE PRESET TO 0 AND 1 RESPECTIVELY. COMPARE INSTRUCTIONS ARE  
 3394 ;THEN EXECUTED AND CHECKED. FIRST R4 IS COMPARED TO R0 THEN R0 TO R4.  
 3395  
 3396 ;TEST 115 TEST DOP NON-MODIFYING INST. W/ SOURCE MODE O,O  
 3397  
 3398 ;TST115: INC (R2) ;UPDATE TEST NUMBER  
 3399 007432 005212 000115 ;CMP #115,(R2) ;SEQUENCE ERROR?  
 3400 007434 022712 ;BNE TST116-10 ;BR TO ERROR HALT ON SEQ ERROR.  
 3401 007440 001042 ;CLR R0 ;R0=0  
 3402 007442 005000 ;CLR R4 ;R4=0  
 3403 007444 005004 ;INC R4 ;R4=1  
 3404 007446 005204 ;CMP R4,R0 ;TRY COMPARE R4 TO R0  
 3405 007450 020400 ;BGT DNM1  
 3406 007452 003004  
 3407 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 3408 ; CONDITIONAL BRANCH INST. AND <=====  
 3409 ; REPLACE THE MOVE INSTRUCTION <=====  
 3410 ; WHICH FOLLOWS W/ 773 <=====  
 3411 007454 012742 000213 ;MOV #213,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 213 \*\*\*\*\*  
 3412 007460 005242 ;INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 3413 007462 000000 ;HALT ;CC'S NOT CORRECT FOR CMP  
 3414 007464 020004 ;CMP R0,R4 ;TRY COMPARE R0 TO R4  
 3415 007466 002404 ;BLT DNM2  
 3416 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 3417 ; CONDITIONAL BRANCH INST. AND <=====  
 3418 ; REPLACE THE MOVE INSTRUCTION <=====  
 3419 ; WHICH FOLLOWS W/ 765 <=====  
 3420 007470 012742 000214 ;MOV #214,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 214 \*\*\*\*\*  
 3421 007474 005242 ;INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 3422 007476 000000 ;HALT ;CC'S NOT CORRECT FOR CMP  
 3423 007500 005200 ;INC R0 ;R0=1  
 3424 007502 020400 ;CMP R4,R0 ;TRY COMPARE R4=1 TO R0=1  
 3425 007504 001404 ;BEQ DNM3  
 3426 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 3427 ; CONDITIONAL BRANCH INST. AND <=====  
 3428 ; REPLACE THE MOVE INSTRUCTION <=====  
 3429 ; WHICH FOLLOWS W/ 756 <=====  
 3430 007506 012742 000215 ;MOV #215,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 215 \*\*\*\*\*  
 3431 007512 005242 ;INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 3432 007514 000000 ;HALT ;CC'S NOT CORRECT (Z=1) FOR CMP  
 3433 007516 005000 ;CLR R0 ;R0=0  
 3434 007520 005100 ;COM R0 ;R0=177777  
 3435 007522 005004 ;CLR R4 ;R4=0  
 3436 007524 030004 ;BIT R0,R4 ;TRY BIT R0 TO R4  
 3437 007526 001404 ;BEQ DNM4  
 3438 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 3439 ; CONDITIONAL BRANCH INST. AND <=====  
 3440 ; REPLACE THE MOVE INSTRUCTION <=====  
 3441 ; WHICH FOLLOWS W/ 745 <=====  
 3442 007530 012742 000216 ;MOV #216,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 216 \*\*\*\*\*  
 3443 007534 005242 ;INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 3444 007536 000000 ;HALT ;CC'S NOT CORRECT FOR BIT  
 3445 007540 005304 ;DEC R4 ;R4=177777

MAINDEC-11-DFKAR-B 11 34 CPU TEST MACY:1 27(732) 01-OCT-76 15:03 PAGE 306  
DFKAR-B.P11 T115 TEST DOP NON-MODIFYING INST. W/ SOURCE MODE 0,0

3446 007542 030004	BIT BMI	R0 R4 TST116	; TRY BIT AGAIN	
3447 007544 100404			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 736	<=====
3448				<=====
3449				<=====
3450				<=====
3451				<=====
3452 007546 012742 000217	MOV INC HALT	\$217 -(R2)	; MOVE TO MAILBOX # ***** 217 ***** ; SET MSGTYP TO FATAL ERROR ; CC'S NOT CORRECT FOR BIT ; OR SEQUENCE ERROR	
3453 007552 005242				
3454 007554 000000				
3455				
3456				
3457				
3458				
3459				
3460				
3461				
3462				
3463				
3464 007556 005212	TST116: INC CMP BNE CLR CLR COM INC CMP BMI BEQ BVS BCS	(R2) \$116, (R2) TST117-10 R0 (R0) (R0) R0 R0, 2#0 DNM03A DNMC3A DNM03A DNM03B	; UPDATE TEST NUMBER ; SEQUENCE ERROR? ; BR TO ERROR HALT ON SEQ ERROR ; R0=0 ; LOC. 0=0 ; LOC. 0=177777 ; R0=1 ; TRY CMP MODE 0,3 ; CC=0001	
3465 007560 022712				
3466 007564 001022				
3467 007566 005000				
3468 007570 005010				
3469 007572 005110				
3470 007574 005200				
3471 007576 020037	000000			
3472 007602 100403				
3473 007604 001402				
3474 007606 102401				
3475 007610 103404				
3476				
3477				
3478				
3479				
3480 007612	DNM03A:			
3481 007612 012742 000220	MOV INC HALT	\$220, -(R2) -(R2)	; MOVE TO MAILBOX # ***** 220 ***** ; SET MSGTYP TO FATAL ERROR ; CC'S NOT SET CORRECTLY	
3482 007616 005242				
3483 007620 000000				
3484 007622 005300	DNM03B: DEC BNE INC BEQ	R0 DNM03C (R0) TST117		
3485 007624 001002				
3486 007626 005210				
3487 007630 001104				
3488				
3489				
3490				
3491				
3492 007632	DNM03C:			
3493 007632 012742 000221	MOV INC HALT	\$221, -(R2) -(R2)	; MOVE TO MAILBOX # ***** 221 ***** ; SET MSGTYP TO FATAL ERROR ; DATA INCORRECTLY MODIFIED BY CMP ; OR SEQUENCE ERROR	
3494 007636 005242				
3495 007640 000000				
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THIS TEST VERIFIES MODE 1 DOP INSTRUCTIONS. R0 IS SET TO -1 AND LOC 0 TO 1. R4 IS THEN CLEARED AND USED TO POINT TO LOC 0. IN THE ADD MODE 1 INSTRUCTION, LOC 0 IS ADDED TO R0 AND THE RESULTS VERIFIED.

TEST 117 TEST MODE 1 W/ DOP INST.

TST117: INC	(R2)	; UPDATE TEST NUMBER
CMP	\$117 (R2)	; SEQUENCE ERROR?
BNE	TST120-10	; BR TO ERROR HALT ON SEQ ERROR
CLR	R0	; R0=0
COM	R0	; R0=177777
CLR	R4	; R4=0
CLR	(R4)	; LOC 0=0
INC	(R4)	; LOC 0=1
ADD	(R4), R0	; TRY ADD SOURCE MODE 1
BEQ	TST120	
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS		
; CONDITIONAL BRANCH INST. AND <=====		
; REPLACE THE MOVE INSTRUCTION <=====		
; WHICH FOLLOWS W/ 771 <=====		
MOV	*222,-(R2)	; MOVE TO MAILBOX * ***** 222 *****
INC	-(R2)	; SET MSGTYP TO FATAL ERROR
HALT		; RESULT OF ADD INCORRECT
		; OR SEQUENCE ERROR

 007642 005212  
 007644 022712 000117

 007650 001007  
 007652 005000

 007654 005100  
 007656 005004

 007660 005014  
 007662 005214

 007664 061400  
 007666 001404

 007670 012742 000222  
 007674 005242  
 007676 000000

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 3526  
 3527  
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 3530  
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 3532  
 3533  
 3534  
 3535 007700 005212  
 3536 007702 022712 000120  
 3537 007706 001007  
 3538 007710 005000  
 3539 007712 005010  
 3540 007714 005110  
 3541 007716 005004  
 3542 007720 151004  
 3543 007722 105104  
 3544 007724 001404  
 3545  
 3546  
 3547  
 3548  
 3549 007726 012742 000223  
 3550 007732 005242  
 3551 007734 000000

\*\*\*\*\*  
 THIS TEST VERIFIES MODE 1 DOP BYTE INSTRUCTIONS WHICH ADDRESS  
 EVEN BYTES. LOC. 0 IS SET TO -1 AND R4 IS CLEARED. THEN R4 IS  
 SET TO -1 USING A BISB THRU R0 WITH MODE 1.

\*\*\*\*\*  
 TEST 120 TEST MODE 1 - EVEN BYTE W/ DOP INSTS.

\*\*\*\*\*  
 TST120: INC (R2) ;UPDATE TEST NUMBER  
 CMP #120, (R2) ;SEQUENCE ERROR?  
 BNE TST121-10 ;BR TO ERROR HALT ON SEQ ERROR  
 CLR R0 ;R0=0  
 CLR (R0) ;LOC. 0=0  
 COM (R0) ;LOC. 0=177777  
 CLR R4 ;R4=0  
 BISB (R0), R4 ;TRY MODE 1- EVEN BYTE W/ DOP  
 COMB R4 ;R4=0  
 BEQ TST121

TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 CONDITIONAL BRANCH INST. AND <=====  
 REPLACE THE MOVE INSTRUCTION <=====  
 WHICH FOLLOWS W/ 771 <=====  
 MOVE TO MAILBOX \* \*\*\*\*\* 223 \*\*\*\*\*  
 SET MSGTYP TO FATAL ERROR  
 RESULT OF BISB IS INCORRECT  
 OR SEQUENCE ERROR

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DFKAA8.P11 T120 TEST MODE 1 - EVEN BYTE W/ DOP INSTS.

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THIS TEST VERIFIES MODE 1 DOP NON-MODIFYING INSTRUCTIONS WHICH ADDRESS EVEN BYTES. LOC. 0 IS SET TO -1 AND R0 IS CLEARED AND USED AS THE ADDRESSING REGISTER. R4 IS SET TO 377 AND A MODE 1,0 CMPB INSTRUCTION IS USED THE RESULTS VERIFIED.

TEST 121 TEST MODE 1 - EVEN BYTE W/ DOP NON-MODIFYING INST.

TST121: INC	(R2)	UPDATE TEST NUMBER
CMP	\$121, (R2)	SEQUENCE ERROR?
BNE	TST122-10	BR TO ERROR HALT ON SEQ ERROR
CLR	R0	R0=0
CLR	(R0)	LOC 0=0
COM	(R0)	LOC 0=177777
CLR	R4	R4=0
COMB	R4	R4=377
CMPB	(R0), R4	TRY MODE 1 - EVEN BYTE W/ DOP NON-MODIFYING
BEQ	TST122	
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====		
; CONDITIONAL BRANCH INST. AND <=====		
; REPLACE THE MOVE INSTRUCTION <=====		
; WHICH FOLLOWS W/ 771 <=====		
MOV	\$224, -(R2)	MOVE TO MAILBOX # ***** 224 *****
INC	-(R2)	SET MSGTYP TO FATAL ERROR
HALT		RESULT OF CMPB INCORRECT
		OR SEQUENCE ERROR

007736 005212  
007740 022712 000121  
007744 001C07  
007746 005000  
007750 005010  
007752 005110  
007754 005004  
007756 105104  
007760 121004  
007762 001404

007764 012742 000224  
007770 005242  
007772 000000

F  
P  
J  
L

MAINDEC-11-DFKAA-B 11 34 CPU TEST MACYII 27(732) 01-OCT-76 15:03 PAGE 310  
DFKAAB.P11 T121 TEST MODE 1 - EVEN BYTE W/ DOP NON-MODIFYING INST.

```

3592
3593 ;*****
3594
3595 ; THIS TEST VERIFIES MODE 1,0 MOVB INSTRUCTIONS
3596 ; WHICH ADDRESS EVEN BYTES. LOC. 0 IS SET TO 177400, R0 IS CLEARED AND
3597 ; R4 IS SET TO -1. MOVB ARE USED TO MOVE BYTE 0 TO R4. THIS
3598 ; VERIFIES THAT THE PROPER BYTE WAS SELECTED AND THAT THE SIGN-X-TEND
3599 ; FUNCTION WITH MODE 0.
3600 ; THEN LOC. 0 IS COMPLEMENTED AND THE SAME PROCEDURE EXERCISES
3601 ; THE LOGIC FOR COMPLEMENTARY DATA.
3602 ; THIS TEST EXERCISES UNIQUE MICROCODE.
3603
3604 ;*****
3605 ;TEST 122 TEST MOV INSTRUCTION MODE 1,0 EVEN BYTE
3606 ;*****
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3625
3626
      007774 005212    000122
      007776 022712
      010002 001020
      C10004 005000
      010006 005010
      010010 105110
      010012 005110
      010014 005004
      01C016 005104
      010020 111004
      010022 005704
      010024 001404
      010026 012742    000225
      010032 005242
      010034 000000
      010036 005110
      010040 111004
      010042 100404
      010044 012742    000226
      010050 005242
      010052 000000
      010054 000000
      010056 000000
      010058 000000
      010060 000000
      010062 000000
      010064 000000
      010066 000000
      010068 000000
      010070 000000
      010072 000000
      010074 000000
      010076 000000
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      010090 000000
      010092 000000
      010094 000000
      010096 000000
      010098 000000
      010100 000000
      010102 000000
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      010108 000000
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      010120 000000
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      010124 000000
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      010136 000000
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      010144 000000
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      010148 000000
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      010196 000000
      010198 000000
      010200 000000
      010202 000000
      010204 000000
      010206 000000
      010208 000000
      010210 000000
      010212 000000
      010214 000000
      010216 000000
      010218 000000
      010220 000000
      010222 000000
      010224 000000
      010226 000000
      010228 000000
      010230 000000
      010232 000000
      010234 000000
      010236 000000
      010238 000000
      010240 000000
      010242 000000
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      010250 000000
      010252 000000
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      010256 000000
      010258 000000
      010260 000000
      010262 000000
      010264 000000
      010266 000000
      010268 000000
      010270 000000
      010272 000000
      010274 000000
      010276 000000
      010278 000000
      010280 000000
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      010294 000000
      010296 000000
      010298 000000
      010300 000000
      010302 000000
      010304 000000
      010306 000000
      010308 000000
      010310 000000
      010312 000000
      010314 000000
      010316 000000
      010318 000000
      010320 000000
      010322 000000
      010324 000000
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      010328 000000
      010330 000000
      010332 000000
      010334 000000
      010336 000000
      010338 000000
      010340 000000
      010342 000000
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      010350 000000
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      010358 000000
      010360 000000
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      010364 000000
      010366 000000
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      010378 000000
      010380 000000
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      010398 000000
      010400 000000
      010402 000000
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      010410 000000
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      010500 000000
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      010506 000000
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      010674 000000
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      010680 000000
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      010686 000000
      010688 000000
      010690 000000
      010692 000000
      010694 000000
      010696 000000
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      010706 000000
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      010808 000000
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      010890 000000
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      010894 000000
      010896 000000
      010898 000000
      010900 000000
      010902 000000
      010904 000000
      010906 000000
      010908 000000
      010910 000000
      010912 000000
      010914 000
```

3627  
 3628 :\*\*\*\*\*  
 3629 :  
 3630 : THIS TEST VERIFIES MODE 1 DOP INSTRUCTIONS WHICH REFERENCE  
 3631 : ODD BYTES. LOC. 0 IS SET TO 177400. R0 IS SET TO 0 AND R4 IS  
 3632 : SET TO 1. THE BISB INSTRUCTION USES THE DATA IN BYTE 1 TO SET BYTE 0.  
 3633 : THE RESULT IS CHECKED BY INCREMENTING THE WORD (LOC. 0) TO ZERO.  
 3634  
 3635 :\*\*\*\*\*  
 3636 :TEST 123 TEST MODE 1-ODD BYTE W/ DOP INSTS.  
 3637 :\*\*\*\*\*  
 3638 010054 005212 000123  
 3639 010056 022712 TST123:  
 3640 010062 001010 INC (R2) ;UPDATE TEST NUMBER  
 3641 010064 005000 CMP #123,(R2) ;SEQUENCE ERROR?  
 3642 010066 005010 BNE TST124-10 ;BR TO ERROR HALT ON SEQ ERROR  
 3643 010070 005004 CLR R0 ;R0=0  
 3644 010072 005204 CLR R4 ;R4=0  
 3645 010074 105114 INC R4 ;R4=1  
 3646 010076 151410 COMB (R4) ;LOC. 0=177400  
 3647 010100 005210 BISB (R4),(R0) ;TRY TO BIS LOW ORDER BITS W/ MODE 1  
 3648 010102 001404 INC (R0) ;CHECK RESULT  
 3649 BEQ TST124 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 3650 ;CONDITIONAL BRANCH INST. AND  
 3651 ;REPLACE THE MOVE INSTRUCTION  
 3652 ;WHICH FOLLOWS W/ 770 <=====  
 3653 010104 012742 000227 MOV #227,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 227 \*\*\*\*\*  
 3654 010110 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 3655 010112 000000 HALT ;RESULT OF BISB INCORRECT  
 3656 ; OR SEQUENCE ERROR

H07

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DFKAA8.P11 T123 TEST MODE 1-ODD BYTE W/ DOP INSTS.

```

3657
3658
3659
3660 THIS TEST VERIFIES MODE 2 DOP INSTRUCTIONS. LOC. R IS SET TO -1.
3661 RO IS CLEARED AND USED AS THE MODE 2 ADDRESSING REGISTER TO MOVE LOC. 0
3662 TO R7. THE DATA RESULTS ARE VERIFIED AND THE INCREMENTING OF THE REGISTER
3663 IS CHECKED.
3664
3665
3666 TEST 124 TEST MODE 2 W/ DOP INSTS.
3667
3668 010114 005212
3669 010116 022712 000124
3670 010122 001015
3671 010124 005000
3672 010126 005010
3673 010130 005110
3674 010132 012004
3675 010134 005204
3676 010136 001404
3677
3678
3679
3680
3681 010140 012742 000230
3682 010144 005242
3683 010146 000000
3684 010150 005300
3685 010152 005300
3686 010154 001404
3687
3688
3689
3690
3691 010156 012742 000231
3692 010162 005242
3693 010164 000000
3694

***** THIS TEST VERIFIES MODE 2 DOP INSTRUCTIONS. LOC. R IS SET TO -1.
RO IS CLEARED AND USED AS THE MODE 2 ADDRESSING REGISTER TO MOVE LOC. 0
TO R7. THE DATA RESULTS ARE VERIFIED AND THE INCREMENTING OF THE REGISTER
IS CHECKED.

***** TEST 124 TEST MODE 2 W/ DOP INSTS.

TST124: INC (R2) ;UPDATE TEST NUMBER
        CMP #124, (R2) ;SEQUENCE ERROR?
        BNE TST125-10 ;BR TO ERROR HALT ON SEQ ERROR
        CLR RO ;RO=0
        CLR (RO) ;LOC. 0=0
        COM (RO) ;LOC. 0=177777
        MOV (RO)+, R4 ;TRY MOVE MODE 2,0
        INC R4 ;CHECK R4
        BEQ DOP2 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                  ;CONDITIONAL BRANCH INST. AND <=====
                  ;REPLACE THE MOVE INSTRUCTION <=====
                  ;WHICH FOLLOWS W/ 772 <=====
                  ;MOVE TO MAILBOX * ***** 230 *****
        MOV #230, -(R2) ;SET MSGTYP TO FATAL ERROR
        INC -(R2) ;RESULT OF MOV INST INCORRECT
        HALT ;TEST RO AFTER MODE 2
DOP2:   DEC RO ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
        DEC RO ;CONDITIONAL BRANCH INST. AND <=====
        BEQ TST125 ;REPLACE THE MOVE INSTRUCTION <=====
                  ;WHICH FOLLOWS W/ 763 <=====
                  ;MOVE TO MAILBOX * ***** 231 *****
        MOV #231, -(R2) ;SET MSGTYP TO FATAL ERROR
        INC -(R2) ;REGISTER NOT INCREMENTED IN MODE 2
        HALT ;OR SEQUENCE ERROR

```

MAINDEC-11-DFKAA-B 11-34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 313  
DFKAAB.P11 T124 TEST MODE 2 W/ DOP INSTS.

```

3695
3696
3697
3698      THIS TEST VERIFIES MODE 2 DOP BYTE INSTRUCTIONS WHICH ADDRESS
3699      :EVEN BYTES. LOC. 0 IS SET TO -1. R0 IS CLEARED AND USED AS THE
3700      :ADDRESSING REGISTER IN A TEST WHICH TRIES TO CLEAR BYTE 1 USING
3701      :BYTE 0 DATA AND A BICB. UNIQUE IN THIS TEST IS USE OF THE
3702      :SAME ADDRESSING REGISTER FOR BOTH SOURCE AND DESTINATION. THE SOURCE AND
3703      :DESTINATION IS CHECKED TO INSURE PROPER FUNCTIONING.
3704
3705
3706      TEST 125      TEST MODE 2 - EVEN BYTE W/ DOP INST.
3707
3708 010166 005212
3709 010170 022712 000125
3710 010174 001016
3711 010176 005000
3712 010200 010010
3713 010202 005110
3714 010204 142010
3715 010206 105737 000001
3716 010212 001404
3717
3718
3719
3720      TST125: INC      (R2)          ;UPDATE TEST NUMBER
3721      CMP      #125, (R2)        ;SEQUENCE ERROR?
3722      BNE      TST126-10       ;BR TO ERROR HALT ON SEQ ERROR
3723      CLR      R0             ;R0=0
3724      MOV      R0, (R0)         ;LOC. 0=0
3725      COM      (R0)           ;LOC. 0=177777
3726      BICB     (R0)+, (R0)       ;TRY TO CLEAR BYTE 1 FROM BYTE 0 W/ BICB
3727      TSTB     J#1             ;CHECK RESULT
3728      BEQ      DOPB2A
3729
3730      : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
3731      : CONDITIONAL BRANCH INST. AND      <=====
3732      : REPLACE THE MOVE INSTRUCTION      <=====
3733      : WHICH FOLLOWS W/ 771      <=====

3734 010214 012742 000232
3735 010220 005242
3736 010222 000000
3737 010224 105137 000000
3738 010230 001404
3739
3740      DOPB2A: MOV      #232, -(R2)      ;MOVE TO MAILBOX * ***** 232 *****
3741      INC      -(R2)           ;SET MSGTYP TO FATAL ERROR
3742      HALT
3743
3744      BEQ      TST126       ;BICB DESTINATION INCORRECT
3745      COMB
3746      TST126       ;CHECK BICB SOURCE
3747
3748      : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
3749      : CONDITIONAL BRANCH INST. AND      <=====
3750      : REPLACE THE MOVE INSTRUCTION      <=====
3751      : WHICH FOLLOWS W/ 762      <=====

3752 010232 012742 000233
3753 010236 005242
3754 010240 000000
3755
3756      MOV      #233, -(R2)      ;MOVE TO MAILBOX * ***** 233 *****
3757      INC      -(R2)           ;SET MSGTYP TO FATAL ERROR
3758      HALT
3759
3760      : BICB SOURCE INCORRECTLY CHANGED      <=====
3761      : OR SEQUENCE ERROR      <=====


```

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 314  
DFKAAB.P11 T125 TEST MODE 2 - EVEN BYTE W/ DOP INST.

```

3734 ****
3735 ****
3736 THIS TEST VERIFIES MODE 2 DOP BYTE INSTRUCTIONS WHICH REFERENCE
3737 ODD BYTES. R0 IS SET TO 1 LOC. 0 IS SET TO 177400, AND R4 IS CLEARED.
3738 A MODE 2 MOVB USES R0 TO MOVE BYTE 1 TO R4. AN INCREMENT
3739 IS USED TO CHECK THAT THE PROPER BYTE WAS MOVED AND SIGN X-TENDED.
3740 ****
3741 ****
3742 TEST 126 TEST MODE 2 - ODD BYTE W/ DOP INST.
3743 ****
3744 010242 005212 000126
3745 010244 022712
3746 010250 001017
3747 010252 005000
3748 010254 005004
3749 010256 005010
3750 010260 005110
3751 010262 105120
3752 010264 112004
3753 010266 005204
3754 010270 001404
3755 ****
3756 ****
3757 ****
3758 ****
3759 010272 012742 000234
3760 010276 005242
3761 010300 000000
3762 010302 005740
3763 010304 005700
3764 010306 001404
3765 ****
3766 ****
3767 ****
3768 ****
3769 010310 012742 000235
3770 010314 005242
3771 010316 000000
3772 ****

;***** THIS TEST VERIFIES MODE 2 DOP BYTE INSTRUCTIONS WHICH REFERENCE
;ODD BYTES. R0 IS SET TO 1 LOC. 0 IS SET TO 177400, AND R4 IS CLEARED.
;A MODE 2 MOVB USES R0 TO MOVE BYTE 1 TO R4. AN INCREMENT
;IS USED TO CHECK THAT THE PROPER BYTE WAS MOVED AND SIGN X-TENDED.

;***** TEST 126 TEST MODE 2 - ODD BYTE W/ DOP INST.

TST126: INC (R2) ;UPDATE TEST NUMBER
         CMP #126, (R2) ;SEQUENCE ERROR?
         BNE TST127-10 ;BR TO ERROR HALT ON SEQ ERROR
         CLR R0 ;R0=0
         CLR R4 ;R4=0
         CLR (R0) ;LOC. 0=0
         COM (R0) ;LOC. 0=177777
         COMB (R0)+ ;LOC 0=177400; R0=1
         MOVB (R0)+, R4 ;TRY DOP MODE 2 W/ ODD BYTE
         INC R4 ;CHECK RESULT OF MOVB
         BEQ DOPB2B ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                     ;CONDITIONAL BRANCH INST. AND
                     ;REPLACE THE MOVE INSTRUCTION
                     ;WHICH FOLLOWS W/ 770 <=====
                     ;MOVE TO MAILBOX # ***** 234 *****
                     ;SET MSGTYP TO FATAL ERROR
                     ;RESULT OF MOVB INCORRECT
                     ;BUMP R0 DOWN BY 2
                     ;CHECK R0 <=====

DOPB2B: TST -(R2) ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
                     ;CONDITIONAL BRANCH INST. AND
                     ;REPLACE THE MOVE INSTRUCTION
                     ;WHICH FOLLOWS W/ 761 <=====
                     ;MOVE TO MAILBOX # ***** 235 *****
                     ;SET MSGTYP TO FATAL ERROR
                     ;MODE 2 BYTE DID NOT INCREMENT REG. CORRECTLY
                     ;OR SEQUENCE ERROR <=====

         MOV #234, -(R2)
         INC -(R2)
         HALT

         TST -(R0)
         RO
         BEQ TST127
         MOV #235, -(R2)
         INC -(R2)
         HALT

```

K07

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DFKAA8.P11 T126 TEST MODE 2 - ODD BYTE W/ DOP INST.

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3773 *****
3774
3775 THIS TEST VERIFIES MODE 3 DOUBLE-OPERAND INSTRUCTIONS.
3776 ;LOC. 0 IS LOADED WITH ALTERNATING ZEROES AND ONES; AND R0 IS LOADED
3777 ;WITH ALTERNATING ONES AND ZEROES. A MODE 3 BIS IS USED TO SET R0
3778 ;TO -1 BY USING LOC. 0 AS THE SOURCE TO BIS THE ZEROES IN R0. THE
3779 ;RESULT IS TESTED BY INCREMENTING R0 AND CHECKING FOR ZERO.
3780
3781 *****
3782 TEST 127 TEST MODE 3 W/ DOP INSTS.
3783 *****
3784 010320 005212
3785 010322 022712 000127
3786 010326 001011
3787 010330 012737 052525 000000
3788 010336 012700 125252
3789 010342 053700 000000
3790 010346 005200
3791 010350 001404
3792 *****
3793 TST127: INC (R2) ;UPDATE TEST NUMBER
3794 CMP #127, (R2) ;SEQUENCE ERROR?
3795 BNE TST130-10 ;BR TO ERROR HALT ON SEQ ERROR
3796 MOV #052525, @#0 ;MOVE 52525 TO LOC. 0
3797 MOV #125252, R0 ;SET ALT. ONE AND ZERO IN R0
3798 BIS @#0, R0 ;TRY TO SET ALL OTHER BITS W/ MODE 3
3799 INC R0 ;TEST RESULT
3800 BEQ TST130
3801 *****
3802 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
3803 ; CONDITIONAL BRANCH INST. AND <=====
3804 ; REPLACE THE MOVE INSTRUCTION <=====
3805 ; WHICH FOLLOWS W/ 767 <=====
3806 *****
3807 010352 012742 000236
3808 INC -(R2) ;MOVE TO MAILBOX * ***** 236 *****
3809 HALT ;SET MSGTYP TO FATAL ERROR
3810 ;BIS W/ MODE 3 INCORRECT RESULT
3811 ;OR SEQUENCE ERROR
3812 *****
3813 THIS TEST VERIFIES MODE 3 DOUBLE OPERAND BYTE INSTRUCTIONS WHICH
3814 ADDRESS EVEN BYTES. BYTE 0 IS SET TO ALTERNATING 1'S AND 0'S; BYTE 1,
3815 ALTERNATING 0'S AND 1'S. R0 IS CLEARED AND A BISB IS USED TO
3816 SET THE LOW BYTE OF R0 TO 252.
3817
3818 *****
3819 TEST 130 TEST MODE 3 - EVEN BYTE W/ DOP INSTS.
3820 *****
3821 010362 005212
3822 010364 022712 000130
3823 010370 001011
3824 010372 012737 052652 000000
3825 010400 005000
3826 010402 153700 000000
3827 010406 022700 000252
3828 010412 001404
3829 *****
3830 TST130: INC (R2) ;UPDATE TEST NUMBER
3831 CMP #130, (R2) ;SEQUENCE ERROR?
3832 BNE TST131-10 ;BR TO ERROR HALT ON SEQ ERROR
3833 MOV #52652, @#0 ;MOVE 1'S AND 0' PATTERN TO LOC. C
3834 CLR R0 ;R0=0
3835 BISB @#0, R0 ;TRY R0=252 W/ MODE 3 - EVEN BYTE
3836 JMP #252, R0 ;BISB W/ EVEN BYTE SUCCESSFUL?
3837 BEQ TST131
3838 *****
3839 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
3840 ; CONDITIONAL BRANCH INST. AND <=====
3841 ; REPLACE THE MOVE INSTRUCTION <=====
3842 ; WHICH FOLLOWS W/ 767 <=====
3843 *****
3844 010414 012742 000237
3845 INC -(R2) ;MOVE TO MAILBOX * ***** 237 *****
3846 HALT ;SET MSGTYP TO FATAL ERROR
3847 ;BISB W/ MODE 3 - EVEN BYTE FAILED
3848 ;OR SEQUENCE ERROR

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3828      THIS TEST VERIFIES MODE 3 DOUBLE OPERAND BYTE INSTRUCTIONS
3829      WHICH ADDRESS ODD BYTES. THE SAME PROCEDURE USED IN PREVIOUS
3830      TEST IS USED HERE. THIS TIME BYTE 1 IS USED AS THE SOURCE BYTE.
3831      THE EXPECTED RESULT IS: R0 = 125.
3832
3833
3834      TEST 131 TEST MODE 3 - ODD BYTE W/ DOP INSTS.
3835
3836 010424 005212      TST131: INC   (R2) ;UPDATE TEST NUMBER
3837 010426 022712 000131      CMP   #131,(R2) ;SEQUENCE ERROR?
3838 010432 001011      BNE   TST132-10 ;BR TO ERROR HALT ON SEQ ERROR
3839 010434 012737 052652 000000      MOV   #52652,0#0 ;MOVE 1'S AND 0'S PATTERN TO LOC 0
3840 010442 005000      CLR   R0 ;R0=0
3841 010444 153700 000001      BISB  @#1,R0 ;TRY R0=152 W/ MODE 3 - ODD BYTE
3842 010450 022700 000125      CMP   #125,R0 ;R0=125?
3843 010454 001404      BEQ   TST132 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
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3848 010456 012742 000240      MOV   #240,-(R2) ;MOVE TO MAILBOX * ***** 240 *****
3849 010462 005242      INC   -(R2) ;SET MSGTYP TO FATAL ERROR
3850 010464 000000      HALT ;BISB W/ MODE 3 - ODD BYTE FAILED
3851
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3853
3854      TEST 132 TEST DEST. MODE 0-BYTE W/ DOP NON-MODIFYING MST
3855
3856 010466 005212      TST132: INC   (R2) ;UPDATE TEST NUMBER
3857 010470 022712 000132      CMP   #132,(R2) ;SEQUENCE ERROR?
3858 010474 001017      BNE   TST133-10 ;BR TO ERROR HALT ON SEQ ERROR
3859 010476 005000      CLR   R0 ;R0=0
3860 010500 105100      COMB  R0 ;R0=377
3861 010502 000263      +SEC!SEV ;SET C AND V BITS
3862 010504 132700 000200      BITB  #200,R0 ;TRY DOPNM DEST. MODE 0-BYTE
3863 010510 001403      BEQ   DNMB0A ;BR TO ERROR IF Z BIT SET
3864 010512 102402      BVS   DNMB0A ;BR TO ERROR IF V BIT SET
3865 010514 103001      BCC   DNMB0A ;BR TO ERROR IF C BIT CLEAR.
3866 010516 100404      BMI   DNMB0B ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
3867
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3871 010520 012742 000241      DNMB0A: MOV   #241,-(R2) ;MOVE TO MAILBOX * ***** 241 *****
3872 010520 012742 000241      DNMB0A: INC   -(R2) ;SET MSGTYP TO FATAL ERROR
3873 010524 005242      HALT ;CC'S INCORRECT
3874 010526 000009      DNMB0B: COMB  R0 ;CHECK DESTINATION DATA
3875 010530 105100      BEQ   TST133 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
3876 010532 001404      DNMB0B: BEQ   TST133 ;CONDITIONAL BRANCH INST. AND      <=====
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3881 010534 012742 000242      MOV   #242,-(R2) ;REPLACE THE MOVE INSTRUCTION
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DFKAAB.P11 T132 TEST DEST. MODE 0-BYTE W/ DOP NON-MODIFYING MST

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3882 010540 005242           INC      -(R2)      ;SET MSGTYP TO FATAL ERROR
3883 010542 000000           HALT
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3889 010544 005212           INC      (R2)      ;TEST 133 TEST DEST. MODE 1 W/ DOP NON-MODIFYING INST
3890 010546 022712 000133     CMP      #133,(R2)   ;*****  
3891 010552 001017           BNE      TST134-10    TEST 133 TEST DEST. MODE 1 W/ DOP NON-MODIFYING INST
3892 010554 005000           CLR      R0          ;BR TO ERROR HALT ON SEQ ERROR
3893 010556 005010           CLR      (R0)       ;R0=0
3894 010560 000241           CLC      ;LOC. 0=0
3895 010562 032710 177777     BIT      #177777,(R0) ;CLEAR C BIT
3896 010566 100403           BMI      DNM1A      ;TRY DOPNM DEST. MODE 1
3897 010570 102402           BVS      DNM1A      ;BR TO ERROR IF N BIT SET
3898 010572 103401           BCS      DNM1A      ;BR TO ERROR IF V BIT SET
3899 010574 001404           BEQ      DNM1B      ;BR TO ERROR IF C BIT SET
3900
3901
3902
3903
3904 010576 012742 000243     DNM1A:  MOV      #243,-(R2)  ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
3905 010576 012742           INC      -(R2)      CONDITIONAL BRANCH INST. AND <=====  
3906 010602 005242           HALT
3907 010604 000000           DNM1B:  TST      (R0)      REPLACE THE MOVE INSTRUCTION <=====  
3908 010606 005710           BEQ      TST134    WHICH FOLLOWS W/ 767 <=====  
3909 C10610 001404
3910
3911
3912
3913
3914 010612 012742 000244     MOV      #244,-(R2)  ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
3915 010616 005242           INC      -(R2)      CONDITIONAL BRANCH INST. AND <=====  
3916 010620 000000           HALT
3917
3918
3919
3920
3921
3922 010622 005212           TST134: INC      (R2)      ;TEST 134 TEST DEST. MODE 2 W/ DOP NON-MODIFYING INST.
3923 010624 022712 000134     CMP      #134,(R2)   ;*****  
3924 010630 001027           BNE      TST135-10    TEST 134 TEST DEST. MODE 2 W/ DOP NON-MODIFYING INST.
3925 010632 005000           CLR      R0          ;BR TO ERROR HALT ON SEQ ERROR
3926 010634 005010           CLR      (R0)       ;R0=0
3927 010636 052710 125252     BIS      #125252,(R0) ;LOC. 0=125252
3928 010642 032720 077777     BIT      #77777,(R0)+ ;TRY DOPNM INST W/ MODE 2
3929 010646 102402           BVS      DNM2A      ;BR TO ERROR IF V BIT SET
3930 010650 001401           BEQ      DNM2A      ;BR TO ERROR IF Z-BIT SET
3931 010652 100004           BPL      DNM2B      ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
3932
3933
3934
3935
3936 010654 012742 000245     DNM2A:  MOV      #245,-(R2)  CONDITIONAL BRANCH INST. AND <=====  
3937 010654 012742           MOV      #245,-(R2)  REPLACE THE MOVE INSTRUCTION <=====  
            ; WHICH FOLLOWS W/ 767 <=====  
            ; MOVE TO MAILBOX * ***** 245 *****
```

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MAINDEC-11-DFKAA-B 11.34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 318  
DFKAAB.P11 T134 TEST DEST. MODE 2 W/ DOP NON-MODIFYING INST.

3938 010660 005242  
 3939 010662 000000  
 3940 010664 005300  
 3941 010666 005300  
 3942 010E70 001404

DNM2B: INC -(R2)  
 HALT  
 DEC RO  
 DEC RO  
 BEQ DNM2D

;SET MSGTYP TO FATAL ERROR  
 ;COND. CODES INCORRECT  
 ;DECREMENT RO TO CHECK IT.

3943  
 3944  
 3945  
 3946  
 3947 010672 012742 000246  
 3948 010672 012742 000246  
 3949 010676 005242  
 3950 010700 000000  
 3951 010702 022710 125252  
 3952 010706 001404

DNM2C: MOV #246,-(R2)  
 INC -(R2)  
 HALT  
 DNM2D: CMP #125252,(RO)  
 BEQ TST135

;MOVE TO MAILBOX # \*\*\*\*\* 246 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;MODE 2 REGISTER NOT INCREMENTED BY 2  
 ;CHECK DEST. DATA

3953  
 3954  
 3955  
 3956  
 3957 010710 012742 000247  
 3958 010714 005242  
 3959 010716 000000

MOV #247,-(R2)  
 INC -(R2)  
 HALT

;MOVE TO MAILBOX # \*\*\*\*\* 247 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;DEST. DATA MODIFIED  
 ;OR SEQUENCE ERROR

3962  
 3963 ;\*\*\*\*\* TEST 135 TEST DEST. MODE 2-BYTE, W/DOP NON-MODIFYING INST \*\*\*\*\*

3964 ;\*\*\*\*\*  
 3965 010720 005212  
 3966 010722 022712 000135  
 3967 010726 001051  
 3968 010730 005000  
 3969 010732 005010  
 3970 010734 052710 052652  
 3971 010740 000263  
 3972 010742 132720 000201  
 3973 010746 001403  
 3974 010750 103002  
 3975 010752 102401  
 3976 010754 100404

TST135: INC (R2)  
 CMP #135,(R2)  
 BNE TST136-10  
 CLR RO  
 CLR (RO)  
 BIS #52652,(RO)  
 +SEC!SEV  
 BITB #201,(RO)+  
 BEQ DNMB2A  
 BCC DNMB2A  
 BVS DNMB2A  
 BMI DNMB2B

;UPDATE TEST NUMBER  
 ;SEQUENCE ERROR?  
 ;BR TO ERROR HALT C.I SEQ ERROR  
 ;RO=0  
 ;LOC. 0=0  
 ;LOC. 0=52652  
 ;SET C AND V BITS  
 ;TRY DOPNM INST. W/ MODE 2 EVEN BYTE  
 ;BR TO ERROR IF Z-BIT SET  
 ;BR TO ERROR IF C-BIT CLEAR  
 ;BR TO ERROR IF V-BIT SET

3977  
 3978  
 3979  
 3980

;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ;CONDITIONAL BRANCH INST. AND  
 ;REPLACE THE MOVE INSTRUCTION  
 ;WHICH FOLLOWS W/ 765

3981 010756  
 3982 010756 012742 000250  
 3983 010762 005242  
 3984 010764 000000  
 3985 010766 005300  
 3986 010770 001404

DNMB2A: MOV #250,-(R2)  
 INC -(R2)  
 HALT  
 DNMB2B: DEC RO  
 BEQ DNMB2C

;MOVE TO MAILBOX # \*\*\*\*\* 250 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;COND. CODES INCORRECT  
 ;CHECK DEST. REGISTER.

3987  
 3988  
 3989  
 3990  
 3991 010772 012742 000251  
 3992 010776 005242  
 3993 011000 000000

MOV #251,-(R2)  
 INC -(R2)  
 HALT

;MOVE TO MAILBOX # \*\*\*\*\* 251 \*\*\*\*\*  
 ;SET MSGTYP TO FATAL ERROR  
 ;DEST. REGISTER NOT INCREMENTED BY 1

MAINDEC-11-DFKAA-8 11.34 CPU TEST  
DFKAA8.P11 T135 TEST DEST. MODE 2-BYTE, W/DOP NON-MODIFYING INST  
MACYII 27(732) 01-OCT-76 15:03 PAGE 319

3994	011002	005200		DNMB2C: INC	R0	: R0=1	
3995	011004	132729	000201	BITB	\$201, (R0)+	: TRY DOPNM INST. W/MODE 2-ODD BYTE	
3996	011010	001402		BEQ	DNMB2D	: BR TO ERROR IF Z-BIT SET	
3997	011012	102401		BVS	DNMB2D	: BR TO ERROR IF V-BIT SET	
3998	011014	100004		BPL	DNMB2E		
3999						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
4000						CONDITIONAL BRANCH INST. AND	(*****)
4001						REPLACE THE MOVE INSTRUCTION	(*****)
4002						WHICH FOLLOWS W/ 745	(*****)
4003	011016	012742	000252	DNMB2D:	MOV	\$252, -(R2)	: MOVE TO MAILBOX # ***** 252 *****
4004	011016	012742	000252		INC	-(R2)	: SET MSGTYP TO FATAL ERROR
4005	011022	005242			HALT		: COND. CODES INCORRECT
4006	011024	000000		DNMB2E: DEC	RO	: DEC RO TO CHECK IT.	
4007	011026	005200			DEC	RO	
4008	011030	005300			BEQ	DNMB2F	
4009	011032	001404					
4010						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
4011						CONDITIONAL BRANCH INST. AND	(*****)
4012						REPLACE THE MOVE INSTRUCTION	(*****)
4013						WHICH FOLLOWS W/ 736	(*****)
4014	011034	012742	000253		MOV	\$253, -(R2)	: MOVE TO MAILBOX # ***** 253 *****
4015	011040	005242			INC	-(R2)	: SET MSGTYP TO FATAL ERROR
4016	011042	000000			HALT		: DEST. REGISTER NOT INCREMENTED BY 1
4017	011044	022710	052652	DNMB2F: CMP	\$52652, (R0)	: CHECK DEST. DATA IS !MODIFIED	
4018	011050	001404			BEQ	TST136	
4019						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
4020						CONDITIONAL BRANCH INST. AND	(*****)
4021						REPLACE THE MOVE INSTRUCTION	(*****)
4022						WHICH FOLLOWS W/ 727	(*****)
4023	011052	012742	000254		MOV	\$254, -(P2)	: MOVE TO MAILBOX # ***** 254 *****
4024	011056	005242			INC	-(R2)	: SET MSGTYP TO FATAL ERROR
4025	011060	000000			HALT		: DEST. DATA WAS MODIFIED.
4026						: OR SEQUENCE ERROR	
4027							
4028							
4029							
4030						***** TEST 136 TEST DEST. MODE 3-BYTES W/DOP NON-MODIFYING INST.	
4031						*****	
4032	011062	005212		TST136: INC	(R2)	: UPDATE TEST NUMBER	
4033	011064	022712	000136		CMP	\$136, (R2)	: SEQUENCE ERROR?
4034	011070	001050			BNE	TST137-10	: BR TO ERROR HALT ON SEQ ERROR
4035	011072	005000			CLR	RO	: RC=0
4036	011074	005010			CLR	(R0)	: LOC. 0=0
4037	011076	052710	125125		BIS	\$125125, (R0)	: LOC. 0=125125
4038	011102	105100			COMB	RO	: RO=377
4039	011104	005200			INC	RO	: RO=400
4040	011106	005010			CLR	(R0)	: LOC. 400=0
4041	011110	000263		+SEC!SEV			: C-BIT=V-BIT=1
4042	011112	132730	000201	BITB	\$201, J(R0)+	: TRY DOPNM W/MODE 3-EVEN BYTE	
4043	011116	001403			BEQ	DNMB3A	: BR TO ERROR IF Z BIT SET
4044	011120	102402			BVS	DNMB3A	: BR TO ERROR IF V BIT SET
4045	011122	103001			BCC	DNMB3A	: BR TO ERROR IF C BIT CLEAR
4046	011124	100004			BPL	DNMB3B	
4047						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
4048						CONDITIONAL BRANCH INST. AND	(*****)
4049						REPLACE THE MOVE INSTRUCTION	(*****)

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MAINDEC-11-DFKAA-9 11:34 CPU TEST MACYII 27(732) 01-OCT-76 15:03 PAGE 320  
DFKAA.B.P11 T136 TEST DEST. MODE 3-BYTES W/DOP NON-MODIFYING INST.

4050							WHICH FOLLOWS W/ 7E2	=====
4051	011126	012742	000255	DNMB3A:	MOV INC HALT	\$255,-(R2) -(R2)	; MOVE TO MAILBOX # ***** 255 ***** ; SET MSGTYP TO FATAL ERROR ; COND. CODES INCORRECT	
4052	011126	012742	000255	DNMB3B:	CMP SEQ	\$402,R0 DNMB3C	; CHECK DEST. REGISTER INC. BY 2 AND INC BY 2 AGAIN	
4053	011132	005242					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 753	=====
4054	011134	000000					; MOVE TO MAILBOX # ***** 256 ***** ; SET MSGTYP TO FATAL ERROR ; DEST. REGISTER NOT INCREMENTED BY 2	=====
4055	011136	022700	000402				; TRY DOPNM DEST MODE 3-BYTE(ODD) ; BR TO ERROR IF Z BIT SET ; BR TO ERROR IF V BIT SET	
4056	011142	001404					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 740	=====
4057								
4058								
4059								
4060								
4061	011144	012742	000256		MOV INC HALT	\$256,-(R2) -(R2)	; MOVE TO MAILBOX # ***** 256 ***** ; SET MSGTYP TO FATAL ERROR ; DEST. REGISTER NOT INCREMENTED BY 2	=====
4062	011150	005242		DNMB3C:	INC INC	R0 R0	; R0=404	
4063	011152	000000			BITS	\$201,0(R0)+	; TRY DOPNM DEST MODE 3-BYTE(ODD)	
4064	011154	005200			SEQ	DNMB3D	; BR TO ERROR IF Z BIT SET	
4065	011156	005200			VVS	DNMB3D	; BR TO ERROR IF V BIT SET	
4066	011160	132730	000201		BMI	DNMB3E		
4067	011164	001402					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 740	=====
4068	011166	102401						
4069	011170	100404						
4070								
4071								
4072								
4073								
4074	011172	012742	000257	DNMB3D:	MOV INC	\$257,-(R2) -(R2)	; MOVE TO MAILBOX # ***** 257 ***** ; SET MSGTYP TO FATAL ERROR ; COND. CODES INCORRECT	=====
4075	011172	012742	000257	DNMB3E:	CLR CMP BEQ	R4 \$125125,(R4) TST137	; R4=0 ; CHECK DEST. DATA	
4076	011176	005242					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 730	=====
4077	011200	000000						
4078	011202	005004						
4079	011204	022714	125125					
4080	011210	001404						
4081							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 730	=====
4082								
4083								
4084								
4085	011212	012742	000260		MOV INC	\$260,-(R2) -(R2)	; MOVE TO MAILBOX # ***** 250 ***** ; SET MSGTYP TO FATAL ERROR ; DEST. DATA MODIFIED	=====
4086	011216	005242					; OR SEQUENCE ERROR	
4087	011220	000000						
4088								
4089								
4090								
4091								
4092								
4093	011222	005212						
4094	011224	022712	000137	TST137:	INC CMP BNE	(R2) \$137,(R2) TST140-10	; UPDATE TEST NUMBER ; SEQUENCE ERROR? ; BR TO ERROR HALT ON SEQ ERROR	
4095	011230	001033			CLR	R0	; R0=0	
4096	011232	005000			CLR	(R0)	; LOC. 0=0	
4097	011234	005010			BIS	\$125252,(R0)	; LOC. 0=125125	
4098	011236	052710	125252		BIS	\$2,R0	; R0=2	
4099	011242	052700	000002		SCC		; SET ALL COND. CODE BITS	
4100	011246	000277			BIT	\$20000,-(R0)	; TRY DOPNM W/ MODE 4	
4101	011250	032740	020000		BMI	DNM4A	; BR TO ERROR IF N-BIT SET	
4102	011254	100403			VVS	DNM4A	; BR TO ERROR IF V-BIT SET	
4103	011256	102402			BCC	DNM4A	; BR TO ERROR IF C-BIT CHAR	
4104	011260	103001			BNE	DNM4B		
4105	011262	001004						

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MRINDEC-II-DFKAA-8 11:34 CPU TEST MACYII 27(732) 01-OCT-76 15:03 PAGE 321  
DFKAA8.P11 T13 TEST DEST. MODE 4 W/COP NON-MODIFYING INST.

4106 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 4107 CONDITIONAL BRANCH INST. AND =====  
 4108 REPLACE THE MOVE INSTRUCTION =====  
 4109 WHICH FOLLOWS W/ 763 =====

4110 011264 012742 000261 DNM4A: MOV #261,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 261 \*\*\*\*\*  
 4111 011264 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 4112 011270 005242 HALT ;COND. CODES INCORRECT  
 4113 011272 000000 TST ;CHECK DEST. REGISTER

4114 011274 005700 BEQ DNM4C ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 4115 011276 001404 DNM4B: MOV #262,-(R2) ;CONDITIONAL BRANCH INST. AND =====  
                           INC -(R2) ;REPLACE THE MOVE INSTRUCTION =====  
                           HALT ;WHICH FOLLOWS W/ 755 =====

4116 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 4117 CONDITIONAL BRANCH INST. AND =====  
 4118 REPLACE THE MOVE INSTRUCTION =====  
 4119 WHICH FOLLOWS W/ 755 =====

4120 011300 012742 000262 MOV #262,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 262 \*\*\*\*\*  
 4121 011304 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 4122 011306 000000 HALT ;DEST. REGISTER NOT DECREMENTED BY 2  
 4123 011310 022737 125252 000000 DNM4C: CMP #125252.3#0 ;CHECK DEST. DATA

4124 011316 001404 BEQ TST140 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
                           MOV #263,-(R2) ;CONDITIONAL BRANCH INST. AND =====  
                           INC -(R2) ;REPLACE THE MOVE INSTRUCTION =====  
                           HALT ;WHICH FOLLOWS W/ 745 =====

4125 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 4126 CONDITIONAL BRANCH INST. AND =====  
 4127 REPLACE THE MOVE INSTRUCTION =====  
 4128 WHICH FOLLOWS W/ 745 =====

4129 011320 012742 000263 MOV #263,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 263 \*\*\*\*\*  
 4130 011324 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 4131 011326 000000 HALT ;DEST. DATA MODIFIED =====  
                           ; OR SEQUENCE ERROR

4132 ;\*\*\*\*\*  
 4133 ;TEST 140 TEST DEST. MODE 4-BYTE W/ DOP NON-MODIFYING INST.  
 4134 ;\*\*\*\*\*  
 4135 ;\*\*\*\*\*  
 4136 ;\*\*\*\*\*  
 4137 011330 005212 TST140: INC (R2) ;UPDATE TEST NUMBER  
 4138 011332 022712 000140 CMP #140,(R2) ;SEQUENCE ERROR?  
 4139 011336 001051 BNE TST141-10 ;BR TO ERROR HALT ON SEQ ERROR  
 4140 011340 005000 CLR RO ;RO=0  
 4141 011342 005010 CLR (RO) ;LOC. 0=0  
 4142 011344 052710 052652 BIS #52652,(RO) ;LOC. 0=52652  
 4143 011350 052700 000002 BIS #2,RO ;RO=2  
 4144 011354 000257 CCC ;COND. CODES=0  
 4145 011356 132740 00J201 BITB #201,-(RO) ;TRY DOPNM INST W/MODE 4 ODD BYTE  
 4146 011362 102403 BVS DNMB4A ;BR TO ERROR IF V BIT SET  
 4147 011364 001402 BEQ DNMB4A ;BR TO ERROR IF Z BIT SET  
 4148 011366 103401 BCS DNMB4A ;BR TO ERROR IF C BIT SET  
 4149 011370 001004 BNE DNMB4B ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
                           ; CONDITIONAL BRANCH INST. AND =====  
                           ; REPLACE THE MOVE INSTRUCTION =====  
                           ; WHICH FOLLOWS W/ 763 =====

4150 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 4151 CONDITIONAL BRANCH INST. AND =====  
 4152 REPLACE THE MOVE INSTRUCTION =====  
 4153 WHICH FOLLOWS W/ 763 =====

4154 011372 DNMB4A: MOV #264,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 264 \*\*\*\*\*  
 4155 011372 012742 000264 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 4156 011376 005242 HALT ;COND. CODES INCORRECT  
 4157 011400 000000 TST ;CHECK DEST. REGISTER

4158 011402 022700 000001 DNMB4B: CMP #1,RO ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 4159 011406 001404 BEQ DNMB4C ;CONDITIONAL BRANCH INST. AND =====

4160 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 4161 CONDITIONAL BRANCH INST. AND =====

MAINDEC-11-DFKAR-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 322  
DFKAR8.P11 T140 TEST DEST. MODE 4-BYTE W/ DOP NON-MODIFYING INST.

4162						REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 754	<=====
4163							<=====
4164	011410	012742	000265		MOV INC HALT	MOVE TO MAILBOX * ***** 265 *****	
4165	011414	005242			*265,-(R2)	SET MSGTYP TO FATAL ERROR	
4166	011416	000000				DEST REG. NOT DECREMENTED BY 1	
4167	011420	132740	000201	DNMB4C:	BITB SEQ BMI	TRY DOPNM INST. W/MODE 4 EVEN BYTE	
4168	011424	001401			*201,-(R0)	BR TO ERROR IF Z-BIT SET	
4169	011426	100404			DNMB4D DNMB4E		
4170						TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
4171						CONDITIONAL BRANCH INST. AND	<=====
4172						REPLACE THE MOVE INSTRUCTION	<=====
4173						WHICH FOLLOWS W/ 744	<=====
4174	011430			DNMB4D:			
4175	011430	012742	000266		MOV INC HALT	MOVE TO MAILBOX * ***** 266 *****	
4176	011434	005242			*266,-(R2)	SET MSGTYP TO FATAL ERROR	
4177	011436	000000				COND. CODES INCORRECT	
4178	011440	005700		DNMB4E:	TST BEQ	CHECK DEST. REGISTER	
4179	011442	001404			RO		
4180					DNMB4F		
4181					MOV INC HALT	TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
4182					*267,-(R2)	CONDITIONAL BRANCH INST. AND	<=====
4183						REPLACE THE MOVE INSTRUCTION	<=====
4184	011444	012742	000267		SET MSGTYP TO FATAL ERROR	WHICH FOLLOWS W/ 736	<=====
4185	011450	005242			DNMB4F:	MOVE TO MAILBOX * ***** 267 *****	
4186	011452	000000			CMP BEQ	SET MSGTYP TO FATAL ERROR	
4187	011454	022710	052652		*52652,(R0)	DEST. REG. NOT DECREMENTED BY 1	
4188	011460	001404			TST141	CHECK DESTINATION DATA	
4189							
4190						TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
4191						CONDITIONAL BRANCH INST. AND	<=====
4192						REPLACE THE MOVE INSTRUCTION	<=====
4193	011462	012742	000270		DNMB4F:	WHICH FOLLOWS W/ 727	<=====
4194	011466	005242			MOV INC HALT	MOVE TO MAILBOX * ***** 270 *****	
4195	011470	000000			*270,-(R2)	SET MSGTYP TO FATAL ERROR	
4196						DEST. DATA MODIFIED	
4197						OR SEQUENCE ERROR	
4198						*****	
4199						; TEST 141 TEST DEST MODE 5 W/DOP NON-MODIFYING INST.	
4200						*****	
4201	011472	005212		TST141:	INC (R2)	UPDATE TEST NUMBER	
4202	011474	022712	000141		CMP #141,(R2)	SEQUENCE ERROR?	
4203	011500	001034			BNE TST142-10	BR TO ERROR HALT ON SEQ ERROR	
4204	011502	005000			CLR RO	RO=0	
4205	011504	005010			CLR (R0)	LOC 0=C	
4206	011506	052710	100000		BIS #100000,(R0)	LOC. 0=100000	
4207	011512	052700	000402		BIS #402,RO	RO=2	
4208	011516	000277			SCC	SET ALL COND. CODE BITS	
4209	011520	032750	100000		BIT #100000,2-(R0)	TRY DOPNM W/MODE 5	
4210	011524	102403			BVS DNMSA	BR TO ERROR IF V-BIT SET	
4211	011526	103002			BCC DNMSA	BR TO ERROR IF C-BIT CLEAR	
4212	011530	001401			BEQ DNMSA	BR TO ERROR IF Z-BIT SET	
4213	011532	100404			BMI DNMSB		
4214						TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
4215						CONDITIONAL BRANCH INST. AND	<=====
4216						REPLACE THE MOVE INSTRUCTION	<=====
4217						WHICH FOLLOWS W/ 763	<=====

MAINDEC-11-DFKAA-B 11:34 CPU TEST  
DFKAAB.P11 T141 TEST DEST MODE 5 MACY11 27(732) 01-OCT-76 15:03 PAGE 323

4218 011534	012742	000271	DNM5A:	MOV #271 -(R2)	MOVE TO MAILBOX # ***** 271 *****	
4219 011534	005242			INC -(R2)	SET MSGTYP TO FATAL ERROR	
4220 011540	005242			HALT	COND. CODES INCORRECT	
4221 011542	000000			CMP #400, R0	CHECK DEST. REGISTER	
4222 011544	022700	000400	DNM5B:	BEQ DNM5C		
4223 011550	001404				TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
4224					CONDITIONAL BRANCH INST. AND	(*****)
4225					REPLACE THE MOVE INSTRUCTION	(*****)
4226					WHICH FOLLOWS W/ 754	(*****)
4227						
4228 011552	012742	000272		MOV #272 -(R2)	MOVE TO MAILBOX # ***** 272 *****	
4229 011556	005242			INC -(R2)	SET MSGTYP TO FATAL ERROR	
4230 011560	000000			HALT	DEST. REGISTER NOT DECREMENTED BY 2	
4231 011562	022737	100000 000000	DNM5C:	CMP #100000, #00	CHECK DESTINATION DATA	
4232 011570	001404			BEQ TST142		
4233					TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
4234					CONDITIONAL BRANCH INST. AND	(*****)
4235					REPLACE THE MOVE INSTRUCTION	(*****)
4236					WHICH FOLLOWS W/ 744	(*****)
4237 011572	012742	000273		MOV #273 -(R2)	MOVE TO MAILBOX # ***** 273 *****	
4238 011576	005242			INC -(R2)	SET MSGTYP TO FATAL ERROR	
4239 011600	000000			HALT	DEST. DATA INCORRECTLY MODIFIED	
4240					OR SEQUENCE ERROR	
4241						
4242					*****	
4243					;TEST 142 TEST DEST. MODE 6 W/DOP NON-MODIFYING INST.	
4244					*****	
4245 011602	005212		TST142:	INC (R2)	UPDATE TEST NUMBER	
4246 011604	022712	000142		CMP #142, (R2)	SEQUENCE ERROR?	
4247 011610	001033			BNE TST143-10	BR TO ERROR HALT ON SEQ ERROR	
4248 011612	005000			CLR R0	R0=0	
4249 011614	005010			CLR (R0)	LOC> 0=0	
4250 011616	052710	000001		BIS #1, (R0)	LOC. 0=1	
4251 011622	005100			COM R0	R0=-1 C-BIT=1	
4252 011624	032760	000001 000001		BIT #1,1(R0)	TRY DOPNM W/MODE 6	
4253 011632	001403			BEQ DNM6A	BR TO ERROR IF Z-BIT SET	
4254 011634	102402			BVS DNM6A	BR TO ERROR IF V-BIT SET	
4255 011636	103001			BCC DNM6A	BR TO ERROR IF C-BIT CLEAR	
4256 011640	100004			BPL DNM6B		
4257					TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
4258					CONDITIONAL BRANCH INST. AND	(*****)
4259					REPLACE THE MOVE INSTRUCTION	(*****)
4260					WHICH FOLLOWS W/ 764	(*****)
4261 011642			DNM6A:			
4262 011642	012742	000274		MOV #274 -(R2)	MOVE TO MAILBOX # ***** 274 *****	
4263 011646	005242			INC -(R2)	SET MSGTYP TO FATAL ERROR	
4264 011650	000000			HALT	COND CODES INCORRECT	
4265 011652	022700	177777	DNM6B:	CMP #-1, R0	CHECK DEST. REGISTER	
4266 011656	001404			BEQ DNM6C		
4267					TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
4268					CONDITIONAL BRANCH INST. AND	(*****)
4269					REPLACE THE MOVE INSTRUCTION	(*****)
4270					WHICH FOLLOWS W/ 755	(*****)
4271 011660	012742	000275		MOV #275 -(R2)	MOVE TO MAILBOX # ***** 275 *****	
4272 011664	005242			INC -(R2)	SET MSGTYP TO FATAL ERROR	
4273 011666	000000			HALT	DEST. REGISTER MODIFIED	

## GO8

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 DFKAA8.P11 T142 TEST DEST. MODE 6 W/DOP NON-MODIFYING INST.

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4274 011670 022737 000001 000000 DNM6C: CMP #1,0#0 ;CHECK DEST. DATA
4275 011676 001404 BEQ TST143 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
4276 ; CONDITIONAL BRANCH INST. AND
4277 ; REPLACE THE MOVE INSTRUCTION
4278 ; WHICH FOLLOWS W/ 745
4279 ; =====
4280 011700 012742 000276 MOV #276,-(R2) ;MOVE TO MAILBOX # ***** 276 *****
4281 011704 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4282 011706 000000 HALT ;DEST. DATA MODIFIED
4283 ; OR SEQUENCE ERROR
4284
4285 ;*****
4286 ;TEST 143 TEST DEST MODE 7 W/DOP NON-MODIFYING INST.
4287 ;*****
4288 011710 005212 TST143: INC (R2) ;UPDATE TEST NUMBER
4289 011712 022712 000143 CMP #143,(R2) ;SEQUENCE ERROR?
4290 011716 001034 BNE TST144-10 ;BR TO ERROR HALT ON SEQ ERROR
4291 011720 005000 CLR R0 ;R0=0
4292 011722 005010 CLR (R0) ;LOC. 0=0 C-BIT=0
4293 011724 052710 125125 BIS #125125,(R0) ;LOC. 0=125125
4294 011730 052700 000001 BIS #1,R0 ;R0=1
4295 011734 132770 000125 000403 BITB #125,3403(R0) ;TRY DOPNM W/MODE 7
4296 011742 102403 BVS DNM7A ;BR TO ERROR IF V-BIT SET
4297 011744 100402 BMI DNM7A ;BR TO ERROR IF N-BIT SET
4298 011746 103401 BCS DNM7A ;BR TO ERROR IF C-BIT SET
4299 011750 001404 BEQ DNM7B ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
4300 ; CONDITIONAL BRANCH INST. AND
4301 ; REPLACE THE MOVE INSTRUCTION
4302 ; WHICH FOLLOWS W/ 763
4303 ; =====
4304 011752 DNM7A: ;MOVE TO MAILBOX # ***** 277 *****
4305 011752 012742 000277 MOV #277,-(R2) ;SET MSGTYP TO FATAL ERROR
4306 011756 005242 INC -(R2) ;COND. CODES INCORRECT
4307 011760 000000 HALT ;CHECK DEST. REGISTER
4308 011762 022700 000001 DNM7B: CMP #1,R0 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
4309 011766 001404 BEQ DNM7C ; CONDITIONAL BRANCH INST. AND
4310 ; REPLACE THE MOVE INSTRUCTION
4311 ; WHICH FOLLOWS W/ 754
4312 ; =====
4313 011770 012742 000300 DNM7C: MOV #300,-(R2) ;MOVE TO MAILBOX # ***** 300 *****
4314 011774 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4315 011776 000000 HALT ;DESTINATION REGISTER MODIFIED
4316 012000 022737 125125 000000 DNM7C: CMP #125125,0#0 ;CHECK DEST. DATA
4317 012006 001404 BEQ TST144 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
4318 ; CONDITIONAL BRANCH INST. AND
4319 ; REPLACE THE MOVE INSTRUCTION
4320 ; WHICH FOLLOWS W/ 744
4321 ; =====
4322 012010 012742 000301 DNM7C: MOV #301,-(R2) ;MOVE TO MAILBOX # ***** 301 *****
4323 012014 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4324 012016 000000 HALT ;DEST. DATA INCORRECT
4325 ; OR SEQUENCE ERROR
4326
4327
4328
4329 ;*****

```

MAINDEC-11-DFKAA-8 11.34 CPU TEST  
DFKAA8.P11 T143 TEST DEST MODE 7 W/DOP NON-MODIFYING INST.

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4330  
4331  
4332  
4333  
4334  
4335  
4336  
4337 012020 005212  
4338 012022 022712 000144  
4339 012026 001016  
4340 012030 005000  
4341 012032 005010  
4342 012034 005100  
4343 012036 005004  
4344 012040 010014  
4345 012042 102402  
4346 012044 001401  
4347 012046 100404  
4348  
4349  
4350  
4351  
4352 012050  
4353 012050 012742 000302  
4354 012054 005242  
4355 012056 000000  
4356 012060 005704  
4357 012062 001404  
4358  
4359  
4360  
4361  
4362 012064 012742 000303  
4363 012070 005242  
4364 012072 000000  
4365  
4366  
4367  
4368  
4369  
4370  
4371  
4372  
4373  
4374  
4375  
4376 012074 005212  
4377 012076 022712 000145  
4378 012102 001025  
4379 012104 005000  
4380 012106 005010  
4381 012110 005110  
4382 012112 010020  
4383 012114 100402  
4384 012116 102401  
4385 012120 001404

THIS TEST VERIFIES THE MOV DESTINATION MODE 1 INSTRUCTION.  
DATA IS SET IN R0 USING S0P INSTRUCTIONS AND THEN MOVED TO LOC. 0  
USING MOV SRC MODE 0, DEST. MODE 1.

\*\*\*\*\*  
TEST 144 TEST MOV DESTINATION MODE 1  
\*\*\*\*\*

TST144: INC (R2)  
CMP #144, (R2)  
BNE TST145-10  
CLR R0  
CLR (R0)  
COM R0  
CLR R4  
MOV R0, (R4)  
BVS MDM1A  
BEQ MDM1A  
BMI MDM1B  
; UPDATE TEST NUMBER  
; SEQUENCE ERROR?  
; BR TO ERROR HALT ON SEQ ERROR  
; R0=0  
; LOC. 0=0  
; R0=-1  
; R4 POINTS TO LOC. 0  
; TRY MOVE MODE 0,i  
; BR TO ERROR IF V SET  
; BR TO ERROR IF Z SET

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 770   
; =====

MDM1A:  
MOV #302, -(R2)  
INC -(R2)  
HALT  
TST145  
; MOVE TO MAILBOX # \*\*\*\*\* 302 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; CONDITION CODE NOT CORRECT

MDM1B:  
TST R4  
BEQ TST145  
; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND  
; REPLACE THE MOVE INSTRUCTION  
; WHICH FOLLOWS W/ 762   
; =====

MOV #303, -(R2)  
INC -(R2)  
HALT  
; MOVE TO MAILBOX # \*\*\*\*\* 303 \*\*\*\*\*  
; SET MSGTYP TO FATAL ERROR  
; DESTINATION REGISTER INCORRECTLY ALTERED  
; OR SEQUENCE ERROR

\*\*\*\*\*  
THIS TEST VERIFIES THE MOV DESTINATION MODE 2 INSTRUCTION.  
DATA IS SET IN R0 USING S0P INSTRUCTIONS AND THEN MOVED  
TO LOCATION 0 USING MOV SRC MODE 0, DEST. MODE 1.

\*\*\*\*\*  
TEST 145 TEST MOV DESTINATION MODE 2  
\*\*\*\*\*

TST145: INC (R2)  
CMP #145, (R2)  
BNE TST146-10  
CLR R0  
CLR (R0)  
COM (R0)  
MOV R0, (R0)+  
BMI MDM2A  
BVS MDM2A  
BEQ MDM2B  
; UPDATE TEST NUMBER  
; SEQUENCE ERROR?  
; BR TO ERROR HALT ON SEQ ERROR  
; R0=0  
; LOC. 0=0  
; LOC. 0=-1  
; TRY MOVE MODE 0,2  
; BR TO ERROR IF N SET  
; BR TO ERROR IF V SET

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DFKAA8.P11 T145 TEST MOV DESTINATION MODE 2

4386  
4387  
4388  
4389  
4390 012122 012742 000304 MDM2A:  
4391 012122 005242 000304 MOV #304,-(R2) ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
4392 012126 005242 HALT INC -(R2) CONDITIONAL BRANCH INST. AND  
4393 012130 000000 DEC RO REPLACE THE MOVE INSTRUCTION  
4394 012132 005300 DEC RO WHICH FOLLOWS W/ 771  
4395 012134 005300 BEQ MDM2D <=====  
4396 012136 001404  
  
4397  
4398  
4399  
4400 012140 012742 000305 MDM2C:  
4401 012140 005242 000305 MOV #305,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 304 \*\*\*\*\*  
4402 012144 005242 HALT INC -(R2) ; SET MSGTYP TO FATAL ERROR  
4403 012146 000000 TST BEQ 0x0 ; CC'S INCORRECT  
4404 012150 005737 000000 MDM2D: TST TST146  
4405 012154 001404 BEQ TST146 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
4406  
4407  
4408  
4409  
4410 012156 012742 000306 MDM2D:  
4411 012162 005242 000306 MOV #306,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 305 \*\*\*\*\*  
4412 012164 000000 INC HALT ; SET MSGTYP TO FATAL ERROR  
4413  
4414  
4415  
4416  
4417  
4418 THIS TEST VERIFIES DESTINATION MODE 2 W/MOV8 INSTS. TWO DIFFERENT MOV8  
4419 INSTRUCTIONS ARE USED TO MOVE A TEST PATTERN FIRST TO BYTE 0 THEN TO BYTE 1.  
4420  
4421  
4422  
4423 TEST 146 TEST MOV-BYTE DESTINATION MODE 2  
4424 012166 005212 TST146: INC (R2) ; UPDATE TEST NUMBER  
4425 012170 022712 000146 CMP #146,(R2) ; SEQUENCE ERROR?  
4426 012174 001046 BNE TST147-10 ; BR TO ERROR HALT ON SEQ ERROR  
4427 012176 005000 CLR RO ; RO=0  
4428 012200 005010 CLR (RO) ; LOC. 0=0  
4429 012202 112720 000125 MOVB #125,(R0)+ ; TRY DESTINATION MODE 2 W/EVEN BYTE  
4430 012206 102402 BVS MBDM2A ; BR TO ERROR IF V SET  
4431 012210 001401 BEQ MBDM2A ; BR TO ERROR IF Z SET  
4432 012212 100004 BPL MBDM2B  
  
4433  
4434  
4435  
4436 TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
4437 012214 012742 000307 MBDM2A: CONDITIONAL BRANCH INST. AND  
4438 012214 005242 000307 MOV #307,-(R2) REPLACE THE MOVE INSTRUCTION  
4439 012220 005242 HALT INC -(R2) WHICH FOLLOWS W/ 771 <=====  
4440 012222 000000 MBDM2B: CMP #1,RO ; MOVE TO MAILBOX # \*\*\*\*\* 307 \*\*\*\*\*  
4441 012224 022700 000001 HALT ; SET MSGTYP TO FATAL ERROR  
; CC'S INCORRECT



## K08

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 328  
DFKAAB.P11 T147 TEST MOV(S) DESTINATION MODE 3

4498	012352	001401		BEQ	MDM3A	;BR TO ERROR IF Z SET	
4499	012354	100404		BMI	MDM3B	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 766	<=====
4500							
4501							
4502							
4503							
4504	012356		MDM3A:				
4505	012356	012742	000314	MOV	#314,-(R2)	;MOVE TO MAILBOX # ***** 314 *****	
4506	012362	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
4507	012364	000000		HALT		;CC'S INCORRECT	
4508	012366	022700	000402	CMP	#402, R0	;CHECK DEST. MODE REGISTER	
4509	012372	001404		BEQ	MDM3C	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 757	<=====
4510							
4511							
4512							
4513							
4514	012374	012742	000315	MOV	#315,-(R2)	;MOVE TO MAILBOX # ***** 315 *****	
4515	012400	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
4516	012402	000000		HALT		;REGISTER NOT INCREMENTED BY 2	
4517	012404	022737	125252, 000000	CMP	#125252,0#0	;CHECK DESTINATION DATA	
4518	012412	001404		BEQ	MDM3D	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 747	<=====
4519							
4520							
4521							
4522							
4523	012414	012742	000316	MOV	#316,-(R2)	;MOVE TO MAILBOX # ***** 316 *****	
4524	012420	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
4525	012422	000000		HALT		;DESTINATION DATA INCORRECT	
4526	012424	112737	000125 000000	MOVB	#125,0#0	;TRY MOVB DESTINATION MODE Z EVEN BYTE	
4527	012432	022737	125125 000000	CMP	#125125,0#0	;CHECK DATA	
4528	012440	001404		BEQ	MDM3E	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 734	<=====
4529							
4530							
4531							
4532							
4533	012442	012742	000317	MOV	#317,-(R2)	;MOVE TO MAILBOX # ***** 317 *****	
4534	012446	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
4535	012450	000000		HALT		;DESTINATION DATA INCORRECT	
4536	012452	112737	000525 000001	MOVB	#525,0#1	;TRY MOVB DESTINATION MODE 2 ODD BYTE	
4537	012460	022737	052525 000000	CMP	#52525,0#0	;CHECK DATA	
4538	012466	001404		BEQ	TST150	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 721	<=====
4539							
4540							
4541							
4542							
4543	012470	012742	000320	MOV	#320,-(R2)	;MOVE TO MAILBOX # ***** 320 *****	
4544	012474	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
4545	012476	000000		HALT			

\*\*\*\*\*  
 THIS TEST VERIFIES THE MOV DESTINATION MODE 4 INSTRUCTION.  
 SOP INSTRUCTIONS ON R0 ARE USED TO CLEAR TARGET LOCATION 0.  
 R4 IS USED AS THE MODE 4 ADDRESSING REGISTER, AND  
 CONDITIONAL BRANCHES ARE USED TO VERIFY THE DATA.

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 DFKAAB.P11 T147 TEST MOV(B) DESTINATION MODE 3

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4554 ;*****
4555 ;TEST 150 TEST MOV DESTINATION MODE 4
4556 ;*****
4557 012500 005212 000150 TST150: INC (R2) ;UPDATE TEST NUMBER
4558 012502 022712 000150 CMP #150, (R2) ;SEQUENCE ERROR?
4559 012506 001026 000002 BNE TST151-10 ;BR TO ERROR HALT ON SEQ ERROR
4560 012510 005000 CLR R0 ;R0=0
4561 012512 005010 CLR (R0) ;LOC C=0
4562 012514 012704 000002 MOV #2, R4 ;R4=2
4563 012520 012744 012345 MOV #12345, -(R4) ;TRY MOV DEST. MODE 4
4564 012524 102402 BVS MDM4A ;BR TO ERROR IF V-BIT SET
4565 012526 001401 BEQ MDM4A ;BR TO ERROR IF Z-BIT SET
4566 012530 100004 BPL MDM4B ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
4567 ;CONDITIONAL BRANCH INST. AND
4568 ;REPLACE THE MOVE INSTRUCTION
4569 ;WHICH FOLLOWS W/ 767 <=====
4570 ;<=====

4571 012532 000321 MDM4A: MOV #321, -(R2) ;MOVE TO MAILBOX # ***** 321 *****
4572 012532 012742 000321 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4573 012536 005242 HALT ;CC'S NOT CORRECT
4574 012540 000000 MDM4B: TST R4 ;CHECK DECREMENTING OF MODE 4 REG.
4575 012542 005704 BEQ MDM4C ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
4576 012544 001404 ;CONDITIONAL BRANCH INST. AND
4577 ;REPLACE THE MOVE INSTRUCTION
4578 ;WHICH FOLLOWS W/ 761 <=====
4579 ;<=====

4581 012546 012742 000322 MDM4C: MOV #322, -(R2) ;MOVE TO MAILBOX # ***** 322 *****
4582 012552 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4583 012554 000000 HALT ;DESTINATION MODE REGISTER NOT DECREMENTED BY 2
4584 012556 022710 012345 CMP #12345, (R0) ;CHECK DESTINATION DATA
4585 012562 001404 BEQ TST151 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
4586 ;CONDITIONAL BRANCH INST. AND
4587 ;REPLACE THE MOVE INSTRUCTION
4588 ;WHICH FOLLOWS W/ 752 <=====
4589 ;<=====

4590 012564 012742 000323 MOV #323, -(R2) ;MOVE TO MAILBOX # ***** 323 *****
4591 012570 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
4592 012572 000000 HALT ;DESTINATION DATA INCORRECT
4593 ; OR SEQUENCE ERROR
4594 ;<=====

4595 ;*****
4596 ;*****
4597 ;THIS TEST VERIFIES THE MOVB DESTINATION MODE 4 INSTRUCTION
4598 ;ON BOTH ODD AND EVEN BYTES. S0P INSTRUCTIONS ON R4 ARE
4599 ;USED TO CLEAR TARGET LOCATION 0. R0 IS USED AS THE MODE 4
4600 ;ADDRESSING REGISTER, AND CMP AND CONDITIONAL BRANCH
4601 ;INSTRUCTIONS ARE USED TO VERIFY THE DATA.
4602 ;<=====

4603 ;*****
4604 ;TEST 151 TEST MOVB DESTINATION MODE 4
4605 ;*****
4606 012574 005212 000151 TST151: INC (R2) ;UPDATE TEST NUMBER
4607 012576 022712 000151 CMP #151, (R2) ;SEQUENCE ERROR?
4608 012602 001046 BNE TST152-10 ;BR TO ERROR HALT ON SEQ ERROR
4609 012604 005004 CLR R4 ;R4=0

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MRINDEC-11-DFKRAA-B 11-34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 330  
 DFKRAA.B.P11 T151 TEST MOVB DESTINATION MODE 4

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4610 012606 005014           CLR   (R4)      ;LOC. D=0
4611 012610 012700 000002     MOV   #2, R0    ;R0 = 2
4612 012614 112740 125125     MOVB  #125125,-(R0) ;TRY MOVB DEST. MODE 4-ODD BYTE
4613 012620 020027 000001     CMP   R0, #1      ;CHECK THAT DEST. REG. WAS DECREMENTED
4614 012624 001404           BEQ   MBDM4A
4615                               ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
4616                               ; CONDITIONAL BRANCH INST. AND             <=====
4617                               ; REPLACE THE MOVE INSTRUCTION             <=====
4618                               ; WHICH FOLLOWS W/ 767                  <=====

4619 012626 012742 000324           MOV   #324,-(R2) ;MOVE TO MAILBOX # ****** 324 *****
4620 012632 005242           INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
4621 012634 000000           HALT
4622 012636 021427 052400           MBDM4A: CMP   (R4), #52400 ;DESTINATION REG. NOT DECREMENTED BY 1
4623 012642 001404           BEQ   MBDM4B ;CHECK DEST. DATA
4624                               ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
4625                               ; CONDITIONAL BRANCH INST. AND             <=====
4626                               ; REPLACE THE MOVE INSTRUCTION             <=====
4627                               ; WHICH FOLLOWS W/ 760                  <=====

4628 012644 012742 000325           MOV   #325,-(R2) ;MOVE TO MAILBOX # ****** 325 *****
4629 012650 005242           INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
4630 012652 000000           HALT
4631 012654 112740 125125           MBDM4B: MOVB  #125125,-(R0) ;TRY MOVB DEST. MODE 4--EVEN BYTE
4632 012660 102402           BVS   MBDM4C ;BR. TO ERROR IF V-BIT SET
4633 012662 001401           BEQ   MBDM4C ;BR TO ERROR IF Z-BIT SET
4634 012664 100004           BPL   MBDM4D
4635                               ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
4636                               ; CONDITIONAL BRANCH INST. AND             <=====
4637                               ; REPLACE THE MOVE INSTRUCTION             <=====
4638                               ; WHICH FOLLOWS W/ 747                  <=====

4639 012666 012742 000326           MBDM4C: MOV   #326,-(R2) ;MOVE TO MAILBOX # ****** 326 *****
4640 012666 005242           INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
4641 012672 005242           HALT
4642 012674 000000           MBDM4D: TST   R0      ;COND. CODES INCORRECT
4643 012676 005700           BEQ   MBDM4E ;CHECK MODE 4 DEST. REGISTER
4644 012700 001404
4645                               ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
4646                               ; CONDITIONAL BRANCH INST. AND             <=====
4647                               ; REPLACE THE MOVE INSTRUCTION             <=====
4648                               ; WHICH FOLLOWS W/ 741                  <=====

4649 012702 012742 000327           MBDM4E: MOV   #327,-(R2) ;MOVE TO MAILBOX # ****** 327 *****
4650 012706 005242           INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
4651 012710 000000           HALT
4652 012712 021427 052525           MBDM4E: CMP   (R4), #52525 ;DESTINATION REG NOT DECREMENTED BY 1
4653 012716 001404           BEQ   TST152 ;CHECK DEST. DATA
4654                               ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
4655                               ; CONDITIONAL BRANCH INST. AND             <=====
4656                               ; REPLACE THE MOVE INSTRUCTION             <=====
4657                               ; WHICH FOLLOWS W/ 732                  <=====

4658 012720 012742 000330           MOV   #330,-(R2) ;MOVE TO MAILBOX # ****** 330 *****
4659 012724 005242           INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
4660 012726 000000           HALT
4661
4662
4663
4664
4665
  ;***** THIS TEST VERIFIES THE MOV DESTINATION MODE 5 AND THE MOVB
  ;
```

4666 :DESTINATION MODE 5 - EVEN BYTE INSTRUCTIONS. R4 IS A  
 4667 :pointer to target location 0 AND R0 IS SETUP TO  
 4668 :POINT TO LOCATION 376 FOR THE MOV AND LOCATION 404 FOR  
 4669 :THE MOVB INSTRUCTIONS. CMP INSTRUCTIONS ARE USED TO VERIFY  
 4670 :PROPER ADDRESSING AND DATA.  
 4671 ;  
 4672 ;\*\*\*\*\*  
 4673 ;TEST 152 TEST MOV DESTINATION MODE 5  
 4674 ;\*\*\*\*\*  
 4675 012730 005212 000152 TST152: INC (R2) ;UPDATE TEST NLMRBR  
 4676 012732 022712 000152 CMP #152,(R2) ;SEQUENCE ERROR?  
 4677 012736 001051 BNE TST153-10 ;BR TO ERROR HALT ON SEQ ERROR  
 4678 012740 005004 CLR R4 ;R4=0  
 4679 012742 005014 CLR (R4) ;LOC. 0 = 0  
 4680 012744 012700 000400 MOV #400,R0 ;R0=400  
 4681 012750 012750 004321 MOV #4321,0-(R0) ;TRY MOV DEST. MODE 5  
 4682 012754 102402 BVS MDM5A ;BR TO ERROR IF V-BIT SET  
 4683 012756 001401 BEQ MDM5A ;BR TO ERROR IF Z-BIT SET  
 4684 012760 100004 BPL MDM5B ;  
 4685 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 4686 ; CONDITIONAL BRANCH INST. AND <=====  
 4687 ; REPLACE THE MOVE INSTRUCTION <=====  
 4688 ; WHICH FOLLOWS W/ 767 <=====  
 4689 012762 012742 000331 MDM5A:  
 4690 012762 005242 000331 MOV #331,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 331 \*\*\*\*\*  
 4691 012766 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 4692 012770 000000 HALT ;COND. CODES INCORRECT  
 4693 012772 022700 000376 MDM5B: CMP #376,R0 ;CHECK MODE 5 REG. WAS DECREMENTED  
 4694 012776 001404 BEQ MDM5C ;  
 4695 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 4696 ; CONDITIONAL BRANCH INST. AND <=====  
 4697 ; REPLACE THE MOVE INSTRUCTION <=====  
 4698 ; WHICH FOLLOWS W/ 760 <=====  
 4699 013000 012742 000332 MDM5C:  
 4700 013004 005242 INC #332,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 332 \*\*\*\*\*  
 4701 013006 000000 HALT ;SET MSGTYP TO FATAL ERROR  
 4702 013010 022714 004321 MDM5D: CMP #4321,(R4) ;MODE 5 REGISTER NOT DECREMENTED BY 2  
 4703 013014 001404 BEQ MDM5D ;CHECK D'ST. DATA  
 4704 ;  
 4705 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 4706 ; CONDITIONAL BRANCH INST. AND <=====  
 4707 ; REPLACE THE MOVE INSTRUCTION <=====  
 4708 013016 012742 000333 MDM5D:  
 4709 013022 005242 INC #333,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 333 \*\*\*\*\*  
 4710 013024 000000 HALT ;SET MSGTYP TO FATAL ERROR  
 4711 013026 012700 000406 MDM5D: MOV #406,R0 ;DEST. DATA INCORRECT  
 4712 013032 112750 000377 MOVB #377,0-(R0) ;R0=406  
 4713 013036 022700 000404 CMP #404,R0 ;TRY MOV DEST. MODE 5 --EVEN BYTE  
 4714 013042 001404 BEQ MDM5E ;CHECK MODE 5 REG.  
 4715 ;  
 4716 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 4717 ; CONDITIONAL BRANCH INST. AND <=====  
 4718 ; REPLACE THE MOVE INSTRUCTION <=====  
 4719 013044 012742 000334 MDM5E:  
 4720 013050 005242 INC #334,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 334 \*\*\*\*\*  
 4721 013052 000000 HALT ;SET MSGTYP TO FATAL ERROR  
 ;MODE 5 REGISTER NOT DECREMENTED BY 2

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DFKAA8.P11 T152 TEST MOV DESTINATION MODE 5

4722 013054 022714 177721	MOMSE: CMP BEQ	0177721,(R4) TST153	:CHECK DEST. DATA
4723 013060 001404			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS w/ 727 <span style="float: right;">(*****)</span>
4724			<span style="float: right;">(*****)</span>
4725			<span style="float: right;">(*****)</span>
4726			<span style="float: right;">(*****)</span>
4727			<span style="float: right;">(*****)</span>
4728 013062 012742 0C0305	MOV INC HALT	*335,-(R2)	:MOVE TO MAILBOX # ***** 335 ***** SET MSGTYP TO FATAL ERROR DEST. DATA INCORRECT OR SEQUENCE ERROR
4729 013066 005242			
4730 013070 000000			
4731			
4732			
4733			
4734			
4735			***** THIS TEST VERIFIES THE MOV DESTINATION MODE 6 AND MOVB - EVEN BYTE
4736			DESTINATION MODE 6 INSTRUCTIONS. R0 IS USED TO SETUP TARGET LOC.0
4737			FOR BOTH TESTS. PATTERNS OF ONES AND ZEROES ARE MOVED INTO LOC.0
4738			BY MODE 6 INSTRUCTIONS, AND CMP INSTRUCTIONS ARE USED TO VERIFY
4739			PROPER ADDRESSING AND DATA.
4740			
4741			***** TEST 153 TEST MOV DESTINATION MODE 6
4742			*****
4743			TST153: INC (R2) :UPDATE TEST NUMBER
4744 013072 005212	000153	CMP *153,(R2) :SEQUENCE ERROR?	
4745 013074 022712		BNE TST154-10 :BR TO ERROR HALT ON SEQ ERROR	
4746 013100 001054		CLR R0 :R0=0	
4747 013102 005000		CLR (R0) :LOC. 0=0	
4748 013104 005010		INC R0 :R0=1	
4749 013106 005200		MOV *052525,-1(R0) :TRY MOV DEST. MODE 6	
4750 013110 012760	052525 177777	BVS MDM6A :BR TO ERROR IF V-BIT SET	
4751 013116 102402		BEQ MDM6A :BR TO ERROR IF Z-BIT SET	
4752 013120 001401		BPL MDM6B	
4753 013122 100004			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS w/ 757 <span style="float: right;">(*****)</span>
4754			<span style="float: right;">(*****)</span>
4755			<span style="float: right;">(*****)</span>
4756			<span style="float: right;">(*****)</span>
4757			<span style="float: right;">(*****)</span>
4758 013124		MDM6A:	
4759 013124 012742 000336		MOV -(R2)	:MOVE TO MAILBOX # ***** 336 *****
4760 013130 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
4761 013132 000000		HALT	:COND. CODES INCORRECT
4762 013134 022700 000001		CMP !,R0	:CHECK DEST. REGISTER UNALTERED
4763 013140 001404		BEQ MDM6C	
4764			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS w/ 760 <span style="float: right;">(*****)</span>
4765			<span style="float: right;">(*****)</span>
4766			<span style="float: right;">(*****)</span>
4767			<span style="float: right;">(*****)</span>
4768 013142 012742 000337		MOV -(R2)	:MOVE TO MAILBOX # ***** 337 *****
4769 013146 005242		INC -(R2)	:SET MSGTYP TO FATAL ERROR
4770 013150 000000		HALT	:DEST. REGISTER INCORRECTLY ALTERED
4771 013152 022737 052525 000000		CMP *52525,000	:CHECK DEST. DATA
4772 013160 001404		BEQ MDM6D	
4773			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS w/ 750 <span style="float: right;">(*****)</span>
4774			<span style="float: right;">(*****)</span>
4775			<span style="float: right;">(*****)</span>
4776			<span style="float: right;">(*****)</span>
4777 013162 012742 000340		MOV *340,-(R2)	:MOVE TO MAILBOX # ***** 340 *****

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 DFKAAB.P11 T153 TEST MOV DESTINATION MODE 6

4778	013166	005242			INC	- (R2)	: SET MSGTYP TO FATAL ERROR	
4779	013170	000000			HALT		: DEST. DATA INCORRECT	
4780	013172	012700	000002	177777	M0M6D:	MOV #2, R0	: RO=2	
4781	013176	112760	000377		MOV B	#377, -1(R0)	: TRY MOVB DEST. MODE 6	
4782	013204	022700	000002		CMP	#2, R0	: CHECK DEST. REGISTER UNALTERED	
4783	C13210	001404			BEQ	M0M6E		
4784							: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(=====)
4785							CONDITIONAL BRANCH INST. AND	(=====)
4786							REPLACE THE MOVE INSTRUCTION	(=====)
4787							WHICH FOLLOWS W/ 734	(=====)
4788	013212	012742	000341		MOV	#341, -(R2)	: MOVE TO MAILBOX # ***** 341 *****	
4789	013216	005242			INC	-(R2)	: SET MSGTYP TO FATAL ERROR	
4790	013220	000000			HALT		: DEST. REGISTER INCORRECTLY ALTERED	
4791	013222	022737	177525	000000	M0M6E:	CMP #177525, R0	: CHECK DEST. DATA	
4792	013230	001404			BEQ	TST154		
4793							: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(=====)
4794							CONDITIONAL BRANCH INST. AND	(=====)
4795							REPLACE THE MOVE INSTRUCTION	(=====)
4796							WHICH FOLLOWS W/ 724	(=====)
4797	013232	012742	000342		MOV	#342, -(R2)	: MOVE TO MAILBOX # ***** 342 *****	
4798	013236	005242			INC	-(R2)	: SET MSGTYP TO FATAL ERROR	
4799	013240	000000			HALT		: DEST. DATA INCORRECT	
4800							; OR SEQUENCE ERROR	
4801								
4802								
4803								
4804								
4805								
4806								
4807								
4808								
4809								
4810								
4811								
4812	013242	005212			TST154:	INC (R2)	: UPDATE TEST NUMBER	
4813	013244	022712	000154			CMP #154, (R2)	: SEQUENCE ERROR?	
4814	013250	001053				BNE TST155-10	: BR TO ERROR HALT ON SEQ ERROR	
4815	013252	005004				CLR R4	: R4=0	
4816	013254	005014				CLR (R4)	: LOC.0=0	
4817	013256	012700	000403	177777		MOV #403, R0	: RO=403	
4818	013262	012770	070707			MOV #70707, 3-1(R0)	: TRY MOV W/DEST MODE 7	
4819	013270	102402				BVS M0M7A	: BR. TO ERROR IF V-BIT SET	
4820	013272	001401				BEQ M0M7A	: BR TO ERROR IF Z-BIT SET	
4821	013274	100004				BPL M0M7B		
4822							: TO SCOPE: CLEAR THE RIGHT B E ? THIS	(=====)
4823							CONDITIONAL BRANCH IN T. AND	(=====)
4824							REPLACE THE MOVE INSTRUCTION	(=====)
4825							WHICH FOLLOWS W/ 766	(=====)
4826	013276							
4827	013276	012742	000343		M0M7A:	MOV #343, -(R2)	: MOVE TO MAILBOX # ***** 343 *****	
4828	013302	005242				INC -(R2)	: SET MSGTYP TO FATAL ERROR	
4829	013304	000000				HALT	: COND. CODES INCORRECT	
4830	013306	022700	000403		M0M7B:	CMP #403, R0	: CHECK DEST. REGISTER	
4831	013312	001404				BEQ M0M7C		
4832							: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(=====)
4833							CONDITIONAL BRANCH INST. AND	(=====)

4834  
 4835  
 4836 013314 012742 000344 :MOV #344,-(R2) :REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 757 <===== <=====  
 4837 013320 005242 INC -(R2) :MOVE TO MAILBOX # \*\*\*\*\* 344 \*\*\*\*\*  
 4838 013322 000000 HALT :SET MSGTYP TO FATAL ERROR  
 4839 013324 022737 070707 000000 MDM?C: CMP #70707,3#0 :DEST. REGISTER INCORRECTLY ALTERED  
 4840 013332 001404 BEQ MDM7D :CHECK DEST. DATA  
 4841 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 4842 : CONDITIONAL BRANCH INST. AND  
 4843 : REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 747 <===== <===== <===== <=====  
 4844 :  
 4845 013334 012742 000345 :MOV #345,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 345 \*\*\*\*\*  
 4846 013340 005242 INC -(R2) :SET MSGTYP TO FATAL EROR  
 4847 013342 000000 HALT :DEST. DATA INCORRECT  
 4848 013344 112770 107070 000001 MDM7D: MOVB #1C7070,31(R0) :TRY MOVB W/DEST MODE ?--ODD BYTE  
 4849 013352 022700 000403 BEQ #403,R0 :CHECK MODE 7 DEST. REG.  
 4850 013356 001404 MDM7E :  
 4851 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 4852 : CONDITIONAL BRANCH INST. AND  
 4853 : REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 735 <===== <===== <===== <=====  
 4854 :  
 4855 013360 012742 000346 :MOV #346,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 346 \*\*\*\*\*  
 4856 013364 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 4857 013366 000000 HALT :DEST. DATA INCORRECT  
 4858 013370 022737 034307 000000 MDM7E: CMP #34307,3#0 :CHECK DEST. DATA  
 4859 013376 001404 BEQ TST155 :  
 4860 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 4861 : CONDITIONAL BRANCH INST. AND  
 4862 : REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 725 <===== <===== <===== <=====  
 4863 :  
 4864 013400 012742 000347 :MOV #347,-(R2) :MOVE TO MAILBOX # \*\*\*\*\* 347 \*\*\*\*\*  
 4865 013404 005242 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 4866 013406 000000 HALT :DESTINATION DATA INCORRECT  
 4867 : OR SEQUENCE ERROR  
 4868 :  
 4869 :\*\*\*\*\*  
 4870 :  
 4871 : THIS TEST VERIFIES MODE 4 DOUBLE OPERAND INSTRUCTIONS.  
 4872 : THE TEST USES MODE 4 ADDRESSING WITH REGISTER 0 TO MOVE THRU A  
 4873 : TABLE OF OPERANDS. THE TABLE OF OPERANDS AND THE WORK LOCATION IS  
 4874 : STORED FOLLOWING THE TEST CODE. A SERIES OF 5 DOP INSTRUCTIONS UTILIZES  
 4875 : THE DATA IN THE TABLE TO CYCLE THE WORK LOCATION THRU A SET OF  
 4876 : VALUE. THE DATA HAS BEEN CHOSEN TO INSURE THAT NO SINGLE ERROR WILL  
 4877 : GO UNDETECTED. WORD AND BYTE INSTRUCTION ACCESSING BOTH EVEN AND  
 4878 : ODD ADDRESSES ARE USED IN THE TEST. THE LISTING SHOWS THE  
 4879 : EXPECTED INTERMEDIATE RESULT AS EACH INSTRUCTION IS EXECUTED.  
 4880 :  
 4881 :\*\*\*\*\*  
 4882 : TEST 155 TEST MODE 4 W/ DOP INSTS.  
 4883 :\*\*\*\*\*  
 4884 013410 005212 TST155: INC (R2) :UPDATE TEST NUMBER  
 4885 013412 022712 000155 CMP #155,(R2) :SEQUENCE ERROR?  
 4886 013416 001015 BNE DOP4 :BR TO ERROR HALT ON SEQ ERROR  
 4887 013420 012700 013472 MOV #TBL1,R0 :INITIALIZE R0  
 4888 013424 014037 013472 MOV -(R0),#TBL1 :TBL1=125252  
 4889 013430 064037 013472 ADD -(R0),#TBL1 :TBL1=000377

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DFKAA8.P11 T155 TEST MODE 4 W/ DOP INSTS.

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4890 013434 144037 013472      B1CB  -(R0),@TBL1    ;TBL1=000252
4891 013440 154037 013473      BISB  -(R0),@TBL1+1  ;TBL1=125252
4892 013444 024037 013472      CMP   -(R0),@TBL1    ;CHECK RESULT
4893 013450 001411      BEQ   TST156

4894                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      (****)
4895                                     ; CONDITIONAL BRANCH INST. AND      (****)
4896                                     ; REPLACE THE MOVE INSTRUCTION      (****)
4897                                     ; WHICH FOLLOWS W/ 763      (****)

4898 013452      DCP4:      MOV   #350,-(R2)  ;MOVE TO MAILBOX # ***** 350 *****
4899 013452 012742 000350      INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
4900 013456 005242      HALT
4901 013460 000000      TBL1:  0

4902
4903
4904 013462 125252      125252
4905 013464 052652      52652
4906 013466 053125      53125
4907 013470 125252      125252
4908 013472 000000      TBL1:  0

4909
4910
4911
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4913
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4916
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4918
4919
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4921
4922 013474 005212      TST156: INC  (R2)    ;UPDATE TEST NUMBER
4923 013476 022712 000156      CMP   #156,(R2)  ;SEQUENCE ERROR?
4924 013502 001015      BNE   DOP5    ;BR TO ERROR HALT ON SEQ ERROR
4925 013504 012700 013560      MOV   #TBL2+2, R0  ;INITIALIZE R0
4926 013510 015037 013472      MOV   @-(R0),@TBL1  ;TBL1=125252
4927 013514 065037 013472      ADD   @-(R0),@TBL1  ;TBL1=000377
4928 013520 145037 013472      B1CB  @-(R0),@TBL1  ;TBL1=000252
4929 013524 155037 013473      BISB  @-(R0),@TBL1+1 ;TBL1=125252
4930 013530 025037 013472      CMP   @-(R0),@TBL1    ;CHECK RESULT
4931 013534 001411      BEQ   TST157

4932                                     ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      (****)
4933                                     ; CONDITIONAL BRANCH INST. AND      (****)
4934                                     ; REPLACE THE MOVE INSTRUCTION      (****)
4935                                     ; WHICH FOLLOWS W/ 763      (****)

4936 013536      DOP5:      MOV   #351,-(R2)  ;MOVE TO MAILBOX # ***** 351 *****
4937 013536 012742 000351      INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
4938 013542 005242      HALT
4939 013544 000000      TBL2:  TBL1-10
4940
4941 013546 013462      TBL1-6
4942 013550 013464      TBL1-5
4943 013552 013465      TBL1-4
4944 013554 013466      TBL1-2
4945 013556 013470

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4946 ****
4947
4948      THIS TEST VERIFIES MODE 6 DOUBLE OPERAND INSTRUCTIONS.
4949      IT USES THE SAME DATA AS THAT USED IN THE MODE 4 TESTS.
4950      THIS TIME THE DATA IS ACCESSED USING MODE 6. R0 IS SET
4951      TO POINT TO THE MIDDLE OF THE TABLE. THE TABLE IS ACCESSED FROM
4952      BOTTOM TO TOP BY VARYING THE OFFSET IN THE MODE 6 INSTRUCTIONS.
4953      THE DATA RESULTS ARE IDENTICAL TO THOSE EXPECTED IN THE MODE 4
4954      TESTS.
4955
4956 ****
4957      TEST 157      TEST MODE 6 W/ DOP INSTS.
4958 ****
4959 013560 005212
4960 013562 022712 000157
4961 013566 001022
4962 013570 012700 013466
4963 013574 016037 000002 013472
4964 013602 066037 000000 013472
4965 013610 146037 177777 013472
4966 013616 156037 177776 013473
4967 013624 026037 177774 013472
4968 013632 001404
4969      TST157: INC    (R2)      ;UPDATE TEST NUMBER
4970          CMP    #157, (R2)   ;SEQUENCE ERROR?
4971          BNE    TST160-10  ;BR TO ERROR HALT ON SEQ ERROR
4972          MOV    #TBL1-4, R0  ;INITIALIZE R0
4973          MOV    2(R0), #TBL1  ;TBL1=125252
4974          ADD    0(R0), #TBL1  ;TBL1=000377
4975          BICB   -1(R0), #TBL1  ;TBL1=000252
4976          BISB   -2(R0), #TBL1+1 ;TBL1=125252
4977          CMP    -4(R0), #TBL1  ;CHECK RESULT
4978          BEQ    TST160
4979          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
4980          ; CONDITIONAL BRANCH INST. AND      <=====
4981          ; REPLACE THE MOVE INSTRUCTION      <=====
4982          ; WHICH FOLLOWS W/ 756      <=====
4983
4984 013634 012742 000352
4985 013640 005242
4986 013642 000000
4987
4988 ****
4989      THIS TEST VERIFIES MODE 7 DOUBLE OPERAND INSTRUCTIONS.
4990      THIS TEST USES THE SAME ADDRESS TABLE AND DATA TABLE USED BY
4991      THE MODE 5 TESTS. THIS TIME THE DATA IS ACCESSED USING MODE 7.
4992      R0 IS SET TO POINT TO THE MIDDLE OF THE ADDRESS TABLE IN THE MODE 5
4993      TEST. THE TABLE IS ACCESSED FROM BOTTOM TO TOP BY VARYING THE OFFSET
4994      IN THE MODE 7 INSTRUCTIONS. THE DATA RESULTS ARE IDENTICAL TO
4995      THOSE EXPECTED IN THE MODE 5 TESTS.
4996
4997 ****
4998      TEST 160      TEST MODE 7 W/ DOP INSTS.
4999 ****
5000 013644 005212
5001 013646 022712 000160
5002
5003 013652 001022
5004 013654 012700 013552
5005 013660 017037 000004 013472
5006 013666 067037 000002 013472
5007 013674 147037 000000 013472
5008 013702 157037 177776 013473
5009 013710 027037 177774 013472
5010 013716 001404
5011
5012      TST160: INC    (R2)      ;UPDATE TEST NUMBER
5013          CMP    #160, (R2)   ;SEQUENCE ERROR?
5014          BNE    TST161-10  ;BR TO ERROR HALT ON SEQ ERROR
5015          MOV    #TBL2-4, R0  ;INITIALIZE R0
5016          MOV    #4(R0), #TBL1  ;TBL1=125252
5017          ADD    #2(R0), #TBL1  ;TBL1=000377
5018          BICB   #0(R0), #TBL1  ;TBL1=000252
5019          BISB   #2(R0), #TBL1+1 ;TBL1=125252
5020          CMP    #4(R0), #TBL1  ;CHECK RESULT
5021          BEQ    TST161
5022          ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
5023          ; CONDITIONAL BRANCH INST. AND      <=====
```

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MAINDEC-11-DFKAA-8 11 34 CPJ TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 337  
DFKAA8.PII T160 TEST MODE 7 W/ DOP INSTS.

5002  
 5003  
 5004 013720 012742 000353 MOV #353,-(R2) ;REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 756 <=====  
 5005 013724 005242 INC -(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 353 \*\*\*\*\* <=====  
 5006 013726 000000 HALT ;SET MSGTYP TO FATAL ERROR  
 5007 ;RESULT OF MODE 7 INSTS INCORRECT  
 5008 ;OR SEQUENCE ERROR  
 5009 ;\*\*\*\*\*  
 5010 ; THIS TEST VERIFIES THE ROTATE MODE 0 INSTRUCTIONS.  
 5011 ;R0 IS LOADED WITH A DATA PATTERN, THE C-BIT IS LOADED, AND  
 5012 ;AN ROL INSTRUCTION IS EXECUTED WITH MODE 0. THE OPERATION IS CHECKED  
 5013 ;BY TESTING THE RESULTING DATA AND THE STATE OF THE C AND V BITS.  
 5014 ;NEXT, THE SAME PROCEDURE IS EXECUTED TO TEST MODE 0 BYTE INSTRUCTIONS.  
 5015 ;\*\*\*\*\*  
 5016 ;TEST 161 TEST ROTATE INSTRUCTIONS OF MODE 0  
 5017 ;\*\*\*\*\*  
 5018 013730 005212 TST161: INC (R2) ;UPDATE TEST NUMBER  
 5019 013732 022712 000161 CMP #161,(R2) ;SEQUENCE ERROR?  
 5020 013736 001026 BNE TST162-10 ;BR TO ERROR HALT ON SEQ ERROR  
 5021 013740 012700 125252 MOV #125252,R0 ;INITIALIZE DATA  
 5022 013744 000261 SEC ;SET C-BIT  
 5023 013746 006100 ROL R0 ;TRY ROL W/ MODE 0  
 5024 013750 102004 BVC ROTOA ;CC=0011  
 5025 013752 103003 BCC ROTOB ;CHECK DATA  
 5026 013754 022700 052525  
 5027 013760 001404 BEQ  
 5028 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 5029 ; CONDITIONAL BRANCH INST. AND  
 5030 ; REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 767 <=====  
 5031 ;<=====  
 5032 ;<=====  
 5033 013762 ROTA: MOV #354,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 354 \*\*\*\*\*  
 5034 013762 012742 000354 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 5035 013766 005242 HALT ;ROL MODE 0 FAILED  
 5036 013770 000000 ;INITIALIZE DATA  
 5037 013772 012700 ROTOB: MOV #125252,R0 ;SET C-BIT  
 5038 013776 000261 SEC ;TRY ROL W/ MODE 0 EVEN BYTE  
 5039 014000 106100 ROLB R0 ;CC=0011  
 5040 014002 102004 BVC ROTOC ;ROTAC  
 5041 014004 103003 BCC ROTOC ;CHECK DATA  
 5042 014006 022700 125125  
 5043 014012 001404 BEQ TST162 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 5044 ; CONDITIONAL BRANCH INST. AND  
 5045 ; REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 752 <=====  
 5046 ;<=====  
 5047 ;<=====  
 5048 014014 ROTOC: MOV #355,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 355 \*\*\*\*\*  
 5049 014014 012742 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 5050 014020 005242 HALT ;ROLB MODE 0 FAILED  
 5051 014022 000000 ;OR SEQUENCE ERROR  
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 5066 014024 005212  
 5067 014026 022712 000162  
 5068 014032 001051  
 5069 014034 005000  
 5070 014036 012710 052525  
 5071 014042 000241  
 5072 014044 006110  
 5073 014046 102005  
 5074 014050 103404  
 5075 014052 023727 000000 125252  
 5076 014060 001404  
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 5081 014062  
 5082 014062 012742 000356  
 5083 014066 005242  
 5084 014070 000000  
 5085 014072 000261  
 5086 014074 012710 125252  
 5087 014100 106110  
 5088 014102 102005  
 5089 014104 103004  
 5090 014106 022737 125125 000000  
 5091 014114 001404  
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 5096 014116  
 5097 014116 012742 000357  
 5098 014122 005242  
 5099 014124 000000  
 5100 014126 012710 125252  
 5101 014132 005000  
 5102 014134 005200  
 5103 014136 000261  
 5104 014140 106110  
 5105 014142 102005  
 5106 014144 103004  
 5107 014146 022737 052652 000000  
 5108 014154 001404

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;***** THIS TEST VERIFIES THE ROTATE MODE 1 INSTRUCTIONS.
;THE DATA TO BE ROTATED IS IN LOC 0. R0 IS USED AS THE
;ADDRESSING REGISTER. THE C-BIT IS LOADED AND AN ROL IS EXECUTED.
;THE RESULTS ARE CHECKED BY COMPARING THE DATA RESULTS AND TESTING
;THE C AND V BITS. THIS PROCEDURE IS THEN REPEATED TWICE MORE
;TO TEST THE BYTE ROTATES. FIRST ON BYTE 0, THEN ON BYTE 1.

;***** TEST 162 TEST ROTATE INSTRUCTIONS W/ MODE 1
;***** TST162: INC (R2) ;UPDATE TEST NUMBER
;***** CMP #162,(R2) ;SEQUENCE ERROR?
;***** BNE TST163-10 ;BR TO ERROR HALT ON SEQ ERROR
;***** CLR R0 ;POINT TO LOC. 0
;***** MOV #52525,(R0) ;INITIALIZE DATA
;***** CLC ;CLEAR C-BIT
;***** ROL (R0) ;TRY ROL W/ MODE 1
;***** BVC ROT1A ;CC=1010
;***** BCS ROT1A
;***** CMP #0, #125252 ;CHECK RESULT
;***** BEQ ROT1B ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;***** ; CONDITIONAL BRANCH INST. AND <=====
;***** ; REPLACE THE MOVE INSTRUCTION <=====
;***** ; WHICH FOLLOWS W/ 765 <=====

ROT1A:
;***** MOV #356,-(R2) ;MOVE TO MAILBOX * ***** 356 *****
;***** INC -(R2) ;SET MSGTYP TO FATAL ERROR
;***** HALT ;ROL MODE 1 FAILED

ROT1B:
;***** SEC ;INITIALIZE DATA
;***** MOV #125252,(R0) ;TRY ROLB W/ MODE 1 EVEN BYTE
;***** ROLB (R0) ;CC=1011
;***** BVC ROT1C ;BCC ROT1C
;***** BCC ROT1C
;***** CMP #125125,0#0 ;TEST RESULT
;***** BEQ ROT1D ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
;***** ; CONDITIONAL BRANCH INST. AND <=====
;***** ; REPLACE THE MOVE INSTRUCTION <=====
;***** ; WHICH FOLLOWS W/ 747 <=====

ROT1C:
;***** MOV #357,-(R2) ;MOVE TO MAILBOX * ***** 357 *****
;***** INC -(R2) ;SET MSGTYP TO FATAL ERROR
;***** HALT ;ROLB W/ MODE 1 EVEN BYTE FAILED

ROT1D:
;***** MOV #125252,(R0) ;POINT TO ODD BYTE
;***** CLR R0 ;SET C-BIT
;***** INC R0 ;TRY ROLB W/ MODE 1 ODD BYTE
;***** ROLB (R0) ;CC=0011
;***** BVC ROT1E ;BCC ROT1E
;***** BCC ROT1E
;***** CMP #052652,0#0 ;CHECK DATA
;***** BEQ TST163
  
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5109 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 5110 ; CONDITIONAL BRANCH INST. AND =====  
 5111 ; REPLACE THE MOVE INSTRUCTION =====  
 5112 ; WHICH FOLLOWS W/ 727 =====  
 5113 014156 ROTIE:  
 5114 014156 012742 000360 MOV #360,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 360 \*\*\*\*\*  
 5115 014162 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 5116 014164 000000 HALT ;ROLB W/ MODE 1 ODD BYTE FAILED  
 ; OR SEQUENCE ERROR  
 5119 ;\*\*\*\*\*  
 5121 ; THIS TEST VERIFIES MODE 2 ROTATE INSTRUCTIONS.  
 5122 ; THE SAME PROCEDURE AS IN THE OTHER ROTATE TESTS ARE USED. RO  
 5123 ; IS USED AS THE ADDRESSING REGISTER AND IS CHECKED FOR PROPER  
 5124 ; INCREMENTING. BYTE INSTRUCTIONS ARE ALSO CHECKED.  
 5126 ;\*\*\*\*\*  
 5127 ;TEST 163 TEST ROTATE INSTRUCTIONS W/ MODE 2  
 5128 ;\*\*\*\*\*  
 5129 014166 005212 TST163: INC (R2) ;UPDATE TEST NUMBER  
 5130 014170 022712 000163 CMP #163,(R2) ;SEQUENCE ERROR?  
 5131 014174 001057 BNE TST164-10 ;BR TO ERROR HALT ON SEQ ERROR  
 5132 014176 005000 CLR RO ;POINT TO LOC 0  
 5133 014200 012710 MOV #173737,(RO) ;INITIALIZE DATA  
 5134 014204 000241 CLC ;CLEAR C-BIT  
 5135 014206 006120 ROL (RO)+ ;TRY ROL W/ MODE 2  
 5136 014210 103007 BCC ROT2A ;CHECK C-BIT  
 5137 014212 022737 167676 000000 CMP #167676,0#0 ;CHECK DATA  
 5138 014220 001003 BNE ROT2A ;BRANCH IF RESULT INCORRECT  
 5139 014222 005300 DEC RO ;TEST RO  
 5140 014224 005300 DEC RO ;  
 5141 014226 001404 BEQ ROT2B ;  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 ; CONDITIONAL BRANCH INST. AND =====  
 ; REPLACE THE MOVE INSTRUCTION =====  
 ; WHICH FOLLOWS W/ 763 =====  
 5145 ;\*\*\*\*\*  
 5146 014230 ROT2A:  
 5147 014230 012742 000361 MOV #361,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 361 \*\*\*\*\*  
 5148 014234 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 5149 014236 000000 HALT ;ROL W/ MODE 2 FAILED  
 5150 014240 005000 CLR RO ;POINT TO LOC 0  
 5151 014242 012710 MOV #4040,(RO) ;INITIALIZE DATA  
 5152 014246 000241 CLC ;CLEAR C-BIT  
 5153 014250 106120 ROL (RO)+ ;TRY ROLB W/ MODE 2 EVEN BYTE  
 5154 014252 103406 BCS ROT2C ;CHECK C-BIT  
 5155 014254 022737 004100 000000 CMP #4100,0#0 ;CHECK DATA  
 5156 014262 001002 BNE ROT2C ;BRANCH IF DATA INCORRECT  
 5157 014264 005300 DEC RO ;CHECK RO  
 5158 014266 001404 BEQ ROT2D ;  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 ; CONDITIONAL BRANCH INST. AND =====  
 ; REPLACE THE MOVE INSTRUCTION =====  
 ; WHICH FOLLOWS W/ 743 =====  
 5163 014270 ROT2C:  
 5164 014270 012742 000362 MOV #362,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 362 \*\*\*\*\*

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 DFKAA8.P11 T163 TEST ROTATE INSTRUCTIONS W/ MODE 2

5165 014274 005242		INC -(R2)	SET MSGTYP TO FATAL ERROR
5166 014276 000000		HALT	;ROLB W/ MODE 2 EVEN BYTE FAILED
5167 014300 005000		ROT2D: CLR R0	;POINT TO LOC 0
5168 014302 012710	004040	MOV \$4040,(R0)	INITIALIZE DATA
5169 014306 005200		INC R0	;POINT TO ODD BYTE OF DATA
5170 014310 000261		SEC	;SET C-BIT
5171 014312 106120		ROLA (R0)+	;TRY ROL W/ MODE 2 ODD BYTE
5172 014314 103407		BCS ROT2E	;CHECK C-BIT
5173 014316 022737	010440 000000	CMP #10440,J#0	;CHECK DATA
5174 014324 001003		BNE ROT2E	;BRANCH IF DATA INCORRECT
5175 014326 005300		DEC R0	;CHECK R0
5176 014330 005300		DEC R0	
5177 014332 001404		BEQ TST164	
5178			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
5179			CONDITIONAL BRANCH INST. AND
5180			REPLACE THE MOVE INSTRUCTION
5181			WHICH FOLLOWS W/ 721
5182 014334			<=====
5183 014334 012742 000363		ROT2E: MOV #363,-(R2)	MOVE TO MAILBOX # ***** 363 *****
5184 014340 005242		INC -(R2)	;SET MSGTYP TO FATAL ERROR
5185 014342 000000		HALT	;ROLB W/ MODE 2 ODD BYTE FAILED
5186			; OR SEQUENCE ERROR

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5190      **** THIS TEST VERIFIES MODE 3 ROTATE INSTRUCTIONS.
5191      **** THIS TEST USES THE SAME PROCEDURES AS IN THE OTHER ROTATE
5192      **** TESTS. THE DATA IS STORED IN LOC. 0 AND IS ADDRESSED USING
5193      **** MODE 37. BYTE ADDRESSING IS ALSO CHECKED FOR EVEN AND ODD BYTES.
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5195      **** TEST 164 TEST ROTATE INSTRUCTIONS /W MODE 3
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5197
5198 014344 005212    000164      TST164: INC   (R2)      ; UPDATE TEST NUMBER
5199 014346 022712    000164      CMP   #164,(R2)    ; SEQUENCE ERROR?
5200 014352 001051    000000      BNE   TST165-10   ; BR TO ERROR HALT ON SEQ ERROR
5201 014354 012737    052525 000000      MOV   #52525,0#0  ; INITIALIZE DATA IN LOC 0
5202 014362 000261    000000      SEC
5203 014364 006137    000000      ROL   0#0
5204 014370 103404    000000      BCS   ROT3A
5205 014372 022737    125253 000000      CMP   #125253,0#0 ; CHECK C-BIT
5206 014400 001404    000000      BEQ   ROT3B
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5211 014402 012742    000364      ROT3A: MOV   #364,-(R2)  ; MOVE TO MAILBOX * ***** 364 *****
5212 014402 012742    000364      INC   -(R2)
5213 014406 005242    000000      HALT
5214 014410 000000    125252 000000      ROT3B: MOV   #125252,0#0  ; SET MSGTYP TO FATAL ERROR
5215 014412 012737    000000      CLC
5216 014420 000241    000000      ROLB  0#0
5217 014422 106137    000000      ROLB  0#0
5218 014426 103004    000000      BCC   ROT3C
5219 014430 023727    000000 125124 4$:   CMP   0#0, #125124 ; TRY ROL W/ MODE 3 EVEN BYTE
5220 014436 001404    000000      BEQ   ROT3D
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5225 014440 012742    000365      ROT3C: MOV   #365,-(R2)  ; MOVE TO MAILBOX * ***** 365 *****
5226 014440 012742    000365      INC   -(R2)
5227 014444 005242    000000      HALT
5228 014446 000000    125252 000000      ROT3D: MOV   #125252,0#0  ; SET MSGTYP TO FATAL ERROR
5229 014450 012737    000000      SEC
5230 014456 000261    000001      ROLB  0#1
5231 014460 106137    000001      ROLB  0#1
5232 014464 103004    000000      BCC   ROT3E
5233 014466 022737    052652 000000      CMP   #052652,0#0 ; TRY ROL W/ MODE 3 ODD BYTE
5234 014474 001404    000000      BEQ   TST165
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5239 014476 012742    000366      ROT3E: MOV   #366,-(R2)  ; MOVE TO MAILBOX * ***** 366 *****
5240 014476 012742    000366      INC   -(R2)
5241 014502 005242    000000      HALT
5242 014504 000000    **** TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
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5243 ; OR SEQUENCE ERROR  
 5244  
 5245 ;\*\*\*\*\*  
 5246 ;  
 5247 ; THIS TEST VERIFIES MODE 4 ROTATE INSTRUCTIONS. THE DATA IS  
 5248 ; STORED IN LOC. 0. R0 IS SET TO 2 AND THE CARRY IS SET. AN ROL MODE 4  
 5249 ; IS USED TO ROTATE LOCATION 0 USING R0. THE DATA IS CHECKED  
 5250 ; AND THE C AND V BITS ARE TESTED. THE PROPER DECREMENTING OF  
 5251 ; R0 IS VERIFIED.  
 5252 ;\*\*\*\*\*  
 5253 ; TEST 165 TEST MODE 4 W/ ROTATE INSTRUCTIONS  
 5254 ;\*\*\*\*\*  
 5255 TST165: INC (R2) ; UPDATE TEST NUMBER  
 5256 014506 005212 000165 CMP #165, (R2) ; SEQUENCE ERROR?  
 5257 014510 022712 000165 BNE TST166-10 ; BR TO ERROR HALT ON SEQ ERROR  
 5258 014514 001016 000000 MOV #070707, @#0 ; INITIALIZE DATA IN LOC. 0  
 5259 014516 012737 070707 000000 MOV #2, R0 ; INITIALIZE R0 AS POINTER  
 5260 014524 012700 000002 SEC ; SET C-BIT  
 5261 014530 000261 ROL -(R0) ; TRY ROL W/ MODE 4  
 5262 014532 006140 BCS ROT4 ; CHECK C-BIT  
 5263 014534 103406 CMP #161617, @#0 ; CHECK DATA  
 5264 014536 022737 161617 000000 BNE ROT4 ; BRANCH IF DATA INCORRECT  
 5265 014544 001002 TST R0 ; CHECK MODE 4 REGISTER  
 5266 014546 005700 BEQ TST166 ;  
 5267 014550 C01404 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 5268 ; CONDITIONAL BRANCH INST. AND <=====  
 5269 ; REPLACE THE MOVE INSTRUCTION <=====  
 5270 ; WHICH FOLLOWS W/ 762 <=====  
 5271 ;  
 5272 014552 ROT4: MOV #367, -(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 367 \*\*\*\*\*  
 5273 014552 012742 000367 INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 5274 014556 005242 000000 HALT ; ROL MODE 4 FAILED  
 5275 014560 000000 ; OR SEQUENCE ERROR  
 5276 ;\*\*\*\*\*  
 5277 ;  
 5278 ;  
 5279 ;  
 5280 ; THIS TEST VERIFIES MODE 5 ROTATE INSTRUCTIONS.  
 5281 ; THE DATA IS STORED IN A WORK LOCATION (ROTX) AT THE END OF THE  
 5282 ; TEST CODE. LOC. 0 IS LOADED WITH THE ADDRESS OF THE DATA (ROTX).  
 5283 ; R0 IS SET TO 2. THE CARRY IS CLEARED AND A MODE 5 ROL  
 5284 ; IS EXECUTED USING R0 AS AN ADDRESSING REGISTER. THE DATA IS  
 5285 ; CHECKED, THE C AND V BITS TESTED, AND R0 CHECKED FOR PROPER  
 5286 ; DECREMENTING.  
 5287 ;\*\*\*\*\*  
 5288 ; TEST 166 TEST MODE 5 W/ ROTATE INSTRUCTIONS  
 5289 ;\*\*\*\*\*  
 5290 TST166: INC (R2) ; UPDATE TEST NUMBER  
 5291 014562 005212 000166 CMP #166, (R2) ; SEQUENCE ERROR?  
 5292 014564 022712 000166 BNE ROT5 ; BR TO ERROR HALT ON SEQ ERROR  
 5293 014570 001021 000000 MOV #ROTX, @#0 ; MOVE POINTER TO LOC. 0  
 5294 014572 012737 014644 000000 MOV #2, R0 ; SET MODE 5 REG. TO LOC. 0  
 5295 014600 012700 000002 000000 MOV #107070, ROTX ; INITIALIZE DATA  
 5296 014604 012767 107070 000032 CLC ; CLEAR C-BIT  
 5297 014612 000241 ROL @-(R0) ; TRY ROL W/ MODE 5

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DFKAAB.P11 T166 TEST MODE 5 W/ ROTATE INSTRUCTIONS

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5299 014616 103006          BCC   ROT5      ;CHECK C-BIT
5300 014620 022737 016160 014644  CMP   #016160,&*ROTX ;CHECK DATA
5301 014626 001002          BNE   ROT5      ;BRANCH IF DATA INCORRECT
5302 014630 005700          TST   RO        ;CHECK MODE 5 REGISTER
5303 014632 001405          BEQ   TST167    ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
5304                               ; CONDITIONAL BRANCH INST. AND      <=====
5305                               ; REPLACE THE MOVE INSTRUCTION      <=====
5306                               ; WHICH FOLLOWS W/ 757      <=====

5308 014634          ROT5:    MOV   #370,-(R2) ;MOVE TO MAILBOX # ***** 370 *****
5309 014634 012742 000370    INC   -(R2)     ;SET MSGTYP TO FATAL ERROR
5310 014640 005242          HALT          ;ROL MODE 5 FAILED
5311 014642 000000          ; OR SEQUENCE ERROR

5313 014644 000000          ROTX:   0

5315                               ;*****
5316                               ;*****
5317                               ; THIS TEST VERIFIES MODE 6 ROTATE INSTRUCTIONS.
5318                               ; IT USES THE SAME PROCEDURE AS THE ABOVE TEST EXCEPT THE
5319                               ; ROTATE INSTRUCTION USES MODE 6 ADDRESSING WITH REGISTER 7.
5320                               ; THE DATA IS STILL OPERATED ON IN LOC. ROTX (SEE PREVIOUS TEST).
5321                               ;*****
5322                               ;TEST 167      TEST MODE 6 W/ ROTATE INSTRUCTIONS
5323                               ;*****
5324                               ;*****
5325 014646 005212          TST167: INC   (R2)    ;UPDATE TEST NUMBER
5326 014650 022712 000167    CMP   #167,(R2) ;SEQUENCE ERROR?
5327 014654 001013          BNE   TST170-10 ;BR TO ERROR HALT ON SEG ERROR
5328 014656 012737 125252 014644  MOV   #125252,&*ROTX ;INITIALIZE DATA
5329 014664 000261          SEC   ;SET C-BIT
5330 014666 006167 177752    ROL   ROTX      ;TRY ROL W/ MODE 6
5331 014672 103004          BCC   ROT6      ;CHECK C-BIT
5332 014674 022737 052525 014644  CMP   #52525,&*ROTX ;CHECK DATA
5333 014702 001404          BEQ   TST170    ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
5334                               ; CONDITIONAL BRANCH INST. AND      <=====
5335                               ; REPLACE THE MOVE INSTRUCTION      <=====
5336                               ; WHICH FOLLOWS W/ 765      <=====

5338 014704          ROT6:    MOV   #371,-(R2) ;MOVE TO MAILBOX # ***** 371 *****
5339 014704 012742 000371    INC   -(R2)     ;SET MSGTYP TO FATAL ERROR
5340 014710 005242          HALT          ;ROL W/ MODE 6 FAILED
5341 014712 000000          ; OR SEQUENCE ERROR
5342

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 5347 THIS TEST VERIFIES MODE 7 ROTATE INSTRUCTIONS.  
 5348 THE DATA IS SET IN LOC. ROTX (SEE PREVIOUS TEST). THE ROL INSTRUCTION  
 5349 ADDRESSES IT INDIRECTLY USING MODE 7 AND INDIRECT ADDRESS LOCATION  
 5350 (ROTXAD) FOLLOWING THE TEST CODE.  
 5351  
 5352 TEST 170 TEST MODE 7 W/ ROTATE INSTRUCTIONS  
 5353  
 5354 014714 005212 000170 TST170: INC (R2) ;UPDATE TEST NUMBER  
 5355 014716 022712 000170 CMP #170,(R2) ;SEQUENCE ERROR?  
 5356 014722 001016 BNE ROT7 ;BR TO ERROR HALT ON SEQ ERROR  
 5357 014724 012737 052525 014644 MOV #525-5, @#ROTX ;INITIALIZE DATA  
 5358 014732 012737 014644 014770 MOV @#ROT7, @#RUTXAD ;INITIALIZE ADDRESS POINTER  
 5359 014740 000241 CLC ;CLEAR C-BIT  
 5360 014742 006177 000022 ROL @ROTXAD ;TRY ROL W/ MODE 7  
 5361 014746 103404 BCS ROT7 ;CHECK C-BIT  
 5362 014750 023727 014644 125252 CMP @#ROTX, #125252 ;CHECK DATA  
 5363 014756 001405 BEQ TST171 ;  
 5364 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 5365 ; CONDITIONAL BRANCH INST. AND <=====  
 5366 ; REPLACE THE MOVE INSTRUCTION <=====  
 5367 ; WHICH FOLLOWS W/ 762 <=====  
 5368 014760 012742 000372 ROT7:  
 5369 014760 012742 000372 MOV #372,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 372 \*\*\*\*\*  
 5370 014764 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 5371 014766 000000 HALT ;ROL W/ MODE 7 FAILED  
 5372 ; OR SEQUENCE ERROR  
 5373 014770 000000 ROTXAD: 0  
 5374  
 5375  
 5376 THIS TEST VERIFIES MODE 0 SWAB INSTRUCTION. RO IS SET TO  
 5377 177400. A SWAB MODE 0 IS EXECUTED AND THE CONDITIONAL BRANCH  
 5378 IS USED TO CHECK THE SIGN OF THE RESULT. ALSO, A COMPARISON  
 5379 IS MADE TO CHECK THE DATA RESULTS.  
 5380  
 5381  
 5382 TEST 171 TEST MODE 0 W/ SWAB INST.  
 5383  
 5384  
 5385 014772 005212 000171 TST171: INC (R2) ;UPDATE TEST NUMBER  
 5386 014774 022712 000171 CMP #171,(R2) ;SEQUENCE ERROR?  
 5387 015000 001013 BNE TST172-10 ;BR TO ERROR HALT ON SEQ ERROR  
 5388 015002 012700 177400 MOV #177400,RO ;MOVE TEST PATTERN TO RO  
 5389 015006 000300 SWAB RO ;TRY SWAB MODE 0  
 5390 015010 100404 BMI S80 ;  
 5391 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 5392 ; CONDITIONAL BRANCH INST. AND <=====  
 5393 ; REPLACE THE MOVE INSTRUCTION <=====  
 5394 ; WHICH FOLLOWS W/ 774 <=====  
 5395 015012 012742 000373 MOV #373,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 373 \*\*\*\*\*  
 5396 015016 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 5397 015020 000000 HALT ;SWAB DID NOT SET CC'S CORRECT

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DFKAR-B.P11 T171 TEST MODE 0 W/ SWAB INST.

5399 015022 022700 000377	SBO: CMP BEQ	#377 R0 TST172	;CHECK RESULT
5400 015026 001404			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 765 ; (=====)
5401			
5402			
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5405 015030 012742 000374	MOV INC HALT	#374,-(R2) -(R2)	;MOVE TO MAILBOX * ***** 374 ***** ;SET MSGTYP TO FATAL ERROR ;RESULT OF SWAB MODE 0 FAILED ; OR SEQUENCE ERROR
5406 C15C34 005242			
5407 015036 000000			
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5420 015040 005212	TST172: INC	(R2)	;TEST 172 TEST MODE 1 W/ SWAB INST ;UPDATE TEST NUMBER
5421 015042 022712	CMP	#172,(R2)	;SEQUENCE ERROR?
5422 015046 001011	BNE	TST173-10	;BR TO ERROR HALT ON SEQ ERROR
5423 015050 012737	MOV	#125652,2#0	;MOVE TEST PATTERN TO LOC. 0
5424 015056 005000	CLR	R0	;R0=0
5425 015060 000310	SWAB	(R0)	;TRY SWAB MODE 1
5426 015062 022737	CMP	#125253,2#0	;CHECK RESULT
5427 015070 001404	BEQ	TST173	; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 767 ; (=====)
5428			
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5431			
5432 015072 012742	MOV	#375,-(R2)	;MOVE TO MAILBOX * ***** 375 *****
5433 015076 005242	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
5434 015100 000000	HALT		;RESULT OF SWAB MODE 1 FAILED ; OR SEQUENCE ERROR
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THIS TEST VERIFIES MODE 2 SWAB INSTRUCTION. THE TEST PATTERN IS MOVED TO LOC 0. R0 IS CLEARED AND USED AS THE MODE 2 ADDRESSING REGISTER. THE RESULTS ARE CHECKED WITH A COMPARE. R0 IS CHECKED FOR PROPER DECREMENTING.

TEST 173 TEST MODE 2 W/ SWAB INST

TST173:	INC	(R2)	UPDATE TEST NUMBER
	CMP	\$173, (R2)	SEQUENCE ERROR?
	BNE	TST174-10	BR TO ERROR HALT ON SEQ ERROR
	MOV	\$125152,000	MOVE TEST PATTERN TO LOC. 0
	CLR	R0	R0=0
	SWAB	(R0)+	TRY SWAB MODE 2
	CMP	\$65252,000	CHECK RESULT
	BEQ	S82	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND   
; REPLACE THE MOVE INSTRUCTION   
; WHICH FOLLOWS W/ 767   
; \*\*\*\* 376 \*\*\*\*

015134 012742 000376	MOV	\$376, -(R2)	MOVE TO MAILBOX # **** 376 ****
015140 005242	INC	-(R2)	SET MSGTYP TO FATAL ERROR
015142 000000	HALT		RESULT OF SWAB MODE 0 FAILED
015144 152700 000002	S82:	SUB \$2, R0	CHECK EFFECT OF REG.
015150 001404	BEQ	TST174	

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND   
; REPLACE THE MOVE INSTRUCTION   
; WHICH FOLLOWS W/ 760   
; \*\*\*\* 377 \*\*\*\*

015152 012742 000377	MOV	\$377, -(R2)	MOVE TO MAILBOX # **** 377 ****
015156 005242	INC	-(R2)	SET MSGTYP TO FATAL ERROR
015160 000000	HALT		REGISTER VALUE INCORRECT OR SEQUENCE ERROR

THIS TEST VERIFIES MODE 3 SWAB INSTRUCTION. THE TEST PATTERN IS MOVED TO LOC 0. A MODE 3 SWAB INSTRUCTION IS EXECUTED USING R7 AS THE ADDRESSING REGISTER. A COMPARE VERIFIES THE DATA RESULTS.

TEST 174 TEST MODE 3 W/SWAB INST.

TST174:	INC	(R2)	UPDATE TEST NUMBER
	CMP	\$174, (R2)	SEQUENCE ERROR?
	BNE	TST175-10	BR TO ERROR HALT ON SEQ ERROR
	MOV	\$377,000	MOVE TEST PATTERN TO LOC. 0
	SWAB	700	TRY SWAB W/ MODE 3
	CMP	\$17400,000	CHECK RESULT
	BEQ	TST175	

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DFKAA8.P11 T174 TEST MODE 3 W/SWAB INST.

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5496 015214 012742 000400  
5497 015220 005242  
5498 015222 000000  
5499

MOV \$400,-(R2)  
INC -(R2)  
HALT

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
: CONDITIONAL BRANCH INST. AND  
: REPLACE THE MOVE INSTRUCTION  
: WHICH FOLLOWS W/ 767  
: MOVE TO MAILBOX # \*\*\*\*\* 400 \*\*\*\*\*  
: SET MSGTYP TO FATAL ERROR  
: RESULT OF SWAB INCORRECT  
; OR SEQUENCE ERROR

MAINDEC-11-DFKAR-B 11:34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 348  
DFKAR-B.P11 T174 TEST MODE 3 W/SWAB INST.

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THIS TEST VERIFIES MODE 4 SWAB INSTRUCTIONS. THE DATA IS MOVED TO LOC 0. R0 IS SET TO 2 AND USED AS THE MODE 4 ADDRESSING REGISTER. THE DATA IS CHECKED WITH A COMPARE AND R0 IS CHECKED FOR PROPER DECREMENTING.

TEST 175 TEST MODE 4 W/ SWAB INST

TST175: INC (R2) ;UPDATE TEST NUMBER

CMP #175, (R2) ;SEQUENCE ERROR?

BNE TST176-10 ;BR TO ERROR HALT ON SEQ ERROR

MOV #125652, #0 ;MOVE TEST PATTERN TO LOC. 0

MOV #2, R0 ;SET UP REGISTER POINTER

SWAB -(R0) ;TRY SWAB MODE 4

CMP #125253, #0 ;CHECK RESULT

BEQ SB4 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS

CONDITIONAL BRANCH INST. AND

REPLACE THE MOVE INSTRUCTION

WHICH FOLLOWS W/ 766

&lt;=====

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&lt;=====

MOV #401, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 401 \*\*\*\*\*

INC -(R2) ;SET MSGTYP TO FATAL ERROR

HALT ;RESULT OF SWAB INCORRECT

TST R0 ;CHECK EFFECT ON REG.

BEQ TST176 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS

CONDITIONAL BRANCH INST. AND

REPLACE THE MOVE INSTRUCTION

WHICH FOLLOWS W/ 760

&lt;=====

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MOV #402, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 402 \*\*\*\*\*

INC -(R2) ;SET MSGTYP TO FATAL ERROR

HALT ;REGISTER VALUE INCORRECT

; OR SEQUENCE ERROR

MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 349  
 DFKAA8.P11 T175 TEST MODE 4 W/ SWAB INST

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5541      THIS TEST VERIFIES MODE 5 SWAB INSTRUCTION. THE TEST USES
5542      ;TWO LOCATIONS FOLLOWING THE TEST CODE. SB5X HOLDS THE DATA;
5543      ;SB5XAD IS A POINTER TO THE DATA LOCATION. THE DATA IS MOVED TO
5544      ;SB5X AND R0 IS SET TO TWO PLUS THE ADDRESS OF SB5XAD. FOLLOWING
5545      ;THE MODE 5 SWAB SB5X IS CHECKED FOR THE PROPER DATA. R0 IS
5546      ;CHECKED TO SEE THAT IT WAS DECREMENTED PROPERLY.
5547
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5549      ;TEST 176      TEST MODE 5 W/ SWAB INST.
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5551 015304 005212      TST176: INC    (R2)      ;UPDATE TEST NUMBER
5552 015306 022712      CMP     #176,(R2)   ;SEQUENCE ERROR?
5553 015312 001021      BNE     SB5      ;BR TO ERROR HALT ON SEQ ERROR
5554 015314 012700      MOV     #SB5XAD+2,R0  ;SET UP POINTER TO WORK LOCATION
5555 015320 01157       125125 000040      MOV     #125125,SB5X  ;MOVE PATTERN TO WORK LOCATION
5556 015326 000350      SWAB    @-(R0)    ;TRY SWAB MODE 5
5557 015330 022767      CMP     #52652,SB5X  ;CHECK RESULT
5558 015336 001404      BEQ     SB5A    ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
5559                               ;CONDITIONAL BRANCH INST. AND      <=====
5560                               ;REPLACE THE MOVE INSTRUCTION      <=====
5561                               ;WHICH FOLLOWS W/ 766      <=====
5562
5563 015340 012742      000403      MOV     #403,-(R2)  ;MOVE TO MAILBOX # ***** 403 *****
5564 015344 005242      INC     -(R2)    ;SET MSGTYP TO FATAL ERROR
5565 015346 000000      HALT    SB5A:    ;RESULT OF SWAB INCORRECT
5566 015350 020027      015370      CMP     R0,SB5XAD  ;CHECK RESULT OF REG.
5567 015354 001406      BEQ     TST177  ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
5568                               ;CONDITIONAL BRANCH INST. AND      <=====
5569                               ;REPLACE THE MOVE INSTRUCTION      <=====
5570                               ;WHICH FOLLOWS W/ 757      <=====
5571
5572 015356
5573 015356 012742      000404      SB5:    MOV     #404,-(R2)  ;MOVE TO MAILBOX # ***** 404 *****
5574 015362 005242      INC     -(R2)    ;SET MSGTYP TO FATAL ERROR
5575 015364 000000      HALT    SB5X:    ;REGISTER VALUE INCORRECT
5576                               ;OR SEQUENCE ERROR
5577 015366 000000      0       SB5XAD: SB5X  ;WORK LOCATION
5578 015370 015366
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5584      THIS TEST VERIFIES MODE 6 SWAB INSTRUCTION. THIS TEST
5585      USES A WORK LOCATION (SB6X) FOLLOWING THE TEST CODE. TEST DATA
5586      IS LOADED INTO THE WORK LOCATION. R0, THE ADDRESSING REGISTER
5587      IS LOADED WITH 6 LESS THAN THE ADDRESS OF THE WORK LOCATION.
5588      THE MODE 6 SWAB IS EXECUTED WITH A +6 OFFSET. THE DATA IS
5589      VERIFIED WITH A COMPARE.
5590
5591      TEST 177 TEST MODE 6 W/ SWAB INST.
5592
5593 015372 005212      TST177: INC    (R2) ;UPDATE TEST NUMBER
5594 015374 022712 000177      CMP    #177,(R2) ;SEQUENCE ERROR?
5595 015400 001013      BNE    SB6 ;BR TO ERROR HALT ON SEQ ERROR
5596 015402 012767 125125 000030      MOV    #125125,SB6X ;MOVE PATTERN TO WORK LOCATION
5597 015410 012700 015432      MOV    #SB6X-6,R0 ;MOVE OFFSET POINTER TO R0
5598 015414 000360 000006      SWAB   6(R0) ;TRY SWAB W/ MODE 6
5599 015420 022760 052652 000006      CMP    #52652,6(R0) ;CHECK RESULT
5600 015426 001405      BEQ    TST200
5601
5602
5603
5604      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
5605 015430      ; CONDITIONAL BRANCH INST. AND      <===== 
5606 015430 012742 000405      SB6:      MOV    #405,-(R2) ;MOVE TO MAILBOX * ***** 405 *****
5607 015434 005242      INC    -(R2) ;SET MSGTYP TO FATAL ERROR
5608 015436 000000      HALT   ;RESULT OF SWAB INCORRECT
5609
5610 015440 000000      SB6X:  0 ;OR SEQUENCE ERROR
5611

```

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 DFKAA8.P11 T177 TEST MODE 6 W/ SWAB INST.

```

5612
5613
5614
5615      THIS TEST VERIFIES MODE 7 SWAB INSTRUCTION. THIS TEST
5616      USES TWO LOCATIONS FOLLOWING THE TEST CODE: A WORK LOCATION
5617      (SB7X) AND A POINTER TO THE WORK LOCATION (SB7XAD). DATA IS MOVED
5618      TO THE WORK LOCATION. R0 IS LOADED WITH 72 LESS THAN THE ADDRESS
5619      OF THE ADDRESS POINTER. THE DATA IS SWAB'ED USING A MODE 7
5620      INSTRUCTION WITH AN OFFSET OF +72. THE DATA IS VERIFIED WITH A
5621      COMPARE.
5622
5623      **** TEST 200 TEST MODE 7 W/ SWAB INST. ****
5624
5625
5626 015442 005212      TST200: INC    (R2)      ;UPDATE TEST NUMBER
5627 015444 022712 000200      CMP    *200,(R2)   ;SEQUENCE ERROR?
5628 015450 001013      BNE    SB7      ;BR TO ERROR HALT ON SEQ ERROR
5629 015452 012767 177400 000030      MOV    *177400,SB7X ;MOVE PATTERN TO WORK LOCATION
5630 015460 012700 015420      MOV    *SB7XAD-72,R0 ;MOVE OFFSET POINTER TO R0
5631 015464 000370 000072      SWAB   @72(R0)   ;TRY SWAB MODE 7
5632 015470 027027 000072 000377      CMP    @72(R0),#377 ;CHECK RESULTS
5633 015476 001406      BEQ    TST201
5634
5635
5636
5637      ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====
5638 015500      SB7:      MOV    *406,-(R2)  ;CONDITIONAL BRANCH INST. AND      <=====
5639 015500 012742 000406      INC    -(R2)    ;REPLACE THE MOVE INSTRUCTION      <=====
5640 015504 005242      HALT
5641 015506 000000
5642
5643 015510 000000      SB7X:     0
5644 015512 015510      SB7XAD:  SB7X
5645

```

5646  
 5647  
 5648  
 5649 : THIS TEST VERIFIES ALL LEGAL MODES OF THE JMP INSTRUCTION.  
 5650 : BECAUSE OF THE NATURE OF THE INSTRUCTION UNDER TEST, THIS TEST  
 5651 : UTILIZES SEVERAL DIFFERENT TECHNIQUES. THE CODE IS NOT EXECUTED  
 5652 : IN A LINEAR FASHION. THE DIFFERENT MODES ARE EXECUTED IN ORDER  
 5653 : FROM 1-7. HOWEVER, THE CODE IS ARRANGED SO THAT CONTROL LEAP  
 5654 : FROGS THRU THE TEST CODE. THE ORDER OF APPEARANCE OF THE CODE  
 5655 : IS:  
 5656 : JMP MODE 1  
 5657 : JMP MODE 3  
 5658 : JMP MODE 2  
 5659 : JMP MODE 4  
 5660 : JMP MODE 6  
 5661 : JMP MODE 5  
 5662 : JMP MODE ?  
 5663 : AN INTERNAL SEQUENCE TEST (JMPSEQ) IS USED TO INSURE THAT THE  
 5664 : JUMPS ARE OCCURRING IN THE PROGRAMMED SEQUENCE.  
 5665 : THE TEST IS MADE UP OF SEVERAL BLOCKS OF CODE. EACH CODE  
 5666 : BEGINS WITH A LABEL WHICH INDICATES THE MODE BEING EXECUTED IN  
 5667 : THAT BLOCK. A SIMPLE PROCEDURE IS FOLLOWED IN EACH BLOCK. FOR  
 5668 : EXAMPLE THE CODE BEGINNING AT JMP3 WILL FIRST COMPARE THE RESULTS  
 5669 : OF THE PREVIOUS MODE 2 JUMP. (ANY REGISTER CHANGES ARE VERIFIED  
 5670 : AND THE SEQUENCE CHECK IS MADE). THEN THE REGISTERS ARE SETUP  
 5671 : FOR A MODE 3 JUMP TO THE NEXT TEST BLOCK (HERE, JMP4), THE SEQUENCE  
 5672 : CHECKER IS UPDATED AND THE JUMP IS EXECUTED.  
 5673 : IF A FAILURE OCCURS, THE SEQUENCE CHECKER WILL ASSIST IN  
 5674 : DETERMINING JUST WHICH MODE FAILED. IF THE SEQUENCE IS CORRECT  
 5675 : THEN THE ERROR DETECTED WAS A MODE FAILURE (E.G. FAILURE OF THE  
 5676 : REGISTER TO BE INCREMENTED IN MODE 2 JUMP.)  
 5677  
 5678 :\*\*\*\*\*  
 5679 :TEST 201 TEST THE JMP INSTRUCTION IN ALL MODES  
 5680 :\*\*\*\*\*  
 5681 015514 005212 :  
 5682 015516 022712 :  
 5683 015522 001150 :  
 5684 015524 005067 :  
 5685 015530 012700 :  
 5686 015534 000110 :  
 5687 015536 022700 :  
 5688 015542 001404 :  
 TST201: INC (R2) : UPDATE TEST NUMBER  
 CMP #201, (R2) : SEQUENCE ERROR?  
 BNE JMPCK+6 : BR TO ERROR HALT ON SEQ ERROR  
 CLR JMPSEQ : ESTABLISH A SEQUENCE CHECKER  
 MOV #JMP2, R0 : SET R0=JUMP TARGET  
 JMP (R0) : TRY JMP MODE 1  
 JMP3: CMP #.+2, R0 : CHECK RESULT OF MODE 2 JUMP  
 BEQ JMP3A :  
 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 : CONDITIONAL BRANCH INST. AND <=====  
 : REPLACE THE MOVE INSTRUCTION <=====  
 : WHICH FOLLOWS W/ 770 <=====  
 5689 :  
 5690 :  
 5691 :  
 5692 :  
 5693 015544 012742 :  
 5694 015550 005242 :  
 5695 015552 000000 :  
 5696 015554 026727 :  
 5697 015562 001404 :  
 MOV #407 -(R2) : MOVE TO MAILBOX \* \*\*\*\*\* 407 \*\*\*\*\*  
 INC -(R2) : SET MSGTYP TO FATAL ERROR  
 HALT : REGISTER VALUE AFTER JMP MODE 2 INCORRECT  
 JMP3A: CMP JMPSEQ, #1 : MAKE SURE JMPs ARE IN SEQUENCE: JMPSEQ=1?  
 BEQ JMP3B :  
 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 : CONDITIONAL BRANCH INST. AND <=====  
 : REPLACE THE MOVE INSTRUCTION <=====  
 : WHICH FOLLOWS W/ 760 <=====  
 5698 :  
 5699 :  
 5700 :  
 5701 :

## J10

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DFKAAB.P11 T201 TEST THE JMP INSTRUCTION IN ALL MODES

5702	015564	012742	000410		MOV	#410,-(R2)	;MOVE TO MAILBOX # ***** 410 *****
5703	015570	005242			INC	-(R2)	;SET MSGTYP TO FATAL ERROR
5704	015572	000000			HALT		;SHOULD BE HERE FROM JMP MODE 2 ONLY
5705	015574	012700	015606	JMP3B:	MOV	#IJMP4,RO	;POINT RO TO INDIRECT JMP ADDR.
5706	015600	005267	000252		INC	JMPSEQ	;UPDATE SEQUENCE CHECKER
5707	015604	000130			JMP	0(R0)+	;TRY JMP MODE 3
5708	015606	015640		IJMP4:	JMP4		;ADDRESS INDIRECT JUMP
5709							
5710	015610	005767	000242	JMP2:	TST	JMPSEQ	;CHECK THAT JMPS ARE IN SEQUENCE: JMPSEQ=0?
5711	015614	001404			BEQ	JMP2A	
5712							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 743
5713							<=====
5714							<=====
5715							<=====
5716	015616	012742	000411		MOV	#411,-(R2)	;MOVE TO MAILBOX # ***** 411 *****
5717	015622	005242			INC	-(R2)	;SET MSGTYP TO FATAL ERROR
5718	015624	000000			HALT		;SHOULD BE HERE FROM JMP MODE 1 ONLY
5719	015626	005267	000224	JMP2A:	INC	JMPSEQ	;UPDATE SEQUENCE CHECKER
5720	015632	012700	015536		MOV	#JMP3,RO	;SET RO=JUMP TARGET
5721	015636	000120			JMP	(R0)+	;TRY A JUMP MODE 2 TO "JMP3"
5722	015640	022700	015610	JMP4:	CMP	#IJMP4+2,RO	;CHECK RESULT OF REGISTER IN MODE 3 JUMP
5723	015644	001404			BEQ	JMP4A	
5724							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 727
5725							<=====
5726							<=====
5727							<=====
5728	015646	012742	000412		MOV	#412,-(R2)	;MOVE TO MAILBOX # ***** 412 *****
5729	015652	005242			INC	-(R2)	;SET MSGTYP TO FATAL ERROR
5730	015654	000000			HALT		;REGISTER VALUE AFTER MODE 3 JUMP INCORRECT
5731	015656	022767	000002	000172	JMP4A:	CMP	#2,JMPSEQ
5732	015664	001404			BEQ	JMP4B	;CHECK JUMP SEQUENCE: JMPSEQ=2?
5733							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 717
5734							<=====
5735							<=====
5736							<=====
5737	015666	012742	000413		MOV	#413,-(R2)	;MOVE TO MAILBOX # ***** 413 *****
5738	015672	005242			INC	-(R2)	;SET MSGTYP TO FATAL ERROR
5739	015674	000000			HALT		;SHOULD BE ONLY FROM MODE 3 JUMP
5740	015676	012700	015746	JMP4B:	MOV	#JMP5+2,RO	;SET UP POINTER TO JUMP TARGET
5741	015702	005267	000150		INC	JMPSEQ	;UPDATE SEQUENCE CHECKER
5742	015706	000140			JMP	-(R0)	;TRY JUMP MODE 4 TO "JMP4"
5743							
5744	015710	022767	000004	000140	JMP6:	CMP	#4,JMPSEQ
5745	015716	001404			BEQ	JMP6A	;CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=4?
5746							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 702
5747							<=====
5748							<=====
5749							<=====
5750	015720	012742	000414		MOV	#414,-(R2)	;MOVE TO MAILBOX # ***** 414 *****
5751	015724	005242			INC	-(R2)	;SET MSGTYP TO FATAL ERROR
5752	015726	000000			HALT		;SHOULD BE HERE ONLY FROM MODE 5 JUMP
5753	015730	012700	016376	JMP6A:	MOV	#JMP7+376,RO	;SET UP OFFSET POINTER TO JUMP TARGET
5754	015734	005267	000116		INC	JMPSEQ	;UPDATE JUMP SEQUENCE
5755	015740	000160	177402		JMP	-376(R0)	;TRY MODE 6 JUMP
5756							
5757	015744	022767	000003	000104	JMPS:	CMP	#3,JMPSEQ
							;CHECK THAT JUMPS ARE IN SEQUENCE: JMPSEQ=3?

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 DFKAA8.P11 T201 TEST THE JMP INSTRUCTION IN ALL MODES

5758	015752	001404		BEQ	JMP5A		
5759						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 664	<=====
5760						MOVE TO MAILBOX # ***** 415 *****	<=====
5761						SET MSGTYP TO FATAL ERROR	<=====
5762						SHOULD ONLY BE HERE FROM MODE 4 JUMP	<=====
5763	015754	012742	000415	MOV	#415 -(R2)	SET UP POINTER TO INDIRECT JUMP ADDR.	<=====
5764	015760	005242		INC	-(R2)	UPDATE JUMP SEQUENCE	<=====
5765	015762	000000		HALT		TRY JUMP MODE 5 TO "JMP6"	<=====
5766	015764	012700	016000	JMP5A:	MOV	INDIRECT ADDRESS POINTER	<=====
5767	015770	005267	000062		INC		
5768	015774	000150			JMP		
5769	015776	015710		IJMP5:	JMP6		
5770							
5771	016000	022767	000005	000050	JMP7:	CMP	; CHECK JUMPS IN SEQUENCE: JMPSEQ=5?
5772	016006	001404				BEQ	JMP7A
5773							
5774						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 646	<=====
5775						MOVE TO MAILBOX # ***** 416 *****	<=====
5776						SET MSGTYP TO FATAL ERROR	<=====
5777	016010	012742	000416	MOV	#416 -(R2)	SHOULD ONLY BE HERE FROM MODE 6 JUMP	<=====
5778	016014	005242		INC	-(R2)	SET UP OFFSET POINTER TO INDIRECT ADDR.	<=====
5779	016016	000000		HALT		UPDATE JUMP SEQUENCE	<=====
5780	016020	012700	016044	JMP7A:	MOV	TRY MODE 7 JUMP	<=====
5781	016024	005267	000026		INC	INDIRECT ADDRESS	<=====
5782	016030	000170	177770		JMP		
5783	016034	016036		IJMP:	JMPCK		
5784							
5785	016036	026727	000014	000006	JMPCK:	CMP	; CHECK JUMPS IN SEQUENCE: JMPSEQ
5786	016044	001405				BEQ	TST202
5787							
5788						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 627	<=====
5789						MOVE TO MAILBOX # ***** 417 *****	<=====
5790						SET MSGTYP TO FATAL ERROR	<=====
5791	016046	012742	000417	MOV	#417 -(R2)	SHOULD ONLY BE HERE FROM MODE 6 JUMP	<=====
5792	016052	005242		INC	-(R2)	OR SEQUENCE ERROR	<=====
5793	016054	000000		HALT			
5794							
5795	016056	000000		JMPSEQ:	0		

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5796
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5798
5799 ;*****
5800 ; THIS TEST VERIFIES ALL LEGAL MODES OF THE JSR INSTRUCTION.
5801 ; THE CONCEPT OF LEAP FROGGING AND SEQUENCE CHECKING (JSRSEQ) IS
5802 ; IDENTICAL TO THAT USED IN JMP TEST (SEE PREVIOUS TEST). EACH
5803 ; BLOCK OF CODE VERIFIES THE PREVIOUS JSR BY CHECKING THE SEQUENCE,
5804 ; CHECKING THAT THE PC WAS SAVED IN THE SPECIFIED REGISTER, CHECKING
5805 ; THAT THE SP WAS DECREMENTED, CHECKING THAT THE REGISTER WAS
5806 ; SAVED ON THE STACK, AND FINALLY CHECKING THAT ANY MODE ADDRESS
5807 ; REGISTER ALTERATIONS (E.G. INCREMENT REGISTER IN MODE 2) WERE
5808 ; SUCCESSFUL. R1 IS USED AS THE REGISTER IN ALL JSR INSTRUCTIONS.
5809 ; IF A FAILURE OCCURS, THE SEQUENCE CHECKER WILL ASSIST IN
5810 ; DETERMINING JUST WHICH MODE FAILED. IF THE SEQUENCE IS CORRECT
5811 ; THEN THE ERROR DETECTED WAS A FUNCTIONAL FAILURE (E.G., INCORRECT
5812 ; REGISTER SAVED).
5813 ;*****
5814 ;TEST 202 TEST JSR INSTRUCTION W/ ALL MODES
5815 ;*****
5816 016060 005212      000202
5817 016062 022712      000202
5818 016066 001001      000202
5819 016070 000402      000202
5820 016072 000137      016526
5821
5822 016076 012706      000500
5823 016102 012700      016210
5824 016106 005037      016506
5825 016112 005001      000202
5826 016114 005101      000202
5827 016116 004110      000202
5828
5829
5830 016120 012742      000420
5831 016124 005242      000420
5832 016126 000000      000202
5833
5834
5835 016130 022737      000001 016506
5836 016136 001014      JSR3:   CMP    #1 J# JSRSEQ
5837 016140 020127      BNE    JSR3A
5838 016144 001011      CMP    R1, #JSR4
5839 016146 022706      BNE    JSR3A
5840 016152 001006      CMP    #STBOT-2,R6
5841 016154 022716      BNE    JSR3A
5842 016160 001003      CMP    #125252, (R6)
5843 016162 022700      BNE    JSR3A
5844 016166 001404      CMP    #JSR3+2, R0
5845
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5848
5849 016170 012742      JSR3A: MOV    #421, -(R2)
5850 016170 000421      INC    -(R2)
5851 016174 005242      ;MOVE TO MAILBOX * ***** 421 *****
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MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 356  
DFKAA8.P11 T202 TEST JSR INSTRUCTION W/ ALL MODES

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MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 357  
DFKAA8.P11 T202 TEST JSR INSTRUCTION W/ ALL MODES

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5962 ****
5963 ****
5964 ****
5965 THIS TEST VERIFIES THE RTS INSTRUCTION. THE STACK POINTER
5966 IS INITIALIZED AND A TEST PATTERN STORED ON STACK. R0 IS LOADED
5967 WITH RETURN ADDRESS. AN RTS IS EXECUTED, AND, AT THE TARGET
5968 ADDRESS, A CHECK IS MADE THAT R0 WAS PROPERLY RESTORED FROM THE
5969 STACK.
5970 ****
5971 TEST 203 TEST RTS INSTRUCTION
5972 ****
5973 016536 005212 000203 TST203: INC (R2) UPDATE TEST NUMBER
5974 016540 022712 000203 CMP $203,(R2) SEQUENCE ERROR?
5975 016544 001016 BNE TST204-10 BR TO ERROR HALT ON SEQ ERROR
5976 016546 012706 000500 MOV #STBOT,R6 INITIALIZE STACK POINTER
5977 016552 012746 052525 MOV #52525,-(R6) INITIALIZE TOP OF STACK
5978 016556 012700 016574 MOV #RTS1,R0 INITIALIZE RETURN REGISTER
5979 016562 000200 RTS R0 TRY RTS THROUGH R0
5980 : TO SCOPE: REPLACE THE MOVE INSTRUCTION FOLLOWING W/ 770 (****)
5981 016564 012742 000430 MOV #430,-(R2) MOVE TO MAILBOX # ***** 430 *****
5982 016570 005242 INC -(R2) SET MSGTYP TO FATAL ERROR
5983 016572 000000 HALT RTS FAILED
5984 016574 022700 052525 RTS1: CMP #52525,R0 CHECK THAT R0 RESTORED FROM STACK
5985 016600 001404 BEQ TST204 : TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
5986 : CONDITIONAL BRANCH INST. AND (****)
5987 : REPLACE THE MOVE INSTRUCTION (****)
5988 : WHICH FOLLOWS W/ 762 (****)
5989 : MOVE TO MAILBOX # ***** 431 *****
5990 016602 012742 000431 MOV #431,-(R2)
5991 016606 005242 INC -(R2) SET MSGTYP TO FATAL ERROR
5992 016610 000000 HALT RTS MALFUNCTIONED
5993 : CR SEQUENCE ERROR

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THESE NEXT FOUR TESTS VERIFY THE FUNCTIONING OF A GROUP OF FOUR INSTRUCTIONS. THE GROUP CONSISTS OF THE INSTRUCTIONS: MOV, BIC, BIT AND BIS. THESE INSTRUCTIONS ARE SIMILAR IN THE WAY THEY EFFECT THE C AND V BITS. THEY ALL LEAVE THE V-BIT CLEAR AND THE C-BIT UNAFFECTED.

THE TEST PROCEDURE IS AS FOLLOWS: THE N, Z, AND V BITS ARE LOADED WITH THE COMPLEMENT OF THE EXPECTED RESULTS, THE C-BIT IS LOADED WITH THE DESIRED RESULT. THE INSTRUCTION IS EXECUTED WITH DIFFERENT DATA PATTERNS AND THE RESULTS ARE VERIFIED WITH A SERIES OF CONDITIONAL BRANCH INSTRUCTIONS. THE DATA IS CHOSEN TO PRODUCT ALL POSSIBLE COMBINATIONS OF THE C AND V BITS.

## TEST 204 TEST MOV INSTRUCTION

TST204: INC (R2) :UPDATE TEST NUMBER  
 CMP #204, (R2) :SEQUENCE ERROR?  
 BNE TST205-10 :BR TO ERROR HALT ON SEQ ERROR  
 SCC :CC=0110  
 +CLN!CLC  
 MOV #100000, R0 :CC=1000  
 BLOS MOVI  
 BVS MOVI  
 BMI MOV2

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 : CONDITIONAL BRANCH INST. AND  
 : REPLACE THE MOVE INSTRUCTION  
 : WHICH FOLLOWS W/ 771

MOV1:  
 MCV #432 -(R2) :MOVE TO MAILBOX # \*\*\*\*\* 432 \*\*\*\*\*  
 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 HALT :MOV DID NOT SET CC'S CORRECTLY

MOV2:  
 SCC :CC=1011  
 CLZ  
 MOV #0, R0 :CC=0101  
 BHI MOV3 :C OR Z = 0?  
 BVS MOV3 :V=1?  
 BPL TST205

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 : CONDITIONAL BRANCH INST. AND  
 : REPLACE THE MOVE INSTRUCTION  
 : WHICH FOLLOWS W/ 756

MOV3:  
 MOV #433 -(R2) :MOVE TO MAILBOX # \*\*\*\*\* 433 \*\*\*\*\*  
 INC -(R2) :SET MSGTYP TO FATAL ERROR  
 HALT :MOV DID NOT SET CC'S CORRECTLY  
 , OR SEQUENCE ERROR

## TEST 205 TEST BIT INSTRUCTION

TST205: INC (R2) :UPDATE TEST NUMBER  
 CMP #205, (R2) :SEQUENCE ERROR?  
 BNE TST206-10 :BR TO ERROR HALT ON SEQ ERROR

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DFKAA.B.P11 T205 TEST BIT INSTRUCTION

6050	016706	012700	100001		MOV #100001, R0		
6051	016712	000277			SCC		
6052	016714	000251			+CLN!CLC		
6053	016716	032700	100000		BIT #100000, R0		
6054	016722	101402			BLOS BIT1		
6055	C16724	102401			BVS BIT1		
6056	016726	100404			SMI BIT2		
6057						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
6058						CONDITIONAL BRANCH INST. AND	<=====
6059						REPLACE THE MOVE INSTRUCTION	<=====
6060						WHICH FOLLOWS W/ 767	<=====
6061	016730			BIT1:			
6062	016730	012742	000434		MOV #434, -(R2)		
6063	016734	005242			INC -(R2)		
6064	016736	000000			HALT		
6065						: MOVE TO MAILBOX # ***** 434 *****	
6066	016740	000277				: SET MSGTYP TO FATAL ERROR	
6067	016742	000244				: BIT DID NOT SET CC'S CORRECTLY	
6068	016744	032700	077776	BIT2:	SCC		
6069	016750	101002			CLZ		
6070	016752	102401			BIT	#77776, R0	
6071	016754	100004			BHI	BIT3	
6072					BVS	BIT3	
6073					BPL	TST206	
6074						: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
6075						CONDITIONAL BRANCH INST. AND	<=====
6076	016756			BIT3:			
6077	016756	012742	000435		MOV #435, -(R2)		
6078	016762	005242			INC -(R2)		
6079	016764	000000			HALT		
6080						: MOVE TO MAILBOX # ***** 435 *****	
6081						: SET MSGTYP TO FATAL ERROR	
6082						: BIT DID NOT SET CC'S CORRECTLY	
6083						: OR SEE _NCE ERROR	
6084	016766	005212				***** -***** -***** -***** -*****	
6085	016770	022712	000206			; TEST 206 TEST BIC INSTRUCTION	
6086	016774	001024				***** -***** -***** -***** -*****	
6087	016776	012700	177777			TST206: INC (R2)	
6088	017002	000277				CMP #206, (R2)	
6089	017004	000251				BNE TST207-10	
6090	017006	042700	077777			MOV #177777, R0	
6091	017012	101402				SCC	
6092	017014	102401				+CLN!CLC	
6093	017016	100404				BIC #77777, R0	
6094						CC=0110	
6095						BLOS BIC1	
6096						BVS BIC1	
6097						BMI BIC2	
6098	017020					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
6099	017020	012742	000436	BIC1:		CONDITIONAL BRANCH INST. AND	<=====
6100	017024	005242			MOV #436, -(R2)		<=====
6101	017026	000000			INC -(R2)		<=====
6102	017030	000277			HALT		
6103	017032	000244				: SET MSGTYP TO FATAL ERROR	
6104	017034	042700	100000			: BIC DID NOT SET CC'S CORRECTLY	
6105	017040	101002		BIC2:	SCC		
					CLZ		
					BIC	#100000, R0	
					BHI	BIC3	
						CC=0101	

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DFKAA8.P11 T206 TEST BIC INSTRUCTION

6106 017042 102401		BVS	BIC3		
6107 017044 100004		BPL	TST207		
6108				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	=====
6109				CONDITIONAL BRANCH INST. AND	=====
6110				REPLACE THE MOVE INSTRUCTION	=====
6111				WHICH FOLLOWS W/ 754	=====
6112 017046					
6113 017046 012742 000437		BIC3:	MOV #437 -(R2)	: MOVE TO MAILBOX # ***** 437 *****	
6114 017052 005242			INC -(R2)	: SET MSGTYP TO FATAL ERROR	
6115 017054 000000			HALT	: BIC DID NOT SET CC'S CORRECTLY	
6116				OR SEQUENCE ERROR	
6117				*****	
6118				: TEST 207 TEST BIS INSTRUCTION	
6119				*****	
6120 017056 005212	000207	TST207: INC (R2)		: UPDATE TEST NUMBER	
6121 017060 022712		CMP #207 (R2)		: SEQUENCE ERROR?	
6122 017064 001025		BNE TST210-10		: BR TO ERROR HALT ON SEQ ERROR	
6123 017066 005200		CLR R0		: R0=0	
6124 017070 000277		SCC		: CC=1010	
6125 017072 000251		+CLN!CLC			
6126 017074 052700 000000		BIS #0, R0		: CC=0100 R0=0	
6127 017100 103403		BCS BIS1			
6128 017102 102402		BVS BIS1			
6129 017104 100401		BMI BIS1			
6130 017106 001404		BEQ BIS2			
6131				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	=====
6132				CONDITIONAL BRANCH INST. AND	=====
6133				REPLACE THE MOVE INSTRUCTION	=====
6134				WHICH FOLLOWS W/ 767	=====
6135 017110		BIS1: MOV #440 -(R2)		: MOVE TO MAILBOX # ***** 440 *****	
6136 017110 012742 000440		INC -(R2)		: SET MSGTYP TO FATAL ERROR	
6137 017114 005242		HALT		: BIS DID NOT SET CC'S CORRECTLY	
6138 017116 000000		SCC		: CC=0111	
6139 017120 000277		CLN			
6140 017122 000250		BIS #177777, R0		: CC=1001	
6141 017124 052700 177777		BCC BIS3			
6142 017130 103003		BVS BIS3			
6143 017132 102402		BEQ BIS3			
6144 017134 001401		BMI TST210			
6145 017136 100404				: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	=====
6146				CONDITIONAL BRANCH INST. AND	=====
6147				REPLACE THE MOVE INSTRUCTION	=====
6148				WHICH FOLLOWS W/ 753	=====
6149					
6150 017140		BIS3: MOV #441 -(R2)		: MOVE TO MAILBOX # ***** 441 *****	
6151 017140 012742 000441		INC -(R2)		: SET MSGTYP TO FATAL ERROR	
6152 017144 005242		HALT		: BIS DID NOT SET CC'S CORRECTLY	
6153 017146 000000				OR SEQUENCE ERROR	
6154					

6155  
 6156 ;\*\*\*\*\*  
 6157 :  
 6158 : THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE INC AND  
 6159 : DEC INSTRUCTIONS. THESE INSTRUCTIONS BOTH EFFECT THE C AND V  
 6160 : BITS THE SAME; THE C-BIT IS LEFT UNCHANGED AND THE V-BIT IS DEPENDENT  
 6161 : UPON THE DATA RESULTS. THE SAME PROCEDURE IS USED. THE CONDITION  
 6162 : CODE BITS ARE INITIALIZED, THE INSTRUCTION IS EXECUTED AND THE  
 6163 : RESULTS ARE VERIFIED WITH A SERIES OF CONDITIONAL BRANCH INSTRUCTIONS.  
 6164 : THIS PROCEDURE IS REPEATED WITH SEVERAL DATA PATTERNS TO PRODUCE  
 6165 : DIFFERENT COMBINATIONS OF THE C AND V BITS.  
 6166  
 6167 ;\*\*\*\*\*  
 6168 ;TEST 210 TEST INC INSTRUCTION  
 6169 ;\*\*\*\*\*  
 6170 017150 005212 000210 TST210: INC (R2) ;UPDATE TEST NUMBER  
 6171 017152 022712 000210 CMP #210, (R2) ;SEQUENCE ERROR?  
 6172 017156 001037 077777 BNE TST211-10 ;BR TO ERROR HALT ON SEQ ERROR  
 6173 017160 012700 077777 MOV #077777, R0 ;R0=077777  
 6174 017164 000257 CCC ;CC=0100  
 6175 017166 000264 SEZ  
 6176 017170 005200 INC R0 ;CC=1010 R0=10000  
 6177 017172 101402 BLOS INC1  
 6178 017174 100001 BPL INC1  
 6179 017176 102404 BVS INC2 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 6180 ; CONDITIONAL BRANCH INST. AND  
 6181 ; REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 770 <=====  
 6182  
 6183  
 6184 017200 012742 000442 INC1:  
 6185 017200 012742 000442 MOV #442, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 442 \*\*\*\*\*  
 6186 017204 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6187 017206 000000 HALT ;INC DID NOT SET CC'S CORRECTLY  
 6188 017210 052700 077777 INC2: BIS #777777, R0 ;R0=177777  
 6189 017214 000261 SEC ;CC=1011  
 6190 017216 000244 CLZ  
 6191 017220 005200 INC R0 ;CC=0101 R0=0  
 6192 017222 100403 BMI INC3  
 6193 017224 102402 BVS INC3  
 6194 017226 103001 BCC INC3  
 6195 017230 001404 BEQ INC4 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 6196 ; CONDITIONAL BRANCH INST. AND  
 6197 ; REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 753 <=====  
 6198  
 6199  
 6200 017232 012742 000443 INC3:  
 6201 017232 012742 000443 MOV #443, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 443 \*\*\*\*\*  
 6202 017236 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6203 017240 000000 HALT ;INC DID NOT SET CC'S CORRECTLY  
 6204  
 6205 017242 000277 SCC ;CC=1110  
 6206 017244 000241 CLC  
 6207 017246 005200 INC R0 ;CC=0000 R0=1  
 6208 017250 101402 BLOS INC5  
 6209 017252 100401 BMI INC5  
 6210 017254 100004 BPL TST211

## G11

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DFKAA.B.P11 T210 TEST INC INSTRUCTION

6211 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 6212 CONDITIONAL BRANCH INST. AND =====  
 6213 REPLACE THE MOVE INSTRUCTION =====  
 6214 WHICH FOLLOWS W/ 741 =====

6215 017256 017256 012742 000444 INC5: MOV #444,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 444 \*\*\*\*\*  
 6216 017256 005242 HALT ;SET MSGTYP TO FATAL ERROR  
 6217 017262 000000 INC -(R2) ;INC DID NOT SET CC'S CORRECTLY  
 6218 017264 000000 ;OR SEQUENCE ERROR

6219  
 6220  
 6221 ;\*\*\*\*\* TEST 211 TEST DEC INSTRUCTION \*\*\*\*\*  
 6222 ;\*\*\*\*\*  
 6223 ;\*\*\*\*\*  
 6224 017266 005212 000211 TST211: INC (R2) ;UPDATE TEST NUMBER  
 6225 017270 022712 000211 CMP #211,(R2) ;SEQUENCE ERROR?  
 6226 017274 001051 BNE TST212-10 ;BR TO ERROR HALT ON SEQ ERROR  
 6227 017276 012700 000002 MOV #2,R0 ;R0=2  
 6228 017302 000277 SCC ;CC=1111  
 6229 017304 005300 DEC R0 ;CC=0001 R0=1  
 6230 017306 100403 BMI DEC1  
 6231 017310 001402 BEQ DEC1  
 6232 017312 102401 BVS DEC1  
 6233 017314 103404 BCS DEC2 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 6234 CONDITIONAL BRANCH INST. AND =====  
 6235 REPLACE THE MOVE INSTRUCTION =====  
 6236 WHICH FOLLOWS W/ 770 =====

6237  
 6238 017316 017316 012742 000445 DEC1: MOV #445,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 445 \*\*\*\*\*  
 6239 017322 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6240 017324 000000 HALT ;DEC DID NOT SET CC'S CORRECTLY  
 6241 017326 000261 SEC ;CC=1011  
 6242 017330 000244 CLZ  
 6243 017332 005300 DEC R0 ;CC=0101 R0=0  
 6244 017334 101002 BMI DEC3  
 6245 017336 100401 BVC DEC3  
 6246 017340 102004 DEC4 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 6247 CONDITIONAL BRANCH INST. AND =====  
 6248 REPLACE THE MOVE INSTRUCTION =====  
 6249 WHICH FOLLOWS W/ 756 =====

6250  
 6251  
 6252 017342 017342 012742 000446 DEC3: MOV #446,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 446 \*\*\*\*\*  
 6253 017346 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6254 017350 000000 HALT ;DEC DID NOT SET CC'S CORRECTLY  
 6255 017352 000277 SCC ;CC=0110  
 6256 +CLN!CLC  
 6257 017354 000251 DEC R0 ;CC=1000 R0=177777  
 6258 017356 005300 BLOS DEC5  
 6259 017360 101402 BVS DEC5  
 6260 017362 102401 BMI DEC6 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS =====  
 6261 017364 100404 DECS  
 6262  
 6263  
 6264  
 6265 WHICH FOLLOWS W/ 744 =====

6266 017366 DEC5:

## H11

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 DFKAAAB.P11 T211 TEST DEC INSTRUCTION

6267 017366 012742 000447		MUV #447 -(R2)	; MOVE TO MAILBOX # ***** 447 *****
6268 017372 005242		INC -(R2)	; SET MSGTYP TO FATAL ERROR
6269 017374 000000		HALT	; DEC DID NOT SET CC'S CORRECTLY
6270 017376 042700	077777	DEC6: BIC #77777, R0	; R0=100000
6271 017402 000277		SCC	; CC=0101
6272 017404 000252		+CLN!CLV	
6273 017406 005300		DEC R0	; CC=1011 R0=77777
6274 017410 100403		BMI DEC7	; CC=0011
6275 017412 001402		BEQ DEC7	
6276 017414 102001		BVC DEC7	
6277 017416 103404		BCS TST212	
6278			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 727 ; =====
6279			<=====
6280			<=====
6281			<=====
6282 017420		DEC7:	
6283 017420 012742 000450		MOV #450 -(R2)	; MOVE TO MAILBOX # ***** 450 *****
6284 017424 005242		INC -(R2)	; SET MSGTYP TO FATAL ERROR
6285 017426 000000		HALT	; DEC DID NOT SET CC'S CORRECTLY
6286			; OR SEQUENCE ERROR
6287			

6288  
 6289  
 6290  
 6291 THESE NEXT THREE TESTS VERIFY THE FUNCTIONING OF THE CLR,  
 6292 TST, AND SWAB INSTRUCTIONS. THESE THREE INSTRUCTIONS ALL LEAVE  
 6293 THE C AND V BITS CLEARED. AGAIN, THE CONDITION CODES ARE PRESET,  
 6294 THE INSTRUCTION EXECUTED AND THE RESULTS CHECKED WITH CONDITIONAL  
 6295 BRANCH INSTRUCTIONS. THE PROCEDURE IS REPEATED TO PRODUCE OTHER  
 6296 COMBINATIONS OF CONDITION CODES.  
 6297  
 6298 TEST 212 TEST CLR INSTRUCTION  
 6299  
 6300  
 6301 017430 005212 ;  
 6302 017432 022712 000212 TST212: INC (R2) ;UPDATE TEST NUMBER  
 6303 017436 001007 CMP #212,(R2) ;SEQUENCE ERROR?  
 6304 017440 000277 BNE TST213-10 ;BR TO ERROR HALT ON SEQ ERROR  
 6305 017442 000244 SCC ;CC=1011  
 6306 017444 005000 CLZ  
 6307 017446 100403 CLR RO ;CC=0100 RO=0  
 6308 017450 102402 BMI CLR1  
 6309 017452 103401 BVS CLR1  
 6310 017454 001404 BCS CLR1  
 6311 BEQ TST213 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ======  
 6312 ; CONDITIONAL BRANCH INST. AND ======  
 6313 ; REPLACE THE MOVE INSTRUCTION ======  
 6314 ; WHICH FOLLOWS W/ 771 ======  
 6315 017456 ;  
 6316 017456 012742 000451 CLR1:  
 6317 017462 005242 MOV #451,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 451 \*\*\*\*\*  
 6318 017464 000000 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6319 HALT ;CLR DID NOT SET CC'S CORRECTLY  
 6320 ; OR SEQUENCE ERROR  
 6321  
 6322 TEST 213 TEST TST INSTRUCTION  
 6323  
 6324 017466 005212 ;  
 6325 017470 022712 000213 TST213: INC (R2) ;UPDATE TEST NUMBER  
 6326 017474 001022 CMP #213,(R2) ;SEQUENCE ERROR?  
 6327 017476 000277 BNE TST214-10 ;BR TO ERROR HALT ON SEQ ERROR  
 6328 017500 000244 SCC ;CC=1011  
 6329 017502 005700 CLZ  
 6330 017504 100403 TST RO ;CC=0100  
 6331 017506 102402 BMI TEST1  
 6332 017510 103401 BVS TEST1  
 6333 017512 001404 BCS TEST1  
 6334 BEQ TEST2 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ======  
 6335 ; CONDITIONAL BRANCH INST. AND ======  
 6336 ; REPLACE THE MOVE INSTRUCTION ======  
 6337 ; WHICH FOLLOWS W/ 771 ======  
 6338 017514 ;  
 6339 017514 012742 000452 TEST1:  
 6340 017520 005242 MOV #452,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 452 \*\*\*\*\*  
 6341 017522 000000 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6342 017524 005300 HALT ;TEST DID NOT SET CC'S CORRECTLY  
 6343 017526 000277 DEC RO ;MAKE RO NEGATIVE  
 6344 SCC ;CC=0111

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DFKAAB.P11 T213 TEST TST INSTRUCTION

6344	017530	000250		CLN					
6345	017532	005700		TST	RO				
6346	017534	101402		BLOS	TEST3				
6347	017536	102401		BVS	TEST3				
6348	017540	100404		BMI	TST21 <sup>4</sup>				
6349									;CC=1000
6350									: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND
6351									REPLACE THE MOVE INSTRUCTION
6352									WHICH FOLLOWS W/ 756
6353	017542		TEST3:						=====
6354	017542	012742	000453	MOV	#453 -(R2)				=====
6355	017546	005242		INC	-(R2)				=====
6356	017550	000000		HALT					=====
6357									
6358									
6359									
6360									
6361	017552	005212		TEST3:	INC	(R2)			=====
6362	017554	022712	000214	CMP	#214, (R2)				=====
6363	017560	001023		BNE	TST215-10				=====
6364	017562	012700	170000	MOV	#170000, RO				=====
6365	017566	000277		SCC					=====
6366	017570	000250		CLN					=====
6367	017572	000300		SWAB	RO				=====
6368	017574	101402		BLOS	SWB1				=====
6369	017576	102401		BVS	SWB1				=====
6370	017600	100404		BMI	SWB2				=====
6371									
6372									
6373									
6374									
6375	017602		SWB1:						=====
6376	017602	012742	000454	MOV	#454 -(R2)				=====
6377	017606	005242		INC	-(R2)				=====
6378	017610	000000		HALT					=====
6379	017612	000277		SWB2:	SCC				=====
6380	017614	000244		CLZ					=====
6381	017616	000300		SWAB	RO				=====
6382	017620	102403		BVS	SWB3				=====
6383	017622	103402		BCS	SWB3				=====
6384	017624	100401		BMI	SWB3				=====
6385	017626	001404		BEQ	TST215				=====
6386									
6387									
6388									
6389									
6390	017630		SWB3:						=====
6391	017630	012742	000455	MOV	#455 -(R2)				=====
6392	017634	005242		INC	-(R2)				=====
6393	017636	000000		HALT					=====

=====
 ; TEST 214 TEST SWAB INSTRUCTION
 =====

=====
 ;TEST214: INC (R2)
 ;CMP #214, (R2)
 ;BNE TST215-10
 ;MOV #170000, RO
 ;SCC
 ;CLN
 ;SWAB RO
 ;BLOS SWB1
 ;BVS SWB1
 ;BMI SWB2
 =====

=====
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 770
 =====

=====
 ; SWB1: MOV #454 -(R2)
 ; INC -(R2)
 ; HALT
 =====

=====
 ; SWB2: SCC
 ; CLZ
 ; SWAB RO
 ; BVS SWB3
 ; BCS SWB3
 ; BMI SWB3
 ; BEQ TST215
 =====

=====
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 755
 =====

=====
 ; SWB3: MOV #455 -(R2)
 ; INC -(R2)
 ; HALT
 =====

K11

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DFKAAB.P11 T214 TEST SWAB INSTRUCTION

THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE ADD AND  
 ADC INSTRUCTIONS. BOTH OF THESE INSTRUCTIONS HANDLE THE C AND  
 V BITS IDENTICALLY. THE PROCEDURE IS TO PRESET THE CONDITION  
 CODES, EXECUTE THE INSTRUCTION WITH A PARTICULAR SET OF DATA, AND  
 THEN CHECK THE RESULTS BY EXECUTING A SERIES OF CONDITIONAL  
 BRANCHES. THIS PROCEDURE IS REPEATED SEVERAL TIMES WITH DIFFERENT  
 DATA TO PRODUCE EVERY COMBINATION OF C AND V BITS.

TEST 215 TEST ADD INSTRUCTION

6408	017640	005212		TST215: INC (R2)	; UPDATE TEST NUMBER
6409	017642	022712	000215	CMP #215, (R2)	; SEQUENCE ERROR?
6410	017646	001062		BNE TST216-10	; BR TO ERROR HALT ON SEQ ERROR
6411	017650	012700	040000	MOV #40000, R0	; R0=40000
6412	017654	000277		SCC	; CC=1111
6413	017656	062700	030000	ADD #30000, R0	; CC=0000 R0=70000
6414	017662	101402		BLOS ADD1	
6415	017664	102401		BVS ADD1	
6416	017666	100004		BPL ADD2	
6417					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS 6418
6419					CONDITIONAL BRANCH INST. AND 6420
6421	017670				REPLACE THE MOVE INSTRUCTION 6422
6423	017670	012742	000456	ADD1: MOV #456, -(R2)	WHICH FOLLOWS W/ 770 <=====
6424	017674	005242		INC -(R2)	; MOVE TO MAILBOX # ***** 456 *****
6425	017676	000000		HALT	; SET MSGTYP TO FATAL ERROR
6426	017700	000264		ADD2: SEZ	; ADD DID NOT SET CC'S CORRECTLY
6427	017702	062700	010000	ADD ADD3	; CC=0100
6428	017706	101402		BLOS ADD3	
6429	017710	102001		BVC ADD3	
6430	017712	100404		BMI ADD4	
6431					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS 6432
6433					CONDITIONAL BRANCH INST. AND 6434
6435	017714				REPLACE THE MOVE INSTRUCTION 6436
6437	017714	012742	000457	ADD3: MOV #457, -(R2)	WHICH FOLLOWS W/ 756 <=====
6438	017720	005242		INC -(R2)	; MOVE TO MAILBOX # ***** 457 *****
6439	017722	000000		HALT	; SET MSGTYP TO FATAL ERROR
6440	017724	000257		ADD4: CCC	; ADD DID NOT SET CC'S CORRECTLY
6441	017726	000270		SEN	; CC=1000
6442	017730	062700	100000	ADD ADD5	
6443	017734	101002		BHI ADD5	
6444	017736	102001		BVC ADD5	
6445	017740	100004		BPL ADD6	
6446					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS 6447
6448					CONDITIONAL BRANCH INST. AND 6449
6449	017742			ADD5:	REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 743 <=====

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DFKAAB.P11 T215 TEST ADD INSTRUCTION

6450	017742	012742	000460		MUV	#460 -(R2)	; MOVE TO MAILBOX # ***** 460 *****	
6451	017746	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
6452	017750	000000			HALT		; ADD DID NOT SET CC'S CORRECTLY	
6453	017752	062700	177777	ADD6:	ADD	#177777, R0	; CC=1000 R0=177777	
6454	017756	101402			BLOS	ADD7		
6455	017760	102401			BVS	ADD7		
6456	017762	100404			BMI	ADD8		
6457							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
6458							CONDITIONAL BRANCH INST. AND	(*****)
6459							REPLACE THE MOVE INSTRUCTION	(*****)
6460							WHICH FOLLOWS W/ 732	(*****)
6461	017764			ADD7:	MOV	#461 -(R2)	; MOVE TO MAILBOX # ***** 461 *****	
6462	017764	012742	000461		INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
6463	017770	005242			HALT		; ADD DID NOT SET CC'S CORRECTLY	
6464	017772	000000			SCC		; CC=1010	
6465	017774	000277			+CLC:CLZ			
6466	017776	000245			ADD	#1, R0	; CC=0101 R=0	
6467	020000	062700	000001		BVS	ADD9		
6468	020004	102403			BCC	ADD9		
6469	020006	103002			BMI	ADD9		
6470	020010	100401			BEQ	TST216		
6471	020012	001404					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
6472							CONDITIONAL BRANCH INST. AND	(*****)
6473							REPLACE THE MOVE INSTRUCTION	(*****)
6474							WHICH FOLLOWS W/ 716	(*****)
6475				ADD9:	MOV	#462 -(R2)	; MOVE TO MAILBOX # ***** 462 *****	
6476	020014	012742	000462		INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
6477	020014	005242			HALT		; ADD DID NOT SET CC'S CORRECTLY	
6478	020020	000000					; OR SEQUENCE ERROR	
6479	020022							
6480								
6481								
6482								
6483								
6484								
6485	020024	005212		TST216:	INC	(R2)	; UPDATE TEST NUMBER	
6486	020026	022712	000216		CMP	#216 (R2)	; SEQUENCE ERROR?	
6487	020032	001037			BNE	TST217-10	; BR TO ERROR HALT ON SEQ ERROR	
6488	020034	012700	077777		MOV	#077777, R0		
6489	020040	000277			SCC		; CC=0101	
6490	020042	000252			+CLN!CLV			
6491	020044	005500			ADC	R0	; CC=1010	
6492	020046	101402			BLOS	ADC1		
6493	020050	102001			BVC	ADC1		
6494	020052	100404			BMI	ADC2		
6495							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(*****)
6496							CONDITIONAL BRANCH INST. AND	(*****)
6497							REPLACE THE MOVE INSTRUCTION	(*****)
6498							WHICH FOLLOWS W/ 770	(*****)
6499	020054	012742	000463	ADC1:	MOV	#463 -(R2)	; MOVE TO MAILBOX # ***** 463 *****	
6500	020054	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
6501	020060	000000			HALT		; ADC DID NOT SET CC'S CORRECTLY	
6502	020062	052700	077777	ADC2:	BIS	#77777, R0		
6503	020064				SCC			
6504	020070	000277			CLZ			
6505	020072	000244						

## MII

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 DFKAA8.P11 T216 TEST ADC INSTRUCTION

6506 020074 005500	AUC	RO	;CC=0101 RO=0
6507 020076 101002	BHI	ADC3	
6508 020100 102401	BVS	ADC3	
6509 020102 100004	BPL	ADC4	
6510			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
6511			CONDITIONAL BRANCH INST. AND <=====
6512			REPLACE THE MOVE INSTRUCTION <=====
6513			WHICH FOLLOWS W/ 754 <=====
6514 020104	ADC3:		
6515 020104 012742 000464	MOV	#464 -(R2)	;MOVE TO MAILBOX # ***** 464 *****
6516 020110 005242	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
6517 020112 000000	HALT		;ADC DID NOT SET CC'S CORRECTLY
6518 020114 000277	SCC		
6519 020116 000245	+CLZ!CLC		
6520 020120 005500	ADC	RD	;CC=0100
6521 020122 102403	BVS	ADC5	
6522 020124 103402	BCS	ADC5	
6523 020126 100401	BMI	ADC5	
6524 020130 001404	BEQ	TST217	
6525			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
6526			CONDITIONAL BRANCH INST. AND <=====
6527			REPLACE THE MOVE INSTRUCTION <=====
6528			WHICH FOLLOWS W/ 741 <=====
6529 020132	ADC5:		
6530 020132 012742 000465	MOV	#465 -(R2)	;MOVE TO MAILBOX # ***** 465 *****
6531 020136 005242	INC	-(R2)	;SET MSGTYP TO FATAL ERROR
6532 020140 000000	HALT		;ADC DID NOT SET CC'S CORRECTLY
6533			; OR SEQUENCE ERROR

6534  
 6535  
 6536  
 6537  
 6538      THESE NEXT THREE TESTS VERIFY THE FUNCTIONING OF THE NEG,  
 6539      CMP, AND COM INSTRUCTIONS. EACH OF THESE INSTRUCTIONS GENERATE  
 6540      THE C AND V BITS IDENTICALLY. THE CONDITION CODES ARE PRESET  
 6541      THE INSTRUCTIONS EXECUTED, AND THE RESULTS CHECKED WITH A SERIES  
 6542      OF CONDITIONAL BRANCH INSTRUCTIONS. THIS PROCEDURE IS REPEATED  
 6543      SEVERAL TIMES WITH DIFFERENT DATA IN ORDER TO GENERATE DIFFERENT  
 6544      COMBINATIONS OF THE C AND V BITS.  
 6545  
 6546  
 6547      \*\*\*\* TEST 217 TEST NEG INSTRUCTION \*\*\*\*  
 6548 020142 005212      TST217: INC (R2) ;UPDATE TEST NUMBER  
 6549 020144 022712 000217      CMP #217, (R2) ;SEQUENCE ERROR?  
 6550 020150 001042      BNE TST220-10 ;BR TO ERROR HALT ON SEQ ERROR  
 6551 020152 012700 000001      MOV #1, R0 ;CC=0110  
 6552 020156 000277      SCC +CLN!CLC  
 6553 020160 000251      NEG RO ;CC=1001    RO=177777  
 6554 020162 005400      BCC NEG1  
 6555 020164 103003      BVS NEG1  
 6556 020166 102402      BEQ NEG1  
 6557 020170 001401      BMI NEG2  
 6558 020172 100404  
 6559  
 6560  
 6561      TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====  
 6562      CONDITIONAL BRANCH INST. AND      <=====  
 6563 020174      REPLACE THE MOVE INSTRUCTION      <=====  
 6564 020174 012742 000466      NEG1: MOV #466, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 466 \*\*\*\*\*  
 6565 020200 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6566 020202 000000      HALT ;NEG DID NOT SET CC'S CORRECTLY  
 6567 020204 042700 077777      NEG2: BIC #77777, RO ;CC=0100  
 6568 020210 000257      CCC  
 6569 020212 000264      SEZ  
 6570 020214 005400      NEG RO ;CC=1011    RO=100000  
 6571 020216 102003      BVC NEG3  
 6572 020220 103002      BCC NEG3  
 6573 020222 001401      BEQ NEG3  
 6574 020224 100404      BMI NEG4  
 6575  
 6576  
 6577      TO SCOPE: CLEAR THE RIGHT BYTE OF THIS      <=====  
 6578      CONDITIONAL BRANCH INST. AND      <=====  
 6579 020226      REPLACE THE MOVE INSTRUCTION      <=====  
 6580 020226 012742 000467      NEG3: MOV #467, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 467 \*\*\*\*\*  
 6581 020232 005242      INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6582 020234 000000      HALT ;NEG DID NOT SET CC'S CORRECTLY  
 6583 020236 005000      CLR RO  
 6584 020240 000277      SCC  
 6585 020242 000244      CLZ  
 6586 020244 005400      NEG RO ;CC=0100    RO=0  
 6587 020246 102403      BVS NEG5  
 6588 020250 103402      BCS NEG5  
 6589 020252 001001      BNE NEG5

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DFKAA8.P11 T217 TEST NEG INSTRUCTION

6590	020254	100004	BPL	TST220	
6591					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS 6592
6593					CONDITIONAL BRANCH INST. AND 6594
6595	020256	012742	NEGS:	MOV	REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 736
6596	020256	000470		INC	(=====)
6597	020262	005242		HALT	(=====)
6598	020264	000000			(=====)
6599					(=====)
6600					
6601					*****
6602					TEST 220 TEST CMP INSTRUCTION
6603					*****
6604	020266	005212		TST220: INC	*****
6605	020270	022712	000220	CMP	:UPDATE TEST NUMBER
6606	020274	001060		BNE	:SEQUENCE ERROR?
6607	020276	012700	000005	MOV	:BR TO ERROR HALT ON SEQ ERROR
6608	020302	000257		CCC	;CC=1010
6609	020304	000271		+SEN!SEC	
6610	020306	022700	000005	CMP	;CC=0101
6611	020312	101002		BHI	
6612	020314	102401		BVS	
6613	020316	100004		BPL	
6614					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
6615					CONDITIONAL BRANCH INST. AND
6616					REPLACE THE MOVE INSTRUCTION
6617					WHICH FOLLOWS W/ 767
6618	020320	012742	000471	CMP1:	(=====)
6619	020320	012742	000471	MOV	MOVE TO MAILBOX # ***** 471 *****
6620	020324	005242		INC	:SET MSGTYP TO FATAL ERROR
6621	020326	000000		HALT	:CMP DID NOT SET CC'S CORRECTLY
6622	020330	012700	100000	MOV	
6623	020334	000277		SCC	;CC=1101
6624	020336	000242		CLV	
6625	020340	020027	077777	CMP	;CC=0010
6626	020344	101402		BLOS	
6627	020346	102001		CMP3	
6628	020350	100004		BVC	
6629				BPL	
6630					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
6631					CONDITIONAL BRANCH INST. AND
6632					REPLACE THE MOVE INSTRUCTION
6633					WHICH FOLLOWS W/ 752
6634	020352	012742	000472	CMP3:	(=====)
6635	020356	005242		MOV	MOVE TO MAILBOX # ***** 472 *****
6636	020360	000000		INC	:SET MSGTYP TO FATAL ERROR
6637	020362	052700	040000	HALT	:CMP DID NOT SET CC'S CORRECTLY
6638	020366	000257		BIS	;R0=140000
6639	020370	000264		CCC	;CC=0100
6640	020372	022700	040000	SEZ	
6641	020376	102003		CMP	;CC=1011
6642	020400	103002		BVC	
6643	020402	001401		BCC	
6644	020404	10C404		BEQ	
6645				BMI	
					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS

6646  
 6647  
 6648  
 6649 020406 012742 000473 : CMP5:  
 6650 020406 005242 000000 MOV \$473,-(R2)  
 6651 020412 005242 HALT -(R2)  
 6652 020414 000000 BIC \$40000, R0  
 6653 020416 042700 040000 SCC  
 6654 020422 000277 CMP \$-1, R0  
 6655 020424 022700 177777 BLOS  
 6656 020430 101402 CMP7  
 6657 020432 102401 BVS  
 6658 020434 100004 BPL TST221  
 6659  
 6660  
 6661  
 6662  
 6663 020436 012742 000474 : CMP7:  
 6664 020436 012742 000474 MOV \$474,-(R2)  
 6665 020442 005242 INC -(R2)  
 6666 020444 000000 HALT  
 6667  
 6668  
 6669  
 6670 : TEST 221 TEST COM INSTRUCTION  
 6671 :  
 6672 020446 005212 000221 TST221: INC (R2)  
 6673 020450 022712 000221 CMP \$221, (R2)  
 6674 020454 001010 BNE TST222-10  
 6675 020456 012700 177777 MOV \$-1, R0  
 6676 020462 000257 CCC  
 6677 020464 000265 +SEC!SEZ  
 6678 020466 005100 COM RO  
 6679 020470 101002 BHI COM1  
 6680 020472 102401 BVS COM1  
 6681 020474 100004 BPL TST222  
 6682  
 6683  
 6684  
 6685  
 6686 020476 C12742 000475 : COM1:  
 6687 020476 C12742 000475 MOV \$475,-(R2)  
 6688 020502 005242 INC -(R2)  
 6689 020504 000000 HALT  
 6690  
 6691

; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 734 <=====  
 ; MOVE TO MAILBOX # \*\*\*\*\* 473 \*\*\*\*\*  
 ; SET MSGTYP TO FATAL ERROR  
 ; CMP DID NOT SET CC'S CORRECTLY  
 ; CC=1111  
 ; CC=0000  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 720 <=====  
 ; MOVE TO MAILBOX # \*\*\*\*\* 474 \*\*\*\*\*  
 ; SET MSGTYP TO FATAL ERROR  
 ; CMP DID NOT SET CC'S CORRECTLY  
 ; OR SEQUENCE ERROR  
 ;\*\*\*\*\*  
 ; TEST 221 TEST COM INSTRUCTION  
 ;\*\*\*\*\*  
 ; UPDATE TEST NUMBER  
 ; SEQUENCE ERROR?  
 ; BR TO ERROR HALT ON SEQ ERROR  
 ; CC=1010  
 ; CC=0101  
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ; CONDITIONAL BRANCH INST. AND  
 ; REPLACE THE MOVE INSTRUCTION  
 ; WHICH FOLLOWS W/ 770 <=====  
 ; MOVE TO MAILBOX # \*\*\*\*\* 475 \*\*\*\*\*  
 ; SET MSGTYP TO FATAL ERROR  
 ; COM DID NOT SET CC'S CORRECTLY  
 ; OR SEQUENCE ERROR

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THESE NEXT TWO TESTS VERIFY THE FUNCTIONING OF THE SUB AND SBC INSTRUCTIONS. BOTH OF THESE INSTRUCTIONS HANDLE THE C AND V BITS IDENTICALLY. THE PROCEDURE IS TO PRESET THE CONDITION CODES, EXECUTE THE INSTRUCTION WITH A PARTICULAR SET OF DATA, AND THEN CHECK THE RESULTS BY EXECUTING A SERIES OF CONDITIONAL BRANCHES. THIS PROCEDURE IS REPEATED SEVERAL TIMES WITH DIFFERENT DATA PATTERNS TO PROVIDE EVERY COMBINATION OF THE C AND V BITS.

## TEST 222 TEST SUB INSTRUCTION

```

TST222: INC    (R2)      ;UPDATE TEST NUMBER
          CMP    #222, (R2)   ;SEQUENCE ERROR?
          BNE    TST223-10   ;BR TO ERROR HALT ON SEQ ERROR
          MOV    #125252, R0
          CCC
          +SEN!SEC
          SUB    #125252, R0
          BHI    SUB1
          BVS    SUB1
          BPL    SUB2

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 767

## SUB1:

```

          MOV    #476, -(R2)  ;MOVE TO MAILBOX * ***** 476 *****
          INC    -(R2)        ;SET MSGTYP TO FATAL ERROR
          HALT
          SUB2: BIS    #100000, R0  ;SUB DID NOT SET CC'S CORRECTLY
          SCC
          CLV
          SUB   #77777, R0
          BLOS
          SUB3
          BVC
          BPL   SUB4

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 752

## SUB3:

```

          MOV    #477, -(R2)  ;MOVE TO MAILBOX * ***** 477 *****
          INC    -(R2)        ;SET MSGTYP TO FATAL ERROR
          HALT

```

## SUB4:

```

          COM    R0
          SCC
          SUB   #100000, R0
          BLOS
          SUB5
          BVS
          BPL   SUB6

```

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND

6748  
 6749  
 6750 020620 012742 000500 ; REPLACE THE MOVE INSTRUCTION (=====)  
 6751 020620 005242 000500 ; WHICH FOLLOWS W/ 737 (=====)  
 6752 020624 005242  
 6753 020626 000000  
 6754 020630 000257  
 6755 020632 000264  
 6756 020634 162700 140000 ; MOVE TO MAILBOX # \*\*\*\*\* 500 \*\*\*\*\*  
 6757 020640 102003 ; SET MSGTYP TO FATAL ERROR  
 6758 020642 103002 ; SUB DID NOT SET CC'S CORRECTLY  
 6759 020644 001401 ; CC=0100  
 6760 020646 100404 ;  
 6761  
 6762  
 6763  
 6764 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====)  
 6765 020650 012742 000501 ; CONDITIONAL BRANCH INST. AND (=====)  
 6766 020650 012742 000501 ; REPLACE THE MOVE INSTRUCTION (=====)  
 6767 020654 005242 ; WHICH FOLLOWS W/ 723 (=====)  
 6768 020656 000000 ;  
 6769  
 6770 ;\*\*\*\*\*  
 6771 ;TEST 223 TEST SBC INSTRUCTION  
 6772 ;\*\*\*\*\*  
 6773 020660 005212 000223 ;\*\*\*\*\*  
 6774 020662 022712 000223 ;\*\*\*\*\*  
 6775 020666 001053 000001 ;\*\*\*\*\*  
 6776 020670 012700 000001 ;\*\*\*\*\*  
 6777 020674 000277 ;\*\*\*\*\*  
 6778 020676 000244 ;\*\*\*\*\*  
 6779 020700 005600 ;\*\*\*\*\*  
 6780 020702 103403 ;\*\*\*\*\*  
 6781 020704 102402 ;\*\*\*\*\*  
 6782 020706 100401 ;\*\*\*\*\*  
 6783 020710 001404 ;\*\*\*\*\*  
 6784 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====)  
 6785 ; CONDITIONAL BRANCH INST. AND (=====)  
 6786 ; REPLACE THE MOVE INSTRUCTION (=====)  
 6787 ; WHICH FOLLOWS W/ 767 (=====)  
 6788 020712 012742 000502 ;  
 6789 020712 012742 000502 ; SBC1: MOVE TO MAILBOX # \*\*\*\*\* 502 \*\*\*\*\*  
 6790 020716 005242 ; SET MSGTYP TO FATAL ERROR  
 6791 020720 000000 ; SBC DID NOT SET CC'S CORRECTLY  
 6792 020722 000277 ; CC=1010  
 6793 020724 000245 ;  
 6794 020726 005600 ;+CLZ!CLC  
 6795 020730 103403 ; SBC R0  
 6796 020732 102402 ; BCS SBC3  
 6797 020734 100401 ; BVS SBC3  
 6798 020736 001404 ; BMI SBC3  
 6799 ; BEQ SBC4 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====)  
 6800 ; CONDITIONAL BRANCH INST. AND (=====)  
 6801 ; REPLACE THE MOVE INSTRUCTION (=====)  
 6802 ; WHICH FOLLOWS W/ 754 (=====)  
 6803 020740 ; SBC3:

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DFKAA8.P11 T223 TEST SBC INSTRUCTION

6839 ;\*\*\*\*\*  
 6840 ;\*\*\*\*\*  
 6841 ;\*\*\*\*\* THESE NEXT FOUR TESTS VERIFY THE FUNCTIONING OF THE ROL,  
 6842 ;ROR, ASL AND ASR INSTRUCTIONS. SPECIAL DATA PATTERNS ARE LOADED  
 6843 ;AND ROTATED SEVERAL TIMES FOR EACH TEST. THE CONDITION CODES  
 6844 ;ARE PRESET BEFORE EACH ROTATION AND THE CONDITION CODES ARE  
 6845 ;CHECKED AFTER EACH ROTATION. THE FINAL CHECK IN EACH TEST IS  
 6846 ;TO VERIFY THE COMMULATIVE DATA RESULT. THE DATA PATTERNS HAVE  
 6847 ;BEEN SELECTED TO PRODUCE ALL COMBINATIONS OF THE C AND V BITS.  
 6848 ;\*\*\*\*\*  
 6849 ;\*\*\*\*\*  
 6850 ;TEST 224 TEST ROL INSTRUCTION  
 6851 ;\*\*\*\*\*  
 6852 021026 005212 000224 ;ST224: INC (R2) ;UPDATE TEST NUMBER  
 6853 021030 022712 000224 CMP #224, (R2) ;SEQUENCE ERROR?  
 6854 021034 001053 144000 BNE TST225-10 ;BR TO ERROR HALT ON SEQ ERROR  
 6855 021036 012700 144000 MOV #144000, R0 ;R0=144000  
 6856 021042 000257 CCC ;CC=0110  
 6857 021044 000266 +SEZ!SEV  
 6858 021046 006100 ROL R0 ;CC=1001 R0=110000  
 6859 021050 103003 BCC ROL1  
 6860 021052 102402 BVS ROL1  
 6861 021054 001401 BEQ ROL1  
 6862 021056 100404 BMI ROL2  
 6863 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 6864 ; CONDITIONAL BRANCH INST. AND <=====  
 6865 ; REPLACE THE MOVE INSTRUCTION <=====  
 6866 ; WHICH FOLLOWS W/ 767 <=====  
 6867 021060 012742 000506 ROL1:  
 6868 021060 012742 000506 MOV #506,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 506 \*\*\*\*\*  
 6869 021064 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 6870 021066 000000 HALT  
 6871 021070 000277 SCC ;CC=1100  
 6872 021072 000243 +CLV!CLC  
 6873 021074 006100 ROL R0 ;CC=0011 R0=020000  
 6874 021076 103003 BCC ROL3  
 6875 021100 102002 BVC ROL3  
 6876 021102 001401 BEQ ROL3  
 6877 021104 100004 BPL ROL4  
 6878 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 6879 ; CONDITIONAL BRANCH INST. AND <=====  
 6880 ; REPLACE THE MOVE INSTRUCTION <=====  
 6881 ; WHICH FOLLOWS W/ 754 <=====  
 6882 021106 012742 000507 ROL3:  
 6883 021106 012742 000507 MOV #507,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 507 \*\*\*\*\*  
 6884 021112 005242 INC -(R2) ;SET MSGTYP T) FATAL ERROR  
 6885 021114 000000 HALT ;ROL DID NOT SET CC'S CORRECTLY  
 6886 021116 000277 SCC ;CC=0111  
 6887 021120 000250 CLN  
 6888 021122 006100 ROL R0 ;CC=0000 R0=040001  
 6889 021124 101402 BLOS ROL5  
 6890 021126 102401 BVS ROL5  
 6891 021130 100004 BPL ROL6  
 6892 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====  
 6893 ; CONDITIONAL BRANCH INST. AND <=====  
 6894 ; REPLACE THE MOVE INSTRUCTION <=====

6895  
 6896 021132 012742 000510 ROL5: ; WHICH FOLLOWS W/ 742   
 6897 021132 005242 INC \*510,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 510 \*\*\*\*\*  
 6898 021136 005242 HALT ;SET MSGTYP TO FATAL ERROR  
 6899 021140 000000 CCC ;ROL DID NOT SET CC'S CORRECTLY  
 6900 021142 000257 CC=0101  
 6901 021144 000265 +SEZ!SEC  
 6902 021146 006100 ROL RO ;CC=1010 RO=100003  
 6903 021150 101405 BLOS ROL7  
 6904 021152 102004 BVC ROL7  
 6905 021154 100003 BPL ROL7  
 6906 021156 022700 100003 CMP #100003,RO  
 6907 021162 001404 BEQ TST225 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 6908 ; CONDITIONAL BRANCH INST. AND   
 6909 ; REPLACE THE MOVE INSTRUCTION   
 6910 ; WHICH FOLLOWS W/ 725   
 6911 ;  
 6912 021164 012742 000511 ROL7: ; MOVE TO MAILBOX \* \*\*\*\*\* 511 \*\*\*\*\*  
 6913 021164 012742 INC \*511,-(R2) ;SET MSGTYP TO FATAL ERROR  
 6914 021170 005242 HALT ;ROL MALFUNCTIONED  
 6915 021172 000000 ; OR SEQUENCE ERROR  
 6916 ;\*\*\*\*\*  
 6917 ;TEST 225 TEST ROR INSTRUCTION  
 6918 ;\*\*\*\*\*  
 6919 ;\*\*\*\*\*  
 6920 021174 005212 000225 TST225: INC (R2) ;UPDATE TEST NUMBER  
 6921 021176 022712 000225 CMP #225,(R2) ;SEQUENCE ERROR?  
 6922 021202 001051 BNE TST226-10 ;BR TO ERROR HALT ON SEQ ERROR  
 6923 021204 012700 MOV #23,RO ;RO=23  
 6924 021210 000277 SCC ;CC=0111  
 6925 021212 000250 CLN  
 6926 021214 006000 ROR RO ;CC=1001 RO=100011  
 6927 021216 102403 BVS ROR1  
 6928 021220 103002 BCC ROR1  
 6929 021222 001401 BEQ ROR1  
 6930 021224 100404 BMI ROR2 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 6931 ; CONDITIONAL BRANCH INST. AND   
 6932 ; REPLACE THE MOVE INSTRUCTION   
 6933 ; WHICH FOLLOWS W/ 767   
 6934 ;  
 6935 021226 012742 000512 ROR1: ; MOVE TO MAILBOX \* \*\*\*\*\* 512 \*\*\*\*\*  
 6936 021226 012742 INC \*512,-(R2) ;SET MSGTYP TO FATAL ERROR  
 6937 021232 005242 HALT ;ROR DID NOT SET CC'S CORRECTLY  
 6938 021234 000000 CCC ;CC=1100  
 6939 021236 000257 +SEN!SEZ  
 6940 021240 000274 ROR RO ;CC=0011 RO=040004  
 6941 021242 006000 BVC ROR3  
 6942 021244 102003 BCC ROR3  
 6943 021246 103002 BEQ ROR3  
 6944 021250 001401 BPL ROR4 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 6945 021252 100004 ; CONDITIONAL BRANCH INST. AND   
 6946 ; REPLACE THE MOVE INSTRUCTION   
 6947 ; WHICH FOLLOWS W/ 754   
 6948 ;  
 6949 ;  
 6950 021254 ROR3:

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 DFKAA8.P11 T225 TEST ROR INSTRUCTION

6951	021254	012742	000513		MUV	#513,-(R2)	; MOVE TO MAILBOX # ***** 513 *****	
6952	021260	005242		ROR4:	INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
6953	021262	000000			HALT		; ROR DID NOT SET CC'S CORRECTLY	
6954	021264	000277			SCC		; CC=1110	
6955	021266	000241			CLC			
6956	021270	006000			ROR	RO	; CC=0000 RO=020002	
6957	021272	101403			BLOS	R0RS		
6958	021274	102402			BVS	R0RS		
6959	021276	001401			BEQ	R0RS		
6960	021300	100004			BPL	R0R6		
6961							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
6962							CONDITIONAL BRANCH INST. AND	<=====
6963							REPLACE THE MOVE INSTRUCTION	<=====
6964							WHICH FOLLOWS W/ 741	<=====
6965	021302			R0R5:	MOV	#514,-(R2)	; MOVE TO MAILBOX # ***** 514 *****	
6966	021302	012742	000514		INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
6967	021306	005242			HALT		; ROR DID NOT SET CC'S CORRECTLY	
6968	021310	000000			CCC		; CC=0101	
6969	021312	000257			+SEC!SEZ			
6970	021314	000265			ROR	RO	; CC=1010 RO=110001	
6971	021316	006000			BLOS	R0R7		
6972	021320	101402			BVC	R0R7		
6973	021322	102001			BMI	TST226		
6974	021324	100404					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
6975							CONDITIONAL BRANCH INST. AND	<=====
6976							REPLACE THE MOVE INSTRUCTION	<=====
6977							WHICH FOLLOWS W/ 727	<=====
6979	021326			R0R7:	MOV	#515,-(R2)	; MOVE TO MAILBOX # ***** 515 *****	
6980	021326	012742	000515		INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
6981	021332	005242			HALT		; ROR DID NOT PRODUCE CORRECT RESULTS	
6982	021334	000000					; OR SEQUENCE ERROR	
6984							*****	
6985							; TEST 226 TEST ASL INSTRUCTION	
6986							*****	
6987	021336	005212			TST226:	INC	(R2)	; UPDATE TEST NUMBER
6988	021340	022712	000226			CMP	#226,(R2)	; SEQUENCE ERROR?
6989	021344	001054				BNE	TST227-10	; BR TO ERROR HALT ON SEQ ERROR
6990	021346	012700	144000			MOV	#144000,RO	; RO=14000
6991	021352	000257				CCC		; CC=0110
6992	021354	000271				+SEN!SEC		
6993	021356	006300				ASL	RO	; CC=1001 RO=110000
6994	021360	103003				BCC	ASL1	
6995	021362	102402				BVS	ASL1	
6996	021364	001401				BEQ	ASL1	
6997	021366	100404				BMI	ASL2	
6998							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
6999							CONDITIONAL BRANCH INST. AND	<=====
7000							REPLACE THE MOVE INSTRUCTION	<=====
7001							WHICH FOLLOWS W/ 767	<=====
7002	021370			ASL1:	MOV	#516,-(R2)	; MOVE TO MAILBOX # ***** 516 *****	
7003	021370	012742	000516		INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
7004	021374	005242			HALT			
7005	021376	000000			SCC		; CC=1100	
7006	021400	000277						

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 DFKAAB.P11 T226 TEST ASL INSTRUCTION

7007	021402	000243		+CLV!CLC			
7008	021404	006300		ASL	R0	;CC=0011 R0=020000	
7009	021406	103003		BCC	ASL3		
7010	021410	102002		BVC	ASL3		
7011	021412	001401		BEQ	ASL3		
7012	021414	100004		BPL	ASL4		
7013						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
7014						CONDITIONAL BRANCH INST. AND	<=====
7015						REPLACE THE MOVE INSTRUCTION	<=====
7016						WHICH FOLLOWS W/ 754	<=====
7017	021416			ASL3:			
7018	021416	012742	000517	MOV	*517 -(R2)	;MOVE TO MAILBOX # ***** 517 *****	
7019	021422	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
7020	021424	000000		HALT		;ASL DID NOT SET CC'S CORRECTLY	
7021	021426	000277		SCC		;CC=0111	
7022	021430	000250		CLN			
7023	021432	006300		ASL	R0	;CC=0000 R0=040000	
7024	021434	101402		BLOS	ASL5		
7025	021436	102401		BVS	ASL5		
7026	021440	100004		BPL	ASL6		
7027						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
7028						CONDITIONAL BRANCH INST. AND	<=====
7029						REPLACE THE MOVE INSTRUCTION	<=====
7030						WHICH FOLLOWS W/ 742	<=====
7031	021442			ASL5:			
7032	021442	012742	000520	MOV	*520 -(R2)	;MOVE TO MAILBOX # ***** 520 *****	
7033	021446	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
7034	021450	000000		HALT		;ASL DID NOT SET CC'S CORRECTLY	
7035	021452	000257		CCC		;CC=0101	
7036	021454	000265		+SEZ!SEC			
7037	021456	006300		ASL	R0	;CC=1010 R0=100000	
7038	021460	103406		BCS	ASL7		
7039	021462	001405		BEQ	ASL7		
7040	021464	102004		BVC	ASL7		
7041	021466	100003		BPL	ASL7		
7042	021470	022700	100000	CMP	*100000, R0		
7043	021471	001404		BEQ	TST227		
7044						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	<=====
7045						CONDITIONAL BRANCH INST. AND	<=====
7046						REPLACE THE MOVE INSTRUCTION	<=====
7047						WHICH FOLLOWS W/ 724	<=====
7048	021476			ASL7:			
7049	021476	012742	000521	MOV	*521 -(R2)	;MOVE TO MAILBOX # ***** 521 *****	
7050	021502	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
7051	021504	000000		HALT		;ASL MALFUNCTIONED	
7052						; OR SEQUENCE ERROR	

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DFKAAB.P11 T226 TEST ASL INSTRUCTION

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7053 ;*****
7054 ;TEST 227 TEST ASR INSTRUCTION
7055 ;*****
7056 021506 005212      TST227: INC   (R2)    ;UPDATE TEST NUMBER
7057 021510 022712 000227   CMP   *227 (R2)  ;SEQUENCE ERROR?
7058 021514 001060       BNE   TST230-10 ;BR TO ERROR HALT ON SEQ ERROR
7059 021516 012700 100023   MOV   #100023, R0 ;R0=100023
7060 021522 000277       SCC   ;CC=0110
7061 021524 000250       CLN
7062 021526 006200       ASR   R0          ;CC=1001 RP=1400 1
7063 021530 102403       BVS   ASR1
7064 021532 103002       BCC   ASR1
7065 021534 001401       BEQ   ASR1
7066 021536 100404       BMI   ASR2
7067 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
7068 ; CONDITIONAL BRANCH INST. AND <=====
7069 ; REPLACE THE MOVE INSTRUCTION <=====
7070 ; WHICH FOLLOWS W/ 767 <=====

7071 021540 012742 000522      ASR1: MOV   *522,-(R2) ;MOVE TO MAILBOX * ***** 522 *****
7072 021540 012742 000522      ASR1: INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
7073 021544 005242           HALT
7074 021546 000000           BIC   #100000, R0 ;ASR DID NOT SET CC'S CORRECTLY
7075 021550 042700 100000      ASR2: BIC   #100000, R0 ;R0=40011
7076 021554 000277           SCC   ;CC=1100
7077 021556 000243           +CLV!CLC
7078 021560 006200           ASR   R0          ;CC=0011 R0=020004
7079 021562 102003           BVC   ASR3
7080 021564 103002           BCC   ASR3
7081 021566 001401           BEQ   ASR3
7082 021570 100004           BPL   ASR4
7083 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
7084 ; CONDITIONAL BRANCH INST. AND <=====
7085 ; REPLACE THE MOVE INSTRUCTION <=====
7086 ; WHICH FOLLOWS W/ 752 <=====

7087 021572 012742 000523      ASR3: MOV   *523,-(R2) ;MOVE TO MAILBOX * ***** 523 *****
7088 021572 012742 000523      ASR3: INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
7089 021576 005242           HALT
7090 021600 000000           SCC   ;ASR DID NOT SET CC'S CORRECTLY
7091 021602 000277           SCC   ;CC=1111
7092
7093 021604 006200           ASR   R0          ;CC=0000 R0=010002
7094 021606 101403           BLOS  ASR5
7095 021610 102402           BVS   ASR5
7096 021612 001401           BEQ   ASR5
7097 021614 100004           BPL   ASR6
7098 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====
7099 ; CONDITIONAL BRANCH INST. AND <=====
7100 ; REPLACE THE MOVE INSTRUCTION <=====
7101 ; WHICH FOLLOWS W/ 740 <=====

7102 021616 012742 000524      ASR5: MOV   *524,-(R2) ;MOVE TO MAILBOX * ***** 524 *****
7103 021616 012742 000524      ASR5: INC   -(R2)    ;SET MSGTYP TO FATAL ERROR
7104 021622 005242           HALT
7105 021624 000000           BIS   #100000, R0 ;ASR DID NOT SET CC'S CORRECTLY
7106 021626 052700 100000      ASR6: BIS   #100000, R0 ;R0=110002
7107 021632 000257           CCC   ;CC=0101
7108 021634 000265           +SEZ!SEC

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L12

MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 381  
DFKAAB.P11 T227 TEST ASR INSTRUCTION

7109 021636 006200 ASR RO ;C=1010 RO=144001  
 7110 021640 101406 BLOS ASR7  
 7111 021642 102005 BVC ASR7  
 7112 021644 100004 BPL ASR7  
 7113 021E46 001403 BEQ ASR7  
 7114 021650 022700 144001 CMP #144001,RO ;CHECK RESULT OF ASR'S  
 7115 021654 001404 BEQ TST230  
 7116  
 7117  
 7118  
 7119  
 7120 021656 ASR7:  
 7121 021656 012742 000525 MOV #525,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 525 \*\*\*\*\*  
 7122 021662 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 7123 021664 000000 HALT ;ASR DID NOT FUNCTION CORRECTLY  
 7124 ; OR SEQUENCE ERROR  
 7125  
 7126  
 7127  
 7128 ;\*\*\*\*\*  
 7129  
 7130 THIS TEST VERIFIES THE SXT INSTRUCTION. CONDITION CODES  
 7131 ARE PRESET IN EACH OF THE TWO POSSIBLE CASES. WITH THE N-BIT SET,  
 7132 THE TEST CHECKS FOR ALL ONES IN THE DESTINATION. WITH THE N-BIT  
 7133 CLEAR, THE DESTINATION SHOULD CONTAIN ALL ZEROES. THE DATA  
 7134 IS VERIFIED BY CONDITIONAL BRANCHES.  
 7135  
 7136 ;TEST 230 TEST THE SXT INSTRUCTION  
 7137 ;\*\*\*\*\*  
 7138 TST230: INC (R2) ;UPDATE TEST NUMBER  
 7139 021666 005212 000230 CMP #230,(R2) ;SEQUENCE ERROR?  
 7140 021670 022712 BNE TST231-10 ;BR TO ERROR HALT ON SEQ ERROR  
 7141 021674 001033 CLR RO ;SET CC=1011  
 7142 021676 005000 SCC  
 7143 021700 000277 CLZ  
 7144 021702 000244 SXT RO ;TRY SXT  
 7145 021704 006700 BPL SXTO ;TEST CC=1001  
 7146 021706 100006 BNE SXTO  
 7147 021710 001405 BEQ SXTO  
 7148 021712 102404 BVS SXTO  
 7149 021714 103003 BCC SXTO  
 7150 021716 022700 177777 CMP #-1,RO ;CHECK DATA RESULT  
 7151 021722 001404 BEQ SXTO ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 7152  
 7153  
 7154  
 7155  
 7156 021724 SXT0:  
 7157 021724 012742 000526 MOV #526,-(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 526 \*\*\*\*\*  
 7158 021730 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 7159 021732 000000 HALT ;RESULTS OF SXT INCORRECT  
 7160 021734 005000 CLR RO ;RO=0  
 7161 021735 005010 CLR (RO) ;LOC. 0=0  
 7162 021740 005110 COM (RO) ;LOC. 0=177777  
 7163 021742 000257 CCC ;SET CC=0110  
 7164 021744 000266 +SEZ!SEV

## M12

MAINDEC-11-DFKAA-B 11.34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 382  
DFKAAB.P11 T230 TEST THE SXT INSTRUCTION

7165 021746 006710	SXT	(R0)	
7166 021750 001005	BNE	SXT2	; TEST CC=0100
7167 021752 103404	BCS	SXT2	
7168 021754 102403	BVS	SXT2	
7169 021756 100402	BMI	SXT2	
7170 021760 005710	TST	(R0)	
7171 021762 001404	BEQ	TST231	
7172			; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS 7173
			CONDITIONAL BRANCH INST. AND 7174
			REPLACE THE MOVE INSTRUCTION 7175
			WHICH FOLLOWS W/ 745 7176 021764
7177 021764 012742 000527	SXT2:		MOVE TO MAILBOX # ***** 527 *****
7178 021770 005242	MOV	*527,-(R2)	:SET MSGTYP TO FATAL ERROR
7179 021772 000000	INC	-(R2)	:RESULTS OF SXT INCORRECT
7180	HALT		: OR SEQUENCE ERROR

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 383  
DFKAAB,P11 T230 TEST THE SXT INSTRUCTION

N12

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7181 *****
7182
7183 ; THIS TEST VERIFIES THE XOR INSTRUCTION. UNIQUE PATTERNS
7184 ; OF ONES AND ZEROES ARE MOVED TO DATA REGISTERS R0 AND R1.
7185 ; AFTER THE FIRST XOR INSTRUCTION R0=36146. AN XOR IS THEN
7186 ; EXECUTED WITH THIS NEW VALUE AND THE CONTENTS OF R1 TO
7187 ; REPRODUCE THE ORIGINAL VALUE IF R0=31525.
7188 *****
7189 ; TEST 231 TEST THE XOR INSTRUCTION
7190 *****
7191 TST231: INC (R2) ; UPDATE TEST NUMBER
7192 021774 005212
7193 021776 022712 000231 ; SEQUENCE ERROR?
7194 022002 001035 BNE TST232-10 ; BR TO ERROR HALT ON SEQ ERROR
7195 022004 012700 007463 MOV #7463,R0 ; SET UP R0
7196 022010 012701 031525 MOV #31525,R1 ; SET UP R1
7197 022014 000277 SCC ; SET CC=1110
7198 022016 000241 CLC
7199 022020 074100 XOR R1,R0 ; TRY XOR
7200 022022 101406 BLOS XOR1 ; CC=0000?
7201 022024 102405 BVS XOR1
7202 022026 001404 BEQ XOR1
7203 022030 100403 BMI XOR1
7204 022032 022700 036146 CMP #36146,R0 ; DATA RESULT CORRECT?
7205 022036 001404 BEQ XOR2
7206 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; =====
7207 ; CONDITIONAL BRANCH INST. AND ; =====
7208 ; REPLACE THE MOVE INSTRUCTION ; =====
7209 ; WHICH FOLLOWS W/ 762 ; =====
7210 022040
7211 022040 012742 000530 XOR1: MOV #530,-(R2) ; MOVE TO MAILBOX * ***** 530 *****
7212 022044 005242 000530 INC -(R2) ; SET MSGTYP TO FATAL ERROR
7213 022046 000000 HALT ;
7214 022050 010104 XOR2: MOV R1,R4 ; ;
7215 022052 000261 SEC ; CC=1110
7216 022054 000241 CLC
7217 022056 074400 XOR R4,R0 ; TRY XOR MODE 0,0
7218 022060 101406 BLOS XOR3 ; CC=0000?
7219 022062 102405 BVS XOR3
7220 022064 001404 BEQ XOR3
7221 022066 100403 BMI XOR3
7222 022070 022700 007463 CMP #7463,R0
7223 022074 001404 BEQ TST232
7224 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; =====
7225 ; CONDITIONAL BRANCH INST. AND ; =====
7226 ; REPLACE THE MOVE INSTRUCTION ; =====
7227 ; WHICH FOLLOWS W/ 743 ; =====
7228 022076
7229 022076 012742 000531 XOR3: MOV #531,-(R2) ; MOVE TO MAILBOX * ***** 531 *****
7230 022102 005242 000000 INC -(R2) ; SET MSGTYP TO FATAL ERROR
7231 022104 000000 HALT ; RESULT OF XOR INCORRECT
7232 ; OR SEQUENCE ERROR

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7233

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 022106 005212  
 022110 022712 000232  
 022114 001023  
 022116 012700 000525  
 022122 010004  
 022124 000277  
 022126 101002  
 022130 100001  
 022132 102404

THIS TEST VERIFIES THE SOB INSTRUCTION. R4 IS USED AS A COUNTER WHILE R0 IS THE ADDRESS REGISTER. CONDITIONAL BRANCHES ARE USED TO VERIFY PROPER TRANSFER OF CONTROL WHILE R4 IS CHECKED TO INSURE PROPER DECREMENTING OF R0.

7244 TEST 232 TEST SOB INSTRUCTION

 TST232: INC (R2) ;UPDATE TEST NUMBER  
 CMP #232, (R2) ;SEQUENCE ERROR?  
 BNE TST233-10 ;BR TO ERROR HALT ON SEQ ERROR

 MOV #525, R0  
 MOV R0, R4  
 SCC ;SET CC=1111  
 S081: BHI S082 ;CC=1111?  
 BPL S082  
 BVS S083

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 771

 S082:  
 MOV #532, -(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 532 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR

 S083: HALT  
 DEC R4 ;COUNT ITERATIONS  
 SCC ;CC=1111  
 SOB R0, S081 ;DO SOB W/ R0  
 BHI S084 ;CHECK CC=1111  
 BPL S084  
 BVC S084  
 TST R4 ;ITERATION COUNT OK?  
 BEQ TST233

: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
CONDITIONAL BRANCH INST. AND  
REPLACE THE MOVE INSTRUCTION  
WHICH FOLLOWS W/ 755

 S084:  
 MOV #533, -(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 533 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;INCORRECT # OF BRANCHES OR CC'S CHANGED  
; OR SEQUENCE ERROR

7277

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7283

7284

7285

7286

\*\*\*\*\*  
 THIS TEST VERIFIES THE MARK INSTRUCTION. THE EFFECTS  
 OF THE MARK INSTRUCTION ARE SIMULATED BY THE PROGRAM INSTRUCTIONS.  
 THE CONTENTS OF RS AND THE STACK POINTER ARE CHECKED AFTER EACH  
 OF THE TWO ROUTINES IN THE TEST.

\*\*\*\*\*  
 TEST 233 TEST MARK INSTRUCTION

7287 022174	005212	TST233: INC (R2)	; UPDATE TEST NUMBER
7288 022176	022712	CMP #233, (R2)	; SEQUENCE ERROR?
7289 022202	001062	BNE TST234-10	; BR TO ERROR HALT ON SEQ ERROR
7290 022204	012706	MOV #ST80T, SP	
7291 022210	012746	MOV #125252, -(SP)	: PUT RS VALUE ON STACK
7292 022214	162706	SUB #74, SP	: EFFECTIVELY PUT 36 ARGUMENTS ON STACK
7293 022220	012705	MOV #MRK1, R5	: SET NEW PC IN RS
7294 022224	012746	MOV #6436, -(SP)	: PUT MARK 36 INST. ON STACK
7295 022230	000277	SCC	: SET CC=1111
7296 022232	000137	JMP #400	: XFER CONTL TO MARK 36 INST. ON STACK
7297 022236	012742	MOV #534, -(R2)	: MOVE TO MAILBOX # ***** 534 *****
7298 022242	005242	INC -(R2)	: SET MSGTYP TO FATAL ERROR
7299 022244	000000	HALT	: MARK INST. SHOULD HAVE JUMPED TO MRK1
7300 022246	101010	BHI MRK2	: TEST CC UNAFFECTED
7301 022250	100007	BPL MRK2	: IE. CC=1111
7302 022252	102006	BVC MRK2	
7303 022254	020527	CMP RS, #125252	: CHECK RS RESTORED FROM STACK
7304 022260	001003	BNE MRK2	
7305 022262	022706	CMP #STBOT, R6	: CHECK STACK POINTER READJUSTED CORRECTLY.
7306 022266	001404	BEQ MRK3	
7307			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
7308			CONDITIONAL BRANCH INST. AND (=====
7309			REPLACE THE MOVE INSTRUCTION (=====
7310			WHICH FOLLOWS W/ 746 (=====
7311 022270		MRK2:	
7312 022270	012742	MOV #535, -(R2)	: MOVE TO MAILBOX # ***** 535 *****
7313 022274	005242	INC -(R2)	: SET MSGTYP TO FATAL ERROR
7314 022276	000000	HALT	: RESULTS OF MARK INCORRECT
7315 022300	012746	MOV #52525, -(SP)	
7316 022304	012746	MOV #6400, -(SP)	: PUT MARK 0 INST. ON STACK
7317 022310	010605	MOV SP, RS	: SET ADDR. OF MARK INST. IN RS
7318 022312	004737	JSR PC, #MRK4	: DO JSR
7319 022316	000137	JMP #MRK5	
7320 022322	000205	RTS RS	: DO RTS WITH RS TO MARK INST ON STACK
7321 022324	012742	MOV #536, -(R2)	: MOVE TO MAILBOX # ***** 536 *****
7322 022330	005242	INC -(R2)	: SET MSGTYP TO FATAL ERROR
7323 022332	000000	HALT	: RTS, MARK SEQUENCE FAILED
7324 022334	022706	CMP #STBOT, R6	: STACK ADJUSTED CORRECTLY
7325 022340	001003	BNE MRK6	: IF NOT: BR
7326 022342	022705	CMP #52525, RS	: CHECK IF RS RESTORED FROM STACK
7327 022346	001404	BEQ TST234	
7328			: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS (=====
7329			CONDITIONAL BRANCH INST. AND (=====
7330			REPLACE THE MOVE INSTRUCTION (=====
7331			WHICH FOLLOWS W/ 716 (=====
7332 022350		MRK6:	

D13

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DFKAA8.P11 T233 TEST MARK INSTRUCTION

7333 022350 012742 000537  
7334 022354 005242  
7335 022356 000000  
7336

MUV  
INC  
HALT

1537 -(R2)  
-(P2}

:MOVE TO MAILBOX # \*\*\*\*\* 537 \*\*\*\*\*  
:SET MSGTYP TO FATAL ERROR  
:RESULTS OF MARK INCORRECT  
:OR SEQUENCE ERROR

MAINDEC-II-DFKAR-B 11 34 CPU TEST MACYII 27(732) 01-OCT-76 15:03 PAGE 387  
DFKAR-B.P11 T233 TEST MARK INSTRUCTION

7337 177776

PS=177776

\*\*\*\*\*  
THESE NEXT SEVEN TESTS VERIFY THE MTPS INSTRUCTION IN ALL MODES. THE PSW IS DEFINED BY AN EQUATE STATEMENT BEFORE THE FIRST MTPS TEST. IN EACH TEST A PATTERN OF ONES AND ZEROES IS SET IN A DATA REGISTER AND MOVED TO THE PSW. THE DATA IN THE PSW, AND THE DATA REGISTER ADDRESS, ARE CHECKED TO VERIFY PROPER EXECUTION OF THE INSTRUCTION.

7347 :TEST 234 TEST MTPS INSTRUCTION  
7348 :\*\*\*\*\*  
7349 :\*\*\*\*\*  
7350 022360 005212 ;TST234: INC (R2) ;UPDATE TEST NUMBER  
7351 022362 022712 000234 CMP \$234, (R2) ;SEQUENCE ERROR?  
7352 022366 001024 BNE TST235-10 ;BR TO ERROR HALT ON SEQ ERROR  
7353 022370 012700 000377 MOV #377, R0  
7354 022374 000257 CCC  
7355 022376 106400 MTPS R0  
7356 022400 022767 000357 155370 CMP #357 PS  
7357 022406 001404 BEQ MTPS1

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND   
; REPLACE THE MOVE INSTRUCTION   
; WHICH FOLLOWS W/ 770   
; =====

7362 022410 012742 000540 MOV #540, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 540 \*\*\*\*\*  
7363 022414 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
7364 022416 000000 HALT ;MTPS FAILED  
7365 022420 005000 MTPS1: CLR R0  
7366 022422 005010 CLR (R0)  
7367 022424 000277 SCC  
7368 022426 106410 MTPS (R0) ;TRY MTPS MODE 1  
7369 022430 100403 BMI MTPS1A ;CHECK PS  
7370 022432 102402 BVS MTPS1A  
7371 022434 103401 BCS MTPS1A  
7372 022436 001004 BNE TST235

; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
; CONDITIONAL BRANCH INST. AND   
; REPLACE THE MOVE INSTRUCTION   
; WHICH FOLLOWS W/ 754   
; =====

7377 022440 MTPS1A: MOV #541, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 541 \*\*\*\*\*  
7378 022440 012742 000541 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
7379 022444 005242 HALT ;MTPS FAILED  
7380 022446 000000 ;OR SEQUENCE ERROR

\*\*\*\*\*  
7383 :TEST 235 TEST MTPS MODE 2  
7384 :\*\*\*\*\*  
7385 :\*\*\*\*\*

7386 022450 005212 ;TST235: INC (R2) ;UPDATE TEST NUMBER  
7387 022452 022712 000235 CMP \$235, (R2) ;SEQUENCE ERROR?  
7388 022456 001021 BNE TST236-10 ;BR TO ERROR HALT ON SEQ ERROR  
7389 022460 005000 CLR R0  
7390 022462 012710 177777 MOV #-1, (R0) ;R0=0  
7391 022466 005037 177776 CLR #PS ;LOC. 0=-1  
7392 022472 106420 MTPS (R0)+ ;PS=0  
;TRY MTPS W/MODE 2

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DFKAAB.P11 T235 TEST MTPS MODE 2

7393	022474	022737	000357	177776	CMP BEQ	#357, 0*PS MTPS2	;CHECK DATA	
7394	022502	001404					: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 766	<=====
7395								<=====
7396								<=====
7397								<=====
7398								<=====
7399	022504	012742	000542		MOV INC HALT	*542,-(R2)	:MOVE TO MAILBOX * ***** 542 *****	
7400	022510	005242					:SET MSGTYP TO FATAL ERROR	
7401	022512	000000					:DEST. DATA INCORRECT	
7402	022514	022700	000001		MTPS2:	CMP BEQ	:CHECK DEST. REGISTER.	
7403	022520	001404						
7404							: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 757	<=====
7405								<=====
7406								<=====
7407								<=====
7408	022522	012742	000543		MOV INC HALT	*543,-(R2)	:MOVE TO MAILBOX * ***** 543 *****	
7409	022526	005242					:SET MSGTYP TO FATAL ERROR	
7410	022530	000000					:DEST REGISTER NOT INCREMENTED BY 1	
7411							, OR SEQUENCE ERROR	
7412								
7413							;***** ;TEST 236 TEST MTPS MODE 3 ;*****	
7414								
7415								
7416	022532	005212			TST236:	INC (R2)	;UPDATE TEST NUMBER	<=====
7417	022534	022712	000236			CMP #236,(R2)	;SEQUENCE ERROR?	
7418	022540	001024				BNE TST237-10	:BR TO ERROR HALT ON SEQ ERROR	
7419	022542	012700	000402			MOV #402,R0	:R0=402	
7420	022546	005010				CLR (R0)	:LOC. 402=0	
7421	022550	012737	052652	000000		MOV #52652,0*0	:LOC. 0=52652	
7422	022556	005037	177776			CLR 0*PS	:PS=0	
7423	022562	106430				MTPS 0(R0)+	:TRY MTPS W/MODE 3	
7424	022564	022737	000252	177776		CMP #252,0*PS	:CHECK DEST. DATA	
7425	022572	001404				BEQ MTPS3		
7426							: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 763	<=====
7427								<=====
7428								<=====
7429								<=====
7430	022574	012742	000544		MOV INC	*544,-(R2)	:MOVE TO MAILBOX * ***** 544 *****	
7431	022600	005242				- (R2)	:SET MSGTYP TO FATAL ERROR	
7432	022602	000000					:DEST. DATA INCORRECT	
7433	022604	022700	000404		MTPS3:	CMP BEQ	:CHECK MODE 3 REGISTER.	
7434	022610	001404						
7435							: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS CONDITIONAL BRANCH INST. AND REPLACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 754	<=====
7436								<=====
7437								<=====
7438								<=====
7439	022612	012742	000545		MOV INC	*545,-(R2)	:MOVE TO MAILBOX * ***** 545 *****	
7440	022616	005242				- (R2)	:SET MSGTYP TO FATAL ERROR	
7441	022620	000000					:MODE 3 REGISTER INCORRECT	
7442							, OR SEQUENCE ERROR	
7443								
7444							;***** ;TEST 237 TEST MTPS MODE 4 ;*****	
7445								
7446								
7447	022622	005212	000237		TST237:	INC (R2)	;UPDATE TEST NUMBER	
7448	022624	022712	000237			CMP #237,(R2)	;SEQUENCE ERROR?	

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 DFKAAB.P11 T237 TEST MTPS MODE 4

7449	022630	001022		BNE	TST240-10	;BR TO ERROR HALT ON SEQ ERROR	
7450	022632	012700	000001	MOV	#1, R0	;R0=1	
7451	022636	012737	125125	MOV	#125125,0#0	;LOC. 0 = 125125	
7452	022644	005037	000000	CLR	#0#PS	;PS=0	
7453	022650	106440	177776	MTPS	- (R0)	;TRY MTPS W/MODE 4	
7454	022652	022737	000105	CMP	#105, #0#PS	;CHECK DEST. DATA	
7455	022660	001404		BEQ	MTPS4		
7456						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(=====)
7457						CONDITIONAL BRANCH INST. AND	(=====)
7458						REPLACE THE MOVE INSTRUCTION	(=====)
7459						WHICH FOLLOWS W/ 764	(=====)
7460	022662	012742	000546	MOV	#546,-(R2)	;MOVE TO MAILBOX # ***** 546 *****	
7461	022666	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
7462	022670	000000		HALT		;DEST. DATA INCORRECT	
7463	022672	005700		TST	RO	;CHECK MODE 4 REGISTER	
7464	022674	001404		BEQ	TST240		
7465						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(=====)
7466						CONDITIONAL BRANCH INST. AND	(=====)
7467						REPLACE THE MOVE INSTRUCTION	(=====)
7468						WHICH FOLLOWS W/ 756	(=====)
7469	022676	012742	000547	MOV	#547,-(R2)	;MOVE TO MAILBOX # ***** 547 *****	
7470	022702	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
7471	022704	000000		HALT		;MODE 4 REGISTER NOT DECREMENTED BY 1	
7472						; OR SEQUENCE ERROR	
7473							
7474						;*****	
7475						:TEST 240 TEST MTPS MODE 5	
7476						;*****	
7477	022706	005212		TST240:	INC (R2)	;UPDATE TEST NUMBER	
7478	022710	022712	000240		CMP #240, (R2)	;SEQUENCE ERROR?	
7479	022714	001021			BNE TST241-10	;BR TO ERROR HALT ON SEQ ERROR	
7480	022716	012700	000404		MOV #404, RO	;R0=404	
7481	022722	012737	177400	MOV	#177400, #0#0	;LOC. 0=177400	
7482	022730	000277		SCC		;SET ALL COND. CODES	
7483	022732	106450		MTPS	#-(R0)	;TRY MTPS W/MODE 5	
7484	022734	005737	177776	TST	#0#PS	;CHECK DEST. DATA.	
7485	022740	001404		BEQ	MTPS5		
7486						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(=====)
7487						CONDITIONAL BRANCH INST. AND	(=====)
7488						REPLACE THE MOVE INSTRUCTION	(=====)
7489						WHICH FOLLOWS W/ 766	(=====)
7490	022742	012742	000550	MOV	#550,-(R2)	;MOVE TO MAILBOX # ***** 550 *****	
7491	022746	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
7492	022750	000000		HALT		;DESTINATION DATA INCORRECT	
7493	022752	022700	000402	MTPS5:	CMP #402, RO	;CHECK MODE 5 REGISTER	
7494	022756	001404		BEQ	TST241		
7495						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS	(=====)
7496						CONDITIONAL BRANCH INST. AND	(=====)
7497						REPLACE THE MOVE INSTRUCTION	(=====)
7498						WHICH FOLLOWS W/ 757	(=====)
7499	022760	012742	000551	MOV	#551,-(R2)	;MOVE TO MAILBOX # ***** 551 *****	
7500	022764	005242		INC	-(R2)	;SET MSGTYP TO FATAL ERROR	
7501	022766	000000		HALT		;MODE 5 REGISTER NOT DECREMENTED BY 2	
7502						; OR SEQUENCE ERROR	
7503							
7504						;*****	

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MACY11 27(732) 01-OCT-76 15:03 PAGE 390  
DFKAA8.P1I T240 TEST MTPS MODE 5

				TEST 241		TEST MTPS MODE 6			
7505				TST241: INC (R2)		;UPDATE TEST NUMBER			
7506				CMP #241, (R2)		;SEQUENCE ERROR?			
7507	022770	005212	000241	BNE TST242-10		;BR TO ERROR HALT ON SEQ ERROR			
7508	022772	022712		MOV #52652, @#0		;LOC. 0=52652			
7509	022776	001024		MOV #406, R0		;R0=406			
7510	023000	012737	052652	000000	CLR #PS	;PS=0			
7511	023006	012700	000406		MTPS -406(R0)	;TRY MTPS W/MODE 6			
7512	023012	005037	177776		CMP #252, @#PS	;CHECK DEST. DATA			
7513	023016	106460	177372		BEQ MTPS6				
7514	023022	022737	000252	177776					
7515	023030	001404				; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 763		<=====	
7516									
7517								<=====	
7518								<=====	
7519								<=====	
7520	023032	012742	000552		MOV #552, -(R2)	;MOVE TO MAILBOX # ***** 552 *****			
7521	023036	005242			INC -(R2)	;SET MSGTYP TO FATAL ERROR			
7522	023040	000000			HALT	;DEST. DATA INCORRECT			
7523	023042	022700	000406		MTPS6: CMP #406, R0	;CHECK MODE 6 REGISTER			
7524	023046	001404			BEQ TST242				
7525						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 754		<=====	
7526								<=====	
7527								<=====	
7528								<=====	
7529	023050	012742	000553		MOV #553, -(R2)	;MOVE TO MAILBOX # ***** 553 *****			
7530	023054	005242			INC -(R2)	;SET MSGTYP TO FATAL ERROR			
7531	023056	000000			HALT	;MODE 6 REGISTER MODIFIED ; OR SEQUENCE ERROR			
7532									
7533									
7534						;***** TEST 242 ***** TEST MTPS MODE 7			
7535									
7536						;***** TEST 242 ***** TEST MTPS MODE 7			
7537	023060	005212	000242		TST242: INC (R2)	;UPDATE TEST NUMBER			
7538	023062	022712	000242		CMP #242, (R2)	;SEQUENCE ERROR?			
7539	023066	001024			BNE TST243-10	;BR TO ERROR HALT ON SEQ ERROR			
7540	023070	012737	052652	000000	MOV #52652, @#0	;LOC. 0=52652			
7541	023076	012700	000410		MOV #410, R0	;R0=410			
7542	023102	005037	177776		CLR #PS	;PS=0			
7543	023106	106470	177776		MTPS @-2(R0)	;TRY MTPS W/MODE 7			
7544	023112	022737	000105	177776	CMP #105, @#PS	;CHECK DEST. DATA			
7545	023120	001404			BEQ MTPS7				
7546						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 763		<=====	
7547								<=====	
7548								<=====	
7549								<=====	
7550	023122	012742	000554		MOV #554, -(R2)	;MOVE TO MAILBOX # ***** 554 *****			
7551	023126	005242			INC -(R2)	;SET MSGTYP TO FATAL ERROR			
7552	023130	000000			HALT	;DESTINATION DATA INCORRECT			
7553	023132	022700	000410		MTPS7: CMP #410, R0	;CHECK MODE 7 REGISTER			
7554	023136	001404			BEQ TST243				
7555						; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 754		<=====	
7556								<=====	
7557								<=====	
7558								<=====	
7559	023140	012742	000555		MOV #555, -(R2)	;MOVE TO MAILBOX # ***** 555 *****			
7560	023144	005242			INC -(R2)	;SET MSGTYP TO FATAL ERROR			

I13

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DFKAA.B.P11 T242 TEST MPS MODE 7

7561 023146 000000  
7562  
7563

HALT

; MODE 7 REGISTER MODIFIED  
; OR SEQUENCE ERROR

7564 \*\*\*\*  
 7565  
 7566 THE NEXT SEVEN TESTS VERIFY THE MFPS INSTRUCTION IN ALL  
 7567 MODES. IN EACH TEST, A PATTERN OF ONES AND ZEROES IS MOVED TO THE  
 7568 PSW, AND AN MFPS INSTRUCTION MOVES THE DATA TO A LOCATION SETUP  
 7569 BY R0, EITHER DIRECTLY OR INDIRECTLY. CONDITIONAL BRANCHES ARE  
 7570 USED TO CHECK PROPER ADDRESSING AND DATA.  
 7571  
 7572 \*\*\*\*  
 7573 TEST 243 TEST MFPS INSTRUCTION  
 7574 \*\*\*\*  
 7575 023150 005212 000243 TST243: INC (R2) ;UPDATE TEST NUMBER  
 7576 023152 022712 000243 CMP #243, (R2) ;SEQUENCE ERROR?  
 7577 023156 001025 000377 177776 BNE TST244-10 ;BR TO ERROR HALT ON SEQ ERROR  
 7578 023160 012737 000377 177776 MOV #377,0#PS  
 7579 023166 106700 MFPS R0  
 7580 023170 022700 177757 CMP #177757,R0  
 7581 023174 001404 BEQ MFPS1 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 7582 ; CONDITIONAL BRANCH INST. AND   
 7583 ; REPLACE THE MOVE INSTRUCTION   
 7584 ; WHICH FOLLOWS W/ 771   
 7585 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 7586 023176 012742 000556 MOV #556,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 556 \*\*\*\*\*  
 7587 023202 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 7588 023204 000000 HALT ;MFPS FAILED  
 7589  
 7590 023206 005000 MFPS1: CLR R0  
 7591 023210 012737 177777 000000 MOV #-1,0#0  
 7592 023216 005037 177776 CLR 0#PS  
 7593 023222 106710 MFPS (R0)  
 7594 023224 105737 TSTB #0  
 7595 023230 001404 BEQ TST244 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 7596 ; CONDITIONAL BRANCH INST. AND   
 7597 ; REPLACE THE MOVE INSTRUCTION   
 7598 ; WHICH FOLLOWS W/ 753   
 7599 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 7600 023232 012742 000557 MOV #557,-(R2) ;MOVE TO MAILBOX \* \*\*\*\*\* 557 \*\*\*\*\*  
 7601 023236 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 7602 023240 000000 HALT ;MFPS FAILED  
 7603 ; OR SEQUENCE ERROR  
 7604  
 7605 \*\*\*\*  
 7606 TEST 244 TEST MFPS MODE 2  
 7607 \*\*\*\*  
 7608 023242 005212 000244 TST244: INC (R2) ;UPDATE TEST NUMBER  
 7609 023244 022712 000244 CMP #244, (R2) ;SEQUENCE ERROR?  
 7610 023250 001031 BNE TST245-10 ;BR TO ERROR HALT ON SEQ ERROR  
 7611 023252 005000 CLR R0 ;R0=0  
 7612 023254 005010 CLR (R0) ;LOC. 0=0  
 7613 023256 012737 000377 177776 MOV #377,0#PS ;SET PS=357  
 7614 023264 106720 MFPS (R0) ;TRY MFPS W/MODE 2  
 7615 023266 103003 BCC MFPS2A ;BR TO ERROR IF C BIT CLEAR  
 7616 023270 102402 BVS MFPS2A ;BR TO ERROR IF V BIT SET  
 7617 023272 001401 BEQ MFPS2A ;BR TO ERROR IF Z BIT SET  
 7618 023274 100404 BMI MFPS2B ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 7619 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS   
 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS

MAINDEC-11-DFKAA-8 11:34 CPU TEST  
DFKAA8.P11 T244 TEST MFPS MODE 2

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7620							CONDITIONAL BRANCH INST. AND REF. ACE THE MOVE INSTRUCTION WHICH FOLLOWS W/ 756	<=====
7621								<=====
7622								<=====
7623	023276	012742	000560	MFPS2A:	MOV	#560,-(R2)	; MOVE TO MAILBOX # ***** 560 *****	<=====
7624	023276	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	<=====
7625	023302	005242			HALT		; COND. CODES INCORRECT	<=====
7626	023304	000000			CMP	#357,&#0	; CHECK DEST. DATA	<=====
7627	023306	022737	000357	000000	MFPS2B:	BEQ		
7628	023314	001404					; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 756	<=====
7629								<=====
7630								<=====
7631								<=====
7632								<=====
7633	023316	012742	000561		MOV	#561,-(R2)	; MOVE TO MAILBOX # ***** 561 *****	<=====
7634	023322	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	<=====
7635	023324	000000			HALT		; DEST. DATA INCORRECT	<=====
7636	023326	022700	000001		CMP	#1, R0	; CHECK MODE Z REGISTER	<=====
7637	023332	001404			BEQ	TST245		
7638							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 747	<=====
7639								<=====
7640								<=====
7641								<=====
7642	023334	012742	000562		MOV	#562,-(R2)	; MOVE TO MAILBOX # ***** 562 *****	<=====
7643	023340	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	<=====
7644	023342	000000			HALT		; MODE 2 REGISTER NOT INCREMENTED 1 ; OR SEQUENCE ERROR	<=====
7645								
7646								
7647							***** ; TEST 245 TEST MFPS MODE 3 *****	
7648								
7649								
7650	023344	005212			TST245:	INC	(R2)	; UPDATE TEST NUMBER
7651	023346	022712	000245			CMP	#245,(R2)	; SEQUENCE ERROR?
7652	023352	001033				BNE	TST246-10	; BR TO ERROR HALT ON SEQ ERROR
7653	023354	012700	000406			MOV	#406,R0	; R0=406
7654	023360	005037	000000			'LR	&#0	; LOC. 0=0
7655	023364	012737	000252	177776		I, V	#252,&#0PS	; PS=252
7656	023372	106730				MFPS	&(R0)+	; TRY MFPS WITH MODE 3
7657	023374	103403				BCS	MFPS3A	; BR TO ERROR IF C-BIT SET
7658	023376	102402				BVS	MFPS3A	; BR TO ERROR IF V-BIT SET
7659	023400	001401				BEQ	MFPS3A	; BR TO ERROR IF Z-BIT SET
7660	023402	100404				BMI	MFPS3B	
7661							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 764	<=====
7662								<=====
7663								<=====
7664								<=====
7665	023404				MFPS3A:			
7666	023404	012742	000563		MOV	#563,-(R2)	; MOVE TO MAILBOX # ***** 563 *****	<=====
7667	023410	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	<=====
7668	023412	000000			HALT		; CONDITION CODES INCORRECT	<=====
7669	023414	022737	125000	000000	MFPS3B:	CMP	#125000,&#0	; CHECK DEST. DATA
7670	023422	001404			BEQ			
7671							; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS ; CONDITIONAL BRANCH INST. AND ; REPLACE THE MOVE INSTRUCTION ; WHICH FOLLOWS W/ 754	<=====
7672								<=====
7673								<=====
7674								<=====
7675	023424	012742	000564		MOV	#564,-(R2)	; MOVE TO MAILBOX # ***** 564 *****	<=====

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DFKAAB.PII T245 TEST MFPS MODE 3

MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 395  
 DFKAA8.P11 T246 TEST MFPS MODE 4

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7732 :TEST 247      TEST MFPS MODE 5
7733 :*****  

7734 023560 005212 000247 TST247: INC (R2) :UPDATE TEST NUMBER
7735 023562 022712 000247 CMP #247, (R2) :SEQUENCE ERROR?
7736 023566 001033 BNE TST250-10 :BR TO ERROR HALT ON SEQ ERROR
7737 023570 012700 000410 MOV #410, R0 :R0=410
7738 023574 012737 177777 000000 MOV #-1, @#0 :LOC. 0=-1
7739 023602 005037 177776 CLR @#PS :PS=0
7740 023606 106750 MFPS @-(R0) :TRY MFPS W/MODE 5
7741 023610 103403 BCS MFPS5A :BR TO ERROR IF C-BIT SET
7742 023612 102402 BVS MFPS5A :BR TO ERROR IF V-BIT SET
7743 023614 100401 BMI MFPS5A :BR TO ERROR IF N-BIT SET
7744 023616 001404 BEQ MFPS5B :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
7745 : CONDITIONAL BRANCH INST. AND <=====>
7746 : REPLACE THE MOVE INSTRUCTION <=====>
7747 : WHICH FOLLOWS W/ 764 <=====>
7748 ;  

7749 023620 012742 000571 MFPS5A: MOV #571, -(R2) :MOVE TO MAILBOX # ***** 571 *****
7750 023620 005242 000571 INC -(R2) :SET MSGTYP TO FATAL ERROR
7751 023524 005242 HALT :COND. CODES INCORRECT
7752 023626 000000 000000 MFPS5B: CMP #377, @#0 :CHECK DEST. DATA
7753 023630 022737 000377 000000 BEQ MFPS5C :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
7754 023636 001404 000406 MFPS5C: MOV #572, -(R2) :CONDITIONAL BRANCH INST. AND <=====>
7755 :SET MSGTYP TO FATAL ERROR <=====>
7756 :DEST DATA INCORRECT <=====>
7757 :CHECK MODE 5 REGISTER <=====>
7758 ;  

7759 023640 012742 000572 MFPS5C: INC -(R2) :MOVE TO MAILBOX # ***** 572 *****
7760 023644 005242 HALT :SET MSGTYP TO FATAL ERROR
7761 023646 000000 000406 MFPS5C: CMP R0, #406 :DEST DATA INCORRECT
7762 023650 020027 BEQ TST250 :CHECK MODE 5 REGISTER
7763 023654 001404 000406 MFPS5C: MOV #573, -(R2) :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
7764 :CONDITIONAL BRANCH INST. AND <=====>
7765 :REPLACE THE MOVE INSTRUCTION <=====>
7766 :WHICH FOLLOWS W/ 745 <=====>
7767 ;  

7768 023656 012742 000573 MFPS5C: INC -(R2) :MOVE TO MAILBOX # ***** 573 *****
7769 023662 005242 HALT :SET MSGTYP TO FATAL ERROR
7770 023664 000000 000406 MFPS5C: HALT :MODE 5 REGISTER NOT DECREMENTED BY 2
7771 ; OR SEQUENCE ERROR  

7772 ;  

7773 :*****  

7774 :TEST 250      TEST MFPS MODE 6
7775 :*****  

7776 023666 005212 000250 TST250: INC (R2) :UPDATE TEST NUMBER
7777 023670 022712 000250 CMP #250, (R2) :SEQUENCE ERROR?
7778 023674 001034 BNE TST251-10 :BR TO ERROR HALT ON SEQ ERROR
7779 023676 012700 000401 MOV #401, R0 :R0=410
7780 023702 005037 000000 CLR @#0 :LOC. 0=0
7781 023706 012737 000252 177776 MOV #252, @#PS :PS=252
7782 023714 106760 177377 MFPS -401(R0) :TRY MFPS W/MODE 6
7783 023720 102403 BVS MFPS6A :BR TO ERROR IF V-BIT SET
7784 023722 103402 BCS MFPS6A :BR TO ERROR IF C-BIT SET
7785 023724 001401 BEQ MFPS6A :BR TO ERROR IF Z-BIT SET
7786 023726 100404 BMI MFPS6B :TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <=====>
7787 ;
  
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MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 396  
DFKAAB.P11 T250 TEST MFPS MODE 6

7788  
 7789  
 7790  
 7791 023730 012742 000574 MFPS6A: MOV #574,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 574 \*\*\*\*\*  
 7792 023730 005242 - INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 7793 023734 005242 HALT ; COND. CODES INCORRECT  
 7794 023736 000000 000252 000000 MFPS6B: CMP #252,0#0 ; CHECK DEST. DATA  
 7795 023740 022737 000401 BEQ MFPS6C ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 7796 023746 001404 ; CONDITIONAL BRANCH INST. AND  
 7797 ; REPLACE THE MOVE INSTRUCTION  
 7798 WHICH FOLLOWS W/ 753  
 7799  
 7800  
 7801 023750 012742 000575 MOV #575,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 575 \*\*\*\*\*  
 7802 023754 005242 INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 7803 023756 000000 HALT ; DEST. DATA INCORRECT  
 7804 023760 022700 000401 CMP #401, R0 ; CHECK DEST. REGISTER  
 7805 023764 001404 BEQ TST251 ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 7806 ; CONDITIONAL BRANCH INST. AND  
 7807 ; REPLACE THE MOVE INSTRUCTION  
 7808 WHICH FOLLOWS W/ 744  
 7809  
 7810 023766 012742 000576 MOV #576,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 576 \*\*\*\*\*  
 7811 023772 005242 INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 7812 023774 000000 HALT ; DEST. DATA INCORRECT  
 7813 ; OR SEQUENCE ERROR  
 7814  
 7815 ;\*\*\*\*\*  
 7816 ;TEST 251 TEST MFPS MODE ?  
 7817 ;\*\*\*\*\*  
 7818 023776 005212 TST251: INC (R2) ; UPDATE TEST NUMBER  
 7819 024000 022712 000251 CMP #251, (R2) ; SEQUENCE ERROR?  
 7820 024004 001034 BNE TST252-10 ; BR TO ERROR HALT ON SEQ ERROR  
 7821 024006 012700 000777 MOV #777, R0 ; R0=777  
 7822 024012 005037 000000 CLR 0#0 ; LOC. 0=0  
 7823 024016 012737 000125 MOV #125, 0#PS ; PS=125  
 7824 024024 106770 177407 MFPS 0-371(R0) ; TRY MFPS W/MODE ?  
 7825 024030 102403 BVS MFPS7A ; BR TO ERROR IF V-BIT SET  
 7826 024032 103002 BCC MFPS7A ; BR TO ERROR IF C-BIT SET  
 7827 024034 001401 BEQ MFPS7A ; BR TO ERROR IF Z-BIT SET  
 7828 024036 100004 BPL MFPS7B ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 7829 ; CONDITIONAL BRANCH INST. AND  
 7830 ; REPLACE THE MOVE INSTRUCTION  
 7831 WHICH FOLLOWS W/ 763  
 7832  
 7833 024040 MFPS7A: MOV #577,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 577 \*\*\*\*\*  
 7834 024040 012742 000577 INC -(R2) ; SET MSGTYP TO FATAL ERROR  
 7835 024044 005242 HALT ; CONDITION CODE INCORRECT  
 7836 024046 000000 042400 000000 MFPS7B: CMP #42400, 0#0 ; CHECK DESTINATION DATA  
 7837 024050 022737 BEQ MFPS7C ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 7838 024056 001404 ; CONDITIONAL BRANCH INST. AND  
 7839 ; REPLACE THE MOVE INSTRUCTION  
 7840 WHICH FOLLOWS W/ 753  
 7841  
 7842  
 7843 024060 012742 000600 MOV #600,-(R2) ; MOVE TO MAILBOX # \*\*\*\*\* 600 \*\*\*\*\*  
 7844

MAINDEC-11-DFKAR-B 11:34 CPU TEST MACY!1 27(732) 01-OCT-76 15:03 PAGE 397  
DFKAR8.P11 T251 TEST MFPS MODE 7

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7844 024064 005242           INC      -(R2)      ;SET MSGTYP TO FATAL ERROR
7845 024066 000000           HALT
7846 024070 022700 000777   MFPS7C: CMP      #777, R0    ;DEST. DATA INCORRECT
7847 024074 001404           BEG      TST252   ;CHECK MODE 7 REGISTER
7848
7849
7850
7851
7852 024076 012742 000601   MCV      #601, -(R2)  ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
7853 024102 005242           INC      -(R2)      CONDITIONAL BRANCH INST. AND
7854 024104 000000           HALT
7855
7856
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7867
7868 024106 005212           TST252: INC    (R2)      ;TEST THAT RESET DOES NOT CLEAR PSW
7869 024110 022712 000252   CMP      #252, (R2)  ;UPDATE TEST NUMBER
7870 024114 001014           BNE      TST253-10  ;SEQUENCE ERROR?
7871 024116 123727 025652 000377   CMPB     #PASSPT, #377  ;BR TO ERROR HALT ON SEQ ERROR
7872 024124 001014           BNE      REST
7873 024126 012737 000357 177776   MOV      #357, #PS  ;ONLY DUE RESET EVERY 256. PASSES
7874 024134 000005           RESET
7875 024136 022737 000357 177776   CMP      #357, #PS  ;BR IF TO SKIP TEST
7876 024144 001404           BEG      TST253  ;MOV ONES TO PSW
7877
7878
7879
7880
7881 024146 012742 000602   MCV      #602, -(R2)  ;PSW CORRECT?
7882 024152 005242           INC      -(R2)
7883 024154 000000           HALT
7884
7885 024156
7886
7887
7888
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7892
7893
7894
7895 024156 005212           TST253: TEST 253  TEST USER MODE R6 CAN HOLD A ONE IN EVERY POSITION
7896 024160 022712 000253   INC      (R2)      ;UPDATE TEST NUMBER
7897 024164 001014           CMP      #253, (R2)  ;SEQUENCE ERROR?
7898 024166 052767 140000 153602   BNE      TST254-10  ;BR TO ERROR HALT ON SEQ ERROR
7899 024174 012706 000001           BIS      #USRM, PS ;SET USER MODE
7900
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MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 398  
DFKAA8.P11 T253 TEST USER MODE R6 CAN HOLD A ONE IN EVERY POSITION

7900	024200	000241						:CLEAR C-BIT
7901	024202	006106			LSP1:	CLC	ROL	:ROTATE 1 POSITION
7902	024204	103376				BCC	R6	:BR IF NOT ALL DONE
7903	024206	001407				BEQ	USP1	:BR IF NO BITS PICKED
7904	024210	042767	140000	153560		BIC	USPIA	:CLEAR USER MODE
7905	024216	012742	000603			MOV	#603,-(R2)	;MOVE TO MAILBOX * ***** 603 *****
7906	024222	005242				INC	-(R2)	;SET MSGTYP TO FATAL ERROR
7907	024224	000000				HALT		;USER MODE R6 PICKED A BIT
7908	024226							
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7920	024226	005212				TEST254: INC	(R2)	:UPDATE TEST NUMBER
7921	024230	022712	000254			CMP	#254,(R2)	:SEQUENCE ERROR?
7922	024234	001036				BNE	USP4-14	;BR TO ERROR HALT ON SEQ ERROR
7923	024236	052767	140000	153532		BIS	USR,PS	:SET USER MODE
7924	024244	012706	177777			MOV	#-1,R6	:SET USER R6 TO ALL ONES
7925	024250	022706	177777			CMP	#-1,R6	:READ AND CHECK USER R6
7926	024254	001407				BEQ	USP2	:BR IF NO ERROR
7927	024256	042767	140000	153512		BIC	USR,PS	:CLEAR USER MODE
7928	024264	012742	000604			MOV	#604,-(R2)	;MOVE TO MAILBOX * ***** 604 *****
7929	024270	005242				INC	-(R2)	;SET MSGTYP TO FATAL ERROR
7930	024272	000000				HALT		;USER R6 WILL NOT HOLD ALL ONES
7931	024274	042767	140000	153474	JSP2:	BIC	USR,PS	:SET KERNEL MODE
7932	024302	022706	177777			CMP	#-1,R6	:KERNEL MODE R6 ADDR. FROM USER MODE?>>
7933	024306	001004				BNE	USP3	
7934								: TO SCOPE: CLEAR THE RIGHT BYTE OF THIS <====
7935								CONDITIONAL BRANCH INST. AND <====
7936								REPLACE THE MOVE INSTRUCTION <====
7937								WHICH FOLLOWS W/ 753 <====
7938	024310	012742	000605			MOV	#605,-(R2)	;MOVE TO MAILBOX * ***** 605 *****
7939	024314	005242				INC	-(R2)	;SET MSGTYP TO FATAL ERROR
7940	02431E	000000				HALT		;DUAL ADDRESSING ERROR USER/KERNEL R6
7941	024320	005006				CLR	R6	:CLEAR KERNEL MODE SP
7942	024322	052767	140000	153446	USP3:	BIS	USR,PS	:SET USER MODE
7943	024330	022706	177777			CMP	#-1,R6	:CHECK USER R6 NOT ADDR. FROM KERNEL MODE
7944	024334	001404				BEQ	USP4	:BR IF NO ERROR
7945	024336	012742	000606			MOV	#606,-(R2)	;MOVE TO MAILBOX * ***** 606 *****
7946	024342	005242				INC	-(R2)	;SET MSGTYP TO FATAL ERROR
7947	024344	000000				HALT		;DUAL ADDRESSING ERROR OR SEQUENCE ERROR
7948	024346	012706	000500			MOV	#STBOT,R6	:RESTORE SP USER
7949	024352	042767	140000	153416	USP4:	BIC	USR,PS	:SET KERNEL MODE
7950	024360	012706	000500			MOV	#STBOT,R6	:RESTORE SP KERNEL
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THESE NEXT TWO TESTS VERIFY MFPI AND MTPI INSTRUCTIONS  
WITH R6 IN MODE 0.

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7958 :TEST 255 TEST MFPI WITH R6 IN MODE 0
7959 :*****+
7960 024364 005212 000255 TST255: INC (R2) ;UPDATE TEST NUMBER
7961 024366 022712 000255 CMP #255, (R2) ;SEQUENCE ERROR?
7962 024372 001032 000500 BNE TST256-10 ;BR TO ERROR HALT ON SEQ ERROR
7963 024374 012706 000500 MOV #STBOT, R6 ;INITIALIZE KERNEL STACK POINTER
7964 024400 012767 140000 153370 MOV #USR, PS ;SET USER MODE/PREVIOUS KERNEL
7965 024406 012706 026116 MOV #USTBOT, R6 ;INITIALIZE USER STACK POINTER
7966 024412 006506 MFPI R6 ;TRY MFPI WITH MODE 0
7967 024414 022767 140000 153354 CMP #140000, PS ;CHECK PSW
7968 024422 001407 BEQ MFPIO ;BR IF NO ERROR
7969 024424 042767 140000 153344 BIC #USR, PS ;CLEAR USER MODE
7970 024432 012742 000607 001444 MOV #607, -(R2) ;MOVE TO MAILBOX * ***** 607 *****
7971 024436 005242 HALT INC -(R2) ;SET MSGTYP TO FATAL ERROR
7972 024440 000000 HALT ;INCORRECT PSW FROM MFPI
7973 024442 022767 000500 001444 MFPIO: CMP #STBOT, USTBOT-2 ;CHECK DATA ON STACK
7974 024450 001407 BEQ MFPIOA ;BR IF NO ERROR
7975 024452 042767 140000 153316 BIC #USR, PS ;CLEAR USER MODE
7976 024460 012742 000610 001444 MOV #610, -(R2) ;MOVE TO MAILBOX * ***** 610 *****
7977 024464 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
7978 024466 000000 HALT ;INCORRECT DATA FROM MFPI
7979 024470 MFPIOA: ;*****+
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7982 :TEST 256 TEST MTPI WITH R6 IN MODE 0
7983 :*****+
7984 024470 005212 000256 TST256: INC (R2) ;UPDATE TEST NUMBER
7985 024472 022712 000256 CMP #256, (R2) ;SEQUENCE ERROR?
7986 024476 001032 153272 BNE TST257-10 ;BR TO ERROR HALT ON SEQ ERROR
7987 024500 005067 CLR PS ;SET KERNEL MODE
7988 024504 005006 CLR R6 ;INITIALIZE KERNEL R6
7989 024506 012767 140000 153262 MOV #USR, PS ;SET USER MODE/PREVIOUS KERNEL
7990 024514 012706 026116 MOV #USTBOT, R6 ;INITIALIZE USER STACK POINTER
7991 024520 012746 000500 MOV #STBOT, -(R6) ;SET UP TARGET DATA
7992 024524 006606 MTPI R6 ;TRY MODE 0 MTPI
7993 024526 022767 140000 153242 CMP #USR, PS ;CHECK PSW
7994 024534 001407 BEQ MTPIO ;BR IF NO ERROR
7995 024536 042767 140000 153232 BIC #USR, PS ;CLEAR USER MODE
7996 024544 012742 000611 001404 MOV #611, -(R2) ;MOVE TO MAILBOX * ***** 611 *****
7997 024550 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
7998 024552 000000 HALT ;PS INCORRECT FOLLOWING MTPI
7999 024554 005067 153216 CLR PS ;SET KERNEL MODE
8000 024560 020627 000500 CMP R6, #STBOT ;CHECK TARGET DATA
8001 024564 001404 BEQ TST257 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
8002 ;CONDITIONAL BRANCH INST. AND
8003 ;REPLACE THE MOVE INSTRUCTION
8004 ;WHICH FOLLOWS W/ 745 <=====
8005 ;*****+
8006 024566 012742 000612 MOV #612, -(R2) ;MOVE TO MAILBOX * ***** 612 *****
8007 024572 005242 INC -(R2) ;SET MSGTYP TO FATAL ERROR
8008 024574 000000 HALT ;DATA INCORRECT FOLLOWING MTPI
8009 ;OR SEQUENCE ERROR
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 THIS TEST VERIFIES THE CONTENTS OF THE BRANCH ROM. THE TEST  
 EXECUTES EVERY POSSIBLE BRANCH WITH EVERY POSSIBLE CONDITION  
 CODE COMBINATION.

THE ROUTINE USES TWO TABLES. THE BRANCH TABLE HOLDS ALL THE  
 POSSIBLE BRANCH INSTRUCTIONS, THE OTHER TABLE (YNTAB) HOLDS BIT MAPS FOR  
 EACH BRANCH. A ONE IN THE BIT MAP INDICATES THAT THE CORRESPONDING  
 BRANCH INSTRUCTION SHOULD BRANCH FOR THE CONDITION CODE SETTING WHICH  
 CORRESPONDS TO THE BIT POSITION WITHIN THE MAP. FOR EXAMPLE IF THE LEFT  
 MOST BIT IS A ONE THEN THE CORRESPONDING BRANCH INSTRUCTION SHOULD BRANCH  
 WHEN THE CONDITION CODES ARE 0.

THE ROUTINE CONSISTS OF NESTED LOOPS: THE OUTER LOOP SETS UP  
 ALL THE POSSIBLE BRANCH INSTRUCTIONS. THE INNER LOOP SETS UP EVERY POSSIBLE  
 CONDITION CODE FOR EACH BRANCH.

THE BIT MAP IS USED TO SET THE ADDRESS LOCATION IN TWO  
 JUMP MODE 3 INSTRUCTIONS. THE ADDRESSES ARE CHANGED TO ALLOW THE  
 PROGRAM TO CONTINUE OR JUMP TO AN ERROR ROUTINE DEPENDING UPON  
 WHETHER IT HANDLED THE BRANCH INSTRUCTION CORRECTLY.

AT ANY ERROR HALT, LOCATION, BRH, HOLDS THE BRANCH INSTRUCTION  
 UNDER TEST AND LOCATION, CC, HOLDS THE VALUE OF THE CONDITION CODES  
 AT THE TIME THE BRANCH WAS EXECUTED.

\*\*\*\*\*  
 ;TEST 257 TEST THE BRANCH ROM  
 \*\*\*\*\*

SET257:	INC	(R2)	;UPDATE TEST NUMBER
	CMP	\$257, (R2)	;SEQUENCE ERROR?
	BNE	ER	;BR TO ERROR HALT ON SEQ ERROR
SETUP:	MOV	\$BRTTAB, R0	;INITIALIZE BRANCH TABLE POINTER
	MOV	\$YNTTAB, R4	;INITIALIZE YES/NO BRANCH MAP POINTER
	MOV	\$15, BRCT	;INITIALIZE BRANCH TABLE COUNT
SETBR:	MOV	(R0)+, BRH	;GET NEXT BRANCH INST.
	MOV	(R4)+, R1	;GET NEXT BRANCH MAP
	MOV	\$-1, CC	;INITIALIZE CONDITION CODE VALUE
	MOV	\$16, R3	;INITIALIZE CONDITION CODE COUNT
SETCC:	INC	CC	;SET FOR NEXT CC VALUE
	BIT	\$100000, R1	;SEE IF SHOULD BR W/ THESE CC'S
	MOV	\$177776, R5	;SIMULATE A JNE
	BIC	\$177773, R5	(JUMP NOT EQUAL)
	JMP	+4(R5)	TO SET2BR
	JMP	SET2BR	
	MOV	\$CONT, NBR	;SET TO CONTINUE IF NO BRANCH
	MOV	\$ER, YBR	;SET TO REPORT ERROR IF BRANCH
	JMP	AROUND	;GO AROUND OPPOSITE CONDITION
SET2BR:	MOV	\$ER, NBR	;SET TO REPORT ERROR IF NO BRANCH
	MOV	\$CONT, YBR	;SET TO CONTINUE IF BRANCH
AROUND:	ROL	R1	;UPDATE BIT MAP
	MOV	(PC)+, \$((PC)+)	;SET CONDITION CODE
CC:	O		;NEW CC VALUE GOES HERE
	177776		
BRH:	O		;BRANCH INST. GOES HERE
	JMP	\$((PC)+)	;THIS JUMP IF NO BRANCH
NBR:	O		;WHERE TO GO IF NO BRANCH OCCURS

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DFKAA8.P11 T257 TEST THE BRANCH ROM

8067	024746	000137		JMP	J(PC)+	THIS JUMP IF BRANCH OCCURS	
8068	024750	000000		YBR:	O	WHERE TO GO IF BRANCH OCCURS	
8069	024752	012702	000304	ER:	MOV	\$TESTN,R2	RESTORE POINTER
8070	024756	012742	000613		MOV	#613,-(R2)	MOVE TO MAILBOX # ***** 613 *****
8071	024762	005242			INC	-(R2)	SET MSGTYP TO FATAL ERROR
8072	024764	000000			HALT		
8073	024766	000000					
8074	024770	005303		BRCT:	O		
8075	024772	013705	177776	CCNT:	DEC	R3	CC'S DONE?
8076	024776	042705	177773		MOV	#177776,R5	SIMULATE A JNE
8077	025002	000165	025006		BIC	#177773,R5	(JUMP NOT EQUAL)
8078	025006	000167	177632		JMP	.+4(R5)	TO SETCC
8079	025012	005367	177750			SETCC	
8080	025016	013705	177776		DEC	BRCT	BR'S DONE?
8081	025022	042705	177773		MOV	#177776,R5	SIMULATE A JNE
8082	025026	000165	025032		BIC	#177773,R5	(JUMP NOT EQUAL)
8083	025032	000167	177566		JMP	.+4(R5)	TO SETBR
					JMP	SETBR	

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 8097 025044 001052  
 8098 025046 005000  
 8099 025050 005001  
 8100 025052 005002  
 8101 025054 005003  
 8102 025056 005004  
 8103 025060 005005  
 8104 025062 005006  
 8105 025064 052700 000001  
 8106 025070 052701 000002  
 8107 025074 052702 000004  
 8108 025100 052703 000010  
 8109 025104 052704 000020  
 8110 025110 052705 000040  
 8111 025114 052706 000100  
 8112 025120 022706 000100  
 8113 025124 001022  
 8114 025126 022705 000040  
 8115 025132 001017  
 8116 025134 022704 000020  
 8117 025140 001014  
 8118 025142 022703 000010  
 8119 025146 001011  
 8120 025150 022702 000004  
 8121 025154 001006  
 8122 025156 022701 000002  
 8123 025162 001003  
 8124 025164 022700 000001  
 8125 025170 001404  
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 8130 025172  
 8131 025172 012742 000614  
 8132 025176 005242  
 8133 025200 000000  
 8134 025202 012702 000304  
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;\*\*\*\*\*  
 ;THE FOLLOWING TEST VERIFIES THAT NO DUAL ADDRESSING OF THE GENERAL  
 ;REGISTERS OCCURS. ALL REGISTERS ARE CLEARED, AND A UNIQUE BIT IS SET  
 ;IN EACH. CMP INSTRUCTIONS CHECK THAT ONLY ONE BIT IS SET IN EACH  
 ;REGISTER.  
 ;\*\*\*\*\*  
 ;TEST 260 DUAL REGISTER ADDRESSING TEST  
 ;\*\*\*\*\*  
 TST260: INC (R2) ;UPDATE TEST NUMBER  
 CMP #260, (R2) ;SEQUENCE ERROR?  
 BNE DAERR ;BR TO ERROR HALT ON SEQ ERROR  
 BITCLR: CLR R0 ;INITIALIZE ALL REGISTERS  
 CLR R1  
 CLR R2  
 CLR R3  
 CLR R4  
 CLR R5  
 CLR R6  
 BITSET: BIS #1, R0 ;SET R0=1  
 BIS #2, R1 ;R1=2  
 BIS #4, R2 ;R2=4  
 BIS #10, R3 ;R3=10  
 BIS #20, R4 ;R4=20  
 BIS #40, R5 ;R5=40  
 BIS #100, R6 ;R6=100  
 BITCHK: CMP #100, R6 ;TEST THAT NO DUAL ADDRESSING OCCURRED  
 BNE DAERR ;BR TO ERROR HALT IF ANY OTHER BITS ARE SET  
 CMP #40, R5  
 BNE DAERR  
 CMP #20, R4  
 BNE DAERR  
 CMP #10, R3  
 BNE DAERR  
 CMP #4, R2  
 BNE DAERR  
 CMP #2, R1  
 BNE DAERR  
 CMP #1, R0  
 BEQ BITCON ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  
 ;CONDITIONAL BRANCH INST. AND  
 ;REPLACE THE MOVE INSTRUCTION  
 ;WHICH FOLLOWS W/ 726 <=====  
 ;DAERR:  
 MOV #614, -(R2) ;MOVE TO MAILBOX # \*\*\*\*\* 614 \*\*\*\*\*  
 INC -(R2) ;SET MSGTYP TO FATAL ERROR  
 HALT ;DUAL ADDRESSING ERROR  
 BITCON: MOV #\$TESTN, R2 ;RESTORE POINTER

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8136
8137      THIS TEST VERIFIES THAT THE UPPER BYTE OF THE PSW IS NOT AFFECTED
8138      WHEN THE PRIORITY LEVEL OR CC'S ARE CHANGED. ALL BITS ARE
8139      INITIALLY SET IN THE PSW, AND THE LOW BYTE IS CLEARED. A BIT
8140      INSTRUCTION VERIFIES THE DATA.
8141
8142      **** TEST 261 TEST BYTE INSTRUCTION ON PSW ****
8143
8144      TST261: INC    (R2)          ; UPDATE TEST NUMBER
8145      025206 005212           ; CMP    #261, (R2)        ; SEQUENCE ERROR?
8146      025210 022712 000261     ; BNE    BTERR           ; BR TO ERROR HALT ON SEQ ERROR
8147      025214 001012           ; BIS    #170357,2@PS   ; SET ALL POSSIBLE BITS IN PSW
8148      025216 052737 170357 177776 ; CLRB   @PS            ; CLR PR LEVEL AND CC'S
8149      025224 105037 177776           ; MOV    @PS, R0         ; COPY CONTENTS OF PSW
8150      025230 013700 177776           ; BIT    #170000, R0   ; TEST THAT UPPER BYTE IS UNAFFECTED
8151      025234 032700 170000           ; BNE    BTCON           ; CONTINUE IF OK
8152      025240 001006           ; BTERR: CLR    @PS            ; RETURN TO KERNEL MODE
8153      025242 005037 177776           ; MOV    #615, -(R2)    ; MOVE TO MAILBOX * ***** 615 *****
8154      025246 012742 000615           ; INC    -(R2)          ; SET MSGTYP TO FATAL ERROR
8155      025252 005242           ; HALT   @PS            ; BYTE INSTRUCTION ALTERED PSW
8156      025254 000000           ; BTCON: CLR    @PS            ; RETURN TO KERNEL MODE
8157      025256 005037 177776           ; **** THIS TEST VERIFIES THAT A JMP INSTRUCTION DOES NOT ALTER THE
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8159      8160
8161      8162      CONDITION CODES IN THE PSW. THE CC'S ARE PRESET, THE JMP IS
8163      8164      EXECUTED, AND CONDITIONAL BRANCHES VERIFY THE STATE OF THE CC'S.
8165
8166      **** TEST 262 TEST THAT JMP INSTRUCTION DOES NOT AFFECT CONDITION CODES ****
8167
8168      TST262: INC    (R2)          ; UPDATE TEST NUMBER
8169      025262 005212           ; CMP    #262, (R2)        ; SEQUENCE ERROR?
8170      025264 022712 000262     ; BNE    TST263-10       ; BR TO ERROR HALT ON SEQ ERROR
8171      025270 001010           ; SCC    +CLN!CLV        ; CC=0101
8172      025272 000277           ; +CLN!CLV
8173      025274 000252           ; JMP    JMPT             ; JUMP TO TEST PSW
8174      025276 000167 000000           ; JMPT: BMI    JMPERR          ; BR TO ERROR HALT IF N-BIT IS SET
8175      025302 100403           ; BNE    JMPERR          ; BR TO ERROR HALT IF Z-BIT IS CLEAR
8176      025304 001002           ; BVS    JMPERR          ; BR TO ERROR HALT IF V-BIT IF SET
8177      025306 102401           ; BCS    TST263           ; TO SCOPE: CLEAR THE RIGHT BYTE OF THIS
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8182      025312 005212           ; JMPERR: MOV    #616, -(R2)    ; =====
8183      025312 012742 000616     ; INC    -(R2)          ; =====
8184      025316 005242           ; HALT   @PS            ; =====
8185      025320 000000           ;           ; MOVE TO MAILBOX * ***** 616 *****
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MAINDEC-11-DFKAAB-8 11:34 CPU TEST MACY 11 27(732) 01-OCT-76 15:03 PAGE 404  
DFKAAB.P11 T262 TEST THAT JMP INSTRUCTION DOES NOT AFFECT CONDITION CODES

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      THIS TEST VERIFIES THE SET AND CLEAR CONDITION CODE INSTRUCTIONS.  

      THE TEST CONSISTS OF TWO ROUTINES, ONE TO TEST ALL CLEAR CC  

      INSTRUCTIONS, AND THE SECOND TO TEST ALL SET CC INSTRUCTIONS. ALL  

      POSSIBLE COMBINATIONS OF CONDITION CODES ARE TESTED, INCLUDING NOP'S.  

      TO TEST THE CLEAR CC INSTRUCTIONS, ALL CONDITION CODES ARE  

      INITIALLY SET. THE INSTRUCTION IS EXECUTED, AND THE PSW IS CHECKED  

      TO VERIFY THE PROPER COMBINATION OF CONDITION CODES.  

      TO TEST THE SET CC INSTRUCTIONS, THE CONDITION CODES ARE  

      INITIALLY CLEARED, AND ONLY THE REQUIRED BITS ARE SET BY THE SET CC  

      INSTRUCTION. THE CONTENTS OF THE PSW ARE CHECKED TO VERIFY THAT  

      ONLY THE REQUIRED BITS WERE SET.  

****  

:TEST 263 TEST SET CC AND CLEAR CC INSTRUCTIONS  

****  

TST263: INC (R2) ;UPDATE TEST NUMBER  

      CMP #263, (R2) ;SEQUENCE ERROR?  

      BNE CCERR ;BR TO ERROR HALT ON SEQ ERROR  

      MOV #240, CC1 ;INITIALIZE CLR CC INSTRUCTION CODES  

      MOV #17, CC2 ;INITIALIZE OCTAL MAP  

      MOV #261, SC3 ;INITIALIZE SET CC INSTRUCTION CODES  

      MOV #1, SC4 ;INITIALIZE OCTAL MAP  

      CLRCOD: SCC ;SET ALL CONDITION CODES  

      CC1: O ;CONDITION CODE INSTRUCTION  

      MOV #PS, R4 ;COPY THE PSW  

      BIC #177760, R4 ;ISOLATE CONDITION CODES  

      CMP (PC)+, R4 ;CHECK THAT PROPER CC'S WERE CLEARED  

      O ;OCTAL REPRESENTATION OF CC'S  

      BEQ CON1 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  

              ;CONDITIONAL BRANCH INST. AND  

              ;REPLACE THE MOVE INSTRUCTION  

              ;WHICH FOLLOWS W/ 753  

      MOV #617, -(R2) ;MOVE TO MAILBOX # ***** 61 *****  

      INC -(R2) ;SET MSGTYP TO FATAL ERROR  

      HALT ;CLEAR CC INSTRUCTION FAILED  

      CON1: DEC CC2 ;SET NEXT OCTAL MAP OF CC'S  

      INC CC1 ;GET NEXT CLEAR CC INSTRUCTION  

      CMP CC1, #257 ;TEST FOR CCC INSTRUCTION  

      BLE CLRCD ;GO TEST NEXT INSTRUCTION IF NOT FOUND  

      CLRCD ;CHECK FOR NOP=260  

      CMP CC1, #260 ;GO TEST SET CC INSTRUCTIONS  

      BNE SETCD ;SET OCTAL MAP TO TEST NOP  

      M V #17, CC2 ;GO TEST NOP  

      SETCD ;CLEAR ALL CONDITION CODES  

      BR CLRCD ;CONDITION CODE INSTRUCTION  

      CCC ;COY PSW  

      O ;CLEAR AWAY UNWANTED BITS  

      MOV #PS, R4 ;CHECK THAT PROPER CC'S WERE SET  

      BIC #177760, R4 ;OCTAL REPRESENTATION OF CC'S  

      CMP (PC)+, R4 ;TO SCOPE: CLEAR THE RIGHT BYTE OF THIS  

      O ;CONDITIONAL BRANCH INST. AND  

      BEQ CON2 ;REPLACE THE MOVE INSTRUCTION
  
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MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 405  
 DFKAAB.P11 T263 TEST SET CC AND CLEAR CC INSTRUCTIONS

8243							WHICH FOLLOWS W/ 716	<=====
8244	025476							
8245	025476	012742	000620	CCERR:	MOV	#620,-(R2)	; MOVE TO MAILBOX # ***** 620 *****	
8246	025502	005242			INC	-(R2)	; SET MSGTYP TO FATAL ERROR	
8247	025504	000000			HALT		; SET CC FAILED OR SEQUENCE ERROR	
8248	025506	005267	177760	CON2:	INC	SC4	; SET NEXT OCTAL MAP	
8249	025512	005267	177740		INC	SC3	; PREPARE NEXT SET CC INSTRUCTION	
8250	025516	026727	177734	000277	CMP	SC3, #277	; FINISHED?	
8251	025524	003753			BLE	SETCD	; BR IF NO	

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MAINDEC-11-DFKAA-8 11:34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 406  
DFKAAB.P11 T263 TEST SET CC AND CLEAR CC INSTRUCTIONS

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 407  
 DFKAA.B.P11 T264 END OF PASS SEQUENCE

8290					.EVEN			
8291	025706	000402			BRTAB:	BR	.+6	
8292	025710	001002				BNE	.+6	
8293	025712	001402				BEQ	.+6	
8294	025714	002002				BGE	.+6	
8295	025716	002402				BLT	.+6	
8296	025720	003002				BGT	.+6	
8297	025722	003402				BLE	.+6	
8298	025724	100002				BPL	.+6	
8299	025726	100402				BMI	.+6	
8300	025730	101002				BHI	.+6	
8301	025732	101402				BLOS	.+6	
8302	025734	102002				BVC	.+6	
8303	025736	102402				BVS	.+6	
8304	025740	103002				BCC	.+6	; SAME AS BHIS
8305	025742	103402				BCS	.+6	; SAME AS BLO
8306								
8307		000002				.RADIX	2	
8308	025744	177777				YNTAB:	1111111111111111	
8309	025746	170360					1111000011110000	; BR
8310	025750	007417					0000111100001111	; BNE: Z=0
8311	025752	146063					1100110000110011	; BEQ: Z=1
8312	025754	031714					0011001111001100	; BGE: N XOR V =0
8313	025756	140060					1100000000110000	; BLT: N XOR V =1
8314	025760	037717					0011111111001111	; BGT: Z+(N XOR V) =0
8315								; BLE: Z+(N XOR V) =1
8316	025762	177400					1111111100000000	; BPL: N=0
8317	025764	000377					0000000011111111	; BMI: N=1
8318	025766	120240					1010000010100000	; BHI: C+Z=0
8319	025770	057537					0101111101011111	; BLOS: C+Z=1
8320	025772	146314					1100110011001100	; BVC: V=0
8321	025774	031463					0011001100110011	; BVS: V=1
8322	025776	125252					1010101010101010	; BCC: C=0
8323	026000	052525					0101010101010101	; BCS: C=1
8324		000010				.RADIX	8	
8325								
8326	026002	012737	026012	C00024	PWRDN:	MOV	*PWRUP, @#24	
8327	026010	000000				HALT		; SET UP FOR A POWER UP
8328								
8329	026012	012737	026002	000024	PWRUP:	MOV	*PWRDN, @#24	
8330	026020	012706	000500			MOV	*ST80T, R6	; SET UP STACK POINTER
8331	026024	132767	000040	152267		BITB	*#40_SENVIM	; SHOULD PRINT?
8332	026032	001010				BNE	PWR2	; IF NOT: BR
8333	026034	012700	026060			MOV	*PFMES, R0	; GET POWER FAIL MESSG.
8334	026040	105737	177564		WATE:	TSTB	@#TPS	; TTY READY?
8335	026044	100375				BPL	WATE	; IF NOT: BR
8336	026046	112037	177566			MOVB	(R0)+, @#TPB	; PRINT NEXT CHAR.
8337	026052	001372				BNE	WATE	; IF NOT DONE: BR
8338	026054	000137	000500		PWR2:	JMP	*#START	; START PROGRAM AGAIN
8339								
8340	026060	006412	047520	042527	PFMES:	.PSCIZ	<12><15>.POWER FAILURE.<12><15>	
8341	026066	020122	040506	046111				
8342	026074	051125	005105	000015				
8343					.EVEN			
8344	026102	000006			BLKV:	6		
8345	026116				USTPJT:			

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 408  
 DFKAA.B.P11 T264 END OF PASS SEQUENCE

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8346
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8352 026116
8353 026116 012742 000622      T04:    MOV    #622,-(R2) ;MOVE TO MAILBOX # ***** 622 *****
8354 026122 005242              INC    -(R2)  ;SET MSGTYP TO FATAL ERROR
8355 026124 000000              HALT   ;TRAPPED THRU LOC. 4
8356 026126
8357 026126 012742 000623      T010:   MOV    #623,-(R2) ;MOVE TO MAILBOX # ***** 623 *****
8358 026132 005242              INC    -(R2)  ;SET MSGTYP TO FATAL ERROR
8359 026134 000000              HALT   ;TRAPPED THRU LOC. 10
8360 026136
8361 026136 012742 000624      T014:   MOV    #624,-(R2) ;MOVE TO MAILBOX # ***** 624 *****
8362 026142 005242              INC    -(R2)  ;SET MSGTYP TO FATAL ERROR
8363 026144 000000              HALT   ;TRAPPED THRU LOC. 14
8364 026146
8365 026146 012742 000625      T030:   MOV    #625,-(R2) ;MOVE TO MAILBOX # ***** 625 *****
8366 026152 005242              INC    -(R2)  ;SET MSGTYP TO FATAL ERROR
8367 026154 000000              HALT   ;TRAPPED THRU LOC. 30
8368 026156
8369 026156 012742 000626      T034:   MOV    #626,-(R2) ;MOVE TO MAILBOX # ***** 626 *****
8370 026162 005242              INC    -(R2)  ;SET MSGTYP TO FATAL ERROR
8371 026164 000000              HALT   ;TRAPPED THRU LOC. 34
8372 026166
8373 026166 012742 000627      T0114:  MOV    #627,-(R2) ;MOVE TO MAILBOX # ***** 627 *****
8374 026172 005242              INC    -(R2)  ;SET MSGTYP TO FATAL ERROR
8375 026174 000000              HALT   ;TRAPPED THRU LOC. 114
8376 026176
8377 026176 012742 000630      T0244:  MOV    #630,-(R2) ;MOVE TO MAILBOX # ***** 630 *****
8378 026202 005242              INC    -(R2)  ;SET MSGTYP TO FATAL ERROR
8379 026204 000000              HALT   ;TRAPPED THRU LOC. 244
8380 026206
8381 026206 012742 000631      T0250:  MOV    #631,-(R2) ;MOVE TO MAILBOX # ***** 631 *****
8382 026212 005242              INC    -(R2)  ;SET MSGTYP TO FATAL ERROR
8383 026214 000000              HALT   ;TRAPPED THRU LOC. 250
8384 026214 000001              .END

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\*\*\*\*\* THE FOLLOWING ARE SPECIAL CPU TRAP HANDLERS TO TRAP AND REPORT SPECIAL TRAPS. \*\*\*\*\*

MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 410  
 DFKAA8.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

A\$BASE = 000000	432			
A\$CDW1 = 000000	432			
A\$CDW2 = 000000	432			
A\$CPUOP= 000000	432	447		
A\$CT 025E16	8262	8264	8269	8272*
A\$DC1 J20054	6492	6493	6499*	
A\$DC2 020064	6494	6503*		
A\$DC3 020104	6507	6508	6514*	
A\$DC4 020114	6509	6518*		
A\$DC5 020132	6521	6522	6523	6527*
A\$DW0 = 000000	432			
A\$DW1 = 000000	432			
A\$DW10= 000000	432			
A\$DW11= 000000	432			
A\$DW12= 000000	432			
A\$DW13= 000000	432			
A\$DW14= 000000	432			
A\$DW15= 000000	432			
A\$DW2 = 000000	432			
A\$DW3 = 000000	432			
A\$DW4 = 000000	432			
A\$DW5 = 000000	432			
A\$DW6 = 000000	432			
A\$DW7 = 000000	432			
A\$DW8 = 000000	432			
A\$DW9 = 000000	432			
A\$D1 017670	6414	6415	6421*	
A\$D2 017700	6416	6425*		
A\$D3 017714	6428	6429	6435*	
A\$D4 017724	6430	6439*		
A\$D5 017742	6442	6443	6449*	
A\$D6 017752	6444	6453*		
A\$D7 017764	6454	6455	6461*	
A\$D8 017774	6456	6465*		
A\$D9 020014	6468	6469	6470	6476*
A\$EVCT= 000000	432	438		
A\$EV\$M = 000000	432			
A\$ENV = 000000	432	443		
A\$ENV\$M = 000000	432	444		
A\$FATAL= 000000	432	435		
A\$ADR1= 000000	432			
A\$ADR2= 000000	432			
A\$ADR3= 000000	432			
A\$ADR4= 000000	432			
A\$AMS1= 000000	432			
A\$AMS2= 000000	432			
A\$AMS3= 000000	432			
A\$AMS4= 000000	432			
A\$MSGAD= 000000	432	440		
A\$MSGLG= 000000	432	441		
A\$MSGTY= 000000	432	434		
A\$TYP1= 000000	432			
A\$TYP2= 000000	432			
A\$TYP3= 000000	432			
A\$TYP4= 000000	432			
A\$PASS = 000000	432	437		

MACY!1 27(732) 01-OCT-76 15:03 PAGE 411  
 DFKAAB.P11 CROSS REFERENCE TABLE -- USEP SYMBOLS

APRIOC=	000000	432			
AROUND	024730	6056	8059*		
ASL1	021370	6994	6995	6996	7002*
ASL2	021400	6997	7006*		
ASL3	021416	7009	7010	7011	7017*
ASL4	021426	7012	7021*		
ASL5	021442	7024	7025	7031*	
ASL6	021452	7026	7035*		
ASL7	021476	7038	7039	7040	7041 7048*
ASR1	021540	7063	7064	7065	7071*
ASR2	021550	7066	7075*		
ASR3	021572	7079	7080	7081	7087*
ASR4	021602	7082	7091*		
ASRS	021616	7094	7095	7096	7102*
ASR6	021626	7097	7106*		
ASR7	021656	7110	7111	7112	7113 7120*
ASUREG=	000000	432	445		
ATESTIN=	000000	432	436		
AUNIT =	000000	432	439		
AUSUR =	000000	432	446		
AVECT1=	000000	432			
AVECT2=	000000	432			
BIC1	017020	6091	6092	6098*	
BIC2	017030	6093	6102*		
BIC3	017046	6105	6106	6112*	
BIS1	017110	6127	6128	6129	6135*
BIS2	017120	6130	6139*		
BIS3	017140	6142	6143	6144	6150*
BITCHK	025120	8112*			
BITCLR	025046	8098*			
BITCON	025202	8125	8134*		
BITSET	025064	8105*			
BIT1	016730	6054	6055	6061*	
BIT2	016740	6056	6066*		
BIT3	016756	6069	6070	6076*	
BRCT	024766	8043*	8073*	8079*	
BRC1	003040	1443	1449*		
BRC2	003050	1444	1454*		
BPC3	003067	1456	1462*		
BRH	024740	8044*	8064*		
BRN1	002720	1349	1355*		
BRN2	002730	1350	1360*		
BRN3	002740	1362	1368*		
BPTAB	025706	8041	8291*		
BRV1	002770	1396	1402*		
BRV2	003000	1397	1407*		
BRV3	003010	1409	1415*		
BRZ1	002650	1302	1308*		
BFZ2	002660	1303	1313*		
BRZ3	002670	1315	1321*		
BP1	000572	538	544*		
BP2	000602	539	548*		
BP3	000614	549	557*		
BP4	000622	558	564*		
BP5	000632	559	568*		
BTCON	025256	8152	8157*		

MAINDEC-11-DFKAA-B 11 34 CPU TEST MACY!1 27(732) 01-OCT-76 15:03 PAGE 412  
 DFKAA-B.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

BTERR	025242	8147	8153*					
CC	024734	9046*	8048*	8062*				
CCERR	025476	8206	8244*					
CC1	025364	8207*	8212*	8226*	8227	8229		
CC2	025400	9208*	8216*	8225*	8231*			
CLRCD	025362	8211*	8228	8232				
CLRI	017456	6307	6308	6309	6315*			
CMP1	020320	6611	6612	6618*				
CMP2	020330	6613	6622*					
CMP3	020352	6626	6627	6633*				
CMP4	020362	6628	6637*					
CMP5	020406	6641	6642	6643	6649*			
CMP6	020416	6644	6653*					
CMP7	020436	6656	6657	6663*				
COM1	020476	6679	6680	6686*				
CONT	024770	8054	8058	8074*				
CON1	025414	8217	8225*					
CON2	025506	8239	8248*					
DRERR	025172	8097	8113	8115	8117	8119	8121	8123
DEC1	017316	6230	6231	6232	6238*			
DEC2	017326	6233	6242*					
DEC3	017342	6245	6246	6252*				
DEC4	017352	6247	6256*					
DEC5	017366	6259	6260	6266*				
DEC6	017376	6261	6270*					
DEC7	017420	6274	6275	6276	6282*			
DMM80A	010520	3863	3864	3865	3871*			
DMM80B	010530	3866	3875*					
DMM82A	010756	3973	3974	3975	3981*			
DMM82B	010766	3976	3985*					
DMM82C	011002	3986	3994*					
DMM82D	011016	3995	3997	4003*				
DMM82E	011026	3998	4007*					
DMM82F	011044	4009	4017*					
DMM83A	011126	4043	4044	4045	4051*			
DMM83B	011136	4046	4055*					
DMM83C	011154	4056	4064*					
DMM83D	011172	4067	4068	4074*				
DMM83E	011202	4069	4078*					
DMM84A	011372	4145	4147	4148	4154*			
DMM84B	011402	4149	4158*					
DMM84C	011420	4159	4167*					
DMM84D	011430	4168	4174*					
DMM84E	011440	4169	4178*					
DMM84F	011454	4179	4187*					
DMM03A	007612	3472	3473	3474	3480*			
DMM03B	007622	3475	3484*					
DMM03C	007632	3485	3492*					
DMM1	007464	3406	3414*					
DMM1A	010576	3896	3897	3898	3904*			
DMM1B	010606	3899	3908*					
DMM2	007500	3415	3423*					
DMM2A	010654	3929	3930	3936*				
DMM2B	010664	3931	3940*					
DMM2C	010672	3947*						
DMM2D	010702	3942	3951*					

MAINDEC-11-DFKAR-8 11:34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 413  
DFKAR8.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

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MAINDEC-11-DFKAA-8 11:34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 414  
DFKAA8.PII CROSS REFERENCE TABLE -- USER SYMBOLS

MAINDEC-11-DFKAA-B 11:34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 415  
 DFKAA8.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

MOMSE	013054	4714	4722*	
MOMSA	013124	4751	4752	4758*
MOMSB	013134	4753	4762*	
MOMSC	013152	4763	4771*	
MOMSD	013172	4772	4780*	
MOMSE	013222	4783	4791*	
MOMSA	013276	4819	4820	4825*
MOMSB	013306	4821	4830*	
MOMSC	013324	4831	4839*	
MOMSD	013344	4840	4848*	
MOMSE	013370	4850	4858*	
MFP10	024442	7968	7973*	
MFP10A	024470	7974	7979*	
MFP51	023206	7581	7590*	
MFP52A	023275	7615	7616	7617 7623*
MFP52B	023306	7618	7627*	
MFP52C	023326	7628	7636*	
MFP53A	023404	7657	7658	7659 7665*
MFP53B	023414	7660	7669*	
MFP53C	023434	7670	7678*	
MFP54A	023512	7699	7700	7701 7707*
MFP54B	023522	7702	7711*	
MFP54C	023542	7712	7720*	
MFP55A	023620	7741	7742	7743 7749*
MFP55B	023630	7744	7753*	
MFP55C	023650	7754	7762*	
MFP56A	023730	7783	7784	7785 7791*
MFP56B	023740	7786	7795*	
MFP56C	023760	7796	7804*	
MFP57A	024040	7825	7825	7827 7833*
MFP57B	024050	7828	7837*	
MFP57C	024070	7838	7846*	
MOV1	016640	6017	6018	6024*
MOV2	016650	6019	6029*	
MOV3	016666	6032	6033	6039*
MRK1	022246	7293	7300*	
MRK2	022270	7300	7301	7302 7304 7311*
MRK3	022300	7306	7315*	
MRK4	022322	7318	7320*	
MRK5	022334	7319	7324*	
MRK6	022350	7325	7332*	
MSG	025654	8265	8285*	
MTP10	024554	7994	7999*	
MTP51	022420	7357	7365*	
MTP51A	022440	7369	7370	7371 7377*
MTP52	022514	7394	7402*	
MTP53	022604	7425	7433*	
MTP54	022672	7455	7463*	
MTP55	022752	7485	7493*	
MTP56	023042	7515	7523*	
MTP57	023132	7545	7553*	
NBR	024744	8054*	8057*	8065*
NEG00	004010	1905	1906	1907 1913*
NEG01	004020	1908	1918*	
NEG02	004034	1919	1928*	
NEG03	004050	1930	1931	1932 1938*

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MAINDEC-11-DFKAA-8 11 34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 416  
DFKAA8.PII CROSS REFERENCE TABLE -- USER SYMBOLS



MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732)  
DFKAA.B.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

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2090*	2092*	2125*	2126*	2127*	2176*	2177*	2178*	2179*	2180*	2181*	2190*	2191*
2192*	2193*	2194*	2195*	2197*	2214*	2215*	2216*	2217*	2221*	2245*	2254*	2290*
2291*	2292*	2293*	2302*	2303*	2304*	2306*	2307*	2308*	2341*	2342*	2343*	2344*
2353*	2354*	2355*	2357*	2383*	2384*	2385*	2386*	2395*	2397*	2424*	2425*	2426*
2427*	2428*	2437*	2439*	2457*	2458*	2459*	2460*	2473*	2482*	2498*	2499*	2500*
2501*	2502*	2505*	2527*	2528*	2544*	2546*	2550*	2579*	2590*	2581*	2582*	2583*
2596*	2597*	2598*	2664*	2667	2696*	2697*	2700	2728*	2729*	2732	2760*	2761*
2762*	2765	2777*	2778*	2781	2809*	2810*	2813	2826*	2827*	2852*	2853*	2854*
2857	2869*	2878*	2881	2894*	2895*	2919*	2920*	2921*	2922*	2925	2938*	2939*
2965*	2966*	2967*	2968*	2969*	2970	2973	2987	3000	3001	3025*	3026*	3027*
3030	3042	3066*	3067*	3068*	3069*	3070*	3073	3085*	3086*	3110*	3111*	3112*
3113*	3116	3128*	3152*	3153*	3154*	3155*	3158	3170*	3193*	3194*	3196	3220*
3222*	3223	3247*	3250*	3263*	3288*	3289	3298*	3299*	3301	3311	3322*	3323*
3326	3327	3337	3361*	3362*	3363*	3364*	3365*	3366	3402*	3405	3414	3423*
3424	3433*	3434*	3436	3446	3467*	3468*	3469*	3470*	3471	3484*	3486*	3510*
3511*	3515*	3538*	3539*	3540*	3542	3567*	3568*	3569*	3572	3600*	3601*	3602*
3603*	3606	3616*	3617	3641*	3642*	3646*	3647*	3671*	3672*	3673*	3674	3684*
3685*	3711*	3712*	3713*	3714*	3747*	3749*	3750*	3751*	3752	3762	3763	3788*
3789*	3790*	3814*	3815*	3816	3840*	3841*	3842	3859*	3860*	3862	3875*	3892*
3893*	3895	3908	3925*	3926*	3927*	3928	3940*	3941*	3951	3968*	3969*	3970*
3972	3985*	3994*	3995	4007*	4008*	4017	4035*	4036*	4037*	4038*	4039*	4040*
4042	4055	4064*	4065*	4066	4096*	4097*	4098*	4099*	4101	4114	4140*	4141*
4142*	4143*	4145	4158	4167	4178	4187	4204*	4205*	4206*	4207*	4209	4222
4248*	4249*	4250*	4251*	4252	4265	4291*	4292*	4293*	4294*	4295	4308	4340*
4341*	4342*	4344	4379*	4380*	4381*	4382*	4394*	4395*	4427*	4428*	4429*	4441
4450*	4462	4493*	4494*	4496*	4508	4560*	4561*	4584	4611*	4612*	4613	4631*
4643	4680*	4681*	4693	4711*	4712*	4713	4747*	4748*	4749*	4750*	4762	4780*
4781*	4782	4817*	4818*	4830	4848*	4849	4887*	4888	4889	4890	4891	4892
4925*	4926	4927	4928	4929	4930	4962*	4963	4964	4965	4966	4967	4993*
4994	4995	4996	4997	4998	5022*	5024*	5027	5037*	5039*	5042	5069*	5070*
5072*	5086*	5087*	5100*	5101*	5102*	5104*	5132*	5133*	5135*	5139*	5140*	5150*
5151*	5153*	5157*	5167*	5168*	5169*	5171*	5175*	5176*	5260*	5262*	5266	5295*
5298*	5302	5389*	5390*	5399	5424*	5425*	5452*	5453*	5463*	5516*	5517*	5527
5554*	5556*	5566	5597*	5598*	5599	5530*	5631*	5632	5685*	5686	5687	5705*
5707	5720*	5721	5722	5740*	5742	5753*	5755	5766*	5768	5780*	5782	5823*
5827	5843	5875*	5876	5891*	5892	5898	5914	5925*	5926	5977*	5978*	5984
6016*	6031*	6050*	6053	6068	6087*	6090*	6104*	6123*	6126*	6141*	6173*	6176*
6188*	6191*	6207*	6227*	6229*	6244*	6258*	6270*	6273*	6306*	6329	6342*	6345
6364*	6367*	6381*	6411*	6413*	6427*	6441*	6453*	6467*	6488*	6491*	6503*	6506*
6520*	6551*	6554*	6567*	6570*	6583*	6586*	6607*	6610	6622*	6625	6637*	6640
6653*	6655	6675*	6678*	6709*	6712*	6724*	6727*	6739*	6742*	6756*	6776*	6779*
6794*	6809*	6822*	6825*	6855*	6858*	6873*	6888*	6902*	6906	6923*	6926*	6941*
6956*	6971*	6990*	6993*	7008*	7023*	7037*	7042	7059*	7062*	7075*	7078*	7093*
7106*	7109*	7114	7142*	7145*	7150	7160*	7161*	7162*	7165*	7170	7195*	7199*
7204	7217*	7222	7246*	7247	7262*	7353*	7355*	7365*	7366*	7368*	7389*	7390*
7392*	7402	7419*	7420*	7423*	7433	7450*	7453*	7463	7480*	7483*	7493	7511*
7513*	7523	7541*	7543*	7553	7579*	7580	7590*	7593*	7611*	7612*	7614*	7636
7653*	7656*	7678	7695*	7698*	7720	7737*	7740*	7762	7779*	7782*	7804	7821*
7824*	7846	8041*	8044	8098*	8105*	8124	8150*	8151	8265*	8268	8270	8272*
8275	8333*	8336										
906*	911*	930*	935*	937	5825*	5826*	5827*	5837	5854*	5858	5873*	5876*
5880	5892*	5896	5909*	5912	5926*	5930	5941*	5949	7196*	7199	7214	3045*
8049	2059*	8099*	8106*	8122								
934	513*											
516*	527*	534*	535	545*	546*	554*	555*	565*	566*	574*	575*	596*
597	601*	608*	615*	616	626*	627*	634*	635	645*	646*	653*	654

663*	664*	686*	687	698*	699*	706*	707	717*	718*	727*	728*	735*
736	751*	752*	759*	760	771*	772*	779*	780	795*	796*	830*	831
841*	842*	849*	850	859*	860*	867*	868	877*	878*	885*	886	895*
896*	903*	904	919*	920*	927*	928	944*	945*	951*	952	954*	959*
966*	967*	968*	970*	975*	976	978*	983*	985	987*	989*	990*	992*
997*	998	1013*	1014*	1021*	1022	1038*	1039*	1046*	1047	1062*	1063*	1070*
1071	1087*	1088*	1096*	1097	1112*	1113*	1120*	1121	1137*	1138*	1145*	1146
1161*	1162*	1169*	1170	1186*	1187*	1209*	1210	1220*	1221*	1228*	1229	1238*
1239*	1246*	1247	1256*	1257*	1264*	1265	1274*	1275*	1296*	1297	1309*	1310*
1322*	1323*	1343*	1344	1356*	1357*	1369*	1370*	1390*	1391	1403*	1404*	1416*
1417*	1437*	1438	1450*	1451*	1463*	1464*	1506*	1507	1515*	1516*	1526*	1527*
1535*	1536*	1553*	1554	1563*	1564*	1581*	1582*	1595*	1596	1604*	1605*	1616*
1617*	1632*	1633	1642*	1643*	1655*	1656*	1670*	1671	1682*	1683*	1697*	1698*
1715*	1716	1728*	1729*	1744*	1745*	1762*	1763	1776*	1777*	1792*	1793*	1810*
1811	1824*	1825*	1840*	1841*	1853*	1854	1868*	1869*	1986*	1887*	1899*	1900
1914*	1915*	1924*	1925*	1939*	1940*	1948*	1949*	1955*	1956	1971*	1972*	1981*
1982*	1995*	1996*	2004*	2005*	2011*	2012	2027*	2028*	2041*	2042*	2050*	2051*
2072*	2073	2085*	2086*	2099*	2100*	2119*	2120	2134*	2135*	2152*	2153*	2173*
2174	2187*	2188*	2204*	2205*	2211*	2212	2231*	2232*	2240*	2241*	2251*	2252*
2260*	2261*	2271*	2272*	2287*	2288	2299*	2300*	2315*	2316*	2338*	2339	2350*
2351*	2364*	2365*	2380*	2381	2392*	2393*	2404*	2405*	2421*	2422	2434*	2435*
2446*	2447*	2454*	2455	2470*	2471*	2479*	2480*	2488*	2499*	2495*	2496	2515*
2516*	2524*	2525*	2534*	2535*	2541*	2542	2560*	2561*	2634*	2570*	2576*	2577
2593*	2594*	2605*	2606*	2621*	2622	2631*	2632*	2644*	2645*	2661*	2662	2677*
2678*	2693*	2694	2709*	2710*	2725*	2726	2742*	2743*	2757*	2758	2774*	2775*
2791*	2792*	2806*	2807	2823*	2824*	2833*	2834*	2849*	2850	2866*	2867*	2875*
2876*	2891*	2892*	2901*	2902*	2916*	2917	2935*	2936*	2945*	2946*	2962*	2963
2982*	2983*	2997*	2998*	3007*	3008*	3022*	3023	3039*	3040*	3048*	3049*	3063*
3064	3082*	3083*	3092*	3093*	3107*	3108	3125*	3126*	3134*	3135*	3149*	3150
3167*	3168*	3176*	3177*	3190*	3191	3203*	3204*	3217*	3218	3230*	3231*	3244*
3245	3260*	3261*	3269*	3270*	3285*	3286	3295*	3296*	3308*	3309*	3319*	3320*
3334*	3335*	3345*	3346*	3358*	3359	3376*	3377*	3386*	3387*	3399*	3400	3411*
3412*	3420*	3421*	3430*	3431*	3442*	3443*	3452*	3453*	3464*	3465	3481*	3482*
3493*	3494*	3507*	3508	3521*	3522*	3535*	3536	3549*	3550*	3564*	3565	3578*
3579*	3597*	3598	3613*	3614*	3623*	3624*	3638*	3639	3653*	3654*	3668*	3669
3681*	3682*	3691*	3692*	3708*	3709	3721*	3722*	3730*	3731*	3744*	3745	3759*
3760*	3769*	3770*	3784*	3785	3796*	3797*	3810*	3811	3822*	3823*	3836*	3837
3848*	3849*	3856*	3857	3872*	3873*	3881*	3882*	3889*	3890	3905*	3906*	3914*
3915*	3922*	3923	3937*	3938*	3948*	3949*	3957*	3958*	3965*	3966	3982*	3983*
3991*	3992*	4004*	4005*	4014*	4015*	4023*	4024*	4032*	4033	4052*	4053*	4061*
4062*	4075*	4076*	4085*	4086*	4093*	4094	4111*	4112*	4120*	4121*	4129*	4130*
4137*	4138	4155*	4156*	4164*	4165*	4175*	4176*	4184*	4185*	4193*	4194*	4201*
4202	4219*	4220*	4228*	4229*	4237*	4238*	4245*	4246	4262*	4263*	4271*	4272*
4280*	4281*	4288*	4289	4305*	4306*	4314*	4315*	4323*	4324*	4337*	4338	4353*
4354*	4362*	4363*	4376*	4377	4391*	4392*	4402*	4403*	4411*	4412*	4424*	4425
4438*	4439*	4447*	4448*	4459*	4460*	4468*	4469*	4477*	4478*	4490*	4491	4505*
4506*	4514*	4515*	4523*	4524*	4533*	4534*	4543*	4544*	4557*	4558	4572*	4573*
4581*	4582*	4590*	4591*	4606*	4607	4619*	4620*	4628*	4629*	4640*	4641*	4649*
4650*	4658*	4659*	4675*	4676	4690*	4691*	4699*	4700*	4708*	4709*	4719*	4720*
4728*	4729*	4744*	4745	4759*	4760*	4768*	4769*	4777*	4778*	4788*	4789*	4797*
4798*	4812*	4813	4827*	4828*	4836*	4837*	4845*	4846*	4855*	4856*	4864*	4865*
4884*	4885	4899*	4900*	4922*	4923	4937*	4938*	4959*	4960	4973*	4974*	4990*
4991	5004*	5005*	5019*	5020	5034*	5035*	5049*	5050*	5066*	5067	5082*	5083*
5097*	5098*	5114*	5115*	5129*	5130	5147*	5148*	5164*	5165*	5183*	5184*	5198*
5199	5212*	5213*	5226*	5227*	5240*	5241*	5256*	5257	5273*	5274*	5291*	5292
5309*	5310*	5325*	5326	5339*	5340*	5354*	5355	5369*	5370*	5386*	5387	5396*

MAINDEC-11-DFKAA-B 11 34 CPU TEST MACY11 27(732)  
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5397*	5405*	5406*	5420*	5421	5432*	5433*	5449*	5449	5460*	5461*	5469*	5470*
5485*	5486	5496*	5497*	5512*	5513	5524*	5525*	5533*	5534*	5551*	5552	5563*
5564*	5573*	5574*	5593*	5594	5606*	5607*	5626*	5627	5639*	5640*	5681*	5682
5693*	5694*	5702*	5703*	5716*	5717*	5728*	5729*	5737*	5738*	5750*	5751*	5763*
5764*	5777*	5778*	5791*	5792*	5816*	5817	5831*	5832*	5850*	5851*	5869*	5870*
5987*	5888*	5905*	5906*	5921*	5922*	5937*	5938*	5956*	5957*	5972*	5973	5981*
5982*	5990*	5991*	6011*	6012	6025*	6026*	6040*	6041*	6047*	6048	6062*	6063*
6077*	6078*	6084*	6085	6099*	6100*	6113*	6114*	6120*	6121	6136*	6137*	6151*
6152*	6170*	6171	6185*	6186*	6201*	6202*	6216*	6217*	6224*	6225	6239*	6240*
6253*	6254*	6267*	6268*	6283*	6284*	6301*	6302	6316*	6317*	6324*	6325	6339*
6340*	6354*	6355*	6361*	6362	6376*	6377*	6391*	6392*	6408*	6409	6422*	6423*
6436*	6437*	6450*	6451*	6462*	6463*	6477*	6478*	6485*	6486	6500*	6501*	6515*
6516*	6530*	6531*	6548*	6549	6564*	6565*	6580*	6581*	6596*	6597*	6604*	6605
6619*	6620*	6634*	6635*	6650*	6651*	6664*	6665*	6672*	6673	6687*	6688*	6706*
6707	6721*	6722*	6736*	6737*	6751*	6752*	6766*	6767*	6773*	6774	6789*	6790*
6804*	6805*	6819*	6820*	6834*	6835*	6852*	6853	6868*	6869*	6883*	6884*	6897*
6898*	6913*	6914*	6920*	6921	6936*	6937*	6951*	6952*	6966*	6967*	6980*	6981*
6987*	6988	7003*	7004*	7018*	7019*	7032*	7033*	7049*	7050*	7056*	7057	7072*
7073*	7088*	7089*	7103*	7104*	7121*	7122*	7139*	7140	7157*	7158*	7177*	7178*
7192*	7193	7211*	7212*	7229*	7230*	7243*	7244	7257*	7258*	7273*	7274*	7287*
7288	7297*	7298*	7312*	7313*	7321*	7322*	7333*	7334*	7350*	7351	7362*	7363*
7378*	7379*	7386*	7387	7399*	7400*	7408*	7409*	7416*	7417	7430*	7431*	7439*
7440*	7447*	7448	7460*	7461*	7469*	7470*	7477*	7478	7490*	7491*	7499*	7500*
7507*	7508	7520*	7521*	7529*	7530*	7537*	7538	7550*	7551*	7559*	7560*	7575*
7576	7586*	7587*	7600*	7601*	7608*	7609	7624*	7625*	7633*	7634*	7642*	7643*
7650*	7651	7666*	7667*	7675*	7676*	7684*	7685*	7692*	7693	7708*	7709*	7717*
7718*	7726*	7727*	7734*	7735	7750*	7751*	7759*	7760*	7768*	7769*	7776*	7777
7792*	7793*	7801*	7802*	7810*	7811*	7818*	7819	7834*	7835*	7843*	7844*	7852*
7853*	7868*	7869	7881*	7882*	7895*	7896	7905*	7906*	7920*	7921	7928*	7929*
7938*	7939*	7945*	7946*	7960*	7961	7970*	7971*	7976*	7977*	7984*	7985	7996*
7997*	8006*	8007*	8038*	8039	8069*	8070*	8071*	8095*	8096	8100*	8107*	8120
8131*	8132*	8134*	8145*	8146	8154*	8155*	8168*	8169	8183*	8184*	8204*	8205
8222*	8223*	8245*	8246*	8255*	8256	8281*	8282*	8353*	8354*	8357*	8358*	8361*
8362*	8365*	8366*	8369*	8370*	8373*	8374*	8377*	8378*	8381*	8382*		

R2ERR 001742

R3 =%000003

R3ERR 002062  
DU - 1000000

R4 =%000004

**1000\***   **1005\***   **1024\***   **1029\***   **1031**   **8047\***   **8074\***   **8101\***   **8108\***   **8118**

**1028**    **1037**    **1032x**    **1030x**    **1029**    **2122x**    **2122x**    **2120x**    **2120x**    **2122x**    **2120x**    **2120x**    **2111x**

~~1049\*~~ ~~1054\*~~ ~~1073\*~~ ~~1078\*~~ ~~1080~~ ~~2122\*~~ ~~2123\*~~ ~~2124\*~~ ~~2128\*~~ ~~2137\*~~ ~~2138\*~~ ~~2139\*~~ ~~2141\*~~  
~~2142\*~~ ~~2144\*~~ ~~2145\*~~ ~~2218\*~~ ~~2219\*~~ ~~2220\*~~ ~~2224\*~~ ~~2225\*~~ ~~2E02\*~~ ~~2E04\*~~ ~~2E18\*~~ ~~2E4E\*~~ ~~2E42\*~~

2143\* 2144\* 2145\* 2218\* 2219\* 2220\* 2234\* 2265\* 2503\* 2504\* 2518\* 2545\* 2547\*  
2548\* 2549\* 2563\* 3195\* 3196\* 3197\* 3221\* 3223\* 3224\* 3248\* 3249\* 3250 3289\*

~~E348\*~~ ~~E349\*~~ ~~E383\*~~ ~~J135\*~~ ~~J158\*~~ ~~J197\*~~ ~~J221\*~~ ~~J223\*~~ ~~J224\*~~ ~~J248\*~~ ~~J249\*~~ ~~J250\*~~ ~~J283\*~~  
~~3300\*~~ ~~3301\*~~ ~~3302\*~~ ~~3311\*~~ ~~3312\*~~ ~~3313\*~~ ~~3324\*~~ ~~3325\*~~ ~~3326\*~~ ~~3327\*~~ ~~3328\*~~ ~~3337\*~~ ~~3338\*~~

**3388\***   **3381\***   **3382\***   **3311\***   **3312\***   **3313\***   **3321\***   **3323\***   **3328\***   **3327\***   **3328\***   **3327\***   **3328\***

**3515**   **3541\***   **3542\***   **3543\***   **3570\***   **3571\***   **3572**   **3604\***   **3605\***   **3606\***   **3607**   **3617\***   **3643\***

**3644\***   **3645\***   **3646**   **3674\***   **3675\***   **3748\***   **3752\***   **3753\***   **4078\***   **4079**   **4343\***   **4344\***   **4356**

**4562\***   **4563\***   **4575**   **4609\***   **4610\***   **4622**   **4652**   **4678\***   **4679\***   **4702**   **4722**   **4815\***   **4816\***  
~~2211x~~   ~~2212~~   ~~2243x~~   ~~2268x~~   ~~2266~~   ~~2242x~~   ~~2245~~   ~~2122x~~   ~~2128x~~   ~~2115~~   ~~2212x~~   ~~2211x~~   ~~2215~~

7214\* 7217 7247\* 7260\* 7266 8042\* 8045 8102\* 8109\* 8116 8213\* 8214\* 8215  
8235\* 8236\* 8237

~~8235\*~~ 8236\* 8237  
~~1072~~ 1086\*

1077 1088 1099\* 1104\* 1123\* 1128\* 1130 7293\* 7303 7317\* 7320\* 7326 8050\* 8051\* 8052

**8075\***   **8076\***   **8077**   **8080\***   **8081\***   **8082**   **8103\***   **8110\***   **8114**

**1127**      **1136**      1141      1142      1143      1144      1145      1146      1147      1148      1149      1150      1151      1152

411\* 515\* 526\* 1148\* 1153\* 1172\* 1177\* 1179 1212\* 5822\* 5839 5841 5860

R6 =%000006

**5862**   **5872\***   **5975\***   **5976\***   **7305**   **7324**   **7899\***   **7901\***   **7924\***   **7925**   **7932**   **7941\***   **7943**  
~~7848\*~~   ~~7850\*~~   ~~7863\*~~   ~~7865\*~~   ~~7866~~   ~~7888\*~~   ~~7890\*~~   ~~7891\*~~   ~~7892\*~~   ~~8000~~   ~~8104\*~~   ~~8111\*~~   ~~8113~~

7948 7950 7953 7955 7956 7958 7959 7960 7961 7962 8000 8104 8111 8112

~~8330\*~~      1176      1185\*

R6ERR 002426

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MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 421  
 DFKAA8.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

R7	=%000007	410*	2624*		
SBC1	020712	6790	6781	6782	6788*
SBC2	020722	6783	6792*		
SBC3	020740	6795	6796	6797	6803*
SBC4	020750	6798	6807*		
SBC5	020766	6810	6811	6812	6818*
SBC6	020776	6813	6822*		
SBC7	021016	6826	6827	6833*	
SBO	015022	5391	5399*		
SB2	015144	5455	5463*		
SB4	015270	5519	5527*		
SB5	015356	5553	5572*		
SB5A	015350	5558	5566*		
SB5X	015366	5555*	5557	5577*	5578
SB5XAD	015370	5554	5566	5578*	
SB6	015430	5595	5605*		
SB6X	015440	5596*	5597	5610*	
SB7	015500	5628	5638*		
SB7X	015510	5629*	5643*	5644	
SB7XAD	015512	5630	5644*		
SCOPE =	000240	409*			
SC3	025456	8209*	8234*	8249*	8250
SC4	025472	8210*	8238*	8248*	
SETBR	024624	8044*	8083		
SETCC	024644	8048*	8078		
SETCD	025454	8230	8233*	8251	
SETUP	024606	8041*			
SET2BR	024714	8053	8057*		
SHL	001200	741*	744		
SHLE	001214	742	750*		
SHR	001314	785*	788		
SHRE	001330	786	794*		
SNMB0A	005754	2701	2702	2708*	
SNMB1A	006060	2766	2767	2773*	
SNMB1B	006070	2768	2777*		
SNMB1C	006112	2782	2783	2784	2790*
SNMB2A	006234	2858	2859	2865*	
SNMB2B	006244	2860	2869*		
SNMB2C	006260	2870	2878*		
SNMB2D	006300	2882	2883	2884	2890*
SNMB2E	006310	2885	2894*		
SNMB3A	006452	2974	2975	2981*	
SNMB3B	006462	2976	2985*		
SNMB3C	006500	2988	2989	2990	2996*
SNMB3D	006510	2991	3000*		
SNM0A	005711	2668	2669	2670	2676*
SNM1A	006016	2733	2734	2735	2741*
SNM2A	006154	2814	2815	2816	2822*
SNM2B	006164	2817	2826*		
SNM3A	006364	2926	2927	2928	2934*
SNM3B	006374	2929	2938*		
SNM4A	006560	3031	3032	3038*	
SNM4B	006570	3033	3042*		
SNM5A	006642	3074	3075	3081*	
SNM5B	006652	3076	3085*		
SNM6A	006726	3117	3118	3124*	

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DFKAAB.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

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DFKAAB.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

MAINDEC-11-DFKAB-8 11 34 CPU TEST  
 MACY11 27(732) 01-OCT-76 15:03 PAGE 424  
 DFKAB8.P114 CROSS REFERENCE TABLE -- USER SYMBOLS

TST134	013622	3891	3909	3922*
TST135	010720	3924	3952	3965*
TST136	011062	3967	4018	4032*
TST137	011222	4034	4080	4093*
TST14	001320	832	836	849*
TST140	011330	4095	4124	4137*
TST141	011472	4139	4188	4201*
TST142	011602	4203	4232	4245*
TST143	011710	4247	4275	4288*
TST144	012020	4290	4318	4337*
TST145	012074	4339	4357	4376*
TST146	012166	4378	4406	4424*
TST147	012322	4426	4472	4490*
TST148	001422	951	854	867*
TST150	012500	4492	4538	4557*
TST151	012574	4559	4585	4606*
TST152	012730	4608	4653	4675*
TST153	013072	4677	4723	4744*
TST154	013242	4746	4792	4812*
TST155	013410	4814	4859	4884*
TST156	013474	4893	4922*	
TST157	013560	4931	4959*	
TST158	001454	869	672	885*
TST160	013644	4961	4968	4990*
TST161	013730	4992	4999	5019*
TST162	014024	5021	5043	5066*
TST163	014166	5068	5108	5129*
TST164	014344	5131	5177	5198*
TST165	014506	5200	5234	5256*
TST166	014562	5258	5267	5291*
TST167	014646	5303	5325*	
TST168	001506	887	890	903*
TST170	014714	5327	5333	5354*
TST171	014772	5363	5386*	
TST172	015040	5388	5400	5420*
TST173	015102	5422	5427	5448*
TST174	015162	5450	5464	5485*
TST175	015224	5487	5491	5512*
TST176	015304	5514	5528	5551*
TST177	015372	5567	5593*	
TST2	000644	536	569	596*
TST20	001552	905	913	927*
TST200	015442	5600	5626*	
TST201	015514	5633	5681*	
TST202	016060	5786	5816*	
TST203	016536	5950	5972*	
TST204	016612	5974	5985	6011*
TST205	016676	6013	6034	6047*
TST206	016766	6049	6071	6084*
TST207	017056	6086	6107	6120*
TST21	001622	929	938	951*
TST210	017150	6122	6145	6170*
TST211	017266	6172	6210	6224*
TST212	017430	6226	6277	6301*
TST213	017466	6303	6310	6324*
TST214	017552	6326	6348	6361*

TST215	017640	6363	6385	6408*
TST216	020024	6410	6471	6485*
TST217	020142	6487	6524	6548*
TST22	001676	975*		
TST220	020256	6550	6590	6604*
TST221	020446	6506	6658	6672*
TST222	020506	6674	6681	6706*
TST223	020660	6708	6760	6773*
TST224	021026	6775	6828	6852*
TST225	021174	5854	6907	6920*
TST226	021336	6922	6974	6987*
TST227	021506	6989	7043	7056*
TST23	001756	977	997*	
TST230	021666	7058	7115	7139*
TST231	021774	7141	7171	7192*
TST232	022106	7194	7223	7243*
TST233	022174	7245	7267	7287*
TST234	022360	7289	7327	7350*
TST235	022450	7352	7372	7386*
TST236	022532	7388	7403	7416*
TST237	022622	7418	7434	7447*
TST24	002022	999	1007	1021*
TST240	022706	7449	7464	7477*
TST241	022770	7479	7494	7507*
TST242	023060	7509	7524	7537*
TST243	023150	7539	7554	7575*
TST244	023242	7577	7595	7608*
TST245	023344	7610	7637	7650*
TST246	023452	7652	7679	7692*
TST247	023560	7694	7721	7734*
TST25	002072	1023	1032	1046*
TST250	023666	7735	7763	7776*
TST251	023776	7778	7805	7818*
TST252	024106	7820	7847	7868*
TST253	024156	7870	7876	7895*
TST254	024226	7997	7920*	
TST255	024364	7960*		
TST256	024470	7962	7984*	
TST257	024576	7986	8001	8038*
TST26	002136	1048	1056	1070*
TST260	025036	8095*		
TST261	025206	8145*		
TST262	025262	8168*		
TST263	025322	8170	8177	8204*
TST264	025526	8255*		
TST27	002206	1072	1081	1096*
TST3	000700	598	602	615*
TST30	002252	1098	1106	1120*
TST31	002322	1122	1131	1145*
TST32	002366	1147	1155	1169*
TST33	002436	1171	1180	1209*
TST34	002476	1211	1215	1228*
TST35	002534	1230	1233	1246*
TST36	002572	1248	1251	1264*
TST37	002630	1266	1269	1296*
TST4	000736	617	621	634*



SERN = 000632	4048	545	546	554	555	565	566	574	575	607	608	626	627
	645	646	663	664	698	899	717	718	727	728	751	752	771
	728	795	796	841	842	859	860	977	878	895	896	919	920
	944	945	96	968	986	996	1013	1014	1038	1039	1062	1063	1087
	1088	1112	1113	1137	1138	1161	1162	1186	1187	1220	1221	1238	1239
	1256	1257	1274	1275	1309	1310	1322	1323	1356	1357	1369	1370	1403
	1404	1416	1417	1450	1451	1463	1464	1515	1515	1526	1527	1535	1536
	1563	1564	1581	1582	1604	1605	1616	1617	1642	1643	1655	1656	1632
	1683	1697	1698	1728	1729	1744	1745	1776	1777	1792	1793	1824	1825
	1840	1841	1868	1869	1886	1887	1914	1915	1924	1925	1939	1940	1948
	1949	1971	1972	1981	1982	1995	1996	2004	2005	2027	2028	2041	2042
	2050	2051	2085	2086	2099	2100	2134	2135	2152	2153	2187	2188	2204
	2205	2231	2232	2240	2241	2251	2252	2260	2261	2271	2272	2299	2300
	2315	2316	2350	2351	2364	2365	2392	2393	2404	2405	2434	2435	2446
	2447	2470	2471	2479	2480	2488	2484	2515	2516	2524	2525	2534	2535
	2560	2561	2569	2570	2593	2594	2605	2606	2631	2632	2644	2645	2677
	2678	2709	2710	2742	2743	2774	2775	2791	2792	2823	2824	2833	2834
	2866	2867	2875	2876	2891	2892	2901	2902	2935	2936	2945	2946	2982
	2983	2997	2998	3007	3008	3039	3040	3048	3049	3082	3083	3092	3093
	3125	3126	3134	3135	3167	3168	3176	3177	3203	3204	3230	3231	3260
	3261	3269	3270	3295	3296	3308	3309	3319	3320	3334	3335	3345	3346
	3376	3377	3386	3387	3411	3412	3420	3421	3432	3431	3442	3443	3452
	3453	3481	3482	3493	3494	3521	3522	3549	3550	3578	3579	3613	3614
	3623	3624	3653	3654	3681	3682	3691	3692	3721	3722	3730	3731	3759
	3760	3769	3770	3796	3797	3822	3823	3848	3849	3872	3873	3881	3882
	3905	3906	3914	3915	3937	3938	3948	3949	3957	3958	3992	3993	3994
	3992	4004	4005	4014	4015	4023	4024	4052	4053	4061	4062	4075	4076
	4085	4086	4111	4112	4120	4121	4129	4130	4155	4156	4164	4165	4175
	4176	4184	4185	4193	4194	4219	4220	4228	4229	4237	4238	4262	4263
	4271	4272	4280	4281	4305	4306	4314	4315	4323	4324	4353	4354	4362
	4363	4391	4392	4402	4403	4411	4412	4438	4439	4447	4448	4459	4460
	4469	4469	4477	4478	4505	4506	4514	4515	4523	4524	4533	4534	4543
	4544	4572	4573	4581	4582	4590	4591	4619	4620	4628	4629	4640	4641
	4649	4650	4658	4659	4690	4691	4699	4700	4708	4709	4719	4720	4728
	4729	4759	4760	4768	4769	4777	4778	4788	4789	4797	4798	4827	4828
	4936	4937	4945	4946	4955	4956	4964	4965	4989	4990	4993	4998	4999
	4974	5004	5005	5034	5035	5049	5050	5082	5083	5097	5098	5114	5115
	5147	5148	5164	5165	5183	5184	5212	5213	5226	5227	5240	5241	5273
	5274	5309	5310	5339	5340	5369	5370	5396	5397	5405	5406	5432	5433
	5460	5461	5469	5470	5496	5497	5524	5525	5533	5534	5563	5564	5573
	5574	5606	5607	5639	5640	5693	5694	5702	5703	5716	5717	5728	5729
	5737	5738	5750	5751	5763	5764	5777	5778	5791	5792	5831	5832	5850
	5851	5869	5870	5887	5888	5905	5906	5921	5922	5937	5938	5956	5957
	5981	5982	5990	5991	6025	6026	6040	6041	6062	6063	6077	6078	6099
	6100	6113	6114	6136	6137	6151	6152	6185	6186	6201	6202	6216	6217
	6239	6240	6253	6254	6267	6268	6283	6284	6316	6317	6339	6340	6354
	6355	6376	6377	6391	6392	6422	6423	6436	6437	6450	6451	6462	6463
	6477	6478	6500	6501	6515	6516	6530	6531	6564	6565	6580	6581	6596
	6597	6619	6620	6634	6635	6650	6651	6664	6665	6687	6688	6721	6722
	6736	6737	6751	6752	6766	6767	6789	6790	6804	6805	6819	6820	6834
	6835	6868	6869	6883	6884	6897	6898	6913	6914	6936	6937	6951	6952
	6966	6967	6980	6981	7003	7004	7018	7019	7032	7033	7049	7050	7072
	7073	7088	7089	7103	7104	7121	7122	7157	7158	7177	7178	7211	7212
	7229	7230	7257	7258	7273	7274	7297	7298	7312	7313	7321	7322	7333
	7334	7362	7363	7378	7379	7399	7400	7408	7409	7430	7431	7439	7440
	7460	7461	7469	7470	7490	7491	7499	7500	7520	7521	7529	7530	7550

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MAINDEC-11-DFKAA-8 11:34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 428  
DFKAA8.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

SERROR=	000302	7551*	7559	7560*	7586	7587*	7600	7601*	7624	7625*	7633	7634*	7642	7643*
SETABL	000320	7666	7667*	7675	7676*	7684	7695*	7708	7709*	7717	7718*	7726	7727*	7750
SETEND	000330	7751*	7759	7760*	7768	7769*	7792	7793*	7801	7802*	7810	7811*	7834	7835*
SFATAL	000302	7843	7844*	7852	7853*	7881	7882*	7905	7906*	7928	7929*	7938	7939*	7945
SHIBTS	000330	7946*	7970	7971*	7976	7977*	7996	7997*	8006	8007*	8070	8071*	8131	8132*
SMAIL	000300	8154	8155*	8183	8184*	8222	8223*	8245	8246*	8281	8282*	8353	8354*	8357
SMBADR	000332	8358*	8361	8362*	8365	8366*	8369	8370*	8373	8374*	8377	8378*	8361	8382*
SMMSGD	000314	442*	454*	472*	521									
SMMSGLG	000316													
SMMSGTY	000300													
SPASS	000306													
SPASTM	000336													
SSVPC =	000400													
SSWR =	000000													
SSWREG	000322													
STESTN	000304													
STN =	000265													
404*	404*	516	522	527	569	593	599*	602	612	618*	621	631	637*	640
650	656*	658	683	689*	693	700	709*	712	722	732	738*	745		
756	762*	766	776	782*	789	800	806*	813	836	846	852*	854	864	
870*	872	882	888*	890	900	906*	913	924	930*	938	948	954*		
972	978*	994	1000*	1007	1018	1024*	1032	1043	1049*	1056	1067	1073*		
1081	1093	1099*	1106	1117	1123*	1131	1142	1148*	1155	1166	1172*	1180		
1206	1212*	1215	1225	1231*	1233	1243	1249*	1251	1261	1267*	1269	1293		
1299*	1316	1340	1346*	1363	1387	1393*	1410	1434	1440*	1457	1503	1509*		
1530	1550	1556*	1575	1592	1598*	1610	1629	1635*	1649	1667	1673*	1691		
1712	1718*	1738	1759	1765*	1786	1807	1813*	1834	1850	1856*	1880	1896		
1902*	1943	1952	1958*	1999	2008	2014*	2045	2069	2075*	2093	2116	2122*		
2146	2170	2176*	2198	2208	2214*	2266	2284	2290*	2309	2335	2341*	2358		
2377	2383*	2398	2418	2424*	2440	2451	2457*	2483	2492	2498*	2529	2538		
2544*	2564	2573	2579*	2600	2618	2624*	2638	2658	2664*	2671	2690	2696*		
2703	2722	2728*	2736	2754	2760*	2785	2803	2809*	2828	2846	2852*	2896		
2913	2919*	2940	2959	2965*	3002	3019	3025*	3043	3060	3066*	3087	3104		
3110*	3129	3146	3152*	3171	3187	3193*	3198	3214	3220*	3225	3241	3247*		
3264	3282	3288*	3340	3355	3361*	3381	3396	3402*	3447	3461	3467*	3487		
3504	3510*	3516	3532	3538*	3544	3561	3567*	3573	3594	3600*	3618	3635		
3641*	3648	3665	3671*	3686	3705	3711*	3725	3741	3747*	3764	3781	3787*		
3791	3807	3813*	3817	3833	3839*	3843	3853	3859*	3876	3886	3892*	3909		
3919	3925*	3952	3962	3968*	4018	4029	4035*	4080	4090	4096*	4124	4134		
4140*	4188	4198	4204*	4232	4242	4242*	4275	4285	4291*	4318	4334	4340*		
4357	4373	4379*	4406	4421	4427*	4472	4487	4493*	4538	4554	4560*	4585		
4603	4609*	4653	4672	4678*	4723	4741	4747*	4792	4809	4815*	4859	4881		
4887*	4893	4919	4925*	4931	4956	4962*	4968	4987	4993*	4999	5016	5022*		
5043	5063	5069*	5108	5126	5132*	5177	5195	5201*	5234	5253	5259*	5267		
5288	5294*	5303	5322	5328*	5333	5351	5357*	5363	5383	5389*	5400	5417		
5423*	5427	5445	5451*	5464	5482	5488*	5491	5509	5515*	5528	5548	5554*		
5567	5590	5596*	5600	5623	5629*	5633	5678	5684*	5786	5813	5819*	5950		
5969	5975*	5985	6008	6014*	6034	6044	6050*	6071	6081	6087*	6107	6117		
6123*	6145	6167	6173*	6210	6221	6227*	6277	6298	6304*	6310	6321	6327*		
6348	6358	6364*	6385	6405	6411*	6471	6482	6488*	6524	6545	6551*	6590		

6601	6607*	6658	6669	6675*	6681	6703	6709*	6760	6770	6776*	6828	6849
6855*	6907	6917	6923*	6974	6994	6990*	7043	7053	7059*	7115	7136	7142*
7171	7189	7195*	7223	7240	7246*	7267	7284	7290*	7327	7347	7353*	7372
7383	7389*	7403	7413	7419*	7434	7444	7450*	7464	7474	7480*	7494	7504
7510*	7524	7534	7540*	7554	7572	7578*	7595	7605	7611*	7637	7647	7653*
7679	7689	7695*	7721	7731	7737*	7763	7773	7779*	7805	7815	7821*	7947
7865	7871*	7876	7892	7898*	7917	7923*	7957	7963*	7981	7987*	8001	8035
8041*	8092	8098*	8142	8148*	8165	8171*	8177	8201	8207*	8252	8258*	
STSTM	000334	474*										
S*STNM=	000304	522*	528*									
SUNIT	000312	439*										
SJNITM	000340	476*										
SUSRW	000324	446*										
SX	= C25536											
537*	552	572	599*	605	618*	624	637*	643	656*	661	689*	696
709*	715	725	738*	748	762*	769	782*	792	833*	839	852*	957
870*	875	888*	893	906*	916	930*	941	954*	978*	1000*	1010	1024*
1035	1049*	1059	1073*	1084	1099*	1109	1123*	1134	1148*	1158	1172*	1183
1212*	1218	1231*	1236	1249*	1254	1267*	1272	1299*	1306	1319	1346*	1353
1366	1393*	1400	1413	1440*	1447	1460	1509*	1513	1524	1533	1556*	1561
1578	1598*	1602	1613	1635*	1640	1652	1673*	1680	1694	1718*	1726	1741
1765*	1774	1789	1813*	1822	1837	1856*	1866	1883	1902*	1911	1922	1936
1946	1958*	1968	1979	1992	2002	2014*	2024	2039	2048	2075*	2083	2096
2122*	2132	2149	2176*	2185	2201	2214*	2228	2238	2249	2258	2269	2290*
2297	2312	2341*	2348	2361	2383*	2390	2401	2424*	2432	2443	2457*	2467
2477	2486	2498*	2512	2522	2532	2544*	2557	2567	2579*	2590	2603	2624*
2629	2641	2664*	2674	2696*	2706	2728*	2739	2760*	2771	2788	2809*	2820
2831	2852*	2863	2873	2888	2899	2919*	2932	2943	2965*	2979	2994	3005
3025*	3036	3046	3066*	3079	3090	3110*	3122	3132	3152*	3164	3174	3193*
3201	3220*	3228	3247*	3257	3267	3288*	3293	3306	3317	3332	3343	3361*
3373	3384	3402*	3409	3418	3428	3440	3450	3467*	3478	3490	3510*	3519
3538*	3547	3567*	3576	3600*	3611	3621	3641*	3651	3671*	3679	3689	3711*
3719	3728	3747*	3757	3767	3787*	3794	3813*	3820	3839*	3846	3859*	3869
3979	3892*	3902	3912	3925*	3934	3945	3955	3968*	3979	3989	4001	4012
4021	4035*	4049	4059	4072	4083	4096*	4108	4118	4127	4140*	4152	4162
4172	4182	4191	4204*	4216	4226	4235	4248*	4259	4269	4278	4291*	4302
4312	4321	4340*	4350	4360	4379*	4388	4399	4409	4427*	4435	4445	4456
4466	4475	4493*	4502	4512	4521	4531	4541	4560*	4569	4579	4588	4609*
4617	4626	4637	4647	4656	4678*	4687	4697	4706	4717	4726	4747*	4756
4766	4775	4786	4795	4815*	4824	4834	4843	4853	4862	4887*	4896	4925*
4934	4962*	4971	4993*	5002	5022*	5031	5046	5069*	5079	5094	5111	5132*
5144	5161	5180	5201*	5209	5223	5237	5259*	5270	5294*	5306	5328*	5336
5357*	5366	5389*	5394	5403	5423*	5430	5451*	5458	5467	5493*	5494	5515*
5522	5531	5554*	5561	5570	5596*	5603	5629*	5636	5684*	5691	5700	5714
5726	5735	5748	5761	5775	5789	5819*	5847	5866	5884	5902	5918	5934
5953	5975*	5988	6014*	6022	6037	6050*	6059	6074	6087*	6096	6110	6123*
6133	6148	6173*	6182	6198	6213	6227*	6236	6250	6264	6280	6304*	6313
6327*	6336	6351	6364*	6373	6388	6411*	6419	6433	6447	6459	6474	6488*
6497	6512	6527	6551*	6561	6577	6593	6607*	6616	6631	6647	6661	6675*
6684	6709*	6718	6733	6748	6763	6776*	6786	6801	6816	6831	6855*	6865
6880	6894	6910	6923*	6933	6948	6963	6977	6990*	7000	7015	7029	7046
7059*	7069	7085	7100	7118	7142*	7154	7174	7195*	7208	7226	7246*	7254
7220	7290*	7309	7330	7353*	7360	7375	7389*	7397	7406	7419*	7428	7437
7450*	7458	7467	7480*	7488	7497	7510*	7518	7527	7540*	7548	7557	7578*
7584	7598	7611*	7621	7631	7640	7653*	7663	7673	7682	7695*	7705	7715
7724	7737*	7747	7757	7766	7779*	7789	7799	7808	7821*	7831	7841	7850
7871*	7879	7898*	7923*	7936	7963*	7987*	8004	8041*	8098*	8128	8148*	8171*

SXX = 177716	9180	8207	8220	8242	8258	6618	6968	7158	7258	7488	7698	7928	8398	
	5528	5728	6058	6248	6438	10108	10358	10598	10848	11098	11348	11588	11838	
	8578	8758	8938	9168	9418	13068	13198	13538	13668	14008	14138	14478	14608	
	12188	12368	12548	12728	13028	16138	16408	16528	16808	16948	17268	17418	17748	
	15248	15338	15618	15788	16028	19118	19228	19368	19468	19588	19798	19928	20028	
	17898	18228	18378	18668	18838	20968	21328	21498	21858	22018	22288	22388	22498	
	20248	20398	20488	20838	23128	23488	23618	23908	24018	24328	24438	24678	24778	
	22698	22978	23128	23488	23618	23908	26038	26298	26418	26748	27068	27398	27718	
	25228	25328	25578	25678	25908	28888	28998	29328	29438	29798	29948	30058	30368	
	28208	28318	28638	28738	28998	31228	31328	31648	31748	32018	32288	32578	32678	
	30798	30908	31228	31328	31648	34098	34188	34288	34408	34508	34788	34908	35198	
	33328	33438	33738	33848	34098	36798	36898	37198	37288	37578	37678	37948	38208	
	35768	36118	36218	36518	36798	39348	39458	39558	39798	39898	40018	40128	40498	
	38698	38798	39028	39128	39348	40838	41088	41188	41278	41528	41628	41728	41828	
	40598	40728	42598	42698	42788	43028	43128	43218	43508	43608	43888	43998	44098	
	42358	44458	44668	44758	45028	45128	45218	45318	45418	45698	45798	45888	46178	
	46268	46378	46478	46568	46878	46978	47068	47178	47268	47568	47668	47758	47968	
	47958	48248	48348	48438	48538	48628	48668	49348	49718	50028	50318	50468	50798	
	50948	51118	51448	51618	51808	52098	52238	52378	52708	53068	53368	53668	53948	
	54038	54308	54588	54678	54948	55228	55318	55618	55708	56038	56368	56918	57008	
	57148	57268	57358	57488	57618	57758	57898	58478	58668	58848	59028	59188	59348	
	59538	59888	60228	60378	60598	60748	60968	61108	61338	61488	61828	61988	62138	
	62368	62508	62648	62808	63138	63368	63518	63738	63888	64198	64338	64478	64598	
	64748	64978	65128	65278	65618	65778	65938	66168	66318	66478	66618	66848	67188	
	67338	67488	67638	67868	68018	68168	68318	68658	68808	68948	69108	69338	69488	
SXXX = 000716	9180	80048	81288	81808	82208	82428	8618	8968	9158	9258	9488	9698	9928	9398
	5528	5728	6058	6248	6438	10108	10358	10598	10848	11098	11348	11588	11838	
	8578	8758	8938	9168	9418	13068	13198	13538	13668	14008	14138	14478	14608	
	12188	12368	12548	12728	13028	16138	16408	16528	16808	16948	17268	17418	17748	
	15248	15338	15618	15788	16028	18838	19118	19228	19368	19468	19688	19798	19928	
	17898	18228	18378	18668	18838	20968	21328	21498	21858	22018	22288	22388	22498	
	20248	20398	20488	20838	23128	23488	23618	23908	24018	24328	24438	24678	24868	
	22698	22978	23128	23488	23618	23908	25908	26038	26298	26418	26748	27068	27398	
	25228	25328	25578	25678	25908	28888	28998	29328	29438	29798	29948	30058	30368	
	28208	28318	28638	28738	28998	31228	31328	31648	31748	32018	32288	32578	32678	
	30798	30908	31228	31328	31648	34098	34188	34288	34408	34508	34788	34908	35198	
	33328	33438	33738	33848	34098	36798	36898	37198	37288	37578	37678	37948	38208	
	35768	36118	36218	36518	36798	39348	39458	39558	39798	39898	40018	40128	40498	
	38698	38798	39028	39128	39348	40838	41088	41188	41278	41528	41628	41728	41828	
	40598	40728	42598	42698	42788	43028	43128	43218	43508	43608	43888	43998	44098	
	42358	44458	44668	44758	45028	45128	45218	45318	45418	45698	45798	45888	46178	
	46268	46378	46478	46568	46878	46978	47068	47178	47268	47568	47668	47758	47868	
	47958	48248	48348	48438	48538	48628	48668	49348	49718	50028	50318	50468	50798	
	50948	51118	51448	51618	51808	52098	52238	52378	52708	53068	53368	53668	53948	
	54038	54308	54588	54678	54948	55228	55318	55618	55708	56038	56368	56918	57008	
	57148	57268	57358	57488	57618	57758	57898	58478	58668	58848	59028	59188	59348	
	59538	59888	60228	60378	60598	60748	60968	61108	61338	61488	61828	61988	62138	
	62368	62508	62648	62808	63138	63368	63518	63738	63888	64198	64338	64478	64598	
	64748	64978	65128	65278	65618	65778	65938	66168	66318	66478	66618	66848	67188	
	67338	67488	67638	67868	68018	68168	68318	68658	68808	68948	69108	69338	69488	

MAINDEC-11-DFKAA-8 11:34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 431  
DFKAA8.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

COMMEN	18																
ENDCOM	18																
ERROR	4048	544	548	564	568	602	621	640	658	693	712	722	745	766	789		
	836	854	872	890	913	938	967	988	1007	1032	1056	1081	1106	1131	1155		
	1120	1215	1233	1251	1269	1303	1316	1350	1363	1397	1410	1444	1457	1510	1521		
	1530	1558	1575	1599	1610	1637	1649	1677	1691	1723	1738	1771	1786	1819	1834		
	1863	1880	1908	1919	1933	1943	1965	1976	1989	1999	2021	2036	2045	2080	2093		
	2129	2146	2182	2198	2225	2235	2246	2255	2266	2294	2309	2345	2358	2387	2398		
	2429	2440	2464	2474	2483	2509	2519	2529	2554	2564	2587	2600	2626	2638	2671		
	2703	2736	2768	2785	2817	2828	2860	2870	2885	2896	2929	2940	2976	2991	3002		
	3033	3043	3076	3087	3119	3129	3161	3171	3198	3225	3254	3264	3290	3303	3314		
	3329	3340	3370	3381	3406	3415	3425	3437	3447	3475	3487	3516	3544	3573	3608		
	3618	3648	3676	3686	3716	3725	3754	3764	3791	3817	3843	3866	3876	3899	3909		
	3931	3942	3952	3976	3986	3998	4009	4018	4046	4056	4069	4080	4105	4115	4124		
	4149	4159	4169	4179	4188	4213	4223	4232	4256	4266	4275	4299	4309	4318	4347		
	4357	4385	4396	4406	4432	4442	4453	4463	4472	4499	4509	4518	4528	4538	4566		
	4576	4585	4614	4623	4634	4644	4653	4684	4694	4703	4714	4723	4753	4763	4772		
	4783	4792	4821	4831	4840	4850	4859	4893	4931	4968	4999	5028	5043	5076	5091		
	5108	5141	5158	5177	5206	5220	5234	5267	5303	5333	5363	5391	5400	5427	5455		
	5464	5491	5519	5528	5558	5567	5600	5633	5688	5697	5711	5723	5732	5745	5758		
	5772	5786	5830	5844	5863	5881	5899	5915	5931	5950	5981	5985	6019	6034	6056		
	6071	6093	6107	6130	6145	6179	6195	6210	6233	6247	6261	6277	6310	6333	6348		
	6370	6385	6416	6430	6444	6456	6471	6494	6509	6524	6558	6574	6590	6613	6628		
	6644	6658	6681	6715	6730	6745	6760	6783	6798	6813	6828	6862	6877	6891	6907		
	6930	6945	6963	6974	6997	7012	7026	7043	7066	7082	7097	7115	7151	7171	7205		
	7223	7251	7267	7297	7306	7321	7327	7357	7372	7394	7403	7425	7434	7455	7464		
	7485	7494	7515	7524	7545	7554	7581	7595	7618	7628	7637	7660	7670	7679	7702		
	7712	7721	7744	7754	7763	7786	7796	7805	7828	7838	7847	7876	7905	7928	7933		
	7945	7970	7976	7996	8001	8070	8125	8154	8177	8217	8239	8280	8352	8356	8360		
	8364	8368	8372	8376	8380												
ESCAPE	18																
GETPRI	18																
GETSR	18																
JNE	71258	8050	8075	8080													
LOOP	4048	552	572	605	624	643	661	696	715	725	748	769	792	839	857		
	875	893	916	941	1010	1035	1059	1084	1109	1134	1158	1183	1218	1236	1254		
	1272	1306	1319	1353	1366	1407	1413	1447	1460	1513	1524	1533	1561	1578	1602		
	1613	1640	1652	1680	1694	1726	1741	1774	1789	1822	1837	1866	1883	1911	1922		
	1936	1946	1968	1979	1992	2002	2024	2039	2048	2083	2096	2132	2149	2185	2201		
	2228	2238	2249	2258	2269	2297	2312	2348	2361	2390	2401	2432	2443	2467	2477		
	2486	2512	2522	2532	2557	2567	2590	2603	2629	2641	2674	2706	2739	2771	2788		
	2820	2831	2863	2873	2888	2899	2932	2943	2979	2994	3005	3036	3046	3079	3090		
	3122	3132	3164	3174	3201	3228	3257	3267	3293	3306	3317	3332	3343	3373	3384		
	3409	3418	3428	3440	3450	3478	3490	3519	3547	3576	3611	3621	3651	3679	3689		
	3719	3728	3757	3767	3794	3820	3846	3869	3879	3902	3912	3934	3945	3955	3979		
	3989	4001	4012	4021	4049	4059	4072	4083	4108	4118	4127	4152	4162	4172	4182		
	4191	4216	4226	4235	4259	4269	4278	4302	4312	4321	4350	4360	4388	4399	4409		
	4435	4445	4456	4466	4475	4502	4512	4521	4531	4541	4569	4579	4588	4617	4626		
	4637	4647	4656	4687	4697	4706	4717	4726	4756	4766	4775	4786	4795	4824	4834		
	4843	4853	4862	4896	4934	4971	5002	5031	5046	5079	5094	5111	5144	5161	5180		
	5209	5223	5237	5270	5306	5336	5366	5394	5403	5430	5458	5467	5494	5522	5531		
	5561	5570	5603	5636	5691	5700	5714	5726	5735	5748	5761	5775	5789	5847	5866		
	5884	5902	5918	5934	5953	5988	6022	6037	6059	6074	6096	6110	6133	6148	61		

## K16

MAINDEC-11-DFKAA-8 11:34 CPU TEST  
DFKAA8.P11 CROSS REFERENCE TABLE -- MACRO NAMES

MACY11 27(732) 01-OCT-76 15:03 PAGE 434

7029	7046	7069	7085	7100	7118	7154	7174	7208	7226	7254	7270	7309	7330	7360	
7375	7397	7406	7428	7437	7458	7467	7498	7497	7518	7527	7548	7557	7584	7598	
7621	7631	7640	7663	7673	7682	7705	7715	7724	7747	7757	7766	7789	7799	7808	
7831	7841	7850	7879	7936	8004	8128	8180	8220	8242						
MULT															
NEWTST	1*	404*	531	593	612	631	650	683	703	732	756	776	827	846	864
	882	900	924	948	972	994	1018	1043	1067	1093	1117	1142	1166	1206	1225
	1243	1261	1293	1340	1387	1434	1503	1550	1592	1629	1667	1712	1759	1807	1850
	1896	1952	2008	2069	2116	2170	2208	2284	2335	2377	2418	2451	2492	2538	2573
	2618	2658	2690	2722	2754	2803	2846	2913	2959	3019	3060	3104	3146	3197	3214
	3241	3282	3355	3396	3461	3504	3532	3561	3594	3635	3665	3705	3741	3781	3807
	3833	3853	3886	3919	3962	4029	4090	4134	4198	4242	4285	4334	4373	4421	4487
	4554	4603	4672	4741	4809	4881	4919	4956	4987	5016	5063	5126	5195	5253	5288
	5322	5351	5383	5417	5445	5482	5509	5548	5590	5623	5678	5813	5969	6008	6044
	6081	6117	6167	6221	6298	6321	6358	6405	6482	6545	6601	6669	6703	6770	6849
	6917	6984	7053	7136	7189	7240	7284	7347	7383	7413	7444	7474	7504	7534	7572
	7605	7647	7689	7731	7773	7815	7865	7892	7917	7957	7981	8035	8092	8142	8165
	8201	8252													
POP	1*														
PUSH	1*														
REPORT	1*														
SETPRI	1*														
SETUP	1*														
SKIP	1*														
SLASH	1*														
STARS	1*														
	593	595	420	431	458	460	467	478	480	501	503	509	531	533	579
	756	758	612	614	631	633	650	652	668	683	685	703	705	732	734
	924	926	776	778	800	827	829	846	848	864	866	882	884	900	902
	1095	1117	1119	1142	1144	1166	1168	1191	1206	1208	1225	1227	1243	1245	1261
	1263	1280	1293	1295	1327	1340	1342	1374	1387	1389	1421	1434	1436	1468	1486
	1490	1503	1505	1541	1550	1552	1586	1592	1594	1621	1629	1631	1660	1667	1669
	1703	1712	1714	1749	1759	1761	1797	1807	1809	1845	1850	1852	1891	1896	1898
	1952	1954	2008	2010	2055	2069	2071	2104	2116	2118	2157	2170	2172	2208	2210
	2276	2284	2286	2320	2335	2337	2369	2377	2379	2409	2418	2420	2451	2453	2492
	2494	2538	2540	2573	2575	2610	2618	2620	2650	2658	2660	2682	2690	2692	2714
	2722	2724	2747	2754	2756	2796	2803	2805	2838	2846	2848	2906	2913	2915	2950
	2959	2961	3011	3019	3021	3053	3060	3062	3097	3104	3106	3139	3146	3148	3181
	3187	3189	3208	3214	3216	3235	3241	3243	3274	3282	3284	3350	3355	3357	3390
	3396	3398	3456	3461	3463	3497	3504	3506	3526	3532	3534	3554	3561	3563	3583
	3594	3596	3628	3635	3637	3658	3665	3667	3696	3705	3707	3734	3741	3743	3773
	3781	3783	3800	3807	3809	3826	3833	3835	3853	3855	3886	3888	3919	3921	3962
	3964	4029	4031	4090	4092	4134	4136	4198	4200	4242	4244	4285	4287	4328	4334
	4336	4367	4373	4375	4416	4421	4423	4482	4487	4489	4547	4554	4556	4595	4603
	4605	4663	4672	4674	4733	4741	4743	4802	4809	4811	4869	4881	4883	4910	4919
	4921	4946	4956	4958	4977	4987	4989	5008	5016	5018	5054	5063	5065	5119	5126
	5128	5188	5195	5197	5245	5253	5255	5278	5288	5290	5315	5322	5324	5344	5351
	5353	5376	5383	5385	5410	5417	5419	5438	5445	5447	5475	5482	5484	5502	5509
	5511	5539	5548	5550	5581	5590	5592	5613	5623	5625	5647	5678	5680	5797	5813
	5815	5962	5969	5971	5994	6008	6010	6044	6046	6081	6117	6119	6156	6167	6484
	6169	6221	6223	6289	6298	6300	6321	6323	6358	6360	6395	6405	6407	6482	6484
	6535	6545	6547	6601	6603	6669	6671	6693	6703	6705	6770	6772	6839	6849	6851
	6917	6919	6984	6986	7053	7055	7128	7136	7138	7181	7189	7191	7233	7240	7242
	7277	7284	7286	7338	7347	7349	7383	7385	7413	7415	7444	7446	7474	7476	7504
	7506	7534	7536	7564	7572	7574	7605	7607	7647	7649	7689	7691	7731	7733	7773
	7775	7815	7817	7857	7865	7867	7887	7892	7894	7910	7917	7919	7952	7957	7959

MAINDEC-11-DFKAA-B 11:34 CPU TEST  
DFKAAAB.P11 CROSS REFERENCE TABLE -- MACRO NAMES  
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	7981 8201	7983 8203	8012 8252	8035 8254	8037 8346	8085 8350	8092	8094	8136	8142	8144	8159	8165	8167	8187
SWRSU	1*														
TYPBIN	1*														
TYPDEC	1*														
TYPNAM	1*														
TYPNUM	1*														
TYPOCS	1*														
TYPOCT	1*														
TYPTXT	1*														
S\$ERCD	404*	545	554	565	574	607	626	645	663	698	717	727	751	771	795
	841	859	877	895	919	944	967	989	1013	1038	1062	1087	1112	1137	1161
	1186	1220	1238	1256	1274	1309	1322	1356	1369	1403	1416	1450	1463	1515	1526
	1535	1563	1581	1604	1616	1642	1655	1682	1697	1728	1744	1776	1792	1824	1840
	1868	1886	1914	1924	1939	1948	1971	1981	1995	2004	2027	2041	2050	2085	2099
	2134	2152	2187	2204	2231	2240	2251	2260	2271	2299	2315	2350	2364	2392	2404
	2434	2446	2470	2479	2488	2515	2524	2534	2560	2569	2593	2605	2631	2644	2677
	2709	2742	2774	2791	2823	2833	2866	2875	2891	2901	2935	2945	2982	2997	3007
	3039	3048	3082	3092	3125	3134	3167	3176	3203	3230	3260	3269	3295	3308	3319
	3334	3345	3376	3386	3411	3420	3430	3442	3452	3481	3493	3521	3549	3578	3613
	3623	3653	3681	3691	3721	3730	3759	3769	3796	3822	3848	3872	3881	3905	3914
	3937	3948	3957	3982	3991	4004	4014	4023	4052	4061	4075	4085	4111	4120	4129
	4155	4164	4175	4184	4193	4219	4228	4237	4262	4271	4280	4305	4314	4323	4353
	4362	4391	4402	4411	4438	4447	4459	4468	4477	4493	4505	4523	4533	4543	4572
	4581	4590	4619	4628	4640	4649	4658	4690	4699	4708	4719	4728	4759	4768	4777
	4788	4797	4827	4836	4845	4855	4864	4899	4937	4973	5004	5034	5049	5082	5097
	5114	5147	5164	5183	5212	5226	5240	5273	5309	5339	5369	5396	5405	5432	5460
	5469	5496	5524	5533	5563	5573	5606	5639	5693	5702	5716	5728	5737	5750	5763
S\$ERNU	404*	545	554	565	574	607	626	645	663	699	717	727	751	771	795
	841	859	877	895	919	944	967	989	1013	1038	1062	1087	1112	1137	1161
	1186	1220	1238	1256	1274	1309	1322	1356	1369	1403	1416	1450	1463	1515	1526
	1535	1563	1581	1604	1616	1642	1655	1682	1697	1728	1744	1776	1792	1824	1840
	1868	1886	1914	1924	1939	1948	1971	1981	1995	2004	2027	2041	2050	2085	2099
	2134	2152	2187	2204	2231	2240	2251	2260	2271	2299	2315	2350	2364	2392	2404
	2434	2446	2470	2479	2488	2515	2524	2534	2560	2569	2593	2605	2631	2644	2677
	2709	2742	2774	2791	2823	2833	2866	2875	2891	2901	2935	2945	2982	2997	3007
	3039	3048	3082	3092	3125	3134	3167	3176	3203	3230	3260	3269	3295	3308	3319
	3334	3345	3376	3386	3411	3420	3430	3442	3452	3481	3493	3521	3549	3578	3613
	3623	3653	3681	3691	3721	3730	3759	3769	3796	3822	3848	3872	3881	3905	3914
	3937	3948	3957	3982	3991	4004	4014	4023	4052	4061	4075	4085	4111	4120	4129
	4155	4164	4175	4184	4193	4219	4228	4237	4262	4271	4280	4305	4314	4323	4353
	4362	4391	4402	4411	4438	4447	4459	4468	4477	4493	4505	4523	4533	4543	4572
	4581	4590	4619	4628	4640	4649	4658	4690	4699	4708	4719	4728	4759	4768	4777
	4788	4797	4827	4836	4845	4855	4864	4899	4937	4973	5004	5034	5049	5082	5097
	5114	5147	5164	5183	5212	5226	5240	5273	5309	5339	5369	5396	5405	5432	5460
	5469	5496	5524	5533	5563	5573	5606	5639	5693	5702	5716	5728	5737	5750	5763

MAINDEC-11-DFKAA-B 11/34 CPU TEST  
DFKAA.B.P11 CROSS REFERENCE TABLE -- MACRO NAMES 01-OCT-76 15:03 PAGE 436

5777	5791	5831	5850	5869	5887	5905	5921	5937	5956	5981	5990	6025	6040	6062	
6077	6099	6113	6136	6151	6185	6201	6216	6239	6253	6267	6283	6316	6339	6354	
6376	6391	6422	6436	6450	6462	6477	6500	6515	6530	6564	6580	6596	6619	6634	
6650	6664	6687	6721	6736	6751	6766	6789	6804	6819	6834	6868	6883	6897	6913	
6936	6951	6966	6980	7003	7018	7032	7049	7072	7088	7103	7121	7157	7177	7211	
7229	7257	7273	7297	7312	7321	7333	7362	7378	7399	7408	7430	7439	7460	7469	
7490	7499	7520	7529	7550	7559	7596	7600	7624	7633	7642	7666	7675	7684	7708	
7717	7726	7750	7759	7768	7792	7801	7810	7834	7843	7852	7881	7905	7928	7938	
7945	7970	7976	7996	8006	8070	8131	8154	8183	8222	8245	8281	8353	8357	8361	
8365	8369	8373	8377	8381											
<b>SSERRO</b>	404*	569	602	621	640	658	693	712	722	745	766	789	836	854	872
	890	913	938	1007	1032	1056	1081	1106	1131	1155	1180	1215	1233	1251	1269
	1316	1363	1410	1457	1530	1575	1610	1649	1691	1738	1786	1834	1880	1943	1999
	2045	2093	2146	2198	2266	2309	2358	2398	2440	2483	2529	2564	2600	2638	2671
	2703	2736	2785	2828	2896	2940	3002	3043	3087	3129	3171	3198	3225	3264	3340
	3381	3447	3487	3516	3544	3573	3618	3648	3686	3725	3764	3791	3817	3843	3876
	3909	3952	4018	4090	4124	4188	4232	4275	4318	4357	4406	4472	4538	4585	4653
	4723	4792	4859	4893	4931	4968	4999	5043	5108	5177	5234	5267	5303	5333	5363
	5400	5427	5464	5491	5528	5567	5600	5633	5786	5950	5985	6034	6071	6107	6145
	6210	6277	6310	6348	6385	6471	6524	6590	6658	6681	6760	6828	6907	6974	7043
	7115	7171	7223	7267	7327	7403	7434	7464	7494	7524	7554	7595	7637	7679	
	7721	7763	7805	7847	7876	8001	8177								
<b>SSESCA</b>	1*														
	404*	552	572	605	624	643	661	696	715	725	748	769	792	839	857
	975	893	916	941	1010	1035	1059	1084	1109	1134	1158	1183	1218	1236	1254
	1272	1306	1319	1353	1366	1400	1413	1447	1460	1513	1524	1533	1561	1578	1602
	1613	1640	1652	1680	1694	1726	1741	1774	1789	1822	1837	1866	1883	1911	1922
	1936	1946	1968	1979	1992	2002	2024	2039	2048	2083	2096	2132	2149	2185	2201
	2228	2238	2249	2258	2269	2297	2312	2348	2361	2390	2401	2432	2443	2467	2477
	2486	2512	2522	2532	2557	2567	2590	2603	2629	2641	2674	2706	2739	2771	2788
	2820	2831	2863	2873	2988	2999	2932	2943	2979	2994	3005	3036	3046	3079	3090
	3122	3132	3164	3174	3201	3228	3257	3267	3293	3306	3317	3332	3343	3373	3384
	3409	3418	3428	3440	3450	3478	3490	3519	3547	3576	3611	3621	3651	3679	3699
	3719	3728	3757	3767	3794	3820	3846	3869	3879	3902	3912	3934	3945	3955	3979
	3989	4001	4012	4021	4049	4059	4072	4083	4108	4118	4127	4156	4162	4172	4182
	4191	4216	4226	4235	4259	4269	4278	4302	4312	4321	4350	4360	4388	4399	4409
	4435	4445	4456	4466	4475	4502	4512	4521	4531	4541	4569	4579	4588	4617	4626
<b>SSLOOP</b>	4637	4647	4656	4687	4697	4706	4717	4726	4756	4766	4775	4786	4795	4824	4834
	4843	4853	4862	4896	4934	4971	5002	5031	5046	5079	5094	5111	5144	5161	5180
	5209	5223	5237	5270	5306	5336	5366	5394	5403	5430	5458	5467	5494	5522	5531
	5561	5570	5603	5636	5691	5700	5714	5726	5735	5748	5761	5775	5789	5847	5866
	5884	5902	5918	5934	5953	5988	6022	6037	6059	6074	6096	6110	6133	6148	6182
	6198	6213	6238	6250	6264	6280	6313	6336	6351	6373	6388	6419	6433	6447	6459
	6474	6497	6512	6527	6561	6577	6593	6616	6631	6647	6661	6684	6718	6733	6748
	6763	6786	6801	6816	6831	6865	6880	6894	6910	6933	6948	6963	6977	7000	7015
	7029	7046	7059	7085	7100	7118	7154	7174	7208	7226	7254	7270	7309	7330	7360
	7375	7397	7406	7428	7437	7458	7467	7488	7497	7518	7527	7548	7557	7584	7598
	7621	7631	7640	7663	7673	7682	7705	7715	7724	7747	7757	7766	7789	7799	7808
	7831	7841	7850	7879	7936	8004	8128	8180	8220	8242	826	827	846	864	
	1*	404*	531	593	612	631	650	683	703	732	756	776	827		
	882	900	924	948	972	994	1018	1043	1067	1093	1117	1142	1166	1206	1225
	1243	1261	1293	1340</td											

B01

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DFKAA-B.P11 CROSS REFERENCE TABLE -- MACRO NAMES

SSSAIP	18
EQUAT	18
HEROE	18
KITI	18
SETUP	18
SURHI	18
SACTI	18
SAPTB	18
SAPTH	18
SAPTY	18
SASTRA	18
SCATC	18
SCMTR	18
SDB2D	18
SDB2G	18
SDIV	18
SEOP	18
SERRD	18
SERRT	18
SMUL	18
SPADE	18
STRAND	18
SPCODE	18
SPCOG	18
SPREAD	18
SR2AZ	18
SSAVE	18
SSB2D	18
SSB2G	18
SSCOB	18
SSIZE	18
SEUPR	18
STRAPP	18
STYPC	18
STYDF	18
STYDE	18
STYPC	18
SYOCH	18

## C01

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 DFKAAB.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

200	1567	1648	6491	6506	6520	4927	4964	4995	6413	6427	6441	6453	6467
200	3196	3327	3366	3515	4889	4927	4964	4995	6413	6427	6441	6453	6467
200	6993	7008	7023	7037	7093	7093	7109	7109	7109	7109	7109	7109	7109
200	7092	7098	7098	7109	7109	7109	7109	7109	7109	7109	7109	7109	7109
200	7112	744	788	912	960	1006	1055	1105	1154	1443	3865	3974	4045
200	4255	5026	5041	5089	5106	5136	5218	5232	5299	5331	6142	6194	6469
200	6642	6758	6810	6859	6874	6928	6943	6994	7009	7064	7080	7149	7615
200	7902	8304											7699
205	936	984	1030	1079	1129	1178	1444	1456	1908	1933	1965	1989	2021
205	2509	2554	2587	2670	2734	2783	2815	2883	2927	2989	3254	3370	3475
205	4298	5074	5154	5172	5204	5263	5361	6127	6233	6277	6309	6332	6522
205	6780	6795	7038	7167	7371	7657	7741	7784	8177	8305			
205	538	569	602	621	640	658	693	722	742	745	766	786	836
205	872	890	910	913	934	938	958	961	982	986	1004	1007	1028
205	1056	1077	1081	1103	1106	1127	1131	1152	1155	1176	1180	1215	1233
205	1303	1315	1510	1530	1575	1599	1610	1637	1649	1677	1691	1723	1738
205	1819	1834	1863	1890	1906	1919	1931	1943	1963	1976	1987	1999	2019
205	2080	2093	2129	2146	2182	2198	2223	2235	2266	2294	2309	2345	2358
205	2429	2440	2462	2474	2483	2507	2519	2529	2552	2564	2585	2600	2626
205	2736	2785	2817	2828	2870	2885	2896	2929	2940	2991	3043	3087	3129
205	3225	3252	3264	3290	3303	3314	3329	3340	3368	3381	3425	3437	3473
205	3544	3573	3608	3648	3676	3686	3716	3725	3754	3764	3791	3817	3843
205	3899	3909	3930	3942	3952	3973	3986	3996	4009	4018	4043	4056	4067
205	4124	4147	4159	4168	4179	4188	4212	4223	4232	4253	4266	4275	4299
205	4346	4357	4385	4396	4406	4431	4442	4452	4463	4472	4498	4509	4518
205	4565	4576	4585	4614	4623	4633	4644	4653	4683	4694	4703	4714	4723
205	4772	4783	4792	4820	4831	4840	4850	4859	4893	4931	4968	4999	5028
205	5091	5108	5141	5158	5177	5206	5220	5234	5267	5303	5333	5363	5400
205	5464	5491	5519	5528	5558	5567	5600	5633	5688	5697	5711	5723	5732
205	5772	5796	5844	5863	5881	5899	5915	5931	5950	5985	6130	6144	6195
205	6310	6333	6385	6471	6524	6557	6573	6643	6759	6783	6798	6812	6861
205	6929	6944	6959	6996	7011	7039	7043	7065	7081	7096	7113	7115	7147
205	7202	7205	7220	7223	7267	7306	7327	7357	7394	7403	7425	7434	7455
205	7494	7515	7524	7545	7554	7581	7595	7617	7628	7637	7659	7670	7701
205	7721	7744	7754	7763	7785	7796	7805	7827	7838	7847	7876	7903	7926
205	7974	7994	8001	8125	8217	8239	8264	8269	8273	8293			
205	8294												
205	3406	8296											
205	6032	6069	6105	6245	6442	6507	6611	6679	6713	7249	7263	7300	8300
205	3301	3326	6090	6104	6270	6567	6653	6822	7075	7904	7927	7931	7949
205	7995	8051	8076	8081	8214	8236							
205	3714	4890	4928	4965	4996								
205	3311	3789	3927	3970	4037	4098	4099	4142	4143	4206	4207	4250	4293
205	6141	6188	6503	6637	6724	7106	7898	7923	7942	8105	8106	8107	8108
205	8111	8148											
205	3542	3646	3815	3841	4891	4929	4966	4997					
205	3436	3446	3895	3928	4101	4209	4252	6053	6068	8049	8151		
205	3862	3972	3995	4042	4066	4145	4167	4295	8261	8331			
205	8228	8251	8297										
205	2702	2767	2859	2975	3032	3075	3118	3160	6017	6054	6091	6177	6208
205	6368	6414	6428	6454	6492	6626	6656	6728	6743	6826	6889	6903	6957
205	7094	7110	7200	7218	8301								
205	3415	8295											
205	1350	1362	1457	1521	1558	1930	1986	2246	2461	2506	2551	2584	2669
205	2768	2784	2816	2860	2884	2928	2976	2990	3002	3033	3076	3119	3367
205	3472	3618	3866	3896	3976	4069	4102	4169	4213	4297	4347	4383	4453

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MAINDEC-11-DFKRAA-B 11/34 CPU TEST  
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 DFKRAA.B.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

BNE	6019	6056	6093	6129	6145	6192	6209	6230	6246	6261	6274	6307	6330	6348	6370
	6384	6430	6456	6470	6494	6523	6558	6574	6644	6760	6792	6797	6813	6862	6930
	6974	6997	7056	7169	7203	7221	7369	7618	7660	7743	7786	8174	8299		
	536	549	5558	598	617	636	655	688	708	737	761	781	832	851	869
	827	905	929	953	977	999	1023	1048	1072	1098	1122	1147	1171	1211	1230
	1248	1266	1298	1302	1316	1345	1392	1439	1508	1555	1568	1597	1634	1672	1717
	1764	1812	1855	1901	1957	2013	2074	2121	2175	2213	2289	2340	2382	2423	2456
	2497	2543	2578	2623	2663	2695	2727	2759	2808	2851	2918	2964	3024	3065	3109
	3151	3192	3219	3246	3287	3360	3401	3466	3485	3509	3537	3566	3599	3640	3670
	3710	3746	3786	3812	3838	3858	3891	3924	3967	4034	4095	4105	4139	4149	4203
	4247	4290	4339	4378	4426	4492	4559	4608	4677	4746	4814	4886	4924	4961	4992
	5021	5068	5131	5138	5156	5174	5200	5258	5265	5293	5301	5327	5356	5388	5422
	5450	5487	5514	5553	5595	5628	5683	5818	5836	5838	5840	5842	5857	5859	5861
	5879	5895	5997	5911	5913	5929	5948	5974	6013	6049	6086	6122	6172	6226	6303
	6326	6363	6410	6487	6550	6589	6606	6674	6708	6775	6854	6922	6989	7058	7141
	7166	7194	7245	7289	7304	7325	7352	7372	7388	7418	7449	7479	7509	7539	7577
	7610	7652	7694	7736	7778	7820	7870	7872	7897	7922	7933	7962	7986	8040	8097
	8113	8115	8117	8119	8121	8123	8147	8152	8170	8175	8205	8230	8257	8259	8262
BPL	8292	8332	8337												
	1349	1363	1571	1608	1646	1686	1689	1736	1782	1831	1877	1905	1962	2018	2091
	2140	2142	2196	2222	2255	2305	2356	2396	2438	2636	3251	3931	3998	4046	4256
	4432	4566	4634	4684	4753	4821	6034	6071	6107	6178	6210	6416	6444	6509	6590
	6613	6628	6658	6681	6715	6730	6745	6828	6877	6891	6905	6955	6960	7012	7026
BR	7041	7082	7097	7112	7146	7250	7264	7301	7702	7828	8267	8298	8335		
BVC	539	559	5819	8232	8271	8291									
BVS	1396	1410	5025	5040	5073	5088	5105	6247	6276	6429	6443	6493	6571	6627	6641
	6729	6757	6827	6875	6904	6942	6973	7010	7040	7079	7111	7265	7302	8302	
	1397	1409	1907	1932	1954	1988	2020	2224	2463	2508	2553	2586	2668	2701	2733
	2766	2782	2814	2858	2882	2926	2974	2988	3031	3074	3117	3159	3253	3369	3474
	3864	3897	3929	3975	3997	4044	4068	4103	4146	4210	4254	4296	4345	4384	4430
	4451	4497	4564	4632	4682	4751	4819	6018	6033	6055	6070	6092	6106	6128	6143
	6179	6193	6232	6260	6308	6331	6347	6369	6382	6415	6455	6468	6508	6521	6556
	6587	6612	6657	6680	6714	6744	6781	6796	6811	6860	6890	6927	6958	6995	7025
	7063	7095	7148	7168	7201	7219	7251	7370	7616	7658	7700	7742	7782	7825	8176
CCC	8303														
CLC	537	1300	1347	1394	1441	4144	6174	6439	6568	6608	6638	6676	6710	6754	6856
	6900	6939	6969	6991	7035	7107	7163	7354	8233						
CLC	6293	740	763	784	908	956	1002	1051	1101	1150	1455	3894	5071	5134	5152
	5216	5297	5359	6015	6052	6089	6125	6206	6257	6466	6519	6553	6793	6972	6955
CLN	7007	7077	7198	7216	7900										
CLR	1361	2699	2764	2856	2972	3072	3115	3157	6015	6052	6089	6125	6140	6257	6272
	6344	6366	6490	6553	6808	6887	6925	7022	7061	8172					
	1509	1556	1635	1636	1673	1674	1718	1719	1765	1768	1770	1813	1816	1856	1859
	1902	1958	1959	2014	2015	2075	2078	2079	2122	2125	2126	2176	2179	2214	2217
	2218	2219	2290	2293	2341	2342	2344	2383	2386	2424	2428	2457	2458	2498	2499
	2502	2503	2544	2545	2547	2579	2580	2624	2664	2696	2728	2729	2760	2761	2777
	2809	2810	2852	2853	2919	2920	2965	2966	3025	3026	3066	3097	3110	3111	3152
	3153	3193	3195	3220	3221	3247	3248	3288	3322	3324	3361	3362	3402	3403	3433
	3435	3467	3468	3510	3512	3513	3538	3539	3541	3567	3568	3570	3600	3601	3604
	3641	3642	3643	3671	3672	3711	3747	3748	3749	3814	3840	3859	3892	3893	3925
	3926	3968	3969	4035	4036	4040	4078	4096	4097	4140	4141	4204	4205	4248	4249
	4291	4292	4340	4341	4343	4379	4380	4427	4428	4494	4495	4560	4561	4609	4610
	4678	4679	4747	4748	4815	4816	5069	5101	5132	5150	5167	5424			

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 DFKAAB.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

CLRS	1598	1676	1722	1818	1862	2128	2181	2548	8149					
CLV	1408	6272	6490	6624	6726	6824	6872	7007	7077	8172				
CLZ	1314	2666	2731	2780	2812	2880	2924	2986	3029	6030	6067	6103	6190	6243
	6328	6380	6466	6505	6519	6585	6778	6793	7144					6305
CMP	535	597	616	620	635	639	654	657	687	692	707	721	736	760
	780	831	850	853	868	871	886	889	904	928	937	952	976	985
	1022	1031	1047	1071	1080	1097	1121	1130	1146	1170	1179	1210	1229	1232
	1250	1265	1268	1297	1344	1391	1438	1507	1554	1596	1633	1671	1716	1763
	1854	1900	1956	2012	2073	2120	2174	2212	2288	2339	2381	2422	2455	2496
	2577	2822	2862	2694	2726	2758	2807	2850	2917	2963	3023	3064	3108	3150
	3218	3245	3286	3359	3400	3405	3414	3424	3465	3471	3508	3536	3565	3598
	3669	3709	3745	3785	3811	3816	3837	3842	3857	3890	3923	3951	3966	4017
	4055	4079	4094	4123	4138	4158	4187	4202	4222	4231	4246	4265	4274	4289
	4317	4338	4377	4425	4441	4462	4471	4491	4508	4517	4527	4537	4558	4584
	4613	4622	4652	4676	4693	4702	4713	4722	4745	4762	4771	4782	4791	4813
	4839	4849	4858	4885	4892	4923	4930	4960	4967	4991	4998	5020	5027	5042
	5075	5090	5107	5130	5137	5155	5173	5199	5205	5219	5233	5257	5264	5292
	5326	5332	5355	5362	5387	5399	5421	5426	5449	5454	5486	5490	5513	5552
	5557	5566	5594	5599	5627	5632	5682	5687	5696	5722	5731	5744	5757	5771
	5817	5835	5837	5839	5841	5843	5858	5860	5862	5878	5880	5894	5898	5910
	5912	5914	5928	5930	5947	5949	5973	5994	6012	6048	6085	6121	6225	6302
	6325	6362	6409	6486	6549	6605	6610	6625	6640	6655	6673	6707	6774	6853
	6921	6988	7042	7057	7114	7140	7150	7193	7204	7222	7244	7288	7303	7324
	7326	7351	7356	7387	7393	7402	7417	7424	7433	7448	7454	7478	7493	7508
	7523	7538	7544	7553	7576	7580	7609	7627	7635	7651	7669	7678	7693	7711
	7735	7753	7762	7777	7795	7804	7819	7837	7846	7869	7875	7896	7921	7932
	7943	7961	7967	7973	7985	7993	8000	8039	8096	8112	8114	8116	8118	8122
	8124	8146	8169	8205	8215	8227	8229	8237	8250	8256	8263			
CMPB	3572	7871	8268											
COM	1519	1529	1572	1675	1720	1769	1781	1817	1860	2090	2127	2180	2304	2355
	2437	2459	2581	3027	3068	3112	3154	3194	3222	3299	3300	3325	3434	3469
	3540	3569	3603	3605	3616	3673	3713	3750	4251	4342	4381	5826	6678	6739
	1607	1687	1734	1766	1814	1829	1857	1875	1928	1984	2076	2123	2177	2215
	2263	2291	2384	2425	2500	2527	2546	2549	2582	2596	2597	2697	2762	2854
	2939	2967	2968	3069	3086	3113	3128	3155	3170	3323	3363	3379	3543	3571
	3645	3724	3751	3860	3875	4038								
DEC	1557	1574	1645	1731	1779	1780	1783	1784	1827	1832	1871	1872	1874	1878
	1998	2035	2044	2088	2089	2137	2138	2143	2144	2190	2191	2192	2193	2482
	2518	2528	2826	2827	2869	2894	2895	2922	2938	3302	3380	3445	3484	3684
	3940	3941	3985	4007	4008	4394	4395	5139	5140	5157	5175	5176	6229	6244
	6273	6342	7260	8074	8079	8225								
DEC8	2030	2031	2034	2563	2598									
HALT	417	547	556	567	576	609	628	647	665	700	719	729	753	797
	843	861	879	897	921	946	969	991	1015	1040	1064	1089	1114	1163
	1188	1222	1240	1258	1276	1311	1324	1358	1371	1405	1418	1452	1465	1528
	1537	1565	1583	1606	1618	1644	1657	1684	1699	1730	1746	1778	1794	1826
	1870	1888	1916	1926	1941	1950	1973	1983	1997	2006	2029	2043	2052	2087
	2136	2154	2189	2206	2233	2242	2253	2262	2273	2301	2317	2352	2366	2394
	2436	2448	2472	2481	2490	2517	2526	2536	2562	2571	2595	2607	2633	2646
	2711	2744	2776	2793	2825	2835	2868	2877	2893	2903	2937	2947	2984	2999
	3041	3050	3084	3094	3127	3136	3169	3178	3205	3232	3262	3271	3297	3310
	3336	3347	3378	3388	3413	3422	3432	3444	3454	3483	3495	3523	3551	3615
	3625	3655	3683	3693	3723	3732	3761	3771	3798	3824	3850	3874	3883	3907
	3939	3950	3959	3984	3993	4006	4016	4025	4054	4063	4077	4087	4113	4122
	4157	4166	4177	4186	4195	4221	4230	4239	4264	4273	4282	4307	4316	4325
	4364	4393	4404	4413	4440	4449	4461	4470	4479	4507	4516	4525	4535	4574

FO1

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 DFKAAAB.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

4583	4592	4621	4630	4642	4651	4660	4692	4701	4710	4721	4730	4761	4770	4779
4790	4799	4829	4838	4847	4857	4866	4901	4933	4975	5006	5036	5051	5084	5099
5116	5149	5166	5185	5214	5228	5242	5275	5311	5341	5371	5398	5407	5434	5462
5471	5498	5526	5535	5565	5575	5608	5641	5695	5704	5718	5730	5739	5752	5765
5779	5793	5833	5852	5871	5889	5907	5923	5939	5958	5983	5992	6027	6042	6064
6079	6101	6115	6138	6153	6187	6203	6218	6241	6255	6269	6295	6318	6341	6356
6378	6393	6424	6438	6452	6464	6479	6502	6517	6532	6566	6582	6598	6621	6636
6652	6666	6689	6723	6738	6753	6768	6791	6806	6821	6836	6870	6885	6899	6915
6938	6953	6968	6982	7005	7020	7034	7051	7074	7090	7105	7123	7159	7179	7213
7231	7259	7275	7299	7314	7323	7335	7364	7380	7401	7410	7432	7441	7462	7471
7492	7501	7522	7531	7552	7561	7588	7602	7626	7635	7644	7668	7677	7686	7710
7719	7728	7752	7761	7770	7794	7803	7812	7836	7845	7854	7883	7907	7930	7940
7947	7972	7978	7998	8008	8072	8133	8156	8185	8224	8247	8283	8327	8355	8359
INC	8363	8367	8371	8375	8379	8383	8383	8383	8383	8383	8383	8383	8383	8383
534	546	555	566	575	596	608	615	627	634	646	653	664	686	699
706	718	728	735	741	752	759	772	779	785	796	830	842	849	860
867	878	885	896	903	909	920	927	933	945	951	957	968	975	981
990	997	1003	1014	1021	1027	1039	1046	1052	1063	1070	1076	1088	1096	1102
1113	1120	1126	1138	1145	1151	1162	1169	1175	1187	1209	1221	1228	1239	1246
1257	1264	1275	1296	1310	1323	1343	1357	1370	1390	1404	1417	1437	1451	1464
1506	1516-	1518	1520	1527	1536	1553	1564	1573	1582	1595	1605	1617	1632	1643
1656	1670	1683	1685	1698	1715	1721	1729	1732	1733	1745	1762	1767	1777	1785
1793	1810	1815	1825	1828	1841	1853	1858	1861	1869	1873	1887	1899	1903	1915
1918	1925	1940	1949	1955	1960	1972	1975	1982	1996	2005	2011	2016	2028	2042
2051	2072	2077	2086	2092	2100	2119	2124	2135	2139	2153	2173	2178	2198	2204
2205	2211	2216	2220	2232	2234	2241	2244	2252	2261	2265	2272	2287	2292	2300
2302	2303	2306	2307	2308	2316	2338	2351	2353	2354	2357	2365	2380	2385	2393
2397	2405	2421	2426	2427	2435	2439	2447	2454	2471	2480	2489	2495	2501	2516
2525	2535	2541	2561	2570	2576	2594	2606	2621	2632	2634	2637	2645	2661	2678
2693	2710	2725	2743	2757	2775	2778	2792	2806	2824	2834	2849	2867	2876	2878
2892	2902	2916	2936	2946	2962	2969	2983	2998	3008	3022	3040	3049	3063	3070
3083	3085	3093	3107	3126	3135	3149	3168	3177	3190	3197	3204	3217	3224	3231
3244	3249	3261	3263	3270	3285	3296	3298	3309	3312	3313	3320	3328	3335	3339
3346	3358	3364	3377	3387	3399	3404	3412	3421	3423	3431	3443	3453	3464	3470
3482	3486	3494	3507	3514	3522	3535	3550	3564	3579	3597	3614	3624	3638	3644
3647	3654	3668	3675	3682	3692	3708	3722	3731	3744	3753	3760	3770	3784	3790
3797	3810	3823	3836	3849	3856	3873	3882	3889	3906	3915	3922	3938	3949	3958
3965	3983	3992	3994	4005	4015	4024	4032	4039	4053	4062	4064	4065	4076	4086
4093	4112	4121	4130	4137	4156	4165	4176	4185	4194	4201	4220	4229	4238	4245
4263	4272	4281	4288	4306	4315	4324	4337	4354	4363	4376	4392	4403	4412	4424
4439	4448	4460	4469	4478	4490	4506	4515	4524	4534	4544	4557	4573	4582	4591
4606	4620	4629	4641	4650	4659	4675	4691	4700	4709	4720	4729	4744	4749	4760
4769	4778	4789	4798	4812	4828	4837	4846	4856	4865	4884	4900	4922	4938	4959
4974	4990	5005	5019	5035	5050	5066	5083	5098	5102	5115	5129	5148	5165	5169
5184	5198	5213	5227	5241	5256	5274	5291	5310	5325	5340	5354	5370	5386	5397
5406	5420	5433	5448	5461	5470	5485	5497	5512	5525	5534	5551	5564	5574	5593
5607	5626	5640	5681	5694	5703	5706	5717	5719	5729	5738	5741	5751	5754	5764
5767	5778	5781	5792	5816	5832	5851	5853	5870	5874	5888	5890	5906	5908	5922
5924	5938	5940	5957	5972	5982	5991	6011	6026	6041	6047	6063	6078	6084	6100
6114	6120	6137	6152	6170	6176	6186	6191	6202	6207	6217	6224	6240	6254	6268
6284	6301	6317	6324	6340	6355	6361	6377	6392	6408	6423	6437	6451	6463	6478
6485	6501	6516	6531	6548	6565	6581	6597	6604	6620	6635	6651	6665	6672	6688
6706	6722	6737	6752	6767	6773	6790	6805							

G01

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DFKAR-B.PII CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

H01

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DFKAAB.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

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 DFKAA8.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

6044	6065	6081	6102	6117	6139	6155	6188	6204	6220	6242	6256	6270	6287	6320
6342	6358	6379	6394	6425	6439	6453	6465	6481	6503	6518	6534	6567	6583	6600
6622	6637	6653	6668	6691	6724	6739	6754	6769	6792	6807	6822	6838	6871	6886
6900	6917	6939	6954	6969	6984	7006	7021	7035	7053	7075	7091	7106	7125	7160
7121	7214	7233	7260	7277	7300	7315	7324	7337	7365	7382	7402	7412	7433	7443
7463	7473	7493	7503	7523	7533	7553	7563	7589	7604	7627	7636	7646	7669	7678
7688	7711	7720	7730	7753	7762	7772	7795	7804	7814	7837	7846	7856	7885	7908
7931	7941	7948	7973	7979	7999	8010	8073	8134	8157	8187	8225	8248	8284	8356
8360	8364	8368	8372	8376	8380	8384								
.EVEN	432	8290	8343											
	423	425	454	456	545	549	557	565	569	602	621	640	658	693
	722	745	766	789	836	854	872	890	913	938	967	988	1007	1032
	1081	1106	1131	1155	1180	1215	1233	1251	1269	1303	1312	1316	1350	1359
	1397	1406	1410	1444	1453	1457	1510	1518	1521	1529	1530	1558	1566	1575
	1607	1610	1637	1645	1649	1677	1685	1691	1723	1731	1738	1771	1779	1819
	1827	1834	1863	1871	1880	1908	1917	1919	1927	1933	1942	1943	1965	1974
	1984	1989	1998	1999	2021	2030	2036	2044	2045	2080	2088	2093	2129	2137
	2182	2190	2198	2225	2234	2235	2243	2246	2254	2255	2263	2266	2294	2302
	2345	2353	2358	2387	2395	2398	2429	2437	2440	2464	2473	2474	2482	2509
	2518	2519	2527	2529	2554	2563	2564	2587	2596	2600	2626	2634	2638	2671
	2736	2768	2777	2785	2817	2826	2828	2860	2869	2870	2878	2885	2894	2929
	2938	2940	2976	2985	2991	3000	3002	3033	3042	3043	3076	3085	3087	3119
	3129	3161	3170	3171	3198	3225	3254	3263	3264	3290	3298	3303	3311	3314
	3329	3337	3340	3370	3379	3381	3406	3414	3415	3423	3425	3433	3437	3445
	3475	3484	3487	3516	3544	3573	3608	3616	3618	3648	3676	3684	3686	3716
	3725	3754	3762	3764	3791	3817	3843	3866	3875	3876	3899	3908	3909	3931
	3942	3951	3952	3976	3985	3994	3998	4007	4009	4017	4018	4046	4055	4056
	4064	4069	4078	4080	4105	4114	4115	4123	4124	4149	4158	4167	4169	4178
	4179	4187	4188	4213	4222	4223	4231	4232	4256	4265	4266	4274	4275	4308
	4309	4317	4318	4347	4356	4357	4385	4394	4396	4405	4406	4432	4441	4450
	4453	4462	4463	4471	4472	4499	4508	4509	4517	4518	4526	4536	4538	4566
	4575	4576	4584	4585	4614	4622	4623	4631	4634	4643	4644	4652	4653	4684
	4694	4702	4703	4711	4714	4722	4723	4753	4762	4763	4771	4772	4780	4783
	4792	4821	4830	4831	4839	4840	4848	4850	4858	4859	4893	4931	4968	4999
	5037	5043	5076	5085	5091	5100	5108	5141	5150	5158	5167	5177	5206	5215
	5229	5234	5267	5303	5333	5363	5391	5399	5400	5427	5455	5463	5464	5491
	5527	5528	5558	5566	5567	5600	5633	5688	5696	5697	5705	5711	5719	5723
	5732	5740	5745	5753	5758	5766	5772	5780	5786	5830	5844	5853	5863	5872
	5890	5899	5908	5915	5924	5931	5940	5950	5981	5985	6019	6028	6034	6056
	6071	6093	6102	6107	6130	6139	6145	6179	6188	6195	6204	6210	6233	6242
	6256	6261	6270	6277	6310	6333	6342	6348	6370	6379	6385	6416	6425	6439
	6444	6453	6456	6465	6471	6494	6503	6509	6518	6524	6558	6567	6574	6583
	6613	6622	6628	6637	6644	6653	6658	6681	6715	6724	6730	6739	6745	6754
	6783	6792	6798	6807	6813	6822	6828	6862	6871	6877	6886	6891	6900	6907
	6939	6945	6954	6960	6969	6974	6997	7006	7012	7021	7026	7035	7043	7066
	7082	7091	7097	7106	7115	7151	7160	7171	7205	7214	7223	7251	7260	7297
	7306	7315	7321	7327	7357	7365	7372	7394	7402	7403	7425	7433	7434	7463
	7464	7485	7493	7494	7515	7523	7524	7545	7553	7554	7581	7589	7595	7618
	7628	7636	7637	7660	7669	7670	7678	7679	7702	7711	7712	7720	7721	7744
	7754	7762	7763	7786	7795	7796	7804	7805	7828	7837	7838	7846	7847	7905
	7928	7933	7941	7945	7970	7976	7996	8001	8070	8125	8134	8154	8177	8225
	8239	8248	8280	8352	8356	8360	8364	8368	8372	8376	8380			
.IFF	425	427	545	557	565	569	578	602	611	621	630	640	649	658
	693	702	712	721	722	731	745	755	766	775	789	799	836	854
	863	872	881	890	899	913	923	938	948	967	988			

MAINDEC-11-DFKAA-8 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 446  
 DFKAAAB.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

1242	1251	1260	1269	1278	1312	1316	1326	1359	1363	1373	1406	1410	1420	1453
1457	1467	1518	1529	1530	1539	1566	1575	1585	1607	1610	1620	1645	1649	1659
1685	1691	1701	1731	1738	1748	1779	1786	1796	1827	1834	1844	1871	1880	1890
1917	1927	1942	1943	1952	1974	1984	1998	1999	2008	2030	2044	2045	2054	2088
2093	2103	2137	2146	2156	2190	2198	2208	2234	2243	2254	2263	2266	2275	2302
2309	2319	2353	2358	2368	2395	2398	2408	2437	2440	2450	2473	2482	2483	2492
2518	2527	2529	2538	2563	2584	2573	2596	2600	2609	2634	2638	2648	2671	2681
2703	2713	2736	2746	2777	2785	2795	2826	2828	2837	2869	2878	2894	2905	
2938	2940	2949	2985	3000	3002	3011	3042	3043	3052	3085	3087	3096	3128	3129
3138	3170	3171	3180	3198	3207	3225	3234	3263	3264	3273	3298	3311	3322	3337
3340	3349	3379	3381	3390	3414	3423	3433	3445	3447	3456	3484	3487	3497	3516
3525	3544	3553	3573	3582	3616	3618	3627	3648	3657	3684	3686	3695	3724	3725
3734	3762	3764	3773	3791	3800	3817	3826	3843	3852	3875	3876	3885	3908	3909
3918	3940	3951	3952	3961	3985	3994	4007	4017	4018	4027	4055	4064	4078	4080
4089	4114	4123	4124	4133	4158	4167	4178	4187	4188	4197	4222	4231	4232	4241
4265	4274	4275	4284	4308	4317	4318	4327	4356	4357	4366	4394	4405	4406	4415
4441	4450	4462	4471	4472	4481	4508	4517	4526	4536	4538	4546	4575	4584	4585
4594	4622	4631	4643	4652	4653	4662	4693	4702	4711	4722	4723	4732	4771	
4780	4791	4792	4801	4830	4839	4848	4858	4859	4868	4893	4903	4931	4941	4968
4977	4999	5008	5037	5043	5053	5085	5100	5108	5118	5150	5167	5177	5187	5215
5229	5234	5244	5267	5277	5303	5313	5333	5343	5363	5373	5399	5400	5409	5427
5436	5463	5464	5473	5491	5500	5527	5528	5537	5566	5567	5577	5600	5610	5633
5643	5696	5705	5719	5731	5740	5753	5766	5780	5786	5795	5830	5853	5872	5890
5908	5924	5940	5950	5960	5981	5985	5994	6028	6034	6044	6065	6071	6081	6102
6107	6117	6139	6145	6155	6188	6204	6210	6220	6242	6256	6270	6277	6287	6310
6320	6342	6348	6358	6379	6385	6394	6425	6439	6453	6465	6471	6481	6503	6516
6524	6534	6567	6583	6590	6600	6622	6637	6653	6658	6668	6681	6691	6724	6739
6754	6760	6769	6792	6807	6822	6828	6838	6871	6886	6900	6907	6917	6939	6954
6969	6974	6984	7006	7021	7035	7043	7053	7075	7091	7106	7115	7125	7160	7171
7181	7214	7223	7233	7260	7267	7277	7297	7315	7321	7327	7337	7365	7372	7382
7402	7403	7412	7433	7434	7443	7463	7464	7473	7493	7494	7503	7523	7524	7533
7553	7554	7563	7589	7595	7604	7627	7636	7637	7646	7669	7678	7679	7688	7711
7720	7721	7730	7753	7762	7763	7772	7795	7804	7805	7814	7837	7846	7847	7856
7876	7885	7905	7928	7941	7945	7970	7976	7996	8001	8010	8070	8134	8154	8177
8187	8225	8248	8280	8352	8356	8360	8364	8368	8372	8376	8380			
545	549	552	565	569	602	621	640	658	693	712	722	745	766	789
836	854	872	890	913	938	967	988	1007	1032	1056	1081	1106	1131	1155
1180	1215	1233	1251	1269	1303	1312	1316	1350	1359	1363	1397	1406	1410	1444
1453	1457	1510	1518	1521	1529	1530	1558	1566	1575	1599	1607	1610	1637	1645
1649	1677	1685	1691	1723	1731	1738	1771	1779	1786	1819	1827	1834	1863	1871
1980	1908	1917	1919	1927	1933	1942	1943	1965	1974	1976	1984	1989	1998	1999
2021	2030	2036	2044	2045	2080	2088	2093	2129	2137	2146	2182	2190	2198	2225
2234	2235	2243	2246	2254	2255	2263	2266	2294	2302	2309	2345	2353	2358	2387
2395	2398	2429	2437	2440	2464	2473	2474	2482	2483	2509	2518	2519	2527	2529
2554	2563	2564	2587	2596	2600	2626	2634	2638	2671	2703	2736	2768	2777	2785
2817	2826	2828	2860	2869	2870	2878	2885	2894	2896	2929	2938	2940	2976	2985
2991	3000	3002	3033	3042	3043	3076	3085	3087	3119	3128	3129	3161	3170	3171
3198	3225	3254	3263	3264	3290	3298	3303	3311	3314	3322	3329	3337	3340	3370
3379	3381	3406	3414	3415	3423	3425	3433	3437	3445	3447	3475	3484	3487	3516
3544	3573	3608	3616	3618	3648	3676	3684	3686	3716	3724	3725	3754	3762	3764
3791	3817	3843	3866	3875	3876	3899	3908	3909	3931	3940	3942	3951	3952	3976
3985	3986	3994	3998	4007	4009	4017	4018	4046	4055	4056	4064	4069	4078	4080
4105	4114	4115	4123	4124	4149	4158								

## K01

MAINDEC-11-DFKAA-B 11/34 CPU TEST MACY11 27(732) 01-OCT-76 15:03 PAGE 447  
 DFKAAB.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

4614	4622	4623	4631	4634	4643	4644	4652	4653	4684	4693	4694	4702	4703	4711
4714	4722	4723	4753	4762	4763	4771	4772	4780	4783	4791	4792	4821	4830	4831
4839	4840	4848	4850	4858	4859	4893	4931	4968	4999	5028	5037	5043	5076	5085
5091	5100	5108	5141	5150	5158	5167	5177	5206	5215	5220	5229	5234	5267	5303
5323	5363	5391	5399	5400	5427	5455	5463	5464	5491	5519	5527	5528	5558	5566
5567	5600	5633	5688	5696	5697	5705	5711	5719	5723	5731	5732	5740	5745	5753
5758	5766	5772	5780	5786	5830	5844	5853	5863	5872	5881	5890	5899	5908	5915
5924	5931	5940	5950	5981	5985	6019	6028	6034	6056	6065	6071	6093	6102	6107
6130	6139	6145	6179	6188	6195	6204	6210	6233	6242	6247	6256	6261	6270	6277
6310	6333	6342	6348	6370	6379	6385	6416	6425	6430	6439	6444	6453	6456	6465
6471	6494	6503	6509	6518	6524	6558	6567	6574	6583	6590	6613	6622	6628	6637
6644	6653	6658	6681	6715	6724	6730	6739	6745	6754	6760	6783	6792	6798	6807
6813	6822	6828	6862	6871	6877	6886	6891	6900	6907	6930	6939	6945	6954	6960
6969	6974	6997	7006	7012	7021	7026	7035	7043	7066	7075	7082	7091	7097	7106
7115	7151	7160	7171	7205	7214	7223	7251	7260	7267	7297	7306	7315	7321	7327
7357	7365	7372	7394	7402	7403	7425	7433	7434	7455	7463	7464	7485	7493	7494
7515	7523	7524	7545	7553	7554	7581	7589	7595	7618	7627	7628	7636	7637	7660
7669	7670	7678	7679	7702	7711	7712	7720	7721	7744	7753	7754	7762	7763	7786
7795	7796	7804	7805	7828	7837	7838	7846	7847	7876	7905	7928	7933	7941	7945
7970	7976	7996	8001	8070	8125	8134	8154	8177	8217	8225	8239	8248	8280	8352
. IIF														
432	531	536	545	554	565	574	577	593	598	607	610	612	617	626
629	631	636	645	648	650	655	663	666	683	688	698	701	703	708
717	720	727	730	732	737	750	754	756	761	771	774	776	781	794
798	827	832	841	844	846	851	859	862	864	869	877	880	882	887
895	898	900	905	918	922	924	929	943	947	948	953	954	967	972
977	988	994	999	1012	1016	1018	1023	1037	1041	1043	1048	1061	1065	1067
1072	1086	1090	1093	1098	1111	1115	1117	1122	1136	1140	1142	1147	1160	1164
1166	1171	1185	1199	1206	1211	1220	1223	1225	1230	1238	1241	1243	1248	1256
1259	1261	1266	1277	1293	1298	1308	1321	1325	1340	1345	1355	1368	1372	1535
1387	1392	1402	1415	1419	1434	1439	1449	1462	1466	1503	1508	1515	1526	1642
1538	1550	1555	1563	1580	1584	1592	1597	1604	1615	1619	1629	1634	1642	1654
1658	1667	1672	1682	1696	1700	1712	1717	1729	1743	1747	1759	1764	1776	1791
1795	1807	1812	1824	1839	1843	1850	1855	1868	1885	1889	1896	1901	1913	1924
1938	1948	1951	1952	1957	1970	1981	1994	2004	2007	2008	2013	2026	2041	2050
2053	2069	2074	2085	2098	2102	2116	2121	2134	2151	2155	2170	2175	2187	2203
2207	2208	2213	2230	2240	2251	2260	2271	2274	2284	2289	2299	2314	2318	2335
2340	2350	2363	2367	2377	2382	2392	2403	2407	2418	2423	2434	2445	2449	2451
2456	2469	2479	2488	2491	2492	2497	2514	2524	2534	2537	2538	2543	2559	2569
2572	2573	2578	2592	2605	2608	2618	2623	2624	2631	2643	2647	2658	2663	2676
2680	2690	2695	2708	2712	2722	2727	2741	2745	2754	2759	2773	2790	2794	2803
2808	2822	2833	2836	2846	2851	2865	2875	2890	2901	2904	2913	2918	2934	2945
2948	2959	2964	2981	2996	3007	3010	3019	3024	3038	3048	3051	3060	3065	3081
3092	3095	3104	3109	3124	3134	3137	3146	3151	3166	3176	3179	3187	3192	3203
3206	3214	3219	3230	3233	3241	3246	3259	3269	3272	3282	3287	3295	3308	3319
3334	3345	3348	3355	3360	3375	3386	3389	3396	3401	3411	3420	3430	3442	3452
3455	3461	3466	3480	3492	3496	3504	3509	3521	3524	3532	3537	3549	3552	3561
3566	3578	3581	3594	3599	3613	3623	3626	3635	3640	3653	3656	3665	3670	3681
3691	3694	3705	3710	3721	3730	3733	3741	3746	3759	3769	3772	3781	3786	3796
3799	3807	3812	3822	3825	3833	3838	3848	3851	3853	3858	3871	3881	3884	3886
3891	3904	3914	3917	3919	3924	3936	3947	3957	3960	3962	3967	3981	3991	4003
4014	4023	4026	4029	4034	4051	4061	4074	4085	4088	4090	4095	4110	4120	4129
4132	4134	4139	4154	4164	4174	4184	4193	4196	4198	4203				

4603	4608	4619	4628	4639	4649	4658	4661	4672	4677	4689	4699	4708	4719	4728
4731	4741	4746	4758	4768	4777	4788	4797	4800	4809	4814	4826	4836	4845	4855
4864	4867	4881	4886	4887	4898	4902	4919	4924	4925	4936	4940	4956	4961	4973
4976	4987	4992	5004	5007	5016	5021	5033	5048	5052	5063	5068	5081	5096	5113
5117	5126	5131	5146	5163	5182	5186	5195	5200	5211	5225	5239	5243	5253	5258
5272	5276	5288	5293	5294	5308	5312	5322	5327	5338	5342	5351	5356	5357	5368
5372	5383	5388	5396	5405	5509	5514	5524	5533	5536	5545	5554	5563	5572	5576
5482	5487	5496	5499	5509	5609	5623	5628	5629	5638	5642	5678	5683	5684	5693
5590	5595	5596	5605	5620	5633	5677	5791	5794	5813	5818	5819	5830	5849	5886
5716	5728	5737	5750	5763	5777	5774	5981	5990	5993	6008	6013	6024	6039	6043
5904	5920	5936	5955	5959	5969	5974	5981	5990	5993	6016	6117	6122	6135	6150
6044	6049	6061	6076	6080	6081	6086	6098	6112	6116	6252	6266	6282	6286	6298
6167	6172	6184	6200	6215	6219	6221	6225	6238	6255	6390	6394	6405	6410	6421
6315	6319	6321	6326	6338	6353	6357	6258	6363	6375	6390	6394	6405	6410	6421
6435	6449	6461	6476	6480	6482	6487	6499	6514	6529	6533	6545	6550	6563	6579
6595	6599	6601	6606	6618	6633	6649	6663	6667	6669	6674	6686	6690	6703	6708
6720	6735	6750	6765	6769	6770	6775	6788	6803	6818	6833	6837	6849	6854	6867
6882	6896	6912	6916	6917	6922	6935	6950	6965	6979	6983	6984	6989	7002	7017
7031	7048	7052	7053	7058	7071	7087	7102	7120	7124	7136	7141	7156	7176	7180
7189	7194	7210	7228	7232	7240	7245	7256	7272	7276	7284	7289	7297	7311	7321
7332	7336	7347	7352	7362	7377	7381	7383	7388	7399	7408	7411	7413	7430	
7439	7442	7444	7449	7460	7469	7472	7474	7479	7490	7499	7502	7504	7509	7520
7529	7532	7534	7539	7550	7559	7562	7572	7577	7586	7600	7603	7605	7610	7623
7633	7642	7645	7647	7652	7665	7675	7684	7687	7689	7694	7707	7717	7726	7729
7731	7736	7749	7759	7768	7771	7773	7778	7791	7801	7810	7813	7815	7820	7833
7843	7852	7855	7865	7870	7881	7884	7892	7897	7905	7917	7922	7923	7928	7938
7945	7957	7962	7970	7976	7981	7986	7996	8006	8009	8035	8040	8041	8070	8092
8097	8098	8130	8142	8147	8148	8154	8165	8170	8182	8201	8206	8207	8222	
8244	8252	8257	8258	8280	8352	8356	8360	8364	8368	8372	8376	8380		
1	404	408	417	422	534	537	546	552	555	566	572	575	596	599
605	608	615	618	624	627	634	637	643	646	653	656	661	664	686
689	696	699	706	709	715	718	725	728	735	738	748	752	759	782
769	772	779	782	792	796	830	833	839	842	849	852	857	860	867
870	875	878	885	888	893	896	903	906	916	920	927	930	941	945
951	954	968	975	978	990	997	1000	1010	1014	1021	1024	1035	1039	1046
1049	1059	1063	1070	1073	1084	1088	1096	1099	1109	1113	1120	1123	1134	1138
1145	1148	1158	1162	1169	1172	1183	1187	1209	1212	1218	1221	1228	1231	1236
1239	1246	1249	1254	1257	1264	1267	1272	1275	1296	1299	1306	1310	1319	1323
1343	1346	1353	1357	1366	1370	1390	1393	1400	1404	1413	1417	1437	1440	1447
1451	1460	1464	1506	1509	1513	1516	1524	1527	1533	1536	1553	1556	1561	1564
1578	1582	1595	1598	1602	1605	1613	1617	1632	1635	1640	1643	1652	1656	1670
1673	1680	1683	1694	1698	1715	1718	1726	1729	1741	1745	1762	1765	1774	
1789	1793	1810	1813	1822	1825	1837	1841	1853	1856	1866	1869	1883	1887	1899
1902	1911	1915	1922	1925	1936	1940	1946	1949	1955	1958	1968	1972	1979	
1992	1996	2002	2005	2011	2014	2024	2028	2039	2042	2048	2051	2072	2075	
2086	2096	2100	2119	2122	2238	2241	2249	2252	2258	2261	2269	2272	2287	
2211	2214	2228	2232	2238	2341	2348	2351	2361	2365	2380	2383	2390	2393	
2300	2312	2316	2338	2341	2443	2447	2454	2457	2467	2471	2477	2480	2486	
2421	2424	2432	2435	2525	2532	2535	2541	2544	2557	2561	2567	2570	2576	
2498	2512	2516	2522	2621	2624	2629	2632	2641	2645	2661	2664	2674	2678	
2593	2594	2603	2725	2728	2739	2743	2757	2760	2771	2775	2788	2792	2806	
2596	2706	2710	2834	2849	2852	2863	2867	2873	2876	2888	2892	2899	2902	
2820	2824	2831	2943	2946	2962	2965	2979	2983	2994	3005	3008	3022	3025	
2919	2932	2936												

**MAINDEC-11-DFKAA-B 11/34 CPU TEST  
DFKAAB.P11 CROSS REFERENCE TABL**

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M01

.MACRO  
.MCALL  
.MEXIT  
.NLIST

689	696	699	706	709	715	718	725	728	735	738	748	752	759	762
769	772	779	782	792	796	830	833	839	842	849	852	857	860	867
870	875	878	885	888	893	896	903	906	916	920	927	930	941	945
951	954	968	975	978	990	997	1000	1010	1014	1021	1024	1035	1039	1046
1049	1059	1063	1070	1073	1084	1088	1096	1099	1109	1113	1120	1123	1134	1138
1145	1148	1158	1162	1169	1172	1183	1187	1209	1212	1218	1221	1228	1231	1236
1239	1246	1249	1254	1257	1264	1267	1272	1275	1296	1299	1306	1310	1319	1323
1343	1346	1353	1357	1366	1370	1390	1393	1400	1404	1413	1417	1437	1440	1447
1451	1460	1464	1506	1509	1513	1516	1524	1527	1533	1536	1553	1556	1561	1564
1578	1582	1595	1598	1602	1605	1613	1617	1632	1635	1640	1643	1652	1656	1670
1673	1680	1683	1694	1698	1715	1718	1726	1729	1741	1745	1762	1765	1774	1777
1789	1793	1810	1813	1822	1825	1837	1841	1853	1856	1866	1869	1883	1887	1899
1902	1911	1915	1922	1925	1936	1940	1946	1949	1955	1958	1968	1972	1979	1982
1992	1996	2002	2005	2011	2122	2132	2135	2149	2153	2173	2176	2185	2072	2083
2086	2096	2100	2119	2122	2238	2241	2249	2252	2258	2261	2269	2272	2287	2290
2211	2214	2228	2232	2341	2348	2351	2361	2365	2380	2383	2390	2393	2401	2405
2300	2312	2316	2338	2435	2443	2447	2454	2457	2467	2471	2477	2480	2486	2495
2421	2424	2432	2522	2525	2532	2535	2541	2544	2557	2561	2567	2570	2576	2579
2498	2512	2516	2606	2621	2624	2629	2632	2641	2645	2661	2664	2674	2678	2693
2590	2594	2603	2710	2725	2728	2739	2743	2757	2760	2771	2775	2788	2792	2809
2896	2706	2831	2834	2849	2852	2863	2867	2873	2876	2888	2892	2899	2902	2916
2919	2932	2936	2943	2946	2962	2965	2979	2983	2994	2998	3005	3008	3022	3025
3036	3040	3046	3049	3063	3066	3079	3083	3090	3093	3107	3110	3122	3126	3132
3135	3149	3152	3164	3168	3174	3177	3190	3193	3201	3204	3217	3220	3228	3231
3244	3247	3257	3261	3267	3270	3285	3288	3293	3296	3306	3309	3317	3320	3332
3335	3343	3346	3358	3361	3373	3377	3384	3387	3399	3402	3409	3412	3418	3421
3428	3431	3440	3443	3450	3453	3464	3467	3478	3482	3490	3494	3507	3510	3519
3522	3535	3538	3547	3550	3564	3567	3576	3579	3597	3600	3611	3614	3621	3624
3638	3641	3651	3654	3668	3671	3679	3682	3689	3692	3708	3711	3719	3722	3728
3731	3744	3747	3757	3760	3767	3770	3784	3787	3794	3797	3810	3813	3820	3823
3836	3839	3846	3849	3856	3859	3869	3873	3879	3882	3889	3892	3902	3906	3912
3915	3922	3925	3934	3938	3945	3949	3955	3958	3965	3968	3979	3983	3989	3992
4001	4005	4012	4015	4021	4024	4032	4035	4049	4053	4059	4062	4072	4076	4083
4086	4093	4096	4108	4112	4118	4121	4127	4130	4137	4140	4152	4156	4162	4165
4172	4176	4182	4185	4191	4194	4201	4204	4216	4220	4226	4229	4235	4238	4245
4248	4259	4263	4269	4272	4278	4281	4288	4291	4302	4306	4312	4315	4321	4324
4337	4340	4350	4354	4360	4363	4376	4379	4388	4392	4399	4403	4409	4412	4424
4427	4435	4439	4445	4448	4456	4460	4466	4469	4475	4478	4490	4493	4502	4506
4512	4515	4521	4524	4531	4534	4541	4544	4557	4560	4569	4573	4579	4582	4588
4591	4606	4609	4617	4620	4626	4629	4637	4641	4647	4650	4656	4659	4675	4678
4687	4691	4697	4700	4706	4709	4717	4720	4726	4729	4744	4747	4756	4760	4766
4769	4775	4778	4786	4789	4795	4798	4812	4815	4824	4828	4834	4837	4843	4846
4853	4856	4862	4865	4884	4887	4896	4900	4922	4925	4934	4938	4959	4962	4973
4974	4990	4993	5002	5005	5019	5022	5031	5035	5046	5050	5066	5069	5079	5083
5094	5098	5111	5115	5129	5132	5144	5148	5161	5165	5180	5184	5198	5201	5209
5213	5223	5227	5237	5241	5256	5259	5270	5274	5291	5294	5306	5310	5325	5338
5336	5340	5354	5357	5366	5370	5386	5389	5394	5397	5403	5406	5420	5423	5430
5433	5448	5451	5458	5461	5467	5470	5485	5488	5494	5497	5512	5515	5522	5525
5531	5534	5551	5554	5561	5564	5570	5574	5593	5596	5603	5607	5626	5629	5638
5640	5681	5684	5691	5694	5700	5703	5714	5717	5726	5729	5735	5738	5748	5751
5761	5764	5775	5778	5789	5792	5816	5819	5832	5847	5851	5866	5870	5884	5888
5902	5906	5918	5922	5934	5938	5953	5957	5972	5975	5982	5988	5991	6011	6014
6022	6026	6037	6041	6047	6050	6059	6063	607						

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 DFKAAB.P11 C6055 REFERENCE TABLE -- PERMANENT SYMBOLS

6327	6336	6340	6351	6355	6361	6364	6373	6377	6385	6392	6408	6411	6419	6423
6433	6437	6447	6451	6459	6463	6474	6478	6485	6488	6497	6501	6512	6516	6527
6531	6548	6551	6561	6565	6577	6581	6592	6597	6604	6607	6616	6620	6631	6635
6641	6651	6661	6665	6672	6675	6684	6688	6706	6709	6718	6722	6733	6737	6748
6752	6763	6764	6773	6776	6786	6790	6801	6805	6816	6820	6831	6835	6852	6855
6865	6869	6880	6884	6894	6898	6910	6914	6920	6923	6933	6937	6948	6952	6963
6957	6977	6981	6987	6990	7000	7004	7015	7019	7029	7033	7046	7050	7056	7059
7069	7073	7085	7089	7090	7104	7118	7122	7139	7142	7154	7158	7174	7178	7192
7195	7208	7212	7226	7230	7243	7246	7254	7258	7270	7274	7287	7290	7298	7309
7313	7322	7330	7334	7350	7353	7360	7363	7375	7379	7386	7389	7397	7400	7406
7439	7446	7449	7428	7431	7437	7440	7447	7450	7458	7461	7467	7470	7477	7480
7488	7491	7497	7500	7507	7510	7518	7521	7527	7530	7537	7540	7548	7551	7557
7560	7575	7578	7584	7587	7598	7601	7608	7611	7621	7625	7631	7634	7640	7643
7650	7653	7663	7667	7673	7676	7682	7685	7692	7695	7705	7709	7715	7718	7724
7727	7734	7737	7747	7751	7757	7760	7766	7769	7776	7779	7789	7793	7799	7802
7808	7811	7818	7821	7831	7835	7841	7844	7850	7853	7868	7871	7879	7882	7885
7898	7906	7920	7923	7929	7936	7939	7946	7960	7963	7971	7977	7984	7987	7997
8004	8007	8038	8041	8071	8095	8098	8128	8132	8145	8148	8155	8168	8171	8180
8184	8204	8207	8220	8223	8242	8246	8255	8258	8282	8354	8358	8362	8366	8370
RACIX	8307	8324												
REX														
REP	417													
SEG	428	456	534	580	596	615	634	653	669	686	706	735	759	779
801	830	849	867	885	903	927	951	975	997	1021	1046	1070	1096	1120
1145	1169	1192	1209	1228	1246	1264	1278	1296	1343	1390	1437	1469	1506	1553
1595	1632	1670	1715	1762	1810	1853	1899	1955	2011	2072	2119	2173	2211	2287
2238	2380	2421	2454	2495	2541	2576	2621	2661	2693	2725	2757	2806	2849	2916
2962	3022	3063	3107	3149	3190	3217	3244	3285	3358	3399	3454	3507	3535	3564
3597	3638	3668	3708	3744	3784	3810	3836	3856	3889	3922	3965	4032	4093	4137
4201	4245	4288	4337	4376	4424	4490	4557	4606	4675	4744	4812	4884	4922	4959
4990	5019	5066	5129	5198	5256	5291	5325	5354	5386	5420	5448	5485	5512	5551
5593	5626	5681	5816	5972	6011	6047	6084	6120	6170	6224	6301	6324	6361	6408
6485	6548	6604	6572	6706	6773	6852	6920	6987	7056	7139	7192	7243	7287	7350
7386	7416	7447	7477	7507	7537	7575	7608	7650	7692	7734	7776	7818	7868	7895
7920	7960	7984	8038	8095	8145	8168	8204	8255						
TUE	434	435	436	437	438	439	440	441	445	446	447	472	473	474
WOR	426	434	435	436	437	438	439	440	441	445	446	472	473	474
	475	476												

ERRORS DETECTED: 0  
 DEFAULT GLOBALS GENERATED: 0

\* DFKAAB.SEG/SOL/CRF/PAGNUM/NL:TOC/DS:ERFZ=SYSMAC.CO,DFKAAB.P11  
 RUN-TIME: 88 120 21 SECONDS  
 RUN-TIME RATIO: 445/230=1.9  
 CORE USED: 34K (67 PAGES)

COA