

11/70

MEMORY MANAGEMENT DIAG  
MD-11-DEKBE-B

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1. ABSTRACT  
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THIS PROGRAM WILL TEST ALL OF THE MEMORY MANAGEMENT LOGIC AND ENABLE THE FIELD SERVICE REPRESENTATIVE TO ISOLATE THE DETECTED FAILURES TO A REPLACABLE MODULE. IT IS ASSUMED THAT BOTH THE CPU AND THE CACHE HAVE BEEN TESTED, OR ARE KNOWN TO BE FUNCTIONING CORRECTLY, AND THAT THE PROGRAM IS STARTED FROM ADDRESS 200. THIS WILL PROVIDE THE EARLIEST DETECTION OF MEMORY MANAGEMENT RELATED ERRORS AND ENABLE LOOPING ON THE ERROR INVOLVING MINIMUM LOGIC. THIS PROGRAM MAY ALSO EXPOSE FAULTS THAT ARE ON THE INTERFACE BETWEEN MEMORY MANAGEMENT AND OTHER SECTIONS OF THE COMPUTER.

THIS PROGRAM HAS BEEN SEGMENTED IN THE FOLLOWING WAY: ALL DATA TABLES, ERROR MESSAGES, AND SUBROUTINES RESIDE IN LOW CORE (VIRTUAL PAGES 0 & 1 IE. ADDRESSES 001100 THRU 037776). RIGHT NOW THE END OF THE SUBROUTINES IS AROUND 025000, SO THERE IS SOME ROOM FOR FUTURE EXPANSION. THE TEST CODE STARTS AT VIRTUAL PAGE 2 (ADDRESS 040000) AND EXPANDS TOWARD PAGE 4 (ADDRESS 100000). THE END OF THE PROGRAM IS NOW AROUND ADDRESS 074000, SO MODIFICATIONS CAN BE MADE WITHOUT RE-SEGMENTING THE PROGRAM.

THE REASON FOR THIS SEGMENTATION IS TWO-FOLD, FIRST IT ENABLES THE OPERATOR TO TELL FROM THE ADDRESS LIGHTS EXACTLY WHERE THE PROGRAM HAS HALTED OR "HUNG-UP". THAT IS, DID IT HALT IN THE ERROR ROUTINE OR IN A TRAP ROUTINE BECAUSE OF A CONDITION IMPOSSIBLE TO RECOVER FROM (ON PAGE 0 OR 1), OR DID IT GET "HUNG-UP" IN THE TEST CODE ON PAGE 2 OR 3. THE OTHER REASON IS THAT CERTAIN MEMORY MANAGEMENT FUNCTIONS LOCK UP THE VIRTUAL PC OF THE INSTRUCTION AND THE PROGRAM, IN ORDER TO OPERATE PROPERLY, MUST KNOW WHERE IT IS AT ALL TIMES. IT SEEMS MUCH SIMPLER FOR THE CODE TO START AT A PREDETERMINED BOUNDARY SO THAT IF THE MESSAGES CHANGE OR A NEW SUBROUTINE IS ADDED THE PAGE THAT THE CODE IS ON WILL REMAIN THE SAME.

EACH TEST WILL SET THE LOOP ON ERROR POINTER (\$LPERR) TO THE MINIMUM NECESSARY SETUP CODE, IF ANY, FOR THE FUNCTION UNDER TEST. A SYNCHRONIZATION INSTRUCTION (NOP) IS PROVIDED BEFORE THE INSTRUCTION(S) THAT TEST(S) EACH NEW FUNCTION. THIS WILL ENABLE THE FIELD SERVICE REPRESENTATIVE TO UTILIZE THE MICRO BREAK REGISTER TO GENERATE AN "EXTERNAL SYNC" PULSE ON THE BACK PLANE FOR BETTER PULSE RESOLUTION.

SECTION 8.2 OF THIS DOCUMENT CONTAINS SOME IDEAS THAT I HAD WHEN I WAS WRITING THIS PROGRAM ON HOW TO EFFECTIVELY UTILIZE IT TO MAKE FAULT ISOLATION EASIER. IF THESE IDEAS ARE NOT CORRECT OR NEED TO BE EXPANDED TO PROVIDE MORE INFORMATION PLEASE WRITE DOWN YOUR SUGGESTIONS AND FORWARD THEM TO THE DIAGNOSTIC DEPARTMENT.

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IT SHOULD BE NOTED THAT THIS PROGRAM DOES NOT CHECK OUT THE

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CONSOLE OR THE CONSOLE CABLES THAT PLUG INTO THE MEMORY  
MANAGEMENT BOARDS. THE PROGRAM ASSUMES THAT THOSE COMPONENTS  
HAVE BEEN TESTED OR ARE KNOWN TO BE GOOD.

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2. REQUIREMENTS  
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2.1 EQUIPMENT  
THE BASIC PDP-11/70 COMPUTER, INCLUDING AN OPERATING CPU, CACHE,  
AND MEMORY. AN LA-30 OR EQUIVALENT DEVICE IS ALSO NEEDED FOR  
ERROR MESSAGES, AND END OF PASS REPORTS.

2.2 STORAGE  
THIS PROGRAM REQUIRES 16K OF MEMORY TO LOAD AND AT LEAST 20K  
OF MEMORY TO RUN IN. IT WILL SCAN MEMORY FROM 16K TO 124K ON 2K  
BOUNDARIES, AND FROM 120K TO THE SIZE JUMPERS ON 8K BOUNDARIES.

2.3 PRELIMINARY PROGRAMS  
THE CPU AND CACHE DIAGNOSTICS SHOULD BE RUN BEFORE THIS PROGRAM.  
MAIN MEMORY SHOULD BE SCANNED FOR AT LEAST THE FIRST 28K TO SEE  
THAT A PROGRAM WILL EXECUTE CORRECTLY BEFORE ANY PROGRAM IS RUN.

3. LOADING PROCEDURE  
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3.1 METHOD  
THIS PROGRAM CAN BE LOADED FROM ANY DEVICE THAT IS SUPPORTED  
BY XXDP, AND SHOULD BE LOADED USING THE XXDP PROCEDURE FOR THAT  
DEVICE.

4. STARTING PROCEDURE  
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4.1 STARTING ADDRESSES  
200 THIS ADDRESS WILL RUN THE COMPLETE PROGRAM  
204 THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 2  
TEST THE READ/WRITE BITS IN THE MEMORY STATUS REGISTERS  
210 THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 3  
PAGE ADDRESS AND PAGE DESCRIPTOR TESTS  
214 THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 4  
RELOCATION AND ADDER TESTS  
220 THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 5  
MEMORY MANAGEMENT ABORTS AND TRAPS LOGIC TESTS  
224 THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 6  
D-SPACE TESTS, CORRECT TIMING OF I & D SPACE  
230 THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 7  
A & W BIT LOGIC TEST AND DUAL MAPPING TESTS  
234 THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 8  
MOVE FROM AND MOVE TO PERVIOUS MODE INSTRUCTION TESTS

4.2 PROGRAM AND OPERATOR ACTION  
AFTER THE PROGRAM IS LOADED, THE FIRST TIME IT IS RUN IT WILL  
IDENTIFY ITSELF AND RUN A QUICK VERIFY PASS. AT THE END OF  
EACH PASS THE PROGRAM WILL TYPE OUT THE PASS NUMBER AND THE

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TOTAL NUMBER OF ERRORS FOUND ON THAT PASS.

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4.3

SPECIAL STARTING PROCEDURE  
IF IT APPEARS THAT THE CACHE IS CAUSING SOME TROUBLE AND  
YOU STILL WANT TO RUN THIS PROGRAM, IT IS POSSIBLE TO RUN  
THIS PROGRAM WITH THE CACHE DISABLED. SIMPLY LOAD THE  
CACHE CONTROL REGISTER (17777746) WITH THE DESIRED NUMBER,  
THEN LOAD THE PC (17777707) WITH THE STARTING ADDRESS AND PRESS  
CONTINUE. THE PROGRAM WILL NOW RUN AS IF YOU HAD LOADED THE  
STARTING ADDRESS AND PRESSED START BUT NOW THE CACHE CONTROL  
REGISTER IS DISABLING THE CACHE.  
BIT00 -DISABLE TRAPS  
BIT01 -DISABLE UNIBUS TRAPS  
BIT02 -FORCE MISS ON READ GROUP 0  
BIT03 -FORCE MISS ON READ GROJP 1  
BIT04 -FORCE REPLACE GROUP 0  
BIT05 -FORCE REPLACE GROUP 1

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5. OPERATING PROCEDURE  
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5.1 OPERATIONAL SWITCH SETTINGS

SW15 1= HALT ON ERROR  
SW14 1= LOOP ON THE TEST THAT YOU ARE IN  
SW13 1= INHIBIT ALL ERROR TYPE OUTS  
SW12 1= INHIBIT TRACE TRAP ON EVERY OTHER PASS  
SW11 1= INHIBIT ITERATIONS AFTER FIRST PASS  
SW10 1= RING BELL ON ERROR  
SW09 1= LOOP ON ERROR  
SW08 1= LOOP ON TEST IN SWR<06:00>  
SW07 1= INHIBIT MULTIPLE ERROR TYPE OUTS

5.2 SUBROUTINE ABSTRACTS

ALL SUBROUTINE ABSTRACTS APPEAR IN THE CODE, BEFORE THEIR EXPANSION, AND IN THE DOCUMENT THAT IMMEDIATELY FOLLOWS THIS. THE FOLLOWING IS A LIST OF THEIR TITLES.

5.2.1 MACRO LIBRARY SUBROUTINES (FOUND IN MOST PROGRAMS)

END OF PASS ROUTINE  
SCOPE HANDLER ROUTINE  
ERROR HANDLER ROUTINE  
ERROR MESSAGE TYPE OUT ROUTINE  
CONVERT 16-BIT VIRTUAL ADDRESS TO 22-BIT PHYSICAL ADDRESS  
SAVE & RESTORE R0-R5 ROUTINES  
TYPE ROUTINE  
BINARY TO OCTAL (ASCII) AND TYPE ROUTINE  
CONVERT BINARY TO DECIMAL AND TYPE ROUTINE  
TRAP DECODER  
POWER DOWN AND UP ROUTINE  
DOUBLE LENGTH BINARY TO OCTAL ASCII CONVERT ROUTINE

5.2.2 SUBROUTINES UNIQUE TO THIS PROGRAM

TURN OFF AND SAVE T-BIT  
RESTORE T-BIT TO ITS PREVIOUS CONDITION  
CLEAR 16 PAR'S OR PDR'S STARTING FROM ADDRESS IN R5  
CLEANUP LOCATIONS THAT HOLD LOGICAL 'AND' AND 'OR'  
P.A.R. OR P.D.R. ADDRESS TIMED OUT WHEN REFERENCED  
DUAL ADDRESSING WHEN LOADING A P.A.R. OR P.D.R.  
COUNT PATTERN ERROR IN P.A.R.'S OR P.D.R.'S

5.2.3 TRAP AND ABORT HANDLER ROUTINES

CPU TRAP HANDLER  
CACHE TRAPS AND ABORTS HANDLER  
MEMORY MANAGEMENT TRAPS AND ABORTS HANDLER  
TRAP ROUTINES FOR ABORT IN SUPERVISOR AND USER MODE

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6. ERRORS  
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6.1 ERROR HALTS AND DESCRIPTION  
WHEN THE PROGRAM DETECTS AN ERROR CONDITION IT ISSUES AN  
"ERROR" (EMT) CALL. THIS CAUSES THE CPU TO TRAP TO THE  
"ERROR HANDLER ROUTINE" WHICH PRINTS OUT THE ERROR MESSAGE  
IF ANY, AND CHECKS THE SWITCH REGISTER FOR THE MODE SELECTED.  
THE PROGRAM WILL REACT AS FOLLOWS:  
HALT ON THE ERROR IF SW15=1, IS UP  
INHIBIT ERROR TYPE OUT IF SW13=1, IS UP  
RING BELL ON THE ERROR IF SW10=1, IS UP  
LOOP ON THE ERROR IF SW09=1, IS UP  
INHIBIT MULTIPLE TYPE OUTS IF SW07=1, IS UP

6.2 ERROR RECOVERY  
IF SWITCH 09 IS UP, THE PROGRAM WILL LOOP BACK TO WHERE THE  
LOOP ON ERROR POINTER (\$LPERR) IS SET. THIS WILL PROVIDE  
THE TIGHTEST POSSIBLE SCOPING LOOP, AND PROVIDES ALL NECESSARY  
SETUP CODE TO RECREATE THE ERROR. IF A SYNC POINT IS DESIRED  
TO EXTERNAL SYNC THE SCOPE JUST PRIOR TO THE FAILING OPERATION  
LOAD THE MICRO BREAK REGISTER WITH "044" AND USE THE "NOP"  
PROVIDED.

6.3 SAMPLE ERROR TYPE OUTS  
CPU TRAP OR ABORT THRU 'ERRVEC' (004) HAD INCORRECT CONDITION  
EXPECTD RECEIVD TESTNO PC AT ABORT  
000040 000020 000047 XXXXXX

THIS ERROR MESSAGE INDICATES THAT THE CPU TIMED OUT OVER THE  
UNIBUS WHEN IT WAS EXPECTING A CACHE NON-EXISTANT MEMORY TRAP.  
THIS TEST IS CHECKING THE CARRY PROPAGATION, THAT IS DETERMINED FROM  
LOOKING AT THE INDEX AT THE FRONT OF THE LISTING.

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3937. RESTRICTIONS  
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## 7.1 STARTING RESTRICTIONS

IF A STARTING POINT OTHER THAN "200" IS USED AND ERRORS ARE REPORTED, THEY MAY BE DUE TO LOGIC THAT IS ASSUMED TO BE WORKING AS A RESULT OF TESTS THAT WERE NOT RUN.

7.2 OPERATING RESTRICTIONS  
NONE8. MISCELLANEOUS  
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## 8.1 EXECUTION TIME

THE RUN TIME FOR A SINGLE PASS WITH NO ITERATIONS IS APPROXIMATELY 10 SECONDS.

## 8.2 HINTS ON HOW TO GET MORE INFORMATION FROM THE PROGRAM

IF AN ERROR OCCURS THE FIRST THING THAT SHOULD BE NOTED IS WHAT PASS DID THE ERROR OCCUR ON. IF THE PASS HAS AN EVEN NUMBER AND SWITCH 12 IS DOWN THEN THE ERROR MIGHT BE T-BIT SENSITIVE. TRY TO RUN AGAIN WITH SWITCH 12 UP, THIS WILL INHIBIT T-BIT TRAPPING.  
IF THE PASS NUMBER IS GREATER THAN ONE THE ERROR MIGHT BE ITERATION SENSITIVE. TRY TO RUN AGAIN WITH SWITCH 11 UP, THIS WILL INHIBIT ITERATIONS.  
NOW THAT YOU HAVE DETERMINED HOW TO MAKE THE MACHINE FAIL LOOK IN THE INDEX AT THE FRONT OF THE LISTING TO FIND THE TITLE OF THE TEST THAT WAS RUNNING WHEN THE ERROR CONDITION OCCURRED. GO TO THE LISTING AND READ THE PARAGRAPH AT THE BEGINNING OF THE TEST SO THAT YOU KNOW WHAT THE TEST IS TRYING TO DO. NOW READ THE ERROR MESSAGE AND IF THERE IS A COLUMN LABELED "ERRORPC" GO TO THAT LOCATION IN THE TEST. THIS IS THE PC OF THE "ERROR" STATEMENT. THE NUMBER IS THE ERROR MESSAGE NUMBER AND IN THE FRONT OF THE LISTING IS THE "ERROR MESSAGE POINTER TABLE" WHICH WILL TELL YOU WHAT WORDS WERE TYPED OUT.

IF YOU WANT TO SCOPE THIS ERROR CONDITION, PUT UP SWITCH 09 (LOOP ON ERROR) OR IF YOU WANT TO LOOP ON THE ENTIRE TEST PUT UP SWITCH 14. YOU WILL PROBABLY WANT TO INHIBIT THE ERROR TYPE OUT AT THIS POINT, SWITCH 13 WILL DO THAT.  
IF YOU NEED TO DO ACCURATE SCOPING AND NEED A GOOD SYNC POINT THEN MAKE SURE THAT THE MICRO BREAK REGISTER (177770) HAS "044" IN IT. THIS WILL CAUSE A PULSE ON THE BACK PLANE AT PIN # AE1 (SLOT 10) WHENEVER A "NOP" IS EXECUTED, AND THAT PULSE WILL MAKE AN EXCELLENT "EXTERNAL SYNC" SIGNAL FOR YOUR SCOPE. THERE IS A "NOP" JUST BEFORE EACH INSTRUCTION THAT TESTS A MEMORY MANAGEMENT FUNCTION FOR THE FIRST TIME, SO YOU SHOULD BE ABLE TO SCOPE ON ANY FAILURE THAT THIS PROGRAM CAN DETECT.

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9. PROGRAM DESCRIPTION

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THE DOCUMENT THAT FOLLOWS THIS ONE HAS A PARAGRAPH DESCRIBING  
EACH OF THE TESTS. THERE IS ALSO A PARAGRAPH DESCRIBING  
EACH MAJOR GROUP OF TESTS.

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DEKBE-8-D  
PRODUCT NAME: PDP-11/70 MEMORY MANAGEMENT DIAGNOSTIC  
DATE CREATED: 21-JUL-75  
MAINTAINER: DIAGNOSTIC ENGINEERING  
AUTHOR: DALE A. ROEDGER

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IT SHOULD BE NOTED THAT THIS PROGRAM DOES NOT CHECK OUT THE

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CONSOLE OR THE CONSOLE CABLES THAT PLUG INTO THE MEMORY  
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7142. REQUIREMENTS  
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THIS PROGRAM REQUIRES 16K OF MEMORY TO LOAD AND AT LEAST 20K OF MEMORY TO RUN IN. IT WILL SCAN MEMORY FROM 16K TO 124K ON 2K BOUNDARIES, AND FROM 120K TO THE SIZE JUMPERS ON 8K BOUNDARIES.
- 2.3 PRELIMINARY PROGRAMS  
THE CPU AND CACHE DIAGNOSTICS SHOULD BE RUN BEFORE THIS PROGRAM. MAIN MEMORY SHOULD BE SCANNED FOR AT LEAST THE FIRST 28K TO SEE THAT A PROGRAM WILL EXECUTE CORRECTLY BEFORE ANY PROGRAM IS RUN.

3. LOADING PROCEDURE  
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- 3.1 METHOD  
THIS PROGRAM CAN BE LOADED FROM ANY DEVICE THAT IS SUPPORTED BY XXDP, AND SHOULD BE LOADED USING THE XXDP PROCEDURE FOR THAT DEVICE.

4. STARTING PROCEDURE  
-----

- 4.1 STARTING ADDRESSES
- |     |   |
|-----|---|
| 200 | THIS ADDRESS WILL RUN THE COMPLETE PROGRAM  |
| 204 | THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 2<br>TEST THE READ/WRITE BITS IN THE MEMORY STATUS REGISTERS |
| 210 | THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 3<br>PAGE ADDRESS AND PAGE DESCRIPTOR TESTS                  |
| 214 | THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 4<br>RELOCATION AND ADDER TESTS                              |
| 220 | THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 5<br>MEMORY MANAGEMENT ABORTS AND TRAPS LOGIC TESTS          |
| 224 | THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 6<br>D-SPACE TESTS, CORRECT TIMING OF I & D SPACE            |
| 230 | THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 7<br>A & W BIT LOGIC TEST AND DUAL MAPPING TESTS             |
| 234 | THIS ADDRESS WILL START THE PROGRAM AT ENTRY POINT 8<br>MOVE FROM AND MOVE TO PERVIOUS MODE INSTRUCTION TESTS   |
- 4.2 PROGRAM AND OPERATOR ACTION  
AFTER THE PROGRAM IS LOADED, THE FIRST TIME IT IS RUN IT WILL IDENTIFY ITSELF AND RUN A QUICK VERIFY PASS. AT THE END OF EACH PASS THE PROGRAM WILL TYPE OUT THE PASS NUMBER AND THE

M02

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715

TOTAL NUMBER OF ERRORS FOUND ON THAT PASS.

716  
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719  
720  
721  
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735

4.3

SPECIAL STARTING PROCEDURE  
IF IT APPEARS THAT THE CACHE IS CAUSING SOME TROUBLE AND YOU STILL WANT TO RUN THIS PROGRAM, IT IS POSSIBLE TO RUN THIS PROGRAM WITH THE CACHE DISABLED. SIMPLY LOAD THE CACHE CONTROL REGISTER (17777746) WITH THE DESIRED NUMBER, THEN LOAD THE PC (17777707) WITH THE STARTING ADDRESS AND PRESS CONTINUE. THE PROGRAM WILL NOW RUN AS IF YOU HAD LOADED THE STARTING ADDRESS AND PRESSED START BUT NOW THE CACHE CONTROL REGISTER IS DISABLING THE CACHE.  
BIT00 -DISABLE TRAPS  
BIT01 -DISABLE UNIBUS TRAPS  
BIT02 -FORCE MISS ON READ GROUP 0  
BIT03 -FORCE MISS ON READ GROUP 1  
BIT04 -FORCE REPLACE GROUP 0  
BIT05 -FORCE REPLACE GROUP 1

5. OPERATING PROCEDURE  
-----

5.1 OPERATIONAL SWITCH SETTINGS

SW15	1=	HALT ON ERROR
SW14	1=	LOOP ON THE TEST THAT YOU ARE IN
SW13	1=	INHIBIT ALL ERROR TYPE OUTS
SW12	1=	INHIBIT TRACE TRAP ON EVERY OTHER PASS
SW11	1=	INHIBIT ITERATIONS AFTER FIRST PASS
SW10	1=	RING BELL ON ERROR
SW09	1=	LOOP ON ERROR
SW08	1=	LOOP ON TEST IN SWR<06:00>
SW07	1=	INHIBIT MULTIPLE ERROR TYPE OUTS

5.2 SUBROUTINE ABSTRACTS  
ALL SUBROUTINE ABSTRACTS APPEAR IN THE CODE, BEFORE THEIR EXPANSION, AND IN THE DOCUMENT THAT IMMEDIATELY FOLLOWS THIS. THE FOLLOWING IS A LIST OF THEIR TITLES.

5.2.1 MACRO LIBRARY SUBROUTINES (FOUND IN MOST PROGRAMS)

END OF PASS ROUTINE  
SCOPE HANDLER ROUTINE  
ERROR HANDLER ROUTINE  
ERROR MESSAGE TYPE OUT ROUTINE  
CONVERT 16-BIT VIRTUAL ADDRESS TO 22-BIT PHYSICAL ADDRESS  
SAVE & RESTORE RO-R5 ROUTINES  
TYPE ROUTINE  
BINARY TO OCTAL (ASCII) AND TYPE ROUTINE  
CONVERT BINARY TO DECIMAL AND TYPE ROUTINE  
TRAP DECODER  
POWER DOWN AND UP ROUTINE  
DOUBLE LENGTH BINARY TO OCTAL ASCII CONVERT ROUTINE

5.2.2 SUBROUTINES UNIQUE TO THIS PROGRAM

TURN OFF AND SAVE T-BIT  
RESTORE T-BIT TO ITS PREVIOUS CONDITION  
CLEAR 16 PAR'S OR PDR'S STARTING FROM ADDRESS IN R5  
CLEANUP LOCATIONS THAT HOLD LOGICAL 'AND' AND 'OR'  
P.A.R. OR P.D.R. ADDRESS TIMED OUT WHEN REFERENCED  
DUAL ADDRESSING WHEN LOADING A P.A.R. OR P.D.R.  
COUNT PATTERN ERROR IN P.A.R.'S OR P.D.R.'S

5.2.3 TRAP AND ABORT HANDLER ROUTINES

CPU TRAP HANDLER  
CACHE TRAPS AND ABORTS HANDLER  
MEMORY MANAGEMENT TRAPS AND ABORTS HANDLER  
TRAP ROUTINES FOR ABORT IN SUPERVISOR AND USER MODE

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C03

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11-11-75  
10:30  
9:30

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PAGE 8



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0100

7. RESTRICTIONS  
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7.1 STARTING RESTRICTIONS  
IF A STARTING POINT OTHER THAN "200" IS USED AND ERRORS ARE REPORTED, THEY MAY BE DUE TO LOGIC THAT IS ASSUMED TO BE WORKING AS A RESULT OF TESTS THAT WERE NOT RUN.

7.2 OPERATING RESTRICTIONS  
NONE

8. MISCELLANEOUS  
-----

8.1 EXECUTION TIME  
THE RUN TIME FOR A SINGLE PASS WITH NO ITERATIONS IS APPROXIMATELY 10 SECONDS.

8.2 HINTS ON HOW TO GET MORE INFORMATION FROM THE PROGRAM

IF AN ERROR OCCURS THE FIRST THING THAT SHOULD BE NOTED IS WHAT PASS DID THE ERROR OCCUR ON. IF THE PASS HAS AN EVEN NUMBER AND SWITCH 12 IS DOWN THEN THE ERROR MIGHT BE T-BIT SENSITIVE. TRY TO RUN AGAIN WITH SWITCH 12 UP, THIS WILL INHIBIT T-BIT TRAPPING.  
IF THE PASS NUMBER IS GREATER THAN ONE THE ERROR MIGHT BE ITERATION SENSITIVE. TRY TO RUN AGAIN WITH SWITCH 11 UP. THIS WILL INHIBIT ITERATIONS.  
NOW THAT YOU HAVE DETERMINED HOW TO MAKE THE MACHINE FAIL LOOK IN THE INDEX AT THE FRONT OF THE LISTING TO FIND THE TITLE OF THE TEST THAT WAS RUNNING WHEN THE ERROR CONDITION OCCURRED. GO TO THE LISTING AND READ THE PARAGRAPH AT THE BEGINNING OF THE TEST SO THAT YOU KNOW WHAT THE TEST IS TRYING TO DO. NOW READ THE ERROR MESSAGE AND IF THERE IS A COLUMN LABELED "ERRORPC" GO TO THAT LOCATION IN THE TEST. THIS IS THE PC OF THE "ERROR" STATEMENT. THE NUMBER IS THE ERROR MESSAGE NUMBER AND IN THE FRONT OF THE LISTING IS THE "ERROR MESSAGE POINTER TABLE" WHICH WILL TELL YOU WHAT WORDS WERE TYPED OUT.  
IF YOU WANT TO SCOPE THIS ERROR CONDITION, PUT UP SWITCH 09 (LOOP ON ERROR) OR IF YOU WANT TO LOOP ON THE ENTIRE TEST PUT UP SWITCH 14. YOU WILL PROBABLY WANT TO INHIBIT THE ERROR TYPE OUT AT THIS POINT, SWITCH 13 WILL DO THAT.  
IF YOU NEED TO DO ACCURATE SCOPING AND NEED A GOOD SYNC POINT THEN MAKE SURE THAT THE MICRO BREAK REGISTER (1777770) HAS "044" IN IT. THIS WILL CAUSE A PULSE ON THE BACK PLANE AT PIN # AE1 (SLOT 10) WHENEVER A "NOP" IS EXECUTED, AND THAT PULSE WILL MAKE AN EXCELLENT "EXTERNAL SYNC" SIGNAL FOR YOUR SCOPE. THERE IS A "NOP" JUST BEFORE EACH INSTRUCTION THAT TESTS A MEMORY MANAGEMENT FUNCTION FOR THE FIRST TIME, SO YOU SHOULD BE ABLE TO SCOPE ON ANY FAILURE THAT THIS PROGRAM CAN DETECT.

F03

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## 8.3

## ROM STATE DESCRIPTIONS

THIS IS A LIST OF THE ROM OUTPUTS FROM THE MEMORY MANAGEMENT ROMS ON 'SSRA', WITH A SENTENCE OR TWO DESCRIBING THEIR MEANING AS IT RELATES TO MEMORY MANAGEMENT.

## ROM OUT01 - ROM OUT03

THESE OUTPUTS ARE SENT TO MULTIPLEXERS AND REGISTERS ON 'SSRA' TO INDICATE A PARTICULAR MACHINE FUNCTION. THE ENCODING OF THESE OUTPUTS IS SHOWN IN A TRUTH TABLE ON 'SSRA'.

## ROM OUT04

DESTINATION MODE -- THIS IS USED TO ENABLE RELOCATION IF BIT08 OF MMRO IS SET AND THIS IS THE DESTINATION CYCLE OF THE INSTRUCTION.

## ROM OUT05

MFP + MTP -- THIS IS USED TO CLOCK THE PREVIOUS MODE INTO THE "SPACE" FLIP-FLOPS ON 'SSRB', DURING A MFP + MTP INST.

## ROM OUT06

TRAP OR ABORT -- THIS IS USED TO FORCE SETTING OF THE 'KERNEL SPACE' FLIP-FLOP ON 'SSRB' DURING A TRAP OR ABORT SEQUENCE.

## ROM OUT07

BUST -- THIS IS USED TO CLOCK MOST OF THE LATCHES IN MEMORY MANAGEMENT SUCH AS: 'SPACE' F/F'S, STATUS REGISTERS....

## ROM OUT08

MFP + MTP -- THIS ASSERTS 'SSRB I SPACEB' TO FORCE I-SPACE ON MFPI + MTP I INSTRUCTIONS IF THE PSW IS NOT (USER MODE/ PREVIOUS USER MODE).

## ROM OUT09

INST + INDEX FETCH -- THIS ASSERTS 'SSRB I SPACEA' WHICH FORCES I-SPACE DURING AN INSTRUCTION OR INDEX WORD FETCH.

## ROM OUT10

THIS DOES NOT EXIST.

## ROM OUT11

INST STARTED IN I-SPACE -- THIS ASSERTS 'SSRB I SPACEB' TO FORCE I-SPACE IF 'SSRB PREV=I' IS SET.

## ROM OUT12

CONSOLE -- THIS ASSERTS 'SSRB I SPACEA' IF 'SSRK CNSL I SPACE M' IS TRUE AND YOU EXAMINE OR DEPOSIT.

## ROM OUT13

SRCM = 1+2+3+4+5 -- IF THE SOURCE FIELD IS 7 THIS ASSERTS 'SSRB I SPACEB' WHICH FORCES I-SPACE.

## ROM OUT14

DSTM = 1+2 -- IF THE DESTINATION FIELD IS 7 THIS ASSERTS 'SSRB I SPACEB' WHICH FORCES I-SPACE.

H03

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ROM OUT15  
DSTM = 3 -- IF THE DESTINATION FIELD IS 7 THIS ASSERTS 'SSRB I SPACEA' WHICH FORCES I-SPACE DURING THE DESTINATION CYCLE.

ROM OUT16  
FLOATING POINT -- IF THE DSTF = 7 AND THE DSTM = 2 THEN THIS ASSERTS 'SSRB I SPACEA' WHICH FORCES I-SPACE ON IMMEDIATE F.P.INST.

NOTE: THE FOLLOWING ROM STATES ARE NOT EXPLICITLY TESTED DUE TO THE FACT THAT I COULDN'T FIGURE OUT A WAY TO TEST THEM UNDER RUN CONDITIONS. THE LOGIC ASSOCIATED WITH THEM HAS BEEN TESTED BY OTHER ROM STATES BUT THESE STATES ARE NOT TESTED.

ROM OUT05  
SHR.00, NEG.00, D12.90, D40.30, D12.30

ROM OUT09  
FET.06, FET.08, FET.09  
THESE NEXT ARE TESTED ON PASSES WITH T-BIT TRAPPING  
(PASS 2, 4)  
FET.01, FET.02, FET.03

ROM OUT12  
EXM.10, EXM.20, DEP.10, DEP.20

ROM OUT13  
S45.10

ROM OUT16 FLOATING POINT  
FSV.00, FSV.10

990  
991  
992  
993  
994  
995  
996  
997  
998  
999  
000

9. PROGRAM DESCRIPTION  
-----

THE DOCUMENT THAT FOLLOWS THIS ONE HAS A PARAGRAPH DESCRIBING  
EACH OF THE TESTS. THERE IS ALSO A PARAGRAPH DESCRIBING  
EACH MAJOR GROUP OF TESTS.

000001

2  
.END

K03

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DEKBEB.P11 CROSS REFERENCE TABLE -- USER SYMBOLS

DEKBER=	*****	GX	498
.MAIN.=	*****	GX	497

L03

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DEKBEB.P11 CROSS REFERENCE TABLE -- PERMANENT SYMBOLS

.END 990  
.REM 1 500

. ABS. 000000 000  
000004 001

% ERRORS DETECTED: 1  
% DEFAULT GLOBALS GENERATED: 2

\* DEKBEB.SEQ/SOL/CRF/PAGNUM=DEKBEB  
RUN-TIME: 3 5 0 SECONDS  
RUN-TIME RATIO: 52/8=5.8  
CORE USED: 5K (11 PAGES)

