MDE/T·11

SYS BUS DIAG
CVCDDBO

AH-T011B-MC
FICHE 1 OF 2

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IDENTIFICATION

PRODUCT CODE: AC-T009B-MC

PRODUCT NAME: CVCDDB0 MDE/T-11 SYS BUS DIAG

PRODUCT DATE: OCTOBER 1982

MAINTAINER: DIAGNOSTIC ENGINEERING

THE FOLLOWING ARE TRADEMARKS OF DIGITAL EQUIPMENT CORPORATION:

DIGITAL	PDP	UNIBUS	MASSBUS
DEC	DECUS	DECTAPE	

REVISION HISTORY

REVISION   DATA   REASONS
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A   SEPTEMBER 1981   FIRST RELEASE
B   APRIL 1982   FIXED PROBLEM THAT
                                       ALLOWED BOTH THE SIGNAL
                                       DBLD L AND THE SIGNAL
                                       COLB L TO BE ASSERTED
                                       AT THE SAME TIME.

TABLE OF CONTENTS

1.0   GENERAL INFORMATION

1.1   PROGRAM ABSTRACT

THE MDE/T-11 SYSTEM BUS DIAGNOSTIC WILL TEST THE LOGIC ON THE MEMORY
SIMULATOR, THE STATE ANALYZER, THE POD, AND THE TARGET EMULATOR
MODULES THAT WERE NOT TESTABLE RUNNING THE INDIVIDUAL MDE/T-11 MODULE
DIAGNOSTICS. THIS DIAGNOSTIC WILL NOT TEST THE SIGNALS TO AND FROM
THE TARGET SYSTEM FROM THE POD MODULE. THE PROGRAM WILL USE EACH
OF THE MDE/T-11 MODULES TO SETUP THE LOGIC TO TEST THE LOGIC THAT WAS
NOT TESTABLE PREVIOUSLY RUNNING THE INDIVIDUAL DIAGNOSTICS.

THIS DIAGNOSTIC HAS BEEN WRITTEN FOR USE WITH THE DIAGNOSTIC
RUNTIME SERVICES SOFTWARE (SUPERVISOR). THESE SERVICES PROVIDE
THE INTERFACE TO THE OPERATOR AND TO THE SOFTWARE ENVIRONMENT.
THIS PROGRAM CAN BE USED WITH XXDP+, ACT, APT, SLIDE AND PAPER
TAPE. FOR A COMPLETE DESCRIPTION OF THE RUNTIME SERVICES, REFER
TO THE XXDP+ USER'S MANUAL. THERE IS A BRIEF DESCRIPTION OF
THE RUNTIME SERVICES IN SECTION 2 OF THIS DOCUMENT.

NOTE: THIS PROGRAM HAS NOT BEEN TESTED IN THE APT ENVIRONMENT, HOWEVER,
         THE APT INTERFACE HAS BEEN PROVIDED IN THE DIAGNOSTIC.

NOTE: THE T-11 POD MUST BE CONNECTED TO THE TARGET EMULATOR MODULE
         AND DISCONNECTED FROM THE TARGET SYSTEM BEFORE THE EXECUTION
         OF THIS DIAGNOSTIC.

1.2   SYSTEM REQUIREMENTS

1. LSI-11 OR EQUIVALENT TYPE CPU WITH Q-BUS
2. MINIMUM OF 16K WORDS OF MEMORY
3. CONSOLE TERMINAL AND CONTROLLER
4. MDE/T-11 BACKPLANE AND CABLES
5. MEMORY SIMULATOR MODULE (M8740)
6. STATE ANALYZER MODULE (M8741)
7. TARGET EMULATOR MODULE (M8742)
8. T-11 POD
9. MXV11 MODULE AND MDE/T-11 ROMS
10. STORAGE DEVICE WITH CONTROLLER (OPTIONAL)
11. XXDP+ MEDIA FOR STORAGE DEVICE (OPTIONAL)

1.3   RELATED DOCUMENTS AND STANDARDS

CHQUS? XXDP+ USER'S MANUAL (THE ''?'' IN CHQUS INDICATES THE REVISION
LEVEL OF THE DOCUMENT. AT THE TIME THIS PROGRAM WAS WRITTEN, THE
REVISION LEVEL WAS ''E''.

1.4   DIAGNOSTIC HIERARCY PREREQUISITES

ALL HARDWARE THAT IS SPECIFIED IN SECTION 1.2 OF THIS DOCUMENT
MUST BE OPERATIONAL AND FREE OF ALL FAULTS.

1.5   ASSUMPTIONS

BEFORE THIS PROGRAM IS EXECUTED, IT IS ASSUMED THAT THE FOLLOWING
DIAGNOSTICS HAVE RUN SUCCESSFULLY.

        MDE/T-11 MEMORY SIMULATOR DIAGNOSTIC
        MDE/T-11 STATE ANALYZER DIAGNOSTIC
        MDE/T-11 TARGET EMULATOR DIAGNSOTIC

2.0   OPERATING INSTRUCTIONS

THIS SECTION CONTAINS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES.
FOR DETAILED INFORMATION, REFER TO THE XXDP+ USER'S MANUAL (CHQUS).

2.1   COMMANDS

THERE ARE ELEVEN LEGAL COMMANDS FOR THE DIAGNOSTIC RUNTIME SERVICES
(SUPERVISOR). THIS SECTION LISTS THE COMMANDS AND GIVES A VERY
BRIEF DESCRIPTION OF THEM. THE XXDP+ USER'S MANUAL HAS MORE DETAILS.

        COMMAND   EFFECT
        -------   ----------------------------------
        START   START THE DIAGNOSTIC FROM AN INITIAL STATE
        RESTART   START THE DIAGNOSTIC WITHOUT INITIALIZING
        CONTINUE   CONTINUE AT TEST THAT WAS INTERRUPTED (AFTER ^C)
        PROCEED   CONTINUE FROM AN ERROR HALT
        EXIT   RETURN TO XXDP+ MONITOR (XXDP+ OPERATION ONLY!)
        ADD   ACTIVATE A UNIT FOR TESTING (ALL UNITS ARE
                             CONSIDERED TO BE ACTIVE AT START TIME
        DROP   DEACTIVATE A UNIT
        PRINT   PRINT STATISTICAL INFORMATION (IF IMPLEMENTED
                             BY THE DIAGNOSTIC - SECTION 4.0)
        DISPLAY   TYPE A LIST OF ALL DEVICE INFORMATION
        FLAGS   TYPE THE STATE OF ALL FLAGS (SEE SECTION 2.3)
        ZFLAGS   CLEAR ALL FLAGS (SEE SECTION 2.3)

A COMMAND CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. SO
YOU MAY, FOR EXAMPLE, TYPE ''STA'' INSTEAD OF ''START''.

2.2   SWITCHES

THERE ARE SEVERAL SWITCHES WHICH ARE USED TO MODIFY SUPERVISOR OPERATION.
THESE SWITCHES ARE APPENDED TO THE LEGAL COMMANDS. ALL OF THE LEGAL
SWITCHES ARE TABULATED BELOW WITH A BRIEF DESCRIPTION OF EACH.
IN THE DESCRIPTIONS BELOW, A DECIMAL NUMBER IS DESIGNATED BY ''DDDDD''.

        SWITCH   EFFECT
        ------   ------------------------------------
        /TESTS:LIST   EXECUTE ONLY THOSE TESTS SPECIFIED IN
                             THE LIST.   LIST IS A STRING OF TEST
                             NUMBERS, FOR EXAMPLE - /TESTS:1:5:7-10.
                             THIS LIST WILL CAUSE TESTS 1,5,7,8,9,10 TO
                             BE RUN. ALL OTHER TESTS WILL NOT BE RUN.
        /PASS:DDDDD   EXECUTE DDDDD PASSES (DDDDD = 1 TO 64000)
        /FLAGS:FLGS   SET SPECIFIED FLAGS. FLAGS ARE DESCRIBED
                             IN SECTION 2.3.
        /EOP:DDDDD   REPORT END OF PASS MESSAGE AFTER EVERY
                             DDDDD PASSES ONLY. (DDDDD = 1 TO 64000)

```
              /UNITS:LIST       TEST/ADD/DROP ONLY THOSE UNITS SPECIFIED
                                IN THE LIST.  LIST EXAMPLE - /UNITS:0:5:10-12
                                USE UNITS 0,5,10,11,12 (UNIT NUMBERS = 0-63)
```

EXAMPLE OF SWITCH USAGE:

          START/TESTS:1-5/PASS:1000/EOP:100

THE EFFECT OF THIS COMMAND WILL BE: 1) TESTS 1 THROUGH 5 WILL BE
EXECUTED, 2) ALL UNITS WILL BE TESTED 1000 TIMES AND 3) THE END OF
PASS MESSAGES WILL BE PRINTED AFTER EACH 100 PASSES ONLY. A
SWITCH CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. YOU MAY,
FOR EXAMPLE, TYPE "/TES:1-5" INSTEAD OF "/TESTS:1-5".

BELOW IS A TABLE THAT SPECIFIES WHICH SWITCHES CAN BE USED BY EACH
COMMAND.

```
              TESTS   PASS   FLAGS   EOP    UNITS
              ----------------------------------------
START           X       X      X      X       X
RESTART         X       X      X      X       X
CONTINUE                X      X      X
PROCEED                        X
DROP                                          X
ADD                                           X
PRINT
DISPLAY                                       X
FLAGS
ZFLAGS
EXIT
```

2.3   FLAGS

FLAGS ARE USED TO SET UP CERTAIN OPERATIONAL PARAMETERS SUCH AS
LOOPING ON ERROR. ALL FLAGS ARE CLEARED AT STARTUP AND REMAIN
CLEARED UNTIL EXPLICITLY SET USING THE FLAGS SWITCH. FLAGS
ARE ALSO CLEARED AFTER A START COMMAND UNLESS SET USING THE
FLAG SWITCH. THE ZFLAGS COMMAND MAY ALSO BE USED TO CLEAR
ALL FLAGS. WITH THE EXCEPTION OF THE START AND ZFLAGS COMMANDS,
NO COMMANDS AFFECT THE STATE OF THE FLAGS; THEY REMAIN SET OR
CLEARED AS SPECIFIED BY THE LAST FLAG SWITCH.

```
              FLAG             EFFECT
              ----             ------------------------------------
              HOE              HALT ON ERROR - CONTROL IS RETURNED TO
                               RUNTIME SERVICES COMMAND MODE
              LOE              LOOP ON ERROR
              IER*             INHIBIT ALL ERROR REPORTS
              IBE*             INHIBIT ALL ERROR REPORTS EXCEPT
                               FIRST LEVEL  (FIRST LEVEL CONTAINS
                               ERROR TYPE, NUMBER, PC, TEST AND UNIT)
              IXE*             INHIBIT EXTENDED ERROR REPORTS (THOSE
                               CALLED BY PRINTX MACRO'S)
              PRI              DIRECT MESSAGES TO LINE PRINTER
              PNT              PRINT TEST NUMBER AS TEST EXECUTES
```

```
            BOE              "BELL" ON ERROR
            UAM              UNATTENDED MODE (NO MANUAL INTERVENTION)
            ISR              INHIBIT STATISTICAL REPORTS (DOES NOT
                             APPLY TO DIAGNOSTICS WHICH DO NOT SUPPORT
                             STATISTICAL REPORTING)
            IDR              INHIBIT PROGRAM DROPPING OF UNITS
            ADR              EXECUTE AUTODROP CODE
            LOT              LOOP ON TEST
            EVL              EXECUTE EVALUATION (ON DIAGNOSTICS WHICH
                             HAVE EVALUATION SUPPORT)
```

          *ERROR MESSAGES ARE DESCRIBED IN SECTION 3.1

SEE THE XXDP+ USER'S MANUAL FOR MORE DETAILS ON FLAGS. YOU MAY
SPECIFY MORE THAN ONE FLAG WITH THE FLAG SWITCH. FOR EXAMPLE,
TO CAUSE THE PROGRAM TO LOOP ON ERROR, INHIBIT ERROR REPORTS
AND TYPE A "BELL" ON ERROR, YOU MAY USE THE FOLLOWING STRING:

        /FLAGS:LOE:IER:BOE

2.4 HARDWARE QUESTIONS

WHEN A DIAGNOSTIC IS STARTED, THE RUNTIME SERVICES WILL PROMPT
THE USER FOR HARDWARE INFORMATION BY TYPING "CHANGE HW (L) ?"
YOU MUST ANSWER "Y" AFTER A START COMMAND UNLESS THE HARDWARE
INFORMATION HAS BEEN "PRELOADED" USING THE SETUP UTILITY (SEE
CHAPTER 6 OF THE XXDP+ USER'S MANUAL). WHEN YOU ANSWER THIS
QUESTION WITH A "Y", THE RUNTIME SERVICES WILL ASK FOR THE NUMBER
OF UNITS (IN DECIMAL). YOU WILL THEN BE ASKED THE FOLLOWING
QUESTIONS FOR EACH UNIT.

CSR ADDRESS:
VECTOR ADDRESS:
DEVICE NUMBER FOR MEMORY SIMULATOR:
DEVICE NUMBER FOR STATE ANALYZER:
DEVICE NUMBER FOR TARGET EMULATOR:

2.5 SOFTWARE QUESTIONS

AFTER YOU HAVE ANSWERED THE HARDWARE QUESTIONS OR AFTER A RESTART
OR CONTINUE COMMAND, THE RUNTIME SERVICES WILL ASK FOR SOFTWARE
PARAMETERS. THESE PARAMETERS WILL GOVERN SOME DIAGNOSTIC SPECIFIC
OPERATION MODES. YOU WILL BE PROMPTED BY "CHANGE SW (L) ?"
IF YOU WISH TO CHANGE ANY PARAMETERS, ANSWER BY TYPING
"Y". THE SOFTWARE QUESTIONS AND THE DEFAULT VALUES ARE DESCRIBED
IN THE NEXT PARAGRAPH(S).

THERE ARE NO SOFTWARE QUESTIONS IN THIS PROGRAM.

2.6 EXTENDED P-TABLE DIALOGUE

WHEN YOU ANSWER THE HARDWARE QUESTIONS, YOU ARE BUILDING ENTRIES

IN A TABLE THAT DESCRIBES THE DEVICES UNDER TEST. THE SIMPLEST
WAY TO BUILD THIS TABLE IS TO ANSWER ALL QUESTIONS FOR EACH
UNIT TO BE TESTED. IF YOU HAVE A MULTIPLEXED DEVICE SUCH AS
A MASS STORAGE CONTROLLER WITH SEVERAL DRIVES OR A COMMUNICATION
DEVICE WITH SEVERAL LINES, THIS BECOMES TEDIOUS SINCE MOST OF
THE ANSWERS ARE REPETITIOUS.

TO ILLUSTRATE A MORE EFFICIENT METHOD, SUPPOSE YOU ARE TESTING
A FICTIONAL DEVICE, THE XY11. SUPPOSE THIS DEVICE CONSISTS OF
A CONTROL MODULE WITH EIGHT UNITS (SUB-DEVICES) ATTACHED TO IT.
THESE UNITS ARE DESCRIBED BY THE OCTAL NUMBERS 0 THROUGH 7. THERE
IS ONE HARDWARE PARAMETER THAT CAN VARY AMONG UNITS CALLED THE
Q-FACTOR. THIS Q-FACTOR MAY BE 0 OR 1. BELOW IS A SIMPLE WAY
TO BUILD A TABLE FOR ONE XY11 WITH EIGHT UNITS.

```
# UNITS (D) ?  8<CR>

UNIT 1
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  0<CR>
Q-FACTOR (O) 0 ?  1<CR>

UNIT 2
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  1<CR>
Q-FACTOR (O) 1 ?  0<CR>

UNIT 3
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  2<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 4
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  3<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 5
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  4<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 6
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  5<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 7
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  6<CR>
Q-FACTOR (O) 0 ?  1<CR>

UNIT 8
CSR ADDRESS (O)  160000<CR>
SUB-DEVICE # (O) ?  7<CR>
Q-FACTOR (O) 1 ?  <CR>
```

NOTICE THAT THE DEFAULT VALUE FOR THE Q-FACTOR CHANGES WHEN A
NON-DEFAULT RESPONSE IS GIVEN. BE CAREFUL WHEN SPECIFYING
MULTIPLE UNITS!

AS YOU CAN SEE FROM THE ABOVE EXAMPLE, THE HARDWARE PARAMETERS
DO NOT VARY SIGNIFICANTLY FROM UNIT TO UNIT. THE PROCEDURE SHOWN IS
NOT VERY EFFICIENT.

THE RUNTIME SERVICES CAN TAKE MULTIPLE UNIT SPECIFICATIONS HOWEVER.
LET'S BUILD THE SAME TABLE USING THE MULTIPLE SPECIFICATION
FEATURE.

```
# UNITS (D) ?  8<CR>

UNIT 1
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  0,1<CR>
Q-FACTOR (O) O ?  1,0<CR>

UNIT 3
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  2-5<CR>
Q-FACTOR (O) O ?  0<CR>

UNIT 7
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  6,7<CR>
Q-FACTOR (O) O ?  1<CR>
```

AS YOU CAN SEE IN THE ABOVE DIALOGUE, THE RUNTIME SERVICES WILL
BUILD AS MANY ENTRIES AS IT CAN WITH THE INFORMATION GIVEN IN ANY
ONE PASS THROUGH THE QUESTIONS. IN THE FIRST PASS, TWO ENTRIES
ARE BUILT SINCE TWO SUB-DEVICES AND Q-FACTORS WERE SPECIFIED. THE
SERVICES ASSUME THAT THE CSR ADDRESS IS 160000 FOR BOTH SINCE IT
WAS SPECIFIED ONLY ONCE. IN THE SECOND PASS, FOUR ENTRIES WERE
BUILT. THIS IS BECAUSE FOUR SUB-DEVICES WERE SPECIFIED. THE
"-" CONSTRUCT TELLS THE RUNTIME SERVICES TO INCREMENT THE DATA
FROM THE FIRST NUMBER TO THE SECOND. IN THIS CASE, SUB-DEVICES
2, 3, 4 AND 5 WERE SPECIFIED. (IF THE SUB-DEVICE WERE SPECIFIED
BY ADDRESSES, THE INCREMENT WOULD BE BY 2 SINCE ADDRESSES MUST
BE ON AN EVEN BOUNDARY.) THE CSR ADDRESSES AND Q-FACTORS FOR
THE FOUR ENTRIES ARE ASSUMED TO BE 160000 AND 0 RESPECTIVELY
SINCE THEY WERE ONLY SPECIFIED ONCE. THE LAST TWO UNITS ARE
SPECIFIED IN THE THIRD PASS.

THE WHOLE PROCESS COULD HAVE BEEN ACCOMPLISHED IN ONE PASS AS
SHOWN BELOW.

```
# UNITS (D) ?  8<CR>

UNIT 1
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  0-7<CR>
Q-FACTOR (O) O ?  0,1,0,...,1,1<CR>
```

AS YOU CAN SEE FROM THIS EXAMPLE, NULL REPLIES (COMMAS ENCLOSING
A NULL FIELD) TELL THE RUNTIME SERVICES TO REPEAT THE LAST REPLY.

2.7 QUICK START-UP PROCEDURE (XXDP+)

    NOTE: THE T-11 POD MUST BE CONNECTED TO THE TARGET EMULATOR AND
           DISCONNECTED FROM THE TARGET SYSTEM BEFORE EXECUTION OF THIS
           DIAGNOSTIC.

TO START-UP THIS PROGRAM:

        1. BOOT XXDP+

        2. ANSWER ANY QUESTIONS ASKED AND GIVE THE DATE.

        3. TYPE ''R NAME'', WHERE NAME IS THE NAME OF THE BIN OR BIC
           FILE FOR THIS PROGRAM

        4. TYPE ''START''

        5. ANSWER THE ''CHANGE HW'' QUESTION WITH ''Y''

        6. ANSWER ALL THE HARDWARE QUESTIONS

        7. ANSWER THE ''CHANGE SW'' QUESTION WITH ''N''

WHEN YOU FOLLOW THIS PROCEDURE YOU WILL BE USING ONLY THE
DEFAULTS FOR FLAGS AND SOFTWARE PARAMETERS. THESE DEFAULTS
ARE DESCRIBED IN SECTIONS 2.3 AND 2.5.

3.0 ERROR INFORMATION

3.1 TYPES OF ERROR MESSAGES

THERE ARE THREE LEVELS OF ERROR MESSAGES THAT MAY BE ISSUED BY
A DIAGNOSTIC: GENERAL, BASIC AND EXTENDED. GENERAL ERROR MESSAGES
ARE ALWAYS PRINTED UNLESS THE ''IER'' FLAG IS SET (SECTION 2.3).
THE GENERAL ERROR MESSAGE IS OF THE FORM:

        NAME   TYPE   NUMBER   ON UNIT NUMBER   TST NUMBER PC:XXXXXX
        ERROR MESSAGE

.WHERE; NAME = DIAGNOSTIC NAME
        TYPE = ERROR TYPE (SYS FATAL, DEV FATAL, HARD OR SOFT)
        NUMBER = ERROR NUMBER
        UNIT NUMBER = 0 - N (N IS LAST UNIT IN PTABLE)
        TST NUMBER = TEST AND SUBTEST WHERE ERROR OCCURRED
        PC:XXXXXX = ADDRESS OF ERROR MESSAGE CALL

BASIC ERROR MESSAGES ARE MESSAGES THAT CONTAIN SOME ADDITIONAL
INFORMATION ABOUT THE ERROR. THESE ARE ALWAYS PRINTED UNLESS
THE ''IER'' OR ''IBE'' FLAGS ARE SET (SECTION 2.3). THESE MESSAGES
ARE PRINTED AFTER THE ASSOCIATED GENERAL MESSAGE.

EXTENDED ERROR MESSAGES CONTAIN SUPPLEMENTARY ERROR INFORMATION
SUCH AS REGISTER CONTENTS OR GOOD/BAD DATA. THESE ARE ALWAYS

PRINTED UNLESS THE "IER", "IBE" OR "IXE" FLAGS ARE SET (SECTION 2.3).
THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL ERROR
MESSAGE AND ANY ASSOCIATED BASIC ERROR MESSAGES.

3.2 SPECIFIC ERROR MESSAGES

WHEN AN ERROR IS REPORTED ON THE CONSOLE TERMINAL, THE USER SHOULD
REFER TO THE PROGRAM LISTING FOR THE TEST SEQUENCE BEING PERFORMED
AT THE TIME THE ERROR WAS DETECTED. THE "PC" REPORTED IN THE ERROR
MESSAGE INDICATES THE ADDRESS OF THE ERROR CALL. EACH STEP OF A TEST
IS DESCRIBED IN DETAIL TO HELP THE USER UNDERSTAND THE TEST SEQUENCE.
ONCE UNDERSTANDING THE TEST SEQUENCE, THE USER SHOULD BE ABLE TO
DETERMINE THE FAULT OR FAULTS WHICH COULD CAUSE THE ERROR.

AN EXAMPLE OF AN ERROR PRINTOUT IS SHOWN BELOW:

```
CVCDD DVC FTL ERR 0000X ON UNIT 00 TST 001 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG X ERROR
REGX = LOAD: XXXXXX READ: XXXXXX
                 OR
REGX = LOAD: XXXXXX GOOD: XXXXXX READ: XXXXXX
```

THE FIRST LINE OF THE ERROR PRINTOUT ABOVE IS DESCRIBED IN SECTION 3.1
OF THIS DOCUMENT. THE ERROR NUMBER, 0000X, IN THE FIRST LINE OF THE
ERROR PRINTOUT WILL INDICATE THE CONTROL REGISTER THAT THE PROGRAM
DETECTED AN ERROR IN, AND THE MODULE THAT WAS SELECTED AT THE TIME THE
ERROR OCCURED. USING THE ERROR NUMBER PRINTED IN THE ERROR MESSAGE,
DETERMINE FROM THE TABLE BELOW WHICH MODULE WAS SELECTED AND WHICH
CONTROL REGISTER WAS IN ERROR.

CONTROL REG IN ERROR	MEMORY SIMULATOR ERROR NUMBERS	STATE ANALYZER ERROR NUMBERS	TARGET EMULATOR ERROR NUMBERS
0	1	5	9
2	2	6	10
4	3	7	11
6	4	8	12

TO HELP THE USER TO DETERMINE THE FAILURE, THE PROGRAM WILL PRINT THE
SECOND LINE OF THE ABOVE ERROR MESSAGE. THIS MESSAGE WILL ATTEMPT TO
INDICATE TO THE USER THE AREA OF LOGIC BEING TESTED AT THE TIME THE
FAILURE OCCURED. THIS "ERROR TYPE MESSAGE" WILL NOT BE PRINTED FOR
ALL ERRORS.

THE "ERROR TYPE MESSAGES" ARE LISTED BELOW BY MODULES AND THE CONTROL
REGISTERS FOR WHICH THEY ARE REPORTED.

```
MEMORY SIMULATOR MODULE
   CONTROL REGISTER 0
      NO "ERROR TYPE MESSAGES" FOR THIS CONTROL REGISTER
   CONTROL REGISTER 2
      TE TO MS ADDRESS BUS ERROR - MSAD 17:16
      MAP PROTECT LOGIC ERROR
   CONTROL REGISTER 4
```

                    MSAD 15:0 REG ERROR
                    TE TO MS ADDRESS BUS ERROR - MSAD 15:0
                 CONTROL REGISTER 6
                    DATA ERROR IN MAP PROTECT RAM
                    DATA ERROR IN MODULE SELECT RAM 0
                    DATA ERROR IN MODULE SELECT RAM 1
                    DATA ERROR IN MEMORY SIMULATOR RAM

              STATE ANALYZER MODULE
                 CONTROL REGISTER 0
                    CDAL 15:0 REG ERROR
                 CONTROL REGISTER 2
                    PDAL 7:0 REG ERROR
                 CONTROL REGISTER 4
                    OR ARRAY RAM DATA ERROR - ORO 7:0
                    FUSL7 FLIP-FLOP - OR ARRAY RAM DATA ERROR
                 CONTROL REGISTER 6
                    TE TO SA ADDRESS BUS ERROR - TRDI 15:0
                    TE TO SA - XSEL1, EDSEL0, ADDR 17:16 + BTS 3:0 ERROR - TRDI 47:32
                    TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:40 ERROR
                    MS RAM DATA TO SA TRDI BUS BITS 31:16 ERROR
                    TRACE RAM ADDRESS REG ERROR - TRAD 10:0
                    OR ADDRESS REG ERROR - ORAD 3:0
                    FUSL 3:0 FLIP-FLOP ERROR

              TARGET EMULATOR MODULE
                 CONTROL REGISTER 0
                    GDAL 15:0 REG ERROR
                 CONTROL REGISTER 2
                    ADAL 15:0 REG ERROR
                 CONTROL REGISTER 4
                    VDAL 7:0 OR PAUSE STATE MACHINE ERROR
                 CONTROL REGISTER 6
                    HDAL 15:0 REG ERROR
                    MR 15:0 REG ERROR
                    FDAL 7:0 REG ERROR
                    EOAI 7:0 OR FDAL 7:0 REG ERROR
                    CTL 7:0 OR FDAL 7:0 REG ERROR
                    DIAG ADDR 15:0 REG ERROR
                    FORCE JUMP ADDRESS READBACK REG ERROR
                    MS RAM DATA TO TE EODAL BUS ERROR VIA SYSTEM DATA BUS
                    MS RAM DATA TO TE EIDAL BUS ERROR VIA EODAL + SYSTEM DATA BUS
                    MS RAM DATA TO TE EIDAL BUS ERROR VIA TDAL BUS LATCHES
                    MEMBRK H FAILED TO SET BREAK FLIP-FLOP OR FAILED TO INTERRUPT
                    FDAL REG 7:2 TO EODAL BUS ERROR
                    FDAL REG 7:2 TO EIDAL BUS ERROR
                    FDAL REG 7:2 TO TDAL LATCHES TO EIDAL BUS ERROR

        THE THIRD LINE OF THE ERROR PRINTOUT, WHICH MAY BE THE SECOND LINE
        IF THE "ERROR TYPE MESSAGE" IS NOT PRINTED, WILL INDICATE THE CONTROL
        REGISTER (0, 2, 4 OR 6) THAT THE PROGRAM DETECTED IN ERROR.

        THE LAST PORTION OF THE ERROR PRINTOUT WILL INDICATE CONTROL REGISTER
        INFORMATION. ON SOME ERRORS, DATA FOR MORE THEN ONE CONTROL REGISTER
        WILL BE PRINTED OUT. THIS IS DONE TO HELP THE USER TO DETERMINE THE
        FAULT ON ERRORS WHICH REQUIRE PREVIOUS CONTROL REGISTER SETUP. IF

MORE THEN ONE CONTROL REGISTER IS PRINTED, THE PREVIOUS MESSAGE "CONTROL
REG X ERROR" WILL INDICATE THE CONTROL REGISTER THAT THE PROGRAM FOUND
IN ERROR. A DESCRIPTION OF THE WORDS USED TO INDICATE CONTROL REGISTER
INFORMATION IS AS FOLLOWS:

REGX: "X" OF "REGX" WILL INDICATE THE CONTROL REGISTER FOR
                WHICH THE FOLLOWING DATA IS REPORTED. "X" WILL BE
                A 0, 2, 4 OR 6.

LOAD: DATA THAT WAS LOADED INTO THE CONTROL REGISTER OR THE
                EXPECTED DATA TO BE IN THE CONTROL REGISTER ON A READ.

GOOD: EXPECTED DATA TO BE IN THE CONTROL REGISTER ON A READ.
                THIS PORTION OF THE CONTROL REGISTER INFORMATION WILL
                ONLY BE PRINTED IN THE PROGRAM EXPECTS "READ ONLY" BITS
                OF THE CONTROL REGISTER TO BE SET.

READ: DATA THAT WAS READ FROM CONTROL REGISTER VIA THE PROGRAM

XXXXXX: SIX OCTAL DIGITS INDICATING THE DATA FOR THE ABOVE WORDS

4.0 PERFORMANCE AND PROGRESS REPORTS

AT THE END OF EACH PASS, THE PASS COUNT IS GIVEN ALONG WITH THE
TOTAL NUMBER OF ERRORS REPORTED SINCE THE DIAGNOSTIC WAS STARTED.
THE "EOP" SWITCH CAN BE USED TO CONTROL HOW OFTEN THE END
OF PASS MESSAGE IS PRINTED. SECTION 2.2 DESCRIBES SWITCHES.

5.0 DEVICE INFORMATION TABLES

5.1 DEVICE INFORMATION FOR MEMORY SIMULATOR

CONTROL REGISTER 0 (163010)

    15 ID H   BIT15 = 1 READ DEVICE TYPE IN BITS 11:8, MEMORY
                 SIMULATOR DEVICE TYPE EQUALS 1 (0400)

                 BIT 15 = 0 READ DEVICE NUMBER INTO BITS 11:8

    14 SIG14H   ALWAYS A 0 ON READ
    13 SIG13H   ALWAYS A 0 ON READ
    12 SIG12H   ALWAYS A 0 ON READ

                 BITS 11:8 ARE USED TO SELECT THE DEVICE NUMBER OF
                 THE MEMORY SIMULATOR. THESE BITS MUST BE EQUAL TO
                 THE SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.

    11 SIG11H   DEVICE NUMBER/TYPE
    10 SIG10H   DEVICE NUMBER/TYPE
     9 SIG9H   DEVICE NUMBER/TYPE
     8 SIG8H   DEVICE NUMBER/TYPE

     7   SPARE

     6 CKH   CLOCK HIGH (R/W)
     5 WRVH   WRITE VIOLATION F/F (READ ONLY)

```
           4   RDVH      READ VIOLATION F/F (PEAD ONLY)
           3   8BITH     8 BIT MODE (1) - 16 BIT MODE (0) - (R/W)
           2   MPH       MAP PROTECT SELECT (R/W)
           1   CTSH      MEM ACCESS FROM LSI-11 BUS (0) - (R/W)
                         MEM ACCESS FROM SYSTEM BUS (1) - (R/W)
           0   RSTH      BIT 0 = 1 RESET MEMORY SIMULATOR MODULE (R/W)
```

CONTROL REGISTER 2 (163012)

```
      15:8        THESE BITS ARE NOT AVAILABLE IN THIS CONTROL REGISTER

       7   MSBRKH  MEMORY SIMULATOR BREAK (READ ONLY)
       6   WRENH   MAP PROTECT RAM SIGNAL WRE H (READ ONLY)
       5   ESRH    MAP PROTECT RAM SIGNAL MPIN H (READ ONLY)

       4           SPARE - ALWAYS A 0 ON READ (READ ONLY)

       3   MSEL1H  MEMORY SELECT (R/W)
       2   MSEL0H  MEMORY SELECT (R/W)

               MSEL1    MSEL0
               -----    -----
                 0        0      SELECT SIMULATOR MEMORY - SSM L
                 0        1      SELECT MODULE SELECT MEMORY 0 - SMDS0 L
                 1        0      SELECT MAP PROTECT MEMORY - SMPM L
                 1        1      SELECT MODULE SELECT MEMORY 1 - SMDS1 L

       1   MSAD17H MEMORY SIMULATOR ADDRESS 17 (R/W)
       0   MSAD16H MEMORY SIMULATOR ADDRESS 16 (R/W)
```

CONTROL REGISTER 4 (163014) - MSAD 15:0 REGISTER

```
      15   MSAD15H MEMORY SIMULATOR ADDRESS 15 (R/W)
      14   MSAD14H MEMORY SIMULATOR ADDRESS 14 (R/W)
      13   MSAD13H MEMORY SIMULATOR ADDRESS 13 (R/W)
      12   MSAD12H MEMORY SIMULATOR ADDRESS 12 (R/W)
      11   MSAD11H MEMORY SIMULATOR ADDRESS 11 (R/W)
      10   MSAD10H MEMORY SIMULATOR ADDRESS 10 (R/W)
       9   MSAD9H  MEMORY SIMULATOR ADDRESS 09 (R/W)
       8   MSAD8H  MEMORY SIMULATOR ADDRESS 08 (R/W)
       7   MSAD7H  MEMORY SIMULATOR ADDRESS 07 (R/W)
       6   MSAD6H  MEMORY SIMULATOR ADDRESS 06 (R/W)
       5   MSAD5H  MEMORY SIMULATOR ADDRESS 05 (R/W)
       4   MSAD4H  MEMORY SIMULATOR ADDRESS 04 (R/W)
       3   MSAD3H  MEMORY SIMULATOR ADDRESS 03 (R/W)
       2   MSAD2H  MEMORY SIMULATOR ADDRESS 02 (R/W)
       1   MSAD1H  MEMORY SIMULATOR ADDRESS 01 (R/W)
       0   MSAD0H  MEMORY SIMULATOR ADDRESS 00 (R/W)
```

CONTROL REGISTER 6 (163016)

```
      WHEN THE MAP PROTECTION RAM IS SELECTED VIA CONTROL REGISTER 2,
      THE FOLLOWING BITS ARE LOADED INTO OR READ FROM THE MAP PROTECTION
      RAMS VIA CONTROL REGISTER 6

       3   MUTBH     NOT USED
```

```
2  RDEH      BIT 2 = 1 MEMORY IS READ ENABLED
1  WREH      BIT 1 = 1 MEMORY IS WRITE ENABLED
0  MPINH     BIT 0 = 1 SELECT MEMORY SIMULATOR RAM NOT TARGET RAM
```

WHEN MODULE SELECT RAM 0 OR 1 IS SELECTED VIA CONTROL REGISTER 2,
THE FOLLOWING BITS ARE LOADED INTO OR READ FROM MODULE SELECT RAMS
0 OR 1 VIA CONTROL REGISTER 6.

```
3  EN3H      SELECTS 4TH BANK OF MEMORY SIMULATOR MEMORY
2  EN2H      SELECTS 3RD BANK OF MEMORY SIMULATOR MEMORY
1  EN1H      SELECTS 2ND BANK OF MEMORY SIMULATOR MEMORY
0  EN0H      SELECTS 1ST BANK OF MEMORY SIMULATOR MEMORY
```

WHEN THE MEMORY SIMULATOR RAMS ARE SELECTED VIA CONTROL REGISTER 2,
ALL 16 BITS ARE LOADED INTO AND READ FROM THE SIMULATOR MEMORY RAMS
VIA CONTROL REGISTER 2.

5.2 DEVICE INFORMATION FOR STATE ANALYZER

CONTROL REGISTER 0 (163010) - CDAL REGISTER

```
15  CDAL15    BIT 15 = 1 READ DEVICE TYPE IN BITS 11:8. STATE
              ANALYZER DEVICE TYPE EQUALS 2 (1000)

              BIT 15 = 0 READ DEVICE NUMBER INTO BITS 11:8.

14  CDAL14    ALWAYS A 0 ON READ
13  CDAL13    ALWAYS A 0 ON READ
12  CDAL12    ALWAYS A 0 ON READ

              BITS 11:8 ARE USED TO SELECT THE DEVICE NUMBER OF
              THE STATE ANALYZER.  THESE BITS MUST BE EQUAL TO THE
              SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.

11  CDAL11    DEVICE NUMBER/TYPE
10  CDAL10    DEVICE NUMBER/TYPE
 9  CDAL9     DEVICE NUMBER/TYPE
 8  CDAL8     DEVICE NUMBER/TYPE

 7  CDAL7     1 - DISABLE OUTPUTS OF "OR ADDRESS REG" - ENABLE
                  FOUT 3:0 TO DRIVE "OR" ADDRESS
              0 - ENABLE OUTPUTS OF "OR ADDRESS REG"

 6  CDAL6     1/0 CLOCK THE SIGNAL "TRANST H"

 5  CDAL5     1 - STOP TRACING WHEN "TRAD10 H" SET HIGH
              0 - CONTINUOUS TRACING

 4  CDAL4     1 - ENABLE ALL AND/OR ARRAY RAMS
              0 - ENABLE ONLY ONE AND/OR ARRAY RAM AT A TIME

 3  CDAL3     TRACE RAM BUS SELECT
 2  CDAL2     TRACE RAM BUS SELECT

              CDAL3 CDAL2
              ----- -----
```

```
                    0    0         ENABLE OUTPUTS OF TRACE RAM DATA IN
                                   BUFFER ONTO TRACE RAM BUS
                    0    1         ENABLE TRACE RAM DATA ONTO TRACE RAM BUS
                    1    0         ENABLE SYSTEM BUS AND SBL 59:56 FLIP-
                                   FLOPS ONTO TRACE RAM BUS

        1   CDAL1   1 - ENABLE FUNCTION SELECT FLIP-FLOPS ONTO SYSTEM BUS
                    0 - DISABLE FUNCTION SELECT FLIP-FLOPS FROM SYSTEM BUS

        0   CDAL0   1 - CLEAR TRACE RAM ADDRESS REGISTER, CLEAR TRACING FLIP
                        FLOP, CLEAR SBL 59:56 FLIP-FLOPS, AND RELOAD EVENT
                        COUNTERS FROM EVENT COUNTER REGISTERS.
```

CONTROL REGISTER 2 (163012) - PDAL REGISTER

```
    15:8            BITS 15:8 ARE NOT AVAILABLE FOR THIS REGISTER

     7   PDAL7   1 - CLEAR EVENT COUNTERS
     6   PDAL6   1 - PRESET TRACING FLIP-FLOP
     5   PDAL5   0 - PRESET FUNCTION SELECT FLIP-FLOPS
     4   PDAL4   1 - EXTERNAL PROBE "CLK" SIGNAL WILL LOAD EXTP 7:0
                     FLIP-FLOPS WHEN "CLK" IS SET LOW.
                 0 - EXTERNAL PROBE "CLK" SIGNAL WILL LOAD EXTP 7:0
                     FLIP-FLOPS WHEN "CLK" IS SET HIGH.
     3   PDAL3   SELECT POINTER REGISTER
     2   PDAL2   SELECT POINTER REGISTER
     1   PDAL1   SELECT POINTER REGISTER
     0   PDAL0   SELECT POINTER REGISTER
```

STATE ANALYZER'S POINTER REGISTER AND CONTROL REGISTER 4 (163014)

```
        PDAL BITS 3:0  -  SIGNAL  -  DESCRIPTION

            00          PTER0 L     WRITE/READ AND ARRAY RAM 0
            01          PTER1 L     WRITE/READ AND ARRAY RAM 1
            02          PTER2 L     WRITE/READ AND ARRAY RAM 2
            03          PTER3 L     WRITE/READ AND ARRAY RAM 3
            04          PTER4 L     WRITE/READ AND ARRAY RAM 4
            05          PTER5 L     WRITE/READ AND ARRAY RAM 5
            06          PTER6 L     WRITE/READ AND ARRAY RAM 6
            07          PTER7 L     WRITE/READ AND ARRAY RAM 7
            10          PTER8 L     WRITE/READ AND ARRAY RAM 8
            11          PTER9 L     WRITE/READ AND ARRAY RAM 9
            12          PTER10 L    WRITE/READ AND ARRAY RAM 10
            13          PTER11 L    WRITE/READ AND ARRAY RAM 11
            14          PTER12 L    WRITE/READ AND ARRAY RAM 12
            15          PTER13 L    WRITE/READ AND ARRAY RAM 13
            16          PTER14 L    WRITE/READ AND ARRAY RAM 14
            17          PTER15 L    WRITE/READ OR ARRAY RAM'S
```

STATE ANALYZER'S POINTER REGISTER AND CONTROL REGISTER 6 (163016)

```
        PDAL BITS 3:0 -  SIGNAL  -  DESCRIPTION

            00          PTER0 L     WRITE/READ TRACE RAM (TRAM) ADDRESS REG
            01          PTER1 L     WRITE TRAM 15:0 WITH TRDI DATA FROM
```

```
                                          TRAM BUS SELECTED.
                                          READ TRDI 15:0 DATA FROM TRAM BUS SELECTED
            02           PTER2 L          WRITE TRAM 31:16 WITH TRDI DATA FROM
                                          TRAM BUS SELECTED.
                                          READ TRDI 31:16 DATA FROM TRAM BUS SELECTED
            03           PTER3 L          WRITE TRAM 47:32 WITH TRDI DATA FROM
                                          TRAM BUS SELECTED
                                          READ TRDI 47:32 DATA FROM TRAM BUS SELECTED
            04           PTER4 L          WRITE TRAM 55:48 WITH TRDI DATA FROM
                                          TRAM BUS SELECTED.
                                          READ TRDI 59:48 DATA FROM TRAM BUS SELECTED.
            05           PTER5 L          WRITE TRAM DATA IN BUFFER 15:0 FROM Q-BUS
                                          DATA BITS 15:0
            06           PTER6 L          WRITE TRAM DATA IN BUFFER 31:16 FROM
                                          Q-BUS DATA BITS 15:0.
            07           PTER7 L          WRITE TRAM DATA IN BUFFER 47:32 FROM
                                          Q-BUS DATA IN BITS 15:0.
            10           PTER8 L          WRITE TRAM DATA IN BUFFER 59:48 FROM
                                          Q-BUS DATA IN BITS 15:0
            11           PTER9 L          LOAD EVENT COUNTER REGISTER 0 AND EVENT
                                          COUNTER 0. CLEAR SBL56 FLIP-FLOP.
            12           PTER10 L         LOAD EVENT COUNTER REGISTER 1 AND EVENT
                                          COUNTER 1. CLEAR SBL57 FLIP-FLOP.
            13           PTER11 L         LOAD EVENT COUNTER REGISTER 2 AND EVENT
                                          COUNTER 2. CLEAR SBL58 FLIP-FLOP.
            14           PTER12 L         LOAD EVENT COUNTER REGISTER 3 AND EVENT
                                          COUNTER 3. CLEAR SBL59 FLIP-FLOP.
            15           PTER13 L         NOT USED
            16           PTER14 L         NOT USED
            17           PTER15 L         READ/WRITE "OR ADDRESS REGISTER" (CDAL7=0)
                                          READ FOUT F/F'S ON OR ADDRESS BITS (CDAL7=1)
```

NOTE: THE TRACE RAM (TRAM) BUS SELECTED IS CONTROLLED BY CONTROL
         REGISTER 0 BITS CDAL3 AND CDAL2.

5.3 DEVICE INFORMATION FOR TARGET EMULATOR MODULE

CONTROL REGISTER 0 (163010) - GDAL REGISTER

```
     15  GDAL15   BIT 15 = 1 READ DEVICE TYPE IN BITS 15-8. TARGET
                  EMULATOR DEVICE TYPE EQUALS 0 (0000)

                  BIT 15 = 0 READ DEVICE NUMBER INTO BITS 11:8.

     14  GDAL14   ALWAYS A 0 ON READ
     13  GDAL13   ALWAYS A 0 ON READ
     12  GDAL12   ALWAYS A 0 ON READ

                  BITS 11:8 ARE USED TO SELECT THE DEVICE NUMBER OF
                  THE TARGET EMULATOR. THESE BITS MUST BE EQUAL TO
                  THE SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.

     11  GDAL11   DEVICE NUMBER/TYPE
     10  GDAL10   DEVICE NUMBER/TYPE
      9  GDAL9    DEVICE NUMBER/TYPE
      8  GDAL8    DEVICE NUMBER/TYPE
```

```
            7  GDAL7   SINGLE STEP BREAK INDICATOR (READ ONLY)
            6  GDAL6   TIMEOUT BREAK INDICATOR (READ ONLY)
            5  GDAL5   MEMORY SIMULATOR BREAK INDICATOR (READ ONLY)
            4  GDAL4   STATE ANALYZER BREAK INDICATOR (READ ONLY)
            3  GDAL3   TARGET EMULATOR INTERRUPT ENABLE (R/W)
            2  GDAL2   POINTER FOR EXTENDED REGISTER SELECT (R/W)
            1  GDAL1   POINTER FOR EXTENDED REGISTER SELECT (R/W)
            0  GDAL0   POINTER FOR EXTENDED REGISTER SELECT (R/W)

        EXTENDED REGISTER SELECTED VIA GDAL BITS 2:0

            GDAL2   GDAL1   GDAL0    REGISTER SELECTED VIA R/W TO CONTROL REGISTER 6

              0       0       0      WRITE DIAGNOSTIC ADDRESS REGISTER
                                     READBACK OF ADDRESS BUS
              0       0       1      WRITE NEW FORCE JUMP ADDRESS REGISTER
                                     READBACK OF FORCE JUMP ADDRESS READBACK REG
              0       1       0      WRITE FDAL AND EOAI REGISTER
                                     READBACK OF FDAL/EOAI OR FDAL/CTL REG
              0       1       1      READ/WRITE HDAL REGISTER
              1       0       0      READ/WRITE MODE REGISTER
              1       0       1      READBACK OF TARGET MODE REGISTER
              1       1       0      READBACK OF EIDAL BUS
              1       1       1      READBACK OF EODAL BUS

        CONTROL REGISTER 2 (163012) - ADAL REGISTER

           15  ADAL15  SELECT COLUMN AI FOR STATE ANALYZER (1)
           14  ADAL14  SELECT ROW/COLUMN AI FOR STATE ANALYZER (.)
                       SELECT SERVICE AI FOR STATE ANALYZER (0)
           13  ADAL13  ENABLE SERVICE FROM TARGET EMULATOR (1)
                       ENABLE SERVICE FROM THE TARGET (0)
           12  ADAL12  ENABLE MODE FROM TARGET EMULATOR (1)
                       ENABLE MODE FROM THE TARGET (0)
           11  ADAL11  DISABLE SERVICE TO THE TARGET (1)
                       ENABLE  SERVICE TO THE TARGET (0)
           10  ADAL10  MASTER SWITCH
            9  ADAL9   ENABLE STATE ANALYZER CLOCKS (1)
            8  ADAL8   ENABLE TIMEOUT BREAK (1)
                       DISABLE TIMEOUT BREAK (0)
            7  ADAL7   ENABLE REFRESH TO STATE ANALYZER (1)
                       DISBALE REFRESH TO STATE ANALYZER (0)
            6  ADAL6   SPARE
            5  ADAL5   ENABLE SINGLE STEP BREAK (1)
                       DISABLE SINGLE STEP BREAK (0)
            4  ADAL4   ENABLE PAUSE STATE TO RUN MODE (1)
                       ENABLE PAUSE STATE TO PAUSE MODE (0)
            3  ADAL3   POWER UP FROM TARGET (1)
            2  ADAL2   POWER UP FROM TARGET EMULATOR
            1  ADAL1   SELECT TARGET EMULATOR CRYSTAL CLOCK (1)
                       SELECT CLOCK FROM THE STATE ANALYZER (0)
            0  ADAL0   RESET BREAK LOGIC - ZEROES BREAK LATCH FLIP-FLOP, SINGLE
                       STEP BREAK FLIP-FLOP AND MEMORY SIMULATOR BREAK LATCH
                       FLIP-FLOP
```

CONTROL REGISTER 4 (163014) - VDAL REGISTER

```
15  VDAL15   TNFJ H - TAKE NEW FORCE JUMP ADDRESS F/F (READ)
14  VDAL14   EP8N H - 8 BIT ADDRESS HB F/F (READ)
13  VDAL13   EP8G H - 8 BIT ADDRESS LB F/F (READ)
12  VDAL12   EP8F H - 8 BIT INSTRUCTION HB F/F (READ)
11  VDAL11   EPFN H - 16 BIT ADDRESS F/F (READ)
10  VDAL10   EPSF H - PAUSE STATE SYNC F/F (READ)
 9  VDAL9    PSMW H - PAUSE STATE WORKING F/F (READ)
 8  VDAL8    OUTNEW H - GET NEW ADDRESS F/F (READ)
 7  VDAL7    DIAGNOSTIC FETCT H (READ/WRITE)
 6  VDAL6    MSDI H - DATA IN LOGIC LEVEL (READ)
 5  VDAL5    BTS1 H -
 4  VDAL4    EDEOC H - LOGIC LEVEL OF STATE ANALYZER CLOCK (READ)
 3  VDAL3    READ H - LOGIC LEVEL OF REAT H (READ)
 2  VDAL2    DIAGNOSTIC RESET OF THE TARGET EMULATOR MODULE AND
             CLOCKS THE TAI AND TDAL LATCHES (READ/WRITE)
 1  VDAL1    SPARE (READ/WRITE)
 0  VDAL0    ENABLE TAI AND TDAL READBACK FROM POD (READ/WRITE)
```

CONTROL REGISTER 6 (163016) - FDAL REIGSTER (EOAI/CTL ON FDAL 15:8)

```
 7  FDAL7    INTERRUPT VECTOR
 6  FDAL6    INTERRUPT VECTOR
 5  FDAL5    INTERRUPT VECTOR
 4  FDAL4    INTERRUPT VECTOR
 3  FDAL3    INTERRUPT VECTOR
 2  FDAL2    INTERRUPT VECTOR
 1  FDAL1    SPARE
 0  FDAL0    SELECT EOAI REG TO BE READBACK ON FDAL BITS 15:8 (1)
             SELECT CTL  REG TO BE READBACK ON FDAL BITS 15:8 (0)
```

CONTROL REGISTER 6 (163016) - HDAL REGISTER - DIAGNOSTIC CONTROL BITS

```
15  HDAL15   DIAGNOSTIC CONTROL OF PPI L WHEN HDAL2 EQUALS A ONE
14  HDAL14   DIAGNOSTIC CONTROL OF EIDAL17 H WHEN HDAL2 EQUALS A ONE
13  HDAL13   DIAGNOSTIC CONTROL OF PCAS H WHEN HDAL2 EQUALS A ONE
12  HDAL12   DIAGNOSTIC CONTROL OF PRAS H WHEN HDAL2 EQUALS A ONE
11  HDAL11   DIAGNOSTIC CONTROL OF EIDAL16 H WHEN HDAL2 EQUALS A ONE
10  HDAL10   SPARE
 9  HDAL9    ENABLE DIAGNOSTIC ADDRESS REGISTER TO ADDRESS BUS
 8  HDAL8    DIAGNOSTIC CONTROL OF CREADY L WHEN HDAL2 EQUALS A ONE
 7  HDAL7    DIAGNOSTIC CONTROL OF PBCLR H WHEN HDAL2 EQUALS A ONE
 6  HDAL6    DIAGNOSTIC CONTROL OF PSEL1 L WHEN HDAL2 EQUALS A ONE
 5  HDAL5    DIAGNOSTIC CONTROL OF PSEL0 L WHEN HDAL2 EQUALS A ONE
 4  HDAL4    DIAGNOSTIC CONTROL OF PR/WHB L WHEN HDAL2 EQUALS A ONE
 3  HDAL3    DIAGNOSTIC CONTROL OF PR/WLB L WHEN HDAL2 EQUALS A ONE
 2  HDAL2    ENABLES PROGRAM TO GENERATE T-11 SIGNALS LISTED IN HDAL (1)
             ENABLES T-11 TO GENERATE T-11 SIGNALS LISTED IN HDAL (0)
 1  HDAL1    SPARE
 0  HDAL0    DIAGNOSTIC CONTROL OF MSDI H WHEN HDAL2 EQUALS A ONE
```

CONTROL REGISTER 6 (163016) - MODE REGISTER

```
15  MR15     T-11 START/RESTART ADDRESS SELECT
14  MR14     T-11 START/RESTART ADDRESS SELECT
```

```
        13  MR13      T-11 START/RESTART ADDRESS SELECT
        12  MR12      T-11 USER MODE (1)
                      T-11 TESTER MODE (0)
        11  MR11      SELECT 8 BIT BUS (1)
                      SELECT 16 BIT BUS (0)
        10  MR10      T-11 DYNAMIC MODE ONLY - SELECTS 4K/16K (1)
                      T-11 DYNAMIC MODE ONLY - SELECTS 64K (0)
         9  MR9       T-11 STATIC MEMORY SELECT (1)
                      T-11 DYNAMIC MEMORY SELECT (0)
         8  MR8       T-11 DELAYED READ/WRITE SELECT (1)
                      T-11 NROMAL READ/WRITE SELECT (0)
         7  MR7       NOT DEFINED
         6  MR6       NOT DEFINED
         5  MR5       NOT DEFINED
         4  MR4       NOT DEFINED
         3  MR3       NOT DEFINED
         2  MR2       NOT DEFINED
         1  MR1       T-11 STANDARD MICROCYCLE (1)
                      T-11 LONG MICROCYCLE (0)
         0  MR0       T-11 PROCESSOR CLOCK (1)
                      T-11 CONSTANT CLOCK (0)
```

6.0 TEST SUMMARIES

TEST 1:

THIS TEST WILL BE EXECUTED AS THE FIRST TEST IN THE PROGRAM AND AT THE
BEGINNING OF EACH TEST IN THE PROGRAM. THE PURPOSE OF THIS TEST IS TO
INITIALIZE THE MDE/T-11 MODULES (MEMORY SIMULATOR, STATE ANALYZER AND TARGET
EMULATOR) TO A KNOWN STATE. THE TEST SEQUENCE IS DESCRIBED BELOW.

MDE/T-11 MEMORY SIMULATOR MODULE INITIALIZATION SEQUENCE:
1.   LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVICE NUMBER TO
        SELECT THE MEMORY SIMULATOR MODULE.
2.   LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
        AND THE BIT TO SET THE SIGNAL 'RST H' TO THE HIGH STATE. WHEN
        THE SIGNAL 'RST H' IS SET HIGH, THE 'RDV' AND 'WRV' FLIP-FLOPS
        WILL BE PRESET TO A ONE THUS CAUSING THE SIGNALS 'RDV H' AND
        'WRV H' TO BE ASSERTED LOW. THE SIGNALS 'RDV H' AND 'WRV H'
        SHOULD BE READ AS ZEROES WHEN CONTROL REGISTER 0 IS READ.
3.   LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
        AND BIT 15 SET TO A ONE. THE BIT WHICH SET THE SIGNAL 'RST H'
        TO THE HIGH STATE WILL BE CLEARED THUS SETTING THE SIGNAL LOW.
        WHEN BIT 15 IS SET TO A ONE, THE DEVICE TYPE WILL BE READ BACK
        ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE
        NUMBER.
4.   CLEAR BIT 15 IN CONTROL REGISTER 0 AND THEN READ AND CHECK
        CONTROL REGISTER 0 FOR THE DEVICE NUMBER.
5.   LOAD, READ AND CHECK CONTROL REGISTER 2'S READ/WRITE BITS 3:0
        WITH A DATA PATTERN OF ZEROES. THESE BITS WILL SET THE SIGNALS
        MSEL1 H, MSEL0 H, MSAD17 H, AND MSAD16 H TO THE LOW STATE. THE
        READ ONLY SIGNALS MSBRK H, WREN H, AND ESR H WILL BE IGNORED AT
        THIS POINT IN TIME.
6.   LOAD, READ AND CHECK CONTROL REGISTER 4'S READ/WRITE BITS 15:0
        WITH A DATA PATTERN OF ALL ZEROES. THESE BITS WILL SET THE
        SIGNALS MSAD 15:0 H TO THE LOW STATE.

MDE/T-11 STATE ANALYZER MODULE INITIALIZATION

1.   LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVIE NUMBER TO
       SELECT THE STATE ANALYZER MODULE.
2.   LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
       AND THE BIT TO SET THE SIGNAL "CDAL0 H" TO THE HIGH STATE.
       WHEN THE SIGNAL "CDAL0 H" IS SET HIGH, THE TRACE RAM ADDRESS
       REGISTER, THE TRACING AND SBL FLIP-FLOPS WILL BE CLEARED AND
       THE EVENT COUNTERS WILL BE LOADED WITH DATA FROM THE EVENT
       COUNTER REGISTERS.
3.   LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
       AND THE BIT TO SET THE SIGNAL CDAL15 H TO A ONE. THE BIT WHICH
       SET "CDAL0 H" TO THE HIGH STATE WILL BE CLEARED THUS SETTING THE
       SIGNAL "CDAL0 H" TO THE LOW STATE. WHEN "CDAL15 H" IS SET TO A
       ONE, THE DEVICE TYPE WILL BE READ ON A READ COMMAND TO CONTROL
       REGISTER 0 INSTEAD OF THE DEVICE NUMBER.
4.   CLEAR THE BIT WHICH SET "CDAL15 H" TO THE HIGH STATE AND THEN
       READ AND CHECK CONTROL REGISTER 0 FOR THE DEVICE NUMBER.
5.   LOAD, READ AND CHECK CONTROL REGISTER 4'S PDAL REGISTER WITH
       A DATA PATTERN OF ALL ZEROES. THIS WILL CAUSE THE SIGNALS
       "PDAL 7:0 H" TO BE ASSERTED LOW. THIS WILL ALSO CAUSE THE
       SIGNAL PTER0 L TO BE ASSERTED LOW IN THE POINTER REGISTER.

MDE/T-11 TARGET EMULATOR MODULE INITIALIZATION

1.   LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVICE NUMBER TO
       SELECT THE TARGET EMULATOR MODULE.
2.   LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
       AND ALL READ/WRITE BITS SET TO A ZERO. THE READ ONLY SIGNALS
       SSBRK H, TOBRK H, AND MEMBRK H WILL BE IGNORED DURING THE
       READING OF CONTROL REGISTER 0.
3.   LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
       AND THE BIT TO SET THE SIGNAL "GDAL15 H" TO THE HIGH STATE.
       WHEN THE SIGNAL "GDAL15 H" IS SET HIGH (1), THE DEVICE TYPE WILL
       BE READ ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE
       DEVICE NUMBER.
4.   SET THE SIGNAL "GDAL15 H" TO THE LOW STATE BY CLEARING THE BIT
       IN CONTROL REGISTER 0. ALSO SET THE READ/WRITE BITS "GDAL1 H"
       AND "GDAL0 H" TO A ONE. ALL OTHER READ/WRITE BITS WILL BE
       LOADED WITH ZEROES. WHEN "GDAL2 H" IS SET TO A ZERO AND THE
       SIGNALS "GDAL1 H" AND "GDAL0 H" ARE SET TO ONES, THE HDAL
       REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
       CONTROL REGISTER 6.
5.   LOAD, READ AND CHECK HDAL REGISTER WITH A DATA PATTERN OF 4
       WHICH WILL CAUSE THE SIGNAL "HDAL2 H" TO BE ASSERTED HIGH (1)
       AND ALL OTHER HDAL BITS TO BE ASSERTED LOW (0). WHEN "HDAL2 H"
       IS ASSERTED HIGH, THE PROGRAM CAN GENERATE THE T-11 TIMING AND
       CONTROL SIGNALS.
6.   LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
       AND WITH "GDAL2 H" SET TO A ONE AND GDAL BITS 1 AND 0 SET TO A
       ZERO. THIS WILL CAUSE THE MODE REGISTER TO BE SELECTED ON A
       WRITE OR READ COMMAND TO CONTROL REGISTER 6.
7.   LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF
       ALL ZEORES. MODE REGISTER BIT MR11 H ON A ZERO WILL SELECT 16
       BIT ADDRESS MODE.

8.   LOAD, READ AND CHECK CONTROL REGISTER 2'S ADAL REGISTER WITH
       ADALO H SET TO A ONE AND THEN A ZERO. SETTING AND CLEARING THE
       SIGNAL ADALO H WILL CAUSE A PULSE TO BE ISSUED ON THE SIGNAL
       'BRKRES L'. ALL OTHER ADAL REGISTER BITS WILL BE LOADED AND
       CHECKED WITH ZEORES. PULSING THE SIGNAL 'BRKRES L' WILL CLEAR
       THE SINGLE STEP SYNC FLIP-FLOP, THE BREAK INTERRUPT LATCH FLIP-
       FLOP, THE MEMORY SIMULATOR BREAK LATCH FLIP-FLOP (MEMBRK) AND
       THE TIMEOUT BREAK ONE SHOT WILL BE RESET.
9.   READ AND CHECK CONTROL REGISTER 0 TO CHECK THAT ALL THE BREAK
       SIGNALS ARE READ AS ZEROES. THESE SIGNALS ARE SSBRK H, TOBRK H,
       MEMBRK H AND EDBRK H.
10.   LOAD, READ AND CHECK CONTROL REGISTER 4'S VDAL REGISTER WITH
       VDAL2 H SET TO A ONE AND THEN A ZERO. ALL OTHER VDAL REGISTER
       READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES. SETTING
       AND CLEARING THE SIGNAL VDAL2 H WILL CAUSE A PULSE TO BE ISSUED
       ON THE SIGNAL INVD L. A PULSE ON THE SIGNAL INVD L WILL CAUSE
       ALL THE FLIP-FLOP'S AND SOME REGISTERS NOT CLEARED BY THE SIGNAL
       'BRKRES L' PREVIOULSY TO BE INITIALIZED TO SOME PREDEFINED
       STATE. THE READ ONLY BITS WILL BE CHECKED TO BE ZERO AS A
       RESULT OF THE SIGNAL 'INVD L' BEING PULSED.

TEST 2:

THIS TEST WILL CHECK THAT THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS
REGISTER AND ADDRESS BITS 17:16 CAN BE ENABLED TO THE SYSTEM ADDRESS
BUS AND THAT THE ADDRESS BUS BITS 17:0 CAN BE CLOCKED INTO THE MEMORY
SIMULATOR AND STATE ANALYZER SYSTEM BUS LATCHES FOR THESE BITS DURING
A NORMAL T-11 TIMING CYCLE. A NORMAL T-11 TIMING CYCLE OCCURS WHEN
RAS, CAS AND PI ARE SET TO THEIR ASSERTED STATE IN THE ORDER LISTED AND
THEN DEASSERTED IN THE FOLLOWING ORDER: CAS, PI AND RAS. THE ADDRESS
BUS DATA PATTERNS USED DURING THIS TEST ARE AS FOLLOWS: 577777, 252525,
725252 AND 000000. TARGET EMULATOR HDAL REGISTER BITS 14 AND 11 CONTROL
THE STATE OF ADDRESS BITS 17 AND 16.

WHEN PRAS H IS SET HIGH, THE SIGNAL 'ADVAL H' WILL BE SET HIGH THUS
CLOCKING SYSTEM ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR SYSTEM
ADDRESS BUS LATCHES. WHEN XRAS H IS SET HIGH, THE SIGNALS 'EDCK0 H' AND
'EDCK1 H' WILL BE SET HIGH THUS CLOCKING SYSTEM ADDRESS BUS BITS 15:0
INTO THE STATE ANALYZERS SYSTEM ADDRESS BUS LATCHES FOR THESE BITS.
WHEN XPI L IS SET LOW, THE SIGNAL 'EDCK4 H' WILL BE SET HIGH THUS
CLOCKING THE SYSTEM BUS SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H
AND OBTS BITS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE
BITS. ALL THE SIGNALS MENTIONED ABOVE ARE GENERATED ON THE TARGET
EMULATOR MODULE. THE PROGRAM WILL CHECK THAT SYSTEM ADDRESS BUS BITS
17:0 WERE CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES
BY ENABLING THE LATCHES TO MSAD BITS 17:0 VIA THE SIGNAL 'CTS L' AND
THEN READING AND CHECKING THESE BITS VIA CONTROL REGISTER 2 AND 4. THE
PROGRAM WILL CHECK THAT SYSTEM ADDRESS BUS BITS 17:0 AND THE SIGNALS
XSEL1 H, EDSEL0 H, AND OBTS BITS 3:0 WERE CLOCKED INTO THE STATE
ANALYZER SYSTEM BUS LATCHES FOR THESE BITS. THE STATE ANALYZERS SYSTEM
BUS LATCHES ARE ENABLED TO STATE ANALYZERS TRDI BUS BY SETTING THE
SIGNAL 'TRSL2 L' TO THE LOW STATE. THE PROGRAM WILL THEN READ AND CHECK
TRDI BUS BITS 15:0 AND 39:32 FOR THE SYSTEM BUS DATA.

TEST 3:

THIS TEST WILL CHECK THAT DATA, WRITTEN INTO LOCATIONS OF THE MEMORY
SIMULATOR RAM, CAN BE ENABLED TO THE TARGET EMULATOR MODULE AND CLOCKED
INTO THE STATE ANALYZER MODULE VIA THE SYSTEM DATA BUS WHEN A 'READ''
OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE IN 16 BIT
MODE.   ADDRESSES 0, 20000, 40000 AND 60000, WHICH ARE THE FIRST LOCA-
TIONS OF EACH 4K BANK OF MEMORY SIMULATOR RAM, WILL BE WRITTEN WITH A
DATA PATTERN OF 125252, 052525, 177777, AND 000000 RESPECTIVELY.
LOCATIONS OF THE MEMORY SIMULATOR RAM WILL BE ADDRESSED VIA THE DIAGNOS-
TIC ADDRESS REGISTER ON THE TARGET EMULATOR MODULE DURING A NORMAL T-11
TIMING CYCLE.   A NORMAL T-11 TIMING CYCLE OCCURS WHEN RAS, CAS AND PI
ARE ASSERTED IN THE ORDER LISTED AND THEN DE-ASSERTED IN THE FOLLOWING
ORDER CAS, PI AND RAS.   THE PROGRAM WILL CHECK THAT THE SYSTEM ADDRESS
BUS WAS CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES AND
THE STATE ANALYZERS SYSTEM BUS LATCHES WHEN THE SIGNALS XRAS H AND
PRAS H ARE ASSERTED HIGH ON THE TARGET EMULATOR MODULE.   WHEN THE
TARGET EMULATOR SIGNALS XR/WLB H, XR/WHB H, XRAS H, AND XCAS H ARE
ASSERTED HIGH, THE TARGET EMULATOR SIGNALS 'READ H'' AND 'MSDI H'' WILL
BE ASSERTED HIGH.   THE SIGNAL 'READ H'' BEING ASSERTED WILL ENABLE
MEMORY SIMULATOR RAM DATA ADDRESSED BY THE TARGET EMULATOR MODULE ONTO
THE SYSTEM DATA BUS.   THE SYSTEM DATA BUS WILL BE ENABLED TO THE TARGET
EMULATOR'S EODAL BUS VIA THE SIGNAL 'MSDI H'' AND THE EODAL BUS WILL BE
ENABLED TO THE TARGET EMULATOR'S EIDAL BUS VIA THE SIGNALS COHB L AND
COLB L.   THE SIGNALS COHB L AND COLB L ARE ASSERTED LOW AS A RESULT OF
THE SIGNALS ETR L, PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L BEING
ASSERTED HIGH.   THE PROGRAM WILL READ AND CHECK THE TARGET EMULATOR'S
EODAL AND EIDAL BUS TO CONTAIN THE EXPECTED MEMORY SIMULATOR RAM DATA.
WHEN THE SIGNAL XCAS L IS RETURNED TO ITS DE-ASSERTED STATE, THE SIGNALS
'EDCK2 H'' AND 'EDCK3 H'' WILL GO FROM A LOW TO A HIGH STATE THUS CLOCKING
THE SYSTEM DATA BUS INTO THE STATE ANALYZER SYSTEM DATA BUS LATCHES.
THE PROGRAM WILL CHECK THAT THE SYSTEM DATA BUS WAS CLOCKED INTO THE
STATE ANALYZER'S SYSTEM DATA BUS LATCHES BY ENABLING THE LATCHES TO THE
STATE ANALYZER'S TRDI BUS VIA THE SIGNAL TRSL2 L AND THEN READING TRDI
BUS BITS 31:16 TO CONTAIN THE EXPECTED MEMORY SIMULATOR RAM DATA.   THE
PROGRAM WILL ALSO CHECK THAT THE STATE ANALYZER'S TRACE RAM ADDRESS
REGISTER WAS INCREMENTED BY ONE VIA THE SIGNAL 'CTR L'' WHEN THE TARGET
EMULATOR SIGNAL 'EDEOC H'' WAS SET HIGH.

TEST 4:

THIS TEST WILL CHECK THAT DATA WRITTEN INTO ADDRESS 0 AND 2 OF THE
MEMORY SIMULATOR RAM CAN BE ENABLED TO THE TARGET EMULATOR MODULE VIA
THE LOW BYTE OF THE SYSTEM DATA BUS WHEN A 'READ'' OPERATION IS BEING
EXECUTED FROM THE TARGET EMULATOR MODULE IN 8 BIT MODE.   THE TARGET
EMULATOR MODULE WILL BE SETUP TO 8 BIT MODE AND THE MEMORY SIMULATOR
MODULE WILL BE SETUP TO 8 BIT MODE AFTER THE DATA HAS BEEN WRITTEN INTO
THE MEMORY SIMULATOR RAM AND CHECKED.   ADDRESS 0 AND 2 OF THE MEMORY
SIMULATOR RAM WILL BE WRITTEN WITH A DATA PATTERN OF 125125 AND 052652
RESPECTIVELY.   ADDRESSES 0, 1, 2 AND 3 OF THE MEMORY SIMULATOR RAM WILL
BE ADDRESSED VIA THE TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER WHEN
A NORMAL T-11 TIMING CYCLE OCCURS.   A NORMAL T-11 TIMING CYCLE OCCURS
WHEN RAS, CAS AND PI ARE ASSERTED IN THE ORDER GIVEN AND THEN DE-ASSERTED
IN THE FOLLOWING ORDER CAS, PI AND THEN RAS.   THE PROGRAM WILL CHECK
THAT THE SYSTEM ADDRESS BUS WAS CLOCKED INTO THE MEMORY SIMULATORS
SYSTEM ADDRESS BUS LATCHES WHEN THE SIGNAL PRAS H WAS ASSERTED HIGH ON
THE TARGET EMULATOR MODULE.   WHEN THE TARGET EMULATOR SIGNALS XR/WLB H,
XRAS H, XCAS H AND MR11 H ARE ASSERTED HIGH, THE TARGET EMULATOR SIGNALS

''READ H'' AND ''MSDI H'' WILL BE ASSERTED HIGH. THE SIGNAL ''READ H'' BEING
ASSERTED WILL ENABLE THE LOW BYTE OF MEMORY SIMULATOR RAM DATA TO THE
LOW BYTE OF THE SYSTEM DATA BUS IF THE ADDRESS WAS EVEN, OR THE HIGH
BYTE OF THE MEMORY SIMULATOR RAM DATA WILL BE ENEBALED TO THE LOW BYTE
OF THE SYSTEM DATA BUS IF THE ADDRESS WAS ODD. THE DATA ENABLED TO
THE LOW BYTE OF THE SYSTEM DATA BUS WILL BE 125, 252, 252 AND 125 FOR
ADDRESSES 0, 1, 2 AND 3 RESPECTIVELY. THE SYSTEM DATA BUS WILL BE
ENABLED TO THE LOW BYTE OF THE TARGET EMULATOR'S EODAL BUS VIA THE
SIGNAL ''MSDI H'' AND THE LOW BYTE OF THE EODAL BUS WILL BE ENABLED TO
THE LOW BYTE OF THE TARGET EMULATOR'S EIDAL BUS VIA THE SIGNAL ''COLB L''.
THE SIGNAL ''COLB L'' WILL BE ASSERTED LOW AS A RESULT OF THE SIGNALS
ETR L, PR/WLB H, PPI H AND DMG L BEING ASSERTED HIGH. THE PROGRAM WILL
READ AND CHECK THE TARGET EMULATORS EODAL AND EIDAL BUSES TO CONTAIN THE
EXPECTED BYTE OF MEMORY SIMULATOR RAM DATA.

TEST 5:

THIS TEST WILL CHECK THAT DATA FROM THE MEMORY SIMULATOR RAM CAN BE
ENABLED TO THE TARGET EMULATOR'S TDAL BUS AND CLOCKED INTO THE TDAL
DIAGNOSTIC LATCHES WHEN A ''READ'' OPERATION IS BEING EXECUTED FROM THE
TARGET EMULATOR MODULE. THE TEST WILL CHECK THAT THE TDAL DIAGNOSTIC
LATCHES CAN BE ENABLED TO THE SYSTEM DATA BUS AND THAT THE SYSTEM DATA
BUS CAN BE WRITTEN BACK INTO THE MEMORY SIMULATOR RAM LOCATION WHEN A
''WRITE'' OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE.
THE TEST WILL INITIALLY LOAD AND CHECK MEMORY SIMULATOR RAM LOCATIONS
000000, 020000, 040000 AND 060000 WITH DATA PATTERNS 125252, 146314,
000377 AND 000000 RESPECTIVELY. ONCE EACH LOCATION HAS BEEN WRITTEN AND
CHECKED, THE PROGRAM WILL ISSUE A ''READ'' OPERATION FROM THE TARGET
EMULATOR MODULE TO ONE OF THE MEMORY SIMULATOR RAM LOCATIONS AND CHECK
THAT THE DATA IS PRESENT ON THE TARGET EMULATOR'S EODAL AND EIDAL BUSES.
MEMORY SIMULATOR RAM DATA WILL ALSO BE ENABLED TO THE TARGET EMULATOR'S
TDAL BUS. TO CAPTURE THIS DATA, THE PROGRAM MUST SET AND CLEAR THE
SIGNAL ''VDAL2 H'' TO CLOCK THE TDAL BUS DATA INTO THE TDAL DIAGNOSTIC
LATCHES. ONCE MEMORY SIMULATOR RAM DATA HAS BEEN CLOCKED INTO THE TDAL
DIAGNOSTIC LATCHES, THE PROGRAM WILL WRITE THE ONE'S COMPLEMENT OF THE
INITIAL MEMORY SIMULATOR RAM DATA BACK INTO THE LOCATION ADDRESSED AND
THEN CHECK THAT THE LOCATION CONTAINS THE ONE'S COMPLEMENT OF THE
INITIAL DATA. THE PROGRAM WILL NOW ENABLE THE TDAL DIAGNOSTIC LATCHES,
WHICH CONTAINS THE INITIAL MEMORY SIMULATOR RAM DATA, TO THE SYSTEM DATA
BUS AND THEN WRITE THIS DATA VIA A ''WRITE'' OPERATION FROM THE TARGET
EMULATOR MODULE BACK INTO THE MEMORY SIMULATOR RAM LOCATION INITIALLY
READ. THE PROGRAM WILL NOW READ AND CHECK THE MEMORY SIMULATOR RAM
LOCATION TO CONTAIN THE INITIAL DATA.

TEST 6:

THIS TEST WILL READ DATA FROM THE MEMORY SIMULATOR RAM IN 16 BIT MODE
AND STORE THE DATA READ IN THE TARGET EMULATOR'S TDAL DIAGNOSTIC LATCHES.
ONCE THE DATA HAS BEEN STORED IN THE TDAL DIAGNOSTIC LATCHES, THE PROGRAM
WILL CHANGE THE DATA STORED IN THE MEMORY SIMULATOR RAM LOCATION TO ALL
ZEROES. THE PROGRAM WILL NOW SET THE MEMORY SIMULATOR MODULE TO 8 BIT
MODE; LOAD THE EVEN ADDRESS OF THE MEMORY SIMULATOR RAM LOCATION INTO
THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER; ENABLE THE TDAL DIAG-
NOSTIC LATCHES TO THE SYSTEM DATA BUS; AND THEN PERFORM A NORMAL T-11
TIMING CYCLE BY PULSING THE SIGNALS RAS, CAS AND PI. THE ABOVE OPERATION
WILL CAUSE THE LOW BYTE OF THE SYSTEM BUS DATA TO BE WRITTEN INTO THE LOW

BYTE OF THE MEMORY SIMULATOR RAM LOCATION. THE PROGRAM WILL CHECK THAT
THE CORRECT ADDRESS WAS CLOCKED INTO THE MEMORY SIMULATOR'S SYSTEM BUS
ADDRESS LATCHES AND THAT THE LOW BYTE OF THE INITIAL DATA WAS WRITTEN
INTO THE MEMORY SIMULATOR RAM LOCATION. THE HIGH BYTE OF THE LOCATION
SHOULD REMAIN ALL ZEROES DURING THIS WRITE OPERATION. THE PROGRAM WILL
NOW RESET THE MEMORY SIMULATOR MODULE TO 8 BIT MODE; LOAD THE ODD ADDRESS
OF THE MEMORY SIMULATOR LOCATION INTO THE TARGET EMULATOR'S DIAGNOSTIC
ADDRESS REGISTER; AND THEN PERFORM A NORMAL T-11 TIMING CYCLE. THE
ABOVE OPERATION WILL CAUSE THE LOW BYTE OF THE SYSTEM BUS DATA, WHICH
CONTAINS THE DATA OF THE LOW BYTE OF THE TDAL DIAGNOSTIC LATCH, TO BE
WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM LOCATION. THE
PROGRAM WILL CHECK THAT THE CORRECT ADDRESS WAS CLOCKED INTO THE MEMORY
SIMULATOR SYSTEM ADDRESS BUS LATCHES AND THAT THE LOW BYTE OF THE INITIAL
DATA WAS WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM LOCATION.
THE LOW BYTE OF THE LOCATION SHOULD REMAIN UNCHANGED DURING THIS WRITE
OPERATION. THE ABOVE SEQUENCE WILL BE PERFORMED FOR ADDRESSES 0, 20000,
40000 AND 60000. THESE ADDRESSES ARE THE FIRST ADDRESSES OF EACH 4K BANK
OF MEMORY SIMULATOR RAM. THE DATA LOADED INTO THE ADDRESSES ARE 052652,
146063, 000377 AND 125125 RESPECTIVELY. AFTER THE DATA HAS BEEN WRITTEN
BACK INTO THE MEMORY SIMULATOR RAM IN 8 BIT MODE, THE DATA IN THESE
ADDRESSES SHOULD BE 125252, 031463, 177777, AND 052525 RESPECTIVELY. THE
LAST PORTION OF THIS TEST WILL READ AND CHECK EACH ADDRESS TO CONTAIN
THE CORRECT DATA. THIS IS DONE TO CHECK THE RAM WRITE AND SELECT LOGIC.

TEST 7:

THIS TEST WILL CHECK THAT TARGET EMULATOR SIGNALS XSEL1 H, EDSELO H,
ADDR17 H, ADDR16 H, BTS3 H, BTS2 H, BTS1 H AND BTSO H CAN BE ENABLED
TO THE SYSTEM BUS AS SIGNALS CTL 11:8 H AND OBTS 3:0 H RESPECTIVELY,
AND THAT THESE SIGNALS CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM
BUS LATCHES FOR THESE BITS VIA THE TARGET EMULATOR'S SYSTEM BUS CLOCKING
SIGNAL "ENCK4 H". THE PROGRAM WILL CHECK THAT THESE BITS ARE CLOCKED
INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES BY READING THESE LATCHES
ON THE STATE ANALYZERS TRDI BUS BITS 39:32. THE TARGET EMULATOR SIGNALS
"ADDR17 H" AND "ADDR16 H" HAVE BEEN CHECKED IN PREVIOUS TEST. THEREFORE,
THESE SIGNALS WILL ONLY BE CHECKED FOR ZEROES IN THIS TEST. THE PROGRAM
WILL SET THE SIGNALS XSEL1 H, EDSELO H AND BTS BITS 3:0 H TO ONES AND
ZEROES BY MANIPULATING THE ASSOCIATED LOGIC. THE TEST WILL THEN CLOCK
THE CORRESPONDING SYSTEM BUS SIGNALS INTO THE STATE ANALYZER SYSTEM BUS
LATCHES AND CHECK THAT THE SYSTEM BUS LATCHES CONTAIN THE CORRECT DATA
PATTERN. THE PROGRAM WILL ALSO CHECK THAT THE TARGET EMULATOR SYSTEM
BUS CLOCKING SIGNAL "ENCK4 H" CAN BE GENERATED IN DIFFERENT WAYS.

TEST 8:

THIS TEST WILL CHECK THAT DATA LOADED INTO THE TARGET EMULATOR'S EOAI
REGISTER CAN BE ENABLED TO THE CTL BUS, WHICH IS ON THE SYSTEM BUS,
AND THAT THE CTL BUS CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM
BUS CTL 7:0 LATCHES VIA THE TARGET EMULATOR'S CLOCKING SIGNAL "ENCK5 H".
THE TEST WILL ALSO CHECK THAT THE EOAI REGISTER CAN BE CLOCKED INTO
THE TARGET EMULATOR'S CTL REGISTER WHEN THE SIGNAL "XCAS L" IS RETURNED
TO THE DE-ASSERTED STATE AFTER HAVING BEEN ASSERTED. TO CHECK THAT THE
EOAI REGISTER WAS CLOCKED INTO THE CTL REGISTER, THE PROGRAM WILL READ
THE TARGET EMULATOR'S CTL REGISTER AND CHECK THE DATA TO BE THE ONE'S
COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER. THE SYSTEM BUS
CLOCKING SIGNAL "ENCK5 H" IS GENERATED ON THE TARGET EMULATOR MODULE AS

THE SIGNAL "CKAI H". THE PROGRAM WILL CAUSE THE SIGNAL "CKAI H" TO BE
PULSED IN DIFFERENT WAYS DURING THIS TEST. TO CHECK THAT THE EOAI
REGISTER DATA CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS CTL
LATCHES AND THAT A PULSE CAN BE GENERATED ON THE SIGNAL "ENCK5 H", THE
PROGRAM WILL READ THE CTL 7:0 SYSTEM BUS LATCHES ON THE STATE ANALYZER'S
TRDI BUS BITS 47:40 AND CHECK THAT THE DATA READ IS THE ONE'S COMPLEMENT
OF THE DATA LOADED INTO THE TARGET EMULATOR'S EOAI REGISTER. THE TEST
WILL ALSO CHECK THAT THE TARGET EMULATOR SIGNALS XSEL1 H, EDSEL0 H,
ADDR17 H, ADDR16 H AND BTS BITS 3:0 H CAN BE CLOCKED INTO THE STATE
ANALYZER'S SYSTEM BUS LATCHES BY READING THESE BITS ON STATE ANALYZER'S
TRDI BUS BITS 39:32. THE TEST WILL LOAD THE EOAI REGISTER WITH THE
FOLLOWING DATA PATTERNS 377, 000, 252, 125 AND 314.

TEST 9:

THIS TEST WILL CHECK THAT THE MEMORY SIMULATOR "RDV" FLIP-FLOP CAN BE
CLEARED WHEN A READ OPERATION IS EXECUTED FROM THE TARGET EMULATOR
MODULE TO AN ADDRESS WHICH IS MAPPED IN THE MEMROY SIMULATOR'S MAP
PROTECTION RAM TO INHIBIT READS AND WRITES. THE "RDV" FLIP-FLOP WILL
BE CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL "RDE H" BEING ASSERTED
LOW AND A PULSE ON THE SIGNAL "RDS H". THE SIGNAL "RDS H" WILL BE
PULSED WHEN THE MEMORY SIMULATOR SIGNAL "CTS H" IS ASSERTED HIGH AND
A PULSE IS ISSUED ON THE TARGET EMULATOR SIGNAL "READ H". A PULSE
WILL OCCUR ON THE SIGNAL "READ H" WHEN A T-11 READ OPERATION IS BEING
EXECUTED BY THE TARGET EMULATOR MODULE. THE PROGRAM WILL CHECK THAT THE
MEMORY SIMULATOR SIGNAL "MSBRK H" IS ASSERTED HIGH AS A RESULT OF THE
"RDV" FLIP-FLOP BEING CLEARED. THE PROGRAM WILL CHECK THE TARGET
EMULATOR MODULES "MEMBRK" FLIP-FLOP TO BE CLEARED AND THEN CAUSE A
PULSE TO BE ISSUED ON TARGET EMULATOR SIGNAL "XRAS H". THE PROGRAM WILL
NOW CHECK THE "MEMBRK" FLIP-FLOP TO BE SET TO A ONE AS A RESULT OF A
PULSE ON "XRAS H" AND THE MEMORY SIMULATOR'S SYSTEM BUS SIGNAL "MSBRK H"
BEING ASSERTED HIGH. THE PROGRAM WILL NOW PRESET THE "RDV" FLIP-FLOP
BY PULSING MEMORY SIMULATOR SIGNAL "RST H". THE PROGRAM WILL CHECK THAT
THE "RDV" FLIP-FLOP PRESET AND THAT THE SIGNAL "MSBRK H" WENT TO THE LOW
STATE AS A RESULT OF THE "RDV" FLIP-FLOP BEING PRESET. THE PROGRAM WILL
NOW PULSE THE TARGET EMULATOR SIGNAL "XRAS H" AGAIN AND CHECK THAT THE
"MEMBRK" FLIP-FLOP IS STILL SET TO A ONE AS A RESULT OF THE FLIP-FLOP
BEING LATCHED ONCE IT HAS BEEN SET. THE PROGRAM WILL NOW PULSE TARGET
EMULATOR SIGNAL "BRKRES L" AND CHECK THAT THE "MEMBRK" FLIP-FLOP WAS
CLEARED. THE PROGRAM WILL NOW SET THE TARGET EMULATOR SIGNAL "FETCT H"
TO THE HIGH STATE AND PULSE THE SIGNAL "XRAS H". A PULSE ON "XRAS H"
WILL CAUSE THE EDFET FLIP-FLOP TO BE SET AND THE ADDRESS TO BE CLOCKED
INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES. THE ADDRESS WILL
ADDRESS MEMORY ON THE MEMORY SIMULATOR MODULE WHICH IS MAPPED TO INHIBIT
READS AND WRITES, THEREFORE, THE SYSTEM BUS SIGNAL "RDE L" WILL BE
ASSERTED HIGH. AS A RESULT OF "RDE L", "EDFET H", "PSMW L" BEING
ASSERTED HIGH AND A PULSE ON "XRASD H", THE "MEMBRK" FLIP-FLOP WILL BE
DIRECT SET TO A ONE. THE SIGNAL "MEMBRK H" ASSERTED HIGH WILL CAUSE THE
SIGNAL "SOP H" TO BE ASSERTED HIGH. WHEN "SOP H" AND "EDFET H" ARE
ASSERTED HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO
A ONE. THE PROGRAM WILL CHECK THAT THE "MEMBRK" AND "PSMW" FLIP-FLOPS
ARE SET TO ONES. THE PROGRAM WILL NOW SET THE TARGET EMULATOR'S INTER-
RUPT ENBALE BIT AND LOWER THE CPU PRIORITY LEVEL TO ALLOW INTERRUPTS.
THE BREAK INTERRUPT FLIP-FLOP WAS SET TO A ONE PREVIOUSLY AS A RESULT
OF "MEMBRK H" BEING ASSERTED HIGH AND A PULSE BEING ISSUED ON "XRAS L".
THE PROGRAM WILL NOW CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE

INTERRUPT ENABLE BIT BEING SET, THE BREAK INTERRUPT FLIP-FLOP BEING SET,
AND THE CPU PRIORITY LEVEL BEING LOWERED TO ALLOW INTERRUPTS.   THE
PROGRAM WILL ISSUE A PULSE ON "BRKRES L" AND CHECK THAT THE "MEMBRK"
FLIP-FLOP WAS CLEARED BY THE PULSE ON "BRKRES L".

TEST 10:

THIS TEST WILL CHECK THAT THE MEMORY SIMULATOR "WRV" FLIP-FLOP CAN BE
CLEARED WHEN A "WRITE" OPERATION IS EXECUTED FROM THE TARGET EMULATOR
MODULE TO AN ADDRESS WHICH IS MAPPED IN THE MEMORY SIMULATOR MAP PROTEC-
TION RAM TO INHIBIT READS AND WRITES.   THE "WRV" FLIP-FLOP WILL BE
CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL "WRE H" BEING ASSERTED LOW
AND PULSES ON THE SIGNALS "WRHB H" AND "WRLB H".   THE SIGNALS "WRHB H"
AND "WRLB H" ARE PULSED BY THE TARGET EMULATOR MODULE AT "PI" TIME WHEN
THE TARGET EMULATOR MODULE IS EXECUTING A T-11 WRITE OPERATION.   THE
PROGRAM WILL CHECK THAT THE MEMORY SIMULATOR SIGNAL "MSBRK H" IS
ASSERTED HIGH AS A RESULT OF THE "WRV" FLIP-FLOP BEING CLEARED.   THE
PROGRAM WILL CHECK THE TARGET EMULATOR MODULES "MEMBRK" FLIP-FLOP TO
BE CLEARED AND THEN CAUSE A PULSE TO BE ISSUED ON TARGET EMULATOR MODULE
SIGNAL "XRAS H".   THE PROGRAM WILL NOW CHECK THE "MEMBRK" FLIP-FLOP TO
BE SET TO A ONE AS A RESULT OF A PULSE ON "XRAS H" AND THE MEMORY
SIMULATOR SYSTEM BUS SIGNAL "MSBRK H" BEING ASSERTED HIGH.   THE PROGRAM
WILL PRESET THE "WRV" FLIP-FLOP BY PULSING MEMORY SIMULATOR SIGNAL "RST H"
AND CHECK THAT THE SIGNAL "MSBRK H" WENT TO THE LOW STATE AS A RESULT OF
THE "WRV" FLIP-FLOP BEING PRESET.   THE PROGRAM WILL CLEAR THE "MEMBRK"
FLIP-FLOP BY PULSING TARGET EMULATOR SISGNAL "BRKRES L" AND CHECK THAT
THE "MEMBRK" FLIP-FLOP CLEARED.

TEST 11:

THIS TEST WILL CHECK THAT TARGET EMULATOR FDAL REGISTER BITS 7:2 CAN BE
CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES IN 16 BIT MODE WHEN THE TARGET
EMULATOR MODULE IS ADDRESSING A LOCATION WHICH IS MAPPED ON THE MEMORY
SIMULATOR MODULE TO ALLOW READS AND WRITES TO THE TARGET RAM.   TO CHECK
THAT THE TDAL LATCHES WERE CLOCKED WITH FDAL REGISTER DATA, THE PROGRAM
WILL ENABLE THE TDAL LATCHES TO THE EIDAL BUS WITH THE TARGET RAM STILL
BEING ADDRESSED.   THE PROGRAM WILL THEN READ AND CHECK THE EIDAL BUS TO
CONTAIN THE CORRECT FDAL REGISTER DATA.

TEST 12:

THIS TEST WILL CHECK THAT TARGET EMULATOR FDAL REGISTER BITS 7:2 CAN BE
CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES IN 8 BIT MODE WHEN THE TARGET
EMULATOR MODULE IS ADDRESSING A LOCATION WHICH IS MAPPED ON THE MEMORY
SIMULATOR MODULE TO ALLOW READS AND WRITES TO THE TARGET RAM.   TO CHECK
THAT THE TDAL LATCHES WERE CLOCKED WITH FDAL REGISTER DATA, THE PROGRAM
WILL ENABLE THE TDAL LATCHES TO THE EIDAL BUS WITH THE TARGET RAM STILL
BEING ADDRESSED.   THE PROGRAM WILL THEN READ AND CHECK THE EIDAL BUS TO
CONTAIN THE CORRECT FDAL REGISTER DATA.

TEST 13:

THIS TEST WILL CHECK THAT STATE ANALYZER SIGNAL "EDBRK H" CAN BE
ASSERTED HIGH AND LOW WHEN STATE ANALYZER FUNCTION SELECT FLIP-FLOP
"FUSL2" IS CLEARED AND SET.   THE OUTPUT OF FUNCTION SELECT FLIP-FLOP
"FUSL2" IS ENABLED TO THE SYSTEM BUS AS THE SIGNAL "EDBRK H" WHEN THE

SIGNAL "CDAL1 H" IS ASSERTED HIGH. THE PROGRAM WILL CHECK THAT THE
SIGNAL "EDBRK H" IS ASSERTED HIGH AND LOW BY READING THE SIGNAL IN
TARGET EMULATORS CONTROL REGISTER 0. THE TEST WILL ALSO CHECK THAT
THE SIGNAL "EDBRK H" WILL CAUSE THE TARGET EMULATOR'S PAUSE STATE LOGIC
TO BE ENTERED IN "RUN" MODE WHEN THE SIGNAL "FETCT H" IS ASSERTED HIGH
AND A PULSE IS ISSUED ON THE SIGNAL "XRAS H".

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1446
1447
1448                                    .TITLE PROGRAM HEADER AND TABLES
1449                                    .SBTTL  PROGRAM HEADER
1450
1451                                            .ENABL  ABS
1452                                            .ENABL  AMA
1453                                            .DSABL  GBL
1454          002000                            .       =       2000
1455
1456   002000                                   BGNMOD
1457
1458                                    ;++
1459                                    ; THE PROGRAM HEADER IS THE INTERFACE BETWEEN
1460                                    ; THE DIAGNOSTIC PROGRAM AND THE SUPERVISOR.
1461                                    ;--
1462
1463   002000                                   POINTER BGNSETUP
1464
1465
1466   002000                                   HEADER  CVCDD,B,0,60..0,PRIO7
1467   002000                           L$NAME::                 ;DIAGNOSTIC NAME
1468   002000        103                         .ASCII /C/
1469   002001        126                         .ASCII /V/
1470   002002        103                         .ASCII /C/
1471   002003        104                         .ASCII /D/
1472   002004        104                         .ASCII /D/
1473   002005        000                         .BYTE   0
1474   002006        000                         .BYTE   0
1475   002007        000                         .BYTE   0
1476   002010                           L$REV::                  ;REVISION LEVEL
1477   002010        102                         .ASCII  /B/
1478   002011                           L$DEPO::                 ;0
1479   002011        060                         .ASCII  /0/
1480   002012                           L$UNIT::                 ;NUMBER OF UNITS
1481   002012    000001                          .WORD   T$PTHV
1482   002014                           L$TIML::                 ;LONGEST TEST TIME
1483   002014    000074                          .WORD   60.
1484   002016                           L$HPCP::                 ;POINTER TO H.W. QUES.
1485   002016    035162                          .WORD   L$HARD
1486   002020                           L$SPCP::                 ;POINTER TO S.W. QUES.
1487   002020    000000                          .WORD   0
1488   002022                           L$HPTP::                 ;PTR. TO DEF. H.W. PTABLE
1489   002022    002160                          .WORD   L$HW
1490   002024                           L$SPTP::                 ;PTR. TO S.W. PTABLE
1491   002024    000000                          .WORD   0
1492   002026                           L$LADP::                 ;DIAG. END ADDRESS
1493   002026    035470                          .WORD   L$LAST
1494   002030                           L$STA::                  ;RESERVED FOR APT STATS
1495   002030    000000                          .WORD   0
1496   002032                           L$CO::
1497   002032    000000                          .WORD   0
1498   002034                           L$DTYP::                 ;DIAGNOSTIC TYPE
1499   002034    000000                          .WORD   0
1500   002036                           L$APT::                  ;APT EXPANSION
1501   002036    000000                          .WORD   0
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1502  002040                     L$DTP::                    ;PTR. TO DISPATCH TABLE
1503  002040  002124                   .WORD    L$DISPATCH
1504  002042                     L$PRIO::                   ;DIAGNOSTIC RUN PRIORITY
1505  002042  000340                   .WORD    PRIO7
1506  002044                     L$ENVI::                   ;FLAGS DESCRIBE HOW IT WAS SETUP
1507  002044  000000                   .WORD    0
1508  002046                     L$EXP1::                   ;EXPANSION WORD
1509  002046  000000                   .WORD    0
1510  002050                     L$MREV::                   ;SVC REV AND EDIT #
1511  002050     003                   .BYTE    C$REVISION
1512  002051     003                   .BYTE    C$EDIT
1513  002052                     L$EF::                     ;DIAG. EVENT FLAGS
1514  002052  000000                   .WORD    0
1515  002054  000000                   .WORD    0
1516  002056                     L$SPC::
1517  002056  000000                   .WORD    0
1518  002060                     L$DEVP::                   ; POINTER TO DEVICE TYPE LIST
1519  002060  002354                   .WORD    L$DVTYP
1520  002062                     L$REPP::                   ;PTR. TO REPORT CODE
1521  002062  000000                   .WORD    0
1522  002064                     L$EXP4::
1523  002064  000000                   .WORD    0
1524  002066                     L$EXP5::
1525  002066  000000                   .WORD    0
1526  002070                     L$AUT::                    ;PTR. TO ADD UNIT CODE
1527  002070  000000                   .WORD    0
1528  002072                     L$DUT::                    ;PTR. TO DROP UNIT CODE
1529  002072  000000                   .WORD    0
1530  002074                     L$LUN::                    ;LUN FOR EXERCISERS TO FILL
1531  002074  000000                   .WORD    0
1532  002076                     L$DESP::                   ;POINTER TO DIAG. DESCRIPTION
1533  002076  002366                   .WORD    L$DESC
1534  002100                     L$LOAD::                   ;GENERATE SPECIAL AUTOLOAD EMT
1535  002100  104035                   EMT      E$LOAD
1536  002102                     L$ETP::                    ;POINTER TO ERRTBL
1537  002102  000000                   .WORD    0
1538  002104                     L$ICP::                    ;PTR. TO INIT CODE
1539  002104  013112                   .WORD    L$INIT
1540  002106                     L$CCP::                    ;PTR. TO CLEAN-UP CODE
1541  002106  013346                   .WORD    L$CLEAN
1542  002110                     L$ACP::                    ;PTR. TO AUTO CODE
1543  002110  013344                   .WORD    L$AUTO
1544  002112                     L$PRT::                    ;PTR. TO PROTECT TABLE
1545  002112  013104                   .WORD    L$PROT
1546  002114                     L$TEST::                   ;TEST NUMBER
1547  002114  000000                   .WORD    0
1548  002116                     L$DLY::                    ;DELAY COUNT
1549  002116  000000                   .WORD    0
1550  002120                     L$HIME::                   ;PTR. TO HIGH MEM
1551  002120  000000                   .WORD    0
1552
```

```
1553                                    .SBTTL   DISPATCH TABLE
1554
1555                            ;++
1556                            ; THE DISPATCH TABLE CONTAINS THE STARTING ADDRESS OF EACH TEST.
1557                            ; IT IS USED BY THE SUPERVISOR TO DISPATCH TO EACH TEST.
1558                            ;--
1559
1560  002122                            DISPATCH 13.
1561  002122  000015                    .WORD    13
1562  002124                    L$DISPATCH::
1563  002124  013400                    .WORD    T1
1564  002126  013406                    .WORD    T2
1565  002130  014266                    .WORD    T3
1566  002132  015670                    .WORD    T4
1567  002134  016770                    .WORD    T5
1568  002136  021132                    .WORD    T6
1569  002140  023752                    .WORD    T7
1570  002142  025430                    .WORD    T8
1571  002144  026612                    .WORD    T9
1572  002146  030116                    .WORD    T10
1573  002150  031072                    .WORD    T11
1574  002152  032604                    .WORD    T12
1575  002154  034326                    .WORD    T13
1576
```

```
1577                                    .SBTTL  DEFAULT HARDWARE P-TABLE
1578
1579                                    ;++
1580                                    ; THE DEFAULT HARDWARE P-TABLE CONTAINS DEFAULT VALUES OF
1581                                    ; THE TEST-DEVICE PARAMETERS.  THE STRUCTURE OF THIS TABLE
1582                                    ; IS IDENTICAL TO THE STRUCTURE OF THE HARDWARE P-TABLES,
1583                                    ; AND IS USED AS A ''TEMPLATE'' FOR BUILDING THE P-TABLES.
1584                                    ;--
1585
1586     002156                                 BGNHW   DFPTBL
1587     002156   000005                        .WORD   L10000-L$HW/2
1588     002160                         L$HW::
1589     002160                         DFPTBL::
1590
1591     002160   163010                         .WORD   163010                  ;CSR ADDRESS
1592     002162   000370                         .WORD   370                     ;VECTOR ADDRESS
1593     002164   000000                         .WORD   0                       ;DEVICE SELECTION # FOR MEMORY SIMULATOR
1594     002166   000001                         .WORD   1                       ;DEVICE SELECTION # FOR STATE ANALYZER
1595     002170   000002                         .WORD   2                       ;DEVICE SELECTION # FOR TARGET EMULATOR
1596
1597
1598     002172                                  ENDHW
1599     002172                         L10000:
1600
1601                                    .SBTTL  SOFTWARE P-TABLE
1602
1603                                    ;++
1604                                    ; THE SOFTWARE TABLE CONTAINS VARIOUS DATA USED BY THE
1605                                    ; PROGRAM AS OPERATIONAL PARAMETERS.  THESE PARAMETERS ARE
1606                                    ; SET UP AT ASSEMBLY TIME AND MAY BE VARIED BY THE OPERATOR
1607                                    ; AT RUN TIME.
1608                                    ;--
1609
1610     002172                                  BGNSW   SFPTBL
1611     002172   000000                         .WORD   L10001-L$SW/2
1612     002174                         L$SW::
1613     002174                         SFPTBL::
1614
1615
1616     002174                                  ENDSW
1617     002174                         L10001:
1618
1619     002174                                  ENDMOD
```

```
1620                                    .TITLE GLOBAL AREAS
1621                                    .SBTTL   GLOBAL EQUATES SECTION
1622
1623
1624    002174                          BGNMOD
1625
1626                            ;++
1627                            ; THE GLOBAL EQUATES SECTION CONTAINS PROGRAM EQUATES THAT
1628                            ; ARE USED IN MORE THAN ONE TEST.
1629                            ;--
1630
1631
1632    002174                          EQUALS
1633                            ;
1634                            ; BIT DIFINITIONS
1635                            ;
1636            100000          BIT15== 100000
1637            040000          BIT14== 40000
1638            020000          BIT13== 20000
1639            010000          BIT12== 10000
1640            004000          BIT11== 4000
1641            002000          BIT10== 2000
1642            001000          BIT09== 1000
1643            000400          BIT08== 400
1644            000200          BIT07== 200
1645            000100          BIT06== 100
1646            000040          BIT05== 40
1647            000020          BIT04== 20
1648            000010          BIT03== 10
1649            000004          BIT02== 4
1650            000002          BIT01== 2
1651            000001          BIT00== 1
1652                            ;
1653            001000          BIT9==  BIT09
1654            000400          BIT8==  BIT08
1655            000200          BIT7==  BIT07
1656            000100          BIT6==  BIT06
1657            000040          BIT5==  BIT05
1658            000020          BIT4==  BIT04
1659            000010          BIT3==  BIT03
1660            000004          BIT2==  BIT02
1661            000002          BIT1==  BIT01
1662            000001          BIT0==  BIT00
1663                            ;
1664                            ; EVENT FLAG DEFINITIONS
1665                            ;   EF32:EF17 RESERVED FOR SUPERVISOR TO PROGRAM COMMUNICATION
1666                            ;
1667            000040          EF.START==      32.                 ; START COMMAND WAS ISSUED
1668            000037          EF.RESTART==    31.                 ; RESTART COMMAND WAS ISSUED
1669            000036          EF.CONTINUE==   30.                 ; CONTINUE COMMAND WAS ISSUED
1670            000035          EF.NEW==        29.                 ; A NEW PASS HAS BEEN STARTED
1671            000034          EF.PWR==        28.                 ; A POWER-FAIL/POWER-UP OCCURRED
1672                            ;
1673                            ;
1674                            ; PRIORITY LEVEL DEFINITIONS
1675                            ;
```

```
1676          000340                       PRI07== 340
1677          000300                       PRI06== 300
1678          000240                       PRI05== 240
1679          000200                       PRI04== 200
1680          000140                       PRI03== 140
1681          000100                       PRI02== 100
1682          000040                       PRI01== 40
1683          000000                       PRI00== 0
1684                                       ;
1685                                       ;OPERATOR FLAG BITS
1686                                       ;
1687          000004                       EVL==        4
1688          000010                       LOT==       10
1689          000020                       ADR==       20
1690          000040                       IDU==       40
1691          000100                       ISR==      100
1692          000200                       UAM==      200
1693          000400                       BOE==      400
1694          001000                       PNT==     1000
1695          002000                       PRI==     2000
1696          004000                       IXE==     4000
1697          010000                       IBE==    10000
1698          020000                       IER==    20000
1699          040000                       LOE==    40000
1700          100000                       HOE==   100000
1701
```

```
1702
1703                              ;****************************************************************************
1704                              ;
1705                              ;        MDE/T-11 MEMORY SIMULATOR CONTROL REGISTER INFORMATION
1706                              ;
1707                              ;****************************************************************************
1708
1709                              ;
1710                              ;MEMORY SIMULATOR CONTROL REGISTER 0
1711                              ;
1712
1713      100000                 IDH==   BIT15                               ;BIT 15=1 READ DEVICE TYPE IN 15:8
1714                                                                          ;MS DEVICE TYPE EQUALS 400 (BIT8=1)
1715                                                                          ;
1716                                                                          ;BIT 15=0 READ DEVICE NUMBER INTO BITS 15:8
1717
1718                                                                          ;BIT 14 ALWAYS READ AS A ZERO
1719                                                                          ;BIT 13 ALWAYS READ AS A ZERO
1720                                                                          ;BIT 12 ALWAYS READ AS A ZERO
1721
1722      004000                 SIG11H==BIT11                               ;BITS 11-8 ARE USED TO SELECT THE
1723      002000                 SIG10H==BIT10                               ;DEVICE NUMBER TO ASSERT THE SIGNAL
1724      001000                 SIG9H== BIT9                                ;DEVE L.   WHEN SELECTING MS THESE BITS
1725      000400                 SIG8H== BIT8                                ;MUST = THE SETTING OF SWITCHES DEV 3:0
1726
1727                                                                          ;BIT 7 ALWAYS READ AS A ZERO (UNUSED)
1728
1729      000100                 CKH==   BIT6                                ;CLOCK HIGH - (R/W)
1730      000040                 WRVH==  BIT5                                ;WRITE VIOLATION (READ ONLY)
1731      000020                 RDVH==  BIT4                                ;READ VIOLATION (READ ONLY)
1732      000010                 BIT8H== BIT3                                ;8 BIT MODE (1) - 16 BIT MODE (0) - (R/W)
1733      000004                 MPH==   BIT2                                ;MAP PROTECT SELECT (R/W)
1734      000002                 CTSH==  BIT1                                ;MEM ACCESS FROM LSI-i1 BUS (1) - (R/W)
1735                                                                          ;MEM ACCESS FROM SYSTEM BUS (0) - (R/W)
1736      000001                 RSTH==  BIT0                                ;RESET MEMORY SIMULATOR MODULE (1) - (R/W)
1737
1738                              ;
1739                              ;MEMORY SIMULATOR CONTROL REGISTER 2
1740                              ;
1741
1742                                                                          ;BITS 15:8 ARE NOT AVAILABLE
1743
1744      000200                 MSBRKH==BIT7                                ;MEMORY SIMULATOR BREAK (READ ONLY)
1745      000100                 WRENH== BIT6                                ;WRITE ENABLE (READ ONLY)
1746      000040                 ESRH==  BIT5                                ;ENABLE SIMULATOR RAM (READ ONLY
1747
1748                                                                          ;BIT 4 ALWAYS READ AS A ZERO (UNUSED)
1749
1750      000010                 MSEL1== BIT3                                ;MEMORY SELECT (R/W)
1751      000004                 MSEL0== BIT2                                ;MEMORY SELECT (R/W)
1752
1753                              ;       MSEL1=0 MSEL0=0 - SELECT SIMULATOR MEMORY - SSM L
1754                              ;       MSEL1=0 MSEL0=1 - SELECT MODULE SELECT MEMORY 0 - SMDS0 L
1755                              ;       MSEL1=1 MSEL0=0 - SELECT MAP PROTECT MEMORY - SMPM L
1756                              ;       MSEL1=1 MSEL0=1 - SELECT MODULE SELECT MEMORY 1 - SMDS1 L
1757
```

```
1758        0G0002              MSAD17==BIT1                        ;MEMORY SIMULATOR ADDRESS 17 (R/W)
1759        000001              MSAD16==BIT0                        ;MEMORY SIMULAOTR ADDRESS 16 (R/W)
1760
1761                            ;
1762                            ;MEMORY SIMULATOR CONTROL REGEISTER 4
1763                            ;
1764
1765        100000              MSAD15==BIT15                       ;MEMORY SIMULATOR ADDRESS 15 (R/W)
1766        040000              MSAD14==BIT14                       ;MEMORY SIMULATOR ADDRESS 14 (R/W)
1767        020000              MSAD13==BIT13                       ;MEMORY SIMULATOR ADDRESS 13 (R/W)
1768        010000              MSAD12==BIT12                       ;MEMORY SIMULATOR ADDRESS 12 (R/W)
1769        004000              MSAD11==BIT11                       ;MEMORY SIMULATOR ADDRESS 11 (R/W)
1770        002000              MSAD10==BIT10                       ;MEMORY SIMULATOTR ADDRESS 10 (R/W)
1771        001000              MSAD9== BIT9                        ;MEMORY SIMULATOR ADDRESS 09 (R/W)
1772        000400              MSAD8== BIT8                        ;MEMORY SIMULATOR ADDRESS 08 (R/W)
1773        000200              MSAD7== BIT7                        ;MEMORY SIMULATOR ADDRESS 07 (R/W)
1774        000100              MSAD6== BIT6                        ;MEMORY SIMULATOR ADDRESS 06 (R/W)
1775        000040              MSAD5== BIT5                        ;MEMORY SIMULATOR ADDRESS 05 (R/W)
1776        000020              MSAD4== BIT4                        ;MEMORY SIMULATOR ADDRESS 04 (R/W)
1777        000010              MSAD3== BIT3                        ;MEMORY SIMULAOTR ADDRESS 03 (R/W)
1778        000004              MSAD2== BIT2                        ;MEMORY SIMULATOR ADDRESS 02 (R/W)
1779        000002              MSAD1== BIT1                        ;MEMORY SIMULATOR ADDRESS 01 (R/W)
1780        000001              MSAD0== BIT0                        ;MEMORY SIMULATOR ADDRESS 00 (R/W)
1781
1782                            ;
1783                            ;MEMORY SIMULATOR MAP PROTECT BITS - CONTROL REGISTER 6
1784                            ;
1785
1786        000010              MUTB==  BIT3                        ;
1787        000004              RDEH==  BIT2                        ;READ ENABLED SIMULATOR MEMORY
1788        000002              WREH==  BIT1                        ;WRITE ENABLED SIMULATOR MEMORY
1789        000001              MPINH== BIT0                        ;MAPPED INTO MEMORY SIMULATOR
```

```
1790                        ;*************************************************************************************
1791
1792                        ;           MDE/T-11 STATE ANALYZER CONTROL REGISTER INFORMATION
1793
1794                        ;*************************************************************************************
1795
1796
1797                        ;
1798                        ;CONTROL REGISTER 0 (CDAL BITS 15:0)
1799                        ;
1800
1801     100000            CDAL15==BIT15                            ;BIT15=1 READ DEVICE TYPE IN BITS 15:8
1802                                                                ;STATE ANALYZER DEVICE TYPE = 1000 (BIT9=1)
1803                                                                ;
1804                                                                ;BIT15=0 READ DEVICE NUMBER INTO
1805                                                                ;BITS 15:8
1806
1807     040000            CDAL14==BIT14                            ;ALWAYS READ AS A ZERO
1808     020000            CDAL13==BIT13                            ;ALWAYS READ AS A ZERO
1809     010000            CDAL12==BIT12                            ;ALWAYS READ AS A ZERO
1810
1811     004000            CDAL11==BIT11                            ;BITS 11:8 ARE USED TO SELECT THE DEVICE
1812     002000            CDAL10==BIT10                            ;NUMBER TO ASSERT THE SIGNAL DEVE L.
1813     001000            CDAL9== BIT9                             ;WHEN SELECTING SA THESE BITS MUST EQUAL
1814     000400            CDAL8== BIT8                             ;THE SETTING OF SWITCHES DEV 3:0
1815
1816     000200            CDAL7== BIT7                             ;1 - DISABLE OUTPUTS OF OR ADDRESS REG
1817                                                                ;     ENABLE FOUT 3:0 TO DRIVE OR ADDRESS
1818                                                                ;0 - ENABLE OUTPUTS OF OR ADDRESS REG
1819
1820     000100            CDAL6== BIT6                             ;1/0 - CLOCK SIGNAL ''TRNST H''
1821
1822     000040            CDAL5== BIT5                             ;1 - STOP TRACING WHEN TRAD10 H SET HIGH
1823                                                                ;0 - CONTINUOUS TRACING
1824
1825     000020            CDAL4== BIT4                             ;1 - ENABLE ALL AND/OR ARRAY RAMS
1826                                                                ;0 - ENABLE ONLY ONE AND/OR ARRAY RAM
1827
1828     000010            CDAL3== BIT3                             ;TRACE RAM BUS SELECT
1829     000004            CDAL2== BIT2                             ;TRACE RAM BUS SELECT
1830
1831     000002            CDAL1== BIT1                             ;ENABLE FUNCTION SELECTS ONTO SYSTEM BUS
1832
1833     000001            CDAL0== BIT0                             ;1/0 - ZERO TRACE ADDRESS REG. TRACING
1834                                                                ;      FLIP-FLOP AND SBL FLIP-FLOPS 59:56.
1835                                                                ;      LOAD EVNT CNTR'S VIA EVNT CNTR REG.
1836
1837
1838                        ;CONTROL REGISTER 2 (PDAL BITS 7:0)
1839                        ;
1840
1841                                                                ;BITS 15:8 ARE NOT AVAILABLE
1842
1843     000200            PDAL7== BIT7                             ;1 - CLEAR EVENT COUNTERS
1844
1845     000100            PDAL6== BIT6                             ;1 - PRESET TRACING FLIP-FLOP
```

```
1846
1847         000040              PDAL5== BIT5                        ;0 - CLEAR FUNCTION SELECT FLIP-FLOPS
1848
1849         000020              PDAL4== BIT4                        ;1 - EXTERNAL PROBE "CLK" SIGNAL WILL
1850                                                                 ;    LOAD EXTP 7:0 F/F'S WHEN "CLK" SET LOW
1851                                                                 ;0 - EXTERNAL PROBE "CLK" SIGNAL WILL
1852                                                                 ;    LOAD EXTP 7:0 F/F'S WHEN "CLK" SET HIGH
1853
1854         000010              PDAL3== BIT3                        ;SELECT POINTER REGISTER (SEE BELOW)
1855         000004              PDAL2== BIT2                        ;SELECT POINTER REGISTER (SEE BELOW)
1856         000002              PDAL1== BIT1                        ;SELECT POINTER REGISTER (SEE BELOW)
1857         000001              PDAL0== BIT0                        ;SELECT POINTER REGISTER (SEE BELOW)
1858
1859                             ;
1860                             ;POINTER REGISTER PTER 15:0 (SELECTED BY PDAL 3:0)
1861                             ;
1862
1863         000000              PTER0== 0                           ;WPT0,RPT0,R/W TRAM ADDRESS 9:0
1864         000001              PTER1== PDAL0                       ;WPT1,RPT1,R/W TRAM DATA LSI-11 TO TRDI 15:0
1865         000002              PTER2== PDAL1                       ;WPT2,RPT2,R/W TRAM DATA LSI-11 TO TRDI 31:16
1866         000003              PTER3== PDAL1!PDAL0                 ;WPT3,RPT3,R/W TRAM DATA LSI-11 TO TRDI 47:32
1867         000004              PTER4== PDAL2                       ;WPT4,RPT4,R/W TRAM DATA LSI-11 TO TRDI 59:48
1868         000005              PTER5== PDAL2!PDAL0                 ;WPT5, WRITE TRACE RAM DATA IN BUF 15:0
1869         000006              PTER6== PDAL2!PDAL1                 ;WPT6, WRITE TRACE RAM DATA IN BUF 31:16
1870         000007              PTER7== PDAL2!PDAL1!PDAL0           ;WPT7, WRITE TRACE RAM DATA IN BUF 47:32
1871         000010              PTER8== PDAL3                       ;WPT8, WRITE TRACE RAM DATA IN BUF 59:48
1872         000011              PTER9== PDAL3!PDAL0                 ;WPT9, LOAD EVENT COUNTER 0
1873         000012              PTER10==PDAL3!PDAL1                 ;WPT10,LOAD EVENT COUNTER 1
1874         000013              PTER11==PDAL3!PDAL1!PDAL0           ;WPT11,LOAD EVENT COUNTER 2
1875         000014              PTER12==PDAL3!PDAL2                 ;WPT12,LOAD EVENT COUNTER 3
1876         000015              PTER13==PDAL3!PDAL2!PDAL0           ;NOT USED
1877         000016              PTER14==PDAL3!PDAL2!PDAL1           ;NOT USED
1878         000017              PTER15==PDAL3!PDAL2!PDAL1!PDAL0     ;WPT15,RPT15, R/W "OR" ADDRESS
1879
1880
```

```
 1881
 1882                           ;***************************************************************************
 1883                           ;
 1884                           ;          MDE/T-11 TARGET EMULATOR CONTROL REGISTER INFORMATION
 1885                           ;
 1886                           ;***************************************************************************
 1887
 1888                           ;
 1889                           ;CONTROL REGISTER 0 (GDAL BITS 15:0)
 1890                           ;
 1891
 1892        100000            GDAL15==BIT15                               ;BIT15=1 READ DEVICE TYPE IN 15:8
 1893                                                                      ;TE DEVICE TYPE EQUALS 0000
 1894                                                                      ;
 1895                                                                      ;BIT15=0 READ DEVICE NUMBER INTO
 1896                                                                      ;BITS 11:8
 1897
 1898        040000            GDAL14==BIT14                               ;ALWAYS A 0 ON READ
 1899        020000            GDAL13==BIT13                               ;ALWAYS A 0 ON READ
 1900        010000            GDAL12==BIT12                               ;ALWAYS A 0 ON READ
 1901
 1902        004000            GDAL11==BIT11                               ;BITS 11-8 ARE USED TO SELECT THE
 1903        002000            GDAL10==BIT10                               ;DEVICE NUMBER TO ASSERT THE SIGNAL
 1904        001000            GDAL9== BIT9                                ;DEVE L. WHEN SELECTING TE THESE BITS
 1905        000400            GDAL8== BIT8                                ;MUST = THE SETTING OF DEV 3 - DEV 0
 1906
 1907        000200            GDAL7== BIT7                                ;SINGLE STEP BREAK INDICATOR (READ ONLY)
 1908        000100            GDAL6== BIT6                                ;TIMEOUT BREAK INDICATOR (READ ONLY)
 1909        000040            GDAL5== BIT5                                ;MEMORY SIM BREAK INDICATOR (READ ONLY)
 1910        000020            GDAL4== BIT4                                ;STATE ANALYZER BREAK INDICATOR (READ ONLY)
 1911        000010            GDAL3== BIT3                                ;ENABLE INTERRUPTS WHEN = TO 1
 1912        000004            GDAL2== BIT2                                ;POINTER FOR EXTENDED REG SELECT
 1913        000002            GDAL1== BIT1                                ;POINTER FOR EXTENDED REG SELECT
 1914        000001            GDAL0== BIT0                                ;POINTER FOR EXTENDED REG SELECT
 1915
 1916                           ;
 1917                           ;EXTENDED REGISTER SELECTED VIA GDAL BITS 2:0
 1918                           ;
 1919
 1920        000000            ADDRES==0                                   ;WRITE DIAG ADDRESS REGISTER (WPT0)
 1921                                                                      ;READ ADDRESS BUS (RPT0)
 1922        000001            FJADR== GDAL0                               ;WRITE NEW FORCE JUMP ADDRESS REG (WPT1)
 1923                                                                      ;READ FORCE JUMP ADDRESS READBACK REG (RPT1)
 1924        000002            FDAL==  GDAL1                               ;WRITE FDAL AND EOAI REGISTERS (WPT2)
 1925                                                                      ;READ FDAL/EOAI OR FDAL/CTL REG (RTP2)
 1926        000003            HDAL==  GDAL1!GDAL0                         ;WRITE/READ HDAL REGISTER (WPT3/RPT3)
 1927        000004            MODE==  GDAL2                               ;WRITE/READ MODEE REGISTER (WPT4/RPT4)
 1928        000005            TARMOD==GDAL2!GDAL0                         ;READ TARGET MODE REGISTER (RPT5)
 1929        000006            EIDAL== GDAL2!GDAL1                         ;READ EIDAL BUS (RPT6)
 1930        000007            EODAL== GDAL2!GDAL1!GDAL0                   ;READ EODAL BUS (RPT7)
 1931
 1932                           ;
 1933                           ;OTHER BIT DEFINITIONS FOR GDAL BITS 7:4
 1934                           ;
 1935
 1936        000200            SSBRK== GDAL7                               ;SINGLE STEP BREAK INDICATOR (READ ONLY)
```

```
1937        000100              TOBRK== GDAL6                    ;TIMEOUT BREAK INDICATOR (READ ONLY)
1938        000040              MEMBRK==GDAL5                    ;MEMORY SIM BREAK INDICATOR (READ ONLY)
1939        000020              EDBRK== GDAL4                    ;STATE ANALYZER BREAK INDICATOR (READ ONLY)
1940
1941                            ;
1942                            ;CONTROL REGISTER 2 (ADAL BITS 15:0)
1943                            ;
1944
1945        100000              ADAL15==BIT15                   ;SELECT COLUMN AI FOR STATE ANALYZER
1946        040000              ADAL14==BIT14                   ;1 - SELECT ROW/COLUMN FOR AI TO STATE ANALYZER
1947                                                            ;0 - SELECT SERVICE FOR AI TO STATE ANALYZER
1948        020000              ADAL13==BIT13                   ;ENABLE SERVICE FOR EMULATOR
1949        010000              ADAL12==BIT12                   ;ENABLE MODE FROM EMULATOR
1950        004000              ADAL11==BIT11                   ;DISABLE SERVICE TO THE TARGET
1951        002000              ADAL10==BIT10                   ;MASTER SWITCH
1952        001000              ADAL9== BIT9                    ;ENABLE STATE ANALYZER CLOCKS (1)
1953        000400              ADAL8== BIT8                    ;ENABLE TIMEOUT BREAK
1954        000200              ADAL7== BIT7                    ;ENABLE REFRESH TO STATE ANALYZER
1955        000100              ADAL6== BIT6                    ;
1956        000040              ADAL5== BIT5                    ;1 - ENABLE SINGLE STEP BREAK
1957                                                            ;0 - DISABLE SINGLE STEP BREAK
1958        000020              ADAL4== BIT4                    ;1 - PAUSE STATE MACHINE (RUN MODE)
1959                                                            ;0 - PAUSE STATE MACHINE (PAUSE MODE)
1960        000010              ADAL3== BIT3                    ;POWER-UP FROM TARGET (1)
1961        000004              ADAL2== BIT2                    ;POWER-UP FROM T-11
1962        000002              ADAL1== BIT1                    ;ENABLE INTERNAL CLOCK (1)
1963        000001              ADAL0== BIT0                    ;RESETS BREAK LOGIC (1)
1964
1965
1966                            ;
1967                            ;CONTROL REGISTER 4 (VDAL BITS 15:0)
1968                            ;
1969        100000              VDAL15==BIT15                   ;TDFI H - TAKE NEW FORCE JUMP ADDRESS (READ ONLY
1970        040000              VDAL14==BIT14                   ;EP8N H - 8 BIT ADDRESS HB F/F (READ ONLY)
1971        020000              VDAL13==BIT13                   ;EP8G H - 8 BIT ADDRESS LB F/F (READ ONLY)
1972        010000              VDAL12==BIT12                   ;EP8F H - 8 BIT INSTR HB F/F (READ ONLY)
1973        004000              VDAL11==BIT11                   ;EPFN H - 16 BIT ADDRESS F/F (READ ONLY)
1974        002000              VDAL10==BIT10                   ;EPSF H - PAUSE STATE SYNC F/F (READ ONLY)
1975        001000              VDAL9== BIT9                    ;PSMW H - PAUSE STATE WORKING F/F (READ ONLY)
1976        000400              VDAL8== BIT8                    ;PSMW  H - GET NEW ADDRESS F/F (READ ONLY)
1977        000200              VDAL7== BIT7                    ;DIAGNOSTIC FETCT H (R/W)
1978        000100              VDAL6== BIT6                    ;MSDI H - LOGIC LEVEL MSDI H (READ ONLY)
1979        000040              VDAL5== BIT5                    ;BTS1 H - LOGIC LEVEL BTS1 H (READ ONLY)
1980        000020              VDAL4== BIT4                    ;EDEOC H - LOGIC LEVEL EDEOC H (READ ONLY)
1981        000010              VDAL3== BIT3                    ;READ H - LOGIC LEVEL READ H (READ ONLY)
1982        000004              VDAL2== BIT2                    ;CLOCK TAI, TDAL, 0 PAUSE STATE MACHINE (R/W)
1983        000002              VDAL1== BIT1                    ;SPARE
1984        000001              VDAL0== BIT0                    ;ENABLE TAI AND TDAL READBACK FROM POD (R/W)
1985
1986
1987                            ;
1988                            ;CONTROL REGISTER 6 (HDAL BITS 15:0)
1989                            ;
1990        100000              HDAL15==BIT15                   ;1/0 - PULSE SIGNAL XPI L
1991        040000              HDAL14==BIT14                   ;1/0 - PULSE SIGNAL EIDAL17 H
1992        020000              HDAL13==BIT13                   ;1/0 - PULSE SIGNAL XCAS H
```

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1993        010000              HDAL12==BIT12                       ;1/0 - PULSE SIGNAL XRAS H
1994        004000              HDAL11==BIT11                       ;1/0 - PULSE SIGNAL EIDAL16 H
1995        002000              HDAL10==BIT10                       ;SPARE
1996        001000              HDAL9== BIT9                        ;1 - ENABLE DIAG ADDRESS TO ADDRESS BUS
1997                                                                ;0 - ENABLE EIDAL BUS TO ADDRESS BUS
1998                                                                ;     WHEN ADAL10 H IS SET TO A ONE AND
1999                                                                ;     DISABLE DIAG ADDRESS FROM ADDRESS BUS
2000        000400              HDAL8== BIT8                        ;1/0 - PULSE CREADY H
2001        000200              HDAL7== BIT7                        ;1/0 - PULSE PBCLR H
2002        000100              HDAL6== BIT6                        ;1/0 - PULSE PSEL1 H
2003        000040              HDAL5== BIT5                        ;1/0 - PULSE PSEL0 H
2004        000020              HDAL4== BIT4                        ;1/0 - PULSE PR/WHB L
2005        000010              HDAL3== BIT3                        ;1/0 - PULSE PR/WLB L
2006        000004              HDAL2== BIT2                        ;1 - ENABLES DIAG CONTROL OF T-11 TIMING
2007                                                                ;    AND CONTROL SIGNALS
2008                                                                ;0 - ENABLES T-11 TO GENERATE SIGNALS
2009        000002              HDAL1== BIT1                        ;SPARE
2010        000001              HDAL0== BIT0                        ;1/0 - PULSE MSDI H
2011
2012                            ;
2013                            ;CONTROL REGISTER 6 (MODE REG BITS MR 15:0)
2014                            ;
2015
2016        100000              MR15==  BIT15                       ;
2017        040000              MR14==  BIT14                       ;
2018        020000              MR13==  BIT13                       ;
2019        010000              MR12==  BIT12                       ;
2020        004000              MR11==  BIT11                       ;1 - 8 BIT ADDRESS SELECTION
2021                                                                ;0 - 16 BIT ADDRESS SELECTION
2022        002000              MR10==  BIT10                       ;
2023        001000              MR9==   BIT9                        ;
2024        000400              MR8==   BIT8                        ;
2025        000200              MR7==   BIT7                        ;
2026        000100              MR6==   BIT6                        ;
2027        000040              MR5==   BIT5                        ;
2028        000020              MR4==   BIT4                        ;
2029        000010              MR3==   BIT3                        ;
2030        000004              MR2==   BIT2                        ;
2031        000002              MR1==   BIT1                        ;
2032        000001              MR0==   BIT0                        ;
2033
2034                            ;
2035                            ;CONTROL REGISTER 6 (FDAL BITS 7:0)
2036                            ;
2037
2038                                                                ;THE CTL REGISTER AND EOAI REGISTER ARE
2039                                                                ;MULTIPLEXED INTO BITS 15:8. THE REGISTER
2040                                                                ;TO BE READ IS SELECTED BY FDAL0.
2041
2042        000200              FDAL7== BIT7                        ;INTERRUPT VECTOR
2043        000100              FDAL6== BIT6                        ;INTERRUPT VECTOR
2044        000040              FDAL5== BIT5                        ;INTERRUPT VECTOR
2045        000020              FDAL4== BIT4                        ;INTERRUPT VECTOR
2046        000010              FDAL3== BIT3                        ;INTERRUPT VECTOR
2047        000004              FDAL2== BIT2                        ;INTERRUPT VECTOR
2048        000002              FDAL1== BIT1                        ;SPARE
```

```
2049          0G0001                    FDAL0== BIT0                              ;1 - ENABLES EOAI 7:0 BUS TO BE READ ON 15:8
2050                                                                              ;0 - ENABLES CTL 7:0 REG TO BE READ ON 15:8
2051
2052                                    ;
2053                                    ;CONTROL REGISTER 6 (DIAG. ADDR BITS 15:0)
2054                                    ;
2055
2056          100000                    ADDR15==BIT15                             ;
2057          040000                    ADDR14==BIT14                             ;
2058          020000                    ADDR13==BIT13                             ;
2059          010000                    ADDR12==BIT12                             ;
2060          004000                    ADDR11==BIT11                             ;
2061          002000                    ADDR10==BIT10                             ;
2062          001000                    ADDR9== BIT9                              ;
2063          000400                    ADDR8== BIT8                              ;
2064          000200                    ADDR7== BIT7                              ;
2065          000100                    ADDR6== BIT6                              ;
2066          000040                    ADDR5== BIT5                              ;
2067          000020                    ADDR4== BIT4                              ;
2068          000010                    ADDR3== BIT3                              ;
2069          000004                    ADDR2== BIT2                              ;
2070          000002                    ADDR1== BIT1                              ;
2071          000001                    ADDR0== BIT0                              ;
2072
```

```
2073                                     .SBTTL   GLOBAL DATA SECTION
2074
2075                                     ;++
2076                                     ; THE GLOBAL DATA SECTION CONTAINS DATA THAT ARE USED
2077                                     ; IN MORE THAN ONE TEST.
2078                                     ;--
2079
2080
2081   002174                                    ERRTBL
2082   002174                            L$ERRTBL::
2083   002174   000000                   ERRTYP::          .WORD   0
2084   002176   000000                   ERRNBR::          .WORD   0
2085   002200   000000                   ERRMSG::          .WORD   0
2086   002202   000000                   ERRBLK::          .WORD   0
2087
2088                                     ;
2089                                     ;GLOBAL DATA FOR CONTROL REGISTER ADDRESSES AND DEVICE INFORMATION
2090                                     ;
2091
2092   002204   163010                   REG0::   .WORD   163010              ;CONTROL REGISTER 0
2093   002206   163012                   REG2::   .WORD   163012              ;CONTROL REGISTER 2
2094   002210   163014                   REG4::   .WORD   163014              ;CONTROL REGISTER 4
2095   002212   163016                   REG6::   .WORD   163016              ;CONTROL REGISTER 6
2096
2097   002214   000000                   TEVECT::.WORD    0                   ;TARGET EMULATOR VECTOR ADDRESS
2098
2099   002216   000000                   MSDEV:: .WORD    0                   ;MEMORY SIMULATOR DEVICE NUMBER
2100   002220   000000                   MSTYPE::.WORD    0                   ;MEMORY SIMULATOR DEVICE TYPE
2101
2102   002222   000000                   EDDEV:: .WORD    0                   ;STATE ANALYZER DEVICE NUMBER
2103   002224   000000                   EDTYPE::.WORD    0                   ;STATE ANALYZER DEVICE TYPE
2104
2105   002226   000000                   TEDEV:: .WORD    0                   ;TARGET EMULATOR DEVICE NUMBER
2106   002230   000000                   TETYPE::.WORD    0                   ;TARGET EMULATOR DEVICE TYPE
2107
2108   002232   000000                   UNITNB::.WORD    0                   ;NUMBER OF UNIT BEING TESTED (0-?)
2109
2110
2111                                     ;
2112                                     ;GLOBAL DATA FOR MEMORY SIMULATOR
2113                                     ;
2114
2115   002234   000000                   S0LOAD::.WORD    0                   ;WORD LOADED INTO REG 0
2116   002236   000000                   S0GOOD::.WORD    0                   ;EXPECTED REGISTER 0 CONTENTS ON READ
2117   002240   000000                   S0MASK::.WORD    0                   ;REG 0 MASK WORD
2118   002242   000000                   S0READ::.WORD    0                   ;ACTUAL REGISTER 0 READ FOR REG 0
2119
2120   002244   000000                   S2LOAD::.WORD    0                   ;WORD LOADED INTO REGISTER 2
2121   002246   000000                   S2GOOD::.WORD    0                   ;EXPECTED REGISTER 2 CONTENTS ON READ
2122   002250   000000                   S2MASK::.WORD    0                   ;REGISTER 2 MASK WORD
2123   002252   000000                   S2READ::.WORD    0                   ;REG 2 READ WITH MASK BITS CLEARED
2124
2125   002254   000000                   S4LOAD::.WORD    0                   ;WORD LOADED INTO REG 4
2126   002256   000000                   S4READ::.WORD    0                   ;ACTUAL REGISTER 4 READ
2127
2128   002260   000000                   S6LOAD::.WORD    0                   ;WORD LOADED INTO REGISTER 6
```

```
2129  002262  000000              S6GOOD::.WORD    0        ,           ;EXPECTED REGISTER 6 CONTENTS ON READ
2130  002264  000000              S6MASK::.WORD    0                    ;REGISTER 6 MASK WORD
2131  002266  000000              S6READ::.WORD    0                    ;ACTUAL REGISTER 6 READ
2132  002270  000000              S6BAD:: .WORD    0                    ;REG 6 READ WITH MASK BITS CLEARED
2133
2134
2135                              ;GLOBAL DATA FOR STATE ANALYZER
2136                              ;
2137
2138  002272  000000              E0LOAD::.WORD    0                    ;WORD LOADED INTO REGISTER 0
2139  002274  000000              E0GOOD::.WORD    0                    ;EXPECTED REG 0
2140  002276  000000              E0READ::.WORD    0                    ;ACTUAL REG 0 READ
2141
2142  002300  000000              E2LOAD::.WORD    0                    ;WORD LOADED INTO REGISTER 2
2143  002302  000000              E2READ::.WORD    0                    ;ACTUAL REGISTER 2 READ
2144
2145  002304  000000              E4LOAD::.WORD    0                    ;WORD LOADED INTO REGISTER 4
2146  002306  000000              E4GOOD::.WORD    0                    ;EXPECTED REGISTER 4 DATA
2147  002310  000000              E4MASK::.WORD    0                    ;REGISTER 4 MASK WORD
2148  002312  000000              E4READ::.WORD    0                    ;ACTUAL REGISTER 4 READ
2149  002314  000000              E4BAD:: .WORD    0                    ;REG 4 READ WITH MASKED BITS CLEARED
2150
2151  002316  000000              E6LOAD::.WORD    0                    ;WORD LOADED INTO REGISTER 6
2152  002320  000000              E6MASK::.WORD    0                    ;REGISTER 6 MASK WORD
2153  002322  000000              E6READ::.WORD    0                    ;REG 6 READ WITH MASKED BITS CLEARED
2154
2155
2156                              ;GLOBAL DATA FOR TARGET EMULATOR
2157                              ;
2158
2159  002324  000000              T0LOAD::.WORD    0                    ;WORD LOADED INTO REGISTER 0
2160  002326  000000              T0GOOD::.WORD    0                    ;EXPECTED REG 0
2161  002330  000000              T0MASK::.WORD    0                    ;BITS TO BE IGNORED ON COMPARE
2162  002332  000000              T0READ::.WORD    0                    ;DATA READ MASKED WITH T0MASK
2163
2164  002334  000000              T2LOAD::.WORD    0                    ;WORD LOADED INTO REGISTER 2
2165  002336  000000              T2READ::.WORD    0                    ;ACTUAL REG 2 READ
2166
2167  002340  000000              T4LOAD::.WORD    0                    ;WORD LOADED INTO REGISTER 4
2168  002342  000000              T4GOOD::.WORD    0                    ;EXPECTED DATA FROM REGISTER 4
2169  002344  000000              T4READ::.WORD    0                    ;DATA READ FROM REGISTER 4
2170
2171  002346  000000              T6LOAD::.WORD    0                    ;WORD LOADED INTO REGISTER 6
2172  002350  000000              T6READ::.WORD    0                    ;ACTUAL REGISTER 6 READ
2173  002352  000000              T6MASK::.WORD    0                    ;BITS TO BE IGNORED
```

```
2174                                    .SBTTL   GLOBAL TEXT SECTION
2175
2176                                    ;++
2177                                    ; THE GLOBAL TEXT SECTION CONTAINS FORMAT STATEMENTS,
2178                                    ; MESSAGES, AND ASCII INFORMATION THAT ARE USED IN
2179                                    ; MORE THAN ONE TEST.
2180                                    ;--
2181
2182                                    ;
2183                                    ; NAMES OF DEVICES SUPPORTED BY PROGRAM
2184                                    ;
2185    002354                                  DEVTYP   <MDE/T-11>
2186    002354                          L$DVTYP::
2187    002354   042115  027505  026524         .ASCIZ   %MDE/T-11%
2188    002362   030461    000                  .ASCIZ   %MDE/T-11%
2189             002366                          .EVEN
2190
2191
2192                                    ; TEST DESCRIPTION
2193                                    ;
2194    002366                                  DESCRIPT         <SYSTEM BUS DIAG.>
2195    002366                          L$DESC::
2196    002366   054523  052123  046505         .ASCIZ   /SYSTEM BUS DIAG./
2197    002374   041040  051525  042040
2198    002402   040511  027107   000
2199             002410                          .EVEN
2200
2201
2202                                    ;**********************************************************************
2203                                    ;
2204                                    ;     ERROR MESSAGES FOR MEMORY SIMULATOR MODULE
2205                                    ;
2206                                    ;**********************************************************************
2207
2208
2209                                    ;
2210                                    ;CONTROL REGISTER 0 ERROR MESSAGES
2211                                    ;
2212
2213                                    ;
2214                                    ;CONTROL REGISTER 2 ERROR MESSAGES
2215                                    ;
2216
2217    002410   042524  052040  020117  TEMSA1::.ASCIZ  /TE TO MS ADDRESS BUS ERROR - MSAD 17:16/
2218    002416   051515  040440  042104
2219    002424   042522  051523  041040
2220    002432   051525  042440  051122
2221    002440   051117  026440  046440
2222    002446   040523  020104  033461
2223    002454   030472  000066
2224    002460   040515  020120  051120  MSGMPL::.ASCIZ  /MAP PROTECT LOGIC ERROR/
2225    002466   052117  041505  020124
2226    002474   047514  044507  020103
2227    002502   051105  047522  000122
2228
2229                                    ;
```

```
2230                                              ;CONTROL REGISTER 4 ERROR MESSAGES
2231                                              ;
2232
2233    002510    051515    042101    030440    MSADRG::.ASCIZ  /MSAD 15:0 REG ERROR/
2234    002516    035065    020060    042522
2235    002524    020107    051105    047522
2236    002532    000122
2237    002534    042524    052040    020117    TEMSAD::.ASCIZ  /TE TO MS ADDRESS BUS ERROR - MSAD 15:0/
2238    002542    051515    040440    042104
2239    002550    042522    051523    041040
2240    002556    051525    042440    051122
2241    002564    051117    026440    046440
2242    002572    040523    020104    032461
2243    002600    030072       000
2244
2245
2246                                              ;CONTROL REGISTER 6 ERROR MESSAGES
2247                                              ;
2248
2249    002603       104    052101    020101    MSGMP:: .ASCIZ  /DATA ERROR IN MAP PROTECT RAM/
2250    002610    051105    047522    020122
2251    002616    047111    046440    050101
2252    002624    050040    047522    042524
2253    002632    052103    051040    046501
2254    002640       000
2255    002641       104    052101    020101    MSGMS0::.ASCIZ  /DATA ERROR IN MODULE SELECT RAM 0/
2256    002646    051105    047522    020122
2257    002654    047111    046440    042117
2258    002662    046125    020105    042523
2259    002670    042514    052103    051040
2260    002676    046501    030040       000
2261    002703       104    052101    020101    MSGMS1::.ASCIZ  /DATA ERROR IN MODULE SELECT RAM 1/
2262    002710    051105    047522    020122
2263    002716    047111    046440    042117
2264    002724    046125    020105    042523
2265    002732    042514    052103    051040
2266    002740    046501    030440       000
2267    002745       104    052101    020101    MSGMSR::.ASCIZ  /DATA ERROR IN MEMORY SIMULATOR RAM/
2268    002752    051105    047522    020122
2269    002760    047111    046440    046505
2270    002766    051117    020131    044523
2271    002774    052515    040514    047524
2272    003002    020122    040522    000115
```

```
2273                                      ;*************************************************************************
2274
2275                                      ;          ERROR MESSAGES FOR STATE ANALYZER MODULE
2276
2277                                      ;*************************************************************************
2278
2279
2280
2281                                      ;CONTROL REGISTER 0 ERROR MESSAGES
2282                                      ;
2283
2284    003010  042103  046101  030440    CDALRG::.ASCIZ  /CDAL 15:0 REG ERROR/
2285    003016  035065  020060  042522
2286    003024  020107  051105  047522
2287    003032  000122
2288
2289
2290                                      ;CONTROL REGISTER 2 ERROR MESSAGES
2291                                      ;
2292
2293    003034  042120  046101  033440    PDALRG::.ASCIZ  /PDAL 7:0 REG ERROR/
2294    003042  030072  051040  043505
2295    003050  042440  051122  051117
2296    003056     000
2297
2298
2299                                      ;CONTROL REGISTER 4 ERROR MESSAGES
2300                                      ;
2301
2302    003057     117  020122  051101    ORDATA::.ASCIZ  /OR ARRAY RAM DATA ERROR - ORO 7:0/
2303    003064  040522  020131  040522
2304    003072  020115  040504  040524
2305    003100  042440  051122  051117
2306    003106  026440  047440  047522
2307    003114  033440  030072     000
2308    003121     106  051525  033514    FUSL7:: .ASCIZ  /FUSL7 FLIP-FLOP - OR ARRAY RAM DATA ERROR/
2309    003126  043040  044514  026520
2310    003134  046106  050117  026440
2311    003142  047440  020122  051101
2312    003150  040522  020131  040522
2313    003156  020115  040504  040524
2314    003164  042440  051122  051117
2315    003172     000
2316
2317
2318                                      ;CONTROL REGISTER 6 ERROR MESSAGES
2319                                      ;
2320
2321    003173     124  020105  047524    TEEDAD::.ASCIZ  /TE TO SA ADDRESS BUS ERROR - TRDI 15:0/
2322    003200  051440  020101  042101
2323    003206  051104  051505  020123
2324    003214  052502  020123  051105
2325    003222  047522  02012_  020055
2326    003230  051124  044504  030440
2327    003236  035065  000060
2328    003242  042524  052040  020117    TEEDA1::.ASCIZ  /TE TO SA - XSEL1, EDSELO, ADDR 17:16 + BTS 3:0 ERROR - TRDI 47:32/
```

```
2329   003250   040523   026440   054040
2330   003256   042523   030514   020054
2331   003264   042105   042523   030114
2332   003272   020054   042101   051104
2333   003300   030440   035067   033061
2334   003306   025440   041040   051524
2335   003314   031440   030072   042440
2336   003322   051122   051117   026440
2337   003330   052040   042122   020111
2338   003336   033464   031472   000062
2339   003344   042524   041440   046124   TEEDCT::.ASCIZ  /TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:40 ERROR/
2340   003352   041040   051525   033440
2341   003360   030072   052040   020117
2342   003366   040523   052040   042122
2343   003374   020111   052502   020123
2344   003402   044502   051524   032040
2345   003410   035067   030064   042440
2346   003416   051122   051117      000
2347
2348   003423      115   020123   040522   MSEDDE::.ASCIZ  /MS RAM DATA TO SA TRDI BUS BITS 31:16 ERROR/
2349   003430   020115   040504   040524
2350   003436   052040   020117   040523
2351   003444   052040   042122   020111
2352   003452   052502   020123   044502
2353   003460   051524   031440   035061
2354   003466   033061   042440   051122
2355   003474   051117      000
2356   003477      124   040522   042503   TRADRS::.ASCIZ  /TRACE RAM ADDRESS REG ERROR - TRAD 10:0/
2357   003504   051040   046501   040440
2358   003512   042104   042522   051523
2359   003520   051040   043505   042440
2360   003526   051122   051117   026440
2361   003534   052040   040522   020104
2362   003542   030061   030072      000
2363   003547      117   020122   042101   ORADER::.ASCIZ  /OR ADDRESS REG ERROR - ORAD 3:0/
2364   003554   051104   051505   020123
2365   003562   042522   020107   051105
2366   003570   047522   020122   020055
2367   003576   051117   042101   031440
2368   003604   030072      000
2369   003607      106   051525   020114   FUSL30::.ASCIZ  /FUSL 3:0 FLIP-FLOP ERROR/
2370   003614   035063   020060   046106
2371   003622   050111   043055   047514
2372   003630   020120   051105   047522
2373   003636   000122
```

```
2374                                    ;************************************************************************
2375
2376                                    ;            ERROR MESSAGES FOR TARGET EMULATOR MODULE
2377
2378                                    ;************************************************************************
2379
2380                                    ;
2381                                    ;ASCII MESSAGES USED BY ERROR CALLS
2382                                    ;
2383                                    ;CONTROL REGISTER 0 ERROR MESSAGES
2384
2385    003640  042107  046101  030440  GDALRG::.ASCIZ  /GDAL 15:0 REG ERROR/
2386    003646  035065  020060  042522
2387    003654  020107  051105  047522
2388    003662  000122
2389
2390                                    ;CONTROL REGISTER 2 ERROR MESSAGES
2391
2392    003664  042101  046101  030440  ADALRG::.ASCIZ  /ADAL 15:0 REG ERROR/
2393    003672  035065  020060  042522
2394    003700  020107  051105  047522
2395    003706  000122
2396
2397                                    ;CONTROL REGISTER 4 ERROR MESSAGES
2398
2399    003710  042126  046101  033440  VDALRG::.ASCIZ  /VDAL 7:0 OR PAUSE STATE MACHINE ERROR/
2400    003716  030072  047440  020122
2401    003724  040520  051525  020105
2402    003732  052123  052101  020105
2403    003740  040515  044103  047111
2404    003746  020105  051105  047522
2405    003754  000122
2406
2407                                    ;CONTROL REGISTER 6 ERROR MESSAGES
2408
2409    003756  042110  046101  030440  HDALRG::.ASCIZ  /HDAL 15:0 REG ERROR/
2410    003764  035065  020060  042522
2411    003772  020107  051105  047522
2412    004000  000122
2413    004002  051115  030440  035065  MODREG::.ASCIZ  /MR 15:0 REG ERROR/
2414    004010  020060  042522  020107
2415    004016  051105  047522  000122
2416    004024  042106  046101  033440  FDALRG::.ASCIZ  /FDAL 7:0 REG ERROR/
2417    004032  030072  051040  043505
2418    004040  042440  051122  051117
2419    004046     000
2420    004047     105  040517  020111  EOAIFD::.ASCIZ  /EOAI 7:0 OR FDAL 7:0 REG ERROR/
2421    004054  035067  020060  051117
2422    004062  043040  040504  020114
2423    004070  035067  020060  042522
2424    004076  020107  051105  047522
2425    004104  000122
2426    004106  052103  020114  035067  CTLFDL::.ASCIZ  /CTL 7:0 OR FDAL 7:0 REG ERROR/
2427    004114  020060  051117  043040
2428    004122  040504  020114  035067
2429    004130  020060  042522  020107
```

```
2430  004136  051105  047522  000122
2431  004144  044504  043501  040440   ADDRRG::.ASCIZ  /DIAG ADDR 15:0 REG ERROR/
2432  004152  042104  020122  032461
2433  004160  030072  051040  043505
2434  004166  042440  051122  051117
2435  004174    000
2436  004175    106   051117  042503   FJADRG::.ASCIZ  /FORCE JUMP ADDRESS READBACK REG ERROR/
2437  004202  045040  046525  020120
2438  004210  042101  051104  051505
2439  004216  020123  042522  042101
2440  004224  040502  045503  051040
2441  004232  043505  042440  051122
2442  004240  051117    000
2443  004243    115   020123  040522   MSTEDE::.ASCIZ  /MS RAM DATA TO TE EODAL BUS ERROR VIA SYSTEM DATA BUS/
2444  004250  020115  040504  040524
2445  004256  052040  020117  042524
2446  004264  042440  042117  046101
2447  004272  041040  051525  042440
2448  004300  051122  051117  053040
2449  004306  040511  051440  051531
2450  004314  042524  020115  040504
2451  004322  040524  041040  051525
2452  004330    000
2453  004331    115   020123  040522   MSTEEI::.ASCIZ  /MS RAM DATA TO TE EIDAL BUS ERROR VIA EODAL + SYSTEM BUS/
2454  004336  020115  040504  040524
2455  004344  052040  020117  042524
2456  004352  042440  042111  046101
2457  004360  041040  051525  042440
2458  004366  051122  051117  053040
2459  004374  040511  042440  042117
2460  004402  046101  025440  051440
2461  004410  051531  042524  020115
2462  004416  052502  000123
2463  004422  051515  051040  046501   MSTETD::.ASCIZ  /MS RAM DATA TO TE EIDAL BUS ERROR VIA TDAL BUS LATCHES/
2464  004430  042040  052101  020101
2465  004436  047524  052040  020105
2466  004444  044505  040504  020114
2467  004452  052502  020123  051105
2468  004460  047522  020122  044526
2469  004466  020101  042124  046101
2470  004474  041040  051525  046040
2471  004502  052101  044103  051505
2472  004510    000
2473  004511    115   046505  051102   NOINT:: .ASCIZ  /MEMBRK H FAILED TO SET BREAK FLIP-FLOP OR FAILED TO INTERRUPT/
2474  004516  020113  020110  040506
2475  004524  046111  042105  052040
2476  004532  020117  042523  020124
2477  004540  051102  040505  020113
2478  004546  046106  050111  043055
2479  004554  047514  020120  051117
2480  004562  043040  044501  042514
2481  004570  020104  047524  044440
2482  004576  052116  051105  052522
2483  004604  052120    000
2484  004607    106   040504  020114   FDEODL::.ASCIZ  /FDAL REG 7:2 TO EODAL BUS ERROR/
2485  004614  042522  020107  035067
```

```
2486  004622  020062  047524  042440
2487  004630  042117  046101  041040
2488  004636  051525  042440  051122
2489  004644  051117     000
2490  004647     106  040504  020114    FDEIDL::.ASCIZ  /FDAL REG 7:2 TO EIDAL BUS ERROR/
2491  004654  042522  020107  035067
2492  004662  020062  047524  042440
2493  004670  042111  046101  041040
2494  004676  051525  042440  051122
2495  004704  051117     000
2496  004707     106  040504  020114    FDTDEI::.ASCIZ   /FDAL REG 7:2 TO TDAL LATCHES TO EIDAL BUS ERROR/
2497  004714  042522  020107  035067
2498  004722  020062  047524  052040
2499  004730  040504  020114  040514
2500  004736  041524  042510  020123
2501  004744  047524  042440  042111
2502  004752  046101  041040  051525
2503  004760  042440  051122  051117
2504  004766     000
2505          004770                             .EVEN
```

```
2506
2507                              ;*****************************************************************************
2508                              ;
2509                              ; FORMAT STATEMENTS USED IN PRINT CALLS
2510                              ;
2511                              ;*****************************************************************************
2512
2513   004770  040445  047503  052116  EMSGR0::.ASCIZ  /%ACONTROL REG 0 ERROR%N/
2514   004776  047522  020114  042522
2515   005004  020107  020060  051105
2516   005012  047522  022522  000116
2517   005020  040445  047503  052116  EMSGR2::.ASCIZ  /%ACONTROL REG 2 ERROR%N/
2518   005026  047522  020114  042522
2519   005034  020107  020062  051105
2520   005042  047522  022522  000116
2521   005050  040445  047503  052116  EMSGR4::.ASCIZ  /%ACONTROL REG 4 ERROR%N/
2522   005056  047522  020114  042522
2523   005064  020107  020064  051105
2524   005072  047522  022522  000116
2525   005100  040445  047503  052116  EMSGR6::.ASCIZ  /%ACONTROL REG 6 ERROR%N/
2526   005106  047522  020114  042522
2527   005114  020107  020066  051105
2528   005122  047522  022522  000116
2529   005130  040445  042522  030107  REG0EQ::.ASCIZ  /%AREG0 = /
2530   005136  036440  000040
2531   005142  040445  042522  031107  REG2EQ::.ASCIZ  /%AREG2 = /
2532   005150  036440  000040
2533   005154  040445  042522  032107  REG4EQ::.ASCIZ  /%AREG4 = /
2534   005162  036440  000040
2535   005166  040445  042522  033107  REG6EQ::.ASCIZ  /%AREG6 = /
2536   005174  036440  000040
2537
2538                              ;
2539                              ;FORMAT STATEMENTS FOR REPORTING ERROR INFORMATION
2540                              ;
2541
2542   005200  040445  047514  042101  FSLR::  .ASCIZ  /%ALOAD: %06%S1%AREAD: %06%N/
2543   005206  020072  047445  022466
2544   005214  030523  040445  042522
2545   005222  042101  020072  047445
2546   005230  022466  000116
2547   005234  040445  047514  042101  FSLGB:: .ASCIZ  /%ALOAD: %06%S1%AGOOD: %06%S1%AREAD: %06%N/
2548   005242  020072  047445  022466
2549   005250  030523  040445  047507
2550   005256  042117  020072  047445
2551   005264  022466  030523  040445
2552   005272  042522  042101  020072
2553   005300  047445  022466  000116
2554
2555                                      .EVEN
```

B 5

GLOBAL AREAS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 53
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR MEMORY SIMULATOR MODULE   SEQ 0053

```
2556                                      .SBTTL  GLOBAL ERROR REPORT SECTION FOR MEMORY SIMULATOR MODULE
2557
2558    005306                            BGNMSG  SOEROR
2559    005306                    SOEROR::
2560    005306  004537  006762            JSR     R5,PRNTBS            ;GO PRINT CONTROL REGISTER THAT FAILED
2561    005312  004770                    .WORD   EMSGR0
2562    005314  004737  005514            JSR     PC,PRNTS0           ;GO PRINT CONTROL REGISTER 0 ERROR INFO
2563    005320                            ENDMSG
2564    005320                    L10002:
2565    005320  104423                    TRAP    C$MSG
2566
2567    005322                            BGNMSG  S2EROR
2568    005322                    S2EROR::
2569    005322  004537  006762            JSR     R5,PRNTBS            ;GO PRINT CONTROL REGISTER THAT FAILED
2570    005326  005020                    .WORD   EMSGR2
2571    005330  004737  005634            JSR     PC,PRNTS2           ;GO PRINT CONTROL REGISTER 2 ERROR INFO
2572    005334                            ENDMSG
2573    005334                    L10003:
2574    005334  104423                    TRAP    C$MSG
2575
2576    005336                            BGNMSG  S4EROR
2577    005336                    S4EROR::
2578    005336  004537  006762            JSR     R5,PRNTBS            ;GO PRINT CONTROL REGISTER THAT FAILED
2579    005342  005050                    .WORD   EMSGR4
2580    005344  004737  005754            JSR     PC,PRNTS4           ;GO PRINT CONTROL REGISTER 4 ERROR INFO
2581    005350                            ENDMSG
2582    005350                    L10004:
2583    005350  104423                    TRAP    C$MSG
2584
2585    005352                            BGNMSG  S6EROR
2586    005352                    S6EROR::
2587    005352  004537  006762            JSR     R5,PRNTBS            ;GO PRINT CONTROL REGISTER THAT FAILED
2588    005356  005100                    .WORD   EMSGR6
2589    005360  004737  006026            JSR     PC,PRNTS6           ;GO PRINT CONTROL REGISTER 6 ERROR INFO
2590    005364                            ENDMSG
2591    005364                    L10005:
2592    005364  104423                    TRAP    C$MSG
2593
2594    005366                            BGNMSG  S02ERR
2595    005366                    S02ERR::
2596    005366  004537  006762            JSR     R5,PRNTBS            ;GO PRINT CONTROL REGISTER THAT FAILED
2597    005372  005020                    .WORD   EMSGR2
2598    005374  004737  005514            JSR     PC,PRNTS0           ;GO PRINT CONTROL REGISTER 0 ERROR INFO
2599    005400  004737  005634            JSR     PC,PRNTS2           ;GO PRINT CONTROL REGISTER 2 ERROR INFO
2600    005404                            ENDMSG
2601    005404                    L10006:
2602    005404  104423                    TRAP    C$MSG
2603
2604    005406                            BGNMSG  S04ERR
2605    005406                    S04ERR::
2606    005406  004537  006762            JSR     R5,PRNTBS            ;GO PRINT CONTROLREGISTER THAT FAILED
2607    005412  005050                    .WORD   EMSGR4
2608    005414  004737  005514            JSR     PC,PRNTS0           ;GO PRINT CONTROL REGISTER 0 ERROR INFO
2609    005420  004737  005754            JSR     PC,PRNTS4           ;GO PRINT CONTROL REGISTER 4 ERROR INFO
2610    005424                            ENDMSG
2611    005424                    L10007:
```

C 5

GLOBAL AREAS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 54
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR MEMORY SIMULATOR MODULE   SEQ 0054

```
2612   005424  104423                        TRAP    C$MSG
2613
2614   005426                                BGNMSG  SOALLR
2615   005426                        SOALLR::
2616   005426  004537  006762                JSR     R5,PRNTBS              ;GO PRINT CONTROL REGISTER THAT FAILED
2617   005432  004770                        .WORD   EMSGR0
2618   005434  004737  005472                JSR     PC,PRNTAL              ;GO PRINT ALL CONTROL REGISTER'S INFO
2619   005440                                ENDMSG
2620   005440                        L10010:
2621   005440  104423                        TRAP    C$MSG
2622
2623   005442                                BGNMSG  S2ALLR
2624   005442                        S2ALLR::
2625   0C5442  004537  006762                JSR     R5,PRNTBS              ;GO PRINT CONTROL REGISTER THAT FAILED
2626   005446  005020                        .WORD   EMSGR2
2627   005450  004737  005472                JSR     PC,PRNTAL              ;GO PRINT ALL CONTROL REGISTER'S INFO
2628   005454                                ENDMSG
2629   005454                        L10011:
2630   005454  104423                        TRAP    C$MSG
2631
2632   005456                                BGNMSG  S6ALLR
2633   005456                        S6ALLR::
2634   005456  004537  006762                JSR     R5,PRNTBS              ;GO PRINT CONTROL REGISTER THAT FAILED
2635   005462  005100                        .WORD   EMSGR6
2636   005464  004737  005472                JSR     PC,PRNTAL              ;GO PRINT ALL CONTROL REGISTER'S INFO
2637   005470                                ENDMSG
2638   005470                        L10012:
2639   005470  104423                        TRAP    C$MSG
2640
2641
2642                                  ;ROUTINE TO PRINT ALL CONTROL REGISTERS ERROR INFORMATION
2643                                  ;
2644
2645   005472  004737  005514        PRNTAL::JSR     PC,PRNTS0              ;GO PRINT CONTROL REGISTER 0 ERROR INFO
2646   005476  004737  005634                JSR     PC,PRNTS2              ;GO PRINT CONTROL REGISTER 2 ERROR INFO
2647   005502  004737  005754                JSR     PC,PRNTS4              ;GO PRINT CONTROL REGISTER 4 ERROR INFO
2648   005506  004737  006026                JSR     PC,PRNTS6              ;GO PRINT CONTROL REGISTER 6 ERROR INFO
2649   005512  000207                        RTS     PC                     ;RETURN BACK TO THE ERROR ROUTINE
2650
2651                                  ;PRINT CONTROL REGISTER 0 ERROR INFORMATION
2652
2653   005514                        PRNTS0::PRINTX  #REG0EQ
2654   005514  012746  005130                MOV     #REG0EQ,-(SP)
2655   005520  012746  000001                MOV     #1,-(SP)
2656   005524  010600                        MOV     SP,R0
2657   005526  104415                        TRAP    C$PNTX
2658   005530  062706  000004                ADD     #4,SP
2659   005534  023737  002234  002236        CMP     SOLOAD,SOGOOD          ;CHECK LOADED DIFFERENT THEN EXPECTED
2660   005542  001417                        BEQ     1$                     ;IF NOT THEN PRINT "LOAD" AND "READ"
2661   005544                                PRINTX  #FSLGB,SOLOAD,SOGOOD,SOREAD
2662   005544  013746  002242                MOV     SOREAD,-(SP)
2663   005550  013746  002236                MOV     SOGOOD,-(SP)
2664   005554  013746  002234                MOV     SOLOAD,-(SP)
2665   005560  012746  005234                MOV     #FSLGB,-(SP)
2666   005564  012746  000004                MOV     #4,-(SP)
2667   005570  010600                        MOV     SP,R0
```

D 5

GLOBAL AREAS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 55
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR MEMORY SIMULATOR MODULE   SEQ 0055

```
2668   005572  104415                    TRAP     C$PNTX
2669   005574  062706   000012           ADD      #12,SP
2670   005600  000414                    BR       2$
2671   005602                   1$:      PRINTX   #FSLR,S0LOAD,S0READ
2672   005602  013746   002242           MOV      S0READ,-(SP)
2673   005606  013746   002234           MOV      S0LOAD,-(SP)
2674   005612  012746   005200           MOV      #FSLR,-(SP)
2675   005616  012746   000003           MOV      #3,-(SP)
2676   005622  010600                    MOV      SP,R0
2677   005624  104415                    TRAP     C$PNTX
2678   005626  062706   000010           ADD      #10,SP
2679   005632  000207           2$:      RTS      PC
2680
2681                            ;PRINT CONTROL REGISTER 2 ERROR INFORMATION
2682
2683   005634                   PRNTS2::PRINTX  #REG2EQ
2684   005634  012746   005142           MOV      #REG2EQ,-(SP)
2685   005640  012746   000001           MOV      #1,-(SP)
2686   005644  010600                    MOV      SP,R0
2687   005646  104415                    TRAP     C$PNTX
2688   005650  062706   000004           ADD      #4,SP
2689   005654  023737   002244  002246   CMP      S2LOAD,S2GOOD       ;CHECK IF LOADED DIFFERENT THEN EXPECTED
2690   005662  001417                    BEQ      1$                  ;IF NOT THEN PRINT "LOAD" AND "READ"
2691   005664                            PRINTX   #FSLGB,S2LOAD,S2GOOD,S2READ
2692   005664  013746   002252           MOV      S2READ,-(SP)
2693   005670  013746   002246           MOV      S2GOOD,-(SP)
2694   005674  013746   002244           MOV      S2LOAD,-(SP)
2695   005700  012746   005234           MOV      #FSLGB,-(SP)
2696   005704  012746   000004           MOV      #4,-(SP)
2697   005710  010600                    MOV      SP,R0
2698   005712  104415                    TRAP     C$PNTX
2699   005714  062706   000012           ADD      #12,SP
2700   005720  000414                    BR       2$
2701   005722                   1$:      PRINTX   #FSLR,S2LOAD,S2READ
2702   005722  013746   002252           MOV      S2READ,-(SP)
2703   005726  013746   002244           MOV      S2LOAD,-(SP)
2704   005732  012746   005200           MOV      #FSLR,-(SP)
2705   005736  012746   000003           MOV      #3,-(SP)
2706   005742  010600                    MOV      SP,R0
2707   005744  104415                    TRAP     C$PNTX
2708   005746  062706   000010           ADD      #10,SP
2709   005752  000207           2$:      RTS      PC
2710
2711                            ;PRINT CONTROL REGISTER 4 ERROR INFORMATION
2712
2713   005754                   PRNTS4::PRINTX  #REG4EQ
2714   005754  012746   005154           MOV      #REG4EQ,-(SP)
2715   005760  012746   000001           MOV      #1,-(SP)
2716   005764  010600                    MOV      SP,R0
2717   005766  104415                    TRAP     C$PNTX
2718   005770  062706   000004           ADD      #4,SP
2719   005774                            PRINTX   #FSLR,S4LOAD,S4READ
2720   005774  013746   002256           MOV      S4READ,-(SP)
2721   006000  013746   002254           MOV      S4LOAD,-(SP)
2722   006004  012746   005200           MOV      #FSLR,-(SP)
2723   006010  012746   000003           MOV      #3,-(SP)
```

```
2724  006014  010600                    MOV     SP,R0
2725  006016  104415                    TRAP    C$PNTX
2726  006020  062706  000010            ADD     #10,SP
2727  006024  000207                    RTS     PC
2728
2729                            ;PRINT CONTROL REGISTER 6 ERROR INFORMATION
2730
2731  006026                    PRNTS6::PRINTX  #REG6EQ
2732  006026  012746  005166            MOV     #REG6EQ,-(SP)
2733  006032  012746  000001            MOV     #1,-(SP)
2734  006036  010600                    MOV     SP,R0
2735  006040  104415                    TRAP    C$PNTX
2736  006042  062706  000004            ADD     #4,SP
2737  006046  023737  002260  002262    CMP     S6LOAD,S6GOOD          ;CHECK IF LOADED DIFFERENT THEN EXPECTED
2738  006054  001417                    BEQ     1$                    ;IF NOT THEN PRINT "LOAD" AND "READ"
2739  006056                    PRINTX  #FSLGB,S6LOAD,S6GOOD,S6BAD
2740  006056  013746  002270            MOV     S6BAD,-(SP)
2741  006062  013746  002262            MOV     S6GOOD,-(SP)
2742  006066  013746  002260            MOV     S6LOAD,-(SP)
2743  006072  012746  005234            MOV     #FSLGB,-(SP)
2744  006076  012746  000004            MOV     #4,-(SP)
2745  006102  010600                    MOV     SP,R0
2746  006104  104415                    TRAP    C$PNTX
2747  006106  062706  000012            ADD     #12,SP
2748  006112  000414                    BR      2$
2749  006114                    1$:     PRINTX  #FSLR,S6LOAD,S6BAD
2750  006114  013746  002270            MOV     S6BAD,-(SP)
2751  006120  013746  002260            MOV     S6LOAD,-(SP)
2752  006124  012746  005200            MOV     #FSLR,-(SP)
2753  006130  012746  000003            MOV     #3,-(SP)
2754  006134  010600                    MOV     SP,R0
2755  006136  104415                    TRAP    C$PNTX
2756  006140  062706  000010            ADD     #10,SP
2757  006144  000207            2$:     RTS     PC
```

F 5

GLOBAL AREAS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 57
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR STATE ANALYZER MODULE   SEQ 0057

```
2758                                     .SBTTL  GLOBAL ERROR REPORT SECTION FOR STATE ANALYZER MODULE
2759
2760  006146                             BGNMSG  EOEROR
2761  006146                     EOEROR::
2762  006146  004537  006762             JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2763  006152  004770                     .WORD   EMSGR0
2764  006154  004737  006302             JSR     PC,PRNTE0               ;GO PRINT CONTROL REGISTER 0 INFO
2765  006160                             ENDMSG
2766  006160                     L10013:
2767  006160  104423                     TRAP    C$MSG
2768
2769  006162                             BGNMSG  E2EROR
2770  006162                     E2EROR::
2771  006162  004537  006762             JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2772  006166  005020                     .WORD   EMSGR2
2773  006170  004737  006422             JSR     PC,PRNTE2               ;GO PRINT CONTROL REGISTER 2 INFO
2774  006174                             ENDMSG
2775  006174                     L10014:
2776  006174  104423                     TRAP    C$MSG
2777
2778  006176                             BGNMSG  E4EROR
2779  006176                     E4EROR::
2780  006176  004537  006762             JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2781  006202  005050                     .WORD   EMSGR4
2782  006204  004737  006260             JSR     PC,PRNTAR               ;GO PRINT ALL CONTROL REGISTERS
2783  006210                             ENDMSG
2784  006210                     L10015:
2785  006210  104423                     TRAP    C$MSG
2786
2787  006212                             BGNMSG  E026ER
2788  006212                     E026ER::
2789  006212  004537  006762             JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2790  006216  005100                     .WORD   EMSGR6
2791  006220  004737  006242             JSR     PC,PR026E               ;GO PRINT CONTROL REG'S 0, 2, AND 6
2792  006224                             ENDMSG
2793  006224                     L10016:
2794  006224  104423                     TRAP    C$MSG
2795
2796  006226                             BGNMSG  E6ALLR
2797  006226                     E6ALLR::
2798  006226  004737  006762             JSR     PC,PRNTBS               ;GO PRINT CONTROL REGISTER THAT FAILED
2799  006232  005100                     .WORD   EMSGR6
2800  006234  004737  006260             JSR     PC,PRNTAR               ;GO PRINT ALL CONTROL REGISTER'S INFO
2801  006240                             ENDMSG
2802  006240                     L10017:
2803  006240  104423                     TRAP    C$MSG
2804
2805                             ;ROUTINE TO PRINT CONTROL REGISTER 0, 2, AND 6 ERROR INFORMATION
2806
2807  006242  004737  006302     PR026E::JSR     PC,PRNTE0               ;GO PRINT CONTROL REGISTER 0 INFO
2808  006246  004737  006422             JSR     PC,PRNTE2               ;GO PRINT CONTROL REGISTER 2 INFO
2809  006252  004737  006614             JSR     PC,PRNTE6               ;GO PRINT CONTROL REGISTER 6 INFO
2810  006256  000207                     RTS     PC
2811
2812                             ;ROUTINE TO PRINT ALL THE CONTROL REGISTERS ERROR INFORMATION
2813
```

G 5

GLOBAL AREAS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 58
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR STATE ANALYZER MODULE   SEQ 0058

```
2814  006260  004737  006302          PRNTAR::JSR     PC,PRNTE0                      ;GO PRINT CONTROL REGISTER 0 INFO
2815  006264  004737  006422                   JSR     PC,PRNTE2                      ;GO PRINT CONTROL REGISTER 2     0
2816  006270  004737  006474                   JSR     PC,PRNTE4                      ;GO PRINT CONTROL REGISTER 4
2817  006274  004737  006614                   JSR     PC,PRNTE6                      ;GO PRINT CONTROL REGISTER 6     0
2818  006300  000207                   RTS     PC
2819
2820                                    ;PRINT CONTROL REGISTER 0 ERROR INFORMATION
2821
2822  006302                           PRNTE0::PRINTX  #REG0EQ
2823  006302  012746  005130                   MOV     #REG0EQ,-(SP)
2824  006306  012746  000001                   MOV     #1,-(SP)
2825  006312  010600                            MOV     SP,R0
2826  006314  104415                            TRAP    C$PNTX
2827  006316  062706  000004                    ADD     #4,SP
2828  006322  023737  002272  002274            CMP     EOLOAD,EOGOOD                  ;CHECK IF LOADED DIFFERENT THEN EXPECTED
2829  006330  001417                            BEQ     1$                            ;IF NOT PRINT "LOAD" AND "READ:
2830  006332                                    PRINTX  #FSLGB,EOLOAD,EOGOOD,EOREAD
2831  006332  013746  002276                    MOV     EOREAD,-(SP)
2832  006336  013746  002274                    MOV     EOGOOD,-(SP)
2833  006342  013746  002272                    MOV     EOLOAD,-(SP)
2834  006346  012746  005234                    MOV     #FSLGB,-(SP)
2835  006352  012746  000004                    MOV     #4,-(SP)
2836  006356  010600                            MOV     SP,R0
2837  006360  104415                            TRAP    C$PNTX
2838  006362  062706  000012                    ADD     #12,SP
2839  006366  000414                            BR      2$
2840  006370                           1$:      PRINTX  #FSLR,EOLOAD,EOREAD
2841  006370  013746  002276                    MOV     EOREAD,-(SP)
2842  006374  013746  002272                    MOV     EOLOAD,-(SP)
2843  006400  012746  005200                    MOV     #FSLR,-(SP)
2844  006404  012746  000003                    MOV     #3,-(SP)
2845  006410  010600                            MOV     SP,R0
2846  006412  104415                            TRAP    C$PNTX
2847  006414  062706  000010                    ADD     #10,SP
2848  006420  000207                   2$:      RTS     PC
2849
2850                                    ;PRINT CONTROL REGISTER 2 ERROR INFORMATION
2851
2852  006422                           PRNTE2::PRINTX  #REG2EQ
2853  006422  012746  005142                    MOV     #REG2EQ,-(SP)
2854  006426  012746  000001                    MOV     #1,-(SP)
2855  006432  010600                            MOV     SP,R0
2856  006434  104415                            TRAP    C$PNTX
2857  006436  062706  000004                    ADD     #4,SP
2858  006442                                    PRINTX  #FSLR,E2LOAD,E2READ
2859  006442  013746  002302                    MOV     E2READ,-(SP)
2860  006446  013746  002300                    MOV     E2LOAD,-(SP)
2861  006452  012746  005200                    MOV     #FSLR,-(SP)
2862  006456  012746  000003                    MOV     #3,-(SP)
2863  006462  010600                            MOV     SP,R0
2864  006464  104415                            TRAP    C$PNTX
2865  006466  062706  000010                    ADD     #10,SP
2866  006472  000207                            RTS     PC
2867
2868                                    ;PRINT CONTROL REGISTER 4 ERROR INFORMATION
2869
```

```
2870  006474                    PRNTE4::PRINTX  #REG4EQ
2871  006474  012746  005154            MOV     #REG4EQ,-(SP)
2872  006500  012746  000001            MOV     #1,-(SP)
2873  006504  010600                    MOV     SP,R0
2874  006506  104415                    TRAP    C$PNTX
2875  006510  062706  000004            ADD     #4,SP
2876  006514  023737  002304  002306    CMP     E4LOAD,E4GOOD          ;CHECK IF LOADED DIFFERENT THEN EXPECTED
2877  006522  001417                    BEQ     1$                    ;IF NOT THEN PRINT ''LOAD'' AND ''READ''
2878  006524                            PRINTX  #FSLGB,E4LOAD,E4GOOD,E4BAD
2879  006524  013746  002314            MOV     E4BAD,-(SP)
2880  006530  013746  002306            MOV     E4GOOD,-(SP)
2881  006534  013746  002304            MOV     E4LOAD,-(SP)
2882  006540  012746  005234            MOV     #FSLGB,-(SP)
2883  006544  012746  000004            MOV     #4,-(SP)
2884  006550  010600                    MOV     SP,R0
2885  006552  104415                    TRAP    C$PNTX
2886  006554  062706  000012            ADD     #12,SP
2887  006560  000414                    BR      2$
2888  006562                    1$:     PRINTX  #FSLR,E4LOAD,E4BAD
2889  006562  013746  002314            MOV     E4BAD,-(SP)
2890  006566  013746  002304            MOV     E4LOAD,-(SP)
2891  006572  012746  005200            MOV     #FSLR,-(SP)
2892  006576  012746  000003            MOV     #3,-(SP)
2893  006602  010600                    MOV     SP,R0
2894  006604  104415                    TRAP    C$PNTX
2895  006606  062706  000010            ADD     #10,SP
2896  006612  000207            2$:     RTS     PC
2897
2898                            ;PRINT CONTROL REGISTER 6 ERROR INFORMATION
2899
2900  006614                    PRNTE6::PRINTX  #REG6EQ
2901  006614  012746  005166            MOV     #REG6EQ,-(SP)
2902  006620  012746  000001            MOV     #1,-(SP)
2903  006624  010600                    MOV     SP,R0
2904  006626  104415                    TRAP    C$PNTX
2905  006630  062706  000004            ADD     #4,SP
2906  006634                            PRINTX  #FSLR,E6LOAD,E6READ
2907  006634  013746  002322            MOV     E6READ,-(SP)
2908  006640  013746  002316            MOV     E6LOAD,-(SP)
2909  006644  012746  005200            MOV     #FSLR,-(SP)
2910  006650  012746  000003            MOV     #3,-(SP)
2911  006654  010600                    MOV     SP,R0
2912  006656  104415                    TRAP    C$PNTX
2913  006660  062706  000010            ADD     #10,SP
2914  006664  000207                    RTS     PC
2915
```

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GLOBAL AREAS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 60
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR TARGET EMULATOR MODULE   SEQ 0060

```
2916                                    .SBTTL   GLOBAL ERROR REPORT SECTION FOR TARGET EMULATOR MODULE
2917
2918                                    ;++
2919                                    ; THE GLOBAL ERROR REPORT SECTION CONTAINS MESSAGE PRINTING AREAS
2920                                    ; USED BY MORE THAN TEST TO OUTPUT ADDITIONAL ERROR INFORMATION.  PRINTB
2921                                    ; (BASIC) AND PRINTX (EXTENDED) CALLS ARE USED TO CALL PRINT SERVICES.
2922                                    ;--
2923
2924
2925   006666                                   BGNMSG   TOEROR
2926   006666                           TOEROR::
2927   006666  004537  006762                   JSR      R5,PRNTBS                 ;GO PRINT CONTROL REG THAT FAILED
2928   006672  004770                            .WORD    EMSGRO
2929   006674  004737  007054                    JSR      PC,PRNTTO                 ;GO PRINT CONTROL REGISTER 0 INFO
2930   006700                                    ENDMSG
2931   006700                           L10020:
2932   006700  104423                            TRAP     C$MSG
2933
2934   006702                                   BGNMSG   T2EROR
2935   006702                           T2EROR::
2936   006702  004537  006762                   JSR      R5,PRNTBS                 ;GO PRINT CONTROL REG THAT FAILED
2937   006706  005020                            .WORD    EMSGR2
2938   006710  004737  007174                    JSR      PC,PRNTT2                 ;GO PRINT CONTROL REGISTER 2 INFO
2939   006714                                    ENDMSG
2940   006714                           L10021:
2941   006714  104423                            TRAP     C$MSG
2942
2943   006716                                   BGNMSG   T4EROR
2944   006716                           T4EROR::
2945   006716  004537  006762                   JSR      R5,PRNTBS                 ;GO PRINT CONTROL REG THAT FAILED
2946   006722  005050                            .WORD    EMSGR4
2947   006724  004737  007246                    JSR      PC,PRNTT4                 ;GO PRINT CONTROL REGISTER 4 INFO
2948   006730                                    ENDMSG
2949   006730                           L10022:
2950   006730  104423                            TRAP     C$MSG
2951
2952   006732                                   BGNMSG   TO6ERR
2953   006732                           TO6ERR::
2954   006732  004537  006762                   JSR      R5,PRNTBS                 ;GO PRINT CONTROL REG THAT FAILED
2955   006736  005100                            .WORD    EMSGR6
2956   006740  004737  007002                    JSR      PC,PRO6T                  ;GO PRINT CONTROL REG 0 AND 6 INFO
2957   006744                                    ENDMSG
2958   006744                           L10023:
2959   006744  104423                            TRAP     C$MSG
2960
2961   006746                                   BGNMSG   T6ALLR
2962   006746                           T6ALLR::
2963   006746  004537  006762                   JSR      R5,PRNTBS                 ;GO PRINT CONTROL REG THAT FAILED
2964   006752  005100                            .WORD    EMSGR6
2965   006754  004737  007032                    JSR      PC,ALPRNT                 ;GO PRINT ALL CONTROL REGISTER INFO
2966   006760                                    ENDMSG
2967   006760                           L10024:
2968   006760  104423                            TRAP     C$MSG
2969
2970                                    ;ROUTINE TO PRINT WHAT CONTROL REGISTER DETECTED THE ERROR.
2971
```

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GLOBAL AREAS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 61
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR TARGET EMULATOR MODULE   SEQ 0061

```
2972  006762                      PRNTBS::PRINTB  (R5)+
2973  006762  012546              MOV       (R5)+,-(SP)
2974  006764  012746  000001      MOV       #1,-(SP)
2975  006770  010600              MOV       SP,R0
2976  006772  104414              TRAP      C$PNTB
2977  006774  062706  000004      ADD       #4,SP
2978  007000  000205              RTS       R5
2979
2980                              ;ROUTINE TO PRINT CONTROL REGISTER 0 AND 6 ERROR INFORMATION
2981
2982  007002  004737  007054      PRO6T:: JSR      PC,PRNTT0
2983  007006  004737  007366              JSR      PC,PRNTT6
2984  007012  000207                      RTS      PC
2985
2986                              ;ROUTINE TO PRINT CONTROL REGISTER 0, 2 AND 6 ERROR INFORMATION
2987
2988  007014  004737  007054      PRO26T::JSR      PC,PRNTT0              ;GO PRINT CONTROL REGISTER 0 INFO
2989  007020  004737  007174              JSR      PC,PRNTT2              ;GO PRINT CONTROL REGISTER 2 INFO
2990  007024  004737  007366              JSR      PC,PRNTT6              ;GO PRINT CONTROL REGISTER 6 INFO
2991  007030  000207                      RTS      PC
2992
2993                              ;ROUTINE TO PRINT ALL TARGET EMULATORS CONTROL REGISTER INFORMATION
2994
2995  007032  004737  007054      ALPRNT::JSR      PC,PRNTT0              ;GO PRINT CONTROL REGISTER 0 INFO
2996  007036  004737  007174              JSR      PC,PRNTT2              ;GO PRINT CONTROL REGISTER 2 INFO
2997  007042  004737  007246              JSR      PC,PRNTT4              ;GO PRINT CONTROL REGISTER 4 INFO
2998  007046  004737  007366              JSR      PC,PRNTT6              ;GO PRINT CONTROL REGISTER 6 INFO
2999  007052  000207                      RTS      PC
3000
3001                              ;PRINT CONTROL REGISTER 0 ERROR INFORMATION
3002
3003  007054                      PRNTT0::PRINTX   #REG0EQ
3004  007054  012746  005130      MOV       #REG0EQ,-(SP)
3005  007060  012746  000001      MOV       #1,-(SP)
3006  007064  010600              MOV       SP,R0
3007  007066  104415              TRAP      C$PNTX
3008  007070  062706  000004      ADD       #4,SP
3009  007074  023737  002324  002326  CMP   TOLOAD,TOGOOD              ;CHECK IF LOADED DIFFERENT THEN EXPECTED
3010  007102  001417              BEQ       1$                        ;IF NOT THEN PRINT ''LOAD'' AND ''READ''
3011  007104                      PRINTX   #FSLGB,TOLOAD,TOGOOD,TOREAD
3012  007104  013746  002332      MOV       TOREAD,-(SP)
3013  007110  013746  002326      MOV       TOGOOD,-(SP)
3014  007114  013746  002324      MOV       TOLOAD,-(SP)
3015  007120  012746  005234      MOV       #FSLGB,-(SP)
3016  007124  012746  000004      MOV       #4,-(SP)
3017  007130  010600              MOV       SP,R0
3018  007132  104415              TRAP      C$PNTX
3019  007134  062706  000012      ADD       #12,SP
3020  007140  000414              BR        2$
3021  007142                      1$:      PRINTX   #FSLR,TOLOAD,TOREAD
3022  007142  013746  002332      MOV       TOREAD,-(SP)
3023  007146  013746  002324      MOV       TOLOAD,-(SP)
3024  007152  012746  005200      MOV       #FSLR,-(SP)
3025  007156  012746  000003      MOV       #3,-(SP)
3026  007162  010600              MOV       SP,R0
3027  007164  104415              TRAP      C$PNTX
```

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GLOBAL AREAS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 62
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR TARGET EMULATOR MODULE   SEQ 0062

```
3028   007166   062706   000010              ADD      #10,SP
3029   007172   000207              2$:      RTS      PC
3030
3031                                          ;PRINT CONTROL REGISTER 2 ERROR INFORMATION
3032
3033   007174                       PRNTT2::PRINTX  #REG2EQ
3034   007174   012746   005142              MOV      #REG2EQ,-(SP)
3035   007200   012746   000001              MOV      #1,-(SP)
3036   007204   010600                       MOV      SP,R0
3037   007206   104415                       TRAP     C$PNTX
3038   007210   062706   000004              ADD      #4,SP
3039   007214                                PRINTX   #FSLR,T2LOAD,T2READ
3040   007214   013746   002336              MOV      T2READ,-(SP)
3041   007220   013746   002334              MOV      T2LOAD,-(SP)
3042   007224   012746   005200              MOV      #FSLR,-(SP)
3043   007230   012746   000003              MOV      #3,-(SP)
3044   007234   010600                       MOV      SP,R0
3045   007236   104415                       TRAP     C$PNTX
3046   007240   062706   000010              ADD      #10,SP
3047   007244   000207                       RTS      PC
3048
3049                                          ;PRINT CONTROL REGISTER 4 ERROR INFORMATION
3050
3051   007246                       PRNTT4::PRINTX  #REG4EQ
3052   007246   012746   005154              MOV      #REG4EQ,-(SP)
3053   007252   012746   000001              MOV      #1,-(SP)
3054   007256   010600                       MOV      SP,R0
3055   007260   104415                       TRAP     C$PNTX
3056   007262   062706   000004              ADD      #4,SP
3057   007266   023737   002340   002342     CMP      T4LOAD,T4GOOD           ;CHECK IF LOADED DIFFERENT THEN EXPECTED
3058   007274   001417                        BEQ      1$                     ;IF NOT THEN PRINT "LOAD" AND "READ"
3059   007276                                PRINTX   #FSLGB,T4LOAD,T4GOOD,T4READ
3060   007276   013746   002344              MOV      T4READ,-(SP)
3061   007302   013746   002342              MOV      T4GOOD,-(SP)
3062   007306   013746   002340              MOV      T4LOAD,-(SP)
3063   007312   012746   005234              MOV      #FSLGB,-(SP)
3064   007316   012746   000004              MOV      #4,-(SP)
3065   007322   010600                       MOV      SP,R0
3066   007324   104415                       TRAP     C$PNTX
3067   007326   062706   000012              ADD      #12,SP
3068   007332   000414                        BR       2$
3069   007334                       1$:      PRINTX   #FSLR,T4LOAD,T4READ
3070   007334   013746   002344              MOV      T4READ,-(SP)
3071   007340   013746   002340              MOV      T4LOAD,-(SP)
3072   007344   012746   005200              MOV      #FSLR,-(SP)
3073   007350   012746   000003              MOV      #3,-(SP)
3074   007354   010600                       MOV      SP,R0
3075   007356   104415                       TRAP     C$PNTX
3076   007360   062706   000010              ADD      #10,SP
3077   007364   000207              2$:      RTS      PC
3078
```

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GLOBAL AREAS   MACY11 30A(1052)   16-JUN-82 13:46 PAGE 63
CVCDDB.P11   14-JUN-82 09:54   GLOBAL ERROR REPORT SECTION FOR TARGET EMULATOR MODULE   SEQ 0063

```
3079
3080                                        ;PRINT CONTROL REGISTER 6 ERROR INFORMATION
3081
3082  007366                    PRNTT6::PRINTX   #REG6EQ
3083  007366  012746  005166          MOV      #REG6EQ,-(SP)
3084  007372  012746  000001          MOV      #1,-(SP)
3085  007376  010600                  MOV      SP,R0
3086  007400  104415                  TRAP     C$PNTX
3087  007402  062706  000004          ADD      #4,SP
3088  007406                          PRINTX   #FSLR,T6LOAD,T6READ
3089  007406  013746  002350          MOV      T6READ,-(SP)
3090  007412  013746  002346          MOV      T6LOAD,-(SP)
3091  007416  012746  005200          MOV      #FSLR,-(SP)
3092  007422  012746  000003          MOV      #3,-(SP)
3093  007426  010600                  MOV      SP,R0
3094  007430  104415                  TRAP     C$PNTX
3095  007432  062706  000010          ADD      #10,SP
3096  007436  000207                  RTS      PC
3097
```

```
3098                              .SBTTL   GLOBAL SUBROUTINES SECTION
3099
3100                              ;++
3101                              ; THE GLOBAL SUBROUTINES SECTION CONTAINS THE SUBROUTINES
3102                              ; THAT ARE USED IN MORE THAN ONE TEST.
3103                              ;--
3104
3105                              ;++
3106                              ; FUNCTIONAL DESCRIPTION:
3107                              ;    SUBROUTINE TO....SELECT AND INITIALIZE TARGET EMULATOR
3108
3109                              ; INPUTS:
3110                              ;    LOCATION TEDEV CONTAINS USER DEFINED DEVICE NUMBER IN BITS 11-8
3111                              ;    LOCATION TETYPE CONTAINS TARGET EMULATOR DEVICE TYPE AND GDAL BIT 15
3112
3113
3114
3115                              ; IMPLICIT INPUTS:
3116
3117
3118                              ; OUTPUTS:
3119                              ;    T0LOAD CONTAINS USER DEFINED UNIT NUMBER IN BITS 11-8
3120                              ;    T2LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 2 WAS CLEARED
3121                              ;    T4LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 4 WAS CLEARED
3122                              ;    T6LOAD CONTAINS ALL ZEROES TO INDICATE MODE REGISTER WAS CLEARED
3123                              ;
3124                              ;    T0MASK EQUALS 0 TO CHECK ALL CONTROL REGISTER 0 BITS
3125                              ;    T6MASK EQUALS 0 TO CHECK ALL CONTROL REGISTER 6 BITS
3126
3127
3128                              ; IMPLICIT OUTPUTS:
3129
3130
3131                              ; SUBORDINATE ROUTINES USED:
3132                              ;    LDRDT0 ROUTINE TO LOAD, READ AND COMPARE REGISTER 0
3133                              ;    LDRDOT ROUTINE TO LOAD, READ AND COMPARE REGISTER 0 (USED FOR DEVICE TYPE)
3134                              ;    LDRDT2 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 2
3135                              ;    LDRDT4 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 4
3136                              ;    LDRDT6 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 6
3137
3138
3139                              ; FUNCTIONAL SIDE EFFECTS:
3140                              ;    TARGET EMULATOR SELECTED
3141                              ;    CONTROL REGISTER 0 LOW BYTE EQUALS 0 (GDAL 7:0)
3142                              ;    CONTROL REGISTER 2 EQUALS 0 (ADAL 15:0)
3143                              ;    CONTROL REGISTER 4 LOW BYTE EQUALS 0 (VDAL 15:0)
3144                              ;    CONTROL REGISTER 6 - HDAL 15:0 REGISTER EQUALS FOUR
3145                              ;    CONTROL REGISTER 6 - MODE REGISTER 15:0 EQUALS ZERO
3146
3147
3148                              ; CALLING SEQUENCE:
3149                              ;    JSR PC,INITTE
3150
3151                              ;--
3152
3153
```

```
3154                                        ;NOTE:  ON A START OR RESTART COMMAND TO THE DIAGNOSTIC SUPERVISOR, A
3155                                        ;       BUS RESET INSTRUCTION WILL BE ISSUED TO CLEAR ALL MODULES.  THIS
3156                                        ;       IS NEEDED TO CLEAR SIGNALS COMING INTO THE TARGET EMULATOR THAT
3157                                        ;       MAY BE SET ON THE MEMORY SIMULATOR MODULE OR STATE ANALYZER MODULE.
3158
3159
3160
3161
3162   007440                       INITMD::
3163   007440                       INITMS::BGNSEG
3164   007440  104404                       TRAP    C$BSEG
3165
3166                                        ;THE FOLLOWING SECTION OF CODE WILL SELECT AND INITIALIZE THE MEMORY
3167                                        ;SIMULATOR MODULE.   THE SIGNAL RST H WILL BE SET TO A ONE IN CONTROL
3168                                        ;REGISTER 0 TO PRESET THE RDV AND WRV FLIP-FLOPS.  WHEN THE RDV AND
3169                                        ;WRV FLIP-FLOPS ARE PRESET, THE SIGNALS ''RDV H'' AND ''WRV H'' WILL BE
3170                                        ;READ AS ZEROES IN CONTROL REGISTER 0.  ALL OTHER READ/WRITE BITS IN
3171                                        ;CONTROL REGISTER 0 WILL BE LOADED AND CHECKED FOR ZEROES.
3172
3173   007442  013737  002216  002234       MOV     MSDEV,SOLOAD           ;GET USER DEFINED DEVICE NUMBER
3174   007450  005237  002234               INC     SOLOAD                ;SET BIT TO SET RST H TO A ONE
3175   007454  005037  002240               CLR     SOMASK                ;CLEAR REGISTER 0 MASK WORD
3176   007460  013701  002204               MOV     REG0,R1               ;GET CONTROL REGISTER 0 DEVICE ADDRESS
3177   007464  113761  002217  000001       MOVB    MSDEV+1,1(R1)         ;LOAD HIGH BYTE WITH DEVICE NUMBER
3178   007472  004737  010506               JSR     PC,LDRDS0             ;GO LOAD, READ AND CHECK REGISTER 0
3179   007476  001405                        BEQ    1$                    ;IF LOADED OK THEN CONTINUE
3180   007500                               ERRDF   1,,SOEROR             ;MEM SIM REG 0 NOT EQUAL EXPECTED
3181   007500  104455                        TRAP   C$ERDF
3182   007502  000001                        .WORD  1
3183   007504  000000                        .WORD  0
3184   007506  005306                        .WORD  SOEROR
3185   007510                               CKLOOP
3186   007510  104406                        TRAP   C$CLP1
3187
3188                                        ;THE FOLLOWING SECTION WILL SET CONTROL REGISTER 0 BIT 15 TO A ONE.
3189                                        ;WHEN CONTROL REGISTER 0 BIT 15 IS SET TO A ONE, THE MODULES DEVICE
3190                                        ;TYPE WILL BE READBACK ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD
3191                                        ;OF THE MODULES DEVICE NUMBER.  THE MEMORY SIMULATORS DEVICE TYPE SHOULD
3192                                        ;EQUAL ONE (400).  THE SIGNAL RST H WILL BE LOADED AND CHECKED TO BE
3193                                        ;ZERO.
3194
3195   007512  013737  002216  002234  1$:   MOV     MSDEV,SOLOAD         ;GET USER DEFINED DEVICE NUMBER
3196   007520  052737  100000  002234        BIS     #IDH,SOLOAD         ;SELECT DEVICE TYPE INSTEAD OF NUMBER
3197   007526  013737  002220  002236        MOV     MSTYPE,SOGOOD       ;GET DEVICE TYPE AND SAVE (400)
3198   007534  004737  010514                JSR     PC,LDRD0S           ;GO LOAD, READ AND CHECK REGISTER 0
3199   007540  001405                        BEQ     2$                  ;IF LOADED OK THEN CONTINUE
3200   007542                                ERRDF   1,,SOEROR           ;DEVICE TYPE OR LOW BYTE NOT = EXPECTED
3201   007542  104455                        TRAP    C$ERDF
3202   007544  000001                        .WORD   1
3203   007546  000000                        .WORD   0
3204   007550  005306                        .WORD   SOEROR
3205   007552                                CKLOOP
3206   007552  104406                        TRAP    C$CLP1
3207
3208                                        ;SET CONTROL REGISTER 0 BIT 15 TO A ZERO AND CHECK THAT THE DEVICE
3209                                        ;NUMBER CAN BE READBACK AGAIN INSTEAD OF THE DEVICE TYPE.
```

```
3210
3211    007554  042737  100000  002234  2$:    BIC    #IDH,SOLOAD             ;SETUP TO READBACK DEVICE NUMBER
3212    007562  004737  010506                 JSR    PC,LDRDSO              ;GO LOAD, READ AND CHECK REGISTER 0
3213    007566  001405                         BEQ    3$                     ;IF LOADED OK THEN CONTINUE
3214    007570                                 ERRDF  1,,SOEROR              ;DEVICE # OR LOW BYTE NOT = EXPECTED
3215    007570  104455                         TRAP   C$ERDF
3216    007572  000001                         .WORD  1
3217    007574  000000                         .WORD  0
3218    007576  005306                         .WORD  SOEROR
3219    007600                                 CKLOOP
3220    007600  104406                         TRAP   C$CLP1
3221
3222                                           ;SET THE SIGNALS MSEL1 H, MSEL2 H, MSAD17 H AND MSAD16 H TO ZEROES IN
3223                                           ;CONTROL REGISTER 2 AND CHECK THAT THESE SIGNALS ARE READBACK AS ZEROES.
3224                                           ;AS A RESULT OF THE SIGNAL MP H BEING A ZERO IN CONTROL REGISTER 0,
3225                                           ;CONTROL REGISTER 2 READ ONLY BITS ESR H, WREN H AND MEMBRK H WILL NOT BE
3226                                           ;CHECKED AT THIS POINT IN TIME BECAUSE THEY SHOULD BE TRI-STATED.
3227
3228    007602  005037  002244        3$:      CLR    S2LOAD                 ;SETUP TO CLEAR R/W BITS
3229    007606  012737  177740  002250         MOV    #177740,S2MASK         ;IGNORE READ ONLY AND UNUSED BITS
3230    007614  004737  010546                 JSR    PC,LDRDS2              ;GO LOAD, READ AND CHECK REGISTER 2
3231    007620  001405                         BEQ    4$                     ;IF LOADED OK THEN CONTINUE
3232    007622                                 ERRDF  2,,S2EROR              ;REGISTER 2 NOT EQUAL TO ZERO
3233    007622  104455                         TRAP   C$ERDF
3234    007624  000002                         .WORD  2
3235    007626  000000                         .WORD  0
3236    007630  005322                         .WORD  S2EROR
3237    007632                                 CKLOOP
3238    007632  104406                         TRAP   C$CLP1
3239
3240                                           ;CLEAR MSAD BITS 15:0 IN CONTROL REGISTER 4 AND CHECK THAT THESE BITS
3241                                           ;ARE CLEARED BY READING BACK CONTROL REGISTER 4.
3242
3243    007634  005037  002254        4$:      CLR    S4LOAD                 ;SETUP TO CLEAR ALL MSAD BITS (15:0)
3244    007640  004737  010606                 JSR    PC,LDRDS4              ;GO LOAD, READ AND CHECK REGISTER 4
3245    007644  001404                         BEQ    5$                     ;IF LOADED OK THEN CONTINUE
3246    007646                                 ERRDF  3,MSADRG,S4EROR        ;CONTROL REGISTER 4 NOT EQUAL TO 0
3247    007646  104455                         TRAP   C$ERDF
3248    007650  000003                         .WORD  3
3249    007652  002510                         .WORD  MSADRG
3250    007654  005336                         .WORD  S4EROR
3251    007656  012737  177760  002264  5$:    MOV    #177760,S6MASK         ;SETUP REG 6 MASK WORD FOR FUTURE USE
3252    007664                                 ENDSEG
3253    007664                         10000$:
3254    007664  104405                         TRAP   C$ESEG
3255
3256    007666                         INITED::BGNSEG
3257    007666  104404                         TRAP   C$BSEG
3258
3259                                           ;THE FOLLOWING SECTION OF CODE WILL SELECT AND INITIALIZE THE STATE
3260                                           ;ANALYZER MODULE.  THE SIGNAL "CDALO H" WILL BE SET TO A ONE TO CLEAR
3261                                           ;THE TRACE RAM ADDRESS REGISTER, TO CLEAR THE TRACING AND SBL FLIP-FLOPS,
3262                                           ;AND TO LOAD THE EVENT COUNTERS FROM THE EVENT COUNTER REGISTERS.  ALL
3263                                           ;OTHER READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES.
3264
3265    007670  013737  002222  002272         MOV    EDDEV,EOLOAD           ;GET USER DEFINED DEVICE NUMBER
```

```
3266  007676  005237  002272              INC   EOLOAD              ;SET BIT CDAL0 H TO A ONE
3267  007702  013701  002204              MOV   REG0,R1             ;GET DEVICE'S REGISTER 0 ADDRESS
3268  007706  113761  002223    000001    MOVB  EDDEV+1,1(R1)       ;LOAD HIG' BYTE WITH DEVICE NUMBER
3269  007714  004737  010700              JSR   PC,LDRDEO           ;GO LOAD, READ AND CHECK REGISTER 0
3270  007720  001405                      BEQ   1$                  ;IF LOADED OK TEHN CONTINUE
3271  007722                              ERRDF 5,CDALRG,EOEROR     ;STATE ANALYZER REG 0 NOT = EXPECTED
3272  007722  104455                      TRAP  C$ERDF
3273  007724  000005                      .WORD 5
3274  007726  003010                      .WORD CDALRG
3275  007730  006146                      .WORD EOEROR
3276  007732                              CKLOOP
3277  007732  104406                      TRAP  C$CLP1
3278
3279                                       ;THE FOLLOWING SECTION WILL SET CONTROL REGISTER 0 BIT 15 TO A ONE.
3280                                       ;WHEN CDAL15 H IS SET TO A ONE, THE MODULES DEVICE TYPE WILL BE READ-
3281                                       ;BACK ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE
3282                                       ;NUMBER.  THE STATE ANALYZERS DEVICE TYPE SHOULD EQUAL TWO (1000).  THE
3283                                       ;SIGNAL "CDAL0 H" WILL BE LOADED AND CHECKED FOR ZEROES.
3284
3285  007734  013737  002222  002272  1$:  MOV   EDDEV,EOLOAD        ;GET USER DEFINED DEVICE NUMBER
3286  007742  052737  100000  002272       BIS   #CDAL15,EOLOAD      ;SELECT DEVICE TYPE TO BE READ
3287  007750  013737  002224  002274       MOV   EDTYPE,EOGOOD       ;GET DEVICE TYPE AND SAVE (1000)
3288  007756  004737  010706              JSR   PC,LDRDOE           ;GO LOAD, READ AND CHECK REGISTER 0
3289  007762  001405                      BEQ   2$                  ;IF LOADED OK THEN CONTINUE
3290  007764                              ERRDF 5,CDALRG,EOEROR     ;DEVICE TYPE OR LOW BYTE NOT = EXPECTED
3291  007764  104455                      TRAP  C$ERDF
3292  007766  000005                      .WORD 5
3293  007770  003010                      .WORD CDALRG
3294  007772  006146                      .WORD EOEROR
3295  007774                              CKLOOP
3296  007774  104406                      TRAP  C$CLP1
3297
3298                                       ;SET CONTROL REGISTER 0 BIT 15 TO A ZERO AND CHECK THAT THE DEVICE
3299                                       ;NUMBER CAN BE READBACK AGAIN INSTEAD OF THE DEVICE TYPE.
3300
3301  007776  042737  100000  002272  2$:  BIC   #CDAL15,EOLOAD      ;SELECT DEVICE NUMBER TO BE READ
3302  010004  004737  010700              JSR   PC,LDRDEO           ;GO LOAD, READ AND CHECK REGISTER 0
3303  010010  001405                      BEQ   3$                  ;IF LOADED OK THEN CONTINUE
3304  010012                              ERRDF 5,CDALRG,EOEROR     ;DEVICE # OR LOW BYTE NOT = EXPECTED
3305  010012  104455                      TRAP  C$ERDF
3306  010014  000005                      .WORD 5
3307  010016  003010                      .WORD CDALRG
3308  010020  006146                      .WORD EOEROR
3309  010022                              CKLOOP
3310  010022  104406                      TRAP  C$CLP1
3311
3312                                       ;LOAD, READ AND CHECK CONTROL REGISTER 2 WITH A DATA PATTERN OF ALL
3313                                       ;ZEROES.  THE HIGH BYTE OF CONTROL REGISTER 2 IS NOT AVAILABLE,
3314                                       ;THEREFORE, ON A READ COMMAND TO CONTROL REGISTER 2, THE HIGH BYTE
3315                                       ;WILL BE IGNORED.
3316
3317  010024  005037  002300          3$:  CLR   E2LOAD              ;SETUP TO CLEAR ALL READ/WRITE BITS
3318  010030  004737  010732              JSR   PC,LDRDE2           ;GO LOAD, READ AND CHECK REGISTER 2
3319  010034  001404                      BEQ   4$                  ;IF LOADED OK THEN CONTINUE
3320  010036                              ERRDF 6,PDALRG,E2EROR     ;PDAL 7:0 REGISTER NOT EQUAL TO ZERO
3321  010036  104455                      TRAP  C$ERDF
```

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3322   010040  000006                           .WORD   6
3323   010042  003034                           .WORD   PDALRG
3324   010044  006162                           .WORD   E2EROR
3325   010046  005037  002310      4$:    CLR    E4MASK                    ;SET REGISTER 4 MASK WORD TO ZERO
3326   010052  005037  002320             CLR    E6MASK                    ;SET REGISTER 6 MASK WORD TO ZERO
3327   010056                             ENDSEG
3328   010056                      10001$:
3329   010056  104405                     TRAP   C$ESEG
3330
3331   010060                      INITTE::BGNSEG                          ;ROUTINE TO INIT TE MODULE
3332   010060  104404                     TRAP   C$BSEG
3333
3334                               ;THE FOLLOWING SECTION OF CODE WILL SELECT AND INITIALIZE THE TARGET
3335                               ;EMULATOR MODULE.  THE READ/WRITE BITS WILL BE LOADED AND CHECKED
3336                               ;FOR ZEROES.  THE READ ONLY BITS, EXCEPT EDBRK H, WILL BE IGNORED
3337                               ;AT THIS POINT IN TIME.  THE SIGNAL 'EDBRK H' SHOULD BE READ AS A ZERO
3338                               ;AS A RESULT OF THE SIGNAL ''CDAL1 H'' BEING LOADED TO A ZERO IN CONTROL
3339                               ;REGISTER ZERO OF THE STATE ANALYZER MODULE.
3340
3341   010062  013737  002226  002324      MOV   TEDEV,TOLOAD              ;GET USER DEFINED DEVICE NUMBER
3342   010070  012737  000340  002330      MOV   #SSBRK!TOBRK!MEMBRK,TOMASK ;SETUP TO IGNORE READ ONLY BITS
3343   010076  013701  002204             MOV    REG0,R1                   ;GET DEVICE'S CONTROL REGISTER 0 ADDRESS
3344   010102  113761  002227  000001     MOVB   TEDEV+1,1(R1)            ;LOAD HIGH BYTE WITH THE DEVICE NUMBER
3345   010110  004737  011100             JSR    PC,LDRDTO                 ;GO LOAD,READ AND COMPARE REG 0
3346   010114  001404                     BEQ    1$                        ;IF COMPARE WAS GOOD THEN CONT
3347   010116                             ERRDF  9,GDALRG,TOEROR           ;DEVICE # OR LB NOT = EXPECTED
3348   010116  104455                     TRAP   C$ERDF
3349   010120  000011                     .WORD  9
3350   010122  003640                     .WORD  GDALRG
3351   010124  006666                     .WORD  TOEROR
3352
3353                               ;THE FOLLOWING SECTION WILL SET CONTROL REGISTER 0 BIT 15 TO A ONE.
3354                               ;WHEN GDAL15 H IS SET TO A ONE, THE MODULES DEVICE TYPE WILL BE READ-
3355                               ;BACK ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE
3356                               ;NUMBER. THE TARGET EMULATORS DEVICE TYPE SHOULD EQUAL ZERO (000000).
3357
3358   010126  052737  100000  002324  1$: BIS   #GDAL15,TOLOAD            ;SETUP TO READ DEVICE TYPE
3359   010134  013737  002230  002326     MOV    TETYPE,TOGOOD             ;SETUP EXPECTED DATA
3360   010142  004737  011106             JSR    PC,LDRDOT                 ;LOAD, READ AND COMPARE REG 0
3361   010146  001405                     BEQ    2$                        ;IF EQUAL THEN DEVICE TYPE COMPARED
3362   010150                             ERRDF  9,GDALRG,TOEROR           ;DEVICE TYPE NOT EQUAL EXPECTED
3363   010150  104455                     TRAP   C$ERDF
3364   010152  000011                     .WORD  9
3365   010154  003640                     .WORD  GDALRG
3366   010156  006666                     .WORD  TOEROR
3367   010160                             CKLOOP
3368   010160  104406                     TRAP   C$CLP1
3369
3370                               ;RESET THE SIGNAL GDAL15 H TO A 0 SO THAT THE DEVICE NUMBER WILL BE
3371                               ;READ AGAIN.  SET GDAL1 H AND GDAL0 H TO ONES AND GDAL2 H TO A ZERO.
3372                               ;THIS IS DONE SO THAT THE HDAL REGISTER CAN BE SELECTED AND INITIALIZED.
3373
3374   010162  013737  002226  002324  2$: MOV   TEDEV,TOLOAD              ;GET USER DEFINED DEVICE NUMBER
3375   010170  052737  000003  002324     BIS    #GDAL1!GDAL0,TOLOAD       ;SET BITS TO SELECT THE HDAL REGISTER
3376   010176  004737  011100             JSR    PC,LDRDTO                 ;GO LOAD, READ AND CHECK GDAL REGISTER
3377   010202  001405                     BEQ    3$                        ;IF LOADED OK THEN CONTINUE
```

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3378  010204                              ERRDF   9,GDALRG,TOEROR       ;GDAL REGISTER NOT EQUAL TO EXPECTED
3379  010204  104455                      TRAP    C$ERDF
3380  010206  000011                      .WORD   9
3381  010210  003640                      .WORD   GDALRG
3382  010212  006666                      .WORD   TOEROR
3383  010214                              CKLOOP
3384  010214  104406                      TRAP    C$CLP1
3385
3386                              ;LOAD, READ AND CHECK THE HDAL REGISTER WITH A DATA PATTERN OF FOUR.
3387                              ;HDAL2 H SET TO A ONE WILL ENABLE THE PROGRAM TO GENERATE AND CONTROL
3388                              ;THE T-11 TIMING AND CONTROL SIGNALS INSTEAD OF THE T-11 GENERATING THEM.
3389                              ;ON A WRITE COMMAND TO CONTROL REIGSTER 6 WITH GDAL BITS 1 AND 0 SET,
3390                              ;PULSES WILL OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H.   THESE
3391                              ;PULSES WILL LOAD THE DATA INTO THE HDAL REGISTER.  ON A READ COMMAND
3392                              ;TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REGISTER
3393                              ;VIA THE SIGNAL RPT3 L.
3394
3395  010216  012737  000004  002346  3$: MOV     #HDAL2,T6LOAD         ;SETUP BIT TO BE LOADED
3396  010224  005037  002352              CLR     T6MASK               ;SETUP MASK WORK TO COMPARE ALL BITS
3397  010230  004737  011216              JSR     PC,LDRDT6            ;GO LOAD, READ AND CHECK HDAL REGISTER
3398  010234  001405                      BEQ     4$                   ;IF LOADED OK THEN CONTINUE
3399  010236                              ERRDF   12,HDALRG,T06ERR     ;HDAL REGISTER NOT EQUAL TO EXPECTED.
3400  010236  104455                      TRAP    C$ERDF
3401  010240  000014                      .WORD   12
3402  010242  003756                      .WORD   HDALRG
3403  010244  006732                      .WORD   T06ERR
3404  010246                              CKLOOP
3405  010246  104406                      TRAP    C$CLP1
3406
3407                              ;SELECT THE MODE REGISTER BY SETTING GDAL BIT 2 TO A ONE AND GDAL BITS
3408                              ;1 AND 0 TO ZEROES.  THIS IS DONE SO THAT THE MODE REGISTER CAN BE
3409                              ;SELECTED AND CLEARED.
3410
3411  010250  013737  002226  002324  4$: MOV     TEDEV,TOLOAD         ;GET USER DEFINED DEVICE NUMBER
3412  010256  052737  000004  002324      BIS     #GDAL2,TOLOAD        ;GET BIT TO SELECT MODE REGISTER
3413  010264  004737  011100              JSR     PC,LDRDT0            ;GO LOAD, READ AND CHECK MODE REGISTER
3414  010270  001405                      BEQ     5$                   ;IF LOADED OK THEN CONTINUE
3415  010272                              ERRDF   9,GDALRG,TOEROR      ;GDAL REGISTER NOT EQUAL EXPECTED
3416  010272  104455                      TRAP    C$ERDF
3417  010274  000011                      .WORD   9
3418  010276  003640                      .WORD   GDALRG
3419  010300  006666                      .WORD   TOEROR
3420  010302                              CKLOOP
3421  010302  104406                      TRAP    C$CLP1
3422
3423                              ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES.
3424                              ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BIT 2 SET TO A ONE
3425                              ;AND GDAL BITS 1 AND 0 SET TO ZEROES, PULSES WILL OCCUR ON THE SIGNALS
3426                              ;WPT4 LB H AND WPT4 HB H.   THESE PULSES WILL LOAD THE DATA ON THE WRITE
3427                              ;COMMAND INTO THE MODE REGISTER.  ON A READ COMMAND TO CONTROL REGISTER 6,
3428                              ;DATA WILL BE READBACK FROM THE MODE REGISTER VIA THE SIGNAL RPT4 L.
3429
3430  010304  005037  002346          5$: CLR     T6LOAD               ;SETUP TO LOAD ALL ZEROES INTO MODE REG
3431  010310  004737  011216              JSR     PC,LDRDT6            ;GO LOAD, READ AND CHECK MODE REGISTER
3432  010314  001405                      BEQ     6$                   ;IF LOADED OK THEN CONTINUE
3433  010316                              ERRDF   12,MODREG,T06ERR     ;MODE REGISTER NOT EQUAL EXPECTED
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3434  010316  104455                        TRAP    C$ERDF
3435  010320  000014                        .WORD   12
3436  010322  004002                        .WORD   MODREG
3437  010324  006732                        .WORD   TO6ERR
3438  010326                                 CKLOOP
3439  010326  104406                        TRAP    C$CLP1
3440
3441                              ;SET AND CLEAR ADAL0 H IN CONTROL REGISTER 2 TO CLEAR THE SINGLE STEP
3442                              ;BREAK FLIP-FLOP AND THE MEMORY SIMULATOR BREAK LATCH (MEMBRK) FLIP-FLOP.
3443                              ;ALL OTHER BITS IN CONTROL REGISTER 2 WILL BE CLEARED.  ADAL8 H ON A ZERO
3444                              ;WILL INHIBIT THE TIMEOUT BREAK ONE SHOT OUTPUT TO BE READ IN ITS LOGICAL
3445                              ;STATE.  THE SIGNAL "TOBRK H" WILL BE ASSERTED LOW WHEN ADAL8 H IS A ZERO.
3446                              ;AFTER SETTING AND CLEARING ADAL0 H IN CONTROL REGISTER 2, THE TEST WILL
3447                              ;READ CONTROL REGISTER 0 AND CHECK THAT SINGLE STEP BREAK FLIP-FLOP,
3448                              ;MEMORY SIMULATOR BREAK FLIP-FLOP, AND TIMEOUT BREAK SIGNALS ARE READ
3449                              ;BACK AS ZEROES.
3450
3451  010330  012737  000001  002334  6$:   MOV     #ADAL0,T2LOAD       ;SETUP BIT TO BE LOADED TO 0 SSBRK F/F
3452  010336  004737  011140               JSR     PC,LDRDT2           ;GO LOAD, READ AND CHECK REGISTER 2
3453  010342  001405                        BEQ     7$                  ;IF LOADED OK THEN CONTINUE
3454  010344                                ERRDF   10,ADALRG,T2EROR    ;REGISTER 2 NOT EQUAL TO ADAL0
3455  010344  104455                        TRAP    C$ERDF
3456  010346  000012                        .WORD   10
3457  010350  003664                        .WORD   ADALRG
3458  010352  006702                        .WORD   T2EROR
3459  010354                                CKLOOP
3460  010354  104406                        TRAP    C$CLP1
3461  010356  005037  002334        7$:     CLR     T2LOAD              ;SETUP TO CLEAR ADAL0
3462  010362  004737  011140               JSR     PC,LDRDT2           ;GO LOAD, READ AND CHECK REGISTER 2
3463  010366  001405                        BEQ     8$                  ;IF LOADED OK THEN CONTINUE
3464  010370                                ERRDF   10,ADALRG,T2EROR    ;REGISTER 2 NOT EQUAL EXPECTED
3465  010370  104455                        TRAP    C$ERDF
3466  010372  000012                        .WORD   10
3467  010374  003664                        .WORD   ADALRG
3468  010376  006702                        .WORD   T2EROR
3469  010400                                CKLOOP
3470  010400  104406                        TRAP    C$CLP1
3471
3472                              ;LOAD, READ AND CHECK CONTROL REGISTER 0.  CHECK TIMEOUT BREAK SIGNAL
3473                              ;TO BE ZERO AND CHECK MEMORY SIMULATOR BREAK AND SINGLE STEP BREAK FLIP-
3474                              ;FLOPS TO BE CLEARED.
3475
3476  010402  005037  002330        8$:     CLR     TOMASK              ;CLEAR MASK TO CHECK ALL BITS IN REG 0
3477  010406  105037  002324               CLRB    TOLOAD              ;SETUP TO CLEAR THE LOWER BYTE
3478  010412  004737  011100               JSR     PC,LDRDTO           ;GO LOAD, READ AND CHECK GDAL REGISTER
3479  010416  001405                        BEQ     9$                  ;IF ALL BITS CHECKED THEN CONTINUE
3480  010420                                ERRDF   9,GDALRG,TOEROR     ;REGISTER 0 NOT EQUAL TO DEVICE NUMBER
3481  010420  104455                        TRAP    C$ERDF
3482  010422  000011                        .WORD   9
3483  010424  003640                        .WORD   GDALRG
3484  010426  006666                        .WORD   TOEROR
3485  010430                                CKLOOP
3486  010430  104406                        TRAP    C$CLP1
3487
3488                              ;SET AND CLEAR VDAL2 IN CONTROL REGISTER 4.  WHEN VDAL2 IS SET TO A
3489                              ;ONE, THE PAUSE STATE MACHINE FLIP-FLOPS WILL BE CLEARED.  THESE F/F'S
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3490                                           ;ARE READBACK IN VDAL REGISTER BITS 15:8.  THE REMAINING VDAL READ/
3491                                           ;WRITE BITS WILL BE LOADED AND CHECKED FOR ZEORES.
3492
3493   010432  012737  000004  002340  9$:    MOV     #VDAL2,T4LOAD       ;SETUP BIT TO BE LOADED
3494   010440  004737  011164                  JSR     PC,LDRDT4          ;GO LOAD, READ AND CHECK VDAL REG
3495   010444  001405                           BEQ     10$               ;IF LOADED OK THEN CONTINUE
3496   010446                                   ERRDF   11,VDALRG,T4EROR  ;VDAL REGISTER NOT EQUAL TO 2
3497   010446  104455                            TRAP    C$ERDF
3498   010450  000013                            .WORD   11
3499   010452  003710                            .WORD   VDALRG
3500   010454  006716                            .WORD   T4EROR
3501   010456                                   CKLOOP
3502   010456  104406                            TRAP    C$CLP1
3503   010460  005037  002340          10$:    CLR     T4LOAD             ;SETUP TO CLEAR VDAL2
3504   010464  004737  011164                  JSR     PC,LDRDT4          ;GO LOAD, READ AND CHECK VDAL REG
3505   010470  001404                           BEQ     11$               ;IF LOADED OK THEN CONTINUE
3506   010472                                   ERRDF   11,VDALRG,T4EROR  ;VDAL REG NOT EQUAL TO 0
3507   010472  104455                            TRAP    C$ERDF
3508   010474  000013                            .WORD   11
3509   010476  003710                            .WORD   VDALRG
3510   010500  006716                            .WORD   T4EROR
3511   010502                          11$:    ENDSEG
3512   010502                          10002$:
3513   010502  104405                           TRAP    C$ESEG
3514
3515   010504  000207                           RTS     PC                ;RETURN BACK TO TEST
3516
```

```
3517
3518                            ;********************************************************************************
3519                            ;
3520                            ;        MDE/T-11 MEMORY SIMULATOR ROUTINES TO LOAD CONTROL REGISTERS 0,2,4,+6
3521                            ;
3522                            ;********************************************************************************
3523
3524                            ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF MEMORY SIMULATOR CONTROL REGISTER
3525                            ;0.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF THE ''CMP'' INSTRUCTION.
3526
3527  010506  013737  002234  002236  LDRDS0::MOV    S0LOAD,S0GOOD         ;PUT DATA LOADED INTO EXPECTED
3528  010514  013777  002234  171462  LDRD0S::MOV    S0LOAD,@REG0         ;WRITE WORD TO REGISTER 0
3529  010522  017737  171456  002242  READS0::MOV    @REG0,S0READ         ;READ REGISTER CONTENTS BACK
3530  010530  043737  002240  002242          BIC    S0MASK,S0READ        ;CLEAR UNWANTED BITS OF REG 0
3531  010536  023737  002236  002242          CMP    S0GOOD,S0READ        ;COMPARE EXPECTED WITH THAT READ
3532  010544  000207                          RTS    PC                   ;EXIT WITH CONDITION CODES SET
3533
3534                            ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF MEMORY SIMULATOR CONTROL REGISTER
3535                            ;2.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF THE ''CMP'' INSTRUCTION.
3536
3537  010546  013737  002244  002246  LDRDS2::MOV    S2LOAD,S2GOOD        ;PUT DATA TO BE LOADED INTO EXPECTED
3538  010554  013777  002244  171424  LDRD2S::MOV    S2LOAD,@REG2         ;WRITE BITS INTO REGISTER 2
3539  010562  017737  171420  002252  READS2::MOV    @REG2,S2READ         ;READ REGISTER 2 BACK AND SAVE
3540  010570  043737  002250  002252          BIC    S2MASK,S2READ        ;CLEAR UNWANTED BITS IN REG 2
3541  010576  023737  002246  002252          CMP    S2GOOD,S2READ        ;CHECK IF EXPECTED = ACTUAL READ
3542  010604  000207                          RTS    PC                   ;EXIT WITH CONDITION CODES SET
3543
3544                            ;ROUTINE TO LOAD, READ AND COMAPRE CONTENTS OF MEMORY SIMULATOR CONTROL REGISTER
3545                            ;4.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF THE ''CMP'' INSTRUCTION.
3546
3547  010606  013777  002254  171374  LDRDS4::MOV    S4LOAD,@REG4         ;WRITE WORD INTO REGISTER 4
3548  010614  017737  171370  002256  READS4::MOV    @REG4,S4READ         ;READ WORD BACK FROM REG 4
3549  010622  023737  002254  002256          CMP    S4LOAD,S4READ        ;COMPARE LOADED WITH WORD READ
3550  010630  000207                          RTS    PC                   ;RETURN WITH CONDTION CODES SET
3551
3552                            ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF MOMORY SIMULATOR CONTROL REGISTER
3553                            ;6.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF THE ''CMP'' INSTRUCTION.
3554
3555  010632  013737  002260  002262  LDRDS6::MOV    S6LOAD,S6GOOD        ;COPY DATA TO BE LOADED
3556  010640  013777  002260  171344  LDRD6S::MOV    S6LOAD,@REG6         ;WRITE WORD INTO REGISTER 6
3557  010646  017737  171340  002266  READS6::MOV    @REG6,S6READ         ;READ CONTROL REGISTER 6 BACK
3558  010654  013737  002266  002270          MOV    S6READ,S6BAD         ;COPY DATA READ
3559  010662  043737  002264  002270          BIC    S6MASK,S6BAD         ;CLEAR UNWANTED BITS IN WORD READ
3560  010670  023737  002262  002270          CMP    S6GOOD,S6BAD         ;COMPARE EXPECTED WITH ACTUAL READ
3561  010676  000207                          RTS    PC                   ;EXIT WITH CONDTION CODES SET
3562
```

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3563                           ;**********************************************************************
3564                           ;
3565                           ;      MDE/T-11 STATE ANALYZER ROUTINES USED TO LOAD CONTROL REGISTERS 0,2,4,+6
3566                           ;
3567                           ;**********************************************************************
3568
3569                           ;ROUTINE TO LOAD, READ AND COMPARE THE CONTENTS OF STATE ANALYZER CONTROL
3570                           ;REGISTER 0.  CONDITION CODES ARE SET ON EXIT AS A RESULT OF "CMP" INSTRUCTION.
3571
3572   010700  013737  002272  002274  LDRDE0::MOV   E0LOAD,E0GOOD        ;PUT DATA LOADED INTO EXPECTED
3573   010706  013777  002272  171270  LDRD0E::MOV   E0LOAD,@REG0         ;WRITE WORD INTO REGISTER 0
3574   010714  017737  171264  002276  READE0::MOV   @REG0,E0READ         ;READ REGISTER 0 CONTENTS BACK
3575   010722  023737  002274  002276         CMP    E0GOOD,E0READ        ;COMPARE EXPECTED WITH ACTUAL
3576   010730  000207                         RTS    PC                   ;EXIT WITH CONDTION CODES SET
3577
3578                           ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF STATE ANALYZER CONTROL REGISTER 2.
3579                           ;CONDTION CODES ARE SET ON EXIT AS A RESULT OF "CMP" INSTRUCTION.
3580
3581   010732  013777  002300  171246  LDRDE2::MOV   E2LOAD,@REG2         ;WRITE WORD INTO REGISTER 2
3582   010740  017737  171242  002302  READE2::MOV   @REG2,E2READ         ;READ CONTENTS OF REGISTER 2 BACK
3583   010746  042737  177400  002302         BIC    #177400,E2READ       ;CLEAR HIGH BYTE BITS
3584   010754  023737  002300  002302         CMP    E2LOAD,E2READ        ;COMPARE LOADED WITH ACTUAL READ
3585   010762  000207                         RTS    PC                   ;EXIT WITH CONDTION CODES SET
3586
3587                           ;ROUTINE TO LOAD, READ AND CHECK CONTENTS OF STATE ANALYZER CONTROL REGISTER 4.
3588                           ;CONDTION CODES WILL BE SET ON EXIT AS A RESULT OF "CMP" INSTRUCTION.
3589
3590   010764  013737  002304  002306  LDRDAR::MOV   E4LOAD,E4GOOD        ;COPY DATA TO BE LOADED
3591   010772  000337  002306         SWAB   E4GOOD               ;LOW TO HIGH BYTE TO SIMULATE READBACK
3592   010776  000403                         BR     LDRD4E               ;GO LOAD READ + CHECK AND ARRAY
3593
3594   011000  013737  002304  002306  LDRDE4::MOV   E4LOAD,E4GOOD        ;COPY DATA LOADED TO EXPECTED DATA
3595   011006  013777  002304  171174  LDRD4E::MOV   E4LOAD,@REG4         ;WRITE WORD INTO REGISTER 4
3596   011014  017737  171170  002312  READE4::MOV   @REG4,E4READ         ;READ WORD BACK FROM REGISTER 4
3597   011022  013737  002312  002314         MOV    E4READ,E4BAD         ;COPY DATA READ
3598   011030  043737  002310  002314         BIC    E4MASK,E4BAD         ;CLEAR UNWANTED BITS
3599   011036  023737  002306  002314         CMP    E4GOOD,E4BAD         ;COMPARE WORD EXPECTED WITH ACTUAL
3600   011044  000207                         RTS    PC                   ;RETURN WITH CONDITION CODES SET
3601
3602                           ;ROUTINE TO LOAD, READ AND CHECK CONTENTS OF STATE ANALYZER CONTROL REGISTER 6.
3603                           ;CONDITION CODES WILL BE SET ON EXIT AS A RESULT OF "CMP" INSTRUCTION.
3604
3605   011046  013777  002316  171136  LDRDE6::MOV   E6LOAD,@REG6         ;WRITE WORD INTO REGISTER 6
3606   011054  017737  171132  002322  READE6::MOV   @REG6,E6READ         ;READ THE WORD BACK
3607   011062  043737  002320  002322         BIC    E6MASK,E6READ        ;CLEAR UNWANTED BITS
3608   011070  023737  002316  002322         CMP    E6LOAD,E6READ        ;COMPARE DATA LOADED WITH ACTUAL READ
3609   011076  000207                         RTS    PC                   ;EXIT WITH CONDITION CODES SET
3610
```

```
3611                             ;***************************************************************************
3612                             ;
3613                             ;      MDE/T-11 TARGET EMULATOR ROUTINES TO LOAD CONTROL REGISTERS 0,2,4,+6
3614                             ;
3615                             ;***************************************************************************
3616
3617                             ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF TARGET EMULATOR CONTROL REGISTER 0.
3618                             ;CONDITION CODES ARE SET ON EXIT AS RESULT OF THE "CMP" INSTRUCTION.
3619
3620   011100  013737  002324  002326  LDRDT0::MOV     TOLOAD,TOGOOD      ;PUT DATA LOADED INTO EXPECTED
3621   011106  013777  002324  171070  LDRDOT::MOV     TOLOAD,@REG0       ;WRITE WORD TO REGISTER 0
3622   011114  017737  171064  002332  READT0::MOV     @REG0,TOREAD       ;READ REGISTER CONTENTS BACK
3623   011122  043737  002330  002332          BIC     TOMASK,TOREAD      ;CLEAR OUT UNWANTED BITS
3624   011130  023737  002326  002332          CMP     TOGOOD,TOREAD      ;COMPARE EXPECTED WITH THAT READ
3625   011136  000207                          RTS     PC                 ;EXIT WITH CONDITION CODES SET
3626
3627                             ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OFTARGET EMULATOR CONTROL REGISTER 2.
3628                             ;CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION
3629
3630   011140  013777  002334  171040  LDRDT2::MOV     T2LOAD,@REG2       ;WRITE BITS INTO REGISTER 2
3631   011146  017737  171034  002336  READT2::MOV     @REG2,T2READ       ;READ REGISTER 2 BACK
3632   011154  023737  002334  002336          CMP     T2LOAD,T2READ      ;CHECK IF EXP EQUALS ACTUAL
3633   011162  000207                          RTS     PC                 ;EXIT WITH CONDITION CODES SET
3634
3635                             ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF TARGET EMULATOR CONTROL REGISTER 4.
3636                             ;CONDITION CODES ARE SET ON EXET AS RESULT OF "CMP" INSTRUCTION.
3637
3638   011164  013737  002340  002342  LDRDT4::MOV     T4LOAD,T4GOOD      ;SETUP EXPECTED DATA
3639   011172  013777  002340  171010  LDRD4T::MOV     T4LOAD,@REG4       ;WRITE WORD INTO REGISTER 4
3640   011200  017737  171004  002344  READT4::MOV     @REG4,T4READ       ;READ WORD BACK FROM REGISTER 4
3641   011206  023737  002342  002344          CMP     T4GOOD,T4READ      ;COMPARE WORD EXPECTED WITH READ
3642   011214  000207                          RTS     PC                 ;RETURN WITH CONDITION CODES SET
3643
3644                             ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF TARGET EMULATOR CONTROL REGISTER 6.
3645                             ;CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION.
3646
3647   011216  013777  002346  170766  LDRDT6::MOV     T6LOAD,@REG6       ;WRITE WORD INTO REGISTER 6
3648   011224  017737  170762  002350  READT6::MOV     @REG6,T6READ       ;READ THE WORD BACK
3649   011232  043737  002352  002350          BIC     T6MASK,T6READ      ;CLEAR OUT ANY UNWANTED BITS
3650   011240  023737  002346  002350          CMP     T6LOAD,T6READ      ;COMPARE DATA LOADED WITH DATA READ
3651   011246  000207                          RTS     PC                 ;EXIT WITH CONDTION CODES SET
3652
```

```
3653                                    ;********************************************************************************
3654                                    ;
3655                                    ;           MDE/T-11 MEMORY SIMULATOR SUBROUTINES USED BY THE PROGRAM
3656                                    ;
3657                                    ;********************************************************************************
3658
3659
3660                                    ;ROUTINE TO SELECT THE MEMORY SIMULATOR MODULE
3661
3662    011250  010146                  SLCTMS::MOV     R1,-(SP)                ;SAVE CPU REGISTER 0
3663    011252  013701   002204                 MOV     REG0,R1                 ;GET DEVICE'S REGISTER 0 ADDRESS
3664    011256  113761   002235  000001         MOVB    SOLOAD+1,1(R1)          ;LOAD USER DEFINED DEVICE NUMBER
3665    011264  012601                          MOV     (SP)+,R1                ;RESTORE CPU REGISTER
3666    011266  000207                          RTS     PC                      ;RETURN BACK TO PROGRAM
3667
3668                                    ;ROUTINE TO PULSE THE SIGNAL 'RST H'.  A PULSE ON 'RST H' WILL PRESET
3669                                    ;THE RDV AND WRV FLIP-FLOP'S TO A ONE.  WHEN THE FLIP-FLOP'S ARE SET TO
3670                                    ;A ONE, THE SIGNAL 'BRK L' WILL BE ASSERTED HIGH, THUS NO BREAK CONDITION
3671                                    ;IS GENERATED.
3672
3673    011270                          MSRSTH::BGNSEG
3674    011270  104404                          TRAP    C$BSEG
3675    011272  052737   000001  002234         BIS     #RSTH,SOLOAD            ;SETUP BIT TO SET RST H TO HIGH STATE
3676    011300  042737   000060  002240         BIC     #RDVH!WRVH,SOMASK       ;SETUP TO EXPECT RDV + WRV F/F'S A 0
3677    011306  004737   010506                 JSR     PC,LDRDS0               ;GO LOAD, READ AND CHECK REG 0
3678    011312  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
3679    011314                                  ERRDF   1,,SOEROR               ;MEM SIM CONTROL REG 0 NOT = EXPECTED
3680    011314  104455                          TRAP    C$ERDF
3681    011316  000001                          .WORD   1
3682    011320  000000                          .WORD   0
3683    011322  005306                          .WORD   SOEROR
3684    011324                                  CKLOOP
3685    011324  104406                          TRAP    C$CLP1
3686    011326  042737   000001  002234 1$:     BIC     #RSTH,SOLOAD            ;SETUP BIT TO SET RST H TO LOW STATE
3687    011334  004737   010506                 JSR     PC,LDRDS0               ;GO LOAD, READ AND CHECK REGISTER 0
3688    011340  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
3689    011342                                  ERRDF   1,,SOEROR               ;MEM SIM CONTROL REG 0 NOT = EXPECTED
3690    011342  104455                          TRAP    C$ERDF
3691    011344  000001                          .WORD   1
3692    011346  000000                          .WORD   0
3693    011350  005306                          .WORD   SOEROR
3694    011352                          2$:     ENDSEG
3695    011352                          10003$:
3696    011352  104405                          TRAP    C$ESEG
3697    011354  000207                          RTS     PC                      ;RETURN BACK TO TEST
3698
3699                                    ;THE FOLLOWING ROUTINE WILL LOAD, READ AND CHECK THE MEMORY SIMULATOR
3700                                    ;MAP PROTECTION RAM.  THE MAP PROTECTION RAM WILL BE SETUP TO ALLOW
3701                                    ;READS AND WRITES IN THE FIRST 16K WORDS OF MEMORY SIMULATOR RAM.  THE
3702                                    ;FIRST 16K OF MEMORY WILL INCLUDE ADDRESSES 0 TO 077776. ALL ADDRESSESS
3703                                    ;ABOVE 16K WILL BE SETUP TO CAUSE A READ OR WRITE VIOLATION IF ADDRESSED.
3704                                    ;ALL MEMORY WILL BE MAPPED TO THE MEMORY SIMULATOR MODULE.
3705
3706    011356                          MPRAM:: BGNSEG
3707    011356  104404                          TRAP    C$BSEG
3708
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3709  011360  005037  002254              CLR     S4LOAD                  ;SETUP STARTING MSAD 15:0 ADDRESS
3710  011364  012737  000010  002244      MOV     #MSEL1,S2LOAD           ;SETUP STARTING MSAD 17:16 ADDRESS AND
3711                                                                       ;BITS TO SELECT MAP PROTECTION RAM
3712
3713                                        ;TOGGLE THE SIGNAL "RST H" IN CONTROL REGISTER 0 AND SET THE SIGNAL
3714                                        ;"MP H" TO A ONE.  APULSE ON THE SIGNAL "RST H" WILL PRESET THE "RDV" AND
3715                                        ;"WRV" FLIP-FLOPS TO A ONE, THUS SETTING THE SIGNAL "BRK L" TO THE HIGH
3716                                        ;STATE.  SETTING THE SIGNAL "MP H" TO A ONE WILL ENABLE MAP PROTECTION
3717                                        ;RAM BITS "MPIN H", "WRE H", AND "RDE H" TO THE SYSTEM BUS AS SIGNALS
3718                                        ;"ETR H", "WVIOL H", AND "RDE L" RESPECTIVELY.  THE SIGNAL "BRK L" WILL
3719                                        ;BE ENABLED TO THE SYSTEM BUS AS THE SIGNAL "MSBRK H" VIA THE SIGNAL
3720                                        ;"MP H".  SETTING THE SIGNAL "MP H" TO A ONE WILL ALSO ENABLE THE
3721                                        ;SIGNALS "MPIN H", "WRE H" AND "BRK L" TO CONTROL REGISTER 2 AS SIGNALS
3722                                        ;"ESR H", "WREN H" AND "MSBRK H" RESPECTIVELY.
3723
3724  011372  112737  000005  002234      MOVB    #RSTH!MPH,SOLOAD        ;SETUP BITS TO BE LOADED
3725  011400  004737  011270              JSR     PC,MSRSTH               ;PULSE RST H AND SET MP H TO A ONE
3726
3727  011404                        1$:   BGNSEG
3728  011404  104404                      TRAP    C$BSEG
3729
3730                                        ;SET THE SIGNAL MSEL1 H TO A ONE AND THE SIGNAL MSELO H TO A ZERO.
3731                                        ;SETTING THESE SIGNALS TO THE STATES MENTIONED WILL CAUSE THE MAP
3732                                        ;PROTECTION RAM TO BE SELECTED AND ADDRESSED ON A WRITE OR READ COMMAND
3733                                        ;TO CONTROL REGISTER 6 VIA THE SIGNAL "SMPM H".  MSAD BITS 17 AND 16
3734                                        ;IN CONTROL REGISTER 2 WILL BE LOADED AND CHECKED FOR THE ADDRESS BEING
3735                                        ;TESTED.
3736
3737  011406  012737  177540  002250      MOV     #177540,S2MASK          ;SETUP TO IGNORE UNWANTED BITS ON READ
3738  011414  004737  010546              JSR     PC,LDRDS2               ;GO LOAD, READ AND CHECK CONTROL REG 2
3739  011420  001405                      BEQ     2$                      ;IF LOADED OK THEN CONTINUE
3740  011422                              ERRDF   2,,S2EROR               ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
3741  011422  104455                      TRAP    C$ERDF
3742  011424  000002                      .WORD   2
3743  011426  000000                      .WORD   0
3744  011430  005322                      .WORD   S2EROR
3745  011432                              CKLOOP
3746  011432  104406                      TRAP    C$CLP1
3747
3748                                        ;LOAD, READ AND CHECK CONTROL REGISTER 4 FOR THE ADDRESS TO BE TESTED.
3749                                        ;CONTROL REGISTER 4 CONTAINS BITS FOR MSAD ADDRESSES 15:0.
3750
3751  011434  004737  010606        2$:   JSR     PC,LDRDS4               ;LOAD, READ AND CHECK CONTROL REGISTER 4
3752  011440  001405                      BEQ     3$                      ;IF LOADED OK THEN CONTINUE
3753  011442                              ERRDF   3,MSADRG,S4EROR         ;MSAD 15:0 REGISTER ERROR
3754  011442  104455                      TRAP    C$ERDF
3755  011444  000003                      .WORD   3
3756  011446  002510                      .WORD   MSADRG
3757  011450  005336                      .WORD   S4EROR
3758  011452                              CKLOOP
3759  011452  104406                      TRAP    C$CLP1
3760
3761                                        ;LOAD READ AND CHECK MAP PROTECTION RAM LOCATION ADDRESSED BY MSAD BITS
3762                                        ;17:0.  ADDRESSES 0 TO 077400 WILL BE LOADED AND CHECKED WITH A DATA
3763                                        ;PATTERN OF 17.  ADDRESSES OVER 077400 WILL BE LOADED AND CHECKED WITH
3764                                        ;A DATA PATTERN OF 11.
```

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3765
3766  011454  012737  177760  002264  3$:    MOV    #177760,S6MASK           ;SETUP TO CHECK ONLY LOWER 4 BITS
3767  011462  012737  000011  002260         MOV    #MUTB!MPINH,S6LOAD        ;SETUP DATA PATTERN OF 11
3768  011470  032737  000003  002244         BIT    #MSAD17!MSAD16,S2LOAD     ;CHECK IF ADDRESS ABOVE 16K WORDS
3769  011476  001006                         BNE    4$                       ;IF YES - LOAD R/W VIOLATION SETUP
3770  011500  005737  002254                 TST    S4LOAD                   ;CHECK IF OVER 16K WORDS
3771  011504  100403                         BMI    4$                       ;IF YES - LOAD R/W VIOLATION SETUP
3772  011506  052737  000006  002260         BIS    #WREH!RDEH,S6LOAD        ;SETUP TO ALLOW R/W TO 1ST 16K WORDS
3773  011514  004737  010632          4$:    JSR    PC,LDRDS6                ;LOAD,READ AND CHECK MAP PROTECT RAM
3774  011520  001405                         BEQ    5$                       ;IF LOADED OK THEN CONTINUE
3775  011522                                 ERRDF  4,MSGMP,S6ALLR           ;MAP PROTECT RAM DATA ERROR
3776  011522  104455                         TRAP   C$ERDF
3777  011524  000004                         .WORD  4
3778  011526  002603                         .WORD  MSGMP
3779  011530  005456                         .WORD  S6ALLR
3780  011532                                 CKLOOP
3781  011532  104406                         TRAP   C$CLP1
3782
3783                                  ;CHECK MAP PROTECT RAM DATA BITS 'MPIN H' AND 'WRE H' IN CONTROL
3784                                  ;REGISTER 2 AS 'ESR H' AND 'WREN H' RESPECTIVELY.
3785
3786  011534  042737  000140  002250  5$:    BIC    #ESRH!WRENH,S2MASK       ;SETUP TO CHECK ESR H AND WREN H
3787  011542  052737  000140  002246         BIS    #ESRH!WRENH,S2GOOD       ;EXPECT ESR H AND WREN H TO BE ONES
3788  011550  032737  000006  002260         BIT    #WREH!RDEH,S6LOAD        ;CHECK IF RAM WAS W/R ENABLED
3789  011556  001003                         BNE    6$                       ;IF YES THEN GO READ CONTROL REGISTER 2
3790  011560  042737  000100  002246         BIC    #WRENH,S2GOOD            ;THIS ADDRESS WAS NOT WRITE ENABLED
3791  011566  004737  010562          6$:    JSR    PC,READS2                ;GO READ AND CHECK CONTROL REGISTER 2
3792  011572  001404                         BEQ    7$                       ;IF OK THEN CONTINUE
3793  011574                                 ERRDF  2,MSGMPL,S2ALLR          ;REGISTER 2 NOT EQUAL EXPECTED
3794  011574  104455                         TRAP   C$ERDF
3795  011576  000002                         .WORD  2
3796  011600  002460                         .WORD  MSGMPL
3797  011602  005442                         .WORD  S2ALLR
3798  011604                          7$:    ENDSEG
3799  011604                       10005$:
3800  011604  104405                         TRAP   C$ESEG
3801
3802                                  ;UPDATE THE ADDRESSES MSAD 15:0 AND MSAD 17:16
3803
3804  011606  062737  000400  002254         ADD    #MSAD8,S4LOAD            ;UPDATE MSAD BITS 15:8 BY ONE
3805  011614  001273                         BNE    1$                       ;IF NOT 0 THEN GO LOAD NEXT RAM LOCATION
3806  011616  005237  002244                 INC    S2LOAD                   ;UPDATE MSAD BITS 17:16 BY ONE
3807  011622  032737  000004  002244         BIT    #MSEL0,S2LOAD            ;CHECK IF RAM LOCATIONS DONE
3808  011630  001665                         BEQ    1$                       ;IF NOT THEN LOAD NEXT LOCATION
3809  011632  005337  002244                 DEC    S2LOAD                   ;RESET CONTROL REG 2 VALUE TO ACTUAL
3810  011636                                 ENDSEG
3811  011636                       10004$:
3812  011636  104405                         TRAP   C$ESEG
3813
3814  011640  000207                         RTS    PC                       ;RETURN BACK TO THE TEST
3815
3816                                  ;THE FOLLOWING ROUTINE WILL SELECT MODULE SELECT RAM 0 AND LOAD DATA
3817                                  ;PATTERNS 1, 2, 4, 10, 0, 0, 0, AND 0 INTO CONSECUTIVE LOCATIONS OF
3818                                  ;MODULE SELECT RAM 0 STARTING AT ADDRESS 0 OF MODULE SELECT RAM 0.
3819                                  ;MODULE SELECT RAM 0 WILL BE SETUP TO SELECT THE FIRST 16K WORDS OF
3820                                  ;MEMORY STARTING AT ADDRESS 0 AND ENDING WITH ADDRESS 0777760.
```

```
3821
3822   011642   012737  000001  002260  MSRAM0::MOV    #BIT0,S6LOAD             ;SETUP STARTING PATTERN TO BE 1
3823   011650   005037  002254          CLR    S4LOAD                           ;SET STARTING ADDRESS TO BE 0
3824
3825   011654                   1$:     BGNSEG
3826   011654   104404                   TRAP   C$BSEG
3827
3828                                     ;SET CONTROL REGISTER 2 BIT ''MSEL0 H'' TO A ONE AND BITS ''MSEL1 H'',
3829                                     ;''MSAD17 H'' AND ''MSAD16 H'' TO ZEROES.  ''MSEL0 H'' ON A ONE AND ''MSEL1 H''
3830                                     ;ON A ZERO WILL CAUSE THE SIGNAL ''SMDS0 L'' TO BE ASSERTED ON A WRITE OR
3831                                     ;READ COMMAND TO CONTROL REGISTER 6.  ''SMDS0 L'' WILL SELECT MODULE
3832                                     ;SELECT RAM 0.
3833
3834   011656   012737  000004  002244          MOV    #MSEL0,S2LOAD            ;SETUP BITS TO BE LOADED
3835   011664   012737  177540  002250          MOV    #177540,S2MASK           ;SETUP REGISTER 2 MASK WORD
3836   011672   004737  010546                  JSR    PC,LDRDS2                ;LOAD, READ AND CHECK CONTROL REG 2
3837   011676   001405                          BEQ    2$                       ;IF LOADED OK THEN CONTINUE
3838   011700                                   ERRDF  2,,S2EROR                ;REGISTER 2 NOT EQUAL EXPECTED
3839   011700   104455                          TRAP   C$ERDF
3840   011702   000002                          .WORD  2
3841   011704   000000                          .WORD  0
3842   011706   005322                          .WORD  S2EROR
3843   011710                                   CKLOOP
3844   011710   104406                          TRAP   C$CLP1
3845
3846                                     ;LOAD THE ADDRESS OF MODULE SELECT RAM 0 TO BE TESTED INTO CONTROL
3847                                     ;REGISTER 4.  CONTROL REGISTER 4 MSAD BITS 15:13 ARE USED TO SELECT
3848                                     ;THE ADDRESS OF MODULE SELECT RAM 0.
3849
3850   011712   004737  010606          2$:     JSR    PC,LDRDS4                ;LOAD, READ AND CHECK CONTROL REG 4
3851   011716   001405                          BEQ    3$                       ;IF LOADED OK THEN CONTINUE
3852   011720                                   ERRDF  3,MSADRG,S4EROR          ;MSAD 15:0 REGISTER ERROR
3853   011720   104455                          TRAP   C$ERDF
3854   011722   000003                          .WORD  3
3855   011724   002510                          .WORD  MSADRG
3856   011726   005336                          .WORD  S4EROR
3857   011730                                   CKLOOP
3858   011730   104406                          TRAP   C$CLP1
3859
3860                                     ;WRITE THE DATA PATTERN INTO MODULE SELECT RAM 0 AND CHECK THAT THE
3861                                     ;PATTERN WAS LOADED CORRECTLY.  THE FOLLOWING PATTERN WILL BE WRITTEN
3862                                     ;INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS
3863                                     ;0; 1, 2, 4, 10, 0, 0, 0, AND 0.  THESE PATTERNS WILL CAUSE THE FIRST
3864                                     ;16K WORDS OF THE MEMORY SIMULATOR MEMORY TO BE SELECTED WHEN ADDRESSED.
3865
3866   011732   012737  177760  002264  3$:     MOV    #177760,S6MASK           ;SETUP TO IGNORE UNWANTED BITS
3867   011740   004737  010632                  JSR    PC,LDRDS6                ;LOAD, READ AND CHECK MODULE SELECT RAM 0
3868   011744   001404                          BEQ    4$                       ;IF LOADED OK THEN CONTINUE
3869   011746                                   ERRDF  4,MSGMS0,S6ALLR          ;DATA ERROR IN MODULE SELECT RAM 0
3870   011746   104455                          TRAP   C$ERDF
3871   011750   000004                          .WORD  4
3872   011752   002641                          .WORD  MSGMS0
3873   011754   005456                          .WORD  S6ALLR
3874   011756                   4$:     ENDSEG
3875   011756                   10006$:
3876   011756   104405                          TRAP   C$ESEG
```

```
3877
3878   011760  006337  002260                ASL     S6LOAD             ;UPDATE MODULE SELECT RAM 0 DATA PATTERN
3879   011764  043737  002264  002260         BIC     S6MASK,S6LOAD      ;IF PATTERN WAS 20 THEN SET IT TO 0
3880   011772  062737  020000  002254         ADD     #MSAD13,S4LOAD     ;UPDATE ADDRESS TO MODULE SELECT RAM 0
3881   012000  001325                         BNE     1$                 ;IF NOT 0 LOAD NEXT ADDRESS OF RAM 0
3882   012002  162737  020000  002254         SUB     #MSAD13,S4LOAD     ;RESET WORD TO ACTUAL MSAD ADDRESS
3883   012010  000207                         RTS     PC                 ;RETURN BACK TO THE TEST
3884
3885                                    ;THE FOLLOWING ROUTINE WILL SELECT MODULE SELECT RAM 1 AND LOAD THE
3886                                    ;DATA PATTERNS 17, 0, 0 AND 0 INTO CONSECUTIVE LOCATIONS OF MODULE
3887                                    ;SELECT RAM 1 STARTING AT ADDRESS 0.  MODULE SELECT RAM 1 WILL BE SETUP
3888                                    ;TO SELECT THE FIRST 32K WORDS OF MEMORY SIMULATOR RAM STARTING AT
3889                                    ;ADDRESS 0 AND ENDING WITH ADDRESS 177776.
3890
3891   012012  012737  000017  002260  MSRAM1::MOV     #17,S6LOAD         ;SETUP STARTING DATA PATTERN
3892   012020  012737  000001  002262         MOV     #1,S6GOOD          ;WHEN A PATTERN OF ALL 1'S IS LOADED,
3893                                                                      ;A PATTERN OF 1 WILL BE READBACK FROM RAM
3894   012026  012737  000014  002244         MOV     #MSEL1!MSELO,S2LOAD ;SETUP STARTING ADDRESS (MSAD 17:16=0)
3895
3896   012034                          1$:    BGNSEG
3897   012034  104404                         TRAP    C$BSEG
3898
3899                                    ;SET CONTROL REGISTER 2 BITS 'MSEL1 H' AND 'MSELO H' TO ONES AND 'MSAD17 H'
3900                                    ;AND 'MSAD16 H' TO MODULE SELECT RAM 1'S ADDRESS TO BE TESTED.  'MSEL1 H'
3901                                    ;AND 'MSELO H' SET TO ONES WILL CAUSE THE SIGNAL 'SMDS1 L' TO BE ASSERTED
3902                                    ;ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.  THE SIGNAL 'SMDS1 L'
3903                                    ;WILL SELECT MODULE SELECT RAM 1.
3904
3905   012036  012737  177540  002250         MOV     #177540,S2MASK     ;SETUP TO IGNORE UNWANTED BITS
3906   012044  004737  010546                 JSR     PC,LDRDS2          ;LOAD, READ AND CHECK CONTROL REG 2
3907   012050  001405                         BEQ     2$                 ;IF LOADED OK THEN CONTINUE
3908   012052                                 ERRDF   2,,S2EROR          ;REGISTER 2 NOT EQUAL EXPECTED
3909   012052  104455                         TRAP    C$ERDF
3910   012054  000002                         .WORD   2
3911   012056  000000                         .WORD   0
3912   012060  005322                         .WORD   S2EROR
3913   012062                                 CKLOOP
3914   012062  104406                         TRAP    C$CLP1
3915
```

```
3916
3917                                    ;WRITE THE DATA PATTERN INTO MODULE SELECT RAM 1 AND CHECK THAT THE
3918                                    ;CORRECT PATTERN WAS LOADED CORRECTLY.  THE FOLLOWING DATA PATTERN WILL
3919                                    ;BE WRITTEN INTO CONSECUTIVE LOCATIONS OF MODULE SEELECT RAM 1 STARTING
3920                                    ;AT ADDRESS 0; 17, 0, 0 AND 0.  THESE PATTERNS WILL CAUSE THE FIRST 32K
3921                                    ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
3922
3923  012064  012737 177760 002264 2$:  MOV     #177760,S6MASK       ;SETUP TO IGNORE UNWANTED BITS
3924  012072  004737 010640           JSR     PC,LDRD6S            ;LOAD READ + CHECK MODULE SELECT RAM 1
3925  012076  001404                  BEQ     3$                  ;IF LOADED OK THEN CONTINUE
3926  012100                          ERRDF   4,MSGMS1,S6ALLR      ;DATA ERROR IN MODULE SELECT RAM 1
3927  012100  104455                  TRAP    C$ERDF
3928  012102  000004                  .WORD   4
3929  012104  002703                  .WORD   MSGMS1
3930  012106  005456                  .WORD   S6ALLR
3931  012110                     3$:  ENDSEG
3932  012110                 10007$:
3933  012110  104405                  TRAP    C$ESEG
3934
3935  012112  005037 002260           CLR     S6LOAD              ;SET DATA PATTERN TO 0 AFTER 1ST LOAD
3936  012116  005037 002262           CLR     S6GOOD              ;EXPECT PATTERN OF 0 TO BE READ
3937  012122  005237 002244           INC     S2LOAD              ;UPDATE MODULE SELECT RAM 1 ADDRESS BY 1
3938  012126  032737 000004 002244    BIT     #MSEL0,S2LOAD       ;CHECK IF ALL ADDRESSES WRITTEN
3939  012134  001737                  BEQ     1$                  ;IF NOT THEN LOAD NEXT ADDRESS
3940  012136  005337 002244           DEC     S2LOAD              ;RESET ADDRESS TO ACTUAL ADDRESS LOADED
3941  012142  000207                  RTS     PC                  ;RETURN BACK TO THE TEST BEING EXECUTED
```

```
3942                                    ;*********************************************************************************
3943                                    ;
3944                                    ;        MDE/T-11 STATE ANALYZER SUBROUTINES USED BY THE PROGRAM
3945                                    ;
3946                                    ;*********************************************************************************
3947
3948                                            ;ROUTINE TO SELECT THE STATE ANALYZER MODULE
3949
3950    012144  010146                  SLCTED::MOV     R1,-(SP)                ;SAVE CPU REGISTER 0
3951    012146  013701  002204                  MOV     REG0,R1                 ;GET DEVICE'S REGISTER 0 ADDRESS
3952    012152  113761  002273  000001          MOVB    EOLOAD+1,1(R1)          ;LOAD USER DEFINED DEVICE NUMBER
3953    012160  012601                          MOV     (SP)+,R1                ;RESTOR CPU REGISTER 0
3954    012162  000207                          RTS     PC                      ;RETURN BACK TO PROGRAM
3955
3956                                            ;THE FOLLOWING ROUTINE WILL LOAD THE STATE ANALYZER'S PDAL REGISTER
3957                                            ;WITH THE WORD FOLLOWING THE CALL TO THIS ROUTINE.
3958
3959    012164  012537  002300          LDPDAL::MOV     (R5)+,E2LOAD            ;GET THE WORD TO BE LOADED
3960    012170                                  BGNSEG
3961    012170  104404                          TRAP    C$BSEG
3962    012172  004737  010732                  JSR     PC,LDRDE2               ;LOAD, READ AND CHECK CONTROL REGISTER 2
3963    012176  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
3964    012200                                  ERRDF   6,PDALRG,E2EROR         ;PDAL REGISTER NOT EQUAL WORD LOADED
3965    012200  104455                          TRAP    C$ERDF
3966    012202  000006                          .WORD   6
3967    012204  003034                          .WORD   PDALRG
3968    012206  006162                          .WORD   E2EROR
3969    012210                          1$:     ENDSEG
3970    012210                          10010$:
3971    012210  104405                          TRAP    C$ESEG
3972    012212  000205                          RTS     R5                      ;RETURN BACK TO THE TEST BEING PERFORMED
3973
3974
```

```
3975                                    ;********************************************************************************
3976                                    ;
3977                                    ;       MDE/T-11 TARGET EMULATOR SUBROUTINES USED BY THE PROGRAM
3978                                    ;
3979                                    ;********************************************************************************
3980
3981                                            ;ROUTINE TO SELECT THE TARGET EMULATOR MODULE
3982
3983    012214  010146                  SLCTTE::MOV     R1,-(SP)                :SAVE CPU REGISTER 0
3984    012216  013701  002204                  MOV     REG0,R1                 ;GET DEVICE'S REGISTER 0 ADDRESS
3985    012222  113761  002325  000001          MOVB    TOLOAD+1,1(R1)          ;LOAD USER DEFINED DEVICE NUMBER
3986    012230  012601                          MOV     (SP)+,R1                ;RESTOR CPU REGISTER 0
3987    012232  000207                          RTS     PC                      ;RETURN BACK TO PROGRAM
3988
3989                                    ;THE FOLLOWING ROUTINE WILL SELECT THE POINTER REGISTER SPECIFIED BY THE WORD
3990                                    ;FOLLOWING THE CALL TO THIS ROUTINE.  THE REGISTER SELECTED WILL NOT BE ACCESSED
3991                                    ;UNTIL A WRITE OR READ COMMAND IS ISSUED TO TARGET EMULATOR CONTROL REGISTER 6.
3992                                    ;THE EXTENDED REGISTER WILL BE SELECTED BY GDAL BITS 2:0 IN TARGET EMULATOR
3993                                    ;CONTROL REGISTER 0.  THE REGISTERS SELECTED BY GDAL BITS 2:0 ARE AS FOLLOWS:
3994                                    ;       ADDRES - GDAL 2:0 = 0 - WRITE DIAGNOSTIC ADDRESS REGISTER (WPT0)
3995                                    ;                               READ ADDRESS BUS (RPT0)
3996                                    ;       FJADR  - GDAL 2:0 = 1 - WRITE NEW FORCE JUMP ADDRESS REGISTER (WPT1)
3997                                    ;                               READ FORCE JUMP ADDRESS READBACK REGISTER (RPT1)
3998                                    ;       FDAL   - GDAL 2:0 = 2 - WRITE FDAL AND EOAI REGISTERS (WPT2)
3999                                    ;                               READ FDAL/EOAI REGISTERS OR FDAL/CTL REGISTERS (RPT2)
4000                                    ;       HDAL   - GDAL 2:0 = 3 - WRITE/READ HDAL REGISTER (WPT3/RPT3)
4001                                    ;       MODE   - GDAL 2:0 = 4 - WRITE/READ MODE REGISTER (WPT4/RPT4)
4002                                    ;       TARMOD - GDAL 2:0 = 5 - READ TARGET MODE REGISTER (RPT5)
4003                                    ;       EIDAL  - GDAL 2:0 = 6 - READ EIDAL BUS (RPT6)
4004                                    ;       EODAL  - GDAL 2:0 = 7 - READ EODAL BUS (RPT7)
4005                                    ;THE ROUTINE IS CALLED IN THE FOLLOWING WAY WITH THE REGISTER TO BE SELECTED IN
4006                                    ;THE LOCATION AFTER THE CALL
4007                                    ;
4008                                    ;       JSR     R5,SELTER       :CALL TO THIS ROUTINE
4009                                    ;       .WORD   ADDRES          ;WORD TO SELECT THE EXTENDED REGISTER
4010
4011    012234                          SELTER::BGNSEG
4012    012234  104404                          TRAP    C$BSEG
4013    012236  111537  002324                  MOVB    (R5),TOLOAD             ;GET THE REGISTER BITS TO BE SELECTED
4014    012242  004737  011100                  JSR     PC,LDRDT0               ;GO LOAD, READ AND CHECK GDAL REGISTER
4015    012246  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
4016                                            ERRDF   9,GDALRG,TOEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
4017    012250  104455                          TRAP    C$ERDF
4018    012252  000011                          .WORD   9
4019    012254  003640                          .WORD   GDALRG
4020    012256  006666                          .WORD   TOEROR
4021    012260                          1$:     ENDSEG
4022    012260
4023    012260  104405                  10011$: TRAP    C$ESEG
4024    012262  005725                          TST     (R5)+                   ;UPDATE RETURN POINTER TO PROGRAM
4025    012264  000205                          RTS     R5                      ;RETURN BACK TO THE TEST
4026
4027                                    ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL12 IN THE HDAL REGISTER.  HDAL12
4028                                    ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNALS ''XRAS L'' AND
4029                                    ;''XRAS H''.  HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL
4030                                    ;THE T-11 TIMING AND CONTROL SIGNALS.
```

```
4031
4032   012266  004737  012300      XRAS::  JSR     PC,XRASH            ;GO SET XRAS H (HIGH) AND XRAS L (LOW)
4033   012272  004737  012332              JSR     PC,XRASL            ;GO SET XRAS H (LOW) AND XRAS L (HIGH)
4034   012276  000207                      RTS     PC                 ;RETURN BACK TO TEST
4035
4036                                ;THE FOLLOWING ROUTINE WILL SET HDAL12 H AND HDAL2 H TO ONES.  HDAL2 H ON A ONE
4037                                ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
4038                                ;HDAL12 H ON A ONE WILL CAUSE THE SIGNAL XRAS H TO BE ASSERTED HIGH AND THE
4039                                ;SIGNAL XRAS L TO BE ASSERTED LOW
4040
4041   012300                      XRASH:: BGNSEG
4042   012300  104404                      TRAP    C$BSEG
4043   012302  052737  010004  002346      BIS     #HDAL12!HDAL2,T6LOAD  ;SETUP BIT TO BE LOADED
4044   012310  004737  011216              JSR     PC,LDRDT6          ;GO LOAD, READ AND CHECK HDAL REGISTER
4045   012314  001404                      BEQ     1$                 ;IF LOADED OK THEN CONTINUE
4046   012316                              ERRDF   12,HDALRG,T06ERR   ;HDAL REGISTER NOT EQUAL EXPECTED
4047   012316  104455                      TRAP    C$ERDF
4048   012320  000014                      .WORD   12
4049   012322  003756                      .WORD   HDALRG
4050   012324  006732                      .WORD   T06ERR
4051   012326                      1$:     ENDSEG
4052   012326                      10012$:
4053   012326  104405                      TRAP    C$ESEG
4054   012330  000207                      RTS     PC                 ;RETURN BACK TO TEST
4055
4056                                ;THE FOLLOWING ROUTINE WILL SET HDAL12 H TO A ZERO AND HDAL2 H TO A ONE.
4057                                ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND
4058                                ;CONTROL SIGNALS.  HDAL12 H ON A ZERO WILL CAUSE THE SIGNAL XRAS H TO BE
4059                                ;ASSERTED LOW AND THE SIGNAL XRAS L TO BE ASSERTED HIGH.
4060
4061   012332                      XRASL:: BGNSEG
4062   012332  104404                      TRAP    C$BSEG
4063   012334  052737  000004  002346      BIS     #HDAL2,T6LOAD      ;SETUP DIAGNOSTIC CONTROL BIT
4064   012342  042737  010000  002346      BIC     #HDAL12,T6LOAD     ;SETUP BIT TO BE CLEARED
4065   012350  004737  011216              JSR     PC,LDRDT6          ;GO LOAD, READ AND CHECK HDAL REGISTER
4066   012354  001404                      BEQ     1$                 ;IF LOADED OK THEN CONTINUE
4067   012356                              ERRDF   12,HDALRG,T06ERR   ;HDAL REGISTER NOT EQUAL EXPECTED
4068   012356  104455                      TRAP    C$ERDF
4069   012360  000014                      .WORD   12
4070   012362  003756                      .WORD   HDALRG
4071   012364  006732                      .WORD   T06ERR
4072   012366                      1$:     ENDSEG
4073   012366                      10013$:
4074   012366  104405                      TRAP    C$ESEG
4075   012370  000207                      RTS     PC                 ;RETURN BACK TO TEST
4076
4077                                ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL13 IN THE HDAL REGISTER.  HDAL13
4078                                ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNALS ''XCAS L'' AND
4079                                ;''XCAS H''.  HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL
4080                                ;THE T-11 TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
4081
4082   012372  004737  012404      XCAS::  JSR     PC,XCASH           ;GO SET XCAS H (HIGH) AND XCAS L (LOW)
4083   012376  004737  012436              JSR     PC,XCASL           ;GO SET XCAS H (LOW) AND XCAS L (HIGH)
4084   012402  000207                      RTS     PC
4085
4086                                ;THE FOLLOWING ROUTINE WILL SET HDAL13 H AND HDAL2 H TO ONES.  HDAL2 H ON A ONE
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```
4087                                     ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.  HDAL13 H
4088                                     ;ON A ONE WILL CAUSE THE SIGNAL XCAS H TO BE ASSERTED HIGH AND THE SIGNAL XCAS L
4089                                     ;TO BE ASSERTED LOW.
4090
4091    012404                     XCASH:: BGNSEG
4092    012404   104404                   TRAP    C$BSEG
4093    012406   052737  020004  002346   BIS     #HDAL13!HDAL2,T6LOAD     ;SETUP BITS TO BE LOADED
4094    012414   004737  011216           JSR     PC,LDRDT6               ;GO LOAD, READ AND CHECK HDAL REGISTER
4095    012420   001404                   BEQ     1$                     ;IF LOADED OK THEN CONTINUE
4096    012422                            ERRDF   12,HDALRG,T06ERR       ;HDAL REGISTER NOT EQUAL EXPECTED
4097    012422   104455                   TRAP    C$ERDF
4098    012424   000014                   .WORD   12
4099    012426   003756                   .WORD   HDALRG
4100    012430   006732                   .WORD   T06ERR
4101    012432                     1$:     ENDSEG
4102    012432                     10014$:
4103    012432   104405                   TRAP    C$ESEG
4104    012434   000207                   RTS     PC
4105
4106                                     ;THE FOLLOWING ROUTINE WILL SET HDAL13 H TO A ZERO AND HDAL2 H TO A ONE.
4107                                     ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND
4108                                     ;CONTROL SIGNALS.  HDAL13 H ON A ZERO WILL CAUSE THE SIGNAL XCAS H TO BE
4109                                     ;ASSERTED LOW AND THE SIGNAL XCAS L TO BE ASSERTED HIGH.
4110
4111    012436                     XCASL:: BGNSEG
4112    012436   104404                   TRAP    C$BSEG
4113    012440   052737  000004  002346   BIS     #BIT2,T6LOAD           ;SETUP DIAGNOSTIC CONTROL BIT
4114    012446   042737  020000  002346   BIC     #HDAL13,T6LOAD         ;SETUP BIT TO BE CLEARED
4115    012454   004737  011216           JSR     PC,LDRDT6             ;GO LOAD, READ AND CHECK HDAL REGISTER
4116    012460   001404                   BEQ     1$                     ;IF LOADED OK THEN CONTINUE
4117    012462                            ERRDF   12,HDALRG,T06ERR       ;HDAL REGISTER NOT EQUAL EXPECTED
4118    012462   104455                   TRAP    C$ERDF
4119    012464   000014                   .WORD   12
4120    012466   003756                   .WORD   HDALRG
4121    012470   006732                   .WORD   T06ERR
4122    012472                     1$:     ENDSEG
4123    012472                     10015$:
4124    012472   104405                   TRAP    C$ESEG
4125    012474   000207                   RTS     PC                     ;RETURN BACK TO TEST
4126
4127                                     ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL15 IN THE HDAL REGISTER.  HDAL15
4128                                     ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNAL "XPI H".
4129                                     ;HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL THE T-11
4130                                     ;TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
4131
4132    012476   004737  012510   XPI::    JSR     PC,XPIH               ;GO SET PPI L AND XPI L TO THE LOW STATE
4133    012502   004737  012542           JSR     PC,XPIL               ;GO SET PPI L AND XPI L TO HIGH STATE
4134    012506   000207                   RTS     PC                     ;RETURN BACK TO TEST
4135
4136                                     ;THE FOLLOWING ROUTINE WILL SET HDAL15 H AND HDAL2 H TO ONES.  HDAL2 H ON A ONE
4137                                     ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.  HDAL15 H
4138                                     ;ON A ONE WILL ASSERT THE SIGNALS PPI L AND XPI L TO THE LOW STATE.
4139
4140    012510                     XPIH::   BGNSEG
4141    012510   104404                   TRAP    C$BSEG
4142    012512   052737  100004  002346   BIS     #HDAL15!HDAL2,T6LOAD   ;SETUP BITS TO BE LOADED
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4143  012520  004737  011216           JSR    PC,LDRDT6           ;GO LOAD, READ AND CHECK HDAL REGISTER
4144  012524  001404                    BEQ    1$                 ;IF LOADED OK THEN CONTINUE
4145  012526                            ERRDF  12,HDALRG,T06ERR   ;HDAL REGISTER NOT EQUAL EXPECTED
4146  012526  104455                    TRAP   C$ERDF
4147  012530  000014                    .WORD  12
4148  012532  003756                    .WORD  HDALRG
4149  012534  006732                    .WORD  T06ERR
4150  012536                     1$:    ENDSEG
4151  012536                     10016$:
4152  012536  104405                    TRAP   C$ESEG
4153  012540  000207                    RTS    PC                 ;RETURN BACK TO TEST
4154
4155                             ;THE FOLLOWING ROUTINE WILL SET HDAL15 H TO A ZERO AND HDAL2 H TO A ONE.  HDAL2 H
4156                             ;ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
4157                             ;HDAL15 H ON A ZERO WILL CAUSE THE SIGNALS PPI L AND XPI L TO BE ASSERTED HIGH.
4158
4159  012542                     XPIL:: BGNSEG
4160  012542  104404                    TRAP   C$BSEG
4161  012544  052737  000004  002346    BIS    #HDAL2,T6LOAD      ;SETUP DIAGNOSTIC CONTROL BIT
4162  012552  042737  100000  002346    BIC    #HDAL15,T6LOAD     ;SETUP BIT TO BE CLEARED
4163  012560  004737  011216            JSR    PC,LDRDT6          ;GO LOAD, READ AND CHECK HDAL REGISTER
4164  012564  001404                    BEQ    1$                 ;IF LOADED OK THEN CONTINUE
4165  012566                            ERRDF  12,HDALRG,T06ERR   ;HDAL REGISTER NOT EQUAL EXPECTED
4166  012566  104455                    TRAP   C$ERDF
4167  012570  000014                    .WORD  12
4168  012572  003756                    .WORD  HDALRG
4169  012574  006732                    .WORD  T06ERR
4170  012576                     1$:    ENDSEG
4171  012576                     10017$:
4172  012576  104405                    TRAP   C$ESEG
4173  012600  000207                    RTS    PC                 ;RETURN BACK TO TEST
4174
4175                             ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL7 IN THE HDAL REGISTER.  HDAL7
4176                             ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNAL XBCLR H + PBCLR H.
4177                             ;HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL THE T-11
4178                             ;TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
4179
4180  012602  004737  012614    XBCLR:: JSR    PC,XBCLRH          ;SET XBCLR H AND PBCLR H TO HIGH STATE
4181  012606  004737  012646            JSR    PC,XBCLRL          ;SET XBCLR H AND PBCLR H TO LOW STATE
4182  012612  000207                    RTS    PC                 ;RETURN BACK TO TEST
4183
4184                             ;THE FOLLOWING ROUTINE WILL SET HDAL7 H AND HDAL2 H TO ONES.  HDAL2 H ON A ONE
4185                             ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.  HDAL7 H
4186                             ;ON A ONE WILL ASSERT THE SIGNALS XBCLR H AND PBCLR H TO THE HIGH STATE
4187
4188  012614                     XBCLRH::BGNSEG
4189  012614  104404                    TRAP   C$BSEG
4190  012616  052737  000204  002346    BIS    #HDAL7!HDAL2,T6LOAD ;SETUP BITS TO BE LOADED
4191  012624  004737  011216            JSR    PC,LDRDT6          ;GO LOAD, READ AND CHECK HDAL REGISTER
4192  012630  001404                    BEQ    1$                 ;IF LOADED OK THEN CONTINUE
4193  012632                            ERRDF  12,HDALRG,T06ERR   ;HDAL REGISTER NOT EQUAL EXPECTED
4194  012632  104455                    TRAP   C$ERDF
4195  012634  000014                    .WORD  12
4196  012636  003756                    .WORD  HDALRG
4197  012640  006732                    .WORD  T06ERR
4198  012642                     1$:    ENDSEG
```

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4199  012642                         10020$:
4200  012642  104405                        TRAP    C$ESEG
4201  012644  000207                        RTS     PC                          ;RETURN BACK TO TEST
4202
4203                                  ;THE FOLLOWING ROUTINE WILL SET HDAL7 H TO A ZERO AND HDAL2 H TO A ONE.  HDAL2 H
4204                                  ;ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
4205                                  ;HDAL7 H ON A ZERO WILL CAUSE THE SIGNALS XBCLR H AND PBCLR H TO BE ASSERTED LOW
4206
4207  012646                         XBCLRL::BGNSEG
4208  012646  104404                        TRAP    C$BSEG
4209  012650  052737  000004  002346        BIS     #HDAL2,T6LOAD               ;SETUP DIAGNOSTIC CONTROL BIT
4210  012656  042737  000200  002346        BIC     #HDAL7,T6LOAD               ;SETUP BIT TO BE CLEARED
4211  012664  004737  011216              JSR     PC,LDRDT6                   ;GO LOAD, READ AND CHECK HDAL REGISTER
4212  012670  001404                        BEQ     1$                         ;IF LOADED OK THEN CONTINUE
4213  012672                                ERRDF   12,HDALRG,T06ERR           ;HDAL REGISTER NOT EQUAL EXPECTED
4214  012672  104455                        TRAP    C$ERDF
4215  012674  000014                        .WORD   12
4216  012676  003756                        .WORD   HDALRG
4217  012700  006732                        .WORD   T06ERR
4218  012702                         1$:    ENDSEG
4219  012702                         10021$:
4220  012702  104405                        TRAP    C$ESEG
4221  012704  000207                        RTS     PC                          ;RETURN BACK TO TEST
4222
4223                                  ;THE FOLLOWING ROUTINE WILL SET AND CLEAR VDAL2 H IN CONTROL REGISTER 4.  VDAL2 H
4224                                  ;ON A ONE WILL CLEAR THE FOLLOWING FLIP-FLOPS:
4225                                  ;     PAUSE STATE WORKING         PSM H   0
4226                                  ;     PAUSE STATE SYNC            EPSF H  0
4227                                  ;     16 BIT ADDRESS              EPFN H  0
4228                                  ;     8 BIT INSTRUCTION HB        EP8F H  0
4229                                  ;     8 BIT ADDRESS LB            EP8G H  0
4230                                  ;     8 BIT ADDRESS HB            EP8N H  0
4231                                  ;     TAKE NEW F.J. ADDRESS       TNFI H  0
4232                                  ;     GET NEW ADDRESS FLIP-FLOP   OUT NEW H
4233                                  ;     PAUSE MODE FLIP-FLOP        PAUSE L 0
4234                                  ;     REFRESH FLIP-FLOP           REFR H  0
4235                                  ;     FETCT LATCH FLIP-FLOP       EDFET H 0
4236                                  ;SETTING AND CLEARING VDAL2 H WILL ALSO CLOCK THE TAI AND TDAL BUSSES INTO THE
4237                                  ;DIAGNOSTIC LATCHES.
4238
4239  012706                         CLRPSM::BGNSEG
4240  012706  104404                        TRAP    C$BSEG
4241  012710  052737  000004  002340        BIS     #VDAL2,T4LOAD              ;SETUP BIT TO SET VDAL2 H TO A ONE
4242  012716  004737  011164              JSR     PC,LDRDT4                   ;GO LOAD, READ AND CHECK VDAL REGISTER
4243  012722  001405                        BEQ     1$                         ;IF ALL OTHER BITS CLEARED THEN CONT
4244  012724                                ERRDF   11,VDALRG,T4EROR           ;VDAL REG OR PAUSE STATE MACHINE ERROR
4245  012724  104455                        TRAP    C$ERDF
4246  012726  000013                        .WORD   11
4247  012730  003710                        .WORD   VDALRG
4248  012732  006716                        .WORD   T4EROR
4249  012734                                CKLOOP
4250  012734  104406                        TRAP    C$CLP1
4251  012736  042737  000004  002340  1$:   BIC     #VDAL2,T4LOAD              ;SETUP TO CLEAR VDAL2 H
4252  012744  004737  011164              JSR     PC,LDRDT4                   ;GO LOAD, READ AND CHECK VDAL REGISTER
4253  012750  001404                        BEQ     2$                         ;IF LOADED OK THEN CONTINUE
4254  012752                                ERRDF   11,VDALRG,T4EROR           ;VDAL OR PAUSE STATE MACHINE ERROR
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4255  012752  104455                          TRAP     C$ERDF
4256  012754  000013                          .WORD    11
4257  012756  003710                          .WORD    VDALRG
4258  012760  006716                          .WORD    T4EROR
4259  012762                          2$:     ENDSEG
4260  012762                          10022$:
4261  012762  104405                          TRAP     C$ESEG
4262  012764  000207                          RTS      PC                        ;RETURN BACK TO TEST
4263
4264                          ;THE FOLLOWING ROUTINE WILL SET ADAL0 H TO A ONE AND THEN ZERO.  ADAL0 H BEING
4265                          ;SET AND CLEARED WILL CAUSE A PULSE ON THE SIGNAL 'BRKRES L'.  THE SIGNAL
4266                          ;'BRKRES L' WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP AND INTERRUPT RELATED
4267                          ;LOGIC.
4268
4269  012766                  BRKRES::BGNSEG
4270  012766  104404                          TRAP     C$BSEG
4271  012770  052737  000001  002334          BIS      #ADAL0,T2LOAD           ;SETUP BIT TO BE LOADED
4272  012776  004737  011140                  JSR      PC,LDRDT2               ;GO LOAD, READ AND CHECK ADAL REGISTER
4273  013002  001405                           BEQ      1$                      ;IF LOADED OK THEN CONTINUE
4274  013004                          ERRDF    10,ADALRG,T2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
4275  013004  104455                          TRAP     C$ERDF
4276  013006  000012                          .WORD    10
4277  013010  003664                          .WORD    ADALRG
4278  013012  006702                          .WORD    T2EROR
4279  013014                          CKLOOP
4280  013014  104406                          TRAP     C$CLP1
4281  013016  042737  000001  002334  1$:     BIC      #ADAL0,T2LOAD           ;SETUP BIT TO BE CLEARED
4282  013024  004737  011140                  JSR      PC,LDRDT2               ;GO LOAD, READ AND CHECK ADAL REGISTER
4283  013030  001404                           BEQ      2$                      ;IF LOADED OK THEN CONTINUE
4284  013032                          ERRDF    10,ADALRG,T2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
4285  013032  104455                          TRAP     C$ERDF
4286  013034  000012                          .WORD    10
4287  013036  003664                          .WORD    ADALRG
4288  013040  006702                          .WORD    T2EROR
4289  013042                          2$:     ENDSEG
4290  013042                          10023$:
4291  013042  104405                          TRAP     C$ESEG
4292  013044  000207                          RTS      PC                        ;RETRUN BACK TO TEST
4293
4294                          ;TARGET EMULATOR INTERRUPT SERVICE ROUTINE
4295
4296  013046                          BGNSRV   INTSRV
4297  013046                  INTSRV::
4298  013046  017737  167132  002332          MOV      @REG0,TOREAD            ;READ GDAL REGISTER AND SAVE
4299  013054  012702  177777                  MOV      #-1,R2                  ;SET SOFTWARE INTERRUPT FLAG
4300  013060                          ENDSRV   #PRI07
4301  013060                          L10025:
4302  013060  142766  000340  000002          BICB     #340,2(SP)
4303  013066  152766  000340  000002          BISB     #PRI07,2(SP)
4304  013074  000002                          RTI
4305
4306  013076                          ENDMOD
4307
```

```
4308                                     .TITLE MISCELLANEOUS SECTIONS
4309                                     .SBTTL  REPORT CODING SECTION
4310
4311    013076                                   BGNMOD
4312
4313                             ;++
4314                             ; THE REPORT CODING SECTION CONTAINS THE
4315                             ; "PRINTS" CALLS THAT GENERATE STATISTICAL REPORTS.
4316                             ;--
4317
4318    013076                                   BGNRPT
4319    013076                     L$RPT::
4320
4321
4322    013076                                   EXIT    RPT
4323    013076  000167                           .WORD   J$JMP
4324    013100  000000                           .WORD   L10026-2-.
4325
4326
4327                                             .EVEN
4328
4329    013102                                   ENDRPT
4330    013102                     L10026:
4331    013102  104425                           TRAP    C$RPT
4332
4333                             .SBTTL  PROTECTION TABLE
4334
4335                             ;++
4336                             ; THIS TABLE IS USED BY THE RUNTIME SERVICES
4337                             ; TO PROTECT THE LOAD MEDIA.
4338                             ;--
4339
4340    013104                                   BGNPROT
4341    013104                     L$PROT::
4342
4343    013104  177777                           -1              ;OFFSET INTO P-TABLE FOR CSR ADDRESS
4344    013106  177777                           -1              ;OFFSET INTO P-TABLE FOR MASSBUS ADDRESS
4345    013110  177777                           -1              ;OFFSET INTO P-TABLE FOR DRIVE NUMBER
4346
4347    013112                                   ENDPROT
4348
```

```
4349                                          .SBTTL   INITIALIZE SECTION
4350
4351                                  ;++
4352                                  ; THE INITIALIZE SECTION CONTAINS THE CODING THAT IS PERFORMED
4353                                  ; AT THE BEGINNING OF EACH PASS.
4354                                  ;--
4355
4356    013112                                BGNINIT
4357    013112                        L$INIT::
4358    013112                                READEF   #EF.START          ;SEE IF A START COMMAND
4359    013112   012700   000040             MOV      #EF.START,RO
4360    013116   104447                      TRAP     C$REFG
4361    013120                                BCOMPLETE          1$       ;BRANCH IF START COMMAND
4362    013120   103410                      BCS      1$
4363    013122                                READEF   #EF.RESTART        ;SEE IF A RESTART COMMAND
4364    013122   012700   000037             MOV      #EF.RESTART,RO
4365    013126   104447                      TRAP     C$REFG
4366    013130                                BCOMPLETE          1$       ;BRANCH IF RESTART
4367    013130   103404                      BCS      1$
4368    013132                                READEF   #EF.PWR            ;SEE IF RECOVERING FROM A POWER FAIL
4369    013132   012700   000034             MOV      #EF.PWR,RO
4370    013136   104447                      TRAP     C$REFG
4371    013140                                BNCOMPLETE         2$       ;IF NOT CHECK IN CONTINUE
4372    013140   103014                      BCC      2$
4373    013142                        1$:     BRESET                      ;ISSUE A BUS RESET
4374    013142   104433                      TRAP     C$RESET
4375    013144                                SETVEC   #100,#102,#RTI     ;SETUP CLOCK VECTOR TO DO A RETURN
4376    013144   012746   000002             MOV      #RTI,-(SP)
4377    013150   012746   000102             MOV      #102,-(SP)
4378    013154   012746   000100             MOV      #100,-(SP)
4379    013160   012746   000003             MOV      #3,-(SP)
4380    013164   104437                      TRAP     C$SVEC
4381    013166   062706   000010             ADD      #10,SP
4382    013172                        2$:     READEF   #EF.NEW            ;SEE IF A NEW PASS
4383    013172   012700   000035             MOV      #EF.NEW,RO
4384    013176   104447                      TRAP     C$REFG
4385    013200                                BNCOMPLETE         3$       ;IF NOT GO CHECK IF CONTINUE
4386    013200   103003                      BCC      3$
4387    013202   012737   177777   002232    MOV      #-1,UNITNB         ;SETUP TO INIT UNIT NUMBER
4388    013210                        3$:     READEF   #EF.CONTINUE       ;CHECK IF CONTINUE
4389    013210   012700   000036             MOV      #EF.CONTINUE,RO
4390    013214   104447                      TRAP     C$REFG
4391    013216                                BCOMPLETE          6$       ;IF YES THEN EXIT
4392    013216   103444                      BCS      6$
4393    013220   005237   002232    4$:       INC      UNITNB            ;INC TO NEW UNIT NUMBER
4394    013224                                GPHARD   UNITNB,R5          ;GET DEVICE INFORMATION
4395    013224   013700   002232             MOV      UNITNB,RO
4396    013230   104442                      TRAP     C$GPHRD
4397    013232   010005                      MOV      RO,R5
4398    013234                                BNCOMPLETE         4$       ;GO TRY ANOTHER UNIT
4399    013234   103371                      BCC      4$
4400    013236   012701   002204             MOV      #REGO,R1           ;ADDRESS OF SA DEVICE ADDRESS TABLE
4401    013242   005002                      CLR      R2                 ;CLEAR OFFSET TO ADD TO TABLE ADDRESS
4402    013244   011511            5$:        MOV      (R5),(R1)          ;GET ADDRESS AND SAVE
4403    013246   060221                      ADD      R2,(R1)+           ;ADD OFFSET TO ADDRESS
4404    013250   005202                      INC      R2                 ;UPDATE OFFSET BY 2
```

```
4405  013252  005202                  INC    R2                    ;
4406  013254  022702  000010          CMP    #10,R2                ;CHECK IF DONE LOADING TABLE
4407  013260  001371                  BNE    5$                    ;GO UPDATE NEXT ADDRESS
4408  013262  005725                  TST    (R5)+                 ;UPDATE THE POINTER
4409  013264  012521                  MOV    (R5)+,(R1)+           ;SAVE TARGET EMULATOR VECTOR ADDRESS
4410  013266  005011                  CLR    (R1)                  ;CLEAR MEMORY SIMULATOR DEVICE NUMBER
4411  013270  105721                  TSTB   (R1)+                 ;UPDATE POINTER TO HIGH BYTE
4412  013272  111521                  MOVB   (R5),(R1)+            ;SAVE MEMORY SIMULATOR DEVICE NUMBER
4413  013274  005725                  TST    (R5)+                 ;UPDATE POINTER TO NEXT PARAMETER
4414  013276  012721  100400          MOV    #IDH!SIG8H,(R1)+      ;SAVE MEMORY SIMULATOR DEVICE TYPE #
4415  013302  005011                  CLR    (R1)                  ;CLEAR STATE ANALYZER DEVICE NUMBER
4416  013304  105721                  TSTB   (R1)+                 ;UPDATE POINTER TO HIGH BYTE
4417  013306  111521                  MOVB   (R5),(R1)+            ;SAVE STATE ANALYZER DEVICE NUMBER
4418  013310  005725                  TST    (R5)+                 ;UPDATE POINTER TO NEXT PARAMETER
4419  013312  012721  101000          MOV    #CDAL15!CDAL9,(R1)+   ;SAVE STATE ANALYZER DEVICE TYPE #
4420  013316  005011                  CLR    (R1)                  ;CLEAR TARGET EMULATOR DEVICE NUMBER
4421  013320  105721                  TSTB   (R1)+                 ;UPDATE POINTER TO HIGH BYTE
4422  013322  111521                  MOVB   (R5),(R1)+            ;SAVE TARGET EMULATOR DEVICE NUMBER
4423  013324  012711  100000          MOV    #GDAL15,(R1)          ;SAVE TARGET EMULATOR DEVICE TYPE #
4424  013330                  6$:     SETPRI #PRI07               ;RAISE PROCESSOR PRIORITY
4425  013330  012700  000340          MOV    #PRI07,R0
4426  013334  104441                  TRAP   C$SPRI
4427
4428
4429  013336                          EXIT   INIT
4430  013336  104432                  TRAP   C$EXIT
4431  013340  000002                  .WORD  L10030-.
4432
4433
4434                                  .EVEN
4435
4436  013342                          ENDINIT
4437  013342          L10030:
4438  013342  104411                  TRAP   C$INIT
4439
4440                          .SBTTL  AUTODROP SECTION
4441
4442                          ;++
4443                          ; THIS CODE IS EXECUTED IMMEDIATELY AFTER THE INITIALIZE CODE IF
4444                          ; THE "ADR" FLAG WAS SET.  THE UNIT(S) UNDER TEST ARE CHECKED TO
4445                          ; SEE IF THEY WILL RESPOND.  THOSE THAT DON'T ARE IMMEDIATELY
4446                          ; DROPPED FROM TESTING.
4447                          ;--
4448
4449  013344                          BGNAUTO
4450  013344          L$AUTO::
4451
4452
4453  013344                          ENDAUTO
4454  013344          L10031:
4455  013344  104461                  TRAP   C$AUTO
```

```
4456                                     .SBTTL  CLEANUP CODING SECTION
4457
4458                                     ;++
4459                                     ; THE CLEANUP CODING SECTION CONTAINS THE CODING THAT IS PERFORMED
4460                                     ; AFTER THE HARDWARE TESTS HAVE BEEN PERFORMED.
4461                                     ;--
4462
4463    013346                           BGNCLN
4464    013346                   L$CLEAN::
4465    013346                           SETPRI  #PRIO7                  ;RAISE THE CPU PRIORITY LEVEL TO 7
4466    013346  012700  000340           MOV     #PRIO7,RO
4467    013352  104441                   TRAP    C$SPRI
4468    013354                           BRESET                          ;DO A RESET TO CLEAR ALL MDE/T-11 MODULES
4469    013354  104433                   TRAP    C$RESET
4470
4471    013356                           EXIT    CLN
4472    013356  104432                   TRAP    C$EXIT
4473    013360  000002                   .WORD   L10032-.
4474
4475
4476                                     .EVEN
4477
4478    013362                           ENDCLN
4479    013362                   L10032:
4480    013362  104412                   TRAP    C$CLEAN
4481
4482                                     .SBTTL  DROP UNIT SECTION
4483
4484                                     ;++
4485                                     ; THE DROP-UNIT SECTION CONTAINS THE CODING THAT CAUSES A DEVICE
4486                                     ; TO NO LONGER BE TESTED.
4487                                     ;--
4488
4489    013364                           BGNDU
4490    013364                   L$DU::
4491
4492
4493    013364                           EXIT    DU
4494    013364  000167                   .WORD   J$JMP
4495    013366  000000                   .WORD   L10033-2-.
4496
4497
4498                                     .EVEN
4499
4500    013370                           ENDDU
4501    013370                   L10033:
4502    013370  104453                   TRAP    C$DU
```

```
4503                                    .SBTTL  ADD UNIT SECTION
4504
4505                                    ;++
4506                                    ; THE ADD-UNIT SECTION CONTAINS ANY CODE THE PROGRAMMER WISHES
4507                                    ;  TO BE EXECUTED IN CONJUNCTION WITH THE ADDING OF A UNIT BACK
4508                                    ;  TO THE TEST CYCLE.
4509                                    ;--
4510
4511    013372                                  BGNAU
4512    013372                          L$AU::
4513
4514
4515    013372                                  EXIT    AU
4516    013372   000167                         .WORD   J$JMP
4517    013374   000000                         .WORD   L10034-2-.
4518
4519
4520                                            .EVEN
4521
4522    013376                                  ENDAU
4523    013376                          L10034:
4524    013376   104452                         TRAP    C$AU
4525
4526    013400                                  ENDMOD
4527
```

```
4528                              .TITLE HARDWARE TESTS
4529
4530                              .SBTTL  TEST 1: INITIALIZE ALL MDE/T-11 SYSTEM MODULES
4531
4532    013400                    BGNMOD
4533
4534                       ;++
4535                       ;       THIS TEST WILL BE EXECUTED AS THE FIRST TEST IN THE PROGRAM AND AT THE
4536                       ;       BEGINNING OF EACH TEST IN THE PROGRAM.  THE PURPOSE OF THIS TEST IS TO
4537                       ;       INITIALIZE THE MDE/T-11 MODULES (MEMORY SIMULATOR, STATE ANALYZER AND TARGET
4538                       ;       EMULATOR) TO A KNOWN STATE.  THE TEST SEQUENCE IS DESCRIBED BELOW.
4539                       ;
4540                       ;       MDE/T-11 MEMORY SIMULATOR MODULE INITIALIZATION SEQUENCE:
4541                       ;
4542                       ;       1.    LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVICE NUMBER TO
4543                       ;             SELECT THE MEMORY SIMULATOR MODULE.
4544                       ;       2.    LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
4545                       ;             AND THE BIT TO SET THE SIGNAL "RST H" TO THE HIGH STATE.  WHEN
4546                       ;             THE SIGNAL "RST H" IS SET HIGH, THE "RDV" AND "WRV" FLIP-FLOPS
4547                       ;             WILL BE PRESET TO A ONE THUS CAUSING THE SIGNALS "RDV H" AND
4548                       ;             "WRV H" TO BE ASSERTED LOW.  THE SIGNALS "RDV H" AND "WRV H"
4549                       ;             SHOULD BE READ AS ZEROES WHEN CONTROL REGISTER 0 IS READ.
4550                       ;       3.    LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
4551                       ;             AND BIT 15 SET TO A ONE.  THE BIT WHICH SET THE SIGNAL "RST H"
4552                       ;             TO THE HIGH STATE WILL BE CLEARED THUS SETTING THE SIGNAL LOW.
4553                       ;             WHEN BIT 15 IS SET TO A ONE, THE DEVICE TYPE WILL BE READ BACK
4554                       ;             ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE DEVICE
4555                       ;             NUMBER.
4556                       ;       4.    CLEAR BIT 15 IN CONTROL REGISTER 0 AND THEN READ AND CHECK
4557                       ;             CONTROL REGISTER 0 FOR THE DEVICE NUMBER.
4558                       ;       5.    LOAD, READ AND CHECK CONTROL REGISTER 2'S READ/WRITE BITS 3:0
4559                       ;             WITH A DATA PATTERN OF ZEROES.  THESE BITS WILL SET THE SIGNALS
4560                       ;             MSEL1 H, MSEL0 H, MSAD17 H, AND MSAD16 H TO THE LOW STATE.  THE
4561                       ;             READ ONLY SIGNALS MSBRK H, WREN H, AND ESR H WILL BE IGNORED AT
4562                       ;             THIS POINT IN TIME.
4563                       ;       6.    LOAD, READ AND CHECK CONTROL REGISTER 4'S READ/WRITE BITS 15:0
4564                       ;             WITH A DATA PATTERN OF ALL ZEROES.  THESE BITS WILL SET THE
4565                       ;             SIGNALS MSAD 15:0 H TO THE LOW STATE.
4566                       ;
4567                       ;       MDE/T-11 STATE ANALYZER MODULE INITIALIZATION
4568                       ;
4569                       ;       1.    LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVIE NUMBER TO
4570                       ;             SELECT THE STATE ANALYZER MODULE.
4571                       ;       2.    LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
4572                       ;             AND THE BIT TO SET THE SIGNAL "CDAL0 H" TO THE HIGH STATE.
4573                       ;             WHEN THE SIGNAL "CDAL0 H" IS SET HIGH, THE TRACE RAM ADDRESS
4574                       ;             REGISTER, THE TRACING AND SBL FLIP-FLOPS WILL BE CLEARED AND
4575                       ;             THE EVENT COUNTERS WILL BE LOADED WITH DATA FROM THE EVENT
4576                       ;             COUNTER REGISTERS.
4577                       ;       3.    LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
4578                       ;             AND THE BIT TO SET THE SIGNAL CDAL15 H TO A ONE.  THE BIT WHICH
4579                       ;             SET "CDAL0 H" TO THE HIGH STATE WILL BE CLEARED THUS SETTING THE
4580                       ;             SIGNAL "CDAL0 H" TO THE LOW STATE.  WHEN "CDAL15 H" IS SET TO A
4581                       ;             ONE, THE DEVICE TYPE WILL BE READ ON A READ COMMAND TO CONTROL
4582                       ;             REGISTER 0 INSTEAD OF THE DEVICE NUMBER.
4583                       ;       4.    CLEAR THE BIT WHICH SET "CDAL15 H" TO THE HIGH STATE AND THEN
```

D 8

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46   PAGE 94
CVCDDB.P11   14-JUN-82 09:54   TEST 1: INITIALIZE ALL MDE/T-11 SYSTEM MODULES   SEQ 0094

```
4584                    READ AND CHECK CONTROL REGISTER 0 FOR THE DEVICE NUMBER.
4585          5.        LOAD, READ AND CHECK CONTROL REGISTER 4'S PDAL REGISTER WITH
4586                    A DATA PATTERN OF ALL ZEROES.  THIS WILL CAUSE THE SIGNALS
4587                    'PDAL 7:0 H' TO BE ASSERTED LOW.  THIS WILL ALSO CAUSE THE
4588                    SIGNAL PTER0 L TO BE ASSERTED LOW IN THE POINTER REGISTER.
4589
4590                    MDE/T-11 TARGET EMULATOR MODULE INITIALIZATION
4591
4592          1.        LOAD HIGH BYTE OF CONTROL REGISTER 0 WITH THE DEVICE NUMBER TO
4593                    SELECT THE TARGET EMULATOR MODULE.
4594          2.        LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
4595                    AND ALL READ/WRITE BITS SET TO A ZERO.  THE READ ONLY SIGNALS
4596                    SSBRK H, TOBRK H, AND MEMBRK H WILL BE IGNORED DURING THE
4597                    READING OF CONTROL REGISTER 0.
4598          3.        LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
4599                    AND THE BIT TO SET THE SIGNAL 'GDAL15 H' TO THE HIGH STATE.
4600                    WHEN THE SIGNAL 'GDAL15 H' IS SET HIGH (1), THE DEVICE TYPE WILL
4601                    BE READ ON A READ COMMAND TO CONTROL REGISTER 0 INSTEAD OF THE
4602                    DEVICE NUMBER.
4603          4.        SET THE SIGNAL 'GDAL15 H' TO THE LOW STATE BY CLEARING THE BIT
4604                    IN CONTROL REGISTER 0. ALSO SET THE READ/WRITE BITS 'GDAL1 H'
4605                    AND 'GDAL0 H' TO A ONE.  ALL OTHER READ/WRITE BITS WILL BE
4606                    LOADED WITH ZEROES.  WHEN 'GDAL2 H' IS SET TO A ZERO AND THE
4607                    SIGNALS 'GDAL1 H' AND 'GDAL0 H' ARE SET TO ONES, THE HDAL
4608                    REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
4609                    CONTROL REGISTER 6.
4610          5.        LOAD, READ AND CHECK HDAL REGISTER WITH A DATA PATTERN OF 4
4611                    WHICH WILL CAUSE THE SIGNAL 'HDAL2 H' TO BE ASSERTED HIGH (1)
4612                    AND ALL OTHER HDAL BITS TO BE ASSERTED LOW (0).  WHEN 'HDAL2 H'
4613                    IS ASSERTED HIGH, THE PROGRAM CAN GENERATE THE T-11 TIMING AND
4614                    CONTROL SIGNALS.
4615          6.        LOAD, READ AND CHECK CONTROL REGISTER 0 WITH THE DEVICE NUMBER
4616                    AND WITH 'GDAL2 H' SET TO A ONE AND GDAL BITS 1 AND 0 SET TO A
4617                    ZERO.  THIS WILL CAUSE THE MODE REGISTER TO BE SELECTED ON A
4618                    WRITE OR READ COMMAND TO CONTROL REGISTER 6.
4619          7.        LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF
4620                    ALL ZEORES.  MODE REGISTER BIT MR11 H ON A ZERO WILL SELECT 16
4621                    BIT ADDRESS MODE.
4622          8.        LOAD, READ AND CHECK CONTROL REGISTER 2'S ADAL REGISTER WITH
4623                    ADAL0 H SET TO A ONE AND THEN A ZERO.  SETTING AND CLEARING THE
4624                    SIGNAL ADAL0 H WILL CAUSE A PULSE TO BE ISSUED ON THE SIGNAL
4625                    'BRKRES L'.  ALL OTHER ADAL REGISTER BITS WILL BE LOADED AND
4626                    CHECKED WITH ZEORES.  PULSING THE SIGNAL 'BRKRES L' WILL CLEAR
4627                    THE SINGLE STEP SYNC FLIP-FLOP, THE BREAK INTERRUPT LATCH FLIP-
4628                    FLOP, THE MEMORY SIMULATOR BREAK LATCH FLIP-FLOP (MEMBRK) AND
4629                    THE TIMEOUT BREAK ONE SHOT WILL BE RESET.
4630          9.        READ AND CHECK CONTROL REGISTER 0 TO CHECK THAT ALL THE BREAK
4631                    SIGNALS ARE READ AS ZEROES.  THESE SIGNALS ARE SSBRK H, TOBRK H,
4632                    MEMBRK H AND EDBRK H.
4633          10.       LOAD, READ AND CHECK CONTROL REGISTER 4'S VDAL REGISTER WITH
4634                    VDAL2 H SET TO A ONE AND THEN A ZERO.  ALL OTHER VDAL REGISTER
4635                    READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES.  SETTING
4636                    AND CLEARING THE SIGNAL VDAL2 H WILL CAUSE A PULSE TO BE ISSUED
4637                    ON THE SIGNAL INVD L.  A PULSE ON THE SIGNAL INVD L WILL CAUSE
4638                    ALL THE FLIP-FLOP'S AND SOME REGISTERS NOT CLEARED BY THE SIGNAL
4639                    'BRKRES L' PREVIOULSY TO BE INITIALIZED TO SOME PREDEFINED
```

E 8

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 95
CVCDDB.P11   14-JUN-82 09:54   TEST 1: INITIALIZE ALL MDE/T-11 SYSTEM MODULES   SEQ 0095

```
4640                              ;                    STATE.  THE READ ONLY BITS WILL BE CHECKED TO BE ZERO AS A
4641                              ;--                  RESULT OF THE SIGNAL "INVD L" BEING PULSED.
4642                              ;--
4643
4644
4645
4646  013400                              BGNTST
4647  013400                      T1::
4648  013400  004737  007440              JSR     PC,INITMD                  ;INITIALIZE MDE/T-11 SYSTEM MODULES
4649
4650
4651
4652
4653  013404                              ENDTST
4654  013404                      L10035:
4655  013404  104401                      TRAP    C$ETST
4656
```

F 8

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 96
CVCDDB.P11   14-JUN-82 09:54   TEST 2: CHECK ADDRESS BUS TO MS AND SA FROM TE   SEQ 0096

```
4657                                    .SBTTL   TEST 2: CHECK ADDRESS BUS TO MS AND SA FROM TE
4658
4659                             ;++
4660                             ;        THIS TEST WILL CHECK THAT THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS
4661                             ;        REGISTER AND ADDRESS BITS 17:16 CAN BE ENABLED TO THE SYSTEM ADDRESS
4662                             ;        BUS AND THAT THE ADDRESS BUS BITS 17:0 CAN BE CLOCKED INTO THE MEMORY
4663                             ;        SIMULATOR AND STATE ANALYZER SYSTEM BUS LATCHES FOR THESE BITS DURING
4664                             ;        A NORMAL T-11 TIMING CYCLE.  A NORMAL T-11 TIMING CYCLE OCCURS WHEN
4665                             ;        RAS, CAS AND PI ARE SET TO THEIR ASSERTED STATE IN THE ORDER LISTED AND
4666                             ;        THEN DEASSERTED IN THE FOLLOWING ORDER: CAS, PI AND RAS.   THE ADDRESS
4667                             ;        BUS DATA PATTERNS USED DURING THIS TEST ARE AS FOLLOWS: 577777, 252525,
4668                             ;        725252 AND 000000.   TARGET EMULATOR HDAL REGISTER BITS 14 AND 11 CONTROL
4669                             ;        THE STATE OF ADDRESS BITS 17 AND 16.
4670
4671                             ;        WHEN PRAS H IS SET HIGH, THE SIGNAL "ADVAL H" WILL BE SET HIGH THUS
4672                             ;        CLOCKING SYSTEM ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR SYSTEM
4673                             ;        ADDRESS BUS LATCHES.   WHEN XRAS H IS SET HIGH, THE SIGNALS "EDCK0 H" AND
4674                             ;        "EDCK1 H" WILL BE SET HIGH THUS CLOCKING SYSTEM ADDRESS BUS BITS 15:0
4675                             ;        INTO THE STATE ANALYZER'S SYSTEM ADDRESS BUS LATCHES FOR THESE BITS.
4676                             ;        WHEN XPI L IS SET LOW, THE SIGNAL "EDCK4 H" WILL BE SET HIGH THUS
4677                             ;        CLOCKING THE SYSTEM BUS SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H
4678                             ;        AND OBTS BITS 3:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE
4679                             ;        BITS.   ALL THE SIGNALS MENTIONED ABOVE ARE GENERATED ON THE TARGET
4680                             ;        EMULATOR MODULE.   THE PROGRAM WILL CHECK THAT SYSTEM ADDRESS BUS BITS
4681                             ;        17:0 WERE CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES
4682                             ;        BY ENABLING THE LATCHES TO MSAD BITS 17:0 VIA THE SIGNAL "CTS L" AND
4683                             ;        THEN READING AND CHECKING THESE BITS VIA CONTROL REGISTER 2 AND 4.   THE
4684                             ;        PROGRAM WILL CHECK THAT SYSTEM ADDRESS BUS BITS 17:0 AND THE SIGNALS
4685                             ;        XSEL1 H, EDSEL0 H, AND OBTS BITS 3:0 WERE CLOCKED INTO THE STATE
4686                             ;        ANALYZER SYSTEM BUS LATCHES FOR THESE BITS.   THE STATE ANALYZERS SYSTEM
4687                             ;        BUS LATCHES ARE ENABLED TO STATE ANALYZERS TRDI BUS BY SETTING THE
4688                             ;        SIGNAL "TRSL2 L" TO THE LOW STATE.   THE PROGRAM WILL THEN READ AND CHECK
4689                             ;        TRDI BUS BITS 15:0 AND 39:32 FOR THE SYSTEM BUS DATA.
4690                             ;--
4691
4692   013406                    BGNTST
4693   013406           T2::
4694   013406  004737  007440        JSR      PC,INITMD                  ;INITIALIZE MDE/T-11 SYSTEM MODULES
4695
4696   013412  012701  014224        MOV      #30$,R1                    ;DATA TABLE ADDRESS FOR TEST ADDRESSES 15:0
4697
4698   013416                    BGNSEG
4699   013416  104404            TRAP     C$BSEG
4700
4701   013420  005037  002320        CLR      E6MASK                     ;CLEAR REGISTER 6 MASK WORD FOR LOOPING
4702
4703                             ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
4704                             ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
4705
4706   013424  004737  012214        JSR      PC,SLCTTE                  ;SELECT TARGET EMULATOR MODULE
4707
4708                             ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL "BRKRES L"
4709                             ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
4710                             ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
4711                             ;THE SIGNAL "BRKRES L" VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
4712                             ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
```

G 8

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 97
CVCDDB.P11   14-JUN-82 09:54   TEST 2: CHECK ADDRESS BUS TO MS AND SA FROM TE   SEQ 0097

```
4713                                    ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED VIA THE
4714                                    ;THE SIGNAL "RASP L" LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
4715                                    ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
4716                                    ;THE SIGNAL XRAS H IS SET HIGH LATER IN THIS TEST.
4717
4718   013430  012737  043020  002334   MOV    #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
4719   013436  004737  012766           JSR    PC,BRKRES                    ;SET BITS 14, 10 + 9 AND TOGGLE ADALO H
4720
4721                                    ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
4722                                    ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
4723                                    ;REGISTER 6.
4724
4725   013442  004537  012234           JSR    R5,SELTER                    ;SELECT REGISTER SPECIFIED BY NEXT WORD
4726   013446  000003                   .WORD  HDAL                         ;SELECT THE HDAL REGISTER
4727
4728                                    ;SET HDAL REGISTER BITS 9 AND 2 TO A ONE AND HDAL BITS 14 AND 11 TO DATA
4729                                    ;PATTERN TO BE TESTED FOR ADDRESS BITS 17 AND 16.  HDAL2 H ON A ONE WILL
4730                                    ;ENABLE THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
4731                                    ;HDAL9 H ON A ONE WILL ENABLE THE DIGNOSTIC ADDRESS REGISTER ONTO THE
4732                                    ;ADDRESS BUS.  ADDRESS BUS BITS 17 AND 16 WILL BE LOADED WITH A TEST
4733                                    ;PATTERN VIA HDAL REGISTER BITS 14 AND 11 RESPECTIVELY.
4734
4735   013450  012737  001004  002346   MOV    #HDAL9!HDAL2,T6LOAD          ;SET HDAL9 H AND HDAL2 H TO ONES
4736   013456  056137  000010  002346   BIS    10(R1),T6LOAD                ;SETUP ADDRESS BITS 17 AND 16
4737   013464  004737  011216           JSR    PC,LDRDT6                    ;GO LOAD, READ AND CHECK HDAL REGISTER
4738   013470  001405                   BEQ    1$                           ;IF LOADED OK THEN CONTINUE
4739   013472                           ERRDF  12,HDALRG,T06ERR             ;HDAL REGISTER NOT EQUAL EXPECTED
4740   013472  104455                   TRAP   C$ERDF
4741   013474  000014                   .WORD  12
4742   013476  003756                   .WORD  HDALRG
4743   013500  006732                   .WORD  T06ERR
4744   013502                           CKLOOP
4745   013502  104406                   TRAP   C$CLP1
4746
4747                                    ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
4748                                    ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
4749                                    ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
4750
4751   013504  005037  002340    1$:    CLR    T4LOAD                       ;SETUP TO CLEAR ALL OTHER R/W BITS
4752   013510  004737  012706           JSR    PC,CLRPSM                    ;PULSE INVD L VIA VDAL2 H
4753
4754                                    ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON
4755                                    ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
4756                                    ;BE WRITTEN OR READ.
4757
4758   013514  004537  012234           JSR    R5,SELTER                    ;SELECT REGISTER SPECIFIED BY NEXT WORD
4759   013520  000004                   .WORD  MODE                         ;SELECT THE MODE REGISTER
4760
4761                                    ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
4762                                    ;ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
4763
4764   013522  005037  002346           CLR    T6LOAD                       ;SETUP TO CLEAR ALL MODE REGISTER BITS
4765   013526  004737  011216           JSR    PC,LDRDT6                    ;GO LOAD, READ AND CHECK MODE REGISTER
4766   013532  001405                   BEQ    2$                           ;IF LOADED OK THEN CONTINUE
4767   013534                           ERRDF  12,MODREG,T06ERR             ;MODE REGISTER NOT EQUAL EXPECTED
4768   013534  104455                   TRAP   C$ERDF
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H 8

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 98
CVCDDB.P11   14-JUN-82 09:54   TEST 2: CHECK ADDRESS BUS TO MS AND SA FROM TE   SEQ 0098

```
4769  013536  000014                      .WORD    12
4770  013540  004002                      .WORD    MODRFG
4771  013542  006732                      .WORD    TO6ERR
4772  013544                              CKLOOP
4773  013544  104406                      TRAP     C$CLP1
4774
4775                           ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
4776                           ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
4777                           ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDAL0 H
4778                           ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
4779                           ;TER WILL BE ADDRESSED.
4780
4781  013546  004537  012234       2$:    JSR      R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
4782  013552  000002                      .WORD    FDAL                 ;SELECT EOAI AND FDAL REGISTER
4783
4784                           ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER.  THE EOAI REGISTER WILL
4785                           ;BE LOADED AND CHECKED FOR ZEROES.  THE FDAL REGISTER WILL BE LOADED AND
4786                           ;CHECKED FOR A DATA PATTERN OF ONE (FDAL0 H = 1).
4787
4788  013554  012737  000001  002346      MOV      #FDAL0,T6LOAD        ;SETUP EOAI AND FDAL REG DATA PATTERN
4789  013562  004737  011216              JSR      PC,LDRDT6            ;GO LOAD, READ AND CHECK EOAI + FDAL REG
4790  013566  001405                      BEQ      3$                   ;IF LOADED OK THEN CONTINUE
4791  013570                              ERRDF    12,EOAIFD,TO6ERR     ;EOAI OR FDAL REGISTER ERROR
4792  013570  104455                      TRAP     C$ERDF
4793  013572  000014                      .WORD    12
4794  013574  004047                      .WORD    EOAIFD
4795  013576  006732                      .WORD    TO6ERR
4796  013600                              CKLOOP
4797  013600  104406                      TRAP     C$CLP1
4798
4799                           ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
4800                           ;2:0 TO A 0.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
4801                           ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.  THE DIAGNOSTIC
4802                           ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
4803                           ;BIT 9 BEING SET TO A ONE PREVIOULSY.  ON A READ COMMAND TO CONTROL
4804                           ;REGISTER 6, THE DIAGNOSTIC ADDRESS REGISTER WILL BE READBACK.
4805
4806  013602  004537  012234       3$:    JSR      R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
4807  013606  000000                      .WORD    ADDRES               ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
4808
4809                           ;LOAD READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH THE TEST PATTERN
4810                           ;FROM THE DATA TABLE ADDRESSES BY R1
4811
4812  013610  011137  002346              MOV      (R1),T6LOAD          ;GET THE TEST PATTERN FROM THE TABLE
4813  013614  004737  011216              JSR      PC,LDRDT6            ;GO LOAD, READ AND CHECK DIAG ADDRESS REG
4814  013620  001405                      BEQ      4$                   ;IF LOADED OK THEN CONTINUE
4815  013622                              ERRDF    12,ADDRRG,TO6ERR     ;DIAGNOSTIC ADDRESS REGISTER ERROR
4816  013622  104455                      TRAP     C$ERDF
4817  013624  000014                      .WORD    12
4818  013626  004144                      .WORD    ADDRRG
4819  013630  006732                      .WORD    TO6ERR
4820  013632                              CKLOOP
4821  013632  104406                      TRAP     C$CLP1
4822
4823                           ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3.  THE
4824                           ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
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I 8

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 99
CVCDDB.P11   14-JUN-82 09:54   TEST 2: CHECK ADDRESS BUS TO MS AND SA FROM TE   SEQ 0099

```
4825                                                    ;CONTROL REGISTER 6.
4826
4827  013634  004537  012234        4$:     JSR    R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
4828  013640  000003                        .WORD  HDAL                    ;SELECT THE HDAL REGISTER
4829
4830                                                    ;PERFORM A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE:
4831                                                    ;   1.   SET XRAS H AND PRAS H TO THE HIGH STATE
4832                                                    ;   2.   SET XCAS H AND PCAS H TO THE HIGH STATE
4833                                                    ;   3.   SET XPI L AND PPI L TO THE LOW STATE
4834                                                    ;   4.   SET XCAS H AND PCAS H TO THE LOW STATE
4835                                                    ;   5.   SET XPI L AND PPI L TO THE HIGH STATE
4836                                                    ;   6.   SET XRAS H AND PRAS H TO THE LOW STATE
4837                                                    ;PULSING THE SIGNAL PRAS H WILL CAUSE A PULSE TO BE ISSUED ON THE SIGNAL
4838                                                    ;"ADVAL H".  THE SIGNAL "ADVAL H" WILL CLOCK THE ADDRESS BUS SIGNALS
4839                                                    ;"ADDR 17:0" INTO THE MEMORY SIMULATOR ADDRESS LATCHES.  PULSING THE
4840                                                    ;SIGNAL XRAS H WILL CAUSE PULSES TO BE ISSUED ON THE SIGNALS "EDCK0 H"
4841                                                    ;"EDCK1 H".   THESE TWO PULSES WILL CLOCK THE ADDRESS BUS SIGNALS "ADDR
4842                                                    ;15:0" INTO THE STATE ANALYZER'S ADDRESS BUS LATCHES.  PULSING THE SIGNAL
4843                                                    ;XRAS H WILL ALSO CAUSE THE RASP ONE SHOT TO BE FIRED.  A PULSE WILL BE
4844                                                    ;ISSUED ON THE SIGNAL "CKAI H" AS A RESULT OF THE RASP ONE SHOT BEING
4845                                                    ;FIRED.   A PULSE ON THE SIGNAL "CKAI H" WILL CAUSE A PULSE ON THE SIGNAL
4846                                                    ;"EDCK5 H".   THE SIGNAL "EDCK5 H" WILL CLOCK THE CTL 7:0 BUS INTO THE
4847                                                    ;STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE BITS.  PULSING THE SIGNAL
4848                                                    ;XPI L WILL CAUSE A PULSE ON THE SIGNAL "EDCK4 H".  THE SIGNAL "EDCK4 H"
4849                                                    ;WILL CLOCK SYSTEM BUS SIGNALS "CTL 11:8" AND "BTS 3:0" INTO THE STATE
4850                                                    ;ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS.
4851
4852  013642  012737  001004  002346         MOV    #HDAL9!HDAL2,T6LOAD     ;SETUP PREVIOUSLY LOADED BITS
4853  013650  056137  000010  002346         BIS    10(R1),T6LOAD          ;
4854  013656  004737  012300                 JSR    PC,XRASH               ;SET XRAS H AND PRAS H TO HIGH STATE
4855  013662  004737  012404                 JSR    PC,XCASH               ;SET XCAS H AND PCAS H TO HIGH STATE
4856  013666  004737  012510                 JSR    PC,XPIH                ;SET XPI L AND PPI L TO THE LOW STATE
4857  013672  004737  012436                 JSR    PC,XCASL               ;SET XCAS H AND PCAS H TO LOW STATE
4858  013676  004737  012542                 JSR    PC,XPIL                ;SET XPI L AND PPI L TO THE HIGH STATE
4859  013702  004737  012332                 JSR    PC,XRASL               ;SET XRAS H AND PRAS H TO LOW STATE
4860
4861                                                    ;READ CONTROL REGISTER 0 TO CHECK THAT NO BREAK BITS ARE SET AS A RESULT
4862                                                    ;OF XRAS H AND PRAS H BEING PULSED.
4863
4864  013706  004737  011114                 JSR    PC,READT0              ;READ AND CHECK REGISTER 0
4865  013712  001405                         BEQ    5$                     ;IF OK THEN CONTINUE
4866  013714                                 ERRDF  9,GDALRG,TOEROR        ;GDAL REGISTER NOT EQUAL EXPECTED
4867  013714  104455                         TRAP   C$ERDF
4868  013716  000011                         .WORD  9
4869  013720  003640                         .WORD  GDALRG
4870  013722  006666                         .WORD  TOEROR
4871  013724                                 CKLOOP
4872  013724  104406                         TRAP   C$CLP1
4873
4874                                                    ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER).  THE SIGNAL EDEOC H
4875                                                    ;SHOULD BE SET TO A ONE.
4876
4877  013726  052737  000020  002342  5$:    BIS    #VDAL4,T4GOOD          ;CHECK THAT EDEOC H IS SET TO A ONE
4878  013734  004737  011200                 JSR    PC,READT4              ;READ AND CHECK VDAL REGISTER
4879  013740  001405                         BEQ    6$                     ;IF NO CHANGES THEN CONTINUE
4880  013742                                 ERRDF  11,VDALRG,T4EROR       ;VDAL OR PAUSE STATE MACHINE ERROR
```

```
4881   013742   104455                              TRAP    C$ERDF
4882   013744   000013                              .WORD   11
4883   013746   003710                              .WORD   VDALRG
4884   013750   006716                              .WORD   T4EROR
4885   013752                                       CKLOOP
4886   013752   104406                              TRAP    C$CLP1
4887
4888                                      ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
4889                                      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
4890
4891   013754   004737   011250    6$:    JSR     PC,SLCTMS               ;SELECT MEMORY SIMULATOR MODULE
4892
4893                                      ;SET THE SIGNAL CTS H TO A ONE IN CONTROL REGISTER 0 OF THE MEMORY
4894                                      ;SIMULATOR MODULE.  THIS WILL ENABLE THE SYSTEM BUS SIGNALS RECEIVED
4895                                      ;TO THE MEMORY SIMULATOR LOGIC.  IN THIS TEST, CTS H ON A ONE WILL
4896                                      ;ENABLE THE SYSTEM BUS ADDRESSES TO MEMORY SIMULATOR SIGNALS MSAD 17:0.
4897
4898   013760   112737   000002  002234  MOVB    #CTSH,SOLOAD            ;SETUP BIT TO SET CTS H TO A ONE
4899   013766   004737   010506          JSR     PC,LDRDS0              ;GO LOAD, READ AND CHECK REGISTER 0
4900   013772   001405                   BEQ     7$                     ;IF LOADED OK THEN CONTINUE
4901   013774                            ERRDF   1,,SOEROR              ;MEM SIM REG 0 NOT EQUAL EXPECTED
4902   013774   104455                   TRAP    C$ERDF
4903   013776   000001                   .WORD   1
4904   014000   000000                   .WORD   0
4905   014002   005306                   .WORD   SOEROR
4906   014004                            CKLOOP
4907   014004   104406                   TRAP    C$CLP1
4908
4909                                      ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE
4910                                      ;ADDRESSES CLOCKED INTO THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS
4911                                      ;REGISTER WAS CLOCKED INTO THE MEMORY SIMULATOR ADDRESS LATCHES BY THE
4912                                      ;SIGNAL "ADVAL H".  THE SIGNAL "ADVAL H" WAS GENERATED BY PULSING THE
4913                                      ;SIGNAL "PRAS H" ON THE TARGET EMULATOR MODULE.  THE MEMORY SIMULATOR'S
4914                                      ;ADDRESS LATCHES ARE ENABLED TO MSAD BITS 17:0 AS A RESULT OF CTS H
4915                                      ;BEING ASSERTED HIGH AND CTS L BEING ASSERTED LOW.
4916
4917   014006   011137   002254    7$:    MOV     (R1),S4LOAD            ;GET PATTERN LOADED INTO TARGET EMULATOR
4918   014012   004737   010614          JSR     PC,READS4              ;READ AND CHECK CONTROL REGISTER 4
4919   014016   001405                   BEQ     8$                     ;IF OK THEN CONTINUE
4920   014020                            ERRDF   3,TEMSAD,SO4ERR        ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
4921   014020   104455                   TRAP    C$ERDF
4922   014022   000003                   .WORD   3
4923   014024   002534                   .WORD   TEMSAD
4924   014026   005406                   .WORD   SO4ERR
4925   014030                            CKLOOP
4926   014030   104406                   TRAP    C$CLP1
4927
4928                                      ;READ AND CHECK MSAD BITS 17 AND 16 IN CONTROL REGISTER 2 TO SEE IF THEY
4929                                      ;ARE THE SAME AS SET ON THE TARGET EMULATOR MODULE.  ADDRESS BITS 17 AND
4930                                      ;16 ARE CLOCKED INTO THE MEMORY SIMULATOR ADDRESS LATCH BY THE SIGNAL
4931                                      ;"ADVAL H".  THE SIGNAL "ADVAL H" WAS GENERATED BY PULSING THE SIGNAL
4932                                      ;"PRAS H" ON THE TARGET EMULATOR MODULE.  THE MEMORY SIMULATOR'S ADDRESS
4933                                      ;LATCHES ARE ENABLED TO MSAD BITS 17:0 AS A RESULT OF "CTS H" AND "CTS L"
4934                                      ;BEING ASSERTED HIGH AND LOW RESPECTIVELY.
4935
4936   014032   052737   000014  002250  8$:    BIS     #MSEL1!MSEL0,S2MASK    ;SETUP TO IGNORE MSEL1 H AND MSEL0 H
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K 8

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 101
CVCDDB.P11   14-JUN-82 09:54   TEST 2: CHECK ADDRESS BUS TO MS AND SA FROM TE   SEQ 0101

```
4937  014040  016137  000020  002244        MOV    20(R1),S2LOAD           ;GET EXPECTED MSAD BITS 17 AND 16
4938  014046  016137  000020  002246        MOV    20(R1),S2GOOD           ;SAVE FOR COMPARISONS ON A READ COMMAND
4939  014054  004737  010562                JSR    PC,READS2               ;READ AND CHECK CONTROL REGISTER 2
4940  014060  001405                         BEQ    9$                      ;IF OK THEN CONTINUE
4941  014062                                ERRDF  2,TEMSA1,S02ERR         ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
4942  014062  104455                         TRAP   C$ERDF
4943  014064  000002                         .WORD  2
4944  014066  002410                         .WORD  TEMSA1
4945  014070  005366                         .WORD  S02ERR
4946  014072                                CKLOOP
4947  014072  104406                         TRAP   C$CLP1
4948
4949                                         ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
4950                                         ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
4951
4952  014074  004737  012144        9$:      JSR    PC,SLCTED               ;SELECT STATE ANALYZER MODULE
4953
4954                                         ;SET THE SIGNAL TRSL2 L TO THE LOW STATE BY SETTING CDAL REGISTER BIT
4955                                         ;3 TO A ONE AND CDAL REGISTER BIT 2 TO A ZERO.  THE SIGNAL TRSL2 L WILL
4956                                         ;ENABLE THE STATE ANALYZERS SYSTEM BUS LATCHES TO THE STATE ANALYZERS
4957                                         ;TRDI 59:0 BUS.
4958
4959  014100  112737  000010  002272        MOVB   #CDAL3,E0LOAD           ;SETUP BITS TO SET TRSL2 L TO LOW STATE
4960  014106  004737  010700                JSR    PC,LDRDE0               ;GO LOAD, READ AND CHECK CONTROL REG 0
4961  014112  001405                         BEQ    10$                     ;IF LOADED OK THEN CONTINUE
4962  014114                                ERRDF  5,CDALRG,E0EROR         ;CDAL REGISTER NOT EQUAL EXPECTED
4963  014114  104455                         TRAP   C$ERDF
4964  014116  000005                         .WORD  5
4965  014120  003010                         .WORD  CDALRG
4966  014122  006146                         .WORD  E0EROR
4967  014124                                CKLOOP
4968  014124  104406                         TRAP   C$CLP1
4969
4970                                         ;ASSERT THE SIGNAL PTER1 L IN THE POINTER REGISTER BY LOADING THE
4971                                         ;APPROPRIATE BITS IN THE PDAL REGISTER (CONTROL REGISTER 2)
4972
4973  014126  004537  012164        10$:     JSR    R5,LDPDAL               ;LOAD AND CHECK PDAL REG WITH NEXT WORD
4974  014132  000001                         .WORD  PTER1                   ;SETUP TO READ TRDI BUS BITS 15:0
4975
4976                                         ;AS A RESULT OF A PULSE ON THE TARGET EMULATOR'S SIGNAL ''XRAS H'' AT THE
4977                                         ;BEGINNING OF THIS TEST, THE TARGET EMULATOR'S ADDRESS BUS WAS CLOCKED
4978                                         ;INTO THE STATE ANALYZER'S ADDRESS LATCHES VIA THE CLOCKING SIGNALS
4979                                         ;''EDCK0 H'' AND ''EDCK1 H''.  THE PROGRAM HAS ALREADY ASSERTED THE SIGNAL
4980                                         ;''TRSL2 L'' WHICH WILL ENABLE THE SYSTEM BUS LATCHES ONTO THE STATE
4981                                         ;ANALYZER'S TRDI 59:0 BUS.  WHEN THE PROGRAM ISSUES A READ COMMAND TO
4982                                         ;CONTROL REGISTER 6 AND THE PDAL REGISTER IS SETUP TO SELECT PTER1 L,
4983                                         ;A PULSE WILL BE ISSUED ON THE SIGNAL RPT1 L.  THIS SIGNAL WILL READ
4984                                         ;TRDI BUS BITS 15:0 WHICH ARE THE ADDRESS LATCHES FOR SYSTEM BUS
4985                                         ;ADDRESSES 15:0.
4986
4987  014134  011137  002316                MOV    (R1),E6LOAD             ;GET DATA LOADED INTO TARGET EMULATOR
4988  014140  004737  011054                JSR    PC,READE6               ;READ ADDRESSES 15:0 ON TRDI 15:0
4989  014144  001405                         BEQ    11$                     ;IF OK THEN CONTINUE
4990  014146                                ERRDF  8,TEEDAD,E026ER         ;TE TO SA ADDRESS BUS ERROR - TRDI 15:0
4991  014146  104455                         TRAP   C$ERDF
4992  014150  000010                         .WORD  8
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L 8

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 102
CVCDDB.P11   14-JUN-82 09:54   TEST 2: CHECK ADDRESS BUS TO MS AND SA FROM TE   SEQ 0102

```
4993   014152  003173                          .WORD   TEEDAD
4994   014154  006212                          .WORD   E026ER
4995   014156                          CKLOOP
4996   014156  104406                          TRAP    C$CLP1
4997
4998                                   ;ASSERT THE SIGNAL "PTER3 L" IN THE POINTER REGISTER BY LOADING THE
4999                                   ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.
5000
5001   014160  004537  012164          11$:    JSR     R5,LDPDAL                   ;LOAD AND CHECK PDAL REG NEXT WORD
5002   014164  000003                          .WORD   PTER3                      ;SETUP TO READ TRDI BUS BITS 47:32
5003
5004                                   ;AS A RESULT OF PULSES ON THE TARGET EMULATOR'S SIGNALS "RASP L" AND
5005                                   ;"XPI L", PULSES SHOULD HAVE OCCURED ON THE SIGNALS "EDCK5 H" AND
5006                                   ;"EDCK4 H" RESPECTIVELY.  THE PULSE "EDCK5 H" WILL CLCOK THE CTL SYSTEM
5007                                   ;BUS BITS 7:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE
5008                                   ;BITS.  THESE BITS WILL BE READ ONTO THE STATE ANALYZERS TRDI BUS BITS
5009                                   ;47:40.  THIS TEST WILL NOT CHECK THESE BITS AT THIS TIME.  THE PULSE,
5010                                   ;"EDCK4 H", WILL CLOCK SYSTEM BUS ADDRESS BITS 17 AND 16, AND THE TARGET
5011                                   ;EMULATOR'S SIGNALS BTS 3:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES
5012                                   ;FOR THESE BITS.  THESE BITS WILL BE READ ONTO THE STATE ANALYZERS TRDI
5013                                   ;BUS BITS 39:32.  TRDI BUS BITS 47:40 WILL BE IGNORED DURING THIS TEST.
5014                                   ;THE SIGNAL BTS0 H WILL BE READ AS A ONE ON TRDI BIT 32 AS A RESULT OF
5015                                   ;THE TARGET EMULATOR'S SIGNALS BEING SET ACCORDINGLY:
5016                                   ;       XR/WHB L  - HIGH STATE
5017                                   ;       MR11 L    - HIGH STATE
5018                                   ;       XR/WLB H  - LOW STATE
5019                                   ;       INTER L   - HIGH STATE
5020
5021   014166  016137  000030  002316          MOV     30(R1),E6LOAD              ;GET EXPECTED TRDI 39:32 PATTERN
5022   014174  012737  177400  002320          MOV     #177400,E6MASK             ;SETUP TO IGNORE UNWANTED BITS
5023   014202  004737  011054                  JSR     PC,READE6                  ;READ BTS 3:0 + ADDR 17:16 ON TRDI 39:32
5024   014206  001404                          BEQ     12$                        ;IF OK THEN CONTINUE
5025   014210                                  ERRDF   8,TEEDA1,E026ER            ;TE TO SA XSEL1,EDSEL0,ADDR 17:16 + BTS 3:0 ERRO
5026   014210  104455                          TRAP    C$ERDF
5027   014212  000010                          .WORD   8
5028   014214  003242                          .WORD   TEEDA1
5029   014216  006212                          .WORD   E026ER
5030   014220                          12$:    ENDSEG
5031   014220                          10000$:
5032   014220  104405                          TRAP    C$ESEG
5033
5034   014222  000420                          BR      31$
5035
5036                                   ;DATA PATTERN FOR ADDRESS BITS 15:0 TO BE LOADED INTO DIAGNOSTIC ADDRESS
5037                                   ;REGISTER.
5038
5039   014224  177777                  30$:    .WORD   177777
5040   014226  052525                          .WORD   052525
5041   014230  125252                          .WORD   125252
5042   014232  000000                          .WORD   000000
5043
5044                                   ;HDAL REGISTER ADDRESS BITS ON TARGET EMULATOR MODULE TO SET ADDRESS
5045                                   ;BITS 17 AND 16
5046
5047   014234  040000                          .WORD   HDAL14                     ;ADDRESS 17
5048   014236  004000                          .WORD   HDAL11                     ;ADDRESS 16
```

```
5049  014240  044000                          .WORD    HDAL14!HDAL11              ;ADDRESS 17 AND 16
5050  014242  000000                          .WORD    0                         ;ADDRESS 17 AND 16 SET TO A 0
5051
5052                                  ;EXPECTED MEMORY SIMULATOR CONTROL REGISTER 2 MSAD BITS FOR 17 AND 16
5053
5054  014244  000002                          .WORD    MSAD17
5055  014246  000001                          .WORD    MSAD16
5056  014250  000003                          .WORD    MSAD17!MSAD16
5057  014252  000000                          .WORD    0
5058
5059                                  ;EXPECTED STATE ANALYZER BITS FOR XSEL1 H, EDSEL0 H, ADDRESSES 17:16
5060                                  ;AND BTS BITS 3:0
5061
5062  014254  000041                          .WORD    BIT5!BIT0                 ;ADDRESS 17 AND BTS0 H
5063  014256  000021                          .WORD    BIT4!BIT0                 ;ADDRESS 16 AND BTS0 H
5064  014260  000061                          .WORD    BIT5!BIT4!BIT0            ;ADDRESS 17 AND 16 AND BTS0 H
5065  014262  000001                          .WORD    BIT0                      ;BTS0 H
5066
5067  014264                 31$:     ENDTST
5068  014264                 L10036:
5069  014264  104401                          TRAP     C$ETST
5070
```

N 8

HARDWARE TESTS MACY11 30A(1052)   16-JUN-82 13:46 PAGE 104
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0104

```
5071                                    .SBTTL  TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE
5072
5073                                    ;++
5074                                            THIS TEST WILL CHECK THAT DATA, WRITTEN INTO LOCATIONS OF THE MEMORY
5075                                    ;       SIMULATOR RAM, CAN BE ENABLED TO THE TARGET EMULATOR MODULE AND CLOCKED
5076                                    ;       INTO THE STATE ANALYZER MODULE VIA THE SYSTEM DATA BUS WHEN A "READ"
5077                                    ;       OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE IN 16 BIT
5078                                    ;       MODE.  ADDRESSES 0, 20000, 40000 AND 60000, WHICH ARE THE FIRST LOCA-
5079                                    ;       TIONS OF EACH 4K BANK OF MEMORY SIMULATOR RAM, WILL BE WRITTEN WITH A
5080                                    ;       DATA PATTERN OF 125252, 052525, 177777, AND 000000 RESPECTIVELY.
5081                                    ;       LOCATIONS OF THE MEMORY SIMULATOR RAM WILL BE ADDRESSED VIA THE DIAGNOS-
5082                                    ;       TIC ADDRESS REGISTER ON THE TARGET EMULATOR MODULE DURING A NORMAL T-11
5083                                    ;       TIMING CYCLE.  A NORMAL T-11 TIMING CYCLE OCCURS WHEN RAS, CAS AND PI
5084                                    ;       ARE ASSERTED IN THE ORDER LISTED AND THEN DE-ASSERTED IN THE FOLLOWING
5085                                    ;       ORDER CAS, PI AND RAS.  THE PROGRAM WILL CHECK THAT THE SYSTEM ADDRESS
5086                                    ;       BUS WAS CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES AND
5087                                    ;       THE STATE ANALYZER'S SYSTEM BUS LATCHES WHEN THE SIGNALS XRAS H AND
5088                                    ;       PRAS H ARE ASSERTED HIGH ON THE TARGET EMULATOR MODULE.  WHEN THE
5089                                    ;       TARGET EMULATOR SIGNALS XR/WLB H, XR/WHB H, XRAS H, AND XCAS H ARE
5090                                    ;       ASSERTED HIGH, THE TARGET EMULATOR SIGNALS "READ H" AND "MSDI H" WILL
5091                                    ;       BE ASSERTED HIGH.  THE SIGNAL "READ H" BEING ASSERTED WILL ENABLE
5092                                    ;       MEMORY SIMULATOR RAM DATA ADDRESSED BY THE TARGET EMULATOR MODULE ONTO
5093                                    ;       THE SYSTEM DATA BUS.  THE SYSTEM DATA BUS WILL BE ENABLED TO THE TARGET
5094                                    ;       EMULATOR'S EODAL BUS VIA THE SIGNAL "MSDI H" AND THE EODAL BUS WILL BE
5095                                    ;       ENABLED TO THE TARGET EMULATOR'S EIDAL BUS VIA THE SIGNALS COHB L AND
5096                                    ;       COLB L.  THE SIGNALS COHB L AND COLB L ARE ASSERTED LOW AS A RESULT OF
5097                                    ;       THE SIGNALS ETR L, PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L BEING
5098                                    ;       ASSERTED HIGH.  THE PROGRAM WILL READ AND CHECK THE TARGET EMULATOR'S
5099                                    ;       EODAL AND EIDAL BUS TO CONTAIN THE EXPECTED MEMORY SIMULATOR RAM DATA.
5100                                    ;       WHEN THE SIGNAL XCAS L IS RETURNED TO ITS DE-ASSERTED STATE, THE SIGNALS
5101                                    ;       "EDCK2 H" AND "EDCK3 H" WILL GO FROM A LOW TO A HIGH STATE THUS CLOCKING
5102                                    ;       THE SYSTEM DATA BUS INTO THE STATE ANALYZERS SYSTEM DATA BUS LATCHES.
5103                                    ;       THE PROGRAM WILL CHECK THAT THE SYSTEM DATA BUS WAS CLOCKED INTO THE
5104                                    ;       STATE ANALYZER'S SYSTEM DATA BUS LATCHES BY ENABLING THE LATCHES TO THE
5105                                    ;       STATE ANALYZER'S TRDI BUS VIA THE SIGNAL TRSL2 L AND THEN READING TRDI
5106                                    ;       BUS BITS 31:16 TO CONTAIN THE EXPECTED MEMORY SIMULATOR RAM DATA.  THE
5107                                    ;       PROGRAM WILL ALSO CHECK THAT THE STATE ANALYZER'S TRACE RAM ADDRESS
5108                                    ;       REGISTER WAS INCREMENTED BY ONE VIA THE SIGNAL "CTR L" WHEN THE TARGET
5109                                    ;       EMULATOR SIGNAL "EDEOC H" WAS SET HIGH.
5110                                    ;--
5111
5112   014266                           BGNTST
5113   014266                   T3::
5114   014266  004737  007440           JSR     PC,INITMD                 ;INITIALIZE MDE/T-11 SYSTEM MODULES
5115
5116   014272                           BGNSEG
5117   014272  104404                   TRAP    C$BSEG
5118
5119   014274  005037  002320           CLR     E6MASK                    ;CLEAR REGISTER 6 MASK WORD FOR LOOPING
5120
5121                                    ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5122                                    ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5123
5124   014300  004737  012214           JSR     PC,SLCTTE                 ;SELECT TARGET EMULATOR MODULE
5125
5126                                    ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL "BRKRES L"
```

B 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 105
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0105

```
5127                                              ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
5128                                              ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
5129                                              ;THE SIGNAL "BRKRES L" VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
5130                                              ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
5131                                              ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED VIA THE
5132                                              ;THE SIGNAL "RASP L" LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
5133                                              ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
5134                                              ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
5135
5136   014304  012737  043020  002334      MOV    #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD  ;SETUP BITS TO BE LOADED
5137   014312  004737  012766              JSR    PC,BRKRES                      ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
5138
5139                                              ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
5140                                              ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
5141                                              ;REGISTER 6.
5142
5143   014316  004537  012234              JSR    R5,SELTER                      ;SELECT REGISTER SPECIFIED BY NEXT WORD
5144   014322  000003                      .WORD  HDAL                           ;SELECT THE HDAL REGISTER
5145
5146                                              ;SET HDAL REGISTER BITS 9,4,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
5147                                              ;ZERO.  HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
5148                                              ;AND CONTROL SIGNALS.  HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
5149                                              ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS.  HDAL REGISTER
5150                                              ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
5151                                              ;HDAL REGISTER BITS 4 AND 3 SET TO ONES WILL SET THE SIGNALS XR/WLB H
5152                                              ;AND XR/WHB H TO THE HIGH STATE.  THESE SIGNALS WILL CAUSE THE SIGNAL
5153                                              ;"REAT H" TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE SIGNALS XRAS H
5154                                              ;AND XCAS H ARE ASSERTED HIGH.
5155
5156   014324  012737  001034  002346      MOV    #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD  ;SET HDAL BITS 9,4,3 + 2 TO ONES
5157   014332  004737  011216              JSR    PC,LDRDT6                      ;GO LOAD, READ AND CHECK HDAL REGISTER
5158   014336  001405                      BEQ    1$                             ;IF LOADED OK THEN CONTINUE
5159   014340                              ERRDF  12,HDALRG,T06ERR               ;HDAL REGISTER NOT EQUAL EXPECTED
5160   014340  104455                      TRAP   C$ERDF
5161   014342  000014                      .WORD  12
5162   014344  003756                      .WORD  HDALRG
5163   014346  006732                      .WORD  T06ERR
5164   014350                              CKLOOP
5165   014350  104406                      TRAP   C$CLP1
5166
5167                                              ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
5168                                              ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
5169                                              ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY "BRKRES L".
5170
5171   014352  005037  002340      1$:     CLR    T4LOAD                         ;SETUP TO CLEAR ALL OTHER R/W BITS
5172   014356  004737  012706              JSR    PC,CLRPSM                      ;PULSE INVD L VIA VDAL2 H
5173
5174                                              ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON
5175                                              ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
5176                                              ;BE WRITTEN OR READ.
5177
5178   014362  004537  012234              JSR    R5,SELTER                      ;SELECT REGISTER SPECIFIED BY NEXT WORD
5179   014366  000004                      .WORD  MODE                           ;SELECT THE MODE REGISTER
5180
5181                                              ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
5182                                              ;ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
```

C 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 106
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0106

```
5183
5184  014370  005037  002346              CLR     T6LOAD              ;SETUP TO CLEAR ALL MODE REGISTER BITS
5185  014374  004737  011216              JSR     PC,LDRDT6           ;GO LOAD, READ AND CHECK MODE REGISTER
5186  014400  001405                      BEQ     2$                  ;IF LOADED OK THEN CONTINUE
5187  014402                              ERRDF   12,MODREG,T06ERR    ;MODE REGISTER NOT EQUAL EXPECTED
5188  014402  104455                      TRAP    C$ERDF
5189  014404  000014                      .WORD   12
5190  014406  004002                      .WORD   MODREG
5191  014410  006732                      .WORD   T06ERR
5192  014412                              CKLOOP
5193  014412  104406                      TRAP    C$CLP1
5194
5195                              ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
5196                              ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
5197                              ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDAL0 H
5198                              ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED. OTHERWISE, THE CTL REGIS-
5199                              ;TER WILL BE ADDRESSED.
5200
5201  014414  004537  012234      2$:     JSR     R5,SELTER           ;SELECT REGISTER SPECIFIED BY NEXT WORD
5202  014420  000002                      .WORD   FDAL                ;SELECT EOAI AND FDAL REGISTER
5203
5204                              ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER.  THE EOAI REGISTER WILL
5205                              ;BE LOADED AND CHECKED FOR ZEROES.  THE FDAL REGISTER WILL BE LOADED AND
5206                              ;CHECKED FOR A DATA PATTERN OF ONE (FDAL0 H = 1).
5207
5208  014422  012737  000001  002346      MOV     #FDAL0,T6LOAD       ;SETUP EOAI AND FDAL REG DATA PATTERN
5209  014430  004737  011216              JSR     PC,LDRDT6           ;GO LOAD, READ AND CHECK EOAI + FDAL REG
5210  014434  001405                      BEQ     3$                  ;IF LOADED OK THEN CONTINUE
5211  014436                              ERRDF   12,EOAIFD,T06ERR    ;EOAI OR FDAL REGISTER ERROR
5212  014436  104455                      TRAP    C$ERDF
5213  014440  000014                      .WORD   12
5214  014442  004047                      .WORD   EOAIFD
5215  014444  006732                      .WORD   T06ERR
5216  014446                              CKLOOP
5217  014446  104406                      TRAP    C$CLP1
5218
5219                              ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
5220                              ;CHANGES OCCURED DOING THE PAST SEQUENCES.
5221
5222  014450  004737  011200      3$:     JSR     PC,READT4           ;READ AND CHECK VDAL REGISTER
5223  014454  001404                      BEQ     4$                  ;IF NO CHANGES THEN CONTINUE
5224  014456                              ERRDF   11,VDALRG,T4EROR    ;VDAL OR PAUSE STATE MACHINE ERROR
5225  014456  104455                      TRAP    C$ERDF
5226  014460  000013                      .WORD   11
5227  014462  003710                      .WORD   VDALRG
5228  014464  006716                      .WORD   T4EROR
5229  014466              4$:             ENDSEG
5230  014466              10000$:
5231  014466  104405                      TRAP    C$ESEG
5232
5233  014470                              BGNSEG
5234  014470  104404                      TRAP    C$BSEG
5235
5236                              ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5237                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5238
```

D 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 107
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0107

```
5239   014472  004737  011250              JSR     PC,SLCTMS                  ;SELECT MEMORY SIMULATOR MODULE
5240
5241                                        ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM.  THE
5242                                        ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H' AND 'MPIN H' SET TO
5243                                        ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM.  MAP PROTECTION RAM
5244                                        ;BITS 'WRE H' AND 'RDE H' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
5245                                        ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
5246                                        ;WHEN 'RDE H' AND 'WRE H' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
5247                                        ;TO THOSE ADDRESSES.
5248
5249   014476  004737  011356              JSR     PC,MPRAM                   ;GO LOAD, READ AND CHECK MAP PROTECT RAM
5250
5251                                        ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0.  THE FOLLOWING DATA
5252                                        ;PATTERNS; 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
5253                                        ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0.  THESE PATTERNS
5254                                        ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
5255                                        ;ADDRESSED.
5256
5257   014502  004737  011642              JSR     PC,MSRAM0                  ;LOAD, READ AND CHECK MODULE SELECT RAM 0
5258
5259                                        ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1.  THE FOLLOWING DATA PATTERNS
5260                                        ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
5261                                        ;AT ADDRESS 0; 17, 0, 0 AND 0.  THESE PATTERNS WILL ENABLE THE FIRST 32K
5262                                        ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
5263
5264   014506  004737  012012              JSR     PC,MSRAM1                  ;LOAD, READ AND CHECK MODULE SELECT RAM 1
5265
5266   014512  012701  015646              MOV     #30$,R1                    ;SETUP POINTER TO ADDRESS TABLE
5267
5268   014516                        5$:    BGNSEG
5269   014516  104404                       TRAP    C$BSEG
5270
5271                                        ;LOAD MEMORY SIMULATOR RAM ADDRESS TO BE TESTED INTO CONTROL REGISTER 4.
5272                                        ;ADDRESSES TO BE LOADED ARE 0, 20000, 40000 AND 60000.
5273
5274   014520  011137  002254              MOV     (R1),S4LOAD                ;GET ADDRESS FROM ADDRESS TABLE
5275   014524  004737  010606              JSR     PC,LDRDS4                  ;LOAD READ AND CHECK CONTROL REG 4
5276   014530  001405                      BEQ     6$                         ;IF LOADED OK THEN CONTINUE
5277   014532                              ERRDF   3,MSADRG,S4EROR            ;MSAD 15:0 REGISTER ERROR
5278   014532  104455                      TRAP    C$ERDF
5279   014534  000003                      .WORD   3
5280   014536  002510                      .WORD   MSADRG
5281   014540  005336                      .WORD   S4EROR
5282   014542                              CKLOOP
5283   014542  104406                      TRAP    C$CLP1
5284
5285                                        ;CLEAR BITS MSEL1 H, MSEL0 H, MSAD17 H AND MSAD16 H IN CONTROL REGISTER
5286                                        ;2.  MSEL0 H AND MSEL1 H ON A ZERO WILL CAUSE THE SIGNAL 'SSM L' TO BE
5287                                        ;ASSERTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.  ON A WRITE
5288                                        ;OR READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE WRITTEN INTO OR
5289                                        ;READ FROM MEMORY SIMULATOR RAM ADDRESSES BY CONTROL REGISTER 2 AND 4.
5290                                        ;THE MEMORY SIMULATOR RAM'S ARE ENABLED BY THE DATA PATTERNS PREVIOUSLY
5291                                        ;WRITTEN INTO MODULE SELECT RAMS 0 AND 1.  MSAD17 H AND MSAD16 H WILL BE
5292                                        ;LOADED AND CHECKED WITH ZEROES.  THE PROGRAM WILL EXPECT CONTROL REGIS-
5293                                        ;TER 2 BITS 'ESR H' AND 'WREN H' TO BE READ AS ONES AS A RESULT OF MAP
5294                                        ;PROTECTION RAM BITS 'MPIN H' AND 'WRE H' BEING SET TO ONES.
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E 9

HARDWARE TESTS   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 108
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0108

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5295
5296  014544  005037  002244           6$:    CLR    S2LOAD              ;SET ALL BITS IN REG 2 TO ZEROES
5297  014550  013737  002244  002246           MOV    S2LOAD,S2GOOD       ;COPY DATA LOADED TO EXPECTED
5298  014556  052737  000140  002246           BIS    #ESRH!WRENH,S2GOOD  ;EXPECT ESR H AND WREN H TO BE ONES
5299  014564  012737  177400  002250           MOV    #177400,S2MASK      ;SETUP TO COMPARE LOW BYTE
5300  014572  004737  010554                   JSR    PC,LDRD2S           ;LOAD, READ AND CHECK CONTROL REG 2
5301  014576  001405                           BEQ    7$                  ;IF LOADED OK THEN CONTINUE
5302  014600                                   ERRDF  2,,S2EROR           ;CONTROL REGISTER 2 NOT = EXPECTED
5303  014600  104455                           TRAP   C$ERDF
5304  014602  000002                           .WORD  2
5305  014604  000000                           .WORD  0
5306  014606  005322                           .WORD  S2EROR
5307  014610                                   CKLOOP
5308  014610  104406                           TRAP   C$CLP1
5309
5310                                   ;LOAD DATA PATTERN INTO MEMORY SIMULATOR RAM ADDRESSED BY CONTROL
5311                                   ;REGISTER 2 AND 4.  THE ADDRESS AND DATA PATTERN LOADED ARE AS FOLLOWS:
5312                                   ;          ADDRESS          DATA
5313                                   ;          000000           125252
5314                                   ;          020000           052525
5315                                   ;          040000           177777
5316                                   ;          060000           000000
5317
5318  014612  005037  002264           7$:    CLR    S6MASK              ;SETUP TO COMPARE ALL BITS
5319  014616  016137  000010  002260           MOV    10(R1),S6LOAD       ;GET DATA PATTERN FROM THE TABLE
5320  014624  004737  010632                   JSR    PC,LDRDS6           ;GO LAOD, READ AND CHECK RAM LOCATION
5321  014630  001404                           BEQ    8$                  ;IF LOADED OK THEN CONTINUE
5322  014632                                   ERRDF  4,MSGMSR,S6ALLR     ;DATA ERROR IN MEMORY SIMULATOR RAM
5323  014632  104455                           TRAP   C$ERDF
5324  014634  000004                           .WORD  4
5325  014636  002745                           .WORD  MSGMSR
5326  014640  005456                           .WORD  S6ALLR
5327  014642                           8$:    ENDSEG
5328  014642                           10002$:
5329  014642  104405                           TRAP   C$ESEG
5330
5331  014644  005761  000010                   TST    10(R1)              ;CHECK IF LAST DATA PATTERN
5332  014650  001402                           BEQ    9$                  ;IF YES THEN START NEXT SETUP
5333  014652  005721                           TST    (R1)+               ;UPDATE POINTER TO ADDRESS TABLE
5334  014654  000720                           BR     5$                  ;GO LOAD NEXT ADDRESS AND DATA PATTERN
5335
5336                                   ;SET THE SIGNAL "CTS H" TO A ONE IN CONTROL REGISTER 0.  THIS WILL
5337                                   ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
5338                                   ;IN THIS TEST, "CTS H" ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
5339                                   ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
5340                                   ;SYSTEM BUS.
5341
5342  014656  052737  000002  002234   9$:    BIS    #CTSH,S0LOAD        ;SETUP BIT TO BE LOADED
5343  014664  004737  010506                   JSR    PC,LDRDS0           ;GO LOAD, READ AND CHECK CONTROL REG 2
5344  014670  001404                           BEQ    10$                 ;IF LOADED OK THEN CONTINUE
5345  014672                                   ERRDF  1,,S0EROR           ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
5346  014672  104455                           TRAP   C$ERDF
5347  014674  000001                           .WORD  1
5348  014676  000000                           .WORD  0
5349  014700  005306                           .WORD  S0EROR
5350  014702                           10$:   ENDSEG
```

F 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 109
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0109

```
5351   014702                            10001$:
5352   014702   104405                         TRAP    C$ESEG
5353
5354   014704   012701   015646                MOV     #30$,R1                  ;GET POINTER TO ADDRESS AND DATA TABLES
5355
5356   014710                            11$:    BGNSEG
5357   014710   104404                         TRAP    C$BSEG
5358
5359                                            ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5360                                            ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5361
5362   014712   004737   012214                JSR     PC,SLCTTE
5363
5364                                            ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
5365                                            ;2:0 TO A 0.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
5366                                            ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.  THE DIAGNOSTIC
5367                                            ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
5368                                            ;BIT 9 BEING SET TO A ONE PREVIOUSLY.  ON A READ COMMAND TO CONTROL
5369                                            ;REGISTER 6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
5370
5371   014716   004537   012234                JSR     R5,SELTER                ;SELECT REGISTER SPECIFIED BY NEXT WORD
5372   014722   000000                         .WORD   ADDRES                   ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
5373
5374                                            ;LOAD READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A TEST PATTERN
5375                                            ;TO SELECT ADDRESS 0 OF EACH BANK OF THE MEMORY SIMULATOR RAM.  THE
5376                                            ;ADDRESSES LOADED ARE AS FOLLOWS TO SELECT THE BANK OF MEMORY:
5377                                            ;    000000 - SELECTS 1ST 4K OF MEMORY SIMULATOR MEMORY
5378                                            ;    020000 - SELECTS 2ND 4K OF MEMORY SIMULATOR MEMORY
5379                                            ;    040000 - SELECTS 3RD 4K OF MEMORY SIMULATOR MEMORY
5380                                            ;    060000 - SELECTS 4TH 4K OF MEMORY SIMULATOR MEMORY
5381                                            ;EACK BANK OF MEMORY SIMULATOR MEMORY CONSISTS OF 2K WORDS OR 4K BYTES.
5382
5383   014724   011137   002346                MOV     (R1),T6LOAD              ;GET THE TEST PATTERN FROM THE TABLE
5384   014730   004737   011216                JSR     PC,LDRDT6                ;GO LOAD, READ AND CHECK DIAG ADDRESS REG
5385   014734   001405                         BEQ     12$                      ;IF LOADED OK THEN CONTINUE
5386   014736                                  ERRDF   12,ADDRRG,T06ERR         ;DIAGNOSTIC ADDRESS REGISTER ERROR
5387   014736   104455                         TRAP    C$ERDF
5388   014740   000014                         .WORD   12
5389   014742   004144                         .WORD   ADDRRG
5390   014744   006732                         .WORD   T06ERR
5391   014746                                  CKLOOP
5392   014746   104406                         TRAP    C$CLP1
5393
5394                                            ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3.  THE
5395                                            ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
5396                                            ;CONTROL REGISTER 6.
5397
5398   014750   004537   012234          12$:    JSR     R5,SELTER                ;SELECT REGISTER SPECIFIED BY NEXT WORD
5399   014754   000003                         .WORD   HDAL                     ;SELECT THE HDAL REGISTER
5400
5401                                            ;RELOAD HDAL REGISTER BITS FOR SCOPE LOOPING PURPOSES ONLY.  THIS IS
5402                                            ;DONE TO SET ALL THE TIMING SIGNALS BACK TO THE NON-ASSERTED STATE.
5403
5404   014756   012737   001034   002346       MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD  ;GET BITS PREVIOUSLY LOADED
5405   014764   004737   011216                JSR     PC,LDRDT6                ;LOAD, READ AND CHECK HDAL REGISTER
5406   014770   001405                         BEQ     13$                      ;IF LOADED OK THEN CONTINUE
```

```
5407  014772                          ERRDF   12,HDALRG,TO6ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
5408  014772  104455                  TRAP    C$ERDF
5409  014774  000014                  .WORD   12
5410  014776  003756                  .WORD   HDALRG
5411  015000  006732                  .WORD   TO6ERR
5412  015002                          CKLOOP
5413  015002  104406                  TRAP    C$CLP1
5414
5415                          ;START A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE
5416                          ;   1.   SET XRAS H AND PRAS H TO THE HIGH STATE
5417                          ;   2.   SET XCAS H AND PCAS H TO THE HIGH STATE
5418                          ;   3.   SET XPI L AND PPI L TO THE LOW STATE
5419                          ;SETTING THE SIGNAL PRAS H TO THE HIGH STATE WILL CAUSE THE SIGNAL
5420                          ;"ADVAL H" TO GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE SYSTEM
5421                          ;ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR ADDRESS BUS LATCHES.
5422                          ;SETTING THE SIGNAL XRAS H TO THE HIGH STATE WILL CAUSE THE SIGNALS
5423                          ;EDCK0 H AND EDCK1 H TO GO FROM THE LOW STATE TO THE HIGH STATE, THUS
5424                          ;CLOCKING SYSTEM ADDRESS BUS BITS 15:0 INTO THE STATE ANALYZERS ADDRESS
5425                          ;BUS LATCHES FOR THESE BITS.  SETTING THE SIGNAL XRAS H TO THE HIGH
5426                          ;STATE WILL CAUSE THE RASP ONE SHOT TO BE FIRED, THUS CAUSING A PULSE
5427                          ;TO BE ISSUED ON THE SIGNAL CKAI H.  A PULSE ON CKAI H WILL CAUSE A
5428                          ;PULSE ON THE SIGNAL EDCK5 H.  THE SIGNAL EDCK5 H WILL CLOCK THE CTL 7:0
5429                          ;SYSTEM BUS BITS INTO THE STATE ANALYZERS LATCHES FOR THESE BITS.
5430                          ;SETTING THE SIGNAL XPI L TO THE LOW STATE WILL CAUSE THE SIGNAL EDCK4 H
5431                          ;TO GO FROM THE LOW STATE TO THE HIGH STATE, THUS CLOCKING THE SYSTEM
5432                          ;BUS SIGNALS CTL 11:8 AND BTS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS
5433                          ;LATCHES FOR THESE BITS.  WHEN THE SIGNALS XRAS H AND XCAS H ARE ASSERTED
5434                          ;HIGH, THE SIGNAL REAT H WILL GO FROM A LOW TO A HIGH STATE, THUS CAUSING
5435                          ;THE SIGNAL READ H TO GO FROM A LOW TO A HIGH STATE.  THE TARGET EMULATORS
5436                          ;SIGNAL READ H ALONG WITH THE MEMORY SIMULATOR'S SIGNALS CTS H AND ESR H
5437                          ;WILL CAUSE THE MEMORY SIMULATOR RAM DATA TO BE PUT ONTO THE SYSTEM DATA
5438                          ;BUS.  WHEN THE TARGET EMULATORS REAT H IS ASSERTED HIGH, THE
5439                          ;TARGET EMULATORS SIGNAL MSDI H WILL BE ASSERTED HIGH, THUS ENABLING
5440                          ;THE SYSTEM DATA BUS TO THE TARGET EMULATORS EODAL BUS.  THE MEMORY
5441                          ;SIMULATOR RAM'S ARE ADDRESSED BY THE MEMORY SIMULATOR SYSTEM BUS ADDRESS
5442                          ;LATCHES WHICH WERE CLOCKED BY THE SIGNAL ADVAL H.  THE DATA ON SYSTEM
5443                          ;ADDRESS BUS COMES FROM THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER.
5444
5445  015004  004737  012300    13$:  JSR     PC,XRASH                ;SET XRAS H AND PRAS H TO HIGH STATE
5446  015010  004737  012404          JSR     PC,XCASH                ;SET XCAS H AND PCAS H TO HIGH STATE
5447  015014  004737  012510          JSR     PC,XPIH                 ;SET XPI H AND PPI H TO THE LOW STATE
5448
5449                          ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H ARE
5450                          ;ASSERTED HIGH (1'S).
5451
5452  015020  012737  000110  002342  MOV   #VDAL6!VDAL3,T4GOOD       ;EXPECT READ H AND MSDI H TO BE ONES
5453  015026  004737  011200          JSR     PC,READT4               ;READ VDAL AND PAUSE STATE MACHINE REG
5454  015032  001405                  BEQ     14$                     ;IF DATA OK THEN CONTINUE
5455  015034                          ERRDF   11,VDALRG,T4EROR        ;VDAL OR PAUSE STATE MACHINE ERROR
5456  015034  104455                  TRAP    C$ERDF
5457  015036  000013                  .WORD   11
5458  015040  003710                  .WORD   VDALRG
5459  015042  006716                  .WORD   T4EROR
5460  015044                          CKLOOP
5461  015044  104406                  TRAP    C$CLP1
5462
```

H 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 111
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0111

```
5463                                                   ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5464                                                   ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5465
5466   015046  004737  011250          14$:    JSR     PC,SLCTMS                  ;SELECT THE MEMORY SIMULATOR MODULE
5467
5468                                                   ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
5469                                                   ;TARGET EMULATOR MODULE SET THE SIGNALS ADVAL H AND READ H TO THE
5470                                                   ;HIGH STATE FROM THE LOW STATE.
5471
5472   015052  004737  010522                  JSR     PC,READS0                 ;READ AND CHECK CONTROL REGISTER 0
5473   015056  001405                          BEQ     15$                       ;IF NO CHANGES THEN CONTINUE
5474   015060                                  ERRDF   1,,SOEROR                 ;CONTROL REGISTER 0 NOT = EXPECTED
5475   015060  104455                          TRAP    C$ERDF
5476   015062  000001                          .WORD   1
5477   015064  000000                          .WORD   0
5478   015066  005306                          .WORD   SOEROR
5479   015070                                  CKLOOP
5480   015070  104406                          TRAP    C$CLP1
5481
5482                                                   ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
5483                                                   ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
5484                                                   ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.  THE SIGNAL ADVAL H
5485                                                   ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
5486                                                   ;SIGNAL PRAS H WAS SET HIGH FROM THE LOW STATE.  THE MEMORY SIMULATORS
5487                                                   ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
5488                                                   ;BITS VIA THE SIGNALS CTS H AND CTS L.
5489
5490   015072  011137  002254          15$:    MOV     (R1),S4LOAD               ;GET TE DIAG ADDRESS REG DATA LOADED
5491   015076  004737  010614                  JSR     PC,READS4                 ;READ AND CHECK CONTROL REGISTER 4
5492   015102  001405                          BEQ     16$                       ;IF DATA = TE DIAG ADDRESS REG - CONT
5493   015104                                  ERRDF   3,TEMSAD,SO4ERR           ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
5494   015104  104455                          TRAP    C$ERDF
5495   015106  000003                          .WORD   3
5496   015110  002534                          .WORD   TEMSAD
5497   015112  005406                          .WORD   SO4ERR
5498   015114                                  CKLOOP
5499   015114  104406                          TRAP    C$CLP1
5500
5501                                                   ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
5502                                                   ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
5503                                                   ;ZEROES FOR THESE TWO ADDRESSES.  ADDRESS BITS 17 AND 16 WERE CLOCKED
5504                                                   ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
5505                                                   ;ADVAL H.  THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
5506                                                   ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE FROM
5507                                                   ;THE LOW STATE.  THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
5508                                                   ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
5509                                                   ;MEMORY SIMULATOR MODULE.
5510
5511   015116  052737  000014  002250  16$:    BIS     #MSEL0!MSEL1,S2MASK       ;IGNORE TRI-STATED BITS WHEN CTS H SET
5512   015124  005037  002244                  CLR     S2LOAD                    ;EXPECT MSAD 17:16 TO BE ZERO
5513   015130  013737  002244  002246          MOV     S2LOAD,S2GOOD             ;COPY DATA LOADED TO EXPECTED
5514   015136  052737  000140  002246          BIS     #ESRH!WRENH,S2GOOD        ;EXPECT MAP PROTECT BITS TO BE ONES
5515   015144  004737  010562                  JSR     PC,READS2                 ;READ AND CHECK CONTROL REGISTER 2
5516   015150  001405                          BEQ     17$                       ;IF DATA OK THEN CONTINUE
5517   015152                                  ERRDF   2,TEMSA1,SO2ERR           ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
5518   015152  104455                          TRAP    C$ERDF
```

I 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 112
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0112

```
5519   015154   0G0002                          .WORD    2
5520   015156   002410                          .WORD    TEMSA1
5521   015160   005366                          .WORD    SO2ERR
5522   015162                                   CKLOOP
5523   015162   104406                          TRAP     C$CLP1
5524
5525                                           ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
5526                                           ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5527
5528   015164   004737   012144        17$:     JSR      PC,SLCTED              ;SELECT STATE ANALYZER MODULE
5529
5530                                           ;SET THE SIGNAL TRSL2 L TO THE LOW STATE BY SETTING CDAL REGISTER BIT
5531                                           ;3 TO A ONE AND CDAL REGISTER BIT 2 TO A ZERO.  THE SIGNAL TRSL2 L WILL
5532                                           ;ENABLE THE STATE ANALYZER'S SYSTEM BUS LATCHES TO THE EVENT DETECTORS
5533                                           ;TRDI 59:0 BUS.
5534
5535   015170   112737   000010   002272        MOVB     #CDAL3,EOLOAD         ;SETUP BITS TO SET TRSL2 L TO LOW STATE
5536   015176   004737   010700                 JSR      PC,LDRDEO             ;GO LOAD, READ AND CHECK CONTROL REG 0
5537   015202   001405                          BEQ      18$                   ;IF LOADED OK THEN CONTINUE
5538   015204                                   ERRDF    5,CDALRG,EOEROR       ;CDAL REGISTER NOT EQUAL EXPECTED
5539   015204   104455                          TRAP     C$ERDF
5540   015206   000005                          .WORD    5
5541   015210   003010                          .WORD    CDALRG
5542   015212   006146                          .WORD    EOEROR
5543   015214                                   CKLOOP
5544   015214   104406                          TRAP     C$CLP1
5545
5546                                           ;ASSERT THE SIGNAL PTER1 L IN THE POINTER REGISTER BY LOADING THE
5547                                           ;APPROPRIATE BITS IN THE PDAL REGISTER (CONTROL REGISTER 2)
5548
5549   015216   004537   012164        18$:     JSR      R5,LDPDAL             ;LOAD AND CHECK PDAL REG WITH NEXT WORD
5550   015222   000001                          .WORD    PTER1                 ;SETUP TO READ TRDI BUS BITS 15:0
5551
5552                                           ;AS A RESULT OF SETTING THE SIGNAL ''XRAS H'' TO THE HIGH STATE ON THE
5553                                           ;TARGET EMULATOR MODULE,  THE TARGET EMULATOR'S ADDRESS BUS WAS CLOCKED
5554                                           ;INTO THE STATE ANALYZER'S ADDRESS LATCHES VIA THE CLOCKING SIGNALS
5555                                           ;''EDCKO H'' AND 'EDCK1 H''.  THE PROGRAM HAS ALREADY ASSERTED THE SIGNAL
5556                                           ;''TRSL2 L'' WHICH WILL ENABLE THE SYSTEM BUS LATCHES ONTO THE STATE
5557                                           ;ANALYZER'S TRDI 59:0 BUS.  WHEN THE PROGRAM ISSUES A READ COMMAND TO
5558                                           ;CONTROL REGISTER 6 AND THE PDAL REGISTER IS SETUP TO SELECT PTER1 L,
5559                                           ;A PULSE WILL BE ISSUED ON THE SIGNAL RPT1 L.  THIS SIGNAL WILL READ
5560                                           ;TRDI BUS BITS 15:0 WHICH ARE THE ADDRESS LATCHES FOR SYSTEM BUS
5561                                           ;ADDRESSES 15:0.
5562
5563   015224   011137   002316                 MOV      (R1),E6LOAD           ;GET DATA LOADED INTO TARGET EMULATOR
5564   015230   005037   002320                 CLR      E6MASK                ;SETUP TO READ ALL 16 BITS
5565   015234   004737   011054                 JSR      PC,READE6             ;READ ADDRESSES 15:0 ON TRDI 15:0
5566   015240   001405                          BEQ      19$                   ;IF OK THEN CONTINUE
5567   015242                                   ERRDF    8,TEEDAD,E026ER       ;TE TO SA ADDRESS BUS ERROR - TRDI 15:0
5568   015242   104455                          TRAP     C$ERDF
5569   015244   000010                          .WORD    8
5570   015246   003173                          .WORD    TEEDAD
5571   015250   006212                          .WORD    E026ER
5572   015252                                   CKLOOP
5573   015252   104406                          TRAP     C$CLP1
5574
```

J 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 113
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0113

```
5575                                                    ;ASSERT THE SIGNAL "PTER3 L" IN THE POINTER REGISTER BY LOADING THE
5576                                                    ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.
5577
5578   015254  004537  012164          19$:    JSR     R5,LDPDAL                  ;LOAD AND CHECK PDAL REG WITH NEXT WORD
5579   015260  000003                          .WORD   PTER3                      ;SETUP TO READ TRDI BUS BITS 47:32
5580
5581                                                    ;AS A RESULT OF PULSES ON THE TARGET EMULATOR'S SIGNALS "RASP L" AND
5582                                                    ;"XPI L". PULSES SHOULD HAVE OCCURED ON THE SIGNALS "EDCK5 H" AND
5583                                                    ;"EDCK4 H" RESPECTIVELY.  THE PULSE "EDCK5 H" WILL CLCOK THE CTL SYSTEM
5584                                                    ;BUS BITS 7:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE
5585                                                    ;BITS.  THESE BITS WILL BE READ ONTO THE STATE ANALYZERS TRDI BUS BITS
5586                                                    ;47:40.  THIS TEST WILL NOT CHECK THESE BITS AT THIS TIME.  THE PULSE,
5587                                                    ;"EDCK4 H", WILL CLOCK SYSTEM BUS ADDRESS BITS 17 AND 16, AND THE TARGET
5588                                                    ;EMULATOR'S SIGNALS BTS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES
5589                                                    ;FOR THESE BITS.  THESE BITS WILL BE READ ONTO THE STATE ANALYZERS TRDI
5590                                                    ;BUS BITS 39:32.  TRDI BITS 47:40 WILL BE IGNORED DURING THIS TEST.
5591
5592   015262  005037  002316                  CLR     E6LOAD                     ;EXPECT TRDI BITS 39:32 TO BE ZERO
5593   015266  012737  177400  002320          MOV     #177400,E6MASK             ;SETUP TO IGNORE UNWANTED BITS
5594   015274  004737  011054                  JSR     PC,READE6                  ;READ BTS 3:0 + ADDR 17:16 ON TRDI 39:32
5595   015300  001405                          BEQ     20$                        ;IF OK THEN CONTINUE
5596   015302                                  ERRDF   8,TEEDA1,E026ER            ;TE TO SA XSEL1,EDSEL0,ADDR 17:16 + BTS 3:0 ERRO
5597   015302  104455                          TRAP    C$ERDF
5598   015304  000010                          .WORD   8
5599   015306  003242                          .WORD   TEEDA1
5600   015310  006212                          .WORD   E026ER
5601   015312                                  CKLOOP
5602   015312  104406                          TRAP    C$CLP1
5603
5604                                                    ;ASSERT THE SIGNAL "PTER0 L" IN THE POINTER REGISTER BY LOADING THE
5605                                                    ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.  ON A WRITE
5606                                                    ;OR READ COMMAND TO CONTROL REGISTER 6 WHEN PTER0 L IS ASSERTED, THE
5607                                                    ;TRACE RAM ADDRESS REGISTER WILL BE WRITTEN AND READ.  PDAL REGISTER
5608                                                    ;BIT 6 WILL ALSO BE SET TO A ONE TO CAUSE THE TRACING FLIP-FLOP TO
5609                                                    ;BE SET TO THE ONE STATE.  THIS IS DONE SO THAT A PULSE WILL BE ISSUED
5610                                                    ;ON THE SIGNAL "CTR L" LATER ON IN THIS TEST WHEN THE TARGET EMULATOR'S
5611                                                    ;SIGNAL "EDEOC H" IS SET TO A ONE.
5612
5613   015314  004537  012164          20$:    JSR     R5,LDPDAL                  ;LOAD AND CHECK PDAL REG WITH NEXT WORD
5614   015320  000100                          .WORD   PDAL6!PTER0                ;SETUP TO WRITE/READ TRAM ADDRESS REG
5615
5616                                                    ;LOAD, READ AND CHECK THE TRACE RAM ADDRES REGISTER WITH A DATA PATTERN
5617                                                    ;OF ALL ONES (3777).  WHEN THE SIGNAL "EDEOC H" IS SET TO A ONE LATER IN
5618                                                    ;THIS TEST, THE TRACE RAM ADDRESS REGISTER SHOULD BE INCREMENTED TO
5619                                                    ;ZERO BY THE CLOCKING SIGNAL EDEOC H.
5620
5621   015322  012737  174000  002320          MOV     #174000,E6MASK             ;SETUP TO IGNORE UNUSED BITS
5622   015330  012737  003777  002316          MOV     #3777,E6LOAD               ;SETUP TO LOAD ALL ONES
5623   015336  004737  011046                  JSR     PC,LDRDE6                  ;LOAD READ AND CHECK TRAM ADDRESS REG
5624   015342  001404                          BEQ     21$                        ;IF LOADED OK THEN CONTINUE
5625   015344                                  ERRDF   8,TRADRS,E026ER            ;TRACE RAM ADDRESS REG NOT = 3777
5626   015344  104455                          TRAP    C$ERDF
5627   015346  000010                          .WORD   8
5628   015350  003477                          .WORD   TRADRS
5629   015352  006212                          .WORD   E026ER
5630
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K 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 114
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0114

```
5631                                              ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5632                                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5633
5634    015354  004737  012214          21$:     JSR     PC,SLCTTE                ;SELECT THE TARGET EMULATOR MODULE
5635
5636                                              ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO A 7.  THE EODAL BUS
5637                                              ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
5638
5639    015360  004537  012234                   JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
5640    015364  000007                           .WORD   EODAL                   ;SELECT THE EODAL BUS TO BE READ
5641
5642                                              ;AT THIS TIME THE MEMORY SIMULATOR RAM DATA SHOULD BE ENABLED ON THE
5643                                              ;SYSTEM DATA BUS AND ENABLED TO THE TARGET EMULATORS EODAL BUS VIA THE
5644                                              ;TARGET EMULATOR SIGNALS READ H AND MSDI H RESPECTIVELY.  THE MEMORY
5645                                              ;SIMULATOR RAM IS ADDRESSED BY THE TARGET EMULATORS DIAGNOSTIC ADDRESS
5646                                              ;REGISTER WHICH WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS
5647                                              ;BUS LATCHES VIA THE SIGNAL ADVAL H. THE ADDRESSES AND DATA PATTERNS
5648                                              ;STORED IN THE RAM ADDRESSES SELECTED ARE AS FOLLOWS
5649                                              ;       RAM ADDRESS 000000 WAS LOADED WITH 125252
5650                                              ;       RAM ADDRESS 020000 WAS LOADED WITH 052525
5651                                              ;       RAM ADDRESS 040000 WAS LOADED WITH 177777
5652                                              ;       RAM ADDRESS 060000 WAS LOADED WITH 000000
5653
5654    015366  016137  000010  002346           MOV     10(R1),T6LOAD           ;GET DATA LOADED INTO MS RAM ADDRESSED
5655    015374  004737  011224                   JSR     PC,READT6               ;READ SYSTEM DATA BUS ON THE EODAL BUS
5656    015400  001405                           BEQ     22$                     ;IF DATA = MS RAM DATA THEN CONTINUE
5657    015402                                    ERRDF   12,MSTEDE,T6ALLR        ;MS RAM DATA TO TE EODAL BUS ERROR
5658    015402  104455                            TRAP    C$ERDF
5659    015404  000014                            .WORD   12
5660    015406  004243                            .WORD   MSTEDE
5661    015410  006746                            .WORD   T6ALLR
5662    015412                                    CKLOOP
5663    015412  104406                            TRAP    C$CLP1
5664
5665                                              ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  THE EIDAL BUS
5666                                              ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
5667
5668    015414  004537  012234          22$:     JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
5669    015420  000006                           .WORD   EIDAL                   ;SELECT THE EIDAL BUS TO BE READ
5670
5671                                              ;IN THE PREVIOUS DATA CHECK, THE PROGRAM VERIFIED THAT THE MEMORY SIMU-
5672                                              ;LATOR RAM DATA WAS ENBALED TO THE EODAL BUS VIA THE SYSTEM DATA BUS.
5673                                              ;IN THIS SECTION, THE PROGRAM WILL CHECK THAT THE EODAL BUS IS ENABLED
5674                                              ;TO THE EIDAL BUS VIA THE CDAL BUS AS A RESULT OF THE SIGNALS COHB L AND
5675                                              ;COLB L BEING ASSERTED LOW.  THE SIGNALS COHB L AND COLB L ARE ASSERTED
5676                                              ;LOW AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED HIGH: ETR L,
5677                                              ;PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L.  THE DATA READ SHOULD BE
5678                                              ;THE SAME AS THAT WHICH WAS ENABLED TO THE EODAL BUS.  THE ADDRESSES
5679                                              ;AND DATA PATTERNS STORED IN THE RAM ADDRESSES SELECTED ARE AS FOLLOWS:
5680                                              ;       RAM ADDRESS 000000 WAS LOADED WITH 125252
5681                                              ;       RAM ADDRESS 020000 WAS LOADED WITH 052525
5682                                              ;       RAM ADDRESS 040000 WAS LOADED WITH 177777
5683                                              ;       RAM ADDRESS 060000 WAS LOADED WITH 000000
5684
5685    015422  016137  000010  002346           MOV     10(R1),T6LOAD           ;GET DATA LOADED INTO MS RAM ADDRESSED
5686    015430  004737  011224                   JSR     PC,READT6               ;READ SYSTEM DATA BUS ON EIDAL VIA EODAL
```

L 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 115
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0115

```
5687  015434  001405                          BEQ     23$                     ;IF DATA OK THEN CONTINUE
5688  015436                                  ERRDF   12,MSTEEI,T6ALLR        ;MS RAM DATA TO EIDAL BUS VIA EODAL BUS
5689  015436  104455                          TRAP    C$ERDF
5690  015440  000014                          .WORD   12
5691  015442  004331                          .WORD   MSTEEI
5692  015444  006746                          .WORD   T6ALLR
5693  015446                                  CKLOOP
5694  015446  104406                          TRAP    C$CLP1
5695
5696                                   ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
5697                                   ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
5698                                   ;REGISTER 6.
5699
5700  015450  004537  012234        23$:      JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
5701  015454  000003                          .WORD   HDAL                    ;SELECT THE HDAL REGISTER
5702
5703                                   ;FINISH THE T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
5704                                   ;  1. SET XCAS H AND PCAS H TO THE LOW STATE
5705                                   ;  2. SET XPI L AND PPI L TO THE HIGH STATE
5706                                   ;  3. SET XRAS H AND PRAS H TO THE LOW STATE
5707                                   ;SETTING THE SIGNAL XCAS H TO THE LOW STATE AND XCAS L TO THE HIGH STATE
5708                                   ;WILL CAUSE THE SIGNALS EDCK2 H AND EDCK3 H TO BE SET HIGH FROM THE LOW
5709                                   ;STATE, THUS CAUSING THE SYSTEM DATA BUS TO BE CLOCKED INTO THE STATE
5710                                   ;ANALYZERS SYSTEM DATA BUS LATCHES.
5711
5712  015456  012737  001034  002346  MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SETUP PREVIOULSY LOADED BITS
5713  015464  004737  012436          JSR     PC,XCASL                ;SET XCAS H AND PCAS H TO LOW STATE
5714  015470  004737  012542          JSR     PC,XPIL                 ;SET XPI L AND PPI L TO THE HIGH STATE
5715  015474  004737  012332          JSR     PC,XRASL                ;SET XRAS H AND PRAS H TO LOW STATE
5716
5717                                   ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H
5718                                   ;WENT TO A ZERO AS A RESULT OF SETTING THE SIGNALS XCAS H AND XRAS H
5719                                   ;TO THE LOW STATE.  CHECK THAT THE SIGNAL EDEOC H WHEN TO A ONE AS
5720                                   ;A RESULT OF XRAS H AND XCAS H BEING SET LOW AND THE SINGLE STEP SYNC
5721                                   ;FLIP-FLOP BEING SET TO A ONE VIA XCAS H.
5722
5723  015500  012737  000020  002342  MOV     #VDAL4,T4GOOD           ;EXPECT EDEOC H TO BE SET TO A ONE
5724  015506  004737  011200          JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
5725  015512  001405                          BEQ     24$                     ;IF OK THEN CONTINUE
5726  015514                                  ERRDF   11,VDALRG,T4EROR        ;VDAL OR PAUSE STATE MACHINE ERROR
5727  015514  104455                          TRAP    C$ERDF
5728  015516  000013                          .WORD   11
5729  015520  003710                          .WORD   VDALRG
5730  015522  006716                          .WORD   T4EROR
5731  015524                                  CKLOOP
5732  015524  104406                          TRAP    C$CLP1
5733
5734                                   ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
5735                                   ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5736
5737  015526  004737  012144        24$:      JSR     PC,SLCTED               ;SELECT STATE ANALYZER MODULE
5738
5739                                   ;ASSERT THE SIGNAL "PTER2 L" IN THE POINTER REGISTER BY LOADING THE
5740                                   ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER
5741
5742  015532  004537  012164          JSR     R5,LDPDAL               ;LOAD AND CHECK PDAL REG WITH NEXT WORD
```

M 9

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 116
CVCDDB.P11   14-JUN-82 09:54   TEST 3: CHECK DATA BUS TO SA AND TE FROM MS - 16 BIT MODE   SEQ 0116

```
5743   015536  000002                          .WORD    PTER2                   ;SETUP TO READ TRDI BUS BITS 31:16
5744
5745                                            ;TARGET EMULATOR SIGNALS EDCK2 H AND EDCK3 H WERE SET HIGH AS A RESULT
5746                                            ;OF THE TARGET EMULATOR SIGNAL XCAS L BEING SET HIGH.   THE SIGNALS
5747                                            ;EDCK2 H AND EDCK3 H WILL CLOCK THE SYSTEM DATA BUS INTO THE STATE
5748                                            ;ANALYZERS SYSTEM DATA BUS LATCHES FOR THESE BITS.   THESE BITS WILL
5749                                            ;BE READ ON THE STATE ANALYZERS TRDI BUS BITS 31:16.   THE DATA WAS PUT
5750                                            ;ONTO THE SYSTEM DATA BUS DURING A READ OPERATION TO THE MEMORY
5751                                            ;SIMULATOR MODULE.   ON A READ COMMAND TO STATE ANALYZERS CONTROL
5752                                            ;REGISTER 6, THE SIGNAL RPT2 H WILL BE GENERATED THUS READING TRDI
5753                                            ;SYSTEM BUS LATCHES FOR BITS 31:16.   THE ADDRESSES AND DATA PATTERNS
5754                                            ;STORED IN THE RAM ADDRESSES SELECTED ARE AS FOLLOWS:
5755                                            ;        RAM ADDRESS 000000 WAS LOADED WITH 125252
5756                                            ;        RAM ADDRESS 020000 WAS LOADED WITH 052525
5757                                            ;        RAM ADDRESS 040000 WAS LOADED WITH 177777
5758                                            ;        RAM ADDRESS 060000 WAS LOADED WITH 000000
5759
5760   015540  016137  000010  002316          MOV      10(R1),E6LOAD           ;GET MS DATA LOADED INTO RAM
5761   015546  005037  002320                  CLR      E6MASK                  ;SETUP TO READ ALL 16 BITS
5762   015552  004737  011054                  JSR      PC,READE6               ;READ SYSTEM DATA BUS LATCHES - TRDI 31:16
5763   015556  001405                          BEQ      25$                     ;IF OK THEN CONTINUE
5764   015560                                  ERRDF    8,MSEDDE,E026ER         ;MS RAM DATA TO SA TRDI 31:16 BUS ERROR
5765   015560  104455                          TRAP     C$ERDF
5766   015562  000010                          .WORD    8
5767   015564  003423                          .WORD    MSEDDE
5768   015566  006212                          .WORD    E026ER
5769   015570                                  CKLOOP
5770   015570  104406                          TRAP     C$CLP1
5771
5772                                            ;ASSERT THE SIGNAL 'PTERO L' IN THE POINTER REGISTER BY LOADING THE
5773                                            ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.   ON A READ
5774                                            ;COMMAND TO CONTROL REGISTER 6 WITH PTERO L ASSERTED LOW, THE TRACE
5775                                            ;RAM ADDRESS REGISTER WILL BE READ VIA THE SIGNAL 'RPIO H'.
5776
5777   015572  004537  012164          25$:    JSR      R5,LDPDAL               ;LOAD AND CHECK PDAL REG WITH NEXT WORD
5778   015576  000000                          .WORD    PTERO                   ;SELECT TRAM ADDRESS REG TO BE READ
5779
5780                                            ;CHECK THAT THE TRACE RAM ADDRESS REGISTER WAS INCREMENTED TO ZERO BY
5781                                            ;A PULSE BEING ISSUED ON THE SIGNAL 'CTR L'.   THE TRACE RAM ADDRESS
5782                                            ;REGISTER WAS LOADED WITH ALL ONES (3777) EARLIER IN THIS TEST SECTION.
5783                                            ;WHEN THE TARGET EMULATOR'S SIGNAL XCAS L WAS SET TO THE HIGH STATE BY
5784                                            ;SETTING XCAS H TO THE LOW STATE, THE SIGNAL 'EDEOC H' SHOULD GO FROM
5785                                            ;A LOW TO A HIGH STATE.   WHEN THE SIGNAL 'EDEOC H' GOES FROM A LOW TO
5786                                            ;A HIGH STATE, THE STATE ANALYZER SIGNAL 'TRANST H' SHOULD ALSO GO FROM
5787                                            ;A LOW TO A HIGH STATE.   WHEN THE SIGNAL 'TRANST H' GOES TO THE HIGH
5788                                            ;STATE, THE TRACE WRITE WIDTH ONE SHOT WILL BE FIRED.   AS A RESULT OF
5789                                            ;THE TRACING FLIP-FLOP BEING SET TO A ONE VIA PDAL6 H  AND THE TRACE
5790                                            ;WRITE WIDTH ONE SHOT BEING FIRED, A PULSE SHOULD OCCUR ON THE SIGNAL
5791                                            ;'CTR L'.   A PULSE ON 'CTR L' WILL INCREMENT THE TRACE RAM ADDRESS
5792                                            ;REGISTER BY ONE THUS CLCOKING THE TRACE RAM ADDRESS REGISTER FROM
5793                                            ;ALL ONES TO ALL ZEROES.
5794
5795   015600  005037  002316                  CLR      E6LOAD                  ;EXPECT TRAM ADDRESS REGISTER TO BE 0
5796   015604  012737  174000  002320          MOV      #174000,E6MASK          ;SETUP TO IGNORE UNUSED BITS
5797   015612  004737  011054                  JSR      PC,READE6               ;READ AND CHECK TRAM ADDRESS REGISTER
5798   015616  001404                          BEQ      26$                     ;IF 0 THEN CONTINUE
```

```
5799  015620                              ERRDF   8,TRADRS,E026ER          ;CTR L DIDN''T +1 TRAM ADDRESS REGISTER
5800  015620  104455                      TRAP    C$ERDF
5801  015622  000010                      .WORD   8
5802  015624  003477                      .WORD   TRADRS
5803  015626  006212                      .WORD   E026ER
5804  015630                      26$:    ENDSEG
5805  015630                      10003$:
5806  015630  104405                      TRAP    C$ESEG
5807
5808  015632  005761  000010              TST     10(R1)                   ;CHECK IF THIS WAS LAST DATA PATTERN
5809  015636  001413                      BEQ     31$                      ;IF YES THEN END OF TEST
5810  015640  005721                      TST     (R1)+                    ;UPDATE POINTER TO ADDRESS TABLE
5811  015642  000137  014710              JMP     11$                      ;GO CHECK NEXT DATA PATTERN
5812
5813                                      ;DATA PATTERN FOR ADDRESS BITS 15:0 TO BE LOADED INTO DIAGNOSTIC ADDRESS
5814                                      ;REGISTER.
5815
5816  015646  000000              30$:    .WORD   000000
5817  015650  020000                      .WORD   020000
5818  015652  040000                      .WORD   040000
5819  015654  060000                      .WORD   060000
5820
5821                                      ;DATA PATTERN FOR ADDRESS 0 OF EACH 4K MEMORY SIMULATOR RAM
5822
5823  015656  125252                      .WORD   125252
5824  015660  052525                      .WORD   052525
5825  015662  177777                      .WORD   177777
5826  015664  000000                      .WORD   000000
5827
5828  015666              31$:    ENDTST
5829  015666              L10037:
5830  015666  104401                      TRAP    C$ETST
5831
```

B 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 118
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0118

```
5832                              .SBTTL  TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE
5833
5834                         ;++
5835                         ;          THIS TEST WILL CHECK THAT DATA WRITTEN INTO ADDRESS 0 AND 2 OF THE
5836                         ;          MEMORY SIMULATOR RAM CAN BE ENABLED TO THE TARGET EMULATOR MODULE VIA
5837                         ;          THE LOW BYTE OF THE SYSTEM DATA BUS WHEN A "READ" OPERATION IS BEING
5838                         ;          EXECUTED FROM THE TARGET EMULATOR MODULE IN 8 BIT MODE.  THE TARGET
5839                         ;          EMULATOR MODULE WILL BE SETUP TO 8 BIT MODE AND THE MEMORY SIMULATOR
5840                         ;          MODULE WILL BE SETUP TO 8 BIT MODE AFTER THE DATA HAS BEEN WRITTEN INTO
5841                         ;          THE MEMORY SIMULATOR RAM AND CHECKED.  ADDRESS 0 AND 2 OF THE MEMORY
5842                         ;          SIMULATOR RAM WILL BE WRITTEN WITH A DATA PATTERN OF 125125 AND 052652
5843                         ;          RESPECTIVELY.  ADDRESSES 0, 1, 2 AND 3 OF THE MEMORY SIMULATOR RAM WILL
5844                         ;          BE ADDRESSED VIA THE TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER WHEN
5845                         ;          A NORMAL T-11 TIMING CYCLE OCCURS.  A NORMAL T-11 TIMING CYCLE OCCURS
5846                         ;          WHEN RAS, CAS AND PI ARE ASSERTED IN THE ORDER GIVEN AND THEN DE-ASSERTED
5847                         ;          IN THE FOLLOWING ORDER CAS, PI AND THEN RAS.  THE PROGRAM WILL CHECK
5848                         ;          THAT THE SYSTEM ADDRESS BUS WAS CLOCKED INTO THE MEMORY SIMULATORS
5849                         ;          SYSTEM ADDRESS BUS LATCHES WHEN THE SIGNAL PRAS H WAS ASSERTED HIGH ON
5850                         ;          THE TARGET EMULATOR MODULE.  WHEN THE TARGET EMULATOR SIGNALS XR/WLB H,
5851                         ;          XRAS H, XCAS H AND MR11 H ARE ASSERTED HIGH, THE TARGET EMULATOR SIGNALS
5852                         ;          "READ H" AND "MSDI H" WILL BE ASSERTED HIGH.  THE SIGNAL "READ H" BEING
5853                         ;          ASSERTED WILL ENABLE THE LOW BYTE OF MEMORY SIMULATOR RAM DATA TO THE
5854                         ;          LOW BYTE OF THE SYSTEM DATA BUS IF THE ADDRESS WAS EVEN, OR THE HIGH
5855                         ;          BYTE OF THE MEMORY SIMULATOR RAM DATA WILL BE ENEBALED TO THE LOW BYTE
5856                         ;          OF THE SYSTEM DATA BUS IF THE ADDRESS WAS ODD.  THE DATA ENABLED TO
5857                         ;          THE LOW BYTE OF THE SYSTEM DATA BUS WILL BE 125, 252, 252 AND 125 FOR
5858                         ;          ADDRESSES 0, 1, 2 AND 3 RESPECTIVELY.  THE SYSTEM DATA BUS WILL BE
5859                         ;          ENABLED TO THE LOW BYTE OF THE TARGET EMULATOR'S EODAL BUS VIA THE
5860                         ;          SIGNAL "MSDI H" AND THE LOW BYTE OF THE EODAL BUS WILL BE ENABLED TO
5861                         ;          THE LOW BYTE OF THE TARGET EMULATOR'S EIDAL BUS VIA THE SIGNAL "COLB L".
5862                         ;          THE SIGNAL "COLB L" WILL BE ASSERTED LOW AS A RESULT OF THE SIGNALS
5863                         ;          ETR L, PR/WLB H, PPI H AND DMG L BEING ASSERTED HIGH.  THE PROGRAM WILL
5864                         ;          READ AND CHECK THE TARGET EMULATORS EODAL AND EIDAL BUSES TO CONTAIN THE
5865                         ;          EXPECTED BYTE OF MEMORY SIMULATOR RAM DATA.
5866                         ;--
5867
5868  015670                     BGNTST
5869  015670                 T4::
5870  015670  004737  007440     JSR    PC,INITMD               ;INITIALIZE MDE/T-11 SYSTEM MODULES
5871
5872  015674                     BGNSEG
5873  015674  104404             TRAP   C$BSEG
5874
5875                         ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5876                         ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5877
5878  015676  004737  012214     JSR    PC,SLCTTE               ;SELECT TARGET EMULATOR MODULE
5879
5880                         ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL "BRKRES L"
5881                         ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
5882                         ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
5883                         ;THE SIGNAL "BRKRES L" VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
5884                         ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
5885                         ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED VIA THE
5886                         ;THE SIGNAL "RASP L" LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
5887                         ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
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C 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 119
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0119

```
5888                                                    ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
5889
5890   015702  012737  043020  002334          MOV     #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
5891   015710  004737  012766                  JSR     PC,BRKRES               ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
5892
5893                                                    ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
5894                                                    ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
5895                                                    ;REGISTER 6.
5896
5897   015714  004537  012234                  JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
5898   015720  000003                          .WORD   HDAL                   ;SELECT THE HDAL REGISTER
5899
5900                                                    ;SET HDAL REGISTER BITS 9,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
5901                                                    ;ZERO.  HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
5902                                                    ;AND CONTROL SIGNALS.  HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
5903                                                    ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS.  HDAL REGISTER
5904                                                    ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
5905                                                    ;HDAL REGISTER BIT 4 ON A ZERO AND BIT3 ON A ONE WILL SET THE SIGNAL
5906                                                    ;XR/WHB H LOW AND XR/WLB H HIGH RESPECTIVELY.  THESE TWO SIGNALS SET TO
5907                                                    ;THIS STATE WILL CAUSE THE SIGNAL 'REAT H' TO BE ASSERTED HIGH LATER IN
5908                                                    ;THIS TEST WHEN THE SIGNALS XRAS H AND XCAS H ARE ASSERTED HIGH.
5909
5910   015722  012737  001014  002346          MOV     #HDAL9!HDAL3!HDAL2,T6LOAD  ;SET HDAL BITS 9,3 + 2 TO ONES
5911   015730  005037  002352                  CLR     T6MASK                 ;SETUP MASK TO CHECK ALL BITS
5912   015734  004737  011216                  JSR     PC,LDRDT6              ;GO LOAD, READ AND CHECK HDAL REGISTER
5913   015740  001405                          BEQ     1$                     ;IF LOADED OK THEN CONTINUE
5914   015742                                  ERRDF   12,HDALRG,T06ERR       ;HDAL REGISTER NOT EQUAL EXPECTED
5915   015742  104455                          TRAP    C$ERDF
5916   015744  000014                          .WORD   12
5917   015746  003756                          .WORD   HDALRG
5918   015750  006732                          .WORD   T06ERR
5919   015752                                  CKLOOP
5920   015752  104406                          TRAP    C$CLP1
5921
5922                                                    ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
5923                                                    ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
5924                                                    ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
5925
5926   015754  005037  002340          1$:     CLR     T4LOAD                 ;SETUP TO CLEAR ALL OTHER R/W BITS
5927   015760  004737  012706                  JSR     PC,CLRPSM              ;PULSE INVD L VIA VDAL2 H
5928
5929                                                    ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON
5930                                                    ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
5931                                                    ;BE WRITTEN OR READ.
5932
5933   015764  004537  012234                  JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
5934   015770  000004                          .WORD   MODE                   ;SELECT THE MODE REGISTER
5935
5936                                                    ;LOAD, READ AND CHECK MODE REGISTER WITH MODE REGISTER BIT 11 SET TO A
5937                                                    ;ONE AND ALL OTHER MODE REGISTER BITS SET TO A ZERO.  WHEN MODE REGISTER
5938                                                    ;BIT 11 IS SET TO A ONE, 8 BIT MODE IS SELECTED.
5939
5940   015772  012737  004000  002346          MOV     #MR11,T6LOAD           ;SETUP BIT TO SELECT 8 BIT MODE
5941   016000  004737  011216                  JSR     PC,LDRDT6              ;GO LOAD, READ AND CHECK MODE REGISTER
5942   016004  001405                          BEQ     2$                     ;IF LOADED OK THEN CONTINUE
5943   016006                                  ERRDF   12,MODREG,T06ERR       ;MODE REGISTER NOT EQUAL EXPECTED
```

D 10

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46 PAGE 120
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0120

```
5944   016006  104455                           TRAP    C$ERDF
5945   016010  000014                           .WORD   12
5946   016012  004002                           .WORD   MODREG
5947   016014  006732                           .WORD   TO6ERR
5948   016016                                   CKLOOP
5949   016016  104406                           TRAP    C$CLP1
5950

5951                                   ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
5952                                   ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
5953                                   ;READ COMMAND TO CONTROL REGISTER 6..  THE EOAI REGISTER NEEDS FDALO H
5954                                   ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
5955                                   ;TER WILL BE ADDRESSED.
5956

5957   016020  004537  012234          2$:      JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
5958   016024  000002                           .WORD   FDAL                    ;SELECT EOAI AND FDAL REGISTER
5959

5960                                   ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER.  THE EOAI REGISTER WILL
5961                                   ;BE LOADED AND CHECKED FOR ZEROES.  THE FDAL REGISTER WILL BE LOADED AND
5962                                   ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
5963

5964   016026  012737  000001  002346           MOV     #FDALO,T6LOAD           ;SETUP EOAI AND FDAL REG DATA PATTERN
5965   016034  004737  011216                   JSR     PC,LDRDT6               ;GO LOAD, READ AND CHECK EOAI + FDAL REG
5966   016040  001405                            BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5967   016042                                   ERRDF   12,EOAIFD,TO6ERR        ;EOAI OR FDAL REGISTER ERROR
5968   016042  104455                            TRAP    C$ERDF
5969   016044  000014                            .WORD   12
5970   016046  004047                            .WORD   EOAIFD
5971   016050  006732                            .WORD   TO6ERR
5972   016052                                   CKLOOP
5973   016052  104406                            TRAP    C$CLP1
5974

5975                                   ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
5976                                   ;CHANGES OCCURED DOING THE PAST SEQUENCES.
5977

5978   016054  004737  011200          3$:      JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
5979   016060  001404                            BEQ     4$                      ;IF NO CHANGES THEN CONTINUE
5980   016062                                   ERRDF   11,VDALRG,T4EROR        ;VDAL OR PAUSE STATE MACHINE ERROR
5981   016062  104455                            TRAP    C$ERDF
5982   016064  000013                            .WORD   11
5983   016066  003710                            .WORD   VDALRG
5984   016070  006716                            .WORD   T4EROR
5985   016072                          4$:      ENDSEG
5986   016072                          10000$:
5987   016072  104405                            TRAP    C$ESEG
5988

5989   016074                                   BGNSEG
5990   016074  104404                            TRAP    C$BSEG
5991

5992                                   ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
5993                                   ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
5994

5995   016076  004737  011250                   JSR     PC,SLCTMS               ;SELECT MEMORY SIMULATOR MODULE
5996

5997                                   ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM.  THE
5998                                   ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H' AND 'MPIN H' SET TO
5999                                   ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM.  MAP PROTECTION RAM
```

E 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 121
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0121

```
6000                                              ;BITS 'WRE H' AND 'RDE H' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
6001                                              ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
6002                                              ;WHEN 'RDE H' AND 'WRE H' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
6003                                              ;TO THOSE ADDRESSES.
6004
6005    016102  004737  011356                    JSR     PC,MPRAM              ;GO LOAD, READ AND CHECK MAP PROTECT RAM
6006
6007                                              ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0.  THE FOLLOWING DATA
6008                                              ;PATTERNS; 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
6009                                              ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0.  THESE PATTERNS
6010                                              ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
6011                                              ;ADDRESSED.
6012
6013    016106  004737  011642                    JSR     PC,MSRAM0            ;LOAD, READ AND CHECK MODULE SELECT RAM 0
6014
6015                                              ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1.  THE FOLLOWING DATA PATTERNS
6016                                              ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
6017                                              ;AT ADDRESS 0; 17, 0, 0 AND 0.  THESE PATTERNS WILL ENABLE THE FIRST 32K
6018                                              ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
6019
6020    016112  004737  012012                    JSR     PC,MSRAM1            ;LOAD, READ AND CHECK MODULE SELECT RAM 1
6021
6022    016116  005037  002254                    CLR     S4LOAD               ;START ADDRESS AT ADDRESS ZERO
6023    016122  012737  125125  002260            MOV     #125125,S6LOAD       ;DATA PATTERN FOR ADDRESS ZERO
6024
6025    016130                            5$:     BGNSEG
6026    016130  104404                            TRAP    C$BSEG
6027
6028                                              ;LOAD MEMORY SIMULATOR RAM ADDRESS TO BE TESTED INTO CONTROL REGISTER 4.
6029                                              ;ADDRESSES TO BE LOADED ARE 0, 20000, 40000 AND 60000.
6030
6031    016132  004737  010606                    JSR     PC,LDRDS4            ;LOAD READ AND CHECK CONTROL REG 4
6032    016136  001405                            BEQ     6$                   ;IF LOADED OK THEN CONTINUE
6033    016140                                    ERRDF   3,MSADRG,S4EROR      ;MSAD 15:0 REGISTER ERROR
6034    016140  104455                            TRAP    C$ERDF
6035    016142  000003                            .WORD   3
6036    016144  002510                            .WORD   MSADRG
6037    016146  005336                            .WORD   S4EROR
6038    016150                                    CKLOOP
6039    016150  104406                            TRAP    C$CLP1
6040
6041                                              ;CLEAR BITS MSEL1 H, MSEL0 H, MSAD17 H AND MSAD16 H IN CONTROL REGISTER
6042                                              ;2.  MSEL0 H AND MSEL1 H ON A ZERO WILL CAUSE THE SIGNAL 'SSM L' TO BE
6043                                              ;ASSERTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.  ON A WRITE
6044                                              ;OR READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE WRITTEN INTO OR
6045                                              ;READ FROM MEMORY SIMULATOR RAM ADDRESSES BY CONTROL REGISTER 2 AND 4.
6046                                              ;THE MEMORY SIMULATOR RAM'S ARE ENABLED BY THE DATA PATTERNS PREVIOUSLY
6047                                              ;WRITTEN INTO MODULE SELECT RAMS 0 AND 1.  MSAD17 H AND MSAD16 H WILL BE
6048                                              ;LOADED AND CHECKED WITH ZEROES.  THE PROGRAM WILL EXPECT CONTROL REGIS-
6049                                              ;TER 2 BITS 'ESR H' AND 'WREN H' TO BE READ AS ONES AS A RESULT OF MAP
6050                                              ;PROTECTION RAM BITS 'MPIN H' AND 'WRE H' BEING SET TO ONES.
6051
6052    016152  005037  002244            6$:     CLR     S2LOAD               ;SET ALL BITS IN REG 2 TO ZEROES
6053    016156  013737  002244  002246            MOV     S2LOAD,S2GOOD        ;COPY DATA LOADED TO EXPECTED
6054    016164  052737  000140  002246            BIS     #ESRH!WRENH,S2GOOD   ;EXPECT ESR H AND WREN H TO BE ONES
6055    016172  012737  177400  002250            MOV     #177400,S2MASK       ;SETUP TO COMPARE LOW BYTE
```

F 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 122
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0122

```
6056   016200  004737  010554              JSR     PC,LDRD2S          ;LOAD, READ AND CHECK CONTROL REG 2
6057   016204  001405                       BEQ     7$                 ;IF LOADED OK THEN CONTINUE
6058   016206                               ERRDF   2,,S2EROR          ;CONTROL REGISTER 2 NOT = EXPECTED
6059   016206  104455                       TRAP    C$ERDF
6060   016210  000002                       .WORD   2
6061   016212  000000                       .WORD   0
6062   016214  005322                       .WORD   S2EROR
6063   016216                               CKLOOP
6064   016216  104406                       TRAP    C$CLP1
6065
6066                                         ;LOAD DATA PATTERN INTO MEMORY SIMULATOR RAM ADDRESSED BY CONTROL
6067                                         ;REGISTER 2 AND 4.  THE ADDRESS AND DATA PATTERN LOADED ARE AS FOLLOWS:
6068                                         ;        ADDRESS           DATA
6069                                         ;        000000            125125
6070                                         ;        000002            052652
6071
6072   016220  005037  002264      7$:      CLR     S6MASK             ;SETUP TO COMPARE ALL BITS
6073   016224  004737  010632               JSR     PC,LDRDS6          ;GO LAOD, READ AND CHECK RAM LOCATION
6074   016230  001404                       BEQ     8$                 ;IF LOADED OK THEN CONTINUE
6075   016232                               ERRDF   4,MSGMSR,S6ALLR    ;DATA ERROR IN MEMORY SIMULATOR RAM
6076   016232  104455                       TRAP    C$ERDF
6077   016234  000004                       .WORD   4
6078   016236  002745                       .WORD   MSGMSR
6079   016240  005456                       .WORD   S6ALLR
6080   016242                      8$:      ENDSEG
6081   016242                      10002$:
6082   016242  104405                       TRAP    C$ESEG
6083
6084   016244  005737  002254               TST     S4LOAD             ;CHECK IF FIRST TIME THROUGH
6085   016250  001006                       BNE     9$                 ;IF NOT THEN ADDRESS 0 AND 2 LOADED
6086   016252  062737  000002  002254       ADD     #2,S4LOAD          ;UPDATE ADDRESS TO ADDRESS 2
6087   016260  005137  002260               COM     S6LOAD             ;1'S COMPLEMEMT THE DATA
6088   016264  000721                       BR      5$                 ;GO LOAD ADDRESS 2 WITH 052652
6089
6090                                         ;SET THE SIGNALS "CTS H" AND "8BIT H" TO ONES IN CONTROL REGISTER 0.
6091                                         ;"CTS H" ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO THE MEMORY
6092                                         ;SIMULATOR LOGIC.  IN THIS TEST, "CTS H" ON A ONE WILL ENABLE THE
6093                                         ;SYSTEM BUS ADDRESSES TO THE MEMORY SIMULATOR MODULE AND THE MEMORY
6094                                         ;SIMULATOR RAM DATA ONTO THE SYSTEM BUS IN 8 BIT MODE.  THE SIGNAL
6095                                         ;"8BIT H" ON A ONE WILL ENABLE 8 BIT ADDRESSING AND DATA MODE.  EITHER
6096                                         ;THE HIGH OR LOW BYTE OF RAM DATA WILL BE ENABLED TO THE LOW BYTE OF THE
6097                                         ;SYSTEM BUS DEPENDING UPON THE ADDRESS SELECTED.
6098
6099   016266  052737  000012  002234  9$:  BIS     #CTSH!BIT8H,S0LOAD ;SETUP BIT TO BE LOADED
6100   016274  004737  010506               JSR     PC,LDRDS0          ;GO LOAD, READ AND CHECK CONTROL REG 2
6101   016300  001404                       BEQ     10$                ;IF LOADED OK THEN CONTINUE
6102   016302                               ERRDF   1,,S0EROR          ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
6103   016302  104455                       TRAP    C$ERDF
6104   016304  000001                       .WORD   1
6105   016306  000000                       .WORD   0
6106   016310  005306                       .WORD   S0EROR
6107   016312                      10$:     ENDSEG
6108   016312                      10001$:
6109   016312  104405                       TRAP    C$ESEG
5110
6111   016314  012701  016744               MOV     #30$,R1            ;GET POINTER TO ADDRESS AND DATA TABLES
```

G 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 123
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0123

```
 6112
 6113   016320                              11$:    BGNSEG
 6114   016320  104404                              TRAP    C$BSEG
 6115
 6116                                        ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
 6117                                        ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
 6118
 6119   016322  004737  012214                      JSR     PC,SLCTTE
 6120
 6121                                        ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
 6122                                        ;2:0 TO A 0.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
 6123                                        ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.  THE DIAGNOSTIC
 6124                                        ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
 6125                                        ;BIT 9 BEING SET TO A ONE PREVIOULSY.  ON A READ COMMAND TO CONTROL
 6126                                        ;REGISTER 6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
 6127
 6128   016326  004537  012234                      JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
 6129   016332  000000                              .WORD   ADDRES                  ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
 6130
 6131                                        ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
 6132                                        ;FOLLOWING ADDRESSES DEPENDING UPON THE ADDRESS BEING TESTED: 0,1,2 OR 3.
 6133
 6134   016334  011137  002346                      MOV     (R1),T6LOAD             ;GET THE TEST ADDRESS FROM THE TABLE
 6135   016340  005037  002352                      CLR     T6MASK                  ;SETUP TO CHECK ALL 16 BITS
 6136   016344  004737  011216                      JSR     PC,LDRDT6               ;GO LOAD, READ AND CHECK DIAG ADDRESS REG
 6137   016350  001405                              BEQ     12$                     ;IF LOADED OK THEN CONTINUE
 6138   016352                                      ERRDF   12,ADDRRG,T06ERR        ;DIAGNOSTIC ADDRESS REGISTER ERROR
 6139   016352  104455                              TRAP    C$ERDF
 6140   016354  000014                              .WORD   12
 6141   016356  004144                              .WORD   ADDRRG
 6142   016360  006732                              .WORD   T06ERR
 6143   016362                                      CKLOOP
 6144   016362  104406                              TRAP    C$CLP1
 6145
 6146                                        ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3.  THE
 6147                                        ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
 6148                                        ;CONTROL REGISTER 6.
 6149
 6150   016364  004537  012234              12$:    JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
 6151   016370  000003                              .WORD   HDAL                    ;SELECT THE HDAL REGISTER
 6152
 6153                                        ;RELOAD HDAL REGISTER BITS FOR SCOPE LOOPING PURPOSES ONLY.  THIS IS
 6154                                        ;DONE TO SET ALL THE TIMING SIGNALS BACK TO THE NON-ASSERTED STATE.
 6155
 6156   016372  012737  001014  002346              MOV     #HDAL9!HDAL3!HDAL2,T6LOAD ;GET BITS PREVIOUSLY LOADED
 6157   016400  004737  011216                      JSR     PC,LDRDT6               ;LOAD, READ AND CHECK HDAL REGISTER
 6158   016404  001405                              BEQ     13$                     ;IF LOADED OK THEN CONTINUE
 6159   016406                                      ERRDF   12,HDALRG,T06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
 6160   016406  104455                              TRAP    C$ERDF
 6161   016410  000014                              .WORD   12
 6162   016412  003756                              .WORD   HDALRG
 6163   016414  006732                              .WORD   T06ERR
 6164   016416                                      CKLOOP
 6165   016416  104406                              TRAP    C$CLP1
 6166
 6167                                        ;START A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE
```

H 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 124
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0124

```
6168                                                    ;   1.   SET XRAS H AND PRAS H TO THE HIGH STATE
6169                                                    ;   2.   SET XCAS H AND PCAS H TO THE HIGH STATE
6170                                                    ;   3.   SET XPI L AND PPI L TO THE LOW STATE
6171                                                    ;SETTING THE SIGNAL PRAS H TO THE HIGH STATE WILL CAUSE THE SIGNAL
6172                                                    ;"ADVAL H" TO GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE SYSTEM
6173                                                    ;ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR ADDRESS BUS LATCHES.
6174                                                    ;WHEN THE SIGNALS XRAS H AND XCAS H ARE ASSERTED HIGH,  THE SIGNAL REAT H
6175                                                    ;WILL GO FROM A LOW TO A HIGH STATE, THUS CAUSING THE SIGNAL READ H TO
6176                                                    ;GO FROM A LOW TO A HIGH STATE.  THE TARGET EMULATORS SIGNAL READ H
6177                                                    ;ALONG WITH THE MEMORY SIMULATOR;S SIGNALS CTS H AND ESR H WILL CAUSE
6178                                                    ;THE MEMORY SIMULATOR RAM DATA TO BE PUT ONTO THE SYSTEM DATA BUS.  IF THE
6179                                                    ;ADDRESS IS ODD IN 8 BIT MODE, THE HIGH BYTE OF THE RAM LOCATION WILL BE
6180                                                    ;ENABLED TO THE LOW BYTE OF THE DATA BUS.  WHEN THE TARGET EMULATOR'S
6181                                                    ;SIGNAL REAT H IS ASSERTED HIGH, THE TARGET EMULATOR'S SIGNAL MSDI H
6182                                                    ;WILL BE ASSERTED HIGH THUS ENABLING THE SYSTEM DATA BUS TO THE TARGET
6183                                                    ;EMULATOR'S EODAL BUS.  IN 8 BIT MODE, ALL DATA WILL BE READ IN ON THE
6184                                                    ;LOW BYTE OF THE EODAL BUS.  THE MEMORY SIMULATOR RAMS ARE ADDRESSED BY
6185                                                    ;THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES WHICH WERE CLOCKED BY
6186                                                    ;THE SIGNAL ADVAL H.  THE DATA ON THE SYSTEM ADDRESS BUS COMES FROM THE
6187                                                    ;TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER.
6188
6189    016420  004737  012300          13$:    JSR     PC,XRASH                ;SET XRAS H AND PRAS H TO HIGH STATE
6190    016424  004737  012404                 JSR     PC,XCASH                ;SET XCAS H AND PCAS H TO HIGH STATE
6191    016430  004737  012510                 JSR     PC,XPIH                 ;SET XPI H AND PPI H TO THE LOW STATE
6192
6193                                                    ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H ARE
6194                                                    ;ASSERTED HIGH (1'S).
6195
6196    016434  012737  000110  002342         MOV     #VDAL6!VDAL3,T4GOOD     ;EXPECT READ H AND MSDI H TO BE ONES
6197    016442  004737  011200                 JSR     PC,READT4               ;READ VDAL AND PAUSE STATE MACHINE REG
6198    016446  001405                          BEQ     14$                     ;IF DATA OK THEN CONTINUE
6199    016450                                  ERRDF   11,VDALRG,T4EROR        ;VDAL OR PAUSE STATE MACHINE ERROR
6200    016450  104455                          TRAP    C$ERDF
6201    016452  000013                          .WORD   11
6202    016454  003710                          .WORD   VDALRG
6203    016456  006716                          .WORD   T4EROR
6204    016460                                  CKLOOP
6205    016460  104406                          TRAP    C$CLP1
6206
6207                                                    ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6208                                                    ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6209
6210    016462  004737  011250          14$:    JSR     PC,SLCTMS               ;SELECT THE MEMORY SIMULATOR MODULE
6211
6212                                                    ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
6213                                                    ;TARGET EMULATOR MODULE SET THE SIGNALS ADVAL H AND READ H TO THE
6214                                                    ;HIGH STATE FROM THE LOW STATE.
6215
6216    016466  004737  010522                 JSR     PC,READS0               ;READ AND CHECK CONTROL REGISTER 0
6217    016472  001405                          BEQ     15$                     ;IF NO CHANGES THEN CONTINUE
6218    016474                                  ERRDF   1,,S0EROR               ;CONTROL REGISTER 0 NOT = EXPECTED
6219    016474  104455                          TRAP    C$ERDF
6220    016476  000001                          .WORD   1
6221    016500  000000                          .WORD   0
6222    016502  005306                          .WORD   S0EROR
6223    016504                                  CKLOOP
```

I 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 125
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0125

```
6224   016504  104406                          TRAP     C$CLP1
6225
6226                                           ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
6227                                           ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
6228                                           ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.  THE SIGNAL ADVAL H
6229                                           ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
6230                                           ;SIGNAL PRAS H WAS SET HIGH FROM THE LOW STATE.  THE MEMORY SIMULATORS
6231                                           ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
6232                                           ;BITS VIA THE SIGNALS CTS H AND CTS L.
6233
6234   016506  011137  002254     15$:        MOV      (R1),S4LOAD        ;GET TE DIAG ADDRESS REG DATA LOADED
6235   016512  004737  010614                 JSR      PC,READS4          ;READ AND CHECK CONTROL REGISTER 4
6236   016516  001405                          BEQ      16$                ;IF DATA = TE DIAG ADDRESS REG - CONT
6237   016520                                  ERRDF    3,TEMSAD,S04ERR    ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
6238   016520  104455                          TRAP     C$ERDF
6239   016522  000003                          .WORD    3
6240   016524  002534                          .WORD    TEMSAD
6241   016526  005406                          .WORD    S04ERR
6242   016530                                  CKLOOP
6243   016530  104406                          TRAP     C$CLP1
6244
6245                                           ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
6246                                           ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
6247                                           ;ZEROES FOR THESE TWO ADDRESSES.  ADDRESS BITS 17 AND 16 WERE CLOCKED
6248                                           ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
6249                                           ;ADVAL H.  THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
6250                                           ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE FROM
6251                                           ;THE LOW STATE.  THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
6252                                           ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
6253                                           ;MEMORY SIMULATOR MODULE.
6254
6255   016532  052737  000014  002250  16$:   BIS      #MSEL0!MSEL1,S2MASK ;IGNORE TRI-STATED BITS WHEN CTS H SET
6256   016540  005037  002244                 CLR      S2LOAD             ;EXPECT MSAD 17:16 TO BE ZERO
6257   016544  013737  002244  002246         MOV      S2LOAD,S2GOOD      ;COPY DATA LOADED TO EXPECTED
6258   016552  052737  000140  002246         BIS      #ESRH!WRENH,S2GOOD ;EXPECT MAP PROTECT BITS TO BE ONES
6259   016560  004737  010562                 JSR      PC,READS2          ;READ AND CHECK CONTROL REGISTER 2
6260   016564  001405                          BEQ      17$                ;IF DATA OK THEN CONTINUE
6261   016566                                  ERRDF    2,TEMSA1,S02ERR    ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
6262   016566  104455                          TRAP     C$ERDF
6263   016570  000002                          .WORD    2
6264   016572  002410                          .WORD    TEMSA1
6265   016574  005366                          .WORD    S02ERR
6266   016576                                  CKLOOP
6267   016576  104406                          TRAP     C$CLP1
6268
6269                                           ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6270                                           ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6271
6272   016600  004737  012214     17$:        JSR      PC,SLCTTE          ;SELECT THE TARGET EMULATOR MODULE
6273
6274                                           ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO A 7.  THE EODAL BUS
6275                                           ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
6276
6277   016604  004537  012234                 JSR      R5,SELTER          ;SELECT REGISTER SPECIFIED BY NEXT WORD
6278   016610  000007                          .WORD    EODAL              ;SELECT THE EODAL BUS TO BE READ
6279
```

J 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 126
C.VCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0126

```
6280                                                    ;AT THIS TIME THE MEMORY SIMULATOR RAM DATA SHOULD BE ENABLED ON THE
6281                                                    ;SYSTEM DATA BUS AND ENABLED TO THE TARGET EMULATORS EODAL BUS VIA THE
6282                                                    ;TARGET EMULATOR SIGNALS READ H AND MSDI H RESPECTIVELY.  IF THE ADDRESS
6283                                                    ;IS ODD IN 8 BIT MODE, THE HIGH BYTE OF RAM LOCATION IS ENABLED TO THE
6284                                                    ;LOW BYTE OF THE MDE/T-11 SYSTEM DATA BUS.   THE MEMORY SIMULATOR RAM IS
6285                                                    ;ADDRESSED BY THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER WHICH
6286                                                    ;WAS CLOCKED INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA TA
6287                                                    ;THE SIGNAL ADVAL H.  THE ADDRESSES AND DATA PATTERNS STORED IN THE RAM
6288                                                    ;ADDRESSES SELECTED ARE AS FOLLOWS:
6289                                                    ;       RAM ADDRESS 0 LOW BYTE WAS LOADED WITH 125
6290                                                    ;       RAM ADDRESS 0 HIGH BYTE WAS LOADED WITH 252
6291                                                    ;       RAM ADDRESS 2 LOW BYTE WAS LOADED WITH 252
6292                                                    ;       RAM ADDRESS 2 HIGH BYTE WAS LOADED WITH 125
6293
6294    016612   016137  000010  002346          MOV     10(R1),T6LOAD            ;GET DATA LOADED INTO MS RAM ADDRESSED
6295    016620   012737  177400  002352          MOV     #177400,T6MASK          ;SETUP TO IGNORE HIGH BYTE
6296    016626   004737  011224                  JSR     PC,READT6               ;READ SYSTEM DATA BUS ON THE EODAL BUS
6297    016632   001405                           BEQ     18$                     ;IF DATA = MS RAM DATA THEN CONTINUE
6298    016634                                    ERRDF   12,MSTEDE,T6ALLR        ;MS RAM DATA TO TE EODAL BUS ERROR
6299    016634   104455                           TRAP    C$ERDF
6300    016636   000014                           .WORD   12
6301    016640   004243                           .WORD   MSTEDE
6302    016642   006746                           .WORD   T6ALLR
6303    016644                                    CKLOOP
6304    016644   104406                           TRAP    C$CLP1
6305
6306                                                    ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
6307                                                    ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
6308                                                    ;REGISTER 6.
6309
6310    016646   004537  012234          18$:    JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
6311    016652   000003                           .WORD   HDAL                    ;SELECT THE HDAL REGISTER
6312
6313                                                    ;FINISH THE T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
6314                                                    ;   1. SET XCAS H AND PCAS H TO THE LOW STATE
6315                                                    ;   2. SET XPI L AND PPI L TO THE HIGH STATE
6316                                                    ;   3. SET XRAS H AND PRAS H TO THE LOW STATE
6317
6318    016654   012737  001034  002346          MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
6319    016662   005037  002352                  CLR     T6MASK                  ;SETUP TO CHECK ALL 16 BITS
6320    016666   004737  012436                  JSR     PC,XCASL                ;SET XCAS H AND PCAS H TO LOW STATE
6321    016672   004737  012542                  JSR     PC,XPIL                 ;SET XPI L AND PPI L TO THE HIGH STATE
6322    016676   004737  012332                  JSR     PC,XRASL                ;SET XRAS H AND PRAS H TO LOW STATE
6323
6324                                                    ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H
6325                                                    ;WENT TO A ZERO AS A RESULT OF SETTING THE SIGNALS XCAS H AND XRAS H
6326                                                    ;TO THE LOW STATE.  CHECK THAT THE SIGNAL EDEOC H WENT TO A ONE AS
6327                                                    ;A RESULT OF XRAS H AND XCAS H BEING SET LOW AND THE SINGLE STEP SYNC
6328                                                    ;FLIP-FLOP BEING SET TO A ONE VIA XCAS H.
6329
6330    016702   012737  000020  002342          MOV     #VDAL4,T4GOOD           ;EXPECT EDEOC H TO BE SET TO A ONE
6331    016710   004737  011200                  JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
6332    016714   001404                           BEQ     19$                     ;IF OK THEN CONTINUE
6333    016716                                    ERRDF   11,VDALRG,T4EROR        ;VDAL OR PAUSE STATE MACHINE ERROR
6334    016716   104455                           TRAP    C$ERDF
6335    016720   000013                           .WORD   11
```

K 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 127
CVCDDB.P11   14-JUN-82 09:54   TEST 4: CHECK DATA BUS TO TE FROM MS - 8 BIT MODE   SEQ 0127

```
6336   016722  003710                  .WORD    VDALRG
6337   016724  006716                  .WORD    T4EROR
6338   016726                  19$:    ENDSEG
6339   016726                  10003$:
6340   016726  104405                  TRAP     C$ESEG
6341
6342   016730  005761  000012          TST      12(R1)          ;CHECK IF THIS WAS LAST DATA PATTERN
6343   016734  001414                  BEQ      31$             ;IF YES THEN END OF TEST
6344   016736  005721                  TST      (R1)+           ;UPDATE POINTER TO ADDRESS TABLE
6345   016740  000137  016320          JMP      11$             ;GO CHECK NEXT DATA PATTERN
6346
6347                                    ;DATA PATTERN FOR ADDRESS BITS 15:0 TO BE LOADED INTO DIAGNOSTIC ADDRESS
6348                                    ;REGISTER.
6349
6350   016744  000000          30$:    .WORD    000000
6351   016746  000001                  .WORD    000001
6352   016750  000002                  .WORD    000002
6353   016752  000003                  .WORD    000003
6354
6355                                    ;DATA PATTERN FOR ADDRESSES 0 AND 2 OF THE 1ST 4K OF MEMORY SIMULATOR RAM
6356
6357   016754  000125                  .WORD    125             ;DATA FOR LOW BYTE OF ADDRESS 0  (0)
6358   016756  000252                  .WORD    252             ;DATA FOR HIGH BYTE OF ADDRESS 0 (1)
6359   016760  000252                  .WORD    252             ;DATA FOR LOW BYTE OF ADDRESS 2  (2)
6360   016762  000125                  .WORD    125             ;DATA FOR HIGH BYTE OF ADDRESS 2 (3)
6361   016764  000000                  .WORD    0               ;TABLE TERMINATOR
6362
6363   016766                  31$:    ENDTST
6364   016766                  L10040:
6365   016766  104401                  TRAP     C$ETST
6366
```

L 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 128
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0128

```
6367                                    .SBTTL  TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE
6368
6369                                    ;++
6370                                    ;       THIS TEST WILL CHECK THAT DATA FROM THE MEMORY SIMULATOR RAM CAN BE
6371                                    ;       ENABLED TO THE TARGET EMULATOR'S TDAL BUS AND CLOCKED INTO THE TDAL
6372                                    ;       DIAGNOSTIC LATCHES WHEN A 'READ' OPERATION IS BEING EXECUTED FROM THE
6373                                    ;       TARGET EMULATOR MODULE.  THE TEST WILL CHECK THAT THE TDAL DIAGNOSTIC
6374                                    ;       LATCHES CAN BE ENABLED TO THE SYSTEM DATA BUS AND THAT THE SYSTEM DATA
6375                                    ;       BUS CAN BE WRITTEN BACK INTO THE MEMORY SIMULATOR RAM LOCATION WHEN A
6376                                    ;       'WRITE' OPERATION IS BEING EXECUTED FROM THE TARGET EMULATOR MODULE.
6377                                    ;       THE TEST WILL INITIALLY LOAD AND CHECK MEMORY SIMULATOR RAM LOCATIONS
6378                                    ;       000000, 020000, 040000 AND 060000 WITH DATA PATTERNS 125252, 146314,
6379                                    ;       000377 AND 000000 RESPECTIVELY.  ONCE EACH LOCATION HAS BEEN WRITTEN AND
6380                                    ;       CHECKED, THE PROGRAM WILL ISSUE A 'READ' OPERATION FROM THE TARGET
6381                                    ;       EMULATOR MODULE TO ONE OF THE MEMORY SIMULATOR RAM LOCATIONS AND CHECK
6382                                    ;       THAT THE DATA IS PRESENT ON THE TARGET EMULATOR'S EODAL AND EIDAL BUSES.
6383                                    ;       MEMORY SIMULATOR RAM DATA WILL ALSO BE ENABLED TO THE TARGET EMULATOR'S
6384                                    ;       TDAL BUS.  TO CAPTURE THIS DATA, THE PROGRAM MUST SET AND CLEAR THE
6385                                    ;       SIGNAL 'VDAL2 H' TO CLOCK THE TDAL BUS DATA INTO THE TDAL DIAGNOSTIC
6386                                    ;       LATCHES.  ONCE MEMORY SIMULATOR RAM DATA HAS BEEN CLOCKED INTO THE TDAL
6387                                    ;       DIAGNOSTIC LATCHES, THE PROGRAM WILL WRITE THE ONE'S COMPLEMENT OF THE
6388                                    ;       INITIAL MEMORY SIMULATOR RAM DATA BACK INTO THE LOCATION ADDRESSED AND
6389                                    ;       THEN CHECK THAT THE LOCATION CONTAINS THE ONE'S COMPLEMENT OF THE
6390                                    ;       INITIAL DATA.  THE PROGRAM WILL NOW ENABLE THE TDAL DIAGNOSTIC LATCHES,
6391                                    ;       WHICH CONTAINS THE INITIAL MEMORY SIMULATOR RAM DATA, TO THE SYSTEM DATA
6392                                    ;       BUS AND THEN WRITE THIS DATA VIA A 'WRITE' OPERATION FROM THE TARGET
6393                                    ;       EMULATOR MODULE BACK INTO THE MEMORY SIMULATOR RAM LOCATION INITIALLY
6394                                    ;       READ.  THE PROGRAM WILL NOW READ AND CHECK THE MEMORY SIMULATOR RAM
6395                                    ;       LOCATION TO CONTAIN THE INITIAL DATA.
6396                                    ;--
6397
6398    016770                          BGNTST
6399    016770                  T5::
6400    016770  004737  007440          JSR     PC,INITMD               ;INITIALIZE MDE/T-11 SYSTEM MODULES
6401
6402                                    ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6403                                    ;REGISTER O WITH THE USER DEFINED DEVICE NUMBER.
6404
6405    016774  004737  011250          JSR     PC,SLCTMS               ;SELECT MEMORY SIMULATOR MODULE
6406
6407                                    ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM.  THE
6408                                    ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H' AND 'MPIN H' SET TO
6409                                    ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM.  MAP PROTECTION RAM
6410                                    ;BITS 'WRE H' AND 'RDE H' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
6411                                    ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
6412                                    ;WHEN 'RDE H' AND 'WRE H' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
6413                                    ;TO THOSE ADDRESSES.
6414
6415    017000  004737  011356          JSR     PC,MPRAM                ;GO LOAD, READ AND CHECK MAP PROTECT RAM
6416
6417                                    ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0.  THE FOLLOWING DATA
6418                                    ;PATTERNS: 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
6419                                    ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0.  THESE PATTERNS
6420                                    ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
6421                                    ;ADDRESSED.
6422
```

M 10

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82   13:46   PAGE 129
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0129

```
6423   017004  004737  011642                    JSR     PC,MSRAM0              ;LOAD, READ AND CHECK MODULE SELECT RAM 0
6424
6425                                              ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1.  THE FOLLOWING DATA PATTERNS
6426                                              ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
6427                                              ;AT ADDRESS 0; 17, 0, 0 AND 0.  THESE PATTERNS WILL ENABLE THE FIRST 32K
6428                                              ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
6429
6430   017010  004737  012012                    JSR     PC,MSRAM1              ;LOAD, READ AND CHECK MODULE SELECT RAM 1
6431
6432   017014  005001                             CLR     R1                    ;SETUP STARTING ADDRESS TO EQUAL ZERO
6433   017016  012702  021110                     MOV     #50$,R2               ;SETUP POINTER TO DATA TABLE
6434   017022  012703  000002                     MOV     #2,R3                 ;SETUP TO DO EACH ADDRESS TWICE
6435
6436   017026                           1$:       BGNSEG
6437   017026  104404                             TRAP    C$BSEG
6438
6439                                              ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6440                                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6441
6442   017030  004737  012214                     JSR     PC,SLCTTE             ;SELECT TARGET EMULATOR MODULE
6443
6444                                              ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL 'BRKRES L'
6445                                              ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
6446                                              ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
6447                                              ;THE SIGNAL 'BRKRES L' VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
6448                                              ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
6449                                              ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL 'CKAI H' TO BE PULSED VIA THE
6450                                              ;THE SIGNAL 'RASP L' LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
6451                                              ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
6452                                              ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
6453
6454   017034  012737  043020  002334             MOV     #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
6455   017042  004737  012766                     JSR     PC,BRKRES             ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
6456
6457                                              ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
6458                                              ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
6459                                              ;REGISTER 6.
6460
6461   017046  004537  012234                     JSR     R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
6462   017052  000003                             .WORD   HDAL                  ;SELECT THE HDAL REGISTER
6463
6464                                              ;SET HDAL REGISTER BITS 9,4,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
6465                                              ;ZERO.  HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
6466                                              ;AND CONTROL SIGNALS.  HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
6467                                              ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS.  HDAL REGISTER
6468                                              ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
6469                                              ;HDAL REGISTER BITS 4 AND 3 SET TO ONES WILL SET THE SIGNALS XR/WLB H
6470                                              ;AND XR/WHB H TO THE HIGH STATE.  THESE SIGNALS WILL CAUSE THE SIGNAL
6471                                              ;'REAT H' TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE SIGNALS XRAS H
6472                                              ;AND XCAS H ARE ASSERTED HIGH.
6473
6474   017054  012737  001034  002346             MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,4,3 + 2 TO ONES
6475   017062  004737  011216                     JSR     PC,LDRDT6             ;GO LOAD, READ AND CHECK HDAL REGISTER
6476   017066  001405                             BEQ     2$                    ;IF LOADED OK THEN CONTINUE
6477   017070                                     ERRDF   12,HDALRG,T06ERR      ;HDAL REGISTER NOT EQUAL EXPECTED
6478   017070  104455                             TRAP    C$ERDF
```

N 10

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 130
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0130

```
6479   017072   000014                       .WORD    12
6480   017074   003756                       .WORD    HDALRG
6481   017076   006732                       .WORD    TO6ERR
6482   017100                                CKLOOP
6483   017100   104406                       TRAP     C$CLP1
6484
6485                                   ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
6486                                   ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
6487                                   ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY "BRKRES L".
6488
6489   017102   005037   002340   2$:  CLR     T4LOAD           ;SETUP TO CLEAR ALL OTHER R/W BITS
6490   017106   004737   012706        JSR     PC,CLRPSM        ;PULSE INVD L VIA VDAL2 H
6491
6492                                   ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON
6493                                   ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
6494                                   ;BE WRITTEN OR READ.
6495
6496   017112   004537   012234        JSR     R5,SELTER        ;SELECT REGISTER SPECIFIED BY NEXT WORD
6497   017116   000004                 .WORD   MODE             ;SELECT THE MODE REGISTER
6498
6499                                   ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
6500                                   ;ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
6501
6502   017120   005037   002346        CLR     T6LOAD           ;SETUP TO CLEAR ALL MODE REGISTER BITS
6503   017124   004737   011216        JSR     PC,LDRDT6        ;GO LOAD, READ AND CHECK MODE REGISTER
6504   017130   001405                 BEQ     3$               ;IF LOADED OK THEN CONTINUE
6505   017132                          ERRDF   12,MODREG,TO6ERR ;MODE REGISTER NOT EQUAL EXPECTED
6506   017132   104455                 TRAP    C$ERDF
6507   017134   000014                 .WORD   12
6508   017136   004002                 .WORD   MODREG
6509   017140   006732                 .WORD   TO6ERR
6510   017142                          CKLOOP
6511   017142   104406                 TRAP    C$CLP1
6512
6513                                   ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
6514                                   ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
6515                                   ;READ COMMAND TO CONTROL REGISTER 6..  THE EOAI REGISTER NEEDS FDAL0 H
6516                                   ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
6517                                   ;TER WILL BE ADDRESSED.
6518
6519   017144   004537   012234   3$:  JSR     R5,SELTER        ;SELECT REGISTER SPECIFIED BY NEXT WORD
6520   017150   000002                 .WORD   FDAL             ;SELECT EOAI AND FDAL REGISTER
6521
6522                                   ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER.  THE EOAI REGISTER WILL
6523                                   ;BE LOADED AND CHECKED FOR ZEROES.  THE FDAL REGISTER WILL BE LOADED AND
6524                                   ;CHECKED FOR A DATA PATTERN OF ONE (FDAL0 H = 1).
6525
6526   017152   012737   000001   002346   MOV   #FDAL0,T6LOAD  ;SETUP EOAI AND FDAL REG DATA PATTERN
6527   017160   004737   011216        JSR     PC,LDRDT6        ;GO LOAD, READ AND CHECK EOAI + FDAL REG
6528   017164   001405                 BEQ     4$               ;IF LOADED OK THEN CONTINUE
6529   017166                          ERRDF   12,EOAIFD,TO6ERR ;EOAI OR FDAL REGISTER ERROR
6530   017166   104455                 TRAP    C$ERDF
6531   017170   000014                 .WORD   12
6532   017172   004047                 .WORD   EOAIFD
6533   017174   006732                 .WORD   TO6ERR
6534   017176                          CKLOOP
```

B 11

HARDWARE TESTS MACY11 30A(1052)   16-JUN-82 13:46 PAGE 131
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0131

```
6535   017176  104406                           TRAP     C$CLP1
6536
6537                                   ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
6538                                   ;CHANGES OCCURED DOING THE PAST SEQUENCES.
6539
6540   017200  004737  011200    4$:   JSR      PC,READT4              ;READ AND CHECK VDAL REGISTER
6541   017204  001405                  BEQ      5$                     ;IF NO CHANGES THEN CONTINUE
6542   017206                          ERRDF    11,VDALRG,T4EROR       ;VDAL OR PAUSE STATE MACHINE ERROR
6543   017206  104455                  TRAP     C$ERDF
6544   017210  000013                  .WORD    11
6545   017212  003710                  .WORD    VDALRG
6546   017214  006716                  .WORD    T4EROR
6547   017216                          CKLOOP
6548   017216  104406                  TRAP     C$CLP1
6549
6550                                   ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6551                                   ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6552
6553   017220  004737  011250    5$:   JSR      PC,SLCTMS              ;SELECT MEMORY SIMULATOR MODULE
6554
6555                                   ;SET THE SIGNAL "MP H" TO A ONE AND PULSE THE SIGNAL "RST H".  THE
6556                                   ;SIGNAL "MP H" ON A ONE WILL ENABLE THE MAP PROTECTION RAM BITS
6557                                   ;TO THE SYSTEM BUS ALONG WITH THE SIGNAL MSBRK H.  PULSING THE SIGNAL
6558                                   ;"RST H" WILL PRESE1 THE RDV AND WRV FLIP-FLOP'S TO A ONE.  WHEN THE
6559                                   ;FLIP-FLOP'S ARE SET TO A ONE, THE SIGNAL "BRK L" WILL BE ASSERTED
6560                                   ;HIGH, THUS NO BREAK CONDITION IS GENERATED FROM THE MEMORY SIMULATOR.
6561
6562   017224  112737  000004  002234  MOVB     #MPH,SOLOAD            ;SET THE SIGNAL MP H TO HIGH STATE
6563   017232  004737  011270          JSR      PC,MSRSTH             ;SET RST H TO ONE AND PULSE RST H
6564
6565                                   ;LOAD MEMORY SIMULATOR RAM ADDRESS TO BE TESTED INTO CONTROL REGISTER 4.
6566                                   ;THE ADDRESSES TO BE TESTED ARE 000000, 020000, 040000 OR 060000.
6567
6568   017236  010137  002254          MOV      R1,S4LOAD             ;SETUP TO LOAD ADDRESS TO BE TESTED
6569   017242  004737  010606          JSR      PC,LDRDS4             ;LOAD READ AND CHECK CONTROL REG 4
6570   017246  001405                  BEQ      6$                    ;IF LOADED OK THEN CONTINUE
6571   017250                          ERRDF    3,MSADRG,S4EROR       ;MSAD 15:0 REGISTER ERROR
6572   017250  104455                  TRAP     C$ERDF
6573   017252  000003                  .WORD    3
6574   017254  002510                  .WORD    MSADRG
6575   017256  005336                  .WORD    S4EROR
6576   017260                          CKLOOP
6577   017260  104406                  TRAP     C$CLP1
6578
6579                                   ;CLEAR BITS MSEL1 H, MSEL0 H, MSAD17 H AND MSAD16 H IN CONTROL REGISTER
6580                                   ;2.  MSEL0 H AND MSEL1 H ON A ZERO WILL CAUSE THE SIGNAL "SSM L" TO BE
6581                                   ;ASSERTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.  ON A WRITE
6582                                   ;OR READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE WRITTEN INTO OR
6583                                   ;READ FROM MEMORY SIMULATOR RAM ADDRESSES BY CONTROL REGISTER 2 AND 4.
6584                                   ;THE MEMORY SIMULATOR RAM'S ARE ENABLED BY THE DATA PATTERNS PREVIOUSLY
6585                                   ;WRITTEN INTO MODULE SELECT RAMS 0 AND 1.  MSAD17 H AND MSAD16 H WILL BE
6586                                   ;LOADED AND CHECKED WITH ZEROES.  THE PROGRAM WILL EXPECT CONTROL REGIS-
6587                                   ;TER 2 BITS "ESR H" AND "WREN H" TO BE READ AS ONES AS A RESULT OF MAP
6588                                   ;PROTECTION RAM BITS "MPIN H" AND "WRE H" BEING SET TO ONES.
6589
6590   017262  005037  002244    6$:   CLR      S2LOAD                ;SET ALL BITS IN REG 2 TO ZEROES
```

C 11

HARDWARE TESTS MACV11 30A(1052) 16-JUN-82 13:46 PAGE 132
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0132

```
6591  017266  013737  002244 002246        MOV     S2LOAD,S2GOOD          ;COPY DATA LOADED TO EXPECTED
6592  017274  052737  000140 002246        BIS     #ESRH!WRENH,S2GOOD     ;EXPECT ESR H AND WREN H TO BE ONES
6593  017302  012737  177400 002250        MOV     #177400,S2MASK         ;SETUP TO COMPARE LOW BYTE
6594  017310  004737  010554               JSR     PC,LDRD2S              ;LOAD, READ AND CHECK CONTROL REG 2
6595  017314  001405                        BEQ     7$                     ;IF LOADED OK THEN CONTINUE
6596  017316                                ERRDF   2,,S2EROR              ;CONTROL REGISTER 2 NOT = EXPECTED
6597  017316  104455                        TRAP    C$ERDF
6598  017320  000002                        .WORD   2
6599  017322  000000                        .WORD   0
6600  017324  005322                        .WORD   S2EROR
6601  017326                                CKLOOP
6602  017326  104406                        TRAP    C$CLP1

6603
6604                                        ;LOAD DATA PATTERN INTO MEMORY SIMULATOR RAM ADDRESSED BY CONTROL
6605                                        ;REGISTER 2 AND 4.  ONE OF THE FOLLOWING DATA PATTERNS WILL BE LOADED
6606                                        ;INTO THE TEST ADDRESS LISTED BELOW:
6607                                        ;    ADDRESS 000000 WILL BE LOADED WITH 125252 AND 052525
6608                                        ;    ADDRESS 020000 WILL BE LOADED WITH 146314 AND 031463
6609                                        ;    ADDRESS 040000 WILL BE LOADED WITH 000377 AND 177400
6610                                        ;    ADDRESS 060000 WILL BE LOADED WITH 000000 AND 177777
6611
6612  017330  005037  002264        7$:    CLR     S6MASK                 ;SETUP TO COMPARE ALL BITS
6613  017334  011237  002260               MOV     (R2),S6LOAD            ;GET THE DATA PATTERN FROM THE TABLE
6614  017340  004737  010632               JSR     PC,LDRDS6              ;GO LOAD, READ AND CHECK RAM LOCATION
6615  017344  001405                        BEQ     8$                     ;IF LOADED OK THEN CONTINUE
6616  017346                                ERRDF   4,MSGMSR,S6ALLR        ;DATA ERROR IN MEMORY SIMULATOR RAM
6617  017346  104455                        TRAP    C$ERDF
6618  017350  000004                        .WORD   4
6619  017352  002745                        .WORD   MSGMSR
6620  017354  005456                        .WORD   S6ALLR
6621  017356                                CKLOOP
6622  017356  104406                        TRAP    C$CLP1

6623
6624                                        ;SET THE SIGNAL "CTS H" TO A ONE IN CONTROL REGISTER 0.  THIS WILL
6625                                        ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
6626                                        ;IN THIS TEST, "CTS H" ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
6627                                        ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
6628                                        ;SYSTEM BUS.
6629
6630  017360  052737  000002 002234  8$:   BIS     #CTSH,S0LOAD           ;SETUP BIT TO BE LOADED
6631  017366  004737  010506               JSR     PC,LDRDS0              ;GO LOAD, READ AND CHECK CONTROL REG 2
6632  017372  001405                        BEQ     9$                     ;IF LOADED OK THEN CONTINUE
6633  017374                                ERRDF   1,,S0EROR              ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
6634  017374  104455                        TRAP    C$ERDF
6635  017376  000001                        .WORD   1
6636  017400  000000                        .WORD   0
6637  017402  005306                        .WORD   S0EROR
6638  017404                                CKLOOP
6639  017404  104406                        TRAP    C$CLP1
6640
6641                                        ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6642                                        ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6643
6644  017406  004737  012214        9$:    JSR     PC,SLCTTE
6645
6646                                        ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
```

D 11

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 133
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0133

```
6647                                               ;2:0 TO A 0.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
6648                                               ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.  THE DIAGNOSTIC
6649                                               ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
6650                                               ;BIT 9 BEING SET TO A ONE PREVIOUSLY.  ON A READ COMMAND TO CONTROL
6651                                               ;REGISTER 6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
6652
6653    017412  004537  012234                     JSR     R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
6654    017416  000000                             .WORD   ADDRES                ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
6655
6656                                               ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
6657                                               ;FOLLOWING ADDRESSES: 000000, 020000, 040000, OR 060000.
6658
6659    017420  010137  002346                     MOV     R1,T6LOAD             ;GET THE TEST ADDRESS TO BE LOADED
6660    017424  004737  011216                     JSR     PC,LDRDT6             ;GO LOAD, READ + CHECK DIAG ADDRESS REG
6661    017430  001405                             BEQ     10$                   ;IF LOADED OK THEN CONTINUE
6662    017432                                     ERRDF   12,ADDRRG,T06ERR      ;DIAGNOSTIC ADDRESS REGISTER ERROR
6663    017432  104455                             TRAP    C$ERDF
6664    017434  000014                             .WORD   12
6665    017436  004144                             .WORD   ADDRRG
6666    017440  006732                             .WORD   T06ERR
6667    017442                                     CKLOOP
6668    017442  104406                             TRAP    C$CLP1
6669
6670                                               ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3.  THE
6671                                               ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
6672                                               ;CONTROL REGISTER 6.
6673
6674    017444  004537  012234          10$:       JSR     R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
6675    017450  000003                             .WORD   HDAL                  ;SELECT THE HDAL REGISTER
6676    017452  012737  001034  002346             MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD  ;GET BITS PREVIOUSLY LOADED
6677
6678                                               ;START A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE
6679                                               ;   1.   SET XRAS H AND PRAS H TO THE HIGH STATE
6680                                               ;   2.   SET XCAS H AND PCAS H TO THE HIGH STATE
6681                                               ;   3.   SET XPI L AND PPI L TO THE LOW STATE
6682                                               ;SETTING THE SIGNAL PRAS H TO THE HIGH STATE WILL CAUSE THE SIGNAL
6683                                               ;"ADVAL H" TO GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE SYSTEM
6684                                               ;ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR ADDRESS BUS LATCHES.
6685                                               ;WHEN   THE   SIGNALS   XRAS  H   AND   XCAS  H   ARE   ASSERTED
6686                                               ;HIGH, THE SIGNAL REAT H WILL GO FROM A LOW TO A HIGH STATE, THUS CAUSING
6687                                               ;THE SIGNAL READ H TO GO FROM A LOW TO A HIGH STATE.  THE TARGET EMULATORS
6688                                               ;SIGNAL READ H ALONG WITH THE MEMORY SIMULATOR'S SIGNALS CTS H AND ESR H
6689                                               ;WILL CAUSE THE MEMORY SIMULATOR RAM DATA TO BE PUT ONTO THE SYSTEM DATA
6690                                               ;BUS.  WHEN THE TARGET EMULATORS SIGNAL REAT H IS ASSERTED HIGH, THE
6691                                               ;TARGET EMULATORS SIGNAL MSDI H WILL BE ASSERTED HIGH, THUS ENABLING
6692                                               ;THE SYSTEM DATA BUS TO THE TARGET EMULATORS EODAL BUS.  THE MEMORY
6693                                               ;SIMULATOR RAM'S ARE ADDRESSED BY THE MEMORY SIMULATOR SYSTEM BUS ADDRESS
6694                                               ;LATCHES WHICH WERE CLOCKED BY THE SIGNAL ADVAL H.  THE DATA ON SYSTEM
6695                                               ;ADDRESS BUS COMES FROM THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER.
6696
6697    017460  004737  012300                     JSR     PC,XRASH              ;SET XRAS H AND PRAS H TO HIGH STATE
6698    017464  004737  012404                     JSR     PC,XCASH              ;SET XCAS H AND PCAS H TO HIGH STATE
6699    017470  004737  012510                     JSR     PC,XPIH               ;SET XPI H AND PPI H TO THE LOW STATE
6700
6701                                               ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H ARE
6702                                               ;ASSERTED HIGH (1'S).
```

E 11

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46 PAGE 134
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0134

```
6703
6704   017474   012737   000110   002342        MOV      #VDAL6!VDAL3,T4GOOD      ;EXPECT READ H AND MSDI H TO BE ONES
6705   017502   004737   011200                  JSR      PC,READT4               ;READ VDAL AND PAUSE STATE MACHINE REG
6706   017506   001405                            BEQ      11$                     ;IF DATA OK THEN CONTINUE
6707   017510                                     ERRDF    11,VDALRG,T4EROR        ;VDAL OR PAUSE STATE MACHINE ERROR
6708   017510   104455                            TRAP     C$ERDF
6709   017512   000013                            .WORD    11
6710   017514   003710                            .WORD    VDALRG
6711   017516   006716                            .WORD    T4EROR
6712   017520                                     CKLOOP
6713   017520   104406                            TRAP     C$CLP1
6714
6715                                              ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6716                                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6717
6718   017522   004737   011250        11$:       JSR      PC,SLCTMS               ;SELECT THE MEMORY SIMULATOR MODULE
6719
6720                                              ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
6721                                              ;TARGET EMULATOR MODULE SET THE SIGNALS ADVAL H AND READ H TO THE
6722                                              ;HIGH STATE FROM THE LOW STATE.
6723
6724   017526   004737   010522                  JSR      PC,READS0               ;READ AND CHECK CONTROL REGISTER 0
6725   017532   001405                            BEQ      12$                     ;IF NO CHANGES THEN CONTINUE
6726   017534                                     ERRDF    1,,S0EROR               ;CONTROL REGISTER 0 NOT = EXPECTED
6727   017534   104455                            TRAP     C$ERDF
6728   017536   000001                            .WORD    1
6729   017540   000000                            .WORD    0
6730   017542   005306                            .WORD    S0EROR
6731   017544                                     CKLOOP
6732   017544   104406                            TRAP     C$CLP1
6733
6734                                              ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
6735                                              ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
6736                                              ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.   THE SIGNAL ADVAL H
6737                                              ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
6738                                              ;SIGNAL PRAS H WAS SET HIGH FROM THE LOW STATE.   THE MEMORY SIMULATORS
6739                                              ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
6740                                              ;BITS VIA THE SIGNALS CTS H AND CTS L.
6741
6742   017546   010137   002254        12$:       MOV      R1,S4LOAD               ;GET THE EXPECTED ADDRESS LOADED
6743   017552   004737   010614                  JSR      PC,READS4               ;READ AND CHECK CONTROL REGISTER 4
6744   017556   001405                            BEQ      13$                     ;IF DATA = TE DIAG ADDRESS REG - CONT
6745   017560                                     ERRDF    3,TEMSAD,S04ERR         ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
6746   017560   104455                            TRAP     C$ERDF
6747   017562   000003                            .WORD    3
6748   017564   002534                            .WORD    TEMSAD
6749   017566   005406                            .WORD    S04ERR
6750   017570                                     CKLOOP
6751   017570   104406                            TRAP     C$CLP1
6752
6753                                              ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
6754                                              ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
6755                                              ;ZEROES FOR THESE TWO ADDRESSES.   ADDRESS BITS 17 AND 16 WERE CLOCKED
6756                                              ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
6757                                              ;ADVAL H.   THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
6758                                              ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE FROM
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6759                                          ;THE LOW STATE.  THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
6760                                          ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
6761                                          ;MEMORY SIMULATOR MODULE.
6762
6763    017572  052737  000014  002250  13$:  BIS     #MSEL0!MSEL1,S2MASK   ;IGNORE TRI-STATED BITS WHEN CTS H SET
6764    017600  005037  002244              CLR     S2LOAD               ;EXPECT MSAD 17:16 TO BE ZERO
6765    017604  013737  002244  002246        MOV     S2LOAD,S2GOOD        ;COPY DATA LOADED TO EXPECTED
6766    017612  052737  000140  002246        BIS     #ESRH!WRENH,S2GOOD   ;EXPECT MAP PROTECT BITS TO BE ONES
6767    017620  004737  010562                JSR     PC,READS2            ;READ AND CHECK CONTROL REGISTER 2
6768    017624  001405                        BEQ     14$                  ;IF DATA OK THEN CONTINUE
6769    017626                                ERRDF   2,TEMSA1,S02ERR      ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
6770    017626  104455                        TRAP    C$ERDF
6771    017630  000002                        .WORD   2
6772    017632  002410                        .WORD   TEMSA1
6773    017634  005366                        .WORD   S02ERR
6774    017636                                CKLOOP
6775    017636  104406                        TRAP    C$CLP1
6776
6777                                          ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6778                                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6779
6780    017640  004737  012214        14$:    JSR     PC,SLCTTE            ;SELECT THE TARGET EMULATOR MODULE
6781
6782                                          ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO A 7.  THE EODAL BUS
6783                                          ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
6784
6785    017644  004537  012234                JSR     R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
6786    017650  000007                        .WORD   EODAL                ;SELECT THE EODAL BUS TO BE READ
6787
6788                                          ;AT THIS TIME THE MEMORY SIMULATOR RAM DATA SHOULD BE ENABLED ON THE
6789                                          ;SYSTEM DATA BUS AND ENABLED TO THE TARGET EMULATORS EODAL BUS VIA THE
6790                                          ;TARGET EMULATOR SIGNALS READ H AND MSDI H RESPECTIVELY.  THE MEMORY
6791                                          ;SIMULATOR RAM IS ADDRESSED BY THE TARGET EMULATORS DIAGNOSTIC ADDRESS
6792                                          ;REGISTER WHICH WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS
6793                                          ;BUS LATCHES VIA THE SIGNAL ADVAL H.  THE DATA PATTERNS LOADED INTO
6794                                          ;THE TEST ADDRESSES OF THE MEMORY SIMULATOR RAM'S ARE LISTED BELOW:
6795                                          ;     ADDRESS 000000 WAS LOADED WITH 125252 AND 052525
6796                                          ;     ADDRESS 020000 WAS LOADED WITH 146314 AND 031463
6797                                          ;     ADDRESS 040000 WAS LOADED WITH 000377 AND 177400
6798                                          ;     ADDRESS 060000 WAS LOADED WITH 000000 AND 177777
6799
6800    017652  013737  002260  002346        MOV     S6LOAD,T6LOAD        ;GET DATA LOADED INTO MS RAM ADDRESSED
6801    017660  004737  011224                JSR     PC,READT6            ;READ SYSTEM DATA BUS ON THE EODAL BUS
6802    017664  001405                        BEQ     15$                  ;IF DATA = MS RAM DATA THEN CONTINUE
6803    017666                                ERRDF   12,MSTEDE,T6ALLR     ;MS RAM DATA TO TE EODAL BUS ERROR
6804    017666  104455                        TRAP    C$ERDF
6805    017670  000014                        .WORD   12
6806    017672  004243                        .WORD   MSTEDE
6807    017674  006746                        .WORD   T6ALLR
6808    017676                                CKLOOP
6809    017676  104406                        TRAP    C$CLP1
6810
6811                                          ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  THE EIDAL BUS
6812                                          ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
6813
6814    017700  004537  012234        15$:    JSR     R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
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G 11

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 136
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0136

```
6815    017704  060006                                  .WORD   EIDAL                   ;SELECT THE EIDAL BUS TO BE READ
6816
6817                                                    ;IN THE PREVIOUS DATA CHECK, THE PROGRAM VERIFIED THAT THE MEMORY SIMU-
6818                                                    ;LATOR RAM DATA WAS ENBALED TO THE EODAL BUS VIA THE SYSTEM DATA BUS.
6819                                                    ;IN THIS SECTION, THE PROGRAM WILL CHECK THAT THE EODAL BUS IS ENABLED
6820                                                    ;TO THE EIDAL BUS VIA THE CDAL BUS AS A RESULT OF THE SIGNALS COHB L AND
6821                                                    ;COLB L BEING ASSERTED LOW.   THE SIGNALS COHB L AND COLB L ARE ASSERTED
6822                                                    ;LOW AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED HIGH: ETR L,
6823                                                    ;PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L.   THE DATA READ SHOULD BE
6824                                                    ;THE SANE AS THAT WHICH WAS ENABLED TO THE EODAL BUS.   THE DATA PATTERNS
6825                                                    ;LOADED INTO THE TEST ADDRESS OF THE MEMORY SIMULATOR RAMS ARE AS FOLLOWS:
6826                                                    ;       ADDRESS 000000 WAS LOADED WITH 125252 AND 052525
6827                                                    ;       ADDRESS 020000 WAS LOADED WITH 146314 AND 031463
6828                                                    ;       ADDRESS 040000 WAS LOADED WITH 000377 AND 177400
6829                                                    ;       ADDRESS 060000 WAS LOADED WITH 000000 AND 177777
6830
6831    017706  013737  002260  002346          MOV     S6LOAD,T6LOAD           ;GET DATA LOADED INTO MS RAM ADDRESSED
6832    017714  004737  011224                  JSR     PC,READT6               ;READ SYSTEM DATA BUS ON EIDAL VIA EODAL
6833    017720  001405                           BEQ     16$                     ;IF DATA OK THEN CONTINUE
6834    017722                                  ERRDF   12,MSTEEI,T6ALLR        ;MS RAM DATA TO EIDAL BUS VIA EODAL BUS
6835    017722  104455                           TRAP    C$ERDF
6836    017724  000014                           .WORD   12
6837    017726  004331                           .WORD   MSTEEI
6838    017730  006746                           .WORD   T6ALLR
6839    017732                                  CKLOOP
6840    017732  104406                           TRAP    C$CLP1
6841
6842                                                    ;IN THE PREVIOUS DATA CHECKS, MEMORY SIMULATOR RAM DATA WAS ENABLED TO
6843                                                    ;THE SYSTEM DATA BUS WHICH ALSO WAS ENABLED TO THE EODAL, CDAL AND EIDAL
6844                                                    ;BUSES.   IN ADDITION TO THESE BUSES, MEMORY SIMULATOR RAM DATA WILL BE
6845                                                    ;ENABLED TO THE TDAL BUS VIA THE CDAL BUS BY THE SIGNALS DTHB L AND
6846                                                    ;DTLB H.   THE SIGNALS DTHB L AND DTLB L ARE ASSERTED LOW AS A RESULT OF
6847                                                    ;THE SIGNALS PSEL1 L, PSELO L, PBCLR L AND CPIW L BEING ASSERTED HIGH AND
6848                                                    ;THE T-11 SIGNAL CCAS H BEING ASSERTED LOW.   TO CAPTURE THE MEMORY
6849                                                    ;SIMULATOR RAM DATA ON THE TDAL BUS, THE PROGRAM WILL SET VDAL2 H TO A
6850                                                    ;ONE AND THEN A ZERO TO CLOCK THE TDAL BUS DATA INTO THE TDAL DIAGNOSTIC
6851                                                    ;LATCHES.
6852
6853    017734  052737  000004  002340  16$:     BIS     #VDAL2,T4LOAD           ;SET BIT TO CLOCK TDAL DIAG LATCHES
6854    017742  052737  000004  002342          BIS     #VDAL2,T4GOOD           ;EXPECT VDAL2 H TO BE SET ON READ
6855    017750  004737  011172                  JSR     PC,LDRD4T               ;LOAD, READ AND CHECK VDAL REGISTER
6856    017754  001405                           BEQ     17$                     ;IF LOADED OK THEN CONTINUE
6857    017756                                  ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
6858    017756  104455                           TRAP    C$ERDF
6859    017760  000013                           .WORD   11
6860    017762  003710                           .WORD   VDALRG
6861    017764  006716                           .WORD   T4EROR
6862    017766                                  CKLOOP
6863    017766  104406                           TRAP    C$CLP1
6864    017770  042737  000004  002340  17$:     BIC     #VDAL2,T4LOAD           ;SET CLOCK SIGNAL TO A ZERO
6865    017776  042737  000004  002342          BIC     #VDAL2,T4GOOD           ;EXPECT VDAL2 H TO BE 0 ON A READ
6866    020004  004737  011172                  JSR     PC,LDRD4T               ;LOAD, READ AND CHECK VDAL REGISTER
6867    020010  001405                           BEQ     18$                     ;IF LOADED OK THEN CONTINUE
6868    020012                                  ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
6869    020012  104455                           TRAP    C$ERDF
6870    020014  000013                           .WORD   11
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6871   020016   003710                              .WORD    VDALRG
6872   020020   006716                              .WORD    T4EROR
6873   020022                                       CKLOOP
6874   020022   104406                              TRAP     C$CLP1
6875
6876                                        ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.   THE HDAL
6877                                        ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
6878                                        ;REGISTER 6.
6879
6880   020024   004537   012234     18$:    JSR      R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
6881   020030   000003                              .WORD    HDAL                   ;SELECT THE HDAL REGISTER
6882
6883                                        ;FINISH THE T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
6884                                        ;  1. SET XCAS H AND PCAS H TO THE LOW STATE
6885                                        ;  2. SET XPI L AND PPI L TO THE HIGH STATE
6886                                        ;  3. SET XRAS H AND PRAS H TO THE LOW STATE
6887
6888   020032   012737   001034   002346    MOV      #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SETUP PREVIOULSY LOADED BITS
6889   020040   004737   012436             JSR      PC,XCASL               ;SET XCAS H AND PCAS H TO LOW STATE
6890   020044   004737   012542             JSR      PC,XPIL                ;SET XPI L AND PPI L TO THE HIGH STATE
6891   020050   004737   012332             JSR      PC,XRASL               ;SET XRAS H AND PRAS H TO LOW STATE
6892
6893                                        ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H
6894                                        ;WENT TO A ZERO AS A RESULT OF SETTING THE SIGNALS XCAS H AND XRAS H
6895                                        ;TO THE LOW STATE.
6896
6897   020054   005037   002342             CLR      T4GOOD                 ;EXPECT VDAL REGISTER TO BE A 0
6898   020060   004737   011200             JSR      PC,READT4              ;READ AND CHECK VDAL REGISTER
6899   020064   001405                       BEQ      19$                    ;IF OK THEN CONTINUE
6900   020066                                ERRDF    11,VDALRG,T4EROR       ;VDAL OR PAUSE STATE MACHINE ERROR
6901   020066   104455                       TRAP     C$ERDF
6902   020070   000013                       .WORD    11
6903   020072   003710                       .WORD    VDALRG
6904   020074   006716                       .WORD    T4EROR
6905   020076                                CKLOOP
6906   020076   104406                       TRAP     C$CLP1
6907
6908                                        ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6909                                        ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6910
6911   020100   004737   011250     19$:    JSR      PC,SLCTMS              ;SELECT THE MEMORY SIMULATOR MODULE
6912
6913                                        ;SET THE SIGNAL CTS H TO THE LOW STATE BY CLEARING THE BIT IN CONTROL
6914                                        ;REGISTER 0.   THIS WILL DISABLE THE SYSTEM BUS SIGNALS TO AND FROM
6915                                        ;THE MEMORY SIMULATOR MODULE.
6916
6917   020104   112737   000004   002234    MOVB     #MPH,SOLOAD            ;CLEAR CTS H AND LEAVE MP H SET TO A 1
6918   020112   004737   010506             JSR      PC,LDRDS0              ;LOAD, READ AND CHECK CONTROL REG 0
6919   020116   001405                       BEQ      20$                    ;IF LOADED OK THEN CONTINUE
6920   020120                                ERRDF    1,,SOEROR              ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
6921   020120   104455                       TRAP     C$ERDF
6922   020122   000001                       .WORD    1
6923   020124   000000                       .WORD    0
6924   020126   005306                       .WORD    SOEROR
6925   020130                                CKLOOP
6926   020130   104406                       TRAP     C$CLP1
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6927
6928                                              ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
6929                                              ;LOADED PREVIOUSLY IS STILL LOADED
6930
6931   020132  004737  010614           20$:     JSR     PC,READS4              ;READ AND CHECK CONTROL REGISTER 4
6932   020136  001405                            BEQ     21$                   ;IF ADDRESS 0 THEN CONTINUE
6933   020140                                     ERRDF   3,MSADRG,S4EROR       ;MSAD 15:0 REGISTER ERROR
6934   020140  104455                            TRAP    C$ERDF
6935   020142  000003                            .WORD   3
6936   020144  002510                            .WORD   MSADRG
6937   020146  005336                            .WORD   S4EROR
6938   020150                                     CKLOOP
6939   020150  104406                            TRAP    C$CLP1
6940
6941                                              ;READ CONTROL REGISTER 0 TO CHECK THAT THE DATA LOADED INTO IT PREVIOUSLY
6942                                              ;HAS NOT CHANGED.  THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
6943                                              ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBRK H.  THE SIGNALS ESR H
6944                                              ;AND WREN H SHOULD BE READ AS ONES.
6945
6946   020152  012737  177400  002250  21$:     MOV     #177400,S2MASK        ;SETUP TO CHECK ALL OFF LOW BYTE
6947   020160  004737  010562                    JSR     PC,READS2             ;READ AND CHECK CONTROL REGISTER 2
6948   020164  001405                            BEQ     22$                   ;IF NO CHANGE THEN CONTINUE
6949   020166                                     ERRDF   2,,S2EROR             ;CONTROL REG 2 NOT EQUAL EXPECTED
6950   020166  104455                            TRAP    C$ERDF
6951   020170  000002                            .WORD   2
6952   020172  000000                            .WORD   0
6953   020174  005322                            .WORD   S2EROR
6954   020176                                     CKLOOP
6955   020176  104406                            TRAP    C$CLP1
6956
6957                                              ;WRITE INTO THE MEMORY SIMULATOR RAM'S TEST ADDRESS THE ONES COMPLEMENT
6958                                              ;OF THE DATA WHICH WAS PREVIOUSLY WRITTEN INTO IT.
6959
6960   020200  005137  002260           22$:     COM     S6LOAD                ;MAKE THE 1'S COMPLEMENT OF PREVIOUS DATA
6961   020204  004737  010632                    JSR     PC,LDRDS6             ;GO LOAD, READ AND CHECK MEM SIM RAM LOC
6962   020210  001405                            BEQ     23$                   ;IF LOADED OK THEN CONTINUE
6963   020212                                     ERRDF   4,MSGMSR,S6ALLR       ;DATA ERROR IN MEMORY SIMULATOR RAM
6964   020212  104455                            TRAP    C$ERDF
6965   020214  000004                            .WORD   4
6966   020216  002745                            .WORD   MSGMSR
6967   020220  005456                            .WORD   S6ALLR
6968   020222                                     CKLOOP
6969   020222  104406                            TRAP    C$CLP1
6970
6971                                              ;SET THE SIGNAL CTS H TO A ONE IN CONTROL REGISTER 0.  THIS WILL ENABLE
6972                                              ;THE SYTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR MODULE.
6973
6974   020224  052737  000002  002234  23$:     BIS     #CTSH,S0LOAD          ;SETUP BIT TO BE LOADED
6975   020232  004737  010506                    JSR     PC,LDRDS0             ;LOAD, READ AND CHECK REGISTER 0
6976   020236  001405                            BEQ     24$                   ;IF LOADED OK THEN CONTINUE
6977   020240                                     ERRDF   1,,S0EROR             ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
6978   020240  104455                            TRAP    C$ERDF
6979   020242  000001                            .WORD   1
6980   020244  000000                            .WORD   0
6981   020246  005306                            .WORD   S0EROR
6982   020250                                     CKLOOP
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J 11

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 139
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0139

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6983  020250  104406                              TRAP    C$CLP1
6984
6985                                              ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
6986                                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
6987
6988  020252  004737  012214         24$:        JSR     PC,SLCTTE               ;SELECT THE TARGET EMULATOR MODULE.
6989
6990                                              ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 2.  THE
6991                                              ;EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR READ COMMAND TO
6992                                              ;CONTROL REGISTER 6.
6993
6994  020256  004537  012234                     JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
6995  020262  000002                             .WORD   FDAL                   ;SELECT EOAI AND FDAL REGISTER
6996
6997                                              ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER.  THE EOAI REGISTER WILL BE
6998                                              ;LOADED AND CHECKED FOR A DATA PATTERN OF ALL ZEROES.  THE FDAL REGISTER
6999                                              ;WILL BE LOADED AND CHECKED FOR A DATA PATTERN OF 3 (FDAL1 H AND FDAL0 H).
7000                                              ;FDAL0 H ON A ONE WILL SELECT THE EOAI REGISTER TO BE READ ON A READ COMMAND
7001                                              ;TO CONTROL REGISTER 6 INCTEAD OF THE CTL REGISTER.  FDAL1 H ON A ONE WILL
7002                                              ;ENABLE THE SIGNALS WR HB H AND WR LB H TO THE SYSTEM BUS WHEN THE SIGNAL
7003                                              ;DMG L IS ASSERTED LOW LATER ON IN THIS TEST.
7004
7005  020264  012737  000003  002346             MOV     #FDAL1!FDAL0,T6LOAD    ;SETUP BITS TO BE LOADED
7006  020272  004737  011216                     JSR     PC,LDRDT6              ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER
7007  020276  001405                             BEQ     25$                    ;IF LOADED OK THEN CONTINUE
7008  020300                                     ERRDF   12,EOAIFD,T06ERR       ;EOAI 7:0 OR FDAL 7:0 REGISTER ERROR
7009  020300  104455                             TRAP    C$ERDF
7010  020302  000014                             .WORD   12
7011  020304  004047                             .WORD   EOAIFD
7012  020306  006732                             .WORD   T06ERR
7013  020310                                     CKLOOP
7014  020310  104406                             TRAP    C$CLP1
7015
7016                                              ;SLECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL REGISTER
7017                                              ;WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
7018
7019  020312  004537  012234         25$:        JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
7020  020316  000003                             .WORD   HDAL                   ;SELECT THE HDAL REGISTER
7021
7022                                              ;SET THE SIGNALS PSEL0 L AND PSEL1 L TO THE LOW STATE BY SETTING HDAL
7023                                              ;REGISTER BITS 5 AND 6 TO ONES.  SETTING THESE SIGNALS LOW WILL CAUSE
7024                                              ;THE SIGNALS DBHB L AND DBLB L TO BE ASSERTED LOW THUS ENABLING THE
7025                                              ;TDAL BUS TO THE CDAL BUS AND EIDAL BUS.  SETTING PSEL0 L AND PSEL1 L
7026                                              ;WILL ALSO CAUSE THE SIGNAL DMG L TO BE ASSERTED LOW.  SET THE SIGNALS
7027                                              ;XR/WHB L AND XR/WLB L TO THE HIGH STATE BY SETTING HDAL REGISTER BITS
7028                                              ;4 AND 3 TO A ZERO.  THIS WILL SET THE READ/WRITE CONTROL LOGIC TO DO
7029                                              ;A WRITE WHEN THE SIGNAL XPI H IS SET HIGH.  HDAL9 H WILL BE SET TO A
7030                                              ;ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS
7031                                              ;BUS.  THE DIAGNOSTIC ADDRESS REGISTER WAS LOADED WITH ADDRESS 0 EARLIER
7032                                              ;IN THIS TEST.  HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM
7033                                              ;TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
7034
7035  020320  012737  001144  002346             MOV     #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD  ;SETUP BITS TO BE LOADED
7036  020326  004737  011216                     JSR     PC,LDRDT6              ;LOAD, READ AND CHECK HDAL REGISTER
7037  020332  001405                             BEQ     26$                    ;IF LOADED OK THEN CONTINUE
7038  020334                                     ERRDF   12,HDALRG,T06ERR       ;HDAL REGISTER NOT EQUAL EXPECTED
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7039   020334   104455                            TRAP    C$ERDF
7040   020336   000014                            .WORD   12
7041   020340   003756                            .WORD   HDALRG
7042   020342   006732                            .WORD   TO6ERR
7043   020344                                     CKLOOP
7044   020344   104406                            TRAP    C$CLP1
7045
7046                                          ;SET VDAL0 H TO A ONE TO ENABLE THE OUTPUTS OF THE TDAL DIAGNOSTIC
7047                                          ;LATCHES ONTO THE TDAL BUS.  THE TDAL BUS WILL BE ENABLED TO THE CDAL
7048                                          ;BUS VIA DBHB L AND DBLB L.  THE CDAL BUS WILL BE ENABLED TO THE EIDAL
7049                                          ;BUS UNCONDITIONALY.
7050
7051   020346   012737  000001  002340  26$:  MOV     #VDAL0,T4LOAD              ;SETUP BIT TO BE LOADED
7052   020354   004737  011164              JSR     PC,LDRDT4                 ;LOAD, READ AND CHECK VDAL REGISTER
7053   020360   001405                      BEQ     27$                       ;IF LOADED OK THEN CONTINUE
7054   020362                               ERRDF   11,VDALRG,T4EROR          ;VDAL REGISTER NOT EQUAL EXPECTED
7055   020362   104455                      TRAP    C$ERDF
7056   020364   000013                      .WORD   11
7057   020366   003710                      .WORD   VDALRG
7058   020370   006716                      .WORD   T4EROR
7059   020372                               CKLOOP
7060   020372   104406                      TRAP    C$CLP1
7061
7062                                          ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ
7063                                          ;COMMAND TO CONTROL REGISTER 6 THE EIDAL BUS WILL BE READ.
7064
7065   020374   004537  012234         27$:  JSR     R5,SELTER                 ;SELECT REGISTER SPECIFIED BY NEXT WORD
7066   020400   000006                      .WORD   EIDAL                     ;SELECT THE EIDAL BUS TO BE READ
7067
7068                                          ;AT THIS POINT IN TIME THE EIDAL BUS SHOULD HAVE THE TDAL DIAGNOSTIC
7069                                          ;LATCHES ENABLED TO IT BY THE SIGNALS DBHB L AND DBLB L BEING ASSERTED
7070                                          ;LOW AND VDAL0 H BEING SET TO A ONE.  THE TDAL LATCHES WERE CLOCKED
7071                                          ;EARLIER IN THE TEST BY THE SIGNAL VDAL2 H.  THESE LATCHES WERE
7072                                          ;CLOCKED WITH THE DATA FROM THE MEMORY SIMULATOR RAM DURING A READ
7073                                          ;OPERATION OF THE MEMORY SIMULATOR RAM TEST ADDRESS.
7074
7075   020402   011237  002346              MOV     (R2),T6LOAD               ;GET 1ST DATA WRITTEN TO MS RAM
7076   020406   004737  011224              JSR     PC,READ*6                 ;READ AND CHECK EIDAL BUS
7077   020412   001405                      BEQ     28$                       ;IF DATA OK THEN CONTINUE
7078   020414                               ERRDF   12,MSTETD,T6ALLR          ;MS RAM DATA TO EIDAL BUS VIA TDAL BUS
7079   020414   104455                      TRAP    C$ERDF
7080   020416   000014                      .WORD   12
7081   020420   004422                      .WORD   MSTETD
7082   020422   006746                      .WORD   T6ALLR
7083   020424                               CKLOOP
7084   020424   104406                      TRAP    C$CLP1
7085
7086                                          ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
7087                                          ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
7088                                          ;REGISTER 6.
7089
7090   020426   004537  012234         28$:  JSR     R5,SELTER                 ;SELECT REGISTER SPECIFIED BY NEXT WORD
7091   020432   000003                      .WORD   HDAL                      ;SELECT THE HDAL REGISTER
7092   020434   012737  001144  002346      MOV     #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
7093
7094                                          ;AT THE PRESENT TIME, MEMORY SIMULATOR DATA WHICH WAS READ FROM THE TEST
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L 11

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 141
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0141

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7095                                                  ;ADDRESS OF THE MEMORY SIMULATOR RAM EARLIER IN THIS TEST, IS NOW ENABLED
7096                                                  ;TO THE SYSTEM DATA BUS VIA THE TDAL DIAGNOSTIC LATCHES.  THIS DATA WAS
7097                                                  ;PRESENT ON THE EIDAL BUS IN THE LAST DATA CHECK ABOVE.  THE EIDAL BUS
7098                                                  ;IS ENABLED TO THE SYSTEM DATA BUS BY THE SIGNAL MSDO H BEING ASSERTED
7099                                                  ;HIGH.  THE PROGRAM WILL NOW WRITE THE DATA ON THE SYSTEM DATA BUS BACK
7100                                                  ;INTO ADDRESS ZERO ON THE MEMORY SIUMULATOR RAM BY DOING A NORMAL T-11
7101                                                  ;TIMING CYCLE.  WHEN PRAS H IS SET HIGH, THE ADDRESS BUS WHICH CONTAINS
7102                                                  ;THE DIAGNOSTIC ADDRESS REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY
7103                                                  ;SIMULATOR SYSTEM ADDRESS BUS LATCHES.  WHEN XPI H IS SET HIGH IN THE
7104                                                  ;FOLLOWING TIMING SEQUENCE, THE DATA WILL BE WRITTEN INTO ADDRESS ZERO
7105                                                  ;OF THE MEMORY SIMULATOR RAM.   THE WRITE SIGNALS FROM THE TARGET
7106                                                  ;EMULATOR MODULE TO THE MEMORY SIMULATOR MODULE ARE WT HB H AND WT LB H.
7107
7108   020442  004737  012300          JSR    PC,XRASH          ;SET XRAS H AND PRAS H TO HIGH STATE
7109   020446  004737  012404          JSR    PC,XCASH          ;SET XCAS H AND PCAS H TO HIGH STATE
7110   020452  004737  012510          JSR    PC,XPIH           ;SET XPI H AND PPI H TO HIGH STATE
7111   020456  004737  012436          JSR    PC,XCASL          ;SET XCAS H AND PCAS H TO LOW STATE
7112   020462  004737  012542          JSR    PC,XPIL           ;SET XPI H AND PPIH TO LOW STATE
7113   020466  004737  012332          JSR    PC,XRASL          ;SET XRAS H AND PRAS H TO LOW STATE
7114
7115                                                  ;READ VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A ONE
7116                                                  ;IN THE VDAL REGISTER AS A RESULT OF THE ABOVE T-11 TIMING SEQUENCE.
7117
7118   020472  052737  000020  002342  BIS    #VDAL4,T4GOOD     ;EXPECT EDEOC H TO BE SET TO A ONE
7119   020500  004737  011200          JSR    PC,READT4         ;READ AND CHECK VDAL REGISTER
7120   020504  001405                  BEQ    29$               ;IF OK THEN CONTINUE
7121   020506                          ERRDF  11,VDALRG,T4EROR  ;VDAL REGISTER NOT EQUAL EXPECTED
7122   020506  104455                  TRAP   C$ERDF
7123   020510  000013                  .WORD  11
7124   020512  003710                  .WORD  VDALRG
7125   020514  006716                  .WORD  T4EROR
7126   020516                          CKLOOP
7127   020516  104406                  TRAP   C$CLP1
7128
7129                                                  ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE ON CONTROL
7130                                                  ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7131
7132   020520  004737  011250     29$: JSR    PC,SLCTMS         ;SELECT THE MEMORY SIMULATOR MODULE
7133
7134                                                  ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
7135                                                  ;TARGET EMULATOR MODULE PULSED THE SIGNAL ADVAL H BY TOGGLING THE
7136                                                  ;SIGNAL PRAS H.
7137
7138   020524  00473"  010522          JSR    PC,READS0         ;READ AND CHECK CONTROL REGISTER 0
7139   020530  001405                  BEQ    30$               ;IF NO CHANGES THEN CONTINUE
7140   020532                          ERRDF  1,,SOEROR         ;CONTROL REGISTER 0 NOT = EXPECTED
7141   020532  104455                  TRAP   C$ERDF
7142   020534  000001                  .WORD  1
7143   020536  000000                  .WORD  0
7144   020540  005306                  .WORD  SOEROR
7145   020542                          CKLOOP
7146   020542  104406                  TRAP   C$CLP1
7147
7148                                                  ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
7149                                                  ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
7150                                                  ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.  THE SIGNAL ADVAL H
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M 11

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 142
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0142

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7151                                         ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
7152                                         ;SIGNAL PRAS H WAS SET TO A ONE AND THEN A ZERO.  THE MEMORY SIMULATORS
7153                                         ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
7154                                         ;BITS VIA THE SIGNALS CTS H AND CTS L.
7155
7156  020544  010137  002254    30$:  MOV    R1,S4LOAD              ;SETUP THE EXPECTED ADDRESS TO BE READ
7157  020550  004737  010614          JSR    PC,READS4             ;READ AND CHECK CONTROL REGISTER 4
7158  020554  001405                  BEQ    31$                    ;IF DATA = TE DIAG ADDRESS REG - CONT
7159  020556                          ERRDF  3,TEMSAD,S04ERR        ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
7160  020556  104455                  TRAP   C$ERDF
7161  020560  000003                  .WORD  3
7162  020562  002534                  .WORD  TEMSAD
7163  020564  005406                  .WORD  S04ERR
7164  020566                          CKLOOP
7165  020566  104406                  TRAP   C$CLP1
7166
7167                                         ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
7168                                         ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
7169                                         ;ZEROES FOR THESE TWO ADDRESSES.  ADDRESS BITS 17 AND 16 WERE CLOCKED
7170                                         ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
7171                                         ;ADVAL H.  THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
7172                                         ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE AND THEN TO
7173                                         ;THE LOW STATE.  THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
7174                                         ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
7175                                         ;MEMORY SIMULATOR MODULE.
7176
7177  020570  052737  000014  002250  31$:  BIS    #MSEL0!MSEL1,S2MASK   ;IGNORE TRI-STATED BITS WHEN CTS H SET
7178  020576  005037  002244          CLR    S2LOAD                ;EXPECT MSAD 17:16 TO BE ZERO
7179  020602  013737  002244  002246  MOV    S2LOAD,S2GOOD         ;COPY DATA LOADED TO EXPECTED
7180  020610  052737  000140  002246  BIS    #ESRH!WRENH,S2GOOD    ;EXPECT MAP PROTECT BITS TO BE ONES
7181  020616  004737  010562          JSR    PC,READS2             ;READ AND CHECK CONTROL REGISTER 2
7182  020622  001405                  BEQ    32$                    ;IF DATA OK THEN CONTINUE
7183  020624                          ERRDF  2,TEMSA1,S02ERR        ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
7184  020624  104455                  TRAP   C$ERDF
7185  020626  000002                  .WORD  2
7186  020630  002410                  .WORD  TEMSA1
7187  020632  005366                  .WORD  S02ERR
7188  020634                          CKLOOP
7189  020634  104406                  TRAP   C$CLP1
7190
7191                                         ;SET THE SIGNAL CTS H TO THE LOW STATE BY CLEARING THE BIT IN CONTROL
7192                                         ;REGISTER 0.  THIS WILL DISABLE THE SYSTEM BUS SIGNALS TO AND FROM
7193                                         ;THE MEMORY SIMULATOR MODULE.
7194
7195  020636  112737  000004  002234  32$:  MOVB   #MPH,S0LOAD           ;CLEAR CTS H AND LEAVE MP H SET TO A 1
7196  020644  004737  010506          JSR    PC,LDRDS0             ;LOAD, READ AND CHECK CONTROL REG 0
7197  020650  001405                  BEQ    33$                    ;IF LOADED OK THEN CONTINUE
7198  020652                          ERRDF  1,,S0EROR              ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
7199  020652  104455                  TRAP   C$ERDF
7200  020654  000001                  .WORD  1
7201  020656  000000                  .WORD  0
7202  020660  005306                  .WORD  S0EROR
7203  020662                          CKLOOP
7204  020662  104406                  TRAP   C$CLP1
7205
7206                                         ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
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7207                                              ;LOADED PREVIOUSLY IS STILL LOADED
7208
7209   020664  004737  010614      33$:  JSR     PC,READS4          ;READ AND CHECK CONTROL REGISTER 4
7210   020670  001405                    BEQ     34$                ;IF ADDRESS 0 THEN CONTINUE
7211   020672                            ERRDF   3,MSADRG,S4EROR    ;MSAD 15:0 REG ERROR
7212   020672  104455                    TRAP    C$ERDF
7213   020674  000003                    .WORD   3
7214   020676  002510                    .WORD   MSADRG
7215   020700  005336                    .WORD   S4EROR
7216   020702                            CKLOOP
7217   020702  104406                    TRAP    C$CLP1
7218
7219                                              ;READ CONTROL REGISTER 2 TO CHECK THAT THE DATA LOADED INTO IT PREVIOUSLY
7220                                              ;HAS NOT CHANGED.  THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
7221                                              ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBRK H.  THE SIGNALS ESR H
7222                                              ;AND WREN H SHOULD BE READ AS ONES.
7223
7224   020704  012737  177400  002250  34$:  MOV  #177400,S2MASK    ;SETUP TO CHECK ALL OFF LOW BYTE
7225   020712  004737  010562            JSR     PC,READS2          ;READ AND CHECK CONTROL REGISTER 2
7226   020716  001405                    BEQ     35$                ;IF NO CHANGE THEN CONTINUE
7227   020720                            ERRDF   2,,S2EROR          ;CONTROL REG 2 NOT EQUAL EXPECTED
7228   020720  104455                    TRAP    C$ERDF
7229   020722  000002                    .WORD   2
7230   020724  000000                    .WORD   0
7231   020726  005322                    .WORD   S2EROR
7232   020730                            CKLOOP
7233   020730  104406                    TRAP    C$CLP1
7234
7235                                              ;READ CONTENTS OF THE MEMORY SIMULATOR RAM ADDRESS TO CHECK THAT THE DATA
7236                                              ;INITIALLY LOADED INTO IT WAS WRITTEN BACK INTO IT FROM THE TARGET
7237                                              ;EMULATOR MODULE DURING A WRITE OPERATION. IN THE FIRST PART OF THIS
7238                                              ;TEST THE DATA WAS READ FROM THE MEMORY SIMULAOTR RAM INTO THE TARGET
7239                                              ;EMULATOR AND SAVED IN THE TARGET EMULATORS TDAL DIAGNOSTIC LATCHES.
7240                                              ;THE PROGRAM THEN COMPLEMENTED THE DATA PATTERN WRITTEN INTO THE ADDRESS
7241                                              ;OF THE MEMORY SIMULATOR RAM.  THE PROGRAM THEN ENABLED THE TDAL DIAG-
7242                                              ;NOSTIC LATCHES TO THE TDAL BUS AND WROTE THE DATA BACK INTO THE ADDRESS
7243                                              ;OF THE MEMORY SIMULATOR RAM.  THE FOLLOWING CHECK WILL TEST THAT THIS
7244                                              ;HAPPENED CORRECTLY.
7245
7246   020732  011237  002260      35$:  MOV     (R2),S6LOAD        ;GET INITIAL MS RAM DATA LOADED
7247   020736  013737  002260  002262      MOV   S6LOAD,S6GOOD      ;COPY DATA FOR COMPARE IN SUBROUTINE
7248   020744  004737  010646            JSR     PC,READS6          ;READ AND CHECK MS LOC 0 RAM DATA
7249   020750  001404                    BEQ     36$                ;IF DATA OK THEN CONTINUE
7250   020752                            ERRDF   4,MSGMSR,S6ALLR    ;DATA ERROR IN MEMORY SIMULATOR RAM
7251   020752  104455                    TRAP    C$ERDF
7252   020754  000004                    .WORD   4
7253   020756  002745                    .WORD   MSGMSR
7254   020760  005456                    .WORD   S6ALLR
7255   020762                      36$:  ENDSEG
7256   020762                    10000$:
7257   020762  104405                    TRAP    C$ESEG
7258
7259   020764  005722                    TST     (R2)+              ;UPDATE THE DATA TABLE POINTER
7260   020766  005303                    DEC     R3                 ;CHECK IF ADDRESS DONE TWICE
7261   020770  001402                    BEQ     37$                ;IF YES THEN UPDATE TEST ADDRESS
7262   020772  000137  017026            JMP     1$                 ;DO SAME ADDRESS WITH NEW PATTERN
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B 12

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 144
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0144

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7263  020776  012703  000002     37$:   MOV    #2,R3              ;UPDATE TO DO NEXT ADDRESS TWICE
7264  021002  062701  020000            ADD    #MSAD13,R1         ;UPDATE ADDRESS TO NEXT MS RAM BANK
7265  021006  100402                    BMI    38$               ;IF DONE EACH BANK OF MEMORY - EXIT
7266  021010  000137  017026            JMP    1$                ;GO DO TWO PATTERNS WITH THIS ADDRESS
7267
7268                                     ;TO CHECK THAT ADDRESS 0 OF EACH 4K BANK OF MEMORY SIMULATOR RAM WAS
7269                                     ;SELECTED AND WRITTEN CORRECTLY, THE PROGRAM WILL READ THE FIRST ADDRESS
7270                                     ;OF EACH 4K BANK OF MEMORY SIMULATOR RAM AND CHECK THE DATA TO BE EQUAL
7271                                     ;TO WHAT WAS WRITTEN INTO IT PREVIOUSLY.  THE ADDRESSES AND THE DATA
7272                                     ;PATTERNS EXPECTED ARE AS FOLLOWS:
7273                                     ;     ADDRESS 000000 WAS WRITTEN WITH 052525
7274                                     ;     ADDRESS 020000 WAS WRITTEN WITH 031463
7275                                     ;     ADDRESS 040000 WAS WRITTEN WITH 177400
7276                                     ;     ADDRESS 060000 WAS WRITTEN WITH 177777
7277
7278  021014  005001             38$:   CLR    R1                ;SETUP STARTING ADDRESSS TO  BE 0
7279  021016  012702  021112            MOV    #50$+2,R2         ;SETUP ADDRESS OF DATA TABLE
7280
7281                                     ;LOAD, READ AND CHECK CONTROL REGISTER 4 WITH THE ADDRESS OF THE LOCATION
7282                                     ;TO BE CHECKED.   THE ADDRESSES TO BE LOADED ARE 0, 20000, 40000, AND 60000.
7283
7284  021022  010137  002254     39$:   MOV    R1,S4LOAD         ;GET THE ADDRESS TO BE LOADED
7285  021026  004737  010606            JSR    PC,LDRDS4         ;LOAD, READ AND CHECK CONTROL REGISTER 4
7286  021032  001405                    BEQ    40$               ;IF LOADED OK THEN CONTINUE
7287  021034                            ERRDF  3,MSADRG,S4EROR   ;MSAD 15:0 REGISTER ERROR
7288  021034  104455                    TRAP   C$ERDF
7289  021036  000003                    .WORD  3
7290  021040  002510                    .WORD  MSADRG
7291  021042  005336                    .WORD  S4EROR
7292  021044                            CKLOOP
7293  021044  104406                    TRAP   C$CLP1
7294
7295                                     ;EARLIER IN THIS TEST, CONTROL REGISTER 2 BITS MSAD16 H, MSAD17 H, MSEL1 L,
7296                                     ;AND MSEL0 L WERE WRITTEN TO ZEROES.  WHEN A READ COMMAND IS ISSUED TO
7297                                     ;CONTROL REGISTER 6 AND THE SIGNALS MSEL1 L AND MSEL0 L ARE ASSERTED LOW,
7298                                     ;A PULSE WILL BE ISSUED ON THE SIGNAL SSM L.  THIS SIGNAL ALONG WITH THE
7299                                     ;READ COMMAND, WILL READ THE DATA FROM THE MEMORY SIMULATOR RAM ADDRESSED
7300                                     ;BY CONTROL REGISTER 2 AND 4 BITS.
7301
7302  021046  011237  002260     40$:   MOV    (R2),S6LOAD       ;GET THE DATA FROM THE TABLE
7303  021052  012237  002262            MOV    (R2)+,S6GOOD      ;COPY DATA FOR DATA COMPARE
7304  021056  005722                    TST    (R2)+             ;UPDATE POINTER TO NEXT EXPECTED DATA
7305  021060  004737  010646            JSR    PC,READS6         ;READ AND CHECK MEMORY SIM RAM DATA
7306  021064  001405                    BEQ    41$               ;IF DATA OK THEN CONTINUE
7307  021066                            ERRDF  4,MSGMSR,S6ALLR   ;DATA ERROR IN MEMORY SIMULATOR RAM
7308  021066  104455                    TRAP   C$ERDF
7309  021070  000004                    .WORD  4
7310  021072  002745                    .WORD  MSGMSR
7311  021074  005456                    .WORD  S6ALLR
7312  021076                            CKLOOP
7313  021076  104406                    TRAP   C$CLP1
7314
7315  021100  062701  020000     41$:   ADD    #MSAD13,R1        ;UPDATE THE ADDRESS TO NEXT 4K MEMORY
7316  021104  100346                    BPL    39$               ;IF NOT DONE CHECK THIS 4K MEMORY BANK
7317  021106  000410                    BR     5$                ;EXIT THE TEST
7318
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C 12

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46 PAGE 145
CVCDDB.P11   14-JUN-82 09:54   TEST 5: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 16 BIT MODE   SEQ 0145

```
7319  021110  125252        50$:    .WORD   125252          ;ADDRESS 000000 DATA PATTERNS
7320  021112  052525                .WORD   052525          ;
7321  021114  146314                .WORD   146314          ;ADDRESS 020000 DATA PATTERNS
7322  021116  031463                .WORD   031463          ;
7323  021120  000377                .WORD   000377          ;ADDRESS 040000 DATA PATTERNS
7324  021122  177400                .WORD   177400          ;
7325  021124  000000                .WORD   000000          ;ADDRESS 060000 DATA PATTERNS
7326  021126  177777                .WORD   177777          ;
7327
7328  021130              51$:    ENDTST
7329  021130              L10041:
7330  021130  104401                TRAP    C$ETST
7331
```

D 12

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 146
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0146

```
7332                                        .SBTTL  TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE
7333
7334                                   ;++
7335                                   ;       THIS TEST WILL READ DATA FROM THE MEMORY SIMULATOR RAM IN 16 BIT MODE
7336                                   ;       AND STORE THE DATA READ IN THE TARGET EMULATOR'S TDAL DIAGNOSTIC LATCHES.
7337                                   ;       ONCE THE DATA HAS BEEN STORED IN THE TDAL DIAGNOSTIC LATCHES, THE PROGRAM
7338                                   ;       WILL CHANGE THE DATA STORED IN THE MEMORY SIMULATOR RAM LOCATION TO ALL
7339                                   ;       ZEROES.  THE PROGRAM WILL NOW SET THE MEMORY SIMULATOR MODULE TO 8 BIT
7340                                   ;       MODE; LOAD THE EVEN ADDRESS OF THE MEMORY SIMULATOR RAM LOCATION INTO
7341                                   ;       THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER; ENABLE THE TDAL DIAG-
7342                                   ;       NOSTIC LATCHES TO THE SYSTEM DATA BUS; AND THEN PERFORM A NORMAL T-11
7343                                   ;       TIMING CYCLE BY PULSING THE SIGNALS RAS, CAS AND PI.  THE ABOVE OPERATION
7344                                   ;       WILL CAUSE THE LOW BYTE OF THE SYSTEM BUS DATA TO BE WRITTEN INTO THE LOW
7345                                   ;       BYTE OF THE MEMORY SIMULATOR RAM LOCATION.  THE PROGRAM WILL CHECK THAT
7346                                   ;       THE CORRECT ADDRESS WAS CLOCKED INTO THE MEMORY SIMULATOR'S SYSTEM BUS
7347                                   ;       ADDRESS LATCHES AND THAT THE LOW BYTE OF THE INITIAL DATA WAS WRITTEN
7348                                   ;       INTO THE MEMORY SIMULATOR RAM LOCATION.  THE HIGH BYTE OF THE LOCATION
7349                                   ;       SHOULD REMAIN ALL ZEROES DURING THIS WRITE OPERATION.  THE PROGRAM WILL
7350                                   ;       NOW RESET THE MEMORY SIMULATOR MODULE TO 8 BIT MODE; LOAD THE ODD ADDRESS
7351                                   ;       OF THE MEMORY SIMULATOR LOCATION INTO THE TARGET EMULATOR'S DIAGNOSTIC
7352                                   ;       ADDRESS REGISTER; AND THEN PERFORM A NORMAL T-11 TIMING CYCLE.  THE
7353                                   ;       ABOVE OPERATION WILL CAUSE THE LOW BYTE OF THE SYSTEM BUS DATA, WHICH
7354                                   ;       CONTAINS THE DATA OF THE LOW BYTE OF THE TDAL DIAGNOSTIC LATCH, TO BE
7355                                   ;       WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM LOCATION.  THE
7356                                   ;       PROGRAM WILL CHECK THAT THE CORRECT ADDRESS WAS CLOCKED INTO THE MEMORY
7357                                   ;       SIMULATOR SYSTEM ADDRESS BUS LATCHES AND THAT THE LOW BYTE OF THE INITIAL
7358                                   ;       DATA WAS WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM LOCATION.
7359                                   ;       THE LOW BYTE OF THE LOCATION SHOULD REMAIN UNCHANGED DURING THIS WRITE
7360                                   ;       OPERATION.  THE ABOVE SEQUENCE WILL BE PERFORMED FOR ADDRESSES 0, 20000,
7361                                   ;       40000 AND 60000.  THESE ADDRESSES ARE THE FIRST ADDRESSES OF EACH 4K BANK
7362                                   ;       OF MEMORY SIMULATOR RAM.  THE DATA LOADED INTO THE ADDRESSES ARE 052652,
7363                                   ;       146063, 000377 AND 125125 RESPECTIVELY.  AFTER THE DATA HAS BEEN WRITTEN
7364                                   ;       BACK INTO THE MEMORY SIMULATOR RAM IN 8 BIT MODE, THE DATA IN THESE
7365                                   ;       ADDRESSES SHOULD BE 125252, 031463, 177777, AND 052525 RESPECTIVELY. THE
7366                                   ;       LAST PORTION OF THIS TEST WILL READ AND CHECK EACH ADDRESS TO CONTAIN
7367                                   ;       THE CORRECT DATA.  THIS IS DONE TO CHECK THE RAM WRITE AND SELECT LOGIC.
7368                                   ;--
7369
7370    021132                              BGNTST
7371    021132                         T6::
7372    021132  004737  007440              JSR     PC,INITMD                       ;INITIALIZE MDE/T-11 SYSTEM MODULES
7373
7374                                   ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7375                                   ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7376
7377    021136  004737  011250              JSR     PC,SLCTMS                       ;SELECT MEMORY SIMULATOR MODULE
7378
7379                                   ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM.  THE
7380                                   ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H' AND 'MPIN H' SET TO
7381                                   ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM.  MAP PROTECTION RAM
7382                                   ;BITS 'WRE H' AND 'RDE H' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
7383                                   ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
7384                                   ;WHEN 'RDE H' AND 'WRE H' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
7385                                   ;TO THOSE ADDRESSES.
7386
7387    021142  004737  011356              JSR     PC,MPRAM                        ;GO LOAD, READ AND CHECK MAP PROTECT RAM
```

```
7388
7389                                        ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0.  THE FOLLOWING DATA
7390                                        ;PATTERNS: 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
7391                                        ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0.  THESE PATTERNS
7392                                        ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
7393                                        ;ADDRESSED.
7394
7395    021146  004737  011642              JSR     PC,MSRAM0                 ;LOAD, READ AND CHECK MODULE SELECT RAM 0
7396
7397                                        ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1.  THE FOLLOWING DATA PATTERNS
7398                                        ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
7399                                        ;AT ADDRESS 0: 17, 0, 0 AND 0.  THESE PATTERNS WILL ENABLE THE FIRST 32K
7400                                        ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
7401
7402    021152  004737  012012              JSR     PC,MSRAM1                 ;LOAD, READ AND CHECK MODULE SELECT RAM 1
7403
7404    021156  005001                      CLR     R1                        ;SETUP STARTING ADDRESS TO EQUAL ZERO
7405    021160  012702  023740              MOV     #52$,R2                   ;SETUP POINTER TO DATA TABLE
7406
7407    021164                      1$:     BGNSEG
7408    021164  104404                      TRAP    C$BSEG
7409
7410                                        ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7411                                        ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7412
7413    021166  004737  012214              JSR     PC,SLCTTE                 ;SELECT TARGET EMULATOR MODULE
7414
7415                                        ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL "BRKRES L"
7416                                        ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
7417                                        ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
7418                                        ;THE SIGNAL "BRKRES L" VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
7419                                        ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
7420                                        ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED VIA THE
7421                                        ;THE SIGNAL "RASP L" LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
7422                                        ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
7423                                        ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
7424
7425    021172  012737  043020  002334      MOV     #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
7426    021200  004737  012766              JSR     PC,BRKRES                 ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
7427
7428                                        ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
7429                                        ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
7430                                        ;REGISTER 6.
7431
7432    021204  004537  012234              JSR     R5,SELTER                 ;SELECT REGISTER SPECIFIED BY NEXT WORD
7433    021210  000003                      .WORD   HDAL                      ;SELECT THE HDAL REGISTER
7434
7435                                        ;SET HDAL REGISTER BITS 9,4,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
7436                                        ;ZERO.  HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
7437                                        ;AND CONTROL SIGNALS.  HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
7438                                        ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS.  HDAL REGISTER
7439                                        ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
7440                                        ;HDAL REGISTER BITS 4 AND 3 SET TO ONES WILL SET THE SIGNALS XR/WLB H
7441                                        ;AND XR/WHB H TO THE HIGH STATE.  THESE SIGNALS WILL CAUSE THE SIGNAL
7442                                        ;"REAT H" TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE SIGNALS XRAS H
7443                                        ;AND XCAS H ARE ASSERTED HIGH.
```

F 12

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 148
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0148

```
7444
7445   021212  012737  001034  002346            MOV      #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,4,3 + 2 TO ONES
7446   021220  004737  011216                     JSR      PC,LDRDT6                 ;GO LOAD, READ AND CHECK HDAL REGISTER
7447   021224  001405                              BEQ      2$                       ;IF LOADED OK THEN CONTINUE
7448   021226                                      ERRDF    12,HDALRG,TO6ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
7449   021226  104455                              TRAP     C$ERDF
7450   021230  000014                              .WORD    12
7451   021232  003756                              .WORD    HDALRG
7452   021234  006732                              .WORD    TO6ERR
7453   021236                                      CKLOOP
7454   021236  104406                              TRAP     C$CLP1
7455
7456                                               ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
7457                                               ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
7458                                               ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L".
7459
7460   021240  005037  002340            2$:       CLR      T4LOAD                   ;SETUP TO CLEAR ALL OTHER R/W BITS
7461   021244  004737  012706                      JSR      PC,CLRPSM                ;PULSE INVD L VIA VDAL2 H
7462
7463                                               ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON
7464                                               ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
7465                                               ;BE WRITTEN OR READ.
7466
7467   021250  004537  012234                      JSR      R5,SELTER                ;SELECT REGISTER SPECIFIED BY NEXT WORD
7468   021254  000004                              .WORD    MODE                     ;SELECT THE MODE REGISTER
7469
7470                                               ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
7471                                               ;ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
7472
7473   021256  005037  002346                      CLR      T6LOAD                   ;SETUP TO CLEAR ALL MODE REGISTER BITS
7474   021262  004737  011216                      JSR      PC,LDRDT6                ;GO LOAD, READ AND CHECK MODE REGISTER
7475   021266  001405                              BEQ      3$                       ;IF LOADED OK THEN CONTINUE
7476   021270                                      ERRDF    12,MODREG,TO6ERR         ;MODE REGISTER NOT EQUAL EXPECTED
7477   021270  104455                              TRAP     C$ERDF
7478   021272  000014                              .WORD    12
7479   021274  004002                              .WORD    MODREG
7480   021276  006732                              .WORD    TO6ERR
7481   021300                                      CKLOOP
7482   021300  104406                              TRAP     C$CLP1
7483
7484                                               ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
7485                                               ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
7486                                               ;READ COMMAND TO CONTROL REGISTER 6..  THE EOAI REGISTER NEEDS FDALO H
7487                                               ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
7488                                               ;TER WILL BE ADDRESSED.
7489
7490   021302  004537  012234            3$:       JSR      R5,SELTER                ;SELECT REGISTER SPECIFIED BY NEXT WORD
7491   021306  000002                              .WORD    FDAL                     ;SELECT EOAI AND FDAL REGISTER
7492
7493                                               ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER.  THE EOAI REGISTER WILL
7494                                               ;BE LOADED AND CHECKED FOR ZEROES.  THE FDAL REGISTER WILL BE LOADED AND
7495                                               ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
7496
7497   021310  012737  000001  002346            MOV      #FDALO,T6LOAD            ;SETUP EOAI AND FDAL REG DATA PATTERN
7498   021316  004737  011216                     JSR      PC,LDRDT6               ;GO LOAD, READ AND CHECK EOAI + FDAL REG
7499   021322  001405                             BEQ      4$                      ;IF LOADED OK THEN CONTINUE
```

```
7500  021324                                  ERRDF   12,EOAIFD,TO6ERR       ;EOAI OR FDAL REGISTER ERROR
7501  021324  104455                          TRAP    C$ERDF
7502  021326  000014                          .WORD   12
7503  021330  004047                          .WORD   EOAIFD
7504  021332  006732                          .WORD   TO6ERR
7505  021334                                  CKLOOP
7506  021334  104406                          TRAP    C$CLP1
7507

7508                          ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
7509                          ;CHANGES OCCURED DOING THE PAST SEQUENCES.
7510
7511  021336  004737  011200  4$:     JSR     PC,READT4              ;READ AND CHECK VDAL REGISTER
7512  021342  001405                          BEQ     5$                     ;IF NO CHANGES THEN CONTINUE
7513  021344                                  ERRDF   11,VDALRG,T4EROR       ;VDAL OR PAUSE STATE MACHINE ERROR
7514  021344  104455                          TRAP    C$ERDF
7515  021346  000013                          .WORD   11
7516  021350  003710                          .WORD   VDALRG
7517  021352  006716                          .WORD   T4EROR
7518  021354                                  CKLOOP
7519  021354  104406                          TRAP    C$CLP1
7520

7521                          ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7522                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7523
7524  021356  004737  011250  5$:     JSR     PC,SLCTMS              ;SELECT MEMORY SIMULATOR MODULE
7525

7526                          ;SET THE SIGNAL 'MP H' TO A ONE AND PULSE THE SIGNAL 'RST H'.  THE
7527                          ;SIGNAL 'MP H' ON A ONE WILL ENABLE THE MAP PROTECTION RAM BITS
7528                          ;TO THE SYSTEM BUS ALONG WITH THE SIGNAL MSBRK H.  PULSING THE SIGNAL
7529                          ;'RST H' WILL PRESET THE RDV AND WRV FLIP-FLOP'S TO A ONE.  WHEN THE
7530                          ;FLIP-FLOP'S ARE SET TO A ONE, THE SIGNAL 'BRK L' WILL BE ASSERTED
7531                          ;HIGH, THUS NO BREAK CONDITION IS GENERATED FROM THE MEMORY SIMULATOR.
7532
7533  021362  112737  000004  002234  MOVB    #MPH,SOLOAD            ;SET THE SIGNAL MP H TO HIGH STATE
7534  021370  004737  011270          JSR     PC,MSRSTH             ;SET RST H TO ONE AND PULSE RST H
7535

7536                          ;LOAD MEMORY SIMULATOR RAM ADDRESS TO BE TESTED INTO CONTROL REGISTER 4.
7537                          ;THE ADDRESSES TO BE TESTED ARE 000000, 020000, 040000 OR 060000.
7538
7539  021374  010137  002254          MOV     R1,S4LOAD             ;SETUP TO LOAD ADDRESS TO BE TESTED
7540  021400  004737  010606          JSR     PC,LDRDS4             ;LOAD READ AND CHECK CONTROL REG 4
7541  021404  001405                  BEQ     6$                    ;IF LOADED OK THEN CONTINUE
7542  021406                          ERRDF   3,MSADRG,S4EROR       ;MSAD 15:0 REGISTER ERROR
7543  021406  104455                  TRAP    C$ERDF
7544  021410  000003                  .WORD   3
7545  021412  002510                  .WORD   MSADRG
7546  021414  005336                  .WORD   S4EROR
7547  021416                          CKLOOP
7548  021416  104406                  TRAP    C$CLP1
7549

7550                          ;CLEAR BITS MSEL1 H, MSEL0 H, MSAD17 H AND MSAD16 H IN CONTROL REGISTER
7551                          ;2.  MSEL0 H AND MSEL1 H ON A ZERO WILL CAUSE THE SIGNAL 'SSM L' TO BE
7552                          ;ASSERTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.  ON A WRITE
7553                          ;OR READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE WRITTEN INTO OR
7554                          ;READ FROM MEMORY SIMULATOR RAM ADDRESSES BY CONTROL REGISTER 2 AND 4.
7555                          ;THE MEMORY SIMULATOR RAM'S ARE ENABLED BY THE DATA PATTERNS PREVIOUSLY
```

H 12

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 150
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0150

```
7556                                                      ;WRITTEN INTO MODULE SELECT RAMS 0 AND 1.  MSAD17 H AND MSAD16 H WILL BE
7557                                                      ;LOADED AND CHECKED WITH ZEROES.  THE PROGRAM WILL EXPECT CONTROL REGIS-
7558                                                      ;TER 2 BITS 'ESR H' AND 'WREN H' TO BE READ AS ONES AS A RESULT OF MAP
7559                                                      ;PROTECTION RAM BITS 'MPIN H' AND 'WRE H' BEING SET TO ONES.
7560
7561   021420  005037  002244            6$:    CLR     S2LOAD                    ;SET ALL BITS IN REG 2 TO ZEROES
7562   021424  013737  002244  002246           MOV     S2LOAD,S2GOOD             ;COPY DATA LOADED TO EXPECTED
7563   021432  052737  000140  002246           BIS     #ESRH!WRENH,S2GOOD        ;EXPECT ESR H AND WREN H TO BE ONES
7564   021440  012737  177400  002250           MOV     #177400,S2MASK            ;SETUP TO COMPARE LOW BYTE
7565   021446  004737  010554                   JSR     PC,LDRD2S                 ;LOAD, READ AND CHECK CONTROL REG 2
7566   021452  001405                           BEQ     7$                        ;IF LOADED OK THEN CONTINUE
7567   021454                                   ERRDF   2,,S2EROR                 ;CONTROL REGISTER 2 NOT = EXPECTED
7568   021454  104455                           TRAP    C$ERDF
7569   021456  000002                           .WORD   2
7570   021460  000000                           .WORD   0
7571   021462  005322                           .WORD   S2EROR
7572   021464                                   CKLOOP
7573   021464  104406                           TRAP    C$CLP1
7574
7575                                                      ;LOAD DATA PATTERN INTO MEMORY SIMULATOR RAM ADDRESSED BY CONTROL
7576                                                      ;REGISTER 2 AND 4.  ONE OF THE FOLLOWING DATA PATTERNS WILL BE LOADED
7577                                                      ;INTO THE TEST ADDRESS LISTED BELOW:
7578                                                      ;    ADDRESS 000000 WILL BE LOADED WITH 052652
7579                                                      ;    ADDRESS 020000 WILL BE LOADED WITH 146063
7580                                                      ;    ADDRESS 040000 WILL BE LOADED WITH 000377
7581                                                      ;    ADDRESS 060000 WILL BE LOADED WITH 125125
7582
7583   021466  005037  002264            7$:    CLR     S6MASK                    ;SETUP TO COMPARE ALL BITS
7584   021472  011237  002260                   MOV     (R2),S6LOAD               ;GET THE DATA PATTERN FROM THE TABLE
7585   021476  004737  010632                   JSR     PC,LDRDS6                 ;GO LOAD, READ AND CHECK RAM LOCATION
7586   021502  001405                           BEQ     8$                        ;IF LOADED OK THEN CONTINUE
7587   021504                                   ERRDF   4,MSGMSR,S6ALLR           ;DATA ERROR IN MEMORY SIMULATOR RAM
7588   021504  104455                           TRAP    C$ERDF
7589   021506  000004                           .WORD   4
7590   021510  002745                           .WORD   MSGMSR
7591   021512  005456                           .WORD   S6ALLR
7592   021514                                   CKLOOP
7593   021514  104406                           TRAP    C$CLP1
7594
7595                                                      ;SET THE SIGNAL 'CTS H' TO A ONE IN CONTROL REGISTER 0.  THIS WILL
7596                                                      ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
7597                                                      ;IN THIS TEST, 'CTS H' ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
7598                                                      ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
7599                                                      ;SYSTEM BUS.
7600
7601   021516  052737  000002  002234    8$:    BIS     #CTSH,S0LOAD              ;SETUP BIT TO BE LOADED
7602   021524  004737  010506                   JSR     PC,LDRDS0                 ;GO LOAD, READ AND CHECK CONTROL REG 2
7603   021530  001405                           BEQ     9$                        ;IF LOADED OK THEN CONTINUE
7604   021532                                   ERRDF   1,,S0EROR                 ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
7605   021532  104455                           TRAP    C$ERDF
7606   021534  000001                           .WORD   1
7607   021536  000000                           .WORD   0
7608   021540  005306                           .WORD   S0EROR
7609   021542                                   CKLOOP
7610   021542  104406                           TRAP    C$CLP1
7611
```

I 12

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 151
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0151

```
7612                                              ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7613                                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7614
7615    021544  004737  012214          9$:       JSR    PC,SLCTTE
7616
7617
7618                                              ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
7619                                              ;2:0 TO A 0.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN WITH THE
7620                                              ;TEST PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.  THE DIAGNOSTIC
7621                                              ;ADDRESS REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER
7622                                              ;BIT 9 BEING SET TO A ONE PREVIOULSY.  ON A READ COMMAND TO CONTROL
7623                                              ;REGISTER 6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
7624
7625    021550  004537  012234                    JSR    R5,SELTER                 ;SELECT REGISTER SPECIFIED BY NEXT WORD
7626    021554  000000                            .WORD  ADDRES                    ;SELECT THE DIAG ADDRESS REG AND ADDR BUS
7627
7628                                              ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
7629                                              ;FOLLOWING ADDRESSES: 000000, 020000, 040000, OR 060000.
7630
7631    021556  010137  002346                    MOV    R1,T6LOAD                 ;GET THE TEST ADDRESS TO BE LOADED
7632    021562  004737  011216                    JSR    PC,LDRDT6                 ;GO LOAD, READ + CHECK DIAG ADDRESS REG
7633    021566  001405                            BEQ    10$                       ;IF LOADED OK THEN CONTINUE
7634    021570                                    ERRDF  12,ADDRRG,T06ERR          ;DIAGNOSTIC ADDRESS REGISTER ERROR
7635    021570  104455                            TRAP   C$ERDF
7636    021572  000014                            .WORD  12
7637    021574  004144                            .WORD  ADDRRG
7638    021576  006732                            .WORD  T06ERR
7639    021600                                    CKLOOP
7640    021600  104406                            TRAP   C$CLP1
7641
7642                                              ;SELECT HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3.  THE
7643                                              ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
7644                                              ;CONTROL REGISTER 6.
7645
7646    021602  004537  012234          10$:      JSR    R5,SELTER                 ;SELECT REGISTER SPECIFIED BY NEXT WORD
7647    021606  000003                            .WORD  HDAL                      ;SELECT THE HDAL REGISTER
7648    021610  012737  001034  002346            MOV    #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;GET BITS PREVIOUSLY LOADED
7649
7650                                              ;START A T-11 MACHINE CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE
7651                                              ;  1.   SET XRAS H AND PRAS H TO THE HIGH STATE
7652                                              ;  2.   SET XCAS H AND PCAS H TO THE HIGH STATE
7653                                              ;  3.   SET XPI L AND PPI L TO THE LOW STATE
7654                                              ;SETTING THE SIGNAL PRAS H TO THE HIGH STATE WILL CAUSE THE SIGNAL
7655                                              ;"ADVAL H" TO GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE SYSTEM
7656                                              ;ADDRESS BUS BITS 17:0 INTO THE MEMORY SIMULATOR ADDRESS BUS LATCHES.
7657                                              ;WHEN  THE  SIGNALS  XRAS  H  AND  XCAS  H  ARE  ASSERTED
7658                                              ;HIGH, THE SIGNAL REAT H WILL GO FROM A LOW TO A HIGH STATE, THUS CAUSING
7659                                              ;THE SIGNAL READ H TO GO FROM A LOW TO A HIGH STATE.  THE TARGET EMULATORS
7660                                              ;SIGNAL READ H ALONG WITH THE MEMORY SIMULATOR'S SIGNALS CTS H AND ESR H
7661                                              ;WILL CAUSE THE MEMORY SIMULATOR RAM DATA TO BE PUT ONTO THE SYSTEM DATA
7662                                              ;BUS.  WHEN THE TARGET EMULATORS SIGNAL REAT H IS ASSERTED HIGH, THE
7663                                              ;TARGET EMULATORS SIGNAL MSDI H WILL BE ASSERTED HIGH, THUS ENABLING
7664                                              ;THE SYSTEM DATA BUS TO THE TARGET EMULATORS EODAL BUS.  THE MEMORY
7665                                              ;SIMULATOR RAM'S ARE ADDRESSED BY THE MEMORY SIMULATOR SYSTEM BUS ADDRESS
7666                                              ;LATCHES WHICH WERE CLOCKED BY THE SIGNAL ADVAL H.  THE DATA ON SYSTEM
7667                                              ;ADDRESS BUS COMES FROM THE TARGET EMULATOR'S DIAGNOSTIC ADDRESS REGISTER.
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J 12

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 152
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0152

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7668
7669    021616  004737  012300           JSR     PC,XRASH               ;SET XRAS H AND PRAS H TO HIGH STATE
7670    021622  004737  012404           JSR     PC,XCASH               ;SET XCAS H AND PCAS H TO HIGH STATE
7671    021626  004737  012510           JSR     PC,XPIH                ;SET XPI H AND PPI H TO THE LOW STATE
7672
7673                                      ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H ARE
7674                                      ;ASSERTED HIGH (1'S).
7675
7676    021632  012737  000110  002342    MOV     #VDAL6!VDAL3,T4GOOD    ;EXPECT READ H AND MSDI H TO BE ONES
7677    021640  004737  011200            JSR     PC,READT4              ;READ VDAL AND PAUSE STATE MACHINE REG
7678    021644  001405                    BEQ     11$                    ;IF DATA OK THEN CONTINUE
7679    021646                            ERRDF   11,VDALRG,T4EROR       ;VDAL OR PAUSE STATE MACHINE ERROR
7680    021646  104455                    TRAP    C$ERDF
7681    021650  000013                    .WORD   11
7682    021652  003710                    .WORD   VDALRG
7683    021654  006716                    .WORD   T4EROR
7684    021656                            CKLOOP
7685    021656  104406                    TRAP    C$CLP1
7686
7687                                      ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7688                                      ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7689
7690    021660  004737  011250    11$:    JSR     PC,SLCTMS              ;SELECT THE MEMORY SIMULATOR MODULE
7691
7692                                      ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
7693                                      ;TARGET EMULATOR MODULE SET THE SIGNALS ADVAL H AND READ H TO THE
7694                                      ;HIGH STATE FROM THE LOW STATE.
7695
7696    021664  004737  010522            JSR     PC,READS0              ;READ AND CHECK CONTROL REGISTER 0
7697    021670  001405                    BEQ     12$                    ;IF NO CHANGES THEN CONTINUE
7698    021672                            ERRDF   1,,S0EROR              ;CONTROL REGISTER 0 NOT = EXPECTED
7699    021672  104455                    TRAP    C$ERDF
7700    021674  000001                    .WORD   1
7701    021676  000000                    .WORD   0
7702    021700  005306                    .WORD   S0EROR
7703    021702                            CKLOOP
7704    021702  104406                    TRAP    C$CLP1
7705
7706                                      ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
7707                                      ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
7708                                      ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.  THE SIGNAL ADVAL H
7709                                      ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
7710                                      ;SIGNAL PRAS H WAS SET HIGH FROM THE LOW STATE.  THE MEMORY SIMULATORS
7711                                      ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
7712                                      ;BITS VIA THE SIGNALS CTS H AND CTS L.
7713
7714    021704  010137  002254    12$:    MOV     R1,S4LOAD             ;GET THE EXPECTED ADDRESS LOADED
7715    021710  004737  010614            JSR     PC,READS4             ;READ AND CHECK CONTROL REGISTER 4
7716    021714  001405                    BEQ     13$                   ;IF DATA = TE DIAG ADDRESS REG - CONT
7717    021716                            ERRDF   3,TEMSAD,S04ERR       ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
7718    021716  104455                    TRAP    C$ERDF
7719    021720  000003                    .WORD   3
7720    021722  002534                    .WORD   TEMSAD
7721    021724  005406                    .WORD   S04ERR
7722    021726                            CKLOOP
7723    021726  104406                    TRAP    C$CLP1
```

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7724
7725                                          ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
7726                                          ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
7727                                          ;ZEROES FOR THESE TWO ADDRESSES.  ADDRESS BITS 17 AND 16 WERE CLOCKED
7728                                          ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
7729                                          ;ADVAL H.  THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
7730                                          ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE FROM
7731                                          ;THE LOW STATE.  THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
7732                                          ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
7733                                          ;MEMORY SIMULATOR MODULE.
7734
7735  021730  052737  000014  002250  13$:  BIS     #MSEL0!MSEL1,S2MASK     ;IGNORE TRI-STATED BITS WHEN CTS H SET
7736  021736  005037  002244              CLR     S2LOAD                 ;EXPECT MSAD 17:16 TO BE ZERO
7737  021742  013737  002244  002246      MOV     S2LOAD,S2GOOD          ;COPY DATA LOADED TO EXPECTED
7738  021750  052737  000140  002246      BIS     #ESRH!WRENH,S2GOOD     ;EXPECT MAP PROTECT BITS TO BE ONES
7739  021756  004737  010562              JSR     PC,READS2              ;READ AND CHECK CONTROL REGISTER 2
7740  021762  001405                      BEQ     14$                    ;IF DATA OK THEN CONTINUE
7741  021764                              ERRDF   2,TEMSA1,S02ERR        ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
7742  021764  104455                      TRAP    C$ERDF
7743  021766  000002                      .WORD   2
7744  021770  002410                      .WORD   TEMSA1
7745  021772  005366                      .WORD   S02ERR
7746  021774                              CKLOOP
7747  021774  104406                      TRAP    C$CLP1
7748
7749                                          ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7750                                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7751
7752  021776  004737  012214              14$:  JSR     PC,SLCTTE              ;SELECT THE TARGET EMULATOR MODULE
7753
7754                                          ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO A 7.  THE EODAL BUS
7755                                          ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
7756
7757  022002  004537  012234              JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
7758  022006  000007                      .WORD   EODAL                  ;SELECT THE EODAL BUS TO BE READ
7759
7760                                          ;AT THIS TIME THE MEMORY SIMULATOR RAM DATA SHOULD BE ENABLED ON THE
7761                                          ;SYSTEM DATA BUS AND ENABLED TO THE TARGET EMULATORS EODAL BUS VIA THE
7762                                          ;TARGET EMULATOR SIGNALS READ H AND MSDI H RESPECTIVELY.  THE MEMORY
7763                                          ;SIMULATOR RAM IS ADDRESSED BY THE TARGET EMULATORS DIAGNOSTIC ADDRESS
7764                                          ;REGISTER WHICH WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS
7765                                          ;BUS LATCHES VIA THE SIGNAL ADVAL H.  THE DATA PATTERNS LOADED INTO
7766                                          ;THE TEST ADDRESSES OF THE MEMORY SIMULATOR RAM'S ARE LISTED BELOW:
7767                                          ;    ADDRESS 000000 WILL BE LOADED WITH 052652
7768                                          ;    ADDRESS 020000 WILL BE LOADED WITH 146063
7769                                          ;    ADDRESS 040000 WILL BE LOADED WITH 000377
7770                                          ;    ADDRESS 060000 WILL BE LOADED WITH 125125
7771
7772  022010  013737  002260  002346      MOV     S6LOAD,T6LOAD          ;GET DATA LOADED INTO MS RAM ADDRESSED
7773  022016  004737  011224              JSR     PC,READT6              ;READ SYSTEM DATA BUS ON THE EODAL BUS
7774  022022  001405                      BEQ     15$                    ;IF DATA = MS RAM DATA THEN CONTINUE
7775  022024                              ERRDF   12,MSTEDE,T6ALLR       ;MS RAM DATA TO TE EODAL BUS ERROR
7776  022024  104455                      TRAP    C$ERDF
7777  022026  000014                      .WORD   12
7778  022030  004243                      .WORD   MSTEDE
7779  022032  006746                      .WORD   T6ALLR
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7780   022034                              CKLOOP
7781   022034   104406                     TRAP     C$CLP1
7782
7783                                        ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.   THE EIDAL BUS
7784                                        ;WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6.
7785
7786   022036   004537  012234      15$:   JSR      R5,SELTER                  ;SELECT REGISTER SPECIFIED BY NEXT WORD
7787   022042   000006                      .WORD    EIDAL                      ;SELECT THE EIDAL BUS TO BE READ
7788
7789                                        ;IN THE PREVIOUS DATA CHECK, THE PROGRAM VERIFIED THAT THE MEMORY SIMU-
7790                                        ;LATOR RAM DATA WAS ENBALED TO THE EODAL BUS VIA THE SYSTEM DATA BUS.
7791                                        ;IN THIS SECTION, THE PROGRAM WILL CHECK THAT THE EODAL BUS IS ENABLED
7792                                        ;TO THE EIDAL BUS VIA THE CDAL BUS AS A RESULT OF THE SIGNALS COHB L AND
7793                                        ;COLB L BEING ASSERTED LOW.   THE SIGNALS COHB L AND COLB L ARE ASSERTED
7794                                        ;LOW AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED HIGH: ETR L,
7795                                        ;PR/WLB H, PR/WHB H, PPI H, DMG L, AND MR11 L.   THE DATA READ SHOULD BE
7796                                        ;THE SANE AS THAT WHICH WAS ENABLED TO THE EODAL BUS.   THE DATA PATTERNS
7797                                        ;LOADED INTO THE TEST ADDRESS OF THE MEMORY SIMULATOR RAMS ARE AS FOLLOWS:
7798                                        ;    ADDRESS 000000 WILL BE LOADED WITH 052652
7799                                        ;    ADDRESS 020000 WILL BE LOADED WITH 146063
7800                                        ;    ADDRESS 040000 WILL BE LOADED WITH 000377
7801                                        ;    ADDRESS 060000 WILL BE LOADED WITH 125125
7802
7803   022044   013737  002260  002346     MOV      S6LOAD,T6LOAD              ;GET DATA LOADED INTO MS RAM ADDRESSED
7804   022052   004737  011224             JSR      PC,READT6                  ;READ SYSTEM DATA BUS ON EIDAL VIA EODAL
7805   022056   001405                      BEQ      16$                       ;IF DATA OK THEN CONTINUE
7806   022060                               ERRDF    12,MSTEEI,T6ALLR          ;MS RAM DATA TO EIDAL BUS VIA EODAL BUS
7807   022060   104455                      TRAP     C$ERDF
7808   022062   000014                      .WORD    12
7809   022064   004331                      .WORD    MSTEEI
7810   022066   006746                      .WORD    T6ALLR
7811   022070                               CKLOOP
7812   022070   104406                      TRAP     C$CLP1
7813
7814                                        ;IN THE PREVIOUS DATA CHECKS, MEMORY SIMULATOR RAM DATA WAS ENABLED TO
7815                                        ;THE SYSTEM DATA BUS WHICH ALSO WAS ENABLED TO THE EODAL, CDAL AND EIDAL
7816                                        ;BUSES.   IN ADDITION TO THESE BUSES, MEMORY SIMULATOR RAM DATA WILL BE
7817                                        ;ENABLED TO THE TDAL BUS VIA THE CDAL BUS BY THE SIGNALS DTHB L AND
7818                                        ;DTLB H.   THE SIGNALS DTHB L AND DTLB L ARE ASSERTED LOW AS A RESULT OF
7819                                        ;THE SIGNALS PSEL1 L, PSEL0 L, PBCLR L AND CPIW L BEING ASSERTED HIGH AND
7820                                        ;THE T-11 SIGNAL CCAS H BEING ASSERTED LOW.   TO CAPTURE THE MEMORY
7821                                        ;SIMULATOR RAM DATA ON THE TDAL BUS, THE PROGRAM WILL SET VDAL2 H TO A
7822                                        ;ONE AND THEN A ZERO TO CLOCK THE TDAL BUS DATA INTO THE TDAL DIAGNOSTIC
7823                                        ;LATCHES.
7824
7825   022072   052737  000004  002340  16$:  BIS    #VDAL2,T4LOAD            ;SET BIT TO CLOCK TDAL DIAG LATCHES
7826   022100   052737  000004  002342        BIS    #VDAL2,T4GOOD            ;EXPECT VDAL2 H TO BE SET ON READ
7827   022106   004737  011172                 JSR    PC,LDRD4T               ;LOAD, READ AND CHECK VDAL REGISTER
7828   022112   001405                         BEQ    17$                     ;IF LOADED OK THEN CONTINUE
7829   022114                                  ERRDF  11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
7830   022114   104455                         TRAP   C$ERDF
7831   022116   000013                         .WORD  11
7832   022120   003710                         .WORD  VDALRG
7833   022122   006716                         .WORD  T4EROR
7834   022124                                  CKLOOP
7835   022124   104406                         TRAP   C$CLP1
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M 12

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 155
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0155

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7836   022126  042737  000004  002340   17$:    BIC     #VDAL2,T4LOAD          :SET CLOCK SIGNAL TO A ZERO
7837   022134  042737  000004  002342           BIC     #VDAL2,T4GOOD          :EXPECT VDAL2 H TO BE 0 ON A READ
7838   022142  004737  011172                    JSR     PC,LDRD4T             :LOAD, READ AND CHECK VDAL REGISTER
7839   022146  001405                            BEQ     18$                  :IF LOADED OK THEN CONTINUE
7840   022150                                    ERRDF   11,VDALRG,T4EROR     :VDAL REGISTER NOT EQUAL EXPECTED
7841   022150  104455                            TRAP    C$ERDF
7842   022152  000013                            .WORD   11
7843   022154  003710                            .WORD   VDALRG
7844   022156  006716                            .WORD   T4EROR
7845   022160                                    CKLOOP
7846   022160  104406                            TRAP    C$CLP1
7847
7848                                     :SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
7849                                     :REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
7850                                     :REGISTER 6.
7851
7852   022162  004537  012234           18$:    JSR     R5,SELTER            :SELECT REGISTER SPECIFIED BY NEXT WORD
7853   022166  000003                            .WORD   HDAL                 :SELECT THE HDAL REGISTER
7854
7855                                     :FINISH THE T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
7856                                     :  1. SET XCAS H AND PCAS H TO THE LOW STATE
7857                                     :  2. SET XPI L AND PPI L TO THE HIGH STATE
7858                                     :  3. SET XRAS H AND PRAS H TO THE LOW STATE
7859
7860   022170  012737  001034  002346           MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD  ;SETUP PREVIOULSY LOADED BITS
7861   022176  004737  012436                    JSR     PC,XCASL             :SET XCAS H AND PCAS H TO LOW STATE
7862   022202  004737  012542                    JSR     PC,XPIL              :SET XPI L AND PPI L TO THE HIGH STATE
7863   022206  004737  012332                    JSR     PC,XRASL             :SET XRAS H AND PRAS H TO LOW STATE
7864
7865                                     :READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS READ H AND MSDI H
7866                                     :WENT TO A ZERO AS A RESULT OF SETTING THE SIGNALS XCAS H AND XRAS H
7867                                     :TO THE LOW STATE.
7868
7869   022212  005037  002342                    CLR     T4GOOD               :EXPECT VDAL REGISTER TO BE A 0
7870   022216  004737  011200                    JSR     PC,READT4            :READ AND CHECK VDAL REGISTER
7871   022222  001405                            BEQ     19$                  :IF OK THEN CONTINUE
7872   022224                                    ERRDF   11,VDALRG,T4EROR     :VDAL OR PAUSE STATE MACHINE ERROR
7873   022224  104455                            TRAP    C$ERDF
7874   022226  000013                            .WORD   11
7875   022230  003710                            .WORD   VDALRG
7876   022232  006716                            .WORD   T4EROR
7877   022234                                    CKLOOP
7878   022234  104406                            TRAP    C$CLP1
7879
7880                                     :SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7881                                     :REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7882
7883   022236  004737  011250           19$:    JSR     PC,SLCTMS            :SELECT THE MEMORY SIMULATOR MODULE
7884
7885                                     :SET THE SIGNAL CTS H TO THE LOW STATE BY CLEARING THE BIT IN CONTROL
7886                                     :REGISTER 0.  THIS WILL DISABLE THE SYSTEM BUS SIGNALS TO AND FROM
7887                                     :THE MEMORY SIMULATOR MODULE.
7888
7889   022242  112737  000004  002234           MOVB    #MPH,SOLOAD          :CLEAR CTS H AND LEAVE MP H SET TO A 1
7890   022250  004737  010506                    JSR     PC,LDRDS0            :LOAD, READ AND CHECK CONTROL REG 0
7891   022254  001405                            BEQ     20$                  :IF LOADED OK THEN CONTINUE
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N 12

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 156
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0156

```
7892   022256                                    ERRDF   1,,SOEROR           ;CONTROL REGISTER O NOT EQUAL EXPECTED
7893   022256   104455                           TRAP    C$ERDF
7894   022260   000001                           .WORD   1
7895   022262   000000                           .WORD   0
7896   022264   005306                           .WORD   SOEROR
7897   022266                                    CKLOOP
7898   022266   104406                           TRAP    C$CLP1
7899
7900                                             ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
7901                                             ;LOADED PREVIOUSLY IS STILL LOADED
7902
7903   022270   004737   010614      20$:        JSR     PC,READS4           ;READ AND CHECK CONTROL REGISTER 4
7904   022274   001405                           BEQ     21$                 ;IF ADDRESS 0 THEN CONTINUE
7905   022276                                    ERRDF   3,MSADRG,S4EROR      ;MSAD 15:0 REGISTER ERROR
7906   022276   104455                           TRAP    C$ERDF
7907   022300   000003                           .WORD   3
7908   022302   002510                           .WORD   MSADRG
7909   022304   005336                           .WORD   S4EROR
7910   022306                                    CKLOOP
7911   022306   104406                           TRAP    C$CLP1
7912
7913                                             ;READ CONTROL REGISTER 0 TO CHECK THAT THE DATA LOADED INTO IT PREVIOUSLY
7914                                             ;HAS NOT CHANGED.  THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
7915                                             ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBRK H.  THE SIGNALS ESR H
7916                                             ;AND WREN H SHOULD BE READ AS ONES.
7917
7918   022310   012737   177400  002250  21$:    MOV     #177400,S2MASK       ;SETUP TO CHECK ALL OFF LOW BYTE
7919   022316   004737   010562            JSR     PC,READS2            ;READ AND CHECK CONTROL REGISTER 2
7920   022322   001405                           BEQ     22$                 ;IF NO CHANGE THEN CONTINUE
7921   022324                                    ERRDF   2,,S2EROR           ;CONTROL REG 2 NOT EQUAL EXPECTED
7922   022324   104455                           TRAP    C$ERDF
7923   022326   000002                           .WORD   2
7924   022330   000000                           .WORD   0
7925   022332   005322                           .WORD   S2EROR
7926   022334                                    CKLOOP
7927   022334   104406                           TRAP    C$CLP1
7928
7929                                             ;WRITE INTO THE MEMORY SIMULATOR RAM'S TEST ADDRESS A DATA PATTERN OF
7930                                             ;ALL ZEROES.  THIS IS DONE TO CHECK THAT DATA CAN BE WRITTEN BACK INTO
7931                                             ;THIS ADDRESS LATER ON IN THIS TEST IN 8 BIT MODE.
7932
7933   022336   005037   002260      22$:        CLR     S6LOAD              ;SET NEW DATA PATTERN TO ALL ZEROES
7934   022342   004737   010632            JSR     PC,LDRDS6            ;GO LOAD, READ AND CHECK MEM SIM RAM LOC
7935   022346   001405                           BEQ     23$                 ;IF LOADED OK THEN CONTINUE
7936   022350                                    ERRDF   4,MSGMSR,S6ALLR      ;DATA ERROR IN MEMORY SIMULATOR RAM
7937   022350   104455                           TRAP    C$ERDF
7938   022352   000004                           .WORD   4
7939   022354   002745                           .WORD   MSGMSR
7940   022356   005456                           .WORD   S6ALLR
7941   022360                                    CKLOOP
7942   022360   104406                           TRAP    C$CLP1
7943
7944                                             ;SET THE SIGNALS CTS H AND 8 BIT H TO ONES IN CONTROL REGISTER 0.  CTS H
7945                                             ;ON A ONE WILL ENABLE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR
7946                                             ;MODULE.  8 BIT H ON A ONE WILL SET THE MEMORY SIMULATOR MODULE TO 8 BIT
7947                                             ;DATA MODE.
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B 13

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7948
7949    022362  052737  000012  002234  23$:    BIS     #CTSH!BIT8H,SOLOAD      ;SETUP BITS TO BE LOADED
7950    022370  004737  010506                  JSR     PC,LDRDSO              ;LOAD, READ AND CHECK REGISTER 0
7951    022374  001405                          BEQ     24$                   ;IF LOADED OK THEN CONTINUE
7952    022376                                  ERRDF   1,,SOEROR             ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
7953    022376  104455                          TRAP    C$ERDF
7954    022400  000001                          .WORD   1
7955    022402  000000                          .WORD   0
7956    022404  005306                          .WORD   SOEROR
7957    022406                                  CKLOOP
7958    022406  104406                          TRAP    C$CLP1
7959
7960                                            ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
7961                                            ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
7962
7963    022410  004737  012214          24$:    JSR     PC,SLCTTE             ;SELECT THE TARGET EMULATOR MODULE.
7964
7965                                            ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 2.  THE
7966                                            ;EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR READ COMMAND TO
7967                                            ;CONTROL REGISTER 6.
7968
7969    022414  004537  012234                  JSR     R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
7970    022420  000002                          .WORD   FDAL                 ;SELECT EOAI AND FDAL REGISTER
7971
7972                                            ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER.  THE EOAI REGISTER WILL BE
7973                                            ;LOADED AND CHECKED FOR A DATA PATTERN OF ALL ZEROES.  THE FDAL REGISTER
7974                                            ;WILL BE LOADED AND CHECKED FOR A DATA PATTERN OF 3 (FDAL1 H AND FDALO H).
7975                                            ;FDALO H ON A ONE WILL SELECT THE EOAI REGISTER TO BE READ ON A READ COMMAND
7976                                            ;TO CONTROL REGISTER 6 INCTEAD OF THE CTL REGISTER.  FDAL1 H ON A ONE WILL
7977                                            ;ENABLE THE SIGNALS WR HB H AND WR LB H TO THE SYSTEM BUS WHEN THE SIGNAL
7978                                            ;DMG L IS ASSERTED LOW LATER ON IN THIS TEST.
7979
7980    022422  012737  000003  002346          MOV     #FDAL1!FDALO,T6LOAD  ;SETUP BITS TO BE LOADED
7981    022430  004737  011216                  JSR     PC,LDRDT6            ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER
7982    022434  001405                          BEQ     25$                 ;IF LOADED OK THEN CONTINUE
7983    022436                                  ERRDF   12,EOAIFD,T06ERR    ;EOAI 7:0 OR FDAL 7:0 REGISTER ERROR
7984    022436  104455                          TRAP    C$ERDF
7985    022440  000014                          .WORD   12
7986    022442  004047                          .WORD   EOAIFD
7987    022444  006732                          .WORD   T06ERR
7988    022446                                  CKLOOP
7989    022446  104406                          TRAP    C$CLP1
7990
7991                                            ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL REGISTER
7992                                            ;WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
7993
7994    022450  004537  012234          25$:    JSR     R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
7995    022454  000003                          .WORD   HDAL                 ;SELECT THE HDAL REGISTER
7996
7997                                            ;SET THE SIGNALS PSELO L AND PSEL1 L TO THE LOW STATE BY SETTING HDAL
7998                                            ;REGISTER BITS 5 AND 6 TO ONES.  SETTING THESE SIGNALS LOW WILL CAUSE
7999                                            ;THE SIGNALS DBHB L AND DBLB L TO BE ASSERTED LOW THUS ENABLING THE
8000                                            ;TDAL BUS TO THE CDAL BUS AND EIDAL BUS.  SETTING PSELO L AND PSEL1 L
8001                                            ;WILL ALSO CAUSE THE SIGNAL DMG L TO BE ASSERTED LOW.  SET THE SIGNALS
8002                                            ;XR/WHB L AND XR/WLB L TO THE HIGH STATE BY SETTING HDAL REGISTER BITS
8003                                            ;4 AND 3 TO A ZERO.  THIS WILL SET THE READ/WRITE CONTROL LOGIC TO DO
```

C 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 158
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0158

```
8004                                          ;A WRITE WHEN THE SIGNAL XPI H IS SET HIGH.  HDAL9 H WILL BE SET TO A
8005                                          ;ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS
8006                                          ;BUS.  THE DIAGNOSTIC ADDRESS REGISTER WAS LOADED WITH THE TEST ADDRESS EARLIER
8007                                          ;IN THIS TEST.  HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM
8008                                          ;TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
8009
8010  022456  012737  001144  002346         MOV    #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD  ;SETUP BITS TO BE LOADED
8011  022464  004737  011216                 JSR    PC,LDRDT6               ;LOAD, READ AND CHECK HDAL REGISTER
8012  022470  001405                          BEQ    26$                    ;IF LOADED OK THEN CONTINUE
8013  022472                                  ERRDF  12,HDALRG,T06ERR       ;HDAL REGISTER NOT EQUAL EXPECTED
8014  022472  104455                          TRAP   C$ERDF
8015  022474  000014                          .WORD  12
8016  022476  003756                          .WORD  HDALRG
8017  022500  006732                          .WORD  T06ERR
8018  022502                                  CKLOOP
8019  022502  104406                          TRAP   C$CLP1
8020
8021                                          ;SET VDAL0 H TO A ONE TO ENABLE THE OUTPUTS OF THE TDAL DIAGNOSTIC
8022                                          ;LATCHES ONTO THE TDAL BUS.  THE TDAL BUS WILL BE ENABLED TO THE CDAL
8023                                          ;BUS VIA DBHB L AND DBLB L.  THE CDAL BUS WILL BE ENABLED TO THE EIDAL
8024                                          ;BUS UNCONDITIONALY.
8025
8026  022504  012737  000001  002340  26$:   MOV    #VDAL0,T4LOAD          ;SETUP BIT TO BE LOADED
8027  022512  004737  011164                 JSR    PC,LDRDT4              ;LOAD, READ AND CHECK VDAL REGISTER
8028  022516  001405                          BEQ    27$                   ;IF LOADED OK THEN CONTINUE
8029  022520                                  ERRDF  11,VDALRG,T4EROR      ;VDAL REGISTER NOT EQUAL EXPECTED
8030  022520  104455                          TRAP   C$ERDF
8031  022522  000013                          .WORD  11
8032  022524  003710                          .WORD  VDALRG
8033  022526  006716                          .WORD  T4EROR
8034  022530                                  CKLOOP
8035  022530  104406                          TRAP   C$CLP1
8036
8037                                          ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ
8038                                          ;COMMAND TO CONTROL REGISTER 6 THE EIDAL BUS WILL BE READ.
8039
8040  022532  004537  012234          27$:   JSR    R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
8041  022536  000006                          .WORD  EIDAL                 ;SELECT THE EIDAL BUS TO BE READ
8042
8043                                          ;AT THIS POINT IN TIME THE EIDAL BUS SHOULD HAVE THE TDAL DIAGNOSTIC
8044                                          ;LATCHES ENABLED TO IT BY THE SIGNALS DBHB L AND DBLB L BEING ASSERTED
8045                                          ;LOW AND VDAL0 H BEING SET TO A ONE.  THE TDAL LATCHES WERE CLOCKED
8046                                          ;EARLIER IN THE TEST BY THE SIGNAL VDAL2 H.  THESE LATCHES WERE
8047                                          ;CLOCKED WITH THE DATA FROM THE MEMORY SIMULATOR RAM DURING A READ
8048                                          ;OPERATION OF THE MEMORY SIMULATOR RAM TEST ADDRESS.
8049
8050  022540  011237  002346                 MOV    (R2),T6LOAD           ;GET 1ST DATA WRITTEN TO MS RAM
8051  022544  004737  011224                 JSR    PC,READT6             ;READ AND CHECK EIDAL BUS
8052  022550  001405                          BEQ    28$                   ;IF DATA OK THEN CONTINUE
8053  022552                                  ERRDF  12,MSTETD,T6ALLR      ;MS RAM DATA TO EIDAL BUS VIA TDAL BUS
8054  022552  104455                          TRAP   C$ERDF
8055  022554  000014                          .WORD  12
8056  022556  004422                          .WORD  MSTETD
8057  022560  006746                          .WORD  T6ALLR
8058  022562                                  CKLOOP
8059  022562  104406                          TRAP   C$CLP1
```

D 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 159
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0159

```
8060
8061                                                  ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
8062                                                  ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
8063                                                  ;REGISTER 6.
8064
8065    022564  004537  012234          28$:    JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
8066    022570  000003                          .WORD   HDAL                    ;SELECT THE HDAL REGISTER
8067    022572  012737  001144  002346          MOV     #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD ;SETUP PREVIOUSLY LOADED BITS
8068
8069                                                  ;AT THE PRESENT TIME, MEMORY SIMULATOR DATA WHICH WAS READ FROM THE TEST
8070                                                  ;ADDRESS OF THE MEMORY SIMULATOR RAM EARLIER IN THIS TEST, IS NOW ENABLED
8071                                                  ;TO THE SYSTEM DATA BUS VIA THE TDAL DIAGNOSTIC LATCHES.  THIS DATA WAS
8072                                                  ;PRESENT ON THE EIDAL BUS IN THE LAST DATA CHECK ABOVE.  THE EIDAL BUS
8073                                                  ;IS ENABLED TO THE SYSTEM DATA BUS BY THE SIGNAL MSDO H BEING ASSERTED
8074                                                  ;HIGH.  THE PROGRAM WILL NOW WRITE THE DATA ON THE SYSTEM DATA BUS BACK
8075                                                  ;INTO THE TEST ADDRESS ON THE MEMORY SIUMULATOR RAM BY DOING A NORMAL T-11
8076                                                  ;TIMING CYCLE.  WHEN PRAS H IS SET HIGH, THE ADDRESS BUS WHICH CONTAINS
8077                                                  ;THE DIAGNOSTIC ADDRESS REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY
8078                                                  ;SIMULATOR SYSTEM ADDRESS BUS LATCHES.  WHEN XPI H IS SET HIGH IN THE
8079                                                  ;FOLLOWING TIMING SEQUENCE, THE DATA WILL BE WRITTEN INTO THE LOW BYTE
8080                                                  ;OF THE MEMORY SIMULATOR RAM ADDRESS.   THE WRITE SIGNALS FROM THE TARGET
8081                                                  ;EMULATOR MODULE TO THE MEMORY SIMULATOR MODULE ARE WT HB H AND WT LB H.
8082
8083    022600  004737  012300                  JSR     PC,XRASH                ;SET XRAS H AND PRAS H TO HIGH STATE
8084    022604  004737  012404                  JSR     PC,XCASH                ;SET XCAS H AND PCAS H TO HIGH STATE
8085    022610  004737  012510                  JSR     PC,XPIH                 ;SET XPI H AND PPI H TO HIGH STATE
8086    022614  004737  012436                  JSR     PC,XCASL                ;SET XCAS H AND PCAS H TO LOW STATE
8087    022620  004737  012542                  JSR     PC,XPIL                 ;SET XPI H AND PPIH TO LOW STATE
8088    022624  004737  012332                  JSR     PC,XRASL                ;SET XRAS H AND PRAS H TO LOW STATE
8089
8090                                                  ;READ VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A ONE
8091                                                  ;IN THE VDAL REGISTER AS A RESULT OF THE ABOVE T-11 TIMING SEQUENCE.
8092
8093    022630  052737  000020  002342          BIS     #VDAL4,T4GOOD           ;EXPECT EDEOC H TO BE SET TO A ONE
8094    022636  004737  011200                  JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
8095    022642  001405                          BEQ     29$                     ;IF OK THEN CONTINUE
8096    022644                                  ERRDF   11,VDALRG,T4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
8097    022644  104455                          TRAP    C$ERDF
8098    022646  000013                          .WORD   11
8099    022650  003710                          .WORD   VDALRG
8100    022652  006716                          .WORD   T4EROR
8101    022654                                  CKLOOP
8102    022654  104406                          TRAP    C$CLP1
8103
8104                                                  ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE ON CONTROL
8105                                                  ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8106
8107    022656  004737  011250          29$:    JSR     PC,SLCTMS               ;SELECT THE MEMORY SIMULATOR MODULE
8108
8109                                                  ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
8110                                                  ;TARGET EMULATOR MODULE PULSED THE SIGNAL ADVAL H BY TOGGLING THE
8111                                                  ;SIGNAL PRAS H.
8112
8113    022662  004737  010522                  JSR     PC,READS0               ;READ AND CHECK CONTROL REGISTER 0
8114    022666  001405                          BEQ     30$                     ;IF NO CHANGES THEN CONTINUE
8115    022670                                  ERRDF   1,,SOEROR                ;CONTROL REGISTER 0 NOT = EXPECTED
```

E 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 160
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0160

```
8116  022670  104455                          TRAP    C$ERDF
8117  022672  000001                          .WORD   1
8118  022674  000000                          .WORD   0
8119  022676  005306                          .WORD   SOEROR
8120  022700                                  CKLOOP
8121  022700  104406                          TRAP    C$CLP1
8122
8123                                  ;READ AND CHECK MSAD BITS 15:0 IN CONTROL REGISTER 4 TO SEE IF THE THE
8124                                  ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
8125                                  ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.  THE SIGNAL ADVAL H
8126                                  ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE TARGET EMULATORS
8127                                  ;SIGNAL PRAS H WAS SET TO A ONE AND THEN A ZERO.  THE MEMORY SIMULATORS
8128                                  ;SYSTEM ADDRESS BUS LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0
8129                                  ;BITS VIA THE SIGNALS CTS H AND CTS L.
8130
8131  022702  010137  002254  30$:   MOV     R1,S4LOAD              ;SETUP THE EXPECTED ADDRESS TO BE READ
8132  022706  004737  010614         JSR     PC,READS4             ;READ AND CHECK CONTROL REGISTER 4
8133  022712  001405                 BEQ     31$                   ;IF DATA = TE DIAG ADDRESS REG - CONT
8134  022714                         ERRDF   3,TEMSAD,SO4ERR       ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
8135  022714  104455                 TRAP    C$ERDF
8136  022716  000003                 .WORD   3
8137  022720  002534                 .WORD   TEMSAD
8138  022722  005406                 .WORD   SO4ERR
8139  022724                         CKLOOP
8140  022724  104406                 TRAP    C$CLP1
8141
8142                                  ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
8143                                  ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE, WHICH WAS
8144                                  ;ZEROES FOR THESE TWO ADDRESSES.  ADDRESS BITS 17 AND 16 WERE CLOCKED
8145                                  ;INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL
8146                                  ;ADVAL H.  THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET EMULATOR
8147                                  ;MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE AND THEN TO
8148                                  ;THE LOW STATE.  THE MEMORY SIMULATOR SYSTEM BUS ADDRESS LATCHES ARE
8149                                  ;ENABLED TO MSAD 17:0 BITS VIA THE SIGNALS CTS H AND CTS L ON THE
8150                                  ;MEMORY SIMULATOR MODULE.
8151
8152  022726  052737  000014  002250 31$:  BIS  #MSEL0!MSEL1,S2MASK  ;IGNORE TRI-STATED BITS WHEN CTS H SET
8153  022734  005037  002244         CLR     S2LOAD                ;EXPECT MSAD 17:16 TO BE ZERO
8154  022740  013737  002244  002246 MOV    S2LOAD,S2GOOD         ;COPY DATA LOADED TO EXPECTED
8155  022746  052737  000140  002246 BIS    #ESRH!WRENH,S2GOOD    ;EXPECT MAP PROTECT BITS TO BE ONES
8156  022754  004737  010562         JSR     PC,READS2            ;READ AND CHECK CONTROL REGISTER 2
8157  022760  001405                 BEQ     32$                   ;IF DATA OK THEN CONTINUE
8158  022762                         ERRDF   2,TEMSA1,SO2ERR       ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
8159  022762  104455                 TRAP    C$ERDF
8160  022764  000002                 .WORD   2
8161  022766  002410                 .WORD   TEMSA1
8162  022770  005366                 .WORD   SO2ERR
8163  022772                         CKLOOP
8164  022772  104406                 TRAP    C$CLP1
8165
8166                                  ;SET THE SIGNAL CTS H TO THE LOW STATE BY CLEARING THE BIT IN CONTROL
8167                                  ;REGISTER 0.  THIS WILL DISABLE THE SYSTEM BUS SIGNALS TO AND FROM
8168                                  ;THE MEMORY SIMULATOR MODULE.  THE MODULE WILL BE SET BACK TO 16 BIT DATA
8169                                  ;MODE BY CLEARING THE SIGNAL 8 BIT H IN CONTROL REGISTER 0.  THIS IS DONE
8170                                  ;TO CHECK THAT ONLY THE LOW BYTE OF THE DATA WAS WRITTEN INTO THE MEMORY
8171                                  ;SIMULATOR RAM IN 8 BIT MODE.
```

F 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 161
CVCDDB.P;1   14-JUN-82 09.54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0161

```
8172
8173   022774  112737  000004  002234   32$:   MOVB    #MPH,SOLOAD              ;CLEAR CTS H AND LEAVE MP H SET TO A 1
8174   023002  004737  010506                   JSR     PC,LDRDSO               ;LOAD, READ AND CHECK CONTROL REG 0
8175   023006  001405                           BEQ     33$                     ;IF LOADED OK THEN CONTINUE
8176   023010                                   ERRDF   1,,SOEROR               ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
8177   023010  104455                           TRAP    C$ERDF
8178   023012  000001                           .WORD   1
8179   023014  000000                           .WORD   0
8180   023016  005306                           .WORD   SOEROR
815·   023020                                   CKLOOP
8182   023020  104406                           TRAP    C$CLP1
8183
8184                                            ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
8185                                            ;LOADED PREVIOUSLY IS STILL LOADED
8186
3187   023022  004737  010614           33$:   JSR     PC,READS4               ;READ AND CHECK CONTROL REGISTER 4
8188   023026  001405                           BEQ     34$                     ;IF ADDRESS 0 THEN CONTINUE
8189   023030                                   ERRDF   3,MSADRG,S4EROR         ;MSAD 15:0 REG ERROR
8190   023030  104455                           TRAP    C$ERDF
8191   023032  000003                           .WORD   3
8192   023034  002510                           .WORD   MSADRG
8193   023036  005336                           .WORD   S4EROR
8194   023040                                   CKLOOP
8195   023040  104406                           TRAP    C$CLP1
8196
8197                                            ;READ CONTROL REGISTER 2 TO CHECK THAT THE DATA LOADED INTO IT PREVIOUSLY
8198                                            ;HAS NOT CHANGED.  THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
8199                                            ;MSAD16 H, MSAD17 H, MSELO L, MSEL1 L AND MSBRK H.  THE SIGNALS ESR H
8200                                            ;AND WREN H SHOULD BE READ AS ONES.
8201
8202   023042  012737  177400  002250   34$:   MOV     #177400,S2MASK          ;SETUP TO CHECK ALL OFF LOW BYTE
8203   023050  004737  010562                   JSR     PC,READS2               ;READ AND CHECK CONTROL REGISTER 2
8204   023054  001405                           BEQ     35$                     ;IF NO CHANGE THEN CONTINUE
8205   023056                                   ERRDF   2,,S2EROR               ;CONTROL REG 2 NOT EQUAL EXPECTED
8206   023056  104455                           TRAP    C$ERDF
8207   023060  000002                           .WORD   2
8208   023062  000000                           .WORD   0
8209   023064  005322                           .WORD   S2EROR
8210   023066                                   CKLOOP
8211   023066  104406                           TRAP    C$CLP1
8212
8213                                            ;READ CONTENTS OF THE MEMORY SIMULATOR RAM ADDRESS TO CHECK THAT THE LOW BYTE OF
8214                                            ;DATA INITIALLY LOADED INTO IT WAS WRITTEN BACK INTO IT FROM THE TARGET
8215                                            ;EMULATOR MODULE DURING A WRITE OPERATION. IN THE FIRST PART OF THIS
8216                                            ;TEST THE DATA WAS READ FROM THE MEMORY SIMULATOR RAM INTO THE TARGET
8217                                            ;EMULATOR AND SAVED IN THE TARGET EMULATORS TDAL DIAGNOSTIC LATCHES.
8218                                            ;THE PROGRAM THEN CLEARED THE DATA PATTERN WRITTEN INTO THE ADDRESS
8219                                            ;OF THE MEMORY SIMULATOR RAM.  THF PROGRAM THEN ENABLED THE TDAL DIAG-
8220                                            ;NOSTIC LATCHES TO THE TDAL BUS AND WROTE THE LOW BYTE OF DATA BACK INTO THE ADD
8221                                            ;OF THE MEMORY SIMULATOR RAM.  THE FOLLOWING CHECK WILL TEST THAT THIS
8222                                            ;HAPPENED CORRECTLY.
8223
8224   023070  005037  002260           35$:   CLR     S6LOAD                  ;CLEAR THE HIGH BYTE OF EXPECTED WORD
8225   023074  111237  002260                   MOVB    (R2),S6LOAD             ;GET INITIAL LOW BYTE OF MS RAM DATA
8226   023100  013737  002260  002262           MOV     S6LOAD,S6GOOD           ;COPY DATA FOR COMPARE IN SUBROUTINE
8227   023106  004737  010646                   JSR     PC,READS6               ;READ AND CHECK MS RAM DATA
```

G 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 162
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0162

```
8228   023112  061405                          BEQ     36$                     ;IF DATA OK THEN CONTINUE
8229   023114                                  ERRDF   4,MSGMSR,S6ALLR         ;DATA ERROR IN MEMORY SIMULATOR RAM
8230   023114  104455                          TRAP    C$ERDF
8231   023116  000004                          .WORD   4
8232   023120  002745                          .WORD   MSGMSR
8233   023122  005456                          .WORD   S6ALLR
8234   023124                                  CKLOOP
8235   023124  104406                          TRAP    C$CLP1
8236
8237                                           ;SET THE SIGNALS CTS H AND 8 BIT H TO ONES IN CONTROL REGISTER 0.  CTS H
8238                                           ;ON A ONE WILL ENABLE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR
8239                                           ;RAM.  8 BIT H ON A ONE WILL SET THE MODULE UP IN 8 BIT DATA MODE.
8240
8241   023126  052737  000012  002234  36$:    BIS     #CTSH!BIT8H,S0LOAD      ;SETUP BITS TO BE LOADED
8242   023134  004737  010506                  JSR     PC,LDRDS0              ;LOAD, READ AND CHECK CONTROL REG 0
8243   023140  001405                          BEQ     37$                     ;IF LOADED OK THEN CONTINUE
8244   023142                                  ERRDF   1,,S0EROR              ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
8245   023142  104455                          TRAP    C$ERDF
8246   023144  000001                          .WORD   1
8247   023146  000000                          .WORD   0
8248   023150  005306                          .WORD   S0EROR
8249   023152                                  CKLOOP
8250   023152  104406                          TRAP    C$CLP1
8251
8252                                           ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8253                                           ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8254
8255   023154  004737  012214          37$:    JSR     PC,SLCTTE             ;SELECT TARGET EMULATOR MODULE
8256
8257                                           ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO A
8258                                           ;0.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN ON A WRITE COMMAND
8259                                           ;TO CONTROL REGISTER 6.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE ENABLED
8260                                           ;TO THE ADDRESS BUS BY HDAL9 H BEING SET TO A ONE, WHICH IT IS.  ON A READ
8261                                           ;COMMAND TO CONTROL REGISTER 6, THE DIAGNOSTIC ADDRESS REGISTER WILL BE READ.
8262
8263   023160  004537  012234                  JSR     R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
8264   023164  000000                          .WORD   ADDRES                ;SELECT DIAG ADDRESS REG AND ADDRESS BUS
8265
8266                                           ;LOAD, READ AND CHECK THE DIAGNSOTIC ADDRESS REGISTER WITH ONE OF THE
8267                                           ;FOLLOWING ADDRESSES: 000001, 020001, 040001, OR 060001.
8268
8269   023166  010137  002346                  MOV     R1,T6LOAD             ;GET THE TEST ADDRESS
8270   023172  005237  002346                  INC     T6LOAD                ;MAKE THE ADDRESS ODD
8271   023176  004737  011216                  JSR     PC,LDRDT6             ;LOAD, READ AND CHECK DIAG ADDRESS REG
8272   023202  001405                          BEQ     38$                     ;IF LOADED OK THEN CONTINUE
8273   023204                                  ERRDF   12,ADDRRG,T06ERR       ;DIAG ADDRESS REG NOT EQUAL EXPECTED
8274   023204  104455                          TRAP    C$ERDF
8275   023206  000014                          .WORD   12
8276   023210  004144                          .WORD   ADDRRG
8277   023212  006732                          .WORD   T06ERR
8278   023214                                  CKLOOP
8279   023214  104406                          TRAP    C$CLP1
8280
8281                                           ;SLECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ COMMAND
8282                                           ;TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ BACK TO THE LSI-11.
8283
```

H 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 163
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0163

```
8284  023216  004537  012234      38$:    JSR     R5,SELTER                :SELECT REGISTER SPECIFIED BY NEXT WORD
8285  023222  000006                       .WORD   EIDAL                    :SELECT THE EIDAL BUS TO BE READ
8286
8287                                        ;AT THIS POINT IN TIME THE EIDAL BUS SHOULD HAVE THE TDAL DIAGNOSTIC
8288                                        ;LATCHES ENEBLED TO IT BY THE SIGNALS DBHB L AND DBLB L BEING ASSERTED
8289                                        ;LOW AND THE SIGNAL VDAL0 H BEING SET TO A ONE.  THE TDAL LATCHES WERE
8290                                        ;CLOCKED EARLIER IN THE TEST BY THE SIGNAL VDAL2 H.  THESE LATCHES WERE
8291                                        ;CLOCKED WITH THE DATA FROM THE MEMORY SIMULATOR RAM DURING A READ
8292                                        ;OPERATION FROM THE MEMORY SIMULATOR RAM'S TEST ADDRESS.
8293
8294  023224  011237  002346              MOV     (R2),T6LOAD              :GET 1ST DATA WRITTEN TO MS RAM
8295  023230  004737  011224              JSR     PC,READT6                :READ AND CHECK EIDAL BUS
8296  023234  001405                       BEQ     39$                      :IF DATA OK THEN CONTINUE
8297  023236                               ERRDF   12,MSTETD,T6ALLR         :MS RAM DATA TO EIDAL BUS VIA TDAL BUS
8298  023236  104455                       TRAP    C$ERDF
8299  023240  000014                       .WORD   12
8300  023242  004422                       .WORD   MSTETD
8301  023244  006746                       .WORD   T6ALLR
8302  023246                               CKLOOP
8303  023246  104406                       TRAP    C$CLP1
8304
8305                                        ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
8306                                        ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
8307                                        ;REGISTER 6.
8308
8309  023250  004537  012234      39$:    JSR     R5,SELTER                :SELECT REGISTER SPECIFIED BY NEXT WORD
8310  023254  000003                       .WORD   HDAL                     :SELECT THE HDAL REGISTER
8311  023256  012737  001144  002346       MOV     #HDAL9!HDAL6!HDAL5!HDAL2,T6LOAD ;SETUP BITS PREVIOUSLY LOADED
8312
8313                                        ;AT THE PRESENT TIME, MEMORY SIMULATOR DATA WHICH WAS READ FROM THE TEST
8314                                        ;ADDRESS EARLIER IN THIS TEST, IS NOW ENABLED TO THE SYSTEM DATA BUS VIA
8315                                        ;THE TDAL DIAGNOSTIC LATCHES.  THIS DATA WAS PRESENT ON THE EIDAL BUS IN
8316                                        ;THE LAST DATA CHECK ABOVE.  THE EIDAL BUS IS ENABLED TO SYSTEM DATA BUS
8317                                        ;BY THE SIGNAL MSDO H BEING ASSERTED HIGH.  THE PROGRAM WILL NOW WRITE THE
8318                                        ;LOW BYTE OF THE SYSTEM BUS DATA INTO THE HIGH BYTE OF THE MEMORY SIMULATOR
8319                                        ;RAM ADDRESSED.  THIS IS DONE BY DOING A NORMAL T-11 TIMING CYCLE.  WHEN
8320                                        ;PRAS H IS SET HIGH, THE ADDRESS BUS, WHICH CONTAINS THE DIAGNOSTIC ADDRESS
8321                                        ;REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS
8322                                        ;BUS LATCHES.  WHEN XPI H IS SET HIGH, THE LOW BYTE OF DATA WILL BE
8323                                        ;WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM ADDRESSED.  THE
8324                                        ;WRITE SIGNALS FROM THE TARGET EMULATOR MODULE TO THE MEMORY SIMULATOR
8325                                        ;MODULE ARE WT HB H AND WT LB H.
8326
8327  023264  004737  012300              JSR     PC,XRASH                 :SET XRAS H AND PRAS H TO HIGH STATE
8328  023270  004737  012404              JSR     PC,XCASH                 :SET XCAS H AND PCAS H TO HIGH STATE
8329  023274  004737  012510              JSR     PC,XPIH                  :SET XPI H AND PPI H TO HIGH STATE
8330  023300  004737  012436              JSR     PC,XCASL                 :SET XCAS H AND PCAS H TO LOW STATE
8331  023304  004737  012542              JSR     PC,XPIL                  :SET XPI H AND PPI H TO LOW STATE
8332  023310  004737  012332              JSR     PC,XRASL                 :SET XRAS H AND PRAS H TO LOW STATE
8333
8334                                        ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A
8335                                        ;ONE AS A RESULT OF THE ABOVE TIMING SEQUENCE.
8336
8337  023314  052737  000020  002342       BIS     #VDAL4,T4GOOD            :EXPECT EDEOC H TO BE SET TO A ONE
8338  023322  004737  011200              JSR     PC,READT4                :READ AND CHECK VDAL REGISTER
8339  023326  001405                       BEQ     40$                      :IF OK THEN CONTINUE
```

I 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 164
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0164

```
8340   023330                                   ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
8341   023330   104455                          TRAP    C$ERDF
8342   023332   000013                          .WORD   11
8343   023334   003710                          .WORD   VDALRG
8344   023336   006716                          .WORD   T4EROR
8345   023340                                   CKLOOP
8346   023340   104406                          TRAP    C$CLP1
8347

8348                                            ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8349                                            ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8350

8351   023342   004737  011250        40$:      JSR     PC,SLCTMS               ;SELECT THE MEMORY SIMULATOR MODULE
8352

8353                                            ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED WHEN THE
8354                                            ;TARGET EMULATOR MODULE PERFORMED A NORMAL T-11 TIMING CYCLE.
8355

8356   023346   004737  010522                  JSR     PC,READS0               ;READ AND CHECK CONTROL REGISTER 0
8357   023352   001405                          BEQ     41$                     ;IF NO CHANGES THEN CONTINUE
8358   023354                                   ERRDF   1,,S0EROR               ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
8359   023354   104455                          TRAP    C$ERDF
8360   023356   000001                          .WORD   1
8361   023360   000000                          .WORD   0
8362   023362   005306                          .WORD   S0EROR
8363   023364                                   CKLOOP
8364   023364   104406                          TRAP    C$CLP1
8365

8366                                            ;READ AND CHECK MSAD BITS 15:0 IN CONTROLR REGISTER 4 TO SEE IF THE
8367                                            ;SYSTEM ADDRESS BUS BITS 15:0 WERE CLOCKED INTO THE MEMORY SIMULATOR
8368                                            ;SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.   THE SIGNAL ADVAL H
8369                                            ;WAS GENERATED ON THE TARGET EMULATOR MODULE WHEN THE SIGNAL PRAS H WAS
8370                                            ;SET TO A ONE FROM A ZERO.   THE MEMORY SIMULATOR SYSTEM ADDRESS BUS
8371                                            ;LATCHES ARE ENABLED TO MEMORY SIMULATOR MSAD 17:0 BITS VIA THE SIGNALS
8372                                            ;CTS H AND CTS L.
8373

8374   023366   010137  002254        41$:      MOV     R1,S4LOAD               ;GET THE EVEN TEST ADDRESS
8375   023372   005237  002254                  INC     S4LOAD                  ;MAKE THE ADDRESS ODD
8376   023376   004737  010614                  JSR     PC,READS4               ;READ AND CHECK MSAD BITS 15:0
8377   023402   001405                          BEQ     42$                     ;IF OK THEN CONTINUE
8378   023404                                   ERRDF   3,TEMSAD,S04ERR         ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
8379   023404   104455                          TRAP    C$ERDF
8380   023406   000003                          .WORD   3
8381   023410   002534                          .WORD   TEMSAD
8382   023412   005406                          .WORD   S04ERR
8383   023414                                   CKLOOP
8384   023414   104406                          TRAP    C$CLP1
8385

8386                                            ;READ AND CHECK MSAD BITS 17:16 IN CONTROL REGISTER 2 TO SEE IF THEY
8387                                            ;ARE THE SAME AS THAT LOADED ON THE TARGET EMULATOR MODULE.  ADDRESS BITS
8388                                            ;17 AND 16 WERE CLOCKED INTO MEMORY SIMULATOR ADDRESS BUS LATCHES VIA
8389                                            ;THE SIGNAL ADVAL H.   THE SIGNAL ADVAL H WAS GENERATED ON THE TARGET
8390                                            ;EMULATOR MODULE WHEN THE PROGRAM SET THE SIGNAL PRAS H TO THE HIGH STATE
8391                                            ;AND THEN TO THE LOW STATE.    THE MEMORY SIMULATOR SYSTEM BUS LATCHES
8392                                            ;ARE ENABLED TO MSAD BITS 17:0 VIA THE SIGNALS CTS H AND CTS L ON THE
8393                                            ;MEMORY SIMULATOR MODULE.
8394

8395   023416   052737  000014  002250  42$:    BIS     #MSEL1!MSEL0,S2MASK     ;IGNORE TRI-STATED BITS WHEN CTS H SET
```

J 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 165
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0165

```
8396   023424   005037   002244            CLR     S2LOAD                    ;EXPECT MSAD BITS 17 + 16 TO BE 0
8397   023430   013737   002244   002246   MOV     S2LOAD,S2GOOD             ;COPY DATA FOR DATA COMPARE
8398   023436   052737   000140   002246   BIS     #ESRH!WRENH,S2GOOD        ;EXPECT MAP PROTECT BITS TO BE ONES
8399   023444   004737   010562            JSR     PC,READS2                 ;READ AND CHECK CONTROL REGISTER 2
8400   023450   001405                     BEQ     43$                       ;IF DATA OK THEN CONTINUE
8401   023452                              ERRDF   2,TEMSA1,S02ERR           ;TE TO MS ADDRESS BUS ERROR - MSAD 17:16
8402   023452   104455                     TRAP    C$ERDF
8403   023454   000002                     .WORD   2
8404   023456   002410                     .WORD   TEMSA1
8405   023460   005366                     .WORD   S02ERR
8406   023462                              CKLOOP
8407   023462   104406                     TRAP    C$CLP1
8408
8409                                       ;SET THE SIGNALS CTS H AND 8 BIT H TO THE LOW STATES BY CLEARING THESE
8410                                       ;BITS IN CONTROL REGISTER 0.  CTS H ON A ZERO WILL DISABLE THE SYSTEM
8411                                       ;BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR MODULE.  WHEN 8 BIT H IS
8412                                       ;SET TO A ZERO, THE MEMORY SIMULATOR MODULE WILL BE SETUP TO 16 BIT DATA
8413                                       ;MODE.  THIS IS DONE TO CHECK THAT THE LOW BYTE OF DATA ON THE SYSTEM
8414                                       ;BUS WAS WRITTEN INTO THE HIGH BYTE OF THE MEMORY SIMULATOR RAM LOCATION
8415
8416   023464   112737   000004   002234  43$:  MOVB  #MPH,S0LOAD            ;CLEAR CTS H AND 8 BIT H
8417   023472   004737   010506            JSR     PC,LDRDS0                 ;LOAD, READ AND CHECK CONTROL REG 0
8418   023476   001405                     BEQ     44$                       ;IF LOADED OK THEN CONTINUE
8419   023500                              ERRDF   1,,S0EROR                 ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
8420   023500   104455                     TRAP    C$ERDF
8421   023502   000001                     .WORD   1
8422   023504   000000                     .WORD   0
8423   023506   005306                     .WORD   S0EROR
8424   023510                              CKLOOP
8425   023510   104406                     TRAP    C$CLP1
8426
8427                                       ;READ CONTROL REGISTER 4 TO CHECK THAT THE MEMORY SIMULATOR ADDRESS
8428                                       ;LOADED PREVIOUSLY HAS NOT CHANGED.  THIS ADDRESS SHOULD BE EVEN.
8429
8430   023512   010137   002254           44$:  MOV   R1,S4LOAD             ;GET THE ADDRESS BEING TESTED
8431   023516   004737   010614            JSR     PC,READS4                 ;READ AND CHECK MSAD BITS 15:0
8432   023522   001405                     BEQ     45$                       ;IF ADDRESS OK THEN CONTINUE
8433   023524                              ERRDF   3,MSADRG,S4EROR           ;MSAD 15:0 REGISTER ERROR
8434   023524   104455                     TRAP    C$ERDF
8435   023526   000003                     .WORD   3
8436   023530   002510                     .WORD   MSADRG
8437   023532   005336                     .WORD   S4EROR
8438   023534                              CKLOOP
8439   023534   104406                     TRAP    C$CLP1
8440
8441                                       ;READ CONTROL REGISTER 2 TO CHECK THAT THE DATA LOADED INTO IT BEFORE
8442                                       ;HAS NOT CHANGED.  THE FOLLOWING SIGNALS SHOULD BE READ AS ZEROES:
8443                                       ;MSAD16 H, MSAD17 H, MSEL0 L, MSEL1 L AND MSBRK H.  THE SIGNALS ESR H
8444                                       ;WREN H SHOULD BE READ AS ONES.
8445
8446   023536   012737   177400   002250  45$:  MOV   #177400,S2MASK        ;SETUP TO CHECK ALL OF LOW BYTE
8447   023544   004737   010562            JSR     PC,READS2                 ;READ AND CHECK CONTROL REGISTER 2
8448   023550   001405                     BEQ     46$                       ;IF OK THEN CONTINUE
8449   023552                              ERRDF   2,,S2EROR                 ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
8450   023552   104455                     TRAP    C$ERDF
8451   023554   000002                     .WORD   2
```

K 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 166
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0166

```
8452   023556   000000                              .WORD    0
8453   023560   005322                              .WORD    S2EROR
8454   023562                              CKLOOP
8455   023562   104406                              TRAP     C$CLP1
8456
8457                                       ;READ CONTENTS OF MEMORY SIMULATOR RAM ADDRESS TO CHECK THAT THE LOW
8458                                       ;BYTE OF DATA INITIALLY LOADED INTO IT WAS WRITTEN BACK INTO THE HIGH
8459                                       ;BYTE OF THE LOCATION FROM THE TARGET EMULATOR MODULE DURING A WRITE
8460                                       ;OPERATION.  IN THE FIRST PART OF THE TEST, THE DATA WAS READ FROM THE
8461                                       ;MEMORY SIMULATOR RAM INTO THE TARGET EMULATOR DIAGNOSTIC TDAL LATCHES
8462                                       ;AND SAVED IN THESE LATCHES.  THE PROGRAM THEN CLEARED THIS MEMORY
8463                                       ;SIMULATOR RAM LOCATION AND WROTE THE LOW BYTE OF THE LOCATION WITH DATA
8464                                       ;FROM THE TARGET EMULATORS TDAL LATCHES VIA THE DATA BUS.  THE LAST
8465                                       ;PORTION OF THIS TEST WILL CAUSE THE HIGH BYTE OF THE MEMORY SIMULATOR
8466                                       ;RAM TO BE WRITTEN WITH THE LOW BYTE OF DATA FROM THE TARGET EMULATOR'S
8467                                       ;TDAL LATCHES VIA THE DATA BUS.
8468
8469   023564   011237   002260    46$:    MOV      (R2),S6LOAD         ;GET INITIAL DATA PATTERN
8470   023570   111237   002261            MOVB     (R2),S6LOAD+1       ;COPY LOW BYTE TO HIGH BYTE
8471   023574   013737   002260  002262    MOV      S6LOAD,S6GOOD       ;COPY DATA FOR DATA COMPARE
8472   023602   004737   010646            JSR      PC,READS6           ;READ AND CHECK MS RAM DATA
8473   023606   001404                      BEQ      47$                 ;IF DATA OK THEN HIGH BYTE WRITTEN OK
8474   023610                               ERRDF    4,MSGMSR,S6ALLR     ;DATA ERROR IN MEMORY SIMULATOR RAM
8475   023610   104455                      TRAP     C$ERDF
8476   023612   000004                      .WORD    4
8477   023614   002745                      .WORD    MSGMSR
8478   023616   005456                      .WORD    S6ALLR
8479   023620                      47$:    ENDSEG
8480   023620                      10000$:
8481   023620   104405                      TRAP     C$ESEG
8482
8483   023622   005722                      TST      (R2)+               ;UPDATE THE DATA TABLE POINTER
8484   023624   062701   020000            ADD      #MSAD13,R1          ;UPDATE ADDRESS TO NEXT MS RAM BANK
8485   023630   100402                      BMI      48$                 ;IF DONE EACH BANK OF MEMORY - EXIT
8486   023632   000137   021164            JMP      1$                  ;GO DO TWO PATTERNS WITH THIS ADDRESS
8487
8488                                       ;TO CHECK THAT ADDRESS 0 OF EACH 4K BANK OF MEMORY SIMULATOR RAM WAS
8489                                       ;SELECTED AND WRITTEN CORRECTLY, THE PROGRAM WILL READ THE FIRST ADDRESS
8490                                       ;OF EACH 4K BANK OF MEMORY SIMULATOR RAM.  THE DATA WILL BE DIFFERENT
8491                                       ;THEN THAT WHICH WAS WRITTEN INTO IT INITIALLY.  WHEN THE MEMORY SIMULATOR
8492                                       ;RAM WAS SETUP TO 8 BIT MODE AND DATA WAS WRITTEN INTO IT FROM THE TARGET
8493                                       ;EMULATOR MODULE, THE LOW BYTE OF THE INITIAL DATA PATTERN WILL BE WRITTEN
8494                                       ;INTO THE LOW BYTE OF THE ADDRESS WHEN THE ADDRESS IS EVEN AND THE LOW
8495                                       ;BYTE OF THE INITIAL DATA PATTERN WILL BE WRITTEN INTO THE HIGH BYTE OF
8496                                       ;THE ADDRESS WHEN THE ADDRESS IS ODD.  THE ADDRESSES LOADED INITIALLY
8497                                       ;AND THE EXPECTED DATA PATTERNS TO BE IN THE ADDRESSES NOW ARE LISTED BELOW:
8498                                       ;    ADDRESS 000000 WAS 052652 NOW SHOULD BE 125252
8499                                       ;    ADDRESS 020000 WAS 146063 NOW SHOULD BE 031463
8500                                       ;    ADDRESS 040000 WAS 000377 NOW SHOULD BE 177777
8501                                       ;    ADDRESS 060000 WAS 125125 NOW SHOULD BE 052525
8502
8503   023636   005001                      48$:    CLR      R1                  ;SETUP STARTING ADDRESS TO BE 0
8504   023640   012702   023740             MOV      #52$,R2             ;SETUP ADDRESS OF DATA TABLE
8505
8506                                       ;LOAD, READ AND CHECK CONTROL REGISTER 4 WITH THE ADDRESS OF THE LOCATION
8507                                       ;TO BE CHECKED.  THE ADDRESSES TO BE LOADED ARE 0, 20000, 40000, AND 60000.
```

L 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 167
CVCDDB.P11   14-JUN-82 09:54   TEST 6: READ MS DATA TO TE - WRITE DATA TO MS VIA TE - 8 BIT MODE   SEQ 0167

```
8508
8509   023644   010137   002254        49$:    MOV     R1,S4LOAD          ;GET THE ADDRESS TO BE LOADED
8510   023650   004737   010606                JSR     PC,LDRDS4          ;LOAD, READ AND CHECK CONTROL REGISTER 4
8511   023654   001405                         BEQ     50$                ;IF LOADED OK THEN CONTINUE
8512   023656                                  ERRDF   3,MSADRG,S4EROR    ;MSAD 15:0 REGISTER ERROR
8513   023656   104455                         TRAP    C$ERDF
8514   023660   000003                         .WORD   3
8515   023662   002510                         .WORD   MSADRG
8516   023664   005336                         .WORD   S4EROR
8517   023666                                  CKLOOP
8518   023666   104406                         TRAP    C$CLP1
8519
8520                                           ;EARLIER IN THIS TEST, CONTROL REGISTER 2 BITS MSAD16 H, MSAD17 H, MSEL1 L,
8521                                           ;AND MSEL0 L WERE WRITTEN TO ZEROES.  WHEN A READ COMMAND IS ISSUED TO
8522                                           ;CONTROL REGISTER 6 AND THE SIGNALS MSEL1 L AND MSEL0 L ARE ASSERTED LOW,
8523                                           ;A PULSE WILL BE ISSUED ON THE SIGNAL SSM L.  THIS SIGNAL ALONG WITH THE
8524                                           ;READ COMMAND, WILL READ THE DATA FROM THE MEMORY SIMULATOR RAM ADDRESSED
8525                                           ;BY CONTROL REGISTER 2 AND 4 BITS.
8526
8527   023670   011237   002260        50$:    MOV     (R2),S6LOAD        ;GET THE DATA FROM THE TABLE
8528   023674   111237   002261                MOVB    (R2),S6LOAD+1      ;COPY LOW BYTE TO HIGH BYTE
8529   023700   013737   002260   002262       MOV     S6LOAD,S6GOOD      ;SETUP EXPECTED DATA
8530   023706   004737   010646                JSR     PC,READS6          ;READ AND CHECK MEMORY SIM RAM DATA
8531   023712   001405                         BEQ     51$                ;IF DATA OK THEN CONTINUE
8532   023714                                  ERRDF   4,MSGMSR,S6ALLR    ;DATA ERROR IN MEMORY SIMULATOR RAM
8533   023714   104455                         TRAP    C$ERDF
8534   023716   000004                         .WORD   4
8535   023720   002745                         .WORD   MSGMSR
8536   023722   005456                         .WORD   S6ALLR
8537   023724                                  CKLOOP
8538   023724   104406                         TRAP    C$CLP1
8539
8540   023726   005722                51$:    TST     (R2)+              ;UPDATE POINTER TO DATA TABLE
8541   023730   062701   020000                ADD     #MSAD13,R1         ;UPDATE THE ADDRESS TO NEXT 4K MEMORY
8542   023734   100343                         BPL     49$                ;IF NOT DONE CHECK THIS 4K MEMORY BANK
8543   023736   000404                         BR      53$                ;EXIT THE TEST
8544
8545   023740   052652                52$:    .WORD   052652             ;ADDRESS 000000 DATA PATTERN
8546   023742   146063                         .WORD   146063             ;ADDRESS 020000 DATA PATTERN
8547   023744   000377                         .WORD   000377             ;ADDRESS 040000 DATA PATTERN
8548   023746   125125                         .WORD   125125             ;ADDRESS 060000 DATA PATTERN
8549
8550   023750                         53$:    ENDTST
8551   023750                         L10042:
8552   023750   104401                         TRAP    C$ETST
8553
8554
8555
8556
```

M 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 168
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0168

```
8557                                    .SBTTL  TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED
8558
8559                            ;++
8560                            ;       THIS TEST WILL CHECK THAT TARGET EMULATOR SIGNALS XSEL1 H, EDSEL0 H,
8561                            ;       ADDR17 H, ADDR16 H, BTS3 H, BTS2 H, BTS1 H AND BTS0 H CAN BE ENABLED
8562                            ;       TO THE SYSTEM BUS AS SIGNALS CTL 11:8 H AND OBTS 3:0 H RESPECTIVELY,
8563                            ;       AND THAT THESE SIGNALS CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM
8564                            ;       BUS LATCHES FOR THESE BITS VIA THE TARGET EMULATOR'S SYSTEM BUS CLOCKING
8565                            ;       SIGNAL 'ENCK4 H'.   THE PROGRAM WILL CHECK THAT THESE BITS ARE CLOCKED
8566                            ;       INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES BY READING THESE LATCHES
8567                            ;       ON THE STATE ANALYZERS TRDI BUS BITS 39:32.   THE TARGET EMULATOR SIGNALS
8568                            ;       "ADDR17 H" AND "ADDR16 H" HAVE BEEN CHECKED IN PREVIOUS TEST, THEREFORE,
8569                            ;       THESE SIGNALS WILL ONLY BE CHECKED FOR ZEROES IN THIS TEST.   THE PROGRAM
8570                            ;       WILL SET THE SIGNALS XSEL1 H, EDSEL0 H AND BTS BITS 3:0 H TO ONES AND
8571                            ;       ZEROES BY MANIPULATING THE ASSOCIATED LOGIC.   THE TEST WILL THEN CLOCK
8572                            ;       THE CORRESPONDING SYSTEM BUS SIGNALS INTO THE STATE ANALYZER SYSTEM BUS
8573                            ;       LATCHES AND CHECK THAT THE SYSTEM BUS LATCHES CONTAIN THE CORRECT DATA
8574                            ;       PATTERN.   THE PROGRAM WILL ALSO CHECK THAT THE TARGET EMULATOR SYSTEM
8575                            ;       BUS CLOCKING SIGNAL 'ENCK4 H' CAN BE GENERATED IN DIFFERENT WAYS.
8576                            ;--
8577
8578    023752                          BGNTST
8579    023752                  T7::
8580    023752   004737  007440         JSR     PC,INITMD               ;INITIALIZE MDE/T-11 SYSTEM MODULES
8581    023756                          BGNSEG
8582    023756   104404                 TRAP    C$BSEG
8583    023760   005037  002320         CLR     E6MASK                  ;CLEAR REGISTER 6 MASK WORD FOR LOOPING
8584
8585                            ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8586                            ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8587
8588    023764   004737  012214         JSR     PC,SLCTTE               ;SELECT TARGET EMULATOR MODULE
8589
8590                            ;SET ADAL REGISTER BITS 14, 10, 9, 7, AND 4 TO A ONE AND PULSE THE
8591                            ;SIGNAL 'BRKRES L' BY SETTING AND CLEARING ADAL REGISTER BIT 0.
8592                            ;   ADAL14H = 1            ALLOWS RASP L TO PULSE CKAI H WHEN XRAS H PULSED
8593                            ;   ADAL10H = 1            ENABLES TE SIGNALS TO MDE/T-11 SYSTEM BUS
8594                            ;   ADAL9H  = 1            WHEN ADAL10H = 1 ENABLES EDCK 5:0 SIGNALS TO BUS
8595                            ;   ADAL7H  = 1            ALLOWS 'REFR' FLIP-FLOP TO BE CLOCKED VIA XRAS H
8596                            ;   ADAL4H  = 1            SETS PAUSE MODE F/F TO RUN MODE WHEN CLOCKED BY XRAS H
8597
8598    023770   012737  043220  002334 MOV     #ADAL14!ADAL10!ADAL9!ADAL7!ADAL4,T2LOAD  ;SETUP BITS TO BE LOADED
8599    023776   004737  012766         JSR     PC,BRKRES               ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
8600
8601                            ;SELECT THE HDAL REG BY SETTING GDAL BITS 2:0 TO A 3.   THE HDAL REG
8602                            ;WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REG 6.
8603
8604    024002   004537  012234         JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
8605    024006   000003                 .WORD   HDAL                    ;SELECT THE HDAL REGISTER
8606
8607                            ;SET HDAL REGISTER BITS TO THE FOLLOWING BIT SETTINGS:
8608                            ;   HDAL14H = 0           ;SETS ADDR17 H TO LOW STATE (0)
8609                            ;   HDAL11H = 0           ;SETS ADDR16 H TO LOW STATE (0)
8610                            ;   HDAL9H  = 1           ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
8611                            ;   HDAL6H  = 0           ;SETS XSEL1 L TO HIGH STATE
8612                            ;   HDAL5H  = 1           ;SETS XSEL0 L TO LOW STATE
```

N 13

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 169
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0169

```
8613                                            ;   HDAL4H  = 0              ;SET XR/WHB L TO HIGH STATE
8614                                            ;   HDAL3H  = 1              ;SET XR/WLB L TO LOW STATE
8615                                            ;   HDAL2H  = 1              ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
8616
8617    024010  012737  001054  002346          MOV      #HDAL9!HDAL5!HDAL3!HDAL2,T6LOAD  ;SET HDAL BITS 9,5,3 + 2 TO ONES
8618    024016  004737  011216                  JSR      PC,LDRDT6                ;GO LOAD, READ AND CHECK HDAL REGISTER
8619    024022  001405                           BEQ      1$                      ;IF LOADED OK THEN CONTINUE
8620    024024                                   ERRDF    12,HDALRG,T06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
8621    024024  104455                           TRAP     C$ERDF
8622    024026  000014                           .WORD    12
8623    024030  003756                           .WORD    HDALRG
8624    024032  006732                           .WORD    T06ERR
8625    024034                                   CKLOOP
8626    024034  104406                           TRAP     C$CLP1
8627
8628                                            ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
8629                                            ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
8630                                            ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
8631
8632    024036  005037  002340          1$:     CLR      T4LOAD                   ;SETUP TO CLEAR ALL OTHER R/W BITS
8633    024042  004737  012706                  JSR      PC,CLRPSM                ;PULSE INVD L VIA VDAL2 H
8634
8635                                            ;SELECT MODE REG BY SETTING GDAL REG BITS 2:0 TO A 4.  ON A WRITE OR READ
8636                                            ;COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL BE WRITTEN OR READ.
8637
8638    024046  004537  012234                  JSR      R5,SELTER                ;SELECT REGISTER SPECIFIED BY NEXT WORD
8639    024052  000004                           .WORD    MODE                     ;SELECT THE MODE REGISTER
8640
8641                                            ;LOAD, READ AND CHECK THE MODE REGISTER WITH BIT 11 SET TO A ONE AND
8642                                            ;ALL OTHER READ/WRITE BITS CLEARED.  THIS WILL SET THE TARGET EMUALTOR
8643                                            ;MODULE TO 8 BIT ADDRESSING MODE.
8644
8645    024054  012737  004000  002346          MOV      #MR11,T6LOAD             ;SETUP BIT TO SET MR1i H TO HIGH STATE
8646    024062  004737  011216                  JSR      PC,LDRDT6                ;GO LOAD, READ AND CHECK MODE REGISTER
8647    024066  001405                           BEQ      2$                      ;IF LOADED OK THEN CONTINUE
8648    024070                                   ERRDF    12,MODREG,T06ERR        ;MODE REGISTER NOT EQUAL EXPECTED
8649    024070  104455                           TRAP     C$ERDF
8650    024072  000014                           .WORD    12
8651    024074  004002                           .WORD    MODREG
8652    024076  006732                           .WORD    T06ERR
8653    024100                                   CKLOOP
8654    024100  104406                           TRAP     C$CLP1
8655
8656                                            ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
8657                                            ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
8658                                            ;READ COMMAND TO CONTROL REGISTER 6..  THE EOAI REGISTER NEEDS FDAL0 H
8659                                            ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
8660                                            ;TER WILL BE ADDRESSED.
8661
8662    024102  004537  012234          2$:     JSR      R5,SELTER                ;SELECT REGISTER SPECIFIED BY NEXT WORD
8663    024106  000002                           .WORD    FDAL                     ;SELECT EOAI AND FDAL REGISTER
8664
8665                                            ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER.  THE EOAI REGISTER WILL
8666                                            ;BE LOADED AND CHECKED FOR ZEROES.  THE FDAL REGISTER WILL BE LOADED AND
8667                                            ;CHECKED FOR A DATA PATTERN OF ONE (FDAL0 H = 1).
8668
```

B 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 170
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0170

```
8669   024110  012737  000001  002346        MOV      #FDALO,T6LOAD            ;SETUP EOAI AND FDAL REG DATA PATTERN
8670   024116  004737  011216                JSR      PC,LDRDT6               ;GO LOAD, READ AND CHECK EOAI + FDAL REG
8671   024122  001405                         BEQ      3$                      ;IF LOADED OK THEN CONTINUE
8672   024124                                 ERRDF    12,EOAIFD,T06ERR        ;EOAI OR FDAL REGISTER ERROR
8673   024124  104455                         TRAP     C$ERDF
8674   024126  000014                         .WORD    12
8675   024130  004047                         .WORD    EOAIFD
8676   024132  006732                         .WORD    T06ERR
8677   024134                                 CKLOOP
8678   024134  104406                         TRAP     C$CLP1
8679
8680                                           ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO A 0.
8681                                           ;THE DIAGNOSTIC ADDRESS REGISTER WILL BE WRITTEN ON A WRITE COMMAND TO
8682                                           ;CONTROL REGISTER 6.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE ENABLED TO
8683                                           ;THE SYSTEM ADDRESS BUS VIA THE SIGNAL HDAL9 H.  ON A READ COMMAND TO
8684                                           ;CONTROL REGISTER 6, THE SYTEM ADDRESS BUS WILL BE READ.
8685
8686   024136  004537  012234        3$:      JSR      R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
8687   024142  000000                         .WORD    ADDRES                  ;SELECT THE DIAGNOSTC ADDRESS REGISTER
8688
8689                                           ;LOAD READ AND CHECK DIAGNOSTIC ADDRESS REG WITH A DATA PATTERN OF 0'S
8690
8691   024144  005037  002346                CLR      T6LOAD                  ;SETUP DATA PATTERN OF ALL ZEORES
8692   024150  004737  011216                JSR      PC,LDRDT6               ;LOAD, READ AND CHECK DIAG ADDRESS REG
8693   024154  001405                         BEQ      4$                      ;IF LOADED OK THEN CONTINUE
8694   024156                                 ERRDF    12,ADDRRG,T06ERR        ;DIAG ADDRESS REG NOT EQUAL TO ZERO
8695   024156  104455                         TRAP     C$ERDF
8696   024160  000014                         .WORD    12
8697   024162  004144                         .WORD    ADDRRG
8698   024164  006732                         .WORD    T06ERR
8699   024166                                 CKLOOP
8700   024166  104406                         TRAP     C$CLP1
8701
8702                                           ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE
8703                                           ;IN CONTROL REGISTER 4.
8704
8705   024170  012737  000200  002340 4$:     MOV      #VDAL7,T4LOAD           ;SETUP BIT TO SET FETCT H TO HIGH STATE
8706   024176  004737  011164                JSR      PC,LDRDT4               ;LOAD, READ AND CHECK VDAL REGISTER
8707   024202  001405                         BEQ      5$                      ;IF LOADED OK THEN CONTINUE
8708   024204                                 ERRDF    11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
8709   024204  104455                         TRAP     C$ERDF
8710   024206  000013                         .WORD    11
8711   024210  003710                         .WORD    VDALRG
8712   024212  006716                         .WORD    T4EROR
8713   024214                                 CKLOOP
8714   024214  104406                         TRAP     C$CLP1
8715
8716                                           ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
8717                                           ;REG WILL BE WRITTEN AND READ ON A WRITE AND READ COMMAND TO CONTROL REG 6
8718
8719   024216  004537  012234        5$:      JSR      R5,SELTER               ;SELECT REG SPECIFIED BY THE NEXT WORD
8720   024222  000003                         .WORD    HDAL                    ;SELECT THE HDAL REGISTER
8721
8722                                           ;TOGGLE THE SIGNAL XRAS H AND XRAS L BY SETTING AND CLEARING HDAL REGISTER
8723                                           ;BIT 12.  WHEN XRAS H IS SET HIGH FROM BEING ASSERTED LOW, THE FOLLOWING
8724                                           ;FLIP-FLOPS WILL BE SET AS LISTED.
```

C 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 171
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0171

```
8725                                          ;  PAUSE  F/F = 1 THUS SETTING PAUSE L TO LOW STATE
8726                                          ;  ENCLK  F/F = 1 THUS SETTING ENCLK H TO HIGH STATE
8727                                          ;  EDFET  F/F = 1 THUS SETTING EDFET H TO HIGH STATE
8728                                          ;  BTFET  F/F = 1 THUS SETTING BTFET L TO LOW STATE
8729                                          ;  EDSEL0 F/F = 0 THUS SETTING EDSEL0 H TO HIGH STATE
8730                                          ;  REFR   F/F = 1 THUS SETTING REFR H  TO HIGH STATE
8731                                          ;  ENEDC  F/F = 1 THUS SETTING ENEDC H TO HIGH STATE
8732                                          ;WHEN XRAS L IS RETURNED TO THE HIGH STATE AFTER HAVING BEEN ASSERTED
8733                                          ;LOW, THE SIGNAL REFP L WILL BE ASSERTED LOW AS A RESULT OF THE REFR
8734                                          ;FLIP-FLOP BEING SET TO A ONE.  WHEN THE SIGNAL REFP L IS SET LOW, THE
8735                                          ;SIGNAL EDCK4 H WILL BE SET TO THE HIGH STATE THUS CLOCKING THE SIGNALS
8736                                          ;XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE
8737                                          ;ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
8738
8739  024224  012737  001054  002346         MOV    #HDAL9!HDAL5!HDAL3!HDAL2,T6LOAD ;BITS PREVIOUSLY LOADED
8740  024232  004737  012266                 JSR    PC,XRAS              ;GO PULSE XRAS H AND XRAS L VIA HDAL12
8741
8742                                          ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL OBTS1 H IS SET TO A ONE
8743                                          ;AS A RESULT OF THE BTFET FLIP-FLOP BEING SET TO A ONE AND THE SIGNAL
8744                                          ;INTER L BEING ASSERTED HIGH.  THE SIGNAL EDEOC H SHOULD ALSO BE READ AS
8745                                          ;A ONE IN THE VDAL REGISTER AS A RESULT OF THE FOLLOWING SIGNALS BEING
8746                                          ;ASSERTED HIGH: CYCLE L, ENEDC H, PSM L, AND SOP L.
8747
8748  024236  052737  000060  002342         BIS    #VDAL5!VDAL4,T4GOOD  ;EXPECT OBTS1 H AND EDEOC H TO BE ONES
8749  024244  004737  011200                 JSR    PC,READT4            ;READ AND CHECK VDAL REGISTER
8750  024250  001405                          BEQ    6$                   ;IF OK THEN CONTINUE
8751  024252                                  ERRDF  11,VDALRG,T4EROR     ;BTS1 H OR EDEOC H PROBABLY NOT SET TO A ONE
8752  024252  104455                          TRAP   C$ERDF
8753  024254  000013                          .WORD  11
8754  024256  003710                          .WORD  VDALRG
8755  024260  006716                          .WORD  T4EROR
8756  024262                                  CKLOOP
8757  024262  104406                          TRAP   C$CLP1
8758
8759                                          ;READ CONTROL REGISTER 0 AND CHECK THAT NO CHANGES OCCURED AS A RESULT
8760                                          ;OF PULSING THE SIGNALS XRAS H AND XRAS L.
8761
8762  024264  004737  011114        6$:       JSR    PC,READT0            ;READ AND CHECK THE GDAL REGISTER
8763  024270  001405                          BEQ    7$                   ;IF NO CHANGE THEN CONTINUE
8764  024272                                  ERRDF  9,GDALRG,T0EROR      ;GDAL REG CHANGED AFTER PULSING XRAS
8765  024272  104455                          TRAP   C$ERDF
8766  024274  000011                          .WORD  9
8767  024276  003640                          .WORD  GDALRG
8768  024300  006666                          .WORD  T0EROR
8769  024302                                  CKLOOP
8770  024302  104406                          TRAP   C$CLP1
8771
8772                                          ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
8773                                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8774
8775  024304  004737  012144        7$:       JSR    PC,SLCTED            ;SELECT THE STATE ANALYZER MODULE
8776
8777                                          ;SET THE SIGNAL TRSL2 L TO THE LOW STATE BY SETTING CDAL REGISTER BIT
8778                                          ;3 TO A ONE AND CDAL REGISTER BIT 2 TO A ZERO.  THE SIGNAL TRSL2 L WILL
8779                                          ;ENABLE THE STATE ANALYZER'S SYSTEM BUS LATCHES ONTO TRDI BUS BITS 59:0.
8780
```

D 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 172
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0172

```
8781  024310  112737  000010  002272          MOVB   #CDAL3,E0LOAD          ;SETUP BITS TO SET TRSL2 L TO LOW STATE
8782  024316  004737  010700                   JSR    PC,LDRDE0             ;LOAD, READ AND CHECK CDAL REGISTER
8783  024322  001405                           BEQ    8$                   ;IF LOADED OK THEN CONTINUE
8784  024324                                   ERRDF  5,CDALRG,E0EROR       ;CDAL REGISTER NOT EQUAL EXPECTED
8785  024324  104455                           TRAP   C$ERDF
8786  024326  000005                           .WORD  5
8787  024330  003010                           .WORD  CDALRG
8788  024332  006146                           .WORD  E0EROR
8789  024334                                   CKLOOP
8790  024334  104406                           TRAP   C$CLP1
8791
8792                                            ;ASSERT THE SIGNAL PTER3 L IN THE POINTER REGISTER BY LOADING THE
8793                                            ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.
8794
8795  024336  004537  012164         8$:       JSR    R5,LDPDAL            ;LOAD AND CHECK PDAL REG WITH NEXT WORD
8796  024342  000003                           .WORD  PTER3                ;SETUP TO READ TRDI BUS BITS 47:32
8797
8798                                            ;AS A REUSLT OF THE TARGET EMULATOR'S REFR FLIP-FLOP BEING SET AND A
8799                                            ;PULSE ON THE TARGET EMULATOR SIGNALS XRAS H AND XRAS L, THE TARGET
8800                                            ;EMULATOR SIGNAL EDCK4 H WILL GO FROM A LOW TO A HIGH STATE THUS
8801                                            ;CLOCKING THE TARGET EMULATOR SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H,
8802                                            ;ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZER'S SYSTEM BUS
8803                                            ;LATCHES FOR THESE BITS.  CHECK TRDI BITS 38, 35 AND 33 TO BE SET AS
8804                                            ;A RESULT OF TARGET EMULATOR SIGNALS EDSEL0 H, BTS3 H, AND BTS1 H BEING
8805                                            ;ASSERTED TO THE HIGH STATE.
8806
8807  024344  012737  177400  002320          MOV    #177400,E6MASK        ;SETUP TO IGNORE TRDI BITS 47:40
8808  024352  012737  000112  002316          MOV    #BIT6!BIT3!BIT1,E6LOAD ;EXPECT EDSEL0, OBTS3 AND BTS1 TO BE SET
8809  024360  004737  011054                   JSR    PC,READE6            ;READ AND CHECK TRDI BITS 39:32
8810  024364  001405                           BEQ    9$                   ;IF OK THEN CONTINUE
8811  024366                                   ERRDF  8,TEEDA1,E026ER       ;TE TO SA XSEL1,EDSEL0,ADDR 17:16 + BTS 3:0 ERRO
8812  024366  104455                           TRAP   C$ERDF
8813  024370  000010                           .WORD  8
8814  024372  003242                           .WORD  TEEDA1
8815  024374  006212                           .WORD  E026ER
8816  024376                                   CKLOOP
8817  024376  104406                           TRAP   C$CLP1
8818
8819                                            ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8820                                            ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8821
8822  024400  004737  012214         9$:       JSR    PC,SLCTTE            ;SELECT THE TARGET EMULATOR MODULE
8823
8824                                            ;SET THE SIGNAL XSEL0 L TO THE HIGH STATE BY CLEARING HDAL REGISTER
8825                                            ;BIT 5.  THE HDAL REGISTER WILL BE LOADED WITH THE FOLLOWING BITS:
8826                                            ;  HDAL14H = 0           ;SETS ADDR17 H TO LOW STATE (0)
8827                                            ;  HDAL11H = 0           ;SETS ADDR16 H TO LOW STATE (0)
8828                                            ;  HDAL9H  = 1           ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
8829                                            ;  HDAL6H  = 0           ;SETS XSEL1 L TO HIGH STATE
8830                                            ;  HDAL5H  = 0           ;SETS XSEL0 L TO HIGH STATE
8831                                            ;  HDAL4H  = 0           ;SET XR/WHB L TO HIGH STATE
8832                                            ;  HDAL3H  = 1           ;SET XR/WLB L TO LOW STATE
8833                                            ;  HDAL2H  = 1           ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
8834
8835  024404  012737  001014  002346          MOV    #HDAL9!HDAL3!HDAL2,T6LOAD ;SETUP TO SET XSEL0 L TO LOW STATE
8836  024412  004737  011216                   JSR    PC,LDRDT6            ;LOAD, READ AND CHECK HDAL REGISTER
```

```
8837  024416  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
8838  024420                                  ERRDF   12,HDALRG,T06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
8839  024420  104455                          TRAP    C$ERDF
8840  024422  000014                          .WORD   12
8841  024424  003756                          .WORD   HDALRG
8842  024426  006732                          .WORD   T06ERR
8843  024430                                  CKLOOP
8844  024430  104406                          TRAP    C$CLP1
8845
8846                                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8847                                          ;WHEN XRAS H IS SET HIGH, THE PAUSE MODE FLIP-FLOP WILL BE SET TO RUN
8848                                          ;MODE THUS SETTING THE SIGNAL PAUSE L TO THE LOW STATE; THE EDFET FLIP-
8849                                          ;FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL EDFET H TO THE HIGH
8850                                          ;STATE; THE BTFET FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL
8851                                          ;BTFET L TO THE LOW STATE;  THE EDSELO FLIP-FLOP WILL BE SET TO A
8852                                          ;ZERO THUS SETTING THE SIGNAL EDSELO H TO THE LOW STATE; AND THE REFR
8853                                          ;FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL REFR H TO THE
8854                                          ;HIGH STATE.  WHEN XRAS L IS RETURNED TO THE HIGH STATE AFTER HAVING
8855                                          ;BEEN ASSERTED TO THE LOW STATE,  THE SIGNAL REFP L WILL BE  ASSERTED
8856                                          ;LOW AS A REUSLT OF THE REFR FLIP-FLOP BEING SET TO A ONE.  WHEN THE
8857                                          ;SIGNAL REFP L IS SET LOW AFTER HAVING BEEN ASSERTED HIGH, THE SIGNAL
8858                                          ;EDCK4 H WILL BE SET HIGH THUS CLOCKING TARGET EMULATOR SIGNALS XSEL1 H,
8859                                          ;EDSELO H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZER
8860                                          ;SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
8861
8862  024432  004737  012266        10$:     JSR     PC,XRAS                 ;GO PULSE XRAS H AND XRAS L VIA HDAL12
8863
8864                                          ;READ THE VDAL REG TO CHECK THAT THE SIGNALS OBTS1 H AND EDEOC H STILL 1'S
8865
8866  024436  004737  011200                 JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
8867  024442  001405                          BEQ     11$                     ;IF NO CHANGE THEN CONTINUE
8868  024444                                  ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
8869  024444  104455                          TRAP    C$ERDF
8870  024446  000013                          .WORD   11
8871  024450  003710                          .WORD   VDALRG
8872  024452  006716                          .WORD   T4EROR
8873  024454                                  CKLOOP
8874  024454  104406                          TRAP    C$CLP1
8875
8876                                          ;READ CONTROL REGISTER 0 AND CHECK THAT NO CHANGES OCCURED AS A RESULT
8877                                          ;OF PULSING THE SIGNALS XRAS H AND XRAS L.
8878
8879  024456  004737  011114        11$:     JSR     PC,READT0               ;READ AND CHECK GDAL REGISTER
8880  024462  001405                          BEQ     12$                     ;IF NO CHANGE THEN CONTINUE
8881  024464                                  ERRDF   9,GDALRG,T0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
8882  024464  104455                          TRAP    C$ERDF
8883  024466  000011                          .WORD   9
8884  024470  003640                          .WORD   GDALRG
8885  024472  006666                          .WORD   T0EROR
8886  024474                                  CKLOOP
8887  024474  104406                          TRAP    C$CLP1
8888
8889                                          ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
8890                                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8891
8892  024476  004737  012144        12$:     JSR     PC,SLCTED               ;SELECT THE STATE ANALYZER MODULE
```

F 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 174
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSELO H, + BTS BITS 3:0 TO ED   SEQ 0174

```
8893
8894                                                  ;ON THE PREVIOUS SELECTION OF THE STATE ANALYZER MODULE, CDAL3 H WAS
8895                                                  ;SET TO A ONE IN CONTROL REGISTER 0 TO SET THE SIGNAL TRSL2 L TO THE
8896                                                  ;LOW STATE.  WHEN TRSL2 L IS ASSERTED LOW, THE SYSTEM BUS LATCHES
8897                                                  ;ARE ENABLED TO TRDI BUS BITS 59:0.  READ AND CHECK CONTROL REGISTER 0.
8898
8899   024502  004737  010714                 JSR     PC,READE0            ;READ AND CHECK CDAL REGISTER
8900   024506  001405                          BEQ     13$                 ;IF OK THEN CONTINUE
8901   024510                                  ERRDF   5,CDALRG,EOEROR     ;CDAL REGISTER NOT EQUAL EXPECTED
8902   024510  104455                          TRAP    C$ERDF
8903   024512  000005                          .WORD   5
8904   024514  003010                          .WORD   CDALRG
8905   024516  006146                          .WORD   EOEROR
8906   024520                                  CKLOOP
8907   024520  104406                          TRAP    C$CLP1
8908
8909                                                  ;THE PDAL REGISTER WAS LOADED PREVIOUSLY WITH BITS TO SET THE SIGNAL
8910                                                  ;PTER3 L TO THE LOW STATE IN THE POINTER REGISTER.  AS A RESULT OF
8911                                                  ;THE TARGET EMULATOR SIGNALS REFR FLIP-FLOP BEING SET TO A ONE AND A
8912                                                  ;PULSE BEING ISSUED ON THE TARGET EMULATOR SIGNALS XRAS H AND XRAS L,
8913                                                  ;THE TARGET EMULATOR SIGNAL EDCK4 H WILL GO FROM A LOW TO A HIGH
8914                                                  ;STATE VIA THE REFP L, THUS CLOCKING THE TARGET EMULATOR SIGNALS XSEL1 H
8915                                                  ;EDSELO H, ADDR17 H, ADDR16 H, AND OBTS BITS 3:0 INTO THE STATE ANALYZER
8916                                                  ;TRDI SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).  CHECK TRDI BITS
8917                                                  ;35 AND 33 TO BE ONES AS A REUSLT OF THE TARGET EMULATOR SIGNALS OBTS3 H
8918                                                  ;AND OBTS1 H BEING ASSERTED HIGH.
8919
8920   024522  012737  000012  002316  13$:    MOV     #BIT3!BIT1,E6LOAD   ;EXPECT OBTS1 H AND OBTS3 H TO BE ONES
8921   024530  004737  011054                  JSR     PC,READE6           ;READ AND CHECK TRDI BITS 39:32
8922   024534  001405                          BEQ     14$                 ;IF OK THEN CONTINUE
8923   024536                                  ERRDF   8,TEEDA1,E026ER     ;TE TO SA XSEL1,EDSELO,ADDR 17:16 + BTS 3:0 ERRO
8924   024536  104455                          TRAP    C$ERDF
8925   024540  000010                          .WORD   8
8926   024542  003242                          .WORD   TEEDA1
8927   024544  006212                          .WORD   E026ER
8928   024546                                  CKLOOP
8929   024546  104406                          TRAP    C$CLP1
8930
8931                                                  ;SELECT TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
8932                                                  ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
8933
8934   024550  004737  012214                 14$:    JSR     PC,SLCTTE           ;SELECT THE TARGET EMULATOR MODULE
8935
8936                                                  ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES HAVE OCCURED.
8937
8938   024554  004737  011114                  JSR     PC,READT0           ;READ AND CHECK GDAL REGISTER
8939   024560  001405                          BEQ     15$                 ;IF NO CHANGES THEN CONTINUE
8940   024562                                  ERRDF   9,GDALRG,TOEROR     ;GDAL REGISTER NOT EQUAL EXPECTED
8941   024562  104455                          TRAP    C$ERDF
8942   024564  000011                          .WORD   9
8943   024566  003640                          .WORD   GDALRG
8944   024570  006666                          .WORD   TOEROR
8945   024572                                  CKLOOP
8946   024572  104406                          TRAP    C$CLP1
8947
8948                                                  ;SET THE SIGNAL FETCT H TO THE LOW STATE AND PULSE THE SIGNAL INVD L
```

G 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 175
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0175

```
8949                                                ;BY SETTING AND CLEARING VDAL2 H.  A PULSE ON INVD L WILL CLEAR/SET
8950                                                ;ALL FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY THE
8951                                                ;SIGNAL BRKRES L.  FOR THIS PARTICULAR TEST, A PULSE ON INVD L WILL
8952                                                ;CLEAR THE BTFET AND EDSEL0  FLIP-FLOPS.
8953
8954    024574  005037  002340          15$:       CLR      T4LOAD                      ;SETUP TO CLEAR FETCT H
8955    024600  004737  012706                     JSR      PC,CLRPSM                   ;SET FETCT H LOW AND PULSE INVD L
8956
8957                                                ;SET THE SIGNAL XSEL0 L TO THE LOW STATE BY SETTING HDAL REGISTER BIT
8958                                                ;5 TO A ONE.  THE HDAL REGISTER WILL BE LOADED WITH THE FOLLOWING BITS:
8959                                                ;  HDAL14H = 0               ;SETS ADDR17 H TO LOW STATE (0)
8960                                                ;  HDAL11H = 0               ;SETS ADDR16 H TO LOW STATE (0)
8961                                                ;  HDAL9H  = 1               ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
8962                                                ;  HDAL6H  = 0               ;SETS XSEL1 L TO HIGH STATE
8963                                                ;  HDAL5H  = 1               ;SETS XSEL0 L TO LOW STATE
8964                                                ;  HDAL4H  = 0               ;SET XR/WHB L TO HIGH STATE
8965                                                ;  HDAL3H  = 1               ;SET XR/WLB L TO LOW STATE
8966                                                ;  HDAL2H  = 1               ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
8967
8968    024604  012737  001054  002346  MOV      #HDAL9!HDAL5!HDAL3!HDAL2,T6LOAD ;SETUP BITS TO  BE LOADED
8969    024612  004737  011216                     JSR      PC,LDRDT6                   ;LOAD, READ AND CHECK HDAL REGISTER
8970    024616  001405                             BEQ      16$                         ;IF LOADED OK THEN CONTINUE
8971    024620                                     ERRDF    12,HDALRG,T06ERR            ;HDAL REGISTER NOT EQUAL EXPECTED
8972    024620  104455                             TRAP     C$ERDF
8973    024622  000014                             .WORD    12
8974    024624  003756                             .WORD    HDALRG
8975    024626  006732                             .WORD    T06ERR
8976    024630                                     CKLOOP
8977    024630  104406                             TRAP     C$CLP1
8978
8979                                                ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL REGISTER BIT 13.
8980                                                ;A PULSE ON XCAS H WILL CAUSE THE ENCLK FLIP-FLOP AND THE ENEDC FLIP-FLOP
8981                                                ;TO BE SET TO ONES.  THE EDSEL0 FLIP-FLOP WILL BE CLOCKED TO A ZERO THUS
8982                                                ;SETTING THE SIGNAL EDSEL0 H TO THE HIGH STATE
8983
8984    024632  004737  012372          16$:       JSR      PC,XCAS                     ;GO PULSE XCAS H AND XCAS L VIA HDAL13 H
8985
8986                                                ;READ VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A ONE
8987                                                ;AS A RESULT OF CYCLE L, PSM L, ENEDC H AND SOP L BEING ASSERTED HIGH.
8988
8989    024636  052737  000020  002342  BIS      #VDAL4,T4GOOD               ;EXPECT EDEOC H TO BE SET TO A ONE
8990    024644  004737  011200                     JSR      PC,READT4                   ;READ AND CHECK VDAL REGISTER
8991    024650  001405                             BEQ      17$                         ;IF OK THEN CONTINUE
8992    024652                                     ERRDF    11,VDALRG,T4EROR            ;VDAL REGISTER NOT EQUAL EXPECTED
8993    024652  104455                             TRAP     C$ERDF
8994    024654  000013                             .WORD    11
8995    024656  003710                             .WORD    VDALRG
8996    024660  006716                             .WORD    T4EROR
8997    024662                                     CKLOOP
8998    024662  104406                             TRAP     C$CLP1
8999
9000                                                ;TOGGLE THE SIGNAL XPI L BY SETTING AND CLEARING HDAL REGISTER BIT 15.
9001                                                ;WHEN XPI L IS TOGGLED, A PULSE WILL OCCUR ON THE SIGNAL EDCK4 H.  A
9002                                                ;PULSE ON EDCK4 H WILL CLOCK THE TARGET EMULATOR SIGNALS XSEL1 H,
9003                                                ;EDSEL0 H, ADDR17 H, ADDR16 H, AND OBTS BITS 3:0 INTO THE STATE ANALYZERS
9004                                                ;SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
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9005
9006    024664  004737  012476              17$:    JSR     PC,XPI                    ;GO PULSE XPI L VIA HDAL15 H
9007
9008                                                ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9009                                                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9010
9011    024670  004737  012144                      JSR     PC,SLCTED                 ;SELECT THE STATE ANALYZER MODULE
9012
9013                                                ;FROM PREVIOUS SELECTIONS OF THE STATE ANALYZER MODULE, CDAL3 H WAS
9014                                                ;SET TO A ONE IN CONTROL REGISTER 0 AND BITS WERE LOADED INTO CONTROL
9015                                                ;REGISTER 2'S PDAL REGISTER TO SET THE SIGNAL PTER3 L IN THE POINTER
9016                                                ;REGISTER.  WHEN CDAL3 H IS SET TO A ONE AND CDAL2 H IS SET TO A ZERO,
9017                                                ;THE SIGNAL TRSL2 L IS SET TO THE LOW STATE.  THE SIGNAL TRSL2 '. WILL
9018                                                ;ENABLE THE STATE ANALYZER SYSTEM BUS LATCHES ONTO TRDI BUS BITS 59:0.
9019                                                ;WHEN PTER3 L IS ASSERTED LOW IN THE POINTER REGISTER AND A READ COMMAND
9020                                                ;IS ISSUED TO CONTROL REGISTER 6, TRDI BUS BITS 47:32 WILL BE READ.  AS
9021                                                ;A RESULT OF PULSING THE TARGET EMULATOR SIGNAL XPI L, A PULSE SHOULD
9022                                                ;HAVE OCCURED ON THE TARGET EMULATOR SIGNAL EDCK4 H.  A PULSE ON THE
9023                                                ;SIGNAL EDCK4 H SHOULD HAVE CLOCKED THE TARGET EMULATOR SIGNALS XSEL1 H,
9024                                                ;EDSEL0 H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZERS
9025                                                ;TRDI SYSTEM BUS LATCHES FOR BITS 39:32.  AS A RESULT OF PULSING INVD L
9026                                                ;ON THE TARGET EMULATOR MODULE,  THE ONLY BIT THAT SHOULD BE ASSERTED
9027                                                ;HIGH WHEN READ IS THE BIT FOR EDSEL0 H, TRDI BIT 38.  INVD L SHOULD
9028                                                ;HAVE CLEARED THE TARGET EMULATOR FLIP-FLOPS BTFET, EDSEL0, AND REFR.
9029                                                ;A PULSE ON XCAS H SHOULD HAVE CAUSED THE EDSEL0 FLIP-FLOP TO BE CLOCKED
9030                                                ;TO A ZERO THUS SETTING THE SIGNAL EDSEL0 H TO THE HIGH STATE.  THE
9031                                                ;SIGNAL XSEL0 L WAS ASSERTED LOW IN THE LAST SELECTION OF THE TARGET
9032                                                ;EMULATOR MODULE.  THE PROGRAM CAN NOT TEST THAT THE SIGNAL INVD L CLEARED
9033                                                ;THE EDSEL0 FLIP-FLOP BECAUSE THE ENCLK FLIP-FLOP IS ALSO CLEARED BY
9034                                                ;THE SIGNAL INVD L.
9035
9036    024674  012737  000100  002316              MOV     #BIT6,E6LOAD              ;EXPECT EDSEL0 H TO BE A 1 ON TRDI38 H
9037    024702  004737  011054                      JSR     PC,READE6                 ;READ TRDI BUS BITS 47:32
9038    024706  001405                              BEQ     18$                       ;IF LOADED OK THEN CONTINUE
9039    024710                                      ERRDF   8,TEEDA1,E026ER           ;TE TO SA XSEL1,EDSEL0,ADDR 17:16 + BTS 3:0 ERRO
9040    024710  104455                              TRAP    C$ERDF
9041    024712  000010                              .WORD   8
9042    024714  003242                              .WORD   TEEDA1
9043    024716  006212                              .WORD   E026ER
9044    024720                                      CKLOOP
9045    024720  104406                              TRAP    C$CLP1
9046
9047                                                ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9048                                                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9049
9050    024722  004737  012214              18$:    JSR     PC,SLCTTE                 ;SELECT TARGET EMULATOR MODULE
9051
9052                                                ;SET THE SIGNALS INTER L AND INTER H TO THE LOW AND HIGH STATE RESPECTIVELY
9053                                                ;BY SETTING THE SIGNAL XSEL0 L TO THE HIGH STATE AND XSEL1 L TO THE LOW
9054                                                ;STATE.  TO DO THIS THE PROGRAM WILL LOAD HDAL REGISTER WITH THE FOLLOWING
9055                                                ;BIT PATTERNS:
9056                                                ;   HDAL14H = 0             ;SETS ADDR17 H TO LOW STATE (0)
9057                                                ;   HDAL11H = 0             ;SETS ADDR16 H TO LOW STATE (0)
9058                                                ;   HDAL9H  = 1             ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
9059                                                ;   HDAL6H  = 1             ;SETS XSEL1 L TO LOW STATE
9060                                                ;   HDAL5H  = 0             ;SETS XSEL0 L TO HIGH STATE
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I 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 177
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSELO H, + BTS BITS 3:0 TO ED   SEQ 0177

```
9061                                          ;  HDAL4H  = 0          ;SET XR/WHB L TO HIGH STATE
9062                                          ;  HDAL3H  = 1          ;SET XR/WLB L TO LOW STATE
9063                                          ;  HDAL2H  = 1          ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
9064
9065  024726  012737  001114  002346    MOV      #HDAL9!HDAL6!HDAL3!HDAL2,T6LOAD  ;SETUP HDAL BITS TO BE LOADED
9066  024734  004737  011216            JSR      PC,LDRDT6            ;LOAD, READ AND CHECK HDAL REGISTER
9067  024740  001405                    BEQ      19$                 ;IF LOADED OK THEN CONTINUE
9068  024742                            ERRDF    12,HDALRG,T06ERR     ;HDAL REGISTER NOT EQUAL EXPECTED
9069  024742  104455                    TRAP     C$ERDF
9070  024744  000014                    .WORD    12
9071  024746  003756                    .WORD    HDALRG
9072  024750  006732                    .WORD    T06ERR
9073  024752                            CKLOOP
9074  024752  104406                    TRAP     C$CLP1
9075
9076                                    ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL REG-
9077                                    ;ISTER BIT 12.  WHEN XRAS H IS SET TO THE HIGH STATE, THE PAUSE MODE
9078                                    ;FLIP-FLOP WILL BE SET TO RUN MODE THUS SETTING THE SIGNAL PAUSE L TO
9079                                    ;THE LOW STATE; THE EDFET FLIP-FLOP WILL BE SET TO A ZERO THUS SETTING
9080                                    ;THE SIGNAL EDFET H TO THE LOW STATE; THE BTFET FLIP-FLOP WILL BE SET TO
9081                                    ;A ZERO THUS SETTING THE SIGNAL BTFET L TO THE HIGH STATE; THE EDSELO
9082                                    ;FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL EDSELO H TO THE
9083                                    ;LOW STATE.  WHEN XRAS H IS SET TO THE HIGH STATE, THE REFR FLIP-FLOP
9084                                    ;WILL BE SET TO A ZERO THUS SETTING THE SIGNAL REFR L TO THE HIGH STATE.
9085                                    ;A PULSE WILL OCCUR ON THE SIGNAL EDCK4 H WHEN XRAS H IS TOGGLED AS A
9C86                                    ;RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED HIGH: INTER H, XPI L,
9087                                    ;AND REFP L.  WHEN THE SIGNAL EDCK4 H IS PULSED, THE SIGNALS XSEL1 H,
9088                                    ;EDSELO H, ADDR17 H, ADDR16 H, AND OBTS BITS 3:0 ARE CLOCKED INTO THE
9089                                    ;STATE ANALYZER'S SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
9090
9091  024754  004737  012266    19$:    JSR      PC,XRAS             ;GO PULSE XRAS H AND XRAS L VIA HDAL12
9092
9093                                    ;CHECK THE SIGNAL OBTS1 H TO BE SET TO A ONE IN CONTROL REGISTER 4 AS A
9094                                    ;RESULT OF THE SIGNAL INTER L BEING ASSERTED LOW AND THE BTFET FLIP-
9095                                    ;FLOP BEING SET TO A ZERO.  CHECK THAT THE SIGNAL EDEOC H IS ALSO SET TO
9096                                    ;A ONE AS A RESULT OF CYCLE L, ENEDC H, PSM L, AND SOP L BEING ASSERTED
9097                                    ;TO THE HIGH STATES.
9098
9099  024760  012737  000060  002342    MOV      #VDAL5!VDAL4,T4GOOD  ;EXPECT OBTS1 H AND EDEOC H TO BE ONES
9100  024766  004737  011200            JSR      PC,READT4           ;READ AND CHECK VDAL REGISTER
9101  024772  001405                    BEQ      20$                 ;IF NO CHANGES THEN CONTINUE
9102  024774                            ERRDF    11,VDALRG,T4EROR     ;VDAL REGISTER NOT EQUAL EXEPECTED
9103  024774  104455                    TRAP     C$ERDF
9104  024776  000013                    .WORD    11
9105  025000  003710                    .WORD    VDALRG
9106  025002  006716                    .WORD    T4EROR
9107  025004                            CKLOOP
9108  025004  104406                    TRAP     C$CLP1
9109
9110                                    ;READ CONTROL REGISTER 0, GDAL REGISTER, AND CHECK THAT NO CHANGES
9111                                    ;OCCURED AS A RESULT OF PULSING THE SIGNALS XRAS H AND XRAS L.
9112
9113  025006  004737  011114    20$:    JSR      PC,READT0           ;READ AND CHECK GDAL REGISTER
9114  025012  001405                    BEQ      21$                 ;IF NO CHANGES THEN CONTINUE
9115  025014                            ERRDF    9,GDALRG,TOEROR      ;GDAL REGISTER NOT EQUAL EXPECTED
9116  025014  104455                    TRAP     C$ERDF
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J 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 178
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0178

```
9117   025016  000011              .WORD   9
9118   025020  003640              .WORD   GDALRG
9119   025022  006666              .WORD   TOEROR
9120   025024                      CKLOOP
9121   025024  104406              TRAP    C$CLP1
9122
9123                       ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9124                       ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9125
9126   025026  004737  012144    21$:  JSR     PC,SLCTED          ;SELECT STATE ANALYZER MODULE
9127
9128                       ;IN PREVIOUS SELECTIONS OF THE STATE ANALYZER MODULE, CDAL3 H WAS SET
9129                       ;TO A ONE AND CDAL2 H WAS SET TO A ZERO TO ASSERT THE SIGNAL TRSL2 L.
9130                       ;WHEN TRSL2 L IS ASSERTED LOW, THE STATE ANALYZER'S SYSTEM BUS LATCHES
9131                       ;ARE ENABLED TO THE STATE ANALYZER'S TRDI BUS BITS 59:0.  BITS WERE ALSO
9132                       ;LOADED INTO CONTROL REGISTER 2'S PDAL REGISTER TO ASSERT THE SIGNAL
9133                       ;PTER3 L TO THE LOW STATE IN THE POINTER REGISTER.  WHEN A READ COMMAND
9134                       ;IS ISSUED TO CONTRO' REGISTER 6 AND PTER3 L IS ASSERTED LOW, TRDI BUS
9135                       ;BITS 47:32 WILL BE READ.  AS A RESULT OF PULSING XRAS H ON THE TARGET
9136                       ;EMULATOR MODULE WHEN THE SIGNAL INTER H WAS ASSERTED HIGH, A PULSE
9137                       ;SHOULD HAVE OCCURED ON THE TARGET EMULAOTR SIGNAL EDCK4 H.  A PULSE
9138                       ;ON THE SIGNAL EDCK4 H WILL CLOCK THE TARGET EMULATOR SIGNALS XSEL1 H,
9139                       ;EDSEL0 H, ADDR17 H, ADDR16 H, AND OBTS BITS 3:0 INTO THE STATE ANALYZERS
9140                       ;SYSTEM BUS LATCHES FOR THESE BITS, TRDI BUS BITS 39:32.  STATE ANALYZER
9141                       ;TRDI BITS 39, 33 AND 32 SHOULD BE READ AS ONES AS A RESULT OF XSEL1 H
9142                       ;BEING ASSERTED HIGH AND INTER L BEING ASSERTED LOW ON THE TARGET
9143                       ;EMULATOR MODULE.
9144
9145   025032  012737  000203  002316    MOV  #BIT7!BIT1!BIT0,E6LOAD  ;EXPECT XSEL1 H,OBTS1 H + BTS0 H TO = 1
9146   025040  004737  011054              JSR     PC,READE6          ;READ AND CHECK TRDI BUS BITS 39:32
9147   025044  001405                      BEQ     22$                ;IF OK THEN CONTINUE
9148   025046                              ERRDF   8,TEEDA1,E026ER    ;TE TO SA XSEL1,EDSEL0,ADDR 17:16 + BTS 3:0 ERRO
9149   025046  104455                      TRAP    C$ERDF
9150   025050  000010                      .WORD   8
9151   025052  003242                      .WORD   TEEDA1
9152   025054  006212                      .WORD   E026ER
9153   025056                              CKLOOP
9154   025056  104406                      TRAP    C$CLP1
9155
9156                       ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9157                       ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9158
9159   025060  004737  012214    22$:  JSR     PC,SLCTTE          ;SELECT THE TARGET EMULATOR MODULE
9160
9161                       ;SET THE SIGNALS INTER L AND INTER H TO THE HIGH AND LOW STATES RESPEC-
9162                       ;TIVELY.  SET THE SIGNAL DMG L TO THE LOW STATE BY SETTING XSEL1 L
9163                       ;AND XSEL0 L TO THE LOW STATES VIA BITS IN THE HDAL REGISTER.  THE HDAL
9164                       ;REGISTER WILL BE LOADED WITH THE FOLLOWING BITS
9165                       ;   HDAL14H = 0              ;SETS ADDR17 H TO LOW STATE (0)
9166                       ;   HDAL11H = 0              ;SETS ADDR16 H TO LOW STATE (0)
9167                       ;   HDAL9H  = 1              ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
9168                       ;   HDAL6H  = 1              ;SETS XSEL1 L TO LOW STATE
9169                       ;   HDAL5H  = 1              ;SETS XSEL0 L TO LOW STATE
9170                       ;   HDAL4H  = 0              ;SET XR/WHB L TO HIGH STATE
9171                       ;   HDAL3H  = 1              ;SET XR/WLB L TO LOW STATE
9172                       ;   HDAL2H  = 1              ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
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K 14

HARDWARE TESTS MAC/11 30A(1052) 16-JUN-82 13:46 PAGE 179
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSELO H, + BTS BITS 3:0 TO ED   SEQ 0179

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9173
9174    025064  012737  001154  002346          MOV     #HDAL9!HDAL6!HDAL5!HDAL3!HDAL2,T6LOAD ;SETUP HDAL REG BITS
9175    025072  004737  011216                  JSR     PC,LDRDT6                ;LOAD, READ AND CHECK HDAL REGISTER
9176    025076  001405                          BEQ     23$                     ;IF LOADED OK THEN CONTINUE
9177    025100                                  ERRDF   12,HDALRG,T06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
9178    025100  104455                          TRAP    C$ERDF
9179    025102  000014                          .WORD   12
9180    025104  003756                          .WORD   HDALRG
9181    025106  006732                          .WORD   T06ERR
9182    025110                                  CKLOOP
9183    025110  104406                          TRAP    C$CLP1
9184
9185                                    ;SET ADAL REGISTER BIT 7 TO A ZERO TO HOLD THE REFR FLIP-FLOP IN THE
9186                                    ;ZERO STATE.  WHEN THE REFR FLIP-FLOP IS HELP CLEARED, THE SIGNALS
9187                                    ;REFR L AND REFP L WILL BE HELD TO THE HIGH STATE.
9188
9189    025112  042737  000200  002334  23$:    BIC     #ADAL7,T2LOAD           ;SETUP BIT TO HOLD REFR F/F CLEARED
9190    025120  004737  011140                  JSR     PC,LDRDT2               ;LOAD, READ AND CHECK ADAL REGISTER
9191    025124  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
9192    025126                                  ERRDF   10,ADALRG,T2EROR        ;ADAL REGISTER NOT EQUAL EXPECTED
9193    025126  104455                          TRAP    C$ERDF
9194    025130  000012                          .WORD   10
9195    025132  003664                          .WORD   ADALRG
9196    025134  006702                          .WORD   T2EROR
9197    025136                                  CKLOOP
9198    025136  104406                          TRAP    C$CLP1
9199
9200                                    ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL
9201                                    ;REGISTER BIT 12.  WHEN THESE SIGNALS ARE TOGGLED, THE PAUSE MODE FLIP-
9202                                    ;FLOP WILL BE SET TO RUN MODE THUS SETTING THE SIGNAL PAUSE L TO THE
9203                                    ;LOW STATE; THE EDFET FLIP-FLOP WILL BE SET TO A ZERO THUS SETTING THE
9204                                    ;SIGNAL EDFET H TO THE LOW STATE; THE BTFET FLIP-FLOP WILL BE SET TO A
9205                                    ;ZERO THUS SETTING THE SIGNAL BTFET L TO THE HIGH STATE; AND THE EDSELO
9206                                    ;FLIP-FLOP WILL BE SET TO A ZERO THUS SETTING THE SIGNAL EDSELO H TO THE
9207                                    ;HIGH STATE.
9208
9209    025140  004737  012266          24$:    JSR     PC,XRAS                 ;GO PULSE XRAS H AND XRAS L VIA HDAL12
9210
9211                                    ;TOGGLE THE SIGNAL XPI L BY SETTING AND CLEARING HDAL REGISTER BIT 15.
9212                                    ;WHEN XPI L IS SET LOW AND THE SIGNAL INTER H IS ASSERTED LOW AND THE
9213                                    ;SIGNAL REFP L IS ASSERTED HIGH, THE SIGNAL EDCK4 H WILL GO FROM A LOW
9214                                    ;TO A HIGH STATE THUS CLOCKING THE SIGNALS XSEL1 H, EDSELO H, ADDR17 H,
9215                                    ;ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZER'S SYSTEM BUS LATCHES
9216                                    ;FOR THESE BITS, TRDI 39:32.  THE SIGNALS XSEL1 H, EDSELO H AND OBTS. H
9217                                    ;SHOULD BE ASSERTED HIGH AT THIS POINT IN TIME.  WHEN XPI L IS RETURNED
9218                                    ;TO THE HIGH STATE, THE SIGNAL EDCK4 H WILL BE SET LOW.
9219
9220    025144  004737  012476                  JSR     PC,XPI                  ;GO PULSE XPI L VIA HDAL REG BIT 15
9221
9222                                    ;CHECK OBTS1 H TO BE A ZERO IN CONTROL REGISTER 4 AS A RESULT OF THE
9223                                    ;SIGNAL INTER L BEING ASSERTED HIGH AND THE BTFET FLIP-FLOP BEING SET
9224                                    ;TO A ZERO.  EXPECT EDEOC H TO BE READ AS A ONE AS A RESULT OF THE
9225                                    ;SIGNALS CYCLE L, ENEDC H, PSM L AND SOP L BEING ASSERTED HIGH.
9226
9227    025150  012737  000020  002342          MOV     #VDAL4,T4GOOD           ;EXPECT EDEOC H TO BE SET TO A ONE
9228    025156  004737  011200                  JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
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L 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 180
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0180

```
9229  025162  001405                              BEQ     25$                     ;IF NO CHANGES THEN CONTINUE
9230  025164                                      ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
9231  025164  104455                              TRAP    C$ERDF
9232  025166  000013                              .WORD   11
9233  025170  003710                              .WORD   VDALRG
9234  025172  006716                              .WORD   T4EROR
9235  025174                                      CKLOOP
9236  025174  104406                              TRAP    C$CLP1
9237
9238                                              ;READ CONTROL REGISTER 0'S GDAL REGISTER AND CHECK THAT NO CHANGES
9239                                              ;OCCURED AS A RESULT OF PULSING XRAS AND XPI.
9240
9241  025176  004737  011114           25$:       JSR     PC,READT0               ;READ AND CHECK GDAL REGISTER
9242  025202  001405                              BEQ     26$                     ;IF NO CHANGES THEN CONTINUE
9243  025204                                      ERRDF   9,GDALRG,T0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
9244  025204  104455                              TRAP    C$ERDF
9245  025206  000011                              .WORD   9
9246  025210  003640                              .WORD   GDALRG
9247  025212  006666                              .WORD   T0EROR
9248  025214                                      CKLOOP
9249  025214  104406                              TRAP    C$CLP1
9250
9251                                              ;SELECT STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9252                                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9253
9254  025216  004737  012144           26$:       JSR     PC,SLCTED               ;SELECT STATE ANALYZER MODULE
9255
9256                                              ;IN PREVIOUS SELECTIONS OF THE STATE ANALYZER MODULE, CDAL3 H WAS SET TO
9257                                              ;A ONE AND CDAL2 H WAS SET TO A ZERO.  THIS WAS DONE TO ASSERT THE
9258                                              ;SIGNAL TRSL2 L.  WHEN TRSL2 L IS ASSERTED LOW, THE STATE ANALYZER'S
9259                                              ;SYSTEM BUS LATCHES ARE ENABLED TO THE STATE ANALYZERS TRDI BUS BITS 59:0.
9260                                              ;BITS WERE ALSO LOADED INTO CONTROL REGISTER 2'S PDAL REGISTER TO ASSERT
9261                                              ;THE SIGNAL PTER3 L IN THE POINTER REGISTER.  WHEN A READ COMMAND IS
9262                                              ;ISSUED TO CONTROL REGISTER 6 ABD PTER3 L IS ASSERTED LOW, TRDI BUS BITS
9263                                              ;47:32 ARE READ.  AS A RESULT OF PULSING XPI L ON THE TARGET EMULATOR
9264                                              ;MODULE, A PULSE SHOULD HAVE OCCURED ON THE SIGNAL EDCK4 H.  A PULSE
9265                                              ;ON THE SIGNAL EDCK4 H WILL CLOCK THE TARGET EMULATOR SIGNALS XSEL1 H,
9266                                              ;EDSEL0 H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0 INTO THE STATE ANALYZERS
9267                                              ;SYSTEM BUS LATCHES FOR THESE BITS, TRDI BUS BITS 39:32.  WHEN THESE
9268                                              ;BITS ARE READ, TRDI BITS 39. 38 AND 34 SHOULD BE SET TO ONES AS A
9269                                              ;RESULT OF XSEL1 H, EDSEL0 H AND OBTS2 H BEING ASSERTED HIGH ON THE
9270                                              ;TARGET EMULATOR MODULE.  OBTS2 H IS ASSERTED HIGH AS A RESULT OF
9271                                              ;TARGET EMULATOR SIGNALS DMG L BEING LOW AND ASPI L BEING HIGH.
9272
9273  025222  012737  000304  002316   MOV     #BIT7!BIT6!BIT2,E6LOAD  ;EXPECT XSEL1 H, EDSEL0 H AND OBTS2 H
9274  025230  004737  011054              JSR     PC,READE6               ;READ AND CHECK TRDI BUS BITS 39:32
9275  025234  001405                       BEQ     27$                     ;IF OK THEN CONTINUE
9276  025236                                ERRDF   8,TEEDA1,E026ER         ;TE TO SA XSEL1,EDSEL0,ADDR 17:16 + BTS 3:0 ERRO
9277  025236  104455                        TRAP    C$ERDF
9278  025240  000010                        .WORD   8
9279  025242  003242                        .WORD   TEEDA1
9280  025244  006212                        .WORD   E026ER
9281  025246                                CKLOOP
9282  025246  104406                        TRAP    C$CLP1
9283
9284                                        ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
```

M 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 181
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSELO H, + BTS BITS 3:0 TO ED   SEQ 0181

```
9285                                                    ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9286
9287   025250  004737  012214          27$:    JSR     PC,SLCTTE                   ;SELECT THE TARGET EMULATOR MODULE
9288
9289                                                    ;SET THE SIGNAL DMG L BACK TO THE HIGH STATE BY SETTING THE SIGNALS
9290                                                    ;XSELO L AND XSEL1 L TO THE HIGH STATES VIA THE HDAL REGISTER.  THE
9291                                                    ;HDAL REGISTER WILL BE LOADED WITH THE FOLLOWING BITS:
9292                                                    ;  HDAL14H = 0          ;SETS ADDR17 H TO THE LOW STATE (0)
9293                                                    ;  HDAL13H = 0          ;SETS ADDR16 H TO THE LOW STATE (0)
9294                                                    ;  HDAL9H  = 1          ;ENABLES DIAG ADDRESS REG TO SYSTEM ADDRESS BUS
9295                                                    ;  HDAL6H  = 0          ;SET XSEL1 L TO THE HIGH STATE
9296                                                    ;  HDAL5H  = 0          ;SET XSELO L TO THE HIGH STATE
9297                                                    ;  HDAL4H  = 0          ;SET XR/WHB L TO THE HIGH STATE
9298                                                    ;  HDAL3H  = 1          ;SET XR/WLB L TO THE LOW STATE
9299                                                    ;  HDAL2H  = 1          ;ALLOWS PROGRAM TO GENERATE T-11 TIMING SIGNALS
9300
9301   025254  012737  001014  002346          MOV     #HDAL9!HDAL3!HDAL2,T6LOAD  ;SETUP HDAL REGISTER BITS TO BE LOADED
9302   025262  004737  011216                  JSR     PC,LDRDT6                   ;LOAD,READ AND CHECK HDAL REGISTER
9303   025266  001405                          BEQ     28$                        ;IF LOADED OK THEN CONTINUE
9304   025270                                  ERRDF   12,HDALRG,T06ERR           ;HDAL REGISTER NOT EQUAL EXPECTED
9305   025270  104455                          TRAP    C$ERDF
9306   025272  000014                          .WORD   12
9307   025274  003756                          .WORD   HDALRG
9308   025276  006732                          .WORD   T06ERR
9309   025300                                  CKLOOP
9310   025300  104406                          TRAP    C$CLP1
9311
9312                                                    ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL
9313                                                    ;REGISTER BIT 12.  WHEN THESE SIGNALS ARE TOGGLED, THE PAUSE MODE FLIP-
9314                                                    ;FLOP WILL BE SET TO RUN MODE THUS SETTING THE SIGNAL PAUSE L TO THE
9315                                                    ;LOW STATE; THE EDFET FLIP-FLOP WILL BE SET TO A ZERO THUS SETTING THE
9316                                                    ;SIGNAL EDFET H TO THE LOW STATE; THE BTFET FLIP-FLOP WILL BE SET TO A
9317                                                    ;ZERO THUS SETTING THE SIGNAL BTFET L TO THE HIGH STATE; AND THE EDSELO
9318                                                    ;FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL EDSELO H TO THE
9319                                                    ;LOW STATE.
9320
9321   025302  004737  012266          28$:    JSR     PC,XRAS                    ;GO PULSE XRAS H + XRAS L VIA HDAL12 H
9322
9323                                                    ;SET THE SIGNAL XCAS H TO THE LOW STATE AND THEN SET THE SIGNAL XPI L
9324                                                    ;TO THE LOW STATE.  WHEN XCAS H IS SET HIGH WITHOUT XRAS L SET LOW, THE
9325                                                    ;SIGNAL ASPI L WILL BE ASSERTED LOW.  THE SIGNAL ASPI L WILL SET THE
9326                                                    ;SIGNALS OBTS2 H AND OBTS3 H TO THE HIGH STATES.  WHEN XPI L IS SET LOW
9327                                                    ;AND THE SIGNAL INTER H IS ASSERTED LOW AND THE SIGNAL REFP L IS
9328                                                    ;ASSERTED HIGH, THE SIGNAL EDCK4 H WILL GO FROM A LOW TO A HIGH STATE.
9329                                                    ;WHEN THE SIGNAL EDCK4 H GOES FROM A LOW TO A HIGH STATE, THE TARGET
9330                                                    ;EMULATOR SIGNALS XSEL1 H, EDSELO H, ADDR17 H, ADDR16 H, AND OBTS BITS
9331                                                    ;3:0 WILL BE CLOCKED INTO THE STATE ANALYZER SYSTEM BUS LATCHES FOR
9332                                                    ;THESE BITS, WHICH ARE TRDI SYSTEM BUS LATCHES FOR BITS 39:32.
9333
9334   025306  004737  012404                  JSR     PC,XCASH                   ;SET XCAS H HIGH AND XCAS L LOW
9335   025312  004737  012510                  JSR     PC,XPIH                    ;SET XPI H HIGH AND XPI L LOW
9336
9337                                                    ;RETURN XCAS H AND XPI L TO THE LOW AND HIGH STATE RESPECTIVELY.  WHEN
9338                                                    ;XPI L IS SET HIGH THE SIGNAL EDCK4 H WILL GO TO THE LOW STATE FROM THE
9339                                                    ;HIGH STATE.  THE SIGNAL ASPI L WILL BE SET HIGH WHEN XCAS H IS SET TO
9340                                                    ;THE LOW STATE FROM THE HIGH STATE.
```

N 14

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 182
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0182

```
9341
9342   025316  004737  012436              JSR     PC.XCASL                ;SET XCAS H LOW AND XCAS L HIGH
9343   025322  004737  012542              JSR     PC.XPIL                 ;SET XPI H LOW AND XPI L HIGH
9344
9345                                        ;READ THE VDAL REGISTER AND CHECK THAT THE ONLY SIGNAL SET IN THE
9346                                        ;VDAL REGISTER IS BIT 4, WHICH IS THE SIGNAL EDEOC H.
9347
9348   025326  052737  000020  002342      BIS     #VDAL4,T4GOOD           ;EXPECT EDEOC H TO BE A ONE
9349   025334  004737  011200              JSR     PC.READT4               ;READ AND CHEKC VDAL REGISTER
9350   025340  001405                      BEQ     29$                     ;IF EDEOC H SET THEN CONTINUE
9351   025342                              ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
9352   025342  104455                      TRAP    C$ERDF
9353   025344  000013                      .WORD   11
9354   025346  003710                      .WORD   VDALRG
9355   025350  006716                      .WORD   T4EROR
9356   025352                              CKLOOP
9357   025352  104406                      TRAP    C$CLP1
9358
9359                                        ;READ AND CHECK CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED
9360                                        ;WHEN XRAS, XCAS AND XPI WERE TOGGLED.
9361
9362   025354  004737  011114      29$:    JSR     PC.READT0               ;READ AND CHECK GDAL REGISTER
9363   025360  001405                      BEQ     30$                     ;IF NO CHANGES THEN CONTINUE
9364   025362                              ERRDF   9,GDALRG,T0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
9365   025362  104455                      TRAP    C$ERDF
9366   025364  000011                      .WORD   9
9367   025366  003640                      .WORD   GDALRG
9368   025370  006666                      .WORD   T0EROR
9369   025372                              CKLOOP
9370   025372  104406                      TRAP    C$CLP1
9371
9372                                        ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9373                                        ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9374
9375   025374  004737  012144      30$:    JSR     PC.SLCTED               ;SELECT THE STATE ANALYZER MODULE
9376
9377                                        ;IN PREVIOUS SELECTIONS OF THE STATE ANALYZER MODULE, CDAL3 H WAS SET
9378                                        ;TO A ONE AND CDAL2 H WAS SET TO A ZERO.  THIS WAS DONE TO ASSERT THE
9379                                        ;SIGNAL TRSL2 L.  WHEN TRSL2 L IS ASSERTED LOW, THE STATE ANALYZER
9380                                        ;SYSTEM BUS LATCHES ARE ENABLED TO THE STATE ANALYZERS TRDI BUS BITS
9381                                        ;59:0.  BITS WERE ALSO LOADED INTO CONTROL REGISTER 2'S PDAL REGISTER TO
9382                                        ;SET THE SIGNAL PTER3 L IN THE POINTER REGISTER.  WHEN A READ COMMAND IS
9383                                        ;ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER3 L IS ASSERTED LOW,
9384                                        ;TRDI BUS BITS 47:32 ARE READ.  AS A RESULT OF PULSING THE SIGNAL XPI L
9385                                        ;ON THE TARGET EMULATOR MODULE, A PULSE SHOULD HAVE OCCURED ON THE
9386                                        ;SIGNAL EDCK4 H.  A PULSE ON THE SIGNAL EDCK4 H WILL CLOCK THE TARGET
9387                                        ;EMULATOR SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H AND OBTS BITS 3:0
9388                                        ;INTO THE STATE ANALYZER SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).
9389                                        ;AT THE TIME XPI L WAS SET LOW, THE TARGET EMULATOR SIGNAL ASPI L WAS
9390                                        ;ALSO SET LOW, THUS SETTING THE SIGNALS OBTS2 H AND OBTS3 H TO THE HIGH
9391                                        ;STATE, THEREFORE THESE BITS SHOULD BE READ AS ONES ON STATE ANALYZER
9392                                        ;TRDI BITS 34 AND 35.
9393
9394   025400  012737  000014  002316      MOV     #BIT3!BIT2,E6LOAD       ;EXPECT OBTS3 H AND OBTS2 H TO BE ONES
9395   025406  004737  011054              JSR     PC.READE6               ;READ AND CHECK TRDI BITS 39:32
9396   025412  001404                      BEQ     31$                     ;IF OK THEN CONTINUE
```

B 15

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46   PAGE 183
CVCDDB.P11   14-JUN-82 09:54   TEST 7: CHECK TE SIGNALS XSEL1 H, EDSEL0 H, + BTS BITS 3:0 TO ED   SEQ 0183

```
9397   025414                              ERRDF   8,TEEDA1,EO26ER        ;TE TO SA XSEL1,EDSEL0,ADDR 17:16 + BTS 3:0 ERRO
9398   025414   104455                     TRAP    C$ERDF
9399   025416   000010                     .WORD   8
9400   025420   003242                     .WORD   TEEDA1
9401   025422   006212                     .WORD   EO26ER
9402   025424                      31$:    ENDSEG
9403   025424              10000$:
9404   025424   104405                     TRAP    C$ESEG
9405
9406   025426                              ENDTST
9407   025426              L10043:
9408   025426   104401                     TRAP    C$ETST
9409
```

C 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 184
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0184

```
9410                                    .SBTTL  TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40
9411
9412                             ;++
9413                             ;      THIS TEST WILL CHECK THAT DATA LOADED INTO THE TARGET EMULATOR'S EOAI
9414                             ;      REGISTER CAN BE ENABLED TO THE CTL BUS, WHICH IS ON THE SYSTEM BUS,
9415                             ;      AND THAT THE CTL BUS CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM
9416                             ;      BUS CTL 7:0 LATCHES VIA THE TARGET EMULATOR'S CLOCKING SIGNAL "ENCK5 H".
9417                             ;      THE TEST WILL ALSO CHECK THAT THE EOAI REGISTER CAN BE CLOCKED INTO
9418                             ;      THE TARGET EMULATOR'S CTL REGISTER WHEN THE SIGNAL "XCAS L" IS RETURNED
9419                             ;      TO THE DE-ASSERTED STATE AFTER HAVING BEEN ASSERTED.  TO CHECK THAT THE
9420                             ;      EOAI REGISTER WAS CLOCKED INTO THE CTL REGISTER, THE PROGRAM WILL READ
9421                             ;      THE TARGET EMULATOR'S CTL REGISTER AND CHECK THE DATA TO BE THE ONE'S
9422                             ;      COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER.  THE SYSTEM BUS
9423                             ;      CLOCKING SIGNAL "ENCK5 H" IS GENERATED ON THE TARGET EMULATOR MODULE AS
9424                             ;      THE SIGNAL "CKAI H".  THE PROGRAM WILL CAUSE THE SIGNAL "CKAI H" TO BE
9425                             ;      PULSED IN DIFFERENT WAYS DURING THIS TEST.  TO CHECK THAT THE EOAI
9426                             ;      REGISTER DATA CAN BE CLOCKED INTO THE STATE ANALYZER'S SYSTEM BUS CTL
9427                             ;      LATCHES AND THAT A PULSE CAN BE GENERATED ON THE SIGNAL "ENCK5 H", THE
9428                             ;      PROGRAM WILL READ THE CTL 7:0 SYSTEM BUS LATCHES ON THE STATE ANALYZER'S
9429                             ;      TRDI BUS BITS 47:40 AND CHECK THAT THE DATA READ IS THE ONE'S COMPLEMENT
9430                             ;      OF THE DATA LOADED INTO THE TARGET EMULATOR'S EOAI REGISTER.  THE TEST
9431                             ;      WILL ALSO CHECK THAT THE TARGET EMULATOR SIGNALS XSEL1 H, EDSEL0 H,
9432                             ;      ADDR17 H, ADDR16 H AND BTS BITS 3:0 H CAN BE CLOCKED INTO THE STATE
9433                             ;      ANALYZER'S SYSTEM BUS LATCHES BY READING THESE BITS ON STATE ANALYZER'S
9434                             ;      TRDI BUS BITS 39:32.  THE TEST WILL LOAD THE EOAI REGISTER WITH THE
9435                             ;      FOLLOWING DATA PATTERNS 377, 000, 252, 125 AND  314.
9436                             ;--
9437
9438    025430                          BGNTST
9439    025430               T8::
9440
9441    025430  004737  007440          JSR      PC,INITMD               ;INITIALIZE MDE/T-11 SYSTEM MODULES
9442
9443    025434  012701  026576          MOV      #30$,R1                 ;GET ADDRESS OF CTL DATA TABLE
9444
9445    025440               1$:        BGNSEG
9446    025440  104404                  TRAP     C$BSEG
9447
9448                             ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9449                             ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9450
9451    025442  004737  012214          JSR      PC,SLCTTE               ;SELECT TARGET EMULATOR MODULE
9452
9453                             ;SET ADAL REGISTER BITS 13, 10, 9 AND 4 TO A ONE AND PULSE THE SIGNAL
9454                             ;BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT 0.
9455                             ;  ADAL14H = 0                 SELECTS CLOCKING EDGE OF XCAS TO PULSE CKAI H
9456                             ;  ADAL13H = 1                 ALLOWS ATC L TO GO LOW WHEN PPI L SET LOW
9457                             ;  ADAL10H = 1                 ENABLES TE SIGNALS TO MDE/T-11 SYSTEM BUS
9458                             ;  ADAL9H  = 1                 WHEN ADAL10H=1 ENABLES EDCK 5:0 TO SYS BUS
9459                             ;  ADAL4H  = 1                 SETS PAUSE MODE F/F TO RUN MODE WHEN XRAS H PULS
9460
9461    025446  012737  023020  002334  MOV    #ADAL13!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
9462    025454  004737  012766          JSR      PC,BRKRES               ;LOAD ABOVE BITS + PULSE BRKRES L
9463
9464                             ;SELECT THE MODE REGISTER BY SETTING GDAL BITS 2:0 TO 4.  ON A WRITE OR
9465                             ;READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL BE WRITTEN
```

D 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 185
CVCDUB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0185

```
9466                                              ;OR READ.
9467
9468   025460  004537  012234              JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
9469   025464  000004                      .WORD   MODE                    ;SELETC THE MODE REGISTER
9470
9471                                              ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
9472                                              ;ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE.
9473
9474   025466  005037  002346              CLR     T6LOAD                  ;SETUP DATA PATTERN OF ALL ZEROES
9475   025472  004737  011216              JSR     PC,LDRDT6               ;LOAD, READ AND CHECK MODE REGISTER
9476   025476  001405                      BEQ     2$                      ;IF LOADED OK THEN CONTINUE
9477   025500                              ERRDF   12,MODREG,T06ERR        ;MODE REGISTER NOT EQUAL EXPECTED
9478   025500  104455                      TRAP    C$ERDF
9479   025502  000014                      .WORD   12
9480   025504  004002                      .WORD   MODREG
9481   025506  006732                      .WORD   T06ERR
9482   025510                              CKLOOP
9483   025510  104406                      TRAP    C$CLP1
9484
9485                                              ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO
9486                                              ;A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSES ON A WRITE OR READ
9487                                              ;COMMAND TO CONTROL REGISTER 6.  THE EOAI REGISTER WILL BE SELECTED ON
9488                                              ;A READ COMMAND WHEN FDAL REGISTER BIT 0 IS SET TO A ONE.
9489
9490   025512  004537  012234       2$:     JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
9491   025516  000002                      .WORD   FDAL                    ;SELECT EOAI AND FDAL REGISTER
9492
9493                                              ;WRITE THE EOAI REGISTER WITH THE DATA PATTERN FROM THE DATA TABLE. THIS
9494                                              ;DATA PATTERN WILL BE PLACED ONTO THE CTL BUS LATER ON IN THIS TEST.
9495                                              ;FDAL REGISTER BIT 0 WILL BE LOADED WITH A ONE AND ALL OTHER FDAL REGIS-
9496                                              ;TER BITS WILL BE LOADED WITH A ZERO.  FDAL0 H ON A ONE WILL CAUSE THE
9497                                              ;EOAI REGISTER TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD
9498                                              ;OF THE CTL REGISTER.
9499
9500   025520  011137  002346              MOV     (R1),T6LOAD             ;GET DATA PATTERN FROM DATA TABLE
9501   025524  052737  000001  002346      BIS     #FDAL0,T6LOAD           ;SET FDAL0 H TO A ONE
9502   025532  004737  011216              JSR     PC,LDRDT6               ;LOAD, READ AND CHECK EOAI AND FDAL REG
9503   025536  001405                      BEQ     3$                      ;IF LOADED OK THEN CONTINUE
9504   025540                              ERRDF   12,EOAIFD,T06ERR        ;EOAI OR FDAL REGISTER ERROR
9505   025540  104455                      TRAP    C$ERDF
9506   025542  000014                      .WORD   12
9507   025544  004047                      .WORD   EOAIFD
9508   025546  006732                      .WORD   T06ERR
9509   025550                              CKLOOP
9510   025550  104406                      TRAP    C$CLP1
9511
9512                                              ;SELECT THE HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3.  THE
9513                                              ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
9514                                              ;CONTROL REGISTER 6.
9515
9516   025552  004537  012234       3$:     JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
9517   025556  000003                      .WORD   HDAL                    ;SELECT THE HDAL REGISTER
9518
9519                                              ;SET ALL HDAL REGISTER BITS TO A ZERO EXCEPT HDAL REGISTER BIT 2.  HDAL
9520                                              ;REGISTER BIT 2 ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
9521                                              ;TIMING AND CONTROL SIGNALS.
```

E 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 186
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0186

```
9522
9523   025560  012737  000004  002346        MOV    #HDAL2,T6LOAD              ;SETUP BITS TO BE LOADED
9524   025566  004737  011216               JSR    PC,LDRDT6                 ;LOAD, READ AND CHECK HDAL REGISTER
9525   025572  001405                       BEQ    4$                        ;IF LOADED OK THEN CONTINUE
9526   025574                               ERRDF  12,HDALRG,T06ERR          ;HDAL REGISTER NOT EQUAL EXPECTED
9527   025574  104455                       TRAP   C$ERDF
9528   025576  000014                       .WORD  12
9529   025600  003756                       .WORD  HDALRG
9530   025602  006732                       .WORD  T06ERR
9531   025604                               CKLOOP
9532   025604  104406                       TRAP   C$CLP1
9533
9534                                         ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL2 H IN CONTROL
9535                                         ;REGISTER 4.  PULSING THE SIGNAL INVD L ON THE TARGET EMULATOR MODULE
9536                                         ;WILL INITIALIZE ALL THE FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT
9537                                         ;INITIALIZED BY THE SIGNAL BRKRES L.
9538
9539   025606  005037  002340        4$:    CLR    T4LOAD                    ;SETUP TO CLEAR ALL OTHER R/W BITS
9540   025612  004737  012706               JSR    PC,CLRPSM                 ;PULSE INVD L VIA VDAL2 H.
9541
9542                                         ;PERFORM A T-11 TIMING CYCLE BY DOING THE FOLLOWING SEQUENCE:
9543                                         ;  1. SET XRAS H AND XRAS L TO HIGH AND LOW STATE RESPECTIVELY
9544                                         ;  2. SET XCAS H AND XCAS L TO HIGH AND LOW STATE RESPECTIVELY
9545                                         ;  3. SET XPI H AND XPI L TO HIGH AND LOW STATE RESPECTIVELY
9546                                         ;  4. SET XCAS H AND XCAS L TO LOW AND HIGH STATE RESPECTIVELY
9547                                         ;  5. SET XPI H AND XPI L TO LOW AND HIGH STATE RESPECTIVELY
9548                                         ;  6. SET XRAS H AND XCAS H TO LOW AND HIGH STATE RESPECTIVELY
9549                                         ;AS A RESULT OF THE ABOVE TIMING SEQUENCE, A PULSE WILL BE ISSUED ON THE
9550                                         ;SIGNALS EDCK4 H AND EDCK5 H.  A PULSE ON EDCK4 H WILL CLOCK THE SIGNALS
9551                                         ;XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H, AND BTS BITS 3:0 INTO THE STATE
9552                                         ;ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS (TRDI 39:32).  A PULSE ON
9553                                         ;EDCK5 H, WHICH WAS GENERATED BY A PULSE ON THE SIGNAL CKAI H, WILL CLOCK
9554                                         ;CTL BUS BITS 7:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE
9555                                         ;BITS (TRDI 47:40).  THE EOAI REGISTER IS ONLY ENABLED TO THE CTL BUS
9556                                         ;WHEN PPI L IS ASSERTED LOW.  WHEN PPI L IS ASSERTED LOW, THE EOAI
9557                                         ;REGISTER WILL BE ENABLED TO THE CAI BUS VIA THE SIGNAL ATC L.  THE
9558                                         ;CAI BUS WILL BE ENABLED TO THE EIAI BUS UNCONDITIONALLY AND THE EIAI
9559                                         ;BUS WILL BE ENABLED TO THE CTL BUS VIA THE SIGNAL ADAL10 H.  THE
9560                                         ;SIGNALS CKAI H AND EDCK5 H WILL GO FROM A HIGH STATE TO A LOW STATE AND
9561                                         ;BACK TO A HIGH STATE WEHN THE SIGNAL XCAS L IS PULSED IN THE ABOVE
9562                                         ;TIMING SEQUENCE.  WHEN XCAS L IS RETURNED TO THE HIGH STATE, THE CTL
9563                                         ;BUS DATA WILL BE CLOCKED INTO THE TARGET EMULATORS CTL REGISTER AND INTO
9564                                         ;THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS.  THE DATA CLOCKED
9565                                         ;INTO THE TARGET EMULATORS CTL REGISTER AND THE STATE ANALYZERS SYSTEM
9566                                         ;BUS LATCHES WILL BE THE ONES COMPLEMENT OF THE DATA LOADED INTO THE
9567                                         ;EOAI REGISTER AT THE BEGINNING OF THIS TEST.
9568
9569   025616  004737  012300               JSR    PC,XRASH                  ;SET XRAS H HIGH AND XRAS L LOW
9570   025622  004737  012404               JSR    PC,XCASH                  ;SET XCAS H HIGH AND XCAS L LOW
9571   025626  004737  012510               JSR    PC,XPIH                   ;SET XPI H HIGH AND XPI L LOW
9572   025632  004737  012436               JSR    PC,XCASL                  ;SET XCAS H LOW AND XCAS L HIGH
9573   025636  004737  012542               JSR    PC,XPIL                   ;SET XPI H LOW AND XPI L HIGH
9574   025642  004737  012332               JSR    PC,XRASL                  ;SET XRAS H LOW AND XRAS L HIGH
9575
9576                                         ;READ VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A ONE
9577                                         ;AS A RESULT OF THE ABOVE TIMING SEQUENCE.
```

F 15

HARDWARE TESTS MACY11 30A(1052)   16-JUN-82 13:46 PAGE 187
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0187

```
9578
9579  025646  012737  000020  002342       MOV    #VDAL4,T4GOOD        ;EXPECT EDEOC H TO BE SET TO A ONE
9580  025654  004737  011200               JSR    PC,READT4           ;READ AND CHECK VDAL REGISTER
9581  025660  001405                        BEQ    5$                  ;IF OK THEN CONTINUE
9582  025662                                ERRDF  11,VDALRG,T4EROR    ;VDAL REGISTER NOT EQUAL EXPECTED
9583  025662  104455                        TRAP   C$ERDF
9584  025664  000013                        .WORD  11
9585  025666  003710                        .WORD  VDALRG
9586  025670  006716                        .WORD  T4EROR
9587  025672                                CKLOOP
9588  025672  104406                        TRAP   C$CLP1
9589
9590                                         ;SELECT THE CTL/EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
9591                                         ;TO A 2.  THE CTL AND FDAL REGISTER WILL BE ADDRESSED ON A READ COMMAND
9592                                         ;TO CONTROL REGISTER 6 WHEN FDAL0 H IS SET TO A ZERO.
9593
9594  025674  112737  000002  002324  5$:   MOVB   #FDAL,T0LOAD        ;GET GDAL BITS TO BE LOADED
9595  025702  004737  011100               JSR    PC,LDRDT0           ;LOAD, READ AND CHECK GDAL REGISTER
9596  025706  001405                        BEQ    6$                  ;IF LOADED OK THEN CONTINUE
9597  025710                                ERRDF  9,GDALRG,T0EROR     ;GDAL REGISTER NOT EQUAL EXPECTED
9598  025710  104455                        TRAP   C$ERDF
9599  025712  000011                        .WORD  9
9600  025714  003640                        .WORD  GDALRG
9601  025716  006666                        .WORD  T0EROR
9602  025720                                CKLOOP
9603  025720  104406                        TRAP   C$CLP1
9604
9605                                         ;WRITE ALL ZEROES INTO THE FDAL REGISTER.  THE EOAI REGISTER WILL NOT
9606                                         ;BE CHANGED AT THIS POINT IN TIME.  WHEN FDAL0 H IS SET TO A ZERO, THE
9607                                         ;CTL REGISTER WILL BE READ ON A READ COMMAND TO CONTROL REGISTER 6
9608                                         ;INSTEAD OF THE EOAI REGISTER.
9609
9610  025722  112777  000000  154262  6$:   MOVB   #0,@REG6            ;WRITE 0'S INTO FDAL REGISTER ONLY
9611
9612                                         ;READ THE CTL AND FDAL REGISTER TO CHECK THAT THE DATA READ IS THE 1'S
9613                                         ;COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER AT THE BEGINNING
9614                                         ;OF THIS TEST.  THE CTL BUS DATA WAS CLOCKED INTO THE CTL REGISTER WHEN
9615                                         ;THE SIGNAL XCAS L WAS SET TO THE HIGH STATE AFTER HAVING BEEN SET LOW.
9616
9617  025730  016137  000002  002346        MOV    2(R1),T6LOAD        ;GET 1'S COMPLEMENT OF EOAI REG DATA
9618  025736  004737  011224               JSR    PC,READT6           ;READ CTL AND FDAL REGISTER
9619  025742  001405                        BEQ    7$                  ;IF DATA OK THEN CONTINUE
9620  025744                                ERRDF  12,CTLFDL,T06ERR    ;CTL 7:0 OR FDAL 7:0 REG ERROR
9621  025744  104455                        TRAP   C$ERDF
9622  025746  000014                        .WORD  12
9623  025750  004106                        .WORD  CTLFDL
9624  025752  006732                        .WORD  T06ERR
9625  025754                                CKLOOP
9626  025754  104406                        TRAP   C$CLP1
9627
9628                                         ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9629                                         ;REGISTER 0 WITH THE USER DEFINBED DEVICE NUMBER.
9630
9631  025756  004737  012144          7$:   JSR    PC,SLCTED           ;SELECT STATE ANALYZER MODULE
9632
9633                                         ;SET THE SIGNAL TRSL2 L TO THE LOW STATE BY SETTING CDAL3 H TO A ONE AND
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9634                                                    ;CDAL2 H TO A ZERO IN CONTROL REGISTER 0.  THE SIGNAL TRSL2 L WILL ENABLE
9635                                                    ;THE STATE ANALYZER'S SYSTEM BUS LATCHES TO TRDI BUS BITS 59:0.
9636
9637   025762  112737  000010  002272       MOVB   #CDAL3,E0LOAD              ;SETUP CDAL REGISTER BITS TO LOAD
9638   025770  004737  010700                JSR    PC,LDRDE0                 ;LOAD, READ AND CHECK CDAL REGISTER
9639   025774  001405                        BEQ    8$                        ;IF LOADED OK THEN CONTINUE
9640   025776                                ERRDF  5,CDALRG,E0EROR           ;CDAL REGISTER NOT EQUAL EXPECTED
9641   025776  104455                        TRAP   C$ERDF
9642   026000  000005                        .WORD  5
9643   026002  003010                        .WORD  CDALRG
9644   026004  006146                        .WORD  E0EROR
9645   026006                                CKLOOP
9646   026006  104406                        TRAP   C$CLP1
9647
9648                                                    ;ASSERT THE SIGNAL PTER3 L IN THE POINTER REGISTER BY LOADING THE
9649                                                    ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.
9650
9651   026010  004537  012164           8$:  JSR    R5,LDPDAL                 ;LOAD AND CHECK PDAL REGISTER
9652   026014  000003                        .WORD  PTER3                     ;SETUP TO READ TRDI BUS BITS 47:32
9653
9654                                                    ;AS A RESULT OF PERFORMING A NORMAL T-11 TIMING CYCLE, A PULSE SHOULD
9655                                                    ;HAVE OCCURED ON THE SIGNAL EDCK4 H AND A PULSE SHOULD HAVE OCCURED
9656                                                    ;ON THE SIGNAL EDCK5 H.  A PULSE ON EDCK4 H WILL CLOCK THE TARGET
9657                                                    ;EMULATOR SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H, AND BTS BITS
9658                                                    ;3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS.  THESE
9659                                                    ;BITS WILL BE READ ON TRDI BUS BITS 39:32.  A PULSE ON EDCK5 H WILL
9660                                                    ;CLOCK THE TARGET EMULATORS CTL BUS INTO THE STATE ANALYZERS SYSTEM BUS
9661                                                    ;LATCHES FOR THESE BITS.  THESE BITS WILL BE READ ON TRDI BUS BITS 47:40.
9662                                                    ;A PULSE ON THE SIGNAL EDCK5 H, VIA THE SIGNAL CKAI H WILL CLOCK THE
9663                                                    ;CTL BUS DATA, WHICH HAS EOAI REGISTER DATA ENABLED TO IT VIA THE CAI
9664                                                    ;AND EIAI BUS, INTO THE STATE ANALYZERS SYTEM BUS LATCHES.  THE DATA
9665                                                    ;READ ON TRDI BUS BITS 47:40 WILL BE THE ONES COMPLEMENT OF THE DATA
9666                                                    ;LOADED INTO THE TARGET EMULATORS EOAI REGISTER.  THE SIGNAL BTS0 H
9667                                                    ;SHOULD BE SET TO A ONE ON THE TARGET EMULATOR MODULE, THEREFORE, TRDI
9668                                                    ;BIT 32 SHOULD BE READ AS A ONE ALSO.
9669
9670   026016  016137  000002  002316       MOV    2(R1),E6LOAD              ;GET 1'S COMP OF EOAI REG DATA LOADED
9671   026024  052737  000001  002316       BIS    #BIT0,E6LOAD              ;EXPECT BTS0 H TO BE SET TO A ONE
9672   026032  004737  011054                JSR    PC,READE6                ;READ AND CHECK TRDI BUS BITS 47:32
9673   026036  001405                        BEQ    9$                        ;IF DATA OK THEN CONTINUE
9674   026040                                ERRDF  8,TEEDCT,E026ER           ;TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:40 ERROR
9675   026040  104455                        TRAP   C$ERDF
9676   026042  000010                        .WORD  8
9677   026044  003344                        .WORD  TEEDCT
9678   026046  006212                        .WORD  E026ER
9679   026050                                CKLOOP
9680   026050  104406                        TRAP   C$CLP1
9681
9682                                                    ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9683                                                    ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9684
9685   026052  004737  012214           9$:  JSR    PC,SLCTTE                 ;SELECT THE TARGET EMULATOR MODULE
9686
9687                                                    ;LOAD, READ AND CHECK THE EOAI AND FDAL REGISTER.  THE FDAL REGISTER
9688                                                    ;WAS SELECTED IN THE PREVIOUS SELECTION OF THE TARGET EMULATOR MODULE.
9689                                                    ;THE EOAI REGISTER WILL BE LOADED WITH THE ONES COMPLEMENT OF THE DATA
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H 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 189
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0189

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9690                                              ;LOADED INTO IT IN THE PREVIOUS SELECTION OF THE TARGET EMULATOR MODULE.
9691
9692   026056  016137  000002  002346        MOV     2(R1),T6LOAD            ;GET THE DATA FROM THE DATA TABLE
9693   026064  052737  000001  002346        BIS     #FDAL0,T6LOAD           ;SELECT EOAI REGISTER TO BE READ
9694   026072  004737  011216                JSR     PC,LDRDT6               ;LOAD, READ AND CHECK EOAI + FDAL REG
9695   026076  001405                         BEQ     10$                    ;IF LOADED OK THEN CONTINUE
9696   026100                                 ERRDF   12,EOAIFD,T06ERR        ;EOAI 7:0 OF FDAL 7:0 REG ERROR
9697   026100  104455                         TRAP    C$ERDF
9698   026102  000014                         .WORD   12
9699   026104  004047                         .WORD   EOAIFD
9700   026106  006732                         .WORD   T06ERR
9701   026110                                 CKLOOP
9702   026110  104406                         TRAP    C$CLP1
9703
9704                                              ;SET ADAL REGISTER BITS 15 AND 14 TO ONES.  WHEN THESE TWO BITS ARE SET
9705                                              ;TO ONES, THE SIGNALS CKAI H AND EDCK5 H WILL BE SET HIGH WHEN THE
9706                                              ;SIGNAL XCAS H IS SET HIGH.  THE SIGNAL EDCK5 H GOING FROM A LOW TO A
9707                                              ;HIGH STATE WILL CLOCK THE CTL BUS INTO THE STATE ANALYZERS SYSTEM BUS
9708                                              ;LATCHES FOR THOSE BITS.
9709
9710   026112  052737  140000  002334  10$:   BIS     #ADAL15!ADAL14,T2LOAD   ;SETUP ADAL BITS TO BE LOADED
9711   026120  004737  011140                JSR     PC,LDRDT2               ;LOAD, READ AND CHECK ADAL REGISTER
9712   026124  001405                         BEQ     11$                    ;IF LOADED OK THEN CONTINUE
9713   026126                                 ERRDF   10,ADALRG,T2EROR        ;ADAL REGISTER NOT EQUAL EXPECTED
9714   026126  104455                         TRAP    C$ERDF
9715   026130  000012                         .WORD   10
9716   026132  003664                         .WORD   ADALRG
9717   026134  006702                         .WORD   T2EROR
9718   026136                                 CKLOOP
9719   026136  104406                         TRAP    C$CLP1
9720
9721                                              ;SELECT THE HDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 3.  ON
9722                                              ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL
9723                                              ;BE WRITTEN OR READ.
9724
9725   026140  004537  012234          11$:   JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
9726   026144  000003                         .WORD   HDAL                    ;SELECT THE HDAL REGISTER
9727
9728                                              ;SET THE SIGNALS XR/WHB L AND XR/WLB L TO THE LOW STATE BY SETTING HDAL
9729                                              ;REGISTER BITS 4 AND 3 TO ONES.  SETTING THESE TWO SIGNALS LOW WILL
9730                                              ;CAUSE THE SIGNAL BTS0 H TO GO FROM A HIGH TO A LOW STATE.  THIS IS DONE
9731                                              ;TO CHECK THAT A PULSE IS ISSUED ON THE SIGNAL EDCK4 H WHEN THE SIGNAL
9732                                              ;XPI L IS SET TO THE LOW STATE FROM THE HIGH STATE.
9733
9734   026146  012737  000034  002346        MOV     #HDAL4!HDAL3!HDAL2,T6LOAD  ;SETUP BITS TO BE LOADED
9735   026154  004737  011216                JSR     PC,LDRDT6               ;LOAD, READ AND CHECK HDAL REGISTER
9736   026160  001405                         BEQ     12$                    ;IF LOADED OK THEN CONTINUE
9737   026162                                 ERRDF   12,HDALRG,T06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
9738   026162  104455                         TRAP    C$ERDF
9739   026164  000014                         .WORD   12
9740   026166  003756                         .WORD   HDALRG
9741   026170  006732                         .WORD   T06ERR
9742   026172                                 CKLOOP
9743   026172  104406                         TRAP    C$CLP1
9744
9745                                              ;SET THE SIGNALS XPI L AND PPI L TO THE LOW STATE BY SETTING HDAL REGIS-
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I 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 190
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0190

```
9746                                    ;TER BIT 15 TO A ONE.  WHEN PPI L IS SET LOW, THE SIGNAL ATC L WILL BE
9747                                    ;ASSERTED LOW THUS ENABLING THE EOAI REGISTER TO THE CAI BUS.  THE CAI
9748                                    ;BUS WILL BE ENABLED TO THE EIAI BUS UNCONDITIONALLY AND THE EIAI BUS
9749                                    ;WILL BE ENABLED TO THE CTL BUS BY ADAL REGISTER BIT 10 BEING SET TO A
9750                                    ;ONE.  WHEN XPI L IS SET LOW, THE SIGNAL EDCK4 H WILL GO FROM A LOW TO
9751                                    ;A HIGH STATE THUS CLOCKING THE SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H,
9752                                    ;ADDR16 H AND BTS BITS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES
9753                                    ;FOR THESE BITS (TRDI BUS BITS 39:32).
9754
9755  026174  004737  012510    12$:    JSR     PC,XPIH                  ;SET XPI L AND PPI L TO LOW STATE
9756
9757                                    ;SET THE SIGNAL XCAS H TO THE HIGH STATE AND THE SIGNAL XCAS L TO THE
9758                                    ;LOW STATE.  WHEN XCAS H IS SET HIGH, THE SIGNALS CKAI H AND EDCK5 H
9759                                    ;WILL GO FROM A LOW TO A HIGH STATE, THUS CLOCKING THE CTL 7:0 BUS INTO
9760                                    ;THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS (TRDI BUS BITS 47:40).
9761
9762  026200  004737  012404            JSR     PC,XCASH                 ;SET XCAS H HIGH AND XCAS L LOW
9763
9764                                    ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H WENT TO A ZERO
9765                                    ;WHEN XCAS L WAS ASSERTED LOW.
9766
9767  026204  005037  002342            CLR     T4GOOD                   ;EXPECT ALL VDAL BITS TO BE A ZERO
9768  026210  004737  011200            JSR     PC,READT4                ;READ AND CHECK VDAL REGISTER
9769  026214  001405                    BEQ     13$                      ;IF ALL ZERO THEN CONTINUE
9770  026216                            ERRDF   11,VDALRG,T4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
9771  026216  104455                    TRAP    C$ERDF
9772  026220  000013                    .WORD   11
9773  026222  003710                    .WORD   VDALRG
9774  026224  006716                    .WORD   T4EROR
9775  026226                            CKLOOP
9776  026226  104406                    TRAP    C$CLP1
9777
9778                                    ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9779                                    ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9780
9781  026230  004737  012144    13$:    JSR     PC,SLCTED                ;SELECT THE STATE ANALYZER MODULE
9782
9783                                    ;IN THE PREVIOUS SELECTION OF THE STATE ANALYZER MODULE, THE SIGNAL
9784                                    ;TRSL2 L WAS ASSERTED LOW TO ENABLE THE STATE ANALYZERS SYSTEM BUS
9785                                    ;LATCHES ONTO TRDI BUS BITS 59:0, AND PTER3 L WAS ASSERTED LOW IN
9786                                    ;THE POINTER REGISTER SO THAT TRDI BUS BITS 47:32 COULD BE READ ON A
9787                                    ;READ COMMAND TO CONTROL REGISTER 6.  THIS NEXT SECTION WILL READ TRDI
9788                                    ;BUS BITS 47:32 TO CHECK THAT THE TARGET EMULATORS CTL BUS BITS 7:0 AND
9789                                    ;THE SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H, AND BTS BITS 3:0
9790                                    ;WERE CLOCKED INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE
9791                                    ;BITS VIA THE TARGET EMULATORS SIGNALS EDCK5 H AND EDCK4 H.  WHEN THE
9792                                    ;CTL BUS IS READ ON TRDI BUS BITS 47:40, THE DATA WILL BE THE ONES
9793                                    ;COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER IN THE PREVIOUS
9794                                    ;SELECTION OF THE TARGET EMULATOR MODULE.  THE SIGNAL BTS0 H SHOULD BE
9795                                    ;READ AS A ZERO ON TRDI BUS BIT 32.
9796
9797  026234  011137  002316            MOV     (R1),E6LOAD              ;GET 1'S COMP OF EOAI DATA LOADED
9798  026240  004737  011054            JSR     PC,READE6                ;READ AND CHECK TRDI BUS BITS 47:32
9799  026244  001405                    BEQ     14$                      ;IF DATA OK THEN CONTINUE
9800  026246                            ERRDF   8,TEEDCT,E026ER          ;TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:32 ERROR
9801  026246  104455                    TRAP    C$ERDF
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J 15

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46 PAGE 191
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0191

```
9802   026250  0G0010                              .WORD    8
9803   026252  003344                              .WORD    TEEDCT
9804   026254  006212                              .WORD    E026ER
9805   026256                              CKLOOP
9806   026256  104406                              TRAP     C$CLP1
9807
9808                                       ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
9809                                       ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9810
9811   026260  004737  012214       14$:          JSR      PC,SLCTTE                  ;SELECT THE TARGET EMULATOR MODULE
9812
9813                                       ;SET THE SIGNAL XCAS H TO THE LOW STATE AND THE SIGNAL XCAS L TO THE
9814                                       ;HIGH STATE.  SETTING XCAS L TO THE HIGH STATE WILL CLOCK THE CTL BUS
9815                                       ;INTO THE CTL REGISTER.  ALSO SET THE SIGNALS XPI L AND PPI L TO THE
9816                                       ;HIGH STATE.  SETTING PPI L TO THE HIGH STATE WILL DISABLE THE EOAI
9817                                       ;REGISTER TO THE CAI BUS.
9818
9819   026264  004737  012436              JSR      PC,XCASL                  ;SET XCAS H LOW AND XCAS L HIGH
9820   026270  004737  012542              JSR      PC,XPIL                   ;SET XPI L HIGH AND PPI L HIGH
9821
9822                                       ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS SET TO
9823                                       ;A ONE AS A RESULT OF XCAS L BEING SET TO THE HIGH STATE.
9824
9825   026274  012737  000020  002342      MOV      #VDAL4,T4GOOD             ;EXPECT EDEOC H TO BE SET TO A ONE
9826   026302  004737  011200              JSR      PC,READT4                 ;READ AND CHECK VDAL REGISTER
9827   026306  001405                       BEQ      15$                       ;IF LOADED OK THEN CONTINUE
9828   026310                               ERRDF    11,VDALRG,T4EROR          ;VDAL REGISTER NCT EQUAL EXPECTED
9829   026310  104455                       TRAP     C$ERDF
9830   026312  000013                       .WORD    11
9831   026314  003710                       .WORD    VDALRG
9832   026316  006716                       .WORD    T4EROR
9833   026320                               CKLOOP
9834   026320  104406                       TRAP     C$CLP1
9835
9836                                       ;SELECT THE CTL/EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
9837                                       ;TO A 2.  THE CTL AND FDAL REGISTER WILL BE ADDRESSED ON A READ COMMAND
9838                                       ;COMMAND TO CONTROL REGISTER 6 WHEN FDAL REGISTER BIT 0 IS A ZERO.
9839
9840   026322  112737  000002  002324 15$:  MOVB     #FDAL,TOLOAD             ;GET GDAL BITS TO BE LOADED
9841   026330  004737  011100              JSR      PC,LDRDT0                 ;LOAD, READ AND CHECK GDAL REGISTER
9842   026334  001405                       BEQ      16$                       ;IF LOADED OK THEN CONTINUE
9843   026336                               ERRDF    9,GDALRG,TOEROR           ;GDAL REGISTER NOT EQUAL EXPECTED
9844   026336  104455                       TRAP     C$ERDF
9845   026340  000011                       .WORD    9
9846   026342  003640                       .WORD    GDALRG
9847   026344  006666                       .WORD    TOEROR
9848   026346                               CKLOOP
9849   026346  104406                       TRAP     C$CLP1
9850
9851                                       ;WRITE ALL ZEROES INTO THE FDAL REGISTER.  THE EOAI REGISTER DATA WILL
9852                                       ;NOT BE CHANGED ON THIS WRITE COMMAND.  WHEN FDAL0 H IS SET TO A ZERO,
9853                                       ;THE CTL AND FDAL REGISTER WILL BE READ ON A READ COMMAND TO CONTROL
9854                                       ;REGISTER 6 INSTEAD OF THE EOAI AND FDAL REGISTER.
9855
9856   026350  112777  000000  153634 16$:  MOVB     #0,@REG6                 ;LOAD FDAL REG WITH ALL ZEROES
9857
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K 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 192
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0192

```
9858                                          ;READ THE CTL AND FDAL REGISTER TO CHECK THAT THE DATA READ FROM THE
9859                                          ;CTL REGISTER IS THE ONES COMPLEMENT OF THE DATA LOADED INTO THE EOAI
9860                                          ;REGISTER.  THE CTL BUS DATA WAS CLOCKED INTO THE CTL REGISTER WHEN THE
9861                                          ;SIGNAL XCAS L WAS SET FROM A LOW TO A HIGH STATE.
9862
9863  026356  011137  002346             MOV     (R1),T6LOAD            ;GET 1'S COMP OF EOAI REGISTER DATA
9864  026362  004737  011224             JSR     PC,READT6             ;READ CTL AND FDAL REGISTER DATA
9865  026366  001405                      BEQ     17$                   ;IF DATA OK THEN CONTINUE
9866  026370                              ERRDF   12,CTLFDL,T06ERR      ;CTL 7:0 OR FDAL 7:0 REGISTER ERROR
9867  026370  104455                      TRAP    C$ERDF
9868  026372  000014                      .WORD   12
9869  026374  004106                      .WORD   CTLFDL
9870  026376  006732                      .WORD   T06ERR
9871  026400                              CKLOOP
9872  026400  104406                      TRAP    C$CLP1
9873
9874                                          ;LOAD, READ AND CHECK EOAI AND FDAL REGISTER.  THE ECAI REGISTER WILL
9875                                          ;BE LOADED WITH A DATA PATTERN OF 314.  THE FDAL REGISTER WILL BE LOADED
9876                                          ;WITH A DATA PATTERN OF 001.  WHEN FDALO H IS SET TO A ONE AND A READ
9877                                          ;COMMAND IS USSUED TO CONTROL REGISTER 6, THE EOAI AND FDAL REGISTER
9878                                          ;WILL BE READ INSTEAD OF THE CTL AND FDAL REGISTERS.
9879
9880  026402  012737  146001  002346  17$:  MOV     #146001,T6LOAD        ;GET EOAI AND FDAL DATA PATTERNS
9881  026410  004737  011216             JSR     PC,LDRDT6             ;LOAD, READ AND CHECK EOAI AND FDAL
9882  026414  001405                      BEQ     18$                   ;IF LOADED OK THEN CONTINUE
9883  026416                              ERRDF   12,EOAIFD,T06ERR      ;EOAI 7:0 OR FDAL 7:0 REGISTER ERROR
9884  026416  104455                      TRAP    C$ERDF
9885  026420  000014                      .WORD   12
9886  026422  004047                      .WORD   EOAIFD
9887  026424  006732                      .WORD   T06ERR
9888  026426                              CKLOOP
9889  026426  104406                      TRAP    C$CLP1
9890
9891                                          ;SET ADAL REGISTER BIT 15 TO A ZERO AND LEAVE BIT 14 SET TO A ONE.  WHEN
9892                                          ;ADAL BIT 15 IS SET TO A ZERO AND BIT 14 IS SET TO A ONE AND A PULSE IS
9893                                          ;ISSUED ON THE SIGNAL XRAS H, A PULSE WILL BE ISSUED ON THE SIGNAL RASP L
9894                                          ;WHICH WILL CAUSE A PULSE TO BE ISSUED ON THE SIGNALS CKAI H AND EDCK5 H.
9895                                          ;A PULSE ON THE SIGNAL EDCK5 H WILL CLOCK THE CTL BUS DATA INTO THE STATE
9896                                          ;ANALYZERS SYSTEM BUS LATCHES FOR THESE BITS (TRDI 47:40).
9897
9898  026430  042737  100000  002334  18$:  BIC     #ADAL15,T2LOAD        ;SETUP TO CLEAR ADAL BIT 15
9899  026436  004737  011140             JSR     PC,LDRDT2             ;LOAD, READ AND CHECK ADAL REGISTER
9900  026442  001405                      BEQ     19$                   ;IF LOADED OK THEN CONTINUE
9901  026444                              ERRDF   10,ADALRG,T2EROR      ;ADAL REGISTER NOT EQUAL EXPECTED
9902  026444  104455                      TRAP    C$ERDF
9903  026446  000012                      .WORD   10
9904  026450  003664                      .WORD   ADALRG
9905  026452  006702                      .WORD   T2EROR
9906  026454                              CKLOOP
9907  026454  104406                      TRAP    C$CLP1
9908
9909                                          ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  ON A WRITE
9910                                          ;OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE
9911                                          ;WRITTEN OR READ.
9912
9913  026456  004537  012234             19$:  JSR     R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
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L 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 193
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0193

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9914    026462  000003                              .WORD   HDAL                    ;SELECT THE HDAL REGISTER
9915
9916                                                ;SET THE SIGNALS XR/WHB L AND XR/WLB L BACK TO THE HIGH STATE BY SETTING
9917                                                ;HDAL REGISTER BITS 4 AND 3 TO A ZERO.  THIS WILL CAUSE THE SIGNAL BTS0 H
9918                                                ;TO BE SET TO THE HIGH STATE (1).
9919
9920    026464  012737  000004  002346              MOV     #HDAL2,T6LOAD           ;SETUP BIT TO BE LOADED
9921    026472  004737  011216                      JSR     PC,LDRDT6               ;LOAD, READ AND CHECK HDAL REGISTER
9922    026476  001405                              BEQ     20$                     ;IF LOADED OK THEN CONTINUE
9923    026500                                      ERRDF   12,HDALRG,T06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
9924    026500  104455                              TRAP    C$ERDF
9925    026502  000014                              .WORD   12
9926    026504  003756                              .WORD   HDALRG
9927    026506  006732                              .WORD   T06ERR
9928    026510                                      CKLOOP
9929    026510  104406                              TRAP    C$CLP1
9930
9931                                                ;SET THE SIGNALS XPI L AND PPI L TO THE LOW STATE BY SETTING HDAL REGISTER
9932                                                ;BIT 15 TO A ONE.  WHEN XPI L IS SET TO THE LOW STATE, THE SIGNAL EDCK4 H
9933                                                ;WILL BE SET HIGH THUS CLOCKING THE SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H,
9934                                                ;ADDR16 H, AND BTS BITS 3:0 INTO THE STATE ANALYZERS SYSTEM BUS LATCHES
9935                                                ;FOR THESE BITS (TRDI 39:32).  SETTING THE SIGNAL PPI L TO THE LOW STATE
9936                                                ;WILL CAUSE THE SIGNAL ATC L TO BE SET LOW WHICH WILL ENABLE THE EOAI
9937                                                ;REGISTER TO THE CAI BUS.  THE CAI BUS WILL BE ENABLED TO THE EIAI BUS
9938                                                ;AND TO THE CTL BUS VIA ADAL10 H.
9939
9940    026512  004737  012510      20$:            JSR     PC,XPIH                 ;SET XPI L AND PPI L TO LOW STATE
9941
9942                                                ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL REGISTER BIT 12.
9943                                                ;WHEN XRAS H IS PULSED, A PULSE WILL OCCUR ON THE SIGNAL RASP L.  WHEN
9944                                                ;ADAL BIT 15 IS A ZERO AND ADAL BIT 14 IS A ONE AND A PULSE IS ISSUED
9945                                                ;ON THE SIGNAL RASP L, A PULSE WILL OCCUR ON THE SIGNAL CKAI H WHICH WILL
9946                                                ;CAUSE A PULSE TO OCCUR ON THE SIGNAL EDCK5 H.  A PULSE ON THE SIGNAL
9947                                                ;EDCK5 H WILL CLOCK THE TARGET EMULATORS CTL BUS INTO THE STATE ANALYZERS
9948                                                ;SYSTEM BUS LATCHES FOR THESE BITS (TRDI BITS 47:40).
9949
9950    026516  004737  012266                      JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
9951
9952                                                ;DISABLE THE EOAI REGISTER FROM THE CTL BUS BY SETTING THE SIGNALS XPI L
9953                                                ;AND PPI L TO THE HIGH STATE BY SETTING HDAL REGISTER BIT 15 TO A ZERO.
9954
9955    026522  004737  012542                      JSR     PC,XPIL                 ;SET XPI L AND PPI L TO HIGH STATE
9956
9957                                                ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
9958                                                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
9959
9960    026526  004737  012144                      JSR     PC,SLCTED               ;SLECT THE STATE ANALYZER MODULE
9961
9962                                                ;IN A PREVIOUS SELECTION OF THE STATE ANALYZER MODULE, THE SIGNAL
9963                                                ;TRSL2 L WAS ASSERTED LOW TO ENABLE THE STATE ANALYZERS SYSTEM BUS
9964                                                ;LATCHES ONTO TRDI BUS BITS 59:0, AND PTER3 L WAS ASSERTED LOW IN
9965                                                ;THE POINTER REGISTER SO THAT TRDI BUS BITS 47:32 COULD BE READ ON A
9966                                                ;READ COMMAND TO CONTROL REGISTER 6.  THIS NEXT SECTION WILL READ TRDI
9967                                                ;BUS BITS 47:32 TO CHECK THAT THE TARGET EMULATORS CTL BUS BITS 7:0 AND
9968                                                ;THE SIGNALS XSEL1 H, EDSEL0 H, ADDR17 H, ADDR16 H, AND BTS BITS 3:0
9969                                                ;WERE CLOCKED INTO THE STATE ANALYZERS SYSTEM BUS LATCHES FOR THESE
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M 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 194
CVCDDB.P11   14-JUN-82 09:54   TEST 8: CHECK TE SIGNALS CTL 7:0 TO SA TRDI BITS 47:40   SEQ 0194

```
9970                                              ;BITS VIA THE TARGET EMULATORS SIGNALS EDCK5 H AND EDCK4 H.  WHEN THE
9971                                              ;CTL BUS IS READ ON TRDI BUS BITS 47:40, THE DATA WILL BE THE ONES
9972                                              ;COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER IN THE PREVIOUS
9973                                              ;SELECTION OF THE TARGET EMULATOR MODULE.  THE SIGNAL BTS0 H SHOULD BE
9974                                              ;READ AS A ONE ON TRDI BUS BIT 32.
9975
9976  026532  012737  031401  002316       MOV    #031401,E6LOAD       ;GET 1'S COMP OF EOAI REG DATA
9977  026540  004737  011054               JSR    PC,READE6           ;READ AND CHECK TRDI BITS 47:32
9978  026544  001404                        BEQ    21$                 ;IF LOADED OK THEN CONTINUE
9979  026546                                ERRDF  8,TEEDCT,E026ER     ;TE CTL BUS 7:0 TO SA TRDI BUS BITS 47:32 ERROR
9980  026546  104455                        TRAP   C$ERDF
9981  026550  000010                        .WORD  8
9982  026552  003344                        .WORD  TEEDCT
9983  026554  006212                        .WORD  E026ER
9984  026556                        21$:    ENDSEG
9985  026556                        10000$:
9986  026556  104405                        TRAP   C$ESEG
9987  026560  062701  000004               ADD    #4,R1               ;UPDATE TABLE POINTER TO NEXT DATA SET
9988  026564  022711  177777               CMP    #-1,(R1)            ;CHECK IF END OF TABLE
9989  026570  001407                        BEQ    31$                 ;IF YES THEN EXIT
9990  026572  000137  025440               JMP    1$                  ;ELSE LOAD NEXT DATA SET INTO EOAI REG
9991
9992  026576  177400               30$:    .WORD  177400
9993  026600  000000                        .WORD  000000
9994  026602  125000                        .WORD  125000
9995  026604  052400                        .WORD  052400
9996  026606  177777                        .WORD  177777              ;TABLE TERMINATOR
9997
9998  026610                        31$:    ENDTST
9999  026610                        L10044:
10000 026610  104401                        TRAP   C$ETST
10001
```

N 15

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 195
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEG 0195

```
10002                              .SBTTL TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT
10003
10004                        ;++
10005                              THIS TEST WILL CHECK THAT THE MEMORY SIMULATOR 'RDV' FLIP-FLOP CAN BE
10006                              CLEARED WHEN A READ OPERATION IS EXECUTED FROM THE TARGET EMULATOR
10007                              MODULE TO AN ADDRESS WHICH IS MAPPED IN THE MEMROY SIMULATOR'S MAP
10008                              PROTECTION RAM TO INHIBIT READS AND WRITES.  THE 'RDV' FLIP-FLOP WILL
10009                              BE CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL 'RDE H' BEING ASSERTED
10010                              LOW AND A PULSE ON THE SIGNAL 'RDS H'.  THE SIGNAL 'RDS H' WILL BE
10011                              PULSED WHEN THE MEMORY SIMULATOR SIGNAL 'CTS H' IS ASSERTED HIGH AND
10012                              A PULSE IS ISSUED ON THE TARGET EMULATOR SIGNAL 'READ H'.  A PULSE
10013                              WILL OCCUR ON THE SIGNAL 'READ H' WHEN A T-11 READ OPERATION IS BEING
10014                              EXECUTED BY THE TARGET EMULATOR MODULE.  THE PROGRAM WILL CHECK THAT THE
10015                              MEMORY SIMULATOR SIGNAL 'MSBRK H' IS ASSERTED HIGH AS A RESULT OF THE
10016                              'RDV' FLIP-FLOP BEING CLEARED.  THE PROGRAM WILL CHECK THE TARGET
10017                              EMULATOR MODULES 'MEMBRK' FLIP-FLOP TO BE CLEARED AND THEN CAUSE A
10018                              PULSE TO BE ISSUED ON TARGET EMULATOR SIGNAL 'XRAS H'.  THE PROGRAM WILL
10019                              NOW CHECK THE 'MEMBRK' FLIP-FLOP TO BE SET TO A ONE AS A RESULT OF A
10020                              PULSE ON 'XRAS H' AND THE MEMORY SIMULATOR'S SYSTEM BUS SIGNAL 'MSBRK H'
10021                              BEING ASSERTED HIGH.  THE PROGRAM WILL NOW PRESET THE 'RDV' FLIP-FLOP
10022                              BY PULSING MEMORY SIMULATOR SIGNAL 'RST H'.  THE PROGRAM WILL CHECK THAT
10023                              THE 'RDV' FLIP-FLOP PRESET AND THAT THE SIGNAL 'MSBRK H' WENT TO THE LOW
10024                              STATE AS A RESULT OF THE 'RDV' FLIP-FLOP BEING PRESET.  THE PROGRAM WILL
10025                              NOW PULSE THE TARGET EMULATOR SIGNAL 'XRAS H' AGAIN AND CHECK THAT THE
10026                              'MEMBRK' FLIP-FLOP IS STILL SET TO A ONE AS A RESULT OF THE FLIP-FLOP
10027                              BEING LATCHED ONCE IT HAS BEEN SET.  THE PROGRAM WILL NOW PULSE TARGET
10028                              EMULATOR SIGNAL 'BRKRES L' AND CHECK THAT THE 'MEMBRK' FLIP-FLOP WAS
10029                              CLEARED.  THE PROGRAM WILL NOW SET THE TARGET EMULATOR SIGNAL 'FETCT H'
10030                              TO THE HIGH STATE AND PULSE THE SIGNAL 'XRAS H'.  A PULSE ON 'XRAS H'
10031                              WILL CAUSE THE EDFET FLIP-FLOP TO BE SET AND THE ADDRESS TO BE CLOCKED
10032                              INTO THE MEMORY SIMULATOR SYSTEM ADDRESS BUS LATCHES.  THE ADDRESS WILL
10033                              ADDRESS MEMORY ON THE MEMORY SIMULATOR MODULE WHICH IS MAPPED TO INHIBIT
10034                              READS AND WRITES, THEREFORE, THE SYSTEM BUS SIGNAL 'RDE L' WILL BE
10035                              ASSERTED HIGH.  AS A RESULT OF 'RDE L', 'EDFET H', 'PSMW L' BEING
10036                              ASSERTED HIGH AND A PULSE ON 'XRASD H', THE 'MEMBRK' FLIP-FLOP WILL BE
10037                              DIRECT SET TO A ONE.  THE SIGNAL 'MEMBRK H' ASSERTED HIGH WILL CAUSE THE
10038                              SIGNAL 'SOP H' TO BE ASSERTED HIGH.  WHEN 'SOP H' AND 'EDFET H' ARE
10039                              ASSERTED HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO
10040                              A ONE.  THE PROGRAM WILL CHECK THAT THE 'MEMBRK' AND 'PSMW' FLIP-FLOPS
10041                              ARE SET TO ONES.  THE PROGRAM WILL NOW SET THE TARGET EMULATOR'S INTER-
10042                              RUPT ENBALE BIT AND LOWER THE CPU PRIORITY LEVEL TO ALLOW INTERRUPTS.
10043                              THE BREAK INTERRUPT FLIP-FLOP WAS SET TO A ONE PREVIOUSLY AS A RESULT
10044                              OF 'MEMBRK H' BEING ASSERTED HIGH AND A PULSE BEING ISSUED ON 'XRAS L'.
10045                              THE PROGRAM WILL NOW CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE
10046                              INTERRUPT ENABLE BIT BEING SET, THE BREAK INTERRUPT FLIP-FLOP BEING SET,
10047                              AND THE CPU PRIORITY LEVEL BEING LOWERED TO ALLOW INTERRUPTS.   THE
10048                              PROGRAM WILL ISSUE A PULSE ON 'BRKRES L' AND CHECK THAT THE 'MEMBRK'
10049                        ;--   FLIP-FLOP WAS CLEARED BY THE PULSE ON 'BRKRES L'.
10050
10051
10052    026612               BGNTST
10053    026612        T9::
10054    026612  004737  007440    JSR     PC,INITMD               ;INITIALIZE MDE/T-11 SYSTEM MODULES
10055
10056    026616               BGNSEG
10057    026616  104404        TRAP    C$BSEG
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B 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 196
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEQ 0196

```
10058
10059   026620                                      SETPRI  #PRI07                  ;RAISE CPU PRIORITY TO 7
10060   026620  012700  000340                      MOV     #PRI07,R0
10061   026624  104441                              TRAP    C$SPRI
10062
10063                                               ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10064                                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10065
10066   026626  004737  011250                      JSR     PC,SLCTMS               ;SELECT MEMORY SIMULATOR MODULE
10067
10068                                               ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM.  THE
10069                                               ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H'' AND 'MPIN H'' SET TO
10070                                               ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM.  MAP PROTECTION RAM
10071                                               ;BITS 'WRE H'' AND 'RDE H'' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
10072                                               ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
10073                                               ;WHEN 'RDE H'' AND 'WRE H'' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
10074                                               ;TO THOSE ADDRESSES.
10075
10076   026632  004737  011356                      JSR     PC,MPRAM                ;GO LOAD, READ AND CHECK MAP PROTECT RAM
10077
10078                                               ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0.  THE FOLLOWING DATA
10079                                               ;PATTERNS: 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
10080                                               ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0.  THESE PATTERNS
10081                                               ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE
10082                                               ;ADDRESSED.
10083
10084   026636  004737  011642                      JSR     PC,MSRAM0               ;LOAD, READ AND CHECK MODULE SELECT RAM 0
10085
10086                                               ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1.  THE FOLLOWING DATA PATTERNS
10087                                               ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
10088                                               ;AT ADDRESS 0; 17, 0, 0 AND 0.  THESE PATTERNS WILL ENABLE THE FIRST 32K
10089                                               ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
10090
10091   026642  004737  012012                      JSR     PC,MSRAM1               ;LOAD, READ AND CHECK MODULE SELECT RAM 1
10092
10093                                               ;SET THE SIGNAL 'CTS H'' TO A ONE IN CONTROL REGISTER 0.  THIS WILL
10094                                               ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
10095                                               ;IN THIS TEST, 'CTS H'' ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
10096                                               ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
10097                                               ;SYSTEM BUS.
10098
10099   026646  052737  000002  002234              BIS     #CTSH,SOLOAD            ;SETUP BIT TO BE LOADED
10100   026654  004737  010506                      JSR     PC,LDRDS0               ;GO LOAD, READ AND CHECK CONTROL REG 2
10101   026660  001405                              BEQ     1$                      ;IF LOADED OK THEN CONTINUE
10102   026662                                      ERRDF   1,,SOEROR               ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
10103   026662  104455                              TRAP    C$ERDF
10104   026664  000001                              .WORD   1
10105   026666  000000                              .WORD   0
10106   026670  005306                              .WORD   SOEROR
10107   026672                              CKLOOP
10108   026672  104406                              TRAP    C$CLP1
10109
10110                                               ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10111                                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10112
10113   026674  004737  012214            1$:       JSR     PC,SLCTTE               ;SELECT TARGET EMULATOR MODULE
```

C 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 197
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEQ 0197

```
10114
10115                                          ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL "BRKRES L"
10116                                          ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
10117                                          ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
10118                                          ;THE SIGNAL "BRKRES L" VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
10119                                          ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
10120                                          ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED VIA THE
10121                                          ;THE SIGNAL "RASP L" LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
10122                                          ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
10123                                          ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
10124
10125   026700  012737  043020  002334         MOV     #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
10126   026706  004737  012766                 JSR     PC,BRKRES                ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
10127
10128                                          ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
10129                                          ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
10130                                          ;REGISTER 6.
10131
10132   026712  004537  012234                 JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
10133   026716  000003                         .WORD   HDAL                    ;SELECT THE HDAL REGISTER
10134
10135                                          ;SET HDAL REGISTER BITS 9,4,3 + 2 TO A ONE AND HDAL BITS 14 AND 11 TO A
10136                                          ;ZERO.  HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
10137                                          ;AND CONTROL SIGNALS.  HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
10138                                          ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS.  HDAL REGISTER
10139                                          ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
10140                                          ;HDAL REGISTER BITS 4 AND 3 SET TO ONES WILL SET THE SIGNALS XR/WLB H
10141                                          ;AND XR/WHB H TO THE HIGH STATE.  THESE SIGNALS WILL CAUSE THE SIGNAL
10142                                          ;"REAT H" TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE SIGNALS XRAS H
10143                                          ;AND XCAS H ARE ASSERTED HIGH.
10144
10145   026720  012737  001034  002346         MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;SET HDAL BITS 9,4,3 + 2 TO ONES
10146   026726  004737  011216                 JSR     PC,LDRDT6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10147   026732  001405                         BEQ     2$                      ;IF LOADED OK THEN CONTINUE
10148   026734                                 ERRDF   12,HDALRG,TO6ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
10149   026734  104455                         TRAP    C$ERDF
10150   026736  000014                         .WORD   12
10151   026740  003756                         .WORD   HDALRG
10152   026742  006732                         .WORD   TO6ERR
10153   026744                                 CKLOOP
10154   026744  104406                         TRAP    C$CLP1
10155
10156                                          ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
10157                                          ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
10158                                          ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY "BRKRES L".
10159
10160   026746  005037  002340         2$:     CLR     T4LOAD                  ;SETUP TO CLEAR ALL OTHER R/W BITS
10161   026752  004737  012706                 JSR     PC,CLRPSM               ;PULSE INVD L VIA VDAL2 H
10162
10163                                          ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON
10164                                          ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
10165                                          ;BE WRITTEN OR READ.
10166
10167   026756  004537  012234                 JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
10168   026762  000004                         .WORD   MODE                    ;SELECT THE MODE REGISTER
10169
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D 16

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10170                                          ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
10171                                          ;ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
10172
10173  026764  005037  002346        CLR     T6LOAD              ;SETUP TO CLEAR ALL MODE REGISTER BITS
10174  026770  004737  011216        JSR     PC,LDRDT6           ;GO LOAD, READ AND CHECK MODE REGISTER
10175  026774  001405                BEQ     3$                  ;IF LOADED OK THEN CONTINUE
10176  026776                        ERRDF   12,MODREG,TO6ERR    ;MODE REGISTER NOT EQUAL EXPECTED
10177  026776  104455                TRAP    C$ERDF
10178  027000  000014                .WORD   12
10179  027002  004002                .WORD   MODREG
10180  027004  006732                .WORD   TO6ERR
10181  027006                        CKLOOP
10182  027006  104406                TRAP    C$CLP1
10183
10184                                          ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
10185                                          ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
10186                                          ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
10187                                          ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
10188                                          ;TER WILL BE ADDRESSED.
10189
10190  027010  004537  012234    3$: JSR     R5,SELTER           ;SELECT REGISTER SPECIFIED BY NEXT WORD
10191  027014  000002                .WORD   FDAL                ;SELECT EOAI AND FDAL REGISTER
10192
10193                                          ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER.  THE EOAI REGISTER WILL
10194                                          ;BE LOADED AND CHECKED FOR ZEROES.  THE FDAL REGISTER WILL BE LOADED AND
10195                                          ;CHECKED FOR A DATA PATTERN OF ONE (FDALO H = 1).
10196
10197  027016  012737  000001  002346  MOV   #FDALO,T6LOAD       ;SETUP EOAI AND FDAL REG DATA PATTERN
10198  027024  004737  011216        JSR     PC,LDRDT6           ;GO LOAD, READ AND CHECK EOAI + FDAL REG
10199  027030  001405                BEQ     4$                  ;IF LOADED OK THEN CONTINUE
10200  027032                        ERRDF   12,EOAIFD,TO6ERR    ;EOAI OR FDAL REGISTER ERROR
10201  027032  104455                TRAP    C$ERDF
10202  027034  000014                .WORD   12
10203  027036  004047                .WORD   EOAIFD
10204  027040  006732                .WORD   TO6ERR
10205  027042                        CKLOOP
10206  027042  104406                TRAP    C$CLP1
10207
10208                                          ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
10209                                          ;2:0 TO A 0.  THE DIAGNSOTIC ADDRESS REGISTER WILL BE WRITTEN WITH A DATA
10210                                          ;PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.  THE DIAGNOSTIC ADDRESS
10211                                          ;REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER BIT 10
10212                                          ;BEING SET TO A ONE PREVIOUSLY.  ON A READ COMMAND TO CONTROL REGISTER
10213                                          ;6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
10214
10215  027044  004537  012234    4$: JSR     R5,SELTER           ;SELECT REGISTER SPECIFIED BY NEXT WORD
10216  027050  000000                .WORD   ADDRES              ;SELECT DIAG ADDRESS REG AND ADDRESS BUS
10217
10218                                          ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA PATTERN
10219                                          ;OF 100000.  THIS WILL CAUSE MEMORY NOT MAPPED TO BE SELECTED LATER ON IN
10220                                          ;THIS TEST.  ADDRESS BITS 17 AND 16 WERE SET TO A ZERO EARLIER IN THIS
10221                                          ;TEST VIA THE HDAL REGISTER.
10222
10223  027052  012737  100000  002346  MOV   #ADDR15,T6LOAD      ;SETUP DATA PATTERN OF 100000
10224  027060  004737  011216        JSR     PC,LDRDT6           ;LOAD, READ ADN CHECK DIAG ADDRESS REG
10225  027064  001405                BEQ     5$                  ;IF LOADED OK THEN CONTINUE
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E 16

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10226   027066                              ERRDF   12,ADDRRG,T06ERR      ;DIAGNOSTIC ADDRESS REGISTER ERROR
10227   027066   104455                     TRAP    C$ERDF
10228   027070   000014                     .WORD   12
10229   027072   004144                     .WORD   ADDRRG
10230   027074   006732                     .WORD   T06ERR
10231   027076                              CKLOOP
10232   027076   104406                     TRAP    C$CLP1
10233
10234                                        ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
10235                                        ;CHANGES OCCURED DURING THE PAST SEQUENCES.
10236
10237   027100   004737   011200    5$:     JSR     PC,READT4             ;READ AND CHECK VDAL REGISTER
10238   027104   001405                     BEQ     6$                    ;IF NO CHANGES THEN CONTINUE
10239   027106                              ERRDF   11,VDALRG,T4EROR      ;VDAL OR PAUSE STATE MACHINE ERROR
10240   027106   104455                     TRAP    C$ERDF
10241   027110   000013                     .WORD   11
10242   027112   003710                     .WORD   VDALRG
10243   027114   006716                     .WORD   T4EROR
10244   027116                              CKLOOP
10245   027116   104406                     TRAP    C$CLP1
10246
10247                                        ;RE-SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE
10248                                        ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
10249                                        ;CONTROL REGISTER 6.
10250
10251   027120   004537   012234    6$:     JSR     R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
10252   027124   000003                     .WORD   HDAL                  ;SELECT THE HDAL REGISTER
10253
10254   027126   012737   001034  002346    MOV     #HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;BITS THAT WERE PREVIOUSLY LOADED
10255
10256                                        ;PERFORM A T-11 TIMING CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE:
10257                                        ;  1. SET XRAS H AND PRAS H TO THE HIGH STATE
10258                                        ;  2. SET XCAS H AND PCAS H TO THE HIGH STATE
10259                                        ;  3. SET XPI L AND PPI L TO THE LOW STATE
10260                                        ;  4. SET XCAS H AND PCAS H TO THE LOW STATE
10261                                        ;  5. SET XPI L AND PPI L TO THE HIGH STATE
10262                                        ;  6. SET XRAS H AND PRAS H TO THE LOW STATE
10263                                        ;WHEN PRAS H IS SET HIGH, THE SYSTEM ADDRESS BUS, WHICH CONTAINS THE
10264                                        ;TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER DATA, WILL BE CLOCKED INTO
10265                                        ;THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.
10266                                        ;WHEN XRAS H AND XCAS H ARE ASSERTED HIGH, THE TARGET EMULATOR SIGNALS
10267                                        ;REAT H AND READ H WILL BE ASSERTED HIGH.  THE SIGNAL READ H WILL ATEMPT
10268                                        ;TO READ DATA FROM THE MEMORY SIMULATOR RAM.  HOWEVER, IN THIS TEST, THE
10269                                        ;MAP PROTECT RAM IS SETUP TO INHIBIT READS AND WRITES TO THE ADDRESS
10270                                        ;SELECTED (10000).  THEREFORE, A READ VIOLATION SHOULD OCCUR THUS CAUSING
10271                                        ;THE SIGNAL MSBRK H TO BE ASSERTED HIGH.  THE READ VIOLATION FLIP-FLOP
10272                                        ;WILL BE CLOCKED VIA THE SIGNAL RDS H.  THE SIGNAL RDS H WILL BE ASSERTED
10273                                        ;HIGH WHEN CTS H IS ASSERTED HIGH AND THE SIGNAL READ H GOES FROM A LOW
10274                                        ;TO A HIGH STATE.  THE SIGNAL MSBRK H WILL NOT BE CLOCKED INTO THE TARGET
10275                                        ;EMULATORS MEMBRK FLIP-FLOP UNTIL THE SIGNAL XRAS H IS PULSED AGAIN.
10276
10277   027134   004737   012300             JSR     PC,XRASH              ;SET XRAS H AND PRAS H TO HIGH STATE
10278   027140   004737   012404             JSR     PC,XCASH              ;SET XCAS H AND PCAS H TO HIGH STATE
10279   027144   004737   012510             JSR     PC,XPIH               ;SET XPI L AND PPI L TO LOW STATE
10280   027150   004737   012436             JSR     PC,XCASL              ;SET XCAS H AND PCAS H TO LOW STATE
10281   027154   004737   012542             JSR     PC,XPIL               ;SET XPI L AND PPI L TO HIGH STATE
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F 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 200
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEQ 0200

```
10282   027160  004737  012332                  JSR     PC,XRASL                ;SET XRAS H AND PRAS H TO LOW STATE
10283
10284                                           ;READ TARGET EMULATORS GDAL REGISTER TO CHECK THAT NO CHANGES HAVE
10285                                           ;OCCURED AS A RESULT OF THE ABOVE TIMING SEQUENCE.  THE SIGNAL MEMBRK H
10286                                           ;SHOULD BE ASSERTED LOW UNTIL A PULSE IS ISSUED ON THE SIGNAL XRAS H
10287                                           ;AGAIN.
10288
10289   027164  004737  011114                  JSR     PC,READTO               ;READ AND CHECK GDAL REGISTER
10290   027170  001405                          BEQ     7$                      ;IF DATA OK THEN CONTINUE
10291   027172                                  ERRDF   9,GDALRG,TOEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
10292   027172  104455                          TRAP    C$ERDF
10293   027174  000011                          .WORD   9
10294   027176  003640                          .WORD   GDALRG
10295   027200  006666                          .WORD   TOEROR
10296   027202                                  CKLOOP
10297   027202  104406                          TRAP    C$CLP1
10298
10299                                           ;READ VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS ASSERTED HIGH
10300                                           ;AS A RESULT OF THE SIGNALS CYCLE L, ENEDC H, PSM L, AND SOP L BEING
10301                                           ;ASSERTED TO THE HIGH STATE.
10302
10303   027204  052737  000020  002342  7$:     BIS     #VDAL4,T4GOOD           ;EXPECT EDEOC H TO BE A ONE
10304   027212  004737  011200                  JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
10305   027216  001405                          BEQ     8$                      ;IF OK THEN CONTINUE
10306   027220                                  ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
10307   027220  104455                          TRAP    C$ERDF
10308   027222  000013                          .WORD   11
10309   027224  003710                          .WORD   VDALRG
10310   027226  006716                          .WORD   T4EROR
10311   027230                                  CKLOOP
10312   027230  104406                          TRAP    C$CLP1
10313
10314                                           ;SELECT MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10315                                           ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10316
10317   027232  004737  011250          8$:     JSR     PC,SLCTMS               ;SELECT THE MEMORY SIMULATOR MODULE
10318
10319                                           ;READ CONTROL REGISTER 4 BITS MSAD 15:0 TO CHECK THAT THE TARGET EMULATORS
10320                                           ;DIAGNOSTIC ADDRESS REGISTER, WHICH WAS ENABLED TO THE SYSTEM ADDRESS
10321                                           ;BUS, WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES.
10322                                           ;THE ADDRESS READ SHOULD BE EQUAL TO 10000.
10323
10324   027236  012737  100000  002254          MOV     #MSAD15,S4LOAD          ;SETUP EXPECTED ADDRESS FOR COMPARE
10325   027244  004737  010614                  JSR     PC,READS4               ;READ AND CHECK MSAD BITS 15:0
10326   027250  001405                          BEQ     9$                      ;IF ADDRESS OK THEN CONTINUE
10327   027252                                  ERRDF   3,TEMSAD,SO4ERR         ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
10328   027252  104455                          TRAP    C$ERDF
10329   027254  000003                          .WORD   3
10330   027256  002534                          .WORD   TEMSAD
10331   027260  005406                          .WORD   SO4ERR
10332   027262                                  CKLOOP
10333   027262  104406                          TRAP    C$CLP1
10334
10335                                           ;READ AND CHECK CONTROL REGISTER 2 BITS.  MSAD16 H AND MSAD17 H SHOULD
10336                                           ;BE READ AS ZEROES AS A RESULT OF DATA LOADED INTO THE TARGET EMULATOR
10337                                           ;MODULE.  THE SIGNALS MSEL0 H AND MSEL1 H WILL BE IGNORED BECAUSE THESE
```

G 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 201
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEQ 0201

```
10338                                        ;SIGNALS ARE TRI-STATED AS A REUSLT OF THE SIGNAL CTS H BEING ASSERTED
10339                                        ;HIGH.  THE SIGNALS ESR H AND MSBRK H SHOULD BE READ AS ONES. THE SIGNAL
10340                                        ;MSBRK H SHOULD BE A ONE AS A RESULT OF TRYING TO READ ADDRESS 10000 WHICH
10341                                        ;WAS MAPPED TO INHIBIT READS AND WRITES.  THE RDV FLIP-FLOP SHOULD BE
10342                                        ;CLEARED THUS CAUSING THE SIGNAL BRK L TO BE ASSERTED LOW WHICH WILL
10343                                        ;CAUSE THE SIGNAL MSBRK H TO BE ASSERTED HIGH.
10344
10345   027264  012737  177414  002250  9$:  MOV     #177414,S2MASK          ;SETUP TO IGNORE UNWANTED BITS
10346   027272  005037  002244               CLR     S2LOAD                  ;SETUP VALUES FOR R/W BITS
10347   027276  012737  000240  002246       MOV     #ESRH!MSBRKH,S2GOOD     ;EXPECT ESR H AND MSBRK H TO BE ONES
10348   027304  004737  010562               JSR     PC,READS2               ;READ AND CHECK CONTROL REGISTER 2
10349   027310  001405                        BEQ     10$                     ;IF DATA OK THEN CONTINUE
10350   027312                                ERRDF   2,,S2EROR               ;CONTROL REGISTER 2 NOT EQUAL EPXETCED
10351   027312  104455                        TRAP    C$ERDF
10352   027314  000002                        .WORD   2
10353   027316  000000                        .WORD   0
10354   027320  005322                        .WORD   S2EROR
10355   027322                                CKLOOP
10356   027322  104406                        TRAP    C$CLP1
10357
10358                                        ;READ CONTROL REGISTER 0 TO CHECK THAT THE RDV F/F IS SET TO A ONE
10359
10360   027324  052737  000020  002236  10$: BIS     #RDVH,S0GOOD            ;EXPECT RDV FLIP-FLOP TO BE A ONE
10361   027332  004737  010522               JSR     PC,READS0               ;READ AND CHECK CONTROL REGISTER 0
10362   027336  001405                        BEQ     11$                     ;IF OK THEN CONTINUE
10363   027340                                ERRDF   1,,S0EROR               ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
10364   027340  104455                        TRAP    C$ERDF
10365   027342  000001                        .WORD   1
10366   027344  000000                        .WORD   0
10367   027346  005306                        .WORD   S0EROR
10368   027350                                CKLOOP
10369   027350  104406                        TRAP    C$CLP1
10370
10371                                        ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10372                                        ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10373
10374   027352  004737  012214          11$: JSR     PC,SLCTTE               ;SELECT THE TARGET EMULATOR MODULE
10375
10376                                        ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL REGISTER BIT 12.
10377                                        ;WHEN XRAS H IS PULSED, THE SIGNAL MSBRK H FROM THE MEMORY SIMULATOR
10378                                        ;MODULE, WHICH IS HIGH, SHOULD BE CLOCKED INTO THE MEMBRK FLIP-FLOP THUS
10379                                        ;SETTING THE SIGNAL MEMBRK H TO THE HIGH STATE
10380
10381   027356  004737  012266               JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
10382
10383                                        ;READ GDAL REGISTER TO CHECK THAT THE SIGNAL MEMBRK H IS ASSERTED HIGH
10384                                        ;AS A RESULT OF MSBRK H BEING HIGH AND A PULSE ON THE SIGBAL XRAS H.
10385                                        ;THE MEMBRK FLIP-FLOP SHOULD NOW BE SET TO A ONE.
10386
10387   027362  052737  000040  002326       BIS     #MEMBRK,TOGOOD          ;EXPECT MEMBRK H TO BE A ONE
10388   027370  004737  011114               JSR     PC,READTO               ;READ AND CHECK GDAL REGISTER
10389   027374  001405                        BEQ     12$                     ;IF OK THEN CONTINUE
10390   027376                                ERRDF   9,GDALRG,TOEROR         ;MEMBRK FLIP-FLOP PROBABLY NOT SET
10391   027376  104455                        TRAP    C$ERDF
10392   027400  000011                        .WORD   9
10393   027402  003640                        .WORD   GDALRG
```

H 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 202
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEQ 0202

```
10394   027404  006666                              .WORD   TOEROR
10395   027406                              CKLOOP
10396   027406  104406                              TRAP    C$CLP1
10397
10398                                       ;READ VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS ASSERTED LOW
10399                                       ;WHEN MEMBRK H IS ASSERTED HIGH AND SOP L IS ASSERTED LOW.
10400
10401   027410  042737  000020  002342  12$:  BIC     #VDAL4,T4GOOD          ;EXPECT EDEOC H TO BE A 0
10402   027416  004737  011200              JSR     PC,READT4             ;READ AND CHECK VDAL REGISTER
10403   027422  001405                      BEQ     13$                   ;IF OK THEN CONTINUE
10404   027424                              ERRDF   11,VDALRG,T4EROR      ;VDAL REGISTER NOT EQUAL EXPECTED
10405   027424  104455                      TRAP    C$ERDF
10406   027426  000013                      .WORD   11
10407   027430  003710                      .WORD   VDALRG
10408   027432  006716                      .WORD   T4EROR
10409   027434                              CKLOOP
10410   027434  104406                      TRAP    C$CLP1
10411
10412                                       ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10413                                       ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10414
10415   027436  004737  011250          13$:  JSR     PC,SLCTMS             ;SELECT THE MEMORY SIMULATOR MODULE
10416
10417                                       ;TO CHECK THAT THE MEMBRK FLIP-FLOP ON THE TARGET EMULATOR MODULE ONCE
10418                                       ;SET WILL REMAIN SET UNTIL CLEARED BY BRKRES L. THE PROGRAM WILL PRESET
10419                                       ;THE RDV AND WRV FLIP-FLOPS BY PULSING THE SIGNAL RST H THUS SETTING THE
10420                                       ;SIGNAL MSBRK H TO THE LOW STATE.
10421
10422   027442  004737  011270              JSR     PC,MSRSTH             ;GO PULSE RST H TO PRESET WRV + RDV F/F'S
10423
10424                                       ;READ CONTROL REGISTER 2 TO CHECK THAT THE SIGNAL MSBRK H WENT TO A
10425                                       ;ZERO AS A RESULT OF PULSING RST H.
10426
10427   027446  042737  000200  002246      BIC     #MSBRKH,S2GOOD        ;EXPECT MSBRK H TO BE A ZERO
10428   027454  004737  010562              JSR     PC,READS2             ;READ AND CHECK CONTROL REGISTER 2
10429   027460  001405                      BEQ     14$                   ;IF OK THEN CONTINUE
10430   027462                              ERRDF   2,,S2EROR             ;MSBRK H PROBABLY NOT 0 AFTER RST H
10431   027462  104455                      TRAP    C$ERDF
10432   027464  000002                      .WORD   2
10433   027466  000000                      .WORD   0
10434   027470  005322                      .WORD   S2EROR
10435   027472                              CKLOOP
10436   027472  104406                      TRAP    C$CLP1
10437
10438                                       ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10439                                       ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10440
10441   027474  004737  012214          14$:  JSR     PC,SLCTTE             ;SELECT TARGET EMULATOR MODULE
10442
10443                                       ;WITH MSBRK H ASSERTED LOW AND MEMBRK H ASSERTED HIGH, PULSE XRAS H
10444                                       ;TO CHECK THAT THE MEMBRK FLIP-FLOP WILL REMAIN LATCHED TO THE ONE
10445                                       ;STATE.
10446
10447   027500  004737  012266              JSR     PC,XRAS               ;PULSE XRAS H VIA HDAL12 H
10448
10449                                       ;READ CONTROL REGISTER 0 TO CHECK THAT THE SIGNAL MEMBRK H IS STILL
```

I 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 203
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEQ 0203

```
10450                                              ;ASSERTED HIGH EVEN THOUGH MSBRK H IS LOW AND A PULSE WAS ISSUED ON THE
10451                                              ;SIGNAL XRAS H.  THE MEMBRK FLIP-FLOP SHOULD REMAIN LATHCED TO A ONE
10452                                              ;UNTIL CLEARED BY A PULSE ON THE SIGNAL BRKRES L.
10453
10454   027504  004737  011114           JSR      PC,READTO           ;READ AND CHECK GDAL REGISTER
10455   027510  001405                    BEQ      15$                 ;IF NO CHANGE THEN CONTINUE
10456   027512                            ERRDF    9,GDALRG,TOEROR     ;GDAL REGISTER NOT EQUAL EXPECTED
10457   027512  104455                    TRAP     C$ERDF
10458   027514  000011                    .WORD    9
10459   027516  003640                    .WORD    GDALRG
10460   027520  006666                    .WORD    TOEROR
10461   027522                            CKLOOP
10462   027522  104406                    TRAP     C$CLP1
10463
10464                                              ;GO PULSE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT
10465                                              ;ZERO.  A PULSE ON THE SIGNAL BRKRES L WILL CAUSE THE MEMBRK FLIP-FLOP
10466                                              ;TO BE CLEARED.
10467
10468   027524  004737  012766    15$:    JSR      PC,BRKRES           ;GO PULSE BRKRES L VIA ADALO H
10469
10470                                              ;READ GDAL REGISTER TO CHECK THAT BRKRES L CLEARED MEMBRK FLIP-FLOP
10471
10472   027530  042737  000040  002326    BIC      #MEMBRK,TOGOOD      ;EXPECT MEMBRK H TO BE A ZERO
10473   027536  004737  011114            JSR      PC,READTO           ;READ AND CHECK GDAL REGISTER
10474   027542  001405                    BEQ      16$                 ;IF OK THEN CONTINUE
10475   027544                            ERRDF    9,GDALRG,TOEROR     ;MEMBRK F/F PROBABLY NOT 0 AFTER RST H
10476   027544  104455                    TRAP     C$ERDF
10477   027546  000011                    .WORD    9
10478   027550  003640                    .WORD    GDALRG
10479   027552  006666                    .WORD    TOEROR
10480   027554                            CKLOOP
10481   027554  104406                    TRAP     C$CLP1
10482
10483                                              ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL REGISTER BIT 7
10484                                              ;TO A ONE AND CHECK THAT THE SIGNAL EDEOC H IS NOW SET TO A ONE AS A
10485                                              ;RESULT OF THE SIGNAL SOP L RETURNING TO THE HIGH STATE AFTER THE SIGNAL
10486                                              ;MEMBRK H WENT TO THE LOW STATE.
10487
10488   027556  012737  000200  002340    16$:    MOV      #VDAL7,T4LOAD       ;SETUP BIT TO BE LOADED
10489   027564  013737  002340  002342    MOV      T4LOAD,T4GOOD       ;COPY DATA LOADED TO EXPECTED
10490   027572  052737  000020  002342    BIS      #VDAL4,T4GOOD       ;EXPECT EDEOC H TO BE A ONE
10491   027600  004737  011172            JSR      PC,LDRD4T           ;LOAD, READ AND CHECK VDAL REGISTER
10492   027604  001405                    BEQ      17$                 ;IF VDAL REGISTER OK THEN CONTINUE
10493   027606                            ERRDF    11,VDALRG,T4EROR    ;VDAL REGISTER NOT EQUAL EXPECTED
10494   027606  104455                    TRAP     C$ERDF
10495   027610  000013                    .WORD    11
10496   027612  003710                    .WORD    VDALRG
10497   027614  006716                    .WORD    T4EROR
10498   027616                            CKLOOP
10499   027616  104406                    TRAP     C$CLP1
10500
10501                                              ;TOGGLE THE SIGNALS XRAS AND PRAS BY SETTING AND CLEARING HDAL12 H.
10502                                              ;SETTING THE SIGNAL XRAS H TO THE HIGH STATE WILL CLOCK THE EDFET, BTFET
10503                                              ;AND PAUSE MODE FLIP-FLOPS TO A ONE THUS SETTING THE SIGNAL EDFET H TO
10504                                              ;THE HIGH STATE, AND THE SIGNALS BTFET L AND PAUSE L TO THE LOW STATES.
10505                                              ;SETTING PRAS H TO THE HIGH STATE WILL SET THE SIGNAL ADVAL H TO THE
```

J 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 204
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEQ 0204

```
10506                                              ;HIGH STATE WHICH WILL CAUSE THE SYSTEM ADDRESS BUS TO BE CLOCKED INTO
10507                                              ;THE MEMORY SIMULATOR'S SYSTEM ADDRESS BUS LATCHES.  THE ADDRESS CLOCKED
10508                                              ;WILL BE 100000 WHICH IS MAPPED ON THE MEMORY SIMULATOR MODULE TO INHIBIT
10509                                              ;READS AND WRITES, THEREFORE, THE MEMORY SIMULATOR SIGNAL RDE L SHOULD
10510                                              ;BE ASSERTED HIGH.  AS A RESULT OF RDE L BEING ASSERTED HIGH, THE EDFET
10511                                              ;FLIP-FLOP BEING SET TO A ONE, THE PAUSE STATE WORKING FLIP-FLOP BEING
10512                                              ;A ZERO AND A PULSE BEING ISSUED ON THE SIGNAL XRASD H, THE MEMBRK FLIP-
10513                                              ;FLOP WILL BE DIRECT SET TO A ONE THUS CAUSING THE SIGNALS MEMBRK H
10514                                              ;AND PSMW H TO BE ASSERTED HIGH.  WHEN XRAS L IS RETURNED TO THE HIGH
10515                                              ;STATE AFTER HAVING BEEN SET LOW, THE STATE OF MEMBRK H WILL BE CLOCKED
10516                                              ;INTO THE INTERRUPT BREAK FLIP-FLOP THUS CAUSING THAT FLIP-FLOP TO BE
10517                                              ;SET TO A ONE.
10518
10519   027620  004737  012266         17$:   JSR     PC,XRAS                ;GO PULSE XRAS H AND PRAS H VIA HDAL12
10520
10521                                              ;READ GDAL REGISTER TO CHECK THAT MEMBRK FLIP-FLOP WAS DIRECT SET TO
10522                                              ;A ONE BY A PULSE ON XRASD H AND THE FOLLOWING SIGNALS BEING ASSERTED
10523                                              ;HIGH: RDE L, EDFET H, AND PSMW L.
10524
10525   027624  052737  000040  002326        BIS     #MEMBRK,TOGOOD         ;EXPECT MEMBRK F/F TO BE SET
10526   027632  004737  011114                JSR     PC,READTO             ;READ AND CHECK VDAL REGISTER
10527   027636  001405                        BEQ     18$                    ;IF OK THEN CONTINUE
10528   027640                                ERRDF   9,GDALRG,TOEROR        ;MEMBRK F/F PROBABLY NOT DIRECT SET TO 1
10529   027640  104455                        TRAP    C$ERDF
10530   027642  000011                        .WORD   9
10531   027644  003640                        .WORD   GDALRG
10532   027646  006666                        .WORD   TOEROR
10533   027650                                CKLOOP
10534   027650  104406                        TRAP    C$CLP1
10535
10536                                              ;READ THE VDAL REGISTER AND CHECK THAT THE PAUSE STATE WORKING FLIP-
10537                                              ;FLOP WAS SET TO A ONE VIA EDFET H AND SOP H.  THE SIGNAL SOP H IS SET
10538                                              ;HIGH VIA MEMBRK H.  CHECK EDEOC H TO BE A ZERO AS A RESULT OF SOP L
10539                                              ;BEING ASSERTED LOW.  BTS1 H WILL BE A ONE AS A RESULT OF THE BTFET
10540                                              ;FLIP-FLOP BEING SET TO A ONE WHEN XRAS H WAS PULSED.
10541
10542   027652  042737  000020  002342  18$:   BIC     #VDAL4,T4GOOD         ;EXPECT EDEOC H TO BE A ZERO
10543   027660  052737  001040  002342        BIS     #VDAL9!VDAL5,T4GOOD   ;EXPECT PSMW H AND BTS1 H TO BE HIGH
10544   027666  004737  011200                JSR     PC,READT4             ;READ AND CHECK VDAL REGISTER
10545   027672  001405                        BEQ     19$                    ;IF OK THEN CONTINUE
10546   027674                                ERRDF   11,VDALRG,T4EROR       ;VDAL REGISTER NOT EQUAL EXPECTED
10547   027674  104455                        TRAP    C$ERDF
10548   027676  000013                        .WORD   11
10549   027700  003710                        .WORD   VDALRG
10550   027702  006716                        .WORD   T4EROR
10551   027704                                CKLOOP
10552   027704  104406                        TRAP    C$CLP1
10553
10554                                              ;SETUP TARGET EMULATOR INTERRUPT VECTOR TO THE VECTOR SPECIFIED BY
10555                                              ;THE USER AT PROGRAM START TIME.  THE CPU PRIORITY LEVEL WILL BE RESET
10556                                              ;TO PRIORITY LEVEL 7 WHEN AN INTERRUPT OCCURS.
10557
10558   027706                          19$:   SETVEC  TEVECT,#INTSRV,#PRI07  ;SETUP INTERRUPT VECTOR
10559   027706  012746  000340                MOV     #PRIO7,-(SP)
10560   027712  012746  013046                MOV     #INTSRV,-(SP)
10561   027716  013746  002214                MOV     TEVECT,-(SP)
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K 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 205
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEQ 0205

```
10562  027722  012746  000003              MOV     #3,-(SP)
10563  027726  104437                      TRAP    C$SVEC
10564  027730  062706  000010              ADD     #10,SP
10565  027734  005002                      CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
10566
10567                                       ;SET TARGET EMULATORS INTERRUPT ENABLE BIT TO A ONE BY SETTING GDAL
10568                                       ;REGISTER BIT 3 TO A ONE.
10569
10570  027736  052737  000010  002324      BIS     #GDAL3,TOLOAD           ;SETUP BIT TO BE LOADED TO SET INT ENA
10571  027744  052737  000010  002326      BIS     #GDAL3,TOGOOD           ;SETUP BIT TO BE EXPECTED ON READ
10572  027752  004737  011106              JSR     PC,LDRDOT               ;LOAD, READ AND CHECK GDAL REGISTER
10573  027756  001405                      BEQ     20$                     ;IF LOADED OK THEN CONTINUE
10574  027760                              ERRDF   9,GDALRG,TOEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
10575  027760  104455                      TRAP    C$ERDF
10576  027762  000011                      .WORD   9
10577  027764  003640                      .WORD   GDALRG
10578  027766  006666                      .WORD   TOEROR
10579  027770                              CKLOOP
10580  027770  104406                      TRAP    C$CLP1
10581
10582                                       ;LOWER THE CPU PRIORITY LEVEL TO ZERO.  AN INTERRUPT SHOULD OCCUR AS
10583                                       ;A RESULT OF THE BREAK INTERRUPT FLIP-FLOP BEING SET AND THE TARGET
10584                                       ;EMULATORS INTERRUPT ENABLE BIT BEING SET TO A ONE.
10585
10586  027772                      20$:    SETPRI  #PRI00                  ;LOWER THE CPU PRIORITY LEVEL
10587  027772  012700  000000              MOV     #PRI00,R0
10588  027776  104441                      TRAP    C$SPRI
10589
10590                                       ;CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE CPU PRIORITY LEVEL
10591                                       ;BEING SET TO ZERO, THE BREAK INTERRUPT FLIP-FLOP BEING SET TO A ONE,
10592                                       ;AND THE TARGET EMULATOR'S INTERRUPT ENBALE BIT BEING SET TO A ONE.
10593                                       ;THE BREAK INTERRUPT FLIP-FLOP WAS SET TO A ONE AS A RESULT OF MEMBRK H
10594                                       ;BEING ASSERTED HIGH AND A PULSE ON THE SIGNAL XRAS L.
10595
10596  030000  000240                      NOP                             ;DO A DUMMY INSTRUCTION TO ALLOW INTERRUPT
10597  030002  005702                      TST     R2                      ;CHECK IF AN INTERRUPT OCCURED
10598  030004  001005                      BNE     21$                     ;IF YES THEN CONTINUE
10599  030006                              ERRDF   9,NOINT,TOEROR          ;FAILED TO INTERRUPT WITH MEMBRK H SET
10600  030006  104455                      TRAP    C$ERDF
10601  030010  000011                      .WORD   9
10602  030012  004511                      .WORD   NOINT
10603  030014  006666                      .WORD   TOEROR
10604  030016                              CKLOOP
10605  030016  104406                      TRAP    C$CLP1
10606
10607                                       ;AT THIS POINT IN TIME THE CPU PRIORITY LEVEL IS AT 7 AS A RESULT OF
10608                                       ;AN INTERRUPT.  CHECK THE PREVIOUS GDAL REGISTER AGAINST THE GDAL
10609                                       ;REGISTER READ IN THE INTERRUPT SERVICE ROUTINE.
10610
10611  030020  023737  002326  002332  21$: CMP    TOGOOD,TOREAD           ;CHECK PREVIOUS AGAINST READ FROM INTERRUPT
10612  030026  001405                      BEQ     22$                     ;IF THE SAME THEN CONTINUE
10613  030030                              ERRDF   9,GDALRG,TOEROR         ;GDAL REG CHANGED AFTER AN INTERRUPT
10614  030030  104455                      TRAP    C$ERDF
10615  030032  000011                      .WORD   9
10616  030034  003640                      .WORD   GDALRG
10617  030036  006666                      .WORD   TOEROR
```

L 16

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 206
CVCDDB.P11   14-JUN-82 09:54   TEST 9: CHECK READ TO MS TO SET MSBRK H, MEMBRK H + CAUSE AN INTERRUPT   SEG 0206

```
10618  030040                               CKLOOP
10619  030040  104406                       TRAP    C$CLP1
10620
10621                                        ;ISSUE A PULSE ON THE SIGNAL BRKRES L TO CLEAR THE MEMBRK FLIP-FLOP AND
10622                                        ;THE BREAK INTERRUPT FLIP-FLOP.
10623
10624  030042  004737  012766       22$:    JSR     PC,BRKRES               ;GO PULSE BRKRES L VIA ADALO H
10625
10626                                        ;READ THE GDAL REGISTER TO CHECK THAT THE MEMBRK FLIP-FLOP WAS CLEARED
10627                                        ;BY A PULSE ON THE SIGNAL BRKRES L.
10628
10629  030046  042737  000040  002326        BIC     #MEMBRK,TOGOOD          ;EXPECT MEMBRK H TO BE  A ZERO
10630  030054  004737  011114               JSR     PC,READTO               ;READ AND CHECK GDAL REGISTER
10631  030060  001405                       BEQ     23$                     ;IF OK THEN CONTINUE
10632  030062                               ERRDF   9,GDALRG,TOEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
10633  030062  104455                       TRAP    C$ERDF
10634  030064  000011                       .WORD   9
10635  030066  003640                       .WORD   GDALRG
10636  030070  006666                       .WORD   TOEROR
10637  030072                               CKLOOP
10638  030072  104406                       TRAP    C$CLP1
10639
10640                                        ;ISSUE A PULSE ON THE SIGNAL INVD L TO INITIALIZE ALL OTHER FLIP-FLOPS
10641                                        ;NO CLEARED BY THE SIGNAL BRKRES L.
10642
10643  030074  005037  002340       23$:    CLR     T4LOAD                  ;SETUP TO CLEAR ALL VDAL R/W BITS
10644  030100  004737  012706               JSR     PC,CLRPSM               ;PULSE INVD L VIA VDAL2 H
10645
10646  030104                               CLRVEC  TEVECT                  ;RELEASE TARGET EMULATOR VECTOR
10647  030104  013700  002214               MOV     TEVECT,R0
10648  030110  104436                       TRAP    C$CVEC
10649
10650  030112                               ENDSEG
10651  030112                       10000$:
10652  030112  104405                       TRAP    C$ESEG
10653
10654  030114                               ENDTST
10655  030114                       L10045:
10656  030114  104401                       TRAP    C$ETST
10657
```

B 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 207
CVCDDB.P11   14-JUN-82 09:54   TEST 10: CHECK WRITE TO MS TO SET MSBRK H AND TE MEMBRK H   SEQ 0207

```
10658                                      .SBTTL  TEST 10: CHECK WRITE TO MS TO SET MSBRK H AND TE MEMBRK H
10659
10660                                  ;++
10661                                  ;       THIS TEST WILL CHECK THAT THE MEMORY SIMULATOR 'WRV' FLIP-FLOP CAN BE
10662                                  ;       CLEARED WHEN A 'WRITE' OPERATION IS EXECUTED FROM THE TARGET EMULATOR
10663                                  ;       MODULE TO AN ADDRESS WHICH IS MAPPED IN THE MEMORY SIMULATOR MAP PROTEC-
10664                                  ;       TION RAM TO INHIBIT READS AND WRITES.  THE 'WRV' FLIP-FLOP WILL BE
10665                                  ;       CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL 'WRE H' BEING ASSERTED LOW
10666                                  ;       AND PULSES ON THE SIGNALS 'WRHB H' AND 'WRLB H'.  THE SIGNALS 'WRHB H'
10667                                  ;       AND 'WRLB H' ARE PULSED BY THE TARGET EMULATOR MODULE AT 'PI' TIME WHEN
10668                                  ;       THE TARGET EMULATOR MODULE IS EXECUTING A T-11 WRITE OPERATION.  THE
10669                                  ;       PROGRAM WILL CHECK THAT THE MEMORY SIMULATOR SIGNAL 'MSBRK H' IS
10670                                  ;       ASSERTED HIGH AS A RESULT OF THE 'WRV' FLIP-FLOP BEING CLEARED.  THE
10671                                  ;       PROGRAM WILL CHECK THE TARGET EMULATOR MODULES 'MEMBRK' FLIP-FLOP TO
10672                                  ;       BE CLEARED AND THEN CAUSE A PULSE TO BE ISSUED ON TARGET EMULATOR MODULE
10673                                  ;       SIGNAL 'XRAS H'.  THE PROGRAM WILL NOW CHECK THE 'MEMBRK' FLIP-FLOP TO
10674                                  ;       BE SET TO A ONE AS A RESULT OF A PULSE ON 'XRAS H' AND THE MEMORY
10675                                  ;       SIMULATOR SYSTEM BUS SIGNAL 'MSBRK H' BEING ASSERTED HIGH.  THE PROGRAM
10676                                  ;       WILL PRESET THE 'WRV' FLIP-FLOP BY PULSING MEMORY SIMULATOR SIGNAL 'RST H'
10677                                  ;       AND CHECK THAT THE SIGNAL 'MSBRK H' WENT TO THE LOW STATE AS A RESULT OF
10678                                  ;       THE 'WRV' FLIP-FLOP BEING PRESET.  THE PROGRAM WILL CLEAR THE 'MEMBRK'
10679                                  ;       FLIP-FLOP BY PULSING TARGET EMULATOR SISGNAL 'BRKRES L' AND CHECK THAT
10680                                  ;       THE 'MEMBRK' FLIP-FLOP CLEARED.
10681                                  ;--
10682
10683    030116                        BGNTST
10684    030116                   T10::
10685    030116  004737  007440        JSR     PC,INITMD                  ;INITIALIZE MDE/T-11 SYSTEM MODULES
10686    030122                        BGNSEG
10687    030122  104404                TRAP    C$BSEG
10688
10689                                  ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10690                                  ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10691
10692    030124  004737  011250        JSR     PC,SLCTMS                  ;SELECT MEMORY SIMULATOR MODULE
10693
10694                                  ;GO LOAD, READ AND CHECK THE MEMORY SIMULATOR MAP PROTECTION RAM.  THE
10695                                  ;MAP PROTECTION RAM WILL HAVE THE BITS 'MUTB H' AND 'MPIN H' SET TO
10696                                  ;ONES FOR ALL ADDRESSES IN THE MAP PROTECTION RAM.  MAP PROTECTION RAM
10697                                  ;BITS 'WRE H' AND 'RDE H' WILL BE SET TO ONES FOR THE FIRST 16K WORDS OF
10698                                  ;MEMORY SIMULATOR RAM AND TO ZEROES FOR ALL ADDRESSES ABOVE 16K WORDS.
10699                                  ;WHEN 'RDE H' AND 'WRE H' ARE SET TO ONES, READ AND WRITES ARE ALLOWED
10700                                  ;TO THOSE ADDRESSES.
10701
10702    030130  004737  011356        JSR     PC,MPRAM                   ;GO LOAD, READ AND CHECK MAP PROTECT RAM
10703
10704                                  ;GO LOAD, READ AND CHECK MODULE SELECT RAM 0.  THE FOLLOWING DATA
10705                                  ;PATTERNS: 1, 2, 4, 10, 0, 0, 0, AND 0 WILL BE LOADED INTO CONSECUTIVE
10706                                  ;LOCATIONS OF MODULE SELECT RAM 0 STARTING AT ADDRESS 0.  THESE PATTERNS
10707                                  ;WILL ENABLE THE FIRST 16K WORDS OF THE MEMORY SIMULATOR RAM TO BE ADDRESSED
10708
10709    030134  004737  011642        JSR     PC,MSRAM0                  ;LOAD, READ AND CHECK MODULE SELECT RAM 0
10710
10711                                  ;GO LOAD, READ AND CHECK MODULE SELECT RAM 1.  THE FOLLOWING DATA PATTERNS
10712                                  ;WILL BE LOADED INTO CONSECUTIVE LOCATIONS OF MODULE SELECT RAM 1 STARTING
10713                                  ;AT ADDRESS 0; 17, 0, 0 AND 0.  THESE PATTERNS WILL ENABLE THE FIRST 32K
```

C 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 208
CVCDDB.P11   14-JUN-82 09:54   TEST 10: CHECK WRITE TO MS TO SET MSBRK H AND TE MEMBRK H   SEQ 0208

```
10714                                                  ;WORDS OF MEMORY SIMULATOR RAM TO BE SELECTED WHEN ADDRESSED.
10715
10716    030140  004737  012012                        JSR     PC,MSRAM1               ;LOAD, READ AND CHECK MODULE SELECT RAM 1
10717
10718                                                  ;SET THE SIGNAL "CTS H" TO A ONE IN CONTROL REGISTER 0.  THIS WILL
10719                                                  ;ENABLE THE SYSTEM BUS SIGNALS TO AND FROM THE MEMORY SIMULATOR LOGIC.
10720                                                  ;IN THIS TEST, "CTS H" ON A ONE WILL ENABLE THE SYSTEM BUS ADDRESSES TO
10721                                                  ;THE MEMORY SIMULATOR MODULE AND THE MEMORY SIMULATOR RAM DATA ONTO THE
10722                                                  ;SYSTEM BUS.
10723
10724    030144  052737  000002  002234                BIS     #CTSH,SOLOAD            ;SETUP BIT TO BE LOADED
10725    030152  004737  010506                        JSR     PC,LDRDS0              ;GO LOAD, READ AND CHECK CONTROL REG 2
10726    030156  001405                                BEQ     1$                     ;IF LOADED OK THEN CONTINUE
10727    030160                                        ERRDF   1,,SOEROR              ;CONTPOL REGISTER 0 NOT EQUAL EXPECTED
10728    030160  104455                                TRAP    C$ERDF
10729    030162  000001                                .WORD   1
10730    030164  000000                                .WORD   0
10731    030166  005306                                .WORD   SOEROR
10732    030170                                        CKLOOP
10733    030170  104406                                TRAP    C$CLP1
10734
10735                                                  ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10736                                                  ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10737
10738    030172  004737  012214         1$:            JSR     PC,SLCTTE              ;SELECT TARGET EMULATOR MODULE
10739
10740                                                  ;SET ADAL REGISTER BITS 14,10,9 AND 4 TO A ONE AND PULSE THE SIGNAL "BRKRES L"
10741                                                  ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
10742                                                  ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
10743                                                  ;THE SIGNAL "BRKRES L" VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
10744                                                  ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
10745                                                  ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL "CKAI H" TO BE PULSED VIA THE
10746                                                  ;THE SIGNAL "RASP L" LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
10747                                                  ;ONE WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN
10748                                                  ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
10749
10750    030176  012737  043020  002334                MOV     #ADAL14!ADAL10!ADAL9!ADAL4,T2LOAD ;SETUP BITS TO BE LOADED
10751    030204  004737  012766                        JSR     PC,BRKRES              ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
10752
10753                                                  ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
10754                                                  ;REG WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REG 6
10755
10756    030210  004537  012234                        JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
10757    030214  000003                                .WORD   HDAL                   ;SELECT THE HDAL REGISTER
10758
10759                                                  ;SET HDAL REGISTER BITS 9 AND 2 TO A ONE AND HDAL BITS 14, 11, 4 + 3  TO A
10760                                                  ;ZERO.  HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO SET THE T-11 TIMING
10761                                                  ;AND CONTROL SIGNALS.  HDAL9 H ON A ONE WILL ENABLE THE OUTPUTS OF THE
10762                                                  ;DIAGNOSTIC ADDRESS REGISTER ONTO THE SYSTEM ADDRESS BUS.  HDAL REGISTER
10763                                                  ;BITS 14 AND 11 ON A ZERO WILL SET ADDRESS BITS 17 AND 16 TO A ZERO.
10764                                                  ;HDAL REGISTER BITS 4 AND 3 SET TO ZEROES WILL SET THE SIGNALS XR/WLB L
10765                                                  ;AND XR/WHBL TO THE HIGH STATE.  THESE SIGNALS WILL CAUSE THE SIGNALS
10766                                                  ;"WT HB H AND WT LB H" TO BE ASSERTED HIGH LATER IN THIS TEST WHEN THE
10767                                                  ;SIGNAL XPI H IS SET TO THE HIGH STATE FROM THE LOW STATE.
10768
10769    030216  012737  001004  002346                MOV     #HDAL9!HDAL2,T6LOAD    ;SET HDAL BITS 9 AND 2 TO ONES
```

D 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 209
CVCDDB.P11   14-JUN-82 09:54   TEST 10: CHECK WRITE TO MS TO SET MSBRK H AND TE MEMBRK H   SEQ 0209

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10770  030224  004737  011216              JSR    PC,LDRDT6          ;GO LOAD, READ AND CHECK HDAL REGISTER
10771  030230  001405                       BEQ    2$                 ;IF LOADED OK THEN CONTINUE
10772  030232                               ERRDF  12,HDALRG,TO6ERR   ;HDAL REGISTER NOT EQUAL EXPECTED
10773  030232  104455                       TRAP   C$ERDF
10774  030234  000014                       .WORD  12
10775  030236  003756                       .WORD  HDALRG
10776  030240  006732                       .WORD  TO6ERR
10777  030242                               CKLOOP
10778  030242  104406                       TRAP   C$CLP1

10779
10780                                        ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
10781                                        ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
10782                                        ;FLIP-FLOPS ON THE TARGET EMULATOR MODULE NOT CLEARED BY 'BRKRES L'.
10783
10784  030244  005037  002340       2$:     CLR    T4LOAD             ;SETUP TO CLEAR ALL OTHER R/W BITS
10785  030250  004737  012706               JSR    PC,CLRPSM          ;PULSE INVD L VIA VDAL2 H

10786
10787                                        ;SELECT MODE REG BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON A WRITE OR
10788                                        ;READ COMMAND TO CONTROL REG 6, THE MODE REG WILL BE WRITTEN OR READ
10789
10790  030254  004537  012234               JSR    R5,SELTER          ;SELECT REGISTER SPECIFIED BY NEXT WORD
10791  030260  000004                        .WORD  MODE               ;SELECT THE MODE REGISTER

10792
10793                                        ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
10794                                        ;ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
10795
10796  030262  005037  002346               CLR    T6LOAD             ;SETUP TO CLEAR ALL MODE REGISTER BITS
10797  030266  004737  011216               JSR    PC,LDRDT6          ;GO LOAD, READ AND CHECK MODE REGISTER
10798  030272  001405                        BEQ    3$                 ;IF LOADED OK THEN CONTINUE
10799  030274                                ERRDF  12,MODREG,TO6ERR   ;MODE REGISTER NOT EQUAL EXPECTED
10800  030274  104455                        TRAP   C$ERDF
10801  030276  000014                        .WORD  12
10802  030300  004002                        .WORD  MODREG
10803  030302  006732                        .WORD  TO6ERR
10804  030304                                CKLOOP
10805  030304  104406                        TRAP   C$CLP1

10806
10807                                        ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
10808                                        ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
10809                                        ;READ COMMAND TO CONTROL REGISTER 6..  THE EOAI REGISTER NEEDS FDAL0 H
10810                                        ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
10811                                        ;TER WILL BE ADDRESSED.
10812
10813  030306  004537  012234       3$:     JSR    R5,SELTER          ;SELECT REGISTER SPECIFIED BY NEXT WORD
10814  030312  000002                        .WORD  FDAL               ;SELECT EOAI AND FDAL REGISTER

10815
10816                                        ;LOAD, READ AND CHECK FDAL AND EOAI REGISTER.  THE EOAI REGISTER WILL
10817                                        ;BE LOADED AND CHECKED FOR ZEROES.  THE FDAL REGISTER WILL BE LOADED AND
10818                                        ;CHECKED FOR A DATA PATTERN OF ONE (FDAL0 H = 1).
10819
10820  030314  012737  000001  002346       MOV    #FDAL0,T6LOAD      ;SETUP EOAI AND FDAL REG DATA PATTERN
10821  030322  004737  011216               JSR    PC,LDRDT6          ;GO LOAD, READ AND CHECK EOAI + FDAL REG
10822  030326  001405                        BEQ    4$                 ;IF LOADED OK THEN CONTINUE
10823  030330                                ERRDF  12,EOAIFD,TO6ERR   ;EOAI OR FDAL REGISTER ERROR
10824  030330  104455                        TRAP   C$ERDF
10825  030332  000014                        .WORD  12
```

```
10826  030334  004047                          .WORD   EOAIFD
10827  030336  006732                          .WORD   TO6ERR
10828  030340                          CKLOOP
10829  030340  104406                          TRAP    C$CLP1
10830
10831                                  ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
10832                                  ;2:0 TO A 0.  THE DIAGNSOTIC ADDRESS REGISTER WILL BE WRITTEN WITH A DATA
10833                                  ;PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.  THE DIAGNOSTIC ADDRESS
10834                                  ;REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER BIT 10
10835                                  ;BEING SET TO A ONE PREVIOUSLY.  ON A READ COMMAND TO CONTROL REGISTER
10836                                  ;6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
10837
10838  030342  004537  012234    4$:         JSR     R5,SELTER                 ;SELECT REGISTER SPECIFIED BY NEXT WORD
10839  030346  000000                          .WORD   ADDRES                    ;SELECT DIAG ADDRESS REG AND ADDRESS BUS
10840
10841                                  ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA PATTERN
10842                                  ;OF 100000.  THIS WILL CAUSE MEMORY NOT MAPPED TO BE SELECTED LATER ON IN
10843                                  ;THIS TEST.  ADDRESS BITS 17 AND 16 WERE SET TO A ZERO EARLIER IN THIS
10844                                  ;TEST VIA THE HDAL REGISTER.
10845
10846  030350  012737  100000  002346    MOV     #ADDR15,T6LOAD            ;SETUP DATA PATTERN OF 100000
10847  030356  004737  011216            JSR     PC,LDRDT6                 ;LOAD, READ ADN CHECK DIAG ADDRESS REG
10848  030362  001405                    BEQ     5$                       ;IF LOADED OK THEN CONTINUE
10849  030364                          ERRDF   12,ADDRRG,TO6ERR           ;DIAGNOSTIC ADDRESS REGISTER ERROR
10850  030364  104455                    TRAP    C$ERDF
10851  030366  000014                    .WORD   12
10852  030370  004144                    .WORD   ADDRRG
10853  030372  006732                    .WORD   TO6ERR
10854  030374                          CKLOOP
10855  030374  104406                    TRAP    C$CLP1
10856
10857                                  ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
10858                                  ;CHANGES OCCURED DURING THE PAST SEQUENCES.
10859
10860  030376  004737  011200    5$:         JSR     PC,READT4                 ;READ AND CHECK VDAL REGISTER
10861  030402  001405                    BEQ     6$                       ;IF NO CHANGES THEN CONTINUE
10862  030404                          ERRDF   11,VDALRG,T4EROR           ;VDAL OR PAUSE STATE MACHINE ERROR
10863  030404  104455                    TRAP    C$ERDF
10864  030406  000013                    .WORD   11
10865  030410  003710                    .WORD   VDALRG
10866  030412  006716                    .WORD   T4EROR
10867  030414                          CKLOOP
10868  030414  104406                    TRAP    C$CLP1
10869
10870                                  ;RE-SELECT THE HDAL REG BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL REG
10871                                  ;WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL REG 6.
10872
10873  030416  004537  012234    6$:         JSR     R5,SELTER                 ;SELECT REGISTER SPECIFIED BY NEXT WORD
10874  030422  000003                    .WORD   HDAL                     ;SELECT THE HDAL REGISTER
10875  030424  012737  001004  002346    MOV     #HDAL9!HDAL2,T6LOAD       ;BITS THAT WERE PREVIOUSLY LOADED
10876
10877                                  ;PERFORM A T-11 TIMING CYCLE BY DOING THE FOLLOWING TIMING SEQUENCE:
10878                                  ;  1. SET XRAS H AND PRAS H TO THE HIGH STATE
10879                                  ;  2. SET XCAS H AND PCAS H TO THE HIGH STATE
10880                                  ;  3. SET XPI L AND PPI L TO THE LOW STATE
10881                                  ;  4. SET XCAS H AND PCAS H TO THE LOW STATE
```

F 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 211
CVCDDB.P11   14-JUN-82 09:54   TEST 10: CHECK WRITE TO MS TO SET MSBRK H AND TE MEMBRK H   SEQ 0211

```
10882                                        ;  5. SET XPI L AND PPI L TO THE HIGH STATE
10883                                        ;  6. SET XRAS H AND PRAS H TO THE LOW STATE
10884                                        ;WHEN PRAS H IS SET HIGH, THE SYSTEM ADDRESS BUS, WHICH CONTAINS THE
10885                                        ;TARGET EMULATORS DIAGNOSTIC ADDRESS REGISTER DATA, WILL BE CLOCKED INTO
10886                                        ;THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES VIA THE SIGNAL ADVAL H.
10887                                        ;WHEN XPI H IS SET HIGH AND THE SIGNALS XR/WHB L AND XR/WLB L ARE
10888                                        ;ASSERTED HIGH, THE SIGNALS WT HB H AND WT LB H WILL BE SET TO THE HIGH
10889                                        ;STATE.  THESE TWO SIGNALS WILL ATTEMPT TO WRITE DATA INTO THE MEMORY
10890                                        ;SIMULATOR MODULE'S RAMS.  HOWEVER, THE ADDRESS UNDER TEST (100000) IS
10891                                        ;MAPPED TO INHIBIT READS AND WRITES, THEREFORE, THE MEMORY SIMULATOR'S
10892                                        ;WRV (WRITE VIOLATION) FLIP-FLOP SHOULD BE CLEARED VIA PULSES ON THE
10893                                        ;SIGNALS WRHB L AND WRLB L WHEN THE SIGNAL WRE H IS ASSERTED LOW.  AS A
10894                                        ;RESULT OF THE WRV FLIP-FLOP BEING CLEARED, THE SIGNAL MSBRK H WILL BE
10895                                        ;ASSERTED HIGH VIA THE SIGNAL BRK L.  THE SIGNAL MSBRK H WILL NOT BE
10896                                        ;CLOCKED INTO THE TARGET EMULATOR'S MEMBRK FLIP-FLOP UNTIL THE SIGNAL
10897                                        ;XRAS H IS PULSED ON THE TARGET EMULATOR MODULE.
10898
10899   030432  004737  012300               JSR     PC,XRASH                ;SET XRAS H AND PRAS H TO HIGH STATE
10900   030436  004737  012404               JSR     PC,XCASH                ;SET XCAS H AND PCAS H TO HIGH STATE
10901   030442  004737  012510               JSR     PC,XPIH                 ;SET XPI L AND PPI L TO LOW STATE
10902   030446  004737  012436               JSR     PC,XCASL                ;SET XCAS H AND PCAS H TO LOW STATE
10903   030452  004737  012542               JSR     PC,XPIL                 ;SET XPI L AND PPI L TO HIGH STATE
10904   030456  004737  012332               JSR     PC,XRASL                ;SET XRAS H AND PRAS H TO LOW STATE
10905
10906                                        ;READ TARGET EMULATORS GDAL REGISTER TO CHECK THAT NO CHANGES HAVE
10907                                        ;OCCURED AS A RESULT OF THE ABOVE TIMING SEQUENCE.  THE SIGNAL MEMBRK H
10908                                        ;SHOULD BE ASSERTED LOW UNTIL A PULSE IS ISSUED ON THE SIGNAL XRAS H AGAIN.
10909
10910   030462  004737  011114               JSR     PC,READTO               ;READ AND CHECK GDAL REGISTER
10911   030466  001405                       BEQ     7$                      ;IF DATA OK THEN CONTINUE
10912   030470                               ERRDF   9,GDALRG,TOEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
10913   030470  104455                       TRAP    C$ERDF
10914   030472  000011                       .WORD   9
10915   030474  003640                       .WORD   GDALRG
10916   030476  006666                       .WORD   TOEROR
10917   030500                               CKLOOP
10918   030500  104406                       TRAP    C$CLP1
10919
10920                                        ;READ VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS ASSERTED HIGH
10921                                        ;AS A RESULT OF THE SIGNALS CYCLE L, ENEDC H, PSM L, AND SOP L BEING
10922                                        ;ASSERTED TO THE HIGH STATE.
10923
10924   030502  052737  000020  002342  7$:  BIS     #VDAL4,T4GOOD           ;EXPECT EDEOC H TO BE A ONE
10925   030510  004737  011200               JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
10926   030514  001405                       BEQ     8$                      ;IF OK THEN CONTINUE
10927   030516                               ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
10928   030516  104455                       TRAP    C$ERDF
10929   030520  000013                       .WORD   11
10930   030522  003710                       .WORD   VDALRG
10931   030524  006716                       .WORD   T4EROR
10932   030526                               CKLOOP
10933   030526  104406                       TRAP    C$CLP1
10934
10935                                        ;SELECT MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10936                                        ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
10937
```

G 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 212
CVCDDB.P11   14-JUN-82 09:54   TEST 10: CHECK WRITE TO MS TO SET MSBRK H AND TE MEMBRK H   SEQ 0212

```
10938   030530  004737  011250        8$:     JSR    PC,SLCTMS                 ;SELECT THE MEMORY SIMULATOR MODULE
10939
10940                                          ;READ CONTROL REGISTER 4 BITS MSAD 15:0 TO CHECK THAT THE TARGET EMULATORS
10941                                          ;DIAGNOSTIC ADDRESS REGISTER, WHICH WAS ENABLED TO THE SYSTEM ADDRESS
10942                                          ;BUS, WAS CLOCKED INTO THE MEMORY SIMULATORS SYSTEM ADDRESS BUS LATCHES.
10943                                          ;THE ADDRESS READ SHOULD BE EQUAL TO 10000.
10944
10945   030534  012737  100000  002254        MOV    #MSAD15,S4LOAD            ;SETUP EXPECTED ADDRESS FOR COMPARE
10946   030542  004737  010614                JSR    PC,READS4                 ;READ AND CHECK MSAD BITS 15:0
10947   030546  001405                         BEQ    9$                        ;IF ADDRESS OK THEN CONTINUE
10948   030550                                ERRDF  3,TEMSAD,S04ERR           ;TE TO MS ADDRESS BUS ERROR - MSAD 15:0
10949   030550  104455                         TRAP   C$ERDF
10950   030552  000003                         .WORD  3
10951   030554  002534                         .WORD  TEMSAD
10952   030556  005406                         .WORD  S04ERR
10953   030560                                CKLOOP
10954   030560  104406                         TRAP   C$CLP1
10955
10956                                          ;READ AND CHECK CONTROL REGISTER 2 BITS.  MSAD16 H AND MSAD17 H SHOULD
10957                                          ;BE READ AS ZEROES AS A RESULT OF DATA LOADED INTO THE TARGET EMULATOR
10958                                          ;MODULE.  THE SIGNALS MSEL0 H AND MSEL1 H WILL BE IGNORED BECAUSE THESE
10959                                          ;SIGNALS ARE TRI-STATED AS A REUSLT OF THE SIGNAL CTS H BEING ASSERTED
10960                                          ;HIGH.  THE SIGNALS ESR H AND MSBRK H SHOULD BE READ AS ONES. THE SIGNAL
10961                                          ;MSBRK H SHOULD BE A ONE AS A RESULT OF TRYING TO WRITE ADDRESS 10000 WHICH
10962                                          ;WAS MAPPED TO INHIBIT READS AND WRITES.  THE WRV FLIP-FLOP SHOULD BE
10963                                          ;CLEARED THUS CAUSING THE SIGNAL BRK L TO BE ASSERTED LOW WHICH WILL
10964                                          ;CAUSE THE SIGNAL MSBRK H TO BE ASSERTED HIGH.
10965
10966   030562  012737  177414  002250  9$:   MOV    #177414,S2MASK           ;SETUP TO IGNORE UNWANTED BITS
10967   030570  005037  002244                CLR    S2LOAD                    ;SETUP VALUES FOR R/W BITS
10968   030574  012737  000240  002246        MOV    #ESRH!MSBRKH,S2GOOD       ;EXPECT ESR H AND MSBRK H TO BE ONES
10969   030602  004737  010562                JSR    PC,READS2                 ;READ AND CHECK CONTROL REGISTER 2
10970   030606  001405                         BEQ    10$                       ;IF DATA OK THEN CONTINUE
10971   030610                                ERRDF  2,,S2EROR                 ;CONTROL REGISTER 2 NOT EQUAL EPXETCED
10972   030610  104455                         TRAP   C$ERDF
10973   030612  000002                         .WORD  2
10974   030614  000000                         .WORD  0
10975   030616  005322                         .WORD  S2EROR
10976   030620                                CKLOOP
10977   030620  104406                         TRAP   C$CLP1
10978
10979                                          ;READ CONTROL REGISTER 0 TO CHECK THAT THE WRV F/F IS SET TO A ONE
10980
10981   030622  052737  000040  002236  10$:  BIS    #WRVH,S0GOOD             ;EXPECT WRV FLIP-FLOP TO BE A ONE
10982   030630  004737  010522                JSR    PC,READS0                 ;READ AND CHECK CONTROL REGISTER 0
10983   030634  001405                         BEQ    11$                       ;IF OK THEN CONTINUE
10984   030636                                ERRDF  1,,S0EROR                 ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
10985   030636  104455                         TRAP   C$ERDF
10986   030640  000001                         .WORD  1
10987   030642  000000                         .WORD  0
10988   030644  005306                         .WORD  S0EROR
10989   030646                                CKLOOP
10990   030646  104406                         TRAP   C$CLP1
10991
10992                                          ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
10993                                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
```

H 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 213
CVCDDB.P11   14-JUN-82 09:54   TEST 10: CHECK WRITE TO MS TO SET MSBRK H AND TE MEMBRK H   SEQ 0213

```
10994
10995    030650  004737  012214            11$:   JSR    PC,SLCTTE                ;SELECT THE TARGET EMULATOR MODULE
10996
10997                                              ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL REGISTER BIT 12.
10998                                              ;WHEN XRAS H IS PULSED, THE SIGNAL MSBRK H FROM THE MEMORY SIMULATOR
10999                                              ;MODULE, WHICH IS HIGH, SHOULD BE CLOCKED INTO THE MEMBRK FLIP-FLOP THUS
11000                                              ;SETTING THE SIGNAL MEMBRK H TO THE HIGH STATE
11001
11002    030654  004737  012266                   JSR    PC,XRAS                  ;GO PULSE XRAS H VIA HDAL12 H
11003
11004                                              ;READ GDAL REGISTER TO CHECK THAT THE SIGNAL MEMBRK H IS ASSERTED HIGH
11005                                              ;AS A RESULT OF MSBRK H BEING HIGH AND A PULSE ON THE SIGBAL XRAS H.
11006                                              ;THE MEMBRK FLIP-FLOP SHOULD NOW BE SET TO A ONE.
11007
11008    030660  052737  000040  002326           BIS    #MEMBRK,TOGOOD           ;EXPECT MEMBRK H TO BE A ONE
11009    030666  004737  011114                   JSR    PC,READTO                ;READ AND CHECK GDAL REGISTER
11010    030672  001405                           BEQ    12$                      ;IF OK THEN CONTINUE
11011    030674                                   ERRDF  9,GDALRG,TOEROR          ;MEMBRK FLIP-FLOP PROBABLY NOT SET
11012    030674  104455                           TRAP   C$ERDF
11013    030676  000011                           .WORD  9
11014    030700  003640                           .WORD  GDALRG
11015    030702  006666                           .WORD  TOEROR
11016    030704                                   CKLOOP
11017    030704  104406                           TRAP   C$CLP1
11018
11019                                              ;READ VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H IS ASSERTED LOW
11020                                              ;WHEN MEMBRK H IS ASSERTED HIGH AND SOP L IS ASSERTED LOW.
11021
11022    030706  042737  000020  002342  12$:     BIC    #VDAL4,T4GOOD            ;EXPECT EDEOC H TO BE A 0
11023    030714  004737  011200                   JSR    PC,READT4                ;READ AND CHECK VDAL REGISTER
11024    030720  001405                           BEQ    13$                      ;IF OK THEN CONTINUE
11025    030722                                   ERRDF  11,VDALRG,T4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
11026    030722  104455                           TRAP   C$ERDF
11027    030724  000013                           .WORD  11
11028    030726  003710                           .WORD  VDALRG
11029    030730  006716                           .WORD  T4EROR
11030    030732                                   CKLOOP
11031    030732  104406                           TRAP   C$CLP1
11032
11033                                              ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11034                                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11035
11036    030734  004737  011250            13$:   JSR    PC,SLCTMS                ;SELECT THE MEMORY SIMULATOR MODULE
11037
11038                                              ;THE PROGRAM WILL PRESET THE RDV AND WRV FLIP-FLOPS BY PULSING THE
11039                                              ;SIGNAL RST H.  WHEN THE RDV AND WRV FLIP-FLOPS ARE BRESET THE SIGNAL
11040                                              ;MSBRK H WILL BE SET TO THE LOW STATE.
11041
11042    030740  004737  011270                   JSR    PC,MSRSTH                ;GO PULSE RST H TO PRESET WRV + RDV F/F'S
11043
11044                                              ;READ REG 2 TO CHECK THAT MSBRK H WENT TO A 0 AS A RESULT OF PULSING RST H.
11045
11046    030744  042737  000200  002246           BIC    #MSBRKH,S2GOOD           ;EXPECT MSBRK H TO BE A ZERO
11047    030752  004737  010562                   JSR    PC,READS2                ;READ AND CHECK CONTROL REGISTER 2
11048    030756  001405                           BEQ    14$                      ;IF OK THEN CONTINUE
11049    030760                                   ERRDF  2,,S2EROR                 ;MSBRK H PROBABLY NOT 0 AFTER RST H
```

I 1

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46 PAGE 214
CVCDDB.P11   14-JUN-82 09:54   TEST 10: CHECK WRITE TO MS TO SET MSBRK H AND TE MEMBRK H   SEQ 0214

```
11050  030760  104455                        TRAP    C$ERDF
11051  030762  000002                        .WORD   2
11052  030764  000000                        .WORD   0
11053  030766  005322                        .WORD   S2EROR
11054  030770                                CKLOOP
11055  030770  104406                        TRAP    C$CLP1
11056
11057                               ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11058                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11059
11060  030772  004737  012214      14$:      JSR     PC,SLCTTE           ;SELECT TARGET EMULATOR MODULE
11061
11062                               ;GO PULSE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT
11063                               ;0. A PULSE ON THE SIGNAL BRKRES L WILL CAUSE THE MEMBRK F/F TO BE O'ED.
11064
11065  030776  004737  012766                JSR     PC,BRKRES           ;GO PULSE BRKRES L VIA ADAL0 H
11066
11067                               ;READ GDAL REGISTER TO CHECK THAT BRKRES L CLEARED MEMBRK FLIP-FLOP
11068
11069  031002  042737  000040 002326 BIC     #MEMBRK,TOGOOD      ;EXPECT MEMBRK H TO BE A ZERO
11070  031010  004737  011114                JSR     PC,READT0           ;READ AND CHECK GDAL REGISTER
11071  031014  001405                        BEQ     15$                 ;IF OK THEN CONTINUE
11072  031016                                ERRDF   9,GDALRG,TOEROR     ;MEMBRK F/F PROBABLY NOT 0 AFTER RST H
11073  031016  104455                        TRAP    C$ERDF
11074  031020  000011                        .WORD   9
11075  031022  003640                        .WORD   GDALRG
11076  031024  006666                        .WORD   TOEROR
11077  031026                                CKLOOP
11078  031026  104406                        TRAP    C$CLP1
11079
11080                               ;CHECK THAT THE SIGNAL EDEOC H IS NOW SET TO A 1 AS A RESULT OF THE SIGNAL
11081                               ;SOP L RETURNING TO THE HIGH STATE AFTER THE SIGNAL MEMBRK H WENT TO LOW STATE.
11082
11083  031030  052737  000020 002342 15$:    BIS     #VDAL4,T4GOOD       ;EXPECT EDEOC H TO BE A ONE
11084  031036  004737  011200                JSR     PC,READT4           ;READ AND CHECK THE VDAL REGISTER
11085  031042  001405                        BEQ     16$                 ;IF VDAL REGISTER OK THEN CONTINUE
11086  031044                                ERRDF   11,VDALRG,T4EROR    ;VDAL REGISTER NOT EQUAL EXPECTED
11087  031044  104455                        TRAP    C$ERDF
11088  031046  000013                        .WORD   11
11089  031050  003710                        .WORD   VDALRG
11090  031052  006716                        .WORD   T4EROR
11091  031054                                CKLOOP
11092  031054  104406                        TRAP    C$CLP1
11093
11094                               ;ISSUE A PULSE ON THE SIGNAL INVD L TO INITIALIZE ALL OTHER FLIP-FLOPS
11095                               ;ON THE MODULE NOT CLEARED VIA THE SIGNAL BRKRES L.
11096
11097  031056  005037  002340      16$:      CLR     T4LOAD              ;SETUP TO CLEAR ALL VDAL R/W BITS
11098  031062  004737  012706                JSR     PC,CLRPSM           ;PULSE INVD L VIA VDAL2 H
11099  031066                                ENDSEG
11100  031066                      10000$:
11101  031066  104405                        TRAP    C$ESEG
11102  031070                                ENDTST
11103  031070                      L10046:
11104  031070  104401                        TRAP    C$ETST
```

J 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 215
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0215

```
11105                                    .SBTTL  TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE
11106
11107                            ;++
11108                            ;        THIS TEST WILL CHECK THAT TARGET EMULATOR FDAL REGISTER BITS 7:2 CAN
11109                            ;        BE CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES IN 16 BIT MODE WHEN THE
11110                            ;        TARGET EMULATOR MODULE IS ADDRESSING A LOCATION WHICH IS MAPPED ON THE
11111                            ;        MEMORY SIMULATOR MODULE TO ALLOW READS AND WRITES TO THE TARGET RAM.
11112                            ;        TO CHECK THAT THE TDAL LATCHES WERE CLOCKED WITH FDAL REGISTER DATA,
11113                            ;        THE PROGRAM WILL ENABLE THE TDAL LATCHES TO THE EIDAL BUS WITH THE
11114                            ;        TARGET RAM STILL BEING ADDRESSED.  THE PROGRAM WILL THEN READ AND CHECK
11115                            ;        THE EIDAL BUS TO CONTAIN THE CORRECT FDAL REGISTER DATA.
11116                            ;--
11117
11118   031072                           BGNTST
11119   031072                   T11::
11120
11121   031072  004737  007440          JSR     PC,INITMD               ;INITIALIZE MDE/T-11 SYSTEM MODULES
11122
11123   031076                           BGNSEG
11124   031076  104404                   TRAP    C$BSEG
11125
11126                            ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11127                            ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11128
11129   031100  004737  011250          JSR     PC,SLCTMS               ;SELECT THE MEMORY SIMULATOR MODULE
11130
11131                            ;TOGGLE THE SIGNAL RST H IN CONTROL REGISTER 0 AND SET THE SIGNAL MP H
11132                            ;TO A ONE.  A PULSE ON THE SIGNAL RST H WILL PRESET THE WRV AND RDV
11133                            ;FLIP-FLOPS THUS CAUSING THE SIGNAL BRK L TO BE ASSERTED HIGH.  SETTING
11134                            ;THE SIGNAL MP H TO A ONE WILL ENABLE MAP PROTECTION BITS MPIN H,
11135                            ;WRE H AND RDE H TO THE SYSTEM BUS ALONG WITH THE SIGNAL BRK L.  THESE
11136                            ;SIGNALS WILL BE ENABLED TO THE SYSTEM BUS AS ETR H, WVIOL H, MSBRK H
11137                            ;AND RDE L.  SETTING THE SIGNAL MP H WILL ALSO ENABLE THE SIGNALS MPIN H
11138                            ;WRE H, AND BRK L TO CONTROL REGISTER 2 AS SIGNALS ESR H, WREN H AND
11139                            ;MSBRK H RESPECTIVELY.
11140
11141   031104  112737  000005  002234  MOVB    #RSTH!MPH,SOLOAD        ;SETUP BITS TO BE LOADED
11142   031112  004737  011270          JSR     PC,MSRSTH               ;PULSE RST H AND SET MP H TO A ONE
11143
11144                            ;THE FOLLOWING SECTION WILL LOAD, READ AND CHECK THE MEMORY SIMULATOR
11145                            ;MAP PROTECTION RAM.  THE MAP PROTECTION RAM WILL BE SETUP TO ALLOW
11146                            ;READS AND WRITES TO THE FIRST 128 WORDS OF MEMORY.  THE FIRST 128
11147                            ;WORDS OF MEMORY WILL BE MAPPED TO SELECT THE TARGET MEMORY.  THE
11148                            ;REMAINING LOCATIONS OF THE MAP PROTECTION RAM WILL BE MAPPED TO THE
11149                            ;MEMORY SIMULATOR RAM AND SETUP TO INHIBIT READS AND WRITES TO THOSE
11150                            ;LOCATIONS (777776-000400).
11151
11152   031116  005037  002254          CLR     S4LOAD                  ;SETUP STARTING MSAD 15:0 BITS
11153   031122  012737  000010  002244  MOV     #MSEL1,S2LOAD           ;SETUP STARTING MSAD 17:16 BITS AND
11154                                                                    ;BITS TO SELECT MAP PROTECTION RAM
11155
11156   031130                   1$:     BGNSEG
11157   031130  104404                   TRAP    C$BSEG
11158
11159                            ;SET THE SIGNAL MSEL1 H TO A ONE AND MSEL0 H TO A ZERO.  THIS WILL
11160                            ;CAUSE THE MAP PROTECTION RAM TO BE SELECTED VIA THE SIGNAL SMPM H
```

K 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 216
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0216

```
11161                                              ;WHEN A READ OR WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6.  MSAD
11162                                              ;BITS 17 AND 16 IN CONTROL REGISTER 2 WILL BE LOADED AND CHECKED FOR
11163                                              ;THE ADDRESS BEING TESTED.
11164
11165   031132  012737  177540  002250             MOV     #177540,S2MASK       ;SETUP TO IGNORE ESR H + WREN H
11166   031140  004737  010546                      JSR     PC,LDRDS2            ;LOAD, READ AND CHECK CONTROL REG 2
11167   031144  001405                              BEQ     2$                   ;IF LOADED OK THEN CONTINUE
11168   031146                                      ERRDF   2,,S2EROR            ;CONTROL REG 2 NOT EQUAL EXPECTED
11169   031146  104455                              TRAP    C$ERDF
11170   031150  000002                              .WORD   2
11171   031152  000000                              .WORD   0
11172   031154  005322                              .WORD   S2EROR
11173   031156                                      CKLOOP
11174   031156  104406                              TRAP    C$CLP1
11175
11176                                              ;LOAD, READ AND CHECK CONTROL REGISTER 4 FOR THE ADDRESS BEING TESTED.
11177                                              ;CONTROL REGISTER 4 CONTAINS BITS FOR MSAD ADDRESS BITS 15:0.
11178
11179   031160  004737  010606            2$:      JSR     PC,LDRDS4            ;LOAD, READ AND CHECK CONTROL REG 4
11180   031164  001405                              BEQ     3$                   ;IF LOADED OK THEN CONTINUE
11181   031166                                      ERRDF   3,MSADRG,S4EROR      ;MSAD BITS 15:0 NOT EQUAL EXPECTED
11182   031166  104455                              TRAP    C$ERDF
11183   031170  000003                              .WORD   3
11184   031172  002510                              .WORD   MSADRG
11185   031174  005336                              .WORD   S4EROR
11186   031176                                      CKLOOP
11187   031176  104406                              TRAP    C$CLP1
11188
11189                                              ;LOAD, READ ADN CHECK MAP PROTECTION RAM LOCATION ADDRESSED BY MSAD
11190                                              ;BITS 17:0.  ADDRESSES 0 TO 376 WILL BE LOADED AND CHECKED WITH A
11191                                              ;DATA PATTERN OF 16.  ALL OTHER ADDRESSES WILL BE LOADED AND CHECKED
11192                                              ;WITH A DATA PATTERN OF 11.
11193
11194   031200  012737  177760  002264    3$:      MOV     #177760,S6MASK       ;SETUP TO IGNORE UNUSED BITS
11195   031206  012737  000011  002260             MOV     #MUTB!MPINH,S6LOAD   ;SETUP FOR ADDRESSES OVER 376
11196   031214  032737  000003  002244             BIT     #MSAD17!MSAD16,S2LOAD ;CHECK IF ADDRESS ABOVE 16K WORDS
11197   031222  001006                              BNE     4$                   ;IF YES - LOAD R/W VIOLATION SETUP
11198   031224  005737  002254                      TST     S4LOAD               ;CHECK IF ADDRESS WAS OVER 376
11199   031230  001003                              BNE     4$                   ;IF YES - LOAD R/W VIOLATION SETUP
11200   031232  012737  000016  002260             MOV     #MUTB!RDEH!WREH,S6LOAD ;SETUP TO ALLOW R/W TO FIRST 128 WORDS
11201   031240  004737  010632            4$:      JSR     PC,LDRDS6            ;LOAD, READ AND CHECK MAP PROTECT RAM
11202   031244  001405                              BEQ     5$                   ;IF LOADED OK THEN CONTINUE
11203   031246                                      ERRDF   4,MSGMP,S6ALLR       ;MAP PROTECT RAM DATA ERROR
11204   031246  104455                              TRAP    C$ERDF
11205   031250  000004                              .WORD   4
11206   031252  002603                              .WORD   MSGMP
11207   031254  005456                              .WORD   S6ALLR
11208   031256                                      CKLOOP
11209   031256  104406                              TRAP    C$CLP1
11210
11211                                              ;CHECK MAP PROTECTION RAM DATA BITS MPIN H AND WRE H IN CONTROL
11212                                              ;REGISTER 2 AS ESR H AND WREN H RESPECTIVELY.
11213
11214   031260  042737  000140  002250    5$:      BIC     #ESRH!WRENH,S2MASK   ;SETUP TO CHECK ESR H AND WREN H
11215   031266  052737  000100  002246             BIS     #WRENH,S2GOOD        ;EXPECT WREN H TO BE A ONE
11216   031274  032737  000006  002260             BIT     #WREH!RDEH,S6LOAD    ;CHECK IF RAM WAS W/R ENABLED
```

L 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 217
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0217

```
11217  031302  001006                        BNE     6$                      ;IF YES THEN GO READ CONTROL REG 2
11218  031304  042737  000100  002246        BIC     #WRENH,S2GOOD           ;THIS ADDRESS WAS NOT WRITE ENABLED
11219  031312  052737  000040  002246        BIS     #ESRH,S2GOOD            ;EXPECT ESR H TO BE SET TO A ONE
11220  031320  004737  010562         6$:    JSR     PC,READS2               ;GO READ AND CHECK CONTROL REG 2
11221  031324  001404                        BEQ     7$                      ;IF OK THEN CONTINUE
11222  031326                                ERRDF   2,MSGMPL,S2ALLR         ;REGISTER 2 NOT EQUAL EXPECTED
11223  031326  104455                        TRAP    C$ERDF
11224  031330  000002                        .WORD   2
11225  031332  002460                        .WORD   MSGMPL
11226  031334  005442                        .WORD   S2ALLR
11227  031336                         7$:    ENDSEG
11228  031336                         10001$:
11229  031336  104405                        TRAP    C$ESEG
11230
11231                                         ;UPDATE CONTROL REGISTERS 4 AND 2 FOR MSAD ADDRESS TO BE TESTED
11232
11233  031340  062737  000400  002254        ADD     #MSAD8,S4LOAD           ;UPDATE MSAD BITS 15:8 BY ONE
11234  031346  001270                        BNE     1$                      ;IF NOT 0 THEN LOAD NEXT RAM LOCATION
11235  031350  005237  002244                INC     S2LOAD                  ;UPDATE MSAD BITS 17:16 BY ONE
11236  031354  032737  000004  002244        BIT     #MSEL0,S2LOAD           ;CHECK IF ALL RAM LOCATIONS DONE
11237  031362  001662                        BEQ     1$                      ;IF NOT THEN LOAD NEXT RAM LOCATION
11238  031364  005337  002244                DEC     S2LOAD                  ;RESET REG 2 TO ACTUAL VALUE LOADED
11239
11240                                         ;SET THE SIGNAL CTS H TO A ONE IN CONTROL REGISTER 0.  WHEN CTS H IS
11241                                         ;SET TO A ONE,  THE SYSTEM BUS LATCHES WILL BE ENABLED TO THE MEMORY
11242                                         ;SIMULATOR MODULE.
11243
11244  031370  052737  000002  002234        BIS     #CTSH,S0LOAD            ;SETUP BIT TO SET CTS H TO A ONE
11245  031376  004737  010506                JSR     PC,LDRDS0               ;GO LOAD, READ AND CHECK REG 0
11246  031402  001404                        BEQ     8$                      ;IF LOADED OK THEN CONTINUE
11247  031404                                ERRDF   1,,S0EROR               ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
11248  031404  104455                        TRAP    C$ERDF
11249  031406  000001                        .WORD   1
11250  031410  000000                        .WORD   0
11251  031412  005306                        .WORD   S0EROR
11252  031414                         8$:    ENDSEG
11253  031414                         10000$:
11254  031414  104405                        TRAP    C$ESEG
11255
11256  031416                                BGNSEG
11257  031416  104404                        TRAP    C$BSEG
11258
11259                                         ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11260                                         ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11261
11262  031420  004737  012214                JSR     PC,SLCTTE               ;SELECT THE TARGET EMULATOR MODULE
11263
11264  031424  005037  002352                CLR     T6MASK                  ;RESET CONTROL REGISTER 6 MASK WORD
11265
11266                                         ;SET ADAL REGISTER BITS 14,10 AND 9 TO A ONE AND PULSE THE SIGNAL ''BRKRES L''
11267                                         ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
11268                                         ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
11269                                         ;THE SIGNAL ''BRKRES L'' VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
11270                                         ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
11271                                         ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL ''CKAI H'' TO BE PULSED VIA THE
11272                                         ;THE SIGNAL ''RASP L'' LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
```

M 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 218
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0218

```
11273                                       ;ZERO WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE PAUSE MODE WHEN
11274                                       ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
11275
11276   031430  012737  043000  002334      MOV     #ADAL14!ADAL10!ADAL9,T2LOAD  ;SETUP BITS TO BE LOADED
11277   031436  004737  012766              JSR     PC,BRKRES                    ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
11278
11279                                       ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
11280                                       ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
11281                                       ;REGISTER 6.
11282
11283   031442  004537  012234              JSR     R5,SELTER                    ;SELECT REGISTER SPECIFIED BY NEXT WORD
11284   031446  000003                      .WORD   HDAL                         ;SELECT THE HDAL REGISTER
11285
11286                                       ;SET HDAL REGISTER BITS 9, 6 AND 2 TO A ONE AND HDAL BITS 14, 11, 5, 4
11287                                       ;AND 3 TO A ZERO.  HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO CONTROL
11288                                       ;THE T-11 TIMING AND CONTROL SIGNALS.  HDAL9 H ON A ONE WILL ENABLE THE
11289                                       ;OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER TO THE SYSTEM ADDRESS BUS.
11290                                       ;HDAL14 H AND HDAL11 H ON A ZERO WILL SET SYSTEM ADDRESS BITS 17 AND 16
11291                                       ;TO A ZERO.  HDAL4 H AND HDAL3 H SET TO ZEROES WILL SET THE SIGNALS
11292                                       ;PR/WHB L AND PR/WLB L TO THE HIGH STATE.  THESE TWO SIGNALS WILL CAUSE
11293                                       ;THE SIGNALS DTLB L AND DTHB L TO BE ASSERTED LOW LATER ON IN THE TEST
11294                                       ;WHEN SOME OTHER GATING SIGNALS ARE ENABLED HIGH.  DTHB L AND DTLB L
11295                                       ;ASSERTED LOW WILL ENABLE THE CDAL BUS TO THE TDAL BUS.  HDAL5 H ON A
11296                                       ;ZERO AND HDAL6 H ON A ONE WILL CAUSE THE SIGNAL PSEL0 L TO BE ASSERTED
11297                                       ;HIGH AND PSEL1 L TO BE ASSERTED LOW.  PSEL1 L SET LOW WILL DISABLE ONE
11298                                       ;OF THE DATA PATHS TO THE TDAL BUS.  WITH PSEL0 L SET HIGH AND PSEL1 L
11299                                       ;SET LOW, THE SIGNAL INTER L WILL BE ASSERTED LOW THUS ENABLING FDAL
11300                                       ;REGISTER BITS 7:2 TO THE EODAL BUS AND CLEARING THE EOAI REGISTER.
11301
11302   031450  012737  001104  002346      MOV     #HDAL9!HDAL6!HDAL2,T6LOAD  ;SET HDAL BITS 9, 6 AND 2 TO ONES
11303   031456  004737  011216              JSR     PC,LDRDT6                    ;GO LOAD, READ AND CHECK HDAL REGISTER
11304   031462  001405                      BEQ     9$                           ;IF LOADED OK THEN CONTINUE
11305   031464                              ERRDF   12,HDALRG,T06ERR             ;HDAL REGISTER NOT EQUAL EXPECTED
11306   031464  104455                      TRAP    C$ERDF
11307   031466  000014                      .WORD   12
11308   031470  003756                      .WORD   HDALRG
11309   031472  006732                      .WORD   T06ERR
11310   031474                              CKLOOP
11311   031474  104406                      TRAP    C$CLP1
11312
11313                                       ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
11314                                       ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
11315                                       ;FLIP-FLOPS ON THE MODULE NOT CLEARED BY THE SIGNAL "BRKRES L".  SET
11316                                       ;THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
11317                                       ;ON A READ COMMAND TO CONTROL REGISTER 4, THE SIGNAL BTS1 H WILL BE SET
11318                                       ;TO A ONE AS A RESULT OF THE SIGNAL INTER L BEING ASSERTED LOW.  THE
11319                                       ;SIGNAL INTER L IS ASSERTED LOW AS A RESULT OF PSEL0 L BEING ASSERTED
11320                                       ;HIGH AND PSEL1 L BEING ASSERTED LOW.
11321
11322   031476  012737  000204  002340  9$: MOV     #VDAL7!VDAL2,T4LOAD         ;SETUP BITS TO BE LOADED
11323   031504  013737  002340  002342      MOV     T4LOAD,T4GOOD               ;COPY LOADED TO EXPECTED
11324   031512  052737  000040  002342      BIS     #VDAL5,T4GOOD               ;EXPECT BTS1 H TO BE A ONE
11325   031520  004737  011172              JSR     PC,LDRD4T                   ;GO LOAD, READ AND CHECK VDAL REG
11326   031524  001405                      BEQ     10$                         ;IF OK THEN CONTINUE
11327   031526                              ERRDF   11,VDALRG,T4EROR            ;VDAL REG NOT EQUAL TO EXPECTED
11328   031526  104455                      TRAP    C$ERDF
```

N 1

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 219
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0219

```
11329   031530   000013                          .WORD   11
11330   031532   003710                          .WORD   VDALRG
11331   031534   006716                          .WORD   T4EROR
11332   031536                          CKLOOP
11333   031536   104406                          TRAP    C$CLP1
11334   031540   042737  000004  002340  10$:    BIC     #VDAL2,T4LOAD          ;SET VDAL2 H TO THE LOW STATE
11335   031546   042737  000004  002342          BIC     #VDAL2,T4GOOD          ;SETUP TO EXPECT IT TO BE ZERO
11336   031554   004737  011172                  JSR     PC,LDRD4T              ;GO LOAD, READ AND CHECK VDAL REG
11337   031560   001405                          BEQ     11$                    ;IF OK THEN CONTINUE
11338   031562                          ERRDF   11,VDALRG,T4EROR               ;VDAL REG NOT EQUAL TO EXPECTED
11339   031562   104455                          TRAP    C$ERDF
11340   031564   000013                          .WORD   11
11341   031566   003710                          .WORD   VDALRG
11342   031570   006716                          .WORD   T4EROR
11343   031572                          CKLOOP
11344   031572   104406                          TRAP    C$CLP1
11345
11346                                   ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON
11347                                   ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
11348                                   ;BE WRITTEN OR READ.
11349
11350   031574   004537  012234          11$:    JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
11351   031600   000004                          .WORD   MODE                   ;SELECT THE MODE REGISTER
11352
11353                                   ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL
11354                                   ;ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL SELECT 16 BIT ADDRESS MODE
11355
11356   031602   005037  002346                  CLR     T6LOAD                 ;SETUP TO CLEAR ALL MODE REGISTER BITS
11357   031606   004737  011216                  JSR     PC,LDRDT6              ;GO LOAD, READ AND CHECK MODE REGISTER
11358   031612   001405                          BEQ     12$                    ;IF LOADED OK THEN CONTINUE
11359   031614                          ERRDF   12,MODREG,TO6ERR               ;MODE REGISTER NOT EQUAL EXPECTED
11360   031614   104455                          TRAP    C$ERDF
11361   031616   000014                          .WORD   12
11362   031620   004002                          .WORD   MODREG
11363   031622   006732                          .WORD   TO6ERR
11364   031624                          CKLOOP
11365   031624   104406                          TRAP    C$CLP1
11366
11367                                   ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
11368                                   ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
11369                                   ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDALO H
11370                                   ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
11371                                   ;TER WILL BE ADDRESSED.
11372
11373   031626   004537  012234          12$:    JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
11374   031632   000002                          .WORD   FDAL                   ;SELECT EOAI AND FDAL REGISTER
11375
11376                                   ;LOAD, READ AND CHECK THE FDAL AND EOAI REGISTER.  THE EOAI REGISTER
11377                                   ;WILL BE HELD CLEARED BY THE SIGNAL INTER L BEING ASSERTED LOW.  TO
11378                                   ;CHECK THIS, THE PROGRAM WILL ATTEMPT TO LOAD ALL ONES INTO THE EOAI
11379                                   ;REGISTER.  ALL ZEROES SHOULD BE READ BACK FROM THE EOAI REGISTER WHEN
11380                                   ;THE SIGNAL INTER L IS HELD LOW.  THE FDAL REGISTER WILL BE LOADED AND
11381                                   ;CHECKED WITH A DATA PATTERN OF 125.  FDALO H ON A ONE WILL ENABLE THE
11382                                   ;EOAI REGISTER TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD
11383                                   ;OF THE CTL REGISTER.
11384
```

B 2

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46 PAGE 220
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0220

```
11385  031634  012737  000125  002346          MOV     #125,T6LOAD              :SETUP FDAL REGISTER BITS
11386  031642  012777  177525  150342          MOV     #177525,@REG6            :LOAD EOAI AND FDAL REGISTER
11387  031650  004737  011224                  JSR     PC,READT6                :READ AND CHECK EOAI AND FDAL REGISTER
11388  031654  001405                          BEQ     13$                      :IF LOADED OK THEN CONTINUE
11389  031656                                  ERRDF   12,EOAIFD,T06ERR         :INTER L PROBALY DIDN'T CLEAR EOAI REG
11390  031656  104455                          TRAP    C$ERDF
11391  031660  000014                          .WORD   12
11392  031662  004047                          .WORD   EOAIFD
11393  031664  006732                          .WORD   T06ERR
11394  031666                                  CKLOOP
11395  031666  104406                          TRAP    C$CLP1
11396
11397                                          :SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
11398                                          :2:0 TO A 0.   THE DIAGNSOTIC ADDRESS REGISTER WILL BE WRITTEN WITH A DATA
11399                                          :PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.   THE DIAGNOSTIC ADDRESS
11400                                          :REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER BIT 10
11401                                          :BEING SET TO A ONE PREVIOUSLY.   ON A READ COMMAND TO CONTROL REGISTER
11402                                          :6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
11403
11404  031670  004537  012234          13$:    JSR     R5,SELTER                :SELECT REGISTER SPECIFIED BY NEXT WORD
11405  031674  000000                          .WORD   ADDRES                   :SELECT DIAG ADDRESS REG AND ADDRESS BUS
11406
11407                                          :LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA PATTERN
11408                                          :OF 000000.   THIS WILL CAUSE TARGET MEMORY TO BE SELECTED LATER ON IN
11409                                          :THIS TEST.   ADDRESS BITS 17 AND 16 WERE SET TO A ZERO EARLIER IN THIS
11410                                          :TEST VIA THE HDAL REGISTER.
11411
11412  031676  005037  002346                  CLR     T6LOAD                   :SETUP TO LOAD ADDRESS 000000
11413  031702  004737  011216                  JSR     PC,LDRDT6                :LOAD, READ ADN CHECK DIAG ADDRESS REG
11414  031706  001405                          BEQ     14$                      :IF LOADED OK THEN CONTINUE
11415  031710                                  ERRDF   12,ADDRRG,T06ERR         :DIAGNOSTIC ADDRESS REGISTER ERROR
11416  031710  104455                          TRAP    C$ERDF
11417  031712  000014                          .WORD   12
11418  031714  004144                          .WORD   ADDRRG
11419  031716  006732                          .WORD   T06ERR
11420  031720                                  CKLOOP
11421  031720  104406                          TRAP    C$CLP1
11422
11423                                          :READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
11424                                          :CHANGES OCCURED DURING THE PAST SEQUENCES.
11425
11426  031722  004737  011200          14$:    JSR     PC,READT4                :READ AND CHECK VDAL REGISTER
11427  031726  001405                          BEQ     15$                      :IF NO CHANGES THEN CONTINUE
11428  031730                                  ERRDF   11,VDALRG,T4EROR         :VDAL OR PAUSE STATE MACHINE ERROR
11429  031730  104455                          TRAP    C$ERDF
11430  031732  000013                          .WORD   11
11431  031734  003710                          .WORD   VDALRG
11432  031736  006716                          .WORD   T4EROR
11433  031740                                  CKLOOP
11434  031740  104406                          TRAP    C$CLP1
11435
11436                                          :RE-SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.   THE
11437                                          :HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
11438                                          :CONTROL REGISTER 6.
11439
11440  031742  004537  012234          15$:    JSR     R5,SELTER                :SELECT REGISTER SPECIFIED BY NEXT WORD
```

C 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 221
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0221

```
11441   031746  0G0003                              .WORD   HDAL                        ;SELECT THE HDAL REGISTER
11442
11443   031750  012737  001104  002346              MOV     #HDAL9!HDAL6!HDAL2,T6LOAD ;BITS THAT WERE PREVIOUSLY LOADED
11444
11445                                               ;SET THE SIGNALS XRAS H AND PRAS H TO THE HIGH STATES BY SETTING HDAL12 H
11446                                               ;TO A ONE.  WHEN XRAS H IS SET HIGH, THE PAUSE MODE FLIP-FLOP, THE
11447                                               ;EDFET FLIP-FLOP, AND THE BTFET FLIP-FLOP WILL BE CLOCKED TO ONES.
11448                                               ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE AS A
11449                                               ;RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.  SOP H IS ASSERTED
11450                                               ;HIGH WHEN THE SIGNAL PAUSE L IS ASSERTED HIGH (PAUSE MODE).  WHEN
11451                                               ;PRAS H IS SET HIGH, THE ADDRESS BUS, WHICH CONTAINS THE DIAGNOSTIC
11452                                               ;ADDRESS REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY SIMULATORS
11453                                               ;SYSTEM ADDRESS BUS LATCHES.  SELECTING ADDRESS ZERO ON THE MEMORY
11454                                               ;SIMULATOR MODULE WILL CAUSE THE SIGNALS ETR H AND WVIOL L TO BE
11455                                               ;ASSERTED HIGH.
11456
11457   031756  004737  012300              JSR     PC,XRASH                    ;SET XRAS H AND PRAS H TO THE HIGH STATE
11458
11459                                               ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL PSMW H IS ASSERTED
11460                                               ;HIGH AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.
11461
11462   031762  052737  001000  002342              BIS     #VDAL9,T4GOOD               ;EXPECT PSMW H TO BE A ONE
11463   031770  004737  011200              JSR     PC,READT4                   ;READ AND CHECK VDAL REGISTER
11464   031774  001405                      BEQ     16$                         ;IF OK THEN CONTINUE
11465   031776                              ERRDF   11,VDALRG,T4EROR            ;VDAL REGISTER NOT EQUAL EXPECTED
11466   031776  104455                      TRAP    C$ERDF
11467   032000  000013                      .WORD   11
11468   032002  003710                      .WORD   VDALRG
11469   032004  006716                      .WORD   T4EROR
11470   032006                              CKLOOP
11471   032006  104406                      TRAP    C$CLP1
11472
11473                                               ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11474                                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11475
11476   032010  004737  011250      16$:    JSR     PC,SLCTMS
11477
11478                                               ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED AS A RESULT
11479                                               ;OF CLOCKING THE SYSTEM ADDRESS BUS INTO THE MEMORY SIMULATOR SYSTEM
11480                                               ;ADDRESS BUS LATCHES.
11481
11482   032014  004737  010522              JSR     PC,READS0                   ;READD AND CHECK CONTROL REISTER 0
11483   032020  001405                      BEQ     17$                         ;IF OK THEN CONTINUE
11484   032022                              ERRDF   1,,S0EROR                   ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
11485   032022  104455                      TRAP    C$ERDF
11486   032024  000001                      .WORD   1
11487   032026  000000                      .WORD   0
11488   032030  005306                      .WORD   S0EROR
11489   032032                              CKLOOP
11490   032032  104406                      TRAP    C$CLP1
11491
11492                                               ;READ CONTROL REGISTER 4 TO CHECK THAT ADDRESS 0 WAS CLOCKED INTO THE
11493                                               ;SYSTEM ADDRESS BUS LATCHES.  WHEN CTS H IS ASSERTED HIGH, THE SYSTEM
11494                                               ;ADDRESS BUS LATHCES ARE ENABLED TO MSAD BITS 17:0
11495
11496   032034  005037  002254      17$:    CLR     S4LOAD                      ;SETUP TO EXPECT ADDRESS TO BE 0
```

D 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 222
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0222

```
11497  032040  004737  010614           JSR    PC,READS4              ;READ AND CHECK MSAD 15:0
11498  032044  001405                    BEQ    18$                    ;IF OK THEN CONTINUE
11499  032046                            ERRDF  3,MSADRG,SO4ERR        ;MSAD 15:0 SYSTEM ADDRESS BUS LATCH ERROR
11500  032046  104455                    TRAP   C$ERDF
11501  032050  000003                    .WORD  3
11502  032052  002510                    .WORD  MSADRG
11503  032054  005406                    .WORD  SO4ERR
11504  032056                            CKLOOP
11505  032056  104406                    TRAP   C$CLP1
11506
11507                                     ;READ CONTROL REGISTER 2 TO CHECK THAT MSAD BITS 17 AND 16 ARE ZERO AND
11508                                     ;THAT THE SIGNALS ESR H AND MSBRK H ARE ZERO.  THE SIGNAL WREN H SHOULD
11509                                     ;BE ASSERTED HIGH BECAUSE THE MAP PROTECTION RAM WAS SETUP TO ALLOW
11510                                     ;READS AND WRITES TO ADDRESSES 0-376.
11511
11512  032060  052737  000014  002250  18$:  BIS    #MSEL1!MSELO,S2MASK    ;SETUP TO IGNORE TRI-STATED BITS
11513  032066  012737  000010  002244        MOV    #MSEL1,S2LOAD          ;SETUP PREVIOULSY LOADED BIT
11514  032074  012737  000100  002246        MOV    #WRENH,S2GOOD          ;EXPECT WREN H TO BE ASSERTED HIGH
11515  032102  004737  010562                JSR    PC,READS2             ;READ AND CHECK CONTROL REGISTER 2
11516  032106  001405                        BEQ    19$                   ;IF OK THEN CONTINUE
11517  032110                                ERRDF  2,,S2EROR             ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
11518  032110  104455                        TRAP   C$ERDF
11519  032112  000002                        .WORD  2
11520  032114  000000                        .WORD  0
11521  032116  005322                        .WORD  S2EROR
11522  032120                                CKLOOP
11523  032120  104406                        TRAP   C$CLP1
11524
11525                                     ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11526                                     ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11527
11528  032122  004737  012214          19$:  JSR    PC,SLCTTE             ;SELECT THE TARGET EMULATOR MODULE
11529
11530
11531                                     ;SELECT THE EODAL BUS BY SETTING GDDAL BITS 2:0 TO A 7.  ON A READ
11532                                     ;COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ VIA THE
11533                                     ;SIGNAL RPT7 L.
11534
11535  032126  004537  012234                JSR    R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
11536  032132  000007                        .WORD  EODAL                 ;SELECT THE EODAL BUS TO BE READ
11537
11538                                     ;AT THIS POINT IN TIME, FDAL REGISTER BITS 7:2 SHOULD BE ENABLED TO THE
11539                                     ;EODAL BUS VIA THE SIGNAL INTER L.  THE FDAL REGISTER WAS LOADED
11540                                     ;PREVIOUSLY WITH A DATA PATTERN OF 125.  WHEN READ ON THE EODAL BUS,
11541                                     ;BITS 1 AND 0 WILL BE READ AS A ZERO.
11542
11543  032134  012737  000124  002346        MOV    #124,T6LOAD           ;SETUP EXPECTED FDAL DATA TO EODAL BUS
11544  032142  012737  177400  002352        MOV    #177400,T6MASK        ;SETUP TO IGNORE TRI-STATED HIGH BYTE
11545  032150  004737  011224                JSR    PC,READT6             ;READ AND CHECK THE EODAL BUS
11546  032154  001405                        BEQ    20$                   ;IF OK THEN CONTINUE
11547  032156                                ERRDF  12,FDEODL,T6ALLR      ;FDAL REG 7:2 TO EODAL BUS ERROR
11548  032156  104455                        TRAP   C$ERDF
11549  032160  000014                        .WORD  12
11550  032162  004607                        .WORD  FDEODL
11551  032164  006746                        .WORD  T6ALLR
11552  032166                                CKLOOP
```

E 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 223
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0223

```
11553   032166  104406                              TRAP    C$CLP1
11554
11555                                               ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
11556                                               ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
11557                                               ;REGISTER 6.
11558
11559   032170  004537  012234            20$:      JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
11560   032174  000003                              .WORD   HDAL                    ;SELECT THE HDAL REGISTER
11561
11562   032176  012737  011104  002346              MOV     #HDAL12!HDAL9!HDAL6!HDAL2,T6LOAD ;BITS PREVIOUSLY SET
11563   032204  005037  002352                      CLR     T6MASK                  ;CLEAR CONTROL REGISTER 6 MASK WORD
11564
11565                                               ;TO ENABLE THE EODAL BUS TO THE CDAL BUS THE PROGRAM MUST SET THE SIGNAL
11566                                               ;ADAL13 H TO THE HIGH STATE BY SETTING ADAL13 H TO A ONE. WHEN ADAL13 H,
11567                                               ;PSEL0 L, AND PSEL1 H ARE ASSERTED HIGH, THE SIGNALS COHB L AND COLB L
11568                                               ;WILL BE ASSERTED LOW THUS ENABLING THE EODAL BUS TO THE CDAL BUS.
11569                                               ;THE EODAL BUS PRESENTLY CONTAINS DATA FROM FDAL REGISTER BITS 7:2 (124).
11570                                               ;THE CDAL BUS WILL UNCONDITIONALLY BE ENABLED TO THE EIDAL BUS.  THE CDAL
11571                                               ;BUS WILL ALSO BE ENABLED TO THE TDAL BUS BY THE SIGNALS DTHB L AND
11572                                               ;DTLB L BEING ASSERTED LOW.  THESE TWO SIGNALS ARE ASSERTED LOW AS A
11573                                               ;RESULT OF WVIOL L, ETR H, PR/WHB L, PR/WLB L, MR11 L, PBCLR L, AND
11574                                               ;PSEL0 L BEING ASSERTED HIGH.
11575
11576   032210  052777  020000  147770              BIS     #ADAL13,@REG2           ;SET ADAL13 H TO THE HIGH STATE
11577
11578                                               ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ
11579                                               ;COMMAND TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ VIA RPT6 L.
11580
11581   032216  004537  012234                      JSR     R5,SELTER               ;SELECT REG SPECIFIED BY NEXT WORD
11582   032222  000006                              .WORD   EIDAL                   ;SELECT THE EIDAL BUS TO BE READ
11583
11584                                               ;AT THE PRESENT TIME DATA FROM FDAL REGISTER BITS 7:2 (124) ARE ENABLED
11585                                               ;TO THE EODAL BUS, THE CDAL BUS, THE EIDAL BUS AND THE TDAL BUS VIA
11586                                               ;THE SIGNALS INTER L, COHB L, COLB L, DTHB L AND DTLB L .  THE
11587                                               ;FOLLOWING SECTION WILL READ THE EIDAL BUS TO CHECK THAT THE FDAL
11588                                               ;REGISTER DATA IS ENABLED TO IT VIA THE EODAL AND  CDAL BUSSES.
11589
11590   032224  012737  000124  002346              MOV     #124,T6LOAD             ;SETUP EXPECTED FDAL TO EIDAL BUS DATA
11591   032232  012737  177400  002352              MOV     #177400,T6MASK          ;SETUP TI IGNORE TRI-STATED HIGH BYTE
11592   032240  004737  011224                      JSR     PC,READT6               ;READ AND CHECK EIDAL BUS DATA
11593   032244  001405                              BEQ     21$                     ;IF DATA OK THEN CONTINUE
11594   032246                                      ERRDF   12,FDEIDL,T6ALLR        ;FDAL REG 7:2 TO EIDAL BUS ERROR VIA CDAL
11595   032246  104455                              TRAP    C$ERDF
11596   032250  000014                              .WORD   12
11597   032252  004647                              .WORD   FDEIDL
11598   032254  006746                              .WORD   T6ALLR
11599   032256                                      CKLOOP
11600   032256  104406                              TRAP    C$CLP1
11601   032260  042777  020000  147720  21$:        BIC     #ADAL13,@REG2           ;CLEARING ADAL13 H DEASSERTS COLB L
11602
11603                                               ;AT THE PRESENT TIME DATA FROM FDAL REGISTER BITS 7:2 (124) ARE ENABLED
11604                                               ;TO THE EODAL BUS, THE CDAL BUS, THE EIDAL BUS AND THE TDAL BUS VIA THE
11605                                               ;SIGNALS INTER L, COHB L, COLB L, DTHB L, AND DTLB L.  TO CHECK
11606                                               ;THAT FDAL REGISTER BITS 7:2 ARE ENABLED TO THE TDAL BUS, THE
11607                                               ;PROGRAM MUST CLOCK THE DATA INTO THE TDAL DIAGNOSTIC LATCHES FIRST SO
11608                                               ;THAT THE DATA CAN BE READ BACK LATER ON IN THIS TEST.  TO CLOCK THE
```

F 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 224
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0224

```
11609                                                  ;DATA INTO THE TDAL LATCHES, THE PROGRAM MUST SET THE SIGNAL VDAL2 H TO
11610                                                  ;A ONE AND THEN ZERO.  PULSING THE SIGNAL VDAL2 H WILL CAUSE A PULSE ON
11611                                                  ;THE SIGNAL "INVD L" WHICH WILL CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS,
11612                                                  ;THE EDFET AND BTFET FLIP-FLOPS.  WITH THESE FLIP-FLOPS CLEARED, THE
11613                                                  ;FDAL REGISTER DATA WILL BE DISABLED FROM THE CDAL BUS, THE EIDAL BUS AND
11614                                                  ;THE TDAL BUS.  THE SIGNAL FETCT H WILL ALSO BE SET TO A ZERO IN THE
11615                                                  ;FOLLOWING SECTION.
11616
11617  032266  012737  000004  002340        MOV     #VDAL2,T4LOAD           ;SET FETCT H LOW AND SET VDAL2 H HIGH
11618  032274  013737  002340  002342        MOV     T4LOAD,T4GOOD          ;COPY DATA LOADED TO EXPECTED
11619  032302  052737  000040  002342        BIS     #VDAL5,T4GOOD          ;EXPECT BTS1 H TO BE A 1 VIA INTER L
11620  032310  004737  011172                JSR     PC,LDRD4T             ;LOAD, READ AND CHECK VDAL REGISTER
11621  032314  001405                        BEQ     22$                   ;IF LOADED OK THEN CONTINUE
11622  032316                                ERRDF   11,VDALRG,T4EROR      ;VDAL REGISTER NOT EQUAL EXPECTED
11623  032316  104455                        TRAP    C$ERDF
11624  032320  000013                        .WORD   11
11625  032322  003710                        .WORD   VDALRG
11626  032324  006716                        .WORD   T4EROR
11627  032326                                CKLOOP
11628  032326  104406                        TRAP    C$CLP1
11629  032330  042737  000004  002340  22$:  BIC     #VDAL2,T4LOAD         ;SETUP TO SET VDAL2 H LOW
11630  032336  042737  000004  002342        BIC     #VDAL2,T4GOOD         ;SETUP TO EXPECT VDAL2 H TO BE A 0
11631  032344  004737  011172                JSR     PC,LDRD4T            ;LOAD, READ AND CHECK VDAL REGISTER
11632  032350  001405                        BEQ     23$                  ;IF LOADED OK THEN CONTINUE
11633  032352                                ERRDF   11,VDALRG,T4EROR     ;VDAL REGISTER NOT EQUAL EXPECTED
11634  032352  104455                        TRAP    C$ERDF
11635  032354  000013                        .WORD   11
11636  032356  003710                        .WORD   VDALRG
11637  032360  006716                        .WORD   T4EROR
11638  032362                                CKLOOP
11639  032362  104406                        TRAP    C$CLP1
11640
11641                                         ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
11642                                         ;REGISTER WILL 9E WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
11643                                         ;REGISTER 6.
11644
11645  032364  004537  012234         23$:  JSR     R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
11646  032370  000003                        .WORD   HDAL                 ;SELECT THE HDAL REGISTER
11647
11648                                         ;THE FOLLOWING SECTION WILL SET THE SIGNALS XRAS H AND PPI H TO THE
11649                                         ;LOW STATE BY CLEARING HDAL REGISTER BITS 15 AND 12.
11650
11651  032372  012737  111104  002346        MOV     #HDAL15!HDAL12!HDAL9!HDAL6!HDAL2,T6LOAD  ;LOADED BITS
11652  032400  005037  002352                CLR     T6MASK               ;SETUP MASK WORD TO CHECK ALL BITS
11653  032404  004737  012542                JSR     PC,XPIL              ;SET XPI H AND PPI H LOW
11654  032410  004737  012332                JSR     PC,XRASL             ;SET XRAS H AND PRAS H LOW
11655
11656                                         ;SET HDAL REGISTER BITS 4 AND 3 TO A ONE TO SET THE SIGNALS PR/WHB H AND
11657                                         ;PR/WLB H TO THE HIGH STATE.
11658
11659  032414  052737  000030  002346        BIS     #HDAL4!HDAL3,T6LOAD  ;SET PR/WHB H AND PR/WLB H TO HIGH STATE
11660  032422  004737  011216                JSR     PC,LDRDT6            ;LOAD, READ AND CHECK THE HDAL REGISTER
11661  032426  001405                        BEQ     24$                  ;IF LOADED OK THEN CONTINUE
11662  032430                                ERRDF   12,HDALRG,T06ERR     ;HDAL REGISTER NOT EQUAL EXPECTED
11663  032430  104455                        TRAP    C$ERDF
11664  032432  000014                        .WORD   12
```

G 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 225
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0225

```
11665   032434  003756                          .WORD    HDALRG
11666   032436  006732                          .WORD    TO6ERR
11667   032440                          CKLOOP
11668   032440  104406                          TRAP     C$CLP1
11669
11670                                   ;SET THE SIGNAL VDALO H TO A ONE TO ENABLE THE OUTPUTS OF THE TDAL
11671                                   ;DIAGNOSTIC LATCHES ONTO THE TDAL BUS. THE TDAL LATCHES WERE LOADED
11672                                   ;WITH DATA FROM FDAL REGISTER BITS 7:2 (124) EARLIER IN THIS TEST.
11673
11674   032442  052737  000001  002340  24$:    BIS      #VDALO,T4LOAD        ;SETUP BIT TO BE LOADED
11675   032450  052737  000001  002342          BIS      #VDALO,T4GOOD        ;EXPECT VDALO H TO BE SET ON READ
11676   032456  004737  011172                  JSR      PC,LDRD4T            ;LOAD, READ AND CHECK VDAL REGISTER
11677   032462  001405                          BEQ      25$                  ;IF LOADED OK THEN CONTINUE
11678   032464                                  ERRDF    11,VDALRG,T4EROR     ;VDAL REGISTER NOT EQUAL EXPECTED
11679   032464  104455                          TRAP     C$ERDF
11680   032466  000013                          .WORD    11
11681   032470  003710                          .WORD    VDALRG
11682   032472  006716                          .WORD    T4EROR
11683   032474                          CKLOOP
11684   032474  104406                          TRAP     C$CLP1
11685
11686                                   ;THE FOLLOWING SIGNALS ETR H, MR11 L, PR/WHB H, PR/WLB H, AND PSMW L
11687                                   ;SHOULD BE ASSERTED HIGH.  THERFORE, BY SETTING PPI H TO THE HIGH
11688                                   ;STATE, THE SIGNALS DBHB L AND DBLB L SHOULD BE ASSERTED LOW.  THESE
11689                                   ;TWO SIGNALS WILL ENABLE THE TDAL BUS, WHICH HAS THE TDAL DIAGNOSTIC
11690                                   ;LATCHES ENABLED TO IT, TO THE CDAL BUS AND THE CDAL BUS WILL BE ENABLED
11691                                   ;TO THE EIDAL BUS UNCONDTIONALLY.  THE TDAL LATCHES WERE LOADED EARLIER
11692                                   ;IN THIS TEST WITH DATA FROM FDAL REGISTER BITS 7:2 (124).
11693
11694   032476  004737  012510          25$:    JSR      PC,XPIH              ;SET XPI H AND PPI H TO HIGH STATE
11695
11696                                   ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ
11697                                   ;COMMAND TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ VIA THE
11698                                   ;SIGNAL RPT6 L.
11699
11700   032502  004537  012234                  JSR      R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
11701   032506  000006                          .WORD    EIDAL                ;SELECT THE EIDAL BUS TO BE READ
11702
11703                                   ;AT THE PRESENT TIME THE TDAL DIAGNOSTIC LATCHES ARE ENABLED TO THE
11704                                   ;TDAL BUS, THE CDAL BUS AND THE EIDAL BUS VIA THE SIGHALS VDALO H,
11705                                   ;DBHB L ABD DBLB L.  THE TDAL LATCHES WERE LOADED EARLIER IN THE TEST
11706                                   ;WITH DATA FROM FDAL REGISTER BITS 7:2 (124).  THE PROGRAM WILL
11707                                   ;NOW READ THE EIDAL BUS TO CHECK THAT FDAL REGISTER BITS 7:2 DATA
11708                                   ;(124) WAS LOADED INTO THE TDAL LATCHES AND THAT THE TDAL LATCHES
11709                                   ;ARE ENABLED TO THE EIDAL BUS.
11710
11711   032510  012737  000124  002346          MOV      #124,T6LOAD          ;SETUP EXPECTED FDAL TO EIDAL BUS DATA
11712   032516  012737  177400  002352          MOV      #177400,T6MASK       ;SETUP TO IGNORE TRI-STATED HIGH BYTE
11713   032524  004737  011224                  JSR      PC,READT6            ;READ AND CHECK THE EIDAL BUS
11714   032530  001405                          BEQ      26$                  ;IF DATA OK THEN CONTINUE
11715   032532                                  ERRDF    12,FDTDEI,T6ALLR     ;FDAL TO TDAL LATCHES TO EIDAL BUS ERROR
11716   032532  104455                          TRAP     C$ERDF
11717   032534  000014                          .WORD    12
11718   032536  004707                          .WORD    FDTDEI
11719   032540  006746                          .WORD    T6ALLR
11720   032542                          CKLOOP
```

H 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 226
CVCDDB.P11   14-JUN-82 09:54   TEST 11: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 16 BIT MODE   SEQ 0226

```
11721   032542  104406                              TRAP    C$CLP1
11722
11723                                       ;SELECT THE HDAL REGISER BY SETTING DGAL BITS 2:0 TO A 3.  THE HDAL
11724                                       ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
11725                                       ;CONTROL REGISTER 6.
11726
11727   032544  004537  012234      26$:    JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
11728   032550  000003                      .WORD   HDAL                    ;SELECT THE HDAL REGISTER
11729
11730   032552  012737  101034  002346      MOV     #HDAL15!HDAL9!HDAL4!HDAL3!HDAL2,T6LOAD ;BIT LOADED BEFORE - HDAL6 H
11731   032560  005037  002352              CLR     T6MASK                  ;SETUP MASK TO CHECK ALL BITS
11732
11733                                       ;SET THE SIGNALS XPI H AND PPI H TO THE LOW STATE BY CLEARING HDAL
11734                                       ;REGISTER BIT 15.  ALOS SET THE SIGNAL PSEL1 L TO THE HIGH STATE BY
11735                                       ;SETTING HDAL REGISTER BIT 6 TO A 0.
11736
11737   032564  004737  012542              JSR     PC,XPIL                 ;SET XPI H AND PPI H TO LOW STATE
11738
11739                                       ;ISSUE A PULSE ON THE SIGNAL "INVD L" TO RE-INITIALIZE THE MODULE.
11740
11741   032570  005037  002340              CLR     T4LOAD                  ;SETUP TO CLEAR ALL BITS
11742   032574  004737  012706              JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
11743
11744   032600                              ENDSEG
11745   032600                      10002$:
11746   032600  104405                      TRAP    C$ESEG
11747
11748   032602                              ENDTST
11749   032602                      L10047:
11750   032602  104401                      TRAP    C$ETST
11751
```

I 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 227
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0227

```
11752                                   .SBTTL  TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE
11753
11754                           ;++
11755                           ;       THIS TEST WILL CHECK THAT TARGET EMULATOR FDAL REGISTER BITS 7:2 CAN
11756                           ;       BE CLOCKED INTO THE TDAL DIAGNOSTIC LATCHES IN 8 BIT MODE WHEN THE
11757                           ;       TARGET EMULATOR MODULE IS ADDRESSING A LOCATION WHICH IS MAPPED ON THE
11758                           ;       MEMORY SIMULATOR MODULE TO ALLOW READS AND WRITES TO THE TARGET RAM.
11759                           ;       TO CHECK THAT THE TDAL LATCHES WERE CLOCKED WITH FDAL REGISTER DATA,
11760                           ;       THE PROGRAM WILL ENABLE THE TDAL LATCHES TO THE EIDAL BUS WITH THE
11761                           ;       TARGET RAM STILL BEING ADDRESSED.  THE PROGRAM WILL THEN READ AND CHECK
11762                           ;       THE EIDAL BUS TO CONTAIN THE CORRECT FDAL REGISTER DATA.
11763                           ;--
11764
11765    032604                         BGNTST
11766    032604                  T12::
11767
11768    032604  004737  007440         JSR     PC,INITMD                   ;INITIALIZE MDE/T-11 SYSTEM MODULES
11769
11770    032610                         BGNSEG
11771    032610  104404                 TRAP    C$BSEG
11772
11773                           ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11774                           ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11775
11776    032612  004737  011250         JSR     PC,SLCTMS                   ;SELECT THE MEMORY SIMULATOR MODULE
11777
11778                           ;TOGGLE THE SIGNAL RST H IN CONTROL REGISTER 0 AND SET THE SIGNAL MP H
11779                           ;TO A ONE.  A PULSE ON THE SIGNAL RST H WILL PRESET THE WRV AND RDV
11780                           ;FLIP-FLOPS THUS CAUSING THE SIGNAL BRK L TO BE ASSERTED HIGH.  SETTING
11781                           ;THE SIGNAL MP H TO A ONE WILL ENABLE MAP PROTECTION BITS MPIN H,
11782                           ;WRE H AND RDE H TO THE SYSTEM BUS ALONG WITH THE SIGNAL BRK L.  THESE
11783                           ;SIGNALS WILL BE ENABLED TO THE SYSTEM BUS AS ETR H, WVIOL H, MSBRK H
11784                           ;AND RDE L.  SETTING THE SIGNAL MP H WILL ALSO ENABLE THE SIGNALS MPIN H
11785                           ;WRE H, AND BRK L TO CONTROL REGISTER 2 AS SIGNALS ESR H, WREN H AND
11786                           ;MSBRK H RESPECTIVELY.
11787
11788    032616  112737  000005  002234 MOVB    #RSTH!MPH,SOLOAD            ;SETUP BITS TO BE LOADED
11789    032624  004737  011270         JSR     PC,MSRSTH                   ;PULSE RST H AND SET MP H TO A ONE
11790
11791                           ;THE FOLLOWING SECTION WILL LOAD, READ AND CHECK THE MEMORY SIMULATOR
11792                           ;MAP PROTECTION RAM.  THE MAP PROTECTION RAM WILL BE SETUP TO ALLOW
11793                           ;READS AND WRITES TO THE FIRST 128 WORDS OF MEMORY.  THE FIRST 128
11794                           ;WORDS OF MEMORY WILL BE MAPPED TO SELECT THE TARGET MEMORY.  THE
11795                           ;REMAINING LOCATIONS OF THE MAP PROTECTION RAM WILL BE MAPPED TO THE
11796                           ;MEMORY SIMULATOR RAM AND SETUP TO INHIBIT READS AND WRITES TO THOSE
11797                           ;LOCATIONS (777776-000400).
11798
11799    032630  005037  002254         CLR     S4LOAD                      ;SETUP STARTING MSAD 15:0 BITS
11800    032634  012737  000010  002244 MOV     #MSEL1,S2LOAD               ;SETUP STARTING MSAD 17:16 BITS AND
11801                                                                       ;BITS TO SELECT MAP PROTECTION RAM
11802
11803    032642                  1$:    BGNSEG
11804    032642  104404                 TRAP    C$BSEG
11805
11806                           ;SET THE SIGNAL MSEL1 H TO A ONE AND MSEL0 H TO A ZERO.  THIS WILL
11807                           ;CAUSE THE MAP PROTECTION RAM TO BE SELECTED VIA THE SIGNAL SMPM H
```

J 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 228
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0228

```
11808                                                    ;WHEN A READ OR WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6.  MSAD
11809                                                    ;BITS 17 AND 16 IN CONTROL REGISTER 2 WILL BE LOADED AND CHECKED FOR
11810                                                    ;THE ADDRESS BEING TESTED.
11811
11812   032644  012737  177540  002250         MOV     #177540,S2MASK          ;SETUP TO IGNORE ESR H + WREN H
11813   032652  004737  010546                 JSR     PC,LDRDS2               ;LOAD, READ AND CHECK CONTROL REG 2
11814   032656  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
11815   032660                                  ERRDF   2,,S2EROR               ;CONTROL REG 2 NOT EQUAL EXPECTED
11816   032660  104455                          TRAP    C$ERDF
11817   032662  000002                          .WORD   2
11818   032664  000000                          .WORD   0
11819   032666  005322                          .WORD   S2EROR
11820   032670                                  CKLOOP
11821   032670  104406                          TRAP    C$CLP1
11822
11823                                                    ;LOAD, READ AND CHECK CONTROL REGISTER 4 FOR THE ADDRESS BEING TESTED.
11824                                                    ;CONTROL REGISTER 4 CONTAINS BITS FOR MSAD ADDRESS BITS 15:0.
11825
11826   032672  004737  010606         2$:      JSR     PC,LDRDS4               ;LOAD, READ AND CHECK CONTROL REG 4
11827   032676  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
11828   032700                                  ERRDF   3,MSADRG,S4EROR         ;MSAD BITS 15:0 NOT EQUAL EXPECTED
11829   032700  104455                          TRAP    C$ERDF
11830   032702  000003                          .WORD   3
11831   032704  002510                          .WORD   MSADRG
11832   032706  005336                          .WORD   S4EROR
11833   032710                                  CKLOOP
11834   032710  104406                          TRAP    C$CLP1
11835
11836                                                    ;LOAD, READ ADN CHECK MAP PROTECTION RAM LOCATION ADDRESSED BY MSAD
11837                                                    ;BITS 17:0.   ADDRESSES 0 TO 376 WILL BE LOADED AND CHECKED WITH A
11838                                                    ;DATA PATTERN OF 16.  ALL OTHER ADDRESSES WILL BE LOADED AND CHECKED
11839                                                    ;WITH A DATA PATTERN OF 11.
11840
11841   032712  012737  177760  002264  3$:     MOV     #177760,S6MASK          ;SETUP TO IGNORE UNUSED BITS
11842   032720  012737  000011  002260          MOV     #MUTB!MPINH,S6LOAD      ;SETUP FOR ADDRESSES OVER 376
11843   032726  032737  000003  002244          BIT     #MSAD17!MSAD16,S2LOAD   ;CHECK IF ADDRESS ABOVE 16K WORDS
11844   032734  001006                          BNE     4$                      ;IF YES - LOAD R/W VIOLATION SETUP
11845   032736  005737  002254                  TST     S4LOAD                  ;CHECK IF ADDRESS WAS OVER 376
11846   032742  001003                          BNE     4$                      ;IF YES - LOAD R/W VIOLATION SETUP
11847   032744  012737  000016  002260          MOV     #MUTB!RDEH!WREH,S6LOAD  ;SETUP TO ALLOW R/W TO FIRST 128 WORDS
11848   032752  004737  010632         4$:      JSR     PC,LDRDS6               ;LOAD, READ AND CHECK MAP PROTECT RAM
11849   032756  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
11850   032760                                  ERRDF   4,MSGMP,S6ALLR          ;MAP PROTECT RAM DATA ERROR
11851   032760  104455                          TRAP    C$ERDF
11852   032762  000004                          .WORD   4
11853   032764  002603                          .WORD   MSGMP
11854   032766  005456                          .WORD   S6ALLR
11855   032770                                  CKLOOP
11856   032770  104406                          TRAP    C$CLP1
11857
11858                                                    ;CHECK MAP PROTECTION RAM DATA BITS MPIN H AND WRE H IN CONTROL
11859                                                    ;REGISTER 2 AS ESR H AND WREN H RESPECTIVELY.
11860
11861   032772  042737  000140  002250  5$:     BIC     #ESRH!WRENH,S2MASK      ;SETUP TO CHECK ESR H AND WREN H
11862   033000  052737  000100  002246          BIS     #WRENH,S2GOOD           ;EXPECT WREN H TO BE A ONE
11863   033006  032737  000006  002260          BIT     #WREH!RDEH,S6LOAD       ;CHECK IF RAM WAS W/R ENABLED
```

K 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 229
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0229

```
11864  033014  001006                        BNE    6$                       ;IF YES THEN GO READ CONTROL REG 2
11865  033016  042737  000100  002246        BIC    #WRENH,S2GOOD            ;THIS ADDRESS WAS NOT WRITE ENABLED
11866  033024  052737  000040  002246        BIS    #ESRH,S2GOOD             ;EXPECT ESR H TO BE SET TO A ONE
11867  033032  004737  010562         6$:    JSR    PC,READS2                ;GO READ AND CHECK CONTROL REG 2
11868  033036  001404                        BEQ    7$                       ;IF OK THEN CONTINUE
11869  033040                                ERRDF  2,MSGMPL,S2ALLR          ;REGISTER 2 NOT EQUAL EXPECTED
11870  033040  104455                        TRAP   C$ERDF
11871  033042  000002                        .WORD  2
11872  033044  002460                        .WORD  MSGMPL
11873  033046  005442                        .WORD  S2ALLR
11874  033050                         7$:    ENDSEG
11875  033050                      10001$:
11876  033050  104405                        TRAP   C$ESEG
11877
11878                                         ;UPDATE CONTROL REGISTERS 4 AND 2 FOR MSAD ADDRESS TO BE TESTED
11879
11880  033052  062737  000400  002254        ADD    #MSAD8,S4LOAD            ;UPDATE MSAD BITS 15:8 BY ONE
11881  033060  001270                        BNE    1$                       ;IF NOT 0 THEN LOAD NEXT RAM LOCATION
11882  033062  005237  002244                INC    S2LOAD                   ;UPDATE MSAD BITS 17:16 BY ONE
11883  033066  032737  000004  002244        BIT    #MSEL0,S2LOAD            ;CHECK IF ALL RAM LOCATIONS DONE
11884  033074  001662                        BEQ    1$                       ;IF NOT THEN LOAD NEXT RAM LOCATION
11885  033076  005337  002244                DEC    S2LOAD                   ;RESET REG 2 TO ACTUAL VALUE LOADED
11886
11887                                         ;SET THE SIGNAL CTS H TO A ONE IN CONTROL REGISTER 0.  WHEN CTS H IS
11888                                         ;SET TO A ONE,  THE SYSTEM BUS LATCHES WILL BE ENABLED TO THE MEMORY
11889                                         ;SIMULATOR MODULE.
11890
11891  033102  052737  000002  002234        BIS    #CTSH,S0LOAD             ;SETUP BIT TO SET CTS H TO A ONE
11892  033110  004737  010506                JSR    PC,LDRDS0                ;GO LOAD, READ AND CHECK REG 0
11893  033114  001404                        BEQ    8$                       ;IF LOADED OK THEN CONTINUE
11894  033116                                ERRDF  1,,S0EROR                ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
11895  033116  104455                        TRAP   C$ERDF
11896  033120  000001                        .WORD  1
11897  033122  000000                        .WORD  0
11898  033124  005306                        .WORD  S0EROR
11899  033126                         8$:    ENDSEG
11900  033126                      10000$:
11901  033126  104405                        TRAP   C$ESEG
11902
11903  033130                                BGNSEG
11904  033130  104404                        TRAP   C$BSEG
11905
11906                                         ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
11907                                         ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
11908
11909  033132  004737  012214                JSR    PC,SLCTTE                ;SELECT THE TARGET EMULATOR MODULE
11910
11911  033136  005037  002352                CLR    T6MASK                   ;RESET CONTROL REGISTER 6 MASK WORD
11912
11913                                         ;SET ADAL REGISTER BITS 14,10 AND 9 TO A ONE AND PULSE THE SIGNAL ''BRKRES L''
11914                                         ;BY TOGGLING ADAL REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL
11915                                         ;ENABLE THE TARGET EMULATOR MODULE SIGNALS TO THE SYSTEM BUS.  PULSING
11916                                         ;THE SIGNAL ''BRKRES L'' VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE
11917                                         ;TARGET EMULATOR MODULE.  ADAL REGISTER BIT 14 ON A ONE AND ADAL REGISTER
11918                                         ;BIT 15 ON A ZERO WILL CAUSE THE SIGNAL ''CKAI H'' TO BE PULSED VIA THE
11919                                         ;THE SIGNAL ''RASP L'' LATER ON IN THIS TEST.  ADAL REGISTER BIT 4 ON A
```

L 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 230
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0230

```
11920                                                  ;ZERO WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE PAUSE MODE WHEN
11921                                                  ;THE SIGNAL XRAS H IS SET HIGH LATER ON IN THIS TEST.
11922
11923   033142  012737  043000  002334        MOV     #ADAL14!ADAL10!ADAL9,T2LOAD ;SETUP BITS TO BE LOADED
11924   033150  004737  012766                JSR     PC,BRKRES                   ;SET BITS 14, 10 + 9 AND TOGGLE ADAL0 H
11925
11926                                                  ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
11927                                                  ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
11928                                                  ;REGISTER 6.
11929
11930   033154  004537  012234                JSR     R5,SELTER                   ;SELECT REGISTER SPECIFIED BY NEXT WORD
11931   033160  000003                        .WORD   HDAL                        ;SELECT THE HDAL REGISTER
11932
11933                                                  ;SET HDAL REGISTER BITS 9, 6, 4 AND 2 TO A ONE AND HDAL BITS 14, 11, 5
11934                                                  ;AND 3 TO A ZERO.  HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO CONTROL
11935                                                  ;THE T-11 TIMING AND CONTROL SIGNALS.  HDAL9 H ON A ONE WILL ENABLE THE
11936                                                  ;OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER TO THE SYSTEM ADDRESS BUS.
11937                                                  ;HDAL14 H AND HDAL11 H ON A ZERO WILL SET SYSTEM ADDRESS BITS 17 AND 16
11938                                                  ;TO A ZERO.  HDAL4 H ON A ONE AND HDAL3 H ON A ZERO WILL SET PR/WHB L
11939                                                  ;LOW AND PR/WLB L HIGH.  PR/WLB L ASSERTED HIGH WILL CAUSE THE SIGNAL
11940                                                  ;DTLB L TO BE ASSERTED LOW LATER ON IN THE TEST WHEN SOME OTHER GATING
11941                                                  ;SIGNALS ARE ASSERTED HIGH.  DTHB L WILL ALSO BE ASSERTED LOW AS A RESULT
11942                                                  ;OF DMG L, PBCLR L, AND MR11 H BEING ASSERTED HIGH.  THE SIGNALS DTLB L AND
11943                                                  ;DTHB L ASSERTED LOW WILL ENABLE THE CDAL BUS TO THE TDAL BUS.  HDAL5 H ON A
11944                                                  ;ZERO AND HDAL6 H ON A ONE WILL CAUSE THE SIGNAL PSEL0 L TO BE ASSERTED
11945                                                  ;HIGH AND PSEL1 L TO BE ASSERTED LOW.  PSEL1 L SET LOW WILL DISABLE ONE
11946                                                  ;OF THE DATA PATHS TO THE TDAL BUS.  WITH PSEL0 L SET HIGH AND PSEL1 L
11947                                                  ;SET LOW, THE SIGNAL INTER L WILL BE ASSERTED LOW THUS ENABLING FDAL
11948                                                  ;REGISTER BITS 7:2 TO THE EODAL BUS AND CLEARING THE EOAI REGISTER.
11949
11950   033162  012737  001124  002346        MOV     #HDAL9!HDAL6!HDAL4!HDAL2,T6LOAD ;SET HDAL BITS 9, 6, 4 AND 2 TO 1'S
11951   033170  004737  011216                JSR     PC,LDRDT6                   ;GO LOAD, READ AND CHECK HDAL REGISTER
11952   033174  001405                        BEQ     9$                          ;IF LOADED OK THEN CONTINUE
11953   033176                                ERRDF   12,HDALRG,TO6ERR            ;HDAL REGISTER NOT EQUAL EXPECTED
11954   033176  104455                        TRAP    C$ERDF
11955   033200  000014                        .WORD   12
11956   033202  003756                        .WORD   HDALRG
11957   033204  006732                        .WORD   TO6ERR
11958   033206                                CKLOOP
11959   033206  104406                        TRAP    C$CLP1
11960
11961                                                  ;PULSE THE SIGNAL "INVD L" BY SETTING AND CLEARING VDAL2 H IN CONTROL
11962                                                  ;REGISTER 4.  PULSING THE SIGNAL "INVD L" WILL INITIALIZE ALL THE
11963                                                  ;FLIP-FLOPS ON THE MODULE NOT CLEARED BY THE SIGNAL 'BRKRES L'.  SET
11964                                                  ;THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
11965                                                  ;ON A READ COMMAND TO CONTROL REGISTER 4, THE SIGNAL BTS1 H WILL BE SET
11966                                                  ;TO A ONE AS A RESULT OF THE SIGNAL INTER L BEING ASSERTED LOW.  THE
11967                                                  ;SIGNAL INTER L IS ASSERTED LOW AS A RESULT OF PSEL0 L BEING ASSERTED
11968                                                  ;HIGH AND PSEL1 L BEING ASSERTED LOW.
11969
11970   033210  012737  000204  002340  9$:   MOV     #VDAL7!VDAL2,T4LOAD         ;SETUP BITS TO BE LOADED
11971   033216  013737  002340  002342        MOV     T4LOAD,T4GOOD               ;COPY LOADED TO EXPECTED
11972   033224  052737  000040  002342        BIS     #VDAL5,T4GOOD               ;EXPECT BTS1 H TO BE A ONE
11973   033232  004737  011172                JSR     PC,LDRD4T                   ;GO LOAD, READ AND CHECK VDAL REG
11974   033236  001405                        BEQ     10$                         ;IF OK THEN CONTINUE
11975   033240                                ERRDF   11,VDALRG,T4EROR            ;VDAL REG NOT EQUAL TO EXPECTED
```

M 2

HARDWARE TESTS   MACY11 30A(1052)   16-JUN-82 13:46 PAGE 231
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0231

```
11976  033240  104455                          TRAP    C$ERDF
11977  033242  000013                          .WORD   11
11978  033244  003710                          .WORD   VDALRG
11979  033246  006716                          .WORD   T4EROR
11980  033250                          CKLOOP
11981  033250  104406                          TRAP    C$CLP1
11982  033252  042737  000004  002340  10$:    BIC     #VDAL2,T4LOAD         ;SET VDAL2 H TO THE LOW STATE
11983  033260  042737  000004  002342          BIC     #VDAL2,T4GOOD        ;SETUP TO EXPECT IT TO BE ZERO
11984  033266  004737  011172                  JSR     PC,LDRD4T            ;GO LOAD, READ AND CHECK VDAL REG
11985  033272  001405                          BEQ     11$                  ;IF OK THEN CONTINUE
11986  033274                                  ERRDF   11,VDALRG,T4EROR     ;VDAL REG NOT EQUAL TO EXPECTED
11987  033274  104455                          TRAP    C$ERDF
11988  033276  000013                          .WORD   11
11989  033300  003710                          .WORD   VDALRG
11990  033302  006716                          .WORD   T4EROR
11991  033304                          CKLOOP
11992  033304  104406                          TRAP    C$CLP1
11993
11994                                  ;SELECT MODE REGISTER BY SETTING GDAL REGISTER BITS 2:0 TO A 4.  ON
11995                                  ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE MODE REGISTER WILL
11996                                  ;BE WRITTEN OR READ.
11997
11998  033306  004537  012234          11$:    JSR     R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
11999  033312  000004                          .WORD   MODE                 ;SELECT THE MODE REGISTER
12000
12001                                  ;LOAD, READ AND CHECK THE MODE REGISTER WITH MR11 H SET TO A ONE AND
12002                                  ;ALL OTHER MODE REGISTER BITS SET TO A ZERO.  MODE REGISTER BIT 11 SET
12003                                  ;TO A ONE WILL SET THE TARGET EMULATOR MODULE TO 8 BIT MODE.
12004
12005  033314  012737  004000  002346          MOV     #MR11,T6LOAD         ;SETUP BIT TO SET MR11 H TO HIGH STATE
12006  033322  004737  011216                  JSR     PC,LDRDT6            ;GO LOAD, READ AND CHECK MODE REGISTER
12007  033326  001405                          BEQ     12$                  ;IF LOADED OK THEN CONTINUE
12008  033330                                  ERRDF   12,MODREG,T06ERR     ;MODE REGISTER NOT EQUAL EXPECTED
12009  033330  104455                          TRAP    C$ERDF
12010  033332  000014                          .WORD   12
12011  033334  004002                          .WORD   MODREG
12012  033336  006732                          .WORD   T06ERR
12013  033340                          CKLOOP
12014  033340  104406                          TRAP    C$CLP1
12015
12016                                  ;SELECT THE EOAI AND FDAL REGISTER BY SETTING GDAL REGISTER BITS 2:0
12017                                  ;TO A 2.  THE EOAI AND FDAL REGISTER WILL BE ADDRESSED ON A WRITE OR
12018                                  ;READ COMMAND TO CONTROL REGISTER 6.. THE EOAI REGISTER NEEDS FDAL0 H
12019                                  ;TO BE SET TO A ONE IN ORDER TO BE ADDRESSED, OTHERWISE, THE CTL REGIS-
12020                                  ;TER WILL BE ADDRESSED.
12021
12022  033342  004537  012234          12$:    JSR     R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
12023  033346  000002                          .WORD   FDAL                 ;SELECT EOAI AND FDAL REGISTER
12024
12025                                  ;LOAD, READ AND CHECK THE FDAL AND EOAI REGISTER.  THE EOAI REGISTER
12026                                  ;WILL BE HELD CLEARED BY THE SIGNAL INTER L BEING ASSERTED LOW.  TO
12027                                  ;CHECK THIS, THE PROGRAM WILL ATTEMPT TO LOAD ALL ONES INTO THE EOAI
12028                                  ;REGISTER.  ALL ZEROES SHOULD BE READ BACK FROM THE EOAI REGISTER WHEN
12029                                  ;THE SIGNAL INTER L IS HELD LOW.  THE FDAL REGISTER WILL BE LOADED AND
12030                                  ;CHECKED WITH A DATA PATTERN OF 251.  FDAL0 H ON A ONE WILL ENABLE THE
12031                                  ;EOAI REGISTER TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD
```

N 2

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 232
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0232

```
12032                                                    ;OF THE CTL REGISTER.
12033
12034   033350  012737  000251  002346         MOV     #251,T6LOAD            ;SETUP FDAL REGISTER BITS
12035   033356  012777  177651  146626         MOV     #177651,@REG6          ;LOAD EOAI AND FDAL REGISTER
12036   033364  004737  011224                 JSR     PC,READT6              ;READ AND CHECK EOAI AND FDAL REGISTER
12037   033370  001405                          BEQ     13$                    ;IF LOADED OK THEN CONTINUE
12038   033372                                  ERRDF   12,EOAIFD,T06ERR       ;INTER L PROBALY DIDN'T CLEAR EOAI REG
12039   033372  104455                          TRAP    C$ERDF
12040   033374  000014                          .WORD   12
12041   033376  004047                          .WORD   EOAIFD
12042   033400  006732                          .WORD   T06ERR
12043   033402                                  CKLOOP
12044   033402  104406                          TRAP    C$CLP1
12045
12046                                                    ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL REGISTER BITS
12047                                                    ;2:0 TO A 0.  THE DIAGNSOTIC ADDRESS REGISTER WILL BE WRITTEN WITH A DATA
12048                                                    ;PATTERN ON A WRITE COMMAND TO CONTROL REGISTER 6.  THE DIAGNOSTIC ADDRESS
12049                                                    ;REGISTER WILL BE ENABLED TO THE ADDRESS BUS BY HDAL REGISTER BIT 10
12050                                                    ;BEING SET TO A ONE PREVIOUSLY.  ON A READ COMMAND TO CONTROL REGISTER
12051                                                    ;6, THE ADDRESS BUS BITS 15:0 WILL BE READBACK TO THE LSI-11.
12052
12053   033404  004537  012234          13$:    JSR     R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
12054   033410  000000                          .WORD   ADDRES                ;SELECT DIAG ADDRESS REG AND ADDRESS BUS
12055
12056                                                    ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA PATTERN
12057                                                    ;OF 000000.  THIS WILL CAUSE TARGET MEMORY TO BE SELECTED LATER ON IN
12058                                                    ;THIS TEST.  ADDRESS BITS 17 AND 16 WERE SET TO A ZERO EARLIER IN THIS
12059                                                    ;TEST VIA THE HDAL REGISTER.
12060
12061   033412  005037  002346                 CLR     T6LOAD                 ;SETUP TO LOAD ADDRESS 000000
12062   033416  004737  011216                 JSR     PC,LDRDT6             ;LOAD, READ ADN CHECK DIAG ADDRESS REG
12063   033422  001405                          BEQ     14$                    ;IF LOADED OK THEN CONTINUE
12064   033424                                  ERRDF   12,ADDRRG,T06ERR       ;DIAGNOSTIC ADDRESS REGISTER ERROR
12065   033424  104455                          TRAP    C$ERDF
12066   033426  000014                          .WORD   12
12067   033430  004144                          .WORD   ADDRRG
12068   033432  006732                          .WORD   T06ERR
12069   033434                                  CKLOOP
12070   033434  104406                          TRAP    C$CLP1
12071
12072                                                    ;READ AND CHECK CONTROL REGISTER 4 (VDAL REGISTER) TO CHECK THAT NO
12073                                                    ;CHANGES OCCURED DURING THE PAST SEQUENCES.
12074
12075   033436  004737  011200          14$:    JSR     PC,READT4             ;READ AND CHECK VDAL REGISTER
12076   033442  001405                          BEQ     15$                    ;IF NO CHANGES THEN CONTINUE
12077   033444                                  ERRDF   11,VDALRG,T4EROR       ;VDAL OR PAUSE STATE MACHINE ERROR
12078   033444  104455                          TRAP    C$ERDF
12079   033446  000013                          .WORD   11
12080   033450  003710                          .WORD   VDALRG
12081   033452  006716                          .WORD   T4EROR
12082   033454                                  CKLOOP
12083   033454  104406                          TRAP    C$CLP1
12084
12085                                                    ;RE-SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE
12086                                                    ;HDAL REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
12087                                                    ;CONTROL REGISTER 6.
```

B 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 233
CVCD 9.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0233

```
12088
12089  033456  004537  012234        15$:    JSR     R5,SELTER            ;SELECT REGISTER SPECIFIED BY NEXT WORD
12090  033462  000003                         .WORD   HDAL                 ;SELECT THE HDAL REGISTER
12091
12092  033464  012737  001124  002346         MOV     #HDAL9!HDAL6!HDAL4!HDAL2,T6LOAD ;BITS THAT WERE PREVIOUSLY LOADED
12093
12094                                          ;SET THE SIGNALS XRAS H AND PRAS H TO THE HIGH STATES BY SETTING HDAL12 H
12095                                          ;TO A ONE.  WHEN XRAS H IS SET HIGH, THE PAUSE MODE FLIP-FLOP, THE
12096                                          ;EDFET FLIP-FLOP, AND THE BTFET FLIP-FLOP WILL BE CLOCKED TO ONES.
12097                                          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE AS A
12098                                          ;RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.  SOP H IS ASSERTED
12099                                          ;HIGH WHEN THE SIGNAL PAUSE L IS ASSERTED HIGH (PAUSE MODE).  WHEN
12100                                          ;PRAS H IS SET HIGH, THE ADDRESS BUS, WHICH CONTAINS THE DIAGNOSTIC
12101                                          ;ADDRESS REGISTER DATA, WILL BE CLOCKED INTO THE MEMORY SIMULATORS
12102                                          ;SYSTEM ADDRESS BUS LATCHES.  SELECTING ADDRESS ZERO ON THE MEMORY
12103                                          ;SIMULATOR MODULE WILL CAUSE THE SIGNALS ETR H AND WVIOL L TO BE
12104                                          ;ASSERTED HIGH.
12105
12106  033472  004737  012300                 JSR     PC,XRASH             ;SET XRAS H AND PRAS H TO THE HIGH STATE
12107
12108                                          ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL PSMW H IS ASSERTED
12109                                          ;HIGH AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.
12110
12111  033476  052737  001000  002342         BIS     #VDAL9,T4GOOD        ;EXPECT PSMW H TO BE A ONE
12112  033504  004737  011200                 JSR     PC,READT4            ;READ AND CHECK VDAL REGISTER
12113  033510  001405                         BEQ     16$                  ;IF OK THEN CONTINUE
12114  033512  001405                         ERRDF   11,VDALRG,T4EROR     ;VDAL REGISTER NOT EQUAL EXPECTED
12115  033512  104455                         TRAP    C$ERDF
12116  033514  000013                         .WORD   11
12117  033516  003710                         .WORD   VDALRG
12118  033520  006716                         .WORD   T4EROR
12119  033522                                 CKLOOP
12120  033522  104406                         TRAP    C$CLP1
12121
12122                                          ;SELECT THE MEMORY SIMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
12123                                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
12124
12125  033524  004737  011250        16$:    JSR     PC,SLCTMS
12126
12127                                          ;READ CONTROL REGISTER 0 TO CHECK THAT NO CHANGES OCCURED AS A RESULT
12128                                          ;OF CLOCKING THE SYSTEM ADDRESS BUS INTO THE MEMORY SIMULATOR SYSTEM
12129                                          ;ADDRESS BUS LATCHES.
12130
12131  033530  004737  010522                 JSR     PC,READS0            ;READD AND CHECK CONTROL REISTER 0
12132  033534  001405                         BEQ     17$                  ;IF OK THEN CONTINUE
12133  033536                                 ERRDF   1,,S0EROR            ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
12134  033536  104455                         TRAP    C$ERDF
12135  033540  000001                         .WORD   1
12136  033542  000000                         .WORD   0
12137  033544  005306                         .WORD   S0EROR
12138  033546                                 CKLOOP
12139  033546  104406                         TRAP    C$CLP1
12140
12141                                          ;READ CONTROL REGISTER 4 TO CHECK THAT ADDRESS 0 WAS CLOCKED INTO THE
12142                                          ;SYSTEM ADDRESS BUS LATCHES.  WHEN CTS H IS ASSERTED HIGH, THE SYSTEM
12143                                          ;ADDRESS BUS LATHCES ARE ENABLED TO MSAD BITS 17:0
```

C 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 234
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0234

```
12144
12145   033550  005037  002254       17$:    CLR     S4LOAD                      ;SETUP TO EXPECT ADDRESS TO BE 0
12146   033554  004737  010614               JSR     PC,READS4                   ;READ AND CHECK MSAD 15:0
12147   033560  001405                        BEQ     18$                         ;IF OK THEN CONTINUE
12148   033562                                ERRDF   3,MSADRG,S04ERR             ;MSAD 15:0 SYSTEM ADDRESS BUS LATCH ERROR
12149   033562  104455                        TRAP    C$ERDF
12150   033564  000003                        .WORD   3
12151   033566  002510                        .WORD   MSADRG
12152   033570  005406                        .WORD   S04ERR
12153   033572                                CKLOOP
12154   033572  104406                        TRAP    C$CLP1
12155
12156                                         ;READ CONTROL REGISTER 2 TO CHECK THAT MSAD BITS 17 AND 16 ARE ZERO AND
12157                                         ;THAT THE SIGNALS ESR H AND MSBRK H ARE ZERO.  THE SIGNAL WREN H SHOULD
12158                                         ;BE ASSERTED HIGH BECAUSE THE MAP PROTECTION RAM WAS SETUP TO ALLOW
12159                                         ;READS AND WRITES TO ADDRESSES 0-376.
12160
12161   033574  052737  000014  002250 18$:   BIS     #MSEL1!MSEL0,S2MASK         ;SETUP TO IGNORE TRI-STATED BITS
12162   033602  012737  000010  002244        MOV     #MSEL1,S2LOAD               ;SETUP PREVIOULSY LOADED BIT
12163   033610  012737  000100  002246        MOV     #WRENH,S2GOOD               ;EXPECT WREN H TO BE ASSERTED HIGH
12164   033616  004737  010562               JSR     PC,READS2                   ;READ AND CHECK CONTROL REGISTER 2
12165   033622  001405                        BEQ     19$                         ;IF OK THEN CONTINUE
12166   033624                                ERRDF   2,,S2EROR                   ;CONTROL REGISTER 2 NOT EQUAL EXPECTED
12167   033624  104455                        TRAP    C$ERDF
12168   033626  000002                        .WORD   2
12169   033630  000000                        .WORD   0
12170   033632  005322                        .WORD   S2EROR
12171   033634                                CKLOOP
12172   033634  104406                        TRAP    C$CLP1
12173
12174                                         ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
12175                                         ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
12176
12177   033636  004737  012214       19$:    JSR     PC,SLCTTE                   ;SELECT THE TARGET EMULATOR MODULE
12178
12179                                         ;SELECT THE EODAL BUS BY SETTING GDDAL BITS 2:0 TO A 7.  ON A READ
12180                                         ;COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ VIA THE
12181                                         ;SIGNAL RPT7 L.
12182
12183   033642  004537  012234               JSR     R5,SELTER                   ;SELECT REGISTER SPECIFIED BY NEXT WORD
12184   033646  000007                        .WORD   EODAL                       ;SELECT THE EODAL BUS TO BE READ
12185
12186                                         ;AT THIS POINT IN TIME, FDAL REGISTER BITS 7:2 SHOULD BE ENABLED TO THE
12187                                         ;EODAL BUS VIA THE SIGNAL INTER L.  THE FDAL REGISTER WAS LOADED
12188                                         ;PREVIOUSLY WITH A DATA PATTERN OF 251.  WHEN READ ON THE EODAL BUS,
12189                                         ;BITS 1 AND 0 WILL BE READ AS A ZERO.
12190
12191   033650  012737  000250  002346        MOV     #250,T6LOAD                 ;SETUP EXPECTED FDAL DATA TO EODAL BUS
12192   033656  012737  177400  002352        MOV     #177400,T6MASK              ;SETUP TO IGNORE TRI-STATED HIGH BYTE
12193   033664  004737  011224               JSR     PC,READT6                   ;READ AND CHECK THE EODAL BUS
12194   033670  001405                        BEQ     20$                         ;IF OK THEN CONTINUE
12195   033672                                ERRDF   12,FDEODL,T6ALLR            ;FDAL REG 7:2 TO EODAL BUS ERROR
12196   033672  104455                        TRAP    C$ERDF
12197   033674  000014                        .WORD   12
12198   033676  004607                        .WORD   FDEODL
12199   033700  006746                        .WORD   T6ALLR
```

D 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 235
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0235

```
12200   033702                                        CKLOOP
12201   033702   104406                                TRAP    C$CLP1
12202
12203                                                  ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
12204                                                  ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
12205                                                  ;REGISTER 6.
12206
12207   033704   004537   012234          20$:        JSR     R5,SELTER                 ;SELECT REGISTER SPECIFIED BY NEXT WORD
12208   033710   000003                                .WORD   HDAL                      ;SELECT THE HDAL REGISTER
12209
12210   033712   012737   011124   002346             MOV     #HDAL12!HDAL9!HDAL6!HDAL4!HDAL2,T6LOAD ;BITS PREVIOUSLY SET
12211   033720   005037   002352                       CLR     T6MASK                    ;CLEAR CONTROL REGISTER 6 MASK WORD
12212
12213                                                  ;TO ENABLE THE EODAL BUS TO THE CDAL BUS THE PROGRAM MUST SET THE SIGNAL
12214                                                  ;ADAL13 H TO THE HIGH STATE BY SETTING ADAL13 H TO A ONE. WHEN ADAL13 H,
12215                                                  ;PSEL0 L, AND PSEL1 H ARE ASSERTED HIGH, THE SIGNAL COLB L WILL BE ASSERTED
12216                                                  ;LOW THUS ENABLING THE LOW BYTE OF THE EODAL BUS TO THE CDAL BUS.
12217                                                  ;THE EODAL BUS PRESENTLY CONTAINS DATA FROM FDAL REGISTER BITS 7:2 (250).
12218                                                  ;THE CDAL BUS WILL UNCONDITIONALLY BE ENABLED TO THE EIDAL BUS.  THE CDAL
12219                                                  ;BUS WILL ALSO BE ENABLED TO THE TDAL BUS BY THE SIGNALS DTHB L AND
12220                                                  ;DTLB L BEING ASSERTED LOW.  THESE TWO SIGNALS ARE ASSERTED LOW AS A
12221                                                  ;RESULT OF WVIOL L, ETR H, PR/WLB L, MR11 H, PBCLR L, AND PSEL0 L BEING
12222                                                  ;ASSERTED HIGH.
12223
12224   033724   052777   020000   146254             BIS     #ADAL13,@REG2             ;SET ADAL13 H TO THE HIGH STATE
12225
12226                                                  ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ
12227                                                  ;COMMAND TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ VIA RPT6 L.
12228
12229   033732   004537   012234                       JSR     R5,SELTER                 ;SELECT REG SPECIFIED BY NEXT WORD
12230   033736   000006                                .WORD   EIDAL                     ;SELECT THE EIDAL BUS TO BE READ
12231
12232                                                  ;AT THE PRESENT TIME DATA FROM FDAL REGISTER BITS 7:2 (250) ARE ENABLED
12233                                                  ;TO THE EODAL BUS, THE CDAL BUS, THE EIDAL BUS AND THE TDAL BUS VIA
12234                                                  ;THE SIGNALS INTER L, COLB L, DTHB L AND DTLB L.  THE FOLLOWING SECTION
12235                                                  ;WILL READ THE EIDAL BUS TO CHECK THAT THE FDAL REGISTER DATA IS ENABLED
12236                                                  ;TO IT VIA THE EODAL AND CDAL BUSSES.
12237
12238   033740   012737   000250   002346             MOV     #250,T6LOAD               ;SETUP EXPECTED FDAL TO EIDAL BUS DATA
12239   033746   012737   177400   002352             MOV     #177400,T6MASK            ;SETUP TI IGNORE TRI-STATED HIGH BYTE
12240   033754   004737   011224                       JSR     PC,READT6                 ;READ AND CHECK EIDAL BUS DATA
12241   033760   001405                                BEQ     21$                       ;IF DATA OK THEN CONTINUE
12242   033762                                         ERRDF   12,FDEIDL,T6ALLR          ;FDAL REG 7:2 TO EIDAL BUS ERROR VIA CDAL
12243   033762   104455                                TRAP    C$ERDF
12244   033764   000014                                .WORD   12
12245   033766   004647                                .WORD   FDEIDL
12246   033770   006746                                .WORD   T6ALLR
12247   033772                                         CKLOOP
12248   033772   104406                                TRAP    C$CLP1
12249   033774   042777   020000   146204  21$:        BIC     #ADAL13,@REG2             ;CLEAR ADAL13 TO DISABLE COLB L
12250
12251                                                  ;AT THE PRESENT TIME DATA FROM FDAL REGISTER BITS 7:2 (250) ARE ENABLED
12252                                                  ;TO THE EODAL BUS, THE CDAL BUS, THE EIDAL BUS AND THE TDAL BUS VIA THE
12253                                                  ;SIGNALS  INTER L,  COLB L,  DTHB L,  AND  DTLB L.  TO  CHECK
12254                                                  ;THAT FDAL REGISTER BITS 7:2 (250) ARE ENABLED TO THE TDAL BUS, THE
12255                                                  ;PROGRAM MUST CLOCK THE DATA INTO THE TDAL DIAGNOSTIC LATCHES FIRST SO
```

```
12256                                              ;THAT THE DATA CAN BE READ BACK LATER ON IN THIS TEST.  TO CLOCK THE
12257                                              ;DATA INTO THE TDAL LATCHES, THE PROGRAM MUST SET THE SIGNAL VDAL2 H TO
12258                                              ;A ONE AND THEN ZERO.  PULSING THE SIGNAL VDAL2 H WILL CAUSE A PULSE ON
12259                                              ;THE SIGNAL "INVD L" WHICH WILL CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS,
12260                                              ;THE EDFET AND BTFET FLIP-FLOPS.  WITH THESE FLIP-FLOPS CLEARED, THE
12261                                              ;FDAL REGISTER DATA WILL BE DISABLED FROM THE CDAL BUS, THE EIDAL BUS AND
12262                                              ;THE TDAL BUS.  THE SIGNAL FETCT H WILL ALSO BE SET TO A ZERO IN THE
12263                                              ;FOLLOWING SECTION.
12264
12265   034002  012737  000004  002340         MOV     #VDAL2,T4LOAD           ;SET FETCT H LOW AND SET VDAL2 H HIGH
12266   034010  013737  002340  002342         MOV     T4LOAD,T4GOOD           ;COPY DATA LOADED TO EXPECTED
12267   034016  052737  000040  002342         BIS     #VDAL5,T4GOOD           ;EXPECT BTS1 H TO BE A 1 VIA INTER L
12268   034024  004737  011172                 JSR     PC,LDRD4T               ;LOAD, READ AND CHECK VDAL REGISTER
12269   034030  001405                          BEQ     22$                    ;IF LOADED OK THEN CONTINUE
12270   034032                                  ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
12271   034032  104455                          TRAP    C$ERDF
12272   034034  000013                          .WORD   11
12273   034036  003710                          .WORD   VDALRG
12274   034040  006716                          .WORD   T4EROR
12275   034042                                  CKLOOP
12276   034042  104406                          TRAP    C$CLP1
12277   034044  042737  000004  002340  22$:    BIC     #VDAL2,T4LOAD           ;SETUP TO SET VDAL2 H LOW
12278   034052  042737  000004  002342         BIC     #VDAL2,T4GOOD           ;SETUP TO EXPECT VDAL2 H TO BE A 0
12279   034060  004737  011172                 JSR     PC,LDRD4T               ;LOAD, READ AND CHECK VDAL REGISTER
12280   034064  001405                          BEQ     23$                    ;IF LOADED OK THEN CONTINUE
12281   034066                                  ERRDF   11,VDALRG,T4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
12282   034066  104455                          TRAP    C$ERDF
12283   034070  000013                          .WORD   11
12284   034072  003710                          .WORD   VDALRG
12285   034074  006716                          .WORD   T4EROR
12286   034076                                  CKLOOP
12287   034076  104406                          TRAP    C$CLP1
12288
12289                                              ;SELECT THE HDAL REGISTER BY SETTING GDAL BITS 2:0 TO A 3.  THE HDAL
12290                                              ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO CONTROL
12291                                              ;REGISTER 6.
12292
12293   034100  004537  012234         23$:    JSR     R5,SELTER               ;SELECT REGISTER SPECIFIED BY NEXT WORD
12294   034104  000003                          .WORD   HDAL                   ;SELECT THE HDAL REGISTER
12295
12296                                              ;THE FOLLOWING SECTION WILL SET THE SIGNALS XRAS H AND PPI H TO THE
12297                                              ;LOW STATE BY CLEARING HDAL REGISTER BITS 15 AND 12.
12298
12299   034106  012737  111124  002346         MOV     #HDAL15!HDAL12!HDAL9!HDAL6!HDAL4!HDAL2,T6LOAD  ;LOADED BITS
12300   034114  005037  002352                 CLR     T6MASK                 ;SETUP MASK WORD TO CHECK ALL BITS
12301   034120  004737  012542                 JSR     PC,XPIL                ;SET XPI H AND PPI H LOW
12302   034124  004737  012332                 JSR     PC,XRASL               ;SET XRAS H AND PRAS H LOW
12303
12304                                              ;SET HDAL BIT 4 TO A ZERO AND HDAL BIT 3 TO A ONE TO SET PR/WHB L HIGH
12305                                              ;AND PR/WLB L LOW.
12306
12307   034130  042737  000020  002346         BIC     #HDAL4,T6LOAD           ;SET PR/WHB L HIGH
12308   034136  052737  000010  002346         BIS     #HDAL3,T6LOAD           ;SET PR/WLB L LOW
12309   034144  004737  011216                 JSR     PC,LDRDT6               ;LOAD, READ AND CHECK THE HDAL REGISTER
12310   034150  001405                          BEQ     24$                    ;IF LOADED OK THEN CONTINUE
12311   034152                                  ERRDF   12,HDALRG,T06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
```

F 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 237
CVCDDB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0237

```
12312   034152   104455                          TRAP    C$ERDF
12313   034154   000014                          .WORD   12
12314   034156   003756                          .WORD   HDALRG
12315   034160   006732                          .WORD   TO6ERR
12316   034162                                   CKLOOP
12317   034162   104406                          TRAP    C$CLP1
12318
12319                                            ;SET THE SIGNAL VDAL0 H TO A ONE TO ENABLE THE OUTPUTS OF THE TDAL
12320                                            ;DIAGNOSTIC LATCHES ONTO THE TDAL BUS. THE TDAL LATCHES WERE LOADED
12321                                            ;WITH DATA FROM FDAL REGISTER BITS 7:2 (250) EARLIER IN THIS TEST.
12322
12323   034164   052737  000001  002340  24$:    BIS     #VDAL0,T4LOAD          ;SETUP BIT TO BE LOADED
12324   034172   052737  000001  002342          BIS     #VDAL0,T4GOOD          ;EXPECT VDAL0 H TO BE SET ON READ
12325   034200   004737  011172                  JSR     PC,LDRD4T              ;LOAD, READ AND CHECK VDAL REGISTER
12326   034204   001405                          BEQ     25$                    ;IF LOADED OK THEN CONTINUE
12327   034206                                   ERRDF   11,VDALRG,T4EROR       ;VDAL REGISTER NOT EQUAL EXPECTED
12328   034206   104455                          TRAP    C$ERDF
12329   034210   000013                          .WORD   11
12330   034212   003710                          .WORD   VDALRG
12331   034214   006716                          .WORD   T4EROR
12332   034216                                   CKLOOP
12333   034216   104406                          TRAP    C$CLP1
12334
12335                                            ;THE FOLLOWING SIGNALS ETR H , MR11 H , PR/WHB L , AND  PSMW L
12336                                            ;SHOULD BE ASSERTED HIGH.  THERFORE, BY SETTING PPI H TO THE HIGH
12337                                            ;STATE, THE SIGNAL DBLB L SHOULD BE ASSERTED LOW..  THIS
12338                                            ;SIGNAL WILL ENABLE THE TDAL BUS,   WHICH HAS THE TDAL DIAGNOSTIC
12339                                            ;LATCHES ENABLED TO IT, TO THE CDAL BUS AND THE CDAL BUS WILL BE ENABLED
12340                                            ;TO THE EIDAL BUS UNCONDTIONALLY.  THE TDAL LATCHES WERE LOADED EARLIER
12341                                            ;IN THIS TEST WITH DATA FROM FDAL REGISTER BITS 7:2 (250).
12342
12343   034220   004737  012510          25$:    JSR     PC,XPIH                ;SET XPI H AND PPI H TO HIGH STATE
12344
12345                                            ;SELECT THE EIDAL BUS BY SETTING GDAL BITS 2:0 TO A 6.  ON A READ
12346                                            ;COMMAND TO CONTROL REGISTER 6, THE EIDAL BUS WILL BE READ VIA THE
12347                                            ;SIGNAL RPT6 L.
12348
12349   034224   004537  012234                  JSR     R5,SELTER              ;SELECT REGISTER SPECIFIED BY NEXT WORD
12350   034230   000006                          .WORD   EIDAL                  ;SELECT THE EIDAL BUS TO BE READ
12351
12352                                            ;AT THE PRESENT TIME THE TDAL DIAGNOSTIC LATCHES ARE ENABLED TO THE
12353                                            ;TDAL BUS, THE CDAL BUS AND THE EIDAL BUS VIA THE SIGHALS VDAL0 H,
12354                                            ;DBLB L.  THE TDAL LATCHES WERE LOADED EARLIER IN THE  TEST
12355                                            ;WITH DATA FROM FDAL REGISTER BITS 7:2 (250).  THE PROGRAM WILL
12356                                            ;NOW READ THE EIDAL BUS TO CHECK THAT FDAL REGISTER BITS 7:2 DATA
12357                                            ;(250) WAS LOADED INTO THE TDAL LATCHES AND THAT THE TDAL LATCHES
12358                                            ;ARE ENABLED TO THE EIDAL BUS.
12359
12360   034232   012737  000250  002346          MOV     #250,T6LOAD           ;SETUP EXPECTED FDAL TO EIDAL BUS DATA
12361   034240   012737  177400  002352          MOV     #177400,T6MASK        ;SETUP TO IGNORE TRI-STATED HIGH BYTE
12362   034246   004737  011224                  JSR     PC,READT6             ;READ AND CHECK THE EIDAL BUS
12363   034252   001405                          BEQ     26$                    ;IF DATA OK THEN CONTINUE
12364   034254                                   ERRDF   12,FDTDEI,T6ALLR       ;FDAL TO TDAL LATCHES TO EIDAL BUS ERROR
12365   034254   104455                          TRAP    C$ERDF
12366   034256   000014                          .WORD   12
12367   034260   004707                          .WORD   FDTDEI
```

G 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 238
CVCODB.P11   14-JUN-82 09:54   TEST 12: W/R DATA TO/FROM TDAL LATCHES WITH ETR H SET HIGH - 8 BIT MODE   SEQ 0238

```
12368  034262  006746                              .WORD    T6ALLR
12369  034264                              CKLOOP
12370  034264  104406                              TRAP     C$CLP1
12371
12372                                      ;SELECT THE HDAL REGISER BY SETTING DGAL BITS 2:0 TO A 3.  THE HDAL
12373                                      ;REGISTER WILL BE WRITTEN OR READ ON A WRITE OR READ COMMAND TO
12374                                      ;CONTROL REGISTER 6.
12375
12376  034266  004537  012234      26$:   JSR      R5,SELTER             ;SELECT REGISTER SPECIFIED BY NEXT WORD
12377  034272  000003                             .WORD    HDAL                  ;SELECT THE HDAL REGISTER
12378
12379  034274  012737  101014  002346      MOV     #HDAL15!HDAL9!HDAL3!HDAL2,T6LOAD ;BIT LOADED BEFORE - HDAL6 H
12380  034302  005037  002352              CLR     T6MASK                ;SETUP MASK TO CHECK ALL BITS
12381
12382                                      ;SET THE SIGNALS XPI H AND PPI H TO THE LOW STATE BY CLEARING HDAL
12383                                      ;REGISTER BIT 15.  ALOS SET THE SIGNAL PSEL1 L TO THE HIGH STATE BY
12384                                      ;SETTING HDAL REGISTER BIT 6 TO A 0.
12385
12386  034306  004737  012542              JSR      PC,XPIL              ;SET XPI H AND PPI H TO LOW STATE
12387
12388                                      ;ISSUE A PULSE ON THE SIGNAL "INVD L" TO RE-INITIALIZE THE MODULE.
12389
12390  034312  005037  002340              CLR      T4LOAD               ;SETUP TO CLEAR ALL BITS
12391  034316  004737  012706              JSR      PC,CLRPSM            ;GO PULSE INVD L VIA VDAL2 H
12392
12393  034322                              ENDSEG
12394  034322                      10002$:
12395  034322  104405                      TRAP     C$ESEG
12396
12397  034324                              ENDTST
12398  034324                      L10050:
12399  034324  104401                      TRAP     C$ETST
12400
```

```
12401                              .SBTTL   TEST 13: CHECK SA SIGNAL ''EDBRK H'' TO TE MODULE
12402
12403                              ;++
12404                              ; THIS TEST WILL CHECK THAT STATE ANALYZER SIGNAL ''EDBRK H'' CAN BE ASSERTED HIGH
12405                              ; AND LOW WHEN STATE ANALYZER'S FUNCTION SELECT FLIP-FLOP ''FUSL2'' IS CLEARED AND
12406                              ; SET.  THE OUTPUT OF FUNCTION SELECT FLIP-FLOP ''FUSL2'' IS ENABLED TO THE SYSTEM
12407                              ; BUS WHEN THE SIGNAL ''CDAL1 H'' IS ASSERTED HIGH.  THE PROGRAM WILL CHECK THAT
12408                              ; THE SIGNAL ''EDBRK H'' IS ASSERTED HIGH AND LOW BY READING THIS SIGNAL IN THE
12409                              ; TARGET EMULATOR'S CONTROL REGISTER 0.  THE TEST WILL ALSO CHECK THAT THE SIGNAL
12410                              ; ''EDBRK H'' WILL CAUSE THE TARGET EMULATOR'S PAUSE STATE LOGIC TO BE ENTERED IN
12411                              ; ''RUN'' MODE WHEN THE SIGNAL ''FETCT H'' IS ASSERTED HIGH AND A PULSE IS ISSUED ON
12412                              ; THE SIGNAL ''XRAS H''.
12413                              ;--
12414
12415    034326                   BGNTST
12416    034326           T13::
12417
12418    034326  004737  007440        JSR     PC,INITMD               ;INITIALIZE THE SYSTEM MODULES
12419
12420    034332                   BGNSEG
12421    034332  104404          TRAP     C$BSEG
12422
12423                              ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
12424                              ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER
12425
12426    034334  004737  012144        JSR     PC,SLCTED               ;SELECT THE STATE ANALYZER MODULE
12427
12428                              ;CLEAR LOW BYTE OF CONTROL REGISTER 0.  CDAL7 H BEING SET TO A ZERO
12429                              ;WILL ENBALE THE OUTPUTS OF THE OR ADDRESS REGISTER TO ORAD 3:0.
12430                              ;CDAL4 H ON A ZERO WILL ENABLE ONLY ONE AND/OR ARRAY RAM TO BE SELECTED
12431                              ;AT ONE TIME VIA THE POINTER REGISTER.  IN THIS TEST PTER15 L WILL
12432                              ;SELECT THE OR ARRAY RAM.  CDAL1 H ON A ZERO WILL DISABLE THE SIGNAL
12433                              ;FUSL2 H TO THE SYSTEM BUS SIGNAL EDBRK H.
12434
12435    034340  105037  002272        CLRB    EOLOAD                  ;SETUP TO CLEAR LOW BYTE
12436    034344  004737  010700        JSR     PC,LDRDEO               ;LOAD, READ AND CHECK CDAL REGISTER
12437    034350  001405              BEQ     1$                      ;IF LOADED OK THEN CONTINUE
12438    034352                      ERRDF   5,CDALRG,EOEROR         ;CDAL REGISTER NOT EQUAL EXPECTED
12439    034352  104455              TRAP    C$ERDF
12440    034354  000005              .WORD   5
12441    034356  003010              .WORD   CDALRG
12442    034360  006146              .WORD   EOEROR
12443    034362                      CKLOOP
12444    034362  104406              TRAP    C$CLP1
12445
12446                              ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER BY LOADING THE
12447                              ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.  ON A WRITE
12448                              ;OR READ COMMAND OT CONTROL REGISTER 6 WHEN PTER15 L IS ASSERTED. THE
12449                              ;OR ADDRESS REGISTER WILL BE WRITTEN OR READ.  PDAL REGISTER BIT 5 WILL
12450                              ;REMAIN A ZERO TO HOLD THE FLIP-FLOP'S FUSL7 AND FUSL 3:0 TO THE PRESET
12451                              ;STATE.
12452
12453    034364  004537  012164   1$:    JSR     R5,LDPDAL               ;LOAD AND CHECK PDAL REG WITH NEXT WORD
12454    034370  000017              .WORD   PTER15                  ;SETUP TO WRITE/READ OR ADDRESS REG
12455
12456                              ;LOAD, READ AND CHECK THE OR ADDRESS REGISTER WITH A DATA PATTERN OF ALL
```

I 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 240
CVCDDB.P11   14-JUN-82 09:54   TEST 13: CHECK SA SIGNAL ''EDBRK H'' TO TE MODULE   SEQ 0240

```
12457                                           ;ZEROES WHICH WILL CAUSE ADDRESS ZERO OF THE OR ARRAY RAM TO BE SELECTED.
12458                                           ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L
12459                                           ;ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH WILL LOAD
12460                                           ;THE ''OR ADDRESS REGISTER''.  ON A READ COMMAND TO CONTROL REGISTER 6
12461                                           ;WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL
12462                                           ;RPT15 H WHICH WILL READ THE DATA FROM THE ''OR ADDRESS REGISTER''.
12463
12464   034372  005037  002316            CLR     E6LOAD              ;SETUP TO LOAD ALL ZEROES
12465   034376  012737  177760  002320    MOV     #177760,E6MASK      ;SETUP TO IGNORE UNWANTED BITS
12466   034404  004737  011046            JSR     PC,LDRDE6           ;LOAD, READ AND CHECK ''OR ADDRESS REG''
12467   034410  001405                    BEQ     2$                  ;IF LOADED OK THEN CONTINUE
12468   034412                            ERRDF   8,ORADER,E026ER     ;''OR ADDRESS REG'' ERROR ORAD 3:0
12469   034412  104455                    TRAP    C$ERDF
12470   034414  000010                    .WORD   8
12471   034416  003547                    .WORD   ORADER
12472   034420  006212                    .WORD   E026ER
12473   034422                            CKLOOP
12474   034422  104406                    TRAP    C$CLP1
12475
12476                                           ;LOAD READ AND CHECK THE OR ARRAY RAM ADDRESSED BY THE OR ADDRESS
12477                                           ;REGISTER WITH A DATA PATTERN OF 004.  THE SIGNALS OR07 L TO OR03 L
12478                                           ;AND OR01 L TO OR00 L WILL BE ASSERTED HIGH AND THE SIGNAL OR02 L
12479                                           ;WILL BE ASSERTED LOW.
12480
12481   034424  012737  000004  002304  2$: MOV  #4,E4LOAD           ;SETUP DATA TO BE LOADED
12482   034432  012737  177400  002310    MOV     #177400,E4MASK      ;SETUP MASK TO IGNORE UNWANTED BITS
12483   034440  004737  011000            JSR     PC,LDRDE4           ;LOAD, READ AND CHECK OR ARRAY RAM
12484   034444  001405                    BEQ     3$                  ;IF LOADED OK THEN CONTINUE
12485   034446                            ERRDF   7,ORDATA,E4EROR     ;''OR ARRAY RAM'' DATA ERROR
12486   034446  104455                    TRAP    C$ERDF
12487   034450  000007                    .WORD   7
12488   034452  003057                    .WORD   ORDATA
12489   034454  006176                    .WORD   E4EROR
12490   034456                            CKLOOP
12491   034456  104406                    TRAP    C$CLP1
12492
12493                                           ;DISABLE THE PRESET SIGNAL TO THE FUNCTION SELECT FLIP-FLOPS FUSL7,
12494                                           ;FUSL3, FUSL2, FUSL1 AND FUSL0 BY SETTING PDAL5 H TO A ONE. THE BITS
12495                                           ;TO ASSERT THE SIGNAL PTER15 L LOW WILL ALSO REMAIN SET.
12496
12497   034460  004537  012164          3$: JSR  R5,LDPDAL           ;LOAD READ + CHECK PDAL WITH NEXT WORD
12498   034464  000057                    .WORD   PDAL5!PTER15        ;SET PDAL5 H TO 1 AND PTER15 L LOW
12499
12500                                           ;SET AND CLEAR THE SIGNAL CDAL6 H IN CONTROL REGISTER 0.  SETTING AND
12501                                           ;CLEARING CDAL6 H WILL CAUSE THE ''AND STABLE'' ONE SHOT TO FIRE WHICH
12502                                           ;WILL CAUSE THE ''OR STABLE'' ONE SHOT TO FIRE.  THE ''OR STABLE'' ONE
12503                                           ;SHOT BEING FIRED WILL CLOCK THE ''OR ARRAY RAM'' DATA INTO THE FUNCTION
12504                                           ;SELECT FLIP-FLOPS.  WITH A DATA PATTERN OF 004 IN THE ''OR ARRAY RAM'',
12505                                           ;FUNCTION SELECT FLIP-FLOP FUSL2 SHOULD BE CLEARED THUS SETTING THE
12506                                           ;SIGNAL FUSL2 H TO THE HIGH STATE. ALL OTHER FUNCTION SELECT FLIP-FLOPS
12507                                           ;WILL BE SET TO A ONE THUS SETTING THERE OUTPUTS LOW.
12508
12509   034466  052737  000100  002272  4$: BIS  #CDAL6,E0LOAD       ;SET THE SIGNAL TRANST H HIGH
12510   034474  004737  010700            JSR     PC,LDRDE0           ;LOAD, READ AND CHECK CDAL REGISTER
12511   034500  001405                    BEQ     5$                  ;IF LOADED OK THEN CONTINUE
12512   034502                            ERRDF   5,CDALRG,E0EROR     ;CDAL REGISTER NOT EQUAL EXPECTED
```

J 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 241
CVCDDB.P11   14-JUN-82 09:54   TEST 13: CHECK SA SIGNAL "EDBRK H" TO TE MODULE   SEQ 0241

```
12513  034502  104455                          TRAP    C$ERDF
12514  034504  000005                          .WORD   5
12515  034506  003010                          .WORD   CDALRG
12516  034510  006146                          .WORD   EOEROR
12517  034512                                  CKLOOP
12518  034512  104406                          TRAP    C$CLP1
12519  034514  042737  000100  002272  5$:     BIC     #CDAL6,EOLOAD        ;SET THE SIGNAL TRANST H LOW
12520  034522  004737  010700                  JSR     PC,LDRDEO           ;LOAD, READ AND CHECK CDAL REGISTER
12521  034526  001405                          BEQ     6$                  ;IF LOADED OK THEN CONTINUE
12522  034530                                  ERRDF   5,CDALRG,EOEROR     ;CDAL REGISTER NOT EQUAL EXPECTED
12523  034530  104455                          TRAP    C$ERDF
12524  034532  000005                          .WORD   5
12525  034534  003010                          .WORD   CDALRG
12526  034536  006146                          .WORD   EOEROR
12527  034540                                  CKLOOP
12528  034540  104406                          TRAP    C$CLP1
12529
12530                                          ;CHECK THAT FUNCTION SELECT FLIP-FLOP FUSL7  IS SET TO A ONE (LOW)
12531                                          ;BY READING THE OR ARRAY RAM DATA AND FUSL7 IN BIT 12 OF CONTROL
12532                                          ;REGISTER 4.
12533
12534  034542  042737  010000  002310  6$:     BIC     #BIT12,E4MASK       ;SETUP TO READ FUSL7 H
12535  034550  004737  011014                  JSR     PC,READE4           ;READ OR ARRAY RAM DATA AND FUSL7 H
12536  034554  001405                          BEQ     7$                  ;IF OK THEN CONTINUE
12537  034556                                  ERRDF   7,FUSL7,E4EROR      ;FUSL7 PROBABLY NOT SET TO ONE (LOW)
12538  034556  104455                          TRAP    C$ERDF
12539  034560  000007                          .WORD   7
12540  034562  003121                          .WORD   FUSL7
12541  034564  006176                          .WORD   E4EROR
12542  034566                                  CKLOOP
12543  034566  104406                          TRAP    C$CLP1
12544
12545                                          ;ASSER THE SIGNAL PTER4 L IN THE POINTER REGISTER BY LOADING THE
12546                                          ;APPROPRIATE BITS IN CONTROL REGISTER 2'S PDAL REGISTER.  THE
12547                                          ;SIGNAL PDAL5 H WILL ALSO REMAIN SET.
12548
12549  034570  004537  012164          7$:     JSR     R5,LDPDAL           ;LOAD AND CHECK PDAL REG WITH NEXT WORD
12550  034574  000044                          .WORD   PDAL5!PTER4         ;SETUP TO READ FUSL F/F'S 3:0
12551
12552                                          ;READ FUNCTION SELECT FLIP-FLOPS FUSL 3:0 VIA CONTROL REGISTER 6.
12553                                          ;FUSL2 SHOULD BE SET TO ONE ON A READ COMMAND AND ALL OTHER FUNCTION
12554                                          ;SELECT FLIP-FLOPS SHOULD BE READ AS A ZERO.
12555
12556  034576  012737  040000  002316          MOV     #BIT14,E6LOAD       ;SETUP FUSL2 BIT TO BE SET
12557  034604  012737  007777  002320          MOV     #007777,E6MASK      ;SETUP TO IGNORE TRDI BITS
12558  034612  004737  011054                  JSR     PC,READE6           ;READ AND CHECK FUSL F/F'S 3:0
12559  034616  001405                          BEQ     8$                  ;IF OK THEN CONTINUE
12560  034620                                  ERRDF   8,FUSL30,E6ALLR     ;FUSL2 NOT 1 OR OTHER F/F'S SET
12561  034620  104455                          TRAP    C$ERDF
12562  034622  000010                          .WORD   8
12563  034624  003607                          .WORD   FUSL30
12564  034626  006226                          .WORD   E6ALLR
12565  034630                                  CKLOOP
12566  034630  104406                          TRAP    C$CLP1
12567
12568                                          ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
```

K 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 242
CVCDDB.P11   14-JUN-82 09:54   TEST 13: CHECK SA SIGNAL "EDBRK H" TO TE MODULE   SEQ 0242

```
12569                                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER
12570
12571   034632  004737  012214        8$:     JSR     PC,SLCTTE              ;SELECT TARGET EMULATOR MODULE.
12572
12573                                          ;SET ADAL REGISTER BITS 10, 9 AND 4 TO A ONES AND ALL OTHER ADAL BITS TO
12574                                          ;A ZERO.  PULSE THE SIGNAL "BRKRES L" BY SETTING AND CLEARING ADAL
12575                                          ;REGISTER BIT 0.  ADAL10 H AND ADAL9 H SET TO ONES WILL ENABLE THE
12576                                          ;TARGET EMULATOR SIGNALS TO THE SYSTEM BUS.  ADAL4 H SET TO A ONE
12577                                          ;WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE RUN MODE WHEN A
12578                                          ;PULSE IS ISSUED ON THE SIGNAL XRAS H.  A PULSE ON THE SIGNAL BRKRES L
12579                                          ;VIA ADAL0 H WILL CLEAR THE BREAK LOGIC ON THE MEMORY SIMULATOR MODULE.
12580
12581   034636  012737  003000  002334        MOV     #ADAL10!ADAL9,T2LOAD   ;SETUP ADAL REGISTER BITS TO LOAD
12582   034644  004737  012766               JSR     PC,BRKRES              ;SET BITS AND PULSE BRKRES L
12583
12584                                          ;READ CONTROL REGISTER 0 TO CHECK THAT NO BREAKS ARE SET IN GDAL
12585                                          ;BITS 7:4.  ALSO LOAD BITS IN CONTROL REGISTER 0'S GDAL REGISTER TO
12586                                          ;SELECT THE HDAL REGISTER.  THE HDAL REGISTER WILL BE WRITTEN OR READ
12587                                          ;ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
12588
12589   034650  112737  C00003  002324        MOVB    #HDAL,TOLOAD           ;SETUP BITS TO BE LOADED
12590   034656  004737  011100               JSR     PC,LDRDT0             ;LOAD, READ AND CHECK GDAL REGISTER
12591   034662  001405                        BEQ     9$                    ;IF LOADED OK THEN CONTINUE
12592   034664                                ERRDF   9,GDALRG,TOEROR       ;GDAL REGISTER NOT EQUAL TO EXPECTED
12593   034664  104455                        TRAP    C$ERDF
12594   034666  000011                        .WORD   9
12595   034670  003640                        .WORD   GDALRG
12596   034672  006666                        .WORD   TOEROR
12597   034674                                CKLOOP
12598   034674  104406                        TRAP    C$CLP1
12599
12600                                          ;SET HDAL REGISTER BIT 2 TO A ONE AND ALL OTHER HDAL BITS TO A ZERO.
12601                                          ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11 TIMING
12602                                          ;AND CONTROL SIGNALS.
12603
12604   034676  012737  000004  002346  9$:   MOV     #HDAL2,T6LOAD          ;SETUP BIT TO BE LOADED
12605   034704  004737  011216               JSR     PC,LDRDT6            ;LOAD, READ AND CHECK HDAL REGISTER
12606   034710  001405                        BEQ     10$                   ;IF LOADED OK THEN CONTINUE
12607   034712                                ERRDF   12,HDALRG,TO6ERR      ;HDAL REGISTER NOT EQUAL TO EXPECTED
12608   034712  104455                        TRAP    C$ERDF
12609   034714  000014                        .WORD   12
12610   034716  003756                        .WORD   HDALRG
12611   034720  006732                        .WORD   TO6ERR
12612   034722                                CKLOOP
12613   034722  104406                        TRAP    C$CLP1
12614
12615                                          ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL2 H IN CONTROL
12616                                          ;REGISTER 4.  PULSING THE SIGNAL INVD L WILL INITIALIZE ALL THE
12617                                          ;FLIP-FLOP'S ON THE MODULE NOT CLEARED BY BRKRES L.  SET THE SIGNAL
12618                                          ;FETCT H TO THE HIGH STATE BY SETTING VDAL REGISTER BIT 7 TO A ONE.
12619
12620   034724  012737  000200  002340 10$:   MOV     #VDAL7,T4LOAD          ;SET BIT TO SET FETCT H HIGH
12621   034732  004737  012706               JSR     PC,CLRPSM             ;PULSE INVD L BY TOGGLING VDAL4 H
12622
12623                                          ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
12624                                          ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
```

L 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 243
CVCDDB.P11   14-JUN-82 09:54   TEST 13: CHECK SA SIGNAL ''EDBRK H'' TO TE MODULE   SEQ 0243

```
12625
12626    034736  004737  012144                    JSR     PC,SLCTED                ;SELECT THE STATE ANALYZER MODULE
12627
12628                                               ;SET THE SIGNAL CDAL1 H TO A ONE TO ENABLE FUNCTION SELECT FLIP-FLOP
12629                                               ;FUSL2 TO THE SYSTEM BUS AS THE SIGNAL EDBRK H.  THE FLIP-FLOP SHOULD
12630                                               ;BE CLEARED THUS SETTING THE SIGNAL FUSL2 H TO THE HIGH STATE WHICH
12631                                               ;WILL CAUSE THE SIGNAL EDBRK H TO BE SET TO THE HIGH STATE.
12632
12633    034742  052737  000002  002272            BIS     #CDAL1,EOLOAD            ;SETUP BIT TO BE LOADED
12634    034750  004737  010700                     JSR     PC,LDRDEO               ;LOAD, READ AND CHECK CDAL REGISTER
12635    034754  001405                             BEQ     11$                     ;IF LOADED OK THEN CONTINUE
12636    034756                                     ERRDF   5,CDALRG,EOEROR         ;CDAL REGISTER NOT EQUAL EXPECTED
12637    034756  104455                             TRAP    C$ERDF
12638    034760  000005                             .WORD   5
12639    034762  003010                             .WORD   CDALRG
12640    034764  006146                             .WORD   EOEROR
12641    034766                                     CKLOOP
12642    034766  104406                             TRAP    C$CLP1
12643
12644                                               ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
12645                                               ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
12646
12647    034770  004737  012214            11$:     JSR     PC,SLCTTE               ;SELECT THE TARGET EMULATOR MODULE
12648
12649                                               ;READ CONTROL REGISTER 0 TO CHECK THAT STATE ANALYZER'S SIGNAL EDBRK H
12650                                               ;IS READ AS A ONE IN THE GDAL REGISTER.  THE SIGNAL EDBRK H SHOULD BE
12651                                               ;ASSERTED HIGH AS A RESULT OF STATE ANALYZER'S FUNCTION SELECT FLIP-
12652                                               ;FLOP FUSL2 BEING CLEARED AND CDAL1 H BEING ASSERTED HIGH.
12653
12654    034774  052737  000020  002326            BIS     #EDBRK,TOGOOD           ;EXPECT EDBRK H TO BE A ONE
12655    035002  004737  011114                     JSR     PC,READTO               ;READ AND CHECK GDAL REGISTER
12656    035006  001405                             BEQ     12$                     ;IF OK THEN CONTINUE
12657    035010                                     ERRDF   9,GDALRG,TOEROR         ;EDBRK H PROBABLY NOT SET HIGH
12658    035010  104455                             TRAP    C$ERDF
12659    035012  000011                             .WORD   9
12660    035014  003640                             .WORD   GDALRG
12661    035016  006666                             .WORD   TOEROR
12662    035020                                     CKLOOP
12663    035020  104406                             TRAP    C$CLP1
12664
12665                                               ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H. WHEN XRAS H
12666                                               ;IS SET HIGH, THE PAUSE MODE FLIP-FLOP WILL BE SET TO RUN MODE THUS
12667                                               ;SETTING THE SIGNAL PAUSE L TO THE LOW STATE, THE EDFET FLIP-FLOP WILL
12668                                               ;BE SET TO A ONE THUS SETTING THE SIGNAL EDFET H TO THE HIGH STATE,
12669                                               ;AND THE BTFET FLIP-FLOP WILL BE SET TO A ONE THUS SETTING THE SIGNAL
12670                                               ;BTFET L TO THE LOW STATE.  AS A RESULT OF EDBRK H BEING ASSERTED HIGH,
12671                                               ;THE SIGNALS BRK H AND SOP H WILL BE ASSERTED HIGH.  AS A RESULT OF
12672                                               ;SOP H AND EDFET H BEING ASSERTED HIGH, THE PAUSE STATE WORKING FLIP-
12673                                               ;FLOP WILL BE DIRECT SET TO A ONE THUS CAUSING THE SIGNAL PSMW H TO
12674                                               ;BE ASSERTED HIGH.
12675
12676    035022  004737  012266            12$:     JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
12677
12678                                               ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-
12679                                               ;FLOP IS SET TO A ONE AS A RESULT OF EDBRK H AND EDFET H BEING
12680                                               ;ASSERTED HIGH.  THE SIGNAL BTS1 H WILL ALSO BE SET TO A ONE AS A
```

M 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 244
CVCDDB.P11   14-JUN-82 09:54   TEST 13: CHECK SA SIGNAL ''EDBRK H'' TO TE MODULE   SEQ 0244

```
12681                                                ;RESULT OF THE BTFET FLIP-FLOP BEING SET TO A ONE AND THE SIGNAL INTER L
12682                                                ;BEING ASSERTED HIGH.
12683
12684   035026  052737  001040  002342       BIS     #VDAL9!VDAL5,T4GOOD      ;EXPECT PSMW H AND BTS1 H TO BE SET
12685   035034  004737  011200               JSR     PC,READT4               ;READ AND CHECK VDAL REGISTER
12686   035040  001405                        BEQ     13$                     ;IF OK THEN CONTINUE
12687   035042                                 ERRDF   11,VDALRG,T4EROR        ;EDBRK H PROBABLY DIDN'T SET BRK H HIGH
12688   035042  104455                         TRAP    C$ERDF
12689   035044  000013                         .WORD   11
12690   035046  003710                         .WORD   VDALRG
12691   035050  006716                         .WORD   T4EROR
12692   035052                                 CKLOOP
12693   035052  104406                         TRAP    C$CLP1
12694
12695                                                ;SET THE SIGNAL FETCT H TO THE LOW STATE BY CLEARING VDAL7 H AND PULSE
12696                                                ;THE SIGNAL INVD L BY SETTING AND CLEARING THE SIGNAL VDAL2 H. A PULSE
12697                                                ;ON INVD L WILL CLEAR THE EDFET, PSMW AND BTFET FLIP-FLOPS.
12698
12699   035054  005037  002340       13$:       CLR     T4LOAD                  ;SETUP TO CLEAR ALL R/W BITS
12700   035060  004737  012706                  JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
12701
12702                                                ;SELECT THE STATE ANALYZER MODULE BY WRITING THE HIGH BYTE OF CONTROL
12703                                                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER.
12704
12705   035064  004737  012144                  JSR     PC,SLCTED               ;SELECT THE STATE ANALYZER MODULE
12706
12707                                                ;SET THE SIGNAL PDAL5 H TO THE LOW STATE BY CLEARING THE BIT IN
12708                                                ;CONTROL REGISTER 2'S PDAL REGISTER.  PDAL5 H ON A ZERO WILL PRESET
12709                                                ;ALL THE FUNCTION SELECT FLIP-FLOPS TO A ONE THUS SETTING ALL THE
12710                                                ;ZERO OUTPUTS OF THE FUNCTION SELECT FLIP-FLOP'S TO THE LOW STATE.
12711                                                ;WHEN FUSL2 FLIP-FLOP IS PRESET TO A ONE, THE SIGNALS FUSL2 H AND
12712                                                ;EDBRK H WILL BE SET TO THE LOW STATE.
12713
12714   035070  004537  012164                  JSR     R5,LDPDAL               ;LOAD AND CHECK PDAL REG WITH NEXT WORD
12715   035074  000004                          .WORD   PTER4                   ;SETUP TO READ FUSL F/F'S 3:0
12716
12717                                                ;READ FUNCTION SELECT FLIP-FLOP'S FUSL 3:0 VIA CONTROL REGISTER 6
12718                                                ;TO CHECK THAT THESE FLIP-FLOPS ARE PRESET TO A ONE.  WHEN THE FLIP-
12719                                                ;FLOPS ARE PRESET TO A ONE, THEY WILL BE READ AS ZEROES WHEN CONTROL
12720                                                ;REGISTER 6 IS READ.
12721
12722   035076  042737  040000  002316          BIC     #BIT14,E6LOAD           ;EXPECT FUSL2 TO BE A 0 WHEN READ
12723   035104  004737  011054                  JSR     PC,READE6               ;READ AND CHECK FUSL F/F'S 3:0
12724   035110  001405                          BEQ     14$                     ;IF OK THEN CONTINUE
12725   035112                                  ERRDF   8,FUSL30,E6ALLR         ;PDAL5 PROBABLY FAILED TO PRESET F/F'S
12726   035112  104455                          TRAP    C$ERDF
12727   035114  000010                          .WORD   8
12728   035116  003607                          .WORD   FUSL30
12729   035120  006226                          .WORD   E6ALLR
12730   035122                                  CKLOOP
12731   035122  104406                          TRAP    C$CLP1
12732
12733                                                ;SELECT THE TARGET EMULATOR MODULE BY WRITING THE HIGH BYTE OF CONTROL
12734                                                ;REGISTER 0 WITH THE USER DEFINED DEVICE NUMBER
12735
12736   035124  004737  012214       14$:       JSR     PC,SLCTTE               ;SELECT THE TARGET EMULATOR MODULE
```

N 3

HARDWARE TESTS MACY11 30A(1052) 16-JUN-82 13:46 PAGE 245
CVCDDB.P11   14-JUN-82 09:54   TEST 13: CHECK SA SIGNAL ''EDBRK H'' TO TE MODULE   SEQ 0245

```
12737
12738                                      ;READ CONTROL REGISTER 0'S GDAL REGISTER TO CHECK THAT THE SIGNAL
12739                                      ;EDBRK H IS READ AS A ZERO AFTER THE PROGRAM HAD PRESET THE STATE
12740                                      ;ANALYZERS FUNCTION SELECT FLIP-FLOP'S TO A ONE VIA PDAL5 H (0).
12741
12742  035130  042737  000020  002326      BIC      #EDBRK,TOGOOD        ;EXPECT EDBRK H TO BE A ZERO
12743  035136  004737  011114               JSR      PC,READTO           ;READ AND CHECK GDAL REGISTER
12744  035142  001404                       BEQ      15$                 ;IF OK THEN CONTINUE
12745  035144                               ERRDF    9,GDALRG,TOEROR     ;EDBRK H PROBABLY STILL SET HIGH
12746  035144  104455                       TRAP     C$ERDF
12747  035146  000011                       .WORD    9
12748  035150  003640                       .WORD    GDALRG
12749  035152  006666                       .WORD    TOEROR
12750  035154                       15$:    ENDSEG
12751  035154                       10000$:
12752  035154  104405                       TRAP     C$ESEG
12753
12754  035156                               ENDTST
12755  035156                       L40051:
12756  035156  104401                       TRAP     C$ETST
12757  035160                               ENDMOD
12758
```

```
12759                                        .TITLE PARAMETER CODING
12760                                        .SBTTL  HARDWARE PARAMETER CODING SECTION
12761
12762    035160                              BGNMOD
12763
12764                              ;++
12765                              ; THE HARDWARE PARAMETER CODING SECTION CONTAINS MACROS
12766                              ; THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
12767                              ; MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
12768                              ; INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
12769                              ; MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
12770                              ; WITH THE OPERATOR.
12771                              ;--
12772
12773    035160                              BGNHRD
12774    035160    000027                    .WORD L10052-L$HARD/2
12775    035162                    L$HARD::
12776
12777                              ;HARDWARE P-TABLE QUESTIONS
12778                              ;
12779                              ;        ASK FOR MDE/T-11 CSR ADDRESS
12780                              ;        ASK FOR MDE/T-11 VECTOR ADDRESS
12781                              ;        ASK FOR MDE/T-11 MEORY SIMULATOR DEVICE NUMBER
12782                              ;        ASK FOR MDE/T-11 STATE ANALYZER DEVICE NUMBER
12783                              ;        ASK FOR MDE/T-11 TARGET EMULATOR DEVICE NUMBER
12784                              ;
12785
12786    035162                              GPRMA    MSG1,0,0,160000,177770,YES
12787    035162    000031                    .WORD    T$CODE
12788    035164    035240                    .WORD    MSG1
12789    035166    160000                    .WORD    T$LOLIM
12790    035170    177770                    .WORD    T$HILIM
12791    035172                              GPRMA    MSG2,2,0,000370,000370,YES
12792    035172    001031                    .WORD    T$CODE
12793    035174    035254                    .WORD    MSG2
12794    035176    000370                    .WORD    T$LOLIM
12795    035200    000370                    .WORD    T$HILIM
12796    035202                              GPRMD    MSG3,4,0,177777,0,000017,YES
12797    035202    002032                    .WORD    T$CODE
12798    035204    035273                    .WORD    MSG3
12799    035206    177777                    .WORD    177777
12800    035210    000000                    .WORD    T$LOLIM
12801    035212    000017                    .WORD    T$HILIM
12802    035214                              GPRMD    MSG4,6,0,177777,0,000017,YES
12803    035214    003032                    .WORD    T$CODE
12804    035216    035336                    .WORD    MSG4
12805    035220    177777                    .WORD    177777
12806    035222    000000                    .WORD    T$LOLIM
12807    035224    000017                    .WORD    T$HILIM
12808    035226                              GPRMD    MSG5,10,0,177777,0,000017,YES
12809    035226    004032                    .WORD    T$CODE
12810    035230    035377                    .WORD    MSG5
12811    035232    177777                    .WORD    177777
12812    035234    000000                    .WORD    T$LOLIM
12813    035236    000017                    .WORD    T$HILIM
12814    035240                              ENDHRD
```

```
12815                                              .EVEN
12816   035240                              L10052:
12817
12818                                       ;
12819                                       ;HARDWARE P-TABLE MESSAGES
12820                                       ;
12821
12822   035240  051503  020122  042101      MSG1:   .ASCIZ  /CSR ADDRESS/
12823   035246  051104  051505  000123
12824   035254  042526  052103  051117      MSG2:   .ASCIZ  /VECTOR ADDRESS/
12825   035262  040440  042104  042522
12826   035270  051523     0C0
12827   035273     104  053105  041511      MSG3:   .ASCIZ  /DEVICE NUMBER FOR MEMORY SIMULATOR/
12828   035300  020105  052516  041115
12829   035306  051105  043040  051117
12830   035314  046440  046505  051117
12831   035322  020131  044523  052515
12832   035330  040514  047524  000122
12833   035336  042504  044526  042503      MSG4:   .ASCIZ  /DEVICE NUMBER FOR STATE ANALYZER/
12834   035344  047040  046525  042502
12835   035352  020122  047506  020122
12836   035360  052123  052101  020105
12837   035366  047101  046101  055131
12838   035374  051105     000
12839   035377     104  053105  041511      MSG5:   .ASCIZ  /DEVICE NUMBER FOR TARGET EMULATOR/
12840   035404  020105  052516  041115
12841   035412  051105  043040  051117
12842   035420  052040  051101  042507
12843   035426  020124  046505  046125
12844   035434  052101  051117     000
12845           035442                              .EVEN
12846
12847
```

```
12848                                    .SBTTL   SOFTWARE PARAMETER CODING SECTION
12849
12850
12851                            ;++
12852                            ; THE SOFTWARE PARAMETER CODING SECTION CONTAINS MACROS
12853                            ; THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
12854                            ; MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
12855                            ; INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
12856                            ; MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
12857                            ; WITH THE OPERATOR.
12858                            ;--
12859    035442                          BGNSFT
12860    035442  000000                  .WORD L10053-L$SOFT/2
12861    035444                  L$SOFT::
12862
12863
12864                                    .EVEN
12865
12866    035444                          ENDSFT
12867                                    .EVEN
12868    035444                  L10053:
12869
12870    035444                  $PATCH::
12871    035444  000010                  .BLKW   10
12872
12873    035464                          LASTAD
12874                                    .EVEN
12875    035464  035506                  .WORD T$FREE
12876    035466  000007                  .WORD T$SIZE
12877    035470                  L$LAST::
12878    035470                          ENDMOD
12879
12880    035470                          BGNSETUP        1.
12881    035470                          BGNPTAB
12882    035470  000000                  .WORD   0
12883    035472  000005                  .WORD   L10056-./2-1
12884    035474                  L10054:
12885    035474  163010                  .WORD   163010
12886    035476  000370                  .WORD   370
12887    035500  000000                  .WORD   0
12888    035502  000001                  .WORD   1
12889    035504  000002                  .WORD   2
12890    035506                          ENDPTAB
12891    035506                  L10056:
12892    035506                          ENDSETUP
12893            000001          .END
```

```
ADALRG  003664 G     2392#   3457    3467    4277    4287    9195    9716    9904
ADAL0 = 000001 G     1963#   3451    4271    4281
ADAL1 = 000002 G     1962#
ADAL10= 002000 G     1951#   4718    5136    5890    6454    7425    8598    9461    10125   10750   11276   11923   12581
ADAL11= 004000 G     1950#
ADAL12= 010000 G     1949#
ADAL13= 020000 G     1948#   9461    11576   11601   12224   12249
ADAL14= 040000 G     1946#   4718    5136    5890    6454    7425    8598    9710    10125   10750   11276   11923
ADAL15= 100000 G     1945#   9710    9898
ADAL2 = 000004 G     1961#
ADAL3 = 000010 G     1960#
ADAL4 = 000020 G     1958#   4718    5136    5890    6454    7425    8598    9461    10125   10750
ADAL5 = 000040 G     1956#
ADAL6 = 000100 G     1955#
ADAL7 = 000200 G     1954#   8598    9189
ADAL8 = 000400 G     1953#
ADAL9 = 001000 G     1952#   4718    5136    5890    6454    7425    8598    9461    10125   10750   11276   11923   12581
ADDRES= 000000 G     1920#   4807    5372    6129    6654    7626    8264    8687    10216   10839   11405   12054
ADDRRG  004144 G     2431#   4818    5389    6141    6665    7637    8276    8697    10229   10852   11418   12067
ADDR0 = 000001 G     2071#
ADDR1 = 000002 G     2070#
ADDR10= 002000 G     2061#
ADDR11= 004000 G     2060#
ADDR12= 010000 G     2059#
ADDR13= 020000 G     2058#
ADDR14= 040000 G     2057#
ADDR15= 100000 G     2056#   10223   10846
ADDR2 = 000004 G     2069#
ADDR3 = 000010 G     2068#
ADDR4 = 000020 G     2067#
ADDR5 = 000040 G     2066#
ADDR6 = 000100 G     2065#
ADDR7 = 000200 G     2064#
ADDR8 = 000400 G     2063#
ADDR9 = 001000 G     2062#
ADR   = 000020 G     1689#
ALPRNT  007032 G     2965    2995#
ASSEMB= 000010       1450
BIT0  = 000001 G     1662#   1736    1759    1780    1789    1833    1857    1914    1963    1984    2010    2032    2049
                     2071    3822    5062    5063    5064    5065    9145    9671
BIT00 = 000001 G     1651#   1662
BIT01 = 000002 G     1650#   1661
BIT02 = 000004 G     1649#   1660
BIT03 = 000010 G     1648#   1659
BIT04 = 000020 G     1647#   1658
BIT05 = 000040 G     1646#   1657
BIT06 = 000100 G     1645#   1656
BIT07 = 000200 G     1644#   1655
BIT08 = 000400 G     1643#   1654
BIT09 = 001000 G     1642#   1653
BIT1  = 000002 G     1661#   1734    1758    1779    1788    1831    1856    1913    1962    1983    2009    2031    2048
                     2070    8808    8920    9145
BIT10 = 002000 G     1641#   1723    1770    1812    1903    1951    1974    1995    2022    2061
BIT11 = 004000 G     1640#   1722    1769    1811    1902    1950    1973    1994    2020    2060
BIT12 = 010000 G     1639#   1768    1809    1900    1949    1972    1993    2019    2059    12534
BIT13 = 020000 G     1638#   1767    1808    1899    1948    1971    1992    2018    2058
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BIT14 = 040000 G    1637#   1766   1807   1898   1946   1970   1991   2017   2057   12556  12722
BIT15 = 100000 G    1636#   1713   1765   1801   1892   1945   1969   1990   2016   2056
BIT2  = 000004 G    1660#   1733   1751   1778   1787   1829   1855   1912   1961   1982   2006   2030   2047
                    2069   4113   9273   9394
BIT3  = 000010 G    1659#   1732   1750   1777   1786   1828   1854   1911   1960   1981   2005   2029   2046
                    2068   8808   8920   9394
BIT4  = 000020 G    1658#   1731   1776   1825   1849   1910   1958   1980   2004   2028   2045   2067   5063
                    5064
BIT5  = 000040 G    1657#   1730   1746   1775   1822   1847   1909   1956   1979   2003   2027   2044   2066
                    5062   5064
BIT6  = 000100 G    1656#   1729   1745   1774   1820   1845   1908   1955   1978   2002   2026   2043   2065
                    8808   9036   9273
BIT7  = 000200 G    1655#   1744   1773   1816   1843   1907   1954   1977   2001   2025   2042   2064   9145
                    9273
BIT8  = 000400 G    1654#   1725   1772   1814   1905   1953   1976   2000   2024   2063
BIT8H = 000010 G    1732#   6099   7949   8241
BIT9  = 001000 G    1653#   1724   1771   1813   1904   1952   1975   1996   2023   2062
BOE   = 000400 G    1693#
BRKRES 012766 G     4269#   4719   5137   5891   6455   7426   8599   9462   10126  10468  10624  10751  11065
                    11277  11924  12582
CDALRG 003010 G     2284#   3274   3293   3307   4965   5541   8787   8904   9643   12441  12515  12525  12639
CDAL0 = 000001 G    1833#
CDAL1 = 000002 G    1831#   12633
CDAL10= 002000 G    1812#
CDAL11= 004000 G    1811#
CDAL12= 010000 G    1809#
CDAL13= 020000 G    1808#
CDAL14= 040000 G    1807#
CDAL15= 100000 G    1801#   3286   3301   4419
CDAL2 = 000004 G    1829#
CDAL3 = 000010 G    1828#   4959   5535   8781   9637
CDAL4 = 000020 G    1825#
CDAL5 = 000040 G    1822#
CDAL6 = 000100 G    1820#   12509  12519
CDAL7 = 000200 G    1816#
CDAL8 = 000400 G    1814#
CDAL9 = 001000 G    1813#   4419
CKH   = 000100 G    1729#
CLRPSM 012706 G     4239#   4752   5172   5927   6490   7461   8633   8955   9540   10161  10644  10785  11098
                    11742  12391  12621  12700
CTLFDL 004106 G     2426#   9623   9869
CTSH  = 000002 G    1734#   4898   5342   6099   6630   6974   7601   7949   8241   10099  10724  11244  11891
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C$AUTO= 000061      1450#   4455
C$BRK = 000022      1450#
C$BSEG= 000004      1450#   3164   3257   3332   3674   3707   3728   3826   3897   3961   4012   4042   4062
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                    5873   5990   6026   6114   6437   7408   8582   9446   10057  10687  11124  11157  11257
                    11771  11804  11904  12421
C$BSUB= 000002      1450#
C$CEFG= 000045      1450#
C$CLCK= 000062      1450#
C$CLEA= 000012      1450#   4480
C$CLOS= 000035      1450#
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6267	6304	6483	6511	6535	6548	6577	6602	6622	6639	6668	6713	6732
6751	6775	6809	6840	6863	6874	6906	6926	6939	6955	6969	6983	7014
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7812	7835	7846	7878	7898	7911	7927	7942	7958	7989	8019	8035	8059
8102	8121	8140	8164	8182	8195	8211	8235	8250	8279	8303	8346	8364
8384	8407	8425	8439	8455	8518	8538	8626	8654	8678	8700	8714	8757
8770	8790	8817	8844	8874	8887	8907	8929	8946	8977	8998	9045	9074
9108	9121	9154	9183	9198	9236	9249	9282	9310	9357	9370	9483	9510
9532	9588	9603	9626	9646	9680	9702	9719	9743	9776	9806	9834	9849
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C$DCLN= 000044	1450#											
C$DODU= 000051	1450#											
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C$DU = 000053	1450#	4502										
C$EDIT= 000003	1450#	1512										
C$ERDF= 000055	1450#	3181	3201	3215	3233	3247	3272	3291	3305	3321	3348	3363	3379
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	3794	3839	3853	3870	3909	3927	3965	4017	4047	4068	4097	4118	4146
	4166	4194	4214	4245	4255	4275	4285	4740	4768	4792	4816	4867	4881
	4902	4921	4942	4963	4991	5026	5160	5188	5212	5225	5278	5303	5323
	5346	5387	5408	5456	5475	5494	5518	5539	5568	5597	5626	5658	5689
	5727	5765	5800	5915	5944	5968	5981	6034	6059	6076	6103	6139	6160
	6200	6219	6238	6262	6299	6334	6478	6506	6530	6543	6572	6597	6617
	6634	6663	6708	6727	6746	6770	6804	6835	6858	6869	6901	6921	6934
	6950	6964	6978	7009	7039	7055	7079	7122	7141	7160	7184	7199	7212
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	7680	7699	7718	7742	7776	7807	7830	7841	7873	7893	7906	7922	7937
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C$ESUB= 000003        1450#
C$ETST= 000001        1450#   4655   5069   5830   6365   7330   8552   9408  10000  10656  11104  11750  12399
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C$EXIT= 000032        1450#   4430   4472
C$GETB= 000026        1450#
C$GETW= 000027        1450#
C$GMAN= 000043        1450#
C$GPHR= 000042        1450#   4396
C$GPLO= 000030        1450#
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C$INIT= 000011        1450#   4438
C$INLP= 000020        1450#
C$MANI= 000050        1450#
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C$MSG = 000023        1450#   2565   2574   2583   2592   2602   2612   2621   2630   2639   2767   2776   2785
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C$OPEN= 000034        1450#
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C$QIO = 000377        1450#
C$RDBU= 000007        1450#
C$REFG= 000047        1450#   4360   4365   4370   4384   4390
C$RESE= 000033        1450#   4374   4469
C$REVI= 000003        1450#   1511
C$RFLA= 000021        1450#
C$RPT = 000025        1450#   4331
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C$SPRI= 000041        1450#   4426   4467  10061  10588
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DIAGMC= 000000        1450
EDBRK = 000020 G      1939#  12654  12742
EDDEV   002222 G      2102#   3265   3268   3285
EDTYPE  002224 G      2103#   3287
EF.CON= 000036 G      1669#   4389
EF.NEW= 000035 G      1670#   4383
EF.PWR= 000034 G      1671#   4369
EF.RES= 000037 G      1668#   4364
EF.STA= 000040 G      1667#   4359
EIDAL = 000006 G      1929#   5669   6815   7066   7787   8041   8285  11582  11701  12230  12350
EMSGR0  004770 G      2513#   2561   2617   2763   2928
EMSGR2  005020 G      2517#   2570   2597   2626   2772   2937
EMSGR4  005050 G      2521#   2579   2607   2781   2946
EMSGR6  005100 G      2525#   2588   2635   2790   2799   2955   2964
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                          10826    11392    12041
EODAL = 000007 G          1930#     5640     6278     6786     7758    11536    12184
ERRBLK  002202 G          2086#
ERRMSG  002200 G          2085#
ERRNBR  002176 G          2084#
ERRTYP  002174 G          2083#
ESRH  = 000040 G          1746#     3786     3787     5298     5514     6054     6258     6592     6766     7180     7563     7738     8155
                          8398    10347    10968    11214    11219    11861    11866
EVL   = 000004 G          1687#
E$END = 002100            1450#
E$LOAD= 000035            1450#     1535
EOEROR  006146 G          2761#     3275     3294     3308     4966     5542     8788     8905     9644    12442    12516    12526    12640
EOGOOD  002274 G          2139#     2828     2832     3287*    3572*    3575
EOLOAD  002272 G          2138#     2828     2833     2842     3265*    3266*    3285*    3286*    3301*    3572     3573     3952     4959*
                          5535*    8781*    9637*   12435*   12509*   12519*   12633*
EOREAD  002276 G          2140#     2831     2841     3574*    3575
EO26ER  006212 G          2788#     4994     5029     5571     5600     5629     5768     5803     8815     8927     9043     9152     9280
                          9401     9678     9804     9983    12472
E2EROR  006162 G          2770#     3324     3968
E2LOAD  002300 G          2142#     2860     3317*    3581     3584     3959*
E2READ  002302 G          2143#     2859     3582*    3583*    3584
E4BAD   002314 G          2149#     2879     2889     3597*    3598*    3599
E4EROR  006176 G          2779#    12489    12541
E4GOOD  002306 G          2146#     2876     2880     3590*    3591*    3594*    3599
E4LOAD  002304 G          2145#     2876     2881     2890     3590     3594     3595    12481*
E4MASK  002310 G          2147#     3325*    3598    12482*   12534*
E4READ  002312 G          2148#     3596     3597
E6ALLR  006226 G          2797#    12564    12729
E6LOAD  002316 G          2151#     2908     3605     3608     4987*    5021*    5563*    5592*    5622*    5760*    5795*    8808*    8920*
                          9036*    9145*    9273*    9394*    9670*    9671*    9797*    9976*   12464*   12556*   12722*
E6MASK  002320 G          2152#     3326*    3607     4701*    5022*    5119*    5564*    5593*    5621*    5761*    5796*    8583*    8807*
                         12465*   12557*
E6READ  002322 G          2153#     2907     3606*    3607*    3608
FDAL  = 000002 G          1924#     4782     5202     5958     6520     6995     7491     7970     8663     9491     9594     9840    10191
                         10814    11374    12023
FDALRG  004024 G          2416#
FDAL0 = 000001 G          2049#     4788     5208     5964     6526     7005     7497     7980     8669     9501     9693    10197    10820
FDAL1 = 000002 G          2048#     7005     7980
FDAL2 = 000004 G          2047#
FDAL3 = 000010 G          2046#
FDAL4 = 000020 G          2045#
FDAL5 = 000040 G          2044#
FDAL6 = 000100 G          2043#
FDAL7 = 000200 G          2042#
FDEIDL  004647 G          2490#    11597    12245
FDEODL  004607 G          2484#    11550    12198
FDTDEI  004707 G          2496#    11718    12367
FJADR = 000001 G          1922#
FJADRG  004175 G          2436#
FSLGB   005234 G          2547#     2665     2695     2743     2834     2882     3015     3063
FSLR    005200 G          2542#     2674     2704     2722     2752     2843     2861     2891     2909     3024     3042     3072     3091
FUSL30  003607 G          2369#    12563    12728
FUSL7   003121 G          2308#    12540
F$AU  = 000015            1450#     4512     4523
F$AUTO= 000020            1450#     4450     4454
F$BGN = 000040            1450#     1457     1620     1625     2559     2568     2577     2586     2595     2605     2615     2624     2633
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                        4464    4472    4490    4496    4512    4518    4527    4533    4647    4654    4693    4699    5068
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F$CLEA= 000007          1450#   4464    4479
F$DU  = 000016          1450#   4490    4501
F$END = 000041          1450#   1457    1620    1625    2566    2575    2584    2593    2603    2613    2622    2631    2640
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                        5113    5232    5353    5807    5829    5831    5869    5988    6110    6341    6364    6366    6399
                        7258    7329    7331    7371    8482    8551    8553    8579    9405    9407    9409    9439    9987
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F$HARD= 000004          1450#   12774   12815
F$HW  = 000013          1450#   1587    1599
F$INIT= 000006          1450#   4357    4437
F$JMP = 000050          1450#   4323    4430    4472    4494    4516
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F$MSG = 000011          1450#   2559    2564    2568    2573    2577    2582    2586    2591    2595    2601    2605    2611
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F$PROT= 000021          1450#   4341    4348
F$PWR = 000017          1450#
F$RPT = 000012          1450#   4319    4330
F$SEG = 000003          1450#   3164    3253    3257    3328    3332    3512    3674    3695    3707    3728    3799    3811
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                        4102    4112    4123    4141    4151    4160    4171    4189    4199    4208    4219    4240    4260
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F$SOFT= 000005          1450#   12860   12867
F$SRV = 000010          1450#   4297    4301
F$SUB = 000002          1450#
F$SW  = 000014          1450#   1611    1617
F$TEST= 000001          1450#   4648    4654    4694    5068    5114    5829    5870    6364    6400    7329    7372    8551
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GDALRG  003640 G        2385#   3350    3365    3381    3418    3483    4019    4869    8767    8884    8943    9118    9246
                        9367    9600    9846   10294   10393   10459   10478   10531   10577   10616   10635   10915   11014
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GDAL0 = 000001 G        1914#   1922    1926    1928    1930    3375
GDAL1 = 000002 G        1913#   1924    1926    1929    1930    3375
GDAL10= 002000 G        1903#
GDAL11= 004000 G        1902#
GDAL12= 010000 G        1900#
GDAL13= 020000 G        1899#
GDAL14= 040000 G        1898#
GDAL15= 100000 G        1892#   3358    4423
```

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GDAL2 = 000004 G    1912#   1927    1928    1929    1930    3412
GDAL3 = 000010 G    1911#   10570   10571
GDAL4 = 000020 G    1910#   1939
GDAL5 = 000040 G    1909#   1938
GDAL6 = 000100 G    1908#   1937
GDAL7 = 000200 G    1907#   1936
GDAL8 = 000400 G    1905#
GDAL9 = 001000 G    1904#
G$CNTO= 000200      1450#
G$DELM= 000372      1450#
G$DISP= 000003      1450#
G$EXCP= 000400      1450#
G$HILI= 000002      1450#
G$LOLI= 000001      1450#
G$NO  = 000000      1450#
G$OFFS= 000400      1450#   12787   12792   12797   12803   12809
G$OFSI= 000376      1450#   12787   12792   12797   12803   12809
G$PRMA= 000001      1450#   12787   12792
G$PRMD= 000002      1450#   12797   12803   12809
G$PRML= 000000      1450#
G$RADA= 000140      1450#
G$RADB= 000000      1450#
G$RADD= 000040      1450#
G$RADL= 000120      1450#
G$RADO= 000020      1450#   12787   12792   12797   12803   12809
G$XFER= 000004      1450#
G$YES = 000010      1450#   12787   12792   12797   12803   12809
HDAL  = 000003 G    1926#   4726    4828    5144    5399    5701    5898    6151    6311    6462    6675    6881    7020
                    7091    7433    7647    7853    7995    8066    8310    8605    8720    9517    9726    9914    10133
                    10252   10757   10874   11284   11441   11560   11646   11728   11931   12090   12208   12294   12377
                    12589
HDALRG  003756 G    2409#   3402    4049    4070    4099    4120    4148    4168    4196    4216    4742    5162    5410
                    5917    6162    6480    7041    7451    8016    8623    8841    8974    9071    9180    9307    9529
                    9740    9926    10151   10775   11308   11665   11956   12314   12610
HDAL0 = 000001 G    2010#
HDAL1 = 000002 G    2009#
HDAL10= 002000 G    1995#
HDAL11= 004000 G    1994#   5048    5049
HDAL12= 010000 G    1993#   4043    4064    11562   11651   12210   12299
HDAL13= 020000 G    1992#   4093    4114
HDAL14= 040000 G    1991#   5047    5049
HDAL15= 100000 G    1990#   4142    4162    11651   11730   12299   12379
HDAL2 = 000004 G    2006#   3395    4043    4063    4093    4142    4161    4190    4209    4735    4852    5156    5404
                    5712    5910    6156    6318    6474    6676    6888    7035    7092    7445    7648    7860    8010
                    8067    8311    8617    8739    8835    8968    9065    9174    9301    9523    9734    9920    10145
                    10254   10769   10875   11302   11443   11562   11651   11730   11950   12092   12210   12299   12379
                    12604
HDAL3 = 000010 G    2005#   5156    5404    5712    5910    6156    6318    6474    6676    6888    7445    7648    7860
                    8617    8739    8835    8968    9065    9174    9301    9734    10145   10254   11659   11730   12308
                    12379
HDAL4 = 000020 G    2004#   5156    5404    5712    6318    6474    6676    6888    7445    7648    7860    9734    10145
                    10254   11659   11730   11950   12092   12210   12299   12307
HDAL5 = 000040 G    2003#   7035    7092    8010    8067    8311    8617    8739    8968    9174
HDAL6 = 000100 G    2002#   7035    7092    8010    8067    8311    9065    9174    11302   11443   11562   11651   11950
                    12092   12210   12299
HDAL7 = 000200 G    2001#   4190    4210
```

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HDAL8 = 000400 G    2000#
HDAL9 = 001000 G    1996#    4735     4852     5156     5404     5712     5910     6156     6318     6474     6676     6888     7035
                    7092     7445     7648     7860     8010     8067     8311     8617     8739     8835     8968     9065     9174
                    9301    10145    10254    10769    10875    11302    11443    11562    11651    11730    11950    12092    12210
                   12299    12379
HELP  = 000000      1448#    1450     1465     1553     1577     1597     1615     1620#    1623     1631     2080     2191     2507
                    2915     2916     2934     3108     3114     3117     3127     3130     3138     3147     3151     3159     3160
                    4308#    4321     4326     4349     4428     4433     4452     4470     4475     4492     4497     4514     4519
                    4529#    4644     4645     4650     4651    12757    12760#   12814    12847    12863    12869    12873    12880
HOE   = 100000 G    1700#
IBE   = 010000 G    1697#
IDH   = 100000 G    1713#    3196     3211     4414
IDU   = 000040 G    1690#
IER   = 020000 G    1698#
INITED  007666 G    3256#
INITMD  007440 G    3162#    4648     4694     5114     5870     6400     7372     8580     9441    10054    10685    11121    11768
                   12418
INITMS  007440 G    3163#
INITTE  010060 G    3331#
INTSRV  013046 G    4297#   10560
ISR   = 000100 G    1691#
IXE   = 004000 G    1696#
I$AU  = 000041      1450#    4512#    4525#
I$AUTO= 000041      1450#    4450#    4456#
I$CLN = 000041      1450#    4464#    4472#    4481#
I$DU  = 000041      1450#    4490#    4503#
I$HRD = 000041     12774#   12817#
I$INIT= 000041      1450#    4357#    4430     4439#
I$MOD = 000041      1450#    1457#    1620#    1625#    4307#    4312#    4527#    4533#   12758#   12763#   12879#
I$MSG = 000041      1450#    2559#    2566#    2568#    2575#    2577#    2584#    2586#    2593#    2595#    2603#    2605#    2613#
                    2615#    2622#    2624#    2631#    2633#    2640#    2761#    2768#    2770#    2777#    2779#    2786#    2788#
                    2795#    2797#    2804#    2926#    2933#    2935#    2942#    2944#    2951#    2953#    2960#    2962#    2969#
I$PROT= 000040      1450#    4341#
I$PTAB= 000041      1450#   12882#   12891#
I$PWR = 000041      1450#
I$RPT = 000041      1450#    4319#    4332#
I$SEG = 000041      1450#    3164#    3255#    3257#    3330#    3332#    3514#    3674#    3697#    3707#    3728#    3813#    3826#
                    3877#    3897#    3934#    3961#    3972#    4012#    4024#    4042#    4054#    4062#    4075#    4092#    4104#
                    4112#    4125#    4141#    4153#    4160#    4173#    4189#    4201#    4208#    4221#    4240#    4262#    4270#
                    4292#    4647     4693     4699#    5033#    5113     5117#    5232#    5234#    5269#    5353#    5357#    5807#
                    5869     5873#    5988#    5990#    6026#    6110#    6114#    6341#    6399     6437#    7258#    7371     7408#
                    8482#    8579     8582#    9405#    9439     9446#    9987#   10053    10057#   10653#   10684    10687#   11102#
                   11119    11124#   11157#   11255#   11257#   11747#   11766    11771#   11804#   11902#   11904#   12396#   12416
                   12421#   12753#
I$SETU= 000041      1450#   12881#   12882    12893#
I$SFT = 000041     12860#   12869#
I$SRV = 000041      1450#    4297#    4305#
I$SUB = 000041      1450#    4647     4693     5113     5869     6399     7371     8579     9439    10053    10684    11119    11766
                   12416
I$TST = 000041      1450#    4647#    4654#    4656#    4693#    5068#    5070#    5113#    5829#    5831#    5869#    6364#    6366#
                    6399#    7329#    7331#    7371#    8551#    8553#    8579#    9407#    9409#    9439#    9999#   10001#   10053#
                   10655#   10657#   10684#   11103#   11105#   11119#   11749#   11751#   11766#   12398#   12400#   12416#   12755#
                   12757#
J$JMP = 000107      1450#    4323     4494     4516
LDPDAL  012764 G    3959#    4973     5001     5549     5578     5613     5742     5777     8795     9651    12453    12497    12549
                   12714
```

```
LDRDAR  010764 G    3590#
LDRDE0  010700 G    3269    3302    3572#   4960    5536    8782    9638    12436   12510   12520   12634
LDRDE2  010732 G    3318    3581#   3962
LDRDE4  011000 G    3594#   12483
LDRDE6  011046 G    3605#   5623    12466
LDRDS0  010506 G    3178    3212    3527#   3677    3687    4899    5343    6100    6631    6918    6975    7196    7602
                    7890    7950    8174    8242    8417    10100   10725   11245   11892
LDRDS2  010546 G    3230    3537#   3738    3836    3906    11166   11813
LDRDS4  010606 G    3244    3547#   3751    3850    5275    6031    6569    7255    7540    8510    11179   11826
LDRDS6  010632 G    3555#   3773    3867    5320    6073    6614    6961    7585    7934    11201   11848
LDRDT0  011100 G    3345    3376    3413    3478    3620#   4014    9595    9841    12590
LDRDT2  011140 G    3452    3462    3630#   4272    4282    9190    9711    9899
LDRDT4  011164 G    3494    3504    3638#   4242    4252    7052    8027    8706
LDRDT6  011216 G    3397    3431    3647#   4044    4065    4094    4115    4143    4163    4191    4211    4737    4765
                    4789    4813    5157    5185    5209    5384    5405    5912    5941    5965    6136    6157    6475
                    6503    6527    6660    7006    7036    7446    7474    7498    7632    7981    8011    8271    8618
                    8646    8670    8692    8836    8969    9066    9175    9302    9475    9502    9524    9694    9735
                    9881    9921    10146   10174   10198   10224   10770   10797   10821   10847   11303   11357   11413
                    11660   11951   12006   12062   12309   12605
LDRD0E  010706 G    3288    3573#
LDRD0S  010514 G    3198    3528#
LDRD0T  011106 G    3360    3621#   10572
LDRD2S  010554 G    3538#   5300    6056    6594    7565
LDRD4E  011006 G    3592    3595#
LDRD4T  011172 G    3639#   6855    6866    7827    7838    10491   11325   11336   11620   11631   11676   11973   11984
                    12268   12279   12325
LDRD6S  010640 G    3556#   3924
LOE   = 040000 G    1699#
LOT   = 000010 G    1688#
L$ACP   002110 G    1542#
L$APT   002036 G    1500#
L$AU    013372 G    4512#
L$AUT   002070 G    1526#
L$AUTO  013344 G    1543    4450#
L$CCP   002106 G    1540#
L$CLEA  013346 G    1541    4464#
L$CO    002032 G    1496#
L$DEPO  002011 G    1478#
L$DESC  002366 G    1533    2195#
L$DESP  002076 G    1532#
L$DEVP  002060 G    1518#
L$DISP  002124 G    1503    1562#
L$DLY   002116 G    1548#
L$DTP   002040 G    1502#
L$DTYP  002034 G    1498#
L$DU    013364 G    4490#
L$DUT   002072 G    1528#
L$DVTY  002354 G    1519    2186#
L$EF    002052 G    1513#
L$ENVI  002044 G    1506#
L$ERRT  002174 G    2082#
L$ETP   002102 G    1536#
L$EXP1  002046 G    1508#
L$EXP4  002064 G    1522#
L$EXP5  002066 G    1524#
L$HARD  035162 G    1485    12774   12775#
```

```
L$HIME   002120 G       1550#
L$HPCP   002016 G       1484#
L$HPTP   002022 G       1488#
L$HW     002160 G       1489     1587     1588#
L$ICP    002104 G       1538#
L$INIT   013112 G       1539     4357#
L$LADP   002026 G       1492#
L$LAST   035470 G       1493    12877#   12893
L$LOAD   002100 G       1534#
L$LUN    002074 G       1530#
L$MREV   002050 G       1510#
L$NAME   002000 G       1467#
L$PRIO   002042 G       1504#
L$PROT   013104 G       1545     4341#
L$PRT    002112 G       1544#
L$REPP   002062 G       1520#
L$REV    002010 G       1476#
L$RPT    013076 G       4319#
L$SOFT   035444 G      12860    12861#
L$SPC    002056 G       1516#
L$SPCP   002020 G       1486#
L$SPTP   002024 G       1490#
L$STA    002030 G       1494#
L$SW     002174 G       1611     1612#
L$TEST   002114 G       1546#
L$TIML   002014 G       1482#
L$UNIT   002012 G       1480#
L10000   002172         1587     1599#
L10001   002174         1611     1617#
L10002   005320         2564#
L10003   005334         2573#
L10004   005350         2582#
L10005   005364         2591#
L10006   005404         2601#
L10007   005424         2611#
L10010   005440         2620#
L10011   005454         2629#
L10012   005470         2638#
L10013   006160         2766#
L10014   006174         2775#
L10015   006210         2784#
L10016   006224         2793#
L10017   006240         2802#
L10020   006700         2931#
L10021   006714         2940#
L10022   006730         2949#
L10023   006744         2958#
L10024   006760         2967#
L10025   013060         4301#
L10026   013102         4324     4330#
L10030   013342         4431     4437#
L10031   013344         4454#
L10032   013362         4473     4479#
L10033   013370         4495     4501#
L10034   013376         4517     4523#
L10035   013404         4654#
```

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L10036  014264        5068#
L10037  015666        5829#
L10040  016766        6364#
L10041  021130        7329#
L10042  023750        8551#
L10043  025426        9407#
L10044  026610        9999#
L10045  030114       10655#
L10046  031070       11103#
L10047  032602       11749#
L10050  034324       12398#
L10051  035156       12755#
L10052  035240       12774   12816#
L10053  035444       12860   12868#
L10054  035474       12884#
L10056  035506       12883   12891#
MEMBRK= 000040 G      1938#   3342   10387   10472   10525   10629   11008   11069
MODE  = 000004 G      1927#   4759    5179    5934    6497    7468    8639    9469   10168   10791   11351   11999
MODREG  004002 G      2413#   3436    4770    5190    5946    6508    7479    8651    9480   10179   10802   11362   12011
MPH   = 000004 G      1733#   3724    6562    6917    7195    7533    7889    8173    8416   11141   11788
MPINH = 000001 G      1789#   3767   11195   11842
MPRAM   011356 G      3706#   5249    6005    6415    7387   10076   10702
MR0   = 000001 G      2032'
MR1   = 000002 G      2031.
MR10  = 002000 G      2022#
MR11  = 004000 G      2020#   5940    8645   12005
MR12  = 010000 G      2019#
MR13  = 020000 G      2018#
MR14  = 040000 G      2017#
MR15  = 100000 G      2016.#
MR2   = 000004 G      2030.
MR3   = 000010 G      2029#
MR4   = 000020 G      2028#
MR5   = 000040 G      2027#
MR6   = 000100 G      2026#
MR7   = 000200 G      2025#
MR8   = 000400 G      2024#
MR9   = 001000 G      2023#
MSADRG  002510 G      2233#   3249    3756    3855    5280    6036    6574    6936    7214    7290    7545    7908    8192
                      8436    8515   11184   11502   11831   12151
MSAD0 = 000001 G      1780#
MSAD1 = 000002 G      1779#
MSAD10= 002000 G      1770#
MSAD11= 004000 G      1769#
MSAD12= 010000 G      1768#
MSAD13= 020000 G      1767#   3880    3882    7264    7315    8484    8541
MSAD14= 040000 G      1766#
MSAD15= 100000 G      1765#  10324   10945
MSAD16= 000001 G      1759#   3768    5055    5056   11196   11843
MSAD17= 000002 G      1758#   3768    5054    5056   11196   11843
MSAD2 = 000004 G      1778#
MSAD3 = 000010 G      1777#
MSAD4 = 000020 G      1776#
MSAD5 = 000040 G      1775#
MSAD6 = 000100 G      1774#
MSAD7 = 000200 G      1773#
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MSAD8 = 000400 G      1772#    3804    11233    11880
MSAD9 = 001000 G      1771#
MSBRKH= 000200 G      1744#   10347    10427    10968    11046
MSDEV   002216 G      2099#    3173     3177     3195
MSEDDE  003423 G      2348#    5767
MSEL0 = 000004 G      1751#    3807     3834     3894     3938     4936     5511     6255     6763     7177     7735     8152     8395
                     11236    11512    11883    12161
MSEL1 = 000010 G      1750#    3710     3894     4936     5511     6255     6763     7177     7735     8152     8395    11153    11512
                     11513    11800    12161    12162
MSGMP   002603 G      2249#    3778    11206    11853
MSGMPL  002460 G      2224#    3796    11225    11872
MSGMSR  002745 G      2267#    5325     6078     6619     6966     7253     7310     7590     7939     8232     8477     8535
MSGMS0  002641 G      2255#    3872
MSGMS1  002703 G      2261#    3929
MSG1    035240       12788    12822#
MSG2    035254       12793    12824#
MSG3    035273       12798    12827#
MSG4    035336       12804    12833#
MSG5    035377       12810    12839#
MSRAM0  011642 G      3822#    5257     6013     6423     7395    10084    10709
MSRAM1  012012 G      3891#    5264     6020     6430     7402    10091    10716
MSRSTH  011270 G      3673#    3725     6563     7534    10422    11042    11142    11789
MSTEDE  004243 G      2443#    5660     6301     6806     7778
MSTEEI  004331 G      2453#    5691     6837     7809
MSTETD  004422 G      2463#    7081     8056     8300
MSTYPE  002220        2100#    3197
MUTB  = 000010 G      1786#    3767    11195    11200    11842    11847
NOINT   004511 G      2473#   10602
ONEFIL= 000001           1#    1446     1448#    1451     1620#    1622     4308#    4310     4528     4529#    4531    12759    12760#
                     12761
ORADER  003547 G      2363#   12471
ORDATA  003057 G      2302#   12488
O$APTS= 000000        1450#    1494
O$AU  = 000000        1450#    1526
O$BGNR= 000000        1450#    1520
O$BGNS= 000000        1450#    1486
O$DU  = 000000        1450#    1528
O$ERRT= 000000        1450#    1536
O$GNSW= 000000        1450#    1490
O$POIN= 000001        1450#    1464#    1552
O$SETU= 000001        1450#    1464#    1480    12875
PDALRG  003034 G      2293#    3323     3967
PDAL0 = 000001 G      1857#    1864     1866     1868     1870     1872     1874     1876     1878
PDAL1 = 000002 G      1856#    1865     1866     1869     1870     1873     1874     1877     1878
PDAL2 = 000004 G      1855#    1867     1868     1869     1870     1875     1876     1877     1878
PDAL3 = 000010 G      1854#    1871     1872     1873     1874     1875     1876     1877     1878
PDAL4 = 000020 G      1849#
PDAL5 = 000040 G      1847#   12498    12550
PDAL6 = 000100 G      1845#    5614
PDAL7 = 000200 G      1843#
PNT   = 001000 G      1694#
PRI   = 002000 G      1695#
PRI00 = 000000 G      1683#   10587
PRI01 = 000040 G      1682#
PRI02 = 000100 G      1681#
PRI03 = 000140 G      1680#
```

```
PRIO4 = 000200 G        1679#
PRIO5 = 000240 G        1678#
PRIO6 = 000300 G        1677#
PRIO7 = 000340 G        1505     1676#    4303     4425     4466     10060    10559
PRNTAL  005472 G        2618     2627     2636     2645#
PRNTAR  006260 G        2782     2800     2814#
PRNTBS  006762 G        2560     2569     2578     2587     2596     2606     2616     2625     2634     2762     2771     2780     2789
                        2798     2927     2936     2945     2954     2963     2972#
PRNTE0  006302 G        2764     2807     2814     2822#
PRNTE2  006422 G        2773     2808     2815     2852#
PRNTE4  006474 G        2816     2870#
PRNTE6  006614 G        2809     2817     2900#
PRNTS0  005514 G        2562     2598     2608     2645     2653#
PRNTS2  005634 G        2571     2599     2646     2683#
PRNTS4  005754 G        2580     2609     2647     2713#
PRNTS6  006026 G        2589     2648     2731#
PRNTT0  007054 G        2929     2982     2988     2995     3003#
PRNTT2  007174 G        2938     2989     2996     3033#
PRNTT4  007246 G        2947     2997     3051#
PRNTT6  007366 G        2983     2990     2998     3082#
PRO26E  006242 G        2791     2807#
PRO26T  007014 G        2988#
PRO6T   007002 G        2956     2982#
PTER0 = 000000 G        1863#    5614     5778
PTER1 = 000001 G        1864#    4974     5550
PTER10= 000012 G        1873#
PTER11= 000013 G        1874#
PTER12= 000014 G        1875#
PTER13= 000015 G        1876#
PTER14= 000016 G        1877#
PTER15= 000017 G        1878#    12454    12498
PTER2 = 000002 G        1865#    5743
PTER3 = 000003 G        1866#    5002     5579     8796     9652
PTER4 = 000004 G        1867#    12550    12715
PTER5 = 000005 G        1868#
PTER6 = 000006 G        1869#
PTER7 = 000007 G        1870#
PTER8 = 000010 G        1871#
PTER9 = 000011 G        1872#
RDEH  = 000004 G        1787#    3772     3788     11200    11216    11847    11863
RDVH  = 000020 G        1731#    3676     10360
READE0  010714 G        3574#    8899
READE2  010740 G        3582#
READE4  011014 G        3596#    12535
READE6  011054 G        3606#    4988     5023     5565     5594     5762     5797     8809     8921     9037     9146     9274     9395
                        9672     9798     9977     12558    12723
READS0  010522 G        3529#    5472     6216     6724     7138     7696     8113     8356     10361    10982    11482    12131
READS2  010562 G        3539#    3791     4939     5515     6259     6767     6947     7181     7225     7739     7919     8156     8203
                        8399     8447     10348    10428    10969    11047    11220    11515    11867    12164
READS4  010614 G        3548#    4918     5491     6235     6743     6931     7157     7209     7715     7903     8132     8187     8376
                        8431     10325    10946    11497    12146
READS6  010646 G        3557#    7248     7305     8227     8472     8530
READT0  011114 G        3622#    4864     8762     8879     8938     9113     9241     9362     10289    10388    10454    10473    10526
                        10630    10910    11009    11070    12655    12743
READT2  011146 G        3631#
READT4  011200 G        3640#    4878     5222     5453     5724     5978     6197     6331     6540     6705     6898     7119     7511
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E 5

PARAMETER CODING   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 263
CVCDDB.P11   14-JUN-82 09:54   CROSS REFERENCE TABLE -- USER SYMBOLS   SEQ 0262

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READT6  011224 G    3648#   5655    5686    6296    6801    6832    7076    7773    7804    8051    8295    9618    9864
                   11387   11545   11592   11713   12036   12193   12240   12362
REG0    002204 G    2092#   3176    3267    3343    3528*   3529    3573*   3574    3621*   3622    3663    3951    3984
                    4298    4400
REG0EQ  005130 G    2529#   2654    2823    3004
REG2    002206 G    2093#   3538*   3539    3581*   3582    3630*   3631   11576*  11601*  12224*  12249*
REG2EQ  005142 G    2531#   2684    2853    3034
REG4    002210 G    2094#   3547*   3548    3595*   3596    3639*   3640
REG4EQ  005154 G    2533#   2714    2871    3052
REG6    002212 G    2095#   3556*   3557    3605*   3606    3647*   3648    9610*   9856*  11386*  12035*
REG6EQ  005166 G    2535#   2732    2901    3083
RSTH  = 000001 G    1736#   3675    3686    3724   11141   11788
SELTER  012234 G    4011#   4725    4758    4781    4806    4827    5143    5178    5201    5371    5398    5639    5668
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                    6785    6814    6880    6994    7019    7065    7090    7432    7467    7490    7625    7646    7757
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                    8719    9468    9490    9516    9725    9913   10132   10167   10190   10215   10251   10756   10790
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                   11727   11930   11998   12022   12053   12089   12183   12207   12229   12293   12349   12376
SFPTBL  002174 G    1613#
SIG10H= 002000 G    1723#
SIG11H= 004000 G    1722#
SIG8H = 000400 G    1725#   4414
SIG9H = 001000 G    1724#
SLCTED  012144 G    3950#   4952    5528    5737    8775    8892    9011    9126    9254    9375    9631    9781    9960
                   12426   12626   12705
SLCTMS  011250 G    3662#   4891    5239    5466    5995    6210    6405    6553    6718    6911    7132    7377    7524
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                   12125
SLCTTE  012214 G    3983#   4706    5124    5362    5634    5878    6119    6272    6442    6644    6780    6988    7413
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SSBRK = 000200 G    1936#   3342
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PARAMETER CODING   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 264
CVCDDB.P11   14-JUN-82 09:54   CROSS REFERENCE TABLE -- USER SYMBOLS

F 5

SEQ 0263

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G 5

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PARAMETER CODING   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 266
CVCDDB.P11   14-JUN-82 09:54   CROSS REFERENCE TABLE -- USER SYMBOLS   SEQ 0265

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7927	7928	7937	7938	7939	7940	7941	7942	7943	7953	7954	7955	7956
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8159	8160	8161	8162	8163	8164	8165	8177	8178	8179	8180	8181	8182
8183	8190	8191	8192	8193	8194	8195	8196	8206	8207	8208	8209	8210
8211	8212	8230	8231	8232	8233	8234	8235	8236	8245	8246	8247	8248
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8301	8302	8303	8304	8341	8342	8343	8344	8345	8346	8347	8359	8360
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8434	8435	8436	8437	8438	8439	8440	8450	8451	8452	8453	8454	8455
8456	8475	8476	8477	8478	8479	8481	8482	8513	8514	8515	8516	8517
8518	8519	8533	8534	8535	8536	8537	8538	8539	8552	8553	8582	8583
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8788	8789	8790	8791	8812	8813	8814	8815	8816	8817	8818	8839	8840
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PARAMETER CODING   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 267
CVCDDB.P11   14-JUN-82 09:54   CROSS REFERENCE TABLE -- USER SYMBOLS   SEQ 0266

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12564	12565	12566	12567	12593	12594	12595	12596	12597	12598	12599	12608	12609
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	2776	2784	2785	2793	2794	2802	2803	2931	2932	2940	2941	2949	2950
	2958	2959	2967	2968	3253	3254	3328	3329	3512	3513	3695	3696	3799

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4073	4074	4102	4103	4123	4124	4151	4152	4171	4172	4199	4200	4219
4220	4260	4261	4290	4291	4301	4302	4330	4331	4437	4438	4454	4455
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8552	9403	9404	9407	9408	9985	9986	9999	10000	10651	10652	10655	10656
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5117#	5234#	5269#	5357#	5830#	5873#	5990#	6026#	6114#	6365#	6437#	7330#	7408#
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11771#	11804#	11904#	12399#	12421#	12756#	12817#	12869#					

SOALLR 005426 G
2615#											

SOEROR 005306 G
2559#	3184	3204	3218	3683	3693	4905	5349	5478	6·06	6222	6637	6730
6924	6981	7144	7202	7608	7702	7896	7956	8119	8·80	8248	8362	8423
10106	10367	10731	10988	11251	11488	11898	12137					

SOGOOD 002236 G
2116#	2659	2663	3197*	3527*	3531	10360*	10981*					

SOLOAD 002234 G
2115#	2659	2664	2673	3173*	3174*	3195*	3196*	3211*	3527	3528	3664	3675*
3686*	3724*	4898*	5342*	6099*	6562*	6630*	6917*	6974*	7195*	7533*	7601*	7889*
7949*	8173*	8241*	8416*	10099*	10724*	11141*	11244*	11788*	11891*			

SOMASK 002240 G
2117#	3175*	3530	3676*									

SOREAD 002242 G
| 2118# | 2662 | 2672 | 3529* | 3530* | 3531 | | | | | | | |

SO2ERR 005366 G
| 2595# | 4945 | 5521 | 6265 | 6773 | 7187 | 7745 | 8162 | 8405 | | | | |

SO4ERR 005406 G
| 2605# | 4924 | 5497 | 6241 | 6749 | 7163 | 7721 | 8138 | 8382 | 10331 | 10952 | 11503 | 12152 |

S2ALLR 005442 G
| 2624# | 3797 | 11226 | 11873 | | | | | | | | | |

S2EROR 005322 G
2568#	3236	3744	3842	3912	5306	6062	6600	6953	7231	7571	7925	8209
8453	10354	10434	10975	11053	11172	11521	11819	12170				

S2GOOD 002246 G
2121#	2689	2693	3537*	3541	3787*	3790*	4938*	5297*	5298*	5513*	5514*	6053*
6054*	6257*	6258*	6591*	6592*	6765*	6766*	7179*	7180*	7562*	7563*	7737*	7738*
8154*	8155*	8397*	8398*	10347*	10427*	10968*	11046*	11215*	11218*	11219*	11514*	11862*
11865*	11866*	12163*										

S2LOAD 002244 G
2120#	2689	2694	2703	3228*	3537	3538	3710*	3768	3806*	3807	3809*	3834*
3894*	3937*	3938	3940*	4937*	5296*	5297	5512*	5513	6052*	6053	6256*	6257
6590*	6591	6764*	6765	7178*	7179	7561*	7562	7736*	7737	8153*	8154	8396*
8397*	10346*	10967*	11153*	11196	11235*	11236	11238*	11513*	11800*	11843	11882*	11883
11885*	12162*											

S2MASK 002250 G
2122#	3229*	3540	3737*	3786*	3835*	3905*	4936*	5299*	5511*	6055*	6255*	6593*
6763*	6946*	7177*	7224*	7564*	7735*	7918*	8152*	8202*	8395*	8446*	10345*	10966*
11165*	11214*	11512*	11812*	11861*	12161*							

S2READ 002252 G
| 2123# | 2692 | 2702 | 3539* | 3540* | 3541 | | | | | | | |

S4EROR 005336 G
2577#	3250	3757	3856	5281	6037	6575	6937	7215	7291	7546	7909	8193
8437	8516	11185	11832									

S4LOAD 002254 G
2125#	2721	3243*	3547	3549	3709*	3770	3804*	3823*	3880*	3882*	4917*	5274*
5490*	6022*	6084	6086*	6234*	6568*	6742*	7156*	7284*	7539*	7714*	8131*	8374*
8375*	8430*	8509*	10324*	10945*	11152*	11198	11233*	11496*	11799*	11845	11880*	12145*

S4READ 002256 G
| 2126# | 2720 | 3548* | 3549 | | | | | | | | | |

S6ALLR 005456 G
2633#	3779	3873	3930	5326	6079	6620	6967	7254	7311	7591	7940	8233
8478	8536	11207	11854									

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PARAMETER CODING   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 269
CVCDDB.P11   14-JUN-82 09:54   CROSS REFERENCE TABLE -- USER SYMBOLS   SEQ 0268

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S6BAD    002270 G      2132#    2740     2750     3558*    3559*    3560
S6EROR   005352 G      2586#
S6GOOD   002262 G      2129#    2737     2741     3555*    3560     3892*    3936*    7247*    7303*    8226*    8471*    8529*
S6LOAD   002260 G      2128#    2737     2742     2751     3555     3556     3767*    3772*    3788     3822*    3878*    3879*    3891*
                       3935*    5319*    6023*    6087*    6613*    6800     6831     6960*    7246*    7247     7302*    7584*    7772
                       7803     7933*    8224*    8225*    8226     8469*    8470*    8471     8527*    8528*    8529     11195*   11200*
                       11216    11842*   11847*   11863
S6MASK   002264 G      2130#    3251#    3559     3766*    3866*    3879     3923*    5318*    6072*    6612*    7583*    11194*   11841*
S6READ   002266 G      2131#    3557*    3558
TARMOD=  000005 G      1928#
TEDEV    002226 G      2105#    3341     3344     3374     3411
TEEDAD   003173 G      2321#    4993     5570
TEEDA1   003242 G      2328#    5028     5599     8814     8926     9042     9151     9279     9400
TEEDCT   003344 G      2339#    9677     9803     9982
TEMSAD   002534 G      2237#    4923     5496     6240     6748     7162     7720     8137     8381     10330    10951
TEMSA1   002410 G      2217#    4944     5520     6264     6772     7186     7744     8161     8404
TETYPE   002230 G      2106#    3359
TEVECT   002214 G      2097#    10561    10647
TOBRK =  000100 G      1937#    3342
TRADRS   003477 G      2356#    5628     5802
T$ARGC=  000003        1468#    1469#    1470#    1471#    1472#    1473#    2654#    2658     2662#    2669     2672#    2678     2684#
                       2688     2692#    2699     2702#    2708     2714#    2718     2720#    2726     2732#    2736     2740#    2747
                       2750#    2756     2823#    2827     2831#    2838     2841#    2847     2853#    2857     2859#    2865     2871#
                       2875     2879#    2886     2889#    2895     2901#    2905     2907#    2913     2973#    2977     3004#    3008
                       3012#    3019     3022#    3028     3034#    3038     3040#    3046     3052#    3056     3060#    3067     3070#
                       3076     3083#    3087     3089#    3095
T$CODE=  004032        12787#   12792#   12797#   12803#   12809#
T$ERRN=  000011        1450#    3182#    3202#    3216#    3234#    3248#    3273#    3292#    3306#    3322#    3349#    3364#    3380#
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                       6201#    6220#    6239#    6263#    6300#    6335#    6479#    6507#    6531#    6544#    6573#    6598#    6618#
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                       11183#   11205#   11224#   11249#   11307#   11329#   11340#   11361#   11391#   11417#   11430#   11467#   11486#
                       11501#   11519#   11549#   11596#   11624#   11635#   11664#   11680#   11717#   11817#   11830#   11852#   11871#
                       11896#   11919#   11977#   11988#   12010#   12040#   12066#   12079#   12116#   12135#   12150#   12168#   12197#
                       12244#   12272#   12283#   12313#   12329#   12366#   12440#   12470#   12487#   12514#   12524#   12539#   12562#
                       12594#   12609#   12638#   12659#   12689#   12727#   12747#
T$EXCP=  000000        12787#   12791    12792#   12796    12797#   12802    12803#   12808    12809#   12814
T$FLAG=  000050        4323#    4325     4430#    4472#    4494#    4496     4516#    4518
T$FREE=  035506        12875    12893#
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T$GMAN= 000000     1450#
T$HILI= 000017    12787#  12790   12792#  12795   12797#  12801   12803#  12807   12809#  12813
T$LAST= 000001     1450#  12875#  12881
T$LOLI= 000000    12787#  12789   12792#  12794   12797#  12800   12803#  12806   12809#  12812
T$LSYM= 010000     1450#   1600    1618    2565    2574    2583    2592    2602    2612    2621    2630    2639    2767
                   2776    2785    2794    2803    2932    2941    2950    2959    2968    4302    4331    4438    4455
                   4480    4502    4524    4655    5069    5830    6365    7330    8552    9408   10000   10656   11104
                  11750   12399   12756   12817   12869
T$LTNO= 000015    12878#
T$NEST= 177777     1450#   1457#   1587#   1599#   1611#   1617#   1620#   1625#   2559#   2564#   2568#   2573#   2577#
                   2582#   2586#   2591#   2595#   2601#   2605#   2611#   2615#   2620#   2624#   2629#   2633#   2638#
                   2761#   2766#   2770#   2775#   2779#   2784#   2788#   2793#   2797#   2802#   2926#   2931#   2935#
                   2940#   2944#   2949#   2953#   2958#   2962#   2967#   3164#   3253#   3257#   3328#   3332#   3512#
                   3674#   3695#   3707#   3728#   3799#   3811#   3826#   3875#   3897#   3932#   3961#   3970#   4012#
                   4022#   4042#   4052#   4062#   4073#   4092#   4102#   4112#   4123#   4141#   4151#   4160#   4171#
                   4189#   4199#   4208#   4219#   4240#   4260#   4270#   4290#   4297#   4301#   4307#   4312#   4319#
                   4330#   4341#   4348#   4357#   4437#   4450#   4454#   4464#   4479#   4490#   4501#   4512#   4523#
                   4527#   4533#   4648#   4654#   4694#   4699#   5031#   5068#   5114#   5117#   5230#   5234#   5269#
                   5328#   5351#   5357#   5805#   5829#   5870#   5873#   5986#   5990#   6026#   6081#   6108#   6114#
                   6339#   6364#   6400#   6437#   7256#   7329#   7372#   7408#   8480#   8551#   8580#   8582#   9403#
                   9407#   9440#   9446#   9985#   9999#  10054#  10057#  10651#  10655#  10685#  10687#  11100#  11103#
                  11120#  11124#  11157#  11228#  11253#  11257#  11745#  11749#  11767#  11771#  11804#  11875#  11900#
                  11904#  12394#  12398#  12417#  12421#  12751#  12755#  12758#  12763#  12774#  12815#  12860#  12867#
                  12879#
T$NS0 = 000000     1457#   1620    1625#   4307    4312#   4527    4533#  12758   12763#  12879
T$NS1 = 000005     1587#   1599    1611#   1617    2559#   2564    2568#   2573    2577#   2582    2586#   2591    2595#
                   2601    2605#   2611    2615#   2620    2624#   2629    2633#   2638    2761#   2766    2770#   2775
                   2779#   2784    2788#   2793    2797#   2802    2926#   2931    2935#   2940    2944#   2949    2953#
                   2958    2962#   2967    3164#   3253    3257#   3328    3332#   3512    3674#   3695    3707#   3811
                   3826#   3875    3897#   3932    3961#   3970    4012#   4022    4042#   4052    4062#   4073    4092#
                   4102    4112#   4123    4141#   4151    4160#   4171    4189#   4199    4208#   4219    4240#   4260
                   4270#   4290    4297#   4301    4319#   4330    4341#   4348    4357#   4437    4450#   4454    4464#
                   4479    4490#   4501    4512#   4523    4648#   4654    4694#   5068    5114#   5829    5870#   6364
                   6400#   7329    7372#   8551    8580#   9407    9440#   9999   10054#  10655   10685#  11103   11120#
                  11749   11767#  12398   12417#  12755   12774#  12815   12860#  12867
T$NS2 = 000003     3728#   3799    4699#   5031    5117#   5230    5234#   5351    5357#   5805    5873#   5986    5990#
                   6108    6114#   6339    6437#   7256    7408#   8480    8582#   9403    9446#   9985   10057#  10651
                  10687#  11100   11124#  11253   11257#  11745   11771#  11900   11904#  12394   12421#  12751
T$NS3 = 000003     5269#   5328    6026#   6081   11157#  11228   11804#  11875
T$PCNT= 000000    12881#  12882#
T$PTAB= 010055    12882#  12885
T$PTHV= 000001     1481   12893#
T$PTNU= 000001     1450#  12885#  12893
T$SAVL= 177777     1450#
T$SEGL= 177777     1450#   3164#   3253#   3255    3257#   3328#   3330    3332#   3512#   3514    3674#   3695#   3697
                   3707#   3728#   3799#   3801    3811#   3813    3826#   3875#   3877    3897#   3932#   3934    3961#
                   3970#   3972    4012#   4022#   4024    4042#   4052#   4054    4062#   4073#   4075    4092#   4102#
                   4104    4112#   4123#   4125    4141#   4151#   4153    4160#   4171#   4173    4189#   4199#   4201
                   4208#   4219#   4221    4240#   4260#   4262    4270#   4290#   4292    4699#   5031#   5033    5117#
                   5230#   5232    5234#   5269#   5328#   5330    5351#   5353    5357#   5805#   5807    5873#   5986#
                   5988    5990#   6026#   6081#   6083    6108#   6110    6114#   6339#   6341    6437#   7256#   7258
                   7408#   8480#   8482    8582#   9403#   9405    9446#   9985#   9987   10057#  10651#  10653   10687#
                  11100#  11102   11124#  11157#  11228#  11230   11253#  11255   11257#  11745#  11747   11771#  11804#
                  11875#  11877   11900#  11902   11904#  12394#  12396   12421#  12751#  12753
T$SEK0= 010000     3164#   3253    3257#   3328    3332#   3512    3674#   3695    3707#   3811    3826#   3875    3897#
                   3932    3961#   3970    4012#   4022    4042#   4052    4062#   4073    4092#   4102    4112#   4123
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M 5

PARAMETER CODING   MACY11 30A(1052) 16-JUN-82 13:46 PAGE 271
CVCDDB.P11   14-JUN-82 09:54   CROSS REFERENCE TABLE -- USER SYMBOLS   SEQ 0270

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                    4141#    4151     4160#    4171     4189#    4199     4208#    4219     4240#    4260     4270#    4290     4699#
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                    6437#    7256     7408#    8480     8582#    9403     9446#    9985     10057#   10651    10687#   11100    11124#
                    11253    11257#   11745    11771#   11900    11904#   12394    12421#   12751
T$SEK1= 010001      3728#    3799     5269#    5328     6026#    6081     11157#   11228    11804#   11875
T$SIZE= 000007      12876    12893#
T$SUBN= 000000      1450#    4647#    4693#    5113#    5869#    6399#    7371#    8579#    9439#    10053#   10684#   11119#   11766#
                    12416#
T$TAGL= 177777      1450#
T$TAGN= 010057      1450#    1587#    1611#    2559#    2568#    2577#    2586#    2595#    2605#    2615#    2624#    2633#    2761#
                    2770#    2779#    2788#    2797#    2926#    2935#    2944#    2953#    2962#    4297#    4319#    4341#    4357#
                    4450#    4464#    4490#    4512#    4648#    4694#    5114#    5870#    6400#    7372#    8580#    9440#    10054#
                    10685#   11120#   11767#   12417#   12774#   12860#   12881#   12882#   12883#
T$TEMP= 000000      1563#    1564#    1565#    1566#    1567#    1568#    1569#    1570#    1571#    1572#    1573#    1574#    1575#
                    1576#    1599#    1617#    1620#    2564#    2573#    2582#    2591#    2601#    2611#    2620#    2629#    2638#
                    2766#    2775#    2784#    2793#    2802#    2931#    2940#    2949#    2958#    2967#    3253#    3328#    3512#
                    3695#    3799#    3811#    3875#    3932#    3970#    4022#    4052#    4073#    4102#    4123#    4151#    4171#
                    4199#    4219#    4260#    4290#    4301#    4307#    4323#    4324     4330#    4348#    4430#    4431     4437#
                    4454#    4472#    4473     4479#    4494#    4495     4501#    4516#    4517     4523#    4527#    4654#    5031#
                    5068#    5230#    5328#    5351#    5805#    5829#    5986#    6081#    6108#    6339#    6364#    7256#    7329#
                    8480#    8551#    9403#    9407#    9985#    9999#    10651#   10655#   11100#   11103#   11228#   11253#   11745#
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                    12815#   12867#   12879#
T$TEST= 000015      1450#    4647#    4693#    5113#    5869#    6399#    7371#    8579#    9439#    10053#   10684#   11119#   11766#
                    12416#   12878
T$TSTM= 177777      1450#    2565     2574     2583     2592     2602     2612     2621     2630     2639     2657     2668     2677
                    2687     2698     2707     2717     2725     2735     2746     2755     2767     2776     2785     2794     2803
                    2826     2837     2846     2856     2864     2874     2885     2894     2904     2912     2932     2941     2950
                    2959     2968     2976     3007     3018     3027     3037     3045     3055     3066     3075     3086     3094
                    3164     3181     3186     3201     3206     3215     3220     3233     3238     3247     3254     3257     3272
                    3277     3291     3296     3305     3310     3321     3329     3332     3348     3363     3368     3379     3384
                    3400     3405     3416     3421     3434     3439     3455     3460     3465     3470     3481     3486     3497
                    3502     3507     3513     3674     3680     3685     3690     3696     3707     3728     3741     3746     3754
                    3759     3776     3781     3794     3800     3812     3826     3839     3844     3853     3858     3870     3876
                    3897     3909     3914     3927     3933     3961     3965     3971     4012     4017     4023     4042     4047
                    4053     4062     4068     4074     4092     4097     4103     4112     4118     4124     4141     4146     4152
                    4160     4166     4172     4189     4194     4200     4208     4214     4220     4240     4245     4250     4255
                    4261     4270     4275     4280     4285     4291     4331     4360     4365     4370     4374     4380     4384
                    4390     4396     4426     4430     4438     4455     4467     4469     4472     4480     4502     4524     4655
                    4699     4740     4745     4768     4773     4792     4797     4816     4821     4867     4872     4881     4886
                    4902     4907     4921     4926     4942     4947     4963     4968     4991     4996     5026     5032     5069
                    5117     5160     5165     5188     5193     5212     5217     5225     5231     5234     5269     5278     5283
                    5303     5308     5323     5329     5346     5352     5357     5387     5392     5408     5413     5456     5461
                    5475     5480     5494     5499     5518     5523     5539     5544     5568     5573     5597     5602     5626
                    5658     5663     5689     5694     5727     5732     5765     5770     5800     5806     5830     5873     5915
                    5920     5944     5949     5968     5973     5981     5987     5990     6026     6034     6039     6059     6064
                    6076     6082     6103     6109     6114     6139     6144     6160     6165     6200     6205     6219     6224
                    6238     6243     6262     6267     6299     6304     6334     6340     6365     6437     6478     6483     6506
                    6511     6530     6535     6543     6548     6572     6577     6597     6602     6617     6622     6634     6639
                    6663     6668     6708     6713     6727     6732     6746     6751     6770     6775     6804     6809     6835
                    6840     6858     6863     6869     6874     6901     6906     6921     6926     6934     6939     6950     6955
                    6964     6969     6978     6983     7009     7014     7039     7044     7055     7060     7079     7084     7122
                    7127     7141     7146     7160     7165     7184     7189     7199     7204     7212     7217     7228     7233
                    7251     7257     7288     7293     7308     7313     7330     7408     7449     7454     7477     7482     7501
                    7506     7514     7519     7543     7548     7568     7573     7588     7593     7605     7610     7635     7640
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8121	8135	8140	8159	8164	8177	8182	8190	8195	8206	8211	8230	8235
8245	8250	8274	8279	8298	8303	8341	8346	8359	8364	8379	8384	8402
8407	8420	8425	8434	8439	8450	8455	8475	8481	8513	8518	8533	8538
8552	8582	8621	8626	8649	8654	8673	8678	8695	8700	8709	8714	8752
8757	8765	8770	8785	8790	8812	8817	8839	8844	8869	8874	8882	8887
8902	8907	8924	8929	8941	8946	8972	8977	8993	8998	9040	9045	9069
9074	9103	9108	9116	9121	9149	9154	9178	9183	9193	9198	9231	9236
9244	9249	9277	9282	9305	9310	9352	9357	9365	9370	9398	9404	9408
9446	9478	9483	9505	9510	9527	9532	9583	9588	9598	9603	9621	9626
9641	9646	9675	9680	9697	9702	9714	9719	9738	9743	9771	9776	9801
9806	9829	9834	9844	9849	9867	9872	9884	9889	9902	9907	9924	9929
9980	9986	10000	10057	10061	10103	10108	10149	10154	10177	10182	10201	10206
10227	10232	10240	10245	10292	10297	10307	10312	10328	10333	10351	10356	10364
10369	10391	10396	10405	10410	10431	10436	10457	10462	10476	10481	10494	10499
10529	10534	10547	10552	10563	10575	10580	10588	10600	10605	10614	10619	10633
10638	10648	10652	10656	10687	10728	10733	10773	10778	10800	10805	10824	10829
10850	10855	10863	10868	10913	10918	10928	10933	10949	10954	10972	10977	10985
10990	11012	11017	11026	11031	11050	11055	11073	11078	11087	11092	11101	11104
11124	11157	11169	11174	11182	11187	11204	11209	11223	11229	11248	11254	11257
11306	11311	11328	11333	11339	11344	11360	11365	11390	11395	11416	11421	11429
11434	11466	11471	11485	11490	11500	11505	11518	11523	11548	11553	11595	11600
11623	11628	11634	11639	11663	11668	11679	11684	11716	11721	11746	11750	11771
11804	11816	11821	11829	11834	11851	11856	11870	11876	11895	11901	11904	11954
11959	11976	11981	11987	11992	12009	12014	12039	12044	12065	12070	12078	12083
12115	12120	12134	12139	12149	12154	12167	12172	12196	12201	12243	12248	12271
12276	12282	12287	12312	12317	12328	12333	12365	12370	12395	12399	12421	12439
12444	12469	12474	12486	12491	12513	12518	12523	12528	12538	12543	12561	12566
12593	12598	12608	12613	12637	12642	12658	12663	12688	12693	12726	12731	12746
12752	12756											

Symbol													
T$TSTS= 000001	1450#	4648#	4694#	5114#	5870#	6400#	7372#	8580#	9440#	10054#	10685#	11120#	11767#
	12417#												
T$$AU = 010034	4512#	4516	4523										
T$$AUT= 010031	4450#	4454											
T$$CLE= 010032	4464#	4472	4479										
T$$DAT= 010056	12883#	12891											
T$$DU = 010033	4490#	4494	4501										
T$$HAR= 010052	12774#	12816											
T$$HW = 010000	1587#	1599											
T$$INI= 010030	4357#	4430	4437#										
T$$MSG= 010024	2559#	2564	2568#	2573	2577#	2582	2586#	2591	2595#	2601	2605#	2611	2615#
	2620	2624#	2629	2633#	2638	2761#	2766	2770#	2775	2779#	2784	2788#	2793
	2797#	2802	2926#	2931	2935#	2940	2944#	2949	2953#	2958	2962#	2967	
T$$PC = 000001	12881#	12893											
T$$PRO= 010027	4341#												
T$$PTA= 010055	12881#	12884	12885#										
T$$RPT= 010026	4319#	4323	4330										
T$$SEG= 010000	3164#	3253#	3257#	3328#	3332#	3512#	3674#	3695#	3707#	3728#	3799#	3811#	3826#
	3875#	3897#	3932#	3961#	3970#	4012#	4022#	4042#	4052#	4062#	4073#	4092#	4102#
	4112#	4123#	4141#	4151#	4160#	4171#	4189#	4199#	4208#	4219#	4240#	4260#	4270#
	4290#	4699#	5031#	5117#	5230#	5234#	5269#	5328#	5351#	5357#	5805#	5873#	5986#
	5990#	6026#	6081#	6108#	6114#	6339#	6437#	7256#	7408#	8480#	8582#	9403#	9446#
	9985#	10057#	10651#	10687#	11100#	11124#	11157#	11228#	11253#	11257#	11745#	11771#	11804#
	11875#	11900#	11904#	12394#	12421#	12751#							
T$$SOF= 010053	12860#	12868											

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T$$SRV= 010025      4297#    4301
T$$SW = 010001      1611#    1617
T$$TES= 010051      4648#    4654     4694#    5068     5114#    5829     5870#    6364     6400#    7329     7372#    8551     8580#
                    9407     9440#    9999    10054#   10655    10685#   11103    11120#   11749    11767#   12398    12417#   12755
TOEROR  006666 G    2926#    3351     3366     3382     3419     3484     4020     4870     8768     8885     8944     9119     9247
                    9368     9601     9847    10295    10394    10460    10479    10532    10578    10603    10617    10636    10916
                   11015    11076    12596    12661    12749
TOGOOD  002326 G    2160#    3009     3013     3359*    3620*    3624    10387*   10472*   10525*   10571*   10611    10629*   11008*
                   11069    12654*   12742*
TOLOAD  002324 G    2159#    3009     3014     3023     3341*    3358*    3374*    3375*    3411*    3412*    3477*    3620     3621
                    3985     4013*    9594*    9840*   10570*   12589*
TOMASK  002330 G    2161#    3342*    3476*    3623
TOREAD  002332 G    2162#    3012     3022     3622*    3623*    3624     4298*   10611
TO6ERR  006732 G    2953#    3403     3437     4050     4071     4100     4121     4149     4169     4197     4217     4743     4771
                    4795     4819     5163     5191     5215     5390     5411     5918     5947     5971     6142     6163     6481
                    6509     6533     6666     7012     7042     7452     7480     7504     7638     7987     8017     8277     8624
                    8652     8676     8698     8842     8975     9072     9181     9308     9481     9508     9530     9624     9700
                    9741     9870     9887     9927    10152    10180    10204    10230    10776    10803    10827    10853    11309
                   11363    11393    11419    11666    11957    12012    12042    12068    12315    12611
T1      013400 G    1563     4647#
T10     030116 G    1572    10684#
T11     031072 G    1573    11119#
T12     032604 G    1574    11766#
T13     034326 G    1575    12416#
T2      013406 G    1564     4693#
T2EROR  006702 G    2935#    3458     3468     4278     4288     9196     9717     9905
T2LOAD  002334 G    2164#    3041     3451*    3461*    3630     3632     4271*    4281*    4718*    5136*    5890*    6454*    7425*
                    8598*    9189*    9461*    9710*    9898*   10125*   10750*   11276*   11923*   12581*
T2READ  002336 G    2165#    3040     3631*    3632
T3      014266 G    1565     5113#
T4      015670 G    1566     5869#
T4EROR  006716 G    2944#    3500     3510     4248     4258     4884     5228     5459     5730     5984     6203     6337     6546
                    6711     6861     6872     6904     7058     7125     7517     7683     7833     7844     7876     8033     8100
                    8344     8712     8755     8872     8996     9106     9234     9355     9586     9774     9832    10243    10310
                   10408    10497    10550    10866    10931    11029    11090    11331    11342    11432    11469    11626    11637
                   11682    11979    11990    12081    12118    12274    12285    12331    12691
T4GOOD  002342 G    2168#    3057     3061     3638*    3641     4877*    5452*    5723*    6196*    6330*    6704*    6854*    6865*
                    6897*    7118*    7676*    7826*    7837*    7869*    8093*    8337*    8748*    8989*    9099*    9227*    9348*
                    9579*    9767*    9825*   10303*   10401*   10489*   10490*   10542*   10543*   10924*   11022*   11083*   11323*
                   11324*   11335*   11462*   11618*   11619*   11630*   11675*   11971*   11972*   11983*   12111*   12266*   12267*
                   12278*   12324*   12684*
T4LOAD  002340 G    2167#    3057     3062     3071     3493*    3503*    3638     3639     4241*    4251*    4751*    5171*    5926*
                    6489*    6853*    6864*    7051*    7460*    7825*    7836*    8026*    8632*    8705*    8954*    9539*   10160*
                   10488*   10489    10643*   10784*   11097*   11322*   11323    11334*   11617*   11618    11629*   11674*   11741*
                   11970*   11971    11982*   12265*   12266    12277*   12323*   12390*   12620*   12699*
T4READ  002344 G    2169#    3060     3070     3640*    3641
T5      016770 G    1567     6399#
T6      021132 G    1568     7371#
T6ALLR  006746 G    2962#    5661     5692     6302     6807     6838     7082     7779     7810     8057     8301    11551    11598
                   11719    12199    12246    12368
T6LOAD  002346 G    2171#    3090     3395*    3430*    3647     3650     4043*    4063*    4064*    4093*    4113*    4114*    4142*
                    4161*    4162*    4190*    4209*    4210*    4735*    4736*    4764*    4788*    4812*    4852*    4853*    5156*
                    5184*    5208*    5383*    5404*    5654*    5685*    5712*    5910*    5940*    5964*    6134*    6156*    6294*
                    6318*    6474*    6502*    6526*    6659*    6676*    6800*    6831*    6888*    7005*    7035*    7075*    7092*
                    7445*    7473*    7497*    7631*    7648*    7772*    7803*    7860*    7980*    8010*    8050*    8067*    8269*
                    8270*    8294*    8311*    8617*    8645*    8669*    8691*    8739*    8835*    8968*    9065*    9174*    9301*
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                          9474*   9500*   9501*   9523*   9617*   9692*   9693*   9734*   9863*   9880*   9920*  10145*  10173*
                         10197*  10223*  10254*  10769*  10796*  10820*  10846*  10875*  11302*  11356*  11385*  11412*  11443*
                         11543*  11562*  11590*  11651*  11659*  11711*  11730*  11950*  12005*  12034*  12061*  12092*  12191*
                         12210*  12238*  12299*  12307*  12308*  12360*  12379*  12604*
T6MASK   002352 G         2173#   3396    3649    5911    6135    6295    6319   11264*  11544*  11563*  11591*  11652*  11712*
                         11731*  11911*  12192*  12211*  12239*  12300*  12361*  12380*
T6READ   002350 G         2172#   3089    3648*   3649*   3650
T7       023752 G         1569    8579#
T8       025430 G         1570    9439#
T9       026612 G         1571   10053#
UAM    = 000200 G         1692#
UNITNB   002232 G         2108#   4387*   4393*   4395
VDALRG   003710 G         2399#   3499    3509    4247    4257    4883    5227    5458    5729    5983    6202    6336    6545
                          6710    6860    6871    6903    7057    7124    7516    7682    7832    7843    7875    8032    8099
                          8343    8711    8754    8871    8995    9105    9233    9354    9585    9773    9831   10242   10309
                         10407   10496   10549   10865   10930   11028   11089   11330   11341   11431   11468   11625   11636
                         11681   11978   11989   12080   12117   12273   12284   12330   12690
VDAL0  = 000001 G         1984#   7051    8026   11674   11675   12323   12324
VDAL1  = 000002 G         1983#
VDAL10 = 002000 G         1974#
VDAL11 = 004000 G         1973#
VDAL12 = 010000 G         1972#
VDAL13 = 020000 G         1971#
VDAL14 = 040000 G         1970#
VDAL15 = 100000 G         1969#
VDAL2  = 000004 G         1982#   3493    4241    4251    6853    6854    6864    6865    7825    7826    7836    7837   11322
                         11334   11335   11617   11629   11630   11970   11982   11983   12265   12277   12278
VDAL3  = 000010 G         1981#   5452    6196    6704    7676
VDAL4  = 000020 G         1980#   4877    5723    6330    7118    8093    8337    8748    8989    9099    9227    9348    9579
                          9825   10303   10401   10490   10542   10924   11022   11083
VDAL5  = 000040 G         1979#   8748    9099   10543   11324   11619   11972   12267   12684
VDAL6  = 000100 G         1978#   5452    6196    6704    7676
VDAL7  = 000200 G         1977#   8705   10488   11322   11970   12620
VDAL8  = 000400 G         1976#
VDAL9  = 001000 G         1975#  10543   11462   12111   12684
WREH   = 000002 G         1788#   3772    3788   11200   11216   11847   11863
WRENH  = 000100 G         1745#   3786    3787    3790    5298    5514    6054    6258    6592    6766    7180    7563    7738
                          8155    8398   11214   11215   11218   11514   11861   11862   11865   12163
WRVH   = 000040 G         1730#   3676   10981
XBCLR    012602 G         4180#
XBCLRH   012614 G         4180    4188#
XBCLRL   012646 G         4181    4207#
XCAS     012372 G         4082#   8984
XCASH    012404 G         4082    4091#   4855    5446    6190    6698    7109    7670    8084    8328    9334    9570    9762
                         10278   10900
XCASL    012436 G         4083    4111#   4857    5713    6320    6889    7111    7861    8086    8330    9342    9572    9819
                         10280   10902
XPI      012476 G         4132#   9006    9220
XPIH     012510 G         4132    4140#   4856    5447    6191    6699    7110    7671    8085    8329    9335    9571    9755
                          9940   10279   10901   11694   12343
XPIL     012542 G         4133    4159#   4858    5714    6321    6890    7112    7862    8087    8331    9343    9573    9820
                          9955   10281   10903   11653   11737   12301   12386
XRAS     012266 G         4032#   8740    8862    9091    9209    9321    9950   10381   10447   10519   11002   12676
XRASH    012300 G         4032    4041#   4854    5445    6189    6697    7108    7669    8083    8327    9569   10277   10899
                         11457   12106
XRASL    012332 G         4033    4061#   4859    5715    6322    6891    7113    7863    8088    8332    9574   10282   10904
```

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                              11654    12302
X$ALWA= 000000                1450#
X$FALS= 000040                1450#
X$OFFS= 000400                1450#
X$TRUE= 000020                1450#
$PATCH  035444 G             12870#
.     = 035506                1454#   2189#   2199#   2505#   4324    4431    4473    4495    4517   12845#  12871#  12883   12893


. ABS.  035506      000


ERRORS DETECTED:  0

CVCDDB.OBJ,CVCDDB.SEQ/CRF:SYM/SOL/NL:TOC=SVC/ML,CVCDDB.P11
RUN-TIME: 59 67 4 SECONDS
RUN-TIME RATIO: 618/131=4.6
CORE USED:  17K  (33 PAGES)
```