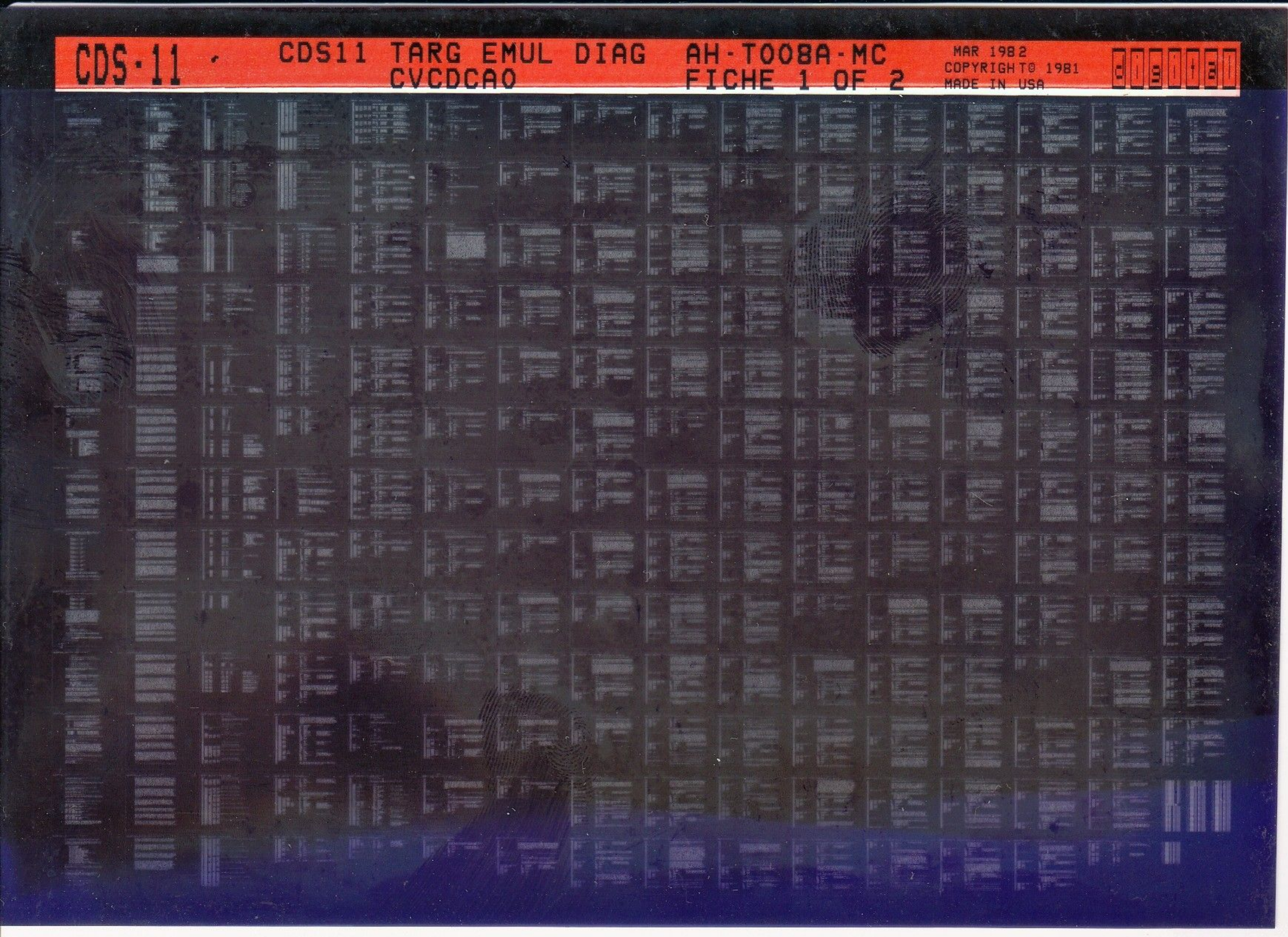
CDS-11 · CDS11 TARG EMUL DIAG AH-T008A-MC
CVCDCA0 FICHE 1 OF 2



CDS·11 CDS11 TARG EMUL DIAG AH·T008A·MC
CVCDCA0 FICHE 2 OF 2
MAR 1982

MADE IN USA

.REM &

IDENTIFICATION

PRODUCT CODE: AC-T006A-MC

PRODUCT NAME: CVCDCA0 CDS-11 TARGET EMUL DIAG

PRODUCT DATE: SEPTEMBER '981

MAINTAINER: DIAGNOSTIC ENGINEERING

REVISION HISTORY

REVISION	DATE	REASONS
1	SEPTEMBER 1981	FIRST RELEASE

TABLE OF CONTENTS

1.0 GENERAL INFORMATION

1.1 PROGRAM ABSTRACT

THE CDS-1 TARGET EMULATOR DIAGNOSTIC WILL TEST ALL THE LOGIC ON THE TARGET EMULATOR MODULE AND THE "POD" THAT IS TESTABLE WITHOUT THE ADDITION OF OTHER CDS MODULES. ALL DATA PATHS AND REGISTERS WITHIN THE TARGET EMULATOR MODULE ARE TESTED. HOWEVER, THE OUTPUT AND INPUT SIGNALS TO AND FROM THE TARGET SYSTEM ARE NOT TESTED. LIMITED TESTING OF THE SYSTEM BUS IS PERFORMED. THE PROGRAM ALSO CHECKS THAT THE TARGET EMULATOR MODULE CAN GENERATE INTERRUPTS TO THE LSI-11. THE T-11 CHIP WILL BE ENABLED IN THE LAST PART OF THIS DIAGNOSTIC, HOWEVER, ONLY LIMITED TESTING OF THE T-11 WILL BE PERFORMED.

THIS DIAGNOSTIC HAS BEEN WRITTEN FOR USE WITH THE DIAGNOSTIC RUNTIME SERVICES SOFTWARE (SUPERVISOR). THESE SERVICES PROVIDE THE INTERFACE TO THE OPERATOR AND TO THE SOFTWARE ENVIRONMENT. THIS PROGRAM CAN BE USED WITH XXDP+, ACT APT, SLIDE AND PAPER TAPE. FOR A COMPLETE DESCRIPTION OF THE RUNTIME SERVICES, REFER TO THE XXDP+ USER'S MANUAL. THERE IS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES IN SECTION 2 OF THIS DOCUMENT.

NOTE: THIS PROGRAM HAS NOT BEEN TESTED IN THE APT ENVIRONMENT, HOWEVER, THE APT INTERFACE HAS BEEN PROVIDED IN THE DIAGNOSTIC.

NOTE: THE T-11 POD MUST BE CONNECTED TO THE TARGET EMULATOR MODULE AND DISCONNECT FROM THE TARGET SYSTEM BEFORE EXECUTION OF THIS PROGRAM.

1.2 SYSTEM REQUIREMENTS

1. LSI-11 OR EQUIVALENT TYPE CPU WITH Q-BUS
2. MINIMUM OF 16K WORDS OF MEMORY
3. CONSOLE TERMINAL AND CONTROLLER
4. CDS-11 BACKPLANE AND CABLES
5. TARGET EMULATOR MODULE(S) (M8742)
6. T-11 POD(S)
7. MXV11 MODULE AND CDS-11 ROMS
8. STORAGE DEVICE WITH CONTROLLER (OPTIONAL)
9. XXDP+ MEDIA FOR STORAGE DEVICE (OPTIONAL)

1.3 RELATED DOCUMENTS AND STANDARDS

CHQUS? XXDP+ USER'S MANUAL (THE "?" IN CHQUS INDICATES THE REVISION LEVEL OF THE DOCUMENT. AT THE TIME THIS PROGRAM WAS WRITTEN, THE REVISION LEVEL WAS "E".

1.4 DIAGNOSTIC HIERARCY PREREQUISITES

ALL HARDWARE THAT IS SPECIFIED IN SECTION 1.2 OF THIS DOCUMENT MUST BE OPERATIONAL AND FREE OF ALL FAULTS.

1.5 ASSUMPTIONS

2.0 OPERATING INSTRUCTIONS

THIS SECTION CONTAINS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES.
FOR DETAILED INFORMATION, REFER TO THE XXDP+ USER'S MANUAL (CHQUS).

2.1 COMMANDS

THERE ARE ELEVEN LEGAL COMMANDS FOR THE DIAGNOSTIC RUNTIME SERVICES
(SUPERVISOR). THIS SECTION LISTS THE COMMANDS AND GIVES A VERY
BRIEF DESCRIPTION OF THEM. THE XXDP+ USER'S MANUAL HAS MORE DETAILS.

COMMAND	EFFECT
START	START THE DIAGNOSTIC FROM AN INITIAL STATE
RESTART	START THE DIAGNOSTIC WITHOUT INITIALIZING
CONTINUE	CONTINUE AT TEST THAT WAS INTERRUPTED (AFTER ^C)
PROCEED	CONTINUE FROM AN ERROR HALT
EXIT	RETURN TO XXDP+ MONITOR (XXDP+ OPERATION ONLY.)
ADD	ACTIVATE A UNIT FOR TESTING (ALL UNITS ARE CONSIDERED TO BE ACTIVE AT START TIME
DROP	DEACTIVATE A UNIT
PRINT	PRINT STATISTICAL INFORMATION (IF IMPLEMENTED BY THE DIAGNOSTIC - SECTION 4.0)
DISPLAY	TYPE A LIST OF ALL DEVICE INFORMATION
FLAGS	TYPE THE STATE OF ALL FLAGS (SEE SECTION 2.3)
ZFLAGS	CLEAR ALL FLAGS (SEE SECTION 2.3)

A COMMAND CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. SO
YOU MAY, FOR EXAMPLE, TYPE "STA" INSTEAD OF "START".

2.2 SWITCHES

THERE ARE SEVERAL SWITCHES WHICH ARE USED TO MODIFY SUPERVISOR OPERATION.
THESE SWITCHES ARE APPENDED TO THE LEGAL COMMANDS. ALL OF THE LEGAL
SWITCHES ARE TABULATED BELOW WITH A BRIEF DESCRIPTION OF EACH.
IN THE DESCRIPTIONS BELOW, A DECIMAL NUMBER IS DESIGNATED BY "DDDDD".

SWITCH	EFFECT
/TESTS:LIST	EXECUTE ONLY THOSE TESTS SPECIFIED IN THE LIST. LIST IS A STRING OF TEST NUMBERS, FOR EXAMPLE - /TESTS:1:5:7-10. THIS LIST WILL CAUSE TESTS 1,5,7,8,9,10 TO BE RUN. ALL OTHER TESTS WILL NOT BE RUN.
/PASS:DDDDD	EXECUTE DDDDD PASSES (DDDDD = 1 TO 64000)
/FLAGS:FLGS	SET SPECIFIED FLAGS. FLAGS ARE DESCRIBED IN SECTION 2.3.
/EOP:DDDDD	REPORT END OF PASS MESSAGE AFTER EVERY DDDDD PASSES ONLY. (DDDDD = 1 TO 64000)
/UNITS:LIST	TEST/ADD/DROP ONLY THOSE UNITS SPECIFIED IN THE LIST. LIST EXAMPLE - /UNITS:0:5:10-12 USE UNITS 0,5,10,11,12 (UNIT NUMBERS = 0-63)

EXAMPLE OF SWITCH USAGE:

```
START/TESTS:1-5/PASS:1000/EOP:100
```

THE EFFECT OF THIS COMMAND WILL BE: 1) TESTS 1 THROUGH 5 WILL BE EXECUTED, 2) ALL UNITS WILL BE TESTED 1000 TIMES AND 3) THE END OF PASS MESSAGES WILL BE PRINTED AFTER EACH 100 PASSES ONLY. A SWITCH CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. YOU MAY, FOR EXAMPLE, TYPE "/TES:1-5" INSTEAD OF "/TESTS:1-5".

BELOW IS A TABLE THAT SPECIFIES WHICH SWITCHES CAN BE USED BY EACH COMMAND.

	TESTS	PASS	FLAGS	EOP	UNITS
START	X	X	X	X	X
RESTART	X	X	X	X	X
CONTINUE		X	X	X	
PROCEED			X		
DROP					X
ADD					X
PRINT					
DISPLAY					X
FLAGS					
ZFLAGS					
EXIT					

2.3 FLAGS

FLAGS ARE USED TO SET UP CERTAIN OPERATIONAL PARAMETERS SUCH AS LOOPING ON ERROR. ALL FLAGS ARE CLEARED AT STARTUP AND REMAIN CLEARED UNTIL EXPLICITLY SET USING THE FLAGS SWITCH. FLAGS ARE ALSO CLEARED AFTER A START COMMAND UNLESS SET USING THE FLAG SWITCH. THE ZFLAGS COMMAND MAY ALSO BE USED TO CLEAR ALL FLAGS. WITH THE EXCEPTION OF THE START AND ZFLAGS COMMANDS, NO COMMANDS AFFECT THE STATE OF THE FLAGS; THEY REMAIN SET OR CLEARED AS SPECIFIED BY THE LAST FLAG SWITCH.

FLAG	EFFECT
HOE	HALT ON ERROR - CONTROL IS RETURNED TO RUNTIME SERVICES COMMAND MODE
LOE	LOOP ON ERROR
IER*	INHIBIT ALL ERROR REPORTS
IBE*	INHIBIT ALL ERROR REPORTS EXCEPT FIRST LEVEL (FIRST LEVEL CONTAINS ERROR TYPE, NUMBER, PC, TEST AND UNIT)
IXE*	INHIBIT EXTENDED ERROR REPORTS (THOSE CALLED BY PRINTX MACRO'S)
PRI	DIRECT MESSAGES TO LINE PRINTER
PNT	PRINT TEST NUMBER AS TEST EXECUTES
BOE	"BELL" ON ERROR
UAM	UNATTENDED MODE (NO MANUAL INTERVENTION)
ISR	INHIBIT STATISTICAL REPORTS (DOES NOT APPLY TO DIAGNOSTICS WHICH DO NOT SUPPORT STATISTICAL REPORTING)
IDR	INHIBIT PROGRAM DROPPING OF UNITS
ADR	EXECUTE AUTODROP CODE
LOT	LOOP ON TEST

EVL EXECUTE EVALUATION (ON DIAGNOSTICS WHICH HAVE EVALUATION SUPPORT)

*ERROR MESSAGES ARE DESCRIBED IN SECTION 3.1

SEE THE XXDP+ USER'S MANUAL FOR MORE DETAILS ON FLAGS. YOU MAY SPECIFY MORE THAN ONE FLAG WITH THE FLAG SWITCH. FOR EXAMPLE, TO CAUSE THE PROGRAM TO LOOP ON ERROR, INHIBIT ERROR REPORTS AND TYPE A "BELL" ON ERROR, YOU MAY USE THE FOLLOWING STRING:

```
/FLAGS:LOE:IER:BOE
```

2.4 HARDWARE QUESTIONS

WHEN A DIAGNOSTIC IS STARTED, THE RUNTIME SERVICES WILL PROMPT THE USER FOR HARDWARE INFORMATION BY TYPING "CHANGE HW (L) ?" YOU MUST ANSWER "Y" AFTER A START COMMAND UNLESS THE HARDWARE INFORMATION HAS BEEN "PRELOADED" USING THE SETUP UTILITY (SEE CHAPTER 6 OF THE XXDP+ USER'S MANUAL). WHEN YOU ANSWER THIS QUESTION WITH A "Y", THE RUNTIME SERVICES WILL ASK FOR THE NUMBER OF UNITS (IN DECIMAL). YOU WILL THEN BE ASKED THE FOLLOWING QUESTIONS FOR EACH UNIT.

```
CSR ADDRESS:
VECTOR ADDRESS:
DEVICE NUMBER:
```

2.5 SOFTWARE QUESTIONS

AFTER YOU HAVE ANSWERED THE HARDWARE QUESTIONS OR AFTER A RESTART OR CONTINUE COMMAND, THE RUNTIME SERVICES WILL ASK FOR SOFTWARE PARAMETERS. THESE PARAMETERS WILL GOVERN SOME DIAGNOSTIC SPECIFIC OPERATION MODES. YOU WILL BE PROMPTED BY "CHANGE SW (L) ?" IF YOU WISH TO CHANGE ANY PARAMETERS, ANSWER BY TYPING "Y". THE SOFTWARE QUESTIONS AND THE DEFAULT VALUES ARE DESCRIBED IN THE NEXT PARAGRAPH(S).

THERE ARE NO SOFTWARE QUESTIONS IN THIS PROGRAM.

2.6 EXTENDED P-TABLE DIALOGUE

WHEN YOU ANSWER THE HARDWARE QUESTIONS, YOU ARE BUILDING ENTRIES IN A TABLE THAT DESCRIBES THE DEVICES UNDER TEST. THE SIMPLEST WAY TO BUILD THIS TABLE IS TO ANSWER ALL QUESTIONS FOR EACH UNIT TO BE TESTED. IF YOU HAVE A MULTIPLEXED DEVICE SUCH AS A MASS STORAGE CONTROLLER WITH SEVERAL DRIVES OR A COMMUNICATION DEVICE WITH SEVERAL LINES, THIS BECOMES TEDIOUS SINCE MOST OF THE ANSWERS ARE REPETITIOUS.

TO ILLUSTRATE A MORE EFFICIENT METHOD, SUPPOSE YOU ARE TESTING A FICTIONAL DEVICE, THE XY11. SUPPOSE THIS DEVICE CONSISTS OF A CONTROL MODULE WITH EIGHT UNITS (SUB-DEVICES) ATTACHED TO IT.

THESE UNITS ARE DESCRIBED BY THE OCTAL NUMBERS 0 THROUGH 7. THERE
IS ONE HARDWARE PARAMETER THAT CAN VARY AMONG UNITS CALLED THE
Q-FACTOR. THIS Q-FACTOR MAY BE 0 OR 1. BELOW IS A SIMPLE WAY
TO BUILD A TABLE FOR ONE XY11 WITH EIGHT UNITS.

```
# UNITS (D) ?  8<CR>

UNIT 1
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  0<CR>
Q-FACTOR (O) 0 ?  1<CR>

UNIT 2
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  1<CR>
Q-FACTOR (O) 1 ?  0<CR>

UNIT 3
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  2<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 4
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  3<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 5
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  4<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 6
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  5<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 7
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  6<CR>
Q-FACTOR (O) 0 ?  1<CR>

UNIT 8
CSR ADDRESS (O)  160000<CR>
SUB-DEVICE # (O) ?  7<CR>
Q-FACTOR (O) 1 ?  <CR>
```

NOTICE THAT THE DEFAULT VALUE FOR THE Q-FACTOR CHANGES WHEN A
NON-DEFAULT RESPONSE IS GIVEN. BE CAREFUL WHEN SPECIFYING
MULTIPLE UNITS!

AS YOU CAN SEE FROM THE ABOVE EXAMPLE, THE HARDWARE PARAMETERS
DO NOT VARY SIGNIFICANTLY FROM UNIT TO UNIT. THE PROCEDURE SHOWN IS
NOT VERY EFFICIENT.

THE RUNTIME SERVICES CAN TAKE MULTIPLE UNIT SPECIFICATIONS HOWEVER.

LET'S BUILD THE SAME TABLE USING THE MULTIPLE SPECIFICATION FEATURE.

```
        # UNITS (D) ?  8<CR>

        UNIT 1
        CSR ADDRESS (O) ?  160000<CR>
        SUB-DEVICE # (O) ?  0,1<CR>
        Q-FACTOR (O) 0 ?  1,0<CR>

        UNIT 3
        CSR ADDRESS (O) ?  160000<CR>
        SUB-DEVICE # (O) ?  2-5<CR>
        Q-FACTOR (O) 0 ?  0<CR>

        UNIT 7
        CSR ADDRESS (O) ?  160000<CR>
        SUB-DEVICE # (O) ?  6,7<CR>
        Q-FACTOR (O) 0 ?  1<CR>
```

AS YOU CAN SEE IN THE ABOVE DIALOGUE, THE RUNTIME SERVICES WILL BUILD AS MANY ENTRIES AS IT CAN WITH THE INFORMATION GIVEN IN ANY ONE PASS THROUGH THE QUESTIONS. IN THE FIRST PASS, TWO ENTRIES ARE BUILT SINCE TWO SUB-DEVICES AND Q-FACTORS WERE SPECIFIED. THE SERVICES ASSUME THAT THE CSR ADDRESS IS 160000 FOR BOTH SINCE IT WAS SPECIFIED ONLY ONCE. IN THE SECOND PASS, FOUR ENTRIES WERE BUILT. THIS IS BECAUSE FOUR SUB-DEVICES WERE SPECIFIED. THE "-" CONSTRUCT TELLS THE RUNTIME SERVICES TO INCREMENT THE DATA FROM THE FIRST NUMBER TO THE SECOND. IN THIS CASE, SUB-DEVICES 2, 3, 4 AND 5 WERE SPECIFIED. (IF THE SUB-DEVICE WERE SPECIFIED BY ADDRESSES, THE INCREMENT WOULD BE BY 2 SINCE ADDRESSES MUST BE ON AN EVEN BOUNDARY.) THE CSR ADDRESSES AND Q-FACTORS FOR THE FOUR ENTRIES ARE ASSUMED TO BE 160000 AND 0 RESPECTIVELY SINCE THEY WERE ONLY SPECIFIED ONCE. THE LAST TWO UNITS ARE SPECIFIED IN THE THIRD PASS.

THE WHOLE PROCESS COULD HAVE BEEN ACCOMPLISHED IN ONE PASS AS SHOWN BELOW.

```
        # UNITS (D) ?  8<CR>

        UNIT 1
        CSR ADDRESS (O) ?  160000<CR>
        SUB-DEVICE # (O) ?  0-7<CR>
        Q-FACTOR (O) 0 ?  0,1,0,,,,1,1<CR>
```

AS YOU CAN SEE FROM THIS EXAMPLE, NULL REPLIES (COMMAS ENCLOSING A NULL FIELD) TELL THE RUNTIME SERVICES TO REPEAT THE LAST REPLY.

2.7 QUICK START-UP PROCEDURE (XXDP+)

NOTE: THE T-11 POD MUST BE CONNECTED TO THE TARGET EMULATOR MODULE AND DISCONNECTED FROM THE TARGET SYSTEM BEFORE EXECUTION OF THIS DIAGNOSTIC.

TO START-UP THIS PROGRAM:

1. BOOT XXDP+

2. ANSWER ANY QUESTIONS ASKED AND GIVE THE DATE.

3. TYPE 'R NAME', WHERE NAME IS THE NAME OF THE BIN OR BIC FILE FOR THIS PROGRAM

4. TYPE 'START'

5. ANSWER THE 'CHANGE HW' QUESTION WITH 'Y'

6. ANSWER ALL THE HARDWARE QUESTIONS

7. ANSWER THE 'CHANGE SW' QUESTION WITH 'N'

WHEN YOU FOLLOW THIS PROCEDURE YOU WILL BE USING ONLY THE DEFAULTS FOR FLAGS AND SOFTWARE PARAMETERS. THESE DEFAULTS ARE DESCRIBED IN SECTIONS 2.3 AND 2.5.

3.0 ERROR INFORMATION

3.1 TYPES OF ERROR MESSAGES

THERE ARE THREE LEVELS OF ERROR MESSAGES THAT MAY BE ISSUED BY A DIAGNOSTIC: GENERAL, BASIC AND EXTENDED. GENERAL ERROR MESSAGES ARE ALWAYS PRINTED UNLESS THE 'IER' FLAG IS SET (SECTION 2.3). THE GENERAL ERROR MESSAGE IS OF THE FORM:

```
NAME  TYPE  NUMBER  ON UNIT NUMBER  TST NUMBER P .XXXXXX
ERROR MESSAGE
```

WHERE: NAME = DIAGNOSTIC NAME
TYPE = ERROR TYPE (SYS FATAL, DEV FATAL, HARD OR SOFT)
NUMBER = ERROR NUMBER
UNIT NUMBER = 0 - N (N IS LAST UNIT IN PTABLE)
TST NUMBER = TEST AND SUBTEST WHERE ERROR OCCURRED
PC:XXXXXX = ADDRESS OF ERROR MESSAGE CALL

BASIC ERROR MESSAGES ARE MESSAGES THAT CONTAIN SOME ADDITIONAL INFORMATION ABOUT THE ERROR. THESE ARE ALWAYS PRINTED UNLESS THE 'IER' OR 'IBE' FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL MESSAGE.

EXTENDED ERROR MESSAGES CONTAIN SUPPLEMENTARY ERROR INFORMATION SUCH AS REGISTER CONTENTS OR GOOD/BAD DATA. THESE ARE ALWAYS PRINTED UNLESS THE 'IER', 'IBE' OR 'IXE' FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL ERROR MESSAGE AND ANY ASSOCIATED BASIC ERROR MESSAGES.

3.2 SPECIFIC ERROR MESSAGES

WHEN AN ERROR IS REPORTED ON THE CONSOLE TERMINAL, THE USER SHOULD REFER TO THE PROGRAM LISTING FOR THE TEST SEQUENCE BEING PERFORMED AT THE TIME THE ERROR WAS DETECTED. THE 'PC' REPORTED IN THE ERROR MESSAGE INDICATES THE ADDRESS OF THE ERROR CALL. EACH STEP OF A TEST

IS DESCRIBED IN DETAIL TO HELP THE USER UNDERSTAND THE TEST SEQUENCE.
ONCE UNDERSTANDING THE TEST SEQUENCE, THE USER SHOULD BE ABLE TO
DETERMINE THE FAULT OR FAULTS WHICH COULD CAUSE THE ERROR.

THE ERROR PRINTOUTS WILL USE THE FOLLOWING WORDS TO INDICATE ERROR
INFORMATION. A DESCRIPTION OF THE WORDS PRINTED OUT ARE AS FOLLOWS:

REG:	ONE OF THE TARGET EMULATOR MODULE'S CONTROL REGISTERS
LOAD	DATA THAT WAS LOADED INTO THE CONTROL REGISTER OR EXPECTED DATA TO BE IN CONTROL REGISTER ON A READ
RFAD:	DATA THAT WAS READ FROM THE CONTROL REGISTER
GOOD:	EXPECTED CONTROL REGISTER DATA
BAD:	DATA 'READ" FROM THE CONTROL REGISTER
XXXXXX:	SIX OCTAL DIGITS INDICATING THE DATA FOR THE ABOVE WORDS

THERE ARE FIVE ERROR NUMBERS ASSOCIATED WITH THIS DIAGNOSTIC. THE ERROR
NUMBERS AND THEIR MEANINGS ARE DESCRIBED BELOW:

ERROR NUMBER 1 - ERROR DETECTED CHECKING CONTROL REGISTER 0
ERROR NUMBER 2 - ERROR DETECTED CHECKING CONTROL REGISTER 2
ERROR NUMBER 3 - ERROR DETECTED CHECKING CONTROL REGISTER 4
ERROR NUMBER 4 - ERROR DETECTED CHECKING CONTROL REGISTER 6
ERROR NUMBER 5 - ERROR DETECTED TRYING TO RUN THE T-11 CHIP

EXAMPLES OF EACH TYPE OF CONTROL REGISTER ERROR PRINTOUT ARE SHOWN BELOW:

** CONTROL REGISTER 0 ERROR MESSAGES **

```
CVCDC DVC FTL ERR 00001 ON UNIT 00 TST 001 SUB 000 PC: XXXXXX
GDAL 15:0 REG ERROR
CONTROL REG 0 ERROR
REG0 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX
```

THE ABOVE ERROR MESSAGE WILL BE PRINTED OUT FOR ALL CONTROL REGISTER 0
ERRORS EXCEPT THOSE ERRORS DETECTED WHILE TESTING THE TARGET EMULATOR
INTERRUPT LOGIC. IF AN ERROR WAS DETECTED WHILE CHECKING THE TARGET
EMULATOR INTERRUPT LOGIC, THE ABOVE ERROR MESSAGE WILL BE REPORTED,
HOWEVER, THE MESSAGE "GDAL 15:0 REG ERROR" WILL BE REPLACED WITH EITHER
"UNEXPECTED INTERRUPT OCCURED" OR "FAILED TO INTERRUPT". THE INFORMA-
TION PRINTED OUT FOR CONTROL REGISTER 0 MAY HELP THE USER IN DETERMIN-
ING THE ERROR, HOWEVER, THE GOOD AND BAD DATA MAY BE THE SAME, THEREFORE
REFER TO THE PROGRAM LISTING FOR THE TEST SEQUENCE BEING PERFORMED AT
THE TIME THE ERROR OCCURED.

```
TIME OUT ERROR ADDRESSING CONTROL REG 0
```

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS
CONTROL REGISTER 0 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR
#4.

** CONTROL REGISTER 2 ERROR MESSAGE **

```
CVCDC DVC FTL ERR 00002 ON UNIT 00 TST 004 SUB 000 PC: XXXXXX
ADAL 15:0 REG ERROR
CONTROL REG 2 ERROR
REG2 = LOAD: XXXXXX READ: XXXXXX
```

THE ABOVE ERROR MESSAGE WILL BE PRINTED FOR ALL CONTROL REGISTER 2
ERRORS EXCEPT A TIME OUT ERROR.

TIME OUT ERROR ADDRESSING CONTROL REG 2

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS
CONTROL REGISTER 2 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR
#4.

** CONTROL REGISTER 4 ERROR MESSAGE **

```
CVCDC DVC FTL ERR 00003 ON UNIT 00 TST 006 SUB 000 PC: XXXXXX
VDAL 7:0 OR PAUSE STATE MACHINE ERROR
CONTROL REG 4 ERROR
REG4 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX
```

THE ABOVE ERROR MESSAGE WILL BE REPORTED FOR ALL CONTROL REGISTER 4
ERRORS EXCEPT A TIME OUT ERROR.

TIME OUT ERROR ADDRESSING CONTROL REG 4

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS
CONTROL REGISTER 4 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR
#4.

** CONTROL REGISTER 6 ERROR MESSAGE **

THERE ARE THREE TYPES OF ERROR MESSAGES THAT ARE REPORTED FOR CONTROL
REGISTER 6 ERRORS WHICH ARE SHOWN BELOW.

```
CVCDC DVC FTL ERR 00004 ON UNIT 00 TST 008 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 - LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG6 - LOAD: XXXXXX READ: XXXXXX

CVCDC DVC FTL ERR 00004 ON UNIT 00 TST 021 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX

CVCDC DVC FTL ERR 00005 ON UNIT 00 TST 021 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX
```

IN THE ABOVE ERRORS, REFER TO THE LINE INDICATING "REG6 =" FOR CONTROL
REGISTER 6 ERROR INFORMATION. THE REMAINING CONTROL REGISTER INFORMA-
TION IS GIVEN TO INDICATE WHAT WAS LOADED INTO THOSE REGISTERS PREVIOUS
TO THE ERROR. THIS IS DONE TO AID THE USER IN DETERMINING THE FAULT
ON ERRORS WHICH NEED PREVIOUS CONTROL REGISTER SETUP.

IF THE NUMBER REPORTED FOR "DVC FTL ERR" WAS 00005, THEN THE ERROR OCCURED AS A RESULT OF THE PROGRAM TRYING TO TEST THE T-11 CHIP.

THE ERROR TYPE MESSAGE IN THE ABOVE ERROR REPORTS WILL BE ONE OF THOSE LISTED BELOW. THESE MESSAGES ARE REPORTED TO HELP THE USER IDENTIFY THE AREA OF LOGIC BEING TESTED IN WHICH THE ERROR WAS DETECTED. THESE ERROR TYPE MESSAGES ARE AS FOLLOWS:

HDAL 15:0 REG ERROR
MR 15:0 REG ERROR
FDAL 7:0 REG ERROR
EOAI 7:0 OR FDAL 7:0 REG ERROR
DIAG ADDR 15:0 REG ERROR
FORCE JUMP ADDRESS READBACK REG ERROR
INSTR REG TO EODAL BUS READBACK ERROR
MODE REG TO EODAL BUS READBACK ERROR
FORCE JUMP ADDRESS REG TO EODAL BUS READBACK ERROR
CTL 7:0 OR FDAL 7:0 REG ERROR
MODE REG TO EIDAL BUS READBACK ERROR
MODE REG TO TARGET MODE REG ERROR
MODE REG TO ADDRESS BUS READBACK ERROR
OLD FJA TO EIDAL BUS ERROR
OLD FJA TO ADDRESS BUS ERROR
OLD FJA TO TDAL LATCH EIDAL BUS ERROR
TDAL LATCH TO EIDAL TO DATA TO EODAL BUS ERROR
FDAL REG TO EODAL BUS ERROR
FDAL REG TO EODAL BUS TO EIDAL BUS ERROR
PAUSE STATE NOT ENTERED WHEN T-11 IS POWERED UP
FORCE JUMP ADDRESS NOT = EXPECTED T-11 START-RESTART ADDRESS

TIME OUT ERROR ADDRESSING CONTROL REG 6

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 0 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR #4.

4.0 PERFORMANCE AND PROGRESS REPORTS

AT THE END OF EACH PASS, THE PASS COUNT IS GIVEN ALONG WITH THE TOTAL NUMBER OF ERRORS REPORTED SINCE THE DIAGNOSTIC WAS STARTED. THE "EOP" SWITCH CAN BE USED TO CONTROL HOW OFTEN THE END OF PASS MESSAGE IS PRINTED. SECTION 2.2 DESCRIBES SWITCHES.

5.0 DEVICE INFORMATION TABLES

CONTROL REGISTER 0 (163010) - GDAL REGISTER

15	GDAL15	BIT 15 = 1 READ DEVICE TYPE IN BITS 15-8. TARGET EMULATOR DEVICE TYPE EQUALS 0 (0000) BIT 15 = 0 READ DEVICE NUMBER INTO BITS 15:8.
14	GDAL14	ALWAYS A 0 ON READ
13	GDAL13	ALWAYS A 0 ON READ

12 GDAL12 ALWAYS A 0 ON READ

BITS 11:8 ARE USED TO SELECT THE DEVICE NUMBER OF THE TARGET EMULATOR. THESE BITS MUST BE EQUAL TO THE SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.

11	GDAL11	DEVICE NUMBER/TYPE
10	GDAL10	DEVICE NUMBER/TYPE
9	GDAL9	DEVICE NUMBER/TYPE
8	GDAL8	DEVICE NUMBER/TYPE
7	GDAL7	SINGLE STEP BREAK INDICATOR (READ ONLY)
6	GDAL6	TIMEOUT BREAK INDICATOR (READ ONLY)
5	GDAL5	MEMORY SIMULATOR BREAK INDICATOR (READ ONLY)
4	GDAL4	STATE ANALYZER BREAK INDICATOR (READ ONLY)
3	GDAL3	TARGET EMULATOR INTERRUPT ENABLE (R/W)
2	GDAL2	POINTER FOR EXTENDED REGISTER SELECT (R/W)
1	GDAL1	POINTER FOR EXTENDED REGISTER SELECT (R/W)
0	GDAL0	POINTER FOR EXTENDED REGISTER SELECT (R/W)

EXTENDED REGISTER SELECTED VIA GDAL BITS 2:0

GDAL2	GDAL1	GDAL0	REGISTER SELECTED VIA R/W TO CONTROL REGISTER 6
0	0	0	WRITE DIAGNOSTIC ADDRESS REGISTER READBACK OF ADDRESS BUS
0	0	1	WRITE NEW FORCE JUMP ADDRESS REGISTER READBACK OF FORCE JUMP ADDRESS READBACK REG
0	1	0	WRITE FDAL AND EOAI REGISTER READBACK OF FDAL/EOAI OR FDAL/CTL REG
0	1	1	R/W HDAL REGISTER
1	0	0	R/W MODE REGISTER
1	0	1	READBACK OF TARGET MODE REGISTER
1	1	0	READBACK OF EIDAL BUS
1	1	1	READBACK OF EODAL BUS

CONTROL REGISTER 2 (163012) - ADAL REGISTER

15	ADAL15	SELECT COLUMN AI FOR STATE ANALYZER (1)
14	ADAL14	SELECT ROW/COLUMN AI FOR STATE ANALYZER (1) SELECT SERVICE AI FOR STATE ANALYZER (0)
13	ADAL13	ENABLE SERVICE FROM TARGET EMULATOR (1) ENABLE SERVICE FROM THE TARGET (0)
12	ADAL12	ENABLE MODE FROM TARGET EMULATOR (1) ENABLE MODE FROM THE TARGET (0)
11	ADAL11	DISABLE SERVICE TO THE TARGET (1) ENABLE SERVICE TO THE TARGET (0)
10	ADAL10	MASTER SWITCH
9	ADAL9	ENABLE STATE ANALYZER CLOCKS (1)
8	ADAL8	ENABLE TIMEOUT BREAK (1) DISABLE TIMEOUT BREAK (0)
7	ADAL7	ENABLE REFRESH TO STATE ANALYZER (1) DISBALE REFRESH TO STATE ANALYZER (0)
6	ADAL6	SPARE
5	ADAL5	ENABLE SINGLE STEP BREAK (1) DISABLE SINGLE STEP BREAK (0)

4	ADAL4	ENABLE PAUSE STATE TO RUN MODE (1) ENABLE PAUSE STATE TO PAUSE MODE (0)
3	ADAL3	POWER UP FROM TARGET (1)
2	ADAL2	POWER UP FROM TARGET EMULATOR
1	ADAL1	SELECT TARGET EMULATOR CRYSTAL CLOCK (1) SELECT CLOCK FROM THE STATE ANALYZER (0)
0	ADAL0	RESET BREAK LOGIC - ZEROES BREAK LATCH FLIP-FLOP, SINGLE STEP BREAK FLIP-FLOP AND MEMORY SIMULATOR BREAK LATCH FLIP-FLOP

CONTROL REGISTER 4 (163014) - VDAL REGISTER

15	VDAL15	TNFJ H - TAKE NEW FORCE JUMP ADDRESS F/F (READ)
14	VDAL14	EP8N H - 8 BIT ADDRESS HB F/F (READ)
13	VDAL13	EP8G H - 8 BIT ADDRESS LB F/F (READ)
12	VDAL12	EP8F H - 8 BIT INSTRUCTION HB F/F (READ)
11	VDAL11	EPFN H - 16 BIT ADDRESS F/F (READ)
10	VDAL10	EPSF H - PAUSE STATE SYNC F/F (READ)
9	VDAL9	PSMW H - PAUSE STATE WORKING F/F (READ)
8	VDAL8	OUTNEW H - GET NEW ADDRESS F/F (READ)
7	VDAL7	DIAGNOSTIC FETCT H (READ/WRITE)
6	VDAL6	MSDI H - DATA IN LOGIC LEVEL (READ)
5	VDAL5	BTS1 H -
4	VDAL4	EDEOC H - LOGIC LEVEL OF STATE ANALYZER CLOCK (READ)
3	VDAL3	READ H - LOGIC LEVEL OF REAT H (READ)
2	VDAL2	DIAGNOSTIC RESET OF THE TARGET EMULATOR MODULE AND CLOCKS THE TAI AND TDAL LATCHES (READ/WRITE)
1	VDAL1	SPARE (READ/WRITE)
0	VDAL0	ENABLE TAI AND TDAL READBACK FROM POD (READ/WRITE)

CONTROL REGISTER 6 (163016) - FDAL REIGSTER (EOAI/CTL ON FDAL 15:8)

7	FDAL7	INTERRUPT VECTOR
6	FDAL6	INTERRUPT VECTOR
5	FDAL5	INTERRUPT VECTOR
4	FDAL4	INTERRUPT VECTOR
3	FDAL3	INTERRUPT VECTOR
2	FDAL2	INTERRUPT VECTOR
1	FDAL1	SPARE
0	FDAL0	SELECT EOAI REG TO BE READBACK ON FDAL BITS 15:8 (1) SELECT CTL REG TO BE READBACK ON FDAL BITS 15:8 (0)

CONTROL REGISTER 6 (163016) - HDAL REGISTER - DIAGNOSTIC CONTROL BITS

15	HDAL15	DIAGNOSTIC CONTROL OF PPI L WHEN HDAL2 EQUALS A ONE
14	HDAL14	DIAGNOSTIC CONTROL OF EIDAL17 H WHEN HDAL2 EQUALS A ONE
13	HDAL13	DIAGNOSTIC CONTROL OF PCAS H WHEN HDAL2 EQUALS A ONE
12	HDAL12	DIAGNOSTIC CONTROL OF PRAS H WHEN HDAL2 EQUALS A ONE
11	HDAL11	DIAGNOSTIC CONTROL OF EIDAL16 H WHEN HDAL2 EQUALS A ONE
10	HDAL10	SPARE
9	HDAL9	ENABLE DIAGNOSTIC ADDRESS REGISTER TO ADDRESS BUS
8	HDAL8	DIAGNOSTIC CONTROL OF CREADY L WHEN HDAL2 EQUALS A ONE
7	HDAL7	DIAGNOSTIC CONTROL OF PBCLR H WHEN HDAL2 EQUALS A ONE
6	HDAL6	DIAGNOSTIC CONTROL OF PSEL1 L WHEN HDAL2 EQUALS A ONE
5	HDAL5	DIAGNOSTIC CONTROL OF PSEL0 L WHEN HDAL2 EQUALS A ONE
4	HDAL4	DIAGNOSTIC CONTROL OF PR/WHB L WHEN HDAL2 EQUALS A ONE

3	HDAL3	DIAGNOSTIC CONTROL OF PR/WLB L WHEN HDAL2 EQUALS A ONE
2	HDAL2	ENABLES PROGRAM TO GENERATE T-11 SIGNALS LISTED IN HDAL (1) ENABLES T-11 TO GENERATE T-11 SIGNALS LISTED IN HDAL (0)
1	HDAL1	SPARE
0	HDAL0	DIAGNOSTIC CONTROL OF MSDI H WHEN HDAL2 EQUALS A ONE

CONTROL REGISTER 6 (163016) - MODE REGISTER

15	MR15	T-11 START/RESTART ADDRESS SELECT
14	MR14	T-11 START/RESTART ADDRESS SELECT
13	MR13	T-11 START/RESTART ADDRESS SELECT
12	MR12	T-11 USER MODE (1) T-11 TESTER MODE (0)
11	MR11	SELECT 8 BIT BUS (1) SELECT 16 BIT BUS (0)
10	MR10	T-11 DYNAMIC MODE ONLY - SELECTS 4K/16K (1) T-11 DYNAMIC MODE ONLY - SELECTS 64K (0)
9	MR9	T-11 STATIC MEMORY SELECT (1) T-11 DYNAMIC MEMORY SELECT (0)
8	MR8	T-11 DELAYED READ/WRITE SELECT (1) T-11 NROMAL READ/WRITE SELECT (0)
7	MR7	NOT DEFINED
6	MR6	NOT DEFINED
5	MR5	NOT DEFINED
4	MR4	NOT DEFINED
3	MR3	NOT DEFINED
2	MR2	NOT DEFINED
1	MR1	T-11 STANDARD MICROCYCLE (1) T-11 LONG MICROCYCLE (0)
0	MR0	T-11 PROCESSOR CLOCK (1) T-11 CONSTANT CLOCK (0)

6.0 TEST SUMMARIES

TEST 1:

THIS TEST WILL CHECK THAT THE TARGET EMULATOR MODULE CAN BE SELECTED AND INITIALIZED TO A KNOWN STATE. THE TEST DESCRIBED BELOW WILL BE EXECUTED AT THE BEGINNING OF EACH TEST TO PUT THE TARGET EMULATOR MODULE IN A KNOWN STATE.

THE TEST WILL LOAD AND CHECK THAT THE DEVICE NUMBER CAN BE LOADED INTO AND READ FROM CONTROL REGISTER 0. ALL THE READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES. THE TEST WILL CHECK THAT THE TARGET EMULATOR DEVICE TYPE CAN BE READ BY SETTING CONTROL REGISTER 0 BIT 15 TO A ONE AND THEN READING CONTROL REGISTER 0. THE TEST WILL SET CONTROL REGISTER BIT 15 TO A ZERO AND BITS 1 AND 0 TO ONES. BIT15 ON A ZERO WILL ENABLE THE DEVICE NUMBER TO BE READ AGAIN. BITS 1 AND 0 SET TO ONES WILL CAUSE THE HDAL REGISTER TO BE SELECTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6. THE TEST WILL NOW LOAD, READ AND CHECK THE HDAL REGISTER WITH HDAL2 SET TO A ONE AND ALL OTHER HDAL BITS CLEARED. HDAL2 SET TO A ONE WILL ENABLE THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS USING HDAL REGISTER BITS. THE TEST WILL NOW SET CONTROL REGISTER 0 BITS 1 AND 0 TO ZEROES AND SET BIT 2 TO A ONE. CONTROL REGISTER 0 BIT 2 ON A ONE WILL CAUSE THE MODE REGISTER TO BE SELECTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6. THE TEST WILL LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES. MODE REGISTER BIT 11 ON A ZERO WILL CAUSE 16 BIT ADDRESS MODE TO BE SELECTED. THE TEST WILL SET ADAL REGISTER BIT 0 TO A ONE AND THEN ZERO. ALL

OTHER ADAL REGISTER BITS WILL BE LOADED AND CHECKED FOR ZEROES. ADAL0 BEING SET TO A ONE WILL CLEAR THE BREAK LATCH FLIP-FLOP, THE SINGLE STEP BREAK FLIP-FLOP, AND THE MEMORY SIMULATOR BREAK FLIP-FLOP. ADAL REGISTER BIT 2 ON A ZERO WILL CAUSE THE T-11 TO BE TURNED OFF. THE TEST WILL THEN READ AND CHECK CONTROL REGISTER 0 TO CHECK THAT ALL THE BREAK INDICATOR BITS ARE CLEARED. THE TEST WILL NOW SET VDAL REGISTER BIT 2 TO A ONE AND THEN A ZERO. ALL OTHER VDAL READ/WRITE BITS WILL BE LOADED AND CHECKED FOR ZEROES. VDAL REGISTER BIT 2 ON A ONE WILL CAUSE ALL THE FLIP-FLOPS ON THE TARGET EMULATOR MODULE, EXCEPT THOSE INITIALIZED BY ADAL0, TO BE SET TO A KNOWN STATE.

TEST 2:

THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS, GDAL 3:0, CAN BE SET TO ALL ONES (17), AND THEN SET TO ALL ZEROES. THE READ ONLY BITS, GDAL7:4, ARE CHECKED TO BE CLEARED DURING THIS TEST.

TEST 3:

THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS GDAL 3:0, CAN BE LOADED WITH ONES AND ZEORES (12) AND THEN LOADED WITH ZEROES AND ONES (5). THE READ ONLY BITS GDAL 7:4 ARE CHECKED TO BE CLEARED DURING THIS TEST.

TEST 4:

THIS TEST WILL CHECK CONTROL REGISTER 0 R/W BITS USING A BINARY COUNT PATTERN. THE PATTERN WILL START INITIALLY AT 0 AND INCREMENT BY ONE UNTIL THE PATTERN EQUALS 17. THE READ ONLY BITS, GDAL 7:4, ARE CHECKED TO BE CLEARED DURING THIS TEST.

TEST 5:

THIS TEST WILL CHECK THAT CONTROL REGISTER 2 BITS ADAL 15:0 CAN BE SET TO ALL ONES (177777) AND THEN ALL ZEORES (000000).

TEST 6:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 15:0 WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN WITH AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TEST 7:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 7:0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH A PATTERN OF 0 AND INCREMENT TO 377 BY AN INCREMENT OF ONE.

TEST 8:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 15:8 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH A PATTERN OF 0 AND INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED.

TEST 9:

THIS TEST WILL CHECK THAT CONTROL REGISTER 4 READ/WRITE BITS VDAL7, VDAL2, VDAL1 AND VDAL0 CAN BE SET AND CLEARED. THE TEST WILL CHECK THESE BITS

USING A DECREMENTING BINARY COUNT PATTERN. THE READ ONLY BITS WILL BE CHECKED TO BE ZEROES DURING THIS TEST. READ ONLY BITS VDAL 15:8 SHOULD BE ZERO AS A RESULT OF VDAL2 H BEING SET TO A ONE DURING THIS TEST. READ ONLY BITS 6:3 SHOULD BE A ZERO AS A RESULT OF ADAL BIT 10 BEING A ZERO. THE ADAL REGISTER WAS CLEARED IN THE ABOVE ROUTINE "INITTE".

TEST 10:

THIS TEST WILL CHECK THAT HDAL REGISTER BITS 15:0 CAN BE SET TO ALL ONES (177777) AND THEN TO ALL ZEROES (000000). TO SELECT THE HDAL REGISTER, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, PULSES WILL OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H. THESE PULSES WILL CAUSE THE DATA ON THE WRITE COMMAND TO BE LOADED INTO THE HDAL REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, A PULSE WILL OCCUR ON THE SIGNAL RPT3 L. THIS SIGNAL WILL CAUSE THE HDAL REGISTER TO BE READBACK.

TEST 11:

THIS TEST WILL CHECK THAT HDAL REGISTER BITS 15:0 CAN BE LOADED WITH AN ALTERNATING ONE AND ZEROES DATA PATTERN (125252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525). TO SELECT THE HDAL REGISTER, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, PULSES WILL OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H. THESE PULSES WILL CAUSE THE DATA ON A WRITE COMMAND TO BE LOADED INTO THE HDAL REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, A PULSE WILL OCCUR ON THE SIGNAL RPT3 L. THIS SIGNAL WILL CAUSE THE HDAL REGISTER TO BE READBACK.

TEST 12:

THIS TEST WILL CHECK THE LOW BYTE OF THE HDAL REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS BEEN LOADED INTO THE HDAL REGISTER. THE BITS BEING TESTED ARE HDAL BITS 7:0. TO SELECT THE HDAL REIGSTER, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE HDAL REGISTER VIA THE SIGNAL RPT3 L.

TEST 13:

THIS TEST WILL CHECK THE HIGH BYTE OF THE HDAL REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED INTO THE HDAL REGISTER. THE BITS BEING TESTED ARE HDAL BITS 15:8. TO SELECT THE HDAL REIGSTER, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE HDAL REGISTER VIA THE SIGNAL RPT3 L.

TEST 14:

THIS TEST WILL CHECK THAT MODE REGISTER BITS 15:0 CAN BE SET TO ALL ONES (177777) AND THEN TO ALL ZEROES (000000). TO SELECT THE MODE REGISTER, THE

TEST WILL SET GDAL2 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE, PULSES WILL BE OCCUR ON THE SIGNALS WPT4 LB H AND WPT4 HB H. THESE PULSE WILL CAUSE THE DATA ON THE WRITE COMMAND TO BE LOADED INTO THE MODE REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET IN CONTROL REGISTER 0, A PULSE WILL OCCUR ON THE SIGNAL RPT4 L. THIS SIGNAL WILL CAUSE THE MODE REGISTER TO BE READBACK

TEST 15:

THIS TEST WILL CHECK THAT MODE REGISTER BITS 15:0 CAN BE LOADED WITH AN ALTERNATING ONE AND ZEROES DATA PATTERN (125252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525). TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 IN THE LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE IN REG 0, PULSES WILL OCCUR ON THE SIGNALS WPT4 LB H AND WPT4 HB H. THESE PULSES WILL CAUSE THE DATA ON A WRITE COMMAND TO BE LOADED INTO THE MODE REGISTER. ON A READ COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE, A PULSE WILL OCCUR ON THE SIGNAL RPT4 L. THIS SIGNAL WILL CAUSE THE MODE REGISTER TO BE READBACK.

TEST 16:

THIS TEST WILL CHECK THE LOW BYTE OF THE MODE REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS BEEN LOADED INTO THE MODE REGISTER. THE BITS BEING TESTED ARE MR BITS 7:0. TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 TO A 1 IN LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTRO REGISTER 6, DATA WILL BE LOADED INTO THE MODE REGISTER VIA THE SIGNALS WP - LB H AND WPT4 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE MODE REGISTER VIA THE SIGNAL RPT4 L.

TEST 17:

THIS TEST WILL CHECK THE HIGH BYTE OF THE MODE REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED INTO THE MODE REGISTER. THE BITS BEING TESTED ARE MR BITS 15:8. TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 TO A 1 IN LOW BYTE OF CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE MODE REGISTER VIA THE SIGNALS WPT4 LB H AND WPT4 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE MODE REGISTER VIA THE SIGNAL RPT4 L.

TEST 18:

THIS TEST WILL CHECK THAT FDAL REGISTER BITS 7:0 CAN BE SET TO ALL ONES (377) AND THEN TO ALL ZEROES (000). TO SELECT THE FDAL REGISTER, THE TEST WILL SET GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO FDAL REGISTER BITS 7:0 VIA THE SIGNAL WPT2 LB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE FDAL REGISTER VIA THE SIGNAL RPT2 L. THE HIGH BYTE, WHICH IS ANOTHER REGISTER, WILL BE IGNORED DURING THIS TEST.

TEST 19:

THIS TEST WILL CHECK THAT FDAL REGISTER BITS 7:0 CAN BE LOADED WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (125). TO SELECT THE FDAL REGISTER, THE TEST WILL SET THE SIGNAL

GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO FDAL REGISTER BITS 7:0 VIA THE SIGNAL WPT2 LB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE FDAL REGISTER VIA THE SIGNAL RPT2 L. THE HIGH BYTE, WHICH IS ANOTHER REGISTER, WILL BE IGNORED DURING THIS TEST.

TEST20:

THIS TEST WILL CHECK FDAL REGISTER BITS 7:0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START AT 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS BEEN LOADED INTO THE FDAL REGISTER. TO SELECT THE FDAL REGISTER, THE TEST WILL SET GDAL1 TO A ONE IN CONTROL REGISTER 0. ON A WRITE COMMANND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE FDAL REG VIA THE SIGNAL WPT2 LB H. ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE FDAL REG VIA THE SIGNAL RPT2 L.

TEST 21:

THIS TEST WILL CHECK EOAI REGISTER BITS 7:0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH ZERO AND INCREMENT BY ONE UNTIL A PATTERN OF ALL ONES HAS BEEN LOADED INTO THE EOAI REGISTER AND CHECKED. THE EOAI REGISTER IS THE HIGH BYTE OF THE FDAL REGISTER. DATA IS LOADED INTO THE EOAI REGISTER VIA THE SIGNAL WPT2 HB H WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE FDAL REGISTER IS SELECTED VIA GDAL BITS 2:0. TO READ THE EOAI BUS, THE PROGRAM WILL SET FDAL0 H TO A ONE TO SELECT THE EOAI BUS TO BE READ INSTEAD OF THE CTL BUS. THE EOAI BUS IS READ BACK TO THE LSI-11 VIA THE SIGNAL RAT2 L WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE FDAL REGISTER IS SELECTED.

TEST 22:

THIS TEST WILL CHECK THAT THE DIAGNOSTIC ADDRESS REGISTER BITS ADDR 15:0 CAN BE LOADED WITH ALL ONES (177777) AND THEN ALL ZEROES (000000).
.
TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAGNOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER, 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAGNOSTIC ADDRESS REGISTER.

TEST 23:

THIS TEST WILL CHECK THAT THE DAIGNOSTIC ADDRESS REGISTER BITS ADDR 15:0 CAN BE LOADED WITH AN ALTERNATING ONES AND ZEROES DATA PATERRN (125252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
.
TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL

SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAGNOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAGNOSTIC ADDRESS REGISTER.

TEST 24:

THIS TEST WILL CHECK THE LOW BYTE OF THE DIAGNOSTIC ADDRESS REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS BEEN LOADED INTO DIAGNOSTIC ADDRESS REGISTER BITS ADDR 7:0. THE HIGH BYTE OF THE DIAGNOSTIC ADDRESS REGISTER WILL BE LOADED WITH ZEROES DURING THIS TEST.
:
TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAGNOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAGNOSTIC ADDRESS REGISTER.

TEST 25:

THIS TEST WILL CHECK THE HIGH BYTE OF THE DIAGNOSTIC ADDRESS REGISTER USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED INTO DIAGNOSTIC ADDRESS REGISTER BITS ADDR 15:8. THE LOW BYTE OF THE DIAGNOSTIC ADDRESS REGISTER WILL BE LOADED WITH ZEROES DURING THIS TEST.
:
TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0. ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L. TO SELECT THE DIAGNOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H AND WPT0 HB H. ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAGNOSTIC ADDRESS REGISTER.

TEST 26:

THIS TEST WILL CHECK THAT THE MODE REGISTER CAN BE READBACK ON THE EODAL BUS. THE MODE REGISTER WILL BE LOADED WITH THE FOLLOWING PATTERNS: 125252,052525,

177400, 000377, 177777, AND 0000000. FOR EACH PATTERN LOADED THE TEST WILL ENABLE THE MODE REGISTER ONTO THE EODAL BUS AND READ AND CHECK THE EODAL BUS FOR THE CORRECT MODE REGISTER PATTERN. THE MODE REGISTER WILL BE ENABLED TO THE EODAL BUS WHEN ADAL12 H IS SET TO A ONE AND THE SIGNAL XBCLR H IS ASSERTED HIGH.

TEST 27:

THIS TEST WILL CHECK THE FORCE JUMP ADDRESS READBACK REGISTER WITH THE FOLLOWING DATA PATTERNS 125252, 052525, 177400, 000377 , 1777777, AND 000000. THE DIAGNOSTIC ADDRESS REGISTER WILL PROVIDE THE DATA ON THE ADDRESS BUS TO THE FORCE JUMP ADDRESS REGISTER AND FORCE JUMP ADDRESS READBACK REGISTER.

TEST 28:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 16 BIT ADDRESS MODE. THE PAUSE STATE MACHINE FLIP-FLOPS , PAUSE STATE WORKING , AND PAUSE STATE SYNC AND 16 BIT ADDRESS WILL BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO AND ADAL0 H WILL BE SET TO A ONE DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK AND ADAL0 H ON A ONE WILL CLEAR THE BREAK LOGIC, THUS SETTING THE SIGNAL BRK H TO A ZERO.

THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE OLD FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS. THE OLD FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125252, 052525 177400, 000377, 177777, AND 000000. THE OLD FORCE JUMP ADDRESS REGISTER GETS ITS DATA FROM THE DIAGNOSTIC ADDRESS REGISTER WHICH IS ENABLED ON THE ADDRESS BUS DURING THIS TEST.

TEST 29:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 16 BIT ADDRESS MODE. THE PAUSE STATE MACHINE FLIP - FLOP'S , PAUSE STATE WORKING , PAUSE STATE SYNC AND 16 BIT ADDRESS WILL BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO AND ADAL0 H WILL BE SET TO A ONE DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK AND ADAL0 H ON A ONE WILL CLEAR THE BREAK LOGIC, THUS SETTING THE SIGNAL BRK H TO A ZERO.

THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE NEW FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS. THE NEW FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125252, 052525 177400, 000377, 177777, AND 000000. THE NEW FORCE JUMP ADDRESS REGISTER IS LOADED AT THE BEGINNING OF THE TEST.

TEST 30:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN "RUN" AND 16 BIT ADDRESS MODE. WHEN THE PAUSE STATE MACHINE IS SETUP IN "RUN" MODE VIA ADAL4 H ON A ONE AND A PULSE ON THE SIGNAL XRAS H, THE PAUSE STATE MACHINE CAN ONLY BE ENTERED WHEN A BREAK CONDTION IS RECEIVED ON THE SIGNAL "BRK H". THIS TEST WILL USE THE

TIMEOUT BREAK ONE SHOT TO GENERATE THE BREAK CONDITION. THE TEST WILL CHECK THAT THE PAUSE STATE MACHINE IS NOT ENTERED WHEN NO BREAK CONDITION IS RECEIVED AND THAT IT IS ENTERED WHEN A BREAK CONDITION IS RECEIVED. THE TEST WILL CHECK ALL THE PAUSE STATE LOGIC ASSOCIATED WITH THE SIGNAL 'BRK H'. THE TEST WILL CHECK THAT THE SIGNAL ''TOBRK H'' IS SET IN CONTROL REGISTER 0 WHEN THE TIME OUT BREAK ONE SHOT IS NOT BEING FIRED AND THAT IT IS NOT SET WHEN THE TIME OUT BREAK ONE SHOT IS BEING FIRED.

TEST 31:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN ''RUN'' AND 16 BIT ADDRESS MODE. WHEN THE PAUSE STATE MACHINE IS SETUP IN 'RUN'' MODE VIA ADAL4 H ON A ONE AND A PULSE ON XRAS H, THE PAUSE STATE MACHINE CAN ONLY BE ENTERED WHEN A BREAK CONDITION IS RECEIVED ON THE SIGNAL 'BRK H''. THIS TEST WILL USE THE SINGLE STEP BREAK FLIP-FLOP TO GENERATE THE BREAK CONDITION. THE TEST WILL CHECK THAT THE PAUSE STATE MACHINE IS NOT ENTERED WHEN THE SINGLE STEP BREAK FLIP-FLOP IS CLEARED AND THAT IT CAN BE ENTERED WHEN THE SINGLE STEP BREAK FLIP-FLOP IS SET TO A ONE. THE TEST WILL CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP ONCE SET, WILL REMAIN LATCHED TO THE SET STATE UNTIL CLEARED BY A PULSE BEING ISSUED ON THE SIGNAL 'BRKRES L''. THE TEST WILL SET THE PAUSE STATE MACHINE FLIP-FLOP'S: PAUSE STATE WORKING, PAUSE STATE SYNC AND 16 BIT ADDRESS VIA THE SIGNALS XRAS H AND XCAS H. ONCE ALL THESE FLIP-FLOPS ARE SET TO THE ONE STATE, THE TEST WILL CHECK THAT THEY CAN BE CLEARED BY ISSUING A PULSE ON THE SIGNAL ''INVD L''.

TEST 32:

THIS TEST WILL CHECK THAT THE EDFET FLIP-FLOP CAN BE CLEARED WHEN A PULSE IS ISSUED OF THE SIGNAL XPI L. THE TEST WILL SET ADAL4 H TO A ZERO TO CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE PAUSE MODE WHEN A PULSE IS ISSUED ON THE SIGNAL XRAS H. THE TEST WILL SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE. THE TEST WILL THEN PULSE XRAS H TO SET THE EDFET FLIP-FLOP TO A ONE AND TO SET THE PAUSE MODE FLIP-FLOP TO THE PAUSE MODE. WHEN EDFET FLIP-FLOP IS SET TO A ONE AND THE PAUSE MODE FLIP-FLOP IS SET TO THE PAUSE MODE, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE. THE TEST WILL NOW PULSE THE SIGNAL XPI L TO CLEAR THE EDFET FLIP-FLOP. WHEN THE EDFET FLIP-FLOP IS CLEARED, THE SIGNAL PB H WILL BE ASSERTED LOW. THE SIGNAL PB H IS THE DATA INPUT LEAD TO THE PAUSE STATE WORKING FLIP-FLOP. THE TEST WILL NOW PULSE THE SIGNAL XCAS H. WHEN A PULSE IS ISSUED ON THE SIGNAL XCAS H AND THE SIGNAL PB H IS ASSERTED LOW, THE PAUSE STATE SYNC FLIP-FLOP WILL BE CLOCKED TO A ZERO. THE SIGNAL XCAS H WILL ALSO CLOCK THE PAUSE STATE WORKING FLIP-FLOP TO A ONE.

TEST 33:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 8 BIT ADDRESS MODE. THE PAUSE STATE WORKING FLIP - FLOP'S , PAUSE STATE WORKING , PAUSE STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB AND 8 BIT ADDRESS HB WILL BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND AND ADAL8 H WILL BE SET TO A ZERO DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK. ADAL0 H WILL BE SET AND CLEARED TO CLEAR THE BREAK LOGIC. WITH THE TIMEOUT BREAK DISABLED AND THE BREAK LOGIC CLEARED, THE SIGNAL BRK H WILL BE A ZERO. MR BIT 11 WILL BE SET TO A ONE IN THE MODE REGISTER TO ENABLE 8 BIT ADDRESS MODE.

THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE OLD FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS IN 8 BIT ADDRESS MODE. THE OLD FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125125, 052652, 000377, 177400, 125252, 052525, 177777, AND 000000. THE OLD FORCE JUMP ADDRESS REGISTER GETS ITS DATA FROM THE DIAGNOSTIC ADDRESS REGISTER WHICH IS ENABLED TO THE ADDRESS BUS DURING THIS TEST.

TEST 34:

THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 8 BIT ADDRESS MODE. THE PAUSE STATE MACHINE FLIP - FLOP'S, PAUSE STATE WORKING, PAUSE STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB AND 8 BIT ADDRESS HB WILL BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H. THE SIGNALS ADAL4 H AND AND ADAL8 H WILL BE SET TO A ZERO DURING THIS TEST. ADAL4 H ON A ZERO WILL PUT THE PAUSE STATE MACHINE IN PAUSE MODE. ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK. ADAL0 H WILL BE SET AND CLEARED TO CLEAR THE BREAK LOGIC. WITH THE TIMEOUT BREAK DISABLED AND THE BREAK LOGIC CLEARED, THE SIGNAL BRK H WILL BE A ZERO. MR BIT 11 WILL BE SET TO A ONE IN THE MODE REGISTER TO ENABLE 8 BIT ADDRESS MODE.

THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE NEW FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS IN 8 BIT ADDRESS MODE. THE NEW FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125125, 052652, 000377, 177400, 125252, 052525, 177777, AND 000000. THE NEW FORCE JUMP ADDRESS REGISTER IS LOADED WITH THE DATA AT THE BEGINNING OF THE TEST.

TEST 35:

THIS TEST WILL CHECK THAT THE PAUSE STATE MACHINE FLIP - FLOPS, PAUSE STATE WORKING, PAUSE STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB, AND 8 BIT ADDRESS HB, CAN BE CLEARED WHEN THE SIGNAL VDAL2 H IS ASSERTED HIGH. ALL THE ABOVE FLIP-FLOPS ARE SET TO A ONE BY SETTING THE SIGNAL FETCT H TO A ONE, SETTING THE SIGNAL ADAL4 H TO A ZERO, AND PULSING THE SIGNALS XRAS H AND XCAS H. ONCE ALL THE FLIP-FLOPS ARE SET TO ONES, THE TEST WILL SET THE SIGNAL VDAL2 H AND CHECK THAT ALL THE PAUSE STATE MACHINE FLIP-FLOPS CLEARED.

TEST 36

THIS TEST WILL CHECK THAT THE EOAI REGISTER BITS 7:0 CAN BE LOADED AND READ BACK CORRECTLY. THE TEST WILL ALSO CHECK THE DATA PATH TO BE CONNECTED AND FUNCTIONING PROPERLY FROM THE EOAI REGISTER TO THE EOAI BUS, TO THE CAI BUS, TO THE EIAI BUS, TO THE CTL BUS AND INTO THE CTL REGISTER. THE TEST WILL CHECK THE DATA PATH FROM THE EOAI REGISTER TO THE EOAI BUS, TO THE CAI BUS, TO THE TAI BUS, TO THE TAI DIAGNOSTIC LATCH, AND BACK FROM THE TAI DIAGNOSTIC LATCH TO THE CAI BUS, TO THE EIAI BUS, TO THE CTL BUS AND INTO THE CTL REGISTER. THE DATA PATTERN USED DURING THIS TEST WILL BE AN INCREMENTING BINARY COUNT PATTERN. THE DATA READBACK FROM THE CTL REGISTER WILL BE THE ONES COMPLEMENT OF THE DATA LOADED INTO THE EOAI REGISTER.

TEST 37:

THIS TEST WILL CHECK THE DATA PATH FROM THE MODE REGISTER TO THE ADDRESS BUS.

TO DO THIS, THE TEST WILL ENABLE THE DATA PATH FROM THE MODE REGISTER TO THE EODAL BUS, TO THE CDAL BUS, TO THE EIDAL BUS, AND TO THE ADDRESS BUS. THIS IS DONE BY SETTING XBCLR H AND PBCLR H TO THE HIGH STATE AND BY SETTING ADAL12 H AND ADAL10 H TO ONES. THE TARGET MODE READBACK REGISTER WILL ALSO BE CHECKED TO HAVE BEEN LOADED WITH THE EIDAL BUS DATA WHEN THE SIGNAL XBCLR L IS SET TO THE HIGH STATE FROM THE LOW STATE. THE MODE REGISTER WILL BE LOADED WITH THE FOLLOWING DATA PATTERNS, 146063, 031714, 125252, 052525, 177777 AND 000000. FOR EACH DATA PATTERN LOADED, THE PROGRAM WILL CHECK THE DATA TO BE PRESENT ON THE THE EODAL BUS, THE EIDAL BUS, AND THE ADDRESS BUS. THE TEST WILL ALSO CHECK THAT EACH PATTERN CAN BE LOADED INTO THE TARGET MODE READBACK REGISTER.

TEST 38:

THIS TEST WILL CHECK THE DATA PATH FROM THE DIAGNOSTIC ADDRESS REGISTER TO THE OLD FORCE JUMP ADDRESS REGISTER, TO THE EODAL BUS, TO THE EIDAL BUS, AND TO THE ADDRESS BUS. THIS PART OF THE TEST USES THE PAUSE STATE MACHINE LOGIC TO LOAD THE OLD FORCE JUMP ADDRESS REGISTER AND TO PLACE THE OLD FORCE JUMP ADDRESS REGISTER DATA ONTO THE EODAL BUS. WHEN THE OLD FORCE JUMP ADDRESS REGISTER DATA IS ENABLED TO THE EODAL BUS, THE TEST WILL ENABLE THE DATA TO THE TDAL BUS AND LATCH THE DATA INTO THE TDAL DIAGNOSTIC LATCHES. THE NEXT PART OF THE TEST WILL CHECK THAT THE TDAL DIAGNOSTIC LATCHES CAN BE ENABLED TO THE EIDAL BUS AND THAT THE EIDAL BUS CAN BE ENABLED TO THE EODAL BUS THROUGH THE DATA BUS.

TEST 39:

THIS TEST WILL CHECK THAT THE FDAL REGISTER CAN BE ENABLED TO THE EODAL BUS VIA THE SIGNAL INTER L AND THAT THE EODAL BUS CAN BE ENABLED TO THE EIDAL BUS VIA THE SIGNAL COLB L. THE TEST WILL ALSO CHECK THAT THE EOAI REGISTER CAN BE CLEARED WHEN THE SIGNAL INTER L IS ASSERTED LOW. A BINARY COUNT DATA PATTERN WILL BE LOADED INTO THE FDAL REGISTER STARTING WITH A DATA PATTERN OF ONE AND INCREMENTING BY FOUR UNTIL THE DATA PATTERN 375 HAS BEEN LOADED AND CHECKED.

TEST 40:

THIS TEST WILL CHECK THAT THE SIGNALS READ H AND MSDI H CA N BE ASSERTED HIGH AND LOW. THESE SIGNALS ARE ASSERTED HIGH AND LOW BY CHANGING THE LOGIC LEVELS ON THE INPUT SIGNALS TO THE GATES WHICH GENERATE THE SIGNALS. THE SIGNALS READ H AND MSDI H ARE READ IN THE VDAL REGISTER AS BITS 3 AND 6 RESPECTIVELY.

TEST 41:

THIS TEST WILL CHECK THAT THE SIGNALS FETCT H AND BTS1 H CAN BE ASSERTED HIGH AND LOW. THESE TWO SIGNALS ARE ASSERTED HIGH AND LOW BY CHANGING THE INPUT SIGNALS TO THE GATES WHICH GENERATE THESE SIGNALS. THE PAUSE STATE MACHINE LOGIC IS USED TO TEST THE SIGNAL FETCT H. THE SIGNAL FETCT H IS ALSO CHECKED ON THE SIGNAL BTS1 H. THE SIGNAL BTS1 H IS READ IN THE VDAL REGISTER ON BIT 5.

TEST 42:

THIS TEST WILL CHECK THAT THE SIGNAL EDEOC H CAN BE SET TO THE HIGH STATE AND TO THE LOW STATE. THE SIGNAL EDEOC H IS READ IN THE VDAL REGISTER ON BIT 4 WHEN ADAL REAGISTER BIT 10 IS SET TO A ONE. THE PROGRAM WILL CHECK THE SIGNAL EDEOC H TO SET AND CLEAR C CHANGING THE LOGIC LEVELS ON THE FOLLOWING SIGNALS: ADAL9 H, PSM L, INTER L, REFR L, XRAS H, XRAS L, XCAS H, XCAS L AND SOP L. THE

TEST WILL USE THE SIGNAL EDEOC H TO CHECK THAT THE REFR FLIP-FLOP CAN BE SET AND CLEARED. THE REFR FLIP-FLOP WILL BE CHECKED TO BE CLEARED BY CHANGING THE LOGIC LEVELS ON THE SIGNALS ADAL7 H AND XCAS H. THHE REFR FLIP-FLOP CAN NOT BE CHECKED TO BE CLEARED BY THE SIGNAL INVD L BECAUSE OF THE LOGIC DESIGN.

TEST 43:

THIS TEST WILL CHECK THE TARGET EMULATORS INTERRUPT LOGIC USING THE SIGNALS TOBRK H AND BRK H TO CAUSE INTERRUPT REQUESTS. THE TEST WILL CHECK THAT NO INTERRUPTS OCCUR WHEN THE INTERRUPT ENABLE BIT IS CLEARED AND THE INTERRUPT REQUEST SIGNAL IS ASSERTED HIGH. THE TEST WILL CHECK THAT AN INTERPUPT WILL OCCUR WHEN THE INTERURPT ENABLE BIT IS SET AND THE SIGNAL TOBRK H IS ASSERTED HIGH. THE TEST WILL CHECK THAT THE BREAK LATCH FLIP-FLOP CAN BE SET, CLEARED, AND THAT IT CAN CAUSE AN INTERRUPT.

TEST 44:

THIS TEST WILL CHECK THAT THE SIGNALS ADAL 15:9, ADAL 7:3, ADAL 1:0, HDAL 15:0, FDAL7 H - FDAL0 H, VDAL7 H, VDAL2 H - VDAL0 H, GDAL15 H, GDAL2 H - GDAL0 H, AND MR15 H - MR0 H CAN ALL BE SET TO ONES. THEN A BRESET INSTRUCTION IS ISSUED AND THESE SIGNALS ARE TESTED TO THEN BE ZEROS. THEN THE PAUSE STATE WORKING FLIP-FLOP AND THE SINGLE STEP BREAK FLIP-FLOP ARE SET TO ONES AND AGAIN A BRESET INSTRUCTION IS ISSUED AND THESE FLIP-FLOPS ARE TESTED TO THEN BE ZEROS.

TEST 45:

THIS TEST WILL CHFCK THAT THE T-11 CAN BE POWERED-UP TO ALL ITS STARTING ADDRESSES AND THAT IT CAN RUN WITH DIFFERENT MODES SELECTED. THE PROGRAM WILL USE THE PAUSE STATE MACHINE TO CHECK THAT THE T-11 POWERED-UP TO THE STARTING ADDRESS SELECTED BY THE MODE REGISTER. THE PROGRAM WILL SELECT THE FOLLOWING T-11 MODES: 16 BIT STATIC, 16 BIT DYNAMIC 4K/16K, 16 BIT DYNAMIC 64K, 8 BIT STATIC, 8 BIT DYNAMIC 4K/16K AND 8 BIT DYNAMIC 64K. FOR EACH MODE SELECTED, THE PROGRAM WILL CHECK THAT THE T-11 CAN BE POWERED-UP AT EACH OF ITS STARTING ADDRESSES. THE PROGRAM WILL SELECT THE CLOCK ON THE TARGET EMULATOR MODULE TO PROVIDE THE TIMING TO THE T-11 CHIP. THE TEST WILL ALSO CHECK THAT THE NEW FORCE JUMP ADDRESS REGISTER CAN BE LOADED AND THAT ITS CONTENTS CAN BE LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER.

```
                                .TITLE PROGRAM HEADER AND TABLES
                                .SBTTL  PROGRAM HEADER

                                        .ENABL  ABS
                                        .ENABL  AMA
                                        .DSABL  GBL
002000                                  .       =       2000

002000                                  BGNMOD

                                ;++
                                ; THE PROGRAM HEADER IS THE INTERFACE BETWEEN
                                ; THE DIAGNOSTIC PROGRAM AND THE SUPERVISOR.
                                ;--

002000                                  POINTER BGNSETUP


002000                                  HEADER  CVCDC,A,0,60.,0,PRI07
002000                          L$NAME::                ;DIAGNOSTIC NAME
002000  103                             .ASCII /C/
002001  126                             .ASCII /V/
002002  103                             .ASCII /C/
002003  104                             .ASCII /D/
002004  103                             .ASCII /C/
002005  000                             .BYTE   0
002006  000                             .BYTE   0
002007  000                             .BYTE   0
002010                          L$REV::                 ;REVISION LEVEL
002010  101                             .ASCII  /A/
002011                          L$DEPO::                ;0
002011  060                             .ASCII  /0/
002012                          L$UNIT::                ;NUMBER OF UNITS
002012  000001                          .WORD   T$PTHV
002014                          L$TIML::                ;LONGEST TEST TIME
002014  000074                          .WORD   60.
002016                          L$HPCP::                ;POINTER TO H.W. QUES.
002016  036444                          .WORD   L$HARD
002020                          L$SPCP::                ;POINTER TO S.W. QUES.
002020  000000                          .WORD   0
002022                          L$HPTP::                ;PTR. TO DEF. H.W. PTABLE
002022  002260                          .WORD   L$HW
002024                          L$SPTP::                ;PTR. TO S.W. PTABLE
002024  000000                          .WORD   0
002026                          L$LADP::                ;DIAG. END ADDRESS
002026  036636                          .WORD   L$LAST
002030                          L$STA::                 ;RESERVED FOR APT STATS
002030  000000                          .WORD   0
002032                          L$CO::
002032  000000                          .WORD   0
002034                          L$DTYP::                ;DIAGNOSTIC TYPE
002034  000000                          .WORD   0
002036                          L$APT::                 ;APT EXPANSION
002036  000000                          .WORD   0
```

```
1415  002040                          L$DTP::                 ;PTR. TO DISPATCH TABLE
1416  002040  002124                          .WORD   L$DISPATCH
1417  002042                          L$PRIO::                ;DIAGNOSTIC RUN PRIORITY
1418  002042  000340                          .WORD   PRI07
1419  002044                          L$ENVI::                ;FLAGS DESCRIBE HOW IT WAS SETUP
1420  002044  000000                          .WORD   0
1421  002046                          L$EXP1::                ;EXPANSION WORD
1422  002046  000000                          .WORD   0
1423  002050                          L$MREV::                ;SVC REV AND EDIT #
1424  002050     003                          .BYTE   C$REVISION
1425  002051     003                          .BYTE   C$EDIT
1426  002052                          L$EF::                  ;DIAG. EVENT FLAGS
1427  002052  000000                          .WORD   0
1428  002054  000000                          .WORD   0
1429  002056                          L$SPC::
1430  002056  000000                          .WORD   0
1431  002060                          L$DEVP::                ; POINTER TO DEVICE TYPE LIST
1432  002060  002350                          .WORD   L$DVTYP
1433  002062                          L$REPP::                ;PTR. TO REPORT CODE
1434  002062  000000                          .WORD   0
1435  002064                          L$EXP4::
1436  002064  000000                          .WORD   0
1437  002066                          L$EXP5::
1438  002066  000000                          .WORD   0
1439  002070                          L$AUT::                 ;PTR. TO ADD UNIT CODE
1440  002070  000000                          .WORD   0
1441  002072                          L$DUT::                 ;PTR. TO DROP UNIT CODE
1442  002072  000000                          .WORD   0
1443  002074                          L$LUN::                 ;LUN FOR EXERCISERS TO FILL
1444  002074  000000                          .WORD   0
1445  002076                          L$DESP::                ;POINTER TO DIAG. DESCRIPTION
1446  002076  002360                          .WORD   L$DESC
1447  002100                          L$LOAD::                ;GENERATE SPECIAL AUTOLOAD EMT
1448  002100  104035                          EMT     E$LOAD
1449  002102                          L$ETP::                 ;POINTER TO ERRTBL
1450  002102  000000                          .WORD   0
1451  002104                          L$ICP::                 ;PTR. TO INIT CODE
1452  002104  010066                          .WORD   L$INIT
1453  002106                          L$CCP::                 ;PTR. TO CLEAN-UP CODE
1454  002106  010300                          .WORD   L$CLEAN
1455  002110                          L$ACP::                 ;PTR. TO AUTO CODE
1456  002110  010276                          .WORD   L$AUTO
1457  002112                          L$PRT::                 ;PTR. TO PROTECT TABLE
1458  002112  010060                          .WORD   L$PROT
1459  002114                          L$TEST::                ;TEST NUMBER
1460  002114  000000                          .WORD   0
1461  002116                          L$DLY::                 ;DELAY COUNT
1462  002116  000000                          .WORD   0
1463  002120                          L$HIME::                ;PTR. TO HIGH MEM
1464  002120  000000                          .WORD   0
1465
```

```
                                .SBTTL  DISPATCH TABLE

                                ;++
                                ; THE DISPATCH TABLE CONTAINS THE STARTING ADDRESS OF EACH TEST.
                                ; IT IS USED BY THE SUPERVISOR TO DISPATCH TO EACH TEST.
                                ;--

002122                                  DISPATCH 45.
002122  000055                          .WORD   45
002124                          L$DISPATCH::
002124  010344                          .WORD   T1
002126  010352                          .WORD   T2
002130  010436                          .WORD   T3
002132  010524                          .WORD   T4
002134  010574                          .WORD   T5
002136  010660                          .WORD   T6
002140  010746                          .WORD   T7
002142  011016                          .WORD   T8
002144  011062                          .WORD   T9
002146  011160                          .WORD   T10
002150  011250                          .WORD   T11
002152  011342                          .WORD   T12
002154  011416                          .WORD   T13
002156  011466                          .WORD   T14
002160  011556                          .WORD   T15
002162  011650                          .WORD   T16
002164  011724                          .WORD   T17
002166  011774                          .WORD   T18
002170  012072                          .WORD   T19
002172  012172                          .WORD   T20
002174  012246                          .WORD   T21
002176  012320                          .WORD   T22
002200  012442                          .WORD   T23
002202  012566                          .WORD   T24
002204  012666                          .WORD   T25
002206  012770                          .WORD   T26
002210  013236                          .WORD   T27
002212  013662                          .WORD   T28
002214  014570                          .WORD   T29
002216  015562                          .WORD   T30
002220  016752                          .WORD   T31
002222  020046                          .WORD   T32
002224  020316                          .WORD   T33
002226  021604                          .WORD   T34
002230  023156                          .WORD   T35
002232  023534                          .WORD   T36
002234  024356                          .WORD   T37
002236  024706                          .WORD   T38
002240  026132                          .WORD   T39
002242  026646                          .WORD   T40
002244  030566                          .WORD   T41
002246  031576                          .WORD   T42
002250  033332                          .WORD   T43
002252  034546                          .WORD   T44
002254  035716                          .WORD   T45
```

```
                                        .SBTTL  DEFAULT HARDWARE P-TABLE

                                        ;++
                                        ; THE DEFAULT HARDWARE P-TABLE CONTAINS DEFAULT VALUES OF
                                        ; THE TEST-DEVICE PARAMETERS.  THE STRUCTURE OF THIS TABLE
                                        ; IS IDENTICAL TO THE STRUCTURE OF THE HARDWARE P-TABLES,
                                        ; AND IS USED AS A "TEMPLATE" FOR BUILDING THE P-TABLES.
                                        ;--

002256                                          BGNHW   DFPTBL
002256  000003                                  .WORD   L10000-L$HW/2
002260                                  L$HW::
002260                                  DFPTBL::

002260  163010                                  .WORD   163010                  ;CSR ADDRESS
002262  000370                                  .WORD   370                     ;VECTOR ADDRESS
002264  000002                                  .WORD   2                       ;DEVICE SELECTION NUMBER

002266                                          ENDHW
002266                                  L10000:

                                        .SBTTL  SOFTWARE P-TABLE

                                        ;++
                                        ; THE SOFTWARE TABLE CONTAINS VARIOUS DATA USED BY THE
                                        ; PROGRAM AS OPERATIONAL PARAMETERS.  THESE PARAMETERS ARE
                                        ; SET UP AT ASSEMBLY TIME AND MAY BE VARIED BY THE OPERATOR
                                        ; AT RUN TIME.
                                        ;--

002266                                          BGNSW   SFPTBL
002266  000000                                  .WORD   L10001-L$SW/2
002270                                  L$SW::
002270                                  SFPTBL::


002270                                          ENDSW
002270                                  L10001:

002270                                          ENDMOD
```

```
                                .TITLE GLOBAL AREAS
                                .SBTTL  GLOBAL EQUATES SECTION


002270                                  BGNMOD

                                ;++
                                ; THE GLOBAL EQUATES SECTION CONTAINS PROGRAM EQUATES THAT
                                ; ARE USED IN MORE THAN ONE TEST.
                                ;--


002270                                  EQUALS
                                ;
                                ; BIT DIFINITIONS
                                ;
100000                          BIT15== 100000
040000                          BIT14== 40000
020000                          BIT13== 20000
010000                          BIT12== 10000
004000                          BIT11== 4000
002000                          BIT10== 2000
001000                          BIT09== 1000
000400                          BIT08== 400
000200                          BIT07== 200
000100                          BIT06== 100
000040                          BIT05== 40
000020                          BIT04== 20
000010                          BIT03== 10
000004                          BIT02== 4
000002                          BIT01== 2
000001                          BIT00== 1
                                ;
001000                          BIT9==  BIT09
000400                          BIT8==  BIT08
000200                          BIT7==  BIT07
000100                          BIT6==  BIT06
000040                          BIT5==  BIT05
000020                          BIT4==  BIT04
000010                          BIT3==  BIT03
000004                          BIT2==  BIT02
000002                          BIT1==  BIT01
000001                          BIT0==  BIT00
                                ;
                                ; EVENT FLAG DEFINITIONS
                                ;   EF32:EF17 RESERVED FOR SUPERVISOR TO PROGRAM COMMUNICATION
                                ;
000040                          EF.START==      32.                     ; START COMMAND WAS ISSUED
000037                          EF.RESTART==    31.                     ; RESTART COMMAND WAS ISSUED
000036                          EF.CONTINUE==   30.                     ; CONTINUE COMMAND WAS ISSUED
000035                          EF.NEW==        29.                     ; A NEW PASS HAS BEEN STARTED
000034                          EF.PWR==        28.                     ; A POWER-FAIL/POWER-UP OCCURRED
                                ;
                                ;
                                ; PRIORITY LEVEL DEFINITIONS
                                ;
```

```
                        PRI07== 340
                        PRI06== 300
                        PRI05== 240
                        PRI04== 200
                        PRI03== 140
                        PRI02== 100
                        PRI01== 40
                        PRI00== 0
                        ;
                        ;OPERATOR FLAG BITS
                        ;
                        EVL==        4
                        LOT==       10
                        ADR==       20
                        IDU==       40
                        ISR==      100
                        UAM==      200
                        BOE==      400
                        PNT==     1000
                        PRI==     2000
                        IXE==     4000
                        IBE==    10000
                        IER==    20000
                        LOE==    40000
                        HOF==   100000

                        ;
                        ;CONTROL REGISTER 0 (GDAL BITS 15:0)
                        ;

100000                  GDAL15==BIT15                   ;BIT15=1 READ DEVICE TYPE IN 15:8
                                                        ;TE DEVICE TYPE EQUALS 0000
                                                        ;
                                                        ;BIT15=0 READ DEVICE NUMBER INTO
                                                        ;BITS 11:8

040000                  GDAL14==BIT14                   ;ALWAYS A 0 ON READ
020000                  GDAL13==BIT13                   ;ALWAYS A 0 ON READ
010000                  GDAL12==BIT12                   ;ALWAYS A 0 ON READ

004000                  GDAL11==BIT11                   ;BITS 11-8 ARE USED TO SELECT THE
002000                  GDAL10==BIT10                   ;DEVICE NUMBER TO ASSERT THE SIGNAL
001000                  GDAL9== BIT9                    ;DEVE L. WHEN SELECTING TE THESE BITS
000400                  GDAL8== BIT8                    ;MUST = THE SETTING OF DEV 3 - DEV 0

000200                  GDAL7== BIT7                    ;SINGLE STEP BREAK INDICATOR (READ ONLY)
000100                  GDAL6== BIT6                    ;TIMEOUT BREAK INDICATOR (READ ONLY)
000040                  GDAL5== BIT5                    ;MEMORY SIM BREAK INDICATOR (READ ONLY)
000020                  GDAL4== BIT4                    ;STATE ANALYZER BREAK INDICATOR (READ ONLY)
000010                  GDAL3== BIT3                    ;ENABLE INTERRUPTS WHEN = TO 1
000004                  GDAL2== BIT2                    ;POINTER FOR EXTENDED REG SELECT
000002                  GDAL1== BIT1                    ;POINTER FOR EXTENDED REG SELECT
000001                  GDAL0== BIT0                    ;POINTER FOR EXTENDED REG SELECT

000200                  SSBRK== GDAL7                   ;SINGLE STEP BREAK INDICATOR (READ ONLY)
000100                  TOBRK== GDAL6                   ;TIMEOUT BREAK INDICATOR (READ ONLY)
```

```
1675            000040                  MSBRK== GDAL5                           ;MEMORY SIM BREAK INDICATOR (READ ONLY)
1676            000020                  EDBRK== GDAL4                           ;STATE ANALYZER BREAK INDICATOR (READ ONLY)
1677
1678                                    ;
1679                                    ;CONTROL REGISTER 2 (ADAL BITS 15:0)
1680
1681
1682            100000                  ADAL15==BIT15                           ;SELECT COLUMN AI FOR STATE ANALYZER
1683            040000                  ADAL14==BIT14                           ;1 - SELECT ROW/COLUMN FOR AI TO STATE ANALYZER
1684                                                                            ;0 - SELECT SERVICE FOR AI TO STATE ANALYZER
1685            020000                  ADAL13==BIT13                           ;ENABLE SERVICE FOR EMULATOR
1686            010000                  ADAL12==BIT12                           ;ENABLE MODE FROM EMULATOR
1687            004000                  ADAL11==BIT11                           ;DISABLE SERVICE TO THE TARGET
1688            002000                  ADAL10==BIT10                           ;MASTER SWITCH
1689            001000                  ADAL9== BIT9                            ;ENABLE STATE ANALYZER CLOCKS (1)
1690            000400                  ADAL8== BIT8                            ;ENABLE TIMEOUT BREAK
1691            000200                  ADAL7== BIT7                            ;ENABLE REFRESH TO STATE ANALYZER
1692            000100                  ADAL6== BIT6                            ;
1693            000040                  ADAL5== BIT5                            ;1 - ENABLE SINGLE STEP BREAK
1694                                                                            ;0 - DISABLE SINGLE STEP BREAK
1695            000020                  ADAL4== BIT4                            ;1 - PAUSE STATE MACHINE (RUN MODE)
1696                                                                            ;0 - PAUSE STATE MACHINE (PAUSE MODE)
1697            000010                  ADAL3== BIT3                            ;POWER-UP FROM TARGET (1)
1698            000004                  ADAL2== BIT2                            ;POWER-UP FROM T-11
1699            000002                  ADAL1== BIT1                            ;ENABLE INTERNAL CLOCK (1)
1700            000001                  ADAL0== BIT0                            ;RESETS BREAK LOGIC (1)
1701
1702                                    ;
1703                                    ;CONTROL REGISTER 1 (VDAL BITS 15:0)
1704                                    ;
1705
1706            100000                  VDAL15==BIT15                           ;TDFI H - TAKE NEW FORCE JUMP ADDRESS (READ ONLY
1707            040000                  VDAL14==BIT14                           ;EP8N H - 8 BIT ADDRESS HB F/F (READ ONLY)
1708            020000                  VDAL13==BIT13                           ;EP8G H - 8 BIT ADDRESS LB F/F (READ ONLY)
1709            010000                  VDAL12==BIT12                           ;EP8F H - 8 BIT INSTR HB F/F (READ ONLY)
1710            004000                  VDAL11==BIT11                           ;EPFN H - 16 BIT ADDRESS F/F (READ ONLY)
1711            002000                  VDAL10==BIT10                           ;EPSF H - PAUSE STATE SYNC F/F (READ ONLY)
1712            001000                  VDAL9== BIT9                            ;PSMW H - PAUSE STATE WORKING F/F (READ ONLY)
1713            000400                  VDAL8== BIT8                            ;PSMW  H - GET NEW ADDRESS F/F (READ ONLY)
1714            000200                  VDAL7== BIT7                            ;DIAGNOSTIC FETCT H (R/W)
1715            000100                  VDAL6== BIT6                            ;MSDI H - LOGIC LEVEL MSDI H (READ ONLY)
1716            000040                  VDAL5== BIT5                            ;BTS1 H - LOGIC LEVEL BTS1 H (READ ONLY)
1717            000020                  VDAL4== BIT4                            ;EDEOC H - LOGIC LEVEL EDEOC H (READ ONLY)
1718            000010                  VDAL3== BIT3                            ;READ H - LOGIC LEVEL READ H (READ ONLY)
1719            000004                  VDAL2== BIT2                            ;CLOCK TAI, TDAL, 0 PAUSE STATE MACHINE (R/W)
1720            000002                  VDAL1== BIT1                            ;SPARE
1721            000001                  VDAL0== BIT0                            ;ENABLE TAI AND TDAL READBACK FROM POD (R/W)
1722
1723                                    ;
1724                                    ;CONTROL REGISTER 6 (HDAL BITS 15:0)
1725                                    ;
1726
1727             100000                 HDAL15==BIT15                           ;1/0 - PULSE SIGNAL XPI L
1728             040000                 HDAL14==BIT14                           ;1/0 - PULSE SIGNAL EIDAL17 H
1729             020000                 HDAL13==BIT13                           ;1/0 - PULSE SIGNAL XCAS H
1730             010000                 HDAL12==BIT12                           ;1/0 - PULSE SIGNAL XRAS H
```

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1731            004000          HDAL11==BIT11                   ;1/0 - PULSE SIGNAL EIDAL16 H
1732            002000          HDAL10==BIT10                   ;SPARE
1733            001000          HDAL9== BIT9                    ;1 - ENABLE DIAG ADDRESS TO ADDRESS BUS
1734                                                            ;0 - ENABLE EIDAL BUS TO ADDRESS BUS
1735                                                            ;    WHEN ADAL10 H IS SET TO A ONE AND
1736                                                            ;    DISABLE DIAG ADDRESS FROM ADDRESS BUS
1737            000400          HDAL8== BIT8                    ;1/0 - PULSE CREADY H
1738            000200          HDAL7== BIT7                    ;1/0 - PULSE PBCLR H
1739            000100          HDAL6== BIT6                    ;1/0 - PULSE PSEL1 H
1740            000040          HDAL5== BIT5                    ;1/0 - PULSE PSEL0 H
1741            000020          HDAL4== BIT4                    ;1/0 - PULSE PR/WHB L
1742            000010          HDAL3== BIT3                    ;1/0 - PULSE PR/WLB L
1743            000004          HDAL2== BIT2                    ;1 - ENABLES DIAG CONTROL OF T-11 TIMING
1744                                                            ;    AND CONTROL SIGNALS
1745                                                            ;0 - ENABLES T-11 TO GENERATE SIGNALS
1746            000002          HDAL1== BIT1                    ;SPARE
1747            000001          HDAL0== BIT0                    ;1/0 - PULSE MSDI H
1748
1749                            ;
1750                            ;CONTROL REGISTER 6 (MODE REG BITS MR 15:0)
1751                            ;
1752
1753            100000          MR15==  BIT15                   ;
1754            040000          MR14==  BIT14                   ;
1755            020000          MR13==  BIT13                   ;
1756            010000          MR12==  BIT12                   ;
1757            004000          MR11==  BIT11                   ;1 - 8 BIT ADDRESS SELECTION
1758                                                            ;0 - 16 BIT ADDRESS SELECTION
1759            002000          MR10==  BIT10                   ;
1760            001000          MR9==   BIT9                    ;
1761            000400          MR8==   BIT8                    ;
1762            000200          MR7==   BIT7                    ;
1763            000100          MR6==   BIT6                    ;
1764            000040          MR5==   BIT5                    ;
1765            000020          MR4==   BIT4                    ;
1766            000010          MR3==   BIT3                    ;
1767            000004          MR2==   BIT2                    ;
1768            000002          MR1==   BIT1                    ;
1769            000001          MR0==   BIT0                    ;
1770
1771                            ;
1772                            ;CONTROL REGISTER 6 (FDAL BITS 7:0)
1773                            ;
1774
1775            000200          FDAL7== BIT7                    ;INTERRUPT VECTOR
1776            000100          FDAL6== BIT6                    ;INTERRUPT VECTOR
1777            000040          FDAL5== BIT5                    ;INTERRUPT VECTOR
1778            000020          FDAL4== BIT4                    ;INTERRUPT VECTOR
1779            000010          FDAL3== BIT3                    ;INTERRUPT VECTOR
1780            000004          FDAL2== BIT2                    ;INTERRUPT VECTOR
1781            000002          FDAL1== BIT1                    ;SPARE
1782            000001          FDAL0== BIT0                    ;1 - ENABLES EOAI 7:0 BUS TO BE READ
1783                                                            ;0 - ENABLES CTL 7:0 REG TO BE READ
1784
1785                            ;
1786                            ;CONTROL REGISTER 6 (DIAG. ADDR BITS 15:0)
```

```
1787                                    ;
1788
1789            100000                  ADDR15==BIT15                   ;
1790            040000                  ADDR14==BIT14                   ;
1791            020000                  ADDR13==BIT13                   ;
1792            010000                  ADDR12==BIT12                   ;
1793            004000                  ADDR11==BIT11                   ;
1794            002000                  ADDR10==BIT10                   ;
1795            001000                  ADDR9== BIT9                    ;
1796            000400                  ADDR8== BIT8                    ;
1797            000200                  ADDR7== BIT7                    ;
1798            000100                  ADDR6== BIT6                    ;
1799            000040                  ADDR5== BIT5                    ;
1800            000020                  ADDR4== BIT4                    ;
1801            000010                  ADDR3== BIT3                    ;
1802            000004                  ADDR2== BIT2                    ;
1803            000002                  ADDR1== BIT1                    ;
1804            000001                  ADDR0== BIT0                    ;
1805
```

```
1806                                    .SBTTL  GLOBAL DATA SECTION
1807
1808                                    ;++
1809                                    ; THE GLOBAL DATA SECTION CONTAINS DATA THAT ARE USED
1810                                    ; IN MORE THAN ONE TEST.
1811                                    ;--
1812
1813
1814  002270                                    ERRTBL
1815  002270                            L$ERRTBL::
1816  002270  000000                    ERRTYP::        .WORD   0
1817  002272  000000                    ERRNBR::        .WORD   0
1818  002274  000000                    ERRMSG::        .WORD   0
1819  002276  000000                    ERRBLK::        .WORD   0
1820
1821                                    ;
1822                                    ;GLOBAL DATA FOR TARGET EMULATOR
1823                                    ;
1824
1825  002300  163010                    REG0::  .WORD   163010          ;CONTROL REGISTER 0
1826  002302  163012                    REG2::  .WORD   163012          ;CONTROL REGISTER 2
1827  002304  163014                    REG4::  .WORD   163014          ;CONTROL REGISTER 4
1828  002306  163016                    REG6::  .WORD   163016          ;CONTROL REGISTER 6
1829
1830  002310  000000                    IDDEV:: .WORD   0               ;TARGET EMULATOR DEVICE # (11:8)
1831  002312  000000                    TEVECT::.WORD   0               ;TARGET EMULATOR VECTOR ADDRESS
1832  002314  000000                    UNITNB::.WORD   0               ;
1833  002316  000000                    IDTYPE::.WORD   0               ;TARGET EMULATOR DEVICE TYPE (15-8)
1834
1835  002320  000000                    R0LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 0
1836  002322  000000                    R0GOOD::.WORD   0               ;EXPECTED REG 0
1837  002324  000000                    R0MASK::.WORD   0               ;BITS TO BE IGNORED ON COMPARE
1838  002326  000000                    R0BAD:: .WORD   0               ;DATA READ MASKED WITH R0MASK
1839
1840  002330  000000                    R2LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 2
1841  002332  000000                    R2READ::.WORD   0               ;ACTUAL REG 2 READ
1842
1843  002334  000000                    R4LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 4
1844  002336  000000                    R4GOOD::.WORD   0               ;EXPECTED DATA FROM REGISTER 4
1845  002340  000000                    R4BAD:: .WORD   0               ;DATA READ FROM REGISTER 4
1846
1847  002342  000000                    R6LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 6
1848  002344  000000                    R6READ::.WORD   0               ;ACTUAL REGISTER 6 READ
1849  002346  000000                    R6MASK::.WORD   0               ;BITS TO BE IGNORED
```

```
                                        .SBTTL  GLOBAL TEXT SECTION

                                        ;++
                                        ; THE GLOBAL TEXT SECTION CONTAINS FORMAT STATEMENTS,
                                        ; MESSAGES, AND ASCII INFORMATION THAT ARE USED IN
                                        ; MORE THAN ONE TEST.
                                        ;--

                                        ;
                                        ; NAMES OF DEVICES SUPPORTED BY PROGRAM
                                        ;
                                                DEVTYP  <CDS-11>
002350                                  L$DVTYP::
002350  042103  026523  030461                 .ASCIZ  /CDS-11/
002356     000
002360                                          .EVEN


                                        ; TEST DESCRIPTION
                                        ;
                                                DESCRIPT        <TARGET EMULATOR DIAG.>
002360                                  L$DESC::
002360  040524  043522  052105                  .ASCIZ  /TARGET EMULATOR DIAG./
002366  042440  052515  040514
002374  047524  020122  044504
002402  043501  000056
                                                .EVEN


                                        ;
                                        ;ASCII MESSAGES USED BY ERROR CALLS
                                        ;

                                        ;CONTROL REGISTER 0 ERROR MESSAGES

002406  042107  046101  030440  GDALRG::.ASCIZ  /GDAL 15:0 REG ERROR/
002414  035065  020060  042522
002422  020107  051105  047522
002430  000122
002432  047125  054105  042520  UNEXIN::.ASCIZ  /UNEXPECTED INTERRUPT OCCURED/
002440  052103  042105  044440
002446  052116  051105  052522
002454  052120  047440  041503
002462  051125  042105     000
002467     106  044501  042514  NOINT:: .ASCIZ  /FAILED TO INTERRUPT/
002474  020104  047524  044440
002502  052116  051105  052522
002510  052120     000


                                        ;CONTROL REGISTER 2 ERROR MESSAGES

002513     101  040504  020114  ADALRG::.ASCIZ  /ADAL 15:0 REG ERROR/
002520  032461  030072  051040
002526  043505  042440  051122
002534  051117     000
```

```
1906                                    ;CONTROL REGISTER 4 ERROR MESSAGES
1907
1908  002537     126  040504  020114  VDALRG::.ASCIZ  /VDAL 7:0 OR PAUSE STATE MACHINE ERROR/
1909  002544  035067  020060  051117
1910  002552  050040  052501  042523
1911  002560  051440  040524  042524
1912  002566  04 :40  041501  044510
1913  002574  042516  042440  051122
1914  002602  051117     000
1915
1916                                    ;CONTROL REGISTER 6 ERROR MESSAGES
1917
1918  002605     110  040504  020114  HDALRG::.ASCIZ  /HDAL 15:0 REG ERROR/
1919  002612  032461  030072  051040
1920  002620  043505  042440  051122
1921  002626  051117     000
1922  002631     115  020122  032461  MODREG::.ASCIZ  /MR 15:0 REG ERROR/
1923  002636  030072  051040  043505
1924  002644  042440  051122  051117
1925  002652     000
1926  002653     106  040504  020114  FDALRG::.ASCIZ  /FDAL 7:0 REG ERROR/
1927  002660  035067  020060  042522
1928  002665  020107  051105  047522
1929  002674  000122
1930  002676  047505  044501  033440  EOAIFD::.ASCIZ  /EOAI 7:0 OR FDAL 7:0 REG ERROR/
1931  002704  030072  047440  020122
1932  002712  042106  046101  033440
1933  002720  030072  051040  043505
1934  002726  042440  051122  051117
1935  002734     000
1936  002735     104  040511  020107  ADDRRG::.ASCIZ  /DIAG ADDR 15:0 REG ERROR/
1937  002742  04 :01  051104  030440
1938  002750  035065  020060  042522
1939  002756  020107  051105  047522
1940  002764  000122
1941  002766  047506  041522  020105  FJADRG::.ASCIZ  /FORCE JUMP ADDRESS READBACK REG ERROR/
1942  002774  052512  050115  040440
1943  003002  042104  042522  051523
1944  003010  051040  040505  041104
1945  003016  041501  020113  042522
1946  003024  020107  051105  047522
1947  003032  000122
1948  003034  047111  052123  020122  IEODAL::.ASCIZ  /INSTR REG TO EODAL BUS READBACK ERROR/
1949  003042  042522  020107  047524
1950  003050  042440  042117  046101
1951  003056  041040  051525  051040
1952  003064  040505  041104  041501
1953  003072  020113  051105  047522
1954  003100  000122
1955  003102  047515  042504  051040  MEODAL::.ASCIZ  /MODE REG TO EODAL BUS READBACK ERROR/
1956  003110  043505  052040  020117
1957  003116  047505  040504  020114
1958  003124  052502  020123  042522
1959  003132  042101  040502  045503
1960  003140  042440  051122  051117
1961  003146     000
```

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1962  003147    106  051117  042503  FEODAL::.ASCIZ  /FORCE JUMP ADDRESS REG TO EODAL BUS READBACK ERROR/
1963  003154  045040  046525  020120
1964  003162  042101  051104  051505
1965  003170  020123  042522  020107
1966  003176  047524  042440  042117
1967  003204  046101  041040  051525
1968  003212  051040  040505  041104
1969  003220  041501  020113  051105
1970  003226  047522  000122
1971  003232  052103  020114  035067  CTLFDL::.ASCIZ  CTL 7:0 OR FDAL 7:0 REG ERROR/
1972  003240  020060  051117  043040
1973  003246  040504  020114  035067
1974  003254  020060  042522  020107
1975  003262  051105  047522  000122
1976  003270  047515  042504  051040  MEIDAL::.ASCIZ  /MODE REG TO EIDAL BUS READBACK ERROR/
1977  003276  043505  052040  020117
1978  003304  044505  040504  020114
1979  003312  052502  020123  042522
1980  003320  042101  040502  045503
1981  003326  042440  051122  051117
1982  003334     000
1983  003335     115  042117  020105  MTOTMR::.ASCIZ  /MODE REG TO TARGET MODE REG ERROR/
1984  003342  042522  020107  047524
1985  003350  052040  051101  042507
1986  003356  020124  047515  042504
1987  003364  051040  043505  042440
1988  003372  051122  051117     000
1989  003377     115  042117  020105  MADDRS::.ASCIZ  /MODE REG TO ADDRESS BUS READBACK ERROR/
1990  003404  042522  020107  047524
1991  003412  040440  042104  042522
1992  003420  051523  041040  051525
1993  003426  051040  040505  041104
1994  003434  041501  020113  051105
1995  003442  047522  000122
1996  003446  046117  020104  045106  FJAEID::.ASCIZ  /OLD FJA TO EIDAL BUS ERROR/
1997  003454  020101  047524  042440
1998  003462  042111  046101  041040
1999  003470  051525  042440  051122
2000  003476  051117     000
2001  003501     117  042114  043040  FJAADR::.ASCIZ  /OLD FJA TO ADDRESS BUS ERROR/
2002  003506  040512  052040  020117
2003  003514  042101  051104  051505
2004  003522  020123  052502  020123
2005  003530  051105  047522  000122
2006  003536  046117  020104  045106  FJATDL::.ASCIZ  /OLD FJA TO TDAL LATCH TO EIDAL BUS ERROR/
2007  003544  020101  047524  052040
2008  003552  040504  020114  040514
2009  003560  041524  020110  047524
2010  003566  042440  042111  046101
2011  003574  041040  051525  042440
2012  003602  051122  051117     000
2013  003607     124  040504  020114  TDLEOD::.ASCIZ  /TDAL LATCH TO EIDAL TO DATA TO EODAL BUS ERROR/
2014  003614  040514  041524  020110
2015  003622  047524  042440  042111
2016  003630  046101  052040  020117
2017  003636  040504  040524  052040
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2018  003644  020117  047505  040504
2019  003652  020114  052502  020123
2020  003660  051105  047522  000122
2021  003666  042106  046101  051040  FDALEO::.ASCIZ  /FDAL REG TO EODAL BUS ERROR/
2022  003674  043505  052040  020117
2023  003702  047505  040504  020114
2024  003710  052502  020123  051105
2025  003716  047522  000122
2026  003722  042106  046101  051040  FDALEI::.ASCIZ  /FDAL REG TO EODAL BUS TO EIDAL BUS ERROR/
2027  003730  043505  052040  020117
2028  003736  047505  040504  020114
2029  003744  052502  020123  047524
2030  003752  042440  042111  046101
2031  003760  041040  051525  042440
2032  003766  051122  051117     000
2033  003773     120  052501  042523  NOPSM:: .ASCIZ  /PAUSE STATE NOT ENTERED WHEN T-11 CHIP IS POWERED-UP/
2034  004000  051440  040524  042524
2035  004006  047040  052117  042440
2036  004014  052116  051105  042105
2037  004022  053440  042510  020116
2038  004030  026524  030461  041440
2039  004036  044510  020120  051511
2040  004044  050040  053517  051105
2041  004052  042105  052455  000120
2042  004060  047506  041522  020105  FJSTAD::.ASCIZ  /FORCE JUMP ADDRESS NOT = EXPECTED T-11 START-RESTART ADDRESS/
2043  004066  052512  050115  040440
2044  004074  042104  042522  051523
2045  004102  047040  052117  036440
2046  004110  042440  050130  041505
2047  004116  042524  020104  026524
2048  004124  030461  051440  040524
2049  004132  052122  051055  051505
2050  004140  040524  052122  040440
2051  004146  042104  042522  051523
2052  004154     000
2053          004156                        .EVEN
2054
2055                                  ;
2056                                  ; FORMAT STATEMENTS USED IN PRINT CALLS
2057                                  ;
2058
2059  004156  040445  047503  052116  EMSGR0::.ASCIZ  /%ACONTROL REG 0 ERROR%N/
2060  004164  047522  020114  042522
2061  004172  020107  020060  051105
2062  004200  047522  022522  000116
2063  004206  040445  047503  052116  EMSGR2::.ASCIZ  /%ACONTROL REG 2 ERROR%N/
2064  004214  047522  020114  042522
2065  004222  020107  020062  051105
2066  004230  047522  022522  000116
2067  004236  040445  047503  052116  EMSGR4::.ASCIZ  /%ACONTROL REG 4 ERROR%N/
2068  004244  047522  020114  042522
2069  004252  020107  020064  051105
2070  004260  047522  022522  000116
2071  004266  040445  047503  052116  EMSGR6::.ASCIZ  /%ACONTROL REG 6 ERROR%N/
2072  004274  047522  020114  042522
2073  004302  020107  020066  051105
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```
2074  004310  047522  022522  000116
2075  004316  040445  042522  030107  REG0EQ::.ASCIZ  /%AREG0 = /
2076  004324  036440  000040
2077  004330  040445  042522  031107  REG2EQ::.ASCIZ  /%AREG2 = /
2078  004336  036440  000040
2079  004342  040445  042522  032107  REG4EQ.::.ASCIZ  /%AREG4 = /
2080  004350  036440  000040
2081  004354  040445  042522  033107  REG6EQ::.ASCIZ  /%AREG6 = /
2082  004362  036440  000040
2083  004366  040445  047514  042101  FRMTR0::.ASCIZ  /%ALOAD: %06%S1%AGOOD: %06%S1%ABAD: %06%N/
2084  004374  020072  047445  022466
2085  004402  030523  040445  047507
2086  004410  042117  020072  047445
2087  004416  022466  030523  040445
2088  004424  040502  035104  022440
2089  004432  033117  047045     000
2090  004437     045  046101  040517  FRMTR2::.ASCIZ  /%ALOAD: %06%S1%AREAD: %06%N/
2091  004444  035104  022440  033117
2092  004452  051445  022461  051101
2093  004460  040505  035104  022440
2094  004466  033117  047045     000
2095  004473     045  052101  046511  MSGTM0::.ASCIZ   /%ATIME OUT ERROR ADDRESSING CONTROL REG 0%N/
2096  004500  020105  052517  020124
2097  004506  051105  047522  020122
2098  004514  042101  051104  051505
2099  004522  044523  043516  041440
2100  004530  047117  051124  046117
2101  004536  051040  043505  030040
2102  004544  047045     000
2103  004547     045  052101  046511  MSGTM2::.ASCIZ   /%ATIME OUT ERROR ADDRESSING CONTROL REG 2%N/
2104  004554  020105  052517  020124
2105  004562  051105  047522  020122
2106  004570  042101  051104  051505
2107  004576  044523  043516  041440
2108  004604  047117  051124  046117
2109  004612  051040  043505  031040
2110  004620  047045     000
2111  004623     045  052101  046511  MSGTM4::.ASCIZ   /%ATIME OUT ERROR ADDRESSING CONTROL REG 4%N/
2112  004630  020105  052517  020124
2113  004636  051105  047522  020122
2114  004644  042101  051104  051505
2115  004652  044523  043516  041440
2116  004660  047117  051124  046117
2117  004666  051040  043505  032040
2118  004674  047045     000
2119  004677     045  052101  046511  MSGTM6::.ASCIZ   /%ATIME OUT ERROR ADDRESSING CONTROL REG 6%N/
2120  004704  020105  052517  020124
2121  004712  051105  047522  020122
2122  004720  042101  051104  051505
2123  004726  044523  043516  041440
2124  004734  047117  051124  046117
2125  004742  051040  043505  033040
2126  004750  047045     000
2127          004754                  .EVEN
2128
```

```
                        .SBTTL  GLOBAL ERROR REPORT SECTION

                        ;++
                        ; THE GLOBAL ERROR REPORT SECTION CONTAINS MESSAGE PRINTING AREAS
                        ; USED BY MORE THAN TEST TO OUTPUT ADDITIONAL ERROR INFORMATION.  PRINTB
                        ; (BASIC) AND PRINTX (EXTENDED) CALLS ARE USED TO CALL PRINT SERVICES.
                        ;--

004754                          BGNMSG  R0EROR
004754                  R0EROR::
004754  004537  005160          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
004760  004156                  .WORD   EMSGR0
004762  004737  005230          JSR     PC,PRNTR0               ;GO PRINT CONTROL REGISTER 0 INFO
004766                          ENDMSG
004766                  L10002:
004766  104423                  TRAP    C$MSG

004770                          BGNMSG  R2EROR
004770                  R2EROR::
004770  004537  005160          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
004774  004206                  .WORD   EMSGR2
004776  004737  005306          JSR     PC,PRNTR2               ;GO PRINT CONTROL REGISTER 2 INFO
005002                          ENDMSG
005002                  L10003:
005002  104423                  TRAP    C$MSG

005004                          BGNMSG  R4EROR
005004                  R4EROR::
005004  004537  005160          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
005010  004236                  .WORD   EMSGR4
005012  004737  005360          JSR     PC,PRNTR4               ;GO PRINT CONTROL REGISTER 4 INFO
005016                          ENDMSG
005016                  L10004:
005016  104423                  TRAP    C$MSG

005020                          BGNMSG  R06ERR
005020                  R06ERR::
005020  004537  005160          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
005024  004266                  .WORD   EMSGR6
005026  004737  005200          JSR     PC,PR06R                ;GO PRINT CONTROL REG 0 AND 6 INFO
005032                          ENDMSG
005032                  L10005:
005032  104423                  TRAP    C$MSG

005034                          BGNMSG  R026ER
005034                  R026ER::
005034  004537  005160          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
005040  004266                  .WORD   EMSGR6
005042  004737  005212          JSR     PC,PR026R
005046                          ENDMSG
005046                  L10006:
005046  104423                  TRAP    C$MSG

005050                          BGNMSG  R0TM
005050                  R0TM::
```

```
2185  005050                                    PRINTB  #MSGTM0
2186  005050  012746  004473                    MOV     #MSGTM0,-(SP)
2187  005054  012746  000001                    MOV     #1,-(SP)
2188  005060  010600                            MOV     SP,R0
2189  005062  104414                            TRAP    C$PNTB
2190  005064  062706  000004                    ADD     #4,SP
2191  005070                                    ENDMSG
2192  005070                              L10007:
2193  005070  104423                            TRAP    C$MSG
2194
2195  005072                                    BGNMSG  R2TM
2196  005072                              R2TM::
2197  005072                                    PRINTB  #MSGTM2
2198  005072  012746  004547                    MOV     #MSGTM2,-(SP)
2199  005076  012746  000001                    MOV     #1,-(SP)
2200  005102  010600                            MOV     SP,R0
2201  005104  104414                            TRAP    C$PNTB
2202  005106  062706  000004                    ADD     #4,SP
2203  005112                                    ENDMSG
2204  005112                              L10010:
2205  005112  104423                            TRAP    C$MSG
2206
2207  005114                                    BGNMSG  R4TM
2208  005114                              R4TM::
2209  005114                                    PRINTB  #MSGTM4
2210  005114  012746  004623                    MOV     #MSGTM4,-(SP)
2211  005120  012746  000001                    MOV     #1,-(SP)
2212  005124  010600                            MOV     SP,R0
2213  005126  104414                            TRAP    C$PNTB
2214  005130  062706  000004                    ADD     #4,SP
2215  005134                                    ENDMSG
2216  005134                              L10011:
2217  005134  104423                            TRAP    C$MSG
2218
2219  005136                                    BGNMSG  R6TM
2220  005136                              R6TM::
2221  005136                                    PRINTB  #MSGTM6
2222  005136  012746  004677                    MOV     #MSGTM6,-(SP)
2223  005142  012746  000001                    MOV     #1,-(SP)
2224  005146  010600                            MOV     SP,R0
2225  005150  104414                            TRAP    C$PNTB
2226  005152  062706  000004                    ADD     #4,SP
2227  005156                                    ENDMSG
2228  005156                              L10012:
2229  005156  104423                            TRAP    C$MSG
2230
2231                                    ;ROUTINE TO PRINT WHAT CONTROL REGISTER DETECTED THE ERROR.
2232
2233  005160                            PRNTBS::PRINTB  (R5)+
2234  005160  012546                            MOV     (R5)+,-(SP)
2235  005162  012746  000001                    MOV     #1,-(SP)
2236  005166  010600                            MOV     SP,R0
2237  005170  104414                            TRAP    C$PNTB
2238  005172  062706  000004                    ADD     #4,SP
2239  005176  000205                            RTS     R5
2240
```

```
2241                                    ;ROUTINE TO PRINT CONTROL REGISTER 0 AND 6 ERROR INFORMATION
2242
2243  005200  004737  005230            PR06R:: JSR     PC,PRNTR0
2244  005204  004737  005436                    JSR     PC,PRNTR6
2245  005210  000207                            RTS     PC
2246
2247                                    ;ROUTINE TO PRINT CONTROL REGISTER 0, 2 AND 6 ERROR INFORMATION
2248
2249  005212  004737  005230            PR026R::JSR     PC,PRNTR0               ;GO PRINT CONTROL REGISTER 0 INFO
2250  005216  004737  005306                    JSR     PC,PRNTR2               ;GO PRINT CONTROL REGISTER 2 INFO
2251  005222  004737  005436                    JSR     PC,PRNTR6               ;GO PRINT CONTROL REGISTER 6 INFO
2252  005226  000207                            RTS     PC
2253
2254                                    ;PRINT CONTROL REGISTER 0 ERROR INFORMATION
2255
2256  005230                            PRNTR0::PRINTX  #REG0EQ
2257  005230  012746  004316                    MOV     #REG0EQ,-(SP)
2258  005234  012746  000001                    MOV     #1,-(SP)
2259  005240  010600                            MOV     SP,R0
2260  005242  104415                            TRAP    C$PNTX
2261  005244  062706  000004                    ADD     #4,SP
2262  005250                                    PRINTX  #FRMTR0,R0LOAD,R0GOOD,R0BAD
2263  005250  013746  002326                    MOV     R0BAD,-(SP)
2264  005254  013746  002322                    MOV     R0GOOD,-(SP)
2265  005260  013746  002320                    MOV     R0LOAD,-(SP)
2266  005264  012746  004366                    MOV     #FRMTR0,-(SP)
2267  005270  012746  000004                    MOV     #4,-(SP)
2268  005274  010600                            MOV     SP,R0
2269  005276  104415                            TRAP    C$PNTX
2270  005300  062706  000012                    ADD     #12,SP
2271  005304  000207                            RTS     PC
2272
2273                                    ;PRINT CONTROL REGISTER 2 ERROR INFORMATION
2274
2275  005306                            PRNTR2::PRINTX  #REG2EQ
2276  005306  012746  004330                    MOV     #REG2EQ,-(SP)
2277  005312  012746  000001                    MOV     #1,-(SP)
2278  005316  010600                            MOV     SP,R0
2279  005320  104415                            TRAP    C$PNTX
2280  005322  062706  000004                    ADD     #4,SP
2281  005326                                    PRINTX  #FRMTR2,R2LOAD,R2READ
2282  005326  013746  002332                    MOV     R2READ,-(SP)
2283  005332  013746  002330                    MOV     R2LOAD,-(SP)
2284  005336  012746  004437                    MOV     #FRMTR2,-(SP)
2285  005342  012746  000003                    MOV     #3,-(SP)
2286  005346  010600                            MOV     SP,R0
2287  005350  104415                            TRAP    C$PNTX
2288  005352  062706  000010                    ADD     #10,SP
2289  005356  000207                            RTS     PC
2290
2291                                    ;PRINT CONTROL REGISTER 4 ERROR INFORMATION
2292
2293  005360                            PRNTR4::PRINTX  #REG4EQ
2294  005360  012746  004342                    MOV     #REG4EQ,-(SP)
2295  005364  012746  000001                    MOV     #1,-(SP)
2296  005370  010600                            MOV     SP,R0
```

```
2297  005372  104415                  TRAP    C$PNTX
2298  005374  062706  000004          ADD     #4,SP
2299  005400                          PRINTX  #FRMTR0,R4LOAD,R4GOOD,R4BAD
2300  005400  013746  002340          MOV     R4BAD,-(SP)
2301  005404  013746  002336          MOV     R4GOOD,-(SP)
2302  005410  013746  002334          MOV     R4LOAD,-(SP)
2303  005414  012746  004366          MOV     #FRMTR0,-(SP)
2304  005420  012746  000004          MOV     #4,-(SP)
2305  005424  010600                  MOV     SP,R0
2306  005426  104415                  TRAP    C$PNTX
2307  005430  062706  000012          ADD     #12,SP
2308  005434  000207                  RTS     PC
2309
2310                          ;PRINT CONTROL REGISTER 6 ERROR INFORMATION
2311
2312  005436                  PRNTR6::PRINTX  #REG6EQ
2313  005436  012746  004354          MOV     #REG6EQ,-(SP)
2314  005442  012746  000001          MOV     #1,-(SP)
2315  005446  010600                  MOV     SP,R0
2316  005450  104415                  TRAP    C$PNTX
2317  005452  062706  000004          ADD     #4,SP
2318  005456                          PRINTX  #FRMTR2,R6LOAD,R6READ
2319  005456  013746  002344          MOV     R6READ,-(SP)
2320  005462  013746  002342          MOV     R6LOAD,-(SP)
2321  005466  012746  004437          MOV     #FRMTR2,-(SP)
2322  005472  012746  000003          MOV     #3,-(SP)
2323  005476  010600                  MOV     SP,R0
2324  005500  104415                  TRAP    C$PNTX
2325  005502  062706  000010          ADD     #10,SP
2326  005506  000207                  RTS     PC
2327
```

```
                        .SBTTL  GLOBAL SUBROUTINES SECTION

                        ;++
                        ; THE GLOBAL SUBROUTINES SECTION CONTAINS THE SUBROUTINES
                        ; THAT ARE USED IN MORE THAN ONE TEST.
                        ;--

                        ;++
                        ; FUNCTIONAL DESCRIPTION:
                        ;    SUBROUTINE TO....SELECT AND INITIALIZE TARGET EMULATOR

                        ; INPUTS:
                        ;    LOCATION IDDEV CONTAINS USER DEFINED DEVICE NUMBER IN BITS 11-8
                        ;    LOCATION IDTYPE CONTAINS TARGET EMULATOR DEVICE TYPE AND GDAL BIT 15



                        ; IMPLICIT INPUTS:


                        ; OUTPUTS:
                        ;    R0LOAD CONTAINS USER DEFINED UNIT NUMBER IN BITS 11-8
                        ;    R2LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 2 WAS CLEARED
                        ;    R4LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 4 WAS CLEARED
                        ;    R6LOAD CONTAINS ALL ZEROES TO INDICATE MODE REGISTER WAS CLEARED
                        ;
                        ;    R0MASK EQUALS 0 TO CHECK ALL CONTROL REGISTER 0 BITS
                        ;    R6MASK EQUALS 0 TO CHECK ALL CONTROL REGISTER 6 BITS


                        ; IMPLICIT OUTPUTS:


                        ; SUBORDINATE ROUTINES USED:
                        ;    LDRDR0 ROUTINE TO LOAD, READ AND COMPARE REGISTER 0
                        ;    LDRDOR ROUTINE TO LOAD, READ AND COMPARE REGISTER 0 (USED FOR DEVICE TYPE)
                        ;    LDRDR2 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 2
                        ;    LDRDR4 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 4
                        ;    LDRDR6 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 6


                        ; FUNCTIONAL SIDE EFFECTS:
                        ;    TARGET EMULATOR SELECTED
                        ;    CONTROL REGISTER 0 LOW BYTE EQUALS 0 (GDAL 7:0)
                        ;    CONTROL REGISTER 2 EQUALS 0 (ADAL 15:0)
                        ;    CONTROL REGISTER 4 LOW BYTE EQUALS 0 (VDAL 15:0)
                        ;    CONTROL REGISTER 6 - HDAL 15:0 REGISTER EQUALS FOUR
                        ;    CONTROL REGISTER 6 - MODE REGISTER 15:0 EQUALS ZERO


                        ; CALLING SEQUENCE:
                        ;    JSR PC,INITTE

                        ;--
```

```
                                        ;NOTE:  ON A START OR RESTART COMMAND TO THE DIAGNOSTIC SUPERVISOR, A
                                        ;       BUS RESET INSTRUCTION WILL BE ISSUED TO CLEAR ALL MODULES.  THIS
                                        ;       IS NEEDED TO CLEAR SIGNALS COMING INTO THE TARGET EMULATOR THAT
                                        ;       MAY BE SET ON THE MEMORY SIMULATOR MODULE OR STATE ANALYZER MODULE.


005510                          INITTE::BGNSEG                          ;ROUTINE TO INIT TE MODULE
005510  104404                          TRAP    C$BSEG
005512                                  SETVEC  #4,#1$,#PRI07           ;SETUP VECTOR
005512  012746  000340                  MOV     #PRI07,-(SP)
005516  012746  005630                  MOV     #1$,-(SP)
005522  012746  000004                  MOV     #4,-(SP)
005526  012746  000003                  MOV     #3,-(SP)
005532  104437                          TRAP    C$SVEC
005534  062706  000010                  ADD     #10,SP

                                        ;LOAD DEVICE NUMBER INTO REGISTER 0 AND CHECK IT

005540  012737  000300  002324          MOV     #SSBRK!TOBRK,ROMASK     ;SETUP TO IGNORE TE BREAK SIGNALS
005546  013737  002310  002320          MOV     IDDEV,ROLOAD            ;GET USER DEFINED DEVICE NUMBER
005554  013737  002320  002322          MOV     ROLOAD,ROGOOD           ;PUT DATA LOADED INTO EXPECTED
005562  013777  002320  174510          MOV     ROLOAD,@REG0            ;WRITE WORD TO REGISTER 0
005570  017737  174504  002326          MOV     @REG0,ROBAD             ;READ REGISTER CONTENTS BACK
005576  043737  002324  002326          BIC     ROMASK,ROBAD            ;CLEAR OUT UNWANTED BITS
005604  023737  002322  002326          CMP     ROGOOD,ROBAD            ;COMPARE EXPECTED WITH THAT READ
005612  001414                          BEQ     2$                      ;IF COMPARE WAS GOOD THEN CONT
005614                                  ERRDF   1,GDALRG,ROEROR         ;DEVICE # OR LB NOT = EXPECTED
005614  104455                          TRAP    C$ERDF
005616  000001                          .WORD   1
005620  002406                          .WORD   GDALRG
005622  004754                          .WORD   ROEROR
005624                                  CKLOOP
005624  104406                          TRAP    C$CLP1
005626  000406                          BR      2$                      ;BRANCH AROUND TIME OUT ERROR
005630  005726                  1$:     TST     (SP)+                   ;CLEAN UP STACK
005632  005726                          TST     (SP)+                   ;CLEAN UP STACK
005634                                  ERRDF   1,,ROTM                 ;TIME OUT ERROR REG 0
005634  104455                          TRAP    C$ERDF
005636  000001                          .WORD   1
005640  000000                          .WORD   0
005642  005050                          .WORD   ROTM
005644                          2$:     CLRVEC  #4                      ;CLEAR VECTOR
005644  012700  000004                  MOV     #4,R0
005650  104436                          TRAP    C$CVEC
005652                                  ENDSEG
005652                          10000$:
005652  104405                          TRAP    C$ESEG

                                        ;READ DEVICE TYPE IN REGISTER 0 - DEVICE TYPE SHOULD EQUAL 0

005654                                  BGNSEG
005654  104404                          TRAP    C$BSEG
005656  052737  100000  002320          BIS     #GDAL15,ROLOAD          ;SETUP TO READ DEVICE TYPE
005664  013737  002316  002322          MOV     IDTYPE,ROGOOD           ;SETUP EXPECTED DATA
005672  004737  006562                  JSR     PC,LDRDOR               ;LOAD, READ AND COMPARE REG 0
```

```
2440  005676  001404                          BEQ     3$                      ;IF EQUAL THEN DEVICE TYPE COMPARED
2441  005700                                  ERRDF   1,GDALRG,ROEROR         ;DEVICE TYPE NOT EQUAL EXPECTED
2442  005700  104455                          TRAP    C$ERDF
2443  005702  000001                          .WORD   1
2444  005704  002406                          .WORD   GDALRG
2445  005706  004754                          .WORD   ROEROR
2446  005710                          3$:     ENDSEG
2447  005710                          10001$:
2448  005710  104405                          TRAP    C$ESEG
2449
2450                                          ;RESET THE SIGNAL GDAL15 H TO A 0 SO THAT THE DEVICE NUMBER WILL BE
2451                                          ;READ AGAIN.  SET GDAL1 H AND GDAL0 H TO ONES AND GDAL2 H TO A ZERO.
2452                                          ;THIS IS DONE SO THAT THE HDAL REGISTER CAN BE SELECTED AND INITIALIZED.
2453
2454  005712                                  BGNSEG
2455  005712  104404                          TRAP    C$BSEG
2456  005714  013737  002310  002320          MOV     IDDEV,ROLOAD            ;GET USER DEFINED DEVICE NUMBER
2457  005722  052737  000003  002320          BIS     #GDAL1!GDAL0,ROLOAD     ;SET BITS TO SELECT THE HDAL REGISTER
2458  005730  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
2459  005734  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
2460  005736                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL TO EXPECTED
2461  005736  104455                          TRAP    C$ERDF
2462  005740  000001                          .WORD   1
2463  005742  002406                          .WORD   GDALRG
2464  005744  004754                          .WORD   ROEROR
2465  005746                                  CKLOOP
2466  005746  104406                          TRAP    C$CLP1
2467
2468                                          ;LOAD, READ AND CHECK THE HDAL REGISTER WITH A DATA PATTERN OF FOUR.
2469                                          ;HDAL2 H SET TO A ONE WILL ENABLE THE PROGRAM TO GENERATE AND CONTROL
2470                                          ;THE T-11 TIMING AND CONTROL SIGNALS INSTEAD OF THE T-11 GENERATING THEM.
2471                                          ;ON A WRITE COMMAND TO CONTROL REIGSTER 6 WITH GDAL BITS 1 AND 0 SET,
2472                                          ;PULSES WILL OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H.  THESE
2473                                          ;PULSES WILL LOAD THE DATA INTO THE HDAL REGISTER.  ON A READ COMMAND
2474                                          ;TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REGISTER
2475                                          ;VIA THE SIGNAL RPT3 L.
2476
2477  005750                          4$:     SETVEC  #4,#5$,#PRI07           ;SETUP VECTOR
2478  005750  012746  000340                  MOV     #PRI07,-(SP)
2479  005754  012746  006056                  MOV     #5$,-(SP)
2480  005760  012746  000004                  MOV     #4,-(SP)
2481  005764  012746  000003                  MOV     #3,-(SP)
2482  005770  104437                          TRAP    C$SVEC
2483  005772  062706  000010                  ADD     #10,SP
2484  005776  012737  000004  002342          MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
2485  006004  005037  002346                  CLR     R6MASK                  ;SETUP MASK WORK TO COMPARE ALL BITS
2486  006010  013777  002342  174270          MOV     R6LOAD,@REG6            ;WRITE WORD INTO REG 6
2487  006016  017737  174264  002344          MOV     @REG6,R6READ            ;READ THE WORD BACK
2488  006024  043737  002346  002344          BIC     R6MASK,R6READ           ;CLEAR OUT ANY UNWANTED BITS
2489  006032  023737  002342  002344          CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED WITH DATA READ
2490  006040  001414                          BEQ     6$                      ;IF COMPARE WAS GOOD THEN CONT
2491  006042                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL TO EXPECTED
2492  006042  104455                          TRAP    C$ERDF
2493  006044  000004                          .WORD   4
2494  006046  002605                          .WORD   HDALRG
2495  006050  005020                          .WORD   R06ERR
```

```
                                        CKLOOP
006052  104406                          TRAP    C$CLP1
006054  000406                          BR      6$                      ;BRANCH AROUND TIME OUT ERROR
006056  005726                  5$:     TST     (SP)+                   ;CLEAN UP STACK
006060  005726                          TST     (SP)+                   ;CLEAN UP STACK
006062                                  ERRDF   4,,R6TM                 ;TIME OUT ERROR REG 6
006062  104455                          TRAP    C$ERDF
006064  000004                          .WORD   4
006066  000000                          .WORD   0
006070  005136                          .WORD   R6TM
006072                          6$:     CLRVEC  #4                      ;CLEAR VECTOR
006072  012700  000004                  MOV     #4,R0
006076  104436                          TRAP    C$CVEC
006100                                  ENDSEG
006100                          10002$:
006100  104405                          TRAP    C$ESEG

                                        ;SELECT THE MODE REGISTER BY SETTING GDAL BIT 2 TO A ONE AND GDAL BITS
                                        ;1 AND 0 TO ZEROES.  THIS IS DONE SO THAT THE MODE REGISTER CAN BE
                                        ;SELECTED AND CLEARED.

006102                                  BGNSEG
006102  104404                          TRAP    C$BSEG
006104  013737  002310  002320          MOV     IDDEV,ROLOAD            ;GET USER DEFINED DEVICE NUMBER
006112  052737  000004  002320          BIS     #GDAL2,ROLOAD           ;GET BIT TO SELECT MODE REGISTER
006120  004737  006554                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK MODE REGISTER
006124  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
006126                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
006126  104455                          TRAP    C$ERDF
006130  000001                          .WORD   1
006132  002406                          .WORD   GDALRG
006134  004754                          .WORD   ROEROR
006136                                  CKLOOP
006136  104406                          TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES.
                                        ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BIT 2 SET TO A ONE
                                        ;AND GDAL BITS 1 AND 0 SET TO ZEROES, PULSES WILL OCCUR ON THE SIGNALS
                                        ;WPT4 LB H AND WPT4 HB H.  THESE PULSES WILL LOAD THE DATA ON THE WRIT
                                        ;COMMAND INTO THE MODE REGISTER.  ON A READ COMMAND TO CONTROL REGISTER 6,
                                        ;DATA WILL BE READBACK FROM THE MODE REGISTER VIA THE SIGNAL RPT4 L.

006140  005037  002342          7$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES INTO MODE REG
006144  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
006150  001404                          BEQ     8$                      ;IF LOADED OK THEN CONTINUE
006152                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
006152  104455                          TRAP    C$ERDF
006154  000004                          .WORD   4
006156  002631                          .WORD   MODREG
006160  005020                          .WORD   R06ERR
006162                          8$:     ENDSEG
006162                          10003$:
006162  104405                          TRAP    C$ESEG

006164                                  BGNSEG
006164  104404                          TRAP    C$BSEG
```

```
2552
2553                                        ;SET AND CLEAR ADAL0 IN CONTROL REGISTER 2 TO CLEAR SINGLE STEP BREAK
2554                                        ;FLIP-FLOP. ALL OTHER BITS IN CONTROL REGISTER 2 WILL BE CLEARED.
2555                                        ;ADAL8 ON A ZERO WILL INHIBIT THE TIMEOUT BREAK ONE SHOT OUTPUT TO
2556                                        ;BE READ IN ITS LOGICAL STATE.  THE SIGNAL, TOBRK H, WILL BE ASSERTED
2557                                        ;LOW WHEN ADAL8 IS A ZERO.  AFTER SETTING AND CLEARING ADAL0 IN CONTROL
2558                                        ;REGISTER 2, THE TEST WILL READ CONTROL REGISTER 0 AND CHECK THAT SINGLE
2559                                        ;STEP BREAK FLIP-FLOP AND THE TIMEOUT BREAK SIGNALS ARE READBACK AS
2560                                        ;ZEORES.
2561
2562  006166                                SETVEC  #4,#9$,#PRI07           ;SETUP VECTOR
2563  006166  012746  000340               MOV     #PRI07,-(SP)
2564  006172  012746  006262               MOV     #9$,-(SP)
2565  006176  012746  000004               MOV     #4,-(SP)
2566  006202  012746  000003               MOV     #3,-(SP)
2567  006206  104437                       TRAP    C$SVEC
2568  006210  062706  000010               ADD     #10,SP
2569  006214  012737  000001  002330       MOV     #ADAL0,R2 JAD           ;SETUP BIT TO BE LOADED TO 0 SSBRK F/F
2570  006222  013777  002330  174052       MOV     R2LOAD,@REG2            ;WRITE BITS INTO REGISTER 2
2571  006230  017737  174046  002332       MOV     @REG    ,READ           ;READ REGISTER 2 BACK
2572  006236  023737  002330  002332       CMP     R2LOAD,READ             ;CHECK IF EXP EQUALS ACTUAL
2573  006244  001415                       BEQ     10$                     ;IF COMPARE WAS GOOD THEN CONT
2574  006246                                ERRDF   2,ADALRG,R2EROR         ;REG 2 NOT EQUAL TO ADAL 0
2575  006246  104455                       TRAP    C$ERDF
2576  006250  000002                       .WORD   2
2577  006252  002513                       .WORD   ADALRG
2578  006254  004770                       .WORD   R2EROR
2579  006256                                CKLOOP
2580  006256  104406                       TRAP    C$CLP1
2581  006260  000407                       BR      10$                     ;BRANCH AROUND TIME OUT ERROR
2582  006262  005726              9$:      TST     (SP)+                   ;CLEAN UP STACK
2583  006264  005726                       TST     (SP)+                   ;CLEAN UP STACK
2584  006266                                ERRDF   2,,R2TM                 ;TIME OUT ERROR REG 2
2585  006266  104455                       TRAP    C$ERDF
2586  006270  000002                       .WORD   2
2587  006272  000000                       .WORD   0
2588  006274  005072                       .WORD   R2TM
2589  006276                                CKLOOP
2590  006276  104406                       TRAP    C$CLP1
2591  006300                        10$:    CLRVEC  #4                      ;CLEAR VECTOR
2592  006300  012700  000004               MOV     #4,R0
2593  006304  104436                       TRAP    C$CVEC
2594  006306  005037  002330               CLR     R2LOAD                  ;SETUP TO CLEAR ADAL0
2595  006312  004737  006614               JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
2596  006316  001405                       BEQ     11$                     ;IF LOADED OK THEN CONTINUE
2597  006320                                ERRDF   2,ADALRG,R2EROR         ;REGISTER 2 NOT EQUAL EXPECTED
2598  006320  104455                       TRAP    C$ERDF
2599  006322  000002                       .WORD   2
2600  006324  002513                       .WORD   ADALRG
2601  006326  004770                       .WORD   R2EROR
2602  006330                                CKLOOP
2603  006330  104406                       TRAP    C$CLP1
2604
2605                                        ;LOAD, READ AND CHECK CONTROL REGISTER 0. CHECK THE TIMEOUT BREAK AND
2606                                        ;THE SINGLE STEP BREAK FLIP-FLOPS TO BE CLEARED AS A RESULT OF ADAL0 H
2607                                        ;BEING SET AND CLEARED IN THE PREVIOUS CHECK.
```

```
2608
2609  006332  005037  002324          11$:    CLR     R0MASK                  ;CLEAR MASK TO CHECK ALL BITS IN REG 0
2610  006336  105037  002320                  CLRB    R0LOAD                  ;SETUP TO CLEAR THE LOWER BYTE
2611  006342  004737  006554                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK GDAL REGISTER
2612  006346  001404                         BEQ     12$                     ;IF ALL BITS CHECKED THEN CONTINUE
2613  006350                                  ERRDF   1,GDALRG,R0EROR         ;REGISTER 0 NOT EQUAL TO DEVICE NUMBER
2614  006350  104455                         TRAP    C$ERDF
2615  006352  000001                         .WORD   1
2616  006354  002406                         .WORD   GDALRG
2617  006356  004754                         .WORD   R0EROR
2618  006360                          12$:    ENDSEG
2619  006360                          10004$:
2620  006360  104405                         TRAP    C$ESEG
2621
2622  006362                                  BGNSEG
2623  006362  104404                         TRAP    C$BSEG
2624
2625                                          ;SET AND CLEAR VDAL2 IN CONTROL REGISTER 4.  WHEN VDAL2 IS SET TO A
2626                                          ;ONE, THE PAUSE STATE MACHINE FLIP-FLOPS WILL BE CLEARED.  THESE F/F'S
2627                                          ;ARE READBACK IN VDAL REGISTER BITS 15:8.  THE REMAINING VDAL READ/
2628                                          ;WRITE BITS WILL BE LOADED AND CHECKED FOR ZEORES.
2629
2630  006364                                  SETVEC  #4,#13$,#PRI07          ;SETUP VECTOR
2631  006364  012746  000340                 MOV     #PRI07,-(SP)
2632  006370  012746  006466                 MOV     #13$,-(SP)
2633  006374  012746  000004                 MOV     #4,-(SP)
2634  006400  012746  000003                 MOV     #3,-(SP)
2635  006404  104437                         TRAP    C$SVEC
2636  006406  062706  000010                 ADD     #10,SP
2637  006412  012737  000004  002334        MOV     #VDAL2,R4LOAD           ;SETUP BIT TO BE LOADED
2638  006420  013737  002334  002336        MOV     R4LOAD,R4GOOD           ;SETUP EXPECTED DATA
2639  006426  013777  002334  173650        MOV     R4LOAD,@REG4            ;WRITE WORD INTO REGISTER 4
2640  006434  017737  173644  002340        MOV     @REG4,R4BAD             ;READ WORD BACK FROM REGISTER 4
2641  006442  023737  002336  002340        CMP     R4GOOD,R4BAD            ;COMPARE WORD EXPECTED WITH READ
2642  006450  001415                         BEQ     14$                     ;IF LOADED OK THEN CONT
2643  006452                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL TO 2
2644  006452  104455                         TRAP    C$ERDF
2645  006454  000003                         .WORD   3
2646  006456  002537                         .WORD   VDALRG
2647  006460  005004                         .WORD   R4EROR
2648  006462                                  CKLOOP
2649  006462  104406                         TRAP    C$CLP1
2650  006464  000407                         BR      14$                     ;BRANCH AROUND TIME OUT ERROR
2651
```

```
2652  006466  005726                  13$:    TST     (SP)+                   ;CLEAN UP STACK
2653  006470  005726                          TST     (SP)+                   ;CLEAN UP STACK
2654  006472                                  ERRDF   3,,R4TM                 ;TIME OUT ERROR REG 4
2655  006472  104455                          TRAP    C$ERDF
2656  006474  000003                          .WORD   3
2657  006476  000000                          .WORD   0
2658  006500  005114                          .WORD   R4TM
2659  006502                                  CKLOOP
2660  006502  104406                          TRAP    C$CLP1
2661  006504                          14$:    CLRVEC  #4                      ;CLEAR VECTOR
2662  006504  012700  000004                 MOV     #4,R0
2663  006510  104436                          TRAP    C$CVEC
2664  006512  005037  002334                 CLR     R4LOAD                  ;SETUP TO CLEAR VDAL2
2665  006516  004737  006640                 JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REG
2666  006522  001404                          BEQ     15$                     ;IF LOADED OK THEN CONTINUE
2667  006524                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REG NOT EQUAL TO 0
2668  006524  104455                          TRAP    C$ERDF
2669  006526  000003                          .WORD   3
2670  006530  002537                          .WORD   VDALRG
2671  006532  005004                          .WORD   R4EROR
2672  006534                          15$:    ENDSEG
2673  006534                          10005$:
2674  006534  104405                          TRAP    C$ESEG
2675
2676  006536  012737  000000  002324         MOV     #0,R0MASK               ;CLEAR CONTROL REGISTER 0 MASK WORD
2677  006544  012737  000000  002346         MOV     #0,R6MASK               ;CLEAR CONTROL REGISTER 6 MASK WORD
2678  006552  000207                          RTS     PC                      ;RETURN BACK TO TEST
2679
```

```
2680
2681                                    ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF REGISTER 0
2682                                    ;CONDITION CODES ARE SET ON EXIT AS RESULT OF THE ''CMP'' INSTRUCTION.
2683
2684  006554  013737  002320  002322  LDRDR0::MOV     R0LOAD,R0GOOD           ;PUT DATA LOADED INTO EXPECTED
2685  006562  013777  002320  173510  LDRD0R::MOV     R0LOAD,@REG0            ;WRITE WORD TO REGISTER 0
2686  006570  017737  173504  002326  READR0::MOV     @REG0,R0BAD             ;READ REGISTER CONTENTS BACK
2687  006576  043737  002324  002326          BIC     R0MASK,R0BAD            ;CLEAR OUT UNWANTED BITS
2688  006604  023737  002322  002326          CMP     R0GOOD,R0BAD            ;COMPARE EXPECTED WITH THAT READ
2689  006612  000207                          RTS     PC                      ;EXIT WITH CONDITION CODES SET
2690
2691                                    ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF REGISTER 2.
2692                                    ;CONDITION CODES ARE SET ON EXIT AS RESULT OF ''CMP'' INSTRUCTION
2693
2694  006614  013777  002330  173460  LDRDR2::MOV     R2LOAD,@REG2            ;WRITE BITS INTO REGISTER 2
2695  006622  017737  173454  002332  READR2::MOV     @REG2,R2READ            ;READ REGISTER 2 BACK
2696  006630  023737  002330  002332          CMP     R2LOAD,R2READ           ;CHECK IF EXP EQUALS ACTUAL
2697  006636  000207                          RTS     PC                      ;EXIT WITH CONDITION CODES SET
2698
2699                                    ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF REGISTER 4.
2700                                    ;CONDITION CODES ARE SET ON EXET AS RESULT OF ''CMP'' INSTRUCTION.
2701
2702  006640  013737  002334  002336  LDRDR4::MOV     R4LOAD,R4GOOD           ;SETUP EXPECTED DATA
2703  006646  013777  002334  173430  LDRD4R::MOV     R4LOAD,@REG4            ;WRITE WORD INTO REGISTER 4
2704  006654  017737  173424  002340  READR4::MOV     @REG4,R4BAD             ;READ WORD BACK FROM REGISTER 4
2705  006662  023737  002336  002340          CMP     R4GOOD,R4BAD            ;COMPARE WORD EXPECTED WITH READ
2706  006670  000207                          RTS     PC                      ;RETURN WITH CONDITION CODES SET
2707
2708                                    ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF CONTROL REGISTER 6
2709                                    ;CONDITION CODES ARE SET ON EXIT AS RESULT OF ''CMP'' INSTRUCTION.
2710
2711  006672  013777  002342  173406  LDRDR6::MOV     R6LOAD,@REG6            ;WRITE WORD INTO REGISTER 6
2712  006700  017737  173402  002344  READR6::MOV     @REG6,R6READ            ;READ THE WORD BACK
2713  006706  043737  002346  002344          BIC     R6MASK,R6READ           ;CLEAR OUT ANY UNWANTED BITS
2714  006714  023737  002342  002344          CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED WITH DATA READ
2715  006722  000207                          RTS     PC                      ;EXIT WITH CONDTION CODES SET
2716
2717                                    ;TARGET EMULATOR INTERRUPT SERVICE ROUTINE
2718
2719  006724                                  BGNSRV  INTSRV
2720  006724                          INTSRV::
2721  006724  017737  173350  002326          MOV     @REG0,R0BAD             ;READ GDAL REGISTER AND SAVE
2722  006732  012702  177777                  MOV     #-1,R2                  ;SET SOFTWARE INTERRUPT FLAG
2723  006736                                  ENDSRV  #PRI07
2724  006736                          L10013:
2725  006736  142766  000340  000002          BICB    #340,2(SP)
2726  006744  152766  000340  000002          BISB    #PRI07,2(SP)
2727  006752  000002                          RTI
2728
```

```
                                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0 TO
                                ;SELECT THE HDAL REGISTER.  THE HDAL REGISTER WILL BE SELECTED BY EITHER
                                ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6 WHEN GDAL BIT2 EQUALS A 0
                                ;AND GDAL BIT 1 AND GDAL BIT 0 EQUAL A ONE.

006754                          SLHDAL::BGNSEG
006754  104404                          TRAP    C$BSEG
006756  112737  000003  002320          MOVB    #GDAL1!GDAL0,ROLOAD     ;SETUP BITS TO BE SELECTED
006764  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REG
006770  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
006772                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
006772  104455                          TRAP    C$ERDF
006774  000001                          .WORD   1
006776  002406                          .WORD   GDALRG
007000  004754                          .WORD   ROEROR
007002                          1$:     ENDSEG
007002                          10000$:
007002  104405                          TRAP    C$ESEG
007004  000207                          RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0 TO
                                ;SELECT THE MODE REGISTER.  THE MODE REGISTER WILL BE SELECTED BY EITHER
                                ;A WRITE OR READ COMMAND TO CONTROL REGISTER 6 WHEN GDAL BIT 2 EQUALS A ONE
                                ;AND GDAL BIT 1 AND GDAL BIT 0 EQUALS A ZERO.

007006                          SLMODR::BGNSEG
007006  104404                          TRAP    C$BSEG
007010  112737  000004  002320          MOVB    #GDAL2,ROLOAD           ;SETUP BITS TO SELECT MODE REGISTER
007016  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
007022  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007024                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
007024  104455                          TRAP    C$ERDF
007026  000001                          .WORD   1
007030  002406                          .WORD   GDALRG
007032  004754                          .WORD   ROEROR
007034                          1$:     ENDSEG
007034                          10001$:
007034  104405                          TRAP    C$ESEG
007036  000207                          RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0 TO SELECT
                                ;THE ADDRESS BUS TO BE READBACK VIA THE SIGNAL RPT1 L WHEN A READ COMMAND IS
                                ;ISSUED TO CONTROL REGISTER 6.  ON A WRITE COMMAND TO CONTROL REGISTER 6, THE
                                ;NEW FORCE JUMP ADDRESS REG WILL BE LOADED WITH LSI-11 Q-BUS DATA BY THE SIGNALS
                                ;WPT1 LB H AND WPT1 HB H.  SELECT POINTER ONE BY SETTING GDAL0 H TO A ONE AND
                                ;GDAL1 H AND GDAL2 H TO A ZERO.

007040                          SLFJAR::BGNSEG
007040  104404                          TRAP    C$BSEG
007042  112737  000001  002320          MOVB    #GDAL0,ROLOAD           ;SETUP TO SET GDAL0 H TO A ONE
007050  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
007054  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007056                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
007056  104455                          TRAP    C$ERDF
007060  000001                          .WORD   1
007062  002406                          .WORD   GDALRG
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```
                                        .WORD   ROEROR
                                1$:     ENDSEG
                                10002$:
                                        TRAP    C$ESEG
                                        RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0 TO SELECT
                                ;THE DIAGNOSTICE ADDRESS REGISTER.  THE DIAGNOSTIC ADDRESS REGISTER WILL BE
                                ;SELECTED BY EITHER A WRITE OR READ COMMAND TO CONTROL REGISTER 6 WHEN GDAL
                                ;BITS 2:0 ARE EQUAL TO A ZERO.

007072                          SLDADR::BGNSEG
007072  104404                          TRAP    C$BSEG
007074  105037  002320                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
007100  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
007104  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007106                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
007106  104455                          TRAP    C$ERDF
007110  000001                          .WORD   1
007112  002406                          .WORD   GDALRG
007114  004754                          .WORD   ROEROR
007116                          1$:     ENDSEG
007116                          10003$:
007116  104405                          TRAP    C$ESEG
007120  000207                          RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 GDAL BITS 2:0
                                ;TO SELECT THE EODAL 15:0 BUS TO BE READBACK TO THE LSI-11 BUS WHEN
                                ;A READ COMMAND IS ISSUED TO CONTROL REGISTER 6.  CONTROL REGISTER 0
                                ;GDAL BITS 2:0 WILL BE SET TO ONES TO SELECT THE EODAL BUS READBACK.

007122                          SEODAL::BGNSEG
007122  104404                          TRAP    C$BSEG
007124  112737  000007  002320          MOVB    #GDAL2!GDAL1!GDAL0,ROLOAD ;SETUP BITS TO BE LOADED
007132  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
007136  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007140                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL TO EXPECTED
007140  104455                          TRAP    C$ERDF
007142  000001                          .WORD   1
007144  002406                          .WORD   GDALRG
007146  004754                          .WORD   ROEROR
007150                          1$:     ENDSEG
007150                          10004$:
007150  104405                          TRAP    C$ESEG
007152  000207                          RTS     PC

                                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 BITS 2:0 TO SELECT THE
                                ; FDAL REGISTER.  THE FDAL REGISTER WILL BE SELECTED BY EITHER A READ OR WRITE
                                ;COMMAND TO CONTROL REGISTER 6 WHEN GDAL BIT 1 IS SET TO A ONE AND GDAL BITS
                                ;2 AND 0 ARE SET TO ZEROES.

007154                          SLFDAL::BGNSEG
007154  104404                          TRAP    C$BSEG
007156  112737  000002  002320          MOVB    #GDAL1,ROLOAD           ;SETUP TO SET GDAL1 H TO A ONE
007164  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
007170  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
```

```
                                        ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
                                        TRAP    C$ERDF
                                        .WORD   1
                                        .WORD   GDALRG
                                        .WORD   ROEROR
                                1$:     ENDSEG
                                10005$:
                                        TRAP    C$ESEG
                                        RTS     PC

                                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 BITS 2:0 TO SELECT THE
                                ;TARGET MODE REGISTER.  THE TARGET MODE REGISTER WILL BE SELECTED ON A READ
                                ;COMMAND TO CONTROL REGISTER 6 WHEN GDAL BITS 2 AND 0 ARE SET AND GDAL BIT1
                                ;IS CLEARED.

007206                          SELTMR::BGNSEG
007206  104404                          TRAP    C$BSEG
007210  112737  000005  002320          MOVB    #GDAL2!GDAL0,ROLOAD     ;SETUP BITS TO BE LOADED
007216  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
007222  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007224                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
007224  104455                          TRAP    C$ERDF
007226  000001                          .WORD   1
007230  002406                          .WORD   GDALRG
007232  004754                          .WORD   ROEROR
007234                          1$:     ENDSEG
007234                          10006$:
007234  104405                          TRAP    C$ESEG
007236  000207                          RTS     PC

                                ;THE FOLLOWING ROUTINE WILL SETUP CONTROL REGISTER 0 BITS 2:0 TO SELECT THE
                                ;EIDAL BUS TO BE READBACK.  THE EIDAL BUS WILL BE SELECTED ON A READ COMMAND
                                ;TO CONTROL REGISTER 6 WHEN GDAL BITS 2 AND 1 ARE SET TO ONES AND GDAL BIT 0
                                ;IS A ZERO.

007240                          SEIDAL::BGNSEG
007240  104404                          TRAP    C$BSEG
007242  112737  000006  002320          MOVB    #GDAL2!GDAL1,ROLOAD     ;SETUP BITS TO BE LOADED
007250  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
007254  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007256                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
007256  104455                          TRAP    C$ERDF
007260  000001                          .WORD   1
007262  002406                          .WORD   GDALRG
007264  004754                          .WORD   ROEROR
007266                          1$:     ENDSEG
007266                          10007$:
007266  104405                          TRAP    C$ESEG
007270  000207                          RTS     PC
```

```
                                ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL12 IN THE HDAL REGISTER.  HDAL12
                                ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNALS ''XRAS L'' AND
                                ;''XRAS H''.  HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL
                                ;THE T-11 TIMING AND CONTROL SIGNALS.

007272  004737  007304        XRAS::  JSR     PC,XRASH                ;GO SET XRAS H (HIGH) AND XRAS L (LOW)
007276  004737  007336                JSR     PC,XRASL                ;GO SET XRAS H (LOW) AND XRAS L (HIGH)
007302  000207                        RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SET HDAL12 H AND HDAL2 H TO ONES.  HDAL2 H ON A ONE
                                ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
                                ;HDAL12 H ON A ONE WILL CAUSE THE SIGNAL XRAS H TO BE ASSERTED HIGH AND THE
                                ;SIGNAL XRAS L TO BE ASSERTED LOW

007304                          XRASH:: BGNSEG
007304  104404                        TRAP    C$BSEG
007306  052737  010004  002342        BIS     #HDAL12!HDAL2,R6LOAD    ;SETUP BIT TO BE LOADED
007314  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
007320  001404                        BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007322                                ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
007322  104455                        TRAP    C$ERDF
007324  000004                        .WORD   4
007326  002605                        .WORD   HDALRG
007330  005020                        .WORD   R06ERR
007332                          1$:     ENDSEG
007332                          10010$:
007332  104405                        TRAP    C$ESEG
007334  000207                        RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SET HDAL12 H TO A ZERO AND HDAL2 H TO A ONE.
                                ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND
                                ;CONTROL SIGNALS.  HDAL12 H ON A ZERO WILL CAUSE THE SIGNAL XRAS H TO BE
                                ;ASSERTED LOW AND THE SIGNAL XRAS L TO BE ASSERTED HIGH.

007336                          XRASL:: BGNSEG
007336  104404                        TRAP    C$BSEG
007340  052737  000004  002342        BIS     #HDAL2,R6LOAD           ;SETUP DIAGNOSTIC CONTROL BIT
007346  042737  010000  002342        BIC     #HDAL12,R6LOAD          ;SETUP BIT TO BE CLEARED
007354  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
007360  001404                        BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007362                                ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
007362  104455                        TRAP    C$ERDF
007364  000004                        .WORD   4
007366  002605                        .WORD   HDALRG
007370  005020                        .WORD   R06ERR
007372                          1$:     ENDSEG
007372                          10011$:
007372  104405                        TRAP    C$ESEG
007374  000207                        RTS     PC                      ;RETURN BACK TO TEST


                                ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL13 IN THE HDAL REGISTER.  HDAL13
                                ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNALS ''XCAS L'' AND
                                ;''XCAS H''.  HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL
                                ;THE T-11 TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
```

```
2946
2947  007376  004737  007410          XCAS::  JSR     PC,XCASH                ;GO SET XCAS H (HIGH) AND XCAS L (LOW)
2948  007402  004737  007442                  JSR     PC,XCASL                ;GO SET XCAS H (LOW) AND XCAS L (HIGH)
2949  007406  000207                          RTS     PC
2950
2951                                  ;THE FOLLOWING ROUTINE WILL SET HDAL13 H AND HDAL2 H TO ONES.  HDAL2 H ON A ONE
2952                                  ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.  HDAL13 H
2953                                  ;ON A ONE WILL CAUSE THE SIGNAL XCAS H TO BE ASSERTED HIGH AND THE SIGNAL XCAS L
2954                                  ;TO BE ASSERTED LOW.
2955
2956  007410                          XCASH:: BGNSEG
2957  007410  104404                          TRAP    C$BSEG
2958  007412  052737  020004  002342          BIS     #HDAL13!HDAL2,R6LOAD    ;SETUP BITS TO BE LOADED
2959  007420  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
2960  007424  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
2961  007426                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
2962  007426  104455                          TRAP    C$ERDF
2963  007430  000004                          .WORD   4
2964  007432  002605                          .WORD   HDALRG
2965  007434  005020                          .WORD   R06ERR
2966  007436                          1$:     ENDSEG
2967  007436                          10012$:
2968  007436  104405                          TRAP    C$ESEG
2969  007440  000207                          RTS     PC
2970
2971                                  ;THE FOLLOWING ROUTINE WILL SET HDAL13 H TO A ZERO AND HDAL2 H TO A ONE.
2972                                  ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND
2973                                  ;CONTROL SIGNALS.  HDAL13 H ON A ZERO WILL CAUSE THE SIGNAL XCAS H TO BE
2974                                  ;ASSERTED LOW AND THE SIGNAL XCAS L TO BE ASSERTED HIGH.
2975
2976  007442                          XCASL:: BGNSEG
2977  007442  104404                          TRAP    C$BSEG
2978  007444  052737  000004  002342          BIS     #BIT2,R6LOAD            ;SETUP DIAGNOSTIC CONTROL BIT
2979  007452  042737  020000  002342          BIC     #HDAL13,R6LOAD          ;SETUP BIT TO BE CLEARED
2980  007460  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
2981  007464  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
2982  007466                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
2983  007466  104455                          TRAP    C$ERDF
2984  007470  000004                          .WORD   4
2985  007472  002605                          .WORD   HDALRG
2986  007474  005020                          .WORD   R06ERR
2987  007476                          1$:     ENDSEG
2988  007476                          10013$:
2989  007476  104405                          TRAP    C$ESEG
2990  007500  000207                          RTS     PC                      ;RETURN BACK TO TEST
2991
2992                                  ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL15 IN THE HDAL REGISTER.  HDAL15
2993                                  ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNAL ''XPI H''.
2994                                  ;HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL THE T-11
2995                                  ;TIMING AND CONTROL SIGNALS SUCH AS ABOVE.
2996
2997  007502  004737  007514          XPI::   JSR     PC,XPIH                 ;GO SET PPI L AND XPI L TO THE LOW STATE
2998  007506  004737  007546                  JSR     PC,XPIL                 ;GO SET PPI L AND XPI L TO HIGH STATE
2999  007512  000207                          RTS     PC                      ;RETURN BACK TO TEST
3000
3001                                  ;THE FOLLOWING ROUTINE WILL SET HDAL15 H AND HDAL2 H TO ONES.  HDAL2 H ON A ONE
```

```
                                ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.  HDAL15 H
                                ;ON A ONE WILL ASSERT THE SIGNALS PPI L AND XPI L TO THE LOW STATE.

007514                          XPIH::  BGNSEG
007514  104404                          TRAP    C$BSEG
007516  052737  100004  002342          BIS     #HDAL15!HDAL2,R6LOAD    ;SETUP BITS TO BE LOADED
007524  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
007530  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007532                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
007532  104455                          TRAP    C$ERDF
007534  000004                          .WORD   4
007536  002605                          .WORD   HDALRG
007540  005020                          .WORD   R06ERR
007542                          1$:     ENDSEG
007542                          10014$:
007542  104405                          TRAP    C$ESEG
007544  000207                          RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SET HDAL15 H TO A ZERO AND HDAL2 H TO A ONE.  HDAL2 H
                                ;ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
                                ;HDAL15 H ON A ZERO WILL CAUSE THE SIGNALS PPI L AND XPI L TO BE ASSERTED HIGH.

007546                          XPIL::  BGNSEG
007546  104404                          TRAP    C$BSEG
007550  052737  000004  002342          BIS     #HDAL2,R6LOAD           ;SETUP DIAGNOSTIC CONTROL BIT
007556  042737  100000  002342          BIC     #HDAL15,R6LOAD          ;SETUP BIT TO BE CLEARED
007564  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
007570  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007572                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
007572  104455                          TRAP    C$ERDF
007574  000004                          .WORD   4
007576  002605                          .WORD   HDALRG
007600  005020                          .WORD   R06ERR
007602                          1$:     ENDSEG
007602                          10015$:
007602  104405                          TRAP    C$ESEG
007604  000207                          RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SET AND CLEAR HDAL7 IN THE HDAL REGISTER.  HDAL7
                                ;BEING SET AND CLEARED WILL CAUSE A PULSE TO OCCUR ON THE SIGNAL XBCLR H + PBCLR H.
                                ;HDAL2 H WILL ALSO BE SET TO A ONE TO ALLOW THE PROGRAM TO CONTROL THE T-11
                                ;TIMING AND CONTROL SIGNALS SUCH AS ABOVE.

007606  004737  007620          XBCLR:: JSR     PC,XBCLRH               ;SET XBCLR H AND PBCLR H TO HIGH STATE
007612  004737  007652                  JSR     PC,XBCLRL               ;SET XBCLR H AND PBCLR H TO LOW STATE
007616  000207                          RTS     PC                      ;RETURN BACK TO TEST

                                ;THE FOLLOWING ROUTINE WILL SET HDAL7 H AND HDAL2 H TO ONES.  HDAL2 H ON A ONE
                                ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.  HDAL7 H
                                ;ON A ONE WILL ASSERT THE SIGNALS XBCLR H AND PBCLR H TO THE HIGH STATE

007620                          XBCLRH::BGNSEG
007620  104404                          TRAP    C$BSEG
007622  052737  000204  002342          BIS     #HDAL7!HDAL2,R6LOAD     ;SETUP BITS TO BE LOADED
007630  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
007634  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
```

```
3058  007636                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
3059  007636  104455                          TRAP    C$ERDF
3060  007640  000004                          .WORD   4
3061  007642  002605                          .WORD   HDALRG
3062  007644  005020                          .WORD   R06ERR
3063  007646                          1$:     ENDSEG
3064  007646                          10016$:
3065  007646  104405                          TRAP    C$ESEG
3066  007650  000207                          RTS     PC                      ;RETURN BACK TO TEST
3067
3068                                  ;THE FOLLOWING ROUTINE WILL SET HDAL7 H TO A ZERO AND HDAL2 H TO A ONE.  HDAL2 H
3069                                  ;ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
3070                                  ;HDAL7 H ON A ZERO WILL CAUSE THE SIGNALS XBCLR H AND PBCLR H TO BE ASSERTED LOW
3071
3072  007652                          XBCLRL::BGNSEG
3073  007652  104404                          TRAP    C$BSEG
3074  007654  052737  000004  002342          BIS     #HDAL2,R6LOAD           ;SETUP DIAGNOSTIC CONTROL BIT
3075  007662  042737  000200  002342          BIC     #HDAL7,R6LOAD           ;SETUP BIT TO BE CLEARED
3076  007670  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
3077  007674  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
3078  007676                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
3079  007676  104455                          TRAP    C$ERDF
3080  007700  000004                          .WORD   4
3081  007702  002605                          .WORD   HDALRG
3082  007704  005020                          .WORD   R06ERR
3083  007706                          1$:     ENDSEG
3084  007706                          10017$:
3085  007706  104405                          TRAP    C$ESEG
3086  007710  000207                          RTS     PC                      ;RETURN BACK TO TEST
3087
```

```
                                ;THE FOLLOWING ROUTINE WILL SET AND CLEAR VDAL2 H IN CONTROL REGISTER 4.  VDAL2 H
                                ;ON A ONE WILL CLEAR THE FOLLOWING FLIP-FLOPS:
                                ;    PAUSE STATE WORKINC          PSMW H  0
                                ;    PAUSE STATE SYNC             EPSF H  0
                                ;    16 BIT ADDRESS               EPFN H  0
                                ;    8 BIT INSTRUCTION HB         EP8F H  0
                                ;    8 BIT ADDRESS LB             EP8G H  0
                                ;    8 BIT ADDRESS HB             EP8N H  0
                                ;    TAKE NEW F.J. ADDRESS        TNFI H  0
                                ;    GET NEW ADDRESS FLIP-FLOP    OUT NEW H
                                ;    PAUSE MODE FLIP-FLOP         PAUSE L 0
                                ;    REFRESH FLIP-FLOP            REFR H  0
                                ;    FETCT LATCH FLIP-FLOP        EDFET H 0
                                ;SETTING AND CLEARING VDAL2 H WILL ALSO CLOCK THE TAI AND TDAL BUSSES INTO THE
                                ;DIAGNOSTIC LATCHES.

007712                          CLRPSM::BGNSEG
007712  104404                          TRAP    C$BSEG
007714  052737  000004  002334          BIS     #VDAL2,R4LOAD           ;SETUP BIT TO SET VDAL2 H TO A ONE
007722  004737  006640                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REGISTER
007726  001405                          BEQ     1$                      ;IF ALL OTHER BITS CLEARED THEN CONT
007730                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REG OR PAUSE STATE MACHINE ERROR
007730  104455                          TRAP    C$ERDF
007732  000003                          .WORD   3
007734  002537                          .WORD   VDALRG
007736  005004                          .WORD   R4EROR
007740                                  CKLOOP
007740  104406                          TRAP    C$CLP1
007742  042737  000004  002334  1$:     BIC     #VDAL2,R4LOAD           ;SETUP TO CLEAR VDAL2 H
007750  004737  006640                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REGISTER
007754  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
007756                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
007756  104455                          TRAP    C$ERDF
007760  000003                          .WORD   3
007762  002537                          .WORD   VDALRG
007764  005004                          .WORD   R4EROR
007766                          2$:     ENDSEG
007766                          10020$:
007766  104405                          TRAP    C$ESEG
007770  000207                          RTS     PC                      ;RETURN BACK TO TEST
```

```
                                ;THE FOLLOWING ROUTINE WILL SET ADAL0 H TO A ONE AND THEN ZERO.  ADAL0 H BEING
                                ;SET AND CLEARED WILL CAUSE A PULSE ON THE SIGNAL 'BRKRES L".  THE SIGNAL
                                ;'BRKRES L" WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP AND INTERRUPT RELATED
                                ;LOGIC.

007772                          BRKRES::BGNSEG
007772  104404                          TRAP    C$BSEG
007774  052737  000001  002330          BIS     #ADAL0,R2LOAD           ;SETUP BIT TO BE LOADED
010002  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
010006  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010010                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
010010  104455                          TRAP    C$ERDF
010012  000002                          .WORD   2
010014  002513                          .WORD   ADALRG
010016  004770                          .WORD   R2EROR
010020                                  CKLOOP
010020  104406                          TRAP    C$CLP1
010022  042737  000001  002330  1$:     BIC     #ADAL0,R2LOAD           ;SETUP BIT TO BE CLEARED
010030  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
010034  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010036                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
010036  104455                          TRAP    C$ERDF
010040  000002                          .WORD   2
010042  002513                          .WORD   ADALPG
010044  004770                          .WORD   R2EROR
010046                          2$:     ENDSEG
010046                          10021$:
010046  104405                          TRAP    C$ESEG
010050  000207                          RTS     PC                      ;RETRUN BACK TO TEST

010052                          ENDMOD
```

```
                                        .TITLE MISCELLANEOUS SECTIONS
                                        .SBTTL  REPORT CODING SECTION

010052                                          BGNMOD

                                        ;++
                                        ; THE REPORT CODING SECTION CONTAINS THE
                                        ; "PRINTS" CALLS THAT GENERATE STATISTICAL REPORTS.
                                        ;--

010052                                          BGNRPT
010052                                  L$RPT::

010052                                          EXIT    RPT
010052  000167                                  .WORD   J$JMP
010054  000000                                  .WORD   L10014-2-.

                                                .EVEN

010056                                          ENDRPT
010056                                  L10014:
010056  104425                                  TRAP    C$RPT

                                        .SBTTL  PROTECTION TABLE

                                        ;++
                                        ; THIS TABLE IS USED BY THE RUNTIME SERVICES
                                        ; TO PROTECT THE LOAD MEDIA.
                                        ;--

010060                                          BGNPROT
010060                                  L$PROT::

010060  177777                                  -1              ;OFFSET INTO P-TABLE FOR CSR ADDRESS
010062  177777                                  -1              ;OFFSET INTO P-TABLE FOR MASSBUS ADDRESS
010064  177777                                  -1              ;OFFSET INTO P-TABLE FOR DRIVE NUMBER

010066                                          ENDPROT
```

```
                                .SBTTL  INITIALIZE SECTION

                                ;++
                                ; THE INITIALIZE SECTION CONTAINS THE CODING THAT IS PERFORMED
                                ; AT THE BEGINNING OF EACH PASS.
                                ;--

010066                                  BGNINIT
010066                          L$INIT::
010066                                  READEF  #EF.START               ;SEE IF A START COMMAND
010066  012700  000040                  MOV     #EF.START,R0
010072  104447                          TRAP    C$REFG
010074                                  BCOMPLETE       1$              ;BRANCH IF START COMMAND
010074  103410                          BCS     1$
010076                                  READEF  #EF.RESTART             ;SEE IF A RESTART COMMAND
010076  012700  000037                  MOV     #EF.RESTART,R0
010102  104447                          TRAP    C$REFG
010104                                  BCOMPLETE       1$              ;BRANCH IF RESTART
010104  103404                          BCS     1$
010106                                  READEF  #EF.PWR                 ;SEE IF RECOVERING FROM A POWER FAIL
010106  012700  000034                  MOV     #EF.PWR,R0
010112  104447                          TRAP    C$REFG
010114                                  BNCOMPLETE      2$              ;IF NOT CHECK IN CONTINUE
010114  103014                          BCC     2$
010116                          1$:     BRESET                          ;ISSUE A BUS RESET
010116  104433                          TRAP    C$RESET
010120                                  SETVEC  #100,#102,#RTI          ;SETUP CLOCK VECTOR TO DO A RETURN
010120  012746  000002                  MOV     #RTI,-(SP)
010124  012746  000102                  MOV     #102,-(SP)
010130  012746  000100                  MOV     #100,-(SP)
010134  012746  000003                  MOV     #3,-(SP)
010140  104437                          TRAP    C$SVEC
010142  062706  000010                  ADD     #10,SP
010146                          2$      READEF  #EF.NEW                 ;SEE IF A NEW PASS
010146  012700  000035                  MOV     #EF.NEW,R0
010152  104447                          TRAP    C$REFG
010154                                  BNCOMPLETE      3$              ;IF NOT GO CHECK IF CONTINUE
010154  103003                          BCC     3$
010156  012737  177777  002314          MOV     #-1,UNITNB              ;SETUP TO INIT UNIT NUMBER
010164                          3$:     READEF  #EF.CONTINUE            ;CHECK IF CONTINUE
010164  012700  000036                  MOV     #EF.CONTINUE,R0
010170  104447                          TRAP    C$REFG
010172                                  BCOMPLETE       6$              ;IF YES THEN EXIT
010172  103433                          BCS     6$
010174  005237  002314          4$:     INC     UNITNB                  ;INC TO NEW UNIT NUMBER
010200                                  GPHARD  UNITNB,R5               ;GET DEVICE INFORMATION
010200  013700  002314                  MOV     UNITNB,R0
010204  104442                          TRAP    C$GPHRD
010206  010005                          MOV     R0,R5
010210                                  BNCOMPLETE      4$              ;GO TRY ANOTHER UNIT
010210  103371                          BCC     4$
010212  012701  002300                  MOV     #REG0,R1                ;ADDRESS OF ED DEVICE ADDRESS TABLE
010216  005002                          CLR     R2                      ;CLEAR OFFSET TO ADD TO TABLE ADDRESS
010220  011511                  5$:     MOV     (R5),(R1)               ;GET ADDRESS AND SAVE
010222  060221                          ADD     R2,(R1)+                ;ADD OFFSET TO ADDRESS
010224  005202                          INC     R2                      ;UPDATE OFFSET BY 2
```

```
3261  010226  005202                        INC     R2                      ;
3262  010230  022702  000010                CMP     #10,R2                  ;CHECK IF DONE LOADING TABLE
3263  010234  001371                        BNE     5$                      ;GO UPDATE NEXT ADDRESS
3264  010236  005725                        TST     (R5)+                   ;UPDATE THE POINTER
3265  010240  012537  002312                MOV     (R5)+,TEVECT            ;GET TARGET EMULATOR VECTOR ADDRES
3266  010244  005037  002310                CLR     IDDEV                   ;CLEAR OUT DEVICE NUMBER
3267  010250  111537  002311                MOVB    (R5),IDDEV+1            ;GET THE TE DEVICE NUMBER
3268  010254  012737  100000  002316        MOV     #GDAL15,IDTYPE          ;SETUP TE DEVICE TYPE
3269  010262                          6$:   SETPRI  #PRI07                  ;RAISE PROCESSOR PRIORITY
3270  010262  012700  000340                MOV     #PRI07,R0
3271  010266  104441                        TRAP    C$SPRI
3272
3273
3274  010270                                EXIT    INIT
3275  010270  104432                        TRAP    C$EXIT
3276  010272  000002                        .WORD   L10016-.
3277
3278
3279                                        .EVEN
3280
3281  010274                                ENDINIT
3282  010274                          L10016:
3283  010274  104411                        TRAP    C$INIT
```

```
                                        .SBTTL  AUTODROP SECTION

                                        ;++
                                        ; THIS CODE IS EXECUTED IMMEDIATELY AFTER THE INITIALIZE CODE IF
                                        ; THE "ADR" FLAG WAS SET.  THE UNIT(S) UNDER TEST ARE CHECKED TO
                                        ; SEE IF THEY WILL RESPOND.  THOSE THAT DON'T ARE IMMEDIATELY
                                        ; DROPPED FROM TESTING.
                                        ;--

010276                                          BGNAUTO
010276                                  L$AUTO::


010276                                          ENDAUTO
010276                                  L10017:
010276  104461                                  TRAP    C$AUTO

                                        .SBTTL  CLEANUP CODING SECTION

                                        ;++
                                        ; THE CLEANUP CODING SECTION CONTAINS THE CODING THAT IS PERFORMED
                                        ; AFTER THE HARDWARE TESTS HAVE BEEN PERFORMED.
                                        ;--

010300                                          BGNCLN
010300                                  L$CLEAN::
010300                                          SETPRI  #PRI07                  ;RAISE THE CPU PRIORITY LEVEL TO 7
010300  012700  000340                          MOV     #PRI07,R0
010304  104441                                  TRAP    C$SPRI
010306  013777  002310  171764                  MOV     IDDEV,@REG0             ;CLEAR CONTROL REGISTER 0 EXCEPT
                                                                                ;FOR DEVICE NUMBER
010314  012777  000000  171760                  MOV     #0,@REG2                ;CLEAR REGISTER 2


010322                                          EXIT    CLN
010322  104432                                  TRAP    C$EXIT
010324  000002                                  .WORD   L10020-.


                                        .EVEN

010326                                          ENDCLN
010326                                  L10020:
010326  104412                                  TRAP    C$CLEAN
```

```
                                        .SBTTL  DROP UNIT SECTION

                                        ;++
                                        ; THE DROP-UNIT SECTION CONTAINS THE CODING THAT CAUSES A DEVICE
                                        ; TO NO LONGER BE TESTED.
                                        ;--

                                                BGNDU
                                        L$DU::

                                                EXIT    DU
                                                .WORD   J$JMP
                                                .WORD   L10021-2-.


                                                .EVEN

                                                ENDDU
                                        L10021:
                                                TRAP    C$DU

                                        .SBTTL  ADD UNIT SECTION

                                        ;++
                                        ; THE ADD-UNIT SECTION CONTAINS ANY CODE THE PROGRAMMER WISHES
                                        ;  TO BE EXECUTED IN CONJUNCTION WITH THE ADDING OF A UNIT BACK
                                        ;  TO THE TEST CYCLE.
                                        ;--

                                                BGNAU
                                        L$AU::

                                                EXIT    AU
                                                .WORD   J$JMP
                                                .WORD   L10022-2-.


                                                .EVEN

                                                ENDAU
                                        L10022:
                                                TRAP    C$AU

                                                ENDMOD
```

```
                                .TITLE HARDWARE TESTS

                                .SBTTL  TEST 1: SELECT AND INITIALIZE TARGET EMULATOR

010344                                  BGNMOD

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TARGET EMULATOR MODULE CAN BE SELECTED AND
                                ; INITIALIZED TO A KNOWN STATE.  THE TEST DESCRIBED BELOW WILL BE EXECUTED AT
                                ; THE BEGINNING OF EACH TEST TO PUT THE TARGET EMULATOR IN A KNOWN STATE.
                                ;
                                ; THE TEST WILL LOAD AND CHECK THAT THE DEVICE NUMBER CAN BE LOADED INTO AND
                                ; READ FROM CONTROL REGISTER 0.  ALL THE READ/WRITE BITS WILL BE LOADED AND
                                ; CHECKED FOR ZEROES.  THE TEST WILL CHECK THAT THE TARGET EMULATOR DEVICE
                                ; TYPE CAN BE READ BY SETTING CONTROL REGISTER 0 BIT 15 TO A ONE AND THEN
                                ; READING CONTROL REGISTER 0.  THE TEST WILL SET CONTROL REGISTER 0 BIT 15 TO
                                ; A ZERO AND BITS 1 AND 0 TO ONES.  BIT 15 ON A ZERO WILL ENABLE THE DEVICE
                                ; NUMBER TO BE READ AGAIN.  BITS 1 AND 0 SET TO ONES WILL CAUSE THE HDAL
                                ; REGISTER TO BE SELECTED ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
                                ; THE TEST WILL NOW LOAD, READ AND CHECK THE HDAL REGISTER WITH HDAL BIT 2
                                ; SET TO A ONE AND ALL OTHER HDAL BITS CLEARED.  HDAL BIT 2 SET TO A ONE WILL
                                ; ENABLE THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS USING THE
                                ; BITS IN THE HDAL REGISTER.  THE TEST WILL NOW SET CONTROL REGISTER 0 BITS
                                ; 1 AND 0 TO ZEROES AND BIT 2 TO A ONE.  CONTROL REGISTER 0 BIT 2 ON A ONE WILL
                                ; CAUSE THE MODE REGISTER TO BE SELETCED ON A WRITE OR READ COMMAND TO CONTROL
                                ; REGISTER 6.  THE TEST WILL LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA
                                ; PATTERN OF ALL ZEROES.  MODE REGISTER BIT 11 ON A ZERO WILL CAUSE 16 BIT
                                ; ADDRESS MODE TO BE SELECTED.  THE TEST WILL SET ADAL REGISTER BIT 0 TO A 1
                                ; AND THEN A ZERO.  ALL OTHER ADAL REGISTER BITS WILL BE LOADED AND CHECKED FOR
                                ; ZEROES.  ADAL REGISTER BIT 0 BEING SET TO A ONE WILL CLEAR THE BREAK LATCH
                                ; FLIP-FLOP, THE SINGLE STEP BREAK FLIP-FLOP AND THE MEMORY SIMULATOR BREAK
                                ; FLIP-FLOP.  ADAL REGISTER BIT 2 ON A ZERO WILL CAUSE THE T-11 CHIP TO BE
                                ; TURNED OFF.  THE TEST WILL THEN READ AND CHECK CONTROL REGISTER 0 TO CHECK
                                ; THAT ALL THE BREAK BITS ARE CLEARED.  THE TEST WILL NOW SET VDAL REGISTER
                                ; BIT 2 TO A ONE AND THEN A ZERO.  ALL OTHER VDAL READ/WRITE BITS WILL BE
                                ; LOADED AND CHECKED FOR ZEROES.  VDAL REGISTER BIT 2 ON A ONE WILL CAUSE ALL
                                ; THE FLIP-FLOPS ON THE TARGET EMULATOR MODULE, EXCEPT THOSE CLEARED BY ADAL
                                ; REGISTER BIT 0, TO BE SET TO A KNOWN STATE.
                                ;--


010344                                  BGNTST
010344                          T1::
010344  004737  005510                  JSR     PC,INITTE               ;INITIALIZE THE TARGET EMULATOR


010350                                  ENDTST
010350                          L10023:
010350  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 2: GDAL 3:0 R/W REG TEST (1'S AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS, GDAL 3:0, CAN
                                ; BE SET TO ALL ONES (17), AND THEN SET TO ALL ZEROES.  THE READ ONLY BITS,
                                ; GDAL7:4, ARE CHECKED TO BE CLEARED DURING THIS TEST.
                                ;--

010352                                  BGNTST
010352                          T2::
010352  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

010356                                  BGNSEG
010356  104404                          TRAP    C$BSEG

                                        ;CHECK THAT R/W BITS GDAL 3:0 CAN BE SET TO ALL ONES

010360  112737  000017  002320          MOVB    #17,ROLOAD              ;SETUP BITS TO BE LOADED
010366  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
010372  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010374                                  ERRDF   1,GDALRG,ROEROR         ;REGISTER 0 NOT EQUAL 17
010374  104455                          TRAP    C$ERDF
010376  000001                          .WORD   1
010400  002406                          .WORD   GDALRG
010402  004754                          .WORD   ROEROR
010404                          1$:     ENDSEG
010404                          '0000$:
010404  104405                          TRAP    C$ESEG

010406                                  BGNSEG
010406  104404                          TRAP    C$BSEG

                                        ;CHECK THAT R/W BITS GDAL 3:0 CAN BE SET TO ALL ZEROES

010410  105037  002320                  CLRB    ROLOAD                  ;SETUP TO CLEAR ALL BITS
010414  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
010420  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010422                                  ERRDF   1,GDALRG,ROEROR         ;REGISTER 0 R/W BITS NOT EQUAL 0
010422  104455                          TRAP    C$ERDF
010424  000001                          .WORD   1
010426  002406                          .WORD   GDALRG
010430  004754                          .WORD   ROEROR
010432                          2$:     ENDSEG
010432                          10001$:
010432  104405                          TRAP    C$ESEG
010434                                  ENDTST
010434                          L10024:
010434  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 3: GDAL 3:0 R/W REG TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS GDAL 3:0, CAN
                                ; BE LOADED WITH ONES AND ZEORES (12) AND THEN LOADED WITH ZEROES AND ONES (5).
                                ; THE READ ONLY BITS GDAL 7:4 ARE CHECKED TO BE CLEARED DURING THIS TEST.
                                ;--

010436                                  BGNTST
010436                          T3::
010436  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

010442                                  BGNSEG
010442  104404                          TRAP    C$BSEG

                                        ;LOAD READ/WRITE BITS GDAL 3:0 WITH AN ALTERNATING ONES AND ZEROES DATA
                                        ;PATTERN (12).

010444  112737  000012  002320          MOVB    #12,ROLOAD              ;SETUP BITS TO BE LOADED
010452  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
010456  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010460                                  ERRDF   1,GDALRG,ROEROR         ;REGISTER 0 NOT EQUAL TO 12
010460  104455                          TRAP    C$ERDF
010462  000001                          .WORD   1
010464  002406                          .WORD   GDALRG
010466  004754                          .WORD   ROEROR
010470                          1$:     ENDSEG
010470                          10000$:
010470  104405                          TRAP    C$ESEG

010472                                  BGNSEG
010472  104404                          TRAP    C$BSEG

                                        ;LOAD READ/WRITE BITS GDAL 3:0 WITH AN ALTERNATING ZEROES AND ONES DATA
                                        ;PATTERN

010474  112737  000005  002320          MOVB    #5,ROLOAD               ;SETUP BITS TO BE LOADED
010502  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
010506  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010510                                  ERRDF   1,GDALRG,ROEROR         ;REGISTER 0 NOT EQUAL TO 5
010510  104455                          TRAP    C$ERDF
010512  000001                          .WORD   1
010514  002406                          .WORD   GDALRG
010516  004754                          .WORD   ROEROR
010520                          2$:     ENDSEG
010520                          10001$:
010520  104405                          TRAP    C$ESEG
010522                                  ENDTST
010522                          L10025:
010522  104401                          TRAP    C$ETST
```

```
                        .SBTTL  TEST 4: GDAL 3:0 R/W REG TEST VIA BINARY COUNT

                        ;++
                        ; THIS TEST WILL CHECK CONTROL REGISTER 0 R/W BITS USING A BINARY COUNT PATTERN.
                        ; THE PATTERN WILL START INITIALLY AT 0 AND INCREMENT BY ONE UNTIL THE PATTERN
                        ; EQUALS 17.  THE READ ONLY BITS, GDAL 7:4, ARE CHECKED TO BE CLEARED DURING
                        ; THIS TEST.
                        ;--

010524                          BGNTST
010524                  T4::
010524  004737  0055'0          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

010530  105037  002320          CLRB    ROLOAD                  ;SETUP TO START PATTERN AT 0

010534                  1$:     BGNSEG
010534  104404                  TRAP    C$BSEG
010536  004737  006554          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK CONTROL REG 0
010542  001404                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010544                          ERRDF   1,GDALRG,ROEROR         ;REGISTER 0 NOT EQUAL EXPECTED
010544  104455                  TRAP    C$ERDF
010546  000001                  .WORD   1
010550  002406                  .WORD   GDALRG
010552  004754                  .WORD   ROEROR
010554                  2$:     ENDSEG
010554                  10000$:
010554  104405                  TRAP    C$ESEG
010556  005237  002320          INC     ROLOAD                  ;UPDATE REGISTER 0 BY ONE
010562  122737  000020  002320  CMPB    #20,ROLOAD              ;CHECK IF ALL R/W BITS TESTED
010570  001361                  BNE     1$                      ;IF NOT THEN LOAD NEXT PATTERN
010572                          ENDTST
010572                  L10026:
010572  104401                  TRAP    C$ETST

```

```
                                .SBTTL  TEST 5: ADAL 15:0 REG TEST (1'S AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT CONTROL REGISTER 2 BITS ADAL 15:0 CAN BE SET TO
                                ; ALL ONES (177777) AND THEN ALL ZEORES (000000).
                                ;--

010574                                  BGNTST
010574                          T5::
010574  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

010600                                  BGNSEG
010600  104404                          TRAP    C$BSEG

                                        ;LOAD, READ AND CHECK CONTROL REGISTER 2 WITH A DATA PATTERN OF ALL ONES

010602  012737  177777  002330          MOV     #177777,R2LOAD          ;SETUP FOR ALL ONES DATA PATTERN
010610  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
010614  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010616                                  ERRDF   2,ADALRG,R2EROR         ;REGISTER 2 NOT EQUAL 177777
010616  104455                          TRAP    C$ERDF
010620  000002                          .WORD   2
010622  002513                          .WORD   ADALRG
010624  004770                          .WORD   R2EROR
010626                          1$:     ENDSEG
010626                          10000$:
010626  104405                          TRAP    C$ESEG

010630                                  BGNSEG
010630  104404                          TRAP    C$BSEG

                                        ;LOAD, READ AND CHECK CONTROL REG 2 WITH A DATA PATTERN OF ALL ZEROES.

010632  005037  002330                  CLR     R2LOAD                  ;SETUP ALL ZEROES DATA PATTERN
010636  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
010642  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010644                                  ERRDF   2,ADALRG,R2EROR         ;REGISTER 2 NOT EQUAL TO 000000
010644  104455                          TRAP    C$ERDF
010646  000002                          .WORD   2
010650  002513                          .WORD   ADALRG
010652  004770                          .WORD   R2EROR
010654                          2$:     ENDSEG
010654                          10001$:
010654  104405                          TRAP    C$ESEG
010656                                  ENDTST
010656                          L10027:
010656  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 6: ADAL 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 15:0 WITH AN
                                ; ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN WITH AN ALTERNATING
                                ; ZEROES AND ONES DATA PATTERN (052525).
                                ;--

010660                                  BGNTST
010660                          T6::
010660  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

010664                                  BGNSEG
010664  104404                          TRAP    C$BSEG

                                        ;LOAD, READ AND CHECK CONTROL REGISTER 2 WITH AN ALTERNATING ONES AND
                                        ;ZEORES DATA PATTERN (125252)

010666  012737  125252  002330          MOV     #125252,R2LOAD          ;SETUP DATA PATTERN TO BE LOADED
010674  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
010700  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010702                                  ERRDF   2,ADALRG,R2EROR         ;REGISTER 2 NOT EQUAL 125252
010702  104455                          TRAP    C$ERDF
010704  000002                          .WORD   2
010706  002513                          .WORD   ADALRG
010710  004770                          .WORD   R2EROR
010712                          1$:     ENDSEG
010712                          10000$:
010712  104405                          TRAP    C$ESEG

010714                                  BGNSEG
010714  104404                          TRAP    C$BSEG

                                        ;LOAD, READ AND CHECK CONTROL REGISTER 2 WITH AN ALTERNATING ZEROES AND
                                        ;ONES DATA PATTERN (052525)

010716  012737  052525  002330          MOV     #052525,R2LOAD          ;SETUP PATTERN TO BE LOADED
010724  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
010730  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010732                                  ERRDF   2,ADALRG,R2EROR         ;REGISTER 2 NOT EQUAL 052525
010732  104455                          TRAP    C$ERDF
010734  000002                          .WORD   2
010736  002513                          .WORD   ADALRG
010740  004770                          .WORD   R2EROR
010742                          2$:     ENDSEG
010742                          10001$:
010742  104405                          TRAP    C$ESEG
010744                                  ENDTST
010744                          L10030:
010744  104401                          TRAP    C$ETST
```

```
                        .SBTTL  TEST 7: ADAL 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

                        ;++
                        ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 7:0 USING A
                        ; BINARY COUNT PATTERN.  THE TEST PATTERN WILL START WITH A PATTERN OF 0 AND
                        ; INCREMENT TO 377 BY AN INCREMENT OF ONE.
                        ;--

010746                          BGNTST
010746                  T7::
010746  004737  005510          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

010752  005037  002330          CLR     R2LOAD                  ;SET PATTERN INITIALLY TO 0

010756                  1$:     BGNSEG
010756  104404                  TRAP    C$BSEG
010760  004737  006614          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
010764  001404                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010766                          ERRDF   2,ADALRG,R2EROR         ;REGISTER 2 NOT EQUAL EXPECTED
010766  104455                  TRAP    C$ERDF
010770  000002                  .WORD   2
010772  002513                  .WORD   ADALRG
010774  004770                  .WORD   R2EROR
010776                  2$:     ENDSEG
010776                  10000$:
010776  104405                  TRAP    C$ESEG
011000  005237  002330          INC     R2LOAD                  ;UPDATE TEST PATTERN BY ONE
011004  032737  000400  002330  BIT     #ADAL8,R2LOAD           ;CHECK IF PATTERN DONE
011012  001761                  BEQ     1$                      ;IF NOT THEN DO NEXT PATTERN
011014                          ENDTST
011014                  L10031:
011014  104401                  TRAP    C$ETST
```

```
                                        .SBTTL  TEST 8: ADAL 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

                                        ;++
                                        ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS ADAL 15:8 USING A
                                        ; BINARY COUNT PATTERN.  THE TEST PATTERN WILL START WITH A PATTERN OF 0 AND
                                        ; INCREMENT BY 400 UNTIL THE PATTERN 177400 HAS BEEN LOADED.
                                        ;--

011016                                          BGNTST
011016                                  T8::
011016  004737  005510                          JSP     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011022  005037  002330                          CLR     R2LOAD                  ;SET PATTERN INITIALLY TO 0

011026                                  1$:     BGNSEG
011026  104404                                  TRAP    C$BSEG
011030  004737  006614                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
011034  001404                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011036                                          ERRDF   2,ADALRG,R2EROR         ;REGISTER 2 NOT EQUAL EXPECTED
011036  104455                                  TRAP    C$ERDF
011040  000002                                  .WORD   2
011042  002513                                  .WORD   ADALRG
011044  004770                                  .WORD   R2EROR
011046                                  2$:     ENDSEG
011046                                  10000$:
011046  104405                                  TRAP    C$ESEG
011050  062737  000400  002330                  ADD     #ADAL8,R2LOAD           ;UPDATE TEST PATTERN BY ONE
011056  001363                                  BNE     1$                      ;IF NOT DONE THEN DO NEXT PATTERN
011060                                          ENDTST
011060                                  L10032:
011060  104401                                  TRAP    C$ETST
```

```
                                        .SBTTL  TEST 9: VDAL REGISTER R/W BIT TEST

                                        ;++
                                        ; THIS TEST WILL CHECK THAT CONTROL REGISTER 4 READ/WRITE BITS VDAL7, VDAL2,
                                        ; VDAL1 AND VDAL0 CAN BE SET AND CLEARED.  THE TEST WILL CHECK THESE BITS
                                        ; USING A DECREMENTING BINARY COUNT PATTERN.  THE READ ONLY BITS WILL BE CHECKED
                                        ; TO BE ZEROES DURING THIS TEST.  READ ONLY BITS VDAL 15:8 SHOULD BE ZERO AS A
                                        ; RESULT OF VDAL2 H BEING SET TO A ONE DURING THIS TEST.  READ ONLY BITS 6:3
                                        ; SHOULD BE A ZERO AS A RESULT OF ADAL BIT 10 BEING A ZERO.  THE ADAL REGISTER
                                        ; WAS CLEARED IN THE ABOVE ROUTINE "INITTE".
                                        ;--

011062                                          BGNTST
011062                                  T9::
011062  004737  005510                          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
011066  012737  000207  002334                  MOV     #VDAL7!VDAL2!VDAL1!VDAL0,R4LOAD  ;START ALL R/W BITS ON A ONE
011074  012701  000010                          MOV     #8.,R1                  ;SETUP TEST PATTERN COUNTER

011100                                  1$:     BGNSEG
011100  104404                                  TRAP    C$BSEG

                                        ;LOAD, READ AND CHECK VDAL REGISTER'S READ/WRITE BITS WITH A DECREASING
                                        ;BINARY COUNT PATTERN.  THE PATTERN WILL START AT 207 AND DECREASE BY
                                        ;ONE TO A PATTERN OF 200.  THE PATTERN WILL THEN BE RESET TO 7 AND
                                        ;DECREASE BY ONE UNTIL THE PATTERN OF ZERO HAS BFEN LOADED AND CHECKED.

011102  004737  006640                          JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REGISTER
011106  001404                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011110                                          ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
011110  104455                                  TRAP    C$ERDF
011112  000003                                  .WORD   3
011114  002537                                  .WORD   VDALRG
011116  005004                                  .WORD   R4EROR
011120                                  2$:     ENDSEG
011120                                  10000$:
011120  104405                                  TRAP    C$ESEG

011122  005301                                  DEC     R1                      ;CHECK IF DONE WITH LOW ORDER 3 BITS
011124  001403                                  BEQ     3$                      ;IF YES CHECK IF BIT 7 HAS BEEN CLEARED
011126  005337  002334                          DEC     R4LOAD                  ;DECREMENT TEST PATTERN BY ONE
011132  000762                                  BR      1$                      ;GO LOAD THE NEXT PATTERN
011134  105737  002334                  3$:     TSTB    R4LOAD                  ;CHECK IF BIT 7 HAS BEEN CLEARED
011140  100006                                  BPL     4$                      ;IF YES THEN TEST IS DONE
011142  012701  000010                          MOV     #8.,R1                  ;RESET PATTERN COUNTER
011146  012737  000007  002334                  MOV     #VDAL2!VDAL1!VDAL0,R4LOAD  ;SET THE LOW ORDER 3 BITS TO ONES
011154  000751                                  BR      1$                      ;REPEAT THE TEST AGAIN WITH BIT 7 A 0
011156                                  4$:     ENDTST
011156                                  L10033:
011156  104401                                  TRAP    C$ETST
```

```
                                .SBTTL  TEST 10: HDAL 15:0 REG TEST (1'S AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT HDAL REGISTER BITS 15:0 CAN BE SET TO ALL ONES
                                ; (177777) AND THEN TO ALL ZEROES (000000).  TO SELECT THE HDAL REGISTER, THE
                                ; TEST WILL SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0.  ON A WRITE
                                ; COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, PULSES WILL
                                ; OCCUR ON THE SIGNALS WPT3 LB H AND WPT3 HB H. THESE PULSES WILL CAUSE THE
                                ; DATA ON THE WRITE COMMAND TO BE LOADED INTO THE HDAL REGISTER.  ON A READ
                                ; COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, A PULSE WILL
                                ; OCCUR ON THE SIGNAL RPT3 L. THIS SIGNAL WILL CAUSE THE HDAL REGISTER TO BE
                                ; READBACK.
                                ;--

011160                                  BGNTST
011160                          T10::
011160  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011164                                  BGNSEG
011164  104404                          TRAP    C$BSEG

                                        ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
                                        ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

011166  004737  006754                  JSR     PC,SLHDAL               ;SELECT HDAL REG VID GDAL BITS 2:0

                                        ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH A DATA PATTERN OF
                                        ;ALL ONES (177777) BY ISSUING A WRITE AND READ COMMAND TO CONTROL
                                        ;REGISTER 6 WITH GDAL1 AND GDAL0 SET IN CONTROL REGISTER 0.

011172  012737  177777  002342          MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
011200  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
011204  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
011206                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 177777
011206  104455                          TRAP    C$ERDF
011210  000004                          .WORD   4
011212  002605                          .WORD   HDALRG
011214  005020                          .WORD   R06ERR
011216                          1$:     ENDSEG
011216                          10000$:
011216  104405                          TRAP    C$ESEG
```

```
3815  011220                                BGNSEG
3816  011220  104404                        TRAP    C$BSEG
3817
3818                                        ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH A DATA PATTERN OF
3819                                         ALL ZEORES (000000) BY ISSUING A WRITE AND READ COMMAND TO CONTROL
3820                                        ;REGISTER 6 WITH GDAL1 AND GDAL0 SET IN CONTROL REGISTER 0.
3821
3822  011222  005037  002342                CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
3823  011226  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
3824  011232  001404                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
3825  011234                                ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 000000
3826  011234  104455                        TRAP    C$ERDF
3827  011236  000004                        .WORD   4
3828  011240  002605                        .WORD   HDALRG
3829  011242  005020                        .WORD   R06ERR
3830  011244                        2$:     ENDSEG
3831  011244                        10001$:
3832  011244  104405                        TRAP    C$ESEG
3833  011246                                ENDTST
3834  011246                        L10034:
3835  011246  104401                        TRAP    C$ETST
3836
```

```
                                .SBTTL  TEST 11: HDAL 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT HDAL REGISTER BITS 15:0 CAN BE LOADED WITH AN
                                ; ALTERNATING ONE AND ZEROES DATA PATTERN (125252) AND AN ALTERNATING ZEROES AND
                                ; ONES DATA PATTERN (052525).  TO SELECT THE HDAL REGISTER, THE TEST WILL SET
                                ; GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0.  ON A WRITE COMMAND TO CONTROL
                                ; REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES, PULSES WILL OCCUR ON THE SIGNALS
                                ; WPT3 LB H AND WPT3 HB H.  THESE PULSES WILL CAUSE THE DATA ON A WRITE COMMAND
                                ; TO BE LOADED INTO THE HDAL REGISTER.  ON A READ COMMAND TO CONTROL REGISTER 6
                                ; WITH GDAL1 AND GDAL0 SET TO ONES, A PULSE WILL OCCUR ON THE SIGNAL RPT3 L.
                                ; THIS SIGNAL WILL CAUSE THE HDAL REGISTER TO BE READBACK.
                                ;--

011250                                  BGNTST
011250                          T11::
011250  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011254                                  BGNSEG
011254  104404                          TRAP    C$BSEG

                                ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
                                ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

011256  004737  006754                   JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH AN ALTERNATING ONES
                                ;AND ZEROES DATA PATTERN (125252) BY ISSUING A WRITE AND READ COMMAND
                                ;TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET TO ONES IN CONTROL
                                ;REGISTER 0.

011262  012737  125252  002342          MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
011270  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
011274  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
011276                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 125252
011276  104455                          TRAP    C$ERDF
011300  000004                          .WORD   4
011302  002605                          .WORD   HDALRG
011304  005020                          .WORD   R06ERR
011306                          1$:     ENDSEG
011306                          10000$:
011306  104405                          TRAP    C$ESEG
```

```
3880
3881  011310                                    BGNSEG
3882  011310  104404                            TRAP    C$BSEG
3883
3884                                            ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH AN ALTERNATING
3885                                            ;ZEROES AND ONES DATA PATTERN (052525) BY ISSUING A WRITE AND READ
3886                                            ;COMMAND TO CONTROL REGISTER 6 WITH GDAL1 AND GDAL0 SET IN CONTROL
3887                                            ;REGISTER 0.
3888
3889  011312  012737  052525  002342            MOV     #052525,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
3890  011320  004737  006672                    JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
3891  011324  001404                            BEQ     2$                      ;IF LOADED OK THEN CONTINUE
3892  011326                                    ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 052525
3893  011326  104452                            TRAP    C$ERDF
3894  011330  000004                            .WORD   4
3895  011332  002605                            .WORD   HDALRG
3896  011334  005020                            .WORD   R06ERR
3897  011336                                2$: ENDSEG
3898  011336                            10001$:
3899  011336  104405                            TRAP    C$ESEG
3900
3901  011340                                    ENDTST
3902  011340                            L10035:
3903  011340  104401                            TRAP    C$ETST
3904
```

```
                                .SBTTL  TEST 12: HDAL 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

                                ;++
                                ; THIS TEST WILL CHECK THE LOW BYTE OF THE HDAL REGISTER USING A BINARY COUNT
                                ; PATTERN.  THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE
                                ; PATTERN 377 HAS BEEN LOADED INTO THE HDAL REGISTER.  THE BITS BEING TESTED
                                ; ARE HDAL BITS 7:0.  TO SELECT THE HDAL REIGSTER, THE TEST WILL SET GDAL1 AND
                                ; GDAL0 TO ONES IN CONTROL REGISTER 0.  ON A WRITE COMMAND TO CONTROL REGISTER
                                ; 6, DATA WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND
                                ; WPT3 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM
                                ; THE HDAL REGISTER VIA THE SIGNAL RPT3 L.
                                ;--

                                        BGNTST
011342                          T12::
011342
011342  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011346  005037  002342                  CLR     R6LOAD                  ;START INITIAL PATTERN AT 0

                                1$:     BGNSEG
011352                                  TRAP    C$BSEG
011352  104404

                                        ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
                                        ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

011354  004737  006754                JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0

                                        ;LOAD, READ ADN CHECK HDAL REGISTER BITS 7:0 WITH A BINARY COUNT PATTERN
                                        ;THE HIGH BYTE OF THE HDAL REGISTER WILL BE CHECKED TO CONTAIN ZEROES
                                        ;DURING THIS TEST.

011360  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK THE HDAL REG
011364  001404                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011366                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REG NOT EQUAL EXPECTED
011366  104455                        TRAP    C$ERDF
011370  000004                        .WORD   4
011372  002605                        .WORD   HDALRG
011374  005020                        .WORD   R06ERR
011376                          2$:     ENDSEG
011376                          10000$:
011376  104405                        TRAP    C$ESEG
011400  005237  002342                INC     R6LOAD                  ;UPDATE TEST PATTERN BY ONE
011404  032737  000400  002342        BIT     #HDAL8,R6LOAD           ;CHECK IF TEST PATTERN DONE
011412  001757                        BEQ     1$                      ;IF NOT THEN LOAD NEXT PATTERN
011414                                  ENDTST
011414                          L10036:
011414  104401                        TRAP    C$ETST
```

```
                        .SBTTL  TEST 13: HDAL 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

                        ;++
                        ; THIS TEST WILL CHECK THE HIGH BYTE OF THE HDAL REGISTER USING A BINARY COUNT
                        ; PATTERN.  THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE
                        ; PATTERN 177400 HAS BEEN LOADED INTO THE HDAL REGISTER.  THE BITS BEING TESTED
                        ; ARE HDAL BITS 15:8.  TO SELECT THE HDAL REIGSTER, THE TEST WILL SET GDAL1 AND
                        ; GDAL0 TO ONES IN CONTROL REGISTER 0.  ON A WRITE COMMAND TO CONTROL REGISTER
                        ; 6, DATA WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND
                        ; WPT3 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM
                        ; THE HDAL REGISTER VIA THE SIGNAL RPT3 L.
                        ;--

011416                          BGNTST
011416                  T13::
011416  004737  005510          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011422  005037  002342          CLR     R6LOAD                  ;START INITIAL PATTERN AT 0

011426                  1$:     BGNSEG
011426  104404                  TRAP    C$BSEG

                                ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
                                ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

011430  004737  006754          JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH A BINARY COUNT PATTERN
                                ;THE LOW BYTE OF THE HDAL REGISTER WILL BE CHECKED TO CONTAIN ZEROES
                                ;DURING THIS TEST.

011434  004737  006672          JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK THE HDAL REG
011440  001404                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011442                          ERRDF   4,HDALRG,R06ERR         ;HDAL REG NOT EQUAL EXPECTED
011442  104455                  TRAP    C$ERDF
011444  000004                  .WORD   4
011446  002605.                 .WORD   HDALRG
011450  005020                  .WORD   R06ERR
011452                  2$:     ENDSEG
011452                  10000$:
011452  104405                  TRAP    C$ESEG
011454  062737  000400  002342  ADD     #HDAL8,R6LOAD           ;UPDATE THE HIGH BYTE BY ONE
011462  001361                  BNE     1$                      ;IF PATTERN NOT DONE LOAD NEXT WORD
011464                          ENDTST
011464                  L10037:
011464  104401                  TRAP    C$ETST
```

```
                                .SBTTL  TEST 14: MODE REG 15:0 REG TEST (1'S AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT MODE REGISTER BITS 15:0 CAN BE SET TO ALL ONES
                                ; (177777) AND THEN TO ALL ZEROES (000000).  TO SELECT THE MODE REGISTER, THE
                                ; TEST WILL SET GDAL2 TO A ONE IN CONTROL REGISTER 0.  ON A WRITE COMMAND TO
                                ; CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE, PULSES WILL BE OCCUR ON THE
                                ; SIGNALS WPT4 LB H AND WPT4 HB H.  THESE PULSE WILL CAUSE THE DATA ON THE
                                ; WRITE COMMAND TO BE LOADED INTO THE MODE REGISTER.  ON A READ COMMAND TO
                                ; CONTROL REGISTER 6 WITH GDAL2 SET IN CONTROL REGISTER 0, A PULSE WILL OCCUR
                                ; ON THE SIGNAL RPT4 L.  THIS SIGNAL WILL CAUSE THE MODE REGISTER TO BE READBACK
                                ;--

011466                                  BGNTST
011466                          T14::
011466  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011472                                  BGNSEG
011472  104404                          TRAP    C$BSEG

                                        ;SET GDAL2 TO A ONE IN CONTROL REGISTER 0 TO SELECT THE MODE REGISTER
                                        ;WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

011474  004737  007006                JSR     PC,SLMODR               ;GO SELECT MODE REG VIA GDAL BITS 2:0

                                        ;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH A DATA PATTERN OF
                                        ;ALL ONES (177777) BY ISSUING A WRITE AND READ COMMAND TO CONTROL
                                        ;REGISTER 6 WITH GDAL2 SET IN CONTROL REGISTER 0.

011500  012737  177777  002342          MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
011506  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
011512  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
011514                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL 177777
011514  104455                          TRAP    C$ERDF
011516  000004                          .WORD   4
011520  002631                          .WORD   MODREG
011522  005020                          .WORD   R06ERR
011524                          1$:     ENDSEG
011524                          10000$:
011524  104405                          TRAP    C$ESEG
```

```
4041
4042  011526                                    BGNSEG
4043  011526  104404                            TRAP    C$BSEG
4044
4045                                            ;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH A DATA PATTERN OF
4046                                            ;ALL ZEORES (000000) BY ISSUING A WRITE AND READ COMMAND TO CONTROL
4047                                            ;REGISTER 6 WITH GDAL2 SET IN CONTROL REGISTER 0.
4048
4049  011530  005037  002342                    CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
4050  011534  004737  006672                    JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
4051  011540  001404                            BEQ     2$                      ;IF LOADED OK THEN CONTINUE
4052  011542                                    ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL 000000
4053  011542  104455                            TRAP    C$ERDF
4054  011544  000004                            .WORD   4
4055  011546  002631                            .WORD   MODREG
4056  011550  005020                            .WORD   R06ERR
4057  011552                            2$:     ENDSEG
4058  011552                            10001$:
4059  011552  104405                            TRAP    C$ESEG
4060
4061  011554                                    ENDTST
4062  011554                            L10040:
4063  011554  104401                            TRAP    C$ETST
4064
```

```
                                .SBTTL  TEST 15: MODE REG 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT MODE REGISTER BITS 15:0 CAN BE LOADED WITH AN
                                ; ALTERNATING ONE AND ZEROES DATA PATTERN (125252) AND AN ALTERNATING ZEROES AND
                                ; ONES DATA PATTERN (052525).  TO SELECT THE MODE REGISTER, THE TEST WILL SET
                                ; GDAL2 IN THE LOW BYTE OF CONTROL REGISTER 0.   ON A WRITE COMMAND TO CONTROL
                                ; REGISTER 6 WITH GDAL2 SET TO A ONE IN REG 0, PULSES WILL OCCUR ON THE SIGNALS
                                ; WPT4 LB H AND WPT4 HB H.  THESE PULSES WILL CAUSE THE DATA ON A WRITE COMMAND
                                ; TO BE LOADED INTO THE MODE REGISTER.  ON A READ COMMAND TO CONTROL REGISTER 6
                                ; WITH GDAL2 SET TO A ONE, A PULSE WILL OCCUR ON THE SIGNAL RPT4 L.  THIS SIGNAL
                                ; WILL CAUSE THE MODE REGISTER TO BE READBACK.
                                ;--

011556                                  BGNTST
011556                          T15::
011556  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011562                                  BGNSEG
011562  104404                          TRAP    C$BSEG

                                ;SET GDAL2 TO A ONE IN THE LOW BYTE OF CONTROL REGISTER 0 TO SELECT THE
                                ;MODE REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REG 6.

011564  004737  007006                  JSR     PC,SLMODR               ;GO SELECT MODE REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH AN ALTERNATING ONES
                                ;AND ZEROES DATA PATTERN (125252) BY ISSUING A WRITE AND READ COMMAND
                                ;TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE IN CONTROL REGISTER 0.

011570  012737  125252  002342          MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
011576  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
011602  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
011604                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL 125252
011604  104455                          TRAP    C$ERDF
011606  000004                          .WORD   4
011610  002631                          .WORD   MODREG
011612  005020                          .WORD   R06ERR
011614                          1$:     ENDSEG
011614                          10000$:
011614  104405                          TRAP    C$ESEG
```

```
4107
4108  011616                                    BGNSEG
4109  011616  104404                            TRAP    C$BSEG
4110
4111                                            ;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH AN ALTERNATING
4112                                            ;ZEROES AND ONES DATA PATTERN (052525) BY ISSUING A WRITE AND READ
4113                                            ;COMMAND TO CONTROL REGISTER 6 WITH GDAL2 SET TO A ONE IN CONTROL REG 0.
4114
4115  011620  012737  052525  002342              MOV     #052525,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
4116  011626  004737  006672                      JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
4117  011632  001404                              BEQ     2$                      ;IF LOADED OK THEN CONTINUE
4118  011634                                      ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL 052525
4119  011634  104455                              TRAP    C$ERDF
4120  011636  000004                              .WORD   4
4121  011640  002631                              .WORD   MODREG
4122  011642  005020                              .WORD   R06ERR
4123  011644                            2$:       ENDSEG
4124  011644                            10001$:
4125  011644  104405                              TRAP    C$ESEG
4126
4127  011646                                      ENDTST
4128  011646                            L10041:
4129  011646  104401                              TRAP    C$ETST
4130
```

```
                        .SBTTL  TEST 16: MODE REG 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

                        ;++
                        ; THIS TEST WILL CHECK THE LOW BYTE OF THE MODE REGISTER USING A BINARY COUNT
                        ; PATTERN.  THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE UNTIL THE
                        ; PATTERN 377 HAS BEEN LOADED INTO THE MODE REGISTER.  THE BITS BEING TESTED
                        ; ARE MR BITS 7:0.  TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 TO A 1
                        ; IN LOW BYTE OF CONTROL REGISTER 0.  ON A WRITE COMMAND TO CONTROL REGISTER
                        ; 6, DATA WILL BE LOADED INTO THE MODE REGISTER VIA THE SIGNALS WPT4 LB H AND
                        ; WPT4 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM
                        ; THE MODE REGISTER VIA THE SIGNAL RPT4 L.
                        ;--

011650                          BGNTST
011650                  T16::
011650  004737  005510          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011654  005037  002342          CLR     R6LOAD                  ;START INITIAL PATTERN AT 0

011660                  1$:     BGNSEG
01166'  104404                  TRAP    C$BSEG

                                ;SET GDAL2 TO A ONE IN THE LOW BYTE OF CONTROL REGISTER 0 TO SELECT THE
                                ;MODE REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REG 6.

011662  004737  007006          JSR     PC,SLMODR               ;GO SELECT MODE REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK MODE REGISTER BITS 7:0 WITH A BINARY COUNT PATTERN
                                ;THE HIGH BYTE OF THE MODE REGISTER WILL BE CHECKED TO CONTAIN ZEROES
                                ;DURING THIS TEST.

011666  004737  0066'2          JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK THE MODE REG
011672  001404                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011674                          ERRDF   4,MODREG,R06ERR         ;MODE REG NOT EQUAL EXPECTED
011674  104455                  TRAP    C$ERDF
011676  000004                  .WORD   4
011700  002631                  .WORD   MODREG
011702  005020                  .WORD   R06ERR
011704                  2$:     ENDSEG
011704                  10000$:
011704  104405                  TRAP    C$ESEG
011706  005237  002342          INC     R6LOAD                  ;UPDATE TEST PATTERN BY ONE
011712  032737  000400  002342  BIT     #MR8,R6LOAD             ;CHECK IF TEST PATTERN DONE
011720  001757                  BEQ     1$                      ;IF NOT THEN LOAD NEXT PATTERN
011722                          ENDTST
011722                  L10042:
011722  104401                  TRAP    C$ETST
```

```
                                        .SBTTL  TEST 17: MODE REG 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

                                        ;++
                                        ; THIS TEST WILL CHECK THE HIGH BYTE OF THE MODE REGISTER USING A BINARY COUNT
                                        ; PATTERN.  THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400 UNTIL THE
                                        ; PATTERN 177400 HAS BEEN LOADED INTO THE MODE REGISTER.  THE BITS BEING TESTED
                                        ; ARE MR BITS 15:8.  TO SELECT THE MODE REGISTER, THE TEST WILL SET GDAL2 TO A 1
                                        ; IN LOW BYTE OF CONTROL REGISTER 0.  ON A WRITE COMMAND TO CONTROL REGISTER
                                        ; 6, DATA WILL BE LOADED INTO THE MODE REGISTER VIA THE SIGNALS WPT4 LB H AND
                                        ; WPT4 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM
                                        ; THE MODE REGISTER VIA THE SIGNAL RPT4 L.
                                        ;--

011724                                          BGNTST
011724                                  T17::
011724  004737  005510                          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

011730  005037  002342                          CLR     R6LOAD                  ;START INITIAL PATTERN AT 0

011734                                  1$:     BGNSEG
011734  104404                                  TRAP    C$BSEG

                                                ;SET GDAL2 TO A ONE IN THE LOW BYTE OF CONTROL REGISTER 0 TO SELECT THE
                                                ;MODE REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REG 6.

011736  004737  007006                          JSR     PC,SLMODR               ;GO SELECT MODE REG VIA GDAL BITS 2:0

                                                ;LOAD, READ AND CHECK MODE REGISTER BITS 15:8 WITH BINARY COUNT PATTERN
                                                ;THE LOW BYTE OF THE MODE REGISTER WILL BE CHECKED TO CONTAIN ZEROES
                                                ;DURING THIS TEST.

011742  004737  006672                          JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK THE MODE REG
011746  001404                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011750                                          ERRDF   4,MODREG,R06ERR         ;MODE REG NOT EQUAL EXPECTED
011750  104455                                  TRAP    C$ERDF
011752  000004                                  .WORD   4
011754  002631                                  .WORD   MODREG
011756  005020                                  .WORD   R06ERR
011760                                  2$:     ENDSEG
011760                                  10000$:
011760  104405                                  TRAP    C$ESEG
011762  062737  000400  002342                  ADD     #MR8,R6LOAD             ;UPDATE THE HIGH BYTE BY 1
011770  001361                                  BNE     1$                      ;IF PATTERN NOT DONE THEN LOAD NEXT
011772                                          ENDTST
011772                                  L10043:
011772  104401                                  TRAP    C$ETST
```

```
                                .SBTTL  TEST 18: FDAL 7:0 REG TEST (1'S AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT FDAL REGISTER BITS 7:0 CAN BE SET TO ALL ONES (377)
                                ; AND THEN TO ALL ZEROES (000).  TO SELECT THE FDAL REGISTER, THE TEST WILL SET
                                ; GDAL1 TO A ONE IN CONTROL REGISTER 0.  ON A WRITE COMMAND TO CONTROL REGISTER
                                ; 6, DATA WILL BE LOADED INTO FDAL REGISTER BITS 7:0 VIA THE SIGNAL WPT2 LB H.
                                ; ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE FDAL
                                ; REGISTER VIA THE SIGNAL RPT2 L.  THE HIGH BYTE, WHICH IS ANOTHER REGISTER,
                                ; WILL BE IGNORED DURING THIS TEST.
                                ;--

011774                                  BGNTST
011774                          T18::
011774  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

012000                                  BGNSEG
012000  104404                          TRAP    C$BSEG

                                ;SET GDAL1 IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER WHEN A
                                ;WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

012002  004737  007154                  JSR     PC,SLFDAL               ;GE SELECT FDAL REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH A DATA PATTERN OF ALL
                                ;ONES (377) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
                                ;WITH GDAL1 SET TO A ONE IN CONTROL REGISTER 0.

012006  012737  177400  002346          MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE
012014  012737  000377  002342          MOV     #377,R6LOAD             ;SETUP DATA TO BE LOADED
012022  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK FDAL REG
012026  001404                          BEQ     1$                      ;IF DATA LOADED OK THEN CONTINUE
012030                                  ERRDF   4,FDALRG,R06ERR         ;FDAL REGISTER NOT EQUAL TO 377
012030  104455                          TRAP    C$ERDF
012032  000004                          .WORD   4
012034  002653                          .WORD   FDALRG
012036  005020                          .WORD   R06ERR
012040                          1$:     ENDSEG
012040                          10000$:
012040  104405                          TRAP    C$ESEG
```

```
                                        BGNSEG
012042                                  TRAP    C$BSEG

                                        ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH A DATA PATTERN OF ALL
                                        ;ZEROES (000) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
                                        ;WITH GDAL1 SET TO A ONE IN CONTROL REGISTER C.

012044  005037  002342                  CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
012050  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK FDAL REG
012054  001404                          BEQ     2$                      ;IF DATA LOADED OK THEN CONTINUE
012056                                  ERRDF   4,FDALRG,R06ERR         ;FDAL REGISTER NOT EQUAL TO 000
012056  104455                          TRAP    C$ERDF
012060  000004                          .WORD   4
012062  002653                          .WORD   FDALRG
012064  005020                          .WORD   R06ERR
012066                          2$:     ENDSEG
012066                          10001$:
012066  104405                          TRAP    C$ESEG

                                        ENDTST
012070                          L10044:
012070  104401                          TRAP    C$ETST
```

```
                                        .SBTTL  TEST 19: FDAL 7:0 REG TEST (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK THAT FDAL REGISTER BITS 7:0 CAN BE LOADED WITH AN ALTER-
                                        ; NATING ONES AND ZEROES DATA PATTERN (252) AND AN ALTERNATING ZEROES AND ONES
                                        ; DATA PATTERN (125).  TO SELECT THE FDAL REGISTER, THE TEST WILL SET THE SIGNAL
                                        ; GDAL1 TO A ONE IN CONTROL REGISTER 0.  ON A WRITE COMMAND TO CONTROL REGISTER
                                        ; 6, DATA WILL BE LOADED INTO FDAL REGISTER BITS 7:0 VIA THE SIGNAL WPT2 LB H.
                                        ; ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE FDAL
                                        ; REGISTER VIA THE SIGNAL RPT2 L.  THE HIGH BYTE, WHICH IS ANOTHER REGISTER,
                                        ; WILL BE IGNORED DURING THIS TEST.
                                        ;--

012072                                          BGNTST
012072                                  119::
012072  004737  0055'0,                         JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

012076                                          BGNSEG
012076  104404                                  TRAP    C$BSEG

                                        ;SET GDAL1 IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER WHEN A
                                        ;WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

012100  004737  007154                         JSR     PC,SLFDAL               ;GO SELECT FDAL REG VIA GDAL BITS 2:0

                                        ;LOAD, READ AND CHECK FDAL REGISTER BITS 7 0 WITH AN ALTERNATING ONES
                                        ;AND ZEROES DATA PATTERN (252) BY ISSUING A WRITE AND READ COMMAND TO
                                        ;CONTROL REGISTER 6 WITH GDAL' SET TO A ONE IN CONTROL REGISTER 0.

012104  012737  177400  002346                MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE
012112  012737  000252  002342                MOV     #252,R6LOAD             ;SETUP DATA TO BE LOADED
012120  004737  006672                        JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK FDAL REG
012124  001404                                BEQ     1$                      ;IF DATA LOADED OK THEN CONTINUE
012126                                        ERRDF   4,FDALRG,R06ERR         ;FDAL REGISTER NOT EQUAL TO 252
012126  104455                                TRAP    C$ERDF
012130  000004                                .WORD   4
012132  002653                                .WORD   FDALRG
012134  005020                                .WORD   R06ERR
012136                                  1$:     ENDSEG
012136                                  10000$:
012136  104405                                TRAP    C$ESEG
```

```
4333
4334  012140                                    BGNSEG
4335  012140  104404                            TRAP    C$BSEG
4336
4337                                            ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH AN ALTERNATING ZEROES
4338                                            ;AND ONES DATA PATTERN (125) BY ISSUING A WRITE AND READ COMMAND TO
4339                                            ;CONTROL REGISTER 6 WITH GDAL1 SET TO A ONE IN CONTROL REGISTER 0.
4340
4341  012142  012737  000125  002342            MOV     #125,R6LOAD             ;SETUP DATA TO BE LOADED
4342  012150  004737  006672                    JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK FDAL REG
4343  012154  001404                            BEQ     2$                      ;IF DATA LOADED OK THEN CONTINUE
4344  012156                                    ERRDF   4,FDALRG,R06ERR         ;FDAL REGISTER NOT EQUAL TO 125
4345  012156  104455                            TRAP    C$ERDF
4346  012160  000004                            .WORD   4
4347  012162  002653                            .WORD   FDALRG
4348  012164  005020                            .WORD   R06ERR
4349  012166                            2$:     ENDSEG
4350  012166                            10001$:
4351  012166  104405                            TRAP    C$ESEG
4352
4353  012170                                    ENDTST
4354  012170                            L10045:
4355  012170  104401                            TRAP    C$E
4356
```

```
                                        .SBTTL  TEST 20: FDAL 7:0 REG TEST USING BINARY COUNT

                                        ;++
                                        ; THIS TEST WILL CHECK FDAL REGISTER BITS 7:0 USING A BINARY COUNT PATTERN. THE
                                        ; TEST PATTERN WILL START AT 0 AND INCREMENT BY ONE UNTIL THE PATTERN 377 HAS
                                        ; BEEN LOADED INTO THE FDAL REGISTER.  TO SELECT THE FDAL REGISTER, THE TEST
                                        ; WILL SET GDAL1 TO A ONE IN CONTROL REGISTER 0.  ON A WRITE COMMANND TO CONTROL
                                        ; REGISTER 6, DATA WILL BE LOADED INTO THE FDAL REG VIA THE SIGNAL WPT2 LB H.
                                        ; ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ FROM THE FDAL REG
                                        ; VIA THE SIGNAL RPT2 L.
                                        ;--

                                                BGNTST
012172                                  T20::
012172                                          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
012172  004737  005510                          CLR     R6LOAD                  ;SET STARTING PATTERN TO ZERO
012176  005037  002342                          MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE ON READ
012202  012737  177400  002346
                                        1$:     BGNSEG
012210                                          TRAP    C$BSEG
012210  104404
                                                ;SET GDAL1 TO A ONE IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER
                                                ;WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.

012212  004737  007154                         JSR     PC,SLFDAL               ;GO SELECT FDAL REG VIA GDAL BITS 2:0

                                                ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH A BINARY COUNT PATTERN
                                                ;FROM 0 TO 377 BY AN INCREMENT OF ONE.

012216  004737  006672                         JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK FDAL REG
012222  001404                                 BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012224                                          ERRDF   4,FDALRG,R06ERR         ;FDAL REG NOT EQUAL EXPECTED (0-377)
012224  104455                                  TRAP    C$ERDF
012226  000004                                  .WORD   4
012230  002653                                  .WORD   FDALRG
012232  005020                                  .WORD   R06ERR
012234                                  2$:     ENDSEG
012234                                  10000$:
012234  104405                                  TRAP    C$ESEG
012236  105237  002342                          INCB    R6LOAD                  ;UPDATE TEST PATTERN BY ONE
012242  001362                                  BNE     1$                      ;IF NOT 0 THEN LOAD NEXT PATTERN
012244                                          ENDTST
012244                                  L10046:
012244  104401                                  TRAP    C$ETST
```

```
                                .SBTTL  TEST 21: EOAI 7:0 REG TEST USING BINARY COUNT

                                ;++
                                ; THIS TEST WILL CHECK EOAI REGISTER BITS 7:0 USING A BINARY COUNT PATTERN.  THE
                                ; TEST PATTERN WILL START WITH ZERO AND INCREMENT BY ONE UNTIL A PATTERN OF ALL
                                ; ONES HAS BEEN LOADED INTO THE EOAI REGISTER AND CHECKED.  THE EOAI REGISTER IS
                                ; THE HIGH BYTE OF THE FDAL REGISTER.  DATA IS LOADED INTO THE EOAI REGISTER VIA
                                ; THE SIGNAL WPT2 HB H WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                ; THE FDAL REGISTER IS SELECTED VIA GDAL BITS 2:0.  TO READ THE EOAI BUS, THE
                                ; PROGRAM WILL SET FDAL0 H TO A ONE TO SELECT THE EOAI BUS TO BE READ INSTEAD OF
                                ; THE CTL BUS.  THE EOAI BUS IS READ BACK TO THE LSI-11 VIA THE SIGNAL RAT2 L
                                ; WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE FDAL REGISTER IS
                                ; SELECTED.
                                ;--

012246                                  BGNTST
012246                          T21::
012246  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
012252  012737  000001  002342          MOV     #FDAL0,R6LOAD           ;SETUP EOAI FDAI ENABLES + DATA PATTERN

012260                          1$:     BGNSEG
012260  104404                          TRAP    C$BSEG

                                        ;SELECT FDAL REGISTER BY SETTING GDAL1 H TO A ONE AND GDAL BITS 2 AND 0
                                        ;TO ZEORES IN CONTROL REGISTER 0.

012262  004737  007154                  JSR     PC,SLFDAL               ,SELECT FDAL AND EOAI REG VIA GDAL 2:0

                                        ;LOAD, READ AND CHECK EOAI REGIS.ER BITS 7:0 WITH THE BINARY COUNT DATA
                                        ;PATTERN.  THE EOAI REGISTER IS THE HIGH BYTE OF THE FDAL REGISTER.  THE
                                        ;DATA PATTERN WILL BE LOADED VIA THE SIGNAL WPT2 HB H WHEN A WRITE
                                        ;COMMAND IS ISSUED TO CONTROL REGISTER 6.  FDAL  REGISTER BIT 0 WILL ALSO
                                        ;BE WRITTEN INTO THE FDAL REGISTER ON THE WRITE COMMAND TO CONTROL
                                        ;REGISTER 6. THE EOAI REGISTER WILL BE READBACK VIA THE SIGNAL RAT2 L WHEN
                                        ;A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL FDAL0 H IS
                                        ;SET TO A ONE.  THE SIGNAL FDAL0 H ON A ONE WILL CAUSE THE EOAI BUS TO BE
                                        ;READBACK ON THE READ COMMAND INSTEAD OF THE CTL 7:0 BUS.

012266  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK FDAL + EOAI
012272  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012274                                  ERRDF   4,EOAIFD,R06ERR         ;EOAI REG OR FDAL REG ERROR
012274  104455                          TRAP    C$ERDF
012276  000004                          .WORD   4
012300  002676                          .WORD   EOAIFD
012302  005020                          .WORD   R06ERR
012304                          2$:     ENDSEG
012304                          10000$:
012304  104405                          TRAP    C$ESEG

012306  062737  000400  002342          ADD     #BIT8,R6LOAD            ;UPDATE EOAI PATTERN BY ONE
012314  103361                          BCC     1$                      ;IF NOT DONE LOAD NEXT PATTERN
012316                                  ENDTST
012316                          L10047:
012316  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 22: DIAG ADDR 15:0 REG TEST (1'S AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT THE DIAGNOSTIC ADDRESS REGISTER BITS ADDR 15:0 CAN
                                ; BE LOADED WITH ALL ONES (177777) AND THEN ALL ZEROES (000000).
                                ;
                                ; TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS
                                ; BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H
                                ; IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL
                                ; SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0.  ON A WRITE OR READ COMMAND
                                ; TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS
                                ; WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L.  TO SELECT THE DIAG-
                                ; NOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER
                                ; 0.  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA
                                ; WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H
                                ; AND WPT0 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR
                                ; ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAG-
                                ; NOSTIC ADDRESS REGISTER.
                                ;--

012320                                  BGNTST
012320                          T22::
012320  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

012324                                  BGNSEG
012324  104404                          TRAP    C$BSEG

                                ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
                                ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

012326  004737  006754                JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH HDAL9 H SET TO A ONE.
                                ;ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE
                                ;THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H.  ON A READ
                                ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REG-
                                ;ISTER VIA THE SIGNAL RPT3 L.

012332  012737  001000  002342        MOV     #HDAL9,R6LOAD           ;SETUP DATA TO BE LOADED
012340  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REG
012344  001405                        BEQ     1$                      ;IF DATA LOADED OK THEN CONTINUE
012346                                ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 1000
012346  104455                        TRAP    C$ERDF
012350  000004                        .WORD   4
012352  002605                        .WORD   HDALRG
012354  005020                        .WORD   R06ERR
012356                                CKLOOP
012356  104406                        TRAP    C$CLP1

                                ;CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0 TO SELECT THE DIAGNOSTIC
                                ;ADDRESS REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

012360  004737  007072        1$:     JSR     PC,SLDADR               ;SELECT DIAG ADDRESS REG VIA GDAL 2:0

                                ;LOAD, READ AND CHECK DIAGNOSTIC ADDRESS REGISTER BITS 15:0 WITH A
                                ;DATA PATTERN OF 177777.  ON A WRITE COMMAND TO CONTROL REGISTER 6
```

```
4513                                                ;WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC
4514                                                ;ADDRESS REGISTER VIA THE SIGNALS WPTO LB H AND WPTO HB H.  ON A READ
4515                                                ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAG-
4516                                                ;NOSTIC ADDRESS REGISTER VIA THE SIGNAL RPTO L.  PREVIOUSLY IN THIS
4517                                                ;TEST, HDAL9 WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER
4518                                                ;BITS ONTO THE ADDRESS BUS.
4519
4520  012364  012737  177777  002342                MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
4521  012372  004737  006672                        JSR     PC,LDRDR6               ;LOAD READ AND CHECK DIAG ADDRESS REG
4522  012376  001404                                BEQ     2$                      ;IF LOADED OK THEN CONTINUE
4523  012400                                        ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDR REG NOT EQUAL 177777
4524  012400  104455                                TRAP    C$ERDF
4525  012402  000004                                .WORD   4
4526  012404  002735                                .WORD   ADDRRG
4527  012406  005020                                .WORD   R06ERR
4528  012410                                2$:     ENDSEG
4529  012410                                10000$:
4530  012410  104405                                TRAP    C$ESEG
4531
4532  012412                                        BGNSEG
4533  012412  104404                                TRAP    C$BSEG
4534
4535                                                ;LOAD, READ AND CHECK DAIGNOSTIC ADDRESS REGISTER BITS 15:0 WITH A DATA
4536                                                ;PATTERN OF 000000.  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL
4537                                                ;BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC ADDRESS
4538                                                ;REGISTER VIA THE SIGNALS WPTO LB H AND WPTO HB H.  ON A READ COMMAND
4539                                                ;TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAGNOSTIC
4540                                                ;ADDRESS REGISTER VIA THE SIGNAL RPTO L.  PREVIOUSLY IN THIS TEST, HDAL9
4541                                                ;WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER ONTO THE
4542                                                ;ADDRESS BUS
4543
4544  012414  005037  002342                        CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
4545  012420  004737  006672                        JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK ADDRESS REG
4546  012424  001404                                BEQ     3$                      ;IF DATA LOADED OK THEN CONTINUE
4547  012426                                        ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDR REG NOT EQUAL 000000
4548  012426  104455                                TRAP    C$ERDF
4549  012430  000004                                .WORD   4
4550  012432  002735                                .WORD   ADDRRG
4551  012434  005020                                .WORD   R06ERR
4552  012436                                3$:     ENDSEG
4553  012436                                10001$:
4554  012436  104405                                TRAP    C$ESEG
4555  012440                                        ENDTST
4556  012440                                L10050:
4557  012440  104401                                TRAP    C$ETST
4558
```

```
                                .SBTTL  TEST 23: DIAG ADDR 15:0 REG TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT THE DAIGNOSTIC ADDRESS REGISTER BITS ADDR 15:0 CAN
                                ; BE LOADED WITH AN ALTERNATING ONES AND ZEROES DATA PATERRN (125252) AND AN
                                ; ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
                                ;
                                ; TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS
                                ; BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H
                                ; IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL
                                ; SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0.  ON A WRITE OR READ COMMAND
                                ; TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS
                                ; WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L.  TO SELECT THE DIAG-
                                ; NOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER
                                ; 0.  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA
                                ; WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H
                                ; AND WPT0 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR
                                ; ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAG-
                                ; NOSTIC ADDRESS REGISTER.
                                ;--

012442                                  BGNTST
012442                          T23::
012442  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

012446                                  BGNSEG
012446  104404                          TRAP    C$BSEG

                                ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
                                ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

012450  004737  006754                   JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH HDAL9 H SET TO A ONE.
                                ;ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE
                                ;THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H.  ON A READ
                                ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REG-
                                ;ISTER VIA THE SIGNAL RPT3 L.

012454  012737  001000  002342          MOV     #HDAL9,R6LOAD           ;SETUP DATA TO BE LOADED
012462  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REG
012466  001405                          BEQ     1$                      ;IF DATA LOADED OK THEN CONTINUE
012470                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 1000
012470  104455                          TRAP    C$ERDF
012472  000004                          .WORD   4
012474  002605                          .WORD   HDALRG
012476  005020                          .WORD   R06ERR
012500                                  CKLOOP
012500  104406                          TRAP    C$CLP1

                                ;CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0 TO SELECT THE DIAGNOSTIC
                                ;ADDRESS REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

012502  004737  007072          1$:     JSR     PC,SLDADR               ;SELECT DIAG ADDRESS REG VIA GDAL 2:0

                                ;LOAD, READ AND CHECK DIAGNOSTIC ADDRESS REGISTER BITS 15:0 WITH A
```

```
                                                ;DATA PATTERN OF 125252.  ON A WRITE COMMAND TO CONTROL REGISTER 6
                                                ;WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC
                                                ;ADDRESS REGISTER VIA THE SIGNALS WPTO LB H AND WPTO HB H.  ON A READ
                                                ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAG-
                                                ;NOSTIC ADDRESS REGISTER VIA THE SIGNAL RPTO L.  PREVIOUSLY IN THIS
                                                ;TEST, HDAL9 WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER
                                                ;BITS ONTO THE ADDRESS BUS.

012506  012737  125252  002342          MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
012514  004737  006672                  JSR     PC,LDRDR6               ;LOAD READ AND CHECK DIAG ADDRESS REG
012520  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012522                                  ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDR REG NOT EQUAL 125252
012522  104455                          TRAP    C$ERDF
012524  000004                          .WORD   4
012526  002735                          .WORD   ADDRRG
012530  005020                          .WORD   R06ERR
012532                          2$:     ENDSEG
012532                          10000$:
012532  104405                          TRAP    C$ESEG

012534                                  BGNSEG
012534  104404                          TRAP    C$BSEG

                                                ;LOAD, READ AND CHECK DAIGNOSTIC ADDRESS REGISTER BITS 15:0 WITH A DATA
                                                ;PATTERN OF 052525.  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL
                                                ;BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC ADDRESS
                                                ;REGISTER VIA THE SIGNALS WPTO LB H AND WPTO HB H.  ON A READ COMMAND
                                                ;TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAGNOSTIC
                                                ;ADDRESS REGISTER VIA THE SIGNAL RPTO L.  PREVIOUSLY IN THIS TEST, HDAL9
                                                ;WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER ONTO THE
                                                ;ADDRESS BUS

012536  012737  052525  002342          MOV     #052525,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
012544  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK ADDRESS REG
012550  001404                          BEQ     3$                      ;IF DATA LOADED OK THEN CONTINUE
012552                                  ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDR REG NOT EQUAL 052525
012552  104455                          TRAP    C$ERDF
012554  000004                          .WORD   4
012556  002735                          .WORD   ADDRRG
012560  005020                          .WORD   R06ERR
012562                          3$:     ENDSEG
012562                          10001$:
012562  104405                          TRAP    C$ESEG
012564                                  ENDTST
012564                          L10051:
012564  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 24: DIAG ADDR 15:0 REG TEST (LOW BYTE) USING BINARY COUNT

                                ;++
                                ; THIS TEST WILL CHECK THE LOW BYTE OF THE DIAGNOSTIC ADDRESS REGISTER USING A
                                ; BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY ONE
                                ; UNTIL THE PATTERN 377 HAS BEEN LOADED INTO DIAGNOSTIC ADDRESS REGISTER BITS
                                ; ADDR 7:0.  THE HIGH BYTE OF THE DIAGNOSTIC ADDRESS REGISTER WILL BE LOADED
                                ; WITH ZEROES DURING THIS TEST.
                                ;
                                ; TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS
                                ; BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H
                                ; IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL
                                ; SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0.  ON A WRITE OR READ COMMAND
                                ; TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS
                                ; WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L.  TO SELECT THE DIAG-
                                ; NOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER
                                ; 0.  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA
                                ; WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H
                                ; AND WPT0 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR
                                ; ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAG-
                                ; NOSTIC ADDRESS REGISTER.
                                ;--

012566                                  BGNTST
012566                          T24::
012566  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
012572  005001                          CLR     R1                      ;SET DATA PATTERN INITIALLY TO 0

012574                          1$:     BGNSEG
012574  104404                          TRAP    C$BSEG

                                ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
                                ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

012576  004737  006754                  JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH HDAL9 H SET TO A ONE.
                                ;ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE
                                ;THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H.  ON A READ
                                ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REG-
                                ;ISTER VIA THE SIGNAL RPT3 L.

012602  012737  001000  002342          MOV     #HDAL9,R6LOAD           ;SETUP DATA TO BE LOADED
012610  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REG
012614  001405                          BEQ     2$                      ;IF DATA LOADED OK THEN CONTINUE
012616                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 1000
012616  104455                          TRAP    C$ERDF
012620  000004                          .WORD   4
012622  002605                          .WORD   HDALRG
012624  005020                          .WORD   R06ERR
012626                                  CKLOOP
012626  104406                          TRAP    C$CLP1
```

```
4715
4716                                    ;CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0 TO SELECT THE DIAGNOSTIC
4717                                    ;ADDRESS REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.
4718
4719  012630  004737  007072      2$:   JSR     PC,SLDADR               ;SELECT DIAG ADDRESS REG VIA GDAL 2:0
4720
4721                                    ;LOAD, READ AND CHECK DIAGNOSTIC ADDRESS REGISTER BITS 7:0 WITH THE
4722                                    ;BINARY COUNT PATTERN (0-377).  ON A WRITE COMMAND TO CONTROL REGISTER 6
4723                                    ;WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC
4724                                    ;ADDRESS REGISTER VIA THE SIGNALS WPTO LB H AND WPTO HB H.  ON A READ
4725                                    ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAG-
4726                                    ;NOSTIC ADDRESS REGISTER VIA THE SIGNAL RPTO L.  PPEVIOUSLY IN THIS
4727                                    ;TEST, HDAL9 WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER
4728                                    ;BITS ONTO THE ADDRESS BUS.
4729
4730  012634  010137  002342            MOV     R1,R6LOAD               ;SETUP DATA TO BE LOADED
4731  012640  004737  006672            JSR     PC,LDRDR6               ;LOAD READ AND CHECK DIAG ADDRESS REG
4732  012644  001404                    BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4733  012646                            ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDR REG NOT EQUAL 125252
4734  012646  104455                    TRAP    C$ERDF
4735  012650  000004                    .WORD   4
4736  012652  002735                    .WORD   ADDRRG
4737  012654  005020                    .WORD   R06ERR
4738  012656                      3$:   ENDSEG
4739  012656                      10000$:
4740  012656  104405                    TRAP    C$ESEG
4741  012660  105201                    INCB    R1                      ;UPDATE THE TEST PATTERN BY ONE
4742  012662  001344                    BNE     1$                      ;IF NOT 0 THEN LOAD NEXT PATTERN
4743  012664                            ENDTST
4744  012664                      L10052:
4745  012664  104401                    TRAP    C$ETST
4746
```

```
                                .SBTTL  TEST 25: DIAG ADDR 15:0 REG TEST (HIGH BYTE) USING BINARY COUNT

                                ;++
                                ; THIS TEST WILL CHECK THE HIGH BYTE OF THE DIAGNOSTIC ADDRESS REGISTER USING A
                                ; BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT BY 400
                                ; UNTIL THE PATTERN 177400 HAS BEEN LOADED INTO DIAGNOSTIC ADDRESS REGISTER BITS
                                ; ADDR 15:8.  THE LOW BYTE OF THE DIAGNOSTIC ADDRESS REGISTER WILL BE LOADED
                                ; WITH ZEROES DURING THIS TEST.
                                ;
                                ; TO ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO THE ADDRESS
                                ; BUS AND TO DISABLE THE EIDAL BUS TO THE ADDRESS BUS, THE TEST WILL SET HDAL9 H
                                ; IN THE HDAL REGISTER TO A ONE. TO SELECT THE HDAL REG, THE TEST WILL
                                ; SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0.  ON A WRITE OR READ COMMAND
                                ; TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED BY THE WRITE SIGNALS
                                ; WRT3 LB H AND WRT3 HB H, AND BY THE READ SIGNAL RPT3 L.  TO SELECT THE DIAG-
                                ; NOSTIC ADDRESS REGISTER, THE TEST WILL CLEAR GDAL BITS 2:0 IN CONTROL REGISTER
                                ; 0.  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH GDAL BITS 2:0 CLEARED, DATA
                                ; WILL BE LOADED INTO THE ADDRESS REGISTER BY PULSES ON THE SIGNALS WPT0 LB H
                                ; AND WPT0 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, A PULSE WILL OCCUR
                                ; ON THE SIGNAL RPT0 L WHICH WILL CAUSE THE DATA TO BE READBACK FROM THE DIAG-
                                ; NOSTIC ADDRESS REGISTER.
                                ;--

012666                                  BGNTST
012666                          T25::
012666  004737  005570                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
012672  005001                           CLR     R1                      ;SET DATA PATTERN INITIALLY TO 0

012674                          1$:     BGNSEG
012674  104404                           TRAP    C$BSEG

                                ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
                                ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

012676  004737  006754                   JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH HDAL9 H SET TO A ONE.
                                ;ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED INTO THE
                                ;THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND WPT3 HB H.  ON A READ
                                ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE HDAL REG-
                                ;ISTER VIA THE SIGNAL RPT3 L.

012702  012737  001000  002342           MOV     #HDAL9,R6LOAD           ;SETUP DATA TO BE LOADED
012710  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REG
012714  001405                           BEQ     2$                      ;IF DATA LOADED OK THEN CONTINUE
012716                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 1000
012716  104455                           TRAP    C$ERDF
012720  000004                           .WORD   4
012722  002605                           .WORD   HDALRG
012724  005020                           .WORD   R06ERR
012726                                   CKLOOP
012726  104406                           TRAP    C$CLP1
```

```
                                        ;CLEAR GDAL BITS 2:0 IN CONTROL REGISTER 0 TO SELECT THE DIAGNOSTIC
                                        ;ADDRESS REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

012730  004737  007072        2$:       JSR     PC,SLDADR               ;SELECT DIAG ADDRESS REG VIA GDAL 2:0

                                        ;LOAD, READ AND CHECK DIAGNOSTIC ADDRESS REGISTER BITS 15:8 WITH THE
                                        ;BINARY COUNT PATTERN (400-177400).  ON A WRITE COMMAND TO CONTROL REG 6
                                        ;WITH GDAL BITS 2:0 CLEARED, DATA WILL BE LOADED INTO THE DIAGNOSTIC
                                        ;ADDRESS REGISTER VIA THE SIGNALS WPTO LB H AND WPTO HB H.  ON A READ
                                        ;COMMAND TO CONTROL REGISTER 6, DATA WILL BE READBACK FROM THE DIAG-
                                        ;NOSTIC ADDRESS REGISTER VIA THE SIGNAL RPTO L.  PREVIOUSLY IN THIS
                                        ;TEST, HDAL9 WAS SET TO A ONE TO ENABLE THE DIAGNOSTIC ADDRESS REGISTER
                                        ;BITS ONTO THE ADDRESS BUS.

012734  010137  002342                  MOV     R1,R6LOAD               ;SETUP DATA TO BE LOADED
012740  004737  006672                  JSR     PC,LDRDR6               ;LOAD READ AND CHECK DIAG ADDRESS REG
012744  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
012746                                  ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDR REG NOT EQUAL 125252
012750  104455                          TRAP    C$ERDF
012752  000004                          .WORD   4
012754  002735                          .WORD   ADDRRG
012756  005020                          .WORD   R06ERR
012756                          3$:     ENDSEG
012756                          10000$:
012756  104405                          TRAP    C$ESEG
012760  062701  000400                  ADD     #ADDR8,R1               ;UPDATE TEST PATTERN BY 400
012764  001343                          BNE     1$                      ;IF NOT 0 THEN LOAD NEXT PATTERN
012766                                  ENDTST
012766                          L10053:
012766  104401                          TRAP    C$ETST
```

```
                                        .SBTTL  TEST 26: READBACK MODE REG ON EODAL 15:0 BUS

                                        ;++
                                        ; THIS TEST WILL CHECK THAT THE MODE REGISTER CAN BE READBACK ON THE EODAL BUS.
                                        ; THE MODE REGISTER WILL BE LOADED WITH THE FOLLOWING PATTERNS: 125252,052525,
                                        ; 177400, 000377, 177777, AND 0000000.  FOR EACH PATTERN LOADED THE TEST
                                        ; WILL ENABLE THE MODE REGISTER ONTO THE EODAL BUS AND READ AND CHECK THE EODAL
                                        ; BUS FOR THE CORRECT MODE REGISTER PATTERN.  THE MODE REGISTER WILL BE ENABLED
                                        ; TO THE EODAL BUS WHEN ADAL12 H IS SET TO A ONE AND THE SIGNAL XBCLR H IS
                                        ; ASSERTED HIGH.
                                        ;--

012770                                          BGNTST
012770                                  T26::
012770  004737  005510                          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
012774  012701  013220                          MOV     #7$,R1                  ;GET ADDRESS OF STARTING DATA PATTERN
013000  012702  000006                          MOV     #6,R2                   ;COUNTER FOR NUMBER OF PATTERNS

013004                                  1$:     BGNSEG
013004  104404                                  TRAP    C$BSEG

                                                ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

013006  004737  006754                          JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0

                                                ;LOAD, READ AND CHECK THE HDAL REGISTER WITH HDAL7 H AND HDAL2 H SET TO
                                                ;ONES.  HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11
                                                ;TIMING AND CONTROL SIGNALS.  HDAL7 H ON A ONE WILL CAUSE THE SIGNALS
                                                ;PBCLR H AND XBCLR H TO BE ASSERTED HIGH.

013012  005037  002342                          CLR     R6LOAD                  ;SETUP TO CLEAR ALL OTHER HDAL BITS
013016  004737  007620                          JSR     PC,XBCLRH               ;SET XBCLR H (HIGH) AND HDAL2 H TO A 1

                                                ;SELECT THE MODE REGISTER BY SETTING GDAL2 H TO A ONE AND GDAL BITS
                                                ;1 AND 0 TO ZEROES.  THE MODE REGISTER WILL BE SELECTED ON A WRITE OR
                                                ;READ COMMAND TO CONTROL REGISTER 6.

013022  004737  007006                          JSR     PC,SLMODR               ;SELECT MODE REG VIA GDAL BITS 2:0

                                                ;LOAD, READ AND CHECK MODE REGISTER WITH ONE OF THE FOLLOWING DATA
                                                ;PATTERNS: 125252, 052525, 177400, 000377, 177777, AND 000000.

013026  011137  002342                          MOV     (R1),R6LOAD             ;GET A DATA PATTERN FROM TABLE
013032  004737  006672                          JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
013036  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
013040                                          ERRDF   4,MODREG,R06ERR         ;MODE REG NOT EQUAL TO EXPECTED
013040  104455                                  TRAP    C$ERDF
013042  000004                                  .WORD   4
013044  002631                                  .WORD   MODREG
013046  005020                                  .WORD   R06ERR
013050                                          CKLOOP
013050  104406                                  TRAP    C$CLP1

                                                ;SET ADAL12 H TO A ONE IN ADAL REGISTER.  WHEN ADAL12 H IS SET TO A ONE
                                                ;AND THE SIGNAL XBCLR H IS ASSERTED HIGH, THE MODE REGISTER WILL BE
                                                ;ENABLED TO THE EODAL BUS.
```

```
4888
4889  013052  012737  010000  002330  2$:     MOV     #ADAL12,R2LOAD          ;SETUP ADAL BITS TO BE LOADED
4890  013060  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
4891  013064  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4892  013066                                   ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
4893  013066  104455                          TRAP    C$ERDF
4894  013070  000002                          .WORD   2
4895  013072  002513                          .WORD   ADALRG
4896  013074  004770                          .WORD   R2EROR
4897  013076                                   CKLOOP
4898  013076  104406                          TRAP    C$CLP1
4899
4900                                           ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  AT THIS POINT
4901                                           ;THE MODE REGISTER WILL BE ENABLED TO THE EODAL BUS.  ON A READ COMMAND
4902                                           ;TO CONTROL REGISTER 6, THE MODE REGISTER WILL BE READBACK TO THE LSI-11
4903                                           ;TROUGH THE EODAL BUS
4904
4905  013100  004737  007122          3$:     JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
4906
4907                                           ;READ AND CHECK THAT THE MODE REGISTER WAS READBACK ON THE LSI-11 BUS
4908                                           ;THROUGH THE EODAL BUS, WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER
4909                                           ;6.  THE MODE REGISTER IS ENABLED TO THE EODAL BUS WHEN THE SIGNAL
4910                                           ;XBCLR H IS ASSERTED HIGH AND ADAL12 H IS SET TO A ONE.
4911
4912  013104  011137  002342                  MOV     (R1),R6LOAD             ;GET MODE REGISTER DATA PATTERN
4913  013110  004737  006700                  JSR     PC,READR6               ;GO READ MODE REG ON THE EODAL BUS
4914  013114  001405                          BEQ     4$                      ;IF DATA = MODE REG THEN CONTINUE
4915  013116                                   ERRDF   4,MEODAL,R026ER         ;MODE REGISTER TO EODAL BUS ERROR
4916  013116  104455                          TRAP    C$ERDF
4917  013120  000004                          .WORD   4
4918  013122  003102                          .WORD   MEODAL
4919  013124  005034                          .WORD   R026ER
4920  013126                                   CKLOOP
4921  013126  104406                          TRAP    C$CLP1
4922
4923                                           ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
4924
4925  013130  004737  006754          4$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
4926
4927                                           ;LOAD, READ AND CHECK THE HDAL REGISTER WITH A DATA PATTERN OF ALL
4928                                           ;ZEROES.  WHEN HDAL2 H IS SET TO A ZERO, THE T-11 WILL PROVIDE THE
4929                                           ;TIMING AND CONTROL SIGNALS TO THE TARGET EMULATOR MODULE.  AT THIS
4930                                           ;TIME, THE T-11 IS TURNED OFF AS A RESULT OF ADAL2 H BEING A ZERO.  WHEN
4931                                           ;THE T-11 IS TURNED OFF, THE SIGNALS PBCLR H AND XBCLR H WILL BE ASSERTED
4932                                           ;HIGH.  THEREFORE, THE MODE REGISTER SHOULD STILL BE ENABLED TO THE
4933                                           ;EODAL BUS AS A RESULT OF XBCLR H AND ADAL12 H BEING ASSERTED HIGH.
4934
4935  013134  005037  002342                  CLR     R6LOAD                  ;SETUP TO CLEAR ALL HDAL REGISTER BITS
4936  013140  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK THE HDAL REG
4937  013144  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
4938  013146                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
4939  013146  104455                          TRAP    C$ERDF
4940  013150  000004                          .WORD   4
4941  013152  002605                          .WORD   HDALRG
4942  013154  005020                          .WORD   R06ERR
4943  013156                                   CKLOOP
```

```
 4944  013156  104406                      TRAP    C$CLP1
 4945
 4946                                      ;SELECT THE EODAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
 4947
 4948  013160  004737  007122      5$:     JSR     PC,SEODAL ~             ;SELECT EODAL BUS VIA GDAL BITS 2:0
 4949
 4950                                      ;AS A RESULT OF HDAL2 H BEING CLEARED, THE T-11 WILL PROVIDE THE
 4951                                      ;TIMING AND CONTROL SIGNALS TO THE TARGET EMULATOR MODULE.  AT THIS
 4952                                      ;TIME, THE T-11 IS TURNED OFF BY ADAL2 H BEING A ZERO, THEREFORE,
 4953                                      ;THE SIGNALS PBCLR H AND XBCLR H WILL BE ASSERTED HIGH.  WHEN XBCLR H
 4954                                      ;AND ADAL12 H ARE ASSERTED HIGH, THE MODE REGISTER WILL BE ENABLED TO
 4955                                      ;THE EODAL BUS.
 4956
 4957  013164  011137  002342              MOV     (R1),R6LOAD             ;GET MODE REGISTER DATA PATTERN
 4958  013170  004737  006700              JSR     PC,READR6               ;READ THE EODAL BUS FOR MODE REG DATA
 4959  013174  001404                      BEQ     6$                      ;IF DATA OK THEN CONTINUE
 4960  013176                              ERRDF   4,MEODAL,R026ER         ;MODE REG TO EODAL BUS ERROR
 4961  013176  104455                      TRAP    C$ERDF
 4962  013200  000004                      .WORD   4
 4963  013202  003102                      .WORD   MEODAL
 4964  013204  005034                      .WORD   R026ER
 4965  013206                      6$:     ENDSEG
 4966  013206                      10000$:
 4967  013206  104405                      TRAP    C$ESEG
 4968
 4969  013210  005721                      TST     (R1)+                   ;UPDATE THE POINTER TO DATA TABLE
 4970  013212  005302                      DEC     R2                      ;CHECK IF ALL PATTERNS TESTED
 4971  013214  001273                      BNE     1$                      ;IF NOT THEN LOAD NEXT PATTERN
 4972  013216  000406                      BR      8$                      ;IF YES THEN END OF TEST
 4973
 4974  013220  125252              7$:     .WORD   125252
 4975  013222  052525                      .WORD   052525
 4976  013224  177400                      .WORD   177400
 4977  013226  000377                      .WORD   000377
 4978  013230  177777                      .WORD   177777
 4979  013232  000000                      .WORD   000000
 4980
 4981  013234                      8$:     ENDTST
 4982  013234                      L10054:
 4983  013234  104401                      TRAP    C$ETST
 4984
```

```
                                        .SBTTL  TEST 27: WRITE DIAG ADRESS REG INTO FJA READBACK REG (READ VIA RPT1 L)

                                        ;++
                                        ; THIS TEST WILL CHECK THE FORCE JUMP ADDRESS READBACK REGISTER WITH THE FOLLOWING
                                        ; DATA PATTERNS 125252, 052525, 177400, 000377 , 1777777, AND 000000. THE DIAG-
                                        ; NOSTIC ADDRESS REGISTER WILL PROVIDE THE DATA ON THE ADDRESS BUS TO THE FORCE
                                        ; JUMP ADDRESS REGISTER AND FORCE JUMP ADDRESS READBACK REGISTER.
                                        ;--

                                                BGNTST
013236                                  T27::
013236  004737  005510                            JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
013242  012701  013644                            MOV     #10$,R1                 ;GET ADDRESS OF DATA TABLE
013246  012702  000006                            MOV     #6,R2                   ;THE NUMBER OF DATA PATTERNS

013252                                  1$:     BGNSEG
013252  104404                                  TRAP    C$BSEG

                                                ;SELECT THE HDAL REGISTER BY SETTING GDAL1 AND GDAL0 TO ONES IN
                                                ;CONTROL REGISTER 0 GDAL BITS 2:0.  ON A WRITE COMMAND OR RFAD
                                                ;COMMAND TO CONTROL REGISTER 6, THE HDAL REGISTER WILL BE SELECTED.

013254  004737  006754                            JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA THE GDAL REG

                                                ;SET HDAL9 H AND HDAL2 H TO ONES IN THE HDAL REGISTER.  HDAL9 H ON A
                                                ;ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS REGISTER ONTO
                                                ;THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS BUS.
                                                ;HDAL2 H ON A ONE WILL ENABLE THE PROGRAM TO CONTROL THE T-11 TIMING
                                                ;AND CONTROL SIGNALS.  ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA
                                                ;WILL BE LOADED INTO THE HDAL REGISTER VIA THE SIGNALS WPT3 LB H AND
                                                ;WPT3 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE
                                                ;READBACK FROM THE HDAL REGISTER VIA THE SIGNAL RPT3 L.

013260  012737  001004  002342                    MOV     #HDAL9!HDAL2,R6LOAD     ;SETUP DATA TO BE LOADED
013266  004737  006672                            JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
013272  001405                                    BEQ     2$                      ;IF LOADED OK THEN CONTINUE
013274                                          ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
013274  104455                                  TRAP    C$ERDF
013276  000004                                  .WORD   4
013300  002605                                  .WORD   HDALRG
013302  005020                                  .WORD   R06ERR
013304                                          CKLOOP
013304  104406                                  TRAP    C$CLP1

                                                ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
                                                ;ZEROES.  ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE
                                                ;DIAGNOSTIC ADDRESS REGISTER WILL BE SELECTED.

013306  004737  007072            2$:         JSR     PC,SLDADR               ;GO SELECT DIAG ADDRESS REG VIA GDAL 2:0

                                                ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
                                                ;FOLLOWING DATA PATTERNS 125252, 052525, 177400, 000377, 177777 OR
                                                ;000000.  ON A WRITE COMMAND TO CONTROL REGISTER 6, DATA WILL BE LOADED
                                                ;INTO THE DIAGNOSTIC ADDRESS REGISTER VIA THE SIGNAL WPT0 LB H AND
                                                ;WPT0 HB H.  ON A READ COMMAND TO CONTROL REGISTER 6, DATA WILL BE READ-
                                                ;BACK FROM THE DIAGNOSTIC ADDRESS REGISTER VIA THE SIGNAL RPT0 L.
```

```
                                        ;PREVIOUSLY IN THIS TEST, HDAL9 H WAS SET TO A ONE TO DISABLE THE EIDAL
                                        ;BUS FROM THE ADDRESS BUS AND ENABLE THE DIAGNOSTIC ADDRESS REGISTER TO
                                        ;THE ADDRESS BUS.

013312  011137  002342                  MOV     (R1),R6LOAD             ;GET THE DATA PATTERN FROM THE TABLE
013316  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK DIAG ADDR REG
013322  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
013324                                  ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDRESS REG NOT EQUAL EXPECTED
013324  104455                          TRAP    C$ERDF
013326  000004                          .WORD   4
013330  002735                          .WORD   ADDRRG
013332  005020                          .WORD   R06ERR
013334                                  CKLOOP
013334  104406                          TRAP    C$CLP1

                                        ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE.  SET
                                        ;AND CLEAR VDAL2 H TO CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS AND OTHER
                                        ;FLIP-FLOPS.

013336  012737  000200  002334  3$:     MOV     #VDAL7,R4LOAD           ;SETUP BIT TO SET FETCT H
013344  004737  007712                  JSR     PC,CLRPSM               ;SET FETCT H AND CLEAR PAUSE STATE F/F'S

                                        ;RESELECT THE HDAL REGISTER VIA THE GDAL REGISTER, SO THAT THE SIGNALS
                                        ;XRAS H AND XRAS L CAN BE PULSED BY SETTING AND CLEARING HDAL12 H.

013350  004737  006754                  JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA THE GDAL REG

                                        ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING THE SIGNAL
                                        ;HDAL12 H.  THE SIGNAL XRAS H WILL CLOCK THE STATE OF FETCT H INTO THE
                                        ;EDFET FLIP-FLOP, THUS SETTING EDFET H TO A ONE.  THE SIGNAL XRAS H WILL
                                        ;CAUSE THE SIGNAL RASP H TO PULSE.  WHEN THE EDFET FLIP-FLOP IS SET TO A
                                        ;ONE AND THE SIGNAL RASP H IS PULSED, A PULSE WILL BE ISSUED
                                        ;ON THE SIGNAL DFET H.  THE SIGNAL DFET H WILL CLOCK THE DIAGNOSTIC
                                        ;ADDRESS REGISTER WHICH IS ENABLED TO THE ADDRESS BUS INTO THE OLD FORCE
                                        ;JUMP ADDRESS REGISTER AND THE FORCE JUMP ADDRESS READBACK REGISTER.

013354  012737  001004  002342          MOV     #HDAL9!HDAL2,R6LOAD     ;RESET PREVIOUS CONTENTS OF HDAL REG
013362  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS L AND XRAS H VIA HDAL12 H

                                        ;ADAL4 H WAS SET TO A ZERO AT THE BEGINNING OF THIS TEST IN THE ROUTINE
                                        ;"INITTE".  PULSING THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H (0)
                                        ;INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L TO THE
                                        ;HIGH STATE (1).  THE SIGNAL PAUSE L BEING ASSERTED HIGH WILL CAUSE THE
                                        ;SIGNAL SOP H TO BE ASSERTED HIGH.  WHEN SOP H AND EDFET H ARE ASSERTED
                                        ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE,
                                        ;THUS SETTING THE SIGNAL PSMW H TO THE HIGH STATE.  THE SIGNAL PSMW H
                                        ;IS READ IN VDAL REGISTER AS VDAL9 H.

013366  052737  001000  002336          BIS     #VDAL9,R4GOOD           ;SETUP TO EXPECT PSMW H TO BE A 1
013374  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
013400  001405                          BEQ     4$                      ;IF OK THEN CONTINUE
013402                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
013402  104455                          TRAP    C$ERDF
013404  000003                          .WORD   3
013406  002537                          .WORD   VDALRG
013410  005004                          .WORD   R4EROR
```

```
5097  013412                                CKLOOP
5098  013412  104406                        TRAP    C$CLP1
5099
5100                                        ;SELECT THE FORCE JUMP ADDRESS REGISTER BY SETTING GDAL0 H TO A ONE
5101                                        ;AND GDAL1 H AND GDAL2 H TO ZEROES.  ON A READ COMMAND TO CONTROL
5102                                        ;REGISTER 6, THE FORCE JUMP ADDRESS READBACK REGISTER WILL BE READBACK
5103                                        ;VIA THE SIGNAL RPT1 L.
5104
5105  013414  004737  007040        4$:     JSR     PC,SLFJAR               ;GO SELECT FJA REG VIA GDAL REG
5106
5107                                        ;READ THE FORCE JUMP ADDRESS READBACK REGISTER TO CHECK THAT THE DIAG-
5108                                        ;NOSTIC ADDRESS REGISTER DATA WAS LOADED INTO IT WHEN THE SIGNAL RASP H
5109                                        ;WAS PULSED WITH THE FLIP-FLOP DFET H SET TO A ONE.  THE FORCE JUMP ADDRESS
5110                                        ;READBACK REGISTER IS LOADED BY THE SIGNAL DFET H.
5111
5112  013420  011137  002342                MOV     (R1),R6LOAD             ;GET PATTERN LOADED INTO DIAG ADDR REG
5113  013424  004737  006700                JSR     PC,READR6               ;GO READ FORCE JUMP ADDRESS READBACK REG
5114  013430  001405                        BEQ     5$                      ;IF DATA OK THEN CONTINUE
5115  013432                                ERRDF   4,FJADRG,R06ERR         ;FJA READBACK REG NOT = DIAG ADDRESS REG
5116  013432  104455                        TRAP    C$ERDF
5117  013434  000004                        .WORD   4
5118  013436  002766                        .WORD   FJADRG
5119  013440  005020                        .WORD   R06ERR
5120  013442                                CKLOOP
5121  013442  104406                        TRAP    C$CLP1
5122
5123                                        ;RESELECT THE DIAGNOSTIC ADDRESS REGISTER VIA THE GDAL BITS
5124
5125  013444  004737  007072        5$:     JSR     PC,SLDADR               ;GO SELECT DIAG ADDRESS REG VIA GDAL 2:0
5126
5127                                        ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA
5128                                        ;PATTERN OF 031463.
5129
5130  013450  012737  031463  002342        MOV     #031463,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
5131  013456  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK DIAG ADDR REG
5132  013462  001405                        BEQ     6$                      ;IF LOADED OK THEN CONTINUE
5133  013464                                ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDRESS REG NOT EQUAL EXPECTED
5134  013464  104455                        TRAP    C$ERDF
5135  013466  000004                        .WORD   4
5136  013470  002735                        .WORD   ADDRRG
5137  013472  005020                        .WORD   R06ERR
5138  013474                                CKLOOP
5139  013474  104406                        TRAP    C$CLP1
5140
5141                                        ;SET THE SIGNAL VDAL7 H TO A ZERO TO ASSERT THE SIGNAL FETCT H LOW.
5142
5143  013476  042737  000200  002334  6$:   BIC     #VDAL7,R4LOAD           ;SETUP TO CLEAR THE SIGNAL FETCT H
5144  013504  012737  001000  002336        MOV     #VDAL9,R4GOOD           ;SETUP TO EXPECT PSMW H TO BE SET TO 1
5145  013512  004737  006646                JSR     PC,LDRD4R               ;GO LOAD, READ AND CHECK VDAL REG
5146  013516  001405                        BEQ     7$                      ;IF LOADED OK THEN CONTINUE
5147  013520                                ERRDF   3,VDALRG,R4EROR         ;VDAL REG OR PAUSE STATE MACHINE ERROR
5148  013520  104455                        TRAP    C$ERDF
5149  013522  000003                        .WORD   3
5150  013524  002537                        .WORD   VDALRG
5151  013526  005004                        .WORD   R4EROR
5152  013530                                CKLOOP
```

```
                013530  104406                  TRAP    C$CLP1
5154
5155                                            ;RESELECT THE HDAL REGISTER VIA THE GDAL REGISTER SO THAT THE SIGNAL
5156                                            ;XRAS H AND XRAS L CAN BE PULSED BY SETTING AND CLEARING HDAL12 H.
5157
5158    013532  004737  006754          7$:     JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA THE GDAL REG
5159
5160                                            ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  WITH THE
5161                                            ;SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE EDFET
5162                                            ;FLIP-FLOP WILL BE SET TO A ZERO, THUS ASSERTING THE SIGNAL EDFET H TO
5163                                            ;THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL PB H WILL BE
5164                                            ;ASSERTED LOW.  WHEN THE SIGNAL XRAS H IS ASSERTED PULSES WILL OCCUR ON
5165                                            ;THE SIGNALS RASP H AND RASP L.
5166                                            ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE SIGNAL
5167                                            ;RASP L WHEN THE SIGNALS EPFN L, EP8N L AND PSMW H ARE ALL ASSERTED TO
5168                                            ;THE  HIGH  STATE.  WHEN THE EDFET H FLIP-FLOP IS SET TO A ZERO AND THE
5169                                            ;SIGNAL RASP H IS PULSED, NO PULSE SHOULD OCCUR ON THE SIGNAL DFET H,
5170                                            ;THERFORE, THE DIAGNOSTIC ADDRESS REGISTER WHICH IS ENABLED TO THE
5171                                            ;ADDRESS BUS WILL NOT BE LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER
5172                                            ;OR THE FORCE JUMP ADDRESS READBACK REGISTER.  THE ADDRESS BUS PRESENTLY
5173                                            ;CONTAINS THE DIAGNOSTIC ADDRESS REGISTER DATA PATTERN 031463.
5174
5175    013536  012737  001004  002342          MOV     #HDAL9!HDAL2,R6LOAD     ;RESET PREVIOUS CONTENTS OF HDAL REG
5176    013544  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS L AND XRAS H VIA HDAL12 H
5177
5178                                            ;CHECK THAT THE SIGNAL PSMW H IS STILL SET IN THE VDAL REGISTER AS A
5179                                            ;RESULT OF THE PAUSE STATE MACHINE WORKING FLIP-FLOP BEING SET.
5180
5181    013550  004737  006654                  JSR     PC,READR4               ;GO CHECK VDAL AND PAUSE STATE MACHINE
5182    013554  001405                          BEQ     8$                      ;IF NO CHANGES THEN CONTINUE
5183    013556                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
5184    013556  104455                          TRAP    C$ERDF
5185    013560  000003                          .WORD   3
5186    013562  002537                          .WORD   VDALRG
5187    013564  005004                          .WORD   R4EROR
5188    013566                                  CKLOOP
5189    013566  104406                          TRAP    C$CLP1
5190
519                                             ;RESELECT THE FORCE JUMP ADDRESS REGISTER VIA THE GDAL REGISTER BITS
5192                                            ;2:0.  ON A READ COMMAND TO CONTROL REGISTER 6, THE FORCE JUMP ADDRESS
5193                                            ;READBACK REGISTER WILL BE READBACK VIA THE SIGNAL RPT1 L.
5194
5195    013570  004737  007040          8$:     JSR     PC,SLFJAR               ;GO SELECT THE FORCE JUMP ADDRESS REG
5196
5197                                            ;READ THE FORCE JUMP ADDRESS READBACK REGISTER AND CHECK THAT THE NEW
5198                                            ;DATA (031463) WAS NOT LOADED INTO IT WHEN THE SIGNAL EDFET H IS
5199                                            ;ASSERTED LOW AND THE SIGNAL RASP H WAS PULSED.  NO PULSES SHOULD
5200                                            ;OCCUR ON THE SIGNAL DFET H WHEN THE SIGNAL EDFET H IS LOW.
5201
5202    013574  011137  002342                  MOV     (R1),R6LOAD             ;GET THE DATA PREVIOUSLY LOADED INTO
5203                                                                            ;THE FORCE JUMP ADDRESS REGISTER
5204    013600  004737  006700                  JSR     PC,READR6               ;GO READ FORCE JUMP ADDRESS REGISTER
5205    013604  001405                          BEQ     9$                      ;IF NO CHANGE IN DATA THEN CONTINUE
5206    013606                                  ERRDF   4,FJADRG,R06ERR         ;FORCE JUMP ADDRESS READBACK REG ERROR
5207    013606  104455                          TRAP    C$ERDF
5208    013610  000004                          .WORD   4
```

```
5209  013612  002766                  .WORD   FJADRG
5210  013614  005020                  .WORD   R06ERR
5211                                                    ;IF DATA EQUALS 031463 THEN DFET H WAS
5212                                                    ;PULSED WHEN FETCT H WAS ASSERTED LOW
5213  013616                          CKLOOP
5214  013616  104406                  TRAP    C$CLP1
5215
5216                                  ;CLEAR THE PAUSE STATE MACHINE BY SETTING AND CLEARING WAL2 H
5217
5218  013620  005037  002334    9$:   CLR     R4LOAD                  ;SETUP TO EXPECT PSMW H TC BE A 0
5219  013624  004737  007712          JSR     PC,CLRPSM
5220  013630                          ENDSEG
5221  013630                  10000$:
5222  013630  104405                  TRAP    C$ESEG
5223
5224  013632  005721                  TST     (R1)+                   ;UPDATE POINTER TO DATA TABLE
5225  013634  005302                  DEC     R2                      ;CHECK IF ALL DATA PATTERNS LOADED
5226  013636  001410                  BEQ     11$                     ;IF YES THEN END OF THE TEST
5227  013640  000137  013252          JMP     1$                      ;IF NOT LOAD NEXT PATTERN
5228
5229  013644  125252            10$:  .WORD   125252
5230  013646  052525                  .WORD   052525
5231  013650  177400                  .WORD   177400
5232  013652  000377                  .WORD   000377
5233  013654  177777                  .WORD   177777
5234  013656  000000                  .WORD   000000
5235
5236  013660                  11$:    ENDTST
5237  013660                  L10055:
5238  013660  104401                  TRAP    C$ETST
```

```
                                .SBTTL  TEST 28: PAUSE STATE MACHINE - 16 BIT ADDRESS - PAUSE MODE - OLD FJA

                                ;++
                                ; THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 16 BIT ADDRESS MODE.  THE
                                ; PAUSE  STATE  MACHINE  FLIP-FLOPS , PAUSE STATE WORKING , AND  PAUSE
                                ; STATE SYNC AND 16 BIT ADDRESS WILL BE CLOCKED TO ONES AND ZEROES BY PULSING
                                ; THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL
                                ; FETCT H.  THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO AND ADAL0 H
                                ; WILL BE SET TO A ONE DURING THIS TEST.  ADAL4 H ON A ZERO WILL PUT THE PAUSE
                                ; STATE MACHINE IN PAUSE MODE.  ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT BREAK
                                ; SIGNAL FROM CAUSING A BREAK AND ADAL0 H ON A ONE WILL CLEAR THE BREAK LOGIC,
                                ; THUS SETTING THE SIGNAL BRK H TO A ZERO.
                                ;
                                ; THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE OLD
                                ; FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS.  THE OLD FORCE JUMP
                                ; ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125252, 052525
                                ; 177400, 000377, 177777, AND 000000.  THE OLD FORCE JUMP ADDRESS REGISTER GETS
                                ; ITS DATA FROM THE DIAGNOSTIC ADDRESS REGISTER WHICH IS ENABLED ON THE ADDRESS
                                ; BUS DURING THIS TEST.
                                ;--

013662                                  BGNTST
013662                          T28::
013662  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
013666  012701  014552                   MOV     #19$,R1                 ;GET ADDRESS OF DATA TABLE
013672  012702  000006                   MOV     #6,R2                   ;COUNTER FOR NUMBER OF DATA PATTERNS

013676                          1$:     BGNSEG
013676  104404                          TRAP    C$BSEG

                                        ;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDAL0
                                        ;TO A ZERO.

013700  004737  007006                   JSR     PC,SLMODR               ;GO SELECT MODE REG VIA CONTROL REG 0

                                        ;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH ZEROES.  MR BIT 11
                                        ;ON A ZERO WILL ENABLE 16 BIT ADDRESS SELECTION TO THE PAUSE STATE
                                        ;MACHINE.

013704  005037  002342                   CLR     R6LOAD                  ;SETUP DATA TO BE ZERO
013710  004737  006672                   JSR     PC,LDRDR6               ;LOAD, READ AND CHECK MODE REGISTER
013714  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
013716                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO 0
013716  104455                          TRAP    C$ERDF
013720  000004                          .WORD   4
013722  002631                          .WORD   MODREG
013724  005020                          .WORD   R06ERR
013726                                  CKLOOP
013726  104406                          TRAP    C$CLP1

                                        ;SET GDAL1 AND GDAL0 TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
                                        ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

013730  004737  006754          2$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0

                                        ;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
```

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5295                                        ;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
5296                                        ;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
5297                                        ;BUS.  HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
5298                                        ;TIMING AND CONTROL SIGNALS.
5299
5300  013734  012737  001004  002342        MOV     #HDAL9.HDAL2,R6LOAD     ;SETUP BITS TO BE LOADED
5301  013742  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
5302  013746  001405                        BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5303  013750                                ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
5304  013750  104455                        TRAP    C$ERDF
5305  013752  000004                        .WORD   4
5306  013754  002605                        .WORD   HDALRG
5307  013756  005020                        .WORD   R06ERR
5308  013760                                CKLOOP
5309  013760  104406                        TRAP    C$CLP1
5310
5311                                        ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
5312                                        ;ZEROES.  ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
5313                                        ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.
5314
5315  013762  004737  007072        3$:     JSR     PC,SLDADR               ;GO SELECT DIAG. ADDRESS REG VIA GDAL 2:0
5316
5317                                        ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
5318                                        ;FOLLOWING DATA PATTERNS: 125252, 052525, 177400, 000377, 177777, AND
5319                                        ;000000.
5320
5321  013766  011137  002342                MOV     (R1),R6LOAD             ;GET DATA PATTERN FROM TABLE
5322  013772  004737  006672                JSR     PC,LDRDR6               ;GO LOAD READ AND CHECK DIAG ADDRESS REG
5323  013776  001405                        BEQ     4$                      ;IF LOADED OK THEN CONTINUE
5324  014000                                ERRDF   4,ADDRRG,R06FRR         ;DIAG ADDRESS REG NOT EQUAL EXPECTED
5325  014000  104455                        TRAP    C$ERDF
5326  014002  000004                        .WORD   4
5327  014004  002735                        .WORD   ADDRRG
5328  014006  005020                        .WORD   R06ERR
5329  014010                                CKLOOP
5330  014010  104406                        TRAP    C$CLP1
5331
5332                                        ;LOAD, READ AND CHECK  ADAL REGISTER WITH A DATA PATTERN OF 000001.
5333                                        ;ADAL0 ON A ONE WILL HOLD THE BREAK LOGIC CLEARED.  ADAL4 ON A ZERO
5334                                        ;WILL CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE
5335                                        ;WHEN THE SIGNAL XRAS H IS PULSED.
5336
5337  014012  012737  000001  002330  4$:     MOV     #ADAL0,R2LOAD           ;SETUP BIT TO BE LOADED
5338  014020  004737  006614                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REG
5339  014024  001405                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
5340  014026                                ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL 1
5341  014026  104455                        TRAP    C$ERDF
5342  014030  000002                        .WORD   2
5343  014032  002513                        .WORD   ADALRG
5344  014034  004770                        .WORD   R2EROR
5345  014036                                CKLOOP
5346  014036  104406                        TRAP    C$CLP1
5347
5348                                        ;SET VDAL2 H TO A ONE AND THEN CLEAR VDAL2 H. VDAL2 H ON A ONE WILL
5349                                        ;CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS
5350
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5351  014040  005037  002334          5$:     CLR     R4LOAD                  ;SETUP TO CLEAR ALL BITS IN VDAL REG
5352  014044  004737  007712                  JSR     PC,CLRPSM               ;GO SET AND CLEAR VDAL2 H
5353
5354                                          ;SELECT THE NEW FORCE JUMP ADDRESS REGISTER BY SETTING GDAL1 H TO A
5355                                          ;ONE AND GDAL BITS 1 AND 2 TO ZEORES.  ON A WRITE COMMAND TO CONTROL
5356                                          ;REGISTER 6, DATA WILL BE LOADED INTO THE NEW FORCE JUMP ADDRESS
5357                                          ;REGISTER  AND THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL BE SET
5358                                          ;TO A ONE.
5359
5360  014050  004737  007040                  JSR     PC,SLFJAR               ;SELECT FORCE JUMP ADDRESS REG VIA GDAL
5361
5362                                          ;ISSUE A WRITE COMMAND TO CONTROL REGISTER 6 TO WRITE THE DATA PATTERN
5363                                          ;146314 INTO THE NEW FORCE JUMP ADDRESS REGISTER VIA THE SIGNALS
5364                                          ;WPT1 HB H AND WPT1 LB H.  THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP
5365                                          ;WILL ALSO GET SET VIA THE SIGNAL WPT1 LB H.  THE NEW FORCE JUMP
5366                                          ;ADDRESS REGISTER IS WRITTEN WITH DATA TO CHECK THAT THE CORRECT FORCE
5367                                          ;JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL BUS WHEN THE 16 BIT
5368                                          ;ADDRESS FLIP-FLOP IS SET.  THE OLD FORCE JUMP ADDRESS REGISTER SHOULD
5369                                          ;BE ENABLED TO THE EODAL BUS DURING THIS TEST.  THE TAKE NEW FORCE
5370                                          ;JUMP ADDRESS FLIP-FLOP WILL BE CLEARED FOLLOWING THE CHECK THAT IT
5371                                          ;WAS SET TO A ONE.
5372
5373  014054  012777  146314  166224          MOV     #146314,@REG6           ;WRITE NEW FORCE JUMP ADDRESS REGISTER
5374
5375                                          ;READ THE VDAL REGISTER TO CHECK THAT THE NEW FORCE JUMP ADDRESS FLIP-
5376                                          ;FLOP IS SET TO A ONE.  THE FLIP-FLOP WILL BE READ IN THE VDAL REGISTER
5377                                          ;AS THE SIGNAL TNFJ H.
5378
5379  014062  052737  100000  002336          BIS     #VDAL15,R4GOOD          ;SETUP TO EXPECT TNFJ H TO BE A 1
5380  014070  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
5381  014074  001405                          BEQ     8$                      ;IF TNFJ H SET THEN CONTINUE
5382  014076                                  ERRDF   3,VDALRG,R4EROR         ;TNFJ H PROBABLY NOT SET IN VDAL REG
5383  014076  104455                          TRAP    C$ERDF
5384  014100  000003                          .WORD   3
5385  014102  002537                          .WORD   VDALRG
5386  014104  005004                          .WORD   R4EROR
5387  014106                                  CKLOOP
5388  014106  104406                          TRAP    C$CLP1
5389
5390                                          ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H. SET VDAL2 H TO A ONE
5391                                          ;TO CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS AND THE TAKE NEW FORCE
5392                                          ;JUMP ADDRESS FLIP-FLOP.
5393
5394  014110  012737  000200  002334  8$:     MOV     #VDAL7,R4LOAD           ;SETUP BIT TO SET FETCT H
5395  014116  004737  007712                  JSR     PC,CLRPSM               ;GO SET FETCT H AND PULSE VDAL2 H
5396
5397                                          ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
5398                                          ;TO ONES.  BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
5399                                          ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L
5400
5401  014122  004737  006754                  JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL 2:0
5402
5403                                          ;TOGGLE THE SIGNAL XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
5404                                          ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
5405                                          ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
5406                                          ;HIGH STATE.  THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
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                                        ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
                                        ;TO THE HIGH STATE.  THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
                                        ;SIGNAL PAUSE L IS ASSERTED HIGH.  WHEN SOP H AND FETCT H ARE ASSERTED
                                        ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
                                        ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
                                        ;PSMW H WILL BE ASSERTED HIGH.  THE SIGNAL PSMW H IS READ IN THE VDAL
                                        ;REGISTER AS VDAL9 H.  WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
                                        ;SIGNAL PB H WILL BE ASSERTED HIGH.  THE SIGNAL PB H IS THE DATA INPUT
                                        ;LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
                                        ;
                                        ;THE SIGNAL XRAS H WILL CAUSE THE SIGNAL RASP H TO BE PULSED.  WHEN THE
                                        ;SIGNAL RASP H IS PULSED AND THE SIGNAL EDFET H IS ASSERTED HIGH, A
                                        ;PULSE WILL BE ISSUED ON THE SIGNAL DFET H.  THE SIGNAL DFET H WILL
                                        ;CLOCK THE ADDRESS BUS INTO THE OLD FORCE JUMP ADDRESS REGISTER.  AT THE
                                        ;PRESENT TIME THE DIAGNOSTIC ADDRESS REGISTER IS ENABLED ONTO THE
                                        ;ADDRESS BUS, THEREFORE THE OLD FORCE JUMP ADDRESS REGISTER WILL BE
                                        ;LOADED WITH THE DATA FROM THE DIAGNOSTIC ADDRESS REGISTER.

014126  012737  001004  002342          MOV     #HDAL9!HDAL2,R6LOAD     ;BITS PREVIOUSLY SET IN HDAL REG
014134  004737  007272                  JSR     PC,XRAS                 ;PULSE XRAS H AND XRAS L VIA HDAL12 H

                                        ;CLEAR VDAL7 H IN THE VDAL REGISTER THUS SETTING THE SIGNAL FETCT H TO
                                        ;THE LOW STATE.  CHECK THE PAUSE STATE MACHINE TO BE IN THE FOLLOWING
                                        ;STATE AS A RESULT OF SOP H AND EDFET H BEING ASSERTED HIGH.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    16 BIT ADDRESS - EPFN H - 0

014140  042737  000200  002334          BIC     #VDAL7,R4LOAD           ;SETUP TO CLEAR FETCT H
014146  013737  002334  002336          MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
014154  052737  001000  002336          BIS     #VDAL9,R4GOOD           ;EXPECT PSMW H TO BE SET
014162  004737  006646                  JSR     PC,LDRD4R               ;GO LOAD, READ AND CHECK VDAL REG
014166  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
014170                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
014170  104455                          TRAP    C$ERDF
014172  000003                          .WORD   3
014174  002537                          .WORD   VDALRG
014176  005004                          .WORD   R4EROR
014200                                  CKLOOP
014200  104406                          TRAP    C$CLP1

                                        ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
                                        ;SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
                                        ;SIGNAL "PB H", WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
                                        ;SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE.  THE SIGNAL XCAS H
                                        ;WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-FLOP (0)
                                        ;INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE 16 BIT ADDRESS
                                        ;FLIP-FLOP TO A ZERO.

014202  004737  007410          11$:    JSR     PC,XCASH                ;SET XCAS H TO THE HIGH STATE

                                        ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                        ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING SET TO 1.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    16 BIT ADDRESS - EPFN H - 0
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                                BIS     #VDAL10,R4GOOD          ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
                                JSR     PC,READR4               ;GO READ AND CHECK PAUSE STATE MACHINE
                                BEQ     12$                     ;IF LOADED OK THEN CONTINUE
                                ERRDF   3,VDALRG,R4EROR         ;EPSF H PROBABLE NOT SET IN VDAL REG
                                TRAP    C$ERDF
                                .WORD   3
                                .WORD   VDALRG
                                .WORD   R4EROR
                                CKLOOP
                                TRAP    C$CLP1

                                ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE 16 BIT
                                ;INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE EODAL BUS AT THIS TIME.
                                ;ON A READ COMMAND TO CONTROL REGISTER 6. THE EODAL BUS WILL BE ENABLED
                                ;TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.

                        12$:    JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0

                                ;THE SIGNAL ACAS H WILL BE ASSERTED HIGH AS A RESULT OF THE SIGNAL
                                ;XCAS H BEING ASSERTED HIGH AND THE SIGNAL PSMW H BEING ASSERTED HIGH.
                                ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH AND THE PAUSE STATE SYNC FLIP-
                                ;FLOP IS SET TO A ONE, THE SIGNALS EDRL L AND EDRH L WILL BE ASSERTED
                                ;LOW.  THESE TWO SIGNALS WILL ENABLE THE 16 BIT INSTRUCTION REGISTER
                                ;ONTO THE EODAL BUS.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER
                                ;6 WITH GDAL BITS 2:0 SET TO ONES, A PULSE WILL BE ISSUED ON THE SIGNAL
                                ;RPT7 L.  THE SIGNAL RPT7 L WILL READBACK THE 16 BIT INSTRUCTION REGIS-
                                ;TER WHICH IS ENABLED TO THE EODAL BUS AT THIS POINT IN TIME.

                                MOV     #137,R6LOAD             ;SETUP EXPECTED 16 BIT INSTRUCTION (JMP)
                                JSR     PC,READR6               ;READ 16 BIT INSTRUCTION REG ON EODAL BUS
                                BEQ     13$                     ;IF INSTRUCTION EQUALS "JMP" THEN CONT
                                ERRDF   4,IEODAL,R06ERR         ;EODAL BUS ERROR OR 16 BIT INSTRUCTION
                                TRAP    C$ERDF
                                .WORD   4
                                .WORD   IEODAL
                                .WORD   R06ERR
                                                                ;REGISTER ERROR, OR 16 BIT INSTRUCTION
                                                                ;REGISTER NOT ENABLED TO THE BUS
                                CKLOOP
                                TRAP    C$CLP1

                                ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND
                                ;GDAL0 TO ONES.

                        13$:    JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0

                                ;SET THE SIGNAL XCAS H TO A ZERO BY CLEARING HDAL13 H IN HDAL REGISTER

                                MOV     #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
                                JSR     PC,XCASL                ;GO SET XCAS H TO THE LOW STATE

                                ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
                                ;THIS IS DONE TO SIMULATE A MACHINE CYCLE.

                                JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
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                                        ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
                                        ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
                                        ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
                                        ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
                                        ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
                                        ;AND RASP L WILL BE PULSED.
                                        ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
                                        ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.

014310  004737  007272                 JSR     PC,XRAS                 ;GO PULSE XRAS H BY HDAL12

                                        ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
                                        ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    16 BIT ADDRESS - EPFN H - 0

014314  004737  006654                 JSR     PC,READR4               ;CHECK VDAL AND PAUSE STATE MACHINE
014320  001405                          BEQ     14$                     ;IF OK THEN CONTINUE
014322                                  ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE WORKING F/F PROBABLY NOT SET
014322  104455                          TRAP    C$ERDF
014324  000003                          .WORD   3
014326  002537                          .WORD   VDALRG
014330  005004                          .WORD   R4EROR
014332                                  CKLOOP
014332  104406                          TRAP    C$CLP1

                                        ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
                                        ;SIGNAL XCAS H GOING FROM A 0 TO A 1 WILL CLOCK THE LEVEL OF THE
                                        ;SIGNAL "PB H", WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP,
                                        ;THUS CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO.  THE SIGNAL
                                        ;XCAS H WILL ALSO CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC
                                        ;FLIP-FLOP (1) INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE
                                        ;16 BIT ADDRESS FLIP-FLOP TO A ONE.

014334  004737  007410          14$:    JSR     PC,XCASH                ;SET THE SIGNAL XCAS H TO HIGH STATE

                                        ;READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
                                        ;FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING A 1.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    16 BIT ADDRESS - EPFN H - 1

014340  042737  002000  002336          BIC     #VDAL10,R4GOOD          ;CLEAR BITS FOR EPSF H
014346  052737  004000  002336          BIS     #VDAL11,R4GOOD          ;SET BIT FOR EPFN H
014354  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
014360  001405                          BEQ     15$                     ;IF OK THEN CONTINUE
014362                                  ERRDF   3,VDALRG,R4EROR         ;EPFN H PROBABLY NOT SET IN VDAL REG
014362  104455                          TRAP    C$ERDF
014364  000003                          .WORD   3
014366  002537                          .WORD   VDALRG
014370  005004                          .WORD   R4EROR
014372                                  CKLOOP
014372  104406                          TRAP    C$CLP1
```

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                                        ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE FORCE
                                        ;JUMP ADDRESS REGISTER SHOULD BE ENABLED ON THE EODAL BUS AT THIS TIME.
                                        ;ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ
                                        ;BACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.

014374  004737  007122          15$.   JSR     PC,SEODAL                ;SELECT EODAL BUS VIA GDAL BITS 2:0

                                        ;ON THE FIRST PULSE OF XRAS H WHEN THE SIGNAL EDFET H WAS SET HIGH,
                                        ;THE FORCE JUMP ADDRESS REGISTER SHOULD HAVE BEEN LOADED WITH THE DATA
                                        ;IN THE DIAGNOSTIC ADDRESS REGISTER VIA THE CLOCKING SIGNAL DFET H
                                        ;(ADDRESS BUS TO FORCE JUMP ADDRESS REGISTER).  AT THIS POINT IN TIME,
                                        ;THE FORCE JUMP ADDRESS REGISTER WILL BE ENABLED TO THE EODAL BUS VIA
                                        ;THE SIGNALS OEARH L AND OEARL L.  THESE SIGNALS ARE ASSERTED LOW AS A
                                        ;RESULT OF THE FLIP-FLOP "GET NEW ADDRESS" BEING CLEARED AND THE
                                        ;SIGNALS EARH H AND EARL H BEING ASSERTED HIGH.  THE "GET NEW ADDRESS"
                                        ;FLIP-FLOP WAS CLEARED AT THE BEGINNING OF THE TEST WHEN VDAL REGISTER
                                        ;BIT 2 WAS SET AND CLEARED.  THE SIGNAL EARH H AND EARL H ARE ASSERTED
                                        ;HIGH AS A RESULT OF THE 16 BIT ADDRESS FLIP-FLOP BEING SET TO A ONE,
                                        ;THE SIGNAL ACAS H BEING ASSERTED HIGH, AND MODE REGISTER BIT 11 SETUP
                                        ;FOR 16 BIT ADDRESS MODE.  THE FOLLOWING SECTION WILL READ THE EODAL
                                        ;BUS VIA THE SIGNAL RPT7 L AND CHECK THAT THE DIAGNOSTIC ADDRESS
                                        ;REGISTER WAS LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER AND THAT
                                        ;THE OLD FORCE JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL BUS.
                                        ;
                                        ;IF THE ADDRESS READ FROM THE FORCE JUMP ADDRESS REGISTER EQUALS
                                        ;146314 THEN THE WRONG FORCE JUMP ADDRESS REGISTER WAS READ.  THE
                                        ;DATA PATTERN 146314 WAS WRITTEN INTO THE NEW FORCE JUMP ADDRESS
                                        ;REGISTER WHICH SHOULD NOT BE SELECTED.  CHECK THE "GET NEW ADDRESS"
                                        ;FLIP-FLOP TO CHECK THAT IT IS CLEARED.  THE "GET NEW ADDRESS" FLIP
                                        ;FLOP WAS CLEARED BY VDAL2 H AT THE BEGINNING OF THE TEST.  THE OLD
                                        ;FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL BUS DURING
                                        ;THIS TEST.  THE OLD FORCE JUMP ADDRESS REGISTER IS THAT REGISTER
                                        ;WHICH GETS ITS DATA FROM THE ADDRESS BUS.

014400  011137  002342              MOV     (R1),R6LOAD              ;GET DATA LOADED INTO DIAG ADDRESS REG
014404  004737  006700              JSR     PC,READR6                ;READ FORCE JUMP ADDRESS ON EODAL BUS
014410  001405                      BEQ     16$                      ;IF FORCE JUMP ADDRESS REG OK THEN CONT
014412                              ERRDF   4,FEODAL,R06ERR          ;FORCE JUMP ADDRESS REG TO EODAL BUS FRR
014412  104455                      TRAP    C$ERDF
014414  000004                      .WORD   4
014416  003147                      .WORD   FEODAL
014420  005020                      .WORD   R06ERR
014422                              CKLOOP
014422  104406                      TRAP    C$CLP1

                                        ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL BITS 1
                                        ;AND 0 TO ZEROES.

014424  004737  006754          16$:   JSR     PC,SLHDAL                ;SELECT HDAL REG VIA GDAL BITS 2:0

                                        ;SET THE SIGNAL XCAS H WHICH IS PRESENTLY ASSERTED HIGH TO THE LOW
                                        ;STATE BY SETTING HDAL13 H TO A ZERO.

014430  012737  021004  002342      MOV     #HDAL13!HDAL9.HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
014436  004737  007442              JSR     PC,XCASL                 ;GO SET XCAS H TO THE LOW STATE
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                                        ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
                                        ;THIS IS DONE TO SIMULATE A MACHINE CYCLE.

014442  004737  007502                 JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H

                                        ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
                                        ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
                                        ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL
                                        ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
                                        ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
                                        ;AND RASP L WILL BE PULSED.
                                        ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO BY RASP L
                                        ;WHEN THE SIGNALS EP8N L AND PSMW H ARE ASSERTED HIGH AND EPFN L IS
                                        ;ASSERTED LOW.  A SHORT TIME AFTER RASP L, THE SIGNAL PSMW H WILL BE
                                        ;ASSERTED LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP BEING
                                        ;CLEARED.

014446  004737  007272                 JSR     PC,XRAS                 ;PULSE XRAS VIA THE SIGNAL HDAL12

                                        ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
                                        ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 0
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    16 BIT ADDRESS - EPFN H - 1

014452  042737  001000  002336          BIC     #VDAL9,R4GOOD           ;SETUP TO EXPECT PSMW H TO BE 0
014460  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
014464  001405                          BEQ     17$                     ;IF OK THEN CONTINUE
014466                                  ERRDF   3,VDALRG,R4EROR         ;PSMW H PROBABLY NOT ZEROED
014466  104455                          TRAP    C$ERDF
014470  000003                          .WORD   3
014472  002537                          .WORD   VDALRG
014474  005004                          .WORD   R4EROR
014476                                  CKLOOP
014476  104406                          TRAP    C$CLP1

                                        ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13.  THE SIGNAL
                                        ;XCAS H WILL CLOCK THE OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP INTO
                                        ;THE 16 BIT ADDRESS FLIP-FLOP, THUS CLEARING THE 16 BIT ADDRESS F/F.

014500  004737  007376          17$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H

                                        ;READ VDAL REGISTER AND CHECK PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
                                        ;THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
                                        ;   PAUSE STATE WORKING - PSMW H - 0
                                        ;   PAUSE STATE SYNC - EPSF H - 0
                                        ;   16 BIT ADDRESS - EPFN H - 0

014504  042737  004000  002336          BIC     #VDAL11,R4GOOD          ;SETUP TO EXPECT EPFN H TO BE 0
014512  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
014516  001405                          BEQ     18$                     ;IF OK THEN CONTINUE
014520                                  ERRDF   3,VDALRG,R4EROR         ;EPFN H PROBABLY NOT CLEARED
014520  104455                          TRAP    C$ERDF
014522  000003                          .WORD   3
014524  002537                          .WORD   VDALRG
014526  005004                          .WORD   R4EROR
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5687  014530                          CKLOOP
5688  014530  104406                  TRAP    C$CLP1
5689
5690                                  ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
5691                                  ;THIS IS DONE TO FINISH THE MACHINE CYCLE.
5692
5693  014532  004737  007502  18$:    JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
5694  014536                          ENDSEG
5695  014536                  10000$:
5696  014536  104405                  TRAP    C$ESEG
5697
5698  014540  005721                  TST     (R1)+                   ;UPDATE POINTER TO DIAG ADDRESS DATA TABLE
5699  014542  005302                  DEC     R2                      ;CHECK IF ALL PATTERNS HAVE BEEN LOADED
5700  014544  001410                  BEQ     20$                     ;IF YES THEN END OF TEST
5701  014546  000137  013676          JMP     1$                      ;IF NOT THEN LOAD NEXT PATTERN
5702
5703  014552  125252          19$:    .WORD   125252
5704  014554  052525                  .WORD   052525
5705  014556  177400                  .WORD   177400
5706  014560  000377                  .WORD   000377
5707  014562  177777                  .WORD   177777
5708  014564  000000                  .WORD   000000
5709
5710  014566                  20$:    ENDTST
5711  014566                  L10056:
5712  014566  104401                  TRAP    C$ETST
5713
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                                .SBTTL  TEST 29: PAUSE STATE MACHINE - 16 BIT ADDRESS - PAUSE MODE - NEW FJA

                                ;++
                                ; THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 16 BIT ADDRESS MODE.  THE
                                ; PAUSE  STATE  MACHINE  FLIP - FLOP'S , PAUSE  STATE  WORKING , PAUSE
                                ; STATE SYNC AND 16 BIT ADDRESS WILL BE CLOCKED TO ONES AND ZEROES BY PULSING
                                ; THE SIGNALS XRAS H AND XCAS H AND CHANGING THE LOGIC LEVEL ON THE SIGNAL
                                ; FETCT H.  THE SIGNALS ADAL4 H AND ADAL8 H WILL BE SET TO A ZERO ANT ADAL0 H
                                ; WILL BE SET TO A ONE DURING THIS TEST.  ADAL4 H ON A ZERO WILL PUT THE PAUSE
                                ; STATE MACHINE IN PAUSE MODE.  ADAL8 H ON A ZERO WIL' DISABLE THE TIMEOUT BREAK
                                ; SIGNAL FROM CAUSING A BREAK AND ADAL0 H ON A ONE WILL CLEAR THE BREAK LOGIC,
                                ; THUS SETTING THE SIGNAL BRK H TO A ZERO.
                                ;
                                ; THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE NEW
                                ; FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS.  THE NEW FORCE JUMP
                                ; ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA PATTERNS: 125252, 052525
                                ; 177400, 000377, 177777, AND 000000.  THE NEW FORCE JUMP ADDRFSS REGISTER IS
                                ; LOADED AT THE BEGINNING OF THE TEST.
                                ;--

014570                                  BGNTST
014570                          T29::
014570  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
014574  012701  015544                   MOV     #17$,R1                 ;GET ADDRESS OF DATA TABLE
014600  012702  000006                   MOV     #6,R2                   ;COUNTER FOR NUMBER OF DATA PATTERNS

014604                          '$:     BGNSEG
014604  104404                          TRAP    C$BSEG

                                ;SELECT THE MODE REGISTER BY SETTIPG GDAL2 TO A ONE AND GDAL1 AND GDAL0
                                ;TO A ZERO.

014606  004737  007006                   JSR     PC,SLMODR               ;GC SELECT MODE REG VIA CONTROL REG 0

                                ;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH ZEROES.  MR BIT 11
                                ;ON A ZERO WILL ENABLE 16 BIT ADDRESS SELECTION TO THE PAUSE STATE
                                ;MACHINE.

014612  005037  002342                   CLR     R6LOAD                  ;SETUP DATA TO BE ZERO
014616  004737  006672                   JSR     PC,LDRDR6               ;LOAD, READ AND CHECK MODE REGISTER
014622  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
014624                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO 0
014624  104455                          TRAP    C$ERDF
014626  000004                          .WORD   4
014630  002631                          .WORD   MODREG
014632  005020                          .WORD   R06ERR
014634                                  CKLOOP
014634  104406                          TRAP    C$CLP1

                                ;SET GDAL1 AND GDAL0 TO ONES IN THE GDAL REGISTER TO SELEC  THE HDAL
                                ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

014636  004737  006754          2$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2-0

                                ;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
                                ;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
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                                        ;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
                                        ;BUS.  HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
                                        ;TIMING AND CONTROL SIGNALS.

014642  012737  001004  002342          MOV     #HDAL9!HDAL2,R6LOAD     ;SETUP BITS TO BE LOADED
014650  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
014654  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
014656                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
014656  104455                          TRAP    C$ERDF
014660  000004                          .WORD   4
014662  002605                          .WORD   HDALRG
014664  005020                          .WORD   R06ERR
014666                                  CKLOOP
014666  104406                          TRAP    C$CLP1

                                        ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
                                        ;ZEROES.  ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
                                        ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.

014670  004737  007072          3$:     JSR     PC,SLDADR               ;GO SELECT DIAG. ADDRESS REG VIA GDAL 2:0

                                        ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA PATTERN
                                        ;OF 146314.  THE DIAGNOSTIC ADDRESS REGISTER IS WRITTEN WITH DATA TO
                                        ;CHECK THAT THE CORRECT FORCE JUMP ADDRESS IS ENABLED TO THE EODAL BUS
                                        ;WHEN THE 16 BIT ADDRESS FLIP-FLOP IS SET.  THE NEW FORCE JUMP ADDRESS
                                        ;REGISTER WILL BE ENABLED TO THE EODAL BUS IN THIS TEST.

014674  012737  146314  002342          MOV     #146314,R6LOAD          ;WRITE DIAG ADDRESS REG WITH 146314
014702  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD READ AND CHECK DIAG ADDRESS REG
014706  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
014710                                  ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDRESS REG NOT EQUAL EXPECTED
014710  104455                          TRAP    C$ERDF
014712  000004                          .WORD   4
014714  002735                          .WORD   ADDRRG
014716  005020                          .WORD   R06ERR
014720                                  CKLOOP
014720  104406                          TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK  ADAL REGISTER WITH A DATA PATTERN OF 000001.
                                        ;ADAL0 ON A ONE WILL HOLD THE BREAK LOGIC CLEARED.  ADAL4 ON A ZERO
                                        ;WILL CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE
                                        ;WHEN THE SIGNAL XRAS H IS PULSED.

014722  012737  000001  002330  4$:     MOV     #ADAL0,R2LOAD           ;SETUP BIT TO BE LOADED
014730  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REG
014734  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
014736                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL 1
014736  104455                          TRAP    C$ERDF
014740  000002                          .WORD   2
014742  002513                          .WORD   ADALRG
014744  004770                          .WORD   R2EROR
014746                                  CKLOOP
014746  104406                          TRAP    C$CLP1

                                        ;SET VDAL2 H TO A ONE AND THEN CLEAR VDAL2 H. VDAL2 H ON A ONE WILL
                                        ;CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS
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5826
5827  014750  005037  002334        5$:     CLR     R4LOAD                  ;CLEAR WORKING BITS FOR VDAL REG
5828  014754  004737  007712                JSR     PC,CLRPSM               ;SET VDAL2 H TO A 1 AND THEN 0
5829
5830                                        ;SELECT THE NEW FORCE JUMP ADDRESS REGISTER BY SETTING GDAL0 H TO A
5831                                        ;ONE AND GDAL BITS 1 AND 2 TO ZEORES.  ON A WRITE COMMAND TO CONTROL
5832                                        ;REGISTER 6, DATA WILL BE LOADED INTO THE NEW FORCE JUMP ADDRESS
5833                                        ;REGISTER  AND THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL BE SET
5834                                        ;TO A ONE.
5835
5836  014760  004737  007040                JSR     PC,SLFJAR               ;SELECT FORCE JUMP ADDRESS REG VIA GDAL
5837
5838                                        ;ISSUE A WRITE COMMAND TO CONTROL REGISTER 6 TO WRITE DATA INTO THE NEW
5839                                        ;FORCE JUMP ADDRESS REGISTER.  THE DATA WILL BE LOADED INTO THE NEW FORCE
5840                                        ;JUMP ADDRESS REGISTER VIA THE SIGNALS WPT1 LB H AND WPT1 HB H.  THE TAKE
5841                                        ;NEW FORCE JUMP ADDRESS FLIP-FLOP WILL ALSO BE CLOCKED TO A ONE BY THE
5842                                        ;SIGNAL WPT1 LB H.  THE DATA PATTERNS LOADED WILL BE ONE OF THE FOLLOW-
5843                                        ;ING: 125252, 052525, 177400, 000377, 177777, AND 000000.
5844
5845  014764  011177  165316                MOV     (R1),@REG6              ;WRITE NEW FORCE JUMP ADDRESS REGISTER
5846
5847                                        ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE (1).
5848                                        ;CHECK THAT THE SIGNAL WPT1 LB H CLOCKED THE TAKE NEW FORCE JUMP ADDRESS
5849                                        ;FLIP-FLOP TO A ONE.
5850
5851  014770  012737  000200  002334        MOV     #VDAL7,R4LOAD           ;SETUP BITS TO BE LOADED
5852  014776  013737  002334  002336        MOV     R'LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
5853  015004  052737  100000  002336        BIS     #VDAL15,R4GOOD          ;SETUP TO EXPECT TNFJ H FLIP-FLOP = 1
5854  015012  004737  006646                JSR     PC,LDRD4R               ;GO LOAD, READ AND CHECK VDAL REGISTER
5855  015016  001405                        BEQ     6$                      ;IF LOADED OK THEN CONTINUE
5856  015020                                ERRDF   3,VDALRG,R4EROR         ;TNFJ H PROBABLY NOT SET IN VDAL REG
5857  015020  104455                        TRAP    C$ERDF
5858  015022  000003                        .WORD   3
5859  015024  002537                        .WORD   VDALRG
5860  015026  005004                        .WORD   R4EROR
5861  015030                                CKLOOP
5862  015030  104406                        TRAP    C$CLP1
5863
5864                                        ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
5865                                        ;TO ONES.  BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
5866                                        ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L
5867
5868  015032  004737  006754        6$:     JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL 2:0
5869
5870                                        ;SET HDAL12 H TO A ONE TO SET THE SIGNALS XRAS H AND XRAS L TO THE
5871                                        ;HIGH AND LOW STATE RESPECTIVELY.  THEY WILL REMAIN SET TO THESE STATES
5872                                        ;UNTIL THE PROGRAM HAS PULSED THE SIGNALS XPI H AND XPI L.
5873                                        ;
5874                                        ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
5875                                        ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
5876                                        ;HIGH STATE.  THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
5877                                        ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
5878                                        ;TO THE HIGH STATE.  THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
5879                                        ;SIGNAL PAUSE L IS ASSERTED HIGH.  WHEN SOP H AND EDFET H ARE ASSERTED
5880                                        ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
5881                                        ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
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                                        ;PSMW H WILL BE ASSERTED HIGH.  THE SIGNAL PSMW H IS READ IN THE VDAL
                                        ;REGISTER AS VDAL9 H.  WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
                                        ;SIGNAL PB H WILL BE ASSERTED HIGH.  THE SIGNAL PB H IS THE DATA INPUT
                                        ;LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
                                        ;
                                        ;THE SIGNAL XRAS H WILL CAUSE THE SIGNAL RASP H TO BE PULSED.  WHEN THE
                                        ;SIGNAL RASP H IS PULSED AND THE SIGNAL EDFET H IS ASSERTED HIGH, A
                                        ;PULSE WILL BE ISSUED ON THE SIGNAL DFET H.  THE SIGNAL DFET H WILL
                                        ;CLOCK THE ADDRESS BUS INTO THE OLD FORCE JUMP ADDRESS REGISTER.  AT THE
                                        ;PRESENT TIME THE DIAGNOSTIC ADDRESS REGISTER IS ENABLED ONTO THE
                                        ;ADDRESS BUS, THEREFORE THE OLD FORCE JUMP ADDRESS REGISTER WILL BE
                                        ;LOADED WITH THE DATA FROM THE DIAGNOSTIC ADDRESS REGISTER.

015036  012737  001004  002342          MOV     #HDAL9!HDAL2,R6LOAD     ;BITS PREVIOUSLY SET IN HDAL REG
015044  004737  007304                  JSR     PC,XRASH                ;SET XRAS H HIGH AND XRAS L LOW VIA HDAL12

                                        ;CLEAR VDAL7 H IN THE VDAL REGISTER THUS SETTING THE SIGNAL FETCT H TO
                                        ;THE LOW STATE.  CHECK THE PAUSE STATE MACHINE TO BE IN THE FOLLOWING
                                        ;STATE AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.  THE "TAKE
                                        ;NEW FORCE JUMP ADDRESS" FLIP-FLOP WAS SET TO A ONE EARLIER WHEN THE
                                        ;NEW FORCE JUMP ADDRESS REGISTER WAS LOADED WITH THE DATA PATTERN.
                                        ;       PAUSE STATE WORKING - PSMW H - 1
                                        ;       PAUSE STATE SYNC - EPSF H - 0
                                        ;       16 BIT ADDRESS - EPFN H - 0
                                        ;       TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;       GET NEW ADDRESS - OUTNEW H - 0

015050  042737  000200  002334          BIC     #VDAL7,R4LOAD           ;SETUP TO CLEAR FETCT H
015056  013737  002334  002336          MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
015064  052737  101000  002336          BIS     #VDAL15!VDAL9,R4GOOD     ;EXPECT PSMW H AND TNFJ H TO BE SET
015072  004737  006646                  JSR     PC,LDRD4R               ;GO LOAD, READ AND CHECK VDAL REGISTER
015076  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
015100                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
015100  104455                          TRAP    C$ERDF
015102  000003                          .WORD   3
015104  002537                          .WORD   VDALRG
015106  005004                          .WORD   R4EROR
015110                                  CKLOOP
015110  104406                          TRAP    C$CLP1

                                        ;THE SIGNALS XRAS H AND XRAS L ARE STILL ASSERTED TO THE HIGH AND LOW
                                        ;STATE RESPECTIVELY BY HDAL12 H BEING SET TO A ONE.  THEY WILL REMAIN
                                        ;SET TO THESE STATES UNTIL THE SIGNALS XPI H AND XPI L HAVE BEEN PULSED
                                        ;
                                        ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
                                        ;SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
                                        ;SIGNAL "PB H", WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
                                        ;SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE.  THE SIGNAL XCAS H
                                        ;WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-FLOP (0)
                                        ;INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE 16 BIT ADDRESS
                                        ;FLIP-FLOP TO A ZERO.

015112  004737  007410          7$:     JSR     PC,XCASH                ;ASSERT XCAS H TO HIGH STATE

                                        ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                        ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING SET TO 1.
```

```
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    16 BIT ADDRESS - EPFN H - 0
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;    GET NEW ADDRESS - OUTNEW H - C

015116  052737  002000  002336          BIS     #VDAL10,R4GOOD          ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
015124  004737  006654                  JSR     PC,READR4               ;GO READ AND CHECK PAUSE STATE MACHINE
015130  001405                          BEQ     8$                      ;IF LOADED OK THEN CONTINUE
015132                                  ERRDF   3,VDALRG,R4EROR         ;EPSF H PROBABLE NOT SET IN VDAL REG
015132  104455                          TRAP    C$ERDF
015134  000003                          .WORD   3
015136  002537                          .WORD   VDALRG
015140  005004                          .WORD   R4EROR
015142                                  CKLOOP
015142  104406                          TRAP    C$CLP1

                                        ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE 16 BIT
                                        ;INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE EODAL BUS AT THIS TIME.
                                        ;ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE ENABLED
                                        ;TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.

015144  004737  007122          8$:     JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0

                                        ;THE SIGNAL ACAS H WILL BE ASSERTED HIGH AS A RESULT OF THE SIGNAL
                                        ;XCAS H BEING ASSERTED HIGH AND THE SIGNAL PSMW H BEING ASSERTED HIGH.
                                        ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH AND THE PAUSE STATE SYNC FLIP-
                                        ;FLOP IS SET TO A ONE, THE SIGNALS EDRL L AND EDRH L WILL BE ASSERTED
                                        ;LOW.  THESE TWO SIGNALS WILL ENABLE THE 16 BIT INSTRUCTION REGISTER
                                        ;ONTO THE EODAL BUS.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER
                                        ;6 WITH GDAL BITS 2:0 SET TO ONES, A PULSE WILL BE ISSUED ON THE SIGNAL
                                        ;RPT7 L.  THE SIGNAL RPT7 L WILL READBACK THE 16 BIT INSTRUCTION REGIS-
                                        ;TER WHICH IS ENABLED TO THE EODAL BUS AT THIS POINT IN TIME.

015150  012737  000137  002342          MOV     #137,R6LOAD             ;SETUP EXPECTED 16 BIT INSTRUCTION (JMP)
015156  004737  006700                  JSR     PC,READR6               ;READ 16 BIT INSTRUCTION REG ON EODAL BUS
015162  001405                          BEQ     9$                      ;IF INSTRUCTION EQUALS "JMP" THEN CONT
015164                                  ERRDF   4,IEODAL,R06ERR         ;EODAL BUS ERROR, OR 16 BIT INSTRUCTION
015164  104455                          TRAP    C$ERDF
015166  000004                          .WORD   4
015170  003034                          .WORD   IEUDAL
015172  005020                          .WORD   R06ERR
                                                                        ;REGISTER ERROR, OR 16 BIT INSTRUCTION
                                                                        ;REGISTER NOT ENABLED TO THE BUS
015174                                  CKLOOP
015174  104406                          TRAP    C$CLP1

                                        ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND
                                        ;GDAL0 TO ONES

015176  004737  006754          9$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0

                                        ;SET THE SIGNAL XCAS H TO A ZERO BY CLEARING HDAL13 H IN HDAL REGISTER
                                        ;
                                        ;THE SIGNALS XRAS H AND XRAS L WILL REMAIN ASSERTED TO THE HIGH AND LOW
                                        ;STATE RESPECTIVELY BY HDAL'  H BEING SET TO A ONE.  THEY WILL NOT BE
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                                        ;DEASSERTED UNTIL PULSES HAVE BEEN ISSUED ON XPI H AND XPI L.
                                        ;
015202  012737  031004  002342          MOV     #HDAL13!HDAL12!HDAL9!HDAL2,R6LOAD ;BITS PREVIOUSLY LOADED IN HDAL
015210  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO THE LOW STATE
                                        ;
                                        ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
                                        ;THIS IS DONE TO SIMULATE A MACHINE CYCLE.
                                        ;
015214  004737  007502                  JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
                                        ;
                                        ;READ THE VDAL REGISTER AGAIN TO CHECK THAT THE ''TAKE NEW FORCE JUMP
                                        ;ADDRESS '' FLIP-FLOP IS STILL SET.  IT SHOULD NOT CLEAR UNTIL THE
                                        ;NEXT XCAS H PULSE.  THE PAUSE STATE MACHINE FLIP-FLOPS SHOULD REMAIN
                                        ;UNCHANGED AFTER XPI H AND XPI L WERE PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    16 BIT ADDRESS - EPFN H - 0
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;    GET NEW ADDRESS - OUTNEW H - 0
                                        ;
015220  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
015224  001405                          BEQ     10$                     ;IF OK THEN CONTINUE
015226                                  ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE MACHINE CHANGED AFTER XPI
015226  104455                          TRAP    C$ERDF
015230  000003                          .WORD   3
015232  002537                          .WORD   VDALRG
015234  005004                          .WORD   R4EROR
015236                                  CKLOOP
015236  104406                          TRAP    C$CLP1
                                        ;
                                        ;SET THE SIGNALS XRAS H AND XRAS L TO THERE DE-ASSERTED STATE BY CLEARING
                                        ;HDAL12 H IN THE HDAL REGISTER.  WHEN XRAS L IS RETURNED TO THE HIGH
                                        ;STATE, THE ''GET NEW ADDRESS'' FLIP-FLOP WILL BE CLOCKED TO A ONE AS A
                                        ;RESULT OF THE ''TAKE NEW FORCE JUMP ADDRESS'' FLIP-FLOP BEING SET AND THE
                                        ;''PAUSE STATE SYNC'' FLIP-FLOP BEING SET.  WHEN THE ''GET NEW ADDRESS'' FLIP-
                                        ;FLOP IS SET, THE SIGNAL ''OUTNEW H'' WILL BE ASSERTED HIGH.  THE OUTNEW H
                                        ;SIGNAL IS READ IN THE VDAL REGISTER AS VDAL BIT 8
                                        ;
015240  004737  007336          10$:    JSR     PC,XRASL                ;SET XRAS H LOW AND XRAS L HIGH VIA HDAL12
                                        ;
                                        ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
                                        ;BE IN THE FOLLOWING STATE.  THE ''GET NEW ADDRESS'' FLIP-FLOP SHOULD HAVE
                                        ;BEEN SET TO A ONE WHEN XRAS L WAS RETURNED TO THE HIGH STATE. THE
                                        ;''GET NEW ADDRESS'' FLIP-FLOP WAS CLOCKED TO A ONE BY XRAS L WHEN THE
                                        ;''TAKE NEW FORCE JUMP ADDRESS'' FLIP-FLOP AND THE ''PAUSE STATE SYNC''
                                        ;FLIP-FLOP WERE SET TO A ONE.
                                        ;    PAUSE STATE WORKING - PSMH H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    16 BIT ADDRESS - EPFN H - 0
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;    GET NEW ADDRESS - OUTNEW H - 1
                                        ;
015244  052737  000400  002336          BIS     #VDAL8,R4GOOD           ;EXPECT OUTNEW H TO BE A ONE
015252  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
015256  001405                          BEQ     11$                     ;IF OK THEN CONTINUE
015260                                  ERRDF   3,VDALRG,R4EROR         ;OUTNEW H PROBABLY NOT SET TO A ONE
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                                        TRAP    C$ERDF
                                        .WORD   3
                                        .WORD   VDALRG
                                        .WORD   R4EROR
                                        CKLOOP
                                        TRAP    C$C_P1

                                        ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
                                        ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
                                        ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
                                        ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
                                        ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
                                        ;AND RASP L WILL BE PULSED.
                                        ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
                                        ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.

015272  004737  007272        11$:    JSR     PC,XRAS                 ;GO PULSE XRAS H BY HDAL12

                                        ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
                                        ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    16 BIT ADDRESS - EPFN H - 0
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;    GET NEW ADDRESS - OUTNEW H - 1

015276  004737  006654                  JSR     PC,READR4               ;CHECK VDAL AND PAUSE STATE MACHINE
015302  001405                          BEQ     12$                     ;IF OK THEN CONTINUE
015304                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
015304  104455                          TRAP    C$ERDF
015306  000003                          .WORD   3
015310  002537                          .WORD   VDALRG
015312  005004                          .WORD   R4EROR
015314                                  CKLOOP
015314  104406                          TRAP    C$CLP1

                                        ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
                                        ;SIGNAL XCAS H GOING FROM A 0 TO A 1 WILL CLOCK THE LEVEL OF THE
                                        ;SIGNAL  "PB H" , WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP,
                                        ;THUS CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO.  THE SIGNAL
                                        ;XCAS H WILL ALSO CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC
                                        ;FLIP-FLOP (1) INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE
                                        ;16 BIT ADDRESS FLIP-FLOP TO A ONE.
                                        ;
                                        ;THE SIGNAL XCAS H WILL ALSO CAUSE THE "TAKE NEW FORCE JUMP ADDRESS"
                                        ;FLIP-FLOP TO BE CLEARED WHEN THE "GET NEW ADDRESS" FLIP-FLOP IS SET
                                        ;TO A ONE.

015316  004737  007410        12$:    JSR     PC,XCASH                ;ASSERT XCAS H TO THE HIGH STATE

                                        ;READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
                                        ;FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING A 1.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    16 BIT ADDRESS - EPFN H - 1
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 0
```

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                                        ;    GET NEW ADDRESS - OUTNEW H - 1
                                        ;
015322  042737  102000  002336          BIC     #VDAL15!VDAL10,R4GOOD   ;CLEAR BITS FOR EPSF H AND TNFJ H
015330  052737  004000  002336          BIS     #VDAL11,R4GOOD          ;SET BIT FOR EPFN H
015336  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
015342  001405                          BEQ     13$                     ;IF OK THEN CONTINUE
015344                                  ERRDF   3,VDALRG,R4EROR         ;EPFN H PROBABLY NOT SET IN VDAL REG
015344  104455                          TRAP    C$ERDF
015346  000003                          .WORD   3
015350  002537                          .WORD   VDALRG
015352  005004                          .WORD   R4EROR
015354                                  CKLOOP
015354  104406                          TRAP    C$CLP1
                                        ;
                                        ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE NEW FORCE
                                        ;JUMP ADDRESS REGISTER SHOULD BE ENABLED ON THE EODAL BUS AT THIS TIME.
                                        ;ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ
                                        ;BACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
                                        ;
015356  004737  007122          13$:    JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
                                        ;
                                        ;AT THIS POINT IN TIME, THE NEW FORCE JUMP ADDRESS REGISTER WILL BE
                                        ;ENABLED TO THE EODAL BUS VIA THE SIGNALS NEARH L AND NEARL L.  THESE
                                        ;SIGNALS ARE ASSERTED LOW AS A RESULT OF THE "GET NEW ADDRESS"
                                        ;FLIP-FLOP BEING SET AND THE SIGNALS EARH H AND EARL H BEING
                                        ;ASSERTED HIGH.  THE "GET NEW ADDRESS" FLIP-FLOP WAS SET WHEN
                                        ;THE PAUSE STATE SYNC FLIP-FLOP WAS A ONE, A PULSE WAS ISSUED ON
                                        ;XRAS L, AND THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WAS SET TO A ONE.
                                        ;THE SIGNAL EARH H AND EARL H ARE ASSERTED HIGH AS A RESULT OF 16 BIT
                                        ;ADDRESS FLIP-FLOP BEING SET TO A ONE, THE SIGNAL ACAS H ASSERTED HIGH,
                                        ;AND MODE REGISTER BIT 11 SET TO A ZERO FOR 16 BIT ADDRESS MODE.  THE
                                        ;FOLLOWING SECTION WILL READ THE EODAL BUS VIA THE SIGNAL RPT7 L AND
                                        ;CHECK THAT THE NEW FORCE JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL
                                        ;BUS.  THE NEW FORCE JUMP ADDRESS REGISTER WAS WRITTEN AT THE BEGINNING
                                        ;OF THIS TEST VIA THE SIGNALS WPT1 LB H AND WPT1 HB H.
                                        ;
                                        ;IF THE ADDRESS READ FROM THE FORCE JUMP ADDRESS REGISTER EQUALS 146314,
                                        ;THEN THE WRONG FORCE JUMP ADDRESS REGISTER WAS READ.  THE DATA PATTERN
                                        ;146314 WAS WRITTEN INTO THE OLD FORCE JUMP ADDRESS REGISTER VIA THE
                                        ;SIGNAL DFET H AND THE DIAGNOSTIC ADDRESS REGISTER.  CHECK THE "GET
                                        ;NEW ADDRESS" FLIP-FLOP TO BE SET TO A ONE AND CHECK THE NEW FORCE
                                        ;JUMP ADDRESS SELECTION LOGIC.
                                        ;
015362  011137  002342                  MOV     (R1),R6LOAD             ;GET DATA LOADED INTO NEW FJA REG
015366  004737  006700                  JSR     PC,READR6               ;READ NEW FORCE JUMP ADDRESS ON EODAL BUS
015372  001405                          BEQ     14$                     ;IF FORCE JUMP ADDRESS REG OK THEN CONT
015374                                  ERRDF   4,FEODAL,R06ERR         ;NEW FORCE JUMP ADDRESS REG TO EODAL BUS ERR
015374  104455                          TRAP    C$ERDF
015376  000004                          .WORD   4
015400  003147                          .WORD   FEODAL
015402  005020                          .WORD   R06ERR
015404                                  CKLOOP
015404  104406                          TRAP    C$CLP1
                                        ;
                                        ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL BITS 1
                                        ;AND 0 TO ZEROES.
```

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6162
6163  015406  004737  006754          14$:    JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
6164
6165                                          ;SET THE SIGNAL XCAS H, WHICH IS PRESENTLY SET HIGH, TO THE LOW STATE BY
6166                                          ;SETTING HDAL13 H TO A ZERO.
6167
6168  015412  012737  021004  002342          MOV     #HDAL13.HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
6169  015420  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO THE LOW STATE
6170
6171                                          ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
6172                                          ;THIS IS DONE TO SIMULATE A MACHINE CYCLE.
6173
6174  015424  004737  007502                  JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
6175
6176                                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
6177                                          ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
6178                                          ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL
6179                                          ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
6180                                          ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
6181                                          ;AND RASP L WILL BE PULSED.
6182                                          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO BY RASP L
6183                                          ;WHEN THE SIGNALS EP8N L AND PSMW H ARE ASSERTED HIGH AND EPFN L IS
6184                                          ;ASSERTED LOW.  A SHORT TIME AFTER RASP L, THE SIGNAL PSMW H WILL BE
6185                                          ;ASSERTED LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP BEING
6186                                          ;CLEARED.
6187
6188  015430  004737  007272                  JSR     PC,XRAS                 ;PULSE XRAS VIA THE SIGNAL HDAL12
6189
6190                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
6191                                          ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
6192                                          ;    PAUSE STATE WORKING - PSMW H - 0
6193                                          ;    PAUSE STATE SYNC - EPSF H - 0
6194                                          ;    16 BIT ADDRESS - EPFN H - 1
6195                                          ;    TAKE NEW FJ ADDRESS - TNFJ H - 0
6196                                          ;    GET NEW ADDRESS - OUTNEW H - 1
6197
6198  015434  042737  001000  002336          BIC     #VDAL9,R4GOOD           ;SETUP TO EXPECT PSMW H TO BE 0
6199  015442  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
6200  015446  001405                          BEQ     15$                     ;IF OK THEN CONTINUE
6201  015450                                  ERRDF   3,VDALRG,R4EROR         ;PSMW H PROBABLY NOT 0'ED BY CLPS H
6202  015450  104455                          TRAP    C$ERDF
6203  015452  000003                          .WORD   3
6204  015454  002537                          .WORD   VDALRG
6205  015456  005004                          .WORD   R4EROR
6206  015460                                  CKLOOP
6207  015460  104406                          TRAP    C$CLP1
6208
6209                                          ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13.  THE SIGNAL
6210                                          ;XCAS H WILL CLOCK THE OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP INTO
6211                                          ;THE 16 BIT ADDRESS FLIP-FLOP, THUS CLEARING THE 16 BIT ADDRESS F/F.
6212
6213  015462  004737  007376          15$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
6214
6215                                          ;READ VDAL REGISTER AND CHECK PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
6216                                          ;THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
6217                                          ;   PAUSE STATE WORKING - PSMW H - 0
```

```
                                        ;   PAUSE STATE SYNC - EPSF H - 0
                                        ;   16 BIT ADDRESS - EPFN H - 0
                                        ;   TAKE NEW FJ ADDRESS - TNFJ H - 0
                                        ;   GET NEW ADDRESS - OUTNEW H - 1

015466  042737  004000  002336        BIC     #VDAL11,R4GOOD          ;SETUP TO EXPECT EPFN H TO BE 0
015474  004737  006654                JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
015500  001405                        BEQ     16$                     ;IF OK THEN CONTINUE
015502                                ERRDF   3,VDALRG,R4EROR         ;EPFN H PROBABLY NOT CLEARED
015502  104455                        TRAP    C$ERDF
015504  000003                        .WORD   3
015506  002537                        .WORD   VDALRG
015510  005004                        .WORD   R4EROR
015512                                CKLOOP
015512  104406                        TRAP    C$CLP1

                                        ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
                                        ;THIS IS DONE TO FINISH THE MACHINE CYCLE.

015514  004737  007502        16$:    JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H

                                        ;TO CHECK THAT THE "GET NEW ADDRESS" FLIP-FLOP CAN BE CLEARED, THE
                                        ;PROGRAM WILL SET VDAL2 H TO A ONE AND THEN A ZERO.  THE "GET NEW
                                        ;ADDRESS" FLIP-FLOP WILL BE CLEARED  WHEN VDAL2 H IS SET TO A ONE.

015520  005037  002334                CLR     R4LOAD                  ;CLEAR WORKING BITS FOR VDAL REG
015524  004737  007712                JSR     PC,CLRPSM               ;SET VDAL2 H TO A 1 AND THEN 0

015530                                ENDSEG
015530                          10000$:
015530  104405                        TRAP    C$ESEG

015532  005721                        TST     (R1)+                   ;UPDATE POINTER TO DIAG ADDRESS DATA TABLE
015534  005302                        DEC     R2                      ;CHECK IF ALL PATTERNS HAVE BEEN LOADED
015536  001410                        BEQ     18$                     ;IF YES THEN END OF TEST
015540  000137  014604                JMP     1$                      ;IF NOT THEN LOAD NEXT PATTERN

015544  125252          17$:          .WORD   125252
015546  052525                        .WORD   052525
015550  177400                        .WORD   177400
015552  000377                        .WORD   000377
015554  177777                        .WORD   177777
015556  000000                        .WORD   000000

015560                          18$:    ENDTST
015560                          L10057:
015560  104401                        TRAP    C$ETST
```

```
                                .SBTTL  TEST 30: CHECK TIMEOUT BREAK ONE SHOT IN RUN MODE

                                ;++
                                ; THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN "RUN" AND 16 BIT ADDRESS MODE.
                                ; WHEN THE PAUSE STATE MACHINE IS SETUP IN "RUN" MODE VIA ADAL4 H ON A ONE AND
                                ; A PULSE ON THE SIGNAL XRAS H, THE PAUSE STATE MACHINE CAN ONLY BE ENTERED WHEN
                                ; A BREAK CONDTION IS RECEIVED ON THE SIGNAL 'BRK H".  THIS TEST WILL USE THE
                                ; TIMEOUT BREAK ONE SHOT TO GENERATE THE BREAK CONDITION.  THE TEST WILL CHECK
                                ; THAT THE PAUSE STATE MACHINE IS NOT ENTERED WHEN NO BREAK CONDITION IS RECEIVED
                                ; AND THAT IT IS ENTERED WHEN A BREAK CONDITION IS RECEIVED.  THE TEST WILL CHECK
                                ; ALL THE PAUSE STATE LOGIC ASSOCIATED WITH THE SIGNAL 'BRK H".  THE TEST WILL
                                ; CHECK THAT THE SIGNAL "TOBRK H" IS SET IN CONTROL REGISTER 0 WHEN THE TIME OUT
                                ; BREAK ONE SHOT IS NOT BEING FIRED AND THAT IT IS NOT SET WHEN THE TIME OUT
                                ; BREAK ONE SHOT IS BEING FIRED.
                                ;--

015562                                  BGNTST
015562                          T30::
015562  004737  005510                    JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

015566                                  BGNSEG
015566  104404                          TRAP    C$BSEG

                                ;SELECT MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

015570  004737  007006                JSR     PC,SLMODR               ;SELECT MODE REGISTER VIA GDAL BITS 2:0

                                ;CLEAR ALL BITS IN THE MODE REGISTER.  MODE REGISTER BIT 11 ON A ZERO
                                ;WILL SELECT 16 BIT ADDRESS MODE FOR THE PAUSE STATE MACHINE.

015574  005037  002342                CLR     R6LOAD                  ;SETUP TO CLEAR ALL BITS
015600  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
015604  001405                        BEQ     1$                      ;IF LOADED OK THEN CONTINUE
015606                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
015606  104455                          TRAP    C$ERDF
015610  000004                          .WORD   4
015612  002631                          .WORD   MODREG
015614  005020                          .WORD   R06ERR
015616                                  CKLOOP
015616  104406                          TRAP    C$CLP1

                                ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

015620  004737  006754          1$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0

                                ;SET HDAL REGISTER BIT 2 TO A ONE AND ALL OTHER HDAL REGISTER BITS TO A
                                ;ZERO.  WHEN HDAL2 H IS SET TO A ONE, THE PROGRAM CAN GENERATE THE T-11
                                ;TIMING AND CONTROL SIGNALS.

015624  012737  000004  002342        MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
015632  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
015636  001405                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
015640                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
015640  104455                          TRAP    C$ERDF
015642  000004                          .WORD   4
015644  002605                          .WORD   HDALRG
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6322  015646  005020                          .WORD   R06ERR
6323  015650                                  CKLOOP
6324  015650  104406                          TRAP    C$CLP1
6325
6326                                          ;SET ADAL REGISTER BIT 4 TO A ONE AND ALL OTHER ADAL REGISTER BITS TO A
6327                                          ;ZERO.  WHEN A PULSE IS ISSUED ON XRAS H AND ADAL4 H IS SET TO A ONE,
6328                                          ;THE PAUSE MODE FLIP-FLOP WILL BE CLOCKED TO THE RUN MODE.  WHEN THE
6329                                          ;PAUSE MODE FLIP-FLOP IS SET TO THE RUN MODE, THE SIGNAL PAUSE L WILL
6330                                          ;BE ASSERTED LOW.  ADAL8 H ON A ZERO WILL CAUSE THE SIGNAL TOBRK H TO
6331                                          ;BE ASSERTED LOW.  WHEN THE SIGNAL TOBRK H IS ASSERTED LOW, THE SIGNAL
6332                                          ;BRK H WILL ALSO BE ASSERTED LOW.
6333
6334  015652  012737  000020  002330  2$:     MOV     #ADAL4,R2LOAD           ;SETUP BIT TO BE LOADED
6335  015660  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
6336  015664  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
6337  015666                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
6338  015666  104455                          TRAP    C$ERDF
6339  015670  000002                          .WORD   2
6340  015672  002513                          .WORD   ADALRG
6341  015674  004770                          .WORD   R2EROR
6342  015676                                  CKLOOP
6343  015676  104406                          TRAP    C$CLP1
6344
6345                                          ;TOGGLE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL2 H IN THE VDAL
6346                                          ;REGISTER.  A PULSE ON INVD L WILL CLEAR ALL THE FLIP-FLOPS ON THE
6347                                          ;MODULE EXCEPT THE SINGLE STEP BREAK FLIP-FLOP AND THE MEMORY SIMULATOR
6348                                          ;BREAK FLIP-FLOP.  A PULSE ON INVD L WILL ALSO SET THE PAUSE MODE FLIP-
6349                                          ;FLOP TO THE RUN MODE, THUS ASSERTING THE SIGNAL PAUSE L TO THE LOW STATE.
6350                                          ;A PULSE ON INVD L WILL ALSO RESET THE TIMEOUT BREAK ONE-SHOT.
6351
6352  015700  005037  002334          3$:     CLR     R4LOAD                  ;SETUP TO CLEAR VDAL R/W BITS
6353  015704  004737  007712                  JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
6354
6355                                          ;SET ADAL REGISTER BIT 8 TO A ONE.  ADAL8 H ON A ONE WILL ENABLE THE
6356                                          ;SIGNAL TOBRK H TO CONTROL REGISTER 0 AND TO THE BRK H LOGIC.  AT THIS
6357                                          ;POINT IN TIME, THE TIMEOUT BREAK ONE SHOT HAS NOT BEEN FIRED BY THE
6358                                          ;SIGNAL DFET H, THEREFORE, THE SIGNAL TOBRK H WILL BE ASSERTED HIGH
6359                                          ;WHEN ADAL8 H IS ASSERTED HIGH (1).  WHEN THE SIGNAL TOBRK H IS ASSERTED
6360                                          ;HIGH, THE SIGNAL BRK H WILL ALSO BE ASSERTED HIGH.
6361
6362  015710  052737  000400  002330          BIS     #ADAL8,R2LOAD           ;SETUP BIT TO BE LOADED
6363  015716  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
6364  015722  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
6365  015724                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
6366  015724  104455                          TRAP    C$ERDF
6367  015726  000002                          .WORD   2
6368  015730  002513                          .WORD   ADALRG
6369  015732  004770                          .WORD   R2EROR
6370  015734                                  CKLOOP
6371  015734  104406                          TRAP    C$CLP1
6372
6373                                          ;READ CONTROL REGISTER 0 AND CHECK THAT THE SIGNAL TOBRK H IS SET TO
6374                                          ;A ONE WHEN THE ONE SHOT HAS NOT BEEN FIRED AND THE SIGNAL ADAL8 H IS
6375                                          ;ASSERTED HIGH.
6376
6377  015736  052737  000100  002322  4$:     BIS     #TOBRK,R0GOOD           ;EXPECT TOBRK H TO BE A ONE
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6378  015744  004737  006570          JSR     PC,READR0               ;READ AND CHECK GDAL REGISTER
6379  015750  001405                  BEQ     5$                      ;IF OK THEN CONTINUE
6380  015752                          ERRDF   1,GDALRG,ROEROR         ;TOBRK H PROBABLY NOT A ONE
6381  015752  104455                  TRAP    C$ERDF
6382  015754  000001                  .WORD   1
6383  015756  002406                  .WORD   GDALRG
6384  015760  004754                  .WORD   ROEROR
6385  015762                          CKLOOP
6386  015762  104406                  TRAP    C$CLP1
6387
6388                                  ;READ THE VDAL REGISTER AND CHECK THAT THE PAUSE STATE MACHINE FLIP-
6389                                  ;FLOPS DID NOT CHANGE STATE WHEN THE SIGNALS TOBRK H AND BRK H WERE
6390                                  ;ASSERTED HIGH.
6391
6392  015764  004737  006654  5$:     JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
6393  015770  001405                  BEQ     6$                      ;IF OK THEN CONTINUE
6394  015772                          ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
6395  015772  104455                  TRAP    C$ERDF
6396  015774  000003                  .WORD   3
6397  015776  002537                  .WORD   VDALRG
6398  016000  005004                  .WORD   R4EROR
6399  016002                          CKLOOP
6400  016002  104406                  TRAP    C$CLP1
6401
6402                                  ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  WHEN
6403                                  ;XRAS H IS PULSED AND FETCT H IS ASSERTED LOW, THE EDFET FLIP-FLOP
6404                                  ;AND THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO.
6405                                  ;WHEN EDFET FLIP-FLOP IS CLEARED AND A PULSE IS ISSUED ON RASP H,
6406                                  ;NO PULSE SHOULD OCCUR ON THE SIGNAL DFET H.  A PULSE ON XRAS H
6407                                  ;CAUSES THE SIGNAL RASP H TO BE PULSED.  IF NO PULSE OCCURS ON THE
6408                                  ;SIGNAL DFET H, THE TIMEOUT ONE SHOT WILL REMAIN UNFIRED AND THE
6409                                  ;SIGNAL TOBRK H WILL REMAIN HIGH.  THE PAUSE MODE FLIP-FLOP WILL
6410                                  ;BE CLOCKED TO THE RUN MODE BY XRAS H AS A RESULT OF ADAL4 H BEING
6411                                  ;ASSERTED HIGH (1).  WHEN THE PAUSE MODE ONE SHOT IS SET TO RUN
6412                                  ;MODE, THE SIGNAL PAUSE L WILL BE ASSERTED LOW.
6413
6414  016004  004737  007272  6$:     JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
6415
6416                                  ;READ CONTROL REGISTER 0 TO CHECK THAT THE SIGNAL TOBRK H IS STILL
6417                                  ;SET TO A ONE AFTER A PULSE WAS ISSUED ON XRAS H AND THE EDFET FLIP-
6418                                  ;FLOP WAS CLOCKED TO A ZERO.  THE TIMEOUT BREAK ONE SHOT SHOULD NOT
6419                                  ;BE FIRED BY THE SIGNAL DFET H WHEN THE EDFET FLIP-FLOP IS CLEARED.
6420
6421  016010  004737  006570          JSR     PC,READR0               ;READ AND CHECK GDAL REGISTER
6422  016014  001405                  BEQ     7$                      ;IF OK THEN CONTINUE
6423  016016                          ERRDF   1,GDALRG,ROEROR         ;TOBRK ONE SHOT PROBAB   FIRED
6424  016016  104455                  TRAP    C$ERDF
6425  016020  000001                  .WORD   1
6426  016022  002406                  .WORD   GDALRG
6427  016024  004754                  .WORD   ROEROR
6428  016026                          CKLOOP
6429  016026  104406                  TRAP    C$CLP1
6430
6431                                  ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP
6432                                  ;DID NOT GET SET TO A ONE WHEN THE EDFET FLIP-FLOP IS CLEARED AND THE
6433                                  ;BRK H SIGNAL IS ASSERTED HIGH.  JUST AS A NOTE, THE SIGNAL PAUSE L
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                                        ;SHOULD BE ASSERTED LOW.
                                        ;
016030  004737  006654          7$:   JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
016034  001405                        BEQ     8$                      ;IF OK THEN CONTINUE
016036                                ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
016036  104455                        TRAP    C$ERDF
016040  000003                        .WORD   3
016042  002537                        .WORD   VDALRG
016044  005004                        .WORD   R4EROR
016046                                CKLOOP
016046  104406                        TRAP    C$CLP1
                                        ;
                                        ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  A PULSE
                                        ;ON XCAS H WILL CLOCK THE LEVEL OF THE SIGNAL PB H, WHICH SHOULD BE
                                        ;LOW AS A RESULT OF EDFET H BEING ASSERTED LOW, INTO THE PAUSE STATE
                                        ;SYNC FLIP-FLOP, THUS SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A
                                        ;ZERO.
                                        ;
016050  004737  007376          8$:   JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
                                        ;
                                        ;READ CONTROL REGISTER 0 TO CHECK THAT A PULSE ON XCAS H DID NOT
                                        ;CAUSE THE TIME OUT BREAK ONE SHOT TO BE FIRED.  THIS CONDITION SHOULD
                                        ;NEVER EXISTS.
                                        ;
016054  004737  006570                JSR     PC,READR0               ;READ AND CHECK GDAL REGISTER
016060  001405                        BEQ     9$                      ;IF NO CHANGES THEN CONTINUE
016062                                ERRDF   1,GDALRG,R0EROR         ;TIMEOUT BREAK ONE SHOT FIRED
016062  104455                        TRAP    C$ERDF
016064  000001                        .WORD   1
016066  002406                        .WORD   GDALRG
016070  004754                        .WORD   R0EROR
016072                                CKLOOP
016072  104406                        TRAP    C$CLP1
                                        ;
                                        ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE SYNC FLIP-FLOP
                                        ;WAS CLOCKED TO A ZERO AS A RESULT OF THE SIGNAL EDFET H BEING ASSERTED
                                        ;LOW.
                                        ;
016074  004737  006654          9$:   JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
016100  001405                        BEQ     10$                     ;IF OK THEN CONTINUE
016102                                ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
016102  104455                        TRAP    C$ERDF
016104  000003                        .WORD   3
016106  002537                        .WORD   VDALRG
016110  005004                        .WORD   R4EROR
016112                                CKLOOP
016112  104406                        TRAP    C$CLP1
                                        ;
                                        ;SET THE SIGNAL ADAL8 H TO A ZERO.  WHEN ADAL8 H IS A ZERO, THE SIGNAL
                                        ;TOBRK H WILL BE ASSERTED LOW WHICH WILL CAUSE THE SIGNAL BRK H TO BE
                                        ;ASSERTED LOW.
                                        ;
016114  042737  000400  002330  10$:   BIC     #ADAL8,R2LOAD           ;SETUP TO CLEAR ADAL BIT 8
016122  004737  006614                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
016126  001405                        BEQ     11$                     ;IF LOADED OK THEN CONTINUE
016130                                ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
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6490  016130  104455                          TRAP    C$ERDF
6491  016132  000002                          .WORD   2
6492  016134  002513                          .WORD   ADALRG
6493  016136  004770                          .WORD   R2EROR
6494  016140                                  CKLOOP
6495  016140  104406                          TRAP    C$CLP1
6496
6497                                          ;READ CONTROL REGISTER 0 TO CHECK THAT THE SIGNAL TOBRK H IS READ AS
6498                                          ;A ZERO WHEN ADAL REGISTER BIT 8 IS SET TO A ZERO.
6499
6500  016142  042737  000100  002322  11$:   BIC     #TOBRK,ROGOOD           ;EXPECT TOBRK H TO BE A ZERO
6501  016150  004737  006570                  JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
6502  016154  001405                          BEQ     12$                     ;IF OK THEN CONTINUE
6503  016156                                  ERRDF   1,GDALRG,ROEROR         ;TOBRK K PROBABLY STILL HIGH
6504  016156  104455                          TRAP    C$ERDF
6505  016160  000001                          .WORD   1
6506  016162  002406                          .WORD   GDALRG
6507  016164  004754                          .WORD   ROEROR
6508  016166                                  CKLOOP
6509  016166  104406                          TRAP    C$CLP1
6510
6511                                          ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
6512                                          ;CHECK THE PAUSE STATE MACHINE FLIP-FLOP'S TO BE CLEARED.
6513
6514  016170  012737  000200  002334  12$:   MOV     #VDAL7,R4LOAD           ;SETUP BIT TO SET FETCT H TO HIGH STATE
6515  016176  004737  006640                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REGISTER
6516  016202  001405                          BEQ     13$                     ;IF OK THEN CONTINUE
6517  016204                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
6518  016204  104455                          TRAP    C$ERDF
6519  016206  000003                          .WORD   3
6520  016210  002537                          .WORD   VDALRG
6521  016212  005004                          .WORD   R4EROR
6522  016214                                  CKLOOP
6523  016214  104406                          TRAP    C$CLP1
6524
6525                                          ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  A PULSE
6526                                          ;ON XRAS H WITH THE SIGNAL FETCT H SET HIGH, WILL CAUSE THE EDFET
6527                                          ;FLIP-FLOP TO BE CLOCKE  TO A ONE, THUS SETTING THE SIGNAL EDFET H TO
6528                                          ;THE HIGH STATE.  THE TIMEOUT BREAK ONE SHOT WILL ALSO BE FIRED AS A
6529                                          ;RESULT OF A PULSE ON THE SIGNAL DFET H.  A PULSE OCCURS ON DFET H AS
6530                                          ;A RESULT OF THE EDFET FLIP-FLOP BEING SET AND THE SIGNAL RASP H  BEING
6531                                          ;PULSED.  THE SIGNAL RASP H IS PULSED VIA A PULSE ON THE SIGNAL XRAS H.
6532
6533  016216  004737  007272          13$:   JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
6534
6535                                          ;SET THE SIGNAL FETCT H TO THE LOW STATE BY CLEARING VDAL7 H.  CHECK
6536                                          ;THE PAUSE STATE MACHINE FLIP-FLOPS TO BE CLEARED AS A RESULT OF
6537                                          ;THE SIGNAL BRK H BEING ASSERTED LOW BY ADAL8 H BEING A ZERO AND THE
6538                                          ;SIGNAL PAUSE L BEING ASSERTED LOW.
6539
6540  016222  042737  000200  002334          BIC     #VDAL7,R4LOAD           ;SETUP TO SET FETCT H TO LOW STATE
6541  016230  004737  006640                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REGISTER
6542  016234  001405                          BEQ     14$                     ;IF OK THEN CONTINUE
6543  016236                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MAHCINE ERROR
6544  016236  104455                          TRAP    C$ERDF
6545  016240  000003                          .WORD   3
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6546  016242  002537                          .WORD   VDALRG
6547  016244  005004                          .WORD   R4EROR
6548  016246                                  CKLOOP
6549  016246  104406                          TRAP    C$CLP1
6550
6551                                          ;SET THE SIGNAL ADAL8 H TO A ONE TO ENABLE THE TIMEOUT BREAK ONE SHOT
6552                                          ;TO THE BRK H LOGIC.  AT THIS POINT IN TIME, THE TIMEOUT BREAK ONE SHOT
6553                                          ;SHOULD HAVE BEEN FIRED BY A PULSE ON THE SIGNAL DFET H.  THEREFORE,
6554                                          ;THE SIGNALS TOBRK H AND BRK H SHOULD BE ASSERTED LOW.
6555
6556  016250  052737  000400  002330  14$:   BIS     #ADAL8,R2LOAD           ;ENABLE TOBRK H TO BRK H LOGIC
6557  016256  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
6558  016262  001405                          BEQ     15$                     ;IF LOADED OK THEN CONTINUE
6559  016264                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
6560  016264  104455                          TRAP    C$ERDF
6561  016266  000002                          .WORD   2
6562  016270  002513                          .WORD   ADALRG
6563  016272  004770                          .WORD   R2EROR
6564  016274                                  CKLOOP
6565  016274  104406                          TRAP    C$CLP1
6566
6567                                          ;READ CONTROL REGISTER 0 TO CHECK THAT THE TIMEOUT BREAK ONE SHOT WAS
6568                                          ;FIRED BY DFET H.  IF THE TOBRK H SIGNAL IS READ AS A ONE, THEN THE
6569                                          ;ONE SHOT PROBABLY FAILED TO FIRE OR THE ONE SHOT FIRED AND THE DELAY
6570                                          ;WAS TO SHORT.
6571
6572  016276  004737  006570          15$:   JSR     PC,READR0               ;READ AND CHECK THE GDAL REGISTER
6573  016302  001405                          BEQ     16$                     ;IF OK THEN CONTINUE
6574  016304                                  ERRDF   1,GDALRG,R0EROR         ;TIMEOUT BREAK ONE SHOT FAILED TO FIRE
6575  016304  104455                          TRAP    C$ERDF
6576  016306  000001                          .WORD   1
6577  016310  002406                          .WORD   GDALRG
6578  016312  004754                          .WORD   R0EROR
6579  016314                                  CKLOOP
6580  016314  104406                          TRAP    C$CLP1
6581
6582                                          ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  A PULSE
6583                                          ;ON XCAS H WILL CLOCK THE LEVEL OF THE SIGNAL PB H, WHICH SHOULD BE
6584                                          ;LOW AT THIS POINT IN TIME, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
6585                                          ;SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO.  THE SIGNAL PB H
6586                                          ;SHOULD BE ASSERTED LOW AS A RESULT OF PAUSE L AND BRK H BEING ASSERTED
6587                                          ;LOW.
6588
6589  016316  004737  007376          16$:   JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
6590
6591                                          ;READ THE VDAL AND PAUSE STATE MACHINE FLIP-FLOPS TO CHECK THAT THE
6592                                          ;PAUSE STATE HAS NOT BEEN ENTERED YET WHILE THE TIMEOUT BREAK ONE
6593                                          ;SHOT IS STILL FIRING.
6594
6595  016322  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
6596  016326  001405                          BEQ     17$                     ;IF OK THEN CONTINUE
6597  016330                                  ERRDF   3,VDALRG,R4EROR         ;TIMEOUT BREAK ONE SHOT TIMED OUT
6598  016330  104455                          TRAP    C$ERDF
6599  016332  000003                          .WORD   3
6600  016334  002537                          .WORD   VDALRG
6601  016336  005004                          .WORD   R4EROR
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6602  016340                                    CKLOOP
6603  016340  104406                            TRAP    C$CLP1
6604
6605                                            ;SETUP A DELAY TO WAIT FOR THE TIMEOUT BREAK ONE SHOT TO FINISH
6606                                            ;FIRING.  THE TIMEOUT BREAK ONE SHOT, ONCE FIRED, WILL NOT TIMEOUT
6607                                            ;UNTIL APPROXIMATELY ONE SECOND HAS OCCURED.
6608
6609  016342  012702  000002          17$:    MOV     #2,R2                   ;SETUP DOUBLE PRECISION COUNTER
6610  016346  005001                            CLR     R1                      ;SETUP SINGLE PRECISION COUNTER
6611  016350  017703  163724          18$:    MOV     @REG0,R3                ;READ GDAL REGISTER
6612  016354  032703  000100                    BIT     #TOBRK,R3               ;CHECK IF TIMEOUT BREAK BIT SET
6613  016360  001004                            BNE     19$                     ;IF YES THEN GO READ REGISTER AGAIN
6614  016362  005301                            DEC     R1                      ;DECREMENT THE FIRST COUNTER
6615  016364  001371                            BNE     18$                     ;IF NOT 0 THEN DO AGAIN
6616  016366  005302                            DEC     R2                      ;DECREMENT THE SECOND COUNTER
6617  016370  001367                            BNE     18$                     ;IF NOT 0 THEN DO AGAIN
6618  016372  052737  000100  002322  19$:    BIS     #TOBRK,ROGOOD           ;EXPECT TOBRK H TO BE SET TO A ONE
6619  016400  004737  006570                    JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
6620  016404  001405                            BEQ     20$                     ;IF OK THEN CONTINUE
6621  016406                                    ERRDF   1,GDALRG,ROEROR         ;TOBRK H PROBABLY NOT SET
6622  016406  104455                            TRAP    C$ERDF
6623  016410  000001                            .WORD   1
6624  016412  002406                            .WORD   GDALRG
6625  016414  004754                            .WORD   ROEROR
6626  016416                                    CKLOOP
6627  016416  104406                            TRAP    C$CLP1
6628
6629                                            ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORD OF FLIP-
6630                                            ;FLOP WAS SET TO A ONE AS A RESULT OF BRK H BEING ASSERTED HIGH BY
6631                                            ;TOBRK H AND THE EDFET FLIP-FLOP BEING SET TO A ONE.
6632
6633  016420  052737  001000  002336  20$:    BIS     #VDAL9,R4GOOD           ;EXPECT PSMW H TO BE A ONE
6634  016426  004737  006654                    JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
6635  016432  001405                            BEQ     21$                     ;IF OK THEN CONTINUE
6636  016434                                    ERRDF   3,VDALRG,R4EROR         ;PSMW H NOT SET VIA BRK H * EDFET H
6637  016434  104455                            TRAP    C$ERDF
6638  016436  000003                            .WORD   3
6639  016440  002537                            .WORD   VDALRG
6640  016442  005004                            .WORD   R4EROR
6641  016444                                    CKLOOP
6642  016444  104406                            TRAP    C$CLP1
6643
6644                                            ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  THE SIGNAL
6645                                            ;XCAS H WILL CLOCK THE LEVEL OF PB H, WHICH SHOULD BE ASSERTED HIGH AS
6646                                            ;A RESULT OF BRK H AND EDFET H BEING ASSERTED HIGH, INTO THE PAUSE
6647                                            ;STATE SYNC FLIP-FLOP, THUS SETTING THE PAUSE STATE SYNC FLIP-FLOP TO
6648                                            ;A ONE.
6649
6650  016446  004737  007376          21$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
6651
6652                                            ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE SYNC FLIP-FLOP
6653                                            ;WAS SET TO A ONE BY XCAS H WHEN BRK H AND EDFET H WERE ASSERTED HIGH.
6654
6655  016452  052737  002000  002336            BIS     #VDAL10,R4GOOD          ;EXPECT EPSF H TO BE A ONE
6656  016460  004737  006654                    JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
6657  016464  001405                            BEQ     22$                     ;IF OK THEN CONTINUE
```

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                                        ERRDF   3,VDALRG,R4EROR         ;EPSF H NOT 1 VIA BRK H AND EDFET H
                                        TRAP    C$ERDF
                                        .WORD   3
                                        .WORD   VDALRG
                                        .WORD   R4EROR
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;SET THE SIGNALS TOBRK H AND BRK H TO THE LOW STATE BY CLEARING ADAL
                                        ;REGISTER BIT 8.

                        22$:            BIC     #ADAL8,R2LOAD           ;SETUP BIT TO BE CLEARED
                                        JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
                                        BEQ     23$                     ;IF LOADED OK THEN CONTINUE
                                        ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
                                        TRAP    C$ERDF
                                        .WORD   2
                                        .WORD   ADALRG
                                        .WORD   R2EROR
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;TOGGLE THE SIGNAL XCAS H AGAIN BY SETTING AND CLEARING HDAL12 H.  THE
                                        ;SIGNAL XCAS H WILL CLOCK THE LEVEL OF PB H, WHICH SHOULD BE ASSERTED
                                        :LOW AS A RESULT OF BRK H AND PAUSE L BEING ASSERTED LOW, INTO THE
                                        ;PAUSE STATE SYNC FLIP-FLOP, THUS CLEARING THE PAUSE STATE SYNC FLIP-
                                        ;FLOP.  THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP, WHICH
                                        ;WAS HIGH, WILL BE CLOCKED INTO THE 16 BIT ADDRESS FLIP-FLOP BY XCAS H,
                                        ;THUS SETTING THE 16 BIT ADDRESS FLIP-FLOP TO A ONE.

                        23$:            JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H

                                        ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE SYNC FLIP-FLOP
                                        ;WAS CLOCKED TO A ZERO BY XCAS H WHEN THE SIGNAL BRK H WAS ASSERTED
                                        ;LOW.  ALSO CHECK THAT THE 16 BIT ADDRESS FLIP-FLOP WAS CLOCKED TO
                                        ;A ONE.

                                        BIC     #VDAL10,R4GOOD          ;EXPECT EPSF H TO BE A 0
                                        BIS     #VDAL11,R4GOOD          ;EXPECT EPFN H TO BE A 1
                                        JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
                                        BEQ     24$                     ;IF OK THEN CONTINUE
                                        ERRDF   3,VDALRG,R4EROR         ;BRK H PROBABLY NOT CLEARED
                                        TRAP    C$ERDF
                                        .WORD   3
                                        .WORD   VDALRG
                                        .WORD   R4EROR
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;SET ADAL REGISTER BIT 8 TO A ONE.  THIS WILL ENABLE THE SIGNALS
                                        ;TOBRK H AND BRK H TO BE ASSERTED HIGH.

                        24$:            BIS     #ADAL8,R2LOAD           ;SETUP BIT TO BE LOADED
                                        JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
                                        BEQ     25$                     ;IF LOADED OK THEN CONTINUE
                                        ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
```

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6714  016602  104455                          TRAP    C$ERDF
6715  016604  000002                          .WORD   2
6716  016606  002513                          .WORD   ADALRG
6717  016610  004770                          .WORD   R2EROR
6718  016612                                  CKLOOP
6719  016612  104406                          TRAP    C$CLP1
6720
6721                                          ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
6722                                          ;WHEN BRK H AND FETCT H ARE ASSERTED HIGH, THE PAUSE MODE FLIP-FLOP
6723                                          ;WILL BE FORCED INTO PAUSE MODE, THUS SETTING THE SIGNAL PAUSE L TO
6724                                          ;THE HIGH STATE.
6725
6726  016614  052737  000200  002334  25$:   BIS     #VDAL7,R4LOAD           ;SETUP BIT TO BE LOADED
6727  016622  052737  000200  002336          BIS     #VDAL7,R4GOOD           ;SETUP BIT TO BE EXPECTED ON READ
6728  016630  004737  006646                  JSR     PC,LDRD4R               ;GO LOAD AND READ VDAL REGISTER
6729  016634  001405                          BEQ     26$                     ;IF OK THEN CONTINUE
6730  016636                                  ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE MACHINE CHANGED
6731  016636  104455                          TRAP    C$ERDF
6732  016640  000003                          .WORD   3
6733  016642  002537                          .WORD   VDALRG
6734  016644  005004                          .WORD   R4EROR
6735  016646                                  CKLOOP
6736  016646  104406                          TRAP    C$CLP1
6737
6738                                          ;SET ADAL REGISTER BIT 8 TO A ZERO TO ASSERT THE SIGNALS BRK H AND
6739                                          ;TOBRK H TO THE LOW STATE.
6740
6741  016650  042737  000400  002330  26$:   BIC     #ADAL8,R2LOAD           ;SETUP BIT TO BE CLEARED
6742  016656  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
6743  016662  001405                          BEQ     27$                     ;IF OK THEN CONTINUE
6744  016664                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
6745  016664  104455                          TRAP    C$ERDF
6746  016666  000002                          .WORD   2
6747  016670  002513                          .WORD   ADALRG
6748  016672  004770                          .WORD   R2EROR
6749  016674                                  CKLOOP
6750  016674  104406                          TRAP    C$CLP1
6751
6752                                          ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  THE
6753                                          ;SIGNAL XCAS H SHOULD CLOCK THE PAUSE STATE SYNC FLIP-FLOP TO A ONE
6754                                          ;AS A RESULT OF PAUSE L BEING ASSERTED HIGH AND THE EDFET FLIP-FLOP
6755                                          ;BEING SET TO A ONE.  THE SIGNAL PAUSE L SHOULD HAVE BEEN SET HIGH
6756                                          ;AS A RESULT OF THE SIGNAL BRK H AND FETCT H BEING ASSERTED HIGH
6757                                          ;PREVIOUSLY.  THE 16 BIT ADDRESS FLIP-FLOP SHOULD BE CLOCKED TO A
6758                                          ;ZERO AS A RESULT OF XCAS H AND THE PREVIOUS OUTPUT OF THE PAUSE STATE
6759                                          ;SYNC FLIP-FLOP, WHICH WAS LOW.
6760
6761  016676  004737  007376          27$:   JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
6762
6763                                          ;READ THE VDAL REGISTER TO CHECK THAT BRK H AND FETCT H BEING ASSERTED
6764                                          ;HIGH PREVIOUSLY CAUSED THE PAUSE MODE FLIP-FLOP TO BE SET TO THE
6765                                          ;PAUSE MODE FROM THE RUN MODE.  WHEN THE PAUSE MODE FLIP-FLOP IS SET
6766                                          ;TO THE PAUSE MODE, THE SIGNAL PAUSE L WILL BE ASSERTED HIGH.
6767
6768  016702  042737  004000  002336          BIC     #VDAL11,R4GOOD          ;EXPECT EPFN H TO BE A 0
6769  016710  052737  002000  002336          BIS     #VDAL10,R4GOOD          ;EXPECT EPSF H TO BE A 1
```

```
6770  016716  004737  006654          JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
6771  016722  001405                  BEQ     28$                     ;IF OK THEN CONTINUE
6772  016724                          ERRDF   3,VDALRG,R4EROR         ;PAUSE L PROBABLY NOT SET HIGH
6773  016724  104455                  TRAP    C$ERDF
6774  016726  000003                  .WORD   3
6775  016730  002537                  .WORD   VDALRG
6776  016732  005004                  .WORD   R4EROR
6777  016734                          CKLOOP
6778  016734  104406                  TRAP    C$CLP1
6779
6780                                  ;CLEAR THE SIGNAL FETCT H AND PULSE THE SIGNAL INVD L VIA VDAL2 H.
6781                                  ;THE SIGNAL INVD L WILL CAUSE THE PAUSE STATE MACHINE FLIP-FLOPS
6782                                  ;TO BE CLEARED.
6783
6784  016736  005037  002334  28$:    CLR     R4LOAD                  ;SETUP TO CLEAR FETCT H
6785  016742  004737  007712          JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
6786
6787  016746                          ENDSEG
6788  016746                  10000$:
6789  016746  104405                  TRAP    C$ESEG
6790  016750                          ENDTST
6791  016750                  L10060:
6792  016750  104401                  TRAP    C$ETST
6793
6794
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                                .SBTTL  TEST 31: PAUSE STATE MACHINE - 16 BIT ADDRESS - RUN MODE

                                ;++
                                ; THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN "RUN" AND 16 BIT ADDRESS MODE.
                                ; WHEN THE PAUSE STATE MACHINE IS SE    IN "RUN" MODE VIA ADAL4 H ON A ONE AND
                                ; A PULSE ON XRAS H, THE PAUSE STATE  ACHINE CAN ONLY BE ENTERED WHEN A BREAK
                                ; CONDITION IS RECEIVED ON THE SIGNAL "BRK H".  THIS TEST WILL USE THE SINGLE
                                ; STEP BREAK FLIP-FLOP TO GENERATE THE BREAK CONDITION.  THE TEST WILL CHECK
                                ; THAT THE PAUSE STATE MACHINE IS NOT ENTERED WHEN THE SINGLE STEP BREAK FLIP-
                                ; FLOP IS CLEARED AND THAT IT CAN BE ENTERED WHEN THE SINGLE STEP BREAK FLIP-
                                ; FLOP IS SET TO A ONE.  THE TEST WILL CHECK THAT THE SINGLE STEP BREAK FLIP-
                                ; FLOP ONCE SET, WILL REMAIN LATCHED TO THE SET STATE UNTIL CLEARED BY A PULSE
                                ; BEING ISSUED ON THE SIGNAL "BRKRES L".  THE TEST WILL SET THE PAUSE STATE
                                ; MACHINE FLIP-FLOP'S: PAUSE STATE WORKING, PAUSE STATE SYNC AND 16 BIT ADDRESS
                                ; VIA THE SIGNALS XRAS H AND XCAS H.  ONCE ALL THESE FLIP-FLOPS ARE SET TO THE
                                ; ONE STATE, THE TEST WILL CHECK THAT THEY CAN BE CLEARED BY ISSUING A PULSE ON
                                ; THE SIGNAL "INVD L".
                                ;--

016752                                  BGNTST
016752                          T31::
016752  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
016756                                  BGNSEG
016756  104404                          TRAP    C$BSEG

                                ;SET AND CLEAR ADAL0 H IN THE ADAL REGISTER TO CAUSE A PULSE ON THE SIGNAL
                                ;BRKRES L.  THE SIGNAL BRKRES L WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP.

016760  005037  002330                   CLR     R2LOAD                  ;SETUP TO CLEAR ALL R/W BITS IN ADAL REG
016764  004737  007772                   JSR     PC,BRKRES               ;GO PULSE BRKRES L VIA ADAL0 H

                                ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 AND CHECK THAT NO BREAK CONDITIONS
                                ;ARE SET IN THE GDAL REGISTER.

016770  004737  007006                   JSR     PC,SLMODR               ;SELECT THE MODE REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK THE MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES.
                                ;MODE REGISTER BIT 11 ON A ZERO WILL ENABLE 16 BIT ADDRESS MODE.

016774  005037  002342                   CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES.
017000  004737  006672                   JSR     PC,LDRDR6               ;LOAD, READ AND CHECK MODE REGISTER
017004  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
017006                                   ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
017006  104455                          TRAP    C$ERDF
017010  000004                          .WORD   4
017012  002631                          .WORD   MODREG
017014  005020                          .WORD   R06ERR
017016                                  CKLOOP
017016  104406                          TRAP    C$CLP1

                                ;SELECT THE HDAL REGISTER VIA GGDAL BITS 2:0 IN CONTROL REGISTER 0.

017020  004737  006754          1$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER  VIA GDAL BITS 2:0

                                ;CLEAR ALL BITS IN THE HDAL REGISTER EXCEPT HDAL2 H. HDAL2 H WILL BE SET
                                ;TO A 1 TO ALLOW THE PROGRAM TO GENERATE THE T-11 TIMING + CONTROL SIGNALS
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6851
6852  017024  012737  000004  002342          MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
6853  017032  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK HDAL REGISTER
6854  017036  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
6855  017040                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
6856  017040  104455                          TRAP    C$ERDF
6857  017042  000004                          .WORD   4
6858  017044  002605                          .WORD   HDALRG
6859  017046  005020                          .WORD   R06ERR
6860  017050                                  CKLOOP
6861  017050  104406                          TRAP    C$CLP1
6862
6863                                          ;TOGGLE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL2 H IN CONTROL
6864                                          ;REGISTER 4.  INVD L WILL INITIALIZE ALL FLIP-FLOPS ON THE MODULE NOT
6865                                          ;CLEARED BY THE SIGNAL BRKRES L.  THE SINGLE STEP SYNC FLIP-FLOP WILL
6866                                          ;BE PRESET TO A ONE THUS SETTING THE SIGNAL PSM L TO THE HIGH STATE.
6867
6868  017052  005037  002334          2$:     CLR     R4LOAD                  ;SETUP TO CLEAR ALL VDAL R/W BITS
6869  017056  004737  007712                  JSR     PC,CLRPSM               ;PULSE INVD L VIA VDAL2 H
6870
6871                                          ;SET ADAL REGISTER BITS 5 AND 4 TO ONES.  ADAL REGISTER BIT 4 ON A ONE
6872                                          ;WILL CAUSE THE PAUSE MODE FLIP-FLOP TO BE SET TO THE "RUN MODE" WHEN THE
6873                                          ;SIGNAL XRAS H IS PULSED.  WHEN THE PAUSE MODE FLIP-FLOP IS SET TO "RUN
6874                                          ;MODE", THE SIGNAL PAUSE L WILL BE ASSERTED LOW, THEREFORE, THE PAUSE
6875                                          ;STATE MACHINE CAN ONLY BE ENTERED WHEN A BREAK CONDITION IS RECEIVED.
6876                                          ;ADAL REGISTER BIT 5 ON A ONE WILL ENABLE THE SINGLE STEP BREAK FLIP-
6877                                          ;FLOP TO BE SET WHEN A PULSE IS ISSUED ON THE SIGNAL XRAS H AND THE
6878                                          ;SIGNALS FETCT H AND PSM L ARE ASSERTED HIGH.
6879
6880  017062  012737  000060  002330          MOV     #ADAL5!ADAL4,R2LOAD     ;SETUP BITS TO BE LOADED
6881  017070  004737  006614                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK ADAL REGISTER
6882  017074  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
6883  017076                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
6884  017076  104455                          TRAP    C$ERDF
6885  017100  000002                          .WORD   2
6886  017102  002513                          .WORD   ADALRG
6887  017104  004770                          .WORD   R2EROR
6888  017106                                  CKLOOP
6889  017106  104406                          TRAP    C$CLP1
6890
6891                                          ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE
6892                                          ;IN CONTROL REGISTER 4'S VDAL REGISTER.
6893
6894  017110  052737  000200  002334  3$:     BIS     #VDAL7,R4LOAD           ;SETUP BIT TO BE LOADED
6895  017116  004737  006640                  JSR     PC,LDRDR4               ;LOAD, READ AND CHECK VDAL REGISTER
6896  017122  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
6897  017124                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
6898  017124  104455                          TRAP    C$ERDF
6899  017126  000003                          .WORD   3
6900  017130  002537                          .WORD   VDALRG
6901  017132  005004                          .WORD   R4EROR
6902  017134                                  CKLOOP
6903  017134  104406                          TRAP    C$CLP1
6904
6905                                          ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  PULSING
6906                                          ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH IS HIGH, INTO
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                                        ;THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L TO THE LOW
                                        ;STATE.  A PULSE ON XRAS H WILL CLOCK THE STATE OF FETCT H, WHICH IS
                                        ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
                                        ;HIGH STATE.  THE SINGLE STEP SYNC FLIP-FLOP WAS PRESET TO A ONE EARLIER
                                        ;IN THIS TEST THUS SETTING THE SIGNAL PSM L TO THE HIGH STATE.  A PULSE
                                        ;ON XRAS H WILL CAUSE THE SINGLE STEP BREAK FLIP-FLOP TO BE SET TO A ONE
                                        ;AS A RESULT OF FETCT H, ADAL5 H AND PSM L BEING ASSERTED HIGH.  WHEN THE
                                        ;SINGLE STEP BREAK FLIP-FLOP GETS SET TO A ONE, THE SIGNAL "BRK H" WILL
                                        ;BE ASSERTED HIGH WHICH WILL CAUSE THE SIGNAL "SOP H" TO BE ASSERTED HIGH.
                                        ;WHEN THE SIGNALS SOP H AND EDFET H ARE ASSERTED HIGH, THE PAUSE STATE
                                        ;WORKING FLIP-FLOP WILL BE PRESET TO A ONE, THUS SETTING THE SIGNALS
                                        ;PSMW H AND PSMW L TO THE HIGH AND LOW STATES RESPECTIVELY.  THE PAUSE
                                        ;MODE FLIP-FLOP WILL BE SET TO PAUSE MODE AS A RESULT OF FETCT H AND
                                        ;BRK H BEING ASSERTED HIGH.  THE SIGNAL PAUSE L WILL BE ASSERTED HIGH
                                        ;AS A RESULT OF THE PAUSE MODE FLIP-FLOP BEING SET TO PAUSE MODE.

017136  004737  007272          4$:    JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H

                                        ;READ THE GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
                                        ;IS SET TO A ONE AS A RESULT OF A PULSE ON THE SIGNAL XRAS H AND THE
                                        ;SIGNALS FETCT H, PSM L AND ADAL5 H BEING ASSERTED HIGH.

017142  052737  000200  002322          BIS     #SSBRK,ROGOOD           ;SETUP TO EXPECT SSBRK H TO EQUAL A 1
017150  004737  006570                  JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
017154  001405                          BEQ     5$                      ;IF OK THEN CONTINUE
017156                                  ERRDF   1,GDALRG,ROEROR         ;SSBRK H PROBABLY NOT SET TO A 1
017156  104455                          TRAP    C$ERDF
017160  000001                          .WORD   1
017162  002406                          .WORD   GDALRG
017164  004754                          .WORD   ROEROR
017166                                  CKLOOP
017166  104406                          TRAP    C$CLP1

                                        ;READ THE VDAL REGISTER TO CHECK THAT SSBRK H BEING ASSERTED HIGH CAUSED
                                        ;THE PAUSE STATE WORKING FLIP-FLOP TO GET SET TO A ONE VIA THE SIGNALS
                                        ;BRK H, SOP H AND EDFET H.

017170  052737  001000  002336  5$:    BIS     #VDAL9,R4GOOD           ;EXPECT PSMW H TO BE ASSERTED HIGH
017176  004737  006654                  JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
017202  001405                          BEQ     6$                      ;IF OK TTHEN CONTINUE
017204                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
017204  104455                          TRAP    C$ERDF
017206  000003                          .WORD   3
017210  002537                          .WORD   VDALRG
017212  005004                          .WORD   R4EROR
017214                                  CKLOOP
017214  104406                          TRAP    C$CLP1

                                        ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  THE SIGNAL
                                        ;XCAS H WILL CLOCK THE SINGLE STEP SYNC FLIP-FLOP TO A ZERO AS A RESULT
                                        ;OF THE SIGNAL PSMW L BEING ASSERTED LOW.  THIS WILL CAUSE THE SIGNAL
                                        ;PSM L TO BE ASSERTED LOW.  THE PAUSE  STATE SYNC FLIP-FLOP WILL BE SET
                                        ;TO A ONE AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH WHEN A
                                        ;PULSE IS ISSUED ON XCAS H.

017216  004737  007376          6$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
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6963
6964                                        ;READ THE VDAL REGISTER TO CHECK THE THE PAUSE STATE SYNC FLIP-FLOP WAS
6965                                        ;SET TO A ONE BBY XCAS H WHEN EDFETT H AND SOP H ARE ASSERTED HIGH.
6966
6967  017222  052737  002000  002336        BIS     #VDAL10,R4GOOD          ;EXPECT EPSF H TO BE SET TO A ONE
6968  017230  004737  006654                JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
6969  017234  001405                        BEQ     7$                      ;IF OK THEN CONTINUE
6970  017236                                ERRDF   3,VDALRG,R4EROR         ;EPSF H PROBABLY NOT SET TO A ONE
6971  017236  104455                        TRAP    C$ERDF
6972  017240  000003                        .WORD   3
6973  017242  002537                        .WORD   VDALRG
6974  017244  005004                        .WORD   R4EROR
6975  017246                                CKLOOP
6976  017246  104406                        TRAP    C$CLP1
6977
6978                                        ;READ GDAL REGISTER TO CHECK THAT SINGLE STEP SYNC FLIP-FLOP IS STILL
6979                                        ;SET TO A ONE AFTER XCAS H IS PULSED. NO CHANGE SHOULD HAVE OCCURED.
6980
6981  017250  004737  006370        7$:     JSR     PC,READR0               ;READ AND CHECK GDAL REGISTER
6982  017254  001405                        BEQ     8$                      ;IF OK THEN CONTINUE
6983  017256                                ERRDF   1,GDALRG,R0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
6984  017256  104455                        TRAP    C$ERDF
6985  017260  000001                        .WORD   1
6986  017262  002406                        .WORD   GDALRG
6987  017264  004754                        .WORD   R0EROR
6988  017266                                CKLOOP
6989  017266  104406                        TRAP    C$CLP1
6990
6991                                        ;TOGGLE THE SIGNAL XRAS H AGAIN BY SETTING AND CLEARING HDAL12 H.  THIS
6992                                        ;IS DONE TO CHECK THAT ONCE THE SINGLE STEP BREAK FLIP-FLOP IS SET TO
6993                                        ;A ONE, IT WILL REMAIN SET TO THAT STATE UNTIL CLEARED VIA A PULSE ON THE
6994                                        ;SIGNAL BRKRES L.  AT THIS POINT IN TIME, FETCT H AND ADAL5 H ARE ASSERTED
6995                                        ;HIGH AND THE SIGNAL PSM L SHOULD BE ASSERTED LOW.  THE PAUSE MODE
6996                                        ;FLIP-FLOP WILL BE HELD IN PAUSE MODE VIA THE SIGNALS BRK H AND FETCT H.
6997
6998  017270  004737  007272        8$:     JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
6999
7000                                        ;READ GDAL REGISTER TO CHECK THAT SSBRK H IS STILL ASSERTED HIGH AS A
7001                                        ;RESULT OF IT BEING LATCHED AND A PULSE ON XRAS H.
7002
7003  017274  004737  006570                JSR     PC,READR0               ;READ AND CHECK GDAL REGISTER
7004  017300  001405                        BEQ     9$                      ;IF OK THEN CONTINUE
7005  017302                                ERRDF   1,GDALRG,R0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
7006  017302  104455                        TRAP    C$ERDF
7007  017304  000001                        .WORD   1
7008  017306  002406                        .WORD   GDALRG
7009  017310  004754                        .WORD   R0EROR
7010  017312                                CKLOOP
7011  017312  104406                        TRAP    C$CLP1
7012
7013                                        ;READ VDAL REGISTER TO CHECK THAT NO CHANGE OCCURED AFTER PULSING XRAS H.
7014
7015  017314  004737  006654        9$:     JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
7016  017320  001405                        BEQ     10$                     ;IF NO CHANGE THEN CONTINUE
7017  017322                                ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
7018  017322  104455                        TRAP    C$ERDF
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7019  017324  000003                          .WORD   3
7020  017326  002537                          .WORD   VDALRG
7021  017330  005004                          .WORD   R4EROR
7022  017332                                  CKLOOP
7023  017332  104406                          TRAP    C$CLP1
7024
7025                                          ;TOGGLE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT 0.
7026                                          ;A PULSE ON BRKRES L WILL CLEAR THE SINGLE STEP BREAK FL.    OP.
7027
7028  017334  004737  007772          10$:    JSR     PC,BRKRES               ;PULSE BRKRES L VIA ADALO H
7029
7030                                          ;READ GDAL REGISTER TO CHECK THAT BRKRES L CLEARING THE SINGLE STEP
7031                                          ;BREAK FLIP-FLOP.  THE SIGNAL SSBRK H SHOULD BE ASSERTED LOW.
7032
7033  017340  042737  000200  002322          BIC     #SSBRK,ROGOOD           ;SETUP TO EXPECT SSBRK H TO BE 0
7034  017346  004737  006570                  JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
7035  017352  001405                          BEQ     11$                     ;IF OK THEN CONTINUE
7036  017354                                  ERRDF   1,GDALRG,ROEROR         ;VDAL REGISTER NOT EQUAL EXPECTED
7037  017354  104455                          TRAP    C$ERDF
7038  017356  000001                          .WORD   1
7039  017360  002406                          .WORD   GDALRG
7040  017362  004754                          .WORD   ROEROR
7041  017364                                  CKLOOP
7042  017364  104406                          TRAP    C$CLP1
7043
7044                                          ;READ VDAL REGISTER TO CHECK THAT NO CHANGE OCCURED AS A RESULT OF
7045                                          ;PULSING BRKRES L.
7046
7047  017366  004737  006654          11$:    JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
7048  017372  001405                          BEQ     12$                     ;IF NO CHANGE THEN CONTINUE
7049  017374                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
7050  017374  104455                          TRAP    C$ERDF
7051  017376  000003                          .WORD   3
7052  017400  002537                          .WORD   VDALRG
7053  017402  005004                          .WORD   R4EROR
7054  017404                                  CKLOOP
7055  017404  104406                          TRAP    C$CLP1
7056
7057                                          ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  THE SINGLE
7058                                          ;STEP BREAK FLIP-FLOP SHOULD NOT BE SET TO A ONE THIS TIME BECAUSE THE
7059                                          ;SIGNAL PSM L WAS ASSERTED LOW EARLIER IN THIS TEST WHEN THE PAUSE STATE
7060                                          ;WORKING FLIP-FLOP WAS SET TO A ONE AND A PULSE WAS ISSUED ON THE SIGNAL
7061                                          ;XCAS H.  THE PAUSE MODE FLIP-FLOP WILL BE SET TO "RUN MODE" AND THE
7062                                          ;EDFET FLIP-FLOP WILL BE SET TO A ONE WHEN THE SIGNAL XRAS H IS PUL  .
7063
7064  017406  004737  007272          12$:    JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
7065
7066                                          ;READ GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP WAS
7067                                          ;NOT SET TO A ONE WHEN PSM L WAS ASSERTED LOW, FETCT H AND ADAL5 H
7068                                          ;WERE ASSEPTED HIGH AND A PULSE WAS ISSUED ON THE SIGNAL XRAS H.
7069
7070  017412  004737  006570                  JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
7071  017416  001405                          BEQ     13$                     ;IF OK THEN CONTINUE
7072  017420                                  ERRDF   1,GDALRG,ROEROR         ;CHECK SIGNAL PSM L TO BE LOW
7073  017420  104455                          TRAP    C$ERDF
7074  017422  000001                          .WORD   1
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7075  017424  002406                          .WORD   GDALRG
7076  017426  004754                          .WORD   ROEROR
7077  017430                                  CKLOOP
7078  017430  104406                          TRAP    C$CLP1
7079
7080                                          ;RE-  VDAL REGISTER TO CHECK THAT NO CHANGES HAVE OCCURED .
7081
7082  017432  004737  006654        13$:     JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
7083  017436  001405                          BEQ     14$                     ;IF NO CHANGE THEN CONTINUE
7084  017440                                  ERRDF   3,VDALRG,R4EROR         ;VVDAL REGISTER NOT EQUAL EXPECTED
7085  017440  104455                          TRAP    C$ERDF
7086  017442  000003                          .WORD   3
7087  017444  002537                          .WORD   VDALRG
7088  017446  005004                          .WORD   R4EROR
7089  017450                                  CKLOOP
7090  017450  104406                          TRAP    C$CLP1
7091
7092                                          ;LEAVING FETCT H ASSERTED HIGH, PULSE THE SIGNAL INVD L BY SETTING AND
7093                                          ;CLEARING VDAL2 H IN THE VDAL REGISTER.  A PULSE ON INVD L WILL
7094                                          ;INITIALIZE THOSE FLIP-FLOPS ON THE MODULE NOT CLEARED BY BRKRES L.
7095                                          ;A PULSE ON INVD L WILL ALSO PRESET THE SINGLE STEP SYNC FLIP-FLOP
7096                                          ;SO THAT THE SIGNAL PSM L WILL BE ASSERTED HIGH.
7097
7098  017452  004737  007712        14$:     JSR     PC,CLRPSM               ;PULSE INVD L AND LEAVE FETCT H SET
7099
7100                                          ;TO CHECK THAT INVD L PRESET THE PAUSE STATE SYNC FLIP-FLOP, THE TEST
7101                                          ;WILL PULSE XRAS H AND EXPECT THE SINGLE STEP BREAK FLIP-FLOP TO BE
7102                                          ;SET TO A ONE AS A RESULT OF FETCT H, ADAL5 H AND PSM L BEING ASSERTED
7103                                          ;HIGH WHEN XRAS H IS PULSED.
7104
7105  017456  004737  007272                  JSR     PC,XRAS                 ;PULSE XRAS H VIA HDAL12 H
7106
7107                                          ;READ GDAL REG TO CHECK THAT THE SINGLE STEP BREAK F/F WAS SET TO A ONE.
7108
7109  017462  052737  000200  002322          BIS     #SSBRK,ROGOOD           ;EXPECT SSBRK H TO BE SET HIGH
7110  017470  004737  006570                  JSR     PC,READR0               ;READ AND CHECK GDAL REGISTER
7111  017474  001405                          BEQ     15$                     ;IF SET THEN CONTINUE
7112  017476                                  ERRDF   1,GDALRG,ROEROR         ;INVD L PROBALY DIDN'T PRESET PSM F/F
7113  017476  104455                          TRAP    C$ERDF
7114  017500  000001                          .WORD   1
7115  017502  002406                          .WORD   GDALRG
7116  017504  004754                          .WORD   ROEROR
7117  017506                                  CKLOOP
7118  017506  104406                          TRAP    C$CLP1
7119
7120                                          ;CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP WAS SET TO A ONE AS A
7121                                          ;RESULT OF EDFET H BEING ASSERTED HIGH AND SOP H BEING ASSERTED HIGH
7122                                          ;VIA BRK H AND SSBRK H.
7123
7124  017510  052737  001000  002336  15$:     BIS     #VDAL9,R4GOOD           ;EXPECT PSMW H TO BE A ONE
7125  017516  004737  006654                  JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
7126  017522  001405                          BEQ     16$                     ;IF OK THEN CONTINUE
7127  017524                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
7128  017524  104455                          TRAP    C$ERDF
7129  017526  000003                          .WORD   3
7130  017530  002537                          .WORD   VDALRG
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7131  017532  005004                          .WORD   R4EROR
7132  017534                                  CKLOOP
7133  017534  104406                          TRAP    C$CLP1
7134
7135                                          ;PULSE THE SIGNALS BRKRES L AND INVD L BY SETTING AND CLEARING THE
7136                                          ;SIGNALS ADAL0 H AND VDAL2 H.  BRKRES L WILL CLEAR THE SINGLE STEP
7137                                          ;BREAK FLIP-FLOP.  INVD L WILL CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS
7138                                          ;AND PRESET THE PSM FLIP-FLOP TO A ONE.
7139
7140  017536  004737  007772          6$:     JSR     PC,BRKRES               ;PULSE BRKRES L VIA ADAL0 H
7141  017542  004737  007712                  JSR     PC,CLRPSM               ;PULSE INVD L VIA VDAL2 H
7142
7143                                          ;READ GDAL REG TO CHECK THAT BRKRES L CLEARED SINGLE STEP BREAK F/F.
7144
7145  017546  042737  000200  002322          BIC     #SSBRK,ROGOOD           ;EXPECT SSBRK H TO BE ASSERTED LOW
7146  017554  004737  006570                  JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
7147  017560  001405                          BEQ     17$                     ;IF CLEARED THEN CONTINUE
7148  017562                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
7149  017562  104455                          TRAP    C$ERDF
7150  017564  000001                          .WORD   1
7151  017566  002406                          .WORD   GDALRG
7152  017570  004754                          .WORD   ROEROR
7153  017572                                  CKLOOP
7154  017572  104406                          TRAP    C$CLP1
7155
7156                                          ;TOGGLE THE SIGNAL XCAS H TO CLOCK THE OUTPUT OF THE PAUSE STATE
7157                                          ;WORKING FLIP-FLOP, WHICH IS HIGH, INTO THE SINGLE STEP SYNC FLIP-FLOP.
7158                                          ;THIS SHOULD CAUSE THE SIGNAL PSM L, WHICH IS ALREADY HIGH, TO BE
7159                                          ;CLOCKED HIGH.  THIS IS DONE TO CHECK THAT THE DATA INPUT LEAD TO THE
7160                                          ;PSM FLIP-FLOP IS NOT FLOATING.
7161
7162  017574  004737  007376          17$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
7163
7164                                          ;TO CHECK THAT THE PSM FLIP-FLOP WAS SET TO A ONE, TOGGLE THE SIGNAL
7165                                          ;XRAS H TO SET THE SINGLE STEP BREAK FLIP-FLOP TO A ONE.  THE SIGNALS
7166                                          ;PSM L, ADAL5 H AND FETCT H SHOULD ALL BBE ASSERTED HIGH.
7167
7168  017600  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
7169
7170                                          ;READ GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP WAS
7171                                          ;SET TO A ONE.
7172
7173  017604  052737  000200  002322          BIS     #SSBRK,ROGOOD           ;EXPECT SSBRK H TO BE ASSERTED HIGH
7174  017612  004737  006570                  JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
7175  017616  001405                          BEQ     1^.                     ;IF OK THEN CONTINUE
7176  017620                                  ERRDF   1,GDALRG,ROEROR         ;XCAS H FAILED TO CLOCK PSM L F/F TO 1
7177  017620  104455                          TRAP    C$ERDF
7178  017622  000001                          .WORD   1
7179  017624  002406                          .WORD   GDALRG
7180  017626  004754                          .WORD   ROEROR
7181  017630                                  CKLOOP
7182  017630  104406                          TRAP    C$CLP1
7183
7184                                          ;PULSE THE SIGNALS BRKRES L AND INVD L BY SETTING AND CLEARING ADAL0 H
7185                                          ;AND VDAL2 H.  BRKRES L WILL CLEAR THE SINGLE STEP BREAK FLIP-FLOP.
7186                                          ;INVD L WILL INITIALIZE ALL FLIP-FLOPS NOT CLEARED BY BRKRES L.  THE
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                                        ;PSM FLIP-FLOP WILL BE PRESET TO A ONE VIA THE SIGNAL INVD L.  THE SIGNAL
                                        ;FETCT H WILL BE SET LOW BY CLEARING VDAL7 H IN THE VDAL REGISTER

017632  004737  007772        18$:    JSR     PC,BRKRES               ;PULSE BRKRES L VIA ADALO H

017636  005037  002334                CLR     R4LOAD                  ;SET FETCT H TO THE LOW STATE
017642  004737  007712                JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H

                                        ;READ GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
                                        ;WAS CLEARED BY BRKRES L.

017646  042737  000200  002322          BIC     #SSBRK,ROGOOD           ;EXPECT SSBRK H TO BE A 0
017654  004737  006570                JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
017660  001405                        BEQ     19$                     ;IF OK THEN CONTINUE
017662                                EPRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
017662  104455                        TRAP    C$ERDF
017664  000001                        .WORD   1
017666  002406                        .WORD   GDALRG
017670  004754                        .WORD   ROEROR
017672                                CKLOOP
017672  104406                        TRAP    C$CLP1

                                        ;PULSE THE SIGNAL XRAS H TO CHEC. THAT THE SINGLE STEP BREAK FLIP-FLOP
                                        ;WILL NOT GET SET TO A ONE WHEN  IE SIGNAL FETCT H IS ASSERTED LOW AND
                                        ;THE SIGNALS ADAL5 H AND PSM L ARE ASSERTED HIGH.

017674  004737  007272        19$:    JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H

                                        ;READ GDAL REGISTER TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
                                        ;DID NOT GET SET TO A ONE WHEN FETCT H WAS SET LOW, PSM L AND  DAL5 H
                                        ;WERE ASSERTED HIGH AND A PULSE WAS ISSUED ON THE SIGNAL XRAS H.

017700  004737  006570                JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
017704  001405                        BEQ     20$                     ;IF OK THEN CONTINUE
017706                                ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
017706  104455                        TRAP    C$ERDF
017710  000001                        .WORD   1
017712  002406                        .WORD   GDALRG
017714  004754                        .WORD   ROEROR
017716                                CKLOOP
017716  104406                        TRAP    C$CLP1

                                        ;SET THE SIGNAL FETCT H TO THE HIGH STATE AND CHECK ALL THE OTHER BITS
                                        ;IN THE VDAL REGGISTER TO BE CLEARED.

017720  012737  000200  002334  20$:    MOV     #VDAL7,R4LOAD           ;SETUP BIT TO SET FETCT H TO HIGH STATE
017726  004737  006640                JSR     PC,LDRDR4               ;LOAD, READ AND CEHCK VDAL REGISTER
017732  001405                        BEQ     21$                     ;IF OK THEN CONTINUE
017734                                ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
017734  104455                        TRAP    C$ERDF
017736  000003                        .WORD   3
017740  002537                        .WOF    VDALRG
017742  005004                        .WOF    R4EROR
017744                                CKL
017744  104406                        TRAP    C$CLP1
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                                        ;SET ADAL REGISTER BIT 5 TO A ZERO.  WHEN THIS BIT IS SET TO A ZERO,
                                        ;THE SINGLE STEP BREAK FLIP-FLOP SHOULD NOT GET SET TO A ONE WHEN
                                        ;A PULSE IS ISSUED ON THE SIGNAL XRAS H.

017746  042737  000040  002330  21$:  BIC     #ADAL5,R2LOAD          ;SETUP TO CLEAR ADAL REGISTER BIT 5
017754  004737  006614                 JSR     PC,LDRDR2              ;IF LOADED OK THEN CONTINUE
017760  001405                         BEQ     22$                    ;IF LOADED OK THEN CONTINUE
017762                                 ERRDF   2,ADALRG,R2EROR        ;ADAL REGISTER NOT EQUAL EXPECTED
017762  104455                         TRAP    C$ERDF
017764  000002                         .WORD   2
017766  002513                         .WORD   ADALRG
017770  004770                         .WORD   R2EROR
017772                                 CKLOOP
017772  104406                         TRAP    C$CLP1

                                        ;PULSE THE SIGNAL XRAS H TO CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
                                        ;WILL NOT GET SET WHEN ADAL5 H IS ASSERTED LOW AND FETCT H AND PSM L
                                        ;ARE ASSERTED HIGH.

017774  004737  007272          22$:  JSR     PC,XRAS                ;GO PULSE XRAS H VIA HDAL12 H

                                        ;READ GDAL REGISTER TO CHECK THAT SINGLE STEP BREAK FLIP-FLOP DID NOT
                                        ;GET SET TO A ONE.

020000  004737  006570                 JSR     PC,READR0              ;READ AND CHECK GDAL REGISTER
020004  001405                         BEQ     23$                    ;IF OK THEN CONTINUE
020006                                 ERRDF   1,GDALRG,R0EROR        ;GDAL REGISTER NOT EQUAL EXPECTED
020006  104455                         TRAP    C$ERDF
020010  000001                         .WORD   1
020012  002406                         .WORD   GDALRG
020014  004754                         .WORD   R0EROR
020016                                 CKLOOP
020016  104406                         TRAP    C$CLP1

                                        ;READ VDAL REGISTER TO CHECK THAT NO CHANGES OCCURED AS A RESULT OF
                                        ;PULSING XRAS H WHEN ADAL5 H WAS SET TO A ZERO.  SET THE SIGNAL FETCT H
                                        ;TO THE LOW STATE.

020020  005037  002334          23$:  CLR     R4LOAD                 ;SETUP TO CLEAR FETCT H
020024  004737  006640                 JSR     PC,LDRDR4              ;LOAD, READ AND CHECK VDAL REGISTER
020030  001404                         BEQ     24$                    ;IF NO CHANGE THEN CONTINUE
020032                                 ERRDF   3,VDALRG,R4EROR        ;VDAL REGISTER NOT EQUAL EXPECTED
020032  104455                         TRAP    C$ERDF
020034  000003                         .WORD   3
020036  002537                         .WORD   VDALRG
020040  005004                         .WORD   R4EROR
020042                          24$:   ENDSEG
020042                          10000$:
020042  104405                         TRAP    C$ESEG
020044                                 ENDTST
020044                          L10061:
020044  104401                         TRAP    C$ETST
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                                .SBTTL  TEST 32: CHECK EDFET F/F TO BE CLEARED VIA XPI L

                                ;++
                                ; THIS TEST WILL CHECK THAT THE EDFET FLIP-FLOP CAN BE CLEARED WHEN A PULSE IS
                                ; ISSUED OF THE SIGNAL XPI L.  THE TEST WILL SET ADAL4 H TO A ZERO TO CAUSE
                                ; THE PAUSE MODE FLIP-FLOP TO BE SET TO THE PAUSE MODE WHEN A PULSE IS ISSUED
                                ; ON THE SIGNAL XRAS H.  THE TEST WILL SET THE SIGNAL FETCT H TO THE HIGH STATE
                                ; BY SETTING VDAL7 H TO A ONE.  THE TEST WILL THEN PULSE XRAS H TO SET THE
                                ; EDFET FLIP-FLOP TO A ONE AND TO SET THE PAUSE MODE FLIP-FLOP TO THE PAUSE MODE.
                                ; WHEN EDFET FLIP-FLOP IS SET TO A ONE AND THE PAUSE MODE FLIP-FLOP IS SET TO
                                ; THE PAUSE MODE, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
                                ; THE TEST WILL NOW PULSE THE SIGNAL XPI L TO CLEAR THE EDFET FLIP-FLOP.  WHEN
                                ; THE EDFET FLIP-FLOP IS CLEARED, THE SIGNAL PB H WILL BE ASSERTED LOW.  THE
                                ; SIGNAL PB H IS THE DATA INPUT LEAD TO THE PAUSE STATE WORKING FLIP-FLOP.  THE
                                ; TEST WILL NOW PULSE THE SIGNAL XCAS H.  WHEN A PULSE IS ISSUED ON THE SIGNAL
                                ; XCAS H AND THE SIGNAL PB H IS ASSERTED LOW, THE PAUSE STATE SYNC FLIP-FLOP WILL
                                ; BE CLOCKED TO A ZERO.  THE SIGNAL XCAS H WILL ALSO CLOCK THE PAUSE STATE WORK-
                                ; ING FLIP-FLOP TO A ONE.
                                ;--

020046                                  BGNTST
020046                          T32::
020046  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

020052                                  BGNSEG
020052  104404                          TRAP    C$BSEG

                                ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

020054  004737  007006                JSR     PC,SLMODR               ;SELECT MODE REG VIA GDAL BITS 2:0

                                ;LOAD, READ AND CHECK MODE REGISTER WITH A DATA PATTERN OF ALL ZEROES

020060  005037  002342                  CLR     R6LOAD                  ;SETUP TO CLEAR ALL BITS IN MODE REG
020064  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
020070  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
020072                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO ZERO
020072  104455                          TRAP    C$ERDF
020074  000004                          .WORD   4
020076  002631                          .WORD   MODREG
020100  005020                          .WORD   R06ERR
020102                                  CKLOOP
020102  104406                          TRAP    C$CLP1

                                ;GO PULSE BRKRES L BY SETTING AND CELARING ADAL0 IN THE ADAL REGISTER.
                                ;ALL OTHER ADAL REGISTER BITS WILL BE SET TO A ZERO.

020104  005037  002330          1$:     CLR     R2LOAD                  ;SETUP TO CLEAR ALL ADAL BITS
020110  004737  007772                  JSR     PC,BRKRES               ;GO 0 ADAL REG AND PULSE ADAL0 H

                                ;PULSE INVD L BY SETTING AND CLEARING VDAL2 H IN THE VDAL REGISTER. THE
                                ;SIGNAL INVD L WILL CAUSE THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                ;CLEARED.

020114  005037  002334                  CLR     R4LOAD                  ;SETUP TO CLEAR ALL OTHER R.W BITS
020120  004737  007712                  JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
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7351
7352                                        ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
7353
7354  020124  004737  006754                JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
7355
7356                                        ;LOAD, READ AND CHECK THE HDAL REGISTER WITH HDAL2 H SET TO A ONE.
7357                                        ;HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING
7358                                        ;AND CONTROL SIGNALS.
7359
7360  020130  012737  000004  002342        MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
7361  020136  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK THE HDAL REG
7362  020142  001405                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
7363  020144                                ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EPXECTED
7364  020144  104455                        TRAP    C$ERDF
7365  020146  000004                        .WORD   4
7366  020150  002605                        .WORD   HDALRG
7367  020152  005020                        .WORD   R06ERR
7368  020154                                CKLOOP
7369  020154  104406                        TRAP    C$CLP1
7370
7371                                        ;SET VDAL7 H TO A ONE TO CAUSE THE SIGNAL FETCT H TO BE ASSERTED HIGH.
7372
7373  020156  012737  000200  002334  2$:   MOV     #VDAL7,R4LOAD           ;SETUP BIT TO BE LOADED
7374  020164  004737  006640                JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK THE VDAL REG
7375  020170  001405                        BEQ     3$                      ;IF LOADED OK THEN CONTINUE
7376  020172                                ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
7377  020172  104455                        TRAP    C$ERDF
7378  020174  000003                        .WORD   3
7379  020176  002537                        .WORD   VDALRG
7380  020200  005004                        .WORD   R4EROR
7381  020202                                CKLOOP
7382  020202  104406                        TRAP    C$CLP1
7383
7384                                        ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  THE SIGNAL
7385                                        ;XRAS H WILL CLOCK THE STATE OF FETCT H, WHICH IS HIGH, INTO THE EDFET
7386                                        ;FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE HIGH STATE.  THE
7387                                        ;SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH IS LOW, INTO THE
7388                                        ;PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L TO THE HIGH STATE.
7389                                        ;THE SIGNAL SOP H WILL BE ASSERTED HIGH AS A RESULT OF PAUSE L BEING
7390                                        ;ASSERTED HIGH.  WHEN SOP H AND EDFET H ARE ASSERTED HIGH, THE PAUSE
7391                                        ;STATE WORKING FLIP-FLOP WILL BE SET TO A ONE.  WHEN SOP H AND EDFET H
7392                                        ;ARE ASSERTED HIGH, THE SIGNAL PB H WILL BE ASSERTED HIGH.  THE SIGNAL
7393                                        ;PB H IS THE DATA INPUT LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
7394
7395  020204  004737  007272          3$:   JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
7396
7397                                        ;SET VDAL7 H TO A ZERO TO CAUSE THE SIGNAL FETCT H TO BE ASSERTED LOW.
7398                                        ;CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP WAS SET TO A ONE AS A
7399                                        ;RESULT OF SOP H AND EDFET H BEING ASSERTED HIGH.
7400
7401  020210  042737  000200  002334        BIC     #VDAL7,R4LOAD           ;SETUP TO CLEAR FETCT H
7402  020216  013737  002334  002336        MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO DATA EXPECTED
7403  020224  052737  001000  002336        BIS     #VDAL9,R4GOOD           ;SETUP TO EXPECT PSMW H TO BE A ONE
7404  020232  004737  006646                JSR     PC,LDRD4R               ;GO LOAD, READ AND CHECK VDAL REG
7405  020236  001405                        BEQ     4$                      ;IF LOADED AND CHECK OK THEN CONTINUE
7406  020240                                ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
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7407  020240  104455                          TRAP    C$ERDF
7408  020242  000003                          .WORD   3
7409  020244  002537                          .WORD   VDALRG
7410  020246  005004                          .WORD   R4EROR
7411  020250                                  CKLOOP
7412  020250  104406                          TRAP    C$CLP1
7413
7414                                          ;TOGGLE THE SIGNAL XPI L BY SETTING AND CLEARINC HDAL15 H.  A PULSE ON
7415                                          ;XPI L WILL CLEAR THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H
7416                                          ;TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL PB H, WHICH
7417                                          ;IS THE DATA INPUT LEAD TO THE PAUSE STATE SYNC FLIP-FLOP, WILL BE
7418                                          ;ASSERTED LOW.
7419
7420  020252  004737  007502          4$:     JSR     PC,XPI                  ;GO PULSE XPI L VIA HDAL15 H
7421
7422                                          ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  THE SIGNAL
7423                                          ;XCAS H WILL CLOCK THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO AS A RESULT
7424                                          ;OF PB H BEING ASSERTED LOW.  THE SIGNAL XCAS H WILL ALSO CLOCK THE
7425                                          ;PAUSE STATE WORKING FLIP-FLOP TO A ONE AS A RESULT OF THE SIGNALS
7426                                          ;PSMW H, EPFN L, AND EP8N L BEING ASSERTED HIGH.
7427
7428  020256  004737  007376                  JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
7429
7430                                          ;READ THE VDAL REGISTER TO CHECK THAT XPI L HAD CLEARED THE EDFET FLIP-
7431                                          ;FLOP.  IF XPI L HAD FAILED TO CLEAR THE EDFET FLIP-FLOP, THEN THE PAUSE
7432                                          ;STATE SYNC FLIP-FLOP WILL BE SET TO A ONE.  CHECK THAT XCAS H CLOCKED
7433                                          ;THE PAUSE STATE WORKING FLIP-FLOP TO A ONE.
7434
7435  020262  004737  006654                  JSR     PC,READR4               ;GO READ AND CHECK THE VDAL REGISTER
7436  020266  001405                          BEQ     5$                      ;IF NO CHANGE THE CONTINUE
7437  020270                                  ERRDF   2,VDALRG,R4EROR         ;XPI L PROBABLY FAILED TO ZERO EDFET F/F
7438  020270  104455                          TRAP    C$ERDF
7439  020272  000003                          .WORD   3
7440  020274  002537                          .WORD   VDALRG
7441  020276  005004                          .WORD   R4EROR
7442  020300                                  CKLOOP
7443  020300  104406                          TRAP    C$CLP1
7444
7445                                          ;GO PULSE INVD L VIA VDAL2 H TO CLEAR THE PAUSE STATE WORKING FLIP-FLOP.
7446
7447  020302  005037  002334          5$:     CLR     R4LOAD                  ;SETUP TO EXPECT ALL READ ONLY BITS A 0
7448  020306  004737  007712                  JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
7449
7450  020312                                  ENDSEG
7451  020312                          10000$:
7452  020312  104405                          TRAP    C$ESEG
7453  020314                                  ENDTST
7454  020314                          L10062:
7455  020314  104401                          TRAP    C$ETST
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```
                                .SBTTL  TEST 33: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - OLD FJA

                                ;++
                                ; THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 8 BIT ADDRESS MODE.  THE
                                ; PAUSE  STATE  WORKING  FLIP - FLOP'S , PAUSE  STATE  WORKING , PAUSE
                                ; STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB AND 8 BIT ADDRESS HB WILL
                                ; BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND
                                ; CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H.  THE SIGNALS ADAL4 H AND
                                ; AND ADAL8 H WILL BE SET TO A ZERO DURING THIS TEST.  ADAL4 H ON A ZERO WILL
                                ; PUT THE PAUSE STATE MACHINE IN PAUSE MODE.  ADAL8 H ON A ZERO WILL DISABLE THE
                                ; TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK.  ADALO H WILL BE SET AND CLEARED TO
                                ; CLEAR THE BREAK LOGIC.  WITH THE TIMEOUT BREAK DISABLED AND THE BREAK LOGIC
                                ; CLEARED, THE SIGNAL BRK H WILL BE A ZERO.  MR BIT 11 WILL BE SET TO A ONE
                                ; IN THE MODE REGISTER TO ENABLE 8 BIT ADDRESS MODE.
                                ;
                                ; THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE OLD
                                ; FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS IN 8 BIT ADDRESS
                                ; MODE.  THE OLD FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA
                                ; PATTERNS: 125125, 052652, 000377, 177400, 125252, 052525, 177777, AND 000000.
                                ; THE OLD FORCE JUMP ADDRESS REGISTER GETS ITS DATA FROM THE DIAGNOSTIC ADDRESS
                                ; REGISTER WHICH IS ENABLED TO THE ADDRESS BUS DURING THIS TEST.
                                ;--

020316                                  BGNTST
020316                          T33::
020316  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
020322  012701  021562                  MOV     #20$,R1                 ;GET ADDRESS OF OLD FJA DATA TABLE
020326  012702  000010                  MOV     #8.,R2                  ;NUMBER OF DATA PATTERNS TO BE TESTE

020332                          1$:     BGNSEG
020332  104404                          TRAP    C$BSEG

                                ;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDAL0
                                ;TO A ZERO.

020334  004737  007006                  JSR     PC,SLMODR               ;GO SELECT MODE REG VIA CONTROL REG 0

                                ;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH 4000.  MR   T 11
                                ;ON A ONE WILL ENABLE 8 BIT ADDRESS SELECTION TO THE PAUSE STATE MACHINE

020340  012737  004000  002342          MOV     #MR11,R6LOAD            ;SETUP TO SET MR BIT 11
020346  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL 16 BITS
020352  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK MODE REGISTER
020356  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
020360                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO 0
020360  104455                          TRAP    C$ERDF
020362  000004                          .WORD   4
020364  002631                          .WORD   MODREG
020366  005020                          .WORD   R06ERR
020370                                  CKLOOP
020370  104406                          TRAP    C$CLP1

                                ;SET GDAL1 AND GDAL0 TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
                                ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

020372  004737  006754          2$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
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7512
7513                                    ;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
7514                                    ;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
7515                                    ;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
7516                                    ;BUS.  HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
7517                                    ;TIMING AND CONTROL SIGNALS.
7518
7519  020376  012737  001004  002342          MOV     #HDAL9!HDAL2,R6LOAD     ;SETUP BITS TO BE LOADED
7520  020404  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
7521  020410  0014C5                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
7522  020412                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REG NOT EQUAL TO EXPECTED
7523  020412  104455                          TRAP    C$ERDF
7524  020414  000004                          .WORD   4
7525  020416  002605                          .WORD   HDALRG
7526  020420  005020                          .WORD   R06ERR
7527  020422                                  CKLOOP
7528  020422  104406                          TRAP    C$CLP1
7529
7530                                    ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
7531                                    ;ZEROES.  ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
7532                                    ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.
7533
7534  020424  004737  007072      3$:         JSR     PC,SLDADR               ;GO SELECT DIAG ADDRESS REG VIA GDAL 2:0
7535
7536                                    ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
7537                                    ;FOLLOWING DATA PATTERNS: 125125, 052652, 000377, 177400, 125252,
7538                                    ;052525, 177777 AND 000000.
7539
7540  020430  011137  002342                  MOV     (R1),R6LOAD             ;GET DATA PATTERN FROM TABLE
7541  020434  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK DIAG ADDR REG
7542  020440  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
7543  020442                                  ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDRESS REG NOT EQUAL EXPECTED
7544  020442  104455                          TRAP    C$ERDF
7545  020444  000004                          .WORD   4
7546  020446  002735                          .WORD   ADDRRG
7547  020450  005020                          .WORD   R06ERR
7548  020452                                  CKLOOP
7549  020452  104406                          TRAP    C$CLP1
7550
7551                                    ;LOAD, READ AND CHECK ADAL REGISTER.  ADAL0 WILL BE SET AND CLEARED
7552                                    ;TO CLEAR THE BREAK LOGIC.  ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT
7553                                    ;BREAK SIGNAL FROM CAUSING A BREAK CONDITION.  ADAL4 H ON A ZERO WILL
7554                                    ;CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE WHEN THE
7555                                    ;SIGNAL XRAS H IS PULSED.
7556
7557  020454  005037  002330      4$:         CLR     R2LOAD                  ;SETUP ALL BITS TO BE CLEARED
7558  020460  004737  007772                  JSR     PC,BRKRES               ;GO PULSE ADAL0 H TO CLEAR BREAK LOGIC
7559
7560                                    ;SET VDAL2 H TO A ONE AND THEN ZERO.  VDAL2 H ON A ONE WILL CLEAR THE
7561                                    ;PAUSE STATE MACHINE FLIP-FLOPS AND THE FLIP-FLOPS, TAKE NEW FORCE JUMP
7562                                    ;ADDRESS AND THIS CYCLE GETS NEW ADDRESS.
7563
7564  020464  005037  002334                  CLR     R4LOAD                  ;SETUP TO CLEAR ALL VDAL BITS
7565  020470  004737  007712                  JSR     PC,CLRPSM               ;GO PULSE VDAL2 H TO 0 PAUSE STATE F/F'S
7566
7567                                    ;SELECT THE NEW FORCE JUMP ADDRESS REGISTER BY SETTING GDAL1 H TO A ONE
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                                        ;AND GDAL BITS 2 AND 0 TO ZEROES.  ON A WRITE COMMAND TO CONTROL REG 6,
                                        ;DATA WILL BE LOADED INTO THE NEW FORCE JUMP ADDRESS REGISTER AND THE
                                        ;TAKE NEW FORCE JUMP ADRESS FLIP-FLOP WILL BE SET

020474  004737  007040                  JSR     PC,SLFJAR               ;SELECT NEW FJA VIA GDAL BITS 2:0

                                        ;ISSUE A WRITE COMMAND TO CONTROL REGISTER 6 TO WRITE THE DATA PATTERN
                                        ;146063 INTO THE NEW FORCE JUMP ADDRESS REGISTER VIA THE SIGNALS WPT1 LB
                                        ;H AND WPT1 HB H.  THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL ALSO
                                        ;GET SET VIA THE SIGNAL WPT1 LB H.  THE NEW FORCE JUMP ADDRESS REGISTER
                                        ;IS WRITTEN WITH DATA TO CHECK THAT THE CORRECT FORCE JUMP ADDRESS REG-
                                        ;ISTER IS ENABLED TO THE EODAL BUS WHEN THE 8 BIT ADDRESS FLIP-FLOPS
                                        ;ARE SET TO ONES.  THE OLD FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED
                                        ;TO THE EODAL BUS DURING THIS TEST.

020500  012777  146063  161600          MOV     #146063,@REG6           ;WRITE NEW FJA WITH DATA VIA WPT1

                                        ;READ THE VDAL REGISTER TO CHECK THAT THE TAKE NEW FORCE JUMP ADDRESS
                                        ;FLIP-FLOP WAS SET TO A ONE VIA WPT1 LB H.  THE FLIP-FLOP WILL BE READ
                                        ;BACK AS THE SIGNAL TNFJ H.

020506  052737  100000  002336          BIS     #VDAL15,R4GOOD          ;SETUP TO EXPECT TNFJ H TO BE A 1
020514  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
020520  001405                          BEQ     5$                      ;IF TNFJ H SET THEN CONT
020522                                  ERRDF   3,VDALRG,R4EROR         ;TNFJ H PROBABLY NOT SET
020522  104455                          TRAP    C$ERDF
020524  000003                          .WORD   3
020526  002537                          .WORD   VDALRG
020530  005004                          .WORD   R4EROR
020532                                  CKLOOP
020532  104406                          TRAP    C$CLP1

                                        ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE (1).
                                        ;SET VDAL2 H TO A ONE AND THEN ZERO TO CLEAR THE PAUSE STATE MACHINE
                                        ;AND THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP.

020534  012737  000200  002334  5$:     MOV     #VDAL7,R4LOAD           ;SETUP BIT TO SET FETCT H TO HIGH STATE
020542  004737  007712                  JSR     PC,CLRPSM               ;SET FETCT H HIGH AND PULSE VDAL2 H

                                        ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
                                        ;TO ONES.  BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
                                        ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L,

020546  004737  006754                  JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL 2:0

                                        ;TOGGLE THE SIGNAL XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
                                        ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
                                        ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
                                        ;HIGH STATE.  THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
                                        ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
                                        ;TO THE HIGH STATE.  THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
                                        ;SIGNAL PAUSE L IS ASSERTED HIGH.  WHEN SOP H AND EDFET H ARE ASSERTED
                                        ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
                                        ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
                                        ;PSMW H WILL BE ASSERTED HIGH.  THE SIGNAL PSMW H IS READ IN THE VDAL
                                        ;REGISTER AS VDAL9 H.  WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
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                                        ;SIGNAL PB H WILL BE ASSERTED HIGH.  THE SIGNAL PB H IS THE DATA INPUT
                                        ;LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
                                        ;
                                        ;THE SIGNAL XRAS H WILL CAUSE THE SIGNAL RASP H TO BE PULSED. WHEN THE
                                        ;SIGNAL RASP H IS PULSED AND THE SIGNAL EDFET H IS ASSERTED HIGH, A
                                        ;PULSE WILL BE ISSUED ON THE SIGNAL DFET H.  THE SIGNAL DFET H WILL
                                        ;CLOCK THE ADDRESS BUS INTO THE OLD FORCE JUMP ADDRESS REGISTER.  AT THE
                                        ;PRESENT TIME THE DIAGNOSTIC ADDRESS REGISTER IS ENABLED ONTO THE
                                        ;ADDRESS BUS, THEREFORE THE OLD FORCE JUMP ADDRESS REGISTER WILL BE
                                        ;LOADED WITH THE DATA FROM THE DIAGNOSTIC ADDRESS REGISTER.

020552  012737  001004  002342          MOV     #HDAL9!HDAL2,R6LOAD     ;SETUP BITS PREVIOUSLY LOADED
020560  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS H VIA SIGNAL HDAL12

                                        ;CLEAR VDAL7 H IN THE VDAL REGISTER THUS SETTING THE SIGNAL FETCT H TO
                                        ;THE LOW STATE.  CHECK THE PAUSE STATE MACHINE TO BE IN THE FOLLOWING
                                        ;STATE AS A RESULT OF FETCT H AND SOP H BEING ASSERTED HIGH.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB H - EP8G H - 0
                                        ;    8 BIT ADDRESS HB H - EP8N H - 0

020564  042737  000200  002334          BIC     #VDAL7,R4LOAD           ;SETUP TO CLEAR FETCT H
020572  013737  002334  002336          MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
020600  052737  001000  002336          BIS     #VDAL9,R4GOOD           ;EXPECT PSMW H TO BE SET TO A 1
020606  004737  006646                  JSR     PC,LDRD4R               ;GO LOAD, READ AND CHECK VDAL REG
020612  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
020614                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
020614  104455                          TRAP    C$ERDF
020616  000003                          .WORD   3
020620  002537                          .WORD   VDALRG
020622  005004                          .WORD   R4EROR
020624                                  CKLOOP
020624  104406                          TRAP    C$CLP1

                                        ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
                                        ;SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
                                        ;SIGNAL "PB H", WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP,
                                        ;THUS SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE.  THE SIGNAL
                                        ;XCAS H WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-
                                        ;FLOP (0) INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS CLOCKING THAT
                                        ;FLIP-FLOP TO A ZERO.

020626  004737  007410          6$:     JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H

                                        ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                        ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING SET HIGH.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EP8N H - 0

020632  052737  002000  002336          BIS     #VDAL10,R4GOOD          ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
020640  004737  006654                  JSR     PC,READR4               ;GO READ AND CHECK PAUSE STATE MACHINE
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7680  020644  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
7681  020646                                  ERRDF   5,VDALRG,R4EROR         ;EPSF H PROBABLE NOT SET IN VDAL REG
7682  020646  104455                          TRAP    C$ERDF
7683  020650  000003                          .WORD   3
7684  020652  002537                          .WORD   VDALRG
7685  020654  005004                          .WORD   R4EROR
7686  020656                                  CKLOOP
7687  020656  104406                          TRAP    C$CLP1
7688
7689                                          ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE LOW
7690                                           BYTE OF THE 16 BIT INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE
7691                                          ;EODAL BUS AT THE SAME TIME.  ON A READ COMMAND TO CONTROL REGISTER 6,
7692                                          ;THE EODAL BUS WILL BE ENABLED TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
7693
7694  020660  004737  007122          7$:     JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
7695
7696                                          ;WHEN THE SIGNAL XCAS H IS ASSERTED HIGH AND THE SIGNAL PSMW H IS
7697                                          ;ASSERTED TO THE HIGH STATE, THE SIGNAL ACAS H WILL BE ASSERTED HIGH.
7698                                          ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH, THE PAUSE STATE SYNC FLIP-
7699                                          ;FLOP IS SET TO A ONE, AND MODE REGISTER BIT 11 IS A ONE (8 BIT MODE),
7700                                          ;THE SIGNAL EDRL H WILL BE ASSERTED LOW, THUS ENABLING THE LOW BYTE OF
7701                                          ;THE 16 BIT INSTRUCTION REGISTER ONTO THE EODAL BUS.  THE HIGH BYTE OF
7702                                          ;THE 16 BIT INSTRUCTION REGISTER WILL BE DISABLED ON THE EODAL BUS.
7703                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH GDAL BITS 2:0
7704                                          ;SET TO ONES, A PULSE WILL BE ISSUED ON THE SIGNAL RPT7 L.  THE SIGNAL
7705                                          ;RPT7 L WILL READBACK THE EODAL BUS ONTO THE LSI-11 BUS.
7706
7707  020664  012737  000137  002342          MOV     #137,R6LOAD             ;SETUP EXPECTED LOW BYTE DATA
7708  020672  012737  177400  002346          MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE
7709  020700  004737  006700                  JSR     PC,READR6               ;GO READ LOW BYTE OF INSTR REG ON EODAL
7710  020704  001405                          BEQ     8$                      ;IF INSTR = "JMP" THEN CONTINUE
7711  020706                                  ERRDF   4,IEODAL,R06ERR         ;EODAL BUS ERROR OR 8 BIT LB INSTR ERROR
7712  020706  104455                          TRAP    C$ERDF
7713  020710  000004                          .WORD   4
7714  020712  003034                          .WORD   IEODAL
7715  020714  005020                          .WORD   R06ERR
7716  020716                                  CKLOOP
7717  020716  104406                          TRAP    C$CLP1
7718
7719                                          ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 H TO A ZERO AND GDAL BITS
7720                                          ;1 AND 0 TO A ONE.
7721
7722  020720  004737  006754          8$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
7723
7724                                          ;SET THE SIGNAL XCAS H TO THE LOW STATE BY CLEARING HDAL13 H IN HDAL
7725                                          ;REGISTER.
7726
7727  020724  012737  021004  002342          MOV     #HDAL13!HDAL9!HDAL2,R6LOAD ;BITS THAT WERE PREVIOUSLY SET
7728  020732  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
7729  020736  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H
7730
7731                                          ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H.  THIS IS DONE
7732                                          ;TO SIMULATE A MACHINE CYCLE
7733
7734  020742  004737  007502                  JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
7735
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                                        ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
                                        ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
                                        ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
                                        ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
                                        ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
                                        ;AND RASP L WILL BE PULSED.
                                        ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
                                        ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.

020746  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS H BY HDAL12

                                        ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
                                        ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB  - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EP8N H - 0

020752  004737  006654                  JSR     PC,READR4               ;CHECK VDAL AND PAUSE STATE MACHINE
020756  001405                          BEQ     9$                      ;IF OK THEN CONTINUE
020760                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
020760  104455                          TRAP    C$ERDF
020762  000003                          .WORD   3
020764  002537                          .WORD   VDALRG
020766  005004                          .WORD   R4EROR
020770                                  CKLOOP
020770  104406                          TRAP    C$CLP1

                                        ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
                                        ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE LEVEL OF THE
                                        ;SIGNAL "PB H", WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
                                        ;CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO.  THE SIGNAL XCAS H
                                        ;WILL CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP (1)
                                        ;INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS SETTING THAT FLIP-FLOP
                                        ;TO A ONE.  THE SIGNAL XCAS H WILL ALSO CLOCK THE PREVIOUS STATE OF THE
                                        ;8 BIT INSTRUCTION HB FLIP-FLOP (0) INTO THE 8 BIT ADDRESS LB FLIP-FLOP.
                                        ;THUS CLOCKING THAT FLIP-FLOP TO A ZERO.

020772  004737  007410          9$:     JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H

                                        ;READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
                                        ;FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING SET HIGH
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 1
                                        ;    8 BIT ADDRESS LB - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EPFN H - 0

020776  042737  002000  002336          BIC     #VDAL10,R4GOOD          ;CLEAR BIT FOR EPSF H
021004  052737  010000  002336          BIS     #VDAL12,R4GOOD          ;SET BIT FOR EP8F H
021012  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
021016  001405                          BEQ     10$                     ;IF OK THEN CONTINUE
021020                                  ERRDF   3,VDALRG,R4EROR         ;EP8F H PROBABLY NOT SET IN VDAL REG
021020  104455                          TRAP    C$ERDF
021022  000003                          .WORD   3
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7792  021024  002537                          .WORD   VDALRG
7793  021026  005004                          .WORD   R4EROR
7794  021030                                  CKLOOP
7795  021030  104406                          TRAP    C$CLP1
7796
7797                                          ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE HIGH
7798                                          ;BYTE OF THE 16 BIT INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE
7799                                          ;EODAL BUS AT THIS TIME.  ON A READ COMMAND TO CONTROL REGISTER 6,
7800                                          ;THE EODAL BUS WILL BE ENABLED TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
7801
7802  021032  004737  007122          10$:    JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
7803
7804                                          ;WHEN THE SIGNAL XCAS H IS ASSERTED HIGH AND THE PAUSE STATE WORKING
7805                                          ;FLIP-FLOP IS SET TO A ONE, THE SIGNAL ACAS H WILL BE ASSERTED HIGH.
7806                                          ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH AND THE 8 BIT INSTRUCTION HB
7807                                          ;FLIP-FLOP IS SET TO A ONE, THE SIGNAL ED8H H WILL BE ASSERTED HIGH,
7808                                          ;THUS ENABLING THE HIGH BYTE OF THE 16 BIT INSTRUCTION REGISTER (000)
7809                                          ;ONTO THE LOW BYTE OF THE EODAL BUS.  WHEN A READ COMMAND IS ISSUED TO
7810                                          ;CONTROL REGISTER 6 WITH GDAL BITS 2:0 SET TO ONES, A PULSE WILL BE
7811                                          ;ISSUED ON THE SIGNAL RPT7 L.  THE SIGNAL RPT7 L WILL READBACK THE
7812                                          ;EODAL BUS ONTO THE LSI-11 BUS.
7813
7814  021036  005037  002342                  CLR     R6LOAD                  ;EXPECT HIGH BYTE TO BE ZERO
7815  021042  012737  177400  0023.6         MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE ON READ
7816  021050  004737  006700                  JSR     PC,READR6               ;GO READ 8 BIT HIGH BYTE INSTRUCTION
7817                                                                          ;ON THE EODAL BUS AS LOW BYTE
7818  021054  001405                          BEQ     11$                     ;IF INSTRUCTION EQUALS 0 THEN CONT
7819  021056                                  ERRDF   4,IEODAL,R06ERR         ;EODAL BUS OR 8 BIT HB INSTR ERROR
7820  021056  104455                          TRAP    C$ERDF
7821  021060  000004                          .WORD   4
7822  021062  003034                          .WORD   IEODAL
7823  021064  005020                          .WORD   R06ERR
7824  021066                                  CKLOOP
7825  021066  104406                          TRAP    C$CLP1
7826
7827                                          ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 H TO A ZERO AND GDAL BITS
7828                                          ;1 AND 0 TO ONES.
7829
7830  021070  004737  006754          11$:    JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0
7831
7832                                          ;SET THE SIGNAL XCAS H TO A ZERO BY CLEARING HDAL13 H IN THE HDAL
7833                                          ;REGISTER.
7834
7835  021074  012737  021004  002342          MOV     #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
7836  021102  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
7837  021106  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H
7838
7839                                          ;TOGGLE THE SIGNAL XPI H BY PULSING THE SIGNAL HDAL15 H.  THIS IS DONE
7840                                          ;TO SIMULATE A MACHINE CYCLE.
7841
7842  021112  004737  007502                  JSR     PC,A I                  ;GO PULSE XPI H VIA HDAL15 H
7843
7844                                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
7845                                          ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
7846                                          ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
7847                                          ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
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                                        ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
                                        ;AND RASP L WILL BE PULSED.
                                        ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
                                        ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.

021116  004737  007272                JSR     PC,XRAS                 ;PULSE XRAS VIA THE SIGNAL HDAL12

                                        ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
                                        ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
                                        ;NO CHANGES SHOULD OCCUR IN THE PAUSE STATE MACHINE WHEN XRAS H PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 1
                                        ;    8 BIT ADDRESS LB - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EP8N H - 0

021122  004737  006654                JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
021126  001405                        BEQ     12$                     ;IF OK THEN CONTINUE
021130                                ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE REGISTERS CHANGED
021130  104455                        TRAP    C$ERDF
021132  000003                        .WORD   3
021134  002537                        .WORD   VDALRG
021136  005004                        .WORD   R4EROR
021140                                CKLOOP
021140  104406                        TRAP    C$CLP1

                                        ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
                                        ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE OUTPUT OF THE
                                        ;PAUSE STATE SYNC FLIP-FLOP (0) INTO THE 8 BIT INSTRUCTION HB FLIP-
                                        ;FLOP, THUS CLEARING THE 8 BIT INSTRUCTION HB FLIP-FLOP.  THE PREVIOUS
                                        ;OUTPUT OF THE 8 BIT INSTRUCTION HB FLIP-FLOP (1) WILL BE CLOCKED INTO
                                        ;THE 8 BIT ADDRESS LB FLIP-FLOP THUS SETTING THE 8 BIT ADDRESS LB F/F.

021142  004737  007410        12$:    JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H

                                        ;READ VDAL REGISTER AND CHECK PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
                                        ;THE FOLLOWING STATE AS A RESULT OF XCAS H BEING SET HIGH.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB - EP8G H - 1
                                        ;    8 BIT ADDRESS HB - EP8N H - 0

021146  042737  010000  002336          BIC     #VDAL12,R4GOOD          ;SETUP TO EXPECT EP8F H TO BE 0
021154  052737  020000  002336          BIS     #VDAL13,R4GOOD          ;SETUP TO EXPECT EP8G H TO BE 1
021162  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
021166  001405                        BEQ     13$                     ;IF OK THEN CONTINUE
021170                                ERRDF   3,VDALRG,R4EROR         ;EP8F H PROBABLY NOT 0 OR EP8G H NOT SET
021170  104455                        TRAP    C$ERDF
021172  000003                        .WORD   3
021174  002537                        .WORD   VDALRG
021176  005004                        .WORD   R4EROR
021200                                CKLOOP
021200  104406                        TRAP    C$CLP1

                                        ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE LOW BYTE
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                                        ;OF THE OLD FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL
                                        ;BUS AT THIS TIME.  ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL
                                        ;BUS WILL BE READBACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
                                
021202  004737  007122          13$:    JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
                                
                                        ;ON THE FIRST PULSE OF XRAS H IN THIS TEST WHEN THE SIGNAL EDFET H WAS
                                        ;SET HIGH, THE OLD FORCE JUMP ADDRESS REGISTER SHOULD HAVE BEEN LOADED
                                        ;WITH THE DATA PATTERN IN THE DIAGNOSTIC ADDRESS REGISTER VIA THE
                                        ;CLOCKING SIGNAL DFET H.  AT THIS POINT IN TIME, THE LOW BYTE OF
                                        ;THE OLD FORCE JUMP ADDRESS REGISTER WILL BE ENABLED TO THE EODAL BUS
                                        ;VIA THE SIGNAL OEARL L.  THIS SIGNAL IS ASSERTED LOW AS A RESULT OF
                                        ;THE ''GET NEW ADDRESS'' FLIP - FLOP BEING CLEARED AND THE SIGNAL
                                        ;EARL H BEING ASSERTED HIGH.  THE ''GET NEW ADDRESS'' FLIP - FLOP
                                        ;WAS CLEARED AT THE BEGINNING OF THIS TEST WHEN VDAL2 H WAS SET HIGH.
                                        ;THE SIGNAL EARL H IS ASSERTED HIGH AS A RESULT OF THE 8 BIT ADDRESS LB
                                        ;FLIP-FLOP BEING SET AND THE SIGNAL ACAS H BEING ASSERTED HIGH.  THE
                                        ;FOLLOWING SECTION WILL READ AND CHECK THAT THE LOW BYTE OF THE OLD
                                        ;FORCE JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL BUS. THE EODAL BUS
                                        ;WILL BE READ BACK VIA THE SIGNAL RPT7 L WHEN A READ COMMAND IS ISSUED
                                        ;TO CONTROL REGISTER 6.
                                        ;
                                        ;IF THE LOW BYTE DATA READ BACK FROM THE EODAL BUS EQUALS 063, THEN
                                        ;THE NEW FORCE JUMP ADDRESS REGISTER WAS PROBABLY ENABLED TO THE EODAL
                                        ;BUS INSTEAD OF THE OLD FORCE JUMP ADDRESS REGISTER.  THE DATA PATTERN
                                        ;146063 WAS WRITTEN INTO THE NEW FORCE JUMP ADDRESS REGISTER AT THE
                                        ;BEGINNING OF THE TEST.
                                
                                        MOV     (R1),R6LOAD             ;GET THE DATA LOADED INTO THE DIAG
                                                                        ;ADDRESS REGISTER
                                        BIC     #177400,R6LOAD          ;CLEAR UPPER BYTE
                                        MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE
                                        JSR     PC,READR6               ;READ LB OF OLD FJA ON EODAL BUS
                                        BEQ     14$                     ;IF OLD FLA OK THEN CONTINUE
                                        ERRDF   4,FEODAL,R06ERR         ;OLD FJA TO EODAL BUS ERROR
                                        TRAP    C$ERDF
                                        .WORD   4
                                        .WORD   FEODAL
                                        .WORD   R06ERR
                                        CKLOOP
                                        TRAP    C$CLP1
                                
                                        ;RESELECT THE HDAL REGISTER BY SETTING THE SIGNAL GDAL2 TO A ZERO AND
                                        ;GDAL BITS 1 AND 0 TO ONES.
                                
021246  004737  006754          14$:    JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0
                                
                                        ;SET XCAS H TO THE LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER.
                                
021252  012737  021004  002342          MOV     #HDAL13!HDAL9.HDAL2,R6LOAD ;SETUP BITS PREVIOULSY LOADED
021260  005037  002346                  CLR     R6MASK                  ;SETUP TO COMPARE ALL BITS
021264  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H
                                
                                        ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H.  THIS IS
                                        ;DONE TO SIMULATE A MACHINE CYCLE.
                                
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7960  021270  004737  007502                  JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
7961
7962                                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SE   NG AND CLEARING HDAL12 H.
7963                                          ;WITH THE SIGNAL FETCT H SET LOW AND A PU    BEING ISSUED ON XRAS H, THE
7964                                          ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
7965                                          ;FDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
7966                                          ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
7967                                          ;AND RASP L WILL BE PULSED.
7968                                          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
7969                                          ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
7970
7971  021274  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS VIA HDAL12 H
7972
7973                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
7974                                          ;BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
7975                                          ;    PAUSE STATE WORKING - PSMW H - 1
7976                                          ;    PAUSE STATE SYNC - EPSF H - 0
7977                                          ;    8 BIT INSTRUCTION HB - EP8F H   0
7978                                          ;    8 BIT ADDRESS LB - EP8G H - 1
7979                                          ;    8 BIT ADDRESS HB - EP8N H - 0
7980
7981  021300  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
7982  021304  001405                          BEQ     15$                     ;IF OK THEN CONTINUE
7983  021306                                  ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE MACHINE CHANGED BY XRAS H
7984  021306  104455                          TRAP    C$ERDF
7985  021310  000003                          .WORD   3
7986  021312  002537                          .WORD   VDALRG
7987  021314  005004                          .WORD   R4EROR
7988  021316                                  CKLOOP
7989  021316  104406                          TRAP    C$CLP1
7990
7991                                          ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
7992                                          ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE OUTPUT OF THE
7993                                          ;8 BIT INSTRUCTION HB FLIP-FLOP (0) INTO THE 8 BIT ADDRESS LB FLIP-
7994                                          ;FLOP THUS CLEARING THE 8 BIT ADDRESS LOW BYTE FLIP-FLOP.  THE
7995                                          ;PREVIOUS OUTPUT OF THE 8 BIT ADDRESS LB FLIP-FLOP (1) WILL BE
7996                                          ;CLOCKED INTO THE 8 BIT ADDRESS HB FLIP-FLOP THUS SETTING THE 8 BIT
7997                                          ;ADDRESS HB FLIP-FLOP TO A ONE.
7998
7999  021320  004737  007410          15$:    JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H
8000
8001                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
8002                                          ;BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING SET HIGH.
8003                                          ;    PAUSE STATE WORKING - PSMW H - 1
8004                                          ;    PAUSE STATE SYNC - EPSF H - 0
8005                                          ;    8 BIT INSTRUCTION HB - EP8F H - 0
8006                                          ;    8 BIT ADDRESS LB - EP8F H - 0
8007                                          ;    8 BIT ADDRESS HB - EP8N H - 1
8008
8009  021324  042737  020000  002336          BIC     #VDAL13,R4GOOD          ;SETUP TO EXPECT EP8G H TO BE A 0
8010  021332  052737  040000  002336          BIS     #VDAL14,R4GOOD          ;SETUP TO EXPECT EP8N H TO BE A 1
8011  021340  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
8012  021344  001405                          BEQ     16$                     ;IF OK THEN CONTINUE
8013  021346                                  ERRDF   3,VDALRG,R4EROR         ;EP8G H NOT 0 OR EP8N H NOT A 1
8014  021346  104455                          TRAP    C$ERDF
8015  021350  000003                          .WORD   3
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8016  021352  002537                          .WORD   VDALRG
8017  021354  005004                          .WORD   R4EROR
8018  021356                                  CKLOOP
8019  021356  104406                          TRAP    C$CLP1
8020
8021                                          ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE HIGH BYTE
8022                                          ;OF THE OLD FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL
8023                                          ;BUS AT THIS TIME.  ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL
8024                                          ;BUS WILL BE READBACK TO THE LSI-11 VIA THE SIGNAL RPT7 L.
8025
8026  021360  004737  007122          16$:    JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
8027
8028                                          ;ON THE FIRST PULSE OF XRAS H IN THIS TEST WHEN THE SIGNAL EDFET H
8029                                          ;WAS SET HIGH, THE OLD FORCE JUMP ADDRESS REGISTER SHOULD HAVE BEEN
8030                                          ;LOADED WITH THE DATA PATTERN IN THE DIAGNOSTIC ADDRESS REGISTER VIA
8031                                          ;THE CLOCKING SIGNAL DFET H.  AT THIS POINT IN TIME, THE HIGH BYTE
8032                                          ;OF THE OLD FORCE JUMP ADDRESS REGISTER WILL BE ENABLED TO THE EODAL
8033                                          ;BUS VIA THE SIGNAL OEA8H L.  THIS SIGNAL IS ASSERTED LOW AS A RESULT
8034                                          ;OF  THE  "GET  NEW  ADDRESS"  FLIP - FLOP  BEING  CLEARED  AND  THE
8035                                          ;THE  SIGNAL  EA8H H  BEING  ASSERTED  HIGH.  THE  "GET  NEW  ADDRESS"
8036                                          ;FLIP-FLOP WAS CLEARED AT THE BEGINNING OF THIS TEST BY THE SIGNAL
8037                                          ;VDAL2 H BEING SET AND CLEARED.  THE SIGNAL EA8H H IS ASSERTED HIGH
8038                                          ;AS A RESULT OF THE 8 BIT ADDRESS HB FLIP-FLOP BEING SET TO A ONE AND
8039                                          ;THE SIGNAL ACAS H BEING ASSERTED HIGH.  THE FOLLOWING SECTION WILL
8040                                          ;READ AND CHECK THAT THE HIGH BYTE OF THE OLD FORCE JUMP ADDRESS REG-
8041                                          ;ISTER  IS ENABLED TO THE EODAL BUS.  THE EODAL BUS WILL BE READ BY
8042                                          ;THE SIGNAL RPT7 L WHEN A READ COMMAND IS ISSUED TO CONTROL REG 6.
8043                                          ;
8044                                          ;IF THE DATA READ ON THE EODAL BUS EQUALS    , THEN THE NEW FORCE JUMP
8045                                          ;ADDRESS REGISTER WAS PROBABLY READ INSTEAD OF THE OLD FORCE JUMP
8046                                          ;ADDRESS REGISTER.  THE DATA PATTERN 146063 WAS WRITTEN INTO THE
8047                                          ;NEW FORCE JUMP ADDRESS REGISTER AT THE BEGINNING OF THIS TEST.
8048
8049  021364  011137  002342                  MOV     (R1),R6LOAD             ;GET DIAG ADDRESS REG DATA
8050  021370  000337  002342                  SWAB    R6LOAD                  ;SWAP HIGH BYTE WITH LOW BYTE
8051  021374  042737  177400  002342          BIC     #177400,R6LOAD          ;CLEAR LOW BYTE IN HIGH BYTE POSITION
8052  021402  012737  177400  002346          MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE ON READ
8053  021410  004737  006700                  JSR     PC,READR6               ;READ OLD FJA HB ON EODAL BUS
8054  021414  001405                          BEQ     17$                     ;OF OLD FLA OK THEN CONTINUE
8055  021416                                  ERRDF   4,FEODAL,R06ERR         ;OLD FLA HB TO EODAL BUS ERROR
8056  021416  104455                          TRAP    C$ERDF
8057  021420  000004                          .WORD   4
8058  021422  003147                          .WORD   FEODAL
8059  021424  005020                          .WORD   R06ERR
8060  021426                                  CKLOOP
8061  021426  104406                          TRAP    C$CLP1
8062
8063                                          ;RESELECT THE HDAL REGISTER BY SETTING THE SIGNAL GDAL2 TO A ZERO AND
8064                                          ;GDAL BITS 1 AND 0 TO ONES
8065
8066  021430  004737  006754          17$:    JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0
8067
8068                                          ;SET XCAS H TO THE LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER.
8069
8070  021434  012737  021004  002342          MOV     #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
8071  021442  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
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8072  021446  004737  007442                  JSR     PC,XCASL                ;SET XCAS L TO LOW STATE VIA HDAL13 H
8073
8074                                          ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H.  THIS IS DONE
8075                                          ;TO SIMULATE A MACHINE CYCLE.
8076
8077  021452  004737  007502                  JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
8078
8079                                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8080                                          ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8081                                          ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL
8082                                          ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
8083                                          ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
8084                                          ;AND RASP L WILL BE PULSED.
8085                                          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO BY RASP L
8086                                          ;WHEN THE SIGNALS EPFN L AND PSMW H ARE ASSERTED HIGH AND EP8N L IS
8087                                          ;ASSERTED LOW.  A SHORT TIME AFTER RASP L, THE SIGNAL PSMW H WILL BE
8088                                          ;ASSERTED LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP BEING
8089                                          ;CLEARED.
8090
8091  021456  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
8092
8093                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
8094                                          ;BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8095                                          ;     PAUSE STATE WORKING - PSMW H - 0
8096                                          ;     PAUSE STATE SYNC - EPSF H - 0
8097                                          ;     8 BIT INSTRUCTION HB - EP8F H - 0
8098                                          ;     8 BIT ADDRESS LB - EP8G H - 0
8099                                          ;     8 BIT ADDRESS HB - EP8N H - 1
8100
8101  021462  042737  001000  002336          BIC     #VDAL9,R4GOOD           ;SETUP TO EXPECT PSMW H TO BE A 0
8102  021470  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
8103  021474  001405                          BEQ     18$                     ;IF OK THEN CONTINUE
8104  021476                                  ERRDF   3,VDALRG,R4EROR         ;PSMW H F/F PROBABLY NOT 0
8105  021476  104455                          TRAP    C$ERDF
8106  021500  000003                          .WORD   3
8107  021502  002537                          .WORD   VDALRG
8108  021504  005004                          .WORD   R4EROR
8109  021506                                  CKLOOP
8110  021506  104406                          TRAP    C$CLP1
8111
8112                                          ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  THE SIGNAL
8113                                          ;XCAS H WILL CLOCK THE OUTPUT OF 8 BIT ADDRESS LB FLIP-FLOP (G) INTO THE
8114                                          ;8 ADDRESS HB FLIP-FLOP THUS SETTING THE 8 BIT ADDRESS HB FLIP-FLOP TO
8115                                          ;A ZERO.
8116
8117  021510  004737  007376          18$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
8118
8119                                          ;READ THE VDAL REGISTER AND THE PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
8120                                          ;THE FOLLOWING STATES AS A RESULT OF XCAS H BEING PULSED.
8121                                          ;     PAUSE STATE WORKING - PSMW H - 0
8122                                          ;     PAUSE STATE SYNC - EPSF H - 0
8123                                          ;     8 BIT INSTRUCTION HB - EP8F H - 0
8124                                          ;     8 BIT ADDRESS LB - EP8G H - 0
8125                                          ;     8 BIT ADDRESS HB - EP8N H - 0
8126
8127  021514  042737  040000  002336          BIC     #VDAL14,R4GOOD          ;SETUP TO EXPECT EP8N H TO BE A 0
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8128  021522  004737  006654          JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
8129  021526  001405                  BEQ     19$                     ;IF OK THEN CONTINUE
8130  021530                          ERRDF   3,VDALRG,R4EROR         ;EP8N H PROBABLY NOT CLEARED
8131  021530  104455                  TRAP    C$ERDF
8132  021532  000003                  .WORD   3
8133  021534  002537                  .WORD   VDALRG
8134  021536  005004                  .WORD   R4EROR
8135  021540                          CKLOOP
8136  021540  104406                  TRAP    C$CLP1
8137
8138                                  ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
8139                                  ;THIS IS DONE TO FINISH THE MACHINE CYCLE.
8140
8141  021542  004737  007502  19$:    JSR     PC,XPI                  ;GO PULSE XPI VIA HDAL15 H
8142
8143  021546                          ENDSEG
8144  021546                  10000$:
8145  021546  104405                  TRAP    C$ESEG
8146  021550  005721                  TST     (R1)+                   ;UPDATE TABLE POINTER
8147  021552  005302                  DEC     R2                      ;CHECK IF ALL PATTERNS DONE
8148  021554  001412                  BEQ     21$                     ;IF YES THEN EXIT
8149  021556  000137  020332          JMP     1$                      ;DO NEXT PATTERN
8150
8151  021562  125125          20$:    .WORD   125125
8152  021564  052652                  .WORD   052652
8153  021566  000377                  .WORD   000377
8154  021570  177400                  .WORD   177400
8155  021572  125252                  .WORD   125252
8156  021574  052525                  .WORD   052525
8157  021576  177777                  .WORD   177777
8158  021600  000000                  .WORD   000000
8159
8160  021602                  21$:    ENDTST
8161  021602                  L10063:
8162  021602  104401                  TRAP    C$ETST
8163
```

```
                                        .SBTTL  TEST 34: PAUSE STATE MACHINE - 8 BIT ADDRESS - PAUSE MODE - NEW FJA

                                        ;++
                                        ; THIS TEST WILL CHECK THE PAUSE STATE MACHINE IN 8 BIT ADDRESS MODE.  THE
                                        ; PAUSE  STATE  MACHINE  FLIP - FLOP'S,  PAUSE  STATE  WORKING,  PAUSE
                                        ; STATE SYNC, 8 BIT INSTRUCTION HB, 8 BIT ADDRESS LB AND 8 BIT ADDRESS HB WILL
                                        ; BE CLOCKED TO ONES AND ZEROES BY PULSING THE SIGNALS XRAS H AND XCAS H AND
                                        ; CHANGING THE LOGIC LEVEL ON THE SIGNAL FETCT H.  THE SIGNALS ADAL4 H AND
                                        ; AND ADAL8 H WILL BE SET TO A ZERO DURING THIS TEST.  ADAL4 H ON A ZERO WILL
                                        ; PUT THE PAUSE STATE MACHINE IN PAUSE MODE.  ADAL8 H ON A ZERO WILL DISABLE THE
                                        ; TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK.  ADAL0 H WILL BE SET AND CLEARED TO
                                        ; CLEAR THE BREAK LOGIC.  WITH THE TIMEOUT BREAK DISABLED AND THE BREAK LOGIC
                                        ; CLEARED, THE SIGNAL BRK H WILL BE A ZERO.  MR BIT 11 WILL BE SET TO A ONE
                                        ; IN THE MODE REGISTER TO ENABLE 8 BIT ADDRESS MODE.
                                        ;
                                        ; THE TEST WILL ALSO CHECK THAT THE 16 BIT INSTRUCTION REGISTER AND THE NEW
                                        ; FORCE JUMP ADDRESS REGISTER ARE ENABLED TO THE EODAL BUS IN 8 BIT ADDRESS
                                        ; MODE.  THE NEW FORCE JUMP ADDRESS REGISTER IS TESTED WITH THE FOLLOWING DATA
                                        ; PATTERNS: 125125, 052652, 000377, 177400, 125252, 052525, 177777, AND 000000.
                                        ; THE NEW FORCE JUMP ADDRESS REGISTER IS LOADED WITH THE DATA AT THE BEGINNING
                                        ; OF THE TEST.
                                        ;--

021604                                          BGNTST
021604                                  T34::
021604  004737  005510                          JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
021610  012701  023134                          MOV     #22$,R1                 ;GET ADDRESS OF OLD FJA DATA TABLE
021614  012702  000010                          MOV     #8.,R2                  ;NUMBER OF DATA PATTERNS TO BE TESTED

021620                                  1$:     BGNSEG
021620  104404                                  TRAP    C$BSEG

                                                ;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDAL0
                                                ;TO A ZERO.

021622  004737  007006                          JSR     PC,SLMODR               ;GO SELECT MODE REG VIA CONTROL REG 0

                                                ;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH 4000.  MR BIT 11
                                                ;ON A ONE WILL ENABLE 8 BIT ADDRESS SELECTION TO THE PAUSE STATE MACHINE

021626  012737  004000  002342                  MOV     #MR11,R6LOAD            ;SETUP TO SET MR BIT 11
021634  005037  002346                          CLR     R6MASK                  ;SETUP TO CHECK ALL 16 BITS
021640  004737  006672                          JSR     PC,LDRDR6               ;LOAD, READ AND CHECK MODE REGISTER
021644  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021646                                          ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO 0
021646  104455                                  TRAP    C$ERDF
021650  000004                                  .WORD   4
021652  002631                                  .WORD   MODREG
021654  005020                                  .WORD   R06ERR
021656                                          CKLOOP
021656  104406                                  TRAP    C$CLP1

                                                ;SET GDAL1 AND GDAL0 TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
                                                ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

021660  004737  006754                  2$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS _ 0
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8220
8221                                    ;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
8222                                    ;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
8223                                    ;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
8224                                    ;BUS.  HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
8225                                    ;TIMING AND CONTROL SIGNALS.
8226
8227  021664  012737  001004  002342        MOV     #HDAL9!HDAL2,R6LOAD     ;SETUP BITS TO BE LOADED
8228  021672  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
8229  021676  001405                        BEQ     3$                      ;IF LOADED OK THEN CONTINUE
8230  021700                                ERRDF   4,HDALRG,R06ERR         ;HDAL REG NOT EQUAL TO EXPECTED
8231  021700  104455                        TRAP    C$ERDF
8232  021702  000004                        .WORD   4
8233  021704  002605                        .WORD   HDALRG
8234  021706  005020                        .WORD   R06ERR
8235  021710                                CKLOOP
8236  021710  104406                        TRAP    C$CLP1
8237
8238                                    ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
8239                                    ;ZEROES.  ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
8240                                    ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.
8241
8242  021712  004737  007072        3$:     JSR     PC,SLDADR               ;GO SELECT DIAG ADDRESS REG VIA GDAL 2:0
8243
8244                                    ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH A DATA
8245                                    ;PATTERN OF 146063.  THE DIAGNOSTIC ADDRESS REGISTER IS WRITTEN WITH
8246                                    ;DATA TO CHECK THAT THE CORRECT FORCE JUMP ADDRESS REGISTER IS ENABLED
8247                                    ;TO THE EODAL BUS WHEN THE 8 BIT ADDRESS FLIP-FLOPS ARE SET.  THE NEW
8248                                    ;FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE BUS DURING THIS
8249                                    ;TEST.
8250
8251  021716  012737  146063  002342        MOV     #146063,R6LOAD          ;SETUP DATA PATTERN
8252  021724  004737  006672                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK DIAG ADDR REG
8253  021730  001405                        BEQ     4$                      ;IF LOADED OK THEN CONTINUE
8254  021732                                ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDRESS REG NOT EQUAL EXPECTED
8255  021732  104455                        TRAP    C$ERDF
8256  021734  000004                        .WORD   4
8257  021736  002735                        .WORD   ADDRRG
8258  021740  005020                        .WORD   R06ERR
8259  021742                                CKLOOP
8260  021742  104406                        TRAP    C$CLP1
8261
8262                                    ;LOAD, READ AND CHECK ADAL REGISTER.  ADAL0 WILL BE SET AND CLEARED
8263                                    ;TO CLEAR THE BREAK LOGIC.  ADAL4 ON A ZERO WILL PUT THE PAUSE STATE
8264                                    ;MACHINE IN THE PAUSE MODE.  ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT
8265                                    ;BREAK SIGNAL FROM CAUSING A BREAK CONDITION.  ADAL4 H ON A ZERO WILL
8266                                    ;CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE WHEN THE
8267                                    ;SIGNAL XRAS H IS PULSED.
8268
8269  021744  005037  002330        4$:     CLR     R2LOAD                  ;SETUP TO CLEAR ALL ADAL REGISTER BITS
8270  021750  004737  007772                JSR     PC,BRKRES               ;PULSE BRKRES L VIA ADAL0 H
8271
8272                                    ;SET VDAL2 H TO A ONE AND THEN ZERO.  VDAL2 H ON A ONE WILL CLEAR THE
8273                                    ;PAUSE STATE MACHINE FLIP-FLOPS AND THE FLIP-FLOPS, TAKE NEW FORCE JUMP
8274                                    ;ADDRESS AND GET NEW ADDRESS.
8275
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8276  021754  005037  002334                  CLR     R4LOAD                  ;SETUP TO CLEAR ALL VDAL REGISTER BITS
8277  021760  004737  007712                  JSR     PC,CLRPSM               ;SET AND CLEAR VDAL2 H TO 0 PAUSE STATE
8278
8279                                          ;SELECT THE NEW FORCE JUMP ADDRESS REGISTER BY SETTING GDAL1 H TO A ONE
8280                                          ;AND GDAL BITS 2 AND 0 TO ZEROES.  ON A WRITE COMMAND TO CONTROL REG 6,
8281                                          ;DATA WILL BE LOADED INTO THE NEW FORCE JUMP ADDRESS REGISTER AND THE
8282                                          ;TAKE NEW FORCE JUMP ADRESS FLIP-FLOP WILL BE SET
8283
8284  021764  004737  007040                  JSR     PC,SLFJAR               ;SELECT NEW FJA VIA GDAL BITS 2:0
8285
8286                                          ;ISSUE A WRITE COMMAND TO CONTROL REGISTER 6 TO WRITE THE DATA INTO THE
8287                                          ;NEW FORCE JUMP ADDRESS REGISTER.  THE DATA WILL BE LOADED INTO THE
8288                                          ;FORCE JUMP ADDRESS REGISTER VIA THE SIGNALS WPT1 LB H AND WPT1 HB H.
8289                                          ;THE TAKE NEW FORCE JUMP ADDRESS FLIP-FLOP WILL ALSO BE SET TO A ONE
8290                                          ;BY THE SIGNAL WPT1 LB H.  THE DATA PATTERNS LOADED WILL BE ONE OF THE
8291                                          ;FOLLOWING: 125125, 052652, 000377, 177400, 125252, 052525, 177777 AND
8292                                          ;000000.
8293
8294  021770  011177  160312                  MOV     (R1),@REG6              ;WRITE DATA FROM THE TABLE INTO NEW FJA
8295
8296                                          ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE (1).
8297                                          ;CHECK THAT THE SIGNAL WPT1 LB H CLOCKED THE TAKE NEW FORCE JUMP ADDRESS
8298                                          ;FLIP-FLOP TO A ONE.
8299
8300  021774  012737  000200  002334          MOV     #VDAL7,R4LOAD           ;SETUP BIT TO BE LOADED
8301  022002  013737  002334  002336          MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
8302  022010  052737  100000  002336          BIS     #VDAL15,R4GOOD          ;SETUP TO EXPECT TNFJ H TO BE A 1
8303  022016  004737  006646                  JSR     PC,LDRD4R               ;GO LOAD READ AND CHECK VDAL REG
8304  022022  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8305  022024                                  FRRDF   3,VDALRG,R4EROR         ;TNFJ H PROABABLY NOT SET IN VDAL REG
8306  022024  104455                          TRAP    C$ERDF
8307  022026  000003                          .WORD   3
8308  022030  002537                          .WORD   VDALRG
8309  022032  005004                          .WORD   R4EROR
8310  022034                                  CKLOOP
8311  022034  104406                          TRAP    C$CLP1
8312
8313                                          ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
8314                                          ;TO ONES.  BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
8315                                          ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L,
8316
8317  022036  004737  006754          5$:     JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL 2:0
8318
8319                                          ;SET HDAL12 H TO A ONE TO SET THE SIGNALS XRAS H AND XRAS L TO THE
8320                                          ;HIGH AND LOW STATE RESPECTIVELY.  THEY WILL REMAIN SET TO THESE STATES
8321                                          ;UNTIL THE PROGRAM PULSES THE SIGNALS XPI H AND XPI L.
8322                                          ;
8323                                          ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
8324                                          ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
8325                                          ;HIGH STATE.  THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
8326                                          ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
8327                                          ;TO THE HIGH STATE.  THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
8328                                          ;SIGNAL PAUSE L IS ASSERTED HIGH.  WHEN SOP H AND EDFET H ARE ASSERTED
8329                                          ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
8330                                          ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
8331                                          ;PSMW H WILL BE ASSERTED HIGH.  THE SIGNAL PSMW H IS READ IN THE VDAL
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                                        ;REGISTER AS VDAL9 H.  WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
                                        ;SIGNAL PB H WILL BE ASSERTED HIGH.  THE SIGNAL PB H IS THE DATA INPUT
                                        ;LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
                                        ;
                                        ;THE SIGNAL XRAS H WILL CAUSE THE SIGNAL RASP H TO BE PULSED.  WHEN THE
                                        ;SIGNAL RASP H IS PULSED AND THE SIGNAL EDFET H IS ASSERTED HIGH, A
                                        ;PULSE WILL BE ISSUED ON THE SIGNAL DFET H.  THE SIGNAL DFET H WILL
                                        ;CLOCK THE ADDRESS BUS INTO THE OLD FORCE JUMP ADDRESS REGISTER.  AT THE
                                        ;PRESENT TIME THE DIAGNOSTIC ADDRESS REGISTER IS ENABLED ONTO THE
                                        ;ADDRESS BUS, THEREFORE THE OLD FORCE JUMP ADDRESS REGISTER WILL BE
                                        ;LOADED WITH THE DATA FROM THE DIAGNOSTIC ADDRESS REGISTER.

022042  012737  001004  012342          MOV     #HDAL9!HDAL2,R6LOAD     ;SETUP BITS PREVIOUSLY LOADED
022050  004737  007304                  JSR     PC,XRASH                ;SET XRAS H HIGH + XRAS L VIA HDAL12 H

                                        ;CLEAR VDAL7 H IN THE VDAL REGISTER THUS SETTING THE SIGNAL FETCT H TO
                                        ;THE LOW STATE.  CHECK THE PAUSE STATE MACHINE TO BE IN THE FOLLOWING
                                        ;STATE AS A RESULT OF EDFET H AND SOP H BEING ASSERTED HIGH.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB H - EP8G H - 0
                                        ;    8 BIT ADDRESS HB H - EP8N H - 0
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;    GET NEW ADDRESS - OUTNEW H - 0

022054  042737  000200  002334          BIC     #VDAL7,R4LOAD           ;SETUP TO CLEAR FETCT H
022062  013737  002334  002336          MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
022070  052737  101000  002336          BIS     #VDAL15!VDAL9,R4GOOD    ;EXPECT PSMW H AND TNFJ H F/F'S
022076  004737  006646                  JSR     PC,LDRD4R               ;GO LOAD, READ AND CHECK VDAL REG
022102  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
022104                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
022104  104455                          TRAP    C$ERDF
022106  000003                          .WORD   3
022110  002537                          .WORD   VDALRG
022112  005004                          .WORD   R4EROR
022114                                  CKLOOP
022114  104406                          TRAP    C$CLP1

                                        ;THE SIGNALS XRAS H AND XRAS L ARE STILL ASSERTED TO THE HIGH AND LOW
                                        ;STATE RESPECTIVELY BY HDAL12 H BEING SET TO A ONE.  THEY WILL REMAIN
                                        ;SET TO THESE STATES UNTIL THE SIGNALS XPI H AND XPI L ARE PULSED.
                                        ;
                                        ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
                                        ;SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
                                        ;SIGNAL "PB H", WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP,
                                        ;THUS SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE.  THE SIGNAL
                                        ;XCAS H WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-
                                        ;FLOP (0) INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS CLOCKING THAT
                                        ;FLIP-FLOP TO A ZERO.

022116  004737  007410          6$:     JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H

                                        ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                        ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
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```
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EP8N H - 0
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;    GET NEW ADDRESS - OUTNEW H - 0

022122  052737  002000  00233r        BIS     #VDAL10,R4GOOD          ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
022130  004737  006654                JSR     PC,READR4               ;GO READ AND CHECK PAUSE STATE MACHINE
022134  001405                        BEQ     7$                      ;IF LOADED OK THEN CONTINUE
022136                                ERRDF   3,VDALRG,R4EROR         ;EPSF H PROBABLE NOT SET IN VDAL REG
022136  104455                        TRAP    C$ERDF
022140  000003                        .WORD   3
022142  002537                        .WORD   VDALRG
022144  005004                        .WORD   R4EROR
022146                                CKLOOP
022146  104406                        TRAP    C$CLP1

                                    ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE LOW
                                    ;BYTE OF THE 16 BIT INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE
                                    ;EODAL BUS AT THE SAME TIME.  ON A READ COMMAND TO CONTROL REGISTER 6,
                                    ;THE EODAL BUS WILL BE ENABLED TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.

022150  004737  007122        7$:     JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0

                                    ;WHEN THE SIGNAL XCAS H IS ASSERTED HIGH AND THE PAUSE STATE WORKING
                                    ;FLIP-FLOP IS SET TO A ONE. THE SIGNAL ACAS H WILL BE ASSERTED HIGH.
                                    ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH, THE PAUSE STATE SYNC FLIP-
                                    ;FLOP IS SET TO A ONE, AND MODE REGISTER BIT 11 IS A ONE (8 BIT MODE),
                                    ;THE SIGNAL EDRL H WILL BE ASSERTED LOW, THUS ENABLING THE LOW BYTE OF
                                    ;THE 16 BIT INSTRUCTION REGISTER ONTO THE EODAL BUS.  THE HIGH BYTE OF
                                    ;THE 16 BIT INSTRUCTION REGISTER WILL BE DISABLED ON THE EODAL BUS.
                                    ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH GDAL BITS 2:0
                                    ;SET TO ONES, A PULSE WILL BE ISSUED ON THE SIGNAL RPT7 L.  THE SIGNAL
                                    ;RPT7 L WILL READBACK THE EODAL BUS ONTO THE LSI-11 BUS.

022154  012737  000137  002342        MOV     #137,R6LOAD             ;SETUP EXPECTED LOW BYTE DATA
022162  012737  177400  002346        MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE
022170  004737  006700                JSR     PC,READR6               ;GO READ LOW BYTE OF INSTR REG ON EODAL
022174  001405                        BEQ     8$                      ;IF INSTR = "JMP" THEN CONTINUE
022176                                ERRDF   4,IEODAL,R06ERR         ;EODAL BUS ERROR OR 8 BIT LB INSTR ERROR
022176  104455                        TRAP    C$ERDF
022200  000004                        .WORD   4
022202  003034                        .WORD   IEODAL
022204  005020                        .WORD   R06ERR
022206                                CKLOOP
022206  104406                        TRAP    C$CLP1

                                    ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 H TO A ZERO AND GDAL BITS
                                    ;1 AND 0 TO A ONE.

022210  004737  006754        8$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0

                                    ;SET THE SIGNAL XCAS H TO A ZERO BY CLEARING HDAL13 H IN HDAL REGISTER.
                                    ;
                                    ;THE SIGNALS XRAS H AND XRAS L WILL REMAIN ASSERTED TO THE HIGH AND LOW
```

```
                                        ;STATE RESPECTIVELY BY HDAL12 H BEING SET TO A ONE.  THEY WILL NOT BE
                                        ;DE-ASSERTED UNTIL PULSES HAVE BEEN ISSUED ON THE SIGNALS XPI H AND XPI L.

022214  012737  031004  002342          MOV     #HDAL13!HDAL12!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
022222  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
022226  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H

                                        ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H.  THIS IS DONE
                                        ;TO SIMULATE A MACHINE CYCLE.

022232  004737  007502                  JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H

                                        ;READ THE VDAL REGISTER AGAIN TO CHECK THAT THE "TAKE NEW FORCE JUMP
                                        ;ADDRESS" FLIP-FLOP IS STILL SET.  IT SHOULD NOT CLEAR UNTIL THE NEXT
                                        ;XCAS H PULSE.  THE PAUSE STATE MACHINE FLIP-FLOPS SHOULD REMAIN
                                        ;UNCHANGED AFTER XPI H AND XPI L ARE PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EP8N H - 0
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;    GET NEW ADDRESS - OUTNEW H - 0

022236  004737  006654                  JSR     PC,READR4               ;READ VDAL REG AND PAUSE STATE MACHINE
022242  001405                          BEQ     9$                      ;IF OK THEN CONTINUE
022244                                  ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE MACHINE CHANGED AFTER XPI
022244  104455                          TRAP    C$ERDF
022246  000003                          .WORD   3
022250  002537                          .WORD   VDALRG
022252  005004                          .WORD   R4EROR
022254                                  CKLOOP
022254  104406                          TRAP    C$CLP1

                                        ;SET THE SIGNALS XRAS H AND XRAS L TO THEIR DE-ASSERTED STATE BY CLEARING
                                        ;HDAL12 H IN THE HDAL REGISTER.  WHEN XRAS L IS RETURNED TO THE HIGH
                                        ;STATE, THE "GET NEW ADDRESS" FLIP-FLOP WILL BE CLOCKED TO A ONE AS A
                                        ;RESULT OF THE "TAKE NEW FORCE JUMP ADDRESS" FLIP-FLOP BEING SET AND
                                        ;THE "PAUSE STATE SYNC" FLIP-FLOP BEING SET.  WHEN THE "GET NEW ADDRESS"
                                        ;FLIP-FLOP IS SET, THE SIGNAL OUTNEW H WILL BE ASSERTED HIGH.  THE
                                        ;OUTNEW H SIGNAL IS READ IN THE VDAL REGISTER AS VDAL BIT 8.

022256  004737  007336          9$:     JSR     PC,XRASL                ;SET XRAS H LOW + XRAS L HIGH VIA HDAL12

                                        ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
                                        ;BE IN THE FOLLOWING STATES.  THE "GET NEW ADDRESS" FLIP-FLOP SHOULD
                                        ;HAVE BEEN SET TO A ONE BY XRAS L AS A RESULT OF THE "TAKE NEW FORCE
                                        ;JUMP ADDRESS" FLIP-FLOP BEING SET AND THE "PAUSE STATE SYNC FLIP-FLOP
                                        ;BEING SET TO A ONE.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EP8N H - 0
                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
                                        ;    GET NEW ADDRESS - OUTNEW H - 1
```

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8500
8501  022262  052737  000400  002336          BIS     #VDAL8,R4GOOD           ;EXPECT OUTNEW H TO BE SET TO A ONE
8502  022270  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
8503  022274  001405                          BEQ     10$                     ;IF OK THEN CONTINUE
8504  022276                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REG NOT EQUAL EXPECTED
8505  022276  104455                          TRAP    C$ERDF
8506  022300  000003                          .WORD   3
8507  022302  002537                          .WORD   VDALRG
8508  022304  005004                          .WORD   R4EROR
8509  022306                                  CKLOOP
8510  022306  104406                          TRAP    C$CLP1
8511
8512                                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8513                                          ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8514                                          ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
8515                                          ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
8516                                          ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
8517                                          ;AND RASP L WILL BE PULSED.
8518                                          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
8519                                          ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
8520
8521  022310  004737  007272          10$:    JSR     PC,XRAS                 ;GO PULSE XRAS H BY HDAL12
8522
8523                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
8524                                          ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8525                                          ;    PAUSE STATE WORKING - PSMW H - 1
8526                                          ;    PAUSE STATE SYNC - EPSF H - 1
8527                                          ;    8 BIT INSTRUCTION HB - EP8F H - 0
8528                                          ;    8 BIT ADDRESS LB  - EP8G H - 0
8529                                          ;    8 BIT ADDRESS HB - EP8N H - 0
8530                                          ;    TAKE NEW FJ ADDRESS - TNFJ H - 1
8531                                          ;    GET NEW ADDRESS - OUTNEW H - 1
8532
8533  022314  004737  006654                  JSR     PC,READR4               ;CHECK VDAL AND PAUSE STATE MACHINE
8534  022320  001405                          BEQ     11$                     ;IF OK THEN CONTINUE
8535  022322                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
8536  022322  104455                          TRAP    C$ERDF
8537  022324  000003                          .WORD   3
8538  022326  002537                          .WORD   VDALRG
8539  022330  005004                          .WORD   R4EROR
8540  022332                                  CKLOOP
8541  022332  104406                          TRAP    C$CLP1
8542
8543                                          ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
8544                                          ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE LEVEL OF THE
8545                                          ;SIGNAL "PB H", WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
8546                                          ;CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO.  THE SIGNAL XCAS H
8547                                          ;WILL CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP (1)
8548                                          ;INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS SETTING THAT FLIP-FLOP
8549                                          ;TO A ONE.  THE SIGNAL XCAS H WILL ALSO CLOCK THE PREVIOUS STATE OF THE
8550                                          ;8 BIT INSTRUCTION HB FLIP-FLOP (0) INTO THE 8 BIT ADDRESS LB FLIP-FLOP,
8551                                          ;THUS CLOCKING THAT FLIP-FLOP TO A ZERO.
8552                                          ;THE SIGNAL XCAS H WILL ALSO CAUSE THE "TAKE NEW FORCE JUMP ADDRESS"
8553                                          ;FLIP-FLOP TO BE CLEARED WHEN THE "GET NEW ADDRESS" FLIP-FLOP IS SET
8554                                          ;TO A ONE.
8555
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8556  022334  004737  007410          11$:    JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H
8557
8558                                          ;READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
8559                                          ;FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING SET HIGH
8560                                          ;    PAUSE STATE WORKING - PSMW H - 1
8561                                          ;    PAUSE STATE SYNC - EPSF H - 0
8562                                          ;    8 BIT INSTRUCTION HB - EP8F H - 1
8563                                          ;    8 BIT ADDRESS LB - EP8G H - 0
8564                                          ;    8 BIT ADDRESS HB - EPFN H - 0
8565                                          ;    TAKE NEW FJ ADDRESS - TNFJ H - 0
8566                                          ;    GET NEW ADDRESS - OUTNEW H - 1
8567
8568  022340  042737  102000  002336          BIC     #VDAL15!VDAL10,R4GOOD   ;CLEAR BIT FOR EPSF H AND TNFJ H
8569  022346  052737  010000  002336          BIS     #VDAL12,R4GOOD          ;SET BIT FOR EP8F H
8570  022354  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
8571  022360  001405                          BEQ     12$                     ;IF OK THEN CONTINUE
8572  022362                                  ERRDF   3,VDALRG,R4EROR         ;EP8F H PROBABLY NOT SET IN VDAL REG
8573  022362  104455                          TRAP    C$ERDF
8574  022364  000003                          .WORD   3
8575  022366  002537                          .WORD   VDALRG
8576  022370  005004                          .WORD   R4EROR
8577  022372                                  CKLOOP
8578  022372  104406                          TRAP    C$CLP1
8579
8580                                          ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE HIGH
8581                                          ;BYTE OF THE 16 BIT INSTRUCTION REGISTER SHOULD BE ASSERTED ON THE
8582                                          ;EODAL BUS AT THIS TIME.  ON A READ COMMAND TO CONTROL REGISTER 6,
8583                                          ;THE EODAL BUS WILL BE ENABLED TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
8584
8585  022374  004737  007122          12$:    JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
8586
8587                                          ;WHEN THE SIGNAL XCAS H IS ASSERTED HIGH AND THE PAUSE STATE WORKING
8588                                          ;FLIP-FLOP IS SET TO A ONE, THE SIGNAL ACAS H WILL BE ASSERTED HIGH.
8589                                          ;WHEN THE SIGNAL ACAS H IS ASSERTED HIGH AND THE 8 BIT INSTRUCTION HB
8590                                          ;FLIP-FLOP IS SET TO A ONE, THE SIGNAL ED8H H WILL BE ASSERTED HIGH,
8591                                          ;THUS ENABLING THE HIGH BYTE OF THE 16 BIT INSTRUCTION REGISTER (000)
8592                                          ;ONTO THE LOW BYTE OF THE EODAL BUS.  WHEN A READ COMMAND IS ISSUED TO
8593                                          ;CONTROL REGISTER 6 WITH GDAL BITS 2:0 SET TO ONES, A PULSE WILL BE
8594                                          ;ISSUED ON THE SIGNAL RPT7 L.  THE SIGNAL RPT7 L WILL READBACK THE
8595                                          ;EODAL BUS ONTO THE LSI-11 BUS.
8596
8597  022400  005037  002342                  CLR     R6LOAD                  ;EXPECT HIGH BYTE TO BE ZERO
8598  022404  012737  177400  002346          MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE ON READ
8599  022412  004737  006700                  JSR     PC,READR6               ;GO READ 8 BIT HIGH BYTE INSTRUCTION
8600                                                                          ;ON THE EODAL BUS AS LOW BYTE
8601  022416  001405                          BEQ     13$                     ;IF INSTRUCTION EQUALS 0 THEN CONT
8602  022420                                  ERRDF   4,IEODAL,R06ERR         ;EODAL BUS OR 8 BIT HB INSTR ERROR
8603  022420  104455                          TRAP    C$ERDF
8604  022422  000004                          .WORD   4
8605  022424  003034                          .WORD   IEODAL
8606  022426  005020                          .WORD   R06ERR
8607  022430                                  CKLOOP
8608  022430  104406                          TRAP    C$CLP1
8609
8610                                          ;RESELECT THE HDAL REGISTER BY SETTING GDAL2 H TO A ZERO AND GDAL BITS
8611                                          ;1 AND 0 TO ONES.
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8612
8613  022432  004737  006754          13$:    JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0
8614
8615                                          ;SET THE SIGNAL XCAS H TO LOW STATE BY CLEARING HDAL13 H IN HDAL REGIS :
8616
8617  022436  012737  021004  002342          MOV     #HDAL13!HDAL9!HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
8618  022444  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
8619  022450  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H
8620
8621                                          ;TOGGLE THE SIGNAL XPI H BY PULSING THE SIGNAL HDAL15 H.  THIS IS DONE
8622                                          ;TO SIMULATE A MACHINE CYCLE.
8623
8624  022454  004737  007502                  JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
8625
8626                                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8627                                          ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8628                                          ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
8629                                          ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
8630                                          ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
8631                                          ;AND RASP L WILL BE PULSED.
8632                                          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
8633                                          ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
8634
8635  022460  004737  007272                  JSR     PC,XRAS                 ;PULSE XRAS VIA THE SIGNAL HDAL12
8636
8637                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
8638                                          ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8639                                          ;NO CHANGES SHOULD OCCUR IN THE PAUSE STATE MACHINE WHEN XRAS H PULSED.
8640                                          ;    PAUSE STATE WORKING - PSMW H - 1
8641                                          ;    PAUSE STATE SYNC - EPSF H - 0
8642                                          ;    8 BIT INSTRUCTION HB - EP8F H - 1
8643                                          ;    8 BIT ADDRESS LB - EP8G H - 0
8644                                          ;    8 BIT ADDRESS HB - EP8N H - 0
8645                                          ;    TAKE NEW FJ ADDRESS - TNFJ H - 0
8646                                          ;    GET NEW ADDRESS - OUTNEW H - 1
8647
8648  022464  004737  006654                  JSR     PC,READP4               ;GO READ VDAL AND PAUSE STATE MACHINE
8649  022470  001405                          BEQ     14$                     ;IF OK THEN CONTINUE
8650  022472                                  ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE REGISTERS CHANGED
8651  022472  104455                          TRAP    C$ERDF
8652  022474  000003                          .WORD   3
8653  022476  002537                          .WORD   VDALRG
8654  022500  005004                          .WORD   R4EROR
8655  022502                                  CKLOOP
8656  022502  104406                          TRAP    C$CLP1
8657
8658                                          ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE. THE
8659                                          ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE OUTPUT OF THE
8660                                          ;PAUSE STATE SYNC FLIP-FLOP (0) INTO THE 8 BIT INSTRUCTION HB FLIP-
8661                                          ;FLOP, THUS CLEARING THE 8 BIT INSTRUCTION HB FLIP-FLOP.  THE PREVIOUS
8662                                          ;OUTPUT OF THE 8 BIT INSTRUCTION HB FLIP-FLOP (1) WILL BE CLOCKED INTO
8663                                          ;THE 8 BIT ADDRESS LB FLIP-FLOP THUS SETTING THE 8 BIT ADDRESS LB F/F.
8664
8665  022504  004737  007410          14$:    JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H
8666
8667                                          ;READ VDAL REGISTER AND CHECK PAUSE STATE MACHINE FLIP-FLOPS TO BE  N
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                                        ;THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
                                        ;   PAUSE STATE WORKING - FSMW H - 1
                                        ;   PAUSE STATE SYNC - EPSF H - 0
                                        ;   8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;   8 BIT ADDRESS LB - EP8G H - 1
                                        ;   8 BIT ADDRESS HB - EP8N H - 0
                                        ;   TAKE NEW FJ ADDRESS - TNFJ H - 0
                                        ;   GET NEW ADDRESS - OUTNEW H - 1

022510  042737  010000  002336        BIC     #VDAL12,R4GOOD          ;SETUP TO EXPECT EP8F H TO BE 0
022516  052737  020000  002336        BIS     #VDAL13,R4GOOD          ;SETUP TO EXPECT EP8G H TO BE 1
022524  004737  006654                JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
022530  001405                      BEQ     15$                     ;IF OK THEN CONTINUE
022532                              ERRDF   3,VDALRG,R4EROR         ;EP8F H PROBABLY NOT 0 OR EP8G H NOT SET
022532  104455                      TRAP    C$ERDF
022534  000003                      .WORD   3
022536  002537                      .WORD   VDALRG
022540  005004                      .WORD   R4EROR
022542                              CKLOOP
022542  104406                      TRAP    C$CLP1

                                        ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE LOW BYTE
                                        ;OF THE NEW FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL
                                        ;BUS AT THIS TIME.  ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL
                                        ;BUS WILL BE READBACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.

022544  004737  007122        15$:    JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0

                                        ;AT THIS POINT IN TIME, THE LOW BYTE OF THE NEW FORCE JUMP ADDRESS REG-
                                        ;ISTER WILL BE ENABLED TO THE EODAL BUS VIA THE SIGNAL NEARL L. THIS
                                        ;SIGNAL IS ASSERTED LOW AS A RESULT OF "GET NEW ADDRESS"
                                        ;FLIP-FLOP BEING SET AND THE SIGNAL EARL H BEING ASSERTED HIGH.  THE
                                        ;"GET NEW ADDRESS" FLIP - FLOP WAS SET WHEN THE PAUSE STATE SYNC FLIP-
                                        ;FLOP WAS A ONE, A PULSE ISSUED ON XRAS L, AND THE TAKE NEW FORCE
                                        ;JUMP ADDRESS FLIP-FLOP WAS SET TO A ONE.  THE SIGNAL EARL H IS ASSERTED
                                        ;HIGH AS A RESULT OF THE 8 BIT ADDRESS LOW BYTE FLIP-FLOP BEING SET TO A
                                        ;ONE AND THE SIGNAL ACAS H BEING ASSERTED HIGH.  THE FOLLOWING SECTION
                                        ;WILL READ AND CHECK THAT THE LOW BYTE OF THE NEW FORCE JUMP ADDRESS
                                        ;REGISTER IS ENABLED TO THE EODAL BUS.  THE EODAL BUS WILL BE READBACK
                                        ;VIA THE SIGNAL RPT7 L WHEN A READ COMMAND IS ISSUED TO CONTROL REG 6.
                                        ;
                                        ;IF THE LOW BYTE DATA READ FROM THE EODAL BUS EQUALS 063, THEN THE OLD
                                        ;FORCE JUMP ADDRESS WAS PROBARLY ENABLED TO THE EODAL BUS INSTEAD OF THE
                                        ;NEW FORCE JUMP ADDRESS REGISTER.  THE OLD FORCE JUMP ADDRESS REGISTER
                                        ;WAS LOADED WITH DATA FROM THE DIAGNOSTIC ADDRESS REGISTER VIA THE SIGNAL
                                        ;DFET H.  THE DIAGNOSTIC ADDRESS REGISTER WAS LOADED WITH A DATA PATTERN
                                        ;OF 146063 AT THE BEGINNING OF THE TEST.

022550  011137  002342                MOV     (R1),R6LOAD             ;GET THE DATA LOADED INTO THE DIAG
                                                                        ;ADDRESS REGISTER
022554  042737  177400  002342        BIC     #177400,R6LOAD          ;CLEAR UPPER BYTE
022562  012737  177400  002346        MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE
022570  004737  006700                JSR     PC,READR6               ;READ LB OF OLD FJA ON EODAL BUS
022574  001405                      BEQ     16$                     ;IF OLD FLA OK THEN CONTINUE
022576                              ERRDF   4,FEODAL,R06ERR         ;OLD FJA TO EODAL BUS ERROR
022576  104455                      TRAP    C$ERDF
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8724  022600  000004                          .WORD   4
8725  022602  003147                          .WORD   FEODAL
8726  022604  005020                          .WORD   R06ERR
8727  022606                                  CKLOOP
8728  022606  104406                          TRAP    C$CLP1
8729
8730                                          ;RESELECT THE HDAL REGISTER BY SETTING THE SIGNAL GDAL2 TO A ZERO AND
8731                                          ;GDAL BITS 1 AND 0 TO ONES.
8732
8733  022610  004737  006754          16$:    JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0
8734
8735                                          ;SET THE SIGNAL XCAS H TO LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER.
8736
8737  022614  012737  021004  002342          MOV     #HDAL13!HDAL9.HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
8738  022622  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
8739  022626  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H
8740
8741                                          ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H.  THIS IS
8742                                          ;DONE TO SIMULATE A MACHINE CYCLE.
8743
8744  022632  004737  007502                  JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
8745
8746                                          ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8747                                          ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8748                                          ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
8749                                          ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
8750                                          ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
8751                                          ;AND RASP L WILL BE PULSED.
8752                                          ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
8753                                          ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
8754
8755  022636  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS VIA HDAL12 H
8756
8757                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
8758                                          ;BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8759                                          ;     PAUSE STATE WORKING - PSMW H - 1
8760                                          ;     PAUSE STATE SYNC - EPSF H - 0
8761                                          ;     8 BIT INSTRUCTION HB - EP8F H - 0
8762                                          ;     8 BIT ADDRESS LB - EP8G H - 1
8763                                          ;     8 BIT ADDRESS HB - EP8N H - 0
8764                                          ;     TAKE NEW FJ ADDRESS - TNFJ H - 0
8765                                          ;     GET NEW ADDRESS - OUTNEW H - 1
8766
8767  022642  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
8768  022646  001405                          BEQ     17$                     ;IF OK THEN CONTINUE
8769  022650                                  ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE MACHINE CHANGED BY XRAS H
8770  022650  104455                          TRAP    C$ERDF
8771  022652  000003                          .WORD   3
8772  022654  002537                          .WORD   VDALRG
8773  022656  005004                          .WORD   R4EROR
8774  022660                                  CKLOOP
8775  022660  104406                          TRAP    C$CLP1
8776
8777                                          ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
8778                                          ;SIGNAL XCAS H GOING FROM A 0 TO A ONE WILL CLOCK THE OUTPUT OF THE
8779                                          ;8 BIT INSTRUCTION HB FLIP-FLOP (0) INTO THE 8 BIT ADDRESS LB FLIP-
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8780                                        ;FLOP THUS CLEARING THE 8 BIT ADDRESS LOW BYTE FLIP-FLOP.  THE
8781                                        ;PREVIOUS OUTPUT OF THE 8 BIT ADDRESS LB FLIP-FLOP (1) WILL BE
8782                                        ;CLOCKED INTO THE 8 BIT ADDRESS HB FLIP-FLOP THUS SETTING THE 8 BIT
8783                                        ;ADDRESS HB FLIP-FLOP TO A ONE.
8784
8785  022662  004737  007410          17$:  JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H
8786
8787                                        ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
8788                                        ;BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
8789                                        ;    PAUSE STATE WORKING - PSMW H - 1
8790                                        ;    PAUSE STATE SYNC - EPSF H - 0
8791                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
8792                                        ;    8 BIT ADDRESS LB - EP8F H - 0
8793                                        ;    8 BIT ADDRESS HB - EP8N H - 1
8794                                        ;    TAKE NEW FJ ADDRESS - TNFJ H - 0
8795                                        ;    GET NEW ADDRESS - OUTNEW H - 1
8796
8797  022666  042737  020000  002336        BIC     #VDAL13,R4GOOD          ;SETUP TO EXPECT EP8G H TO BE A 0
8798  022674  052737  040000  002336        BIS     #VDAL14,R4GOOD          ;SETUP TO EXPECT EP8N H TO BE A 1
8799  022702  004737  006654                JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
8800  022706  001405                        BEQ     18$                     ;IF OK THEN CONTINUE
8801  022710                                ERRDF   3,VDALRG,R4EROR         ;EP8G H NOT 0 OR EP8N H NOT A 1
8802  022710  104455                        TRAP    C$ERDF
8803  022712  000003                        .WORD   3
8804  022714  002537                        .WORD   VDALRG
8805  022716  005004                        .WORD   R4EROR
8806  022720                                CKLOOP
8807  022720  104406                        TRAP    C$CLP1
8808
8809                                        ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE HIGH BYTE
8810                                        ;OF THE NEW FORCE JUMP ADDRESS REGISTER SHOULD BE ENABLED TO THE EODAL
8811                                        ;BUS AT THIS TIME.  ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL
8812                                        ;BUS WILL BE READBACK TO THE LSI-11 VIA THE SIGNAL RPT7 L.
8813
8814  022722  004737  007122          18$:  JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
8815
8816                                        ;AT THIS POINT IN TIME, THE HIGH BYTE OF THE NEW FORCE JUMP ADDRESS REG-
8817                                        ;ISTER WILL BE ENABLED TO THE EODAL BUS VIA THE SIGNAL NEA8H L. THIS
8818                                        ;SIGNAL IS ASSERTED LOW AS A RESULT OF "GET NEW ADDRESS"
8819                                        ;FLIP-FLOP BEING SET AND THE SIGNAL EA8H H BEING ASSERTED HIGH.  THE
8820                                        ;"GET NEW ADDRESS" FLIP-FLOP WAS SET WHEN THE PAUSE STATE SYNC FLIP
8821                                        ;FLOP WAS A ONE,  A PULSE ISSUED ON XRAS L,  AND THE TAKE NEW FORCE
8822                                        ;JUMP ADDRESS FLIP-FLOP WAS SET TO A ONE.  THE SIGNAL EA8H H IS ASSERTED
8823                                        ;HIGH AS A RESULT OF THE 8 BIT ADDRESS HIGH BYTE FLIP-FLOP BEING SET TO A
8824                                        ;ONE AND THE SIGNAL ACAS H BEING ASSERTED HIGH.  THE FOLLOWING SECTION
8825                                        ;WILL READ AND CHECK THAT THE HIGH BYTE OF THE NEW FORCE JUMP ADDRESS
8826                                        ;REGISTER IS ENABLED TO THE EODAL BUS.  THE EODAL BUS WILL BE READBACK
8827                                        ;VIA THE SIGNAL RPT7 L WHEN A READ COMMAND IS ISSUED TO CONTROL REG 6.
8828                                        ;
8829                                        ;IF THE HIGH BYTE DATA READ FROM THE EODAL BUS EQUALS 314, THEN THE OLD
8830                                        ;FORCE JUMP ADDRESS WAS PROBABLY ENABLED TO THE EODAL BUS INSTEAD OF THE
8831                                        ;NEW FORCE JUMP ADDRESS REGISTER.  THE OLD FORCE JUMP ADDRESS REGISTER
8832                                        ;WAS LOADED WITH DATA FROM THE DIAGNOSTIC ADDRESS REGISTER VIA THE SIGNAL
8833                                        ;DFET H.  THE DIAGNOSTIC ADDRESS REGISTER WAS LOADED WITH A DATA PATTERN
8834                                        ;OF 146063 AT THE BEGINNING OF THE TEST.
8835
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8836  022726  011137  002342              MOV     (R1),R6LOAD             ;GET DIAG ADDRESS REG DATA
8837  022732  000337  002342              SWAB    R6LOAD                  ;SWAP HIGH BYTE WITH LOW BYTE
8838  022736  042737  177400  002342      BIC     #177400,R6LOAD          ;CLEAR LOW BYTE IN HIGH BYTE POSITION
8839  022744  012737  177400  002346      MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE ON READ
8840  022752  004737  006700              JSR     PC,READR6               ;READ OLD FJA HB ON EODAL BUS
8841  022756  001405                      BEQ     19$                     ;OF OLD FLA OK THEN CONTINUE
8842  022760                              ERRDF   4,FEODAL,R06ERR         ;OLD FLA HB TO EODAL BUS ERROR
8843  022760  104455                      TRAP    C$ERDF
8844  022762  000004                      .WORD   4
8845  022764  003147                      .WORD   FEODAL
8846  022766  005020                      .WORD   R06ERR
8847  022770                              CKLOOP
8848  022770  104406                      TRAP    C$CLP1
8849
8850                                      ;RESELECT THE HDAL REGISTER BY SETTING THE SIGNAL GDAL2 TO A ZERO AND
8851                                      ;GDAL BITS 1 AND 0 TO ONES
8852
8853  022772  004737  006754      19$:    JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL BITS 2:0
8854
8855                                      ;SET XCAS H TO THE LOW STATE BY CLEARING HDAL13 H IN HDAL REGISTER.
8856
8857  022776  012737  021004  002342      MOV     #HDAL13.HDAL9.HDAL2,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
8858  023004  005037  002346              CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
8859  023010  004737  007442              JSR     PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H
8860
8861                                      ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING HDAL15 H.  THIS IS DONE
8862                                      ;TO SIMULATE A MACHINE CYCLE.
8863
8864  023014  004737  007502              JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
8865
8866                                      ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
8867                                      ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
8868                                      ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL
8869                                      ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL PB H
8870                                      ;WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H AND
8871                                      ;RASP L WILL BE PULSED.
8872                                      ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ZERO BY RASP L WHEN
8873                                      ;THE SIGNALS EPFN L AND PSMW H ARE ASSERTED HIGH AND THE THE SIGNAL
8874                                      ;EP8N L IS ASSERTED LOW.  A SHORT TIME AFTER RASP L, THE SIGNAL PSMW H
8875                                      ;WILL BE ASSERTED LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP
8876                                      ;BEING CLEARED.
8877
8878  023020  004737  007272              JSR     PC,XRAS                 ;GGO PULSE XRAS H AND XRAS L VIA HDAL12
8879
8880                                      ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE TO BE IN THE
8881                                      ;FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
8882                                      ;    PAUSE STATE WORKING - PSMW H - 0
8883                                      ;    PAUSE STATE SYNC - EPSF H - 0
8884                                      ;    8 BIT INSTRUCTION HB - EP8F H - 0
8885                                      ;    8 BIT ADDRESS HB - EP8G H - 0
8886                                      ;    8 BIT ADDRESS LB - EP8N H - 0
8887                                      ;    TAKE NEW FJ ADDRESS - TNFJ H - 0
8888                                      ;    GET NEW ADDRESS - OUTNEW H - 1
8889
8890  023024  042737  001000  002336      BIC     #VDAL9,R4GOOD           ;EXPECT PSMW H TO BE A ZERO
8891  023032  004737  006654              JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
```

```
8892  023036  001405                          BEQ     20$                     ;IF OK THEN CONTINUE
8893  023040                                  ERRDF   3,VDALRG,R4EROR         ;PSMW H F/F PROBABLY NOT CLEARED
8894  023040  104455                          TRAP    C$ERDF
8895  023042  000003                          .WORD   3
8896  023044  002537                          .WORD   VDALRG
8897  023046  005004                          .WORD   R4EROR
8898  023050                                  CKLOOP
8899  023050  104406                          TRAP    C$CLP1
8900
8901                                          ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  THE
8902                                          ;SIGNAL XCAS H WILL CLOCK THE OUTPUT OF THE 8 BIT ADDRESS LB FLIP-
8903                                          ;FLOP (0) INTO THE 8 BIT ADDRESS HB FLIP-FLOP, THUS SETTING THE 8 BIT
8904                                          ;ADDRESS HB FLIP-FLOP TO A ZERO.
8905
8906  023052  004737  007376          20$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
8907
8908                                          ;READ THE VDAL REGISTER AND THE PAUSE STATE MACHINE FLIP-FLOPS TO BE IN
8909                                          ;THE FOLLOWING STATES AS A RESULT OF XCAS H BEING PULSED.
8910                                          ;    PAUSE STATE WORKING - PSMW H - 0
8911                                          ;    PAUSE STATE SYNC - EPSF H - 0
8912                                          ;    8 BIT INSTRUCTION HB - EP8F H - 0
8913                                          ;    8 BIT ADDRESS LB - EP8G H - 0
8914                                          ;    8 BIT ADDRESS HB - EP8N H - 0
8915                                          ;    TAKE NEW FJ ADDRESS - TNFJ H - 0
8916                                          ;    GET NEW ADDRESS - OUTNEW H - 1
8917
8918  023056  042737  040000  002336          BIC     #VDAL14,R4GOOD          ;EXPECT EP8N H TO BE A ZERO
8919  023064  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
8920  023070  001405                          BEQ     21$                     ;IF OK THEN CONTINUE
8921  023072                                  ERRDF   3,VDALRG,R4EROR         ;EP8N H PROBABLY NOT CLEARED
8922  023072  104455                          TRAP    C$ERDF
8923  023074  000003                          .WORD   3
8924  023076  002537                          .WORD   VDALRG
8925  023100  005004                          .WORD   R4EROR
8926  023102                                  CKLOOP
8927  023102  104406                          TRAP    C$CLP1
8928
8929                                          ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
8930                                          ;THIS IS DONE TO FINISH THE MACHINE CYCLE.
8931
8932  023104  004737  007502          21$:    JSR     PC,XPI                  ;GO PULSE XPI VIA HDAL15 H
8933
8934                                          ;SET VDAL2 H TO A ONE AND THEN ZERO TO CLEAR THE ''GET NEW ADDRESS'' FLIP-
8935                                          ;FLOP.
8936
8937  023110  005037  002334                  CLR     R4LOAD                  ;SETUP TO EXPECT ALL BITS CLEARED
8938  023114  004737  007712                  JSR     PC,CLRPSM               ;GO CLEAR PAUSE STATE MACHINE F/F'S
8939
8940  023120                                  ENDSEG
8941  023120                          10000$:
8942  023120  104405                          TRAP    C$ESEG
8943
8944  023122  005721                          TST     (R1)+                   ;UPDATE TABLE POINTER
8945  023124  005302                          DEC     R2                      ;CHECK IF ALL PATTERNS DONE
8946  023126  001412                          BEQ     23$                     ;IF YES THEN EXIT
8947  023130  000137  021620                  JMP     1$                      ;DO NEXT PATTERN
```

```
 8948
 8949  023134  125125                  22$:    .WORD   125125
 8950  023136  052652                          .WORD   052652
 8951  023140  000377                          .WORD   000377
 8952  023142  177400                          .WORD   177400
 8953  023144  125252                          .WORD   125252
 8954  023146  052525                          .WORD   052525
 8955  023150  177777                          .WORD   177777
 8956  023152  000000                          .WORD   000000
 8957
 8958  023154                          23$:    ENDTST
 8959  023154                          L10064:
 8960  023154  104401                          TRAP    C$ETST
 8961
```

```
                                .SBTTL  TEST 35: CLEAR PAUSE STATE MACHINE VIA VDAL2 H - 8 BIT ADDRESS

                                ;++
                                ; THIS  TEST  WILL CHECK  THAT  THE PAUSE  STATE  MACHINE  FLIP - FLOPS,
                                ; PAUSE  STATE  WORKING,  PAUSE  STATE  SYNC, 8  BIT INSTRUCTION HB, 8 BIT
                                ; ADDRESS LB, AND 8 BIT ADDRESS HB, CAN BE CLEARED WHEN THE SIGNAL VDAL2 H IS
                                ; ASSERTED HIGH.  ALL THE ABOVE FLIP-FLOPS ARE SET TO A ONE BY SETTING THE
                                ; SIGNAL FETCT H TO A ONE, SETTING THE SIGNAL ADAL4 H TO A ZERO, AND PULSING
                                ; THE SIGNALS XRAS H AND XCAS H.  ONCE ALL THE FLIP-FLOPS ARE SET TO ONES, THE
                                ; TEST WILL SET THE SIGNAL VDAL2 H AND CHECK THAT ALL THE PAUSE STATE MACHINE
                                ; FLIP-FLOPS CLEARED.
                                ;--

023156                                  BGNTST
023156                          T35::
023156  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR

023162                                  BGNSEG
023162  104404                          TRAP    C$BSEG

                                ;SELECT THE MODE REGISTER BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDAL0
                                ;TO A ZERO.

023164  004737  007006                  JSR     PC,SLMODR               ;GO SELECT MODE REG VIA CONTROL REG 0

                                ;LOAD, READ AND CHECK MODE REGISTER BITS MR 15:0 WITH 4000.  MR BIT 11
                                ;ON A ONE WILL ENABLE 8 BIT ADDRESS SELECTION TO THE PAUSE STATE MACHINE

023170  012737  004000  002342          MOV     #MR11,R6LOAD            ;SETUP TO SET MR BIT 11
023176  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK MODE REGISTER
023202  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
023204                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO 0
023204  104455                          TRAP    C$ERDF
023206  000004                          .WORD   4
023210  002631                          .WORD   MODREG
023212  005020                          .WORD   R06ERR
023214                                  CKLOOP
023214  104406                          TRAP    C$CLP1

                                ;LOAD, READ AND CHECK ADAL REGISTER.  ADAL0 WILL BE SET AND CLEARED
                                ;TO CLEAR THE BREAK LOGIC.  ADAL4 ON A ZERO WILL PUT THE PAUSE STATE
                                ;MACHINE IN THE PAUSE MODE.  ADAL8 H ON A ZERO WILL DISABLE THE TIMEOUT
                                ;BREAK SIGNAL FROM CAUSING A BREAK CONDITION.  ADAL4 H ON A ZERO WILL
                                ;CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE WHEN THE
                                ;SIGNAL XRAS H IS PULSED.

023216  005037  002330          1$:     CLR     R2LOAD                  ;SETUP TO CLEAR ALL ADAL REG BITS
023222  004737  007772                  JSR     PC,BRKRES               ;PULSE BRKRES L VIA ADAL0 H

                                ;SET VDAL7 AND VDAL2 TO ONES IN THE VDAL REGISTER.  VDAL7 ON A ONE WILL
                                ;SET THE SIGNAL FETCT H TO THE HIGH STATE.  VDAL2 ON A ONE WILL CLEAR
                                ;THE PAUSE STATE MACHINE FLIP-FLOPS.  VDAL2 WILL BE RESET TO 0 AFTER
                                ;BEING SET TO A ONE.

023226  012737  000200  002334          MOV     #VDAL7,R4LOAD           ;SETUP BIT TO SET FETCT H
023234  004737  007712                  JSR     PC,CLRPSM               ;SET FETCT H AND PULSE INVD L VIA VDAL2 H
```

```
                                        ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
                                        ;TO ONES.  BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
                                        ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L.

023240  004737  006754                  JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL 2:0

                                        ;CLEAR ALL BITS IN THE HDAL REGISTER EXCEPT HDAL2 H. HDAL2 H ON A ONE
                                        ;WILL ALLOW THE PROGRAM TO CONTROL THE T-11 TIMING AND CONTROL SIGNALS.
                                        ;THE HDAL BITS ARE CLEARED HERE TO INSURE THAT ALL SIGNALS ARE IN A
                                        ;KNOWN STATE WHEN SCOPE LOOPING IS INVOKED BY THE USER

023244  012737  000004  002342          MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE SET TO A ONE
023252  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
023256  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
023260                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
023260  104455                          TRAP    C$ERDF
023262  000004                          .WORD   4
023264  002605                          .WORD   HDALRG
023266  005020                          .WORD   R06ERR
023270                                  CKLOOP
023270  104406                          TRAP    C$CLP1

                                        ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING THE SIGNAL HDAL12 H.
                                        ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
                                        ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
                                        ;HIGH STATE.  THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
                                        ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
                                        ;TO THE HIGH STATE.  THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
                                        ;SIGNAL PAUSE L IS ASSERTED HIGH.  WHEN SOP H AND EDFET H ARE ASSERTED
                                        ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
                                        ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
                                        ;PSMW H WILL BE ASSERTED HIGH.  THE SIGNAL PSMW H IS READ IN THE VDAL
                                        ;REGISTER AS VDAL9 H.  WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
                                        ;SIGNAL PB H WILL BE ASSERTED HIGH.  THE SIGNAL PB H IS THE DATA INPUT
                                        ;LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.

023272  004737  007272          2$:     JSR     PC,XRAS                 ;PULSE XRAS H VIA HDAL12 H

                                        ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                        ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNALS EDFET H AND SOP H
                                        ;BEING ASSERTED HIGH.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 0
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB H - EP8G H - 0
                                        ;    8 BIT ADDRESS HB H - EP8N H - 0

023276  052737  001000  002336          BIS     #VDAL9,R4GOOD           ;EXPECT PSMW H TO BE SET
023304  004737  006654                  JSR     PC,READR4               ;CHECK VDAL AND PAUSE STATE MACHINE
023310  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
023312                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
023312  104455                          TRAP    C$ERDF
023314  000003                          .WORD   3
023316  002537                          .WORD   VDALRG
023320  005004                          .WORD   R4EROR
```

```
                                        CKLOOP
023322                                  TRAP    C$CLP1

                                        ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13.  THE SIGNAL
                                        ;XCAS H WILL CLOCK THE PAUSE STATE SYNC FLIP-FLOP WITH THE LEVEL OF THE
                                        ;SIGNAL 'PB H', WHICH IS HIGH, THUS SETTING THE PAUSE STATE SYNC
                                        ;FLIP-FLOP TO A ONE.  THE SIGNAL XCAS H WILL ALSO CLOCK THE 8 BIT
                                        ;INSTRUCTION HB FLIP-FLOP WITH THE OUTPUT OF THE PAUSE STATE SYNC F/F
                                        ;WHICH WAS 0 BEFORE IT WAS SET TO A ONE BY XCAS H.  THEREFORE 8 BIT
                                        ;INSTRUCTION HB FLIP-FLOP WILL BE CLOCKED TO A ZERO STATE.

023324  004737  007376          3$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13

                                        ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                        ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING PULSED.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 0
                                        ;    8 BIT ADDRESS LB - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EP8N H - 0

023330  052737  002000  002336          BIS     #VDAL10,R4GOOD          ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
023336  004737  006654                  JSR     PC,READR4               ;GO READ AND CHECK PAUSE STATE MACHINE
023342  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
023344                                  ERRDF   3,VDALRG,R4EROR         ;EPSF H PROBABLE NOT SET IN VDAL REG
023344  104455                          TRAP    C$ERDF
023346  000003                          .WORD   3
023350  002537                          .WORD   VDALRG
023352  005004                          .WORD   R4EROR
023354                                  CKLOOP
023354  104406                          TRAP    C$CLP1

                                        ;TOGGLE THE SIGNAL XCAS H AGAIN BY SETTING AND CLEARING HDAL13 H.  THE
                                        ;SIGNAL XCASH WILL CLOCK THE OUTPUT OF THE PAUSE STATE SYNC FLIP-FLOP (1)
                                        ;INTO THE 8 BIT INSTRUCTION HB FLIP-FLOP, THUS SETTING THE 8 BIT INSTRUC-
                                        ;TION HB FLIP-FLOP TO A ONE.

023356  004737  007376          4$:    JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H

                                        ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                        ;IN THE FOLLOWING STATE AS A RESULT OF PULSING THE SIGNAL XCAS H
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    8 BIT INSTRUCTION HB - EP8F H - 1
                                        ;    8 BIT ADDRESS LB - EP8G H - 0
                                        ;    8 BIT ADDRESS HB - EP8N H - 0

023362  052737  010000  002336          BIS     #VDAL12,R4GOOD          ;SETUP TO EXPECT EP8F H TO BE A 1
023370  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
023374  001405                          BEQ     5$                      ;IF OK THEN CONTINUE
023376                                  ERRDF   3,VDALRG,R4EROR         ;EP8F H PROBABLY NOT SET TO A 1
023376  104455                          TRAP    C$ERDF
023400  000003                          .WORD   3
023402  002537                          .WORD   VDALRG
023404  005004                          .WORD   R4EROR
023406                                  CKLOOP
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 9130  023406  104406                          TRAP    C$CLP1
 9131
 9132                                          ;TOGGLE THE SIGNAL XCAS H AGAIN BY SETTING AND CLEARING HDAL13 H.  THE
 9133                                          ;SIGNAL XCAS H WILL CLOCK THE OUTPUT OF THE 8 BIT INSTRUCTION HB FLIP-
 9134                                          ;FLOP (1) INTO THE 8 BIT ADDRESS LB FLIP-FLOP, THUS SETTING THE 8 BIT
 9135                                          ;ADDRESS LB FLIP-FLOP TO A ONE.
 9136
 9137  023410  004737  007376          5$:     JSR     PC,XCAS                 ;GO PULSE XCAS H VIA HDAL13 H
 9138
 9139                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
 9140                                          ;BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
 9141                                          ;    PAUSE STATE WORKING - PSMW H - 1
 9142                                          ;    PAUSE STATE SYNC - EPSF H - 1
 9143                                          ;    8 BIT INSTRUCTION HB - EP8F H - 1
 9144                                          ;    8 BIT ADDRESS LB - EP8G H - 1
 9145                                          ;    8 BIT ADDRESS HB - EP8N H - 0
 9146
 9147  023414  052737  020000  002336          BIS     #VDAL13,R4GOOD          ;SETUP TO EXPECT EP8G H TO BE A ONE
 9148  023422  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
 9149  023426  001405                          BEQ     6$                      ;IF OK THEN CONTINUE
 9150  023430                                  ERRDF   3,VDALRG,R4EROR         ;EP8G H PROBABLY NOT SET
 9151  023430  104455                          TRAP    C$ERDF
 9152  023432  000003                          .WORD   3
 9153  023434  002537                          .WORD   VDALRG
 9154  023436  005004                          .WORD   R4EROR
 9155  023440                                  CKLOOP
 9156  023440  104406                          TRAP    C$CLP1
 9157
 9158                                          ;TOGGLE THE SIGNAL XCAS H AGAIN BY SETTING AND CLEARING HDAL13 H.  THE
 9159                                          ;SIGNAL XCAS H WILL CLOCK THE OUTPUT OF THE 8 BIT ADDRESS LB FLIP-FLOP
 9160                                          ;(1) INTO THE 8 BIT ADDRESS HB FLIP-FLOP, THUS SETTING THE 8 BIT ADDRESS
 9161                                          ;HB FLIP-FLOP TO A ONE
 9162
 9163  023442  004737  007376          6$:     JSR     PC,XCAS                 ;GO PULSE XCAS H VI HDAL13 H.
 9164
 9165                                          ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO
 9166                                          ;BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING PULSED.
 9167                                          ;    PAUSE STATE WORKING - PSMW H - 1
 9168                                          ;    PAUSE STATE SYNC - EPSF H - 1
 9169                                          ;    8 BIT INSTRUCTION HB - EP8F H - 1
 9170                                          ;    8 BIT ADDRESS LB - EP8G H - 1
 9171                                          ;    8 BIT ADDRESS HB - EP8N H - 1
 9172
 9173  023446  052737  040000  002336          BIS     #VDAL14,R4GOOD          ;SETUP TO EXPECT EP8N H TO BE A 1
 9174  023454  004737  006654                  JSF     PC,READR4               ;GO CHECK VDAL AND PAUSE STATE MACHINE
 9175  023460  001405                          BEQ     7$                      ;IF OK THEN CONTINUE
 9176  023462                                  ERRDF   3,VDALRG,R4EROR         ;EP8N H PROBABLY NOT SET TO A 1
 9177  023462  104455                          TRAP    C$ERDF
 9178  023464  000003                          .WORD   3
 9179  023466  002537                          .WORD   VDALRG
 9180  023470  005004                          .WORD   R4EROR
 9181  023472                                  CKLOOP
 9182  023472  104406                          TRAP    C$CLP1
 9183
 9184                                          ;TOGGLE THE SIGNAL XPI L BY SETTING AND CLEARING HDAL15 H.  A PULSE
 9185                                          ;ON THE SIGNAL XPI L WILL CLEAR THE EDFET FLIP-FLOP, THUS DISABLING
```

```
 9186                                           ;THE DIRECT SET INPUT TO THE PAUSE STATE WORKING FLIP-FLOP.
 9187
 9188  023474  004737  007502          7$:     JSR     PC,XPI                  ;GO PULSE XPI L VIA HDAL15 H
 9189
 9190                                           ;READ THE VDAL AND PAUSE STATE MACHINE FLIP-FLOPS TO CHECK THAT XPI L
 9191                                           ;DID NOT CLEAR ANY OF THE PAUSE STATE MACHINE FLIP-FLOPS.
 9192
 9193  023500  004737  006654                  JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
 9194  023504  001405                          BEQ     8$                              ;IF NO CHANGES THEN CONTINUE
 9195  023506                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
 9196  023506  104455                          TRAP    C$ERDF
 9197  023510  000003                          .WORD   3
 9198  023512  002537                          .WORD   VDALRG
 9199  023514  005004                          .WORD   R4EROR
 9200  023516                                  CKLOOP
 9201  023516  104406                          TRAP    C$CLP1
 9202
 9203                                           ;SET THE SIGNAL VDAL2 H TO A ONE AND CHECK THE PAUSE STATE MACHINE FLIP-
 9204                                           ;FLOPS TO BE A ZERO.  VDAL2 H WILL THEN BE CLEARED.
 9205
 9206  023520  005037  002334          8$:     CLR     R4LOAD                  ;SETUP TO EXPECT PAUSE STATE CLEARED
 9207  023524  004737  007712                  JSR     PC,CLRPSM               ;PULSE INVD L VIA VDAL2 H
 9208
 9209  023530                                  ENDSEG
 9210  023530                          10000$:
 9211  023530  104405                          TRAP    C$ESEG
 9212  023532                                  ENDTST
 9213  023532                          L10065:
 9214  023532  104401                          TRAP    C$ETST
 9215
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                                .SBTTL  TEST 36: EOAI REG TO CAI, EIAI, CTL AND TO CTL REG TEST

                                ;++
                                ; THIS TEST WILL CHECK THAT THE EOAI REGISTER BITS 7:0 CAN BE LOADED AND READ
                                ; BACK CORRECTLY.  THE TEST WILL ALSO CHECK THE DATA PATH TO BE CONNECTED AND
                                ; FUNCTIONING PROPERLY FROM THE EOAI REGISTER TO THE EOAI BUS, TO THE CAI BUS,
                                ; TO THE EIAI BUS, TO THE CTL BUS AND INTO THE CTL REGISTER. THE TEST WILL CHECK
                                ; THE DATA PATH FROM THE EOAI REGISTER TO THE EOAI BUS, TO THE CAI BUS, TO THE
                                ; TAI BUS, TO THE TAI DIAGNOSTIC LATCH, AND BACK FROM THE TAI DIAGNOSTIC LATCH
                                ; TO THE CAI BUS, TO THE EIAI BUS, TO THE CTL BUS AND INTO THE CTL REGISTER. THE
                                ; DATA PATTERN USED DURING THIS TEST WILL BE AN INCREMENTING BINARY COUNT PATTERN.
                                ; THE DATA READBACK FROM THE CTL REGISTER WILL BE THE ONES COMPLEMENT OF THE DATA
                                ; LOADED INTO THE EOAI REGISTER.
                                ;--

023534                                  BGNTST
023534                          T36::
023534  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALZE TARGET EMULATOR
023540  005001                          CLR     R1                      ;START DATA PATTERN AT ZERO

023542                          1$:     BGNSEG
023542  104404                          TRAP    C$BSEG

                                        ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0

023544  004737  007006                  JSR     PC,SLMODR               ;SELECT MODE REG VIA GDAL BITS 2:0

                                        ;CLEAR ALL BITS IN THE MODE REGISTER AND CHECK THAT ALL BITS ARE CLEARED

023550  005037  002342                  CLR     R6LOAD                  ;SETUP TO CLEAR ALL BITS
023554  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
023560  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
023562                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO 0
023562  104455                          TRAP    C$ERDF
023564  000004                          .WORD   4
023566  002631                          .WORD   MODREG
023570  005020                          .WORD   R06ERR
023572                                  CKLOOP
023572  104406                          TRAP    C$CLP1

                                        ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

023574  004737  006754          2$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0

                                        ;SET HDAL2 H TO A ONE IN THE HDAL REGISTER TO ALLOW THE PROGRAM TO
                                        ;CONTROL THE T-11 TIMING AND CONTROL SIGNALS.

023600  012737  000004  002342          MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
023606  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
023612  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
023614                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL TO EXPECTED
023614  104455                          TRAP    C$ERDF
023616  000004                          .WORD   4
023620  002605                          .WORD   HDALRG
023622  005020                          .WORD   R06ERR
02 624                                  CKLOOP
```

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9272  023624  104406                          TRAP    C$CLP1
9273
9274                                          ;SET AND CLEAR VDAL2 H IN CONTROL REGISTER 4.  VDAL2 H BEING PULSED
9275                                          ;WILL CAUSE THE PAUSE STATE MACHINE FLIP-FLOPS TO BE CLEARED VIA THE
9276                                          ;SIGNALS INVD L AND INVD H.
9277
9278  023626  005037  002334        3$:     CLR     R4LOAD                  ;SETUP TO CLEAR ALL OTHER VDAL R/W BITS
9279  023632  004737  007712                JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
9280
9281                                          ;SET ADAL13 H AND ADAL10 H TO ONES IN THE ADAL REGISTER. THE SIGNAL
9282                                          ;ATC L WILL BE ASSERTED HIGH WHEN ADAL13 H IS A ONE, ADAL11 H IS A ZERO,
9283                                          ;THE PAUSE STATE WORKING FLIP-FLOP IS A ZERO, AND PPI L IS ASSERTED HIGH.
9284                                          ;ADAL10 H ON A ONE WILL ENABLE THE EIAI 7:0 BUS TO THE CTL 7:0 BUS.
9285
9286  023636  012737  022000  002330        MOV     #ADAL13!ADAL10,R2LOAD   ;SETUP BITS TO BE LOADED
9287  023644  004737  006614                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
9288  023650  001405                        BEQ     4$                      ;IF LOADED OK THEN CONTINUE
9289  023652                                ERRDF   2,ADALRG,R2L OR         ;ADAL REGISTER NOT EQUAL EXPECTED
9290  023652  104455                        TRAP    C$ERDF
9291  023654  000002                        .WORD   2
9292  023656  002513                        .WORD   ADALRG
9293  023660  004770                        .WORD   R2EROR
9294  023662                                CKLOOP
9295  023662  104406                        TRAP    C$CLP1
9296
9297                                          ;SELECT FDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9298
9299  023664  004737  007154        4$:     JSR     PC,SLFDAL               ;GO SELECT FDAL REG VIA GDAL BITS 2:0
9300
9301                                          ;LOAD, READ AND CHECK EOAI REGISTER WITH A BINARY COUNT PATTERN. THE
9302                                          ;EOAI REGISTER IS THE HIGH BYTE OF THE FDAL REGISTER.  THE DATA
9303                                          ;PATTERN WILL BE LOADED INTO THE EOAI REGISTER VIA THE SIGNAL WPT2 HB H
9304                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTPOL REGISTER 6.  FDAL0 H WILL
9305                                          ;BE WRITTEN TO A ONE IN THE FDAL REGISTER AT THE SAME TIME THE EOAI
9306                                          ;REGISTER IS WRITTEN.  FDAL0 H ON A ONE WILL ENABLE THE EOAI REGISTER
9307                                          ;TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD OF THE
9308                                          ;CTL REGISTER.  THE EOAI REGISTER IS READBACK VIA THE SIGNAL RAT2 L.
9309
9310  023670  010137  002342                MOV     R1,R6LOAD               ;GET THE BINARY DATA PATTERN
9311  023674  005237  002342                INC     R6LOAD                  ;SET FDAL0 H TO A ONE
9312  023700  004737  006672                JSR     PC,LDRDR6               ;LOAD, READ AND CHECK EOAI AND FDAL REG
9313  023704  001405                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
9314  023706                                ERRDF   4,EOAIFD,R06ERR         ;EOAI OR FDAL REGISTER ERROR
9315  023706  104455                        TRAP    C$ERDF
9316  023710  000004                        .WORD   4
9317  023712  002676                        .WORD   EOAIFD
9318  023714  005020                        .WORD   R06ERR
9319  023716                                CKLOOP
9320  023716  104406                        TRAP    C$CLP1
9321
9322                                          ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9323
9324  023720  004737  006754        5$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
9325
9326                                          ;SET PPI L AND XPI L TO THE LOW STATE BY SETTING HDAL15 H TO A ONE.
9327                                          ;PPI L BEING SET LOW WILL CAUSE THE SIGNAL ATC ! TO BE ASSERTED LOW.
```

```
                                        ;ATC L ASSERTED LOW WILL ENABLE THE EOAI BUS ONTO THE CAI 7:0 BUS.  THE
                                        ;CAI BUS WILL BE ENABLED TO THE EIAI 7:0 BUS UNCONDITIONALLY.  THE
                                        ;EIAI BUS WILL BE ENABLED TO THE CTL 7:0 BUS VIA ADAL10 H ON A ONE.
                                        ;THE CAI 7:0 BUS WILL ALSO BE ENABLED TO THE TAI 7:0 BUS BY THE SIGNAL
                                        ;ATT L BEING ASSERTED LOW.  THE SIGNAL ATT L IS ASSERTED LOW AS A RESULT
                                        ;OF THE SIGNALS CPT L, MR9 L, AND DMG L BEING ASSERTED HIGH.

9335  023724  012737  000004  002342    MOV     #HDAL2,R6LOAD           ;SETUP BIT PREVIOUSLY LOADED
9336  023732  004737  007514            JSR     PC,XPIH                 ;SET PPI L AND XPI L TO LOW STATE

                                        ;SET AND CLEAR VDAL2 H IN THE VDAL REGISTER TO CLOCK THE TAI 7:0 BUS
                                        ;INTO THE TAI 7:0 DIAGNOSTIC LATCH.  THE DATA CLOCKED INTO THE TAI
                                        ;DIAGNOSTIC LATCH SHOULD BE THAT WHICH WAS WRITTEN INTO THE EOAI REG.

9342  023736  004737  007712            JSR     PC,CLRPSM               ;GO PULSE VDAL2 H TO CLOCK TAI INTO LATCH

                                        ;AT THIS TIME, THE EOAI BUS IS ENABLED TO THE CAI BUS VIA THE SIGNAL
                                        ;ATC L. THE CAI BUS IS ENABLED TO THE EIAI BUS UNCODITIONALLY. THE
                                        ;EIAI BUS IS ENABLED TO THE CTL BUS VIA ADAL10 H ON A ONE.  TO CHECK
                                        ;THAT THE EOAI BUS IS ENABLED TO THE CTL BUS, THE TEST MUST FIRST
                                        ;CLOCK THE CTL BUS DATA INTO THE CTL REGISTER BY PULSING THE SIGNAL
                                        ;XCAS L.  THE SIGNAL XCAS L IS PULSED BY SETTING AND CLEARING HDAL13 H.

9351  023742  004737  007376            JSR     PC,XCAS                 ;PULSE XCAS L VIA HDAL REGISTER BIT 13

                                        ;SET PPI L AND XPI L TO THE HIGH STATE BY CLEARING THE SIGNAL HDAL15 H.
                                        ;THE EOAI BUS WILL BE DISABLED FROM THE CAI BUS BY ATC L BEING SET
                                        ;HIGH WHEN THE SIGNAL PPI L IS RETURNED TO THE HIGH STATE.

9357  023746  004737  007546            JSR     PC,XPIL                 ;GO SET PPI L AND XPI L TO HIGH STATE

                                        ;SELECT FDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

9361  023752  004737  007154            JSR     PC,SLFDAL               ;GO SELECT FDAL REG VIA GDAL BITS 2:0

                                        ;WRITE THE DATA PATTERN 314 INTO THE EOAI REGISTER VIA THE SIGNAL WPT2
                                        ;HB H.  THIS IS DONE TO CHECK THAT THE CTL REGISTER IS READBACK ON A
                                        ;READ COMMAND TO CONTROL REGISTER 6 INSTEAD OF THE EOAI REGISTER.  THE
                                        ;SIGNAL FDAL0 H WILL BE WRITTEN TO A ZERO TO SELECT THE CTL REGISTER
                                        ;TO BE READ VIA THE SIGNAL ROT2 L WHEN A READ COMMAND IS ISSUED TO
                                        ;CONTROL REGISTER 6.

9370  023756  012777  146000  156322    MOV     #146000,@REG6           ;WRITE EOAI AND FDAL REGISTER

                                        ;READ THE CTL AND FDAL REGISTER TO CHECK THAT XCAS L CLOCKED THE CTL
                                        ;7:0 BUS INTO THE CTL REGISTER. THE CTL REGISTER WILL BE READBACK VIA
                                        ;THE SIGNAL ROT2 L WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
                                        ;THE DATA READBACK WILL BE THE ONES COMPLEMENT OF THE DATA WHICH WAS
                                        ;WRITTEN INTO THE EOAI REGISTER AT THE BEGINNING OF THIS TEST.

9378  023764  010137  002342            MOV     R1,R6LOAD               ;SETUP DATA LOADED INTO EOAI
9379  023770  005137  002342            COM     R6LOAD                  ;MAKE THE 1'S COMPLEMENT FOR READBACK
9380  023774  042737  000377  002342    BIC     #377,R6LOAD             ;CLEAR THE FDAL REGISTER BITS
9381  024002  004737  006700            JSR     PC,READR6               ;GO READ CTL AND FDAL REGISTER
9382  024006  001405                    BEQ     6$                      ;IF DATA OK THEN CONTINUE
9383  024010                            ERRDF   4,CTLFDL,R026ER         ;CTL OR FDAL REGISTER ERROR
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 9384  024010  104455                          TRAP    C$ERDF
 9385  024012  000004                          .WORD   4
 9386  024014  003232                          .WORD   CTLFDL
 9387  024016  005034                          .WORD   R026ER
 9388  024020                                  CKLOOP
 9389  024020  104406                          TRAP    C$CLP1
 9390
 9391                                          ;LOAD, READ AND CHECK EOAI REGISTER WITH THE 1'S COMPLEMENT OF THE
 9392                                          ;DATA PREVIOUSLY WRITTEN INTO IT.  THIS IS DONE TO SETUP TO CHANGE THE
 9393                                          ;DATA IN THE CTL REGISTER.  THE CTL REGISTER DATA NEEDS TO BE CHANGED
 9394                                          ;SO THAT THE DATA PATH TO AND FROM THE TAI 7:0 DAIGNOSTIC LATCH CAN BE
 9395                                          ;CHECKED AT A LATER TIME IN THIS TEST.
 9396
 9397  024022  010137  002342          6$:     MOV     R1,R6LOAD               ;GET THE DATA PATTERN JUST LOADED
 9398  024026  005137  002342                  COM     R6LOAD                  ;MAKE THE 1'S COMPLEMENT OF IT
 9399  024032  042737  000376  002342          BIC     #376,R6LOAD             ;CLEAR FDAL BITS 7:1 - FDAL0 H = 1
 9400  024040  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK EOAI AND FDAL REG
 9401  024044  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
 9402  024046                                  ERRDF   4,EOAIFD,R06ERR         ;EOAI OR FDAL REGISTER ERROR
 9403  024046  104455                          TRAP    C$ERDF
 9404  024050  000004                          .WORD   4
 9405  024052  002676                          .WORD   EOAIFD
 9406  024054  005020                          .WORD   R06ERR
 9407  024056                                  CKLOOP
 9408  024056  104406                          TRAP    C$CLP1
 9409
 9410                                          ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
 9411
 9412  024060  004737  006754          7$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
 9413
 9414                                          ;SET PPI L AND XPI L TO THE LOW STATE BY SETTING HDAL15 H TO A ONE.
 9415                                          ;PPI L BEING SET LOW WILL CAUSE THE SIGNAL ATC L TO BE ASSERTED LOW.
 9416                                          ;ATC L WILL ENABLE THE EOAI BUS TO THE CAI BUS. THE CAI BUS WILL BE
 9417                                          ;ENABLED TO THE EIAI BUS UNCODIONALLY.  THE EIAI BUS WILL BE ENABLED TO
 9418                                          ;THE CTL BUS VIA ADAL10 H ON A ONE.
 9419
 9420  024064  012737  000004  002342          MOV     #HDAL2,R6LOAD           ;SETUP BIT PREVIOULY LOADED
 9421  024072  004737  007514                  JSR     PC,XPIH                 ;SET PPI L AND XPI L TO LOW STATE
 9422
 9423                                          ;TOGGLE THE SIGNAL XCAS L BY SETTING AND CLEARING THE SIGNAL HDAL13 H.
 9424                                          ;THE SIGNAL XCAS L WILL CLOCK THE CTL BUS DATA, WHICH CONTAINS THE EOAI
 9425                                          ;BUS DATA, INTO THE CTL REGISTER.
 9426
 9427  024076  004737  007376                  JSR     PC,XCAS                 ;GO PULSE XCAS L VIA HDAL13 H
 9428
 9429                                          ;SET THE SIGNALS PPI L AND XPI L TO THE HIGH STATE BY CLEARING HDAL15 H.
 9430                                          ;WHEN PPI L AND XPI L ARE ASSERTED HIGH, THE EOAI BUS WILL BE DISABLED
 9431                                          ;FROM THE CAI BUS.
 9432
 9433  024102  004737  007546                  JSR     PC,XPIL                 ;SET PPI L AND XPI L TO HIGH STATE
 9434
 9435                                          ;SELECT FDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
 9436
 9437  024106  004737  007154                  JSR     PC,SLFDAL               ;GO SELECT FDAL REG VIA GDAL BITS 2:0
 9438
 9439                                          ;WRITE THE DATA PATTERN 063 INTO THE EOAI REGISTER VIA THE SIGNAL WPT2
```

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                                        ;HB H.  THIS IS DONE TO CHECK THAT THE CTL REGISTER IS READBACK VIA
                                        ;THE SIGNAL ROT2 L INSTEAD OF THE EOAI REGISTER.  FDALO H WILL BE WRITTEN
                                        ;TO A ZERO TO SELECT THE CTL REGISTER

024112  012777  031400  156166          MOV     #031400,@REG6           ;WRITE EOAI AND FDAL REGISTER

                                        ;READ THE CTL AND FDAL REGISTERS TO CHECK THAT XCAS L CLOCKED THE CTL
                                        ;BUS INTO THE CTL REGISTER.  THE DATA PATTERN READBACK WILL BE THE
                                        ;ONES COMPLEMENT OF THAT WHICH WAS WRITTEN INTO THE EOAI REGISTER.

024120  010137  002342                  MOV     R1,R6LOAD               ;GET THE 1'S COMPLEMENT OF DATA LOADED
024124  004737  006700                  JSR     PC,READR6               ;GO READ CTL AND FDAL REGISTER
024130  001405                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
02 132                                  ERRDF   4,CTLFDL,R026ER         ;CTL OR FDAL REGISTER ERROR
024132  104455                          TRAP    C$ERDF
024134  000004                          .WORD   4
024136  003232                          .WORD   CTLFDL
024140  005034                          .WORD   R026ER
024142                                  CKLOOP
024142  104406                          TRAP    C$CLP1

                                        ;SET ADAL13 H TO A ZERO IN THE ADAL REGISTER.  ADAL13 H ON A ZERO WILL
                                        ;ALLOW THE SIGNALS ABT H AND ABT L TO BE ASSERTED HIGH AND LOW RESPEC-
                                        ;TIVELY WHEN THE SIGNAL PPI L IS ASSERTED LOW.  THE SIGNALS ABT H AND
                                        ;ABT L WILL ENABLE THE TAI BUS TO THE CAI BUS WHEN ASSERTED.

024144  042737  020000  002330  8$:     BIC     #ADAL13,R2LOAD          ;SETUP TO ZERO ADAL13
024152  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
024156  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
024160                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
024160  104455                          TRAP    C$ERDF
024162  000002                          .WORD   2
024164  002513                          .WORD   ADALRG
024166  004770                          .WORD   R2EROR
024170                                  CKLOOP
024170  104406                          TRAP    C$CLP1

                                        ;SELECT MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

024172  004737  007006          9$:     JSR     PC,SLMODR               ;GO SELECT MODE REG VIA GDAL BITS 2:0

                                        ;SET MODE REGISTER BIT 9 TO A ONE.  THIS IS DONE TO SET THE SIGNAL ATT L
                                        ;TO THE HIGH STATE.  WHEN THE SIGNAL ATT L IS ASSERTED HIGH, THE CAI
                                        ;BUS WILL BE DISABLED TO THE TAI BUS AND THE  AI DIAGNOSTIC LATCH WILL
                                        ;BE ALLOWED TO DRIVE THE TAI BUS.

024176  012737  001000  002342          MOV     #MR9,R6LOAD             ;SETUP BIT TO BE LOADED
024204  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
024210  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
024212                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
024212  104455                          TRAP    C$ERDF
024214  000004                          .WORD   4
024216  002631                          .WORD   MODREG
024220  005020                          .WORD   R06ERR
024222                                  CKLOOP
024222  104406                          TRAP    C$CLP1
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 9496
 9497                                   ;SET VDAL0 H TO A ONE TO ENABLE THE TAI DAIGNOSTIC LATCH ONTO THE TAI
 9498                                   ;7:0 BUS.  THE TAI DIAGNOSTIC LATCH WAS LOADED WITH THE FIRST EOAI
 9499                                   ;DATA PATTERN AT THE BEGINNING OF THIS TEST.
 9500
 9501  024224  052737  000001  002334  10$:  BIS     #VDAL0,R4LOAD          ;SETUP BIT TO BE LOADED
 9502  024232  004737  006640                JSR     PC,LDFSR4              ;GO LOAD, READ AND CHECK VDAL REGISTER
 9503  024236  001405                       BEQ     11$                    ;IF LOADED OK THEN CONTINUE
 9504  024240                                ERRDF   3,VDALRG,R4EROR        ;VDAL OR PAUSE STATE MACHINE ERROR
 9505  024240  104455                       TRAP    C$ERDF
 9506  024242  000003                       .WORD   3
 9507  024244  002537                       .WORD   VDALRG
 9508  024246  005004                       .WORD   R4EROR
 9509  024250                                CKLOOP
 9510  024250  104406                       TRAP    C$CLP1
 9511
 9512                                   ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
 9513
 9514  024252  004737  006754          11$:  JSR     PC,SLHDAL              ;GO SELECT HDAL REG VIA GDAL BITS 2:0
 9515
 9516                                   ;SET THE SIGNALS PPI L AND XPI L TO THE LOW STATE BY SETTING HDAL
 9517                                   ;REGISTER BIT 15 TO A ONE IN THE HDAL REGISTER.  WHEN PPI L IS ASSERTED
 9518                                   ;LOW THE SIGNALS ABT H AND ABT L WILL BE ASSERTED HIGH AND LOW RESPECTIVELY.
 9519                                   ;THESE TWO SIGNALS WILL ENABLE THE TAI BUS, WHICH CONTAINS THE TAI
 9520                                   ;DIAGNOSTIC LATCH DATA, ONTO THE CAI BUS.  THE CAI BUS WILL BE ENABLED
 9521                                   ;TO THE EIAI BUS.  THE EIAI BUS WILL BE ENABLED TO THE CTL BUS VIA THE
 9522                                   ;SIGNAL ADAL10 H BEING SET TO A ONE.
 9523
 9524  024256  012737  000004  002342       MOV     #HDAL2,R6LOAD          ;SETUP BIT PREVIOUSLY LOADFD
 9525  024264  004737  007514               JSR     PC,XPIH                ;;SET PPI L AND XPI L TO LOW STATE
 9526
 9527                                   ;TO CLOCK THE CTL BUS DATA, WHICH CONTAINS THE TAI DIAGNOSTIC LATCH
 9528                                   ;DATA, INTO THE CTL REGISTER, THE TEST WILL PULSE THE SIGNAL XCAS L
 9529                                   ;BY SETTING AND CLEARING THE SIGNAL HDAL13 H.
 9530
 9531  024270  004737  007376               JSR     PC,XCAS                ;GO PULSE XCAS L VIA HDAL13 H
 9532
 9533                                   ;SET THE SIGNALS PPI L AND XPI L TO THE HIGH STATE BY CLEARING HDAL15 H.
 9534                                   ;WHEN PPI L AND XPI L ARE ASSERTED HIGH, THE TAI BUS WILL BE DISABLED
 9535                                   ;FROM THE CAI BUS.
 9536
 9537  024274  004737  007546               JSR     PC,XPIL                ;SET PPI L AND XPI L TO HIGH STATE
 9538
```

```
9539
9540                                        ;SELECT THE FDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9541
9542  024300  004737  007154                JSR     PC,SLFDAL               ;SELECT FDAL REGISTER VIA GDAL BITS 2:0
9543
9544                                        ;READ THE CTL AND FDAL REGISTER TO CHECK THAT XCAS L CLOCKED THE CTL
9545                                        ;BUS WHICH CONTAINED THE TAI DIAGNOSTIC LATCH DATA INTO THE CTL
9546                                        ;REGISTER.
9547
9548  024304  010137  002342                MOV     R1,R6LOAD               ;GET THE FIRST EOAI DATA PATTERN
9549  024310  005137  002342                COM     R6LOAD                  ;SETUP 1'S COMPLEMENT FOR READBACK
9550  024314  042737  000377  002342        BIC     #377,R6LOAD             ;SETUP FDAL BITS TO BE ZERO
9551  024322  004737  006700                JSR     PC,READR6               ;GO READ CTL AND FDAL REGISTERS
9552  024326  001404                        BEQ     12$                     ;IF DATA OK THEN CONTINUE
9553  024330                                ERRDF   4,CTLFDL,R026ER         ;TAI LATCH TO CTL REGISTER ERROR
9554  024330  104455                        TRAP    C$ERDF
9555  024332  000004                        .WORD   4
9556  024334  003232                        .WORD   CTLFDL
9557  024336  005034                        .WORD   R026ER
9558  024340                        12$:    ENDSEG
9559  024340                        10000$:
9560  024340  104405                        TRAP    C$ESEG
9561
9562  024342  062701  000400                ADD     #BIT8,R1                ;UPDATE THE TEST PATTERN BY ONE
9563  024346  001402                        BEQ     13$                     ;IF DONE THEN EXIT
9564  024350  000137  023542                JMP     1$                      ;GO DO NEXT TEST PATTERN
9565  024354                        13$:    ENDTST
9566  024354                        L10066:
9567  024354  104401                        TRAP    C$ETST
```

```
                                        .SBTTL  TEST 37: MODE REG TO ADDRESS BUS VIA EODAL, CDAL AND EIDAL BUS

                                        ;++
                                        ; THIS TEST WILL CHECK THE DATA PATH FROM THE MODE REGISTER TO THE ADDRESS BUS.
                                        ; TO DO THIS, THE TEST WILL ENABLE THE DATA PATH FROM THE MODE REGISTER TO THE
                                        ; EODAL BUS, TO THE CDAL BUS, TO THE EIDAL BUS, AND TO THE ADDRESS BUS.  THIS IS
                                        ; DONE BY SETTING XBCLR H AND PBCLR H TO THE HIGH STATE AND BY SETTING ADAL12 H
                                        ; AND ADAL10 H TO ONES.  THE TARGET MODE READBACK REGISTER WILL ALSO BE CHECKED
                                        ; TO HAVE BEEN LOADED WITH THE EIDAL BUS DATA WHEN THE SIGNAL XBCLR L IS SET TO
                                        ; THE HIGH STATE FROM THE LOW STATE.  THE MODE REGISTER WILL BE LOADED WITH THE
                                        ; FOLLOWING DATA PATTERNS, 146063, 031714, 125252, 052525, 177777 AND 000000.
                                        ; FOR EACH DATA PATTERN LOADED, THE PROGRAM WILL CHECK THE DATA TO BE PRESENT ON
                                        ; THE THE EODAL BUS, THE EIDAL BUS, AND THE ADDRESS BUS.  THE TEST WILL ALSO
                                        ; CHECK THAT EACH PATTERN CAN BE LOADED INTO THE TARGET MODE READBACK REGISTER.
                                        ;--

024356                                          BGNTST
024356                                  T37::
024356  004737  005510                            JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
024362  012701  024670                            MOV     #8$,R1                  ;SETUP DATA TABLE POINTER
024366  012702  000006                            MOV     #6,R2                   ;SETUP DATA PATTERN COUNTER

024372                                  1$:     BGNSEG
024372  104404                                  TRAP    C$BSEG

                                                ;SET VDAL2 H TO A ONE AND THEN ZERO TO PULSE THE SIGNALS INVD L AND
                                                ;INVD H.  THESE SIGNALS WILL CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS.

024374  005037  002334                        CLR     R4LOAD                  ;SETUP TO CLEAR ALL VDAL REG BITS
024400  004737  007712                        JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H

                                                ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0

024404  004737  006754                        JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0

                                                ;SET HDAL2 H AND HDAL7 H TO ONES IN THE HDAL REGISTER.  ALL OTHER HDAL
                                                ;BITS WILL BE SET TO ZEROES.  HDAL2 H ON A ONE WILL ALLOW THE PROGRAM
                                                ;TO MANIPULATE THE T-11 TIMING AND CONTROL SIGNALS.  HDAL7 H ON A ONE
                                                ;WILL CAUSE THE SIGNALS XBCLR H AND PBCLR H TO BE ASSERTED HIGH. HDAL9 H
                                                ;ON A ZERO WILL ENABLE THE EIDAL BUS TO THE ADDRESS BUS WHEN ADAL10 H IS
                                                ;SET TO A ONE.

024410  012737  000004  002342                MOV     #HDAL2,R6LOAD           ;SETUP DIAGNOSTIC CONTROL BIT
024416  004737  007620                        JSR     PC,XBCLRH               ;SET XBCLR H AND PBCLR H TO HIGH STATE

                                                ;SET ADAL12 H AND ADAL10 H TO ONES IN THE ADAL REGISTER.  ADAL12 H BEING
                                                ;SET HIGH WITH XBCLR H ASSERTED HIGH WILL ENABLE THE MODE REGISTER DATA
                                                ;TO THE EODAL BUS.  ADAL12 H BEING SET HIGH WITH PBCLR H ASSERTED HIGH
                                                ;WILL CAUSE THE SIGNALS COHB L AND COLB L TO BE ASSERTED LOW.  THESE
                                                ;TWO SIGNALS WILL ENABLE THE EODAL BUS TO THE CDAL BUS.  THE CDAL BUS
                                                ;WILL BE ENABLED TO THE EIDAL BUS UNCONDITIONALLY.  ADAL10 H BEING SET
                                                ;TO A ONE WITH HDAL9 H BEING SET TO A ZERO WILL ENABLE THE EIDAL BUS TO
                                                ;THE ADDRESS BUS.

024422  012737  012000  002330                MOV     #ADAL12!ADAL10,R2LOAD   ;SETUP BITS TO BE LOADED
024430  004737  006614                        JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
```

```
 9624  024434  001405                    BEQ     2$                      ;IF LOADED OK THEN CONTINUE
 9625  024436                            ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
 9626  024436  104455                    TRAP    C$ERDF
 9627  024440  000002                    .WORD   2
 9628  024442  002513                    .WORD   ADALRG
 9629  024444  004770                    .WORD   R2EROR
 9630  024446                            CKLOOP
 9631  024446  104406                    TRAP    C$CLP1
 9632
 9633                                    ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
 9634
 9635  024450  004737  007006    2$:     JSR     PC,SLMODR               ;SELECT MODE REG VIA GDAL BITS 2:0
 9636
 9637                                    ;LOAD, READ AND CHECK MODE REGISTER WITH DATA PATTERN FROM DATA TABLE.
 9638
 9639  024454  011137  002342            MOV     (R1),R6LOAD             ;GET THE DATA FROM THE DATA TABLE
 9640  024460  004737  006672            JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
 9641  024464  001405                    BEQ     3$                      ;IF LOADED OK THEN CONTINUE
 9642  024466                            ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
 9643  024466  104455                    TRAP    C$ERDF
 9644  024470  000004                    .WORD   4
 9645  024472  002631                    .WORD   MODREG
 9646  024474  005020                    .WORD   R06ERR
 9647  024476                            CKLOOP
 9648  024476  104406                    TRAP    C$CLP1
 9649
 9650                                    ;SELECT EODAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
 9651
 9652  024500  004737  007122    3$:     JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
 9653
 9654                                    ;THE MODE REGISTER IS ENABLED TO THE EODAL BUS WHEN XBCLR H IS
 9655                                    ;ASSERTED HIGH AND ADAL12 H IS SET TO A ONE.  READ AND CHECK THE EODAL
 9656                                    ;BUS TO CONTAIN THE DATA LOADED INTO THE MODE REGISTER.
 9657
 9658  024504  011137  002342            MOV     (R1),R6LOAD             ;GET THE MODE REGISTER DATA
 9659  024510  004737  006700            JSR     PC,READR6               ;READ AND CHECK EODAL BUS TO = MODE REG
 9660  024514  001405                    BEQ     4$                      ;IF DATA = MODE REG THEN CONTINUE
 9661  024516                            ERRDF   4,MEODAL,R026ER         ;MODE REG TO EODAL BUS ERROR
 9662  024516  104455                    TRAP    C$ERDF
 9663  024520  000004                    .WORD   4
 9664  024522  003102                    .WORD   MEODAL
 9665  024524  005034                    .WORD   R026ER
 9666  024526                            CKLOOP
 9667  024526  104406                    TRAP    C$CLP1
 9668
 9669                                    ;SELECT THE EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
 9670
 9671  024530  004737  007240    4$:     JSR     PC,SEIDAL               ;SELECT EIDAL BUS VIA GDAL BITS 2:0
 9672
 9673                                    ;AT THIS POINT IN TIME, THE MODE REGISTER IS ENABLED TO THE EODAL BUS
 9674                                    ;VIA XBCLR H AND ADAL12 H.  THE EODAL BUS IS ENABLED TO THE CDAL BUS
 9675                                    ;VIA THE SIGNALS COHB L AND COLB L.  THE SIGNALS COHB L AND COLB L ARE
 9676                                    ;ASSERTED LOW AS A RESULT OF PBCLR H BEING ASSERTED HIGH AND ADAL12 H
 9677                                    ;BEING SET TO A ONE.  THE CDAL BUS IS ENABELED TO THE EIDAL BUS UNCON-
 9678                                    ;DITIONALLY.  READ AND CHECK THE EIDAL BUS TO CONTAIN THE MODE REGISTER
 9679                                    ;DATA.
```

```
9680
9681  024534  011137  002342              MOV     (R1),R6LOAD             ;GET THE MODE REGISTER DATA LOADED
9682  024540  004737  006700              JSR     PC,READR6               ;CHECK EIDAL BUS TO = MODE REG DATA
9683  024544  001405                      BEQ     5$                      ;IF DATA = MODE REG DATA THEN CONT
9684  024546                              ERRDF   4,MEIDAL,R026ER         ;MODE REG TO EIDAL BUS ERROR
9685  024546  104455                      TRAP    C$ERDF
9686  024550  000004                      .WORD   4
9687  024552  003270                      .WORD   MEIDAL
9688  024554  005034                      .WORD   R026ER
9689  024556                              CKLOOP
9690  024556  104406                      TRAP    C$CLP1
9691
9692                                      ;SELECT THE ADDRESS BUS VIA THE GDAL BITS 2:0 IN CONTROL REGISTER 0
9693
9694  024560  004737  007072      5$:     JSR     PC,SLDADR               ;SELECT ADDRESS BUS VIA GDAL BITS 2:0
9695
9696                                      ;THE EIDAL BUS WILL BE ENABLED TO THE ADDRESS BUS AT THIS TIME AS A
9697                                      ;RESULT OF HDAL9 H BEING A ZERO AND ADAL10 H BEING A ONE.  THE EIDAL
9698                                      ;BUS PRESENTLY CONTAINS THE MODE REGISTER DATA.
9699
9700  024564  011137  002342              MOV     (R1),R6LOAD             ;GET THE MODE REGISTER DATA
9701  024570  004737  006700              JSR     PC,READR6               ;CHECK ADDRESS BUS TO = MODE REG DATA
9702  024574  001405                      BEQ     6$                      ;IF ADDRESS BUS = MODE REG DATA THEN CONT
9703  024576                              ERRDF   4,MADDRS,R026ER         ;MODE REG TO ADDRESS BUS EEROR
9704  024576  104455                      TRAP    C$ERDF
9705  024600  000004                      .WORD   4
9706  024602  003377                      .WORD   MADDRS
9707  024604  005034                      .WORD   R026ER
9708  024606                              CKLOOP
9709  024606  104406                      TRAP    C$CLP1
9710
9711                                      ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
9712
9713  024610  004737  006754      6$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
9714
9715                                      ;SET THE SIGNAL XBCLR L, WHICH IS PRESENTLY ASSERTED LOW, TO THE HIGH
9716                                      ;STATE BY CLEARING HDAL7 H IN THE HDAL REGISTER.  SETTING XBCLR L TO THE
9717                                      ;HIGH STATE WILL CLOCK THE EIDAL BUS, WHICH CONTAINS MODE REGISTER DATA,
9718                                      ;INTO THE TARGET MODE READBACK REGISTER.  SETTING XBCLR H TO THE LOW
9719                                      ;STATE WILL DISABLE THE MODE REGISTER DATA FROM THE EODAL BUS.
9720
9721  024614  012737  000204  002342      MOV     #HDAL7!HDAL2,R6LOAD     ;SETUP BITS PREVIOUSLY LOADED
9722  024622  004737  007652              JSR     PC,XBCLRL               ;SET XBCLR H TO THE LOW STATE
9723
9724                                      ;SELECT THE TARGET MODE READBACK REGISTER VIA GDAL BITS 2:0
9725
9726  024626  004737  007206              JSR     PC,SELTMR               ;SELECT TARGET MODE READBACK REG VIA GDAL BITS 2
9727
9728                                      ;READ AND CHECK THE TARGET MODE READBACK REGISTER TO CHECK THAT THE
9729                                      ;EIDAL BUS DATA WAS CLOCKED INTO IT WHEN THE SIGNAL XBCLR L WAS SET TO
9730                                      ;THE HIGH STATE.  THE EIDAL BUS CONTAINED THE MODE REGISTER DATA AT THE
9731                                      ;TIME THE SIGNAL XBCLR L WAS SET HIGH.  THE TARGET MODE READBACK REGIS-
9732                                      ;TER WILL BE READBACK TO THE LSI-11 VIA THE SIGNAL RPT5 L WHEN A READ
9733                                      ;COMMAND IS ISSUED TO CONTROL REGISTER 6.
9734
9735  024632  011137  002342              MOV     (R1),R6LOAD             ;GET THE MODE REGISTER DATA
```

```
 9736  024636  004737  006700                  JSR     PC,READR6               ;CHECK TMR TO = MODE REG DATA
 9737  024642  001404                          BEQ     7$                      ;IF DATA = MODE REG THEN CONTINUE
 9738  024644                                  ERRDF   4,MTOTMR,R026ER         ;MODE REGISTER TO TARGET MODE REG ERROR
 9739  024644  104455                          TRAP    C$ERDF
 9740  024646  000004                          .WORD   4
 9741  024650  003335                          .WORD   MTOTMR
 9742  024652  005034                          .WORD   R026ER
 9743  024654                          7$:     ENDSEG
 9744  024654                          10000$:
 9745  024654  104405                          TRAP    C$ESEG
 9746
 9747  024656  005721                          TST     (R1)+                   ;UPDATE DATA TABLE POINTER
 9748  024660  005302                          DEC     R2                      ;DECREMENT DATA TABLE COUNTER
 9749  024662  001410                          BEQ     9$                      ;IF 0 THEN ALL PATTERNS DONE
 9750  024664  000137  024372                  JMP     1$                      ;GO DO NEXT PATTERN
 9751
 9752  024670  146063                  8$:     .WORD   146063
 9753  024672  031714                          .WORD   031714
 9754  024674  125252                          .WORD   125252
 9755  024676  052525                          .WORD   052525
 9756  024700  177777                          .WORD   177777
 9757  024702  000000                          .WORD   000000
 9758
 9759  024704                          9$:     ENDTST
 9760  024704                          L10067:
 9761  024704  104401                          TRAP    C$ETST
 9762
```

```
                                .SBTTL  TEST 38: OLD FJA TO ADDRESS BUS VIA EODAL, CDAL, + EIDAL BUSSES

                                ;++
                                ; THIS TEST WILL CHECK THE DATA PATH FROM THE DIAGNOSTIC ADDRESS REGISTER TO THE
                                ; OLD FORCE JUMP ADDRESS REGISTER, TO THE EODAL BUS, TO THE EIDAL BUS, AND TO
                                ; THE ADDRESS BUS.  THIS PART OF THE TEST USES THE PAUSE STATE MACHINE LOGIC TO
                                ; LOAD THE OLD FORCE JUMP ADDRESS REGISTER AND TO PLACE THE OLD FORCE JUMP
                                ; ADDRESS REGISTER DATA ONTO THE EODAL BUS.  WHEN THE OLD FORCE JUMP ADDRESS
                                ; REGISTER DATA IS ENABLED TO THE EODAL BUS, THE TEST WILL ENABLE THE DATA TO
                                ; THE TDAL BUS AND LATCH THE DATA INTO THE TDAL DIAGNOSTIC LATCHES.  THE NEXT
                                ; PART OF THE TEST WILL CHECK THAT THE TDAL DIAGNOSTIC LATCHES CAN BE ENABLED
                                ; TO THE EIDAL BUS AND THAT THE EIDAL BUS CAN BE ENABLED TO THE EODAL BUS THROUGH
                                ; THE DATA BUS.
                                ;--

 024706                                 BGNTST
 024706                         T38::
 024706  004737  005510                 JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
 024712  012701  026114                 MOV     #23$,R1                 ;GET ADDRESS OF DATA TABLE
 024716  012702  000006                 MOV     #6,R2                   ;COUNTER FOR NUMBER OF DATA PATTERNS

 024722                         1$:     BGNSEG
 024722  104404                         TRAP    C$BSEG
 024724  005037  002346                 CLR     R6MASK                  ;CLEAR MASK FOR REG 6

                                        ;SELECT THE MODE REG BY SETTING GDAL2 TO A ONE AND GDAL1 AND GDAL0 TO A ZERO.

 024730  004737  007006                 JSR     PC,SLMODR               ;GO SELECT MODE REG VIA CONTROL REG 0

                                        ;LOAD, READ AND CHECK MODE REGESTER BITS MR 15:0 WITH ZEROES. MR BIT 11
                                        ;ON A ZERO WILL ENABLE 16 BIT ADDRESS SELECTION TO THE PAUSE STATE MACHINE

 024734  005037  002342                 CLR     R6LOAD                  ;SETUP DATA TO BE ZERO
 024740  004737  006672                 JSR     PC,LDRDR6               ;LOAD, READ AND CHECK MODE REGISTER
 024744  001405                         BEQ     2$                      ;IF LOADED OK THEN CONTINUE
 024746                                 ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO 0
 024746  104455                         TRAP    C$ERDF
 024750  000004                         .WORD   4
 024752  002631                         .WORD   MODREG
 024754  005020                         .WORD   R06ERR
 024756                                 CKLOOP
 024756  104406                         TRAP    C$CLP1

                                        ;SET GDAL1 AND GDAL0 TO ONES IN THE GDAL REGISTER TO SELECT THE HDAL
                                        ;REGISTER ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6.

 024760  004737  006754         2$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0

                                        ;LOAD, READ AND CHECK HDAL REGISTER WITH HDAL9 H AND HDAL2 H SET TO ONES.
                                        ;HDAL9 H SET TO A ONE WILL ENABLE THE OUTPUTS OF THE DIAGNOSTIC ADDRESS
                                        ;REGISTER ONTO THE ADDRESS BUS AND DISABLE THE EIDAL BUS FROM THE ADDRESS
                                        ;BUS.  HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
                                        ;TIMING AND CONTROL SIGNALS.

 024764  012737  001004  002342         MOV     #HDAL9!HDAL2,R6LOAD     ;SETUP BITS TO BE LOADED
 024772  004737  006672                 JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
```

```
9819  024776  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
9820  025000                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
9821  025000  104455                          TRAP    C$ERDF
9822  025002  000004                          .WORD   4
9823  025004  002605                          .WORD   HDALRG
9824  025006  005020                          .WORD   R06ERR
9825  025010                                  CKLOOP
9826  025010  104406                          TRAP    C$CLP1
9827
9828                                          ;SELECT THE DIAGNOSTIC ADDRESS REGISTER BY SETTING GDAL BITS 2:0 TO
9829                                          ;ZEROES.  ON A WRITE OR READ COMMAND TO CONTROL REGISTER 6, THE DIAG-
9830                                          ;NOSTIC ADDRESS REGISTER WILL BE SELECTED.
9831
9832  025012  004737  007072          3$:     JSR     PC,SLDADR               ;GO SELECT DIAG. ADDRESS REG VIA GDAL 2:0
9833
9834                                          ;LOAD, READ AND CHECK THE DIAGNOSTIC ADDRESS REGISTER WITH ONE OF THE
9835                                          ;FOLLOWING DATA PATTERNS: 125252, 052525, 177400, 000377, 177777, + 000000.
9836
9837  025016  011137  002342                  MOV     (R1),R6LOAD             ;GET DATA PATTERN RFOM TABLE
9838  025022  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD READ AND CHECK DIAG ADDRESS REG
9839  025026  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
9840  025030                                  ERRDF   4,ADDRRG,R06ERR         ;DIAG ADDRESS REG NOT EQUAL EXPECTED
9841  025030  104455                          TRAP    C$ERDF
9842  025032  000004                          .WORD   4
9843  025034  002735                          .WORD   ADDRRG
9844  025036  005020                          .WORD   R06ERR
9845  025040                                  CKLOOP
9846  025040  104406                          TRAP    C$CLP1
9847
9848                                          ;SET ADAL13 H, ADAL10 H AND ADAL0 H TO 1'S AND ALL OTHER ADAL BITS TO 0.
9849                                          ;ADAL0 ON A ONE WILL HOLD THE BREAK LOGIC CLEARED.  ADAL4 ON A ZERO
9850                                          ;WILL CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE
9851                                          ;WHEN THE SIGNAL XRAS H IS PULSED.  ADAL10 H ON A ONE WILL ENABLE THE
9852                                          ;EIDAL BUS TO THE ADDRESS BUS WHEN HDAL9 H IS SET TO A 0 LATER ON IN THE TEST.
9853
9854  025042  012737  022001  002330  4$:     MOV     #ADAL13!ADAL10!ADAL0,R2LOAD     ;SETUP BITS TO BE LOADED
9855  025050  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REG
9856  025054  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
9857  025056                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL 1
9858  025056  104455                          TRAP    C$ERDF
9859  025060  000002                          .WORD   2
9860  025062  002513                          .WORD   ADALRG
9861  025064  004770                          .WORD   R2EROR
9862  025066                                  CKLOOP
9863  025066  104406                          TRAP    C$CLP1
9864
9865                                          ;SET VDAL2 H TO A ONE AND THEN CLEAR VDAL2 H. VDAL2 H ON A ONE WILL
9866                                          ;CLEAR THE PAUSE STATE MACHINE FLIP-FLOPS
9867
9868  025070  005037  002334          5$:     CLR     R4LOAD                  ;SETUP TO CLEAR ALL BITS IN VDAL REG
9869  025074  004737  007712                  JSR     PC,CLRPSM               ;GO SET AND CLEAR VDAL2 H
9870
9871                                           SET VDAL7 H TO A ONE IN THE VDAL RFGISTER TO SET THE SIGNAL FETCT H
9872                                          ;TO THE HIGH STATE.
9873
9874  025100  052737  000200  002334          BIS     #VDAL7,R4LOAD           ;SETUP BIT TO BF LOADED
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```
 9875  025106  004737  006640          JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REGISTER
 9876  025112  001405                  BEQ     6$                      ;IF LOADED OK THEN CONTINUE
 9877  025114                          ERRDF   3,VDALRG,R4EROR         ;VDAL REG NOT EQUAL EXPECTED
 9878  025114  104455                  TRAP    C$ERDF
 9879  025116  000003                  .WORD   3
 9880  025120  002537                  .WORD   VDALRG
 9881  025122  005004                  .WORD   R4EROR
 9882  025124                          CKLOOP
 9883  025124  104406                  TRAP    C$CLP1
 9884
 9885                                  ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
 9886                                  ;TO ONES.  BITS IN THE HDAL REGISTER WILL BE SET AND CLEARED LATER IN
 9887                                  ;THIS TEST TO CAUSE PULSES ON THE SIGNALS XRAS H, XRAS L, XCAS H, XCAS L
 9888
 9889  025126  004737  006754  6$:     JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL 2:0
 9890
 9891                                  ;TOGGLE THE SIGNAL XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
 9892                                  ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS
 9893                                  ;HIGH, INTO THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE
 9894                                  ;HIGH STATE.  THE SIGNAL XRAS H WILL CLOCK THE STATE OF ADAL4 H, WHICH
 9895                                  ;IS LOW, INTO THE PAUSE MODE FLIP-FLOP, THUS SETTING THE SIGNAL PAUSE L
 9896                                  ;TO THE HIGH STATE.  THE SIGNAL SOP H WILL BE ASSERTED HIGH WHEN THE
 9897                                  ;SIGNAL PAUSE L IS ASSERTED HIGH.  WHEN SOP H AND EDFET H ARE ASSERTED
 9898                                  ;HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT SET TO A ONE.
 9899                                  ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNAL
 9900                                  ;PSMW H WILL BE ASSERTED HIGH.  THE SIGNAL PSMW H IS READ IN THE VDAL
 9901                                  ;REGISTER AS VDAL9 H.  WHEN EDFET H AND SOP H ARE ASSERTED HIGH, THE
 9902                                  ;SIGNAL PB H WILL BE ASSERTED HIGH.  THE SIGNAL PB H IS THE DATA INPUT
 9903                                  ;LEAD TO THE PAUSE STATE SYNC FLIP-FLOP.
 9904                                  ;
 9905                                  ;THE SIGNAL XRAS H WILL CAUSE THE SIGNAL RASP H TO BE PULSED.  WHEN THE
 9906                                  ;SIGNAL RASP H IS PULSED AND THE SIGNAL EDFET H IS ASSERTED HIGH, A
 9907                                  ;PULSE WILL BE ISSUED ON THE SIGNAL DFET H.  THE SIGNAL DFET H WILL
 9908                                  ;CLOCK THE ADDRESS BUS INTO THE OLD FORCE JUMP ADDRESS REGISTER.  AT THE
 9909                                  ;PRESENT TIME THE DIAGNOSTIC ADDRESS REGISTER IS ENABLED ONTO THE
 9910                                  ;ADDRESS BUS, THEREFORE THE OLD FORCE JUMP ADDRESS REGISTER WILL BE
 9911                                  ;LOADED WITH THE DATA FROM THE DIAGNOSTIC ADDRESS REGISTER.
 9912                                  ;
 9913                                  ;A PULSE ON XRAS H WITH FETCT H SET HIGH WILL CAUSE THE BTFET FLIP-FLOP
 9914                                  ;TO BE SET TO A ONE, THUS SETTING THE SIGNAL BTFET L TO THE LOW STATE.
 9915                                  ;WHEN BTFET L IS ASSERTED LOW AND THE SIGNAL INTER L IS ASSERTED HIGH,
 9916                                  ;THE SIGNAL BTS1 H WILL BE ASSERTED HIGH.  INTER L IS ASSERTED HIGH AS
 9917                                  ;A RESULT OF XSEL0 L AND XSEL1 L BEING ASSERTED HIGH.  BTS1 L WILL BE
 9918                                  ;READ IN THE VDAL REGISTER AS VDAL BIT 5 WHEN ADAL10 H IS SET TO A ONE
 9919                                  ;WHICH IT IS NOW.
 9920
 9921  025132  012737  001004  002342  MOV     #HDAL9!HDAL2,R6LOAD     ;BITS PREVIOUSLY SET IN HDAL REG
 9922  025140  004737  007272          JSR     PC,XRAS                 ;PULSE XRAS H AND XRAS L VIA HDAL12 H
 9923
 9924                                  ;CLEAR VDAL7 H IN THE VDAL REGISTER THUS SETTING THE SIGNAL FETCT H TO
 9925                                  ;THE LOW STATE.  CHECK THE PAUSE STATE MACHINE TO BE IN THE FOLLOWING
 9926                                  ;STATE AS A RESULT OF SOP H AND EDFET H BEING ASSERTED HIGH.
 9927                                  ;ALSO CHECK VDAL REGISTER BIT 5 TO BE SET TO A ONE AS A RESULT OF BTS1 H
 9928                                  ;BEING ASSERTED HIGH AND ADAL10 H BEING A ONE.
 9929                                  ;    PAUSE STATE WORKING - PSMW H - 1
 9930                                  ;    PAUSE STATE SYNC - EPSF H - 0
```

```
                                        ;    16 BIT ADDRESS - EPFN H - 0
                                        ;
025144  042737  000200  002334          BIC     #VDAL7,R4LOAD           ;SETUP TO CLEAR FETCT H
025152  013737  002334  002336          MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
025160  052737  001040  002336          BIS     #VDAL9!VDAL5,R4GOOD     ;EXPECT PSMW H AND BTS1 H TO BE SET
025166  004737  006646                  JSR     PC,LDRD4R               ;GO LOAD, READ AND CHECK VDAL REG
025172  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
025174                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
025174  104455                          TRAP    C$ERDF
025176  000003                          .WORD   3
025200  002537                          .WORD   VDALRG
025202  005004                          .WORD   R4EROR
025204                                  CKLOOP
025204  104406                          TRAP    C$CLP1
                                        ;TOGGLE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  THE
                                        ;SIGNAL XCAS H GOING FROM A ZERO TO A ONE WILL CLOCK THE LEVEL OF THE
                                        ;SIGNAL "PB H", WHICH IS HIGH, INTO THE PAUSE STATE SYNC FLIP-FLOP, THUS
                                        ;SETTING THE PAUSE STATE SYNC FLIP-FLOP TO A ONE.  THE SIGNAL XCAS H
                                        ;WILL ALSO CLOCK THE PREVIOUS STATE OF THE PAUSE STATE SYNC FLIP-FLOP (0)
                                        ;INTO THE 16 BIT ADDRESS FLIP-FLOP, THUS CLOCKING THE 16 BIT ADDRESS
                                        ;FLIP-FLOP TO A ZERO.
                                        ;
                                        ;WHEN A PULSE IS ISSUED ON XCAS H AND XRAS L IS ASSERTED HIGH, A PULSE
                                        ;WILL OCCUR ON THE SIGNAL ASPI L.  WHEN A PULSE IS ISSUED ON ASPI L,
                                        ;THE BTFET FLIP-FLOP WILL BE CLEARED, THUS SETTING THE SIGNAL BTFET L
                                        ;TO THE HIGH STATE.  WHEN BTFET L AND INTER L ARE ASSERTED HIGH, THE
                                        ;SIGNAL BTS1 H WILL BE ASSERTED LOW.
025206  004737  007376          7$:     JSR     PC,XCAS                 ;SET XCAS H TO THE HIGH STATE
                                        ;READ VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS TO BE
                                        ;IN THE FOLLOWING STATE AS A RESULT OF THE SIGNAL XCAS H BEING SET TO 1.
                                        ;ALSO CHECK VDAL5 H TO BE A ZERO AS A RESULT OF BTS1 H BEING ASSERTED
                                        ;LOW AND ADAL10 H BEING SET TO A ONE.
                                        ;    PAUSE STATE WORKING - PSMW H - 1
                                        ;    PAUSE STATE SYNC - EPSF H - 1
                                        ;    16 BIT ADDRESS - EPFN H - 0
025212  052737  002000  002336          BIS     #VDAL10,R4GOOD          ;SETUP TO EXPECT PAUSE STATE SYNC - EPSF
025220  042737  000040  002336          BIC     #VDAL5,R4GOOD           ;EXPECT BTS1 H TO BE A ZERO FROM ASPI L
025226  004737  006654                  JSR     PC,READR4               ;GO READ AND CHECK PAUSE STATE MACHINE
025232  001405                          BEQ     8$                      ;IF LOADED OK THEN CONTINUE
025234                                  ERRDF   3,VDALRG,R4EROR         ;EPSF H NOT SET/BTS1 H NOT LOW VIA ASPI L
025234  104455                          TRAP    C$ERDF
025236  000003                          .WORD   3
025240  002537                          .WORD   VDALRG
025242  005004                          .WORD   R4EROR
025 4                                   CKLOOP
025244  104406                          TRAP    C$CLP1
                                        ;TOGGLE THE SIGNAL XPI H BY SETTING AND CLEARING THE SIGNAL HDAL15 H.
                                        ;THIS IS DONE TO SIMULATE A MACHINE CYCLE.  WHEN THE SIGNAL XPI H IS
                                        ;PULSED, THE EDFET H FLIP-FLOP WILL BE SET TO A ZERO.
025246  004737  007502          8$:     JSR     PC,XPI                  ;GO PULSE XPI H VIA HDAL15 H
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 9987
 9988                                   ;TOGGLE THE SIGNALS XRAS H AND XRAS L BY SETTING AND CLEARING HDAL12 H.
 9989                                   ;WITH THE SIGNAL FETCT H SET LOW AND A PULSE BEING ISSUED ON XRAS H, THE
 9990                                   ;EDFET FLIP-FLOP WILL BE CLOCKED TO A ZERO, THUS ASSERTING THE SIGNAL
 9991                                   ;EDFET H TO THE LOW STATE.  WHEN EDFET H IS ASSERTED LOW, THE SIGNAL
 9992                                   ;PB H WILL BE ASSERTED LOW.  WHEN XRAS H IS PULSED, THE SIGNALS RASP H
 9993                                   ;AND RASP L WILL BE PULSED.
 9994                                   ;THE PAUSE STATE WORKING FLIP-FLOP WILL BE CLOCKED TO A ONE BY THE
 9995                                   ;SIGNAL RASP L WHEN EPFN L, EP8N L, AND PSMW H ARE ALL ASSERTED HIGH.
 9996
 9997  025252  004737  007272          JSR     PC,XRAS                 ;GO PULSE XRAS H BY HDAL12
 9998
 9999                                   ;READ THE VDAL REGISTER AND CHECK THE PAUSE STATE MACHINE FLIP-FLOPS
10000                                   ;TO BE IN THE FOLLOWING STATE AS A RESULT OF XRAS H BEING PULSED.
10001                                   ;    PAUSE STATE WORKING - PSMW H - 1
10002                                   ;    PAUSE STATE SYNC - EPSF H - 1
10003                                   ;    16 BIT ADDRESS - EPFN H - 0
10004
10005  025256  004737  006654          JSR     PC,READR4               ;CHECK VDAL AND PAUSE STATE MACHINE
10006  025262  001405                  BEQ     9$                      ;IF OK THEN CONTINUE
10007  025264                          ERRDF   3,VDALRG,R4EROR         ;PAUSE STATE WORKING F/F PROBABLY NOT SET
10008  025264  104455                  TRAP    C$ERDF
10009  025266  000003                  .WORD   3
10010  025270  002537                  .WORD   VDALRG
10011  025272  005004                  .WORD   R4EROR
10012  025274                          CKLOOP
10013  025274  104406                  TRAP    C$CLP1
10014
10015                                   ;SET THE SIGNAL XCAS H TO A ONE BY SETTING HDAL13 H TO A ONE.  THE
10016                                   ;SIGNAL XCAS H GOING FROM A 0 TO A 1 WILL CLOCK THE LEVEL OF THE
10017                                   ;SIGNAL  'PB H' , WHICH IS LOW, INTO THE PAUSE STATE SYNC FLIP-FLOP,
10018                                   ;THUS CLOCKING THE PAUSE STATE SYNC FLIP-FLOP TO A ZERO.  THE SIGNAL
10019                                   ;XCAS H WILL ALSO CLOCK THE PREVIOUS OUTPUT OF THE PAUSE STATE SYNC
10020                                   ;FLIP-FLOP (1) INTO THE 16 BIT ADDRESS FLIP FLOP, THUS CLOCKING THE
10021                                   ;16 BIT ADDRESS FLIP-FLOP TO A ONE.
10022
10023  025276  004737  007410  9$:      JSR     PC,XCASH                ;SET THE SIGNAL XCAS H TO HIGH STATE
10024
10025                                   ;READ THE VDAL REGISTER AND AND CHECK THE PAUSE STATE MACHINE FLIP-
10026                                   ;FLOPS TO BE IN THE FOLLOWING STATE AS A RESULT OF XCAS H BEING A 1.
10027                                   ;    PAUSE STATE WORKING - PSMW H - 1
10028                                   ;    PAUSE STATE SYNC - EPSF H - 0
10029                                   ;    16 BIT ADDRESS - EPFN H - 1
10030
10031  025302  042737  002000  002336  BIC     #VDAL10,R4GOOD          ;CLEAR BITS FOR EPSF H
10032  025310  052737  004000  002336  BIS     #VDAL11,R4GOOD          ;SET BIT FOR EPFN H
10033  025316  004737  006654          JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
10034  025322  001405                  BEQ     10$                     ;IF OK THEN CONTINUE
10035  025324                          ERRDF   3,VDALRG,R4EROR         ;EPFN H PROBABLY NOT SET IN VDAL REG
10036  025324  104455                  TRAP    C$ERDF
10037  025326  000003                  .WORD   3
10038  025330  002537                  .WORD   VDALRG
10039  025332  005004                  .WORD   R4EROR
10040  025334                          CKLOOP
10041  025334  104406                  TRAP    C$CLP1
10042
```

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10043                                   ;SELECT THE EODAL BUS BY SETTING GDAL BITS 2:0 TO ONES.  THE OLD FORCE
10044                                   ;JUMP ADDRESS REGISTER SHOULD BE ENABLED ON THE EODAL BUS AT THIS TIME.
10045                                   ;ON A READ COMMAND TO CONTROL REGISTER 6, THE EODAL BUS WILL BE READ
10046                                   ;BACK TO THE LSI-11 BUS VIA THE SIGNAL RPT7 L.
10047
10048  025336  004737  007122    10$:  JSR     PC,SEODAL                 ;SELECT EODAL BUS VIA GDAL BITS 2:0
10049
10050                                   ;ON THE FIRST PULSE OF XRAS H WHEN THE SIGNAL EDFET H WAS SET HIGH,
10051                                   ;THE FORCE JUMP ADDRESS REGISTER SHOULD HAVE BEEN LOADED WITH THE DATA
10052                                   ;IN THE DIAGNOSTIC ADDRESS REGISTER VIA THE CLOCKING SIGNAL DFET H
10053                                   ;(ADDRESS BUS TO FORCE JUMP ADDRESS REGISTER).  AT THIS POINT IN TIME,
10054                                   ;THE FORCE JUMP ADDRESS REGISTER WILL BE ENABLED TO THE EODAL BUS VIA
10055                                   ;THE SIGNALS OEARH L AND OEARL L.  THESE SIGNALS ARE ASSERTED LOW AS A
10056                                   ;RESULT  OF  THE  FLIP-FLOP  "GET NEW ADDRESS"  BEING CLEARED AND THE
10057                                   ;SIGNALS EARH H AND EARL H BEING ASSERTED HIGH.  THE "GET NEW ADDRESS"
10058                                   ;FLIP-FLOP WAS CLEARED AT THE BEGINNING OF THE TEST WHEN VDAL REGISTER
10059                                   ;BIT 2 WAS SET AND CLEARED.  THE SIGNAL EARH H AND EARL H ARE ASSERTED
10060                                   ;HIGH AS A RESULT OF THE 16 BIT ADDRESS FLIP-FLOP BEING SET TO A ONE,
10061                                   ;THE SIGNAL ACAS H BEING ASSERTED HIGH, AND MODE REGISTER BIT 11 SETUP
10062                                   ;FOR 16 BIT ADDRESS MODE.  THE FOLLOWING SECTION WILL READ THE EODAL
10063                                   ;BUS VIA THE SIGNAL RPT7 L AND CHECK THAT THE DIAGNOSTIC ADDRESS
10064                                   ;REGISTER WAS LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER AND THAT
10065                                   ;THE OLD FORCE JUMP ADDRESS REGISTER IS ENABLED TO THE EODAL BUS.
10066
10067  025342  011137  002342          MOV     (R1),R6LOAD               ;GET DATA LOADED INTO DIAG ADDRESS REG
10068  025346  004737  006700          JSR     PC,READR6                 ;READ FORCE JUMP ADDRESS ON EODAL BUS
10069  025352  001405                  BEQ     11$                       ;IF FORCE JUMP ADDRESS REG OK THEN CONT
10070  025354                          ERRDF   4,FEODAL,R06ERR           ;FORCE JUMP ADDRESS REG TO EODAL BUS ERR
10071  025354  104455                  TRAP    C$ERDF
10072  025356  000004                  .WORD   4
10073  025360  003147                  .WORD   FEODAL
10074  025362  005020                  .WORD   R06ERR
10075  025364                          CKLOOP
10076  025364  104406                  TRAP    C$CLP1
10077
10078                                   ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10079
10080  025366  004737  006754    11$:  JSR     PC,SLHDAL                 ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10081
10082                                   ;LEAVING THE SIGNAL XCAS H ASSERTED HIGH, ASSERT THE SIGNAL PPI H TO THE
10083                                   ;HIGH STATE BY SETTING HDAL15 H  TO A ONE.  SETTING THE SIGNAL PPI H TO
10084                                   ;THE HIGH STATE WILL CAUSE THE SIGNALS COHB L AND COLB L TO BE ASSERTED
10085                                   ;LOW.  SET HDAL9 H TO A ZERO.  WHEN HDAL9 H IS A ZERO AND ADAL10 H IS A
10086                                   ;ONE, WHICH IT IS, THE EIDAL BUS WILL BE ENABLED TO THE ADDRESS BUS AND
10087                                   ;THE DIAGNOSTIC ADDRESS REGISTER WILL BE DISABLED FROM THE ADDRESS BUS.
10088
10089  025372  012737  020004  002342  MOV     #HDAL13!HDAL2,R6LOAD      ;SETUP BITS PREVIOUSLY LOADED (XCAS H)
10090  025400  004737  007514          JSR     PC,XPIH                   ;SET XPI H AND PPI H TO HIGH STATE
10091
10092                                   ;SELECT THE EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10093
10094  025404  004737  007240          JSR     PC,SEIDAL                 ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10095
10096                                   ;AT THIS POINT IN TIME, THE EODAL BUS, WHICH CONTAINS THE OLD FORCE
10097                                   ;JUMP ADDRESS REGISTER DATA, WILL BE ENABLED TO THE EIDAL BUS VIA THE
10098                                   ;SIGNAL COHB L AND COLB L.  THE SIGNALS COHB L AND COLB L ARE ASSERTED
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10099                                   ;LOW AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP BEING SET; MODE
10100                                   ;REGISTER BIT 11 BEING A ZERO AND PPI H BEING ASSERTED HIGH.  THE
10101                                   ;PROGRAM WILL READ AND CHECK THE EIDAL BUS TO CONTAIN THE OLD FORCE
10102                                   ;JUMP ADDRESS REGISTER DATA.
10103
10104  025410  011137  002342           MOV     (R1),R6LOAD             ;GET OLD FJA REGISTER DATA
10105  025414  004737  006700           JSR     PC,READR6               ;READ EIDAL BUS FOR OLD FJA DATA
10106  025420  001405                   BEQ     12$                     ;IF DATA OK THEN CONTINUE
10107  025422                           ERRDF   4,FJAEID,R026ER         ;OLD FJA TO EIDAL BUS ERROR VIA EODAL
10108  025422  104455                   TRAP    C$ERDF
10109  025424  000004                   .WORD   4
10110  025426  003446                   .WORD   FJAEID
10111  025430  005034                   .WORD   R026ER
10112  025432                           CKLOOP
10113  025432  104406                   TRAP    C$CLP1
10114
10115                                   ;SELECT THE ADDRESS BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10116
10117  025434  004737  007072   12$:    JSR     PC,SLDADR               ;SELECT ADDRESS BUS VIA GDAL BITS 2:0
10118
10119                                   ;AT THIS POINT IN TIME THE EIDAL BUS SHOULD BE ENABLED TO THE ADDRESS
10120                                   ;BUS BY ADAL10 H BEING A ONE AND HDAL9 H BEING A ZERO.  THE EIDAL BUS
10121                                   ;PRESENTLY CONTAINS THE OLD FORCE JUMP ADDRESS REGISTER DATA.
10122
10123  025440  011137  002342           MOV     (R1),R6LOAD             ;GET DATA LOADED INTO OLD FJA REGISTER
10124  025444  004737  006700           JSR     PC,READR6               ;READ AND CHECK ADDRESS BUS FOR OLD FJA
10125  025450  001405                   BEQ     13$                     ;IF DATA OK THEN CONTINUE
10126  025452                           ERRDF   4,FJAADR,R026ER         ;FORCE JUMP ADDRESS TO ADDRESS BUS ERROR
10127  025452  104455                   TRAP    C$ERDF
10128  025454  000004                   .WORD   4
10129  025456  003501                   .WORD   FJAADR
10130  025460  005034                   .WORD   R026ER
10131  025462                           CKLOOP
10132  025462  104406                   TRAP    C$CLP1
10133
10134                                   ;THE OLD FORCE JUMP ADDRESS REGISTER IS PRESENTLY ENABLED TO THE EODAL
10135                                   ;BUS, THE CDAL BUS, THE EIDAL BUS AND THE ADDRESS BUS.  THE CDAL BUS IS
10136                                   ;ALSO ENABLED TO THE TDAL BUS VIA THE SIGNALS DTHB L AND DTLB L.  THE
10137                                   ;SIGNALS DTHB L AND DTLB L ARE ASSERTED LOW AS A RESULT OF PSEL0 L,
10138                                   ;PSEL1 L, PBCLR L AND CPI L BEING ASSERTED HIGH AND THE SIGNAL CCAS H
10139                                   ;BEING ASSERTED LOW.  TO CHECK THE DATA PATH TO THE TDAL BUS, THE TEST
10140                                   ;WILL CLOCK THE TDAL BUS INTO THE TDAL DIAGNOSTIC LATCH BY SETTING AND
10141                                   ;AND CLEARING VDAL2 H.  BY SETTING AND CLEARING VDAL2 H, THE PAUSE
10142                                   ;STATE MACHINE FLIP-FLOPS WILL BE CLEARED AND THE TDAL BUS WILL BE
10143                                   ;LATCHED INTO THE TDAL DIAGNOSTIC LATCH.
10144
10145  025464  005037  002334   13$:    CLR     R4LOAD                  ;SETUP TO EXPECT ALL BITS CLEARED
10146  025470  004737  007712           JSR     PC,CLRPSM               ;PULSE INVD L AND INVD H VIA VDAL2 H
10147                                                                   ;CLOCK TDAL BUS INTO TDAL DIAG LATCH
10148
10149                                   ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10150
10151  025474  004737  006754           JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10152
10153                                   ;SET THE SIGNALS XCAS H AND PCAS H TO THE LOW STATE BY CLEARING HDAL13 H
10154
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10155  025500  012737  120004  002342          MOV     #HDAL15!HDAL13!HDAL2,R6LOAD ;SETUP PREVIOUSLY LOADED BITS
10156  025506  004737  007442                  JSR     PC,XCASL                    ;SET XCAS H AND PCAS H TO LOW STATE
10157
10158                                          ;SET THE SIGNALS XPI H AND PPI H TO THE LOW STATE BY CLEARING HDAL15 H.
10159
10160  025512  004737  007546                  JSR     PC,XPIL
10161
10162                                          ;SET THE SIGNAL PBCLR H TO THE HIGH STATE BY SETTING HDAL7 H TO A ONE.
10163                                          ;WHEN THE SIGNAL PBCLR H IS ASSERTED HIGH AND ADAL12 H IS A ZERO, THE
10164                                          ;TDAL BUS WILL BE ENABLED TO THE CDAL BUS VIA THE SIGNALS DBHB L AND
10165                                          ;DBLB L.
10166
10167  025516  004737  007620                  JSR     PC,XBCLRH                   ;SET PBCLR H TO HIGH STATE VIA HDAL7 H
10168
10169                                          ;TO ENABLE THE TDAL DIAGNOSTIC LATCH ONTO THE TDAL BUS THE TEST WILL
10170                                          ;SET VDAL0 H TO A ONE.  THE TDAL DIAGNOSTIC LATCH WAS LOADED WITH THE
10171                                          ;OLD FORCE JUMP ADDRESS REGISTER DATA EARLIER IN THIS TEST WHEN THE
10172                                          ;SIGNAL VDAL2 H WAS SET AND CLEARED.
10173
10174  025522  052737  000001  002334          BIS     #VDAL0,R4LOAD               ;SETUP BIT TO ENABLE TDAL LATCH
10175  025530  004737  006640                  JSR     PC,LDRDR4                   ;GO LOAD, READ AND CHECK VDAL REGISTER
10176  025534  001405                          BEQ     14$                         ;IF LOADED OK THEN CONTINUE
10177  025536                                  ERRDF   3,VDALRG,R4EROR             ;VDAL OR PAUSE STATE MACHINE ERROR
10178  025536  104455                          TRAP    C$ERDF
10179  025540  000003                          .WORD   3
10180  025542  002537                          .WORD   VDALRG
10181  025544  005004                          .WORD   R4EROR
10182  025546                                  CKLOOP
10183  025546  104406                          TRAP    C$CLP1
10184
10185                                          ;SELECT THE EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10186
10187  025550  004737  007240          14$:    JSR     PC,SEIDAL                   ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10188
10189                                          ;AT THIS POINT IN TIME THE TDAL DIAGNOSTIC LATCH, WHICH WAS LOADED
10190                                          ;EARLIER IN THIS TEST VIA VDAL2 H, IS ENABLED TO THE TDAL BUS BY
10191                                          ;VDAL0 H BEING A ONE.  THE TDAL BUS IS ENABLED TO THE CDAL BUS VIA
10192                                          ;THE SIGNALS DBHB L AND DBLB L.  THESE SIGNALS ARE ASSERTED LOW AS A
10193                                          ;RESULT OF ADAL12 H BEING A ZERO AND THE SIGNAL PBCLR H BEING ASSERTED
10194                                          ;HIGH.  READ AND CHECK THE EIDAL BUS TO CONTAIN THE DATA WHICH WAS
10195                                          ;LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER EARLIER IN THIS TEST.
10196
10197  025554  011137  002342                  MOV     (R1),R6LOAD                 ;GET THE OLD FJA REGISTER DATA
10198  025560  004737  006700                  JSR     PC,READR6                   ;READ EIDAL BUS FOR OLD FJA DATA
10199  025564  001405                          BEQ     15$                         ;IF DATA OK THEN CONTINUE
10200  025566                                  ERRDF   4,FJATDL,R026ER             ;OLD FJA TO TDAL LATCH TO EIDAL BUS ERROR
10201  025566  104455                          TRAP    C$ERDF
10202  025570  000004                          .WORD   4
10203  025572  003536                          .WORD   FJATDL
10204  025574  005034                          .WORD   R026ER
10205  025576                                  CKLOOP
10206  025576  104406                          TRAP    C$CLP1
10207
10208                                          ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10209
10210  025600  004737  006754          15$:    JSR     PC,SLHDAL                   ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
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10211
10212                                   ;SET THE SIGNAL PBCLR H TO THE LOW STATE BY CLEARING HDAL7 H.
10213
10214  025604  012737  000204  002342   MOV     #HDAL7!HDAL2,R6LOAD     ;SETUP BITS PREVIOUSLY LOADED
10215  025612  004737  007652           JSR     PC,XBCLRL               ;SET PBCLR H TO THE LOW STATE VIA HDAL7
10216
10217                                   ;SET THE SIGNALS PSEL0 H, PSEL1 H, AND MSDI H TO THE HIGH STATE BY
10218                                   ;SETTING HDAL6, HDAL5, AND HDAL0 TO ONES IN THE HDAL REGISTER.  WHEN
10219                                   ;PSEL0 H AND PSEL1 H ARE ASSERTED HIGH, THE TDAL BUS WILL BE ENABLED TO
10220                                   ;THE CDAL BUS AGAIN VIA THE SIGNALS DBHB L AND DBLB L.  THE CDAL BUS
10221                                   ;WILL BE ENABLED TO THE EIDAL BUS UNCONDITIONALLY.  THE SIGNALS MSDI H
10222                                   ;AND MSDO H WILL BE ASSERTED HIGH AS A RESULT OF XSEL0 L BEING ASSERTED
10223                                   ;LOW AND HDAL0 H BEING ASSERTED HIGH.  THESE TWO SIGNALS WILL ENABLE THE
10224                                   ;EIDAL BUS TO THE DATA BUS AND T[illegible] THE EODAL BUS.
10225
10226  025616  052737  000141  002342   BIS     #HDAL6!HDAL5!HDAL0,R6LOAD ;SET PSEL0 H,PSEL1 H,MSDO H + MSDI H TO HIGH S
10227  025624  004737  006672           JSR     PC,LDRDR6               ;GO LOAD READ AND CHECK HDAL REGISTER
10228  025630  001405                   BEQ     16$                     ;IF LOADED OK THEN CONTINUE
10229  025632                           ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10230  025632  104455                   TRAP    C$ERDF
10231  025634  000004                   .WORD   4
10232  025636  002605                   .WORD   HDALRG
10233  025640  005020                   .WORD   R06ERR
10234  025642                           CKLOOP
10235  025642  104406                   TRAP    C$CLP1
10236
10237                                   ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL MSDI H IS ASSERTED
10238                                   ;HIGH WHEN HDAL0 H IS SET TO A ONE.  THE LOGIC LEVEL OF THE SIGNAL
10239                                   ;MSDI H IS READBACK INTO THE VDAL REGISTER AS VDAL REGISTER BIT 6.
10240
10241  025644  052737  000100  002336  16$:  BIS     #VDAL6,R4GOOD           ;SETUP TO EXPECT MSDI H AS A ONE
10242  025652  004737  006654           JSR     PC,READR4               ;READ AND CHECK VDAL AND PAUSE STATE
10243  025656  001405                   BEQ     17$                     ;IF MSDI H A ONE THEN CONTINUE
10244  025660                           ERRDF   3,VDALRG,R4EROR         ;VDAL REG ERROR - MSDI H PROBABLY A 0
10245  025660  104455                   TRAP    C$ERDF
10246  025662  000003                   .WORD   3
10247  025664  002537                   .WORD   VDALRG
10248  025666  005004                   .WORD   R4EROR
10249  025670                           CKLOOP
10250  025670  104406                   TRAP    C$CLP1
10251
10252                                   ;SELECT EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10253
10254  025672  004737  007240  17$:     JSR     PC,SEIDAL               ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10255
10256                                   ;AT THIS TIME, THE TDAL DIAGNOSTIC LATCH IS ENABLED TO THE TDAL BUS
10257                                   ;BY VDAL0 H BEING A ONE.  THE TDAL BUS IS ENABLED TO THE CDAL BUS VIA
10258                                   ;THE SIGNALS DBHB L AND DBLB L.  THESE SIGNALS ARE ASSERTED LOW AS A
10259                                   ;RESULT OF THE SIGNALS PSEL0 H AND PSEL1 H BEING ASSERTED HIGH.  THE
10260                                   ;CDAL BUS IS ENABLED TO THE EIDAL BUS UNCONDITIONALLY.  THE TDAL
10261                                   ;DIAGNOSTIC LATCH WAS LOADED EARLIER IN THIS TEST WITH THE OLD FORCE
10262                                   ;JUMP ADDRESS REGISTER DATA.
10263
10264  025676  011137  002342           MOV     (R1),R6LOAD             ;GET OLD FJA REGISTER DATA LOADED
10265  025702  004737  006700           JSR     PC,READR6               ;READ EIDAL BUS FOR OLD FJA REG DATA
10266  025706  001405                   BEQ     18$                     ;IF DATA OK THEN CONTINUE
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10267  025710                                  ERRDF   4,FJATDL,R026ER         ;OLD FJA TO TDAL LATCH TO EIDAL BUS ERROR
10268  025710  104455                          TRAP    C$ERDF
10269  025712  000004                          .WORD   4
10270  025714  003536                          .WORD   FJATDL
10271  025716  005034                          .WORD   R026ER
10272  025720                                  CKLOOP
10273  025720  104406                          TRAP    C$CLP1
10274
10275                                          ;SELECT THE EODAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10276
10277  025722  004737  007122          18$:    JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
10278
10279                                          ;AT THIS TIME, THE TDAL DIAGNOSTIC LATCH IS ENABLED TO THE TDAL BUS
10280                                          ;BY VDAL0 H BEING SET TO A ONE.  THE TDAL BUS IS ENABLED TO THE CDAL
10281                                          ;BUS VIA THE SIGNALS DBHB L AND DBLB L.  THE CDAL BUS IS ENABLED TO THE
10282                                          ;EIDAL BUS UNCONDITIONALLY.  THE EIDAL BUS IS ENABLED TO THE DATA BUS
10283                                          ;BY THE SIGNAL MSDO H.  THE SIGNAL MSDO H IS ASSERTED HIGH AS A RESULT
10284                                          ;OF XSEL0 L BEING ASSERTED LOW.  THE DATA BUS IS ENABLED TO THE EODAL
10285                                          ;BUS BY THE SIGNAL MSDI H BEING ASSERTED HIGH.  THIS SIGNAL IS ASSERTED
10286                                          ;HIGH AS A RESULT OF HDAL0 H BEING SET TO A ONE.  THE TDAL DIAGNOSTIC
10287                                          ;LATCH WAS LOADED EARLIER IN THIS TEST WITH THE OLD FORCE JUMP ADDRESS
10288                                          ;REGISTER DATA.
10289
10290  025726  011137  002342                  MOV     (R1),R6LOAD             ;GET OLD FJA REGISTER DATA LOADED
10291  025732  004737  006700                  JSR     PC,READR6               ;READ EODAL BUS FROM DATA + EIDAL BUSSES
10292  025736  001405                          BEQ     19$                     ;IF DATA OK THEN CONTINUE
10293  025740                                  ERRDF   4,TDLEOD,R026ER         ;EIDAL BUS TO DATA BUS TO EODAL BUS ERROR
10294  025740  104455                          TRAP    C$ERDF
10295  025742  000004                          .WORD   4
10296  025744  003607                          .WORD   TDLEOD
10297  025746  005034                          .WORD   R026ER
10298  025750                                  CKLOOP
10299  025750  104406                          TRAP    C$CLP1
10300
10301                                          ;SET ADAL13 H TO A ZERO.  ADAL13 H ON A ZERO WILL ENABLE THE SIGNAL
10302                                          ;DBLB L TO BE ASSERTED WHEN PSEL1 H IS A ONE.
10303
10304  025752  042737  020000  002330  19$:    BIC     #ADAL13,R2LOAD          ;SETUP BIT TO BE CLEARED
10305  025760  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REG
10306  025764  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
10307  025766                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
10308  025766  104455                          TRAP    C$ERDF
10309  025770  000002                          .WORD   2
10310  025772  002513                          .WORD   ADALRG
10311  025774  004770                          .WORD   R2EROR
10312  025776                                  CKLOOP
10313  025776  104406                          TRAP    C$CLP1
10314
10315                                          ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0.
10316
10317  026000  004737  006754          20$:    JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10318
10319                                          ;SET THE SIGNAL PSEL0 H TO THE LOW STATE AND SET THE SIGNAL PSEL1 H
10320                                          ;TO THE HIGH STATE BY SETTING HDAL5 TO ZERO AND HDAL6 TO ONE IN THE
10321                                          ;HDAL REGISTER.
10322
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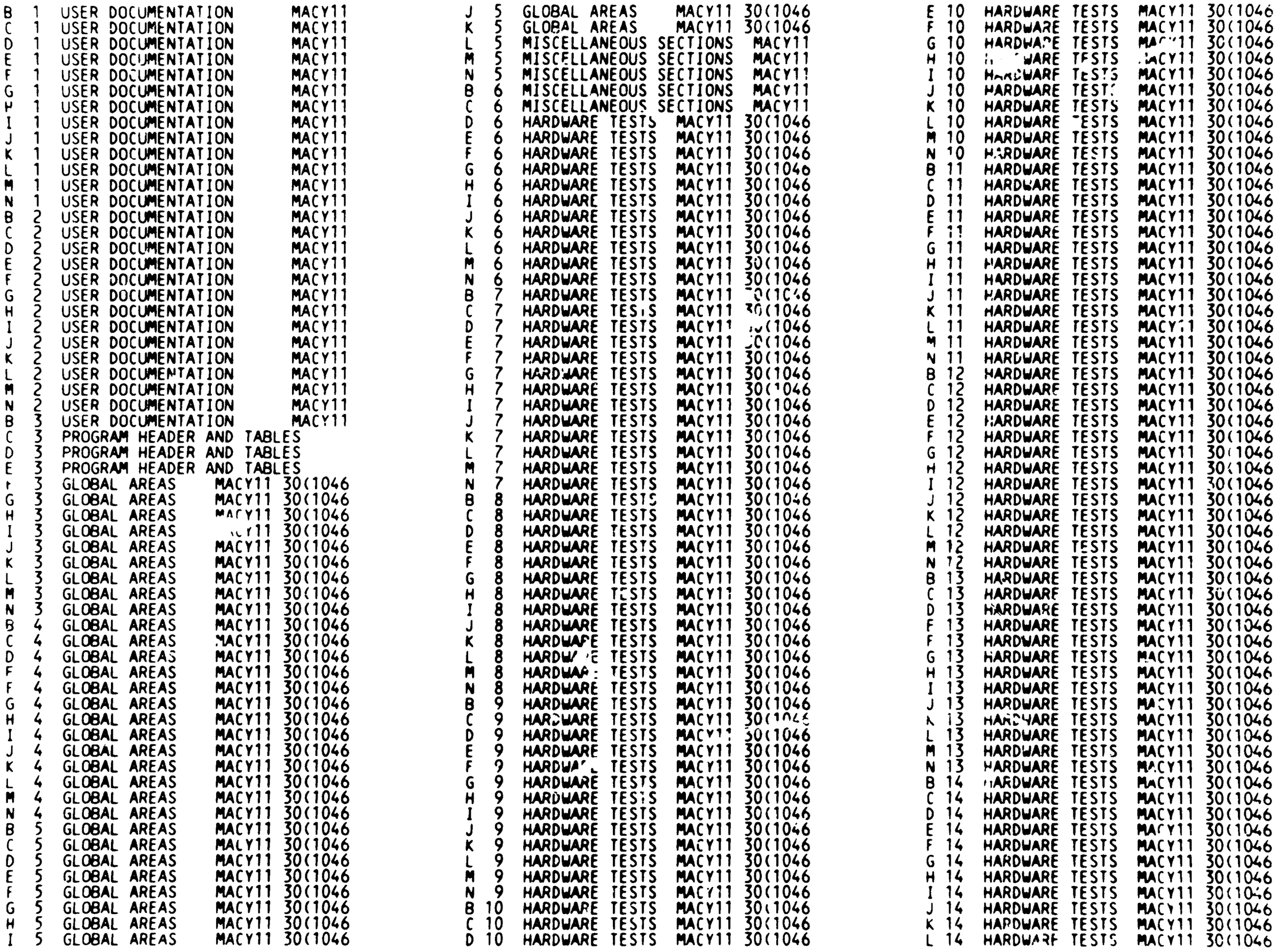
10323  026004  012737  000145  002342          MOV     #HDAL6!HDAL5!HDAL2!HDAL0,R6LOAD ;SETUP BITS PREVIOUSLY LOADED
10324  026012  042737  000040  002342          BIC     #HDAL5,R6LOAD           ;SET THE SIGNAL PSEL0 H TO LOW STATE
10325  026020  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10326  026024  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
10327  026026                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10328  026026  104455                          TRAP    C$ERDF
10329  026030  000004                          .WORD   4
10330  026032  002605                          .WORD   HDALRG
10331  026034  005020                          .WORD   R06ERR
10332  026036                                  CKLOOP
10333  026036  104406                          TRAP    C$CLP1
10334
10335                                          ;SELECT EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0.
10336
10337  026040  004737  007240          21$:    JSR     PC,SEIDAL               ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10338
10339                                          ;AT THIS TIME, THE TDAL DIAGNOSTIC LATCH IS ENABLED TO THE TDAL BUS
10340                                          ;BY VDALO H BEING A ONE.  THE LOW BYTE OF TDAL BUS IS ENABLED TO THE
10341                                          ;LOW BYTE OF THE CDAL BUS VIA THE SIGNAL DBLB L.  THIS SIGNAL IS
10342                                          ;ASSERTED LOW AS A RESULT OF THE SIGNALS PSEL1 H AND ADAL13 L BEING
10343                                          ;ASSERTED HIGH.  THE CDAL BUS IS ENABLED TO THE EIDAL BUS UNCONDITIONALLY.
10344                                          ;THE TIDAL DIAGNOSTIC LATCH WAS LOADED EARLIER IN THIS TEST WITH THE OLD
10345                                          ;FORCE JUMP ADDRESS REGISTER DATA.
10346
10347  026044  005037  002342                  CLR     R6LOAD                  ;CLEAR PREVIOUS BITS
10348  026050  111137  002342                  MOVB    (R1),R6LOAD             ;GET LOW BYTE OF OLD FJA REG DATA LOADED
10349  026054  012737  177400  002346          MOV     #177400,R6MASK          ;MASK OUT HIGH BYTE
10350  026062  004737  006700                  JSR     PC,READR6               ;READ EIDAL BUS FOR OLD FJA REG DATA
10351  026066  001404                          BEQ     22$                     ;IF DATA OK THEN CONTINUE
10352  026070                                  ERRDF   4,FJATDL,R026ER         ;OLD FJA TO TDAL LATCH TO EIDAL BUS ERROR
10353  026070  104455                          TRAP    C$ERDF
10354  026072  000004                          .WORD   4
10355  026074  003536                          .WORD   FJATDL
10356  026076  005034                          .WORD   R026ER
10357  026100                          22$:    ENDSEG
10358  026100                          10000$:
10359  026100  104405                          TRAP    C$ESEG
10360
10361  026102  005721                          TST     (R1)+                   ;UPDATE POINTER TO DIAG ADDRESS DATA TABLE
10362  026104  005302                          DEC     R2                      ;CHECK IF ALL PATTERNS HAVE BEEN LOADED
10363  026106  001410                          BEQ     24$                     ;IF YES THEN END OF TEST
10364  026110  000137  024722                  JMP     1$                      ;IF NOT THEN LOAD NEXT PATTERN
10365
10366  026114  125252                  23$:    .WORD   125252
10367  026116  052525                          .WORD   052525
10368  026120  177400                          .WORD   177400
10369  026122  000377                          .WORD   000377
10370  026124  177777                          .WORD   177777
10371  026126  000000                          .WORD   000000
10372
10373  026130                          24$:    ENDTST
10374  026130                          L10070:
10375  026130  104401                          TRAP    C$ETST
```



```
10376                                   .SBTTL  TEST 39: FDAL REGISTER TO EODAL BUS TO EIDAL BUS TEST
10377
10378                                   ;++
10379                                   ; THIS TEST WILL CHECK THAT THE FDAL REGISTER CAN BE ENABLED TO THE EODAL
10380                                   ; BUS VIA THE SIGNAL INTER L AND THAT THE EODAL BUS CAN BE ENABLED TO THE
10381                                   ; EIDAL BUS VIA THE SIGNAL COL8 L.  THE TEST WILL ALSO CHECK THAT THE EOAI
10382                                   ; REGISTER CAN BE CLEARED WHEN THE SIGNAL INTER L IS ASSERTED LOW.  A BINARY
10383                                   ; COUNT DATA PATTERN WILL BE LOADED INTO THE FDAL REGISTER STARTING WITH A
10384                                   ; DATA PATTERN OF ONE AND INCREMENTING BY FOUR UNTIL THE DATA PATTERN 375 HAS
10385                                   ; BEEN LOADED AND CHECKED.
10386                                   ;--
10387
10388  026132                                   BGNTST
10389  026132                           T39::
10390  026132  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
10391  026136  005001                           CLR     R1                      ;START BINARY COUNT PATTERN AT ZERO.
10392
10393  026140                           1$:     BGNSEG
10394  026140  104404                           TRAP    C$BSEG
10395
10396  026142  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL 16 BITS ON REG 6 READ
10397
10398                                           ;SET VDAL2 H TO A ONE AND THEN A ZERO TO CLEAR THE PAUSE STATE MACHINE
10399                                           ;FLIP-FLOP'S VIA THE SIGNALS INVD L AND INVD H.
10400
10401  026146  005037  002334                  CLR     R4LOAD                  ;SETUP TO 0 ALL OTHER BITS
10402  026152  004737  007712                  JSR     PC,CLRPSM               ;PULSE INVD L AND INVD H VIA VDAL2 H
10403
10404                                           ;SET ADAL13 H TO A ONE IN THE ADAL REGISTER. ADAL13 H ON A ONE WILL
10405                                           ;ENABLE THE LOW BYTE OF THE EODAL BUS TO THE CDAL BUS WHEN PSEL1 H IS
10406                                           ;ASSERTED HIGH LATER ON IN THIS TEST.
10407
10408  026156  012737  020000  002330           MOV     #ADAL13,R2LOAD          ;SETUP BIT TO BE SET TO A ONE
10409  026164  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
10410  026170  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
10411  026172                                   ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
10412  026172  104455                           TRAP    C$ERDF
10413  026174  000002                           .WORD   2
10414  026176  002513                           .WORD   ADALRG
10415  026200  004770                           .WORD   R2EROR
10416  026202                                   CKLOOP
10417  026202  104406                           TRAP    C$CLP1
10418
10419                                           ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10420
10421  026204  004737  006754           2$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
10422
10423                                           ;SET HDAL2 H TO A ONE AND ALL OTHER HDAL BITS TO A ZERO.  HDAL2 H ON
10424                                           ;A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL
10425                                           ;SIGNALS.
10426
10427  026210  012737  000004  002342           MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
10428  026216  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10429  026222  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10430  026224                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10431  026224  104455                           TRAP    C$ERDF
```

```
10432  026226  000004                          .WORD   4
10433  026230  002605                          .WORD   HDALRG
10434  026232  005020                          .WORD   R06ERR
10435  026234                                  CKLOOP
10436  026234  104406                          TRAP    C$CLP1
10437
10438                                          ;SELECT FDAL AND EOAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10439
10440  026236  004737  007154          3$.     JSR     PC,SLFDAL               ;SELECT FDAL AND EOAI REGISTER VIA GDAL
10441
10442                                          ;LOAD READ AND CHECK FDAL REGISTER BITS 7:0 WITH A BINARY COUNT PATTERN
10443                                          ;FROM 1 TO 377 BY AN INCREMENT OF FOUR.  THE EOAI REGISTER WILL BE
10444                                          ;LOADED AND CHECKED WITH A DATA PATTERN OF ALL ONES.
10445
10446  026242  010137  002342                  MOV     R1,R6LOAD               ;GET THE FDAL BINARY COUNT PATTERN
10447  026246  052737  177401  002342          BIS     #177401,R6LOAD          ;SET ALL EOAI REG BITS TO ONES + FDAL0 H
10448  026254  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK FDAL + EOAI REG'S
10449  026260  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
10450  026262                                  ERRDF   4,EOAIFD,R06ERR         ;EOAI OR FDAL REGISTER ERROR
10451  026262  104455                          TRAP    C$ERDF
10452  026264  000004                          .WORD   4
10453  026266  002616                          .WORD   EOAIFD
10454  026270  005020                          .WORD   R06ERR
10455  026272                                  CKLOOP
10456  026272  104406                          TRAP    C$CLP1
10457
10458                                          ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10459
10460  026274  004737  006754          4$:     JSR     PC,SLHDAL               ;SELECT THE HDAL REG VIA GDAL BITS 2:0
10461
10462                                          ;SET HDAL6 H TO A ONE TO ASSERT THE SIGNAL XSEL1 L TO THE LOW STATE.
10463                                          ;HDAL5 H ON A ZERO WILL CAUSE THE SIGNAL XSEL0 L TO BE ASSERTED HIGH.
10464                                          ;WHEN XSEL0 L IS ASSERTED HIGH AND XSEL1 L IS ASSERTED LOW, THE SIGNALS
10465                                          ;INTER H AND INTER L WILL BE ASSERTED HIGH AND LOW RESPECTIVELY.  WHEN
10466                                          ;INTER L IS ASSERTED LOW, THE EOAI REGISTER WILL BE CLEARED AND THE FDAL
10467                                          ;REGISTER WILL BE ENABLED TO THE LOW BYTE OF THE EODAL BUS.
10468
10469  026300  012737  000104  002342          MOV     #HDAL6!HDAL2,R6LOAD     ;SETUP BITS TO BE LOADED
10470  026306  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10471  026312  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
10472  026314                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10473  026314  104455                          TRAP    C$ERDF
10474  026316  000004                          .WORD   4
10475  026320  002605                          .WORD   HDALRG
10476  026322  005020                          .WORD   R06ERR
10477  026324                                  CKLOOP
10478  026324  104406                          TRAP    C$CLP1
10479
10480                                          ;SELECT THE EOAI AND FDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REG 0
10481
10482  026326  004737  007154          5$:     JSR     PC,SLFDAL               ;SELECT EOAI AND FDAL REG VIA GDAL 2:0
10483
10484                                          ;WHEN XSEL0 L IS ASSERTED HIGH AND XSEL1 L IS ASSERTED LOW, THE SIGNALS
10485                                          ;INTER H AND INTER L WILL BE ASSERTED HIGH AND LOW RESPECTIVELY. INTER L
10486                                          ;BEING ASSERTED LOW WILL CLEAR THE EOAI REGISTER WHICH WAS LOADED WITH
10487                                          ;ALL ONES PREVIOUSLY.
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10488
10489  026332  010137  002342                  MOV     R1,R6LOAD               ;GET THE FDAL REGISTER DATA
10490  026336  005237  002342                  INC     R6LOAD                  ;SETUP TO EXPECT FDALO H TO BE SET ALSO
10491  026342  004737  006700                  JSR     PC,READR6               ;CHECK IF EOAI REG WAS 0'ED VIA INTER L
10492  026346  001405                          BE.     6$                      ;IF DATA OK THEN CONTINUE
10493  026350                                   ERRDF   4,EOAIFD,R06ERR         ;INTER L FAILED TO ZERO EOAI REGISTER
10494  026350  104455                          TRAP    C$ERDF
10495  026352  000004                          .WORD   4
10496  026354  002676                          .WORD   EOAIFD
10497  026356  005020                          .WORD   R06ERR
10498  026360                                   CKLOOP
10499  026360  104406                          TRAP    C$CLP1
10500
10501                                           ;SELECT EODAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10502
10503  026362  004737  007122          6$:     JSR     PC,SEODAL               ;SELECT EODAL BUS VIA GDAL BITS 2:0
10504
10505                                           ;WHEN THE SIGNAL INTER L IS ASSERTED LOW, THE FDAL REGISTER WILL BE
10506                                           ;ENABLED TO THE LOW BYTE OF THE EODAL BUS.  THIS NEXT SECTION WILL
10507                                           ;CHECK THE EODAL BUS TO CONTAIN FDAL REGISTER DATA.
10508
10509  026366  010137  002342                  MOV     R1,R6LOAD               ;GET FDAL REGISTER DATA LOADED
10510  026372  012737  177400  002346          MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE ON READ
10511  026400  004737  006700                  JSR     PC,READR6               ;READ AND CHECK EODAL BUS FOR FDAL DATA
10512  026404  001405                          BEQ     7$                      ;IF DATA OK THEN CONTINUE
10513  026406                                   ERRDF   4,FDALEO,R06ERR         ;FDAL REG TO EODAL BUS ERROR
10514  026406  104455                          TRAP    C$ERDF
10515  026410  000004                          .WORD   4
10516  026412  003666                          .WORD   FDALEO
10517  026414  005020                          .WORD   R06ERR
10518  026416                                   CKLOOP
10519  026416  104406                          TRAP    C$CLP1
10520
10521                                           ;SELECT THE EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10522
10523  026420  004737  007240          7$:     JSR     PC,SEIDAL               ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10524
10525                                           ;AT THIS TIME, THE FDAL REGISTER IS ENABLED TO THE LOW BYTE OF THE
10526                                           ;EODAL BUS VIA THE SIGNAL INTER L.  THE LOW BYTE OF THE EODAL BUS IS
10527                                           ;ENABLED TO THE CDAL BUS AND TO THE EIDAL BUS VIA THE SIGNAL COLB L.
10528                                           ;THE SIGNAL COLB L IS ASSERTED LOW AS A RESULT OF ADAL13 H BEING A
10529                                           ;ONE, PSEL1 H BEING ASSERTED HIGH AND PSEL0 L BEING ASSERTED HIGH.
10530
10531  026424  010137  002342                  MOV     R1,R6LOAD               ;GET THE FDAL REGISTER DATA LOADED
10532  026430  012737  177400  002346          MOV     #177400,R6MASK          ;SETUP TO IGNORE THE HIGH BYTE
10533  026436  004737  006700                  JSR     PC,READR6               ;GO READ EIDAL BUS FOR FDAL REG DATA
10534  026442  001405                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
10535  026444                                   ERRDF   4,FDALEI,R026ER         ;FDAL REG TO EODAL TO EIDAL BUS ERROR
10536  026444  104455                          TRAP    C$ERDF
10537  026446  000004                          .WORD   4
10538  026450  003722                          .WORD   FDALEI
10539  026452  005034                          .WORD   R026ER
10540  026454                                   CKLOOP
10541  026454  104406                          TRAP    C$CLP1
10542
10543                                           :SET THE SIGNAL ADAL13 H TO A ZERO.  DOING THIS WILL CAUSE THE SIGNAL
```

```
10544                                           ;COLB L TO BE ASSERTED HIGH, THUS DISABLING THE EODAL BUS TO THE CDAL
10545                                           ;BUS AND TO THE EIDAL BUS.
10546
10547  026456  005037  002330          8$:     CLR     R2LOAD                  ;SETUP TO CLEAR ADAL13 H
10548  026462  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
10549  026466  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
10550  026470                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
10551  026470  104455                          TRAP    C$ERDF
10552  026472  000002                          .WORD   2
10553  026474  002513                          .WORD   ADALRG
10554  026476  004770                          .WORD   R2EROR
10555  026500                                  CKLOOP
10556  026500  104406                          TRAP    C$CLP1
10557
10558                                           ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10559
10560  026502  004737  006754          9$.     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10561
10562                                           ;AT THIS POINT IN TIME, THE SIGNALS ETR L AND DMG L ARE ASSERTED HIGH.
10563                                           ;TO ENABLE THE LOW BYTE OF THE EODAL BUS TO THE CDAL AND EIDAL BUS, THE
10564                                           ;PROGRAM MUST ASSERT THE SIGNAL COLB L TO THE LOW STATE.  TO DO THIS,
10565                                           ;THE PROGRAM MUST SET THE SIGNALS PPI H AND PR/WLB H TO THE HIGH STATE.
10566                                           ;THE PROGRAM WILL SET PPI H AND PR/WLB H TO THE HIGH STATE BY SETTING
10567                                           ;HDAL15 H AND HDAL3 H TO ONES RESPECTIVELY.
10568
10569  026506  012737  100114  002342           MOV     #HDAL15!HDAL6!HDAL3!HDAL2,R6LOAD ;BITS TO BE LOADED
10570  026514  005037  002346                  CLR     R6MASK                  ;SETUP TO CHECK ALL HDAL REG BITS
10571  026520  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10572  026524  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
10573  026526                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10574  026526  104455                          TRAP    C$ERDF
10575  026530  000004                          .WORD   4
10576  026532  002605                          .WORD   HDALRG
10577  026534  005020                          .WORD   R06ERR
10578  026536                                  CKLOOP
10579  026536  104406                          TRAP    C$CLP1
10580
10581                                           ;SELECT EIDAL BUS VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10582
10583  026540  004737  007240          10$:    JSR     PC,SEIDAL               ;SELECT EIDAL BUS VIA GDAL BITS 2:0
10584
10585                                           ;AT THIS POINT IN TIME, THE FDAL REGISTER IS ENABLED TO THE LOW BYTE
10586                                           ;OF THE EODAL BUS VIA THE SIGNAL INTER L.  THE LOW BYTE OF THE EODAL
10587                                           ;BUS IS ENABLED TO THE CDAL BUS AND EIDAL BUS VIA THE SIGNAL COLB L.
10588                                           ;THE SIGNAL COLB L IS ASSERTED LOW AS A RESULT OF THE SIGNALS ETR L,
10589                                           ;PR/WLB H, PPI H, AND DMG L BEING ASSERTED HIGH.
10590
10591  026544  010137  002342                  MOV     R1,R6LOAD               ;GET FDAL REGISTER DATA LOADED
10592  026550  012737  177400  002346           MOV     #177400,R6MASK          ;SETUP TO IGNORE THE HIGH BYTE
10593  026556  004737  006700                  JSR     PC,READR6               ;GO READ EIDAL BUS FOR FDAL REG DATA
10594  026562  001405                          BEQ     11$                     ;IF DATA OK TEHN CONTINUE
10595  026564                                  ERRDF   4,FDALEI,R026ER         ;FDAL TO EODAL TO EIDAL BUS ERROR
10596  026564  104455                          TRAP    C$ERDF
10597  026566  000004                          .WORD   4
10598  026570  003722                          .WORD   FDALEI
10599  026572  005034                          .WORD   R026ER
```

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10600  026574                                  CKLOOP
10601  026574  104406                          TRAP    C$CLP1
10602
10603                                          ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10604
10605  026576  004737  006754          11$:    JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10606
10607                                          ;RESET ALL HDAL REGISTER BITS TO ZERO EXCEPT HDAL REGISTER BIT 2.
10608
10609  026602  012737  000004  002342          MOV     #HDAL2,R6LOAD           ;SETUP TO CLEAR ALL BITS EXCEPT BIT 2
10610  026610  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10611  026614  001404                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
10612  026616                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10613  026616  104455                          TRAP    C$ERDF
10614  026620  000004                          .WORD   4
10615  026622  002605                          .WORD   HDALRG
10616  026624  005020                          .WORD   R06ERR
10617  026626                          12$     ENDSEG
10618  026626                          10000$:
10619  026626  104405                          TRAP    C$ESEG
10620
10621  026630  062701  000004                ADD     #FDAL2,R1               ;UPDATE BINARY COUNT PATTERN BY 4
10622  026634  105701                          TSTB    R1                      ;CHECK IF PATTERN DONE
10623  026636  001402                          BEQ     13$                     ;IF YES THEN EXIT THE TEST
10624  026640  000137  026140                JMP     1$                      ;IF NOT THEN LOAD NEXT PATTERN
10625
10626  026644                          13$:    ENDTST
10627  026644                          L10071:
10628  026644  104401                          TRAP    C$ETST
10629
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10630                                   .SBTTL  TEST 40: CHECK THE SIGNALS 'READ H' AND 'MSDI H'
10631
10632                                   ;++
10633                                   ; THIS TEST WILL CHECK THAT THE SIGNALS READ H AND MSDI H CA N BE ASSERTED HIGH
10634                                   ; AND LOW.  THESE SIGNALS ARE ASSERTED HIGH AND LOW BY CHANGING THE LOGIC LEVELS
10635                                   ; ON THE INPUT SIGNALS TO THE GATES WHICH GENERATE THE SIGNALS.  THE SIGNALS
10636                                   ; READ H AND MSDI H ARE READ IN THE VDAL REGISTER AS BITS 3 AND 6 RESPECTIVELY.
10637                                   ;--
10638
10639  026646                                   BGNTST
10640  026646                           T40::
10641  026646  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
10642  026652                                   BGNSEG
10643  026652  104404                          TRAP    C$BSEG
10644
10645                                           ;SELECT MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10646
10647  026654  004737  007006                 JSR     PC,SLMODR               ;SELECT MODE REG VIA GDAL BITS 2:0
10648
10649                                           ;CLEAR ALL BITS IN THE MODE REGISTER.  MODE REGISTER BIT 11 BEING A
10650                                           ;ZERO WILL CAUSE THE SIGNAL MR11 H AND MR11 L TO BE ASSERTED LOW AND
10651                                           ;HIGH RESPECTIVELY.
10652
10653  026660  005037  002342                   CLR     R6LOAD                  ;SETUP TO CLEAR ALL MODE REG BITS
10654  026664  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REG
10655  026670  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
10656  026672                                   ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
10657  026672  104455                          TRAP    C$ERDF
10658  026674  000004                          .WORD   4
10659  026676  002631                          .WORD   MODREG
10660  026700  005020                          .WORD   R06ERR
10661  026702                                   CKLOOP
10662  026702  104406                          TRAP    C$CLP1
10663
10664                                           ;SELECT THE FDAL AND EOAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REG 0
10665
10666  026704  004737  007154           1$:     JSR     PC,SLFDAL               ;SELECT FDAL VIA GDAL BITS 2:0
10667
10668                                           ;SET FDAL0 H TO A ONE AND ALL OTHER FDAL AND EOAI REGISTER BITS TO
10669                                           ;A ZERO.  FDAL0 H ON A ONE WILL ALLOW THE EOAI REGISTER TO BE READ
10670                                           ;ON A READ COMMAND TO CONTROL REGISTER 6 INSTEAD OF THE CTL REGISTER.
10671                                           ;FDAL1 H ON A ZERO WILL ALLOW THE DMG FLIP-FLOP TO DEASSERT THE SIGNAL
10672                                           ;PSL0 H WHEN THE SIGNAL DMG L IS ASSERTED LOW.
10673
10674  026710  012737  000001  002342           MOV     #FDAL0,P6LOAD           ;SETUP BIT TO BE LOADED
10675  026716  004737  006672                   JSR     PC,LDRDR6               ;LOAD, READ AND CHECK EOAI AND FDAL REG
10676  026722  001405                           BEQ     2$                      ;IF OK THEN CONTINUE
10677  026724                                   ERRDF   4,EOAIFD,R06ERR         ;EOAI OR FDAL REGISTER ERROR
10678  026724  104455                          TRAP    C$ERDF
10679  026726  000004                          .WORD   4
10680  026730  002676                          .WORD   EOAIFD
10681  026732  005020                          .WORD   R06ERR
10682  026734                                   CKLOOP
10683  026734  104406                          TRAP    C$CLP1
10684
10685                                           ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
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10686
10687  026736  004737  006754          2$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
10688
10689                                           ;SET HDAL REG BIT 2 ON A 1 AND ALL OTHER BITS TO A 0.  HDAL2 H ON A ONE
10690                                           ;WILL ALLOW THE PROGRAM TO GENERATE THE T-11 TIMING AND CONTROL SIGNALS.
10691
10692  026742  012737  000004  002342            MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
10693  026750  004737  006672                    JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10694  026754  001405                            BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10695  026756                                    ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10696  026756  104455                            TRAP    C$ERDF
10697  026760  000004                            .WORD   4
10698  026762  002605                            .WORD   HDALRG
10699  026764  005020                            .WORD   R06ERR
10700  026766                                    CKLOOP
10701  026766  104406                            TRAP    C$CLP1
10702
10703                                           ;SET ADAL REGISTER BITS 10 AND 0 TO ONES AND ALL OTHER ADAL BITS TO
10704                                           ;ZEROES.  THE SIGNAL PSLO H WILL BE ASSERTED HIGH WHEN ADAL10 H IS A
10705                                           ;ONE AND THE PAUSE STATE WORKING AND DMG FLIP-FLOPS ARE CLEARED.  THE
10706                                           ;SIGNAL PSLO H WILL ENABLE THE SIGNALS EDEOC H AND REAT H TO THE
10707                                           ;SYSTEM BUS AND TO THE VDAL REG. ADAL0 H ON A 1 WILL HOLD THE BREAK LOGIC CLEARE
10708
10709  026770  012737  002001  002330  3$:     MOV     #ADAL10!ADAL0,R2LOAD    ;SETUP BITS TO BE LOADED
10710  026776  004737  006614                    JSR     PC,LDRDR2               ;LOAD, READ AND CHECK ADAL REGISTER
10711  027002  001405                            BEQ     4$                      ;IF LOADED OK THEN CONTINUE
10712  027004                                    ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
10713  027004  104455                            TRAP    C$ERDF
10714  027006  000002                            .WORD   2
10715  027010  002513                            .WORD   ADALRG
10716  027012  004770                            .WORD   R2EROR
10717  027014                                    CKLOOP
10718  027014  104406                            TRAP    C$CLP1
10719
10720                                           ;SET VDAL2 H TO A ONE AND THEN ZERO.  THIS IS DONE TO INITIALIZE THE
10721                                           ;PAUSE STATE MACHINE FLIP-FLOPS AND ALL OTHER FLIP-FLOPS TO A KNOWN
10722                                           ;STATE.  SETTING AND CLEARING VDAL2 H WILL CAUSE THE SIGNALS INVD L
10723                                           ;AND INVD H TO BE PULSED.
10724
10725  027016  005037  002334          4$:     CLR     R4LOAD                  ;SETUP TO CLEAR ALL OTHER R/W BITS
10726  027022  004737  007712                    JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
10727
10728                                           ;THE NEXT SECTION WILL SET THE HDAL REGISTER BITS TO THE STATE INDICATED
10729                                           ;     HDAL3 H  - 1   ASSERTS XR/WLB H TO THE HIGH STATE
10730                                           ;     HDAL4 H  - 1   ASSERTS XR/WHB H TO THE HIGH STATE
10731                                           ;     HDAL12 H - 1   ASSERTS XRAS H TO THE HIGH STATE
10732                                           ;     HDAL13 H - 1   ASSERTS XCAS H TO THE HIGH STATE
10733                                           ;WHEN THE ABOVE SIGNALS ARE SET TO A ONE AND MODE REGISTER BIT 11 IS
10734                                           ;CLEARED, THE SIGNAL REAT H WILL BE ASSERTED HIGH.  THE SIGNAL REAT H
10735                                           ;WILL BE ENABLED TO THE VDAL REGISTER WHEN THE SIGNAL PSLO H IS ASSERTED
10736                                           ;HIGH.  THE SIGNAL PSLO H IS ASSERTED HIGH AS A RESULT OF THE DMG FLIP-
10737                                           ;FLOP BEING CLEARED, ADAL10 H ON A ONE, AND THE PAUSE STATE WORKING FLIP-
10738                                           ;FLOP BEING CLEARED.  THE SIGNAL REAT H WILL BE READ IN VDAL REGISTER
10739                                           ;BIT 3 AS THE SIGNAL READ H.  VDAL REGISTER BIT 6, WHICH INDICATES
10740                                           ;THE LOGIC LEVEL OF THE SIGNAL MSDI H, WILL ALSO BE SET TO A ONE.  MSDI H
10741                                           ;IS ASSERTED HIGH AS A RESULT OF SIGNALS XSEL0 !, ADAL10 H, PSMW L,
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10742                                           ;REAT H, AND ETR L ALL BEING ASSERTED HIGH.
10743
10744  027026  012737  030034  002342           MOV     #HDAL13!HDAL12.HDAL4.HDAL3!HDAL2,R6LOAD ;BITS TO BE LOADED
10745  027034  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10746  027040  001405                           BEQ     5$                      ;IF LOADED OK THEN CONTINUE
10747  027042                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10748  027042  104455                           TRAP    C$ERDF
10749  027044  000004                           .WORD   4
10750  027046  002605                           .WORD   HDALRG
10751  027050  005020                           .WORD   R06ERR
10752  027052                                   CKLOOP
10753  027052  104406                           TRAP    C$CLP1
10754
10755                                           ;CHECK VDAL BITS 6 + 3 TO BE A 1 AS A RESULT OF MSDI H + READ H BEING SET HIGH.
10756
10757  027054  052737  000110  002336  5$:      BIS     #VDAL6!VDAL3,R4GOOD     ;EXPECT READ H AND MSDI H TO BE ONES
10758  027062  004737  006654                   JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
10759  027066  001405                           BEQ     6$                      ;IF OK THEN CONTINUE
10760  027070                                   ERRDF   3,VDALRG,R4EROR         ;MSDI H AND/OR READ H PROBABLY NOT SET
10761  027070  104455                           TRAP    C$ERDF
10762  027072  000003                           .WORD   3
10763  027074  002537                           .WORD   VDALRG
10764  027076  005004                           .WORD   R4EROR
10765  027100                                   CKLOOP
10766  027100  104406                           TRAP    C$CLP1
10767
10768                                           ;SET ADAL REGISTER BIT 10 TO A ZERO.  WHEN ADAL10 H IS A ZERO, THE
10769                                           ;SIGNAL REAT H WILL BE DISABLED FROM THE VDAL REGISTER AS A RESULT OF
10770                                           ;THE SIGNAL PSLO H BEING ASSERTED LOW.  THE SIGNAL MSDI H WILL BE
10771                                           ;ASSERTED LOW WHEN ADAL10 H IS SET TO A ZERO.
10772
10773  027102  042737  002000  002330  6$:      BIC     #ADAL10,R2LOAD          ;SETUP TO CLEAR ADAL10 H
10774  027110  004737  006614                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADLA REGISTER
10775  027114  001405                           BEQ     7$                      ;IF LOADED OK THEN CONTINUE
10776  027116                                   ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
10777  027116  104455                           TRAP    C$ERDF
10778  027120  000002                           .WORD   2
10779  027122  002513                           .WORD   ADALRG
10780  027124  004770                           .WORD   R2EROR
10781  027126                                   CKLOOP
10782  027126  104406                           TRAP    C$CLP1
10783
10784                                           ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL PSLO H AND MSDI H
10785                                           ;ARE ASSERTED LOW.  WHEN PSLO H IS ASSERTED LOW, THE SIGNAL REAT H,
10786                                           ;WHICH IS PRESENTLY HIGH, WILL BE DISABLED FROM THE VDAL REGISTER.
10787
10788  027130  005037  002336          7$:      CLR     R4GOOD                  ;SETUP TO EXPECT READ H AND MSDI H A 0
10789  027134  004737  006654                   JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
10790  027140  001405                           BEQ     8$                      ;IF OK THEN CONTINUE
10791  027142                                   ERRDF   3,VDALRG,R4EROR         ;MSDI H AND/OR READ H PROBABLY NOT 0
10792  027142  104455                           TRAP    C$ERDF
10793  027144  000003                           .WORD   3
10794  027146  002537                           .WORD   VDALRG
10795  027150  005004                           .WORD   R4EROR
10796  027152                                   CKLOOP
10797  027152  104406                           TRAP    C$CLP1
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10798
10799                                           ;SET ADAL10 H TO A 1 TO CAUSE THE SIGNALS PSLO H,READ H, + MSDI H TO BE SET HIGH
10800
10801  027154  052737  002000  002330  8$:     BIS     #ADAL10,R2LOAD          ;SET BIT TO SET ADAL10 H TO A ONE
10802  027162  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
10803  027166  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
10804  027170                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
10805  027170  104455                          TRAP    C$ERDF
10806  027172  000002                          .WORD   2
10807  027174  002513                          .WORD   ADALRG
10808  027176  004770                          .WORD   R2EROR
10809  027200                                  CKLOOP
10810  027200  104406                          TRAP    C$CLP1
10811
10812                                           ;RECHECK THE VDAL REGISTER TO CHECK THAT THE SIGNALS MSDI H AND READ H
10813                                           ;ARE ASSERTED HIGH AGAIN
10814
10815  027202  052737  000110  002336  9$:     BIS     #VDAL6!VDAL3,R4GOOD     ;EXPECT READ H AND MSDI H TO BE ONES
10816  027210  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
10817  027214  001405                          BEQ     10$                     ;IF OK THEN CONTINUE
10818  027216                                  ERRDF   3,VDALRG,R4EROR         ;MSDI H AND/OR READ H PROBABLY NOT SET
10819  027216  104455                          TRAP    C$ERDF
10820  027220  000003                          .WORD   3
10821  027222  002537                          .WORD   VDALRG
10822  027224  005004                          .WORD   R4EROR
10823  027226                                  CKLOOP
10824  027226  104406                          TRAP    C$CLP1
10825
10826                                           ;SET THE SIGNAL XR/WLB H TO THE LOW STATE BY CLEARING HDAL3 H IN THE
10827                                           ;HDAL REGISTER.  WHEN XR/WLB H IS ASSERTED LOW AND THE SIGNALS XR/WHB H,
10828                                           ;MR11 L, XRAS H, AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H WILL
10829                                           ;BE ASSERTED LOW.  WHEN REAT H IS ASSERTED LOW, THE SIGNALS READ H
10830                                           ;AND MSDI H WILL BE ASSERTED LOW AND READ AS ZEROES IN THE VDAL REGISTER
10831
10832  027230  042737  000010  002342  10$:     BIC     #HDAL3,R6LOAD           ;SETUP TO SET XR/WLB H TO LOW STATE
10833  027236  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
10834  027242  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10835  027244                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10836  027244  104455                          TRAP    C$ERDF
10837  027246  000004                          .WORD   4
10838  027250  002605                          .WORD   HDALRG
10839  027252  005020                          .WORD   R06ERR
10840  027254                                  CKLOOP
10841  027254  104406                          TRAP    C$CLP1
10842
10843                                           ;READ THE VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED
10844                                           ;LOW AS A RESULT OF XR/WLB H BEING ASSERTED LOW.
10845
10846  027256  005037  002336          11$:     CLR     R4GOOD                  ;EXPECT MSDI H AND READ H TO BE 0'S
10847  027262  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
10848  027266  001405                          BEQ     12$                     ;IF OK THEN CONTINUE
10849  027270                                  ERRDF   3,VDALRG,R4EROR         ;WR/WLB H PROBABLY NOT ASSERTED LOW
10850  027270  104455                          TRAP    C$ERDF
10851  027272  000003                          .WORD   3
10852  027274  002537                          .WORD   VDALRG
10853  027276  005004                          .WORD   R4EROR
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10854  027300                                  CKLOOP
10855  027300  104406                          TRAP    C$CLP1
10856
10857                                          ;SET THE SIGNAL XR/WLB H BACK TO THE HIGH STATE BY SETTING HDAL3 H TO
10858                                          ;A ONE AND SET THE SIGNAL XR/WHB H TO THE LOW STATE BY CLEARING HDAL4 H.
10859                                          ;WHEN XR/WHB H IS ASSERTED LOW AND THE SIGNALS XR/WLB H, MR11 L, XRAS H
10860                                          ;AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H WILL BE ASSERTED LOW.
10861                                          ;WHEN REAT H IS ASSERTED LOW, THE SIGNALS READ H AND MSDI H WILL BE
10862                                          ;ASSERTED LOW AND READ AS ZEROES IN THE VDAL REGISTER.
10863
10864  027302  042737  000020  002342  12$:   BIC     #HDAL4,R6LOAD           ;SETUP TO SET XR/WHB H TO LOW STATE
10865  027310  052737  000010  002342        BIS     #HDAL3,R6LOAD           ;SETUP BIT TO SET XR/WLB H TO HIGH STATE
10866  027316  004737  006672                JSR     PC,LDRDR6               ;LOAD, READ AND CHECK THE HDAL REGISTER
10867  027322  001405                        BEQ     13$                     ;IF LOADED OK THEN CONTINUE
10868  027324                                ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
10869  027324  104455                        TRAP    C$ERDF
10870  027326  000004                        .WORD   4
10871  027330  002605                        .WORD   HDALRG
10872  027332  005020                        .WORD   R06ERR
10873  027334                                CKLOOP
10874  027334  104406                        TRAP    C$CLP1
10875
10876                                          ;READ THE VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED
10877                                          ;LOW AS A RESULT OF XR/WHB H BEING ASSERTED LOW.
10878
10879  027336  004737  006654          13$:   JSR     PC,READR4               ;GO READ VDAL AND PAUSE STATE MACHINE
10880  027342  001405                        BEQ     14$                     ;IF OK THEN CONTINUE
10881  027344                                ERRDF   3,VDALRG,R4EROR         ;XR/WHB H PROBABLY NOT ASSERTED LOW
10882  027344  104455                        TRAP    C$ERDF
10883  027346  000003                        .WORD   3
10884  027350  002537                        .WORD   VDALRG
10885  027352  005004                        .WORD   R4EROR
10886  027354                                CKLOOP
10887  027354  104406                        TRAP    C$CLP1
10888
10889                                          ;SET THE SIGNAL XR/WHB H BACK TO THE HIGH STATE BY SETTING HDAL4 H TO
10890                                          ;A ONE, AND SET THE SIGNAL XRAS H TO THE LOW STATE BY CLEARING HDAL12 H.
10891                                          ;WHEN XRAS H IS ASSERTED LOW, AND THE SIGNALS XR/WLB H, XR/WHB H, MR11 L,
10892                                          ;AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H WILL BE ASSERTED LOW.
10893                                          ;WHEN REAT H IS ASSERTED LOW, THE SIGNALS READ H AND MSDI H WILL BE
10894                                          ;ASSERTED LOW AND READ AS ZEROES IN THE VDLA REGISTER.
10895
10896  027356  052737  000020  002342  14$:   BIS     #HDAL4,R6LOAD           ;SET XR/WHB H TO HIGH STATE
10897  027364  004737  007336                JSR     PC,XRASL                ;SET XRAS H TO LOW STATE VIA HDAL12 H
10898
10899                                          ;READ VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED LOW
10900                                          ;AS A RESULT OF XRAS H BEING ASSERTED LOW.
10901
10902  027370  004737  006654                JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
10903  027374  001405                        BEQ     15$                     ;IF OK THEN CONTINUE
10904  027376                                ERRDF   3,VDALRG,R4EROR         ;THE "AND" OF XRAS H AND XCAS H NOT LOW
10905  027376  104455                        TRAP    C$ERDF
10906  027400  000003                        .WORD   3
10907  027402  002537                        .WORD   VDALRG
10908  027404  005004                        .WORD   R4EROR
10909  027406                                CKLOOP
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10910  027406  104406                          TRAP    C$CLP1
10911
10912                                          ;SET THE SIGNAL XRAS H BACK TO THE HIGH STATE BY SETTING HDAL12 H TO
10913                                          ;A ONE AND SET THE SIGNAL XCAS H TO THE LOW STATE BY CLEARING HDAL13 H.
10914                                          ;WHEN XCAS H IS ASSERTED LOW AND THE SIGNALS XR/WLB H, XR/WHB H, MR11 L,
10915                                          ;AND XRAS H ARE ASSERTED HIGH, THE SIGNAL REAT H WILL BE ASSERTED LOW.
10916                                          ;WHEN REAT H IS ASSERTED LOW, THE SIGNALS READ H AND MSDI H WILL BE
10917                                          ;ASSERTED LOW AND READ AS ZEROES IN THE VDAL REGISTER.
10918
10919  027410  052737  010000  002342  15$:    BIS     #HDAL12,R6LOAD          ;SET BIT TO SET XRAS H TO HIGH STATE
10920  027416  004737  007442                  JSR     PC,XCASL                ;SET XCAS H TO LOW STATE VIA HDAL13 H
10921
10922                                          ;READ VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED LOW
10923                                          ;AS A RESULT OF XCAS L BEING ASSERTED LOW.
10924
10925  027422  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
10926  027426  001405                          BEQ     16$                     ;IF OK THEN CONTINUE
10927  027430                                  ERRDF   3,VDALRG,R4EROR         ;THE "AND" OF XRAS H AND XCAS H NOT LOW
10928  027430  104455                          TRAP    C$ERDF
10929  027432  000003                          .WORD   3
10930  027434  002537                          .WORD   VDALRG
10931  027436  005004                          .WORD   R4EROR
10932  027440                                  CKLOOP
10933  027440  104406                          TRAP    C$CLP1
10934
10935                                          ;SET THE SIGNAL XCAS H BACK TO THE HIGH STATE BY SETTING HDAL13 H TO
10936                                          ;A ONE.  WHEN XCAS H IS SET HIGH, THE SIGNAL REAT H WILL BE ASSERTED
10937                                          ;HIGH AS A RESULT OF XR/WLB H, WR/WHB H, MR11 L, XRAS H AND XCAS H
10938                                          ;BEING ASSERTED HIGH.  WHEN REAT H IS ASSERTED HIGH, THE SIGNALS READ H
10939                                          ;AND MSDI H WILL BE ASSERTED HIGH AND READ AS ONES IN THE VDAL REGISTER.
10940
10941  027442  004737  007410          16$:    JSR     PC,XCASH                ;SET XCAS H TO HIGH STATE VIA HDAL13 H
10942
10943                                          ;READ VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED HIGH
10944                                          ;AS A RESULT OF REAT H BEING ASSERTED HIGH.
10945
10946  027446  052737  000110  002336          BIS     #VDAL6!VDAL3,R4GOOD     ;EXPECT READ H AND MSDI H TO BE ONES
10947  027454  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
10948  027460  001405                          BEQ     17$                     ;IF OK THEN CONTINEU
10949  027462                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
10950  027462  104455                          TRAP    C$ERDF
10951  027464  000003                          .WORD   3
10952  027466  002537                          .WORD   VDALRG
10953  027470  005004                          .WORD   R4EROR
10954  027472                                  CKLOOP
10955  027472  104406                          TRAP    C$CLP1
10956
10957                                          ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10958
10959  027474  004737  007006          17$:    JSR     PC,SLMODR               ;SELECT MODE REGISTE VIA GDAL BITS 2:0
10960
10961                                          ;SET MODE REGISTER BIT 11 TO A ONE TO SET THE SIGNAL MR11 H TO THE
10962                                          ;HIGH STATE AND THE SIGNAL MR11 L TO THE LOW STATE.
10963
10964  027500  012737  004000  002342          MOV     #MR11,R6LOAD            ;SETUP BIT TO BE LOADED
10965  027506  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK MODE REGISTER
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10966  027512  001405                          BEQ     18$                     ;IF LOADED OK THEN CONTINUE
10967  027514                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
10968  027514  104455                          TRAP    C$ERDF
10969  027516  000004                          .WORD   4
10970  027520  002631                          .WORD   MODREG
10971  027522  005020                          .WORD   R06ERR
10972  027524                                  CKLOOP
10973  027524  104406                          TRAP    C$CLP1
10974
10975                                          ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
10976
10977  027526  004737  006754          18$:    JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
10978  027532  012737  030034  002342          MOV     #HDAL13!HDAL12!HDAL4!HDAL3!HDAL2,R6LOAD ;BITS PREVIOUSLY LOADED
10979
10980                                          ;READ THE VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED LOW,
10981                                          ;WHEN MR11 L IS ASSERTED LOW AND THE SIGNALS XR/WLB H, XR/WHB H, XRAS H
10982                                          ;AND XCAS H ARE ASSERTED HIGH.
10983
10984  027540  005037  002336                  CLR     R4GOOD                  ;EXPECT READ H AND MSDI H TO BE 0
10985  027544  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
10986  027550  001405                          BEQ     19$                     ;IF OK THEN CONTINUE
10987  027552                                  ERRDF   3,VDALRG,R4EROR         ;READ H AND/OR MSDI H ARE SET HIGH
10988  027552  104455                          TRAP    C$ERDF
10989  027554  000003                          .WORD   3
10990  027556  002537                          .WORD   VDALRG
10991  027560  005004                          .WORD   R4EROR
10992  027562                                  CKLOOP
10993  027562  104406                          TRAP    C$CLP1
10994
10995                                          ;SET THE SIGNAL XR/WHB L TO THE HIGH STATE BY CLEARING HDAL4 H.  WHEN
10996                                          ;XR/WHB L, MR11 H, XRAS H AND XCAS H ARE ASSERTED HIGH, THE SIGNAL REAT H
10997                                          ;WILL BE ASSERTED HIGH.  WHEN REAT H IS ASSERTED HIGH, THE SIGNALS
10998                                          ;READ H + MSDI H WILL BE ASSERTED HIGH AND READ AS ONES IN THE VDAL REG.
10999
11000  027564  042737  000020  002342  19$:    BIC     #HDAL4,R6LOAD           ;SET XR/WHB L TO THE HIGH STATE
11001  027572  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK HDAL REGISTER
11002  027576  001405                          BEQ     20$                     ;IF OK THEN CONTINUE
11003  027600                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
11004  027600  104455                          TRAP    C$ERDF
11005  027602  000004                          .WORD   4
11006  027604  002605                          .WORD   HDALRG
11007  027606  005020                          .WORD   R06ERR
11008  027610                                  CKLOOP
11009  027610  104406                          TRAP    C$CLP1
11010
11011                                          ;READ THE VDAL REGISTER AND CHECK THAT READ H AND MSDI H ARE SET TO ONES
11012                                          ;AS A RESULT OF MR11 H, XR/WHB L, XRAS H AND XCAS H BEING ASSERTED HIGH.
11013
11014  027612  052737  000110  002336  20$:    BIS     #VDAL6!VDAL3,R4GOOD     ;EXPECT READ H AND MSDI H TO BE ONES
11015  027620  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE F/F'S
11016  027624  001405                          BEQ     21$                     ;IF OK THEN CONTINUE
11017  027626                                  ERRDF   3,VDALRG,R4EROR         ;REAT H PROBABLY NOT ASSERTED HIGH
11018  027626  104455                          TRAP    C$ERDF
11019  027630  000003                          .WORD   3
11020  027632  002537                          .WORD   VDALRG
11021  027634  005004                          .WORD   R4EROR
```

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11022  027636                          CKLOOP
11023  027636  104406                  TRAP    C$CLP1
11024
11025                                  ;SET THE SIGNAL XRAS H TO THE LOW STATE TO CHECK THAT THE "AND"
11026                                  ;CONDITION OF XRAS H AND XCAS H WILL CAUSE THE SIGNAL REAT H TO BE
11027                                  ;ASSERTED LOW.
11028
11029  027640  004737  007336  21$:    JSR     PC,XRASL                ;SET XRAS H TO LOW STATE
11030
11031                                  ;READ THE VDAL REGISTER TO CHECK THAT XRAS H BEING SET LOW CAUSED THE
11032                                  ;SIGNALS READ H AND MSDI H TO BE ASSERTED LOW AS A RESULT OF REAT H BEING
11033                                  ;SET TO THE LOW STATE.
11034
11035  027644  005037  002336          CLR     R4GOOD                  ;EXPECT READ HA ND MSDI H TO BE ZEROES
11036  027650  004737  006654          JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11037  027654  001405                  BEQ     22$                     ;IF OK THEN CONTINUE
11038  027656                          ERRDF   3,VDALRG,R4EROR         ;REAT H, READ H, MSDI H OR PSLO H ERROR
11039  027656  104455                  TRAP    C$ERDF
11040  027660  000003                  .WORD   3
11041  027662  002537                  .WORD   VDALRG
11042  027664  005004                  .WORD   R4EROR
11043  027666                          CKLOOP
11044  027666  104406                  TRAP    C$CLP1
11045
11046                                  ;SET THE SIGNAL XRAS H BACK TO THE HIGH STATE BY SETTING HDAL12 H TO A 1
11047
11048  027670  004737  007304  22$:    JSR     PC,XRASH                ;ASSERT XRAS H TO HIGH STATE VIA HDAL12 H
11049
11050                                  ;READ THE VDAL REGISTER AGAIN TO CHECK THAT READ H AND MSDI H ARE SET
11051                                  ;TO ONES AS A RESULT OF REAT H BEING ASSERTED HIGH.
11052
11053  027674  052737  000110  002336  BIS     #VDAL6!VDAL3,R4GOOD     ;EXPECT READ H AND MSDI H TO BE ONES
11054  027702  004737  006654          JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11055  027706  001405                  BEQ     23$                     ;IF OK THEN CONTINUE
11056  027710                          ERRDF   3,VDALRG,R4EROR         ;READ H AND/OR MSDI H NOT SET TO 1'S
11057  027710  104455                  TRAP    C$ERDF
11058  027712  000003                  .WORD   3
11059  027714  002537                  .WORD   VDALRG
11060  027716  005004                  .WORD   R4EROR
11061  027720                          CKLOOP
11062  027720  104406                  TRAP    C$CLP1
11063
11064                                  ;SET THE SIGNAL XSELO L TO THE LOW STATE BY SETTING HDAL5 H TO A ONE.
11065                                  ;WHEN XSELO L IS ASSERTED LOW, THE SIGNAL MSDI H WILL BE ASSERTED LOW.
11066
11067  027722  052737  000040  002342  23$:    BIS     #HDAL5,R6LOAD           ;SET BIT TO SET XSELO L TO LOW STATE
11068  027730  004737  006672          JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
11069  027734  001405                  BEQ     24$                     ;IF LOADED OK THEN CONTINUE
11070  027736                          ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
11071  027736  104455                  TRAP    C$ERDF
11072  027740  000004                  .WORD   4
11073  027742  002605                  .WORD   HDALRG
11074  027744  005020                  .WORD   R06ERR
11075  027746                          CKLOOP
11076  027746  104406                  TRAP    C$CLP1
11077
```

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11078                                                   ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL MSDI H IS ASSERTED
11079                                                   ;LOW WHEN THE SIGNAL XSEL0 L IS ASSERTED LOW.
11080
11081  027750  042737  000100  002336  24$:    BIC     #VDAL6,R4GOOD           ;EXPECT MSDI H TO BE A ZERO
11082  027756  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11083  027762  001405                          BEQ     25$                     ;IF OK THEN CONTINUE
11084  027764                                  ERRDF   3,VDALRG,R4EROR         ;MSDI H NOT A 0 BY XSEL0 L BEING SET LOW
11085  027764  104455                          TRAP    C$ERDF
11086  027766  000003                          .WORD   3
11087  027770  002537                          .WORD   VDALRG
11088  027772  005004                          .WORD   R4EROR
11089  027774                                  CKLOOP
11090  027774  104406                          TRAP    C$CLP1
11091
11092                                                   ;SET THE SIGNAL DMG L BY SETTING XSEL0 L AND XSEL1 L TO THE LOW STATE.
11093                                                   ;WHEN DMG L IS SET LOW, THE DMG FLIP-FLOP WILL BE SET, THUS CAUSING
11094                                                   ;THE SIGNAL PSLO H TO BE ASSERTED LOW. WHEN THE SIGNAL PSLO H IS ASSERTED
11095                                                   ;LOW, THE SIGNAL REAT H WILL BE DISABLED TO THE SIGNAL READ H, THUS
11096                                                   ;CAUSING THE SIGNAL READ H TO BE ASSERTED LOW. THE SIGNAL READ H WILL
11097                                                   ;BE READ AS A ZERO IN THE VDAL REGISTER.
11098
11099  027776  052737  000100  002342  25$:    BIS     #HDAL6,R6LOAD           ;SET BIT TO SET XSEL1 L TO LOW STATE
11100  030004  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK HDAL REGISTER
11101  030010  001405                          BEQ     26$                     ;IF OK THEN CONTINUE
11102  030012                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
11103  030012  104455                          TRAP    C$ERDF
11104  030014  000004                          .WORD   4
11105  030016  002605                          .WORD   HDALRG
11106  030020  005020                          .WORD   R06ERR
11107  030022                                  CKLOOP
11108  030022  104406                          TRAP    C$CLP1
11109
11110                                                   ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL PSLO H WAS ASSERTED
11111                                                   ;LOW WHEN THE DMG FLIP-FLOP WAS SET TO A ONE BY DMG L BEING ASSERTED LOW.
11112                                                   ;THE SIGNAL READ H SHOULD BE A ZERO WHEN PSLO H IS ASSERTED LOW.
11113
11114  030024  042737  000010  002336  26$:    BIC     #VDAL3,R4GOOD           ;EXPECT READ H TO BE A ZERO
11115  030032  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11116  030036  001405                          BEQ     27$                     ;IF OK THEN CONTINUE
11117  030040                                  ERRDF   3,VDALRG,R4EROR         ;PSLO H NOT LOW WHEN DMG F/F SET TO ONE
11118  030040  104455                          TRAP    C$ERDF
11119  030042  000003                          .WORD   3
11120  030044  002537                          .WORD   VDALRG
11121  030046  005004                          .WORD   R4EROR
11122  030050                                  CKLOOP
11123  030050  104406                          TRAP    C$CLP1
11124
11125                                                   ;SELECT FDAL AND EOAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REG 0
11126
11127  030052  004737  007154          27$:    JSR     PC,SLFDAL               ;SELECT FDAL AND EOAI REG VIA GDAL 2:0
11128
11129                                                   ;SET FDAL0 H AND FDAL1 H TO ONES AND ALL OTHER FDAL AND EOAI REGISTER
11130                                                   ;BITS TO ZEROES.  FDAL0 H ON A ONE WILL ENABLE THE EOAI REGISTER TO BE
11131                                                   ;READ WITH THE FDAL REGISTER INSTEAD OF THE CTL REGISTER WHEN A READ
11132                                                   ;COMMAND IS ISSUED TO CONTROL REGISTER 6.
11133
```

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11134  030056  012737  000003  002342          MOV     #FDAL1!FDAL0,R6LOAD     ;SETUP BITS TO BE LOADED
11135  030064  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK FDAL AND EOAI REG'S
11136  030070  001405                          BEQ     28$                     ;IF LOADED OK THEN CONTINUE
11137  030072                                  ERRDF   4,EOAIFD,R06ERR         ;EOAI OR FDAL REGISTER ERROR
11138  030072  104455                          TRAP    C$ERDF
11139  030074  000004                          .WORD   4
11140  030076  002676                          .WORD   EOAIFD
11141  030100  005020                          .WORD   R06ERR
11142  030102                                  CKLOOP
11143  030102  104406                          TRAP    C$CLP1
11144
11145                                          ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL PSLO H IS ASSERTED HIGH
11146                                          ;WHEN FDAL1 H IS A ONE AND THE DMG FLIP-FLOP IS SET TO A ONE.  THE
11147                                          ;SIGNAL REAT H, WHICH IS HIGH, SHOULD BE ENABLED TO VDAL REGISTER BIT 3
11148                                          ;AND READ AS A ONE WHEN PSLO H IS ASSERTED HIGH.
11149
11150  030104  052737  000010  002336  28$:     BIS     #VDAL3,R4GOOD           ;EXPECT READ H TO BE A ONE
11151  030112  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11152  030116  001405                          BEQ     29$                     ;IF OK THEN CONTINUE
11153  030120                                  ERRDF   3,VDALRG,R4EROR         ;PSLO H PROBABLY NOT SET HIGH BY FDAL1 H
11154  030120  104455                          TRAP    C$ERDF
11155  030122  000003                          .WORD   3
11156  030124  002537                          .WORD   VDALRG
11157  030126  005004                          .WORD   R4EROR
11158  030130                                  CKLOOP
11159  030130  104406                          TRAP    C$CLP1
11160
11161                                          ;SET FDAL1 H BACK TO THE LOW STATE BY CLEARING FDAL1 H IN FDLA REGISTER
11162
11163  030132  042737  000002  002342  29$:     BIC     #FDAL1,R6LOAD           ;SETUP TO CLEAR FDAL1 H
11164  030140  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK FDAL AND EOAI
11165  030144  001405                          BEQ     30$                     ;IF OK THEN CONTINUE
11166  030146                                  ERRDF   4,EOAIFD,R06ERR         ;EOAI OR FDAL REGISTER ERROR
11167  030146  104455                          TRAP    C$ERDF
11168  030150  000004                          .WORD   4
11169  030152  002676                          .WORD   EOAIFD
11170  030154  005020                          .WORD   R06ERR
11171  030156                                  CKLOOP
11172  030156  104406                          TRAP    C$CLP1
11173
11174                                          ;WHEN FDAL1 H IS A ZERO AND THE DMG FLIP-FLOP IS SET TO A ONE, THE
11175                                          ;SIGNAL PSLO H WILL BE ASSERTED LOW.  WHEN PSLO H IS ASSERTED LOW, THE
11176                                          ;SIGNAL READ H WILL BE READ AS A ZERO IN THE VDAL REGISTER.  THE
11177                                          ;SIGNAL READ H IS READ IN THE VDAL REGISTER AS BIT 3.
11178
11179  030160  005037  002336          30$:     CLR     R4GOOD                  ;EXPECT READ H TO BE A ZERO
11180  030164  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11181  030170  001405                          BEQ     31$                     ;IF OK THEN CONTINUE
11182  030172                                  ERRDF   3,VDALRG,R4EROR         ;PSLO H PROBABLY NOT SET LOW
11183  030172  104455                          TRAP    C$ERDF
11184  030174  000003                          .WORD   3
11185  030176  002537                          .WORD   VDALRG
11186  030200  005004                          .WORD   R4EROR
11187  030202                                  CKLOOP
11188  030202  104406                          TRAP    C$CLP1
11189
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11190                                                   ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11191
11192  030204  004737  006754          31$:    JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
11193
11194                                                   ;SET XSEL1 L AND XSEL0 L BACK TO THE HIGH STATE BY CLEARING HDAL6 AND
11195                                                   ;HDAL5 H.  THIS WILL SET THE SIGNAL DMG L TO THE HIGH STATE AND ASSERT
11196                                                   ;THE SIGNAL MSDI H TO THE HIGH STATE. THE SIGNAL XRAS H WILL BE SET LOW
11197                                                   ;AND THEN BACK TO THE HIGH STATE TO CLOCK THE DMG F/F TO THE CLEARED STATE.
11198
11199  030210  012737  030004  002342          MOV     #HDAL13!HDAL12!HDAL2,R6LOAD  ;SETUP BITS TO BE CLEARED
11200  030216  004737  007336                  JSR     PC,XRASL                ;SET XRAS H TO LOW STATE
11201  030222  004737  007304                  JSR     PC,XRASH                ;SET XRAS H TO HIGH STATE
11202
11203                                                   ;READ THE VDAL REGISTER TO CHECK THAT READ H AND MSDI H ARE ASSERTED
11204                                                   ;HIGH WHEN MR11 H, XR/WHB L, XRAS H, XCAS H, PSLO H, XSEL0 L, ADAL10 H,
11205                                                   ;REAT H, AND ETR L ARE ASSERTED HIGH AND THE PAUSE STATE WORKING FLIP-
11206                                                   ;FLOP IS CLEARED.
11207
11208  030226  052737  000110  002336          BIS     #VDAL6!VDAL3,R4GOOD     ;EXPECT READ H AND MSDI H TO BE SET
11209  030234  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11210  030240  001405                          BEQ     32$                     ;IF OK THEN CONTINUE
11211  030242                                  ERRDF   3,VDALRG,R4EROR         ;DMG FLIP-FLOP PROBABLY NOT CLEARED
11212  030242  104455                          TRAP    C$ERDF
11213  030244  000003                          .WORD   3
11214  030246  002537                          .WORD   VDALRG
11215  030250  005004                          .WORD   R4EROR
11216  030252                                  CKLOOP
11217  030252  104406                          TRAP    C$CLP1
11218
11219                                                   ;SET THE SIGNAL DMG L TO THE LOW STATE AGAIN BY SETTING XSEL0 L AND
11220                                                   ;XSEL1 L TO THE LOW STATE.  WHEN DMG L IS ASSERTED LOW, THE DMG FLIP-
11221                                                   ;FLOP WILL BE SET TO A ONE, THUS CAUSING THE SIGNAL PSLO H TO BE
11222                                                   ;ASSERTED LOW.  WHEN PSLO H IS SET LOW, THE SIGNAL REAT H, WHICH IS HIGH,
11223                                                   ;WILL BE DISBALED FROM THE SIGNAL READ H, THUS CAUSING READ H TO BE
11224                                                   ;READ IN THE VDAL REGISTER AS A ZERO.
11225
11226  030254  052737  000140  002342  32$:    BIS     #HDAL6!HDAL5,R6LOAD     ;SETUP BITS TO BE LOADED
11227  030262  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ AND CHECK HDAL REGISTER
11228  030266  001405                          BEQ     33$                     ;IF OK THEN CONTINUE
11229  030270                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
11230  030270  104455                          TRAP    C$ERDF
11231  030272  000004                          .WORD   4
11232  030274  002605                          .WORD   HDALRG
11233  030276  005020                          .WORD   R06ERR
11234  030300                                  CKLOOP
11235  030300  104406                          TRAP    C$CLP1
11236
11237                                                   ;READ THE VDAL REGISTER TO CHECK THAT PSLO H IS ASSERTED LOW AS A
11238                                                   ;RESULT OF THE DMG FLIP-FLOP BEING SET TO A ONE AND THAT MSDI H IS
11239                                                   ;ASSERTED LOW AS A RESULT OF XSEL0 L BEING ASSERTED LOW.
11240
11241  030302  005037  002336          33$:    CLR     R4GOOD                  ;EXPECT READ H AND MSDI H TO BE A 0
11242  030306  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11243  030312  001405                          BEQ     34$                     ;IF OK THEN CONTINUE
11244  030314                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
11245  030314  104455                          TRAP    C$ERDF
```

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11246  030316  000003                          .WORD   3
11247  030320  002537                          .WORD   VDALRG
11248  030322  005004                          .WORD   R4EROR
11249  030324                                  CKLOOP
11250  030324  104406                          TRAP    C$CLP1
11251
11252                                          ;SET DMG L TO THE HIGH STATE AGAIN BY SETTING XSEL0 L AND XSEL1 L TO
11253                                          ;THE HIGH STATE.  WHEN XSEL0 L IS RETURNED TO THE HIGH STATE, MSDI H
11254                                          ;WILL BE ASSERTED HIGH.
11255
11256  030326  042737  000140  002342  34$:    BIC     #HDAL6!HDAL5,R6LOAD     ;SETUP TO SET XSEL0 L AND XSEL1 L HIGH
11257  030334  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
11258  030340  001405                          BEQ     35$                     ;IF OK THEN CONTINUE
11259  030342                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL TO EXPECTED
11260  030342  104455                          TRAP    C$ERDF
11261  030344  000004                          .WORD   4
11262  030346  002605                          .WORD   HDALRG
11263  030350  005020                          .WORD   R06ERR
11264  030352                                  CKLOOP
11265  030352  104406                          TRAP    C$CLP1
11266
11267                                          ;SET VDAL2 H TO A ONE TO SET THE SIGNAL INVD L TO THE LOW STATE.  WHEN
11268                                          ;VDAL2 H IS ASSERTED LOW, THE DMG FLIP-FLOP WILL BE CLEARED, THUS
11269                                          ;CAUSING THE SIGNAL PSLO H TO BE ASSERTED HIGH AGAIN.  READ THE VDAL
11270                                          ;REGISTER TO CHECK THAT READ H AND MSDI H ARE ONES AS A RESULT OF
11271                                          ;REAT H BEING ASSERTED HIGH, PSLO H BEING ASSERTED HIGH AND XSEL0 L BEING
11272                                          ;ASSERTED HIGH.
11273
11274  030354  012737  000004  002334  35$.    MOV     #VDAL2,R4LOAD           ;SETUP BIT TO SET INVD L LOW
11275  030362  013737  002334  002336          MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
11276  030370  052737  000110  002336          BIS     #VDAL6!VDAL3,R4GOOD     ;SETUP TO EXPECT READ H AND MSDI H AS 1'S
11277  030376  004737  006646                  JSR     PC,LDRD4R               ;LOAD, READ AND CHECK VDAL REGISTER
11278  030402  001405                          BEQ     36$                     ;IF LOADED OK THEN CONTINUE
11279  030404                                  ERRDF   3,VDALRG,R4EROR         ;INVD L FAILED TO CLEAR DMG FLIP-FLOP
11280  030404  104455                          TRAP    C$ERDF
11281  030406  000003                          .WORD   3
11282  030410  002537                          .WORD   VDALRG
11283  030412  005004                          .WORD   R4EROR
11284  030414                                  CKLOOP
11285  030414  104406                          TRAP    C$CLP1
11286
11287                                          ;SET THE SIGNAL INVD L BACK TO THE HIGH STATE BY CLEARING VDAL2 H.
11288                                          ;SET THE SIGNAL FETCT H TO THE HIGH STATE BY SETTING VDAL7 H TO A ONE.
11289                                          ;THE SIGNALS READ H AND MSDI H SHOULD STILL BE READ AS ONES IN VDAL REG.
11290
11291  030416  012737  000200  002334  36$:    MOV     #VDAL7,R4LOAD           ;SETUP BIT TO LOAD - CLEAR VDAL2 H
11292  030424  013737  002334  002336          MOV     R4LOAD,R4GOOD           ;COPY DATA LOADED TO EXPECTED
11293  030432  052737  000110  002336          BIS     #VDAL6!VDAL3,R4GOOD     ;EXPECT READ H AND MSDi H TO BE ONES
11294  030440  004737  006646                  JSR     PC,LDRD4R               ;LOAD  READ AND CHECK VDAL REGISTER
11295  030444  001405                          BEQ     37$                     ;IF LOADED THEN CONTINUE
11296  030446                                  ERRDF   3,VDALRG,R4EROR         ;VDAL OR PAUSE STATE MACHINE ERROR
11297  030446  104455                          TRAP    C$ERDF
11298  030450  000003                          .WORD   3
11299  030452  002537                          .WORD   VDALRG
11300  030454  005004                          .WORD   R4EROR
11301  030456                                  CKLOOP
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11302  030456  104406                          TRAP    C$CLP1
11303
11304                                          ;THE PROGRAM WILL NOW PULSE XRAS H FROM THE HIGH STATE TO THE LOW
11305                                          ;STATE AND THEN BACK TO THE HIGH STATE.  WHEN XRAS H IS RETURNED
11306                                          ;TO THE HIGH STATE, THE PAUSE STATE WORKING FLIP-FLOP WILL BE DIRECT
11307                                          ;SET TO A ONE BY THE SIGNALS SOP H AND EDFET H BEING ASSERTED HIGH.
11308
11309  030460  004737  007336          37$:    JSR     PC,XRASL                ;SET XRAS H TO LOW STATE
11310  030464  004737  007304                  JSR     PC,XRASH                ;SET XRAS H TO HIGH STATE
11311
11312                                          ;WHEN THE PAUSE STATE WORKING FLIP-FLOP IS SET TO A ONE, THE SIGNALS
11313                                          ;PSLO H AND MSDI H WILL BE ASSERTED LOW.  WHEN PSLO H IS ASSERTED LOW
11314                                          ;THE SIGNAL REAT H WILL BE DISABLED FROM THE VDAL REGISTER THUS
11315                                          ;CAUSING THE SIGNAL READ H TO BE READ AS A ZERO.
11316
11317  030470  052737  001000  002336          BIS     #VDAL9,R4GOOD           ;EXPECT PSMW H TO BE SET TO A ONE
11318  030476  042737  000110  002336          BIC     #VDAL6!VDAL3,R4GOOD     ;EXPECT READ H AND MSDI H TO BE A 0
11319  030504  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11320  030510  001405                          BEQ     38$                     ;IF OK THEN CONTINUE
11321  030512                                  ERRDF   3,VDALRG,R4EROR         ;PSMW L PROBABLY NOT ASSERTED LOW
11322  030512  104455                          TRAP    C$ERDF
11323  030514  000003                          .WORD   3
11324  030516  002537                          .WORD   VDALRG
11325  030520  005004                          .WORD   R4EROR
11326  030522                                  CKLOOP
11327  030522  104406                          TRAP    C$CLP1
11328
11329                                          ;CLEAR ALL BITS IN HDAL REGISTER EXCEPT HDAL2 H
11330
11331  030524  012737  000004  002342  38$:    MOV     #HDAL2,R6LOAD           ;SETUP TO CLEAR ALL BITS EXCEPT HDAL2 H
11332  030532  004737  006672                  JSR     PC,LDRDR6               ;LOAD, READ ADN CHECK HDAL REGISTER
11333  030536  001405                          BEQ     39$                     ;IF LOADED OK THEN CONTINUE
11334  030540                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
11335  030540  104455                          TRAP    C$ERDF
11336  030542  000004                          .WORD   4
11337  030544  002605                          .WORD   HDALRG
11338  030546  005020                          .WORD   R06ERR
11339  030550                                  CKLOOP
11340  030550  104406                          TRAP    C$CLP1
11341
11342                                          ;PULSE INVD L TO CLEAR ALL PAUSE STATE MACHINE FLIP-FLOPS AND ANY OTHER
11343                                          ;FLIP-FLOPS THAT MAY BE SET ATE THIS TIME.
11344
11345  030552  005037  002334          39$:    CLR     R4LOAD                  ;EXPECT VDAL REGISTER BITS TO BE ZERO
11346  030556  004737  007712                  JSR     PC,CLRPSM               ;PULSE INVD L VIA VDAL2 H
11347
11348  030562                                  ENDSEG
11349  030562                          10000$:
11350  030562  104405                          TRAP    C$ESEG
11351  030564                                  ENDTST
11352  030564                          L10072:
11353  030564  104401                          TRAP    C$ETST
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11354                                   .SBTTL  TEST 41: CHECK THE SIGNALS 'FETCT H' AND 'BTS1 H'
11355
11356                                   ;++
11357                                   ; THIS TEST WILL CHECK THAT THE SIGNALS FETCT H AND BTS1 H CAN BE ASSERTED HIGH
11358                                   ; AND LOW.  THESE TWO SIGNALS ARE ASSERTED HIGH AND LOW BY CHANGING THE INPUT
11359                                   ; SIGNALS TO THE GATES WHICH GENERATE THESE SIGNALS.  THE PAUSE STATE MACHINE
11360                                   ; LOGIC IS USED TO TEST THE SIGNAL FETCT H.  THE SIGNAL FETCT H IS ALSO CHECKED
11361                                   ; ON THE SIGNAL BTS1 H.  THE SIGNAL BTS1 H IS READ IN THE VDAL REGISTER ON BIT 5.
11362                                   ;--
11363
11364  030566                                   BGNTST
11365  030566                           T41::
11366  030566  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
11367
11368  030572                                   BGNSEG
11369  030572  104404                           TRAP    C$BSEG
11370
11371                                           ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11372
11373  030574  004737  007006                   JSR     PC,SLMODR               ;SELECT MODE REGISTER VIA GDAL BITS 2:0
11374
11375                                           ;CLEAR ALL BITS IN THE MODE REGISTER WHICH WILL SET ALL OUTPUTS LOW.
11376
11377  030600  005037  002342                   CLR     R6LOAD                  ;SETUP TO CLEAR ALL BITS
11378  030604  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
11379  030610  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
11380  030612                                   ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL TO ZERO
11381  030612  104455                           TRAP    C$ERDF
11382  030614  000004                           .WORD   4
11383  030616  002631                           .WORD   MODREG
11384  030620  005020                           .WORD   R06ERR
11385  030622                                   CKLOOP
11386  030622  104406                           TRAP    C$CLP1
11387
11388                                           ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11389
11390  030624  004737  006754           1$:     JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
11391
11392                                           ;SET HDAL2 H TO A ONE AND ALL OTHER HDAL BITS TO ZEROES.  WHEN HDAL2 H
11393                                           ;IS SET TO A ONE, THE PROGRAM HAS CONTROL OVER THE T-11 TIMING AND
11394                                           ;CONTROL SIGNALS.
11395
11396  030630  012737  000004  002342           MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
11397  030636  004737  006672                   JSR     PC,LDRDR6               ;LOAD, READ AND CHECK HDAL REGISTER
11398  030642  001405                           BEQ     2$                      ;IF OK THEN CONTINUE
11399  030644                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL TO EXPECTED
11400  030644  104455                           TRAP    C$ERDF
11401  030646  000004                           .WORD   4
11402  030650  002605                           .WORD   HDALRG
11403  030652  005020                           .WORD   R06ERR
11404  030654                                   CKLOOP
11405  030654  104406                           TRAP    C$CLP1
11406
11407                                           ;SET ADAL10 H TO A ONE AND ALL OTHER ADAL BITS TO A ZERO.  ADAL10 H
11408                                           ;ON A ONE WILL ENABLE THE SIGNAL BTS1 H TO VDAL REGISTER BIT 5.
11409
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11410  030656  012737  002000  002330  2$:     MOV     #ADAL10,R2LOAD          ;SETUP BIT TO BE LOADED
11411  030664  004737  006614                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK ADAL REGISTER
11412  030670  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
11413  030672                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
11414  030672  104455                          TRAP    C$ERDF
11415  030674  000002                          .WORD   2
11416  030676  002513                          .WORD   ADALRG
11417  030700  004770                          .WORD   R2EROR
11418  030702                                  CKLOOP
11419  030702  104406                          TRAP    C$CLP1
11420
11421                                          ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING THE SIGNAL VDAL2 H.
11422                                          ;THE SIGNAL INVD L, WHEN PULSED, WILL CLEAR THE PAUSE STATE MACHINE
11423                                          ;FLIP-FLOPS, AND OTHER FLIP-FLOPS ON THE MODULE INCLUDING THE BTFET
11424                                          ;FLIP-FLOP
11425
11426  030704  005037  002334          3$:     CLR     R4LOAD                  ;SETUP TO CLEAR ALL R/W BITS
11427  030710  004737  007712                  JSR     PC,CLRPSM               ;PULSE INVD L VIA VDAL2 H
11428
11429                                          ;SET THE SIGNAL INTER L TO THE LOW STATE BY SETTING XSEL1 L TO THE
11430                                          ;LOW STATE AND XSEL0 L TO THE HIGH STATE.  WHEN HDAL5 H IS SET TO A
11431                                          ;ZERO, THE SIGNAL XSEL0 L WILL BE ASSERTED HIGH.  WHEN HDAL6 H IS SET
11432                                          ;TO A ONE, THE SIGNAL XSEL1 L WILL BE ASSERTED LOW.
11433
11434  030714  012737  000104  002342          MOV     #HDAL6!HDAL2,R6LOAD     ;SET XSEL1 L TO LOW STATE VIA HDAL6 H
11435  030722  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
11436  030726  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
11437  030730                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EPXECTED
11438  030730  104455                          TRAP    C$ERDF
11439  030732  000004                          .WORD   4
11440  030734  002605                          .WORD   HDALRG
11441  030736  005020                          .WORD   R06ERR
11442  030740                                  CKLOOP
11443  030740  104406                          TRAP    C$CLP1
11444
11445                                          ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL BTS1 H IS ASSERTED
11446                                          ;HIGH WHEN THE SIGNAL INTER L IS ASSERTED LOW AND THE BTFET FLIP-FLOP
11447                                          ;IS CLEARED.  THE BTFET FLIP-FLOP WAS CLEARED WHEN INVD L WAS PULSED.
11448
11449  030742  052737  000040  002336  4$:     BIS     #VDAL5,R4GOOD           ;SETUP TO EXPECT BTS1 H TO EQUAL A ONE
11450  030750  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11451  030754  001405                          BEQ     5$                      ;IF OK THEN CONTINUE
11452  030756                                  ERRDF   3,VDALRG,R4EROR         ;BTS1 H NOT A 1 WHEN INTER L SET LOW
11453  030756  104455                          TRAP    C$ERDF
11454  030760  000003                          .WORD   3
11455  030762  002537                          .WORD   VDALRG
11456  030764  005004                          .WORD   R4EROR
11457  030766                                  CKLOOP
11458  030766  104406                          TRAP    C$CLP1
11459
11460                                          ;SET THE SIGNAL XSEL1 L TO THE HIGH STATE BY CLEARING HDAL6 H AND SET
11461                                          ;THE SIGNAL XSEL0 L TO THE LOW STATE BY SETTING HDAL5 H TO A ONE.  WHEN
11462                                          ;XSEL0 L IS ASSERTED LOW AND XSEL1 L IS ASSERTED HIGH, THE SIGNAL INTER L
11463                                          ;WILL BE ASSERTED HIGH.  THEREFORE, THE SIGNAL BTS1 H WILL BE ASSERTED
11464                                          ;LOW AS A RESULT OF THE BTFET FLIP-FLOP BEING CLEARED AND THE SIGNAL
11465                                          ;INTER L BEING ASSERTED HIGH.
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11466
11467  030770  012737  000044  002342  5$:     MOV     #HDAL5!HDAL2,R6LOAD     ;SET XSEL0 L LOW + XSEL1 L HIGH
11468  030776  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
11469  031002  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
11470  031004                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
11471  031004  104455                          TRAP    C$ERDF
11472  031006  000004                          .WORD   4
11473  031010  002605                          .WORD   HDALRG
11474  031012  005020                          .WORD   R06ERR
11475  031014                                  CKLOOP
11476  031014  104406                          TRAP    C$CLP1
11477
11478                                          ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL BTS1 H IS READ AS A
11479                                          ;ZERO WHEN INTER L IS ASSERTED HIGH AND THE BTFET FLIP-FLOP IS CLEARED.
11480
11481  031016  005037  002336          6$:     CLR     R4GOOD                  ;SETUP TO EXPECT BTS1 H AS A ZERO
11482  031022  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11483  031026  001405                          BEQ     7$                      ;IF OK THEN CONTINUE
11484  031030                                  ERRDF   3,VDALRG,R4EROR         ;BTS1 H NOT A 0 - INTER L NOT SET HIGH
11485  031030  104455                          TRAP    C$ERDF
11486  031032  000003                          .WORD   3
11487  031034  002537                          .WORD   VDALRG
11488  031036  005004                          .WORD   R4EROR
11489  031040                                  CKLOOP
11490  031040  104406                          TRAP    C$CLP1
11491
11492                                          ;AT THIS POINT IN TIME, THE SIGNAL FETCT H SHOULD BE ASSERTED HIGH AS
11493                                          ;A RESULT OF MODE REGISTER BITS 10 AND 9 BEING A ZERO, XSEL0 L ASSERTED
11494                                          ;LOW AND XSEL1 L ASSERTED HIGH.
11495                                          ;
11496                                          ;THE PROGRAM WILL NOW PULSE THE SIGNAL XRAS H BY SETTING AND CLEARING
11497                                          ;THE SIGNAL HDAL12 H.  THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE
11498                                          ;SIGNAL FETCT H, WHICH SHOULD BE HIGH, INTO THE EDFET FLIP-FLOP, THUS
11499                                          ;SETTING THE SIGNAL EDFET H TO THE HIGH STATE.  THE SIGNAL XRAS H WILL
11500                                          ;CLOCK THE STATE OF ADAL4 H, WHICH IS LOW, INTO THE PAUSE MODE FLIP-FLOP,
11501                                          ;THUS SETTING THE SIGNAL PAUSE L TO THE HIGH STATE.  THE SIGNAL SOP H
11502                                          ;WILL BE ASSERTED HIGH WHEN PAUSE L IS ASSERTED HIGH.  WHEN SOP H AND
11503                                          ;EDFET H ARE ASSERTED HIGH, THE PAUSE STATE WORKING FLIP-FLOP WILL BE
11504                                          ;DIRECT SET TO A ONE, THUS SETTING THE SIGNAL PSMW H TO THE HIGH STATE.
11505                                          ;THE SIGNAL PSMW H WILL BE READ IN THE VDAL REGISTER AS VDAL BIT 9.
11506                                          ;
11507                                          ;WHEN FETCT H IS ASSERTED HIGH AND A PULSE IS ISSUED ON XRAS H, THE
11508                                          ;BTFET FLIP-FLOP WILL BE CLOCKED TO A ONE, THUS CAUSING THE SIGNAL
11509                                          ;BTFET L TO BE ASSERTED LOW.  WHEN BTFET L IS ASSERTED LOW AND INTER L
11510                                          ;IS ASSERTED HIGH, THE SIGNAL BTS1 H WILL BE ASSERTED HIGH.  THE SIGNAL
11511                                          ;BTS1 H WILL BE READ IN THE VDAL REGISTER AS BIT 5 WHEN ADAL10 H IS
11512                                          ;SET TO A ONE. ADAL10 H IS A ONE AT THE PRESENT TIME.
11513
11514  031042  004737  007272          7$:     JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
11515
11516                                          ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNALS PSMW H AND BTS1 H
11517                                          ;ARE ASSERTED HIGH AND THAT THEY ARE READ AS ONES IN THE VDAL REGISTER.
11518
11519  031046  052737  001040  002336          BIS     #VDAL9'VDAL5,R4GOOD     ;EXPECT PSMW H AND BTS1 H TO BE ONES
11520  031054  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11521  031060  001405                          BEQ     8$                      ;IF OK THEN CONTINUE
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11522  031062                                   ERRDF   3,VDALRG,R4EROR         ;FETCT H PROBABLY NOT SET HIGH
11523  031062  104455                           TRAP    C$ERDF
11524  031064  000003                           .WORD   3
11525  031066  002537                           .WORD   VDALRG
11526  031070  005004                           .WORD   R4EROR
11527  031072                                   CKLOOP
11528  031072  104406                           TRAP    C$CLP1
11529
11530                                           ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL2 H.  THE SIGNAL
11531                                           ;INVD L WILL CLEAR THE PAUSE STATE WORKING FLIP-FLOP AND THE BTFET
11532                                           ;FLIP-FLOP.  WHEN BTFET FLIP-FLOP IS CLEARED, THE SIGNAL BTS1 H SHOULD
11533                                           ;BE ASSERTED LOW AS A RESULT OF BTFET L BEING ASSERTED HIGH AND THE
11534                                           ;SIGNAL INTER L BEING ASSERTED HIGH.
11535
11536  031074  012737  000004  002334  8$:      MOV     #VDAL2,R4LOAD           ;SET INVD L TO LOW STATE VIA VDAL2 H
11537  031102  004737  006640                   JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REGISTER
11538  031106  001405                           BEQ     9$                      ;IF OK THEN CONTINUE
11539  031110                                   ERRDF   3,VDALRG,R4EROR         ;BTFET F/F PROBABLY NOT CLEARED BY INVD L
11540  031110  104455                           TRAP    C$ERDF
11541  031112  000003                           .WORD   3
11542  031114  002537                           .WORD   VDALRG
11543  031116  005004                           .WORD   R4EROR
11544  031120                                   CKLOOP
11545  031120  104406                           TRAP    C$CLP1
11546  031122  005037  002334          9$:      CLR     R4LOAD                  ;SET INVD L BACK TO HIGH STATE
11547  031126  004737  006640                   JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK VDAL REGISTER
11548  031132  001405                           BEQ     10$                     ;IF OK THEN CONTINUE
11549  031134                                   ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
11550  031134  104455                           TRAP    C$ERDF
11551  031136  000003                           .WORD   3
11552  031140  002537                           .WORD   VDALRG
11553  031142  005004                           .WORD   R4EROR
11554  031144                                   CKLOOP
11555  031144  104406                           TRAP    C$CLP1
11556
11557                                           ;AT THIS POINT IN TIME, THE SIGNAL FETCT H IS ASSERTED HIGH AS A
11558                                           ;RESULT OF MODE REGISTER BITS 10 AND 9 BEING CLEARED, XSEL0 L ASSERTED
11559                                           ;LOW, AND XSEL1 L ASSERTED HIGH.  TO SET THE SIGNAL FETCT H TO THE
11560                                           ;LOW STATE, THE PROGRAM WILL SET THE SIGNAL XSEL1 L TO THE LOW STATE
11561                                           ;BY SETTING HDAL6 H TO A ONE.
11562
11563  031146  012737  000144  002342  10$:     MOV     #HDAL6!HDAL5!HDAL2,R6LOAD ;SETUP BITS TO BE LOADED
11564  031154  004737  006672                   JSR     PC,LDRDR6               ;LOAD, READ AND CHECK HDAL REGISTER
11565  031160  001405                           BEQ     11$                     ;IF LOADED OK THEN CONTINUE
11566  031162                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL TO EXPECTED
11567  031162  104455                           TRAP    C$ERDF
11568  031164  000004                           .WORD   4
11569  031166  002605                           .WORD   HDALRG
11570  031170  005020                           .WORD   R06ERR
11571  031172                                   CKLOOP
11572  031172  104406                           TRAP    C$CLP1
11573
11574                                           ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING THE SIGNAL HDAL12 H.
11575                                           ;WHEN THE SIGNAL FETCT H IS ASSERTED LOW AND A PULSE IS ISSUED ON THE
11576                                           ;SIGNAL XRAS H, THE EDFET, BTFET AND PAUSE MODE FLIP-FLOPS WILL BE
11577                                           ;CLOCKED TO ZEROES.  THE PAUSE STATE WORKING FLIP-FLOP WILL BE
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11578                                   ;CLOCKED TO A ZERO AS A RESULT OF THE PAUSE STATE WORKING FLIP-FLOP
11579                                   ;ALREADY BEING CLEARED, EPFN L ASSERTED HIGH, EP8N L ASSERTED HIGH AND
11580                                   ;A PULSE BEING ISSUED ON THE SIGNAL RASP L.  WHEN XRAS H IS PULSED THE
11581                                   ;SIGNAL RASP L WILL BE PULSED.
11582
11583  031174  004737  007272    11$:  JSR     PC,XRAS                   ;GO PULSE XRAS H VIA HDAL12 H
11584
11585                                   ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP
11586                                   ;IS NOT SET WHEN THE SIGNAL FETCT H IS ASSERTED LOW BY THE SIGNAL XSEL1 L
11587                                   ;BEING ASSERTED LOW.  THE SIGNAL BTS1 H SHOULD ALSO BE ASSERTED LOW AS
11588                                   ; A RESULT OF THE BTFET FLIP-FLOP BEING A ZERO AND THE SIGNAL INTER L
11589                                   ;BEING ASSERTED HIGH.
11590
11591  031200  004737  006654           JSR     PC,READR4                 ;READ VDAL AND PAUSE STATE MACHINE
11592  031204  001405                   BEQ     12$                       ;IF OK THEN CONTINUE
11593  031206                           ERRDF   3,VDALRG,R4EROR           ;FETCT H PROBABLY NOT LOW BY XSEL1 L
11594  031206  104455                   TRAP    C$ERDF
11595  031210  000003                   .WORD   3
11596  031212  002537                   .WORD   VDALRG
11597  031214  005004                   .WORD   R4EROR
11598  031216                           CKLOOP
11599  031216  104406                   TRAP    C$CLP1
11600
11601                                   ;SET THE SIGNAL XSEL1 L BACK TO THE HIGH STATE BY CLEARING HDAL6 H.
11602                                   ;WHEN XSEL1 L IS RETURNED TO THE HIGH STATE, THE SIGNAL FETCT H SHOULD
11603                                   ;BE ASSERTED HIGH.
11604
11605  031220  012737  000044  002342 12$:  MOV     #HDAL5!HDAL2,R6LOAD       ;SET XSEL1 L TO HIGH STATE
11606  031226  004737  006672           JSR     PC,LDRDR6                 ;GO LOAD, READ AND CHECK HDAL REGISTER
11607  031232  001405                   BEQ     13$                       ;IF OK THEN CONTINUE
11608  031234                           ERRDF   4,HDALRG,R06ERR           ;HDAL REGISTER NOT EQUAL EXPECTED
11609  031234  104455                   TRAP    C$ERDF
11610  031236  000004                   .WORD   4
11611  031240  002605                   .WORD   HDALRG
11612  031242  005020                   .WORD   R06ERR
11613  031244                           CKLOOP
11614  031244  104406                   TRAP    C$CLP1
11615
11616                                   ;SELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11617
11618  031246  004737  007006    13$:  JSR     PC,SLMODR                 ;SELECT MODE REG VIA GDAL BITS 2:0
11619
11620                                   ;SET MODE REGISTER BIT 10 TO A ONE AND MODE REGISTER BIT 9 TO A ZERO.
11621
11622  031252  012737  002000  002342       MOV     #MR10,R6LOAD              ;SETUP BIT TO SET MR10 H TO HIGH STATE
11623  031260  004737  006672           JSR     PC,LDRDR6                 ;GO LOAD, READ AND CHECK MODE REGISTER
11624  031264  001405                   BEQ     14$                       ;IF LOADED OK THEN CONTINUE
11625  031266                           ERRDF   4,MODREG,R06ERR           ;MODE REGISTER NOT EQUAL EXPECTED
11626  031266  104455                   TRAP    C$ERDF
11627  031270  000004                   .WORD   4
11628  031272  002631                   .WORD   MODREG
11629  031274  005020                   .WORD   R06ERR
11630  031276                           CKLOOP
11631  031276  104406                   TRAP    C$CLP1
11632
11633                                   ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
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11634
11635  031300  004737  006754          14$:    JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
11636
11637                                          ;THE SIGNAL FETCT H SHOULD BE ASSERTED LOW AS THIS POINT IN TIME AS A
11638                                          ;RESULT OF MODE REGISTER BIT 10 BEING SET TO A ONE, MODE REGISTER BIT 9
11639                                          ;SET TO A ZERO, XSEL0 L BEING ASSERTED LOW, AND XSEL1 L BEING ASSERTED
11640                                          ;HIGH.  WHEN FETCT H IS ASSERTED LOW AND A PULSE IS ISSUED ON XRAS H,
11641                                          ;THE PAUSE STATE WORKING AND BTFET FLIP-FLOPS SHOULD BE CLOCKED TO A
11642                                          ;ZERO.
11643
11644  031304  012737  000044  002342          MOV     #HDAL5!HDAL2,R6LOAD     ;BITS PREVIOUSLY LOADED
11645  031312  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
11646
11647                                          ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING AND BTFET
11648                                          ;FLIP-FLOPS WERE CLOCKED TO ZEROES BY XRAS H WHEN THE SIGNAL FETCT H
11649                                          ;WAS ASSERTED LOW BY MODE REGISTER BIT 10 BEING A ONE.
11650
11651  031316  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11652  031322  001405                          BEQ     15$                     ;IF OK THEN CONTINUE
11653  031324                                  ERRDF   3,VDALRG,R4EROR         ;FETCT H PROBABLY NOT LOW BY MR10 H A 1
11654  031324  104455                          TRAP    C$ERDF
11655  031326  000003                          .WORD   3
11656  031330  002537                          .WORD   VDALRG
11657  031332  005004                          .WORD   R4EROR
11658  031334                                  CKLOOP
11659  031334  104406                          TRAP    C$CLP1
11660
11661                                          ;RESELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11662
11663  031336  004737  007006          15$:    JSR     PC,SLMODR               ;SELECT MODE REGISTER VIA GDAL BITS 2:0
11664
11665                                          ;SET MODE REGISTER BITS 10 AND 9 TO ONES.
11666
11667  03 342  012737  003000  002342          MOV     #MR10!MR9,R6LOAD        ;SETUP BITS TO SET MR10 + MR9 TO HIGH STATE
11668  031350  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MDOE REIGSTER
11669  031354  001405                          BEQ     16$                     ;IF LOADED OK THEN CONTINUE
11670  031356                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
11671  031356  104455                          TRAP    C$ERDF
11672  031360  000004                          .WORD   4
11673  031362  002631                          .WORD   MODREG
11674  031364  005020                          .WORD   R06ERR
11675  031366                                  CKLOOP
11676  031366  104406                          TRAP    C$CLP1
11677
11678                                          ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11679
11680  031370  004737  006754 .        16$:    JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
11681
11682                                          ;AT THIS POINT IN TIME, THE SIGNAL FETCT H SHOULD BE ASSERTED HIGH AS A
11683                                          ;RESULT OF MODE REGISTER BIT 9 BEING A ONE, XSEL0 L BFING ASSERTED LOW,
11684                                          ;AND XSEL1 L BEING ASSERTED HIGH.
11685                                          ;
11686                                          ;THE PROGRAM WILL NOW PULSE THE SIGNAL XRAS H BY SETTING AND CLEARING
11687                                          ;THE SIGNAL HDAL12 H.  WHEN FETCT H IS HIGH AND A PULSE IS ISSUED ON
11688                                          ;THE SIGNAL XRAS H, THE PAUSE STATE WORKING AND BTFET FLIP-FLOPS SHOULD
11689                                          ;BE SET TO ONES.
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11690
11691  031374  012737  000044  002342          MOV     #HDAL5.HDAL2,R6LOAD     ;SETUP BITS PREVIOUSLY LOADED
11692  031402  004737  007272                  JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
11693
11694                                          ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING FLIP-FLOP
11695                                          ;AND THE BTFET FLIP-FLOP ARE SET TO ONES AS A RESULT OF FETCT H BEING
11696                                          ;ASSERTED HIGH AND A PULSE BEING ISSUED ON XRAS H.
11697
11698  031406  012737  001040  002336          MOV     #VDAL9!VDAL5,R4GOOD     ;EXPECT PSMW H AND BTS1 H TO BE ONES
11699  031414  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11700  031420  001405                          BEQ     17$                     ;IF OK THEN CONTINUE
11701  031422                                  ERRDF   3,VDALRG,R4EROR         ;FETCT H PROBABLY NOT HIGH BY MR9 H A 1
11702  031422  104455                          TRAP    C$ERDF
11703  031424  000003                          .WORD   3
11704  031426  002537                          .WORD   VDALRG
11705  031430  005004                          .WORD   R4EROR
11706  031432                                  CKLOOP
11707  031432  104406                          TRAP    C$CLP1
11708
11709                                          ;PULSE INVD L VIA VDAL2 H TO CLEAR THE PAUSE STATE WORKING AND BTFET
11710                                          ;FLIP-FLOPS.
11711
11712  031434  005037  002334          17$:    CLR     R4LOAD                  ;SETUP TO EXPECT ALL ZEROES ON READBACK
11713  031440  004737  007712                  JSR     PC,CLRPSM               ;PULSE INVD L VIA VDAL2 H
11714
11715                                          ;RESELECT THE MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11716
11717  031444  004737  007006                  JSR     PC,SLMODR               ;SELECT MODE REG VIA GDAL BITS 2:0
11718
11719                                          ;CLEAR MODE REGISTER BIT9 AND LEAVE MODE REGISTER BIT 10 SET TO A ONE.
11720
11721  031450  012737  002000  002342          MOV     #MR10,R6LOAD            ;SETUP BIT TO BE LOADED
11722  031456  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MDOE REGISTER
11723  031462  001405                          BEQ     18$                     ;IF LOADED OK THEN CONTINUE
11724  031464                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
11725  031464  104455                          TRAP    C$ERDF
11726  031466  000004                          .WORD   4
11727  031470  002631                          .WORD   MODREG
11728  031472  005020                          .WORD   R06ERR
11729  031474                                  CKLOOP
11730  031474  104406                          TRAP    C$CLP1
11731
11732                                          ;RESELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11733
11734  031476  004737  006754          18$:    JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
11735
11736                                          ;SET XSEL0 L TO THE HIGH STATE BY CLEARING HDAL5 H.
11737
11738  031502  012737  000004  002342          MOV     #HDAL2,R6LOAD           ;SETUP TO SET XSEL0 L TO HIGH STATE
11739  031510  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
11740  031514  001405                          BEQ     19$                     ;IF OK THEN CONTINUE
11741  031516                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
11742  031516  104455                          TRAP    C$ERDF
11743  031520  000004                          .WORD   4
11744  031522  002605                          .WORD   HDALRG
11745  031524  005020                          .WORD   R06ERR
```

```
11746  031526                                  CKLOOP
11747  031526  104406                          TRAP    C$CLP1
11748
11749                                          ;AT THIS POINT IN TIME THE SIGNAL FETCT H SHOULD BE ASSERTED HIGH AS A
11750                                          ;RESULT OF MODE REGISTER BIT 9 BEING A ZERO, MODE REGISTER BIT 10 BEING
11751                                          ;A ONE, XSEL0 L ASSERTED HIGH AND EIAI0 L BEING ASSERTED LOW.  EIAI0 L
11752                                          ;IS ASSERTED LOW AS A RESULT OF CAI0 H BEING PULLED UP AND NO BUFFERS
11753                                          ;DRIVING THE CAI BUS.
11754                                          ;
11755                                          ;THE PROGRAM WILL NOW PULSE THE SIGNAL XRAS H BY SETTING AND CLEARING
11756                                          ;HDAL12 H.  WHEN FETCT H IS ASSERTED HIGH AND A PULSE IS ISSUED ON THE
11757                                          ;SIGNAL XRAS H, THE PAUSE STATE WORKING FLIP-FLOP AND THE BTFET FLIP-
11758                                          ;FLOP WILL BE SET TO ONES.
11759
11760  031530  004737  007272          19$:    JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
11761
11762                                          ;READ THE VDAL REGISTER TO CHECK THAT THE PAUSE STATE WORKING AND BTFET
11763                                          ;FLIP-FLOPS WERE SET TO ONES AS A RESULT OF FETCT H BEING ASSERTED HIGH
11764                                          ;AND A PULSE BEING ISSUED ON XRAS H.
11765
11766  031534  012.37  001040  002336          MOV     #VDAL9!VDAL5,R4GOOD     ;EXPECT PSMW H AND BTS1 H TO BE SET
11767  031542  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
11768  031546  001405                          BEQ     20$                     ;IF OK THEN CONTINUE
11769  031550                                  ERRDF   3,VDALRG,R4EROR         ;FETCT H PROBABLY NOT SET HIGH
11770  031550  104455                          TRAP    C$ERDF
11771  031552  000003                          .WORD   3
11772  031554  002537                          .WORD   VDALRG
11773  031556  005004                          .WORD   R4EROR
11774  031560                                  CKLOOP
11775  031560  104406                          TRAP    C$CLP1
11776
11777                                          ;PULSE INVDL VIA VDAL2 H TO CLEAR THE PAUSE STATE WORKING AND BTFET
11778                                          ;FLIP-FLOPS.
11779
11780  031562  005037  002334          20$:    CLR     R4LOAD                  ;SETUP TO EXPECT ALL ZEROES
11781  031566  004737  007712                  JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
11782
11783  031572                                  ENDSEG
11784  031572                          10000$:
11785  031572  104405                          TRAP    C$ESEG
11786  031574                                  ENDTST
11787  031574                          L10073:
11788  031574  104401                          TRAP    C$ETST
11789
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11790                                   .SBTTL  TEST 42: CHECK THE REFR FLIP-FLOP AND THE EDEOC H SIGNAL
11791
11792                                   ;++
11793                                   ; THIS TEST WILL CHECK THAT THE SIGNAL EDEOC H CAN BE SET TO THE HIGH STATE AND
11794                                   ; TO THE LOW STATE.  THE SIGNAL EDEOC H IS READ IN THE VDAL REGISTER ON BIT 4
11795                                   ; WHEN ADAL REGISTER BIT 10 IS SET TO A ONE.  THE PROGRAM WILL CHECK THE SIGNAL
11796                                   ; EDEOC H TO SET AND CLEAR BY CHANGING THE LOGIC LEVEL ON THE FOLLOWING SIGNALS:
11797                                   ; ADAL7 H, PSM L, INTER L, REFR L, XRAS H, XRAS L, XCAS H, XCAS L AND SOP L.
11798                                   ; THE TEST WILL USE THE SIGNAL EDEOC H TO CHECK THAT THE REFR FLIP-FLOP CAN BE
11799                                   ; SET AND CLEARED.  THE REFR FLIP-FLOP WILL BE CHECKED TO BE CLEARED BY CHANGING
11800                                   ; THE LOGIC LEVELS ON THE SIGNALS ADAL7 H AND XCAS H.  THE REFR FLIP-FLOP CAN
11801                                   ; NOT BE CHECKED TO BE CLEARED BY THE SIGNAL INVD L BECAUSE OF THE LOGIC DESIGN.
11802                                   ;--
11803
11804  031576                                   BGNTST
11805  031576                           T42:    ;
11806  031576  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
11807  031602                                   BGNSEG
11808  031602  104404                           TRAP    C$BSEG
11809
11810                                   ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
11811
11812  031604  004737  006754                   JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
11813
11814                                   ;SET HDAL2 H TO A ONE IN THE HDAL REGISTER.  WHEN HDAL2 H IS SET TO A
11815                                   ;ONE, THE PROGRAM HAS CONTROL OF THE T-11 TIMING AND CONTROL SIGNALS
11816
11817  031610  012737  000004  002342             MOV     #HDAL2,R6LOAD           ;SETUP BIT TO BE LOADED
11818  031616  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
11819  031622  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
11820  031624                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL TO EXPECTED
11821  031624  104455                           TRAP    C$ERDF
11822  031626  000004                           .WORD   4
11823  031630  002605                           .WORD   HDALRG
11824  031632  005020                           .WORD   R06ERR
11825  031634                                   CKLOOP
11826  031634  104406                           TRAP    C$CLP1
11827
11828                                   ;SET ADAL REGISTER BIT 10 TO A ONE AND ALL OTHER ADAL REGISTER BITS TO
11829                                   ;A ZERO.  ADAL10 H ON A ONE WILL ENABLE THE SIGNAL EDEOC H TO VDAL
11830                                   ;REGISTER BIT 4.  ADAL4 H ON A ZERO WILL CAUSE THE PAUSE MODE FLIP-FLOP
11831                                   ;TO BE CLOCKED TO THE PAUSE MODE WHEN XRAS H IS PULSED.  ADAL9 H ON
11832                                   ;A ZERO WILL CAUSE THE ENCLK  FLIP-FLOP TO BE CLOCKED TO A ZERO WHEN
11833                                   ;EITHER XRAS L OR XCAS L ARE PULSED
11834
11835  031636  012737  002000  002330  1$:      MOV     #ADAL10,R2LOAD          ;SETUP BIT TO BE LOADED
11836  031644  004737  006614                   JSR     PC,LDRDR2               ;LOAD, READ AND CHECK ADAL REGISTER
11837  031650  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
11838  031652                                   ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
11839  031652  104455                           TRAP    C$ERDF
11840  031654  000002                           .WORD   2
11841  031656  002513                           .WORD   ADALRG
11842  031660  004770                           .WORD   R2EROR
11843  031662                                   CKLOOP
11844  031662  104406                           TRAP    C$CLP1
11845
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11846                                   ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL REGISTER BIT 2.
11847                                   ;WHEN INVD L IS PULSED, THE PAUSE STATE MACHINE FLIP-FLOPS, THE REFR
11848                                   ;FLIP-FLOP, THE EDFET FLIP-FLOP, THE ENCLK AND ENEDC FLIP-FLOPS WILL BE
11849                                   ;CLEARED.  THE PAUSE MODE FLIP-FLOP AND THE SINGLE STEP SYNC FLIP-FLOPS
11850                                   ;WILL BE PRESET TO A ONE VIA INVD L THUS SETTING THE SIGNAL PAUSE L
11851                                   ;TO THE LOW STATE AND PSM L TO THE HIGH STATE.  THE SIGNAL FETCT H WILL
11852                                   ;BE ASSERTED HIGH BY SETTING VDAL7 H TO A ONE.  WHEN XRAS H IS PULSED
11853                                   ;LATER ON IN THIS TEST, THE EDFET FLIP-FLOP WILL BE CLOCKED TO A ONE
11854                                   ;AS A RESULT OF FETCT H BEING ASSERTED HIGH.  THE SIGNAL EDEOC H SHOULD
11855                                   ;BE READ AS A ZERO AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED
11856                                   ;AS LISTED.
11857                                   ;       INTER L  -  HIGH
11858                                   ;       REFR L   -  HIGH
11859                                   ;       XRAS H   -  LOW
11860                                   ;       XCAS L   -  HIGH
11861                                   ;       CYCLE L  -  HIGH
11862                                   ;       ADAL9 H  -  LOW
11863                                   ;       ENCLK H  -  LOW
11864                                   ;       ENEDC H  -  LOW
11865                                   ;       PSM L    -  HIGH
11866                                   ;       SUP L    -  HIGH
11867
11868  031664  012737  000200  002334  2$:   MOV     #VDAL7,R4LOAD           ;SETUP BIT TO SET FETCT H HIGH
11869  031672  004737  007712                JSR     PC,CLRPSM               ;SET FETCT H HIGH AND PULSE INVD L
11870
11871                                   ;TOGGLE THE SIGNAL XCAS L TO CLOCK THE STATE OF ADAL9 H INTO THE ENCLK
11872                                   ;FLIP-FLOP, TO CLOCK THE STATE OF THE PSMW FLIP-FLOP INTO THE PSM FLIP-
11873                                   ;FLOP AND TO CAUSE THE CYCLE ONE SHOT TO BE FIRED WHICH WILL CAUSE THE
11874                                   ;STATE OF ENCLK FLIP-FLOP TO BE CLOCKED INTO THE ENEDC FLIP-FLOP. ALL
11875                                   ;THESE FLIP-FLOPS SHOULD BE CLOCKED TO A ZERO.
11876
11877  031676  004737  007376                JSR     PC,XCAS                 ;PULSE XCAS H AND XCAS L VIA HDAL13 H
11878
11879                                   ;READ THE VDAL REGISTER TO CHECK THAT NO CHANGES OCCURED SINCE THE
11880                                   ;LAST CHECK OF THE VDAL REGISTER ABOVE.
11881
11882  031702  004737  006654                JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
11883  031706  001405                      BEQ     3$                      ;IF NO CHANGE THEN CONTINUE
11884  031710                               ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
11885  031710  104455                      TRAP    C$ERDF
11886  031712  000003                      .WORD   3
11887  031714  002537                      .WORD   VDALRG
11888  031716  005004                      .WORD   R4EROR
11889  031720                               CKLOOP
11890  031720  104406                      TRAP    C$CLP1
11891
11892                                   ;SET ADAL REGISTER BIT 9 TO A ONE.  WHEN ADAL9 H IS SET TO A ONE AND
11893                                   ;A PULSE IS ISSUED ON XRAS L OR XCAS L, THE ENCLK FLIP-FLOP WILL BE
11894                                   ;SET TO A ONE.
11895
11896  031722  052737  001000  002330  3$:   BIS     #ADAL9,R2LOAD           ;SETUP BIT TO BE LOADED
11897  031730  004737  006614                JSR     PC,LDRDR2               ;LOAD, READ AND CHECK ADLA REGISTER
11898  031734  001405                      BEQ     4$                      ;IF LOADED OK THEN CONTINUE
11899  031736                               ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
11900  031736  104455                      TRAP    C$ERDF
11901  031740  000002                      .WORD   2
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11902  031742  002513                          .WORD   ADALRG
11903  031744  004770                          .WORD   R2EROR
11904  031746                                  CKLOOP
11905  031746  104406                          TRAP    C$CLP1
11906
11907                                          ;TOGGLE THE SIGNALS XCAS H AND XCAS L BY SETTING AND CLEARING HDAL13 H.
11908                                          ;A PULSE ON XCAS H WILL CLOCK THE OUTPUT OF THE PSMW FLIP-FLOP INTO THE
11909                                          ;PSM FLIP-FLOP THUS SETTING THE SIGNAL PSM L TO THE HIGH STATE.  A PULSE
11910                                          ;ON XCAS L WILL CLOCK THE LEVEL OF ADAL9 H INTO THE ENCLK FLIP-FLOP THUS
11911                                          ;CLOCKING THAT FLIP-FLOP TO A ONE.  A PULSE ON XCAS L WILL CAUSE A PULSE
11912                                          ;ON THE SIGNAL CYCLE L WHICH WILL CAUSE THE CYCLE ONE SHOT TO BE FIRED.
11913                                          ;WHEN THE CYCLE ONE SHOT IS FIRED, THE STATE OF THE ENCLK FLIP-FLOP WILL
11914                                          ;BE CLOCKED INTO THE ENEDC FLIP-FLOP THUS SETTING THE SIGNAL ENEDC H
11915                                          ;TO THE HIGH STATE.
11916
11917  031750  004737  007376          4$:     JSR     PC,XCAS                 ;GO PULSE XCAS H AND XCAS L VIA HDAL13 H
11918
11919                                          ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H IS SET TO A
11920                                          ;ONE AS A RESULT OF THE FOLLOWING SIGNALS BEING ASSERTED AS LISTED.
11921                                          ;       INTER L  -  HIGH
11922                                          ;       REFR L   -  HIGH
11923                                          ;       XRAS H   -  LOW
11924                                          ;       XCAS L   -  HIGH
11925                                          ;       CYCLE L  -  HIGH
11926                                          ;       ADAL9 H  -  HIGH
11927                                          ;       ENCLK H  -  HIGH
11928                                          ;       ENEDC H  -  HIGH
11929                                          ;       PSM L    -  HIGH
11930                                          ;       SOP L    -  HIGH
11931
11932  031754  052737  000020  002336          BIS     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ONE
11933  031762  004737  006654                  JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
11934  031766  001405                          BEQ     5$                      ;IF OK THEN CONTINUE
11935  031770                                  ERRDF   3,VDALRG,R4EROR         ;EDEOC H PROBABLY NOT SET
11936  031770  104455                          TRAP    C$ERDF
11937  031772  000003                          .WORD   3
11938  031774  002537                          .WORD   VDALRG
11939  031776  005004                          .WORD   R4EROR
11940  032000                                  CKLOOP
11941  032000  104406                          TRAP    C$CLP1
11942
11943                                          ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  A PULSE
11944                                          ;ON XRAS H WILL CLOCK THE PAUSE MODE FLIP-FLOP TO A ZERO THUS SETTING
11945                                          ;THE SIGNALS PAUSE L AND SOP H TO THE HIGH STATES.  A PULSE ON XRAS H
11946                                          ;WILL ALSO CLOCK THE EDFET AND BTFET FLIP-FLOPS TO ONES AS A RESULT OF
11947                                          ;FETCT H BEING ASSERTED HIGH.  WHEN THE VDAL REGISTER IS READ THE
11948                                          ;SIGNALS PSMW H AND BTS1 H SHOULD BE READ AS ONES AS A RESULT OF THE
11949                                          ;PAUSE STATE WORKING AND BTFET FLIP-FLOPS BEING SET TO ONES.
11950
11951  032002  004737  007272          5$:     JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
11952
11953                                          ;READ THE VDAL REGISTER AND CHECK THAT THE SIGNAL EDEOC H WENT TO A
11954                                          ;ZERO AS A RESULT OF SOP L BEING ASSERTED LOW.  THE FOLLOWING SIGNALS
11955                                          ;SHOULD BE ASSERTED AS LISTED.  WHEN THE VDAL REGISTER IS READ, THE
11956                                          ;SIGNALS PSMW H AND BTS1 H SHOULD BE READ AS ONES AS A RESULT OF THE
11957                                          ;PAUSE STATE WORKING AND BTFET FLIP-FLOPS BEING SET TO ONES.
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11958                                          ;       INTER L  -  HIGH
11959                                          ;       REFR L   -  HIGH
11960                                          ;       XRAS H   -  LOW
11961                                          ;       XCAS L   -  HIGH
11962                                          ;       CYCLE L  -  HIGH
11963                                          ;       ADAL9 H  -  HIGH
11964                                          ;       ENCLK H  -  HIGH
11965                                          ;       ENEDC H  -  HIGH
11966                                          ;       PSM L    -  HIGH
11967                                          ;       SOP L    -  LOW
11968
11969  032006  052737  001040  002336          BIS     #VDAL9!VDAL5,R4GOOD     ;EXPECT PSMW H TO BE A ONE
11970  032014  042737  000020  002336          BIC     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ZERO
11971  032022  004737  006654                  JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
11972  032026  001405                          BEQ     6$                      ;IF OK THEN CONTINUE
11973  032030                                  ERRDF   3,VDALRG,R4EROR         ;SOP L PROBABLY FAILED TO 0 EDEOC H
11974  032030  104455                          TRAP    C$ERDF
11975  032032  000003                          .WORD   3
11976  032034  002537                          .WORD   VDALRG
11977  032036  005004                          .WORD   R4EROR
11978  032040                                  CKLOOP
11979  032040  104406                          TRAP    C$CLP1
11980
11981                                          ;SET ADAL REGISTER BIT 4 TO A ONE.  WHEN XRAS H IS PULSED, THE PAUSE
11982                                          ;MODE FLIP-FLOP WILL BE CLOCKED TO RUN MODE THUS SETTING THE SIGNALS
11983                                          ;PAUSE L AND SOP H TO THE LOW STATE.  THE SIGNAL SOP L WILL BE ASSERTED
11984                                          ;TO THE HIGH STATE.
11985
11986  032042  052737  000020  002330  6$:     BIS     #ADAL4,R2LOAD           ;SETUP BIT TO BE LOADED
11987  032050  004737  006614                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK ADAL REGISTER
11988  032054  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
11989  032056                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
11990  032056  104455                          TRAP    C$ERDF
11991  032060  000002                          .WORD   2
11992  032062  002513                          .WORD   ADALRG
11993  032064  004770                          .WORD   R2EROR
11994  032066                                  CKLOOP
11995  032066  104406                          TRAP    C$CLP1
11996
11997                                          ;SET THE SIGNAL FETCT H TO THE LOW STATE AND CHECK THAT NO CHANGES HAVE
11998                                          ;OCCURED IN THE VDAL REGISTER.  NO CHANGES SHOULD OCCUR UNTIL XRAS H IS
11999                                          ;PULSED AGAIN.
12000
12001  032070  042737  000200  002334  7$:     BIC     #VDAL7,R4LOAD           ;SETUP BIT TO CLEAR FETCT H
12002  032076  042737  000200  002336          BIC     #VDAL7,R4GOOD           ;EXPECT FETCT H TO BE A 0 ON A READ
12003  032104  004737  006646                  JSR     PC,LDRD4R               ;LOAD, READ AND CHECK VDAL REGISTER
12004  032110  001405                          BEQ     8$                      ;IF OK THEN CONTINUE
12005  032112                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
12006  032112  104455                          TRAP    C$ERDF
12007  032114  000003                          .WORD   3
12008  032116  002537                          .WORD   VDALRG
12009  032120  005004                          .WORD   R4EROR
12010  032122                                  CKLOOP
12011  032122  104406                          TRAP    C$CLP1
12012
12013                                          ;PULSE THE SIGNAL XRAS H TO SET THE SIGNAL PAUSE L TO THE LOW STATE AND
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12014                                          ;THE SIGNAL SOP L TO THE HIGH STATE.  THE SIGNALS EDFET H AND BTFET H
12015                                          ;WILL BE CLOCKED TO A LOW STATE AS A RESULT OF THE SIGNAL FETCT H BEING
12016                                          ;ASSERTED LOW AND A PULSE BEING ISSUED ON THE SIGNAL XRAS H.
12017
12018  032124  004737  007272          8$:     JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
12019
12020                                          ;READ THE VDAL REGISTER AND CHECK THE THE SIGNAL EDEOC H IS SE' TO A
12021                                          ;ONE AS A RESULT OF THE FOLLOWING SIGNALS BE.ING SE' TO THE STATES LISTED
12022                                          ;       INTER L  -  HIGH
12023                                          ;       REFR L   -  HIGH
12024                                          ;       XRAS H   -  LOW
12025                                          ;       XCAS L   -  HIGH
12026                                          ;       CYCLE L  -  HIGH
12027                                          ;       ADAL9 H  -  HIGH
12028                                          ;       ENCLK H  -  HIGH
12029                                          ;       ENEDC H  -  HIGH
12030                                          ;       PSM L    -  HIGH
12031                                          ;       SOP L    -  HIGH
12032
12033  032130  052737  000020  002336          BIS     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE SET TO A ONE
12034  032136  042737  000040  002336          BIC     #VDAL5,R4GOOD           ;EXPECT BTS1 H TO BE A ZERO
12035  032144  004737  006654                  JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
12036  032150  001405                          BEQ     9$                      ;IF OK THEN CONTINUE
12037  032152                                  ERRDF   3,VDALRG,R4EROR         ;EDEOC H PROBABLY NOT SET TO A ONE
12038  032152  104455                          TRAP    C$ERDF
12039  032154  000003                          .WORD   3
12040  032156  002537                          .WORD   VDALRG
12041  032160  005004                          .WORD   R4EROR
12042  032162                                  CKLOOP
12043  032162  104406                          TRAP    C$CLP1
12044
12045                                          ;PULSE THE SIGNALS XCAS H AND XCAS L BY SETTING AND CLEARING HDAL13 H.
12046                                          ;A PULSE ON XCAS H WILL CLOCK THE PSM FLIP-FLOP TO A ZERO AS A RESULT
12047                                          ;OF THE PSMW FLIP-FLOP BEING SET TO A ONE.  THE ENEDC FLIP-FLOP WILL
12048                                          ;AGAIN BE CLOCKED TO A ONE AS A RESULT OF XCAS L BEING PULSED AND
12049                                          ;ADAL9 H BEING SET TO A ONE.
12050
12051  032164  004737  007376          9$:     JSR     PC,XCAS                 ;GO PULSE XCAS H AND XCAS L VIA HDAL13 H
12052
12053                                          ;CHECK EDEOC H TO BE A ZERO AS A RESULT OF THE PSM FLIP-FLOP BEING
12054                                          ;CLEARED.  TEH FOLLOWING SIGNALS SHOULD BE ASSERTED IN THE STATES AS
12055                                          ;LISTED BELOW.
12056                                          ;       INTER L  -  HIGH
12057                                          ;       REFR L   -  HIGH
12058                                          ;       XRAS H   -  LOW
12059                                          ;       XCAS L   -  HIGH
12060                                          ;       CYCLE L  -  HIGH
12061                                          ;       ADAL9 H  -  HIGH
12062                                          ;       ENCLK H  -  HIGH
12063                                          ;       ENEDC H  -  HIGH
12064                                          ;       PSM L    -  LOW
12065                                          ;       SOP L    -  HIGH
12066
12067  032170  042737  000020  002336          BIC     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ZERO
12068  032176  004737  006654                  JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
12069  032202  001405                          BEQ     10$                     ;IF OK THEN CONTINUE
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12070  032204                          ERRDF   3,VDALRG,R4EROR         ;PSM L PROBABLY NOT ASSERTED LOW
12071  032204  104455                  TRAP    C$ERDF
12072  032206  000003                  .WORD   3
12073  032210  002537                  .WORD   VDALRG
12074  032212  005004                  .WORD   R4EROR
12075  032214                          CKLOOP
12076  032214  104406                  TRAP    C$CLP1
12077
12078                                  ;PULE THE SIGNAL INVD L BE SETTING AND CLEARING VDAL REGISTER BIT 2.
12079                                  ;A PULSE ON INVD L WILL CLEAR ALL THE PAUSE STATE MACHINE FLIP-FLOPS,
12080                                  ;THE EDFET FLIP-FLOP, THE ENCLK  AND ENEDC FLIP-FLOPS.  THE PAUSE
12081                                  ;AND PSM FLIP-FLOPS WILL BE PRESET TO A ONE THUS SETTING THE SIGNALS
12082                                  ;PAUSE L TO THE LOW STATE AND PSM L TO THE HIGH STATE.
12083
12084  032216  005037  002334  10$:    CLR     R4LOAD                  ;SETUP TO CLEAR ALL R/W BITS
12085  032222  004737  007712          JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
12086
12087                                  ;PULSE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  THE PAUSE
12088                                  ;MODE FLIP-FLOP WILL BE SET TO RUN MODE AS A RESULT OF ADAL4 H BEING
12089                                  ;ASSERTED HIGH.  THE ENCLK FLIP-FLOP WILL BE CLOCKED TO A ONE AS A
12090                                  ;RESULT OF ADAL9 H BEING ASSERTED HIGH.
12091
12092  032226  004737  007272          JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
12093
12094                                  ;READ VDAL REGISTER TO CHECK THAT EDEOC H IS STILL A ZERO AFTER
12095                                  ;PULSING XRAS H,  THE FOLLOWING SIGNALS SHOULD BE ASSERTED AS LISTED
12096                                  ;       INTER L  -  HIGH
12097                                  ;       REFR L   -  HIGH
12098                                  ;       XRAS H   -  LOW
12099                                  ;       XCAS L   -  HIGH
12100                                  ;       CYCLE L  -  HIGH
12101                                  ;       ADAL9 H  -  HIGH
12102                                  ;       ENCLK H  -  HIGH
12103                                  ;       ENEDC H  -  LOW
12104                                  ;       PSM L    -  HIGH
12105                                  ;       SOP L    -  HIGH
12106
12107  032232  004737  006654          JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
12108  032236  001405                  BEQ     11$                     ;IF OK THEN CONTINUE
12109  032240                          ERRDF   3,VDALRG,R4EROR         ;INVD L PROBABLY NOT O'ED ENEDC F/F
12110  032240  104455                  TRAP    C$ERDF
12111  032242  000003                  .WORD   3
12112  032244  002537                  .WORD   VDALRG
12113  032246  005004                  .WORD   R4EROR
12114  032250                          CKLOOP
12115  032250  104406                  TRAP    C$CLP1
12116
12117                                  ;PULSE THE SIGNALS XCAS H AND XCAS L BY SETTING AND CLEARING HDAL13 H.
12118                                  ;A PULSE ON XCAS H WILL CLOCK THE PSM FLIP-FLOP TO A ONE AND A PULSE ON
12119                                  ;XCAS L WILL CLOCK THE ENEDC FLIP-FLOP TO A ONE.
12120
12121  032252  004737  007376  11$:    JSR     PC,XCAS                 ;GO PULSE XCAS H AND XCAS L VIA HDAL13 H
12122
12123                                  ;READ THE VDAL REGISTER TO CHECK THAT THE SIGNAL EDEOC H WAS SET TO A
12124                                  ;ONE AS A RESULT OF ENEDC FLIP-FLOP BEING SET TO A ONE.  THE FOLLOWING SIGNALS
12125                                  ;SHOULD BE ASSERTED AS LISTED BELOW
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12126                                           ;       INTER L  -  HIGH
12127                                           ;       REFR L   -  HIGH
12128                                           ;       XRAS H   -  LOW
12129                                           ;       XCAS L   -  HIGH
12130                                           ;       CYCLE L  -  HIGH
12131                                           ;       ADAL9 H  -  HIGH
12132                                           ;       ENCLK H  -  HIGH
12133                                           ;       ENEDC H  -  HIGH
12134                                           ;       PSM L    -  HIGH
12135                                           ;       SOP L    -  HIGH
12136
12137  032256  052737  000020  002336           BIS     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE ASSERTED
12138  032264  004737  006654                   JSR     PC,READR4               ;READ AND CHECK VDAL REGISTER
12139  032270  001405                           BEQ     12$                     ;IF OK THEN CONTINUE
12140  032272                                   ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
12141  032272  104455                           TRAP    C$ERDF
12142  032274  000003                           .WORD   3
12143  032276  002537                           .WORD   VDALRG
12144  032300  005004                           .WORD   R4EROR
12145  032302                                   CKLOOP
12146  032302  104406                           TRAP    C$CLP1
12147
12148                                           ;SET THE SIGNALS XCAS H AND XCAS L TO THE HIGH AND LOW STATE RESPECTIVELY
12149                                           ;BY SETTING HDAL13 H TO A ONE.  XCAS H BEING SET HIGH WILL CLOCK THE
12150                                           ;SINGLE STEP SYNC FLIP-FLOP TO A ONE THUS SETTING THE SIGNAL PSM L TO
12151                                           ;THE HIGH STATE.
12152
12153  032304  004737  007410           12$:    JSR     PC,XCASH                ;SET XCAS H HIGH AND XCAS L LOW
12154
12155                                           ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT OF
12156                                           ;THE SIGNALS BELOW BEING IN THE FOLLOWING STATE.
12157                                           ;       INTER L  -  HIGH
12158                                           ;       REFR L   -  HIGH
12159                                           ;       XRAS H   -  LOW
12160                                           ;       XCAS L   -  LOW
12161                                           ;       ENEDC H  -  HIGH
12162                                           ;       PSM L    -  HIGH
12163                                           ;       SOP L    -  HIGH
12164
12165  032310  042737  000020  002336           BIC     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ZERO
12166  032316  004737  006654                   JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12167  032322  001405                           BEQ     13$                     ;IF OK THEN CONTINUE
12168  032324                                   ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
12169  032324  104455                           TRAP    C$ERDF
12170  032326  000003                           .WORD   3
12171  032330  002537                           .WORD   VDALRG
12172  032332  005004                           .WORD   R4EROR
12173  032334                                   CKLOOP
12174  032334  104406                           TRAP    C$CLP1
12175
12176                                           ;SET THE SIGNALS XCAS H AND XCAS L TO THE LOW AND HIGH STATE RESPECTIVELY
12177                                           ;BY CLEARING HDAL13 H IN THE HDAL REGISTER.
12178
12179  032336  004737  007442           13$:    JSR     PC,XCASL                ;SET XCAS H LOW AND XCAS L HIGH
12180
12181                                           ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
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12182                                           ;THE FOLLOWING SIGNALS BEING SET AS LISTED.
12183                                           ;       INTER L  -  HIGH
12184                                           ;       REFR L   -  HIGH
12185                                           ;       XRAS H   -  LOW
12186                                           ;       XCAS L   -  HIGH
12187                                           ;       ENEDC H  -  HIGH
12188                                           ;       PSM L    -  HIGH
12189                                           ;       SOP L    -  HIGH
12190
12191  032342  052737  000020  002336          BIS     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE SET TO A ONE
12192  032350  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12193  032354  001405                          BEQ     14$                     ;IF OK THEN CONTINUE
12194  032356                                  ERRDF   3,VDALRG,R4EROR         ;EDEOC H PROBABLY NOT SET HIGH
12195  032356  104455                          TRAP    C$ERDF
12196  032360  000003                          .WORD   3
12197  032362  002537                          .WORD   VDALRG
12198  032364  005004                          .WORD   R4EROR
12199  032366                                  CKLOOP
12200  032366  104406                          TRAP    C$CLP1
12201
12202                                           ;SET THE SIGNAL XRAS H TO THE HIGH STATE BY SETTING HDAL12 H TO A ONE.
12203                                           ;WHEN ADAL7 H IS A ZERO, THE REFR FLIP-FLOP WILL BE HELD TO THE
12204                                           ;CLEARED STATE AND WILL NOT BE CLOCKED TO A ONE BY XRAS L WHEN THE
12205                                           ;SIGNAL INTER L IS ASSERTED HIGH.  THERFORE THE SIGNAL REFR L WILL
12206                                           ;REMAIN ASSERTED HIGH.
12207
12208  032370  004737  007304          14$:    JSR     PC,XRASH                ;SET XRAS H HIGH AND XRAS L LOW
12209
12210                                           ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12211                                           ;THE FOLLOWING SIGNALS BEING SET AS LISTED.
12212                                           ;       INTER L  -  HIGH
12213                                           ;       REFR L   -  HIGH
12214                                           ;       XRAS H   -  HIGH
12215                                           ;       XCAS L   -  HIGH
12216                                           ;       ADAL9 H  -  HIGH
12217                                           ;       PSM L    -  HIGH
12218                                           ;       SOP L    -  HIGH
12219
12220  032374  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12221  032400  001405                          BEQ     15$                     ;IF OK THEN CONTINUE
12222  032402                                  ERRDF   3,VDALRG,R4EROR         ;EDEOC H PROBABLY ASSERTED LOW
12223  032402  104455                          TRAP    C$ERDF
12224  032404  000003                          .WORD   3
12225  032406  002537                          .WORD   VDALRG
12226  032410  005004                          .WORD   R4EROR
12227  032412                                  CKLOOP
12228  032412  104406                          TRAP    C$CLP1
12229
12230                                           ;SET THE SIGNAL INTER L TO THE LOW STATE BY SETTING XSEL1 L TO THE
12231                                           ;LOW STATE.  XSEL1 L WILL BE SET LOW BY SETTING HDAL6 H TO A ONE.
12232
12233  032414  052737  000100  002342  15$:    BIS     #HDAL6,R6LOAD           ;SET XSEL1 L TO THE LOW STATE
12234  032422  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
12235  032426  001405                          BEQ     16$                     ;IF LOADED OK THEN CONTINUE
12236  032430                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
12237  032430  104455                          TRAP    C$ERDF
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12238  032432  000004                          .WORD   4
12239  032434  002605                          .WORD   HDALRG
12240  032436  005020                          .WORD   R06ERR
12241  032440                                  CKLOOP
12242  032440  104406                          TRAP    C$CLP1
12243
12244                                          ;CHECK THE SIGNAL BTS1 H TO BE SET TO A ONE AS A RESULT OF THE BTSET
12245                                          ;FLIP-FLOP BEING CLEARED AND THE SIGNAL INTER L BEING ASSERTED LOW.
12246                                          ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT OF
12247                                          ;THE FOLLOWING SIGNALS BEING SET AS LISTED.
12248                                          ;       INTER L  -  LOW
12249                                          ;       REFR L   -  HIGH
12250                                          ;       XRAS H   -  HIGH
12251                                          ;       XCAS L   -  HIGH
12252                                          ;       ENEDC H  -  HIGH
12253                                          ;       PSM L    -  HIGH
12254                                          ;       SOP L    -  HIGH
12255
12256  032442  052737  000040  002336  16$:   BIS     #VDAL5,R4GOOD           ;EXPECT BTS1 H TO BE A ONE VIA INTER L
12257  032450  042737  000020  002336          BIC     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ZERO
12258  032456  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12259  032462  001405                          BEQ     17$                     ;IF OK THEN CONTINUE
12260  032464                                  ERRDF   3,VDALRG,R4EROR         ;EDEOC H NOT 0 WHEN INTER L SET LOW
12261  032464  104455                          TRAP    C$ERDF
12262  032466  000003                          .WORD   3
12263  032470  002537                          .WORD   VDALRG
12264  032472  005004                          .WORD   R4EROR
12265  032474                                  CKLOOP
12266  032474  104406                          TRAP    C$CLP1
12267
12268                                          ;SET THE SIGNAL XRAS H TO THE LOW STATE BY CLEARING HDAL12 H.
12269
12270  032476  004737  007336          17$.    JSR     PC,XRASL                ;SET XRAS H TO THE LOW STATE
12271
12272                                          ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12273                                          ;THE FOLLOWING SIGNALS BEING SET AS LISTED
12274                                          ;       INTER L  -  LOW
12275                                          ;       REFR L   -  HIGH
12276                                          ;       XRAS H   -  LOW
12277                                          ;       XCAS L   -  HIGH
12278                                          ;       ENEDC H  -  HIGH
12279                                          ;       PSM L    -  HIGH
12280                                          ;       SOP L    -  HIGH
12281
12282  032502  052737  000020  002336          BIS     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ONE
12283  032510  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12284  032514  001405                          BEQ     18$                     ;IF OK THEN CONTINUE
12285  032516                                  ERRDF   3,VDALRG,R4EROR         ;EDEOC H NOT 1 WHEN XRAS H SET LOW
12286  032516  104455                          TRAP    C$ERDF
12287  032520  000003                          .WORD   3
12288  032522  002537                          .WORD   VDALRG
12289  032524  005004                          .WORD   R4EROR
12290  032526                                  CKLOOP
12291  032526  104406                          TRAP    C$CLP1
12292
12293                                          ;SET THE SIGNAL INTER L BACK TO THE HIGH STATE BY SETTING XSEL1 L HIGH.
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12294                                          ;XSEL1 L IS SET HIGH BY CLEARING HDAL6 H IN THE HDAL REGISTER.
12295
12296  032530  042737  000100  002342  18$:    BIC     #HDAL6,R6LOAD          ;SETUP TO SET XSEL1 L TO HIGH STATE
12297  032536  004737  006672                  JSR     PC,LDRDR6              ;GO LOAD, READ AND CHECK HDAL REGISTER
12298  032542  001405                         BEQ     19$                    ;IF LOADED OK TEHN CONTINUE
12299  032544                                 ERRDF   4,HDALRG,R06ERR        ;HDAL REGISTER NOT EQUAL EXPECTED
12300  032544  104455                         TRAP    C$ERDF
12301  032546  000004                         .WORD   4
12302  032550  002605                         .WORD   HDALRG
12303  032552  005020                         .WORD   R06ERR
12304  032554                                 CKLOOP
12305  032554  104406                         TRAP    C$CLP1
12306
12307                                          ;CHECK THE SIGNAL BTS1 H TO BE A ZERO AS A RESULT OF THE BTFET FLIP-FLOP
12308                                          ;BEING CLEARED AND THE SIGNAL INTER L BEING SET TO THE HIGH STATE.
12309                                          ;
12310                                          ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12311                                          ;THE FOLLOWING SIGNALS BEING SET AS LISTED BELOW.
12312                                          ;       INTER L  -  HIGH
12313                                          ;       REFR L   -  HIGH
12314                                          ;       XRAS H   -  LOW
12315                                          ;       XCAS L   -  HIGH
12316                                          ;       ENEDC H  -  HIGH
12317                                          ;       PSM L    -  HIGH
12318                                          ;       SOP L    -  HIGH
12319
12320  032556  042737  000040  002336  19$:    BIC     #VDAL5,R4GOOD          ;EXPECT BTS1 H TO BE A 0 VIA INTER L
12321  032564  004737  006654                  JSR     PC,READR4              ;READ VDAL AND PAUSE STATE MACHINE
12322  032570  001405                         BEQ     20$                    ;IF OK THEN CONTINUE
12323  032572                                 ERRDF   3,VDALRG,R4EROR        ;EDEOC H NOT A ONE WHEN INTER L HIGH
12324  032572  104455                         TRAP    C$ERDF
12325  032574  000003                         .WORD   3
12326  032576  002537                         .WORD   VDALRG
12327  032600  005004                         .WORD   R4EROR
12328  032602                                 CKLOOP
12329  032602  104406                         TRAP    C$CLP1
12330
12331                                          ;SET THE SIGNAL ADAL7 H TO A ONE. WHEN ADAL7 H IS A ONE, THE REFR FLIP-
12332                                          ;FLOP CAN BE CLEARED EITHER BY XCAS H BEING SET HIGH, OR INVD L BEING
12333                                          ;SET LOW, OR BY ADAL7 H BEING SET BACK TO A ZERO.  THE REFR FLIP-FLOP
12334                                          ;CAN NOT BE CHECKED TO BE CLEARED BY THE SIGNAL INVD L BECAUSE OF THE
12335                                          ;LOGIC DESIGN.
12336
12337  032604  052737  000200  002330  20$:    BIS     #ADAL7,R2LOAD          ;SETUP BIT TO BE LOADED
12338  032612  004737  006614                  JSR     PC,LDRDR2              ;GO LOAD, READ AND CHECK ADAL REGISTER
12339  032616  001405                         BEQ     21$                    ;IF OK THEN CONTINUE
12340  032620                                 ERRDF   2,ADALRG,R2EPOR        ;ADAL REGISTER NOT EQUAL EXPECTED
12341  032620  104455                         TRAP    C$ERDF
12342  032622  000002                         .WORD   2
12343  032624  002513                         .WORD   ADALRG
12344  032626  004770                         .WORD   R2EROR
12345  032630                                 CKLOOP
12346  032630  104406                         TRAP    C$CLP1
12347
12348
12349                                          ;SET THE SIGNALS XRAS H AND XRAS L TO THE HIGH AND LOW STATES RESPECTIVELY
                                               ;BY SETTING HDAL12 H TO A ONE.  SETTING XRAS L TO THE LOW STATE WILL
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12350                                   ;CLOCK THE LEVEL OF INTER L, WHICH IS HIGH, INTO THE REFR FLIP-FLOP,
12351                                   ;THUS CLOCKING THE FLIP-FLOP TO A ONE.  WHEN THE REFR FLIP-FLOP IS
12352                                   ;SET TO A ONE, THE SIGNAL REFR L WILL BE ASSERTED TO THE LOW STATE.
12353
12354  032632  004737  007304    21$:   JSR     PC,XRASH                 ;SET XRAS H HIGH AND XRAS L LOW
12355
12356                                   ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT OF
12357                                   ;THE FOLLOWING SIGNALS BEING SET AS LISTED BELOW.
12358                                   ;       INTER L   -  HIGH
12359                                   ;       REFR L    -  LOW
12360                                   ;       XRAS H    -  HIGH
12361                                   ;       XCAS L    -  HIGH
12362                                   ;       ENEDC H   -  HIGH
12363                                   ;       PSM L     -  HIGH
12364                                   ;       SOP L     -  HIGH
12365
12366  032636  042737  000020  002336    BIC     #VDAL4,R4GOOD            ;EXPECT EDEOC H TO BE A ZERO
12367  032644  004737  006654            JSR     PC,READR4                ;READ VDAL AND PAUSE STATE MACHINE
12368  032650  001405                    BEQ     22$                      ;IF OK THEN CONTINUE
12369  032652                            ERRDF   3,VDALRG,R4EROR          ;REFR F/F PROBABLY NOT SET TO A ONE
12370  032652  104455                    TRAP    C$ERDF
12371  032654  000003                    .WORD   3
12372  032656  002537                    .WORD   VDALRG
12373  032660  005004                    .WORD   R4EROR
12374  032662                            CKLOOP
12375  032662  104406                    TRAP    C$CLP1
12376
12377                                   ;PULSE THE SIGNAL XCAS H BY SETTING AND CLEARING HDAL13 H.  A PULSE
12378                                   ;ON XCAS H WHEN ADAL7 H IS SET TO A ONE WILL CLEAR THE REFR FLIP-FLOP,
12379                                   ;THUS SETTING THE SIGNAL REFR L TO THE HIGH STATE.
12380
12381  032664  004737  007376    22$:   JSR     PC,XCAS                  ;PULSE XCAS H AND XCAS L VIA HDAL13 H
12382
12383                                   ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12384                                   ;THE FOLLOWING SIGNALS BEING SET AS LISTED
12385                                   ;       INTER L   -  HIGH
12386                                   ;       REFR L    -  HIGH
12387                                   ;       XRAS H    -  HIGH
12388                                   ;       XCAS L    -  HIGH
12389                                   ;       ENEDC H   -  HIGH
12390                                   ;       PSM L     -  HIGH
12391                                   ;       SOP L     -  HIGH
12392
12393  032670  052737  000020  002336    BIS     #VDAL4,R4GOOD            ;EXPECT EDEOC H TO BE A ONE
12394  032676  004737  006654            JSR     PC,READR4                ;READ VDAL AND PAUSE STATE MACHINE
12395  032702  001405                    BEQ     23$                      ;IF OK THEN CONTINUE
12396  032704                            ERRDF   3,VDALRG,R4EROR          ;REFR F/F NOT CLEARED BY XCAS H
12397  032704  104455                    TRAP    C$ERDF
12398  032706  000003                    .WORD   3
12399  032710  002537                    .WORD   VDALRG
12400  032712  005004                    .WORD   R4EROR
12401  032714                            CKLOOP
12402  032714  104406                    TRAP    C$CLP1
12403
12404                                   ;SET XRAS H AND XRAS L TO THE LOW AND HIGH STATES RESPECTIVELY BY
12405                                   ;CLEARING HDAL12 H.  THIS IS DONE SO THAT THE REFR FLIP-FLOP CAN BE
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12406                                           ;SET TO A ONE AGAIN WHEN XRAS H IS PULSED AGAIN IN THE NEXT SECTION
12407
12408  032716  004737  007336          23$:    JSR     PC,XRASL                ;SET XRAS H LOW AND XRAS L HIGH
12409
12410                                           ;SET THE SIGNAL XRAS H AND XRAS L TO THE HIGH AND LOW STATE RESPECTIVELY
12411                                           ;BY SETTING HDAL12 H TO A ONE.  SETTING XRAS L TO THE LOW STATE WILL
12412                                           ;CLOCK THE LEVEL OF INTER L, WHICH IS HIGH, INTO THE REFR FLIP-FLOP,
12413                                           ;THUS SETTING THE FLIP-FLOP TO A ONE. THE SIGNAL REFR L WILL BE SET TO
12414                                           ;THE LOW STATE WHEN THE REFR FLIP-FLOP IS SET TO A ONE.
12415
12416  032722  004737  007304                  JSR     PC,XRASH                ;SET XRAS H HIGH AND XRAS L LOW
12417
12418                                           ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT OF
12419                                           ;THE FOLLOWING SIGNALS BEING SET AS LISTED.
12420                                           ;       INTER L  -  HIGH
12421                                           ;       REFR L   -  LOW
12422                                           ;       XRAS H   -  HIGH
12423                                           ;       XCAS L   -  HIGH
12424                                           ;       ENEDC H  -  HIGH
12425                                           ;       PSM L    -  HIGH
12426                                           ;       SOP L    -  HIGH
12427
12428  032726  042737  000020  002336          BIC     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ZERO
12429  032734  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12430  032740  001405                          BEQ     24$                     ;IF OK THEN CONTINUE
12431  032742                                  ERRDF   3,VDALRG,R4EROR         ;REFR F/F PROBABLY NOT SET TO A ONE
12432  032742  104455                          TRAP    C$ERDF
12433  032744  000003                          .WORD   3
12434  032746  002537                          .WORD   VDALRG
12435  032750  005004                          .WORD   R4EROR
12436  032752                                  CKLOOP
12437  032752  104406                          TRAP    C$CLP1
12438
12439                                           ;SET THE SIGNAL ADAL7 H TO A ZERO.  WHEN ADAL7 H IS SET TO A ZERO, THE
12440                                           ;REFR FLIP-FLOP WILL BE CLEARED, THUS SETTING THE SIGNAL REFR L TO THE
12441                                           ;HIGH STATE.
12442
12443  032754  042737  000200  002330  24$:    BIC     #ADAL7,R2LOAD           ;SET ADAL7 H TO A ZERO
12444  032762  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
12445  032766  001405                          BEQ     25$                     ;IF LOADED OK THEN CONTINUE
12446  032770                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
12447  032770  104455                          TRAP    C$ERDF
12448  032772  000002                          .WORD   2
12449  032774  002513                          .WORD   ADALRG
12450  032776  004770                          .WORD   R2EROR
12451  033000                                  CKLOOP
12452  033000  104406                          TRAP    C$CLP1
12453
12454                                           ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12455                                           ;THE FOLLOWING SIGNALS BEING SET AS LISTED
12456                                           ;       INTER L  -  HIGH
12457                                           ;       REFR L   -  HIGH
12458                                           ;       XRAS H   -  HIGH
12459                                           ;       XCAS L   -  HIGH
12460                                           ;       ENEDC H  -  HIGH
12461                                           ;       PSM L    -  HIGH
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12462                                                   ;       SOP L    -  HIGH
12463
12464  033002  052737  000020  002336  25$:    BIS     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ONE
12465  033010  004737  006654                   JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12466  033014  001405                           BEQ     26$                     ;IF OK THEN CONTINUE
12467  033016                                   ERRDF   3,VDALRG,R4EROR         ;REFR F/F NOT CLEARED BY ADAL7 H A 0
12468  033016  104455                           TRAP    C$ERDF
12469  033020  000003                           .WORD   3
12470  033022  002537                           .WORD   VDALRG
12471  033024  005004                           .WORD   R4EROR
12472  033026                                   CKLOOP
12473  033026  104406                           TRAP    C$CLP1
12474
12475                                           ;SET ADAL7 H BACK TO A ONE.  THIS WILL ALLOW THE REFR FLIP-FLOP TO
12476                                           ;BE CLEARED.
12477
12478  033030  052737  000200  002330  26$:    BIS     #ADAL7,R2LOAD           ;SETUP BIT TO BE LOADED
12479  033036  004737  006614                   JSR     PC,LDRDR2               ;LOAD, READ AND CHECK ADAL REGISTER
12480  033042  001405                           BEQ     27$                     ;IF LOADED OK THEN CONTINUE
12481  033044                                   ERRDF   3,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
12482  033044  104455                           TRAP    C$ERDF
12483  033046  000003                           .WORD   3
12484  033050  002513                           .WORD   ADALRG
12485  033052  004770                           .WORD   R2EROR
12486  033054                                   CKLOOP
12487  033054  104406                           TRAP    C$CLP1
12488
12489                                           ;SET THE SIGNALS XRAS H AND XRAS L TO THE LOW AND HIGH STATE RESPECTIVELY
12490                                           ;BY CLEARING HDAL12 H.
12491
12492  033056  004737  007336          27$:    JSR     PC,XRASL                ;SET XRAS H LOW AND XRAS L HIGH
12493
12494                                           ;SET THE SIGNAL INTER L TO THE LOW STATE BY SETTING XSEL1 L TO THE
12495                                           ;LOW STATE.  XSEL1 L IS SET LOW BY SETTING HDAL6 H TO A ONE
12496
12497  033062  052737  000100  002342           BIS     #HDAL6,R6LOAD           ;SETUP BIT TO BE LOADED
12498  033070  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
12499  033074  001405                           BEQ     28$                     ;IF OK THEN CONTINUE
12500  033076                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
12501  033076  104455                           TRAP    C$ERDF
12502  033100  000004                           .WORD   4
12503  033102  002605                           .WORD   HDALRG
12504  033104  005020                           .WORD   R06ERR
12505  033106                                   CKLOOP
12506  033106  104406                           TRAP    C$CLP1
12507
12508                                           ;SET THE SIGNAL XRAS H AND XRAS L TO THE HIGH AND LOW STATE RESPECTIVELY
12509                                           ;BY SETTING HDAL 12 H TO A ONE.  WHEN XRAS L IS SET LOW, THE REFR FLIP-
12510                                           ;FLOP WILL BE CLOCKED TO A ZERO AS A RESULT OF INTER L BEING ASSERTED
12511                                           ;LOW.  WHEN REFR FLIP-FLOP IS A ZERO, THE SIGNAL REFR L WILL BE ASSERTED
12512                                           ;TO THE HIGH STATE.
12513
12514  033110  004737  007304          28$:    JSR     PC,XRASH                ;SET XRAS H AND XRAS L LOW
12515
12516                                           ;CHECK THE SIGNAL BTS1 H TO BE A ONE AS A RESULT OF THE BTFET FLIP-FLOP
12517                                           ;BEING CLEARED AND THE SIGNAL INTER L BEING ASSERTED TO THE LOW STATE.
```

```
12518                                                   ;
12519                                                   ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE SET TO A ZERO AS A
12520                                                   ;RESULT OF THE FOLLOWING SIGNALS BEING SET AS LISTED
12521                                                   ;       INTER L  -  LOW
12522                                                   ;       REFR L   -  HIGH
12523                                                   ;       XRAS H   -  HIGH
12524                                                   ;       XCAS L   -  HIGH
12525                                                   ;       ENEDC H  -  HIGH
12526                                                   ;       PSM L    -  HIGH
12527                                                   ;       SOP L    -  HIGH
12528
12529  033114  052737  000040  002336          BIS     #VDAL5,R4GOOD           ;EXPECT BTS1 H TO BE A 1 VIA INTER L
12530  033122  042737  000020  002336          BIC     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ZERO
12531  033130  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12532  033134  001405                          BEQ     29$                     ;IF OK THEN CONTINUE
12533  033136                                  ERRDF   3,VDALRG,R4EROR         ;REFR F/F PROBABLY NOT A ZERO
12534  033136  104455                          TRAP    C$ERDF
12535  033140  000003                          .WORD   3
12536  033142  002537                          .WORD   VDALRG
12537  033144  005004                          .WORD   R4EROR
12538  033146                                  CKLOOP
12539  033146  104406                          TRAP    C$CLP1
12540
12541                                                   ;SET THE SIGNAL INTER L BACK TO THE HIGH STATE BY SETTING XSEL1 L
12542                                                   ;BACK TO THE HIGH STATE BY SETTING HDAL6 H TO A ZERO.
12543
12544  033150  042737  000100  002342  29$:     BIC     #HDAL6,R6LOAD           ;SET XSEL1 L TO THE LOW STATE
12545  033156  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
12546  033162  001405                          BEQ     30$                     ;IF OK THEN CONTINUE
12547  033164                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
12548  033164  104455                          TRAP    C$ERDF
12549  033166  000004                          .WORD   4
12550  033170  002605                          .WORD   HDALRG
12551  033172  005020                          .WORD   R06ERR
12552  033174                                  CKLOOP
12553  033174  104406                          TRAP    C$CLP1
12554
12555                                                   ;CHECK THE SIGNAL BTS1 H TO BE A ZERO AS A RESULT OF THE BTFET FLIP-FLOP
12556                                                   ;BEING CLEARED AND THE SIGNAL INTER L BEING SET TO THE HIGH STATE.
12557                                                   ;
12558                                                   ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ONE AS A RESULT OF
12559                                                   ;THE FOLLOWING SIGNALS BEING SET AS LISTED
12560                                                   ;       INTER L  -  HIGH
12561                                                   ;       REFR L   -  HIGH
12562                                                   ;       XRAS H   -  HIGH
12563                                                   ;       XCAS L   -  HIGH
12564                                                   ;       ENEDC H  -  HIGH
12565                                                   ;       PSM L    -  HIGH
12566                                                   ;       SOP L    -  HIGH
12567
12568  033176  042737  000040  002336  30$:     BIC     #VDAL5,R4GOOD           ;EXPECT BTS1 H TO BE A 0 VIA INTER L
12569  033204  052737  000020  002336          BIS     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ONE
12570  033212  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12571  033216  001405                          BEQ     31$                     ;IF OK THEN CONTINUE
12572  033220                                  ERRDF   3,VDALRG,R4EROR         ;EDEOC H NOT SET TO A ONE
12573  033220  104455                          TRAP    C$ERDF
```

```
12574  033222  000003                          .WORD   3
12575  033224  002537                          .WORD   VDALRG
12576  033226  005004                          .WORD   R4EROR
12577  033230                                  CKLOOP
12578  033230  104406                          TRAP    C$CLP1
12579
12580                                          ;SET THE SIGNALS XRAS H AND XRAS L TO THE LOW AND HIGH STATE RESPECTIVELY
12581                                          ;BY CLEARING HDAL12 H.
12582
12583  033232  004737  007336        31$:    JSR     PC,XRASL                ;SET XRAS H LOW AND XRAS L HIGH
12584
12585                                          ;SET ADAL7 H AND ADAL4 H TO ZEROES IN THE ADAL REGISTER.  ADAL7 H ON
12586                                          ;A ZERO WILL HOLD THE REFR FLIP-FLOP IN THE CLEARED STATE, THUS
12587                                          ;CAUSING THE SIGNAL REFR L TO REMAIN HIGH.  ADAL4 H ON A ZERO WILL
12588                                          ;ALLOW THE PAUSE MODE FLIP-FLOP TO BE CLOCKED TO THE PAUSE MODE WHEN
12589                                          ;A PULSE IS ISSUED ON THE SIGNAL XRAS H.
12590
12591  033236  042737  000220  002330          BIC     #ADAL7!ADAL4,R2LOAD     ;SETUP BITS TO BE CLEARED
12592  033244  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
12593  033250  001405                          BEQ     32$                     ;IF LOADED OK THEN CONTINUE
12594  033252                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
12595  033252  104455                          TRAP    C$ERDF
12596  033254  000002                          .WORD   2
12597  033256  002513                          .WORD   ADALRG
12598  033260  004770                          .WORD   R2EROR
12599  033262                                  CKLOOP
12600  033262  104406                          TRAP    C$CLP1
12601
12602                                          ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  WHEN
12603                                          ;XRAS H IS PULSED AND ADAL4 H IS SET TO A ZERO, THE PAUSE MODE FLIP-
12604                                          ;FLOP WILL BE CLOCKED TO A ZERO, THUS SETTING THE SIGNAL PAUSE L TO
12605                                          ;THE HIGH STATE.  WHEN PAUSE L IS ASSERTED HIGH, THE SIGNAL SOP L
12606                                          ;WILL BE ASSERTED LOW, THUS SETTING THE SIGNAL EDEOC H TO THE LOW
12607                                          ;STATE.
12608
12609  033264  004737  007272        32$:    JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
12610
12611                                          ;READ THE VDAL REGISTER AND CHECK EDEOC H TO BE A ZERO AS A RESULT
12612                                          ;OF THE FOLLOWING SIGNALS BEING SET AS LISTED
12613                                          ;       INTER L   -  HIGH
12614                                          ;       REFR L    -  HIGH
12615                                          ;       XRAS H    -  LOW
12616                                          ;       XCAS L    -  HIGH
12617                                          ;       ENEDC H   -  HIGH
12618                                          ;       PSM L     -  HIGH
12619                                          ;       SOP L     -  LOW
12620
12621  033270  042737  000020  002336          BIC     #VDAL4,R4GOOD           ;EXPECT EDEOC H TO BE A ZERO
12622  033276  004737  006654                  JSR     PC,READR4               ;READ VDAL AND PAUSE STATE MACHINE
12623  033302  001405                          BEQ     33$                     ;IF OK THEN CONTINUE
12624  033304                                  ERRDF   3,VDALRG,R4EROR         ;EDEOC H NOT 0 VIA SOP L SET LOW
12625  033304  104455                          TRAP    C$ERDF
12626  033306  000003                          .WORD   3
12627  033310  002537                          .WORD   VDALRG
12628  033312  005004                          .WORD   R4EROR
12629  033314                                  CKLOOP
```

```
12630  033314  104406                          TRAP    C$CLP1
12631
12632                                          ;RESET ALL FLIP-FLOPS BY PULSING INVD L VIA VDAL2 H
12633
12634  033316  005037  002334          33$:    CLR     R4LOAD                  ;SETUP TO CLEAR ALL BITS
12635  033322  004737  007712                  JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
12636
12637  033326                                  ENDSEG
12638  033326                          10000$:
12639  033326  104405                          TRAP    C$ESEG
12640  033330                                  ENDTST
12641  033330                          L10074:
12642  033330  104401                          TRAP    C$ETST
12643
```

```
12644                                   .SBTTL  TEST 43: TARGET EMULATOR INTERRUPT LOGIC TEST
12645
12646                                   ;++
12647                                   ; THIS TEST WILL CHECK THE TARGET EMULATOR'S INTERRUPT LOGIC USING THE SIGNALS
12648                                   ; TOBRK H AND BRK H TO CAUSE INTERRUPT REQUESTS.  THE TEST WILL CHECK THAT NO
12649                                   ; INTERRUPTS OCCUR WHEN THE INTERRUPT ENABLE BIT IS CLEARED AND THE INTERRUPT
12650                                   ; REQUEST SIGNAL IS ASSERTED HIGH.  THE TEST WILL CHECK THAT AN INTERRUPT WILL
12651                                   ; OCCUR WHEN THE INTERRUPT ENABLE BIT IS SET AND THE SIGNAL TOBRK H IS ASSERTED
12652                                   ; HIGH.  THE TEST WILL CHECK THAT THE BREAK LATCH FLIP-FLOP CAN BE SET, CLEARED,
12653                                   ; AND THAT IT CAN CAUSE AN INTERRUPT.
12654                                   ;--
12655
12656  033332                                   BGNTST
12657  033332                           T43::
12658  033332  004737  005510                   JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
12659
12660  033336                                   BGNSEG
12661  033336  104404                           TRAP    C$BSEG
12662
12663                                           ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE ANY INTERRUPTS FROM
12664                                           ;OCCURING.
12665
12666  033340                                   SETPRI  #PRI07                  ;RAISE THE CPU PRIORITY LEVEL TO 7
12667  033340  012700  000340                   MOV     #PRI07,R0
12668  033344  104441                           TRAP    C$SPRI
12669
12670                                           ;SELECT HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
12671
12672  033346  004737  006754                   JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
12673
12674                                           ;SET HDAL REGISTER BIT 2 TO A ONE AND ALL OTHER HDAL REGISTER BITS TO
12675                                           ;ZEROES.  HDAL2 H ON A ONE WILL ALLOW THE PROGRAM TO GENERATE THE T-11
12676                                           ;TIMING AND CONTROL SIGNALS.
12677
12678  033352  012737  000004  002342           MOV     #HDAL2,R6LOAD           ;SETUP BITS TO BE LOADED
12679  033360  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
12680  033364  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
12681  033366                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
12682  033366  104455                           TRAP    C$ERDF
12683  033370  000004                           .WORD   4
12684  033372  002605                           .WORD   HDALRG
12685  033374  005020                           .WORD   R06ERR
12686  033376                                   CKLOOP
12687  033376  104406                           TRAP    C$CLP1
12688
12689                                           ;CLEAR ALL ADAL REGISTER BITS.  TOGGLE THE SIGNAL BRKRES L BY SETTING
12690                                           ;AND CLEARING ADAL REGISTER BIT 0.  THE SIGNAL BRKRES L WILL CLEAR THE
12691                                           ;SINGLE STEP BREAK FLIP-FLOP, THE MEMORY SIMULATOR BREAK FLIP-FLOP, AND
12692                                           ;THE BREAK LATCH FLIP-FLOP.
12693
12694  033400  005037  002330           1$:     CLR     R2LOAD                  ;SETUP TO CLEAR ALL ADAL BITS
12695  033404  004737  007772                   JSR     PC,BRKRES               ;GO PULSE BRKRES L VIA ADAL REG BIT 0
12696
12697                                           ;TOGGLE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL REGISTER BIT 2.
12698                                           ;ALL OTHER VDAL READ/WRITE BITS WILL BE CLEARED AND THE READ ONLY BITS
12699                                           ;WILL BE CHECKED TO BE ZERO. THE SIGNAL INVD L WILL SET ALL THE FLIP-
```

```
12700                                   ;FLOPS ON THE MODULE, NOT CLEARED BY BRKRES L, TO A KNOWN STATE.
12701                                   ;A PULSE ON THE SIGNAL INVD L WILL ALSO CLEAR THE TIMEOUT BREAK ONE-
12702                                   ;SHOT, THUS SETTING ITS OUTPUT TO THE HIGH STATE.
12703
12704  033410  005037  002334           CLR     R4LOAD                  ;SETUP TO CLEAR ALL VDAL BITS
12705  033414  004737  007712           JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
12706
12707                                   ;SET INTERRUPT VECTOR TO VECTOR SPECIFIED BY USER AT PROGRAM START TIME.
12708                                   ;THE CPU PRIORITY LEVEL WILL BE RESET TO PRIORITY LEVEL 7 WHEN AN
12709                                   ;INTERRUPT OCCURS.
12710
12711  033420                           SETVEC  TEVECT,#INTSRV,#PRI07
12712  033420  012746  000340           MOV     #PRI07,-(SP)
12713  033424  012746  006724           MOV     #INTSRV,-(SP)
12714  033430  013746  002312           MOV     TEVECT,-(SP)
12715  033434  012746  000003           MOV     #3,-(SP)
12716  033440  104437                   TRAP    C$SVEC
12717  033442  062706  000010           ADD     #10,SP
12718  033446  005002                   CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
12719
12720                                   ;SET CPU PRIORITY LEVEL TO ZERO.  THIS WILL ALLOW AN INTERRUPT TO OCCUR
12721                                   ;WHEN THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET AND A BREAK CONDI-
12722                                   ;TION IS GENERATED.
12723
12724  033450                           SETPRI  #PRI00                  ;LOWER CPU PRIORITY LEVEL TO ZERO
12725  033450  012700  000000           MOV     #PRI00,R0
12726  033454  104441                   TRAP    C$SPRI
12727
12728                                   ;ISSUE A DUMMY INSTRUCTION HERE TO CHECK THAT NO INTERRUPT OCCURED
12729
12730  033456  000240                   NOP
12731
12732                                   ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT
12733                                   ;ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT IS CLEARED, AND NO
12734                                   ;BREAK CONDITION IS BEING GENERATED.
12735
12736  033460  005702                   TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
12737  033462  001406                   BEQ     2$                      ;IF NO INTERRUPT THEN CONTINUE
12738  033464                           ERRDF   1,UNEXIN,ROEROR         ;INTERRUPTED WITH INT ENA + BRK H A 0
12739  033464  104455                   TRAP    C$ERDF
12740  033466  000001                   .WORD   1
12741  033470  002432                   .WORD   UNEXIN
12742  033472  004754                   .WORD   ROEROR
12743  033474  005002                   CLR     R2                      ;CLEAR SOFTWARE INTERUPT FLAG
12744  033476                           CKLOOP
12745  033476  104406                   TRAP    C$CLP1
12746
12747                                   ;SET TARGET EMULATOR INTERRUPT ENABLE BIT TO A ONE BY SETTING GDAL
12748                                   ;REGISTER BIT 3 TO A ONE.  NO INTERRUPT SHOULD OCCUR AT THIS POINT IN
12749                                   ;TIME.
12750
12751  033500  052737  000010  002320  2$:     BIS     #GDAL3,ROLOAD           ;SETUP BIT TO BE LOADED
12752  033506  004737  006554                   JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
12753  033512  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
12754  033514                                   ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
12755  033514  104455                           TRAP    C$ERDF
```

```
12756  033516  000001                  .WORD   1
12757  033520  002406                  .WORD   GDALRG
12758  033522  004754                  .WORD   ROEROR
12759  033524                          CKLOOP
12760  033524  104406                  TRAP    C$CLP1
12761
12762                                  ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT
12763                                  ;ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, AND
12764                                  ;NO BREAK CONDITION IS BEING GENERATED BY THE PROGRAM.
12765
12766  033526  005702          3$:     TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
12767  033530  001406                  BEQ     4$                      ;IF NO INTERRUPT THEN CONTINUE
12768  033532                          ERRDF   1,UNEXIN,ROEROR         ;INTERRUPT WITH INT ENA A 1 + BRK H A 0
12769  033532  104455                  TRAP    C$ERDF
12770  033534  000001                  .WORD   1
12771  033536  002432                  .WORD   UNEXIN
12772  033540  004754                  .WORD   ROEROR
12773  033542  005002                  CLR     R2                      ;RESET SOFTWARE INTERRUPT FLAG
12774  033544                          CKLOOP
12775  033544  104406                  TRAP    C$CLP1
12776
12777                                  ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  THIS IS
12778                                  ;DONE TO CHECK THAT THE BREAK INTERRUPT LATCH FLIP-FLOP IS CLOCKED
12779                                  ;TO A ZERO WHEN THE SIGNAL BRK H IS ASSERTED LOW.
12780
12781  033546  004737  007272  4$:     JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
12782
12783                                  ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT
12784                                  ;ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, THE
12785                                  ;BREAK LATCH FLIP-FLOP IS CLEARED, AND NO BREAK CONDITION IS BEING
12786                                  ;GENERATED BY THE PROGRAM.
12787
12788  033552  005702                  TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
12789  033554  001406                  BEQ     5$                      ;IF NO INTERRUPT THEN CONTINUE
12790  033556                          ERRDF   1,UNEXIN,ROEROR         ;CHECK BREAK LATCH FLIP-FLOP TO BE A 0
12791  033556  104455                  TRAP    C$ERDF
12792  033560  000001                  .WORD   1
12793  033562  002432                  .WORD   UNEXIN
12794  033564  004754                  .WORD   ROEROR
12795  033566  005002                  CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
12796  033570                          CKLOOP
12797  033570  104406                  TRAP    C$CLP1
12798
12799                                  ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE ANY INTERRUPTS FROM
12800                                  ;OCCURING.
12801
12802  033572                  5$:     SETPRI  #PRIO7                  ;DISABLE INTERRUPTS
12803  033572  012700  000340          MOV     #PRIO7,R0
12804  033576  104441                  TRAP    C$SPRI
12805
12806                                  ;SET ADAL REGISTER BIT 8 TO A ONE TO ENABLE THE TIMEOUT BREAK ONE SHOTS
12807                                  ;OUTPUT TO THE GDAL REGISTER AND TO THE SIGNAL BRK H.  THE TIMEOUT
12808                                  ;BREAK ONE SHOT HAS NOT BEEN FIRED, THEREFORE, THE SIGNALS TOBRK H AND
12809                                  ;BRK H SHOULD BE ASSERTED HIGH TO INDICATE A BREAK CONDITION.  AN
12810                                  ;INTERRUPT WILL BE GENERATED BY THE SIGNAL TOBRK H AS SOON AS THE PROGRAM
12811                                  ;LOWERS THE CPU PRIORITY LEVEL TO ZERO.
```

```
12812
12813  033600  052737  000400  002330          BIS     #ADAL8,R2LOAD           ;SETUP BIT TO ENABLE TOBRK H OUTPUT
12814  033606  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
12815  033612  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
12816  033614                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
12817  033614  104455                          TRAP    C$ERDF
12818  033616  000002                          .WORD   2
12819  033620  002513                          .WORD   ADALRG
12820  033622  004770                          .WORD   R2EROR
12821  033624                                  CKLOOP
12822  033624  104406                          TRAP    C$CLP1
12823
12824                                          ;READ THE GDAL REGISTER TO CHECK THAT THE TOBRK H BIT IS SET TO A ONE
12825                                          ;AS A RESULT OF ADAL8 H BEING ASSERTED HIGH AND TIMEOUT BREAK ONE SHOT
12826                                          ;NOT BEING IN THE FIRED STATE.
12827
12828  033626  052737  000100  002322  6$:     BIS     #TOBRK,ROGOOD           ;EXPECT TOBRK H TO BE A ONE
12829  033634  004737  006570                  JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
12830  033640  001405                          BEQ     7$                      ;IF OK THEN CONTINUE
12831  033642                                  ERRDF   1,GDALRG,ROEROR         ;TOBRK H PROBABLY NOT SET TO A ONE
12832  033642  104455                          TRAP    C$ERDF
12833  033644  000001                          .WORD   1
12834  033646  002406                          .WORD   GDALRG
12835  033650  004754                          .WORD   ROEROR
12836  033652                                  CKLOOP
12837  033652  104406                          TRAP    C$CLP1
12838
12839                                          ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT 7,
12840                                          ;THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, AND THE
12841                                          ;SIGNAL TOBRK H IS ASSERTED HIGH
12842
12843  033654  005702                  7$:     TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
12844  033656  001406                          BEQ     8$                      ;IF NO INTERRUPT THEN CONTINUE
12845  033660                                  ERRDF   1,UNEXIN,ROEROR         ;INTERRUPT WITH CPU PRIORITY LEVEL - 7
12846  033660  104455                          TRAP    C$ERDF
12847  033662  000001                          .WORD   1
12848  033664  002432                          .WORD   UNEXIN
12849  033666  004754                          .WORD   ROEROR
12850  033670  005002                          CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
12851  033672                                  CKLOOP
12852  033672  104406                          TRAP    C$CLP1
12853
12854                                          ;LOWER THE CPU PRIORITY LEVEL TO ZERO. AN INTERRUPT SHOULD OCCUR AS A
12855                                          ;RESULT OF TOBRK H BEING ASSERTED HIGH AND THE TARGET EMULATOR INTER-
12856                                          ;RUPT ENABLE BIT BEING SET TO A ONE.
12857
12858  033674                          8$:     SETPRI  #PRI00                  ;ENABLE INTERRUPTS TO OCCUR
12859  033674  012700  000000                  MOV     #PRI00,R0
12860  033700  104441                          TRAP    C$SPRI
12861
12862                                          ;CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE CPU PRIORITY LEVEL
12863                                          ;BEING SET TO ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT BEING SET
12864                                          ;TO A ONE, AND THE SIGNAL TOBRK H BEING ASSERTED HIGH.
12865
12866  033702  000240                          NOP                             ;DO A DUMMY INSTRUCTION TO ALLOW INTERRUPTS
12867  033704  005702                          TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
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```
12868  033706  001005                          BNE     9$                      ;IF INTERRUPTED THEN CONTINUE
12869  033710                                  ERRDF   1,NOINT,ROEROR          ;FAILED TO INTERRUPT
12870  033710  104455                          TRAP    C$ERDF
12871  033712  000001                          .WORD   1
12872  033714  002467                          .WORD   NOINT
12873  033716  004754                          .WORD   ROEROR
12874  033720                                  CKLOOP
12875  033720  104406                          TRAP    C$CLP1
12876
12877                                          ;AT THIS POINT IN TIME THE CPU PRIORITY LEVEL IS AT 7 AS A REUSLT OF
12878                                          ;AN INTERRUPT.  CHECK THE PREVIOUS GDAL REGISTER AGAINST THE GDAL
12879                                          ;REGISTER READ IN THE INTERRUPT SERVICE ROUTINE.
12880
12881  033722  005002                  9$:     CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
12882  033724  023737  002322  002326          CMP     ROGOOD,ROBAD            ;CHECK EXPECTED AGAINST READ FROM INTERRUPT
12883  033732  001405                          BEQ     10$                     ;IF OK THEN CONTINUE
12884  033734                                  ERRDF   1,GDALRG,ROEROR         ;GDAL CHANGED AFTER AN INTERRUPT OCCURED
12885  033734  104455                          TRAP    C$ERDF
12886  033736  000001                          .WORD   1
12887  033740  002406                          .WORD   GDALRG
12888  033742  004754                          .WORD   ROEROR
12889  033744                                  CKLOOP
12890  033744  104406                          TRAP    C$CLP1
12891
12892                                          ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  THE SIGNAL
12893                                          ;XRAS H SHOULD CLOCK THE BREAK LATCH FLIP-FLOP TO A ONE AS A RESULT OF
12894                                          ;THE SIGNAL BRK H BEING ASSERTED HIGH.  THE SIGNAL BRK H IS ASSERTED
12895                                          ;HIGH AS A RESULT OF THE SIGNAL TOBRK H BEING ASSERTED HIGH.
12896
12897  033746  004737  007272          10$:    JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
12898
12899                                          ;SET THE SIGNAL TOBRK H TO THE LOW STATE BY SETTING ADAL8 H TO A ZERO.
12900
12901  033752  042737  000400  002330          BIC     #ADAL8,R2LOAD           ;SETUP TO SET TOBRK H TO LOW STATE
12902  033760  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
12903  033764  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
12904  033766                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
12905  033766  104455                          TRAP    C$ERDF
12906  033770  000002                          .WORD   2
12907  033772  002513                          .WORD   ADALRG
12908  033774  004770                          .WORD   R2EROR
12909  033776                                  CKLOOP
12910  033776  104406                          TRAP    C$CLP1
12911
12912                                          ;READ GDAL REGISTER TO CHECK THAT THE SIGNAL TOBRK H IS A ZERO AS A
12913                                          ;RESULT OF ADAL8 H BEING SET TO A ZERO.
12914
12915  034000  042737  000100  002322  11$:     BIC     #TOBRK,ROGOOD           ;EXPECT TOBRK H TO BE A ZERO
12916  034006  004737  006570                  JSR     PC,READRO               ;READ AND CHECK GDAL REGISTER
12917  034012  001405                          BEQ     12$                     ;IF OK THEN CONTINUE
12918  034014                                  ERRDF   1,GDALRG,ROEROR         ;TOBRK H PROBABLY NOT A ZERO
12919  034014  104455                          TRAP    C$ERDF
12920  034016  000001                          .WORD   1
12921  034020  002406                          .WORD   GDALRG
12922  034022  004754                          .WORD   ROEROR
12923  034024                                  CKLOOP
```

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12924  034024  104406                          TRAP    C$CLP1
12925
12926                                          ;AT THIS POINT IN TIME THE BREAK LATCH FLIP-FLOP SHOULD BE SET TO A ONE
12927                                          ;AND THE SIGNALS TOBRK H AND BRK H SHOULD BE ASSERTED LOW.  THE PROGRAM
12928                                          ;WILL NOW LOWER THE CPU PRIORITY LEVEL TO ZERO.  NO INTERRUPT SHOULD
12929                                          ;OCCUR BECAUSE NEITHER THE REQUEST, ALTHOUGH HIGH, OR THE TARGET EMULATOR
12930                                          ;INTERRUPT ENABLE BIT HAS CHANGED STATE TO CLOCK THE DC003'S INTERRUPT
12931                                          ;REQUEST FLIP-FLOP.
12932
12933  034026                          12$:    SETPRI  #PRI00                  ;LOWER PRIORITY TO ENABLE INTERRUPTS
12934  034026  012700  000000                 MOV     #PRI00,R0
12935  034032  104441                         TRAP    C$SPRI
12936
12937                                          ;CHECK THAT NO INTERRUPT OCCURED AS A RESULT OF THE CPU PRIORITY LEVEL
12938                                          ;BEING AT 0, THE TARGET EMULATOR INTERRUPT ENABLE BIT BEING SET, AND
12939                                          ;THE BREAK LATCH FLIP-FLOP BEING SET TO A ONE.  NO INTERRUPT SHOULD
12940                                          ;OCCUR UNTIL EITHER THE REQUEST OR THE INTERRUPT ENABLE BIT HAS
12941                                          ;TOGGLED.
12942
12943  034034  000240                         NOP                             ;SHOULD NOT INTERRUPT HERE
12944  034036  005702                         TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
12945  034040  001406                         BEQ     13$                     ;IF NO INTERRUPT THEN CONTINUE
12946  034042                                 ERRDF   1,UNEXIN,R0EROR         ;INTERRUPTED W/O TOGGLING I.E. OR RQSTA H
12947  034042  104455                         TRAP    C$ERDF
12948  034044  000001                         .WORD   1
12949  034046  002432                         .WORD   UNEXIN
12950  034050  004754                         .WORD   R0EROR
12951  034052  005002                         CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
12952  034054                                 CKLOOP
12953  034054  104406                         TRAP    C$CLP1
12954
12955                                          ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE INTERRUPTS FROM OCCURING.
12956
12957  034056                          13$:    SETPRI  #PRI07                  ;DISABLE INTERRUPTS FROM OCCURING
12958  034056  012700  000340                 MOV     #PRI07,R0
12959  034062  104441                         TRAP    C$SPRI
12960
12961                                          ;TO CHECK THAT THE BREAK LATCH FLIP-FLOP IS SET TO A ONE, THE PROGRAM
12962                                          ;MUST CLEAR AND SET THE TARGET EMULATORS INTERRUPT ENABLE BIT TO CLOCK
12963                                          ;THE INTERRUPT REQUEST INTO THE DC003'S INTERRUPT REQUEST FLIP-FLOP.
12964
12965  034064  042737  000010  002320          BIC     #GDAL3,R0LOAD           ;SETUP TO CLEAR I.E. BIT
12966  034072  004737  006554                 JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK GDAL REGISTER
12967  034076  001405                         BEQ     14$                     ;IF LOADED OK THEN CONTINUE
12968  034100                                 ERRDF   1,GDALRG,R0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
12969  034100  104455                         TRAP    C$ERDF
12970  034102  000001                         .WORD   1
12971  034104  002406                         .WORD   GDALRG
12972  034106  004754                         .WORD   R0EROR
12973  034110                                 CKLOOP
12974  034110  104406                         TRAP    C$CLP1
12975  034112  052737  000010  002320  14$:   BIS     #GDAL3,R0LOAD           ;SETUP TO SET I.E. BIT TO A 1
12976  034120  004737  006554                 JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK GDAL REGISTER
12977  034124  001405                         BEQ     15$                     ;IF LOADED OK THEN CONTINUE
12978  034126                                 ERRDF   1,GDALRG,R0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
12979  034126  104455                         TRAP    C$ERDF
```

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12980  034130  000001                          .WORD   1
12981  034132  002406                          .WORD   GDALRG
12982  034134  004754                          .WORD   ROEROR
12983  034136                                  CKLOOP
12984  034136  104406                          TRAP    C$CLP1
12985
12986                                          ;AT THIS POINT IN TIME THE BREAK LATCH FLIP-FLOP SHOULD BE SET TO A
12987                                          ;ONE AND THE SIGNALS TOBRK H AND BRK H SHOULD BE ASSERTED LOW.  THE
12988                                          ;DC003'S INTERRUPT REQUEST FLIP-FLOP SHOULD BE SET TO A ONE AS A
12989                                          ;RESULT OF THE INTERRUPT ENABLE BIT BEING CLEARED AND SET AND THE
12990                                          ;BREAK LATCH FLIP-FLOP BEING SET TO A ONE.  THE PROGRAM WILL NOW LOWER
12991                                          ;THE CPU PRIORITY LEVEL TO ZERO AND EXPECT AN INTERRUPT TO OCCUR AS A
12992                                          ;RESULT OF THE BREAK LATCH FLIP-FLOP BEING SET.
12993
12994  034140                          15$:    SETPRI  #PR100                  ;ALLOW INTERURPTS TO OCCUR
12995  034140  012700  000000                 MOV     #PR100,R0
12996  034144  104441                         TRAP    C$SPRI
12997
12998                                          ;CHECK THAT AN INTERRUPT OCCURED AS A RESULT OF THE CPU PRIORITY LEVEL
12999                                          ;BEING AT ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT BEING SET, AND
13000                                          ;THE BREAK LATCH FLIP-FLOP BEING SET TO A ONE.
13001
13002  034146  000240                         NOP                             ;SHOULD INTERRUPT HERE
13003  034150  005702                         TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
13004  034152  001005                         BNE     16$                     ;IF INTERRUPTED THEN CONTINUE
13005  034154                                  ERRDF   1,NOINT,ROEROR          ;BREAK F/F FAILED TO SET OR CAUSE INTERRUPT
13006  034154  104455                         TRAP    C$ERDF
13007  034156  000001                         .WORD   1
13008  034160  002467                         .WORD   NOINT
13009  034162  004754                         .WORD   ROEROR
13010  034164                                  CKLOOP
13011  034164  104406                         TRAP    C$CLP1
13012
13013                                          ;AT THIS POINT IN TIME, THE CPU PRIORITY LEVEL IS AT 7 AS A RESULT OF
13014                                          ;THE INTERRUPT.  CHECK THE PREVIOUS EXPECTED GDAL REGISTER AGAINST THE
13015                                          ;GDAL REGISTER READ IN THE INTERRUPT SERVICE ROUTINE.
13016
13017  034166  005002                  16$:    CLR     R2                      ;CLEAR THE SOFTWARE INTERRUPT FLAG
13018  034170  023737  002322  002326         CMP     ROGOOD,ROBAD            ;CHECK EXPECTED AGAINST READ VIA INTERRUPT
13019  034176  001405                         BEQ     17$                     ;IF OK THEN CONTINUE
13020  034200                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL TO EXPECTED
13021  034200  104455                         TRAP    C$ERDF
13022  034202  000001                         .WORD   1
13023  034204  002406                         .WORD   GDALRG
13024  034206  004754                         .WORD   ROEROR
13025  034210                                  CKLOOP
13026  034210  104406                         TRAP    C$CLP1
13027
13028                                          ;AS RESULT OF THE INTERRUPT, THE BREAK LATCH FLIP-FLOP SHOULD HAVE BEEN
13029                                          ;CLEARED BY THE SIGNAL VECTOR H.  TO TEST THAT THIS HAPPENED, THE
13030                                          ;PROGRAM MUST CLEAR AND SET THE TARGET EMULATORS INTERRUPT ENABLE BIT
13031                                          ;TO CLOCK THE LEVEL OF THE INTERRUPT REQUEST, WHICH SHOULD BE LOW, INTO
13032                                          ;THE DC003'S INTERRUPT REQUEST FLIP-FLOP, THUS CAUSING THE DC003'S
13033                                          ;INTERRUPT REQUEST FLIP-FLOP TO BE CLOCKED TO A ZERO.
13034
13035  034212  042737  000010  002320  17$:    BIC     #GDAL3,ROLOAD           ;SETUP TO CLEAR INTERRUPT ENABLE
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13036  034220  004737  006554                    JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK INT ENA
13037  034224  001405                            BEQ     18$                     ;IF LOADED OK THEN CONTINUE
13038  034226                                    ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
13039  034226  104455                            TRAP    C$ERDF
13040  034230  000001                            .WORD   1
13041  034232  002406                            .WORD   GDALRG
13042  034234  004754                            .WORD   ROEROR
13043  034236                                    CKLOOP
13044  034236  104406                            TRAP    C$CLP1
13045  034240  052737  000010  002320  18$:     BIS     #GDAL3,ROLOAD           ;SETUP TO SET INTERRUPT ENABLE
13046  034246  004737  006554                    JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK GDAL REGISTER
13047  034252  001405                            BEQ     19$                     ;IF LOADED OK THEN CONTINUE
13048  034254                                    ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL TO EXPECTED
13049  034254  104455                            TRAP    C$ERDF
13050  034256  000001                            .WORD   1
13051  034260  002406                            .WORD   GDALRG
13052  034262  004754                            .WORD   ROEROR
13053  034264                                    CKLOOP
13054  034264  104406                            TRAP    C$CLP1
13055
13056                                            ;AS A RESULT OF THE INTERRUPT, THE BREAK LATCH FLIP-FLOP SHOULD HAVE
13057                                            ;BEEN CLEARED BY THE SIGNAL VECTOR H.  THE TEST WILL NOW LOWER THE
13058                                            ;CPU PRIORITY LEVEL AND CHECK THAT NO INTERRUPT WILL OCCUR.
13059
13060  034266                            19$:     SETPRI  #PRI00                  ;ENABLE INTERRUPTS TO OCCUR
13061  034266  012700  000000                    MOV     #PRI00,R0
13062  034272  104441                            TRAP    C$SPRI
13063
13064                                            ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL IS AT ZERO,
13065                                            ;THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, THE SIGNAL
13066                                            ;TOBRK H IS ASSERTED LOW AND THE BREAK LATCH FLIP-FLOP IS CLEARED.
13067
13068  034274  000240                            NOP
13069  034276  005702                            TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
13070  034300  001406                            BEQ     20$                     ;IF NO INTERRUPT THEN CONTINUE
13071  034302                                    ERRDF   1,UNEXIN,ROEROR         ;BREAK LATCH F/F FAILED TO 0 VIA VECTOR H
13072  034302  104455                            TRAP    C$ERDF
13073  034304  000001                            .WORD   1
13074  034306  002432                            .WORD   UNEXIN
13075  034310  004754                            .WORD   ROEROR
13076  034312  005002                            CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
13077  034314                                    CKLOOP
13078  034314  104406                            TRAP    C$CLP1
13079
13080                                            ;SET THE TARGET EMULATOR INTERRUPT ENABLE BIT TO A ZERO.
13081
13082  034316  042737  000010  002320  20$:     BIC     #GDAL3,ROLOAD           ;SETUP TO CLEAR TE INT ENA BIT
13083  034324  004737  006554                    JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK GDAL REGISTER
13084  034330  001405                            BEQ     21$                     ;IF LOADED OK THEN CONTINUE
13085  034332                                    ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
13086  034332  104455                            TRAP    C$ERDF
13087  034334  000001                            .WORD   1
13088  034336  002406                            .WORD   GDALRG
13089  034340  004754                            .WORD   ROEROR
13090  034342                                    CKLOOP
13091  034342  104406                            TRAP    C$CLP1
```

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13092
13093                                           ;SET THE SIGNALS TOBRK H AND BRK H TO THE HIGH STATE BY SETTING ADAL8 H
13094                                           ;TO A ONE.  NO INTERRUPT SHOULD OCCUR AS A RESULT OF THE TARGET EMULATOR
13095                                           ;INTERRUPT ENABLE BIT BEING CLEARED
13096
13097  034344  052737  000400  002330  21$:    BIS     #ADAL8,R2LOAD           ;ENABLE TOBRK H AND BRK H TO HIGH STATE
13098  034352  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
13099  034356  001405                          BEQ     22$                     ;IF OK THEN CONTINUE
13100  034360                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL TO EXPECTED
13101  034360  104455                          TRAP    C$ERDF
13102  034362  000002                          .WORD   2
13103  034364  002513                          .WORD   ADALRG
13104  034366  004770                          .WORD   R2EROR
13105  034370                                  CKLOOP
13106  034370  104406                          TRAP    C$CLP1
13107
13108                                           ;CLOCK THE LEVEL OF BRK H, WHICH SHOULD BE ASSERTED HIGH VIA TOBRK H,
13109                                           ;INTO THE BREAK LATCH FLIP-FLOP, THUS SETTING THE BREAK LATCH FLIP-FLOP
13110                                           ;TO A ONE.  THE BREAK LATCH FLIP-FLOP WILL BE CLOCKED TO A ONE BY
13111                                           ;PULSING THE SIGNAL XRAS H VIA HDAL12 H.
13112
13113  034372  004737  007272          22$:    JSR     PC,XRAS                 ;GO PULSE XRAS H VIA HDAL12 H
13114
13115                                           ;CHECK THAT NO INTERRUPT OCCURED WHEN THE CPU PRIORITY LEVEL WAS AT 0,
13116                                           ;THE TARGET EMULATOR INTERRUPT ENABLE BIT IS CLEARED, THE TIMEOUT
13117                                           ;BREAK SIGNAL IS HIGH AND THE BREAK LATCH FLIP-FLOP IS SET TO A ONE.
13118
13119  034376  052737  000100  002322          BIS     #TOBRK,R0GOOD           ;EXPECT TOBRK H TO BE SET TO A ONE
13120  034404  005702                          TST     R2                      ;CHECK SOFTWARE INTERRUPT FLAG
13121  034406  001406                          BEQ     23$                     ;IF OK THEN CONTINUE
13122  034410                                  ERRDF   1,UNEXIN,R0EROR         ;INTERRUPTED WITH TE INT ENA CLEARED
13123  034410  104455                          TRAP    C$ERDF
13124  034412  000001                          .WORD   1
13125  034414  002432                          .WORD   UNEXIN
13126  034416  004754                          .WORD   R0EROR
13127  034420  005002                          CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
13128  034422                                  CKLOOP
13129  034422  104406                          TRAP    C$CLP1
13130
13131                                           ;SET THE SIGNAL TOBRK H TO THE LOW STATE BY CLEARING ADAL8 H AND PULSE
13132                                           ;THE SIGNAL BRKRES L BY SETTING AND CLEARING THE SIGNAL ADAL0 H. A PULSE
13133                                           ;ON THE SIGNAL BRKRES L WILL CLEAR THE BREAK LATCH FLIP-FLOP.
13134
13135  034424  005037  002330          23$:    CLR     R2LOAD                  ;SETUP TO CLEAR ADAL8 H (TOBRK H - 0)
13136  034430  004737  007772                  JSR     PC,BRKRES               ;GO PULSE BRKRES L VIA ADAL0 H
13137  034434  042737  000100  002322          BIC     #TOBRK,R0GOOD           ;EXPECT TOBRK H TO BE A 0
13138
13139                                           ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE INTERRUPTS
13140
13141  034442                                  SETPRI  #PRI07
13142  034442  012700  000340                  MOV     #PRI07,R0
13143  034446  104441                          TRAP    C$SPRI
13144
13145                                           ;SET THE TARGET EMULATOR INTERRUPT ENABLE BIT TO A ONE BY SETTING
13146                                           ;GDAL REGISTER BIT 3 TO A ONE
13147
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13148  034450  052737  000010  002320          BIS     #GDAL3,ROLOAD           ;SETUP BIT TO BE LOADED
13149  034456  004737  006554                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK GDAL REGISTER
13150  034462  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
13151  034464                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL TO EXPECTED
13152  034464  104455                          TRAP    C$ERDF
13153  034466  000001                          .WORD   1
13154  034470  002406                          .WORD   GDALRG
13155  034472  004754                          .WORD   ROEROR
13156  034474                                  CKLOOP
13157  034474  104406                          TRAP    C$CLP1
13158
13159                                          ;LOWER THE CPU PRIORITY BACK TO ZERO TO ALLOW INTERRUPTS TO OCCUR.
13160                                          ;NO INTERRUPTS SHOULD OCCUR BECAUSE THE BREAK LATCH FLIP-FLOP
13161                                          ;SHOULD HAVE BEEN CLEARED BY THE SIGNAL BRKRES L ABOVE.
13162
13163  034476                          24$:    SETPRI  #PRI00                  ;LOWER THE CPU PRIORITY LEVEL TO 0
13164  034476  012700  000000                  MOV     #PRI00,R0
13165  034502  104441                          TRAP    C$SPRI
13166
13167                                          ;CHECK THAT NO INTERRUPTS OCCURED WHEN THE CPU PRIORITY LEVEL IS AT
13168                                          ;ZERO, THE TARGET EMULATOR INTERRUPT ENABLE BIT IS SET TO A ONE, THE
13169                                          ;SIGNAL TOBRK H IS ASSERTED LOW, AND THE BREAK LATCH FLIP-FLOP IS CLEARED
13170
13171  034504  000240                          NOP
13172  034506  005702                          TST     R2                      ;CHECK THE SOFTWARE INTERRUPT FLAG
13173  034510  001406                          BEQ     25$                     ;IF NO INTERRUPT THEN CONTINUE
13174  034512                                  ERRDF   1,UNEXIN,ROEROR         ;BREAK LATCH F/F NOT CLEARED BY BRKRES L
13175  034512  104455                          TRAP    C$ERDF
13176  034514  000001                          .WORD   1
13177  034516  002432                          .WORD   UNEXIN
13178  034520  004754                          .WORD   ROEROR
13179  034522  005002                          CLR     R2                      ;CLEAR SOFTWARE INTERRUPT FLAG
13180  034524                                  CKLOOP
13181  034524  104406                          TRAP    C$CLP1
13182
13183                                          ;RAISE THE CPU PRIORITY LEVEL TO 7 TO DISABLE INTERRUPTS
13184
13185  034526                          25$:    SETPRI  #PRI07                  ;RAISE CPU PRIORITY LEVEL TO 7
13186  034526  012700  000340                  MOV     #PRI07,R0
13187  034532  104441                          TRAP    C$SPRI
13188
13189                                          ;RETURN THE TARGET EMULATOR INTERRUPT VECTOR BACK TO THE DIAGNOSTIC
13190                                          ;SUPERVISOR VECTOR HANDLER
13191
13192  034534                                  CLRVEC  TEVECT
13193  034534  013700  002312                  MOV     TEVECT,R0
13194  034540  104436                          TRAP    C$CVEC
13195
13196  034542                                  ENDSEG
13197  034542                          10000$:
13198  034542  104405                          TRAP    C$ESEG
13199  034544                                  ENDTST
13200  034544                          L10075:
13201  034544  104401                          TRAP    C$ETST
13202
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13203                                   .SBTTL   TEST 44: INITO L AND INITO H LOGIC TEST
13204
13205                                   ;++
13206                                   ; THIS TEST WILL CHECK THAT THE SIGNALS ADAL 15:9, ADAL 7:3, ADAL 1:0, HDAL 15:0,
13207                                   ; FDAL7 H - FDAL0 H, VDAL7 H, VDAL2 H - VDAL0 H, GDAL15 H, GDAL2 H - GDAL0 H,
13208                                   ; AND MR15 H - MR0 H CAN ALL BE SET TO ONES.  THEN A BRESET INSTRUCTION IS
13209                                   ; ISSUED AND THESE SIGNALS ARE TESTED TO THEN BE ZEROS.  THEN THE PAUSE STATE
13210                                   ; WORKING FLIP-FLOP AND THE SINGLE STEP BREAK FLIP-FLOP ARE SET TO ONES AND
13211                                   ; AGAIN A BRESET INSTRUCTION IS ISSUED AND THESE FLIP-FLOPS ARE TESTED TO THEN
13212                                   ; BE ZEROS.
13213                                   ;--
13214
13215  034546                                   BGNTST
13216  034546                           T44::
13217
13218  034546  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
13219
13220                                   ;CHECK TO SEE IF ADAL15 H - ADAL0 H, HDAL15 H - HDAL0 H, FDAL7 H -
13221                                   ;FDAL0 H, VDAL7 H, VDAL2 H - VDAL0 H, GDAL15 H, GDAL2 H - GDAL0 H, AND
13222                                   ;MR15 H - MR0 H CAN BE SET TO ONES AND THEN CLEARED BY ISSUING A BRESET
13223                                   ;INSTRUCTION.
13224
13225  034552                                   BGNSUB
13226  034552                           T44.1:
13227  034552  104402                          TRAP    C$BSUB
13228  034554  005037  002346                  CLR     R6MASK                  ;CLEAR REG 6 MASK WORD
13229
13230                                   ;LOAD, READ AND CHECK BITS ADAL 15:9, ADAL 7:3, AND ADAL 1:0 WITH ALL ONES.
13231
13232  034560  012737  177373  002330          MOV     #177373,R2LOAD          ;SETUP DATA TO BE LOADED
13233  034566  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
13234  034572  001405                          BEQ     1$                      ;IF LOADED OK THEN CONT
13235  034574                                  ERRDF   2,ADALRG,R2EROR         ;REG 2 NOT EQUAL 177777
13236  034574  104455                          TRAP    C$ERDF
13237  034576  000002                          .WORD   2
13238  034600  002513                          .WORD   ADALRG
13239  034602  004770                          .WORD   R2EROR
13240  034604                                  CKLOOP
13241  034604  104406                          TRAP    C$CLP1
13242
13243                                   ;SET GDAL2 TO A ONE IN CONTROL REGISTER 0 TO SELECT THE MODE REGISTER
13244                                   ;WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13245
13246  034606  004737  007006          1$:     JSR     PC,SLMODR               ;GO SELECT MODE REG VIA GDAL BITS 2:0
13247
13248                                   ;LOAD, READ AND CHECK MODE REGISTER BITS 15:0 WITH A DATA PATTERN OF ALL
13249                                   ;ONES (177777) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
13250                                   ;WITH GDAL2 SET IN CONTROL REGISTER 0.
13251
13252  034612  012737  177777  002342          MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
13253  034620  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REG
13254  034624  001405                          BEQ     2$                      ;IF LOADED OK THEN CONT.
13255  034626                                  ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL 177777
13256  034626  104455                          TRAP    C$ERDF
13257  034630  000004                          .WORD   4
13258  034632  002631                          .WORD   MODREG
```

```
13259  034634  005020                          .WORD   R06ERR
13260  034636                                  CKLOOP
13261  034636  104406                          TRAP    C$CLP1
13262
13263                                          ;LOAD, READ AND CHECK BITS VDAL7 H, VDAL2 H - VDAL0 H WITH ONES.
13264
13265  034640  012737  000207  002334  2$:     MOV     #VDAL7.VDAL2!VDAL1!VDAL0,R4LOAD ;SET ALL R/W BITS TO ONE
13266  034646  004737  006640                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK REG 4
13267  034652  001405                          BEQ     3$                      ;IF LOADED OK THEN CONT
13268  034654                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
13269  034654  104455                          TRAP    C$ERDF
13270  034656  000003                          .WORD   3
13271  034660  002537                          .WORD   VDALRG
13272  034662  005004                          .WORD   R4EROR
13273  034664                                  CKLOOP
13274  034664  104406                          TRAP    C$CLP1
13275
13276                                          ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
13277                                          ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13278
13279  034666  004737  006754          3$:     JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
13280
13281                                          ;LOAD, READ AND CHECK HDAL REGISTER BITS 15:0 WITH A DATA PATTERN OF ALL
13282                                          ;ONES (177777) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
13283                                          ;WITH GDAL1 AND GDAL0 SET IN CONTROL REGISTER 0.
13284
13285  034672  012737  177777  002342          MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
13286  034700  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
13287  034704  001405                          BEQ     4$                      ;IF LOADED OK THEN CONT.
13288  034706                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REG NOT EQUAL 177777
13289  034706  104455                          TRAP    C$ERDF
13290  034710  000004                          .WORD   4
13291  034712  002605                          .WORD   HDALRG
13292  034714  005020                          .WORD   R06ERR
13293  034716                                  CKLOOP
13294  034716  104406                          TRAP    C$CLP1
13295
13296                                          ;SET GDAL1 IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER WHEN A
13297                                          ;WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13298
13299  034720  004737  007154          4$:     JSR     PC,SLFDAL               ;GO SELECT FDAL REG VIA GDAL BITS 2:0
13300
13301                                          ;LOAD, READ AND CHECK FDAL REGISTER BITS 7:0 WITH A DATA PATTERN OF ALL
13302                                          ;ONES (377) BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
13303                                          ;WITH GDAL1 SET TO A ONE IN CONTROL REGISTER 0.
13304
13305  034724  012737  177400  002346          MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE
13306  034732  012737  000377  002342          MOV     #377,R6LOAD             ;SETUP DATA TO BE LOADED
13307  034740  004737  006672                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK FDAL REG
13308  034744  001405                          BEQ     5$                      ;IF DATA LOADED OK THEN CONT
13309  034746                                  ERRDF   4,FDALRG,R06ERR         ;FDAL REG NOT EQUAL TO 377
13310  034746  104455                          TRAP    C$ERDF
13311  034750  000004                          .WORD   4
13312  034752  002653                          .WORD   FDALRG
13313  034754  005020                          .WORD   R06ERR
13314  034756                                  CKLOOP
```

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13315  034756  104406                          TRAP    C$CLP1
13316
13317                                          ;CHECK THAT GDAL BITS 2:0 AND GDAL BIT 15 CAN BE SET TO ONES
13318
13319  034760  013737  002316  002322  5$:     MOV     IDTYPE,ROGOOD          ;SETUP EXPECTED DATA
13320  034766  052737  000007  002322          BIS     #GDAL2!GDAL1.GDAL0,ROGOOD          ;SETUP EXPECTED DATA
13321  034774  052737  100007  002320          BIS     #GDAL15.GDAL2.GDAL1!GDAL0,ROLOAD   ;SETUP BITS TO BE LOADED
13322  035002  004737  006562                  JSR     PC,LDRDOR              ;GO LOAD, READ AND CHECK REG 0
13323  035006  001405                          BEQ     6$                     ;IF LOADED OK THEN CONT
13324  035010                                  ERRDF   1,GDALRG,ROEROR        ;REG 0 NOT EQUAL 100007
13325  035010  104455                          TRAP    C$ERDF
13326  035012  000001                          .WORD   1
13327  035014  002406                          .WORD   GDALRG
13328  035016  004754                          .WORD   ROEROR
13329  035020                                  CKLOOP
13330  035020  104406                          TRAP    C$CLP1
13331
13332                                          ;ISSUE A BRESET INSTRUCTION
13333
13334  035022                          6$:     BRESET                         ;ASSERT INITO L AND INITO H
13335  035022  104433                          TRAP    C$RESET
13336  035024                                  SETVEC  #4,#7$,#PRI07
13337  035024  012746  000340                  MOV     #PRI07,-(SP)
13338  035030  012746  035076                  MOV     #7$,-(SP)
13339  035034  012746  000004                  MOV     #4,-(SP)
13340  035040  012746  000003                  MOV     #3,-(SP)
13341  035044  104437                          TRAP    C$SVEC
13342  035046  062706  000010                  ADD     #10,SP
13343  035052  013705  002300                  MOV     REG0,R5                ;SAVE ADDRESS OF REG 0
13344  035056  113765  002311  000001          MOVB    IDDEV+1,1(R5)          ;SAVE ID NUMBER
13345  035064  000240                          NOP
13346  035066                                  CLRVEC  #4                     ;RELEASE DEVCICE TIMEOUT VECTOR
13347  035066  012700  000004                  MOV     #4,R0
13348  035072  104436                          TRAP    C$CVEC
13349  035074  000421                          BR      8$                     ;IF NO DEVICE TIMEOUT THEN CONTINUE
13350
13351                                          ;A DEVICE TIMEOUT OCCURED WHICH INDICATES THAT THERE IS NO DEVICE #0
13352                                          ;IN THE SYSTEM, THERFORE, THE TARGET EMULATOR HAS TO BE RESELECTED BY
13353                                          ;DOING A "MOV WORD" OPERATION. A "MOVB" OPERATION PERFORMED ABOVE DOES
13354                                          ;A READ/MODIFY WRITE.  THERFORE, IF THERE IS NO DEVICE #0 IN THE SYSTEM,
13355                                          ;A DEVICE TIMEOUT WILL OCCUR TO ADDRESS 4.
13356
13357  035076  005726                  7$:     TST     (SP)+                  ;CLEAN UP STACK AFTER DEVICE TIMEOUT
13358  035100  005726                          TST     (SP)+                  ;
13359  035102                                  CLRVEC  #4                     ;RELEASE DEVICE TIMEOUT VECTOR
13360  035102  012700  000004                  MOV     #4,R0
13361  035106  104436                          TRAP    C$CVEC
13362  035110  013737  002310  002320          MOV     IDDEV,ROLOAD           ;GET TAR EMULATORS DEVICE NUMBER
13363  035116  004737  006554                  JSR     PC,LDRDRO              ;LOAD, READ AND CHECK CONTROL REG 0
13364  035122  001424                          BEQ     9$                     ;IF OK THEN CONTINUE
13365  035124                                  ERRDF   1,GDALRG,ROEROR        ;REGISTER 0 NOT EQUAL EXPECTED
13366  035124  104455                          TRAP    C$ERDF
13367  035126  000001                          .WORD   1
13368  035130  002406                          .WORD   GDALRG
13369  035132  004754                          .WORD   ROEROR
13370  035134                                  CKLOOP
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13371  035134  104406                          TRAP    C$CLP1
13372  035136  000416                          BR      9$                      ;PROCEED IF LOOPING NOT INVOKED
13373
13374                                          ;READ AND CHECK GDAL BITS 2:0 AND GDAL BIT 15 FOR ALL ZEROS.
13375                                          .
13376  035140  013737  002310  002322  8$:     MOV     IDDEV,ROGOOD            ;GET USER DEFINED DEVICE NUMBER
13377  035146  013737  002322  002320          MOV     ROGOOD,ROLOAD           ;SETUP EXPECTED DATA
13378  035154  004737  006570                  JSR     PC,READR0               ;READ AND CHECK REG 0
13379  035160  001405                          BEQ     9$                      ;IF ALL ZEROS THEN CONT.
13380  035162                                  ERRDF   1,GDALRG,ROEROR         ;REGISTER 0 NOT EQUAL 0
13381  035162  104455                          TRAP    C$ERDF
13382  035164  000001                          .WORD   1
13383  035166  002406                          .WORD   GDALRG
13384  035170  004754                          .WORD   ROEROR
13385  035172                                  CKLOOP
13386  035172  104406                          TRAP    C$CLP1
13387
13388                                          ;READ AND CHECK BITS ADAL15 H - ADAL0 H FOR ALL ZEROS.
13389
13390  035174  005037  002330          9$:     CLR     R2LOAD                  ;SETUP EXPECTED DATA
13391  035200  004737  006622                  JSR     PC,READR2               ;READ AND CHECK REG 2
13392  035204  001405                          BEQ     10$                     ;IF ALL ZEROS THEN CONT
13393  035206                                  ERRDF   2,ADALRG,R2EROR         ;REG 2 NOT EQUAL TO 0
13394  035206  104455                          TRAP    C$ERDF
13395  035210  000002                          .WORD   2
13396  035212  002513                          .WORD   ADALRG
13397  035214  004770                          .WORD   R2EROR
13398  035216                                  CKLOOP
13399  035216  104406                          TRAP    C$CLP1
13400
13401                                          ;READ AND CHECK BITS VDAL7 H, VDAL2 H - VD4L0 H FOR ALL ZEROS.
13402
13403  035220  005037  002336          10$:    CLR     R4GOOD                  ;SETUP EXPECTED DATA
13404  035224  004737  006654                  JSR     PC,READR4               ;GO READ AND CHECK REG 4
13405  035230  001405                          BEQ     11$                     ;IF ALL ZEROS THEN CONT
13406  035232                                  ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
13407  035232  104455                          TRAP    C$ERDF
13408  035234  000003                          .WORD   3
13409  035236  002537                          .WORD   VDALRG
13410  035240  005004                          .WORD   R4EROR
13411  035242                                  CKLOOP
13412  035242  104406                          TRAP    C$CLP1
13413
13414                                          ;SET GDAL1 AND GDAL0 TO ONES IN CONTROL REGISTER 0 TO SELECT THE HDAL
13415                                          ;REGISTER WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13416
13417  035244  004737  006754          11$:    JSR     PC,SLHDAL               ;SELECT HDAL REG VIA GDAL BITS 2:0
13418
13419                                          ;READ AND CHECK HDAL REGISTER BITS 15:0 FOR A DATA PATTERN OF ALL
13420                                          ;ZEROS BY ISSUING A READ COMMAN TO CONTRO REGISTER 6 WITH GDAL1 AND
13421                                          ;GDAL0 SET IN CONTROL REGISTER 0.
13422
13423  035250  005037  002342                  CLR     R6LOAD                  ;SETUP EXPECTED DATA
13424  035254  004737  006700                  JSR     PC,READR6               ;READ AND CHECK REG 6
13425  035260  001405                          BEQ     12$                     ;IF ALL ZEROS THEN CONT.
13426  035262                                  ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL 0
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13427  035262  104455                          TRAP    C$ERDF
13428  035264  000004                          .WORD   4
13429  035266  002605                          .WORD   HDALRG
13430  035270  005020                          .WORD   R06ERR
13431  035272                                  CKLOOP
13432  035272  104406                          TRAP    C$CLP1
13433
13434                                          ;SET GDAL2 TO A ONE IN CONTROL REGISTER 0 TO SELECT THE MODE REGISTER
13435                                          ;WHEN A WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13436
13437  035274  004737  007006          12$:    JSR     PC,SLMODR               ;GO SELECT MODE REG VIA GDAL BITS 2:0
13438
13439                                          ;READ AND CHECK MODE REGISTER BITS 15:0 FOR A DATA PATTERN OF ALL
13440                                          ;ZEROS BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6
13441                                          ;WITH GDAL2 SET IN CONTROL REGISTER 0.
13442
13443  035300  005037  002342                  CLR     R6LOAD                  ;SETUP EXPECTED DATA
13444  035304  004737  006700                  JSR     PC,READR6               ;READ AND CHECK REG 6
13445  035310  001405                          BEQ     13$                     ;IF LOADED OK THEN CONT.
13446  035312                                  ERRDF   4,MODREG,R06ERR         ;MODE REG NOT EQUAL 0
13447  035312  104455                          TRAP    C$ERDF
13448  035314  000004                          .WORD   4
13449  035316  002631                          .WORD   MODREG
13450  035320  005020                          .WORD   R06ERR
13451  035322                                  CKLOOP
13452  035322  104406                          TRAP    C$CLP1
13453
13454                                          ;SET GDAL1 IN CONTROL REGISTER 0 TO SELECT THE FDAL REGISTER WHEN A
13455                                          ;WRITE OR READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
13456
13457  035324  004737  007154          13$:    JSR     PC,SLFDAL               ;GO SELECT FDAL REG VIA GDAL BITS 2:0
13458
13459                                          ;READ AND CHECK FDAL REGISTER BITS 7:0 FOR A DATA PATTERN OF ALL ZEROS
13460                                          ;BY ISSUING A WRITE AND READ COMMAND TO CONTROL REGISTER 6 WITH GDAL1
13461                                          ;SET TO A ONE IN CONTROL REGISTER 0.
13462
13463  035330  012737  177400  002346          MOV     #177400,R6MASK          ;SETUP TO IGNORE HIGH BYTE
13464  035336  005037  002342                  CLR     R6LOAD                  ;SETUP EXPECTED DATA
13465  035342  004737  006700                  JSR     PC,READR6               ;READ AND CHECK REG 6
13466  035346  001404                          BEQ     14$                     ;IF DATA LOADED OK THEN CONT
13467  035350                                  ERRDF   4,FDALRG,R06ERR         ;FDAL REGISTER NOT EQUAL TO 0
13468  035350  104455                          TRAP    C$ERDF
13469  035352  000004                          .WORD   4
13470  035354  002653                          .WORD   FDALRG
13471  035356  005020                          .WORD   R06ERR
13472  035360                          14$:    ENDSUB
13473  035360                          L10077:
13474  035360  104403                          TRAP    C$ESUB
13475
13476                                          ;CHECK TO SEE IF PAUSE STATE WORKING FLIP-FLOP CAN BE SET TO ONE AND
13477                                          ;THEN CLEARED BY INITO H.  ALSO CHECK TO SEE IF SINGLE STEP BREAK FLIP-
13478                                          ;FLOP CAN BE SET TO ONE AND THEN CLEARED BY INITO L.
13479
13480  035362                                  BGNSUB
13481  035362                          T44.2:
13482  035362  104402                          TRAP    C$BSUB
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13483
13484                                   ;SET VDAL2 H TO A ONE AND THEN A ZERO.  VDAL2 H ON A ONE WILL CLEAR
13485                                   ;THE PAUSE STATE MACHINE FLIP-FLOPS, AND PRESET THE SINGLE STEP SYNC
13486                                   ;FLIP-FLOP.
13487
13488  035364  005037  002334          CLR     R4LOAD                  ;SETUP TO CLEAR ALL VDAL BITS
13489  035370  004737  007712          JSR     PC,CLRPSM               ;GO PULSE VDAL2 H
13490
13491                                   ;SET VDAL7 H TO A ONE TO SET THE SIGNAL FETCT H TO THE HIGH STATE (1).
13492
13493  035374  012737  000200  002334  MOV     #VDAL7,R4LOAD           ;SETUP BIT TO SET FETCT H TO HIGH STATE
13494  035402  004737  006640          JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK REG 4
13495  035406  001405                  BEQ     1$                      ;IF LOADED OK THEN CONT
13496  035410                          ERRDF   3,VDALRG,R4EROR         ;VDAL REGISTER NOT EQUAL EXPECTED
13497  035410  104455                  TRAP    C$ERDF
13498  035412  000003                  .WORD   3
13499  035414  002537                  .WORD   VDALRG
13500  035416  005004                  .WORD   R4EROR
13501  035420                          CKLOOP
13502  035420  104406                  TRAP    C$CLP1
13503
13504                                   ;LOAD, READ AND CHECK ADAL REGISTER.  ADAL8 H ON A ZERO WILL DISABLE THE
13505                                   ;TIMEOUT BREAK SIGNAL FROM CAUSING A BREAK CONDITION.  ADAL4 H ON A ZERO
13506                                   ;WILL CAUSE THE PAUSE STATE MACHINE TO BE ENTERED ON A FETCH CYCLE WHEN
13507                                   ;THE SIGNAL XRAS H IS PULSED.  ADAL5 H ON A ONE WILL ENABLE A ONE TO BE
13508                                   ;CLOCKED INTO THE SINGLE STEP BREAK FLIP-FLOP WHEN XRAS H IS PULSED.
13509                                   ;ADAL0 H WILL BE SET AND CLEARED TO CLEAR THE BREAK LOGIC.
13510
13511  035422  012737  000040  002330  1$:     MOV     #ADAL5,R2LOAD           ;SETUP BIT TO BE LOADED
13512  035430  004737  007772          JSR     PC,BRKRES               ;GO PULSE ADAL0 H TO CLEAR BREAK LOGIC
13513
13514                                   ;SELECT THE HDAL REGISTER BY SETTING GDAL2 TO A ZERO AND GDAL1 AND GDAL0
13515                                   ;TO ONES.
13516
13517  035434  004737  006754          JSR     PC,SLHDAL               ;GO SELECT HDAL REG VIA GDAL 2:0
13518
13519                                   ;TOGGLE THE SIGNAL XRAS H BY SETTING AND CLEARING HDAL12 H.  THE SIGNAL
13520                                   ;XRAS H WILL CLOCK THE STATE OF THE SIGNAL FETCT H, WHICH IS HIGH, INTO
13521                                   ;THE EDFET FLIP-FLOP, THUS SETTING THE SIGNAL EDFET H TO THE HIGH STATE.
13522                                   ;THE SIGNAL XRAS H WILL CLOCK THE STATE OF THE SINGLE STEP SYNC FLIP-
13523                                   ;FLOP, WHICH IS HIGH, INTO THE SINGLE STEP BREAK FLIP-FLOP WHEN ADAL5 H
13524                                   ;AND FETCT H ARE ONES, THUS SETTING THE SIGNAL SSBRK H TO THE HIGH STATE.
13525                                   ;WHEN SSBRK H IS SET HIGH THE SIGNAL BRK H WILL ALSO BE SET HIGH.  WHEN
13526                                   ;THE SIGNALS BRK H AND FETCT H ARE BOTH SET HIGH THE PAUSE STATE MACHINE
13527                                   ;WILL BE IN THE PAUSE MODE, THUS SETTING SOP H TO THE HIGH STATE.  WHEN
13528                                   ;THE SIGNALS SOP H AND EDFET H ARE BOTH SET HIGH THE PAUSE STATE WORKING
13529                                   ;FLIP-FLOP WILL BE DIRECTLY SET TO THE HIGH STATE, THUS SETTING THE SIGNAL
13530                                   ;PSMW H TO THE HIGH STATE.
13531
13532  035440  005037  002346          CLR     R6MASK                  ;SETUP TO READ ALL BITS
13533  035444  005037  002342          CLR     R6LOAD                  ;CLEAR OUT OLD DATA
13534  035450  004737  007272          JSR     PC,XRAS                 ;GO PULSE XRAS H VIA SIGNAL HDAL12
13535
13536                                   ;READ THE VDAL REGISTER AND CHECK THAT THE PAUSE STATE WORKING FLIP-
13537                                   ;FLOP IS SET TO A ONE.
13538
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13539  035454  052737  001200  002336          BIS     #VDAL9!VDAL7,R4GOOD     ;SETUP BITS TO BE READ
13540  035462  004737  006654                  JSR     PC,READR4               ;GO READ VDAL REG
13541  035466  001405                          BEQ     2$                      ;IF OK THEN CONT
13542  035470                                  ERRDF   3,VDALRG,R4EROR         ;PSMW H PROBABLY NOT SET IN VDAL REG
13543  035470  104455                          TRAP    C$ERDF
13544  035472  000003                          .WORD   3
13545  035474  002537                          .WORD   VDALRG
13546  035476  005004                          .WORD   R4EROR
13547  035500                                  CKLOOP
13548  035500  104406                          TRAP    C$CLP1
13549
13550                                          ;READ THE GDAL REGISTER AND CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
13551                                          ;IS SET TO A ONE.
13552
13553  035502  052737  000200  002322  2$:     BIS     #GDAL7,ROGOOD           ;SETUP EXPECTED BITS
13554  035510  004737  006570                  JSR     PC,READR0               ;GO READ GDAL REG
13555  035514  001405                          BEQ     3$                      ;IF OK THEN CONT.
13556  035516                                  ERRDF   1,GDALRG,ROEROR         ;GDAL REGISTER NOT EQUAL EXPECTED
13557  035516  104455                          TRAP    C$ERDF
13558  035520  000001                          .WORD   1
13559  035522  002406                          .WORD   GDALRG
13560  035524  004754                          .WORD   ROEROR
13561  035526                                  CKLOOP
13562  035526  104406                          TRAP    C$CLP1
13563
13564                                          ;ISSUE A BRESET INSTRUCTION
13565
13566  035530                          3$:     BRESET                          ;ASSERT INIT0 L AND INIT0 H
13567  035530  104433                          TRAP    C$RESET
13568  035532                                  SETVEC  #4,#4$,#PRI07
13569  035532  012746  000340                  MOV     #PRI07,-(SP)
13570  035536  012746  035604                  MOV     #4$,-(SP)
13571  035542  012746  000004                  MOV     #4,-(SP)
13572  035546  012746  000003                  MOV     #3,-(SP)
13573  035552  104437                          TRAP    C$SVEC
13574  035554  062706  000010                  ADD     #10,SP
13575  035560  013705  002300                  MOV     REG0,R5                 ;SAVE ADDRESS OF REG 0
13576  035564  113765  002311  000001          MOVB    IDDEV+1,1(R5)           ;SAVE ID NUMBER
13577  035572  000240                          NOP
13578  035574                                  CLRVEC  #4                      ;RELEASE DEVICE TIMEOUT VECTOR
13579  035574  012700  000004                  MOV     #4,R0
13580  035600  104436                          TRAP    C$CVEC
13581  035602  000420                          BR      5$                      ;NO TIMEOUT OCCURED - CONTINUE
13582
13583                                          ;A DEVICE TIMEOUT OCCURED WHICH INDICATES THAT THERE IS DEVICE #0
13584                                          ;IN THE SYSTEM, THERFORE, THE TARGET EMULATOR HAS TO BE RESELECTED BY
13585                                          ;DOING A "MOV WORD" OPERATION. A "MOVB" OPERATION PERFORMED ABOVE DOES
13586                                          ;A READ/MODIFY WRITE. THERFORE, IF THERE IS NO DEVICE #0 IN THE SYSTEM,
13587                                          ;A DEVICE TIMEOUT WILL OCCUR TO ADDRESS 4.
13588
13589  035604  005726                  4$:     TST     (SP)+                   ;CLEAN UP STACK AFTER DEVICE TIMEOUT
13590  035606  005726                          TST     (SP)+                   ;
13591  035610                                  CLRVEC  #4                      ;RELEASE DEVICE TIMEOUT VECTOR
13592  035610  012700  000004                  MOV     #4,R0
13593  035614  104436                          TRAP    C$CVEC
13594  035616  013737  002310  002320          MOV     !DDEV,ROLOAD            ;GET THE DEVICE NUMBER
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13595  035624  004737  006554          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
13596  035630  001405                  BEQ     5$                      ;IF LOADED OK THEN CONTINUE
13597  035632                          ERRDF   1,GDALRG,R0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
13598  035632  104455                  TRAP    C$ERDF
13599  035634  000001                  .WORD   1
13600  035636  002406                  .WORD   GDALRG
13601  035640  004754                  .WORD   R0EROR
13602  035642                          CKLOOP
13603  035642  104406                  TRAP    C$CLP1
13604
13605                                  ;READ THE VDAL REGISTER AND CHECK  HAT THE PAUSE STATE WORKING
13606                                  ;FLIP-FLOP IS NOW SET TO A ZERO.
13607
13608  035644  005037  002336    5$:   CLR     R4GOOD                  ;SETUP BITS TO BE READ
13609  035650  004737  006654          JSR     PC,READR4               ;GO READ VDAL REG
13610  035654  001405                  BEQ     6$                      ;IF OK THEN CONT.
13611  035656                          ERRDF   3,VDALRG,R4EROR         ;VDAL REG NOT EQUAL EXPECTED
13612  035656  104455                  TRAP    C$ERDF
13613  035660  000003                  .WORD   3
13614  035662  002537                  .WORD   VDALRG
13615  035664  005004                  .WORD   R4EROR
13616  035666                          CKLOOP
13617  035666  104406                  TRAP    C$CLP1
13618
13619                                  ;READ THE GDAL REGISTER AND CHECK THAT THE SINGLE STEP BREAK FLIP-FLOP
13620                                  ;IS NOW SET TO A ZERO.
13621
13622  035670  105037  002322    6$:   CLRB    R0GOOD                  ;SETUP EXPECTED BITS
13623  035674  004737  006570          JSR     PC,READR0               ;GO READ GDAL REG
13624  035700  001404                  BEQ     7$                      ;IF OK THEN CONT.
13625  035702                          ERRDF   1,GDALRG,R0EROR         ;GDAL REGISTER NOT EQUAL EXPECTED
13626  035702  104455                  TRAP    C$ERDF
13627  035704  000001                  .WORD   1
13628  035706  002406                  .WORD   GDALRG
13629  035710  004754                  .WORD   R0EROR
13630  035712                  7$:     ENDSUB
13631  035712                  L10100:
13632  035712  104403                  TRAP    C$ESUB
13633
13634  035714                          ENDTST
13635  035714                  L10076:
13636  035714  104401                  TRAP    C$ETST
```

TEST 45: T-11 STARTING ADDRESS TEST IN DIFFERENT MODE; SEQ 0267

```
13637                                   .SBTTL  TEST 45: T-11 STARTING ADDRESS TEST IN DIFFERENT MODES
13638
13639                                   ;++
13640                                   ; THIS TEST WILL CHECK THAT THE T-11 CAN BE POWERED UP TO ALL ITS STARTING
13641                                   ; ADDRESSES AND THAT IT CAN RUN WITH DIFFERENT MODES SELECTED.  THE PROGRAM WILL
13642                                   ; USE THE PAUSE STATE MACHINE TO CHECK THAT THE T-11 POWERED UP TO THE
13643                                   ; STARTING ADDRESS SELECTED BY THE MODE REGISTER.  THE PROGRAM WILL SELECT THE
13644                                   ; FOLLOWING T-11 MODES; 16 BIT STATIC, 16 BIT DYNAMIC 4K/16K, 16 BIT DYNAMIC 64K,
13645                                   ; 8 BIT STATIC, 8 BIT DYNAMIC 4K/16K AND 8 BIT DYNAMIC 64K.  FOR EACH MODE
13646                                   ; SELECTED, THE PROGRAM WILL CHECK THAT THE T-11 CAN BE POWERED UP AT EACH OF
13647                                   ; ITS STARTING ADDRESSES.  THE PROGRAM WILL SELECT THE CLOCK ON THE TARGET
13648                                   ; EMULATOR MODULE TO PROVIDE THE TIMING TO THE T-11 CHIP.  THE TEST WILL ALSO
13649                                   ; CHECK THAT THE NEW FORCE JUMP ADDRESS REGISTER CAN BE LOADED AND THAT ITS
13650                                   ; CONTENTS CAN BE LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER.
13651                                   ;--
13652
13653  035716                                   BGNTST
13654  035716                           T45::
13655
13656  035716  004737  005510                  JSR     PC,INITTE               ;SELECT AND INITIALIZE TARGET EMULATOR
13657
13658  035722  012701  036362                  MOV     #14$,R1                 ;ADDRESS OF T-11 MODE REGISTER TABLE
13659  035726  005002                          CLR     R2                      ;T-11 STARTING ADDRESS MODE PARAMTER
13660  035730  012703  036400                  MOV     #15$,R3                 ;ADDRESS OF EXPECTED STARTING ADDRESS TABLE
13661
13662  035734                           1$:     BGNSEG
13663  035734  104404                          TRAP    C$BSEG
13664
13665                                   ;LOAD ADAL REGISTER WITH ALL ZEROES TO TURN OFF THE T-11 CHIP AND
13666                                   ;TO DISABLE CERTAIN BUSSES FROM OTHER BUSSES
13667
13668  035736  005037  002330                  CLR     R2LOAD                  ;SETUP TO CLEAR ALL BITS
13669  035742  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD  READ AND CHECI ADAL REGISTER
13670  035746  001405                          BEQ     2$                      ;IF LOADED OK THEN CONT NUE
13671  035750                                   ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
13672  035750  104455                          TRAP    C$ERDF
13673  035752  000002                          .WORD   2
13674  035754  002513                          .WORD   ADALRG
13675  035756  004770                          .WORD   R2EROR
13676  035760                                   CKLOOP
13677  035760  104406                          TRAP    C$CLP1
13678
13679                                   ;PULSE THE SIGNAL BRKRES L BY SETTING AND CLEARING ADAL REGISTER BIT 0.
13680                                   ;THE SIGNAL BRKRES L WILL CLEAR THE BREAK LATCH FLIP-FLOP, THE SINGLE
13681                                   ;STEP BREAK FLIP-FLOP AND THE MEMORY SIMULATOR BREAK FLIP-FLOP.
13682
13683  035762  004737  007772           2$.     JSR     PC,BRKRES               ;GO PULSE BRKRES L VIA ADALO H
13684
13685                                   ;PULSE THE SIGNAL INVD L BY SETTING AND CLEARING VDAL REGISTER BIT 4.
13686                                   ;A PULSE ON THE SIGNAL INVD L WILL INITIALIZE ALL OTHER FLIP-FLOPS ON
13687                                   ;THE MODULE TO A KNWON STATE EXCEPT FOR THOSE CLEARED BY THE SIGNAL
13688                                   ;BRKRES L ABOVE.
13689
13690  035766  005037  002334                  CLR     R4LOAD                  ;SETUP TO CLEAR ALL VDAL R/W BITS
13691  035772  004737  007712                  JSR     PC,CLRPSM               ;GO PULSE INVD L VIA VDAL2 H
13692
```

```
13693                                           ;SELECT THE HDAL REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
13694
13695  035776  004737  006754                   JSR     PC,SLHDAL               ;SELECT HDAL REGISTER VIA GDAL BITS 2:0
13696
13697                                           ;CLEAR ALL BITS IN THE HDAL REGISTER.  HDAL2 H ON A ZERO WILL ALLOW THE
13698                                           ;T-11 CHIP TO GENERATE ALL THE T-11 TIMING AND CONTROL SIGNALS.
13699
13700  036002  005037  002342                   CLR     R6LOAD                  ;SETUP TO CLEAR ALL HDAL BITS
13701  036006  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK HDAL REGISTER
13702  036012  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
13703  036014                                   ERRDF   4,HDALRG,R06ERR         ;HDAL REGISTER NOT EQUAL EXPECTED
13704  036014  104455                           TRAP    C$ERDF
13705  036016  000004                           .WORD   4
13706  036020  002605                           .WORD   HDALRG
13707  036022  005020                           .WORD   R06ERR
13708  036024                                   CKLOOP
13709  036024  104406                           TRAP    C$CLP1
13710
13711                                           ;SELECT THE FDAL AND EOAI REGISTER VIA GDAL BITS 2:0 IN CONTROL REG 0
13712
13713  036026  004737  007154           3$:     JSR     PC,SLFDAL               ;SELECT FDAL AND EOAI REG VIA GDAL 2:0
13714
13715                                           ;SET ALL BITS IN THE EOAI REGISTER TO ZERO.  SET FDAL0 H TO A ONE SO
13716                                           ;THAT THE EOAI REGISTER CAN BE READBACK ON A READ COMMAND TO CONTROL
13717                                           ;REGISTER 6 INSTEAD OF THE CTL REGISTER.
13718
13719  036032  012737  000001  002342           MOV     #FDAL0,R6LOAD           ;SETUP BITS TO BE LOADED
13720  036040  004737  006672                   JSR     PC,LDRDR6               ;LOAD, READ AND CHECK FDAL AND EOAI REG
13721  036044  001405                           BEQ     4$                      ;IF LOADED OK THEN CONTINUE
13722  036046                                   ERRDF   4,EOAIFD,R06ERR         ;EOAI OR FDAL REGISTER ERROR
13723  036046  104455                           TRAP    C$ERDF
13724  036050  000004                           .WORD   4
13725  036052  002676                           .WORD   EOAIFD
13726  036054  005020                           .WORD   R06ERR
13727  036056                                   CKLOOP
13728  036056  104406                           TRAP    C$CLP1
13729
13730                                           ;SELECT MODE REGISTER VIA GDAL BITS 2:0 IN CONTROL REGISTER 0
13731
13732  036060  004737  007006           4$:     JSR     PC,SLMODR               ;SELECT MODE REGISTER VIA GDAL BITS 2:0
13733
13734                                           ;LOAD THE T-11 MODE SELECT PARAMETERS FROM THE MODE TABLE INTO THE
13735                                           ;MODE REGISTER.  THESE PARAMETERS WILL BE USED BY THE T-11 CHIP ON
13736                                           ;ITS POWER-UP SEQUENCE.
13737
13738  036064  011137  002342                   MOV     (R1),R6LOAD             ;GET T-11 MODE SELECT PARAMETER
13739  036070  050237  002342                   BIS     R2,R6LOAD               ;ADD STARTING ADDRESS MODE PARAMETER
13740  036074  004737  006672                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK MODE REGISTER
13741  036100  001405                           BEQ     5$                      ;IF LOADED OK THEN CONTINUE
13742  036102                                   ERRDF   4,MODREG,R06ERR         ;MODE REGISTER NOT EQUAL EXPECTED
13743  036102  104455                           TRAP    C$ERDF
13744  036104  000004                           .WORD   4
13745  036106  002634                           .WORD   MODREG
13746  036110  005020                           .WORD   R06ERR
13747  036112                                   CKLOOP
13748  036112  104406                           TRAP    C$CLP1
```

```
13749
13750                                           ;SET ADAL REGISTER BITS 13, 12, 10, 2, AND 1 TO ONES AND ALL OTHER ADAL
13751                                           ;REGISTER BITS TO ZEROES.  ADAL12 H ON A ONE WILL ENABLE THE MODE
13752                                           ;REGISTER TO THE T-11 CHIP WHEN THE SIGNAL PBCLR H IS ASSERTED HIGH
13753                                           ;AND THE T-11 IS IN ITS POWER-UP SEQUENCE.  ADAL10 H ON A ONE WILL
13754                                           ;ENABLE THE EIAI BUS TO THE CTL BUS AND THE EIDAL BUS TO THE ADDRESS
13755                                           ;BUS.  ADAL2 H ON A ONE WILL CAUSE THE SIGNAL CPUP L TO BE ASSERTED
13756                                           ;LOW.  WHEN CPUP L IS ASSERTED LOW, THE T-11 CHIP WILL START ITS POWER-
13757                                           ;UP SEQUENCE.  ADAL1 H ON A ONE WILL SELECT THE 5.068 MHZ CLOCK ON THE
13758                                           ;TARGET EMULATOR MODULE.  ADAL4 H ON A ZERO WILL CAUSE THE PAUSE STATE
13759                                           ;MACHINE TO BE IN PAUSE MODE ON THE FIRST PULSE OF XRAS H.
13760                                           ;ADAL13 H ON A ONE WILL ALLOW THE T-11 TO EXAMINE THE AI LINES DURING
13761                                           ;THE T-11 POWER UP SEQUENCE.
13762
13763  036114  012737  032006  002330  5$:     MOV     #ADAL13!ADAL12!ADAL10!ADAL2!ADAL1,R2LOAD ;SETUP BITS TO BE LOADED
13764  036122  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
13765  036126  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
13766  036130                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
13767  036130  104455                          TRAP    C$ERDF
13768  036132  000002                          .WORD   2
13769  036134  002513                          .WORD   ADALRG
13770  036136  004770                          .WORD   R2EROR
13771  036140                                  CKLOOP
13772  036140  104406                          TRAP    C$CLP1
13773
13774                                           ;SETUP TIMEOUT COUNTERS TO WAIT FOR THE PAUSE STATE MACHINE TO BE
13775                                           ;ENTERED.  THE PAUSE STATE WORKING FLIP-FLOP SHOULD BE SET WHEN THE
13776                                           ;T-11 CAUSES THE SIGNAL FETCT H TO BE ASSERTED HIGH AND THE T-11
13777                                           ;GENERATES A PULSE ON THE SIGNAL XRAS H.
13778
13779  036142  012705  000002          6$:     MOV     #2,R5                   ;SETUP DOUBLE PRECISION COUNTER
13780  036146  005004                          CLR     R4                      ;CLEAR SIGNLE PRECISSION COUNTER
13781  036150  032777  001000  144126  7$:     BIT     #VDAL9,@REG4            ;CHECK PAUSE STATE WORKING F/F
13782  036156  001011                          BNE     8$                      ;IF SET THEN PAUSE STATE ENTERED
13783  036160  005304                          DEC     R4                      ;DECREMNET FIRST COUNTER
13784  036162  001372                          BNE     7$                      ;IF NOT 0 THEN CHECK PAUSE STATE AGAIN
13785  036164  005305                          DEC     R5                      ;DECREMENT DOUBLE PRECISSION COUNTER
13786  036166  001370                          BNE     7$                      ;IF NOT 0 THEN CHECK PAUSE STATE AGAIN
13787  036170                                  ERRDF   5,NOPSM,R026ER          ;PAUSE STATE NOT ENTERED WHEN T-11 IS ON
13788  036170  104455                          TRAP    C$ERDF
13789  036172  000005                          .WORD   5
13790  036174  005773                          .WORD   NOPSM
13791  036176  005034                          .WORD   R026ER
13792  036200                                  CKLOOP
13793  036200  104406                          TRAP    C$CLP1
13794
13795                                           ;READ THE FORCE JUMP ADDRESS REGISTER TO CHECK THAT THE T-11 PLACED
13796                                           ;THE CORRECT STARTING ADDRESS ONTO THE ADDRESS BUS FOR THE MODE
13797                                           ;SELECTED IN THE MODE REGISTER.  THE ADDRESS BUS IS CLOCKED INTO
13798                                           ;THE FORCE JUMP ADDRESS READBACK REGISTER WHEN THE EDFET FLIP-FLOP
13799                                           ;IS SET TO A ONE AND A PULSE IS ISSUED ON THE SIGNAL RASP H. THE
13800                                           ;CLOCKING SIGNAL GENERATED IS CALLED DFET H.
13801
13802  036202  004737  007040          8$:     JSR     PC,SLFJAR               ;SELECT FJA REG VIA GDAL BITS 2:0
13803
13804                                           ;READ THE FORCE JUMP ADDRESS READBACK REGISTER BACK TO THE LSI-11
```

```
13805
13806  036206  011337  002342                  MOV     (R3),R6LOAD             ;GET EXPECTED ADDRESS FROM THE TABLE
13807  036212  004737  006700                  JSR     PC,READR6               ;READ FJA READBACK REGISTER AND CHECK IT
13808  036216  001405                          BEQ     9$                      ;IF STARTING ADDRESS = EXPECTED - CONT
13809  036220                                  ERRDF   5,FJSTAD,R026ER         ;FJA NOT EQUAL EXPECTED T-11 STARTING ADDRESS
13810  036220  104455                          TRAP    C$ERDF
13811  036222  000005                          .WORD   5
13812  036224  004060                          .WORD   FJSTAD
13813  036226  005034                          .WORD   R026ER
13814  036230                                  CKLOOP
13815  036230  104406                          TRAP    C$CLP1
13816
13817                                          ;THE TEST WILL NOW LOAD THE NEW FORCE JUMP ADDRESS REGISTER WITH AN
13818                                          ;ADDRESS DIFFERENT FROM THE STARTING ADDRESS THAT THE T-11 POWERED UP
13819                                          ;WITH.  THE NEW ADDRESS LOADED WILL CORRESPOND TO ONE OF THE FOLLOWING:
13820                                          ;    IF STARTING ADDRESS = 140000 THEN NEW ADDRESS = 037777
13821                                          ;    IF STARTING ADDRESS = 100000 THEN NEW ADDRESS = 052525
13822                                          ;    IF STARTING ADDRESS = 040000 THEN NEW ADDRESS = 125252
13823                                          ;    IF STARTING ADDRESS = 020000 THEN NEW ADDRESS = 146314
13824                                          ;    IF STARTING ADDRESS = 010000 THEN NEW ADDRESS = 031463
13825                                          ;    IF STARTING ADDRESS = 000000 THEN NEW ADDRESS = 177777
13826                                          ;    IF STARTING ADDRESS = 173000 THEN NEW ADDRESS = 004777
13827                                          ;    IF STARTING ADDRESS = 172000 THEN NEW ADDRESS = 005777
13828
13829  036232  016377  000020  144046  9$:     MOV     20(R3),@REG6            ;WRITE NEW FORCE JUMP ADDRESS REGISTER
13830                                                                          ;WITH NEW ADDRESS FROM TABLE
13831
13832                                          ;READ THE FORCE JUMP ADDRESS READBACK REGISTER TO CHECK THAT THE NEW
13833                                          ;FORCE JUMP ADDRESS WAS LOADED INTO THE OLD FORCE JUMP ADDRESS REGISTER
13834
13835  036240  016337  000020  002342          MOV     20(R3),R6LOAD           ;GET ADDRESS LOADED INTO NEW FJA REG
13836  036246  012704  000004                  MOV     #4,R4                   ;SETUP TO READ 4 TIMES BEFORE FLAGGING
13837                                                                          ;THAT AN ERROR OCCURED
13838  036252  017737  144030  002344  10$:     MOV     @REG6,R6READ            ;READ FJA READBACK REGISTER
13839  036260  023737  002342  002344          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED AGAINST DATA READ
13840  036266  001407                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
13841  036270  005304                          DEC     R4                      ;CHECK IF ALOTTED READS OCCURED
13842  036272  001367                          BNE     10$                     ;IF NOT THEN READ FJA READBACK REG AGAIN
13843  036274                                  ERRDF   5,FJADRG,R026ER         ;NEW FJA NOT LOADED INTO OLD FJA REG
13844  036274  104455                          TRAP    C$ERDF
13845  036276  000005                          .WORD   5
13846  036300  002766                          .WORD   FJADRG
13847  036302  005034                          .WORD   R026ER
13848  036304                                  CKLOOP
13849  036304  104406                          TRAP    C$CLP1
13850
13851                                          ;CLEAR ALL ADAL REGISTER BITS.  THIS WILL TURN THE T-11 CHIP OFF AGAIN.
13852
13853  036306  005037  002330          11$:     CLR     R2LOAD                  ;SETUP TO CLEAR ALL ADAL REGISTER BITS
13854  036312  004737  006614                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK ADAL REGISTER
13855  036316  001404                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
13856  036320                                  ERRDF   2,ADALRG,R2EROR         ;ADAL REGISTER NOT EQUAL EXPECTED
13857  036320  104455                          TRAP    C$ERDF
13858  036322  000002                          .WORD   2
13859  036324  002513                          .WORD   ADALRG
13860  036326  004770                          .WORD   R2EROR
```

```
13861  036330                          12$:    ENDSEG
13862  036330                          10000$:
13863  036330  104405                          TRAP    C$ESEG
13864
13865  036332  062702  020000                  ADD     #BIT13,R2               ;UPDATE T-11 STARTING ADDRESS PARAMETER
13866  036336  001403                          BEQ     13$                     ;IF DONE THEN CONTINUE
13867  036340  005723                          TST     (R3)+                   ;UPDATE STARTING ADDRESS TABLE POINTER
13868  036342  000137  035734                  JMP     1$                      ;GO LOAD AND CHECK NEXT ADDRESS IN THIS MODE
13869
13870  036346  012703  036400          13$:    MOV     #15$,R3                 ;RESET STARTING ADDRESS TABLE POINTER
13871  036352  005721                          TST     (R1)+                   ;UPDATE TABLE MODE PARAMETER POINTER
13872  036354  001431                          BEQ     16$                     ;IF 0 THEN EXIT THE TEST
13873  036356  000137  035734                  JMP     1$                      ;GO LOAD NEXT PARAMETER
13874
13875                                          ;T-11 MODE SELECT PARAMTER TABLE WITHOUT STARTING ADDRESS PARAMTER
13876
13877  036362  011003                  14$:    .WORD   011003                  ;16 BIT STATIC MODE
13878  036364  012003                          .WORD   012003                  ;16 BIT DYNAMIC MODE 4/16 K
13879  036366  010003                          .WORD   010003                  ;16 BIT DYNAMIC MODE 64K
13880  036370  015003                          .WORD   015003                  ;8  BIT STATIC MODE
13881  036372  016003                          .WORD   016003                  ;8  BIT DYNAMIC MODE 4/16K
13882  036374  014003                          .WORD   014003                  ;8  BIT BYNAMIC MODE 64K
13883  036376  000000                          .WORD   0                       ;TABLE TERMINATOR
13884
13885                                          ;EXPECTED T-11 STARTING ADDRESS TABLE
13886
13887  036400  140000                  15$:    .WORD   140000
13888  036402  100000                          .WORD   100000
13889  036404  040000                          .WORD   040000
13890  036406  020000                          .WORD   020000
13891  036410  010000                          .WORD   010000
13892  036412  000000                          .WORD   000000
13893  036414  173000                          .WORD   173000
13894  036416  172000                          .WORD   172000
13895
13896                                          ;ADDRESSES TO BE LOADED INTO NEW FORCE JUMP ADDRESS REGISTER
13897
13898  036420  037777                          .WORD   037777
13899  036422  052525                          .WORD   052525
13900  036424  125252                          .WORD   125252
13901  036426  146314                          .WORD   146314
13902  036430  031463                          .WORD   031463
13903  036432  177777                          .WORD   177777
13904  036434  004777                          .WORD   004777
13905  036436  005777                          .WORD   005777
13906
13907  036440                          16$:    ENDTST
13908  036440                          L10101:
13909  036440  104401                          TRAP    C$ETST
13910
13911  036442                                  ENDMOD
13912
```

```
13913                                   .TITLE PARAMETER CODING
13914
13915                                   .SBTTL  HARDWARE PARAMETER CODING SECTION
13916
13917  036442                                   BGNMOD
13918
13919                                   ;++
13920                                   ; THE HARDWARE PARAMETER CODING SECTION CONTAINS MACROS
13921                                   ; THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
13922                                   ; MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
13923                                   ; INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
13924                                   ; MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
13925                                   ; WITH THE OPERATOR.
13926                                   ;--
13927
13928  036442                                   BGNHRD
13929  036442  000015                           .WORD L10102-L$HARD/2
13930  036444                           L$HARD::
13931
13932                                   ;
13933                                   ;HARDWARE P-TABLE QUESTIONS
13934                                   ;
13935                                   ;       ASK FOR CDS TARGET EMULATOR CSR ADDRESS
13936                                   ;       ASK FOR CDS TARGET EMULATOR VECTOR ADDRESS
13937                                   ;       ASK FOR CDS TARGET EMULATOR DEVICE NUMBER
13938                                   ;
13939
13940  036444                                   GPRMA   MSG1,0,0,0,177777,YES
13941  036444  000031                           .WORD   T$CODE
13942  036446  036476                           .WORD   MSG1
13943  036450  000000                           .WORD   T$LOLIM
13944  036452  177777                           .WORD   T$HILIM
13945  036454                                   GPRMA   MSG2,2,0,0,000774,YES
13946  036454  001031                           .WORD   T$CODE
13947  036456  036512                           .WORD   MSG2
13948  036460  000000                           .WORD   T$LOLIM
13949  036462  000774                           .WORD   T$HILIM
13950  036464                                   GPRMD   MSG3,4,0,177777,0,000017,YES
13951  036464  002032                           .WORD   T$CODE
13952  036466  036531                           .WORD   MSG3
13953  036470  177777                           .WORD   177777
13954  036472  000000                           .WORD   T$LOLIM
13955  036474  000017                           .WORD   T$HILIM
13956
13957
13958
13959  036476                                   ENDHRD
13960                                           .EVEN
13961  036476                           L10102:
```

```
13962
13963                                   ;
13964                                   ;HARDWARE P-TABLE MESSAGES
13965                                   ;
13966
13967  036476  051503  020122  042101  MSG1:   .ASCIZ  /CSR ADDRESS/
13968  036504  051104  051505  000123
13969  036512  042526  052103  051117  MSG2:   .ASCIZ  /VECTOR ADDRESS/
13970  036520  040440  042104  042522
13971  036526  051523     000
13972  036531     104  053105  041511  MSG3:   .ASCIZ  /DEVICE NUMBER/
13973  036536  020105  052516  041115
13974  036544  051105     000
13975          036550                   .EVEN
13976
13977                                   .SBTTL  SOFTWARE PARAMETER CODING SECTION
13978
13979                                   ;++
13980                                   ; THE SOFTWARE PARAMETER CODING SECTION CONTAINS MACROS
13981                                   ; THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
13982                                   ; MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
13983                                   ; INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
13984                                   ; MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
13985                                   ; WITH THE OPERATOR.
13986                                   ;--
13987
13988  036550                           BGNSFT
13989  036550  000000                   .WORD L10103-L$SOFT/2
13990  036552                   L$SOFT::
13991
13992
13993                                   .EVEN
13994
13995  036552                           ENDSFT
13996                                   .EVEN
13997  036552                   L10103:
13998
13999
14000
14001  036552                   $PATCH::
14002  036552  000030                   .BLKW   30
14003
14004
14005  036632                           LASTAD
14006                                   .EVEN
14007  036632  036650                   .WORD T$FREE
14008  036634  000005                   .WORD T$SIZE
14009  036636                   L$LAST::
14010  036636                           ENDMOD
14011
14012
14013
14014  036636                           BGNSETUP        1.
14015  036636                           BGNPTAB
14016  036636  000000                   .WORD   0
14017  036640  000003                   .WORD   L10106-./2-1
```

```
14018  036642
14019  036642  163010                    L10104:
                                                .WORD   163010
14020  036644  000370                            .WORD   370
14021  036646  000002                            .WORD   2
14022  036650                                    ENDPTAB
14023  036650                            L10106:
14024  036650                                    ENDSETUP
14025          000001                    .END
```

```
ADALRG  002513 G    1901#  2577  2600  3144  3154  3583  3600  3633  3651  3681  3713  4895  5343
                    5819   6340  6368  6492  6562  6675  6716  6747  6886  7253  9292  9472  9628
                    9860  10310 10414 10553 10715 10779 10807 11416 11841 11902 11992 12343 12449
                   12484  12597 12819 12907 13103 13238 13396 13674 13769 13859
ADAL0 = 000001 G    1700#  2569  3138  3148  5337  5813  9854 10709
ADAL1 = 000002 G    1699# 13763
ADAL10= 002000 G    1688#  9286  9622  9854 10709 10773 10801 11410 11835 13763
ADAL11= 004000 G    1687#
ADAL12= 010000 G    1686#  4889  9622 13763
ADAL13= 020000 G    1685#  9286  9466  9854 10304 10408 13763
ADAL14= 040000 G    1683#
ADAL15= 100000 G    1682#
ADAL2 = 000004 G    1698# 13763
ADAL3 = 000010 G    1697#
ADAL4 = 000020 G    1695#  6334  6880 11986 12591
ADAL5 = 000040 G    1693#  6880  7247 13511
ADAL6 = 000100 G    1692#
ADAL7 = 000200 G    1691# 12337 12443 12478 12591
ADAL8 = 000400 G    1690#  3687  3718  6362  6486  6556  6669  6710  6741 12813 12901 13097
ADAL9 = 001000 G    1689# 11896
ADDRRG  002735 G    1936#  4526  4550  4629  4653  4736  4821  5051  5136  5327  5803  7546  8257
                    9843
ADDR0 = 000001 G    1804#
ADDR1 = 000002 G    1803#
ADDR10= 002000 G    1794#
ADDR11= 004000 G    1793#
ADDR12= 010000 G    1792#
ADDR13= 020000 G    1791#
ADDR14= 040000 G    1790#
ADDR15= 100000 G    1789#
ADDR2 = 000004 G    1802#
ADDR3 = 000010 G    1801#
ADDR4 = 000020 G    1800#
ADDR5 = 000040 G    1799#
ADDR6 = 000100 G    1798#
ADDR7 = 000200 G    1797#
ADDR8 = 000400 G    1796#  4826
ADDR9 = 001000 G    1795#
ADR   = 000020 G    1632#
ASSEMB= 000010      1363
BIT0  = 000001 G    1605#  1671  1700  1721  1747  1769  1782  1804
BIT00 = 000001 G    1594#  1605
BIT01 = 000002 G    1593#  1604
BIT02 = 000004 G    1592#  1603
BIT03 = 000010 G    1591#  1602
BIT04 = 000020 G    1590#  1601
BIT05 = 000040 G    1589#  1600
BIT06 = 000100 G    1588#  1599
BIT07 = 000200 G    1587#  1598
BIT08 = 000400 G    1586#  1597
BIT09 = 001000 G    1585#  1596
BIT1  = 000002 G    1604#  1670  1699  1720  1746  1768  1781  1803
BIT10 = 002000 G    1584#  1660  1688  1711  1732  1759  1794
BIT11 = 004000 G    1583#  1659  1687  1710  1731  1757  1793
BIT12 = 010000 G    1582#  1657  1686  1709  1730  1756  1792
BIT13 = 020000 G    1581#  1656  1685  1708  1729  1755  1791 13865
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BIT15 = 100000 G      1579#  1649  1682  1706  1727  1753  1789
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BIT3  = 000010 G      1602#  1668  1697  1718  1742  1766  1779  1801
BIT4  = 000020 G      1601#  1667  1695  1717  1741  1765  1778  1800
BIT5  = 000040 G      1600#  1666  1693  1716  1740  1764  1777  1799
BIT6  = 000100 G      1599#  1665  1692  1715  1739  1763  1776  1798
BIT7  = 000200 G      1598#  1664  1691  1714  1738  1762  1775  1797
BIT8  = 000400 G      1597#  1662  1690  1713  1737  1761  1796  4451  9562
BIT9  = 001000 G      1596#  1661  1689  1712  1733  1760  1795
BOE   = 000400 G      1636#
BRKRES  007772 G      3136#  6824  7028  7140  7190  7343  7558  8270  9009  12695  13136  13512  13683
CLRPSM  007712 G      3105#  5061  5219  5352  5395  5828  6244  6353  6785  6869  7098  7141  7193
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C$BRK = 000022        1363#
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C$CLEA= 000012        1363#  3327
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                      8260   8311  8369  8404  8434  8476  8510  8541  8578  8608  8656  8687  8728
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C$DCLN= 000044      1363#
C$DODU= 000051      1363#
C$DRPT= 000024      1363#
C$DU  = 000053      1363#    3348
C$EDIT= 000003      1363#    1425
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C$GMAN= 000043       1363#
C$GPHR= 000042       1363#   3252
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C$PNTF= 000017       1363#
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C$QIO = 000377       1363#
C$RDBU= 000007       1363#
C$REFG= 000047       1363#   3216    3221    3226    3240    3246
C$RESE= 000033       1363#   3230   13335   13567
C$REVI= 000003       1363#   1424
C$RFLA= 000021       1363#
C$RPT = 000025       1363#   3187
C$SEFG= 000046       1363#
C$SPRI= 000041       1363#   3271    3312   12668   12726   12804   12860   12935   12959   12996   13062   13143   13165
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C$SVEC= 000037       1363#   2398    2482    2567    2635    3236   12716   13341   13573
C$TPRI= 000013       1363#
DFPTBL  002260 G     1534#
DIAGMC= 000000       1363
EDBRK = 000020 G     1676#
EF.CON= 000036 G     1612#   3245
EF.NEW= 000035 G     1613#   3239
EF.PWR- 000034 G     1614#   3225
EF.RES= 000037 G     1611#   3220
EF.STA= 000040 G     1610#   3215
EMSGR0  004156 G     2059#   2141
EMSGR2  004206 G     2063#   2150
EMSGR4  004236 G     2067#   2159
EMSGR6  004266 G     2071#   2168    2177
EOAIFD  002676 G     1930#   4445    9317    9405   10453   10496   10680   11140   11169   13725
EPBLK   002276 G     1819#
ERRMSG  002274 G     1818#
ERRNBR  002272 G     1817#
ERRTYP  002270 G     1816#
EVL   = 000004 G     1630#
E$END = 002100       1363#
E$LOAD= 000035       1363#   1448
FDALEI  003722 G     2026#  10538   10598
FDALEO  003666 G     2021#  10516
FDALRG  002653 G     1926#   4261    4281    4327    4347    4391   13312   13470
FDALO = 000001 G     1782#   4420   10674   11134   13719
FDAL1 = 000002 G     1781#  11134   11163
FDAL2 = 000004 G     1780#  10621
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FJAADR  003501 G          2001#  10129
FJADRG  002766 G          1941#   5118    5209   13846
FJAEID  003446 G          1996#  10110
FJATDL  003536 G          2006#  10203   10270   10355
FJSTAD  004060 G          2042#  13812
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FRMTR2  004437 G          2090#   2284    2321
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F$AUTO= 000020            1363#   3294    3298
F$BGN = 000040            1363#   1370    1563    1568    2139    2148    2157    2166    2175    2184    2196    2208    2220
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F$DU  = 000016            1363#   3336    3347
F$END = 000041            1363#   1370    1563    1568    2146    2155    2164    2173    2182    2194    2206    2218    2230
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F$HARD- 000004            1363#   13929   13960
F$HW  = 000013            1363#   1532    1542
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F$MOD = 000000          1363#  1370  1563  1568  3163  3168  3374  3380  13912 13918 14011
F$MSG = 000011          1363#  2139  2144  2148  2153  2157  2162  2166  2171  2175  2180  2184  2192
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F$PWR = 000017          1363#
F$RPT = 000012          1363#  3175  3186
F$SEG = 000003          1363#  2392  2430  2436  2447  2455  2510  2518  2547  2551  2619  2623  2673
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                        3640   3654  3675  3684  3707  3716  3743  3758  3792  3812  3816  3831  3856
                        3877   3882  3898  3925  3944  3973  3992  4018  4038  4043  4058  4084  4104
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                        4350   4376  4394  4423  4448  4482  4529  4533  4553  4585  4632  4636  4656
                        4691   4739  4776  4824  4851  4966  5001  5221  5267  5695  5741  6247  6287
                        6788   6818  7290  7320  7451  7486  8144  8194  8941  8980  9210  9237  9559
                        9591   9744  9785  10358 10394 10618 10643 11349 11369 11784 11808 12638 12661
                        13197  13663 13862
F$SOFT= 000005          1363#  13989 13996
F$SRV = 000010          1363#  2720  2724
F$SUB = 000002          1363#  13227 13473 13482 13631
F$SW  = 000014          1363#  1554  1560
F$TEST= 000001          1363#  3419  3425  3438  3474  3487  3525  3538  3558  3570  3606  3619  3657
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                        4371   4399  4419  4454  4479  4556  4582  4659  4687  4744  4772  4829  4846
                        4982   4996  5237  5262  5711  5736  6263  6284  6791  6816  7293  7317  7454
                        7481   8161  8189  8959  8977  9213  9233  9566  9586  9760  9780  10374 10390
                        10627  10641 11352 11366 11787 11806 12641 12658 13200 13217 13635 13655 13908
GDALRG  002406 G        1885#  2414  2444  2463  2526  2616  2742  2762  2784  2804  2824  2844  2864
                        2884   3451  3468  3501  3519  3549  6383  6426  6463  6506  6577  6624  6935
                        6986   7008  7039  7075  7115  7151  7179  7204  7224  7272  12757 12834 12887
                        12921  12971 12981 13023 13041 13051 13088 13154 13327 13368 13383 13559 13600
                        13628
GDAL0 = 000001 G        1671#  2457  2736  2778  2818  2858  13320 13321
GDAL1 = 000002 G        1670#  2457  2736  2818  2838  2878  13320 13321
GDAL10= 002000 G        1660#
GDAL11= 004000 G        1659#
GDAL12= 010000 G        1657#
GDAL13= 020000 G        1656#
GDAL14= 040000 G        1655#
GDAL15= 100000 G        1649#  2437  3268  13321
GDAL2 = 000004 G        1669#  2520  2756  2818  2858  2878  13320 13321
GDAL3 = 000010 G        1668#  12751 12965 12975 13035 13045 13082 13148
GDAL4 = 000020 G        1667#  1676
GDAL5 = 000040 G        1666#  1675
GDAL6 = 000100 G        1665#  1674
GDAL7 = 000200 G        1664#  1673  13553
GDAL8 = 000400 G        1662#
GDAL9 = 001000 G        1661#
G$CNTO= 000200          1363#
G$DELM= 000372          1363#
G$DISP= 000003          1363#
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G$RADO= 000020          1363#  13941  13946  13951
G$XFER= 000004          1363#
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HDALRG  002605 G        1918#   2494   2913   2934   2964   2985   3013   3033   3061   3081   3809   3828   3874
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                        7366    7525   8233   9036   9269   9823  10232  10330  10433  10475  10576  10615  10698
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                       11611   11744  11823  12239  12302  12503  12550  12684  13291  13429  13706
HDAL0 - 000001 G        1747#  10226  10323
HDAL1 = 000002 G        1746#
HDAL10= 002000 G        1732#
HDAL11= 004000 G        1731#
HDAL12= 010000 G        1730#   2907   2928   5996   8447  10744  10919  10978  11199
HDAL13= 020000 G        1729#   2958   2979   5512   5628   5996   6168   7727   7835   7953   8070   8447   8617
                        8737    8857  10089  10155  10744  10978  11199
HDAL14- 040000 G        1728#
HDAL15= 100000 G        1727#   3007   3027  10155  10569
HDAL2 = 000004 G        1743#   2484   2907   2927   2958   3007   3026   3055   3074   5018   5077   5175   5300
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                        7835    7953   8070   8227   8344   8447   8617   8737   8857   9030   9263   9335   9420
                        9524    9610   9721   9817   9921  10089  10155  10214  10323  10427  10469  10569  10609
                       10692   10744  10978  11199  11331  11396  11434  11467  11563  11605  11644  11691  11738
                       11817   12678
HDAL3 - 000010 G        1742#  10569  10744  10832  10865  10978
HDAL4 = 000020 G        1741#  10744  10864  10896  10978  11000
HDAL5 - 000040 G        1740#  10226  10323  10324  11067  11226  11256  11467  11563  11605  11644  11691
HDAL6 = 000100 G        1739#  10226  10323  10469  10569  11099  11226  11256  11434  11563  12233  12296  12497
                       12544
HDAL7 = 000200 G        1738#   3055   3075   9721  10214
HDAL8   000400 G        1737#   3947   3994
HDAL9   001000 G        1733#   4495   4598   4704   4789   5018   5077   5175   5300   5425   5512   5628   5774
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                        8737    8857   9817   9921
HELP    000000          1361#   1363   1378   1466   1522   1540   1558  1563#   1566   1574   1813   1867   2055
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HOE   - 100000 G        1643#
IBE   = 010000 G        1640#
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IDTYPE  002316 G        1833#   2438  3268*  13319
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IEODAL  003034 G        1948#   5498   5978   7714   7822   8431   8605
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                    4846   4996   5262   5736   6284   6816   7317   7481   8189   8977   9233   9586   9780
                   10390  10641  11366  11806  12658  13218  13656
INTSRV  006724 G    2720#  12713
ISR    = 000100 G   1634#
IXE    = 004000 G   1639#
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I$AUTO= 000041      1363#  3294#  3300#
I$CLN  = 000041     1363#  3309#  3319   3328#
I$DU   = 000041     1363#  3336#  3349#
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I$PWR  = 000041     1363#
I$RPT  = 000041     1363#  3175#  3188#
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                    2869#  2877#  2889#  2906#  2918#  2926#  2939#  2957#  2969#  2977#  2990#  3006#  3018#
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J$JMP  - 000167     1363#  3179   3340   3363
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                  10305 10409 10548 10710 10774 10802 11411 11836 11897 11987 12338 12444 12479
                  12592 12814 12902 13098 13233 13669 13764 13854
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                  11227 11257 11332 11378 11397 11435 11468 11564 11606 11623 11668 11722 11739
                  11818 12234 12297 12498 12545 12679 13253 13286 13307 13701 13720 13740
LDRDOR  006562 G   2439  2685#  13322
LDRD4R  006646 G   2703#  5145  5438  5854  5912  6728  7404  7650  8303  8361  9936  11277  11294
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LOT   = 000010 G   1631#
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L$AU    010336 G   3359#
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L$AUTO  010276 G   1456  3294#
L$CCP   002106 G   1453#
L$CLEA  010300 G   1454  3309#
L$CO    002032 G   1409#
L$DEPO  002011 G   1391#
L$DESC  002360 G   1446  1871#
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L$DEVP  002060 G   1431#
L$DISP  002124 G   1416  1475#
L$DLY   002116 G   1461#
L$DTP   002040 G   1415#
L$DTYP  002034 G   1411#
L$DU    010330 G   3336#
L$DUT   002072 G   1441#
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L$ENVI  002044 G   1419#
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L$EXP5  002066 G   1437#
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L$HIME  002120 G   1463#
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L$LUN   002074 G    1443#
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L$PRIO  002042 G    1417#
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L$PRT   002112 G    1457#
L$REPP  002062 G    1433#
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L$RPT   010052 G    3175#
L$SOFT  036552 G   13989   13990#
L$SPC   002056 G    1429#
L$SPCP  002020 G    1399#
L$SPTP  002024 G    1403#
L$STA   002030 G    1407#
L$SW    002270 G    1554    1555#
L$TEST  002114 G    1459#
L$TIML  002014 G    1395#
L$UNIT  002012 G    1393#
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L10001  002270      1554    1560#
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L10003  005002      2153#
L10004  005016      2162#
L10005  005032      2171#
L10006  005046      2180#
L10007  005070      2192#
L10010  005112      2204#
L10011  005134      2216#
L10012  005156      2228#
L10013  006736      2724#
L10014  010056      3180    3186#
L10016  010274      3276    3282#
L10017  010276      3298#
L10020  010326      3320    3326#
L10021  010334      3341    3347#
L10022  010342      3364    3370#
L10023  010350      3425#
L10024  010434      3474#
L10025  010522      3525#
L10026  010572      3558#
L10027  010656      3606#
L10030  010744      3657#
L10031  011014      3690#
L10032  011060      3721#
L10033  011156      3771#
L10034  011246      3834#
L10035  011340      3902#
L10036  011414      3950#
L10037  011464      3997#
L10040  011554      4062#
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L10042  011722      4176#
L10043  011772      4223#
L10044  012070      4288#
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L10046  012244           4399#
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L10055  013660           5237#
L10056  014566           5711#
L10057  015560           6263#
L10060  016750           6791#
L10061  020044           7293#
L10062  020314           7454#
L10063  021602           8161#
L10064  023154           8959#
L10065  023532           9213#
L10066  024354           9566#
L10067  024704           9760#
L10070  026130          10374#
L10071  026644          10627#
L10072  030564          11352#
L10073  031574          11787#
L10074  033330          12641#
L10075  034544          13200#
L10076  035714          13635#
L10077  035360          13473#
L10100  035712          13631#
L10101  036440          13908#
L10102  036476          13929   13961#
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MR10    = 002000 G       1759#   11622   11667   11721
MR11    = 004000 G       1757#    7496    8204    8990   10964
MR12    = 010000 G       1756#
MR13    = 020000 G       1755#
MR14    = 040000 G       1754#
MR15    = 100000 G       1753#
MR2     = 000004 G       1767#
MR3     = 000010 G       1766#
MR4     = 000020 G       1765#
MR5     = 000040 G       1764#
MR6     = 000100 G       1763#
MR7     = 000200 G       1762#
MR8     = 000400 G       1761#   4173    4220
MR9     = 001000 G       1760#   9486   11667
MSBRK   = 000040 G       1675#
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MSGTM2  004547 G   2103#  2198
MSGTM4  004623 G   2111#  2210
MSGTM6  004677 G   2119#  2222
MSG1    036476    13942  13967#
MSG2    036512    13947  13969#
MSG3    036531    13952  13972#
MTOTMR  003335 G   1983#  9741
NOINT   002467 G   1894#  12872  13008
NOPSM   003773 G   2033#  13790
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                   13916
O$APTS= 000000     1363#  1407
O$AU  = 000000     1363#  1439
O$BGNR= 000000     1363#  1433
O$BGNS= 000000     1363#  1399
O$DU  = 000000     1363#  1441
O$ERRT= 000000     1363#  1449
O$GNSW= 000000     1363#  1403
O$POIN= 000001     1363#  1377#  1465
O$SETU= 000001     1363#  1377#  1393   14007
PNT   = 001000 G   1637#
PRI   = 002000 G   1638#
PRI00 = 000000 G   1626#  12725  12859  12934  12995  13061  13164
PRI01 = 000040 G   1625#
PRI02 = 000100 G   1624#
PRI03 = 000140 G   1623#
PRI04 = 000200 G   1622#
PRI05 = 000240 G   1621#
PRI06 = 000300 G   1620#
PRI07 = 000340 G   1418   1619#  2394   2478   2563   2631   2726   3270   3311   12667  12712  12803  12958
                  13142  13186  13337  13569
PRNTBS  005160 G   2140   2149   2158   2167   2176   2233#
PRNTR0  005230 G   2142   2243   2249   2256#
PRNTR2  005306 G   2151   2250   2275#
PRNTR4  005360 G   2160   2293#
PRNTR6  005436 G   2244   2251   2312#
PR026R  005212 G   2178   2249#
PR06R   005200 G   2169   2243#
READR0  006570 G   2686#  6378   6421   6458   6501   6572   6619   6930   6981   7003   7034   7070   7110
                   7146   7174   7199   7219   7267   12829  12916  13378  13554  13623
READR2  006622 G   2695#  13391
READR4  006654 G   2704#  5090   5181   5380   5465   5537   5565   5657   5680   5945   6014   6047   6076
                   6110   6199   6224   6392   6436   6472   6595   6634   6656   6697   6770   6945   6968
                   7015   7047   7082   7125   7435   7590   7679   7755   7787   7864   7893   7981   8011
                   8102   8128   8396   8468   8502   8533   8570   8648   8679   8767   8799   8891   8919
                   9067   9096   9122   9148   9174   9193   9972   10005  10033  10242  10758  10789  10816
                  10847  10879  10902  10925  10947  10985  11015  11036  11054  11082  11115  11151  11180
                  11209  11242  11319  11450  11482  11520  11591  11651  11699  11767  11882  11933  11971
                  12035  12068  12107  12138  12166  12192  12220  12258  12283  12321  12367  12394  12429
                  12465  12531  12570  12622  13404  13540  13609
READR6  006700 G   2712#  4913   4958   5113   5204   5493   5610   5973   6150   7709   7816   7936   8053
                   8426   8599   8720   8840   9381   9451   9551   9659   9682   9701   9736   10068  10105
                  10124  10198  10265  10291  10350  10491  10511  10533  10593  13424  13444  13465  13807
REGO    002300 G   1825#  2406*  2407   2685*  2686   2721   3256   3313*  6611   13343  13575
REGOEQ  004316 G   2075#  2257
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REG2     002302 G  1826# 2570* 2571  2694* 2695  3315*
REG2EQ   004330 G  2077# 2276
REG4     002304 G  1827# 2639* 2640  2703* 2704  13781
REG4EQ   004342 G  2079# 2294
REG6     002306 G  1828# 2486* 2487  2711* 2712  5373*  5845*  7583*  8294*  9370*  9444*  13829*  13838
REG6EQ   004354 G  2081# 2313
ROBAD    002326 G  1838# 2263  2407* 2408* 2409  2686*  2687*  2688   2721*  12882  13018
ROEROR   004754 G  2139# 2415  2445  2464  2527  2617   2743   2763   2785   2805   2825   2845   2865
                   2885  3452  3469  3502  3520  3550   6384   6427   6464   6507   6578   6625   6936
                   6987  7009  7040  7076  7116  7152   7180   7205   7225   7273   12742  12758  12772
                   12794 12835 12849 12873 12888 12922  12950  12972  12982  13009  13024  13042  13052
                   13075 13089 13126 13155 13178 13328  13369  13384  13560  13601  13629
ROGOOD   002322 G  1836# 2264  2405* 2409  2438* 2684*  2688   6377*  6500*  6618*  6929*  7033*  7109*
                   7145* 7173* 7198* 12828* 12882 12915*  13018  13119*  13137*  13319*  13320*  13376*  13377
                   13553* 13622*
ROLOAD   002320 G  1835# 2265  2404* 2405  2406  2437*  2456*  2457*  2519*  2520*  2610*  2684   2685
                   2736* 2756* 2778* 2798* 2818* 2838*  2858*  2878*  3445*  3462*  3495*  3513*  3540*
                   3554* 3555  12751* 12965* 12975* 13035*  13045*  13082*  13148*  13321*  13362*  13377*  13594*
ROMASK   002324 G  1837# 2403* 2408  2609* 2676* 2687
ROTM     005050 G  2184# 2425
RO26ER   005034 G  2175# 4919  4964  9387  9457  9557   9665   9688   9707   9742   10111  10130  10204
                   10271 10297 10356 10539 10599 13791  13813  13847
RO6ERR   005020 G  2166# 2495  2545  2914  2935  2963   2986   3014   3034   3062   3082   3810   3829
                   3875  3896  3942  3990  4036  4056   4102   4122   4168   4216   4262   4282   4328
                   4348  4392  4446  4502  4527  4551   4605   4630   4654   4711   4737   4796   4822
                   4881  4942  5025  5052  5119  5137   5210   5285   5307   5328   5499   5616   5759
                   5781  5804  5979  6156  6303  6322   6841   6859   7335   7367   7504   7526   7547
                   7715  7823  7942  8059  8212  8234   8258   8432   8606   8726   8846   8997   9037
                   9252  9270  9318  9406  9493  9646   9802   9824   9844   10074  10233  10331  10434
                   10454 10476 10497 10517 10577 10616  10660  10681  10699  10751  10839  10872  10971
                   11007 11074 11106 11141 11170 11233  11263  11338  11384  11403  11441  11474  11570
                   11612 11629 11674 11728 11745 11824  12240  12303  12504  12551  12685  13259  13292
                   13313 13430 13450 13471 13707 13726  13746
R2EROR   004770 G  2148# 2578  2601  3145  3155  3584   3601   3634   3652   3682   3714   4896   5344
                   5820  6341  6369  6493  6563  6676   6717   6748   6887   7254   9293   9473   9629
                   9861  10311 10415 10554 10716 10780  10808  11417  11842  11903  11993  12344  12450
                   12485 12598 12820 12908 13104 13239  13397  13675  13770  13860
R2LOAD   002330 G  1840# 2283  2569* 2570  2572  2594*  2694   2696   3138*  3148*  3577*  3594*  3627*
                   3645* 3672* 3686* 3687  3704* 3718*  4889*  5337*  5813*  6334*  6362*  6486*  6556*
                   6669* 6710* 6741* 6823* 6880* 7247*  7342*  7557*  8269*  9008*  9286*  9466*  9622*
                   9854* 10304* 10408* 10547* 10709* 10773*  10801*  11410*  11835*  11896*  11986*  12337*  12443*
                   12478* 12591* 12694* 12813* 12901* 13097*  13135*  13232*  13390*  13511*  13668*  13763*  13853*
R2READ   002332 G  1841# 2282  2571* 2572  2695* 2696
R2TM     005072 G  2196# 2588
R4BAD    002340 G  1845# 2300  2640* 2641  2704* 2705
R4EROR   005004 G  2157# 2647  2671  3114  3124  3756   5096   5151   5187   5386   5444   5471   5543
                   5571  5663  5686  5860  5918  5951   6020   6053   6082   6116   6205   6230   6398
                   6442  6478  6521  6547  6601  6640   6662   6703   6734   6776   6901   6951   6974
                   7021  7053  7088  7131  7239  7288   7380   7410   7441   7596   7656   7685   7761
                   7793  7870  7899  7987  8017  8108   8134   8309   8367   8402   8474   8508   8539
                   8576  8654  8685  8773  8805  8897   8925   9073   9102   9128   9154   9180   9199
                   9508  9881  9942  9978  10011 10039  10181  10248  10764  10795  10822  10853  10885
                   10908 10931 10953 10991 11021 11042  11060  11088  11121  11157  11186  11215  11248
                   11283 11300 11325 11456 11488 11526  11543  11553  11597  11657  11705  11773  11888
                   11939 11977 12009 12041 12074 12113  12144  12172  12198  12226  12264  12289  12327
                   12373 12400 12435 12471 12537 12576  12628  13272  13410  13500  13546  13615
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                   5564*  5656*  5679*  5852*  5853*  5910*  5911*  5944*  6046*  6108*  6109*  6198*  6223*
                   6633*  6655*  6695*  6696*  6727*  6768*  6769*  6944*  6967*  7124*  7402*  7403*  7589*
                   7648*  7649*  7678*  7785*  7786*  7891*  7892*  8009*  8010*  8101*  8127*  8301*  8302*
                   8359*  8360*  8395*  8501*  8568*  8569*  8677*  8678*  8797*  8798*  8890*  8918*  9066*
                   9095*  9121*  9147*  9173*  9934*  9935*  9970*  9971*  10031*  10032*  10241*  10757*  10788*
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                   11275*  11276*  11292*  11293*  11317*  11318*  11449*  11481*  11519*  11698*  11766*  11932*  11969*
                   11970*  12002*  12033*  12034*  12067*  12137*  12165*  12191*  12256*  12257*  12282*  12320*  12366*
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R4LOAD  002334 G   1843#  2302   2637*  2638   2639   2664*  2702   2703   3107*  3117*  3739*  3763*  3765
                   3768*  5060*  5143*  5218*  5351*  5394*  5435*  5436   5827*  5851*  5852   5909*  5910
                   6243*  6352*  6514*  6540*  6726*  6784*  6868*  6894*  7192*  7232*  7281*  7349*  7373*
                   7401*  7402   7447*  7564*  7604*  7647*  7648   8276*  8300*  8301   8358*  8359   8937*
                   9016*  9206*  9278*  9501*  9596*  9868*  9874*  9933*  9934   10145*  10174*  10401*  10725*
                   11274*  11275  11291*  11292  11345*  11426*  11536*  11546*  11712*  11780*  11868*  12001*  12084*
                   12634*  12704*  13265*  13488*  13493*  13690*
R4TM    005114 G   2208#  2658
R6LOAD  002342 G   1847#  2320   2484*  2486   2489   2538*  2711   2714   2907*  2927*  2928*  2958*  2978*
                   2979*  3007*  3026*  3027*  3055*  3074*  3075*  3803*  3822*  3868*  3889*  3922*  3946*
                   3947   3970*  3994*  4029*  4049*  4095*  4115*  4148*  4172*  4173   4196*  4220*  4255*
                   4275*  4321*  4341*  4372*  4396*  4420*  4451*  4495*  4520*  4544*  4598*  4623*  4647*
                   4704*  4730*  4789*  4815*  4862*  4874*  4912*  4935*  4957*  5018*  5045*  5077*  5112*
                   5130*  5175*  5202*  5278*  5300*  5321*  5425*  5492*  5512*  5609*  5628*  5752*  5774*
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                   8070*  8204*  8227*  8251*  8344*  8424*  8447*  8597*  8617*  8716*  8718*  8737*  8836*
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                   13700*  13719*  13738*  13739*  13806*  13835*  13839
R6MASK  002346 G   1849#  2485*  2488   2677*  2713   4254*  4320*  4373*  7497*  7708*  7728*  7815*  7836*
                   7935*  7954*  8052*  8071*  8205*  8425*  8448*  8598*  8618*  8719*  8738*  8839*  8858*
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R6READ  002344 G   1848#  2319   2487*  2488*  2489   2712*  2713*  2714   13838*  13839
R6TM    005136 G   2220#  2505
SEIDAL  007240 G   2876#  9671   10094  10187  10254  10337  10523  10583
SELTMR  007206 G   2856#  9726
SEODAL  007122 G   2816#  4905   4948   5480   5580   5960   6125   7694   7802   7908   8026   8411   8585
                   8694   8814   9652   10048  10277  10503
SFPTBL  002270 G   1556#
SLDADR  007072 G   2796#  4509   4612   4719   4804   5033   5125   5315   5789   7534   8242   9694   9832
                   10117
SLFDAL  007154 G   2836#  4248   4314   4381   4428   9299   9361   9437   9542   10440  10482  10666  11127
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SLFJAR  007040 G   2776#  5105   5195   5360   5836   7572   8284   13802
SLHDAL  006754 G   2734#  3797   3861   3930   3978   4487   4590   4696   4781   4855   4925   5007   5066
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                   7611   7722   7830   7949   8066   8219   8317   8439   8613   8733   8853   9023   9258
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                     8985    9241    9479    9635    9790   10647   10959   11373   11618   11663   11717   13246   13437
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SSBRK = 000200 G     1673#   2403    6929    7033    7109    7145    7173    7198
SVCGBL= 000000       1363#   1380    1381    1389    1390    1391    1392    1393    1394    1395    1396    1397    1398
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                     2197    2208    2209    2220    2221    2720    2721    3175    3176    3197    3198    3213    3214
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                    14010
SVCINS= 000000       1363#   1381    1382    1383    1384    1385    1386    1387    1388    1389    1390    1391    1392
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3073	3074	3079	3080	3081	3082	3083	3085	3086	3106	3107	3111	3112
3113	3114	3115	3116	3117	3121	3122	3123	3124	3125	3127	3128	3137
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T$SEGL= 177777      1363#  2392#  2430#  2432   2436#  2447#  2449   2455#  2510#  2512   2518#  2547#  2549
                    2551#  2619#  2621   2623#  2673#  2675   2735#  2745#  2747   2755#  2765#  2767   2777#
                    2787#  2789   2797#  2807#  2809   2817#  2827#  2829   2837#  2847#  2849   2857#  2867#
                    2869   2877#  2887#  2889   2906#  2916#  2918   2926#  2937#  2939   2957#  2967#  2969
```

```
                    2977#  2988#  2990   3006#  3016#  3018   3025#  3036#  3038   3054#  3064#  3066   3073#
                    3084#  3086   3106#  3126#  3128   3137#  3157#  3159   3441#  3454#  3456   3458#  3471#
                    3473   3490#  3504#  3506   3508#  3522#  3524   3543#  3552#  3554   3573#  3586#  3588
                    3590#  3603#  3605   3622#  3636#  3638   3640#  3654#  3656   3675#  3684#  3686   3707#
                    3716#  3718   3743#  3758#  3760   3792#  3812#  3814   3816#  3831#  3833   3856#  3877#
                    3879   3882#  3898#  3900   3925#  3944#  3946   3973#  3992#  3994   4018#  4038#  4040
                    4043#  4058#  4060   4084#  4104#  4106   4109#  4124#  4126   4151#  4170#  4172   4199#
                    4218#  4220   4243#  4264#  4266   4269#  4284#  4286   4309#  4330#  4332   4335#  4350#
                    4352   4376#  4394#  4396   4423#  4448#  4450   4482#  4529#  4531   4533#  4553#  4555
                    4585#  4632#  4634   4636#  4656#  4658   4691#  4739#  4741   4776#  4824#  4826   4851#
                    4966#  4968   5001#  5221#  5223   5267#  5695#  5697   5741#  6247#  6249   6287#  6788#
                    6790   6818#  7290#  7292   7320#  7451#  7453   7486#  8144#  8146   8194#  8941#  8943
                    8980#  9210#  9212   9237#  9559#  9561   9591#  9744#  9746   9785#  10358#  10360  10394#
                   10618#  10620  10643#  11349#  11351  11369#  11784#  11786  11808#  12638#  12640  12661#  13197#
                   13199   13663#  13862#  13864
T$SEKO= 010000      2392#  2430   2436#  2447   2455#  2510   2518#  2547   2551#  2619   2623#  2673   2735#
                    2745   2755#  2765   2777#  2787   2797#  2807   2817#  2827   2837#  2847   2857#  2867
                    2877#  2887   2906#  2916   2926#  2937   2957#  2967   2977#  2988   3006#  3016   3025#
                    3036   3054#  3064   3073#  3084   3106#  3126   3137#  3157   3441#  3454   3458#  3471
                    3490#  3504   3508#  3522   3543#  3552   3573#  3586   3590#  3603   3622#  3636   3640#
                    3654   3675#  3684   3707#  3716   3743#  3758   3792#  3812   3816#  3831   3856#  3877
                    3882#  3898   3925#  3944   3973#  3992   4018#  4038   4043#  4058   4084#  4104   4109#
                    4124   4151#  4170   4199#  4218   4243#  4264   4269#  4284   4309#  4330   4335#  4350
                    4376#  4394   4423#  4448   4482#  4529   4533#  4553   4585#  4632   4636#  4656   4691#
                    4739   4776#  4824   4851#  4966   5001#  5221   5267#  5695   5741#  6247   6287#  6788
                    6818#  7290   7320#  7451   7486#  8144   8194#  8941   8980#  9210   9237#  9559   9591#
                    9744   9785#  10358  10394#  10618  10643#  11349  11369#  11784  11808#  12638  12661#  13197
                   13663#  13862
T$SIZE= 000005      14008  14025#
T$SUBN= 000000      1363#  3418#  3437#  3486#  3537#  3569#  3618#  3669#  3701#  3737#  3788#  3852#  3919#
                    3967#  4014#  4080#  4145#  4193#  4239#  4305#  4370#  4418#  4478#  4581#  4686#  4771#
                    4845#  4995#  5261#  5735#  6283#  6815#  7316#  7480#  8188#  8976#  9232#  9585#  9779#
                   10389#  10640#  11365#  11805#  12657#  13216#  13226#  13481#  13654#
T$TAGL= 177777      1363#
T$TAGN= 010107      1363#  1532#  1554#  2139#  2148#  2157#  2166#  2175#  2184#  2196#  2208#  2220#  2720#
                    3175#  3197#  3213#  3294#  3309#  3336#  3359#  3419#  3438#  3487#  3538#  3570#  3619#
                    3670#  3702#  3738#  3789#  3853#  3920#  3968#  4015#  4081#  4146#  4194#  4240#  4306#
                    4371#  4419#  4479#  4582#  4687#  4772#  4846#  4996#  5262#  5736#  6284#  6816#  7317#
                    7481#  8189#  8977#  9233#  9586#  9780#  10390#  10641#  11366#  11806#  12658#  13217#  13227#
                   13482#  13655#  13929#  13989#  14015#  14016#  14017#
T$TEMP= 000000      1476#  1477#  1478#  1479#  1480#  1481#  1482#  1483#  1484#  1485#  1486#  1487#  1488#
                    1489#  1490#  1491#  1492#  1493#  1494#  1495#  1496#  1497#  1498#  1499#  1500#  1501#
                    1502#  1503#  1504#  1505#  1506#  1507#  1508#  1509#  1510#  1511#  1512#  1513#  1514#
                    1515#  1516#  1517#  1518#  1519#  1520#  1521#  1542#  1560#  1563#  2144#  2153#  2162#
                    2171#  2180#  2192#  2204#  2216#  2228#  2430#  2447#  2510#  2547#  2619#  2673#  2724#
                    2745#  2765#  2787#  2807#  2827#  2847#  2867#  2887#  2916#  2937#  2967#  2988#  3016#
                    3036#  3064#  3084#  3126#  3157#  3163#  3179#  3180   3186#  3204#  3275#  3276   3282#
                    3298#  3319#  3320   3326#  3340#  3341   3347#  3363#  3364   3370#  3374#  3425#  3454#
                    3471#  3474#  3504#  3522#  3525#  3552#  3558#  3586#  3603#  3606#  3636#  3654#  3657#
                    3684#  3690#  3716#  3721#  3758#  3771#  3812#  3831#  3834#  3877#  3898#  3902#  3944#
                    3950#  3992#  3997#  4038#  4058#  4062#  4104#  4124#  4128#  4170#  4176#  4218#  4223#
                    4264#  4284#  4288#  4330#  4350#  4354#  4394#  4399#  4448#  4454#  4529#  4553#  4556#
                    4632#  4656#  4659#  4739#  4744#  4824#  4829#  4966#  4982#  5221#  5237#  5695#  5711#
                    6247#  6263#  6788#  6791#  7290#  7293#  7451#  7454#  8144#  8161#  8941#  8959#  9210#
                    9213#  9239#  9566#  9744#  9760#  10358#  10374#  10618#  10627#  11349#  11352#  11784#  11787#
                   12638#  12641#  13197#  13200#  13473#  13631#  13635#  13862#  13908#  13912#  13941#  13946#  13951#
```

```
                    13960#  13996#  14011#
T$TEST= 000055       1363#   3418#   3437#   3486#   3537#   3569#   3618#   3669#   3701#   3737#   3788#   3852#   3919#
                     3967#   4014#   4080#   4145#   4193#   4239#   4305#   4370#   4418#   4478#   4581#   4686#   4771#
                     4845#   4995#   5261#   5735#   6283#   6815#   7316#   7480#   8188#   8976#   9232#   9585#   9779#
                    10389#  10640#  11365#  11805#  12657#  13216#  13226   13481   13654#  14010
T$TSTM= 177777       1363#   2145    2154    2163    2172    2181    2189    2193    2201    2205    2213    2217    2225
                     2229    2237    2260    2269    2279    2287    2297    2306    2316    2324    2392    2398    2412
                     2417    2422    2428    2431    2436    2442    2448    2455    2461    2466    2482    2492    2497
                     2502    2508    2511    2518    2524    2529    2542    2548    2551    2567    2575    2580    2585
                     2590    2593    2598    2603    2614    2620    2623    2635    2644    2649    2655    2660    2663
                     2668    2674    2735    2740    2746    2755    2760    2766    2777    2782    2788    2797    2802
                     2808    2817    2822    2828    2837    2842    2848    2857    2862    2866    2877    2882    2888
                     2906    2911    2917    2926    2932    2938    2957    2962    2968    2977    2983    2989    3006
                     3011    3017    3025    3031    3037    3054    3059    3065    3073    3079    3085    3106    3111
                     3116    3121    3127    3137    3142    3147    3152    3158    3187    3216    3221    3226    3230
                     3236    3240    3246    3252    3271    3275    3283    3299    3312    3319    3327    3348    3371
                     3426    3441    3449    3455    3458    3466    3472    3475    3490    3499    3505    3508    3517
                     3523    3526    3543    3547    3553    3559    3573    3581    3587    3590    3598    3604    3607
                     3622    3631    3637    3640    3649    3655    3658    3675    3679    3685    3691    3707    3711
                     3717    3722    3743    3753    3759    3772    3792    3807    3813    3816    3826    3832    3835
                     3856    3872    3878    3882    3893    3899    3903    3925    3939    3945    3951    3973    3987
                     3993    3998    4018    4033    4039    4043    4053    4059    4063    4084    4099    4105    4109
                     4119    4125    4129    4151    4165    4171    4177    4199    4213    4219    4224    4243    4259
                     4265    4269    4279    4285    4289    4309    4325    4331    4335    4345    4351    4355    4376
                     4389    4395    4400    4423    4443    4449    4455    4482    4499    4504    4524    4530    4533
                     4548    4554    4557    4585    4602    4607    4627    4633    4636    4651    4657    4660    4691
                     4708    4713    4734    4740    4745    4776    4793    4798    4819    4825    4830    4851    4878
                     4883    4893    4898    4916    4921    4939    4944    4961    4967    4983    5001    5022    5027
                     5049    5054    5093    5098    5116    5121    5134    5139    5148    5153    5184    5189    5207
                     5214    5222    5238    5267    5282    5287    5304    5309    5325    5330    5341    5346    5383
                     5388    5441    5446    5468    5473    5496    5503    5540    5545    5568    5573    5613    5618
                     5660    5665    5683    5688    5696    5712    5741    5756    5761    5778    5783    5801    5806
                     5817    5822    5857    5862    5915    5920    5948    5953    5976    5983    6017    6022    6050
                     6055    6079    6084    6113    6118    6153    6158    6202    6207    6227    6232    6248    6264
                     6287    6300    6305    6319    6324    6338    6343    6366    6371    6381    6386    6395    6400
                     6424    6429    6439    6444    6461    6466    6475    6480    6490    6495    6504    6509    6518
                     6523    6544    6549    6560    6565    6575    6580    6598    6603    6622    6627    6637    6642
                     6659    6664    6673    6678    6700    6705    6714    6719    6731    6736    6745    6750    6773
                     6778    6789    6792    6818    6838    6843    6856    6861    6884    6889    6898    6903    6933
                     6938    6948    6953    6971    6976    6984    6989    7006    7011    7018    7023    7037    7042
                     7050    7055    7073    7078    7085    7090    7113    7118    7128    7133    7149    7154    7177
                     7182    7202    7207    7222    7227    7236    7241    7251    7256    7270    7275    7285    7291
                     7294    7320    7332    7337    7364    7369    7377    7382    7407    7412    7438    7443    7452
                     7455    7486    7501    7506    7523    7528    7544    7549    7593    7598    7653    7658    7682
                     7687    7712    7717    7758    7763    7790    7795    7820    7825    7867    7872    7896    7901
                     7939    7944    7984    7989    8014    8019    8056    8061    8105    8110    8131    8136    8145
                     8162    8194    8209    8214    8231    8236    8255    8260    8306    8311    8364    8369    8399
                     8404    8429    8434    8471    8476    8505    8510    8536    8541    8573    8578    8603    8608
                     8651    8656    8682    8687    8723    8728    8770    8775    8802    8807    8843    8848    8894
                     8899    8922    8927    8942    8960    8980    8994    9999    9034    9039    9070    9075    9099
                     9104    9125    9130    9151    9156    9177    9182    9196    9201    9211    9214    9237    9249
                     9254    9267    9272    9290    9295    9315    9320    9384    9389    9403    9408    9454    9459
                     9470    9475    9490    9495    9505    9510    9554    9560    9567    9591    9626    9631    9643
                     9648    9662    9667    9685    9690    9704    9709    9739    9745    9761    9785    9799    9804
                     9821    9826    9841    9846    9858    9863    9878    9883    9939    9944    9975    9980   10008
                    10013   10036   10041   10071   10076   10108   10113   10127   10132   10178   10183   10201   10206
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                    10230  10235  10245  10250  10268  10273  10294  10299  10308  10313  10328  10333  10353
                    10359  10375  10394  10412  10417  10431  10436  10451  10456  10473  10478  10494  10499
                    10514  10519  10536  10541  10551  10556  10574  10579  10596  10601  10613  10619  10628
                    10643  10657  10662  10678  10683  10696  10701  10713  10718  10748  10753  10761  10766
                    10777  10782  10792  10797  10805  10810  10819  10824  10836  10841  10850  10855  10869
                    10874  10882  10887  10905  10910  10928  10933  10950  10955  10968  10973  10988  10993
                    11004  11009  11018  11023  11039  11044  11057  11062  11071  11076  11085  11090  11103
                    11108  11118  11125  11138  11143  11154  11159  11167  11172  11183  11188  11212  11217
                    11230  11235  11245  11250  11260  11265  11280  11285  11297  11302  11322  11327  11335
                    11340  11350  11353  11369  11381  11386  11400  11405  11414  11419  11438  11443  11453
                    11458  11471  11476  11485  11490  11523  11528  11540  11545  11550  11555  11567  11572
                    11594  11599  11609  11614  11626  11631  11654  11659  11671  11676  11702  11707  11725
                    11730  11742  11747  11770  11775  11785  11788  11808  11821  11826  11839  11844  11885
                    11890  11900  11905  11936  11941  11974  11979  11990  11995  12006  12011  12038  12043
                    12071  12076  12110  12115  12141  12146  12169  12174  12195  12200  12223  12228  12237
                    12242  12261  12266  12286  12291  12300  12305  12324  12329  12341  12346  12370  12375
                    12397  12402  12432  12437  12447  12452  12468  12473  12482  12487  12501  12506  12534
                    12539  12548  12553  12573  12578  12595  12600  12625  12630  12639  12642  12661  12668
                    12682  12687  12716  12726  12739  12745  12755  12760  12769  12775  12791  12797  12804
                    12817  12822  12832  12837  12846  12852  12860  12870  12875  12885  12890  12905  12910
                    12919  12924  12935  12947  12953  12959  12969  12974  12979  12984  12996  13006  13011
                    13021  13026  13039  13044  13049  13054  13062  13072  13078  13086  13091  13101  13106
                    13123  13129  13143  13152  13157  13165  13175  13181  13187  13194  13198  13201  13227
                    13236  13241  13256  13261  13269  13274  13289  13294  13310  13315  13325  13330  13335
                    13341  13348  13361  13366  13371  13381  13386  13394  13399  13407  13412  13427  13432
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                    13580  13593  13598  13603  13612  13617  13626  13632  13636  13663  13672  13677  13704
                    13709  13723  13728  13743  13748  13767  13772  13788  13793  13810  13815  13844  13849
                    13857  13863  13909
T$ STS- 000001        1363#  3419#  3438#  3487#  3538#  3570#  3619#  3670#  3702#  3738#  3789#  3853#  3920#
                      3968#  4015#  4081#  4146#  4194#  4240#  4306#  4371#  4419#  4479#  4582#  4687#  4772#
                      4846#  4996#  5262#  5736#  6284#  6816#  7317#  7481#  8189#  8977#  9233#  9586#  9780#
                     10390# 10641# 11366# 11806# 12658# 13217# 13655#
T$$AU = 010022         3359#  3363   3370
T$$AUT= 010017         3294#  3298
T$$CLE= 010020         3309#  3319   3326
T$$DAT= 010106        14017# 14023
T$$DU = 010021         3336#  3340   3347
T$$HAR= 010102        13929# 13961
T$$HW = 010000         1532#  1542
T$$INI= 010016         3213#  3275   3282
T$$MSG= 010012         2139#  2144   2148#  2153   2157#  2162   2166#  2171   2175#  2180   2184#  2192   2196#
                       2204   2208#  2216   2220#  2228
T$$PC = 000001        14015# 14025
T$$PRO= 010015         3197#
T$$PTA= 010105        14015# 14018  14019#
T$$RPT= 010014         3175#  3179   3186
T$$SEG= 010000         2392#  2430#  2436#  2447#  2455#  2510#  2518#  2547#  2551#  2619#  2623#  2673#  2735#
                       2745#  2755#  2765#  2777#  2787#  2797#  2807#  2817#  2827#  2837#  2847#  2857#  2867#
                       2877#  2887#  2906#  2916#  2926#  2937#  2957#  2967#  2977#  2988#  3006#  3016#  3025#
                       3036#  3054#  3064#  3073#  3084#  3106#  3126#  3137#  3157#  3441#  3454#  3458#  3471#
                       3490#  3504#  3508#  3522#  3543#  3552#  3573#  3586#  3590#  3603#  3622#  3636#  3640#
                       3654#  3675#  3684#  3707#  3716#  3743#  3758#  3792#  3812#  3816#  3831#  3856#  3877#
                       3882#  3898#  3925#  3944#  3973#  3992#  4018#  4038#  4043#  4058#  4084#  4104#  4109#
                       4124#  4151#  4170#  4199#  4218#  4243#  4264#  4269#  4284#  4309#  4330#  4335#  4350#
                       4376#  4394#  4423#  4448#  4482#  4529#  4533#  4553#  4585#  4632#  4636#  4656#  4691#
```

```
                    4739#  4776#  4824#  4851#  4966#  5001#  5221#  5267#  5695#  5741#  6247#  6287#  6788#
                    6818#  7290#  7320#  7451#  7486#  8144#  8194#  8941#  8980#  9210#  9237#  9559#  9591#
                    9744#  9785# 10358# 10394# 10618# 10643# 11349# 11369# 11784# 11808# 12638# 12661# 13197#
                   13663# 13862#
T$$SOF= 010103     13989# 13997
T$$SRV= 010013      2720#  2724
T$$SUB= 010100     13227# 13473  13482# 13631
T$$SW = 010001      1554#  1560
T$$TES= 010101      3419#  3425  3438#  3474  3487#  3525  3538#  3558  3570#  3606  3619#  3657  3670#
                    3690   3702#  3721   3738#  3771   3789#  3834   3853#  3902   3920#  3950   3968#  3997
                    4015#  4062   4081#  4128   4146#  4176   4194#  4223   4240#  4288   4306#  4354   4371#
                    4399   4419#  4454   4479#  4556   4582#  4659   4687#  4744   4772#  4829   4846#  4982
                    4996#  5237   5262#  5711   5736#  6263   6284#  6791   6816#  7293   7317#  7454   7481#
                    8161   8189#  8959   8977#  9213   9233#  9566   9586#  9760   9780# 10374  10390# 10627
                   10641# 11352  11366# 11787  11806# 12641  12658# 13200  13217# 13635  13655# 13908
T1      010344 G    1476   3418#
T10     011160 G    1485   3788#
T11     011250 G    1486   3852#
T12     011342 G    1487   3919#
T13     011416 G    1488   3967#
T14     011466 G    1489   4014#
T15     011556 G    1490   4080#
T16     011650 G    1491   4145#
T17     011724 G    1492   4193#
T18     011774 G    1493   4239#
T19     012072 G    1494   4305#
T2      010352 G    1477   3437#
T20     012172 G    1495   4370#
T21     012246 G    1496   4418#
T22     012320 G    1497   4478#
T23     012442 G    1498   4581#
T24     012566 G    1499   4686#
T25     012666 G    1500   4771#
T26     012770 G    1501   4845#
T27     013236 G    1502   4995#
T28     013662 G    1503   5261#
T29     014570 G    1504   5735#
T3      010436 G    1478   3486#
T30     015562 G    1505   6283#
T31     016752 G    1506   6815#
T32     020046 G    1507   7316#
T33     020316 G    1508   7480#
T34     021604 G    1509   8188#
T35     023156 G    1510   8976#
T36     023534 G    1511   9232#
T37     024356 G    1512   9585#
T38     024706 G    1513   9779#
T39     026132 G    1514  10389#
T4      010524 G    1479   3537#
T40     026646 G    1515  10640#
T41     030566 G    1516  11365#
T42     031576 G    1517  11805#
T43     033332 G    1518  12657#
T44     034546 G    1519  13216#
T44.1   034552     13226#
T44.2   035362     13481#
```

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T45      035716 G   1520  13654#
T5       010574 G   1480   3569#
T6       010660 G   1481   3618#
T7       010746 G   1482   3669#
T8       011016 G   1483   3701#
T9       011062 G   1484   3737#
UAM    = 000200 G   1635#
UNEXIN   002432 G   1889#  12741  12771  12793  12848  12949  13074  13125  13177
UNITNB   002314 G   1832#   3243*  3249*  3251
VDALRG   002537 G   1908#   2646   2670   3113   3123   3755   5095   5150   5186   5385   5443   5470   5542
                    5570   5662   5685   5859   5917   5950   6019   6052   6081   6115   6204   6229   6397
                    6441   6477   6520   6546   6600   6639   6661   6702   6733   6775   6900   6950   6973
                    7020   7052   7087   7130   7238   7287   7379   7409   7440   7595   7655   7684   7760
                    7792   7869   7898   7986   8016   8107   8133   8308   8366   8401   8473   8507   8538
                    8575   8653   8684   8772   8804   8896   8924   9072   9101   9127   9153   9179   9198
                    9507   9880   9941   9977  10010  10038  10180  10247  10763  10794  10821  10852  10884
                   10907  10930  10952  10990  11020  11041  11059  11087  11120  11156  11185  11214  11247
                   11282  11299  11324  11455  11487  11525  11542  11552  11596  11656  11704  11772  11887
                   11938  11976  12008  12040  12073  12112  12143  12171  12197  12225  12263  12288  12326
                   12372  12399  12434  12470  12536  12575  12627  13271  13409  13499  13545  13614
VDAL0  -  000001 G   1721#  3739   3768   9501  10174  13265
VDAL1  =  000002 G   1720#  3739   3768  13265
VDAL10=   002000 G   1711#  5464   5563   5944   6108   6655   6695   6769   6967   7678   7785   8395   8568
                    9095   9970  10031
VDAL11=   004000 G   1710#  5564   5679   6109   6223   6696   6768  10032
VDAL12=   010000 G   1709#  7786   7891   8569   8677   9121
VDAL13=   020000 G   1708#  7892   8009   8678   8797   9147
VDAL14=   040000 G   1707#  8010   8127   8798   8918   9173
VDAL15=   100000 G   1706#  5379   5853   5911   6108   7589   8302   8360   8568
VDAL2  -  000004 G   1719#  2637   3107   3117   3739   3768  11274  11536  13265
VDAL3  =  000010 G   1718#  10757  10815  10946  11014  11053  11114  11150  11208  11276  11293  11318
VDAL4     000020 G   1717#  11932  11970  12033  12067  12137  12165  12191  12257  12282  12366  12393  12428
                   12464  12530  12569  12621
VDAL5  =  000040 G   1716#   9935   9971  11449  11519  11698  11766  11969  12034  12256  12320  12529  12568
VDAL6  =  000100 G   1715#  10241  10757  10815  10946  11014  11053  11081  11208  11276  11293  11318
VDAL7  -  000200 G   1714#   3739   5060   5143   5394   5435   5851   5909   6514   6540   6726   6727   6894
                    7232   7373   7401   7604   7647   8300   8358   9016   9874   9933  11291  11868  12001
                   12002  13265  13493  13539
VDAL8  -  000400 G   1713#   6046   8501
VDAL9  =  001000 G   1712#   5089   5144   5437   5656   5911   6198   6633   6944   7124   7403   7649   8101
                    8360   8890   9066   9935  11317  11519  11698  11766  11969  13539  13781
XBCLR     007606 G   3045#
XBCLRH    007620 G   3045   3053#  4863   9611  10167
XBCLRL    007652 G   3046   3072#  9722  10215
XCAS      007376 G   2947#   5671   6213   6452   6589   6650   6688   6761   6962   7162   7428   8117   8906
                    9085   9111   9137   9163   9351   9427   9531   9960  11877  11917  12051  12121  12381
XCASH     007410 G   2947   2956#  5456   5555   5934   6098   7668   7775   7881   7999   8383   8556   8665
                    8785  10023  10941  12153
XCASL     007442 G   2948   2976#  5513   5629   5997   6169   7729   7837   7955   8072   8449   8619   8739
                    8859  10156  10920  12179
XPI       007502 G   2997#   5518   5634   5693   6002   6174   6237   7420   7734   7842   7960   8077   8141
                    8454   8624   8744   8864   8932   9188   9986
XPIH      007514 G   2997   3005#  9336   9421   9525  10090
XPIL      007546 G   2998   3024#  9357   9433   9537  10160
XRAS      007272 G   2896#   5078   5176   5426   5529   5648   6066   6188   6414   6533   6923   6998   7064
                    7105   7168   7213   7262   7395   7636   7745   7853   7971   8091   8521   8635   8755
```

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                        8878    9055    9922    9997   11514   11583   11645   11692   11760   11951   12018   12092   12609
                       12781   12897   13113   13534
XRASH   007304 G        2896    2905#   5896    8345   11048   11201   11310   12208   12354   12416   12514
XRASL   007336 G        2897    2925#   6032    8486   10897   11029   11200   11309   12270   12408   12492   12583
X$ALWA= 000000          1363#
X$FALS= 000040          1363#
X$OFFS= 000400          1363#
X$TRUE= 000020          1363#
$PATCH  036552 G       14001#
.     - 036650          1367#   1865#   2053#   2127#   3180    3276    3320    3341    3364   13975#  14002#  14017   14025


. ABS.  036650     000

 ERRORS DETECTED:  0

 CVCDCA.BIC,CVCDCA/CRF:SYM/SOL/NL:TOC=SVC/ML,CVCDCA.P11
 RUN-TIME: 69 83 5 SECONDS
 RUN-TIME RATIO: 752/158=4.7
 CORE USED:  20K  (40 PAGES)
```