MDE/T-11 MDE/T-11 ST ANLYZR AH-T005B-MC SEP 1982
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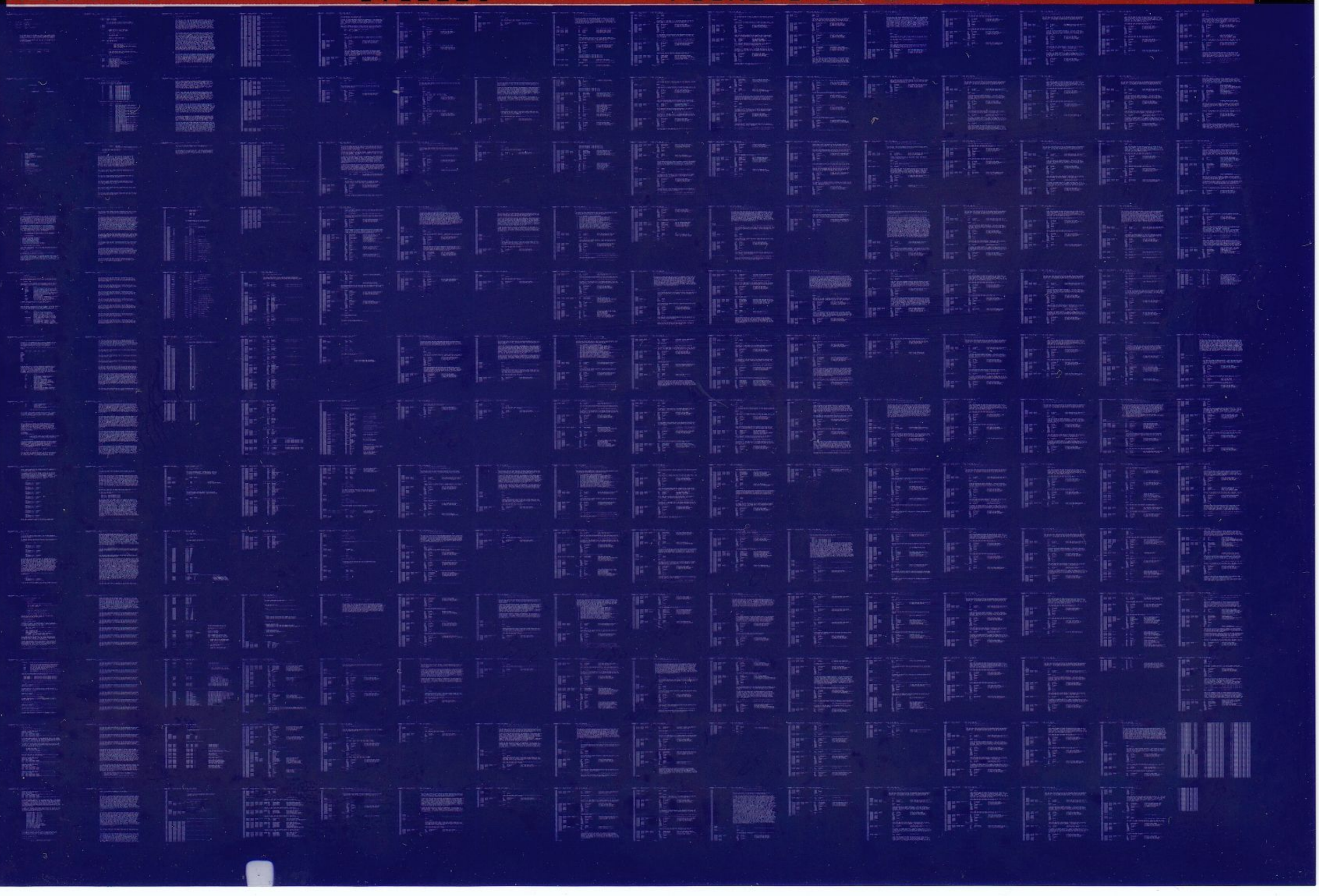

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CVCDBBO

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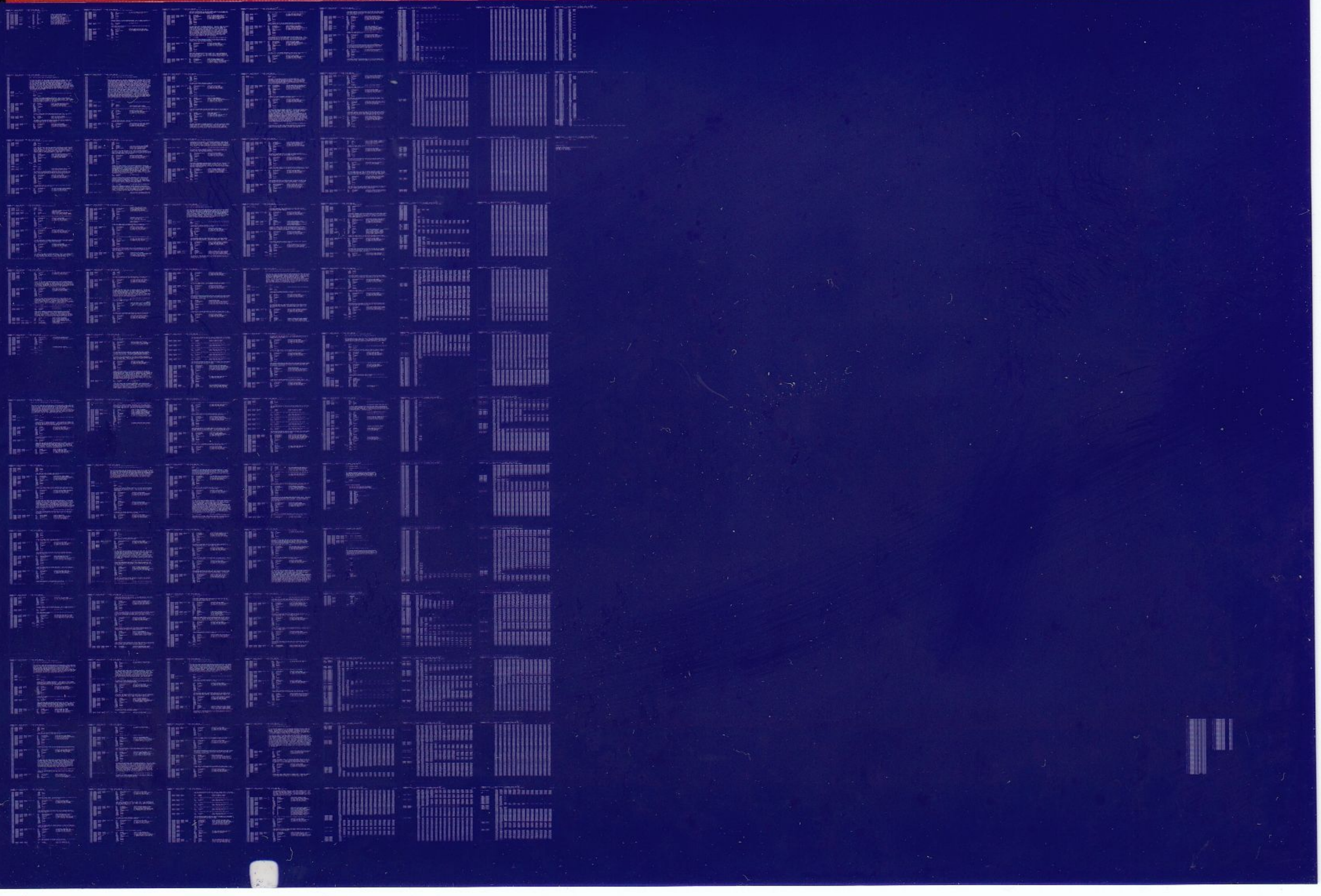

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IDENTIFICATION

PRODUCT CODE: AC-T003B-MC

PRODUCT NAME: CVCDBB0 MDE/T-11 ST ANLYZR DIAG

PRODUCT DATE: OCTOBER 1982

MAINTAINER: DIAGNOSTIC ENGINEERING

REVISION HISTORY

REVISION	DATE	REASONS
A	SEPTEMBER 1981	FIRST RELEASE
B	OCTOBER 1982	DOCUMENTATION CHANGE

TABLE OF CONTENTS

1.0 GENERAL INFORMATION

1.1 PROGRAM ABSTRACT

THE MDE/T-11 STATE ANALYZER DIAGNOSTIC WILL TEST ALL THE LOGIC ON THE STATE ANALYZER MODULE EXCEPT THAT LOGIC PERTAINING TO THE SYSTEM BUS. THE DIAGNOSTIC WILL CHECK ALL THE BITS IN CONTROL REGISTER 0 AND CONTROL REGISTER 2. THE DIAGNOSTIC WILL CHECK THE TRACE RAM ADDRESS REGISTER, THE TRACE RAM DATA IN BUFFERS, THE TRACE RAM'S, THE OR ADDRESS REGISTER, THE OR ARRAY RAM'S, THE AND ARRAY RAM'S, THE EVENT COUNTER REGISTERS, THE EVENT COUNTERS AND EVENT COUNTER LOGIC, THE FUNCTION SELECT FLIP-FLOP LOGIC, THE TRACING FLIP-FLOP LOGIC, THE SBL FLIP-FLOP LOGIC AND THE EXTERNAL PROBE LOGIC.

THIS DIAGNOSTIC HAS BEEN WRITTEN FOR USE WITH THE DIAGNOSTIC RUNTIME SERVICES SOFTWARE (SUPERVISOR). THESE SERVICES PROVIDE THE INTERFACE TO THE OPERATOR AND TO THE SOFTWARE ENVIRONMENT. THIS PROGRAM CAN BE USED WITH XXDP+, ACT, APT, SLIDE AND PAPER TAPE. FOR A COMPLETE DESCRIPTION OF THE RUNTIME SERVICES, REFER TO THE XXDP+ USER'S MANUAL. THERE IS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES IN SECTION 2 OF THIS DOCUMENT.

NOTE: THIS PROGRAM WAS NOT BEEN TESTED IN THE APT ENVIRONMENT, HOWEVER, THE APT INTERFACE HAS BEEN PROVIDED IN THE DIAGNOSTIC.

1.2 SYSTEM REQUIREMENTS

1. LSI-11 OR EQUIVALENT TYPE CPU WITH Q-BUS
2. MINIMUM OF 16K WORDS OF MEMORY
3. CONSOLE TERMINAL AND CONTROLLER
4. MDE/T-11 BACKPLANE AND CABLES
5. STATE ANALYZER MODULE(S) (M8741)
6. MXV11 MODULE AND MDE/T-11 ROMS
7. STORAGE DEVICE WITH CONTROLLER (OPTIONAL)
8. XXDP+ MEDIA FOR STORAGE DEVICE (OPTIONAL)

1.3 RELATED DOCUMENTS AND STANDARDS

CHQUS? XXDP+ USER'S MANUAL (THE "?" IN CHQUS INDICATES THE REVISION LEVEL OF THE DOCUMENT. AT THE TIME THIS PROGRAM WAS WRITTEN, THE REVISION LEVEL WAS "E".

1.4 DIAGNOSTIC HIERARCY PREREQUISITES

ALL HARDWARE THAT IS SPECIFIED IN SECTION 1.2 OF THIS DOCUMENT MUST BE OPERATIONAL AND FREE OF ALL FAULTS.

IF THE EXTERNAL PROBE AND THE STATE ANALYZER EXTERNAL PROBE LOGIC ARE TO BE TESTED BY THE DIAGNOSTIC, THE OPERATOR MUST PLUG THE EXTERNAL PROBE INTO THE STATE ANALYZER AND CONNECT THE EXTERNAL PROBE LEADS 7:0 TO EVENT COUNTER REGISTER 0 SIGNAL LINES SDBL 7:0 L RESPECTIVELY. THE EXTERNAL PROBE LEAD FOR THE CLK MUST BE CONNECTED TO EVENT COUNTER 1'S SIGNAL LINE SDBL8 L.

1.5 ASSUMPTIONS

2.0 OPERATING INSTRUCTIONS

THIS SECTION CONTAINS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES.
FOR DETAILED INFORMATION, REFER TO THE XXDP+ USER'S MANUAL (CHQUS).

2.1 COMMANDS

THERE ARE ELEVEN LEGAL COMMANDS FOR THE DIAGNOSTIC RUNTIME SERVICES
(SUPERVISOR). THIS SECTION LISTS THE COMMANDS AND GIVES A VERY
BRIEF DESCRIPTION OF THEM. THE XXDP+ USER'S MANUAL HAS MORE DETAILS.

COMMAND	EFFECT
START	START THE DIAGNOSTIC FROM AN INITIAL STATE
RESTART	START THE DIAGNOSTIC WITHOUT INITIALIZING
CONTINUE	CONTINUE AT TEST THAT WAS INTERRUPTED (AFTER ^C)
PROCEED	CONTINUE FROM AN ERROR HALT
EXIT	RETURN TO XXDP+ MONITOR (XXDP+ OPERATION ONLY!)
ADD	ACTIVATE A UNIT FOR TESTING (ALL UNITS ARE CONSIDERED TO BE ACTIVE AT START TIME
DROP	DEACTIVATE A UNIT
PRINT	PRINT STATISTICAL INFORMATION (IF IMPLEMENTED BY THE DIAGNOSTIC - SECTION 4.0)
DISPLAY	TYPE A LIST OF ALL DEVICE INFORMATION
FLAGS	TYPE THE STATE OF ALL FLAGS (SEE SECTION 2.3)
ZFLAGS	CLEAR ALL FLAGS (SEE SECTION 2.3)

A COMMAND CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. SO
YOU MAY, FOR EXAMPLE, TYPE "STA" INSTEAD OF "START".

2.2 SWITCHES

THERE ARE SEVERAL SWITCHES WHICH ARE USED TO MODIFY SUPERVISOR OPERATION.
THESE SWITCHES ARE APPENDED TO THE LEGAL COMMANDS. ALL OF THE LEGAL
SWITCHES ARE TABULATED BELOW WITH A BRIEF DESCRIPTION OF EACH.
IN THE DESCRIPTIONS BELOW, A DECIMAL NUMBER IS DESIGNATED BY "DDDDD".

SWITCH	EFFECT
/TESTS:LIST	EXECUTE ONLY THOSE TESTS SPECIFIED IN THE LIST. LIST IS A STRING OF TEST NUMBERS, FOR EXAMPLE - /TESTS:1:5:7-10. THIS LIST WILL CAUSE TESTS 1,5,7,8,9,10 TO BE RUN. ALL OTHER TESTS WILL NOT BE RUN.
/PASS:DDDDD	EXECUTE DDDDD PASSES (DDDDD = 1 TO 64000)
/FLAGS:FLGS	SET SPECIFIED FLAGS. FLAGS ARE DESCRIBED IN SECTION 2.3.
/EOP:DDDDD	REPORT END OF PASS MESSAGE AFTER EVERY DDDDD PASSES ONLY. (DDDDD = 1 TO 64000)
/UNITS:LIST	TEST/ADD/DROP ONLY THOSE UNITS SPECIFIED IN THE LIST. LIST EXAMPLE - /UNITS:0:5:10-12 USE UNITS 0,5,10,11,12 (UNIT NUMBERS = 0-63)

EXAMPLE OF SWITCH USAGE:

START/TESTS:1-5/PASS:1000/EOP:100

THE EFFECT OF THIS COMMAND WILL BE: 1) TESTS 1 THROUGH 5 WILL BE EXECUTED, 2) ALL UNITS WILL BE TESTED 1000 TIMES AND 3) THE END OF PASS MESSAGES WILL BE PRINTED AFTER EACH 100 PASSES ONLY. A SWITCH CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. YOU MAY, FOR EXAMPLE, TYPE "/TES:1-5" INSTEAD OF "/TESTS:1-5".

BELOW IS A TABLE THAT SPECIFIES WHICH SWITCHES CAN BE USED BY EACH COMMAND.

	TESTS	PASS	FLAGS	EOP	UNITS
START	X	X	X	X	X
RESTART	X	X	X	X	X
CONTINUE		X	X	X	
PROCEED			X		
DROP					X
ADD					X
PRINT					
DISPLAY					X
FLAGS					
ZFLAGS					
EXIT					

2.3 FLAGS

FLAGS ARE USED TO SET UP CERTAIN OPERATIONAL PARAMETERS SUCH AS LOOPING ON ERROR. ALL FLAGS ARE CLEARED AT STARTUP AND REMAIN CLEARED UNTIL EXPLICITLY SET USING THE FLAGS SWITCH. FLAGS ARE ALSO CLEARED AFTER A START COMMAND UNLESS SET USING THE FLAG SWITCH. THE ZFLAGS COMMAND MAY ALSO BE USED TO CLEAR ALL FLAGS. WITH THE EXCEPTION OF THE START AND ZFLAGS COMMANDS, NO COMMANDS AFFECT THE STATE OF THE FLAGS; THEY REMAIN SET OR CLEARED AS SPECIFIED BY THE LAST FLAG SWITCH.

FLAG	EFFECT
HOE	HALT ON ERROR - CONTROL IS RETURNED TO RUNTIME SERVICES COMMAND MODE
LOE	LOOP ON ERROR
IER*	INHIBIT ALL ERROR REPORTS
IBE*	INHIBIT ALL ERROR REPORTS EXCEPT FIRST LEVEL (FIRST LEVEL CONTAINS ERROR TYPE, NUMBER, PC, TEST AND UNIT)
IXE*	INHIBIT EXTENDED ERROR REPORTS (THOSE CALLED BY PRINTX MACRO'S)
PRI	DIRECT MESSAGES TO LINE PRINTER
PNT	PRINT TEST NUMBER AS TEST EXECUTES
BOE	"BELL" ON ERROR
UAM	UNATTENDED MODE (NO MANUAL INTERVENTION)
ISR	INHIBIT STATISTICAL REPORTS (DOES NOT APPLY TO DIAGNOSTICS WHICH DO NOT SUPPORT STATISTICAL REPORTING)

IDR	INHIBIT PROGRAM DROPPING OF UNITS
ADR	EXECUTE AUTODROP CODE
LOT	LOOP ON TEST
EVL	EXECUTE EVALUATION (ON DIAGNOSTICS WHICH HAVE EVALUATION SUPPORT)

*ERROR MESSAGES ARE DESCRIBED IN SECTION 3.1

SEE THE XXDP+ USER'S MANUAL FOR MORE DETAILS ON FLAGS. YOU MAY SPECIFY MORE THAN ONE FLAG WITH THE FLAG SWITCH. FOR EXAMPLE, TO CAUSE THE PROGRAM TO LOOP ON ERROR, INHIBIT ERROR REPORTS AND TYPE A "BELL" ON ERROR, YOU MAY USE THE FOLLOWING STRING:

```
/FLAGS:LOE:IER:BOE
```

2.4 HARDWARE QUESTIONS

WHEN A DIAGNOSTIC IS STARTED, THE RUNTIME SERVICES WILL PROMPT THE USER FOR HARDWARE INFORMATION BY TYPING "CHANGE HW (L) ?" YOU MUST ANSWER "Y" AFTER A START COMMAND UNLESS THE HARDWARE INFORMATION HAS BEEN "PRELOADED" USING THE SETUP UTILITY (SEE CHAPTER 6 OF THE XXDP+ USER'S MANUAL). WHEN YOU ANSWER THIS QUESTION WITH A "Y", THE RUNTIME SERVICES WILL ASK FOR THE NUMBER OF UNITS (IN DECIMAL). YOU WILL THEN BE ASKED THE FOLLOWING QUESTIONS FOR EACH UNIT.

```
CSR ADDRESS:
DEVICE NUMBER:
EXTERNAL PROBE CONNECTED:
```

NOTE: IF THE EXTERNAL PROBE AND THE STATE ANALYZER'S EXTERNAL PROBE LOGIC IS TO BE TESTED, REFER TO SECTION 1.4 OF THIS DOCUMENT FOR THE EXTERNAL PROBE CONNECTIONS.

2.5 SOFTWARE QUESTIONS

AFTER YOU HAVE ANSWERED THE HARDWARE QUESTIONS OR AFTER A RESTART OR CONTINUE COMMAND, THE RUNTIME SERVICES WILL ASK FOR SOFTWARE PARAMETERS. THESE PARAMETERS WILL GOVEPN SOME DIAGNOSTIC SPECIFIC OPERATION MODES. YOU WILL BE PROMPTED BY "CHANGE SW (L) ?" IF YOU WISH TO CHANGE ANY PARAMETERS, ANSWER BY TYPING "Y". THE SOFTWARE QUESTIONS AND THE DEFAULT VALUES ARE DESCRIBED IN THE NEXT PARAGRAPH(S).

THERE ARE NO SOFTWARE QUESTIONS IN THIS PROGRAM.

2.6 EXTENDED P-TABLE DIALOGUE

WHEN YOU ANSWER THE HARDWARE QUESTIONS, YOU ARE BUILDING ENTRIES IN A TABLE THAT DESCRIBES THE DEVICES UNDER TEST. THE SIMPLEST WAY TO BUILD THIS TABLE IS TO ANSWER ALL QUESTIONS FOR EACH UNIT TO BE TESTED. IF YOU HAVE A MULTIPLEXED DEVICE SUCH AS

A MASS STORAGE CONTROLLER WITH SEVERAL DRIVES OR A COMMUNICATION
DEVICE WITH SEVERAL LINES, THIS BECOMES TEDIOUS SINCE MOST OF
THE ANSWERS ARE REPETITIOUS.

TO ILLUSTRATE A MORE EFFICIENT METHOD, SUPPOSE YOU ARE TESTING
A FICTIONAL DEVICE, THE XY11. SUPPOSE THIS DEVICE CONSISTS OF
A CONTROL MODULE WITH EIGHT UNITS (SUB-DEVICES) ATTACHED TO IT.
THESE UNITS ARE DESCRIBED BY THE OCTAL NUMBERS 0 THROUGH 7. THERE
IS ONE HARDWARE PARAMETER THAT CAN VARY AMONG UNITS CALLED THE
Q-FACTOR. THIS Q-FACTOR MAY BE 0 OR 1. BELOW IS A SIMPLE WAY
TO BUILD A TABLE FOR ONE XY11 WITH EIGHT UNITS.

```
# UNITS (D) ?  8<CR>

UNIT 1
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  0<CR>
Q-FACTOR (O) 0 ?  1<CR>

UNIT 2
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  1<CR>
Q-FACTOR (O) 1 ?  0<CR>

UNIT 3
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  2<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 4
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  3<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 5
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  4<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 6
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  5<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 7
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  6<CR>
Q-FACTOR (O) 0 ?  1<CR>

UNIT 8
CSR ADDRESS (O)  160000<CR>
SUB-DEVICE # (O) ?  7<CR>
Q-FACTOR (O) 1 ?  <CR>
```

NOTICE THAT THE DEFAULT VALUE FOR THE Q-FACTOR CHANGES WHEN A
NON-DEFAULT RESPONSE IS GIVEN. BE CAREFUL WHEN SPECIFYING

MULTIPLE UNITS!

AS YOU CAN SEE FROM THE ABOVE EXAMPLE, THE HARDWARE PARAMETERS DO NOT VARY SIGNIFICANTLY FROM UNIT TO UNIT. THE PROCEDURE SHOWN IS NOT VERY EFFICIENT.

THE RUNTIME SERVICES CAN TAKE MULTIPLE UNIT SPECIFICATIONS HOWEVER. LET'S BUILD THE SAME TABLE USING THE MULTIPLE SPECIFICATION FEATURE.

```
        # UNITS (D) ?  8<CR>

        UNIT 1
        CSR ADDRESS (O) ?  160000<CR>
        SUB-DEVICE # (O) ?  0,1<CR>
        Q-FACTOR (O) 0 ?  1,0<CR>

        UNIT 3
        CSR ADDRESS (O) ?  160000<CR>
        SUB-DEVICE # (O) ?  2-5<CR>
        Q-FACTOR (O) 0 ?  0<CR>

        UNIT 7
        CSR ADDRESS (O) ?  160000<CR>
        SUB-DEVICE # (O) ?  6,7<CR>
        Q-FACTOR (O) 0 ?  1<CR>
```

AS YOU CAN SEE IN THE ABOVE DIALOGUE, THE RUNTIME SERVICES WILL BUILD AS MANY ENTRIES AS IT CAN WITH THE INFORMATION GIVEN IN ANY ONE PASS THROUGH THE QUESTIONS. IN THE FIRST PASS, TWO ENTRIES ARE BUILT SINCE TWO SUB-DEVICES AND Q-FACTORS WERE SPECIFIED. THE SERVICES ASSUME THAT THE CSR ADDRESS IS 160000 FOR BOTH SINCE IT WAS SPECIFIED ONLY ONCE. IN THE SECOND PASS, FOUR ENTRIES WERE BUILT. THIS IS BECAUSE FOUR SUB-DEVICES WERE SPECIFIED. THE "-" CONSTRUCT TELLS THE RUNTIME SERVICES TO INCREMENT THE DATA FROM THE FIRST NUMBER TO THE SECOND. IN THIS CASE, SUB-DEVICES 2, 3, 4 AND 5 WERE SPECIFIED. (IF THE SUB-DEVICE WERE SPECIFIED BY ADDRESSES, THE INCREMENT WOULD BE BY 2 SINCE ADDRESSES MUST BE ON AN EVEN BOUNDARY.) THE CSR ADDRESSES AND Q-FACTORS FOR THE FOUR ENTRIES ARE ASSUMED TO BE 160000 AND 0 RESPECTIVELY SINCE THEY WERE ONLY SPECIFIED ONCE. THE LAST TWO UNITS ARE SPECIFIED IN THE THIRD PASS.

THE WHOLE PROCESS COULD HAVE BEEN ACCOMPLISHED IN ONE PASS AS SHOWN BELOW.

```
        # UNITS (D) ?  8<CR>

        UNIT ?
        CSR ADDRESS (O) ?  160000<CR>
        SUB-DEVICE # (O) ?  0-7<CR>
        Q-FACTOR (O) 0 ?  0,1,0,,,,1,1<CR>
```

AS YOU CAN SEE FROM THIS EXAMPLE, NULL REPLIES (COMMAS ENCLOSING A NULL FIELD) TELL THE RUNTIME SERVICES TO REPEAT THE LAST REPLY.

2.7 QUICK START-UP PROCEDURE (XXDP+)

TO START-UP THIS PROGRAM:

1. BOOT XXDP+
2. ANSWER ANY QUESTIONS ASKED AND GIVE THE DATE.
3. TYPE 'R NAME', WHERE NAME IS THE NAME OF THE BIN OR BIC FILE FOR THIS PROGRAM
4. TYPE 'START'
5. ANSWER THE 'CHANGE HW' QUESTION WITH 'Y'
6. ANSWER ALL THE HARDWARE QUESTIONS
7. ANSWER THE 'CHANGE SW' QUESTION WITH 'N'

WHEN YOU FOLLOW THIS PROCEDURE YOU WILL BE USING ONLY THE DEFAULTS FOR FLAGS AND SOFTWARE PARAMETERS. THESE DEFAULTS ARE DESCRIBED IN SECTIONS 2.3 AND 2.5.

3.0 ERROR INFORMATION

3.1 TYPES OF ERROR MESSAGES

THERE ARE THREE LEVELS OF ERROR MESSAGES THAT MAY BE ISSUED BY A DIAGNOSTIC: GENERAL, BASIC AND EXTENDED. GENERAL ERROR MESSAGES ARE ALWAYS PRINTED UNLESS THE 'IER' FLAG IS SET (SECTION 2.3). THE GENERAL ERROR MESSAGE IS OF THE FORM:

```
NAME  TYPE  NUMBER  ON UNIT NUMBER  TST NUMBER PC:XXXXXX
ERROR MESSAGE
```

```
,WHERE; NAME = DIAGNOSTIC NAME
        TYPE = ERROR TYPE (SYS FATAL, DEV FATAL, HARD OR SOFT)
        NUMBER = ERROR NUMBER
        UNIT NUMBER = 0 - N (N IS LAST UNIT IN PTABLE)
        TST NUMBER = TEST AND SUBTEST WHERE ERROR OCCURRED
        PC:XXXXXX = ADDRESS OF ERROR MESSAGE CALL
```

BASIC ERROR MESSAGES ARE MESSAGES THAT CONTAIN SOME ADDITIONAL INFORMATION ABOUT THE ERROR. THESE ARE ALWAYS PRINTED UNLESS THE 'IER' OR 'IBE' FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL MESSAGE.

EXTENDED ERROR MESSAGES CONTAIN SUPPLEMENTARY ERROR INFORMATION SUCH AS REGISTER CONTENTS OR GOOD/BAD DATA. THESE ARE ALWAYS PRINTED UNLESS THE 'IER', 'IBE' OR 'IXE' FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL ERROR MESSAGE AND ANY ASSOCIATED BASIC ERROR MESSAGES.

3.2 SPECIFIC ERROR MESSAGES

THE ERROR PRINTOUTS WILL USE THE FOLLOWING WORDS TO INDICATE ERROR

INFORMATION. A DESCRIPTION OF THE WORDS PRINTED OUT ARE AS FOLLOWS:

REG:	ONE OF THE STATE ANALYZER MODULE'S CONTROL REGISTERS
LOAD:	DATA THAT WAS LOADED INTO THE CONTROL REGISTER OR EXPECTED DATA TO BE IN CONTROL REGISTER ON A READ
READ:	DATA THAT WAS READ FROM THE CONTROL REGISTER
MASK:	BITS IN THE CONTROL REGISTER THAT ARE NOT CHECKED
GOOD:	EXPECTED CONTROL REGISTER DATA
BAD:	DATA "READ" FROM THE CONTROL REGISTER WITH THE "MASK" BITS CLEARED
XXXXXX:	SIX OCTAL DIGITS INDICATING THE DATA FOR THE ABOVE WORDS

THERE ARE FOUR ERROR NUMBERS ASSOCIATED WITH THIS DIAGNOSTIC. THE ERROR NUMBERS AND THEIR MEANINGS ARE DESCRIBED BELOW:

FRROR NUMBER 1 - ERROR DETECTED CHECKING CONTROL REGISTER 0
ERROR NUMBER 2 - ERROR DETECTED CHECKING CONTROL REGISTER 2
ERROR NUMBER 3 - ERROR DETECTED CHECKING CONTROL REGISTER 4
ERROR NUMBER 4 - ERROR DETECTED CHECKING CONTROL REGISTER 6

EXAMPLES OF EACH TYPE OF CONTROL REGISTER ERROR PRINTOUT ARE SHOWN BELOW:

** CONTROL REGISTER 0 ERROR MESSAGES **

```
CVCDB DVC FTL ERR 00001 ON UNIT 00 TST 001 SUB 000 PC: XXXXXX
CONTROL REG 0 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX
```

THE ABOVE ERROR MESSAGE IS REPORTED FOR ALL CONTROL REGISTER 0 ERRORS EXCEPT WHEN CHECKING THE STATE ANALYZERS DEVICE TYPE. IF AN ERROR IS ENCOUNTERED WHEN CHECKING THE DEVICE TYPE, THE FOLLOWING ERROR REPORT WILL BE GIVEN:

```
CVCDB DVC FTL ERR 0001 ON UNIT 00 TST 001 SUB 000 PC: XXXXXX
CONTROL REG 0 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX GOOD: XXXXXX
```

```
TIME OUT ERROR ADDRESSING CONTROL REG 0
```

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 0 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR #4.

** CONTROL REGISTER 2 ERROR MESSAGE **

```
CVCDB DVC FTL ERR 00002 ON UNIT 00 TST 004 SUB 000 PC: XXXXXX
CONTROL REG 2 ERROR
REG2 = LOAD: XXXXXX READ: XXXXXX
```

THE ABOVE ERROR MESSAGE WILL BE PRINTED FOR ALL CONTROL REGISTER 2 ERRORS, EXCEPT A TIME OUT ERROR.

```
TIME OUT ERROR ADDRESSING CONTROL REG 2
```

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 2 AND CAN'T. THE PROGRAM THEN JUMPS TO

TIME OUT VECTOR #4.

** CONTROL REGISTER 4 ERROR MESSAGE **

```
CVCDB DVC FTL ERR 00003 ON UNIT 00 TST 006 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 4 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG4 = LOAD: XXXXXX READ: XXXXXX MASK: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX
```

IN THE ABOVE ERROR, REFER TO THE LINE INDICATING 'REG4 =" FOR CONTROL REGISTER 4 ERROR INFORMATION. THE REMAINING CONTROL REGISTER INFORMATION IS GIVEN TO INDICATE WHAT WAS LOADED INTO THESE REGISTERS PREVIOUS TO THE ERROR. THIS IS DONE TO AID THE USER IN DETERMINING THE FAULT ON ERRORS WHICH NEED PREVIOUS CONTROL REGISTER SETUP.

THE ERROR TYPE MESSAGE IN THE ABOVE ERROR REPORT WILL BE ONE OF THOSE LISTED BELOW. THESE MESSAGES ARE REPORTED TO HELP THE USER IDENTIFY THE AREA OF LOGIC BEING TESTED IN WHICH THE ERROR WAS DETECTED. THESE ERROR TYPE MESSAGES ARE AS FOLLOWS:

```
        OR ARRAY DATA ERROR - ORO 7:0
        AND ARRAY DATA ERROR
        FUSL7 FLIP-FLOP - OR ARRAY DATA ERROR
        AND - OR ARRAY DATA ERROR
```

** CONTROL REGISTER 6 ERROR MESSAGE **

THERE ARE FOUR TYPES OF ERROR MESSAGES THAT ARE REPORTED FOR CONTROL REGISTER 6 ERRORS WHICH ARE SHOWN BELOW.

```
CVCDB DVC FTL ERR 00004 ON UNIT 00 TST 008 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX MASK: XXXXXX GOOD: XXXXXX BAD: XXXXXX

CVCDB DVC FTL ERR 00004 ON UNIT 00 TST 021 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
TRAM ADDRESS REG = XXXXXX
REG0 = LOAD: XXXXXX READ: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX

CVCDB DVC FTL ERR 00004 ON UNIT 00 TST 056 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG4 = LOAD: XXXXXX READ: XXXXXX MASK: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX
```

```
CVCDB DVC FTL ERR 00004 ON UNIT 00 TST 053 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
EVNT CNT LOADED: XXXXXX EVNT CNT BEFORE CNT DOWN: XXXXXX
REG0 = LOAD: XXXXXX MASK: XXXXXX
REG2 = LOAD: XXXXXX MASK: XXXXXX
REG4 = LOAD: XXXXXX READ: XXXXXX MASK: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX
```

IN THE ABOVE ERRORS, REFER TO THE LINE INDICATING "REG6 =" FOR CONTROL REGISTER 6 ERROR INFORMATION. THE REMAINING CONTROL REGISTER INFORMATION IS GIVEN TO INDICATE WHAT WAS LOADED INTO THOSE REGISTERS PREVIOUS TO THE ERROR. THIS IS DONE TO AID THE USER IN DETERMINING THE FAULT ON ERRORS WHICH NEED PREVIOUS CONTROL REGISTER SETUP. THE SECOND AND LAST ERROR MESSAGE SHOWN ABOVE PROVIDE ADDITIONAL INFORMATION OF CONDITIONS SETUP PREVIOUS TO THE ERROR WHICH MAY BE HELPFUL TO THE USER IN DETERMINING THE ERROR.

THE ERROR TYPE MESSAGE IN THE ABOVE ERROR REPORTS WILL BE ONE OF THOSE LISTED BELOW. THESE MESSAGES ARE REPORTED TO HELP THE USER IDENTIFY THE AREA OF LOGIC BEING TESTED IN WHICH THE ERROR WAS DETECTED. THESE ERROR TYPE MESSAGES ARE AS FOLLOWS:

```
        TRAM ADDRESS REG - TRAD 9:0
        TRAM DATA IN BUF - TRDI 15:0
        TRAM DATA IN BUF - TRDI 31:16
        TRAM DATA IN BUF - TRDI 47:32
        TRAM DATA IN BUF - TRDI 59:48
        TRAM DATA IN BUF - TRDI 59:0
        TRAM DATA IN BUF SELECTION
        TRAM DATA ERROR - TRDI 15:0
        TRAM DATA ERROR - TRDI 31:16
        TRAM DATA ERROR - TRDI 47:32
        TRAM DATA ERROR - TRDI 55:48
        OR ADDRESS REG - ORAD 3:0
        EVENT COUNTERS OR FOUT 3:0 ERROR
        PDAL7 FAILED TO CLEAR EVENT COUNTERS
        CDAL0 FAILED TO LOAD EVENT COUNTERS
        FUSL 3:0 FLIP-FLOP ERROR
        SBL 59:56 FLIP-FLOP ERROR
        EXPT 7:0 FLIP-FLOP ERROR
```

4.0 PERFORMANCE AND PROGRESS REPORTS

AT THE END OF EACH PASS, THE PASS COUNT IS GIVEN ALONG WITH THE TOTAL NUMBER OF ERRORS REPORTED SINCE THE DIAGNOSTIC WAS STARTED. THE "EOP" SWITCH CAN BE USED TO CONTROL HOW OFTEN THE END OF PASS MESSAGE IS PRINTED. SECTION 2.2 DESCRIBES SWITCHES.

5.0 DEVICE INFORMATION TABLE:

CONTROL REGISTER 0 (163010)

```
    15  CDAL15  BIT 15 = 1 READ DEVICE TYPE IN BITS 15-8. STATE
                ANALYZER DEVICE TYPE EQUALS 2 (1000)
```

BIT 15 = 0 READ DEVICE NUMBER INTO BITS 11-8.

14	CDAL14	ALWAYS A 0 ON READ
13	CDAL13	ALWAYS A 0 ON READ
12	CDAL12	ALWAYS A 0 ON READ
		BITS 11-8 ARE USED TO SELECT THE DEVICE NUMBER OF THE STATE ANALYZER. THESE BITS MUST BE EQUAL TO THE SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.
11	CDAL11	
10	CDAL10	
9	CDAL9	
8	CDAL8	
7	CDAL7	1 - DISABLE OUTPUTS OF "OR ADDRESS REG" ENABLE FOUT 3:0 TO DRIVE "OR" ADDRESS 0 - ENABLE OUTPUTS OF "OR ADDRESS REG"
6	CDAL6	1/0 CLOCK SIGNAL "TRNST H"
5	CDAL5	1 - STOP TRACING WHEN "TRAD10 H" SET HIGH 0 - CONTINUOUS TRACING
4	CDAL4	1 - ENABLE ALL AND/OR ARRAY RAMS 0 - ENABLE ONLY ONE AND/OR ARRAY RAM
3	CDAL3	TRACE RAM BUS SELECT
2	CDAL2	TRACE RAM BUS SELECT

CDAL3	CDAL2	
0	0	ENABLE OUTPUTS OF TRACE RAM DATA IN BUFFER ONTO TRACE RAM BUS
0	1	ENABLE TRACE RAM DATA ONTO TRACE RAM BUS
1	0	ENABLE SYSTEM BUS AND SBL 59:56 FLIP-FLOPS ONTO TRACE RAM BUS

1	CDAL1	1 - ENABLE FUNCTION SELECT F/F'S ONTO SYSTEM BUS
0	CDAL0	1 - CLEAR TRAM ADDRESS REG, CLEAR TRACING FLIP-FLOP, CLEAR SBL 59:56 FLIP-FLOPS, AND RELOAD EVENT COUNTERS FROM EVENT COUNTER REGISTERS

CONTROL REGISTER 2 (163012)

15-8		BITS 15-8 ARE NOT AVAILABLE IN CONTROL REGISTER 2
7	PDAL7	1 - CLEAR EVENT COUNTERS
6	PDAL6	1 - PRESET TRACING FLIP-FLOP
5	PDAL5	0 - CLEAR FUNCTION SELECTS
4	PDAL4	1 - EXTERNAL PROBE "CLK" SIGNAL WILL LOAD EXTP 7:0 FLIP-FLOP'S WHEN "CLK" IS SET LOW. 0 - EXTERNAL PROBE "CLK" SIGNAL WILL LOAD EXTP 7:0 FLIP-FLOP'S WHEN "CLK" IS SET HIGH.
3	PDAL3	SELECT POINTER REGISTER
2	PDAL2	SELECT POINTER REGISTER
1	PDAL1	SELECT POINTER REGISTER

C 2

0 PDAL0 SELECT POINTER REGISTER

STATE ANALYZER'S POINTER REGISTER AND CONTROL REGISTER 4 (163014)

PDAL BITS 3:0	SIGNAL	DESCRIPTION
00	PTER0 L	WRITE/READ AND ARRAY RAM 0
01	PTER1 L	WRITE/READ AND ARRAY RAM 1
02	PTER2 L	WRITE/READ AND ARRAY RAM 2
03	PTER3 L	WRITE/READ AND ARRAY RAM 3
04	PTER4 L	WRITE/READ AND ARRAY RAM 4
05	PTER5 L	WRITE/READ AND ARRAY RAM 5
06	PTER6 L	WRITE/READ AND ARRAY RAM 6
07	PTER7 L	WRITE/READ AND ARRAY RAM 7
10	PTER8 L	WRITE/READ AND ARRAY RAM 8
11	PTER9 L	WRITE/READ AND ARRAY RAM 9
12	PTER10 L	WRITE/READ AND ARRAY RAM 10
13	PTER11 L	WRITE/READ AND ARRAY RAM 11
14	PTER12 L	WRITE/READ AND ARRAY RAM 12
15	PTER13 L	WRITE/READ AND ARRAY RAM 13
16	PTER14 L	WRITE/READ AND ARRAY RAM 14
17	PTER15 L	WRITE/READ OR ARRAY RAM'S

STATE ANALYZER'S POINTER REGISTER AND CONTROL REGISTER 6 (163016)

PDAL BITS 3:0	SIGNAL	DESCRIPTION
00	PTER0 L	WRITE/READ TRACE RAM (TRAM) ADDRESS REG
01	PTER1 L	WRITE TRAM 15:0 WITH TRDI DATA FROM TRAM BUS SELECTED. READ TRDI 15:0 DATA FROM TRAM BUS SELECTED
02	PTER2 L	WRITE TRAM 31:16 WITH TRDI DATA FROM TRAM BUS SELECTED. READ TRDI 31:16 DATA FROM TRAM BUS SELECTED
03	PTER3 L	WRITE TRAM 47:32 WITH TRDI DATA FROM TRAM BUS SELECTED READ TRDI 47:32 DATA FROM TRAM BUS SELECTED.
04	PTER4 L	WRITE TRAM 55:48 WITH TRDI DATA FROM TRAM BUS SELECTED. READ TRDI 59:48 DATA FROM TRAM BUS SELECTED.
05	PTER5 L	WRITE TRAM DATA IN BUFFER 15:0 FROM Q-BUS DATA BITS 15:0
06	PTER6 L	WRITE TRAM DATA IN BUFFER 31:16 FROM Q-BUS DATA BITS 15:0.
07	PTER7 L	WRITE TRAM DATA IN BUFFER 47:32 FROM Q-BUS DATA BITS 15:0
10	PTER8 L	WRITE TRAM DATA IN BUFFER 59:48 FROM Q-BUS DATA BITS 11:0.
11	PTER9 L	LOAD EVENT COUNTER REGISTER 0 AND EVENT COUNTER 0. CLEAR SBL56 FLIP-FLOP
12	PTER10 L	LOAD EVENT COUNTER REGISTER 1 AND EVENT COUNTER 1. CLEAR SBL57 FLIP-FLOP.
13	PTER11 L	LOAD EVENT COUNTER REGISTER 2 AND EVENT COUNTER 2. CLEAR SBL58 FLIP-FLOP.
14	PTER12 L	LOAD EVENT COUNTER REGISTER 3 AND EVENT COUNTER 3. CLEAR SBL59 FLIP-FLOP
15	PTER13 L	NOT USED

16	PTER14 L	NOT USED
17	PTER15 L	READ/WRITE OR ADDRESS REGISTER (CDAL7=0) READ FOUT F/F'S ON 'OR ADDRESS BITS (CDAL7=1)

NOTE: THE TRACE RAM (TRAM) BUS SELECTED IS CONTROLLED BY CONTROL REGISTER 0 BITS CDAL3 AND CDAL2.

6.0 TEST SUMMARIES

TEST 1:

THIS TEST WILL CHECK THAT THE STATE ANALYZER CAN BE SELECTED AND INITIALIZED TO A KNOWN STATE. THIS TEST WILL BE EXECUTED AT THE BEGINNING OF EVERY TEST TO PUT THE MODULE IN A KNOWN STATE. THE TEST WILL LOAD THE DEVICE NUMBER INTO CONTROL REGISTER 0 AND CHECK THAT THE DEVICE NUMBER CAN BE READ BACK CORRECTLY. THE LOW BYTE OF CONTROL REGISTER 0 WILL BE CHECKED TO BE ZERO. THE TEST WILL THEN LOAD THE DEVICE NUMBER AND THE SIGNAL CDAL15 INTO CONTROL REGISTER 0 AND CHECK THAT THE DEVICE TYPE AND THE LOW BYTE CAN BE READ BACK CORRECTLY. THE TEST WILL THEN CLEAR THE SIGNAL CDAL15 IN CONTROL REGISTER 0 AND CHECK THE DEVICE NUMBER IN THE LOW BYTE AGAIN. THE TES" WILL ALSO LOAD ALL ZEROES INTO CONTROL REGISTER 2 AND CHECK THAT ALL ALL ZEROES CAN BE READBACK FROM CONTROL REGISTER 2.

TEST 2:

THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS CDAL7, CDAL6, CDAL5, CDAL4, CDAL3, CDAL2, CDAL1 AND CDAL0 CAN BE SET TO ALL ONES AND THEN ALL ZEROES.

TEST 3:

THIS TEST WILL CHECK CONTROL REGISTER 0 READ/WRITE BITS CDAL7 TO CDAL0 WITH AN ALTERNATING ONES AND ZEROES PATTERN (252) AND THEN AN ALTERNATING ZEROES AND ONES PATTERN (125).

TEST 4:

THIS TEST WILL CHECK CONTROL REGISTER 0 READ/WRITE BITS CDAL7 TO CDAL0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT UNTIL THE TEST PATTERN 377 HAS BEEN LOADED INTO CONTROL REGISTER 0 AND CHECKED.

TEST 5:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS, PDAL7, PDAL6 PDAL5, PDAL4, PDAL3, PDAL2, PDAL1, AND PDAL0, TO BE SET TO ALL ONES AND THEN TO ALL ZEROES.

TEST 6:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7 TO PDAL0 WITH AN ALTERNATING ONES AND ZEROES PATTERN (252) AND THEN AN ALTERNATING ZEROES AND ONES PATTERN (125).

TEST 7:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7 TO PDAL0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT UNTIL THE TEST PATTERN 377 HAS BEEN LOADED AND TESTED.

TEST 8:

THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) BY LOADING A PATTERN OF ALL ONES (3777) INTO THE ADDRESS REGISTER AND THEN READING AND CHECKING THE ADDRESS REGISTER FOR ALL ONES. THE TEST WILL THEN LOAD, READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH A DATA PATTERN OF ALL ZEROES. TO WRITE AND READ THE TRACE RAM ADDRESS REGISTER, THE PROGRAM WILL CLEAR CONTROL REGISTER 0 BITS CDAL7 TO CDAL0, CLEAR CONTROL REGISTER 2 BITS PDAL7 TO PDAL0, LOAD THE DATA PATTERN INTO THE TRACE RAM ADDRESS REGISTER VIA A WRITE COMMAND TO CONTROL REGISTER 6, AND THEN READ THE TRACE RAM ADDRESS REGISTER VIA A READ COMMAND TO CONTROL REGISTER 6. WHEN PDAL3 TO PDAL0 ARE SET TO A 0, THE SIGNAL PTERO L WILL BE ASSERTED LOW IN THE POINTER REGISTER. THIS SIGNAL BEING SET LOW, ALONG WITH A WRITE OR READ COMMAND TO CONTROL REGISTER 6 WILL ASSERT THE SIGNALS WPTO L AND RPTO L RESPECTIVELY. THE SIGNAL WPTO L WILL LOAD THE ADDRESS INTO THE TRACE RAM ADDRESS REGISTER, AND THE SIGNAL RPTO L WILL READ THE ADDRESS FROM THE TRACE RAM ADDRESS REGISTER.

TEST 9:

THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) BY LOADING AN ALTERNATING ONES AND ZEROES PATTERN (2525) INTO THE TRACE RAM ADDRESS REGISTER AND THEN READING AND CHECKING THE ADDRESS REGISTER FOR THE PATTERN LOADED. THE TEST WILL THEN LOAD, READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH AN ALTERNATING ZEROES AND ONES DATA PATTERN (1252).

TEST 10:

THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) USING A BINARY COUNT PATTERN. THE DATA PATTERN WILL START WITH ZERO AND INCREMENT BY ONE UNTIL THE DATA PATTERN 3777 HAS BEEN LOADED AND CHECKED.

TEST 11:

THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE CLEARED WHEN CONTROL REGISTER 0 SIGNAL CDAL 0 H IS SET TO A ONE. THE TEST WILL LOAD ALL ONES (3777) INTO THE TRACE RAM ADDRESS REGISTER AND CHECK THAT ALL ONES WERE LOADED. THE TEST WILL THEN SET THE SIGNAL CDAL 0 H TO A ONE IN CONTROL REGISTER 0 AND THEN READ THE TRACE RAM ADDRESS REGISTER CHECKING IT TO BE 0. THE SIGNAL CDAL 0 H WILL THEN BE CLEARED AND THE TRACE RAM ADDRESS REGISTER WILL BE CHECKED AGAIN TO CONTAIN ALL ZEROES.

TEST 12:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI15 H TO TRDI0 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL ZEROES (000000).

TEST 13:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI15 H TO TRDI0 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TEST 14:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI31 H TO TRDI16 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL ZEROES (000000).

TEST 15:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI31 H TO TRDI16 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TEST 16:

THIS TEST WILL CHCEK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI47 H TO TRDI32 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL ZEROES (000000)

TEST 17:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI47 H TO TRDI32 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TEST 18:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI59 H TO TRDI48 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (007777) AND THEN ALL ZEROES (000000).

TEST 19:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI59 H TO TRDI48 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (005252) AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (002525).

TEST 20:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTERS FROM THE LSI-11 BUS TO BE SELECTED CORRECTLY BY THE POINTER REGISTER. THE TEST WILL WRITE AND CHECK TRDI BITS 15:0 WITH A DATA PATTERN EQUAL TO 1, TRDI BITS 31:16 WITH A DATA PATTERN EQUAL TO 2, TRDI BITS 47:32 WITH A DATA PATTERN EQUAL TO 3 AND TRDI BITS 59:48 WITH A DATA PATTERN EQUAL TO 4. THE TEST WILL READ EACH SET OF TRACE RAM DATA IN BITS CHECKING THE BUFFERS TO CONTAIN THE CORRECT DATA PATTERN.

TEST 21:

THIS TEST WILL CHECK TRACE RAM BITS TRDI 15:0 WITH A DATA PATTERN OF 125252 AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED WITH THESE DATA PATTERNS.

TEST 22:

THIS TEST WILL CHECK TRACE RAM BITS TRDI 31:16 WITH A DATA PATTERN OF 125252 AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED WITH THESE DATA PATTERNS.

TEST 23:

THIS TEST WILL CHECK TRACE RAM BITS TRDI 47:32 WITH A DATA PATTERN OF 125252 AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED WITH THESE DATA PATTERNS.

TEST 24:

THIS TEST WILL CHECK TRACE RAM BITS TRDI 55:48 WITH A DATA PATTERN OF 252 AND 525. EACH LOCATION OF THE TRACE RAM WILL BE CHECKED WITH THESE DATA PATTERNS. HOWEVER THE TRACE RAM DATA IN BUFFERS WHICH LOAD TRACE RAM BITS TRDI 55:48 WILL BE LOADED WITH DATA PATTERNS 5252 AND 2525. TRACE RAM DATA IN BUFFER BITS 59:56 ARE NOT LOADED INTO ANY TRACE RAMS.

TEST 25:

THIS TEST WILL CHECK TRACE RAM TRDI 15:0 TO BE ADDRESSED CORRECTLY AND THAT NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIPS. THE TEST WILL LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND CHECK THE LOCATION TO CONTAIN AS DATA ITS ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN. THE TEST WILL REPEAT THIS SEQUENCE FOR ALL ADDRESSES OF THE TRACE RAM. WHEN ALL ADDRESSES HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND READ EACH LOCATION OF THE 1K TRACE RAM CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

TEST 26:

THIS TEST WILL CHECK TRACE RAM TRDI 31:16 TO BE ADDRESSED CORRECTLY AND THAT NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIPS. THE TEST WILL LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS

ADDRESS. ONCE ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND CHECK THE LOCATION TO CONTAIN AS DATA ITS ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN. THE TEST WILL REPEAT THIS SEQUENCE FOR ALL ADDRESSES OF THE TRACE RAM. WHEN ALL ADDRESSES HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND READ EACH LOCATION OF THE 1K TRACE RAM CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

TEST 27:

THIS TEST WILL CHECK TRACE RAM TRDI 47:32 TO BE ADDRESSED CORRECTLY AND THAT NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIPS. THE TEST WILL LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND CHECK THE LOCATION TO CONTAIN AS DATA ITS ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN. THE TEST WILL REPEAT THIS SEQUENCE FOR ALL ADDRESSES OF THE TRACE RAM. WHEN ALL ADDRESSES HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND READ EACH LOCATION OF THE 1K TRACE RAM CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

TEST 28:

THIS TEST WILL CHECK TRACE RAM TRDI 55:48 TO BE ADDRESSED CORRECTLY AND THAT NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIPS. THE TEST WILL LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND CHECK THE LOCATION TO CONTAIN AS DATA ITS ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN. THE TEST WILL REPEAT THIS SEQUENCE FOR ALL ADDRESSES OF THE TRACE RAM. WHEN ALL ADDRESSES HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND READ EACH LOCATION OF THE 1K TRACE RAM CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

TEST 29:

THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN COUNT UP BY ONE WHEN THE SIGNAL "CTR L" IS PULSED. THE TRACE RAM ADDRESS REGISTER WILL BE COUNTED UP BY ONE FROM ADDRESS 0 TO ADDRESS 3777 AND THEN BACK TO ADDRESS 0. IN ORDER TO PULSE THE SIGNAL "CTR L", THE PROGRAM WILL SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0 WHICH WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE, WHICH WILL CAUSE THE SIGNAL ARST L TO PULSE, WHICH WILL PULSE THE SIGNAL ORST L. WITH THE TRACING FLIP-FLOP HELD IN THE PRESET STATE BY THE SIGNAL PDAL6 BEING SET TO A ZERO AND THE SIGNALS TRST L AND TRANST H BEING PULSED, A PULSE WILL OCCUR ON THE SIGNAL CTR L.

TEST 30:

THIS TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET BY PDAL6 IN CONTROL REGISTER 2 AND CLEARED BY CDAL0 IN CONTROL REGISTER 0.

TEST 31:

THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE INCREMENTED BY ONE VIA THE SIGNAL "CTR L" WHEN THE TRACING FLIP-FLOP IS SET TO A ONE, CDAL REGISTER BIT 5 IS SET TO A ONE, TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ZERO AND THE SIGNALS TRST L AND TRANST H ARE PULSED. THE TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER WILL NOT GET INCREMENTED BY THE SIGNAL "CTR L" WHEN THE TRACING FLIP-FLOP IS SET TO ONE, CDAL REGISTER BIT 5 IS SET TO A ONE, TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE AND THE SIGNALS TRST L AND TRANST H ARE PULSED. THE TEST WILL THEN CHECK THAT THE TRACE RAM ADDRESS REGISTER WILL GET INCREMENTED BY VIA VIA THE SIGNAL "CTR L" WHEN THE TRACING FLIP-FLOP IS SET TO A ONE, CDAL REGISTER BIT 5 IS SET TO A ZERO, TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE AND THE SIGNALS TRST L AND TRANST H ARE PULSED.

TEST 32:

THE TEST WILL CHECK THAT THE TRACE RAMS CAN BE LOADED FROM THE TRACE RAM DATA IN BUFFERS VIA THE SIGNALS "CTR H" AND "CTR L".

THE TEST WILL LOAD AND CHECK EACH TRACE RAM DATA IN BUFFER WITH THE FOLLOWING DATA PATTERNS:

    TRDI 15:0 - DATA PATTERN OF 151515
    TRDI 31:16 - DATA PATTERN OF 113131
    TRDI 47:32 - DATA PATTERN OF 074747
    TRDI 59:48 - DATA PATTERN OF 005555

THE TEST WILL ASSERT THE SIGNAL TRSL0 L BY CLEARING THE LOW BYTE OF CONTROL REGISTER 0. THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS. THE TEST WILL LOAD ADDRESS 0 INTO THE TRACE RAM ADDRESS REGISTER TO SELECT ADDRESS 0 OF ALL TRACE RAMS. THE TEST WILL THEN PRESET THE TRACING FLIP-FLOP TO THE HIGH STATE BY SETTING THE BIT PDAL6 IN CONTROL REGISTER 2. THE TEST WILL NOW SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0. SETTING AND CLEARING THE SIGNAL CDAL6 WITH THE TRACING FLIP-FLOP IN THE PRESET STATE, WILL CAUSE THE SIGNALS CTR L AND CTR H TO PULSE. THE SIGNAL CTR L WILL INCREMENT THE TRACE RAM ADDRESS REGISTER BY ONE. THE SIGNALS CTR L AND CTR H WILL LOAD THE TRACE RAM DATA IN BUFFERS INTO ADDRESS 0 OF TRACE RAM BITS TRDI 55:0. AFTER SETTING AND CLEARING CDAL6, THE PROGRAM WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER INCREMENTED TO ADDRESS 1. THE TEST WILL THEN RESET THE TRACE RAM ADDRESS REGISTER TO ADDRESS 0. THE TEST WILL THEN ASSERT THE SIGNAL TRSL1 L BY SETTING THE SIGNAL CDAL2 IN CONTROL REGISTER 0. THE SIGNAL TRSL1 L WILL ENABLE THE TRACE RAMS TO BE READ. THE TEST WILL NOW READ ADDRESS 0 OF EACH TRACE RAM CHECKING THE DATA TO BE THAT WHICH WAS WRITTEN PREVIOUSLY INTO THE TRACE RAM DATA IN BUFFERS.

TEST 33:

THIS TEST WILL CHECK THE OR ADDRESS REGISTER BITS (ORAD3-ORAD0) BY

LOADING AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND THEN LOADING AND ALTERNATING ZEROES AND ONES DATA PATTERN (05). TO WRITE AND READ THE OR ADDRESS REGISTER, THE PROGRAM WILL CLEAR CONTROL REGISTER 0 BITS (CDAL7-CDAL0). CDAL7 BEING A ZERO WILL ENABLE THE OUTPUTS OF THE OR ADDRESS REGISTER. THE PROGRAM WILL SET PDAL3 TO PDAL0 TO A ONE IN CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER15 L TO BE ASSERTED IN THE POINTER REGISTER. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H. THE SIGNAL WPT15 H WILL LOAD THE DATA FROM BITS 3-0 ON THE WRITE COMMAND INTO OR ADDRESS REGISTER BITS (ORAD3-ORAD0). ON A READ COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL RPT15 H. THE SIGNAL RPT15 H WILL READ THE DATA FROM THE OR ADDRESS REGISTER.

TEST 34:

THIS TEST WILL CHECK THE OR ADDRESS REGISTER BITS ORAD3 TO ORAD0 USING A BINARY COUNT PATTERN STARTING WITH A DATA PATTERN OF ZERO AND INCREMENTING THE PATTERN BY ONE UNTIL THE DATA PATTERN 17 HAS BEEN LOADED AND CHECKED.

TEST 35:

THIS TEST WILL CHECK EACH LOCATION OF THE OR ARRAY RAM (ORO 7:0) WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (125).

THE FOLLOWING SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE OR ARRAY RAM. THE TEST WILL CLEAR ALL THE LOW BITS IN CONTROL REGISTER 0. CDAL7 ENABLES OR ADDRESS REGISTER OUTPUTS. CDAL4 ON A ONE WILL ALLOW ONLY ONE AND/OR ARRAY TO BE SELECTED VIA THE POINTER REGISTER. THE OR ARRAY RAMS WILL BE SELECTED IN THIS TEST BY SETTING PTER15 L IN THE POINTER REGISTER WHICH WILL CAUSE THE SIGNAL PLSL15 L TO BE ASSERTED. THE SIGNAL PLSL15 L WILL ENABLE THE OR ARRAY RAMS TO BE WRITTEN OR READ. THE TEST WILL LOAD THE ADDRESS TO BE TESTED INTO THE OR ADDRESS REGISTER. TO LOAD THE ADDRESS, THE PROGRAM WILL ISSUE A WRITE COMMAND TO CONTROL REGISTER 6. WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH WILL LOAD THE OR ADDRESS REGISTER. TO READ THE OR ADDRESS REGISTER, THE TEST WILL ISSUE A READ COMMAND TO CONTROL REGISTER 6 WHICH WILL CAUSE A PULSE ON THE SIGNAL RPT15 H. THE SIGNAL RPT15 H WILL READ THE DATA FROM THE OR ADDRESS REGISTER. THE TEST WILL NOW WRITE AND READ THE OR ARRAY LOCATION WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252). TO WRITE THE OR ARRAY RAM LOCATION, THE TEST WILL ISSUE A WRITE COMMAND TO CONTROL REGISTER 4. WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPLA15 L. THE SIGNAL WPLA15 L WILL WRITE THE DATA INTO THE OR ARRAY RAM LOCATION. TO READ THE OR ARRAY RAM LOCATION, THE TEST WILL ISSUE A READ COMMAND TO CONTROL REGISTER 4. THE TEST WILL NOW LOAD, READ AND CHECK THE RAM LOCATION WITH AN ALTERNATING ZEROS AND ONES DATA PATTERN (125).

TEST 36:

THIS TEST WILL CHECK THAT ALL ADDRESSES IN THE OR ARRAY RAMS CAN BE ADDRESSED CORRECTLY AND THAT WRITING ONE ADDRESS WILL NOT WRITE ANOTHER

ADDRESS PREVIOUSLY WRITTEN (ADDRESS SHORT). THE TEST WILL WRITE AND CHECK EACH LOCATION OF THE OR ARRAY RAM WITH DATA EQUAL TO ITS ADDRESS. THE DATA PATTERN FOR THE TOP 4 BITS OF THE OR ARRARY RAM WILL BE THE SAME AS THE DATA PATTERN FOR THE LOW 4 BITS OF THE OR ARRAY RAM. AFTER WRITING ALL LOCATIONS OF THE OR ARRAY RAM, THE TEST WILL READ EACH LOCATION OF THE RAM CHECKING THE DATA TO BE EQUAL TO ITS ADDRESS. THE TEST WILL THEN READ EACH LOCATION CHECKING THE DATA TO BE EQUAL TO ITS ADDRESS AND THEN WRITING AND CHECKING THE LOCATION WITH THE ONES COMPLEMENT OF ITS ADDRESS. IF A LOCATION ON THE FIRST READ DOES NOT EQUAL ITS ADDRESS, THEN WRITING A PREVIOUS LOCATION PROBABLY WROTE THE LOCATION IN ERROR ALSO. AFTER ALL LOCATIONS HAVE BEEN TESTED IN THIS MANNER THE PROGRAM WILL READ THE OR ARRAY RAMS AGAIN CHECKING EACH LOCATION TO CONTAIN AS DATA THE ONES COMPLEMENT OF ITS ADDRESS.

TEST 37:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL0 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 3:0.

TEST 38:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL1 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 7:4.

TEST 39:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL2 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 11:8.

TEST 40:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL3 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 15:12.

TEST 41:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL4 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 19:16.

TEST 42:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL5 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 23:20.

TEST 43:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL6 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 27:24.

TEST 44:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL7 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 31:28.

TEST 45:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL8 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 35:32.

TEST 46:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL9 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 39:36.

TEST 47:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL10 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 43:40.

TEST 48:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL11 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 47:44.

TEST 49:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL12 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 51:48.

TEST 50:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL13 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 55:52.

TEST 51:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL14 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 59:56.

TEST 52:

THIS TEST WILL CHECK THAT EACH AND ARRAY IS ACTUALLY SELECTED WHEN ADDRESSED BY THE PLSL SELECT LINE SIGNALS. THE PLSL SELECT SIGNALS ARE GENERATED BY THE POINTER REGISTER PTER SIGNALS VIA CONTROL REGISTER 2. THE TEST WILL CLEAR ALL TRACE RAM DATA IN BUFFER BITS TRDI 59:0. WITH ALL THESE BITS BEING CLEARED, LOCATION 0 OF EACH AND ARRAY WILL BE ADDRESSED. THE TEST WILL THEN SELECT EACH AND ARRAY BY LOADING THE APPROPRIATE PTER SIGNAL IN CONTROL REGISTER 2. THE TEST WILL THEN LOAD, READ AND CHECK THE AND ARRAY WITH THE PTER SIGNAL USED TO SELECT THE AND ARRAY. ONCE EACH AND ARRAY HAS BEEN LOADED AND CHECKED, THE TEST WILL THEN RE-SELECT EACH AND ARRAY CHECKING THE DATA TO BE EQUAL TO THE PTER SELECT SIGNAL. IF ANY ERRORS OCCUR IN THE LAST PORTION OF THE TEST THEN THE ERROR IS PROBABLY RELATED TO THE PLSL SIGNALS OR THE POINTER REGISTER PTER SIGNALS. ONLY ONE AND ARRAY SHOULD BE ENABLED AT A TIME DURING THIS TEST VIA CDAL4 ON A ONE AND THE PTER SELECT SIGNAL.

TEST 53:

THIS TEST WILL CHECK THAT EACH AND ARRAY CAN BE ADDRESSED CORRECTLY AND THAT WRITING ONE LOCATION IN THE AND ARRAY DOES NOT WRITE A HIGHER LOCATION AT THE SAME TIME (ADDRESS SHORT). THE TEST WILL CHECK ONE AND ARRAY AT A TIME UNTIL ALL AND ARRAYS ARE TESTED. THE TEST WILL LOAD AND CHECK EACH LOCATION OF A 16*4 AND ARRAY WITH DATA EQUAL TO THE ADDRESS SELECTED (0-17 OCTAL). ONCE ALL THE LOCATIONS HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL START AT THE BEGINNING ADDRESS OF THE AND ARRAY AND DO THE FOLLOWING:

1. READ LOCATION CHECKING DATA TO EQUAL THE ADDRESS (0-17)
2. WRITE AND CHECK LOCATION WITH THE 1'S COMPLEMEMNT OF ADDRESS
3. SEQUENCE TO NEXT ADDRESS
4 REPEAT STEPS 1-3 UNTIL ALL ADDRESSES HAVE BEEN CHECKED

WHEN THE ABOVE SEQUENCE HAS BEEN COMPLETED, THE TEST WILL RESET THE

ADDRESS TO THE BEGINNING ADDRESS OF THE AND ARRAY AND CHECK EACH LOCATION TO CONTAIN THE 1'S COMPLEMENT OF THE ADDRESS.

TEST 54:

THIS TEST WILL CHECKOUT EVENT COUNTER LOGIC FOR EVENT COUNTERS 0 AND 2. THE TEST WILL CHECK THAT THE EVENT COUNTER REGISTERS AND EVENT COUNTERS ARE LOADED CORRECTLY BY COUNTING DOWN THE EVENT COUNTERS AND CHECKING THE FOUT FLIP-FLOPS FOR A BORROW. WHEN THE EVENT COUNTERS ARE COUNTED DOWN TO ZERO AND ONE MORE COUNT DOWN IS ISSUED, A BORROW IS GENERATED WHICH WILL SET THE OUTPUT OF THE FOUT FLIP-FLOP TO A LOW STATE. THE TEST WILL CHECK THAT THE EVENT COUNTERS ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN A BORROW IS GENERATED. THIS IS DONE BY COUNTING DOWN THE EVENT COUNTERS AGAIN CHECKING FOR A BORROW FROM THE EVENT COUNTERS. THE TEST WILL THEN CHECK THAT THE EVENT COUNTERS CAN BE CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7. AFTER SETTING AND CLEARING THE SIGNAL PDAL7, THE TEST WILL DO ONE MORE COUNT DOWN AND CHECK THAT A BORROW IS GENERATED FROM THE EVENT COUNTERS. THE ABOVE SEQUENCE IS REPEATED WITH EACH OF THE FOLLOWING DATA PATTERNS: 0, 1, 2, 4, 10, 20, 40, 100, 200, 125, AND 252.

TEST 55:

THIS TEST WILL CHECKOUT EVENT COUNTER LOGIC FOR EVENT COUNTERS 1 AND 3. THE TEST WILL CHECK THAT THE EVENT COUNTER REGISTERS AND EVENT COUNTERS ARE LOADED CORRECTLY BY COUNTING DOWN THE EVENT COUNTERS AND CHECKING THE FOUT FLIP-FLOPS FOR A BORROW. WHEN THE EVENT COUNTERS ARE COUNTED DOWN TO ZERO AND ONE MORE COUNT DOWN IS ISSUED, A BORROW IS GENERATED WHICH WILL SET THE OUTPUT OF THE FOUT FLIP-FLOP TO A LOW STATE. THE TEST WILL CHECK THAT THE EVENT COUNTERS ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN A BORROW IS GENERATED. THIS IS DONE BY COUNTING DOWN THE EVENT COUNTERS AGAIN CHECKING FOR A BORROW FROM THE EVENT COUNTERS. THE TEST WILL THEN CHECK THAT THE EVENT COUNTERS CAN BE CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7. AFTER SETTING AND CLEARING THE SIGNAL PDAL7, THE TEST WILL DO ONE MORE COUNT DOWN AND CHECK THAT A BORROW IS GENERATED FROM THE EVENT COUNTERS. THE ABOVE SEQUENCE IS REPEATED WITH EACH OF THE FOLLOWING DATA PATTERNS: 0, 1, 2, 4, 10, 20, 40, 100, 200, 125, AND 252.

TEST 56:

THIS TEST WILL CHECK THAT THE SIGNAL CDAL0, WHEN SET AND CLEARED, WILL CAUSE THE EVENT COUNTERS TO BE LOADED FROM THE EVENT COUNTER REGISTERS.

TEST 57:

THIS TEST WILL CHECK THAT FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3, AND FUSL1 CAN BE SET TO A ONE AND THAT FUNCTION SELECT FLIP-FLOPS FUSL2 AND FUSL0 CAN BE SET TO A ZERO. THE FUNCTION SELECT FLIP-FLOPS ARE SET TO THE STATE MENTIONED VIA THE DATA FROM THE OR ARRAY RAM AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. AFTER CHECKING THAT THE FUNCTION SELECT FLIP-FLOPS ARE IN THE CORRECT STATE VIA CONTROL REGISTER 4 AND CONTROL REGISTER 6, THE TEST WILL SET THE SIGNAL PDAL5 TO A 0 IN CONTROL REGISTER 2. PDAL5 ON A ZERO WILL PRESET THE FUNCTION SELECT FLIP-FLOPS TO THE ZERO STATE. THE TEST WILL THEN VERIFY THAT THE FLIP-FLOPS ARE CLEARED BY READING CONTROL REGISTER

4 AND CONTROL REGISTER 6 AGAIN.

TEST 58:

THIS TEST WILL CHECK THAT FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3, AND FUSL1 CAN BE SET TO A ZERO AND THAT FUNCTION SELECT FLIP-FLOPS FUSL2 AND FUSL0 CAN BE SET TO A ONE. THE FUNCTION SELECT FLIP-FLOPS ARE SET TO THE STATE MENTIONED VIA THE DATA FROM THE OR ARRAY RAM AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. AFTER CHECKING THAT THE FUNCTION SELECT FLIP-FLOPS ARE IN THE CORRECT STATE VIA CONTROL REGISTER 4 AND CONTROL REGISTER 6, THE TEST WILL SET THE SIGNAL PDAL5 TO A 0 IN CONTROL REGISTER 2. PDAL5 ON A ZERO WILL PRESET THE FUNCTION SELECT FLIP-FLOPS TO THE ZERO STATE. THE TEST WILL THEN VERIFY THAT THE FLIP-FLOPS ARE CLEARED BY READING CONTROL REGISTER 4 AND CONTROL REGISTER 6 AGAIN.

TEST 59:

THIS TEST WILL CHECK THAT THE EVENT COUNTERS WILL GET RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE OUTPUT OF FUNCTION SELECT FLIP-FLOP FUSL7 H IS SET TO THE HIGH STATE. TO CHECK THAT THIS HAPPENS, THE TEST WILL LOAD ALL EVENT COUNTERS WITH THE VALUE 377 OCTAL. THE TEST WILL THEN COUNT DOWN THE EVENT COUNTERS UNTIL THE EVENT COUNTERS EQUAL 200 OCTAL. THE TEST CHECKS THAT NO BORROWS ARE GENERATED FROM THE EVENT COUNTERS WHEN THE EVENT COUNTERS ARE COUNTED DOWN. THIS IS DONE BY CHECKING FOUT 3:0 FLIP-FLOPS ON THE ORAD 3:0 SIGNAL LINES. THE TEST WILL THEN LOAD LOCATION ZERO OF THE "OR ARRAY RAM" WITH A DATA PATTERN OF 200 OCTAL WHICH WILL CAUSE THE SIGNAL "ORO 7 L" TO BE ASSERTED LOW. THE TEST WILL THEN SET AND CLEAR THE SIGNAL CDAL6 WHICH WILL CAUSE THE SIGNAL ANST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE PULSED. UPON THE PULSING OF THE SIGNAL ORST L THE "OR ARRAY" DATA WILL BE LOADED INTO THE FUNCTION SELECT FLIP-FLOPS, THUS SETTING THE OUTPUT OF FUSL7 H FLIP-FLOP TO THE HIGH STATE. WHEN FUSL7 H FLIP-FLOP IS SET HIGH, A ONE SHOT WILL BE FIRED WHICH WILL CAUSE THE EVENT COUNTERS TO BE LOADED FROM THE EVENT COUNTER REGISTERS. TO TEST THAT THE EVENT COUNTERS WERE RELOADED FROM THE EVENT COUNTER REGISTERS, THE TEST WILL COUNT DOWN THE EVENT COUNTERS 400 OCTAL TIMES CHECKING THAT NO BORROWS ARE GENERATED FROM THE EVENT COUNTERS UNTIL THE LAST COUNT DOWN IS ISSUED.

TEST 60:

THIS TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET BY FUNCTION SELECT FLIP-FLOP FUSL0 H AND CLEARED BY FUNCTION SELECT FLIP-FLOP FUSL1 H. THE TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET AND CLEARED BY CHECKING THE TRACE RAM ADDRESS REGISTER. THE TRACE RAM ADDRESS REGISTER WILL NOT BE INCREMENTED WHEN THE TRACING FLIP-FLOP IS CLEARED AND CDAL6 IS SET AND CLEARED IN CONTROL REGISTER 0, PULSING TRST L AND TRANST H. THE TRACE RAM ADDRESS REGISTER WILL BE INCREMENTED WHEN THE TRACING FLIP-FLOP IS SET AND CDAL6 IS SET AND CLEARED IN CONTROL REGISTER 0 PULSING TRST L AND TRANST H. THE FUNCTION SELECT FLIP-FLOPS ARE SET AND CLEARED VIA THE "OR ARRAY RAM" DATA AND THE SIGNAL ORST L BEING PULSED.

TEST 61:

THIS TEST WILL CHECK THAT SBL56 AND SBL58 FLIP-FLOPS CAN BE SET AND

CLEARED. SBL57 AND SBL59 ARE CHECKED TO REMAIN CLEARED DURING THIS TEST. SBL 59:56 FLIP-FLOPS ARE CHECKED BY THE PROGRAM ON THE TRACE RAM DATA IN BUS SIGNAL LINES TRDI 59:56 WHEN THE SIGNAL "TRSL2 L" IS ASSERTED LOW. SBL56 FLIP-FLOP IS SET VIA A BORROW FROM EVENT COUNTER 0 AND A COUNT DOWN PULSE TO EVENT COUNTER 0. SBL56 FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 0. SBL58 FLIP-FLOP IS S BY "OR ARRAY RAM" DATA "ORO4 L" BEING SET LOW AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. SBL58 FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 2.

TEST 62:

THIS TEST WILL CHECK THAT SBL57 AND SBL59 FLIP-FLOPS CAN BE SET AND CLEARED. SBL56 AND SBL58 ARE CHECKED TO REMAIN CLEARED DURING THIS TEST. SBL 59:56 FLIP-FLOPS ARE CHECKED BY THE PROGRAM ON THE TRACE RAM DATA IN BUS SIGNAL LINES TRDI 59:56 WHEN THE SIGNAL "TRSL2 L" IS ASSERTED LOW. SBL57 FLIP-FLOP IS SET VIA A BORROW FROM EVENT COUNTER 1 AND A COUNT DOWN PULSE TO EVENT COUNTER 1. SBL57 FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 1. SBL59 FLIP-FLOP IS SET BY "OR ARRAY RAM" DATA "ORO5 L" BEING SET LOW AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. SBL59 FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 3.

TEST 63:

THIS TEST WILL CHECK THAT SBL 59:56 FLIP-FLOPS CAN BE SET AND THAT THEY CAN BE CLEARED BY SETTING AND CLEARING CDAL0 IN CONTROL REGISTER 0. SBL57 AND SBL56 FLIP-FLOPS ARE SET VIA A BORROW FROM EVENT COUNTER 1 AND EVENT COUNTER 0 ALONG WITH THE APPROPRIATE COUNT DOWN PULSES. SBL59 AND SBL58 ARE SET VIA "OR ARRAY RAM" DATA BITS "ORO5 L" AND "ORO4 L" BEING SET LOW AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. THE TEST WILL CHECK THE SBL FLIP-FLOPS TO BE SET BY READING THE TRACE RAM DATA IN BUS BITS TRDI 59:56 WHEN THE SIGNAL TRSL2 L IS ASSERTED LOW. THE TEST WILL THEN SET AND CLEAR CDAL0 IN CONTROL REGISTER 0 AND CHECK THAT SBL 59:56 FLIP-FLOPS CLEARED.

TEST 64:

IF THE OPERATOR ANSWERED YES TO THE HARDWARE QUESTION "EXTERNAL PROBE CONNECTED", THE FOLLOWING TEST WILL BE EXECUTED, OTHERWISE, THE TEST WILL BE ABORTED. BEFORE THIS TEST CAN BE PERFORMED, THE OPERATOR MUST PLUG THE EXTERNAL PROBE INTO THE STATE ANALYZER AND CONNECT THE PROBE LEADS 7:0 TO EVENT COUNTER 0 SIGNALS SDBL 7:0 H RESPECTIVELY. THE PROBE'S CLK LEAD MUST BE CONNECTED TO EVENT COUNTER 1 SIGNAL SDBL8 H.

THE TEST WILL CHECK THE EXTERNAL PROBE AND THE EXTERNAL PROBE LOGIC ON THE STATE ANALYZER MODULE. DATA PATTERNS OF 252 AND 125 WILL BE LOADED INTO EVENT COUNTER 0 TO PROVIDE LOGIC LEVELS TO THE EXTERNAL PROBE. THE SIGNAL SDBL8 L IN EVENT COUNTER 1 WILL BE SET AND CLEARED TO PROVIDE THE "CLK" SIGNAL FOR THE EXTERNAL PROBE. WHEN PDAL4, IN CONTROL REGISTER 2, IS SET TO A ZERO, AND THE CLK SIGNAL IS SET HIGH FROM A LOW STATE, EVENT COUNTER 0'S DATA WILL BE LOADED INTO EXTP 7:0 FLIP-FLOPS. WHEN PDAL4 IS SET TO A ONE AND THE CLK SIGNAL IS SET LOW FROM A HIGH STATE, EVENT COUNTER 0'S DATA WILL BE LOADED INTO EXTP 7:0 FLIP-FLOPS. THE TEST WILL CHECK THAT THE CORRECT DATA IS LOADED INTO EXTP 7:0 FLIP-FLOPS AND THAT THE DATA IS ONLY LOADED ON THE CORRECT TRANSITION OF THE CLK SIGNAL.

EXTP 7:0 FLIP-FLOPS ARE READBACK ON THE TRACE RAM DATA IN BUS SIGNAL LINES TRDI 55:48 WHEN THE SIGNAL TRSL2 L IS ASSERTED LOW.

TEST 65:

THE FOLLOWING TEST WILL CHECK THAT INIT L CAN CLEAR CONTROL REGISTER 2 AND THE LOW BYTE OF CONTROL REGISTER 0. THIS IS DONE BY LOADING ALL ONES INTO CONTROL REGISTER 2 AND THE LOW BYTE OF CONTROL REGISTER 0. THEN A BRESET INSTRUCTION IS ISSUED WHICH SHOULD CLEAR REG 2 AND THE LOW BYTE OF REG 0.

&

```
                                .TITLE PROGRAM HEADER AND TABLES
                                .SBTTL  PROGRAM HEADER

                                        .ENABL  ABS
                                        .ENABL  AMA
                                        .DSABL  GBL
002000                                  .       =       2000

002000                                  BGNMOD

                                ;++
                                ; THE PROGRAM HEADER IS THE INTERFACE BETWEEN
                                ; THE DIAGNOSTIC PROGRAM AND THE SUPERVISOR.
                                ;--

002000                                  POINTER BGNSETUP


002000                                  HEADER  CVCDB,8,0,60.,0,PRI07
002000                          L$NAME::                ;DIAGNOSTIC NAME
002000  103                             .ASCII ,C/
002001  126                             .ASCII /V/
002002  103                             .ASCII /C/
002003  104                             .ASCII /D/
002004  102                             .ASCII /B/
002005  000                             .BYTE   0
002006  000                             .BYTE   0
002007  000                             .BYTE   0
002010                          L$REV::                 ;REVISION LEVEL
002010  102                             .ASCII  /B/
002011                          L$DEPO::                ;0
002011  060                             .ASCII  /0/
002012                          L$UNIT::                ;NUMBER OF UNITS
002012  000001                          .WORD   T$PTHV
002014                          L$TIML::                ;LONGEST TEST TIME
002014  000074                          .WORD   60.
002016                          L$HPCP::                ;POINTER TO H.W. QUES.
002016  037602                          .WORD   L$HARD
002020                          L$SPCP::                ;POINTER TO S.W. QUES.
002020  000000                          .WORD   0
002022                          L$HPTP::                ;PTR. TO DEF. H.W. PTABLE
002022  002330                          .WORD   L$HW
002024                          L$SPTP::                ;PTR. TO S.W. PTABLE
002024  000000                          .WORD   0
002026                          L$LADP::                ;DIAG. END ADDRESS
002026  037744                          .WORD   L$LAST
002030                          L$STA::                 ;RESERVED FOR APT STATS
002030  000000                          .WORD   0
002032                          L$CO::
002032  000000                          .WORD   0
002034                          L$DTYP::                ;DIAGNOSTIC TYPE
002034  000000                          .WORD   0
002036                          L$APT::                 ;APT EXPANSION
002036  000000                          .WORD   0
002040                          L$DTP::                 ;PTR. TO DISPATCH TABLE
002040  002124                          .WORD   L$DISPATCH
```

```
1555  002042
1556  002042  000340          L$PRIO::                ;DIAGNOSTIC RUN PRIORITY
                              .WORD   PRI07
1557  002044
1558  002044  000000          L$ENVI::                ;FLAGS DESCRIBE HOW IT WAS SETUP
                              .WORD   0
1559  002046
1560  002046  000000          L$EXP1::                ;EXPANSION WORD
                              .WORD   0
1561  002050
1562  002050     003          L$MREV::                ;SVC REV AND EDIT #
                              .BYTE   C$REVISION
1563  002051     003                                  .BYTE   C$EDIT
1564  002052
1565  002052  000000          L$EF::                  ;DIAG. EVENT FLAGS
                              .WORD   0
1566  002054  000000                                  .WORD   0
1567  002056
1568  002056  000000          L$SPC::
                              .WORD   0
1569  002060
1570  002060  002424          L$DEVP::                ; POINTER TO DEVICE TYPE LIST
                              .WORD   L$DVTYP
1571  002062
1572  002062  000000          L$REPP::                ;PTR. TO REPORT CODE
                              .WORD   0
1573  002064
1574  002064  000000          L$EXP4::
                              .WORD   0
1575  002066
1576  002066  000000          L$EXP5::
                              .WORD   0
1577  002070
1578  002070  000000          L$AUT::                 ;PTR. TO ADD UNIT CODE
                              .WORD   0
1579  002072
1580  002072  000000          L$DUT::                 ;PTR. TO DROP UNIT CODE
                              .WORD   0
1581  002074
1582  002074  000000          L$LUN::                 ;LUN FOR EXERCISERS TO FILL
                              .WORD   0
1583  002076
1584  002076  002436          L$DESP::                ;POINTER TO DIAG. DESCRIPTION
                              .WORD   L$DESC
1585  002100
1586  002100  104035          L$LOAD::                ;GENERATE SPECIAL AUTOLOAD EMT
                              EMT     E$LOAD
1587  002102
1588  002102  000000          L$ETP::                 ;POINTER TO ERRTBL
                              .WORD   0
1589  002104
1590  002104  006736          L$ICP::                 ;PTR. TO INIT CODE
                              .WORD   L$INIT
1591  002106
1592  002106  007124          L$CCP::                 ;PTR. TO CLEAN-UP CODE
                              .WORD   L$CLEAN
1593  002110
1594  002110  007122          L$ACP::                 ;PTR. TO AUTO CODE
                              .WORD   L$AUTO
1595  002112
1596  002112  006730          L$PRT::                 ;PTR. TO PROTECT TABLE
                              .WORD   L$PROT
1597  002114
1598  002114  000000          L$TEST::                ;TEST NUMBER
                              .WORD   0
1599  002116
1600  002116  000000          L$DLY::                 ;DELAY COUNT
                              .WORD   0
1601  002120
1602  002120  000000          L$HIME::                ;PTR. TO HIGH MEM
                              .WORD   0
1603
```

```
                                        .SBTTL  DISPATCH TABLE

                                        ;++
                                        ; THE DISPATCH TABLE CONTAINS THE STARTING ADDRESS OF EACH TEST.
                                        ; IT IS USED BY THE SUPERVISOR TO DISPATCH TO EACH TEST.
                                        ;--

002122                                          DISPATCH 65.
002122  000101                                  .WORD   65
002124                                  L$DISPATCH::
002124  007162                                  .WORD   T1
002126  007170                                  .WORD   T2
002130  007254                                  .WORD   T3
002132  007342                                  .WORD   T4
002134  007404                                  .WORD   T5
002136  007470                                  .WORD   T6
002140  007556                                  .WORD   T7
002142  007620                                  .WORD   T8
002144  007734                                  .WORD   T9
002146  010052                                  .WORD   T10
002150  010156                                  .WORD   T11
002152  010404                                  .WORD   T12
002154  010450                                  .WORD   T13
002156  010516                                  .WORD   T14
002160  010562                                  .WORD   T15
002162  010630                                  .WORD   T16
002164  010674                                  .WORD   T17
002166  010742                                  .WORD   T18
002170  011006                                  .WORD   T19
002172  011054                                  .WORD   T20
002174  011410                                  .WORD   T21
002176  011604                                  .WORD   T22
002200  012000                                  .WORD   T23
002202  012174                                  .WORD   T24
002204  012412                                  .WORD   T25
002206  013244                                  .WORD   T26
002210  014076                                  .WORD   T27
002212  014730                                  .WORD   T28
002214  015650                                  .WORD   T29
002216  016060                                  .WORD   T30
002220  016502                                  .WORD   T31
002222  017002                                  .WORD   T32
002224  017452                                  .WORD   T33
002226  017552                                  .WORD   T34
002230  017636                                  .WORD   T35
002232  020030                                  .WORD   T36
002234  020630                                  .WORD   T37
002236  021002                                  .WORD   T38
002240  021156                                  .WORD   T39
002242  021352                                  .WORD   T40
002244  021540                                  .WORD   T41
002246  021732                                  .WORD   T42
002250  022126                                  .WORD   T43
002252  022322                                  .WORD   T44
002254  022510                                  .WORD   T45
002256  022702                                  .WORD   T46
```

```
1660  002260  023076                    .WORD   T47
1661  002262  023272                    .WORD   T48
1662  002264  023460                    .WORD   T49
1663  002266  023652                    .WORD   T50
1664  002270  024046                    .WORD   T51
1665  002272  024242                    .WORD   T52
1666  002274  024550                    .WORD   T53
1667  002276  025324                    .WORD   T54
1668  002300  026244                    .WORD   T55
1669  002302  027164                    .WORD   T56
1670  002304  027670                    .WORD   T57
1671  002306  030276                    .WORD   T58
1672  002310  030670                    .WORD   T59
1673  002312  031454                    .WORD   T60
1674  002314  032712                    .WORD   T61
1675  002316  034032                    .WORD   T62
1676  002320  035152                    .WORD   T63
1677  002322  036244                    .WORD   T64
1678  002324  037330                    .WORD   T65
1679
```

```
                                .SBTTL  DEFAULT HARDWARE P-TABLE

                                ;++
                                ; THE DEFAULT HARDWARE P-TABLE CONTAINS DEFAULT VALUES OF
                                ; THE TEST-DEVICE PARAMETERS.  THE STRUCTURE OF THIS TABLE
                                ; IS IDENTICAL TO THE STRUCTURE OF THE HARDWARE P-TABLES,
                                ; AND IS USED AS A "TEMPLATE" FOR BUILDING THE P-TABLES.
                                ;--

002326                                  BGNHW   DFPTBL
002326  000003                         .WORD   L10000-L$HW/2
002330                          L$HW::
002330                          DFPTBL::

002330  163010                         .WORD   163010                  ;CSR ADDRESS
002332  000001                         .WORD   1                       ;DEVICE SELECTION NUMBER
002334  000000                         .WORD   0                       ;EXTERNAL PROBE INDICATOR (0 = NO)

002336                                  ENDHW
002336                          L10000:

                                .SBTTL  SOFTWARE P-TABLE

                                ;++
                                ; THE SOFTWARE TABLE CONTAINS VARIOUS DATA USED BY THE
                                ; PROGRAM AS OPERATIONAL PARAMETERS.  THESE PARAMETERS ARE
                                ; SET UP AT ASSEMBLY TIME AND MAY BE VARIED BY THE OPERATOR
                                ; AT RUN TIME.
                                ;--

002336                                  BGNSW   SFPTBL
002336  000000                         .WORD   L10001-L$SW/2
002340                          L$SW::
002340                          SFPTBL::


002340                                  ENDSW
002340                          L10001:

002340                                  ENDMOD
```

```
                                .TITLE GLOBAL AREAS
                                .SBTTL  GLOBAL EQUATES SECTION


002340                                  BGNMOD

                                ;++
                                ; THE GLOBAL EQUATES SECTION CONTAINS PROGRAM EQUATES THAT
                                ; ARE USED IN MORE THAN ONE TEST.
                                ;--


002340                                  EQUALS
                                ;
                                ; BIT DIFINITIONS
                                ;
                                BIT15== 100000
                                BIT14== 40000
                                BIT13== 20000
                                BIT12== 10000
                                BIT11== 4000
                                BIT10== 2000
                                BIT09== 1000
                                BIT08== 400
                                BIT07== 200
                                BIT06== 100
                                BIT05== 40
                                BIT04== 20
                                BIT03== 10
                                BIT02== 4
                                BIT01== 2
                                BIT00== 1
                                ;
                                BIT9==  BIT09
                                BIT8==  BIT08
                                BIT7==  BIT07
                                BIT6==  BIT06
                                BIT5==  BIT05
                                BIT4==  BIT04
                                BIT3==  BIT03
                                BIT2==  BIT02
                                BIT1==  BIT01
                                BIT0==  BIT00
                                ;
                                ; EVENT FLAG DEFINITIONS
                                ;   EF32:EF17 RESERVED FOR SUPERVISOR TO PROGRAM COMMUNICATION
                                ;
                                EF.START==      32.                     ; START COMMAND WAS ISSUED
                                EF.RESTART==    31.                     ; RESTART COMMAND WAS ISSUED
                                EF.CONTINUE==   30.                     ; CONTINUE COMMAND WAS ISSUED
                                EF.NEW==        29.                     ; A NEW PASS HAS BEEN STARTED
                                EF.PWR==        28.                     ; A POWER-FAIL/POWER-UP OCCURRED
                                ;
                                ;
                                ; PRIORITY LEVEL DEFINITIONS
                                ;
```

```
1777            000340                  PRI07== 340
1778            000300                  PRI06== 300
1779            000240                  PRI05== 240
1780            000200                  PRI04== 200
1781            000140                  PRI03== 140
1782            000100                  PRI02== 100
1783            000040                  PRI01== 40
1784            000000                  PRI00== 0
1785                                    ;
1786                                    ;OPERATOR FLAG BITS
1787                                    ;
1788            000004                  EVL==       4
1789            000010                  LOT==      10
1790            000020                  ADR==      20
1791            000040                  IDU==      40
1792            000100                  ISR==     100
1793            000200                  UAM==     200
1794            000400                  BOE==     400
1795            001000                  PNT==    1000
1796            002000                  PRI==    2000
1797            004000                  IXE==    4000
1798            010000                  IBE==   10000
1799            020000                  IER==   20000
1800            040000                  LOE==   40000
1801            100000                  HOE==  100000
1802
1803                                    ;
1804                                    ;CONTROL REGISTER 0 (CDAL BITS 15-0)
1805                                    ;
1806
1807            100000                  CDAL15==BIT15                   ;BIT15=1 READ DEVICE TYPE IN 15-8
1808                                                                    ;ED DEVICE TYPE EQUALS 1000 (BIT9=1)
1809                                                                    ;
1810                                                                    ;BIT15=0 READ DEVICE NUMBER INTO
1811                                                                    ;BITS 11-8
1812
1813            040000                  CDAL14==BIT14                   ;ALWAYS A 0 ON READ
1814            020000                  CDAL13==BIT13                   ;ALWAYS A 0 ON READ
1815            010000                  CDAL12==BIT12                   ;ALWAYS A 0 ON READ
1816
1817            004000                  CDAL11==BIT11                   ;BITS 11-8 ARE USED TO SELECT THE
1818            002000                  CDAL10==BIT10                   ;DEVICE NUMBER TO ASSERT THE SIGNAL
1819            001000                  CDAL9== BIT9                    ;DEVE L. WHEN SELECTING ED THESE BITS
1820            000400                  CDAL8== BIT8                    ;MUST = THE SETTING OF DEV 3 - DEV 0
1821
1822            000200                  CDAL7== BIT7                    ;1 - DISABLE OUTPUTS OF OR ADDRESS REG
1823                                                                    ;    ENABLE FOUT 3:0 TO DRIVE OR ADDRESS
1824                                                                    ;0 - ENABLE OUTPUTS OF OR ADDRESS REG
1825
1826            000100                  CDAL6== BIT6                    ;1/0 - CLOCK SIGNAL ''TRNST H''
1827
1828            000040                  CDAL5== BIT5                    ;1 - STOP TRACING WHEN TRAD10 H SET HIGH
1829                                                                    ;0 - CONTINUOS TRACING
1830
1831            000020                  CDAL4== BIT4                    ;1 - ENABLE ALL AND/OR ARRAY RAMS
1832                                                                    ;0 - ENABLE ONLY ONE AND/OR ARRAY RAMS
```

```
1833
1834            000010                  CDAL3== BIT3                    ;TRACE RAM BUS SELECT
1835            000004                  CDAL2== BIT2                    ;TRACE RAM BUS SELECT
1836
1837            000002                  CDAL1== BIT1                    ;ENABLE FUNCTION SELECTS ONTO SYSTEM BUS
1838
1839            000001                  CDAL0== BIT0                    ;1/0 - ZERO TRAM ADDRESS REG, TRACING
1840                                                                    ;     FLIP-FLOP AND SBL FLIP-FLOPS 59:56.
1841                                                                    ;     LOAD EVNT CNTR'S VIA EVNT CNTR REG.
1842
1843                                    ;
1844                                    ;CONTROL REGISTER 2 (PDAL BITS 7-0)
1845                                    ;
1846
1847                                                                    ;BITS 15-8 ARE UNUSED BITS
1848
1849            000200                  PDAL7== BIT7                    ;1 - CLEAR EVENT COUNTERS
1850            000100                  PDAL6== BIT6                    ;1 - PRESET TRACING FLIP-FLOP
1851            000040                  PDAL5== BIT5                    ;0 - CLEAR FUNCTION SELECT FLIP-FLOPS
1852            000020                  PDAL4== BIT4                    ;1 - EXTERNAL PROBE "CLK" SIGNAL WILL
1853                                                                    ;     LOAD EXTP 7:0 F/F'S WHEN "CLK" SET LOW
1854                                                                    ;0 - EXTERNAL PROBE "CLK" SIGNAL WILL
1855                                                                    ;     LOAD EXTP 7:0 F/F'S WHEN "CLK" SET HIGH
1856            000010                  PDAL3== BIT3                    ;SELECTS POINTER REIGSTER (SEE BELOW)
1857            000004                  PDAL2== BIT2                    ;SELECTS POINTER REGISTER (SEE BELOW)
1858            000002                  PDAL1== BIT1                    ;SELECTS POINTER REGISTER (SEE BELOW)
1859            000001                  PDAL0== BIT0                    ;SELECTS POINTER REGISTER (SEE BELOW)
1860
1861                                    ;
1862                                    ;POINTER REGISTER PTER 15-0 (SELECTED BY PDAL 3-0)
1863                                    ;
1864
1865            000000                  PTER0== 0                       ;WPT0,RPT0,R/W TRAM AUDRESS (9-0)
1866            000001                  PTER1== PDAL0                   ;WPT1,RPT1,R/W TRAM DATA LSI-11 TO TRDI (15-0)
1867            000002                  PTER2== PDAL1                   ;WPT2,RPT2,R/W TRAM DATA LSI-11 TO TRDI (31-16)
1868            000003                  PTER3== PDAL1!PDAL0             ;WPT3,RPT3,R/W TRAM DATA LSI-11 TO TRDI (47-32)
1869            000004                  PTER4== PDAL2                   ;WPT4,RPT4,R/W TRAM DATA LSI-11 TO TRDI (59-48)
1870            000005                  PTER5== PDAL2!PDAL0             ;WPT5,WRITE TRACE RAM DATA IN BUF (15-0)
1871            000006                  PTER6== PDAL2!PDAL1             ;WPT6,WRITE TRACE RAM DATA IN BUF (31-16)
1872            000007                  PTER7== PDAL2!PDAL1!PDAL0       ;WPT7,WRITE TRACE RAM DATA IN BUF (47-32)
1873            000010                  PTER8== PDAL3                   ;WPT8,WRITE TRACE RAM DATA IN BUF (59-48)
1874            000011                  PTER9== PDAL3!PDAL0             ;WPT9,LOAD EVENT COUNTER 0
1875            000012                  PTER10==PDAL3!PDAL1             ;WPT10,LOAD EVENT COUNTER 1
1876            000013                  PTER11==PDAL3!PDAL1!PDAL0       ;WPT11,LOAD EVENT COUNTER 2
1877            000014                  PTER12==PDAL3!PDAL2             ;WPT12,LOAD EVENT COUNTER 3
1878            000015                  PTER13==PDAL3!PDAL2!PDAL0       ;NOT USED
1879            000016                  PTER14==PDAL3!PDAL2!PDAL1       ;NOT USED
1880            000017                  PTER15==PDAL3!PDAL2!PDAL1!PDAL0 ;WPT15,RPT15,R/W "OR" ADDRESS
1881
1882
```

```
                                .SBTTL  GLOBAL DATA SECTION

                                ;++
                                ; THE GLOBAL DATA SECTION CONTAINS DATA THAT ARE USED
                                ; IN MORE THAN ONE TEST.
                                ;--


                                        ERRTBL
002340                          L$ERRTBL::
002340  000000                  ERRTYP::        .WORD   0
002342  000000                  ERRNBR::        .WORD   0
002344  000000                  ERRMSG::        .WORD   0
002346  000000                  ERRBLK::        .WORD   0

                                ;
                                ;GLOBAL DATA FOR STATE ANALYZER
                                ;
002350  163010                  REG0::  .WORD   163010          ;CONTROL REGISTER 0
002352  163012                  REG2::  .WORD   163012          ;CONTROL REGISTER 2
002354  163014                  REG4::  .WORD   163014          ;CONTROL REGISTER 4
002356  163016                  REG6::  .WORD   163016          ;CONTROL REGISTER 6

002360  000000                  IDDEV:: .WORD   0               ;STATE ANALYZER DEVICE # (11-8)
002362  000000                  UNITNB::.WORD   0               ;
002364  000000                  IDTYPE::.WORD   0               ;STATE ANALYZER DEVICE TYPE (15-8)
002366  000000                  EXTPRB::.WORD   0               ;EXTERNAL PROBE INDICATOR (0 = NO PROBE)

002370  000000                  R0LOAD::.WORD   0               .WORD LOADED INTO REGISTER 0
002372  000000                  R0GOOD::.WORD   0               ;EXPECTED REG 0
002374  000000                  R0READ::.WORD   0               ;ACTUAL REG 0 READ

002376  000000                  R2LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 2
002400  000000                  R2READ::.WORD   0               ;ACTUAL REG 2 READ

002402  000000                  R4LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 4
002404  000000                  R4GOOD::.WORD   0               ;EXPECTED DATA FROM REGISTER 4
002406  000000                  R4MASK::.WORD   0               ;BITS TO BE IGNORED ON COMPARE
002410  000000                  R4READ::.WORD   0               ;WORD READ OUT OF REGISTER 4
002412  000000                  R4BAD:: .WORD   0               ;DATA READ MASKED WITH R4MASK

002414  000000                  R6LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 6
002416  000000                  R6MASK::.WORD   0               ;REGSITER 6 MASK WORD
002420  000000                  R6READ::.WORD   0               ;ACTUAL REGISTER 6 READ
002422  000000                  R6BAD:: .WORD   0               ;REG 6 READ MINUS MASK WORD
```

```
                                        .SBTTL  GLOBAL TEXT SECTION

                                        ;++
                                        ; THE GLOBAL TEXT SECTION CONTAINS FORMAT STATEMENTS,
                                        ; MESSAGES, AND ASCII INFORMATION THAT ARE USED IN
                                        ; MORE THAN ONE TEST.
                                        ;--

                                        ;
                                        ; NAMES OF DEVICES SUPPORTED BY PROGRAM
                                        ;
002424                                          DEVTYP  <MDE/T-11>
002424                                  L$DVTYP::
002424  042115  027505  026524                  .ASCIZ  %MDE/T-11%
002432  030461     000
        002436                                  .EVEN


                                        ; TEST DESCRIPTION
                                        ;
002436                                          DESCRIPT        <STATE ANALYZER DIAG.>
002436                                  L$DESC::
002436  052123  052101  020105                  .ASCIZ  /STATE ANALYZER DIAG./
002444  047101  046101  055131
002452  051105  042040  040511
002460  027107     000
        002464                                  .EVEN


                                        ;
                                        ;ASCII MESSAGES USED BY ERROR CALLS - CONTROL REGISTER 6
                                        ;
002464  051124  046501  040440  TRADER::.ASCIZ  /TRAM ADDRESS REG - TRAD 10:0/
002472  042104  042522  051523
002500  051040  043505  026440
002506  052040  040522  020104
002514  030061  030072     000
002521     124  040522  020115  TRDI15::.ASCIZ  /TRAM DATA IN BUF - TRDI 15:0/
002526  040504  040524  044440
002534  020116  052502  020106
002542  020055  051124  044504
002550  030440  035065  000060
002556  051124  046501  042040  TRDI31::.ASCIZ  /TRAM DATA IN BUF - TRDI 31:16/
002564  052101  020101  047111
002572  041040  043125  026440
002600  052040  042122  020111
002606  030463  030472  000066
002614  051124  046501  042040  TRDI47::.ASCIZ  /TRAM DATA IN BUF - TRDI 47:32/
002622  052101  020101  047111
002630  041040  043125  026440
002636  052040  042122  020111
002644  033464  031472  000062
002652  051124  046501  042040  TRDI59::.ASCIZ  /TRAM DATA IN BUF - TRDI 59:48/
002660  052101  020101  047111
002666  041040  043125  026440
```

```
1985  002674  052040  042122  020111
1986  002702  034465  032072  000070
1987  002710  051124  046501  042040  TRDIER::.ASCIZ  /TRAM DATA IN BUF - TRDI 59:0/
1988  002716  052101  020101  047111
1989  002724  041040  043125  026440
1990  002732  052040  042122  020111
1991  002740  034465  030072     000
1992  002745     124  040522  020115  TRDISE::.ASCIZ  /TRAM DATA IN BUF SELECTION/
1993  002752  040504  040524  044440
1994  002760  020116  052502  020106
1995  002766  042523  042514  052103
1996  002774  047511  000116
1997  003000  051124  046501  042040  TRAM15::.ASCIZ  /TRAM DATA ERROR - TRDI 15:0/
1998  003006  052101  020101  051105
1999  003014  047522  020122  020055
2000  003022  051124  044504  030440
2001  003030  035065  000060
2002  003034  051124  046501  042040  TRAM31::.ASCIZ  /TRAM DATA ERROR - TRDI 31:16/
2003  003042  052101  020101  051105
2004  003050  047522  020122  020055
2005  003056  051124  044504  031440
2006  003064  035061  033061     000
2007  003071     124  040522  020115  TRAM47::.ASCIZ  /TRAM DATA ERROR - TRDI 47:32/
2008  003076  040504  040524  042440
2009  003104  051122  051117  026440
2010  003112  052040  042122  020111
2011  003120  033464  031472  000062
2012  003126  051124  046501  042040  TRAM55::.ASCIZ  /TRAM DATA ERROR - TRDI 55:48/
2013  003134  052101  020101  051105
2014  003142  047522  020122  020055
2015  003150  051124  044504  032440
2016  003156  035065  034064     000
2017  003163     117  020122  042101  ORADER::.ASCIZ  /OR ADDRESS REG - ORAD 3:0/
2018  003170  051104  051505  020123
2019  003176  042522  020107  020055
2020  003204  051117  042101  031440
2021  003212  030072     000
2022  003215     105  042526  052116  EVNTCT::.ASCIZ  /EVENT COUNTERS OR FOUT 3:0 ERROR/
2023  003222  041440  052517  052116
2024  003230  051105  020123  051117
2025  003236  043040  052517  020124
2026  003244  035063  020060  051105
2027  003252  047522  000122
2028  003256  042120  046101  020067  EVNTCL::.ASCIZ  /PDAL7 FAILED TO CLEAR EVENT COUNTERS/
2029  003264  040506  046111  042105
2030  003272  052040  020117  046103
2031  003300  040505  020122  053105
2032  003306  047105  020124  047503
2033  003314  047125  042524  051522
2034  003322     000
2035  003323     103  040504  030114  EVNTRL::.ASCIZ  /CDAL0 FAILED TO LOAD EVENT COUNTERS/
2036  003330  043040  044501  042514
2037  003336  020104  047524  046040
2038  003344  040517  020104  053105
2039  003352  047105  020124  047503
2040  003360  047125  042524  051522
```

```
2041  003366     000
2042  003367     106  051525  020114  FUSL30::.ASCIZ  /FUSL 3:0 FLIP-FLOP ERROR/
2043  003374  035063  020060  046106
2044  003402  050111  043055  047514
2045  003410  020120  051105  047522
2046  003416  000122
2047  003420  041123  020114  034465  SBLERR::.ASCIZ  /SBL 59:56 FLIP-FLOP ERROR/
2048  003426  032472  020066  046106
2049  003434  050111  043055  047514
2050  003442  020120  051105  047522
2051  003450  000122
2052  003452  054105  050124  033440  EXTPER::.ASCIZ  /EXTP 7:0 FLIP-FLOP OR LOGIC ERROR/
2053  003460  030072  043040  044514
2054  003466  026520  046106  050117
2055  003474  047440  020122  047514
2056  003502  044507  020103  051105
2057  003510  047522  000122
2058
2059                                  ;
2060                                  ;ASCII MESSAGES USED BY ERROR CALLS - CONTROL REGISTER 4
2061                                  ;
2062
2063  003514  051117  040440  051122  ORDATA::.ASCIZ  /OR ARRAY DATA ERROR - ORO 7:0/
2064  003522  054501  042040  052101
2065  003530  020101  051105  047522
2066  003536  020122  020055  051117
2067  003544  020117  035067  000060
2068  003552  047101  020104  051101  ANDERR::.ASCIZ  /AND ARRAY RAM DATA ERROR/
2069  003560  040522  020131  040522
2070  003566  020115  040504  040524
2071  003574  042440  051122  051117
2072  003602     000
2073  003603     106  051525  033514  FUSL7:: .ASCIZ  /FUSL7 FLIP-FLOP - OR ARRAY DATA ERROR/
2074  003610  043040  044514  026520
2075  003616  046106  050117  026440
2076  003624  047440  020122  051101
2077  003632  040522  020131  040504
2078  003640  040524  042440  051122
2079  003646  051117     000
2080  003651     101  042116  026440  ANDOR::.ASCIZ   /AND - OR ARRAY DATA ERROR/
2081  003656  047440  020122  051101
2082  003664  040522  020131  040504
2083  003672  040524  042440  051122
2084  003700  051117     000
2085
2086        003704                          .EVEN
2087
2088
2089                                  ;
2090                                  ; FORMAT STATEMENTS USED IN PRINT CALLS
2091                                  ;
2092
2093  003704  040445  047503  052116  EMSGR0::.ASCIZ  /%ACONTROL REG 0 ERROR%N/
2094  003712  047522  020114  042522
2095  003720  020107  020060  051105
2096  003726  047522  022522  000116
```

```
 2097  003734  040445  047503  052116  EMSGR2::.ASCIZ  /%ACONTROL REG 2 ERROR%N/
 2098  003742  047522  020114  042522
 2099  003750  020107  020062  051105
 2100  003756  047522  022522  000116
 2101  003764  040445  047503  052116  EMSGR4::.ASCIZ  /%ACONTROL REG 4 ERROR%N/
 2102  003772  047522  020114  042522
 2103  004000  020107  020064  051105
 2104  004006  047522  022522  000116
 2105  004014  040445  047503  052116  EMSGR6::.ASCIZ  /%ACONTROL REG 6 ERROR%N/
 2106  004022  047522  020114  042522
 2107  004030  020107  020066  051105
 2108  004036  047522  022522  000116
 2109  004044  040445  042522  030107  REG0EQ::.ASCIZ  /%AREG0 = /
 2110  004052  036440  000040
 2111  004056  040445  042522  031107  REG2EQ::.ASCIZ  /%AREG2 = /
 2112  004064  036440  000040
 2113  004070  040445  042522  032107  REG4EQ::.ASCIZ  /%AREG4 = /
 2114  004076  036440  000040
 2115  004102  040445  042522  033107  REG6EQ::.ASCIZ  /%AREG6 = /
 2116  004110  036440  000040
 2117  004114  040445  051124  046501  MSGTRM::.ASCIZ  /%ATRAM ADDRESS REG = %O6%N/
 2118  004122  040440  042104  042522
 2119  004130  051523  051040  043505
 2120  004136  036440  022440  033117
 2121  004144  047045     000
 2122  004147     045  046101  040517  FRMTOR::.ASCIZ  /%ALOAD: %O6%S1%AREAD: %O6%S1%AGOOD: %O6%N/
 2123  004154  035104  022440  033117
 2124  004162  051445  022461  051101
 2125  004170  040505  035104  022440
 2126  004176  033117  051445  022461
 2127  004204  043501  047517  035104
 2128  004212  022440  033117  047045
 2129  004220     000
 2130  004221     045  046101  040517  FRMTRO::.ASCIZ  /%ALOAD: %O6%S1%AREAD: %O6%N/
 2131  004226  035104  022440  033117
 2132  004234  051445  022461  051101
 2133  004242  040505  035104  022440
 2134  004250  033117  047045     000
 2135
 2136  004255     045  046101  040517  FRMTR4::.ASCIZ  /%ALOAD: %O6%S1%AREAD: %O6%S1%AMASK: %O6%S1%AGOOD: %O6%S1%ABAD: %O6%N/
 2137  004262  035104  022440  033117
 2138  004270  051445  022461  051101
 2139  004276  040505  035104  022440
 2140  004304  033117  051445  022461
 2141  004312  046501  051501  035113
 2142  004320  022440  033117  051445
 2143  004326  022461  043501  047517
 2144  004334  035104  022440  033117
 2145  004342  051445  022461  041101
 2146  004350  042101  020072  047445
 2147  004356  022466  000116
 2148  004362  040445  053105  052116  FRMTEC::.ASCIZ  /%AEVNT CNT LOADED: %O6%S1%AEVNT CNT BEFORE CNT DOWN: %O6%N/
 2149  004370  041440  052116  046040
 2150  004376  040517  042504  035104
 2151  004404  022440  033117  051445
 2152  004412  022461  042501  047126
```

```
2153  004420  020124  047103  020124
2154  004426  042502  047506  042522
2155  004434  041440  052116  042040
2156  004442  053517  035116  022440
2157  004450  033117  047045     000
2158  004455     045  052101  046511  MSGTM0::.ASCIZ  /%ATIME OUT ERROR ADDRESSING CONTROL REG 0%N/
2159  004462  020105  052517  020124
2160  004470  051105  047522  020122
2161  004476  042101  051104  051505
2162  004504  044523  043516  041440
2163  004512  047117  051124  046117
2164  004520  051040  043505  030040
2165  004526  047045     000
2166  004531     045  052101  046511  MSGTM2::.ASCIZ  /%ATIME OUT ERROR ADDRESSING CONTROL REG 2%N/
2167  004536  020105  052517  020124
2168  004544  051105  047522  020122
2169  004552  042101  051104  051505
2170  004560  044523  043516  041440
2171  004566  047117  051124  046117
2172  004574  051040  043505  031040
2173  004602  047045     000
2174
2175
2176          004606                  .EVEN
2177
2178
2179
```

```
                        .SBTTL  GLOBAL ERROR REPORT SECTION

                        ;++
                        ; THE GLOBAL ERROR REPORT SECTION CONTAINS MESSAGE PRINTING AREAS
                        ; USED BY MORE THAN TEST TO OUTPUT ADDITIONAL ERROR INFORMATION.  PRINTB
                        ; (BASIC) AND PRINTX (EXTENDED) CALLS ARE USED TO CALL PRINT SERVICES.
                        ;--


004606                          BGNMSG  ROEROR
004606                  ROEROR::
004606  004537  005132          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
004612  003704                  .WORD   EMSGR0
004614  004737  005212          JSR     PC,PRNTR0               ;GO PRINT CONTROL REGISTER 0 INFO


004620                          ENDMSG
004620                  L10002:
004620  104423                  TRAP    C$MSG

004622                          BGNMSG  ERORR0
004622                  ERORR0::
004622  004537  005132          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
004626  003704                  .WORD   EMSGR0
004630                          PRINTX  #REGOEQ
004630  012746  004044          MOV     #REGOEQ,-(SP)
004634  012746  000001          MOV     #1,-(SP)
004640  010600                  MOV     SP,R0
004642  104415                  TRAP    C$PNTX
004644  062706  000004          ADD     #4,SP
004650                          PRINTX  #FRMTOR,ROLOAD,ROREAD,ROGOOD
004650  013746  002372          MOV     ROGOOD,-(SP)
004654  013746  002374          MOV     ROREAD,-(SP)
004660  013746  002370          MOV     ROLOAD,-(SP)
004664  012746  004147          MOV     #FRMTOR,-(SP)
004670  012746  000004          MOV     #4,-(SP)
004674  010600                  MOV     SP,R0
004676  104415                  TRAP    C$PNTX
004700  062706  000012          ADD     #12,SP
004704                          ENDMSG
004704                  L10003:
004704  104423                  TRAP    C$MSG

004706                          BGNMSG  R2EROR
004706                  R2EROR::
004706  004537  005132          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
004712  003734                  .WORD   EMSGR2
004714  004737  005264          JSR     PC,PRNTR2               ;GO PRINT CONTROL REGISTER 2 INFO
004720                          ENDMSG
004720                  L10004:
004720  104423                  TRAP    C$MSG

004722                          BGNMSG  R4EROR
```

```
2236  004722                        R4EROR::
2237  004722  004537  005132                JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2238  004726  003764                        .WORD   EMSGR4
2239  004730  004737  005152                JSR     PC,PRNTAL               ;GO PRINT ALL REGISTERS
2240  004734                                ENDMSG
2241  004734                        L10005:
2242  004734  104423                        TRAP    C$MSG
2243
2244  004736                                BGNMSG  R026ER
2245  004736                        R026ER::
2246  004736  004537  005132                JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2247  004742  004014                        .WORD   EMSGR6
2248  004744  004737  005174                JSR     PC,PR026R
2249  004750                                ENDMSG
2250  004750                        L10006:
2251  004750  104423                        TRAP    C$MSG
2252
2253  004752                                BGNMSG  ALLREG
2254  004752                        ALLREG::
2255  004752  004537  005132                JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2256  004756  004014                        .WORD   EMSGR6
2257  004760  004737  005152                JSR     PC,PRNTAL
2258  004764                                ENDMSG
2259  004764                        L10007:
2260  004764  104423                        TRAP    C$MSG
2261
2262  004766                                BGNMSG  TRAMER
2263  004766                        TRAMER::
2264  004766  004537  005132                JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2265  004772  004014                        .WORD   EMSGR6
2266  004774                                PRINTB  #MSGTRM,TRADRS
2267  004774  013746  006376                MOV     TRADRS,-(SP)
2268  005000  012746  004114                MOV     #MSGTRM,-(SP)
2269  005004  012746  000002                MOV     #2,-(SP)
2270  005010  010600                        MOV     SP,R0
2271  005012  104414                        TRAP    C$PNTB
2272  005014  062706  000006                ADD     #6,SP
2273  005020  004737  005174                JSR     PC,PR026R
2274  005024                                ENDMSG
2275  005024                        L10010:
2276  005024  104423                        TRAP    C$MSG
2277
2278  005026                                BGNMSG  EVNTER
2279  005026                        EVNTER::
2280  005026  004537  005132                JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2281  005032  004014                        .WORD   EMSGR6
2282  005034                                PRINTX  #FRMTEC,R1,R2
2283  005034  010246                        MOV     R2,-(SP)
2284  005036  010146                        MOV     R1,-(SP)
2285  005040  012746  004362                MOV     #FRMTEC,-(SP)
2286  005044  012746  000003                MOV     #3,-(SP)
2287  005050  010600                        MOV     SP,R0
2288  005052  104415                        TRAP    C$PNTX
2289  005054  062706  000010                ADD     #10,SP
2290  005060  004737  005152                JSR     PC,PRNTAL
2291  005064                                ENDMSG
```

```
2292  005064                          L10011:
2293  005064  104423                          TRAP    C$MSG
2294  005066                                  BGNMSG  ROTM
2295  005066                          ROTM::
2296  005066                                  PRINTB  #MSGTM0
2297  005066  012746  004455                  MOV     #MSGTM0,-(SP)
2298  005072  012746  000001                  MOV     #1,-(SP)
2299  005076  010600                          MOV     SP,R0
2300  005100  104414                          TRAP    C$PNTB
2301  005102  062706  000004                  ADD     #4,SP
2302  005106                                  ENDMSG
2303  005106                          L10012:
2304  005106  104423                          TRAP    C$MSG
2305
2306  005110                                  BGNMSG  R2TM
2307  005110                          R2TM::
2308  005110                                  PRINTB  #MSGTM0
2309  005110  012746  004455                  MOV     #MSGTM0,-(SP)
2310  005114  012746  000001                  MOV     #1,-(SP)
2311  005120  010600                          MOV     SP,R0
2312  005122  104414                          TRAP    C$PNTB
2313  005124  062706  000004                  ADD     #4,SP
2314  005130                                  ENDMSG
2315  005130                          L10013:
2316  005130  104423                          TRAP    C$MSG
2317
2318                                  ;ROUTINE TO PRINT WHAT CONTROL REGISTER DETECTED THE ERROR.
2319
2320  005132                          PRNTBS::PRINTB  (R5)+
2321  005132  012546                          MOV     (R5)+,-(SP)
2322  005134  012746  000001                  MOV     #1,-(SP)
2323  005140  010600                          MOV     SP,R0
2324  005142  104414                          TRAP    C$PNTB
2325  005144  062706  000004                  ADD     #4,SP
2326  005150  000205                          RTS     R5
2327
2328
2329                                  ;ROUTINE TO PRINT ALL CONTROL REGISTER ERROR INFORMATION
2330
2331  005152  004737  005212          PRNTAL::JSR     PC,PRNTR0               ;GO PRINT CONTROL REGISTER 0 INFO
2332  005156  004737  005264                  JSR     PC,PRNTR2               ;GO PRINT CONTROL REGISTER 2 INFO
2333  005162  004737  005336                  JSR     PC,PRNTR4               ;GO PRINT CONTROL REGISTER 4 INFO
2334  005166  004737  005424                  JSR     PC,PRNTR6               ;GO PRINT CONTROL REGISTER 6 INFO
2335  005172  000207                          RTS     PC
2336
2337                                  ;ROUTINE TO PRINT CONTROL REGISTER 0, 2 AND 6 ERROR INFORMATION
2338
2339  005174  004737  005212          PR026R::JSR     PC,PRNTR0               ;GO PRINT CONTROL REGISTER 0 INFO
2340  005200  004737  005264                  JSR     PC,PRNTR2               ;GO PRINT CONTROL REGISTER 2 INFO
2341  005204  004737  005424                  JSR     PC,PRNTR6               ;GO PRINT CONTROL REGISTER 6 INFO
2342  005210  000207                          RTS     PC
2343
2344                                  ;PRINT CONTROL REGISTER 0 ERROR INFORMATION
2345
2346  005212                          PRNTR0::PRINTX  #REG0EQ
2347  005212  012746  004044                  MOV     #REG0EQ,-(SP)
```

```
2348  005216  012746  000001          MOV     #1,-(SP)
2349  005222  010600                  MOV     SP,R0
2350  005224  104415                  TRAP    C$PNTX
2351  005226  062706  000004          ADD     #4,SP
2352  005232                          PRINTX  #FRMTR0,R0LOAD,R0READ
2353  005232  013746  002374          MOV     R0READ,-(SP)
2354  005236  013746  002370          MOV     R0LOAD,-(SP)
2355  005242  012746  004221          MOV     #FRMTR0,-(SP)
2356  005246  012746  000003          MOV     #3,-(SP)
2357  005252  010600                  MOV     SP,R0
2358  005254  104415                  TRAP    C$PNTX
2359  005256  062706  000010          ADD     #10,SP
2360  005262  000207                  RTS     PC
2361
2362                          ;PRINT CONTROL REGISTER 2 ERROR INFORMATION
2363
2364  005264                  PRNTR2::PRINTX  #REG2EQ
2365  005264  012746  004056          MOV     #REG2EQ,-(SP)
2366  005270  012746  000001          MOV     #1,-(SP)
2367  005274  010600                  MOV     SP,R0
2368  005276  104415                  TRAP    C$PNTX
2369  005300  062706  000004          ADD     #4,SP
2370  005304                          PRINTX  #FRMTR0,R2LOAD,R2READ
2371  005304  013746  002400          MOV     R2READ,-(SP)
2372  005310  013746  002376          MOV     R2LOAD,-(SP)
2373  005314  012746  004221          MOV     #FRMTR0,-(SP)
2374  005320  012746  000003          MOV     #3,-(SP)
2375  005324  010600                  MOV     SP,R0
2376  005326  104415                  TRAP    C$PNTX
2377  005330  062706  000010          ADD     #10,SP
2378  005334  000207                  RTS     PC
2379
2380                          ;PRINT CONTROL REGISTER 4 ERROR INFORMATION
2381
2382  005336                  PRNTR4::PRINTX  #REG4EQ
2383  005336  012746  004070          MOV     #REG4EQ,-(SP)
2384  005342  012746  000001          MOV     #1,-(SP)
2385  005346  010600                  MOV     SP,R0
2386  005350  104415                  TRAP    C$PNTX
2387  005352  062706  000004          ADD     #4,SP
2388  005356                          PRINTX  #FRMTR4,R4LOAD,R4READ,R4MASK,R4GOOD,R4BAD
2389  005356  013746  002412          MOV     R4BAD,-(SP)
2390  005362  013746  002404          MOV     R4GOOD,-(SP)
2391  005366  013746  002406          MOV     R4MASK,-(SP)
2392  005372  013746  002410          MOV     R4READ,-(SP)
2393  005376  013746  002402          MOV     R4LOAD,-(SP)
2394  005402  012746  004255          MOV     #FRMTR4,-(SP)
2395  005406  012746  000006          MOV     #6,-(SP)
2396  005412  010600                  MOV     SP,R0
2397  005414  104415                  TRAP    C$PNTX
2398  005416  062706  000016          ADD     #16,SP
2399  005422  000207                  RTS     PC
2400
```

```
2401
2402                                    ;PRINT CONTROL REGISTER 6 ERROR INFORMATION
2403
2404  005424                            PRNTR6::PRINTX  #REG6EQ
2405  005424  012746  004102                    MOV     #REG6EQ,-(SP)
2406  005430  012746  000001                    MOV     #1,-(SP)
2407  005434  010600                            MOV     SP,R0
2408  005436  104415                            TRAP    C$PNTX
2409  005440  062706  000004                    ADD     #4,SP
2410  005444                                    PRINTX  #FRMTR0,R6LOAD,R6READ
2411  005444  013746  002420                    MOV     R6READ,-(SP)
2412  005450  013746  002414                    MOV     R6LOAD,-(SP)
2413  005454  012746  004221                    MOV     #FRMTR0,-(SP)
2414  005460  012746  000003                    MOV     #3,-(SP)
2415  005464  010600                            MOV     SP,R0
2416  005466  104415                            TRAP    C$PNTX
2417  005470  062706  000010                    ADD     #10,SP
2418  005474  000207                            RTS     PC
2419
```

```
                        .SBTTL  GLOBAL SUBROUTINES SECTION

                        ;++
                        ; THE GLOBAL SUBROUTINES SECTION CONTAINS THE SUBROUTINES
                        ; THAT ARE USED IN MORE THAN ONE TEST.
                        ;--

                        ;++
                        ; FUNCTIONAL DESCRIPTION:
                        ;    SUBROUTINE TO....SELECT AND INITIALIZE STATE ANALYZER


                        ; INPUTS:
                        ;    LOCATION IDDEV CONTAINS USER DEFINED DEVICE NUMBER IN BITS 11-8


                        ; IMPLICIT INPUTS:


                        ; OUTPUTS:
                        ;    ROLOAD CONTAINS USER DEFINED UNIT NUMBER IN BITS 11-8
                        ;    ROMASK CONTAINS CONTROL REGISTER 0 MASK WORD (000200)
                        ;    R2LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 2 WAS CLEARED


                        ; IMPLICIT OUTPUTS:


                        ; SUBORDINATE ROUTINES USED:
                        ;    LDRDR0 ROUTINE TO LOAD, READ AND COMPARE REGISTER 0
                        ;    LDRDOR ROUTINE TO LOAD, READ AND COMPARE REGISTER 0 (USED FOR DEVICE TYPE)
                        ;    LDRDR2 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 2


                        ; FUNCTIONAL SIDE EFFECTS:
                        ;    STATE ANALYZER SELECTED
                        ;    CONTROL REGISTER 0 LOW BYTE EQUALS 0
                        ;    CONTROL REGISTER 2 EQUALS 0


                        ; CALLING SEQUENCE:
                        ;    JSR PC,INITED

                        ;--



005476                  INITED::BGNSEG                          ;ROUTINE TO INIT ED MODULE
005476  104404                  TRAP    C$BSEG
005500                          SETVEC  #4,#1$,#PRI07           ;SETUP VECTOR
005500  012746  000340          MOV     #PRI07,-(SP)
005504  012746  005602          MOV     #1$,-(SP)
005510  012746  000004          MOV     #4,-(SP)
005514  012746  000003          MOV     #3,-(SP)
005520  104437                  TRAP    C$SVEC
```

```
2476  005522  062706  000010                    ADD     #10,SP
2477
2478                                            ;LOAD DEVICE NUMBER INTO REGISTER 0 AND CHECK IT
2479
2480  005526  013737  002360  002370            MOV     IDDEV,ROLOAD            ;GET USER DEFINED DEVICE NUMBER
2481  005534  013737  002370  002372            MOV     ROLOAD,ROGOOD           ;PUT DATA LOADED INTO  EXPECTED
2482  005542  013777  002370  174600            MOV     ROLOAD,@REG0            ;WRITE WORD TO REGISTER 0
2483  005550  017737  174574  002374            MOV     @REG0,ROREAD            ;READ REGISTER CONTENTS BACK
2484  005556  023737  002372  002374            CMP     ROGOOD,ROREAD           ;COMPARE EXPECTED WITH THAT READ
2485  005564  001414                            BEQ     2$                      ;IF COMPARE WAS GOOD THEN CONT
2486  005566                                    ERRDF   1,,ROEROR               ;REG 0 NOT EQUAL EXPECTED
2487  005566  104455                            TRAP    C$ERDF
2488  005570  000001                            .WORD   1
2489  005572  000000                            .WORD   0
2490  005574  004606                            .WORD   ROEROR
2491  005576                                    CKLOOP
2492  005576  104406                            TRAP    C$CLP1
2493  005600  000406                            BR      2$                      ;BRANCH AROUND TIME OUT ERROR
2494  005602  005726                    1$:     TST     (SP)+                   ;CLEAN UP STACK
2495  005604  005726                            TST     (SP)+                   ;CLEAN UP STACK
2496  005606                                    ERRDF   1,,ROTM                 ;TIME OUT ERROR REG 0
2497  005606  104455                            TRAP    C$ERDF
2498  005610  000001                            .WORD   1
2499  005612  000000                            .WORD   0
2500  005614  005066                            .WORD   ROTM
2501  005616                            2$:     CLRVEC  #4                      ;CLEAR VECTOR
2502  005616  012700  000004                    MOV     #4,R0
2503  005622  104436                            TRAP    C$CVEC
2504  005624                                    ENDSEG
2505  005624                            10000$:
2506  005624  104405                            TRAP    C$ESEG
2507
2508                                            ;READ DEVICE TYPE IN REGISTER 0
2509
2510  005626                                    BGNSEG
2511  005626  104404                            TRAP    C$BSEG
2512  005630  052737  100000  002370            BIS     #CDAL15,ROLOAD          ;SETUP TO READ DEVICE TYPE
2513  005636  013737  002364  002372            MOV     IDTYPE,ROGOOD           ;SETUP EXPECTED DATA
2514  005644  004737  006112                    JSR     PC,LDRDOR               ;LOAD, READ AND COMPARE REG 0
2515  005650  001404                            BEQ     3$                      ;IF EQUAL THEN DEVICE TYPE COMPARED
2516  005652                                    ERRDF   1,,ERORR0               ;DEVICE TYPE NOT EQUAL EXPECTED
2517  005652  104455                            TRAP    C$ERDF
2518  005654  000001                            .WORD   1
2519  005656  000000                            .WORD   0
2520  005660  004622                            .WORD   ERORR0
2521  005662                            3$:     ENDSEG
2522  005662                            10001$:
2523  005662  104405                            TRAP    C$ESEG
2524
2525                                            ;RESET THE SIGNAL CDAL15 TO 0 TO READ DEVICE NUMBER AGAIN AND SET AND
2526                                            ;CLEAR THE SIGNAL CDAL0 TO CLEAR THE TRACE RAM ADDRESS REGISTER, TO
2527                                            ;CLEAR THE TRACING FLIP-FLOP, TO RELOAD THE EVENT COUNTERS AND TO CLEAR
2528                                            ;SBL FLIP FLOPS 59:56.
2529
2530  005664                                    BGNSEG
2531  005664  104404                            TRAP    C$BSEG
```

```
2532  005666  013737  002360  002370          MOV     IDDEV,ROLOAD            ;GET USER DEFINED DEVICE NUMBER
2533  005674  052737  000001  002370          BIS     #CDALO,ROLOAD           ;SETUP TO SET THE CLEAR SIGNAL
2534  005702  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REG 0
2535  005706  001405                          BEQ     4$                      ;IF OK THEN CONTINUE
2536  005710                                  ERRDF   1,,ROEROR               ;REG 0 NOT EQUAL DEVICE #
2537  005710  104455                          TRAP    C$ERDF
2538  005712  000001                          .WORD   1
2539  005714  000000                          .WORD   0
2540  005716  004606                          .WORD   ROEROR
2541  005720                                  CKLOOP
2542  005720  104406                          TRAP    C$CLP1
2543  005722  042737  000001  002370  4$:     BIC     #CDALO,ROLOAD           ;SETUP TO CLEAR THE SIGNAL CDALO
2544  005730  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
2545  005734  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
2546  005736                                  ERRDF   1,,ROLOAD               ;REG 0 NOT EQUAL DEVICE NUMBER
2547  005736  104455                          TRAP    C$ERDF
2548  005740  000001                          .WORD   1
2549  005742  000000                          .WORD   0
2550  005744  002370                          .WORD   ROLOAD
2551  005746                          5$:     ENDSEG
2552  005746                          10002$:
2553  005746  104405                          TRAP    C$ESEG
2554
2555                                          ;CLEAR AND CHECK CONTROL REGISTER 2
2556
2557  005750                                  BGNSEG
2558  005750  104404                          TRAP    C$BSEG
2559  005752                                  SETVEC  #4,#6$,#PRI07           ;SETUP VECTOR
2560  005752  012746  000340                  MOV     #PRI07,-(SP)
2561  005756  012746  006052                  MOV     #6$,-(SP)
2562  005762  012746  000004                  MOV     #4,-(SP)
2563  005766  012746  000003                  MOV     #3,-(SP)
2564  005772  104437                          TRAP    C$SVEC
2565  005774  062706  000010                  ADD     #10,SP
2566  006000  005037  002376                  CLR     R2LOAD                  ;SETUP TO CLEAR ALL BITS
2567  006004  013777  002376  174340          MOV     R2LOAD,@REG2            ;WRITE BITS INTO REG 2
2568  006012  017737  174334  002400          MOV     @REG2,R2READ            ;READ REG 2 BACK
2569  006020  042737  177400  002400          BIC     #177400,R2READ          ;CLEAR UNWANTED BITS IN REG 2
2570  006026  023737  002376  002400          CMP     R2LOAD,R2READ           ;CHECK IF EXP EQUALS ACTUAL
2571  006034  001414                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
2572  006036                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
2573  006036  104455                          TRAP    C$ERDF
2574  006040  000002                          .WORD   2
2575  006042  000000                          .WORD   0
2576  006044  004706                          .WORD   R2EROR
2577  006046                                  CKLOOP
2578  006046  104406                          TRAP    C$CLP1
2579  006050  000406                          BR      7$                      ;BRANCH AROUND TIME OUT ERROR
2580  006052  005726                  6$:     TST     (SP)+                   ;CLEAN UP STACK
2581  006054  005726                          TST     (SP)+                   ;CLEAN UP STACK
2582  006056                                  ERRDF   2,,R2TM                 ;TIME OUT ERROR REG 2
2583  006056  104455                          TRAP    C$ERDF
2584  006060  000002                          .WORD   2
2585  006062  000000                          .WORD   0
2586  006064  005110                          .WORD   R2TM
2587  006066                          7$:     CLRVEC  #4                      ;CLEAR VECTOR
```

```
2588  006066  012700  000004              MOV     #4,R0
2589  006072  104436                      TRAP    C$CVEC
2590  006074  005037  002416              CLR     R6MASK                  ;SETUP TO CHECK ALL CONTROL REG 6 BITS
2591  006100                              ENDSEG
2592  006100                        10003$:
2593  006100  104405                      TRAP    C$ESEG
2594
2595  006102  000207                      RTS     PC                      ;RETURN BACK TO TEST
2596
2597                                  ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF REGISTER 0
2598                                  ;CONDITION CODES ARE SET ON EXIT AS RESULT OF THE "CMP" INSTRUCTION.
2599
2600  006104  013737  002370  002372  LDRDR0::MOV     R0LOAD,R0GOOD           ;PUT DATA LOADED INTO EXPECTED
2601  006112  013777  002370  174230  LDRD0R::MOV     R0LOAD,@REG0            ;WRITE WORD TO REGISTER 0
2602  006120  017737  174224  002374  READR0::MOV     @REG0,R0READ            ;READ REGISTER CONTENTS BACK
2603  006126  023737  002372  002374          CMP     R0GOOD,R0READ           ;COMPARE EXPECTED WITH THAT READ
2604  006134  000207                      RTS     PC                      ;EXIT WITH CONDITION CODES SET
2605
2606                                  ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF REGISTER 2.
2607                                  ;CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION
2608
2609  006136  013777  002376  174206  LDRDR2::MOV     R2LOAD,@REG2            ;WRITE BITS INTO REGISTER 2
2610  006144  017737  174202  002400  READR2::MOV     @REG2,R2READ            ;READ REGISTER 2 BACK
2611  006152  042737  177400  002400          BIC     #177400,R2READ          ;CLEAR UNWANTED BITS IN REG 2
2612  006160  023737  002376  002400          CMP     R2LOAD,R2READ           ;CHECK IF EXP EQUALS ACTUAL
2613  006166  000207                      RTS     PC                      ;EXIT WITH CONDITION CODES SET
2614
2615                                  ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF REGISTER 4.
2616                                  ;CONDITION CODES ARE SET ON EXET AS RESULT OF "CMP" INSTRUCTION.
2617
2618  006170  013737  002402  002404  LDRDAR::MOV     R4LOAD,R4GOOD           ;COPY DATA TO BE LOADED
2619  006176  000337  002404                  SWAB    R4GOOD                  ;LOW TO HIGH BYTE TO SIMULATE READBACK
2620  006202  000403                      BR      LDRD4R                  ;GO LOAD, READ + CHECK AND ARRAY
2621
2622  006204  013737  002402  002404  LDRDR4::MOV     R4LOAD,R4GOOD           ;SETUP EXPECTED DATA
2623  006212  013777  002402  174134  LDRD4R::MOV     R4LOAD,@REG4            ;WRITE WORD INTO REGISTER 4
2624  006220  017737  174130  002410  READR4::MOV     @REG4,R4READ            ;READ WORD BACK FROM REGISTER 4
2625  006226  013737  002410  002412          MOV     R4READ,R4BAD            ;COPY DATA READ
2626  006234  043737  002406  002412          BIC     R4MASK,R4BAD            ;CLEAR UNWANTED BITS
2627  006242  023737  002404  002412          CMP     R4GOOD,R4BAD            ;COMPARE WORD EXPECTED WITH READ
2628  006250  000207                      RTS     PC                      ;RETURN WITH CONDITION CODES SET
2629
2630                                  ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF CONTROL REGISTER 6
2631                                  ;CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION.
2632
2633  006252  013777  002414  174076  LDRDR6::MOV     R6LOAD,@REG6            ;WRITE WORD INTO REGISTER 6
2634  006260  017737  174072  002420  READR6::MOV     @REG6,R6READ            ;READ THE WORD BACK
2635  006266  013737  002420  002422          MOV     R6READ,R6BAD            ;COPY DATA READ
2636  006274  043737  002416  002420          BIC     R6MASK,R6READ           ;MASK OUT UNWANTED BITS
2637  006302  023737  002414  002420          CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED WITH DATA READ
2638  006310  000207                      RTS     PC                      ;EXIT WITH CONDTION CODES SET
2639
```

```
                        ;**
                        ; THIS ROUTINE WILL WRITE AND READ THE TRACE RAM ADDRESS REGISTER BITS TRAD 9:0
                        ; WITH THE CONTENTS OF LOCATION "TRADRS"
                        ;
                        ; TO WRITE THE TRACE RAM ADDRESS REGISTER THE PROGRAM WILL CLEAR CONTROL REG 2
                        ; BITS PDAL7 TO PDAL0 WHICH WILL ASSERT THE SIGNAL PTERO L IN THE POINTER REG-
                        ; ISTER.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REIGSTER 0 WITH THE SIGNAL
                        ; PTERO L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPTO L. THE SIGNAL
                        ; WPTO L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE TRACE RAM ADDRESS
                        ; REGISTER.
                        ;
                        ; WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH THE SIGNAL PTERO L
                        ; ASSERTED IN THE POINTER REGISTER, A PULSE WILL BE ISSUED ON THE SIGNAL RPTO H.
                        ; THE SIGNAL RPTO H WILL READ THE DATA FROM THE TRACE RAM ADDRESS REGISTER.
                        ;
                        ;       INPUT:  LOCATION "TRADRS" MUST CONTAIN ADDRESS TO LOAD
                        ;       CALL:   JSR     PC,TRADLD
                        ;       EXIT:   LOCATION R6MASK WILL EQUAL 176000
                        ;--

006312                  TRADLD::BGNSEG
006312  104404                  TRAP    C$BSEG

                                ;CLEAR ALL BITS IN CONTROL REGISTER 2. CONTROL REGISTER 2 BITS PDAL3
                                ;TO PDAL0 BEING CLEARED WILL ASSERT THE SIGNAL PTERO L IN THE POINTER
                                ;REGISTER.

006314  005037  002376          CLR     R2LOAD                  ;SETUP TO CLEAR ALL BITS IN REG 2
006320  004737  006136          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
006324  001405                  BEQ     1$                      ;IF LOADED OK THEN CONTINUE
006326                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
006326  104455                  TRAP    C$ERDF
006330  000002                  .WORD   2
006332  000000                  .WORD   0
006334  004706                  .WORD   R2EROR
006336                          CKLOOP
006336  104406                  TRAP    C$CLP1

                                ;WRITE THE TRACE RAM ADDRESS WITH THE ADDRESS IN LOCATION "TRADRS".
                                ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTERO L
                                ;ASSERTED, THE SIGNAL WPTO L WILL PULSE TO LOAD THE TRACE RAM ADDRESS
                                ;REGISTER.  ON A READ COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL
                                ;PTERO L ASSERTED, THE SIGNAL RPTO H WILL PULSE TO READ THE TRACE RAM
                                ;ADDRESS REGISTER BITS TRAD 9:0.

006340  013737  006376  002414  1$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS TO BE LOADED
006346  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
006354  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ & CHECK TRAD BITS 9:0
006360  001404                          BEQ     2$                      ;IF ADDRESS OK THEN CONTINUE
006362                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQUAL "TRADRS"
006362  104455                          TRAP    C$ERDF
006364  000004                          .WORD   4
006366  002464                          .WORD   TRADER
006370  004736                          .WORD   R026ER
006372                          2$:     ENDSEG
006372                          10004$:
```

```
2696  006372  104405                  TRAP    C$ESEG
2697  006374  000207                  RTS     PC
2698
2699  006376  000000          TRADRS::.WORD   0                       ;CONTAINS TRACE RAM ADDRESS
2700
2701                          ;**
2702                          ; THIS ROUTINE WILL USE THE CONTENTS OF R5 AS A POINTER TO A WORD TO BE
2703                          ; LOADED TO CONTROL REGISTER 2.  THE WORD WILL ASSERT A PARTICULAR SIGNAL
2704                          ; IN THE POINTER REGISTER.
2705                          ;--
2706
2707  006400  012537  002376  ASSERT::MOV     (R5)+,R2LOAD            ;SETUP BITS TO BE LOADED
2708  006404                          BGNSEG
2709  006404  104404                  TRAP    C$BSEG
2710  006406  004737  006136          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
2711  006412  001404                  BEQ     1$                      ;IF LOADED OK THEN CONTINUE
2712  006414                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
2713  006414  104455                  TRAP    C$ERDF
2714  006416  000002                  .WORD   2
2715  006420  000000                  .WORD   0
2716  006422  004706                  .WORD   R2EROR
2717  006424                  1$:     ENDSEG
2718  006424                  10005$:
2719  006424  104405                  TRAP    C$ESEG
2720  006426  000205                  RTS     R5                      ;EXIT BACK TO MAIN LINE CODE
```

```
                        ;**
                        ; THIS TEST WILL WRITE AND READ THE TRACE RAM DATA IN BUFFERS FROM THE LSI-11
                        ; BUS WITH THE CONTENTS OF LOCATION "R6LOAD".  THE TRACE RAM DATA IN BUFFERS
                        ; TESTED BY THIS ROUTINE ARE TRDI BITS 15:0, TRDI BITS 31:16, TRDI BITS 47:32,
                        ; OR TRDI BITS 59:48.  FOR EACH CALL TO THIS ROUTINE, ONLY ONE SET OF TRACE
                        ; RAM DATA IN BUFFERS WILL BE TESTED.
                        ;
                        ; PREVIOUS TO THIS ROUTINE, IN ROUTINE "INITED", CONTROL REGISTER 0 BITS CDAL7
                        ; TO CDAL0 WERE CLEARED.  CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                        ; TRSL0 L TO BE ASSERTED.  THE SIGNAL TRSL0 L ASSERTED WILL ENABLE THE OUTPUTS
                        ; OF THE TRACE RAM DATA IN BUFFERS.
                        ;
                        ; TO WRITE THE TRACE RAM DATA IN BUFFERS, THE PROGRAM WILL LOAD CONTROL REG 2
                        ; WITH THE BITS TO SELECT PTER5 L, PTER6 L, PTER7 L OR PTER8 L IN THE POINTER
                        ; REGISTER.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH ONE OF
                        ; THE ABOVE SIGNALS SET IN THE POINTER REGISTER, A PULSE WILL BE ISSUED ON
                        ; THE SIGNAL WPT5 H, WPT6 H, WPT7 H, OR WPT8 H RESPECTIVELY.  THESE LAST
                        ; SIGNALS MENTIONED WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE TRACE
                        ; RAM DATA IN BUFFER BITS TRDI 15:0, TRDI 31:16, TRDI 47:32, OR TRDI 59:48
                        ; RESPECTIVELY.
                        ;
                        ; TO READ THE TRACE RAM DATA IN BUFFERS, THE PROGRAM WILL LOAD CONTROL REGISTER
                        ; 2 WITH THE BITS TO SELECT PTER1 L, PTER2 L, PTER3 L OR PTER4 L IN THE POINTER
                        ; REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH ONE OF THE
                        ; ABOVE SIGNALS SET IN THE POINTER REGISTER, A PULSE WILL BE ISSUED ON THE SIGNAL
                        ; RTP1 H, RPT2 H, RPT3 H OR RPT4 H RESPECTIVELY.  THESE LAST SIGNALS ON A READ
                        ; COMMAND WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BITS TRDI 15:0,
                        ; TRDI 31:16, TRDI 47:32 OR TRDI 59:48 RESPECTIVELY.
                        ;
                        ;       INPUT:  LOCATION "R6LOAD" CONTAINS DATA TO BE LOADED
                        ;
                        ;       CALL:   JSR     R5,TRDIBF       ;GO LOAD,READ + CHECK TRAM DATA IN BUF.
                        ;               .WORD   PTER5           ;CONTROL REGISTER 2 WRITE POINTER SEL.
                        ;                                       ;READ POINTER WILL BE DONE BY DOING -4.
                        ;--
                        ;
006430                  TRDIBF::BGNSEG
006430  104404          TRAP    C$BSEG
                        ;
                        ;SET PDAL BITS 3-0 IN CONTROL REGISTER 2 TO ASSERT THE SIGNAL
                        ;PTER5 L, PTER6 L, PTER7 L OR PTER8 L. THE PARAMTER FOLLOWING THE CALL
                        ;CONTAINS THE BITS TO BE LOADED INTO CONTROL REGISTER 2.
                        ;
006432  011537  002376  MOV     (R5),R2LOAD     ;GET THE PDAL BITS TO BE LOADED
006436  004737  006136  JSR     PC,LDRDR2       ;GO LOAD, READ AND CHECK REG  2
006442  001405          BEQ     1$              ;IF LOADED OK THE CONTINUE
006444                  ERRDF   2,,R2EROR       ;REGISTER 2 NOT EQUAL EXPECTED
006444  104455          TRAP    C$ERDF
006446  000002          .WORD   2
006450  000000          .WORD   0
006452  004706          .WORD   R2EROR
006454                  CKLOOP
006454  104406          TRAP    C$CLP1
                        ;
                        ;LOAD DATA PATTERN INTO TRACE RAM DATA IN BUFFER. WHEN A WRITE COMMAND
                        ;IS ISSUED TO CONTROL REGISTER 6 WITH THE SIGNAL PTER5 L, PTER6 L,
```

```
                                        ;PTER7 L OR PTER8 L ASSERTED, A PULSE WILL BE ISSUED ON WPT5 H, WPT6 H,
                                        ;WPT7 H OR WPT8 H RESPECTIVELY WHICH WILL LOAD THE DATA INTO THE TRACE
                                        ;RAM DATA IN BUFFER.

006456  013777  002414  173672  1$:   MOV     R6LOAD,@REG6            ;WRITE DATA INTO TRAM DATA IN BUF

                                        ;SUBTRACT 4 FROM THE PDAL BITS LOADED PREVIOUSLY INTO CONTROL REGISTER
                                        ;2 TO ASSERT THE SIGNALS PTER1 L, PTER2 L, PTER3 L OR PTER4 L IN THE
                                        ;POINTER REGISTER.

006464  162737  000004  002376          SUB     #4,R2LOAD               ;BACK UP POINTER REGISTER BY 4 SIGNALS
006472  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
006476  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
006500                                  ERRDF   2,,R2EROR               ;REGISTER 2NOT EQULA EXPECTED
006500  104455                          TRAP    C$ERDF
006502  000002                          .WORD   2
006504  000000                          .WORD   0
006506  004706                          .WORD   R2EROR
006510                                  CKLOOP
006510  104406                          TRAP    C$CLP1

                                        ;READ AND CHECK DATA PATTERN FROM THE TRACE RAM DATA IN BUFFER. WHEN
                                        ;A READ COMMAND IS ISUED TO CONTROL REGISTER 6 WITH THE SIGNAL PTER1 L,
                                        ;PTER2 L, PTER3 L OR PTER4 L ASSERTED, A PULSE WILL BE ISSUED ON THE
                                        ;SIGNAL RPT1 H, RPT2 H, RPT3 H OR RPT4 H RESPECTIVELY WHICH WILL READ
                                        ;THE DATA FROM  THE TRACE RAM DATA IN BUFFER SELECTED.

006512  017737  173640  002420  2$:   MOV     @REG6,R6READ            ;READ THE DATA AND SAVE IT
006520  022715  000010                  CMP     #PTER8,(R5)             ;CHECK IF TESTING TRDI 59:48
006524  001003                          BNE     3$                      ;IF NOT GO CHECK ALL BITS
006526  042737  170000  002420          BIC     #170000,R6READ          ;CLEAR UNUSED BITS
006534  023737  002414  002420  3$:    CMP     R6LOAD,R6READ           ;CHECK DATA LOADED AGAINST DATA READ
006542  001434                          BEQ     7$                      ;IF DATA OK THEN EXIT
006544  022715  000005                  CMP     #PTER5,(R5)             ;CHECK IF TRDI BITS 15:0
006550  001005                          BNE     4$                      ;IF NOT CHECK NEXT SET
006552                                  ERRDF   4,TRDI15,R026ER         ;TRDI 15 TO TRDI 0 NOT EQUAL EXPECTED
006552  104455                          TRAP    C$ERDF
006554  000004                          .WORD   4
006556  002521                          .WORD   TRDI15
006560  004736                          .WORD   R026ER
006562  000424                          BR      7$                      ;CONTINUE IF PROCEED FROM ERROR
006564  022715  000006          4$:     CMP     #PTER6,(R5)             ;CHECK IF TRDI BITS 31:16
006570  001005                          BNE     5$                      ;IF NOT THEN CHECK NEXT SET
006572                                  ERRDF   4,TRDI31,R026ER         ;TRDI 31 TO TRDI 16 NOT EQUAL EXPECTED
006572  104455                          TRAP    C$ERDF
006574  000004                          .WORD   4
006576  002556                          .WORD   TRDI31
006600  004736                          .WORD   R026ER
006602  000414                          BR      7$                      ;CONTINUE IF PROCEED FROM ERROR
006604  022715  000007          5$:     CMP     #PTER7,(R5)             ;CHECK IF TRDI NITS 47:32
006610  001005                          BNE     6$                      ;IF NOT MUST BE TRDI BITS 59:48
006612                                  ERRDF   4,TRDI47,R026ER         ;TRDI 47 TO TRDI 32 NOT EQUAL EXPECTED
006612  104455                          TRAP    C$ERDF
006614  000004                          .WORD   4
006616  002614                          .WORD   TRDI47
006620  004736                          .WORD   R026ER
```

```
2833  006622  000404                        BR      7$                      ;CONTINUE IF PROCEED FROM ERROR
2834  006624                          6$:     ERRDF   4,TRDI59,R026ER         ;TRDI 59 TO TRDI 48 NOT EQUAL EXPECTED
2835  006624  104455                        TRAP    C$ERDF
2836  006626  000004                        .WORD   4
2837  006630  002652                        .WORD   TRDI59
2838  006632  004736                        .WORD   R026ER
2839  006634                          7$:     ENDSEG
2840  006634                          10006$:
2841  006634  104405                        TRAP    C$ESEG
2842  006636  005725                        TST     (R5)+                   ;UPDATE POINTER FOR RETURN
2843  006640  000205                        RTS     R5                      ;EXIT BACK TO MAIN LINE CODE
2844
2845                                  ;THE FOLLOWING ROUTINE WILL SET AND CLEAR CDAL6 IN CONTROL REGISTER 0. SETTING
2846                                  ;AND CLEARING CDAL6 WILL CAUSE A PULSE ON THE SIGNAL TRANST H.  THE SIGNAL
2847                                  ;TRANST H WILL CAUSE A PULSE ON THE SIGNAL ANST L, WHICH WILL CAUSE A PULSE ON
2848                                  ;THE SIGNAL ORST L.
2849
2850  006642                          TRANST::BGNSEG
2851  006642  104404                        TRAP    C$BSEG
2852  006644  052737  000100  002370        BIS     #CDAL6,ROLOAD           ;SET BIT CDAL6 IN CONTROL REGISTER 0
2853  006652  004737  006104                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
2854  006656  001405                        BEQ     1$                      ;IF LOADED OK THEN CONTINUE
2855  006660                                ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
2856  006660  104455                        TRAP    C$ERDF
2857  006662  000001                        .WORD   1
2858  006664  000000                        .WORD   0
2859  006666  004606                        .WORD   ROEROR
2860  006670                                CKLOOP
2861  006670  104406                        TRAP    C$CLP1
2862  006672  042737  000100  002370  1$:   BIC     #CDAL6,ROLOAD           ;SETUP TO CLEAR CDAL6
2863  006700  004737  006104                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
2864  006704  001404                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
2865  006706                                ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
2866  006706  104455                        TRAP    C$ERDF
2867  006710  000001                        .WORD   1
2868  006712  000000                        .WORD   0
2869  006714  004606                        .WORD   ROEROR
2870  006716                          2$:     ENDSEG
2871  006716                          10007$:
2872  006716  104405                        TRAP    C$ESEG
2873  006720  000207                        RTS     PC                      ;RETURN BACK TO TEST BEING EXECUTED
2874
2875  006722                                ENDMOD
2876
2877                                  .TITLE MISCELLANEOUS SECTIONS
2878                                  .SBTTL  REPORT CODING SECTION
2879
2880  006722                                BGNMOD
2881
2882                                  ;++
2883                                  ; THE REPORT CODING SECTION CONTAINS THE
2884                                  ; "PRINTS" CALLS THAT GENERATE STATISTICAL REPORTS.
2885                                  ;--
2886
2887  006722                                BGNRPT
2888  006722                          L$RPT::
```

```
2889
2890
2891  006722                                  EXIT    RPT
2892  006722  000167                          .WORD   J$JMP
2893  006724  000000                          .WORD   L10014-2-.
2894
2895
2896                                          .EVEN
2897
2898  006726                                  ENDRPT
2899  006726                          L10014:
2900  006726  104425                          TRAP    C$RPT
2901
2902                                  .SBTTL  PROTECTION TABLE
2903
2904                                  ;++
2905                                  ; THIS TABLE IS USED BY THE RUNTIME SERVICES
2906                                  ; TO PROTECT THE LOAD MEDIA.
2907                                  ;--
2908
2909  006730                                  BGNPROT
2910  006730                          L$PROT::
2911
2912  006730  177777                          -1              ;OFFSET INTO P-TABLE FOR CSR ADDRESS
2913  006732   77777                          -1              ;OFFSET INTO P-TABLE FOR MASSBUS ADDRESS
2914  006734  17~777                          -1              ;OFFSET INTO P-TABLE FOR DRIVE NUMBER
2915
2916  006736                                  ENDPROT
```

```
                                        .SBTTL  INITIALIZE SECTION

                                        ;++
                                        ; THE INITIALIZE SECTION CONTAINS THE CODING THAT IS PERFORMED
                                        ; AT THE BEGINNING OF EACH PASS.
                                        ;--

006736                                          BGNINIT
006736                                  L$INIT::
006736                                          READEF  #EF.START               ;SEE IF A START COMMAND
006736  012700  000040                          MOV     #EF.START,R0
006742  104447                                  TRAP    C$REFG
006744                                          BCOMPLETE       1$              ;BRANCH IF START COMMAND
006744  103410                                  BCS     1$
006746                                          READEF  #EF.RESTART             ;SEE IF A RESTART COMMAND
006746  012700  000037                          MOV     #EF.RESTART,R0
006752  104447                                  TRAP    C$REFG
006754                                          BCOMPLETE       1$              ;BRANCH IF RESTART
006754  103404                                  BCS     1$
006756                                          READEF  #EF.PWR                 ;SEE IF RECOVERING FROM A POWER FAIL
006756  012700  000034                          MOV     #EF.PWR,R0
006762  104447                                  TRAP    C$REFG
006764                                          BNCOMPLETE      2$              ;IF NOT CHECK IN CONTINUE
006764  103001                                  BCC     2$
006766                                  1$:     BRESET                          ;ISSUE A BUS RESET TO CLEAR THE SYSTEM
006766  104433                                  TRAP    C$RESET
006770                                  2$:     READEF  #EF.NEW                 ;SEE IF A NEW PASS
006770  012700  000035                          MOV     #EF.NEW,R0
006774  104447                                  TRAP    C$REFG
006776                                          BNCOMPLETE      3$              ;IF NOT GO CHECK IF CONTINUE
006776  103003                                  BCC     3$
007000  012737  177777  002362                  MOV     #-1,UNITNB              ;SETUP TO INIT UNIT NUMBER
007006                                  3$:     READEF  #EF.CONTINUE            ;CHECK IF CONTINUE
007006  012700  000036                          MOV     #EF.CONTINUE,R0
007012  104447                                  TRAP    C$REFG
007014                                          BCOMPLETE       6$              ;IF YES THEN EXIT
007014  103434                                  BCS     6$
007016  005237  002362                  4$:     INC     UNITNB                  ;INC TO NEW UNIT NUMBER
007022                                          GPHARD  UNITNB,R5               ;GET DEVICE INFORMATION
007022  013700  002362                          MOV     UNITNB,R0
007026  104442                                  TRAP    C$GPHRD
007030  010005                                  MOV     R0,R5
007032                                          BNCOMPLETE      4$              ;GO TRY ANOTHER UNIT
007032  103371                                  BCC     4$
007034  012701  002350                          MOV     #REG0,R1                ;ADDRESS OF ED DEVICE ADDRESS TABLE
007040  005002                                  CLR     R2                      ;CLEAR OFFSET TO ADD TO TABLE ADDRESS
007042  011511                          5$:     MOV     (R5),(R1)               ;GET ADDRESS AND SAVE
007044  060221                                  ADD     R2,(R1)+                ;ADD OFFSET TO ADDRESS
007046  005202                                  INC     R2                      ;UPDATE OFFSET BY 2
007050  005202                                  INC     R2                      ;
007052  022702  000010                          CMP     #10,R2                  ;CHECK IF DONE LOADING TABLE
007056  001371                                  BNE     5$                      ;GO UPDATE NEXT ADDRESS
007060  005725                                  TST     (R5)+                   ;UPDATE THE POINTER
007062  005037  002360                          CLR     IDDEV                   ;CLEAR OUT DEVICE NUMBER
```

```
2973  007066  111537  002361                  MOVB    (R5),IDDEV+1            ;GET THE ED DEVICE NUMBER
2974  007072  012737  101000  002364          MOV     #CDAL15!CDAL9,IDTYPE    ;SETUP ED DEVICE TYPE
2975  007100  005725                          TST     (R5)+                   ;UPDATE THE POINTER
2976  007102  011537  002366                  MOV     (R5),EXTPRB             ;GET EXTERNAL PROBE INDICATOR
2977  007106                          6$:     SETPRI  #PRI07                  ;RAISE PROCESSOR PRIORITY
2978  007106  012700  000340                  MOV     #PRI07,R0
2979  007112  104441                          TRAP    C$SPRI
2980
2981
2982  007114                                  EXIT    INIT
2983  007114  104432                          TRAP    C$EXIT
2984  007116  000002                          .WORD   L10016-.
2985
2986
2987                                          .EVEN
2988
2989  007120                                  ENDINIT
2990  007120                          L10016:
2991  007120  104411                          TRAP    C$INIT
2992
2993                                  .SBTTL  AUTODROP SECTION
2994
2995                                  ;++
2996                                  ; THIS CODE IS EXECUTED IMMEDIATELY AFTER THE INITIALIZE CODE IF
2997                                  ; THE "ADR" FLAG WAS SET.  THE UNIT(S) UNDER TEST ARE CHECKED TO
2998                                  ; SEE IF THEY WILL RESPOND.  THOSE THAT DON'T ARE IMMEDIATELY
2999                                  ; DROPPED FROM TESTING.
3000                                  ;--
3001
3002  007122                                  BGNAUTO
3003  007122                          L$AUTO::
3004
3005
3006  007122                                  ENDAUTO
3007  007122                          L10017:
3008  007122  104461                          TRAP    C$AUTO
3009
3010                                  .SBTTL  CLEANUP CODING SECTION
3011
3012                                  ;++
3013                                  ; THE CLEANUP CODING SECTION CONTAINS THE CODING THAT IS PERFORMED
3014                                  ; AFTER THE HARDWARE TESTS HAVE BEEN PERFORMED.
3015                                  ;--
3016
3017  007124                                  BGNCLN
3018  007124                          L$CLEAN::
3019  007124  013777  002360  173216          MOV     IDDEV,@REG0             ;CLEAR CONTROL REGISTER 0 EXCEPT
3020                                                                          ;FOR DEVICE NUMBER
3021  007132  012777  000000  173212          MOV     #0,@REG2                ;CLEAR REGISTER 2
3022
3023
3024  007140                                  EXIT    CLN
3025  007140  104432                          TRAP    C$EXIT
3026  007142  000002                          .WORD   L10020-.
3027
3028
```

```
                                        .EVEN

                                        ENDCLN
                                L10020:
                                        TRAP    C$CLEAN

                                .SBTTL  DROP UNIT SECTION

                                ;++
                                ; THE DROP-UNIT SECTION CONTAINS THE CODING THAT CAUSES A DEVICE
                                ; TO NO LONGER BE TESTED.
                                ;--

                                        BGNDU
                                L$DU::


                                        EXIT    DU
                                        .WORD   J$JMP
                                        .WORD   L10021-2-.


                                        .EVEN

                                        ENDDU
                                L10021:
                                        TRAP    C$DU

                                .SBTTL  ADD UNIT SECTION

                                ;++
                                ; THE ADD-UNIT SECTION CONTAINS ANY CODE THE PROGRAMMER WISHES
                                ;  TO BE EXECUTED IN CONJUNCTION WITH THE ADDING OF A UNIT BACK
                                ;  TO THE TEST CYCLE.
                                ;--

                                        BGNAU
                                L$AU::


                                        EXIT    AU
                                        .WORD   J$JMP
                                        .WORD   L10022-2-.


                                        .EVEN

                                        ENDAU
                                L10022:
                                        TRAP    C$AU

                                        ENDMOD
```

```
                                .TITLE HARDWARE TESTS

                                .SBTTL  TEST 1: SELECT AND INITIALIZE STATE ANALYZER

007162                                  BGNMOD

                                ;++
                                ; TEST TO CHECK THAT THE STATE ANALYZER CAN BE SELECTED AND INITIALIZED TO
                                ; A KNOWN STATE. THIS TEST WILL BE EXECUTED AT THE BEGINNING OF EVERY TEST
                                ; TO PUT THE MODULE IN A KNOWN STATE.  THE TEST WILL LOAD THE DEVICE NUMBER INTO
                                ; CONTROL REGISTER 0 AND CHECK THAT THE DEVICE NUMBER CAN BE READ CORRECTLY.
                                ; THE LOW BYTE OF CONTROL REGISTER 0 WILL BE CHECKED TO BE ZERO. THE TEST WILL
                                ; THEN LOAD THE DEVICE NUMBER AND THE SIGNAL CDAL15 INTO CONTROL REGISTER 0,
                                ; AND CHECK THAT THE DEVICE TYPE AND THE LOW BYTE CAN BE READ BACK CORRECTLY.
                                ; THE TEST WILL THEN CLEAR THE SIGNAL CDAL15 IN CONTROL REGISTER 0 AND CHECK
                                ; THE DEVICE NUMBER AND THE LOW BYTE TO BE CORRECT.  THE TEST WILL THEN LOAD
                                ; READ AND CHECK CONTROL REGISTER 2 WITH ZEORES.
                                ;--



007162                                  BGNTST
007162                          T1::
007162  004737  005476                  JSR     PC,INITED               ;INITIALIZE THE STATE ANALYZER



007166                                  ENDTST
007166                          L10023:
007166  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 2: CONTROL REG 0 TES: (1'S, AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS CDAL7,CDAL6,
                                ; CDAL5,CDAL4,CDAL3,CDAL2,CDAL1, AND CDAL0 CAN BE SET TO A ONE AND THEN
                                ; SET TO ALL ZEROES.
                                ;--

007170                                  BGNTST
007170                          T2::
007170  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007174                                  BGNSEG
007174  104404                          TRAP    C$BSEG

                                        ;SET CONTROL REGISTER 0 R/W BITS CDAL7 TO CDAL0 TO ALL ONES

007176  112737  000377  002370          MOVB    #377,ROLOAD             ;SETUP TO LOAD ALL ONES
007204  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
007210  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007212                                  ERRDF   1,,ROEROR               ;CDAL7 TO CDAL0 NOT EQL TO 377
007212  104455                          TRAP    C$ERDF
007214  000001                          .WORD   1
007216  000000                          .WORD   0
007220  004606                          .WORD   ROEROR
007222                          1$:     ENDSEG
007222                          10000$:
007222  104405                          TRAP    C$ESEG

007224                                  BGNSEG
007224  104404                          TRAP    C$BSEG

                                        ;SET CONTROL REGISTER 0 R/W BITS CDAL7 TO CDAL0 TO ALL ZEROES

007226  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR ALL BITS
007232  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
007236  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
007240                                  ERRDF   1,,ROEROR               ;CDAL7 TO CDAL0 NOT EQL 0
007240  104455                          TRAP    C$ERDF
007242  000001                          .WORD   1
007244  000000                          .WORD   0
007246  004606                          .WORD   ROEROR
007250                          2$:     ENDSEG
007250                          10001$:
007250  104405                          TRAP    C$ESEG
007252                                  ENDTST
007252                          L10024:
007252  104401                          TRAP    C$ETST
```

```
                                        .SBTTL  TEST 3: CONTROL REG 0 TEST (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK CONTROL REGISTER 0 READ/WRITE BITS CDAL7 TO CDAL0
                                        ; WITH AN ALTERNATING ONES AND ZEROES PATTERN (252) AND THEN AN ALTERNATING
                                        ; ZEROES AND ONES PATTERN (125).
                                        ;--

007254                                  T3::    BGNTST
007254                                          
007254  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007260                                          BGNSEG
007260  104404                                  TRAP    C$BSEG

                                        ;SET CDAL7, CDAL5, CDAL3, AND CDAL1 EQUAL TO ONES
                                        ;SET CDAL6, CDAL4, CDAL2, AND CDAL0 EQUAL TO ZEROES

007262  112737  000252  002370                  MOVB    #252,ROLOAD             ;SET ONES AND ZEROES PATTERN
007270  004737  006104                          JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
007274  001404                                  BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007276                                          ERRDF   1,,ROEROR               ;CDAL7 TO CDAL0 NOT EQL 252
007276  104455                                  TRAP    C$ERDF
007300  000001                                  .WORD   1
007302  000000                                  .WORD   0
007304  004606                                  .WORD   ROEROR
007306                                  1$:     ENDSEG
007306                                  10000$:
007306  104405                                  TRAP    C$ESEG

007310                                          BGNSEG
007310  104404                                  TRAP    C$BSEG

                                        ;SET CDAL7, CDAL5, CDAL3 AND CDAL1 TO ZEROES
                                        ;SET CDAL6, CDAL4, CDAL2 AND CDAL0 TO ONES

007312  112737  000125  002370                  MOVB    #125,ROLOAD             ;SET ZEROES AND ONES PATTERN
007320  004737  006104                          JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
007324  001404                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
007326                                          ERRDF   1,,ROEROR               ;CDAL7 TO CDAL0 NOT EQL 125
007326  104455                                  TRAP    C$ERDF
007330  000001                                  .WORD   1
007332  000000                                  .WORD   0
007334  004606                                  .WORD   ROEROR
007336                                  2$:     ENDSEG
007336                                  10001$:
007336  104405                                  TRAP    C$ESEG
007340                                          ENDTST
007340                                  L10025:
007340  104401                                  TRAP    C$ETST
```

```
                                .SBTTL  TEST 4: CONTROL REGISTER 0 TEST USING A BINARY COUNT

                                ;++
                                ; THIS TEST WILL CHECK CONTROL REGISTER 0 READ/WRITE BITS CDAL7 TO CDAL0
                                ; USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND
                                ; INCREMENT UNTIL THE TEST PATTERN 377 HAS BEEN LOADED AND TESTED.
                                ;--

007342                                  BGNTST
007342                          T4::
007342  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007346  105037  002370                  CLRB    ROLOAD                  ;SET TEST PATTERN INITIALLY TO 0

007352                          1$:     BGNSEG
007352  104404                          TRAP    C$BSEG
007354  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
007360  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
007362                                  ERRDF   1,,ROEROR               ;REG 0 NOT EQUAL EXPECTED
007362  104455                          TRAP    C$ERDF
007364  000001                          .WORD   1
007366  000000                          .WORD   0
007370  004606                          .WORD   ROEROR
007372                          2$:     ENDSEG
007372                          10000$:
007372  104405                          TRAP    C$ESEG

007374  105237  002370                  INCB    ROLOAD                  ;UPDATE THE TEST PATTERN BY 1
007400  001364                          BNE     1$                      ;IF NOT 0 LOAD, NEXT PATTERN
007402                                  ENDTST
007402                          L10026:
007402  104401                          TRAP    C$ETST
```

```
                                       .SBTTL  TEST 5: CONTROL REG 2 TEST (1'S, AND 0'S)

                                       ;++
                                       ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7, PDAL6, PDAL5,
                                       ; PDAL4, PDAL3, PDAL2, PDAL1 AND PDAL0, TO BE SET TO ALL ONES AND THEN ALL
                                       ; ZEROES.
                                       ;--

007404                                         BGNTST
007404                                 T5::
007404  004737  005476                         JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007410                                         BGNSEG
007410  104404                                 TRAP    C$BSEG

                                               ;SET CONTROL REGISTER 2 BITS PDAL7 TO PDAL0 TO ALL ONES

007412  012737  000377  002376                 MOV     #377,R2LOAD             ;SETUP BITS TO BE LOADED
007420  004737  006136                         JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
007424  001404                                 BEQ     1$                      ;IF ALL ONES THEN CONTINUE
007426                                         ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL 377
007426  104455                                 TRAP    C$ERDF
007430  000002                                 .WORD   2
007432  000000                                 .WORD   0
007434  004706                                 .WORD   R2EROR
007436                                 1$:     ENDSEG
007436                                 10000$:
007436  104405                                 TRAP    C$ESEG

007440                                         BGNSEG
007440  104404                                 TRAP    C$BSEG

                                               ;SET CONTROL REGISTER 2 BITS PDAL7 TO PDAL0 TO ALL ZEROES

007442  005037  002376                         CLR     R2LOAD                  ;SETUP TO CLEAR ALL BITS
007446  004737  006136                         JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
007452  001404                                 BEQ     2$                      ;IF ALL ZEROES THEN CONTINUE
007454                                         ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL TO 0
007454  104455                                 TRAP    C$ERDF
007456  000002                                 .WORD   2
007460  000000                                 .WORD   0
007462  004706                                 .WORD   R2EROR
007464                                 2$:     ENDSEG
007464                                 10001$:
007464  104405                                 TRAP    C$ESEG
007466                                         ENDTST
007466                                 L10027:
007466  104401                                 TRAP    C$ETST
```

```
                                .SBTTL  TEST 6: CONTROL REG 2 TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7 TO PDAL0 WITH
                                ; AN ALTERNATING ONES AND ZEROES PATTERN (252) AND THEN AN ALTERNATING ZEROES
                                ; AND ONES PATTERN (125).
                                ;--

007470                                  BGNTST
007470                          T6::
007470  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007474                                  BGNSEG
007474  104404                          TRAP    C$BSEG

                                        ;SET PDAL7, PDAL5, PDAL3, AND PDAL1 TO ONES
                                        ;SET PDAL6, PDAL4, PDAL2, AND PDAL0 TO ZEROES

007476  012737  000252  002376          MOV     #252,R2LOAD             ;SETUP BITS TO BE LOADED
007504  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
007510  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007512                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL 252
007512  104455                          TRAP    C$ERDF
007514  000002                          .WORD   2
007516  000000                          .WORD   0
007520  004706                          .WORD   R2EROR
007522                          1$:     ENDSEG
007522                          10000$:
007522  104405                          TRAP    C$ESEG

007524                                  BGNSEG
007524  104404                          TRAP    C$BSEG

                                        ;SET PDAL7, PDAL5, PDAL3 AND PDAL1 TO ZEROES
                                        ;SET PDAL6, PDAL4, PDAL2 AND PDAL0 TO ONES

007526  012737  000125  002376          MOV     #125,R2LOAD             ;SETUP BITS TO BE LOADED
007534  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
007540  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
007542                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL 125
007542  104455                          TRAP    C$ERDF
007544  000002                          .WORD   2
007546  000000                          .WORD   0
007550  004706                          .WORD   R2EROR
007552                          2$:     ENDSEG
007552                          10001$:
007552  104405                          TRAP    C$ESEG
007554                                  ENDTST
007554                          L10030:
007554  104401                          TRAP    C$ETST
```

```
                                        .SBTTL  TEST 7: CONTROL REG 2 TEST USING A BINARY COUNT

                                        ;++
                                        ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7 TO PDAL0
                                        ; USING A BINARY COUNT PATTERN.  THE TEST WILL START WITH DATA PATTERN OF
                                        ; ZERO AND INCREMENT THE PATTERN UNTIL THE PATTERN 377 HAS BEEN LOADED AND
                                        ; TESTED
                                        ;--

007556                                          BGNTST
007556                                  T7::
007556  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
007562  005037  002376                          CLR     R2LOAD                  ;SET TEST PATTERN TO ZERO

007566                                  1$:     BGNSEG
007566  104404                                  TRAP    C$BSEG
007570  004737  006136                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
007574  001404                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
007576                                          ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL EXPECTED
007576  104455                                  TRAP    C$ERDF
007600  000002                                  .WORD   2
007602  000000                                  .WORD   0
007604  004706                                  .WORD   R2EROR
007606                                  2$:     ENDSEG
007606                                  10000$:
007606  104405                                  TRAP    C$ESEG

007610  105237  002376                          INCB    R2LOAD                  ;INCREMENT THE TEST PATTERN BY 1
007614  001364                                  BNE     1$                      ;IF NOT 0 THEN LOAD NEXT PATTERN
007616                                          ENDTST
007616                                  L10031:
007616  104401                                  TRAP    C$ETST
```

```
                        .SBTTL  TEST 8: TRAM ADDRESS REG TEST (1'S, AND 0'S)

                        ;++
                        ; THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) BY
                        ; LOADING A PATTERN OF ALL ONES (3777) INTO THE ADDRESS REGISTER AND THEN
                        ; READING AND CHECKING THE REGISTER FOR ALL ONES.  THE TEST WILL THEN LOAD,
                        ; READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH A DATA PATTERN OF ALL
                        ; ZEROES.  TO WRITE AND READ THE TRACE RAM ADDRESS REGISTER, THE PROGRAM WILL
                        ; CLEAR CONTROL REGISTER 0 BITS CDAL7 TO CDAL0, CLEAR CONTROL REGISTER 2 BITS
                        ; PDAL7 TO PDAL0, LOAD THE DATA PATTERN INTO THE TRACE RAM ADDRESS REGISTER
                        ; VIA A WRITE COMMAND TO CONTROL REGISTER 6, AND THEN READ THE TRACE RAM ADDRESS
                        ; REGISTER VIA A READ COMMAND TO CONTROL REGISTER 6.  WHEN PDAL BITS 3,2,1, AND 0
                        ; ARE SET TO A 0, THE POINTER REGISTER SIGNAL PTER0 L WILL BE ASSERTED LOW. THIS
                        ; SIGNAL BEING SET LOW ALONG WITH A WRITE OR READ COMMAND TO CONTROL REGISTER 6
                        ; WILL ASSERT THE SIGNAL WPT0 L OR RPT0 H RESPECTIVELY.  THE SIGNAL WPT0 L WILL
                        ; LOAD THE ADDRESS INTO THE TRACE RAM ADDRESS REGISTER AND THE SIGNAL RPT0 H
                        ; WILL READ THE ADDRESS FROM THE TRACE RAM ADDRESS REGISTER.
                        ;--

                                BGNTST
                        T8::
                                JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                BGNSEG
                                TRAP    C$BSEG

                                ;CLEAR ALL BITS IN CONTROL REGISTER 2. CONTROL REGISTER 2 BITS PDAL3 TO
                                ;PDAL0 BEING CLEARED WILL ASSERT THE SIGNAL PTER0 L IN THE POINTER REG.

                                CLR     R2LOAD                  ;SETUP TO CLEAR CONTROL REGISTER 2
                                JSR     PC,LDRDR2               ;GO LOAD, READ AND  CHECK REG 2
                                BEQ     1$                      ;IF LOADED OK THEN CONTINUE
                                ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL TO 0
                                TRAP    C$ERDF
                                .WORD   2
                                .WORD   0
                                .WORD   R2EROR
                                CKLOOP
                                TRAP    C$CLP1

                                ;WRITE ALL ONES INTO THE TRACE RAM ADDRESS REGISTER AND CHECK THAT ALL
                                ;ONES WERE WRITTEN. ON A WRITE  COMMAND TO CONTROL REGISTER 6, THE
                                ;SIGNAL WPT0 L WILL BE ASSERTED TO LOAD THE TRACE RAM ADDRESS REGISTER.
                                ;ON A READ COMMAND TO CONTROL REGISTER 6, THE SIGNAL RPT0 H WILL BE
                                ;ASSERTED TO READ THE TRACE RAM ADDRESS REGISTER

                        1$:     MOV     #3777,R6LOAD            ;SETUP BITS TO BE LOADED
                                MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
                                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
                                BEQ     2$                      ;IF LOADED  OK THEN CONTINUE
                                ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQL 1777
                                TRAP    C$ERDF
                                .WORD   4
                                .WORD   TRADER
                                .WORD   R026ER
                                CKLOOP
```

```
3433  007704  104406                  TRAP    C$CLP1
3434
3435                                  ;WRITE, READ AND CHECK TRACE RAM ADDRESS REGISTER WITH A DATA PATTERN
3436                                  ;OF ALL ZEROES.
3437
3438  007706  005037  002414    2$:   CLR     R6LOAD                  ;SETUP TO CLEAR TRAM ADDRESS REG
3439  007712  004737  006252          JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
3440  007716  001404                  BEQ     3$                      ;IF ALL ZEROES THEN CONTINUE
3441  007720                          ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQL 0
3442  007720  104455                  TRAP    C$ERDF
3443  007722  000004                  .WORD   4
3444  007724  002464                  .WORD   TRADER
3445  007726  004736                  .WORD   R026ER
3446  007730                  3$:     ENDSEG
3447  007730                  10000$:
3448  007730  104405                  TRAP    C$ESEG
3449  007732                          ENDTST
3450  007732                  L10032:
3451  007732  104401                  TRAP    C$ETST
```

```
                                .SBTTL  TEST 9: TRAM ADDRESS REG TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) BY
                                ; LOADING AN ALTERNATING ONES AND ZEROES PATTERN (2525) INTO THE TRACE RAM
                                ; ADDRESS REGISTER AND THEN READING AND CHECKING THE REGISTER FOR THE PATTERN
                                ; LOADED. THE TEST WILL THEN LOAD, READ AND CHECK THE TRACE RAM ADDRESS REGISTER
                                ; WITH AN ALTERNATING ZEROES AND ONES DATA PATTERN (1252).
                                ;--

007734                                  BGNTST
007734                          T9::
007734  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007740                                  BGNSEG
007740  104404                          TRAP    C$BSEG

                                ;CLEAR ALL BITS IN CONTROL REGISTER 2. CONTROL REGISTER 2 BITS PDAL3 TO
                                ;PDAL0 BEING CLEARED WILL ASSERT THE SIGNAL PTER0 L IN THE POINTER REG.

007742  005037  002376                   CLR     R2LOAD                  ;SETUP TO CLEAR CONTROL REGISTER 2
007746  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND  CHECK REG 2
007752  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007754                                  ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL TO 0
007754  104455                          TRAP    C$ERDF
007756  000002                          .WORD   2
007760  000000                          .WORD   0
007762  004706                          .WORD   R2EROR
007764                                  CKLOOP
007764  104406                          TRAP    C$CLP1

                                ;WRITE AN ALTERNATING ONES AND ZEROES DATA PATTERN (2525) INTO THE
                                ;TRACE RAM AND CHECK THAT THE DATA PATTERN CAN BE READ BACK CORECTLY.
                                ;ON A WRITE COMMAND TO CONTROL REGISTER 6, THE SIGNAL WPTO  L WILL BE
                                ;ASSERTED TO LOAD THE TRACE RAM ADDRESS REGISTER.  ON A READ COMMAND TO
                                ;CONTROL REGISTER 6, THE SIGNAL RPTO H WILL BE ASSERTED TO READ THE
                                ;TRACE RAM ADDRESS REGISTER.

007766  012737  002525  002414  1$:     MOV     #2525,R6LOAD            ;SETUP BITS TO BE LOADED
007774  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
010002  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
010006  001405                          BEQ     2$                      ;IF LOADED  OK THEN CONTINUE
010010                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQL 2525
010010  104455                          TRAP    C$ERDF
010012  000004                          .WORD   4
010014  002464                          .WORD   TRADER
010016  004736                          .WORD   R026ER
010020                                  CKLOOP
010020  104406                          TRAP    C$CLP1
```

```
3502
3503                                            ;WRITE, READ, AND CHECK TRACE RAM ADDRESS REGISTER WITH AN ALTERNATING
3504                                            ;ZEROES AND ONES DATA PATTERN (1252)
3505
3506  010022  012737  001252  002414  2$:     MOV     #1252,R6LOAD            ;SETUP BITS TO BE LOADED
3507  010030  004737  006252                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
3508  010034  001404                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
3509  010036                                    ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQL 1252
3510  010036  104455                           TRAP    C$ERDF
3511  010040  000004                           .WORD   4
3512  010042  002464                           .WORD   TRADER
3513  010044  004736                           .WORD   R026ER
3514  010046                            3$:     ENDSEG
3515  010046                            10000$:
3516  010046  104405                           TRAP    C$ESEG
3517  010050                                    ENDTST
3518  010050                            L10033:
3519  010050  104401                           TRAP    C$ETST
3520
```

```
                                .SBTTL  TEST 10: TRAM ADDRESS REG TEST USING BINARY COUNT

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0)
                                ; USING A BINARY COUNT PATTERN.  THE DATA PATTERN WILL START WITH ZERO AND
                                ; INCREMENT BY ONE UNTIL THE DATA PATTERN 3777 HAS BEEN LOADED AND CHECKED.
                                ;--

010052                                  BGNTST
010052                          T10::
010052  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
010056  005037  002414                   CLR     R6LOAD                  ;SET DATA PATTERN INITIALLY TO ZERO
010062  012737  174000  002416           MOV     #174000,R6MASK          ;SETUP MASK TO IGNORE UNUSED BITS

010070                                  BGNSEG
010070  104404                          TRAP    C$BSEG

                                        ;CLEAR ALL BITS IN CONTROL REGISTER 2. CONTROL REGISTER 2 BITS PDAL3
                                        ;TO PDAL0 BEING CLEARED WILL ASSERT THE SIGNAL PTER0 L IN THE POINTER REG.

010072  005037  002376                   CLR     R2LOAD                  ;SETUP TO CLEAR CONTROL REG 2
010076  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
010102  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010104                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL TO 0
010104  104455                          TRAP    C$ERDF
010106  000002                          .WORD   2
010110  000000                          .WORD   0
010112  004706                          .WORD   R2EROR
010114                          1$:     ENDSEG
010114                          10000$:
010114  104405                          TRAP    C$ESEG

010116                          2$:     BGNSEG
010116  104404                          TRAP    C$BSEG

                                        ;WRITE, READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH A DATA
                                        ;PATTERN FROM 0 TO 3777

010120  004737  006252                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
010124  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
010126                                  ERRDF   4,TRADER,R026ER         ;DATA ERROR LOADING TRAM ADDRESS REG
010126  104455                          TRAP    C$ERDF
010130  000004                          .WORD   4
010132  002464                          .WORD   TRADER
010134  004736                          .WORD   R026ER
010136                          3$:     ENDSEG
010136                          10001$:
010136  104405                          TRAP    C$ESEG

010140  005237  002414                   INC     R6LOAD                  ;UPDATE DATA PATTERN BY 1
010144  032737  004000  002414           BIT     #BIT11,R6LOAD           ;CHECK IF LAST PATTERN WAS 3777
010152  001761                          BEQ     2$                      ;IF NOT LOAD NEXT NUMBER AND CHECK IT
010154                                  ENDTST
010154                          L10034:
010154  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 11: ZERO TRAM ADDRESS REG WITH CDAL 0 H.

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE CLEARED WHEN
                                ; THE SIGNAL CDAL 0 H IS SET TO A ONE IN CONTROL REGISTER 0. THE TEST WILL LOAD
                                ; ALL ONES (3777) INTO THE TRACE RAM ADDRESS REGISTER AND CHECK THAT ALL ONES
                                ; WERE LOADED.  THE TEST WILL THEN SET THE SIGNAL CDAL 0 H TO A ONE IN CONTROL
                                ; REGISTER 0.  THE TEST WILL THEN READ THE TRACE RAM ADDRESS REGISTER CHECKING
                                ; IT TO BE CLEARED.  THE SIGNAL CDAL 0 H WILL BE CLEARED IN CONTROL REGISTER 0
                                ; AND THE TRACE RAM ADDRESS REGISTER WILL BE READ AGAIN TO CHECK THAT NO BITS
                                ; GOT SET AFTER CLEARING THE SIGNAL CDAL 0 H.
                                ;--

010156                                  BGNTST
010156                          T11::
010156  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
010162                                  BGNSEG
010162  104404                          TRAP    C$BSEG
                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0. THIS IS DONE TO INIT
                                        ;THE SEGMENT TO A KNOWN STATE ON SCOPE LOOPING.

010164  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOW BYTE
010170  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
010174  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010176                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
010176  104455                          TRAP    C$ERDF
010200  000001                          .WORD   1
010202  000000                          .WORD   0
010204  004606                          .WORD   R0EROR

                                        ;CLEAR ALL BITS IN CONTROL REG 2 TO ASSERT THE SIGNAL PTER0 L IN POINTER REG.

010206  005037  002376          1$:     CLR     R2LOAD                  ;SETUP TO CLEAR ALL REG 2 BITS
010212  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD,READ AND CHECK REG 2
010216  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010220                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL TO 0
010220  104455                          TRAP    C$ERDF
010222  000002                          .WORD   2
010224  000000                          .WORD   0
010226  004706                          .WORD   R2EROR

                                        ;WRITE, READ, AND CHECK TRACE RAM ADDRESS REGISTER WITH DATA PATTERN OF 3777

010230  012737  003777  002414  2$:     MOV     #3777,R6LOAD            ;SETUP BITS TO BE LOADED
010236  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP MASK TO IGNORE UNUSED BITS
010244  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
010250  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
010252                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQL 3777
010252  104455                          TRAP    C$ERDF
010254  000004                          .WORD   4
010256  002464                          .WORD   TRADER
010260  004736                          .WORD   R026ER
010262                                  CKLOOP
010262  104406                          TRAP    C$CLP1

                                        ;SET CDALO H IN CONTROL REG 0 TO CLEAR THE TRACE RAM ADDRESS REGISTER.
```

```
3632
3633  010264  112737  000001  002370  3$:     MOVB    #CDAL0,ROLOAD           ;SETUP BIT TO BE LOADED
3634  010272  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
3635  010276  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
3636  010300                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
3637  010300  104455                          TRAP    C$ERDF
3638  010302  000001                          .WORD   1
3639  010304  000000                          .WORD   0
3640  010306  004606                          .WORD   ROEROR
3641  010310                                   CKLOOP
3642  010310  104406                          TRAP    C$CLP1
3643
3644                                         ;READ TRACE RAM ADDRESS REGISTER TO CHECK THAT CDALO H ON A ONE
3645                                         ;CLEARED THE TRACE RAM ADDRESS REGISTER.
3646
3647  010312  005037  002414          4$:     CLR     R6LOAD                  ;SIMULATE A CLEAR
3648  010316  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK REG 6
3649  010322  001405                          BEQ     5$                      ;IF EQUAL TO 0 THEN CONTINUE
3650  010324                                   ERRDF   4,TRADER,R026ER         ;CDALO H FAILED TO 0 TRAM ADDRESS REG
3651  010324  104455                          TRAP    C$ERDF
3652  010326  000004                          .WORD   4
3653  010330  002464                          .WORD   TRADER
3654  010332  004736                          .WORD   R026ER
3655  010334                                   CKLOOP
3656  010334  104406                          TRAP    C$CLP1
3657
3658                                         ;CLEAR SIGNAL CDAL 0 H IN CONTROL REGISTER 0
3659
3660  010336  105037  002370          5$:     CLRB    ROLOAD                  ;SETUP TO CLEAR CDALO H BIT
3661  010342  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
3662  010346  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
3663  010350                                   ERRDF   1,,ROEROR               ;REG 0 LOW BYTE NOT EQUAL TO 0
3664  010350  104455                          TRAP    C$ERDF
3665  010352  000001                          .WORD   1
3666  010354  000000                          .WORD   0
3667  010356  004606                          .WORD   ROEROR
3668  010360                                   CKLOOP
3669  010360  104406                          TRAP    C$CLP1
3670
3671                                         ;READ TRACE RAM ADDRESS REGISTER AGAIN CHECKING THAT IT DID NOT
3672                                         ;CHANGE AFTER CLEARING THE SIGNAL CDAL 0 H.
3673
3674  010362  004737  006260          6$:     JSR     PC,READR6               ;GO READ AND CHECK REGISTER 6
3675  010366  001404                          BEQ     7$                      ;IF TRAM ADDRESS REG STILL 0 THEN CONT
3676  010370                                   ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG BITS SET AFTER CDALO H CLEARED
3677  010370  104455                          TRAP    C$ERDF
3678  010372  000004                          .WORD   4
3679  010374  002464                          .WORD   TRADER
3680  010376  004736                          .WORD   R026ER
3681  010400                           7$:     ENDSEG
3682  010400                           10000$:
3683  010400  104405                          TRAP    C$ESEG
3684  010402                                   ENDTST
3685  010402                           L10035:
3686  010402  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 12: TRAM DATA IN BUF - TRDI 15:0 (1'S, AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI15 H TO
                                ; TRDI0 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                ; RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL
                                ; ZEROES (000000).
                                ;
                                ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                ; THE PROGRAM WILL THEN SET PDAL2 AND PDAL0 IN CONTROL REGISTER 2 WHICH WILL
                                ; CAUSE THE SIGNAL PTER5 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER5 L IS ASSERTED, A
                                ; PULSE WILL BE ISSUED ON THE SIGNAL WPT5 H. THE SIGNAL WPT5 H WILL CLOCK THE
                                ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 15:0).
                                ;
                                ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL0 IN
                                ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER1 L TO BE ASSERTED IN THE
                                ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                ; THE SIGNAL PTER1 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT1 H.
                                ; THE SIGNAL RPT1 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                ; TO THE LSI-11 BUS.
                                ;--

010404                                  BGNTST
010404                          T12::
010404  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

010410                                  BGNSUB
010410                          T12.1:
010410  104402                          TRAP    C$BSUB

                                        ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                        ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                        ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                        ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 15:0
                                        ;WITH A DATA PATTERN EQUAL TO 177777.

010412  012737  177777  002414          MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
010420  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
010424  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
010426                                  ENDSUB
010426                          L10037:
010426  104403                          TRAP    C$ESUB
```

```
3736
3737  010430                                BGNSUB
3738  010430                          T12.2:
3739  010430  104402                        TRAP    C$BSUB
3740
3741                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 15:0
3742                                        ;WITH A DATA PATTERN EQUAL TO 000000.
3743
3744  010432  005037  002414                CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
3745  010436  004537  006430                JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3746  010442  000005                        .WORD   PTER5                   ;SELECT TRDI BITS 15:0
3747  010444                                ENDSUB
3748  010444                          L10040:
3749  010444  104403                        TRAP    C$ESUB
3750
3751  010446                                ENDTST
3752  010446                          L10036:
3753  010446  104401                        TRAP    C$ETST
3754
```

```
3755                                    .SBTTL  TEST 13: TRAM DATA IN BUF - TRDI 15:0 (1'S + 0'S,0'S + 1'S)
3756
3757                                    ;++
3758                                    ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI15 H TO
3759                                    ; TRDI0 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
3760                                    ; RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252)
3761                                    ; AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
3762                                    ;
3763                                    ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
3764                                    ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
3765                                    ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
3766                                    ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
3767                                    ; THE PROGRAM WILL THEN SET PDAL2 AND PDAL0 IN CONTROL REGISTER 2 WHICH WILL
3768                                    ; CAUSE THE SIGNAL PTER5 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
3769                                    ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER5 L IS ASSEPTED, A
3770                                    ; PULSE WILL BE ISSUED ON THE SIGNAL WPT5 H. THE SIGNAL WPT5 H WILL CLOCK THE
3771                                    ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 15:0).
3772                                    ;
3773                                    ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL0 IN
3774                                    ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER1 L TO BE ASSERTED IN THE
3775                                    ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
3776                                    ; THE SIGNAL PTER1 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT1 H.
3777                                    ; THE SIGNAL RPT1 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
3778                                    ; TO THE LSI-11 BUS.
3779                                    ;--
3780
3781  010450                                    BGNTST
3782  010450                            T13::
3783  010450  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
3784
3785  010454                                    BGNSUB
3786  010454                            T13.1:
3787  010454  104402                           TRAP    C$BSUB
3788
3789                                          ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
3790                                          ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
3791                                          ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
3792                                          ;TRACE RAM DATA IN BUFFERS TO BE READ.
3793
3794                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 15:0
3795                                          ;WITH A DATA PATTERN EQUAL TO 125252.
3796
3797  010456  012737  125252  002414           MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
3798  010464  004537  006430                   JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3799  010470  000005                           .WORD   PTER5                   ;SELECT TRDI BITS 15:0
3800  010472                                    ENDSUB
3801  010472                            L10042:
3802  010472  104403                           TRAP    C$ESUB
3803
```

```
3804
3805  010474                                  BGNSUB
3806  010474                          T13.2:
3807  010474  104402                          TRAP    C$BSUB
3808
3809                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 15:0
3810                                          ;WITH A DATA PATTERN EQUAL TO 052525.
3811
3812  010476  012737  052525  002414          MOV     #052525,R6LOAD          ;SETUP DATA TO BE LOADED
3813  010504  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3814  010510  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
3815  010512                                  ENDSUB
3816  010512                          L10043:
3817  010512  104403                          TRAP    C$ESUB
3818
3819  010514                                  ENDTST
3820  010514                          L10041:
3821  010514  104401                          TRAP    C$ETST
3822
```

TEST 14: TRAM DATA IN BUF - TRDI 31:16 (1'S, AND 0'S) SEQ 0080

```
3823                                    .SBTTL  TEST 14: TRAM DATA IN BUF - TRDI 31:16 (1'S, AND 0'S)
3824
3825                                    ;++
3826                                    ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI31 H TO
3827                                    ; TRDI16 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
3828                                    ; RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL
3829                                    ; ZEROES (000000).
3830                                    ;
3831                                    ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
3832                                    ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
3833                                    ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
3834                                    ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
3835                                    ; THE PROGRAM WILL THEN SET PDAL2 AND PDAL1 IN CONTROL REGISTER 2 WHICH WILL
3836                                    ; CAUSE THE SIGNAL PTER6 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
3837                                    ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER6 L IS ASSERTED, A
3838                                    ; PULSE WILL BE ISSUED ON THE SIGNAL WPT6 H. THE SIGNAL WPT6 H WILL CLOCK THE
3839                                    ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 31:16).
3840                                    ;
3841                                    ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL1 IN
3842                                    ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER2 L TO BE ASSERTED IN THE
3843                                    ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
3844                                    ; THE SIGNAL PTER2 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT2 H.
3845                                    ; THE SIGNAL RPT2 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
3846                                    ; TO THE LSI-11 BUS.
3847                                    ;--
3848
3849  010516                                    BGNTST
3850  010516                            T14::
3851  010516  004737  005476                    JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
3852
3853  010522                                    BGNSUB
3854  010522                            T14.1:
3855  010522  104402                           TRAP    C$BSUB
3856
3857                                            ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
3858                                            ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
3859                                            ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
3860                                            ;TRACE RAM DATA IN BUFFERS TO BE READ.
3861
3862                                            ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 31:16
3863                                            ;WITH A DATA PATTERN EQUAL TO 177777.
3864
3865  010524  012737  177777  002414             MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
3866  010532  004537  006430                     JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3867  010536  000006                             .WORD   PTER6                   ;SELECT TRDI BITS 31:16
3868  010540                                    ENDSUB
3869  010540                            L10045:
3870  010540  104403                           TRAP    C$ESUB
3871
```

```
3872
3873  010542                                  BGNSUB
3874  010542                          T14.2:
3875  010542  104402                          TRAP    C$BSUB
3876
3877                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 31:16
3878                                          ;WITH A DATA PATTERN EQUAL TO 000000.
3879
3880  010544  005037  002414                  CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
3881  010550  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3882  010554  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
3883  010556                                  ENDSUB
3884  010556                          L10046:
3885  010556  104403                          TRAP    C$ESUB
3886
3887  010560                                  ENDTST
3888  010560                          L10044:
3889  010560  104401                          TRAP    C$ETST
3890
```

```
                        .SBTTL  TEST 15: TRAM DATA IN BUF - TRDI 31:16 (1'S + 0'S,0'S + 1'S)

                        ;++
                        ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI31 H TO
                        ; TRDI16 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                        ; RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252)
                        ; AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
                        ;
                        ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                        ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                        ; TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                        ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                        ; THE PROGRAM WILL THEN SET PDAL2 AND PDAL1 IN CONTROL REGISTER 2 WHICH WILL
                        ; CAUSE THE SIGNAL PTER6 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                        ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER6 L IS ASSERTED, A
                        ; PULSE WILL BE ISSUED ON THE SIGNAL WPT6 H. THE SIGNAL WPT6 H WILL CLOCK THE
                        ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 31:16).
                        ;
                        ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL1 IN
                        ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER2 L TO BE ASSERTED IN THE
                        ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                        ; THE SIGNAL PTER2 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT2 H.
                        ; THE SIGNAL RPT2 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                        ; TO THE LSI-11 BUS.
                        ;--

                                BGNTST
                        T15::
                                JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                BGNSUB
                        T15.1:
                                TRAP    C$BSUB

                                ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                ;THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 31:16
                                ;WITH A DATA PATTERN EQUAL TO 125252.

                                MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
                                JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
                                .WORD   PTER6                   ;SELECT TRDI BITS 31:16
                                ENDSUB
                        L10050:
                                TRAP    C$ESUB
```

```
3941
3942  010606                                  BGNSUB
3943  010606                            T15.2:
3944  010606  104402                          TRAP    C$BSUB
3945
3946                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 31:16
3947                                          ;WITH A DATA PATTERN EQUAL TO 052525.
3948
3949  010610  012737  052525  002414          MOV     #052525,R6LOAD          ;SETUP DATA TO BE LOADED
3950  010616  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3951  010622  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
3952  010624                                  ENDSUB
3953  010624                            L10051:
3954  010624  104403                          TRAP    C$ESUB
3955
3956  010626                                  ENDTST
3957  010626                            L10047:
3958  010626  104401                          TRAP    C$ETST
3959
```

```
                                .SBTTL  TEST 16: TRAM DATA IN BUF - TRDI 47:32 (1'S, AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI47 H TO
                                ; TRDI32 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                ; RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL
                                ; ZEROES (000000).
                                ;
                                ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                ; THE PROGRAM WILL THEN SET PDAL2,PDAL1 AND PDAL0 IN CONTROL REGISTER 2 WHICH WILL
                                ; CAUSE THE SIGNAL PTER7 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER7 L IS ASSERTED, A
                                ; PULSE WILL BE ISSUED ON THE SIGNAL WPT7 H. THE SIGNAL WPT7 H WILL CLOCK THE
                                ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 47:32).
                                ;
                                ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET PDAL1 AND PDAL0 IN
                                ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER3 L TO BE ASSERTED IN THE
                                ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                ; THE SIGNAL PTER3 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT3 H.
                                ; THE SIGNAL RPT3 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                ; TO THE LSI-11 BUS.
                                ;--

010630                                  BGNTST
010630                          T16::
010630  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

010634                                  BGNSUB
010634                          T16.1:
010634  104402                          TRAP    C$BSUB

                                ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                ;THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 47:32
                                ;WITH A DATA PATTERN EQUAL TO 177777.

010636  012737  177777  002414          MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
010644  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
010650  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
010652                                  ENDSUB
010652                          L10053:
010652  104403                          TRAP    C$ESUB
```

```
4009
4010  010654                                  BGNSUB
4011  010654                            T16.2:
4012  010654  104402                          TRAP    C$BSUB
4013
4014                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 47:32
4015                                          ;WITH A DATA PATTERN EQUAL TO 0C0000.
4016
4017  010656  005037  002414                  CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
4018  010662  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4019  010666  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
4020  010670                                  ENDSUB
4021  010670                            L10054:
4022  010670  104403                          TRAP    C$ESUB
4023
4024  010672                                  ENDTST
4025  010672                            L10052:
4026  010672  104401                          TRAP    C$ETST
4027
```

```
                                        .SBTTL  TEST 17: TRAM DATA IN BUF - TRDI 47:32 (1'S + 0'S,0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI47 H TO
                                        ; TRDI32 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                        ; RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252)
                                        ; AND THEN AND ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
                                        ;
                                        ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                        ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                        ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                        ; THE PROGRAM WILL THEN SET PDAL2,PDAL1 AND PDAL0 IN CONTROL REGISTER 2 WHICH WILL
                                        ; CAUSE THE SIGNAL PTER7 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                        ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER7 L IS ASSERTED, A
                                        ; PULSE WILL BE ISSUED ON THE SIGNAL WPT7 H. THE SIGNAL WPT7 H WILL CLOCK THE
                                        ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 47:32).
                                        ;
                                        ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET PDAL1 AND PDAL0 IN
                                        ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER3 L TO BE ASSERTED IN THE
                                        ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                        ; THE SIGNAL PTER3 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT3 H.
                                        ; THE SIGNAL RPT3 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                        ; TO THE LSI-11 BUS.
                                        ;--

010674                                          BGNTST
010674                                  T17::
010674  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

010700                                          BGNSUB
010700                                  T17.1:
010700  104402                                  TRAP    C$BSUB

                                        ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                        ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                        ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                        ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 47:32
                                        ;WITH A DATA PATTERN EQUAL TO 125252.

010702  012737  125252  002414                  MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
010710  004537  006430                          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
010714  000007                                  .WORD   PTER7                   ;SELECT TRDI BITS 47:32
010716                                          ENDSUB
010716                                  L10056:
010716  104403                                  TRAP    C$ESUB
```

```
4077
4078  010720                                    BGNSUB
4079  010720                              T17.2:
4080  010720  104402                            TRAP    C$BSUB
4081
4082                                            ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 47:32
4083                                            ;WITH A DATA PATTERN EQUAL TO 052525.
4084
4085  010722  012737  052525  002414            MOV     #052525,R6LOAD          ;SETUP DATA TO BE LOADED
4086  010730  004537  006430                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4087  010734  000007                            .WORD   PTER7                   ;SELECT TRDI BITS 47:32
4088  010736                                    ENDSUB
4089  010736                              L10057:
4090  010736  104403                            TRAP    C$ESUB
4091
4092  010740                                    ENDTST
4093  010740                              L10055:
4094  010740  104401                            TRAP    C$ETST
4095
```

```
                                .SBTTL  TEST 18: TRAM DATA IN BUF - TRDI 59:48 (1'S, AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI59 H TO
                                ; TRDI48 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                ; RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (007777) AND THEN ALL
                                ; ZEROES (000000).
                                ;
                                ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                ; THE PROGRAM WILL THEN SET PDAL3 IN CONTROL REGISTER 2 WHICH WILL
                                ; CAUSE THE SIGNAL PTER8 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER8 L IS ASSERTED, A
                                ; PULSE WILL BE ISSUED ON THE SIGNAL WPT8 H. THE SIGNAL WPT8 H WILL CLOCK THE
                                ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 59:48).
                                ;
                                ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL2 IN
                                ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER4 L TO BE ASSERTED IN THE
                                ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                ; THE SIGNAL PTER4 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT4 H.
                                ; THE SIGNAL RPT4 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                ; TO THE LSI-11 BUS.
                                ;--

010742                                  BGNTST
010742                          T18::
010742  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

010746                                  BGNSUB
010746                          T18.1:
010746  104402                          TRAP    C$BSUB

                                ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 59:48
                                ;WITH A DATA PATTERN EQUAL TO 007777.

010750  012737  007777  002414          MOV     #007777,R6LOAD          ;SETUP DATA TO BE LOADED
010756  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
010762  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
010764                                  ENDSUB
010764                          L10061:
010764  104403                          TRAP    C$ESUB
```

```
4145
4146  010766                                  BGNSUB
4147  010766                            T18.2:
4148  010766  104402                          TRAP    C$BSUB
4149
4150                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 59:48
4151                                          ;WITH A DATA PATTERN EQUAL TO 000000.
4152
4153  010770  005037  002414                  CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
4154  010774  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4155  011000  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
4156  011002                                  ENDSUB
4157  011002                            L10062:
4158  011002  104403                          TRAP    C$ESUB
4159
4160  011004                                  ENDTST
4161  011004                            L10060:
4162  011004  104401                          TRAP    C$ETST
4163
```

```
                                .SBTTL  TEST 19: TRAM DATA IN BUF - TRDI 59:48 (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI59 H TO
                                ; TRDI48 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                ; RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (005252),
                                ; AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (002525).
                                ;
                                ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                ; THE PROGRAM WILL THEN SET PDAL3 IN CONTROL REGISTER 2 WHICH WILL
                                ; CAUSE THE SIGNAL PTER8 ' TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER8 L IS ASSERTED, A
                                ; PULSE WILL BE ISSUED ON THE SIGNAL WPT8 H. THE SIGNAL WPT8 H WILL CLOCK THE
                                ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 59:48).
                                ;
                                ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL2 IN
                                ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER4 L TO BE ASSERTED IN THE
                                ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                ; THE SIGNAL PTER4 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT4 H.
                                ; THE SIGNAL RPT4 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                ; TO THE LSI-11 BUS.
                                ;--

011006                                  BGNTST
011006                          T19.:
011006  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

011012                                  BGNSUB
011012                          T19.1:
011012  104402                          TRAP    C$BSUB

                                ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 59:48
                                ;WITH A DATA PATTERN EQUAL TO 005252.

011014  012737  005252  002414          MOV     #005252,R6LOAD          ;SETUP DATA TO BE LOADED
011022  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
011026  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
011030                                  ENDSUB
011030                          L10064:
011030  104403                          TRAP    C$ESUB
```

```
4213
4214  011032                                    BGNSUB
4215  011032                              T19.2:
4216  011032  104402                            TRAP    C$BSUB
4217
4218                                            ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 59:48
4219                                            ;WITH A DATA PATTERN EQUAL TO 002525.
4220
4221  011034  012737  002525  002414            MOV     #002525,R6LOAD          ;SETUP DATA TO BE LOADED
4222  011042  004537  006430                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4223  011046  000010                            .WORD   PTER8                   ;SELECT TRDI BITS 59:48
4224  011050                                    ENDSUB
4225  011050                              L10065:
4226  011050  104403                            TRAP    C$ESUB
4227
4228  011052                                    ENDTST
4229  011052                              L10063:
4230  011052  104401                            TRAP    C$ETST
4231
```

```
                        .SBTTL  TEST 20: TRAM DATA IN BUF SELECTION TEST

                        ;++
                        ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER FROM THE LSI-11 BUS TO
                        ; BE SELECTED CORRECTLY BY THE POINTER REGISTER.  THE TEST WILL WRITE AND
                        ; CHECK TPDI BITS 15:0 WITH A DATA PATTERN EQUAL TO 1, TRDI BITS 31:16 WITH
                        ; A DATA PATTERN EQUAL TO 2, TRDI BITS 47:32 WITH A DATA PATTERN EQUAL TO
                        ; 3, AND TRDI BITS 59:32 WITH A DATA PATTERN EQUAL TO 4.  THE TEST WILL THEN
                        ; READ EACH SET OF TRDI BITS CHECKING THE DATA PATTERN TO BE THAT WHICH WAS
                        ; WRITTEN PREVIOUSLY IN THIS TEST.
                        ;--

011054                          BGNTST
011054                  T20::
011054  004737  005476          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

011060  012701  000005          MOV     #PTER5,R1               ;SETUP WORKING WRITE POINTER
011064  012702  000001          MOV     #PTER1,R2               ;SETUP WORKING READ POINTER
011070  012703  000001          MOV     #1,R3                   ;SETUP INITIAL DATA PATTERN
011074  005037  002416          CLR     R6MASK                  ;CLEAR MASK WORD TO READ ALL BITS

011100                  1$:     BGNSEG
011100  104404                  TRAP    C$BSEG

                        ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO
                        ;THIS CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 BEING CLEARED
                        ;WILL CAUSE THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE
                        ;OUTPUTS OF THE TRACE RAM DATA IN BUFFERS TO BE READ.

                        ;LOAD PDAL BITS 3-0 TO SELECT POINTER REGISTER SIGNALS PTER5, PTER6,
                        ;PTER7 OR PTER8.

011102  010137  002376          MOV     R1,R2LOAD               ;SETUP TO LOAD POINTER REGISTER
011106  004737  006136          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHEKC REG 2
011112  001405                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011114                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
011114  104455                  TRAP    C$ERDF
011116  000002                  .WORD   2
011120  000000                  .WORD   0
011122  004706                  .WORD   R2EROR
011124                          CKLOOP
011124  104406                  TRAP    C$CLP1

                        ;LOAD DATA PATTERN OF 1 INTO TRDI BITS 15:0
                        ;LOAD DATA PATTERN OF 2 INTO TRDI BITS 31:16
                        ;LOAD DATA PATTERN OF 3 INTO TRDI BITS 47:32
                        ;LOAD DATA PATTERN OF 4 INTO TRDI BITS 59:48

011126  010337  002414  2$:     MOV     R3,R6LOAD               ;SETUP DATA TO BE LOADED
011132  010377  171220          MOV     R3,@REG6                ;WRITE DATA INTO TRAM DATA IN BUF

                        ;LOAD PDAL BITS 2-0 TO SELECT POINTER REGISTER PTER1, PTER2, PTER3,
                        ;OR PTER4.

011136  010237  002376          MOV     R2,R2LOAD               ;SETUP BITS TO BE LOADED
011142  004737  006136          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
```

```
4288  011146  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4289  011150                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
4290  011150  104455                          TRAP    C$ERDF
4291  011152  000002                          .WORD   2
4292  011154  000000                          .WORD   0
4293  011156  004706                          .WORD   R2EROR
4294  011160                                  CKLOOP
4295  011160  104406                          TRAP    C$CLP1
4296
4297                                          ;READ DATA PATTERN OF 1 FROM TRDI 15:0
4298                                          ;READ DATA PATTERN OF 2 FROM TRDI 31:16
4299                                          ;READ DATA PATTERN OF 3 FROM TRDI 47:32
4300                                          ;READ DATA PATTERN OF 4 FROM TRDI 59:48
4301
4302  011162  017737  171170  002420  3$:     MOV     @REG6,R6READ            ;READ DATA PATTERN FROM TRDI BITS
4303  011170  043737  002416  002420          BIC     R6MASK,R6READ           ;CLEAR UNUSED BITS IF ANY
4304  011176  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
4305  011204  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
4306  011206                                  ERRDF   4,TRDIER,R026ER         ;TRAM DATA IN BUF DATA ERROR
4307  011206  104455                          TRAP    C$ERDF
4308  011210  000004                          .WORD   4
4309  011212  002710                          .WORD   TRDIER
4310  011214  004736                          .WORD   R026ER
4311  011216                          4$:     ENDSEG
4312  011216                          10000$:
4313  011216  104405                          TRAP    C$ESEG
4314
4315  011220  005201                          INC     R1                      ;UPDATE WORKING WRITE POINTER
4316  011222  005202                          INC     R2                      ;UPDATE WORKING READ POINTER
4317  011224  005203                          INC     R3                      ;UPDATE DATA PATTERN
4318  011226  022703  000004                  CMP     #4,R3                   ;CHECK IF TRDI BITS 59:48
4319  011232  001004                          BNE     5$                      ;IF NOT CHECK IF DONE
4320  011234  012737  170000  002416          MOV     #170000,R6MASK          ;SETUP TO IGNORE TOP 4 BITS
4321  011242  000716                          BR      1$                      ;GO DO LAST REGISTER
4322  011244  022703  000005          5$:     CMP     #5,R3                   ;CHECK IF DONE
4323  011250  001313                          BNE     1$                      ;IF NOT GO LOAD NEXT PATTERN
4324
4325  011252  012702  000001                  MOV     #PTER1,R2               ;RESET WORKING READ POINTER
4326  011256  012703  000001                  MOV     #1,R3                   ;RESET DATA PATTERN TO 1
4327  011262  005037  002416                  CLR     R6MASK                  ;CLEAR REGISTER 6 MASK WORD
4328
4329  011266                          6$:     BGNSEG
4330  011266  104404                          TRAP    C$BSEG
4331
4332                                          ;LOAD PDAL BITS 2-0 TO SELECT PTER1, PTER2, PTER3, OR PTER4.
4333
4334  011270  010237  002376                  MOV     R2,R2LOAD               ;SETUP BITS TO BE LOADED
4335  011274  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
4336  011300  001405                          BEQ     7$                      ;IF LOADED OK THEN CONINUE
4337  011302                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
4338  011302  104455                          TRAP    C$ERDF
4339  011304  000002                          .WORD   2
4340  011306  000000                          .WORD   0
4341  011310  004706                          .WORD   R2EROR
4342  011312                                  CKLOOP
4343  011312  104406                          TRAP    C$CLP1
```

```
                                                ;READ DATA PATTERN OF 1 FROM TRDI BITS 15:0
                                                ;READ DATA PATTERN OF 2 FROM TRDI BITS 31:16
                                                ;READ DATA PATTERN OF 3 FROM TRDI BITS 47:32
                                                ;READ DATA PATTERN OF 4 FROM TRDI BITS 59:48

011314  010337  002414          7$:     MOV     R3,R6LOAD               ;SETUP DATA PREVIOUSLY LOADED
011320  017737  171032  002420          MOV     @REG6,R6READ            ;READ DATA FROM TRDI BITS
011326  043737  002416  002420          BIC     R6MASK,R6READ           ;CLEAR UNUSED BITS IF ANY
011334  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
011342  001404                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
011344                                  ERRDF   4,TRDISE,R026ER         ;TRAM DATA IN BUF SELECTION ERROR
011344  104455                          TRAP    C$ERDF
011346  000004                          .WORD   4
011350  002745                          .WORD   TRDISE
011352  004736                          .WORD   R026ER
011354                          8$:     ENDSEG
011354                          10001$:
011354  104405                          TRAP    C$ESEG

011356  005202                          INC     R2                      ;UPDATE WORKING READ POINTER
011360  005203                          INC     R3                      ;UPDATE DATA PATTERN
011362  022703  000004                  CMP     #4,R3                   ;CHECK IF LAST REGISTER
011366  001004                          BNE     9$                      ;IF NOT CHECK IF DONE
011370  012737  170000  002416          MOV     #170000,R6MASK          ;SETUP MASK WORD TO IGNORE UNUSED BITS
011376  000733                          BR      6$                      ;GO DO LAST REGISTER
011400  022703  000005          9$:     CMP     #5,R3                   ;CHECK IF DONE
011404  001330                          BNE     6$                      ;IF NOT THEN LOAD NEXT REGISTER
011406                                  ENDTST
011406                          L10066:
011406  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 21: TRAM DATA TEST - TRDI 15:0 (125252-052525)

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM BITS TRDI 15:0 WITH A DATA PATTERN OF 125252
                                ; AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED FOR THIS DATA
                                ; PATTERN BEFORE THE NEXT SEQUENTIAL LOCATION IS CHECKED.
                                ;
                                ; THIS TEST IS PERFORMED IN THE FOLLOWING MANNER:
                                ;    1.  CLEAR LOW BYTE OF CONTROL REGISTER 0 TO SET SIGNAL TRSLO L
                                ;    2.  SET PTER0 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    3.  WRITE AND READ TRAM ADDRESS REG VIA SIGNALS WPT0 L AND RPT0 H
                                ;    4.  SET PTER5 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    5.  WRITE DATA PATTERN (125252-052525) INTO TRAM DATA IN BUF BITS TRDI 15:0
                                ;        VIA WPT5 H AND WRITE TO CONTROL REGISTER 6.
                                ;    6.  SET PTER1 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    7.  READ DATA PATTERN FROM TRAM DATA IN BUFFER VIA RPT1 H AND READ TO REG 6
                                ;    8.  WRITE TRACE RAM VIA WPT1 H AND WRITE TO CONTROL REGISTER 6
                                ;    9.  SET SIGNAL TRSL1 L BY SETTING CDAL2 = 1 IN REGISTER 0
                                ;   10.  READ TRACE RAM VIA RPT1 H AND READ TO CONTROL REGISTER 6
                                ;   11.  COMPLEMENT DATA PATTERN - REPEAT STEPS 1-10 WITH THIS PATTERN
                                ;   12.  RESET DATA PATTERN TO 125252 - INCREMENT ADDRESS BY 1
                                ;   13.  REPEAT STEPS 1-12 UNTIL ALL OF THE 1K ADDRESS HAVE BEEN CHECKED.
                                ;--

                                    BGNTST
                                T21::
011410  004737  005476              JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
011414  005037  006376              CLR     TRADRS                  ;SET TRACE RAM ADDRESS TO ZERO
011420  012701  125252              MOV     #125252,R1              ;SETUP STARTING DATA PATTERN

011424                          1$: BGNSEG
011424  104404                      TRAP    C$BSEG

                                    ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING ZERO
                                    ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE
                                    ;TRACE RAM DATA IN BUFFERS

011426  105037  002370              CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
011432  004737  006104              JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
011436  001405                      BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011440                              ERRDF   1,,R0EROR               ;REGISTER 0 LOW BYTE NOT 0
011440  104455                      TRAP    C$ERDF
011442  000001                      .WORD   1
011444  000000                      .WORD   0
011446  004606                      .WORD   R0EROR
011450                              CKLOOP
011450  104406                      TRAP    C$CLP1

                                    ;LOAD TRACE RAM ADDRESS REGISTER WITH CONTENTS OF LOCATION "TRADRS"

011452  004737  006312          2$: JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0 WITH A DATA
                                    ;PATTERN OF 125252 OR 052525.

011456  010137  002414              MOV     R1,R6LOAD               ;SETUP DATA PATTERN TO BE LOADED
```

```
4432  011462  004537  006430                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4433  011466  000005                            .WORD   PTER5                   ;SELECT TRDI BITS 15:0
4434
4435                                            ;WRITE THE TRACE RAM LOCATION ADDRESSED BY TRACE RAM ADDRESS REGISTER
4436                                            ;WITH THE DATA PATTERN STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 15:0.
4437
4438  011470  012777  000000  170660            MOV     #0,@REG6                ;WRITE THE RAM FROM DATA IN BUFFERS
4439
4440                                            ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
4441                                            ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
4442                                            ;BITS TRDI 15:0 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
4443                                            ;THE SIGNAL RPT1 H.
4444
4445  011476  052737  000004  002370            BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
4446  011504  004737  006104                    JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
4447  011510  001405                            BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4448  011512                                    ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
4449  011512  104455                            TRAP    C$ERDF
4450  011514  000001                            .WORD   1
4451  011516  000000                            .WORD   0
4452  011520  004606                            .WORD   ROEROR
4453  011522                                    CKLOOP
4454  011522  104406                            TRAP    C$CLP1
4455
4456                                            ;READ DATA FROM TRACE RAM BITS TRDI 15:0
4457
4458  011524  017737  170626  002420  3$:       MOV     @REG6,R6READ            ;READ DATA FROM THE RAM
4459  011532  023737  002414  002420            CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED INTO TRACE RAM
4460                                                                            ;DATA IN BUFFERS TRDI 15:0 WITH DATA
4461                                                                            ;READ FROM THE TRACE RAM
4462  011540  001404                                    BEQ     4$              ;IF DATA THE SAME THEN CONTINUE
4463  011542                                            ERRDF   4,TRAM15,TRAMER ;TRAM DATA ERROR TRDI 15:0
4464  011542  104455                                    TRAP    C$ERDF
4465  011544  000004                                    .WORD   4
4466  011546  003000                                    .WORD   TRAM15
4467  011550  004766                                    .WORD   TRAMER
4468  011552                                    4$:     ENDSEG
4469  011552                                    10000$:
4470  011552  104405                                    TRAP    C$ESEG
4471
4472  011554  005701                                    TST     R1              ;CHECK DATA PATTERN TO SEE IF DONE
4473  011556  100002                                    BPL     5$              ;IF DONE THEN UPDATE TO NEXT ADDRESS
4474  011560  005101                                    COM     R1              ;MAKE PATTERN 052525
4475  011562  000720                                    BR      1$              ;GO DO THIS PATTERN
4476  011564  005101                            5$:     COM     R1              ;MAKE DATA PATTERN 125252
4477  011566  005237  006376                            INC     TRADRS          ;UPDATE TO NEXT SEQUENTIAL ADDRESS
4478  011572  032737  002000  006376                    BIT     #BIT10,TRADRS   ;CHECK IF ALL 1K ADDRESSES DONE
4479  011600  001711                                    BEQ     1$              ;IF NOT THEN DO NEXT ADDRESS
4480  011602                                            ENDTST
4481  011602                                    L10067:
4482  011602  104401                                    TRAP    C$ETST
```

```
                                .SBTTL  TEST 22: TRAM DATA TEST - TRDI 31:16 (125252-052525)

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM BITS TRDI 31:16 WITH A DATA PATTERN OF 125252
                                ; AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED FOR THIS DATA
                                ; PATTERN BEFORE THE NEXT SEQUENTIAL LOCATION IS CHECKED.
                                ;
                                ; THIS TEST IS PERFORMED IN THE FOLLOWING MANNER:
                                ;    1.  CLEAR LOW BYTE OF CONTROL REGISTER 0 TO SET SIGNAL TRSLO L
                                ;    2.  SET PTER0 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    3.  WRITE AND READ TRAM ADDRESS REG VIA SIGNALS WPT0 L AND RPT0 H
                                ;    4.  SET PTER6 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    5.  WRITE DATA PATTERN (125252-052525) INTO TRAM DATA IN BUF BITS TRDI 31:16
                                ;        VIA WPT6 H AND WRITE TO CONTROL REGISTER 6.
                                ;    6.  SET PTER2 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    7.  READ DATA PATTERN FROM TRAM DATA IN BUFFER VIA RPT2 H AND READ TO REG 6
                                ;    8.  WRITE TRACE RAM VIA WPT2 H AND WRITE TO CONTROL REGISTER 6
                                ;    9.  SET SIGNAL TRSL1 L BY SETTING CDAL2 = 1 IN REGISTER 0
                                ;   10.  READ TRACE RAM VIA RPT2 H AND READ TO CONTROL REGISTER 6
                                ;   11.  COMPLEMENT DATA PATTERN - REPEAT STEPS 1-10 WITH THIS PATTERN
                                ;   12.  RESET DATA PATTERN TO 125252 - INCREMENT ADDRESS BY 1
                                ;   13.  REPEAT STEPS 1-12 UNTIL ALL OF THE 1K ADDRESS HAVE BEEN CHECKED.
                                ;--

011604                                  BGNTST
011604                          T22::
011604  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
011610  005037  006376                  CLR     TRADRS                  ;SET TRACE RAM ADDRESS TO ZERO
011614  012701  125252                  MOV     #125252,R1              ;SETUP STARTING DATA PATTERN

011620                          1$:     BGNSEG
011620  104404                          TRAP    C$BSEG

                                ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING ZERO
                                ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE
                                ;TRACE RAM DATA IN BUFFERS

011622  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
011626  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
011632  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011634                                  ERRDF   1,,R0EROR               ;REGISTER 0 LOW BYTE NOT 0
011634  104455                          TRAP    C$ERDF
011636  000001                          .WORD   1
011640  000000                          .WORD   0
011642  004606                          .WORD   R0EROR
011644                                  CKLOOP
011644  104406                          TRAP    C$CLP1

                                ;LOAD TRACE RAM ADDRESS REGISTER WITH CONTENTS OF LOCATION "TRADRS"

011646  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 31:16 WITH A DATA
                                ;PATTERN OF 125252 OR 052525.

011652  010137  002414                  MOV     R1,R6LOAD               ;SETUP DATA PATTERN TO BE LOADED
```

```
4539  011656  004537  006430                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4540  011662  000006                            .WORD   PTER6                   ;SELECT TRDI BITS 31:16
4541
4542                                            ;WRITE THE TRACE RAM LOCATION ADDRESSED BY TRACE RAM ADDRESS REGISTER
4543                                            ;WITH THE DATA PATTERN STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 31:16.
4544
4545  011664  012777  000000  170464            MOV     #0,@REG6                ;WRITE THE RAM FROM DATA IN BUFFERS
4546
4547                                            ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
4548                                            ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
4549                                            ;BITS TRDI 31:16 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
4550                                            ;THE SIGNAL RPT2 H.
4551
4552  011672  052737  000004  002370            BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
4553  011700  004737  006104                    JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
4554  011704  001405                            BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4555  011706                                    ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
4556  011706  104455                            TRAP    C$ERDF
4557  011710  000001                            .WORD   1
4558  011712  000000                            .WORD   0
4559  011714  004606                            .WORD   ROEROR
4560  011716                                    CKLOOP
4561  011716  104406                            TRAP    C$CLP1
4562
4563                                            ;READ DATA FROM TRACE RAM BITS TRDI 31:16
4564
4565  011720  017737  170432  002420  3$:       MOV     @REG6,R6READ            ;READ DATA FROM THE RAM
4566  011726  023737  002414  002420            CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED INTO TRACE RAM
4567                                                                            ;DATA IN BUFFERS TRDI 31:16 WITH DATA
4568                                                                            ;READ FROM THE TRACE RAM
4569  011734  001404                                    BEQ     4$              ;IF DATA THE SAME THEN CONTINUE
4570  011736                                            ERRDF   4,TRAM31,TRAMER ;TRAM DATA ERROR TRDI 31:16
4571  011736  104455                                    TRAP    C$ERDF
4572  011740  000004                                    .WORD   4
4573  011742  003034                                    .WORD   TRAM31
4574  011744  004766                                    .WORD   TRAMER
4575  011746                                    4$:     ENDSEG
4576  011746                                    10000$:
4577  011746  104405                                    TRAP    C$ESEG
4578
4579  011750  005701                                    TST     R1              ;CHECK DATA PATTERN TO SEE IF DONE
4580  011752  100002                                    BPL     5$              ;IF DONE THEN UPDATE TO NEXT ADDRESS
4581  011754  005101                                    COM     R1              ;MAKE PATTERN 052525
4582  011756  000720                                    BR      1$              ;GO DO THIS PATTERN
4583  011760  005101                            5$:     COM     R1              ;MAKE DATA PATTERN 125252
4584  011762  005237  006376                            INC     TRADRS          ;UPDATE TO NEXT SEQUENTIAL ADDRESS
4585  011766  032737  002000  006376                    BIT     #BIT10,TRADRS   ;CHECK IF ALL 1K ADDRESSES DONE
4586  011774  001711                                    BEQ     1$              ;IF NOT THEN DO NEXT ADDRESS
4587  011776                                            ENDTST
4588  011776                                    L10070:
4589  011776  104401                                    TRAP    C$ETST
```

```
                                .SBTTL  TEST 23: TRAM DATA TEST - TRDI 47:32 (125252-052525)

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM BITS TRDI 47:32 WITH A DATA PATTERN OF 125252
                                ; AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED FOR THIS DATA
                                ; PATTERN BEFORE THE NEXT SEQUENTIAL LOCATION IS CHECKED.
                                ;
                                ; THIS TEST IS PERFORMED IN THE FOLLOWING MANNER:
                                ;    1.  CLEAR LOW BYTE OF CONTROL REGISTER 0 TO SET SIGNAL TRSLO L
                                ;    2.  SET PTER0 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    3.  WRITE AND READ TRAM ADDRESS REG VIA SIGNALS WPT0 L AND RPT0 H
                                ;    4.  SET PTER7 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    5.  WRITE DATA PATTERN (125252-052525) INTO TRAM DATA IN BUF BITS TRDI 47:32
                                ;        VIA WPT7 H AND WRITE TO CONTROL REGISTER 6.
                                ;    6.  SET PTER3 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    7.  READ DATA PATTERN FROM TRAM DATA IN BUFFER VIA RPT3 H AND READ TO REG 6
                                ;    8.  WRITE TRACE RAM VIA WPT3 H AND WRITE TO CONTROL REGISTER 6
                                ;    9.  SET SIGNAL TRSL1 L BY SETTING CDAL2 = 1 IN REGISTER 0
                                ;   10.  READ TRACE RAM VIA RPT3 H AND READ TO CONTROL REGISTER 6
                                ;   11.  COMPLEMENT DATA PATTERN - REPEAT STEPS 1-10 WITH THIS PATTERN
                                ;   12.  RESET DATA PATTERN TO 125252 - INCREMENT ADDRESS BY 1
                                ;   13.  REPEAT STEPS 1-12 UNTIL ALL OF THE 1K ADDRESS HAVE BEEN CHECKED.
                                ;--

012000                                  BGNTST
012000                          T23::
012000  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
012004  005037  006376                  CLR     TRADRS                  ;SET TRACE RAM ADDRESS TO ZERO
012010  012701  125252                  MOV     #125252,R1              ;SETUP STARTING DATA PATTERN

012014                          1$:     BGNSEG
012014  104404                          TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING ZERO
                                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE
                                        ;TRACE RAM DATA IN BUFFERS

012016  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
012022  004737  006104                  JSR     PC,LDRDRO               ;GO LOAD,READ AND CHECK REGISTER 0
012026  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012030                                  ERRDF   1,,ROEROR               ;REGISTER 0 LOW BYTE NOT 0
012030  104455                          TRAP    C$ERDF
012032  000001                          .WORD   1
012034  000000                          .WORD   0
012036  004606                          .WORD   ROEROR
012040                                  CKLOOP
012040  104406                          TRAP    C$CLP1

                                        ;LOAD TRACE RAM ADDRESS REGISTER WITH CONTENTS OF LOCATION "TRADRS"

012042  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 47:32 WITH A DATA
                                        ;PATTERN OF 125252 OR 052525.

012046  010137  002414                  MOV     R1,R6LOAD               ;SETUP DATA PATTERN TO BE LOADED
```

```
 4646  012052  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
 4647  012056  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
 4648
 4649                                          ;WRITE THE TRACE RAM LOCATION ADDRESSED BY TRACE RAM ADDRESS REGISTER
 4650                                          ;WITH THE DATA PATTERN STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 47:32.
 4651
 4652  012060  012777  000000  170270          MOV     #0,@REG6                ;WRITE THE RAM FROM DATA IN BUFFERS
 4653
 4654                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
 4655                                          ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
 4656                                          ;BITS TRDI 47:32 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
 4657                                          ;THE SIGNAL RPT3 H.
 4658
 4659  012066  052737  000004  002370          BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
 4660  012074  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
 4661  012100  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
 4662  012102                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
 4663  012102  104455                          TRAP    C$ERDF
 4664  012104  000001                          .WORD   1
 4665  012106  000000                          .WORD   0
 4666  012110  004606                          .WORD   ROEROR
 4667  012112                                  CKLOOP
 4668  012112  104406                          TRAP    C$CLP1
 4669
 4670                                          ;READ DATA FROM TRACE RAM BITS TRDI 47:32
 4671
 4672  012114  017737  170236  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM THE RAM
 4673  012122  023737  002414  002420          CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED INTO TRACE RAM
 4674                                                                          ;DATA IN BUFFERS TRDI 47:32 WITH DATA
 4675                                                                          ;READ FROM THE TRACE RAM
 4676  012130  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
 4677  012132                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR TRDI 47:32
 4678  012132  104455                          TRAP    C$ERDF
 4679  012134  000004                          .WORD   4
 4680  012136  003071                          .WORD   TRAM47
 4681  012140  004766                          .WORD   TRAMER
 4682  012142                          4$:     ENDSEG
 4683  012142                          10000$:
 4684  012142  104405                          TRAP    C$ESEG
 4685
 4686  012144  005701                          TST     R1                      ;CHECK DATA PATTERN TO SEE IF DONE
 4687  012146  100002                          BPL     5$                      ;IF DONE THEN UPDATE TO NEXT ADDRESS
 4688  012150  005101                          COM     R1                      ;MAKE PATTERN 052525
 4689  012152  000720                          BR      1$                      ;GO DO THIS PATTERN
 4690  012154  005101                  5$:     COM     R1                      ;MAKE DATA PATTERN 125252
 4691  012156  005237  006376                  INC     TRADRS                  ;UPDATE TO NEXT SEQUENTIAL ADDRESS
 4692  012162  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES DONE
 4693  012170  001711                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
 4694  012172                                  ENDTST
 4695  012172                          L10071:
 4696  012172  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 24: TRAM DATA TEST - TRDI 55:48 (252-525)

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM BITS TRDI 55:48 WITH A DATA PATTERN OF 252
                                ; AND 525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED WITH THESE DATA
                                ; PATTERNS BEFORE THE NEXT LOCATION IS CHECKED. WHEN LOADING THE TRACE RAM
                                ; DATA IN BUFFER BITS TRDI 59:48, THE FOLLOWING DATA PATTERN WILL BE LOADED
                                ; INTO TRDI BITS 59:48, 5252 AND 2525. WHEN DATA IS CLOCKED FROM THE TRACE
                                ; RAM DATA IN BUFFER TO THE TRACE RAM, ONLY TRDI BITS 55:48 ARE LOADED INTO THE
                                ; TRACE RAM. THERE IS NO TRACE RAM FOR BITS TRDI 59:56.
                                ; THIS TEST IS PERFORMED IN THE FOLLOWING MANNER:
                                ;    1.  CLEAR LOW BYTE OF CONTROL REGISTER 0 TO SET SIGNAL TRSLO L
                                ;    2.  SET PTER0 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    3.  WRITE AND READ TRAM ADDRESS REG VIA SIGNALS WPTO L AND RPTO H
                                ;    4.  SET PTER8 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    5.  WRITE DATA PATTERN (5252-2525) INTO TRAM DATA IN BUF BITS TRDI 59:48
                                ;        VIA WPT8 H AND WRITE TO CONTROL REGISTER 6.
                                ;    6.  SET PTER4 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    7.  READ DATA PATTERN FROM TRAM DATA IN BUFFER VIA RPT4 H AND READ TO REG 6
                                ;    8.  WRITE TRACE RAM VIA WPT4 H AND WRITE TO CONTROL REGISTER 6
                                ;    9.  SET SIGNAL TRSL1 L BY SETTING CDAL2 = 1 IN REGISTER 0
                                ;   10.  READ TRACE RAM VIA RPT4 H AND READ TO CONTROL REGISTER 6
                                ;   11.  COMPLEMENT DATA PATTERN - REPEAT STEPS 1-10 WITH THIS PATTERN
                                ;   12.  RESET DATA PATTERN TO 5252 - INCREMENT ADDRESS BY 1
                                ;   13.  REPEAT STEPS 1-12 UNTIL ALL OF THE 1K ADDRESS HAVE BEEN CHECKED.
                                ;--

012174                                  BGNTST
012174                          T24::
012174  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
012200  005037  006376                  CLR     TRADRS                  ;SET TRACE RAM ADDRESS TO ZERO
012204  012701  005252                  MOV     #5252,R1                ;SETUP STARTING DATA PATTERN

012210                          1$:     BGNSEG
012210  104404                          TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING ZERO
                                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE
                                        ;TRACE RAM DATA IN BUFFERS

012212  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
012216  004737  006104                  JSR     PC,LDRDRO               ;GO LOAD,READ AND CEHCK REGISTER 0
012222  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012224                                  ERRDF   1,,ROEROR               ;REGISTER 0 LOW BYTE NOT 0
012224  104455                          TRAP    C$ERDF
012226  000001                          .WORD   1
012230  000000                          .WORD   0
012232  004606                          .WORD   ROEROR
012234                                  CKLOOP
012234  104406                          TRAP    C$CLP1

                                        ;LOAD TRACE RAM ADDRESS REGISTER WITH CONTENTS OF LOCATION "TRADRS"

012236  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 59:48 WITH A DATA
```

```
4753                                            ;PATTERN OF 5252 OR 2525.
4754
4755  012242  010137  002414                    MOV     R1,R6LOAD               ;SETUP DATA PATTERN TO BE LOADED
4756  012246  004537  006430                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4757  012252  000010                            .WORD   PTER8                   ;SELECT TRDI BITS 59:48
4758
4759                                            ;WRITE THE TRACE RAM LOCATION ADDRESSED BY TRACE RAM ADDRESS REGISTER
4760                                            ;WITH THE DATA PATTERN STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 55:48.
4761
4762  012254  012777  000000  170074            MOV     #0,@REG6                ;WRITE THE RAM FROM DATA IN BUFFERS
4763
4764                                            ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
4765                                            ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
4766                                            ;BITS TRDI 55:48 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
4767                                            ;THE SIGNAL RPT4 H.
4768
4769  012262  052737  000004  002370            BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
4770  012270  004737  006104                    JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
4771  012274  001405                            BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4772  012276                                    ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
4773  012276  104455                            TRAP    C$ERDF
4774  012300  000001                            .WORD   1
4775  012302  000000                            .WORD   0
4776  012304  004606                            .WORD   R0EROR
4777  012306                                    CKLOOP
4778  012306  104406                            TRAP    C$CLP1
4779
4780                                            ;READ DATA FROM TRACE RAM BITS TRDI 55:48
4781
4782  012310  017737  170042  002420  3$:       MOV     @REG6,R6READ            ;READ DATA FROM THE RAM
4783  012316  042737  177400  002420            BIC     #177400,R6READ          ;CLEAR BITS NOT IN TRACE RAM
4784  012324  042737  177400  002414            BIC     #177400,R6LOAD          ;CLEAR BITS NOT LOADED INTO TRACE RAM
4785  012332  023737  002414  002420            CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED INTO TRACE RAM
4786                                                                            ;DATA IN BUFFERS TRDI 55:48 WITH DATA
4787                                                                            ;READ FROM THE TRACE RAM
4788  012340  001404                            BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
4789  012342                                    ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR TRDI 55:48
4790  012342  104455                            TRAP    C$ERDF
4791  012344  000004                            .WORD   4
4792  012346  003126                            .WORD   TRAM55
4793  012350  004766                            .WORD   TRAMER
4794  012352                            4$:     ENDSEG
4795  012352                            10000$:
4796  012352  104405                            TRAP    C$ESEG
4797  012354  022701  002525                    CMP     #2525,R1                ;CHECK TO SEE IF DATA PATTERNS DONE
4798  012360  001403                            BEQ     5$                      ;IF YES THEN UPDATE THE ADDRESS
4799  012362  012701  002525                    MOV     #2525,R1                ;COMPLEMENT THE DATA PATTERN LOADED
4800  012366  000710                            BR      1$                      ;GO LOAD THIS DATA PATTERN INTO RAM
4801  012370  012701  005252            5$:     MOV     #5252,R1                ;RESET THE DATA PATTERN
4802  012374  005237  006376                    INC     TRADRS                  ;UPDATE TO NEXT SEQUENTIAL ADDRESS
4803  012400  032737  002000  006376            BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES DONE
4804  012406  001700                            BEQ     1$                      ;IF NOT THEN DO NEXT SET OF ADDRESSES
4805  012410                                    ENDTST
4806  012410                            L10072:
4807  012410  104401                            TRAP    C$ETST
```

```
                                .SBTTL  TEST 25: TRAM ADDRESS/SHORT TEST - TRDI 15:0

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM TRDI 15:0 TO BE ADDRESSED CORRECTLY AND THAT
                                ; NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIP'S. THE TEST WILL
                                ; LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE
                                ; ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK THE ADDRESS TO CONTAIN ITS
                                ; ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO
                                ; THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN.  THE TEST WILL
                                ; REPEAT THIS SEQUENCE FOR ALL ADDRESSES IN THE TRACE RAM.  WHEN ALL ADDRESSES
                                ; HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK ALL OF THE RAM TO CONTAIN THE
                                ; ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
                                ;--

012412                                  BGNTST
012412                          T25::
012412  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        ;THE FOLLOWING SUB TEST WILL WRITE EACH LOCATION OF TRACE RAM TRDI 15:0
                                        ;WITH A DATA PATTERN EQUAL TO ITS ADDRESS.  AS EACH LOCATION IS WRITTEN,
                                        ;THE TEST WILL READ THE LOCATION AND CHECK THAT THE DATA EQUALS ITS
                                        ;ADDRESS.

012416                                  BGNSUB
012416                          T25.1:
012416  104402                          TRAP    C$BSUB
012420  005037  006376                  CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
012424                          1$:     BGNSEG
012424  104404                          TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING A ZERO
                                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE
                                        ;RAM DATA IN BUFFERS.

012426  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
012432  004737  006104                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
012436  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012440                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
012440  104455                          TRAP    C$ERDF
012442  000001                          .WORD   1
012444  000000                          .WORD   0
012446  004606                          .WORD   ROEROR
012450                                  CKLOOP
012450  104406                          TRAP    C$CLP1

                                        ;WRITE AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF LOCA-
                                        ;TION "TRADRS". THE POINTER REGISTER ON EXIT FROM ROUTINE TRADLD WILL
                                        ;HAVE THE SIGNAL PTER0 L ASSERTED.

012452  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;WRITE THE TRACE RAM ADDRESS INTO THE TRACE RAM DATA IN BUFFERS IN
                                        ;BUFFER BITS TRDI 15:0. ON EXIT FROM ROUTINE "TRDIBF" THE POINTER
                                        ;REGISTER WILL HAVE THE SIGNAL PTER1 L ASSERTED.
```

```
4864
4865  012456  013737  006376  002414          MOV     TRADRS,R6LOAD           ;SETUP DATA TO EQUAL TRAM ADDRESS REG
4866  012464  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
4867  012470  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
4868
4869                                          ;WRITE THE ADDRESS IN THE TRACE RAM DATA IN BUFFERS INTO TRACE RAM
4870                                          ;BITS TRDI 15:0
4871
4872  012472  012777  000000  167656          MOV     #0,@REG6                ;WRTIE RAM WITH DATA IN BUFFERS
4873
4874                                          ;SET CDAL2 TO 1 AND CDAL3 TO 0 IN CONTROL REGISTER 0 TO SET THE SIGNAL
4875                                          ;TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW THE DATA IN THE TRACE RAM TO
4876                                          ;BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT1 H.
4877
4878  012500  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
4879  012506  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
4880  012512  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4881  012514                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
4882  012514  104455                          TRAP    C$ERDF
4883  012516  000001                          .WORD   1
4884  012520  000000                          .WORD   0
4885  012522  004606                          .WORD   R0EROR
4886  012524                                  CKLOOP
4887  012524  104406                          TRAP    C$CLP1
4888
4889                                          ;READ AND CHECK TRACE RAM DATA TRDI 15:0.  THE DATA SHOULD EQUAL THE
4890                                          ;ADDRESS BEING TESTED.
4891
4892  012526  017737  167624  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM TRDI 15:0
4893  012534  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED TO EQUAL DATA READ
4894  012542  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
4895  012544                                  ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR - TRDI 15:0
4896  012544  104455                          TRAP    C$ERDF
4897  012546  000004                          .WORD   4
4898  012550  003000                          .WORD   TRAM15
4899  012552  004766                          .WORD   TRAMER
4900  012554                          4$:     ENDSEG
4901  012554                          10000$:
4902  012554  104405                          TRAP    C$ESEG
4903  012556  005237  006376                  INC     TRADRS                  ;UPDATE TRACE RAM ADDRESS BY 1
4904  012562  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF 1K YET
4905  012570  001715                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
4906  012572                                  ENDSUB
4907  012572                          L10074:
4908  012572  104403                          TRAP    C$ESUB
4909
4910                                          ;THE FOLLOWING SUB TEST WILL RESET THE POINTER TO THE BEGINNING
4911                                          ;ADDRESS OF THE TRACE RAM, CHECK THE LOCATION TO EQUAL ITS ADDRESS,
4912                                          ;WRITE,READ, AND CHECK THE LOCATION WITH THE ONES COMPLEMENT OF ITS
4913                                          ;ADDRESS. THIS SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE TRACE
4914                                          ;RAM FOR TRACE RAM TRDI 15:0. THIS TEST WILL CHECK THAT THE TRACE RAM
4915                                          ;CAN BE ADDRESSED CORRECTLY AND THAT WRITING A LOCATION DOES NOT WRITE
4916                                          ;A HIGHER LOCATION.
4917
4918  012574                                  BGNSUB
4919  012574                          T25.2:
```

```
                012574  104402                          TRAP    C$BSUB
                012576  005037  006376                  CLR     TRADRS                  ;RESET TRAM ADDRESS TO ADDRESS 0

                012602                          1$:     BGNSEG
                012602  104404                          TRAP    C$BSEG

                                                        ;SET CDAL2 TO A 1 AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
                                                        ;SIGNAL TRSL1 L. THIS SIGNAL WILL ALLOW THE TRACE RAM TO BE READ ON A
                                                        ;READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT1 H.

                012604  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
                012612  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
                012616  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
                012620                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
                012620  104455                          TRAP    C$ERDF
                012622  000001                          .WORD   1
                012624  000000                          .WORD   0
                012626  004606                          .WORD   R0EROR
                012630                                  CKLOOP
                012630  104406                          TRAP    C$CLP1

                                                        ;GO LOAD ADDRESS TO BE CHECKED INTO TRACE RAM ADDRESS REGISTER USING
                                                        ;THE CONTENTS OF LOCATION "TRADRS" AS THE ADDRESS TO BE LOADED. ON
                                                        ;EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER WILL HAVE THE SIGNAL
                                                        ;PTER0 L ASSERTED.

                012632  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG

                                                        ;SET THE SIGNAL PTER1 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2

                012636  012737  000001  002376          MOV     #PTER1,R2LOAD           ;SETUP REGISTER 2 BITS TO BE LOADED
                012644  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
                012650  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
                012652                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
                012652  104455                          TRAP    C$ERDF
                012654  000002                          .WORD   2
                012656  000000                          .WORD   0
                012660  004706                          .WORD   R2EROR
                012662                                  CKLOOP
                012662  104406                          TRAP    C$CLP1

                                                        ;READ THE DATA THAT WAS PREVIOUSLY WRITTEN IN THE FIRST SUB TEST AND
                                                        ;CHECK THAT THE DATA IS EQUAL TO THE ADDRESS BEING TESTED.

                012664  013737  006376  002414  3$:     MOV     TRADRS,R6LOAD           ;SETUP DATA PREVIOUSLY WRITTEN
                012672  017737  167460  002420          MOV     @REG6,R6READ            ;READ THE DATA FROM THE TRACE RAM
                012700  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK IF DATA IS EQUAL TO ITS ADDRESS
                012706  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
                012710                                  ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR - TRDI 15:0 OR ADDRESS
                012710  104455                          TRAP    C$ERDF
                012712  000004                          .WORD   4
                012714  003000                          .WORD   TRAM15
                012716  004766                          .WORD   TRAMER
                                                                                        ;FAILURE OR ADDRESS SHORT
                012720                          4$:     ENDSEG
                012720                          10000$:
```

```
 4976  012720  104405                          TRAP    C$ESEG
 4977
 4978                                          ;THE FOLLOWING SECTION OF CODE WILL WRITE THE TRACE RAM DATA IN BUFFERS
 4979                                          ;AND THE TRACE RAM WITH THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
 4980
 4981  012722                                  BGNSEG
 4982  012722  104404                          TRAP    C$BSEG
 4983
 4984                                          ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
 4985                                          ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
 4986
 4987  012724  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOWER BYTE
 4988  012730  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
 4989  012734  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
 4990  012736                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
 4991  012736  104455                          TRAP    C$ERDF
 4992  012740  000001                          .WORD   1
 4993  012742  000000                          .WORD   0
 4994  012744  004606                          .WORD   R0EROR
 4995  012746                                  CKLOOP
 4996  012746  104406                          TRAP    C$CLP1
 4997
 4998                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0 WITH DATA
 4999                                          ;EQUAL TO THE ONES COMPLEMENT OF THE ADDRESS. ON EXIT FROM ROUTINE
 5000                                          ;"TRDIBF", THE POINTER REGISTER WILL HAVE THE SIGNAL PTER1 L ASSERTED.
 5001
 5002  012750  013737  006376  002414  5$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS UNDER TEST
 5003  012756  005137  002414                  COM     R6LOAD                  ;COMPLEMENT THE ADDRESS
 5004  012762  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
 5005  012766  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
 5006
 5007                                          ;WRITE TRACE RAM LOCATION WITH DATA PATTERN EQUAL TO THE COMPLEMENT
 5008                                          ;OF ITS ADDRESS.  THE DATA TO BE WRITTEN INTO THE TRACE RAM IS
 5009                                          ;STORED IN THE TRACE RAM DATA IN BUFFERS TRDI 15:0.
 5010
 5011  012770  012777  000000  167360          MOV     #0,@REG6                ;WRITE RAM WITH TRAM DATA IN BUF
 5012
 5013                                          ;SET CDAL2 TO A 1 AND CDAL 3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
 5014                                          ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
 5015                                          ;BITS TRDI 15:0 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
 5016                                          ;THE SIGNAL RPT1 H.
 5017
 5018  012776  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
 5019  013004  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
 5020  013010  001405                          BEQ     6$                      ;IF LOADEDOK THEN CONTINUE
 5021  013012                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
 5022  013012  104455                          TRAP    C$ERDF
 5023  013014  000001                          .WORD   1
 5024  013016  000000                          .WORD   0
 5025  013020  004606                          .WORD   R0EROR
 5026  013022                                  CKLOOP
 5027  013022  104406                          TRAP    C$CLP1
 5028
 5029                                          ;READ DATA FROM THE TRACE RAM TRDI 15:0 CHECKING THE DATA TO BE THE
 5030                                          ;ONES COMPLEMENT OF THE ADDRESS UNDER TEST
 5031
```

```
5032  013024  017737  167326  002420  6$:     MOV     @REG6,R6READ            ;READ DATA FROM THE TRACE RAM
5033  013032  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5034  013040  001404                          BEQ     7$                      ;ID DATA EQUAL THEN CONTINUE
5035  013042                                  ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR - TRDI 15:0
5036  013042  104455                          TRAP    C$ERDF
5037  013044  000004                          .WORD   4
5038  013046  003000                          .WORD   TRAM15
5039  013050  004766                          .WORD   TRAMER
5040  013052                          7$:     ENDSEG
5041  013052                          10001$:
5042  013052  104405                          TRAP    C$ESEG
5043  013054  005237  006376                  INC     TRADRS                  ;UPDATE THE ADDRESS BY 1
5044  013060  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES BEEN TESTED
5045  013066  001645                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5046  013070                                  ENDSUB
5047  013070                          L10075:
5048  013070  104403                          TRAP    C$ESUB
5049
5050                                          ;THE FOLLOWING SUB TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING
5051                                          ;ADDRESS OF THE TRACE RAM AND CHECK EACH LOCATION OF THE TRACE RAM TO
5052                                          ;CONTAIN THE ONES COMPLEMENT OF ITS ADDRESS. IN A FAILURE OCCURS, THE
5053                                          ;ERROR MAY BE AN ADDRESS SHORT IN WHICH WRITING A LOCATION IN THE
5054                                          ;PREVIOUS SUB TEST WROTE A LOCATION LOWER THEN THE ADDRESS BEING TESTED.
5055
5056  013072                                  BGNSUB
5057  013072                          T25.3:
5058  013072  104402                          TRAP    C$BSUB
5059  013074  005037  006376                  CLR     TRADRS                  ;CLEAR THE ADDRESS TO ADDRESS 0
5060
5061  013100                          1$:     BGNSEG
5062  013100  104404                          TRAP    C$BSEG
5063
5064                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO ASSERT
5065                                          ;THE SIGNAL TRSL1 L.  THE SIGNAL TRSL1 L WILL ALLOW THE DATA FROM THE
5066                                          ;TRACE RAM BITS TRDI 15:0 TO BE READ ON A READ COMMAND TO CONTROL
5067                                          ;REGISTER 6 VIA THE SIGNAL RPT1 H.
5068
5069  013102  112737  000004  002370          MOVB    #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5070  013110  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
5071  013114  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5072  013116                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5073  013116  104455                          TRAP    C$ERDF
5074  013120  000001                          .WORD   1
5075  013122  000000                          .WORD   0
5076  013124  004606                          .WORD   R0EROR
5077  013126                                  CKLOOP
5078  013126  104406                          TRAP    C$CLP1
5079
5080                                          ;LOAD,READ AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF
5081                                          ;LOCATION "TRADRS".  ON EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER
5082                                          ;WILL HAVE THE SIGNAL PTER0 L ASSERTED.
5083
5084  013130  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5085
5086                                          ;SET SIGNAL PTER1 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5087
```

```
5088  013134  012737  000001  002376          MOV     #PTER1,R2LOAD           ;SETUP BITS TO BE LOADED
5089  013142  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5090  013146  001405                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
5091  013150                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5092  013150  104455                          TRAP    C$ERDF
5093  013152  000002                          .WORD   2
5094  013154  000000                          .WORD   0
5095  013156  004706                          .WORD   R2EROR
5096  013160                                   CKLOOP
5097  013160  104406                          TRAP    C$CLP1
5098
5099                                           ;READ DATA PREVIOUSLY WRITTEN IN THE LAST SUB TEST CHECKING THE DATA
5100                                           ;TO BE THE COMPLEMENT OF THE ADDRESS.
5101
5102  013162  013737  006376  002414  3$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS BEING TESTED
5103  013170  005137  002414                  COM     R6LOAD                  ;MAKE IT THE ONES COMPLEMENT
5104  013174  017737  167156  002420          MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM
5105  013202  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5106  013210  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5107  013212                                   ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR - TRDI 15:0
5108  013212  104455                          TRAP    C$ERDF
5109  013214  000004                          .WORD   4
5110  013216  003000                          .WORD   TRAM15
5111  013220  004766                          .WORD   TRAMER
5112  013222                           4$:     ENDSEG
5113  013222                           10000$:
5114  013222  104405                          TRAP    C$ESEG
5115  013224  005237  006376                  INC     TRADRS                  ;UPDATE THE ADDRESS BY ONE
5116  013230  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES CHECKED
5117  013236  001720                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5118  013240                                   ENDSUB
5119  013240                           L10076:
5120  013240  104403                          TRAP    C$ESUB
5121  013242                                   ENDTST
5122  013242                           L10073:
5123  013242  104401                          TRAP    C$ETST
5124
```

```
                        .SBTTL  TEST 26: TRAM ADDRESS/SHORT TEST - TRDI 31:16

                        ;++
                        ; THIS TEST WILL CHECK TRACE RAM TRDI 31:16 TO BE ADDRESSED CORRECTLY AND THAT
                        ; NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIP'S. THE TEST WILL
                        ; LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE
                        ; ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET
                        ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK THE ADDRESS TO CONTAIN ITS
                        ; ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO
                        ; THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN.  THE TEST WILL
                        ; REPEAT THIS SEQUENCE FOR ALL ADDRESSES IN THE TRACE RAM.  WHEN ALL ADDRESSES
                        ; HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET
                        ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK ALL OF THE RAM TO CONTAIN THE
                        ; ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
                        ;--

013244                          BGNTST
013244                  T26::
013244  004737  005476          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                        ;THE FOLLOWING SUB TEST WILL WRITE EACH LOCATION OF TRACE RAM TRDI 31:16
                        ;WITH A DATA PATTERN EQUAL TO ITS ADDRESS.  AS EACH LOCATION IS WRITTEN,
                        ;THE TEST WILL READ THE LOCATION AND CHECK THAT THE DATA EQUALS ITS
                        ;ADDRESS.

013250                          BGNSUB
013250                  T26.1:
013250  104402                  TRAP    C$BSUB
013252  005037  006376          CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
013256                  1$:     BGNSEG
013256  104404                  TRAP    C$BSEG

                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING A ZERO
                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE
                        ;RAM DATA IN BUFFERS.

013260  105037  002370          CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
013264  004737  006104          JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
013270  001405                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
013272                          ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
013272  104455                  TRAP    C$ERDF
013274  000001                  .WORD   1
013276  000000                  .WORD   0
013300  004606                  .WORD   ROEROR
013302                          CKLOOP
013302  104406                  TRAP    C$CLP1

                        ;WRITE AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF LOCA-
                        ;TION "TRADRS". THE POINTER REGISTER ON EXIT FROM ROUTINE TRADLD WILL
                        ;HAVE THE SIGNAL PTER0 L ASSERTED.

013304  004737  006312  2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                        ;WRITE THE TRACE RAM ADDRESS INTO THE TRACE RAM DATA IN BUFFERS IN
                        ;BUFFER BITS TRDI 31:16. ON EXIT FROM ROUTINE "TRDIBF" THE POINTER
                        ;REGISTER WILL HAVE THE SIGNAL PTER2 L ASSERTED.
```

```
5181
5182  013310  013737  006376  002414          MOV     TRADRS,R6LOAD           ;SETUP DATA TO EQUAL TRAM ADDRESS REG
5183  013316  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5184  013322  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
5185
5186                                          ;WRITE THE ADDRESS IN THE TRACE RAM DATA IN BUFFERS INTO TRACE RAM
5187                                          ;BITS TRDI 31:16
5188
5189  013324  012777  000000  167024          MOV     #0,@REG6                ;WRTIE RAM WITH DATA IN BUFFERS
5190
5191                                          ;SET CDAL2 TO 1 AND CDAL3 TO 0 IN CONTROL REGISTER 0 TO SET THE SIGNAL
5192                                          ;TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW THE DATA IN THE TRACE RAM TO
5193                                          ;BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT2 H.
5194
5195  013332  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5196  013340  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
5197  013344  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5198  013346                                  ERRDF   1.,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5199  013346  104455                          TRAP    C$ERDF
5200  013350  000001                          .WORD   1
5201  013352  000000                          .WORD   0
5202  013354  004606                          .WORD   R0EROR
5203  013356                                  CKLOOP
5204  013356  104406                          TRAP    C$CLP1
5205
5206                                          ;READ AND CHECK TRACE RAM DATA TRDI 31:16.  THE DATA SHOULD EQUAL THE
5207                                          ;ADDRESS BEING TESTED.
5208
5209  013360  017737  166772  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM TRDI 31:16
5210  013366  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED TO EQUAL DATA READ
5211  013374  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
5212  013376                                  ERRDF   4,TRAM31,TRAMER         ;TRAM DATA ERROR - TRDI 31:16
5213  013376  104455                          TRAP    C$ERDF
5214  013400  000004                          .WORD   4
5215  013402  003034                          .WORD   TRAM31
5216  013404  004766                          .WORD   TRAMER
5217  013406                          4$:     ENDSEG
5218  013406                          10000$:
5219  013406  104405                          TRAP    C$ESEG
5220  013410  005237  006376                  INC     TRADRS                  ;UPDATE TRACE RAM ADDRESS BY 1
5221  013414  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF 1K YET
5222  013422  001715                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
5223  013424                                  ENDSUB
5224  013424                          L10100:
5225  013424  104403                          TRAP    C$ESUB
5226
5227                                          ;THE FOLLOWING SUB TEST WILL RESET THE POINTER TO THE BEGINNING
5228                                          ;ADDRESS OF THE TRACE RAM, CHECK THE LOCATION TO EQUAL ITS ADDRESS,
5229                                          ;WRITE,READ, AND CHECK THE LOCATION WITH THE ONES COMPLEMENT OF ITS
5230                                          ;ADDRESS. THIS SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE TRACE
5231                                          ;RAM FOR TRACE RAM TRDI 31:16. THIS TEST WILL CHECK THAT THE TRACE RAM
5232                                          ;CAN BE ADDRESSED CORRECTLY AND THAT WRITING A LOCATION DOES NOT WRITE
5233                                          ;A HIGHER LOCATION.
5234
5235  013426                                  BGNSUB
5236  013426                          T26.2:
```

```
5237  013426  104402                          TRAP    C$BSUB
5238  013430  005037  006376                  CLR     TRADRS                  ;RESET TRAM ADDRESS TO ADDRESS 0
5239
5240  013434                          1$:     BGNSEG
5241  013434  104404                          TRAP    C$BSEG
5242
5243                                          ;SET CDAL2 TO A 1 AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5244                                          ;SIGNAL TRSL1 L. THIS SIGNAL WILL ALLOW THE TRACE RAM TO BE READ ON A
5245                                          ;READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT2 H.
5246
5247  013436  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5248  013444  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
5249  013450  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5250  013452                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5251  013452  104455                          TRAP    C$ERDF
5252  013454  000001                          .WORD   1
5253  013456  000000                          .WORD   0
5254  013460  004606                          .WORD   ROEROR
5255  013462                                  CKLOOP
5256  013462  104406                          TRAP    C$CLP1
5257
5258                                          ;GO LOAD ADDRESS TO BE CHECKED INTO TRACE RAM ADDRESS REGISTER USING
5259                                          ;THE CONTENTS OF LOCATION "TRADRS" AS THE ADDRESS TO BE LOADED. ON
5260                                          ;EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER WILL HAVE THE SIGNAL
5261                                          ;PTER0 L ASSERTED.
5262
5263  013464  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5264
5265                                          ;SET THE SIGNAL PTER2 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5266
5267  013470  012737  000002  002376          MOV     #PTER2,R2LOAD           ;SETUP REGISTER 2 BITS TO BE LOADED
5268  013476  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5269  013502  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5270  013504                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5271  013504  104455                          TRAP    C$ERDF
5272  013506  000002                          .WORD   2
5273  013510  000000                          .WORD   0
5274  013512  004706                          .WORD   R2EROR
5275  013514                                  CKLOOP
5276  013514  104406                          TRAP    C$CLP1
5277
5278                                          ;READ THE DATA THAT WAS PREVIOUSLY WRITTEN IN THE FIRST SUB TEST AND
5279                                          ;CHECK THAT THE DATA IS EQUAL TO THE ADDRESS BEING TESTED.
5280
5281  013516  013737  006376  002414  3$:     MOV     TRADRS,R6LOAD           ;SETUP DATA PREVIOUSLY WRITTEN
5282  013524  017737  166626  002420          MOV     @REG6,R6READ            ;READ THE DATA FROM THE TRACE RAM
5283  013532  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK IF DATA IS EQUAL TO ITS ADDRESS
5284  013540  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5285  013542                                  ERRDF   4,TRAM31,TRAMER         ;TRAM DATA ERROR - TRDI 31:16 OR ADDRESS
5286  013542  104455                          TRAP    C$ERDF
5287  013544  000004                          .WORD   4
5288  013546  003034                          .WORD   TRAM31
5289  013550  004766                          .WORD   TRAMER
5290                                                                          ;FAILURE OR ADDRESS SHORT
5291  013552                          4$:     ENDSEG
5292  013552                          10000$:
```

```
5293  013552  104405                          TRAP    C$ESEG
5294
5295                                          ;THE FOLLOWING SECTION OF CODE WILL WRITE THE TRACE RAM DATA IN BUFFERS
5296                                          ;AND THE TRACE RAM WITH THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
5297
5298  013554                                  BGNSEG
5299  013554  104404                          TRAP    C$BSEG
5300
5301                                          ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
5302                                          ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
5303
5304  013556  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOWER BYTE
5305  013562  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
5306  013566  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
5307  013570                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5308  013570  104455                          TRAP    C$ERDF
5309  013572  000001                          .WORD   1
5310  013574  000000                          .WORD   0
5311  013576  004606                          .WORD   R0EROR
5312  013600                                  CKLOOP
5313  013600  104406                          TRAP    C$CLP1
5314
5315                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 31:16 WITH DATA
5316                                          ;EQUAL TO THE ONES COMPLEMENT OF THE ADDRESS. ON EXIT FROM ROUTINE
5317                                          ;"TRDIBF", THE POINTER REGISTER WILL HAVE THE SIGNAL PTER2 L ASSERTED.
5318
5319  013602  013737  0C6376  002414  5$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS UNDER TEST
5320  013610  005137  002414                  COM     R6LOAD                  ;COMPLEMENT THE ADDRESS
5321  013614  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5322  013620  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
5323
5324                                          ;WRITE TRACE RAM LOCATION WITH DATA PATTERN EQUAL TO THE COMPLEMENT
5325                                          ;OF ITS ADDRESS.  THE DATA TO BE WRITTEN INTO THE TRACE RAM IS
5326                                          ;STORED IN THE TRACE RAM DATA IN BUFFERS TRDI 31:16.
5327
5328  013622  012777  000000  166526          MOV     #0,@REG6                ;WRITE RAM WITH TRAM DATA IN BUF
5329
5330                                          ;SET CDAL2 TO A 1 AND CDAL 3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5331                                          :SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
5332                                          ;BITS TRDI 31:16 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
5333                                          ;THE SIGNAL RPT2 H.
5334
5335  013630  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5336  013636  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
5337  013642  001405                          BEQ     6$                      ;IF LOADEDOK THEN CONTINUE
5338  013644                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5339  013644  104455                          TRAP    C$ERDF
5340  013646  000001                          .WORD   1
5341  013650  000000                          .WORD   0
5342  013652  004606                          .WORD   R0EROR
5343  013654                                  CKLOOP
5344  013654  104406                          TRAP    C$CLP1
5345
5346                                          ;READ DATA FROM THE TRACE RAM TRDI 31:16 CHECKING THE DATA TO BE THE
5347                                          ;ONES COMPLEMENT OF THE ADDRESS UNDER TEST
5348
```

```
5349  013656  017737  166474  002420  6$:     MOV     @REG6,R6READ            ;READ DATA FROM THE TRACE RAM
5350  013664  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5351  013672  001404                          BEQ     7$                      ;ID DATA EQUAL THEN CONTINUE
5352  013674                                  ERRDF   4,TRAM31,TRAMER         ;TRAM DATA ERROR - TRDI 31:16
5353  013674  104455                          TRAP    C$ERDF
5354  013676  000004                          .WORD   4
5355  013700  003034                          .WORD   TRAM31
5356  013702  004766                          .WORD   TRAMER
5357  013704                          7$:     ENDSEG
5358  013704                          10001$:
5359  013704  104405                          TRAP    C$ESEG
5360  013706  005237  006376                  INC     TRADRS                  ;UPDATE THE ADDRESS BY 1
5361  013712  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES BEEN TESTED
5362  013720  001645                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5363  013722                                  ENDSUB
5364  013722                          L10101:
5365  013722  104403                          TRAP    C$ESUB
5366
5367                                          ;THE FOLLOWING SUB TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING
5368                                          ;ADDRESS OF THE TRACE RAM AND CHECK EACH LOCATION OF THE TRACE RAM TO
5369                                          ;CONTAIN THE ONES COMPLEMENT OF ITS ADDRESS. IN A FAILURE OCCURS, THE
5370                                          ;ERROR MAY BE AN ADDRESS SHORT IN WHICH WRITING A LOCATION IN THE
5371                                          ;PREVIOUS SUB TEST WROTE A LOCATION LOWER THEN THE ADDRESS BEING TESTED.
5372
5373  013724                                  BGNSUB
5374  013724                          T26.3:
5375  013724  104402                          TRAP    C$BSUB
5376  013726  005037  006376                  CLR     TRADRS                  ;CLEAR THE ADDRESS TO ADDRESS 0
5377
5378  013732                          1$:     BGNSEG
5379  013732  104404                          TRAP    C$BSEG
5380
5381                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO ASSERT
5382                                          ;THE SIGNAL TRSL1 L.  THE SIGNAL TRSL1 L WILL ALLOW THE DATA FROM THE
5383                                          ;TRACE RAM BITS TRDI 31:16 TO BE READ ON A READ COMMAND TO CONTROL
5384                                          ;REGISTER 6 VIA THE SIGNAL RPT2 H.
5385
5386  013734  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5387  013742  004737  006104                  JSR     PC,LDRDRO               ;GO LOAD,READ AND CHECK REGISTER 0
5388  013746  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5389  013750                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5390  013750  104455                          TRAP    C$ERDF
5391  013752  000001                          .WORD   1
5392  013754  000000                          .WORD   0
5393  013756  004606                          .WORD   ROEROR
5394  013760                                  CKLOOP
5395  013760  104406                          TRAP    C$CLP1
5396
5397                                          ;LOAD,READ AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF
5398                                          ;LOCATION "TRADRS".  ON EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER
5399                                          ;WILL HAVE THE SIGNAL PTER0 L ASSERTED.
5400
5401  013762  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5402
5403                                          ;SET SIGNAL PTER2 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5404
```

```
5405  013766  012737  000002  002376          MOV     #PTER2,R2LOAD           ;SETUP BITS TO BE LOADED
5406  013774  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5407  014000  001405                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
5408  014002                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5409  014002  104455                          TRAP    C$ERDF
5410  014004  000002                          .WORD   2
5411  014006  000000                          .WORD   0
5412  014010  004706                          .WORD   R2EROR
5413  014012                                  CKLOOP
5414  014012  104406                          TRAP    C$CLP1
5415
5416                                          ;READ DATA PREVIOUSLY WRITTEN IN THE LAST SUB TEST CHECKING THE DATA
5417                                          ;TO BE THE COMPLEMENT OF THE ADDRESS.
5418
5419  014014  013737  006376  002414  3$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS BEING TESTED
5420  014022  005137  002414                  COM     R6LOAD                  ;MAKE IT THE ONES COMPLEMENT
5421  014026  017737  166324  002420          MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM
5422  014034  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5423  014042  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5424  014044                                  ERRDF   4,TRAM31,TRAMER         ;TRAM DATA ERROR - TRDI 31:16
5425  014044  104455                          TRAP    C$ERDF
5426  014046  000004                          .WORD   4
5427  014050  003034                          .WORD   TRAM31
5428  014052  004766                          .WORD   TRAMER
5429  014054                          4$:     ENDSEG
5430  014054                          10000$:
5431  014054  104405                          TRAP    C$ESEG
5432  014056  005237  006376                  INC     TRADRS                  ;UPDATE THE ADDRESS BY ONE
5433  014062  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES CHECKED
5434  014070  001720                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5435  014072                                  ENDSUB
5436  014072                          L10102:
5437  014072  104403                          TRAP    C$ESUB
5438  014074                                  ENDTST
5439  014074                          L10077:
5440  014074  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 27: TRAM ADDRESS/SHORT TEST - TRDI 47:32

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM TRDI 47:32 TO BE ADDRESSED CORRECTLY AND THAT
                                ; NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIP'S. THE TEST WILL
                                ; LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE
                                ; ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK THE ADDRESS TO CONTAIN ITS
                                ; ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO
                                ; THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN.  THE TEST WILL
                                ; REPEAT THIS SEQUENCE FOR ALL ADDRESSES IN THE TRACE RAM.  WHEN ALL ADDRESSES
                                ; HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK ALL OF THE RAM TO CONTAIN THE
                                ; ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
                                ;--

014076                                  BGNTST
014076                          T27::
014076  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        ;THE FOLLOWING SUB TEST WILL WRITE EACH LOCATION OF TRACE RAM TRDI 47:32
                                        ;WITH A DATA PATTERN EQUAL TO ITS ADDRESS.  AS EACH LOCATION IS WRITTEN,
                                        ;THE TEST WILL READ THE LOCATION AND CHECK THAT THE DATA EQUALS ITS
                                        ;ADDRESS.

014102                                  BGNSUB
014102                          T27.1:
014102  104402                          TRAP    C$BSUB
014104  005037  006376                  CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
014110                          1$:     BGNSEG
014110  104404                          TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING A ZERO
                                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE
                                        ;RAM DATA IN BUFFERS.

014112  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
014116  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
014122  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
014124                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
014124  104455                          TRAP    C$ERDF
014126  000001                          .WORD   1
014130  000000                          .WORD   0
014132  004606                          .WORD   ROEROR
014134                                  CKLOOP
014134  104406                          TRAP    C$CLP1

                                        ;WRITE AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF LOCA-
                                        ;TION "TRADRS". THE POINTER REGISTER ON EXIT FROM ROUTINE TRADLD WILL
                                        ;HAVE THE SIGNAL PTER0 L ASSERTED.

014136  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;WRITE THE TRACE RAM ADDRESS INTO THE TRACE RAM DATA IN BUFFERS IN
                                        ;BUFFER BITS TRDI 47:32. ON EXIT FROM ROUTINE "TRDIBF" THE POINTER
                                        ;REGISTER WILL HAVE THE SIGNAL PTER3 L ASSERTED.
```

```
5497
5498  014142  013737  006376  002414          MOV     TRADRS,R6LOAD           ;SETUP DATA TO EQUAL TRAM ADDRESS REG
5499  014150  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5500  014154  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
5501
5502                                          ;WRITE THE ADDRESS IN THE TRACE RAM DATA IN BUFFERS INTO TRACE RAM
5503                                          ;BITS TRDI 47:32
5504
5505  014156  012777  000000  166172          MOV     #0,@REG6                ;WRTIE RAM WITH DATA IN BUFFERS
5506
5507                                          ;SET CDAL2 TO 1 AND CDAL3 TO 0 IN CONTROL REGISTER 0 TO SET THE SIGNAL
5508                                          ;TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW THE DATA IN THE TRACE RAM TO
5509                                          ;BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT3 H.
5510
5511  014164  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5512  014172  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
5513  014176  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5514  014200                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5515  014200  104455                          TRAP    C$ERDF
5516  014202  000001                          .WORD   1
5517  014204  000000                          .WORD   0
5518  014206  004606                          .WORD   R0EROR
5519  014210                                  CKLOOP
5520  014210  104406                          TRAP    C$CLP1
5521
5522                                          ;READ AND CHECK TRACE RAM DATA TRDI 47:32.  THE DATA SHOULD EQUAL THE
5523                                          ;ADDRESS BEING TESTED.
5524
5525  014212  017737  166140  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM TRDI 47:32
5526  014220  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED TO EQUAL DATA READ
5527  014226  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
5528  014230                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR - TRDI 47:32
5529  014230  104455                          TRAP    C$ERDF
5530  014232  000004                          .WORD   4
5531  014234  003071                          .WORD   TRAM47
5532  014236  004766                          .WORD   TRAMER
5533  014240                          4$:     ENDSEG
5534  014240                          10000$:
5535  014240  104405                          TRAP    C$ESEG
5536  014242  005237  006376                  INC     TRADRS                  ;UPDATE TRACE RAM ADDRESS BY 1
5537  014246  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF 1K YET
5538  014254  001715                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
5539  014256                                  ENDSUB
5540  014256                          L10104:
5541  014256  104403                          TRAP    C$ESUB
5542
5543                                          ;THE FOLLOWING SUB TEST WILL RESET THE POINTER TO THE BEGINNING
5544                                          ;ADDRESS OF THE TRACE RAM, CHECK THE LOCATION TO EQUAL ITS ADDRESS,
5545                                          ;WRITE,READ, AND CHECK THE LOCATION WITH THE ONES COMPLEMENT OF ITS
5546                                          ;ADDRESS. THIS SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE TRACE
5547                                          ;RAM FOR TRACE RAM TRDI 47:32. THIS TEST WILL CHECK THAT THE TRACE RAM
5548                                          ;CAN BE ADDRESSED CORRECTLY AND THAT WRITING A LOCATION DOES NOT WRITE
5549                                          ;A HIGHER LOCATION.
5550
5551  014260                                  BGNSUB
5552  014260                          T27.2:
```

```
5553  014260  104402                          TRAP    C$BSUB
5554  014262  005037  006376                  CLR     TRADRS                  ;RESET TRAM ADDRESS TO ADDRESS 0
5555
5556  014266                          1$:     BGNSEG
5557  014266  104404                          TRAP    C$BSEG
5558
5559                                          ;SET CDAL2 TO A 1 AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5560                                          ;SIGNAL TRSL1 L. THIS SIGNAL WILL ALLOW THE TRACE RAM TO BE READ ON A
5561                                          ;READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT3 H.
5562
5563  014270  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5564  014276  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
5565  014302  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5566  014304                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5567  014304  104455                          TRAP    C$ERDF
5568  014306  000001                          .WORD   1
5569  014310  000000                          .WORD   0
5570  014312  004606                          .WORD   ROEROR
5571  014314                                  CKLOOP
5572  014314  104406                          TRAP    C$CLP1
5573
5574                                          ;GO LOAD ADDRESS TO BE CHECKED INTO TRACE RAM ADDRESS REGISTER USING
5575                                          ;THE CONTENTS OF LOCATION "TRADRS" AS THE ADDRESS TO BE LOADED. ON
5576                                          ;EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER WILL HAVE THE SIGNAL
5577                                          ;PTER0 L ASSERTED.
5578
5579  014316  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5580
5581                                          ;SET THE SIGNAL PTER3 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5582
5583  014322  012737  000003  002376          MOV     #PTER3,R2LOAD           ;SETUP REGISTER 2 BITS TO BE LOADED
5584  014330  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5585  014334  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5586  014336                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5587  014336  104455                          TRAP    C$ERDF
5588  014340  000002                          .WORD   2
5589  014342  000000                          .WORD   0
5590  014344  004706                          .WORD   R2EROR
5591  014346                                  CKLOOP
5592  014346  104406                          TRAP    C$CLP1
5593
5594                                          ;READ THE DATA THAT WAS PREVIOUSLY WRITTEN IN THE FIRST SUB TEST AND
5595                                          ;CHECK THAT THE DATA IS EQUAL TO THE ADDRESS BEING TESTED.
5596
5597  014350  013737  006376  002414  3$:     MOV     TRADRS,R6LOAD           ;SETUP DATA PREVIOUSLY WRITTEN
5598  014356  017737  165774  002420          MOV     @REG6,R6READ            ;READ THE DATA FROM THE TRACE RAM
5599  014364  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK IF DATA IS EQUAL TO ITS ADDRESS
5600  014372  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5601  014374                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR - TRDI 47:32 OR ADDRESS
5602  014374  104455                          TRAP    C$ERDF
5603  014376  000004                          .WORD   4
5604  014400  003071                          .WORD   TRAM47
5605  014402  004766                          .WORD   TRAMER
5606                                                                          ;FAILURE OR ADDRESS SHORT
5607  014404                          4$:     ENDSEG
5608  014404                          10000$:
```

```
5609  014404  104405                          TRAP    C$ESEG
5610
5611                                          ;THE FOLLOWING SECTION OF CODE WILL WRITE THE TRACE RAM DATA IN BUFFERS
5612                                          ;AND THE TRACE RAM WITH THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
5613
5614  014406                                  BGNSEG
5615  014406  104404                          TRAP    C$BSEG
5616
5617                                          ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
5618                                          ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
5619
5620  014410  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOWER BYTE
5621  014414  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
5622  014420  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
5623  014422                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5624  014422  104455                          TRAP    C$ERDF
5625  014424  000001                          .WORD   1
5626  014426  000000                          .WORD   0
5627  014430  004606                          .WORD   R0EROR
5628  014432                                  CKLOOP
5629  014432  104406                          TRAP    C$CLP1
5630
5631                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 47:32 WITH DATA
5632                                          ;EQUAL TO THE ONES COMPLEMENT OF THE ADDRESS. ON EXIT FROM ROUTINE
5633                                          ;"TRDIBF", THE POINTER REGISTER WILL HAVE THE SIGNAL PTER3 L ASSERTED.
5634
5635  014434  013737  006376  002414  5$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS UNDER TEST
5636  014442  C05137  002414                  COM     R6LOAD                  ;COMPLEMENT THE ADDRESS
5637  014446  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5638  014452  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
5639
5640                                          ;WRITE TRACE RAM LOCATION WITH DATA PATTERN EQUAL TO THE COMPLEMENT
5641                                          ;OF ITS ADDRESS.  THE DATA TO BE WRITTEN INTO THE TRACE RAM IS
5642                                          ;STORED IN THE TRACE RAM DATA IN BUFFERS TRDI 47:32.
5643
5644  014454  012777  000000  165674          MOV     #0,@REG6                ;WRITE RAM WITH TRAM DATA IN BUF
5645
5646                                          ;SET CDAL2 TO A 1 AND CDAL 3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5647                                          ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
5648                                          ;BITS TRDI 47:32 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
5649                                          ;THE SIGNAL RPT3 H.
5650
5651  014462  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5652  014470  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
5653  014474  001405                          BEQ     6$                      ;IF LOADEDOK THEN CONTINUE
5654  014476                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5655  014476  104455                          TRAP    C$ERDF
5656  014500  000001                          .WORD   1
5657  014502  000000                          .WORD   0
5658  014504  004606                          .WORD   R0EROR
5659  014506                                  CKLOOP
5660  014506  104406                          TRAP    C$CLP1
5661
5662                                          ;READ DATA FROM THE TRACE RAM TRDI 47:32 CHECKING THE DATA TO BE THE
5663                                          ;ONES COMPLEMENT OF THE ADDRESS UNDER TEST
5664
```

```
5665  014510  017737  165642  002420  6$:     MOV     @REG6,R6READ            ;READ DATA FROM THE TRACE RAM
5666  014516  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5667  014524  001404                          BEQ     7$                      ;ID DATA EQUAL THEN CONTINUE
5668  014526                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR - TRDI 47:32
5669  014526  104455                          TRAP    C$ERDF
5670  014530  000004                          .WORD   4
5671  014532  003071                          .WORD   TRAM47
5672  014534  004766                          .WORD   TRAMER
5673  014536                          7$:     ENDSEG
5674  014536                          10001$:
5675  014536  104405                          TRAP    C$ESEG
5676  014540  005237  006376                  INC     TRADRS                  ;UPDATE THE ADDRESS BY 1
5677  014544  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES BEEN TESTED
5678  014552  001645                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5679  014554                                  ENDSUB
5680  014554                          L10105:
5681  014554  104403                          TRAP    C$ESUB
5682
5683                                          ;THE FOLLOWING SUB TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING
5684                                          ;ADDRESS OF THE TRACE RAM AND CHECK EACH LOCATION OF THE TRACE RAM TO
5685                                          ;CONTAIN THE ONES COMPLEMENT OF ITS ADDRESS. IN A FAILURE OCCURS, THE
5686                                          ;ERROR MAY BE AN ADDRESS SHORT IN WHICH WRITING A LOCATION IN THE
5687                                          ;PREVIOUS SUB TEST WROTE A LOCATION LOWER THEN THE ADDRESS BEING TESTED.
5688
5689  014556                                  BGNSUB
5690  014556                          T27.3:
5691  014556  104402                          TRAP    C$BSUB
5692  014560  005037  006376                  CLR     TRADRS                  ;CLEAR THE ADDRESS TO ADDRESS 0
5693
5694  014564                          1$:     BGNSEG
5695  014564  104404                          TRAP    C$BSEG
5696
5697                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO ASSERT
5698                                          ;THE SIGNAL TRSL1 L.  THE SIGNAL TRSL1 L WILL ALLOW THE DATA FROM THE
5699                                          ;TRACE RAM BITS TRDI 47:32 TO BE READ ON A READ COMMAND TO CONTROL
5700                                          ;REGISTER 6 VIA THE SIGNAL RPT3 H.
5701
5702  014566  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5703  014574  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
5704  014600  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5705  014602                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5706  014602  104455                          TRAP    C$ERDF
5707  014604  000001                          .WORD   1
5708  014606  000000                          .WORD   0
5709  014610  004606                          .WORD   ROEROR
5710  014612                                  CKLOOP
5711  014612  104406                          TRAP    C$CLP1
5712
5713                                          ;LOAD,READ AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF
5714                                          ;LOCATION "TRADRS".  ON EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER
5715                                          ;WILL HAVE THE SIGNAL PTER0 L ASSERTED.
5716
5717  014614  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5718
5719                                          ;SET SIGNAL PTER3 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5720
```

```
5721  014620  012737  000003  002376          MOV     #PTER3,R2LOAD           ;SETUP BITS TO BE LOADED
5722  014626  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5723  014632  001405                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
5724  014634                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5725  014634  104455                          TRAP    C$ERDF
5726  014636  000002                          .WORD   2
5727  014640  000000                          .WORD   0
5728  014642  004706                          .WORD   R2EROR
5729  014644                                  CKLOOP
5730  014644  104406                          TRAP    C$CLP1
5731
5732                                          ;READ DATA PREVIOUSLY WRITTEN IN THE LAST SUB TEST CHECKING THE DATA
5733                                          ;TO BE THE COMPLEMENT OF THE ADDRESS.
5734
5735  014646  013737  006376  002414  3$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS BEING TESTED
5736  014654  005137  002414                  COM     R6LOAD                  ;MAKE IT THE ONES COMPLEMENT
5737  014660  017737  165472  002420          MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM
5738  014666  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5739  014674  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5740  014676                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR - TRDI 47:32
5741  014676  104455                          TRAP    C$ERDF
5742  014700  000004                          .WORD   4
5743  014702  003071                          .WORD   TRAM47
5744  014704  004766                          .WORD   TRAMER
5745  014706                          4$:     ENDSEG
5746  014706                          10000$:
5747  014706  104405                          TRAP    C$ESEG
5748  014710  005237  006376                  INC     TRADRS                  ;UPDATE THE ADDRESS BY ONE
5749  014714  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES CHECKED
5750  014722  001720                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5751  014724                                  ENDSUB
5752  014724                          L10106:
5753  014724  104403                          TRAP    C$ESUB
5754  014726                                  ENDTST
5755  014726                          L101.3:
5756  014726  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 28: TRAM ADDRESS/SHORT TEST - TRDI 55:48

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM TRDI 55:48 TO BE ADDRESSED CORRECTLY AND THAT
                                ; NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIP'S. THE TEST WILL
                                ; LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE
                                ; ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK THE ADDRESS TO CONTAIN ITS
                                ; ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO
                                ; THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN.  THE TEST WILL
                                ; REPEAT THIS SEQUENCE FOR ALL ADDRESSES IN THE TRACE RAM.  WHEN ALL ADDRESSES
                                ; HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK ALL OF THE RAM TO CONTAIN THE
                                ; ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
                                ;--

014730                                  BGNTST
014730                          T28::
014730  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        ;THE FOLLOWING SUB TEST WILL WRITE EACH LOCATION OF TRACE RAM TRDI 55:48
                                        ;WITH A DATA PATTERN EQUAL TO ITS ADDRESS.  AS EACH LOCATION IS WRITTEN,
                                        ;THE TEST WILL READ THE LOCATION AND CHECK THAT THE DATA EQUALS ITS
                                        ;ADDRESS.

014734                                  BGNSUB
014734                          T28.1:
014734  104402                          TRAP    C$BSUB
014736  005037  006376                   CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
014742                          1$:     BGNSEG
014742  104404                          TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING A ZERO
                                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE
                                        ;RAM DATA IN BUFFERS.

014744  105037  002370                   CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
014750  004737  006104                   JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
014754  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
014756                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
014756  104455                          TRAP    C$ERDF
014760  000001                          .WORD   1
014762  000000                          .WORD   0
014764  004606                          .WORD   ROEROR
014766                                  CKLOOP
014766  104406                          TRAP    C$CLP1

                                        ;WRITE AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF LOCA-
                                        ;TION "TRADRS". THE POINTER REGISTER ON EXIT FROM ROUTINE TRADLD WILL
                                        ;HAVE THE SIGNAL PTER0 L ASSERTED.

014770  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;WRITE THE TRACE RAM ADDRESS INTO THE TRACE RAM DATA IN BUFFERS IN
                                        ;BUFFER BITS TRDI 59:48. ON EXIT FROM ROUTINE "TRDIBF" THE POINTER
                                        ;REGISTER WILL HAVE THE SIGNAL PTER4 L ASSERTED.
```

```
5813
5814  014774  013737  006376  002414          MOV     TRADRS,R6LOAD           ;SETUP DATA TO EQUAL TRAM ADDRESS REG
5815  015002  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5816  015006  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 55:48
5817
5818                                          ;WRITE THE ADDRESS IN THE TRACE RAM DATA IN BUFFERS INTO TRACE RAM
5819                                          ;BITS TRDI 55:48
5820
5821  015010  012777  000000  165340          MOV     #0,@REG6                ;WRTIE RAM WITH DATA IN BUFFERS
5822
5823                                          ;SET CDAL2 TO 1 AND CDAL3 TO 0 IN CONTROL REGISTER 0 TO SET THE SIGNAL
5824                                          ;TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW THE DATA IN THE TRACE RAM TO
5825                                          ;BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT4 H.
5826
5827  015016  052737  000004  002370          BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5828  015024  004737  006104                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
5829  015030  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5830  015032                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5831  015032  104455                          TRAP    C$ERDF
5832  015034  000001                          .WORD   1
5833  015036  000000                          .WORD   0
5834  015040  004606                          .WORD   ROEROR
5835  015042                                  CKLOOP
5836  015042  104406                          TRAP    C$CLP1
5837
5838                                          ;READ AND CHECK TRACE RAM DATA TRDI 55:48.  THE DATA SHOULD EQUAL THE
5839                                          ;ADDRESS BEING TESTED.
5840
5841  015044  017737  165306  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM TRDI 55:48
5842  015052  042737  177400  002420          BIC     #177400,R6READ          ;CLEAR BITS NOT AVAILABLE IN TRACE RAM
5843  015060  042737  177400  002414          BIC     #177400,R6LOAD          ;ONLY 8 BITS WERE LOADED, 0 TOP 4 BITS
5844  015066  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED TO EQUAL DATA READ
5845  015074  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
5846  015076                                  ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR - TRDI 55:48
5847  015076  104455                          TRAP    C$ERDF
5848  015100  000004                          .WORD   4
5849  015102  003126                          .WORD   TRAM55
5850  015104  004766                          .WORD   TRAMER
5851  015106                          4$:     ENDSEG
5852  015106                          10000$:
5853  015106  104405                          TRAP    C$ESEG
5854  015110  005237  006376                  INC     TRADRS                  ;UPDATE TRACE RAM ADDRESS BY 1
5855  015114  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF 1K YET
5856  015122  001707                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
5857  015124                                  ENDSUB
5858  015124                          L10110:
5859  015124  104403                          TRAP    C$ESUB
5860
5861                                          ;THE FOLLOWING SUB TEST WILL RESET THE POINTER TO THE BEGINNING
5862                                          ;ADDRESS OF THE TRACE RAM, CHECK THE LOCATION TO EQUAL ITS ADDRESS,
5863                                          ;WRITE,READ, AND CHECK THE LOCATION WITH THE ONES COMPLEMENT OF ITS
5864                                          ;ADDRESS. THIS SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE TRACE
5865                                          ;RAM FOR TRACE RAM TRDI 55:48. THIS TEST WILL CHECK THAT THE TRACE RAM
5866                                          ;CAN BE ADDRESSED CORRECTLY AND THAT WRITING A LOCATION DOES NOT WRITE
5867                                          ;A HIGHER LOCATION.
5868
```

```
5869  015126                                  BGNSUB
5870  015126                          T28.2:
5871  015126  104402                          TRAP    C$BSUB
5872  015130  005037  006376                  CLR     TRADRS                  ;RESET TRAM ADDRESS TO ADDRESS 0
5873
5874  015134                          1$:     BGNSEG
5875  015134  104404                          TRAP    C$BSEG
5876
5877                                          ;SET CDAL2 TO A 1 AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5878                                          ;SIGNAL TRSL1 L. THIS SIGNAL WILL ALLOW THE TRACE RAM TO BE READ ON A
5879                                          ;READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT4 H.
5880
5881  015136  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5882  015144  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
5883  015150  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5884  015152                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5885  015152  104455                          TRAP    C$ERDF
5886  015154  000001                          .WORD   1
5887  015156  000000                          .WORD   0
5888  015160  004606                          .WORD   R0EROR
5889  015162                                  CKLOOP
5890  015162  104406                          TRAP    C$CLP1
5891
5892                                          ;GO LOAD ADDRESS TO BE CHECKED INTO TRACE RAM ADDRESS REGISTER USING
5893                                          ;THE CONTENTS OF LOCATION "TRADRS" AS THE ADDRESS TO BE LOADED. ON
5894                                          ;EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER WILL HAVE THE SIGNAL
5895                                          ;PTER0 L ASSERTED.
5896
5897  015164  004737  006312          2$:     JSR     PC,TRADLD               ;GO LOAD,READ & CHECK TRAM ADDRESS REG
5898
5899                                          ;SET THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5900
5901  015170  012737  000004  002376          MOV     #PTER4,R2LOAD           ;SETUP REGISTER 2 BITS TO BE LOADED
5902  015176  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5903  015202  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5904  015204                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5905  015204  104455                          TRAP    C$ERDF
5906  015206  000002                          .WORD   2
5907  015210  000000                          .WORD   0
5908  015212  004706                          .WORD   R2EROR
5909  015214                                  CKLOOP
5910  015214  104406                          TRAP    C$CLP1
5911
5912                                          ;READ THE DATA THAT WAS PREVIOUSLY WRITTEN IN THE FIRST SUB TEST AND
5913                                          ;CHECK THAT THE DATA IS EQUAL TO THE ADDRESS BEING TESTED.
5914
5915  015216  013737  006376  002414  3$:     MOV     TRADRS,R6LOAD           ;SETUP DATA PREVIOUSLY WRITTEN
5916  015224  017737  165126  002420          MOV     @REG6,R6READ            ;READ THE DATA FROM THE TRACE RAM
5917  015232  042737  177400  002414          BIC     #177400,R6LOAD          ;ONLY 8 BITS OF ADDRESS WAS LOADED
5918  015240  042737  177400  002420          BIC     #177400,R6READ          ;CLEAR BITS THAT ARE NOT VALID
5919  015246  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK IF DATA IS EQUAL TO ITS ADDRESS
5920  015254  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5921  015256                                  ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR - TRDI 55:48 OR ADDRESS
5922  015256  104455                          TRAP    C$ERDF
5923  015260  000004                          .WORD   4
5924  015262  003126                          .WORD   TRAM55
```

```
5925  015264  004766                          .WORD   TRAMER
5926                                                                ;FAILURE OR ADDRESS SHORT
5927  015266                          4$:     ENDSEG
5928  015266                          10000$:
5929  015266  104405                          TRAP    C$ESEG
5930
5931                                          ;THE FOLLOWING SECTION OF CODE WILL WRITE THE TRACE RAM DATA IN BUFFERS
5932                                          ;AND THE TRACE RAM WITH THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
5933
5934  015270                                  BGNSEG
5935  015270  104404                          TRAP    C$BSEG
5936
5937                                          ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
5938                                          ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
5939
5940  015272  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOWER BYTE
5941  015276  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
5942  015302  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
5943  015304                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5944  015304  104455                          TRAP    C$ERDF
5945  015306  000001                          .WORD   1
5946  015310  000000                          .WORD   0
5947  015312  004606                          .WORD   R0EROR
5948  015314                                  CKLOOP
5949  015314  104406                          TRAP    C$CLP1
5950
5951                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 59:48 WITH DATA
5952                                          ;EQUAL TO THE ONES COMPLEMENT OF THE ADDRESS. ON EXIT FROM ROUTINE
5953                                          ;"TRDIBF", THE POINTER REGISTER WILL HAVE THE SIGNAL PTER4 L ASSERTED.
5954
5955  015316  013737  006376  002414  5$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS UNDER TEST
5956  015324  005137  002414                  COM     R6LOAD                  ;COMPLEMENT THE ADDRESS
5957  015330  042737  170000  002414          BIC     #170000,R6LOAD          ;CLEAR TOP 4 BITS WHICH NOT AVAILABLE
5958  015336  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5959  015342  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 55:48
5960
5961                                          ;WRITE TRACE RAM LOCATION WITH DATA PATTERN EQUAL TO THE COMPLEMENT
5962                                          ;OF ITS ADDRESS.  THE DATA TO BE WRITTEN INTO THE TRACE RAM IS
5963                                          ;STORED IN THE TRACE RAM DATA IN BUFFERS TRDI 55:48.
5964
5965  015344  012777  000000  165004          MOV     #0,@REG6                ;WRITE RAM WITH TRAM DATA IN BUF
5966
5967                                          ;SET CDAL2 TO A 1 AND CDAL 3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5968                                          ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
5969                                          ;BITS TRDI 55:48 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
5970                                          ;THE SIGNAL RPT4 H.
5971
5972  015352  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5973  015360  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
5974  015364  001405                          BEQ     6$                      ;IF LOADEDOK THEN CONTINUE
5975  015366                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5976  015366  104455                          TRAP    C$ERDF
5977  015370  000001                          .WORD   1
5978  015372  000000                          .WORD   0
5979  015374  004606                          .WORD   R0EROR
5980  015376                                  CKLOOP
```

```
5981  015376  104406                          TRAP    C$CLP1
5982
5983                                          ;READ DATA FROM THE TRACE RAM TRDI 55:48 CHECKING THE DATA TO BE THE
5984                                          ;ONES COMPLEMENT OF THE ADDRESS UNDER TEST
5985
5986  015400  017737  164752  002420  6$:     MOV     @REG6,R6READ            ;READ DATA FROM THE TRACE RAM
5987  015406  042737  177400  002420          BIC     #177400,R6READ          ;CLEAR BITS NOT AVIALABLE
5988  015414  042737  177400  002414          BIC     #177400,R6LOAD          ;CLEAR BITS THAT WERE NOT LOADED
5989  015422  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5990  015430  001404                          BEQ     7$                      ;ID DATA EQUAL THEN CONTINUE
5991  015432                                  ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR - TRDI 55:48
5992  015432  104455                          TRAP    C$ERDF
5993  015434  000004                          .WORD   4
5994  015436  003126                          .WORD   TRAM55
5995  015440  004766                          .WORD   TRAMER
5996  015442                          7$:     ENDSEG
5997  015442                          10001$:
5998  015442  104405                          TRAP    C$ESEG
5999  015444  005237  006376                  INC     TRADRS                  ;UPDATE THE ADDRESS BY 1
6000  015450  032737  002000  006376          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES BEEN TESTED
6001  015456  001626                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
6002  015460                                  ENDSUB
6003  015460                          L10111:
6004  015460  104403                          TRAP    C$ESUB
6005
6006                                          ;THE FOLLOWING SUB TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING
6007                                          ;ADDRESS OF THE TRACE RAM AND CHECK EACH LOCATION OF THE TRACE RAM TO
6008                                          ;CONTAIN THE ONES COMPLEMENT OF ITS ADDRESS. IN A FAILURE OCCURS, THE
6009                                          ;ERROR MAY BE AN ADDRESS SHORT IN WHICH WRITING A LOCATION IN THE
6010                                          ;PREVIOUS SUB TEST WROTE A LOCATION LOWER THEN THE ADDRESS BEING TESTED.
6011
6012  015462                                  BGNSUB
6013  015462                          T28.3:
6014  015462  104402                          TRAP    C$BSUB
6015  015464  005037  006376                  CLR     TRADRS                  ;CLEAR THE ADDRESS TO ADDRESS 0
6016
6017  015470                          1$:     BGNSEG
6018  015470  104404                          TRAP    C$BSEG
6019
6020                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO ASSERT
6021                                          ;THE SIGNAL TRSL1 L.  THE SIGNAL TRSL1 L WILL ALLOW THE DATA FROM THE
6022                                          ;TRACE RAM BITS TRDI 55:48 TO BE READ ON A READ COMMAND TO CONTROL
6023                                          ;REGISTER 6 VIA THE SIGNAL RPT4 H.
6024
6025  015472  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
6026  015500  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
6027  015504  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
6028  015506                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
6029  015506  104455                          TRAP    C$ERDF
6030  015510  000001                          .WORD   1
6031  015512  000000                          .WORD   0
6032  015514  004606                          .WORD   ROEROR
6033  015516                                  CKLOOP
6034  015516  104406                          TRAP    C$CLP1
6035
6036                                          ;LOAD,READ AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF
```

```
6037                                            ;LOCATION "TRADRS".  ON EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER
6038                                            ;WILL HAVE THE SIGNAL PTER0 L ASSERTED.
6039
6040  015520  004737  006312          2$:       JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
6041
6042                                            ;SET SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
6043
6044  015524  012737  000004  002376            MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
6045  015532  004737  006136                    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
6046  015536  001405                            BEQ     3$                      ;IF DATA OK THEN CONTINUE
6047  015540                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
6048  015540  104455                            TRAP    C$ERDF
6049  015542  000002                            .WORD   2
6050  015544  000000                            .WORD   0
6051  015546  004706                            .WORD   R2EROR
6052  015550                                    CKLOOP
6053  015550  104406                            TRAP    C$CLP1
6054
6055                                            ;READ DATA PREVIOUSLY WRITTEN IN THE LAST SUB TEST CHECKING THE DATA
6056                                            ;TO BE THE COMPLEMENT OF THE ADDRESS.
6057
6058  015552  013737  006376  002414  3$:       MOV     TRADRS,R6LOAD           ;GET THE ADDRESS BEING TESTED
6059  015560  005137  002414                    COM     R6LOAD                  ;MAKE IT THE ONES COMPLEMENT
6060  015564  042737  177400  002414            BIC     #177400,R6LOAD          ;CLEAR BITS THAT WERE NOT LOADED
6061  015572  017737  164560  002420            MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM
6062  015600  042737  177400  002420            BIC     #177400,R6READ          ;CLEAR BITS THAT ARE NOT AVAILABLE
6063  015606  023737  002414  002420            CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
6064  015614  001404                            BEQ     4$                      ;IF DATA OK THEN CONTINUE
6065  015616                                    ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR - TRDI 55:48
6066  015616  104455                            TRAP    C$ERDF
6067  015620  000004                            .WORD   4
6068  015622  003126                            .WORD   TRAM55
6069  015624  004766                            .WORD   TRAMER
6070  015626                            4$:     ENDSEG
6071  015626                            10000$:
6072  015626  104405                            TRAP    C$ESEG
6073  015630  005237  006376                    INC     TRADRS                  ;UPDATE THE ADDRESS BY ONE
6074  015634  032737  002000  006376            BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES CHECKED
6075  015642  001712                            BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
6076  015644                                    ENDSUB
6077  015644                            L10112:
6078  015644  104403                            TRAP    C$ESUB
6079  015646                                    ENDTST
6080  015646                            L10107:
6081  015646  104401                            TRAP    C$ETST
6082
```

```
                                .SBTTL  TEST 29: TRAM ADDRESS REG COUNT UP TEST - TRAD 10:0

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN COUNT UP BY
                                ; ONE WHEN THE SIGNAL CTR L IS PULSED.  THE TRACE RAM ADDRESS REGISTER WILL BE
                                ; COUNTED UP BY ONE FROM THE ADDRESS 0 TO ADDRESS 3777 AND THEN BACK TO 0.  IN
                                ; ORDER TO PULSE THE SIGNAL CTR L, THE PROGRAM WILL SET AND CLEAR THE SIGNAL
                                ; CDAL6 IN CONTROL REGISTER 0 WHICH WILL CAUSE THE SIGNALS TRANST H AND TRST L
                                ; TO PULSE.  THIS WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE
                                ; THE SIGNAL ORST L TO PULSE.  WITH THE TRACING FLIP-FLOP HELD IN THE PRESET
                                ; STATE BY THE SIGNAL PDAL6 BEING A ONE AND THE SIGNALS TRANST H AND TRST L
                                ; BEING PULSED, A PULSE WILL OCCUR ON THE SIGNAL CTR L.
                                ;--

015650                                  BGNTST
015650                          T29::

015650  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

015654                                  BGNSEG
015654  104404                          TRAP    C$BSEG

                                ;SETUP CONTROL REGISTER 2 SO THAT THE SIGNAL PTERO L WILL BE ASSERTED
                                ;IN THE POINTER REGISTER.  WHEN THE SIGNAL PTERO L IS ASSERTED AND A
                                ;READ COMMAND IS ISSUED TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON
                                ;THE SIGNAL RPTO H. THE SIGNAL RPTO H WILL CAUSE THE TRACE RAM ADDRESS
                                ;REGISTER TO BE READ.  PDAL6 BEING A ONE IN CONTROL REGISTER 2 WILL
                                ;PRESET THE OUTPUT OF THE TRACING FLIP-FLOP TO A HIGH CONDITION.

015656  012737  000100  002376          MOV     #PDAL6!PTERO,R2LOAD     ;SETUP BITS TO LOAD IN CONTROL REG 2
015664  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECH REG 2
015670  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
015672                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL TO 0
015672  104455                          TRAP    C$ERDF
015674  000002                          .WORD   2
015676  000000                          .WORD   0
015700  004706                          .WORD   R2EROR
015702                                  CKLOOP
015702  104406                          TRAP    C$CLP1

                                ;SET AND CLEAR THE SIGNAL CDAL0 IN CONTROL REGISTER 0. THIS IS DONE TO
                                ;CLEAR THE TRACE RAM ADDRESS REGISTER TO ADDRESS 0.

                                ;SET THE SIGNAL CDAL0 TO A ONE

015704  112737  000001  002370  1$:     MOVB    #CDAL0,R0LOAD           ;SETUP BIT TO BE LOADED
015712  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REG 0
015716  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
015720                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
015720  104455                          TRAP    C$ERDF
015722  000001                          .WORD   1
015724  000000                          .WORD   0
015726  004606                          .WORD   R0EROR
015730                                  CKLOOP
015730  104406                          TRAP    C$CLP1
```

```
6139                                                    ;CLEAR THE SIGNAL CDALO IN CONTROL REGISTER 0
6140
6141  015732  105037  002370          2$:     CLRB    R0LOAD                  ;SETUP TO CLEAR CDALO
6142  015736  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
6143  015742  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
6144  015744                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
6145  015744  104455                          TRAP    C$ERDF
6146  015746  000001                          .WORD   1
6147  015750  000000                          .WORD   0
6148  015752  004606                          .WORD   R0EROR
6149  015754                                  CKLOOP
6150  015754  104406                          TRAP    C$CLP1
6151
6152                                                    ;READ TRACE RAM ADDRESS REGISTER CHECKING THAT THE SIGNAL CDALO CLEARED
6153                                                    ;ALL BITS IN THE TRACE RAM ADDRESS REGISTER.
6154
6155  015756  005037  002414          3$:     CLR     R6LOAD                  ;SETUP EXPECTED CONTENTS
6156  015762  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
6157  015770  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK TRACE RAM ADDRESS REG
6158  015774  001405                          BEQ     4$                      ;IF TRAM ADDRESS REG EQUALS 0 THEN CONT
6159  015776                                  ERRDF   4,TRADER,R026ER         ;CDALO FAILED TO 0 TRAM ADDRESS REGISTER
6160  015776  104455                          TRAP    C$ERDF
6161  016000  000004                          .WORD   4
6162  016002  002464                          .WORD   TRADER
6163  016004  004736                          .WORD   R026ER
6164  016006                                  CKLOOP
6165  016006  104406                          TRAP    C$CLP1
6166
6167                                                    ;THE FOLLOWING SECTION OF CODE WILL BE EXECUTED FOR EACH ADDRESS OF THE
6168                                                    ;TRACE RAM ADDRESS REGISTER.  THE ADDRESS REGISTER WILL BE INCREMENTED
6169                                                    ;BY ONE VIA THE SIGNAL "CTR L" EACH TIME THE SIGNAL CDAL6 IS SET AND
6170                                                    ;CLEARED.
6171
6172                                                    ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0. SETTING AND
6173                                                    ;CLEARING THE SIGNAL CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L
6174                                                    ;TO PULSE.  THIS WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL
6175                                                    ;CAUSE THE SIGNAL ORST L TO PULSE.  WITH THE TRACING FLIP-FLOP HELD IN
6176                                                    ;THE PRESET STATE BY THE SIGNAL PDAL6 BEING A ONE AND THE SIGNALS
6177                                                    ;TRANST H AND TRST L BEING PULSED, A PULSE WILL OCCUR ON THE SIGNAL
6178                                                    ;CTR L.  THE SIGNAL CTR L WILL CAUSE THE TRACE RAM ADDRESS REGISTER TO
6179                                                    ;COUNT UP BY ONE ADDRESS.
6180
6181  016010  004737  006642          4$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
6182
6183                                                    ;CHECK THAT THE SIGNAL CTR L INCREMENTED THE TRACE RAM ADDRESS REGISTER
6184                                                    ;BY ONE.
6185
6186  016014  005237  002414          6$:     INC     R6LOAD                  ;UPDATE THE EXPECTED ADDRESS BY ONE
6187  016020  042737  174000  002414          BIC     #174000,R6LOAD          ;ALLOW WRAP AROUND TO ZERO
6188  016026  004737  006260                  JSR     PC,READR6               ;READ AND CHECK TRACE RAM ADDRESS REG
6189  016032  001405                          BEQ     7$                      ;IF ADDRESS INCREMENTED THEN CONTINUE
6190  016034                                  ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO INCREMENT TRAM ADDRESS REG
6191  016034  104455                          TRAP    C$ERDF
6192  016036  000004                          .WORD   4
6193  016040  002464                          .WORD   TRADER
6194  016042  004736                          .WORD   R026ER
```

```
 6195  016044                                  CKLOOP
 6196  016044  104406                          TRAP    C$CLP1
 6197  016046  005737  002414          7$:     TST     R6LOAD          ;CHECK IF BACK TO ADDRESS 0
 6198  016052  001356                          BNE     4$              ;IF NOT THEN INCREMENT ADDRESS AGAIN
 6199  016054                                  ENDSEG
 6200  016054                          10000$:
 6201  016054  104405                          TRAP    C$ESEG
 6202  016056                                  ENDTST
 6203  016056                          L10113:
 6204  016056  104401                          TRAP    C$ETST
 6205
```

```
                                .SBTTL  TEST 30: SET/CLEAR TRACING F/F TEST VIA PDAL6 + CDAL0

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET BY PDAL6 IN
                                ; CONTROL REGISTER 2 AND CLEARED BY CDAL0 IN CONTROL REGISTER 0.
                                ;
                                ; TO CHECK THAT THE TRACING FLIP-FLOP CAN BE SET, THE PROGRAM WILL SET PDAL6
                                ; TO A ONE IN CONTROL REGISTER 2 WHICH WILL CAUSE THE OUTPUT OF THE TRACING
                                ; FLIP-FLOP TO BE SET HIGH. THE TEST WILL THEN CLEAR PDAL6 IN CONTROL REGISTER
                                ; 2.  THE TRACE RAM ADDRESS REGISTER WILL THEN BE LOADED AND CHECKED WITH THE
                                ; ADDRESS 1775. THE TEST WILL THEN SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL
                                ; REGISTER 0.  SETTING AND CLEARING CDAL6 IN CONTROL REGISTER 0 WILL CAUSE THE
                                ; SIGNALS TRANST H AND TRST L TO PULSE.  THIS WILL THEN CAUSE THE SIGNAL
                                ; ANST L TO PULSE WHICH WILL THEN CAUSE THE SIGNAL ORST L TO PULSE.  WITH THE
                                ; TRACING FLIP-FLOP PRESET HIGH AND THE SIGNALS TRANST H AND TRST L BEING PULSED
                                ; A PULSE WILL OCCUR ON THE SIGNAL CTR L.  THE SIGNAL CTR L WILL CAUSE THE
                                ; TRACE RAM ADDRESS REGISTER TO INCREMENT BY ONE.  THE TEST WILL CHECK THE TRACE
                                ; RAM ADDRESS REGISTER TO BE INCREMENTED BY ONE TO ADDRESS 1776.  THE TEST WILL
                                ; THEN SET AND CLEAR THE SIGNAL CDAL0 IN CONTROL REGISTER 0.  THE SIGNAL CDAL0
                                ; WILL CLEAR THE TRACE RAM ADDRESS REGISTER AND THE TRACING FLIP-FLOP.  TO
                                ; CHECK THAT THE TRACE RAM ADDRESS REGISTER WAS CLEARED, THE TEST WILL READ
                                ; THE TRACE RAM ADDRESS REGISTER CHECKING IT TO BE 0.  TO CHECK THAT THE
                                ; TRACING FLIP-FLOP CLEARED, THE TEST WILL AGAIN SET AND CLEAR THE SIGNAL
                                ; CDAL6 IN CONTROL REGISTER 0.  WHEN THE TRACING FLIP-FLOP IS CLEARED AND THE
                                ; SIGNALS TRANST H AND TRST L ARE PULSED, A PULSE SHOULD NOT OCCUR ON THE SIGNAL
                                ; CTR L, THUS, THE TRACE RAM ADDRESS REGISTER SHOULD NOT BE INCREMENTED.  THE
                                ; TEST WILL READ THE TRACE RAM ADDRESS REGISTER CHECKING IT TO BE ZERO.  THE
                                ; TEST WILL SET AND CLEAR THE SIGNAL CDAL6 AGAIN TO CHECK THAT THE DATA LEAD
                                ; TO THE TRACING FLIP-FLOP WAS NOT CLOCKED INTO THE TRACING FLIP-FLOP AS A ONE
                                ; OR HIGH STATE.  THE TEST WILL READ THE TRACE RAM ADDRESS AGAIN VALIDATING THE
                                ; ADDRESS TO BE ZERO.  THE TEST WILL NOW SET THE SIGNAL PDAL6 IN CONTROL REGIS-
                                ; TER 2 TO PRESET THE TRACING FLIP-FLOP TO A HIGH STATE.  THE SIGNAL CDAL6 IN
                                ; CONTROL REGISTER 0 WILL THEN BE SET AND CLEARED.  WITH THE SIGNALS TRANST H
                                ; AND TRST L BEING PULSED AND THE TRACING FLIP-FLOP IN THE PRESET STATE, A
                                ; PULSE WILL OCCUR ON THE SIGNAL CTR L WHICH WILL CAUSE THE TRACE RAM ADDRESS
                                ; REGISTER TO BE INCREMENTED BY ONE.  THE TEST WILL READ THE TRACE RAM ADDRESS
                                ; REGISTER CHECKING THE ADDRESS TO EQUAL 1.
                                ;--

016060                                  BGNTST
016060                          T30::
016060  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

016064                                  BGNSEG
016064  104404                          TRAP    C$BSEG

                                        ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO CLEAR ANY BITS THAT MAY BE
                                        ;SET WHEN LOOPING ON AN ERROR.

016066  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR ALL LOW BITS
016072  004737  006104                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
016076  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
016100                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
016100  104455                          TRAP    C$ERDF
016102  000001                          .WORD   1
016104  000000                          .WORD   0
```

```
6262  016106  004606                          .WORD   R0EROR
6263  016110                                  CKLOOP
6264  016110  104406                          TRAP    C$CLP1
6265
6266                                          ;PRESET THE TRACING FLIP-FLOP BY SETTING PDAL6 TO A 1. THE OUTPUT OF
6267                                          ;THE TRACING FLIP-FLOP SHOULD BE SET HIGH.  WITH PDAL BITS 3-0 SET TO
6268                                          ;ZERO, THE SIGNAL PTERO L WILL BE ASSERTED IN THE POINTER REGISTER.
6269                                          ;PDAL5 ON A ZERO WILL HOLD THE FUNCTION SELECT F/F'S TO A 0 STATE (LOW).
6270
6271  016112  012737  000100  002376  1$:     MOV     #PDAL6!PTERO,R2LOAD     ;SETUP BITS TO BE LOADED
6272  016120  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
6273  016124  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
6274  016126                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
6275  016126  104455                          TRAP    C$ERDF
6276  016130  000002                          .WORD   2
6277  016132  000000                          .WORD   0
6278  016134  004706                          .WORD   R2EROR
6279  016136                                  CKLOOP
6280  016136  104406                          TRAP    C$CLP1
6281
6282                                          ;RELEASE THE PRESET SIDE OF THE TRACING FLIP-FLOP BY SETTING PDAL6 TO 0
6283
6284  016140  042737  000100  002376  2$:     BIC     #PDAL6,R2LOAD           ;SETUP BIT TO BE CLEARED
6285  016146  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
6286  016152  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
6287  016154                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
6288  016154  104455                          TRAP    C$ERDF
6289  016156  000002                          .WORD   2
6290  016160  000000                          .WORD   0
6291  016162  004706                          .WORD   R2EROR
6292  016164                                  CKLOOP
6293  016164  104406                          TRAP    C$CLP1
6294
6295                                          ;LOAD ADDRESS 1775 INTO TRACE RAM ADDRESS REGISTER
6296
6297  016166  012737  001775  002414  3$:     MOV     #1775,R6LOAD            ;SETUP ADDRESS TO BE LOADED
6298  016174  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP MASK TO IGNORE UNUSED BITS
6299  016202  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD,READ AND CHECK TRAM ADDR REG
6300  016206  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
6301  016210                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQUAL 1775
6302  016210  104455                          TRAP    C$ERDF
6303  016212  000004                          .WORD   4
6304  016214  002464                          .WORD   TRADER
6305  016216  004736                          .WORD   R026ER
6306  016220                                  CKLOOP
6307  016220  104406                          TRAP    C$CLP1
6308
6309                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. SETTING AND CLEARING
6310                                          ;CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE.  THIS WILL
6311                                          ;THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE THE SIGNAL
6312                                          ;ORST L TO PULSE.  WITH THE TRACING FLIP-FLOP PRESET AND THE SIGNALS
6313                                          ;TRANST H AND TRST L BEING PULSED, A PULSE WILL OCCUR ON THE SIGNAL
6314                                          ;CTR L WHICH WILL CAUSE THE TRACE RAM ADDRESS REGISTER TO BE COUNTED
6315                                          ;UP BY ONE.
6316
6317  016222  004737  006642          4$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
```

```
6318
6319                                        ;CHECK THAT THE SIGNAL "CTR L" UPDATED THE TRACE RAM ADDRESS REGISTER
6320
6321  016226  005237  002414        6$:     INC     R6LOAD                  ;UPDATE THE EXPECTED ADDRESS TO 1776
6322  016232  004737  006260                JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
6323  016236  001405                        BEQ     7$                      ;IF UPDATED BY ONE THEN CONTINUE
6324  016240                                ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO UPDATE ADDRESS BY ONE
6325  016240  104455                        TRAP    C$ERDF
6326  016242  000004                        .WORD   4
6327  016244  002464                        .WORD   TRADER
6328  016246  004736                        .WORD   R026ER
6329  016250                                CKLOOP
6330  016250  104406                        TRAP    C$CLP1
6331
6332                                        ;SET AND CLEAR CDAL0 IN CONTROL REGISTER 0 TO CHECK THAT CDAL0 WILL
6333                                        ;CLEAR THE TRACE RAM ADDRESS REGISTER AND THE TRACING FLIP-FLOP.
6334
6335  016252  052737  000001  002370  7$:     BIS     #CDAL0,R0LOAD           ;SETUP BIT TO BE SET
6336  016260  004737  006104                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
6337  016264  001405                        BEQ     8$                      ;IF LOADED OK THEN CONTINUE
6338  016266                                ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
6339  016266  104455                        TRAP    C$ERDF
6340  016270  000001                        .WORD   1
6341  016272  000000                        .WORD   0
6342  016274  004606                        .WORD   R0EROR
6343  016276                                CKLOOP
6344  016276  104406                        TRAP    C$CLP1
6345
6346                                        ;CLEAR THE SIGNAL CDAL0 IN CONTROL REGISTER 0
6347
6348  016300  042737  000001  002370  8$:     BIC     #CDAL0,R0LOAD           ;SETUP BIT TO BE CLEARED
6349  016306  004737  006104                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
6350  016312  001405                        BEQ     9$                      ;IF LOADED OK THEN CONTINUE
6351  016314                                ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQULA EXPECTED
6352  016314  104455                        TRAP    C$ERDF
6353  016316  000001                        .WORD   1
6354  016320  000000                        .WORD   0
6355  016322  004606                        .WORD   R0EROR
6356  016324                                CKLOOP
6357  016324  104406                        TRAP    C$CLP1
6358
6359                                        ;READ TRACE RAM ADDRESS REGISTER CHECKING THAT THE SIGNAL CDAL0
6360                                        ;CLEARED THE TRACE RAM ADDRESS REGISTER.
6361
6362  016326  005037  002414        9$:     CLR     R6LOAD                  ;SET EXPECTED ADDRESS TO BE 0
6363  016332  004737  006260                JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
6364  016336  001405                        BEQ     10$                     ;IF ADDRESS EQUALS 0 THEN CONTINUE
6365  016340                                ERRDF   4,TRADER,R026ER         ;CDAL0 FAILED TO CLEAR TRAM ADDR REG
6366  016340  104455                        TRAP    C$ERDF
6367  016342  000004                        .WORD   4
6368  016344  002464                        .WORD   TRADER
6369  016346  004736                        .WORD   R026ER
6370  016350                                CKLOOP
6371  016350  104406                        TRAP    C$CLP1
6372
6373                                        ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0 TO CHECK THAT THE
```

```
                                        ;SIGNAL CDAL0 CLEARED THE TRACING FLIP-FLOP. NO PULSE SHOULD OCCUR
                                        ;ON THE SIGNAL CTR L, THEREFORE, THE TRACE RAM ADDRESS REGISTER
                                        ;SHOULD NOT BE UPDATED WHEN THE SIGNALS TRANST H AND TRST L ARE PULSED.

016352  004737  006642        10$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0

                                        ;READ TRACE RAM ADDRESS REGISTER AGAIN CHECKING THAT THE TRACE ADDRESS
                                        ;REGISTER DID NOT INCREMENT WHEN THE TRACING FLIP-FLOP WAS IN A 0
                                        ;STATE. THE TRACING FLIP-FLOP WAS CLEARED PREVIOUSLY VIA THE SIGNAL CDAL0.

016356  004737  006260        12$:    JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRS REGISTER
016362  001405                        BEQ     13$                     ;IF ADDRESS STILL 0 THEN CONTINUE
016364                                ERRDF   4,TRADER,R026ER         ;TRACING F/F FIALED TO 0 VIA CDAL0
016364  104455                        TRAP    C$ERDF
016366  000004                        .WORD   4
016370  002464                        .WORD   TRADER
016372  004736                        .WORD   R026ER
016374                                CKLOOP
016374  104406                        TRAP    C$CLP1
                                                                        ;OR PULSE ISSUED ON SIGNAL CTR L

                                        ;CLOCK CDAL6 AGAIN TO CHECK THAT THE DATA INPUT LEAD TO THE TRACING
                                        ;FLIP-FLOP WAS NOT HIGH + THAT THE TRACING FLIP-FLOP DID NOT GET SET.

016376  004737  006642        13$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0

                                        ;READ THE TRACE RAM ADDRESS REGISTER AGAIN CHECKING THAT THE ADDRESS
                                        ;REGISTER DID NOT INCREMENT WHEN THE TRACING FLIP-FLOP WAS IN THE
                                        ;ZERO STATE.  IF THE ADDRESS DID CHANGE, CHECK THE DATA INPUT LEAD
                                        ;TO THE TRACING FLIP-FLOP. IT SHOULD BE AT A LOW LEVEL.

016402  004737  006260        15$:    JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
016406  001405                        BEQ     16$                     ;IF ADDRESS STILL 0 THEN CONTINUE
016410                                ERRDF   4,TRADER,R026ER         ;TRACING FLIP-FLOP GOT SET
016410  104455                        TRAP    C$ERLF
016412  000004                        .WORD   4
016414  002464                        .WORD   TRADER
016416  004736                        .WORD   R026ER
016420                                CKLOOP
016420  104406                        TRAP    C$CLP1

                                        ;SET PDAL6 TO A 1 IN CONTROL REGISTER 2 TO PRESET THE TRACING FLIP-FLOP
                                        ;TO A ONE. WHEN THE TRACING FLIP-FLOP IS PRESET AND THE SIGNAL CDAL6 IS
                                        ;TOGGLED, A PULSE WILL OCCUR ON THE SIGNAL CTR L WHICH SHOULD INCREMENT
                                        ;THE TRACE RAM ADDRESS REGISTER.

016422  052737  000100  002376  16$:    BIS     #PDAL6,R2LOAD           ;SETUP TO CLEAR PDAL6
016430  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD,READ AND CHECK REGISTER 2
016434  001405                        BEQ     17$                     ;IF LOADED OK THEN CONTINUE
016436                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
016436  104455                        TRAP    C$ERDF
016440  000002                        .WORD   2
016442  000000                        .WORD   0
016444  004706                        .WORD   R2EROR
016446                                CKLOOP
016446  104406                        TRAP    C$CLP1
```

```
6430
6431                                        ;CLOCK SIGNAL CDAL6 TO CAUSE A PULSE TO OCCUR ON THE SIGNAL CTR L WHEN
6432                                        ;THE TRACING FLIP-FLOP IS PRESET
6433
6434  016450  004737  006642        17$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
6435
6436                                        ;CHECK THAT THE TRACE RAM ADDRESS REGISTER WAS INCREMENTED BY ONE
6437                                        ;WHEN THE TRACING FLIP-FLOP IS SET AND THE SIGNALS TRANST H AND TRST L
6438                                        ;ARE PULSED.  THE ABOVE SIGNALS WILL CAUSE A PULSE ON CTR L WHICH
6439                                        ;WILL CAUSE THE TRACE RAM ADDRESS REGISTER TO INCREMENT.
6440
6441  016454  005237  002414        19$:    INC     R6LOAD                  ;UPDATE EXPECTED TRAM ADDRESS REG
6442  016460  004737  006260              JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
6443  016464  001404                      BEQ     20$                     ;IF INCREMENTED BY 1 THEN CONTINUE
6444  016466                              ERRDF   4,TRADER,R026ER         ;TRACING F/F PROBABLY NOT PRESET
6445  016466  104455                      TRAP    C$ERDF
6446  016470  000004                      .WORD   4
6447  016472  0024C.                      .WORD   TRADER
6448  016474  004736                      .WORD   R026ER
6449  016476                        20$:  ENDSEG
6450  016476                        10000$:
6451  016476  104405                      TRAP    C$ESEG
6452  016500                              ENDTST
6453  016500                        L10114:
6454  016500  104401                      TRAP    C$ETST
6455
```

```
                                .SBTTL  TEST 31: CHECK CDAL5 H AND TRAD10 H TO INHIBIT PULSES ON CTR L

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE INCREMENTED
                                ; BY ONE VIA THE SIGNAL "CTR L" WHEN THE TRACING FLIP-FLOP IS SET TO A ONE,
                                ; CDAL REGISTER BIT 5 IS SET TO A ONE, TRACE RAM ADDRESS REGISTER BIT 10 IS SET
                                ; TO A ZERO AND THE SIGNALS TRANST H AND TRST L ARE PULSED VIA THE SETTING AND
                                ; CLEARING OF CDAL6 IN CONTROL REGISTER 0.  THE TEST WILL CHECK THAT THE TRACE
                                ; RAM ADDRESS REGISTER WILL NOT GET INCREMENTED BY ONE VIA THE SIGNAL CTR L WHEN
                                ; THE TRACING FLIP-FLOP IS SET TO A ONE, CDAL REGISTER BIT 5 IS SET TO A ONE,
                                ; TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE, AND THE SIGNALS TRANST H
                                ; AND TRST L ARE PULSED VIA THE SETTING AND CLEARING OF CDAL6 IN CONTROL REGIS-
                                ; TER 0.  THE TEST WILL THEN CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE
                                ; INCREMENTED BY ONE VIA THE SIGNAL CTR L WHEN THE TRACING FLIP-FLOP IS SET TO
                                ; A ONE, CDAL REGISTER BIT 5 IS SET TO A ZERROR, TRACE RAM ADDRESS REGISTER BIT
                                ; 10 IS SET TO A ONE, AND THE SIGNALS TRANST H AND TRST L ARE PULSED VIA THE
                                ; SETTING AND CLEARING OF CDAL6 IN CONTROL REGISTER 0.
                                ;--

016502                                  BGNTST
016502                          T31::

016502  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

016506                                  BGNSEG
016506  104404                          TRAP    C$BSEG

                                        ;SET CDAL5 H TO A ONE IN CONTROL REGISTER 0 AND CLEAR ALL OTHER R/W
                                        ;BITS IN THE LOW BYTE.  WHEN CDAL5 H IS SET TO A ONE, TRACING WILL BE
                                        ;INHIBITED WHEN TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE.

016510  112737  000040  002370          MOVB    #CDAL5,ROLOAD           ;SETUP BIT TO BE LOADED
016516  004737  006104                  JSR     PC,LDRDR0               ;LOAD, READ AND CHECK CONTROL REG 0
016522  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
016524                                  ERRDF   1,,ROEROR               ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
016524  104455                          TRAP    C$ERDF
016526  000001                          .WORD   1
016530  000000                          .WORD   0
016532  004606                          .WORD   ROEROR
016534                                  CKLOOP
016534  104406                          TRAP    C$CLP1

                                        ;PRESET THE TRACING FLIP-FLOP BY SETTING PDAL6 H TO A ONE.  SETTING
                                        ;PDAL6 H TO A ONE WILL CAUSE THE OUTPUT OF THE TRACING FLIP-FLOP TO BE
                                        ;SET TO THE HIGH STATE.  PDAL BITS 3:0 WILL BE SET TO A ZERO WHICH WILL
                                        ;CAUSE THE SIGNAL PTER0 L TO BE ASSERTED IN THE POINTER REGISTER.  PDAL5 H
                                        ;WILL BE SET TO A ZERO WHICH WILL CAUSE THE FUNCTION SELECT FLIP-FLOPS
                                        ;TO BE HELD TO A ZERO STATE (LOW).

016536  012737  000100  002376  1$:     MOV     #PDAL6!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
016544  004737  006136                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK PDAL REGISTER
016550  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
016552                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
016552  104455                          TRAP    C$ERDF
016554  000002                          .WORD   2
016556  000000                          .WORD   0
```

```
6512  016560  004706                          .WORD   R2EROR
6513  016562                                  CKLOOP
6514  016562  104406                          TRAP    C$CLP1
6515
6516                                          ;RELEASE THE PRESET SIDE OF THE TRACING FLIP-FLOP BY SETTING PDAL6 H
6517                                          ;TO A ZERO.
6518
6519  016564  042737  000100  002376  2$:     BIC     #PDAL6,R2LOAD           ;SETUP BIT TO BE CLEARED
6520  016572  004737  006136                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK PDAL REGISTER
6521  016576  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
6522  016600                                  ERRDF   2,,R2EROR               ;PDAL REGISTER NOT EQUAL EXPECTED
6523  016600  104455                          TRAP    C$ERDF
6524  016602  000002                          .WORD   2
6525  016604  000000                          .WORD   0
6526  016606  004706                          .WORD   R2EROR
6527  016610                                  CKLOOP
6528  016610  104406                          TRAP    C$CLP1
6529
6530                                          ;LOAD, READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH A DATA PATTERN
6531                                          ;OF 1777.
6532
6533  016612  012737  001777  002414  3$:     MOV     #1777,R6LOAD            ;SETUP DATA PATTERN TO BE LOADED
6534  016620  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
6535  016626  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK TRAM ADDR REG
6536  016632  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
6537  016634                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG ERROR - NOT = 1777
6538  016634  104455                          TRAP    C$ERDF
6539  016636  000004                          .WORD   4
6540  016640  002464                          .WORD   TRADER
6541  016642  004736                          .WORD   R026ER
6542  016644                                  CKLOOP
6543  016644  104406                          TRAP    C$CLP1
6544
6545                                          ;CLOCK THE SIGNAL CDAL6 H IN CONTROL REGISTER 0.  SETTING AND CLEARING
6546                                          ;CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED. THIS
6547                                          ;WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE THE SIGNAL
6548                                          ;ORST L TO PULSE. A PULSE SHOULD OCCUR ON THE SIGNAL CTR L AS A RESULT
6549                                          ;OF THE TRACING FLIP-FLOP BEING SET, CDAL REGISTER BIT 5 BEING A ONE,
6550                                          ;TRACE RAM ADDRESS REGISTER BIT 10 BEING SET TO A ZERO AND THE SIGNALS
6551                                          ;TRANST H AND TRST L BEING PULSED.  A PULSE ON THE SIGNAL CTR L WILL
6552                                          ;CAUSE THE TRACE RAM ADDRESS REGISTER TO BE INCREMENTED FROM 1777 TO
6553                                          ;2000, THUS SETTING TRAD10 TO A ONE.
6554
6555  016646  004737  006642          4$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 H TO PULSE TRANST H
6556
6557                                          ;CHECK THAT THE SIGNAL "CTR L" INCREMENTED THE TRACE RAM ADDRESS REGISTER
6558                                          ;FROM 1777 TO 2000.  TRACE RAM ADDRESS REGISTER BIT 10 IS NOW SET TO A 1
6559
6560  016652  005237  002414                  INC     R6LOAD                  ;UPDATE EXPECTED ADDRESS TO 2000
6561  016656  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
6562  016662  001405                          BEQ     5$                      ;IF OK THEN CONTINUE
6563  016664                                  ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO INCREMENT TRAM ADDR REG
6564  016664  104455                          TRAP    C$ERDF
6565  016666  000004                          .WORD   4
6566  016670  002464                          .WORD   TRADER
6567  016672  004736                          .WORD   R026ER
```

```
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0 TO CAUSE THE SIGNALS
                                        ;TRANST H AND TRST L TO BE PULSED.  THIS WILL THEN CAUSE THE SIGNAL
                                        ;ANST L TO BE PULSED WHICH WILL THEN CAUSE THE SIGNAL ORST L TO BE
                                        ;PULSED.  NO PULSE SHOULD OCCUR ON THE SIGNAL CTR L WHEN CDAL REGISTER
                                        ;BIT 5 IS SET TO A ONE AND TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO
                                        ;A ONE EVEN THOUGH THE TRACING FLIP-FLOP IS SET TO A ONE AND THE SIGNALS
                                        ;TRANST H AND TRST L WERE PULSED.  THE TRACE RAM ADDRESS REGISTER SHOULD
                                        ;REMAIN UNCHANGED AFTER TOGGLING CDAL6 H.

016676  004737  006642          5$:   JSR     PC,TRANST               ;SET AND CLEAR CDAL6 H TO PULSE TRANST H

                                        ;READ AND CHECK THE TRACE RAM ADDRESS REGISTER TO CHECK THAT IT DID NOT
                                        ;GET INCREMENTED BY A PULSE ON "CTR L" WHEN CDAL REGISTER BIT 5 WAS SET
                                        ;TO A ONE AND TRACE RAM ADDRESS REGISTER BIT 10 WAS SET TO A ONE.

016702  004737  006260                JSR     PC,READR6               ;READ AND CHECK TRACE RAM ADDRESS REG
016706  001405                         BEQ     6$                      ;IF NO CHANGE THEN CONTINUE
016710                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REGISTER INCREMENTED
016710  104455                         TRAP    C$ERDF
016712  000004                         .WORD   4
016714  002464                         .WORD   TRADER
016716  004736                         .WORD   R026ER
016720                                  CKLOOP
016720  104406                         TRAP    C$CLP1

                                        ;SET THE SIGNAL CDAL5 H TO A ZERO TO ALLOW A PULSE TO BE GENERATED ON
                                        ;THE SIGNAL "CTR L" THE NEXT TIME CDAL6 H IS TOGGLED.

016722  042737  000040  002370  6$:   BIC     #CDAL5,ROLOAD           ;SETUP BIT TO BE LOADED
016730  004737  006104                JSR     PC,LDRDR0               ;LOAD, READ AND CHECK REGISTER 0
016734  001405                         BEQ     7$                      ;IF LOADED OK THEN CONTINUE
016736                                  ERRDF   1,,ROEROR               ;CONTROL REG 0 NOT EQUAL EXPECTED
016736  104455                         TRAP    C$ERDF
016740  000001                         .WORD   1
016742  000000                         .WORD   0
016744  004606                         .WORD   ROEROR
016746                                  CKLOOP
016746  104406                         TRAP    C$CLP1

                                        ;TOGGLE THE SIGNAL CDAL6 IN CONTROL REGISTER 0 TO CAUSE THE SIGNALS
                                        ;TRANST H AND TRST L TO BE PULSED.  THIS WILL THEN CAUSE THE SIGNAL
                                        ;ANST L TO BE PULSED WHICH WILL THEN CAUSE THE SIGNAL ORST L TO BE
                                        ;PULSED.  A PULSE SHOULD OCCUR ON THE SIGNAL CTR L AS A RESULT OF THE
                                        ;TRACING FLIP-FLOP BEING SET TO A ONE, CDAL REGISTER BIT 5 BEING SET
                                        ;TO A ZERO, TRACE RAM ADDRESS REGISTER BIT 10 BEING SET TO A ONE AND
                                        ;THE SIGNALS TRANST H AND TRST L BEING ASSERTED.  A PULSE ON THE SIGNAL
                                        ;CTR L WILL CAUSE THE TRACE RAM ADDRESS REGISTER TO INCREMENT FROM
                                        ;2000 TO 2001.

016750  004737  006642          7$:   JSR     PC,TRANST               ;SET AND CLEAR CDAL6 H TO PULSE TRANST H

                                        ;READ AND CHECK THE TRACE RAM ADDRESS REGISTER TO CHECK THAT IT WAS
                                        ;INCREMENTED BY ONE VIA A PULSE ON THE SIGNAL "CTR L" WHEN CDAL5 H IS
```

TEST 31: CHECK CDAL5 H AND TRAD10 H TO INHIBIT PULSES ON CTR L SEQ 0138

```
6624                                            ;SET TO A ZERO AND TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE.
6625
6626  016754  005237  002414                    INC     R6LOAD                  ;UPDATE EXPECTED ADDRESS TO 2001
6627  016760  004737  006260                    JSR     PC,READR6               ;READ AND CHECK TRACE RAM ADDRESS REG
6628  016764  001404                            BEQ     8$                      ;IF OK THEN CONTINUE
6629  016766                                    ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO +1 TRAM ADDRESS REG
6630  016766  104455                            TRAP    C$ERDF
6631  016770  000004                            .WORD   4
6632  016772  002464                            .WORD   TRADER
6633  016774  004736                            .WORD   R026ER
6634  016776                            8$:     ENDSEC
6635  016776                            10000$:
6636  016776  104405                            TRAP    C$ESEG
6637
6638  017000                                    ENDTST
6639  017000                            L10115:
6640  017000  104401                            TRAP    C$ETST
6641
```

```
                                .SBTTL  TEST 32: LOAD TRACE RAMS VIA SIGNALS CTR H AND CTR L

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACE RAMS CAN BE LOADED FROM THE TRACE RAM
                                ; DATA IN BUFFERS VIA THE SIGNALS CTR H AND CTR L.
                                ;
                                ; THE TEST WILL LOAD AND CHECK THE TRACE RAM DATA IN BUFFERS WITH THE FOLLOWING
                                ; PATTERNS:
                                ;    TRDI 15:0  - DATA PATTERN OF 151515
                                ;    TRDI 31:16 - DATA PATTERN OF 113131
                                ;    TRDI 47:32 - DATA PATTERN OF 074747
                                ;    TRDI 59:48 - DATA PATTERN OF 005555
                                ; THE TEST WILL ASSERT THE SIGNAL TRSL0 L BY CLEARING THE LOW BYTE OF CONTROL
                                ; REGISTER 0.  THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA
                                ; IN BUFFERS.  THE TEST WILL LOAD ADDRESS 0 INTO THE TRACE RAM ADDRESS REGISTER
                                ; TO SELECT ADDRESS 0 OF ALL THE TRACE RAMS.  THE TEST WILL THEN PRESET THE
                                ; TRACING FLIP-FLOP BY SETTING PDAL6 IN CONTROL REGISTER 2.  THE TEST WILL NOW
                                ; SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING
                                ; CDAL6 WITH THE TRACING FLIP-FLOP IN THE PRESET STATE, WILL CAUSE THE SIGNALS
                                ; CTR L AND CTR H TO PULSE.  THE SIGNAL CTR L WILL CAUSE THE TRACE RAM ADDRESS
                                ; REGISTER TO BE INCREMENTED BY ONE.  THE SIGNALS CTR L AND CTR H WILL LOAD THE
                                ; TRACE RAMS WITH THE DATA STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 55:0.
                                ; AFTER SETTING AND CLEARING CDAL6, THE PROGRAM WILL CHECK THAT THE TRACE RAM
                                ; ADDRESS REGISTER INCREMENTED TO ADDRESS ONE. THE TEST WILL THEN RESET THE
                                ; TRACE RAM ADDRESS REGISTER TO ADDRESS 0.  THE TEST WILL THEN ASSERT THE SIGNAL
                                ; TRSL1 L BY SETTING THE SIGNAL CDAL2 TO A ONE IN CONTROL REIGSTER 0.  THE SIGNAL
                                ; TRSL1 L WILL ENABLE THE TRACE RAMS TO BE READ.  THE TEST WILL NOW READ ADDRESS
                                ; ZERO OF EACH TRACE RAM CHECKING THE DATA TO BE THAT WHICH WAS WRITTEN INTO THE
                                ; TRACE RAM DATA IN BUFFERS.
                                ;--

017002                                  BGNTST
017002                          T32::
017002  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

017006                                  BGNSUB
017006                          T32.1:
017006  104402                          TRAP    C$BSUB

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER 15:0 WITH A DATA PATTERN
                                ;OF 151515.

017010  012737  151515  002414          MOV     #151515,R6LOAD          ;SETUP DATA TO BE LOADED
017016  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ AND CHECK TRAM DATA IN BUF
017022  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
017024                                  ENDSUB
017024                          L10117:
017024  104403                          TRAP    C$ESUB

017026                                  BGNSUB
017026                          T32.2:
017026  104402                          TRAP    C$BSUB

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER 31:16 WITH A DATA PATTERN
                                ;OF 113131.
```

```
6698  017030  012737  113131  002414          MOV     #113131,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
6699  017036  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ AND CHECK TRAM DATA IN BUF
6700  017042  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
6701  017044                                  ENDSUB
6702  017044                          L10120:
6703  017044  104403                          TRAP    C$ESUB
6704
6705  017046                                  BGNSUB
6706  017046                          T32.3:
6707  017046  104402                          TRAP    C$BSUB
6708
6709                                          ;LOAD,READ AND CHECK TRACE RAM DATA IN BUFFER 47:32 WITH DATA PATTERN
6710                                          ;OF 074747.
6711
6712  017050  012737  074747  002414          MOV     #074747,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
6713  017056  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ AND CHECK TRAM DATA IN BUF
6714  017062  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
6715  017064                                  ENDSUB
6716  017064                          L10121:
6717  017064  104403                          TRAP    C$ESUB
6718
6719  017066                                  BGNSUB
6720  017066                          T32.4:
6721  017066  104402                          TRAP    C$BSUB
6722
6723                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER 59:48 WITH DATA PATTERN
6724                                          ;OF 005555
6725
6726  017070  012737  005555  002414          MOV     #005555,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
6727  017076  004537  006430                  JSR     R5,TRDIBF               ;LOAD,READ AND CHECK TRAM DATA IN BUF
6728  017102  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
6729  017104                                  ENDSUB
6730  017104                          L10122:
6731  017104  104403                          TRAP    C$ESUB
6732
6733  017106                                  BGNSUB
6734  017106                          T32.5:
6735  017106  104402                          TRAP    C$BSUB
6736
6737                                          ;CLEAR LOW BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING CLEARED
6738                                          ;WILL ASSERT THE SIGNAL TRSL0 L WHICH WILL ENABLE THE OUTPUTS OF THE
6739                                          ;TRACE RAM DATA IN BUFFERS
6740
6741  017110  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE
6742  017114  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
6743  017120  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
6744  017122                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
6745  017122  104455                          TRAP    C$ERDF
6746  017124  000001                          .WORD   1
6747  017126  000000                          .WORD   0
6748  017130  004606                          .WORD   R0EROR
6749  017132                                  CKLOOP
6750  017132  104406                          TRAP    C$CLP1
6751
6752                                          ;LOAD, READ AND CHECK TRACE RAM ADDRESS REGISTER WITH ADDRESS 0
6753
```

```
6754  017134  005037  006376          1$:     CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
6755  017140  004737  006312                  JSR     PC,TRADLD               ;GO LOAD AND CHECK TRACE RAM ADDRESS REG
6756
6757                                          ;SET PDAL6 IN CONTROL REGISTER 2 TO PRESET THE TRACING FLIP-FLOP TO
6758                                          ;THE HIGH STATE.
6759
6760  017144  052737  000100  002376          BIS     #PDAL6,R2LOAD           ;SETUP BIT TO BE LOADED
6761  017152  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
6762  017156  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
6763  017160                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
6764  017160  104455                          TRAP    C$ERDF
6765  017162  000002                          .WORD   2
6766  017164  000000                          .WORD   0
6767  017166  004706                          .WORD   R2EROR
6768  017170                                  CKLOOP
6769  017170  104406                          TRAP    C$CLP1
6770
6771                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING CDAL6
6772                                          ;WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE.  THIS WILL THEN
6773                                          ;CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE THE SIGNAL TRST L
6774                                          ;TO PULSE.  WHEN THE TRACING FLIP-FLOP IS IN THE PRESET STATE AND THE
6775                                          ;SIGNALS TRANST H AND TRST L ARE BEING PULSED, A PULSE WILL OCCUR ON
6776                                          ;THE SIGNALS CTR L AND CTR H.  THE SIGNAL CTR L WILL CAUSE THE TRACE RAM
6777                                          ;ADDRESS REGISTER TO BE INCREMENTED BY ONE.  THE SIGNALS CTR L AND CTR H
6778                                          ;WILL LOAD THE DATA FROM THE TRACE RAM DATA IN BUFFER BITS TRDI 55:0
6779                                          ;INTO ADDRESS 0 OF THE TRACE RAMS.
6780
6781  017172  004737  006642          2$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
6782
6783                                          ;READ TRACE RAM ADDRESS REGISTER CHECKING THE THE SIGNAL "CTR L"
6784                                          ;INCREMENTED THE TRACE RAM ADDRESS REGISTER TO ADDRESS ONE.
6785
6786  017176  012737  000001  002414  4$:     MOV     #1,R6LOAD               ;SETUP EXPECTED ADDRESS
6787  017204  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
6788  017210  001405                          BEQ     5$                      ;IF ADDRESS ONE THEN CONTINUE
6789  017212                                  ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO INCREMENT ADDRESS REG
6790  017212  104455                          TRAP    C$ERDF
6791  017214  000004                          .WORD   4
6792  017216  002464                          .WORD   TRADER
6793  017220  004736                          .WORD   R026ER
6794  017222                                  CKLOOP
6795  017222  104406                          TRAP    C$CLP1
6796
6797                                          ;RESET THE TRACE RAM ADDRESS REGISTER TO ADDRESS 0. THE POINTER REGISTER
6798                                          ;ON EXIT FROM ROUTINE "TRADLD" WILL HAVE THE SIGNAL PTER0 L ASSERTED.
6799
6800  017224  004737  006312          5$:     JSR     PC,TRADLD               ;RESET TRAM ADDRESS REGISTER TO 0
6801
6802                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO CAUSE THE
6803                                          ;SIGNAL TRSL1 L TO BE ASSERTED.  THE SIGNAL TRSL1 L WILL ENABLE THE
6804                                          ;TRACE RAMS SELECTED TO BE READ.
6805
6806  017230  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BIT TO BE SET
6807  017236  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
6808  017242  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
6809  017244                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
```

```
6810  017244  104455                          TRAP    C$ERDF
6811  017246  000001                          .WORD   1
6812  017250  000000                          .WORD   0
6813  017252  004606                          .WORD   ROEROR
6814  017254                                  CKLOOP
6815  017254  104406                          TRAP    C$CLP1
6816
6817                                          ;ASSERT THE SIGNAL PTER1 L IN THE POINTER REGISTER VIA CONTROL REG 2.
6818
6819  017256  004537  006400          6$:     JSR     R5,ASSERT               ;GO ASSERT PTER1
6820  017262  000001                          .WORD   PTER1
6821
6822                                          ;READ TRACE RAM DATA BITS TRDI 15:0 FOR A DATA PATTERN OF 151515
6823
6824  017264  012737  151515  002414  7$:     MOV     #151515,R6LOAD          ;SETUP DATA PREVIOUSLY LOADED
6825  017272  005037  002416                  CLR     R6MASK                  ;SETUP TO READ ALL 16 BITS
6826  017276  004737  006260                  JSR     PC,READR6               ;CHECK TRACE RAM DATA BITS TRDI 15:0
6827  017302  001405                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
6828  017304                                  ERRDF   4,TRAM15,TRAMER         ;CTR L+H FAILED TO LOAD DATA
6829  017304  104455                          TRAP    C$ERDF
6830  017306  000004                          .WORD   4
6831  017310  003000                          .WORD   TRAM15
6832  017312  004766                          .WORD   TRAMER
6833  017314                                  CKLOOP
6834  017314  104406                          TRAP    C$CLP1
6835
6836                                          ;ASSERT THE SIGNAL PTER2 L IN THE POINTER REGISTER VIA CONTROL REG 2
6837
6838  017316  004537  006400          8$:     JSR     R5,ASSERT               ;GO ASSERT PTER2
6839  017322  000002                          .WORD   PTER2
6840
6841                                          ;READ TRACE RAM DATA BITS TRDI 31:16 FOR A DATA PATTERN OF 113131.
6842
6843  017324  012737  113131  002414  9$:     MOV     #113131,R6LOAD          ;SETUP DATA PREVIOUSLY LOADED
6844  017332  004737  006260                  JSR     PC,READR6               ;CHECK TRACE RAM DATA BITS 31:16
6845  017336  001405                          BEQ     10$                     ;IF DATA OK THEN CONTINUE
6846  017340                                  ERRDF   4,TRAM31,TRAMER         ;CTR L+H FAILED TO LOAD DATA
6847  017340  104455                          TRAP    C$ERDF
6848  017342  000004                          .WORD   4
6849  017344  003034                          .WORD   TRAM31
6850  017346  004766                          .WORD   TRAMER
6851  017350                                  CKLOOP
6852  017350  104406                          TRAP    C$CLP1
6853
6854                                          ;ASSERT THE SIGNAL PTER3 L IN THE POINTER REGISTER VIA CONTRCL REG 2
6855
6856  017352  004537  006400          10$:    JSR     R5,ASSERT               ;GO ASSERT PTER3
6857  017356  000003                          .WORD   PTER3
6858
6859                                          ;READ TRACE RAM DATA BITS TRDI 47:32 FOR A DATA PATTERN OF 074747
6860
6861  017360  012737  074747  002414  11$:    MOV     #074747,R6LOAD          ;SETUP DATA PATTERN PREVIOUSLY LOADED
6862  017366  004737  006260                  JSR     PC,READR6               ;CHECK TRACE RAM DATA BITS 47:32
6863  017372  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
6864  017374                                  ERRDF   4,TRAM47,TRAMER         ;CTR L+H FAILED TO LOAD DATA
6865  017374  104455                          TRAP    C$ERDF
```

```
 6866  017376  000004                          .WORD   4
 6867  017400  003071                          .WORD   TRAM47
 6868  017402  004766                          .WORD   TRAMER
 6869  017404                                  CKLOOP
 6870  017404  104406                          TRAP    C$CLP1
 6871
 6872                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REG 2
 6873
 6874  017406  004537  006400          12$:    JSR     R5,ASSERT               ;GO ASSERT PTER4
 6875  017412  000004                          .WORD   PTER4
 6876
 6877                                          ;READ TRACE RAM DATA BITS TRDI 55:48 FOR A DATA PATTERN OF 155
 6878
 6879  017414  012737  000155  002414  13$:    MOV     #155,R6LOAD             ;SETUP DATA PREVIOUSLY WRITTEN -4 BITS
 6880  017422  012737  177400  002416          MOV     #177400,R6MASK          ;SETUP TO IGNORE UNUSED BITS
 6881  017430  004737  006260                  JSR     PC,READR6               ;CHECK TRACE RAM DATA BITS 55:48
 6882  017434  001404                          BEQ     14$                     ;IF DATA OK THEN CONTINUE
 6883  017436                                  ERRDF   4,TRAM55,TRAMER         ;CTR L+H FAILED TO LOAD DATA
 6884  017436  104455                          TRAP    C$ERDF
 6885  017440  000004                          .WORD   4
 6886  017442  003126                          .WORD   TRAM55
 6887  017444  004766                          .WORD   TRAMER
 6888  017446                          14$:    ENDSUB
 6889  017446                          L10123:
 6890  017446  104403                          TRAP    C$ESUB
 6891  017450                                  ENDTST
 6892  017450                          L10116:
 6893  017450  104401                          TRAP    C$ETS1
 6894
```

```
                                .SBTTL  TEST 33: OR ADDRESS REG TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THE OR ADDRESS REGISTER BITS (ORAD 3:0) BY LOADING AN
                                ; ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND THEN AN ALTERNATING ZEROES
                                ; AND ONES DATA PATTERN (05).  TO WRITE AND READ THE OR ADDRESS REGISTER, THE
                                ; PROGRAM WILL CLEAR CONTROL REGISTER 0 BITS (CDAL 7:0). CDAL7 BEING A ZERO
                                ; WILL ENABLE THE OUTPUTS OF THE OR ADDRESS REGISTER.  THE PROGRAM WILL SET
                                ; PDAL3 TO PDAL0 TO ALL ONES WHICH WILL CAUSE THE SIGNAL PTER15 L TO BE ASSERTED
                                ; IN THE POINTER REGISTER.  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE
                                ; SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H.  THE
                                ; SIGNAL WPT15 H WILL LOAD THE DATA ON THE WRITE COMMAND INTO OR ADDRESS REGIS-
                                ; TER BITS ORAD3 TO ORAD0.  ON A READ COMMAND TO CONTROL REGISTER 6 WITH THE
                                ; SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT15 H. THE
                                ; SIGNAL RPT15 H WILL READ THE DATA FROM THE OR ADDRESS REGISTER.
                                ;--

017452                                  BGNTST
017452                          T33::
017452  004737  005476                 JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

017456                                  BGNSEG
017456  104404                          TRAP    C$BSEG

                                ;CONTROL REGISTER 0 BITS CDAL 7:0 ARE CLEARED IN THE ROUTINE "INITED".
                                ;CDAL7 BEING A 0 WILL ENABLE THE OUTPUTS OF THE OR ADDRESS REGISTER.

                                ;SET THE SIGNAL PTER15 L IN THE POINTER REGISTER BY LOADING ALL ONES
                                ;INTO PDAL BITS 3:0 IN CONTROL REGISTER 2.

017460  004537  006400                 JSR     R5,ASSERT               ;GO ASSERT PTER15
017464  000017                          .WORD   PTER15

                                ;WRITE, READ AND CHECK OR ADDRESS REGISTER WITH AN ALTERNATING ONES
                                ;AND ZEROES DATA PATTERN (12). THE SIGNAL WPT15 H WILL PULSE ON A
                                ;WRITE COMMAND TO CONTROL REGISTER 6. THE SIGNAL RPT15 H WILL PULSE
                                ;ON A READ COMMAND TO CONTROL REGISTER 6.

017466  012737  000012  002414  1$:     MOV     #12,R6LOAD              ;SETUP ONES AND ZEROES DATA PATTERN
017474  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNUSED BITS
017502  004737  006252                 JSR     PC,LDRDR6               ;LOAD, RAD AND CHECK OR ADDRESS REG
017506  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
017510                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL 12
017510  104455                          TRAP    C$ERDF
017512  000004                          .WORD   4
017514  003163                          .WORD   ORADER
017516  004736                          .WORD   R026ER
017520                                  CKLOOP
017520  104406                          TRAP    C$CLP1
```

```
 6945
 6946                                          ;WRITE, READ AND CHECK OR ADDRESS REGISTER WITH AN ALTERNATING ZEROES
 6947                                          ;AND ONES DATA PATTERN (05). THE SIGNAL WPT15 H WILL PULSE ON A WRITE
 6948                                          ;COMMAND TO CONTROL REGISTER 6.  THE SIGNAL RPT15 H WILL PULSE ON A
 6949                                          ;READ COMMAND TO CONTROL REGISTER 6.
 6950
 6951  017522  012737  000005  002414  2$:     MOV     #5,R6LOAD               ;SETUP ZEROES AND ONES DATA PATTERN
 6952  017530  004737  006252                  JSR     PC,LDRDR6               ;LOAD,READ AND CHECK OR ADDRESS REG
 6953  017534  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
 6954  017536                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL TO 5
 6955  017536  104455                          TRAP    C$ERDF
 6956  017540  000004                          .WORD   4
 6957  017542  003163                          .WORD   ORADER
 6958  017544  004736                          .WORD   R026ER
 6959  017546                          3$:     ENDSEG
 6960  017546                          10000$:
 6961  017546  104405                          TRAP    C$ESEG
 6962
 6963  017550                                  ENDTST
 6964  017550                          L10124:
 6965  017550  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 34: OR ADDRESS REG TEST USING BINARY COUNT PATTERN

                                ;++
                                ; THIS TEST WILL CHECK THE OR ADDRESS REGISTER BITS ORAD 3:0 USING A BINARY
                                ; COUNT PATTERN.  THE DATA PATTERN WILL START AS ZERO AND BE INCREMENTED UNTIL
                                ; THE DATA PATTERN 17 HAS BEEN LOADED AND CHECKED.
                                ;--

017552                                  BGNTST
017552                          T34::
017552  004737  006476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
017556  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNUSED BITS
017564  005037  002414                  CLR     R6LOAD                  ;SETUP INITIAL PATTERN TO 0

                                        ;CONTROL REGISTER 0 BITS CDAL 7:0 ARE CLEARED ON EXIT FROM ROUTINE
                                        ;"INITED". THE SIGNAL CDAL7 BEING CLEARED WILL ENABLE THE OUTPUTS
                                        ;OF THE OR ADDRESS REGISTER.

017570                          1$:     BGNSEG
017570  104404                          TRAP    C$BSEG

                                        ;SET THE SIGNAL PTER15 L IN THE POINTER REGISTER BY SETTING PDAL 3:0
                                        ;TO ALL ONES IN CONTROL REGISTER 2.

017572  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER15 L
017576  000017                          .WORD   PTER15

                                        ;WRITE, READ AND CHECK THE OR ADDRESS REGISTER WITH THE DATA PATTERN
                                        ;IN LOCATION "R6LOAD".  A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6. A PULSE WILL
                                        ;BE ISSUED ON THE SIGNAL RPT15 H WHEN A READ COMMAND IS ISSUED TO
                                        ;CONTROL REGISTER 6.  THE SIGNAL WPT15 H WILL WRITE THE OR ADDRESS REG-
                                        ;ISTER AND THE SIGNAL RPT15 H WILL READ THE OR ADDRESS REGISTER.

017600  004737  006252          2$:     JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
017604  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
017606                                  ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REGISTER NOT EQUAL EXPECTED
017606  104455                          TRAP    C$ERDF
017610  000004                          .WORD   4
017612  003163                          .WORD   ORADER
017614  004736                          .WORD   RO26ER
017616                          3$:     ENDSEG
017616                          10000$:
017616  104405                          TRAP    C$ESEG

017620  005237  002414                  INC     R6LOAD                  ;INCREMENT THE DATA PATTERN BY 1
017624  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF DONE
017632  001756                          BEQ     1$                      ;IF NOT LOAD AND CHECK NEXT PATTERN
017634                                  ENDTST
017634                          L10125:
017634  104401                          TRAP    C$ETST
```

```
7018                                    .SBTTL  TEST 35: OR ARRAY DATA TEST - ORO 7:0 (1'S + 0'S, 0'S + 1'S)
7019
7020                                    ;++
7021                                    ; THIS TEST WILL CHECK EACH LOCATION OF THE OR ARRAY RAM (ORO 7:0) WITH AN
7022                                    ; ALTERNATING ONES AND ZEROES DATA PATTERN (252) AND AN ALTERNATING ZEROES AND
7023                                    ; ONES DATA PATTERN (125).
7024                                    ;
7025                                    ; THE FOLLOWING SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE OR ARRAY RAM:
7026                                    ;
7027                                    ; THE TEST WILL CLEAR ALL THE LOW BITS IN CONTROL REGISTER 0 TO INITIALIZE
7028                                    ; CONTROL REGISTER 0.  CDAL7 ON A ZERO WILL ENABLE THE OUTPUTS OF THE OR
7029                                    ; ADDRESS REGISTER.  CDAL4 ON A ZERO WILL ALLOW ONLY ONE AND/OR ARRAY RAMS TO
7030                                    ; BE SELECTED VIA THE POINTER REGISTER.  THE OR ARRAY RAMS WILL BE SELECTED IN
7031                                    ; THIS TEST BY SETTING PTER15 L IN THE POINTER REGISTER WHICH WILL CAUSE THE
7032                                    ; SIGNAL PLSL15 L TO BE ASSERTED.  THE SIGNAL PLSL15 L WILL ENABLE THE OR ARRAY
7033                                    ; RAMS TO BE WRITTEN OR READ.  THE TEST WILL LOAD THE ADDRESS TO BE TESTED INTO
7034                                    ; THE OR ADDRESS REGISTER.  TO LOAD THE ADDRESS, THE PROGRAM WILL ISSUE A WRITE
7035                                    ; COMMAND TO CONTROL REGISTER 6.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REG-
7036                                    ; ISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL
7037                                    ; WPT15 H WHICH WILL LOAD THE OR ADDRESS REGISTER.  TO READ THE OR ADDRESS REGIS-
7038                                    ; TER, THE TEST WILL ISSUE A READ COMMAND TO CONTROL REGISTER 6 WHICH WILL CAUSE
7039                                    ; A PULSE ON THE SIGNAL RPT15 H.  THE SIGNAL RPT15 H WILL READ THE DATA FROM THE
7040                                    ; OR ADDRESS REGISTER.  THE TEST WILL NOW WRITE AND READ THE OR ARRAY RAM LOCA-
7041                                    ; TION WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252).  TO WRITE THE
7042                                    ; OR ARRAY RAM LOCATION, THE TEST WILL ISSUE A WRITE COMMAND TO CONTROL REGIS-
7043                                    ; TER 4.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
7044                                    ; PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPLA15 L. THE SIGNAL
7045                                    ; WPLA15 L WILL WRITE THE DATA INTO THE OR ARRAY RAM LOCATION.  TO READ THE OR
7046                                    ; ARRAY RAM LOCATION, THE TEST WILL ISSUE A READ COMMAND TO CONTROL REGISTER 4.
7047                                    ; THE TEST WILL NOW LOAD, READ AND CHECK THE RAM LOCATION WITH AN ALTERNATING
7048                                    ; ZEROS AND ONES DATA PATTERN (125).  THE TEST WILL THEN SEQUENCE TO THE NEXT
7049                                    ; ADDRESS TO BE TESTED UNTIL ALL OR ARRAY RAM LOCATIONS HAVE BEEN CHECKED.
7050                                    ;--
7051
7052  017636                            BGNTST
7053  017636                            T35::
7054  017636  004737  005476           JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
7055  017642  005037  002414           CLR     R6LOAD                  ;SETUP STARTING ADDRESS TO BE 0
7056  017646  012737  177760  002416   MOV     #177760,R6MASK          ;SETUP TO IGNORE UNUSED BITS
7057
7058  017654                            1$:     BGNSEG
7059  017654  104404                    TRAP    C$BSEG
7060
7061                                    ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0. CDAL7 BEING A 0 WILL ENABLE
7062                                    ;THE OUTPUTS OF THE OR ADDRESS REGISTER.  CDAL4 BEING A ZERO WILL CAUSE
7063                                    ;ONLY ONE AND/OR ARRAY RAM TO BE SELECTED VIA THE POINTER REGISTER. IN
7064                                    ;THIS TEST PTER15 L WILL SELECT THE OR ARRAY RAMS.
7065
7066  017656  105037  002370           CLRB    ROLOAD                  ;SETUP TO CLEAR LOW BYTE
7067  017662  004737  006104           JSR     PC,LDRDRO               ;GO LOAD, READ AND CEHCK REGISTER 0
7068  017666  001405                    BEQ     2$                      ;IF LOADED OK THEN CONTINUE
7069  017670                            ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
7070  017670  104455                    TRAP    C$ERDF
7071  017672  000001                    .WORD   1
7072  017674  000000                    .WORD   0
7073  017676  004606                    .WORD   ROEROR
```

```
7074  017700                                  CKLOOP
7075  017700  104406                          TRAP    C$CLP1
7076
7077                                          ;SET THE SIGNAL PTER15 L IN THE POINTER REGISTER BY SETTING PDAL 3:0
7078                                          ;TO ALL ONES IN CONTROL REGISTER 2.
7079
7080  017702  004537  006400          2$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
7081  017706  000017                          .WORD   PTER15
7082
7083                                          ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH THE CONTENTS OF LOCATION
7084                                          ;"R6LOAD".  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL
7085                                          ;PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH
7086                                          ;WILL LOAD THE ADDRESS INTO THE OR ADDRESS REGISTER.  ON A READ COMMAND
7087                                          ;TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL
7088                                          ;BE ISSUED ON THE SIGNAL RPT15 H WHICH WILL READ THE DATA FROM THE OR
7089                                          ;ADDRESS REGISTER.
7090
7091  017710  004737  006252          3$:     JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
7092  017714  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
7093  017716                                  ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REG NOT EQUAL EXPECTED
7094  017716  104455                          TRAP    C$ERDF
7095  017720  000004                          .WORD   4
7096  017722  003163                          .WORD   ORADER
7097  017724  004736                          .WORD   RO26ER
7098  017726                                  CKLOOP
7099  017726  104406                          TRAP    C$CLP1
7100
7101                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
7102                                          ;REGISTER.  AN ALTERNATING ONES AND ZEROES DATA PATTERN (252) WILL BE
7103                                          ;WRITTEN INTO THE LOCATION.  THE OR ARRAY RAMS ARE ENABLED BY THE SIGNAL
7104                                          ;PLSL15 L. THE SIGNAL PLSL15 L IS GENERATED BY PTER15 L BEING ASSERTED
7105                                          ;IN THE POINTER REGISTER AND CDAL4 BEING SET TO A 0 IN CONTROL REGISTER
7106                                          ;0.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
7107                                          ;PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPLA15 L.  THE
7108                                          ;SIGNAL WPLA15 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE OR
7109                                          ;ARRAY LOCATION.  ON A READ COMMAND TO CONTROL REGISTER 4 DATA WILL
7110                                          ;BE READ FROM THE OR ARRAY RAM.
7111
7112  017730  012737  000252  002402  4$:     MOV     #252,R4LOAD             ;SETUP ONES AND ZEROES PATTERN
7113  017736  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNUSED BITS
7114  017744  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
7115  017750  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
7116  017752                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
7117  017752  104455                          TRAP    C$ERDF
7118  017754  000003                          .WORD   3
7119  017756  003514                          .WORD   ORDATA
7120  017760  004722                          .WORD   R4EROR
7121  017762                                  CKLOOP
7122  017762  104406                          TRAP    C$CLP1
7123
```

```
7124
7125                                        ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
7126                                        ;REGISTER WITH AN ALTERNATING ZEROES AND ONES DATA PATTERN (125).
7127
7128  017764  012737  000125  002402  5$:   MOV     #125,R4LOAD             ;SETUP ZEROES AND ONES DATA PATTERN
7129  017772  004737  006204              JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
7130  017776  001404                      BEQ     6$                      ;IF DATA OK THEN CONTINUE
7131  020000                              ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
7132  020000  104455                      TRAP    C$ERDF
7133  020002  000003                      .WORD   3
7134  020004  003514                      .WORD   ORDATA
7135  020006  004722                      .WORD   R4EROR
7136  020010                        6$:   ENDSEG
7137  020010                        10000$:
7138  020010  104405                      TRAP    C$ESEG
7139
7140  020012  005237  002414              INC     R6LOAD                  ;UPDATE THE OR ADDRESS BY ONE
7141  020016  032737  000020  002414      BIT     #BIT4,R6LOAD            ;CHECK IF DONE ALL ADDRESSES
7142  020024  001713                      BEQ     1$                      ;IF NOT THEN LOAD NEXT ADDRESS
7143
7144  020026                              ENDTST
7145  020026                        L10126:
7146  020026  104401                      TRAP    C$ETST
7147
```

```
                                .SBTTL  TEST 36: OR ARRAY RAM ADDRESS/SHORT TEST (ORO 7:0)

                                ;++
                                ; THIS TEST WILL CHECK THAT ALL ADDRESSES IN THE OR ARRAY RAM CAN BE ADDRESSED
                                ; CORRECTLY AND THAT WRITING ONE ADDRESS WILL NOT WRITE ANOTHER ADDRESS PREVIOUSLY
                                ; WRITTEN (ADDRESS SHORT).  THE TEST WILL WRITE AND CHECK EACH LOCATION OF THE
                                ; OR ARRAY RAMS WITH DATA EQUAL TO ITS ADDRESS. THE DATA PATTERN FOR THE TOP 4
                                ; BITS OF THE OR ARRAY RAM WILL BE THE SAME AS THE LOW 4 BITS OF THE OR ARRAY
                                ; RAM.  AFTER WRITING ALL LOCATIONS OF THE OR ARRAY RAM, THE TEST WILL READ EACH
                                ; LOCATION OF THE OR ARRAY RAM CHECKING THE DATA TO BE EQUAL TO ITS ADDRESS. THE
                                ; TEST WILL THEN READ EACH LOCATION CHECKING THE DATA TO BE EQUAL TO ITS ADDRESS
                                ; AND THEN WRITING AND CHECKING THE LOCATION WITH DATA EQUAL TO THE 1'S COMPLE-
                                ; MENT OF ITS ADDRESS.  IF A LOCATION ON THE FIRST READ DOES NOT EQUAL ITS
                                ; ADDRESS, THEN WRITING A PREVIOUS LOCATION PROBABLY WRITE THE LOCATION IN ERROR
                                ; ALSO.  AFTER ALL LOCATIONS HAVE BEEN TESTED IN THIS MANNER, THE PROGRAM WILL
                                ; READ THE OR ARRAY RAMS AGAIN CHECKING EACH LOCATION TO CONTAIN AS DATA THE
                                ; ONES COMPLEMENT OF ITS ADDRESS.
                                ;--

020030                                  BGNTST
020030                          T36::
020030  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

020034                                  BGNSUB
020034                          T36.1:
020034  104402                          TRAP    C$BSUB

020036  005037  002414                   CLR     R6LOAD                  ;SETUP OR ADDRESS TO BE INITIALLY 0
020042  012737  177760  002416           MOV     #177760,R6MASK          ;SETUP TO IGNORE UNUSED BITS IN REG 6
020050  012737  177400  002406           MOV     #177400,R4MASK          ;SETUP TO IGNORE UNUSED BITS IN REG 4

020056                          1$:     BGNSEG
020056  104404                          TRAP    C$BSEG

                                ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.  CDAL4 ON A ZERO WILL ENABLE
                                ;ONLY ONE AND/OR ARRAY RAM TO BE SELECTED VIA THE POINTER REGISTER.  IN
                                ;THIS TEST, THE SIGNAL PTER15 L WILL SELECT THE OR ARRAY RAMS.  CDAL7 ON
                                ;A ZERO WILL ENABLE THE OUTPUTS OF THE OR ADDRESS REGISTER.

020060  105037  002370                   CLRB    ROLOAD                  ;SETUP TO CLEAR THE LOW BYTE
020064  004737  006104                   JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
020070  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
020072                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
020072  104455                          TRAP    C$ERDF
020074  000001                          .WORD   1
020076  000000                          .WORD   0
020100  004606                          .WORD   ROEROR
020102                                  CKLOOP
020102  104406                          TRAP    C$CLP1

                                ;SET THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2

020104  004537  006400          2$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
020110  000017                          .WORD   PTER15

                                ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH THE CONTENTS OF LOCATION
```

```
7204                                            ;'R6LOAD".
7205
7206  020112  004737  006252        3$:       JSR     PC,LDRDR6               ;GO LOAD READ AND CHECK OR ADDRESS REG
7207  020116  001405                           BEQ     4$                      ;IF LOADED OK THEN CONTINUE
7208  020120                                    ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REGISTER NOT EQUAL EXPECTED
7209  020120  104455                           TRAP    C$ERDF
7210  020122  000004                           .WORD   4
7211  020124  003163                           .WORD   ORADER
7212  020126  004736                           .WORD   RO26ER
7213  020130                                    CKLOOP
7214  020130  104406                           TRAP    C$CLP1
7215
7216                                            ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION WITH DATA EQUAL TO THE
7217                                            ;ADDRESS BEING TESTED.  THE DATA FOR THE TOP 4 BITS WILL BE EQUAL TO
7218                                            ;THE DATA PATTERN OF THE LOW 4 BITS.
7219
7220  020132  013701  002414        4$:       MOV     R6LOAD,R1               ;GET THE ADDRESS BEING TESTED
7221  020136  006301                           ASL     R1                      ;MOVE ADDRESS TO TOP 4 BITS
7222  020140  006301                           ASL     R1                      ;
7223  020142  006301                           ASL     R1                      ;
7224  020144  006301                           ASL     R1
7225  020146  063701  002414                  ADD     R6LOAD,R1               ;ADD ADDRESS BACK INTO LOW 4 BITS
7226  020152  010137  002402                  MOV     R1,R4LOAD               ;SAVE THE DATA PATTERN
7227  020156  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD READ AND CHECK OR ARRAY RAM
7228  020162  001404                           BEQ     5$                      ;IF DATA LOADED OK THEN CONINUE
7229  020164                                    ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR (ORO 7:0)
7230  020164  104455                           TRAP    C$ERDF
7231  020166  000003                           .WORD   3
7232  020170  003514                           .WORD   ORDATA
7233  020172  004722                           .WORD   R4EROR
7234  020174                          5$:       ENDSEG
7235  020174                          10000$:
7236  020174  104405                           TRAP    C$ESEG
7237
7238  020176  005237  002414                  INC     R6LOAD                  ;UPDATE THE OR ADDRESS TO NEXT ONE
7239  020202  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF ALL LOCATIONS HAVE BEEN TESTED
7240  020210  001722                           BEQ     1$                      ;IF NOT THEN DO NEXT LOCATION
7241  020212                                    ENDSUB
7242  020212                          L10130:
7243  020212  104403                           TRAP    C$ESUB
7244
7245                                            ;THE FOLLOWING SECTION OF CODE WILL READ EACH LOCATION OF THE OR ARRAY
7246                                            ;RAMS CHECKING THE LOCATIONS TO CONTAIN ITS ADDRESS AS DATA.
7247
7248  020214                                    BGNSUB
7249  020214                          T36.2:
7250  020214  104402                           TRAP    C$BSUB
7251
7252                                            ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER 0,
7253                                            ;AND THE SIGNAL PTER15 L WILL BE ASSERTED IN THE POINTER REGISTER VIA
7254                                            ;CONTROL REGISTER 2.
7255
7256  020216  005037  002414                  CLR     R6LOAD                  ;SETUP OR ADDRESS TO START AT 0
7257
7258  020222                          1$:       BGNSEG
7259  020222  104404                           TRAP    C$BSEG
```

```
7260
7261                                        ;LOAD,READ AND CHECK OR ADDRESS REGISTER WITH THE CONTENTS OF "R6LOAD"
7262
7263  020224  004737  006252                JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
7264  020230  001405                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
7265  020232                                ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL EXPECTED
7266  020232  104455                        TRAP    C$ERDF
7267  020234  000004                        .WORD   4
7268  020236  003163                        .WORD   ORADER
7269  020240  004736                        .WORD   R026ER
7270  020242                                CKLOOP
7271  020242  104406                        TRAP    C$CLP1
7272
7273                                        ;READ AND CHECK OR ARRAY RAM LOCATION TO CONTAIN AS DATA ITS OWN ADDRESS.
7274                                        ;THE DATA FOR THE TOP 4 BITS WILL BE THE SAME AS THE DATA FOR THE LOW
7275                                        ;4 BITS.
7276
7277  020244  013701  002414          2$:   MOV     R6LOAD,R1               ;GET THE ADDRESS BEING TESTED
7278  020250  006301                        ASL     R1                      ;PUT THE ADDRESS IN TOP 4 BITS
7279  020252  006301                        ASL     R1                      ;
7280  020254  006301                        ASL     R1                      ;
7281  020256  006301                        ASL     R1                      ;
7282  020260  063701  002414                ADD     R6LOAD,R1               ;ADD ADDRESS BACK INTO LOW 4 BITS
7283  020264  010137  002402                MOV     R1,R4LOAD               ;SAVE DATA PATTERN PREVIOUSLY LOADED
7284  020270  010137  002404                MOV     R1,R4GOOD               ;SETUP EXPECTED DATA
7285  020274  004737  006220                JSR     PC,READR4               ;GO READ AND CHECK OR ARRAY DATA
7286  020300  001404                        BEQ     3$                      ;IF DATA OK THEN CONTINUE
7287  020302                                ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA NOT EQUAL TO ADDRESS
7288  020302  104455                        TRAP    C$ERDF
7289  020304  000003                        .WORD   3
7290  020306  003514                        .WORD   ORDATA
7291  020310  004722                        .WORD   R4EROF
7292  020312                          3$:   ENDSEG
7293  020312                          10000$:
7294  020312  104405                        TRAP    C$ESEG
7295
7296  020314  005237  002414                INC     R6LOAD                  ;UPDATE OR ADDRESS REGISTER ADDRESS
7297  020320  032737  000020  002414        BIT     #BIT4,R6LOAD            ;CHECK IF ALL ADDRESSES CHECKED
7298  020326  001735                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
7299  020330                                ENDSUB
7300  020330                          L10131:
7301  020330  104403                        TRAP    C$ESUB
7302
7303                                        ;THE FOLLOWING SECTION OF CODE WILL READ EACH LOCATION OF THE OR ARRAY
7304                                        ;RAM CHECKING THE DATA TO EQUAL ITS ADDRESS AND THEN WRITING AND CHECK-
7305                                        ;ING THE LOCATION WITH DATA EQUAL TO THE ONES COMPLEMENT OF ITS ADDRESS.
7306
7307  020332                                BGNSUB
7308  020332                          T36.3:
7309  020332  104402                        TRAP    C$BSUB
7310
7311                                        ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER 0.
7312                                        ;THE SIGNAL, PTER15 L, WILL BE ASSERTED IN THE POINTER REGISTER VIA
7313                                        ;CONTROL REGISTER 2.
7314
7315  020334  005037  002414                CLR     R6LOAD                  ;SETUP OR ADDRESS REG TO BE ADDRESS 0
```

```
                                        1$:     BGNSEG
020340  104404                                  TRAP    C$BSEG

                                                ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH THE CONTENTS OF LOCATION
                                                ;"R6LOAD".

020342  004737  006252                          JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
020346  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
020350                                          ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REGISTER NOT EQUAL EXPECTED
020350  104455                                  TRAP    C$ERDF
020352  000004                                  .WORD   4
020354  003163                                  .WORD   ORADER
020356  004736                                  .WORD   RO26ER
020360                                          CKLOOP
020360  104406                                  TRAP    C$CLP1

                                                ;READ AND CHECK OR ARRAY RAM LOCATION TO CONTAIN AS ITS DATA ITS OWN
                                                ;ADDRESS.  THE DATA IN THE TOP 4 BITS WILL BE THE SAME AS IN THE LOW
                                                ;4 BITS.

020362  013701  002414                  2$:     MOV     R6LOAD,R1               ;GET THE OR ADDRESS REG ADDRESS
020366  006301                                  ASL     R1                      ;MOVE IT TO TOP 4 BITS
020370  006301                                  ASL     R1                      ;
020372  006301                                  ASL     R1                      ;
020374  006301                                  ASL     R1                      ;
020376  063701  002414                          ADD     R6LOAD,R1               ;ADD ADDRESS INTO LOW 4 BITS
020402  010137  002402                          MOV     R1,R4LOAD               ;SAVE THE DATA PREVIOUSLY LOADED
020406  010137  002404                          MOV     R1,R4GOOD               ;SETUP EXPECTED DATA
020412  004737  006220                          JSR     PC,READR4               ;GO READ AND CHECK OR ARRAY DATA
020416  001405                                  BEQ     3$                      ;IF DATA OK THEN CONTINUE
020420                                          ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA NOT EQUAL ADDRESS
020420  104455                                  TRAP    C$ERDF
020422  000003                                  .WORD   3
020424  003514                                  .WORD   ORDATA
020426  004722                                  .WORD   R4EROR
020430                                          CKLOOP
020430  104406                                  TRAP    C$CLP1

                                                ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION WITH THE ONES COMPLEMENT
                                                ;OF ITS ADDRESS. THE TOP 4 BITS WILL EQUAL THE LOW 4 BITS.

020432  005137  002402          3$:     COM     R4LOAD                  ;COMPLMENT THE DATA
020436  042737  177400  002402          BIC     #177400,R4LOAD          ;CLEAR THE HIGH BYTE OF DATA
020444  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY DATA
020450  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
020452                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR 1'S COMP OF ADDRESS
020452  104455                          TRAP    C$ERDF
020454  000003                          .WORD   3
020456  003514                          .WORD   ORDATA
020460  004722                          .WORD   R4EROR
020462                          4$:     ENDSEG
020462                          10000$:
020462  104405                          TRAP    C$ESEG

020464  005237  002414                  INC     R6LOAD                  ;UPDATE OR ADDRESS REGISTER ADDRESS
```

```
7372  020470  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF ALL LOCATIONS TESTED
7373  020476  001720                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
7374  020500                                  ENDSUB
7375  020500                          L10132:
7376  020500  104403                          TRAP    C$ESUB
7377
7378                                          ;THE FOLLOWING SECTION OF CODE WILL READ EACH LOCATION OF THE OR ARRAY
7379                                          ;RAMS CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING
7380                                          ;TESTED.
7381
7382
7383  020502                                  BGNSUB
7384  020502                          T36.4:
7385  020502  104402                          TRAP    C$BSUB
7386
7387                                          ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER 0
7388                                          ;AND THE SIGNAL PTER15 L WILL BE ASSERTED IN THE POINTER REGISTER VIA
7389                                          ;CONTROL REGISTER 2.
7390
7391  020504  005037  002414                  CLR     R6LOAD                  ;SET OR ADDRESS TO START AT 0
7392
7393  020510                          1$:     BGNSEG
7394  020510  104404                          TRAP    C$BSEG
7395
7396                                          ;LOAD,READ AND CHECK OR ADDRFSS REGISTER WITH CONTENTS OF 'R6LOAD'
7397
7398  020512  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
7399  020516  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
7400  020520                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER NOT EQUAL EXPECTED
7401  020520  104455                          TRAP    C$ERDF
7402  020522  000004                          .WORD   4
7403  020524  003163                          .WORD   ORADER
7404  020526  004736                          .WORD   R026ER
7405  020530                                  CKLOOP
7406  020530  104406                          TRAP    C$CLP1
7407
7408                                          ;READ AND CHECK OR ARRAY RAM LOCATION TO CONTAIN AS ITS DATA THE ONES
7409                                          ;COMPLEMENT OF ITS ADDRESS. THE DATA IN THE TOP 4 BITS WILL BE THE
7410                                          ;SAME AS THE DATA IN THE LOW 4 BITS
7411
7412  020532  013701  002414          2$:     MOV     R6LOAD,R1               ;GET THE ADDRESS BEING TESTED
7413  020536  006301                          ASL     R1                      ;MOVE IT TO THE TOP 4 BITS
7414  020540  006301                          ASL     R1                      ;
7415  020542  006301                          ASL     R1                      ;
7416  020544  006301                          ASL     R1                      ;
7417  020546  063701  002414                  ADD     R6LOAD,R1               ;ADD THE ADDRESS BACK INTO LOW 4 BITS
7418  020552  005101                          COM     R1                      ;MAKE THE ONES COMPLEMENT
7419  020554  042701  177400                  BIC     #177400,R1              ;CLEAR UNUSED BITS
7420  020560  010137  002402                  MOV     R1,R4LOAD               ;SAVE THE DATA PREVIOUSLY LOADED
7421  020564  010137  002404                  MOV     R1,R4GOOD               ;SETUP EXPECTED DATA
7422  020570  004737  006220                  JSR     PC,READR4               ;GO READ AND CHECK OR ARRAY DATA
7423  020574  001404                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
7424  020576                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA NOT EQUAL 1'S COMP OF ADDRESS
7425  020576  104455                          TRAP    C$ERDF
7426  020600  000003                          .WORD   3
7427  020602  003514                          .WORD   ORDATA
```

```
 7428  020604  004722                          .WORD   R4EROR
 7429  020606                          3$:     ENDSEG
 7430  020606                          10000$:
 7431  020606  104405                          TRAP    C$ESEG
 7432
 7433  020610  005237  002414                  INC     R6LOAD                  ;UPDATE THE OR ADDRESS REGISTER ADDRESS
 7434  020614  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF DONE
 7435  020622  001732                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
 7436  020624                                  ENDSUB
 7437  020624                          L10133:
 7438  020624  104403                          TRAP    C$ESUB
 7439  020626                                  ENDTST
 7440  020626                          L10127:
 7441  020626  104401                          TRAP    C$ETST
 7442
```

```
                                        .SBTTL  TEST 37: AND ARRAY RAM TEST - PLSLO L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSLO L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 3:0.
                                        ;--

020630                                          BGNTST
020630                                  T37::
020630  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
020634  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
020640  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

020646                                  1$:     BGNSEG
020646  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.  CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

020650  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
020654  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
020660  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
020662                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
020662  104455                                  TRAP    C$ERDF
020664  000001                                  .WORD   1
020666  000000                                  .WORD   0
020670  004606                                  .WORD   R0EROR
020672                                          CKLOOP
020672  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH
                                        ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

020674  004537  006430          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 15:0
020700  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                        ;SET PTER0 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER0 L IS ASSERTED, THE SIGNAL PLSLO L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 3:0.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

020702  004537  006400                          JSR     R5,ASSERT               ;GO ASSERT PTER0
020706  000000                                  .WORD   PTER0

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSLO L.
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
                                        ;PTER0 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA0 L.  THE
                                        ;SIGNAL WPLA0 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
                                        ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
```

```
                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
                                                ;
                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSLO L WITH
                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
                                                ;
020710  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
020716  004737  006170                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
020722  001405                      BEQ     4$                      ;IF DATA OK THEN CONTINUE
020724                              ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
020724  104455                      TRAP    C$ERDF
020726  000003                      .WORD   3
020730  003552                      .WORD   ANDERR
020732  004722                      .WORD   R4EROR
020734                              CKLOOP
020734  104406                      TRAP    C$CLP1
                                                ;
                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSLO L WITH
                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
                                                ;
020736  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
020744  004737  006170                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
020750  001404                      BEQ     5$                      ;IF LOADED OK THEN CONTINUE
020752                              ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
020752  104455                      TRAP    C$ERDF
020754  000003                      .WORD   3
020756  003552                      .WORD   ANDERR
020760  004722                      .WORD   R4EROR
020762                      5$:     ENDSEG
020762                      10000$:
020762  104405                      TRAP    C$ESEG
                                                ;
020764  005237  002414              INC     R6LOAD                  ;UPDATE AND ARRAY ADDRESS BY ONE
020770  032737  000020  002414      BIT     #BIT4,R6LOAD            ;CHECK IF ALL 16 ADDRESSES DONE
020776  001723                      BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
021000                              ENDTST
021000                      L10134:
021000  104401                      TRAP    C$ETST
```

```
                                        .SBTTL  TEST 38: AND ARRAY RAM TEST - PLSL1 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL1 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 7:4.
                                        ;--

021002                                          BGNTST
021002                                  T38::
021002  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021006  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021012  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021020                                  1$:     BGNSEG
021020  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

021022  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021026  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021032  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021034                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021034  104455                                  TRAP    C$ERDF
021036  000001                                  .WORD   1
021040  000000                                  .WORD   0
021042  004606                                  .WORD   R0EROR
021044                                          CKLOOP
021044  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021046  004537  006430          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 15:0
021052  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                        ;SET PTER1 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER1 L IS ASSERTED, THE SIGNAL PLSL1 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 7:4.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

021054  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER1
021060  000001                          .WORD   PTER1

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL1 L.
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
                                        ;PTER1 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA1 L.  THE
                                        ;SIGNAL WPLA1 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
                                        ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
```

```
                                        ;READ BACK FROM THE AND ARRAY RAM SELECTED.
                                        ;
                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL1 L WITH
                                        ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
                                        ;
021062  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
021070  004737  006170                  JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
021074  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
021076                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
021076  104455                          TRAP    C$ERDF
021100  000003                          .WORD   3
021102  003552                          .WORD   ANDERR
021104  004722                          .WORD   R4EROR
021106                                  CKLOOP
021106  104406                          TRAP    C$CLP1
                                        ;
                                        ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL1 L WITH
                                        ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
                                        ;
021110  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
021116  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
021122  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
021124                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
021124  104455                          TRAP    C$ERDF
021126  000003                          .WORD   3
021130  003552                          .WORD   ANDERR
021132  004722                          .WORD   R4EROR
021134                          5$:     ENDSEG
021134                          10000$:
021134  104405                          TRAP    C$ESEG
                                        ;
021136  062737  000020  002414          ADD     #BIT4,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
021144  032737  000400  002414          BIT     #BIT8,R6LOAD            ;CHECK IF ALL 16 ADDRESSES DONE
021152  001722                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
021154                                  ENDTST
021154                  L10135:
021154  104401                          TRAP    C$ETST
```

```
                                        .SBTTL  TEST 39: AND ARRAY RAM TEST - PLSL2 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL2 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 11:8.
                                        ;--

021156                                          BGNTST
021156                                  T39::
021156  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021162  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021166  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021174                                  1$:     BGNSEG
021174  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

021176  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021202  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021206  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021210                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021210  104455                                  TRAP    C$ERDF
021212  000001                                  .WORD   1
021214  000000                                  .WORD   0
021216  004606                                  .WORD   R0EROR
021220                                          CKLOOP
021220  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021222  004537  006430          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 15:0
021226  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                        ;SET PTER2 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER2 L IS ASSERTED, THE SIGNAL PLSL2 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 11:8.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

021230  012737  000002  002376                  MOV     #PTER2,R2LOAD           ;SETUP BITS TO BE LOADED
021236  004737  006136                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
021242  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
021244                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
021244  104455                                  TRAP    C$ERDF
021246  000002                                  .WORD   2
021250  000000                                  .WORD   0
021252  004706                                  .WORD   R2EROR
```

```
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL2 L.
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
                                        ;PTER2 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA2 L.  THE
                                        ;SIGNAL WPLA2 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
                                        ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
                                        ;READ BACK FROM THE AND ARRAY RAM SELECTED.

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL2 L WITH
                                        ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).

021256  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
021264  004737  006170                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
021270  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
021272                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
021272  104455                        TRAP    C$ERDF
02127.  000003                        .WORD   3
021276  003552                        .WORD   ANDERR
021300  004722                        .WORD   R4EROR
021302                                CKLOOP
021302  104406                        TRAP    C$CLP1

                                        ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL2 L WITH
                                        ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).

021304  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
021312  004737  006170                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
021316  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
021320                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
021320  104455                        TRAP    C$ERDF
021322  000003                        .WORD   3
021324  003552                        .WORD   ANDERR
021326  004722                        .WORD   R4EROR
021330                          5$:   ENDSEG
021330                          10000$:
021330  104405                        TRAP    C$ESEG

021332  062737  000400  002414        ADD     #BIT8,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
021340  032737  010000  002414        BIT     #BIT12,R6LOAD           ;CHECK IF ALL 16 ADDRESSES DONE
021346  001712                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
021350                                ENDTST
021350                          L10136:
021350  104401                        TRAP    C$ETST
```

```
                                        .SBTTL  TEST 40: AND ARRAY RAM TEST - PLSL3 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AP ) ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL3 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 15:12.
                                        ;--

021352                                          BGNTST
021352                                  T40::
021352  004737  005476                         JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021356  005037  002414                         CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021362  012737  170377  002406                 MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021370                                  1$:     BGNSEG
021370  104404                                 TRAP    C$BSEG

                                                ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                                ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                                ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                                ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                                ;BUFFERS (TRDI 59:0).

021372  105037  002370                         CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021376  004737  006104                         JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021402  001405                                 BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021404                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021404  104455                                 TRAP    C$ERDF
021406  000001                                 .WORD   1
021410  000000                                 .WORD   0
021412  004606                                 .WORD   R0EROR
021414                                          CKLOOP
021414  104406                                 TRAP    C$CLP1

                                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH
                                                ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                                ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021416  004537  006430          2$:            JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 15:0
021422  000005                                 .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                                ;SET PTER3 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                                ;A ZERO AND THE SIGNAL PTER3 L IS ASSERTED, THE SIGNAL PLSL3 L WILL BE
                                                ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 15:12.
                                                ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                                ;REMAIN HIGH.

021424  012737  000003  002376                 MOV     #PTER3,R2LOAD           ;SETUP BITS TO BE LOADED
021432  004737  006136                         JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
021436  001405                                 BEQ     3$                      ;IF LOADED OK THEN CONTINUE
021440                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
021440  104455                                 TRAP    C$ERDF
021442  000002                                 .WORD   2
021444  000000                                 .WORD   0
021446  004706                                 .WORD   R2EROR
```

```
 7789  021450                                  CKLOOP
 7790  021450  104406                          TRAP    C$CLP1
 7791
 7792                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL3 L.
 7793                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
 7794                                          ;PTER3 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA3 L.  THE
 7795                                          ;SIGNAL WPLA3 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
 7796                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
 7797                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
 7798
 7799                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL3 L WITH
 7800                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
 7801
 7802  021452  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
 7803  021460  004737  006170                  JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
 7804  021464  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
 7805  021466                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
 7806  021466  104455                          TRAP    C$ERDF
 7807  021470  000003                          .WORD   3
 7808  021472  003552                          .WORD   ANDERR
 7809  021474  004722                          .WORD   R4EROR
 7810  021476                                  CKLOOP
 7811  021476  104406                          TRAP    C$CLP1
 7812
 7813                                          ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL3 L WITH
 7814                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
 7815
 7816  021500  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
 7817  021506  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
 7818  021512  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
 7819  021514                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
 7820  021514  104455                          TRAP    C$ERDF
 7821  021516  000003                          .WORD   3
 7822  021520  003552                          .WORD   ANDERR
 7823  021522  004722                          .WORD   R4EROR
 7824  021524                          5$:     ENDSEG
 7825  021524                          10000$:
 7826  021524  104405                          TRAP    C$ESEG
 7827
 7828  021526  062737  010000  002414          ADD     #BIT12,R6LOAD           ;UPDATE AND ARRAY ADDRESS BY ONE
 7829  021534  001315                          BNE     1$                      ;IF NOT 0 THEN DO NEXT ADDRESS
 7830  021536                                  ENDTST
 7831  021536                          L10137:
 7832  021536  104401                          TRAP    C$ETST
 7833
```

```
                                        .SBTTL  TEST 41: AND ARRAY RAM TEST - PLSL4 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL4 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 19:16.
                                        ;--

021540                                          BGNTST
021540                                  T41::
021540  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021544  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021550  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021556                                  1$:     BGNSEG
021556  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSL0 L.
                                        ;THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

021560  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021564  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021570  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021572                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021572  104455                                  TRAP    C$ERDF
021574  000001                                  .WORD   1
021576  000000                                  .WORD   0
021600  004606                                  .WORD   R0EROR
021602                                          CKLOOP
021602  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021604  004537  006430          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 31:16
021610  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16

                                        ;SET PTER4 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER4 L IS ASSERTED, THE SIGNAL PLSL4 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 19:16.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

021612  012737  000004  002376                  MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
021620  004737  006136                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
021624  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
021626                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
021626  104455                                  TRAP    C$ERDF
021630  000002                                  .WORD   2
021632  000000                                  .WORD   0
021634  004706                                  .WORD   R2EROR
```

```
7890  021636                                  CKLOOP
7891  021636  104406                          TRAP    C$CLP1
7892
7893                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL4 L.
7894                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
7895                                          ;PTER4 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA4 L.  THE
7896                                          ;SIGNAL WPLA4 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
7897                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
7898                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
7899
7900                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL4 L WITH
7901                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
7902
7903  021640  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
7904  021646  004737  006170                  JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
7905  021652  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
7906  021654                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
7907  021654  104455                          TRAP    C$ERDF
7908  021656  000003                          .WORD   3
7909  021660  003552                          .WORD   ANDERR
7910  021662  004722                          .WORD   R4EROR
7911  021664                                  CKLOOP
7912  021664  104406                          TRAP    C$CLP1
7913
7914                                          ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL4 L WITH
7915                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
7916
7917  021666  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
7918  021674  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
7919  021700  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
7920  021702                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
7921  021702  104455                          TRAP    C$ERDF
7922  021704  000003                          .WORD   3
7923  021706  003552                          .WORD   ANDERR
7924  021710  004722                          .WORD   R4EROR
7925  021712                          5$:     ENDSEG
7926  021712                          10000$:
7927  021712  104405                          TRAP    C$ESEG
7928
7929  021714  005237  002414                  INC     R6LOAD                  ;UPDATE AND ARRAY ADDRESS BY ONE
7930  021720  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
7931  021726  001713                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
7932  021730                                  ENDTST
7933  021730                          L10140:
7934  021730  104401                          TRAP    C$ETST
7935
```

```
                                        .SBTTL  TEST 42: AND ARRAY RAM TEST - PLSL5 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL5 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 23:20.
                                        ;--

021732                                          BGNTST
021732                                  T42::
021732  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021736  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021742  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021750                                  1$:     BGNSEG
021750  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSL0 L.
                                        ;THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

021752  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021756  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021762  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021764                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021764  104455                                  TRAP    C$ERDF
021766  000001                                  .WORD   1
021770  000000                                  .WORD   0
021772  004606                                  .WORD   R0EROR
021774                                          CKLOOP
021774  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021776  004537  006430          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 31:16
022002  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16

                                        ;SET PTER5 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER5 L IS ASSERTED, THE SIGNAL PLSL5 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 23:20.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

022004  012737  000005  002376                  MOV     #PTER5,R2LOAD           ;SETUP BITS TO BE LOADED
022012  004737  006136                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
022016  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
022020                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
022020  104455                                  TRAP    C$ERDF
022022  000002                                  .WORD   2
022024  000000                                  .WORD   0
022026  004706                                  .WORD   R2EROR
```

```
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL5 L.
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
                                        ;PTERS L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA5 L.  THE
                                        ;SIGNAL WPLA5 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
                                        ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
                                        ;READ BACK FROM THE AND ARRAY RAM SELECTED.

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL5 L WITH
                                        ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).

022032  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
022040  004737  006170                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
022044  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
022046                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
022046  104455                        TRAP    C$ERDF
022050  000003                        .WORD   3
022052  003552                        .WORD   ANDERR
022054  004722                        .WORD   R4EROR
022056                                CKLOOP
022056  104406                        TRAP    C$CLP1

                                        ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL5 L WITH
                                        ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).

022060  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
022066  004737  006170                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
022072  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
022074                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
022074  104455                        TRAP    C$ERDF
022076  000003                        .WORD   3
022100  003552                        .WORD   ANDERR
022102  004722                        .WORD   R4EROR
022104                          5$:   ENDSEG
022104                          10000$:
022104  104405                        TRAP    C$ESEG

022106  062737  000020  002414        ADD     #BIT4,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
022114  032737  000400  002414        BIT     #BIT8,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
022122  001712                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
022124                                ENDTST
022124                          L10141:
022124  104401                        TRAP    C$ETST
```

```
                                        .SBTTL  TEST 43: AND ARRAY RAM TEST - PLSL6 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL6 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 27:24.
                                        ;--

022126                                          BGNTST
022126                                  T43::
022126  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
022132  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
022136  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

022144                                  1$:     BGNSEG
022144  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

022146  105037  002370                        CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
022152  004737  006104                        JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
022156  001405                                BEQ     2$                      ;IF LOADED OK THEN CONTINUE
022160                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
022160  104455                                  TRAP    C$ERDF
022162  000001                                  .WORD   1
022164  000000                                  .WORD   0
022166  004606                                  .WORD   R0EROR
022170                                          CKLOOP
022170  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

022172  004537  006430                  2$:     JSR     R5,TRDI8F               ;LOAD,READ,CHECK TRAM DATA IN BUF 31:16
022176  000006                                  .WORD   PTER6                   ;SELECT TRDI BITS 31:16

                                        ;SET PTER6 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER6 L IS ASSERTED, THE SIGNAL PLSL6 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 27:24.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

022200  012737  000006  002376                MOV     #PTER6,R2LOAD           ;SETUP BITS TO BE LOADED
022206  004737  006136                        JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
022212  001405                                BEQ     3$                      ;IF LOADED OK THEN CONTINUE
022214                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
022214  104455                                  TRAP    C$ERDF
022216  000002                                  .WORD   2
022220  000000                                  .WORD   0
022222  004706                                  .WORD   R2EROR
```

```
8094  022224                                  CKLOOP
8095  022224  104406                          TRAP    C$CLP1
8096
8097                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL6 L.
8098                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8099                                          ;PTER6 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA6 L.  THE
8100                                          ;SIGNAL WPLA6 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8101                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8102                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8103
8104                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL6 L WITH
8105                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8106
8107  022226  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8108  022234  004737  006170                 JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8109  022240  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
8110  022242                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8111  022242  104455                          TRAP    C$ERDF
8112  022244  000003                          .WORD   3
8113  022246  003552                          .WORD   ANDERR
8114  022250  004722                          .WORD   R4EROR
8115  022252                                  CKLOOP
8116  022252  1J4406                          TRAP    C$CLP1
8117
8118                                          ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL6 L WITH
8119                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8120
8121  022254  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8122  022262  004737  006170                 JSR     PC,LDRDA                ;LOAD, READ AND CHECK AND ARRAY RAM
8123  022266  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8124  022270                                  ERRDF   3,ANDERR R4EROR         ;AND ARRAY NOT EQUAL 05
8125  022270  104455                          TRAP    C$ERDF
8126  022272  000003                          .WORD   3
8127  022274  003552                          .WORD   ANDERR
8128  022276  004722                          .WORD   R4EROR
8129  022300                          5$:     ENDSEG
8130  022300                          10000$:
8131  022300  104405                          TRAP    C$ESEG
8132
8133  022302  062737  000400  002414          ADD     #BIT8,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8134  022310  032737  010000  002414          BIT     #BIT12,R6LOAD           ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8135  022316  001712                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8136  022320                                  ENDTST
8137  022320                          L10142:
8138  022320  104401                          TRAP    C$ETST
8139
```

TEST 44: AND ARRAY RAM TES1 - PLSL7 L (1'S + 0'S, 0'S + 1'S) SEQ 0170

```
8140                                    .SBTTL  TEST 44: AND ARRAY RAM TEST - PLSL7 L (1'S + 0'S, 0'S + 1'S)
8141
8142                                    ;++
8143                                    ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
8144                                    ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
8145                                    ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
8146                                    ; SIGNAL PLSL7 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 31:28.
8147                                    ;--
8148
8149  022322                                    BGNTST
8150  022322                            T44::
8151  022322  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
8152  022326  005037  002414                   CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
8153  022332  012737  170377  002466           MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ
8154
8155  022340                            1$:     BGNSEG
8156  022340  104404                           TRAP    C$BSEG
8157
8158                                    ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
8159                                    ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
8160                                    ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
8161                                    ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
8162                                    ;BUFFERS (TRDI 59:0).
8163
8164  022342  105037  002370                   CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
8165  022346  004737  006104                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
8166  022352  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
8167  022354                                    ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
8168  022354  104455                           TRAP    C$ERDF
8169  022356  000001                           .WORD   1
8170  022360  000000                           .WORD   0
8171  022362  004606                           .WORD   R0EROR
8172  022364                                    CKLOOP
8173  022364  104406                           TRAP    C$CLP1
8174
8175                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH
8176                                    ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
8177                                    ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.
8178
8179  022366  004537  006430      2$:   JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 31:16
8180  022372  000006                    .WORD   PTER6                   ;SELECT TRDI BITS 31:16
8181
8182                                    ;SET PTER7 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
8183                                    ;A ZERO AND THE SIGNAL PTER7 L IS ASSERTED, THE SIGNAL PLSL7 L WILL BE
8184                                    ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 31:28.
8185                                    ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
8186                                    ;REMAIN HIGH.
8187
8188  022374  012737  000007  002376           MOV     #PTER7,R2LOAD           ;SETUP BITS TO BE LOADED
8189  022402  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
8190  022406  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
8191  022410                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
8192  022410  104455                           TRAP    C$ERDF
8193  022412  000002                           .WORD   2
8194  022414  000000                           .WORD   0
8195  022416  004706                           .WORD   R2EROR
```

```
8196  022420                                        CKLOOP
8197  022420  104406                                TRAP    C$CLP1
8198
8199                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL7 L.
8200                                                ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8201                                                ;PTER7 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA7 L.  THE
8202                                                ;SIGNAL WPLA7 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8203                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8204                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8205
8206                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL7 L WITH
8207                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8208
8209  022422  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8210  022430  004737  006170                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8211  022434  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
8212  022436                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8213  022436  104455                        TRAP    C$ERDF
8214  022440  000003                        .WORD   3
8215  022442  003552                        .WORD   ANDERR
8216  022444  004722                        .WORD   R4EROR
8217  022446                                CKLOOP
8218  022446  104406                        TRAP    C$CLP1
8219
8220                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL7 L WITH
8221                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8222
8223  022450  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8224  022456  004737  006170                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8225  022462  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8226  022464                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8227  022464  104455                        TRAP    C$ERDF
8228  022466  000003                        .WORD   3
8229  022470  003552                        .WORD   ANDERR
8230  022472  004722                        .WORD   R4EROR
8231  022474                        5$:     ENDSEG
8232  022474                        10000$:
8233  022474  104405                        TRAP    C$ESEG
8234
8235  022476  062737  010000  002414        ADD     #BIT12,R6LOAD           ;UPDATE AND ARRAY ADDRESS BY ONE
8236  022504  001315                        BNE     1$                      ;IF NOT 0 THEN DO NEXT ADDRESS
8237  022506                                ENDTST
8238  022506                        L10143:
8239  022506  104401                        TRAP    C$ETST
8240
```

```
                                        .SBTTL  TEST 45: AND ARRAY RAM TEST - PLSL8 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL8 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 35:32.
                                        ;--

022510                                          BGNTST
022510                                  T45::
022510  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
022514  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
022520  012737  170377  002406                  MOV     #170377,R6MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

022526                                  1$:     BGNSEG
022526  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

022530  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
022534  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
022540  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
022542                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
022542  104455                                  TRAP    C$ERDF
022544  000001                                  .WORD   1
022546  000000                                  .WORD   0
022550  004606                                  .WORD   R0EROR
022552                                          CKLOOP
022552  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

022554  004537  006430            2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 47:32
022560  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32

                                        ;SET PTER8 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER8 L IS ASSERTED, THE SIGNAL PLSL8 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 35:32.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

022562  012737  000010  002376                  MOV     #PTER8,R2LOAD           ;SETUP BITS TO BE LOADED
022570  004737  006136                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
022574  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
022576                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
022576  104455                                  TRAP    C$ERDF
022600  000002                                  .WORD   2
022602  000000                                  .WORD   0
022604  004706                                  .WORD   R2EROR
```

```
 8297  022606                                  CKLOOP
 8298  022606  104406                          TRAP    C$CLP1
 8299
 8300                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL8 L.
 8301                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
 8302                                          ;PTER8 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA8 L.  THE
 8303                                          ;SIGNAL WPLA8 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
 8304                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
 8305                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
 8306
 8307                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL8 L WITH
 8308                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
 8309
 8310  022610  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
 8311  022616  004737  006170                  JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
 8312  022622  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
 8313  022624                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
 8314  022624  104455                          TRAP    C$ERDF
 8315  022626  000003                          .WORD   3
 8316  022630  003552                          .WORD   ANDERR
 8317  022632  004722                          .WORD   R4EROR
 8318  022634                                  CKLOOP
 8319  022634  104406                          TRAP    C$CLP1
 8320
 8321                                          ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL8 L WITH
 8322                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
 8323
 8324  022636  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
 8325  022644  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
 8326  022650  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
 8327  022652                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
 8328  022652  104455                          TRAP    C$ERDF
 8329  022654  000003                          .WORD   3
 8330  022656  003552                          .WORD   ANDERR
 8331  022660  004722                          .WORD   R4EROR
 8332  022662                          5$:     ENDSEG
 8333  022662                          10000$:
 8334  022662  104405                          TRAP    C$ESEG
 8335
 8336  022664  005237  002414                  INC     R6LOAD                  ;UPDATE AND ARRAY ADDRESS BY ONE
 8337  022670  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
 8338  022676  001713                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
 8339  022700                                  ENDTST
 8340  022700                          L10144:
 8341  022700  104401                          TRAP    C$ETST
 8342
```

```
8343                                    .SBTTL  TEST 46: AND ARRAY RAM TEST - PLSL9 L (1'S + 0'S, 0'S + 1'S)
8344
8345                                    ;++
8346                                    ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
8347                                    ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
8348                                    ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
8349                                    ; SIGNAL PLSL9 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 39:36.
8350                                    ;--
8351
8352  022702                                    BGNTST
8353  022702                            T46::
8354  022702  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
8355  022706  005037  002414                   CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
8356  022712  012737  170377  002406           MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ
8357
8358  022720                            1$:     BGNSEG
8359  022720  104404                           TRAP    C$BSEG
8360
8361                                    ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
8362                                    ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
8363                                    ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
8364                                    ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
8365                                    ;BUFFERS (TRDI 59:0).
8366
8367  022722  105037  002370                   CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
8368  022726  004737  006104                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
8369  022732  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
8370  022734                                    ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
8371  022734  104455                           TRAP    C$ERDF
8372  022736  000001                           .WORD   1
8373  022740  000000                           .WORD   0
8374  022742  004606                           .WORD   ROEROR
8375  022744                                    CKLOOP
8376  022744  104406                           TRAP    C$CLP1
8377
8378                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH
8379                                    ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
8380                                    ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.
8381
8382  022746  004537  006430      2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 47:32
8383  022752  000007                     .WORD   PTER7                   ;SELECT TRDI BITS 47:32
8384
8385                                    ;SET PTER9 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
8386                                    ;A ZERO AND THE SIGNAL PTER9 L IS ASSERTED, THE SIGNAL PLSL9 L WILL BE
8387                                    ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 39:36.
8388                                    ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
8389                                    ;REMAIN HIGH.
8390
8391  022754  012737  000011  002376           MOV     #PTER9,R2LOAD           ;SETUP BITS TO BE LOADED
8392  022762  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
8393  022766  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
8394  022770                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
8395  022770  104455                           TRAP    C$ERDF
8396  022772  000002                           .WORD   2
8397  022774  000000                           .WORD   0
8398  022776  004706                           .WORD   R2EROR
```

```
8399  023000                                    CKLOOP
8400  023000  104406                           TRAP    C$CLP1
8401
8402                                            ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL9 L.
8403                                            ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8404                                            ;PTER9 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA9 L.  THE
8405                                            ;SIGNAL WPLA9 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8406                                            ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8407                                            ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8408
8409                                            ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL9 L WITH
8410                                            ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8411
8412  023002  012737  000012  002402  3$:       MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8413  023010  004737  006170                   JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8414  023014  001405                           BEQ     4$                      ;IF DATA OK THEN CONTINUE
8415  023016                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8416  023016  104455                           TRAP    C$ERDF
8417  023020  000003                           .WORD   3
8418  023022  003552                           .WORD   ANDERR
8419  023024  004722                           .WORD   R4EROR
8420  023026                                    CKLOOP
8421  023026  104406                           TRAP    C$CLP1
8422
8423                                            ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL9 L WITH
8424                                            ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8425
8426  023030  012737  000005  002402  4$:       MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8427  023036  004737  006170                   JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8428  023042  001404                           BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8429  023044                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8430  023044  104455                           TRAP    C$ERDF
8431  023046  000003                           .WORD   3
8432  023050  003552                           .WORD   ANDERR
8433  023052  004722                           .WORD   R4EROR
8434  023054                            5$:     ENDSEG
8435  023054                            10000$:
8436  023054  104405                           TRAP    C$ESEG
8437
8438  023056  062737  000020  002414           ADD     #BIT4,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8439  023064  032737  000400  002414           BIT     #BIT8,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8440  023072  001712                           BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8441  023074                                    ENDTST
8442  023074                            L10145:
8443  023074  104401                           TRAP    C$ETST
8444
```

```
                                        .SBTTL  TEST 47: AND ARRAY RAM TEST - PLSL10 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL10 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 43:40.
                                        ;--

023076                                          BGNTST
023076                                  T47::
023076  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
023102  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
023106  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

023114                                  1$:     BGNSEG
023114  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT TH. SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

023116  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
023122  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
023126  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
023130                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
023130  104455                                  TRAP    C$ERDF
023132  000001                                  .WORD   1
023134  000000                                  .WORD   0
023136  004606                                  .WORD   R0EROR
023140                                          CKLOOP
023140  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

023142  004537  006430          2$:     JSR     P5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 47:32
023146  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32

                                        ;SET PTER10 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER10 L IS ASSERTED, THE SIGNAL PLSL10 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 43:40.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

023150  012737  000012  002376                  MOV     #PTER10,R2LOAD          ;SETUP BITS TO BE LOADED
023156  004737  006136                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
023162  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
023164                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
023164  104455                                  TRAP    C$ERDF
023166  000002                                  .WORD   2
023170  000000                                  .WORD   0
023172  004706                                  .WORD   R2EROR
```

```
8501  023174                                    CKLOOP
8502  023174  104406                            TRAP    C$CLP1
8503
8504                                            ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL10 L.
8505                                            ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8506                                            ;PTER10 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA10 L.  THE
8507                                            ;SIGNAL WPLA10 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8508                                            ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8509                                            ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8510
8511                                            ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL10 L WITH
8512                                            ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8513
8514  023176  012737  000012  002402  3$:       MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8515  023204  004737  006170                   JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8516  023210  001405                            BEQ     4$                      ;IF DATA OK THEN CONTINUE
8517  023212                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8518  023212  104455                            TRAP    C$ERDF
8519  023214  000003                            .WORD   3
8520  023216  003552                            .WORD   ANDERR
8521  023220  004722                            .WORD   R4EROR
8522  023222                                    CKLOOP
8523  023222  104406                            TRAP    C$CLP1
8524
8525                                            ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL10 L WITH
8526                                            ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8527
8528  023224  012737  000005  002402  4$:       MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8529  023232  004737  006170                   JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8530  023236  001404                            BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8531  023240                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8532  023240  104455                            TRAP    C$ERDF
8533  023242  000003                            .WORD   3
8534  023244  003552                            .WORD   ANDERR
8535  023246  004722                            .WORD   R4EROR
8536  023250                            5$:     ENDSEG
8537  023250                            10000$:
8538  023250  104405                            TRAP    C$ESEG
8539
8540  023252  062737  000400  002414            ADD     #BIT8,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8541  023260  032737  010000  002414            BIT     #BIT12,R6LOAD           ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8542  023266  001712                            BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8543  023270                                    ENDTST
8544  023270                            L10146:
8545  023270  104401                            TRAP    C$ETST
8546
```

```
8547                                    .SBTTL  TEST 48: AND ARRAY RAM TEST - PLSL11 L (1'S + 0'S, 0'S + 1'S)
8548
8549                                    ;++
8550                                    ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
8551                                    ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
8552                                    ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
8553                                    ; SIGNAL PLSL11 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 47:44.
8554                                    ;--
8555
8556  023272                                    BGNTST
8557  023272                            T48::
8558  023272  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
8559  023276  005037  002414                   CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
8560  023302  012737  170377  002406           MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ
8561
8562  023310                            1$:     BGNSEG
8563  023310  104404                           TRAP    C$BSEG
8564
8565                                          ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
8566                                          ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
8567                                          ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
8568                                          ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
8569                                          ;BUFFERS (TRDI 59:0).
8570
8571  023312  105037  002370                   CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
8572  023316  004737  006104                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
8573  023322  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
8574  023324                                    ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
8575  023324  104455                           TRAP    C$ERDF
8576  023326  000001                           .WORD   1
8577  023330  000000                           .WORD   0
8578  023332  004606                           .WORD   R0EROR
8579  023334                                    CKLOOP
8580  023334  104406                           TRAP    C$CLP1
8581
8582                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH
8583                                          ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
8584                                          ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.
8585
8586  023336  004537  006430           2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 47:32
8587  023342  000007                           .WORD   PTER7                   ;SELECT TRDI BITS 47:32
8588
8589                                          ;SET PTER11 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
8590                                          ;A ZERO AND THE SIGNAL PTER11 L IS ASSERTED, THE SIGNAL PLSL11 L WILL BE
8591                                          ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 47:44.
8592                                          ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
8593                                          ;REMAIN HIGH.
8594
8595  023344  012737  000013  002376           MOV     #PTER11,R2LOAD          ;SETUP BITS TO BE LOADED
8596  023352  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
8597  023356  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
8598  023360                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
8599  023360  104455                           TRAP    C$ERDF
8600  023362  000002                           .WORD   2
8601  023364  000000                           .WORD   0
8602  023366  004706                           .WORD   R2EROR
```

```
 8603  023370                                  CKLOOP
 8604  023370  104406                          TRAP    C$CLP1
 8605
 8606                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL11 L.
 8607                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
 8608                                          ;PTER11 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA11 L.  THE
 8609                                          ;SIGNAL WPLA11 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
 8610                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
 8611                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
 8612
 8613                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL11 L WITH
 8614                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
 8615
 8616  023372  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
 8617  023400  004737  006170                  JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
 8618  023404  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
 8619  023406                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
 8620  023406  104455                          TRAP    C$ERDF
 8621  023410  000003                          .WORD   3
 8622  023412  003552                          .WORD   ANDERR
 8623  023414  004722                          .WORD   R4EROR
 8624  023416                                  CKLOOP
 8625  023416  104406                          TRAP    C$CLP1
 8626
 8627                                          ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL11 L WITH
 8628                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
 8629
 8630  023420  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
 8631  023426  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
 8632  023432  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
 8633  023434                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
 8634  023434  104455                          TRAP    C$ERDF
 8635  023436  000003                          .WORD   3
 8636  023440  003552                          .WORD   ANDERR
 8637  023442  004722                          .WORD   R4EROR
 8638  023444                          5$:     ENDSEG
 8639  023444                          10000$:
 8640  023444  104405                          TRAP    C$ESEG
 8641
 8642  023446  062737  010000  002414          ADD     #BIT12,R6LOAD           ;UPDATE AND ARRAY ADDRESS BY ONE
 8643  023454  001315                          BNE     1$                      ;IF NOT 0 THEN DO NEXT ADDRESS
 8644  023456                                  ENDTST
 8645  023456                          L10147:
 8646  023456  104401                          TRAP    C$ETST
 8647
```

```
                                        .SBTTL  TEST 49: AND ARRAY RAM TEST - PLSL12 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL12 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 51:48.
                                        ;--

023460                                          BGNTST
023460                                  T49::
023460  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
023464  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
023470  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

023476                                  1$:     BGNSEG
023476  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSL0 L.
                                        ;THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

023500  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
023504  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
023510  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
023512                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
023512  104455                                  TRAP    C$ERDF
023514  000001                                  .WORD   1
023516  000000                                  .WORD   0
023520  004606                                  .WORD   R0EROR
023522                                          CKLOOP
023522  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 59:48 WITH
                                        ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

023524  004537  006430          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 59:48
023530  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48

                                        ;SET PTER12 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER12 L IS ASSERTED, THE SIGNAL PLSL12 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 51:48.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

023532  012737  000014  002376                  MOV     #PTER12,R2LOAD          ;SETUP BITS TO BE LOADED
023540  004737  006136                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
023544  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
023546                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
023546  104455                                  TRAP    C$ERDF
023550  000002                                  .WORD   2
023552  000000                                  .WORD   0
023554  004706                                  .WORD   R2EROR
```

```
 8704  023556                                  CKLOOP
 8705  023556  104406                          TRAP    C$CLP1
 8706
 8707                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL12 L.
 8708                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
 8709                                          ;PTER12 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA12 L.  THE
 8710                                          ;SIGNAL WPLA12 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
 8711                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
 8712                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
 8713
 8714                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL12 L WITH
 8715                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
 8716
 8717  023560  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
 8718  023566  004737  006170                  JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
 8719  023572  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
 8720  023574                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
 8721  023574  104455                          TRAP    C$ERDF
 8722  023576  000003                          .WORD   3
 8723  023600  003552                          .WORD   ANDERR
 8724  023602  004722                          .WORD   R4EROR
 8725  023604                                  CKLOOP
 8726  023604  104406                          TRAP    C$CLP1
 8727
 8728                                          ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL12 L WITH
 8729                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
 8730
 8731  023606  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
 8732  023614  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
 8733  023620  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
 8734  023622                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
 8735  023622  104455                          TRAP    C$ERDF
 8736  023624  000003                          .WORD   3
 8737  023626  003552                          .WORD   ANDERR
 8738  023630  004722                          .WORD   R4EROR
 8739  023632                          5$:     ENDSEG
 8740  023632                          10000$:
 8741  023632  104405                          TRAP    C$ESEG
 8742
 8743  023634  005237  002414                  INC     R6LOAD                  ;UPDATE AND ARRAY ADDRESS BY ONE
 8744  023640  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
 8745  023646  001713                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
 8746  023650                                  ENDTST
 8747  023650                          L10150:
 8748  023650  104401                          TRAP    C$ETST
 8749
```

```
                                        .SBTTL  TEST 50: AND ARRAY RAM TEST - PLSL13 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL13 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 55:52.
                                        ;--

023652                                          BGNTST
023652                                  T50::
023652  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
023656  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
023662  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

023670                                  1$:     BGNSEG
023670  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

023672  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
023676  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
023702  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
023704                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
023704  104455                                  TRAP    C$ERDF
023706  000001                                  .WORD   1
023710  000000                                  .WORD   0
023712  004606                                  .WORD   R0EROR
023714                                          CKLOOP
023714  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 59:48 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

023716  004537  006430          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 59:48
023722  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48

                                        ;SET PTER13 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER13 L IS ASSERTED, THE SIGNAL PLSL13 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 55:52.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

023724  012737  000015  002376                  MOV     #PTER13,R2LOAD          ;SETUP BITS TO BE LOADED
023732  004737  006136                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
023736  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
023740                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
023740  104455                                  TRAP    C$ERDF
023742  000002                                  .WORD   2
023744  000000                                  .WORD   0
023746  004706                                  .WORD   R2EROR
```

```
8806  023750                                  CKLOOP
8807  023750  104406                          TRAP    C$CLP1
8808
8809                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL13 L.
8810                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8811                                          ;PTER13 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA13 L.  THE
8812                                          ;SIGNAL WPLA13 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8813                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8814                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8815
8816                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL13 L WITH
8817                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8818
8819  023752  012737  000C12  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8820  023760  004737  006170                 JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8821  023764  001405                         BEQ     4$                      ;IF DATA OK THEN CONTINUE
8822  023766                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8823  023766  104455                         TRAP    C$ERDF
8824  023770  000003                         .WORD   3
8825  023772  003552                         .WORD   ANDERR
8826  023774  004722                         .WORD   R4EROR
8827  023776                                  CKLOOP
8828  023776  104406                         TRAP    C$CLP1
8829
8830                                          ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL13 L WITH
8831                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8832
8833  024000  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8834  024006  004737  006170                 JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8835  024012  001404                         BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8836  024014                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8837  024014  104455                         TRAP    C$ERDF
8838  024016  000003                         .WORD   3
8839  024020  003552                         .WORD   ANDERR
8840  024022  004722                         .WORD   R4EROR
8841  024024                          5$:     ENDSEG
8842  024024                          10000$:
8843  024024  104405                         TRAP    C$ESEG
8844
8845  024026  062737  000020  002414         ADD     #BIT4,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8846  024034  032737  000400  002414         BIT     #BIT8,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8847  024042  001712                         BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8848  024044                                  ENDTST
8849  024044                          L10151:
8850  024044  104401                         TRAP    C$ETST
8851
```

```
8852                                    .SBTTL  TEST 51: AND ARRAY RAM TEST - PLSL14 L (1'S + 0'S, 0'S + 1'S)
8853
8854                                    ;++
8855                                    ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
8856                                    ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
8857                                    ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
8858                                    ; SIGNAL PLSL14 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 59:56.
8859                                    ;--
8860
8861  024046                                    BGNTST
8862  024046                            T51::
8863  024046  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
8864  024052  005037  002414                   CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
8865  024056  012737  170377  002406           MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ
8866
8867  024064                            1$:     BGNSEG
8868  024064  104404                           TRAP    C$BSEG
8869
8870                                          ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
8871                                          ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
8872                                          ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
8873                                          ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
8874                                          ;BUFFERS (TRDI 59:0).
8875
8876  024066  105037  002370                   CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
8877  024072  004737  006104                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
8878  024076  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
8879  024100                                    ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
8880  024100  104455                           TRAP    C$ERDF
8881  024102  000001                           .WORD   1
8882  024104  000000                           .WORD   0
8883  024106  004606                           .WORD   R0FROR
8884  024110                                    CKLOOP
8885  024110  104406                           TRAP    C$CLP1
8886
8887                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 59:48 WITH
8888                                          ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
8889                                          ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.
8890
8891  024112  004537  006430           2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 59:48
8892  024116  000010                           .WORD   PTER8                   ;SELECT TRDI BITS 59:48
8893
8894                                          ;SET PTER14 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
8895                                          ;A ZERO AND THE SIGNAL PTER14 L IS ASSERTED, THE SIGNAL PLSL14 L WILL BE
8896                                          ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 59:56.
8897                                          ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
8898                                          ;REMAIN HIGH.
8899
8900  024120  012737  000016  002376           MOV     #PTER14,R2LOAD          ;SETUP BITS TO BE LOADED
8901  024126  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
8902  024132  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
8903  024134                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
8904  024134  104455                           TRAP    C$ERDF
8905  024136  000002                           .WORD   2
8906  024140  000000                           .WORD   0
8907  024142  004706                           .WORD   R2EROR
```

```
8908  024144                                    CKLOOP
8909  024144  104406                            TRAP    C$CLP1
8910
8911                                            ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL14 L.
8912                                            ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8913                                            ;PTER14 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA14 L.  THE
8914                                            ;SIGNAL WPLA14 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8915                                            ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8916                                            ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8917
8918                                            ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL14 L WITH
8919                                            ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8920
8921  024146  012737  000012  002402  3$:       MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8922  024154  004737  006170                    JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8923  024160  001405                            BEQ     4$                      ;IF DATA OK THEN CONTINUE
8924  024162                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8925  024162  104455                            TRAP    C$ERDF
8926  024164  000003                            .WORD   3
8927  024166  003552                            .WORD   ANDERR
8928  024170  004722                            .WORD   R4EROR
8929  024172                                    CKLOOP
8930  024172  104406                            TRAP    C$CLP1
8931
8932                                            ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL14 L WITH
8933                                            ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8934
8935  024174  012737  000005  002402  4$:       MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8936  024202  004737  006170                    JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8937  024206  001404                            BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8938  024210                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8939  024210  104455                            TRAP    C$ERDF
8940  024212  000003                            .WORD   3
8941  024214  003552                            .WORD   ANDERR
8942  024216  004722                            .WORD   R4EROR
8943  024220                            5$:     ENDSEG
8944  024220                            10000$:
8945  024220  104405                            TRAP    C$ESEG
8946
8947  024222  062737  000400  002414            ADD     #BIT8,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8948  024230  032737  010000  002414            BIT     #BIT12,R6LOAD           ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8949  024236  001712                            BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8950  024240                                    ENDTST
8951  024240                            L10152:
8952  024240  104401                            TRAP    C$ETST
8953
```

```
                                        .SBTTL  TEST 52: AND ARRAY SELECTION TEST

                                        ;++
                                        ; THIS TEST WILL CHECK THAT EACH AND ARRAY IS ACTUALLY SELECTED WHEN ADDRESSED
                                        ; BY THE PLSL SELECT LINE SIGNALS.  THE PLSL SELECT SIGNALS ARE GENERATED BY
                                        ; THE POINTER REGISTER PTER SIGNALS VIA CONTROL REGISTER 2.  THE TEST WILL
                                        ; CLEAR ALL TRACE RAM DATA IN BUFFER BITS TRDI 59:0.  WITH ALL THESE BITS
                                        ; BEING CLEARED, LOCATION 0 OF EACH AND ARRAY WILL BE ADDRESSED.  THE TEST WILL
                                        ; THEN SELECT EACH AND ARRAY BY LOADING THE APPROPRIATE PTER SIGNAL IN CONTROL
                                        ; REGISTER 2.  THE TEST WILL THEN LOAD, READ AND CHECK THE AND ARRAY WITH THE
                                        ; PTER SIGNAL USED TO SELECT THE AND ARRAY.  ONCE EACH AND ARRAY HAS BEEN
                                        ; LOADED AND CHECKED, THE TEST WILL THEN RESELECT EACH AND ARRAY CHECKING THE
                                        ; DATA TO BE EQUAL TO THE PTER SELECT SIGNAL.  IF ANY ERRORS OCCUR IN THE LAST
                                        ; PORTION OF THE TEST, THEN THE ERROR IS PROBABLY RELATED TO THE PLSL SIGNALS
                                        ; OR THE POINTER REGISTER PTER SIGNALS.  ONLY ONE SIGNAL SHOULD BE ENABLED AT
                                        ; A TIME.
                                        ;--

                                                BGNTST
                                        T52::
024242  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
024246  005037  002414                          CLR     R6LOAD                  ;DATA TO BE LOADED INTO TRAM DATA IN BUF
024252  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO LOOK AT AND ARRY BITS ONLY

                                                BGNSUB
                                        T52.1:
024260  104402                          1$:     TRAP    C$BSUB

                                        ;CLEAR CDAL4 IN CONTROL REGISTER 0. CDAL4 ON A ZERO WILL ALLOW ONLY
                                        ;ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER REGISTER.
                                        ;CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSL0 L WHICH WILL
                                        ;ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS.

024262  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
024266  004737  006104                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
024272  001405                                  BEQ     1$                      ;IF LOADED OK THEN CONTINUE
024274                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
024274  104455                                  TRAP    C$ERDF
024276  000001                                  .WORD   1
024300  000000                                  .WORD   0
024302  004606                                  .WORD   R0EROR
024304                                          CKLOOP
024304  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH A
                                        ;DATA PATTERN OF 0

024306  004537  006430                  1$:     JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
024312  000005                                  .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH A
                                        ;DATA PATTERN OF 0

024314  004537  006430                          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
024320  000006                                  .WORD   PTER6                   ;SELECT TRDI BITS 31:16
```

```
                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH A
                                        ;DATA PATTERN OF 0.

024322  004537  006430                JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
024326  000007                        .WORD   PTER7                   ;SELECT TRDI BITS 47:32

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 59:48 WITH A
                                        ;DATA PATTERN OF 0

024330  004537  006430                JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
024334  000010                        .WORD   PTER8                   ;SELECT TRDI BITS 59:48
024336                                ENDSUB
024336                          L10154:
024336  104403                        TRAP    C$ESUB

024340                                BGNSUB
024340                          T52.2:
024340  104402                        TRAP    C$BSUB

                                        ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER
                                        ;0.  ALL THE TRACE RAM DATA IN BUFFER BITS TRDI 59:0 WILL BE CLEARED.
                                        ;THE TRDI BITS ARE USED TO ADDRESS THE AND ARRAYS.  THIS SUBTEST WILL
                                        ;WRITE INTO AND CHECK LOCATION 0 OF EACH AND ARRAY WITH THE PTER SIGNAL
                                        ;WHICH SELECTS THE AND ARRAY.

024342  012737  000000  002376        MOV     #PTER0,R2LOAD           ;SETUP TO START WITH 1ST AND ARRAY

024350                          1$:     BGNSEG
024350  104404                        TRAP    C$BSEG

024352  004737  006136                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
024356  001405                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
024360                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
024360  104455                        TRAP    C$ERDF
024362  000002                        .WORD   2
024364  000000                        .WORD   0
024366  004706                        .WORD   R2EROR
024370                                CKLOOP
024370  104406                        TRAP    C$CLP1

                                        ;LOAD READ AND CHECK AND ARRAY WITH THE PTER SIGNAL WHICH SELECTS THE
                                        ;AND ARRAY.

024372  013737  002376  002402  2$:   MOV     R2LOAD,R4LOAD           ;GET THE PTER SIGNAL USED
024400  004737  006170                JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
024404  001404                        BEQ     3$                      ;IF LOADED OK THEN CONTINUE
024406                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL PTER SIGNAL
024406  104455                        TRAP    C$ERDF
024410  000003                        .WORD   3
024412  003552                        .WORD   ANDERR
024414  004722                        .WORD   R4EROR
024416                          3$:   ENDSEG
024416                          10000$:
024416  104405                        TRAP    C$ESEG
024420  005237  002376                INC     R2LOAD                  ;UPDATE THE PTER SIGNAL BY ONE
024424  022737  000017  002376        CMP     #PTER15,R2LOAD          ;CHECK IF ALL AND ARRAYS WRITTEN
```

```
9066  024432  001346                          BNE     1$                      ;IF NOT THEN LOAD NEXT AND ARRAY
9067  024434                                  ENDSUB
9068  024434                          L10155:
9069  024434  104403                          TRAP    C$ESUB
9070
9071  024436                                  BGNSUB
9072  024436                          T52.3:
9073  024436  104402                          TRAP    C$BSUB
9074
9075                                          ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER
9076                                          ;0.  ALL TRACE RAM DATA IN BUFFER BITS TRDI 59:0 WILL BE CLEARED.
9077                                          ;LOCATION 0 OF EACH AND ARRAY WILL CONTAIN AS DATA THE PTER SIGNAL
9078                                          ;WHICH SELECTS THE AND ARRAY.  THIS SUB TEST WILL READ LOCATION 0
9079                                          ;OF EACH AND ARRAY CHECKING THE DATA TO EQUAL THE PTER SELECT SIGNAL.
9080                                          ;THIS SUB TEST CHECKS THAT EACH AND ARRAY CAN BE SELECTED.
9081
9082  024440  012737  000000  002376          MOV     #PTER0,R2LOAD           ;SETUP TO START WITH THE 1ST AND ARRAY
9083  024446                          1$:     BGNSEG
9084  024446  104404                          TRAP    C$BSEG
9085
9086  024450  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK PEGISTER 2
9087  024454  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
9088  024456                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9089  024456  104455                          TRAP    C$ERDF
9090  024460  000002                          .WORD   2
9091  024462  000000                          .WORD   0
9092  024464  004706                          .WORD   R2EROR
9093  024466                                  CKLOOP
9094  024466  104406                          TRAP    C$CLP1
9095
9096                                          ;READ AND ARRAY CHECKING THE DATA TO EQUAL THE SELECT PTER SIGNAL
9097
9098  024470  013737  002376  002402  2$:     MOV     R2LOAD,R4LOAD           ;GET THE PTER SELECT SIGNAL
9099  024476  013737  002402  002404          MOV     R4LOAD,R4GOOD           ;COPY IT INTO EXPECTED DATA
9100  024504  000337  002404                  SWAB    R4GOOD                  ;PUT ACTUAL BITS IN EXPECTED READBACK
9101  024510  004737  006220                  JSR     PC,READR4               ;GO READ AND CHECK AND ARRAY
9102  024514  001404                          BEQ     3$                      ;IF EQUAL EXPECTED THEN CONTINUE
9103  024516                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY SELECTION ERROR
9104  024516  104455                          TRAP    C$ERDF
9105  024520  000003                          .WORD   3
9106  024522  003552                          .WORD   ANDERR
9107  024524  004722                          .WORD   R4EROR
9108  024526                          3$:     ENDSEG
9109  024526                          10000$:
9110  024526  104405                          TRAP    C$ESEG
9111  024530  005237  002376                  INC     R2LOAD                  ;UPDATE THE PTER SIGNAL
9112  024534  022737  000017  002376          CMP     #PTER15,R2LOAD          ;CHECK IF DONE ALL AND ARRAYS
9113  024542  001341                          BNE     1$                      ;IF NOT THE GO CHECK NEXT AND ARRAY
9114  024544                                  ENDSUB
9115  024544                          L10156:
9116  024544  104403                          TRAP    C$ESUB
9117  024546                                  ENDTST
9118  024546                          L10153:
9119  024546  104401                          TRAP    C$ETST
```

```
                                        .SBTTL  TEST 53: AND ARRAY RAM(S) ADDRESS/SHORT TEST

                                        ;++
                                        ; THIS TEST WILL CHECK THAT EACH AND ARRAY RAM CAN BE ADDRESSED CORRECTLY AND
                                        ; THAT WRITING ONE LOCATION IN THE AND ARRAY DOES NOT WRITE A HIGHER LOCATION
                                        ; AT THE SAME TIME (ADDRESS SHORT).  THE TEST WILL CHECK ONE AND ARRAY RAM AT
                                        ; A TIME UNTIL ALL AND ARRAY RAMS ARE TESTED.  THE TEST WILL LOAD AND CHECK
                                        ; EACH LOCATION OF A 16*4 AND ARRAY WITH DATA EQUAL TO THE ADDRESS SELECTED
                                        ; (0-17 OCTAL).  ONCE ALL THE LOCATIONS HAVE BEEN WRITTEN AND CHECKED, THE TEST
                                        ; WILL START AT THE BEIGNNING ADDRESS OF THE AND ARRAY AND DO THE FOLLOWING:
                                        ;    1.  READ LOCATION CHECKING DATA TO EQUAL THE ADDRESS (0-17 OCTAL)
                                        ;    2.  WRITE AND CHECK LOCATION WITH 1'S COMPLEMENT OF THE ADDRESS
                                        ;    3.  SEQUENCE TO THE NEXT ADDRESS
                                        ;    4.  REPEAT STEPS 1-3 UNTIL ALL ADDRESSES HAVE BEEN CHECKED.
                                        ; WHEN THE ABOVE SEQUENCE HAS BEEN COMPLETED, THE TEST WILL RESET THE ADDRESS
                                        ; TO THE BEGINNING ADDRESS OF THE AND ARRAY AND CHECK EACH LOCATION TO CONTAIN
                                        ; THE 1'S COMPLEMENT OF THE ADDRESS.
                                        ;--

024550                                          BGNTST
024550                                  T53::
024550  004737  005476                           JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

024554  012737  170377  002406                   MOV     #170377,R4MASK          ;SETUP AND ARRAY MASK WORD
024562  005001                                   CLR     R1                      ;CLEAR ADDRESS/DATA COUNTER
024564  012702  000005                           MOV     #PTER5,R2               ;TRAM DATA IN BUFFER SELECTION
024570  012703  000000                           MOV     #PTER0,R3               ;AND ARRAY SELECTION
024574  012704  000001                           MOV     #1,R4                   ;# TO BE ADDED TO TRDI BITS TO GET NEXT
                                                                                 ;AND ARRAY ADDRESS
024600  005037  002414                           CLR     R6LOAD                  ;START AND ARRAY ADDRESS OFF AT 0

024604                                  1$:     BGNSEG
024604  104404                                  TRAP    C$BSEG

                                                ;CLEAR CDAL4 IN CONTROL REGISTER 0 TO SELECT ONLY ONE AND/OR ARRAY
                                                ;VIA THE POINTER REGISTER.  CDAL3 AND CDAL2 ON A 0 WILL ASSERT THE
                                                ;SIGNAL TRSL0 L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA
                                                ;IN BUFFER SELECTED.

024606  105037  002370                           CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
024612  004737  006104                           JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
024616  001405                                   BEQ     2$                      ;IF LOADED OK THEN CONTINUE
024620                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
024620  104455                                  TRAP    C$ERDF
024622  000001                                  .WORD   1
024624  000000                                  .WORD   0
024626  004606                                  .WORD   R0EROR
024630                                          CKLOOP
024630  104406                                  TRAP    C$CLP1

                                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0, 31:16,
                                                ;47:32 OR 59:48 WITH DATA STORED IN LOCATION "R6LOAD".

024632  010237  024642                  2$:     MOV     R2,3$                   ;GET THE TRAM DATA IN BUF SELECTION
024636  004537  006430                           JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
024642  000005                          3$:     .WORD   PTER5                   ;PTER5, PTER6, PTER7, OR PTER8
```

```
9176
9177                                        ;SELECT THE AND ARRAY TO BE TESTED VIA CONTROL REGISTER 2 WITH THE
9178                                        ;PTER SIGNAL IN GENERAL CPU REGISTER R3
9179
9180  024644  010337  002376                MOV     R3,R2LOAD               ;GET THE PTER SELECT SIGNAL
9181  024650  004737  006136                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9182  024654  001405                        BEQ     4$                      ;IF LOADED OK THEN CONTINUE
9183  024656                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9184  024656  104455                        TRAP    C$ERDF
9185  024660  000002                        .WORD   2
9186  024662  000000                        .WORD   0
9187  024664  004706                        .WORD   R2EROR
9188  024666                                CKLOOP
9189  024666  104406                        TRAP    C$CLP1
9190
9191                                        ;LOAD, READ AND CHECK AND ARRAY WITH DATA EQUAL TO ADDRESS SELECTED
9192
9193  024670  010137  002402        4$:     MOV     R1,R4LOAD               ;GET THE ADDRESS BEING TESTED
9194  024674  004737  006170                JSR     PC,LDRDAR               ;GO LOAD, READ AND CEHCK AND ARRAY
9195  024700  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
9196  024702                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR SELECTED VIA REG 2
9197  024702  104455                        TRAP    C$ERDF
9198  024704  000003                        .WORD   3
9199  024706  003552                        .WORD   ANDERR
9200  024710  004722                        .WORD   R4EROR
9201  024712                        5$:     ENDSEG
9202  024712                        10000$:
9203  024712  104405                        TRAP    C$ESEG
9204
9205  024714  060437  002414                ADD     R4,R6LOAD               ;UPDATE AND ARRAY ADDRESS TO NEXT
9206                                                                        ;SEQUENTIAL ADDRESS
9207  024720  005201                        INC     R1                      ;UPDATE ADDRESS/DATA COUNTER
9208  024722  022701  000020                CMP     #20,R1                  ;CHECK IF ALL 16 ADDRESSES DONE
9209  024726  001326                        BNE     1$                      ;IF NOT - DO NEXT ADDRESS OF AND ARRAY
9210
9211  024730  005001                        CLR     R1                      ;RESET ADDRESS/DATA COUNTER
9212  024732  005037  002414                CLR     R6LOAD                  ;RESET AND ARRAY ADDRESS TO 0
9213
9214  024736                        6$:     BGNSEG
9215  024736  104404                        TRAP    C$BSEG
9216
9217                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0, 31:16,
9218                                        ;47:32, OR 59:48 WITH DATA STORED IN LOCATION "R6LOAD".
9219
9220  024740  010237  024750                MOV     R2,7$                   ;GET TRAM DATA IN BUFFER SELECTION
9221  024744  004537  006430                JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
9222  024750  000005                7$:     .WORD   PTER5                   ;PTER5, PTER6, PTER7 OR PTER8
9223
9224                                        ;SELECT THE AND ARRAY TO BE TESTED VIA CONTROL REGISTER 2 WITH THE
9225                                        ;PTER SIGNAL IN GENERAL CPU REGISTER R3
9226
9227  024752  010337  002376                MOV     R3,R2LOAD               ;GET THE PTER SIGNAL TO BE LOADED
9228  024756  004737  006136                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
9229  024762  001405                        BEQ     8$                      ;IF LOADED OK THEN CONTINUE
9230  024764                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9231  024764  104455                        TRAP    C$ERDF
```

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9232  024766  000002                          .WORD   2
9233  024770  000000                          .WORD   0
9234  024772  004706                          .WORD   R2EROR
9235  024774                                  CKLOOP
9236  024774  104406                          TRAP    C$CLP1
9237
9238                                          ;READ AND CHECK AND ARRAY LOCATION TO EQUAL DATA PREVIOUSLY LOADED.
9239                                          ;THE DATA SHOULD EQUAL THE ADDRESS OF THE AND ARRAY (0-17 OCTAL).
9240
9241  024776  010137  002402          8$:     MOV     R1,R4LOAD               ;SETUP DATA PREVIOULSY LOADED
9242  025002  013737  002402  002404          MOV     R4LOAD,R4GOOD           ;COPY IT TO EXPECTED DATA
9243  025010  000337  002404                  SWAB    R4GOOD                  ;PUT EXPECTED DATA IN ACTUAL READBACK
9244  025014  004737  006220                  JSR     PC,READR4               ;GO READ AND CHECK AND ARRAY LOCATION
9245  025020  001404                          BEQ     9$                      ;IF DATA OK THEN CONTINUE
9246  025022                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR OR ADDRESSING ERROR
9247  025022  104455                          TRAP    C$ERDF
9248  025024  000003                          .WORD   3
9249  025026  003552                          .WORD   ANDERR
9250  025030  004722                          .WORD   R4EROR
9251  025032                          9$:     ENDSEG
9252  025032                          10001$:
9253  025032  104405                          TRAP    C$ESEG
9254
9255  025034  005137  002402                  COM     R4LOAD                  ;COMPLEMENT THE ADDRESS
9256  025040  042737  177760  002402          BIC     #177760,R4LOAD          ;CLEAR UNWANTED BITS
9257
9258  025046                                  BGNSEG
9259  025046  104404                          TRAP    C$BSEG
9260
9261                                          ;WRITE, READ AND CHECK AND ARRAY WITH THE 1'S COMPLEMENT OF THE ADDRESS
9262                                          ;BEING TESTED.
9263
9264  025050  004737  006170                  JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
9265  025054  001404                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
9266  025056                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA EROR
9267  025056  104455                          TRAP    C$ERDF
9268  025060  000003                          .WORD   3
9269  025062  003552                          .WORD   ANDERR
9270  025064  004722                          .WORD   R4EROR
9271  025066                          10$:    ENDSEG
9272  025066                          10002$:
9273  025066  104405                          TRAP    C$ESEG
9274
9275  025070  060437  002414                  ADD     R4,R6LOAD               ;UPDATE AND ARRAY ADDRESS BY UPDATING
9276                                                                          ;TRAM DATA IN BUFFER BITS
9277  025074  005201                          INC     R1                      ;UPDATE ADDRESS/DATA COUNTER
9278  025076  022701  000020                  CMP     #20,R1                  ;CHECK IF ALL 16 ADDRESS BEEN TESTED
9279  025102  001315                          BNE     6$                      ;IF NOT THEN CHECK NEXT ADDRESS
9280
9281  025104  005001                          CLR     R1                      ;CLEAR ADDRESS/DATA COUNTER
9282  025106  005037  002414                  CLR     R6LOAD                  ;RESET AND ARRAY ADDRESS TO 0
9283
9284  025112                          11$:    BGNSEG
9285  025112  104404                          TRAP    C$BSEG
9286
9287                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0, 31:16,
```

```
 9288                                          ;47:32, OR 59:48 WITH DATA IN LOCATION 'R6LOAD'.
 9289
 9290  025114  010237  025124                  MOV     R2,12$                  ;GET TRAM DATA IN BUFFER SELECTION
 9291  025120  004537  006430                  JSR     R5,TRDIBF               ;LOAD READ AND CHECK TRAM DATA IN BUF
 9292  025124  000005                  12$:    .WORD   PTER5                   ;PTER5, PTER6, PTER7 OR PTER8
 9293
 9294                                          ;SELECT AND ARRAY TO BE TESTED VIA CONTROL REGISTER 2 WITH THE PTER
 9295                                          ;SIGNAL IN GENERAL REGISTER R3.
 9296
 9297  025126  010337  002376                  MOV     R3,R2LOAD               ;GET THE PTER SIGNAL TO BE LOADED
 9298  025132  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
 9299  025136  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
 9300  025140                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
 9301  025140  104455                          TRAP    C$ERDF
 9302  025142  000002                          .WORD   2
 9303  025144  000000                          .WORD   0
 9304  025146  004706                          .WORD   R2EROR
 9305  025150                                  CKLOOP
 9306  025150  104406                          TRAP    C$CLP1
 9307
 9308                                          ;READ, AND CHECK AND ARRAY LOCATION TO EQUAL THE 1'S COMPLEMENT OF THE
 9309                                          ;ADDRESS SELECTED BY THE TRDI BITS.
 9310
 9311  025152  010137  002402          13$:    MOV     R1,R4LOAD               ;GET THE ADDRESS/DATA COUNTER
 9312  025156  005137  002402                  COM     R4LOAD                  ;MAKE THE 1'S COMPLEMENT
 9313  025162  042737  177760  002402          BIC     #177760,R4LOAD          ;CLEAR UNWANTED BITS
 9314  025170  013737  002402  002404          MOV     R4LOAD,R4GOOD           ;COPY DATA INTO EXPECTED DATA
 9315  025176  000337  002404                  SWAB    R4GOOD                  ;PUT EXPECTED DATA IN READBACK BITS
 9316  025202  004737  006220                  JSR     PC,READR4               ;GO READ AND CHECK AND ARRAY
 9317  025206  001404                          BEQ     14$                     ;IF DATA OK THEN CONTINUE
 9318  025210                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR/OR ADDRESS SHORT
 9319  025210  104455                          TRAP    C$ERDF
 9320  025212  000003                          .WORD   3
 9321  025214  003552                          .WORD   ANDERR
 9322  025216  004722                          .WORD   R4EROR
 9323  025220                          14$:    ENDSEG
 9324  025220                          10003$:
 9325  025220  104405                          TRAP    C$ESEG
 9326
 9327  025222  060437  002414                  ADD     R4,R6LOAD               ;UPDATE TRAM DATA IN BUFFER BITS USED
 9328                                                                          ;FOR ADDRESS SELECTION
 9329  025226  005201                          INC     R1                      ;UPDATE ADDRESS/DATA COUNTER
 9330  025230  022701  000020                  CMP     #20,R1                  ;CHECK IF ALL 16 ADDRESSES TESTED
 9331  025234  001326                          BNE     11$                     ;IF NOT THEN TEST NEXT ADDRESS
 9332
 9333  025236  005001                          CLR     R1                      ;CLEAR ADDRESS/DATA COUNTER
 9334  025240  005037  002414                  CLR     R6LOAD                  ;RESET AND ARRAY ADDRESS TO 0
 9335
 9336  025244  022702  000010                  CMP     #PTER8,R2               ;CHECK IF LAST SET OF DATA IN BUFFERS
 9337  025250  001004                          BNE     15$                     ;IF NOT THEN CONTINUE
 9338  025252  022704  000400                  CMP     #BIT8,R4                ;CHECK IF ALL AND ARRAYS DONE
 9339  025256  001004                          BNE     16$                     ;IF NOT THEN DO NEXT AND ARRAY
 9340  025260  000420                          BR      18$                     ;EXIT THE TEST
 9341  025262  022704  010000          15$:    CMP     #BIT12,R4               ;CHECK IF END OF THIS SET OF DATA IN BUF
 9342  025266  001407                          BEQ     17$                     ;IF YES THEN GO UPDATE PTER SELECTS
 9343  025270  006304                  16$:    ASL     R4                      ;UPDATE TRDI AND ARRAY ADDRESS SELECTION
```

```
 9344  025272  006304                          ASL     R4                      ;
 9345  025274  006304                          ASL     R4
 9346  025276  006304                          ASL     R4
 9347  025300  005203                          INC     R3                      ;UPDATE AND ARRAY PTER SELECT SIGNAL
 9348  025302  000137  024604                  JMP     1$                      ;GO DO NEXT AND ARRAY IN THIS SET
 9349  025306  005202                  17$:    INC     R2                      ;UPDATE TRAM DATA IN BUFFER SELECTION
 9350  025310  005203                          INC     R3                      ;UPDATE AND ARAY PTER SELECT SIGNAL
 9351  025312  012704  000001                  MOV     #1,R4                   ;RESET TRDI AND ARRAY ADDRESS SELECTION
 9352  025316  000137  024604                  JMP     1$                      ;GO DO NEXT SET OF AND ARRAYS
 9353  025322                          18$:    ENDTST
 9354  025322                          L10157:
 9355  025322  104401                          TRAP    C$ETST
 9356
```

```
                                        .SBTTL  TEST 54: EVENT COUNTER 0 AND 2 TEST

                                        ;++
                                        ; THIS TEST WILL CHECKOUT EVENT COUNTER LOGIC FOR EVENT COUNTER 0 AND 2.  THE
                                        ; TEST WILL CHECK THAT THE EVENT COUNTER REGISTERS AND EVENT COUNTERS ARE LOAD-
                                        ; ED CORRECTLY BY COUNTING DOWN THE EVENT COUNTERS AND CHECKING THE FOUT FLIP-
                                        ; FLOPS FOR A BORROW.  WHEN THE EVENT COUNTERS ARE COUNTED DOWN TO ZERO AND ONE
                                        ; MORE COUNT DOWN IS ISSUED, A BORROW IS GENERATED WHICH WILL SET THE OUTPUT OF
                                        ; THE FOUT FLIP-FLOP TO A LOW STATE.  THE TEST WILL CHECK THAT THE EVENT COUNTERS
                                        ; ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN A BORROW IS GENERATED. THIS
                                        ; IS DONE BY COUNTING DOWN THE EVENT COUNTERS AGAIN CHECKING FOR A BORROW FROM
                                        ; THE EVENT COUNTERS.  THE TEST WILL THEN CHECK THAT THE EVENT COUNTERS CAN BE
                                        ; CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7.  AFTER SETTING AND CLEARING
                                        ; THE SIGNAL PDAL7, THE TEST WILL DO ONE MORE COUNT DOWN AND CHECK THAT A BORROW
                                        ; IS GENERATED FROM THE EVENT COUNTERS.  THE ABOVE SEQUENCE IS REPEATED FOR EACH
                                        ; OF THE FOLLOWING DATA PATTERNS: 0, 1, 2, 4, 10, 20, 40, 100, 200, 125 AND 252.
                                        ;--

 025324                                         BGNTST
 025324                                 T54::
 025324  004737  005476                         JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

 025330                                         BGNSEG
 025330  104404                                 TRAP    C$BSEG

                                                ;SET CDAL4 TO A ZERO IN CONTROL REGISTER 0.  CDAL4 BEING A 0 WILL ALLOW
                                                ;ONLY ONE AND/OR ARRAY TO BE SELECTED AT A TIME.  CDAL3 AND CDAL2 ON A
                                                ;ZERO WILL CAUSE THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE
                                                ;OUTPUTS OF THE TRACE RAM DATA IN BUFFERS.  THESE OUTPUTS ARE USED TO
                                                ;ADDRESS THE AND ARRAYS.

 025332  105037  002370                         CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
 025336  004737  006104                         JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
 025342  001405                                 BEQ     1$                      ;IF LOADED OK THEN CONTINUE
 025344                                         ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
 025344  104455                                 TRAP    C$ERDF
 025346  000001                                 .WORD   1
 025350  000000                                 .WORD   0
 025352  004606                                 .WORD   ROEROR
 025354                                         CKLOOP
 025354  104406                                 TRAP    C$CLP1

                                                ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER TRDI 15:0.  ALL ZEROES
                                                ;WILL SELECT ADDRESS 0 OF THE AND ARRAY TO BE USED IN THIS TEST.

 025356  005037  002414         1$:            CLR     R6LOAD                  ;SETUP TO LOAD ZEROES
 025362  004537  006430                         JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
 025366  000005                                 .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                                ;SET PTER0 IN THE POINTER REGISTER VIA CONTROL REGISTER 2.  THIS WILL
                                                ;SELECT THE FIRST AND ARRAY VIA THE SIGNAL PLSLO L.

 025370  012737  000000  002376                 MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
 025376  004737  006136                         JSR     PC,LDRDR2               ;GO LOAD, READ AND CEHCK REGISTER 2
 025402  001405                                 BEQ     2$                      ;IF LOADED OK THEN CONTINUE
 025404                                         ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
```

```
 9413  025404  104455                          TRAP    C$ERDF
 9414  025406  000002                          .WORD   2
 9415  025410  000000                          .WORD   0
 9416  025412  004706                          .WORD   R2EROR
 9417  025414                                  CKLOOP
 9418  025414  104406                          TRAP    C$CLP1
 9419
 9420                                          ;LOAD, READ AND CHECK AND ARRAY RAM WITH DATA PATTERN OF 12.  THIS DATA
 9421                                          :PATTERN WILL SET THE SIGNALS ANDO L AND AND2 L TO THE HIGH STATE AND
 9422                                          ;THE SIGNALS AND1 L AND AND3 L TO THE LOW STATE.  WITH ANDO L AND AND2 L
 9423                                          ;SET HIGH AND THE SIGNAL ANST L BEING PULSED, A PULSE WILL OCCUR
 9424                                          ;ON THE SIGNALS CNDNO H AND CNDN2 H.  THESE SIGNALS WILL COUNT DOWN
 9425                                          ;EVENT COUNTERS 0 AND 2.
 9426
 9427  025416  012737  000012  002402  2$:     MOV     #12,R4LOAD              ;SETUP DATA PATTERN TO BE LOADED
 9428  025424  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
 9429  025432  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY
 9430  025436  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
 9431  025440                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
 9432  025440  104455                          TRAP    C$ERDF
 9433  025442  000003                          .WORD   3
 9434  025444  003552                          .WORD   ANDERR
 9435  025446  004722                          .WORD   R4EROR
 9436  025450                          3$:     ENDSEG
 9437  025450                          10000$:
 9438  025450  104405                          TRAP    C$ESEG
 9439
 9440  025452  005001                          CLR     R1                      ;START EVENT COUNTERS OFF AT 0
 9441
 9442  025454                          4$:     BGNSEG
 9443  025454  104404                          TRAP    C$BSEG
 9444  025456  010102                          MOV     R1,R2                   ;COPY STARTING EVENT COUNTER TO WORKING
 9445
 9446                                          ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0. CDAL7 ON A ONE WILL ALLOW
 9447                                          ;THE FOUT FLIP-FLOPS TO BE READ ON THE OR ADDRESS REGISTER LINES ORAD 3:0.
 9448
 9449  025460  052737  000200  002370          BIS     #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
 9450  025466  004737  006104                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHEKC REGISTER 0
 9451  025472  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
 9452  025474                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
 9453  025474  104455                          TRAP    C$ERDF
 9454  025476  000001                          .WORD   1
 9455  025500  000000                          .WORD   0
 9456  025502  004606                          .WORD   ROEROR
 9457  025504                                  CKLOOP
 9458  025504  104406                          TRAP    C$CLP1
 9459
 9460                                          ;SET AND CLEAR PDAL7 IN CONTROL REGISTER 2. PDAL7 BEING SET WILL
 9461                                          ;CLEAR ALL THE EVENT COUNTERS.
 9462
 9463  025506  052737  000200  002376  5$:     BIS     #PDAL7,R2LOAD           ;SETUP BIT TO BE LOADED
 9464  025514  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
 9465  025520  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
 9466  025522                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
 9467  025522  104455                          TRAP    C$ERDF
 9468  025524  000002                          .WORD   2
```

```
9469  025526  000000                          .WORD   0
9470  025530  004706                          .WORD   R2EROR
9471  025532                                  CKLOOP
9472  025532  104406                          TRAP    C$CLP1
9473
9474                                          ;CLEAR PDAL7 AND LOAD ALL EVENT COUNTER REGISTERS AND EVENT COUNTERS
9475                                          ;WITH THE WORKING EVENT COUNT STORED IN GENERAL CPU REGISTER R2.  THE
9476                                          ;SIGNALS ISSUED IN THE FOLLOWING LOOP ARE WPT9 H, WPTA L, WPT10 H,
9477                                          ;WPTB L, WPT11 H, WPTC L, WPT12 H, AND WPTD L.  THESE SIGNALS ARE USED
9478                                          ;TO LOAD THE DATA INTO THE EVENT COUNTER REGISTERS AND EVENT COUNTERS
9479                                          ;ON A WRITE COMMAND TO CONTROL REGISTER 6.
9480
9481  025534  012737  000011  002376  6$:     MOV     #PTER9,R2LOAD           ;SETUP BITS TO BE LOADED
9482  025542  004737  006136          7$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9483  025546  001405                          BEQ     8$                      ;IF LOADED OK THEN CONTINUE
9484  025550                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9485  025550  104455                          TRAP    C$ERDF
9486  025552  000002                          .WORD   2
9487  025554  000000                          .WORD   0
9488  025556  004706                          .WORD   R2EROR
9489  025560                                  CKLOOP
9490  025560  104406                          TRAP    C$CLP1
9491
9492  025562  010277  154570          8$:     MOV     R2,@REG6                ;LOAD EVENT COUNTERS AND REGISTERS
9493  025566  005237  002376                  INC     R2LOAD                  ;UPDATE TO NEXT POINTER
9494  025572  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL COUNTER S LOADED
9495  025600  001360                          BNE     7$                      ;IF NOT THEN LOAD NEXT COUNTER
9496
9497                                          ;RESELECT THE AND ARRAY SO THAT THE SIGNALS ANDO L AND AND2 L WILL BE
9498                                          ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST.
9499
9500  025602  012737  000000  002376  9$:     MOV     #PTER0,R2LOAD           ;SETUP TO SELECT FIRST AND ARRAY
9501  025610  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9502  025614  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
9503  025616                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9504  025616  104455                          TRAP    C$ERDF
9505  025620  000002                          .WORD   2
9506  025622  000000                          .WORD   0
9507  025624  004706                          .WORD   R2EROR
9508  025626                                  CKLOOP
9509  025626  104406                          TRAP    C$CLP1
9510
9511                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
9512                                          ;CLEARED WILL CAUSE THE SIGNAL TRANST H TO PULSE WHICH WILL CAUSE
9513                                          ;THE SIGNAL ANST L TO PULSE.  THE SIGNAL ANST L BEING PULSED WITH THE
9514                                          ;SIGNALS ANDO L AND AND2 L SET HIGH, WILL CAUSE A PULSE OF THE SIGNALS
9515                                          ;CNDNO H AND CNDN2 H.  THESE SIGNALS WILL CAUSE EVENT COUNTER 0 AND
9516                                          ;EVENT COUNTER 2 TO COUNT DOWN BY ONE RESPECTIVELY.
9517
9518  025630  004737  006642          10$:    JSR     PC,TRANST               ;GO SET AND CLEAR CDAL6 IN CONTROL REG 0
9519
9520                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTRCL REG 2.
9521
9522  025634  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER15
9523  025640  000017                          .WORD   PTER15
9524
```

```
9525                                        ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
9526                                        ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD 3:0
9527                                        ;WILL BE READ BACK.  IN THIS TEST. CDAL7 IS SET TO A ONE, WHICH WILL
9528                                        ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON ORAD 3:0 SIGNAL LINES.
9529                                        ;THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA A BORROW FROM THE EVENT COUNTERS
9530                                        ;AND THE SIGNAL ANST L BEING PULSED.
9531
9532  025642  005037  002414          11$:  CLR     P6LOAD                ;SETUP EXPECTED DATA
9533  025646  005702                        TST     R2                    ;CHECK IF EVENT COUNTER = 0
9534  025650  001003                        BNE     12$                   ;IF NOT THEN A BORROW SHOULD NOT OCCUR
9535  025652  012737  000005  002414        MOV     #5,R6LOAD             ;SETUP TO EXPECT A BORROW FROM COUNTER
9536                                                                      ;0 AND COUNTER 2 ON SIGNALS FOUT0 L AND
9537                                                                      ;FOUT2 L.
9538  025660  017737  154472  002420  12$:  MOV     @REG6,R6READ          ;READ FOUT 3:0 BITS ON ORAD 3:0
9539  025666  042737  177760  002420        BIC     #177760,R6READ        ;CLEAR UNWANTED BITS
9540  025674  023737  002414  002420        CMP     R6LOAD,R6READ         ;CHECK EXPECTED RESULTS AGAINST ACTUAL
9541  025702  001405                        BEQ     13$                   ;IF EQUAL THEN CONTINUE
9542  025704                                ERRDF   4,EVNTCT,EVNTER       ;EVENT COUNTER OR FOUT 3:0 ERROR
9543  025704  104455                        TRAP    C$ERDF
9544  025706  000004                        .WORD   4
9545  025710  003215                        .WORD   EVNTCT
9546  025712  005026                        .WORD   EVNTER
9547  025714                                CKLOOP
9548  025714  104406                        TRAP    C$CLP1
9549  025716  005302                  13$:  DEC     R2                    ;DECREMENT WORKING EVENT COUNTER
9550  025720  100330                        BPL     9$                    ;IF NOT DONE THEN COUNT DOWN AGAIN
9551
9552                                        ;WHEN THE FOUT FLIP-FLOP IS CLEARED BY A BORROW, THE EVENT COUNTERS
9553                                        ;ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE SIGNAL ORST L
9554                                        ;IS PULSED VIA THE PULSING OF SIGNAL ANST L.  THE FOLLOWING SECTION
9555                                        ;OF CODE WILL CHECK THAT THIS HAPPENS BY COUNTING DOWN THE EVENT
9556                                        ;COUNTERS AGAIN.
9557
9558  025722  010102                        MOV     R1,R2                 ;RESET EXPECTED CONTENTS OF EVENT CNTRS
9559
9560                                        ;RESELECT THE AND ARRAY SO THAT THE SIGNALS ANDO L AND AND2 L WILL BE
9561                                        ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGIMENT OF THIS TEST
9562
9563  025724  012737  000000  002376  14$:  MOV     #PTER0,R2LOAD         ;SETUP BITS TO BE LOADED
9564  025732  004737  006136                JSR     PC,LDRDR2             ;GO LOAD, READ AND CHECK REGISTER 2
9565  025736  001405                        BEQ     15$                   ;IF LOADED OK THEN CONTINUE
9566  025740                                ERRDF   2,,R2EROR             ;REGISTER 2 NOT EQUAL EXPECTED
9567  025740  104455                        TRAP    C$ERDF
9568  025742  000002                        .WORD   2
9569  025744  000000                        .WORD   0
9570  025746  004706                        .WORD   R2EROR
9571  025750                                CKLOOP
9572  025750  104406                        TRAP    C$CLP1
9573
9574                                        ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
9575                                        ;CLEARED WILL CAUSE A PULSE ON TRANST H WHICH WILL CAUSE THE SIGNAL
9576                                        ;ANST L TO PULSE.  THE SIGNAL ANST L BEING PULSED WITH THE
9577                                        ;SIGNALS ANDO L AND AND2 L SET HIGH WILL CAUSE A PULSE ON THE SIGNALS
9578                                        ;CNDNO H AND CNDN2 H.  THESE SIGNALS WILL CAUSE EVENT COUNTER 0 AND 2
9579                                        ;TO BE COUNTED DOWN BY ONE RESPECTIVELY.
9580
```

```
9581  025752  004737  006642          15$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
9582
9583                                          ;ASSERT THE SIGNAL PTER15 L IN POINTER REGISTER VIA CONTROL REG 2.
9584
9585  025756  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER15
9586  025762  000017                          .WORD   PTER15
9587
9588                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
9589                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS,
9590                                          ;ORAD 3:0, WILL BE READBACK. IN THIS TEST, CDAL7 IS SET TO A ONE,
9591                                          ;WHICH WILL CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE
9592                                          ;ORAD 3:0 SIGNAL LINES.  THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA THE
9593                                          ;BORROW SIGNAL FROM THE EVENT COUNTERS AND THE SIGNAL ANST L BEING
9594                                          ;PULSED.
9595
9596  025764  005037  002414          16$:    CLR     R6LOAD                  ;SETUP EXPECTED FOUT SIGNALS
9597  025770  005702                          TST     R2                      ;CHECK IF EVENT COUNTER WERE ZERO
9598  025772  001003                          BNE     17$                     ;IF NOT THEN A BORROW SHOULD NOT OCCUR
9599  025774  012737  000005  002414          MOV     #5,R6LOAD               ;SETUP TO EXPECT FOUT0 L AND FOUT2 L
9600                                                                          ;TO BE SET AS A RESULT OF A BORROW
9601                                                                          ;ON EVENT COUNTER 0 AND 2
9602
9603  026002  017737  154350  002420  17$:    MOV     @REG6,R6READ            ;READBACK FOUT 3:0 FLIP-FLOPS
9604  026010  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
9605  026016  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED DATA WITH ACTUAL DATA
9606  026024  001405                          BEQ     18$                     ;IF EQUAL THEN CONTINUE
9607  026026                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
9608  026026  104455                          TRAP    C$ERDF
9609  026030  000004                          .WORD   4
9610  026032  003215                          .WORD   EVNTCT
9611  026034  005026                          .WORD   EVNTER
9612  026036                                  CKLOOP
9613  026036  104406                          TRAP    C$CLP1
9614  026040  005302                  18$:    DEC     R2                      ;CHECK IF COUNTER WAS 0
9615  026042  100330                          BPL     14$                     ;IF NOT COUNT DOWN EVENT COUNTER AGAIN
9616
9617                                          ;WHEN THE FOUT FLIP-FLOP IS CLEARED BY A BORROW. THE EVENT COUNTERS
9618                                          ;ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE SIGNAL ORST L
9619                                          ;IS PULSED VIA THE PULSING OF THE SIGNAL ANST L.  THE PREVIOUS SECTION
9620                                          ;OF CODE VERIFIED THAT THIS HAPPENED.
9621
9622                                          ;THE FOLLOWING SECTION OF CODE WILL CHECK THAT THE EVENT COUNTERS CAN BE
9623                                          ;CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7 IN CONTROL REGISTER 2.
9624                                          ;THE TEST, AFTER SETTING AND CLEARING PDAL7, WILL DO ONE MORE COUNT
9625                                          ;DOWN AND CHECK THAT A BORROW WAS GENERATED FROM COUNTER 0 AND 2.
9626
9627  026044  010102                          MOV     R1,R2                   ;RESET EXPECTED CONTENTS OF EVNT CNTRS
9628
9629                                          ;RESELECT THE AND ARRAY SO THAT THE SIGNALS AND0 L AND AND2 L WILL BE
9630                                          ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST.
9631
9632  026046  012737  000200  002376          MOV     #PTER0!PDAL7,R2LOAD     ;SETUP BITS TO BE LOADED
9633  026054  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
9634  026060  001405                          BEQ     19$                     ;IF LOADED OK THEN CONTINUE
9635  026062                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9636  026062  104455                          TRAP    C$ERDF
```

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 9637  026064  000002                          .WORD   2
 9638  026066  000000                          .WORD   0
 9639  026070  004706                          .WORD   R2EROR
 9640  026072                                  CKLOOP
 9641  026072  104406                          TRAP    C$CLP1
 9642
 9643                                          ;CLEAR PDAL7 IN CONTROL REGISTER 2. THE EVENT COUNTERS SHOULD NOW
 9644                                          ;BE CLEARED. CLEARING PDAL7 WILL ALLOW THE COUNTERS TO BE COUNTED DOWN
 9645
 9646  026074  042737  000200  002376  19$:    BIC     #PDAL7,R2LOAD           ;SETUP TO CLEAR PDAL7
 9647  026102  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
 9648  026106  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
 9649  026110                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
 9650  026110  104455                          TRAP    C$ERDF
 9651  026112  000002                          .WORD   2
 9652  026114  000000                          .WORD   0
 9653  026116  004706                          .WORD   R2EROR
 9654  026120                                  CKLOOP
 9655  026120  104406                          TRAP    C$CLP1
 9656
 9657                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  CDAL6 BEING SET AND
 9658                                          ;CLEARED WILL CAUSE A PULSE ON TRANST H WHICH WILL CAUSE THE SIGNAL
 9659                                          ;ANST L TO PULSE.  THE SIGNAL ANST L BEING PULSED
 9660                                          ;WITH THE SIGNALS ANDO L AND AND2 L SET HIGH, WILL CAUSE A PULSE ON
 9661                                          ;THE SIGNALS CNDNO H  AND CNDN2 H.  THESE SIGNALS WILL COUNT DOWN
 9662                                          ;EVENT COUNTERS 0 AND 2 RESPECTIVELY.  IF PDAL7 CLEARED THE EVENT
 9663                                          ;COUNTERS THEN A BORROW WILL BE GENERATED FROM EVENT COUNTERS 0 AND 2.
 9664
 9665  026122  004737  006642          20$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
 9666
 9667                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REG 2.
 9668
 9669  026126  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER15
 9670  026132  000017                          .WORD   PTER15
 9671
 9672                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
 9673                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD
 9674                                          ;3:0 WILL BE READBACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
 9675                                          ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE ORAD 3:0 SIGNAL
 9676                                          ;LINES.  HAVING SET AND CLEARED PDAL7, TO CLEAR THE EVENT COUNTERS, AND
 9677                                          ;ISSUING A COUNT DOWN TO EVENT COUNTERS 0 AND 2, FOUT FLIP FLOPS 0 AND
 9678                                          ;2 SHOULD BE CLEARED AS A RESULT OF A BORROW AND THE COUNT DOWN PULSE.
 9679
 9680  026134  012737  000005  002414  21$:    MOV     #5,R6LOAD               ;SETUP TO EXPECT FOUTO L AND FOUT2 L
 9681                                                                          ;TO BE SET AS A RESULT OF A BORROW
 9682  026142  017737  154210  002420          MOV     @REG6,R6READ            ;READBACK FOUT 3:0 FLIP-FLOPS
 9683  026150  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
 9684  026156  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED FOUTS AGAINST ACTUAL
 9685  026164  001404                          BEQ     22$                     ;IF THE SAME THEN CONTINUE
 9686  026166                                  ERRDF   4,EVNTCL,EVNTER         ;PDAL7 FAILED TO CLEAR EVENT COUNTERS
 9687  026166  104455                          TRAP    C$ERDF
 9688  026170  000004                          .WORD   4
 9689  026172  003256                          .WORD   EVNTCL
 9690  026174  005026                          .WORD   EVNTER
 9691  026176                          22$:    ENDSEG
 9692  026176                          10001$:
```

```
 9693  026176  104405                        TRAP    C$ESEG
 9694
 9695  026200  005701                        TST     R1              ;CHECK IF FIRST DATA PATTERN
 9696  026202  001003                        BNE     23$             ;IF NOT THEN ROTATE PATTERN LEFT ONCE
 9697  026204  005201                        INC     R1              ;SET PATTERN TO A ONE
 9698  026206  000137  025454                JMP     4$              ;GO DO SEQUENCE WITH THIS PATTERN
 9699  026212  006301              23$:      ASL     R1              ;ARITHMATIC SHIFT LEFT ONCE
 9700  026214  032701  000400                BIT     #400,R1         ;CHECK IF PATTERN GREATER THEN 256
 9701  026220  001002                        BNE     24$             ;IF YES THEN CHECK IF DONE
 9702  026222  000137  025454                JMP     4$              ;GO DO TEST AGAIN WITH ROTATED PATTERN
 9703  026226  105701              24$:      TSTB    R1              ;CHECK IF PATTERN WAS FLOATTING ONE
 9704  026230  001004                        BNE     25$             ;IF NOT THEN END OF TEST
 9705  026232  012701  000125                MOV     #125,R1         ;SETUP TO DO 125 AND 252 PATTERNS
 9706  026236  000137  025454                JMP     4$              ;GO DO TEST WITH 125 FIRST
 9707
 9708  026242              25$:      ENDTST
 9709  026242              L10160:
 9710  026242  104401                        TRAP    C$ETST
 9711
```

```
                                .SBTTL  TEST 55: EVENT COUNTER 1 AND 3 TEST

                                ;++
                                ; THIS TEST WILL CHECKOUT EVENT COUNTER LOGIC FOR EVENT COUNTER 1 AND 3.  THE
                                ; TEST WILL CHECK THAT THE EVENT COUNTER REGISTERS AND EVENT COUNTERS ARE LOAD-
                                ; ED CORRECTLY BY COUNTING DOWN THE EVENT COUNTERS AND CHECKING THE FOUT FLIP-
                                ; FLOPS FOR A BORROW.  WHEN THE EVENT COUNTERS ARE COUNTED DOWN TO ZERO AND ONE
                                ; MORE COUNT DOWN IS ISSUED, A BORROW IS GENERATED WHICH WILL SET THE OUTPUT OF
                                ; THE FOUT FLIP-FLOP TO A LOW STATE.  THE TEST WILL CHECK THAT THE EVENT COUNTERS
                                ; ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN A BORROW IS GENERATED. THIS
                                ; IS DONE BY COUNTING DOWN THE EVENT COUNTERS AGAIN CHECKING FOR A BORROW FROM
                                ; THE EVENT COUNTERS.  THE TEST WILL THEN CHECK THAT THE EVENT COUNTERS CAN BE
                                ; CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7.  AFTER SETTING AND CLEARING
                                ; THE SIGNAL PDAL7, THE TEST WILL DO ONE MORE COUNT DOWN AND CHECK THAT A BORROW
                                ; IS GENERATED FROM THE EVENT COUNTERS.  THE ABOVE SEQUENCE IS REPEATED FOR EACH
                                ; OF THE FOLLOWING DATA PATTERNS: 0, 1, 2, 4, 10, 20, 40, 100, 200, 125 AND 252.
                                ;--

026244                                  BGNTST
026244                          T55::
026244  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

026250                                  BGNSEG
026250  104404                          TRAP    C$BSEG

                                ;SET CDAL4 TO A ZERO IN CONTROL REGISTER 0.  CDAL4 BEING A 0 WILL ALLOW
                                ;ONLY ONE AND/OR ARRAY TO BE SELECTED AT A TIME.  CDAL3 AND CDAL2 ON A
                                ;ZERO WILL CAUSE THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE
                                ;OUTPUTS OF THE TRACE RAM DATA IN BUFFERS.  THESE OUTPUTS ARE USED TO
                                ;ADDRESS THE AND ARRAYS.

026252  105037  002370                  CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
026256  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
026262  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
026264                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
026264  104455                          TRAP    C$ERDF
026266  000001                          .WORD   1
026270  000000                          .WORD   0
026272  004606                          .WORD   R0EROR
026274                                  CKLOOP
026274  104406                          TRAP    C$CLP1

                                ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER TRDI 15:0.  ALL ZEROES
                                ;WILL SELECT ADDRESS 0 OF THE AND ARRAY TO BE USED IN THIS TEST.

026276  005037  002414          1$:     CLR     R6LOAD                  ;SETUP TO LOAD ZEROES
026302  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
026306  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                ;SET PTER0 IN THE POINTER REGISTER VIA CONTROL REGISTER 2.  THIS WILL
                                ;SELECT THE FIRST AND ARRAY VIA THE SIGNAL PLSLO L.

026310  012737  000000  002376          MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
026316  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CEHCK REGISTER 2
026322  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
026324                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
```

```
 9768  026324  104455                          TRAP    C$ERDF
 9769  026326  000002                          .WORD   2
 9770  026330  000000                          .WORD   0
 9771  026332  004706                          .WORD   R2EROR
 9772  026334                                  CKLOOP
 9773  026334  104406                          TRAP    C$CLP1
 9774
 9775                                          ;LOAD, READ AND CHECK AND ARRAY RAM WITH DATA PATTERN OF 5.  THIS DATA
 9776                                          ;PATTERN WILL SET THE SIGNALS AND1 L AND AND3 L TO THE HIGH STATE AND
 9777                                          ;THE SIGNALS ANDO L AND AND2 L TO THE LOW STATE.  WITH AND1 L AND AND3 L
 9778                                          ;SET HIGH AND THE SIGNAL ANST L BEING PULSED, A PULSE WILL OCCUR
 9779                                          ;ON THE SIGNALS CNDN1 H AND CNDN3 H.  THESE SIGNALS WILL COUNT DOWN
 9780                                          ;EVENT COUNTERS 1 AND 3.
 9781
 9782  026336  012737  000005  002402  2$:     MOV     #5,R4LOAD               ;SETUP DATA PATTERN TO BE LOADED
 9783  026344  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
 9784  026352  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY
 9785  026356  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
 9786  026360                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
 9787  026360  104455                          TRAP    C$ERDF
 9788  026362  000003                          .WORD   3
 9789  026364  003552                          .WORD   ANDERR
 9790  026366  004722                          .WORD   R4EROR
 9791  026370                          3$:     ENDSEG
 9792  026370                          10000$:
 9793  026370  104405                          TRAP    C$ESEG
 9794
 9795  026372  005001                          CLR     R1                      ;START EVENT COUNTERS OFF AT 0
 9796
 9797  026374                          4$:     BGNSEG
 9798  026374  104404                          TRAP    C$BSEG
 9799  026376  010102                          MOV     R1,R2                   ;COPY STARTING EVENT COUNTER TO WORKING
 9800
 9801                                          ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0. CDAL7 ON A ONE WILL ALLOW
 9802                                          ;THE FOUT FLIP-FLOPS TO BE READ ON THE OR ADDRESS REGISTER LINES ORAD 3:0.
 9803
 9804  026400  052737  000200  002370          BIS     #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
 9805  026406  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHEKC REGISTER 0
 9806  026412  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
 9807  026414                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
 9808  026414  104455                          TRAP    C$ERDF
 9809  026416  000001                          .WORD   1
 9810  026420  000000                          .WORD   0
 9811  026422  004606                          .WORD   ROEROR
 9812  026424                                  CKLOOP
 9813  026424  104406                          TRAP    C$CLP1
 9814
 9815                                          ;SET AND CLEAR PDAL7 IN CONTROL REGISTER 2. PDAL7 BEING SET WILL
 9816                                          ;CLEAR ALL THE EVENT COUNTERS.
 9817
 9818  026426  052737  000200  002376  5$:     BIS     #PDAL7,R2LOAD           ;SETUP BIT TO BE LOADED
 9819  026434  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
 9820  026440  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
 9821  026442                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
 9822  026442  104455                          TRAP    C$ERDF
 9823  026444  000002                          .WORD   2
```

```
9824  026446  000000                          .WORD   0
9825  026450  004706                          .WORD   R2EROR
9826  026452                                  CKLOOP
9827  026452  104406                          TRAP    C$CLP1
9828
9829                                          ;CLEAR PDAL7 AND LOAD ALL EVENT COUNTER REGISTERS AND EVENT COUNTERS
9830                                          ;WITH THE WORKING EVENT COUNT STORED IN GENERAL CPU REGISTER R2.  THE
9831                                          ;SIGNALS ISSUED IN THE FOLLOWING LOOP ARE WPT9 H, WPTA L, WPT10 H,
9832                                          ;WPTB L, WPT11 H, WPTC L, WPT12 H, AND WPTD L.  THESE SIGNALS ARE USED
9833                                          ;TO LOAD THE DATA INTO THE EVENT COUNTER REGISTERS AND EVENT COUNTERS
9834                                          ;ON A WRITE COMMAND TO CONTROL REGISTER 6.
9835
9836  026454  012737  000011  002376  6$:     MOV     #PTER9,R2LOAD           ;SETUP BITS TO BE LOADED
9837  026462  004737  006136          7$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9838  026466  001405                          BEQ     8$                      ;IF LOADED OK THEN CONTINUE
9839  026470                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9840  026470  104455                          TRAP    C$ERDF
9841  026472  000002                          .WORD   2
9842  026474  000000                          .WORD   0
9843  026476  004706                          .WORD   R2EROR
9844  026500                                  CKLOOP
9845  026500  104406                          TRAP    C$CLP1
9846
9847  026502  010277  153650          8$:     MOV     R2,@REG6                ;LOAD EVENT COUNTERS AND REGISTERS
9848  026506  005237  002376                  INC     R2LOAD                  ;UPDATE TO NEXT POINTER
9849  026512  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL COUNTER S LOADED
9850  026520  001360                          BNE     7$                      ;IF NOT THEN LOAD NEXT COUNTER
9851
9852                                          ;RESELECT THE AND ARRAY SO THAT THE SIGNALS AND1 L AND AND3 L WILL BE
9853                                          ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST.
9854
9855  026522  012737  000000  002376  9$:     MOV     #PTER0,R2LOAD           ;SETUP TO SELECT FIRST AND ARRAY
9856  026530  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9857  026534  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
9858  026536                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9859  026536  104455                          TRAP    C$ERDF
9860  026540  000002                          .WORD   2
9861  026542  000000                          .WORD   0
9862  026544  004706                          .WORD   R2EROR
9863  026546                                  CKLOOP
9864  026546  104406                          TRAP    C$CLP1
9865
9866                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
9867                                          ;CLEARED WILL CAUSE THE SIGNAL TRANST H TO PULSE WHICH WILL CAUSE
9868                                          ;THE SIGNAL ANST L TO PULSE.  THE SIGNAL ANST L BEING PULSED
9869                                          ;WITH THE SIGNALS AND1 L AND AND3 L SET HIGH, WILL CAUSE A PULSE
9870                                          ;OF THE SIGNALS CNDN1 H AND CNDN3 H.  THESE SIGNALS WILL CAUSE EVENT
9871                                          ;COUNTER 1 AND EVENT COUNTER 3 TO COUNT DOWN BY ONE RESPECTIVELY.
9872
9873  026550  004737  006642          10$:    JSR     PC,TRANST               ;GO SET AND CLEAR CDAL6 IN CONTROL REG 0
9874
9875                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REG 2.
9876
9877  026554  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER15
9878  026560  000017                          .WORD   PTER15
9879
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```
9880                                        ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
9881                                        ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD 3:0
9882                                        ;WILL BE READ BACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
9883                                        ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON ORAD 3:0 SIGNAL LINES.
9884                                        ;THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA A BORROW FROM THE EVENT COUNTERS
9885                                        ;AND THE SIGNAL ANST L BEING PULSED.
9886
9887  026562  005037  002414          11$:  CLR     R6LOAD                  ;SETUP EXPECTED DATA
9888  026566  005702                        TST     R2                      ;CHECK IF EVENT COUNTER = 0
9889  026570  001003                        BNE     12$                     ;IF NOT THEN A BORROW SHOULD NOT OCCUR
9890  026572  012737  000012  002414        MOV     #12,R6LOAD              ;SETUP TO EXPECT A BORROW FROM COUNTER
9891                                                                        ;1 AND COUNTER 3 ON SIGNALS FOUT1 L AND
9892                                                                        ;FOUT3 L.
9893  026600  017737  153552  002420  12$:  MOV     @REG6,R6READ            ;READ FOUT 3:0 BITS ON ORAD 3:0
9894  026606  042737  177760  002420        BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
9895  026614  023737  002414  002420        CMP     R6LOAD,R6READ           ;CHECK EXPECTED RESULTS AGAINST ACTUAL
9896  026622  001405                        BEQ     13$                     ;IF EQUAL THEN CONTINUE
9897  026624                                ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
9898  026624  104455                        TRAP    C$ERDF
9899  026626  000004                        .WORD   4
9900  026630  003215                        .WORD   EVNTCT
9901  026632  005026                        .WORD   EVNTER
9902  026634                                CKLOOP
9903  026634  104406                        TRAP    C$CLP1
9904  026636  005302                  13$:  DEC     R2                      ;DECREMENT WORKING EVENT COUNTER
9905  026640  100330                        BPL     9$                      ;IF NOT DONE THEN COUNT DOWN AGAIN
9906
9907                                        ;WHEN THE FOUT FLIP-FLOP IS CLEARED BY A BORROW, THE EVENT COUNTERS
9908                                        ;ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE SIGNAL ORST L
9909                                        ;IS PULSED VIA THE PULSING OF SIGNAL ANST L.  THE FOLLOWING SECTION
9910                                        ;OF CODE WILL CHECK THAT THIS HAPPENS BY COUNTING DOWN THE EVENT
9911                                        ;COUNTERS AGAIN
9912
9913  026642  010102                        MOV     R1,R2                   ;RESET EXPECTED CONTENTS OF EVENT CNTRS
9914
9915                                        ;RESELECT THE AND ARRAY SO THAT THE SIGNALS AND1 L AND AND3 L WILL BE
9916                                        ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGIMENT OF THIS TEST
9917
9918  026644  012737  000000  002376  14$:  MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
9919  026652  004737  006136                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9920  026656  001405                        BEQ     15$                     ;IF LOADED OK THEN CONTINUE
9921  026660                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9922  026660  104455                        TRAP    C$ERDF
9923  026662  000002                        .WORD   2
9924  026664  000000                        .WORD   0
9925  026666  004706                        .WORD   R2EROR
9926  026670                                CKLOOP
9927  026670  104406                        TRAP    C$CLP1
9928
9929                                        ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
9930                                        ;CLEARED WILL CAUSE A PULSE ON TRANST H WHICH WILL CAUSE THE SIGNAL ANST L
9931                                        ;TO PULSE.  THE SIGNAL ANST L BEING PULSED WITH THE
9932                                        ;SIGNALS AND1 L AND AND3 L SET HIGH WILL CAUSE A PULSE ON THE SIGNALS
9933                                        ;CNDN1 H AND CNDN3 H.  THESE SIGNALS WILL CAUSE EVENT COUNTER 0 AND 2
9934                                        ;TO BE COUNTED DOWN BY ONE RESPECTIVELY.
9935
```

```
 9936  026672  004737  006642          15$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
 9937
 9938                                          ;ASSERT THE SIGNAL PTER15 L IN POINTER REGISTER VIA CONTROL REG 2.
 9939
 9940  026676  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER15
 9941  026702  000017                          .WORD   PTER15
 9942
 9943                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
 9944                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS,
 9945                                          ;ORAD 3:0, WILL BE READBACK. IN THIS TEST, CDAL7 IS SET TO A ONE,
 9946                                          ;WHICH WILL CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE
 9947                                          ;ORAD 3:0 SIGNAL LINES.  THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA THE
 9948                                          ;BORROW SIGNAL FROM THE EVENT COUNTERS AND THE SIGNAL ANST L BEING
 9949                                          ;PULSED.
 9950
 9951  026704  005037  002414          16$:    CLR     R6LOAD                  ;SETUP EXPECTED FOUT SIGNALS
 9952  026710  005702                          TST     R2                      ;CHECK IF EVENT COUNTER WERE ZERO
 9953  026712  001003                          BNE     17$                     ;IF NOT THEN A BORROW SHOULD NOT OCCUR
 9954  026714  012737  000012  002414          MOV     #12,R6LOAD              ;SETUP TO EXPECT FOUT1 L AND FOUT3 L
 9955                                                                          ;TO BE SET AS A RESULT OF A BORROW
 9956                                                                          ;ON EVENT COUNTER 1 AND 3
 9957
 9958  026722  017737  153430  002420  17$:    MOV     @REG6,R6READ            ;READBACK FOUT 3:0 FLIP-FLOPS
 9959  026730  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
 9960  026736  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED DATA WITH ACTUAL DATA
 9961  026744  001405                          BEQ     18$                     ;IF EQUAL THEN CONTINUE
 9962  026746                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
 9963  026746  104455                          TRAP    C$ERDF
 9964  026750  000004                          .WORD   4
 9965  026752  003215                          .WORD   EVNTCT
 9966  026754  005026                          .WORD   EVNTER
 9967  026756                                  CKLOOP
 9968  026756  104406                          TRAP    C$CLP1
 9969  026760  005302                  18$:    DEC     R2                      ;CHECK IF COUNTER WAS 0
 9970  026762  100330                          BPL     14$                     ;IF NOT COUNT DOWN EVENT COUNTER AGAIN
 9971
 9972                                          ;WHEN THE FOUT FLIP-FLOP IS CLEARED BY A BORROW. THE EVENT COUNTERS
 9973                                          ;ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE SIGNAL ORST L
 9974                                          ;IS PULSED VIA THE PULSING OF THE SIGNAL ANST L.  THE PREVIOUS SECTION
 9975                                          ;OF CODE VERIFIED THAT THIS HAPPENED.
 9976
 9977                                          ;THE FOLLOWING SECTION OF CODE WILL CHECK THAT THE EVENT COUNTERS CAN BE
 9978                                          ;CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7 IN CONTROL REGISTER 2.
 9979                                          ;THE TEST, AFTER SETTING AND CLEARING PDAL7, WILL DO ONE MORE COUNT
 9980                                          ;DOWN AND CHECK THAT A BORROW WAS GENERATED FROM COUNTER 1 AND 3.
 9981
 9982  026764  010102                          MOV     R1,R2                   ;RESET EXPECTED CONTENTS OF EVNT CNTRS
 9983
 9984                                          ;RESELECT THE AND ARRAY SO THAT THE SIGNALS AND1 L AND AND3 L WILL BE
 9985                                          ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST.
 9986
 9987  026766  012737  000200  002376          MOV     #PTER0!PDAL7,R2LOAD     ;SETUP BITS TO BE LOADED
 9988  026774  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
 9989  027000  001405                          BEQ     19$                     ;IF LOADED OK THEN CONTINUE
 9990  027002                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
 9991  027002  104455                          TRAP    C$ERDF
```

```
 9992  027004  000002                          .WORD   2
 9993  027006  000000                          .WORD   0
 9994  027010  004706                          .WORD   R2EROR
 9995  027012                                  CKLOOP
 9996  027012  104406                          TRAP    C$CLP1
 9997
 9998                                          ;CLEAR PDAL7 IN CONTROL REGISTER 2. THE EVENT COUNTERS SHOULD NOW
 9999                                          ;BE CLEARED. CLEARING PDAL7 WILL ALLOW THE COUNTERS TO BE COUNTED DOWN
10000
10001  027014  042737  000200  002376  19$:    BIC     #PDAL7,R2LOAD           ;SETUP TO CLEAR PDAL7
10002  027022  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
10003  027026  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
10004  027030                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10005  027030  104455                          TRAP    C$ERDF
10006  027032  000002                          .WORD   2
10007  027034  000000                          .WORD   0
10008  027036  004706                          .WORD   R2EROR
10009  027040                                  CKLOOP
10010  027040  104406                          TRAP    C$CLP1
10011
10012                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  CDAL6 BEING SET AND
10013                                          ;CLEARED WILL CAUSE A PULSE ON TRANST H WHICH WILL CAUSE THE SIGNAL
10014                                          ;ANST L TO BE PULSED.  THE SIGNAL ANST L BEING PULSED
10015                                          ;WITH THE SIGNALS AND1 L AND AND3 L SET HIGH, WILL CAUSE A PULSE ON
10016                                          ;THE SIGNALS CNDN1 H  AND CNDN3 H.  THESE SIGNALS WILL COUNT DOWN
10017                                          ;EVENT COUNTERS 1 AND 3 RESPECTIVELY.  IF PDAL7 CLEARED THE EVENT
10018                                          ;COUNTERS THEN A BORROW WILL BE GENERATED FROM EVENT COUNTERS 1 AND 3.
10019
10020  027042  004737  006642          20$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10021
10022                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REG 2.
10023
10024  027046  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER15
10025  027052  000017                          .WORD   PTER15
10026
10027                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
10028                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD
10029                                          ;3:0 WILL BE READBACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
10030                                          ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE ORAD 3:0 SIGNAL
10031                                          ;LINES.  HAVING SET AND CLEARED PDAL7, TO CLEAR THE EVENT COUNTERS, AND
10032                                          ;ISSUING A COUNT DOWN TO EVENT COUNTERS 1 AND 3, FOUT FLIP FLOPS 1 AND
10033                                          ;3 SHOULD BE CLEARED AS A RESULT OF A BORROW AND THE COUNT DOWN PULSE.
10034
10035  027054  012737  000012  002414  21$:    MOV     #12,R6LOAD              ;SETUP TO EXPECT FOUT1 L AND FOUT3 L
10036                                                                          ;TO BE SET AS A RESULT OF A BORROW
10037  027062  017737  153270  002420          MOV     @REG6,R6READ            ;READBACK FOUT 3:0 FLIP-FLOPS
10038  027070  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
10039  027076  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED FOUTS AGAINST ACTUAL
10040  027104  001404                          BEQ     22$                     ;IF THE SAME THEN CONTINUE
10041  027106                                  ERRDF   4,EVNTCL,EVNTER         ;PDAL7 FAILED TO CLEAR EVENT COUNTERS
10042  027106  104455                          TRAP    C$ERDF
10043  027110  000004                          .WORD   4
10044  027112  003256                          .WORD   EVNTCL
10045  027114  005026                          .WORD   EVNTER
10046  027116                          22$:    ENDSEG
10047  027116                          10001$:
```

```
 10048  027116  104405                          TRAP    C$ESEG
 10049
 10050  027120  005701                          TST     R1              ;CHECK IF FIRST DATA PATTERN
 10051  027122  001003                          BNE     23$             ;IF NOT THEN ROTATE PATTERN LEFT ONCE
 10052  027124  005201                          INC     R1              ;SET PATTERN TO A ONE
 10053  027126  000137  026374                  JMP     4$              ;GO DO SEQUENCE WITH THIS PATTERN
 10054  027132  006301                  23$:    ASL     R1              ;ARITHMATIC SHIFT LEFT ONCE
 10055  027134  032701  000400                  BIT     #400,R1         ;CHECK IF PATTERN GREATER THEN 256
 10056  027140  001002                          BNE     24$             ;IF YES THEN CHECK IF DONE
 10057  027142  000137  026374                  JMP     4$              ;GO DO TEST AGAIN WITH ROTATED PATTERN
 10058  027146  105701                  24$:    TSTB    R1              ;CHECK IF PATTERN WAS FLOATTING ONE
 10059  027150  001004                          BNE     25$             ;IF NOT THEN END OF TEST
 10060  027152  012701  000125                  MOV     #125,R1         ;SETUP TO DO 125 AND 252 PATTERNS
 10061  027156  000137  026374                  JMP     4$              ;GO DO TEST WITH 125 FIRST
 10062
 10063  027162                  25$:    ENDTST
 10064  027162                  L10161:
 10065  027162  104401                          TRAP    C$ETST
 10066
```

```
10067                                   .SBTTL  TEST 56: CHECK CDALO TO LOAD EVENT COUNTERS 3:0
10068
10069                                   ;++
10070                                   ; THIS TEST WILL CHECK THAT THE SIGNAL CDALO, WHEN SET AND CLEARED, WILL CAUSE
10071                                   ; THE EVENT COUNTERS TO BE LOADED FROM THE EVENT COUNTER REGISTER. TO DO THIS,
10072                                   ; THE TEST WILL LOAD ALL EVENT COUNTERS AND REGISTERS WITH 377 OCTAL.  THE
10073                                   ; TEST WILL THEN SET AND CLEAR THE SIGNAL PDAL7 IN CONTROL REGISTER 2. SETTING
10074                                   ; AND CLEARING THE SIGNAL PDAL7 WILL ZERO THE EVENT COUNTERS.  THE TEST WILL
10075                                   ; THEN SET AND CLEAR THE SIGNAL CDALO IN CONTROL REGISTER 0.  SETTING AND CLEAR-
10076                                   ; ING CDALO SHOULD CAUSE THE EVENT COUNTERS TO BE RELOADED FROM THE EVENT COUNTER
10077                                   ; REGISTERS.  TO TEST THAT THE EVENT COUNTERS WERE RELOADED FROM THE EVENT COUNTER
10078                                   ; REGISTERS, THE TEST WILL COUNT DOWN ALL THE EVENT COUNTERS AT THE SAME
10079                                   ; TIME CHECKING THAT NO BORROWS ARE GENERATED UNTIL THE EVENT COUNTERS HAVE BEEN
10080                                   ; COUNTED DOWN 400 OCTAL TIMES.
10081
10082  027164                                   BGNTST
10083  027164                           T56::
10084  027164  004737  005476                 JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
10085
10086  027170                                   BGNSEG
10087  027170  104404                          TRAP    C$BSEG
10088
10089                                   ;SET CDAL4 TO A ZERO IN CONTROL REGISTER 0.  CDAL4 H ON A ZERO WILL
10090                                   ;ALLOW ONLY ONE AND/OR ARRAY RAM TO BE SELECTED AT A TIME.  CDAL3 H AND
10091                                   ;CDAL2 H WILL BE SET TO ZEROES TO CAUSE THE SIGNAL TRSLO L TO BE ASSERTED
10092                                   ;WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS.  THESE
10093                                   ;OUTPUTS ARE USED TO ADDRESS THE AND ARRAYS.
10094
10095  027172  105037  002370                 CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
10096  027176  004737  006104                 JSR     PC,LDRDR0               ;LOAD, READ AND CHECK REGISTER 0
10097  027202  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
10098  027204                                   ERRDF   1,,R0EROR               ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
10099  027204  104455                          TRAP    C$ERDF
10100  027206  000001                          .WORD   1
10101  027210  000000                          .WORD   0
10102  027212  004606                          .WORD   R0EROR
10103  027214                                   CKLOOP
10104  027214  104406                          TRAP    C$CLP1
10105
10106                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER TRDI 15:0.  ALL ZEROES
10107                                   ;WILL SELECT ADDRESS 0 OF THE AND ARRAY TO BE USED IN THIS TEST.
10108
10109  027216  005037  002414         1$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
10110  027222  004537  006430                 JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
10111  027226  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
10112
10113                                   ;SET PTER0 L TO THE LOW STATE IN THE POINTER REGISTER BY LOADING THE
10114                                   ;APPROPRIATE BIT PATTERN IN CONTROL REGISTER 2.  THIS WILL SELECT THE
10115                                   ;FIRST AND ARRAY RAM VIA THE SIGNAL PSL0 L.
10116
10117  027230  012737  000000  002376         MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
10118  027236  004737  006136                 JSR     PC,LDRDR2               ;LOAD, READ AND CHECK REGISTER 2
10119  027242  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
10120  027244                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10121  027244  104455                          TRAP    C$ERDF
10122  027246  000002                          .WORD   2
```

```
10123  027250  000000                          .WORD   0
10124  027252  004706                          .WORD   R2EROR
10125  027254                                  CKLOOP
10126  027254  104406                          TRAP    C$CLP1
10127
10128                                          ;LOAD, READ AND CHECK THE FIRST AND ARRAY LOCATION WITH A DATA PATTERN
10129                                          ;OF ALL ZEROES.  THIS DATA PATTERN WILL SET THE SIGNALS AND0 L, AND1 L,
10130                                          ;AND2 L AND AND3 L TO THE HIGH STATE.  WHEN THESE SIGNALS ARE SET HIGH
10131                                          ;AND THE SIGNAL ANST L IS PULSED, PULSES WILL OCCUR ON THE SIGNALS
10132                                          ;CNDN0 H, CNDN1 H, CNDN2 H AND CNDN3 H.  THESE PULSES WILL CAUSE ALL THE
10133                                          ;EVENT COUNTERS TO BE COUNTED DOWN AT THE SAME TIME.
10134
10135  027256  005037  002402          2$:     CLR     R4LOAD                  ;SETUP DATA PATTERN TO BE ALL ZEROES
10136  027262  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
10137  027270  004737  006170                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
10138  027274  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10139  027276                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY RAM DATA ERROR.
10140  027276  104455                          TRAP    C$ERDF
10141  027300  000003                          .WORD   3
10142  027302  003552                          .WORD   ANDERR
10143  027304  004722                          .WORD   R4EROR
10144  027306                          3$:     ENDSEG
10145  027306                          10000$:
10146  027306  104405                          TRAP    C$ESEG
10147
10148  027310                                  BGNSEG
10149  027310  104404                          TRAP    C$BSEG
10150
10151  027312  012701  000377                  MOV     #377,R1                 ;SETUP EVENT COUNTERS WITH ALL ONES
10152  027316  010102                          MOV     R1,R2                   ;SETUP WORKING EVENT COUNTERS
10153
10154                                          ;SET CDAL7 H TO A ONE IN CONTROL REGISTER 0 AND ALL OTHER BITS TO A
10155                                          ;ZERO.  CDAL7 H ON A ONE WILL ALLOW THE FOUT FLIP-FLOPS TO BE READ
10156                                          ;ON THE OR ADDRESS REGISTER BITS ORAD 3:0 LATER ON IN THIS TEST.
10157
10158  027320  112737  000200  002370          MOVB    #CDAL7,R0LOAD           ;SETUP BIT TO BE LOADED
10159  027326  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10160  027332  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
10161  027334                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10162  027334  104455                          TRAP    C$ERDF
10163  027336  000001                          .WORD   1
10164  027340  000000                          .WORD   0
10165  027342  004606                          .WORD   R0EROR
10166  027344                                  CKLOOP
10167  027344  10440b                          TRAP    C$CLP1
10168
10169                                          ;THE FOLLOWING LOOP WILL LOAD ALL EVENT COUNTER REGISTERS AND EVENT
10170                                          ;COUNTERS WITH THE VALUE 377 OCTAL
10171
10172  027346  012737  000011  002376  4$:     MOV     #PTER9,R2LOAD           ;GET VALUE TO SELECT EVENT COUNTER 0
10173  027354  004737  006136          5$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 0
10174  027360  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
10175  027362                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10176  027362  104455                          TRAP    C$ERDF
10177  027364  000002                          .WORD   2
10178  027366  000000                          .WORD   0
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10179  027370  004706                          .WORD   R2EROR
10180  027372                                  CKLOOP
10181  027372  104406                          TRAP    C$CLP1
10182  027374  010177  152756          6$:     MOV     R1,@REG6                ;LOAD EVENT COUNTER REGISTER AND EVENT
10183                                                                          ;COUNTER WITH 377
10184  027400  005237  002376                  INC     R2LOAD                  ;UPDATE POINTER SELECT BY ONE
10185  027404  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL EVENT COUNTERS LOADED
10186  027412  001360                          BNE     5$                      ;IF NOT THEN LOAD NEXT EVENT COUNTER
10187
10188                                          ;CLEAR EVENT COUNTERS BY SETTING AND CLEARING PDAL7 IN CONTROL REG 2.
10189
10190  027414  052737  000200  002376          BIS     #PDAL7,R2LOAD           ;SETUP BIT TO BE LOADED
10191  027422  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10192  027426  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
10193  027430                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10194  027430  104455                          TRAP    C$ERDF
10195  027432  000002                          .WORD   2
10196  027434  000000                          .WORD   0
10197  027436  004706                          .WORD   R2EROR
10198  027440                                  CKLOOP
10199  027440  104406                          TRAP    C$CLP1
10200
10201                                          ;CLEAR PDAL7 IN CONTROL REGISTER 2
10202
10203  027442  042737  000200  002376  7$:     BIC     #PDAL7,R2LOAD           ;SETUP TO CLEAR PDAL7
10204  027450  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10205  027454  001405                          BEQ     8$                      ;IF LOADED OK THEN CONTINUE
10206  027456                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10207  027456  104455                          TRAP    C$ERDF
10208  027460  000002                          .WORD   2
10209  027462  000000                          .WORD   0
10210  027464  004706                          .WORD   R2EROR
10211  027466                                  CKLOOP
10212  027466  104406                          TRAP    C$CLP1
10213
10214                                          ;SET AND CLEAR CDAL0 IN CONTROL REGISTER 0 TO RELOAD THE EVENT COUNTERS
10215                                          ;WITH THE CONTENTS OF THE EVENT COUNTER REGISTERS.  THE EVENT COUNTER
10216                                          ;REGISTERS WERE PREVIOUSLY LOADED WITH 377 OCTAL.
10217
10218  027470  052737  000001  002370  8$:     BIS     #CDAL0,ROLOAD           ;SETUP BIT TO BE LOADED
10219  027476  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10220  027502  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
10221  027504                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10222  027504  104455                          TRAP    C$ERDF
10223  027506  000001                          .WORD   1
10224  027510  000000                          .WORD   0
10225  027512  004606                          .WORD   R0EROR
10226  027514                                  CKLOOP
10227  027514  104406                          TRAP    C$CLP1
10228
10229                                          ;SET CDAL0 H TO A ZERO IN CONTROL REGISTER 0.  CDAL7 H HAS ALREADY BEEN
10230                                          ;SET TO A ONE PREVIOUSLY IN THIS TEST TO ENABLE THE FOUT FLIP-FLOPS
10231                                          ;TO THE OR ADDRESS LINES ORAD 3:0.  CDAL4 H WAS PREVIOUSLY SET TO A ZERO
10232                                          ;TO ENABLE ONLY ONE AND/OR ARRAY RAM TO BE SELECTED AT ONE TIME.
10233
10234  027516  042737  000001  002370  9$:     BIC     #CDAL0,ROLOAD           ;SETUP BIT TO BE CLEARED
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10235  027524  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ, AND CHECK REGISTER 0
10236  027530  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
10237  027532                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10238  027532  104455                          TRAP    C$ERDF
10239  027534  000001                          .WORD   1
10240  027536  000000                          .WORD   0
10241  027540  004606                          .WORD   R0ERCR
10242  027542                                  CKLOOP
10243  027542  104406                          TRAP    C$CLP1
10244
10245                                          ;SELECT THE AND ARRAY WRITTEN PREVIOULSY BY LOADING CONTROL REGISTER
10246                                          ;2 BITS WITH DATA TO ASSERT THE SIGNAL PTER0 L IN THE POINTER REGISTER.
10247                                          ;THE AND ARRAY SELECTED WILL BE THAT ONE SELECTED BY THE SIGNAL PSL0 L.
10248                                          ;LOCATION 0 OF THE AND ARRAY WAS WRITTEN PREVIOUSLY WITH A DATA PATTERN
10249                                          ;OF ALL ZEROES, THEREFORE ALL THE OUTPUTS OF THAT RAM SHOULD BE ASSERTED
10250                                          ;HIGH THUS ASSERTING THE SIGNALS AND 3:0 L TO THE HIGH STATE.
10251
10252  027544  012737  000000  002376  10$:    MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
10253  027552  004737  006136                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK REGISTER 2
10254  027556  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10255  027560                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10256  027560  104455                          TRAP    C$ERDF
10257  027562  000002                          .WORD   2
10258  027564  000000                          .WORD   0
10259  027566  004706                          .WORD   R2EROR
10260  027570                                  CKLOOP
10261  027570  104406                          TRAP    C$CLP1
10262
10263                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
10264                                          ;CLEARED WILL CAUSE THE SIGANL TRANST H TO PULSE WHICH WILL CAUSE THE
10265                                          ;SIGNAL ANST L TO BE PULSED.  THE SIGNAL ANST L BEING PULSED
10266                                          ;WITH THE SIGNALS AND 3:0 L SET HIGH WILL CAUSE A PULSE ON THE SIGNALS
10267                                          ;CNDN0 H, CNDN1 H, CNDN2 H AND CNDN3 H.  THESE SIGNALS WILL CAUSE EVENT
10268                                          ;COUNTERS 0, 1, 2, AND 3 TO BE COUNTED DOWN RESPECTIVELY.
10269
10270  027572  004737  006642          11$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10271
10272                                          ;ASSER THE SIGNAL PTER15 L IN POINTER REGISTER VIA CONTROL REGISTER 2
10273
10274  027576  004537  006400                  JSR     R5,ASSERT               ;GO ASSERT PTER15
10275  027602  000017                          .WORD   PTER15
10276
10277                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
10278                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS
10279                                          ;ORAD 3:0 WILL BE READBACK.  IN THIS TEST, CDAL7 IS SET TO A ONE,
10280                                          ;WHICH WILL CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE ORAD
10281                                          ;3:0 SIGNAL LINES.  THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA THE BORROW
10282                                          ;SIGNAL FROM THE EVENT COUNTERS AND THE SIGNAL ANST L BEING PULSED.
10283
10284  027604  005037  002414          12$:    CLR     R6LOAD                  ;SETUP TO EXPECT NO BORROW
10285  027610  005702                          TST     R2                      ;CHECK IF EVENT COUNTER WAS 0
10286  027612  001003                          BNE     13$                     ;IF NOT THEN NO BORROW EXPECTED
10287  027614  012737  000017  002414          MOV     #17,R6LOAD              ;SETUP TO EXPECT BORROWS FROM EACH
10288                                                                          ;EVENT COUNTER
10289  027622  017737  152530  002420  13$:    MOV     @REG6,R6READ            ;READBACK FOUT 3:0 OR ORAD 3:0 LINES
10290  027630  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
```

```
10291  027636  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED AGAINST ACTUAL
10292  027644  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
10293  027646                                  ERRDF   4,EVNTRL,EVNTER         ;CDALO FAILED TO RELOAD EVENT COUNTERS
10294  027646  104455                          TRAP    C$ERDF
10295  027650  000004                          .WORD   4
10296  027652  003323                          .WORD   EVNTRL
10297  027654  005026                          .WORD   EVNTER
10298  027656                                  CKLOOP
10299  027656  104406                          TRAP    C$CLP1
10300
10301  027660  005302                  14$:    DEC     R2                      ;DECREMENT WORKING COUNTER
10302  027662  100330                          BPL     10$                     ;IF NOT MINUS THEN COUNT DOWN AGAIN
10303  027664                                  ENDSEG
10304  027664                          10001$:
10305  027664  104405                          TRAP    C$ESEG
10306
10307  027666                                  ENDTST
10308  027666                          L10162:
10309  027666  104401                          TRAP    C$ETST
10310
```

```
10311                                   .SBTTL  TEST 57: FUNCTION SELECT F/F TEST (FUSL7-FUSL3-FUSL1)
10312
10313                                   ;++
10314                                   ; THIS TEST WILL CHECK THAT FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3, AND FUSL1
10315                                   ; CAN BE SET TO A ONE AND THAT FUNCTION SELECT FLIP-FLOPS FULS2 AND FUSL0 CAN
10316                                   ; BE SET TO A ZERO.  THE FLIP-FLOPS ARE SET TO THE STATE MENTIONED VIA THE DATA
10317                                   ; FROM THE OR ARRAY RAM AND THE SIGNAL ORST L BEING PULSED.  AFTER
10318                                   ; CHECKING THAT THE FUNCTION SELECT FLIP-FLOPS ARE IN THE CORRECT STATE VIA
10319                                   ; CONTROL REGISTER 4 AND CONTROL REGISTER 6, THE TEST WILL SET THE SIGNAL PDAL5
10320                                   ; TO A ZERO IN CONTROL REGISTER 2.  PDAL5 ON A ZERO WILL PRESET THE FLIP-FLOPS
10321                                   ; TO A ZERO STATE.  THE TEST WILL THEN VERIFY THAT THE FLIP-FLOPS CLEARED BY
10322                                   ; READING CONTROL REGISTER 4 AND CONTROL REGISTER 6 AGAIN.
10323                                   ;--
10324
10325  027670                                   BGNTST
10326  027670                           T57::
10327  027670  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
10328
10329  027674                                   BGNSEG
10330  027674  104404                          TRAP    C$BSEG
10331
10332                                   ;CLEAR LOW BYTE OF CONTROL REGISTER 0.  CDAL7 CLEARED WILL ENABLE THE
10333                                   ;OUTPUTS OF THE OR ADDRESS REGISTER.  CDAL4 BEING A 0 WILL ENABLE ONLY
10334                                   ;ONE AND/OR ARRAY RAM TO BE SELECTED VIA THE POINTER REGISTER.  IN THIS
10335                                   ;TEST, PTER15 L WILL SELECT THE OR ARRAY RAM.
10336
10337  027676  105037  002370                  CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
10338  027702  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10339  027706  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
10340  027710                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
10341  027710  104455                          TRAP    C$ERDF
10342  027712  000001                          .WORD   1
10343  027714  000000                          .WORD   0
10344  027716  004606                          .WORD   ROEROR
10345  027720                                   CKLOOP
10346  027720  104406                          TRAP    C$CLP1
10347
10348                                   ;SETUP BITS IN CONTROL REGISTER 2 TO ASSERT THE SIGNAL PTER15 L IN THE
10349                                   ;POINTER REGISTER.
10350
10351  027722  004537  006400          1$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
10352  027726  000017                          .WORD   PTER15
10353
10354                                   ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH ALL ZEROES.  ON A WRITE
10355                                   ;COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A
10356                                   ;PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH WILL LOAD THE OR
10357                                   ;ADDRESS REGISTER.  ON A READ TO CONTROL REGISTER 6 WITH THE SIGNAL
10358                                   ;PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT15 H WHICH
10359                                   ;WILL READ THE DATA FROM THE OR ADDRESS REGISTER.
10360
10361  027730  005037  002414          2$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
10362  027734  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO READ LOW 4 BITS
10363  027742  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REGISTER 6
10364  027746  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10365  027750                                   ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REG NOT EQUAL ZERO
10366  027750  104455                          TRAP    C$ERDF
```

```
10367  027752  000004                          .WORD   4
10368  027754  003163                          .WORD   ORADER
10369  027756  004736                          .WORD   R026ER
10370  027760                                  CKLOOP
10371  027760  104406                          TRAP    C$CLP1
10372
10373                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
10374                                          ;REGISTER WITH A DATA PATTERN EQUAL TO 252.
10375
10376  027762  012737  000252  002402  3$:     MOV     #252,R4LOAD             ;SETUP THE DATA TO BE LOADED
10377  027770  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP MASK TO IGNORE UNWANTED BITS
10378  027776  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY DATA
10379  030002  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
10380  030004                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR
10381  030004  104455                          TRAP    C$ERDF
10382  030006  000003                          .WORD   3
10383  030010  003514                          .WORD   ORDATA
10384  030012  004722                          .WORD   R4EROR
10385  030014                                  CKLOOP
10386  030014  104406                          TRAP    C$CLP1
10387
10388                                          ;DISABLE THE PRESET SIGNAL TO THE FUNCTION SELECT FLIP-FLOPS FUSL7,
10389                                          ;FUSL3, FUSL2, FUSL1, AND FUSL0 BY SETTING THE SIGNAL PDAL5 TO A ONE.
10390
10391  030016  052737  000040  002376  4$:     BIS     #PDAL5,R2LOAD           ;SETUP BIT TO BE LOADED WITH PTER15
10392  030024  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10393  030030  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
10394  030032                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10395  030032  104455                          TRAP    C$ERDF
10396  030034  000002                          .WORD   2
10397  030036  000000                          .WORD   0
10398  030040  004706                          .WORD   R2EROR
10399  030042                                  CKLOOP
10400  030042  104406                          TRAP    C$CLP1
10401
10402                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  SETTING AND
10403                                          ;CLEARING CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE.
10404                                          ;THIS WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE THE
10405                                          ;SIGNAL ORST L TO PULSE.  THE SIGNAL ORST L BEING PULSED WILL CLOCK
10406                                          ;THE OR ARRAY RAM DATA INTO THE FUNCTION SELECT FLIP-FLOPS.  WITH
10407                                          ;A DATA PATTERN OF 252 IN THE OR ARRAY RAM, FUNCTION SELECT FLIP-FLOPS
10408                                          ;FUSL7, FUSL3 AND FUSL1 SHOULD BE SET HIGH ON THE OUTPUTS AND FUNCTION
10409                                          ;SELECT FLIP-FLOPS FUSL2 AND FUSL0 SHOULD BE SET LOW ON THE OUTPUTS
10410                                          ;WHEN THE SIGNAL ORST L IS PULSED.
10411
10412  030044  004737  006642          5$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10413
10414                                          ;CHECK THAT FUNCTION SELECT FLIP-FLOP FUSL7 IS SET TO A ONE (HIGH)
10415                                          ;BY READING THE OR ARRAY RAM DATA AND FUSL7 IN BIT 12 OF CONTROL
10416                                          ;REGISTER 4.
10417
10418  030050  042737  010000  002406  7$:     BIC     #BIT12,R4MASK           ;SETUP TO READ FULS7
10419  030056  052737  010000  002404          BIS     #BIT12,R4GOOD           ;SETUP TO EXPECT FUSL7 TO EQUAL A 1
10420  030064  004737  006220                  JSR     PC,READR4               ;READ OR ARRAY DATA AND FUSL7
10421  030070  001405                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
10422  030072                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 FLIP-FLOP PROBABLY NOT SET
```

```
10423  030072  104455                          TRAP    C$ERDF
10424  030074  000003                          .WORD   3
10425  030076  003603                          .WORD   FUSL7
10426  030100  004722                          .WORD   R4EROR
10427  030102                                  CKLOOP
10428  030102  104406                          TRAP    C$CLP1
10429
10430                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
10431                                          ;2. THE SIGNAL PDAL5 WILL REMAIN SET ALSO
10432
10433  030104  012737  000044  002376  8$:     MOV     #PDAL5!PTER4,R2LOAD     ;SETUP BITS TO BE LOADED
10434  030112  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10435  030116  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
10436  030120                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10437  030120  104455                          TRAP    C$ERDF
10438  030122  000002                          .WORD   2
10439  030124  000000                          .WORD   0
10440  030126  004706                          .WORD   R2EROR
10441  030130                                  CKLOOP
10442  030130  104406                          TRAP    C$CLP1
10443
10444                                          ;READ FUNCTION SELECT FLIP-FLOPS FUSL 3:0 VIA CONTROL REGISTER 6.
10445                                          ;FUSL3 AND FUSL1 SHOULD BE SET TO A ONE AND FUSL2 AND FUSL0 SHOULD
10446                                          ;BE SET TO A ZERO.
10447
10448  030132  012737  120000  002414  9$:     MOV     #BIT15!BIT13,R6LOAD     ;SETUP EXPECTED BITS TO BE SET
10449  030140  012737  007777  002416          MOV     #007777,R6MASK          ;SETUP TO IGNORE TRDI BITS
10450  030146  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK FUSL 3:0 FLIP-FLOPS
10451  030152  001405                          BEQ     10$                     ;IF EQUAL EXPECTED THEN CONTINUE
10452  030154                                  ERRDF   4,FUSL30,ALLREG         ;FUSL3 + FUSL1 NOT 1 OR OTHER BITS SET
10453  030154  104455                          TRAP    C$ERDF
10454  030156  000004                          .WORD   4
10455  030160  003367                          .WORD   FUSL30
10456  030162  004752                          .WORD   ALLREG
10457  030164                                  CKLOOP
10458  030164  104406                          TRAP    C$CLP1
10459
10460                                          ;CLEAR THE SIGNAL PDAL5 IN CONTROL REGISTER 2. PDAL5 ON A ZERO WILL
10461                                          ;CAUSE THE FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL 3:0 TO BE PRESET TO
10462                                          ;THE ZERO STATE.
10463
10464  030166  042737  000040  002376  10$:    BIC     #PDAL5,R2LOAD           ;CLEAR PDAL5 LEAVE PTER4 SET
10465  030174  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10466  030200  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10467  030202                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10468  030202  104455                          TRAP    C$ERDF
10469  030204  000002                          .WORD   2
10470  030206  000000                          .WORD   0
10471  030210  004706                          .WORD   R2EROR
10472  030212                                  CKLOOP
10473  030212  104406                          TRAP    C$CLP1
10474
10475                                          ;CHECK FUNCTION SELECT FLIP-FLOPS FUSL 3:0 TO BE 0.  THE FLIP-FLOPS
10476                                          ;SHOULD BE CLEARED BY THE SIGNAL PDAL5 BEING A ZERO.
10477
10478  030214  005037  002414          11$:    CLR     R6LOAD                  ;BITS 15:12 SHOULD BE A 0
```

```
10479  030220  004737  006260                  JSR     PC,READR6               ;CHECK FUSL 3:0 TO BE ZERO
10480  030224  001405                          BEQ     12$                     ;IF FUSL 3:0 EQUALS 0 THEN CONTINUE
10481  030226                                  ERRDF   4,FUSL30,ALLREG         ;FUSL 3:0 NOT 0 WHEN PDAL5 = 0
10482  030226  104455                          TRAP    C$ERDF
10483  030230  000004                          .WORD   4
10484  030232  003367                          .WORD   FUSL30
10485  030234  004752                          .WORD   ALLREG
10486  030236                                  CKLOOP
10487  030236  104406                          TRAP    C$CLP1
10488
10489                                          ;RESELECT PTER15 L IN THE POINTER REGISTER. THIS IS DONE TO RECHECK THE
10490                                          ;OR ARRAY RAM DATA AND TO CHECK THAT PDAL5 ON A 0 CLEARED FUSL7 F/F.
10491
10492  030240  004537  006400          12$:    JSR     R5,ASSERT               ;GO ASSERT PTER15
10493  030244  000017                          .WORD   PTER15
10494
10495                                          ;CHECK THAT PDAL5 CLEARED FUSL7 FLIP-FLOP AND THAT THE OR ARRAY RAM
10496                                          ;DATA REMAINED UNCHANGED
10497
10498  030246  042737  010000  002404    13$:  BIC     #BIT12,R4GOOD           ;SET EXPECTED FUSL7 BIT TO A ZERO
10499  030254  004737  006220                  JSR     PC,READR4               ;READ OR ARRAY RAM DATA AND FUSL7
10500  030260  001404                          BEQ     14$                     ;IF DATA AND FULS7 OK THEN CONTINUE
10501  030262                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 PROBABLY NOT CLERED VIA PDAL5
10502  030262  104455                          TRAP    C$ERDF
10503  030264  000003                          .WORD   3
10504  030266  003603                          .WORD   FUSL7
10505  030270  004722                          .WORD   R4EROR
10506  030272                          14$:    ENDSEG
10507  030272                          10000$:
10508  030272  104405                          TRAP    C$ESEG
10509  030274                                  ENDTST
10510  030274                          L10163:
10511  030274  104401                          TRAP    C$ETST
10512
```

```
10513                                   .SBTTL  TEST 58: FUNCTION SELECT F/F TEST (FUSL2-FUSL0)
10514
10515                                   ;++
10516                                   ; THIS TEST WILL CHECK THAT FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3, AND FUSL1
10517                                   ; CAN BE SET TO A ZERO AND THAT FUNCTION SELECT FLIP-FLOPS FUSL2 AND FUSL0 CAN
10518                                   ; BE SET TO A ONE.  THE FLIP-FLOPS ARE SET TO THE STATE MENTIONED VIA THE DATA
10519                                   ; FROM THE OR ARRAY RAM AND THE SIGNAL ORST L BEING PULSED.  AFTER
10520                                   ; CHECKING THAT THE FUNCTION SELECT FLIP-FLOPS ARE IN THE CORRECT STATE VIA
10521                                   ; CONTROL REGISTER 4 AND CONTROL REGISTER 6, THE TEST WILL SET THE SIGNAL PDAL5
10522                                   ; TO A ZERO IN CONTROL REGISTER 2.  PDAL5 ON A ZERO WILL PRESET THE FLIP-FLOPS
10523                                   ; TO A ZERO STATE.  THE TEST WILL THEN VERIFY THAT THE FLIP-FLOPS CLEARED BY
10524                                   ; READING CONTROL REGISTER 4 AND CONTROL REGISTER 6 AGAIN.
10525                                   ;--
10526
10527  030276                                   BGNTST
10528  030276                           T58::
10529  030276  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
10530
10531  030302                                   BGNSEG
10532  030302  104404                          TRAP    C$BSEG
10533
10534                                           ;CLEAR LOW BYTE OF CONTROL REGISTER 0.  CDAL7 BEING A 0 WILL ENABLE
10535                                           ;OUTPUTS OF THE OR ADDRESS REGISTER.  CDAL4 BEING A 0 WILL ENABLE ONLY
10536                                           ;ONE AND/OR ARRAY RAM TO BE SELECTED VIA THE POINTER REGISTER.  IN THIS
10537                                           ;TEST, PTER15 L WILL SELECT THE OR ARRAY RAM.
10538
10539  030304  105037  002370                  CLRB    ROLOAD                  ;SETUP BITS TO BE CLEARED
10540  030310  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10541  030314  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
10542  030316                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
10543  030316  104455                          TRAP    C$ERDF
10544  030320  000001                          .WORD   1
10545  030322  000000                          .WORD   0
10546  030324  004606                          .WORD   ROEROR
10547  030326                                   CKLOOP
10548  030326  104406                  .       TRAP    C$CLP1
10549
10550                                           ;SETUP BITS IN CONTROL REGISTER 2 TO ASSERT THE SIGNAL PTER15 L IN THE
10551                                           ;POINTER REGISTER.
10552
10553  030330  004537  006400          1$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
10554  030334  000017                          .WORD   PTER15
10555
10556                                           ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH ALL ZEROES.  ON A WRITE
10557                                           ;COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A
10558                                           ;PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH WILL LOAD THE OR
10559                                           ;ADDRESS REGISTER.  ON A READ TO CONTROL REGISTER 6 WITH THE SIGNAL
10560                                           ;PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT15 H WHICH
10561                                           ;WILL READ THE DATA FROM THE OR ADDRESS REGISTER.
10562
10563  030336  005037  002414          2$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
10564  030342  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO READ LOW 4 BITS
10565  030350  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REGISTER 6
10566  030354  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10567  030356                                   ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REG NOT EQUAL ZERO
10568  030356  104455                          TRAP    C$ERDF
```

```
10569  030360  000004                          .WORD   4
10570  030362  003163                          .WORD   ORADER
10571  030364  004736                          .WORD   R026ER
10572  030366                                  CKLOOP
10573  030366  104406                          TRAP    C$CLP1
10574
10575                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
10576                                          ;REGISTER WITH A DATA PATTERN EQUAL TO 125.
10577
10578  030370  012737  000125  002402  3$:     MOV     #125,R4LOAD             ;SETUP THE DATA TO BE LOADED
10579  030376  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP MASK TO IGNORE UNWANTED BITS
10580  030404  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY DATA
10581  030410  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
10582  030412                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR
10583  030412  104455                          TRAP    C$ERDF
10584  030414  000003                          .WORD   3
10585  030416  003514                          .WORD   ORDATA
10586  030420  004722                          .WORD   R4EROR
10587  030422                                  CKLOOP
10588  030422  104406                          TRAP    C$CLP1
10589
10590                                          ;DISABLE THE PRESET SIGNAL TO THE FUNCTION SELECT FLIP-FLOPS FUSL7,
10591                                          ;FUSL3, FUSL2, FUSL1, AND FUSL0 BY SETTING THE SIGNAL PDAL5 TO A ONE.
10592
10593  030424  052737  000040  002376  4$:     BIS     #PDAL5,R2LOAD           ;SETUP BIT TO BE LOADED WITH PTER15
10594  030432  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10595  030436  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
10596  030440                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10597  030440  104455                          TRAP    C$ERDF
10598  030442  000002                          .WORD   2
10599  030444  000000                          .WORD   0
10600  030446  004706                          .WORD   R2EROR
10601  030450                                  CKLOOP
10602  030450  104406                          TRAP    C$CLP1
10603
10604                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  SETTING AND
10605                                          ;CLEARING CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE.
10606                                          ;THIS WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE
10607                                          ;THE SIGNAL ORST L TO PULSE.  THE SIGNAL ORST L BEING PULSED WILL
10608                                          ;CLOCK THE OR ARRAY RAM DATA INTO THE FUNCTION SELECT FLIP-FLOPS.
10609                                          ;WITH A DATA PATTERN OF 125 IN THE OR ARRAY RAM, FUNCTION SELECT
10610                                          ;FLIP-FLOPS FUSL2 AND FUSL0 SHOULD BE SET HIGH ON THE OUTPUTS AND
10611                                          ;FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3 AND FUSL1 SHOULD BE SET
10612                                          ;LOW ON THE OUTPUTS WHEN THE SIGNAL ORST L IS PULSED.
10613
10614  030452  004737  006642          5$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10615
10616                                          ;CHECK THAT FUNCTION SELECT FLIP-FLOP FUSL7 IS SET TO A ZERO (LOW)
10617                                          ;BY READING THE OR ARRAY RAM DATA AND FUSL7 IN BIT 12 OF CONTROL
10618                                          ;REGISTER 4.
10619
10620  030456  042737  010000  002406  7$:     BIC     #BIT12,R4MASK           ;SETUP TO READ FULS7
10621  030464  004737  006220                  JSR     PC,READR4               ;READ OR ARRAY DATA AND FUSL7
10622  030470  001405                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
10623  030472                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 FLIP-FLOP PROBABLY NOT CLEARED
10624  030472  104455                          TRAP    C$ERDF
```

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10625  030474  000003                          .WORD   3
10626  030476  003603                          .WORD   FUSL7
10627  030500  004722                          .WORD   R4EROR
10628  030502                                  CKLOOP
10629  030502  104406                          TRAP    C$CLP1
10630
10631                                          ;ASSERT THE SIGNAL PTER4 . IN THE POINTER REGISTER VIA CONTROL REGISTER
10632                                          ;2. THE SIGNAL PDAL5 WILL REMAIN SET ALSO
10633
10634  030504  012737  000044  002376  8$:     MOV     #PDAL5!PTER4,R2LOAD     ;SETUP BITS TO BE LOADED
10635  030512  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10636  030516  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
10637  030520                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10638  030520  104455                          TRAP    C$ERDF
10639  030522  000002                          .WORD   2
10640  030524  000000                          .WORD   0
10641  030526  004706                          .WORD   R2EROR
10642  030530                                  CKLOOP
10643  030530  104406                          TRAP    C$CLP1
10644
10645                                          ;READ FUNCTION SELECT FLIP-FLOPS FUSL 3:0 VIA CONTROL REGISTER 6.
10646                                          ;FUSL2 AND FUSL0 SHOULD BE SET TO A ONE AND FUSL3 AND FUSL1 SHOULD
10647                                          ;BE SET TO A ZERO.
10648
10649  030532  012737  050000  002414  9$:     MOV     #BIT14!BIT12,R6LOAD     ;SETUP EXPECTED BITS TO BE SET
10650  030540  012737  007777  002416          MOV     #007777,R6MASK          ;SETUP TO IGNORE TRDI BITS
10651  030546  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK FUSL 3:0 FLIP-FLOPS
10652  030552  001405                          BEQ     10$                     ;IF EQUAL EXPECTED THEN CONTINUE
10653  030554                                  ERRDF   4,FUSL30,ALLREG         ;FUSL2 + FUSL0 NOT 1 OR OTHER BITS SET
10654  030554  104455                          TRAP    C$ERDF
10655  030556  000004                          .WORD   4
10656  030560  003367                          .WORD   FUSL30
10657  030562  004752                          .WORD   ALLREG
10658  030564                                  CKLOOP
10659  030564  104406                          TRAP    C$CLP1
10660
10661                                          ;CLEAR THE SIGNAL PDAL5 IN CONTROL REGISTER 2. PDAL5 ON A ZERO WILL
10662                                          ;CAUSE THE FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL 3:0 TO BE PRESET TO
10663                                          ;THE ZERO STATE.
10664
10665  030566  042737  000040  002376  10$:    BIC     #PDAL5,R2LOAD           ;CLEAR PDAL5 LEAVE PTER4 SET
10666  030574  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10667  030600  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10668  030602                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10669  030602  104455                          TRAP    C$ERDF
10670  030604  000002                          .WORD   2
10671  030606  000000                          .WORD   0
10672  030610  004706                          .WORD   R2EROR
10673  030612                                  CKLOOP
10674  030612  104406                          TRAP    C$CLP1
10675
10676                                          ;CHECK FUNCTION SELECT FLIP-FLOPS FUSL 3:0 TO BE 0.  THE FLIP-FLOPS
10677                                          ;SHOULD BE CLEARED BY THE SIGNAL PDAL5 BEING A ZERO.
10678
10679  030614  005037  002414          11$:    CLR     R6LOAD                  ;BITS 15:12 SHOULD BE A 0
10680  030620  004737  006260                  JSR     PC,READR6               ;CHECK FUSL 3:0 TO BE ZERO
```

```
10681  030624  001405                        BEQ     12$                     ;IF FUSL 3:0 EQUALS 0 THEN CONTINUE
10682  030626                                ERRDF   4,FUSL30,ALLREG         ;FUSL 3:0 NOT 0 WHEN PDAL5 = 0
10683  030626  104455                        TRAP    C$ERDF
10684  030630  000004                        .WORD   4
10685  030632  003367                        .WORD   FUSL30
10686  030634  004752                        .WORD   ALLREG
10687  030636                                CKLOOP
10688  030636  104406                        TRAP    C$CLP1
10689
10690                                        ;RESELECT PTER15 L IN THE POINTER REGISTER. THIS IS DONE TO RECHECK THE
10691                                        ;OR ARRAY RAM DATA AND TO CHECK THAT PDAL5 ON A 0 CLEARED FUSL7 F/F.
10692
10693  030640  004537  006400        12$:    JSR     R5,ASSERT               ;GO ASSERT PTER15
10694  030644  000017                        .WORD   PTER15
10695
10696                                        ;CHECK THAT FUSL7 FLIP-FLOP IS STILL CLEARED AND THAT THE OR ARRAY RAM
10697                                        ;DATA REMAINED UNCHANGED
10698
10699  030646  004737  006220        13$:    JSR     PC,READR4               ;READ OR ARRAY RAM DATA AND FUSL7
10700  030652  001404                        BEQ     14$                     ;IF DATA AND FULS7 OK THEN CONTINUE
10701  030654                                ERRDF   3,FUSL7,R4EROR          ;FUSL7 PROBABLY NOT CLERED VIA PDAL5
10702  030654  104455                        TRAP    C$ERDF
10703  030656  000003                        .WORD   3
10704  030660  003603                        .WORD   FUSL7
10705  030662  004722                        .WORD   R4EROR
10706  030664                        14$:    ENDSEG
10707  030664                        10000$:
10708  030664  104405                        TRAP    C$ESEG
10709  030666                                ENDTST
10710  030666                        L10164:
10711  030666  104401                        TRAP    C$ETST
10712
```

```
                                .SBTTL  TEST 59: CHECK FUSL7 F/F TO LOAD EVENT COUNTERS

                                ;++
                                ; THIS TEST WILL CHECK THAT THE EVENT COUNTERS WILL GET RELOADED FROM THE EVENT
                                ; COUNTER REGISTERS WHEN THE OUTPUT OF FUNCTION SELECT FLIP-FLOP FUSL7 H IS SET
                                ; TO THE HIGH STATE.  TO CHECK THAT THIS HAPPENS, THE TEST WILL LOAD ALL EVENT
                                ; COUNTER REGISTERS AND EVENT COUNTERS WITH THE VALUE 377 OCTAL.  THE TEST WILL
                                ; COUNT DOWN THE EVENT COUNTERS UNTIL THE EVENT COUNTERS EQUAL 200 OCTAL.  THE
                                ; TEST CHECKS THAT NO BORROWS ARE GENERATED FROM THE EVENT COUNTERS WHEN THE
                                ; EVENT COUNTERS ARE COUNTED DOWN.  THIS IS DONE BY CHECKING THE FOUT 3:0 FLIP-
                                ; FLOPS ON THE ORAD 3:0 SIGNAL LINES.  THE TEST WILL THEN LOAD LOCATION ZERO OF
                                ; THE ''OR ARRAY RAM'' WITH DATA EQUAL TO 200 OCTAL WHICH WILL CAUSE THE SIGNAL
                                ; ''ORO 7 L'' TO BE ASSERTED LOW.  THE TEST WILL THEN SET AND CLEAR THE SIGNAL
                                ; CDAL6 WHICH WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED.
                                ; THIS WILL CAUSE THE SIGNAL ANST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL
                                ; ORST L TO BE PULSED.  THE SIGNAL ORST L BEING PULSED WILL CAUSE THE OR
                                ; ARRAY DATA TO BE LOADED INTO FUNCTION SELECT FLIP-FLOPS, THUS SETTING THE
                                ; OUTPUT OF FUSL7 H FLIP-FLOP TO THE HIGH STATE.  WHEN FUSL7 H FLIP-FLOP IS
                                ; SET HIGH, A ONE SHOT WILL BE FIRED WHICH WILL CAUSE THE EVENT COUNTERS TO
                                ; BE LOADED FROM THE EVENT COUNTER REGISTERS.  TO TEST THAT THE EVENT COUNTERS
                                ; WERE RELOADED FROM THE EVENT COUNTER REGISTERS, THE TEST WILL COUNT DOWN THE
                                ; EVENT COUNTERS 400 OCTAL TIMES CHECKING THAT NO BORROWS ARE GENERATED FROM
                                ; THE EVENT COUNTERS UNTIL THE 400TH COUNT DOWN IS ISSUED.
                                ;--

030670                                  BGNTST
030670                          T59::
030670  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

030674                                  BGNSEG
030674  104404                          TRAP    C$BSEG
030676  012701  000377                  MOV     #377,R1                 ;SETUP STARTING EVENT COUNTER
030702  010102                          MOV     R1,R2                   ;COPY STARTING COUNT TO WORKING COUNT

                                ;CLEAR CDAL4 IN CONTROL REGISTER 0 TO SELECT ONLY ONE AND/OR ARRAY RAM

030704  105037  002370                  CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
030710  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
030714  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
030716                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
030716  104455                          TRAP    C$ERDF
030720  000001                          .WORD   1
030722  000000                          .WORD   0
030724  004606                          .WORD   ROEROR
030726                                  CKLOOP
030726  104406                          TRAP    C$CLP1

                                ;;THE FOLLOWING LOOP WILL LOAD ALL EVENT COUNTER REGISTERS AND EVENT
                                ;COUNTERS WITH THE VALUE 377 OCATAL.

030730  012737  000011  002376  1$:     MOV     #PTER9,R2LOAD           ;SETUP POINTER TO FIRST EVENT COUNTER
030736  004737  006136          2$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
030742  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
030744                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
030744  104455                          TRAP    C$ERDF
030746  000002                          .WORD   2
```

```
10769  030750  000000                          .WORD   0
10770  030752  004706                          .WORD   R2EROR
10771  030754                                  CKLOOP
10772  030754  104406                          TRAP    C$CLP1
10773  030756  010277  151374          3$:     MOV     R2,@REG6                ;LOAD EVENT COUNTERS AND REGISTERS
10774  030762  005237  002376                  INC     R2LOAD                  ;UPDATE VAULE FOR POINTER REGISTER
10775  030766  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL COUNTERS LOADED
10776  030774  001360                          BNE     2$                      ;IF NOT THEN LOAD NEXT VALUE
10777
10778                                          ;SET CDAL7 H TO A ONE AND CDAL4 H TO A ZERO IN CONTROL REGISTER 0.
10779                                          ;CDAL7 H ON A ONE WILL ENABLE THE FOUT FLIP-FLOPS TO BE READBACK ON THE
10780                                          ;ORAD 3:0 SIGNAL LINES.  CDAL4 H ON A ZERO WILL ENABLE ONLY ONE AND/OR
10781                                          ;ARRAY RAM TO BE SELECTED AT ONE TIME.
10782
10783  030776  112737  000200  002370  4$:     MOVB    #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
10784  031004  004737  006104                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
10785  031010  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
10786  031012                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
10787  031012  104455                          TRAP    C$ERDF
10788  031014  000001                          .WORD   1
10789  031016  000000                          .WORD   0
10790  031020  004606                          .WORD   ROEROR
10791  031022                                  CKLOOP
10792  031022  104406                          TRAP    C$CLP1
10793
10794                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER BY LOADING THE
10795                                          ;APPROPRIATE BITS IN CONTROL REGISTER 2.  WHEN PTER15 L IS ASSERTED LOW,
10796                                          ;THE OR ADDRESS LINES, ORAD 3:0, WILL BE READBACK ON A READ COMMAND TO
10797                                          ;CONTROL REGISTER 6.  IN THIS PORTION OF THE TEST, THE FOUT FLIP-FLOPS
10798                                          ;ARE ENABLED TO THE OR ADDRESS LINES VIA CDAL7 H.  WHEN PTER15 L IS
10799                                          ;ASSERTED LOW, ALL THE AND ARRAY RAMS ARE DESELECTED.  WHEN ALL THE
10800                                          ;AND ARRAY RAMS ARE DESELECTED, THE AND ARRAY SIGNALS "AND 3:0 L" WILL
10801                                          ;BE ASSERTED HIGH, THUS ALLOWING ALL THE EVENT COUNTERS TO BE COUNTED
10802                                          ;DOWN WHEN THE SIGNAL ANST L IS PULSED.
10803
10804  031024  004537  006400          5$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
10805  031030  000017                          .WORD   PTER15
10806
10807                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
10808                                          ;CLEARED WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED.
10809                                          ;THIS WILL CAUSE THE SIGNAL ANST L TO BE PULSED.  THE SIGNAL ANST L
10810                                          ;BEING PULSED WITH THE SIGNALS AND 3:0 L SET HIGH WILL CAUSE A PULSE
10811                                          ;ON THE SIGNALS CNDN0 H, CNDN1 H, CNDN2 H AND CNDN3 H.  THESE SIGNALS
10812                                          ;WILL CAUSE ALL THE EVENT COUNTERS TO COUNTED DOWN BY 1.
10813
10814  031032  004737  006642          6$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10815
10816                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
10817                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD
10818                                          ;3:0 WILL BE READBACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
10819                                          ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE ORAD 3:0 SIGNAL
10820                                          ;LINES.  THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA THE BORROW SIGNAL FROM
10821                                          ;THE EVENT COUNTERS AND THE SIGNAL ANST L BEING PULSED.
10822
10823  031036  005037  002414                  CLR     R6LOAD                  ;SETUP TO EXPECT NO BORROW FROM EVENT
10824                                                                          ;COUNTERS. THE EVENT COUNTERS WILL BE
```

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10825
10826  031042  012737  177760  002416          MOV     #177760,R6MASK          ;COUNTED DOWN FROM 377 TO 200.
10827  031050  004737  006260                  JSR     PC,READR6               ;SETUP TO IGNORE UNWANTED BITS
10828  031054  001405                          BEQ     7$                      ;GO READ AND CHECK FOUT 3:0 F/F'S
10829  031056                                  ERRDF   4,EVNTCT,EVNTER         ;IF NO BORROW THEN CONTINUE
10830  031056  104455                          TRAP    C$ERDF                  ;BORROW OCCURED WHEN NOT EXPECTED
10831  031060  000004                          .WORD   4
10832  031062  003215                          .WORD   EVNTCT
10833  031064  005026                          .WORD   EVNTER
10834  031066                                  CKLOOP
10835  031066  104406                          TRAP    C$CLP1
10836  031070  005302                  7$:     DEC     R2                      ;DECREMENT SIMULATED EVENT COUNTER
10837  031072  022702  000200                  CMP     #200,R2                 ;CHECK IF HALF WAY YET
10838  031076  001355                          BNE     6$                      ;IF NOT THEN COUNT DOWN AGAIN
10839
10840  031100  010102                          MOV     R1,R2                   ;COPY STARTING EVENT COUNT TO WORKING
10841                                                                          ;EVENT COUNTER.
10842
10843                                          ;CLEAR THE SIGNAL CDAL7 IN CONTROL REGISTER 0 TO ENABLE THE OUTPUTS
10844                                          ;OF THE OR ADDRESS REGISTER INSTEAD OF THE FOUT FLIP-FLOPS.
10845
10846  031102  042737  000200  002370          BIC     #CDAL7,R0LOAD           ;SETUP BIT TO BE CLEARED
10847  031110  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10848  031114  001405                          BEQ     8$                      ;IF LOADED CK THEN CONTINUE
10849  031116                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10850  031116  104455                          TRAP    C$ERDF
10851  031120  000001                          .WORD   1
10852  031122  000000                          .WORD   0
10853  031124  004606                          .WORD   R0EROR
10854  031126                                  CKLOOP
10855  031126  104406                          TRAP    C$CLP1
10856
10857                                          ;LOAD, READ AND CHECK THE OR ADDRESS REGISTER WITH ADDRESS OF ZERO.
10858
10859  031130  004737  006252          8$:     JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
10860  031134  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
10861  031136                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL TO ZERO
10862  031136  104455                          TRAP    C$ERDF
10863  031140  000004                          .WORD   4
10864  031142  003163                          .WORD   ORADER
10865  031144  004736                          .WORD   R026ER
10866  031146                                  CKLOOP
10867  031146  104406                          TRAP    C$CLP1
10868
10869                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
10870                                          ;REGISTER WITH A DATA PATTERN OF 200. THIS DATA PATTERN WILL SET THE
10871                                          ;FUNCTION SELECT FLIP-FLOP FUSL7 TO THE HIGH STATE WHEN THE SIGNAL
10872                                          ;ORST L IS PULSED.
10873
10874  031150  012737  000200  002402  9$:     MOV     #BIT7,R4LOAD            ;SETUP DATA TO BE LOADED
10875  031156  012737  167400  002406          MOV     #167400,R4MASK          ;SETUP TO CHECK FUSL7 AND OR ARRAY DATA
10876  031164  004737  006204                  JSR     PC,LDRDR4               ;LOAD,READ + CHECK OR ARRAY RAM + FUSL7
10877  031170  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
10878  031172                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 OR OR ARRAY DATA ERROR
10879  031172  104455                          TRAP    C$ERDF
10880  031174  000003                          .WORD   3
```

```
10881  031176  003603                          .WORD   FUSL7
10882  031200  004722                          .WORD   R4EROR
10883  031202                                  CKLOOP
10884  031202  104406                          TRAP    C$CLP1
10885
10886                                          ;SET PDAL5 TO A ONE SO THAT THE FUNCTION SELECT FLIP-FLOPS CAN BE SET
10887                                          ;WITH THE OR ARRAY RAM DATA WHEN THE SIGNAL ORST L IS PULSED.
10888
10889  031204  052737  000040  002376  10$:    BIS     #PDAL5,R2LOAD           ;SET PDAL5 AND BITS FOR PTER15
10890  031212  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10891  031216  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10892  031220                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10893  031220  104455                          TRAP    C$ERDF
10894  031222  000002                          .WORD   2
10895  031224  000000                          .WORD   0
10896  031226  004706                          .WORD   R2EROR
10897  031230                                  CKLOOP
10898  031230  104406                          TRAP    C$CLP1
10899
10900                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  SETTING AND
10901                                          ;CLEARING CDAL6 WILL CAUSE ALL THE EVENT COUNTERS TO BE COUNTED DOWN
10902                                          ;BY ONE WHEN THE SIGNAL ANST L IS PULSED.  WHEN THE SIGNAL ORST L IS
10903                                          ;PULSED, THE FUNCTION SELECT FLIP-FLOPS WILL BE LOADED WITH
10904                                          ;THE DATA FROM THE OR ARRAY RAM, WHICH IN THIS TEST WILL CAUSE FUSL7
10905                                          ;FLIP-FLOP TO BE SET TO THE HIGH STATE.  WHEN FUSL7 FLIP-FLOP IS SET,
10906                                          ;A ONE SHOT WILL BE FIRED WHICH WILL CAUSE THE EVENT COUNTERS TO BE
10907                                          ;RELOADED FROM THE EVENT COUNTER REGISTERS.
10908
10909  031232  004737  006642          11$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10910
10911                                          ;CHECK OR ARRAY RAM DATA AGAIN AND CHECK THAT FUNCTION SELECT FLIP-
10912                                          ;FLOP FUSL7 IS SET TO A ONE.
10913
10914  031236  052737  010000  002404          BIS     #BIT12,R4GOOD           ;SETUP TO EXPECT FUSL7 FLIP-FLOP SET
10915  031244  004737  006220                  JSR     PC,READR4               ;READ AND CHECK FUSL7 + OR ARRAY RAM
10916  031250  001405                          BEQ     12$                     ;IF DATA EQUAL EXPECTED THEN CONTINUE
10917  031252                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 F/F - OR ARRAY RAM DATA ERROR
10918  031252  104455                          TRAP    C$ERDF
10919  031254  000003                          .WORD   3
10920  031256  003603                          .WORD   FUSL7
10921  031260  004722                          .WORD   R4EROR
10922  031262                                  CKLOOP
10923  031262  104406                          TRAP    C$CLP1
10924
10925                                          ;SET PDAL5 TO A 0 IN CONTROL REGISTER 0 TO CLEAR FUSL7 FLIP-FLOP. THE
10926                                          ;EVENT COUNTERS SHOULD HAVE BEEN LOADED WHEN FUSL7 FLIP-FLOP SET.
10927
10928  031264  042737  000040  002376  12$:    BIC     #PDAL5,R2LOAD           ;LEAVE BITS FOR PTER15 IN REG 2
10929  031272  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10930  031276  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
10931  031300                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10932  031300  104455                          TRAP    C$ERDF
10933  031302  000002                          .WORD   2
10934  031304  000000                          .WORD   0
10935  031306  004706                          .WORD   R2EROR
10936  031310                                  CKLOOP
```

```
10937  031310  104406                          TRAP    C$CLP1
10938
10939                                          ;CHECK OR ARRAY RAM AGAIN TO CHECK THAT FUNCTION SELECT FLIP-FLOP FUSL7
10940                                          ;FLIP-FLOP CLEARED.
10941
10942  031312  042737  010000  002404  13$:    BIC     #BIT12,R4GOOD           ;SETUP TO CHECK FUSL7 TO BE 0
10943  031320  004737  006220                  JSR     PC,READR4               ;READ AND CHECK FUSL7 + OR ARRAY DATA
10944  031324  001405                          BEQ     14$                     ;IF FUSL7 EQUALS 0 THEN CONTINUE
10945  031326                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 F/F OR OR ARRAY DATA EROR
10946  031326  104455                          TRAP    C$ERDF
10947  031330  000003                          .WORD   3
10948  031332  003603                          .WORD   FUSL7
10949  031334  004722                          .WORD   R4EROR
10950  031336                                  CKLOOP
10951  031336  104406                          TRAP    C$CLP1
10952
10953                                          ;THE FOLLOWING SECTION OF CODE WILL COUNT DOWN THE EVENT COUNTERS
10954                                          ;TO CHECK THAT THE EVENT COUNTERS WERE RELOADED WHEN FUNCTION SELECT
10955                                          ;FLIP-FLOP FUSL7 WAS SET.  THE EVENT COUNTERS BEFORE THE RELOAD
10956                                          ;CONTAINED 200 OCTAL AND THE EVENT COUNTER REGISTERS CONTAINED 377.
10957
10958                                          ;SET CDAL7 H TO A ONE AND CDAL4 H TO A ZERO IN CONTROL REGISTER 0.
10959                                          ;CDAL7 H ON A ONE WILL ENABLE THE FOUT FLIP-FLOPS TO BE READBACK ON THE
10960                                          ;ORAD 3:0 SIGNAL LINES.  CDAL4 H ON A ZERO WILL ENABLE ONLY ONE AND/OR
10961                                          ;ARRAY RAM TO BE SELECTED AT ONE TIME.
10962
10963  031340  112737  000200  002370  14$:    MOVB    #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
10964  031346  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10965  031352  001405                          BEQ     15$                     ;IF LOADED OK THEN CONTINUE
10966  031354                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
10967  031354  104455                          TRAP    C$ERDF
10968  031356  000001                          .WORD   1
10969  031360  000000                          .WORD   0
10970  031362  004606                          .WORD   ROEROR
10971  031364                                  CKLOOP
10972  031364  104406                          TRAP    C$CLP1
10973
10974                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER BY LOADING THE
10975                                          ;APPROPRIATE BITS IN CONTROL REGISTER 2.  WHEN PTER15 L IS ASSERTED LOW,
10976                                          ;THE OR ADDRESS LINES, ORAD 3:0, WILL BE READBACK ON A READ COMMAND TO
10977                                          ;CONTROL REGISTER 6.  IN THIS PORTION OF THE TEST, THE FOUT FLIP-FLOPS
10978                                          ;ARE ENABLED TO THE OR ADDRESS LINES VIA CDAL7 H.  WHEN PTER15 L IS
10979                                          ;ASSERTED LOW, ALL THE AND ARRAY RAMS ARE DESELECTED.  WHEN ALL THE
10980                                          ;AND ARRAY RAMS ARE DESELECTED, THE AND ARRAY SIGNALS "AND 3:0 L" WILL
10981                                          ;BE ASSERTED HIGH, THUS ALLOWING ALL THE EVENT COUNTERS TO BE COUNTED
10982                                          ;DOWN WHEN THE SIGNAL ANST L IS PULSED.
10983
10984  031366  004537  006400          15$:    JSR     R5,ASSERT               ;GO ASSERT PTER15
10985  031372  000017                          .WORD   PTER15
10986
10987                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
10988                                          ;CLEARED WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED.  THIS
10989                                          ;WILL CAUSE THE SIGNAL ANST L TO BE PULSED.  THE SIGNAL ANST L BEING
10990                                          ;PULSED WITH THE SIGNALS AND 3:0 L SET HIGH WILL CAUSE A PULSE ON THE
10991                                          ;SIGNALS CNDN0 H, CNDN1 H, CNDN2 H AND CNDN3 H WHICH WILL CAUSE THE
10992                                          ;EVENT COUNTERS TO BE COUNTED DOWN BY ONE.
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10993
10994  031374  004737  006642          16$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10995
10996                                           ;WHEN A READ IS ISSUED TO CONTROL REGISTER 6 WITH THE SIGNAL CDAL7
10997                                           ;ON A ONE, THE FOUT FLIP-FLOPS 3:0 OR READBACK ON THE OR ADDRESS REG-
10998                                           ;ISTER SIGNAL LINES ORAD 3:0.  THE FOUT FLIP-FLOPS ARE SET/CLEARED
10999                                           ;VIA A BORROW FROM THE EVENT COUNTERS AND THE SIGNAL ANST L BEING PULSED
11000
11001  031400  005037  002414                  CLR     R6LOAD                  ;SETUP TO EXPECT NO BORROW
11002  031404  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11003  031412  005702                          TST     R2                      ;CHECK IF COUNTER WAS 0 BEFORE CNT DWN
11004  031414  001003                          BNE     17$                     ;IF NOT THEN DON'T EXPECT BORROWS
11005  031416  012737  000017  002414          MOV     #17,R6LOAD              ;EXPECT A BORROW FROM EACH COUNTER
11006  031424  004737  006260          17$:    JSR     PC,READR6               ;GO READ AND CHECK FOUT 3:0 F/F'S
11007  031430  001405                          BEQ     18$                     ;IF FOUT F/F'S EQUAL EXPECTED - CONT
11008  031432                                  ERRDF   4,EVNTCT,EVNTER         ;FUSL7 FAILED TO RELOAD EVENT COUNTERS
11009  031432  104455                          TRAP    C$ERDF
11010  031434  000004                          .WORD   4
11011  031436  003215                          .WORD   EVNTCT
11012  031440  005026                          .WORD   EVNTER
11013  031442                                  CKLOOP
11014  031442  104406                          TRAP    C$CLP1
11015  031444  005302          18$:    DEC     R2                      ;DECREMENT SIMULATED EVENT COUNTER
11016  031446  100352                          BPL     16$                     ;IF NOT MINUS THEN COUNT DOWN AGAIN
11017  031450                                  ENDSEG
11018  031450                          10000$:
11019  031450  104405                          TRAP    C$ESEG
11020
11021  031452                                  ENDTST
11022  031452                          L10165:
11023  031452  104401                          TRAP    CSETST
11024
```

```
                                        .SBTTL  TEST 60: TRACING F/F TEST VIA FUSL0 AND FULS1 F/F'S

                                        ;++
                                        ; THIS TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET BY FUNCTION SELECT
                                        ; FUSL0 H FLIP-FLOP AND CLEARED BY FUNCTION SELECT FUSL1 H FLIP-FLOP.  THE TEST
                                        ; WILL CHECK THAT THE TRACING FLIP-FLOP IS SET AND CLEARED BY CHECKING THE TRACE
                                        ; RAM ADDRESS REGISTER.  THE TRACE RAM ADDRESS REGISTER IS NOT INCREMENTED WHEN
                                        ; THE TRACING F/F IS CLEARED AND THE SIGNALS TRANST H AND TRST L ARE PULSED.
                                        ; THE TRACE RAM ADDRESS REGISTER IS INCREMENTED WHEN THE TRACING FLIP-FLOP IS
                                        ; SET AND THE SIGNALS TRANST H AND TRST L ARE PULSED.  THE FUNCTION SELECT
                                        ; FLIP-FLOPS ARE SET AND CLEARED VIA THE OR ARRAY RAM DATA AND THE SIGNAL
                                        ; ORST L BEING PULSED.
                                        ;--

031454                                          BGNTST
031454                                  T60::
031454  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

031460                                          BGNSEG
031460  104404                                  TRAP    C$BSEG

                                        ;SET AND CLEAR CDAL0 IN CONTROL REGISTER 0 TO CLEAR TRACE RAM ADDRESS
                                        ;REGISTER AND THE TRACING FLIP-FLOP.  CDAL4 WILL BE SET TO A ZERO TO
                                        ;ENABLE ONLY ONE AND/OR ARRAY RAM AT A TIME VIA THE POINTER REGISTER
                                        ;PTER SIGNALS.

031462  112737  000001  002370              MOVB    #CDAL0,ROLOAD           ;SETUP BITS TO BE LOADED
031470  004737  006104                      JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
031474  001405                              BEQ     1$                      ;IF LOADED OK THEN GO CLEAR CDAL0
031476                                      ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
031476  104455                              TRAP    C$ERDF
031500  000001                              .WORD   1
031502  000000                              .WORD   0
031504  004606                              .WORD   R0EROR
031506                                      CKLOOP
031506  104406                              TRAP    C$CLP1
031510  042737  000001  002370  1$:         BIC     #CDAL0,ROLOAD           ;SETUP BIT TO BE CLEARED
031516  004737  006104                      JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
031522  001405                              BEQ     2$                      ;IF LOADED OK THEN CONTINUE
031524                                      ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
031524  104455                              TRAP    C$ERDF
031526  000001                              .WORD   1
031530  000000                              .WORD   0
031532  004606                              .WORD   R0EROR
031534                                      CKLOOP
031534  104406                              TRAP    C$CLP1

                                        ;CLEAR PDAL5 IN CONTROL REGISTER 0 TO PRESET THE OUTPUTS OF THE
                                        ;FUNCTION SELECT FLIP-FLOPS TO THE LOW STATE.

031536  012737  000000  002376  2$:         MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
031544  004737  006136                      JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
031550  001405                              BEQ     3$                      ;IF LOADED OK THEN CONTINUE
031552                                      ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
031552  104455                              TRAP    C$ERDF
```

```
11081  031554  000002                          .WORD   2
11082  031556  000000                          .WORD   0
11083  031560  004706                          .WORD   R2EROR
11084  031562                                  CKLOOP
11085  031562  104406                          TRAP    C$CLP1
11086
11087                                          ;LOAD PDAL5 INTO CONTROL REGISTER 2 ALONG WITH THE BITS TO SELECT THE
11088                                          ;SIGNAL PTER0 L IN THE POINTER REGISTER.
11089
11090  031564  012737  000040  002376  3$:     MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11091  031572  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11092  031576  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
11093  031600                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11094  031600  104455                          TRAP    C$ERDF
11095  031602  000002                          .WORD   2
11096  031604  000000                          .WORD   0
11097  031606  004706                          .WORD   R2EROR
11098  031610                                  CKLOOP
11099  031610  104406                          TRAP    C$CLP1
11100
11101                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0 TO CHECK THAT THE TRACING
11102                                          ;FLIP-FLOP AND THE FUNCTION SELECT FLIP-FLOP FUSL0 ARE CLEARED.  THE
11103                                          ;FUNCTION SELECT FLIP-FLOPS SHOULD BE LOADED TO THE ZERO STATE WHEN THE
11104                                          ;OR ARRAY RAMS ARE DESELECTED AND THE SIGNAL ORST L IS PULSED.
11105                                          ;SETTING AND CLEARING CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L
11106                                          ;TO BE PULSED WHICH WILL CAUSE THE SIGNAL ANST L TO BE PULSED WHICH
11107                                          ;WILL CAUSE THE SIGNAL ORST L TO BE PULSED.  NO PULSE SHOULD OCCUR ON
11108                                          ;THE SIGNAL CTR L, THEREFORE THE TRACE RAM ADDRESS REGISTER SHOULD NOT
11109                                          ;BE INCREMENTED.
11110
11111  031612  004737  006642          4$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11112
11113                                          ;CHECK TRACE RAM ADDRESS REGISTER TO EQUAL ZERO AS A RESULT OF THE
11114                                          ;SIGNAL CDAL0 BEING SET AND CLEARED.  IF AN ERROR OCCURS CHECK THAT
11115                                          ;THE TRACING FLIP-FLOP AND FUNCTION SELECT FLIP-FLOP FUSL0 ARE IN THE
11116                                          ;LOW LEVEL STATE.
11117
11118  031616  005037  002414                  CLR     R6LOAD                  ;SETUP TO CHECK FOR ADDRESS ZERO
11119  031622  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11120  031630  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK RAM ADDRESS REGISTER
11121  031634  001405                          BEQ     5$                      ;IF EQUAL TO ZERO THEN CONTINUE
11122  031636                                  ERRDF   4,TRADER,R026ER         ;CDAL0 FAILED TO CLEAR TRAM ADDRESS REG.
11123  031636  104455                          TRAP    C$ERDF
11124  031640  000004                          .WORD   4
11125  031642  002464                          .WORD   TRADER
11126  031644  004736                          .WORD   R026ER
11127  031646                                  CKLOOP
11128  031646  104406                          TRAP    C$CLP1
11129
11130                                          ;SET AND CLEAR CDAL6 IN CONTROL REIGSTER 0 TO CHECK THAT FUNCTION
11131                                          ;SELECT FLIP-FLOP, FUSL0 H, DID NOT GET SET WHEN THE SIGNAL ORST L
11132                                          ;WAS PULSED IN THE PREVIOUS SECTION.
11133
11134  031650  004737  006642          5$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11135
11136                                          ;CHECK TRACE RAM ADDRESS REGISTER TO EQUAL A ZERO AS A RESULT OF THE
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11137                                          ;SIGNAL CDALO BEING SET AND CLEARED.  IF AN ERROR OCCURS, CHECK THAT
11138                                          ;THE TRACING FLIP-FLOP OUTPUT IS LOW AND THE FUNCTION SELECT FLIP-FLOP,
11139                                          ;FUSLO H, IS IN THE LOW STATE.
11140
11141  031654  005037  002414                 CLR     R6LOAD                  ;SETUP TO CHECK FOR ADDRESS ZERO
11142  031660  012737  174000  002416         MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11143  031666  004737  006260                 JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
11144  031672  001405                         BEQ     6$                      ;IF EQUAL TO ZERO THEN CONTINUE
11145  031674                                 ERRDF   4,TRADER,R026ER         ;TRACING F/F OR FUSLO H F/F SET
11146  031674  104455                         TRAP    C$ERDF
11147  031676  000004                         .WORD   4
11148  031700  002464                         .WORD   TRADER
11149  031702  004736                         .WORD   R026ER
11150  031704                                 CKLOOP
11151  031704  104406                         TRAP    C$CLP1
11152
11153                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REGISTER
11154                                          ;2. PDAL5 WILL ALSO BE SET TO A ONE TO ALLOW THE FUNCTION SELECT FLIP-
11155                                          ;FLOPS TO BE CLOCKED WHEN THE SIGNAL ORST L IS PULSED.  PTER15 L
11156                                          ;WILL ALLOW THE OR ADDRESS REGISTER AND OR ARRAY RAMS TO BE WRITTEN AND
11157                                          ;READ.
11158
11159  031706  012737  000057  002376  6$:    MOV     #PDAL5!PTER15,R2LOAD    ;SETUP BITS TO BE LOADED
11160  031714  004737  006136                 JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REIGSTER 2
11161  031720  001405                         BEQ     7$                      ;IF LOADED OK THEN CONTINUE
11162  031722                                 ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11163  031722  104455                         TRAP    C$ERDF
11164  031724  000002                         .WORD   2
11165  031726  000000                         .WORD   0
11166  031730  004706                         .WORD   R2EROR
11167  031732                                 CKLOOP
11168  031732  104406                         TRAP    C$CLP1
11169
11170                                          ;SELECT ADDRESS 0 IN THE OR ARRAY RAM ADDRESS REGISTER.  CDAL7 ON A
11171                                          ;ZERO IN CONTROL REGISTER 0 WILL ALLOW THE OR ADDRESS REGISTER TO BE
11172                                          ;READBACK ON A READ COMMAND TO CONTROL REGISTER 6.
11173
11174  031734  005037  002414          7$:    CLR     R6LOAD                  ;SETUP TO LOAD ADDRESS 0
11175  031740  012737  177760  002416         MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11176  031746  004737  006252                 JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11177  031752  001405                         BEQ     8$                      ;IF ADDRESS EQUALS 0 THEN CONTINUE
11178  031754                                 ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER ERROR - ORAD 3:0
11179  031754  104455                         TRAP    C$ERDF
11180  031756  000004                         .WORD   4
11181  031760  003163                         .WORD   ORADER
11182  031762  004736                         .WORD   R026ER
11183  031764                                 CKLOOP
11184  031764  104406                         TRAP    C$CLP1
11185
11186                                          ;LOAD, READ AND CHECK ADDRESS 0 OF THE OR ARRAY RAM WITH A DATA PATTERN
11187                                          ;EQUAL TO ONE.  THIS WILL CAUSE THE SIGNAL "ORO 0 L" TO BE ASSERTED LOW.
11188                                          ;ALL OTHER OR ARRAY RAM DATA BITS WILL BE ASSERTED HIGH.
11189
11190  031766  012737  000001  002402  8$:    MOV     #1,R4LOAD               ;SETUP DATA PATTERN TO BE LOADED
11191  031774  012737  177400  002406         MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
11192  032002  004737  006204                 JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY DATA
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11193  032006  001405                          BEQ     9$                      ;IF DATA EQUALS 1 THEN CONTINUE
11194  032010                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
11195  032010  104455                          TRAP    C$ERDF
11196  032012  000003                          .WORD   3
11197  032014  003514                          .WORD   ORDATA
11198  032016  004722                          .WORD   R4EROR
11199  032020                                  CKLOOP
11200  032020  104406                          TRAP    C$CLP1
11201
11202                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REIGSTER 0.  THIS WILL CAUSE
11203                                          ;THE SIGNALS TRANST H AND TRST L TO BE PULSED WHICH WILL CAUSE THE
11204                                          ;SIGNAL ANST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE
11205                                          ;PULSED.  WHEN THE SIGNAL ORST L IS PULSED, FUSLO H FLIP-FLOP SHOULD
11206                                          ;BE CLOCKED TO THE HIGH STATE.  NO PULSE SHOULD OCCUR ON THE CTR L
11207                                          ;SIGNAL BECAUSE THE PREVIOUS STATE OF FUSLO H FLIP-FLOP WAS LOW WHEN
11208                                          ;THE SIGNALS TRANST H AND TRST L WERE PULSED.  THE SIGNALS TRANST H
11209                                          ;AND TRST L WILL CLOCK THE PREVIOUS STATE OF FUSLO H FLIP-FLOP.
11210
11211  032022  004737  006642          9$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11212
11213                                          ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11214                                          ;SIGNAL PTER0 L IN THE POINTER REGISTER.  THIS IS DONE TO SETUP FOR
11215                                          ;A READ OF THE TRACE RAM ADDRESS REGISTER.
11216
11217  032026  012737  000040  002376  11$:     MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11218  032034  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11219  032040  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
11220  032042                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11221  032042  104455                          TRAP    C$ERDF
11222  032044  000002                          .WORD   2
11223  032046  000000                          .WORD   0
11224  032050  004706                          .WORD   R2EROR
11225  032052                                  CKLOOP
11226  032052  104406                          TRAP    C$CLP1
11227
11228                                          ;READ TRACE RAM ADDRESS REGISTER TO CHECK THAT IS WAS NOT INCREMENTED
11229                                          ;BY ONE VIA THE SIGNAL "CTR L" WHEN THE PREVIOUS STATE OF FUSLO H FLIP-
11230                                          ;FLOP WAS LOW AND THE SIGNALS TRANST H AND TRST L WERE PULSED.
11231
11232  032054  005037  002414          12$:    CLR     R6LOAD                  ;SETUP TO EXPECT ADDRESS 0
11233  032060  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11234  032066  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
11235  032072  001405                          BEQ     13$                     ;IF ADDRESS EQUALS 0 THEN CONTINUE
11236  032074                                  ERRDF   4,TRADER,R026ER         ;CTR L WAS PROBABLY ISSUED
11237  032074  104455                          TRAP    C$ERDF
11238  032076  000004                          .WORD   4
11239  032100  002464                          .WORD   TRADER
11240  032102  004736                          .WORD   R026ER
11241  032104                                  CKLOOP
11242  032104  104406                          TRAP    C$CLP1
11243
11244                                          ;SET PDAL5 IN CONTROL REGISTER 2 ALONG WITH THE BITS TO ASSERT THE
11245                                          ;SIGNAL PTER15 L IN THE POINTER REGISTER.
11246
11247  032106  012737  000057  002376  13$:     MOV     #PDAL5!PTER15,R2LOAD    ;SETUP BITS TO BE LOADED
11248  032114  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
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11249  032120  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
11250  032122                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11251  032122  104455                          TRAP    C$ERDF
11252  032124  000002                          .WORD   2
11253  032126  000000                          .WORD   0
11254  032130  004706                          .WORD   R2EROR
11255  032132                                  CKLOOP
11256  032132  104406                          TRAP    C$CLP1
11257
11258                                          ;RELOAD ADDRESS ZERO INTO THE OR ADDRESS REGISTER.
11259
11260  032134  005037  002414          14$:    CLR     R6LOAD                  ;SETUP TO LOAD ADDRESS ZERO
11261  032140  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11262  032146  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11263  032152  001405                          BEQ     15$                     ;IF ADDRESS EQUALS 0 THEN CONTINUE
11264  032154                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG ERROR - ORAD 3:0
11265  032154  104455                          TRAP    C$ERDF
11266  032156  000004                          .WORD   4
11267  032160  003163                          .WORD   ORADER
11268  032162  004736                          .WORD   R026ER
11269  032164                                  CKLOOP
11270  032164  104406                          TRAP    C$CLP1
11271
11272                                          ;LOAD DATA PATTERN EQUAL TO ZERO INTO ADDRESS ZERO OF THE OR ARRAY
11273                                          ;RAM.  THIS WILL CAUSE ALL THE OR ARRAY RAM DATA BIT SIGNALS, ORO 7:0
11274                                          ;TO BE ASSERTED HIGH.
11275
11276  032166  005037  002402          15$:    CLR     R4LOAD                  ;SETUP DATA PATTERN EQUAL TO ZERO
11277  032172  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
11278  032200  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
11279  032204  001405                          BEQ     16$                     ;IF DATA EQUALS 0 THEN CONTINUE
11280  032206                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
11281  032206  104455                          TRAP    C$ERDF
11282  032210  000003                          .WORD   3
11283  032212  003514                          .WORD   ORDATA
11284  032214  004722                          .WORD   R4EROR
11285  032216                                  CKLOOP
11286  032216  104406                          TRAP    C$CLP1
11287
11288                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  THIS WILL CAUSE
11289                                          ;THE SIGNALS TRANST H AND TRST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL
11290                                          ;ANST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE PULSED.
11291                                          ;WHEN THE SIGNAL ORST L IS PULSED, ALL FUNCTION SELECT FLIP-FLOPS
11292                                          ;SHOULD BE CLOCKED TO THE LOW STATE AS A RESULT OF OR ARRAY RAM DATA
11293                                          ;ORO 7:0 BEING ASSERTED HIGH (0).  A PULSE SHOULD BE ISSUED ON THE
11294                                          ;SIGNAL CTR L AS A RESULT OF THE PREVIOUS STATE OF FUSL0 FLIP-FLOP
11295                                          ;(1) AND THE SIGNALS TRANST H AND TRST L BEING PULSED.  THE TRACING
11296                                          ;FLIP-FLOP WILL ALSO BE SET TO A ONE AS A RESULT OF THE SIGNAL CTR L
11297                                          ;AND THE PREVIOUS STATE OF FUSL0 H FLIP-FLOP (1).
11298
11299  032220  004737  006642          16$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11300
11301                                          ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11302                                          ;SIGNAL PTERO L IN THE POINTER REGISTER.  THIS IS DONE TO SETUP FOR A
11303                                          ;READ OF THE TRACE RAM ADDRESS REGISTER.
11304
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11305  032224  012737  000040  002376  18$:    MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11306  032232  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11307  032236  001405                           BEQ     19$                     ;IF LOADED OK THEN CONTINUE
11308  032240                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11309  032240  104455                           TRAP    C$ERDF
11310  032242  000002                           .WORD   2
11311  032244  000000                           .WORD   0
11312  032246  004706                           .WORD   R2EROR
11313  032250                                   CKLOOP
11314  032250  104406                           TRAP    C$CLP1
11315
11316                                           ;READ TRACE RAM ADDRESS REGISTER TO CHECK THAT IT WAS INCREMENTED BY
11317                                           ;ONE VIA THE SIGNAL "CTR L".  THE SIGNAL "CTR L" SHOULD BE GENERATED
11318                                           ;BY THE SIGNALS TRANST H AND TRST L BEING PULSED AND THE PREVIOUS STATE
11319                                           ;OF FUSL0 H FLIP-FLOP (1).
11320
11321  032252  012737  000001  002414  19$:    MOV     #1,R6LOAD               ;SETUP EXPECTED ADDRESS TO EQUAL 1
11322  032260  012737  174000  002416           MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11323  032266  004737  006260                   JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
11324  032272  001405                           BEQ     20$                     ;IF ADDRESS EQUALS ONE THEN CONTINUE
11325  032274                                   ERRDF   4,TRADER,R026ER         ;CTR L PROBABLY FAILED TO PULSE
11326  032274  104455                           TRAP    C$ERDF
11327  032276  000004                           .WORD   4
11328  032300  002464                           .WORD   TRADER
11329  032302  004736                           .WORD   R026ER
11330  032304                                   CKLOOP
11331  032304  104406                           TRAP    C$CLP1
11332
11333                                           ;SET PDAL5 IN CONTROL REGISTER 2 ALONG WITH THE BITS TO ASSERT THE
11334                                           ;SIGNAL PTER15 L IN THE POINTER REGISTER
11335
11336  032306  012737  000057  002376  20$:    MOV     #PDAL5!PTER15,R2LOAD    ;SETUP BITS TO BE LAODED
11337  032314  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11338  032320  001405                           BEQ     21$                     ;IF LOADED OK THEN CONTINUE
11339  032322                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11340  032322  104455                           TRAP    C$ERDF
11341  032324  000002                           .WORD   2
11342  032326  000000                           .WORD   0
11343  032330  004706                           .WORD   R2EROR
11344  032332                                   CKLOOP
11345  032332  104406                           TRAP    C$CLP1
11346
11347                                           ;RELOAD ADDRESS 0 INTO THE OR ADDRESS REGISTER
11348
11349  032334  005037  002414          21$:    CLR     R6LOAD                  ;SETUP TO LOAD ADDRESS ZERO
11350  032340  012737  177760  002416           MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11351  032346  004737  006252                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11352  032352  001405                           BEQ     22$                     ;IF ADDRESS EQUALS 0 THEN CONTINUE
11353  032354                                   ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER NOT EQUAL TO 0
11354  032354  104455                           TRAP    C$ERDF
11355  032356  000004                           .WORD   4
11356  032360  003163                           .WORD   ORADER
11357  032362  004736                           .WORD   R026ER
11358  032364                                   CKLOOP
11359  032364  104406                           TRAP    C$CLP1
11360
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11361                                          ;LOAD DATA PATTERN EQUAL TO TWO INTO ADDRESS ZERO OF THE OR ARRAY RAM.
11362                                          ;THIS WILL CAUSE THE OR ARRAY RAM DATA BIT 'DRO1 L" TO BE ASSERTED LOW
11363                                          ;WITH ALL THE OTHER DATA BITS ASSERTED HIGH.
11364
11365  032366  012737  000002  002402  22$:    MOV     #2,R4LOAD               ;SETUP TO LOAD OR ARRAY RAM WITH 2
11366  032374  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
11367  032402  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
11368  032406  001405                          BEQ     23$                     ;IF DATA EQUALS 2 THEN CONTINUE
11369  032410                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR
11370  032410  104455                          TRAP    C$ERDF
11371  032412  000003                          .WORD   3
11372  032414  003514                          .WORD   ORDATA
11373  032416  004722                          .WORD   R4EROR
11374  032420                                  CKLOOP
11375  032420  104406                          TRAP    C$CLP1
11376
11377                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  THIS WILL CAUSE THE SIGNALS
11378                                          ;TRANST H AND TRST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL ANST L
11379                                          ;TO BE PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE PULSED.  A
11380                                          ;PULSE WILL BE ISSUED ON THE SIGNAL CTR L AS A RESULT OF THE TRACING
11381                                          ;FLIP-FLOP BEING SET FROM THE PREVIOUS CTR L PULSE.  WHEN THE SIGNAL
11382                                          ;ORST L IS PULSED, THE OR ARRAY RAM DATA WILL BE LOADED INTO FUNCTION
11383                                          ;SELECT FLIP-FLOPS, THUS SETTING FUSL1 H FLIP-FLOP TO THE HIGH STATE
11384                                          ;AND THE OTHER FUNCTION SELECT FLIP-FLOPS TO THE LOW STATE.  FUNCTION
11385                                          ;SELECT FLIP-FLOP, FUSL1 H, BEING SET HIGH WILL CLEAR THE TRACING
11386                                          ;FLIP-FLOP, THUS INHIBITING ANY FURTHER PULSES ON THE SIGNAL CTR L
11387                                          ;WHEN THE SIGNALS TRANST H AND TRST L ARE PULSED.
11388
11389  032422  004737  006642          23$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11390
11391                                          ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11392                                          ;SIGNAL PTER0 L IN THE POINTER REGISTER.  THIS IS DONE TO SETUP FOR
11393                                          ;A READ OF THE TRACE RAM ADDRESS REGISTER.
11394
11395  032426  012737  000040  002376  25$:    MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11396  032434  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11397  032440  001405                          BEQ     26$                     ;IF LOADED OK THEN CONTINUE
11398  032442                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11399  032442  104455                          TRAP    C$ERDF
11400  032444  000002                          .WORD   2
11401  032446  000000                          .WORD   0
11402  032450  004706                          .WORD   R2EROR
11403  032452                                  CKLOOP
11404  032452  104406                          TRAP    C$CLP1
11405
11406                                          ;READ TRACE RAM ADDRESS REGISTER TO CHECK THAT IT WAS INCREMENTED BY
11407                                          ;ONE VIA THE SIGNAL "CTR L".  THE SIGNAL "CTR L" SHOULD BE GENERATED
11408                                          ;BY THE SIGNALS TRANST H AND TRST L BEING PULSED AND THE OUTPUT OF THE
11409                                          ;TRACING FLIP-FLOP BEING SET HIGH AT THE TIME THE SIGNALS TRANST H AND
11410                                          ;TRST L WERE PULSED.
11411
11412  032454  012737  000002  002414  26$:    MOV     #2,R6LOAD               ;SETUP EXPECTED ADDRESS TO BE 2
11413  032462  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11414  032470  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
11415  032474  001405                          BEQ     27$                     ;IF ADDRESS EQUALS 2 THEN CONTINUE
11416  032476                                  ERRDF   4,TRADER,R026ER         ;TRACING F/F PROBABLY FAILED TO SET
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11417  032476  104455                          TRAP    C$ERDF
11418  032500  000004                          .WORD   4
11419  032502  002464                          .WORD   TRADER
11420  032504  004736                          .WORD   R026ER
11421  032506                                  CKLOOP
11422  032506  104406                          TRAP    C$CLP1
11423
11424                                          ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11425                                          ;SIGNAL PTER15 L IN THE POINTER REGISTER.
11426
11427  032510  012737  000057  002376  27$:    MOV     #PDAL5!PTER15,R2LOAD    ;SETUP BITS TO BE LOADED
11428  032516  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
11429  032522  001405                          BEQ     28$                     ;IF LOADED OK THEN CONTINUE
11430  032524                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11431  032524  104455                          TRAP    C$ERDF
11432  032526  000002                          .WORD   2
11433  032530  000000                          .WORD   0
11434  032532  004706                          .WORD   R2EROR
11435  032534                                  CKLOOP
11436  032534  104406                          TRAP    C$CLP1
11437
11438                                          ;RELOAD ADDRESS 0 INTO THE OR ADDRESS REGISTER
11439
11440  032536  005037  002414          28$:    CLR     R6LOAD                  ;SETUP TO LOAD ADDRESS 0
11441  032542  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11442  032550  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11443  032554  001405                          BEQ     29$                     ;IF LOADED OK THEN CONTINUE
11444  032556                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL TO 0
11445  032556  104455                          TRAP    C$ERDF
11446  032560  000004                          .WORD   4
11447  032562  003163                          .WORD   ORADER
11448  032564  004736                          .WORD   R026ER
11449  032566                                  CKLOOP
11450  032566  104406                          TRAP    C$CLP1
11451
11452                                          ;LOAD DATA PATTERN EQUAL TO ZERO INTO ADDRESS ZERO OF THE OR ARRAY RAM.
11453                                          ;THIS WILL CAUSE THE OR ARRAY RAM DATA BITS "ORO 7:0" TO BE ASSERTED
11454                                          ;HIGH
11455
11456  032570  005037  002402          29$:    CLR     R4LOAD                  ;SETUP DATA PATTERN OF 0
11457  032574  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP MASK WORD
11458  032602  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRY RAM
11459  032606  001405                          BEQ     30$                     ;IF LOADED OK THEN CONTINUE
11460  032610                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
11461  032610  104455                          TRAP    C$ERDF
11462  032612  000003                          .WORD   3
11463  032614  003514                          .WORD   ORDATA
11464  032616  004722                          .WORD   R4EROR
11465  032620                                  CKLOOP
11466  032620  104406                          TRAP    C$CLP1
11467
11468                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  THIS WILL CAUSE THE SIGNALS
11469                                          ;TRANST H AND TRST L TO PULSED WHICH WILL CAUSE THE SIGNAL ANST L TO BE
11470                                          ;PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE PULSED.  WHEN THE
11471                                          ;SIGNAL ORST L IS PULSED, THE OR ARRAY RAM DATA WILL BE LOADED INTO
11472                                          ;THE FUNCTION SELECT FLIP-FLOPS, THUS SETTING ALL THE OUTPUTS OF THE
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11473                                           ;FLIP-FLOPS TO THE LOW STATE.  THE PREVIOUS CLOCKING OF CDAL6 HAD SET
11474                                           ;FUNCTION SELECT FLIP-FLOP, FUSL1 H, TO THE HIGH STATE, THUS CLEARING
11475                                           ;THE TRACING FLIP-FLOP.  THEREFORE, WHEN CDAL6 IS PULSED THIS TIME TO
11476                                           ;PULSE THE SIGNALS TRANST H AND TRST L, NO PULSE SHOULD BE ISSUED ON THE
11477                                           ;CTR L SIGNAL.  THE TRACE RAM ADDRESS REGISTER WILL NOT BE INCREMENTED.
11478
11479  032622  004737  006642          30$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11480
11481                                           ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11482                                           ;SIGNAL PTER0 L IN THE POINTER REGISTER.  THIS IS DONE TO SETUP FOR
11483                                           ;A READ OF THE TRACE RAM ADDRESS REGISTER.
11484
11485  032626  012737  000040  002376           MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11486  032634  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
11487  032640  001405                           BEQ     31$                     ;IF LOADED OK THEN CONTINUE
11488  032642                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11489  032642  104455                           TRAP    C$ERDF
11490  032644  000002                           .WORD   2
11491  032646  000000                           .WORD   0
11492  032650  004706                           .WORD   R2EROR
11493  032652                                   CKLOOP
11494  032652  104406                           TRAP    C$CLP1
11495
11496                                           ;READ TRACE RAM ADDRESS REGISTER AGAIN TO CHECK THAT THE "TRACING" FLIP-
11497                                           ;FLOP WAS CLEARED WHEN FUNCTION SELECT FLIP-FLOP, FUSL1 H, WAS SET
11498                                           ;HIGH IN THE PREVIOUS SECTION.  WHEN THE TRACING FLIP-FLOP IS CLEARED,
11499                                           ;NO PULSE SHOULD BE ISSUED ON THE SIGNAL CTR L WHEN THE SIGNALS TRANST H
11500                                           ;AND TRST L ARE PULSED.
11501
11502  032654  012737  000002  002414   31$:    MOV     #2,R6LOAD               ;SETUP EXPECTED ADDRESS TO EQUAL 2
11503  032662  012737  174000  002416           MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11504  032670  004737  006260                   JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
11505  032674  001404                           BEQ     32$                     ;IF ADDRESS = 2 THEN CONTINUE
11506  032676                                   ERRDF   4,TRADER,R026ER         ;TRACING F/F FAILED TO CLEAR VIA FUSL1
11507  032676  104455                           TRAP    C$ERDF
11508  032700  000004                           .WORD   4
11509  032702  002464                           .WORD   TRADER
11510  032704  004736                           .WORD   R026ER
11511  032706                           32$:    ENDSEG
11512  032706                           10000$:
11513  032706  104405                           TRAP    C$ESEG
11514  032710                                   ENDTST
11515  032710                           L10166:
11516  032710  104401                           TRAP    C$ETST
11517
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11518                                   .SBTTL  TEST 61: SBL58 AND SBL56 FLIP-FLOP TEST
11519
11520                                   ;++
11521                                   ; THIS TEST WILL CHECK THAT SBL56 AND SBL58 FLIP-FLOPS CAN BE SET AND CLEARED.
11522                                   ; SBL57 AND SBL59 ARE CHECKED TO REMAIN CLEARED DURING THIS TEST.  SBL 59:56
11523                                   ; FLIP-FLOPS ARE CHECKED BY THE PROGRAM ON THE TRACE RAM DATA IN BUS WHEN THE
11524                                   ; SIGNAL "TRSL2 L" IS ASSERTED LOW. SBL 59:56 FLIP-FLOPS WILL BE READBACK ON
11525                                   ; TRDI 59:56 SIGNAL LINES.  SBL56 FLIP-FLOP IS SET VIA A BORROW FROM EVENT
11526                                   ; COUNTER 0 AND EVENT COUNTER 0 COUNT DOWN PULSE.  SBL56 FLIP-FLOP IS CLEARED
11527                                   ; BY RELOADING EVENT COUNTER 0.  SBL58 FLIP-FLOP IS SET BY "OR ARRAY RAM" DATA
11528                                   ; BIT OR04 L BEING SET LOW AND THE SIGNAL ORST L BEING PULSED.  SBL58
11529                                   ; FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 2.
11530                                   ;--
11531
11532  032712                                   BGNTST
11533  032712                           T61::
11534  032712  004737  005476                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
11535  032716                                   BGNSEG
11536  032716  104404                           TRAP    C$BSEG
11537
11538                                           ;CLEAR CDAL4 IN CONTROL REGISTER 0. CDAL4 ON A 0 WILL ALLOW ONLY ONE
11539                                           ;AND/OR ARRAY RAM TO BE SELECTED AT A TIME.
11540
11541  032720  105037  002370                   CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
11542  032724  004737  006104                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11543  032730  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
11544  032732                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
11545  032732  104455                           TRAP    C$ERDF
11546  032734  000001                           .WORD   1
11547  032736  000000                           .WORD   0
11548  032740  004606                           .WORD   ROEROR
11549  032742                                   CKLOOP
11550  032742  104406                           TRAP    C$CLP1
11551
11552                                           ;THE FOLLOWING LOOP WILL LOAD ZEROES INTO EACH OF THE EVENT COUNTER
11553                                           ;REGISTERS AND EVENT COUNTERS.  BY LOADING EACH EVENT COUNTER, THE
11554                                           ;SBL FLIP-FLOPS 59:56 WILL BE CLEARED BY SIGNALS W9 L, W10 L, W11 L,AND W12 L.
11555
11556  032744  012737  000011  002376  1$:      MOV     #PTER9,R2LOAD           ;SETUP TO START LOADING AT COUNTER 0
11557  032752  004737  006136          2$:      JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11558  032756  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
11559  032760                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11560  032760  104455                           TRAP    C$ERDF
11561  032762  000002                           .WORD   2
11562  032764  000000                           .WORD   0
11563  032766  004706                           .WORD   R2EROR
11564  032770                                   CKLOOP
11565  032770  104406                           TRAP    C$CLP1
11566  032772  012777  000000  147356  3$:      MOV     #0,@REG6                ;LOAD ALL ZEROES INTO EVENT COUNTERS
11567  033000  005237  002376                   INC     R2LOAD                  ;UPDATE THE POINTER TO NEXT COUNTER
11568  033004  022737  000015  002376           CMP     #PTER13,R2LOAD          ;CHECK IF ALL EVENT COUNTERS LOADED
11569  033012  001357                           BNE     2$                      ;IF NOT THEN LOAD THE NEXT EVENT COUNTER
11570
11571                                           ;SET CDAL3 TO A ONE AND CDAL2 TO A 0 IN CONTROL REGISTER 0 TO SET THE
11572                                           ;SIGNAL TRSL2 L. THE SIGNAL TRSL2 L WILL ALLOW SBL BITS 59:56 TO BE
11573                                           ;READBACK ON TRDI BITS 59:56.
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11574
11575  033014  052737  000010  002370          BIS     #CDAL3,ROLOAD           ;SETUP BITS TO BE LOADED
11576  033022  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11577  033026  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
11578  033030                                   ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED.
11579  033030  104455                          TRAP    C$ERDF
11580  033032  000001                          .WORD   1
11581  033034  000000                          .WORD   0
11582  033036  004706                          .WORD   R0EROR
11583  033040                                   CKLOOP
11584  033040  104406                          TRAP    C$CLP1
11585
11586                                           ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
11587                                           ;2.  THIS IS DONE TO SETUP FOR A READBACK OF TRDI BITS 59:48.
11588
11589  033042  012737  000004  002376  4$:     MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
11590  033050  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11591  033054  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
11592  033056                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11593  033056  104455                          TRAP    C$ERDF
11594  033060  000002                          .WORD   2
11595  033062  000000                          .WORD   0
11596  033064  004706                          .WORD   R2EROR
11597  033066                                   CKLOOP
11598  033066  104406                          TRAP    C$CLP1
11599
11600                                           ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59:56 ARE CLEARED.
11601                                           ;SBL BITS 59:56 ARE READBACK ON TRDI BITS 59:56 WHEN THE SIGNAL TRSL2 L
11602                                           ;IS ASSERTED.  THE SBL FLIP-FLOPS SHOULD HAVE BEEN CLEARED WHEN THE
11603                                           ;EVENT COUNTERS WERE LOADED.
11604
11605  033070  005037  002414          5$:     CLR     R6LOAD                  ;SETUP EXPECTED DATA
11606  033074  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY TRDI 59:56 BITS
11607  033102  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK SBL 59:56 BITS
11608  033106  001405                          BEQ     6$                      ;IF ALL FLIP-FLOPS CLEARED THEN CONT
11609  033110                                   ERRDF   4,SBLERR,R026ER         ;WRITING EVNT CNTR'S FAILED TO 0 SBL F/F'S 59:56
11610  033110  104455                          TRAP    C$ERDF
11611  033112  000004                          .WORD   4
11612  033114  003420                          .WORD   SBLERR
11613  033116  004736                          .WORD   R026ER
11614  033120                                   CKLOOP
11615  033120  104406                          TRAP    C$CLP1
11616
11617                                           ;CLEAR CDAL3 IN CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
11618                                           ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
11619
11620  033122  042737  000010  002370  6$:     BIC     #CDAL3,ROLOAD           ;SETUP BIT TO BE CLEARED
11621  033130  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11622  033134  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
11623  033136                                   ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
11624  033136  104455                          TRAP    C$ERDF
11625  033140  000001                          .WORD   1
11626  033142  000000                          .WORD   0
11627  033144  004606                          .WORD   R0EROR
11628  033146                                   CKLOOP
11629  033146  104406                          TRAP    C$CLP1
```

```
11630
11631                                   ;THE FOLLOWING SECTION OF CODE WILL LOAD ALL ZEROES INTO ALL THE TRACE
11632                                   ;RAM DATA IN BUFFERS. THIS WILL SELECT ADDRESS ZERO OF ALL THE AND ARRAYS.
11633
11634  033150  005037  002414    7$:   CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
11635  033154  005037  002416          CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
11636
11637                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 15:0
11638
;1639  033160  004537  006430          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
;1640  033164  000005                  .WORD   PTER5                   ;SELECT TRDI BITS 15:0
11641
11642                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 31:16
11643
11644  033166  004537  006430          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
11645  033172  000006                  .WORD   PTER6                   ;SELECT TRDI BITS 31:16
11646
11647                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 47:32
11648
11649  033174  004537  006430          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
11650  033200  000007                  .WORD   PTER7                   ;SELECT TRDI BITS 47:32
11651
11652                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 59:48
11653
11654  033202  004537  006430          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
11655  033206  000010                  .WORD   PTER8                   ;SELECT TRDI BITS 59:48
11656
11657                                   ;THE FOLLOWING SECTION OF CODE WILL WRITE DATA EQUAL TO 16 INTO ADDRESS
11658                                   ;ZERO OF THE AND ARRAY SELECTED BY PTER0 L. THE REMAINING AND ARRAYS
11659                                   ;WILL BE WRITTEN WITH DATA EQUAL TO ZERO.
11660
11661  033210  012737  000000  002376    MOV     #PTER0,R2LOAD           ;SETUP TO SELECT AND ARRAY ZERO
11662  033216  012737  000016  002402    MOV     #16,R4LOAD              ;SETUP DATA FOR THE FIRST AND ARRAY
11663  033224  012737  170377  002406    MOV     #170377,R4MASK          ;SETUP TO CHECK ONLY AND ARRAY DATA BITS
11664  033232  004737  006136      8$:   JSR     PC,LDRDR2               ;LOAD, READ AND CHECK CONTROL REG 2
11665  033236  001405                    BEQ     9$                      ;IF LOADED OK THEN GO WRITE DATA
11666  033240                            ERRDF   2,,R2EROR               ;RECISTER 2 NOT EQUAL EXPECTED
11667  033240  104455                    TRAP    C$ERDF
11668  033242  000002                    .WORD   2
11669  033244  000000                    .WORD   0
11670  033246  004706                    .WORD   R2EROR
11671  033250                            CKLOOP
11672  033250  104406                    TRAP    C$CLP1
11673  033252  004737  006170      9$:   JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
11674  033256  001405                    BEQ     10$                     ;IF LOADED OK THEN CONTINUE
11675  033260                            ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
11676  033260  104455                    TRAP    C$ERDF
11677  033262  000003                    .WORD   3
11678  033264  003552                    .WORD   ANDERR
11679  033266  004722                    .WORD   R4EROR
11680  033270                            CKLOOP
11681  033270  104406                    TRAP    C$CLP1
11682  033272  005037  002402    10$:    CLR     R4LOAD                  ;NOT LOAD REMAINING AND ARRAYS TO 0
11683  033276  005237  002376            INC     R2LOAD                  ;UPDATE POINTER TO NEXT AND ARRAY
11684  033302  022737  000017  002376    CMP     #PTER15,R2LOAD          ;CHECK IF ALL AND ARRAYS WRITTEN
11685  033310  001350                    BNE     8$                      ;IF NOT THEN LOAD 0 INTO NEXT ARRAY
```

```
11686
11687                                           ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTRROL REG 2
11688
11689  033312  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11690  033316  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
11691  033320                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11692  033320  104455                          TRAP    C$ERDF
11693  033322  000002                          .WORD   2
11694  033324  000000                          .WORD   0
11695  033326  004706                          .WORD   R2EROR
11696  033330                                  CKLOOP
11697  033330  104406                          TRAP    C$CLP1
11698
11699                                           ;SELECT ADDRESS ONE IN THE OR ADDRESS REGISTER. LOCATION 1 WILL BE
11700                                           ;WRITTEN WITH DATA TO SET SBL58 FLIP-FLOP LATER ON IN TEST.
11701
11702  033332  012737  000001  002414  11$:     MOV     #1,R6LOAD               ;SETUP ADDRESS TO BE LOADED
11703  033340  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11704  033346  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11705  033352  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
11706  033354                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER ERROR - ORAD 3:0
11707  033354  104455                          TRAP    C$ERDF
11708  033356  000004                          .WORD   4
11709  033360  003163                          .WORD   ORADER
11710  033362  004736                          .WORD   R026ER
11711  033364                                  CKLOOP
11712  033364  104406                          TRAP    C$CLP1
11713
11714                                           ;LOAD LOCATION ONE OF THE OR ARRAY RAMS WITH DATA EQUAL TO 20.  THIS
11715                                           ;DATA PATTERN WILL SET THE SIGNLA OR04 L TO THE LOW STATE AND ALL OTHER
11716                                           ;OR ARRAY DATA BITS TO THE HIGH STATE.  THIS DATA PATTERN WILL CAUSE
11717                                           ;SBL58 FLIP-FLOP TO BE SET TO THE HIGH STATE LATER ON IN THE TEST.
11718
11719  033366  012737  000020  002402  12$:     MOV     #BIT4,R4LOAD            ;SETUP DATA TO BE LOADED
11720  033374  012737  177400  002406          MOV     #177400,R4MASK          ;SETUF TO IGNORE UNWANTED BITS
11721  033402  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
11722  033406  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
11723  033410                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA ERROR
11724  033410  104455                          TRAP    C$ERDF
11725  033412  000003                          .WORD   3
11726  033414  003514                          .WORD   ORDATA
11727  033416  004722                          .WORD   R4EROR
11728  033420                                  CKLOOP
11729  033420  104406                          TRAP    C$CLP1
11730
11731                                           ;SET CDAL4 TO A 1 IN CONTROL REGISTER 0. CDAL4 ON A 1 WILL ENABLE THE
11732                                           ;OUTPUTS OF ALL THE AND AND OR ARRAY RAMS AT THE SAME TIME.
11733
11734  033422  052737  000020  002370  13$:     BIS     #CDAL4,R0LOAD           ;SETUP BE TO BE CLEARED
11735  033430  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11736  033434  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
11737  033436                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
11738  033436  104455                          TRAP    C$ERDF
11739  033440  000001                          .WORD   1
11740  033442  000000                          .WORD   0
11741  033444  004606                          .WORD   R0EROR
```

```
11742  033446                                        CKLOOP
11743  033446  104406                                TRAP    C$CLP1
11744
11745                                                ;READ BOTH THE AND ARRAY RAM AND THE OR ARRAY RAMS DATA.  A DATA
11746                                                ;PATTERN OF 16 WAS WRITTEN INTO THE FIRST AND ARRAY AND ALL ZEROES
11747                                                ;WERE WRITTEN INTO THE REMAINING AND ARRAYS.  A DATA PATTERN EQUAL
11748                                                ;TO 16 SHOULD BE READ BACK FROM THE AND ARRAY DO TO THE WIRED OR
11749                                                ;EFFECT OF THE AND ARRAY OUTPUTS.  A DATA PATTERN EQUAL TO 20 SHOULD
11750                                                ;BE READ BACK FROM THE OR ARRAY RAMS.
11751
11752  033450  112737  000016  002405  14$:    MOVB    #16,R4GOOD+1            ;ADD AND ARRAY DATA TO OR ARRAY DATA
11753  033456  012737  170000  002406          MOV     #170000,R4MASK          ;SETUP TO CHECK AND/OR ARRAY DATA
11754  033464  004737  006220                  JSR     PC,READR4               ;GO READ AND CHECK AND/OR ARRAY DATA
11755  033470  001405                          BEQ     15$                     ;IF DATA OK THEN CONTINUE
11756  033472                                   ERRDF   3,ANDOR,R4EROR          ;AND/OR ARRAY RAM DATA ERROR
11757  033472  104455                          TRAP    C$ERDF
11758  033474  000003                          .WORD   3
11759  033476  003651                          .WORD   ANDOR
11760  033500  004722                          .WORD   R4EROR
11761  033502                                   CKLOOP
11762  033502  104406                          TRAP    C$CLP1
11763
11764                                                ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0 TO CAUSE THE FOUT FLIP-
11765                                                ;FLOPS TO BE USED TO ADDRESS THE OR ARRAY RAMS.
11766
11767  033504  052737  000200  002370  15$:    BIS     #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
11768  033512  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11769  033516  001405                          BEQ     16$                     ;IF LOADED OK THEN CONTINUE
11770  033520                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
11771  033520  104455                          TRAP    C$ERDF
11772  033522  000001                          .WORD   1
11773  033524  000000                          .WORD   0
11774  033526  004606                          .WORD   ROEROR
11775  033530                                   CKLOOP
11776  033530  104406                          TRAP    C$CLP1
11777
11778                                                ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING CDAL6
11779                                                ;WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED, WHICH WILL
11780                                                ;CAUSE THE SIGNAL ANST L TO BE PULSED, WHICH WILL CAUSE THE SIGNAL
11781                                                ;ORST L TO BE PULSED.  WHEN THE SIGNAL ANST L IS PULSED
11782                                                ;A COUNT DOWN PULSE WILL BE ISSUED TO EVENT COUNTER 0 BECAUSE OF THE
11783                                                ;AND ARRAY DATA PATTERN (16).  A BORROW SHOULD BE GENERATED FOR EVENT
11784                                                ;COUNTER 0 BECAUSE ALL ZEROES WERE LOADED INTO THE EVENT COUNTERS. A
11785                                                ;BORROW BEING GENERATED ALONG WITH THE COUNT DOWN PULSE WILL CAUSE THE
11786                                                ;OUTPUT OF THE FOUT0 FLIP-FLOP TO GO TO THE LOW STATE, THUS SELECTING
11787                                                ;ADDRESS ONE ON THE OR ADDRESS LINES ORAD 3:0.  SBL56 FLIP-FLOP SHOULD
11788                                                ;ALSO GET SET AS A RESULT OF THE BORROW AND THE COUNT DOWN PULSE.  WHEN
11789                                                ;THE SIGNAL ORST L IS PULSED, DATA BITS 4 AND 5 OF ADDRESS ONE OF
11790                                                ;THE OR ARRAY RAM WILL BE LOADED INTO SBLE FLIP-FLOPS 59 AND 58, THUS
11791                                                ;SETTING SBL58 FLIP-FLOP TO THE HIGH STATE.
11792
11793  033532  004737  006642          16$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11794
11795                                                ;WITH CDAL7 SET TO A ONE, READ CONTROL REGISTER 6 TO CHECK THAT ONLY
11796                                                ;FOUT0 FLIP-FLOP IS SET TO A ONE.  THE FOUT FLIP-FLOPS ARE USED TO
11797                                                ;ADDRESS THE OR ADDRESS REGISTER VIA SIGNAL LINES ORAD 3:0.
```

```
11798
11799  033536  012737  000001  002414  18$:    MOV     #1,R6LOAD               ;SETUP EXPECTED ADDRESS TO BE ONE
11800  033544  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11801  033552  004737  006260                  JSR     PC,READR6               ;GO READ FOUT FLIP-FLOPS 3:0
11802  033556  001405                          BEQ     19$                     ;IF EQUAL TO A ONE THEN CONTINUE
11803  033560                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
11804  033560  104455                          TRAP    C$ERDF
11805  033562  000004                          .WORD   4
11806  033564  003215                          .WORD   EVNTCT
11807  033566  005026                          .WORD   EVNTER
11808  033570                                  CKLOOP
11809  033570  104406                          TRAP    C$CLP1
11810
11811                                          ;SET CDAL3 TO A ONE AND CDAL2 TO A ZERO IN CONTROL REGISTER 0 TO
11812                                          ;ASSERT THE SIGNAL TRSL2 L. THIS SIGNAL WILL ALLOW THE SBL FLIP-FLOPS
11813                                          ;TO BE READBACK ON THE TRDI 59:56 SIGNAL LINES.
11814
11815  033572  052737  000010  002370  19$:    BIS     #CDAL3,R0LOA            ;SETUP BITS TO BE LOADED
11816  033600  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11817  033604  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
11818  033606                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
11819  033606  104455                          TRAP    C$ERDF
11820  033610  000001                          .WORD   1
11821  033612  000000                          .WORD   0
11822  033614  004606                          .WORD   R0EROR
11823  033616                                  CKLOOP
11824  033616  104406                          TRAP    C$CLP1
11825
11826                                          ;ASSERT THE SIGNAL PTER4 L IN POINTER REG VIA CONTROL REG 2.  THIS IS
11827                                          ;TO SETUP FOR A READBACK OF THE SBL F/F'S ON TRDI 59:56 SIGNAL LINES.
11828
11829  033620  012737  000004  002376  20$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
11830  033626  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11831  033632  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
11832  033634                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11833  033634  104455                          TRAP    C$ERDF
11834  033636  000002                          .WORD   2
11835  033640  000000                          .WORD   0
11836  033642  004706                          .WORD   R2EROR
11837  033644                                  CKLOOP
11838  033644  104406                          TRAP    C$CLP1
11839
11840                                          ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 58 AND 56 ARE
11841                                          ;SET AND THAT SBL FLIP-FLOPS 59 AND 57 ARE CLEARED.  SBL BITS 59:56
11842                                          ;ARE READBACK ON TRDI 59:56 SIGNAL LINES WHEN TRSL2 L IS ASSERTED.
11843
11844  033646  012737  002400  002414  21$:    MOV     #BIT10!BIT8,R6LOAD      ;SETUP TO EXPECT SBL 58 AND 56 SET
11845  033654  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY SBL BITS
11846  033662  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK SBL BITS
11847  033666  001405                          BEQ     22$                     ;IF SBL 58 AND 56 SET THEN CONT
11848  033670                                  ERRDF   4,SBLERR,R026ER         ;SBL 59:56 FLIP-FLOP ERROR
11849  033670  104455                          TRAP    C$ERDF
11850  033672  000004                          .WORD   4
11851  033674  003420                          .WORD   SBLERR
11852  033676  004736                          .WORD   R026ER
11853  033700                                  CKLOOP
```

```
11854  033700  104406                          TRAP    C$CLP1
11855
11856                                          ;LOAD EVENT COUNTERS 0 AND 2 AGAIN WITH 0 TO CHECK THAT THE SBL
11857                                          ;FLIP-FLOPS ARE CLEARED WHEN THE SIGNALS W9 L AND W11 L ARE ISSUED
11858                                          ;FROM LOADING THE EVENT COUNTERS.
11859
11860  033702  012737  000011  002376  22$:    MOV     #PTER9,R2LOAD          ;SETUP BITS TO BE LOADED
11861  033710  004737  006136          23$:    JSR     PC,LDRDR2              ;GO LOAD, READ AND CHECK REGISTER 2
11862  033714  001405                          BEQ     24$                    ;IF LOADED OK THEN CONTINUE
11863  033716                                  ERRDF   2,,R2EROR              ;REGISTER 2 NOT EQUAL EXPECTED
11864  033716  104455                          TRAP    C$ERDF
11865  033720  000002                          .WORD   2
11866  033722  000000                          .WORD   0
11867  033724  004706                          .WORD   R2EROR
11868  033726                                  CKLOOP
11869  033726  104406                          TRAP    C$CLP1
11870  033730  012777  000000  146420  24$:    MOV     #0,@REG6               ;CLEAR EVENT COUNTERS 0 AND 2
11871  033736  022737  000013  002376          CMP     #PTER11,R2LOAD         ;CHECK TO EVENT COUNTER 2 LOADED YET
11872  033744  001404                          BEQ     25$                    ;IF YES THEN CONTINUE
11873  033746  062737  000002  002376          ADD     #2,R2LOAD              ;UPDATE POINTER REGISTER TO COUNTER 2
11874  033754  000755                          BR      23$                    ;GO LOAD EVENT COUNTER 2
11875
11876                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
11877                                          ;READBACK OF THE SBL BITS ON THE TRDI SIGNAL LINES 59:56.  WITH THE
11878                                          ;SIGNAL TRSL2 L ASSERTED, THE SBL FLIP-FLOPS WILL BE READBACK ON
11879                                          ;TRDI BITS 59:56 WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
11880
11881  033756  012737  000004  002376  25$:    MOV     #PTER4,R2LOAD          ;SETUP BITS TO BE LOADED
11882  033764  004737  006136                  JSR     PC,LDRDR2              ;GO LOAD, READ AND CHECK REGISTER 2
11883  033770  001405                          BEQ     26$                    ;IF LOADED OK THEN CONTINUE
11884  033772                                  ERRDF   2,,R2EROR              ;REGISTER 2 NOT EQUAL EXPECTED
11885  033772  104455                          TRAP    C$ERDF
11886  033774  000002                          .WORD   2
11887  033776  000000                          .WORD   0
11888  034000  004706                          .WORD   R2EROR
11889  034002                                  CKLOOP
11890  034002  104406                          TRAP    C$CLP1
11891
11892                                          ;READ CONTROL REGISTER 6 AGAIN TO CHECK THAT LOADING EVENT COUNTERS
11893                                          ;0 AND 2 CLEARED SBL FLIP-FLOPS 58 AND 56.
11894
11895  034004  005037  002414          26$:    CLR     R6LOAD                 ;SETUP TO EXPECT SBL FLIP-FLOPS AS 0
11896  034010  004737  006260                  JSR     PC,READR6              ;GO READ AND CHECK SBL FLIP-FLOPS
11897  034014  001404                          BEQ     27$                    ;IF SBL F/F'S = 0 THEN CONTINUE
11898  034016                                  ERRDF   4,SBLERR,R026ER        ;WRITING EVNT CNTR'S FAILED TO 0 THE SBL F/F'S
11899  034016  104455                          TRAP    C$ERDF
11900  034020  000004                          .WORD   4
11901  034022  003420                          .WORD   SBLERR
11902  034024  004736                          .WORD   R026ER
11903  034026                          27$:    ENDSEG
11904  034026                          10000$:
11905  034026  104405                          TRAP    C$ESEG
11906  034030                                  ENDTST
11907  034030                          L10167:
11908  034030  104401                          TRAP    C$ETST
```

```
                                        .SBTTL  TEST 62: SBL59 AND SBL57 FLIP-FLOP TEST

                                        ;++
                                        ; THIS TEST WILL CHECK THAT SBL57 AND SBL59 FLIP-FLOPS CAN BE SET AND CLEARED.
                                        ; SBL56 AND SBL58 ARE CHECKED TO REMAIN CLEARED DURING THIS TEST.  SBL 59:56
                                        ; FLIP-FLOPS ARE CHECKED BY THE PROGRAM ON THE TRACE RAM DATA IN BUS WHEN THE
                                        ; SIGNAL "TRSL2 L" IS ASSERTED LOW. SBL 59:56 FLIP-FLOPS WILL BE READBACK ON
                                        ; TRDI 59:57 SIGNAL LINES.  SBL56 FLIP-FLOP IS SET VIA A BORROW FROM EVENT
                                        ; COUNTER 1 AND EVENT COUNTER 1 COUNT DOWN PULSE.  SBL57 FLIP-FLOP IS CLEARED
                                        ; BY RELOADING EVENT COUNTER 1.  SBL5 FLIP-FLOP IS SET BY "OR ARRAY RAM" DATA
                                        ; BIT OR05 L BEING SET LOW AND THE SIGNAL ORST L BEING PULSED.  SBL59
                                        ; FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 3.
                                        ;--

034032                                          BGNTST
034032                                  T62::
034032  004737  005476                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
034036                                          BGNSEG
034036  104404                                  TRAP    C$BSEG

                                        ;CLEAR CDAL4 IN CONTROL REGISTER 0. CDAL4 ON A ZERO WILL ALLOW ONLY ONE
                                        ;AND/OR ARRAY RAM TO BE SELECTED AT A TIME.

034040  105037  002370                          CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
034044  004737  006104                          JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
034050  001405                                  BEQ     1$                      ;IF LOADED OK THEN CONTINUE
034052                                          ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
034052  104455                                  TRAP    C$ERDF
034054  000001                                  .WORD   1
034056  000000                                  .WORD   0
034060  004606                                  .WORD   ROEROR
034062                                          CKLOOP
034062  104406                                  TRAP    C$CLP1

                                        ;THE FOLLOWING LOOP WILL LOAD ZEROES INTO EACH OF THE EVENT COUNTER
                                        ;REGISTERS AND EVENT COUNTERS.  BY LOADING EACH EVENT COUNTER, THE
                                        ;SBL FLIP-FLOPS 59:56 WILL BE CLEARED BY SIGNALS W9 L, W10 L, W11 L,AND W12 L.

034064  012737  000011  002376  1$:   MOV     #PTER9,R2LOAD           ;SETUP TO START LOADING AT COUNTER 0
034072  004737  006136          2$:   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
034076  001405                        BEQ     3$                      ;IF LOADED OK THEN CONTINUE
034100                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
034100  104455                        TRAP    C$ERDF
034102  000002                        .WORD   2
034104  000000                        .WORD   0
034106  004706                        .WORD   R2EROR
034110                                CKLOOP
034110  104406                        TRAP    C$CLP1
034112  012777  000000  146236  3$:   MOV     #0,@REG6                ;LOAD ALL ZEROES INTO EVENT COUNTERS
034120  005237  002376                INC     R2LOAD                  ;UPDATE THE POINTER TO NEXT COUNTER
034124  022737  000015  002376        CMP     #PTER13,R2LOAD          ;CHECK IF ALL EVENT COUNTERS LOADED
034132  001357                        BNE     2$                      ;IF NOT THEN LOAD THE NEXT EVENT COUNTER

                                        ;SET CDAL3 TO A ONE AND CDAL2 TO A 0 IN CONTROL REGISTER 0 TO SET THE
                                        ;SIGNAL TRSL2 L. THE SIGNAL TRSL2 L WILL ALLOW SBL BITS 59:56 TO BE
                                        ;READBACK ON TRDI BITS 59:56.
```

```
11966
11966  034134  052737  000010  002370          BIS     #CDAL3,R0LOAD           ;SETUP BITS TO BE LOADED
11967  034142  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11968  034146  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
11969  034150                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED.
11970  034150  104455                          TRAP    C$ERDF
11971  034152  000001                          .WORD   1
11972  034154  000000                          .WORD   0
11973  034156  004606                          .WORD   R0EROR
11974  034160                                  CKLOOP
11975  034160  104406                          TRAP    C$CLP1
11976
11977                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
11978                                          ;2.  THIS IS DONE TO SETUP FOR A READBACK OF TRDI BITS 59:48.
11979
11980  034162  012737  000004  002376  4$:     MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
11981  034170  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11982  034174  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
11983  034176                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11984  034176  104455                          TRAP    C$ERDF
11985  034200  000002                          .WORD   2
11986  034202  000000                          .WORD   0
11987  034204  004706                          .WORD   R2EROR
11988  034206                                  CKLOOP
11989  034206  104406                          TRAP    C$CLP1
11990
11991                                          ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59:56 ARE CLEARED.
11992                                          ;SBL BITS 59:56 ARE READBACK ON TRDI BITS 59:56 WHEN THE SIGNAL TRSL2 L
11993                                          ;IS ASSERTED.  THE SBL FLIP-FLOPS SHOULD HAVE BEEN CLEARED WHEN THE
11994                                          ;EVENT COUNTERS WERE LOADED.
11995
11996  034210  005037  002414          5$:     CLR     R6LOAD                  ;SETUP EXPECTED DATA
11997  034214  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY TRDI 59:56 BITS
11998  034222  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK SBL 59:56 BITS
11999  034226  001405                          BEQ     6$                      ;IF ALL FLIP-FLOPS CLEARED THEN CONT
12000  034230                                  ERRDF   4,SBLERR,R026ER         ;WRITING EVNT CNTR'S FAILED TO 0 SBL F/F'S 59:56
12001  034230  104455                          TRAP    C$ERDF
12002  034232  000004                          .WORD   4
12003  034234  003420                          .WORD   SBLERR
12004  034236  004736                          .WORD   R026ER
12005  034240                                  CKLOOP
12006  034240  104406                          TRAP    C$CLP1
12007
12008                                          ;CLEAR CDAL3 IN CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
12009                                          ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
12010
12011  034242  042737  000010  002370  6$:     BIC     #CDAL3,R0LOAD           ;SETUP BIT TO BE CLEARED
12012  034250  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12013  034254  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
12014  034256                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12015  034256  104455                          TRAP    C$ERDF
12016  034260  000001                          .WORD   1
12017  034262  000000                          .WORD   0
12018  034264  004606                          .WORD   R0EROR
12019  034266                                  CKLOOP
12020  034266  104406                          TRAP    C$CLP1
```

```
12021
12022                                   ;THE FOLLOWING SECTION OF CODE WILL LOAD ALL ZEROES INTO ALL THE TRACE
12023                                   ;RAM DATA IN BUFFERS. THIS WILL SELECT ADDRESS ZERO OF ALL THE AND ARRAYS.
12024
12025 034270 005037 002414        7$:   CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
12026 034274 005037 002416              CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
12027
12028                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 15:0
12029
12030 034300 004537 006430              JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12031 034304 000005                     .WORD   PTER5                   ;SELECT TRDI BITS 15:0
12032
12033                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 31:16
12034
12035 034306 004537 006430              JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12036 034312 000006                     .WORD   PTER6                   ;SELECT TRDI BITS 31:16
12037
12038                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 47:32
12039
12040 034314 004537 006430              JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12041 034320 000007                     .WORD   PTER7                   ;SELECT TRDI BITS 47:32
12042
12043                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 59:48
12044
12045 034322 004537 006430              JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12046 034326 000010                     .WORD   PTER8                   ;SELECT TRDI BITS 59:48
12047
12048                                   ;THE FOLLOWING SECTION OF CODE WILL WRITE DATA EQUAL TO 15 INTO ADDRESS
12049                                   ;ZERO OF THE AND ARRAY SELECTED BY PTER0 L. THE REMAINING AND ARRAYS
12050                                   ;WILL BE WRITTEN WITH DATA EQUAL TO ZERO.
12051
12052 034330 012737 000000 002376       MOV     #PTER0,R2LOAD           ;SETUP TO SELECT AND ARRAY ZERO
12053 034336 012737 000015 002402       MOV     #15,R4LOAD              ;SETUP DATA FOR THE FIRST AND ARRAY
12054 034344 012737 170377 002406       MOV     #170377,R4MASK          ;SETUP TO CHECK ONLY AND ARRAY DATA BITS
12055 034352 004737 006136        8$:   JSR     PC,LDRDR2               ;LOAD, READ AND CHECK CONTROL REG 2
12056 034356 001405                     BEQ     9$                      ;IF LOADED OK THEN GO WRITE DATA
12057 034360                            ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12058 034360 104455                     TRAP    C$ERDF
12059 034362 000002                     .WORD   2
12060 034364 000000                     .WORD   0
12061 034366 004706                     .WORD   R2EROR
12062 034370                            CKLOOP
12063 034370 104406                     TRAP    C$CLP1
12064 034372 004737 006170        9$:   JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
12065 034376 001405                     BEQ     10$                     ;IF LOADED OK THEN CONTINUE
12066 034400                            ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
12067 034400 104455                     TRAP    C$ERDF
12068 034402 000003                     .WORD   3
12069 034404 003552                     .WORD   ANDERR
12070 034406 004722                     .WORD   R4EROR
12071 034410                            CKLOOP
12072 034410 104406                     TRAP    C$CLP1
12073 034412 005037 002402       10$:   CLR     R4LOAD                  ;NOT LOAD REMAINING AND ARRAYS TO 0
12074 034416 005237 002376              INC     R2LOAD                  ;UPDATE POINTER TO NEXT AND ARRAY
12075 034422 022737 000017 002376       CMP     #PTER15,R2LOAD          ;CHECK IF ALL AND ARRAYS WRITTEN
12076 034430 001350                     BNE     8$                      ;IF NOT THEN LOAD 0 INTO NEXT ARRAY
```

```
12077
12078                                           ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTRROL REG 2
12079
12080  034432  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12081  034436  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
12082  034440                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12083  034440  104455                          TRAP    C$ERDF
12084  034442  000002                          .WORD   2
12085  034444  000000                          .WORD   0
12086  034446  004706                          .WORD   R2EROR
12087  034450                                  CKLOOP
12088  034450  104406                          TRAP    C$CLP1
12089
12090                                           ;SELECT ADDRESS TWO IN THE OR ADDRESS REGISTER. LOCATION 2 WILL BE
12091                                           ;WRITTEN WITH DATA TO SET SBL59 FLIP-FLOP LATER ON IN TEST.
12092
12093  034452  012737  000002  002414  11$:     MOV     #2,R6LOAD               ;SETUP ADDRESS TO BE LOADED
12094  034460  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12095  034466  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
12096  034472  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
12097  034474                                  ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REGISTER ERROR - ORAD 3:0
12098  034474  104455                          TRAP    C$ERDF
12099  034476  000004                          .WORD   4
12100  034500  003163                          .WORD   ORADER
12101  034502  004736                          .WORD   RO26ER
12102  034504                                  CKLOOP
12103  034504  104406                          TRAP    C$CLP1
12104
12105                                           ;LOAD LOCATION TWO OF THE OR ARRAY RAMS WITH DATA EQUAL TO 40.  THIS
12106                                           ;DATA PATTERN WILL SET THE SIGNLA ORO5 L TO THE LOW STATE AND ALL OTHER
12107                                           ;OR ARRAY DATA BITS TO THE HIGH STATE.  THIS DATA PATTERN WILL CAUSE
12108                                           ;SBL59 FLIP-FLOP TO BE SET TO THE HIGH STATE LATER ON IN THE TEST.
12109
12110  034506  012737  000040  002402  12$:     MOV     #BIT5,R4LOAD            ;SETUP DATA TO BE LOADED
12111  034514  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
12112  034522  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
12113  034526  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
12114  034530                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA ERROR
12115  034530  104455                          TRAP    C$ERDF
12116  034532  000003                          .WORD   3
12117  034534  003514                          .WORD   ORDATA
12118  034536  004722                          .WORD   R4EROR
12119  034540                                  CKLOOP
12120  034540  104406                          TRAP    C$CLP1
12121
12122                                           ;SET CDAL4 TO A 1 IN CONTROL REGISTER 0. CDAL4 ON A 1 WILL ENABLE THE
12123                                           ;OUTPUTS OF ALL THE AND AND OR ARRAY RAMS AT THE SAME TIME.
12124
12125  034542  052737  000020  002370  13$:     BIS     #CDAL4,ROLOAD           ;SETUP BE TO BE CLEARED
12126  034550  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12127  034554  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
12128  034556                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12129  034556  104455                          TRAP    C$ERDF
12130  034560  000001                          .WORD   1
12131  034562  000000                          .WORD   0
12132  034564  004606                          .WORD   ROEROR
```

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12133  034566                                  CKLOOP
12134  034566  104406                          TRAP    C$CLP1
12135
12136                                          ;READ BOTH THE AND ARRAY RAM AND THE OR ARRAY RAMS DATA.  A DATA
12137                                          ;PATTERN OF 15 WAS WRITTEN INTO THE FIRST AND ARRAY AND ALL ZEROES
12138                                          ;WERE WRITTEN INTO THE REMAINING AND ARRAYS.  A DATA PATTERN EQUAL
12139                                          ;TO 15 SHOULD BE READ BACK FROM THE AND ARRAY DO TO THE WIRED OR
12140                                          ;EFFECT OF THE AND ARRAY OUTPUTS.  A DATA PATTERN EQUAL TO 40 SHOULD
12141                                          ;BE READ BACK FROM THE OR ARRAY RAMS.
12142
12143  034570  112737  000015  002405  14$:   MOVB    #15,R4GOOD+1            ;ADD AND ARRAY DATA TO OR ARRAY DATA
12144  034576  012737  170000  002406        MOV     #170000,R4MASK          ;SETUP TO CHECK AND/OR ARRAY DATA
12145  034604  004737  006220                JSR     PC,READR4               ;GO READ AND CHECK AND/OR ARRAY DATA
12146  034610  001405                        BEQ     15$                     ;IF DATA OK THEN CONTINUE
12147  034612                                ERRDF   3,ANDOR,R4EROR          ;AND/OR ARRAY RAM DATA ERROR
12148  034612  104455                        TRAP    C$ERDF
12149  034614  000003                        .WORD   3
12150  034616  003651                        .WORD   ANDOR
12151  034620  004722                        .WORD   R4EROR
12152  034622                                CKLOOP
12153  034622  104406                        TRAP    C$CLP1
12154
12155                                          ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0 TO CAUSE THE FOUT FLIP-
12156                                          ;FLOPS TO BE USED TO ADDRESS THE OR ARRAY RAMS.
12157
12158  034624  052737  000200  002370  15$:   BIS     #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
12159  034632  004737  006104                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12160  034636  001405                        BEQ     16$                     ;IF LOADED OK THEN CONTINUE
12161  034640                                ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12162  034640  104455                        TRAP    C$ERDF
12163  034642  000001                        .WORD   1
12164  034644  000000                        .WORD   0
12165  034646  004606                        .WORD   ROEROR
12166  034650                                CKLOOP
12167  034650  104406                        TRAP    C$CLP1
12168
12169                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING CDAL6
12170                                          ;WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED, WHICH WILL
12171                                          ;CAUSE THE SIGNAL ANST L TO BE PULSED, WHICH WILL CAUSE THE SIGNAL
12172                                          ;ORST L TO BE PULSED.  WHEN THE SIGNAL ANST L IS PULSED
12173                                          ;A COUNT DOWN PULSE WILL BE ISSUED TO EVENT COUNTER 1 BECAUSE OF THE
12174                                          ;AND ARRAY DATA PATTERN (15).  A BORROW SHOULD BE GENERATED FOR EVENT
12175                                          ;COUNTER 1 BECAUSE ALL ZEROES WERE LOADED INTO THE EVENT COUNTERS. A
12176                                          ;BORROW BEING GENERATED ALONG WITH THE COUNT DOWN PULSE WILL CAUSE THE
12177                                          ;OUTPUT OF THE FOUT1 FLIP-FLOP TO GO TO THE LOW STATE, THUS SELECTING
12178                                          ;ADDRESS TWO ON THE OR ADDRESS LINES ORAD 3:0.  SBL57 FLIP-FLOP SHOULD
12179                                          ;ALSO GET SET AS A RESULT OF THE BORROW AND THE COUNT DOWN PULSE.  WHEN
12180                                          ;THE SIGNAL ORST L IS PULSED, DATA BITS 4 AND 5 OF ADDRESS TWO OF
12181                                          ;THE OR ARRAY RAM WILL BE LOADED INTO SBL FLIP-FLOPS 59 AND 58, THUS
12182                                          ;SETTING SBL59 FLIP-FLOP TO THE HIGH STATE.
12183
12184  034652  004737  006642          16$:   JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
12185
12186                                          ;WITH CDAL7 SET TO A ONE, READ CONTROL REGISTER 6 TO CHECK THAT ONLY
12187                                          ;FOUT1 FLIP-FLOP IS SET TO A ONE.  THE FOUT FLIP-FLOPS ARE USED TO
12188                                          ;ADDRESS THE OR ADDRESS REGISTER VIA SIGNAL LINES ORAD 3:0.
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12189
12190  034656  012737  000002  002414  18$:    MOV     #2,R6LOAD               ;SETUP EXPECTED ADDRESS TO BE TWO
12191  034664  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12192  034672  004737  006260                  JSR     PC,READR6               ;GO READ FOUT FLIP-FLOPS 3:0
12193  034676  001405                          BEQ     19$                     ;IF EQUAL TO A ONE THEN CONTINUE
12194  034700                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
12195  034700  104455                          TRAP    C$ERDF
12196  034702  000004                          .WORD   4
12197  034704  003215                          .WORD   EVNTCT
12198  034706  005026                          .WORD   EVNTER
12199  034710                                  CKLOOP
12200  034710  104406                          TRAP    C$CLP1
12201
12202                                          ;SET CDAL3 TO A ONE AND CDAL2 TO A ZERO IN CONTROL REGISTER 0 TO
12203                                          ;ASSERT THE SIGNAL TRSL2 L. THIS SIGNAL WILL ALLOW THE SBL FLIP-FLOPS
12204                                          ;TO BE READBACK ON THE TRDI 55:56 SIGNAL LINES.
12205
12206  034712  052737  000010  002370  19$:    BIS     #CDAL3,R0LOAD           ;SETUP BITS TO BE LOADED
12207  034720  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12208  034724  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
12209  034726                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12210  034726  104455                          TRAP    C$ERDF
12211  034730  000001                          .WORD   1
12212  034732  000000                          .WORD   0
12213  034734  004606                          .WORD   R0EROR
12214  034736                                  CKLOOP
12215  034736  104406                          TRAP    C$CLP1
12216
12217                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REG VIA CONTROL REG 2. THIS IS
12218                                          ;DONE TO SETUP FOR READBACK OF THE SBL F/F'S ON TRDI 59:56 SIGNAL LINES
12219
12220  034740  012737  000004  002376  20$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12221  034746  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12222  034752  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
12223  034754                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12224  034754  104455                          TRAP    C$ERDF
12225  034756  000002                          .WORD   2
12226  034760  000000                          .WORD   0
12227  034762  004706                          .WORD   R2EROR
12228  034764                                  CKLOOP
12229  034764  104406                          TRAP    C$CLP1
12230
12231                                          ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59 AND 57 ARE
12232                                          ;SET AND THAT SBL FLIP-FLOPS 58 AND 56 ARE CLEARED.  SBL BITS 59:56
12233                                          ;ARE READBACK ON TRDI 59:55 SIGNAL LINES WHEN TRSL2 L IS ASSERTED.
12234
12235  034766  012737  005000  002414  21$:    MOV     #BIT11!BIT9,R6LOAD      ;SETUP TO EXPECT SBL 59 AND 57 SET
12236  034774  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY SBL BITS
12237  035002  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK SBL BITS
12238  035006  001405                          BEQ     22$                     ;IF SBL 58 AND 56 SET THEN CONT
12239  035010                                  ERRDF   4,SBLERR,R026ER         ;SBL 59:56 FLIP-FLOP ERROR
12240  035010  104455                          TRAP    C$ERDF
12241  035012  000004                          .WORD   4
12242  035014  003420                          .WORD   SBLERR
12243  035016  004736                          .WORD   R026ER
12244  035020                                  CKLOOP
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12245  035020  104406                          TRAP    C$CLP1
12246
12247                                          ;LOAD EVENT COUNTERS 1 AND 3 AGAIN WITH 0 TO CHECK THAT THE SBL
12248                                          ;FLIP-FLOPS ARE CLEARED WHEN THE SIGNALS W10 L AND W12 L ARE ISSUED
12249                                          ;FROM LOADING THE EVENT COUNTERS.
12250
12251  035022  012737  000012  002376  22$:    MOV     #PTER10,R2LOAD          ;SETUP BITS TO BE LOADED
12252  035030  004737  006136          23$:    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12253  035034  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
12254  035036                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12255  035036  104455                          TRAP    C$ERDF
12256  035040  000002                          .WORD   2
12257  035042  000000                          .WORD   0
12258  035044  004706                          .WORD   R2EROR
12259  035046                                  CKLOOP
12260  035046  104406                          TRAP    C$CLP1
12261  035050  012777  000000  145300  24$:    MOV     #0,@REG6                ;CLEAR EVENT COUNTERS 1 AND 3
12262  035056  022737  000014  002376          CMP     #PTER12,R2LOAD          ;CHECK TO EVENT COUNTER 2 LOADED YET
12263  035064  001404                          BEQ     25$                     ;IF YES THEN CONTINUE
12264  035066  062737  000002  002376          ADD     #2,R2LOAD               ;UPDATE POINTER REGISTER TO COUNTER 3
12265  035074  000755                          BR      23$                     ;GO LOAD EVENT COUNTER 2
12266
12267                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
12268                                          ;READBACK OF THE SBL BITS ON THE TRDI SIGNAL LINES 59:56.  WITH THE
12269                                          ;SIGNAL TRSL2 L ASSERTED, THE SBL FLIP-FLOPS WILL BE READBACK ON
12270                                          ;TRDI BITS 59:56 WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
12271
12272  035076  012737  000004  002376  25$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12273  035104  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12274  035110  001405                          BEQ     26$                     ;IF LOADED OK THEN CONTINUE
12275  035112                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12276  035112  104455                          TRAP    C$ERDF
12277  035114  000002                          .WORD   2
12278  035116  000000                          .WORD   0
12279  035120  004706                          .WORD   R2EROR
12280  035122                                  CKLOOP
12281  035122  104406                          TRAP    C$CLP1
12282
12283                                          ;READ CONTROL REGISTER 6 AGAIN TO CHECK THAT LOADING EVENT COUNTERS
12284                                          ;1 AND 3 CLEARED SBL FLIP-FLOPS 59 AND 57.
12285
12286  035124  005037  002414          26$:    CLR     R6LOAD                  ;SETUP TO EXPECT SBL FLIP-FLOPS AS 0
12287  035130  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK SBL FLIP-FLOPS
12288  035134  001404                          BEQ     27$                     ;IF SBL F/F'S = 0 THEN CONTINUE
12289  035136                                  ERRDF   4,SBLERR,R026ER         ;WRITING EVNT CNTR'S FAILED TO 0 SBL F/F'S
12290  035136  104455                          TRAP    C$ERDF
12291  035140  000004                          .WORD   4
12292  035142  003420                          .WORD   SBLERR
12293  035144  004736                          .WORD   R026ER
12294  035146                          27$:    ENDSEG
12295  035146                          10000$:
12296  035146  104405                          TRAP    C$ESEG
12297  035150                                  ENDTST
12298  035150                          L10170:
12299  035150  104401                          TRAP    C$ETST
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12300                                   .SBTTL  TEST 63: CHECK SBL FLIP-FLOPS 59:56 TO CLEAR VIA CDAL0
12301
12302                                   ;++
12303                                   ; THIS TEST WILL CHECK THAT SBL 59:56 FLIP-FLOPS CAN BE SET AND THAT THEY CAN BE
12304                                   ; CLEARED BY SETTING AND CLEARING CDAL0 IN CONTROL REGISTER 0.  SBL57 AND SBL56
12305                                   ; ARE SET VIA A BORROW FROM EVENT COUNTER 0 AND EVENT COUNTER 1 ALONG WITH THE
12306                                   ; APPROPRIATE COUNT DOWN PULSES.  SBL59 AND SBL58 ARE SET BY "OR ARRAY RAM" DATA
12307                                   ; BITS "ORO3 L" AND "ORO4 L" BEING SET LOW AND THE SIGNAL ORST L BEING
12308                                   ; PULSED.  THE TEST WILL CHECK THAT THE SBL 59:56 FLIP-FLOPS GOT SET BY READING
12309                                   ; THE SBL 59:56 FLIP-FLOPS BACK ON THE TRACE RAM DATA IN BUS BITS TRDI 59:56
12310                                   ; WHEN THE SIGNAL "TRSL2 L" IS ASSERTED LOW.  THE TEST WILL THEN SET AND CLEAR
12311                                   ; CDAL0 IN CONTROL REGISTER 0 TO CLEAR THE SBL 59:56 FLIP-FLOPS.  THE TEST WIL
12312                                   ; THEN CHECK THAT THE SBL 59:56 FLIP-FLOPS GOT CLEARED.
12313                                   ;--
12314
12315  035152                                   BGNTST
12316  035152                           T63::
12317  035152  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
12318
12319  035156                                   BGNSEG
12320  035156  104404                          TRAP    C$BSEG
12321
12322                                   ;CLEAR CDAL4 IN CONTROL REGISTER 0. CDAL4 ON A ZERO WILL ALLOW ONLY ONE
12323                                   ;AND/OR ARRAY RAM TO BE SELECTED AT A TIME.
12324
12325  035160  105037  002370                  CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
12326  035164  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12327  035170  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
12328  035172                                   ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12329  035172  104455                          TRAP    C$ERDF
12330  035174  000001                          .WORD   1
12331  035176  000000                          .WORD   0
12332  035200  004606                          .WORD   R0EROR
12333  035202                                   CKLOOP
12334  035202  104406                          TRAP    C$CLP1
12335
12336                                   ;THE FOLLOWING LOOP WILL LOAD ZEROES INTO EACH OF THE EVENT COUNTER
12337                                   ;REGISTERS AND EVENT COUNTERS.  BY LOADING EACH EVENT COUNTER, THE
12338                                   ;SBL FLIP-FLOPS 59:56 WILL BE CLEARED BY SIGNALS W9 L, W10 L, W11 L,
12339                                   ;AND W12 L.
12340
12341  035204  012737  000011  002376  1$:     MOV     #PTER9,R2LOAD           ;SETUP TO START LOADING AT COUNTER 0
12342  035212  004737  006136          2$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12343  035216  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
12344  035220                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12345  035220  104455                          TRAP    C$ERDF
12346  035222  000002                          .WORD   2
12347  035224  000000                          .WORD   0
12348  035226  004706                          .WORD   R2EROR
12349  035230                                   CKLOOP
12350  035230  104406                          TRAP    C$CLP1
12351  035232  012777  000000  145116  3$:     MOV     #0,@REG6                ;LOAD ALL ZEROES INTO EVENT COUNTERS
12352  035240  005237  002376                  INC     R2LOAD                  ;UPDATE THE POINTER TO NEXT COUNTER
12353  035244  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL EVENT COUNTERS LOADED
12354  035252  001357                          BNE     2$                      ;IF NOT THEN LOAD THE NEXT EVENT COUNTER
12355
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12356                                           ;SET CDAL3 TO A ONE AND CDAL2 TO A 0 IN CONTROL REGISTER 0 TO SET THE
12357                                           ;SIGNAL TRSL2 L. THE SIGNAL TRSL2 L WILL ALLOW SBL BITS 59:56 TO BE
12358                                           ;READBACK ON TRDI BITS 59:56.
12359
12360  035254  052737  000010  002370           BIS     #CDAL3,ROLOAD           ;SETUP BITS TO BE LOADED
12361  035262  004737  006104                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12362  035266  001405                           BEQ     4$                      ;IF LOADED OK THEN CONTINUE
12363  035270                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED.
12364  035270  104455                           TRAP    C$ERDF
12365  035272  000001                           .WORD   1
12366  035274  000000                           .WORD   0
12367  035276  004606                           .WORD   ROEROR
12368  035300                                   CKLOOP
12369  035300  104406                           TRAP    C$CLP1
12370
12371                                           ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
12372                                           ;2.  THIS IS DONE TO SETUP FOR A READBACK OF TRDI BITS 59:48.
12373
12374  035302  012737  000004  002376  4$:      MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12375  035310  004737  006136                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12376  035314  001405                           BEQ     5$                      ;IF LOADED OK THEN CONTINUE
12377  035316                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12378  035316  104455                           TRAP    C$ERDF
12379  035320  000002                           .WORD   2
12380  035322  000000                           .WORD   0
12381  035324  004706                           .WORD   R2EROR
12382  035326                                   CKLOOP
12383  035326  104406                           TRAP    C$CLP1
12384
12385                                           ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59:56 ARE CLEARED.
12386                                           ;SBL BITS 59:56 ARE READBACK ON TRDI BITS 59:56 WHEN THE SIGNAL TRSL2 L
12387                                           ;IS ASSERTED.  THE SBL FLIP-FLOPS SHOULD HAVE BEEN CLEARED WHEN THE
12388                                           ;EVENT COUNTERS WERE LOADED.
12389
12390  035330  005037  002414           5$:     CLR     R6LOAD                  ;SETUP EXPECTED DATA
12391  035334  012737  170377  002416           MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY TRDI 59:56 BITS
12392  035342  004737  006260                   JSR     PC,READR6               ;GO READ AND CHECK SBL 59:56 BITS
12393  035346  001405                           BEQ     6$                      ;IF ALL FLIP-FLOPS CLEARED THEN CONT
12394  035350                                   ERRDF   4,SBLERR,R026ER         ;WRITING EVENT COUNTERS FAILED TO
12395  035350  104455                           TRAP    C$ERDF
12396  035352  000004                           .WORD   4
12397  035354  003420                           .WORD   SBLERR
12398  035356  004736                           .WORD   R026ER
12399  035360                                   CKLOOP
12400  035360  104406                           TRAP    C$CLP1
12401                                                                           ;ZERO SBL FLIP-FLOPS 59:56
12402
12403                                           ;CLEAR CDAL3 IN CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSL0 L. THE
12404                                           ;SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
12405
12406  035362  042737  000010  002370  6$:      BIC     #CDAL3,ROLOAD           ;SETUP BIT TO BE CLEARED
12407  035370  004737  006104                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12408  035374  001405                           BEQ     7$                      ;IF LOADED OK THEN CONTINUE
12409  035376                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12410  035376  104455                           TRAP    C$ERDF
12411  035400  000001                           .WORD   1
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12412  035402  000000                          .WORD   0
12413  035404  004606                          .WORD   ROEROR
12414  035406                                  CKLOOP
12415  035406  104406                          TRAP    C$CLP1
12416
12417                                          ;THE FOLLOWING SECTION OF CODE WILL LOAD ALL ZEROES INTO ALL THE TRACE
12418                                          ;RAM DATA IN BUFFERS.  THIS WILL SELECT ADDRESS ZERO OF ALL THE AND
12419                                          ;ARRAYS.
12420
12421  035410  005037  002414          7$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
12422  035414  005037  002416                  CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
12423
12424                                          ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 15:0
12425
12426  035420  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12427  035424  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
12428
12429                                          ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 31:16
12430
12431  035426  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12432  035432  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
12433
12434                                          ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 47:32
12435
12436  035434  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12437  035440  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
12438
12439                                          ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 59:48
12440
12441  035442  004537  006430                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12442  035446  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
12443
12444                                          ;THE FOLLOWING SECTION OF CODE WILL WRITE DATA EQUAL TO 14 INTO ADDRESS
12445                                          ;ZERO OF THE AND ARRAY SELECTED BY PTERO L. THE REMAINING AND ARRAYS
12446                                          ;WILL BE WRITTEN WITH DATA EQUAL TO ZERO.
12447
12448  035450  012737  000000  002376          MOV     #PTERO,R2LOAD           ;SETUP TO SELECT AND ARRAY ZERO
12449  035456  012737  000014  002402          MOV     #14,R4LOAD              ;SETUP DATA FOR THE FIRST AND ARRAY
12450  035464  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO CHECK ONLY AND ARRAY DATA BITS
12451  035472  004737  006136          8$:     JSR     PC,LDRDR2               ;LOAD, READ AND CHECK CONTROL REG 2
12452  035476  001405                          BEQ     9$                      ;IF LOADED OK THEN GO WRITE DATA
12453  035500                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12454  035500  104455                          TRAP    C$ERDF
12455  035502  000002                          .WORD   2
12456  035504  000000                          .WORD   0
12457  035506  004706                          .WORD   R2EROR
12458  035510                                  CKLOOP
12459  035510  104406                          TRAP    C$CLP1
12460  035512  004737  006170          9$:     JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
12461  035516  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
12462  035520                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
12463  035520  104455                          TRAP    C$ERDF
12464  035522  000003                          .WORD   3
12465  035524  003552                          .WORD   ANDERR
12466  035526  004722                          .WORD   R4EROR
12467  035530                                  CKLOOP
```

```
12468  035530  104406                          TRAP    C$CLP1
12469  035532  005037  002402          10$:    CLR     R4LOAD                  ;NOT LOAD REMAINING AND ARRAYS TO 0
12470  035536  005237  002376                  INC     R2LOAD                  ;UPDATE POINTER TO NEXT AND ARRAY
12471  035542  022737  000017  002376          CMP     #PTER15,R2LOAD          ;CHECK IF ALL AND ARRAYS WRITTEN
12472  035550  001350                          BNE     8$                      ;IF NOT THEN LOAD 0 INTO NEXT ARRAY
12473
12474                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTRROL REG 2
12475
12476  035552  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12477  035556  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
12478  035560                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12479  035560  104455                          TRAP    C$ERDF
12480  035562  000002                          .WORD   2
12481  035564  000000                          .WORD   0
12482  035566  004706                          .WORD   R2EROR
12483  035570                                  CKLOOP
12484  035570  104406                          TRAP    C$CLP1
12485
12486                                          ;SELECT ADDRESS THREE IN THE OR ADDRESS REGISTER. LOCATION 3 WILL BE
12487                                          ;WRITTEN WITH DATA TO SET SBL59 AND SBL58 FLIP-FLOPS LATER ON IN TEST.
12488
12489  035572  012737  000003  002414  11$:    MOV     #3,R6LOAD               ;SETUP ADDRESS TO BE LOADED
12490  035600  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12491  035606  004737  006252                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
12492  035612  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
12493  035614                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER ERROR - ORAD 3:0
12494  035614  104455                          TRAP    C$ERDF
12495  035616  000004                          .WORD   4
12496  035620  003163                          .WORD   ORADER
12497  035622  004736                          .WORD   R026ER
12498  035624                                  CKLOOP
12499  035624  104406                          TRAP    C$CLP1
12500
12501                                          ;LOAD LOCATION 3 OF THE OR ARRAY RAMS WITH DATA EQUAL TO 60.  THIS DATA
12502                                          ;PATTERN WILL SET THE SIGNAL OR05 L AND OR06 L TO THE LOW STATE AND ALL
12503                                          ;OTHER OR ARRAY DATA BITS TO THE HIGH STATE.  THIS DATA PATTERN WILL
12504                                          ;CAUSE SBL59 AND SBL58 FLIP-FLOPS TO BE SET TO THE HIGH STATE LATER
12505                                          ;ON IN THIS TEST.
12506
12507  035626  012737  000060  002402  12$:    MOV     #BIT5!BIT4,R4LOAD       ;SETUP DATA TO BE LOADED
12508  035634  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
12509  035642  004737  006204                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
12510  035646  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
12511  035650                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA ERROR
12512  035650  104455                          TRAP    C$ERDF
12513  035652  000003                          .WORD   3
12514  035654  003514                          .WORD   ORDATA
12515  035656  004722                          .WORD   R4EROR
12516  035660                                  CKLOOP
12517  035660  104406                          TRAP    C$CLP1
12518
12519                                          ;SET CDAL4 TO A 1 IN CONTROL REGISTER 0. CDAL4 ON A 1 WILL ENABLE THE
12520                                          ;OUTPUTS OF ALL THE AND AND OR ARRAY RAMS AT THE SAME TIME.
12521
12522  035662  052737  000020  002370  13$:    BIS     #CDAL4,R0LOAD           ;SETUP BE TO BE CLEARED
12523  035670  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
```

```
12524  035674  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
12525  035676                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12526  035676  104455                          TRAP    C$ERDF
12527  035700  000001                          .WORD   1
12528  035702  000000                          .WORD   0
12529  035704  004606                          .WORD   ROEROR
12530  035706                                  CKLOOP
12531  035706  104406                          TRAP    C$CLP1
12532
12533                                          ;READ BOTH THE AND ARRAY RAM AND THE OR ARRAY RAMS DATA.  A DATA
12534                                          ;PATTERN OF 14 WAS WRITTEN INTO THE FIRST AND ARRAY AND ALL ZEROES
12535                                          ;WERE WRITTEN INTO THE REMAINING AND ARRAYS.  A DATA PATTERN EQUAL
12536                                          ;TO 14 SHOULD BE READ BACK FROM THE AND ARRAY DO TO THE WIRED OR
12537                                          ;EFFECT OF THE AND ARRAY OUTPUTS.  A DATA PATTERN EQUAL TO 60 SHOULD
12538                                          ;BE READ BACK FROM THE OR ARRAY RAMS.
12539
12540  035710  112737  000014  002405  14$:   MOVB    #14,R4GOOD+1            ;ADD AND ARRAY DATA TO OR ARRAY DATA
12541  035716  012737  170000  002406        MOV     #170000,R4MASK          ;SETUP TO CHECK AND/OR ARRAY DATA
12542  035724  004737  006220                JSR     PC,READR4               ;GO READ AND CHECK AND/OR ARRAY DATA
12543  035730  001405                          BEQ     15$                     ;IF DATA OK THEN CONTINUE
12544  035732                                  ERRDF   3,ANDOR,R4EROR          ;AND/OR ARRAY RAM DATA ERROR
12545  035732  104455                          TRAP    C$ERDF
12546  035734  000003                          .WORD   3
12547  035736  003651                          .WORD   ANDOR
12548  035740  004722                          .WORD   R4EROR
12549  035742                                  CKLOOP
12550  035742  104406                          TRAP    C$CLP1
12551
12552                                          ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0 TO CAUSE THE FOUT FLIP-
12553                                          ;FLOPS TO BE USED TO ADDRESS THE OR ARRAY RAMS.
12554
12555  035744  052737  000200  002370  15$:   BIS     #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
12556  035752  004737  006104                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12557  035756  001405                          BEQ     16$                     ;IF LOADED OK THEN CONTINUE
12558  035760                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12559  035760  104455                          TRAP    C$ERDF
12560  035762  000001                          .WORD   1
12561  035764  000000                          .WORD   0
12562  035766  004606                          .WORD   ROEROR
12563  035770                                  CKLOOP
12564  035770  104406                          TRAP    C$CLP1
12565
12566                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING CDAL6
12567                                          ;WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED, WHICH WILL
12568                                          ;CAUSE THE SIGNAL ANST L TO BE PULSED, WHICH WILL CAUSE THE SIGNAL
12569                                          ;ORST L TO BE PULSED.  WHEN THE SIGNAL ANST L IS PULSED,
12570                                          ;A COUNT DOWN PULSE WILL BE ISSUED TO EVENT COUNTERS 0 AND 1 BECAUSE OF
12571                                          ;THE AND ARRAY DATA PATTERN (14). A BORROW SHOULD BE GENERATED FOR EVENT
12572                                          ;COUNTERS 0 + 1 BECAUSE ALL ZEROES WERE LOADED INTO THE EVENT COUNTERS.
12573                                          ;A BORROW BEING GENERATED ALONG WITH THE COUNT DOWN PULSE WILL CAUSE THE
12574                                          ;OUTPUT OF THE FOUT1 AND FOUTO FLIP-FLOP TO GO TO THE LOW STATE, THUS
12575                                          ;SELECTING ADDRESS 3 ON THE OR ADDRESS LINES ORAD 3:0.  SBL57 AND SBL56
12576                                          ;FLIP-FLOPS SHOULD ALSO GET SET AS A RESULT OF THE BORROW AND THE COUNT
12577                                          ;COUNT DOWN PULSES.  WHEN THE SIGNAL ORST L IS PULSED, DATA BITS 4
12578                                          ;AND 5 OF ADDRESS 3 OF THE OR ARRAY RAM WILL BE LOADED INTO SBL FLIP-
12579                                          ;FLOPS 59 AND 58, THUS SETTING SBL59 AND SBL58 F/F'S TO THE HIGH STATE.
```

```
12580
12581  035772  004737  006642          16$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
12582
12583                                           ;WITH CDAL7 SET TO A ONE, READ CONTROL REGISTER 6 TO CHECK THAT ONLY
12584                                           ;FOUT1 AND FOUT0 F/F'S ARE SET TO A ONE.  THE FOUT F/F'SS ARE USED TO
12585                                           ;ADDRESS THE OR ADDRESS REGISTER VIA SIGNAL LINES ORAD 3:0.
12586
12587  035776  012737  000003  002414  18$:    MOV     #3,R6LOAD               ;SETUP EXPECTED ADDRESS TO BE TWO
12588  036004  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12589  036012  004737  006260                  JSR     PC,READR6               ;GO READ FOUT FLIP-FLOPS 3:0
12590  036016  001405                          BEQ     19$                     ;IF EQUAL TO A ONE THEN CONTINUE
12591  036020                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
12592  036020  104455                          TRAP    C$ERDF
12593  036022  000004                          .WORD   4
12594  036024  003215                          .WORD   EVNTCT
12595  036026  005026                          .WORD   EVNTER
12596  036030                                  CKLOOP
12597  036030  104406                          TRAP    C$CLP1
12598
12599                                           ;SET CDAL3 TO A ONE AND CDAL2 TO A ZERO IN CONTROL REGISTER 0 TO
12600                                           ;ASSERT THE SIGNAL TRSL2 L. THIS SIGNAL WILL ALLOW THE SBL FLIP-FLOPS
12601                                           ;TO BE READBACK ON THE TRDI 59:56 SIGNAL LINES.
12602
12603  036032  052737  000010  002370  19$:    BIS     #CDAL3,R0LOAD           ;SETUP BITS TO BE LOADED
12604  036040  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12605  036044  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
12606  036046                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12607  036046  104455                          TRAP    C$ERDF
12608  036050  000001                          .WORD   1
12609  036052  000000                          .WORD   0
12610  036054  004606                          .WORD   R0EROR
12611  036056                                  CKLOOP
12612  036056  104406                          TRAP    C$CLP1
12613
12614                                           ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
12615                                           ;2.  THIS IS DONE TO SETUP FOR A READBACK OF THE SBL FLIP-FLOPS ON
12616                                           ;TRDI 59:56 SIGNAL LINES.
12617
12618  036060  012737  000004  002376  20$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12619  036066  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12620  036072  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
12621  036074                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12622  036074  104455                          TRAP    C$ERDF
12623  036076  000002                          .WORD   2
12624  036100  000000                          .WORD   0
12625  036102  004706                          .WORD   R2EROR
12626  036104                                  CKLOOP
12627  036104  104406                          TRAP    C$CLP1
12628
12629                                           ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59:56 ARE SET.
12630                                           ;SBL BITS 59:56 ARE READBACK ON TRDI 59:56 SIGNAL LINES WHEN TRSL2 L IS
12631                                           ;ASSERTED.
12632
12633  036106  012737  007400  002414  21$:    MOV     #7400,R6LOAD            ;SETUP TO EXPECT SBL 59:56 SET
12634  036114  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY SBL BITS
12635  036122  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK SBL BITS
```

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12636  036126  001405                          BEQ     22$                     ;IF SBL 58 AND 56 SET THEN CONT
12637  036130                                  ERRDF   4,SBLERR,R026ER         ;SBL 59:56 FLIP-FLOP ERROR
12638  036130  104455                          TRAP    C$ERDF
12639  036132  000004                          .WORD   4
12640  036134  003420                          .WORD   SBLERR
12641  036136  004736                          .WORD   R026ER
12642  036140                                  CKLOOP
12643  036140  104406                          TRAP    C$CLP1
12644
12645                                          ;SET AND CLEAR CDALO IN CONTROL REGISTER 0 TO CLEAR SBL 59:56 F/F'S.
12646
12647  036142  052737  000001  002370  22$:    BIS     #CDALO,ROLOAD           ;SETUP BIT TO BE LOADED
12648  036150  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12649  036154  001405                          BEQ     23$                     ;IF LOADED OK THEN CONTINUE
12650  036156                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12651  036156  104455                          TRAP    C$ERDF
12652  036160  000001                          .WORD   1
12653  036162  000000                          .WORD   0
12654  036164  004606                          .WORD   R0EROR
12655  036166                                  CKLOOP
12656  036166  104406                          TRAP    C$CLP1
12657  036170  042737  000001  002370  23$:    BIC     #CDALO,ROLOAD           ;SETUP TO CLEAR CDALO
12658  036176  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12659  036202  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
12660  036204                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12661  036204  104455                          TRAP    C$ERDF
12662  036206  000001                          .WORD   1
12663  036210  000000                          .WORD   0
12664  036212  004606                          .WORD   R0EROR
12665  036214                                  CKLOOP
12666  036214  104406                          TRAP    C$CLP1
12667
12668                                          ;READ CONTROL REGISTER 6 AGAIN TO CHECK THAT SETTING AND CLEARING
12669                                          ;CDALO IN CONTROL REGISTER 0 ZEROED SBL FLIP-FLOPS 59:56.
12670
12671  036216  005037  002414          24$:    CLR     R6LOAD                  ;SETUP TO EXPECT SBL FLIP-FLOPS AS 0
12672  036222  004737  006260                  JSR     PC,READR6               ;GO READ AND CHECK SBL FLIP-FLOPS
12673  036226  001404                          BEQ     25$                     ;IF SBL F/F'S = 0 THEN CONTINUE
12674  036230                                  ERRDF   4,SBLERR,R026ER         ;SETTING/CLEARING CDALO FAILED TO
12675  036230  104455                          TRAP    C$ERDF
12676  036232  000004                          .WORD   4
12677  036234  003420                          .WORD   SBLERR
12678  036236  004736                          .WORD   R026ER
12679                                                                          ;CLEAR THE SBL FLIP-FLOPS
12680  036240                          25$:    ENDSEG
12681  036240                          10000$:
12682  036240  104405                          TRAP    C$ESEG
12683  036242                                  ENDTST
12684  036242                          L10171:
12685  036242  104401                          TRAP    C$ETST
12686
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12687                                   .SBTTL  TEST 64: EXTERNAL PROBE LOGIC TEST
12688
12689                                   ;++
12690                                   ; IF THE OPERATOR ANSWERED YES TO THE HARDWARE QUESTION "EXTERNAL PROBE CON-
12691                                   ; NECTED", THE FOLLOWING TEST WILL BE EXECUTED, OTHERWISE, THE TEST WILL BE
12692                                   ; ABORTED.  BEFORE THIS TEST CAN BE PERFORMED, THE OPERATOR MUST PLUG THE
12693                                   ; EXTERNAL PROBE INTO THE STATE ANALYZER MODULE AND CONNECT THE PROBE LEADS
12694                                   ; 7:0 TO EVENT COUNTER 0 SIGNALS SDBL 7:0 H RESPECTIVELY.  THE PROBE'S "CLK"
12695                                   ; LEAD MUST BE CONNECTED TO EVENT COUNTER 1'S SIGNAL SDBL8 H.
12696                                   ;
12697                                   ; THIS TEST WILL CHECK THE EXTERNAL PROBE AND THE EXTERNAL PROBE LOGIC ON THE
12698                                   ; STATE ANALYZER MODULE.  DATA PATTERNS OF 252 AND 125 WILL BE LOADED INTO
12699                                   ; EVENT COUNTER 0 TO PROVIDE LOGIC LEVELS TO THE EXTERNAL PROBE'S INPUTS. THE
12700                                   ; SIGNAL SDBL8 H IN EVENT COUNTER 1 WILL BE SET AND CLEARED TO PROVIDE THE "CLK"
12701                                   ; SIGNAL FOR THE EXTERNAL PROBE'S INPUT.  WHEN PDAL4, IN CONTROL REGISTER 2, IS
12702                                   ; SET TO A ZERO AND THE CLK SIGNAL IS SET HIGH FROM A LOW STATE, EVENT COUNTER
12703                                   ; 0'S DATA WILL BE LOADED INTO EXTP 7:0 FLIP-FLOPS.  WHEN PDAL4 IS SET TO A ONE
12704                                   ; AND THE CLK SIGNAL IS SET LOW FROM A HIGH STATE, EVENT COUNTER 0'S DATA WILL
12705                                   ; BE LOADED INTO EXTP 7:0 FLIP-FLOPS.  THIS TEST WILL CHECK THAT THE CORRECT
12706                                   ; DATA IS LOADED INTO EXTP 7:0 FLIP-FLOPS AND THAT THE DATA IS ONLY LOADED ON
12707                                   ; THE CORRECT TRANSITION OF THE CLK SIGNAL.  EXTP 7:0 FLIP-FLOPS ARE READBACK
12708                                   ; OF THE TRACE RAM DATA IN BUS SIGNAL LINES TRDI 55:48 WHEN THE SIGNAL TRSL2 L
12709                                   ; IS ASSERTED LOW.
12710                                   ;--
12711
12712  036244                                   BGNTST
12713  036244                           T64::
12714  036244  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
12715  036250  005737  002366                  TST     EXTPRB                  ;CHECK IF EXTERNAL PROBE CONNECTED
12716  036254  001002                          BNE     1$                      ;IF YES THEN DO THE TEST
12717  036256                                   EXIT    TST                     ;OTHERWISE SKIP THE TEST
12718  036256  104432                          TRAP    C$EXIT
12719  036260  001046                          .WORD   L10172-.
12720  036262                           1$:     BGNSEG
12721  036262  104404                          TRAP    C$BSEG
12722
12723                                   ;ASSERT THE SIGNAL TRSL2 L BY SETTING THE SIGNAL CDAL3 TO A ONE IN
12724                                   ;CONTROL REGISTER 0.  TRSL2 L BEING ASSERTED WILL ENABLE THE OUTPUTS
12725                                   ;OF THE EXTP 7:0 FLIP-FLOPS ONTO THE TRACE RAM DATA IN BUS.  THE
12726                                   ;SIGNALS EXTP 7:0 WILL BE READBACK ON TRDI BITS 55:48 RESPECTIVELY.
12727
12.28  036264  112737  000010  002370          MOVB    #CDAL3,ROLOAD           ;SETUP BIT TO BE LOADED
12729  036272  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12730  036276  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
12731  036300                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12732  036300  104455                          TRAP    C$ERDF
12733  036302  000001                          .WORD   1
12734  036304  000000                          .WORD   0
12735  036306  004606                          .WORD   ROEROR
12736  036310                                   CKLOOP
12737  036310  104406                          TRAP    C$CLP1
12738
12739                                   ;DURING THIS TEST, EVENT COUNTER 0 SIGNALS SDBL 7:0 MUST BE CONNECTED
12740                                   ;TO EXTERNAL PROBE SIGNALS EXT 7:0 RESPECTIVELY.  EVENT COUNTER 1
12741                                   ;SIGNAL SDBL8 MUST BE CONNECTED TO EXTERNAL PROBE SIGNAL CLK.
12742
```

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12743                                          ;THE FOLLOWING SECTION OF CODE WILL LOAD EVENT COUNTER 0 WITH A DATA
12744                                          ;PATTERN OF 252 AND EVENT COUNTER 1 WITH A DATA PATTERN OF 0.  THE
12745                                          ;TEST WILL THEN LOAD EVENT COUNTER 1 WITH A DATA PATTERN OF 1 TO SET
12746                                          ;THE SIGNAL "CLK" TO THE HIGH STATE.  SETTING THE SIGNAL "CLK" TO THE
12747                                          ;HIGH STATE WITH PDAL4 ON A 0 WILL CAUSE EVENT COUNTER 0 DATA TO BE
12748                                          ;LOADED INTO EXTP 7:0 FLIP-FLOP'S.
12749
12750  036312  012701  000252          2$:    MOV     #252,R1                 ;SETUP EVENT COUNTER 0 DATA
12751  036316  012737  000011  002376         MOV     #PTER9,R2LOAD           ;SETUP TO SELECT EVENT COUNTER 0
12752  036324  004737  006136          3$:    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12753  036330  001405                         BEQ     4$                      ;IF LOADED OK THEN CONTINUE
12754  036332                                 ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12755  036332  104455                         TRAP    C$ERDF
12756  036334  000002                         .WORD   2
12757  036336  000000                         .WORD   0
12758  036340  004706                         .WORD   R2EROR
12759  036342                                 CKLOOP
12760  036342  104406                         TRAP    C$CLP1
12761  036344  010177  144006          4$:    MOV     R1,@REG6                ;WRITE DATA INTO EVENT COUNTER 0 OR 1
12762  036350  012737  000012  002376         MOV     #PTER10,R2LOAD          ;SETUP TO LOAD EVENT COUNTER 1
12763  036356  105701                         TSTB    R1                      ;CHECK IF JUST LOADED EVENT COUNTER 0
12764  036360  100002                         BPL     5$                      ;IF NO THEN CHECK EVENT COUNTER 1
12765  036362  005001                         CLR     R1                      ;SETUP EVENT COUNTER 0 DATA TO = 0
12766  036364  000757                         BR      3$                      ;GO LOAD EVENT COUNTER 1 WITH 0
12767  036366  001002          5$:    BNE     6$                      ;IF A ONE LOADED THEN GO READ DATA
12768  036370  005201                         INC     R1                      ;SETUP EVENT COUNTER 1 DATA TO = 1
12769  036372  000754                         BR      3$                      ;GO LOAD EVENT COUNTER 1 WITH 1
12770
12771                                          ;ASSERT PTER4 L IN THE POINTER REG TO ENABLE TRDI BITS 59:48 TO BE READ.
12772
12773  036374  012737  000004  002376  6$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12774  036402  004737  006136                 JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12775  036406  001405                         BEQ     7$                      ;IF LOADED OK THEN CONTINUE
12776  036410                                 ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12777  036410  104455                         TRAP    C$ERDF
12778  036412  000002                         .WORD   2
12779  036414  000000                         .WORD   0
12780  036416  004706                         .WORD   R2EROR
12781  036420                                 CKLOOP
12782  036420  104406                         TRAP    C$CLP1
12783
12784                                          ;READ TRDI BITS 55:48 TO CHECK THAT EVENT COUNTER 0 DATA WAS LOADED
12785                                          ;INTO EXTP 7:0 FLIP-FLOPS WHEN THE SIGNAL "CLK" WAS SET HIGH BY SETTING
12786                                          ;SDBL BIT 8 IN EVENT COUNTER 1.
12787
12788  036422  012737  000252  002414  7$:    MOV     #252,R6LOAD             ;SETUP EXPECTED DATA TO = EVNT CNTR 0
12789  036430  012737  177400  002416         MOV     #177400,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12790  036436  004737  006260                 JSR     PC,READR6               ;GO READ EXTP 7:0 ON TRDI BITS 55:48
12791  036442  001405                         BEQ     8$                      ;IF DATA EQUAL DATA LOADED THEN CONT
12792  036444                                 ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP ERROR OR LOGIC
12793  036444  104455                         TRAP    C$ERDF
12794  036446  000004                         .WORD   4
12795  036450  003452                         .WORD   EXTPER
12796  036452  004736                         .WORD   R026ER
12797  036454                                 CKLOOP
12798  036454  104406                         TRAP    C$CLP1
```

```
12799
12800                                   ;LOAD EVENT COUNTER 0 WITH DATA EQUAL TO 125 AND LOAD EVENT COUNTER 1
12801                                   ;WITH DATA EQUAL TO 0 TO SET SET THE SIGNAL "CLK" TO THE LOW STATE.
12802                                   ;DATA (252) ALREADY IN THE EXTP 7:0 FLIP-FLOPS SHOULD NOT CHANGE BY
12803                                   ;SETTING THE SIGNAL "CLK" LOW.
12804
12805  036456  012701  000125      8$:  MOV     #125,R1                    ;SETUP EVENT COUNTER 0 DATA
12806  036462  012737  000011  002376  MOV     #PTER9,R2LOAD              ;SETUP TO SELECT EVENT COUNTER 0
12807  036470  004737  006136     10$:  JSR     PC,LDRDR2                  ;GO LOAD, READ AND CHECK REGISTER 2
12808  036474  001405                  BEQ     11$                        ;IF LOADED OK THEN CONTINUE
12809  036476                          ERRDF   2,,R2EROR                  ;REGISTER 2 NOT EQUAL EXPECTED
12810  036476  104455                  TRAP    C$ERDF
12811  036500  000002                  .WORD   2
12812  036502  000000                  .WORD   0
12813  036504  004706                  .WORD   R2EROR
12814  036506                          CKLOOP
12815  036506  104406                  TRAP    C$CLP1
12816  036510  010177  143642     11$:  MOV     R1,@REG6                   ;LOAD EVENT COUNTER 0 OR 1
12817  036514  001404                  BEQ     12$                        ;EXIT IF EVENT COUNTER 1 LOADED
12818  036516  005237  002376          INC     R2LOAD                     ;UPDATE POINTER TO EVENT COUNTER 1
12819  036522  005001                  CLR     R1                         ;SETUP TO LOAD EVENT COUNTER 1 WITH 0
12820  036524  000761                  BR      10$                        ;GO LOAD EVENT COUNTER 1 WITH 0
12821
12822                                   ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO ENABLE THE
12823                                   ;READBACK OF TRDI BITS 59:48.
12824
12825  036526  012737  000004  002376  12$:  MOV     #PTER4,R2LOAD              ;SETUP BITS TO BE LOADED
12826  036534  004737  006136          JSR     PC,LDRDR2                  ;GO LOAD, READ AND CHECK REGISTER 2
12827  036540  001405                  BEQ     13$                        ;IF LOADED OK THEN CONTINUE
12828  036542                          ERRDF   2,,R2EROR                  ;REGISTER 2 NOT EQUAL EXPECTED
12829  036542  104455                  TRAP    C$ERDF
12830  036544  000002                  .WORD   2
12831  036546  000000                  .WORD   0
12832  036550  004706                  .WORD   R2EROR
12833  036552                          CKLOOP
12834  036552  104406                  TRAP    C$CLP1
12835
12836                                   ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE SIGNAL "CLK"
12837                                   ;TO THE LOW STATE DID NOT CHANGE THE PREVIOUS DATA (252) LOADED.
12838                                   ;AT THIS POINT THE DATA INPUTS TO THE EXTP 7:0 FLIP-FLOPS WILL
12839                                   ;EQUAL 125 WHICH IS THE DATA IN EVENT COUNTER 0.
12840
12841  036554  004737  006260     13$:  JSR     PC,READR6                  ;GO CHECK EXTP F/F'S TO EQUAL 252
12842  036560  001405                  BEQ     14$                        ;IF DATA OK THEN CONTINUE
12843  036562                          ERRDF   4,EXTPER,R026ER            ;EXTP 7:0 FLIP-FLOPS NOT EQUAL 252
12844  036562  104455                  TRAP    C$ERDF
12845  036564  000004                  .WORD   4
12846  036566  003452                  .WORD   EXTPER
12847  036570  004736                  .WORD   R026ER
12848  036572                          CKLOOP
12849  036572  104406                  TRAP    C$CLP1
12850
12851                                   ;LOAD EVENT COUNTER 1 WITH DATA EQUAL TO 1 TO SET THE SIGNAL "CLK"
12852                                   ;TO THE HIGH STATE.  SETTING THE SIGNAL "CLK" TO THE HIGH STATE WILL
12853                                   ;LOAD THE DATA (125) FROM EVENT COUNTER 0 INTO EXTP 7:0 FLIP-FLOPS.
12854
```

```
12855  036574  012737  000012  002376  14$:    MOV     #PTER10,R2LOAD          ;SETUP TO SELECT EVENT COUNTER 1
12856  036602  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12857  036606  001405                          BEQ     15$                     ;IF LOADED OK THEN CONTINUE
12858  036610                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12859  036610  104455                          TRAP    C$ERDF
12860  036612  000002                          .WORD   2
12861  036614  000000                          .WORD   0
12862  036616  004706                          .WORD   R2EROR
12863  036620                                  CKLOOP
12864  036620  104406                          TRAP    C$CLP1
12865  036622  012777  000001  143526  15$:    MOV     #1,@REG6                ;WRITE 1 INTO EVENT COUNTER 1
12866
12867                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO ENABLE THE
12868                                          ;READBACK OF TRDI BITS 59:48
12869
12870  036630  012737  000004  002376          MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12871  036636  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12872  036642  001404                          BEQ     16$                     ;IF LOADED OK THEN CONTINUE
12873  036644                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12874  036644  104455                          TRAP    C$ERDF
12875  036646  000002                          .WORD   2
12876  036650  000000                          .WORD   0
12877  036652  004706                          .WORD   R2EROR
12878
12879                                          ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE SIGNAL "CLK"
12880                                          ;TO THE HIGH STATE LOADED THE DATA (125) FROM EVENT COUNTER 0 INTO
12881                                          ;EXTP 7:0 FLIP-FLOPS.
12882
12883  036654  012737  000125  002414  16$:    MOV     #125,R6LOAD             ;SETUP DATA LOADED INTO EVENT CNTR 0
12884  036662  004737  006260                  JSR     PC,READR6               ;GO READ EXTP 7:0 ON TRDI BITS 55:48
12885  036666  001405                          BEQ     17$                     ;IF DATA OK THEN CONTINUE
12886  036670                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP'S NOT EQUAL 125
12887  036670  104455                          TRAP    C$ERDF
12888  036672  000004                          .WORD   4
12889  036674  003452                          .WORD   EXTPER
12890  036676  004736                          .WORD   R026ER
12891  036700                                  CKLOOP
12892  036700  104406                          TRAP    C$CLP1
12893
12894                                          ;LOAD EVENT COUNTER 0 WITH DATA EQUAL TO 252 AND LOAD EVENT COUNTER 1
12895                                          ;WITH DATA EQUAL TO 0 TO SET THE SIGNAL "CLK" TO THE LOW STATE. THE
12896                                          ;EXTP 7:0 FLIP-FLOPS SHOULD REMAIN UNCHANGED WHEN THE "CLK" SIGNAL
12897                                          ;GOES FROM A HIGH LEVEL TO A LOW LEVEL WHEN THE SIGNAL PDAL4 IS A 0.
12898
12899  036702  012701  000252          17$:    MOV     #252,R1                 ;SETUP EVENT COUNTER 0 DATA
12900  036706  012737  000011  002376          MOV     #PTER9,R2LOAD           ;SETUP TO SELECT EVENT COUNTER 0
12901  036714  004737  006136          18$:    JSR     PC,LDRDR2               ;GO LOAD READ AND CHECK REGISTER 2
12902  036720  001405                          BEQ     19$                     ;IF LOADED OK THEN CONTINUE
12903  036722                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12904  036722  104455                          TRAP    C$ERDF
12905  036724  000002                          .WORD   2
12906  036726  000000                          .WORD   0
12907  036730  004706                          .WORD   R2EROR
12908  036732                                  CKLOOP
12909  036732  104406                          TRAP    C$CLP1
12910  036734  010177  143416          19$:    MOV     R1,@REG6                ;LOAD DATA INTO EVENT COUNTER 0 CR 1
```

```
12911  036740  001404                          BEQ     20$                     ;EXIT IF EVENT COUNTER 1 LOADED WITH 0
12912  036742  005237  002376                  INC     R2LOAD                  ;SETUP TO SELECT EVENT COUNTER 1
12913  036746  005001                          CLR     R1                      ;SETUP TO SET "CLK" TO A LOW STATE
12914  036750  000761                          BR      18$                     ;GO LOAD EVENT COUNTER 1
12915
12916                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
12917                                          ;READBACK OF TRDI BITS 59:48.
12918
12919  036752  012737  000004  002376  20$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12920  036760  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12921  036764  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
12922  036766                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12923  036766  104455                          TRAP    C$ERDF
12924  036770  000002                          .WORD   2
12925  036772  000000                          .WORD   0
12926  036774  004706                          .WORD   R2EROR
12927  036776                                  CKLOOP
12928  036776  104406                          TRAP    C$CLP1
12929
12930                                          ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE SIGNAL "CLK"
12931                                          ;TO THE LOW STATE DID NOT LOAD THE NEW EVENT COUNTER DATA (252) INTO
12932                                          ;THE EXTP 7:0 FLIP-FLOPS.
12933
12934  037000  004737  006260          21$:    JSR     PC,READR6               ;CHECK EXTP 7:0 F/F'S TO EQUAL 125
12935  037004  001405                          BEQ     22$                     ;IF DATA OK THEN CONTINUE
12936  037006                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP ERROR OR LOGIC
12937  037006  104455                          TRAP    C$ERDF
12938  037010  000004                          .WORD   4
12939  037012  003452                          .WORD   EXTPER
12940  037014  004736                          .WORD   R026ER
12941  037016                                  CKLOOP
12942  037016  104406                          TRAP    C$CLP1
12943
12944                                          ;SET THE SIGNAL PDAL4 TO A ONE IN CONTROL REGISTER 4 ALONG WITH THE
12945                                          ;BITS TO ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER.  SETTING
12946                                          ;PDAL4 TO A ONE WHEN THE SIGNAL "CLK" IS SET LOW, WILL CAUSE EVENT
12947                                          ;COUNTER 0 DATA (252), PREVIOULSY LOADED, TO BE LOADED INTO EXTP 7:0 F/F'S.
12948
12949  037020  052737  000020  002376  22$:    BIS     #PDAL4,R2LOAD           ;SETUP ADDITIONAL BIT TO BE LOADED
12950  037026  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12951  037032  001405                          BEQ     23$                     ;IF LOADED OK THEN CONTINUE
12952  037034                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12953  037034  104455                          TRAP    C$ERDF
12954  037036  000002                          .WORD   2
12955  037040  000000                          .WORD   0
12956  037042  004706                          .WORD   R2EROR
12957  037044                                  CKLOOP
12958  037044  104406                          TRAP    C$CLP1
12959
12960                                          ;READ TRDI BITS 55:48 AGAIN CHECKING THAT SETTING PDAL4 TO A ONE WITH
12961                                          ;THE "CLK" SIGNAL IN THE LOW STATE, CAUSED THE DATA (252) IN EVENT
12962                                          ;COUNTER 0 TO BE LOADED INTO EXTP 7:0 FLIP-FLOPS.
12963
12964  037046  012737  000252  002414  23$:    MOV     #252,R6LOAD             ;SETUP DATA LOADED IN EVENT COUNTER 0
12965  037054  004737  006260                  JSR     PC,READR6               ;GO READ EXTP 7:0 BITS ON TRDI 55:48
12966  037060  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
```

```
12967  037062
12968  037062  104455                          ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP ERROR OR LOGIC
12969  037064  000004                          TRAP    C$ERDF
12970  037066  003452                          .WORD   4
12971  037070  004736                          .WORD   EXTPER
12972  037072                                  .WORD   R026ER
12973  037072  104406                          CKLOOP
12974                                          TRAP    C$CLP1
12975                                          ;LOAD EVENT COUNTER 0 WITH DATA PATTERN EQUAL TO 125 AND EVENT COUNTER
12976                                          ;1 WITH DATA PATTERN EQUAL TO 1 TO SET THE SIGNAL "CLK" TO THE HIGH
12977                                          ;STATE.  WITH PDAL4 SET TO A ONE AND "CLK" SET HIGH, THE NEW DATA WILL
12978                                          ;NOT BE LOADED INTO EXTP 7:0 FLIP-FLOPS.  THE DATA IN EXTP 7:0 FLIP-
12979                                          ;FLOPS SHOULD REMAIN AS 252.
12980
12981  037074  012701  000125          24$:    MOV     #125,R1                 ;SETUP EVENT COUNTER 0 DATA PATTERN
12982  037100  012737  000031  002376          MOV     #PDAL4!PTER9,R2LOAD     ;SETUP TO SELECT EVENT COUNTER 0
12983  037106  004737  006136          25$:    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12984  037112  001405                          BEQ     26$                     ;IF LOADED OK THEN CONTINUE
12985  037114                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12986  037114  104455                          TRAP    C$ERDF
12987  037116  000002                          .WORD   2
12988  037120  000000                          .WORD   0
12989  037122  004706                          .WORD   R2EROR
12990  037124                                  CKLOOP
12991  037124  104406                          TRAP    C$CLP1
12992  037126  010177  143224          26$:    MOV     R1,@REG6                ;LOAD EVENT COUNTER 0 OR 1
12993  037132  005301                          DEC     R1                      ;CHECK IF EVENT COUNTER 1 LOADED
12994  037134  001405                          BEQ     27$                     ;EXIT IF EVENT COUNTER 1 LOADED
12995  037136  005237  002376                  INC     R2LOAD                  ;UPDATE POINTER TO EVENT COUNTER 1
12996  037142  012701  000001                  MOV     #1,R1                   ;SETUP TO LOAD 1 INTO EVNT CNTR 1
12997  037146  000757                          BR      25$                     ;GO LOAD EVENT COUNTER 1 WITH 1
12998
12999                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
13000                                          ;READBACK OF TRDI BITS 59:48. PDAL4 WILL ALSO REMAIN SET IN CONTROL REG 2.
13001
13002  037150  012737  000024  002376  27$:    MOV     #PDAL4!PTER4,R2LOAD     ;SETUP BITS TO BE LOADED
13003  037156  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
13004  037162  001405                          BEQ     28$                     ;IF LOADED OK THEN CONTINUE
13005  037164                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
13006  037164  104455                          TRAP    C$ERDF
13007  037166  000002                          .WORD   2
13008  037170  000000                          .WORD   0
13009  037172  004706                          .WORD   R2EROR
13010  037174                                  CKLOOP
13011  037174  104406                          TRAP    C$CLP1
13012
13013                                          ;READ TRDI BITS 59:48 AGAIN TO CHECK THAT SETTING THE "CLK" SIGNAL TO
13014                                          ;THE HIGH STATE DID NOT LOAD THE DATA (125) IN THE EVENT COUNTERS
13015                                          ;INTO EXTP 7:0 FLIP-FLOPS.  THE EXTP 7:0 FLIP-FLOPS SHOULD CONTAIN
13016                                          ;THE PREVIOUS EVENT COUNTER DATA (252).
13017
13018  037176  004737  006260          28$:    JSR     PC,READR6               ;CHECK DATA TO EQUAL PREVIOUS DATA
13019  037202  001405                          BEQ     29$                     ;IF DATA EQUAL THEN CONTINUE
13020  037204                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP OR LOGIC ERROR
13021  037204  104455                          TRAP    C$ERDF
13022  037206  000004                          .WORD   4
```

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13023  037210  003452                          .WORD   EXTPER
13024  037212  004736                          .WORD   R026ER
13025  037214                                  CKLOOP
13026  037214  104406                          TRAP    C$CLP1
13027
13028                                          ;LOAD EVENT COUNTER 1 WITH DATA EQUAL TO 0 TO SET THE "CLK" SIGNAL
13029                                          ;TO THE LOW STATE. SETTING THE "CLK" SIGNAL TO THE LOW STATE SHOULD
13030                                          ;LOAD THE DATA (125) FROM EVENT COUNTER 0 INTO THE EXTP 7:0 FLIP-FLOPS.
13031
13032  037216  012737  000032  002376  29$:    MOV     #PDAL4!PTER10,R2LOAD    ;SETUP BITS TO BE LOADED
13033  037224  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD READ AND CHECK REGISTER 2
13034  037230  001405                          BEQ     30$                     ;IF LOADED OK THEN CONTINUE
13035  037232                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
13036  037232  104455                          TRAP    C$ERDF
13037  037234  000002                          .WORD   2
13038  037236  000000                          .WORD   0
13039  037240  004706                          .WORD   R2EROR
13040  037242                                  CKLOOP
13041  037242  104406                          TRAP    C$CLP1
13042  037244  012777  000000  143104  30$:    MOV     #0,@REG6                ;LOAD EVENT COUNTER 1 WITH 0
13043
13044                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
13045                                          ;READBACK OF TRDI BITS 59:48
13046
13047  037252  012737  000024  002376          MOV     #PDAL4!PTER4,R2LOAD     ;SETUP BITS TO BE LOADED
13048  037260  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
13049  037264  001405                          BEQ     31$                     ;IF LOADED OK THEN CONTINUE
13050  037266                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
13051  037266  104455                          TRAP    C$ERDF
13052  037270  000002                          .WORD   2
13053  037272  000000                          .WORD   0
13054  037274  004706                          .WORD   R2EROR
13055  037276                                  CKLOOP
13056  037276  104406                          TRAP    C$CLP1
13057
13058                                          ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE SIGNAL "CLK"
13059                                          ;TO THE LOW STATE WITH PDAL4 SET TO A ONE WILL LOAD EVENT COUNTER 0
13060                                          ;DATA (125) INTO  EXTP 7:0 FLIP-FLOPS.
13061
13062  037300  012737  000125  002414  31$:    MOV     #125,R6LOAD             ;SETUP EVENT COUNTER 0 DATA LOADED
13063  037306  004737  006260                  JSR     PC,READR6               ;CHECK DATA TO EQUAL EVENT COUNTER 0
13064  037312  001404                          BEQ     32$                     ;IF DATA EQUAL THEN CONTINUE
13065  037314                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP OR LOGIC ERROR
13066  037314  104455                          TRAP    C$ERDF
13067  037316  000004                          .WORD   4
13068  037320  003452                          .WORD   EXTPER
13069  037322  004736                          .WORD   R026ER
13070  037324                          32$:    ENDSEG
13071  037324                          10000$:
13072  037324  104405                          TRAP    C$ESEG
13073  037326                                  ENDTST
13074  037326                          L10172:
13075  037326  104401                          TRAP    C$ETST
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13076                                   .SBTTL  TEST 65: CHECK THAT INIT L CLEARS REG 0 AND REG 2
13077
13078                                   ;++
13079                                   ; THE FOLLOWING TEST WILL CHECK THAT INIT L CAN CLEAR CONTROL REGISTER 2 AND
13080                                   ; THE LOW BYTE OF CONTROL REGISTER 0.  THIS IS DONE BY LOADING ALL ONES INTO
13081                                   ; CONTROL REGISTER 2 AND THE LOW BYTE OF CONTROL REGISTER 0.  THEN A BRESET
13082                                   ; INSTRUCTION IS ISSUED WHICH SHOULD CLEAR REG 2 AND THE LOW BYTE OF REG 0.
13083                                   ;--
13084
13085  037330                                   BGNTST
13086  037330                           T65::
13087  037330  004737  005476                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
13088  037334                                   BGNSEG
13089  037334  104404                           TRAP    C$BSEG
13090
13091                                           ;CHECK THAT CDAL7 H, CDAL6 H, CDAL5 H, CDAL4 H, CDAL3 H, CDAL2 H,
13092                                           ;CDAL1 H, AND CDAL0 H OF CONTROL REGISTER 0 CAN BE SET TO ONES.
13093
13094  037336  112737  000377  002370           MOVB    #377,R0LOAD             ;SETUP TO LOAD ALL ONES
13095  037344  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
13096  037350  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
13097  037352                                   ERRDF   1,,R0EROR               ;CDAL7 TO CDAL0 NOT EQUAL TO 377
13098  037352  104455                           TRAP    C$ERDF
13099  037354  000001                           .WORD   1
13100  037356  000000                           .WORD   0
13101  037360  004606                           .WORD   R0EROR
13102  037362                                   CKLOOP
13103  037362  104406                           TRAP    C$CLP1
13104
13105                                           ;CHECK THAT PDAL7 H TO PDAL0 H OF CONTROL REGISTER 2 CAN BE SET TO ONES
13106
13107  037364  012737  000377  002376  1$:      MOV     #377,R2LOAD             ;SETUP BITS TO BE LOADED
13108  037372  004737  006136                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
13109  037376  001405                           BEQ     2$                      ;IF ALL ONES THEN CONTINUE
13110  037400                                   ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL 377
13111  037400  104455                           TRAP    C$ERDF
13112  037402  000002                           .WORD   2
13113  037404  000000                           .WORD   0
13114  037406  004706                           .WORD   R2EROR
13115  037410                                   CKLOOP
13116  037410  104406                           TRAP    C$CLP1
13117
13118                                           ;ISSUE A BRESET INSTRUCTION. PDAL7 TO PDAL0 SHOULD THEN BE ZEROS.
13119                                           ;ALSO CDAL7 TO CDAL0 SHOULD THEN BE ZEROS.
13120
13121  037412                           2$:      BRESET                          ;CLEAR REG 2 AND THE LOW BYTE OF REG 0
13122  037412  104433                           TRAP    C$RESET
13123  037414                                   SETVEC  #4,#3$,#PRI07
13124  037414  012746  000340                  MOV     #PRI07,-(SP)
13125  037420  012746  037466                  MOV     #3$,-(SP)
13126  037424  012746  000004                  MOV     #4,-(SP)
13127  037430  012746  000003                  MOV     #3,-(SP)
13128  037434  104437                           TRAP    C$SVEC
13129  037436  062706  000010                  ADD     #10,SP
13130  037442  013705  002350                  MOV     REG0,R5                 ;SAVE ADDRESS OF REG 0
13131  037446  113765  002361  000001          MOVB    IDDEV+1,1(R5)           ;SAVE ID NUMBER
```

```
13132  037454  000240                          NOP
13133  037456                                  CLRVEC  #4                      ;RELEASE DEVICE TIMEOUT VECTOR
13134  037456  012700  000004                  MOV     #4,R0
13135  037462  104436                          TRAP    C$CVEC
13136  037464  000420                          BR      4$                      ;IF NO DEVICE TIMEOUT THEN CHECK REG 0
13137
13138                                          ;A DEVICE TIMEOUT OCCURED WHICH INDICATES THAT THERE IS NO DEVICE #0
13139                                          ;IN THE SYSTEM, THEREFORE, THE STATE ANLAYZER HAS TO BE RESELECTED BY
13140                                          ;DOING A "MOV WORD" OPERATION.  A "MOVB" OPERATION PERFORMED ABOVE DOES
13141                                          ;A READ/MODIFY WRITE.  THEREFORE, IF THERE IS NO DEVICE #0 IN THE SYSTEM
13142                                          ;A DEVICE TIMEOUT WILL OCCUR TO ADDRESS 4.
13143
13144  037466  005726                  3$:     TST     (SP)+                   ;CLEAR UP STACK FROM DEVICE TIMEOUT
13145  037470  005726                          TST     (SP)+                   ;
13146  037472                                  CLRVEC  #4                      ;RELEASE DEVICE TIMEOUT VECTOR
13147  037472  012700  000004                  MOV     #4,R0
13148  037476  104436                          TRAP    C$CVEC
13149  037500  105037  002370                  CLRB    R0LOAD                  ;SETUP TO LOAD ALL ZEROES IN LOW BYTE
13150  037504  004737  006104                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
13151  037510  001420                          BEQ     5$                      ;IF OK THEN GO CHECK REGISTER 2
13152  037512                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
13153  037512  104455                          TRAP    C$ERDF
13154  037514  000001                          .WORD   1
13155  037516  000000                          .WORD   0
13156  037520  004606                          .WORD   R0EROR
13157  037522                                  CKLOOP
13158  037522  104406                          TRAP    C$CLP1
13159  037524  000412                          BR      5$                      ;PROCEED IF NO LOOPING INVOKED
13160
13161  037526  105037  002372          4$:     CLRB    R0GOOD                  ;CLEAR LOWER BYTE OF EXPECTED
13162  037532  004737  006120                  JSR     PC,READR0               ;GO READ AND CHECK REG 0
13163  037536  001405                          BEQ     5$                      ;IF OK THEN CONTINUE
13164  037540                                  ERRDF   1,,R0EROR               ;REG 0 NOT EQUAL EXPECTED
13165  037540  104455                          TRAP    C$ERDF
13166  037542  000001                          .WORD   1
13167  037544  000000                          .WORD   0
13168  037546  004606                          .WORD   R0EROR
13169  037550                                  CKLOOP
13170  037550  104406                          TRAP    C$CLP1
13171  037552  005037  002376          5$:     CLR     R2LOAD                  ;SETUP EXPECTED DATA
13172  037556  004737  006144                  JSR     PC,READR2               ;GO READ AND CHECK REG 2
13173  037562  001404                          BEQ     6$                      ;IF OK THEN CONTINUE
13174  037564                                  ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL TO EXPECTED
13175  037564  104455                          TRAP    C$ERDF
13176  037566  000002                          .WORD   2
13177  037570  000000                          .WORD   0
13178  037572  004706                          .WORD   R2EROR
13179  037574                          6$:     ENDSEG
13180  037574                          10000$:
13181  037574  104405                          TRAP    C$ESEG
13182  037576                                  ENDTST
13183  037576                          L10173:
13184  037576  104401                          TRAP    C$ETST
13185  037600                                  ENDMOD
```

```
                                .TITLE PARAMETER CODING

                                .SBTTL  HARDWARE PARAMETER CODING SECTION

037600                                  BGNMOD

                                ;++
                                ; THE HARDWARE PARAMETER CODING SECTION CONTAINS MACROS
                                ; THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
                                ; MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
                                ; INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
                                ; MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
                                ; WITH THE OPERATOR.
                                ;--

037600                                  BGNHRD
037600  000014                          .WORD L10174-L$HARD/2
037602                          L$HARD::

                                ;
                                ;HARDWARE P-TABLE QUESTIONS
                                ;
                                ;       ASK FOR CDS STATE ANALYZER CSR ADDRESS
                                ;       ASK FOR CDS STATE ANALYZER DEVICE NUMBER
                                ;       ASK IF CDS STATE ANALYZER EXTERNAL PROBE CONNECTED
                                ;

037602                                  GPRMA   MSG1,0,0,0,177777,YES
037602  000031                          .WORD   T$CODE
037604  037632                          .WORD   MSG1
037606  000000                          .WORD   T$LOLIM
037610  177777                          .WORD   T$HILIM
037612                                  GPRMD   MSG2,2,0,177777,0,000017,YES
037612  001032                          .WORD   T$CODE
037614  037646                          .WORD   MSG2
037616  177777                          .WORD   177777
037620  000000                          .WORD   T$LOLIM
037622  000017                          .WORD   T$HILIM
037624                                  GPRML   MSG3,4,177777,YES
037624  002130                          .WORD   T$CODE
037626  037664                          .WORD   MSG3
037630  177777                          .WORD   177777


037632                                  ENDHRD
                                        .EVEN
037632                          L10174:
```

```
13234
13235                                   ;
13236                                   ;HARDWARE P-TABLE MESSAGES
13237                                   ;
13238
13239  037632  051503  020122  042101  MSG1:   .ASCIZ  /CSR ADDRESS/
13240  037640  051104  051505  000123
13241  037646  042504  044526  042503  MSG2:   .ASCIZ  /DEVICE NUMBER/
13242  037654  047040  046525  042502
13243  037662  000122
13244  037664  054105  042524  047122  MSG3:   .ASCIZ  /EXTERNAL PROBE CONNECTED/
13245  037672  046101  050040  047522
13246  037700  042502  041440  047117
13247  037706  042516  052103  042105
13248  037714     000
13249          037716                           .EVEN
13250
13251
13252                                   .SBTTL  SOFTWARE PARAMETER CODING SECTION
13253
13254                                   ;++
13255                                   ; THE SOFTWARE PARAMETER CODING SECTION CONTAINS MACROS
13256                                   ; THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
13257                                   ; MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
13258                                   ; INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
13259                                   ; MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
13260                                   ; WITH THE OPERATOR.
13261                                   ;--
13262
13263  037716                           L$SOFT::BGNSFT
13264  037716  000000                           .WORD L10175-L$SOFT/2
13265  037720                           L10175:
13266
13267
13268                                           .EVEN
13269
13270  037720                                   ENDSFT
13271                                           .EVEN
13272  037720                           $PATCH::
13273
13274
13275
13276  037720                                   LASTAD
13277  037720  000010                           .BLKW   10
13278                                           .EVEN
13279                                           .WORD T$FREE
13280  037740                                   .WORD T$SIZE
13281                                   L$LAST::
13282  037740  037756                           ENDMOD
13283  037742  000005
13284  037744
13285  037744
13286
13287
13288
13289
```

```
13290  037744                          BGNSETUP        1.
13291  037744                          BGNPTAB
13292  037744  000000                  .WORD   0
13293  037746  000003                  .WORD   L10200-./2-1
13294  037750                  L10176:
13295  037750  163010                  .WORD   163010
13296  037752  000001                  .WORD   1
13297  037754  000000                  .WORD   0
13298  037756                          ENDPTAB
13299  037756                  L10200:
13300  037756                          ENDSETUP
13301          000001          .END
```

```
ADR    = 000020 G  1790#
ALLREG  004752 G   2254#  10456  10485  10657  10686
ANDERR  003552 G   2068#   7510   7524   7604   7618   7706   7720   7808   7822   7909   7923   8011   8025
                   8113   8127   8215   8229   8316   8330   8418   8432   8520   8534   8622   8636   8723
                   8737   8825   8839   8927   8941   9059   9106   9199   9249   9269   9321   9434   9789
                  10142  11678  12069  12465
ANDOR   003651 G   2080#  11759  12150  12547
ASSEMB= 000010     1501
ASSERT  006400 G   2707#   6819   6838   6856   6874   6925   6990   7080   7200   7491   7585   9522   9585
                   9669   9877   9940  10024  10274  10351  10492  10553  10693  10804  10984
BIT0   = 000001 G  1763#   1839   1859
BIT00  = 000001 G  1752#   1763
BIT01  = 000002 G  1751#   1762
BIT02  = 000004 G  1750#   1761
BIT03  = 000010 G  1749#   1760
BIT04  = 000020 G  1748#   1759
BIT05  = 000040 G  1747#   1758
BIT06  = 000100 G  1746#   1757
BIT07  = 000200 G  1745#   1756
BIT08  = 000400 G  1744#   1755
BIT09  = 001000 G  1743#   1754
BIT1   = 000002 G  1762#   1837   1858
BIT10  = 002000 G  1742#   1818   4478   4585   4692   4803   4904   5044   5116   5221   5361   5433   5537
                   5677   5749   5855   6000   6074  11844
BIT11  = 004000 G  1741#   1817   3571  12235
BIT12  = 010000 G  1740#   1815   7727   7828   8134   8235   8541   8642   8948   9341  10418  10419  10498
                  10620  10649  10914  10942
BIT13  = 020000 G  1739#   1814  10448
BIT14  = 040000 G  1738#   1813  10649
BIT15  = 100000 G  1737#   1807  10448
BIT2   = 000004 G  1761#   1835   1857
BIT3   = 000010 G  1760#   1834   1856
BIT4   = 000020 G  1759#   1831   1852   7012   7141   7239   7297   7372   7434   7531   7624   7930   8031
                   8337   8438   8744   8845  11719  12507
BIT5   = 000040 G  1758#   1828   1851  12110  12507
BIT6   = 000100 G  1757#   1826   1850
BIT7   = 000200 G  1756#   1822   1849  10874
BIT8   = 000400 G  1755#   1820   7625   7726   8032   8133   8439   8540   8846   8947   9338  11844
BIT9   = 001000 G  1754#   1819  12235
BOE    = 000400 G  1794#
CDAL0  = 000001 G  1839#   2533   2543   3633   6128   6335   6348  10218  10234  11052  11062  12647  12657
CDAL1  = 000002 G  1837#
CDAL10= 002000 G   1818#
CDAL11= 004000 G   1817#
CDAL12= 010000 G   1815#
CDAL13= 020000 G   1814#
CDAL14= 040000 G   1813#
CDAL15= 100000 G   1807#   2512   2974
CDAL2  = 000004 G  1835#   4445   4552   4659   4769   4878   4930   5018   5069   5195   5247   5335   5386
                   5511   5563   5651   5702   5827   5881   5972   6025   6806
CDAL3  = 000010 G  1834#  11575  11620  11815  11966  12011  12206  12360  12406  12603  12728
CDAL4  = 000020 G  1831#  11734  12125  12522
CDAL5  = 000040 G  1828#   6487   6599
CDAL6  = 000100 G  1826#   2852   2862
CDAL7  = 000200 G  1822#   9449   9804  10158  10783  10846  10963  11767  12158  12555
CDAL8  = 000400 G  1820#
```

```
CDAL9 = 001000 G    1819#  2974
C$AU  = 000052      1501#  3078
C$AUTO= 000061      1501#  3008
C$BRK = 000022      1501#
C$BSEG= 000004      1501#  2469  2511  2531  2558  2661  2709  2758  2851  3127  3144  3175  3193
                    3227   3258  3275  3307  3325  3359  3401  3467  3536  3554  3593  4254  4330
                    4407   4514  4621  4731  4838  4924  4982  5062  5155  5241  5299  5379  5471
                    5557   5615  5695  5787  5875  5935  6018  6103  6250  6481  6917  6985  7059
                    7180   7259  7318  7394  7459  7553  7647  7749  7850  7952  8054  8156  8257
                    8359   8461  8563  8664  8766  8868  9038  9084  9152  9215  9259  9285  9380
                    9443   9735  9798  10087 10149 10330 10532 10743 11045 11536 11927 12320 12721
                    13089
C$BSUB= 000002      1501#  3719  3739  3787  3807  3855  3875  3924  3944  3992  4012  4060  4080
                    4128   4148  4196  4216  4835  4920  5058  5152  5237  5375  5468  5553  5691
                    5784   5871  6014  6679  6693  6707  6721  6735  7173  7250  7309  7385  8980
                    9027   9073
C$CEFG= 000045      1501#
C$CLCK= 000062      1501#
C$CLEA= 000012      1501#  3033
C$CLOS= 000035      1501#
C$CLP1= 000006      1501#  2492  2542  2578  2676  2773  2796  2861  3415  3433  3481  3500  3629
                    3642   3656  3669  4273  4295  4343  4422  4454  4529  4561  4636  4668  4746
                    4778   4853  4887  4939  4959  4996  5027  5078  5097  5170  5204  5256  5276
                    5313   5344  5395  5414  5486  5520  5572  5592  5629  5660  5711  5730  5802
                    5836   5890  5910  5949  5981  6034  6053  6121  6137  6150  6165  6196  6264
                    6280   6293  6307  6330  6344  6357  6371  6392  6413  6429  6496  6514  6528
                    6543   6569  6594  6608  6750  6769  6795  6815  6834  6852  6870  6943  7075
                    7099   7122  7196  7214  7271  7331  7353  7406  7476  7513  7570  7607  7664
                    7688   7709  7766  7790  7811  7867  7891  7912  7969  7993  8014  8071  8095
                    8116   8173  8197  8218  8274  8298  8319  8376  8400  8421  8478  8502  8523
                    8580   8604  8625  8681  8705  8726  8783  8807  8828  8885  8909  8930  8996
                    9048   9094  9168  9189  9236  9306  9397  9418  9458  9472  9490  9509  9548
                    9572   9613  9641  9655  9752  9773  9813  9827  9845  9864  9903  9927  9968
                    9996   10010 10104 10126 10167 10181 10199 10212 10227 10243 10261 10299 10346
                    10371  10386 10400 10428 10442 10458 10473 10487 10548 10573 10588 10602 10629
                    10643  10659 10674 10688 10758 10772 10792 10835 10855 10867 10884 10898 10923
                    10937  10951 10972 11014 11061 11071 11085 11099 11128 11151 11168 11184 11200
                    11226  11242 11256 11270 11286 11314 11331 11345 11359 11375 11404 11422 11436
                    11450  11466 11494 11550 11565 11584 11598 11615 11629 11672 11681 11697 11712
                    11729  11743 11762 11776 11809 11824 11838 11854 11869 11890 11941 11956 11975
                    11989  12006 12020 12063 12072 12088 12103 12120 12134 12153 12167 12200 12215
                    12229  12245 12260 12281 12334 12350 12369 12383 12400 12415 12459 12468 12484
                    12499  12517 12531 12550 12564 12597 12612 12627 12643 12656 12666 12737 12760
                    12782  12798 12815 12834 12849 12864 12892 12909 12928 12942 12958 12973 12991
                    13011  13026 13041 13056 13103 13116 13158 13170
C$CVEC= 000036      1501#  2503  2589  13135 13148
C$DCLN= 000044      1501#
C$DODU= 000051      1501#
C$DRPT= 000024      1501#
C$DU  = 000053      1501#  3055
C$EDIT= 000003      1501#  1563
C$ERDF= 000055      1501#  2487  2497  2517  2537  2547  2573  2583  2671  2690  2713  2768  2791
                    2813   2821  2829  2835  2856  2866  3135  3152  3184  3202  3231  3266  3283
                    3316   3334  3363  3410  3428  3442  3476  3495  3510  3545  3562  3601  3612
                    3624   3637  3651  3664  3677  4268  4290  4307  4338  4356  4417  4449  4464
                    4524   4556  4571  4631  4663  4678  4741  4773  4790  4848  4882  4896  4934
```

```
                      4954    4969    4991    5022    5036    5073    5092    5108    5165    5199    5213    5251    5271
                      5286    5308    5339    5353    5390    5409    5425    5481    5515    5529    5567    5587    5602
                      5624    5655    5669    5706    5725    5741    5797    5831    5847    5885    5905    5922    5944
                      5976    5992    6029    6048    6066    6116    6132    6145    6160    6191    6259    6275    6288
                      6302    6325    6339    6352    6366    6387    6408    6424    6445    6491    6509    6523    6538
                      6564    6589    6603    6630    6745    6764    6790    6810    6829    6847    6865    6884    6938
                      6955    7003    7070    7094    7117    7132    7191    7209    7230    7266    7288    7326    7348
                      7363    7401    7425    7471    7508    7522    7565    7602    7616    7659    7683    7704    7718
                      7761    7785    7806    7820    7862    7886    7907    7921    7964    7988    8009    8023    8066
                      8090    8111    8125    8168    8192    8213    8227    8269    8293    8314    8328    8371    8395
                      8416    8430    8473    8497    8518    8532    8575    8599    8620    8634    8676    8700    8721
                      8735    8778    8802    8823    8837    8880    8904    8925    8939    8991    9043    9057    9089
                      9104    9163    9184    9197    9231    9247    9267    9301    9319    9392    9413    9432    9453
                      9467    9485    9504    9543    9567    9608    9636    9650    9687    9747    9768    9787    9808
                      9822    9840    9859    9898    9922    9963    9991   10005   10042   10099   10121   10140   10162
                     10176   10194   10207   10222   10238   10256   10294   10341   10366   10381   10395   10423   10437
                     10453   10468   10482   10502   10543   10568   10583   10597   10624   10638   10654   10669   10683
                     10702   10753   10767   10787   10830   10850   10862   10879   10893   10918   10932   10946   10967
                     11009   11056   11066   11080   11094   11123   11146   11163   11179   11195   11221   11237   11251
                     11265   11281   11309   11326   11340   11354   11370   11399   11417   11431   11445   11461   11489
                     11507   11545   11560   11579   11593   11610   11624   11667   11676   11692   11707   11724   11738
                     11757   11771   11804   11819   11833   11849   11864   11885   11899   11936   11951   11970   11984
                     12001   12015   12058   12067   12083   12098   12115   12129   12148   12162   12195   12210   12224
                     12240   12255   12276   12290   12329   12345   12364   12378   12395   12410   12454   12463   12479
                     12494   12512   12526   12545   12559   12592   12607   12622   12638   12651   12661   12675   12732
                     12755   12777   12793   12810   12829   12844   12859   12874   12887   12904   12923   12937   12953
                     12968   12986   13006   13021   13036   13051   13066   13098   13111   13153   13165   13175

C$ERHR= 000056        1501#
C$ERRO= 000060        1501#
C$ERSF= 000054        1501#
C$ERSO= 000057        1501#
C$ESCA= 000010        1501#
C$ESEG= 000005        1501#   2506    2523    2553    2593    2696    2719    2841    2872    3141    3158    3190    3208
                      3237    3272    3289    3322    3340    3369    3448    3516    3551    3568    3683    4313    4362
                      4470    4577    4684    4796    4902    4976    5042    5114    5219    5293    5359    5431    5535
                      5609    5675    5747    5853    5929    5998    6072    6201    6451    6636    6961    7009    7138
                      7236    7294    7369    7431    7528    7622    7724    7826    7927    8029    8131    8233    8334
                      8436    8538    8640    8741    8843    8945    9063    9110    9203    9253    9273    9325    9438
                      9693    9793   10048   10146   10305   10508   10708   11019   11513   11905   12296   12682   13072
                     13181
C$ESUB= 000003        1501#   3734    3749    3802    3817    3870    3885    3939    3954    4007    4022    4075    4090
                      4143    4158    4211    4226    4908    5048    5120    5225    5365    5437    5541    5681    5753
                      5859    6004    6078    6689    6703    6717    6731    6890    7243    7301    7376    7438    9023
                      9069    9116
C$ETST= 000001        1501#   3112    3161    3211    3243    3292    3343    3375    3451    3519    3575    3686    3753
                      3821    3889    3958    4026    4094    4162    4230    4374    4482    4589    4696    4807    5123
                      5440    5756    6081    6204    6454    6640    6893    6965    7016    7146    7441    7535    7629
                      7731    7832    7934    8036    8138    8239    8341    8443    8545    8646    8748    8850    8952
                      9119    9355    9710   10065   10309   10511   10711   11023   11516   11908   12299   12685   13075
                     13184
C$EXIT= 000032        1501#   2983    3025   12718
C$GETB= 000026        1501#
C$GETW= 000027        1501#
C$GMAN= 000043        1501#
C$GPHR= 000042        1501#   2959
C$GPLO= 000030        1501#
```

```
C$GPRI= 000040           1501#
C$INIT= 000011           1501#   2991
C$INLP= 000020           1501#
C$MANI= 000050           1501#
C$MEM = 000031           1501#
C$MSG = 000023           1501#   2201    2224    2233    2242    2251    2260    2276    2293    2304    2316
C$OPEN= 000034           1501#
C$PNTB= 000014           1501#   2271    2300    2312    2324
C$PNTF= 000017           1501#
C$PNTS= 000016           1501#
C$PNTX= 000015           1501#   2211    2220    2288    2350    2358    2368    2376    2386    2397    2408    2416
C$QIO = 000377           1501#
C$RDBU= 000007           1501#
C$REFG= 000047           1501#   2930    2935    2940    2947    2953
C$RESE= 000033           1501#   2944   13122
C$REVI= 000003           1501#   1562
C$RFLA= 000021           1501#
C$RPT = 000025           1501#   2900
C$SEFG= 000046           1501#
C$SPRI= 000041           1501#   2979
C$SVEC= 000037           1501#   2475    2564   13128
C$TPRI= 000013           1501#
DFPTBL  002330 G         1692#
DIAGMC= 000000           1501
EF.CON= 000036 G         1770#   2952
EF.NEW= 000035 G         1771#   2946
EF.PWR= 000034 G         1772#   2939
EF.RES= 000037 G         1769#   2934
EF.STA= 000040 G         1768#   2929
EMSGR0  003704 G         2093#   2192    2206
EMSGR2  003734 G         2097#   2229
EMSGR4  003764 G         2101#   2238
EMSGR6  004014 G         2105#   2247    2256    2265    2281
ERORR0  004622 G         2204#   2520
ERRBLK  002346 G         1896#
ERRMSG  002344 G         1895#
ERRNBR  002342 G         1894#
ERRTYP  002340 G         1893#
EVL   = 000004 G         1788#
EVNTCL  003256 G         2028#   9689   10044
EVNTCT  003215 G         2022#   9545    9610    9900    9965   10832   11011   11806   12197   12594
EVNTER  005026 G         2279#   9546    9611    9690    9901    9966   10045   10297   10833   11012   11807   12198   12595
EVNTRL  003323 G         2035#  10296
EXTPER  003452 G         2052#  12795   12846   12889   12939   12970   13023   13068
EXTPRB  002366 G         1910#   2976*  12715
E$END = 002100           1501#
E$LOAD= 000035           1501#   1586
FRMTEC  004362 G         2148#   2285
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G$PRML= 000000          1501#  13225
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G$RADB= 000000          1501#
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                  13003 13033 13048  13108
LDRDR4  006204 G   2622#  7114  7129   7227  7360  10378 10580 10876 11192 11278 11367 11458 11721
                  12112 12509
LDRDR6  006252 G   2633#  2687  3425   3439  3492  3507  3559  3621  6299  6535  6935  6952  7000
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                  12095 12491
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LDRD4R  006212 G   2620  2623#
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LOT   = 000010 G   1789#
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MSGTM2  004531 G          2166#
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O$SETU= 000001          1501#   1515#   1531    13282
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PDAL1 = 000002 G        1858#   1867    1868    1871    1872    1875    1876    1879    1880
PDAL2 = 000004 G        1857#   1869    1870    1871    1872    1877    1878    1879    1880
PDAL3 = 000010 G        1856#   1873    1874    1875    1876    1877    1878    1879    1880
PDAL4 = 000020 G        1852#   12949   12982   13002   13032   13047
PDAL5 = 000040 G        1851#   10391   10433   10464   10593   10634   10665   10889   10928   11090   11159   11217   11247
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PDAL6 = 000100 G        1850#   6112    6271    6284    6420    6505    6519    6760
PDAL7 = 000200 G        1849#   9463    9632    9646    9818    9987    10001   10190   10203
PNT   = 001000 G        1795#
PRI   = 002000 G        1796#
PRI00 = 000000 G        1784#
PRI01 = 000040 G        1783#
PRI02 = 000100 G        1782#
PRI03 = 000140 G        1781#
PRI04 = 000200 G        1780#
PRI05 = 000240 G        1779#
PRI06 = 000300 G        1778#
PRI07 = 000340 G        1556    1777#   2471    2560    2978    13124
PRNTAL  005152 G        2239    2257    2290    2331#
PRNTBS  005132 G        2191    2205    2228    2237    2246    2255    2264    2280    2320#
PRNTR0  005212 G        2193    2331    2339    2346#
PRNTR2  005264 G        2230    2332    2340    2364#
PRNTR4  005336 G        2333    2382#
PRNTR6  005424 G        2334    2341    2404#
PR026R  005174 G        2248    2273    2339#
PTER0 = 000000 G        1865#   6112    6271    6505    7492    9035    9082    9146    9409    9500    9563    9632    9764
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                        12448
PTER1 = 000001 G        1866#   4249    4325    4950    5088    6820    7586
PTER10= 000012 G        1875#   8493    12251   12762   12855   13032
PTER11= 000013 G        1876#   8595    11871
PTER12= 000014 G        1877#   8696    12262
PTER13= 000015 G        1878#   8798    9494    9849    10185   10775   11568   11959   12353
PTER14= 000016 G        1879#   8900
PTER15= 000017 G        1880#   6926    6991    7081    7201    9065    9112    9523    9586    9670    9878    9941    10025
                        10275   10352   10493   10554   10694   10805   10985   11159   11247   11336   11427   11684   12075
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PTER2 = 000002 G        1867#   5267    5405    6839    7679
PTER3 = 000003 G        1868#   5583    5721    6857    7781
PTER4 = 000004 G        1869#   5901    6044    6875    7882    10433   10634   11589   11829   11881   11980   12220   12272
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PTER5 = 000005 G        1870#   2810    3731    3746    3799    3814    4248    4433    4867    5005    6686    7483    7577
                        7671    7773    7984    9002    9145    9175    9222    9292    9404    9759    10111   11640   12031
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PTER6 = 000006 G        1871#   2818    3867    3882    3936    3951    4540    5184    5322    6700    7874    7976    8078
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PTER7 = 000007 G        1872#   2826    4004    4019    4072    4087    4647    5500    5638    6714    8188    8281    8383
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READR0  006120 G      2602#  13162
READR2  006144 G      2610#  13172
READR4  006220 G      2624#  7285   7345   7422   9101   9244   9316  10420  10499  10621  10699  10915  10943
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REG0EQ  004044 G      2109#  2208   2347
REG2    002352 G      1903#  2567*  2568   2609*  2610   3021*
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REG4    002354 G      1904#  2623*  2624
REG4EQ  004070 G      2113#  2383
REG6    002356 G      1905#  2633*  2634   2781*  2804   4281*  4302   4351   4438*  4458   4545*  4565   4652*
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                      5349   5421   5505*  5525   5598   5644*  5665   5737   5821*  5841   5916   5965*  5986
                      6061   9492*  9538   9603   9682   9847*  9893   9958  10037  10182*  10289  10773*  11566*
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ROTM    005066 G      2295#  2500
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R2TM    005110 G     2307#   2586
R4BAD   002412 G     1923#   2389    2625*   2626*   2627
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P4GOOD  002404 G     1920#   2390    2618*   2619*   2622*   2627    7284*   7344*   7421*   9099*   9100*   9242*   9243*
                     9314*   9315*   10419*  10498*  10914*  10942*  11752*  12143*  12540*
R4LOAD  002402 G     1919#   2393    2618    2622    2623    7112*   7128*   7226*   7283*   7343*   7358*   7359*   7420*
                     7504*   7518*   7598*   7612*   7700*   7714*   7802*   7816*   7903*   7917*   8005*   8019*   8107*
                     8121*   8209*   8223*   8310*   8324*   8412*   8426*   8514*   8528*   8616*   8630*   8717*   8731*
                     8819*   8833*   8921*   8935*   9053*   9098*   9099    9193*   9241*   9242    9255*   9256*   9311*
                     9312*   9313*   9314    9427*   9782*   10135*  10376*  10578*  10874*  11190*  11276*  11365*  11456*
                    11662*  11682*  11719*  12053*  12073*  12110*  12449*  12469*  12507*
R4MASK  002406 G     1921#   2391    2626    7113*   7177*   7456*   7550*   7644*   7746*   7847*   7949*   8051*   8153*
                     8254*   8356*   8458*   8560*   8661*   8763*   8865*   8976*   9143*   9428*   9783*   10136*  10377*
                    10418*  10579*  10620*  10875*  11191*  11277*  11366*  11457*  11663*  11720*  11753*  12054*  12111*
                    12144*  12450*  12508*  12541*
R4READ  002410 G     1922#   2392    2624*   2625
R6BAD   002422 G     1928#   2635*
R6LOAD  002414 G     1925#   2412    2633    2637    2685*   2781    2808    3423*   3438*   3490*   3506*   3532*   3570*
                     3571    3619*   3647*   3729*   3744*   3797*   3812*   3865*   3880*   3934*   3949*   4002*   4017*
                     4070*   4085*   4138*   4153*   4206*   4221*   4280*   4304    4350*   4353    4431*   4459    4538*
                     4566    4645*   4673    4755*   4784*   4785    4865*   4893    4964*   4966    5002*   5003*   5033
                     5102*   5103*   5105    5182*   5210    5281*   5283    5319*   5320*   5350    5419*   5420*   5422
                     5498*   5526    5597*   5599    5635*   5636*   5666    5735*   5736*   5738    5814*   5843*   5844
                     5915*   5917*   5919    5955*   5956*   5957*   5988*   5989    6058*   6059*   6060*   6063    6155*
                     6186*   6187*   6197    6297*   6321*   6362*   6441*   6533*   6560*   6626*   6684*   6698*   6712*
                     6726*   6786*   6824*   6843*   6861*   6879*   6933*   6951*   6978*   7011*   7012    7055*   7140*
                     7141    7175*   7220    7225    7238*   7239    7256*   7277    7282    7296*   7297    7315*   7337
                     7342    7371*   7372    7391*   7412    7417    7433*   7434    7455*   7530*   7531    7549*   7624*
                     7625    7643*   7726*   7727    7745*   7828*   7846*   7929*   7930    7948*   8031*   8032    8050*
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                     8559*   8642*   8660*   8743*   8744    8762*   8845*   8846    8864*   8947*   8948    8975*   9149*
                     9205*   9212*   9275*   9282*   9327*   9334*   9402*   9532*   9535*   9540    9596*   9599*   9605
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                    11174*  11232* 11260* 11321* 11349* 11412* 11440* 11502* 11605* 11634* 11702* 11799* 11844*
                    11895*  11996* 12025* 12093* 12190* 12235* 12286* 12390* 12421* 12489* 12587* 12633* 12671*
                    12788*  12883* 12964* 13062*
R6MASK  002416 G     1926#  2590*  2636   2686*  3424*  3491*  3533*  3620*  4251*  4303   4320*  4327*  4352
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                    10650*  10826* 11002* 11119* 11142* 11175* 11233* 11261* 11322* 11350* 11413* 11441* 11503*
                    11606*  11635* 11703* 11800* 11845* 11997* 12026* 12094* 12191* 12236* 12391* 12422* 12490*
                    12588*  12634* 12789*
R6READ  002420 G     1927#  2411   2634*  2635   2636*  2637   2804*  2807*  2808   4302*  4303*  4304   4351*
                     4352*  4353   4458*  4459   4565*  4566   4672*  4673   4782*  4783*  4785   4892*  4893
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                     5422   5525*  5526   5598*  5599   5665*  5666   5737*  5738   5841*  5842*  5844   5916*
                     5918*  5919   5986*  5987*  5989   6061*  6062*  6063   9538*  9539*  9540   9603*  9604*
                     9605   9682*  9683*  9684   9893*  9894*  9895   9958*  9959*  9960   10037* 10038* 10039
                    10289*  10290* 10291
SBLERR  003420 G     2047#  11612  11851  11901  12003  12242  12292  12397  12640  12677
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                        5432*   5433    5469*   5498    5536*   5537    5554*   5597    5635    5676*   5677    5692*   5735
                        5748*   5749    5785*   5814    5854*   5855    5872*   5915    5955    5999*   6000    6015*   6058
                        6073*   6074    6754*
TRAMER  004766 G        2263#   4467    4574    4681    4793    4899    4972    5039    5111    5216    5289    5356    5428
                        5532    5605    5672    5744    5850    5925    5995    6069    6832    6850    6868    6887
TRAM15  003000 G        1997#   4466    4898    4971    5038    5110    6831
TRAM31  003034 G        2002#   4573    5215    5288    5355    5427    6849
TRAM47  003071 G        2007#   4680    5531    5604    5671    5743    6867
TRAM55  003126 G        2012#   4792    5849    5924    5994    6068    6886
TRANST  006642 G        2850#   6181    6317    6378    6398    6434    6555    6580    6620    6781    9518    9581    9665
                        9873    9936   10020   10270   10412   10614   10814   10909   10994   11111   11134   11211   11299
                       11389   11479   11793   12184   12581
TRDIBF  006430 G        2757#   3730    3745    3798    3813    3866    3881    3935    3950    4003    4018    4071    4086
                        4139    4154    4207    4222    4432    4539    4646    4756    4866    5004    5183    5321    5499
                        5637    5815    5958    6685    6699    6713    6727    7482    7576    7670    7772    7873    7975
                        8077    8179    8280    8382    8484    8586    8687    8789    8891    9001    9007    9013    9019
                        9174    9221    9291    9403    9758   10110   11639   11644   11649   11654   12030   12035   12040
                       12045   12426   12431   12436   12441
TRDIER  002710 G        1987#   4309
TRDISE  002745 G        1992#   4358
TRDI15  002521 G        1967#   2815
TRDI31  002556 G        1972#   2823
TRDI47  002614 G        1977#   2831
TRDI59  002652 G        1982#   2837
T$ARGC= 000003          1519#   1520#   1521#   1522#   1523#   1524#   2208#   2212    2214#   2221    2267#   2272    2283#
                        2289    2297#   2301    2309#   2313    2321#   2325    2347#   2351    2353#   2359    2365#   2369
                        2371#   2377    2383#   2387    2389#   2398    2405#   2409    2411#   2417
T$CODE= 002130         13214#  13219#  13225#
T$ERRN= 000002          1501#   2488#   2498#   2518#   2538#   2548#   2574#   2584#   2672#   2691#   2714#   2769#   2792#
                        2814#   2822#   2830#   2836#   2857#   2867#   3136#   3153#   3185#   3203#   3232#   3267#   3284#
                        3317#   3335#   3364#   3411#   3429#   3443#   3477#   3496#   3511#   3546#   3563#   3602#   3613#
                        3625#   3638#   3652#   3665#   3678#   4269#   4291#   4308#   4339#   4357#   4418#   4450#   4465#
                        4525#   4557#   4572#   4632#   4664#   4679#   4742#   4774#   4791#   4849#   4883#   4897#   4935#
                        4955#   4970#   4992#   5023#   5037#   5074#   5093#   5109#   5166#   5200#   5214#   5252#   5272#
                        5287#   5309#   5340#   5354#   5391#   5410#   5426#   5482#   5516#   5530#   5568#   5588#   5603#
                        5625#   5656#   5670#   5707#   5726#   5742#   5798#   5832#   5848#   5886#   5906#   5923#   5945#
                        5977#   5993#   6030#   6049#   6067#   6117#   6133#   6146#   6161#   6192#   6260#   6276#   6289#
                        6303#   6326#   6340#   6353#   6367#   6388#   6409#   6425#   6446#   6492#   6510#   6524#   6539#
                        6565#   6590#   6604#   6631#   6746#   6765#   6791#   6811#   6830#   6848#   6866#   6885#   6939#
                        6956#   7004#   7071#   7095#   7118#   7133#   7192#   7210#   7231#   7267#   7289#   7327#   7349#
                        7364#   7402#   7426#   7472#   7509#   7523#   7566#   7603#   7617#   7660#   7684#   7705#   7719#
                        7762#   7786#   7807#   7821#   7863#   7887#   7908#   7922#   7965#   7989#   8010#   8024#   8067#
                        8091#   8112#   8126#   8169#   8193#   8214#   8228#   8270#   8294#   8315#   8329#   8372#   8396#
                        8417#   8431#   8474#   8498#   8519#   8533#   8576#   8600#   8621#   8635#   8677#   8701#   8722#
                        8736#   8779#   8803#   8824#   8838#   8881#   8905#   8926#   8940#   8992#   9044#   9058#   9090#
                        9105#   9164#   9185#   9198#   9232#   9248#   9268#   9302#   9320#   9393#   9414#   9433#   9454#
                        9468#   9486#   9505#   9544#   9568#   9609#   9637#   9651#   9688#   9748#   9769#   9788#   9809#
                        9823#   9841#   9860#   9899#   9923#   9964#   9992#  10006#  10043#  10100#  10122#  10141#  10163#
                       10177#  10195#  10208#  10223#  10239#  10257#  10295#  10342#  10367#  10382#  10396#  10424#  10438#
```

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                    10454#  10469#  10483#  10503#  10544#  10569#  10584#  10598#  10625#  10639#  10655#  10670#  10684#
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                    11010#  11057#  11067#  11081#  11095#  11124#  11147#  11164#  11180#  11196#  11222#  11238#  11252#
                    11266#  11282#  11310#  11327#  11341#  11355#  11371#  11400#  11418#  11432#  11446#  11462#  11490#
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                    11758#  11772#  11805#  11820#  11834#  11850#  11865#  11886#  11900#  11937#  11952#  11971#  11985#
                    12002#  12016#  12059#  12068#  12084#  12099#  12116#  12130#  12149#  12163#  12196#  12211#  12225#
                    12241#  12256#  12277#  12291#  12330#  12346#  12365#  12379#  12396#  12411#  12455#  12464#  12480#
                    12495#  12513#  12527#  12546#  12560#  12593#  12608#  12623#  12639#  12652#  12662#  12676#  12733#
                    12756#  12778#  12794#  12811#  12830#  12845#  12860#  12875#  12888#  12905#  12924#  12938#  12954#
                    12969#  12987#  13007#  13022#  13037#  13052#  13067#  13099#  13112#  13154#  13166#  13176#
T$EXCP= 000000      13214#  13218   13219#  13224
T$FLAG= 000040       2892#   2894    2983#  3025.#  3047#  3049    3070#  3072    12718#
T$FREE= 037756      13282   13301#
T$GMAN= 000000       1501#
T$HILI= 000017      13214#  13217   13219#  13223
T$LAST= 000001       1501#  13282#  13291
T$LOLI= 000000      13214#  13216   13219#  13222
T$LSYM= 010000       1501#   1701    1719    2201    2224    2233    2242    2251    2260    2276    2293    2304    2316
                     2900    2991    3008    3033    3055    3078    3112    3161    3211    3243    3292    3343    3375
                     3451    3519    3575    3686    3734    3749    3753    3802    3817    3821    3870    3885    3889
                     3939    3954    3958    4007    4022    4026    4075    4090    4094    4143    4158    4162    4211
                     4226    4230    4374    4482    4589    4696    4807    4908    5048    5120    5123    5225    5365
                     5437    5440    5541    5681    5753    5756    5859    6004    6078    6081    6204    6454    6640
                     6689    6703    6717    6731    6890    6893    6965    7016    7146    7243    7301    7376    7438
                     7441    7535    7629    7731    7832    7934    8036    8138    8239    8341    8443    8545    8646
                     8748    8850    8952    9023    9069    9116    9119    9355    9710   10065   10309   10511   10711
                    11023   11516   11908   12299   12685   13075   13184   13234   13273
T$LTNO= 000101      13285#
T$NEST= 177777       1501#   1508#   1690#   1700#   1712#   1718#   1721#   1726#   2190#   2200#   2204#   2223#   2227#
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                     2307#   2315#   2469#   2505#   2511#   2522#   2531#   2552#   2558#   2592#   2661#   2695#   2709#
                     2718#   2758#   2840#   2851#   2871#   2876#   2881#   2888#   2899#   2910#   2917#   2927#   2990#
                     3003#   3007#   3018#   3032#   3043#   3054#   3066#   3077#   3081#   3087#   3105#   3111#   3124#
                     3127#   3140#   3144#   3157#   3160#   3172#   3175#   3189#   3193#   3207#   3210#   3222#   3227#
                     3236#   3242#   3255#   3258#   3271#   3275#   3288#   3291#   3304#   3307#   3321#   3325#   3339#
                     3342#   3355#   3359#   3368#   3374#   3398#   3401#   3447#   3450#   3464#   3467#   3515#   3518#
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                     3884#   3888#   3920#   3924#   3938#   3944#   3953#   3957#   3988#   3992#   4006#   4012#   4021#
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                     4192#   4196#   4210#   4216#   4225#   4229#   4246#   4254#   4312#   4330#   4361#   4373#   4402#
                     4407#   4469#   4481#   4509#   4514#   4576#   4588#   4616#   4621#   4683#   4695#   4726#   4731#
                     4795#   4806#   4826#   4835#   4838#   4901#   4907#   4920#   4924#   4975#   4982#   5041#   5047#
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                     5299#   5358#   5364#   5375#   5379#   5430#   5436#   5439#   5459#   5468#   5471#   5534#   5540#
                     5553#   5557#   5608#   5615#   5674#   5680#   5691#   5695#   5746#   5752#   5755#   5775#   5784#
                     5787#   5852#   5858#   5871#   5875#   5928#   5935#   5997#   6003#   6014#   6018#   6071#   6077#
                     6080#   6099#   6103#   6200#   6203#   6247#   6250#   6450#   6453#   6477#   6481#   6635#   6639#
                     6675#   6679#   6688#   6693#   6702#   6707#   6716#   6721#   6730#   6735#   6889#   6892#   6914#
                     6917#   6960#   6964#   6976#   6985#   7008#   7015#   7054#   7059#   7137#   7145#   7169#   7173#
                     7180#   7235#   7242#   7250#   7259#   7293#   7300#   7309#   7318#   7368#   7375#   7385#   7394#
                     7430#   7437#   7440#   7454#   7459#   7527#   7534#   7548#   7553#   7621#   7628#   7642#   7647#
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                     8354#   8359#   8435#   8442#   8456#   8461#   8537#   8544#   8558#   8563#   8639#   8645#   8659#
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                   10330#  10507#  10510#  10529#  10532#  10707#  10710#  10740#  10743#  11018#  11022#  11042#  11045#
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                   12684#  12714#  12721#  13071#  13074#  13087#  13089#  13180#  13183#  13186#  13191#  13202#  13232#
                   13264#  13271#  13286#
T$NS0 = 000000      1508#  1721   1726#  2876   2881#  3081   3087#  13186  13191#  13286
T$NS1 = 000005      1690#  1700   1712#  1718   2190#  2200   2204#  2223   2227#  2232   2236#  2241   2245#
                    2250   2254#  2259   2263#  2275   2279#  2292   2295#  2303   2307#  2315   2469#  2505
                    2511#  2522   2531#  2552   2556#  2592   2661#  2695   2709#  2718   2758#  2840   2851#
                    2871   2888#  2899   2910#  2917   2927#  2990   3003#  3007   3018#  3032   3043#  3054
                    3066#  3077   3105#  3111   3124#  3160   3172#  3210   3222#  3242   3255#  3291   3304#
                    3342   3355#  3374   3398#  3450   3464#  3518   3531#  3574   3591#  3685   3715#  3752
                    3783#  3820   3851#  3888   3920#  3957   3988#  4025   4056#  4093   4124#  4161   4192#
                    4229   4246#  4373   4402#  4481   4509#  4588   4616#  4695   4726#  4806   4826#  5122
                    5143#  5439   5459#  5755   5775#  6080   6099#  6203   6247#  6453   6477#  6639   6675#
                    6892   6914#  6964   6976#  7015   7054#  7145   7169#  7440   7454#  7534   7548#  7628
                    7642#  7730   7744#  7831   7845#  7933   7947#  8035   8049#  8137   8151#  8238   8252#
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                    8974#  9118   9141#  9354   9377#  9709   9732#  10064  10084#  10308  10327#  10510  10529#
                   10710  10740#  11022  11042#  11515  11534#  11907  11925#  12298  12317#  12684  12714#  13074
                   13087#  13183  13202#  13232  13264#  13271
T$NS2 = 000003      3127#  3140   3144#  3157   3175#  3189   3193#  3207   3227#  3236   3258#  3271   3275#
                    3288   3307#  3321   3325#  3339   3359#  3368   3401#  3447   3467#  3515   3536#  3550
                    3554#  3567   3593#  3682   3719#  3733   3739#  3748   3787#  3801   3807#  3816   3855#
                    3869   3875#  3884   3924#  3938   3944#  3953   3992#  4006   4012#  4021   4060#  4074
                    4080#  4089   4128#  4142   4148#  4157   4196#  4210   4216#  4225   4254#  4312   4330#
                    4361   4407#  4469   4514#  4576   4621#  4683   4731#  4795   4835#  4907   4920#  5047
                    5058#  5119   5152#  5224   5237#  5364   5375#  5436   5468#  5540   5553#  5680   5691#
                    5752   5784#  5858   5871#  6003   6014#  6077   6103#  6200   6250#  6450   6481#  6635
                    6679#  6688   6693#  6702   6707#  6716   6721#  6730   6735#  6889   6917#  6960   6985#
                    7008   7059#  7137   7173#  7242   7250#  7300   7309#  7375   7385#  7437   7459#  7527
                    7553#  7621   7647#  7723   7749#  7825   7850#  7926   7952#  8028   8054#  8130   8156#
                    8232   8257#  8333   8359#  8435   8461#  8537   8563#  8639   8664#  8740   8766#  8842
                    8868#  8944   8980#  9022   9027#  9068   9073#  9115   9152#  9202   9215#  9252   9259#
                    9272   9285#  9324   9380#  9437   9443#  9692   9735#  9792   9798#  10047  10087#  10145
                   10149#  10304  10330#  10507  10532#  10707  10743#  11018  11045#  11512  11536#  11904  11927#
                   12295  12320#  12681  12721#  13071  13089#  13180
T$NS3 = 000003      4838#  4901   4924#  4975   4982#  5041   5062#  5113   5155#  5218   5241#  5292   5299#
                    5358   5379#  5430   5471#  5534   5557#  5608   5615#  5674   5695#  5746   5787#  5852
                    5875#  5928   5935#  5997   6018#  6071   7180#  7235   7259#  7293   7318#  7368   7394#
                    7430   9038#  9062   9084#  9109
T$PCNT= 000000     13291#  13292#
T$PTAB= 010177     13292#  13295
T$PTHV= 000001      1532   13301#
T$PTNU= 000001      1501#  13295#  13301
T$SAVL= 177777      1501#
T$SEGL= 177777      1501#  2469#  2505#  2507   2511#  2522#  2524   2531#  2552#  2554   2558#  2592#  2594
                    2661#  2695#  2697   2709#  2718#  2720   2758#  2840#  2842   2851#  2871#  2873   3127#
                    3140#  3142   3144#  3157#  3159   3175#  3189#  3191   3193#  3207#  3209   3227#  3236#
                    3238   3258#  3271#  3273   3275#  3288#  3290   3307#  3321#  3323   3325#  3359#  3341
                    3359#  3368#  3370   3401#  3447#  3449   3467#  3515#  3517   3536#  3550#  3552   3554#
                    3567#  3569   3593#  3682#  3684   4254#  4312#  4314   4330#  4361#  4363   4407#  4469#
                    4471   4514#  4576#  4578   4621#  4683#  4685   4731#  4795#  4797   4838#  4901#  4903
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                    4924#  4975#  4977   4982#  5041#  5043   5062#  5113#  5115   5155#  5218#  5220   5241#
                    5292#  5294   5299#  5358#  5360   5379#  5430#  5432   5471#  5534#  5536   5557#  5608#
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                    5935#  5997#  5999   6018#  6071#  6073   6103#  6200#  6202   6250#  6450#  6452   6481#
                    6635#  6637   6917#  6960#  6962   6985#  7008#  7010   7059#  7137#  7139   7180#  7235#
                    7237   7259#  7293#  7295   7318#  7368#  7370   7394#  7430#  7432   7459#  7527#  7529
                    7553#  7621#  7623   7647#  7723#  7725   7749#  7825#  7827   7850#  7926#  7928   7952#
                    8028#  8030   8054#  8130#  8132   8156#  8232#  8234   8257#  8333#  8335   8359#  8435#
                    8437   8461#  8537#  8539   8563#  8639#  8641   8664#  8740#  8742   8766#  8842#  8844
                    8868#  8944#  8946   9038#  9062#  9064   9084#  9109#  9111   9152#  9202#  9204   9215#
                    9252#  9254   9259#  9272#  9274   9285#  9324#  9326   9380#  9437#  9439   9443#  9692#
                    9694   9735#  9792#  9794   9798#  10047#  10049  10087#  10145#  10147  10149#  10304#  10306
                   10330#  10507#  10509  10532#  10707#  10709  10743#  11018#  11020  11045#  11512#  11514  11536#
                   11904#  11906  11927#  12295#  12297  12320#  12681#  12683  12721#  13071#  13073  13089#  13180#
                   13182
T$SEK0= 010000      2469#  2505   2511#  2522   2531#  2552   2558#  2592   2661#  2695   2709#  2718   2758#
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                    3258#  3271   3275#  3288   3307#  3321   3325#  3339   3359#  3368   3401#  3447   3467#
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T$$AUT= 010017       3003#   3007
T$$CLE= 010020       3018#   3025    3032
T$$DAT= 010200      13293#  13299
T$$DU = 010021       3043#   3047    3054
T$$HAR= 010174      13202#  13233
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T$$MSG= 010013       2190#   2200    2204#   2223    2227#   2232    2236#   2241    2245#   2250    2254#   2259    2263#
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T$$PC = 000001      13291#  13301
T$$PRO= 010015       2910#
T$$PTA= 010177      13291#  13294   13295#
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T$$SEG= 010000       2469#   2505#   2511#   2522#   2531#   2552#   2558#   2592#   2661#   2695#   2709#   2718#   2758#
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T$$SUB= 010156       3719#   3733    3739#   3748    3787#   3801    3807#   3816    3855#   3869    3875#   3884    3924#
                     3938    3944#   3953    3992#   4006    4012#   4021    4060#   4074    4080#   4089    4128#   4142
                     4148#   4157    4196#   4210    4216#   4225    4835#   4907    4920#   5047    5058#   5119    5152#
                     5224    5237#   5364    5375#   5436    5468#   5540    5553#   5680    5691#   5752    5784#   5858
                     5871#   6003    6014#   6077    6079#   6688    6693#   6702    6707#   6716    6721#   6730    6735#
                     6889    7173#   7242    7250#   7300    7309#   7375    7385#   7437    8980#   9022    9027#   9068
                     9073#   9115
T$$SW = 010001       1712#   1718
T$$TES= 010173       3105#   3111    3124#   3160    3172#   3210    3222#   3242    3255#   3291    3304#   3342    3355#
                     3374    3398#   3450    3464#   3518    3531#   3574    3591#   3685    3715#   3752    3783#   3820
                     3851#   3888    3920#   3957    3988#   4025    4056#   4093    4124#   4161    4192#   4229    4246#
                     4373    4402#   4481    4509#   4588    4616#   4695    4726#   4806    4826#   5122    5143#   5439
                     5459#   5755    5775#   6080    6099#   6203    6247#   6453    6477#   6639    6675#   6892    6914#
                     6964    6976#   7015    7054#   7145    7169#   7440    7454#   7534    7548#   7628    7642#   7730
                     7744#   7831    7845#   7933    7947#   8035    8049#   8137    8151#   8238    8252#   8340    8354#
                     8442    8456#   8544    8558#   8645    8659#   8747    8761#   8849    8863#   8951    8974#   9118
                     9141#   9354    9377#   9709    9732#  10064  10084#  10308  10327#  10510  10529#  10710  10740#
                    11022  11042#  11515  11534#  11907  11925#  12298  12317#  12684  12714#  12718  13074  13087#
                    13183
T1          007162 G  1614    3104#
```

T10	010052	G	1623	3530#
T11	010156	G	1624	3590#
T12	010404	G	1625	3714#
T12.1	010410		3718#	
T12.2	010430		3738#	
T13	010450	G	1626	3782#
T13.1	010454		3786#	
T13.2	010474		3806#	
T14	010516	G	1627	3850#
T14.1	010522		3854#	
T14.2	010542		3874#	
T15	010562	G	1628	3919#
T15.1	010566		3923#	
T15.2	010606		3943#	
T16	010630	G	1629	3987#
T16.1	010634		3991#	
T16.2	010654		4011#	
T17	010674	G	1630	4055#
T17.1	010700		4059#	
T17.2	010720		4079#	
T18	010742	G	1631	4123#
T18.1	010746		4127#	
T18.2	010766		4147#	
T19	011006	G	1632	4191#
T19.1	011012		4195#	
T19.2	011032		4215#	
T2	007170	G	1615	3123#
T20	011054	G	1633	4245#
T21	011410	G	1634	4401#
T22	011604	G	1635	4508#
T23	012000	G	1636	4615#
T24	012174	G	1637	4725#
T25	012412	G	1638	4825#
T25.1	012416		4834#	
T25.2	012574		4919#	
T25.3	013072		5057#	
T26	013244	G	1639	5142#
T26.1	013250		5151#	
T26.2	013426		5236#	
T26.3	013724		5374#	
T27	014076	G	1640	5458#
T27.1	014102		5467#	
T27.2	014260		5552#	
T27.3	014556		5690#	
T28	014730	G	1641	5774#
T28.1	014734		5783#	
T28.2	015126		5870#	
T28.3	015462		6013#	
T29	015650	G	1642	6098#
T3	007254	G	1616	3171#
T30	016060	G	1643	6246#
T31	016502	G	1644	6476#
T32	017002	G	1645	6674#
T32.1	017006		6678#	
T32.2	017026		6692#	
T32.3	017046		6706#	

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T32.4   017066          6720#
T32.5   017106          6734#
T33     017452 G        1646    6913#
T34     017552 G        1647    6975#
T35     017636 G        1648    7053#
T36     020030 G        1649    7168#
T36.1   020034          7172#
T36.2   020214          7249#
T36.3   020332          7308#
T36.4   020502          7384#
T37     020630 G        1650    7453#
T38     021002 G        1651    7547#
T39     021156 G        1652    7641#
T4      007342 G        1617    3221#
T40     021352 G        1653    7743#
T41     021540 G        1654    7844#
T42     021732 G        1655    7946#
T43     022126 G        1656    8048#
T44     022322 G        1657    8150#
T45     022510 G        1658    8251#
T46     022702 G        1659    8353#
T47     023076 G        1660    8455#
T48     023272 G        1661    8557#
T49     023460 G        1662    8658#
T5      007404 G        1618    3254#
T50     023652 G        1663    8760#
T51     024046 G        1664    8862#
T52     024242 G        1665    8973#
T52.1   024260          8979#
T52.2   024340          9026#
T52.3   024436          9072#
T53     024550 G        1666    9140#
T54     025324 G        1667    9376#
T55     026244 G        1668    9731#
T56     027164 G        1669   10083#
T57     027670 G        1670   10326#
T58     030276 G        1671   10528#
T59     030670 G        1672   10739#
T6      007470 G        1619    3303#
T60     031454 G        1673   11041#
T61     032712 G        1674   11533#
T62     034032 G        1675   11924#
T63     035152 G        1676   12316#
T64     036244 G        1677   12713#
T65     037330 G        1678   13086#
T7      007556 G        1620    3354#
T8      007620 G        1621    3397#
T9      007734 G        1622    3463#
UAM   = 000200 G        1793#
UNITNB  002362 G        1908#   2950*   2956*   2958
XSALWA= 000000          1501#
XSFALS= 000040          1501#
XSOFFS= 000400          1501#
XSTRUE= 000020          1501#
$PATCH  037720 G       13276#
.     = 037756          1505#   1944#   1955#   2086#   2176#   2893    2984    3026    3048    3071    12719   13249#  13277#
```