CDS·11 CDS11 ST ANLYZR DIAG AH-T005A-MC
CVCDBA0 FICHE 1 OF 2

CDS-11 CDS11 ST ANLYZR DIAG AH-T005A-MC
CVCDBA0 FICHE 2 OF 2

.REM &

IDENTIFICATION

PRODUCT CODE: AC-T003A-MC

PRODUCT NAME: CVCDBA0 CDS-11 ST ANLYZR DIAG

PRODUCT DATE: SEPTEMBER 1981

MAINTAINER: DIAGNOSTIC ENGINEERING

REVISION HISTORY

REVISION	DATE	REASONS
A	SEPTEMBER 1981	FIRST RELEASE

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1.0 GENERAL INFORMATION

1.1 PROGRAM ABSTRACT

THE CDS-11 STATE ANALYZER DIAGNOSTIC WILL TEST ALL THE LOGIC ON THE STATE ANALYZER MODULE EXCEPT THAT LOGIC PERTAINING TO THE SYSTEM BUS. THE DIAGNOSTIC WILL CHECK ALL THE BITS IN CONTROL REGISTER 0 AND CONTROL REGISTER 2. THE DIAGNOSTIC WILL CHECK THE TRACE RAM ADDRESS REGISTER, THE TRACE RAM DATA IN BUFFERS, THE TRACE RAM'S, THE OR ADDRESS REGISTER, THE OR ARRAY RAM'S, THE AND ARRAY RAM'S, THE EVENT COUNTER REGISTERS, THE EVENT COUNTERS AND EVENT COUNTER LOGIC, THE FUNCTION SELECT FLIP-FLOP LOGIC, THE TRACING FLIP-FLOP LOGIC, THE SBL FLIP-FLOP LOGIC AND THE EXTERNAL PROBE LOGIC.

THIS DIAGNOSTIC HAS BEEN WRITTEN FOR USE WITH THE DIAGNOSTIC RUNTIME SERVICES SOFTWARE (SUPERVISOR). THESE SERVICES PROVIDE THE INTERFACE TO THE OPERATOR AND TO THE SOFTWARE ENVIRONMENT. THIS PROGRAM CAN BE USED WITH XXDP+, ACT, APT, SLIDE AND PAPER TAPE. FOR A COMPLETE DESCRIPTION OF THE RUNTIME SERVICES, REFER TO THE XXDP+ USER'S MANUAL. THERE IS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES IN SECTION 2 OF THIS DOCUMENT.

NOTE: THIS PROGRAM WAS NOT BEEN TESTED IN THE APT ENVIRONMENT, HOWEVER, THE APT INTERFACE HAS BEEN PROVIDED IN THE DIAGNOSTIC.

1.2 SYSTEM REQUIREMENTS

1. LSI-11 OR EQUIVALENT TYPE CPU WITH Q-BUS
2. MINIMUM OF 16K WORDS OF MEMORY
3. CONSOLE TERMINAL AND CONTROLLER
4. CDS-11 BACKPLANE AND CABLES
5. STATE ANALYZER MODULE(S) (M8741)
6. MXV11 MODULE AND CDS-11 ROMS
7. STORAGE DEVICE WITH CONTROLLER (OPTIONAL)
8. XXDP+ MEDIA FOR STORAGE DEVICE (OPTIONAL)

1.3 RELATED DOCUMENTS AND STANDARDS

CHQUS? XXDP+ USER'S MANUAL (THE "?" IN CHQUS INDICATES THE REVISION LEVEL OF THE DOCUMENT. AT THE TIME THIS PROGRAM WAS WRITTEN, THE REVISION LEVEL WAS "E".

1.4 DIAGNOSTIC HIERARCY PREREQUISITES

ALL HARDWARE THAT IS SPECIFIED IN SECTION 1.2 OF THIS DOCUMENT MUST BE OPERATIONAL AND FREE OF ALL FAULTS.

IF THE EXTERNAL PROBE AND THE STATE ANALYZER EXTERNAL PROBE LOGIC ARE TO BE TESTED BY THE DIAGNOSTIC, THE OPERATOR MUST PLUG THE EXTERNAL PROBE INTO THE STATE ANALYZER AND CONNECT THE EXTERNAL PROBE LEADS 7:0 TO EVENT COUNTER REGISTER 0 SIGNAL LINES SDBL 7:0 L RESPECTIVELY. THE EXTERNAL PROBE LEAD FOR THE CLK MUST BE CONNECTED TO EVENT COUNTER 1'S SIGNAL LINE SDBL8 L.

1.5 ASSUMPTIONS

2.0 OPERATING INSTRUCTIONS

THIS SECTION CONTAINS A BRIEF DESCRIPTION OF THE RUNTIME SERVICES.
FOR DETAILED INFORMATION, REFER TO THE XXDP+ USER'S MANUAL (CHQUS).

2.1 COMMANDS

THERE ARE FLEVEN LEGAL COMMANDS FOR THE DIAGNOSTIC RUNTIME SERVICES
(SUPERVISOR). THIS SECTION LISTS THE COMMANDS AND GIVES A VERY
BRIEF DESCRIPTION OF THEM. THE XXDP+ USER'S MANUAL HAS MORE DETAILS.

COMMAND	EFFECT
START	START THE DIAGNOSTIC FROM AN INITIAL STATE
RESTART	START THE DIAGNOSTIC WITHOUT INITIALIZING
CONTINUE	CONTINUE AT TEST THAT WAS INTERRUPTED (AFTER ^C)
PROCEED	CONTINUE FROM AN ERROR HALT
EXIT	RETURN TO XXDP+ MONITOR (XXDP+ OPERATION ONLY.)
ADD	ACTIVATE A UNIT FOR TESTING (ALL UNITS ARE CONSIDERED TO BE ACTIVE AT START TIME
DROP	DEACTIVATE A UNIT
PRINT	PRINT STATISTICAL INFORMATION (IF IMPLEMENTED BY THE DIAGNOSTIC - SECTION 4.0)
DISPLAY	TYPE A LIST OF ALL DEVICE INFORMATION
FLAGS	TYPE THE STATE OF ALL FLAGS (SEE SECTION 2.3)
ZFLAGS	CLEAR ALL FLAGS (SEE SECTION 2.3)

A COMMAND CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. SO
YOU MAY, FOR EXAMPLE, TYPE "STA" INSTEAD OF "START".

2.2 SWITCHES

THERE ARE SEVERAL SWITCHES WHICH ARE USED TO MODIFY SUPERVISOR OPERATION.
THESE SWITCHES ARE APPENDED TO THE LEGAL COMMANDS. ALL OF THE LEGAL
SWITCHES ARE TABULATED BELOW WITH A BRIEF DESCRIPTION OF EACH.
IN THE DESCRIPTIONS BELOW, A DECIMAL NUMBER IS DESIGNATED BY "DDDDD".

SWITCH	EFFECT
/TESTS:LIST	EXECUTE ONLY THOSE TESTS SPECIFIED IN THE LIST. LIST IS A STRING OF TEST NUMBERS, FOR EXAMPLE - /TESTS:1:5:7-10. THIS LIST WILL CAUSE TESTS 1,5,7,8,9,10 TO BE RUN. ALL OTHER TESTS WILL NOT BE RUN.
/PASS:DDDDD	EXECUTE DDDDD PASSES (DDDDD = 1 TO 64000)
/FLAGS:FLGS	SET SPECIFIED FLAGS. FLAGS ARE DESCRIBED IN SECTION 2.3.
/EOP:DDDDD	REPORT END OF PASS MESSAGE AFTER EVERY DDDDD PASSES ONLY. (DDDDD = 1 TO 64000)
/UNITS:LIST	TEST/ADD/DROP ONLY THOSE UNITS SPECIFIED IN THE LIST. LIST EXAMPLE - /UNITS:0:5:10-12 USE UNITS 0,5,10,11,12 (UNIT NUMBERS = 0-63)

EXAMPLE OF SWITCH USAGE:

START/TESTS:1-5/PASS:1000/EOP:100

THE EFFECT OF THIS COMMAND WILL BE: 1) TESTS 1 THROUGH 5 WILL BE EXECUTED, 2) ALL UNITS WILL BE TESTED 1000 TIMES AND 3) THE END OF PASS MESSAGES WILL BE PRINTED AFTER EACH 100 PASSES ONLY. A SWITCH CAN BE RECOGNIZED BY THE FIRST THREE CHARACTERS. YOU MAY, FOR EXAMPLE, TYPE "/TES:1-5" INSTEAD OF "/TESTS:1-5".

BELOW IS A TABLE THAT SPECIFIES WHICH SWITCHES CAN BE USED BY EACH COMMAND.

	TESTS	PASS	FLAGS	EOP	UNITS
START	X	X	X	X	X
RESTART	X	X	X	X	X
CONTINUE		X	X	X	
PROCEED			X		
DROP					X
ADD					X
PRINT					
DISPLAY					X
FLAGS					
ZFLAGS					
EXIT					

2.3 FLAGS

FLAGS ARE USED TO SET UP CERTAIN OPERATIONAL PARAMETERS SUCH AS LOOPING ON ERROR. ALL FLAGS ARE CLEARED AT STARTUP AND REMAIN CLEARED UNTIL EXPLICITLY SET USING THE FLAGS SWITCH. FLAGS ARE ALSO CLEARED AFTER A START COMMAND UNLESS SET USING THE FLAG SWITCH. THE ZFLAGS COMMAND MAY ALSO BE USED TO CLEAR ALL FLAGS. WITH THE EXCEPTION OF THE START AND ZFLAGS COMMANDS, NO COMMANDS AFFECT THE STATE OF THE FLAGS; THEY REMAIN SET OR CLEARED AS SPECIFIED BY THE LAST FLAG SWITCH.

FLAG	EFFECT
HOE	HALT ON ERROR - CONTROL IS RETURNED TO RUNTIME SERVICES COMMAND MODE
LOE	LOOP ON ERROR
IER*	INHIBIT ALL ERROR REPORTS
IBE*	INHIBIT ALL ERROR REPORTS EXCEPT FIRST LEVEL (FIRST LEVEL CONTAINS ERROR TYPE, NUMBER, PC, TEST AND UNIT)
IXE*	INHIBIT EXTENDED ERROR REPORTS (THOSE CALLED BY PRINTX MACRO'S)
PRI	DIRECT MESSAGES TO LINE PRINTER
PNT	PRINT TEST NUMBER AS TEST EXECUTES
BOE	"BELL" ON ERROR
UAM	UNATTENDED MODE (NO MANUAL INTERVENTION)
ISR	INHIBIT STATISTICAL REPORTS (DOES NOT APPLY TO DIAGNOSTICS WHICH DO NOT SUPPORT STATISTICAL REPORTING)

IDR	INHIBIT PROGRAM DROPPING OF UNITS
ADR	EXECUTE AUTODROP CODE
LOT	LOOP ON TEST
EVL	EXECUTE EVALUATION (ON DIAGNOSTICS WHICH HAVE EVALUATION SUPPORT)

*ERROR MESSAGES ARE DESCRIBED IN SECTION 3.1

SEE THE XXDP+ USER'S MANUAL FOR MORE DETAILS ON FLAGS. YOU MAY SPECIFY MORE THAN ONE FLAG WITH THE FLAG SWITCH. FOR EXAMPLE, TO CAUSE THE PROGRAM TO LOOP ON ERROR, INHIBIT ERROR REPORTS AND TYPE A "BELL" ON ERROR, YOU MAY USE THE FOLLOWING STRING:

```
/FLAGS:LOE:IER:BOE
```

2.4 HARDWARE QUESTIONS

WHEN A DIAGNOSTIC IS STARTED, THE RUNTIME SERVICES WILL PROMPT THE USER FOR HARDWARE INFORMATION BY TYPING "CHANGE HW (L) ?" YOU MUST ANSWER "Y" AFTER A START COMMAND UNLESS THE HARDWARE INFORMATION HAS BEEN "PRELOADED" USING THE SETUP UTILITY (SEE CHAPTER 6 OF THE XXDP+ USER'S MANUAL). WHEN YOU ANSWER THIS QUESTION WITH A "Y", THE RUNTIME SERVICES WILL ASK FOR THE NUMBER OF UNITS (IN DECIMAL). YOU WILL THEN BE ASKED THE FOLLOWING QUESTIONS FOR EACH UNIT.

```
CSR ADDRESS:
DEVICE NUMBER:
EXTERNAL PROBE CONNECTED:
```

NOTE: IF THE EXTERNAL PROBE AND THE STATE ANALYZER'S EXTERNAL PROBE LOGIC IS TO BE TESTED, REFER TO SECTION 1.4 OF THIS DOCUMENT FOR THE EXTERNAL PROBE CONNECTIONS.

2.5 SOFTWARE QUESTIONS

AFTER YOU HAVE ANSWERED THE HARDWARE QUESTIONS OR AFTER A RESTART OR CONTINUE COMMAND, THE RUNTIME SERVICES WILL ASK FOR SOFTWARE PARAMETERS. THESE PARAMETERS WILL GOVERN SOME DIAGNOSTIC SPECIFIC OPERATION MODES. YOU WILL BE PROMPTED BY "CHANGE SW (L) ?" IF YOU WISH TO CHANGE ANY PARAMETERS, ANSWER BY TYPING "Y". THE SOFTWARE QUESTIONS AND THE DEFAULT VALUES ARE DESCRIBED IN THE NEXT PARAGRAPH(S).

THERE ARE NO SOFTWARE QUESTIONS IN THIS PROGRAM.

2.6 EXTENDED P-TABLE DIALOGUE

WHEN YOU ANSWER THE HARDWARE QUESTIONS, YOU ARE BUILDING ENTRIES IN A TABLE THAT DESCRIBES THE DEVICES UNDER TEST. THE SIMPLEST WAY TO BUILD THIS TABLE IS TO ANSWER ALL QUESTIONS FOR EACH UNIT TO BE TESTED. IF YOU HAVE A MULTIPLEXED DEVICE SUCH AS

A MASS STORAGE CONTROLLER WITH SEVERAL DRIVES OR A COMMUNICATION DEVICE WITH SEVERAL LINES, THIS BECOMES TEDIOUS SINCE MOST OF THE ANSWERS ARE REPETITIOUS.

TO ILLUSTRATE A MORE EFFICIENT METHOD, SUPPOSE YOU ARE TESTING A FICTIONAL DEVICE, THE XY11. SUPPOSE THIS DEVICE CONSISTS OF A CONTROL MODULE WITH EIGHT UNITS (SUB-DEVICES) ATTACHED TO IT. THESE UNITS ARE DESCRIBED BY THE OCTAL NUMBERS 0 THROUGH 7. THERE IS ONE HARDWARE PARAMETER THAT CAN VARY AMONG UNITS CALLED THE Q-FACTOR. THIS Q-FACTOR MAY BE 0 OR 1. BELOW IS A SIMPLE WAY TO BUILD A TABLE FOR ONE XY11 WITH EIGHT UNITS.

```
# UNITS (D) ?  8<CR>

UNIT 1
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  0<CR>
Q-FACTOR (O) 0 ?  1<CR>

UNIT 2
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  1<CR>
Q-FACTOR (O) 1 ?  0<CR>

UNIT 3
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  2<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 4
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  3<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 5
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  4<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 6
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  5<CR>
Q-FACTOR (O) 0 ?  <CR>

UNIT 7
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  6<CR>
Q-FACTOR (O) 0 ?  1<CR>

UNIT 8
CSR ADDRESS (O)  160000<CR>
SUB-DEVICE # (O) ?  7<CR>
Q-FACTOR (O) 1 ?  <CR>
```

NOTICE THAT THE DEFAULT VALUE FOR THE Q-FACTOR CHANGES WHEN A NON-DEFAULT RESPONSE IS GIVEN. BE CAREFUL WHEN SPECIFYING

MULTIPLE UNITS.

AS YOU CAN SEE FROM THE ABOVE EXAMPLE, THE HARDWARE PARAMETERS
DO NOT VARY SIGNIFICANTLY FROM UNIT TO UNIT. THE PROCEDURE SHOWN IS
NOT VERY EFFICIENT.

THE RUNTIME SERVICES CAN TAKE MULTIPLE UNIT SPECIFICATIONS HOWEVER.
LET'S BUILD THE SAME TABLE USING THE MULTIPLE SPECIFICATION
FEATURE.

```
# UNITS (D) ?  8<CR>

UNIT 1
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  0,1<CR>
Q-FACTOR (O) 0 ?  1,0<CR>

UNIT 3
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  2-5<CR>
Q-FACTOR (O) 0 ?  0<CR>

UNIT 7
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  6,7<CR>
Q FACTOR (O) 0 ?  1<CR>
```

AS YOU CAN SEE IN THE ABOVE DIALOGUE, THE RUNTIME SERVICES WILL
BUILD AS MANY ENTRIES AS IT CAN WITH THE INFORMATION GIVEN IN ANY
ONE PASS THROUGH THE QUESTIONS. IN THE FIRST PASS, TWO ENTRIES
ARE BUILT SINCE TWO SUB-DEVICES AND Q-FACTORS WERE SPECIFIED. THE
SERVICES ASSUME THAT THE CSR ADDRESS IS 160000 FOR BOTH SINCE IT
WAS SPECIFIED ONLY ONCE. IN THE SECOND PASS, FOUR ENTRIES WERE
BUILT. THIS IS BECAUSE FOUR SUB-DEVICES WERE SPECIFIED. THE
"-" CONSTRUCT TELLS THE RUNTIME SERVICES TO INCREMENT THE DATA
FROM THE FIRST NUMBER TO THE SECOND. IN THIS CASE, SUB-DEVICES
2, 3, 4 AND 5 WERE SPECIFIED. (IF THE SUB-DEVICE WERE SPECIFIED
BY ADDRESSES, THE INCREMENT WOULD BE BY 2 SINCE ADDRESSES MUST
BE ON AN EVEN BOUNDARY.) THE CSR ADDRESSES AND Q-FACTORS FOR
THE FOUR ENTRIES ARE ASSUMED TO BE 160000 AND 0 RESPECTIVELY
SINCE THEY WERE ONLY SPECIFIED ONCE. THE LAST TWO UNITS ARE
SPECIFIED IN THE THIRD PASS.

THE WHOLE PROCESS COULD HAVE BEEN ACCOMPLISHED IN ONE PASS AS
SHOWN BELOW.

```
# UNITS (D) ?  8<CR>

UNIT 1
CSR ADDRESS (O) ?  160000<CR>
SUB-DEVICE # (O) ?  0-7<CR>
Q-FACTOR (O) 0 ?  0,1,0,,,,1,1<CR>
```

AS YOU CAN SEE FROM THIS EXAMPLE, NULL REPLIES (COMMAS ENCLOSING
A NULL FIELD) TELL THE RUNTIME SERVICES TO REPEAT THE LAST REPLY.

2.7 QUICK START-UP PROCEDURE (XXDP+)

TO START-UP THIS PROGRAM:

1. BOOT XXDP+
2. ANSWER ANY QUESTIONS ASKED AND GIVE THE DATE.
3. TYPE "R NAME", WHERE NAME IS THE NAME OF THE BIN OR BIC FILE FOR THIS PROGRAM
4. TYPE "START"
5. ANSWER THE "CHANGE HW" QUESTION WITH "Y"
6. ANSWER ALL THE HARDWARE QUESTIONS
7. ANSWER THE "CHANGE SW" QUESTION WITH "N"

WHEN YOU FOLLOW THIS PROCEDURE YOU WILL BE USING ONLY THE DEFAULTS FOR FLAGS AND SOFTWARE PARAMETERS. THESE DEFAULTS ARE DESCRIBED IN SECTIONS 2.3 AND 2.5.

3.0 ERROR INFORMATION

3.1 TYPES OF ERROR MESSAGES

THERE ARE THREE LEVELS OF ERROR MESSAGES THAT MAY BE ISSUED BY A DIAGNOSTIC: GENERAL, BASIC AND EXTENDED. GENERAL ERROR MESSAGES ARE ALWAYS PRINTED UNLESS THE "IER" FLAG IS SET (SECTION 2.3). THE GENERAL ERROR MESSAGE IS OF THE FORM:

```
NAME  TYPE  NUMBER  ON UNIT NUMBER  TST NUMBER PC:XXXXXX
ERROR MESSAGE
```

WHERE: NAME = DIAGNOSTIC NAME
TYPE = ERROR TYPE (SYS FATAL, DEV FATAL, HARD OR SOFT)
NUMBER - ERROR NUMBER
UNIT NUMBER = 0 - N (N IS LAST UNIT IN PTABLE)
TST NUMBER = TEST AND SUBTEST WHERE ERROR OCCURRED
PC:XXXXXX = ADDRESS OF ERROR MESSAGE CALL

BASIC ERROR MESSAGES ARE MESSAGES THAT CONTAIN SOME ADDITIONAL INFORMATION ABOUT THE ERROR. THESE ARE ALWAYS PRINTED UNLESS THE "IER" OR "IBE" FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL MESSAGE.

EXTENDED ERROR MESSAGES CONTAIN SUPPLEMENTARY ERROR INFORMATION SUCH AS REGISTER CONTENTS OR GOOD/BAD DATA. THESE ARE ALWAYS PRINTED UNLESS THE "IER", "IBE" OR "IXE" FLAGS ARE SET (SECTION 2.3). THESE MESSAGES ARE PRINTED AFTER THE ASSOCIATED GENERAL ERROR MESSAGE AND ANY ASSOCIATED BASIC ERROR MESSAGES.

3.2 SPECIFIC ERROR MESSAGES

THE ERROR PRINTOUTS WILL USE THE FOLLOWING WORDS TO INDICATE ERROR

INFORMATION. A DESCRIPTION OF THE WORDS PRINTED OUT ARE AS FOLLOWS:

REG:	ONE OF THE STATE ANALYZER MODULE'S CONTROL REGISTERS
LOAD:	DATA THAT WAS LOADED INTO THE CONTROL REGISTER OR EXPECTED DATA TO BE IN CONTROL REGISTER ON A READ
READ:	DATA THAT WAS READ FROM THE CONTROL REGISTER
MASK:	BITS IN THE CONTROL REGISTER THAT ARE NOT CHECKED
GOOD:	EXPECTED CONTROL REGISTER DATA
BAD:	DATA "READ" FROM THE CONTROL REGISTER WITH THE "MASK" BITS CLEARED
XXXXXX:	SIX OCTAL DIGITS INDICATING THE DATA FOR THE ABOVE WORDS

THERE ARE FOUR ERROR NUMBERS ASSOCIATED WITH THIS DIAGNOSTIC. THE ERROR NUMBERS AND THEIR MEANINGS ARE DESCRIBED BELOW:

ERROR NUMBER 1 - ERROR DETECTED CHECKING CONTROL REGISTER 0
ERROR NUMBER 2 - ERROR DETECTED CHECKING CONTROL REGISTER 2
ERROR NUMBER 3 - ERROR DETECTED CHECKING CONTROL REGISTER 4
ERROR NUMBER 4 - ERROR DETECTED CHECKING CONTROL REGISTER 6

EXAMPLES OF EACH TYPE OF CONTROL REGISTER ERROR PRINTOUT ARE SHOWN BELOW:

** CONTROL REGISTER 0 ERROR MESSAGES **

```
CVCDB DVC FTL ERR 00001 ON UNIT 00 TST 001 SUB 000 PC: XXXXXX
CONTROL REG 0 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX
```

THE ABOVE ERROR MESSAGE IS REPORTED FOR ALL CONTROL REGISTER 0 ERRORS EXCEPT WHEN CHECKING THE STATE ANALYZERS DEVICE TYPE. IF AN ERROR IS ENCOUNTERED WHEN CHECKING THE DEVICE TYPE, THE FOLLOWING ERROR REPORT WILL BE GIVEN:

```
CVCDB DVC FTL ERR 0001 ON UNIT 00 TST 001 SUB 000 PC: XXXXXX
CONTROL REG 0 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX GOOD. XXXXXX
```

```
TIME OUT ERROR ADDRESSING CONTROL REG 0
```

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 0 AND CAN'T. THE PROGRAM THEN JUMPS TO TIME OUT VECTOR #4.

** CONTROL REGISTER 2 ERROR MESSAGE **

```
CVCDB DVC FTL ERR 00002 ON UNIT 00 TST 004 SUB 000 PC: XXXXXX
CONTROL REG 2 ERROR
REG2 = LOAD: XXXXXX READ: XXXXXX
```

THE ABOVE ERROR MESSAGE WILL BE PRINTED FOR ALL CONTROL REGISTER 2 ERRORS, EXCEPT A TIME OUT ERROR.

```
TIME OUT ERROR ADDRESSING CONTROL REG 2
```

THE ABOVE ERROR PRINTOUT IS GIVEN WHEN THE PROGRAM IS TRYING TO ADDRESS CONTROL REGISTER 2 AND CAN'T. THE PROGRAM THEN JUMPS TO

TIME OUT VECTOR #4.

** CONTROL REGISTER 4 ERROR MESSAGE **

```
CVCDB DVC FTL ERR 00003 ON UNIT 00 TST 006 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 4 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG4 = LOAD: XXXXXX READ: XXXXXX MASK: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG6 = LOAD: XXXXXX RE'D: XXXXXX
```

IN THE ABOVE ERROR, REFER TO THE LINE INDICATING 'REG4 =' FOR CONTROL REGISTER 4 ERROR INFORMATION. THE REMAINING CONTROL REGISTER INFORMATION IS GIVEN TO INDICATE WHAT WAS LOADED INTO THESE REGISTERS PREVIOUS TO THE ERROR. THIS IS DONE TO AID THE USER IN DETERMINING THE FAULT ON ERRORS WHICH NEED PREVIOUS CONTROL REGISTER SETUP.

THE ERROR TYPE MESSAGE IN THE ABOVE ERROR REPORT WILL BE ONE OF THOSE LISTED BELOW. THESE MESSAGES ARE REPORTED TO HELP THE USER IDENTIFY THE AREA OF LOGIC BEING TESTED IN WHICH THE ERROR WAS DETECTED. THESE ERROR TYPE MESSAGES ARE AS FOLLOWS:

```
        OR ARRAY DATA ERROR - ORO 7:0
        AND ARRAY DATA ERROR
        FUSL7 FLIP-FLOP - OR ARRAY DATA ERROR
        AND - OR ARRAY DATA ERROR
```

** CONTROL REGISTER 6 ERROR MESSAGE **

THERE ARE FOUR TYPES OF ERROR MESSAGES THAT ARE REPORTED FOR CONTROL REGISTER 6 ERRORS WHICH ARE SHOWN BELOW.

```
CVCDB DVC FTL ERR 00004 ON UNIT 00 TST 008 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX MASK: XXXXXX GOOD: XXXXXX BAD: XXXXXX

CVCDB DVC FTL ERR 00004 ON UNIT 00 TST 021 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
TRAM ADDRESS REG = XXXXXX
REG0 - LOAD: XXXXXX READ: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX

CVCDB DVC FTL ERR 00004 ON UNIT 00 TST 056 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
REG0 = LOAD: XXXXXX READ: XXXXXX
REG2 = LOAD: XXXXXX READ: XXXXXX
REG4 = LOAD: XXXXXX READ: XXXXXX MASK: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG6 - LOAD: XXXXXX READ. XXXXXX
```

```
CVCDB DVC FTL ERR 00004 ON UNIT 00 TST 053 SUB 000 PC: XXXXXX
ERROR TYPE MESSAGE (SEE BELOW)
CONTROL REG 6 ERROR
EVNT CNT LOADED: XXXXXX EVNT CNT BEFORE CNT DOWN: XXXXXX
REG0 = LOAD: XXXXXX MASK: XXXXXX
REG2 = LOAD: XXXXXX MASK: XXXXXX
REG4 = LOAD: XXXXXX READ: XXXXXX MASK: XXXXXX GOOD: XXXXXX BAD: XXXXXX
REG6 = LOAD: XXXXXX READ: XXXXXX
```

IN THE ABOVE ERRORS, REFER TO THE LINE INDICATING 'REG6 =" FOR CONTROL REGISTER 6 ERROR INFORMATION. THE REMAINING CONTROL REGISTER INFORMATION IS GIVEN TO INDICATE WHAT WAS LOADED INTO THOSE REGISTERS PREVIOUS TO THE ERROR. THIS IS DONE TO AID THE USER IN DETERMINING THE FAULT ON ERRORS WHICH NEED PREVIOUS CONTROL REGISTER SETUP. THE SECOND AND LAST ERROR MESSAGE SHOWN ABOVE PROVIDE ADDITIONAL INFORMATION OF CONDITIONS SETUP PREVIOUS TO THE ERROR WHICH MAY BE HELPFUL TO THE USER IN DETERMINING THE ERROR.

THE ERROR TYPE MESSAGE IN THE ABOVE ERROR REPORTS WILL BE ONE OF THOSE LISTED BELOW. THESE MESSAGES ARE REPORTED TO HELP THE USER IDENTIFY THE AREA OF LOGIC BEING TESTED IN WHICH THE ERROR WAS DETECTED. THESE ERROR TYPE MESSAGES ARE AS FOLLOWS:

```
TRAM ADDRESS REG - TRAD 9:0
TRAM DATA IN BUF - TRDI 15:0
TRAM DATA IN BUF - TRDI 31:16
TRAM DATA IN BUF - TRDI 47:32
TRAM DATA IN BUF - TRDI 59:48
TRAM DATA IN BUF - TRDI 59:0
TRAM DATA IN BUF SELECTION
TRAM DATA ERROR - TRDI 15:0
TRAM DATA ERROR - TRDI 31:16
TRAM DATA ERROR - TRDI 47:32
TRAM DATA ERROR - TRDI 55:48
OR ADDRESS REG - ORAD 3:0
EVENT COUNTERS OR FOUT 3:0 ERROR
PDAL7 FAILED TO CLEAR EVENT COUNTERS
CDAL0 FAILED TO LOAD EVENT COUNTERS
FUSL 3:0 FLIP-FLOP ERROR
SBL 59:56 FLIP-FLOP ERROR
EXPT 7:0 FLIP-FLOP ERROR
```

4.0 PERFORMANCE AND PROGRESS REPORTS

AT THE END OF EACH PASS, THE PASS COUNT IS GIVEN ALONG WITH THE TOTAL NUMBER OF ERRORS REPORTED SINCE THE DIAGNOSTIC WAS STARTED. THE "LOP" SWITCH CAN BE USED TO CONTROL HOW OFTEN THE END OF PASS MESSAGE IS PRINTED. SECTION 2.2 DESCRIBES SWITCHES.

5.0 DEVICE INFORMATION TABLES

CONTROL REGISTER 0 (163010)

```
15  CDAL15  BIT 15 = 1 READ DEVICE TYPE IN BITS 15-8. STATE
            ANALYZER DEVICE TYPE EQUALS 2 (1000)
```

BIT 15 - 0 READ DEVICE NUMBER INTO BITS 11-8.

14	CDAL14	ALWAYS A 0 ON READ
13	CDAL13	ALWAYS A 0 ON READ
12	CDAL12	ALWAYS A 0 ON READ
		BITS 11-8 ARE USED TO SELECT THE DEVICE NUMBER OF THE STATE ANALYZER. THESE BITS MUST BE EQUAL TO THE SETTING OF SWITCHES DEV 3, DEV 2, DEV 1 AND DEV 0.
11	CDAL11	
10	CDAL10	
9	CDAL9	
8	CDAL8	
7	CDAL7	1 - DISABLE OUTPUTS OF "OR ADDRESS REG" ENABLE FOUT 3:0 TO DRIVE "OR" ADDRESS 0 - ENABLE OUTPUTS OF "OR ADDRESS REG"
6	CDAL6	1/0 CLOCK SIGNAL "TRNST H"
5	CDAL5	1 - STOP TRACING WHEN "TRAD10 H" SET HIGH 0 - CONTINUOUS TRACING
4	CDAL4	1 - ENABLE ALL AND/OR ARRAY RAMS 0 - ENABLE ONLY ONE AND/OR ARRAY RAM
3	CDAL3	TRACE RAM BUS SELECT
2	CDAL2	TRACE RAM BUS SELECT

CDAL3	CDAL2	
0	0	ENABLE OUTPUTS OF TRACE RAM DATA IN BUFFER ONTO TRACE RAM BUS
0	1	ENABLE TRACE RAM DATA ONTO TRACE RAM BUS
1	0	ENABLE SYSTEM BUS AND SBL 59:56 FLIP-FLOPS ONTO TRACE RAM BUS

1	CDAL1	1 - ENABLE FUNCTION SELECT F/F'S ONTO SYSTEM BUS
0	CDAL0	1 - CLEAR TRAM ADDRESS REG, CLEAR TRACING FLIP-FLOP, CLEAR SBL 59:56 FLIP-FLOPS, AND RELOAD EVENT COUNTERS FROM EVENT COUNTER REGISTERS

CONTROL REGISTER 2 (163012)

15-8		BITS 15-8 ARE NOT AVAILABLE IN CONTROL REGISTER 2
7	PDAL7	1 - CLEAR EVENT COUNTERS
6	PDAL6	1 - PRESET TRACING FLIP-FLOP
5	PDAL5	0 - CLEAR FUNCTION SELECTS
4	PDAL4	1 - EXTERNAL PROBE "CLK" SIGNAL WILL LOAD EXTP 7:0 FLIP-FLOP'S WHEN "CLK" IS SET LOW. 0 - EXTERNAL PROBE "CLK" SIGNAL WILL LOAD EXTP 7:0 FLIP-FLOP'S WHEN "CLK" IS SET HIGH.
3	PDAL3	SELECT POINTER REGISTER
2	PDAL2	SELECT POINTER REGISTER
1	PDAL1	SELECT POINTER REGISTER

0 PDAL0 SELECT POINTER REGISTER

STATE ANALYZER'S POINTER REGISTER AND CONTROL REGISTER 4 (163014)

PDAL BITS 3:0	SIGNAL	DESCRIPTION
00	PTER0 L	WRITE/READ AND ARRAY RAM 0
01	PTER1 L	WRITE/READ AND ARRAY RAM 1
02	PTER2 L	WRITE/READ AND ARRAY RAM 2
03	PTER3 L	WRITE/READ AND ARRAY RAM 3
04	PTER4 L	WRITE/READ AND ARRAY RAM 4
05	PTER5 L	WRITE/READ AND ARRAY RAM 5
06	PTER6 L	WRITE/READ AND ARRAY RAM 6
07	PTER7 L	WRITE/READ AND ARRAY RAM 7
10	PTER8 L	WRITE/READ AND ARRAY RAM 8
11	PTER9 L	WRITE/READ AND ARRAY RAM 9
12	PTER10 L	WRITE/READ AND ARRAY RAM 10
13	PTER11 L	WRITE/READ AND ARRAY RAM 11
14	PTER12 L	WRITE/READ AND ARRAY RAM 12
15	PTER13 L	WRITE/READ AND ARRAY RAM 13
16	PTER14 L	WRITE/READ AND ARRAY RAM 14
17	PTER15 L	WRITE/READ OR ARRAY RAM'S

STATE ANALYZER'S POINTER REGISTER AND CONTROL REGISTER 6 (163016)

PDAL BITS 3:0	SIGNAL	DESCRIPTION
00	PTER0 L	WRITE/READ TRACE RAM (TRAM) ADDRESS REG
01	PTER1 L	WRITE TRAM 15:0 WITH TRDI DATA FROM TRAM BUS SELECTED. READ TRDI 15:0 DATA FROM TRAM BUS SELECTED
02	PTER2 L	WRITE TRAM 31:16 WITH TRDI DATA FROM TRAM BUS SELECTED. READ TRDI 31:16 DATA FROM TRAM BUS SELECTED
03	PTER3 L	WRITE TRAM 47:32 WITH TRDI DATA FROM TRAM BUS SELECTED READ TRDI 47:32 DATA FROM TRAM BUS SELECTED.
04	PTER4 L	WRITE TRAM 55:48 WITH TRDI DATA FROM TRAM BUS SELECTED. READ TRDI 59:48 DATA FROM TRAM BUS SELECTED.
05	PTER5 L	WRITE TRAM DATA IN BUFFER 15:0 FROM Q-BUS DATA BITS 15:0
06	PTER6 L	WRITE TRAM DATA IN BUFFER 31:16 FROM Q-BUS DATA BITS 15:0.
07	PTER7 L	WRITE TRAM DATA IN BUFFER 47:32 FROM Q-BUS DATA BITS 15:0
10	PTER8 L	WRITE TRAM DATA IN BUFFER 59:48 FROM Q-BUS DATA BITS 11:0.
11	PTER9 L	LOAD EVENT COUNTER REGISTER 0 AND EVENT COUNTER 0. CLEAR SBL56 FLIP-FLOP
12	PTER10 L	LOAD EVENT COUNTER REGISTER 1 AND EVENT COUNTER 1. CLEAR SBL57 FLIP-FLOP.
13	PTER11 L	LOAD EVENT COUNTER REGISTER 2 AND EVENT COUNTER 2. CLEAR SBL58 FLIP-FLOP.
14	PTER12 L	LOAD EVENT COUNTER REGISTER 3 AND EVENT COUNTER 3. CLEAR SBL59 FLIP-FLOP
15	PTER13 L	NOT USED

16	PTER14 L	NOT USED
17	PTER15 L	READ/WRITE OR ADDRESS REGISTER (CDAL7=0) READ FOUT F/F'S ON 'OR ADDRESS BITS (CDAL7=1)

NOTE: THE TRACE RAM (TRAM) BUS SELECTED IS CONTROLLED BY CONTROL REGISTER 0 BITS CDAL3 AND CDAL2.

6.0 TEST SUMMARIES

TEST 1:

THIS TEST WILL CHECK THAT THE STATE ANALYZER CAN BE SELECTED AND INITIALIZED TO A KNOWN STATE. THIS TEST WILL BE EXECUTED AT THE BEGINNING OF EVERY TEST TO PUT THE MODULE IN A KNOWN STATE. THE TEST WILL LOAD THE DEVICE NUMBER INTO CONTROL REGISTER 0 AND CHECK THAT THE DEVICE NUMBER CAN BE READ BACK CORRECTLY. THE LOW BYTE OF CONTROL REGISTER 0 WILL BE CHECKED TO BE ZERO. THE TEST WILL THEN LOAD THE DEVICE NUMBER AND THE SIGNAL CDAL15 INTO CONTROL REGISTER 0 AND CHECK THAT THE DEVICE TYPE AND THE LOW BYTE CAN BE READ BACK CORRECTLY. THE TEST WILL THEN CLEAR THE SIGNAL CDAL15 IN CONTROL REGISTER 0 AND CHECK THE DEVICE NUMBER IN THE LOW BYTE AGAIN. THE TEST WILL ALSO LOAD ALL ZEROES INTO CONTROL REGISTER 2 AND CHECK THAT ALL ALL ZEROES CAN BE READBACK FROM CONTROL REGISTER 2.

TEST 2:

THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS CDAL7, CDAL6, CDAL5, CDAL4, CDAL3, CDAL2, CDAL1 AND CDAL0 CAN BE SET TO ALL ONES AND THEN ALL ZEROES.

TEST 3:

THIS TEST WILL CHECK CONTROL REGISTER 0 READ/WRITE BITS CDAL7 TO CDAL0 WITH AN ALTERNATING ONES AND ZEROES PATTERN (252) AND THEN AN ALTERNATING ZEROES AND ONES PATTERN (125).

TEST 4:

THIS TEST WILL CHECK CONTROL REGISTER 0 READ/WRITE BITS CDAL7 TO CDAL0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT UNTIL THE TEST PATTERN 377 HAS BEEN LOADED INTO CONTROL REGISTER 0 AND CHECKED.

TEST 5:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS, PDAL7, PDAL6 PDAL5, PDAL4, PDAL3, PDAL2, PDAL1, AND PDAL0, TO BE SET TO ALL ONES AND THEN TO ALL ZEROES.

TEST 6:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7 TO PDAL0 WITH AN ALTERNATING ONES AND ZEROES PATTERN (252) AND THEN AN ALTERNATING ZEROES AND ONES PATTERN (125).

TEST 7:

THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7 TO PDAL0 USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START WITH 0 AND INCREMENT UNTIL THE TEST PATTERN 377 HAS BEEN LOADED AND TESTED.

TEST 8:

THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) BY LOADING A PATTERN OF ALL ONES (3777) INTO THE ADDRESS REGISTER AND THEN READING AND CHECKING THE ADDRESS REGISTER FOR ALL ONES. THE TEST WILL THEN LOAD, READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH A DATA PATTERN OF ALL ZEROES. TO WRITE AND READ THE TRACE RAM ADDRESS REGISTER, THE PROGRAM WILL CLEAR CONTROL REGISTER 0 BITS CDAL7 TO CDAL0, CLEAR CONTROL REGISTER 2 BITS PDAL7 TO PDAL0, LOAD THE DATA PATTERN INTO THE TRACE RAM ADDRESS REGISTER VIA A WRITE COMMAND TO CONTROL REGISTER 6, AND THEN READ THE TRACE RAM ADDRESS REGISTER VIA A READ COMMAND TO CONTROL REGISTER 6. WHEN PDAL3 TO PDAL0 ARE SET TO A 0, THE SIGNAL PTERO L WILL BE ASSERTED LOW IN THE POINTER REGISTER. THIS SIGNAL BEING SET LOW, ALONG WITH A WRITE OR READ COMMAND TO CONTROL REGISTER 6 WILL ASSERT THE SIGNALS WPTO L AND RPTO L RESPECTIVELY. THE SIGNAL WPTO L WILL LOAD THE ADDRESS INTO THE TRACE RAM ADDRESS REGISTER, AND THE SIGNAL RPTO L WILL READ THE ADDRESS FROM THE TRACE RAM ADDRESS REGISTER.

TEST 9:

THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) BY LOADING AN ALTERNATING ONES AND ZEROES PATTERN (2525) INTO THE TRACE RAM ADDRESS REGISTER AND THEN READING AND CHECKING THE ADDRESS REGISTER FOR THE PATTERN LOADED. THE TEST WILL THEN LOAD, READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH AN ALTERNATING ZEROES AND ONES DATA PATTERN (1252).

TEST 10:

THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) USING A BINARY COUNT PATTERN. THE DATA PATTERN WILL START WITH ZERO AND INCREMENT BY ONE UNTIL THE DATA PATTERN 3777 HAS BEEN LOADED AND CHECKED.

TEST 11:

THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE CLEARED WHEN CONTROL REGISTER 0 SIGNAL CDAL 0 H IS SET TO A ONE. THE TEST WILL LOAD ALL ONES (3777) INTO THE TRACE RAM ADDRESS REGISTER AND CHECK THAT ALL ONES WERE LOADED. THE TEST WILL THEN SET THE SIGNAL CDAL 0 H TO A ONE IN CONTROL REGISTER 0 AND THEN READ THE TRACE RAM ADDRESS REGISTER CHECKING IT TO BE 0. THE SIGNAL CDAL 0 H WILL THEN BE CLEARED AND THE TRACE RAM ADDRESS REGISTER WILL BE CHECKED AGAIN TO CONTAIN ALL ZEROES.

TEST 12:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI15 H TO TRDI0 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL ZEROES (000000).

TEST 13:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI15 H TO TRDI0 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TEST 14:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI31 H TO TRDI16 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL ZEROES (000000).

TEST 15:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI31 H TO TRDI16 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TEST 16:

THIS TEST WILL CHCEK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI47 H TO TRDI32 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL ZEROES (000000)

TEST 17:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI47 H TO TRDI32 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252) AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).

TEST 18:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI59 H TO TRDI48 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (007777) AND THEN ALL ZEROES (000000).

TEST 19:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI59 H TO TRDI48 H FROM THE LSI-11 BUS. THE TEST WILL WRITE, READ AND CHECK THE TRACE RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (005252) AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (002525).

TEST 20:

THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTERS FROM THE LSI-11 BUS TO BE SELECTED CORRECTLY BY THE POINTER REGISTER. THE TEST WILL WRITE AND CHECK TRDI BITS 15:0 WITH A DATA PATTERN EQUAL TO 1, TRDI BITS 31:16 WITH A DATA PATTERN EQUAL TO 2, TRDI BITS 47:32 WITH A DATA PATTERN EQUAL TO 3 AND TRDI BITS 59:48 WITH A DATA PATTERN EQUAL TO 4. THE TEST WILL READ EACH SET OF TRACE RAM DATA IN BITS CHECKING THE BUFFERS TO CONTAIN THE CORRECT DATA PATTERN.

TEST 21:

THIS TEST WILL CHECK TRACE RAM BITS TRDI 15:0 WITH A DATA PATTERN OF 125252 AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED WITH THESE DATA PATTERNS.

TEST 22:

THIS TEST WILL CHECK TRACE RAM BITS TRDI 31:16 WITH A DATA PATTERN OF 125252 AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED WITH THESE DATA PATTERNS.

TEST 23:

THIS TEST WILL CHECK TRACE RAM BITS TRDI 47:32 WITH A DATA PATTERN OF 125252 AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED WITH THESE DATA PATTERNS.

TEST 24:

THIS TEST WILL CHECK TRACE RAM BITS TRDI 55:48 WITH A DATA PATTERN OF 252 AND 525. EACH LOCATION OF THE TRACE RAM WILL BE CHECKED WITH THESE DATA PATTERNS. HOWEVER THE TRACE RAM DATA IN BUFFERS WHICH LOAD TRACE RAM BITS TRDI 55:48 WILL BE LOADED WITH DATA PATTERNS 5252 AND 2525. TRACE RAM DATA IN BUFFER BITS 59:56 ARE NOT LOADED INTO ANY TRACE RAMS.

TEST 25:

THIS TEST WILL CHECK TRACE RAM TRDI 15:0 TO BE ADDRESSED CORRECTLY AND THAT NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIPS. THE TEST WILL LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND CHECK THE LOCATION TO CONTAIN AS DATA ITS ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN. THE TEST WILL REPEAT THIS SEQUENCE FOR ALL ADDRESSES OF THE TRACE RAM. WHEN ALL ADDRESSES HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND READ EACH LOCATION OF THE 1K TRACE RAM CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

TEST 26:

THIS TEST WILL CHECK TRACE RAM TRDI 31:16 TO BE ADDRESSED CORRECTLY AND THAT NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIPS. THE TEST WILL LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS

ADDRESS. ONCE ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND CHECK THE LOCATION TO CONTAIN AS DATA ITS ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN. THE TEST WILL REPEAT THIS SEQUENCE FOR ALL ADDRESSES OF THE TRACE RAM. WHEN ALL ADDRESSES HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND READ EACH LOCATION OF THE 1K TRACE RAM CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

TEST 27:

THIS TEST WILL CHECK TRACE RAM TRDI 47:32 TO BE ADDRESSED CORRECTLY AND THAT NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIPS. THE TEST WILL LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND CHECK THE LOCATION TO CONTAIN AS DATA ITS ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN. THE TEST WILL REPEAT THIS SEQUENCE FOR ALL ADDRESSES OF THE TRACE RAM. WHEN ALL ADDRESSES HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND READ EACH LOCATION OF THE 1K TRACE RAM CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

TEST 28:

THIS TEST WILL CHECK TRACE RAM TRDI 55:48 TO BE ADDRESSED CORRECTLY AND THAT NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIPS. THE TEST WILL LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND CHECK THE LOCATION TO CONTAIN AS DATA ITS ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN. THE TEST WILL REPEAT THIS SEQUENCE FOR ALL ADDRESSES OF THE TRACE RAM. WHEN ALL ADDRESSES HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING ADDRESS AND READ EACH LOCATION OF THE 1K TRACE RAM CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

TEST 29:

THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN COUNT UP BY ONE WHEN THE SIGNAL "CTR L" IS PULSED. THE TRACE RAM ADDRESS REGISTER WILL BE COUNTED UP BY ONE FROM ADDRESS 0 TO ADDRESS 3777 AND THEN BACK TO ADDRESS 0. IN ORDER TO PULSE THE SIGNAL "CTR L", THE PROGRAM WILL SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0 WHICH WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE, WHICH WILL CAUSE THE SIGNAL ANST L TO PULSE, WHICH WILL PULSE THE SIGNAL ORST L. WITH THE TRACING FLIP-FLOP HELD IN THE PRESET STATE BY THE SIGNAL PDAL6 BEING SET TO A ZERO AND THE SIGNALS TRST L AND TRANST H BEING PULSED, A PULSE WILL OCCUR ON THE SIGNAL CTR L.

TEST 30:

THIS TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET BY PDAL6 IN CONTROL REGISTER 2 AND CLEARED BY CDAL0 IN CONTROL REGISTER 0.

TEST 31:

THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE INCREMENTED BY ONE VIA THE SIGNAL "CTR L" WHEN THE TRACING FLIP-FLOP IS SET TO A ONE, CDAL REGISTER BIT 5 IS SET TO A ONE, TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ZERO AND THE SIGNALS TRST L AND TRANST H ARE PULSED. THE TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER WILL NOT GET INCREMENTED BY THE SIGNAL "CTR L" WHEN THE TRACING FLIP-FLOP IS SET TO ONE, CDAL REGISTER BIT 5 IS SET TO A ONE, TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE AND THE SIGNALS TRST L AND TRANST H ARE PULSED. THE TEST WILL THEN CHECK THAT THE TRACE RAM ADDRESS REGISTER WILL GET INCREMENTED BY VIA VIA THE SIGNAL "CTR L" WHEN THE TRACING FLIP-FLOP IS SET TO A ONE, CDAL REGISTER BIT 5 IS SET TO A ZERO, TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE AND THE SIGNALS TRST L AND TRANST H ARE PULSED.

TEST 32:

THE TEST WILL CHECK THAT THE TRACE RAMS CAN BE LOADED FROM THE TRACE RAM DATA IN BUFFERS VIA THE SIGNALS "CTR H" AND "CTR L".

THE TEST WILL LOAD AND CHECK EACH TRACE RAM DATA IN BUFFER WITH THE FOLLOWING DATA PATTERNS:

    TRDI 15:0 - DATA PATTERN OF 151515
    TRDI 31:16 - DATA PATTERN OF 113131
    TRDI 47:32 - DATA PATTERN OF 074747
    TRDI 59:48 - DATA PATTERN OF 005555

THE TEST WILL ASSERT THE SIGNAL TRSL0 L BY CLEARING THE LOW BYTE OF CONTROL REGISTER 0. THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS. THE TEST WILL LOAD ADDRESS 0 INTO THE TRACE RAM ADDRESS REGISTER TO SELECT ADDRESS 0 OF ALL TRACE RAMS. THE TEST WILL THEN PRESET THE TRACING FLIP-FLOP TO THE HIGH STATE BY SETTING THE BIT PDAL6 IN CONTROL REGISTER 2. THE TEST WILL NOW SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0. SETTING AND CLEARING THE SIGNAL CDAL6 WITH THE TRACING FLIP-FLOP IN THE PRESET STATE, WILL CAUSE THE SIGNALS CTR L AND CTR H TO PULSE. THE SIGNAL CTR L WILL INCREMENT THE TRACE RAM ADDRESS REGISTER BY ONE. THE SIGNALS CTR L AND CTR H WILL LOAD THE TRACE RAM DATA IN BUFFERS INTO ADDRESS 0 OF TRACE RAM BITS TRDI 55:0. AFTER SETTING AND CLEARING CDAL6, THE PROGRAM WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER INCREMENTED TO ADDRESS 1. THE TEST WILL THEN RESET THE TRACE RAM ADDRESS REGISTER TO ADDRESS 0. THE TEST WILL THEN ASSERT THE SIGNAL TRSL1 L BY SETTING THE SIGNAL CDAL2 IN CONTROL REGISTER 0. THE SIGNAL TRSL1 L WILL ENABLE THE TRACE RAMS TO BE READ. THE TEST WILL NOW READ ADDRESS 0 OF EACH TRACE RAM CHECKING THE DATA TO BE THAT WHICH WAS WRITTEN PREVIOUSLY INTO THE TRACE RAM DATA IN BUFFERS.

TEST 33:

THIS TEST WILL CHECK THE OR ADDRESS REGISTER BITS (ORAD3-ORAD0) BY

LOADING AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND THEN LOADING AND ALTERNATING ZEROES AND ONES DATA PATTERN (05). TO WRITE AND READ THE OR ADDRESS REGISTER, THE PROGRAM WILL CLEAR CONTROL REGISTER 0 BITS (CDAL7-CDAL0). CDAL7 BEING A ZERO WILL ENABLE THE OUTPUTS OF THE OR ADDRESS REGISTER. THE PROGRAM WILL SET PDAL3 TO PDAL0 TO A ONE IN CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER15 L TO BE ASSERTED IN THE POINTER REGISTER. ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H. THE SIGNAL WPT15 H WILL LOAD THE DATA FROM BITS 3-0 ON THE WRITE COMMAND INTO OR ADDRESS REGISTER BITS (ORAD3-ORAD0). ON A READ COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL RPT15 H. THE SIGNAL RPT15 H WILL READ THE DATA FROM THE OR ADDRESS REGISTER.

TEST 34:

THIS TEST WILL CHECK THE OR ADDRESS REGISTER BITS ORAD3 TO ORAD0 USING A BINARY COUNT PATTERN STARTING WITH A DATA PATTERN OF ZERO AND INCREMENTING THE PATTERN BY ONE UNTIL THE DATA PATTERN 17 HAS BEEN LOADED AND CHECKED.

TEST 35:

THIS TEST WILL CHECK EACH LOCATION OF THE OR ARRAY RAM (OR0 7:0) WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (125).

THE FOLLOWING SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE OR ARRAY RAM. THE TEST WILL CLEAR ALL THE LOW BITS IN CONTROL REGISTER 0. CDAL7 ENABLES OR ADDRESS REGISTER OUTPUTS. CDAL4 ON A ONE WILL ALLOW ONLY ONE AND/OR ARRAY TO BE SELECTED VIA THE POINTER REGISTER. THE OR ARRAY RAMS WILL BE SELECTED IN THIS TEST BY SETTING PTER15 L IN THE POINTER REGISTER WHICH WILL CAUSE THE SIGNAL PLSL15 L TO BE ASSERTED. THE SIGNAL PLSL15 L WILL ENABLE THE OR ARRAY RAMS TO BE WRITTEN OR READ. THE TEST WILL LOAD THE ADDRESS TO BE TESTED INTO THE OR ADDRESS REGISTER. TO LOAD THE ADDRESS, THE PROGRAM WILL ISSUE A WRITE COMMAND TO CONTROL REGISTER 6. WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH WILL LOAD THE OR ADDRESS REGISTER. TO READ THE OR ADDRESS REGISTER, THE TEST WILL ISSUE A READ COMMAND TO CONTROL REGISTER 6 WHICH WILL CAUSE A PULSE ON THE SIGNAL RPT15 H. THE SIGNAL RPT15 H WILL READ THE DATA FROM THE OR ADDRESS REGISTER. THE TEST WILL NOW WRITE AND READ THE OR ARRAY LOCATION WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252). TO WRITE THE OR ARRAY RAM LOCATION, THE TEST WILL ISSUE A WRITE COMMAND TO CONTROL REGISTER 4. WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPLA15 L. THE SIGNAL WPLA15 L WILL WRITE THE DATA INTO THE OR ARRAY RAM LOCATION. TO READ THE OR ARRAY RAM LOCATION, THE TEST WILL ISSUE A READ COMMAND TO CONTROL REGISTER 4. THE TEST WILL NOW LOAD, READ AND CHECK THE RAM LOCATION WITH AN ALTERNATING ZEROS AND ONES DATA PATTERN (125).

TEST 36:

THIS TEST WILL CHECK THAT ALL ADDRESSES IN THE OR ARRAY RAMS CAN BE ADDRESSED CORRECTLY AND THAT WRITING ONE ADDRESS WILL NOT WRITE ANOTHER

ADDRESS PREVIOUSLY WRITTEN (ADDRESS SHORT). THE TEST WILL WRITE AND CHECK EACH LOCATION OF THE OR ARRAY RAM WITH DATA EQUAL TO ITS ADDRESS. THE DATA PATTERN FOR THE TOP 4 BITS OF THE OR ARRARY RAM WILL BE THE SAME AS THE DATA PATTERN FOR THE LOW 4 BITS OF THE OR ARRAY RAM. AFTER WRITING ALL LOCATIONS OF THE OR ARRAY RAM, THE TEST WILL READ EACH LOCATION OF THE RAM CHECKING THE DATA TO BE EQUAL TO ITS ADDRESS. THE TEST WILL THEN READ EACH LOCATION CHECKING THE DATA TO BE EQUAL TO ITS ADDRESS AND THEN WRITING AND CHECKING THE LOCATION WITH THE ONES COMPLEMENT OF ITS ADDRESS. IF A LOCATION ON THE FIRST READ DOES NOT EQUAL ITS ADDRESS, THEN WRITING A PREVIOUS LOCATION PROBABLY WROTE THE LOCATION IN ERROR ALSO. AFTER ALL LOCATIONS HAVE BEEN TESTED IN THIS MANNER THE PROGRAM WILL READ THE OR ARRAY RAMS AGAIN CHECKING EACH LOCATION TO CONTAIN AS DATA THE ONES COMPLEMENT OF ITS ADDRESS.

TEST 37:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL0 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 3:0.

TEST 38:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL1 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 7:4.

TEST 39:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL2 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 11:8.

TEST 40:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL3 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 15:12.

TEST 41:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL4 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 19:16.

TEST 42.

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL5 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 23:20.

TEST 43:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL6 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 27:24.

TEST 44:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL7 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 31:28.

TEST 45:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL8 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 35:32.

TEST 46:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL9 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 39:36.

TEST 47:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL10 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 43:40.

TEST 48:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL11 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 47:44.

TEST 49:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL12 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 51.48.

TEST 50:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL13 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 55:52.

TEST 51:

THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA PATTERN (05). THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE SIGNAL PLSL14 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 59:56.

TEST 52:

THIS TEST WILL CHECK THAT EACH AND ARRAY IS ACTUALLY SELECTED WHEN ADDRESSED BY THE PLSL SELECT LINE SIGNALS. THE PLSL SELECT SIGNALS ARE GENERATED BY THE POINTER REGISTER PTER SIGNALS VIA CONTROL REGISTER 2. THE TEST WILL CLEAR ALL TRACE RAM DATA IN BUFFER BITS TRDI 59:0. WITH ALL THESE BITS BEING CLEARED, LOCATION 0 OF EACH AND ARRAY WILL BE ADDRESSED. THE TEST WILL THEN SELECT EACH AND ARRAY BY LOADING THE APPROPRIATE PTER SIGNAL IN CONTROL REGISTER 2. THE TEST WILL THEN LOAD, READ AND CHECK THE AND ARRAY WITH THE PTER SIGNAL USED TO SELECT THE AND ARRAY. ONCE EACH AND ARRAY HAS BEEN LOADED AND CHECKED, THE TEST WILL THEN RE-SELECT EACH AND ARRAY CHECKING THE DATA TO BE EQUAL TO THE PTER SELECT SIGNAL. IF ANY ERRORS OCCUR IN THE LAST PORTION OF THE TEST THEN THE ERROR IS PROBABLY RELATED TO THE PLSL SIGNALS OR THE POINTER REGISTER PTER SIGNALS. ONLY ONE AND ARRAY SHOULD BE ENABLED AT A TIME DURING THIS TEST VIA CDAL4 ON A ONE AND THE PTER SELECT SIGNAL.

TEST 53:

THIS TEST WILL CHECK THAT EACH AND ARRAY CAN BE ADDRESSED CORRECTLY AND THAT WRITING ONE LOCATION IN THE AND ARRAY DOES NOT WRITE A HIGHER LOCATION AT THE SAME TIME (ADDRESS SHORT). THE TEST WILL CHECK ONE AND ARRAY AT A TIME UNTIL ALL AND ARRAYS ARE TESTED. THE TEST WILL LOAD AND CHECK EACH LOCATION OF A 16*4 AND ARRAY WITH DATA EQUAL TO THE ADDRESS SELECTED (0-17 OCTAL). ONCE ALL THE LOCATIONS HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL START AT THE BEGINNING ADDRESS OF THE AND ARRAY AND DO THE FOLLOWING:

1. READ LOCATION CHECKING DATA 0 EQUAL THE ADDRESS (0-17)
2. WRITE AND CHECK LOCATION WITH THE 1'S COMPLEMENT OF ADDRESS
3. SEQUENCE TO NEXT ADDRESS
4. REPEAT STEPS 1-3 UNTIL ALL ADDRESSES HAVE BEEN CHECKED

WHEN THE ABOVE SEQUENCE HAS BEEN COMPLETED, THE TEST WILL RESET THE

ADDRESS TO THE BEGINNING ADDRESS OF THE AND ARRAY AND CHECK EACH LOCATION TO CONTAIN THE 1'S COMPLEMENT OF THE ADDRESS.

TEST 54:

THIS TEST WILL CHECKOUT EVENT COUNTER LOGIC FOR EVENT COUNTERS 0 AND 2. THE TEST WILL CHECK THAT THE EVENT COUNTER REGISTERS AND EVENT COUNTERS ARE LOADED CORRECTLY BY COUNTING DOWN THE EVENT COUNTERS AND CHECKING THE FOUT FLIP-FLOPS FOR A BORROW. WHEN THE EVENT COUNTERS ARE COUNTED DOWN TO ZERO AND ONE MORE COUNT DOWN IS ISSUED, A BORROW IS GENERATED WHICH WILL SET THE OUTPUT OF THE FOUT FLIP-FLOP TO A LOW STATE. THE TEST WILL CHECK THAT THE EVENT COUNTERS ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN A BORROW IS GENERATED. THIS IS DONE BY COUNTING DOWN THE EVENT COUNTERS AGAIN CHECKING FOR A BORROW FROM THE EVENT COUNTERS. THE TEST WILL THEN CHECK THAT THE EVENT COUNTERS CAN BE CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7. AFTER SETTING AND CLEARING THE SIGNAL PDAL7, THE TEST WILL DO ONE MORE COUNT DOWN AND CHECK THAT A BORROW IS GENERATED FROM THE EVENT COUNTERS. THE ABOVE SEQUENCE IS REPEATED WITH EACH OF THE FOLLOWING DATA PATTERNS: 0, 1, 2, 4, 10, 20, 40, 100, 200, 125, AND 252.

TEST 55:

THIS TEST WILL CHECKOUT EVENT COUNTER LOGIC FOR EVENT COUNTERS 1 AND 3. THE TEST WILL CHECK THAT THE EVENT COUNTER REGISTERS AND EVENT COUNTERS ARE LOADED CORRECTLY BY COUNTING DOWN THE EVENT COUNTERS AND CHECKING THE FOUT FLIP-FLOPS FOR A BORROW. WHEN THE EVENT COUNTERS ARE COUNTED DOWN TO ZERO AND ONE MORE COUNT DOWN IS ISSUED, A BORROW IS GENERATED WHICH WILL SET THE OUTPUT OF THE FOUT FLIP-FLOP TO A LOW STATE. THE TEST WILL CHECK THAT THE EVENT COUNTERS ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN A BORROW IS GENERATED. THIS IS DONE BY COUNTING DOWN THE EVENT COUNTERS AGAIN CHECKING FOR A BORROW FROM THE EVENT COUNTERS. THE TEST WILL THEN CHECK THAT THE EVENT COUNTERS CAN BE CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7. AFTER SETTING AND CLEARING THE SIGNAL PDAL7, THE TEST WILL DO ONE MORE COUNT DOWN AND CHECK THAT A BORROW IS GENERATED FROM THE EVENT COUNTERS. THE ABOVE SEQUENCE IS REPEATED WITH EACH OF THE FOLLOWING DATA PATTERNS: 0, 1, 2, 4, 10, 20, 40, 100, 200, 125, AND 252.

TEST 56:

THIS TEST WILL CHECK THAT THE SIGNAL CDAL0, WHEN SET AND CLEARED, WILL CAUSE THE EVENT COUNTERS TO BE LOADED FROM THE EVENT COUNTER REGISTERS.

TEST 57:

THIS TEST WILL CHECK THAT FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3, AND FUSL1 CAN BE SET TO A ONE AND THAT FUNCTION SELECT FLIP-FLOPS FUSL2 AND FUSL0 CAN BE SET TO A ZERO. THE FUNCTION SELECT FLIP-FLOPS ARE SET TO THE STATE MENTIONED VIA THE DATA FROM THE OR ARRAY RAM AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. AFTER CHECKING THAT THE FUNCTION SELECT FLIP-FLOPS ARE IN THE CORRECT STATE VIA CONTROL REGISTER 4 AND CONTROL REGISTER 6, THE TEST WILL SET THE SIGNAL PDAL5 TO A 0 IN CONTROL REGISTER 2. PDAL5 ON A ZERO WILL PRESET THE FUNCTION SELECT FLIP-FLOPS TO THE ZERO STATE. THE TEST WILL THEN VERIFY THAT THE FLIP-FLOPS ARE CLEARED BY READING CONTROL REGISTER

4 AND CONTROL REGISTER 6 AGAIN.

TEST 58:

THIS TEST WILL CHECK THAT FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3, AND FUSL1 CAN BE SET TO A ZERO AND THAT FUNCTION SELECT FLIP-FLOPS FUSL2 AND FUSL0 CAN BE SET TO A ONE. THE FUNCTION SELECT FLIP-FLOPS ARE SET TO THE STATE MENTIONED VIA THE DATA FROM THE OR ARRAY RAM AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. AFTER CHECKING THAT THE FUNCTION SELECT FLIP-FLOPS ARE IN THE CORRECT STATE VIA CONTROL REGISTER 4 AND CONTROL REGISTER 6, THE TEST WILL SET THE SIGNAL PDAL5 TO A 0 IN CONTROL REGISTER 2. PDAL5 ON A ZERO WILL PRESET THE FUNCTION SELECT FLIP-FLOPS TO THE ZERO STATE. THE TEST WILL THEN VERIFY THAT THE FLIP-FLOPS ARE CLEARED BY READING CONTROL REGISTER 4 AND CONTROL REGISTER 6 AGAIN.

TEST 59:

THIS TEST WILL CHECK THAT THE EVENT COUNTERS WILL GET RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE OUTPUT OF FUNCTION SELECT FLIP-FLOP FUSL7 H IS SET TO THE HIGH STATE. TO CHECK THAT THIS HAPPENS, THE TEST WILL LOAD ALL EVENT COUNTERS WITH THE VALUE 377 OCTAL. THE TEST WILL THEN COUNT DOWN THE EVENT COUNTERS UNTIL THE EVENT COUNTERS EQUAL 200 OCTAL. THE TEST CHECKS THAT NO BORROWS ARE GENERATED FROM THE EVENT COUNTERS WHEN THE EVENT COUNTERS ARE COUNTED DOWN. THIS IS DONE BY CHECKING FOUT 3:0 FLIP-FLOPS ON THE ORAD 3:0 SIGNAL LINES. THE TEST WILL THEN LOAD LOCATION ZERO OF THE "OR ARRAY RAM" WITH A DATA PATTERN OF 200 OCTAL WHICH WILL CAUSE THE SIGNAL "ORO 7 L" TO BE ASSERTED LOW. THE TEST WILL THEN SET AND CLEAR THE SIGNAL CDAL6 WHICH WILL CAUSE THE SIGNAL ANST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE PULSED. UPON THE PULSING OF THE SIGNAL ORST L THE "OR ARRAY" DATA WILL BE LOADED INTO THE FUNCTION SELECT FLIP-FLOPS, THUS SETTING THE OUTPUT OF FUSL7 H FLIP-FLOP TO THE HIGH STATE. WHEN FUSL7 H FLIP-FLOP IS SET HIGH, A ONE SHOT WILL BE FIRED WHICH WILL CAUSE THE EVENT COUNTERS TO BE LOADED FROM THE EVENT COUNTER REGISTERS. TO TEST THAT THE EVENT COUNTERS WERE RELOADED FROM THE EVENT COUNTER REGISTERS, THE TEST WILL COUNT DOWN THE EVENT COUNTERS 400 OCTAL TIMES CHECKING THAT NO BORROWS ARE GENERATED FROM THE EVENT COUNTERS UNTIL THE LAST COUNT DOWN IS ISSUED.

TEST 60:

THIS TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET BY FUNCTION SELECT FLIP-FLOP FUSL0 H AND CLEARED BY FUNCTION SELECT FLIP-FLOP FUSL1 H. THE TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET AND CLEARED BY CHECKING THE TRACE RAM ADDRESS REGISTER. THE TRACE RAM ADDRESS REGISTER WILL NOT BE INCREMENTED WHEN THE TRACING FLIP-FLOP IS CLEARED AND CDAL6 IS SET AND CLEARED IN CONTROL REGISTER 0, PULSING TRST L AND TRANST H. THE TRACE RAM ADDRESS REGISTER WILL BE INCREMENTED WHEN THE TRACING FLIP-FLOP IS SET AND CDAL6 IS SET AND CLEARED IN CONTROL REGISTER 0 PULSING TRST L AND TRANST H. THE FUNCTION SELECT FLIP-FLOPS ARE SET AND CLEARED VIA THE "OR ARRAY RAM" DATA AND THE SIGNAL ORST L BEING PULSED.

TEST 61:

THIS TEST WILL CHECK THAT SBL56 AND SBL58 FLIP-FLOPS CAN BE SET AND

CLEARED. SBL57 AND SBL59 ARE CHECKED TO REMAIN CLEARED DURING THIS TEST. SBL 59:56 FLIP-FLOPS ARE CHECKED BY THE PROGRAM ON THE TRACE RAM DATA IN BUS SIGNAL LINES TRDI 59:56 WHEN THE SIGNAL ''TRSL2 L'' IS ASSERTED LOW. SBL56 FLIP-FLOP IS SET VIA A BORROW FROM EVENT COUNTER 0 AND A COUNT DOWN PULSE TO EVENT COUNTER 0. SBL56 FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 0. SBL58 FLIP-FLOP IS SET BY ''OR ARRAY RAM'' DATA ''ORO4 L'' BEING SET LOW AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. SBL58 FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 2.

TEST 62:

THIS TEST WILL CHECK THAT SBL57 AND SBL59 FLIP-FLOPS CAN BE SET AND CLEARED. SBL56 AND SBL58 ARE CHECKED TO REMAIN CLEARED DURING THIS TEST. SBL 59:56 FLIP-FLOPS ARE CHECKED BY THE PROGRAM ON THE TRACE RAM DATA IN BUS SIGNAL LINES TRDI 59.56 WHEN THE SIGNAL ''TRSL2 L'' IS ASSERTED LOW. SBL57 FLIP-FLOP IS SET VIA A BORROW FROM EVENT COUNTER 1 AND A COUNT DOWN PULSE TO EVENT COUNTER 1. SBL57 FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 1. SBL59 FLIP-FLOP IS SET BY ''OR ARRAY RAM'' DATA ''ORO5 L'' BEING SET LOW AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. SBL59 FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 3.

TEST 63:

THIS TEST WILL CHECK THAT SBL 59:56 FLIP-FLOPS CAN BE SET AND THAT THEY CAN BE CLEARED BY SETTING AND CLEARING CDAL0 IN CONTROL REGISTER 0. SBL57 AND SBL56 FLIP-FLOPS ARE SET VIA A BORROW FROM EVENT COUNTER 1 AND EVENT COUNTER 0 ALONG WITH THE APPROPRIATE COUNT DOWN PULSES. SBL59 AND SBL58 ARE SET VIA ''OR ARRAY RAM'' DATA BITS ''ORO5 L'' AND ''ORO4 L'' BEING SET LOW AND THE SIGNAL ORST L BEING PULSED VIA THE PULSING OF CDAL6 IN CONTROL REGISTER 0. THE TEST WILL CHECK THE SBL FLIP-FLOPS TO BE SET BY READING THE TRACE RAM DATA IN BUS BITS TRDI 59:56 WHEN THE SIGNAL TRSL2 L IS ASSERTED LOW. THE TEST WILL THEN SET AND CLEAR CDAL0 IN CONTROL REGISTER 0 AND CHECK THAT SBL 59:56 FLIP-FLOPS CLEARED.

TEST 64:

IF THE OPERATOR ANSWERED YES TO THE HARDWARE QUESTION ''EXTERNAL PROBE CONNECTED'', THE FOLLOWING TEST WILL BE EXECUTED, OTHERWISE, THE TEST WILL BE ABORTED. BEFORE THIS TEST CAN BE PERFORMED, THE OPERATOR MUST PLUG THE EXTERNAL PROBE INTO THE STATE ANALYZER AND CONNECT THE PROBE LEADS 7:0 TO EVENT COUNTER 0 SIGNALS SDBL 7:0 H RESPECTIVELY. THE PROBE'S CLK LEAD MUST BE CONNECTED TO EVENT COUNTER 1 SIGNAL SDBL8 H.

THE TEST WILL CHECK THE EXTERNAL PROBE AND THE EXTERNAL PROBE LOGIC ON THE STATE ANALYZER MODULE. DATA PATTERNS OF 252 AND 125 WILL BE LOADED INTO EVENT COUNTER 0 TO PROVIDE LOGIC LEVELS TO THE EXTERNAL PROBE. THE SIGNAL SDBL8 L IN EVENT COUNTER 1 WILL BE SET AND CLEARED TO PROVIDE THE ''CLK'' SIGNAL FOR THE EXTERNAL PROBE. WHEN PDAL4, IN CONTROL REGISTER 2, IS SET TO A ZERO, AND THE CLK SIGNAL IS SET HIGH FROM A LOW STATE, EVENT COUNTER 0'S DATA WILL BE LOADED INTO EXTP 7:0 FLIP-FLOPS. WHEN PDAL4 IS SET TO A ONE AND THE CLK SIGNAL IS SET LOW FROM A HIGH STATE, EVENT COUNTER 0'S DATA WILL BE LOADED INTO EXTP 7:0 FLIP-FLOPS. THE TEST WILL CHECK THAT THE CORRECT DATA IS LOADED INTO EXTP 7:0 FLIP-FLOPS AND THAT THE DATA IS ONLY LOADED ON THE CORRECT TRANSITION OF THE CLK SIGNAL.

EXTP 7:0 FLIP-FLOPS ARE READBACK ON THE TRACE RAM DATA IN BUS SIGNAL LINES TRDI 55:48 WHEN THE SIGNAL TRSL2 L IS ASSERTED LOW.

TEST 65:

THE FOLLOWING TEST WILL CHECK THAT INIT L CAN CLEAR CONTROL REGISTER 2 AND THE LOW BYTE OF CONTROL REGISTER 0. THIS IS DONE BY LOADING ALL ONES INTO CONTROL REGISTER 2 AND THE LOW BYTE OF CONTROL REGISTER 0. THEN A BRESET INSTRUCTION IS ISSUED WHICH SHOULD CLEAR REG 2 AND THE LOW BYTE OF REG 0.

&

```
                                .TITLE PROGRAM HEADER AND TABLES
                                .SBTTL  PROGRAM HEADER

                                        .ENABL  ABS
                                        .ENABL  AMA
                                        .DSABL  GBL
002000                                  .       =       2000

                                        BGNMOD

                                ;++
                                ; THE PROGRAM HEADER IS THE INTERFACE BETWEEN
                                ; THE DIAGNOSTIC PROGRAM AND THE SUPERVISOR.
                                ;--

                                        POINTER BGNSETUP


                                        HEADER  CVCDB,A,0,60.,0,PRI07
002000                  LSNAME::                        ;DIAGNOSTIC NAME
002000  103                             .ASCII /C/
002001  126                             .ASCII /V/
002002  103                             .ASCII /C/
002003  104                             .ASCII /D/
002004  102                             .ASCII /B/
002005  000                             .BYTE   0
002006  000                             .BYTE   0
002007  000                     LSREV::                 ;REVISION LEVEL
002010  101                             .ASCII  /A/
002010                          LSDEPO::                ;0
002011  060                             .ASCII  /0/
002011                          LSUNIT::                ;NUMBER OF UNITS
002012  000001                          .WORD   TSPTHV
002012                          LSTIML::                ;LONGEST TEST TIME
002014  000074                          .WORD   60.
002014                          LSHPCP::                ;POINTER TO H.W. QUES.
002016  037600                          .WORD   LSHARD
002016                          LSSPCP::                ;POINTER TO S.W. QUES.
002020  000000                          .WORD   0
002020                          LSHPTP::                ;PTR. TO DEF. H.W. PTABLE
002022  002330                          .WORD   LSHW
002022                          LSSPTP::                ;PTR. TO S.W. PTABLE
002024  000000                          .WORD   0
002024                          LSLADP::                ;DIAG. END ADDRESS
002026  037742                          .WORD   LSLAST
002026                          LSSTA::                 ;RESERVED FOR APT STATS
002030  000000                          .WORD   0
002030                          LSCO::
002032  000000                          .WORD   0
002032                          LSDTYP::                ;DIAGNOSTIC TYPE
002034  000000                          .WORD   0
002034                          LSAPT::                 ;APT EXPANSION
002036  000000                          .WORD   0
002036                          LSDTP::                 ;PTR. TO DISPATCH TABLE
002040  002124                          .WORD   LSDISPATCH
```

```
1554  002042                    L$PRIO::                ;DIAGNOSTIC RUN PRIORITY
1555  002042  000340                      .WORD   PRI07
1556  002044                    L$ENVI::                ;FLAGS DESCRIBE HOW IT WAS SETUP
1557  002044  000000                      .WORD   0
1558  002046                    L$EXP1::                ;EXPANSION WORD
1559  002046  000000                      .WORD   0
1560  002050                    L$MREV::                ;SVC REV AND EDIT #
1561  002050     003                      .BYTE   C$REVISION
1562  002051     003                      .BYTE   C$EDIT
1563  002052                    L$EF::                  ;DIAG. EVENT FLAGS
1564  002052  000000                      .WORD   0
1565  002054  000000                      .WORD   0
1566  002056                    L$SPC::
1567  002056  000000                      .WORD   0
1568  002060                    L$DEVP::                ; POINTER TO DEVICE TYPE LIST
1569  002060  002424                      .WORD   L$DVTYP
1570  002062                    L$REPP::                ;PTR. TO REPORT CODE
1571  002062  000000                      .WORD   0
1572  002064                    L$EXP4::
1573  002064  000000                      .WORD   0
1574  002066                    L$EXP5::
1575  002066  000000                      .WORD   0
1576  002070                    L$AUT::                 ;PTR. TO ADD UNIT CODE
1577  002070  000000                      .WORD   0
1578  002072                    L$DUT::                 ;PTR. TO DROP UNIT CODE
1579  002072  000000                      .WORD   0
1580  002074                    L$LUN::                 ;LUN FOR EXERCISERS TO FILL
1581  002074  000000                      .WORD   0
1582  002076                    L$DESP::                ;POINTER TO DIAG. DESCRIPTION
1583  002076  002434                      .WORD   L$DESC
1584  002100                    L$LOAD::                ;GENERATE SPECIAL AUTOLOAD EMT
1585  002100  104035                      EMT     E$LOAD
1586  002102                    L$ETP::                 ;POINTER TO EMT TBL
1587  002102  000000                      .WORD   0
1588  002104                    L$ICP::                 ;PTR. TO INIT CODE
1589  002104  006734                      .WORD   L$INIT
1590  002106                    L$CCP::                 ;PTR. TO CLEAN-UP CODE
1591  002106  007122                      .WORD   L$CLEAN
1592  002110                    L$ACP::                 ;PTR. TO AUTO CODE
1593  002110  007120                      .WORD   L$AUTO
1594  002112                    L$PRT::                 ;PTR. TO PROTECT TABLE
1595  002112  006726                      .WORD   L$PROT
1596  002114                    L$TEST::                ;TEST NUMBER
1597  002114  000000                      .WORD   0
1598  002116                    L$DLY::                 ;DELAY COUNT
1599  002116  000000                      .WORD   0
1600  002120                    L$HIME::                ;PTR. TO HIGH MEM
1601  002120  000000                      .WORD   0
1602
```

```
                        .SBTTL  DISPATCH TABLE

                        ;++
                        ; THE DISPATCH TABLE CONTAINS THE STARTING ADDRESS OF EACH TEST.
                        ; IT IS USED BY THE SUPERVISOR TO DISPATCH TO EACH TEST.
                        ;--

002122                          DISPATCH 65.
002122  000101                  .WORD   65
002124                  L$DISPATCH::
002124  007160                  .WORD   T1
002126  007166                  .WORD   T2
002130  007252                  .WORD   T3
002132  007340                  .WORD   T4
002134  007402                  .WORD   T5
002136  007466                  .WORD   T6
002140  007554                  .WORD   T7
002142  007616                  .WORD   T8
002144  007732                  .WORD   T9
002146  010050                  .WORD   T10
002150  010154                  .WORD   T11
002152  010402                  .WORD   T12
002154  010446                  .WORD   T13
002156  010514                  .WORD   T14
002160  010560                  .WORD   T15
002162  010626                  .WORD   T16
002164  010672                  .WORD   T17
002166  010740                  .WORD   T18
002170  011004                  .WORD   T19
002172  011052                  .WORD   T20
002174  011406                  .WORD   T21
002176  011602                  .WORD   T22
002200  011776                  .WORD   T23
002202  012172                  .WORD   T24
002204  012410                  .WORD   T25
002206  013242                  .WORD   T26
002210  014074                  .WORD   T27
002212  014726                  .WORD   T28
002214  015646                  .WORD   T29
002216  016056                  .WORD   T30
002220  016500                  .WORD   T31
002222  017000                  .WORD   T32
002224  017450                  .WORD   T33
002226  017550                  .WORD   T34
002230  017624                  .WORD   T35
002232  020026                  .WORD   T36
002234  020626                  .WORD   T37
002236  021000                  .WORD   T38
002240  021154                  .WORD   T39
002242  021350                  .WORD   T40
002244  021536                  .WORD   T41
002246  021730                  .WORD   T42
002250  022124                  .WORD   T43
002252  022320                  .WORD   T44
002254  022506                  .WORD   T45
002256  022700                  .WORD   T46
```

```
1659  002260  023074                    .WORD   T47
1660  002262  023270                    .WORD   T48
1661  002264  023456                    .WORD   T49
1662  002266  023650                    .WORD   T50
1663  002270  024044                    .WORD   T51
1664  002272  024240                    .WORD   T52
1665  002274  024546                    .WORD   T53
1666  002276  025322                    .WORD   T54
1667  002300  026242                    .WORD   T55
1668  002302  027162                    .WORD   T56
1669  002304  027666                    .WORD   T57
1670  002306  030274                    .WORD   T58
1671  002310  030666                    .WORD   T59
1672  002312  031452                    .WORD   T60
1673  002314  032710                    .WORD   T61
1674  002316  034030                    .WORD   T62
1675  002320  035150                    .WORD   T63
1676  002322  036242                    .WORD   T64
1677  002324  037326                    .WORD   T65
1678
```

```
                                        .SBTTL  DEFAULT HARDWARE P-TABLE

                                        ;++
                                        ; THE DEFAULT HARDWARE P-TABLE CONTAINS DEFAULT VALUES OF
                                        ; THE TEST-DEVICE PARAMETERS.  THE STRUCTURE OF THIS TABLE
                                        ; IS IDENTICAL TO THE STRUCTURE OF THE HARDWARE P-TABLES,
                                        ; AND IS USED AS A "TEMPLATE" FOR BUILDING THE P-TABLES.
                                        ;--

002326                                          BGNHW   DFPTBL
002326  000003                                 .WORD   L10000-L$HW/2
002330                                  L$HW::
002330                                  DFPTBL::

002330  163010                                  .WORD   163010                  ;CSR ADDRESS
002332  000001                                  .WORD   1                       ;DEVICE SELECTION NUMBER
002334  000000                                  .WORD   0                       ;EXTERNAL PROBE INDICATOR (0 = NO)

002336                                          ENDHW
002336                                  L10000:

                                        .SBTTL  SOFTWARE P-TABLE

                                        ;++
                                        ; THE SOFTWARE TABLE CONTAINS VARIOUS DATA USED BY THE
                                        ; PROGRAM AS OPERATIONAL PARAMETERS.  THESE PARAMETERS ARE
                                        ; SET UP AT ASSEMBLY TIME AND MAY BE VARIED BY THE OPERATOR
                                        ; AT RUN TIME.
                                        ;--

002336                                          BGNSW   SFPTBL
002336  000000                                 .WORD   L10001-L$SW/2
002340                                  L$SW::
002340                                  SFPTBL::


002340                                          ENDSW
002340                                  L10001:

002340                                          ENDMOD
```

```
                                .TITLE GLOBAL AREAS
                                .SBTTL  GLOBAL EQUATES SECTION


002340                                  BGNMOD

                                ;++
                                ; THE GLOBAL EQUATES SECTION CONTAINS PROGRAM EQUATES THAT
                                ; ARE USED IN MORE THAN ONE TEST.
                                ;--


002340                                  EQUALS
                                ;
                                ; BIT DIFINITIONS
                                ;
100000                          BIT15== 100000
040000                          BIT14== 40000
020000                          BIT13== 20000
010000                          BIT12== 10000
004000                          BIT11== 4000
002000                          BIT10== 2000
001000                          BIT09== 1000
000400                          BIT08== 400
000200                          BIT07== 200
000100                          BIT06== 100
000040                          BIT05== 40
000020                          BIT04== 20
000010                          BIT03== 10
000004                          BIT02== 4
000002                          BIT01== 2
000001                          BIT00== 1
                                ;
001000                          BIT9==  BIT09
000400                          BIT8==  BIT08
000200                          BIT7==  BIT07
000100                          BIT6==  BIT06
000040                          BIT5==  BIT05
000020                          BIT4==  BIT04
000010                          BIT3==  BIT03
000004                          BIT2==  BIT02
000002                          BIT1==  BIT01
000001                          BIT0==  BIT00
                                ;
                                ; EVENT FLAG DEFINITIONS
                                ;   EF32:EF17 RESERVED FOR SUPERVISOR TO PROGRAM COMMUNICATION
                                ;
000040                          EF.START==      32.             ; START COMMAND WAS ISSUED
000037                          EF.RESTART==    31.             ; RESTART COMMAND WAS ISSUED
000036                          EF.CONTINUE==   30.             ; CONTINUE COMMAND WAS ISSUED
000035                          EF.NEW==        29.             ; A NEW PASS HAS BEEN STARTED
000034                          EF.PWR==        28.             ; A POWER-FAIL/POWER-UP OCCURRED
                                ;
                                ;
                                ; PRIORITY LEVEL DEFINITIONS
                                ;
```

```
1776            000340                  PRI07== 340
1777            000300                  PRI06== 300
1778            000240                  PRI05== 240
1779            000200                  PRI04== 200
1780            000140                  PRI03== 140
1781            000100                  PRI02== 100
1782            000040                  PRI01== 40
1783            000000                  PRI00== 0
1784                                    ;
1785                                    ;OPERATOR FLAG BITS
1786                                    ;
1787            000004                  EVL==       4
1788            000010                  LOT==      10
1789            000020                  ADR==      20
1790            000040                  IDU==      40
1791            000100                  ISR==     100
1792            000200                  UAM==     200
1793            000400                  BOE==     400
1794            001000                  PNT==    1000
1795            002000                  PRI==    2000
1796            004000                  IXE==    4000
1797            010000                  IBE==   10000
1798            020000                  IER==   20000
1799            040000                  LOE==   40000
1800            100000                  HOE==  100000
1801
1802                                    ;
1803                                    ;CONTROL REGISTER 0 (CDAL BITS 15-0)
1804                                    ;
1805
1806            100000                  CDAL15==BIT15                   ;BIT15=1 READ DEVICE TYPE IN 15-8
1807                                                                    ;ED DEVICE TYPE EQUALS 1000 (BIT9=1)
1808                                                                    ;
1809                                                                    ;BIT15=0 READ DEVICE NUMBER INTO
1810                                                                    ;BITS 11-8
1811
1812            040000                  CDAL14==BIT14                   ;ALWAYS A 0 ON READ
1813            020000                  CDAL13==BIT13                   ;ALWAYS A 0 ON READ
1814            010000                  CDAL12==BIT12                   ;ALWAYS A 0 ON READ
1815
1816            004000                  CDAL11==BIT11                   ;BITS 11-8 ARE USED TO SELECT THE
1817            002000                  CDAL10==BIT10                   ;DEVICE NUMBER TO ASSERT THE SIGNAL
1818            001000                  CDAL9== BIT9                    ;DEVE L. WHEN SELECTING ED THESE BITS
1819            000400                  CDAL8== BIT8                    ;MUST = THE SETTING OF DEV 3 - DEV 0
1820
1821            000200                  CDAL7== BIT7                    ;1 - DISABLE OUTPUTS OF OR ADDRESS REG
1822                                                                    ;    ENABLE FOUT 3:0 TO DRIVE OR ADDRESS
1823                                                                    ;0 - ENABLE OUTPUTS OF OR ADDRESS REG
1824
1825            000100                  CDAL6== BIT6                    ;1/0 - CLOCK SIGNAL "TRNST H"
1826
1827            000040                  CDAL5== BIT5                    ;1 - STOP TRACING WHEN TRAD10 H SET HIGH
1828                                                                    ;0 - CONTINUOS TRACING
1829
1830            000020                  CDAL4== BIT4                    ;1 - ENABLE ALL AND/OR ARRAY RAMS
1831                                                                    ;0 - ENABLE ONLY ONE AND/OR ARRAY RAMS
```

```
1832
1833          000010                  CDAL3== BIT3                    ;TRACE RAM BUS SELECT
1834          000004                  CDAL2== BIT2                    ;TRACE RAM BUS SELECT
1835
1836          000002                  CDAL1== BIT1                    ;ENABLE FUNCTION SELECTS ONTO SYSTEM BUS
1837
1838          000001                  CDAL0== BIT0                    ;1/0 - ZERO TRAM ADDRESS REG, TRACING
1839                                                                  ;     FLIP-FLOP AND SBL FLIP-FLOPS 59:56.
1840                                                                  ;     LOAD EVNT CNTR'S VIA EVNT CNTR REG.
1841
1842                                  ;
1843                                  ;CONTROL REGISTER 2 (PDAL BITS 7-0)
1844                                  ;
1845
1846                                                                  ;BITS 15-8 ARE UNUSED BITS
1847
1848          000200                  PDAL7== BIT7                    ;1 - CLEAR EVENT COUNTERS
1849          000100                  PDAL6== BIT6                    ;1 - PRESET TRACING FLIP-FLOP
1850          000040                  PDAL5== BIT5                    ;0 - CLEAR FUNCTION SELECT FLIP-FLOPS
1851          000020                  PDAL4== BIT4                    ;1 - EXTERNAL PROBE "CLK" SIGNAL WILL
1852                                                                  ;     LOAD EXTP 7:0 F/F'S WHEN "CLK" SET LOW
1853                                                                  ;0 - EXTERNAL PROBE "CLK" SIGNAL WILL
1854                                                                  ;     LOAD EXTP 7:0 F/F'S WHEN "CLK" SET HIGH
1855          000010                  PDAL3== BIT3                    ;SELECTS POINTER REGISTER (SEE BELOW)
1856          000004                  PDAL2== BIT2                    ;SELECTS POINTER REGISTER (SEE BELOW)
1857          000002                  PDAL1== BIT1                    ;SELECTS POINTER REGISTER (SEE BELOW)
1858          000001                  PDAL0== BIT0                    ;SELECTS POINTER REGISTER (SEE BELOW)
1859
1860                                  ;
1861                                  ;POINTER REGISTER PTER 15-0 (SELECTED BY PDAL 3-0)
1862                                  ;
1863
1864          000000                  PTER0== 0                       ;WPT0,RPT0,R/W TRAM ADDRESS (9-0)
1865          000001                  PTER1== PDAL0                   ;WPT1,RPT1,R/W TRAM DATA LSI-11 TO TRDI (15-0)
1866          000002                  PTER2== PDAL1                   ;WPT2,RPT2,R/W TRAM DATA LSI-11 TO TRDI (31-16)
1867          000003                  PTER3== PDAL1!PDAL0             ;WPT3,RPT3,R/W TRAM DATA LSI-11 TO TRDI (47-32)
1868          000004                  PTER4== PDAL2                   ;WPT4,RPT4,R/W TRAM DATA LSI-11 TO TRDI (59-48)
1869          000005                  PTER5== PDAL2!PDAL0             ;WPT5,WRITE TRACE RAM DATA IN BUF (15-0)
1870          000006                  PTER6== PDAL2!PDAL1             ;WPT6,WRITE TRACE RAM DATA IN BUF (31-16)
1871          000007                  PTER7== PDAL2!PDAL1!PDAL0       ;WPT7,WRITE TRACE RAM DATA IN BUF (47-32)
1872          000010                  PTER8== PDAL3                   ;WPT8,WRITE TRACE RAM DATA IN BUF (59-48)
1873          000011                  PTER9== PDAL3!PDAL0             ;WPT9,LOAD EVENT COUNTER 0
1874          000012                  PTER10==PDAL3!PDAL1             ;WPT10,LOAD EVENT COUNTER 1
1875          000013                  PTER11==PDAL3!PDAL1!PDAL0       ;WPT11,LOAD EVENT COUNTER 2
1876          000014                  PTER12==PDAL3!PDAL2             ;WPT12,LOAD EVENT COUNTER 3
1877          000015                  PTER13==PDAL3!PDAL2.PDAL0       ;NOT USED
1878          000016                  PTER14==PDAL3!PDAL2!PDAL1       ;NOT USED
1879          000017                  PTER15==PDAL3!PDAL2!PDAL1!PDAL0 ;WPT15,RPT15,R/W "OR" ADDRESS
1880
1881
```

```
                        .SBTTL  GLOBAL DATA SECTION

                        ;++
                        ; THE GLOBAL DATA SECTION CONTAINS DATA THAT ARE USED
                        ; IN MORE THAN ONE TEST.
                        ;--


                                ERRTBL
002340                  L$ERRTBL::
002340  000000          ERRTYP::        .WORD   0
002342  000000          ERRNBR::        .WORD   0
002344  000000          ERRMSG::        .WORD   0
002346  000000          ERRBLK::        .WORD   0

                        ;
                        ;GLOBAL DATA FOR STATE ANALYZER          .
                        ;
002350  163010          REG0::  .WORD   163010          ;CONTROL REGISTER 0
002352  163012          REG2::  .WORD   163012          ;CONTROL REGISTER 2
002354  163014          REG4::  .WORD   163014          ;CONTROL REGISTER 4
002356  163016          REG6::  .WORD   163016          ;CONTROL REGISTER

002360  000000          IDDEV:: .WORD   0               ;STATE ANALYZER DEVICE # (11-8)
002362  000000          UNITNB::.WORD   0               ;
002364  000000          IDTYPE::.WORD   0               ;STATE ANALYZER DEVICE TYPE (15-8)
002366  000000          EXTPRB::.WORD   0               ;EXTERNAL PROBE INDICATOR (0 = NO PROBE)

002370  000000          R0LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 0
002372  000000          R0GOOD::.WORD   0               ;EXPECTED REG 0
002374  000000          R0READ::.WORD   0               ;ACTUAL REG 0 READ

002376  000000          R2LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 2
002400  000000          R2READ::.WORD   0               ;ACTUAL REG 2 READ

002402  000000          R4LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 4
002404  000000          R4GOOD::.WORD   0               ;EXPECTED DATA FROM REGISTER 4
002406  000000          R4MASK::.WORD   0               ;BITS TO BE IGNORED ON COMPARE
002410  000000          R4READ::.WORD   0               ;WORD READ OUT OF REGISTER 4
002412  000000          R4BAD:: .WORD   0               ;DATA READ MASKED WITH R4MASK

002414  000000          R6LOAD::.WORD   0               ;WORD LOADED INTO REGISTER 6
002416  000000          R6MASK::.WORD   0               ;REGISTER 6 MASK WORD
002420  000000          R6READ::.WORD   0               ;ACTUAL REGISTER 6 READ
002422  000000          R6BAD:: .WORD   0               ;REG 6 READ MINUS MASK WORD
```

```
                                        .SBTTL  GLOBAL TEXT SECTION

                                        ;++
                                        ; THE GLOBAL TEXT SECTION CONTAINS FORMAT STATEMENTS,
                                        ; MESSAGES, AND ASCII INFORMATION THAT ARE USED IN
                                        ; MORE THAN ONE TEST.
                                        ;--

                                        ;
                                        ; NAMES OF DEVICES SUPPORTED BY PROGRAM
                                        ;
002424                                          DEVTYP  <CDS-11>
002424                                  L$DVTYP::
002424  042103  026523  030461                   .ASCIZ  /CDS-11/
002432     000
        002434                                  .EVEN

                                        ; TEST DESCRIPTION
                                        ;
002434                                          DESCRIPT        <STATE ANALYZER DIAG.>
002434                                  L$DESC::
002434  052123  052101  020105                   .ASCIZ  /STATE ANALYZER DIAG./
002442  047101  046101  055131
002450  051105  042040  040511
002456  027107     000
        002462                                  .EVEN


                                        ;ASCII MESSAGES USED BY ERROR CALLS - CONTROL REGISTER 6
                                        ;

002462  051124  046501  040440  TRADER::.ASCIZ  /TRAM ADDRESS REG - TRAD 10:0/
002470  042104  042522  051523
002476  051040  043505  026440
002504  052040  040522  020104
002512  030061  030072     000
002517     124  040522  020115  TRDI15:.ASCIZ  /TRAM DATA IN BUF - TRDI 15:0/
002524  040504  040524  044440
002532  020116  052502  020106
002540  020055  051124  044504
002546  030440  035065  000060
002554  051124  046501  042040  TRDI31:.ASCIZ  /TRAM DATA IN BUF - TRDI 31:16/
002562  052101  020101  047111
002570  041040  043125  026440
002576  052040  042122  020111
002604  030463  030472  000066
002612  051124  046501  042040  TRDI47:.ASCIZ  /TRAM DATA IN BUF - TRDI 47:32/
002620  052101  020101  047111
002626  041040  043125  026440
002634  052040  042122  020111
002642  033464  031472  000062
002650  051124  046501  042040  TRDI59::.ASCIZ  /TRAM DATA IN BUF - TRDI 59:48/
002656  052101  020101  047111
002664  041040  043125  026440
```

```
1984  002672  052040  042122  020111
1985  002700  034465  032072  000070
1986  002706  051124  046501  042040  TRDIER::.ASCIZ  /TRAM DATA IN BUF - TRDI 59:0/
1987  002714  052101  020101  047111
1988  002722  041040  043125  026440
1989  002730  052040  042122  020111
1990  002736  034465  030072     000
1991  002743     124  040522  020 15  TRDISE::.ASCIZ  /TRAM DATA IN BUF SELECTION/
1992  002750  04  04  040524  044440
1993  002756  020116  052502  020106
1994  002764  042523  042514  052103
1995  002772  047511  000116
1996  002776  051124  046501  042040  TRAM15::.ASCIZ  /TRAM DATA ERROR - TRDI 15:0/
1997  003004  052101  020101  051105
1998  003012  047522  020122  020055
1999  003020  051124  044504  030440
2000  003026  035065  000060
2001  003032  051124  046501  042040  TRAM31::.ASCIZ  /TRAM DATA ERROR - TRDI 31:16/
2002  003040  052101  020101  051105
2003  003046  047522  020122  020055
2004  003054  051124  044504  031440
2005  003062  035061  033061     000
2006  003067     124  040522  020115  TRAM47::.ASCIZ  /TRAM DATA ERROR - TRDI 47:32/
2007  003074  040504  040524  042440
2008  003102  051122  051117  026440
2009  003110  052040  042122  020111
2010  003116  033464  031472  000062
2011  003124  051124  046501  04  40  TRAM55::.ASCIZ  /TRAM DATA ERROR - TRDI 55:48/
2012  003132  052101  020101  051105
2013  003140  047522  020122  020055
2014  003146  051124  044504  032440
2015  003154  035065  034064     000
2016  003161     117  020122  042101  ORADER::.ASCIZ  /OR ADDRESS REG - ORAD 3:0/
2017  003166  051104  051505  020123
2018  003174  042522  020107  020055
2019  003202  051117  042101  031440
2020  003210  030072     000
2021  003213     105  042526  052116  EVNTCT::.ASCIZ  /EVENT COUNTERS OR FOUT 3:0 ERROR/
2022  003220  041440  052517  052116
2023  003226  051105  020123  051117
2024  003234  043040  052517  020124
2025  003242  035063  020060  051105
2026  003250  047522  000122
2027  003254  042120  046101  020067  EVNTCL::.ASCIZ  /PDAL7 FAILED TO CLEAR EVENT COUNTERS/
2028  003262  040506  046111  042105
2029  003270  052040  020117  046103
2030  003276  040505  020122  053105
2031  003304  047105  020124  047503
2032  003312  047125  042524  051522
2033  003320     000
2034  003321     103  040504  030114  EVNTRL::.ASCIZ  /CDAL0 FAILED TO LOAD EVENT COUNTERS/
2035  003326  043040  044501  042514
2036  003334  020104  047524  046040
2037  003342  040517  020104  053105
2038  003350  047105  020124  047503
2039  003356  047125  042524  051522
```

```
2040  003364     000
2041  003365     106  051525  020114  FUSL30::.ASCIZ  /FUSL 3:0 FLIP-FLOP ERROR/
2042  003372  035063  020060  046106
2043  003400  050111  043055  047514
2044  003406  020120  051105  047522
2045  003414  000122
2046  003416  041123  020114  034465  SBLERR::.ASCIZ  /SBL 59:56 FLIP-FLOP ERROR/
2047  003424  032472  020066  046106
2048  003432  050111  043055  047514
2049  003440  020120  051105  047522
2050  003446  000122
2051  003450  054105  050124  033440  EXTPER::.ASCIZ  /EXTP 7:0 FLIP-FLOP OR LOGIC ERROR/
2052  003456  030072  043040  044514
2053  003464  026520  046106  050117
2054  003472  047440  020122  047514
2055  003500  044507  020103  051105
2056  003506  047522  000122
2057
2058                                  ;
2059                                  ;ASCII MESSAGES USED BY ERROR CALLS - CONTROL REGISTER 4
2060                                  ;
2061
2062  003512  051117  040440  051122  ORDATA::.ASCIZ  /OR ARRAY DATA ERROR - ORO 7:0/
2063  003520  054501  042040  052101
2064  003526  020101  051105  047522
2065  003534  020122  020055  051117
2066  003542  020117  035067  000060
2067  003550  047101  020104  051101  ANDERR::.ASCIZ  /AND ARRAY RAM DATA ERROR/
2068  003556  040522  020131  040522
2069  003564  020115  040504  040524
2070  003572  042440  051122  051117
2071  003600     000
2072  003601     106  051525  033514  FUSL7:: .ASCIZ  /FUSL7 FLIP-FLOP - OR ARRAY DATA ERROR/
2073  003606  043040  044514  026520
2074  003614  046106  050117  026440
2075  003622  047440  020122  051101
2076  003630  040522  020131  040504
2077  003636  040524  042440  051122
2078  003644  051117     000
2079  003647     101  042116  026440  ANDOR::.ASCIZ   /AND - OR ARRAY DATA ERROR/
2080  003654  047440  020122  051101
2081  003662  040522  020131  040504
2082  003670  040524  042440  051122
2083  003676  051117     000
2084
2085          003702                          .EVEN
2086
2087
2088                                  ;
2089                                  ; FORMAT STATEMENTS USED IN PRINT CALLS
2090                                  ;
2091
2092  003702  040445  047503  052116  EMSGR0::.ASCIZ  /%ACONTROL REG 0 ERROR%N/
2093  003710  047522  020114  042522
2094  003716  020107  020060  051105
2095  003724  047522  022522  000116
```

```
2096  003732  040445  047503  052116  EMSGR2::.ASCIZ  /%ACONTROL REG 2 ERROR%N/
2097  003740  047522  020114  042522
2098  003746  020107  020062  051105
2099  003754  047522  022522  000116
2100  003762  040445  047503  052116  EMSGR4::.ASCIZ  /%ACONTROL REG 4 ERROR%N/
2101  003770  047522  020114  042522
2102  003776  020107  020064  051105
2103  004004  047522  022522  000116
2104  004012  040445  047503  052116  EMSGR6::.ASCIZ  /%ACONTROL REG 6 ERROR%N/
2105  004020  047522  020114  042522
2106  004026  020107  020066  051105
2107  004034  047522  022522  000116
2108  004042  040445  042522  030107  REG0EQ::.ASCIZ  /%AREG0 = /
2109  004050  036440  000040
2110  004054  040445  042522  031107  REG2EQ::.ASCIZ  /%AREG2 = /
2111  004062  036440  000040
2112  004066  040445  042522  032107  REG4EQ::.ASCIZ  /%AREG4 = /
2113  004074  036440  000040
2114  004100  040445  042522  033107  REG6EQ::.ASCIZ  /%AREG6 = /
2115  004106  036440  000040
2116  004112  040445  051124  046501  MSGTRM::.ASCIZ  /%ATRAM ADDRESS REG = %06%N/
2117  004120  040440  042104  042522
2118  004126  051523  051040  043505
2119  004134  036440  022440  033117
2120  004142  047045     000
2121  004145     045  046101  040517  FRMTOR::.ASCIZ  /%ALOAD: %06%S1%AREAD: %06%S1%AGOOD: %06%N/
2122  004152  035104  022440  033117
2123  004160  051445  022461  051101
2124  004166  040505  035104  022440
2125  004174  033117  051445  022461
2126  004202  043501  047517  035104
2127  004210  022440  033117  047045
2128  004216     000
2129  004217     045  046101  040517  FRMTR0::.ASCIZ  /%ALOAD: %06%S1%AREAD: %06%N/
2130  004224  035104  022440  033117
2131  004232  051445  022461  051101
2132  004240  040505  035104  022440
2133  004246  033117  047045     000
2134
2135  004253     045  046101  040517  FRMTR4::.ASCIZ  /%ALOAD: %06%S1%AREAD: %06%S1%AMASK: %06%S1%AGCOD: %06%S1%ABAD: %06%N/
2136  004260  035104  022440  033117
2137  004266  051445  022461  051101
2138  004274  040505  035104  022440
2139  004302  033117  051445  022461
2140  004310  046501  051501  035113
2141  004316  022440  033117  051445
2142  004324  022461  043501  047517
2143  004332  035104  022440  033117
2144  004340  051445  022461  041101
2145  004346  042101  020072  047445
2146  004354  022466  000116
2147  004360  040445  053105  052116  FRMTEC::.ASCIZ  /%AEVNT CNT LOADED: %06%S1%AEVNT CNT BEFORE CNT DOWN: %06%N/
2148  004366  041440  052116  046040
2149  004374  040517  042504  035104
2150  004402  022440  033117  051445
2151  004410  022461  042501  047126
```

```
2152  004416  020124  047103  020124
2153  004424  042502  047506  042522
2154  004432  041440  052116  042040
2155  004440  053517  035116  022440
2156  004446  033117  047045     000
2157  004453     045  052101  046511  MSGTMC::.ASCIZ  /%ATIME OUT ERROR ADDRESSING CONTROL REG 0%N/
2158  004460  020105  052517  020124
2159  004466  051105  047522  020122
2160  004474  042101  051104  051505
2161  004502  044523  043516  041440
2162  004510  047117  051124  046117
2163  004516  051040  043505  030040
2164  004524  047045     000
2165  004527     045  052101  046511  MSGTM2::.ASCIZ  /%ATIME OUT ERROR ADDRESSING CONTROL REG 2%N/
2166  004534  020105  052517  020124
2167  004542  051105  047522  020122
2168  004550  042101  051104  051505
2169  004556  044523  043516  041440
2170  004564  047117  051124  046117
2171  004572  051040  043505  031040
2172  004600  047045     000
2173
2174
2175          004604                      .EVEN
2176
2177
2178
```

```
                                .SBTTL  GLOBAL ERROR REPORT SECTION

                                ;++
                                ; THE GLOBAL ERROR REPORT SECTION CONTAINS MESSAGE PRINTING AREAS
                                ; USED BY MORE THAN TEST TO OUTPUT ADDITIONAL ERROR INFORMATION.  PRINTB
                                ; (BASIC) AND PRINTX (EXTENDED) CALLS ARE USED TO CALL PRINT SERVICES.
                                ;--


004604                                  BGNMSG  ROEROR
004604                          ROEROR::
004604  004537  005130                  JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
004610  003702                          .WORD   EMSGR0
004612  004737  005210                  JSR     PC,PRNTR0               ;GO PRINT CONTROL REGISTER 0 INFO



004616                                  ENDMSG
004616                          L10002:
004616  104423                          TRAP    C$MSG

004620                                  BGNMSG  ERORR0
004620                          ERORR0::
004620  004537  005130                  JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
004624  003702                          .WORD   EMSGR0
004626                                  PRINTX  #REGOEQ
004626  012746  004042                  MOV     #REGOEQ,-(SP)
004632  012746  000001                  MOV     #1,-(SP)
004636  010600                          MOV     SP,R0
004640  104415                          TRAP    C$PNTX
004642  062706  000004                  ADD     #4,SP
004646                                  PRINTX  #FRMTOR,ROLOAD,ROREAD,ROGOOD
004646  013746  002372                  MOV     ROGOOD,-(SP)
004652  013746  002374                  MOV     ROREAD,-(SP)
004656  013746  002370                  MOV     ROLOAD,-(SP)
004662  012746  004145                  MOV     #FRMTOR,-(SP)
004666  012746  000004                  MOV     #4,-(SP)
004672  010600                          MOV     SP,R0
004674  104415                          TRAP    C$PNTX
004676  062706  000012                  ADD     #12,SP
004702                                  ENDMSG
004702                          L10003:
004702  104423                          TRAP    C$MSG

004704                                  BGNMSG  R2EROR
004704                          R2EROR::
004704  004537  005130                  JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
004710  003732                          .WORD   EMSGR2
004712  004737  005262                  JSR     PC,PRNTR2               ;GO PRINT CONTROL REGISTER 2 INFO
004716                                  ENDMSG
004716                          L10004:
004716  104423                          TRAP    C$MSG

                                        BGNMSG  R[illegible]ROR
```

```
2235  004720
2236  004720  004537  005130          R4EROR::
2237  004724  003762                          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2238  004726  004737  005150                  .WORD   EMSGR4
2239  004732                                  JSR     PC,PRNTAL               ;GO PRINT ALL REGISTERS
2240  004732                                  ENDMSG
2241  004732  104423                  L10005:
2242                                          TRAP    C$MSG
2243  004734
2244  004734                                  BGNMSG  R026ER
2245  004734  004537  005130          R026ER::
2246  004740  004012                          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2247  004742  004737  005172                  .WORD   EMSGR6
2248  004746                                  JSR     PC,PR026R
2249  004746                                  ENDMSG
2250  004746  104423                  L10006:
2251                                          TRAP    C$MSG
2252  004750
2253  004750                                  BGNMSG  ALLREG
2254  004750  004537  005130          ALLREG::
2255  004754  004012                          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2256  004756  004737  005150                  .WORD   EMSGR6
2257  004762                                  JSR     PC,PRNTAL
2258  004762                                  ENDMSG
2259  004762  104423                  L10007:
2260                                          TRAP    C$MSG
2261  004764
2262  004764                                  BGNMSG  TRAMER
2263  004764  004537  005130          TRAMER::
2264  004770  004012                          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2265  004772                                  .WORD   EMSGR6
2266  004772  013746  006374                  PRINTB  #MSGTRM,TRADRS
2267  004776  012746  004112                  MOV     TRADRS,-(SP)
2268  005002  012746  000002                  MOV     #MSGTRM,-(SP)
2269  005006  010600                          MOV     #2,-(SP)
2270  005010  104 .4                          MOV     SP,R0
2271  005012  062706  000006                  TRAP    C$PNTB
2272  005016  004737  005172                  ADD     #6,SP
2273  005022                                  JSR     PC,PR026R
2274  005022                                  ENDMSG
2275  005022  104423                  L10010:
2276                                          TRAP    C$MSG
2277  005024
2278  005024                                  BGNMSG  EVNTER
2279  005024  004537  005130          EVNTER::
2280  005030  004012                          JSR     R5,PRNTBS               ;GO PRINT CONTROL REG THAT FAILED
2281  005032                                  .WORD   EMSGR6
2282  005032  010246                          PRINTX  #FRM EC,R1,R2
2283  005034  010146                          MOV     R2,-(SP)
2284  005036  012746  004360                  MOV     R1,-(SP)
2285  005042  012746  000003                  MOV     #FRMTEC,-(SP)
2286  005046  010600                          MOV     #3,-(SP)
2287  005050  104415                          MOV     SP,R0
2288  005052  062706  000010                  TRAP    C$PNTX
2289  005056  004737  005150                  ADD     #10,SP
2290  005062                                  JSR     PC,PRNTAL
                                              ENDMSG
```

```
2291  005062
2292  005062  104423                  L10011:
2293  005064                                  TRAP    C$MSG
2294  005064                                  BGNMSG  ROTM
2295  005064                          ROTM::
2296  005064  012746  004453                 PRINTB  #MSGTM0
2297  005070  012746  000001                 MOV     #MSGTM0,-(SP)
2298  005074  010600                         MOV     #1,-(SP)
2299  005076  104414                         MOV     SP,R0
2300  005100  062706  000004                 TRAP    C$PNTB
2301  005104                                  ADD     #4,SP
2302  005104                                  ENDMSG
2303  005104  104423                  L10012:
2304                                          TRAP    C$MSG
2305  005106
2306  005106                                  BGNMSG  R2TM
2307  005106                          R2TM::
2308  005106  012746  004453                 PRINTB  #MSGTM0
2309  005112  012746  000001                 MOV     #MSGTM0,-(SP)
2310  005116  010600                         MOV     #1,-(SP)
2311  005120  104414                         MOV     SP,R0
2312  005122  062706  000004                 TRAP    C$PNTB
2313  005126                                  ADD     #4,SP
2314  005126                                  ENDMSG
2315  005126  104423                  L10013:
2316                                          TRAP    C$MSG
2317
2318                                  ;ROUTINE TO PRINT WHAT CONTROL REGISTER DETECTED THE ERROR.
2319  005130
2320  005130  012546                  PRNTBS::PRINTB  (R5)+
2321  005132  012746  000001                 MOV     (R5)+,-(SP)
2322  005136  010600                         MOV     #1,-(SP)
2323  005140  104414                         MOV     SP,R0
2324  005142  062706  000004                 TRAP    C$PNTB
2325  005146  000205                         ADD     #4,SP
2326                                          RTS     R5
2327
2328                                  ;ROUTINE TO PRINT ALL CONTROL REGISTER ERROR INFORMATION
2329
2330  005150  004737  005210  PRNTAL::JSR     PC,PRNTR0               ;GO PRINT CONTROL REGISTER 0 INFO
2331  005154  004737  005262          JSR     PC,PRNTR2               ;GO PRINT CONTROL REGISTER 2 INFO
2332  005160  004737  005334          JSR     PC,PRNTR4               ;GO PRINT CONTROL REGISTER 4 INFO
2333  005164  004737  005422          JSR     PC,PRNTR6               ;GO PRINT CONTROL REGISTER 6 INFO
2334  005170  000207                  RTS     PC
2335
2336                                  ;ROUTINE TO PRINT CONTROL REGISTER 0, 2 AND 6 ERROR INFORMATION
2337
2338  005172  004737  005210  PR026R::JSR     PC,PRNTR0               ;GO PRINT CONTROL REGISTER 0 INFO
2339  005176  004737  005262          JSR     PC,PRNTR2               ;GO PRINT CONTROL REGISTER 2 INFO
2340  005202  004737  005422          JSR     PC,PRNTR6               ;GO PRINT CONTROL REGISTER 6 INFO
2341  005206  000207                  RTS     PC
2342
2343                                  ;PRINT CONTROL REGISTER 0 ERROR INFORMATION
2344
2345  005210                          PRNTR0::PRINTX  #REGOEQ
2346  005210  012746  004042                 MOV     #REGOEQ,-(SP)
```

```
2347  005214  012746  000001                  MOV     #1,-(SP)
2348  005220  010600                          MOV     SP,R0
2349  005222  104415                          TRAP    C$PNTX
2350  005224  062706  000004                  ADD     #4,SP
2351  005230                                  PRINTX  #FRMTR0,R0LOAD,R0READ
2352  005230  013746  002374                  MOV     R0READ,-(SP)
2353  005234  013746  002370                  MOV     R0LOAD,-(SP)
2354  005240  012746  004217                  MOV     #FRMTR0,-(SP)
2355  005244  012746  000003                  MOV     #3,-(SP)
2356  005250  010600                          MOV     SP,R0
2357  005252  104415                          TRAP    C$PNTX
2358  005254  062706  000010                  ADD     #10,SP
2359  005260  000207                          RTS     PC
2360
2361                                  ;PRINT CONTROL REGISTER 2 ERROR INFORMATION
2362
2363  005262                          PRNTR2::PRINTX  #REG2EQ
2364  005262  012746  004054                  MOV     #REG2EQ,-(SP)
2365  005266  012746  000001                  MOV     #1,-(SP)
2366  005272  010600                          MOV     SP,R0
2367  005274  104415                          TRAP    C$PNTX
2368  005276  062706  000004                  ADD     #4,SP
2369  005302                                  PRINTX  #FRMTR0,R2LOAD,R2READ
2370  005302  013746  002400                  MOV     R2READ,-(SP)
2371  005306  013746  002376                  MOV     R2LOAD,-(SP)
2372  005312  012746  004217                  MOV     #FRMTR0,-(SP)
2373  005316  012746  000003                  MOV     #3,-(SP)
2374  005322  010600                          MOV     SP,R0
2375  005324  104415                          TRAP    C$PNTX
2376  005326  062706  000010                  ADD     #10,SP
2377  005332  000207                          RTS     PC
2378
2379                                  ;PRINT CONTROL REGISTER 4 ERROR INFORMATION
2380
2381  005334                          PRNTR4::PRINTX  #REG4EQ
2382  005334  012746  004066                  MOV     #REG4EQ,-(SP)
2383  005340  012746  000001                  MOV     #1,-(SP)
2384  005344  010600                          MOV     SP,R0
2385  005346  104415                          TRAP    C$PNTX
2386  005350  062706  000004                  ADD     #4,SP
2387  005354                                  PRINTX  #FRMTR4,R4LOAD,R4READ,R4MASK,R4GOOD,R4BAD
2388  005354  013746  002412                  MOV     R4BAD,-(SP)
2389  005360  013746  002404                  MOV     R4GOOD,-(SP)
2390  005364  013746  002406                  MOV     R4MASK,-(SP)
2391  005370  013746  002410                  MOV     R4READ,-(SP)
2392  005374  013746  002402                  MOV     R4LOAD,-(SP)
2393  005400  012746  004253                  MOV     #FRMTR4,-(SP)
2394  005404  012746  000006                  MOV     #6,-(SP)
2395  005410  010600                          MOV     SP,R0
2396  005412  104415                          TRAP    C$PNTX
2397  005414  062706  000016                  ADD     #16,SP
2398  005420  000207                          RTS     PC
2399
```

```
2400
2401                                    ;PRINT CONTROL REGISTER 6 ERROR INFORMATION
2402
2403  005422                            PRNTR6::PRINTX  #REG6EQ
2404  005422  012746  004100                    MOV     #REG6EQ,-(SP)
2405  005426  012746  000001                    MOV     #1,-(SP)
2406  005432  010600                            MOV     SP,R0
2407  005434  104415                            TRAP    C$PNTX
2408  005436  062706  000004                    ADD     #4,SP
2409  005442                                    PRINTX  #FRMTR0,R6LOAD,R6READ
2410  005442  013746  002420                    MOV     R6READ,-(SP)
2411  005446  013746  002414                    MOV     R6LOAD,-(SP)
2412  005452  012746  004217                    MOV     #FRMTR0,-(SP)
2413  005456  012746  000003                    MOV     #3,-(SP)
2414  005462  010600                            MOV     SP,R0
2415  005464  104415                            TRAP    C$PNTX
2416  005466  062706  000010                    ADD     #10,SP
2417  005472  000207                            RTS     PC
2418
```

```
                                .SBTTL  GLOBAL SUBROUTINES SECTION

                                ;++
                                ; THE GLOBAL SUBROUTINES SECTION CONTAINS THE SUBROUTINES
                                ; THAT ARE USED IN MORE THAN ONE TEST.
                                ;--

                                ;++
                                ; FUNCTIONAL DESCRIPTION:
                                ;    SUBROUTINE TO....SELECT AND INITIALIZE STATE ANALYZER


                                ; INPUTS:
                                ;    LOCATION IDDEV CONTAINS USER DEFINED DEVICE NUMBER IN BITS 11-8



                                ; IMPLICIT INPUTS:


                                ; OUTPUTS:
                                ;    ROLOAD CONTAINS USER DEFINED UNIT NUMBER IN BITS 11-8
                                ;    ROMASK CONTAINS CONTROL REGISTER 0 MASK WORD (000200)
                                ;    R2LOAD CONTAINS ALL ZEROES TO INDICATE CONTROL REGISTER 2 WAS CLEARED


                                ; IMPLICIT OUTPUTS:


                                ; SUBORDINATE ROUTINES USED:
                                ;    LDRDR0 ROUTINE TO LOAD, READ AND COMPARE REGISTER 0
                                ;    LDRDOR ROUTINE TO LOAD, READ AND COMPARE REGISTER 0 (USED FOR DEVICE TYPE)
                                ;    LDRDR2 ROUTINE TO LOAD, READ AND COMPARE CONTROL REGISTER 2


                                ; FUNCTIONAL SIDE EFFECTS:
                                ;    STATE ANALYZER SELECTED
                                ;    CONTROL REGISTER 0 LOW BYTE EQUALS 0
                                ;    CONTROL REGISTER 2 EQUALS 0


                                ; CALLING SEQUENCE:
                                ;    JSR PC,INITED

                                ;--


005474                          INITED::BGNSEG                          ;ROUTINE TO INIT ED MODULE
005474  104404                          TRAP    C$BSEG
005476                                  SETVEC  #4,#1$,#PR107           ;SETUP VECTOR
005476  012746  000340                   MOV     #PR107,-(SP)
005502  012746  005600                   MOV     #1$,-(SP)
005506  012746  000004                   MOV     #4,-(SP)
005512  012746  000003                   MOV     #3,-(SP)
005516  104437                          TRAP    C$SVEC
```

```
2475  005520  062706  000010                ADD     #10.SP
2476
2477                                        ;LOAD DEVICE NUMBER INTO REGISTER 0 AND CHECK IT
2478
2479  005524  013737  002360  002370        MOV     IDDEV,ROLOAD            ;GET USER DEFINED DEVICE NUMBER
2480  005532  013737  002370  002372        MOV     ROLOAD,ROGOOD           ;PUT DATA LOADED INTO  EXPECTED
2481  005540  013777  002370  174602        MOV     ROLOAD,@#REG0           ;WRITE WORD TO REGISTER 0
2482  005546  017737  174576  002374        MOV     @#REG0,ROREAD           ;READ REGISTER CONTENTS BACK
2483  005554  023737  002372  002374        CMP     ROGOOD,ROREAD           ;COMPARE EXPECTED WITH THAT READ
2484  005562  001414                        BEQ     2$                      ;IF COMPARE WAS GOOD THEN CONT
2485  005564                                ERRDF   1,,ROEROR               ;REG 0 NOT EQUAL EXPECTED
2486  005564  104455                        TRAP    C$ERDF
2487  005566  000001                        .WORD   1
2488  005570  000000                        .WORD   0
2489  005572  004604                        .WORD   ROEROR
2490  005574                                CKLOOP
2491  005574  104406                        TRAP    C$CLP1
2492  005576  000406                        BR      2$                      ;BRANCH AROUND TIME OUT ERROR
2493  005600  005726              1$:       TST     (SP)+                   ;CLEAN UP STACK
2494  005602  005726                        TST     (SP)+                   ;CLEAN UP STACK
2495  005604                                ERRDF   1,,ROTM                 ;TIME OUT ERROR REG 0
2496  005604  104455                        TRAP    C$ERDF
2497  005606  000001                        .WORD   1
2498  005610  000000                        .WORD   0
2499  005612  005064                        .WORD   ROTM
2500  005614                        2$:     CLRVEC  #4                      ;CLEAR VECTOR
2501  005614  012700  000004                MOV     #4,R0
2502  005620  104436                        TRAP    C$CVEC
2503  005622                                ENDSEG
2504  005622                        10000$:
2505  005622  104405                        TRAP    C$ESEG
2506
2507                                        ;READ DEVICE TYPE IN REGISTER 0
2508
2509  005624                                BGNSEG
2510  005624  104404                        TRAP    C$BSEG
2511  005626  052737  100000  002370        BIS     #CDAL15,ROLOAD          ;SETUP TO READ DEVICE TYPE
2512  005634  013737  002364  002372        MOV     IDTYPE,ROGOOD           ;SETUP EXPECTED DATA
2513  005642  004737  006110                JSR     PC,LDRDOR               ;LOAD, READ AND COMPARE REG 0
2514  005646  001404                        BEQ     3$                      ;IF EQUAL THEN DEVICE TYPE COMPARED
2515  005650                                ERRDF   1,,ERORR0               ;DEVICE TYPE NOT EQUAL EXPECTED
2516  005650  104455                        TRAP    C$ERDF
2517  005652  000001                        .WORD   1
2518  005654  000000                        .WORD   0
2519  005656  004620                        .WORD   ERORR0
2520  005660                        3$:     ENDSEG
2521  005660                        10001$:
2522  005660  104405                        TRAP    C$ESEG
2523
2524                                        ;RESET THE SIGNAL CDAL15 TO 0 TO READ DEVICE NUMBER AGAIN AND SET AND
2525                                        ;CLEAR THE SIGNAL CDAL0 TO CLEAR THE TRACE RAM ADDRESS REGISTER, TO
2526                                        ;CLEAR THE TRACING FLIP-FLOP, TO RELOAD THE EVENT COUNTERS AND TO CLEAR
  27                                        ;SBL FLIP FLOPS 59:56.
2528
2529  005662                                BGNSEG
2530  005662  104404                        TRAP    C$BSEG
```

```
2531  005664  013737  002360  002370          MOV     IDDEV,ROLOAD            ;GET USER DEFINED DEVICE NUMBER
2532  005672  052737  000001  002370          BIS     #CDALO,ROLOAD           ;SETUP TO SET THE CLEAR SIGNAL
2533  005700  004737  006102                  JSR     PC,LDRDRO               ;GO LOAD,READ AND CHECK REG 0
2534  005704  001405                          BEQ     4$                      ;IF OK THEN CONTINUE
2535  005706                                  ERRDF   1,,ROERROR              ;REG 0 NOT EQUAL DEVICE #
2536  005706  104455                          TRAP    C$ERDF
2537  005710  000001                          .WORD   1
2538  005712  000000                          .WORD   0
2539  005714  004604                          .WORD   ROERROR
2540  005716                                  CKLOOP
2541  005716  104406                          TRAP    C$CLP1
2542  005720  042737  000001  002370  4$:     BIC     #CDALO,ROLOAD           ;SETUP TO CLEAR THE SIGNAL CDALO
2543  005726  004737  006102                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
2544  005732  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
2545  005734                                  ERRDF   1,,ROLOAD               ;REG 0 NOT EQUAL DEVICE NUMBER
2546  005734  104455                          TRAP    C$ERDF
2547  005736  000001                          .WORD   1
2548  005740  000000                          .WORD   0
2549  005742  002370                          .WORD   ROLOAD
2550  005744                          5$:     ENDSEG
2551  005744                          10002$:
2552  005744  104405                          TRAP    C$ESEG
2553
2554                                          ;CLEAR AND CHECK CONTROL REGISTER 2
2555
2556  005746                                  BGNSEG
2557  005746  104404                          TRAP    C$BSEG
2558  005750                                  SETVEC  #4,#6$,#PRI07           ;SETUP VECTOR
2559  005750  012746  000340                  MOV     #PRI07,-(SP)
2560  005754  012746  006050                  MOV     #6$,-(SP)
2561  005760  012746  000004                  MOV     #4,-(SP)
2562  005764  012746  000003                  MOV     #3,-(SP)
2563  005770  104437                          TRAP    C$SVEC
2564  005772  062706  000010                  ADD     #10,SP
2565  005776  005037  002376                  CLR     R2LOAD                  ;SETUP TO CLEAR ALL BITS
2566  006002  013777  002376  174342          MOV     R2LOAD,@REG2            ;WRITE BITS INTO REG 2
2567  006010  017737  174336  002400          MOV     @REG2,R2READ            ;READ REG 2 BACK
2568  006016  042737  177400  002400          BIC     #177400,R2READ          ;CLEAR UNWANTED BITS IN REG 2
2569  006024  023737  002376  002400          CMP     R2LOAD,R2READ           ;CHECK IF EXP EQUALS ACTUAL
2570  006032  001414                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
2571  006034                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
2572  006034  104455                          TRAP    C$ERDF
2573  006036  000002                          .WORD   2
2574  006040  000000                          .WORD   0
2575  006042  004704                          .WORD   R2EROR
2576  006044                                  CKLOOP
2577  006044  104406                          TRAP    C$CLP1
2578  006046  000406                          BR      7$                      ;BRANCH AROUND TIME OUT ERROR
2579  006050  005726                  6$      TST     (SP)+                   ;CLEAN UP STACK
2580  006052  005726                          TST     (SP)+                   ;CLEAN UP STACK
2581  006054                                  ERRDF   2,,R2TM                 ;TIME OUT ERROR REG 2
2582  006054  104455                          TRAP    C$ERDF
2583  006056  000002                          .WORD   2
2584  006060  000000                          .WORD   0
2585  006062  005106                          .WORD   R2TM
2586  006064                          7$:     CLRVEC  #4                      ;CLEAR VECTOR
```

```
2587  006064  012700  000004          MOV     #4,R0
2588  006070  104436                  TRAP    C$CVEC
2589  006072  005037  002416          CLR     R6MASK          ;SETUP TO CHECK ALL CONTROL REG 6 BITS
2590  006076                          ENDSEG
2591  006076                  10003$:
2592  006076  104405                  TRAP    C$ESEG
2593
2594  006100  000207                  RTS     PC              ;RETURN BACK TO TEST
2595
2596                          ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF REGISTER 0
2597                          ;CONDITION CODES ARE SET ON EXIT AS RESULT OF THE "CMP" INSTRUCTION.
2598
2599  006102  013737  002370  002372  LDRDR0::MOV     R0LOAD,R0GOOD   ;PUT DATA LOADED INTO EXPECTED
2600  006110  013777  002370  174232  LDRD0R::MOV     R0LOAD,@REG0    ;WRITE WORD TO REGISTER 0
2601  006116  017737  174226  002374  READR0::MOV     @REG0,R0READ    ;READ REGISTER CONTENTS BACK
2602  006124  023737  002372  002374          CMP     R0GOOD,R0READ   ;COMPARE EXPECTED WITH THAT READ
2603  006132  000207                  RTS     PC              ;EXIT WITH CONDITION CODES SET
2604
2605                          ;ROUTINE TO LOAD, READ, AND COMPARE CONTENTS OF REGISTER 2.
2606                          ;CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION
2607
2608  006134  013777  002376  174210  LDRDR2::MOV     R2LOAD,@REG2    ;WRITE BITS INTO REGISTER 2
2609  006142  017737  174204  002400  READR2::MOV     @REG2,R2READ    ;READ REGISTER 2 BACK
2610  006150  042737  177400  002400          BIC     #177400,R2READ  ;CLEAR UNWANTED BITS IN REG 2
2611  006156  023737  002376  0024            CMP     R2LOAD,R2READ   ;CHECK IF EXP EQUALS ACTUAL
2612  006164  000207                  RTS     PC              ;EXIT WITH CONDITION CODES SET
2613
2614                          ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF REGISTER 4.
2615                          ;CONDITION CODES ARE SET ON EXET AS RESULT OF "CMP" INSTRUCTION.
2616
2617  006166  013737  002402  002404  LDRDAR::MOV     R4LOAD,R4GOOD   ;COPY DATA TO BE LOADED
2618  006174  000337  002404          SWAB    R4GOOD          ;LOW TO HIGH BYTE TO SIMULATE READBACK
2619  006200  000403                  BR      LDRD4R          ;GO LOAD, READ + CHECK AND ARRAY
2620
2621  006202  013737  002402  002404  LDRDR4::MOV     R4LOAD,R4GOOD   ;SETUP EXPECTED DATA
2622  006210  013777  002402  174136  LDRD4R::MOV     R4LOAD,@REG4    ;WRITE WORD INTO REGISTER 4
2623  006216  017737  174132  002410  READR4::MOV     @REG4,R4READ    ;READ WORD BACK FROM REGISTER 4
2624  006224  013737  002410  002412          MOV     R4READ,R4BAD    ;COPY DATA READ
2625  006232  043737  002406  002412          BIC     R4MASK,R4BAD    ;CLEAR UNWANTED BITS
2626  006240  023737  002404  002412          CMP     R4GOOD,R4BAD    ;COMPARE WORD EXPECTED WITH READ
2627  006246  000207                  RTS     PC              ;RETURN WITH CONDITION CODES SET
2628
2629                          ;ROUTINE TO LOAD, READ AND COMPARE CONTENTS OF CONTROL REGISTER 6
2630                          ;CONDITION CODES ARE SET ON EXIT AS RESULT OF "CMP" INSTRUCTION.
2631
2632  006250  013777  002414  174100  LDRDR6::MOV     R6LOAD,@REG6    ;WRITE WORD INTO REGISTER 6
2633  006256  017737  174074  002420  READR6::MOV     @REG6,R6READ    ;READ THE WORD BACK
2634  006264  013737  002420  002422          MOV     R6READ,R6BAD    ;COPY DATA READ
2635  006272  043737  002416  002420          BIC     R6MASK,R6READ   ;MASK OUT UNWANTED BITS
2636  006300  023737  002414  002420          CMP     R6LOAD,R6READ   ;COMPARE DATA LOADED WITH DATA READ
2637  006306  000207                  RTS     PC              ;EXIT WITH CONDITION CODES SET
2638
```

```
                        ;**
                        ; THIS ROUTINE WILL WRITE AND READ THE TRACE RAM ADDRESS REGISTER BITS TRAD 9:0
                        ; WITH THE CONTENTS OF LOCATION "TRADRS"
                        ;
                        ; TO WRITE THE TRACE RAM ADDRESS REGISTER THE PROGRAM WILL CLEAR CONTROL REG 2
                        ; BITS PDAL7 TO PDAL0 WHICH WILL ASSERT THE SIGNAL PTERO L IN THE POINTER REG-
                        ; ISTER.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REIGSTER 6 WITH THE SIGNAL
                        ; PTERO L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPTO L. THE SIGNAL
                        ; WPTO L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE TRACE RAM ADDRESS
                        ; REGISTER.
                        ;
                        ; WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH THE SIGNAL PTERO L
                        ; ASSERTED IN THE POINTER REGISTER, A PULSE WILL BE ISSUED ON THE SIGNAL RPTO H.
                        ; THE SIGNAL RPTO H WILL READ THE DATA FROM THE TRACE RAM ADDRESS REGISTER.
                        ;
                        ;       INPUT:  LOCATION "TRADRS" MUST CONTAIN ADDRESS TO LOAD
                        ;       CALL:   JSR     PC,TRADLD
                        ;       EXIT:   LOCATION R6MASK WILL EQUAL 176000
                        ;--

006310                  TRADLD::BGNSEG
006310  104404                 TRAP    C$BSEG

                                ;CLEAR ALL BITS IN CONTROL REGISTER 2. CONTROL REGISTER 2 BITS PDAL3
                                ;TO PDAL0 BEING CLEARED WILL ASSERT THE SIGNAL PTERO L IN THE POINTER
                                ;REGISTER.

006312  005037  002376          CLR     R2LOAD                  ;SETUP TO CLEAR ALL BITS IN REG 2
006316  004737  006134          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
006322  001405                 BEQ     1$                      ;IF LOADED OK THEN CONTINUE
006324                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
006324  104455                 TRAP    C$ERDF
006326  000002                 .WORD   2
006330  000000                 .WORD   0
006332  004704                 .WORD   R2EROR
006334                          CKLOOP
006334  104406                 TRAP    C$CLP1

                                ;WRITE THE TRACE RAM ADDRESS WITH THE ADDRESS IN LOCATION "TRADRS".
                                ;ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTERO L
                                ;ASSERTED, THE SIGNAL WPTO L WILL PULSE TO LOAD THE TRACE RAM ADDRESS
                                ;REGISTER.  ON A READ COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL
                                ;PTERO L ASSERTED, THE SIGNAL RPTO H WILL PULSE TO READ THE TRACE RAM
                                ;ADDRESS REGISTER BITS TRAD 9:0.

006336  013737  006374  002414  1$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS TO BE LOADED
006344  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
006352  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ + CHECK TRAD BITS 9:0
006356  001404                         BEQ     2$                      ;IF ADDRESS OK THEN CONTINUE
006360                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQUAL "TRADRS"
006360  104455                         TRAP    C$ERDF
006362  000004                         .WORD   4
006364  002462                         .WORD   TRADER
006366  004734                         .WORD   RC26ER
006370                          2$:     ENDSEG
006370                          10004$:
```

```
 2695  006370  104405                    TRAP    C$ESEG
 2696  006372  000207                    RTS     PC
 2697
 2698  006374  000000          TRADRS::.WORD   0                       ;CONTAINS TRACE RAM ADDRESS
 2699
 2700                          ;**
 2701                          ; THIS ROUTINE WILL USE THE CONTENTS OF R5 AS A POINTER TO A WORD TO BE
 2702                          ; LOADED TO CONTROL REGISTER 2.  THE WORD WILL ASSERT A PARTICULAR SIGNAL
 2703                          ; IN THE POINTER REGISTER.
 2704                          ;--
 2705
 2706  006376  012537  002376  ASSERT::MOV     (R5)+,R2LOAD            ;SETUP BITS TO BE LOADED
 2707  006402                          BGNSEG
 2708  006402  104404                    TRAP    C$BSEG
 2709  006404  004737  006134            JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
 2710  006410  001404                    BEQ     1$                      ;IF LOADED OK THEN CONTINUE
 2711  006412                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
 2712  006412  104455                    TRAP    C$ERDF
 2713  006414  000002                    .WORD   2
 2714  006416  000000                    .WORD   0
 2715  006420  004704                    .WORD   R2EROR
 2716  006422                  1$:     ENDSEG
 2717  006422                  10005$:
 2718  006422  104405                    TRAP    C$ESEG
 2719  006424  000205                    RTS     R5                      ;EXIT BACK TO MAIN LINE CODE
```

```
                        ;**
                        ; THIS TEST WILL WRITE AND READ THE TRACE RAM DATA IN BUFFERS FROM THE LSI-11
                        ; BUS WITH THE CONTENTS OF LOCATION "R6LOAD".  THE TRACE RAM DATA IN BUFFERS
                        ; TESTED BY THIS ROUTINE ARE TRDI BITS 15:0, TRDI BITS 31:16, TRDI BITS 47:32,
                        ; OR TRDI BITS 59:48.  FOR EACH CALL TO THIS ROUTINE, ONLY ONE SET OF TRACE
                        ; RAM DATA IN BUFFERS WILL BE TESTED.
                        ;
                        ; PREVIOUS TO THIS ROUTINE, IN ROUTINE "INITED", CONTROL REGISTER 0 BITS CDAL7
                        ; TO CDAL0 WERE CLEARED.  CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                        ; TRSL0 L TO BE ASSERTED.  THE SIGNAL TRSL0 L ASSERTED WILL ENABLE THE OUTPUTS
                        ; OF THE TRACE RAM DATA IN BUFFERS.
                        ;
                        ; TO WRITE THE TRACE RAM DATA IN BUFFERS, THE PROGRAM WILL LOAD CONTROL REG 2
                        ; WITH THE BITS TO SELECT PTER5 L, PTER6 L, PTER7 L OR PTER8 L IN THE POINTER
                        ; REGISTER.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH ONE OF
                        ; THE ABOVE SIGNALS SET IN THE POINTER REGISTER, A PULSE WILL BE ISSUED ON
                        ; THE SIGNAL WPT5 H, WPT6 H, WPT7 H, OR WPT8 H RESPECTIVELY.  THESE LAST
                        ; SIGNALS MENTIONED WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE TRACE
                        ; RAM DATA IN BUFFER BITS TRDI 15:0, TRDI 31:16, TRDI 47:32, OR TRDI 59:48
                        ; RESPECTIVELY.
                        ;
                        ; TO READ THE TRACE RAM DATA IN BUFFERS, THE PROGRAM WILL LOAD CONTROL REGISTER
                        ; 2 WITH THE BITS TO SELECT PTER1 L, PTER2 L, PTER3 L OR PTER4 L IN THE POINTER
                        ; REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH ONE OF THE
                        ; ABOVE SIGNALS SET IN THE POINTER REGISTER, A PULSE WILL BE ISSUED ON THE SIGNAL
                        ; RTP1 H, RPT2 H, RPT3 H OR RPT4 H RESPECTIVELY.  THESE LAST SIGNALS ON A READ
                        ; COMMAND WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BITS TRDI 15:0,
                        ; TRDI 31:16, TRDI 47:32 OR TRDI 59:48 RESPECTIVELY.
                        ;
                        ;       INPUT:  LOCATION "R6LOAD" CONTAINS DATA TO BE LOADED
                        ;
                        ;       CALL:   JSR     R5,TRDIBF       ;GO LOAD,READ + CHECK TRAM DATA IN BUF.
                        ;               .WORD   PTER5           ;CONTROL REGISTER 2 WRITE POINTER SEL.
                        ;                                       ;READ POINTER WILL BE DONE BY DOING -4.
                        ;--

006426                  TRDIBF::BGNSEG
006426  104404                TRAP    C$BSEG

                                ;SET PDAL BITS 3-0 IN CONTROL REGISTER 2 TO ASSERT THE SIGNAL
                                ;PTER5 L, PTER6 L, PTER7 L OR PTER8 L. THE PARAMTER FOLLOWING THE CALL
                                ;CONTAINS THE BITS TO BE LOADED INTO CONTROL REGISTER 2.

006430  011537  002376          MOV     (R5),R2LOAD             ;GET THE PDAL BITS TO BE LOADED
006434  004737  006134          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG  2
006440  001405                  BEQ     1$                      ;IF LOADED OK THE CONTINUE
006442                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
006442  104455                  TRAP    C$ERDF
006444  000002                  .WORD   2
006446  000000                  .WORD   0
006450  004704                  .WORD   R2EROR
006452                          CKLOOP
006452  104406                  TRAP    C$CLP1

                                ;LOAD DATA PATTERN INTO TRACE RAM DATA IN BUFFER. WHEN A WRITE COMMAND
                                ;IS ISSUED TO CONTROL REGISTER 6 WITH THE SIGNAL PTER5 L, PTER6 L,
```

```
                                        ;PTER7 L OR PTER8 L ASSERTED, A PULSE WILL BE ISSUED ON WPT5 H, WPT6 H,
                                        ;WPT7 H OR WPT8 H RESPECTIVELY WHICH WILL LOAD THE DATA INTO THE TRACE
                                        ;RAM DATA IN BUFFER.

006454  013777  002414  173674  1$:   MOV     R6LOAD,@REG6            ;WRITE DATA INTO TRAM DATA IN BUF

                                        ;SUBTRACT 4 FROM THE PDAL BITS LOADED PREVIOUSLY INTO CONTROL REGISTER
                                        ;2 TO ASSERT THE SIGNALS PTER1 L, PTER2 L, PTER3 L OR PTER4 L IN THE
                                        ;POINTER REGISTER.

006462  162737  000004  002376          SUB     #4,R2LOAD               ;BACK UP POINTER REGISTER BY 4 SIGNALS
006470  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
006474  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
006476                                  ERRDF   2,,R2EROR               ;REGISTER 2NOT EQULA EXPECTED
006476  104455                          TRAP    C$ERDF
006500  000002                          .WORD   2
006502  000000                          .WORD   0
006504  004704                          .WORD   R2EROR
006506                                  CKLOOP
006506  104406                          TRAP    C$CLP1

                                        ;READ AND CHECK DATA PATTERN FROM THE TRACE RAM DATA IN BUFFER. WHEN
                                        ;A READ COMMAND IS ISUED TO CONTROL REGISTER 6 WITH THE SIGNAL PTER1 L,
                                        ;PTER2 L, PTER3 L OR PTER4 L ASSERTED, A PULSE WILL BE ISSUED ON THE
                                        ;SIGNAL RPT1 H, RPT2 H, RPT3 H OR RPT4 H RESPECTIVELY WHICH WILL READ
                                        ;THE DATA FROM  THE TRACE RAM DATA IN BUFFER SELECTED.

006510  017737  173642  002420  2$:   MOV     @REG6,R6READ            ;READ THE DATA AND SAVE IT
006516  022715  000010                  CMP     #PTER8,(R5)             ;CHECK IF TESTING TRDI 59:48
006522  001003                          BNE     3$                      ;IF NOT GO CHECK ALL BITS
006524  042737  170000  002420          BIC     #170000,R6READ          ;CLEAR UNUSED BITS
006532  023737  002414  002420  3$:    CMP     R6LOAD,R6READ           ;CHECK DATA LOADED AGAINST DATA READ
006540  001434                          BEQ     7$                      ;IF DATA OK THEN EXIT
006542  022715  000005                  CMP     #PTER5,(R5)             ;CHECK IF TRDI BITS 15:0
006546  001005                          BNE     4$                      ;IF NOT CHECK NEXT SET
006550                                  ERRDF   4,TRDI15,R026ER         ;TRDI 15 TO TRDI 0 NOT EQUAL EXPECTED
006550  104455                          TRAP    C$ERDF
006552  000004                          .WORD   4
006554  002517                          .WORD   TRDI15
006556  004734                          .WORD   R026ER
006560  000424                          BR      7$                      ;CONTINUE IF PROCEED FROM ERROR
006562  022715  000006          4$:    CMP     #PTER6,(R5)             ;CHECK IF TRDI BITS 31:16
00[illegible]  001005                   BNE     5$                      ;IF NOT THEN CHECK NEXT SET
006570                                  ERRDF   4,TRDI31,R026ER         ;TRDI 31 TO TRDI 16 NOT EQUAL EXPECTED
006570  104455                          TRAP    C$ERDF
006572  000004                          .WORD   4
006574  002554                          .WORD   TRDI31
006576  004734                          .WORD   R026ER
006600  000414                          BR      7$                      ;CONTINUE IF PROCEED FROM ERROR
006602  022715  000007          5$:    CMP     #PTER7,(R5)             ;CHECK IF TRDI BITS 47:32
006606  001005                          BNE     6$                      ;IF NOT MUST BE TRDI BITS 59:48
006610                                  ERRDF   4,TRDI47,R026ER         ;TRDI 47 TO TRDI 32 NOT EQUAL EXPECTED
006610  104455                          TRAP    C$ERDF
006612  000004                          .WORD   4
006614  002612                          .WORD   TRDI47
006616  004734                          .WORD   R026ER
```

```
2832  006620  000404                        BR      7$                      ;CONTINUE IF PROCEED FROM ERROR
2833  006622                          6$:     ERRDF   4,TRDI59,R026ER         ;TRDI 59 TO TRDI 48 NOT EQUAL EXPECTED
2834  006622  1044..                        TRAP    C$ERDF
2835  006624  000004                        .WORD   4
2836  006626  002650                        .WORD   TRDI59
2837  006630  004734                        .WORD   R026ER
2838  006632                          7$:     ENDSEG
2839  006632                          10006$:
2840  006632  104405                        TRAP    C$ESEG
2841  006634  005725                        TST     (R5)+                   ;UPDATE POINTER FOR RETURN
2842  006636  000205                        RTS     R5                      ;EXIT BACK TO MAIN LINE CODE
2843
2844                                  ;THE FOLLOWING ROUTINE WILL SET AND CLEAR CDAL6 IN CONTROL REGISTER 0. SETTING
2845                                  ;AND CLEARING CDAL6 WILL CAUSE A PULSE ON THE SIGNAL TRANST H.  THE SIGNAL
2846                                  ;TRANST H WILL CAUSE A PULSE ON THE SIGNAL ANST L, WHICH WILL CAUSE A PULSE ON
2847                                  ;THE SIGNAL ORST L.
2848
2849  006640                          TRANST::BGNSEG
2850  006640  104404                        TRAP    C$BSEG
2851  006642  052737  000100  002370        BIS     #CDAL6,ROLOAD           ;SET BIT CDAL6 IN CONTROL REGISTER 0
2852  006650  004737  006102                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
2853  006654  001405                        BEQ     1$                      ;IF LOADED OK THEN CONTINUE
2854  006656                                ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
2855  006656  104455                        TRAP    C$ERDF
2856  006660  000001                        .WORD   1
2857  006662  000000                        .WORD   0
2858  006664  004604                        .WORD   R0EROR
2859  006666                                CKLOOP
2860  006666  104406                        TRAP    C$CLP1
2861  006670  042737  000100  002370  1$:   BIC     #CDAL6,ROLOAD           ;SETUP TO CLEAR CDAL6
2862  006676  004737  006102                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
2863  006702  001404                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
2864  006704                                ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
2865  006704  104455                        TRAP    C$ERDF
2866  006706  000001                        .WORD   1
2867  006710  000000                        .WORD   0
2868  006712  004604                        .WORD   R0EROR
2869  006714                          2$:     ENDSEG
2870  006714                          10007$:
2871  006714  104405                        TRAP    C$ESEG
2872  006716  000207                        RTS     PC                      ;RETURN BACK TO TEST BEING EXECUTED
2873
2874  006720                                ENDMOD
2875
2876                                  .TITLE MISCELLANEOUS SECTIONS
2877                                  .SBTTL  REPORT CODING SECTION
2878
2879  006720                                BGNMOD
2880
2881                                  ;++
2882                                  ; THE REPORT CODING SECTION CONTAINS THE
2883                                  ; 'PRINTS" CALLS THAT GENERATE STATISTICAL REPORTS.
2884                                  ;--
2885
2886  006720                                BGNRPT
2887  006720                          $RPT::
```

```
                                                EXIT    RPT
006720  000167                                  .WORD   JSJMP
006722  000000                                  .WORD   L10014-2-.


                                                .EVEN

006724                                          ENDRPT
006724                                  L10014:
006724  10442^                                  TRAP    CSRPT

                                        .SBTTL  PROTECTION TABLE

                                        ;++
                                        ; THIS TABLE IS USED BY THE RUNTIME SERVICES
                                        ; TO PROTECT THE LOAD MEDIA.
                                        ;--

006726                                          BGNPROT
006726                                  LSPROT::

006726  177777                                  -1              ;OFFSET INTO P-TABLE FOR CSR ADDRESS
006730  177777                                  -1              ;OFFSET INTO P-TABLE FOR MASSBUS ADDRESS
006732  177777                                  -1              ;OFFSET INTO P-TABLE FOR DRIVE NUMBER

006734                                          ENDPROT
```

```
                                        .SBTTL  INITIALIZE SECTION

                                        ;++
                                        ; THE INITIALIZE SECTION CONTAINS THE CODING THAT IS PERFORMED
                                        ; AT THE BEGINNING OF EACH PASS.
                                        ;--

                                                BGNINIT
                                        L$INIT::
                                                READEF  #EF.START               ;SEE IF A START COMMAND
006734  012700  000040                          MOV     #EF.START,R0
006740  104447                                  TRAP    C$REFG
006742                                          BCOMPLETE       1$              ;BRANCH IF START COMMAND
006742  103410                                  BCS     1$
006744                                          READEF  #EF.RESTART             ;SEE IF A RESTART COMMAND
006744  012700  000037                          MOV     #EF.RESTART,R0
006750  104447                                  TRAP    C$REFG
006752                                          BCOMPLETE       1$              ;BRANCH IF RESTART
006752  103404                                  BCS     1$
006754                                          READEF  #EF.PWR                 ;SEE IF RECOVERING FROM A POWER FAIL
006754  012700  000034                          MOV     #EF.PWR,R0
006760  104447                                  TRAP    C$REFG
006762                                          BNCOMPLETE      2$              ;IF NOT CHECK IN CONTINUE
006762  103001                                  BCC     2$
006764                                  1$:     BRESET                          ;ISSUE A BUS RESET TO CLEAR THE SYSTEM
006764  104433                                  TRAP    C$RESET
006766                                  2$:     READEF  #EF.NEW                 ;SEE IF A NEW PASS
006766  012700  000035                          MOV     #EF.NEW,R0
006772  104447                                  TRAP    C$REFC
006774                                          BNCOMPLETE      3$              ;IF NOT GO CHECK IF CONTINUE
006774  103003                                  BCC     3$
006776  012737  177777  002362                  MOV     #-1,UNITNB              ;SETUP TO INIT UNIT NUMBER
007004                                  3$:     READEF  #EF.CONTINUE            ;CHECK IF CONTINUE
007004  012700  000036                          MOV     #EF.CONTINUE,R0
007010  104447                                  TRAP    C$REFG
007012                                          BCOMPLETE       6$              ;IF YES THEN EXIT
007012  103434                                  BCS     6$
007014  005237  002362                  4$:     INC     UNITNB                  ;INC TO NEW UNIT NUMBER
007020                                          GPHARD  UNITNB,R5               ;GET DEVICE INFORMATION
007020  013700  002362                          MOV     UNITNB,R0
007024  104442                                  TRAP    C$GPHRD
007026  010005                                  MOV     R0,R5
007030                                          BNCOMPLETE      4$              ;GO TRY ANOTHER UNIT
007030  103371                                  BCC     4$
007032  012701  002350                          MOV     #REG0,R1                ;ADDRESS OF ED DEVICE ADDRESS TABLE
007036  005002                                  CLR     R2                      ;CLEAR OFFSET TO ADD TO TABLE ADDRESS
007040  011511                          5$:     MOV     (R5),(R1)               ;GET ADDRESS AND SAVE
007042  060221                                  ADD     R2,(R1)+                ;ADD OFFSET TO ADDRESS
007044  005202                                  INC     R2                      ;UPDATE OFFSET BY 2
007046  005202                                  INC     R2                      ;
007050  022702  000010                          CMP     #10,R2                  ;CHECK IF DONE LOADING TABLE
007054  001371                                  BNE     5$                      ;GO UPDATE NEXT ADDRESS
007056  005725                                  TST     (R5)+                   ;UPDATE THE POINTER
007060  005037  002360                          CLR     IDDEV                   ;CLEAR OUT DEVICE NUMBER
```

```
2972  007064  111537  002361            MOVB    (R5),IDDEV+1            ;GET THE ED DEVICE NUMBER
2973  007070  012737  101000  002364    MOV     #CDAL15.CDAL9,IDTYPE    ;SETUP ED DEVICE TYPE
2974  007076  005725                    TST     (R5)+                   ;UPDATE THE POINTER
2975  007100  011537  002366            MOV     (R5),EXTPRB             ;GET EXTERNAL PROBE INDICATOR
2976  007104                    6$:     SETPRI  #PRI07                  ;RAISE PROCESSOR PRIORITY
2977  007104  012700  000340            MOV     #PRI07,R0
2978  007110  104441                    TRAP    C$SPRI
2979
2980
2981  007112                            EXIT    INIT
2982  007112  104432                    TRAP    C$EXIT
2983  007114  000002                    .WORD   L10016-.
2984
2985
2986                                    .EVEN
2987
2988  007116                            ENDINIT
2989  007116                    L10016:
2990  007116  104411                    TRAP    C$INIT
2991
2992                            .SBTTL  AUTODROP SECTION
2993
2994                            ;++
2995                            ; THIS CODE IS EXECUTED IMMEDIATELY AFTER THE INITIALIZE CODE IF
2996                            ; THE "ADR" FLAG WAS SET.  THE UNIT(S) UNDER TEST ARE CHECKED TO
2997                            ; SEE IF THEY WILL RESPOND.  THOSE THAT DON'T ARE IMMEDIATELY
2998                            ; DROPPED FROM TESTING.
2999                            ;--
3000
3001  007120                            BGNAUTO
3002  007120                    L$AUTO::
3003
3004
3005  007120                            ENDAUTO
3006  007120                    L10017:
3007  007120  104461                    TRAP    C$AUTO
3008
3009                            .SBTTL  CLEANUP CODING SECTION
3010
3011                            ;++
3012                            ; THE CLEANUP CODING SECTION CONTAINS THE CODING THAT IS PERFORMED
3013                            ; AFTER THE HARDWARE TESTS HAVE BEEN PERFORMED.
3014                            ;--
3015
3016  007122                            BGNCLN
3017  007122                    L$CLEAN::
3018  007122  013777  002360  173220    MOV     IDDEV,@REG0             ;CLEAR CONTROL REGISTER 0 EXCEPT
3019                                                                    ;FOR DEVICE NUMBER
3020  007130  012777  000000  173214    MOV     #0,@REG2                ;CLEAR REGISTER 2
3021
3022
3023  007136                            EXIT    CLN
3024  007136  104432                    TRAP    C$EXIT
3025  007140  000002                    .WORD   L10020-.
3026
3027
```

```
                                        .EVEN

                                        ENDCLN
                                L10020:
                                        TRAP    C$CLEAN

                                .SBTTL  DROP UNIT SECTION

                                ;++
                                ; THE DROP-UNIT SECTION CONTAINS THE CODING THAT CAUSES A DEVICE
                                ; TO NO LONGER BE TESTED.
                                ;--

                                        BGNDU
                                L$DU::


                                        EXIT    DU
                                        .WORD   J$JMP
                                        .WORD   L10021-2-.


                                        .EVEN

                                        ENDDU
                                L10021:
                                        TRAP    C$DU

                                .SBTTL  ADD UNIT SECTION

                                ;++
                                ; THE ADD-UNIT SECTION CONTAINS ANY CODE THE PROGRAMMER WISHES
                                ;  TO BE EXECUTED IN CONJUNCTION WITH THE ADDING OF A UNIT BACK
                                ;  TO THE TEST CYCLE.
                                ;--

                                        BGNAU
                                L$AU::


                                        EXIT    AU
                                        .WORD   J$JMP
                                        .WORD   L10022-2-.


                                        .EVEN

                                        ENDAU
                                L10022:
                                        TRAP    C$AU

                                        ENDMOD
```

```
                                .TITLE HARDWARE TESTS

                                .SBTTL  TEST 1: SELECT AND INITIALIZE STATE ANALYZER

007160                                  BGNMOD

                                ;++
                                ; TEST TO CHECK THAT THE STATE ANALYZER CAN BE SELECTED AND INITIALIZED TO
                                ; A KNOWN STATE  THIS TEST WILL BE EXECUTED AT THE BEGINNING OF EVERY TEST
                                ; TO PUT THE MODULE IN A KNOWN STATE.  THE TEST WILL LOAD THE DEVICE NUMBER INTO
                                ; CONTROL REGISTER 0 AND CHECK THAT THE DEVICE NUMBER CAN BE READ CORRECTLY.
                                ; THE LOW BYTE OF CONTROL REGISTER 0 WILL BE CHECKED TO BE ZERO. THE TEST WILL
                                ; THEN LOAD THE DEVICE NUMBER AND THE SIGNAL CDAL15 INTO CONTROL REGISTER 0,
                                ; AND CHECK THAT THE DEVICE TYPE AND THE LOW BYTE CAN BE READ BACK CORRECTLY.
                                ; THE TEST WILL THEN CLEAR THE SIGNAL CDAL15 IN CONTROL REGISTER 0 AND CHECK
                                ; THE DEVICE NUMBER AND THE LOW BYTE TO BE CORRECT.  THE TEST WILL THEN LOAD
                                ; READ AND CHECK CONTROL REGISTER 2 WITH ZEORES.
                                ;--



007160                                  BGNTST
007160                          T1::
007160  004737  005474                  JSR     PC,INITED               ;INITIALIZE THE STATE ANALYZER


007164                                  ENDTST
007164                          L10023:
007164  104401                          TRAP    CSETST
```

```
                                .SBTTL  TEST 2: CONTROL REG 0 TEST (1'S, AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THAT CONTROL REGISTER 0 READ/WRITE BITS CDAL7,CDAL6,
                                ; CDAL5,CDAL4,CDAL3,CDAL2,CDAL1, AND CDAL0 CAN BE SET TO A ONE AND THEN
                                ; SET TO ALL ZEROES.
                                ;--

007166                                  BGNTST
007166                          T2::
007166  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007172                                  BGNSEG
007172  104404                          TRAP    C$BSEG

                                        ;SET CONTROL REGISTER 0 R/W BITS CDAL7 TO CDAL0 TO ALL ONES

007174  112737  000377  002370          MOVB    #377,ROLOAD             ;SETUP TO LOAD ALL ONES
007202  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
007206  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007210                                  ERRDF   1,,ROEROR               ;CDAL7 TO CDAL0 NOT EQL TO 377
007210  104455                          TRAP    C$ERDF
007212  000001                          .WORD   1
007214  000000                          .WORD   0
007216  004604                          .WORD   ROEROR
007220                          1$:     ENDSEG
007220                          10000$:
007220  104405                          TRAP    C$ESEG

007222                                  BGNSEG
007222  104404                          TRAP    C$BSEG

                                        ;SET CONTROL REGISTER 0 R/W BITS CDAL7 TO CDAL0 TO ALL ZEROES

007224  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR ALL BITS
007230  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
007234  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
007236                                  ERRDF   1,,ROEROR               ;CDAL7 TO CDAL0 NOT EQL 0
007236  104455                          TRAP    C$ERDF
007240  000001                          .WORD   1
007242  000000                          .WORD   0
007244  004604                          .WORD   ROEROR
007246                          2$:     ENDSEG
007246                          10001$:
007246  104405                          TRAP    C$ESEG
007250                                  ENDTST
007250                          L10024:
007250  104401                          TRAP    C$ETST
```

```
3161                                    .SBTTL  TEST 3: CONTROL REG 0 TEST (1'S + 0'S, 0'S + 1'S)
3162
3163                                    ;++
3164                                    ; THIS TEST WILL CHECK CONTROL REGISTER 0 READ/WRITE BITS CDAL7 TO CDAL0
3165                                    ; WITH AN ALTERNATING ONES AND ZEROES PATTERN (252) AND THEN AN ALTERNATING
3166                                    ; ZEROES AND ONES PATTERN (125).
3167                                    ;--
3168
3169  007252                                    BGNTST
3170  007252                            T3::
3171  007252  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
3172
3173  007256                                    BGNSEG
3174  007256  104404                           TRAP    C$BSEG
3175
3176                                    ;SET CDAL7, CDAL5, CDAL3, AND CDAL1 EQUAL TO ONES
3177                                    ;SET CDAL6, CDAL4, CDAL2, AND CDAL0 EQUAL TO ZEROES
3178
3179  007260  112737  000252  002370          MOVB    #252,ROLOAD             ;SET ONES AND ZEROES PATTERN
3180  007266  004737  006102                   JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
3181  007272  001404                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
3182  007274                                    ERRDF   1,,ROE..JR              ;CDAL7 TO CDAL0 NOT EQL 252
3183  007274  104455                           TRAP    C$ERDF
3184  007276  000001                           .WORD   1
3185  007300  000000                           .WORD   0
3186  007302  004604                           .WORD   ROEROR
3187  007304                            1$:     ENDSEG
3188  007304                            10000$:
3189  007304  104405                           TRAP    C$ESEG
3190
3191  007306                                    BGNSEG
3192  007306  104404                           TRAP    C$BSEG
3193
3194                                    ;SET CDAL7, CDAL5, CDAL3 AND CDAL1 TO ZEROES
3195                                    ;SET CDAL6, CDAL4, CDAL2 AND CDAL0 TO ONES
3196
3197  007310  112737  000125  002370          MOVB    #125,ROLOAD             ;SET ZEROES AND ONES PATTERN
3198  007316  004737  006102                   JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
3199  007322  001404                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
3200  007324                                    ERRDF   1,,ROEROR               ;CDAL7 TO CDAL0 NOT EQL 125
3201  007324  104455                           TRAP    C$ERDF
3202  007326  000001                           .WORD   1
3203  007330  000000                           .WORD   0
3204  007332  004604                           .WORD   ROEROR
3205  007334                            2$:     ENDSEG
3206  007334                            10001$:
3207  007334  104405                           TRAP    C$ESEG
3208  007336                                    ENDTST
3209  007336                            L10025:
3210  007336  104401                           TRAP    C$ETST
```

TEST 4: CONTROL REGISTER 0 TEST USING A BINARY COUNT SEQ 0065

```
3211                                    .SBTTL  TEST 4: CONTROL REGISTER 0 TEST USING A BINARY COUNT
3212
3213                                    ;++
3214                                    ; THIS TEST WILL CHECK CONTROL REGISTER 0 READ/WRITE BITS CDAL7 TO CDAL0
3215                                    ; USING A BINARY COUNT PATTERN. THE TEST PATTERN WILL START ! "M 0 AND
3216                                    ; INCREMENT UNTIL THE TEST PATTERN 377 HAS BEEN LOADED AND TL   .
3217                                    ;--
3218
3219  007340                                    BGNTST
3220  007340                            T4::
3221  007340  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STA :  NALYZER
3222
3223  007344  105037  002370                   CLRB    ROLOAD                  ;SET TEST PATTERN INITIALLY TO 0
3224
3225  007350                            1$:     BGNSEG
3226  007350  104404                           TRAP    C$BSEG
3227  007352  004737  006102                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
3228  007356  001404                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
3229  007360                                    ERRDF   1,,ROERROR              ;REG 0 NOT EQUAL EXPECTED
3230  007360  104455                           TRAP    C$ERDF
3231  007362  000001                           .WORD   1
3232  007364  000000                           .WORD   0
3233  007366  004604                           .WORD   ROERROR
3234  007370                            2$:     ENDSEG
3235  007370                            10000$:
3236  007370  104405                           TRAP    C$ESEG
3237
3238  007372  105237  002370                   INCB    ROLOAD                  ;UPDATE THE TEST PATTERN BY 1
3239  007376  001364                           BNE     1$                      ;IF NOT 0 LOAD, NEXT PATTERN
3240  007400                                    ENDTST
3241  007400                            L10026:
3242  007400  104401                           TRAP    C$ETST
3243
```

TEST 5: CONTROL REG 2 TEST (1'S, AND 0'S) SEQ 0066

```
                                        .SBTTL  TEST 5: CONTROL REG 2 TEST (1'S, AND 0'S)

                                        ;++
                                        ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7, PDAL6, PDAL5,
                                        ; PDAL4, PDAL3, PDAL2, PDAL1 AND PDAL0, TO BE SET TO ALL ONES AND THEN ALL
                                        ; ZEROES.
                                        ;--

007402                                          BGNTST
007402                                  T5::
007402  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007406                                          BGNSEG
007406  104404                                  TRAP    C$BSEG

                                        ;SET CONTROL REGISTER 2 BITS PDAL7 TO PDAL0 TO ALL ONES

007410  012737  000377  002376                  MOV     #377,R2LOAD             ;SETUP BITS TO BE LOADED
007416  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
007422  001404                                  BEQ     1$                      ;IF ALL ONES THEN CONTINUE
007424                                          ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL 377
007424  104455                                  TRAP    C$ERDF
007426  000002                                  .WORD   2
007430  000000                                  .WORD   0
007432  004704                                  .WORD   R2EROR
007434                                  1$:     ENDSEG
007434                                  10000$:
007434  104405                                  TRAP    C$ESEG

007436                                          BGNSEG
007436  104404                                  TRAP    C$BSEG

                                        ;SET CONTROL REGISTER 2 BITS PDAL7 TO PDAL0 TO ALL ZEROES

007440  005037  002376                          CLR     R2LOAD                  ;SETUP TO CLEAR ALL BITS
007444  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
007450  001404                                  BEQ     2$                      ;IF ALL ZEROES THEN CON INUE
007452                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL 0 0
007452  104455                                  TRAP    C$ERDF
007454  000002                                  .WORD   2
007456  000000                                  .WORD   0
007460  004704                                  .WORD   R2EROR
007462                                  2$:     ENDSEG
007462                                  10001$:
007462  104405                                  TRAP    C$ESEG
007464                                          ENDTST
007464                                  L10027:
007464  104401                                  TRAP    C$ETST
```

```
3293                                    .SBTTL  TEST 6: CONTROL REG 2 TEST (1'S + 0'S, 0'S + 1'S)
3294
3295                                    ;++
3296                                    ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7 TO PDAL0 WITH
3297                                    ; AN ALTERNATING ONES AND ZEROES PATTERN (252) AND THEN AN ALTERNATING ZEROES
3298                                    ; AND ONES PATTERN (125).
3299                                    ;--
3300
3301  007466                                    BGNTST
3302  007466                            T6::
3303  007466  004737  005474                    JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
3304
3305  007472                                    BGNSEG
3306  007472  104404                            TRAP    C$BSEG
3307
3308                                            ;SET PDAL7, PDAL5, PDAL3, AND PDAL1 TO ONES
3309                                            ;SET PDAL6, PDAL4, PDAL2, AND PDAL0 TO ZEROES
3310
3311  007474  012737  000252  002376            MOV     #252,R2LOAD             ;SETUP BITS TO BE LOADED
3312  007502  004737  006134                    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
3313  007506  001404                            BEQ     1$                      ;IF LOADED OK THEN CONTINUE
3314  007510                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL 252
3315  007510  104455                            TRAP    C$ERDF
3316  007512  000002                            .WORD   2
3317  007514  000000                            .WORD   0
3318  007516  004704                            .WORD   R2EROR
3319  007520                                    ENDSEG
3320  007520                            1$:
3321  007520  104405                            TRAP    C$ESEG
3322
3323  007522                                    BGNSEG
3324  007522  104404                            TRAP    C$BSEG
3325
3326                                            ;SET PDAL7, PDAL5, PDAL3 AND PDAL1 TO ZEROES
3327                                            ;SET PDAL6, PDAL4, PDAL2 AND PDAL0 TO ONES
3328
3329  007524  012737  000125  002376            MOV     #125,R2LOAD             ;SETUP BITS TO BE LOADED
3330  007532  004737  006134                    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
3331  007536  001404                            BEQ     2$                      ;IF LOADED OK THEN CONTINUE
3332  007540                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL 125
3333  007540  104455                            TRAP    C$ERDF
3334  007542  000002                            .WORD   2
3335  007544  000000                            .WORD   0
3336  007546  004704                            .WORD   R2EROR
3337  007550                            2$:     ENDSEG
3338  007550                            10001$:
3339  007550  104405                            TRAP    C$ESEG
3340  007552                                    ENDTST
3341  007552                            L10030:
3342  007552  104401                            TRAP    C$ETST
```

TEST 7: CONTROL REG 2 TEST USING A BINARY COUNT SEQ 0068

```
                                .SBTTL  TEST 7: CONTROL REG 2 TEST USING A BINARY COUNT

                                ;++
                                ; THIS TEST WILL CHECK CONTROL REGISTER 2 READ/WRITE BITS PDAL7 TO PDAL0
                                ; USING A BINARY COUNT PATTERN.  THE TEST WILL START WITH DATA PATTERN OF
                                ; ZERO AND INCREMENT THE PATTERN UNTIL THE PATTERN 377 HAS BEEN LOADED AND
                                ; TESTED
                                ;--

007554                                  BGNTST
007554                          T7::
007554  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
007560  005037  002376                   CLR     R2LOAD                  ;SET TEST PATTERN TO ZERO

007564                          1$:     BGNSEG
007564  104404                          TRAP    C$BSEG
007566  004737  006134                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
007572  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
007574                                  ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL EXPECTED
007574  104455                          TRAP    C$ERDF
007576  000002                          .WORD   2
007600  000000                          .WORD   0
007602  004704                          .WORD   R2EROR
007604                          2$:     ENDSEG
007604                          10000$:
007604  104405                          TRAP    C$ESEG

007606  105237  002376                   INCB    R2LOAD                  ;INCREMENT THE TEST PATTERN BY 1
007612  001364                          BNE     1$                      ;IF NOT 0 THEN LOAD NEXT PATTERN
007614                                  ENDTST
007614                          L10031:
007614  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 8: TRAM ADDRESS REG TEST (1'S, AND 0'S)

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) BY
                                ; LOADING A PATTERN OF ALL ONES (3777) INTO THE ADDRESS REGISTER AND THEN
                                ; READING AND CHECKING THE REGISTER FOR ALL ONES.  THE TEST WILL THEN LOAD,
                                ; READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH A DATA PATTERN OF ALL
                                ; ZEROES.  TO WRITE AND READ THE TRACE RAM ADDRESS REGISTER, THE PROGRAM WILL
                                ; CLEAR CONTROL REGISTER 0 BITS CDAL7 TO CDAL0, CLEAR CONTROL REGISTER 2 BITS
                                ; PDAL7 TO PDAL0, LOAD THE DATA PATTERN INTO THE TRACE RAM ADDRESS REGISTER
                                ; VIA A WRITE COMMAND TO CONTROL REGISTER 6, AND THEN READ THE TRACE RAM ADDRESS
                                ; REGISTER VIA A READ COMMAND TO CONTROL REGISTER 6.  WHEN PDAL BITS 3,2,1, AND 0
                                ; ARE SET TO A 0, THE POINTER REGISTER SIGNAL PTER0 L WILL BE ASSERTED LOW. THIS
                                ; SIGNAL BEING SET LOW ALONG WITH A WRITE OR READ COMMAND TO CONTROL REGISTER 6
                                ; WILL ASSERT THE SIGNAL WPTO L OR RPTO H RESPECTIVELY.  THE SIGNAL WPTO L WILL
                                ; LOAD THE ADDRESS INTO THE TRACE RAM ADDRESS RECISTER AND THE SIGNAL RPTO H
                                ; WILL READ THE ADDRESS FROM THE TRACE RAM ADDRESS REGISTER.
                                ;--

007616                                  BGNTST
007616                          T8::
007616  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007622                                  BGNSEG
007622  104404                          TRAP    C$BSEG

                                ;CLEAR ALL BITS IN CONTROL REGISTER 2. CONTROL REGISTER 2 BITS PDAL3 TO
                                ;PDAL0 BEING CLEARED WILL ASSERT THE SIGNAL PTER0 L IN THE POINTER REG.

007624  005037  002376                   CLR     R2LOAD                  ;SETUP TO CLEAR CONTROL REGISTER 2
007630  004737  006134                   JSR     PC,LDRDR2               ;GO LOAD, READ AND  CHECK REG 2
007634  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007636                                  ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL TO 0
007636  104455                          TRAP    C$ERDF
007640  000002                          .WORD   2
007642  000000                          .WORD   0
007644  004704                          .WORD   R2EROR
007646                                  CKLOOP
007646  104406                          TRAP    C$CLP1

                                ;WRITE ALL ONES INTO THE TRACE RAM ADDR  S REGI TER AND CHECK THAT ALL
                                ;ONES WERE WRITTEN. ON A WRITE  COMMAND TO CONTROL REGISTER 6, THE
                                ;SIGNAL WPTO L WILL BE ASSERTED TO LOAD THE TRACE RAM ADDRESS REGISTER.
                                ;ON A READ COMMAND TO CONTROL REGISTER 6, THE SIGNAL RPTO H WILL BE
                                ;ASSERTED TO READ THE TRACE RAM ADDRESS REGISTER

007650  012737  003777  002414  1$:     MOV     #3777,R6LOAD            ;SETUP BITS TO BE LOADED
007656  012737  174000  002416           MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
007664  004737  00 250                   JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
007670  001405                          BEQ     2$                      ;IF LOADED  OK THEN CONTINUE
007672                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQL 1777
007672  104455                          TRAP    C$ERDF
007674  000004                          .WORD   4
007676  002462                          .WORD   TRADER
007700  004734                          .WORD   R026ER
007702                                  CKLOOP
```

```
3432  007702  104406                  TRAP    C$CLP1
3433
3434                                  ;WRITE, READ AND CHECK TRACE RAM ADDRESS REGISTER WITH A DATA PATTERN
3435                                  ;OF ALL ZEROES.
3436
3437  007704  005037  002414    2$:   CLR     R6LOAD                ;SETUP TO CLEAR TRAM ADDRESS REG
3438  007710  004737  006250          JSR     PC,LDRDR6             ;GO LOAD, READ AND CHECK REG 6
3439  007714  001404                  BEQ     3$                    ;IF ALL ZEROES THEN CONTINUE
3440  007716                          ERRDF   4,TRADER,R026ER       ;TRAM ALDRESS REG NOT EQL 0
3441  007716  104455                  TRAP    C$ERDF
3442  007720  000004                  .WORD   4
3443  007722  002462                  .WORD   TRADER
3444  007724  004734                  .WORD   R026ER
3445  007726                  3$:     ENDSEG
3446  007726                  10000$:
3447  007726  104405                  TRAP    C$ESEG
3448  007730                          ENDIST
3449  007730                  L10032:
3450  007730  104407                  TRAP    C$ETST
```

```
                                        .SBTTL  TEST 9: TRAM ADDRESS REG TEST (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0) BY
                                        ; LOADING AN ALTERNATING ONES AND ZEROES PATTERN (2525) INTO THE TRACE RAM
                                        ; ADDRESS REGISTER AND THEN READING AND CHECKING THE REGISTER FOR THE PATTERN
                                        ; LOADED. THE TEST WILL THEN LOAD, READ AND CHECK THE TRACE RAM ADDRESS REGISTER
                                        ; WITH AN ALTERNATING ZEROES AND ONES DATA PATTERN (1252).
                                        ;--

007732                                          BGNTST
007732                                  T9::
007732  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

007736                                          BGNSEG
007736  104404                                  TRAP    C$BSEG

                                        ;CLEAR ALL BITS IN CONTROL REGISTER 2. CONTROL REGISTER 2 BITS PDAL3 TO
                                        ;PDAL0 BEING CLEARED WILL ASSERT THE SIGNAL PTERO L IN THE POINTER REG.

007740  005037  002376                          CLR     R2LOAD                  ;SETUP TO CLEAR CONTROL REGISTER 2
007744  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND  CHECK REG 2
007750  001405                                  BEQ     1$                      ;IF LOADED OK THEN CONTINUE
007752                                          ERRDF   2,,R2ERCR               ;REG 2 NOT EQUAL TO 0
007752  104455                                  TRAP    C$ERDF
007754  000002                                  .WORD   2
007756  000000                                  .WORD   0
007760  004704                                  .WORD   R2EROR
007762                                          CKLOOP
007762  104406                                  TRAP    C$CLP1

                                        ;WRITE AN ALTERNATING ONES AND ZEROES DATA PATTERN (2525) INTO THE
                                        ;TRACE RAM AND CHECK THAT THE DATA PATTERN CAN BE READ BACK CORRECTLY.
                                        ;ON A WRITE COMMAND TO CONTROL REGISTER 6, THE SIGNAL WRTO L WILL BE
                                        ;ASSERTED TO LOAD THE TRACE RAM ADDRESS REGISTER.  ON A READ COMMAND TO
                                        ;CONTROL REGISTER 6, THE SIGNAL RDTO H WILL BE ASSERTED TO READ THE
                                        ;TRACE RAM ADDRESS REGISTER.

007764  012737  002525  002414  1$:     MOV     #2525,R6LOAD            ;SETUP BITS TO BE LOADED
007772  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
010000  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
010004  001405                          BEQ     2$                      ;IF LOADED  OK THEN CONTINUE
010006                                  ERRDF   4,TRADER,RC26ER         ;TRAM ADDRESS REG NOT EQL 2525
010006  104455                          TRAP    C$ERDF
010010  000004                          .WORD   4
010012  002462                          .WORD   TRADER
010014  004734                          .WORD   RD26ER
010016                                  CKLOOP
010016  104406                          TRAP    C$CLP1
```

```
3501
3502                                        ;WRITE, READ, AND CHECK TRACE RAM ADDRESS REGISTER WITH AN ALTERNATING
3503                                        ;ZEROES AND ONES DATA PATTERN (1252)
3504
3505  010020  012737  001252  002414  2$:   MOV     #1252,R6LOAD          ;SETUP BITS TO BE LOADED
3506  010026  004737  006250               JSR     PC,LDRDR6             ;GO LOAD, READ AND CHECK REG
3507  010032  001404                        BEQ     3$                    ;IF LOADED OK THEN CONTINUE
3508  010034                                 ERRDF   4,TRADER,R026ER       ;TRAM ADDRESS REG NOT EQL 1252
3509  010034  104455                        TRAP    C$ERDF
3510  010036  000004                        .WORD   4
3511  010040  002462                        .WORD   TRADER
3512  010042  004734                        .WORD   R026ER
3513  010044                        3$:      ENDSEG
3514  010044                        10000$.
3515  010044  104405                        TRAP    C$ESEG
3516  010046                                 ENDTST
3517  010046                        L10033:
3518  010046  104401                        TRAP    C$ETST
3519
```

```
                        .SBTTL  TEST 10. TRAM ADDRESS REG TEST USING BINARY COUNT

                        ;++
                        ; THIS TEST WILL CHECK THE TRACE RAM ADDRESS REGISTER BITS (TRAD10-TRAD0)
                        ; USING A BINARY COUNT PATTERN.  THE DATA PATTERN WILL START WITH ZERO AND
                        ; INCREMENT BY ONE UNTIL THE DATA PATTERN 3777 HAS BEEN LOADED AND CHECKED.
                        ;--

010050                          BGNTST
010050                  T10::
010050  004737  005474          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
010054  005037  002414          CLR     R6LOAD                  ;SET DATA PATTERN INITIALLY TO ZERO
010060  012737  174000  002416  MOV     #174000,R6MASK          ;SETUP MASK TO IGNORE UNUSED BITS

010066                          BGNSEG
010066  104404                  TRAP    C$BSEG

                        ;CLEAR ALL BITS IN CONTROL REGISTER 2. CONTROL REGISTER 2 BITS PDAL3
                        ;TO PDAL0 BEING CLEARED WILL ASSERT THE SIGNAL PTERO L IN THE POINTER REG.

010070  005037  002376          CLR     R2LOAD                  ;SETUP TO CLEAR CONTROL REG 2
010074  004737  006134          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
010100  001404                  BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010102                          ERRDF   <,,R2EROR               ;REGISTER 2 NOT EQUAL TO 0
010102  104455                  TRAP    C$ERDF
010104  000002                  .WORD   2
010106  000000                  .WORD   0
010110  004704                  .WORD   R2EROR
010112                  1$:     ENDSEG
010112                  10000$:
010112  104405                  TRAP    C$ESEG

010114                  2$:     BGNSEG
010114  104404                  TRAP    C$BSEG

                        ;WRITE, READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH A DATA
                        ;PATTERN FROM 0 TO 3777

010116  004737  006250          JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
010122  001404                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
010124                          ERRDF   4,TRADER,R026ER         ;DATA ERROR LOADING TRAM ADDRESS REG
010124  104455                  TRAP    C$ERDF
010126  000004                  .WORD   4
010130  002462                  .WORD   TRADER
010132  004734                  .WORD   R026ER
010134                  3$:     ENDSEG
010134                  10001$:
010134  104405                  TRAP    C$ESEG

010136  005237  002414          INC     R6LOAD                  ;UPDATE DATA PATTERN BY 1
010142  032737  004000  002414  BIT     #BIT11,R6LOAD           ;CHECK IF LAST PATTERN WAS 3777
010150  001761                  BEQ     2$                      ;IF NOT LOAD NEXT NUMBER AND CHECK IT
010152                          ENDTST
010152                  L10034:
010152  104401                  TRAP    C$ETST
```

```
                                .SBTTL  TEST 11: ZERO TRAM ADDRESS REG WITH CDAL 0 H.

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE CLEARED WHEN
                                ; THE SIGNAL CDAL 0 H IS SET TO A ONE IN CONTROL REGISTER 0. THE TEST WILL LOAD
                                ; ALL ONES (3777) INTO THE TRACE RAM ADDRESS REGISTER AND CHECK THAT ALL ONES
                                ; WERE LOADED.  THE TEST WILL THEN SET THE SIGNAL CDAL 0 H TO A ONE IN CONTROL
                                ; REGISTER 0.  THE TEST WILL THEN READ THE TRACE RAM ADDRESS REGISTER CHECKING
                                ; IT TO BE CLEARED.  THE SIGNAL CDAL 0 H WILL BE CLEARED IN CONTROL REGISTER 0
                                ; AND THE TRACE RAM ADDRESS REGISTER WILL BE READ AGAIN TO CHECK THAT NO BITS
                                ; GET SET AFTER CLEARING THE SIGNAL CDAL 0 H.
                                ;--

010154                                  BGNTST
010154                          1$::
010154  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
010160                                  BGNSEG
010160  104404                          TRAP    C$BSEG
                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0. THIS IS DONE TO INIT
                                        ;THE SEGMENT TO A KNOWN STATE ON SCOPE LOOPING.

010162  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE
010166  004737  C0610^                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
010172  001404                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
010174                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
010174  104455                          TRAP    C$ERDF
010176  000001                          .WORD   1
010200  000000                          .WORD   0
010202  004604                          .WORD   R0EROR

                                        ;CLEAR ALL BITS IN CONTROL REG 2 TO ASSERT THE SIGNAL PTER0 L IN POINTER REG.

010204  005037  002376          2$:     CLR     R2LOAD                  ;SETUP TO CLEAR ALL REG 2 BITS
010210  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD,READ AND CHECK REG 2
010214  001404                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
010216                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL TO 0
010216  104455                          TRAP    C$ERDF
010220  000002                          .WORD   2
010222  000000                          .WORD   0
010224  004704                          .WORD   R2EROR

                                        ;WRITE, READ, AND CHECK TRACE RAM ADDRESS REGISTER WITH DATA PATTERN OF 3777

010226  012737  003777  002414  2$:     MOV     #3777,R6LOAD            ;SETUP BITS TO BE LOADED
010234  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP MASK TO IGNORE UNUSED BITS
010242  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REG 6
010246  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
010250                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG NOT EQL 3777
010250  104455                          TRAP    C$ERDF
010252  000004                          .WORD   4
010254  002462                          .WORD   TRADER
010256  004734                          .WORD   R026ER
010260                                  CALOOP
010260  104406                          TRAP    C$CLP1

                                        ;SET CDALO H IN CONTROL REG 0 TO CLEAR THE TRACE RAM ADDRESS REGISTER.
```

```
3631
3632  010262  112737  000001  002370  3$:     MOVB    #CDAL0,R0LOAD           ;SETUP BIT TO BE LOADED
3633  010270  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
3634  010274  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
3635  010276                                   ERRDF   1,R0EROR                ;REGISTER 0 NOT EQUAL EXPECTED
3636  010276  104455                          TRAP    C$ERDF
3637  010300  000001                          .WORD   1
3638  010302  000000                          .WORD   0
3639  010304  004604                          .WORD   R0EROR
3640  010306                                   CKLOOP
3641  010306  104406                          TRAP    C$CLP1
3642
3643                                           ;READ TRACE RAM ADDRESS REGISTER TO CHECK THAT CDAL0 H ON A ONE
3644                                           ;CLEARED THE TRACE RAM ADDRESS REGISTER.
3645
3646  010310  005037  002414          4$:     CLR     R6LOAD                  ;SIMULATE A CLEAR
3647  010314  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK REG 6
3648  010320  001405                          BEQ     5$                      ;IF EQUAL TO 0 THEN CONTINUE
3649  010322                                   ERRDF   4,TRADER,R026ER         ;CDAL0 H FAILED TO 0 TRAM ADDRESS REG
3650  010322  104455                          TRAP    C$ERDF
3651  010324  000004                          .WORD   4
3652  010326  002462                          .WORD   TRADER
3653  010330  004734                          .WORD   R026ER
3654  010332                                   CKLOOP
3655  010332  104406                          TRAP    C$CLP1
3656
3657                                           ;CLEAR SIGNAL CDAL 0 H IN CONTROL REGISTER 0
3658
3659  010334  105037  002370          5$:     CLRB    R0LOAD                  ;SETUP TO CLEAR CDAL0 H BIT
3660  010340  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
3661  010344  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
3662  010346                                   ERRDF   1,R0EROR                ;REG 0 LOW BYTE NOT EQUAL TO 0
3663  010346  104455                          TRAP    C$ERDF
3664  010350  000001                          .WORD   1
3665  010352  000000                          .WORD   0
3666  010354  004604                          .WORD   R0EROR
3667  010356                                   CKLOOP
3668  010356  104406                          TRAP    C$CLP1
3669
3670                                           ;READ TRACE RAM ADDRESS REGISTER AGAIN CHECKING THAT IT DID NOT
3671                                           ;CHANGE AFTER CLEARING THE SIGNAL CDAL 0 H.
3672
3673  010360  004737  006256          6$:     JSR     PC,READR6               ;GO READ AND CHECK REGISTER 6
3674  010364  001404                          BEQ     7$                      ;IF TRAM ADDRESS REG STILL 0 THEN CONT
3675  010366                                   ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG BITS SET AFTER CDAL0 H CLEARED
3676  010366  104455                          TRAP    C$ERDF
3677  010370  000004                          .WORD   4
3678  010372  002462                          .WORD   TRADER
3679  010374  004734                          .WORD   R026ER
3680  010376                           7$:     ENDSEG
3681  010376                           10000$:
3682  010376  104405                          TRAP    C$ESEG
3683  010400                                   ENDTST
3684  010400                           L10035:
3685  010400  104401                          TRAP    C$ETST
```

```
3686                                    .SBTTL  TEST 12. TRAM DATA IN BUF - TRDI 15:0 (1'S, AND 0'S)
3687
3688                                    ;++
3689                                    ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI15 H TO
3690                                    ; TRDI0 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
3691                                    ; RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL
3692                                    ; ZEROES ((00000).
3693                                    ;
3694                                    ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
3695                                    ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
3696                                    ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
3697                                    ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
3698                                    ; THE PROGRAM WILL THEN SET PDAL2 AND PDAL0 IN CONTROL REGISTER 2 WHICH WILL
3699                                    ; CAUSE THE SIGNAL PTER5 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
3700                                    ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER5 L IS ASSERTED, A
3701                                    ; PULSE WILL BE ISSUED ON THE SIGNAL WPT5 H. THE SIGNAL WPT5 H WILL CLOCK THE
3702                                    ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 15:0).
3703                                    ;
3704                                    ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL0 IN
3705                                    ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER1 L TO BE ASSERTED IN THE
3706                                    ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
3707                                    ; THE SIGNAL PTER1 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT1 H.
3708                                    ; THE SIGNAL RPT1 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
3709                                    ; TO THE LSI-11 BUS.
3710                                    ;--
3711
3712  010402                                    BGNTST
3713  010402                            T12::
3714  010402  004737  005474                    JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
3715
3716  010406                                    BGNSUB
3717  010406                            T12.1:
3718  010406  104402                           TRAP    C$BSUB
3719
3720                                            ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
3721                                            ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
3722                                            ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
3723                                            ;TRACE RAM DATA IN BUFFERS TO BE READ.
3724
3725                                            ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 15:0
3726                                            ;WITH A DATA PATTERN EQUAL TO 177777.
3727
3728  010410  012737  177777  002414             MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
3729  010416  004537  006426                     JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3730  010422  000005                             .WORD   PTER5                   ;SELECT TRDI BITS 15:0
3731  010424                                    ENDSUB
3732  010424                            L10037:
3733  010424  104403                           TRAP    C$ESUB
3734
```

```
3735
3736  010426                                BGNSUB
3737  010426                          T12.2:
3738  010426  104402                        TRAP    C$BSUB
3739
3740                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 15:0
3741                                        ;WITH A DATA PATTERN EQUAL TO 000000.
3742
3743  010430  005037  002414                CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
3744  010434  004537  006426                JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3745  010440  000005                        .WORD   PTER5                   ;SELECT TRDI BITS 15:0
3746  010442                                ENDSUB
3747  010442                          L10040:
3748  010442  104403                        TRAP    C$ESUB
3749
3750  010444                                ENDTST
3751  010444                          L10036:
3752  010444  104401                        TRAP    C$ETST
3753
```

```
                                .SBTTL  TEST 13: TRAM DATA IN BUF - TRDI 15:0 (1'S + 0'S,0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI15 H TO
                                ; TRDI0 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                ; RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252)
                                ; AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
                                ;
                                ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                ; THE PROGRAM WILL THEN SET PDAL2 AND PDAL0 IN CONTROL REGISTER 2 WHICH WILL
                                ; CAUSE THE SIGNAL PTER5 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER5 L IS ASSERTED, A
                                ; PULSE WILL BE ISSUED ON THE SIGNAL WPT5 H.  THE SIGNAL WPT5 H WILL CLOCK THE
                                ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 15:0).
                                ;
                                ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL0 IN
                                ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER1 L TO BE ASSERTED IN THE
                                ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                ; THE SIGNAL PTER1 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT1 H.
                                ; THE SIGNAL RPT1 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                ; TO THE LSI-11 BUS.
                                ;--

                                        BGNTST
                                T13::
                                        JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        BGNSUB
                                T13.1:
                                        TRAP    C$BSUB

                                        ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                        ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                        ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                        ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 15:0
                                        ;WITH A DATA PATTERN EQUAL TO 125252.

010454  012737  125252  002414          MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
010462  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
010466  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
010470                                  ENDSUB
010470                          L10042:
010470  104403                          TRAP    C$ESUB
```

```
3803
3804  010472                                  T13.2:  BGNSUB
3805  010472
3806  010472  104402                                  TRAP    C$BSUB
3807
3808                                                  ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 15:0
3809                                                  ;WITH A DATA PATTERN EQUAL TO 052525.
3810
3811  010474  012737  052525  0024'4                 MOV     #052525,R6LOAD          ;SETUP DATA TO BE LOADED
3812  010502  004537  006426                         JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3813  010506  000005                                 .WORD   PTER5                   ;SELECT TRDI BITS 15:0
3814  010510                                          ENDSUB
3815  010510                                  L10043:
3816  010510  104403                                  TRAP    C$ESUB
3817
3818  010512                                          ENDTST
3819  010512                                  L10041:
3820  010512  104401                                  TRAP    C$ETST
3821
```

```
3822                                    .SBTTL  TEST 14: TRAM DATA IN BUF - TRDI 31:16 (1'S, AND 0'S)
3823
3824                                    ;++
3825                                    ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI31 H TO
3826                                    ; TRDI16 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
3827                                    ; RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL
3828                                    ; ZEROES (000000).
3829                                    ;
3830                                    ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
3831                                    ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
3832                                    ; TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
3833                                    ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
3834                                    ; THE PROGRAM WILL THEN SET PDAL2 AND PDAL1 IN CONTROL REGISTER 2 WHICH WILL
3835                                    ; CAUSE THE SIGNAL PTER6 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
3836                                    ; COMMAND IS ISSUED TO CONTR . REGISTER 6 AND THE SIGNAL PTER6 L IS ASSERTED, A
3837                                    ; PULSE WILL BE ISSUED ON THE SIGNAL WPT6 H. THE SIGNAL WPT6 H WILL CLOCK THE
3838                                    ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 31:16).
3839                                    ;
3840                                    ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL1 IN
3841                                    ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER2 L TO BE ASSERTED IN THE
3842                                    ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
3843                                    ; THE SIGNAL PTER2 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT2 H.
3844                                    ; THE SIGNAL RPT2 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
3845                                    ; TO THE LSI-11 BUS.
3846                                    ;--
3847
3848  010514                            BGNTST
3849  010514                    T14::
3850  010514  004737  005474           JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
3851
3852  010520                            BGNSUB
3853  010520                    T14.1:
3854  010520  104402                   TRAP    C$BSUB
3855
3856                                    ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
3857                                    ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
3858                                    ;THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
3859                                    ;TRACE RAM DATA IN BUFFERS TO BE READ.
3860
3861                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 31:16
3862                                    ;WITH A DATA PATTERN EQUAL TO 177777.
3863
3864  010522  012737  177777  002414   MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
3865  010530  004537  006426           JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3866  010534  000006                   .WORD   PTER6                   ;SELECT TRDI BITS 31:16
3867  010536                            ENDSUB
3868  010536                    L10045:
3869  010536  104403                   TRAP    C$ESUB
3870
```

```
3871
3872  010540                                BGSUB
3873  010540                          T14.2:
3874  010540  104402                        TRAP    C$BSUB
3875
3876                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 31:16
3877                                        ;WITH A DATA PATTERN EQUAL TO 000000.
3878
3879  010542  005037  002414                CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
3880  010546  004537  006426                JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3881  010552  000006                        .WORD   PTER6                   ;SELECT TRDI BITS 31:16
3882  010554                                ENDSUB
3883  010554                          L10046:
3884  010554  104403                        TRAP    C$ESUB
3885
3886  010556                                ENDTST
3887  010556                          L10044:
3888  010556  104401                        TRAP    C$ETST
3889
```

```
3890
3891                                    .SBTTL  TEST 15: TRAM DATA IN BUF - TRDI 31:16 (1'S + 0'S,0'S + 1'S)
3892
3893                                    ;++
3894                                    ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI31 H TO
3895                                    ; TRDI16 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
3896                                    ; RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252)
3897                                    ; AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
3898                                    ;
3899                                    ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
3900                                    ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
3901                                    ; TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
3902                                    ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
3903                                    ; THE PROGRAM WILL THEN SET PDAL2 AND PDAL1 IN CONTROL REGISTER 2 WHICH WILL
3904                                    ; CAUSE THE SIGNAL PTER6 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
3905                                    ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER6 L IS ASSERTED, A
3906                                    ; PULSE WILL BE ISSUED ON THE SIGNAL WPT6 H. THE SIGNAL WPT6 H WILL CLOCK THE
3907                                    ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 31:16).
3908                                    ;
3909                                    ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL1 IN
3910                                    ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER2 L TO BE ASSERTED IN THE
3911                                    ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
3912                                    ; THE SIGNAL PTER2 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT2 H.
3913                                    ; THE SIGNAL RPT2 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
3914                                    ; TO THE LSI-11 BUS.
3915                                    ;--
3916
3917  010560                                    BGNTST
3918  010560                            T15::
3919  010560  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
3920
3921  010564                                    BGNSUB
3922  010564                            T15.1:
3923  010564  104402                           TRAP    C$BSUB
3924
3925                                            ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
3926                                            ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
3927                                            ;THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
3928                                            ;TRACE RAM DATA IN BUFFERS TO BE READ.
3929
3930                                            ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 31.16
3931                                            ;WITH A DATA PATTERN EQUAL TO 125252.
3932
3933  010566  012737  125252  002414            MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
3934  010574  004537  006426                   JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3935  010600  000006                           .WORD   PTER6                   ;SELECT TRDI BITS 31:16
3936  010602                                    ENDSUB
3937  010602                            L10050:
3938  010602  104403                           TRAP    C$ESUB
3939
```

```
3940
3941  010604                                  BGNSUB
3942  010604                          T15.2:
3943  010604  104402                          TRAP    C$BSUB
3944
3945                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 31:16
3946                                          ;WITH A DATA PATTERN EQUAL TO 052525.
3947
3948  010606  012737  052525  002414          MOV     #052525,R6LOAD          ;SETUP DATA TO BE LOADED
3949  010614  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
3950  010620  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
3951  010622                                  ENDSUB
3952  010622                          L10051:
3953  010622  104403                          TRAP    C$ESUB
3954
3955  010624                                  ENDTST
3956  010624                          L10047:
3957  010624  104401                          TRAP    C$ETST
3958
```

```
                                        .SBTTL  TEST 16: TRAM DATA IN BUF - TRDI 47:32 (1'S, AND 0'S)

                                        ;++
                                        ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI47 H TO
                                        ; TRDI32 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                        ; RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (177777) AND THEN ALL
                                        ; ZEROES (000000).
                                        ;
                                        ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                        ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                        ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                        ; THE PROGRAM WILL THEN SET PDAL2,PDAL1 AND PDAL0 IN CONTROL REGISTER 2 WHICH WILL
                                        ; CAUSE THE SIGNAL PTER7 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                        ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER7 L IS ASSERTED, A
                                        ; PULSE WILL BE ISSUED ON THE SIGNAL WPT7 H.  THE SIGNAL WPT7 H WILL CLOCK THE
                                        ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 47:32).
                                        ;
                                        ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET PDAL1 AND PDAL0 IN
                                        ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER3 L TO BE ASSERTED IN THE
                                        ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                        ; THE SIGNAL PTER3 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT3 H.
                                        ; THE SIGNAL RPT3 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                        ; TO THE LSI-11 BUS.
                                        ;--

010626                                  BGNTST
010626                          T16::
010626  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

010632                                  BGNSUB
010632                          T16.1:
010632  104402                          TRAP    C$BSUB

                                        ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                        ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                        ;THE SIGNAL TPSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                        ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 47:32
                                        ;WITH A DATA PATTERN EQUAL TO 177777.

010634  012737  177777  002414          MOV     #177777,R6LOAD          ;SETUP DATA TO BE LOADED
010642  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
010646  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
010650                                  ENDSUB
010650                          110053:
010650  104403                          TRAP    C$ESUB
```

```
 4008
 4009  010652                          T16.2:  BGNSUB
 4010  010652
 4011  010652  104402                          TRAP    C$BSUB
 4012
 4013                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 47:32
 4014                                          ;WITH A DATA PATTERN EQUAL TO 000000.
 4015
 4016  010654  005037  002414                  CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
 4017  010660  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
 4018  010664  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
 4019  010666                                  ENDSUB
 4020  010666                          L10054:
 4021  010666  104403                          TRAP    C$ESUB
 4022
 4023  010670                                  ENDTST
 4024  010670                          L10052:
 4025  010670  104401                          TRAP    C$ETST
 4026
```

```
                                        .SBTTL  TEST 17: TRAM DATA IN BUF - TRDI 47:32 (1'S + 0'S,0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI47 H TO
                                        ; TRDI32 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                        ; RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (125252)
                                        ; AND THEN AND ALTERNATING ZEROES AND ONES DATA PATTERN (052525).
                                        ;
                                        ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                        ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                        ; TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                        ; THE PROGRAM WILL THEN SET PDAL2,PDAL1 AND PDAL0 IN CONTROL REGISTER 2 WHICH WILL
                                        ; CAUSE THE SIGNAL PTER7 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                        ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER7 L IS ASSERTED, A
                                        ; PULSE WILL BE ISSUED ON THE SIGNAL WPT7 H. THE SIGNAL WPT7 H WILL CLOCK THE
                                        ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 47:32).
                                        ;
                                        ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET PDAL1 AND PDAL0 IN
                                        ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER3 L TO BE ASSERTED IN THE
                                        ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                        ; THE SIGNAL PTER3 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT3 H.
                                        ; THE SIGNAL RPT3 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                        ; TO THE LSI-11 BUS.
                                        ;--

010672                                          BGNTST
010672                                  T17::
010672  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

010676                                          BGNSUB
010676                                  T17.1:
010676  104402                                  TRAP    $BSUB

                                                ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                                ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                                ;THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                                ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 47:32
                                                ;WITH A DATA PATTERN EQUAL TO 125252.

010700  012737  125252  002414                  MOV     #125252,R6LOAD          ;SETUP DATA TO BE LOADED
010706  004537  006426                          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
010712  000007                                  .WORD   PTER7                   ;SELECT TRDI BITS 47:32
010714                                          ENDSUB
010714                                  L10056:
010714  104403                                  TRAP    C$ESUB
```

```
4076
4077  010716                                  BGNSUB
4078  010716                            T17.2:
4079  010716  104402                          TRAP    C$BSUB
4080
4081                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 47.32
4082                                          ;WITH A DATA PATTERN EQUAL TO 052525.
4083
4084  010720  012737  052525  002414          MOV     #052525,R6LOAD          ;SETUP DATA TO BE LOADED
4085  010726  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4086  010732  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
4087  010734                                  ENDSUB
4088  010734                            L10057:
4089  010734  104403                          TRAP    C$ESUB
4090
4091  010736                                  ENDTST
4092  010736                            L10055.
4093  010736  104401                          TRAP    C$ETST
4094
```

```
                        .SBTTL  TEST 18: TRAM DATA IN BUF - TRDI 59:48 (1'S, AND 0'S)

                        ;++
                        ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI59 H TO
                        ; TRDI48 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                        ; RAM DATA IN BUFFER WITH A DATA PATTERN OF ALL ONES (007777) AND THEN ALL
                        ; ZEROES (000000).
                        ;
                        ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                        ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                        ; TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                        ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                        ; THE PROGRAM WILL THEN SET PDAL3 IN CONTROL REGISTER 2 WHICH WILL
                        ; CAUSE THE SIGNAL PTER8 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                        ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER8 L IS ASSERTED, A
                        ; PULSE WILL BE ISSUED ON THE SIGNAL WPT8 H. THE SIGNAL WPT8 H WILL CLOCK THE
                        ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 59:48).
                        ;
                        ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL2 IN
                        ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER4 L TO BE ASSERTED IN THE
                        ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                        ; THE SIGNAL PTER4 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT4 H.
                        ; THE SIGNAL RPT4 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                        ;  TO THE LSI-11 BUS.
                        ;

010740                          BGNTST
010740                  T18::
010740  004737  005474          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

010744                          BGNSUB
010744                  T18.1:
010744  104402                  TRAP    C$BSUB

                        ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                        ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                        ;THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                        ;TRACE RAM DATA IN BUFFERS TO BE READ.

                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 59:48
                        ;WITH A DATA PATTERN EQUAL TO 007777.

010746  012737  007777  002414  MOV     #007777,R6LOAD          ;SETUP DATA TO BE LOADED
010754  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
010760  00001C                  .WORD   PTER8                   ;SELECT TRDI BITS 59:48
010762                          ENDSUB
010762                  L10061:
010762  104403                  TRAP    C$ESUB
```

```
4144
4145  010764                                BGNSUB
4146  010764                          T18.2:
4147  010764  104402                        TRAP    C$BSUB
4148
4149                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 59:48
4150                                        ;WITH A DATA PATTERN EQUAL TO 000000.
4151
4152  010766  005037  002414                CLR     R6LOAD                  ;SETUP DATA TO BE LOADED
4153  010772  004537  006426                JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4154  010776  000010                        .WORD   PTER8                   ;SELECT TRDI BITS 59:48
4155  011000                                ENDSUB
4156  011000                          L10062:
4157  011000  104403                        TRAP    C$ESUB
4158
4159  011002                                ENDTST
4160  011002                          L10060:
4161  011002  104401                        TRAP    C$ETST
4162
```

```
                                .SBTTL  TEST 19: TRAM DATA IN BUF - TRDI 59:48 (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER REGISTER BITS TRDI59 H TO
                                ; TRDI48 H FROM THE LSI-11 BUS.  THE TEST WILL WRITE, READ AND CHECK THE TRACE
                                ; RAM DATA IN BUFFER WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (005252),
                                ; AND THEN AN ALTERNATING ZEROES AND ONES DATA PATTERN (002525).
                                ;
                                ; TO WRITE THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL CLEAR CONTROL REGISTER
                                ; 0 BITS CDAL7 TO CDAL0. CDAL3 AND CDAL2 BEING CLEARED WILL CAUSE THE SIGNAL
                                ; TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                ; BUFFER TO BE READ DURING THE READ OPERATION DESCRIBED IN THE NEXT PARAGRAPH.
                                ; THE PROGRAM WILL THEN SET PDAL3 IN CONTROL REGISTER 2 WHICH WILL
                                ; CAUSE THE SIGNAL PTER8 L TO BE ASSERTED IN THE POINTER REGISTER.  WHEN A WRITE
                                ; COMMAND IS ISSUED TO CONTROL REGISTER 6 AND THE SIGNAL PTER8 L IS ASSERTED, A
                                ; PULSE WILL BE ISSUED ON THE SIGNAL WPT8 H. THE SIGNAL WPT8 H WILL CLOCK THE
                                ; DATA INTO THE TRACE RAM DATA IN BUFFER (TRDI 59:48).
                                ;
                                ; TO READ THE TRACE RAM DATA IN BUFFER, THE PROGRAM WILL SET ONLY PDAL2 IN
                                ; CONTROL REGISTER 2 WHICH WILL CAUSE THE SIGNAL PTER4 L TO BE ASSERTED IN THE
                                ; POINTER REGISTER.  WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 AND
                                ; THE SIGNAL PTER4 L IS ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT4 H.
                                ; THE SIGNAL RPT4 H WILL READ THE DATA FROM THE TRACE RAM DATA IN BUFFER BACK
                                ; TO THE LSI-11 BUS.
                                ;--

011004                                  BGNTST
011004                          T19::
011004  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

011010                                  SGNSUB
011010                          T19.1:
011010  104402                          TRAP    C$BSUB

                                        ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO THIS
                                        ;CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 ON A ZERO WILL CAUSE
                                        ;THE SIGNAL TRSL0 L TO BE ASSERTED WHICH WILL ENABLE THE OUTPUTS OF THE
                                        ;TRACE RAM DATA IN BUFFERS TO BE READ.

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 59:48
                                        ;WITH A DATA PATTERN EQUAL TO 005252.

011012  012737  005252  002414          MOV     #005252,R6LOAD          ;SETUP DATA TO BE LOADED
011020  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
011024  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
011026                                  ENDSUB
011026                          L10064:
011026  104403                          TRAP    C$ESUB
```

```
4212
4213  011030                                  BGNSUB
4214  011030                          T19.2:
4215  011030  104402                          TRAP    C$ESUB
4216
4217                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER REGISTER BITS TRDI 59:48
4218                                          ;WITH A DATA PATTERN EQUAL TO 002525.
4219
4220  011032  012737  002525  002414          MOV     #002525,R6LOAD          ;SETUP DATA TO BE LOADED
4221  011040  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4222  011044  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
4223  011046                                  ENDSUB
4224  011046                          L10065:
4225  011046  104403                          TRAP    C$ESUB
4226
4227  011050                                  ENDTST
4228  011050                          L10063:
4229  011050  104401                          TRAP    C$ETST
4230
```

```
                                .SBTTL  TEST 20: TRAM DATA IN BUF SELECTION TEST

                                ;++
                                ; THIS TEST WILL CHECK THE TRACE RAM DATA IN BUFFER FROM THE LSI-11 BUS TO
                                ; BE SELECTED CORRECTLY BY THE POINTER REGISTER.  THE TEST WILL WRITE AND
                                ; CHECK TRDI BITS 15:0 WITH A DATA PATTERN EQUAL TO 1, TRDI BITS 31:16 WITH
                                ; A DATA PATTERN EQUAL TO 2, TRDI BITS 47:32 WITH A DATA PATTERN EQUAL TO
                                ; 3, AND TRDI BITS 59:32 WITH A DATA PATTERN EQUAL TO 4.  THE TEST WILL THEN
                                ; READ EACH SET OF TRDI BITS CHECKING THE DATA PATTERN TO BE THAT WHICH WAS
                                ; WRITTEN PREVIOUSLY IN THIS TEST.
                                ;--

                                        BGNTST
                                T20::
011052  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

011056  012701  000005                   MOV     #PTER5,R1               ;SETUP WORKING WRITE POINTER
011062  012702  000001                   MOV     #PTER1,R2               ;SETUP WORKING READ POINTER
011066  012703  000001                   MOV     #1,R3                   ;SETUP INITIAL DATA PATTERN
011072  005037  002416                   CLR     R6MASK                  ;CLEAR MASK WORD TO READ ALL BITS

011076                          1$:     BGNSEG
011076  104404                          TRAP    C$BSEG

                                        ;CONTROL REGISTER 0 BITS CDAL7 TO CDAL0 ARE CLEARED COMING INTO
                                        ;THIS CODE FROM THE ROUTINE "INITED". CDAL3 AND CDAL2 BEING CLEARED
                                        ;WILL CAUSE THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE
                                        ;OUTPUTS OF THE TRACE RAM DATA IN BUFFERS TO BE READ.

                                        ;LOAD PDAL BITS 3-0 TO SELECT POINTER REGISTER SIGNALS PTER5, PTER6,
                                        ;PTER7 OR PTER8.

011100  010137  002376                  MOV     R1,R2LOAD               ;SETUP TO LOAD POINTER REGISTER
011104  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHEKC REG 2
011110  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011112                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
011112  104455                          TRAP    C$ERDF
011114  000002                          .WORD   2
011116  000000                          .WORD   0
011120  004704                          .WORD   R2EROR
011122                                  CKLOOP
011122  104406                          TRAP    C$CLP1

                                        ;LOAD DATA PATTERN OF 1 INTO TRDI BITS 15:0
                                        ;LOAD DATA PATTERN OF 2 INTO TRDI BITS 31:16
                                        ;LOAD DATA PATTERN OF 3 INTO TRDI BITS 47:32
                                        ;LOAD DATA PATTERN OF 4 INTO TRDI BITS 59:48

011124  010337  002414          2$:     MOV     R3,R6LOAD               ;SETUP DATA TO BE LOADED
011130  010377  171222                  MOV     R3,@REG6                ;WRITE DATA INTO TRAM DATA IN BUF

                                        ;LOAD PDAL BITS 2-0 TO SELECT POINTER REGISTER PTER1  PTER2, PTER3,
                                        ;OR PTER4.

011134  010237  002376                  MOV     R2,R2LOAD               ;SETUP BITS TO BE LOADED
011140  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
```

```
4287  011144  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4288  011146                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
4289  011146  104455                          TRAP    C$ERDF
4290  011150  000002                          .WORD   2
4291  011152  000000                          .WORD   0
4292  011154  004704                          .WORD   R2EROR
4293  011156                                  CKLOOP
4294  011156  104406                          TRAP    C$CLP1
4295
4296                                          ;READ DATA PATTERN OF 1 FROM TRDI 15:0
4297                                          ;READ DATA PATTERN OF 2 FROM TRDI 31:16
4298                                          ;READ DATA PATTERN OF 3 FROM TRDI 47:32
4299                                          ;READ DATA PATTERN OF 4 FROM TRDI 59:48
4300
4301  011160  017737  [illegible]  002420  3$:     MOV     @REG6,R6READ            ;READ DATA PATTERN FROM TRDI BITS
4302  011166  043[illegible]  002416  002420        BIC     R6MASK,R6READ           ;CLEAR UNUSED BITS IF ANY
4303  011174  [illegible]  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
4304  011[illegible]  001404                       BEQ     4$                      ;IF DATA OK THEN CONTINUE
4305  011204                                       ERRDF   4,TRDIER,R026ER         ;TRAM DATA IN BUF DATA ERROR
4306  011204  104455                             TRAP    C$ERDF
4307  011206  000004                             .WORD   4
4308  011210  002706                             .WORD   TRDIER
4309  011212  004734                             .WORD   R026ER
4310  011214                                  4$:     ENDSEG
4311  011214                                  10000$:
4312  011214  104405                          TRAP    C$ESEG
4313
4314  011216  005201                          INC     R1                      ;UPDATE WORKING WRITE POINTER
4315  011220  005202                          INC     R2                      ;UPDATE WORKING READ POINTER
4316  011222  005203                          INC     R3                      ;UPDATE DATA PATTERN
4317  011224  022703  000004                  CMP     #4,R3                   ;CHECK IF TRDI BITS 59:48
4318  011230  001004                          BNE     5$                      ;IF NOT CHECK IF DONE
4319  011232  012737  170000  002416          MOV     #170000,R6MASK          ;SETUP TO IGNORE TOP 4 BITS
4320  011240  000716                          BR      1$                      ;GO DO LAST REGISTER
4321  011242  022703  000005          5$:     CMP     #5,R3                   ;CHECK IF DONE
4322  011246  001313                          BNE     1$                      ;IF NOT GO LOAD NEXT PATTERN
4323
4324  011250  012702  000001                  MOV     #PTER1,R2               ;RESET WORKING READ POINTER
4325  011254  012703  000001                  MOV     #1,R3                   ;RESET DATA PATTERN TO 1
4326  011260  005037  002416                  CLR     R6MASK                  ;CLEAR REGISTER 6 MASK WORD
4327
4328  011264                                  6$:     BGNSEG
4329  011264  104404                          TRAP    C$BSEG
4330
4331                                          ;LOAD PDAL BITS 2-0 TO SELECT PTER1, PTER2, PTER3, OR PTER4.
4332
4333  011266  010237  002376                  MOV     R2,R2LOAD               ;SETUP BITS TO BE LOADED
4334  011272  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
4335  011276  001405                          BEQ     7$                      ;IF LOADED OK THEN CONINUE
4336  011300                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
4337  011300  104455                          TRAP    C$ERDF
4338  011302  000002                          .WORD   2
4339  011304  000000                          .WORD   0
4340  011306  004704                          .WORD   R2EROR
4341  011310                                  CKLOOP
4342  011310  104406                          TRAP    C$CLP1
```

```
4343
4344                                        ;READ DATA PATTERN OF 1 FROM TRDI BITS 15:0
4345                                        ;READ DATA PATTERN OF 2 FROM TRDI BITS 31:16
4346                                        ;READ DATA PATTERN OF 3 FROM TRDI BITS 47:32
4347                                        ;READ DATA PATTERN OF 4 FROM TRDI BITS 59:48
4348
4349  011312  010337  002414          7$:   MOV     R3,R6LOAD               ;SETUP DATA PREVIOUSLY LOADED
4350  011316  017737  171034  002420        MOV     @REG6,R6READ            ;READ DATA FROM TRDI BITS
4351  011324  043737  002416  002420        BIC     R6MASK,R6READ           ;CLEAR UNUSED BITS IF ANY
4352  011332  023737  002414  002420        CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
4353  011340  001404                        BEQ     8$                      ;IF DATA OK THEN CONTINUE
4354  011342                                ERRDF   4,TRDISE,R026ER         ;TRAM DATA IN BUF SELECTION ERROR
4355  011342  104455                        TRAP    C$ERDF
4356  011344  000004                        .WORD   4
4357  011346  002443                        .WORD   TRDISE
4358  011350  004734                        .WORD   R026ER
4359  011352                          8$:   ENDSEG
4360  011352                          10001$:
4361  011352  104405                        TRAP    C$ESEG
4362
4363  011354  005202                        INC     R2                      ;UPDATE WORKING READ POINTER
4364  011356  005203                        INC     R3                      ;UPDATE DATA PATTERN
4365  011360  022703  000004                CMP     #4,R3                   ;CHECK IF LAST REGISTER
4366  011364  001004                        BNE     9$                      ;IF NOT CHECK IF DONE
4367  011366  012737  170000  002416        MOV     #170000,R6MASK          ;SETUP MASK WORD TO IGNORE UNUSED BITS
4368  011374  000733                        BR      6$                      ;GO DO LAST REGISTER
4369  011376  022703  000005          9$:   CMP     #5,R3                   ;CHECK IF DONE
4370  011402  001330                        BNE     6$                      ;IF NOT THEN LOAD NEXT REGISTER
4371  011404                                ENDTST
4372  011404                          L10066:
4373  011404  104401                        TRAP    C$ETST
4374
```

```
                                .SBTTL  TEST 21: TRAM DATA TEST - TRDI 15:0 (125252-052525)

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM BITS TRDI 15:0 WITH A DATA PATTERN OF 125252
                                ; AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED FOR THIS DATA
                                ; PATTERN BEFORE THE NEXT SEQUENTIAL LOCATION IS CHECKED.
                                ;
                                ; THIS TEST IS PERFORMED IN THE FOLLOWING MANNER
                                ;    1.  CLEAR LOW BYTE OF CONTROL REGISTER 0 TO SET SIGNAL TRSLO L
                                ;    2.  SET PTER0 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    3.  WRITE AND READ TRAM ADDRESS REG VIA SIGNALS WPT0 L AND RPT0 H
                                ;    4.  SET PTER5 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    5.  WRITE DATA PATTERN (125252-052525) INTO TRAM DATA IN BUF BITS TRDI 15:0
                                ;        VIA WPT5 H AND WRITE TO CONTROL REGISTER 6.
                                ;    6.  SET PTER1 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    7.  READ DATA PATTERN FROM TRAM DATA IN BUFFER VIA RPT1 H AND READ TO REG 6
                                ;    8.  WRITE TRACE RAM VIA WPT1 H AND WRITE TO CONTROL REGISTER 6
                                ;    9.  SET SIGNAL TRSL1 L BY SETTING CDAL2 = 1 IN REGISTER 0
                                ;   10.  READ TRACE RAM VIA RPT1 H AND READ TO CONTROL REGISTER 6
                                ;   11.  COMPLEMENT DATA PATTERN - REPEAT STEPS 1-10 WITH THIS PATTERN
                                ;   12.  RESET DATA PATTERN TO 125252 - INCREMENT ADDRESS BY 1
                                ;   13.  REPEAT STEPS 1-12 UNTIL ALL OF THE 1K ADDRESS HAVE BEEN CHECKED.
                                ;--

                                        BGNTST
011406                          T21::
011406  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
011412  005037  006374                  CLR     TRADRS                  ;SET TRACE RAM ADDRESS TO ZERO
011416  012701  125252                  MOV     #125252,R1              ;SETUP STARTING DATA PATTERN

011422                          1$:     BGNSEG
011422  104404                          TRAP    C$BSEG

                                ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING ZERO
                                ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE
                                ;TRACE RAM DATA IN BUFFERS

011424  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
011430  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
011434  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011436                                  ERRDF   1,,R0EROR               ;REGISTER 0 LOW BYTE NOT 0
011436  104455                          TRAP    C$ERDF
011440  000001                          .WORD   1
011442  000000                          .WORD   0
011444  004604                          .WORD   R0EROR
011446                                  CKLOOP
011446  104406                          TRAP    C$CLP1

                                ;LOAD TRACE RAM ADDRESS REGISTER WITH CONTENTS OF LOCATION "TRADRS"

011450  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0 WITH A DATA
                                ;PATTERN OF 125252 OR 052525.

011454  010137  002414                  MOV     R1,R6LOAD               ;SETUP DATA PATTERN TO BE LOADED
```

```
4431  011460  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4432  011464  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
4433
4434                                          ;WRITE THE TRACE RAM LOCATION ADDRESSED BY TRACE RAM ADDRESS REGISTER
4435                                          ;WITH THE DATA PATTERN STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 15.0.
4436
4437  011466  012777  000000  170662          MOV     #0,@REG6                ;WRITE THE RAM FROM DATA IN BUFFERS
4438
4439                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
4440                                          ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
4441                                          ;BITS TRDI 15:0 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
4442                                          ;THE SIGNAL RPT1 H.
4443
4444  011474  052737  000004  002370          BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
4445  011502  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
4446  011506  000405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4447  011510                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
4448  011510  104455                          TRAP    C$ERDF
4449  011512  000001                          .WORD   1
4450  011514  000000                          .WORD   0
4451  011516  004604                          .WORD   ROEROR
4452  011520                                  CKLOOP
4453  011520  104406                          TRAP    C$CLP1
4454
4455                                          ;READ DATA FROM TRACE RAM BITS TRDI 15:0
4456
4457  011522  017737  170630  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM THE RAM
4458  011530  023737  002414  002420          CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED INTO TRACE RAM
4459                                                                          ;DATA IN BUFFERS TRDI 15:0 WITH DATA
4460                                                                          ;READ FROM THE TRACE RAM
4461  011536  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
4462  011540                                  ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR TRDI 15:0
4463  011540  104455                          TRAP    C$ERDF
4464  011542  000004                          .WORD   4
4465  011544  002776                          .WORD   TRAM15
4466  011546  004764                          .WORD   TRAMER
4467  011550                          4$:     ENDSEG
4468  011550                          10000$:
4469  011550  104405                          TRAP    C$ESEG
4470
4471  011552  005701                          TST     R1                      ;CHECK DATA PATTERN TO SEE IF DONE
4472  011554  100002                          BPL     5$                      ;IF DONE THEN UPDATE TO NEXT ADDRESS
4473  011556  005101                          COM     R1                      ;MAKE PATTERN 052525
4474  011560  000720                          BR      1$                      ;GO DO THIS PATTERN
4475  011562  005101                  5$:     COM     R1                      ;MAKE DATA PATTERN 125252
4476  011564  005237  006374                  INC     TRADRS                  ;UPDATE TO NEXT SEQUENTIAL ADDRESS
4477  011570  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES DONE
4478  011576  001711                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
4479  011600                                  ENDTST
4480  011600                          L10067:
4481  011600  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 22: TRAM DATA TEST - TRDI 31:16 (125252-052525)

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM BITS TRDI 31:16 WITH A DATA PATTERN OF 125252
                                ; AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED FOR THIS DATA
                                ; PATTERN BEFORE THE NEXT SEQUENTIAL LOCATION IS CHECKED.
                                ;
                                ; THIS TEST IS PERFORMED IN THE FOLLOWING MANNER:
                                ;    1.  CLEAR LOW BYTE OF CONTROL REGISTER 0 TO SET SIGNAL TRSLO L
                                ;    2.  SET PTER0 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    3.  WRITE AND READ TRAM ADDRESS REG VIA SIGNALS WPT0 L AND RPT0 H
                                ;    4.  SET PTER6 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    5.  WRITE DATA PATTERN (125252-052525) INTO TRAM DATA IN BUF BITS TRDI 31:16
                                ;        VIA WPT6 H AND WRITE TO CONTROL REGISTER 6.
                                ;    6.  SET PTER2 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    7.  READ DATA PATTERN FROM TRAM DATA IN BUFFER VIA RPT2 H AND READ TO REG 6
                                ;    8.  WRITE TRACE RAM VIA WPT2 H AND WRITE TO CONTROL REGISTER 6
                                ;    9.  SET SIGNAL TRSL1 L BY SETTING CDAL2 = 1 IN REGISTER 0
                                ;   10.  READ TRACE RAM VIA RPT2 H AND READ TO CONTROL REGISTER 6
                                ;   11.  COMPLEMENT DATA PATTERN - REPEAT STEPS 1-10 WITH THIS PATTERN
                                ;   12.  RESET DATA PATTERN TO 125.52 - INCREMENT ADDRESS BY 1
                                ;   13.  REPEAT STEPS 1-12 UNTIL A L OF THE 1K ADDRESS HAVE BEEN CHECKED.
                                ;--

011602                                  BGNTST
011602                          T22::
011602  004737  005474                 JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
011606  005037  006374                 CLR     TRADRS                  ;SET TRACE RAM ADDRESS TO ZERO
011612  012701  125252                 MOV     #125252,R1              ;SETUP STARTING DATA PATTERN

011616                          1$:     BGNSEG
011616  104404                         TRAP    C$BSEG

                                ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING ZERO
                                ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE
                                ;TRACE RAM DATA IN BUFFERS

011620  105037  002370                 CLRB    ROLOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
011624  004737  006102                 JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
011630  001405                         BEQ     2$                      ;IF LOADED OK THEN CONTINUE
011632                                  ERRDF   1,,ROEROR               ;REGISTER 0 LOW BYTE NOT 0
011632  104455                         TRAP    C$ERDF
011634  000001                         .WORD   1
011636  000000                         .WORD   0
011640  004604                         .WORD   ROEROR
011642                                  CKLOOP
011642  104406                         TRAP    C$CLP1

                                ;LOAD TRACE RAM ADDRESS REGISTER WITH CONTENTS OF LOCATION "TRADRS"

011644  004737  006310         2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 31:16 WITH A DATA
                                ;PATTERN OF 125252 OR 052525.

011650  010137  006414                 MOV     R1,R6LOAD               ;SETUP DATA PATTERN TO BE LOADED
```

```
4538  011654  004537  006426              JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4539  011660  000006                      .WORD   PTER6                   ;SELECT TRDI BITS 31:16
4540
4541                                      ;WRITE THE TRACE RAM LOCATION ADDRESSED BY TRACE RAM ADDRESS REGISTER
4542                                      ;WITH THE DATA PATTERN STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 31:16.
4543
4544  011662  012777  000000  170466      MOV     #0,@REG6                ;WRITE THE RAM FROM DATA IN BUFFERS
4545
4546                                      ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
4547                                      ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
4548                                      ;BITS TRDI 31:16 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
4549                                      ;THE SIGNAL RPT2 H.
4550
4551  011670  052737  000004  002370      BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
4552  011676  004737  006102              JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
4553  011702  001405                      BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4554  011704                              ERRDF   1,,ROERROR              ;REGISTER 0 NOT EQUAL EXPECTED
4555  011704  104455                      TRAP    C$ERDF
4556  011706  000001                      .WORD   1
4557  011710  000000                      .WORD   0
4558  011712  004604                      .WORD   ROERROR
4559  011714                              CKLOOP
4560  011714  104406                      TRAP    C$CLP1
4561
4562                                      ;READ DATA FROM TRACE RAM BITS TRDI 31:16
4563
4564  011716  017737  170434  002420  3$: MOV     @REG6,R6READ            ;READ DATA FROM THE RAM
4565  011724  023737  002414  002420      CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED INTO TRACE RAM
4566                                                                      ;DATA IN BUFFERS TRDI 31:16 WITH DATA
4567                                                                      ;READ FROM THE TRACE RAM
4568  011732  001404                      BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
4569  011734                              ERRDF   4,TRAM31,TRAMER         ;TRAM DATA ERROR TRDI 31:16
4570  011734  104455                      TRAP    C$ERDF
4571  011736  000004                      .WORD   4
4572  011740  003032                      .WORD   TRAM31
4573  011742  004764                      .WORD   TRAMER
4574  011744                          4$: ENDSEG
4575  011744                          10000$:
4576  011744  104405                      TRAP    C$ESEG
4577
4578  011746  005701                      TST     R1                      ;CHECK DATA PATTERN TO SEE IF DONE
4579  011750  100002                      BPL     5$                      ;IF DONE THEN UPDATE TO NEXT ADDRESS
4580  011752  005101                      COM     R1                      ;MAKE PATTERN 052525
4581  011754  000720                      BR      1$                      ;GO DO THIS PATTERN
4582  011756  005101                  5$: COM     R1                      ;MAKE DATA PATTERN 125252
4583  011760  005237  006374              INC     TRADRS                  ;UPDATE TO NEXT SEQUENTIAL ADDRESS
4584  011764  032737  002000  006374      BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES DONE
4585  011772  001711                      BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
4586  011774                              ENDTST
4587  011774                          L10070:
4588  011774  104401                      TRAP    C$ETST
```

```
                                .SBTTL  TEST 23: TRAM DATA TEST - TRDI 47:32 (125252-052525)

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM BITS TRDI 47:32 WITH A DATA PATTERN OF 125252
                                ; AND 052525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED FOR THIS DATA
                                ; PATTERN BEFORE THE NEXT SEQUENTIAL LOCATION IS CHECKED.
                                ;
                                ; THIS TEST IS PERFORMED IN THE FOLLOWING MANNER:
                                ;    1.  CLEAR LOW BYTE OF CONTROL REGISTER 0 TO SET SIGNAL TRSLO L
                                ;    2.  SET PTER0 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    3.  WRITE AND READ TRAM ADDRESS REG VIA SIGNALS WPT0 L AND RPT0 H
                                ;    4.  SET PTER7 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    5.  WRITE DATA PATTERN (125252-052525) INTO TRAM DATA IN BUF BITS TRDI 47:32
                                ;        VIA WPT7 H AND WRITE TO CONTROL REGISTER 6
                                ;    6.  SET PTER3 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    7.  READ DATA PATTERN FROM TRAM DATA IN BUFFER VIA RPT3 H AND READ TO REG 6
                                ;    8.  WRITE TRACE RAM VIA WPT3 H AND WRITE TO CONTROL REGISTER 6
                                ;    9.  SET SIGNAL TRSL1 L BY SETTING CDAL2 = 1 IN REGISTER 0
                                ;   10.  READ TRACE RAM VIA RPT3 H AND READ TO CONTROL REGISTER 6
                                ;   11.  COMPLEMENT DATA PATTERN - REPEAT STEPS 1-10 WITH THIS PATTERN
                                ;   12.  RESET DATA PATTERN TO 125252 - INCREMENT ADDRESS BY 1
                                ;   13.  REPEAT STEPS 1-12 UNTIL ALL OF THE 1K ADDRESS HAVE BEEN CHECKED.
                                ;--

                                        BGNTST
011776                          T23::
011776  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
012002  005037  006374                  CLR     TRADRS                  ;SET TRACE RAM ADDRESS TO ZERO
012006  012701  125252                  MOV     #125252,R1              ;SETUP STARTING DATA PATTERN

012[illegible]                  1$:     BGNSEG
012[illegible]  104404                  TRAP    C$BSEG

                                ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING ZERO
                                ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE
                                ;TRACE RAM DATA IN BUFFERS

012014  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
012020  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
012024  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012026                                  ERRDF   1,,ROEROR               ;REGISTER 0 LOW BYTE NOT 0
012026  104455                          TRAP    C$ERDF
012030  000001                          .WORD   1
012032  000000                          .WORD   0
012034  004604                          .WORD   ROEROR
012036                                  CKLOOP
012036  104406                          TRAP    C$CLP1

                                ;LOAD TRACE RAM ADDRESS RECISTER WITH CONTENTS OF LOCATION "TRADRS"

012040  004737  006310          2$      JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 47:32 WITH A DATA
                                ;PATTERN OF 125252 OR 052525.

012044  010137  002414                  MOV     R1,R6LOAD               ;SETUP DATA PATTERN TO BE LOADED
```

```
4645  012050  004537  006426              JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
4646  012054  000007                      .WORD   PTER7                   ;SELECT TRDI BITS 47:32
4647
4648                                      ;WRITE THE TRACE RAM LOCATION ADDRESSED BY TRACE RAM ADDRESS REGISTER
4649                                      ;WITH THE DATA PATTERN STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 47:32.
4650
4651  012056  012777  000000  170272      MOV     #0,@REG6                ;WRITE THE RAM FROM DATA IN BUFFERS
4652
4653                                      ;SET CDAL2 TO A ONE AND CDAL 5 TO A 0 IN CONTROL REGISTER 0 TO SET THE
4654                                      ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
4655                                      ;BITS TRDI 47:32 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
4656                                      ;THE SIGNAL RPT3 H.
4657
4658  012064  052737  000004  002370      BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
4659  012072  004737  006102              JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
4660  012076  001405                      BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4661  012100                              ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
4662  012100  104455                      TRAP    C$ERDF
4663  012102  000001                      .WORD   1
4664  012104  000000                      .WORD   0
4665  012106  004604                      .WORD   ROEROR
4666  012110                              CKLOOP
4667  012110  104406                      TRAP    C$CLP1
4668
4669                                      ;READ DATA FROM TRACE RAM BITS TRDI 47:32
4670
4671  012112  017737  170240  002420  3$: MOV     @REG6,R6READ            ;READ DATA FROM THE RAM
4672  012120  023737  002414  002420      CMP     R6LOAD,R6READ           ;COMPARE DATA LOADED INTO TRACE RAM
4673                                                                      ;DATA IN BUFFERS TRDI 47:32 WITH DATA
4674                                                                      ;READ FROM THE TRACE RAM
4675  012126  001404                      BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
4676  012130                              ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR TRDI 47:32
4677  012130  104455                      TRAP    C$ERDF
4678  012132  000004                      .WORD   4
4679  012134  003067                      .WORD   TRAM47
4680  012136  004764                      .WORD   TRAMER
4681  012140                          4$: ENDSEG
4682  012140                          10000$:
4683  012140  104405                      TRAP    C$ESEG
4684
4685  012142  005701                      TST     R1                      ;CHECK DATA PATTERN TO SEE IF DONE
4686  012144  100002                      BPL     5$                      ;IF DONE THEN UPDATE TO NEXT ADDRESS
4687  012146  005101                      COM     R1                      ;MAKE PATTERN 052525
4688  012150  000720                      BR      1$                      ;GO DO THIS PATTERN
4689  012152  005101                  5$: COM     R1                      ;MAKE DATA PATTERN 125252
4690  012154  005237  006374              INC     TRADRS                  ;UPDATE TO NEXT SEQUENTIAL ADDRESS
4691  012160  032737  002000  006374      BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES DONE
4692  012166  001711                      BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
4693  012170                              ENDTST
4694  012170                          L10071:
4695  012170  104401                      TRAP    C$ETST
```

```
                                .SBTTL  TEST 24: TRAM DATA TEST - TRDI 55:48 (252-525)

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM BITS TRDI 55:48 WITH A DATA PATTERN OF 252
                                ; AND 525. EACH LOCATION OF THE 1K TRACE RAM WILL BE CHECKED WITH THESE DATA
                                ; PATTERNS BEFORE THE NEXT LOCATION IS CHECKED. WHEN LOADING THE TRACE RAM
                                ; DATA IN BUFFER BITS TRDI 59:48, THE FOLLOWING DATA PATTERN WILL BE LOADED
                                ; INTO TRDI BITS 59:48, 5252 AND 2525. WHEN DATA IS CLOCKED FROM THE TRACE
                                ; RAM DATA IN BUFFER TO THE TRACE RAM, ONLY TRDI BITS 55:48 ARE LOADED INTO THE
                                ; TRACE RAM. THERE IS NO TRACE RAM FOR BITS TRDI 59:56.
                                ; THIS TEST IS PERFORMED IN THE FOLLOWING MANNER:
                                ;    1.  CLEAR LOW BYTE OF CONTROL REGISTER 0 TO SET SIGNAL TRSLO L
                                ;    2.  SET PTER0 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    3.  WRITE AND READ TRAM ADDRESS REG VIA SIGNALS WPT0 L AND RPT0 H
                                ;    4.  SET PTER8 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    5.  WRITE DATA PATTERN (5252-2525) INTO TRAM DATA IN BUF BITS TRDI 59:48
                                ;        VIA WPT8 H AND WRITE TO CONTROL REGISTER 6.
                                ;    6.  SET PTER4 L IN POINTER REGISTER VIA CONTROL REGISTER 2
                                ;    7.  READ DATA PATTERN FROM TRAM DATA IN BUFFER VIA RPT4 H AND READ TO REG 6
                                ;    8.  WRITE TRACE RAM VIA WPT4 H AND WRITE TO CONTROL REGISTER 6
                                ;    9.  SET SIGNAL TRSL1 L BY SETTING CDAL2 = 1 IN REGISTER 0
                                ;   10.  READ TRACE RAM VIA RPT4 H AND READ TO CONTROL REGISTER 6
                                ;   11.  COMPLEMENT DATA PATTERN - REPEAT STEPS 1-10 WITH THIS PATTERN
                                ;   12.  RESET DATA PATTERN TO 5252 - INCREMENT ADDRESS BY 1
                                ;   13.  REPEAT STEPS 1-12 UNTIL ALL OF THE 1K ADDRESS HAVE BEEN CHECKED.
                                ;--

012172                                  BGNTST
012172                          T24::
012172  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
012176  005037  006374                  CLR     TRADRS                  ;SET TRACE RAM ADDRESS TO ZERO
012202  012701  005252                  MOV     #5252,R1                ;SETUP STARTING DATA PATTERN

012206                          1$:     BGNSEG
012206  1044 ,4                        TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING ZERO
                                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE
                                        ;TRACE RAM DATA IN BUFFERS

012210  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
012214  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CEHCK REGISTER 0
012220  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012222                                  ERRDF   1,,ROEROR               ;REGISTER 0 LOW BYTE NOT 0
012222  104455                          TRAP    C$ERDF
012224  000001                          .WORD   1
012226  000000                          .WORD   0
012230  004604                          .WORD   ROEROR
012232                                  CKLOOP
012232  104406                          TRAP    C$CLP1

                                        ;LOAD TRACE RAM ADDRESS REGISTER WITH CONTENTS OF LOCATION "TRADRS"

012234  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 59:48 WITH A DATA
```

```
                                        ;PATTERN OF 5252 OR 2525.
                                        
012240  010137  002414                  MOV     R1,R6LOAD               ;SETUP DATA PATTERN TO BE LOADED
012244  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
012250  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
                                        
                                        ;WRITE THE TRACE RAM LOCATION ADDRESSED BY TRACE RAM ADDRESS REGISTER
                                        ;WITH THE DATA PATTERN STORED IN THE TRACE RAM DATA IN BUFFER BITS TRDI 55:48.
                                        
012252  012777  000000  170076          MOV     #0,@REG6                ;WRITE THE RAM FROM DATA IN BUFFERS
                                        
                                        ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
                                        ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
                                        ;BITS TRDI 55:48 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
                                        ;THE SIGNAL RPT4 H.
                                        
012260  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
012266  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
012272  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
012274                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
012274  104455                          TRAP    C$ERDF
012276  000001                          .WORD   1
012300  000000                          .WORD   0
012302  004604                          .WORD   R0EROR
012304                                  CKLOOP
012304  104406                          TRAP    C$CLP1
                                        
                                        ;READ DATA FROM TRACE RAM BITS TRDI 55:48
                                        
012306  017737  170044  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM THE RAM
012314  042737  177400  002420          BIC     #177400,R6READ          ;CLEAR BITS NOT IN TRACE RAM
012322  042737  177400  002414          BIC     #177400,R6LOAD          ;CLEAR BITS NOT LOADED INTO TRACE RAM
012330  023737  002414  002420          CMP     R6LOAD R6READ           ;COMPARE DATA LOADED INTO TRACE RAM
                                                                        ;DATA IN BUFFERS TRDI 55:48 WITH DATA
                                                                        ;READ FROM THE TRACE RAM
012336  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
012340                                  ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR TRDI 55:48
012340  104455                          TRAP    C$ERDF
012342  000004                          .WORD   4
012344  003124                          .WORD   TRAM55
012346  004764                          .WORD   TRAMER
012350                          4$:     ENDSEG
012350                          10000$:
012350  104405                          TRAP    C$ESEG
012352  022701  002525                  CMP     #2525,R1                ;CHECK TO SEE IF DATA PATTERNS DONE
012356  001403                          BEQ     5$                      ;IF YES THEN UPDATE THE ADDRESS
012360  012701  002525                  MOV     #2525,R1                ;COMPLEMENT THE DATA PATTERN LOADED
012364  000710                          BR      1$                      ;GO LOAD THIS DATA PATTERN INTO RAM
012366  012701  005252          5$:     MOV     #5252,R1                ;RESET THE DATA PATTERN
012372  005237  006374                  INC     TRADRS                  ;UPDATE TO NEXT SEQUENTIAL ADDRESS
012376  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES DONE
012404  001700                          BEQ     1$                      ;IF NOT THEN DO NEXT SET OF ADDRESSES
012406                                  ENDTST
012406                          L10072:
012406  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 25: TRAM ADDRESS/SHORT TEST - TRDI 15:0

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM TRDI 15:0 TO BE ADDRESSED CORRECTLY AND THAT
                                ; NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIP'S. THE TEST WILL
                                ; LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE
                                ; ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK THE ADDRESS TO CONTAIN ITS
                                ; ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRES  INTO
                                ; THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN.  THE TEST WILL
                                ; REPEAT THIS SEQUENCE FOR ALL ADDRESSES IN THE TRACE RAM.  WHEN ALL ADDRESSES
                                ; HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK ALL OF THE RAM TO CONTAIN THE
                                ; ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
                                ;--

012410                                  BGNTST
012410                          T25::
012410  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        ;THE FOLLOWING SUB TEST WILL WRITE EACH LOCATION OF TRACE RAM TRDI 15:0
                                        ;WITH A DATA PATTERN EQUAL TO ITS ADDRESS.  AS EACH LOCATION IS WRITT
                                        ;THE TEST WILL READ THE LOCATION AND CHECK THAT THE DATA EQUALS ITS
                                        ;ADDRESS.

012414                                  BGNSUB
012414                          T25.1:
012414  104402                          TRAP    C$BSUB
012416  005037  006374                   CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
012422                          1$:     BGNSEG
012422  104404                          TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING A ZERO
                                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE
                                        ;RAM DATA IN BUFFERS.

012424  105037  002370                   CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
012430  004737  006102                   JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
012434  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
012436                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
012436  104455                          TRAP    C$ERDF
012440  000001                          .WORD   1
012442  000000                          .WORD   0
012444  004604                          .WORD   ROEROR
012446                                  CKLOOP
012446  104406                          TRAP    C$CLP1

                                        ;WRITE AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF LOCA-
                                        ;TION "TRADRS". THE POINTER REGISTER ON EXIT FROM ROUTINE TRADLD WILL
                                          "E THE SIGNAL PTERO L ASSERTED.

012450  004737  006310           2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;WRITE THE TRACE RAM ADDRESS INTO THE TRACE RAM DATA IN BUFFERS IN
                                        ;BUFFER BITS TRDI 15:0. ON EXIT FROM ROUTINE "TRDIBF" THE POINTER
                                        ;REGISTER WILL HAVE THE SIGNAL P'ER1 L ASSERTED.
```

```
4863
4864  012454  013737  006374  002414          MOV     TRADRS,R6LOAD           ;SETUP DATA TO EQUAL TRAM ADDRESS REG
4865  012462  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
4866  012466  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
4867
4868                                          ;WRITE THE ADDRESS IN THE TRACE RAM DATA IN BUFFERS INTO TRACE RAM
4869                                          ;BITS TRDI 15:0
4870
4871  012470  012777  000000  167660          MOV     #0,@REG6                ;WRTIE RAM WITH DATA IN BUFFERS
4872
4873                                          ;SET CDAL2 TO 1 AND CDAL3 TO 0 IN CONTROL REGISTER 0 TO SET THE SIGNAL
4874                                          ;TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW THE DATA IN THE TRACE RAM TO
4875                                          ;BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT1 H.
4876
4877  012476  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
4878  012504  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
4879  012510  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4880  012512                                  ERRDF   1,,R0ERR0               ;REGISTER 0 NOT EQUAL EXPECTED
4881  012512  104455                          TRAP    C$ERDF
4882  012514  000001                          .WORD   1
4883  012516  000000                          .WORD   0
4884  012520  004604                          .WORD   R0ERR0
4885  012522                                  CKLOOP
4886  012522  104406                          TRAP    C$CLP1
4887
4888                                          ;READ AND CHECK TRACE RAM DATA TRDI 15:0.  THE DATA SHOULD EQUAL THE
4889                                          ;ADDRESS BEING TESTED.
4890
4891  012524  017737  167626  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM TRDI 15:0
4892  012532  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED TO EQUAL DATA READ
4893  012540  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
4894  012542                                  ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR - TRDI 15:0
4895  012542  104455                          TRAP    C$ERDF
4896  012544  000004                          .WORD   4
4897  012546  002776                          .WORD   TRAM15
4898  012550  004764                          .WORD   TRAMER
4899  012552                          4$:     ENDSEG
4900  012552                          10000$:
4901  012552  104405                          TRAP    C$ESEG
4902  012554  005237  006374                  INC     TRADRS                  ;UPDATE TRACE RAM ADDRESS BY 1
4903  012560  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF 1K YET
4904  012566  001715                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
4905  012570                                  ENDSUB
4906  012570                          L10074:
4907  012570  104403                          TRAP    C$ESUB
4908
4909                                          ;THE FOLLOWING SUB TEST WIL. RESET THE POINTER TO THE BEGINNING
4910                                          ;ADDRESS OF THE TRACE RAM, CHECK THE LOCATION TO EQUAL ITS ADDRESS,
4911                                          ;WRITE,READ, AND CHECK THE LOCATION WITH THE ONES COMPLEMENT OF ITS
4912                                          ;ADDRESS. THIS SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE TRACE
4913                                          ;RAM FOR TRACE RAM TRDI 15:0. THIS TEST WILL CHECK THAT THE TRACE RAM
4914                                          ;CAN BE ADDRESSED CORRECTLY AND THAT WRITING A LOCATION DOES NOT WRITE
4915                                          ;A HIGHER LOCATION.
4916
4917  012572                                  BGNSUB
4918  012572                          T25.2:
```

```
4919  012572  104402                          TRAP    C$BSEG
4920  012574  005037  006374                  CLR     TRADRS                  ;RESET TRAM ADDRESS TO ADDRESS 0
4921
4922  012600                          1$:     BGNSEG
4923  012600  104404                          TRAP    C$BSEG
4924
4925                                          ;SET CDAL2 TO A 1 AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
4926                                          ;SIGNAL TRSL1 L. THIS SIGNAL WILL ALLOW THE TRACE RAM TO BE READ ON A
4927                                          ;READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT1 H.
4928
4929  012602  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
4930  012610  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
4931  012614  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
4932  012616                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
4933  012616  104455                          TRAP    C$ERDF
4934  012620  000001                          .WORD   1
4935  012622  000000                          .WORD   0
4936  012624  004604                          .WORD   ROEROR
4937  012626                                  CKLOOP
4938  012626  104406                          TRAP    C$CLP1
4939
4940                                          ;GO LOAD ADDRESS TO BE CHECKED INTO TRACE RAM ADDRESS REGISTER USING
4941                                          ;THE CONTENTS OF LOCATION "TRADRS" AS THE ADDRESS TO BE LOADED. ON
4942                                          ;EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER WILL HAVE THE SIGNAL
4943                                          ;PTER0 L ASSERTED.
4944
4945  012630  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
4946
4947                                          ;SET THE SIGNAL PTER1 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
4948
4949  012634  012737  000001  002376          MOV     #PTER1,R2LOAD           ;SETUP REGISTER 2 BITS TO BE LOADED
4950  012642  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
4951  012646  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
4952  012650                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
4953  012650  104455                          TRAP    C$ERDF
4954  012652  000002                          .WORD   2
4955  012654  000000                          .WORD   0
4956  012656  004704                          .WORD   R2EROR
4957  012660                                  CKLOOP
4958  012660  104406                          TRAP    C$CLP1
4959
4960                                          ;READ THE DATA THAT WAS PREVIOUSLY WRITTEN IN THE FIRST SUB TEST AND
4961                                          ;CHECK THAT THE DATA IS EQUAL TO THE ADDRESS BEING TESTED.
4962
4963  012662  013737  006374  002414  3$:     MOV     TRADRS,R6LOAD           ;SETUP DATA PREVIOUSLY WRITTEN
4964  012670  017737  167462  002420          MOV     @REG6,R6READ            ;READ THE DATA FROM THE TRACE RAM
4965  012676  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK IF DATA IS EQUAL TO ITS ADDRESS
4966  012704  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
4967  012706                                  ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR - TRDI 15:0 OR ADDRESS
4968  012706  104455                          TRAP    C$ERDF
4969  012710  000004                          .WORD   4
4970  012712  002776                          .WORD   TRAM15
4971  012714  004764                          .WORD   TRAMER
4972                                                                          ;FAILURE OR ADDRESS SHORT
4973  012716                          4$:     ENDSEG
4974  012716                          10000$:
```

```
 4975  012716  104405                          TRAP    C$ESEG
 4976
 4977                                          ;THE FOLLOWING SECTION OF CODE WILL WRITE THE TRACE RAM DATA IN BUFFERS
 4978                                          ;AND THE TRACE RAM WITH THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
 4979
 4980  012720                                  BGNSEG
 4981  012720  104404                          TRAP    C$BSEG
 4982
 4983                                          ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSL0 L. THE
 4984                                          ;SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
 4985
 4986  012722  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
 4987  012726  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
 4988  012732  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
 4989  012734                                  ERRDF   1,,R0ERR                ;REGISTER 0 NOT EQUAL EXPECTED
 4990  012734  104455                          TRAP    C$ERDF
 4991  012736  000001                          .WORD   1
 4992  012740  000000                          .WORD   0
 4993  012742  004604                          .WORD   R0ERR
 4994  012744                                  CKLOOP
 4995  012744  104406                          TRAP    C$CLP1
 4996
 4997                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0 WITH DATA
 4998                                          ;EQUAL TO THE ONES COMPLEMENT OF THE ADDRESS. ON EXIT FROM ROUTINE
 4999                                          ;"TRDIBF", THE POINTER REGISTER WILL HAVE THE SIGNAL PTER1 L ASSERTED.
 5000
 5001  012746  013737  006374  002414  5$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS UNDER TEST
 5002  012754  005137  002414                  COM     R6LOAD                  ;COMPLEMENT THE ADDRESS
 5003  012760  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
 5004  012764  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
 5005
 5006                                          ;WRITE TRACE RAM LOCATION WITH DATA PATTERN EQUAL TO THE COMPLEMENT
 5007                                          ;OF ITS ADDRESS.  THE DATA TO BE WRITTEN INTO THE TRACE RAM IS
 5008                                          ;STORED IN THE TRACE RAM DATA IN BUFFERS TRDI 15:0.
 5009
 5010  012766  012777  000000  167362          MOV     #0,@REG6                ;WRITE RAM WITH TRAM DATA IN BUF
 5011
 5012                                          ;SET CDAL2 TO A 1 AND CDAL 3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
 5013                                          ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
 5014                                          ;BITS TRDI 15:0 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
 5015                                          ;THE SIGNAL RPT1 H.
 5016
 5017  012774  052737  000004  002370          BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
 5018  013002  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
 5019  013006  001405                          BEQ     6$                      ;IF LOADEDOK THEN CONTINUE
 5020  013010                                  ERRDF   1,,R0ERR                ;REGISTER 0 NOT EQUAL EXPECTED
 5021  013010  104455                          TRAP    C$ERDF
 5022  013012  000001                          .WORD   1
 5023  013014  000000                          .WORD   0
 5024  013016  004604                          .WORD   R0ERR
 5025  013020                                  CKLOOP
 5026  013020  104406                          TRAP    C$CLP1
 5027
 5028                                          ;READ DATA FROM THE TRACE RAM TRDI 15:0 CHECKING THE DATA TO BE THE
 5029                                          ;ONES COMPLEMENT OF THE ADDRESS UNDER TEST
 5030
```

```
5031  013022  017737  167330  002420  6$:     MOV     @REG6,R6READ            ;READ DATA FROM THE TRACE RAM
5032  013030  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5033  013036  001404                          BEQ     7$                      ;ID DATA EQUAL THEN CONTINUE
5034  013040                                  ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR - TRDI 15:0
5035  013040  104455                          TRAP    C$ERDF
5036  013042  000004                          .WORD   4
5037  013044  002776                          .WORD   TRAM15
5038  013046  004764                          .WORD   TRAMER
5039  013050                          7$:     ENDSEG
5040  013050                          10001$:
5041  013050  104405                          TRAP    C$ESEG
5042  013052  005237  006374                  INC     TRADRS                  ;UPDATE THE ADDRESS BY 1
5043  013056  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES HAVE BEEN TESTED
5044  013064  001645                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5045  013066                                  ENDSUB
5046  013066                          L10075:
5047  013066  104403                          TRAP    C$ESUB
5048
5049                                          ;THE FOLLOWING SUB TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING
5050                                          ;ADDRESS OF THE TRACE RAM AND CHECK EACH LOCATION OF THE TRACE RAM TO
5051                                          ;CONTAIN THE ONES COMPLEMENT OF ITS ADDRESS. IN A FAILURE OCCURS, THE
5052                                          ;ERROR MAY BE AN ADDRESS SHORT IN WHICH WRITING A LOCATION IN THE
5053                                          ;PREVIOUS SUB TEST WROTE A LOCATION LOWER THEN THE ADDRESS BEING TESTED.
5054
5055  013070                                  BGNSUB
5056  013070                          T25.3:
5057  013070  104402                          TRAP    C$BSUB
5058  013072  005037  006374                  CLR     TRADRS                  ;CLEAR THE ADDRESS TO ADDRESS 0
5059
5060  013076                          1$:     BGNSEG
5061  013076  104404                          TRAP    C$BSEG
5062
5063                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO ASSERT
5064                                          ;THE SIGNAL TRSL1 L.  THE SIGNAL TRSL1 L WILL ALLOW THE DATA FROM THE
5065                                          ;TRACE RAM BITS TRDI 15:0 TO BE READ ON A READ COMMAND TO CONTROL
5066                                          ;REGISTER 6 VIA THE SIGNAL RPT1 H.
5067
5068  013100  112737  000004  002370          MOVB    #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5069  013106  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
5070  013112  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5071  013114                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5072  013114  104455                          TRAP    C$ERDF
5073  013116  000001                          .WORD   1
5074  013120  000000                          .WORD   0
5075  013122  004604                          .WORD   R0EROR
5076  013124                                  CKLOOP
5077  013124  104406                          TRAP    C$CLP1
5078
5079                                          ;LOAD,READ AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF
5080                                          ;LOCATION "TRADRS".  ON EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER
5081                                          ;WILL HAVE THE SIGNAL PTER0 L ASSERTED.
5082
5083  013126  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ & CHECK TRAM ADDRESS REG
5084
5085                                          ;SET SIGNAL PTER1 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5086
```

```
5087  013132  012737  000001  002376          MOV     #PTER1,R2LOAD           ;SETUP BITS TO BE LOADED
5088  013140  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5089  013144  001405                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
5090  013146                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5091  013146  104455                          TRAP    C$ERDF
5092  013150  000002                          .WORD   2
5093  013152  000000                          .WORD   0
5094  013154  004704                          .WORD   R2EROR
5095  013156                                   CKLOOP
5096  013156  104406                          TRAP    C$CLP1
5097
5098                                           ;READ DATA PREVIOUSLY WRITTEN IN THE LAST SUB TEST CHECKING THE DATA
5099                                           ;TO BE THE COMPLEMENT OF THE ADDRESS.
5100
5101  013160  013737  006374  002414  3$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS BEING TESTED
5102  013166  005137  002414                  COM     R6LOAD                  ;MAKE IT THE ONES COMPLEMENT
5103  013172  017737  167160  002420          MOV     @R[G6,R6READ            ;READ DATA FROM TRACE RAM
5104  013200  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5105  013206  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5106  013210                                   ERRDF   4,TRAM15,TRAMER         ;TRAM DATA ERROR - TRDI 15:0
5107  013210  104455                          TRAP    C$ERDF
5108  013212  000004                          .WORD   4
5109  013214  002[illegible]                  .WORD   TRAM15
5110  013216  004764                          .WORD   TRAMER
5111  013220                           4$:     ENDSEG
5112  013220                           10000$:
5113  013220  104405                          TRAP    C$ESEG
5114  013222  005237  006374                  INC     TRADRS                  ;UPDATE THE ADDRESS BY ONE
5115  013226  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES CHECKED
5116  013234  001720                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5117  013236                                   ENDSUB
5118  013236                           L10076:
5119  013236  104403                          TRAP    C$ESUB
5120  013240                                   ENDTST
5121  013240                           L10073:
5122  013240  104401                          TRAP    C$ETST
5123
```

```
                                .SBTTL  TEST 26: TRAM ADDRESS/SHORT TEST - TRDI 31:16

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM TRDI 31:16 TO BE ADDRESSED CORRECTLY AND THAT
                                ; NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIP'S. THE TEST WILL
                                ; LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE
                                ; ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK THE ADDRESS TO CONTAIN ITS
                                ; ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO
                                ; THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN.  THE TEST WILL
                                ; REPEAT THIS SEQUENCE FOR ALL ADDRESSES IN THE TRACE RAM.  WHEN ALL ADDRESSES
                                ; HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK ALL OF THE RAM TO CONTAIN THE
                                ; ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
                                ;--

013242                                  BGNTST
013242                          T26::
013242  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        ;THE FOLLOWING SUB TEST WILL WRITE EACH LOCATION OF TRACE RAM TRDI 31:16
                                        ;WITH A DATA PATTERN EQUAL TO ITS ADDRESS.  AS EACH LOCATION IS WRITTEN,
                                        ;THE TEST WILL READ THE LOCATION AND CHECK THAT THE DATA EQUALS ITS
                                        ;ADDRESS.

013246                                  BGNSUB
013246                          T26.1:
013246  104402                          TRAP    C$BSUB
013250  005037  006374                   CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
013254                          1$:     BGNSEG
013254  104404                          TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING A ZERO
                                        ;WILL SET THE SIGNAL TRSL0 L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE
                                        ;RAM DATA IN BUFFERS.

013256  105037  002370                   CLRB    R0LOAD                  ;SETUP TO CLEAR LOWER BYTE
013262  004737  006102                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
013266  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
013270                                  ERRDF   1,,R0ERR0               ;REGISTER 0 NOT EQUAL EXPECTED
013270  104455                          TRAP    C$ERDF
013272  000001                          .WORD   1
013274  000000                          .WORD   0
013276  004604                          .WORD   R0ERR0
013300                                  CKLOOP
013300  104406                          TRAP    C$CLP1

                                        ;WRITE AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF LOCA-
                                        ;TION "TRADRS". THE POINTER REGISTER ON EXIT FROM ROUTINE TRADLD WILL
                                        ;HAVE THE SIGNAL PTER0 L ASSERTED.

013302  004737  006310           2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;WRITE THE TRACE RAM ADDRESS INTO THE TRACE RAM DATA IN BUFFERS IN
                                        ;BUFFER BITS TRDI 31:16. ON EXIT FROM ROUTINE "TRDIBF" THE POINTER
                                        ;REGISTER WILL HAVE THE SIGNAL PTER2 L ASSERTED.
```

```
5180
5181  013306  013737  006374  002414          MOV     TRADRS,R6LOAD           ;SETUP DATA TO EQUAL TRAM ADDRES. .EG
5182  013314  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN B..
5183  013320  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
5184
5185                                          ;WRITE THE ADDRESS IN THE TRACE RAM DATA IN BUFFERS INTO TRACE RAM
5186                                          ;BITS TRDI 31:16
5187
5188  013322  012777  000000  167026          MOV     #0,@REG6                ;WRTIE RAM WITH DATA IN BUFFERS
5189
5190                                          ;SET CDAL2 TO 1 AND CDAL3 TO 0 IN CONTROL REGISTER 0 TO SET THE SIGNAL
5191                                          ;TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW THE DATA IN THE TRACE RAM TO
5192                                          ;BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT2 H.
5193
5194  013330  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5195  013336  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
5196  013342  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5197  013344                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5198  013344  104455                          TRAP    C$ERDF
5199  013346  000001                          .WORD   1
5200  013350  000000                          .WORD   0
5201  013352  004604                          .WORD   R0EROR
5202  013354                                  CKLOOP
5203  013354  104406                          TRAP    C$CLP1
5204
5205                                          ;READ AND CHECK TRACE RAM DATA TRDI 31:16.  THE DATA SHOULD EQUAL THE
5206                                          ;ADDRESS BEING TESTED.
5207
5208  013356  017737  166774  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM TRDI 31:16
5209  013364  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED TO EQUAL DATA READ
5210  013372  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
5211  013374                                  ERRDF   4,TRAM31,TRAMER         ;TRAM DATA ERROR - TRDI 31:16
5212  013374  104455                          TRAP    C$ERDF
5213  013376  000004                          .WORD   4
5214  013400  003032                          .WORD   TRAM31
5215  013402  004764                          .WORD   TRAMER
5216  013404                          4$:     ENDSEG
5217  013404                          10000$:
5218  013404  104405                          TRAP    C$ESEG
5219  013406  005237  006374                  INC     TRADRS                  ;UPDATE TRACE RAM ADDRESS BY 1
5220  013412  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF 1K YET
5221  013420  001715                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
5222  013422                                  ENDSUB
5223  013422                          L10100:
5224  013422  104403                          TRAP    C$ESUB
5225
5226                                          ;THE FOLLOWING SUB TEST WILL RESET THE POINTER TO THE BEGINNING
5227                                          ;ADDRESS OF THE TRACE RAM, CHECK THE LOCATION TO EQUAL ITS ADDRESS,
5228                                          ;WRITE,READ, AND CHECK THE LOCATION WITH THE ONES COMPLEMENT OF ITS
5229                                          ;ADDRESS. THIS SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE TRACE
5230                                          ;RAM FOR TRACE RAM TRDI 31:16. THIS TEST WILL CHECK THAT THE TRACE RAM
5231                                          ;CAN BE ADDRESSED CORRECTLY AND THAT WRITING A LOCATION DOES NOT WRITE
5232                                          ;A HIGHER LOCATION.
5233
5234  013424                                  BGNSUB
5235  013424                          T26.2:
```

```
5236  013424  104402                          TRAP    C$BSUB
5237  013426  005037  006374                  CLR     TRADRS                  ;RESET TRAM ADDRESS TO ADDRESS 0
5238
5239  013432                          1$:     BGNSEG
5240  013432  104404                          TRAP    C$BSEG
5241
5242                                          ;SET CDAL2 TO A 1 AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5243                                          ;SIGNAL TRSL1 L. THIS SIGNAL WILL ALLOW THE TRACE RAM TO BE READ ON A
5244                                          ;READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT2 H.
5245
5246  013434  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5247  013442  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
5248  013446  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5249  013450                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5250  013450  104455                          TRAP    C$ERDF
5251  013452  000001                          .WORD   1
5252  013454  000000                          .WORD   0
5253  013456  004604                          .WORD   ROEROR
5254  013460                                  CKLOOP
5255  013460  104406                          TRAP    C$CLP1
5256
5257                                          ;GO LOAD ADDRESS TO BE CHECKED INTO TRACE RAM ADDRESS REGISTER USING
5258                                          ;THE CONTENTS OF LOCATION "TRADRS" AS THE ADDRESS TO BE LOADED. ON
5259                                          ;EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER WILL HAVE THE SIGNAL
5260                                          ;PTER0 L ASSERTED.
5261
5262  013462  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5263
5264                                          ;SET THE SIGNAL PTER2 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5265
5266  013466  012737  000002  002376          MOV     #PTER2,R2LOAD           ;SETUP REGISTER 2 BITS TO BE LOADED
5267  013474  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5268  013500  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5269  013502                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5270  013502  104455                          TRAP    C$ERDF
5271  013504  000002                          .WORD   2
5272  013506  000000                          .WORD   0
5273  013510  004704                          .WORD   R2EROR
5274  013512                                  CKLOOP
5275  013512  104406                          TRAP    C$CLP1
5276
5277                                          ;READ THE DATA THAT WAS PREVIOUSLY WRITTEN IN THE FIRST SUB TEST AND
5278                                          ;CHECK THAT THE DATA IS EQUAL TO THE ADDRESS BEING TESTED.
5279
5280  013514  013737  006374  002414  3$:     MOV     TRADRS,R6LOAD           ;SETUP DATA PREVIOUSLY WRITTEN
5281  013522  017737  166730  002420          MOV     @REG6,R6READ            ;READ THE DATA FROM THE TRACE RAM
5282  013530  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK IF DATA IS EQUAL TO ITS ADDRESS
5283  013536  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5284  013540                                  ERRDF   4,TRAM31,TRAMER         ;TRAM DATA ERROR - TRDI 31:16 OR ADDRESS
5285  013540  104455                          TRAP    C$ERDF
5286  013542  000004                          .WORD   4
5287  013544  003032                          .WORD   TRAM31
5288  013546  004764                          .WORD   TRAMER
5289                                                                          ;FAILURE OR ADDRESS SHORT
5290  013550                          4$:     ENDSEG
5291  013550                          10000$:
```

```
                                        TRAP    C$ESEG

                                        ;THE FOLLOWING SECTION OF CODE WILL WRITE THE TRACE RAM DATA IN BUFFERS
                                        ;AND THE TRACE RAM WITH THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.

                                        BGNSEG
                                        TRAP    C$BSEG

                                        :CLEAR LOW BYTE OF CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
                                        .SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS

                                        CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
                                        JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
                                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
                                        ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
                                        TRAP    C$ERDF
                                        .WORD   1
                                        .WORD   0
                                        .WORD   ROEROR
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 31:16 WITH DATA
                                        ;EQUAL TO THE ONES COMPLEMENT OF THE ADDRESS. ON EXIT FROM ROUTINE
                                        ;"TRDIBF", THE POINTER REGISTER WILL HAVE THE SIGNAL PTER2 L ASSERTED.

013600  013737  006374  002414  5$:   MOV     TRADRS,R6LOAD           ;GET THE ADDRESS UNDER TEST
013606  005137  002414                COM     R6LOAD                  ;COMPLEMENT THE ADDRESS
013612  004537  006426                JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
013616  000006                        .WORD   PTER6                   ;SELECT TRDI BITS 31:16

                                        ;WRITE TRACE RAM LOCATION WITH DATA PATTERN EQUAL TO THE COMPLEMENT
                                        ;OF ITS ADDRESS.  THE DATA TO BE WRITTEN INTO THE TRACE RAM IS
                                        ;STORED IN THE TRACE RAM DATA IN BUFFERS TRDI 31:16.

013620  012777  000000  166530        MOV     #0,@REG6                ;WRITE RAM WITH TRAM DATA IN BUF

                                        ;SET CDAL2 TO A 1 AND CDAL 3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
                                        ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
                                        ;BITS TRDI 31:16 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
                                        ;THE SIGNAL RPT2 H.

013626  052737  000004  002370        BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
013634  004737  006102                JSR     PC,LDRDRO               ;GO LOAD,READ AND CHECK REGISTER 0
013640  001405                        BEQ     6$                      ;IF LOADEDOK THEN CONTINUE
013642                                ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
013642  104455                        TRAP    C$ERDF
013644  000001                        .WORD   1
013646  000000                        .WORD   0
013650  004604                        .WORD   ROEROR
013652                                CKLOOP
013652  104406                        TRAP    C$CLP1

                                        ;READ DATA FROM THE TRACE RAM TRDI 31:16 CHECKING THE DATA TO BE THE
                                        ;ONES COMPLEMENT OF THE ADDRESS UNDER TEST
```

```
5348  013654  017737  166476  002420  6$:     MOV     @REG6,R6READ            ;READ DATA FROM THE TRACE RAM
5349  013662  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5350  013670  001404                          BEQ     7$                      ;ID DATA EQUAL THEN CONTINUE
5351  013672                                  ERRDF   4,TRAM31,TRAMER         ;TRAM DATA ERROR - TRDI 31:16
5352  013672  104455                          TRAP    C$ERDF
5353  013674  000004                          .WORD   4
5354  013676  003032                          .WORD   TRAM31
5355  013700  004764                          .WORD   TRAMER
5356  013702                          7$:     ENDSEG
5357  013702                          10001$:
5358  013702  104405                          TRAP    C$ESEG
5359  013704  005237  006374                  INC     TRADRS                  ;UPDATE THE ADDRESS BY 1
5360  013710  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES BE N TESTED
5361  013716  001645                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5362  013720                                  ENDSUB
      013720                          L10101:
      013720  104403                          TRAP    C$ESUB
5365
5366                                          ;THE FOLLOWING SUB TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING
5367                                          ;ADDRESS OF THE TRACE RAM AND CHECK EACH LOCATION OF THE TRACE RAM TO
5368                                          ;CONTAIN THE ONES COMPLEMENT OF ITS ADDRESS. IN A FAILURE OCCURS, THE
5369                                          ;ERROR MAY BE AN ADDRESS SHORT IN WHICH WRITING A LOCATION IN THE
5370                                          ;PREVIOUS SUB TEST WROTE A LOCATION LOWER THEN THE ADDRESS BEING TESTED.
5371
5372  013722                                  BGNSUB
5373  013722                          T26.3:
5374  013722  104402                          TRAP    C$BSUB
5375  013724  005037  006374                  CLR     TRADRS                  ;CLEAR THE ADDRESS TO ADDRESS 0
5376
5377  013730                          1$:     BGNSEG
5378  013730  104404                          TRAP    C$BSEG
5379
5380                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO ASSERT
5381                                          ;THE SIGNAL  RSL1 L.  THE SIGNAL TRSL1 L WILL ALLOW THE DATA FROM THE
5382                                          ;TRACE RAM BITS TRDI 31:16 TO BE READ ON A READ COMMAND TO CONTROL
5383                                          ;REGISTER 6 VIA THE SIGNAL RPT2 H.
5384
5385  013732  112737  000004  002370          MOVB    #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5386  013740  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
5387  013744  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5388  013746                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5389  013746  104455                          TRAP    C$ERDF
5390  013750  000001                          .WORD   1
5391  013752  000000                          .WORD   0
5392  013754  004604                          .WORD   R0EROR
5393  013756                                  CKLOOP
5394  013756  104406                          TRAP    C$CLP1
5395
5396                                          ;LOAD,READ AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF
5397                                          ;LOCATION "TRADRS".  ON EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER
5398                                          ;WILL HAVE THE SIGNAL PTER0 L ASSERTED.
5399
5400  013760  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5401
5402                                          ;SET SIGNAL PTER2 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5403
```

```
5404  013764  012737  000002  002376          MOV     #PTER2,R2LOAD           ;SETUP BITS TO BE LOADED
5405  013772  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5406  013776  001405                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
5407  014000                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5408  014000  104455                          TRAP    C$ERDF
5409  014002  000002                          .WORD   2
5410  014004  000000                          .WORD   0
5411  014006  004704                          .WORD   R2EROR
5412  014010                                  CKLOOP
5413  014010  104406                          TRAP    C$CLP1
5414
5415                                          ;READ DATA PREVIOUSLY WRITTEN IN THE LAST SUB TEST CHECKING THE DATA
5416                                          ;TO BE THE COMPLEMENT OF THE ADDRESS.
5417
5418  014012  013737  006374  002414  3$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS BEING TESTED
5419  014020  005137  002414                  COM     R6LOAD                  ;MAKE IT THE ONES COMPLEMENT
5420  014024  017737  166326  002420          MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM
5421  014032  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5422  014040  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5423  014042                                  ERRDF   ^,TRAM31,TRAMER         ;TRAM DATA ERROR - TRDI 31:16
5424  014042  104455                          TRAP    C$ERDF
5425  014044  000004                          .WORD   4
5426  014046  003032                          .WORD   TRAM31
5427  014050  004764                          .WORD   TRAMER
5428  014052                          4$:     ENDSEG
5429  014052                          10000$:
5430  014052  104405                          TRAP    C$ESEG
5431  014054  005237  006374                  INC     TRADRS                  ;UPDATE THE ADDRESS BY ONE
5432  014060  032737  002000  006374          BIT     #BIT10,^RADRS           ;CHECK IF ALL ADDRESSES CHECKED
5433  014066  001720                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5434  014070                                  ENDSUB
5435  014070                          L10102:
5436  014070  104403                          TRAP    C$ESUB
5437  014072                                  ENDTST
5438  014072                          L10077:
5439  014072  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 27: TRAM ADDRESS/SHORT TEST - TRDI 47:32

                                ;++
                                ; THIS TEST WILL CHECK TRACE RAM TRDI 47 32 TO BE ADDRESSED CORRECTLY AND THAT
                                ; NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIP'S. THE TEST WILL
                                ; LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE
                                ; ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK THE ADDRESS TO CONTAIN ITS
                                ; ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO
                                ; THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN.  THE TEST WILL
                                ; REPEAT THIS SEQUENCE FOR ALL ADDRESSES IN THE TRACE RAM.  WHEN ALL ADDRESSES
                                ; HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET
                                ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK ALL OF THE RAM TO CONTAIN THE
                                ; ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
                                ;--

014074                                  BGNTST
014074                          T27::
014074  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        ;THE FOLLOWING SUB TEST WILL WRITE EACH LOCATION OF TRACE RAM TRDI 47:32
                                        ;WITH A DATA PATTERN EQUAL TO ITS ADDRESS.  AS EACH LOCATION IS WRITTEN,
                                        ;THE TEST WILL READ THE LOCATION AND CHECK THAT THE DATA EQUALS ITS
                                        ;ADDRESS.

014100                                  BGNSUB
014100                          T27.1:
014100  104402                          TRAP    C$BSUB
014102  005037  006374                  CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
014106                          1$:     BGNSEG
014106  104404                          TRAP    C$BSEG

                                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING A ZERO
                                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE
                                        ;RAM DATA IN BUFFERS.

014110  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
014114  004737  006102                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
014120  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
014122                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
014122  104455                          TRAP    C$ERDF
014124  000001                          .WORD   1
014126  000000                          .WORD   0
014130  004604                          .WORD   ROEROR
014132                                  CKLOOP
014132  104406                          TRAP    C$CLP1

                                        ;WRITE AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF LOCA-
                                        ;TION "TRADRS". THE POINTER REGISTER ON EXIT FROM ROUTINE TRADLD WILL
                                        ;HAVE THE SIGNAL PTER0 L ASSERTED.

014134  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                                        ;WRITE THE TRACE RAM ADDRESS INTO THE TRACE RAM DATA IN BUFFERS IN
                                        .BUFFER BITS TRDI 47:32. ON EXIT FROM ROUTINE "TRDIBF" THE POINTER
                                        ;REGISTER WILL HAVE THE SIGNAL PTER3 L ASSERTED.
```

```
5496
5497  014140  013737  006374  002414          MOV     TRADRS,R6LOAD           ;SETUP DATA TO EQUAL TRAM ADDRESS REG
5498  014146  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5499  014152  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
5500
5501                                          ;WRITE THE ADDRESS IN THE TRACE RAM DATA IN BUFFERS INTO TRACE RAM
5502                                          ;BITS TRDI 47:32
5503
5504  014154  012777  000000  166174          MOV     #0,@RFG6                ;WRTIE RAM WITH DATA IN BUFFERS
5505
5506                                          ;SET CDAL2 TO 1 AND CDAL3 TO 0 IN CONTROL REGISTER 0 TO SET THE SIGNAL
5507                                          ;TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW THE DATA IN THE TRACE RAM TO
5508                                          ;BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT3 H.
5509
5510  014162  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5511  014170  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
5512  014174  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5513  014176                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5514  014176  104455                          TRAP    C$ERDF
5515  014200  000001                          .WORD   1
5516  014202  000000                          .WORD   0
5517  014204  004604                          .WORD   R0E OR
5518  014206                                  CKLOOP
5519  014206  104406                          TRAP    C$CLP1
5520
5521                                          ;READ AND CHECK TRACE RAM DATA TRDI 47:32.  THE DATA SHOULD EQUAL THE
5522                                          ;ADDRESS BEING TESTED.
5523
5524  014210  013737  166142  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM TRDI 47:32
5525  014216  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED TO EQUAL DATA READ
5526  014224  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
5527  014226                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR - TRDI 47:32
5528  014226  104455                          TRAP    C$ERDF
5529  014230  000004                          .WORD   4
5530  014232  003067                          .WORD   TRAM47
5531  014234  004764                          .WORD   TRAMER
5532  014236                          4$:     ENDSEG
5533  014236                          10000$:
5534  014236  104405                          TRAP    C$ESEG
5535  014240  005237  006374                  INC     TRADRS                  ;UPDATE TRACE RAM ADDRESS BY 1
5536  014244  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF 1K YET
5537  014252  001715                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
5538  014254                                  ENDSUB
5539  014254                          L10104.
5540  014254  104403                          TRAP    C$ESUB
5541
5542                                          ;THE FOLLOWING SUB TEST WILL RESET THE POINTER TO THE BEGINNING
5543                                          ;ADDRESS OF THE TRACE RAM, CHECK THE LOCATION TO EQUAL ITS ADDRESS,
5544                                          ;WRITE,READ, AND CHECK THE LOCATION WITH THE ONES COMPLEMENT OF ITS
5545                                          ;ADDRESS. THIS SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE TRACE
5546                                          ;RAM FOR TRACE RAM TRDI 47:32. THIS TEST WILL CHECK THAT THE TRACE RAM
5547                                          ;CAN BE ADDRESSED CORRECTLY AND THAT WRITING A LOCATION DOES NOT WRITE
5548                                          ;A HIGHER LOCATION.
5549
5550  014256                                  BGNSUB
5551  014256                          T27.2:
```

```
5552  014256  104402                          TRAP    C$BSUB
5553  014260  005037  006374                  CLR     TRADRS                  ;RESET TRAM ADDRESS TO ADDRESS 0
5554
5555  014264                          1$:     BGNSEG
5556  014264  104404                          TRAP    C$BSEG
5557
5558                                          ;SET CDAL2 TO A 1 AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5559                                          ;SIGNAL TRSL1 L. THIS SIGNAL WILL ALLOW THE TRACE RAM TO BE READ ON A
5560                                          ;READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT3 H.
5561
5562  014266  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5563  014274  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
5564  014300  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5565  014302                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5566  014302  104455                          TRAP    C$ERDF
5567  014304  000001                          .WORD   1
5568  014306  000000                          .WORD   0
5569  014310  004604                          .WORD   R0EROR
5570  014312                                  CKLOOP
5571  014312  104406                          TRAP    C$CLP1
5572
5573                                          ;GO LOAD ADDRESS TO BE CHECKED INTO TRACE RAM ADDRESS REGISTER USING
5574                                          ;THE CONTENTS OF LOCATION "TRADRS" AS THE ADDRESS TO BE LOADED. ON
5575                                          ;EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER WILL HAVE THE SIGNAL
5576                                          ;PTER0 L ASSERTED.
5577
5578  014314  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5579
5580                                          ;SET THE SIGNAL PTER3 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5581
5582  014320  012737  000003  002376          MOV     #PTER3,R2LOAL           ;SETUP REGISTER 2 BITS TO BE LOADED
5583  014326  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5584  014332  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5585  014334                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5586  014334  104455                          TRAP    C$ERDF
5587  014336  000002                          .WORD   2
5588  014340  000000                          .WORD   0
5589  014342  004704                          .WORD   R2EROR
5590  014344                                  CKLOOP
5591  014344  104406                          TRAP    C$CLP1
5592
5593                                          ;READ THE DATA THAT WAS PREVIOUSLY WRITTEN IN THE FIRST SUB TEST AND
5594                                          ;CHECK THAT THE DATA IS EQUAL TO THE ADDRESS BEING TESTED.
5595
5596  014346  013737  006374  002414  3$:     MOV     TRADRS,R6LOAD           ;SETUP DATA PREVIOUSLY WRITTEN
5597  014354  017737  165776  002420          MOV     @REG6,R6READ            ;READ THE DATA FROM THE TRACE RAM
5598  014362  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK IF DATA IS EQUAL TO ITS ADDRESS
5599  014370  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5600  014372                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR - TRDI 47:32 OR ADDRESS
5601  014372  104455                          TRAP    C$ERDF
5602  014374  000004                          .WORD   4
5603  014376  003067                          .WORD   TRAM47
5604  014400  004764                          .WORD   TRAMER
5605                                                                          ;FAILURE OR ADDRESS SHORT
5606  014402                          4$:     ENDSEG
5607  014402                          10000$:
```

```
5608  014402  104405                          TRAP    C$ESEG
5609
5610                                          ;THE FOLLOWING SECTION OF CODE WILL WRITE THE TRACE RAM DATA IN BUFFERS
5611                                          ;AND THE TRACE RAM WITH THE ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
5612
5613  014404                                  BGNSEG
5614  014404  104404                          TRAP    C$BSEG
5615
5616                                          ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
5617                                          ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
5618
5619  014406  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
5620  014412  004737  006102                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
5621  014416  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
5622  014420                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5623  014420  104455                          TRAP    C$ERDF
5624  014422  000001                          .WORD   1
5625  014424  000000                          .WORD   0
5626  014426  004604                          .WORD   ROEROR
5627  014430                                  CKLOOP
5628  014430  104406                          TRAP    C$CLP1
5629
5630                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 47:32 WITH DATA
5631                                          ;EQUAL TO THE ONES COMPLEMENT OF THE ADDRESS. ON EXIT FROM ROUTINE
5632                                          ;"TRDIBF", THE POINTER REGISTER WILL HAVE THE SIGNAL PTER3 L ASSERTED.
5633
5634  014432  013737  006374  002414  5$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS UNDER TEST
5635  014440  005137  002414                  COM     R6LOAD                  ;COMPLEMENT THE ADDRESS
5636  014444  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5637  014450  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
5638
5639                                          ;WRITE TRACE RAM LOCATION WITH DATA PATTERN EQUAL TO THE COMPLEMENT
5640                                          ;OF ITS ADDRESS.  THE DATA TO BE WRITTEN INTO THE TRACE RAM IS
5641                                          ;STORED IN THE TRACE RAM DATA IN BUFFERS TRDI 47:32.
5642
5643  014452  012777  000000  165676          MOV     #0,@REG6                ;WRITE RAM WITH TRAM DATA IN BUF
5644
5645                                          ;SET CDAL2 TO A 1 AND CDAL 3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5646                                          ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
5647                                          ;BITS TRDI 47:32 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
5648                                          ;THE SIGNAL RPI3 H.
5649
5650  014460  052737  000004  002370          BIS     #CDAL2,POLOAD           ;SETUP BITS TO BE LOADED
5651  014466  004737  006102                  JSR     PC,LDRDRO               ;GO LOAD,READ AND CHECK REGISTER 0
5652  014472  001405                          BEQ     6$                      ;IF LOADEDOK THEN CONTINUE
5653  014474                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5654  014474  104455                          TRAP    C$ERDF
5655  014476  000001                          .WORD   1
5656  014500  000000                          .WORD   0
5657  014502  004604                          .WORD   ROEROR
5658  014504                                  CKLOOP
5659  014504  104406                          TRAP    C$CLP1
5660
5661                                          ;READ DATA FROM THE TRACE RAM TRDI 47:32 CHECKING THE DATA TO BE THE
5662                                          ;ONES COMPLEMENT OF THE ADDRESS UNDER TEST
5663
```

```
5664  014506  017737  165644  002420  6$:     MOV     @REG6,R6READ            ;READ DATA FROM THE TRACE RAM
5665  014514  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5666  014522  001404                          BEQ     7$                      ;ID DATA EQUAL THEN CONTINUE
5667  014524                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR - TRDI 47:32
5668  014524  104455                          TRAP    C$ERDF
5669  014526  000004                          .WORD   4
5670  014530  003067                          .WORD   TRAM47
5671  014532  004764                          .WORD   TRAMER
5672  014534                          7$:     ENDSEG
5673  014534                          10001$:
5674  014534  104405                          TRAP    C$ESEG
5675  014536  005237  006374                  INC     TRADRS                  ;UPDATE THE ADDRESS BY 1
5676  014542  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES BEEN TESTED
5677  014550  001645                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5678  014552                                  ENDSUB
5679  014552                          L10105:
5680  014552  104403                          TRAP    C$ESUB
5681
5682                                          ;THE FOLLOWING SUB TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING
5683                                          ;ADDRESS OF THE TRACE RAM AND CHECK EACH LOCATION OF THE TRACE RAM TO
5684                                          ;CONTAIN THE ONES COMPLEMENT OF ITS ADDRESS. IN A FAILURE OCCURS, THE
5685                                          ;ERROR MAY BE AN ADDRESS SHORT IN WHICH WRITING A LOCATION IN THE
5686                                          ;PREVIOUS SUB TEST WROTE A LOCATION LOWER THEN THE ADDRESS BEING TESTED.
5687
5688  014554                                  BGNSUB
5689  014554                          T27.3:
5690  014554  104402                          TRAP    C$BSUB
5691  014556  005037  006374                  CLR     TRADRS                  ;CLEAR THE ADDRESS TO ADDRESS 0
5692
5693  014562                          1$:     BGNSEG
5694  014562  104404                          TRAP    C$BSEG
5695
5696                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO ASSERT
5697                                          ;THE SIGNAL TRSL1 L.  THE SIGNAL TRSL1 L WILL ALLOW THE DATA FROM THE
5698                                          ;TRACE RAM BITS TRDI 47:32 TO BE READ ON A READ COMMAND TO CONTROL
5699                                          ;REGISTER 6 VIA THE SIGNAL RPT3 H.
5700
5701  014564  112737  000004  002370          MOVB    #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
5702  014572  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
5703  014576  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
5704  014600                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
5705  014600  104455                          TRAP    C$ERDF
5706  014602  000001                          .WORD   1
5707  014604  000000                          .WORD   0
5708  014606  004604                          .WORD   ROEROR
5709  014610                                  CKLOOP
5710  014610  104406                          TRAP    C$CLP1
5711
5712                                          ;LOAD,READ AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF
5713                                          ;LOCATION "TRADRS".  ON EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER
5714                                          ;WILL HAVE THE SIGNAL PTER0 L ASSERTED.
5715
5716  014612  004737  006310          2$:     JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5717
5718                                          ;SET SIGNAL PTER3 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5719
```

```
5720  014616  012737  000003  002376          MOV     #PTER3,R2LOAD           ;SETUP BITS TO BE LOADED
5721  014624  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
5722  014630  001405                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
5723  014632                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
5724  014632  104455                          TRAP    C$ERDF
5725  014634  000002                          .WORD   2
5726  014636  000000                          .WORD   0
5727  014640  004704                          .WORD   R2EROR
5728  014642                                  CKLOOP
5729  014642  104406                          TRAP    C$CLP1
5730
5731                                          ;READ DATA PREVIOUSLY WRITTEN IN THE LAST SUB TEST CHECKING THE DATA
5732                                          ;TO BE THE COMPLEMENT OF THE ADDRESS.
5733
5734  014644  013737  006374  002414  3$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS BEING TESTED
5735  014652  005137  002414                  COM     R6LOAD                  ;MAKE IT THE ONES COMPLEMENT
5736  014656  017737  165474  002420          MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM
5737  014664  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
5738  014672  001404                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
5739  014674                                  ERRDF   4,TRAM47,TRAMER         ;TRAM DATA ERROR - TRDI 47-32
5740  014674  104455                          TRAP    C$ERDF
5741  014676  000004                          .WORD   4
5742  014700  003067                          .WORD   TRAM47
5743  014702  004764                          .WORD   TRAMER
5744  014704                          4$:     ENDSEG
5745  014704                          10000$:
5746  014704  104405                          TRAP    C$ESEG
5747  014706  005237  006374                  INC     TRADRS                  ;UPDATE THE ADDRESS BY ONE
5748  014712  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES CHECKED
5749  014720  001720                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
5750  014722                                  ENDSUB
5751  014722                          L10106:
5752  014722  104403                          TRAP    C$ESUB
5753  014724                                  ENDTST
5754  014724                          L10103:
5755  014724  104401                          TRAP    C$ETST
```

```
                        .SBTTL  TEST 28: TRAM ADDRESS/SHORT TEST - TRDI 55:48

                        ;++
                        ; THIS TEST WILL CHECK TRACE RAM TRDI 55:48 TO BE ADDRESSED CORRECTLY AND THAT
                        ; NO ADDRESSES ARE SHORTED TOGETHER INTERNAL TO THE RAM CHIP'S. THE TEST WILL
                        ; LOAD AND CHECK EACH TRACE RAM ADDRESS WITH DATA EQUAL TO ITS ADDRESS. ONCE
                        ; ALL OF THE 1K ADDRESSES HAVE BEEN WRITTEN AND CHECKED, THE TEST WILL RESET
                        ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK THE ADDRESS TO CONTAIN ITS
                        ; ADDRESS. THE TEST WILL THEN WRITE THE 1'S COMPLEMENT OF ITS ADDRESS INTO
                        ; THE LOCATION AND CHECK THAT THE 1'S COMPLEMENT WAS WRITTEN.  THE TEST WILL
                        ; REPEAT THIS SEQUENCE FOR ALL ADDRESSES IN THE TRACE RAM.  WHEN ALL ADDRESSES
                        ; HAVE BEEN WRITTEN WITH THE ONES COMPLEMENT OF ITS ADDRESS, THE TEST WILL RESET
                        ; THE POINTER TO THE BEGINNING ADDRESS AND CHECK ALL OF THE RAM TO CONTAIN THE
                        ; ONES COMPLEMENT OF THE ADDRESS BEING TESTED.
                        ;--

014726                          BGNTST
014726                   28::
014726  004737  005474          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                        ;THE FOLLOWING SUB TEST WILL WRITE EACH LOCATION OF TRACE RAM TRDI 55:48
                        ;WITH A DATA PATTERN EQUAL TO ITS ADDRESS.  AS EACH LOCATION IS WRITTEN,
                        ;THE TEST WILL READ THE LOCATION AND CHECK THAT THE DATA EQUALS ITS
                        ;ADDRESS.

                                BGNSUB
014732                  ;28.1:
014732  104402                  TRAP    C$BSUB
014734  005037  006374          CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
014740                  1$:     BGNSEG
014740  104404                  TRAP    C$BSEG

                        ;CLEAR LOWER BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING A ZERO
                        ;WILL SET THE SIGNAL TRSLO L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE
                        ;RAM DATA IN BUFFERS.

014742  105037  002370          CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
014746  004737  006102          JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
014752  001405                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
014754                          ERRDF   1,,ROERUR               ;REGISTER 0 NOT EQUAL EXPECTED
014754  104455                  TRAP    C$ERDF
014756  000001                  .WORD   1
014760  000000                  .WORD   0
014762  004604                  .WORD   ROERUR
014764                          CKLOOP
014764  104406                  TRAP    C$CLP1

                        ;WRITE AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF LOCA-
                        ;TION "TRADRS". THE POINTER REGISTER ON EXIT FROM ROUTINE TRADLD WILL
                        ;HAVE THE SIGNAL PTER0 L ASSERTED.

014766  004737  006310   2$:    JSR     PC,TRADLD               ;GO LOAD,READ AND CHECK TRAM ADDRESS REG

                        ;WRITE THE TRACE RAM ADDRESS INTO THE TRACE RAM DATA IN BUFFERS IN
                        ;BUFFER BITS TRDI 59:48. ON EXIT FROM ROUTINE "TRDIBF" THE POINTER
                        ;REGISTER WILL HAVE THE SIGNAL PTER4 L ASSERTED.
```

```
5812
5813  014772  013737  006374  002414          MOV     TRADRS,R6LOAD           ;SETUP DATA TO EQUAL TRAM ADDRESS REG
5814  015000  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
5815  015004  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 55:48
5816
5817                                          ;WRITE THE ADDRESS IN THE TRACE RAM DATA IN BUFFERS INTO TRACE RAM
5818                                          ;BITS TRDI 55:48
5819
5820  015006  012777  000000  165342          MOV     #0,@RECo                ;WRTIE RAM WITH DATA IN BUFFERS
5821
5822                                          ;SET CDAL2 TO 1 AND CDAL3 TO 0 IN CONTROL REGISTER 0 TO SET THE SIGNAL
5823                                          ;TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW THE DATA IN THE TRACE RAM TO
5824                                          ;BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA THE SIGNAL RPT4 H.
5825
5826  015014  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
5827  015022  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
5828  015026  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
5829  015030                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
5830  015030  104455                          TRAP    C$ERDF
5831  015032  000001                          .WORD   1
5832  015034  000000                          .WORD   0
5833  015036  004604                          .WORD   R0ERR
5834  015040                                  CKLOOP
5835  015040  104406                          TRAP    C$CLP1
5836
5837                                          ;READ AND CHECK TRACE RAM DATA TRDI 55:48.  THE DATA SHOULD EQUAL THE
5838                                          ;ADDRESS BEING TESTED.
5839
5840  015042  017737  165310  002420  3$:     MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM TRDI 55:48
5841  015050  042737  177400  002420          BIC     #177400,R6READ          ;CLEAR BITS NOT AVAILABLE IN TRACE RAM
5842  015056  042737  177400  002414          BIC     #177400,R6LOAD          ;ONLY 8 BITS WERE LOADED, 0 TOP 4 BITS
5843  015064  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED TO EQUAL DATA READ
5844  015072  001404                          BEQ     4$                      ;IF DATA THE SAME THEN CONTINUE
5845  015074                                  ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR - TRDI 55:48
5846  015074  104455                          TRAP    C$ERDF
5847  015076  000004                          .WORD   4
5848  015100  003124                          .WORD   TRAM55
5849  015102  004764                          .WORD   TRAMER
5850  015104                          4$:     ENDSEG
5851  015104                          1C00C$:
5852  015104  104405                          TRAP    C$ESEG
5853  015106  005237  0063'4                 INC     TRADRS                  ;UPDATE TRACE RAM ADDRESS BY 1
5854  015112  032737  0020 )0  006374          BIT     #BIT10,TRADRS           ;CHECK IF 1K YET
5855  015120  001707                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
5856  015122                                  ENDSUB
5857  015122                          C10110:
5858  015122  104403                          TRAP    C$ESUB
5859
5860                                          ;THE FOLLOWING SUB TEST WILL RESET THE POINTER TO THE BEGINNING
5861                                          ;ADDRESS OF THE TRACE RAM, CHECK THE LOCATION TO EQUAL ITS ADDRESS,
5862                                          ;WRITE,READ, AND CHECK THE LOCATION WITH THE ONES COMPLEMENT OF ITS
5863                                          ;ADDRESS. THIS SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE TRACE
5864                                          ;RAM FOR TRACE RAM TRDI 55:48. THIS TEST WILL CHECK THAT THE TRACE RAM
5865                                          ;CAN BE ADDRESSED CORRECTLY AND THAT WRITING A LOCATION DOES NOT WRITE
5866                                          ;A HIGHER LOCATION.
5867
```

```
5868  015124                                  T28.2:  BGNSUB
5869  015124
5870  015124  104402                                  TRAP    C$BSUB
5871  015126  005037  006374                          CLR     TRADRS          ;RESET TRAM ADDRESS TO ADDRESS 0
5872
5873  015132                                  1$:     BGNSEG
5874  015132  104404                                  TRAP    C$BSEG
5875
5876                                                  ;SET CDAL2 TO A 1 AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
5877                                                  ;SIGNAL TRSL1 L. THIS SIGNAL WILL ALLOW THE T  E RAM TO BE READ ON A
5878                                                  ;READ COMMAND TO CONTROL REGISTER 6 VIA THE S.GNAL RPT4 H.
5879
5880  015134  112737  000004  [illegible]            MOVB    #CDAL2,ROLOAD   ;SETUP BITS TO BE LOADED
5881  015142  004737  006[illegible]                 JSR     PC,LDRDR0       ;GO LOAD, READ AND CHECK REGISTER 0
5882  015146  001405                                  BEQ     2$              ;IF LOADED OK THEN CONTINUE
5883  015150                                          ERRDF   1,,ROEROR       ;REGISTER 0 NOT EQUAL EXPECTED
5884  015150  104455                                  TRAP    C$ERDF
5885  015152  000001                                  .WORD   1
5886  015154  000000                                  .WORD   0
5887  015156  004604                                  .WORD   ROEROR
5888  015160                                          CKLOOP
5889  015160  104406                                  TRAP    C$CLP1
5890
5891                                                  ;GO LOAD ADDRESS TO BE CHECKED INTO TRACE RAM ADDRESS REGISTER USING
5892                                                  ;THE CONTENTS OF LOCATION "TRADRS" AS THE ADDRESS TO BE LOADED. ON
5893                                                  ;EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER WILL HAVE THE SIGNAL
5894                                                  ;PTER0 L ASSERTED.
5895
5896  015162  004737  006310                2$:     JSR     PC,TRADLD       ;GO LOAD,READ + CHECK TRAM ADDRESS REG
5897
5898                                                  ;SET THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2
5899
5900  015166  012737  000004  002376                  MOV     #PTER4,R2LOAD   ;SETUP REGISTER 2 BITS TO BE LOADED
5901  015174  004737  006134                          JSR     PC,LDRDR2       ;GO LOAD, READ AND CHECK REGISTER 2
5902  015200  001405                                  BEQ     3$              ;IF LOADED OK THEN CONTINUE
5903  015202                                          ERRDF   2,,R2EROR       ;REGISTER 2 NOT EQUAL EXPECTED
5904  015202  104455                                  TRAP    C$ERDF
5905  015204  000002                                  .WORD   2
5906  015206  000000                                  .WORD   0
5907  015210  004704                                  .WORD   R2EROR
5908  015212                                          CKLOOP
5909  015212  104406                                  TRAP    C$CLP1
5910
5911                                                  ;READ THE DATA THAT WAS PREVIOUSLY WRITTEN IN THE FIRST SUB TEST AND
5912                                                  ;CHECK THAT THE DATA IS EQUAL TO THE ADDRESS BEING TESTED.
5913
5914  015214  013737  006374  002414  3$:     MOV     TRADRS,R6LOAD   ;SETUP DATA PREVIOUSLY WRITTEN
5915  015222  017737  165130  002[illegible]          MOV     @REG6,R6READ    ;READ THE DATA FROM THE TRACE RAM
5916  015230  042737  177400  002414                  BIC     #177400,R6LOAD  ;ONLY 8 BITS OF ADDRESS WAS LOADED
5917  015236  042737  177400  002420                  BIC     #177400,R6READ  ;CLEAR BITS THAT ARE NOT VALID
5918  015244  023737  002414  002420                  CMP     R6LOAD,R6READ   ;CHECK IF DATA IS EQUAL TO ITS ADDRESS
5919  015252  001404                                  BEQ     4$              ;IF DATA OK THEN CONTINUE
5920  015254                                          ERRDF   4,TRAM55,TRAMER ;TRAM DATA ERROR - TRDI 55:48 OR ADDRESS
5921  015254  104455                                  TRAP    C$ERDF
5922  015256  000004                                  .WORD   4
5923  015260  00[illegible]                           .WORD   TRAM55
```

```
                                        .WORD   TRAMER
                                                                ;FAILURE OR ADDRESS SHORT
                                4$:     ENDSEG
                                10000$:
                                        TRAP    C$ESEG

                                ;THE FOLLOWING SECTION OF CODE WILL WRITE THE TRACE RAM DATA IN BUFFERS
                                ;AND THE TRACE RAM WITH THE ONES COMPLEMENT OF    c ADDRESS BEING TESTED.

                                        BGNSEG
                                        TRAP    C$BSEG

                                ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
                                ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS

                                        CLRB    ROLOAD                  ;SETUP TO CLEAR LOWER BYTE
                                        JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
                                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
                                        ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
                                        TRAP    C$ERDF
                                        .WORD   1
                                        .WORD   0
                                        .WORD   ROEROR
                                        CKLOOP
                                        TRAP    C$CLP1

                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 59:48 WITH DATA
                                ;EQUAL TO THE ONES COMPLEMENT OF THE ADDRESS. ON EXIT FROM ROUTINE
                                ;"TRDIBF", THE POINTER REGISTER WILL HAVE THE SIGNAL PTER4 L ASSERTED.

                        5$:     MOV     TRADRS,R6LOAD           ;GET THE ADDRESS UNDER TEST
                                COM     R6LOAD                  ;COMPLEMENT THE ADDRESS
                                BIC     #170000,R6LOAD          ;CLEAR TOP 4 BITS WHICH NOT AVAILABLE
                                JSR     R5,TRDIBF               ;LOAD,READ + CHECK TRAM DATA IN BUF
                                .WORD   PTER8                   ;SELECT TRDI BITS 55:48

                                ;WRITE TRACE RAM LOCATION WITH DATA PATTERN EQUAL TO THE COMPLEMENT
                                ;OF ITS ADDRESS.  THE DATA TO BE WRITTEN INTO THE TRACE RAM IS
                                ;STORED IN THE TRACE RAM DATA IN BUFFERS TRDI 55:48.

                                MOV     #0,@REG6                ;WRITE RAM WITH TRAM DATA IN BUF

                                ;SET CDAL2 TO A 1 AND CDAL 3 TO A 0 IN CONTROL REGISTER 0 TO SET THE
                                ;SIGNAL TRSL1 L. THE SIGNAL TRSL1 L WILL ALLOW DATA FROM THE TRACE RAM
                                ;BITS TRDI 55:48 TO BE READ ON A READ COMMAND TO CONTROL REGISTER 6 VIA
                                ;THE SIGNAL RPT4 H.

                                BIS     #CDAL2,ROLOAD           ;SETUP BITS TO BE LOADED
                                JSR     PC,LDRDRO               ;GO LOAD,READ AND CHECK REGISTER 0
                                BEQ     6$                      ;IF LOADEDOK THEN CONTINUE
                                ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
                                TRAP    C$ERDF
                                .WORD   1
                                .WORD   0
                                .WORD   ROEROR
                                CKLOOP
```

```
 5980  015374  104406                          TRAP    C$CLP1
 5981
 5982                                          ;READ DATA FROM THE TRACE RAM TRDI 55:48 CHECKING THE DATA TO BE THE
 5983                                          ;ONES COMPLEMENT OF THE ADDRESS UNDER TEST
 5984
 5985  015376  017737  164754  002420  6$:     MOV     @REG6,R6READ            ;READ DATA FROM THE TRACE RAM
 5986  015404  042737  177400  002420          BIC     #177400,R6READ          ;CLEAR BITS NOT AVIALABLE
 5987  015412  042737  177400  002414          BIC     #177400,R6LOAD          ;CLEAR BITS THAT WERE NOT LOADED
 5988  015420  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
 5989  015426  001404                          BEQ     7$                      ;ID DATA EQUAL THEN CONTINUE
 5990  015430                                  ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR - TRDI 55:48
 5991  015430  104455                          TRAP    C$ERDF
 5992  015432  000004                          .WORD   4
 5993  015434  003124                          .WORD   TRAM55
 5994  015436  004764                          .WORD   TRAMER
 5995  015440                          7$:     ENDSEG
 5996  015440                          10001$:
 5997  015440  104405                          TRAP    C$ESEG
 5998  015442  005237  006374                  INC     TRADRS                  ;UPDATE THE ADDRESS BY 1
 5999  015446  032737  002000  006374          BIT     #BIT10,TRADRS           ;CHECK IF ALL 1K ADDRESSES BEEN TESTED
 6000  015454  001676                          BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
 6001  015456                                  ENDSUB
 6002  015456                          L10111:
 6003  015456  104403                          TRAP    .$ESUB
 6004
 6005                                          ;THE FOLLOWING SUB TEST WILL RESET THE ADDRESS POINTER TO THE BEGINNING
 6006                                          ;ADDRESS OF THE TRACE RAM AND CHECK EACH LOCATION OF THE TRACE RAM TO
 6007                                          ;CONTAIN THE ONES COMPLEMENT OF ITS ADDRESS. IN A FAILURE OCCURS, THE
 6008                                          ;ERROR MAY BE AN ADDRESS SHORT IN WHICH WRITING A LOCATION IN THE
 6009                                          ;PREVIOUS SUB TEST WROTE A LOCATION LOWER THEN THE ADDRESS BEING TESTED.
 6010
 6011  015460                                  BGNSUB
 6012  015460                          T28.3:
 6013  015460  104402                          TRAP    C$BSUB
 6014  015462  005037  006374                  CLR     TRADRS                  ;CLEAR THE ADDRESS TO ADDRESS 0
 6015
 6016  015466                          1$:     BGNSEG
 6017  015466  104404                          TRAP    C$BSEG
 6018
 6019                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO ASSERT
 6020                                          ;THE SIGNAL TRSL1 L.  THE SIGNAL TRSL1 L WILL ALLOW THE DATA FROM THE
 6021                                          ;TRACE RAM BITS TRDI 55:48 TO BE READ ON A READ COMMAND TO CONTROL
 6022                                          ;REGISTER 6 VIA THE SIGNAL RPT4 H.
 6023
 6024  015470  112737  000004  002370          MOVB    #CDAL2,R0LOAD           ;SETUP BITS TO BE LOADED
 6025  015476  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REGISTER 0
 6026  015502  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
 6027  015504                                  ERRDF   1,,R0ERR                ;REGISTER 0 NOT EQUAL EXPECTED
 6028  015504  104455                          TRAP    C$ERDF
 6029  015506  000001                          .WORD   1
 6030  015510  000000                          .WORD   0
 6031  015512  004604                          .WORD   R0ERR
 6032  015514                                  CKLOOP
 6033  015514  104406                          TRAP    C$CLP1
 6034
 6035                                          ;LOAD,READ AND CHECK TRACE RAM ADDRESS REGISTER WITH THE CONTENTS OF
```

```
                                                ;LOCATION "TRADRS".  ON EXIT FROM ROUTINE "TRADLD" THE POINTER REGISTER
                                                ;WILL HAVE THE SIGNAL PTER0 L ASSERTED.

015516  004737  006310          2$:   JSR     PC,TRADLD               ;GO LOAD,READ + CHECK TRAM ADDRESS REG

                                                ;SET SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2

015522  012737  000004  002376        MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
015530  004737  006134                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
015534  001405                        BEQ     3$                      ;IF DATA OK THEN CONTINUE
015536                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
015536  104455                        TRAP    C$ERDF
015540  000002                        .WORD   2
015542  000000                        .WORD   0
015544  004704                        .WORD   R2EROR
015546                                CKLOOP
015546  104406                        TRAP    C$CLP1

                                                ;READ DATA PREVIOUSLY WRITTEN IN THE LAST SUB TEST CHECKING THE DATA
                                                ;TO BE THE COMPLEMENT OF THE ADDRESS.

015550  013737  006374  002414  3$:   MOV     TRADRS,R6LOAD           ;GET THE ADDRESS BEING TESTED
015556  005137  002414                COM     R6LOAD                  ;MAKE IT THE ONES COMPLEMENT
015562  042737  177400  002414        BIC     #177400,R6LOAD          ;CLEAR BITS THAT WERE NOT LOADED
015570  017737  164562  002420        MOV     @REG6,R6READ            ;READ DATA FROM TRACE RAM
015576  042737  177400  002420        BIC     #177400,R6READ          ;CLEAR BITS THAT ARE NOT AVAILABLE
015604  023737  002414  002420        CMP     R6LOAD,R6READ           ;CHECK DATA LOADED WITH DATA READ
015612  001404                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
015614                                ERRDF   4,TRAM55,TRAMER         ;TRAM DATA ERROR - TRDI 55:48
015614  104455                        TRAP    C$ERDF
015616  000004                        .WORD   4
015620  003124                        .WORD   TRAM55
015622  004764                        .WORD   TRAMER
015624                          4$:   ENDSEG
015624                          10000$:
015624  104405                        TRAP    C$ESEG
015626  005237  006374                INC     TRADRS                  ;UPDATE THE ADDRESS BY ONE
015632  032737  002000  006374        BIT     #BIT10,TRADRS           ;CHECK IF ALL ADDRESSES CHECKED
015640  001712                        BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
015642                                ENDSUB
015642                          L10112:
015642  104403                        TRAP    C$ESUB
015644                                ENDTST
015644                          110107:
015644  104401                        TRAP    C$ETST
6081
```

```
                                .SBTTL  TEST 29: TRAM ADDRESS REG COUNT UP TEST - TRAD 10:0

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN COUNT UP
                                ; ONE WHEN THE SIGNAL CTR L IS PULSED.  THE TRACE RAM ADDRESS REGISTER WILL BE
                                ; COUNTED UP BY ONE FROM THE ADDRESS 0 TO ADDRESS 3777 AND THEN BACK TO 0.  IN
                                ; ORDER TO PULSE THE SIGNAL CTR L, THE PROGRAM WILL SET AND CLEAR THE SIGNAL
                                ; CDAL6 IN CONTROL REGISTER 0 WHICH WILL CAUSE THE SIGNALS TRANST H AND TRST L
                                ; TO PULSE.  THIS WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE
                                ; THE SIGNAL ORST L TO PULSE.  WITH THE TRACING FLIP-FLOP HELD IN THE PRESET
                                ; STATE BY THE SIGNAL PDAL6 BEING A ONE AND THE SIGNALS TRANST H AND TRST L
                                ; BEING PULSED, A PULSE WILL OCCUR ON THE SIGNAL CTR L.
                                ;--

                                        BGNTST
                                T29::

015646  004737  005474                  JSR     PC,.WAITED              ;SELECT AND INITIALIZE STATE ANALYZER

                                        BGNSEG
015652  104404                          TRAP    C$BSEG

                                ;SETUP CONTROL REGISTER 2 SO THAT THE SIGNAL PTERO L WILL BE ASSERTED
                                ;IN THE POINTER REGISTER.  WHEN THE SIGNAL PTERO L IS ASSERTED AND A
                                ;READ COMMAND IS ISSUED TO CONTROL REGISTER 6, A PULSE WILL OCCUR ON
                                ;THE SIGNAL RPTO H. THE SIGNAL RPTO H WILL CAUSE THE TRACE RAM ADDRESS
                                ;REGISTER TO BE READ.  PDAL6 BEING A ONE IN CONTROL REGISTER 2 WILL
                                ;PRESET THE OUTPUT OF THE TRACING FLIP-FLOP TO A HIGH CONDITION.

015654  012737  000100  002376          MOV     #PDAL6!PTERO,R2LOAD     ;SETUP BITS TO LOAD IN CONTROL REG 2
015662  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECH REG 2
015666  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
015670                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL TO 0
015670  104455                          TRAP    C$ERDF
015672  000002                          .WORD   2
015674  000000                          .WORD   0
015676  004704                          .WORD   R2EROR
015700                                  CKLOOP
015700  104406                          TRAP    C$CLP1

                                ;SET AND CLEAR THE SIGNAL CDAL0 IN CONTROL REGISTER 0. THIS IS DONE TO
                                ;CLEAR THE TRACE RAM ADDRESS REGISTER TO ADDRESS 0.

                                ;SET THE SIGNAL CDAL0 TO A ONE

015702  112737  000001  002370  1$:     MOVB    #CDAL0,R0LOAD           ;SETUP BIT TO BE LOADED
015710  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD,READ AND CHECK REG 0
015714  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
015716                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
015716  104455                          TRAP    C$ERDF
015720  000001                          .WORD   1
015722  000000                          .WORD   0
015724  004604                          .WORD   R0EROR
015726                                  CKLOOP
015726  104406                          TRAP    C$CLP1
```

```
                                        ;CLEAR THE SIGNAL CDALO IN CONTROL REGISTER 0
                                        
015730  105037  006370        2$:     CLRB    R0LOAD                  ;SETUP TO CLEAR CDALO
015734  004737  006102                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
015740  001405                        BEQ     3$                      ;IF LOADED OK THEN CONTINUE
015742                                ERRDF   1,,R0ERR                ;REGISTER 0 NOT EQUAL EXPECTED
015742  104455                        TRAP    C$ERDF
015744  000001                        .WORD   1
015746  000000                        .WORD   0
015750  004604                        .WORD   R0ERR
015752                                CKLOOP
015752  104406                        TRAP    C$CLP1
                                        
                                        ;READ TRACE RAM ADDRESS REGISTER CHECKING THAT THE SIGNAL CDALO CLEARED
                                        ;ALL BITS IN THE TRACE RAM ADDRESS REGISTER.
                                        
015754  005037  002414        3$:     CLR     R6LOAD                  ;SETUP EXPECTED CONTENTS
015760  012737  174000  002416        MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
015766  004737  006256                JSR     PC,READR6               ;GO READ AND CHECK TRACE RAM ADDRESS REG
015772  001405                        BEQ     4$                      ;IF TRAM ADDRESS REG EQUALS 0 THEN CONT
015774                                ERRDF   4,TRADER,R026ER         ;CDALO FAILED TO 0 TRAM ADDRESS REGISTER
015774  104455                        TRAP    C$ERDF
015776  000004                        .WORD   4
016000  002462                        .WORD   TRADER
016002  004734                        .WORD   R026ER
016004                                CKLOOP
016004  104406                        TRAP    C$CLP1
                                        
                                        ;THE FOLLOWING SECTION OF CODE WILL BE EXECUTED FOR EACH ADDRESS OF THE
                                        ;TRACE RAM ADDRESS REGISTER.  THE ADDRESS REGISTER WILL BE INCREMENTED
                                        ;BY ONE VIA THE SIGNAL "CTR L" EACH TIME THE SIGNAL CDAL6 IS SET AND
                                        ;CLEARED.
                                        
                                        ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0. SETTING AND
                                        ;CLEARING THE SIGNAL CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L
                                        ;TO PULSE.  THIS WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL
                                        ;CAUSE THE SIGNAL ORST L TO PULSE.  WITH THE TRACING FLIP-FLOP HELD IN
                                        ;THE PRESET STATE BY THE SIGNAL CDAL6 BEING A ONE AND THE SIGNALS
                                        ;TRANST H AND TRST L BEING PULSED, A PULSE WILL OCCUR ON THE SIGNAL
                                        ;CTR L.  THE SIGNAL CTR L WILL CAUSE THE TRACE RAM ADDRESS REGISTER TO
                                        ;COUNT UP BY ONE ADDRESS.
                                        
016006  004737  006640        4$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
                                        
                                        ;CHECK THAT THE SIGNAL CTR L INCREMENTED THE TRACE RAM ADDRESS REGISTER
                                        ;BY ONE.
                                        
016012  005237  002414        6$:     INC     R6LOAD                  ;UPDATE THE EXPECTED ADDRESS BY ONE
016016  042737  174000  002414        BIC     #174000,R6LOAD          ;ALLOW WRAP AROUND TO ZERO
016024  004737  006256                JSR     PC,READR6               ;READ AND CHECK TRACE RAM ADDRESS REG
016030  001405                        BEQ     7$                      ;IF ADDRESS INCREMENTED THEN CONTINUE
016032                                ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO INCREMENT TRAM ADDRESS REG
016032  104455                        TRAP    C$ERDF
016034  000004                        .WORD   4
016036  002462                        .WORD   TRADER
016040  004734                        .WORD   R026ER
```

```
 6194  016042                                  CKLOOP
 6195  016042  104406                          TRAP    C$CLP1
 6196  016044  005737  002414          7$:     TST     R6LOAD          ;CHECK IF BACK TO ADDRESS 0
 6197  016050  001356                          BNE     4$              ;IF NOT THEN INCREMENT ADDRESS AGAIN
 6198  016052                                  ENDSEG
 6199  016052                          10000$:
 6200  016052  104405                          TRAP    C$ESEG
 6201  016054                                  ENDTST
 6202  016054                          L10113:
 6203  016054  104401                          TRAP    C$ETST
 6204
```

```
                                .SBTTL  TEST 30: SET/CLEAR TRACING F/F TEST VIA PDAL6 + CDAL0

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACING F..P-FLOP CAN BE SET BY PDAL6 IN
                                ; CONTROL REGISTER 2 AND  LEARED BY CDAL0 IN CONTROL REGISTER 0.
                                ;
                                ; TO CHECK THAT THE  RACING FLIP-FLOP CAN BE SET, THE PROGRAM WILL SET PDAL6
                                ; TO A ONE IN .ONTR  REGISTER 2 WHICH WILL CAUSE THE OUTPUT OF THE TRACING
                                ; FLIP-FLOP TO BE SE  HIGH. THE TEST WILL THEN CLEAR PDAL6 IN CONTROL REGISTER
                                ; 2.  THE TRACE RAM ADDRESS REGISTER WILL THEN BE LOADED AND CHECKED WITH THE
                                ; ADDRESS 1775. THE TEST WILL THEN SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL
                                ; REGISTER 0.  SETTING AND CLEARING CDAL6 IN CONTROL REGISTER 0 WILL CAUSE THE
                                ; SIGNALS TRANST H AND TRST L TO PULSE.  THIS WILL THEN CAUSE THE SIGNAL
                                ; ANST L TO PULSE WHICH WILL THEN CAUSE THE SIGNAL ORST L TO PULSE.  WITH THE
                                ; TRACING FLIP-FLOP PRESET HIGH AND THE SIGNALS TRANST H AND TRST L BEING PULSED
                                ; A PULSE WILL OCCUR ON THE SIGNAL CTR L.  THE SIGNAL CTR L WILL CAUSE THE
                                ; TRACE RAM ADDRESS REGISTER TO INCREMENT BY ONE.  THE TEST WILL CHECK THE TRACE
                                ; RAM ADDRESS REGISTER TO BE INCREMENTED BY ONE TO ADDRESS 1776.  THE TEST WILL
                                ; THEN SET AND CLEAR THE SIGNAL CDAL0 IN CONTROL REGISTER 0.  THE SIGNAL CDAL0
                                ; WILL CLEAR THE TRACE RAM ADDRESS REGISTER AND THE TRACING FLIP-FLOP.  TO
                                ; CHECK THAT THE TRACE RAM ADDRESS REGISTER WAS CLEARED, THE TEST WILL READ
                                ; THE TRACE RAM ADDRESS REGISTER CHECKING IT TO BE 0.  TO CHECK THAT THE
                                ; TRACING FLIP-FLOP CLEARED, THE TEST WILL AGAIN SET AND CLEAR THE SIGNAL
                                ; CDAL6 IN CONTROL REGISTER 0.  WHEN THE TRACING FLIP-FLOP IS CLEARED AND THE
                                ; SIGNALS TRANST H AND TRST L ARE PULSED  A PULSE SHOULD NOT OCCUR ON THE SIGNAL
                                ; CTR L, THUS, THE TRACE RAM ADDRESS REGISTER SHOULD NOT BE INCREMENTED.  THE
                                ; TEST WILL READ THE TRACE RAM ADDRESS REGISTER CHECKING IT TO BE ZERO.  THE
                                ; TEST WILL SET AND CLEAR THE SIGNAL CDAL6 AGAIN TO CHECK THAT THE DATA LEAD
                                ; TO THE TRACING FLIP-FLOP WAS NOT CLOCKED INTO THE TRACING FLIP-FLOP AS A ONE
                                ; OR HIGH STATE.  THE TEST WILL READ THE TRACE RAM ADDRESS AGAIN VALIDATING THE
                                ; ADDRESS TO BE ZERO.  THE TEST WILL NOW SET THE SIGNAL PDAL6 IN CONTROL REGIS-
                                ; TER 2 TO PRESET THE TRACING FLIP-FLOP TO A HIGH STATE.  THE SIGNAL CDAL6 IN
                                ; CONTROL REGISTER 0 WILL THEN BE SET AND CLEARED.  WITH THE SIGNALS TRANST H
                                ; AND   ST L BEING PULSED AND THE TRACING FLIP-FLOP IN THE PRESET STATE, A
                                ; PULSE WILL OCCUR ON THE SIGNAL CTR L WHICH WILL CAUSE THE TRACE RAM ADDRESS
                                ; REGISTER TO BE INCREMENTED BY ONE.  THE TEST WILL READ THE TRACE RAM ADDRESS
                                ; REGISTER CHECKING THE ADDRESS TO EQUAL 1.
                                ;--

                                        BGNTST
                                T30::
016056  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        BGNSEG
016062  104404                          TRAP    C$BSEG

                                        ;CLEAR LOW BYTE OF CONTROL REGISTER 0 TO CLEAR ANY BITS THAT MAY BE
                                        ;SET WHEN LOOPING ON AN ERROR.

016064  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR ALL LOW BITS
016070  004737  006102                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REG 0
016074  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
016076                                  ERRDF   1,,ROERDR               ;REGISTER 0 NOT EQUAL EXPECTED
016076  104455                          TRAP    C$ERDF
016100  000001                          .WORD   1
016102  000000                          .WORD   0
```

```
6261  016104  004604                          .WORD   R0EROR
6262  016106                                  CKLOOP
6263  016106  104406                          TRAP    C$CLP1
6264
6265                                          ;PRESET THE TRACING FLIP-FLOP BY SETTING PDAL6 TO A 1. THE OUTPUT OF
6266                                          ;THE TRACING FLIP-FLOP SHOULD BE SET HIGH.  WITH PDAL BITS 3-0 SET TO
6267                                          ;ZERO, THE SIGNAL PTERO L WILL BE ASSERTED IN THE POINTER REGISTER.
6268                                          ;PDAL5 ON A ZERO WILL HOLD THE FUNCTION SELECT F/F'S TO A 0 STATE (LOW).
6269
6270  016110  012737  000100  002376  1$:     MOV     #PDAL6!PTERO,R2LOAD     ;SETUP BITS TO BE LOADED
6271  016116  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
6272  016122  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
6273  016124                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
6274  016124  104455                          TRAP    C$ERDF
6275  016126  000002                          .WORD   2
6276  016130  000000                          .WORD   0
6277  016132  004704                          .WORD   R2EROR
6278  016134                                  CKLOOP
6279  016134  104406                          TRAP    C$CLP1
6280
6281                                          ;RELEASE THE PRESET SIDE OF THE TRACING FLIP-FLOP BY SETTING PDAL6 TO 0
6282
6283  016136  042737  000100  002376  2$:     BIC     #PDAL6,R2LOAD           ;SETUP BIT TO BE CLEARED
6284  016144  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
6285  016150  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
6286  016152                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
6287  016152  104455                          TRAP    C$ERDF
6288  016154  000002                          .WORD   2
6289  016156  000000                          .WORD   0
6290  016160  004704                          .WORD   R2EROR
6291  016162                                  CKLOOP
6292  016162  104406                          TRAP    C$CLP1
6293
6294                                          ;LOAD ADDRESS 1775 INTO TRACE RAM ADDRESS REGISTER
6295
6296  016164  012737  001775  002414  3$:     MOV     #1775,R6LOAD            ;SETUP ADDRESS TO BE LOADED
6297  016172  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP MASK TO IGNORE UNUSED BITS
6298  016200  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD,READ AND CHECK TRAM ADDR REG
6299  016204  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
6300  016206                                  ERRDF   -4,TRADER,RO26ER        ;TRAM ADDRESS REG NOT EQUAL 1775
6301  016206  104455                          TRAP    C$ERDF
6302  016210  000004                          .WORD   4
6303  016212  002462                          .WORD   -TRADER
6304  016214  004734                          .WORD   RO26ER
6305  016216                                  CKLOOP
6306  016216  104406                          TRAP    -C$CLP
6307
6308                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. SETTING AND CLEARING
6309                                          ;CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE.  THIS WILL
6310                                          ;THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE THE SIGNAL
6311                                          ;ORST L TO PULSE.  WITH THE TRACING FLIP-FLOP PRESET AND THE SIGNALS
6312                                          ;TRANST H AND TRST L BEING PULSED, A PULSE WILL OCCUR ON THE SIGNAL
6313                                          ;CTR L WHICH WILL CAUSE THE TRACE RAM ADDRESS REGISTER TO BE COUNTED
6314                                          ;UP BY ONE.
6315
6316  016220  004737  006640          4$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
```

```
                                        ;CHECK THAT THE SIGNAL "CTR L" UPDATED THE TRACE RAM ADDRESS REGISTER

016224  005237  002414        6$:     INC     R6LOAD                  ;UPDATE THE EXPECTED ADDRESS TO 1776
016230  004737  006256                JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
016234  001405                        BEQ     7$                      ;IF UPDATED BY ONE THEN CONTINUE
016236                                ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO UPDAT   DDRESS BY ONE
016236  104455                        TRAP    C$ERDF
016240  000004                        .WORD   4
016242  002462                        .WORD   TRADER
016244  004734                        .WORD   R026ER
016246                                CKLOOP
016246  104406                        TRAP    C$CLP1

                                        ;SET AND CLEAR CDAL0 IN CONTROL REGISTER 0 TO CHECK THAT CDAL0 WILL
                                        ;CLEAR THE TRACE RAM ADDRESS REGISTER AND THE TRACING FLIP-FLOP.

016250  052737  000001  002370  7$:     BIS     #CDAL0,R0LOAD           ;SETUP BIT TO BE SET
016256  004737  006102                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
016262  001405                        BEQ     8$                      ;IF LOADED OK THEN CONTINUE
016264                                ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
016264  104455                        TRAP    C$ERDF
016266  000001                        .WORD   1
016270  000000                        .WORD   0
016272  004604                        .WORD   R0EROR
016274                                CKLOOP
016274  104406                        TRAP    C$CLP1

                                        ;CLEAR THE SIGNAL CDAL0 IN CONTROL REGISTER 0

016276  042737  000001  002370  8$:     BIC     #CDAL0,R0LOAD           ;SETUP BIT TO BE CLEARED
016304  004737  006102                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
016310  001405                        BEQ     9$                      ;IF LOADED OK THEN CONTINUE
016312                                ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQULA EXPECTED
016312  104455                        TRAP    C$ERDF
016314  000001                        .WORD   1
016316  000000                        .WORD   0
016320  004604                        .WORD   R0EROR
016322                                CKLOOP
016322  104406                        TRAP    C$CLP1

                                        ;READ TRACE RAM ADDRESS REGISTER CHECKING THAT THE SIGNAL CDAL0
                                        ;CLEARED THE TRACE RAM ADDRESS REGISTER.

016324  005037  002414        9$:     CLR     R6LOAD                  ;SET EXPECTED ADDRESS TO BE 0
016330  004737  006256                JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
016334  001405                        BEQ     10$                     ;IF ADDRESS EQUALS 0 THEN CONTINUE
016336                                ERRDF   4,TRADER,R026ER         ;CDAL0 FAILED TO CLEAR TRAM ADDR REG
016336  104455                        TRAP    C$ERDF
016340  000004                        .WORD   4
016342  002462                        .WORD   TRADER
016344  004734                        .WORD   R026ER
016346                                CKLOOP
016346  104406                        TRAP    C$CLP1

                                        ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0 TO CHECK THAT THE
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                                        ;SIGNAL CDAL0 CLEARED THE TRACING FLIP-FLOP. NO PULSE SHOULD OCCUR
                                        ;ON THE SIGNAL CTR L, THEREFORE, THE TRACE RAM ADDRESS REGISTER
                                        ;SHOULD NOT BE UPDATED WHEN THE SIGNALS TRANST H AND TRST L ARE PULSED.

016350  004737  006640        10$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0

                                        ;READ TRACE RAM ADDRESS REGISTER AGAIN CHECKING THAT THE TRACE ADDRESS
                                        ;REGISTER DID NOT INCREMENT WHEN THE TRACING FLIP-FLOP WAS IN A 0
                                        ;STATE. THE TRACING FLIP-FLOP WAS CLEARED PREVIOUSLY VIA THE SIGNAL CDAL0.

016354  004737  006256        12$:    JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRS REGISTER
016360  001405                        BEQ     13$                     ;IF ADDRESS STILL 0 THEN CONTINUE
016362                                ERRDF   4,TRADER,R026ER         ;TRACING F/F FIALED TO 0 VIA CDAL0
016362  104455                        TRAP    C$ERDF
016364  000004                        .WORD   4
016366  002462                        .WORD   TRADER
016370  004734                        .WORD   R026ER
016372                                CKLOOP
016372  104406                        TRAP    C$CLP1
                                                                        ;OR PULSE ISSUED ON SIGNAL CTR L

                                        ;CLOCK CDAL6 AGAIN TO CHECK THAT THE DATA INPUT LEAD TO THE TRACING
                                        ;FLIP-FLOP WAS NOT HIGH + THAT THE TRACING FLIP-FLOP DID NOT GET SET.

016374  004737  006640        13$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL RE  0

                                        ;READ THE TRACE RAM ADDRESS REGISTER AGAIN CHECKING THAT THE ADDRESS
                                        ;REGISTER DID NOT INCREMENT WHEN THE TRACING FLIP-FLOP WAS IN THE
                                        ;ZERO STATE.  IF THE ADDRESS DID CHANGE, CHECK THE DATA INPUT LEAD
                                        ;TO THE TRACING FLIP-FLOP. IT SHOULD BE AT A LOW LEVEL.

016400  004737  006256        15$:    JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
016404  001405                        BEQ     16$                     ;IF ADDRESS STILL 0 THEN CONTINUE
016406                                ERRDF   4,TRADER,R026ER         ;TRACING FLIP-FLOP GOT SET
016406  104455                        TRAP    C$ERDF
016410  000004                        .WORD   4
016412  002462                        .WORD   TRADER
016414  004734                        .WORD   R026ER
016416                                CKLOOP
016416  104406                        TRAP    C$CLP1

                                        ;SET PDAL6 TO A 1 IN CONTROL REGISTER 2 TO PRESET THE TRACING FLIP-FLOP
                                        ;TO A ONE. WHEN THE TRACING FLIP-FLOP IS PRESET AND THE SIGNAL CDAL6 IS
                                        ;TOGGLED, A PULSE WILL OCCUR ON THE SIGNAL CTR L WHICH SHOULD INCREMENT
                                        ;THE TRACE RAM ADDRESS REGISTER.

016420  052737  000100  002376  16$:    BIS     #PDAL6,R2LOAD           ;SETUP TO CLEAR PDAL6
016426  004737  006134                JSR     PC,LDRDR2               ;GO LOAD,READ AND CHECK REGISTER 2
016432  001405                        BEQ     17$                     ;IF LOADED OK THEN CONTINUE
016434                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
016434  104455                        TRAP    C$ERDF
016436  000002                        .WORD   2
016440  000000                        .WORD   0
016442  004704                        .WORD   R2EROR
016444                                CKLOOP
016444  104406                        TRAP    C$CLP1
```

```
                                        ;CLOCK SIGNAL CDAL6 TO CAUSE A PULSE TO OCCUR ON THE SIGNAL CTR L WHEN
                                        ;THE TRACING FLIP-FLOP IS PRESET

016446  004737  00664C        17$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0

                                        ;CHECK THAT THE TRACE RAM ADDRESS REGISTER WAS INCREMENTED BY ONE
                                        ;WHEN THE TRACING FLIP-FLOP IS SET AND THE SIGNALS TRANST H AND TRST L
                                        ;ARE PULSED.  THE ABOVE SIGNALS WILL CAUSE A PULSE ON CTR L WHICH
                                        ;WILL CAUSE THE TRACE RAM ADDRESS REGISTER TO INCREMENT.

016452  005237  002414        19$:    INC     R6LOAD                  ;UPDATE EXPECTED TRAM ADDRESS REG
016456  004737  006256                JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
016462  001404                        BEQ     20$                     ;IF INCREMENTED BY 1 THEN CONTINUE
016464                                ERRDF   4,TRADER,R026ER         ;TRACING F/F PROBABLY NOT PRESET
016464  104455                        TRAP    C$ERDF
016466  000004                        .WORD   4
016470  002462                        .WORD   TRADER
016472  004734                        .WORD   R026ER
016474                          20$:  ENDSEG
016474                          10000$:
016474  104405                        TRAP    C$ESEG
016476                                ENDTST
016476                          L10114:
016476  104401                        TRAP    C$ETST
```

```
                                .SBTTL  TEST 31: CHECK CDAL5 H AND TRAD10 H TO INHIBIT PULSES ON CTR L

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE INCREMENTED
                                ; BY ONE VIA THE SIGNAL "CTR L" WHEN THE TRACING FLIP-FLOP IS SET TO A ONE,
                                ; CDAL REGISTER BIT 5 IS SET TO A ONE, TRACE RAM ADDRESS REGISTER BIT 10 IS SET
                                ; TO A ZERO AND THE SIGNALS TRANST H AND TRST L ARE PULSED VIA THE SETTING AND
                                ; CLEARING OF CDAL6 IN CONTROL REGISTER 0.  THE TEST WILL CHECK THAT THE TRACE
                                ; RAM ADDRESS REGISTER WILL NOT GET INCREMENTED BY ONE VIA THE SIGNAL CTR L WHEN
                                ; THE TRACING FLIP-FLOP IS SET TO A ONE, CDAL REGISTER BIT 5 IS SET TO A ONE,
                                ; TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE, AND THE SIGNALS TRANST H
                                ; AND TRST L ARE PULSED VIA THE SETTING AND CLEARING OF CDAL6 IN CONTROL REGIS-
                                ; TER 0.  THE TEST WILL THEN CHECK THAT THE TRACE RAM ADDRESS REGISTER CAN BE
                                ; INCREMENTED BY ONE VIA THE SIGNAL CTR L WHEN THE TRACING FLIP-FLOP IS SET TO
                                ; A ONE, CDAL REGISTER BIT 5 IS SET TO A ZERO, TRACE RAM ADDRESS REGISTER BIT
                                ; 10 IS SET TO A ONE, AND THE SIGNALS TRANST H AND TRST L ARE PULSED VIA THE
                                ; SETTING AND CLEARING OF CDAL6 IN CONTROL REGISTER 0.
                                ;--

016500                                  BGNTST
016500                          T31::

016500  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

016504                                  BGNSEG
016504  104404                          TRAP    C$BSEG

                                ;SET CDAL5 H TO A ONE IN CONTROL REGISTER 0 AND CLEAR ALL OTHER R/W
                                ;BITS IN THE LOW BYTE.  WHEN CDAL5 H IS SET TO A ONE, TRACING WILL BE
                                ;INHIBITED WHEN TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE.

016506  112737  000040  002370          MOVB    #CDAL5,R0LOAD           ;SETUP BIT TO BE LOADED
016514  004737  006102                  JSR     PC,LDRDR0               ;LOAD, READ AND CHECK CONTROL REG 0
016520  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
016522                                  ERRDF   1,,R0ERR                ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
016522  104455                          TRAP    C$ERDF
016524  000001                          .WORD   1
016526  000000                          .WORD   0
016530  004604                          .WORD   R0ERR
016532                                  CKLOOP
016532  104406                          TRAP    C$CLP1

                                ;PRESET THE TRACING FLIP-FLOP BY SETTING PDAL6 H TO A ONE.  SETTING
                                ;PDAL6 H TO A ONE WILL CAUSE THE OUTPUT OF THE TRACING FLIP-FLOP TO BE
                                ;SET TO THE HIGH STATE.  PDAL BITS 3:0 WILL BE SET TO A ZERO WHICH WILL
                                ;CAUSE THE SIGNAL PTER0 L TO BE ASSERTED IN THE POINTER REGISTER.  PDAL5 H
                                ;WILL BE SET TO A ZERO WHICH WILL CAUSE THE FUNCTION SELECT FLIP-FLOPS
                                ;TO BE HELD TO A ZERO STATE (LOW).

016534  012737  000100  002376  1$:     MOV     #PDAL6!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
016542  004737  006134                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK PDAL REGISTER
016546  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
016550                                  ERRDF   2,,R2ERR                ;REGISTER 2 NOT EQUAL EXPECTED
016550  104455                          TRAP    C$ERDF
016552  000002                          .WORD   2
016554  000000                          .WORD   0
```

```
6511  016556  004704                          .WORD   R2EROR
6512  016560                                  CKLOOP
6513  016560  104406                          TRAP    C$CLP1
6514
6515                                          ;RELEASE THE PRESET SIDE OF THE TRACING FLIP-FLOP BY SETTING PDAL6 H
6516                                          ;TO A ZERO.
6517
6518  016562  042737  000100  002376  2$:     BIC     #PDAL6,R2LOAD           ;SETUP BIT TO BE CLEARED
6519  016570  004737  006134                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK PDAL REGISTER
6520  016574  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
6521  016576                                  ERRDF   2,,R2ERCR               ;PDAL REGISTER NOT EQUAL EXPECTED
6522  016576  104455                          TRAP    C$ERDF
6523  016600  000002                          .WORD   2
6524  016602  000000                          .WORD   0
6525  016604  004704                          .WORD   R2EROR
6526  016606                                  CKLOOP
6527  016606  104406                          TRAP    C$CLP1
6528
6529                                          ;LOAD, READ AND CHECK THE TRACE RAM ADDRESS REGISTER WITH A DATA PATTERN
6530                                          ;OF 1777.
6531
6532  016610  012737  001777  002414  3$:     MOV     #1777,R6LOAD            ;SETUP DATA PATTERN TO BE LOADED
6533  016616  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNUSED BITS
6534  016624  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK TRAM ADDR REG
6535  016630  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
6536  016632                                  ERRDF   4,TRADER,R026ER         ;TRAM ADDRESS REG ERROR - NOT = 1777
6537  016632  104455                          TRAP    C$ERDF
6538  016634  000004                          .WORD   4
6539  016636  002462                          .WORD   TRADER
6540  016640  004734                          .WORD   R026ER
6541  016642                                  CKLOOP
6542  016642  104406                          TRAP    C$CLP1
6543
6544                                          ;CLOCK THE SIGNAL CDAL6 H IN CONTROL REGISTER 0.  SETTING AND CLEARING
6545                                          ;CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED. THIS
6546                                          ;WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE THE SIGNAL
6547                                          ;ORST L TO PULSE. A PULSE SHOULD OCCUR ON THE SIGNAL CTR L AS A RESULT
6548                                          ;OF THE TRACING FLIP-FLOP BEING SET, CDAL REGISTER BIT 5 BEING A ONE,
6549                                          ;TRACE RAM ADDRESS REGISTER BIT 10 BEING SET TO A ZERO AND THE SIGNALS
6550                                          ;TRANST H AND TRST L BEING PULSED.  A PULSE ON THE SIGNAL CTR L WILL
6551                                          ;CAUSE THE TRACE RAM ADDRESS REGISTER TO BE INCREMENTED FROM 1777 TO
6552                                          ;2000, THUS SETTING TRAD10 TO A ONE.
6553
6554  016644  004737  006640          4$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 H TO PULSE TRANST H
6555
6556                                          ;CHECK THAT THE SIGNAL "CTR L" INCREMENTED THE TRACE RAM ADDRESS REGISTER
6557                                          ;FROM 1777 TO 2000.  TRACE RAM ADDRESS REGISTER BIT 10 IS NOW SET TO A 1
6558
6559  016650  005237  002414                  INC     R6LOAD                  ;UPDATE EXPECTED ADDRESS TO 2000
6560  016654  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
6561  016660  001405                          BEQ     5$                      ;IF OK THEN CONTINUE
6562  016662                                  ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO INCREMENT TRAM ADDR REG
6563  016662  104455                          TRAP    C$ERDF
6564  016664  000004                          .WORD   4
6565  016666  002462                          .WORD   TRADER
6565  016670  004734                          .WORD   R026ER
```

```
6567  016672                                  CKLOOP
6568  016672  104406                          TRAP    C$CLP1
6569
6570                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0 TO CAUSE THE SIGNALS
6571                                          ;TRANST H AND TRST L TO BE PULSED.  THIS WILL THEN CAUSE THE SIGNAL
6572                                          ;ANST L TO BE PULSED WHICH WILL THEN CAUSE THE SIGNAL ORST L TO BE
6573                                          ;PULSED.  NO PULSE SHOULD OCCUR ON THE SIGNAL CTR L WHEN CDAL REGISTER
6574                                          ;BIT 5 IS SET TO A ONE AND TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO
6575                                          ;A ONE EVEN THOUGH THE TRACING FLIP-FLOP IS SET TO A ONE AND THE SIGNALS
6576                                          ;TRANST H AND TRST L WERE PULSED.  THE TRACE RAM ADDRESS REGISTER SHOULD
6577                                          ;REMAIN UNCHANGED AFTER TOGGLING CDAL6 H.
6578
6579  016674  004737  006640          5$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 H TO PULSE TRANST H
6580
6581                                          ;READ AND CHECK THE TRACE RAM ADDRESS REGISTER TO CHECK THAT IT DID NOT
6582                                          ;GET INCREMENTED BY A PULSE ON "CTR L" WHEN CDAL REGISTER BIT 5 WAS SET
6583                                          ;TO A ONE AND TRACE RAM ADDRESS REGISTER BIT 10 WAS SET TO A ONE.
6584
6585  016700  004737  006256                  JSR     PC,READR4               ;READ AND CHECK TRACE RAM ADDRESS REG
6586  016704  001405                          BEQ     6$                      ;IF NO CHANGE THEN CONTINUE
6587  016706                                  ERRDF   4,TRADER,R026ER         ; RAM ADDRESS REGISTER INCREMENTED
6588  016706  104455                          TRAP    C$ERDF
6589  016710  000004                          .WORD   4
6590  016712  002462                          .WORD   TRADER
6591  016714  004734                          .WORD   R026ER
6592  016716                                  CKLOOP
6593  016716  104406                          TRAP    C$CLP1
6594
6595                                          ;SET THE SIGNAL CDAL5 H TO A ZERO TO ALLOW A PULSE TO BE GENERATED ON
6596                                          ;THE SIGNAL "CTR L" THE NEXT TIME CDAL6 H IS TOGGLED.
6597
6598  016720  042737  000040  002370  6$:     BIC     #CDAL5,ROLOAD           ;SETUP BIT TO BE LOADED
6599  016726  004737  006102                  JSR     PC,LDRDR0               ;LOAD, READ AND CHECK REGISTER 0
6600  016732  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
6601  016734                                  ERRDF   1,,R0EROR               ;CONTROL REG 0 NOT EQUAL EXPECTED
6602  016734  104455                          TRAP    C$ERDF
6603  016736  000001                          .WORD   1
6604  016740  000000                          .WORD   0
6605  016742  004604                          .WORD   R0EROR
6606  016744                                  CKLOOP
6607  016744  104406                          TRAP    C$CLP1
6608
6609                                          ;TOGGLE THE SIGNAL CDAL6 IN CONTROL REGISTER 0 TO CAUSE THE SIGNALS
6610                                          ;TRANST H AND TRST L TO BE PULSED.  THIS WILL THEN CAUSE THE SIGNAL
6611                                          ;ANST L TO BE PULSED WHICH WILL THEN CAUSE THE SIGNAL ORST L TO BE
6612                                          ;PULSED.  A PULSE SHOULD OCCUR ON THE SIGNAL CTR L AS A RESULT OF THE
6613                                          ;TRACING FLIP-FLOP BEING SET TO A ONE, CDAL REGISTER BIT 5 BEING SET
6614                                          ;TO A ZERO, TRACE RAM ADDRESS REGISTER BIT 10 BEING SET TO A ONE AND
6615                                          ;THE SIGNALS TRANST H AND TRST L BEING ASSERTED.  A PULSE ON THE SIGNAL
6616                                          ;CTR L WILL CAUSE THE TRACE RAM ADDRESS REGISTER TO INCREMENT FROM
6617                                          ;2000 TO 2001.
6618
6619  016746  004737  006640          7$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 H TO PULSE TRANST H
6620
6621                                          ;READ AND CHECK THE TRACE RAM ADDRESS REGISTER TO CHECK THAT IT WAS
6622                                          ;INCREMENTED BY ONE VIA A PULSE ON THE SIGNAL "CTR L" WHEN CDAL5 H IS
```

```
6623                                                    ;SET TO A ZERO AND TRACE RAM ADDRESS REGISTER BIT 10 IS SET TO A ONE.
6624
6625  016752  005237  002414                          INC     R6LOAD                  ;UPLATE EXPECTED ADDRESS TO 2001
6626  016756  004737  006256                          JSR     PC,READR6               ;READ AND CHECK TRACE RAM ADDRESS REG
6627  016762  001404                                  BEQ     8$                      ;IF OK THEN CONTINUE
6628  016764                                          ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO +1 TRAM ADDRESS REG
6629  016764  104455                                  TRAP    C$ERDF
6630  016766  000004                                  .WORD   4
6631  016770  002462                                  .WORD   TRADER
6632  016772  004734                                  .WORD   R026ER
6633  016774                                  8$:     ENDSEG
6634  016774                                  10000$:
6635  016774  104405                                  TRAP    C$ESEG
6636
6637  016776                                          ENDTST
6638  016776                                  L10115:
6639  016776  104401                                  TRAP    C$ETST
6640
```

```
                                .SBTTL  TEST 32: LOAD TRACE RAMS VIA SIGNALS CTR H AND CTR L

                                ;++
                                ; THIS TEST WILL CHECK THAT THE TRACE RAMS CAN BE LOADED FROM THE TRACE RAM
                                ; DATA IN BUFFERS VIA THE SIGNALS CTR H AND CTR L.
                                ;
                                ; THE TEST WILL LOAD AND CHECK THE TRACE RAM DATA IN BUFFERS WITH THE FOLLOWING
                                ; PATTERNS:
                                ;    TRDI 15:0  - DATA PATTERN OF 151515
                                ;    TRDI 31:16 - DATA PATTERN OF 113131
                                ;    TRDI 47:32 - DATA PATTERN OF 074747
                                ;    TRDI 59:48 - DATA PATTERN OF 005555
                                ; THE TEST WILL ASSERT THE SIGNAL TRSL0 L BY CLEARING THE LOW BYTE OF CONTROL
                                ; REGISTER 0.  THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA
                                ; IN BUFFERS.  THE TEST WILL LOAD ADDRESS 0 INTO THE TRACE RAM ADDRESS REGISTER
                                ; TO SELECT ADDRESS 0 OF ALL THE TRACE RAMS.  THE TEST WILL THEN PRESET THE
                                ; TRACING FLIP-FLOP BY SETTING PDAL6 IN CONTROL REGISTER 2.  THE TEST WILL NOW
                                ; SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING
                                ; CDAL6 WITH THE TRACING FLIP-FLOP IN THE PRESET STATE, WILL CAUSE THE SIGNALS
                                ; CTR L AND CTR H TO PULSE.  THE SIGNAL CTR L WILL CAUSE THE TRACE RAM ADDRESS
                                ; REGISTER TO BE INCREMENTED BY ONE.  THE SIGNALS CTR L AND CTR H WILL LOAD THE
                                ; TRACE RAMS WITH THE DATA STORED IN THE TRACE RAM DATA IN BUFFER BITS TRD. 55:0.
                                ; AFTER SETTING AND CLEARING CDAL6, THE PROGRAM WILL CHECK THAT THE TRACE RAM
                                ; ADDRESS REGISTER INCREMENTED TO ADDRESS ONE. THE TEST WILL THEN RESET THE
                                ; TRACE RAM ADDRESS REGISTER TO ADDRESS 0.  THE TEST WILL THEN ASSERT THE SIGNAL
                                ; TRSL1 L BY SETTING THE SIGNAL CDAL2 TO A ONE IN CONTROL REIGSTER 0.  THE SIGNAL
                                ; TRSL1 L WILL ENABLE THE TRACE RAMS TO BE READ.  THE TEST WILL NOW READ ADDRESS
                                ; ZERO OF EACH TRACE RAM CHECKING THE DATA TO BE THAT WHICH WAS WRITTEN INTO THE
                                ; TRACE RAM DATA IN BUFFERS.
                                ;--

017000                                  BGNTST
017000                          T32::
017000  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

017004                                  BGNSUB
017004                          T32 1:
017004  104402                          TRAP    C$BSUB

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER 15:0 WITH A DATA PATTERN
                                        ;OF 1515 .

017006  012737  151515  002414          MOV     #151515,R6LOAD          ;SETUP DATA TO BE LOADED
017014  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ AND CHECK TRAM DATA IN BUF
017020  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
017022                                  ENDSUB
017022                          L10117:
017022  104403                          TRA     C$ES B

017024                                  BGNSUB
017024                          T32.2:
017024  104402                          TRAP    C$BSUB

                                        ;LOAD, READ AND CHECK TRA E RAM DATA IN BUFFER 31:16 WITH A DATA PATTERN
                                        ;OF 113131.
```

```
 6697  017026  012737  113131  002414          MOV     #113131,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
 6698  017034  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ AND CHECK TRAM DATA IN BUF
 6699  017040  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
 6700  017042                                  ENDSUB
 6701  017042                          L10120:
 6702  017042  104403                          TRAP    C$ESUB
 6703
 6704  017044                                  BGNSUB
 6705  017044                          T32.3:
 6706  017044  104402                          TRAP    C$BSUB
 6707
 6708                                          ;LOAD,READ AND CHECK TRACE RAM DATA IN BUFFER 47:32 WITH DATA PATTERN
 6709                                          ;OF 074747
 6710
 6711  017046  012737  074747  002414          MOV     #074747,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
 6712  017054  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ AND CHECK TRAM DATA IN BUF
 6713  017060  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
 6714  017062                                  ENDSUB
 6715  017062                          L10121:
 6716  017062  104403                          TRAP    C$ESUB
 6717
 6718  017064                                  BGNSUB
 6719  017064                          T32.4:
 6720  017064  104402                          TRAP    C$BSUB
 6721
 6722                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER 59:48 WITH DATA PATTERN
 6723                                          ;OF 005555
 6724
 6725  017066  012737  005555  002414          MOV     #005555,R6LOAD          ;SETUP DATA PATTERN TO BE LOADED
 6726  017074  004537  006426                  JSR     R5,TRDIBF               ;LOAD,READ AND CHECK TRAM DATA IN BUF
 6727  017100  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
 6728  017102                                  ENDSUB
 6729  017102                          L10122:
 6730  017102  104403                          TRAP    C$FSUB
 6731
 6732  017104                                  BGNSUB
 6733  017104                          T32.5:
 6734  017104  104402                          TRAP    C$BSUB
 6735
 6736                                          ;CLEAR LOW BYTE OF CONTROL REGISTER 0. CDAL3 AND CDAL2 BEING CLEARED
 6737                                          ;WILL ASSERT THE SIGNAL TRSL0 L WHICH WILL ENABLE THE OUTPUTS OF THE
 6738                                          ;TRACE RAM DATA IN BUFFERS
 6739
 6740  01, 06  105037  002370                  CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE
 6741  017112  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
 6742  017116  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
 6743  017120                                  ERRDF   1,,R0ERR0R              ;REGISTER 0 NOT EQUAL EXPECTED
 6744  017120  104455                          TRAP    C$ERDF
 6745  017122  000001                          .WORD   1
 6746  017124  000000                          .WORD   0
 6747  017126  004604                          .WORD   R0ERR0R
 6748  017130                                  CKLOOP
 6749  017130  104406                          TRAP    C$CLP1
 6750
 6751                                          ;LOAD, READ AND CHECK TRACE RAM ADDRESS REGISTER WITH ADDRESS 0
 6752
```

```
6753  017132  005037  006374          1$:     CLR     TRADRS                  ;SET ADDRESS TO BE LOADED TO 0
6754  017136  004737  006310                  JSR     PC,TRADLD               ;GO LOAD AND CHECK TRACE RAM ADDRESS REG
6755
6756                                          ;SET PDAL6 IN CONTROL REGISTER 2 TO PRESET THE TRACING FLIP-FLOP TO
6757                                          ;THE HIGH STATE.
6758
6759  017142  052737  000100  002376          BIS     #PDAL6,R2LOAD           ;SETUP BIT TO BE LOADED
6760  017150  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
6761  017154  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
6762  017156                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
6763  017156  10445-                          TRAP    C$ERDF
6764  017160  000002                          .WORD   2
6765  017162  000000                          .WORD   0
6766  017164  004704                          .WORD   R2EROR
6767  017166                                  CKLOOP
6768  017166  104406                          TRAP    C$CLP1
6769
6770                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING CDAL6
6771                                          ;WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE.  THIS WILL THEN
6772                                          ;CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE THE SIGNAL ORST L
6773                                          ;TO PULSE.  WHEN THE TRACING FLIP-FLOP IS IN THE PRESET STATE AND THE
6774                                          ;SIGNALS TRANST H AND TRST L ARE BEING PULSED, A PULSE WILL OCCUR ON
6775                                          ;THE SIGNALS CTR L AND CTR H.  THE SIGNAL CTR L WILL CAUSE THE TRACE RAM
6776                                          ;ADDRESS REGISTER TO BE INCREMENTED BY ONE.  THE SIGNALS CTR L AND CTR H
6777                                          ;WILL LOAD THE DATA FROM THE TRACE RAM DATA IN BUFFER BITS TRDI 55:0
6778                                          ;INTO ADDRESS 0 OF THE TRACE RAMS.
6779
6780  017170  004737  006640          2$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
6781
6782                                          ;READ TRACE RAM ADDRESS REGISTER CHECKING THE THE SIGNAL "CTR L"
6783                                          ;INCREMENTED THE TRACE RAM ADDRESS REGISTER TO ADDRESS ONE.
6784
6785  017174  012737  000001  002414  4$:     MOV     #1,R6LOAD               ;SETUP EXPECTED ADDRESS
6786  017202  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
6787  017206  001405                          BEQ     5$                      ;IF ADDRESS ONE THEN CONTINUE
6788  017210                                  ERRDF   4,TRADER,R026ER         ;CTR L FAILED TO INCREMENT ADDRESS REG
6789  017210  104455                          TRAP    C$ERDF
6790  017212  000004                          .WORD   4
6791  017214  002462                          .WORD   TRADER
6792  017216  004734                          .WORD   R026ER
6793  017220                                  CKLOOP
6794  017220  104406                          TRAP    C$CLP1
6795
6796                                          ;RESET THE TRACE RAM ADDRESS REGISTER TO ADDRESS 0. THE POINTER REGISTER
6797                                          ;ON EXIT FROM ROUTINE "TRADLD" WILL HAVE THE SIGNAL PTER0 L ASSERTED.
6798
6799  017222  004737  006310          5$:     JSR     PC,TRADLD               ;RESET TRAM ADDRESS REGISTER TO 0
6800
6801                                          ;SET CDAL2 TO A ONE AND CDAL3 TO A 0 IN CONTROL REGISTER 0 TO CAUSE THE
6802                                          ;SIGNAL TRSL1 L TO BE ASSERTED.  THE SIGNAL TRSL1 L WILL ENABLE THE
6803                                          ;TRACE RAMS SELECTED TO BE READ.
6804
6805  017226  052737  000004  002370          BIS     #CDAL2,R0LOAD           ;SETUP BIT TO BE SET
6806  017234  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
6807  017240  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
6808  017242                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
```

```
6809  017242  104455                          TRAP    C$ERDF
6810  017244  000001                          .WORD   1
6811  017246  000000                          .WORD   0
6812  017250  004604                          .WORD   R0EROR
6813  017252                                  CKLOOP
6814  017252  104406                          TRAP    C$CLP1
6815
6816                                          ;ASSERT THE SIGNAL PTER' L IN THE POINTER REGISTER VIA CONTROL REG 2.
6817
6818  017254  004537  006376          6$:     JSR     R5,ASSERT               ;GO ASSERT PTER1
6819  017260  000001                          .WORD   PTER1
6820
6821                                          ;READ TRACE RAM DATA BITS TRDI 15:0 FOR A DATA PATTERN OF 151515
6822
6823  017262  012737  151515  002414  7$:     MOV     #151515,R6LOAD          ;SETUP DATA PREVIOUSLY LOADED
6824  017270  005037  002416                  CLR     R6MASK                  ;SETUP TO READ ALL 16 BITS
6825  017274  004737  006256                  JSR     PC,READR6               ;CHECK TRACE  AM DATA BITS TRDI 15:0
6826  017300  001405                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
6827  017302                                  ERRDF   4,TRAM15,TRAMER         ;CTR L+H FAILED TO LOAD DATA
6828  017302  104455                          TRAP    C$ERDF
6829  017304  000004                          .WORD   4
6830  017306  002776                          .WORD   TRAM15
6831  017310  004764                          .WORD   TRAMER
6832  017312                                  CKLOOP
6833  017312  104406                          TRAP    C$CLP1
6834
6835                                          ;ASSERT THE SIGNAL PTER2 L IN THE POINTER REGISTER VIA CONTROL REG 2
6836
6837  017314  004537  006376          8$:     JSR     R5,ASSERT               ;GO ASSERT PTER2
6838  017320  000002                          .WORD   PTER2
6839
6840                                          ;READ TRACE RAM DATA BITS TRDI 31:16 FOR A DATA PAT ERN OF 113131.
6841
6842  017322  012737  113131  002414  9$:     MOV     #113131,R6LOAD          ;SETUP DATA PREVIOUSLY LOADED
6843  017330  004737  006256                  JSR     PC,READR6               ;CHECK TRACE RAM DATA BI  31:16
6844  017334  001405                          BEQ     10$                     ;IF DATA OK THEN CONTINI
6845  017336                                  ERRDF   4,TRAM31,TRAMER         ;CTR L+H FAILED TO LOAD DATA
6846  017336  104455                          TRAP    C$ERDF
6847  017340  000004                          .WORD   4
6848  017342  003032                          .WORD   TRAM31
6849  017344  004764                          .WORD   TRAMER
6850  017346                                  CKLOOP
6851  017346   04406                          TRAP    C$CLP1
6852
6853                                          ;ASSERT THE SIGNAL PTER3 L IN THE POINTER REGISTER VIA CONTROL REG 2
6854
6855  017350  004537  006376          10$:    JSR     R ,ASSERT               ;GO ASSERT PTER3
6856  017354  000003                          .WORD   PTER3
6857
6858                                          ;READ TRACE RAM DATA BITS TRDI 47:32 FOR A DATA PATTERN OF 074747
6859
6860  017356  012737  074747  002414   1$:    MOV     #074747,R6LOAD          ;SETUP DATA PATTERN PREVIOUSLY LOADED
6861  017364  004737  006256                  JSR     PC,READR6               ;CHECK TRACE RAM DATA BITS 47:32
6862  017370  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
6863  017372                                  ERRDF   4,TRAM47,TRAMER         ;CTR L+H FAILED TO LOAD DATA
6864  017372  104455                          TRAP    C$ERDF
```

```
6865  017374  000004                          .WORD   4
6866  017376  003067                          .WORD   TRAM47
6867  017400  004764                          .WORD   TRAMER
6868  017402                                  CKLOOP
6869  017402  104406                          TRAP    C$CLP1
6870
6871                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REG 2
6872
6873  017404  004537  006376          12$:    JSR     R5,ASSERT               ;GO ASSERT PTER4
6874  017410  000004                          .WORD   PTER4
6875
6876                                          ;READ TRACE RAM DATA BITS TRD! 55:48 FOR A DATA PATTERN OF '55
6877
6878  017412  012737  000155  002414   7$:    MOV     #155,R6LOAD             ;SETUP DATA PREVIOUSLY WRITTEN -4 BITS
6879  017420  012737  177400  002416          MOV     #177400,R6MASK          ;SETUP TO IGNORE UNUSED BITS
6880  017426  004737  006256                  JSR     PC,READR6               ;CHECK TRACE RAM DATA BITS 55:48
6881  017432  001404                          BEQ     14$                     ;IF DATA OK THEN CONTINUE
6882  017434                                  ERRDF   4,TRAM55,TRAMER         ;CTR L+H FAILED TO LOAD DATA
6883  017434  104455                          TRAP    C$ERDF
6884  017436  000004                          .WORD   4
6885  017440  003124                          .WORD   TRAM55
6886  017442  004[ 54                         .WORD   TRAMER
6887  017444                          14$:    ENDSUB
6888  017444                          L10123:
6889  017444  104403                          TRAP    C$ESUB
6890  017446                                  ENDTST
6891  017446                          L10116:
6892  017446  104401                          TRAP    C$ETST
6893
```

```
                                .SBTTL  TEST 33  OR ADDRESS REG TEST (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK THE OR ADDRESS REGISTER BITS (ORAD 3:0) BY LOADING AN
                                ; ALTERNATING ONES AND ZEROES DATA PATTERN (12) AND THEN AN ALTERNATING ZEROES
                                ; AND ONES DATA PATTERN (05).  TO WRITE AND READ THE OR ADDRESS REGISTER, THE
                                ; PROGRAM WILL CLEAR CONTROL REGISTER 0 BITS (CDAL 7:0). CDAL7 BEING A ZERO
                                ; WILL ENABLE THE OUTPUTS OF THE OR ADDRESS REGISTER.  THE PROGRAM WILL SET
                                ; PDAL3 TO PDAL0 TO ALL ONES WHICH WILL CAUSE THE SIGNAL PTER15 L TO BE ASSERTED
                                ; IN THE POINTER REGISTER.  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE
                                ; SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H.  THE
                                ; SIGNAL WPT15 H WILL LOAD THE DATA ON THE WRITE COMMAND INTO OR ADDRESS REGIS
                                ; TER BITS ORAD3 TO ORAD0.  ON A READ COMMAND TO CONTROL REGISTER 6 WITH THE
                                ; SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT15 H. THE
                                ; SIGNAL RPT15 H WILL READ THE DATA FROM THE OR ADDRESS REGISTER.
                                ;--

017450                                  BGNTST
017450                          T33::
017450  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

017454                                  BGNSEG
017454  104404                          TRAP    C$BSEG

                                ;CONTROL REGISTER 0 BITS CDAL 7.0 ARE CLEARED IN THE ROUTINE "INITED".
                                ;CDAL7 BEING A 0 WILL ENABLE THE OUTPUTS OF THE OR ADDRESS REGISTER.

                                ;SET THE SIGNAL PTER15 L IN THE POINTER REGISTER BY LOADING ALL ONES
                                ;INTO PDAL BITS 3:0 IN CONTROL REGISTER 2.

017456  004537  006376                  JSR     R5,ASSERT               ;GO ASSERT PTER15
017462  000017                          .WORD   PTER15

                                ;WRITE, READ AND CHECK OR ADDRESS REGISTER WITH AN ALTERNATING ONES
                                ;AND ZEROES DATA PATTERN (12). THE SIGNAL WPT15 H WILL PULSE ON A
                                ;WRITE COMMAND TO CONTROL REGISTER 6. THE SIGNAL RPT15 H WILL PULSE
                                ;ON A READ COMMAND TO CONTROL REGISTER 6.

017464  012737  000012  002414  1$:     MOV     #12,R6LOAD              ;SETUP ONES AND ZEROES DATA PATTERN
017472  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNUSED BITS
017500  004737  006250                  JSR     PC,LDRDR6               ;LOAD, RAD AND CHECK OR ADDRESS REG
017504  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
017506                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL 12
017506  104455                          TRAP    C$ERDF
017510  000004                          .WORD   4
017512  003161                          .WORD   ORADER
017514  004734                          .WORD   R026ER
017516                                  CKLOOP
017516  104406                          TRAP    C$CLP1
```

```
6944
6945                                                    ;WRITE, READ AND CHECK OR ADDRESS REGISTER WITH AN ALTERNATING ZEROES
6946                                                    ;AND ONES DATA PATTERN (05). THE SIGNAL WPT15 H WILL PULSE ON A WRITE
6947                                                    ;COMMAND TO CONTROL REGISTER 6.  THE SIGNAL RPT15 H WILL PULSE ON A
6948                                                    ;READ COMMAND TO CONTROL REGISTER 6.
6949
6950  017520  012737  000005  002414  2$:     MOV     #5,R6LOAD               ;SETUP ZEROES AND ONES DATA PATTERN
6951  017526  004737  006250                  JSR     PC,LDRDR6               ;LOAD,READ AND CHECK OR ADDRESS REG
6952  017532  001404                         BEQ     3$                      ;IF LOADED OK THEN CONTINUE
6953  017534                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL TO 5
6954  017534  104455                         TRAP    C$ERDF
6955  017536  000004                         .WORD   4
6956  017540  003161                         .WORD   ORADER
6957  017542  004734                         .WORD   R026ER
6958  017544                          3$:     ENDSEG
6959  017544                          10000$:
6960  017544  104405                         TRAP    C$ESEG
6961
6962  017546                                  ENDTST
6963  017546                          L10124:
6964  017546  104401                         TRAP    C$ETST
```

```
                                .SBTTL  TEST 34: OR ADDRESS REG TEST USING BINARY COUNT PATTERN

                                ;++
                                ; THIS TEST WILL CHECK THE OR ADDRESS REGISTER BITS ORAD 3:0 USING A BINARY
                                ; COUNT PATTERN.  THE DATA PATTERN WILL START AS ZERO AND BE INCREMENTED UNTIL
                                ; THE DATA PATTERN 17 HAS BEEN LOADED AND CHECKED.
                                ;--

017550                                  BGNTST
017550                          T34::
017550  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
017554  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNUSED BITS
017562  005037  002414                  CLR     R6LOAD                  ;SETUP INITIAL PATTERN TO 0

                                        ;CONTROL REGISTER 0 BITS CDAL 7:0 ARE CLEARED ON EXIT FROM ROUTINE
                                        ;"INITED". THE SIGNAL CDAL7 BEING CLEARED WILL ENABLE THE OUTPUTS
                                        ;OF THE OR ADDRESS REGISTER.

017566                          1$:     BGNSEG
017566  104404                          TRAP    C$BSEG

                                        ;SET THE SIGNAL PTER15 L IN THE POINTER REGISTER BY SETTING PDAL 3:0
                                        ;TO ALL ONES IN CONTROL REGISTER 2.

017570  004537  006376                  JSR     R5,ASSERT               ;GO ASSERT PTER15 L
017574  000017                          .WORD   PTER15

                                        ;WRITE, READ AND CHECK THE OR ADDRESS REGISTER WITH THE DATA PATTERN
                                        ;IN LOCATION "R6LOAD".  A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 6. A PULSE WILL
                                        ;BE ISSUED ON THE SIGNAL RPT15 H WHEN A READ COMMAND IS ISSUED TO
                                        ;CONTROL REGISTER 6.  THE SIGNAL WPT15 H WILL WRITE THE OR ADDRESS REG-
                                        ;ISTER AND THE SIGNAL RPT15 H WILL READ THE OR ADDRESS REGISTER.

017576  004737  006250          2$:     JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
017602  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
017604                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER NOT EQUAL EXPECTED
017604  104455                          TRAP    C$ERDF
017606  000004                          .WORD   4
017610  003161                          .WORD   ORADER
017612  004734                          .WORD   R026ER
017614                          3$:     ENDSEG
017614                          10000$:
017614  104405                          TRAP    C$ESEG

017616  005237  002414                  INC     R6LOAD                  ;INCREMENT THE DATA PATTERN BY 1
017622  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF DONE
017630  001756                          BEQ     1$                      ;IF NOT LOAD AND CHECK NEXT PATTERN
017632                                  ENDTST
017632                          L10125:
017632  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 35: OR ARRAY DATA TEST - ORO 7:0 (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK EACH LOCATION OF THE OR ARRAY RAM (ORO 7:0) WITH AN
                                ; ALTERNATING ONES AND ZEROES DATA PATTERN (252) AND AN ALTERNATING ZEROES AND
                                ; ONES DATA PATTERN (125).
                                ;
                                ; THE FOLLOWING SEQUENCE WILL BE REPEATED FOR EACH ADDRESS OF THE OR ARRAY RAM:
                                ;
                                ; THE TEST WILL CLEAR ALL THE LOW BITS IN CONTROL REGISTER 0 TO INITIALIZE
                                ; CONTROL REGISTER 0.  CDAL7 ON A ZERO WILL ENABLE THE OUTPUTS OF THE OR
                                ; ADDRESS REGISTER.  CDAL4 ON A ZERO WILL ALLOW ONLY ONE AND/OR ARRAY RAMS TO
                                ; BE SELECTED VIA THE POINTER REGISTER.  THE OR ARRAY RAMS WILL BE SELECTED IN
                                ; THIS TEST BY SETTING PTER15 L IN THE POINTER REGISTER WHICH WILL CAUSE THE
                                ; SIGNAL PLSL15 L TO BE ASSERTED.  THE SIGNAL PLSL15 L WILL ENABLE THE OR ARRAY
                                ; RAMS TO BE WRITTEN OR READ.  THE TEST WILL LOAD THE ADDRESS TO BE TESTED INTO
                                ; THE OR ADDRESS REGISTER.  TO LOAD THE ADDRESS, THE PROGRAM WILL ISSUE A WRITE
                                ; COMMAND TO CONTROL REGISTER 6.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REG-
                                ; ISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL
                                ; WPT15 H WHICH WILL LOAD THE OR ADDRESS REGISTER.  TO READ THE OR ADDRESS REGIS-
                                ; TER, THE TEST WILL ISSUE A READ COMMAND TO CONTROL REGISTER 6 WHICH WILL CAUSE
                                ; A PULSE ON THE SIGNAL RPT15 H.  THE SIGNAL RPT15 H WILL READ THE DATA FROM THE
                                ; OR ADDRESS REGISTER.  THE TEST WILL NOW WRITE AND READ THE OR ARRAY RAM LOCA-
                                ; TION WITH AN ALTERNATING ONES AND ZEROES DATA PATTERN (252).  TO WRITE THE
                                ; OR ARRAY RAM LOCATION, THE TEST WILL ISSUE A WRITE COMMAND TO CONTROL REGIS-
                                ; TER 4.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
                                ; PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPLA15 L. THE SIGNAL
                                ; WPLA15 L WILL WRITE THE DATA INTO THE OR ARRAY RAM LOCATION.  TO READ THE OR
                                ; ARRAY RAM LOCATION, THE TEST WILL ISSUE A READ COMMAND TO CONTROL REGISTER 4.
                                ; THE TEST WILL NOW LOAD, READ AND CHECK THE RAM LOCATION WITH AN ALTERNATING
                                ; ZEROS AND ONES DATA PATTERN (125).  THE TEST WILL THEN SEQUENCE TO THE NEXT
                                ; ADDRESS TO BE TESTED UNTIL ALL OR ARRAY RAM LOCATIONS HAVE BEEN CHECKED.
                                ;--

 017634                                 BGNTST
 017634                         T35::
 017634  004737  005474                 JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
 017640  005037  002414                 CLR     R6LOAD                  ;SETUP STARTING ADDRESS TO BE 0
 017644  012737  177760  002416         MOV     #177760,R6MASK          ;SETUP TO IGNORE UNUSED BITS

 017652                         1$:     BGNSEG
 017652  104404                         TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0. CDAL7 BEING A 0 WILL ENABLE
                                        ;THE OUTPUTS OF THE OR ADDRESS REGISTER.  CDAL4 BEING A ZERO WILL CAUSE
                                        ;ONLY ONE AND/OR ARRAY RAM TO BE SELECTED VIA THE POINTER REGISTER. IN
                                        ;THIS TEST PTER15 L WILL SELECT THE OR ARRAY RAMS.

 017654  105037  002370                 CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE
 017660  004737  006102                 JSR     PC,LDRD'C               ;GO LOAD, READ AND CEHCK REGISTER 0
 017664  001405                         BEQ     2$                      ;IF LOADED OK THEN CONTINUE
 017666                                 ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
 017666  104455                         TRAP    C$ERDF
 017670  000001                         .WORD   1
 017672  000000                         .WORD   0
 017674  004604                         .WORD   ROEROR
```

```
7073  017676                                  CKLOOP
7074  017676  104406                          TRAP    C$CLP1
7075
7076                                          ;SET THE SIGNAL PTER15 L IN THE POINTER REGISTER BY SETTING PDAL 3:0
7077                                          ;TO ALL ONES IN CONTROL REGISTER 2.
7078
7079  017700  004537  006376        2$:       JSR     R5,ASSERT               ;GO ASSERT PTER15
7080  017704  000017                          .WORD   PTER15
7081
7082                                          ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH THE CONTENTS OF LOCATION
7083                                          ;"R6LOAD".  ON A WRITE COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL
7084                                          ;PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH
7085                                          ;WILL LOAD THE ADDRESS INTO THE OR ADDRESS REGISTER.  ON A READ COMMAND
7086                                          ;TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A PULSE WILL
7087                                          ;BE ISSUED ON THE SIGNAL RPT15 H WHICH WILL READ THE DATA FROM THE OR
7088                                          ;ADDRESS REGISTER.
7089
7090  017706  004737  006250        3$:       JSR     PC,L.  R6               ;GO        EAD AND CHECK OR ADDRESS REG
7091  017712  001405                          BEQ     .$                      ;IF LO     K THEN CONTINUE
7092  017714                                  ERRDF   4,ORADER,RO26ER         ;OR ADD    . REG NOT EQUAL EXPECTED
7093  017714  104455                          TRAP    C$ERDF
7094  017716  000004                          .WORD   4
7095  017720  003161                          .WORD   ORADER
7096  017722  004734                          .WORD   RO26ER
7097  017724                                  CKLOOP
7098  017724  104406                          TRAP    C$CLP1
7099
7100                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
7101                                          ;REGISTER.  AN ALTERNATING ONES AND ZEROES DATA PATTERN (252) WILL BE
7102                                          ;WRITTEN INTO THE LOCATION.  THE OR ARRAY RAMS ARE ENABLED BY THE SIGNAL
7103                                          ;PLSL15 L. THE SIGNAL PLSL15 L IS GENERATED BY PTER15 L BEING ASSERTED
7104                                          ;IN THE POINTER REGISTER AND CDAL4 BEING SET TO A 0 IN CONTROL REGISTER
7105                                          ;0.  WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
7106                                          ;PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL WPLA15 L.  THE
7107                                          ;SIGNAL WPLA15 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE OR
7108                                          ;ARRAY LOCATION.  ON A READ COMMAND TO CONTROL REGISTER 4 DATA WILL
7109                                          ;BE READ FROM THE OR ARRAY RAM.
7110
7111  017726  012737  000252  002402  4$:     MOV     #25_,R4LOAD             ;SETUP ONES AND ZEROES PATTERN
7112  017734  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNUSED BITS
7113  017742  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
7114  017746  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
7115  017750                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
7116  017750  104455                          TRAP    C$ERDF
7117  017752  000003                          .WORD   3
7118  017754  003512                          .WORD   ORDATA
7119  017756  004720                          .WORD   R4EROR
7120  017760                                  CKLOOP
7121  017760  104406                          TRAP    C$CLP1
7122
```

```
7123
7124                                        ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
7125                                        ;REGISTER WITH AN ALTERNATING ZEROES AND ONES DATA PATTERN (125).
7126
7127  017762  012737  000125  002402  5$:   MOV     #125,R4LOAD             ;SETUP ZEROES AND ONES DATA PATTERN
7128  017770  004737  006202              JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
7129  017774  001404                      BEQ     6$                      ;IF DATA OK THEN CONTINUE
7130  017776                              ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORD 7:0
7131  017776  104455                      TRAP    C$ERDF
7132  020000  000003                      .WORD   3
7133  020002  003512                      .WORD   ORDATA
7134  020004  004720                      .WORD   R4EROR
7135  020006                      6$:     ENDSEG
7136  020006                      10000$:
7137  020006  104405                      TRAP    C$ESEG
7138
7139  020010  005237  002414              INC     R6LOAD                  ;UPDATE THE OR ADDRESS BY ONE
7140  020014  032737  000020  002414      BIT     #BIT4,R6LOAD            ;CHECK IF DONE ALL ADDRESSES
7141  020022  001713                      BEQ     1$                      ;IF NOT THEN LOAD NEXT ADDRESS
7142
7143  020024                              ENDTST
7144  020024                      10125$:
7145  020024  104401                      TRAP    C$ETST
7146
```

```
                                .SBTTL  TEST 36: OR ARRAY RAM ADDRESS/SHORT TEST (ORO 7:0)
                                ;**
                                ; THIS TEST WILL CHECK THAT ALL ADDRESSES IN THE OR ARRAY RAM CAN BE ADDRESSED
                                ; CORRECTLY AND THAT WRITING ONE ADDRESS WILL NOT WRITE ANOTHER ADDRESS PREVIOUSLY
                                ; WRITTEN (ADDRESS SHORT).  THE TEST WILL WRITE AND CHECK EACH LOCATION OF THE
                                ; OR ARRAY RAMS WITH DATA EQUAL TO ITS ADDRESS. THE DATA PATTERN FOR THE TOP 4
                                ; BITS OF THE OR ARRAY RAM WILL BE THE SAME AS THE LOW 4 BITS OF THE OR ARRAY
                                ; RAM.  AFTER WRITING ALL LOCATIONS OF THE OR ARRAY RAM, THE TEST WILL READ EACH
                                ; LOCATION OF THE OR ARRAY RAM CHECKING THE DATA TO BE EQUAL TO ITS ADDRESS. THE
                                ; TEST WILL THEN READ EACH LOCATION CHECKING THE DATA TO BE EQUAL TO ITS ADDRESS
                                ; AND THEN WRITING AND CHECKING THE LOCATION WITH DATA EQUAL TO THE 1'S COMPLE-
                                ; MENT OF ITS ADDRESS.  IF A LOCATION ON THE FIRST READ DOES NOT EQUAL ITS
                                ; ADDRESS, THEN WRITING A PREVIOUS LOCATION PROBABLY WRITE THE LOCATION IN ERROR
                                ; ALSO.  AFTER ALL LOCATIONS HAVE BEEN TESTED IN THIS MANNER, THE PROGRAM WILL
                                ; READ THE OR ARRAY RAMS AGAIN CHECKING EACH LOCATION TO CONTAIN AS DATA THE
                                ; ONES COMPLEMENT OF ITS ADDRESS.
                                ;--

020026                                  BGNTST
020026                          T36::
020026  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

020032                                  BGNSUB
020032                          T36.1:
020032  104402                          TRAP    C$BSUB

020034  005037  002414                  CLR     R6LOAD                  ;SETUP OR ADDRESS TO BE INITIALLY 0
020040  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNUSED BITS IN REG 6
020046  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNUSED BITS IN REG 4

020054                          1$:     BGNSEG
020054  104404                          TRAP    C$BSEG

                                ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.  CDAL4 ON A ZERO WILL ENABLE
                                ;ONLY ONE AND/OR ARRAY RAM TO BE SELECTED VIA THE POINTER REGISTER.  IN
                                ;THIS TEST, THE SIGNAL PTER15 L WILL SELECT THE OR ARRAY RAMS.  CDAL7 ON
                                ;A ZERO WILL ENABLE THE OUTPUTS OF THE OR ADDRESS REGISTER.

020056  105037  002370                  CLRB    ROLOAD                  ;SETUP TO CLEAR THE LOW BYTE
020062  004737  006102                  JSR     PC,LDRDRO               ;GO LOAD, READ AND CHECK REGISTER 0
020066  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
020070                                  ERRDF   1,,ROER...              ;REGISTER 0 NOT EQUAL EXPECTED
020070  104455                          TRAP    C$ERDF
020072  000001                          .WORD   1
020074  000000                          .WORD   0
020076  004604                          .WORD   ROEROR
020100                                  CKLOOP
020100  104406                          TRAP    C...P1

                                ;SET THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REGISTER 2

020102  004537  006376          2$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
020106  000017                          .WORD   PTER15

                                ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH THE CONTENTS OF LOCATION
```

```
7203                                                    ;'R6LOAD'.
7204
7205  020110  004737  006250          3$:     JSR     PC,LDRDR6               ;GO LOAD READ AND CHECK OR ADDRESS REG
7206  020114  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
7207  020116                                  ERRDF   4,ORADER,RO?6ER         ;OR ADDRESS REGISTER NOT EQUAL EXPECTED
7208  020116  104455                          TRAP    C$ERDF
7209  020120  000004                          .WORD   4
7210  020122  003161                          .WORD   ORADER
7211  020124  004734                          .WORD   RO26ER
7212  020126                                  CKLOOP
7213  020126  104406                          TRAP    C$CLP1
7214
7215                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION WITH DATA EQUAL TO THE
7216                                          ;ADDRESS BEING TESTED.  THE DATA FOR THE TOP 4 BITS WILL BE EQUAL TO
7217                                          ;THE DATA PATTERN OF THE LOW 4 BITS.
7218
7219  020130  013701  002414          4$:     MOV     R6LOAD,R1               ;GET THE ADDRESS BEING TESTED
7220  020134  006301                          ASL     R1                      ;MOVE ADDRESS TO TOP 4 BITS
7221  020136  006301                          ASL     R1                      ;
7222  020140  006301                          ASL     R1                      ;
7223  020142  006301                          ASL     R1
7224  020144  063701  002414                  ADD     R6LOAD,R1               ;ADD ADDRESS BACK INTO LOW 4 BITS
7225  020150  010137  002402                  MOV     R1,R4LOAD               ;SAVE THE DATA PATTERN
7226  020154  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD READ AND CHECK OR ARRAY RAM
7227  020160  001404                          BEQ     5$                      ;IF DATA LOADED OK THEN CONINUE
7228  020162                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR (ORO 7:0)
7229  020162  104455                          TRAP    C$ERDF
7230  020164  000003                          .WORD   3
7231  020166  003512                          .WORD   ORDATA
7232  020170  004720                          .WORD   R4EROR
7233  020172                          5$:     ENDSEG
7234  020172                          10000$:
7235  020172  104405                          TRAP    C$ESEG
7236
7237  020174  005237  002414                  INC     R6LOAD                  ;UPDATE THE OR ADDRESS TO NEXT ONE
7238  020200  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF ALL LOCATIONS HAVE BEEN TESTED
7239  020206  001722                          BEQ     1$                      ;IF NOT THEN DO NEXT LOCATION
7240  020210                                  ENDSUB
7241  020210                          L10130:
7242  020210  104403                          TRAP    C$ESUB
7243
7244                                          ;THE FOLLOWING SECTION OF CODE WILL READ EACH LOCATION OF THE OR ARRAY
7245                                          ;RAMS CHECKING THE LOCATIONS TO CONTAIN ITS ADDRESS AS DA A.
7246
7247  020212                                  BGNSUB
7248  020212                          T36.2:
7249  020212  104402                          TRAP    C$BSUB
7250
7251                                          ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER 0,
7252                                          ;AND THE SIGNAL PTER15 L WILL BE ASSERTED IN THE POINTER REGISTER VIA
7253                                          ;CONTROL REGISTER 2.
7254
7255  020214  005037  002414                  CLR     R6LOAD                  ;SETUP OR ADDRESS TO START AT 0
7256
7257  020220                          1$:     BGNSEG
7258  020220  104404                          TRAP    C$BSEG
```

```
7259
7260                                    ;LOAD,READ AND CHECK OR ADDRESS REGISTER WITH THE CONTENTS OF "R6LOAD"
7261
7262  020222  004737  006250            JSR     PC,LDRD26               ;GO LOAD, READ AND CHECK OR ADDRESS REG
7263  020226  001405                    BEQ     2$                      ;IF LOADED OK THEN CONTINUE
7264  020230                            ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL EXPECTED
7265  020230  104455                    TRAP    C$ERDF
7266  020232  000004                    .WORD   4
7267  020234  003161                    .WORD   ORADER
7268  020236  004734                    .WORD   R026ER
7269  020240                            CKLOOP
7270  020240  104406                    TRAP    C$CLP1
7271
7272                                    ;READ AND CHECK OR ARRAY RAM LOCATION TO CONTAIN AS DATA ITS OWN ADDRESS.
7273                                    ;THE DATA FOR THE TOP 4 BITS WILL BE THE SAME AS THE DATA FOR THE LOW
7274                                    ;4 BITS.
7275
7276  020242  013701  002414      2$:   MOV     R6LOAD,R1               ;GET THE ADDRESS BEING TESTED
7277  020246  006301                    ASL     R1                      ;PUT THE ADDRESS IN TOP 4 BITS
7278  020250  006301                    ASL     R1                      ;
7279  020252  006301                    ASL     R1                      ;
7280  020254  006301                    ASL     R1                      ;
7281  020256  063701  002414            ADD     R6LOAD,R1               ;ADD ADDRESS BACK INTO LOW 4 BITS
7282  020262  010137  002402            MOV     R1,R4LOAD               ;SAVE DATA PATTERN PREVIOUSLY LOADED
7283  020266  010137  002404            MOV     R1,R4GOOD               ;SETUP EXPECTED DATA
7284  020272  004737  006216            JSR     PC,R_ADR4               ;GO READ AND CHECK OR ARRAY DATA
7285  020276  001404                    BEQ     3$                      ;IF DATA OK THEN CONTINUE
7286  020300                            ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA NOT EQUAL TO ADDRESS
7287  020300  104455                    TRAP    C$ERDF
7288  020302  000003                    .WORD   3
7289  020304  003512                    .WORD   ORDATA
7290  020306  004720                    .WORD   R4EROR
7291  020310                      3$:   ENDSEG
7292  020310                      10000$:
7293  020310  104405                    TRAP    C$ESEG
7294
7295  020312  005037  002414            INC     R6LOAD                  ;UPDATE OR ADDRESS REGISTER ADDRESS
7296  020316  032737  000020  002414    BIT     #BIT4,R6LOAD            ;CHECK IF ALL ADDRESSES CHECKED
7297  020324  001735                    BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
7298  020326                            ENDSUB
7299  020326                      L10.71:
7300  020326  104403                    TRAP    C$ESUB
7301
7302                                    ;THE FOLLOWING SECTION OF CODE WILL READ EACH LOCATION OF THE OR ARRAY
7303                                    ;RAM CHECKING THE DATA TO EQUAL ITS ADDRESS AND THEN WRITING AND CHECK-
7304                                    ;ING THE LOCATION WITH DATA EQUAL TO THE ONES COMPLEMENT OF ITS ADDRESS.
7305
7306  020330                            BGNSUB
7307  020330                      T36.3:
7308  020330  10440c                    TRAP    C$BSUB
7309
7310                                    ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER 0.
7311                                    ;THE SIGNAL, PTER15 L, WILL BE ASSERTED IN THE POINTER REGISTER VIA
7312                                    ;CONTROL REGISTER 2.
7313
7314  020332  005037  002414            CLR     R6LOAD                  ;SETUP OR ADDRESS REG TO BE ADDRESS 0
```

```
7315
7316  020336                          1$:     BGNSEG
7317  020336  104404                          TRAP    C$BSEG
7318
7319                                          ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH THE CONTENTS OF LOCATION
7320                                          ;"R6LOAD".
7321
7322  020340  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
7323  020344  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
7324  020346                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER NOT EQUAL EXPECTED
7325  020346  104455                          TRAP    C$ERDF
7326  020350  000004                          .WORD   4
7327  020352  003161                          .WORD   ORADER
7328  020354  004734                          .WORD   R026ER
7329  020356                                  CKLOOP
7330  020356  104406                          TRAP    C$CLP1
7331
7332                                          ;READ AND CHECK OR ARRAY RAM LOCATION TO CONTAIN AS ITS DATA ITS OWN
7333                                          ;ADDRESS.  THE DATA IN THE TOP 4 BITS WILL BE THE SAME AS IN THE LOW
7334                                          ;4 BITS.
7335
7336  020360  013701  002414          2$:     MOV     R6LOAD,R1               ;GET THE OR ADDRESS REG ADDRESS
7337  020364  006301                          ASL     R1                      ;MOVE IT TO TOP 4 BITS
7338  020366  006301                          ASL     R1                      ;
7339  020370  006301                          ASL     R1                      ;
7340  020372  006301                          ASL     R1                      ;
7341  020374  063701  002414                  ADD     R6LOAD,R1               ;ADD ADDRESS INTO LOW 4 BITS
7342  020400  010137  002402                  MOV     R1,R4LOAD               ;SAVE THE DATA PREVIOUSLY LOADED
7343  020404  010137  002404                  MOV     R1,R4GOOD               ;SETUP EXPECTED DATA
7344  020410  004737  006216                  JSR     PC,READR4               ;GO READ AND CHECK OR ARRAY DATA
7345  020414  001405                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
7346  020416                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA NOT EQUAL ADDRESS
7347  020416  104455                          TRAP    C$ERDF
7348  020420  000003                          .WORD   3
7349  020422  003512                          .WORD   ORDATA
7350  020424  004720                          .WORD   R4EROR
7351  020426                                  CKLOOP
7352  020426  104406                          TRAP    C$CLP1
7353
7354                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION WITH THE ONES COMPLEMENT
7355                                          ;OF ITS ADDRESS. THE TOP 4 BITS WILL EQUAL THE LOW 4 BITS.
7356
7357  020430  005137  002402          3$:     COM     R4LOAD                  ;COMPLMENT THE DATA
7358  020434  042737  177400  002402          BIC     #177400,R4LOAD          ;CLEAR THE HIGH BYTE OF DATA
7359  020442  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY DATA
7360  020446  001404                          BEQ     4$                      ;IF DATA OK TH.  CONTINUE
7361  020450                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR 1'S COMP OF ADDRESS
7362  020450  104455                          TRAP    C$ERDF
7363  020452  000003                          .WORD   3
7364  020454  003512                          .WORD   ORDATA
7365  020456  004720                          .WORD   R4EROR
7366  020460                          4$:     ENDSEG
7367  020460                          10000$:
7368  020460  104405                          TRAP    C$ESEG
7369
7370  020462  005237  002414                  INC     R6LOAD                  ;UPDATE OR ADDRESS REGISTER ADDRESS
```

```
7371  020466  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF ALL LOCATIONS TESTED
7372  020474  001720                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
7373  020476                                  ENDSUB
7374  020476                          L10132:
7375  020476  104403                          TRAP    C$ESUB
7376
7377                                          ;THE FOLLOWING SECTION OF CODE WILL READ EACH LOCATION OF THE OR ARRAY
7378                                          ;RAMS CHECKING THE DATA TO BE THE ONES COMPLEMENT OF THE ADDRESS BEING
7379                                          ;TESTED.
7380
7381
7382  020500                                  BGNSUB
7383  020500                          T36.4:
7384  020500  104402                          TRAP    C$BSUB
7385
7386                                          ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER 0
7387                                          ;AND THE SIGNAL PTER15 L WILL BE ASSERTED IN THE POINTER REGISTER VIA
7388                                          ;CONTROL REGISTER 2.
7389
7390  020502  005037  002414                  CLR     R6LOAD                  ;SET OR ADDRESS TO START AT 0
7391
7392  020506                          1$:     BGNSEG
7393  020506  104404                          TRAP    C$BSEG
7394
7395                                          ;LOAD,READ AND CHECK OR ADDRESS REGISTER WITH CONTENTS OF "R6LOAD"
7396
7397  020510  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
7398  020514  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
7399  020516                                  ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REGISTER NOT EQUAL EXPECTED
7400  020516  104455                          TRAP    C$ERDF
7401  020520  000004                          .WORD   4
7402  020522  003161                          .WORD   ORADER
7403  020524  004734                          .WORD   RO26ER
7404  020526                                  CKLOOP
7405  020526  104406                          TRAP    C$CLP1
7406
7407                                          ;READ AND CHECK OR ARRAY RAM LOCATION TO CONTAIN AS ITS DATA THE ONES
7408                                          ;COMPLEMENT OF ITS ADDRESS. THE DATA IN THE TOP 4 BITS WILL BE THE
7409                                          ;SAME AS THE DATA IN THE LOW 4 BITS
7410
7411  020530  013701  002414          2$:     MOV     R6LOAD,R1               ;GET THE ADDRESS BEING TESTED
7412  020534  006301                          ASL     R1                      ;MOVE IT TO THE TOP 4 BITS
7413  020536  006301                          ASL     R1                      ;
7414  020540  006301                          ASL     R1                      ;
7415  020542  006301                          ASL     R1                      ;
7416  020544  063701  002414                  ADD     R6LOAD,R1               ;ADD THE ADDRESS BACK INTO LOW 4 BITS
7417  020550  005101                          COM     R1                      ;MAKE THE ONES COMPLEMENT
7418  020552  042701  177400                  BIC     #177400,R1              ;CLEAR UNUSED BITS
7419  020556  010137  002402                  MOV     R1,R4LOAD               ;SAVE THE DATA PREVIOUSLY LOADED
7420  020562  010137  002404                  MOV     R1,R4GOOD               ;SETUP EXPECTED DATA
7421  020566  004737  006216                  JSR     PC,READR4               ;GO READ AND CHECK OR ARRAY DATA
7422  020572  001404                          BEQ     3$                      ;IF DATA OK THEN CONTINUE
7423  020574                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA NOT EQUAL 1'S COMP OF ADDRESS
7424  020574  104455                          TRAP    C$ERDF
7425  020576  000003                          .WORD   3
7426  020600  003512                          .WORD   ORDATA
```

```
7427  020602  004720                        .WORD   R4EROR
7428  020604                        3$:     ENDSEG
7429  020604                        10000$:
7430  020604  104405                        TRAP    C$ESEG
7431
7432  020606  005237  002414                INC     R6LOAD                  ;UPDATE THE OR ADDRESS REGISTER ADDRESS
7433  020612  032737  000020  002414        BIT     #BIT4,R6LOAD            ;CHECK IF DONE
7434  020620  001732                        BEQ     1$                      ;IF NOT THEN CHECK NEXT ADDRESS
7435  020622                                ENDSUB
7436  020622                        L10133:
7437  020622  104403                        TRAP    C$ESUB
7438  020624                                ENDTST
7439  020624                        L10127:
7440  020624  104401                        TRAP    C$ETST
7441
```

```
7442                                    .SBTTL  TEST 37: AND ARRAY RAM TEST - PLSLO L (1'S + 0'S, 0'S + 1'S)
7443
7444                                    ;++
7445                                    ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
7446                                    ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
7447                                    ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
7448                                    ; SIGNAL PLSLO L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 3:0.
7449                                    ;--
7450
7451  020626                                    BGNTST
7452  020626                            T37::
7453  020626  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
7454  020632  005037  002414                   CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
7455  020636  012737  170377  002406           MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ
7456
7457  020644                            1$:     BGNSEG
7458  020644  104404                            TRAP    C$BSEG
7459
7460                                    ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.  CDAL4 OF A ZERO WILL
7461                                    ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
7462                                    ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
7463                                    ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
7464                                    ;BUFFERS (TRDI 59:0).
7465
7466  020646  105037  002370                   CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
7467  020652  004737  006102                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
7468  020656  001405                            BEQ     2$                      ;IF LOADED OK THEN CONTINUE
7469  020660                                    ERRDF   1,,R0ER0R               ;REGISTER 0 NOT EQUAL EXPECTED
7470  020660  104455                            TRAP    C$ERDF
7471  020662  000001                            .WORD   1
7472  020664  000000                            .WORD   0
7473  020666  004604                            .WORD   R0ER0R
7474  020670                                    CKLOOP
7475  020670  104406                            TRAP    C$CLP'
7476
7477                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH
7478                                    ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
7479                                    ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.
7480
7481  020672  004537  006426            2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 15:0
7482  020676  000005                            .WORD   PTER5                   ;SELECT TRDI BITS 15:0
7483
7484                                    ;SET PTER0 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
7485                                    ;A ZERO AND THE SIGNAL PTER0 L IS ASSERTED, THE SIGNAL PLSLO L WILL BE
7486                                    ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 3:0.
7487                                    ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
7488                                    ;REMAIN HIGH.
7489
7490  020700  004537  006376                   JSR     R5,ASSERT               ;GO ASSERT PTER0
7491  020704  000000                            .WORD   PTER0
7492
7493                                    ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSLO L.
7494                                    ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
7495                                    ;PTER0 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA0 L.  THE
7496                                    ;SIGNAL WPLA0 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
7497                                    ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
```

```
                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
                                                ;
                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSLO L WITH
                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
                                                ;
020706  012737  00001c  002402  3$:    MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
020714  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
020720  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
020722                              ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
020722  104455                      TRAP    C$ERDF
020724  000003                      .WORD   3
020726  003550                      .WORD   ANDERR
020730  004720                      .WORD   R4EROR
020732                              CKLOOP
020732  104406                      TRAP    C$CLP1
                                                ;
                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSLO L WITH
                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
                                                ;
020734  012737  000005  002402  4$:    MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
020742  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
020746  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
020750                              ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
020750  104455                      TRAP    C$ERDF
020752  000003                      .WORD   3
020754  003550                      .WORD   ANDERR
020756  004720                      .WORD   R4EROR
020760                          5$: ENDSEG
020760                          10000$:
020760  104405                      TRAP    C$ESEG
                                                ;
020762  005237  002414              INC     R6LOAD                  ;UPDATE AND ARRAY ADDRESS BY ONE
020766  032737  000020  002414      BIT     #BIT4,R6LOAD            ;CHECK IF ALL 16 ADDRESSES DONE
020774  001723                      BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
020776                              ENDTST
020776                      L10134:
020776  104401                      TRAP    C$ETST
```

```
                                        .SBTTL  TEST 38: AND ARRAY RAM TEST - PLSL1 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL1 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 7:4.
                                        ;--

021000                                          BGNTST
021000                                  T38::
021000  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021004  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021010  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021016                                  1$:     BGNSEG
021016  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

021020  105037  902370                  CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021024  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021030  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021032                                  ERRDF   1,,R0ERR0               ;REGISTER 0 NOT EQUAL EXPECTED
021032  104455                          TRAP    C$ERDF
021034  000001                          .WORD   1
021036  000000                          .WORD   0
021040  004604                          .WORD   R0ERR0
021042                                  CKLOOP
021042  104406                          TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021044  004537  006426          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 15:0
021050  000005                          .OPD    PTER5                   ;SELECT TRDI BITS 15:0

                                        ;SET PTER1 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER1 L IS ASSERTED, THE SIGNAL PLSL1 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 7:4.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

021052  004537  006376                  JSR     R5,ASSERT               ;GO ASSERT PTER1
021056  000001                          .WORD   PTER1

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL1 L.
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
                                        ;PTER1 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA1 L.  THE
                                        ;SIGNAL WPLA1 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
                                        ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
```

```
                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
                                                ;
                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL1 L WITH
                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
                                                ;
021060  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
021066  004737  006166              JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
021072  001405                      BEQ     4$                      ;IF DATA OK THEN CONTINUE
021074                              ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
021074  104455                      TRAP    C$ERDF
021076  000003                      .WORD   3
021100  003550                      .WORD   ANDERR
021102  004720                      .WORD   R4EROR
021104                              CKLOOP
021104  104406                      TRAP    C$CLP1
                                                ;
                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL1 L WITH
                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
                                                ;
021106  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
021114  004737  006166              JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
021120  001404                      BEQ     5$                      ;IF LOADED OK THEN CONTINUE
021122                              ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
021122  104455                      TRAP    C$ERDF
021124  000003                      .WORD   3
021126  003550                      .WORD   ANDERR
021130  004720                      .WORD   R4EROR
021132                      5$:     FNDSEG
021132                      10000$:
021132  104405                      TRAP    C$ESEG
                                                ;
021134  062737  000020  002414      ADD     #BIT4,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
021142  032737  000400  002414      BIT     #BIT8,R6LOAD            ;CHECK IF ALL 16 ADDRESSES DONE
021150  001722                      BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
021152                              ENDTST
021152                      L10135:
021152  104401                      TRAP    C$ETST
                                                ;
```

```
                                        .SBTTL  TEST 39: AND ARRAY RAM TEST - PLSL2 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL2 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 11:8.
                                        ;--

021154                                          BGNTST
021154                                  T39::
021154  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021160  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021164  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021172                                  1$:     BGNSEG
021172  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

021174  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021200  004737  006102                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021204  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021206                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021206  104455                                  TRAP    C$ERDF
021210  000001                                  .WORD   1
021212  000000                                  .WORD   0
021214  004604                                  .WORD   R0EROR
021216                                          CKLOOP
021216  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH
                                        ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021220  004537  006426                  2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 15:0
021224  000005                                  .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                        ;SET PTER2 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER2 L IS ASSERTED, THE SIGNAL PLSL2 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 11:8.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

021226  012737  000002  002376                  MOV     #PTER2,R2LOAD           ;SETUP BITS TO BE LOADED
021234  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
021240  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
021242                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
021242  104455                                  TRAP    C$ERDF
021244  000002                                  .WORD   2
021246  000000                                  .WORD   0
021250  004704                                  .WORD   R2EROR
```

```
7686  021252                                    CKLOOP
7687  021252  104406                            TRAP    C$CLP1
7688
7689                                            ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL2 L.
7690                                            ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
7691                                            ;PTER2 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA2 L.  THE
7692                                            ;SIGNAL WPLA2 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
7693                                            ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
7694                                            ;READ BACK FROM THE AND ARRAY RAM SELECTED.
7695
7696                                            ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL2 L WITH
7697                                            ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
7698
7699  021254  012737  000012  002402  3$:       MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
7700  021262  004737  006166                   JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
7701  021266  001405                            BEQ     4$                      ;IF DATA OK THEN CONTINUE
7702  021270                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
7703  021270  104455                            TRAP    C$ERDF
7704  021272  000003                            .WORD   3
7705  021274  003550                            .WORD   ANDERR
7706  021276  004720                            .WORD   R4EROR
7707  021300                                    CKLOOP
7708  021300  104406                            TRAP    C$CLP1
7709
7710                                            ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL2 L WITH
7711                                            ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
7712
7713  021302  012737  000005  002402  4$:       MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
7714  021310  004737  006166                   JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
7715  021314  001404                            BEQ     5$                      ;IF LOADED OK THEN CONTINUE
7716  021316                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
7717  021316  104455                            TRAP    C$ERDF
7718  021320  000003                            .WORD   3
7719  021322  003550                            .WORD   ANDERR
7720  021324  004720                            .WORD   R4EROR
7721  021326                            5$:     ENDSEG
7722  021326                            10000$:
7723  021326  104405                            TRAP     $ESEG
7724
7725  021330  062737  000400  002414            ADD     #BIT8,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
7726  021336  032737  010000  002414            BIT     #BIT12,R6LOAD           ;CHECK IF ALL 16 ADDRESSES DONE
7727  021344  001712                            BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
7728  021346                                    ENDTST
7729  021346                            L10136:
7730  021346  104401                            TRAP    C$ETST
7731
```

```
                                        .SBTTL  TEST 40: AND ARRAY RAM TEST - PLSL3 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL3 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 15:12.
                                        ;--

021350                                          BGNTST
021350                                  T40::
021350  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021354  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021360  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021366                                  1$:     BGNSEG
021366  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0..

021370  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021374  004737  006102                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021400  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021402                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021402  104455                                  TRAP    C$ERDF
021404  000001                                  .WORD   1
021406  000000                                  .WORD   0
021410  004604                                  .WORD   R0EROR
021412                                          CKLOOP
021412  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021414  004537  006426                  2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 15:0
021420  000005                                  .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                        ;SET PTER3 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER3 L IS ASSERTED, THE SIGNAL PLSL3 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 15:12.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS,  THE OUTPUTS WILL
                                        ;REMAIN HIGH.

021422  012737  000003  002376                  MOV     #PTER3,R2LOAD           ;SETUP BITS TO BE LOADED
021430  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
021434  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
021436                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
021436  104455                                  TRAP    C$ERDF
021440  000002                                  .WORD   2
021442  000000                                  .WORD   0
021444  004704                                  .WORD   R2EROR
```

```
7788  021446                                        CKLOOP
7789  021446  104406                                TRAP    C$CLP1
7790
7791                                                ;LOAD, READ AND CHECK AND ARRAY RAM S  ECTED BY THE SI NAL PLSL3 L.
7792                                                ;WHEN A WRITE COMMAND IS ISSUED TO CO  OL REGISTER 4 WITH THE SIGNAL
7793                                                ;PTER3 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA3 L.  THE
7794                                                ;SIGNAL WPLA3 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
7795                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
7796                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
7797
7798                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL3 L WITH
7799                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
7800
7801  021450  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
7802  021456  004737  006166                JSR     PC,LDRDAR               ;GO LOAD.READ AND CHECK AND ARRAY
7803  021462  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
7804  021464                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
7805  021464  104455                        TRAP    C$ERDF
7806  021466  000003                        .WORD   3
7807  021470  003550                        .WORD   ANDERR
7808  021472  004720                        .WORD   R4EROR
7809  021474                                CKLOOP
7810  021474  104406                        TRAP    C$CLP1
7811
7812                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL3 L WITH
7813                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
7814
7815  021476  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
7816  021504  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
7817  021510  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
7818  021512                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
7819  021512  104455                        TRAP    C$ERDF
7820  021514  000003                        .WORD   3
7821  021516  003550                        .WORD   ANDERR
7822  021520  004720                        .WORD   R4EROR
7823  021522                          5$.   ENDSEG
7824  021522                          100[illegible].$:
7825  021522  104405                        TRAP    C$ESEG
7826
7827  021524  062737  010000  002414        ADD     #BIT12,R6LOAD           ;UPDATE AND ARRAY ADDRESS BY ONE
7828  021532  001315                        BNE     1$                      ;IF NOT 0 THEN DO NEXT ADDRESS
7829  021534                                ENDTST
7830  021[illegible]                  L10137:
7831  021534  104401                        TRAP    C$ETST
7832
```

```
                                        .SBTTL  TEST 41: AND ARRAY RAM TEST - PLSL4 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL4 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 19:16.
                                        ;--

021536                                          BGNTST
021536                                  T41::
021536  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021542  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021546  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021554                                  1$:     BGNSEG
021554  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

021556  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021562  004737  006102                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021566  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021570                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021570  104455                                  TRAP    C$ERDF
021572  000001                                  .WORD   1
021574  000000                                  .WORD   0
021576  004604                                  .WORD   R0EROR
021600                                  CKLOOP
021600  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH
                                        ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021602  004537  006426          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 31:16
021606  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16

                                        ;SET PTER4 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER4 L IS ASSERTED, THE SIGNAL PLSL4 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 19:16.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

021610  012737  000004  002376                  MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
021616  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
021622  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
021624                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
021624  104455                                  TRAP    C$ERDF
021626  000002                                  .WORD   2
021630  000000                                  .WORD   0
021632  004736                                  .WORD   R2EROR
```

```
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL4 L.
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
                                        ;PTER4 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA4 L.  THE
                                        ;SIGNAL WPLA4 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
                                        ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
                                        ;READ BACK FROM THE AND ARRAY RAM SELECTED.

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL4 L WITH
                                        ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).

021636  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
021644  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
021650  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
021652                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
021652  104455                        TRAP    C$ERDF
021654  000003                        .WORD   3
021656  003550                        .WORD   ANDERR
021660  004720                        .WORD   R4EROR
021662                                CKLOOP
021662  104406                        TRAP    C$CLP1

                                        ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL4 L WITH
                                        ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).

021664  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
021672  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
021676  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
021700                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
021700  104455                        TRAP    C$ERDF
021702  000003                        .WORD   3
021704  003550                        .WORD   ANDERR
021706  004720                        .WORD   R4EROR
021710                          5$:   ENDSEG
021710                          10000$:
021710  104405                        TRAP    C$ESEG

021712  005237  002414                INC     R6LOAD                  ;UPDATE AND ARRAY ADDRESS BY ONE
021716  032737  000020  002414        BIT     #BIT4,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
021724  001713                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
021726                                ENDTST
021726                          L10140:
021726  104401                        TRAP    C$ETST
```

```
                                        .SBTTL  TEST 42: AND ARRAY RAM TEST - PLSL5 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL5 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 23:20.
                                        ;--

021730                                          BGNTST
021730                                  T42::
021730  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
021734  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
021740  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

021746                                  1$:     BGNSEG
021746  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSL0 L.
                                        ;THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

021750  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
021754  004737  006102                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
021760  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
021762                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
021762  104455                                  TRAP    C$ERDF
021764  00000'                                  .WORD
021766  000000                                  .WORD   0
021770  004604                                  .WORD   R0EROR
021772                                          CKLOOP
021772  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

021774  004537  006426          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 31:16
022000  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16

                                        ;SET PTER 5 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER5 L IS ASSERTED, THE SIGNAL PLSL5 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 23:20.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

022002  012737  000005  002376                  MOV     #PTER5,R2LOAD           ;SETUP BITS TO BE LOADED
022010  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
022014  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
022016                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
022016  104455                                  TRAP    C$ERDF
022020  000002                                  .WORD   2
022022  000000                                  .WORD   0
022024  004704                                  .WORD   R2EROR
```

```
7991  022026                                        CKLOOP
7992  022026  104406                                TRAP    C$CLP1
7993
7994                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL5 L.
7995                                                ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
7996                                                ;PTER5 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA5 L.  THE
7997                                                ;SIGNAL WPLA5 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
7998                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
7999                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8000
8001                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL5 L WITH
8002                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8003
8004  022030  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8005  022036  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8006  022042  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
8007  022044                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8008  022044  104455                        TRAP    C$ERDF
8009  022046  000003                        .WORD   3
8010  022050  003550                        .WORD   ANDERR
8011  022052  004720                        .WORD   R4EROR
8012  022054                                CKLOOP
8013  022054  104406                        TRAP    C$CLP1
8014
8015                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL5 L WITH
8016                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8017
8018  022056  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8019  022064  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8020  022070  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8021  022072                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8022  022072  104455                        TRAP    C$ERDF
8023  022074  000003                        .WORD   3
8024  022076  003550                        .WORD   ANDERR
8025  022100  004720                        .WORD   R4EROR
8026  022102                          5$:   ENDSEG
8027  022102                          10000$:
8028  022102  104405                        TRAP    C$ESEG
8029
8030  022104  062737  000020  002414        ADD     #BIT4,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8031  022112  032737  000400  002414        BIT     #BIT8,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8032  022120  001712                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8033  022122                                ENDTST
8034  022122                          L10141:
8035  022122  104401                        TRAP    C$ETST
8036
```

```
                                        .SBTTL  TEST 43: AND ARRAY RAM TEST - PLSL6 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL6 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 27:24.
                                        ;--

022124                                          BGNTST
022124                                  T43::
022124  004737  005474                          JSR     PC,INITE'               ;SELECT AND INITIALIZE STATE ANALYZER
022130  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
022134  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

022142                                  1$:     BGNSEG
022142  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.  CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

022144  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
022150  004737  006102                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
022154  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
022156                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
022156  104455                                  TRAP    C$ERDF
022160  000001                                  .WORD   1
022162  000000                                  .WORD   0
022164  004604                                  .WORD   R0EROR
022166                                          CKLOOP
022166  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

022170  004537  006426                  2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 31:16
022174  000006                                  .WORD   PTER6                   ;SELECT TRDI BITS 31:16

                                        ;SET PTER6 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER6 L IS ASSERTED, THE SIGNAL PLSL6 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 27:24.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH

022200  012737  000006  002376                  MOV     #PTER6,R2LOAD           ;SETUP BITS TO BE LOADED
022204  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
022210  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
022212                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
022212  104455                                  TRAP    C$ERDF
022214  000002                                  .WORD   2
022216  000000                                  .WORD   0
022220  004704                                  .WORD   R2EROR
```

```
8093  022222                                        CKLOOP
8094  022222  104406                                TRAP    C$CLP1
8095
8096                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL6 L.
8097                                                ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8098                                                ;PTER6 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA6 L.  THE
8099                                                ;SIGNAL WPLA6 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8100                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8101                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8102
8103                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL6 L WITH
8104                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8105
8106  022230  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8107  022236  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8108  022242  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
8109  022244                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8110  022244  104455                        TRAP    C$ERDF
8111  022246  000003                        .WORD   3
8112  022250  003550                        .WORD   ANDERR
8113  022252  004720                        .WORD   R4EROR
8114  022254                                CKLOOP
8115  022254  104406                        TRAP    C$CLP1
8116
8117                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL6 L WITH
8118                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8119
8120  022256  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8121  022264  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8122  022270  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8123  022272                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8124  022272  104455                        TRAP    C$ERDF
8125  022274  000003                        .WORD   3
8126  022276  003550                        .WORD   ANDERR
8127  022300  004720                        .WORD   R4EROR
8128  022302                          5$:   ENDSEG
8129  022302                          10000$:
8130  022302  104405                        TRAP    C$ESEG
8131
8132  022304  062737  000400  002414        ADD     #BIT8,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8133  022312  032737  010000  002414        BIT     #BIT12,R6LOAD           ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8134  022320  001712                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8135  022322                                ENDTST
8136  022322                          L10142:
8137  022322  104401                        TRAP    C$ETST
8138
```

```
                                        .SBTTL  TEST 44: AND ARRAY RAM TEST - PLSL7 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL7 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 31:28.
                                        ;--

022320                                          BGNTST
022320                                  T44::
022320  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
022324  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
022330  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

022336                                  1$:     BGNSEG
022336  104404                                  TRAP    C$BSEG

                                                ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                                ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                                ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                                ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                                ;BUFFERS (TRDI 59:0).

022340  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
022344  004737  006102                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
022350  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
022352                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
022352  104455                                  TRAP    C$ERDF
022354  000001                                  .WORD   1
022356  000000                                  .WORD   0
022360  004604                                  .WORD   R0EROR
022362                                          CKLOOP
022362  104406                                  TRAP    C$CLP1

                                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH
                                                ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                                ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

022364  004537  006426                  2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 31:16
022370  000006                                  .WORD   PTER6                   ;SELECT TRDI BITS 31:16

                                                ;SET PTER7 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                                ;A ZERO AND THE SIGNAL PTER7 L IS ASSERTED, THE SIGNAL PLSL7 L WILL BE
                                                ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 31:28.
                                                ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED.  THUS, THE OUTPUTS WILL
                                                ;REMAIN HIGH.

022372  012737  000007  002376                  MOV     #PTER7,R2LOAD           ;SETUP BITS TO BE LOADED
022400  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
022404  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
022406                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
022406  104455                                  TRAP    C$ERDF
022410  000002                                  .WORD   2
022412  000000                                  .WORD   0
022414  004704                                  .WORD   R2EROR
```

```
8195  022416                                        CKLOOP
8196  022416  104406                                TRAP    C$CLP1
8197
8198                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL7 L.
8199                                                ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8200                                                ;PTER7 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA7 L.  THE
8201                                                ;SIGNAL WPLA7 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8202                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8203                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8204
8205                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL7 L WITH
8206                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8207
8208  022420  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8209  022426  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8210  022432  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
8211  022434                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8212  022434  104455                        TRAP    C$ERDF
8213  022436  000003                        .WORD   3
8214  022440  003550                        .WORD   ANDERR
8215  022442  004720                        .WORD   R4EROR
8216  022444                                CKLOOP
8217  022444  104406                        TRAP    C$CLP1
8218
8219                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL7 L WITH
8220                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8221
8222  022446  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8223  022454  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8224  022460  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8225  022462                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8226  022462  104455                        TRAP    C$ERDF
8227  022464  000003                        .WORD   3
8228  022466  003550                        .WORD   ANDERR
8229  022470  004720                        .WORD   R4EROR
8230  022472                        5$:     ENDSEG
8231  022472                        10000$:
8232  022472  104405                        TRAP    C$ESEG
8233
8234  022474  062737  010000  002414        ADD     #BIT12,R6LOAD           ;UPDATE AND ARRAY ADDRESS BY ONE
8235  022502  001315                        BNE     1$                      ;IF NOT 0 THEN DO NEXT ADDRESS
8236  022504                                ENDTST
8237  022504                        L10143:
8238  022504  104401                        TRAP    C$ETST
8239
```

```
                                        .SBTTL  TEST 45: AND ARRAY RAM TEST - PLSL8 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL8 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 35:32.
                                        ;--

022506                                  BGNTST
022506                          T45::
022506  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
022512  005037  002414                  CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
022516  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

022524                          1$:     BGNSEG
022524  104404                          TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSL0 L.
                                        ;THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

022526  105037  002370                  CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
022532  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
022536  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
022540                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
022540  104455                          TRAP    C$ERDF
022542  000001                          .WORD   1
022544  000000                          .WORD   0
022546  004604                          .WORD   R0EROR
022550                                  CKLOOP
022550  104406                          TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 4 .32 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

022552  004537  006426          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 47:32
022556  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32

                                        ;SET PTER8 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER8 L IS ASSERTED, THE SIGNAL PLSL8 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 35:32.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

022560  012737  000010  002376          MOV     #PTER8,R2LOAD           ;SETUP BITS TO BE LOADED
022566  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
022572  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
022574                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
022574  104455                          TRAP    C$ERDF
022576  000002                          .WORD   2
022600  000000                          .WORD   0
022602  004704                          .WORD   R2EROR
```

```
8296  022604                                  CKLOOP
8297  022604  104406                          TRAP    C$C.P1
8298
8299                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL8 L.
8300                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8301                                          ;PTER8 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA8 L.  THE
8302                                          ;SIGNAL WPLA8 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8303                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8304                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8305
8306                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL8 L WITH
8307                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8308
8309  022606  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8310  022614  004737  006166                  JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8311  022620  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
8312  022622                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8313  022622  104455                          TRAP    C$ERDF
8314  022624  000003                          .WORD   3
8315  022626  003550                          .WORD   ANDERR
8316  022630  004720                          .WORD   R4EROR
8317  022632                                  CKLOOP
8318  022632  104406                          TRAP    C$CLP1
8319
8320                                          ;LOAD, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL8 L WITH
8321                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8322
8323  022634  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8324  022642  004737  006166                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8325  022646  001404                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8326  022650                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8327  022650  104455                          TRAP    C$ERDF
8328  022652  000003                          .WORD   3
8329  022654  003550                          .WORD   ANDERR
8330  022656  004720                          .WORD   R4EROR
8331  022660                          5$:     ENDSEG
8332  022660                          10000$:
8333  022660  104405                          TRAP    C$ESEG
8334
8335  022662  005237  002414                  INC     R6LOAD                  ;UPDATE AND ARRAY ADDRESS BY ONE
8336  022666  032737  000020  002414          BIT     #BIT4,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8337  022674  001713                          BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8338  022676                                  ENDTST
8339  022676                          L10144:
8340  022676  104401                          TRAP    C$ETST
8341
```

```
                                        .SBTTL  TEST 46: AND ARRAY RAM TEST - PLSL9 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL9 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 39:36.
                                        ;--

022700                                          BGNTST
022700                                  T46::
022700  004737  005474                         JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
022704  005037  002414                         CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
022710  012737  170377  002406                 MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

022716                                  1$:     BGNSEG
022716  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSL0 L.
                                        ;THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

022720  105037  002370                         CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
022724  004737  006102                         JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
022730  001405                                 BEQ     2$                      ;IF LOADED OK THEN CONTINUE
022732                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
022732  104455                                  TRAP    C$ERDF
022734  000001                                  .WORD   1
022736  000000                                  .WORD   0
022740  004604                                  .WORD   R0EROR
022742                                          CKLOOP
022742  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

022744  004537  006426          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 47:32
022750  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32

                                        ;SET PTER9 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER9 L IS ASSERTED, THE SIGNAL PLSL9 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 39:36.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

022752  012737  000011  002376                 MOV     #PTER9,R2LOAD           ;SETUP BITS TO BE LOADED
022760  004737  006134                         JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
022764  001405                                 BEQ     3$                      ;IF LOADED OK THEN CONTINUE
022766                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
022766  104455                                  TRAP    C$ERDF
022770  000002                                  .WORD   2
022772  000000                                  .WORD   0
022774  004704                                  .WORD   R2EROR
```

```
8398  022776                                        CKLOOP
8399  022776  104406                                TRAP    C$CLP1
8400
8401                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL9 L.
8402                                                ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8403                                                ;PTER9 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA9 L.  THE
8404                                                ;SIGNAL WPLA9 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8405                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8406                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8407
8408                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL9 L WITH
8409                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8410
8411  023000  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8412  023006  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8413  023012  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
8414  023014                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8415  023014  104455                        TRAP    C$ERDF
8416  023016  000003                        .WORD   3
8417  023020  003550                        .WORD   ANDERR
8418  023022  004720                        .WORD   R4EROR
8419  023024                                CKLOOP
8420  023024  104406                        TRAP    C$CLP1
8421
8422                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL9 L WITH
8423                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8424
8425  023026  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8426  023034  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8427  023040  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8428  023042                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8429  023042  104455                        TRAP    C$ERDF
8430  023044  000003                        .WORD   3
8431  023046  003550                        .WORD   ANDERR
8432  023050  004720                        .WORD   R4EROR
8433  023052                          5$:   ENDSEG
8434  023052                          10000$:
8435  023052  104405                        TRAP    C$ESEG
8436
8437  023054  062737  000020  002414        ADD     #BIT4,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8438  023062  032737  000400  002414        BIT     #BIT8,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8439  023070  001712                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8440  023072                                ENDTST
8441  023072                          [illegible] :
8442  023072  104401                        TRAP    C$ETST
8443
```

```
                                        .SBTTL  TEST 47: AND ARRAY RAM TEST - PLSL10 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL10 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 43:40.
                                        ;--

023074                                          BGNTST
023074                                  T47::
023074  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
023100  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
023104  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

023112                                  1$:     BGNSEG
023112  104404                                  TRAP    C$BSEG

                                                ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                                ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                                ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                                ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                                ;BUFFERS (TRDI 59:0).

023114  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
023120  004737  006102                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
023124  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
023126                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
023126  104455                                  TRAP    C$ERDF
023130  000001                                  .WORD   1
023132  000000                                  .WORD   0
023134  004604                                  .WORD   R0EROR
023136                                          CKLOOP
023136  104406                                  TRAP    C$CLP1

                                                ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH
                                                ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                                ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

023140  004537  006426          2$:             JSR     R5,TRDIRF               ;LOAD,READ,CHECK TRAM DATA IN BUF 47:32
023144  000007                                  .WORD   PTER7                   ;SELECT TRDI BITS 47:32

                                                ;SET PTER10 L IN CONTROL REGISTER C.  WHEN THE SIGNAL CDAL4 IS SET TO
                                                ;A ZERO AND THE SIGNAL PTER10 L IS ASSERTED, THE SIGNAL PLSL10 L WILL BE
                                                ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 43:40.
                                                ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                                ;REMAIN HIGH.

023146  012737  000012  002376                  MOV     #PTER10,R2LOAD          ;SETUP BITS TO BE LOADED
023154  004737  006434                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
023160  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
023162                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
023162  104455                                  TRAP    C$ERDF
023164  000002                                  .WORD   2
023166  000000                                  .WORD   0
023170  004704                                  .WORD   R2EROR
```

```
                                        CKLOOP
                                        TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL10 L.
                                        ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
                                        ;PTER10 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA10 L.  THE
                                        ;SIGNAL WPLA10 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
                                        ;ARRAY RAM  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
                                        ;READ BACK FROM THE AND ARRAY RAM SELECTED.

                                        ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL10 L WITH
                                        ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).

023174  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
023202  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
023206  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
023210                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
023210  104455                        TRAP    C$ERDF
023212  000003                        .WORD   3
023214  003550                        .WORD   ANDERR
023216  004720                        .WORD   R4EROR
023220                                CKLOOP
023220  104406                        TRAP    C$CLP1

                                        ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL10 L WITH
                                        ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).

023222  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
023230  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
023234  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
023236                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
023236  104455                        TRAP    C$ERDF
023240  000003                        .WORD   3
023242  003550                        .WORD   ANDERR
023244  004720                        .WORD   R4EROR
023246                          5$:   ENDSEG
023246                          10000C$:
023246  104405                        TRAP    C$ESEG

023250  062737  000400  002414        ADD     #BIT8,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
023256  032737  010000  002414        BIT     #BIT12,R6LOAD           ;CHECK IF ALL AND ARRAY ADDRESSES DONE
023264  001712                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
023266                                ENDTST
023266                          L10146:
023266  104401                        TRAP    C$ETST
```

```
8546                                    .SBTTL  TEST 48: AND ARRAY RAM TEST - PLSL11 L (1'S + 0'S, 0'S + 1'S)
8547
8548                                    ;++
8549                                    ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
8550                                    ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
8551                                    ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
8552                                    ; SIGNAL PLSL11 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 47:44.
8553                                    ;--
8554
8555  023270                                    BGNTST
8556  023270                            T48::
8557  023270  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
8558  023274  005037  002414                   CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
8559  023300  012737  170377  002406           MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ
8560
8561  023306                            1$:     BGNSEG
8562  023306  104404                           TRAP    C$BSEG
8563
8564                                    ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.  CDAL4 ON A ZERO WILL
8565                                    ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
8566                                    ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
8567                                    ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
8568                                    ;BUFFERS (TRDI 59:0).
8569
8570  023310  105037  002370                   CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
8571  023314  004737  006102                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
8572  023320  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
8573  023322                                    ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
8574  023322  104455                           TRAP    C$ERDF
8575  023324  000001                           .WORD   1
8576  023326  000000                           .WORD   0
8577  023330  004604                           .WORD   R0EROR
8578  023332                                    CKLOOP
8579  023332  104406                           TRAP    C$CLP1
8580
8581                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH
8582                                    ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
8583                                    ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.
8584
8585  023334  004537  006426           2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 47:32
8586  023340  000007                           .WORD   PTER7                   ;SELECT TRDI BITS 47:32
8587
8588                                    ;SET PTER11 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
8589                                    ;A ZERO AND THE SIGNAL PTER11 L IS ASSERTED, THE SIGNAL PLSL11 L WILL BE
8590                                    ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 47:44.
8591                                    ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
8592                                    ;REMAIN HIGH.
8593
8594  023342  012737  0 ,013  002376           MOV     #PTER11,R2LOAD          ;SETUP BITS TO BE LOADED
8595  023350  004737  006134                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
8596  023354  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
8597  023356                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
8598  023356  104455                           TRAP    C$ERDF
8599  023360  000002                           .WORD   2
8600  023362  000000                           .WORD   0
8601  023364  004704                           .WORD   R2EROR
```

```
8602  023366                                  CKLOOP
8603  023366  104406                          TRAP    C$CLP1
8604
8605                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL11 L.
8606                                          ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8607                                          ;PTER11 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA11 L.  THE
8608                                          ;SIGNAL WPLA11 L WILL WRITE THE DATA ON THE WRITE COMMAND I TO THE AND
8609                                          ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8610                                          ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8611
8612                                          ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL11 L WITH
8613                                          ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8614
8615  023370  012737  000012  002402  3$:     MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8616  023376  004737  006166                 JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8617  023402  001405                         BEQ     4$                      ;IF DATA OK THEN CONTINUE
8618  023404                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8619  023404  104455                          TRAP    C$ERDF
8620  023406  000003                          .WORD   3
8621  023410  003550                          .WORD   ANDERR
8622  023412  004720                          .WORD   R4EROR
8623  023414                                  CKLOOP
8624  023414  104406                          TRAP    C$CLP1
8625
8626                                          ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL11 L WITH
8627                                          ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8628
8629  023416  012737  000005  002402  4$:     MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8630  023424  004737  006166                 JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8631  023430  001404                         BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8632  023432                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8633  023432  104455                          TRAP    C$ERDF
8634  023434  000003                          .WORD   3
8635  023436  003550                          .WORD   ANDERR
8636  023440  004720                          .WORD   R4EROR
8637  023442                          5$:     ENDSEG
8638  023442                          10000$:
8639  023442  104405                          TRAP    C$ESEG
8640
8641  023444  062737  010000  002414          ADD     #BIT12,R6LOAD           ;UPDATE AND ARRAY ADDRESS BY ONE
8642  023452  001315                         BNE     1$                      ;IF NOT 0 THEN DO NEXT ADDRESS
8643  023454                                  ENDTST
8644  023454                          L10147:
8645  023454  104401                          TRAP    C$ETST
8646
```

```
                                        .SBTTL  TEST 49: AND ARRAY RAM TEST - PLSL12 L (1'S + 0'S, 0'S + 1'S)

                                        ;++
                                        ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                        ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                        ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                        ; SIGNAL PLSL12 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 51:48.
                                        ;--

023456                                          BGNTST
023456                                  T49::
023456  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
023462  005037  002414                          CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
023466  012737  170377  002406                  MOV     #170377,R.MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

023474                                  1$:     BGNSEG
023474  104404                                  TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.  CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L.
                                        ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

023476  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
023502  004737  006702                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
023506  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
023510                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
023510  104455                                  TRAP    C$ERDF
023512  000001                                  .WORD   1
023514  000000                                  .WORD   0
023516  006604                                  .WORD   R0EROR
023520                                          CKLOOP
023520  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 59:48 WITH
                                        ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

023522  004537  006426                  2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 59:48
023526  000010                                  .WORD   PTER8                   ;SELECT TRDI BITS 59:48

                                        ;SET PTER12 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER12 L IS ASSERTED, THE SIGNAL PLSL12 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 51:48.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

023530  012737  000014  002376                  MOV     #PTER12,R2LOAD          ;SETUP BITS TO BE LOADED
023536  004737  006134                          JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
023542  001405                                  BEQ     3$                      ;IF LOADED OK THEN CONTINUE
023544                                          ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
023544  104455                                  TRAP    C$ERDF
023546  000002                                  .WORD   2
023550  000000                                  .WORD   0
023552  004704                                  .WORD   R2EROR
```

```
8703  023554                                        CKLOOP
8704  023554  104406                                TRAP    C$CLP1
8705
8706                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL12 L.
8707                                                ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8708                                                ;PTER12 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA12 L.  THE
8709                                                ;SIGNAL WPLA12 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8710                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8711                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8712
8713                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL12 L WITH
8714                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8715
8716  023556  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8717  023564  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8718  023570  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
8719  023572                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8720  023572  104455                        TRAP    C$ERDF
8721  023574  000003                        .WORD   3
8722  023576  003550                        .WORD   ANDERR
8723  023600  004720                        .WORD   R4EROR
8724  023602                                CKLOOP
8725  023602  104406                        TRAP    C$CLP1
8726
8727                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL12 L WITH
8728                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8729
8730  023604  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8731  023612  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8732  023616  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8733  023620                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8734  023620  104455                        TRAP    C$ERDF
8735  023622  000003                        .WORD   3
8736  023624  003550                        .WORD   ANDERR
8737  023626  004720                        .WORD   R4EROR
8738  023630                          5$:   ENDSEG
8739  023630                          10000$:
8740  023630  104405                        TRAP    C$ESEG
8741
8742  023632  005237  002414                INC     R6LOAD                  ;UPDATE AND ARRAY ADDRESS BY ONE
8743  023636  032737  000020  002414        BIT     #BIT4,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8744  023644  001713                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8745  023646                                ENDTST
8746  023646                          L10150:
8747  023646  104401                        TRAP    C$ETST
8748
```

```
8749                                    .SBTTL  TEST 50: AND ARRAY RAM TEST - PLSL13 L (1'S + 0'S, 0'S + 1'S)
8750
8751                                    ;++
8752                                    ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
8753                                    ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
8754                                    ; PATTERN (05).  THE AND APRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
8755                                    ; SIGNAL PLSL13 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 55:52.
8756                                    ;--
8757
8758  023650                                    BGNTST
8759  023650                            T50::
8760  023650  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
8761  023654  005037  002414                   CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
8762  023660  012737  170377  002406           MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ
8763
8764  023666                            1$:     BGNSEG
8765  023666  104404                           TRAP    C$BSEG
8766
8767                                          ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.  CDAL4 ON A ZERO WILL
8768                                          ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
8769                                          ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L
8770                                          ;THE SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
8771                                          ;BUFFERS (TRDI 59:0).
8772
8773  023670  105037  002370                   CLRB    R6LOAD                  ;SETUP BITS TO BE LOADED
8774  023674  004737  006102                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
8775  023700  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
8776  023702                                    ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
8777  023702  104455                           TRAP    C$ERDF
8778  023704  000001                           .WORD   1
8779  023706  000000                           .WORD   0
8780  023710  004604                           .WORD   R0EROR
8781  023712                                    CKLOOP
8782  023712  104406                           TRAP    C$CLP1
8783
8784                                          ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 59:48 WITH
8785                                          ;THE DATA STORED IN LOCATION "R6LOAD".  THE OUTPUTS OF THE TRACE RAM
8786                                          ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.
8787
8788  023714  004537  006426           2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 59:48
8789  023720  000010                           .WORD   PTER8                   ;SELECT TRDI BITS 59:48
8790
8791                                          ;SET PTER13 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
8792                                          ;A ZERO AND THE SIGNAL PTER13 L IS ASSERTED, THE SIGNAL PLSL13 L WILL BE
8793                                          ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 55:52.
8794                                          ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED, THUS, THE OUTPUTS WILL
8795                                          ;REMAIN HIGH.
8796
8797  023722  012737  000015  002376           MOV     #PTER13,R2LOAD          ;SETUP BITS TO BE LOADED
8798  023730  004737  006134                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
8799  023734  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
8800  023736                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
8801  023736  104455                           TRAP    C$ERDF
8802  023740  000002                           .WORD   2
8803  023742  000000                           .WORD   0
8804  023744  004704                           .WORD   R2EROR
```

```
8805  023746                                        CKLOOP
8806  023746  104406                                TRAP    C$CLP1
8807
8808                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL13 L.
8809                                                ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8810                                                ;PTER13 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA13 L.  THE
8811                                                ;SIGNAL WPLA13 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8812                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8813                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8814
8815                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL13 L WITH
8816  .                                             ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8817
8818  023750  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA  O BE LOADED
8819  023756  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8820  023762  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
8821  023764                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8822  023764  104455                        TRAP    C$ERDF
8823  023766  000003                        .WORD   3
8824  023770  003550                        .WORD   ANDERR
8825  023772  004720                        .WORD   R4EROR
8826  023774                                CKLOOP
8827  023774  104406                        TRAP    C$CLP1
8828
8829                                                ;WRITE, READ AND CHECK AND ARRAY SE E  D BY THE SIGNAL PLSL13 L WITH
8830                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8831
8832  023776  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8833  024004  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8834  024010  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8835  024012                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8836  024012  104455                        TRAP    C$ERDF
8837  024014  000003                        .WORD   3
8838  024016  003550                        .WORD   ANDERR
8839  024020  004720                        .WORD   R4EROR
8840  024022                          5$:   ENDSEG
8841  024022                          00005$.
8842  024022  104405                        TRAP    C$ESEG
8843
8844  024024  062737  000020  002414        ADD     #BIT4,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8845  024032  032737  000400  002414        BIT     #BIT8,R6LOAD            ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8846  024040  001712                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8847  024042                                ENDTST
8848  024042                          L0151.
8849  024042  104401                        TRAP    C$ETST
8850
```

```
                                .SBTTL  TEST 51: AND ARRAY RAM TEST - PLSL14 L (1'S + 0'S, 0'S + 1'S)

                                ;++
                                ; THIS TEST WILL CHECK EACH LOCATION OF THE AND ARRAY RAM WITH AN ALTERNATING
                                ; ONES AND ZEROES DATA PATTERN (12) AND AN ALTERNATING ZEROES AND ONES DATA
                                ; PATTERN (05).  THE AND ARRAY RAM BEING TESTED IS THE ONE SELECTED BY THE
                                ; SIGNAL PLSL14 L AND ADDRESSED BY TRACE RAM DATA IN BUFFER BITS TRDI 59:56.
                                ;--

                                        BGNTST
                                T51::
024044  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
024050  005037  002414                  CLR     R6LOAD                  ;START TRAM DATA IN BUF DATA = 0
024054  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO IGNORE UNUSED BITS ON AND READ

024062                          1$:     BGNSEG
024062  104404                          TRAP    C$BSEG

                                        ;CLEAR THE LOW BYTE OF CONTROL REGISTER 0.   CDAL4 ON A ZERO WILL
                                        ;ALLOW ONLY ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER
                                        ;REGISTER.  CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSL0 L.
                                        ;THE SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN
                                        ;BUFFERS (TRDI 59:0).

024064  105037  002370                  CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
024070  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
024074  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
024076                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
024076  104455                          TRAP    C$ERDF
024100  000001                          .WORD   1
024102  000000                          .WORD   0
024104  004604                          .WORD   R0EROR
024106                                  CKLOOP
024106  104406                          TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 59:48 WITH
                                        ;THE DATA STORED IN LOCATION 'R6LOAD'.  THE OUTPUTS OF THE TRACE RAM
                                        ;DATA IN BUFFERS ARE USED TO ADDRESS THE AND ARRAY RAMS.

024110  004537  006426          2$:     JSR     R5,TRDIBF               ;LOAD,READ,CHECK TRAM DATA IN BUF 59:48
024114  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48

                                        ;SET PTER14 L IN CONTROL REGISTER 0.  WHEN THE SIGNAL CDAL4 IS SET TO
                                        ;A ZERO AND THE SIGNAL PTER14 L IS ASSERTED, THE SIGNAL PLSL14 L WILL BE
                                        ;ASSERTED WHICH WILL SELECT THE AND ARRAY RAM ADDRESSED BY TRDI BITS 59:56.
                                        ;ALL THE OTHER AND ARRAY RAMS ARE DESELECTED    US, THE OUTPUTS WILL
                                        ;REMAIN HIGH.

024116  012737  000016  002376          MOV     #PTER14,R2LOAD          ;SETUP BITS TO BE LOADED
024124  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
024130  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
024132                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
024132  104455                          TRAP    C$ERDF
024134  000002                          .WORD   2
024136  000000                          .WORD   0
024140  004704                          .WORD   R2EROR
```

```
8907  024142                                        CKLOOP
8908  024142  104406                                TRAP    C$CLP?
8909
8910                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL14 L.
8911                                                ;WHEN A WRITE COMMAND IS ISSUED TO CONTROL REGISTER 4 WITH THE SIGNAL
8912                                                ;PTER14 L ASSERTED, A PULSE WILL OCCUR ON THE SIGNAL WPLA14 L.  THE
8913                                                ;SIGNAL WPLA14 L WILL WRITE THE DATA ON THE WRITE COMMAND INTO THE AND
8914                                                ;ARRAY RAM.  ON A READ COMMAND TO CONTROL REGISTER 4, THE DATA WILL BE
8915                                                ;READ BACK FROM THE AND ARRAY RAM SELECTED.
8916
8917                                                ;LOAD, READ AND CHECK AND ARRAY RAM SELECTED BY THE SIGNAL PLSL14 L WITH
8918                                                ;AN ALTERNATING ONES AND ZEROES DATA PATTERN (12).
8919
8920  024144  012737  000012  002402  3$:   MOV     #12,R4LOAD              ;SETUP DATA TO BE LOADED
8921  024152  004737  006166                JSR     PC,LDRDAR               ;GO LOAD,READ AND CHECK AND ARRAY
8922  024156  001405                        BEQ     4$                      ;IF DATA OK THEN CONTINUE
8923  024160                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 12
8924  024160  104455                        TRAP    C$ERDF
8925  024162  000003                        .WORD   3
8926  024164  003550                        .WORD   ANDERR
8927  024166  004720                        .WORD   R4EROR
8928  024170                                CKLOOP
8929  024170  104406                        TRAP    C$CLP1
8930
8931                                                ;WRITE, READ AND CHECK AND ARRAY SELECTED BY THE SIGNAL PLSL14 L WITH
8932                                                ;AN ALTERNATING ZEROES AND ONES DATA PATTERN (05).
8933
8934  024172  012737  000005  002402  4$:   MOV     #5,R4LOAD               ;SETUP DATA TO BE LOADED
8935  024200  004737  006166                JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
8936  024204  001404                        BEQ     5$                      ;IF LOADED OK THEN CONTINUE
8937  024206                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL 05
8938  024206  104455                        TRAP    C$ERDF
8939  024210  000003                        .WORD   3
8940  024212  003550                        .WORD   ANDERR
8941  024214  004720                        .WORD   R4EROR
8942  024216                          5$:   ENDSEG
8943  024216                          10000$:
8944  024216  104405                        TRAP    C$ESEG
8945
8946  024220  062737  000400  002414        ADD     #BIT8,R6LOAD            ;UPDATE AND ARRAY ADDRESS BY ONE
8947  024226  032737  010000  002414        BIT     #BIT12,R6LOAD           ;CHECK IF ALL AND ARRAY ADDRESSES DONE
8948  024234  001712                        BEQ     1$                      ;IF NOT THEN DO NEXT ADDRESS
8949  024236                                ENDTST
8950  024236                          L10152:
8951  024236  104401                        TRAP    C$ETST
8952
```

```
8953                                    .SBTTL  TEST 52: AND ARRAY SELECTION TEST
8954
8955                                    ;++
8956                                    ; THIS TEST WILL CHECK THAT EACH AND ARRAY IS ACTUALLY SELECTED WHEN ADDRESSED
8957                                    ; BY THE PLSL SELECT LINE SIGNALS.  THE PLSL SELECT SIGNALS ARE GENERATED BY
8958                                    ; THE POINTER REGISTER PTER SIGNALS VIA CONTROL REGISTER 2.  THE TEST WILL
8959                                    ; CLEAR ALL TRACE RAM DATA IN BUFFER BITS TRDI 59:0.  WITH ALL THESE BITS
8960                                    ; BEING CLEARED, LOCATION 0 OF EACH AND ARRAY WILL BE ADDRESSED.  THE TEST WILL
8961                                    ; THEN SELECT EACH AND ARRAY BY LOADING THE APPROPRIATE PTER SIGNAL IN CONTROL
8962                                    ; REGISTER 2.  THE TEST WILL THEN LOAD, READ AND CHECK THE AND ARRAY WITH THE
8963                                    ; PTER SIGNAL USED TO SELECT THE AND ARRAY.  ONCE EACH AND ARRAY HAS BEEN
8964                                    ; LOADED AND CHECKED, THE TEST WILL THEN RESELECT EACH AND ARRAY CHECKING THE
8965                                    ; DATA TO BE EQUAL TO THE PTER SELECT SIGNAL.  IF ANY ERRORS OCCUR IN THE LAST
8966                                    ; PORTION OF THE TEST, THEN THE ERROR IS PROBABLY RELATED TO THE PLSL SIGNALS
8967                                    ; OR THE POINTER REGISTER PTER SIGNALS.  ONLY ONE SIGNAL SHOULD BE ENABLED AT
8968                                    ; A TIME.
8969                                    ;--
8970
8971  024240                                    BGNTST
8972  024240                            T52::
8973  024240  004737  005474                    JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
8974  024244  005037  002414                    CLR     R6LOAD                  ;DATA TO BE LOADED INTO TRAM DATA IN BUF
8975  024250  012737  170377  002406            MOV     #170377,R4MASK          ;SETUP TO LOOK AT AND ARRY BITS ONLY
8976
8977  024256                                    BGNSUB
8978  024256                            T52.1:
8979  024256  104402                            TRAP    C$BSUB
8980
8981                                    ;CLEAR CDAL4 IN CONTROL REGISTER 0. CDAL4 ON A ZERO WILL ALLOW ONLY
8982                                    ;ONE AND/OR ARRAY TO BE ENABLED AT A TIME VIA THE POINTER REGISTER.
8983                                    ;CDAL3 AND CDAL2 ON A ZERO WILL ASSERT THE SIGNAL TRSLO L WHICH WILL
8984                                    ;ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS.
8985
8986  024260  005037  002370                    CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
8987  024264  004737  006102                    JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
8988  024270  001405                            BEQ     1$                      ;IF LOADED OK THEN CONTINUE
8989  024272                                    ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
8990  024272  104455                            TRAP    C$ERDF
8991  024274  000001                            .WORD   1
8992  024276  000000                            .WORD   0
8993  024300  004604                            .WORD   R0EROR
8994  024302                                    CKLOOP
8995  024302  104406                            TRAP    C$CLP1
8996
8997                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 15:0 WITH A
8998                                    ;DATA PATTERN OF 0
8999
9000  024304  004537  006426            1$:     JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
9001  024310  000005                            .WORD   PTER5                   ;SELECT TRDI BITS 15:0
9002
9003                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 31:16 WITH A
9004                                    ;DATA PATTERN OF 0
9005
9006  024312  004537  006426                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
9007  024316  000006                            .WORD   PTER6                   ;SELECT TRDI BITS 31:16
9008
```

```
9009                                            ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 47:32 WITH A
9010                                            ;DATA PATTERN OF 0.
9011
9012  024320  004537  006426                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
9013  024324  000007                            .WORD   PTER7                   ;SELECT TRDI BITS 47:32
9014
9015                                            ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFER BITS TRDI 59:48 WITH A
9016                                            ;DATA PATTERN OF 0
9017
9018  024326  004537  006426                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
9019  024332  000010                            .WORD   PTER8                   ;SELECT TRDI BITS 59:48
9020  024334                                    ENDSUB
9021  024334                          L10154:
9022  024334  104403                            TRAP    C$ESUB
9023
9024  024336                                    BGNSUB
9025  024336                          T52.2:
9026  024336  104402                            TRAP    C$BSUB
9027
9028                                            ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER
9029                                            ;0.  ALL THE TRACE RAM DATA IN BUFFER BITS TRDI 59:0 WILL BE CLEARED.
9030                                            ;THE TRDI BITS ARE USED TO ADDRESS THE AND ARRAYS.  THIS SUBTEST WILL
9031                                            ;WRITE INTO AND CHECK LOCATION 0 OF EACH AND ARRAY WITH THE PTER SIGNAL
9032                                            ;WHICH SELECTS THE AND ARRAY.
9033
9034  024340  012737  000000  002376              MOV     #PTER0,R2LOAD           ;SETUP TO START WITH 1ST AND ARRAY
9035
9036  024346                          1$:       BGNSEG
9037  024346  104404                            TRAP    C$BSEG
9038
9039  024350  004737  006134                    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9040  024354  001405                            BEQ     2$                      ;IF LOADED OK THEN CONTINUE
9041  024356                                    ERRDF   2.,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9042  024356  104455                            TRAP    C$ERDF
9043  024360  000002                            .WORD   2
9044  024362  000000                            .WORD   0
9045  024364  004704                            .WORD   R2EROR
9046  024366                                    CKLOOP
9047  024366  104406                            TRAP    C$CLP1
9048
9049                                            ;LOAD READ AND CHECK AND ARRAY WITH THE PTER SIGNAL WHICH SELECTS THE
9050                                            ;AND ARRAY.
9051
9052  024370  013737  002376  002402    2$:     MOV     R2LOAD,R4LOAD           ;GET THE PTER SIGNAL USED
9053  024376  004737  006166                    JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
9054  024402  001404                            BEQ     3$                      ;IF LOADED OK THEN CONTINUE
9055  024404                                    ERRDF   3,ANDERR,R4EROR         ;AND ARRAY NOT EQUAL PTER SIGNAL
9056  024404  104455                            TRAP    C$ERDF
9057  024406  000003                            .WORD   3
9058  024410  003550                            .WORD   ANDERR
9059  024412  004720                            .WORD   R4EROR
9060  024414                          3$:       ENDSEG
9061  024414                          10000$:
9062  024414  104405                            TRAP    C$ESEG
9063  024416  005237  002376                    INC     R2LOAD                  ;JPDATE THE PTER SIGNAL BY ONE
9064  024422  022737  000017  002376            CMP     #PTER15,R2LOAD          ;CHECK IF ALL AND ARRAYS WRITTEN
```

```
9065  024430  001346                        BNE     1$                      ;IF NOT THEN LOAD NEXT AND ARRAY
9066  024432                                ENDSUB
9067  024432                          L10155:
9068  024432  104403                        TRAP    C$ESUB
9069
9070  024434                                BGNSUB
9071  024434                          T52.3:
9072  024434  104402                        TRAP    C$BSUB
9073
9074                                        ;ON ENTRANCE TO THIS SUB TEST, CDAL4 WILL BE CLEARED IN CONTROL REGISTER
9075                                        ;0.  ALL TRACE RAM DATA IN BUFFER BITS TRDI 59:0 WILL BE CLEARED.
9076                                        ;LOCATION 0 OF EACH AND ARRAY WILL CONTAIN AS DATA THE PTER SIGNAL
9077                                        ;WHICH SELECTS THE AND ARRAY.  THIS SUB TEST WILL READ LOCATION 0
9078                                        ;OF EACH AND ARRAY CHECKING THE DATA TO EQUAL THE PTER SELECT SIGNAL.
9079                                        ;THIS SUB TEST CHECKS THAT EACH AND ARRAY CAN BE SELECTED.
9080
9081  024436  012737  000000  002376        MOV     #PTER0,R2LOAD           ;SETUP TO START WITH THE 1ST AND ARRAY
9082  024444                          1$:   BGNSEG
9083  024444  104404                        TRAP    C$BSEG
9084
9085  024446  004737  006134                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9086  024452  001405                        BEQ     2$                      ;IF LOADED OK THEN CONTINUE
9087  024454                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9088  024454  104455                        TRAP    C$ERDF
9089  024456  000002                        .WORD   2
9090  024460  000000                        .WORD   0
9091  024462  004704                        .WORD   R2EROR
9092  024464                                CKLOOP
9093  024464  104406                        TRAP    C$CLP1
9094
9095                                        ;READ AND ARRAY CHECKING THE DATA TO EQUAL THE SELECT PTER SIGNAL
9096
9097  024466  013737  002376  002402  2$:   MOV     R2LOAD,R4LOAD           ;GET THE PTER SELECT SIGNAL
9098  024474  013737  002402  002404        MOV     R4LOAD,R4GOOD           ;COPY IT INTO EXPECTED DATA
9099  024502  000337  002404                SWAB    R4GOOD                  ;PUT ACTUAL BITS IN EXPECTED READBACK
9100  024506  004737  006216                JSR     PC,READR4               ;GO READ AND CHECK AND ARRAY
9101  024512  001404                        BEQ     3$                      ;IF EQUAL EXPECTED THEN CONTINUE
9102  024514                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY SELECTION ERROR
9103  024514  104455                        TRAP    C$ERDF
9104  024516  000003                        .WORD   3
9105  024520  003550                        .WORD   ANDERR
9106  024522  004720                        .WORD   R4EROR
9107  024524                          3$:   ENDSEG
9108  024524                          10000$:
9109  024524  104405                        TRAP    C$ESEG
9110  024526  005237  002376                INC     R2LOAD                  ;UPDATE THE PTER SIGNAL
9111  024532  022737  000017  002376        CMP     #PTER15,R2LOAD          ;CHECK IF DONE ALL AND ARRAYS
9112  024540  001341                        BNE     1$                      ;IF NOT THE GO CHECK NEXT AND ARRAY
9113  024542                                ENDSUB
9114  024542                          L10156:
9115  024542  104403                        TRAP    C$ESUB
9116  024544                                ENDTST
9117  024544                          L10153:
9118  024544  104401                        TRAP    C$ETST
```

```
                                        .SBTTL  TEST 53: AND ARRAY RAM(S) ADDRESS/SHORT TEST

                                        ;++
                                        ; THIS TEST WILL CHECK THAT EACH AND ARRAY RAM CAN BE ADDRESSED CORRECTLY AND
                                        ; THAT WRITING ONE LOCATION IN THE AND ARRAY DOES NOT WRITE A HIGHER LOCATION
                                        ; AT THE SAME TIME (ADDRESS SHORT).  THE TEST WILL CHECK ONE AND ARRAY RAM AT
                                        ; A TIME UNTIL ALL AND ARRAY RAMS ARE TESTED.  THE TEST WILL LOAD AND CHECK
                                        ; EACH LOCATION OF A 16*4 AND ARRAY WITH DATA EQUAL TO THE ADDRESS SELECTED
                                        ; (0-17 OCTAL).  ONCE ALL THE LOCATIONS HAVE BEEN WRITTEN AND CHECKED, THE TEST
                                        ; WILL START AT THE BEIGNNING ADDRESS OF THE AND ARRAY AND DO THE FOLLOWING:
                                        ;    1.  READ LOCATION CHECKING DATA TO EQUAL THE ADDRESS (0-17 OCTAL)
                                        ;    2.  WRITE AND CHECK LOCATION WITH 1'S COMPLEMENT OF THE ADDRESS
                                        ;    3.  SEQUENCE TO THE NEXT ADDRESS
                                        ;    4.  REPEAT STEPS 1-3 UNTIL ALL ADDRESSES HAVE BEEN CHECKED.
                                        ; WHEN THE ABOVE SEQUENCE HAS BEEN COMPLETED, THE TEST WILL RESET THE ADDRESS
                                        ; TO THE BEGINNING ADDRESS OF THE AND ARRAY AND CHECK EACH LOCATION TO CONTAIN
                                        ; THE 1'S COMPLEMENT OF THE ADDRESS.
                                        ;--

024546                                          BGNTST
024546                                  T53::
024546  004737  005474                          JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

024552  012737  170377  002406                  MOV     #170377,R4MASK          ;SETUP AND ARRAY MASK WORD
024560  005001                                  CLR     R1                      ;CLEAR ADDRESS/DATA COUNTER
024562  012702  000005                          MOV     #PTER5,R2               ;TRAM DATA IN BUFFER SELECTION
024566  012703  000000                          MOV     #PTER0,R3               ;AND ARRAY SELECTION
024572  012704  000001                          MOV     #1,R4                   ;# TO BE ADDED TO TRDI BITS TO GET NEXT
                                                                                ;AND ARRAY ADDRESS
024576  005037  002414                          CLR     R6LOAD                  ;START AND ARRAY ADDRESS OFF AT 0

024602                                  1$:     BGNSEG
024602  104404                                  TRAP    C$BSEG

                                        ;CLEAR CDAL4 IN CONTROL REGISTER 0 TO SELECT ONLY ONE AND/OR ARRAY
                                        ;VIA THE POINTER REGISTER.  CDAL3 AND CDAL2 ON A 0 WILL ASSERT THE
                                        ;SIGNAL TRSL0 L WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA
                                        ;IN BUFFER SELECTED.

024604  105037  002370                          CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
024610  004737  006102                          JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
024614  001405                                  BEQ     2$                      ;IF LOADED OK THEN CONTINUE
024616                                          ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
024616  104455                                  TRAP    C$ERDF
024620  000001                                  .WORD   1
024622  000000                                  .WORD   0
024624  004604                                  .WORD   R0EROR
024626                                          CKLOOP
024626  104406                                  TRAP    C$CLP1

                                        ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0, 31:16,
                                        ;47:32 OR 59:48 WITH DATA STORED IN LOCATION "R6LOAD".

024630  010237  024640         2$:     MOV     R2,3$                   ;GET THE TRAM DATA IN BUF SELECTION
024634  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
024640  000005                 3$:     .WORD   PTER5                   ;PTER5, PTER6, PTER7, OR PTER8
```

```
9175
9176                                    ;SELECT THE AND ARRAY TO BE TESTED VIA CONTROL REGISTER 2 WITH THE
9177                                    ;PTER SIGNAL IN GENERAL CPU REGISTER R3
9178
9179  024642  010337  002376            MOV     R3,R2LOAD               ;GET THE PTER SELECT SIGNAL
9180  024646  004737  006134            JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9181  024652  001405                    BEQ     4$                      ;IF LOADED OK THEN CONTINUE
9182  024654                            ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9183  024654  104455                    TRAP    C$ERDF
9184  024656  000002                    .WORD   2
9185  024660  000000                    .WORD   0
9186  024662  004704                    .WORD   R2EROR
9187  024664                            CKLOOP
9188  024664  104406                    TRAP    C$CLP1
9189
9190                                    ;LOAD, READ AND CHECK AND ARRAY WITH DATA EQUAL TO ADDRESS SELECTED
9191
9192  024666  010137  002402    4$:     MOV     R1,R4LOAD               ;GET THE ADDRESS BEING TESTED
9193  024672  004737  006166            JSR     PC,LDRDR                ;GO LOAD, READ AND CEHCK AND ARRAY
9194  024676  001404                    BEQ     5$                      ;IF LOADED OK THEN CONTINUE
9195  024700                            ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR SELECTED VIA REG 2
9196  024700  104455                    TRAP    C$ERDF
9197  024702  000003                    .WORD   3
9198  024704  003550                    .WORD   ANDERR
9199  024706  004720                    .WORD   R4EROR
9200  024710                    5$:     ENDSEG
9201  024710                    '0000$:
9202  024710  104405                    TRAP    C$ESEG
9203
9204  024712  060437  002414            ADD     R4,R6LOAD               ;UPDATE AND ARRAY ADDRESS TO NEXT
9205                                                                    ;SEQUENTIAL ADDRESS
9206  024716  005201                    INC     R1                      ;UPDATE ADDRESS/DATA COUNTER
9207  024720  022701  000020            CMP     #20,R1                  ;CHECK IF ALL 16 ADDRESSES DONE
9208  024724  001326                    BNE     1$                      ;IF NOT - DO NEXT ADDRESS OF AND ARRAY
9209
9210  024726  005001                    CLR     R1                      ;RESET ADDRESS/DATA COUNTER
9211  024730  005037  002414            CLR     R6LOAD                  ;RESET AND ARRAY ADDRESS TO 0
9212
9213  024734                    6$:     BGNSEG
9214  024734  104404                    TRAP    C$BSEG
9215
9216                                    ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0, 31:16,
9217                                    ;47:32, OR 59:48 WITH DATA STORED IN LOCATION "R6LOAD".
9218
9219  024736  010237  024746            MOV     R2,7$                   ;GET TRAM DATA IN BUFFER SELECTION
9220  024742  004537  006426            JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
9221  024746  000005            7$:     .WORD   PTER5                   ;PTER5, PTER6, PTER7 OR PTER8
9222
9223                                    ;SELECT THE AND ARRAY TO BE TESTED VIA CONTROL REGISTER 2 WITH THE
9224                                    ;PTER SIGNAL IN GENERAL CPU REGISTER R3
9225
9226  024750  010337  002376            MOV     R3,R2LOAD               ;GET THE PTER SIGNAL TO BE LOADED
9227  024754  004737  006134            JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
9228  024760  001405                    BEQ     8$                      ;IF LOADED OK THEN CONTINUE
9229  024762                            ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9230  024762  104455                    TRAP    C$ERDF
```

```
9231  024764  000002                  .WORD   2
9232  024766  000000                  .WORD   0
9233  024770  004704                  .WORD   R2EROR
9234  024772                          CKLOOP
9235  024772  104406                  TRAP    C$CLP1
9236
9237                                  ;READ AND CHECK AND ARRAY LOCATION TO EQUAL DATA PREVIOUSLY LOADED.
9238                                  ;THE DATA SHOULD EQUAL THE ADDRESS OF THE AND ARRAY (0-17 OCTAL).
9239
9240  024774  010137  002402          8$:     MOV     R1,R4LOAD               ;SETUP DATA PREVIOULSY LOADED
9241  025000  013737  002402  002404          MOV     R4LOAD,R4GOOD           ;COPY IT TO EXPECTED DATA
9242  025006  000337  002404                  SWAB    R4GOOD                  ;PUT EXPECTED DATA IN ACTUAL READBACK
9243  025012  004737  006216                  JSR     PC,READR4               ;GO READ AND CHECK AND ARRAY LOCATION
9244  025016  001404                          BEQ     9$                      ;IF DATA OK THEN CONTINUE
9245  025020                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR OR ADDRESSING ERROR
9246  025020  104455                          TRAP    C$ERDF
9247  025022  000003                          .WORD   3
9248  025024  003550                          .WORD   ANDERR
9249  025026  004720                          .WORD   R4EROR
9250  025030                          9$:     ENDSEG
9251  025030                          1000$:
9252  025030  104405                          TRAP    C$ESEG
9253
9254  025032  005137  002402                  COM     R4LOAD                  ;COMPLEMENT THE ADDRESS
9255  025036  042737  177760  002402          BIC     #177760,R4LOAD          ;CLEAR UNWANTED BITS
9256
9257  025044                                  BGNSEG
9258  025044  104404                          TRAP    C$BSEG
9259
9260                                  ;WRITE, READ AND CHECK AND ARRAY WITH THE 1'S COMPLEMENT OF THE ADDRESS
9261                                  ;BEING TESTED.
9262
9263  025046  004737  006166                  JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
9264  025052  001404                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
9265  025054                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA EROR
9266  025054  104455                          TRAP    C$ERDF
9267  025056  000003                          .WORD   3
9268  025060  003550                          .WORD   ANDERR
9269  025062  004720                          .WORD   R4EROR
9270  025064                          10$:    ENDSEG
9271  025064                          1C002$:
9272  025064  104405                          TRAP    C$ESEG
9273
9274  025066  060437  002414                  ADD     R4,R6LOAD               ;UPDATE AND ARRAY ADDRESS BY UPDATING
9275                                                                          ;TRAM DATA IN BUFFER BITS
9276  025072  005201                          INC     R1                      ;UPDATE ADDRESS/DATA COUNTER
9277  025074  022701  000020                  CMP     #20,R1                  ;CHECK IF ALL 16 ADDRESS BEEN TESTED
9278  025100  001315                          BNE     6$                      ;IF NOT THEN CHECK NEXT ADDRESS
9279
9280  025102  005001                          CLR     R1                      ;CLEAR ADDRESS/DATA COUNTER
9281  025104  005037  002414                  CLR     R6LOAD                  ;RESET AND ARRAY ADDRESS TO 0
9282
9283  025110                          11$:    BGNSEG
9284  025110  104404                          TRAP    C$BSEG
9285
9286                                  ;LOAD, READ AND CHECK TRACE RAM DATA IN BUFFERS TRDI 15:0, 31:16,
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                                        ;47:32, OR 59:48 WITH DATA IN LOCATION 'R6LOAD'.

025112  010237  025122                  MOV     R2,12$                  ;GET TRAM DATA IN BUFFER SELECTION
025116  004537  006426                  JSR     R5,TRDIBF               ;LOAD READ AND CHECK TRAM DATA IN BUF
025122  000005          12$:            .WORD   PTER5                   ;PTER5, PTER6, PTER7 OR PTER8

                                        ;SELECT AND ARRAY TO BE TESTED VIA CONTROL REGISTER 2 WITH THE PTER
                                        ;SIGNAL IN GENERAL RECISTER R3.

025124  010337  002376                  MOV     R3,R2LOAD               ;GET THE PTER SIGNAL TO BE LOADED
025130  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
025134  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
025136                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
025136  104455                          TRAP    C$ERDF
025140  000002                          .WORD   2
025142  000000                          .WORD   0
025144  004704                          .WORD   R2EROR
025146                                  CKLOOP
025146  104406                          TRAP    C$CLP1

                                        ;READ, AND CHECK AND ARRAY LOCATION TO EQUAL THE 1'S COMPLEMENT OF THE
                                        ;ADDRESS SELECTED BY THE TRDI BITS.

025150  010137  002402          13$:    MOV     R1,R4LOAD               ;GET THE ADDRESS/DATA COUNTER
025154  005137  002402                  COM     R4LOAD                  ;MAKE THE 1'S COMPLEMENT
025160  042737  177760  002402          BIC     #177760,R4LOAD          ;CLEAR UNWANTED BITS
025166  013737  002402  002404          MOV     R4LOAD,R4GOOD           ;COPY DATA INTO EXPECTED DATA
025174  000337  002404                  SWAB    R4GOOD                  ;PUT EXPECTED DATA IN READBACK BITS
025200  004737  006216                  JSR     PC,READR4               ;GO READ AND CHECK AND ARRAY
025204  001404                          BEQ     14$                     ;IF DATA OK THEN CONTINUE
025206                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR/OR ADDRESS SHORT
025206  104455                          TRAP    C$ERDF
025210  000003                          .WORD   3
025212  003550                          .WORD   ANDERR
025214  004720                          .WORD   R4EROR
025216                          14$:    ENDSEG
025216                          10003$:
025216  104405                          TRAP    C$ESEG

025220  060437  002414                  ADD     R4,R6LOAD               ;UPDATE TRAM DATA IN BUFFER BITS USED
                                                                        ;FOR ADDRESS SELECTION
025224  005201                          INC     R1                      ;UPDATE ADDRESS/DATA COUNTER
025226  022701  000020                  CMP     #20,R1                  ;CHECK IF ALL 16 ADDRESSES TESTED
025232  001326                          BNE     11$                     ;IF NOT THEN TEST NEXT ADDRESS

025234  005001                          CLR     R1                      ;CLEAR ADDRESS/DATA COUNTER
025236  005037  002414                  CLR     R6LOAD                  ;RESET AND ARRAY ADDRESS TO 0

025242  022702  000010                  CMP     #PTER8,R2               ;CHECK IF LAST SET OF DATA IN BUFFERS
025246  001004                          BNE     15$                     ;IF NOT THEN CONTINUE
025250  022704  000400                  CMP     #BIT8,R4                ;CHECK IF ALL AND ARRAYS DONE
025254  001004                          BNE     16$                     ;IF NOT THEN DO NEXT AND ARRAY
025256  000420                          BR      18$                     ;EXIT THE TEST
025260  022704  010000          15$:    CMP     #BIT12,R4               ;CHECK IF END OF THIS SET OF DATA IN BUF
025264  001407                          BEQ     17$                     ;IF YES THEN GO UPDATE PTER SELECTS
025266  006304          16$:    ASL     R4                              ;UPDATE TRDI AND ARRAY ADDRESS SELECTION
```

```
9343  025270  006304                        ASL     R4                      ;
9344  025272  006304                        ASL     R4
9345  025274  006304                        ASL     R4
9346  025276  005203                        INC     R3                      ;  UPDATE AND ARRAY PTER SELECT SIGNAL
9347  025300  000137  024602                JMP     1$                      ;  TO DO NEXT AND ARRAY IN THIS SET
9348  025304  005202                17$:    INC     R2                      ;  UPDATE TRAM DATA IN BUFFER SELECTION
9349  025306  005203                        INC     R3                      ;  UPDATE AND ARAY PTER SELECT SIGNAL
9350  025310  012704  000001                MOV     #1,R4                   ;  RESET TRDI AND ARRAY ADDRESS SELECTION
9351  025314  000137  02460*                JMP     1$                      ;  TO DO NEXT SET OF AND ARRAYS
9352  025320                        18$:    ENDTST
9353  025320                        L**157:
9354  025320  104401                        TRAP    CSE*ST
9355
```

```
                                .SBTTL  TEST 54: EVENT COUNTER 0 AND 2 TEST

                                ;**
                                ; THIS TEST WILL CHECKOUT EVENT COUNTER LOGIC FOR EVENT COUNTER 0 AND 2.  THE
                                ; TEST WILL CHECK THAT THE EVENT COUNTER REGISTERS AND EVENT COUNTERS ARE LOAD-
                                ; ED CORRECTLY BY COUNTING DOWN THE EVENT COUNTERS AND CHECKING THE FOUT FLIP-
                                ; FLOPS FOR A BORROW.  WHEN THE EVENT COUNTERS ARE COUNTED DOWN TO ZERO AND ONE
                                ; MORE COUNT DOWN IS ISSUED, A BORROW IS GENERATED WHICH WILL SET THE OUTPUT OF
                                ; THE FOUT FLIP-FLOP TO A LOW STATE.  THE TEST WILL CHECK THAT THE EVENT COUNTERS
                                ; ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN A BORROW IS GENERATED. THIS
                                ; IS DONE BY COUNTING DOWN THE EVENT COUNTERS AGAIN CHECKING FOR A BORROW FROM
                                ; THE EVENT COUNTERS.  THE TEST WILL THEN CHECK THAT THE EVENT COUNTERS CAN BE
                                ; CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7.  AFTER SETTING AND CLEARING
                                ; THE SIGNAL PDAL7, THE TEST WILL DO ONE MORE COUNT DOWN AND CHECK THAT A BORROW
                                ; IS GENERATED FROM THE EVENT COUNTERS.  THE ABOVE SEQUENCE IS REPEATED FOR EACH
                                ; OF THE FOLLOWING DATA PATTERNS: 0, 1, 2, 4, 10, 20, 40, 100, 200, 125 AND 252.
                                ;--

                                        BGNTST
                                T54::
025322  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

                                        BGNSEG
025326  104404                          TRAP    C$BSEG

                                        ;SET CDAL4 TO A ZERO IN CONTROL REGISTER 0.  CDAL4 BEING A 0 WILL ALLOW
                                        ;ONLY ONE AND/OR ARRAY TO BE SELECTED AT A TIME.  CDAL3 AND CDAL2 ON A
                                        ;ZERO WILL CAUSE THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE
                                        ;OUTPUTS OF THE TRACE RAM DATA IN BUFFERS.  THESE OUTPUTS ARE USED TO
                                        ;ADDRESS THE AND ARRAYS.

025330  105037  002370                  CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
025334  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
025340  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
025342                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
025342  104455                          TRAP    C$ERDF
025344  000001                          .WORD   1
025346  000000                          .WORD   0
025350  004604                          .WORD   R0EROR
025352                                  CKLOOP
025352  104406                          TRAP    C$CLP1

                                        ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER TRDI 15:0.  ALL ZEROES
                                        ;WILL SELECT ADDRESS 0 OF THE AND ARRAY TO BE USED IN THIS TEST.

025354  005037  002414          1$:     CLR     R6LOAD                  ;SETUP TO LOAD ZEROES
025360  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
025364  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                        ;SET PTER0 IN THE POINTER REGISTER VIA CONTROL REGISTER 2.  THIS WILL
                                        ;SELECT THE FIRST AND ARRAY VIA THE SIGNAL PLSLO L.

025366  012737  000000  002376          MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
025374  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CEHCK REGISTER 2
025400  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
025402                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
```

```
9412  025402  104455                  TRAP    C$ERDF
9413  025404  000002                  .WORD   2
9414  025406  000000                  .WORD   0
9415  025410  004704                  .WORD   R2EROR
9416  025412                          CKLOOP
9417  025412  104406                  TRAP    C$CLP1
9418
9419                                  ;LOAD, READ AND CHECK AND ARRAY RAM WITH DATA PATTERN OF 12.  THIS DATA
9420                                  ;PATTERN WILL SET THE SIGNALS ANDO L AND AND2 L TO THE HIGH STATE AND
9421                                  ;THE SIGNALS AND1 L AND AND3 L TO THE LOW STATE.  WITH ANDO L AND AND2 L
9422                                  ;SET HIGH AND THE SIGNAL ANST L BEING PULSED, A PULSE WILL OCCUR
9423                                  ;ON THE SIGNALS CNDNO H AND CNDN2 H.  THESE SIGNALS WILL COUNT DOWN
9424                                  ;EVENT COUNTERS 0 AND 2.
9425
9426  025414  012737  000012  002402  2$:     MOV     #12,R4LOAD              ;SETUP DATA PATTERN TO BE LOADED
9427  025422  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
9428  025430  004737  006166                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY
9429  025434  001 4                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
9430  025436                                  ERRDF   3,ANDERR,R4ERCR         ;AND ARRAY DATA ERROR
9431  025436  104455                  TRAP    C$ERDF
9432  025440  000003                  .WORD   3
9433  025442  003550                  .WORD   ANDERR
9434  025444  004720                  .WORD   R4EROR
9435  025446                          3$:     ENDSEG
9436  025446                          10000$:
9437  025446  104405                  TRAP    C$ESEG
9438
9439  025450  005001                  CLR     R1                      ;START EVENT COUNTERS OFF AT 0
9440
9441  025452                          4$:     BGNSEG
9442  025452  104404                  TRAP    C$BSEG
9443  025454  010102                  MOV     R1,R2                   ;COPY STARTING EVENT COUNTER TO WORKING
9444
9445                                  ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0. CDAL7 ON A ONE WILL ALLOW
9446                                  ;THE FOUT FLIP-FLOPS TO BE READ ON THE OR ADDRESS REGISTER LINES ORAD 3:0.
9447
9448  025456  052737  000200  002370          BIS     #CDAL7,R0LOAD           ;SETUP BIT TO BE LOADED
9449  025464  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
9450  025470  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
9451  025472                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
9452  025472  104455                  TRAP    C$ERDF
9453  025474  000001                  .WORD   1
9454  025476  000000                  .WORD   0
9455  025500  004604                  .WORD   R0EROR
9456  025502                          CKLOOP
9457  025502  104406                  TRAP    C$CLP1
9458
9459                                  ;SET AND CLEAR PDAL7 IN CONTROL REGISTER 2. PDAL7 BEING SET WILL
9460                                  ;CLEAR ALL THE EVENT COUNTERS.
9461
9462  025504  052737  000200  002376  5$:     BIS     #PDAL7,R2LOAD           ;SETUP BIT TO BE LOADED
9463  025512  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9464  025516  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
9465  025520                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9466  025520  104455                  TRAP    C$ERDF
9467  025522  000002                  .WORD   2
```

```
9469  025526  004704                          .WORD   R2EROR
9470  025530                                  CKLOOP
9471  025530  104406                          TRAP    C$CLP1
9472
9473                                          ;CLEAR PDAL7 AND LOAD ALL EVENT COUNTER REGISTERS AND EVENT COUNTERS
9474                                          ;WITH THE WORKING EVENT COUNT STORED IN GENERAL CPU REGISTER R2.  THE
9475                                          ;SIGNALS ISSUED IN THE FOLLOWING LOOP ARE WPT9 H, WPTA L, WPT10 H,
9476                                          ;WPTB L, WPT11 H, WPTC L, WPT12 H, AND WPTD L.  THESE SIGNALS ARE USED
9477                                          ;TO LOAD THE DATA INTO THE EVENT COUNTER REGISTERS AND EVENT COUNTERS
9478                                          ;ON A WRITE COMMAND TO CONTROL REGISTER 6.
9479
9480  025532  012737  [illegible]  006376  6$:     MOV     #PTER9,R2LOAD           ;SETUP BITS TO BE LOADED
9481  025540  004737  [illegible]          7$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9482  025544  001405                              BEQ     8$                      ;IF LOADED OK THEN CONTINUE
9483  025546                                      ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9484  025546  104455                              TRAP    C$ERDF
9485  025550  000002                              .WORD   2
9486  025552  000000                              .WORD   0
9487  025554  004704                              .WORD   R2EROR
9488  025556                                      CKLOOP
9489  025556  104406                              TRAP    C$CLP1
9490
9491  [illegible]  [illegible]  [illegible]          8$:     MOV     R2,@REG6                ;LOAD EVENT COUNTERS AND REGISTERS
9492  [illegible]  [illegible]  [illegible]                  INC     R2LOAD                  ;UPDATE TO NEXT POINTER
9493  [illegible]  [illegible]  [illegible]  006376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL COUNTER S LOADED
9494  [illegible]  [illegible]  36                           BNE     7$                      ;IF NOT THEN LOAD NEXT COUNTER
9495
9496                                          ;RESELECT THE AND ARRAY SO THAT THE SIGNALS ANDO L AND AND2 L WILL BE
9497                                          ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST.
9498
9499  [illegible]  [illegible]  [illegible]  [illegible]  9$:     MOV     #PTER0,R2LOAD           ;SETUP TO SELECT FIRST AND ARRAY
9500  [illegible]  025606  0[illegible]  [illegible]              JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9501  025612  0[illegible]                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
9502  025616                                      ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9503  025616  104455                              TRAP    C$ERDF
9504  025616  000002                              .WORD   2
9505  025620  000000                              .WORD   0
9506  025622  004704                              .WORD   R2EROR
9507  025624                                      CKLOOP
9508  025624  104406                              TRAP    C$CLP1
9509
9510                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
9511                                          ;CLEARED WILL CAUSE THE SIGNAL TRANST H TO PULSE WHICH WILL CAUSE
9512                                          ;THE SIGNAL ANST L TO PULSE.  THE SIGNAL ANST L BEING PULSED WITH THE
9513                                          ;SIGNALS ANDO L AND AND2 L SET HIGH, WILL CAUSE A PULSE OF THE SIGNALS
9514                                          ;CNDNO H AND CNDN2 H.  THESE SIGNALS WILL CAUSE EVENT COUNTER 0 AND
9515                                          ;EVENT COUNTER 2 TO COUNT DOWN BY ONE RESPECTIVELY.
9516
9517  025626  004737  006640          10$:    JSR     PC,TRANST               ;GO SET AND CLEAR CDAL6 IN CONTROL REG 0
9518
9519                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REG 2.
9520
9521  025632  004537  006376                  JSR     R5,ASSERT               ;GO ASSERT PTER15
9522  025636  000017                          .WORD   PTER15
9523
```



```
9524                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
```

```
9525                                    ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD 3:0
9526                                    ;WILL BE READ BACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
9527                                    ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON ORAD 3:0 SIGNAL LINES.
9528                                    ;THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA A BORROW FROM THE EVENT COUNTERS
9529                                    ;AND THE SIGNAL ANST L BEING PULSED.
9530
9531  025640  005037  002414       11$:  CLR     R6_CAD                  ;SETUP EXPECTED DATA
9532  025644  005702                      TST     R2                      ;CHECK IF EVENT COUNTER = 0
9533  025646  001003                      BNE     12$                     ;IF NOT THEN A BORROW SHOULD NOT OCCUR
9534  025650  012737  000005  002414      MOV     #5,R6LOAD               ;SETUP TO EXPECT A BORROW FROM COUNTER
9535                                                                      ;0 AND COUNTER 2 ON SIGNALS FOUTO L AND
9536                                                                      ;FOUT2 L.
9537  025656  017737  154474  002420  12$:  MOV     @REG6,R6READ            ;READ FOUT 3:0 BITS ON ORAD 3:0
9538  025664  042737  177760  002420      BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
9539  025672  023737  002414  002420      CMP     R6LOAD,R6READ           ;CHECK EXPECTED RESULTS AGAINST ACTUAL
9540  025700  001405                      BEQ     13$                     ;IF EQUAL THEN CONTINUE
9541  025702                              ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
9542  025702  104455                      TRAP    C$ERDF
9543  025704  000004                      .WORD   4
9544  025706  003213                      .WORD   EVNTCT
9545  025710  005024                      .WORD   EVNTER
9546  025712                              CKLOOP
9547  025712  104406                      TRAP    C$CLP1
9548  025714  005302              13$:    DEC     R2                      ;DECREMENT WORKING EVENT COUNTER
9549  025716  100330                      BPL     9$                      ;IF NOT DONE THEN COUNT DOWN AGAIN
9550
9551                                    ;WHEN THE FOUT FLIP-FLOP IS CLEARED BY A BORROW, THE EVENT COUNTERS
9552                                    ;ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE SIGNAL ORST L
9553                                    ;IS PULSED VIA THE PULSING OF SIGNAL ANST L.  THE FOLLOWING SECTION
9554                                    ;OF CODE WILL CHECK THAT THIS HAPPENS BY COUNTING DOWN THE EVENT
9555                                    ;COUNTERS AGAIN.
9556
9557  025720  010102                      MOV     R1,R2                   ;RESET EXPECTED CONTENTS OF EVENT CNTRS
9558
9559                                    ;RESELECT THE AND ARRAY SO THAT THE SIGNALS ANDO L AND AND2 L WILL BE
9560                                    ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGIMENT OF THIS TEST
9561
9562  025722  012737  000000  002376  14$:  MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
9563  025730  004737  006134              JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9564  025734  001405                      BEQ     15$                     ;IF LOADED OK THEN CONTINUE
9565  025736                              ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9566  025736  104455                      TRAP    C$ERDF
9567  025740  000002                      .WORD   2
9568  025742  000000                      .WORD   0
9569  025744  004704                      .WORD   R2EROR
9570  025746                              CKLOOP
9571  025746  104406                      TRAP    C$CLP1
9572
9573                                    ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
9574                                    ;CLEARED WILL CAUSE A PULSE ON TRANST H WHICH WILL CAUSE THE SIGNAL
9575                                    ;ANST L TO PULSE.  THE SIGNAL ANST L BEING PULSED WITH THE
9576                                    ;SIGNALS ANDO L AND AND2 L SET HIGH WILL CAUSE A PULSE ON THE SIGNALS
9577                                    ;CNDN0 H AND CNDN2 H.  THESE SIGNALS WILL CAUSE EVENT COUNTER 0 AND 2
9578                                    ;TO BE COUNTED DOWN BY ONE RESPECTIVELY.
9579
```

```
9581
9582                                    ;ASSERT THE SIGNAL PTER15 L IN POINTER REGISTER VIA CONTROL REG 2.
9583
9584  025754  004537  006376            JSR     R5,ASSERT               ;GO ASSERT PTER15
9585  025760  000017                    .WORD   PTER15
9586
9587                                    ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
9588                                    ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS,
9589                                    ;ORAD 3:0, WILL BE READBACK. IN THIS TEST, CDAL7 IS SET TO A ONE,
9590                                    ;WHICH WILL CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE
9591                                    ;ORAD 3:0 SIGNAL LINES.  THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA THE
9592                                    ;BORROW SIGNAL FROM THE EVENT COUNTERS AND THE SIGNAL ANST L BEING
9593                                    ;PULSED.
9594
9595  025762  005037  002414    16$:    CLR     R6LOAD                  ;SETUP EXPECTED FOUT SIGNALS
9596  025766  005702                    TST     R2                      ;CHECK IF EVENT COUNTER WERE ZERO
9597  025770  001003                    BNE     17$                     ;IF NOT THEN A BORROW SHOULD NOT OCCUR
9598  025772  012737  000005  002414    MOV     #5,R6LOAD               ;SETUP TO EXPECT FOUT0 L AND FOUT2 L
9599                                                                    ;TO BE SET AS A RESULT OF A BORROW
9600                                                                    ;ON EVENT COUNTER 0 AND 2
9601
9602  026000  017737  154352  002420  17$:    MOV     @REG6,R6READ            ;READBACK FOUT 3:0 FLIP-FLOPS
9603  026006  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
9604  026014  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED DATA WITH ACTUAL DATA
9605  026022  001405                          BEQ     18$                     ;IF EQUAL THEN CONTINUE
9606  026024                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
9607  026024  104455                          TRAP    C$ERDF
9608  026026  000004                          .WORD   4
9609  026030  003213                          .WORD   EVNTCT
9610  026032  005024                          .WORD   EVNTER
9611  026034                                  CKLOOP
9612  026034  104406                          TRAP    C$CLP1
9613  026036  005302                18$:      DEC     R2                      ;CHECK IF COUNTER WAS 0
9614  026040  100330                          BPL     14$                     ;IF NOT COUNT DOWN EVENT COUNTER AGAIN
9615
9616                                    ;WHEN THE FOUT FLIP-FLOP IS CLEARED BY A BORROW. THE EVENT COUNTERS
9617                                    ;ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE SIGNAL ORST L
9618                                    ;IS PULSED VIA THE PULSING OF THE SIGNAL ANST L.  THE PREVIOUS SECTION
9619                                    ;OF CODE VERIFIED THAT THIS HAPPENED.
9620
9621                                    ;THE FOLLOWING SECTION OF CODE WILL CHECK THAT THE EVENT COUNTERS CAN BE
9622                                    ;CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7 IN CONTROL REGISTER 2.
9623                                    ;THE TEST, AFTER SETTING AND CLEARING PDAL7, WILL DO ONE MORE COUNT
9624                                    ;DOWN AND CHECK THAT A BORROW WAS GENERATED FROM COUNTER 0 AND 2.
9625
9626  026042  010102                    MOV     R1,R2                   ;RESET EXPECTED CONTENTS OF EVNT CNTRS
9627
9628                                    ;RESELECT THE AND ARRAY SO THAT THE SIGNALS ANDO L AND AND2 L WILL BE
9629                                    ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST.
9630
9631  026044  012737  000200  002376    MOV     #PTER0!PDAL7,R2LOAD     ;SETUP BITS TO BE LOADED
9632  026052  004737  006134            JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
9633  026056  001405                    BEQ     19$                     ;IF LOADED OK THEN CONTINUE
9634  026060                            ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9635  026060  104455                    TRAP    C$ERDF
```

```
9636  026062  000002                          .WORD   2
9637  026064  000000                          .WORD   0
9638  026066  004704                          .WORD   R2EROR
9639  026070                                  CKLOOP
9640  026070  104406                          TRAP    C$CLP1
9641
9642                                          ;CLEAR PDAL7 IN CONTROL REGISTER 2. THE EVENT COUNTERS SHOULD NOW
9643                                          ;BE CLEARED. CLEARING PDAL7 WILL ALLOW THE COUNTERS TO BE COUNTED DOWN
9644
9645  026072  042737  000200  002376  19$:    BIC     #PDAL7,R2LOAD           ;SETUP TO CLEAR PDAL7
9646  026100  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
9647  026104  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
9648  026106                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9649  026106  104455                          TRAP    C$ERDF
9650  026110  000002                          .WORD   2
9651  026112  000000                          .WORD   0
9652  026114  004704                          .WORD   R2EROR
9653  026116                                  CKLOOP
9654  026116  104406                          TRAP    C$CLP1
9655
9656                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  CDAL6 BEING SET AND
9657                                          ;CLEARED WILL CAUSE A PULSE ON TRANST H WHICH WILL CAUSE THE SIGNAL
9658                                          ;ANST L TO PULSE.  THE SIGNAL ANST L BEING PULSED
9659                                          ;WITH THE SIGNALS ANDO L AND AND2 L SET HIGH, WILL CAUSE A PULSE ON
9660                                          ;THE SIGNALS CNDNO H  AND CNDN2 H.  THESE SIGNALS WILL COUNT DOWN
9661                                          ;EVENT COUNTERS 0 AND 2 RESPECTIVELY.  IF PDAL7 CLEARED THE EVENT
9662                                          ;COUNTERS THEN A BORROW WILL BE GENERATED FROM EVENT COUNTERS 0 AND 2.
9663
9664  026120  004737  006640          20$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REC 0
9665
9666                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REG 2.
9667
9668  026124  004537  006376                  JSR     R5,ASSERT               ;GO ASSERT PTER15
9669  026130  000017                          .WORD   PTER15
9670
9671                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
9672                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD
9673                                          ;3:0 WILL BE READBACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
9674                                          ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE ORAD 3:0 SIGNAL
9675                                          ;LINES.  HAVING SET AND CLEARED PDAL7, TO CLEAR THE EVENT COUNTERS, AND
9676                                          ;ISSUING A COUNT DOWN TO EVENT COUNTERS 0 AND 2, FOUT FLIP FLOPS 0 AND
9677                                          ;2 SHOULD BE CLEARED AS A RESULT OF A BORROW AND THE COUNT DOWN PULSE.
9678
9679  026132  012737  000005  002414  21$:    MOV     #5,R6LOAD               ;SETUP TO EXPECT FOUT0 L AND FOUT2 L
9680                                                                          ;TO BE SET AS A RESULT OF A BORROW
9681  026140  017737  154212  002420          MOV     @REG6,R6READ            ;READBACK FOUT 3:0 FLIP-FLOPS
9682  026146  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
9683  026154  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED FOUTS AGAINST ACTUAL
9684  026162  001404                          BEQ     22$                     ;IF THE SAME THEN CONTINUE
9685  026164                                  ERRDF   4,EVNTCL,EVNTER         ;PDAL7 FAILED TO CLEAR EVENT COUNTERS
9686  026164  104455                          TRAP    C$ERDF
9687  026166  000004                          .WORD   4
9688  026170  003254                          .WORD   EVNTCL
9689  026172  005024                          .WORD   EVNTER
9690  026174                          22$:    ENDSEG
9691  026174                          10001$:
```

```
9692  026 74   04405                    TRAP    CSESEG
9693
9694  026 76   005701                   TST     R1                      ;CHECK IF FIRST DATA PATTERN
9695  026200   001003                   BNE     23$                     ;IF NOT THEN ROTATE PATTERN LEFT ONE
9696  026202   005201                   INC     R1                      ;SET PATTERN TO A ONE
9697  026204   000137  025452           JMP     4$                      ;GO DO SEQUENCE WITH THIS PATTERN
9698  026210   006301           23$:    ASL     R1                      ;ARITHMETIC SHIFT LEFT ONCE
9699  026212   032701  000400           BIT     #400,R1                 ;CHECK IF PATTERN GREATER THEN 256
9700  026216   001002                   BNE     24$                     ;IF YES THEN CHECK IF DONE
9701  026220   000137  025452           JMP     4$                      ;GO DO TEST AGAIN WITH ROTATED PATTERN
9702  026224   105701           24$:    TSTB    R1                      ;CHECK IF PATTERN WAS FLOATTING ONE
9703  026226   001004                   BNE     25$                     ;IF NOT THEN END OF TEST
9704  026230   012701  000125           MOV     #125,R1                 ;SETUP TO DO 125 AND 252 PATTERNS
9705  026234   000137  025452           JMP     4$                      ;GO DO TEST WITH 125 FIRST
9706
9707  026240           25$:    ENDTST
9708  026240           C10160:
9709  026240   104401                   TRAP    CSETST
9710
```

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9711                                    .SBTTL  TEST 55: EVENT COUNTER 1 AND 3 TEST
9712
9713                                    ;++
9714                                    ; THIS TEST WILL CHECKOUT EVENT COUNTER LOGIC FOR EVENT COUNTER 1 AND 3.  THE
9715                                    ; TEST WILL CHECK THAT THE EVENT COUNTER REGISTERS AND EVENT COUNTERS ARE LOAD-
9716                                    ; ED CORRECTLY BY COUNTING DOWN THE EVENT COUNTERS AND CHECKING THE FOUT FLIP-
9717                                    ; FLOPS FOR A BORROW.  WHEN THE EVENT COUNTERS ARE COUNTED DOWN TO ZERO AND ONE
9718                                    ; MORE COUNT DOWN IS ISSUED, A BORROW IS GENERATED WHICH WILL SET THE OUTPUT OF
9719                                    ; THE FOUT FLIP-FLOP TO A LOW STATE.  THE TEST WILL CHECK THAT THE EVENT COUNTERS
9720                                    ; ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN A BORROW IS GENERATED. THIS
9721                                    ; IS DONE BY COUNTING DOWN THE EVENT COUNTERS AGAIN CHECKING FOR A BORROW FROM
9722                                    ; THE EVENT COUNTERS.  THE TEST WILL THEN CHECK THAT THE EVENT COUNTERS CAN BE
9723                                    ; CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7.  AFTER SETTING AND CLEARING
9724                                    ; THE SIGNAL PDAL7, THE TEST WILL DO ONE MORE COUNT DOWN AND CHECK THAT A BORROW
9725                                    ; IS GENERATED FROM THE EVENT COUNTERS.  THE ABOVE SEQUENCE IS REPEATED FOR EACH
9726                                    ; OF THE FOLLOWING DATA PATTERNS: 0, 1, 2, 4, 10, 20, 40, 100, 200, 125 AND 252.
9727                                    ;--
9728
9729  026242                                    BGNTST
9730  026242                            T55::
9731  026242  004737  005474                    JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
9732
9733  026246                                    BGNSEG
9734  026246  104404                           TRAP    C$BSEG
9735
9736                                            ;SET CDAL4 TO A ZERO IN CONTROL REGISTER 0.  CDAL4 BEING A 0 WILL ALLOW
9737                                            ;ONLY ONE AND/OR ARRAY TO BE SELECTED AT A TIME.  CDAL3 AND CDAL2 ON A
9738                                            ;ZERO WILL CAUSE THE SIGNAL TRSLO L TO BE ASSERTED WHICH WILL ENABLE THE
9739                                            ;OUTPUTS OF THE TRACE RAM DATA IN BUFFERS.  THESE OUTPUTS ARE USED TO
9740                                            ;ADDRESS THE AND ARRAYS.
9741
9742  026250  105037  002370                    CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
9743  026254  004737  006102                    JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
9744  026260  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
9745  026262                                    ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
9746  026262  104455                           TRAP    C$ERDF
9747  026264  000001                           .WORD   1
9748  026266  000000                           .WORD   0
9749  026270  004604                           .WORD   R0EROR
9750  026272                                    CKLOOP
9751  026272  104406                           TRAP    C$CLP1
9752
9753                                            ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER TRDI 15:0.  ALL ZEROES
9754                                            ;WILL SELECT ADDRESS 0 OF THE AND ARRAY TO BE USED IN THIS TEST.
9755
9756  026274  005037  002414           1$:     CLR     R6LOAD                  ;SETUP TO LOAD ZEROES
9757  026300  004537  006426                    JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
9758  026304  000005                           .WORD   PTER5                   ;SELECT TRDI BITS 15:0
9759
9760                                            ;SET PTER0 IN THE POINTER REGISTER VIA CONTROL REGISTER 2.  THIS WILL
9761                                            ;SELECT THE FIRST AND ARRAY VIA THE SIGNAL PLSLO L.
9762
9763  026306  012737  000000  002376             MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
9764  026314  004737  006134                    JSR     PC,LDRDR2               ;GO LOAD, READ AND CEHCK REGISTER 2
9765  026320  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
9766  026322                                    ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
```

```
9767  026322  104455                          TRAP    C$ERDF
9768  026324  000002                          .WORD   2
9769  026326  000000                          .WORD   0
9770  026330  004704                          .WORD   R2EROR
9771  026332                                  CKLOOP
9772  026332  104406                          TRAP    C$CLP1
9773
9774                                          ;LOAD, READ AND CHECK AND ARRAY RAM WITH DATA PATTERN OF 5.  THIS DATA
9775                                          ;PATTERN WILL SET THE SIGNALS AND1 L AND AND3 L TO THE HIGH STATE AND
9776                                          ;THE SIGNALS AND0 L AND AND2 L TO THE LOW STATE.  WITH AND1 L AND AND3 L
9777                                          ;SET HIGH AND THE SIGNAL ANST L BEING PULSED, A PULSE WILL OCCUR
9778                                          ;ON THE SIGNALS CNDN1 H AND CNDN3 H.  THESE SIGNALS WILL COUNT DOWN
9779                                          ;EVENT COUNTERS 1 AND 3.
9780
9781  026334  012737  000005  002402  2$:     MOV     #5,R4LOAD               ;SETUP DATA PATTERN TO BE LOADED
9782  026342  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
9783  026350  004737  006166                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY
9784  026354  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
9785  026356                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
9786  026356  104455                          TRAP    C$ERDF
9787  026360  000003                          .WORD   3
9788  026362  003550                          .WORD   ANDERR
9789  026364  004720                          .WORD   R4EROR
9790  026366                          3$:     ENDSEG
9791  026366                          10000$:
9792  026366  104405                          TRAP    C$ESEG
9793
9794  026370  005001                          CLR     R1                      ;START EVENT COUNTERS OFF AT 0
9795
9796  026372                          4$:     BGNSEG
9797  026372  104404                          TRAP    C$BSEG
9798  026374  010102                          MOV     R1,R2                   ;COPY STARTING EVENT COUNTER TO WORKING
9799
9800                                          ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0. CDAL7 ON A ONE WILL ALLOW
9801                                          ;THE FOUR FLIP-FLOPS TO BE READ ON THE OR ADDRESS REGISTER LINES ORAD 3:0.
9802
9803  026376  052737  000200  002370          BIS     #CDAL7,R0LOAD           ;SETUP BIT TO BE LOADED
9804  026404  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHEKC REGISTER 0
9805  026410  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
9806  026412                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
9807  026412  104455                          TRAP    C$ERDF
9808  026414  000001                          .WORD   1
9809  026416  000000                          .WORD   0
9810  026420  004604                          .WORD   R0EROR
9811  026422                                  CKLOOP
9812  026422  104406                          TRAP    C$CLP1
9813
9814                                          ;SET AND CLEAR PDAL7 IN CONTROL REGISTER 2. PDAL7 BEING SET WILL
9815                                          ;CLEAR ALL THE EVENT COUNTERS.
9816
9817  026424  052737  000200  002376  5$:     BIS     #PDAL7,R2LOAD           ;SETUP BIT TO BE LOADED
9818  026432  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9819  026436  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
9820  026440                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9821  026440  104455                          TRAP    C$ERDF
9822  026442  000002                          .WORD   2
```

```
9823  026444  000000                          .WORD   0
9824  026446  004704                          .WORD   R2EROR
9825  026450                                  CKLOOP
9826  026450  104406                          TRAP    C$CLP1
9827
9828                                          ;CLEAR PDAL7 AND LOAD ALL EVENT COUNTER REGISTERS AND EVENT COUNTERS
9829                                          ;WITH THE WORKING EVENT COUNT STORED IN GENERAL CPU REGISTER R2.  THE
9830                                          ;SIGNALS ISSUED IN THE FOLLOWING LOOP ARE WPT9 H, WPTA L, WPT10 H,
9831                                          ;WPTB L, WPT11 H, WPTC L, WPT12 H, AND WPTD L.  THESE SIGNALS ARE USED
9832                                          ;TO LOAD THE DATA INTO THE EVENT COUNTER REGISTERS AND EVENT COUNTERS
9833                                          ;ON A WRITE COMMAND TO CONTROL REGISTER 6.
9834
9835  026452  012737  000011  002376  6$:     MOV     #PTER9,R2LOAD           ;SETUP BITS TO BE LOADED
9836  026460  004737  006134          7$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9837  026464  001405                          BEQ     8$                      ;IF LOADED OK THEN CONTINUE
9838  026466                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9839  026466  104455                          TRAP    C$ERDF
9840  026470  000002                          .WORD   2
9841  026472  000000                          .WORD   0
9842  026474  004704                          .WORD   R2EROR
9843  026476                                  CKLOOP
9844  026476  104406                          TRAP    C$CLP1
9845
9846  026500  010277  153652          8$:     MOV     R2,@REG6                ;LOAD EVENT COUNTERS AND REGISTERS
9847  026504  005237  002376                  INC     R2LOAD                  ;UPDATE TO NEXT POINTER
9848  026510  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL COUNTER S LOADED
9849  026516  001360                          BNE     7$                      ;IF NOT THEN LOAD NEXT COUNTER
9850
9851                                          ;RESELECT THE AND ARRAY SO THAT THE SIGNALS AND1 L AND AND3 L WILL BE
9852                                          ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST.
9853
9854  026520  012737  000000  002376  9$:     MOV     #PTER0,R2LOAD           ;SETUP TO SELECT FIRST AND ARRAY
9855  026526  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
9856  026532  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
9857  026534                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9858  026534  104455                          TRAP    C$ERDF
9859  026536  000002                          .WORD   2
9860  026540  000000                          .WORD   0
9861  026542  004704                          .WORD   R2EROR
9862  026544                                  CKLOOP
9863  026544  104406                          TRAP    C$CLP1
9864
9865                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
9866                                          ;CLEARED WILL CAUSE THE SIGNAL TRANST H TO PULSE WHICH WILL CAUSE
9867                                          ;THE SIGNAL ANST L TO PULSE.  THE SIGNAL ANST L BEING PULSED
9868                                          ;WITH THE SIGNALS AND1 L AND AND3 L SET HIGH, WILL CAUSE A PULSE
9869                                          ;OF THE SIGNALS CNDN1 H AND CNDN3 H.  THESE SIGNALS WILL CAUSE EVENT
9870                                          ;COUNTER 1 AND EVENT COUNTER 3 TO COUNT DOWN BY ONE RESPECTIVELY.
9871
9872  026546  004737  006640          10$:    JSR     PC,TRANST               ;GO SET AND CLEAR CDAL6 IN CONTROL REG 0
9873
9874                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REG 2.
9875
9876  026552  004537  006376                  JSR     R5,ASSERT               ;GO ASSERT PTER15
9877  026556  000017                          .WORD   PTER15
9878
```

```
                                        ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTERIS
                                        ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD 3:0
                                        ;WILL BE READ BACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
                                        ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON ORAD 3:0 SIGNAL LINES.
                                        ;THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA A BORROW FROM THE EVENT COUNTERS
                                        ;AND THE SIGNAL ANST L BEING PULSED.

026560  005037  002414        11$:    CLR     R6LOAD                  ;SETUP EXPECTED DATA
026564  005702                        TST     R2                      ;CHECK IF EVENT COUNTER = 0
026566  001003                        BNE     12$                     ;IF NOT THEN A BORROW SHOULD NOT OCCUR
026570  012737  000012  002414        MOV     #12,R6LOAD              ;SETUP TO EXPECT A BORROW FROM COUNTER
                                                                        ;1 AND COUNTER 3 ON SIGNALS FOUT1 L AND
                                                                        ;FOUT3 L.
026576  017737  153554  002420  12$:   MOV     @REG6,R6READ            ;READ FOUT 3:0 BITS ON ORAD 3:0
026604  042737  177760  002420        BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
026612  023737  002414  002420        CMP     R6LOAD,R6READ           ;CHECK EXPECTED RESULTS AGAINST ACTUAL
026620  001405                        BEQ     13$                     ;IF EQUAL THEN CONTINUE
026622                                ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
026622  104455                        TRAP    C$ERDF
026624  000004                        .WORD   4
026626  003213                        .WORD   EVNTCT
026630  005024                        .WORD   EVNTER
026632                                CKLOOP
026632  104406                        TRAP    C$CLP1
026634  005302          13$:    DEC     R2                      ;DECREMENT WORKING EVENT COUNTER
026636  100330                        BPL     9$                      ;IF NOT DONE THEN COUNT DOWN AGAIN

                                        ;WHEN THE FOUT FLIP-FLOP IS CLEARED BY A BORROW, THE EVENT COUNTERS
                                        ;ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE SIGNAL ORST L
                                        ;IS PULSED VIA THE PULSING OF SIGNAL ANST L.  THE FOLLOWING SECTION
                                        ;OF CODE WILL CHECK THAT THIS HAPPENS BY COUNTING DOWN THE EVENT
                                        ;COUNTERS AGAIN

026640  010102                        MOV     R1,R2                   ;RESET EXPECTED CONTENTS OF EVENT CNTRS

                                        ;RESELECT THE AND ARRAY SO THAT THE SIGNALS AND1 L AND AND3 L WILL BE
                                        ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST

026642  012737  000000  002376  14$:    MOV     #PTER0,R6LOAD           ;SETUP BITS TO BE LOADED
026650  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
026654  001405                        BEQ     15$                     ;IF LOADED OK THEN CONTINUE
026656                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
026656  104455                        TRAP    C$ERDF
026660  000002                        .WORD   2
026662  000000                        .WORD   0
026664  004704                        .WORD   R2EROR
026666                                CKLOOP
026666  104406                        TRAP    C$CLP1

                                        ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
                                        ;CLEARED WILL CAUSE A PULSE ON TRANST H WHICH WILL CAUSE THE SIGNAL ANST L
                                        ;TO PULSE.  THE SIGNAL ANST L BEING PULSED WITH THE
                                        ;SIGNALS AND1 L AND AND3 L SET HIGH WILL CAUSE A PULSE ON THE SIGNALS
                                        ;CNDN1 H AND CNDN3 H.  THESE SIGNALS WILL CAUSE EVENT COUNTER 0 AND 2
                                        ;TO BE COUNTED DOWN BY ONE RESPECTIVELY.
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```
9935  026670  004737  006640          15$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
9936
9937                                          ;ASSERT THE SIGNAL PTER15 L IN POINTER REGISTER VIA CONTROL REG 2.
9938
9939  026674  004537  006376                  JSR     R5,ASSERT               ;GO ASSERT PTER15
9940  026700  000017                          .WORD   PTER15
9941
9942                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
9943                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS,
9944                                          ;ORAD 3:0, WILL BE READBACK. IN THIS TEST, CDAL7 IS SET TO A ONE,
9945                                          ;WHICH WILL CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE
9946                                          ;ORAD 3:0 SIGNAL LINES.  THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA THE
9947                                          ;BORROW SIGNAL FROM THE EVENT COUNTERS AND THE SIGNAL ANST L BEING
9948                                          ;PULSED.
9949
9950  026702  005037  002414          16$:    CLR     R6LOAD                  ;SETUP EXPECTED FOUT SIGNALS
9951  026706  005702                          TST     R2                      ;CHECK IF EVENT COUNTER WERE ZERO
9952  026710  001003                          BNE     17$                     ;IF NOT THEN A BORROW SHOULD NOT OCCUR
9953  026712  012737  000012  002414          MOV     #12,R6LOAD              ;SETUP TO EXPECT FOUT1 L AND FOUT3 L
9954                                          ;TO BE SET AS A RESULT OF A BORROW
9955                                          ;ON EVENT COUNTER 1 AND 3
9956
9957  026720  017737  153432  002420  17$:    MOV     @REG6,R6READ            ;READBACK FOUT 3:0 FLIP-FLOPS
9958  026726  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
9959  026734  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED DATA WITH ACTUAL DATA
9960  026742  001405                          BEQ     18$                     ;IF EQUAL THEN CONTINUE
9961  026744                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
9962  026744  104455                          TRAP    C$ERDF
9963  026746  000004                          .WORD   4
9964  026750  003213                          .WORD   EVNTCT
9965  026752  005024                          .WORD   EVNTER
9966  026754                                  CRLOOP
9967  026754  104406                          TRAP    C$CLP1
9968  026756  005302          18$:    DEC     R2                      ;CHECK IF COUNTER WAS 0
9969  026760  100330                          BPL     14$                     ;IF NOT COUNT DOWN EVENT COUNTER AGAIN
9970
9971                                          ;WHEN THE FOUT FLIP-FLOP IS CLEARED BY A BORROW, THE EVENT COUNTERS
9972                                          ;ARE RELOADED FROM THE EVENT COUNTER REGISTERS WHEN THE SIGNAL ORST L
9973                                          ;IS PULSED VIA THE PULSING OF THE SIGNAL ANST L.  THE PREVIOUS SECTION
9974                                          ;OF CODE VERIFIED THAT THIS HAPPENED.
9975
9976                                          ;THE FOLLOWING SECTION OF CODE WILL CHECK THAT THE EVENT COUNTERS CAN BE
9977                                          ;CLEARED BY SETTING AND CLEARING THE SIGNAL PDAL7 IN CONTROL REGISTER 2.
9978                                          ;THE TEST, AFTER SETTING AND CLEARING PDAL7, WILL DO ONE MORE COUNT
9979                                          ;DOWN AND CHECK THAT A BORROW WAS GENERATED FROM COUNTER 1 AND 3.
9980
9981  026762  010102                          MOV     R1,R2                   ;RESET EXPECTED CONTENTS OF EVNT CNTRS
9982
9983                                          ;RESELECT THE AND ARRAY SO THAT THE SIGNALS AND1 L AND AND3 L WILL BE
9984                                          ;SET HIGH.  THE AND ARRAY WAS WRITTEN IN THE FIRST SEGMENT OF THIS TEST.
9985
9986  026764  012737  000200  002376          MOV     #PT RO'PDAL7,R2LOAD     ;SETUP BITS TO BE LOADED
9987  026772  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
9988  026776  001405                          BEQ     19$                     ;IF LOADED OK THEN CONTINUE
9989  027000                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
9990  027000  104455                          TRAP    C$ERDF
```

```
 9991  027002  000002                        .WORD   2
 9992  027004  000000                        .WORD   0
 9993  027006  004704                        .WORD   R2EROR
 9994  027010                                CKLOOP
 9995  027010  104406                        TRAP    C$CLP1
 9996
 9997                                        ;CLEAR PDAL7 IN CONTROL REGISTER 2. THE EVENT COUNTERS SHOULD NOW
 9998                                        ;BE CLEARED. CLEARING PDAL7 WILL ALLOW THE COUNTERS TO BE COUNTED DOWN
 9999
10000  027012  042737  000200  002376  19$:  BIC     #PDAL7,R2LOAD           ;SETUP TO CLEAR PDAL7
10001  027020  004737  006134                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
10002  027024  001405                        BEQ     20$                     ;IF LOADED OK THEN CONTINUE
10003  027026                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10004  027026  104455                        TRAP    C$ERDF
10005  027030  000002                        .WORD   2
10006  027032  000000                        .WORD   0
10007  027034  004704                        .WORD   R2EROR
10008  027036                                CKLOOP
10009  027036  104406                        TRAP    C$CLP1
10010
10011                                       ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  CDAL6 BEING SET AND
10012                                       ;CLEARED WILL CAUSE A PULSE ON TRANST H WHICH WILL CAUSE THE SIGNAL
10013                                       ;ANST L  0 BE PULSED.  THE SIGNAL ANST L BEING PULSED
10014                                       ;WITH THE SIGNALS AND1 L AND AND3 L SET HIGH, WILL CAUSE A PULSE ON
10015                                       ;THE SIGNALS CNDN1 H  AND CNDN3 H.  THESE SIGNALS WILL COUNT DOWN
10016                                       ;EVENT COUNTERS 1 AND 3 RESPECTIVELY.  IF PDAL7 CLEARED THE EVENT
10017                                       ;COUNTERS THEN A BORROW WILL BE GENERATED FROM EVENT COUNTERS 1 AND 3.
10018
10019  027040  004737  006640          20$:  JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10020
10021                                       ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REG 2.
10022
10023  027044  004537  006376                JSR     R5,ASSERT               ;GO ASSERT PTER15
10024  027050  000017                        .WORD   PTER15
10025
10026                                       ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
10027                                       ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD
10028                                       ;3:0 WILL BE READBACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
10029                                       ;CAUSE THE FOUR FLIP-FLOPS 3:0 TO BE READBACK ON THE ORAD 3:0 SIGNAL
10030                                       ;LINES.  HAVING SET AND CLEARED PDAL7, TO CLEAR THE EVENT COUNTERS, AND
10031                                       ;ISSUING A COUNT DOWN TO EVENT COUNTERS 1 AND 3, FOUT FLIP FLOPS 1 AND
10032                                       ;3 SHOULD BE CLEARED AS A RESULT OF A BORROW AND THE COUNT DOWN PULSE.
10033
10034  027052  012737  000012  002414  21$:  MOV     #12,R6LOAD              ;SETUP TO EXPECT FOUT1 L AND FOUT3 L
10035                                                                        ;TO BE SET AS A RESULT OF A BORROW
10036  027060  017737  153272  002420        MOV     @REG6,R6READ            ;READBACK FOUT 3:0 FLIP-FLOPS
10037  027066  042737  177760  002420        BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
10038  027074  023737  002414  002420        CMP     R6LOAD,R6READ           ;CHECK EXPECTED FOUTS AGAINST ACTUAL
10039  027102  001404                        BEQ     22$                     ;IF THE SAME THEN CONTINUE
10040  027104                                ERRDF   4,EVNTCL,EVNTER         ;PDAL7 FAILED TO CLEAR EVENT COUNTERS
10041  027104  104455                        TRAP    C$ERDF
10042  027106  000004                        .WORD   4
10043  027110  003254                        .WORD   EVNTCL
10044  027112  005024                        .WORD   EVNTER
10045  027114                          22$:  ENDSEG
10046  027114                          1000$:
```

```
10047  027114  104405                          TRAP    C$ESEG
10048
10049  027116  005701                          TST     R1              ;CHECK IF FIRST DATA PATTERN
10050  027120  001003                          BNE     23$             ;IF NOT THEN ROTATE PATTERN LEFT ONCE
10051  027122  005201                          INC     R1              ;SET PATTERN TO A ONE
10052  027124  000137  026372                  JMP     4$              ;GO DO SEQUENCE WITH THIS PATTERN
10053  027130  006301                  23$:    ASL     R1              ;ARITHMATIC SHIFT LEFT ONCE
10054  027132  032701  000400                  BIT     #400,R1         ;CHECK IF PATTERN GREATER THEN 256
10055  027136  001002                          BNE     24$             ;IF YES THEN CHECK IF DONE
10056  027140  000137  026372                  JMP     4$              ;GO DO TEST AGAIN WITH ROTATED PATTERN
10057  027144  105701                  24$:    TSTB    R1              ;CHECK IF PATTERN WAS FLOATTING ONE
10058  027146  001004                          BNE     25$             ;IF NOT THEN END OF TEST
10059  027150  012701  000125                  MOV     #125,R1         ;SETUP TO DO 125 AND 252 PATTERNS
10060  027154  000137  026372                  JMP     4$              ;GO DO TEST WITH 125 FIRST
10061
10062  027160                  25$:    ENDTST
10063  027160                  L10161:
10064  027160  104401                          TRAP    C$ETST
10065
```

```
                                .SBTTL  TEST 56: CHECK CDAL0 TO LOAD EVENT COUNTERS 3:0

                                ;++
                                ; THIS TEST WILL CHECK THAT THE SIGNAL CDAL0, WHEN SET AND CLEARED, WILL CAUSE
                                ; THE EVENT COUNTERS TO BE LOADED FROM THE EVENT COUNTER REGISTER. TO DO THIS,
                                ; THE TEST WILL LOAD ALL EVENT COUNTERS AND REGISTERS WITH 377 OCTAL.  THE
                                ; TEST WILL THEN SET AND CLEAR THE SIGNAL PDAL7 IN CONTROL REGISTER 2. SETTING
                                ; AND CLEARING THE SIGNAL PDAL7 WILL ZERO THE EVENT COUNTERS.  THE TEST WILL
                                ; THEN SET AND CLEAR THE SIGNAL CDAL0 IN CONTROL REGISTER 0.  SETTING AND CLEAR-
                                ; ING CDAL0 SHOULD CAUSE THE EVENT COUNTERS TO BE RELOADED FROM THE EVENT COUNTER
                                ; REGISTERS.  TO TEST THAT THE EVENT COUNTERS WERE RELOADED FROM THE EVENT COUNTER
                                ; REGISTERS, THE TEST WILL COUNT DOWN ALL THE EVENT COUNTERS AT THE SAME
                                ; TIME CHECKING THAT NO BORROWS ARE GENERATED UNTIL THE EVENT COUNTERS HAVE BEEN
                                ; COUNTED DOWN 400 OCTAL TIMES.

027162                                  BGNTST
027162                          T56::
027162  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER

027166                                  BGNSEG
027166  104404                          TRAP    C$BSEG

                                ;SET CDAL4 TO A ZERO IN CONTROL REGISTER 0.  CDAL4 H ON A ZERO WILL
                                ;ALLOW ONLY ONE AND/OR ARRAY RAM TO BE SELECTED AT A TIME.  CDAL3 H AND
                                ;CDAL2 H WILL BE SET TO ZEROES TO CAUSE THE SIGNAL TRSL0 L TO BE ASSERTED
                                ;WHICH WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS.  THESE
                                ;OUTPUTS ARE USED TO ADDRESS THE AND ARRAYS.

027170  105037  002370                   CLRB    R0LOAD                  ;SETUP TO CLEAR LOW BYTE OF REG 0
027174  004737  006102                   JSR     PC,LDRDR0               ;LOAD, READ AND CHECK REGISTER 0
027200  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
027202                                   ERRDF   1,,R0EROR               ;CONTROL REGISTER 0 NOT EQUAL EXPECTED
027202  104455                          TRAP    C$ERDF
027204  000001                          .WORD   1
027206  000000                          .WORD   0
027210  004604                          .WORD   R0EROR
027212                                  CKLOOP
027212  104406                          TRAP    C$CLP1

                                ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER TRDI 15:0.  ALL ZEROES
                                ;WILL SELECT ADDRESS 0 OF THE AND ARRAY TO BE USED IN THIS TEST.

027214  005037  002414          1$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
027220  004537  006426                   JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
027224  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0

                                ;SET PTER0 L TO THE LOW STATE IN THE POINTER REGISTER BY LOADING THE
                                ;APPROPRIATE BIT PATTERN IN CONTROL REGISTER 2.  THIS WILL SELECT THE
                                ;FIRST AND ARRAY RAM VIA THE SIGNAL PSL0 L.

027226  012737  000000  002376           MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
027234  004737  006134                   JSR     PC,LDRDR2               ;LOAD, READ AND CHECK REGISTER 2
027240  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
027242                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
027242  104455                          TRAP    C$ERDF
027244  000002                          .WORD   2
```

```
10122  027246  000000                          .WORD   0
10123  027250  004704                          .WORD   R2EROR
10124  027252                                  CKLOOP
10125  027252  104406                          TRAP    C$CLP1
10126
10127                                          ;LOAD, READ AND CHECK THE FIRST AND ARRAY LOCATION WITH A DATA PATTERN
10128                                          ;OF ALL ZEROES.  THIS DATA PATTERN WILL SET THE SIGNALS ANDO L, AND1 L,
10129                                          ;AND2 L AND AND3 L TO THE HIGH STATE.  WHEN THESE SIGNALS ARE SET HIGH
10130                                          ;AND THE SIGNAL ANST L IS PULSED, PULSES WILL OCCUR ON THE SIGNALS
10131                                          ;CNDNO H, CNDN1 H, CNDN2 H AND CNDN3 H.  THESE PULSES WILL CAUSE ALL THE
10132                                          ;EVENT COUNTERS TO BE COUNTED DOWN AT THE SAME TIME.
10133
10134  027254  005037  002402          2$:     CLR     R4LOAD                  ;SETUP DATA PATTERN TO BE ALL ZEROES
10135  027260  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
10136  027266  004737  006166                  JSR     PC,LDRDAR               ;LOAD, READ AND CHECK AND ARRAY RAM
10137  027272  001404                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10138  027274                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY RAM DATA ERROR.
10139  027274  104455                          TRAP    C$ERDF
10140  027276  000003                          .WORD   3
10141  027300  003550                          .WORD   ANDERR
10142  027302  004720                          .WORD   R4EROR
10143  027304                          3$:     ENDSEG
10144  027304                          10000$:
10145  027304  104405                          TRAP    C$ESEG
10146
10147  027306                                  BGNSEG
10148  027306  104404                          TRAP    C$BSEG
10149
10150  027310  012701  000377                  MOV     #377,R1                 ;SETUP EVENT COUNTERS WITH ALL ONES
10151  027314  010102                          MOV     R1,R2                   ;SETUP WORKING EVENT COUNTERS
10152
10153                                          ;SET CDAL7 H TO A ONE IN CONTROL REGISTER 0 AND ALL OTHER BITS TO A
10154                                          ;ZERO.  CDAL7 H ON A ONE WILL ALLOW THE FOUT FLIP-FLOPS TO BE READ
10155                                          ;ON THE OR ADDRESS REGISTER BITS ORAD 3:0 LATER ON IN THIS TEST.
10156
10157  027316  112737  000200  002370          MOVB    #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
10158  027324  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10159  027330  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
10160  027332                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
10161  027332  104455                          TRAP    C$ERDF
10162  027334  000001                          .WORD   1
10163  027336  000000                          .WORD   0
10164  027340  004604                          .WORD   ROEROR
10165  027342                                  CKLOOP
10166  027342  104406                          TRAP    C$CLP1
10167
10168                                          ;THE FOLLOWING LOOP WILL LOAD ALL EVENT COUNTER REGISTERS AND EVENT
10169                                          ;COUNTERS WITH THE VALUE 377 OCTAL
10170
10171  027344  012737  000011  002376  4$:     MOV     #PTER9,R2LOAD           ;GET VALUE TO SELECT EVENT COUNTER 0
10172  027352  004737  006134          5$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 0
10173  027356  001405                          BEQ     6$                      ;IF LOADED OK THEN CONTINUE
10174  027360                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10175  027360  104455                          TRAP    C$ERDF
10176  027362  000002                          .WORD   2
10177  027364  000000                          .WORD   0
```

```
10178  027366  004704                          .WORD   R2EROR
10179  0273 J                                  CKLOOP
10180  027370  104406                          TRAP    C$CLP1
10181  027372  010177  152760          6$:     MOV     R1,@REG6                ;LOAD EVENT COUNTER REGISTER AND EVENT
10182                                                                          ;COUNTER WITH 377
10183  027376  005237  002376                  INC     R2LOAD                  ;UPDATE POINTER SELECT BY ONE
10184  027402  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL EVENT COUNTERS LOADED
10185  027410  001360                          BNE     5$                      ;IF NOT THEN LOAD NEXT EVENT COUNTER
10186
10187                                          ;CLEAR EVENT COUNTERS BY SETTING AND CLEARING PDAL7 IN CONTROL REG 2.
10188
10189  027412  052737  000200  002376          BIS     #PDAL7,R2LOAD           ;SETUP BIT TO BE LOADED
10190  027420  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10191  027424  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
10192  027426                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10193  027426  104455                          TRAP    C$ERDF
10194  027430  000002                          .WORD   2
10195  027432  000000                          .WORD   0
10196  027434  004704                          .WORD   R2EROR
10197  027436                                  CKLOOP
10198  027436  104406                          TRAP    C$CLP1
10199
10200                                          ;CLEAR PDAL7 IN CONTROL REGISTER 2
10201
10202  027440  042737  000200  002376  7$:     BIC     #PDAL7,R2LOAD           ;SETUP TO CLEAR PDAL7
10203  027446  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10204  027452  001405                          BEQ     8$                      ;IF LOADED OK THEN CONTINUE
10205  027454                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10206  027454  104455                          TRAP    C$ERDF
10207  027456  000002                          .WORD   2
10208  027460  000000                          .WORD   0
10209  027462  004704                          .WORD   R2EROR
10210  027464                                  CKLOOP
10211  027464  104406                          TRAP    C$CLP1
10212
10213                                          ;SET AND CLEAR CDAL0 IN CONTROL REGISTER 0 TO RELOAD THE  VENT COUNTERS
10214                                          ;WITH THE CONTENTS OF THE EVENT COUNTER REGISTERS.  THE EVENT COUNTER
10215                                          ;REGISTERS WERE PREVIOUSLY LOADED WITH 377 OCTAL.
10216
10217  027466  052737  000001  002370  8$:     BIS     #CDAL0,ROLOAD           ;SETUP BIT TO BE LOADED
10218  027474  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10219  027500  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
10220  027502                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10221  027502  104455                          TRAP    C$ERDF
10222  027504  000001                          .WORD   1
10223  027506  000000                          .WORD   0
10224  027510  004604                          .WORD   R0EROR
10225  027512                                  CKLOOP
10226  027512  104406                          TRAP    C$CLP1
10227
10228                                          ;SET CDAL0 H TO A ZERO IN CONTROL REGISTER 0.  CDAL7 H HAS ALREADY BEEN
10229                                          ;SET TO A ONE PREVIOUSLY IN THIS TEST TO ENABLE THE FOUT FLIP-FLOPS
10230                                          ;TO THE OR ADDRESS LINES ORAD 3:0.  CDAL4 H WAS PREVIOUSLY SET TO A ZERO
10231                                          ;TO ENABLE ONLY ONE AND/OR ARRAY RAM TO BE SELECTED AT ONE TIME.
10232
10233  027514  042737  000001  002370  9$:     BIC     #CDAL0,ROLOAD           ;SETUP BIT TO BE CLEARED
```

```
10234  027522  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ, AND CHECK REGISTER 0
10235  027526  001405                          BEQ     10$                     ;IF LOADED OK THEN CONTINUE
10236  027530                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10237  027530  104455                          TRAP    C$ERDF
10238  027532  000001                          .WORD   1
10239  027534  000000                          .WORD   0
10240  027536  004604                          .WORD   R0EROR
10241  027540                                  CKLOOP
10242  027540  104406                          TRAP    C$CLP1
10243
10244                                          ;SELECT THE AND ARRAY WRITTEN PREVIOULSY BY LOADING CONTROL REGISTER
10245                                          ;2 BITS WITH DATA TO ASSERT THE SIGNAL PTER0 L IN THE POINTER REGISTER.
10246                                          ;THE AND ARRAY SELECTED WILL BE THAT ONE SELECTED BY THE SIGNAL PSL0 L.
10247                                          ;LOCATION 0 OF THE AND ARRAY WAS WRITTEN PREVIOUSLY WITH A DATA PATTERN
10248                                          ;OF ALL ZEROES, THEREFORE ALL THE OUTPUTS OF THAT RAM SHOULD BE ASSERTED
10249                                          ;HIGH THUS ASSERTING THE SIGNALS AND 3:0 L TO THE HIGH STATE.
10250
10251  027542  012737  000000  002376  10$:    MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
10252  027550  004737  006134                  JSR     PC,LDRDR2               ;LOAD, READ AND CHECK REGISTER 2
10253  027554  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10254  027556                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10255  027556  104455                          TRAP    C$ERDF
10256  027560  000002                          .WORD   2
10257  027562  000000                          .WORD   0
10258  027564  004704                          .WORD   R2EROR
10259  027566                                  CKLOOP
10260  027566  104406                          TRAP    C$CLP1
10261
10262                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
10263                                          ;CLEARED WILL CAUSE THE SIGANL TRANST H TO PULSE WHICH WILL CAUSE THE
10264                                          ;SIGNAL ANST L TO BE PULSED.  THE SIGNAL ANST L BEING PULSED
10265                                          ;WITH THE SIGNALS AND 3:0 L SET HIGH WILL CAUSE A PULSE ON THE SIGNALS
10266                                          ;CNDN0 H, CNDN1 H, CNDN2 H AND CNDN3 H.  THESE SIGNALS WILL CAUSE EVENT
10267                                          ;COUNTERS 0, 1, 2, AND 3 TO BE COUNTED DOWN RESPECTIVELY.
10268
10269  027570  004737  006640          11$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10270
10271                                          ;ASSER THE SIGNAL PTER15 L IN POINTER REGISTER VIA CONTROL REGISTER 2
10272
10273  027574  004537  006376                  JSR     R5,ASSERT               ;GO ASSERT PTER15
10274  027600  000017                          .WORD   PTER15
10275
10276                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
10277                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS
10278                                          ;ORAD 3:0 WILL BE READBACK.  IN THIS TEST, CDAL7 IS SET TO A ONE,
10279                                          ;WHICH WILL CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE ORAD
10280                                          ;3:0 SIGNAL LINES.  THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA THE BORROW
10281                                          ;SIGNAL FROM THE EVENT COUNTERS AND THE SIGNAL ANST L BEING PULSED.
10282
10283  027602  005037  002414          12$:    CLR     F6LOAD                  ;SETUP TO EXPECT NO BORROW
10284  027606  005702                          TST     F2                      ;CHECK IF EVENT COUNTER WAS 0
10285  027610  001003                          BNE      3$                     ;IF NOT THEN NO BORROW EXPECTED
10286  027612  012737  000017  002414          MOV     #17,R6LOAD              ;SETUP TO EXPECT BORROWS FROM EACH
10287                                                                          ;EVENT COUNTER
10288  027620  017737  152532  002420  13$:    MOV     @REG6,R6READ            ;READBACK FOUT 3:0 OR ORAD 3:0 LINES
10289  027626  042737  177760  002420          BIC     #177760,R6READ          ;CLEAR UNWANTED BITS
```

```
10290  027634  023737  002414  002420          CMP     R6LOAD,R6READ           ;CHECK EXPECTED AGAINST ACTUAL
10291  027642  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
10292  027644                                  ERRDF   4,EVNTRL,EVNTER         ;CDALO FAILED TO RELOAD EVENT COUNTERS
10293  027644  104455                          TRAP    C$ERDF
10294  027646  000004                          .WORD   4
10295  027650  003321                          .WORD   EVNTRL
10296  027652  005024                          .WORD   EVNTER
10297  027654                                  CKLOOP
10298  027654  104406                          TRAP    C$CLP1
10299
10300  027656  005302                  14$:    DEC     R2                      ;DECREMENT WORKING COUNTER
10301  027660  100330                          BPL     10$                     ;IF NOT MINUS THEN COUNT DOWN AGAIN
10302  027662                                  ENDSEG
10303  027662                          10001$:
10304  027662  104405                          TRAP    C$ESEG
10305
10306  027664                                  ENDTST
10307  027664                          L10162:
10308  027664  104401                          TRAP    C$ETST
10309
```

```
10310                                   .SBTTL  TEST 57: FUNCTION SELECT F/F TEST (FUSL7-FUSL3-FUSL1)
10311
10312                                   ;++
10313                                   ; THIS TEST WILL CHECK THAT FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3, AND FUSL1
10314                                   ; CAN BE SET TO A ONE AND THAT FUNCTION SELECT FLIP-FLOPS FULS2 AND FUSLO CAN
10315                                   ; BE SET TO A ZERO.  THE FLIP-FLOPS ARE SET TO THE STATE MENTIONED VIA THE DATA
10316                                   ; FROM THE OR ARRAY RAM AND THE SIGNAL ORST L BEING PULSED.  AFTER
10317                                   ; CHECKING THAT THE FUNCTION SELECT FLIP-FLOPS ARE IN THE CORRECT STATE VIA
10318                                   ; CONTROL REGISTER 4 AND CONTROL REGISTER 6, THE TEST WILL SET THE SIGNAL PDAL5
10319                                   ; TO A ZERO IN CONTROL REGISTER 2.  PDAL5 ON A ZERO WILL PRESET THE FLIP-FLOPS
10320                                   ; TO A ZERO STATE.  THE TEST WILL THEN VERIFY THAT THE FLIP-FLOPS CLEARED BY
10321                                   ; READING CONTROL REGISTER 4 AND CONTROL REGISTER 6 AGAIN.
10322                                   ;--
10323
10324  027666                                   BGNTST
10325  027666                           T57::
10326  027666  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
10327
10328  027672                                   BGNSEG
10329  027672  104404                          TRAP    C$BSEG
10330
10331                                           ;CLEAR LOW BYTE OF CONTROL REGISTER 0.  CDAL7 CLEARED WILL ENABLE THE
10332                                           ;OUTPUTS OF THE OR ADDRESS REGISTER.  CDAL4 BEING A 0 WILL ENABLE ONLY
10333                                           ;ONE AND/OR ARRAY RAM TO BE SELECTED VIA THE POINTER REGISTER.  IN THIS
10334                                           ;TEST, PTER15 L WILL SELECT THE OR ARRAY RAM.
10335
10336  027674  105037  002370                  CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
10337  027700  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10338  027704  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
10339  027706                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
10340  027706  104455                          TRAP    C$ERDF
10341  027710  000001                          .WORD   1
10342  027712  000000                          .WORD   0
10343  027714  004604                          .WORD   ROEROR
10344  027716                                   CKLOOP
10345  027716  104406                          TRAP    C$CLP1
10346
10347                                           ;SETUP BITS IN CONTROL REGISTER 2 TO ASSERT THE SIGNAL PTER15 L IN THE
10348                                           ;POINTER REGISTER.
10349
10350  027720  004537  006376          1$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
10351  027724  000017                          .WORD   PTER15
10352
10353                                           ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH ALL ZEROES.  ON A WRITE
10354                                           ;COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A
10355                                           ;PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH WILL LOAD THE OR
10356                                           ;ADDRESS REGISTER.  ON A READ TO CONTROL REGISTER 6 WITH THE SIGNAL
10357                                           ;PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT15 H WHICH
10358                                           ;WILL READ THE DATA FROM THE OR ADDRESS REGISTER.
10359
10360  027726  005037  002414          2$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
10361  027732  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO READ LOW 4 BITS
10362  027740  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REGISTER 6
10363  027744  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10364  027746                                   ERRDF   4,ORADER,RO26ER         ;OR ADDRESS REG NOT EQUAL ZERO
10365  027746  104455                          TRAP    C$ERDF
```

```
10366  027750  000004                          .WORD   4
10367  027752  003161                          .WORD   ORADER
10368  027754  004734                          .WORD   RU26ER
10369  027756                                  CKLOOP
10370  027756  104406                          TRAP    C$CLP1
10371
10372                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
10373                                          ;REGISTER WITH A DATA PATTERN EQUAL TO 252.
10374
10375  027760  012737  000252  002402  3$:     MOV     #252,R4LOAD             ;SETUP THE DATA TO BE LOADED
10376  027766  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP MASK TO IGNORE UNWANTED BITS
10377  027774  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY DATA
10378  030000  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
10379  030002                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR
10380  030002  104455                          TRAP    C$ERDF
10381  030004  000003                          .WORD   3
10382  030006  003512                          .WORD   ORDATA
10383  030010  004720                          .WORD   R4EROR
10384  030012                                  CKLOOP
10385  030012  104406                          TRAP    C$CLP1
10386
10387                                          ;DISABLE THE PRESET SIGNAL TO THE FUNCTION SELECT FLIP-FLOPS FUSL7,
10388                                          ;FUSL3, FUSL2, FUSL1, AND FUSL0 BY SETTING THE SIGNAL PDAL5 TO A ONE.
10389
10390  030014  052737  000040  002376  4$:     BIS     #PDAL5,R2LOAD           ;SETUP BIT TO BE LOADED WITH PTER15
10391  030022  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10392  030026  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
10393  030030                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10394  030030  104455                          TRAP    C$ERDF
10395  030032  000002                          .WORD   2
10396  030034  000000                          .WORD   0
10397  030036  004704                          .WORD   R2EROR
10398  030040                                  CKLOOP
10399  030040  104406                          TRAP    C$CLP1
10400
10401                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  SETTING AND
10402                                          ;CLEARING CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE.
10403                                          ;THIS WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE THE
10404                                          ;SIGNAL ORST L TO PULSE.  THE SIGNAL ORST L BEING PULSED WILL CLOCK
10405                                          ;THE OR ARRAY RAM DATA INTO THE FUNCTION SELECT FLIP-FLOPS.  WITH
10406                                          ;A DATA PATTERN OF 252 IN THE OR ARRAY RAM, FUNCTION SELECT FLIP-FLOPS
10407                                          ;FUSL7, FUSL3 AND FUSL1 SHOULD BE SET HIGH ON THE OUTPUTS AND FUNCTION
10408                                          ;SELECT FLIP-FLOPS FUSL2 AND FUSL0 SHOULD BE SET LOW ON THE OUTPUTS
10409                                          ;WHEN THE SIGNAL ORST L IS PULSED.
10410
10411  030042  004737  006640          5$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10412
10413                                          ;CHECK THAT FUNCTION SELECT FLIP-FLOP FUSL7 IS SET TO A ONE (HIGH)
10414                                          ;BY READING THE OR ARRAY RAM DATA AND FUSL7 IN BIT 12 OF CONTROL
10415                                          ;REGISTER 4.
10416
10417  030046  042737  010000  002406  7$:     BIC     #BIT12,R4MASK           ;SETUP TO READ FULS7
10418  030054  052737  010000  002404          BIS     #BIT12,R4GOOD           ;SETUP TO EXPECT FUSL7 TO EQUAL A 1
10419  030062  004737  006216                  JSR     PC,READR4               ;READ OR ARRAY DATA AND FUSL7
10420  030066  001405                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
10421  030070                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 FLIP-FLOP PROBABLY NOT SET
```

```
10422  030070  104455                          TRAP    C$ERDF
10423  030072  000003                          .WORD   3
10424  030074  003601                          .WORD   FUSL7
10425  030076  004720                          .WORD   R4EROR
10426  030100                                  CKLOOP
10427  030100  104406                          TRAP    C$CLP1
10428
10429                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
10430                                          ;2. THE SIGNAL PDAL5 WILL REMAIN SET ALSO
10431
10432  030102  012737  000044  002376  8$:     MOV     #PDAL5!PTER4,R2LOAD     ;SETUP BITS TO BE LOADED
10433  030110  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10434  030114  001405                          BEQ     9$                      ;IF LOADED OK THEN CONTINUE
10435  030116                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10436  030116  104455                          TRAP    C$ERDF
10437  030120  000002                          .WORD   2
10438  030122  000000                          .WORD   0
10439  030124  004704                          .WORD   R2EROR
10440  030126                                  CKLOOP
10441  030126  104406                          TRAP    C$CLP1
10442
10443                                          ;READ FUNCTION SELECT FLIP-FLOPS FUSL 3:0 VIA CONTROL REGISTER 6.
10444                                          ;FUSL3 AND FUSL1 SHOULD BE SET TO A ONE AND FUSL2 AND FUSL0 SHOULD
10445                                          ;BE SET TO A ZERO.
10446
10447  030130  012737  120000  002414  9$:     MOV     #BIT15!BIT13,R6LOAD     ;SETUP EXPECTED BITS TO BE SET
10448  030136  012737  007777  002416          MOV     #007777,R6MASK          ;SETUP TO IGNORE TRDI BITS
10449  030144  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK FUSL 3:0 FLIP-FLOPS
10450  030150  001405                          BEQ     10$                     ;IF EQUAL EXPECTED THEN CONTINUE
10451  030152                                  ERRDF   4,FUSL30,ALLREG         ;FUSL3 + FUSL1 NOT 1 OR OTHER BITS SET
10452  030152  104455                          TRAP    C$ERDF
10453  030154  000004                          .WORD   4
10454  030156  003365                          .WORD   FUSL30
10455  030160  004750                          .WORD   ALLREG
10456  030162                                  CKLOOP
10457  030162  104406                          TRAP    C$CLP1
10458
10459                                          ;CLEAR THE SIGNAL PDAL5 IN CONTROL REGISTER 2. PDAL5 ON A ZERO WILL
10460                                          ;CAUSE THE FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL 3:0 TO BE PRESET TO
10461                                          ;THE ZERO STATE.
10462
10463  030164  042737  000040  002376  10$:    BIC     #PDAL5,R2LOAD           ;CLEAR PDAL5 LEAVE PTER4 SET
10464  030172  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10465  030176  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10466  030200                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10467  030200  104455                          TRAP    C$ERDF
10468  030202  000002                          .WORD   2
10469  030204  000000                          .WORD   0
10470  030206  004704                          .WORD   R2EROR
10471  030210                                  CKLOOP
10472  030210  104406                          TRAP    C$CLP1
10473
10474                                          ;CHECK FUNCTION SELECT FLIP-FLOPS FUSL 3:0 TO BE 0.  THE FLIP-FLOPS
10475                                          ;SHOULD BE CLEARED BY THE SIGNAL PDAL5 BEING A ZERO.
10476
10477  030212  005037  002414          11$:    CLR     R6LOAD                  ;BITS 15:12 SHOULD BE A 0
```

```
10478  030216  004737  006256                  JSR     PC,READR6               ;CHECK FUSL 3:0 TO BE ZERO
10479  030222  001405                          BEQ     12$                     ;IF FUSL 3:0 EQUALS 0 THEN CONTINUE
10480  030224                                  ERRDF   4,FUSL30,ALLREG         ;FUSL 3:0 NOT 0 WHEN PDAL5 = 0
10481  030224  104455                          TRAP    C$ERDF
10482  030226  000004                          .WORD   4
10483  030230  003365                          .WORD   FUSL30
10484  030232  004750                          .WORD   ALLREG
10485  030234                                  CKLOOP
10486  030234  104406                          TRAP    C$CLP1
10487
10488                                          ;RESELECT PTER15 L IN THE POINTER REGISTER. THIS IS DONE TO RECHECK THE
10489                                          ;OR ARRAY RAM DATA AND TO CHECK THAT PDAL5 ON A 0 CLEARED FUSL7 F/F.
10490
10491  030236  004537  006376          12$:    JSR     R5,ASSERT               ;GO ASSERT PTER15
10492  030242  000017                          .WORD   PTER15
10493
10494                                          ;CHECK THAT PDAL5 CLEARED FUSL7 FLIP-FLOP AND THAT THE OR ARRAY RAM
10495                                          ;DATA REMAINED UNCHANGED
10496
10497  030244  042737  010000  002404    13$:  BIC     #BIT12,R4GOOD           ;SET EXPECTED FUSL7 BIT TO A ZERO
10498  030252  004737  006216                  JSR     PC,READR4               ;READ OR ARRAY RAM DATA AND FUSL7
10499  030256  001404                          BEQ     14$                     ;IF DATA AND FULS7 OK THEN CONTINUE
10500  030260                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 PROBABLY NOT CLERED VIA PDAL5
10501  030260  104455                          TRAP    C$ERDF
10502  030262  000003                          .WORD   3
10503  030264  003601                          .WORD   FUSL7
10504  030266  004720                          .WORD   R4EROR
10505  030270                          14$:    ENDSEG
10506  030270                          10000$:
10507  030270  104405                          TRAP    C$ESEG
10508  030272                                  ENDTST
10509  030272                          L10163:
10510  030272  104401                          TRAP    C$ETST
10511
```

```
10512                                   .SBTTL  TEST 58: FUNCTION SELECT F/F TEST (FUSL2-FUSL0)
10513
10514                                   ;+*
10515                                   ;  HIS TEST WILL CHECK THAT FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3, AND FUSL1
10516                                   ; CAN BE SET TO A ZERO AND THAT FUNCTION SELECT FLIP-FLOPS FUSL2 AND FUSL0 CAN
10517                                   ; BE SET TO A ONE.  THE FLIP-FLOPS ARE SET TO THE STATE MENTIONED VIA THE DATA
10518                                   ; FROM THE OR ARRAY RAM AND THE SIGNAL ORST L BEING PULSED.  AFTER
10519                                   ; CHECKING THAT THE FUNCTION SELECT FLIP-FLOPS ARE IN THE CORRECT STATE VIA
10520                                   ; CONTROL REGISTER 4 AND CONTROL REGISTER 6, THE TEST WILL SET THE SIGNAL PDAL5
10521                                   ; TO A ZERO IN CONTROL REGISTER 2.  PDAL5 ON A ZERO WILL PRESET THE FLIP-FLOPS
10522                                   ; TO A ZERO STATE.  THE TEST WILL THEN VERIFY THAT THE FLIP-FLOPS CLEARED BY
10523                                   ; READING CONTROL REGISTER 4 AND CONTROL REGISTER 6 AGAIN.
10524                                   ;--
10525
10526  030274                                   BGNTST
10527  030274                           T58::
10528  030274  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
10529
10530  030300                                   BGNSEG
10531  030300  104404                          TRAP    C$BSEG
10532
10533                                   ;CLEAR LOW BYTE OF CONTROL REGISTER 0.  CDAL7 BEING A 0 WILL ENABLE
10534                                   ;OUTPUTS OF THE OR ADDRESS REGISTER.  CDAL4 BEING A 0 WILL ENABLE ONLY
10535                                   ;ONE AND/OR ARRAY RAM TO BE SELECTED VIA THE POINTER REGISTER.  IN THIS
10536                                   ;TEST, PTER15 L WILL SELECT THE OR ARRAY RAM.
10537
10538  030302  105037  002370                  CLRB    R0LOAD                  ;SETUP BITS TO BE CLEARED
10539  030306  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10540  030312  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
10541  030314                                   ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10542  030314  104455                          TRAP    C$ERDF
10543  030316  000001                          .WORD   1
10544  030320  000000                          .WORD   0
10545  030322  004604                          .WORD   R0EROR
10546  030324                                   CKLOOP
10547  030324  104406                          TRAP    C$CLP1
10548
10549                                   ;SETUP BITS IN CONTROL REGISTER 2 TO ASSERT THE SIGNAL PTER15 L IN THE
10550                                   ;POINTER REGISTER.
10551
10552  030326  004537  006376          1$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
10553  030332  000017                          .WORD   PTER15
10554
10555                                   ;LOAD, READ AND CHECK OR ADDRESS REGISTER WITH ALL ZEROES.  ON A WRITE
10556                                   ;COMMAND TO CONTROL REGISTER 6 WITH THE SIGNAL PTER15 L ASSERTED, A
10557                                   ;PULSE WILL BE ISSUED ON THE SIGNAL WPT15 H WHICH WILL LOAD THE OR
10558                                   ;ADDRESS REGISTER.  ON A READ TO CONTROL REGISTER 6 WITH THE SIGNAL
10559                                   ;PTER15 L ASSERTED, A PULSE WILL BE ISSUED ON THE SIGNAL RPT15 H WHICH
10560                                   ;WILL READ THE DATA FROM THE OR ADDRESS REGISTER.
10561
10562  030334  005037  002414  002416  2$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
10563  030340  012737  177760                  MOV     #177760,R6MASK          ;SETUP TO READ LOW 4 BITS
10564  030346  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK REGISTER 6
10565  030352  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10566  030354                                   ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL ZERO
10567  030354  104455                          TRAP    C$ERDF
```

```
10568  030356  000004                          .WORD   4
10569  030360  003161                          .WORD   ORADER
10570  030362  004734                          .WORD   R026ER
10571  030364                                  CKLOOP
10572  030364  104406                          TRAP    C$CLP1
10573
10574                                          ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
10575                                          ;REGISTER WITH A DATA PATTERN EQUAL TO 125.
10576
10577  03?446  012737  000125  002402  3$:     MOV     #125,R4LOAD             ;SETUP THE DATA TO BE LOADED
10578  03 ?4   012737  177400  002406          MOV     #177400,R4MASK          ;SETUP MASK TO IGNORE UNWANTED BITS
10579  030 02  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY DATA
10580  030406  001405                          BEQ     4$                      ;IF DATA OK THEN CONTINUE
10581  030410                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR
10582  030410  104455                          TRAP    C$ERDF
10583  030412  000003                          .WORD   3
10584  030414  003512                          .WORD   ORDATA
10585  030416  004720                          .WORD   R4EROR
10586  030420                                  CKLOOP
10587  030420  104406                          TRAP    C$CLP1
10588
10589                                          ;DISABLE THE PRESET SIGNAL TO THE FUNCTION SELECT FLIP-FLOPS FUSL7,
10590                                          ;FUSL3, FUSL2, FUSL1, AND FUSL0 BY SETTING THE SIGNAL PDAL5 TO A ONE.
10591
10592  030422  052737  000040  002376  4$:     BIS     #PDAL5,R2LOAD           ;SETUP BIT TO BE LOADED WITH PTER15
10593  030430  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10594  030434  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
10595  030436                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10596  030436  104455                          TRAP    C$ERDF
10597  030440  000002                          .WORD   2
10598  030442  000000                          .WORD   0
10599  030444  004704                          .WORD   R2EROR
10600  030446                                  CKLOOP
10601  030446  104406                          TRAP    C$CLP1
10602
10603                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  SETTING AND
10604                                          ;CLEARING CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L TO PULSE.
10605                                          ;THIS WILL THEN CAUSE THE SIGNAL ANST L TO PULSE WHICH WILL CAUSE
10606                                          ;THE SIGNAL ORST L TO PULSE.  THE SIGNAL ORST L BEING PULSED WILL
10607                                          ;CLOCK THE OR ARRAY RAM DATA INTO THE FUNCTION SELECT FLIP-FLOPS.
10608                                          ;WITH A DATA PATTERN OF 125 IN THE OR ARRAY RAM, FUNCTION SELECT
10609                                          ;FLIP-FLOPS FUSL2 AND FUSL0 SHOULD BE SET HIGH ON THE OUTPUTS AND
10610                                          ;FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL3 AND FUSL1 SHOULD BE SET
10611                                          ;LOW ON THE OUTPUTS WHEN THE SIGNAL ORST L IS PULSED.
10612
10613  030450  004737  006640          5$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10614
10615                                          ;CHECK THAT FUNCTION SELECT FLIP-FLOP FUSL7 IS SET TO A ZERO (LOW)
10616                                          ;BY READING THE OR ARRAY RAM DATA AND FUSL7 IN BIT 12 OF CONTROL
10617                                          ;REGISTER 4.
10618
10619  030454  042737  010000  002406  7$:     BIC     #BIT12,R4MASK           ;SETUP TO READ FULS7
10620  030462  004737  006216                  JSR     PC,READR4               ;READ OR ARRAY DATA AND FUSL7
10621  030466  001405                          BEQ     8$                      ;IF DATA OK THEN CONTINUE
10622  030470                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 FLIP-FLOP PROBABLY NOT CLEARED
10623  030470  104455                          TRAP    C$ERDF
```

```
10624  030472  000003                          .WORD   3
10625  030474  003601                          .WORD   FUSL7
10626  030476  004720                          .WORD   R4EROR
10627  030500                                  CKLOOP
10628  030500  104406                          TRAP    C$CLP1
10629
10630                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
10631                                          ;2. THE SIGNAL PDAL5 WILL REMAIN SET ALSO
10632
10633  030502  012737  000044  002376  8$:     MOV     #PDAL5!PTER4,R2LOAD     ;SETUP BITS TO BE LOADED
10634  030510  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10635  030514  001405                          BEQ     9$                      ;IF LOADED OK THEN CUNTINUE
10636  030516                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10637  030516  104455                          TRAP    C$ERDF
10638  030520  000002                          .WORD   2
10639  030522  000000                          .WORD   0
10640  030524  004704                          .WORD   R2EROR
10641  030526                                  CKLOOP
10642  030526  104406                          TRAP    C$CLP1
10643
10644                                          ;READ FUNCTION SELECT FLIP-FLOPS FUSL 3:0 VIA CONTROL REGISTER 6.
10645                                          ;FUSL2 AND FUSL0 SHOULD BE SET TO A ONE AND FUSL3 AND FUSL1 SHOULD
10646                                          ;BE SET TO A ZERO.
10647
10648  030530  012737  050000  002414  9$:     MOV     #BIT14!BIT12,R6LOAD     ;SETUP EXPECTED BITS TO BE SET
10649  030536  012737  007777  002416          MOV     #007777,R6MASK          ;SETUP TO IGNORE TRDI BITS
10650  030544  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK FUSL 3:0 FLIP-FLOPS
10651  030550  001405                          BEQ     10$                     ;IF EQUAL EXPECTED THEN CONTINUE
10652  030552                                  ERRDF   4,FUSL30,ALLREG         ;FUSL2 + FUSL0 NOT 1 OR OTHER BITS SET
10653  030552  104455                          TRAP    C$ERDF
10654  030554  000004                          .WORD   4
10655  030556  003365                          .WORD   FUSL30
10656  030560  004750                          .WORD   ALLREG
10657  030562                                  CKLOOP
10658  030562  104406                          TRAP    C$CLP1
10659
10660                                          ;CLEAR THE SIGNAL PDAL5 IN CONTROL REGISTER 2. PDAL5 ON A ZERO WILL
10661                                          ;CAUSE THE FUNCTION SELECT FLIP-FLOPS FUSL7, FUSL 3:0 TO BE PRESET TO
10662                                          ;THE ZERO STATE.
10663
10664  030564  042737  000040  002376  10$:    BIC     #PDAL5,R2LOAD           ;CLEAR PDAL5 LEAVE PTER4 SET
10665  030572  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10666  030576  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10667  030600                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10668  030600  104455                          TRAP    C$ERDF
10669  030602  000002                          .WORD   2
10670  030604  000000                          .WORD   0
10671  030606  004704                          .WORD   R2EROR
10672  030610                                  CKLOOP
10673  030610  104406                          TRAP    C$CLP1
10674
10675                                          ;CHECK FUNCTION SELECT FLIP-FLOPS FUSL 3:0 TO BE 0.  THE FLIP-FLOPS
10676                                          ;SHOULD BE CLEARED BY THE SIGNAL PDAL5 BEING A ZERO.
10677
10678  030612  005037  002414          11$:    CLR     R6LOAD                  ;BITS 15:12 SHOULD BE A 0
10679  030616  004737  006256                  JSR     PC,READR6               ;CHECK FUSL 3:0 TO BE ZERO
```

```
10680  030622  001405                  BEQ     12$                     ;IF FUSL 3:0 EQUALS 0 THEN CONTINUE
10681  030624                          ERRDF   4,FUSL30,ALLREG         ;FUSL 3:0 NOT 0 WHEN PDAL5 = 0
10682  030624  104455                  TRAP    C$ERDF
10683  030626  000004                  .WORD   4
10684  030630  003365                  .WORD   FUSL30
10685  030632  004750                  .WORD   ALLREG
10686  030634                          CKLOOP
10687  030634  104406                  TRAP    C$CLP1
10688
10689                                  ;RESELECT PTER15 L IN THE POINTER REGISTER. THIS IS DONE TO RECHECK THE
10690                                  ;OR ARRAY RAM DATA AND TO CHECK THAT PDAL5 ON A 0 CLEARED FUSL7 F/F.
10691
10692  030636  004537  006376  12$:    JSR     R5,ASSERT               ;GO ASSERT PTER15
10693  030642  000017                  .WORD   PTER15
10694
10695                                  ;CHECK THAT FUSL7 FLIP-FLOP IS STILL CLEARED AND THAT THE OR ARRAY RAM
10696                                  ;DATA REMAINED UNCHANGED
10697
10698  030644  004737  006216  13$:    JSR     PC,READR4               ;READ OR ARRAY RAM DATA AND FUSL7
10699  030650  001404                  BEQ     14$                     ;IF DATA AND FULS7 OK THEN CONTINUE
10700  030652                          ERRDF   3,FUSL7,R4EROR          ;FUSL7 PROBABLY NOT CLERED VIA PDAL5
10701  030652  104455                  TRAP    C$ERDF
10702  030654  000003                  .WORD   3
10703  030656  003601                  .WORD   FUSL7
10704  030660  004720                  .WORD   R4EROR
10705  030662                  14$:    ENDSEG
10706  030662                  10000$:
10707  030662  104405                  TRAP    C$ESEG
10708  030664                          ENDTST
10709  030664                  L10164:
10710  030664  104401                  TRAP    C$ETST
10711
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```
10712                                   .SBTTL  TEST 59: CHECK FUSL7 F/F TO LOAD EVENT COUNTERS
10713
10714                                   ;++
10715                                   ; THIS TEST WILL CHECK THAT THE EVENT COUNTERS WILL GET RELOADED FROM THE EVENT
10716                                   ; COUNTER REGISTERS WHEN THE OUTPUT OF FUNCTION SELECT FLIP-FLOP FUSL7 H IS SET
10717                                   ; TO THE HIGH STATE.  TO CHECK THAT THIS HAPPENS, THE TEST WILL LOAD ALL EVENT
10718                                   ; COUNTER REGISTERS AND EVENT COUNTERS WITH THE VALUE 377 OCTAL.  THE TEST WILL
10719                                   ; COUNT DOWN THE EVENT COUNTERS UNTIL THE EVENT COUNTERS EQUAL 200 OCTAL.  THE
10720                                   ; TEST CHECKS THAT NO BORROWS ARE GENERATED FROM THE EVENT COUNTERS WHEN THE
10721                                   ; EVENT COUNTERS ARE COUNTED DOWN.  THIS IS DONE BY CHECKING THE FOUT 3:0 FLIP-
10722                                   ; FLOPS ON THE ORAD 3:0 SIGNAL LINES.  THE TEST WILL THEN LOAD LOCATION ZERO OF
10723                                   ; THE "OR ARRAY RAM" WITH DATA EQUAL TO 200 OCTAL WHICH WILL CAUSE THE SIGNAL
10724                                   ; "ORO 7 L" TO BE ASSERTED LOW.  THE TEST WILL THEN SET AND CLEAR THE SIGNAL
10725                                   ; CDAL6 WHICH WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED.
10726                                   ; THIS WILL CAUSE THE SIGNAL ANST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL
10727                                   ; ORST L TO BE PULSED.  THE SIGNAL ORST L BEING PULSED WILL CAUSE THE OR
10728                                   ; ARRAY DATA TO BE LOADED INTO FUNCTION SELECT FLIP-FLOPS, THUS SETTING THE
10729                                   ; OUTPUT OF FUSL7 H FLIP-FLOP TO THE HIGH STATE.  WHEN FUSL7 H FLIP-FLOP IS
10730                                   ; SET HIGH, A ONE SHOT WILL BE FIRED WHICH WILL CAUSE THE EVENT COUNTERS TO
10731                                   ; BE LOADED FROM THE EVENT COUNTER REGISTERS.  TO TEST THAT THE EVENT COUNTERS
10732                                   ; WERE RELOADED FROM THE EVENT COUNTER REGISTERS, THE TEST WILL COUNT DOWN THE
10733                                   ; EVENT COUNTERS 400 OCTAL TIMES CHECKING THAT NO BORROWS ARE GENERATED FROM
10734                                   ; THE EVENT COUNTERS UNTIL THE 400TH COUNT DOWN IS ISSUED.
10735                                   ;--
10736
10737  030666                                   BGNTST
10738  030666                           T59::
10739  030666  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
10740
10741  030672                                   BGNSEG
10742  030672  104404                           TRAP    C$BSEG
10743  030674  012701  000377                   MOV     #377,R1                 ;SETUP STARTING EVENT COUNTER
10744  030700  010102                           MOV     R1,R2                   ;COPY STARTING COUNT TO WORKING COUNT
10745
10746                                   ;CLEAR CDAL4 IN CONTROL REGISTER 0 TO SELECT ONLY ONE AND/OR ARRAY RAM
10747
10748  030702  105037  002370                   CLRB    R0LOAD                  ;SETUP BITS TO BE LOADED
10749  030706  004737  006102                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10750  030712  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
10751  030714                                   ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10752  030714  104455                           TRAP    C$ERDF
10753  030716  000001                           .WORD   1
10754  030720  000000                           .WORD   0
10755  030722  004604                           .WORD   R0EROR
10756  030724                                   CKLOOP
10757  030724  104406                           TRAP    C$CLP1
10758
10759                                   ;;THE FOLLOWING LOOP WILL LOAD ALL EVENT COUNTER REGISTERS AND EVENT
10760                                   ;COUNTERS WITH THE VALUE 377 OCATAL.
10761
10762  030726  012737  000011  002376  1$:      MOV     #PTER9,R2LOAD           ;SETUP POINTER TO FIRST EVENT COUNTER
10763  030734  004737  006134          2$:      JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10764  030740  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
10765  030742                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10766  030742  104455                           TRAP    C$ERDF
10767  030744  000002                           .WORD   2
```

```
10768  030746  000000                          .WORD   0
10769  030750  004704                          .WORD   R2EROR
10770  030752                                  CKLOOP
10771  030752  104406                          TRAP    C$CLP1
10772  030754  010277  151376          3$:     MOV     R2,@REG6                ;LOAD EVENT COUNTERS AND REGISTERS
10773  030760  005237  002376                  INC     R2LOAD                  ;UPDATE VALUE FOR POINTER REGISTER
10774  030764  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL COUNTERS LOADED
10775  030772  001360                          BNE     2$                      ;IF NOT THEN LOAD NEXT VALUE
10776
10777                                          ;SET CDAL7 H TO A ONE AND CDAL4 H TO A ZERO IN CONTROL REGISTER 0.
10778                                          ;CDAL7 H ON A ONE WILL ENABLE THE FOUT FLIP-FLOPS TO BE READBACK ON THE
10779                                          ;ORAD 3:0 SIGNAL LINES.  CDAL4 H ON A ZERO WILL ENABLE ONLY ONE AND/OR
10780                                          ;ARRAY RAM TO BE SELECTED AT ONE TIME.
10781
10782  030774  112737  000200  002370  4$:     MOVB    #CDAL7,R0LOAD           ;SETUP BIT TO BE LOADED
10783  031002  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10784  031006  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
10785  031010                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10786  031010  104455                          TRAP    C$ERDF
10787  031012  000001                          .WORD   1
10788  031014  000000                          .WORD   0
10789  031016  004604                          .WORD   R0EROR
10790  031020                                  CKLOOP
10791  031020  104406                          TRAP    C$CLP1
10792
10793                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER BY LOADING THE
10794                                          ;APPROPRIATE BITS IN CONTROL REGISTER 2.  WHEN PTER15 L IS ASSERTED LOW,
10795                                          ;THE OR ADDRESS LINES, ORAD 3:0, WILL BE READBACK ON A READ COMMAND TO
10796                                          ;CONTROL REGISTER 6.  IN THIS PORTION OF THE TEST, THE FOUT FLIP-FLOPS
10797                                          ;ARE ENABLED TO THE OR ADDRESS LINES VIA CDAL7 H.  WHEN PTER15 L IS
10798                                          ;ASSERTED LOW, ALL THE AND ARRAY RAMS ARE DESELECTED.  WHEN ALL THE
10799                                          ;AND ARRAY RAMS ARE DESELECTED, THE AND ARRAY SIGNALS "AND 3:0 L" WILL
10800                                          ;BE ASSERTED HIGH, THUS ALLOWING ALL THE EVENT COUNTERS TO BE COUNTED
10801                                          ;DOWN WHEN THE SIGNAL ANST L IS PULSED.
10802
10803  031022  004537  006376          5$:     JSR     R5,ASSERT               ;GO ASSERT PTER15
10804  031026  000017                          .WORD   PTER15
10805
10806                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
10807                                          ;CLEARED WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED.
10808                                          ;THIS WILL CAUSE THE SIGNAL ANST L TO BE PULSED.  THE SIGNAL ANST L
10809                                          ;BEING PULSED WITH THE SIGNALS AND 3:0 L SET HIGH WILL CAUSE A PULSE
10810                                          ;ON THE SIGNALS CNDN0 H, CNDN1 H, CNDN2 H AND CNDN3 H.  THESE SIGNALS
10811                                          ;WILL CAUSE ALL THE EVENT COUNTERS TO COUNTED DOWN BY 1.
10812
10813  031030  004737  006640          6$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10814
10815                                          ;WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6 WITH PTER15 L
10816                                          ;ASSERTED IN THE POINTER REGISTER, THE OR ADDRESS REGISTER BITS ORAD
10817                                          ;3:0 WILL BE READBACK.  IN THIS TEST, CDAL7 IS SET TO A ONE, WHICH WILL
10818                                          ;CAUSE THE FOUT FLIP-FLOPS 3:0 TO BE READBACK ON THE ORAD 3:0 SIGNAL
10819                                          ;LINES.  THE FOUT FLIP-FLOPS ARE SET/CLEARED VIA THE BORROW SIGNAL FROM
10820                                          ;THE EVENT COUNTERS AND THE SIGNAL ANST L BEING PULSED.
10821
10822  031034  005037  002414                  CLR     R6LOAD                  ;SETUP TO EXPECT NO BORROW FROM EVENT
10823                                                                          ;COUNTERS. THE EVENT COUNTERS WILL BE
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10824                                                                   ;COUNTED DOWN FROM 377 TO 200.
10825  031040  012737  177760  002416          MOV     #177760,R6MASK   ;SETUP TO IGNORE UNWANTED BITS
10826  031046  004737  006256                  JSR     PC,READR6        ;GO READ AND CHECK FOUT 3:0 F/F'S
10827  031052  001405                          BEQ     7$               ;IF NO BORROW THEN CONTINUE
10828  031054                                  ERRDF   4,EVNTCT,EVNTER  ;BORROW OCCURED WHEN NOT EXPECTED
10829  031054  104455                          TRAP    C$ERDF
10830  031056  000004                          .WORD   4
10831  031060  003213                          .WORD   EVNTCT
10832  031062  005024                          .WORD   EVNTER
10833  031064                                  CKLOOP
10834  031064  104406                          TRAP    C$CLP1
10835  031066  005302                  7$:     DEC     R2               ;DECREMENT SIMULATED EVENT COUNTER
10836  031070  022702  000200                  CMP     #200,R2          ;CHECK IF HALF WAY YET
10837  031074  001355                          BNE     6$               ;IF NOT THEN COUNT DOWN AGAIN
10838
10839  031076  010102                          MOV     R1,R2            ;COPY STARTING EVENT COUNT TO WORKING
10840                                                                   ;EVENT COUNTER.
10841
10842                                  ;CLEAR THE SIGNAL CDAL7 IN CONTROL REGISTER 0 TO ENABLE THE OUTPUTS
10843                                  ;OF THE OR ADDRESS REGISTER INSTEAD OF THE FOUT FLIP-FLOPS
10844
10845  031100  042737  000200  002370          BIC     #CDAL7,ROLOAD    ;SETUP BIT TO BE CLEARED
10846  031106  004737  006102                  JSR     PC,LDRDR0        ;GO LOAD, READ AND CHECK REGISTER 0
10847  031112  001405                          BEQ     8$               ;IF LOADED OK THEN CONTINUE
10848  031114                                  ERRDF   1,,R0EROR        ;REGISTER 0 NOT EQUAL EXPECTED
10849  031114  104455                          TRAP    C$ERDF
10850  031116  000001                          .WORD   1
10851  031120  000000                          .WORD   0
10852  031122  004604                          .WORD   R0EROR
10853  031124                                  CKLOOP
10854  031124  104406                          TRAP    C$CLP1
10855
10856                                  ;LOAD, READ AND CHECK THE OR ADDRESS REGISTER WITH ADDRESS OF ZERO.
10857
10858  031126  004737  006250          8$:     JSR     PC,LDRDR6        ;GO LOAD, READ AND CHECK OR ADDRESS REG
10859  031132  001405                          BEQ     9$               ;IF LOADED OK THEN CONTINUE
10860  031134                                  ERRDF   4,ORADER,R026ER  ;OR ADDRESS REG NOT EQUAL TO ZERO
10861  031134  104455                          TRAP    C$ERDF
10862  031136  000004                          .WORD   4
10863  031140  003161                          .WORD   ORADER
10864  031142  004734                          .WORD   R026ER
10865  031144                                  CKLOOP
10866  031144  104406                          TRAP    C$CLP1
10867
10868                                  ;LOAD, READ AND CHECK OR ARRAY RAM LOCATION ADDRESSED BY THE OR ADDRESS
10869                                  ;REGISTER WITH A DATA PATTERN OF 200. THIS DATA PATTERN WILL SET THE
10870                                  ;FUNCTION SELECT FLIP-FLOP FUSL7 TO THE HIGH STATE WHEN THE SIGNAL
10871                                  ;ORST L IS PULSED.
10872
10873  031146  012737  000200  002402  9$:     MOV     #BIT7,R4LOAD     ;SETUP DATA TO BE LOADED
10874  031154  012737  167400  002406          MOV     #167400,R4MASK   ;SETUP TO CHECK FUSL7 AND OR ARRAY DATA
10875  031162  004737  006202                  JSR     PC,LDRDR4        ;LOAD,READ + CHECK OR ARRAY RAM + FUSL7
10876  031166  001405                          BEQ     10$              ;IF LOADED OK THEN CONTINUE
10877  031170                                  ERRDF   3,FUSL7,R4EROR   ;FUSL7 OR OR ARRAY DATA ERROR
10878  031170  104455                          TRAP    C$ERDF
10879  031172  000003                          .WORD   3
```

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10880  031174  003601                          .WORD   FUSL7
10881  031176  004720                          .WORD   R4EROR
10882  031200                                  CKLOOP
10883  031200  104406                          TRAP    C$CLP1
10884
10885                                          ;SET PDAL5 TO A ONE SO THAT THE FUNCTION SELECT FLIP-FLOPS CAN BE SET
10886                                          ;WITH THE OR ARRAY RAM DATA WHEN THE SIGNAL ORST L IS PULSED.
10887
10888  031202  052737  000040  002376  10$:   BIS     #PDAL5,R2LOAD           ;SET PDAL5 AND BITS FOR PTER15
10889  031210  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10890  031214  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
10891  031216                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10892  031216  104455                          TRAP    C$ERDF
10893  031220  000002                          .WORD   2
10894  031222  000000                          .WORD   0
10895  031224  004704                          .WORD   R2EROR
10896  031226                                  CKLOOP
10897  031226  104406                          TRAP    C$CLP1
10898
10899                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  SETTING AND
10900                                          ;CLEARING CDAL6 WILL CAUSE ALL THE EVENT COUNTERS TO BE COUNTED DOWN
10901                                          ;BY ONE WHEN THE SIGNAL ANST L IS PULSED.  WHEN THE SIGNAL ORST L IS
10902                                          ;PULSED, THE FUNCTION SELECT FLIP-FLOPS WILL BE LOADED WITH
10903                                          ;THE DATA FROM THE OR ARRAY RAM, WHICH IN THIS TEST WILL CAUSE FUSL7
10904                                          ;FLIP-FLOP TO BE SET TO THE HIGH STATE.  WHEN FUSL7 FLIP-FLOP IS SET,
10905                                          ;A ONE SHOT WILL BE FIRED WHICH WILL CAUSE THE EVENT COUNTERS TO BE
10906                                          ;RELOADED FROM THE EVENT COUNTER REGISTERS.
10907
10908  031230  004737  006640          11$:   JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10909
10910                                          ;CHECK OR ARRAY RAM DATA AGAIN AND CHECK THAT FUNCTION SELECT FLIP-
10911                                          ;FLOP FUSL7 IS SET TO A ONE.
10912
10913  031234  052737  010000  002404          BIS     #BIT12,R4GOOD           ;SETUP TO EXPECT FUSL7 FLIP-FLOP SET
10914  031242  004737  006216                  JSR     PC,READR4               ;READ AND CHECK FUSL7 + OR ARRAY RAM
10915  031246  001405                          BEQ     12$                     ;IF DATA EQUAL EXPECTED THEN CONTINUE
10916  031250                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 F/F - OR ARRAY RAM DATA ERROR
10917  031250  104455                          TRAP    C$ERDF
10918  031252  000003                          .WORD   3
10919  031254  003601                          .WORD   FUSL7
10920  031256  004720                          .WORD   R4EROR
10921  031260                                  CKLOOP
10922  031260  104406                          TRAP    C$CLP1
10923
10924                                          ;SET PDAL5 TO A 0 IN CONTROL REGISTER 0 TO CLEAR FUSL7 FLIP-FLOP. THE
10925                                          ;EVENT COUNTERS SHOULD HAVE BEEN LOADED WHEN FUSL7 FLIP-FLOP SET.
10926
10927  031262  042737  000040  002376  12$:   BIC     #PDAL5,R2LOAD           ;LEAVE BITS FOR PTER15 IN REG 2
10928  031270  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
10929  031274  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
10930  031276                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
10931  031276  104455                          TRAP    C$ERDF
10932  031300  000002                          .WORD   2
10933  031302  000000                          .WORD   0
10934  031304  004704                          .WORD   R2EROR
10935  031306                                  CKLOOP
```

```
10936  031306  104406                          TRAP    C$CLP1
10937
10938                                          ;CHECK OR ARRAY RAM AGAIN TO CHECK THAT FUNCTION SELECT FLIP-FLOP FUSL7
10939                                          ;FLIP-FLOP CLEARED.
10940
10941  031310  042737  010000  002404  13$:    BIC     #BIT12,R4GOOD           ;SETUP TO CHECK FUSL7 TO BE 0
10942  031316  004737  006216                  JSR     PC,READR4               ;READ AND CHECK FUSL7 + OR ARRAY DATA
10943  031322  001405                          BEQ     14$                     ;IF FUSL7 EQUALS 0 THEN CONTINUE
10944  031324                                  ERRDF   3,FUSL7,R4EROR          ;FUSL7 F/F OR OR ARRAY DATA EROR
10945  031324  104455                          TPAP    C$ERDF
10946  031326  000003                          .WORD   3
10947  031330  003601                          .WORD   FUSL7
10948  031332  004720                          .WORD   R4EROR
10949  031334                                  CKLOOP
10950  031334  104406                          TRAP    C$CLP1
10951
10952                                          ;THE FOLLOWING SECTION OF CODE WILL COUNT DOWN THE EVENT COUNTERS
10953                                          ;TO CHECK THAT THE EVENT COUNTERS WERE RELOADED WHEN FUNCTION SELECT
10954                                          ;FLIP-FLOP FUSL7 WAS SET.  THE EVENT COUNTERS BEFORE THE RELOAD
10955                                          ;CONTAINED 200 OCTAL AND THE EVENT COUNTER REGISTERS CONTAINED 377.
10956
10957                                          ;SET CDAL7 H TO A ONE AND CDAL4 H TO A ZERO IN CONTROL REGISTER 0.
10958                                          ;CDAL7 H ON A ONE WILL ENABLE THE FOUT FLIP-FLOPS TO BE READBACK ON THE
10959                                          ;ORAD 3:0 SIGNAL LINES.  CDAL4 H ON A ZERO WILL ENABLE ONLY ONE AND/OR
10960                                          ;ARRAY RAM TO BE SELECTED AT ONE TIME.
10961
10962  031336  112737  000200  0023?0  '4$:    MOVB    #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
10963  031344  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
10964  031350  001405                          BEQ     15$                     ;IF LOADED OK THEN CONTINUE
10965  031352                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
10966  031352  104455                          TRAP    C$ERDF
10967  031354  000001                          .WORD   1
10968  031356  000000                          .WORD   0
10969  031360  004604                          .WORD   R0EROR
10970  031362                                  CKLOOP
10971  031362  104406                          TRAP    C$CLP1
10972
10973                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER BY LOADING THE
10974                                          ;APPROPRIATE BITS IN CONTROL REGISTER 2.  WHEN PTER15 L IS ASSERTED LOW,
10975                                          ;THE OR ADDRESS LINES, ORAD 3:0, WILL BE READBACK ON A READ COMMAND TO
10976                                          ;CONTROL REGISTER 6.  IN THIS PORTION OF THE TEST, THE FOUT FLIP-FLOPS
10977                                          ;ARE ENABLED TO THE OR ADDRESS LINES VIA CDAL7 H.  WHEN PTER15 L IS
10978                                          ;ASSERTED LOW, ALL THE AND ARRAY RAMS ARE DESELECTED.  WHEN ALL THE
10979                                          ;AND ARRAY RAMS ARE DESELECTED, THE AND ARRAY SIGNALS "AND 3:0 L" WILL
10980                                          ;BE ASSERTED HIGH, THUS ALLOWING ALL THE EVENT COUNTERS TO BE COUNTED
10981                                          ;DOWN WHEN THE SIGNAL ANST L IS PULSED.
10982
10983  031364  004537  006376          15$:    JSR     R5,ASSERT               ;GO ASSERT PTER15
10984  031370  000017                          .WORD   PTER15
10985
10986                                          ;CLOCK THE SIGNAL CDAL6 IN CONTROL REGISTER 0. CDAL6 BEING SET AND
10987                                          ;CLEARED WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED.  THIS
10988                                          ;WILL CAUSE THE SIGNAL ANST L TO BE PULSED.  THE SIGNAL ANST L BEING
10989                                          ;PULSED WITH THE SIGNALS AND 3:0 L SET HIGH WILL CAUSE A PULSE ON THE
10990                                          ;SIGNALS CNDN0 H, CNDN1 H, CNDN2 H AND CNDN3 H WHICH WILL CAUSE THE
10991                                          ;EVENT COUNTERS TO BE COUNTED DOWN BY ONE.
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10992
10993  031372  004737  006640          16$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
10994
10995                                           ;WHEN A READ IS ISSUED TO CONTROL REGISTER 6 WITH THE SIGNAL CDAL7
10996                                           ;ON A ONE, THE FOUT FLIP-FLOPS 3:0 OR READBACK ON THE OR ADDRESS REG-
10997                                           ;ISTER SIGNAL LINES ORAD 3:0.  THE FOUT FLIP-FLOPS ARE SET/CLEARED
10998                                           ;VIA A BORROW FROM THE EVENT COUNTERS AND THE SIGNAL ANST L BEING PULSED
10999
11000  031376  005037  002414                  CLR     R6LOAD                  ;SETUP TO EXPECT NO BORROW
11001  031402  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11002  031410  005702                          TST     R2                      ;CHECK IF COUNTER WAS 0 BEFORE CNT DWN
11003  031412  001003                          BNE     17$                     ;IF NOT THEN DON'T EXPECT BORROWS
11004  031414  012737  000017  002414          MOV     #17,R6LOAD              ;EXPECT A BORROW FROM EACH COUNTER
11005  031422  004737  006256          17$:    JSR     PC,READR6               ;GO READ AND CHECK FOUT 3:0 F/F'S
11006  031426  001405                          BEQ     18$                     ;IF FOUT F/F'S EQUAL EXPECTED - CONT
11007  031430                                  ERRDF   4,EVNTCT,EVNTER         ;FUSL7 FAILED TO RELOAD EVENT COUNTERS
11008  031430  104455                          TRAP    C$ERDF
11009  031432  000004                          .WORD   4
11010  031434  003213                          .WORD   EVNTCT
11011  031436  005024                          .WORD   EVNTER
11012  031440                                  CKLOOP
11013  031440  104406                          TRAP    C$CLP1
11014  031442  005302          18$:    DEC     R2                      ;DECREMENT SIMULATED EVENT COUNTER
11015  031444  100352                          BPL     16$                     ;IF NOT MINUS THEN COUNT DOWN AGAIN
11016  031446                                  ENDSEG
11017  031446                          10000$:
11018  031446  104405                          TRAP    C$ESEG
11019
11020  031450                                  ENDTST
11021  031450                          L10165:
11022  031450  104401                          TRAP    C$ETST
11023
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```
11024                                   .SBTTL  TEST 60: TRACING F/F TEST VIA FUSL0 AND FULS1 F/F'S
11025
11026                                   ;++
11027                                   ; THIS TEST WILL CHECK THAT THE TRACING FLIP-FLOP CAN BE SET BY FUNCTION SELECT
11028                                   ; FUSL0 H FLIP-FLOP AND CLEARED BY FUNCTION SELECT FUSL1 H FLIP-FLOP.  THE TEST
11029                                   ; WILL CHECK THAT THE TRACING FLIP-FLOP IS SET AND CLEARED BY CHECKING THE TRACE
11030                                   ; RAM ADDRESS REGISTER.  THE TRACE RAM ADDRESS REGISTER IS NOT INCREMENTED WHEN
11031                                   ; THE TRACING F/F IS CLEARED AND THE SIGNALS TRANST H AND TRST L ARE PULSED.
11032                                   ; THE TRACE RAM ADDRESS REGISTER IS INCREMENTED WHEN THE TRACING FLIP-FLOP IS
11033                                   ; SET AND THE SIGNALS TRANST H AND TRST L ARE PULSED.  THE FUNCTION SELECT
11034                                   ; FLIP-FLOPS ARE SET AND CLEARED VIA THE OR ARRAY RAM DATA AND THE SIGNAL
11035                                   ; ORST L BEING PULSED.
11036                                   ;--
11037
11038
11039  031452                                   BGNTST
11040  031452                           T60::
11041  031452  004737  005474                   JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
11042
11043  031456                                   BGNSEG
11044  031456  104404                           TRAP    C$BSEG
11045
11046                                           ;SET AND CLEAR CDAL0 IN CONTROL REGISTER 0 TO CLEAR TRACE RAM ADDRESS
11047                                           ;REGISTER AND THE TRACING FLIP-FLOP.  CDAL4 WILL BE SET TO A ZERO TO
11048                                           ;ENABLE ONLY ONE AND/OR ARRAY RAM AT A TIME VIA THE POINTER REGISTER
11049                                           ;PTER SIGNALS.
11050
11051  031460  112737  000001  002370           MOVB    #CDAL0,ROLOAD           ;SETUP BITS TO BE LOADED
11052  031466  004737  006102                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11053  031472  001405                           BEQ     1$                      ;IF LOADED OK THEN GO CLEAR CDAL0
11054  031474                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
11055  031474  104455                           TRAP    C$ERDF
11056  031476  000001                           .WORD   1
11057  031500  000000                           .WORD   0
11058  031502  004604                           .WORD   ROEROR
11059  031504                                   CKLOOP
11060  031504  104406                           TRAP    C$CLP1
11061  031506  042737  000001  002370  1$:      BIC     #CDAL0,ROLOAD           ;SETUP BIT TO BE CLEARED
11062  031514  004737  006102                   JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11063  031520  001405                           BEQ     2$                      ;IF LOADED OK THEN CONTINUE
11064  031522                                   ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
11065  031522  104455                           TRAP    C$ERDF
11066  031524  000001                           .WORD   1
11067  031526  000000                           .WORD   0
11068  031530  004604                           .WORD   ROEROR
11069  031532                                   CKLOOP
11070  031532  104406                           TRAP    C$CLP1
11071
11072                                           ;CLEAR PDAL5 IN CONTROL REGISTER 0 TO PRESET THE OUTPUTS OF THE
11073                                           ;FUNCTION SELECT FLIP-FLOPS TO THE LOW STATE.
11074
11075  031534  012737  000000  002376  2$:      MOV     #PTER0,R2LOAD           ;SETUP BITS TO BE LOADED
11076  031542  004737  006134                   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11077  031546  001405                           BEQ     3$                      ;IF LOADED OK THEN CONTINUE
11078  031550                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11079  031550  104455                           TRAP    C$ERDF
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11080  031552  000002                          .WORD   2
11081  031554  000000                          .WORD   0
11082  031556  004704                          .WORD   R2EROR
11083  031560                                  CKLOOP
11084  031560  104406                          TRAP    C$CLP1
11085
11086                                          ;LOAD PDAL5 INTO CONTROL REGISTER 2 ALONG WITH THE BITS TO SELECT THE
11087                                          ;SIGNAL PTER0 L IN THE POINTER REGISTER.
11088
11089  031562  012737  000040  002376  3$:     MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11090  031570  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11091  031574  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
11092  031576                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11093  031576  104455                          TRAP    C$ERDF
11094  031600  000002                          .WORD   2
11095  031602  000000                          .WORD   0
11096  031604  004704                          .WORD   R2EROR
11097  031606                                  CKLOOP
11098  031606  104406                          TRAP    C$CLP1
11099
11100                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0 TO CHECK THAT THE TRACING
11101                                          ;FLIP-FLOP AND THE FUNCTION SELECT FLIP-FLOP FUSL0 ARE CLEARED.  THE
11102                                          ;FUNCTION SELECT FLIP-FLOPS SHOULD BE LOADED TO THE ZERO STA  WHEN THE
11103                                          ;OR ARRAY RAMS ARE DESELECTED AND THE SIGNAL ORST L IS PULSED.
11104                                          ;SETTING AND CLEARING CDAL6 WILL CAUSE THE SIGNALS TRANST H AND TRST L
11105                                          ;TO BE PULSED WHICH WILL CAUSE THE SIGNAL ANST L TO BE PULSED WHICH
11106                                          ;WILL CAUSE THE SIGNAL ORST L TO BE PULSED.  NO PULSE SHOULD OCCUR ON
11107                                          ;THE SIGNAL CTR L, THEREFORE THE TRACE RAM ADDRESS REGISTER SHOULD NOT
11108                                          ;BE INCREMENTED.
11109
11110  031610  004737  006640          4$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11111
11112                                          ;CHECK TRACE RAM ADDRESS REGISTER TO EQUAL ZERO AS A RESULT OF THE
11113                                          ;SIGNAL CDAL0 BEING SET AND CLEARED.  IF AN ERROR OCCURS CHECK THAT
11114                                          ;THE TRACING FLIP-FLOP AND FUNCTION SELECT FLIP-FLOP FUSL0 ARE IN THE
11115                                          ;LOW LEVEL STATE.
11116
11117  031614  005037  002414                  CLR     R6LOAD                  ;SETUP TO CHECK FOR ADDRESS ZERO
11118  031620  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11119  031626  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK RAM ADDRESS REGISTER
11120  031632  001405                          BEQ     5$                      ;IF EQUAL TO ZERO THEN CONTINUE
11121  031634                                  ERRDF   4,TRADER,R026ER         ;CDAL0 FAILED TO CLEAR TRAM ADDRESS REG.
11122  031634  104455                          TRAP    C$ERDF
11123  031636  000004                          .WORD   4
11124  031640  002462                          .WORD   TRADER
11125  031642  004734                          .WORD   R026ER
11126  031644                                  CKLOOP
11127  031644  104406                          TRAP    C$CLP1
11128
11129                                          ;SET AND CLEAR CDAL6 IN CONTROL REIGSTER 0 TO CHECK THAT FUNCTION
11130                                          ;SELECT FLIP-FLOP, FUSL0 H, D D NOT GET SET WHEN THE SIGNAL ORST L
11131                                          ;WAS PULSED IN THE PREVIOUS  CTION.
11132
11133  031646  004737  006640          5$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11134
11135                                          ;CHECK TRACE RAM ADDRESS  GISTER TO EQUAL A ZERO AS A RESULT OF THE
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11136                                          ;SIGNAL CDAL0 BEING SET AND CLEARED.  IF AN ERROR OCCURS, CHECK THAT
11137                                          ;THE TRACING FLIP-FLOP OUTPUT IS LOW AND THE FUNCTION SELECT FLIP-FLOP,
11138                                          ;FUSL0 H, IS IN THE LOW STATE.
11139
11140  031652  005037  002414                 CLR     R6LOAD                  ;SETUP TO CHECK FOR ADDRESS ZERO
11141  031656  012737  174000  002416         MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11142  031664  004737  006256                 JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
11143  031670  001405                         BEQ     6$                      ;IF EQUAL TO ZERO THEN CONTINUE
11144  031672                                 ERRDF   4,TRADER,R026ER         ;TRACING F/F OR FUSL0 H F/F SET
11145  031672  104455                         TRAP    C$ERDF
11146  031674  000004                         .WORD   4
11147  031676  002462                         .WORD   TRADER
11148  031700  004734                         .WORD   R026ER
11149  031702                                 CKLOOP
11150  031702  104406                         TRAP    C$CLP1
11151
11152                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTROL REGISTER
11153                                          ;2. PDAL5 WILL ALSO BE SET TO A ONE TO ALLOW THE FUNCTION SELECT FLIP-
11154                                          ;FLOPS TO BE CLOCKED WHEN THE SIGNAL ORST L IS PULSED.  PTER15 L
11155                                          ;WILL ALLOW THE OR ADDRESS REGISTER AND OR ARRAY RAMS TO BE WRITTEN AND
11156                                          ;READ.
11157
11158  031704  012737  000057  002376  6$:    MOV     #PDAL5!PTER15,R2LOAD    ;SETUP BITS TO BE LOADED
11159  031712  004737  006134                 JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REIGSTER 2
11160  031716  001405                         BEQ     7$                      ;IF LOADED OK THEN CONTINUE
11161  031720                                 ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11162  031720  104455                         TRAP    C$ERDF
11163  031722  000002                         .WORD   2
11164  031724  000000                         .WORD   0
11165  031726  004704                         .WORD   R2EROR
11166  031730                                 CKLOOP
11167  031730  104406                         TRAP    C$CLP1
11168
11169                                          ;SELECT ADDRES' 0 IN THE OR ARRAY RAM ADDRESS REGISTER.  CDAL7 ON A
11170                                          ;ZERO IN CONTRO_ REGISTER 0 WILL ALLOW THE OR ADDRESS REGISTER TO BE
11171                                          ;READBACK ON A READ COMMAND TO CONTROL REGISTER 6.
11172
11173  031732  005037  002414         7$:    CLR     R6LOAD                  ;SETUP TO LOAD ADDRESS 0
11174  031736  012737  177760  002416         MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11175  031744  004737  006250                 JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11176  031750  001405                         BEQ     8$                      ;IF ADDRESS EQUALS 0 THEN CONTINUE
11177  031752                                 ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER ERROR - ORAD 3:0
11178  031752  104455                         TRAP    C$ERDF
11179  031754  000004                         .WORD   4
11180  031756  003161                         .WORD   ORADER
11181  031760  004734                         .WORD   R026ER
11182  031762                                 CKLOOP
11183  031762  104406                         TRAP    C$CLP1
11184
11185                                          ;LOAD, READ AND CHECK ADDRESS 0 OF THE OR ARRAY RAM WITH A DATA PATTERN
11186                                          ;EQUAL TO ONE.  THIS WILL CAUSE THE SIGNAL "ORO 0 L" TO BE ASSERTED LOW.
11187                                          ;ALL OTHER OR ARRAY RAM DATA BITS WILL BE ASSERTED HIGH.
11188
11189  031764  012737  000001  002402  8$:    MOV     #1,R4LOAD               ;SETUP DATA PATTERN TO BE LOADED
11190  031772  012737  177400  002406         MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
11191  032000  004737  006202                 JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY DATA
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11192  032004  001405                          BEQ     9$                      ;IF DATA EQUALS 1 THEN CONTINUE
11193  032006                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
11194  032006  104455                          TRAP    C$ERDF
11195  032010  000003                          .WORD   3
11196  032012  003512                          .WORD   ORDATA
11197  032014  004720                          .WORD   R4EROR
11198  032016                                  CKLOOP
11199  032016  104406                          TRAP    C$CLP1
11200
11201                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REIGSTER 0.  THIS WILL CAUSE
11202                                          ;THE SIGNALS TRANST H AND TRST L TO BE PULSED WHICH WILL CAUSE THE
11203                                          ;SIGNAL ANST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE
11204                                          ;PULSED.  WHEN THE SIGNAL ORST L IS PULSED, FUSL0 H FLIP-FLOP SHOULD
11205                                          ;BE CLOCKED TO THE HIGH STATE.  NO PULSE SHOULD OCCUR ON THE CTR L
11206                                          ;SIGNAL BECAUSE THE PREVIOUS STATE OF FUSL0 H FLIP-FLOP WAS LOW WHEN
11207                                          ;THE SIGNALS TRANST H AND TRST L WERE PULSED.  THE SIGNALS TRANST H
11208                                          ;AND TRST L WILL CLOCK THE PREVIOUS STATE OF FUSL0 H FLIP-FLOP.
11209
11210  032020  004737  006640          9$:     JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11211
11212                                          ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11213                                          ;SIGNAL PTER0 L IN THE POINTER REGISTER.  THIS IS DONE TO SETUP FOR
11214                                          ;A READ OF THE TRACE RAM ADDRESS REGISTER.
11215
11216  032024  012737  000040  002376  11$:     MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11217  032032  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11218  032036  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
11219  032040                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11220  032040  104455                          TRAP    C$ERDF
11221  032042  000002                          .WORD   2
11222  032044  000000                          .WORD   0
11223  032046  004704                          .WORD   R2EROR
11224  032050                                  CKLOOP
11225  032050  104406                          TRAP    C$CLP1
11226
11227                                          ;READ TRACE RAM ADDRESS REGISTER TO CHECK THAT IS WAS NOT INCREMENTED
11228                                          ;BY ONE VIA THE SIGNAL ''CTR L'' WHEN THE PREVIOUS STATE OF FUSL0 H FLIP-
11229                                          ;FLOP WAS LOW AND THE SIGNALS TRANST H AND TRST L WERE PULSED.
11230
11231  032052  005037  002414          12$:    CLR     R6LOAD                  ;SETUP TO EXPECT ADDRESS 0
11232  032056  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11233  032064  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
11234  032070  001405                          BEQ     13$                     ;IF ADDRESS EQUALS 0 THEN CONTINUE
11235  032072                                  ERRDF   4,TRADER,R026ER         ;CTR L WAS PROBABLY ISSUED
11236  032072  104455                          TRAP    C$ERDF
11237  032074  000004                          .WORD   4
11238  032076  002462                          .WORD   TRADER
11239  032100  004734                          .WORD   R026ER
11240  032102                                  CKLOOP
11241  032102  104406                          TRAP    C$CLP1
11242
11243                                          ;SET PDAL5 IN CONTROL REGISTER 2 ALONG WITH THE BITS TO ASSERT THE
11244                                          ;SIGNAL PTER15 L IN THE POINTER REGISTER.
11245
11246  032104  012737  000057  002376  13$:     MOV     #PDAL5!PTER15,R2LOAD    ;SETUP BITS TO BE LOADED
11247  032112  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
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11248  032116  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
11249  032120                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11250  032120  104455                          TRAP    C$ERDF
11251  032122  000002                          .WORD   2
11252  032124  000000                          .WORD   0
11253  032126  004704                          .WORD   R2EROR
11254  032130                                  CKLOOP
11255  032130  104406                          TRAP    C$CLP1
11256
11257                                          ;RELOAD ADDRESS ZERO INTO THE OR ADDRESS REGISTER.
11258
11259  032132  005037  002414          14$:    CLR     R6LOAD                  ;SETUP TO LOAD ADDRESS ZERO
11260  032136  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11261  032144  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11262  032150  001405                          BEQ     15$                     ;IF ADDRESS EQUALS 0 THEN CONTINUE
11263  032152                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG ERROR - ORAD 3:0
11264  032152  104455                          TRAP    C$ERDF
11265  032154  000004                          .WORD   4
11266  032156  003161                          .WORD   ORADER
11267  032160  004734                          .WORD   R026ER
11268  032162                                  CKLOOP
11269  032162  104406                          TRAP    C$CLP1
11270
11271                                          ;LOAD DATA PATTERN EQUAL TO ZERO INTO ADDRESS ZERO OF THE OR ARRAY
11272                                          ;RAM.  THIS WILL CAUSE ALL THE OR ARRAY RAM DATA BIT SIGNALS, ORO 7:0
11273                                          ;TO BE ASSERTED HIGH.
11274
11275  032164  005037  002402          15$:    CLR     R4LOAD                  ;SETUP DATA PATTERN EQUAL TO ZERO
11276  032170  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
11277  032176  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
11278  032202  001405                          BEQ     16$                     ;IF DATA EQUALS 0 THEN CONTINUE
11279  032204                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
11280  032204  104455                          TRAP    C$ERDF
11281  032206  000003                          .WORD   3
11282  032210  003512                          .WORD   ORDATA
11283  032212  004720                          .WORD   R4EROR
11284  032214                                  CKLOOP
11285  032214  104406                          TRAP    C$CLP1
11286
11287                                          ;SET AND CLEAR THE SIGNAL CDAL6 IN CONTROL REGISTER 0.  THIS WILL CAUSE
11288                                          ;THE SIGNALS TRANST H AND TRST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL
11289                                          ;ANST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE PULSED.
11290                                          ;WHEN THE SIGNAL ORST L IS PULSED, ALL FUNCTION SELECT FLIP-FLOPS
11291                                          ;SHOULD BE CLOCKED TO THE LOW STATE AS A RESULT OF OR ARRAY RAM DATA
11292                                          ;ORO 7:0 BEING ASSERTED HIGH (0).  A PULSE SHOULD BE ISSUED ON THE
11293                                          ;SIGNAL CTR L AS A RESULT OF THE PREVIOUS STATE OF FUSL0 FLIP-FLOP
11294                                          ;(1) AND THE SIGNALS TRANST H AND TRST L BEING PULSED.  THE TRACING
11295                                          ;FLIP-FLOP WILL ALSO BE SET TO A ONE AS A RESULT OF THE SIGNAL CTR L
11296                                          ;AND THE PREVIOUS STATE OF FUSL0 H FLIP-FLOP (1).
11297
11298  032216  004737  006640          16$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11299
11300                                          ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11301                                          ;SIGNAL PTER0 L IN THE POINTER REGISTER.  THIS IS DONE TO SETUP FOR A
11302                                          ;READ OF THE TRACE RAM ADDRESS REGISTER.
11303
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11304  032222  012737  000040  002376  18$:    MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11305  032230  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11306  032234  001405                          BEQ     19$                     ;IF LOADED OK THEN CONTINUE
11307  032236                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11308  032236  104455                          TRAP    C$ERDF
11309  032240  000002                          .WORD   2
11310  032242  000000                          .WORD   0
11311  032244  004704                          .WORD   R2EROR
11312  032246                                  CKLOOP
11313  032246  104406                          TRAP    C$CLP1
11314
11315                                          ;READ TRACE RAM ADDRESS REGISTER TO CHECK THAT IT WAS INCREMENTED BY
11316                                          ;ONE VIA THE SIGNAL 'CTR L".  THE SIGNAL "CTR L" SHOULD BE GENERATED
11317                                          ;BY THE SIGNALS TRANST H AND TRST L BEING PULSED AND THE PREVIOUS STATE
11318                                          ;OF FUSL0 H FLIP-FLOP (1).
11319
11320  032250  012737  000001  002414  19$:    MOV     #1,R6LOAD               ;SETUP EXPECTED ADDRESS TO EQUAL 1
11321  032256  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11322  032264  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REG
11323  032270  001405                          BEQ     20$                     ;IF ADDRESS EQUALS ONE THEN CONTINUE
11324  032272                                  ERRDF   4,TRADER,R026ER         ;CTR L PROBABLY FAILED TO PULSE
11325  032272  104455                          TRAP    C$ERDF
11326  032274  000004                          .WORD   4
11327  032276  002462                          .WORD   TRADER
11328  032300  004734                          .WORD   R026ER
11329  032302                                  CKLOOP
11330  032302  104406                          TRAP    C$CLP1
11331
11332                                          ;SET PDAL5 IN CONTROL REGISTER 2 ALONG WITH THE BITS TO ASSERT THE
11333                                          ;SIGNAL PTER15 L IN THE POINTER REGISTER
11334
11335  032304  012737  000057  002376  20$.    MOV     #PDAL5!PTER15,R2LOAD    ;SETUP BITS TO BE LAODED
11336  032312  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11337  032316  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
11338  032320                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11339  032320  104455                          TRAP    C$ERDF
11340  032322  000002                          .WORD   2
11341  032324  000000                          .WORD   0
11342  032326  004704                          .WORD   R2EROR
11343  032330                                  CKLOOP
11344  032330  104406                          TRAP    C$CLP1
11345
11346                                          ;RELOAD ADDRESS 0 INTO THE OR ADDRESS REGISTER
11347
11348  032332  005037  002414          21$:    CLR     R6LOAD                  ;SETUP TO LOAD ADDRESS ZERO
11349  032336  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11350  032344  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11351  032350  001405                          BEQ     22$                     ;IF ADDRESS EQUALS 0 THEN CONTINUE
11352  032352                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER NOT EQUAL TO 0
11353  032352  104455                          TRAP    C$ERDF
11354  032354  000004                          .WORD   4
11355  032356  003161                          .WORD   ORADER
11356  032360  004734                          .WORD   R026ER
11357  032362                                  CKLOOP
11358  032362  104406                          TRAP    C$CLP1
11359
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11360                                           ;LOAD DATA PATTERN EQUAL TO TWO INTO ADDRESS ZERO OF THE OR ARRAY RAM.
11361                                           ;THIS WILL CAUSE THE OR ARRAY RAM DATA BIT 'ORO1 L' TO BE ASSERTED LOW
11362                                           ;WITH ALL THE OTHER DATA BITS ASSERTED HIGH.
11363
11364  032364  012737  000002  002402  22$:    MOV     #2,R4LOAD               ;SETUP TO LOAD OR ARRAY RAM WITH 2
11365  032372  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
11366  032400  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
11367  032404  001405                          BEQ     23$                     ;IF DATA EQUALS 2 THEN CONTINUE
11368  032406                                  ERRDF   3,ORDATA R4EROR         ;OR ARRAY RAM DATA ERROR
11369  032406  104455                          TRAP    C$ERDF
11370  032410  000003                          .WORD   3
11371  032412  003512                          .WORD   ORDATA
11372  032414  004720                          .WORD   R4EROR
11373  032416                                  CKLOOP
11374  032416  104406                          TRAP    C$CLP1
11375
11376                                           ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  THIS WILL CAUSE THE SIGNALS
11377                                           ;TRANST H AND TRST L TO BE PULSED WHICH WILL CAUSE THE SIGNAL ANST L
11378                                           ;TO BE PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE PULSED.  A
11379                                           ;PULSE WILL BE ISSUED ON THE SIGNAL CTR L AS A RESULT OF THE TRACING
11380                                           ;FLIP-FLOP BEING SET FROM THE PREVIOUS CTR L PULSE.  WHEN THE SIGNAL
11381                                           ;ORST L IS PULSED, THE OR ARRAY RAM DATA WILL BE LOADED INTO FUNCTION
11382                                           ;SELECT FLIP-FLOPS, THUS SETTING FUSL1 H FLIP-FLOP TO THE HIGH STATE
11383                                           ;AND THE OTHER FUNCTION SELECT FLIP-FLOPS TO THE LOW STATE.  FUNCTION
11384                                           ;SELECT FLIP-FLOP, FUSL1 H, BEING SET HIGH WILL CLEAR THE TRACING
11385                                           ;FLIP-FLOP, THUS INHIBITING ANY FURTHER PULSES ON THE SIGNAL CTR L
11386                                           ;WHEN THE SIGNALS TRANST H AND TRST L ARE PULSED.
11387
11388  032420  004737  006640          23$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11389
11390                                           ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11391                                           ;SIGNAL PTER0 L IN THE POINTER REGISTER.  THIS IS DONE TO SETUP FOR
11392                                           ;A READ OF THE TRACE RAM ADDRESS REGISTER.
11393
11394  032424  012737  000040  002376  25$:    MOV     #PDAL5!PTER0,R2LOAD     ;SETUP BITS TO BE LOADED
11395  032432  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11396  032436  001405                          BEQ     26$                     ;IF LOADED OK THEN CONTINUE
11397  032440                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11398  032440  104455                          TRAP    C$ERDF
11399  032442  000002                          .WORD   2
11400  032444  000000                          .WORD   0
11401  032446  004704                          .WORD   R2EROR
11402  032450                                  CKLOOP
11403  032450  104406                          TRAP    C$CLP1
11404
11405                                           ;READ TRACE RAM ADDRESS REGISTER TO CHECK THAT IT WAS INCREMENTED BY
11406                                           ;ONE VIA THE SIGNAL 'CTR L'.  THE SIGNAL 'CTR L' SHOULD BE GENERATED
11407                                           ;BY THE SIGNALS TRANST H AND TRST L BEING PULSED AND THE OUTPUT OF THE
11408                                           ;TRACING FLIP-FLOP BEING SET HIGH AT THE TIME THE SIGNALS TRANST H AND
11409                                           ;TRST L WERE PULSED.
11410
11411  032452  012737  000002  002414  26$:    MOV     #2,R6LOAD               ;SETUP EXPECTED ADDRESS TO BE 2
11412  032460  012737  174000  002416          MOV     #174000,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11413  032466  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK TRAM ADDRESS REGISTER
11414  032472  001405                          BEQ     27$                     ;IF ADDRESS EQUALS 2 THEN CONTINUE
11415  032474                                  ERRDF   4,TRADER,RO26ER         ;TRACING F/F PROBABLY FAILED TO SET
```

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11416  032474  104455                          TRAP    C$ERDF
11417  032476  000004                          .WORD   4
11418  032500  002462                          .WORD   TRADER
11419  032502  004734                          .WORD   R026ER
11420  032504                                  CKLOOP
11421  032504  104406                          TRAP    C$CLP1
11422
11423                                          ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11424                                          ;SIGNAL PTER15 L IN THE POINTER REGISTER.
11425
11426  032506  012737  000057  002376  27$:    MOV     #PDAL5!PTER15,R2LOAD    ;SETUP BITS TO BE LOADED
11427  032514  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
11428  032520  001405                          BEQ     28$                     ;IF LOADED OK THEN CONTINUE
11429  032522                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11430  032522  104455                          TRAP    C$ERDF
11431  032524  000002                          .WORD   2
11432  032526  000000                          .WORD   0
11433  032530  004704                          .WORD   R2EROR
11434  032532                                  CKLOOP
11435  032532  104406                          TRAP    C$CLP1
11436
11437                                          ;RELOAD ADDRESS 0 INTO THE OR ADDRESS REGISTER
11438
11439  032534  005037  002414          28$:    CLR     R6LOAD                  ;SETUP TO LOAD ADDRESS 0
11440  032540  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11441  032546  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11442  032552  001405                          BEQ     29$                     ;IF LOADED OK THEN CONTINUE
11443  032554                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REG NOT EQUAL TO 0
11444  032554  104455                          TRAP    C$ERDF
11445  032556  000004                          .WORD   4
11446  032560  003161                          .WORD   ORADER
11447  032562  004734                          .WORD   R026ER
11448  032564                                  CKLOOP
11449  032564  104406                          TRAP    C$CLP1
11450
11451                                          ;LOAD DATA PATTERN EQUAL TO ZERO INTO ADDRESS ZERO OF THE OR ARRAY RAM.
11452                                          ;THIS WILL CAUSE THE OR ARRAY RAM DATA BITS "ORO 7:0" TO BE ASSERTED
11453                                          ;HIGH
11454
11455  032566  005037  002402          29$:    CLR     R4LOAD                  ;SETUP DATA PATTERN OF 0
11456  032572  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP MASK WORD
11457  032600  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRY RAM
11458  032604  001405                          BEQ     30$                     ;IF LOADED OK THEN CONTINUE
11459  032606                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY RAM DATA ERROR - ORO 7:0
11460  032606  104455                          TRAP    C$ERDF
11461  032610  000003                          .WORD   3
11462  032612  003512                          .WORD   ORDATA
11463  032614  004720                          .WORD   R4EROR
11464  032616                                  CKLOOP
11465  0326 6  104406                          TRAP    C$CLP1
11466
11467                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  THIS WILL CAUSE THE SIGNALS
11468                                          ;TRANST H AND TRST L TO PULSED WHICH WILL CAUSE THE SIGNAL ANST L TO BE
11469                                          ;PULSED WHICH WILL CAUSE THE SIGNAL ORST L TO BE PULSED.  WHEN THE
11470                                          ;SIGNAL ORST L IS PULSED, THE OR ARRAY RAM DATA WILL BE LOADED INTO
11471                                          ;THE FUNCTION SELECT FLIP-FLOPS, THUS SETTING ALL THE OUTPUTS OF THE
```

```
11472                                          ;FLIP-FLOPS TO THE LOW STATE.  THE PREVIOUS CLOCKING OF CDAL6 HAD SET
11473                                          ;FUNCTION SELECT FLIP-FLOP, FUSL1 H, TO THE HIGH STATE, THUS CLEARING
11474                                          ;THE TRACING FLIP-FLOP.  THEREFORE, WHEN CDAL6 IS PULSED THIS TIME TO
11475                                          ;PULSE THE SIGNALS TRANST H AND TRST L, NO PULSE SHOULD BE ISSUED ON THE
11476                                          ;CTR L SIGNAL.  THE TRACE RAM ADDRESS REGISTER WILL NOT BE INCREMENTED.
11477
11478  032620  004737  006640          30$:   JSR     PC,TRANST                ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11479
11480                                          ;SET PDAL5 IN CONTROL REGISTER 0 ALONG WITH THE BITS TO ASSERT THE
11481                                          ;SIGNAL PTER0 L IN THE POINTER REGISTER.  THIS IS DONE TO SETUP FOR
11482                                          ;A READ OF THE TRACE RAM ADDRESS REGISTER.
11483
11484  032624  012737  000040  002376          MOV     #PDAL5!PTER0,R2LOAD      ;SETUP BITS TO BE LOADED
11485  032632  004737  006134                  JSR     PC,LDRDR2                ;GO LOAD, READ AND CHECK REG 2
11486  032636  001405                          BEQ     31$                      ;IF LOADED OK THEN CONTINUE
11487  032640                                  ERRDF   2,,R2EROR                ;REGISTER 2 NOT EQUAL EXPECTED
11488  032640  104455                          TRAP    C$ERDF
11489  032642  000002                          .WORD   2
11490  032644  000000                          .WORD   0
11491  032646  004704                          .WORD   R2EROR
11492  032650                                  CKLOOP
11493  032650  104406                          TRAP    C$CLP1
11494
11495                                          ;READ TRACE RAM ADDRESS REGISTER AGAIN TO CHECK THAT THE ''TRACING'' FLIP-
11496                                          ;FLOP WAS CLEARED WHEN FUNCTION SELECT FLIP-FLOP, FUSL1 H, WAS SET
11497                                          ;HIGH IN THE PREVIOUS SECTION.  WHEN THE TRACING FLIP-FLOP IS CLEARED,
11498                                          ;NO PULSE SHOULD BE ISSUED ON THE SIGNAL CTR L WHEN THE SIGNALS TRANST H
11499                                          ;AND TRST L ARE PULSED.
11500
11501  032652  012737  000002  002414  31$:    MOV     #2,R6LOAD                ;SETUP EXPECTED ADDRESS TO EQUAL 2
11502  032660  012737  174000  002416          MOV     #174000,R6MASK           ;SETUP TO IGNORE UNWANTED BITS
11503  032666  004737  006256                  JSR     PC,READR6                ;GO READ AND CHECK TRAM ADDRESS REG
11504  032672  001404                          BEQ     32$                      ;IF ADDRESS = 2 THEN CONTINUE
11505  032674                                  ERRDF   4,TRADER,R026ER          ;TRACING F/F FAILED TO CLEAR VIA FUSL1
11506  032674  104455                          TRAP    C$ERDF
11507  032676  000004                          .WORD   4
11508  032700  002462                          .WORD   TRADER
11509  032702  004734                          .WORD   R026ER
11510  032704                          32$:    ENDSEG
11511  032704                          10000$:
11512  032704  104405                          TRAP    C$ESEG
11513  032706                                  ENDTST
11514  032706                          L10166:
11515  032706  104401                          TRAP    C$ETST
11516
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                                       .SBTTL  TEST 61: SBL58 AND SBL56 FLIP-FLOP TEST
                                       ;++
                                       ; THIS TEST WILL CHECK THAT SBL56 AND SBL58 FLIP-FLOPS CAN BE SET AND CLEARED.
                                       ; SBL57 AND SBL59 ARE CHECKED TO REMAIN CLEARED DURING THIS TEST.  SBL 59:56
                                       ; FLIP-FLOPS ARE CHECKED BY THE PROGRAM ON THE TRACE RAM DATA IN BUS WHEN THE
                                       ; SIGNAL "TRSL2 L" IS ASSERTED LOW. SBL 59:56 FLIP-FLOPS WILL BE READBACK ON
                                       ; TRDI 59:56 SIGNAL LINES.  SBL56 FLIP-FLOP IS SET VIA A BORROW FROM EVENT
                                       ; COUNTER 0 AND EVENT COUNTER 0 COUNT DOWN PULSE.  SBL56 FLIP-FLOP IS CLEARED
                                       ; BY RELOADING EVENT COUNTER 0.  SBL58 FLIP-FLOP IS SET BY "OR ARRAY RAM" DATA
                                       ; BIT OR04 L BEING SET LOW AND THE SIGNAL ORST L BEING PULSED.  SBL58
                                       ; FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 2.
                                       ;--

032710                                         BGNTST
032710                                 T61::
032710  004737  005474                         JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
032714                                         BGNSEG
032714  104404                                 TRAP    C$BSEG

                                       ;CLEAR CDAL4 IN CONTROL REGISTER 0. CDAL4 ON A 0 WILL ALLOW ONLY ONE
                                       ;AND/OR ARRAY RAM TO BE SELECTED AT A TIME.

032716  105037  002370                         CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
032722  004737  006102                         JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
032726  001405                                 BEQ     1$                      ;IF LOADED OK THEN CONTINUE
032730                                         ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
032730  104455                                 TRAP    C$ERDF
032732  000001                                 .WORD   1
032734  000000                                 .WORD   0
032736  004604                                 .WORD   ROEROR
032740                                         CKLOOP
032740  104406                                 TRAP    C$CLP1

                                       ;THE FOLLOWING LOOP WILL LOAD ZEROES INTO EACH OF THE EVENT COUNTER
                                       ;REGISTERS AND EVENT COUNTERS.  BY LOADING EACH EVENT COUNTER, THE
                                       ;SBL FLIP-FLOPS 59:56 WILL BE CLEARED BY SIGNALS W9 L, W10 L, W11 L,AND W12 L.

032742  012737  000011  002376   1$:         MOV     #PTER9,R2LOAD           ;SETUP TO START LOADING AT COUNTER 0
032750  004737  006134            2$:         JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
032754  001405                               BEQ     3$                      ;IF LOADED OK THEN CONTINUE
032756                                       ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
032756  104455                               TRAP    C$ERDF
032760  000002                               .WORD   2
032762  000000                               .WORD   0
032764  004704                               .WORD   R2EROR
032766                                       CKLOOP
032766  104406                               TRAP    C$CLP1
032770  012777  000000  147360   3$:         MOV     #0,@REG6                ;LOAD ALL ZEROES INTO EVENT COUNTERS
032776  005237  002376                       INC     R2LOAD                  ;UPDATE THE POINTER TO NEXT COUNTER
033002  022737  000015  002376               CMP     #PTER13,R2LOAD          ;CHECK IF ALL EVENT COUNTERS LOADED
033010  001357                               BNE     2$                      ;IF NOT THEN LOAD THE NEXT EVENT COUNTER

                                       ;SET CDAL3 TO A ONE AND CDAL2 TO A 0 IN CONTROL REGISTER 0 TO SET THE
                                       ;SIGNAL TRSL2 L. THE SIGNAL TRSL2 L WILL ALLOW SBL BITS 59:56 TO BE
                                       ;READBACK ON TRDI BITS 59:56.
```

```
11573
11574  033012  052737  000010  002370          BIS     #CDAL3,R0LOAD           ;SETUP BITS TO BE LOADED
11575  033020  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11576  033024  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
11577  033026                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED.
11578  033026  104455                          TRAP    C$ERDF
11579  033030  000001                          .WORD   1
11580  033032  000000                          .WORD   0
11581  033034  004604                          .WORD   R0EROR
11582  033036                                  CKLOOP
11583  033036  104406                          TRAP    C$CLP1
11584
11585                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
11586                                          ;2.  THIS IS DONE TO SETUP FOR A READBACK OF TRDI BITS 59:48.
11587
11588  033040  012737  000004  002376  4$:     MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
11589  033046  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11590  033052  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
11591  033054                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11592  033054  104455                          TRAP    C$ERDF
11593  033056  000002                          .WORD   2
11594  033060  000000                          .WORD   0
11595  033062  004704                          .WORD   R2EROR
11596  033064                                  CKLOOP
11597  033064  104406                          TRAP    C$CLP1
11598
11599                                          ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59:56 ARE CLEARED.
11600                                          ;SBL BITS 59:56 ARE READBACK ON TRDI BITS 59:56 WHEN THE SIGNAL TRSI2 L
11601                                          ;IS ASSERTED.  THE SBL FLIP-FLOPS SHOULD HAVE BEEN CLEARED WHEN THE
11602                                          ;EVENT COUNTERS WERE LOADED.
11603
11604  033066  005037  002414          5$:     CLR     R6LOAD                  ;SETUP EXPECTED DATA
11605  033072  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY TRDI 59:56 BITS
11606  033100  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL 59:56 BITS
11607  033104  001405                          BEQ     6$                      ;IF ALL FLIP-FLOPS CLEARED THEN CONT
11608  033106                                  ERRDF   4,SBLERR,R026ER         ;WRITING EVNT CNTR'S FAILED TO 0 SBL F/F'S 59:56
11609  033106  104455                          TRAP    C$ERDF
11610  033110  000004                          .WORD   4
11611  033112  003416                          .WORD   SBLERR
11612  033114  004734                          .WORD   R026ER
11613  033116                                  CKLOOP
11614  033116  104406                          TRAP    C$CLP1
11615
11616                                          ;CLEAR CDAL3 IN CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSLO L. THE
11617                                          ;SIGNAL TRSLO L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
11618
11619  033120  042737  000010  002370  6$:     BIC     #CDAL3,R0LOAD           ;SETUP BIT TO BE CLEARED
11620  033126  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11621  033132  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
11622  033134                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
11623  033134  104455                          TRAP    C$ERDF
11624  033136  000001                          .WORD   1
11625  033140  000000                          .WORD   0
11626  033142  004604                          .WORD   R0EROR
11627  033144                                  CKLOOP
11628  033144  104406                          TRAP    C$CLP1
```

```
11629
11630                                   ;THE FOLLOWING SECTION OF CODE WILL LOAD ALL ZEROES INTO ALL THE TRACE
11631                                   ;RAM DATA IN BUFFERS. THIS WILL SELECT ADDRESS ZERO OF ALL THE AND ARRAYS.
11632
11633  033146  005037  002414    7$:   CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
11634  033152  005037  002416          CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
11635
11636                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 15:0
11637
11638  033156  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
11639  033162  000000                  .WORD   PTER5                   ;SELECT TRDI BITS 15:0
11640
11641                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 31:16
11642
11643  033164  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
11644  033170  000006                  .WORD   PTER6                   ;SELECT TRDI BITS 31:16
11645
11646                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 47:32
11647
11648  033172  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
11649  033176  000007                  .WORD   PTER7                   ;SELECT TRDI BITS 47:32
11650
11651                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 59:48
11652
11653  033200  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
11654  033204  000010                  .WORD   PTER8                   ;SELECT TRDI BITS 59:48
11655
11656                                   ;THE FOLLOWING SECTION OF CODE WILL WRITE DATA EQUAL TO 16 INTO ADDRESS
11657                                   ;ZERO OF THE AND ARRAY SELECTED BY PTERO L. THE REMAINING AND ARRAYS
11658                                   ;WILL BE WRITTEN WITH DATA EQUAL TO ZERO.
11659
11660  033206  012737  000000  002376        MOV     #PTER0,R2LOAD           ;SETUP TO SELECT AND ARRAY ZERO
11661  033214  012737  000016  002402        MOV     #16,R4LOAD              ;SETUP DATA FOR THE FIRST AND ARRAY
11662  033222  012737  170377  002406        MOV     #170377,R4MASK          ;SETUP TO CHECK ONLY AND ARRAY DATA BITS
11663  033230  004737  006134        8$:     JSR     PC,LDRDR2               ;LOAD, READ AND CHECK CONTROL REG 2
11664  033234  001405                        BEQ     9$                      ;IF LOADED OK THEN GO WRITE DATA
11665  033236                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11666  033236  104455                        TRAP    C$ERDF
11667  033240  000002                        .WORD   2
11668  033242  000000                        .WORD   0
11669  033244  004704                        .WORD   R2EROR
11670  033246                                CKLOOP
11671  033246  104406                        TRAP    C$CLP1
11672  033250  004737  006166        9$:     JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
11673  033254  001405                        BEQ     10$                     ;IF LOADED OK THEN CONTINUE
11674  033256                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
11675  033256  104455                        TRAP    C$ERDF
11676  033260  000003                        .WORD   3
11677  033262  003550                        .WORD   ANDERR
11678  033264  004720                        .WORD   R4EROR
11679  033266                                CKLOOP
11680  033266  104406                        TRAP    C$CLP1
11681  033270  005037  002402        10$:    CLR     R4LOAD                  ;NOT LOAD REMAINING AND ARRAYS TO 0
11682  033274  005237  002376                INC     R2LOAD                  ;UPDATE POINTER TO NEXT AND ARRAY
11683  033300  022737  000017  002376        CMP     #PTER15,R2LOAD          ;CHECK IF ALL AND ARRAYS WRITTEN
11684  033306  001350                        BNE     8$                      ;IF NOT THEN LOAD 0 INTO NEXT ARRAY
```

```
11685
11686                                   ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTRROL REG 2
11687
11688  033310  004737  006134           JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11689  033314  001405                   BEQ     11$                     ;IF LOADED OK THEN CONTINUE
11690  033316                           ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11691  033316  104455                   TRAP    C$ERDF
11692  033320  000002                   .WORD   2
11693  033322  000000                   .WORD   0
11694  033324  004704                   .WORD   R2EROR
11695  033326                           CKLOOP
11696  033326  104406                   TRAP    C$CLP1
11697
11698                                   ;SELECT ADDRESS ONE IN THE OR ADDRESS REGISTER. LOCATION 1 WILL BE
11699                                   ;WRITTEN WITH DATA TO SET SBL58 FLIP-FLOP LATER ON IN TEST.
11700
11701  033330  012737  000001  002414  11$:    MOV     #1,R6LOAD               ;SETUP ADDRESS TO BE LOADED
11702  033336  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
11703  033344  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
11704  033350  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
11705  033352                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER ERROR - ORAD 3:0
11706  033352  104455                          TRAP    C$ERDF
11707  033354  000004                          .WORD   4
11708  033356  003161                          .WORD   ORADER
11709  033360  004734                          .WORD   R026ER
11710  033362                                  CKLOOP
11711  033362  104406                          TRAP    C$CLP1
11712
11713                                   ;LOAD LOCATION ONE OF THE OR ARRAY RAMS WITH DATA EQUAL TO 20.  THIS
11714                                   ;DATA PATTERN WILL SET THE SIGNLA OR04 L TO THE LOW STATE AND ALL OTHER
11715                                   ;OR ARRAY DATA BITS TO THE HIGH STATE.  THIS DATA PATTERN WILL CAUSE
11716                                   ;SBL58 FLIP-FLOP TO BE SET TO THE HIGH STATE LATER ON IN THE TEST.
11717
11718  033364  012737  000020  002402  12$:    MOV     #BIT4,R4LOAD            ;SETUP DATA TO BE LOADED
11719  033372  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
11720  033400  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
11721  033404  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
11722  033406                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA ERROR
11723  033406  104455                          TRAP    C$ERDF
11724  033410  000003                          .WORD   3
11725  033412  003512                          .WORD   ORDATA
11726  033414  004720                          .WORD   R4EROR
11727  033416                                  CKLOOP
11728  033416  104406                          TRAP    C$CLP1
11729
11730                                   ;SET CDAL4 TO A 1 IN CONTROL REGISTER 0. CDAL4 ON A 1 WILL ENABLE THE
11731                                   ;OUTPUTS OF ALL THE AND AND OR ARRAY RAMS AT THE SAME TIME.
11732
11733  033420  052737  000020  002370  13$:    BIS     #CDAL4,R0LOAD           ;SETUP BE TO BE CLEARED
11734  033426  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11735  033432  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
11736  033434                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
11737  033434  104455                          TRAP    C$ERDF
11738  033436  000001                          .WORD   1
11739  033440  000000                          .WORD   0
11740  033442  004604                          .WORD   R0EROR
```

```
11741  033444                                  CKLOOP
11742  033444  104406                          TRAP    C$CLP1
11743
11744                                          ;READ BOTH THE AND ARRAY RAM AND THE OR ARRAY RAMS DATA.  A DATA
11745                                          ;PATTERN OF 16 WAS WRITTEN INTO THE FIRST AND ARRAY AND ALL ZEROES
11746                                          ;WERE WRITTEN INTO THE REMAINING AND ARRAYS.  A DATA PATTERN EQUAL
11747                                          ;TO 16 SHOULD BE READ BACK FROM THE AND ARRAY DO TO THE WIRED OR
11748                                          ;EFFECT OF THE AND ARRAY OUTPUTS.  A DATA PATTERN EQUAL TO 20 SHOULD
11749                                          ;BE READ BACK FROM THE OR ARRAY RAMS.
11750
11751  033446  112737  0000 6  002405  14$:    MOVB    #16,R4GOOD+1            ;ADD AND ARRAY DATA TO OR ARRAY DATA
11752  033454  012737  170000  002406          MOV     #170000,R4MASK          ;SETUP TO CHECK AND/OR ARRAY DATA
11753  033462  004737  006216                  JSR     PC,READR4               ;GO READ AND CHECK AND/OR ARRAY DATA
11754  033466  001405                          BEQ     15$                     ;IF DATA OK THEN CONTINUE
11755  033470                                  ERRDF   3,ANDOR,R4EROR          ;AND/OR ARRAY RAM DATA ERROR
11756  033470  104455                          TRAP    C$ERDF
11757  033472  000003                          .WORD   3
11758  033474  003647                          .WORD   ANDOR
11759  033476  004720                          .WORD   R4EROR
11760  033500                                  CKLOOP
11761  033500  104406                          TRAP    C$CLP1
11762
11763                                          ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0 TO CAUSE THE FOUT FLIP-
11764                                          ;FLOPS TO BE USED TO ADDRESS THE OR ARRAY RAMS.
11765
11766  033502  052737  000200  002370  15$:    BIS     #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
11767  033510  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11768  033514  001405                          BEQ     16$                     ;IF LOADED OK THEN CONTINUE
11769  033516                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
11770  033516  104455                          TRAP    C$ERDF
11771  033520  000001                          .WORD   1
11772  033522  000000                          .WORD   0
11773  033524  004604                          .WORD   ROEROR
11774  033526                                  CKLOOP
11775  033526  104406                          TRAP    C$CLP1
11776
11777                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING CDAL6
11778                                          ;WILL CAUSE THE SIGNALS TRANSI H AND TRST L TO BE PULSED, WHICH WILL
11779                                          ;CAUSE THE SIGNAL ANST L TO BE PULSED, WHICH WILL CAUSE THE SIGNAL
11780                                          ;ORST L TO BE PULSED.  WHEN THE SIGNAL ANST L IS PULSED
11781                                          ;A COUNT DOWN PULSE WILL BE ISSUED TO EVENT COUNTER 0 BECAUSE OF THE
11782                                          ;AND ARRAY DATA PATTERN (16).  A BORROW SHOULD BE GENERATED FOR EVENT
11783                                          ;COUNTER 0 BECAUSE ALL ZEROES WERE LOADED INTO THE EVENT COUNTERS. A
11784                                          ;BORROW BEING GENERATED ALONG WITH THE COUNT DOWN PULSE WILL CAUSE THE
11785                                          ;OUTPUT OF THE FOUT0 FLIP-FLOP TO GO TO THE LOW STATE, THUS SELECTING
11786                                          ;ADDRESS ONE ON THE OR ADDRESS LINES ORAD 3:0.  SBL56 FLIP-FLOP SHOULD
11787                                          ;ALSO GET SET AS A RESULT OF THE BORROW AND THE COUNT DOWN PULSE.  WHEN
11788                                          ;THE SIGNAL ORST L IS PULSED, DATA BITS 4 AND 5 OF ADDRESS ONE OF
11789                                          ;THE OR ARRAY RAM WILL BE LOADED INTO SBLE FLIP-FLOPS 59 AND 58, THUS
11790                                          ;SETTING SBL58 FLIP-FLOP TO THE HIGH STATE.
11791
11792  033530  004737  006640          16$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
11793
11794                                          ;WITH CDAL7 SET TO A ONE, READ CONTROL REGISTER 0 TO CHECK THAT ONLY
11795                                          ;FOUT0 FLIP-FLOP IS SET TO A ONE.  THE FOUT FLIP-FLOPS ARE USED TO
11796                                          ;ADDRESS THE OR ADDRESS REGISTER VIA SIGNAL LINES ORAD 3:0.
```

```
 1797
 11798  033534  012737  000001  002414  18$:    MOV     #1,R6LOAD               ;SETUP EXPECTED ADDRESS TO BE ONE
 11799  033542  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
 11800  033550  004737  006256                  JSR     PC,READR6               ;GO READ FOUT FLIP-FLOPS 3:0
 11801  033554  001405                          BEQ     19$                     ;IF EQUAL TO A ONE THEN CONTINUE
 11802  033556                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
 11803  033556  104455                          TRAP    C$ERDF
 11804  033560  000004                          .WORD   4
 11805  033562  003213                          .WORD   EVNTCT
 11806  033564  005024                          .WORD   EVNTER
 11807  033566                                  CKLOOP
 11808  033566  104406                          TRAP    C$CLP1
 11809
 11810                                          ;SET CDAL3 TO A ONE AND CDAL2 TO A ZERO IN CONTROL REGISTER 0 TO
 11811                                          ;ASSERT THE SIGNAL TRSL2 L. THIS SIGNAL WILL ALLOW THE SBL FLIP-FLOPS
 11812                                          ;TO BE READBACK ON THE TRDI 59:56 SIGNAL LINES.
 11813
 11814  033570  052737  000010  002370  19$:    BIS     #CDAL3,R0LOAD           ;SETUP BITS TO BE LOADED
 11815  033576  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
 11816  033602  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
 11817  033604                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
 11818  033604  104455                          TRAP    C$ERDF
 11819  033606  000001                          .WORD   1
 11820  033610  000000                          .WORD   0
 11821  033612  004604                          .WORD   R0EROR
 11822  033614                                  CKLOOP
 11823  033614  104406                          TRAP    C$CLP1
 11824
 11825                                          ;ASSERT THE SIGNAL PTER4 L IN POINTER REG VIA CONTROL REG 2.  THIS IS
 11826                                          ;TO SETUP FOR A READBACK OF THE SBL F/F'S ON TRDI 59:56 SIGNAL LINES.
 11827
 11828  033616  012737  000004  002376  20$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
 11829  033624  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
 11830  033630  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
 11831  033632                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
 11832  033632  104455                          TRAP    C$ERDF
 11833  033634  000002                          .WORD   2
 11834  033636  000000                          .WORD   0
 11835  033640  004704                          .WORD   R2EROR
 11836  033642                                  CKLOOP
 11837  033642  104406                          TRAP    C$CLP1
 11838
 11839                                          ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 58 AND 56 ARE
 11840                                          ;SET AND THAT SBL FLIP-FLOPS 59 AND 57 ARE CLEARED.  SBL BITS 59:56
 11841                                          ;ARE READBACK ON TRDI 59:56 SIGNAL LINES WHEN TRSL2 L IS ASSERTED.
 11842
 11843  033644  012737  002400  002414  21$:    MOV     #BIT10!BIT8,R6LOAD      ;SETUP TO EXPECT SBL 58 AND 56 SET
 11844  033652  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY SBL BITS
 11845  033660  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL BITS
 11846  033664  001405                          BEQ     22$                     ;IF SBL 58 AND 56 SET THEN CONT
 11847  033666                                  ERRDF   4,SBLERR,R026ER         ;SBL 59:56 FLIP-FLOP ERROR
 11848  033666  104455                          TRAP    C$ERDF
 11849  033670  000004                          .WORD   4
 11850  033672  003416                          .WORD   SBLERR
 11851  033674  004734                          .WORD   R026ER
 11852  033676                                  CKLOOP
```

```
11853  033676  104406                          TRAP    C$CLP1
11854
11855                                          ;LOAD EVENT COUNTERS 0 AND 2 AGAIN WITH 0 TO CHECK THAT THE SBL
11856                                          ;FLIP-FLOPS ARE CLEARED WHEN THE SIGNALS W9 L AND W11 L ARE ISSUED
11857                                          ;FROM LOADING THE EVENT COUNTERS.
11858
11859  033700  012737  000011  002376  22$:    MOV     #PTER9,R2LOAD           ;SETUP BITS TO BE LOADED
11860  033706  004737  006134          23$:    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11861  033712  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
11862  033714                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11863  033714  104455                          TRAP    C$ERDF
11864  033716  000002                          .WORD   2
11865  033720  000000                          .WORD   0
11866  033722  004704                          .WORD   R2EROR
11867  033724                                  CKLOOP
11868  033724  104406                          TRAP    C$CLP1
11869  033726  012777  000000  146422  24$:    MOV     #0,@REG6                ;CLEAR EVENT COUNTERS 0 AND 2
11870  033734  022737  000013  002376          CMP     #PTER11,R2LOAD          ;CHECK TO EVENT COUNTER 2 LOADED YET
11871  033742  001404                          BEQ     25$                     ;IF YES THEN CONTINUE
11872  033744  062737  000002  002376          ADD     #2,R2LOAD               ;UPDATE POINTER REGISTER TO COUNTER 2
11873  033752  000755                          BR      23$                     ;GO LOAD EVENT COUNTER 2
11874
11875                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
11876                                          ;READBACK OF THE SBL BITS ON THE TRDI SIGNAL LINES 59:56.  WITH THE
11877                                          ;SIGNAL TRSL2 L ASSERTED, THE SBL FLIP-FLOPS WILL BE READBACK ON
11878                                          ;TRDI BITS 59:56 WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
11879
11880  033754  012737  000004  002376  25$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
11881  033762  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11882  033766  001405                          BEQ     26$                     ;IF LOADED OK THEN CONTINUE
11883  033770                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11884  033770  104455                          TRAP    C$ERDF
11885  033772  000002                          .WORD   2
11886  033774  000000                          .WORD   0
11887  033776  004704                          .WORD   R2EROR
11888  034000                                  CKLOOP
11889  034000  104406                          TRAP    C$CLP1
11890
11891                                          ;READ CONTROL REGISTER 6 AGAIN TO CHECK THAT LOADING EVENT COUNTERS
11892                                          ;0 AND 2 CLEARED SBL FLIP-FLOPS 58 AND 56.
11893
11894  034002  005037  002414          26$:    CLR     R6LOAD                  ;SETUP TO EXPECT SBL FLIP-FLOPS AS 0
11895  034006  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL FLIP-FLOPS
11896  034012  001404                          BEQ     27$                     ;IF SBL F/F'S = 0 THEN CONTINUE
11897  034014                                  ERRDF   4,SBLERR,R026ER         ;WRITING EVNT CNTR'S FAILED TO 0 THE SBL F/F'S
11898  034014  104455                          TRAP    C$ERDF
11899  034016  000004                          .WORD   4
11900  034020  003416                          .WORD   SBLERR
11901  034022  004734                          .WORD   R026ER
11902  034024                          27$:    ENDSEG
11903  034024                          10000$:
11904  034024  104405                          TRAP    C$ESEG
11905  034026                                  ENDTST
11906  034026                          L10167:
11907  034026  104401                          TRAP    C$ETST
```

```
                                .SBTTL  TEST 62: SBL59 AND SBL57 FLIP-FLOP TEST

                                ;++
                                ; THIS TEST WILL CHECK THAT SBL57 AND SBL59 FLIP-FLOPS CAN BE SET AND CLEARED.
                                ; SBL56 AND SBL58 ARE CHECKED TO REMAIN CLEARED DURING THIS TEST.  SBL 59:56
                                ; FLIP-FLOPS ARE CHECKED BY THE PROGRAM ON THE TRACE RAM DATA IN BUS WHEN THE
                                ; SIGNAL "TRSL2 L" IS ASSERTED LOW. SBL 59:56 FLIP-FLOPS WILL BE READBACK ON
                                ; TRDI 59:57 SIGNAL LINES.  SBL56 FLIP-FLOP IS SET VIA A BORROW FROM EVENT
                                ; COUNTER 1 AND EVENT COUNTER 1 COUNT DOWN PULSE.  SBL57 FLIP-FLOP IS CLEARED
                                ; BY RELOADING EVENT COUNTER 1.  SBL5 FLIP-FLOP IS SET BY "OR ARRAY RAM" DATA
                                ; BIT OR05 L BEING SET LOW AND THE SIGNAL ORST L BEING PULSED.  SBL59
                                ; FLIP-FLOP IS CLEARED BY RELOADING EVENT COUNTER 3.
                                ;--

                                        BGNTST
                                T62::
034030  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
034034                                  BGNSEG
034034  104404                          TRAP    C$BSEG

                                        ;CLEAR CDAL4 IN CONTROL REGISTER 0. CDAL4 ON A ZERO WILL ALLOW ONLY ONE
                                        ;AND/OR ARRAY RAM TO BE SELECTED AT A TIME.

034036  105037  002370                  CLRB    ROLOAD                  ;SETUP BITS TO BE LOADED
034042  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
034046  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
034050                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
034050  104455                          TRAP    C$ERDF
034052  000001                          .WORD   1
034054  000000                          .WORD   0
034056  004604                          .WORD   ROEROR
034060                                  CKLOOP
034060  104406                          TRAP    C$CLP1

                                        ;THE FOLLOWING LOOP WILL LOAD ZEROES INTO EACH OF THE EVENT COUNTER
                                        ;REGISTERS AND EVENT COUNTERS.  BY LOADING EACH EVENT COUNTER, THE
                                        ;SBL FLIP-FLOPS 59:56 WILL BE CLEARED BY SIGNALS W9 L, W10 L, W11 L,AND W12 L.

034062  012737  000011  002376  1$:     MOV     #PTER9,R2LOAD           ;SETUP TO START LOADING AT COUNTER 0
034070  004737  006134          2$:     JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
034074  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
034076                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
034076  104455                          TRAP    C$ERDF
034100  000002                          .WORD   2
034102  000000                          .WORD   0
034104  004704                          .WORD   R2EROR
034106                                  CKLOOP
034106  104406                          TRAP    C$CLP1
034110  012777  000000  146240  3$:     MOV     #0,@REG6                ;LOAD ALL ZEROES INTO EVENT COUNTERS
034116  005237  002376                  INC     R2LOAD                  ;UPDATE THE POINTER TO NEXT COUNTER
034122  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL EVENT COUNTERS LOADED
034130  001357                          BNE     2$                      ;IF NOT THEN LOAD THE NEXT EVENT COUNTER

                                        ;SET CDAL3 TO A ONE AND CDAL2 TO A 0 IN CONTROL REGISTER 0 TO SET THE
                                        ;SIGNAL TRSL2 L. THE SIGNAL TRSL2 L WILL ALLOW SBL BITS 59:56 TO BE
                                        ;READBACK ON TRDI BITS 59:56.
```

```
11964
11965  034132  052737  000010  002370          BIS     #CDAL3,R0LOAD           ;SETUP BITS TO BE LOADED
11966  034140  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
11967  034144  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
11968  034146                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED.
11969  034146  104455                          TRAP    C$ERDF
11970  034150  000001                          .WORD   1
11971  034152  000000                          .WORD   0
11972  034154  004604                          .WORD   R0EROR
11973  034156                                  CKLOOP
11974  034156  104406                          TRAP    C$CLP1
11975
11976                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
11977                                          ;2.  THIS IS DONE TO SETUP FOR A READBACK OF TRDI BITS 59:48.
11978
11979  034160  012737  000004  002376  4$:     MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
11980  034166  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
11981  034172  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
11982  034174                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
11983  034174  104455                          TRAP    C$ERDF
11984  034176  000002                          .WORD   2
11985  034200  000000                          .WORD   0
11986  034202  004704                          .WORD   R2EROR
11987  034204                                  CKLOOP
11988  034204  104406                          TRAP    C$CLP1
11989
11990                                          ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59:56 ARE CLEARED.
11991                                          ;SBL BITS 59:56 ARE READBACK ON TRDI BITS 59:56 WHEN THE SIGNAL TRSL2 L
11992                                          ;IS ASSERTED.  THE SBL FLIP-FLOPS SHOULD HAVE BEEN CLEARED WHEN THE
11993                                          ;EVENT COUNTERS WERE LOADED.
11994
11995  034206  005037  002414          5$:     CLR     R6LOAD                  ;SETUP EXPECTED DATA
11996  034212  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY TRDI 59:56 BITS
11997  034220  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL 59:56 BITS
11998  034224  001405                          BEQ     6$                      ;IF ALL FLIP-FLOPS CLEARED THEN CONT
11999  034226                                  ERRDF   4,SBLERR,R026ER         ;WRITING EVNT CNTR'S FAILED TO 0 SBL F/F'S 59:56
12000  034226  104455                          TRAP    C$ERDF
12001  034230  000004                          .WORD   4
12002  034232  003416                          .WORD   SBLERR
12003  034234  004734                          .WORD   R026ER
12004  034236                                  CKLOOP
12005  034236  104406                          TRAP    C$CLP1
12006
12007                                          ;CLEAR CDAL3 IN CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSL0 L. THE
12008                                          ;SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
12009
12010  034240  042737  000010  002370  6$:     BIC     #CDAL3,R0LOAD           ;SETUP BIT TO BE CLEARED
12011  034246  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12012  034252  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
12013  034254                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12014  034254  104455                          TRAP    C$ERDF
12015  034256  000001                          .WORD   1
12016  034260  000000                          .WORD   0
12017  034262  004604                          .WORD   R0EROR
12018  034264                                  CKLOOP
12019  034264  104406                          TRAP    C$CLP1
```

```
12020
12021                                   ;THE FOLLOWING SECTION OF CODE WILL LOAD ALL ZEROES INTO ALL THE TRACE
12022                                   ;RAM DATA IN BUFFERS. THIS WILL SELECT ADDRESS ZERO OF ALL THE AND ARRAYS.
12023
12024  034266  005037  002414    7$:   CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
12025  034272  005037  002416          CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
12026
12027                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 15:0
12028
12029  034276  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12030  034302  000005                  .WORD   PTER5                   ;SELECT TRDI BITS 15:0
12031
12032                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 31:16
12033
12034  034304  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12035  034310  000006                  .WORD   PTER6                   ;SELECT TRDI BITS 31:16
12036
12037                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 47:32
12038
12039  034312  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12040  034316  000007                  .WORD   PTER7                   ;SELECT TRDI BITS 47:32
12041
12042                                   ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 59:48
12043
12044  034320  004537  006426          JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12045  034324  000010                  .WORD   PTER8                   ;SELECT TRDI BITS 59:48
12046
12047                                   ;THE FOLLOWING SECTION OF CODE WILL WRITE DATA EQUAL TO 15 INTO ADDRESS
12048                                   ;ZERO OF THE AND ARRAY SELECTED BY PTERO L. THE REMAINING AND ARRAYS
12049                                   ;WILL BE WRITTEN WITH DATA EQUAL TO ZERO.
12050
12051  034326  012737  000000  002376        MOV     #PTER0,R2LOAD           ;SETUP TO SELECT AND ARRAY ZERO
12052  034334  012737  000015  002402        MOV     #15,R4LOAD              ;SETUP DATA FOR THE FIRST AND ARRAY
12053  034342  012737  170377  002406        MOV     #170377,R4MASK          ;SETUP TO CHECK ONLY AND ARRAY DATA BITS
12054  034350  004737  006134        8$:     JSR     PC,LDRDR2               ;LOAD, READ AND CHECK CONTROL REG 2
12055  034354  001405                        BEQ     9$                      ;IF LOADED OK THEN GO WRITE DATA
12056  034356                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12057  034356  104455                        TRAP    C$ERDF
12058  034360  000002                        .WORD   2
12059  034362  000000                        .WORD   0
12060  034364  004704                        .WORD   R2EROR
12061  034366                                CKLOOP
12062  034366  104406                        TRAP    C$CLP1
12063  034370  004737  006166        9$:     JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
12064  034374  001405                        BEQ     10$                     ;IF LOADED OK THEN CONTINUE
12065  034376                                ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
12066  034376  104455                        TRAP    C$ERDF
12067  034400  000003                        .WORD   3
12068  034402  003550                        .WORD   ANDERR
12069  034404  004720                        .WORD   R4EROR
12070  034406                                CKLOOP
12071  034406  104406                        TRAP    C$CLP1
12072  034410  005037  002402        10$:    CLR     R4LOAD                  ;NOT LOAD REMAINING AND ARRAYS TO 0
12073  034414  005237  002376                INC     R2LOAD                  ;UPDATE POINTER TO NEXT AND ARRAY
12074  034420  022737  000017  002376        CMP     #PTER15,R2LOAD          ;CHECK IF ALL AND ARRAYS WRITTEN
12075  034426  001350                        BNE     8$                      ;IF NOT THEN LOAD 0 INTO NEXT ARRAY
```

```
12076
12077                                           ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTRROL REG 2
12078
12079  034430  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12080  034434  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
12081  034436                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12082  034436  104455                          TRAP    C$ERDF
12083  034440  000002                          .WORD   2
12084  034442  000000                          .WORD   0
12085  034444  004704                          .WORD   R2EROR
12086  034446                                  CKLOOP
12087  034446  104406                          TRAP    C$CLP1
12088
12089                                           ;SELECT ADDRESS TWO IN THE OR ADDRESS REGISTER. LOCATION 2 WILL BE
12090                                           ;WRITTEN WITH DATA TO SET SBL59 FLIP-FLOP LATER ON IN TEST.
12091
12092  034450  012737  000002  002414  11$:     MOV     #2,R6LOAD               ;SETUP ADDRESS TO BE LOADED
12093  034456  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12094  034464  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
12095  034470  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
12096  034472                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER ERROR - ORAD 3:0
12097  034472  104455                          TRAP    C$ERDF
12098  034474  000004                          .WORD   4
12099  034476  003161                          .WORD   ORADER
12100  034500  004734                          .WORD   R026ER
12101  034502                                  CKLOOP
12102  034502  104406                          TRAP    C$CLP1
12103
12104                                           ;LOAD LOCATION TWO OF THE OR ARRAY RAMS WITH DATA EQUAL TO 40.  THIS
12105                                           ;DATA PATTERN WILL SET THE SIGNLA ORO5 L TO THE LOW STATE AND ALL OTHER
12106                                           ;OR ARRAY DATA BITS TO THE HIGH STATE.  THIS DATA PATTERN WILL CAUSE
12107                                           ;SBL59 FLIP-FLOP TO BE SET TO THE HIGH STATE LATER ON IN THE TEST.
12108
12109  034504  012737  000040  002402  12$.     MOV     #BIT5,R4LOAD            ;SETUP DATA TO BE LOADED
12110  034512  012737  177400  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
12111  034520  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
12112  034524  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
12113  034526                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA ERROR
12114  034526  104455                          TRAP    C$ERDF
12115  034530  000003                          .WORD   3
12116  034532  003512                          .WORD   ORDATA
12117  034534  004720                          .WORD   R4EROR
12118  034536                                  CKLOOP
12119  034536  104406                          TRAP    C$CLP1
12120
12121                                           ;SET CDAL4 TO A 1 IN CONTROL REGISTER 0. CDAL4 ON A 1 WILL ENABLE THE
12122                                           ;OUTPUTS OF ALL THE AND AND OR ARRAY RAMS AT THE SAME TIME.
12123
12124  034540  052737  000020  002370  13$.     BIS     #CDAL4,ROLOAD           ;SETUP BE TO BE CLEARED
12125  034546  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12126  034552  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
12127  034554                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12128  034554  104455                          TRAP    C$ERDF
12129  034556  000001                          .WORD   1
12130  034560  000000                          .WORD   0
12131  034562  004604                          .WORD   ROEROR
```

```
12132  034564                                  CKLOOP
12133  034564  104406                          TRAP    C$CLP1
12134
12135                                          ;READ BOTH THE AND ARRAY RAM AND THE OR ARRAY RAMS DATA.  A DATA
12136                                          ;PATTERN OF 15 WAS WRITTEN INTO THE FIRST AND ARRAY AND ALL ZEROES
12137                                          ;WERE WRITTEN INTO THE REMAINING AND ARRAYS.  A DATA PATTERN EQUAL
12138                                          ;TO 15 SHOULD BE READ BACK FROM THE AND ARRAY DO TO THE WIRED OR
12139                                          ;EFFECT OF THE AND ARRAY OUTPUTS.  A DATA PATTERN EQUAL TO 40 SHOULD
12140                                          ;BE READ BACK FROM THE OR ARRAY RAMS.
12141
12142  034566  112737  000015  002405  14$:   MOVB    #15,R4GOOD+1            ;ADD AND ARRAY DATA TO OR ARRAY DATA
12143  034574  012737  170000  002406        MOV     #170000,R4MASK          ;SETUP TO CHECK AND/OR ARRAY DATA
12144  034602  004737  006216                JSR     PC,READR4               ;GO READ AND CHECK AND/OR ARRAY DATA
12145  034606  001405                        BEQ     15$                     ;IF DATA OK THEN CONTINUE
12146  034610                                ERRDF   3,ANDOR,R4EROR          ;AND/OR ARRAY RAM DATA ERROR
12147  034610  104455                        TRAP    C$ERDF
12148  034612  000003                        .WORD   3
12149  034614  003647                        .WORD   ANDOR
12150  034616  004720                        .WORD   R4EROR
12151  034620                                CKLOOP
12152  034620  104406                        TRAP    C$CLP1
12153
12154                                          ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0 TO CAUSE THE FOUT FLIP-
12155                                          ;FLOPS TO BE USED TO ADDRESS THE OR ARRAY RAMS.
12156
12157  034622  052737  000200  002370  15$:   BIS     #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
12158  034630  004737  006102                JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12159  034634  001405                        BEQ     16$                     ;IF LOADED OK THEN CONTINUE
12160  034636                                ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12161  034636  104455                        TRAP    C$ERDF
12162  034640  000001                        .WORD   1
12163  034642  000000                        .WORD   0
12164  034644  004604                        .WORD   ROEROR
12165  034646                                CKLOOP
12166  034646  104406                        TRAP    C$CLP1
12167
12168                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING CDAL6
12169                                          ;WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED, WHICH WILL
12170                                          ;CAUSE THE SIGNAL ANST L TO BE PULSED, WHICH WILL CAUSE THE SIGNAL
12171                                          ;ORST L TO BE PULSED.  WHEN THE SIGNAL ANST L IS PULSED
12172                                          ;A COUNT DOWN PULSE WILL BE ISSUED TO EVENT COUNTER 1 BECAUSE OF THE
12173                                          ;AND ARRAY DATA PATTERN (15).  A BORROW SHOULD BE GENERATED FOR EVENT
12174                                          ;COUNTER 1 BECAUSE ALL ZEROES WERE LOADED INTO THE EVENT COUNTERS. A
12175                                          ;BORROW BEING GENERATED ALONG WITH THE COUNT DOWN PULSE WILL CAUSE THE
12176                                          ;OUTPUT OF THE FOUT1 FLIP-FLOP TO GO TO THE LOW STATE, THUS SELECTING
12177                                          ;ADDRESS TWO ON THE OR ADDRESS LINES ORAD 3:0.  SBL57 FLIP-FLOP SHOULD
12178                                          ;ALSO GET SET AS A RESULT OF THE BORROW AND THE COUNT DOWN PULSE.  WHEN
12179                                          ;THE SIGNAL ORST L IS PULSED, DATA BITS 4 AND 5 OF ADDRESS TWO OF
12180                                          ;THE OR ARRAY RAM WILL BE LOADED INTO SBL FLIP-FLOPS 59 AND 58, THUS
12181                                          ;SETTING SBL59 FLIP-FLOP TO THE HIGH STATE.
12182
12183  034650  004737  006640          16$:   JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
12184
12185                                          ;WITH CDAL7 SET TO A ONE, READ CONTROL REGISTER 6 TO CHECK THAT ONLY
12186                                          ;FOUT1 FLIP-FLOP IS SET TO A ONE.  THE FOUT FLIP-FLOPS ARE USED TO
12187                                          ;ADDRESS THE OR ADDRESS REGISTER VIA SIGNAL LINES ORAD 3:0.
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12188
12189  034654  012737  000002  002414  18$:    MOV     #2,R6LOAD               ;SETUP EXPECTED ADDRESS TO BE TWO
12190  034662  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12191  034670  004737  006256                  JSR     PC,READR6               ;GO READ FOUT FLIP-FLOPS 3:0
12192  034674  001405                          BEQ     19$                     ;IF EQUAL TO A ONE THEN CONTINUE
12193  034676                                  ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
12194  034676  104455                          TRAP    C$ERDF
12195  034700  000004                          .WORD   4
12196  034702  003213                          .WORD   EVNTCT
12197  034704  005024                          .WORD   EVNTER
12198  034706                                  CKLOOP
12199  034706  104406                          TRAP    C$CLP1
12200
12201                                          ;SET CDAL3 TO A ONE AND CDAL2 TO A ZERO IN CONTROL REGISTER 0 TO
12202                                          ;ASSERT THE SIGNAL TRSL2 L. THIS SIGNAL WILL ALLOW THE SBL FLIP-FLOPS
12203                                          ;TO BE READBACK ON THE TRDI 59:56 SIGNAL LINES.
12204
12205  034710  052737  000010  002370  19$:    BIS     #CDAL3,R0LOAD           ;SETUP BITS TO BE LOADED
12206  034716  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12207  034722  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
12208  034724                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12209  034724  104455                          TRAP    C$ERDF
12210  034726  000001                          .WORD   1
12211  034730  000000                          .WORD   0
12212  034732  004604                          .WORD   R0EROR
12213  034734                                  CKLOOP
12214  034734  104406                          TRAP    C$CLP1
12215
12216                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REG VIA CONTROL REG 2. THIS IS
12217                                          ;DONE TO SETUP FOR READBACK OF THE SBL F/F'S ON TRDI 59:56 SIGNAL LINES
12218
12219  034736  012737  000004  002376  20$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12220  034744  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12221  03475C  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
12222  034752                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12223  034752  104455                          TRAP    C$ERDF
12224  034754  000002                          .WORD   2
12225  034756  000000                          .WORD   0
12226  034760  004704                          .WORD   R2EROR
12227  034762                                  CKLOOP
12228  034762  104406                          TRAP    C$CLP1
12229
12230                                          ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59 AND 57 ARE
12231                                          ;SET AND THAT SBL FLIP-FLOPS 58 AND 56 ARE CLEARED.  SBL BITS 59:56
12232                                          ;ARE READBACK ON TRDI 59:56 SIGNAL LINES WHEN TRSL2 L IS ASSERTED.
12233
12234  034764  012737  005000  002414  21$:    MOV     #BIT11!BIT9,R6LOAD      ;SETUP TO EXPECT SBL 59 AND 57 SET
12235  034772  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY SBL BITS
12236  035000  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL BITS
12237  035004  001405                          BEQ     22$                     ;IF SBL 58 AND 56 SET THEN CONT
12238  035006                                  ERRDF   4,SBLERR,R026ER         ;SBL 59:56 FLIP-FLOP ERROR
12239  035006  104455                          TRAP    C$ERDF
12240  035010  000004                          .WORD   4
12241  035012  003416                          .WORD   SBLERR
12242  035014  004734                          .WORD   R026ER
12243  035016                                  CKLOOP
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12244  035016  104406                          TRAP    C$CLP1
12245
12246                                          ;LOAD EVENT COUNTERS 1 AND 3 AGAIN WITH 0 TO CHECK THAT THE SBL
12247                                          ;FLIP-FLOPS ARE CLEARED WHEN THE SIGNALS W10 L AND W12 L ARE ISSUED
12248                                          ;FROM LOADING THE EVENT COUNTERS.
12249
12250  035020  012737  000012  002376  22$:    MOV     #PTER10,R2LOAD          ;SETUP BITS TO BE LOADED
12251  035026  004737  006134          23$:    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12252  035032  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
12253  035034                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12254  035034  104455                          TRAP    C$ERDF
12255  035036  000002                          .WORD   2
12256  035040  000000                          .WORD   0
12257  035042  004704                          .WORD   R2EROR
12258  035044                                  CKLOOP
12259  035044  104406                          TRAP    C$CLP1
12260  035046  012777  000000  145302  24$:    MOV     #0,@REG6                ;CLEAR EVENT COUNTERS 1 AND 3
12261  035054  022737  000014  002376          CMP     #PTER12,R2LOAD          ;CHECK TO EVENT COUNTER 2 LOADED YET
12262  035062  001404                          BEQ     25$                     ;IF YES THEN CONTINUE
12263  035064  062737  000002  002376          ADD     #2,R2LOAD               ;UPDATE POINTER REGISTER TO COUNTER 3
12264  035072  000755                          BR      23$                     ;GO LOAD EVENT COUNTER 2
12265
12266                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
12267                                          ;READBACK OF THE SBL BITS ON THE TRDI SIGNAL LINES 59:56.  WITH THE
12268                                          ;SIGNAL TRSL2 L ASSERTED, THE SBL FLIP-FLOPS WILL BE READBACK ON
12269                                          ;TRDI BITS 59:56 WHEN A READ COMMAND IS ISSUED TO CONTROL REGISTER 6.
12270
12271  035074  012737  000004  002376  25$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12272  035102  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12273  035106  001405                          BEQ     26$                     ;IF LOADED OK THEN CONTINUE
12274  035110                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12275  035110  104455                          TRAP    C$ERDF
12276  035112  000002                          .WORD   2
12277  035114  000000                          .WORD   0
12278  035116  004704                          .WORD   R2EROR
12279  035120                                  CKLOOP
12280  035120  104406                          TRAP    C$CLP1
12281
12282                                          ;READ CONTROL REGISTER 6 AGAIN TO CHECK THAT LOADING EVENT COUNTERS
12283                                          ;1 AND 3 CLEARED SBL FLIP-FLOPS 59 AND 57.
12284
12285  035122  005037  002414          26$:    CLR     R6LOAD                  ;SETUP TO EXPECT SBL FLIP-FLOPS AS 0
12286  035126  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL FLIP-FLOPS
12287  035132  001404                          BEQ     27$                     ;IF SBL F/F'S = 0 THEN CONTINUE
12288  035134                                  ERRDF   4,SBLERR,R026ER         ;WRITING EVNT CNTR'S FAILED TO 0 SBL F/F''
12289  035134  104455                          TRAP    C$ERDF
12290  035136  000004                          .WORD   4
12291  035140  003416                          .WORD   SBLERR
12292  035142  004734                          .WORD   R026ER
12293  035144                          27$:    ENDSEG
12294  035144                          10000$:
12295  035144  104405                          TRAP    C$ESEG
12296  035146                                  ENDTST
12297  035146                          L10170:
12298  035146  104401                          TRAP    C$ETST
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12299                                   .SBTTL  TEST 63: CHECK SBL FLIP-FLOPS 59:56 TO CLEAR VIA CDALO
12300
12301                                   ;++
12302                                   ; THIS TEST WILL CHECK THAT SBL 59:56 FLIP-FLOPS CAN BE SET AND THAT THEY CAN BE
12303                                   ; CLEARED BY SETTING AND CLEARING CDALO IN CONTROL REGISTER 0.  SBL57 AND SBL56
12304                                   ; ARE SET VIA A BORROW FROM EVENT COUNTER 0 AND EVENT COUNTER 1 ALONG WITH THE
12305                                   ; APPROPRIATE COUNT DOWN PULSES.  SBL59 AND SBL58 ARE SET BY "OR ARRAY RAM" DATA
12306                                   ; BITS "ORO5 L" AND "ORO4 L" BEING SET LOW AND THE SIGNAL ORST L BEING
12307                                   ; PULSED.  THE TEST WILL CHECK THAT THE SBL 59:56 FLIP-FLOPS GOT SET BY READING
12308                                   ; THE SBL 59:56 FLIP-FLOPS BACK ON THE TRACE RAM DATA IN BUS BITS TRDI 59:56
12309                                   ; WHEN THE SIGNAL "TRSL2 L" IS ASSERTED LOW.  THE TEST WILL THEN SET AND CLEAR
12310                                   ; CDALO IN CONTROL REGISTER 0 TO CLEAR THE SBL 59:56 FLIP-FLOPS.  THE TEST WILL
12311                                   ; THEN CHECK THAT THE SBL 59:56 FLIP-FLOPS GOT CLEARED.
12312                                   ;--
12313
12314  035150                                   BGNTST
12315  035150                           T63::
12316  035150  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
12317
12318  035154                                   BGNSEG
12319  035154  104404                          TRAP    C$BSEG
12320
12321                                           ;CLEAR CDAL4 IN CONTROL REGISTER 0. CDAL4 ON A ZERO WILL ALLOW ONLY ONE
12322                                           ;AND/OR ARRAY RAM TO BE SELECTED AT A TIME.
12323
12324  035156  105037  002370                  CLRB    #OLOAD                  ;SETUP BITS TO BE LOADED
12325  035162  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12326  035166  001405                          BEQ     1$                      ;IF LOADED OK THEN CONTINUE
12327  035170                                   ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12328  035170  104455                          TRAP    C$ERDF
12329  035172  000001                          .WORD   1
12330  035174  000000                          .WORD   0
12331  035176  004604                          .WORD   R0EROR
12332  035200                                   CKLOOP
12333  035200  104406                          TRAP    C$CLP1
12334
12335                                           ;THE FOLLOWING LOOP WILL LOAD ZEROES INTO EACH OF THE EVENT COUNTER
12336                                           ;REGISTERS AND EVENT COUNTERS.  BY LOADING EACH EVENT COUNTER, THE
12337                                           ;SBL FLIP-FLOPS 59:56 WILL BE CLEARED BY SIGNALS W9 L, W10 L, W11 L,
12338                                           ;AND W12 L.
12339
12340  035202  012737  000011  002376  1$:      MOV     #PTER9,R2LOAD           ;SETUP TO START LOADING AT COUNTER 0
12341  035210  004737  006134          2$:      JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12342  035214  001405                          BEQ     3$                      ;IF LOADED OK THEN CONTINUE
12343  035216                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12344  035216  104455                          TRAP    C$ERDF
12345  035220  000002                          .WORD   2
12346  035222  000000                          .WORD   0
12347  035224  004704                          .WORD   R2EROR
12348  035226                                   CKLOOP
12349  035226  104406                          TRAP    C$CLP1
12350  035230  012777  000000  145120  3$:      MOV     #0,@REG6                ;LOAD ALL ZEROES INTO EVENT COUNTERS
12351  035236  005237  002376                  INC     R2LOAD                  ;UPDATE THE POINTER TO NEXT COUNTER
12352  035242  022737  000015  002376          CMP     #PTER13,R2LOAD          ;CHECK IF ALL EVENT COUNTERS LOADED
12353  035250  001357                          BNE     2$                      ;IF NOT THEN LOAD THE NEXT EVENT COUNTER
12354
```

```
12355                                          ;SET CDAL3 TO A ONE AND CDAL2 TO A 0 IN CONTROL REGISTER 0 TO SET THE
12356                                          ;SIGNAL TRSL2 L. THE SIGNAL TRSL2 L WILL ALLOW SBL BITS 59:56 TO BE
12357                                          ;READBACK ON TRDI BITS 59:56.
12358
12359  035252  052737  000010  002370          BIS     #CDAL3,ROLOAD           ;SETUP BITS TO BE LOADED
12360  035260  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12361  035264  001405                          BEQ     4$                      ;IF LOADED OK THEN CONTINUE
12362  035266                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED.
12363  035266  104455                          TRAP    C$ERDF
12364  035270  000001                          .WORD   1
12365  035272  000000                          .WORD   0
12366  035274  004604                          .WORD   ROEROR
12367  035276                                  CKLOOP
12368  035276  104406                          TRAP    C$CLP1
12369
12370                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
12371                                          ;2.  THIS IS DONE TO SETUP FOR A READBACK OF TRDI BITS 59:48.
12372
12373  035300  012737  000004  002376  4$:     MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12374  035306  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12375  035312  001405                          BEQ     5$                      ;IF LOADED OK THEN CONTINUE
12376  035314                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12377  035314  104455                          TRAP    C$ERDF
12378  035316  000002                          .WORD   2
12379  035320  000000                          .WORD   0
12380  035322  004704                          .WORD   R2EROR
12381  035324                                  CKLOOP
12382  035324  104406                          TRAP    C$CLP1
12383
12384                                          ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59:56 ARE CLEARED.
12385                                          ;SBL BITS 59:56 ARE READBACK ON TRDI BITS 59:56 WHEN THE SIGNAL TRSL2 L
12386                                          ;IS ASSERTED.  THE SBL FLIP-FLOPS SHOULD HAVE BEEN CLEARED WHEN THE
12387                                          ;EVENT COUNTERS WERE LOADED.
12388
12389  035326  005037  002414          5$:     CLR     R6LOAD                  ;SETUP EXPECTED DATA
12390  035332  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY TRDI 59:56 BITS
12391  035340  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL 59:56 BITS
12392  035344  001405                          BEQ     6$                      ;IF ALL FLIP-FLOPS CLEARED THEN CONT
12393  035346                                  ERRDF   4,SBLERR,R026ER         ;WRITING EVENT COUNTERS FAILED TO
12394  035346  104455                          TRAP    C$ERDF
12395  035350  000004                          .WORD   4
12396  035352  003416                          .WORD   SBLERR
12397  035354  004734                          .WORD   R026ER
12398  035356                                  CKLOOP
12399  035356  104406                          TRAP    C$CLP1
12400                                                                          ;ZERO SBL FLIP-FLOPS 59:56
12401
12402                                          ;CLEAR CDAL3 IN CONTROL REGISTER 0 TO ASSERT THE SIGNAL TRSL0 L. THE
12403                                          ;SIGNAL TRSL0 L WILL ENABLE THE OUTPUTS OF THE TRACE RAM DATA IN BUFFERS
12404
12405  035360  042737  000010  002370  6$:     BIC     #CDAL3,ROLOAD           ;SETUP BIT TO BE CLEARED
12406  035366  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12407  035372  001405                          BEQ     7$                      ;IF LOADED OK THEN CONTINUE
12408  035374                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12409  035374  104455                          TRAP    C$ERDF
12410  035376  000001                          .WORD   1
```

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12411  035400  000000                          .WORD   0
12412  035402  004604                          .WORD   R0EROR
12413  035404                                  CKLOOP
12414  035404  104406                          TRAP    C$CLP1
12415
12416                                          ;THE FOLLOWING SECTION OF CODE WILL LOAD ALL ZEROES INTO ALL THE TRACE
12417                                          ;RAM DATA IN BUFFERS.  THIS WILL SELECT ADDRESS ZERO OF ALL THE AND
12418                                          ;ARRAYS.
12419
12420  035406  005037  002414          7$:     CLR     R6LOAD                  ;SETUP TO LOAD ALL ZEROES
12421  035412  005037  002416                  CLR     R6MASK                  ;SETUP TO CHECK ALL BITS
12422
12423                                          ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 15:0
12424
12425  035416  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12426  035422  000005                          .WORD   PTER5                   ;SELECT TRDI BITS 15:0
12427
12428                                          ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 31:16
12429
12430  035424  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12431  035430  000006                          .WORD   PTER6                   ;SELECT TRDI BITS 31:16
12432
12433                                          ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 47:32
12434
12435  035432  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12436  035436  000007                          .WORD   PTER7                   ;SELECT TRDI BITS 47:32
12437
12438                                          ;LOAD ALL ZEROES INTO TRACE RAM DATA IN BUFFER BITS TRDI 59:48
12439
12440  035440  004537  006426                  JSR     R5,TRDIBF               ;LOAD, READ AND CHECK TRAM DATA IN BUF
12441  035444  000010                          .WORD   PTER8                   ;SELECT TRDI BITS 59:48
12442
12443                                          ;THE FOLLOWING SECTION OF CODE WILL WRITE DATA EQUAL TO 14 INTO ADDRESS
12444                                          ;ZERO OF THE AND ARRAY SELECTED BY PTER0 L. THE REMAINING AND ARRAYS
12445                                          ;WILL BE WRITTEN WITH DATA EQUAL TO ZERO.
12446
12447  035446  012737  000000  002376          MOV     #PTER0,R2LOAD           ;SETUP TO SELECT AND ARRAY ZERO
12448  035454  012737  000014  002402          MOV     #14,R4LOAD              ;SETUP DATA FOR THE FIRST AND ARRAY
12449  035462  012737  170377  002406          MOV     #170377,R4MASK          ;SETUP TO CHECK ONLY AND ARRAY DATA BITS
12450  035470  004737  006134          8$:     JSR     PC,LDRDR2               ;LOAD, READ AND CHECK CONTROL REG 2
12451  035474  001405                          BEQ     9$                      ;IF LOADED OK THEN GO WRITE DATA
12452  035476                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12453  035476  104455                          TRAP    C$ERDF
12454  035500  000002                          .WORD   2
12455  035502  000000                          .WORD   0
12456  035504  004704                          .WORD   R2EROR
12457  035506                                  CKLOOP
12458  035506  104406                          TRAP    C$CLP1
12459  035510  004737  006166          9$:     JSR     PC,LDRDAR               ;GO LOAD, READ AND CHECK AND ARRAY
12460  035514  001405                          BEQ     1^$                     ;IF LOADED OK THEN CONTINUE
12461  035516                                  ERRDF   3,ANDERR,R4EROR         ;AND ARRAY DATA ERROR
12462  035516  104455                          TRAP    C$ERDF
12463  035520  000003                          .WORD   3
12464  035522  003550                          .WORD   ANDERR
12465  035524  004720                          .WORD   R4EROR
12466  035526                                  CKLOOP
```

```
12467  035526  104406                          TRAP    C$CLP1
12468  035530  005037  002402          10$:    CLR     R4LOAD                  ;NOT LOAD REMAINING AND ARRAYS TO 0
12469  035534  005237  002376                  INC     R2LOAD                  ;UPDATE POINTER TO NEXT AND ARRAY
12470  035540  022737  000017  002376          CMP     #PTER15,R2LOAD          ;CHECK IF ALL AND ARRAYS WRITTEN
12471  035546  001350                          BNE     8$                      ;IF NOT THEN LOAD C INTO NEXT ARRAY
12472
12473                                          ;ASSERT THE SIGNAL PTER15 L IN THE POINTER REGISTER VIA CONTRROL REG 2
12474
12475  035550  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12476  035554  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
12477  035556                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12478  035556  104455                          TRAP    C$ERDF
12479  035560  000002                          .WORD   2
12480  035562  000000                          .WORD   0
12481  035564  004704                          .WORD   R2EROR
12482  035566                                  CKLOOP
12483  035566  104406                          TRAP    C$CLP1
12484
12485                                          ;SELECT ADDRESS THREE IN THE OR ADDRESS REGISTER. LOCATION 3 WILL BE
12486                                          ;WRITTEN WITH DATA TO SET SBL59 AND SBL58 FLIP-FLOPS LATER ON IN TEST.
12487
12488  035570  012737  000003  002414  11$:    MOV     #3,R6LOAD               ;SETUP ADDRESS TO BE LOADED
12489  035576  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12490  03560'  004737  006250                  JSR     PC,LDRDR6               ;GO LOAD, READ AND CHECK OR ADDRESS REG
12491  035610  001405                          BEQ     12$                     ;IF LOADED OK THEN CONTINUE
12492  035612                                  ERRDF   4,ORADER,R026ER         ;OR ADDRESS REGISTER ERROR - ORAD 3:0
12493  035612  104455                          TRAP    C$ERDF
12494  035614  000004                          .WORD   4
12495  035616  003161                          .WORD   ORADER
12496  035620  004734                          .WORD   R026ER
12497  035622                                  CKLOOP
12498  035622  104406                          TRAP    C$CLP1
12499
12500                                          ;LOAD LOCATION 3 OF THE OR ARRAY RAMS WITH DATA EQUAL TO 60.  THIS DATA
12501                                          ;PATTERN WILL SET THE SIGNAL OR05 L AND OR06 L TO THE LOW STATE AND ALL
12502                                          ;OTHER OR ARRAY DATA BITS TO THE HIGH STATE.  THIS DATA PATTERN WILL
12503                                          ;CAUSE SBL59 AND SBL58 FLIP-FLOPS TO BE SET TO THE HIGH STATE LATER
12504                                          ;ON IN THIS TEST.
12505
12506  035624  012737  000060  002402  12$:    MOV     #BIT5!BIT4,R4LOAD       ;SETUP DATA TO BE LOADED
12507  035632  012737  177'00  002406          MOV     #177400,R4MASK          ;SETUP TO IGNORE UNWANTED BITS
12508  035640  004737  006202                  JSR     PC,LDRDR4               ;GO LOAD, READ AND CHECK OR ARRAY RAM
12509  035644  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
12510  035646                                  ERRDF   3,ORDATA,R4EROR         ;OR ARRAY DATA ERROR
12511  035646  104455                          TRAP    C$ERDF
12512  035650  000003                          .WORD   3
12513  035652  003512                          .WORD   ORDATA
12514  035654  004720                          .WORD   R4EROR
12515  035656                                  CKLOOP
12516  035656  104406                          TRAP    C$CLP1
12517
12518                                          ;SET CDAL4 TO A 1 IN CONTROL REGISTER 0. CDAL4 ON A 1 WILL ENABLE THE
12519                                          ;OUTPUTS OF ALL THE AND AND OR ARRAY RAMS AT THE SAME TIME.
12520
12521  035660  052737  000020  002370  13$:    BIS     #CDAL4,RCLOAD           ;SETUP BE TO BE CLEARED
12522  035666  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
```

```
12523  035672  001405                          BEQ     14$                     ;IF LOADED OK THEN CONTINUE
12524  035674                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12525  035674  104455                          TRAP    C$ERDF
12526  035676  000001                          .WORD   1
12527  035700  000000                          .WORD   0
12528  035702  004604                          .WORD   ROEROR
12529  035704                                  CKLOOP
12530  035704  104406                          TRAP    C$CLP1
12531
12532                                          ;READ BOTH THE AND ARRAY RAM AND THE OR ARRAY RAMS DATA.  A DATA
12533                                          ;PATTERN OF 14 WAS WRITTEN INTO THE FIRST AND ARRAY AND ALL ZEROES
12534                                          ;WERE WRITTEN INTO THE REMAINING AND ARRAYS.  A DATA PATTERN EQUAL
12535                                          ;TO 14 SHOULD BE READ BACK FROM THE AND ARRAY DO TO THE WIRED OR
12536                                          ;EFFECT OF THE AND ARRAY OUTPUTS.  A DATA PATTERN EQUAL TO 60 SHOULD
12537                                          ;BE READ BACK FROM THE OR ARRAY RAMS.
12538
12539  035706  112737  000014  002405  14$:   MOVB    #14,R4GOOD+1            ;ADD AND ARRAY DATA TO OR ARRAY DATA
12540  035714  012737  170000  002406        MOV     #170000,R4MASK          ;SETUP TO CHECK AND/OR ARRAY DATA
12541  035722  004737  006216                JSR     PC,READR4               ;GO READ AND CHECK AND/OR ARRAY DATA
12542  035726  001405                          BEQ     15$                     ;IF DATA OK THEN CONTINUE
12543  035730                                  ERRDF   3,ANDOR,R4EROR          ;AND/OR ARRAY RAM DATA ERROR
12544  035730  104455                          TRAP    C$ERDF
12545  035732  000003                          .WORD   3
12546  035734  003647                          .WORD   ANDOR
12547  035736  004720                          .WORD   R4EROR
12548  035740                                  CKLOOP
12549  035740  104406                          TRAP    C$CLP1
12550
12551                                          ;SET CDAL7 TO A ONE IN CONTROL REGISTER 0 TO CAUSE THE F   FLIP-
12552                                          ;FLOPS TO BE USED TO ADDRESS THE OR ARRAY RAMS.
12553
12554  035742  052737  000200  002370  15$:   BIS     #CDAL7,ROLOAD           ;SETUP BIT TO BE LOADED
12555  035750  004737  006102                JSR     PC,LDRDR0               ;LOAD, READ AND CHECK REGISTER 0
12556  035754  001405                          BEQ     16$                     ;IF LOADED OK THEN CONTINUE
12557  035756                                  ERRDF   1,,ROEROR               ;REGISTER 0 NOT EQUAL EXPECTED
12558  035756  104455                          TRAP    C$ERDF
12559  035760  000001                          .WORD   1
12560  035762  000000                          .WORD   0
12561  035764  004604                          .WORD   ROEROR
12562  035766                                  CKLOOP
12563  035766  104406                          TRAP    C$CLP1
12564
12565                                          ;SET AND CLEAR CDAL6 IN CONTROL REGISTER 0.  SETTING AND CLEARING CDAL6
12566                                          ;WILL CAUSE THE SIGNALS TRANST H AND TRST L TO BE PULSED, WHICH WILL
12567                                          ;CAUSE THE SIGNAL ANST L TO BE PULSED, WHICH WILL CAUSE THE SIGNAL
12568                                          ;ORST L TO BE PULSED.  WHEN THE SIGNAL ANST L IS PULSED,
12569                                          ;A COUNT DOWN PULSE WILL BE ISSUED TO EVENT COUNTERS 0 AND 1 BECAUSE OF
12570                                          ;THE AND ARRAY DATA PATTERN (14). A BORROW SHOULD BE GENERATED FOR EVENT
12571                                          ;COUNTERS 0 + 1 BECAUSE ALL ZEROES WERE LOADED INTO THE EVENT COUNTERS.
12572                                          ;A BORROW BEING GENERATED ALONG WITH THE COUNT DOWN PULSE WILL CAUSE THE
12573                                          ;OUTPUT OF THE FOUT1 AND FOUT0 FLIP-FLOP TO GO TO THE LOW STATE, THUS
12574                                          ;SELECTING ADDRESS 3 ON THE OR ADDRESS LINES ORAD 3:0.  SBL57 AND SBL56
12575                                          ;FLIP-FLOPS SHOULD ALSO GET SET AS A RESULT OF THE BORROW AND THE COUNT
12576                                          ;COUNT DOWN PULSES.  WHEN THE SIGNAL ORST L IS PULSED, DATA BITS 4
12577                                          ;AND 5 OF ADDRESS 3 OF THE OR ARRAY RAM WILL BE LOADED INTO SBL FLIP-
12578                                          ;FLOPS 59 AND 58, THUS SETTING SBL59 AND SBL58 F/F'S TO THE HIGH STATE.
```

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12579
12580  035770  004737  006640          16$:    JSR     PC,TRANST               ;SET AND CLEAR CDAL6 IN CONTROL REG 0
12581
12582                                           ;WITH CDAL7 SET TO A ONE, READ CONTROL REGISTER 6 TO CHECK THAT ONLY
12583                                           ;FOUT1 AND FOUT0 F/F'S ARE SET TO A ONE.  THE FOUT F/F'SS ARE USED TO
12584                                           ;ADDRESS THE OR ADDRESS REGISTER VIA SIGNAL LINES ORAD 3:0.
12585
12586  035774  012737  000003  002414  18$:    MOV     #3,R6LOAD               ;SETUP EXPECTED ADDRESS TO BE TWO
12587  036002  012737  177760  002416          MOV     #177760,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12588  036010  004737  006256                  JSR     PC,READR6               ;GO READ FOUT FLIP-FLOPS 3:0
12589  036014  001405                          BEQ     19$                     ;IF EQUAL TO A ONE THEN CONTINUE
12590  036016                                   ERRDF   4,EVNTCT,EVNTER         ;EVENT COUNTER OR FOUT 3:0 ERROR
12591  036016  104455                          TRAP    C$ERDF
12592  036020  000004                          .WORD   4
12593  036022  003213                          .WORD   EVNTCT
12594  036024  005024                          .WORD   EVNTER
12595  036026                                   CKLOOP
12596  036026  104406                          TRAP    C$CLP1
12597
12598                                           ;SET CDAL3 TO A ONE AND CDAL2 TO A ZERO IN CONTROL REGISTER 0 TO
12599                                           ;ASSERT THE SIGNAL TRSL2 L. THIS SIGNAL WILL ALLOW THE SBL FLIP-FLOPS
12600                                           ;TO BE READBACK ON THE TRDI 59:56 SIGNAL LINES.
12601
12602  036030  052737  000010  002370  19$:    BIS     #CDAL3,R0LOAD           ;SETUP BITS TO BE LOADED
12603  036036  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12604  036042  001405                          BEQ     20$                     ;IF LOADED OK THEN CONTINUE
12605  036044                                   ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12606  036044  104455                          TRAP    C$ERDF
12607  036046  000001                          .WORD   1
12608  036050  000000                          .WORD   0
12609  036052  004604                          .WORD   R0EROR
12610  036054                                   CKLOOP
12611  036054  104406                          TRAP    C$CLP1
12612
12613                                           ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER VIA CONTROL REGISTER
12614                                           ;2.  THIS IS DONE TO SETUP FOR A READBACK OF THE SBL FLIP-FLOPS ON
12615                                           ;TRDI 59:56 SIGNAL LINES.
12616
12617  036056  012737  000004  002376  20$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12618  036064  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12619  036070  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
12620  036072                                   ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12621  036072  104455                          TRAP    C$ERDF
12622  036074  000002                          .WORD   2
12623  036076  000000                          .WORD   0
12624  036100  004704                          .WORD   R2EROR
12625  036102                                   CKLOOP
12626  036102  104406                          TRAP    C$CLP1
12627
12628                                           ;READ CONTROL REGISTER 6 TO CHECK THAT SBL FLIP-FLOPS 59:56 ARE SET.
12629                                           ;SBL BITS 59:56 ARE READBACK ON TRDI 59:56 SIGNAL LINES WHEN TRSL2 L IS
12630                                           ;ASSERTED.
12631
12632  036104  012737  007400  002414  21$:    MOV     #7400,R:LOAD            ;SETUP TO EXPECT SBL 59:56 SET
12633  036112  012737  170377  002416          MOV     #170377,R6MASK          ;SETUP TO CHECK ONLY SBL BITS
12634  036120  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL BITS
```

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12635  036124  001405                          BEQ     22$                     ;IF SBL 58 AND 56 SET THEN CONT
12636  036126                                  ERRDF   4,SBLERR,R026ER         ;SBL 59:56 FLIP-FLOP ERROR
12637  036126  104455                          TRAP    C$ERDF
12638  036130  000004                          .WORD   4
12639  036132  003416                          .WORD   SBLERR
12640  036134  004734                          .WORD   R026ER
12641  036136                                  CKLOOP
12642  036136  104406                          TRAP    C$CLP1
12643
12644                                          ;SET AND CLEAR CDALO IN CONTROL REGISTER 0 TO CLEAR SBL 59:56 F/F'S.
12645
12646  036140  052737  000001  002370  22$:    BIS     #CDALO,ROLOAD           ;SETUP BIT TO BE LOADED
12647  036146  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12648  036152  001405                          BEQ     23$                     ;IF LOADED OK THEN CONTINUE
12649  036154                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12650  036154  104455                          TRAP    C$ERDF
12651  036156  000001                          .WORD   1
12652  036160  000000                          .WORD   0
12653  036162  004604                          .WORD   R0ERCR
12654  036164                                  CKLOOP
12655  036164  104406                          TRAP    C$CLP1
12656  036166  042737  000001  002370  23$:    BIC     #CDALO,ROLOAD           ;SETUP TO CLEAR CDALO
12657  036174  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12658  036200  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
12659  036202                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12660  036202  104455                          TRAP    C$ERDF
12661  036204  000001                          .WORD   1
12662  036206  000000                          .WORD   0
12663  036210  004604                          .WORD   R0EROR
12664  036212                                  CKLOOP
12665  036212  104406                          TRAP    C$CLP1
12666
12667                                          ;READ CONTROL REGISTER 6 AGAIN TO CHECK THAT SETTING AND CLEARING
12668                                          ;CDALO IN CONTROL REGISTER 0 ZEROED SBL FLIP-FLOPS 59:56.
12669
12670  036214  005037  002414          24$:    CLR     R6LOAD                  ;SETUP TO EXPECT SBL FLIP-FLOPS AS 0
12671  036220  004737  006256                  JSR     PC,READR6               ;GO READ AND CHECK SBL FLIP-FLOPS
12672  036224  001404                          BEQ     25$                     ;IF SBL F/F'S = 0 THEN CONTINUE
12673  036226                                  ERRDF   4,SBLERR,R026ER         ;SETTING/CLEARING CDALO FAILED TO
12674  036226  104455                          TRAP    C$ERDF
12675  036230  000004                          .WORD   4
12676  036232  003416                          .WORD   SBLERR
12677  036234  004734                          .WORD   R026ER
12678                                                                          ;CLEAR THE SBL FLIP-FLOPS
12679  036236                          25$:    ENDSEG
12680  036236                          10000$:
12681  036236  104405                          TRAP    C$ESEG
12682  036240                                  ENDTST
12683  036240                          L10171:
12684  036240  104401                          TRAP    C$ETST
12685
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12686                                   .SBTTL  TEST 64: EXTERNAL PROBE LOGIC TEST
12687
12688                                   ;++
12689                                   ; IF THE OPERATOR ANSWERED YES TO THE HARDWARE QUESTION "EXTERNAL PROBE CON-
12690                                   ; NECTED", THE FOLLOWING TEST WILL BE EXECUTED, OTHERWISE, THE TEST WILL BE
12691                                   ; ABORTED.  BEFORE THIS TEST CAN BE PERFORMED, THE OPERATOR MUST PLUG THE
12692                                   ; EXTERNAL PROBE INTO THE STATE ANALYZER MODULE AND CONNECT THE PROBE LEADS
12693                                   ; 7:0 TO EVENT COUNTER 0 SIGNALS SDBL 7:0 H RESPECTIVELY.  THE PROBE'S "CLK"
12694                                   ; LEAD MUST BE CONNECTED TO EVENT COUNTER 1'S SIGNAL SDBL8 H.
12695                                   ;
12696                                   ; THIS TEST WILL CHECK THE EXTERNAL PROBE AND THE EXTERNAL PROBE LOGIC ON THE
12697                                   ; STATE ANALYZER MODULE.  DATA PATTERNS OF 252 AND 125 WILL BE LOADED INTO
12698                                   ; EVENT COUNTER 0 TO PROVIDE LOGIC LEVELS TO THE EXTERNAL PROBE'S INPUTS. THE
12699                                   ; SIGNAL SDBL8 H IN EVENT COUNTER 1 WILL BE SET AND CLEARED TO PRO IDE THE "CLK"
12700                                   ; SIGNAL FOR THE EXTERNAL PROBE'S INPUT.  WHEN PDAL4, IN CONTROL REGISTER 2, IS
12701                                   ; SET TO A ZERO AND THE CLK SIGNAL IS SET HIGH FROM A LOW STATE, EVENT COUNTER
12702                                   ; 0'S DATA WILL BE LOADED INTO EXTP 7:0 FLIP-FLOPS.  WHEN PDAL4 IS SET TO A ONE
12703                                   ; AND THE CLK SIGNAL IS SET LOW FROM A HIGH STATE, EVENT COUNTER 0'S DATA WILL
12704                                   ; BE LOADED INTO EXTP 7:0 FLIP-FLOPS.  THIS TEST WILL CHECK THAT THE CORRECT
12705                                   ; DATA IS LOADED INTO EXTP 7:0 FLIP-FLOPS AND THAT THE DATA IS ONLY LOADED ON
12706                                   ; THE CORRECT TRANSITION OF THE CLK SIGNAL.  EXTP 7:0 FLIP-FLOPS ARE READBACK
12707                                   ; OF THE TRACE RAM DATA IN BUS SIGNAL LINES TRDI 55:48 WHEN THE SIGNAL TRSL2 L
12708                                   ; IS ASSERTED LOW.
12709                                   ;--
12710
12711  036242                                   BGNTST
12712  036242                           T64::
12713  036242  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
12714  036246  005737  002366                  TST     EXTPRB                  ;CHECK IF EXTERNAL PROBE CONNECTED
12715  036252  001002                          BNE     1$                      ;IF YES THEN DO THE TEST
12716  036254                                   EXIT    TST                     ;OTHERWISE SKIP THE TEST
12717  036254  104432                          TRAP    C$EXIT
12718  036256  001046                          .WORD   L10172-.
12719  036260                           1$:     BGNSEG
12720  036260  104404                          TRAP    C$BSEG
12721
12722                                   ;ASSERT THE SIGNAL TRSL2 L BY SETTING THE SIGNAL CDAL3 TO A ONE IN
12723                                   ;CONTROL REGISTER 0.  TRSL2 L BEING ASSERTED WILL ENABLE THE OUTPUTS
12724                                   ;OF THE EXTP 7:0 FLIP-FLOPS ONTO THE TRACE RAM DATA IN BUS.  THE
12725                                   ;SIGNALS EXTP 7:0 WILL BE READBACK ON TRDI BITS 55:48 RESPECTIVELY.
12726
12727  036262  112737  000010  002370          MOVB    #CDAL3,ROLOAD           ;SETUP BIT TO BE LOADED
12728  036270  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REGISTER 0
12729  036274  001405                          BEQ     2$                      ;IF LOADED OK THEN CONTINUE
12730  036276                                   ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
12731  036276  104455                          TRAP    C$ERDF
12732  036300  000001                          .WORD   1
12733  036302  000000                          .WORD   0
12734  036304  004604                          .WORD   R0EROR
12735  036306                                   CKLOOP
12736  036306  10440(                          TRAP    C$CLP1
12737
12738                                   ;DURING THIS TEST, EVENT COUNTER 0 SIGNALS SDBL 7:0 MUST BE CONNECTED
12739                                   ;TO EXTERNAL PROBE SIGNALS EXT 7:0 RESPECTIVELY.  EVENT COUNTER 1
12740                                   ;SIGNAL SDBL8 MUST BE CONNECTED TO EXTERNAL PROBE SIGNAL CLK.
12741
```

```
12742                                          ;THE FOLLOWING SECTION OF CODE WILL LOAD EVENT COUNTER 0 WITH A DATA
12743                                          ;PATTERN OF 252 AND EVENT COUNTER 1 WITH A DATA PATTERN OF 0.  THE
12744                                          ;TEST WILL THEN LOAD EVENT COUNTER 1 WITH A DATA PATTERN OF 1 TO SET
12745                                          ;THE SIGNAL "CLK" TO THE HIGH STATE.  SETTING THE SIGNAL "CLK" TO THE
12746                                          ;HIGH STATE WITH PDAL4 ON A 0 WILL CAUSE EVENT COUNTER 0 DATA TO BE
12747                                          ;LOADED INTO EXTP 7:0 FLIP-FLOP'S.
12748
12749  036310  012701  000252          2$:    MOV     #252,R1                 ;SETUP EVENT COUNTER 0 DATA
12750  036314  012737  000011  002376        MOV     #PTER9,R2LOAD           ;SETUP TO SELECT EVENT COUNTER 0
12751  036322  004737  006134          3$:    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12752  036326  001405                        BEQ     4$                      ;IF LOADED OK THEN CONTINUE
12753  036330                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12754  036330  104455                        TRAP    C$ERDF
12755  036332  000002                        .WORD   2
12756  036334  000000                        .WORD   0
12757  036336  004704                        .WORD   R2EROR
12758  036340                                CKLOOP
12759  036340  104406                        TRAP    C$CLP1
12760  036342  010177  144010          4$:    MOV     R1,@REG6                ;WRITE DATA INTO EVENT COUNTER 0 OR 1
12761  036346  012737  000012  002376        MOV     #PTER10,R2LOAD          ;SETUP TO LOAD EVENT COUNTER 1
12762  036354  105701                        TSTB    R1                      ;CHECK IF JUST LOADED EVENT COUNTER 0
12763  036356  100002                        BPL     5$                      ;IF NO THEN CHECK EVENT COUNTER 1
12764  036360  005001                        CLR     R1                      ;SETUP EVENT COUNTER 0 DATA TO = 0
12765  036362  000757                        BR      3$                      ;GO LOAD EVENT COUNTER 1 WITH 0
12766  036364  001002          5$:    BNE     6$                      ;IF A ONE LOADED THEN GO READ DATA
12767  036366  005201                        INC     R1                      ;SETUP EVENT COUNTER 1 DATA TO = 1
12768  036370  000754                        BR      3$                      ;GO LOAD EVENT COUNTER 1 WITH 1
12769
12770                                          ;ASSERT PTER4 L IN THE POINTER REG TO ENABLE TRDI BITS 59:48 TO BE READ.
12771
12772  036372  012737  000004  002376  6$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12773  036400  004737  006134                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12774  036404  001405                        BEQ     7$                      ;IF LOADED OK THEN CONTINUE
12775  036406                                ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12776  036406  104455                        TRAP    C$ERDF
12777  036410  000002                        .WORD   2
12778  036412  000000                        .WORD   0
12779  036414  004704                        .WORD   R2EROR
12780  036416                                CKLOOP
12781  036416  104406                        TRAP    C$CLP1
12782
12783                                          ;READ TRDI BITS 55:48 TO CHECK THAT EVENT COUNTER 0 DATA WAS LOADED
12784                                          ;INTO EXTP 7:0 FLIP-FLOPS WHEN THE SIGNAL "CLK" WAS SET HIGH BY SETTING
12785                                          ;SDBL BIT 5 IN EVENT COUNTER 1.
12786
12787  036420  012737  000252  002414  7$:    MOV     #252,R6LOAD             ;SETUP EXPECTED DATA TO = EVNT CNTR 0
12788  036426  012737  177400  002416        MOV     #177400,R6MASK          ;SETUP TO IGNORE UNWANTED BITS
12789  036434  004737  006256                JSR     PC,READR6               ;GO READ EXTP 7:0 ON TRDI BITS 55:48
12790  036440  001405                        BEQ     8$                      ;IF DATA EQUAL DATA LOADED THEN CONT
12791  036442                                ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP ERROR OR LOGIC
12792  036442  104455                        TRAP    C$ERDF
12793  036444  000004                        .WORD   4
12794  036446  003450                        .WORD   EXTPER
12795  036450  004734                        .WORD   R026ER
12796  036452                                CKLOOP
12797  036452  104406                        TRAP    C$CLP1
```

```
12798
12799                                          ;LOAD EVENT COUNTER 0 WITH DATA EQUAL TO 125 AND LOAD EVENT COUNTER 1
12800                                          ;WITH DATA EQUAL TO 0 TO SET SET THE SIGNAL "CLK" TO THE LOW STATE.
12801                                          ;DATA (252) ALREADY IN THE EXTP 7:0 FLIP-FLOPS SHOULD NOT CHANGE BY
12802                                          ;SETTING THE SIGNAL "CLK" LOW.
12803
12804  036454  012701  000125          8$:     MOV     #125,R1                 ;SETUP EVENT COUNTER 0 DATA
12805  036460  012737  000011  002376          MOV     #PTER9,R2LOAD           ;SETUP TO SELECT EVENT COUNTER 0
12806  036466  004737  006134          10$:    JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12807  036472  001405                          BEQ     11$                     ;IF LOADED OK THEN CONTINUE
12808  036474                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12809  036474  104455                          TRAP    C$ERDF
12810  036476  000002                          .WORD   2
12811  036500  000000                          .WORD   0
12812  036502  004704                          .WORD   R2EROR
12813  036504                                  CKLOOP
12814  036504  104406                          TRAP    C$CLP1
12815  036506  010177  143644          11$:    MOV     R1,@REG6                ;LOAD EVENT COUNTER 0 OR 1
12816  036512  001404                          BEQ     12$                     ;EXIT IF EVENT COUNTER 1 LOADED
12817  036514  005237  002376                  INC     R2LOAD                  ;UPDATE POINTER TO EVENT COUNTER 1
12818  036520  005001                          CLR     R1                      ;SETUP TO LOAD EVENT COUNTER 1 WITH 0
12819  036522  000761                          BR      10$                     ;GO LOAD EVENT COUNTER 1 WITH 0
12820
12821                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO ENABLE THE
12822                                          ;READBACK OF TRDI BITS 59:48.
12823
12824  036524  012737  000004  002376  12$:    MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12825  036532  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12826  036536  001405                          BEQ     13$                     ;IF LOADED OK THEN CONTINUE
12827  036540                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12828  036540  104455                          TRAP    C$ERDF
12829  036542  000002                          .WORD   2
12830  036544  000000                          .WORD   0
12831  036546  004704                          .WORD   R2EROR
12832  036550                                  CKLOOP
12833  036550  104406                          TRAP    C$CLP1
12834
12835                                          ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE SIGNAL "CLK"
12836                                          ;TO THE LOW STATE DID NOT CHANGE THE PREVIOUS DATA (252) LOADED.
12837                                          ;AT THIS POINT THE DATA INPUTS TO THE EXTP 7:0 FLIP-FLOPS WILL
12838                                          ;EQUAL 125 WHICH IS THE DATA IN EVENT COUNTER 0.
12839
12840  036552  004737  006256          13$:    JSR     PC,READR6               ;GO CHECK EXTP F/F'S TO EQUAL 252
12841  036556  001405                          BEQ     14$                     ;IF DATA OK THEN CONTINUE
12842  036560                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOPS NOT EQUAL 252
12843  036560  104455                          TRAP    C$ERDF
12844  036562  000004                          .WORD   4
12845  036564  003450                          .WORD   EXTPER
12846  036566  004734                          .WORD   R026ER
12847  036570                                  CKLOOP
12848  036570  104406                          TRAP    C$CLP1
12849
12850                                          ;LOAD EVENT COUNTER 1 WITH DATA EQUAL TO 1 TO SET THE SIGNAL "CLK"
12851                                          ;TO THE HIGH STATE.  SETTING THE SIGNAL "CLK" TO THE HIGH STATE WILL
12852                                          ;LOAD THE DATA (125) FROM EVENT COUNTER 0 INTO EXTP 7:0 FLIP-FLOPS.
12853
```

```
12854  036572  012737  000012  002376  14$:    MOV     #PTER10,R2LOAD          ;SETUP TO SELECT EVENT COUNTER 1
12855  036600  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12856  036604  001405                          BEQ     15$                     ;IF LOADED OK THEN CONTINUE
12857  036606                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12858  036606  104455                          TRAP    C$ERDF
12859  036610  000002                          .WORD   2
12860  036612  000000                          .WORD   0
12861  036614  004704                          .WORD   R2EROR
12862  036616                                  CKLOOP
12863  036616  104406                          TRAP    C$CLP1
12864  036620  012777  000001  143530  15$:    MOV     #1,@REG6                ;WRITE 1 INTO EVENT COUNTER 1
12865
12866                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO ENABLE THE
12867                                          ;READBACK OF TRDI BITS 59:48
12868
12869  036626  012737  000004  002376          MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12870  036634  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12871  036640  001404                          BEQ     16$                     ;IF LOADED OK THEN CONTINUE
12872  036642                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12873  036642  104455                          TRAP    C$ERDF
12874  036644  000002                          .WORD   2
12875  036646  000000                          .WORD   0
12876  036650  004704                          .WORD   R2EROR
12877
12878                                          ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE SIGNAL "CLK"
12879                                          ;TO THE HIGH STATE LOADED THE DATA (125) FROM EVENT COUNTER 0 INTO
12880                                          ;EXTP 7:0 FLIP-FLOPS.
12881
12882  036652  012737  000125  002414  16$:    MOV     #125,R6LOAD             ;SETUP DATA LOADED INTO EVENT CNTR 0
12883  036660  004737  006256                  JSR     PC,READR6               ;GO READ EXTP 7:0 ON TRDI BITS 55:48
12884  036664  001405                          BEQ     17$                     ;IF DATA OK THEN CONTINUE
12885  036666                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP'S NOT EQUAL 125
12886  036666  104455                          TRAP    C$ERDF
12887  036670  000004                          .WORD   4
12888  036672  003450                          .WORD   EXTPER
12889  036674  004734                          .WORD   R026ER
12890  036676                                  CKLOOP
12891  036676  104406                          TRAP    C$CLP1
12892
12893                                          ;LOAD EVENT COUNTER 0 WITH DATA EQUAL TO 252 AND LOAD EVENT COUNTER 1
12894                                          ;WITH DATA EQUAL TO 0 TO SET THE SIGNAL "CLK" TO THE LOW STATE. THE
12895                                          ;EXTP 7:0 FLIP-FLOPS SHOULD REMAIN UNCHANGED WHEN THE "CLK" SIGNAL
12896                                          ;GOES FROM A HIGH LEVEL TO A LOW LEVEL WHEN THE SIGNAL PDAL4 IS A 0.
12897
12898  036700  012701  000252          17$:    MOV     #252,R1                 ;SETUP EVENT COUNTER 0 DATA
12899  036704  012737  000011  002376          MOV     #PTER9,R2LOAD           ;SETUP TO SELECT EVENT COUNTER 0
12900  036712  004737  006134          18$:    JSR     PC,LDRDR2               ;GO LOAD READ AND CHECK REGISTER 2
12901  036716  001405                          BEQ     19$                     ;IF LOADED OK THEN CONTINUE
12902  036720                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12903  036720  104455                          TRAP    C$ERDF
12904  036722  000002                          .WORD   2
12905  036724  000000                          .WORD   0
12906  036726  004704                          .WORD   R2EROR
12907  036730                                  CKLOOP
12908  036730  104406                          TRAP    C$CLP1
12909  036732  010177  143420          19$:    MOV     R1,@REG6                ;LOAD DATA INTO EVENT COUNTER 0 OR 1
```

```
12910  036736  001404                          BEQ     20$                     ;EXIT IF EVENT COUNTER 1 LOADED WITH 0
12911  036740  005237  002376                  INC     R2LOAD                  ;SETUP TO SELECT EVENT COUNTER 1
12912  036744  005001                          CLR     R1                      ;SETUP TO SET "CLK" TO A LOW STATE
12913  036746  000761                          BR      18$                     ;GO LOAD EVENT COUNTER 1
12914
12915                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
12916                                          ;READBACK OF TRDI BITS 59:48.
12917
12918  036750  012737  000004  002376  20$:   MOV     #PTER4,R2LOAD           ;SETUP BITS TO BE LOADED
12919  036756  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12920  036762  001405                          BEQ     21$                     ;IF LOADED OK THEN CONTINUE
12921  036764                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12922  036764  104455                          TRAP    C$ERDF
12923  036766  000002                          .WORD   2
12924  036770  000000                          .WORD   0
12925  036772  004704                          .WORD   R2EROR
12926  036774                                  CKLOOP
12927  036774  104406                          TRAP    C$CLP
12928
12929                                          ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE SIGNAL "CLK"
12930                                          ;TO THE LOW STATE DID NOT LOAD THE NEW EVENT COUNTER DATA (252) INTO
12931                                          ;THE EXTP 7:0 FLIP-FLOPS.
12932
12933  036776  004737  006256          21$:   JSR     PC,READR6               ;CHECK EXTP 7:0 F/F'S TO EQUAL 125
12934  037002  001405                          BEQ     22$                     ;IF DATA OK THEN CONTINUE
12935  037004                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP ERROR OR LOGIC
12936  037004  104455                          TRAP    C$ERDF
12937  037006  000004                          .WORD   4
12938  037010  003450                          .WORD   EXTPER
12939  037012  004734                          .WORD   R026ER
12940  037014                                  CKLOOP
12941  037014  104406                          TRAP    C$CLP1
12942
12943                                          ;SET THE SIGNAL PDAL4 TO A ONE IN CONTROL REGISTER 4 ALONG WITH THE
12944                                          ;BITS TO ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER.  SETTING
12945                                          ;PDAL4 TO A ONE WHEN THE SIGNAL "CLK" IS SET LOW, WILL CAUSE EVENT
12946                                          ;COUNTER 0 DATA (252), PREVIOULSY LOADED, TO BE LOADED INTO EXTP 7:0 F/F'S.
12947
12948  037016  052737  000020  002376  22$:   BIS     #PDAL4,R2LOAD           ;SETUP ADDITIONAL BIT TO BE LOADED
12949  037024  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12950  037030  001405                          BEQ     23$                     ;IF LOADED OK THEN CONTINUE
12951  037032                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12952  037032  104455                          TRAP    C$ERDF
12953  037034  000002                          .WORD   2
12954  037036  000000                          .WORD   0
12955  037040  004704                          .WORD   R2EROR
12956  037042                                  CKLOOP
12957  037042  104406                          TRAP    C$CLP1
12958
12959                                          ;READ TRDI BITS 55:48 AGAIN CHECKING THAT SETTING PDAL4 TO A ONE WITH
12960                                          ;THE "CLK" SIGNAL IN THE LOW STATE, CAUSED THE DATA (252) IN EVENT
12961                                          ;COUNTER 0 TO BE LOADED INTO EXTP 7:0 FLIP-FLOPS.
12962
12963  037044  012737  000252  002414  23$:   MOV     #252,R6LOAD             ;SETUP DATA LOADED IN EVENT COUNTER 0
12964  037052  004737  006256                  JSR     PC,READR6               ;GO READ EXTP 7:0 BITS ON TRDI 55:48
12965  037056  001405                          BEQ     24$                     ;IF LOADED OK THEN CONTINUE
```

```
12966  037060                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP ERROR OR LOGIC
12967  037060  104455                         TRAP    C$ERDF
12968  037062  000004                         .WORD   4
12969  037064  003450                         .WORD   EXTPER
12970  037066  004734                         .WORD   R026ER
12971  037070                                  CKLOOP
12972  037070  104406                         TRAP    C$CLP1
12973
12974                                          ;LOAD EVENT COUNTER 0 WITH DATA PATTERN EQUAL TO 125 AND EVENT COUNTER
12975                                          ;1 WITH DATA PATTERN EQUAL TO 1 TO SET THE SIGNAL "CLK" TO THE HIGH
12976                                          ;STATE.  WITH PDAL4 SET TO A ONE AND "CLK" SET HIGH, THE NEW DATA WILL
12977                                          ;NOT BE LOADED INTO EXTP 7:0 FLIP-FLOPS.  THE DATA IN EXTP 7:0 FLIP-
12978                                          ;FLOPS SHOULD REMAIN AS 252.
12979
12980  037072  012701  000125          24$:   MOV     #125,R1                 ;SETUP EVENT COUNTER 0 DATA PATTERN
12981  037076  012737  000031  002376        MOV     #PDAL4!PTER9,R2LOAD     ;SETUP TO SELECT EVENT COUNTER 0
12982  037104  004737  006134          25$:   JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
12983  037110  001405                         BEQ     26$                     ;IF LOADED OK THEN CONTINUE
12984  037112                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
12985  037112  104455                         TRAP    C$ERDF
12986  037114  000002                         .WORD   2
12987  037116  000000                         .WORD   0
12988  037120  004704                         .WORD   R2EROR
12989  037122                                  CKLOOP
12990  037122  104406                         TRAP    C$CLP1
12991  037124  010177  143226          26$:   MOV     R1,@REG6                ;LOAD EVENT COUNTER 0 OR 1
12992  037130  005301                         DEC     R1                      ;CHECK IF EVENT COUNTER 1 LOADED
12993  037132  001405                         BEQ     27$                     ;EXIT IF EVENT COUNTER 1 LOADED
12994  037134  005237  002376                INC     R2LOAD                  ;UPDATE POINTER TO EVENT COUNTER 1
12995  037140  012701  000001                MOV     #1,R1                   ;SETUP TO LOAD 1 INTO EVNT CNTR 1
12996  037144  000757                         BR      25$                     ;GO LOAD EVENT COUNTER 1 WITH 1
12997
12998                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
12999                                          ;READBACK OF TRDI BITS 59:48. PDAL4 WILL ALSO REMAIN SET IN CONTROL REG 2.
13000
13001  037146  012737  000024  002376  27$:   MOV     #PDAL4!PTER4,R2LOAD     ;SETUP BITS TO BE LOADED
13002  037154  004737  006134                JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
13003  037160  001405                         BEQ     28$                     ;IF LOADED OK THEN CONTINUE
13004  037162                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
13005  037162  104455                         TRAP    C$ERDF
13006  037164  000002                         .WORD   2
13007  037166  000000                         .WORD   0
13008  037170  004704                         .WORD   R2EROR
13009  037172                                  CKLOOP
13010  037172  104406                         TRAP    C$CLP1
13011
13012                                          ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE "CLK" SIGNAL TO
13013                                          ;THE HIGH STATE DID NOT LOAD THE DATA (125) IN THE EVENT COUNTERS
13014                                          ;INTO EXTP 7:0 FLIP-FLOPS.  THE EXTP 7:0 FLIP-FLOPS SHOULD CONTAIN
13015                                          ;THE PREVIOUS EVENT COUNTER DATA (252).
13016
13017  037174  004737  006256          28$:   JSR     PC,READR6               ;CHECK DATA TO EQUAL PREVIOUS DATA
13018  037200  001403                         BEQ     29$                     ;IF DATA EQUAL THEN CONTINUE
13019  037202                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP OR LOGIC ERROR
13020  037202  104455                         TRAP    C$ERDF
13021  037204  000004                         .WORD   4
```

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13022  037206  003450                          .WORD   EXTPER
13023  037210  004734                          .WORD   R026ER
13024  037212                                  CKLOOP
13025  037212  104406                          TRAP    C$CLP1
13026
13027                                          ;LOAD EVENT COUNTER 1 WITH DATA EQUAL TO 0 TO SET THE "CLK" SIGNAL
13028                                          ;TO THE LOW STATE. SETTING THE "CLK" SIGNAL TO THE LOW STATE SHOULD
13029                                          ;LOAD THE DATA (125) FROM EVENT COUNTER 0 INTO THE EXTP 7:0 FLIP-FLOPS.
13030
13031  037214  012737  000032  002376  29$:    MOV     #PDAL4!PTER10,R2LOAD    ;SETUP BITS TO BE LOADED
13032  037222  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD READ AND CHECK REGISTER 2
13033  037226  001405                          BEQ     30$                     ;IF LOADED OK THEN CONTINUE
13034  037230                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
13035  037230  104455                          TRAP    C$ERDF
13036  037232  000002                          .WORD   2
13037  037234  000000                          .WORD   0
13038  037236  004704                          .WORD   R2EROR
13039  037240                                  CKLOOP
13040  037240  104406                          TRAP    C$CLP1
13041  037242  012777  000000  143106  30$:    MOV     #0,@REG6                ;LOAD EVENT COUNTER 1 WITH 0
13042
13043                                          ;ASSERT THE SIGNAL PTER4 L IN THE POINTER REGISTER TO SETUP FOR A
13044                                          ;READBACK OF TRDI BITS 59:48
13045
13046  037250  012737  000024  002376          MOV     #PDAL4!PTER4,R2LOAD     ;SETUP BITS TO BE LOADED
13047  037256  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REGISTER 2
13048  037262  001405                          BEQ     31$                     ;IF LOADED OK THEN CONTINUE
13049  037264                                  ERRDF   2,,R2EROR               ;REGISTER 2 NOT EQUAL EXPECTED
13050  037264  104455                          TRAP    C$ERDF
13051  037266  000002                          .WORD   2
13052  037270  000000                          .WORD   0
13053  037272  004704                          .WORD   R2EROR
13054  037274                                  CKLOOP
13055  037274  104406                          TRAP    C$CLP1
13056
13057                                          ;READ TRDI BITS 55:48 AGAIN TO CHECK THAT SETTING THE SIGNAL "CLK"
13058                                          ;TO THE LOW STATE WITH PDAL4 SET TO A ONE WILL LOAD EVENT COUNTER 0
13059                                          ;DATA (125) INTO  EXTP 7:0 FLIP-FLOPS.
13060
13061  037276  012737  000125  002414  31$:    MOV     #125,R6LOAD             ;SETUP EVENT COUNTER 0 DATA LOADED
13062  037304  004737  006256                  JSR     PC,READR6               ;CHECK DATA TO EQUAL EVENT COUNTER 0
13063  037310  001404                          BEQ     32$                     ;IF DATA EQUAL THEN CONTINUE
13064  037312                                  ERRDF   4,EXTPER,R026ER         ;EXTP 7:0 FLIP-FLOP OR LOGIC ERROR
13065  037312  104455                          TRAP    C$ERDF
13066  037314  000004                          .WORD   4
13067  037316  003450                          .WORD   EXTPER
13068  037320  004734                          .WORD   R026ER
13069  037322                          32$:    ENDSEG
13070  037322                          10000$:
13071  037322  104405                          TRAP    C$ESEG
13072  037324                                  ENDTST
13073  037324                          L10172:
13074  037324  104401                          TRAP    C$ETST
```

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13075                                   .SBTTL  TEST 65: CHECK THAT INIT L CLEARS REG 0 AND REG 2
13076
13077                                   ;++
13078                                   ; THE FOLLOWING TEST WILL CHECK THAT INIT L CAN CLEAR CONTROL REGISTER 2 AND
13079                                   ; THE LOW BYTE OF CONTROL REGISTER 0.  THIS IS DONE BY LOADING ALL ONES INTO
13080                                   ; CONTROL REGISTER 2 AND THE LOW BYTE OF CONTROL REGISTER 0.  THEN A BRESET
13081                                   ; INSTRUCTION IS ISSUED WHICH SHOULD CLEAR REG 2 AND THE LOW BYTE OF REG 0.
13082                                   ;--
13083
13084  037326                                   BGNTST
13085  037326                           T65::
13086  037326  004737  005474                  JSR     PC,INITED               ;SELECT AND INITIALIZE STATE ANALYZER
13087  037332                                   BGNSEG
13088  037332  104404                           TRAP    C$BSEG
13089
13090                                           ;CHECK THAT CDAL7 H, CDAL6 H, CDAL5 H, CDAL4 H, CDAL3 H, CDAL2 H,
13091                                           ;CDAL1 H, AND CDAL0 H OF CONTROL REGISTER 0 CAN BE SET TO ONES.
13092
13093  037334  112737  000377  002370           MOVB    #377,ROLOAD             ;SETUP TO LOAD ALL ONES
13094  037342  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
13095  037346  001405                           BEQ     1$                      ;IF LOADED OK THEN CONTINUE
13096  037350                                   ERRDF   1,,ROEROR               ;CDAL7 TO CDAL0 NOT EQUAL TO 377
13097  037350  104455                           TRAP    C$ERDF
13098  037352  000001                           .WORD   1
13099  037354  000000                           .WORD   0
13100  037356  004604                           .WORD   ROEROR
13101  037360                                   CKLOOP
13102  037360  104406                           TRAP    C$CLP1
13103
13104                                           ;CHECK THAT PDAL7 H TO PDAL0 H OF CONTROL REGISTER 2 CAN BE SET TO ONES
13105
13106  037362  012737  000377  002376  1$:      MOV     #377,R2LOAD             ;SETUP BITS TO BE LOADED
13107  037370  004737  006134                  JSR     PC,LDRDR2               ;GO LOAD, READ AND CHECK REG 2
13108  037374  001405                           BEQ     2$                      ;IF ALL ONES THEN CONTINUE
13109  037376                                   ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL 377
13110  037376  104455                           TRAP    C$ERDF
13111  037400  000002                           .WORD   2
13112  037402  000000                           .WORD   0
13113  037404  004704                           .WORD   R2EROR
13114  037406                                   CKLOOP
13115  037406  104406                           TRAP    C$CLP1
13116
13117                                           ;ISSUE A BRESET INSTRUCTION. PDAL7 TO PDAL0 SHOULD THEN BE ZEROS.
13118                                           ;ALSO CDAL7 TO CDAL0 SHOULD THEN BE ZEROS.
13119
13120  037410                           2$:      BRESET                          ;CLEAR REG 2 AND THE LOW BYTE OF REG 0
13121  037410  104433                           TRAP    C$RESET
13122  037412                                   SETVEC  #4,#3$,#PRI07
13123  037412  012746  000340                  MOV     #PRI07,-(SP)
13124  037416  012746  037464                  MOV     #3$,-(SP)
13125  037422  012746  000004                  MOV     #4,-(SP)
13126  037426  012746  000003                  MOV     #3,-(SP)
13127  037432  104437                           TRAP    C$SVEC
13128  037434  062706  000010                  ADD     #10,SP
13129  037440  013705  002350                  MOV     REG0,R5                 ;SAVE ADDRESS OF REG 0
13130  037444  113765  002361  000001          MOVB    IDDEV+1,1(R5)           ;SAVE ID NUMBER
```

```
13131  037452  000240                          NOP
13132  037454                                  CLRVEC  #4                      ;RELEASE DEVICE TIMEOUT VECTOR
13133  037454  012700  000004                  MOV     #4,R0
13134  037460  104436                          TRAP    C$CVEC
13135  037462  000420                          BR      4$                      ;IF NO DEVICE TIMEOUT THEN CHECK REG 0
13136
13137                                          ;A DEVICE TIMEOUT OCCURED WHICH INDICATES THAT THERE IS NO DEVICE #0
13138                                          ;IN THE SYSTEM, THEREFORE, THE STATE ANLAYZER HAS TO BE RESELECTED BY
13139                                          ;DOING A 'MOV WORD' OPERATION.  A 'MOVB' OPERATION PERFORMED ABOVE DOES
13140                                          ;A READ/MODIFY WRITE.  THEREFORE, IF THERE IS NO DEVICE #0 IN THE SYSTEM
13141                                          ;A DEVICE TIMEOUT WILL OCCUR TO ADDRESS 4.
13142
13143  037464  005726                  3$:     TST     (SP)+                   ;CLEAR UP STACK FROM DEVICE TIMEOUT
13144  037466  005726                          TST     (SP)+                   ;
13145  037470                                  CLRVEC  #4                      ;RELEASE DEVICE TIMEOUT VECTOR
13146  037470  012700  000004                  MOV     #4,R0
13147  037474  104436                          TRAP    C$CVEC
13148  037476  105037  002370                  CLRB    R0LOAD                  ;SETUP TO LOAD ALL ZEROES IN LOW BYTE
13149  037502  004737  006102                  JSR     PC,LDRDR0               ;GO LOAD, READ AND CHECK REG 0
13150  037506  001420                          BEQ     5$                      ;IF OK THEN GO CHECK REGISTER 2
13151  037510                                  ERRDF   1,,R0EROR               ;REGISTER 0 NOT EQUAL EXPECTED
13152  037510  104455                          TRAP    C$ERDF
13153  037512  000001                          .WORD   1
13154  037514  000000                          .WORD   0
13155  037516  004604                          .WORD   R0EROR
13156  037520                                  CKLOOP
13157  037520  104406                          TRAP    C$CLP1
13158  037522  000412                          BR      5$                      ;PROCEED IF NO LOOPING INVOKED
13159
13160  037524  105037  002372          4$:     CLRB    R0GOOD                  ;CLEAR LOWER BYTE OF EXPECTED
13161  037530  004737  006116                  JSR     PC,READR0               ;GO READ AND CHECK REG 0
13162  037534  001405                          BEQ     5$                      ;IF OK THEN CONTINUE
13163  037536                                  ERRDF   1,,R0EROR               ;REG 0 NOT EQUAL EXPECTED
13164  037536  104455                          TRAP    C$ERDF
13165  037540  000001                          .WORD   1
13166  037542  000000                          .WORD   0
13167  037544  004604                          .WORD   R0EROR
13168  037546                                  CKLOOP
13169  037546  104406                          TRAP    C$CLP1
13170  037550  005037  002376          5$:     CLR     R2LOAD                  ;SETUP EXPECTED DATA
13171  037554  004737  006142                  JSR     PC,READR2               ;GO READ AND CHECK REG 2
13172  037560  001404                          BEQ     6$                      ;IF OK THEN CONTINUE
13173  037562                                  ERRDF   2,,R2EROR               ;REG 2 NOT EQUAL TO EXPECTED
13174  037562  104455                          TRAP    C$ERDF
13175  037564  000002                          .WORD   2
13176  037566  000000                          .WORD   0
13177  037570  004704                          .WORD   R2EROR
13178  037572                          6$:     ENDSEG
13179  037572                          10000$:
13180  037572  104405                          TRAP    C$ESEG
13181  037574                                  ENDTST
13182  037574                          L10173:
13183  037574  104401                          TRAP    C$ETST
13184  037576                                  ENDMOD
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13185                                   .TITLE PARAMETER CODING
13186
13187                                   .SBTTL  HARDWARE PARAMETER CODING SECTION
13188
13189  037576                                   BGNMOD
13190
13191                                   ;++
13192                                   ; THE HARDWARE PARAMETER CODING SECTION CONTAINS MACROS
13193                                   ; THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
13194                                   ; MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
13195                                   ; INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
13196                                   ; MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
13197                                   ; WITH THE OPERATOR.
13198                                   ;--
13199
13200  037576                                   BGNHRD
13201  037576  000014                           .WORD L10 74-L$HARD/2
13202  037600                          L$HARD::
13203
13204                                   ;
13205                                   ;HARDWARE P-TABLE QUESTIONS
13206                                   ;
13207                                   ;       ASK FOR CDS STATE ANALYZER CSR ADDRESS
13208                                   ;       ASK FOR CDS STATE ANALYZER DEVICE NUMBER
13209                                   ;       ASK IF CDS STATE ANALYZER EXTERNAL PROBE CONNECTED
13210                                   ;
13211
13212  037600                                   GPRMA   MSG1,0,0,0,177777,YES
13213  037600  000031                           .WORD   T$CODE
13214  037602  037630                           .WORD   MSG1
13215  037604  000000                           .WORD   T$LOLIM
13216  037606  177777                           .WORD   T$HILIM
13217  037610                                   GPRMD   MSG2,2,0,177777,0,000017,YES
13218  037610  001032                           .WORD   T$CODE
13219  037612  037644                           .WORD   MSG2
13220  037614  177777                           .WORD   177777
13221  037616  000000                           .WORD   T$LOLIM
13222  037620  000017                           .WORD   T$HILIM
13223  037622                                   GPRML   MSG3,4,177777,YES
13224  037622  002130                           .WORD   T$CODE
13225  037624  037662                           .WORD   MSG3
13226  037626  177777                           .WORD   177777
13227
13228
13229
13230  037630                                   ENDHRD
13231                                           .EVEN
13232  037630                          L10174:
```

```
13233
13234                                   ;
13235                                   ;HARDWARE P-TABLE MESSAGES
13236                                   ;
13237
13238  037630  051503  020122  042101  MSG1:   .ASCIZ  /CSR ADDRESS/
13239  037636  051104  051505  000123
13240  037644  042504  044526  042503  MSG2:   .ASCIZ  /DEVICE NUMBER/
13241  037652  047040  046525  042502
13242  037660  000122
13243  037662  054105  042524  047122  MSG3:   .ASCIZ  /EXTERNAL PROBE CONNECTED/
13244  037670  046101  050040  047522
13245  037676  042502  041440  047117
13246  037704  042516  052103  042105
13247  037712     000
13248          037714                           .EVEN
13249
13250
13251                                   .SBTTL  SOFTWARE PARAMETER CODING SECTION
13252
13253                                   ;++
13254                                   ; THE SOFTWARE PARAMETER CODING SECTION CONTAINS MACROS
13255                                   ; THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES.  THE
13256                                   ; MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE
13257                                   ; INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES.  THE
13258                                   ; MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS
13259                                   ; WITH THE OPERATOR.
13260                                   ;--
13261
13262  037714                           BGNSFT
13263  037714  000000                   .WORD L10175-L$SOFT/2
13264  037716                  L$SOFT::
13265
13266
13267                                   .EVEN
13268
13269  037716                           ENDSFT
13270                                   .EVEN
13271  037716                  L10175:
13272
13273
13274
13275  037716                  $PATCH::
13276  037716  000010                   .BLKW   10
13277
13278
13279  037736                           LASTAD
13280                                   .EVEN
13281  037736  037754                   .WORD T$FREE
13282  037740  000005                   .WORD T$SIZE
13283  037742                  L$LAST::
13284  037742                           ENDMOD
13285
13286
13287
13288
```

```
13289  037742                          BGNSETUP        1.
13290  037742                          BGNPTAB
13291  037742  000000                  .WORD   0
13292  037744  000003                  .WORD   L10200-./2-1
13293  037746                  L10176:
13294  037746  163010                  .WORD   163010
13295  037750  000001                  .WORD   1
13296  037752  000000                  .WORD   0
13297  037754                          ENDPTAB
13298  037754                  L10200:
13299  037754                          ENDSETUP
13300          000001          .END
```

```
ADR    = 000020 G   1789#
ALLREG  004750 G    2253#  10455  10484  10656  10685
ANDERR  003550 G    2067#   7509   7523   7603   7617   7705   7719   7807   7821   7908   7922   8010   8024
                    8112   8126   8214   8228   8315   8329   8417   8431   8519   8533   8621   8635   8722
                    8736   8824   8838   8926   8940   9058   9105   9198   9248   9268   9320   9433   9788
                   10141  11677  12068  12464
ANDOR   003647 G    2079#  11758  12149  12546
ASSEMB= 000010      1500
ASSERT  006376 G    2706#   6818   6837   6855   6873   6924   6989   7079   7199   7490   7584   9521   9584
                    9668   9876   9939  10023  10273  10350  10491  10552  10692  10803  10983
BIT0   = 000001 G    1762#   1838   1858
BIT00  = 000001 G    1751#   1762
BIT01  = 000002 G    1750#   1761
BIT02  = 000004 G    1749#   1760
BIT03  = 000010 G    1748#   1759
BIT04  = 000020 G    1747#   1758
BIT05  = 000040 G    1746#   1757
BIT06  = 000100 G    1745#   1756
BIT07  = 000200 G    1744#   1755
BIT08  = 000400 G    1743#   1754
BIT09  = 001000 G    1742#   1753
BIT1   = 000002 G    1761#   1836   1857
BIT10  = 002000 G    1741#   1817   4477   4584   4691   4802   4903   5043   5115   5220   5360   5432   5536
                    5676   5748   5854   5999   6073  11843
BIT11  = 004000 G    1740#   1816   3570  12234
BIT12  = 010000 G    1739#   1814   7726   7827   8133   8234   8540   8641   8947   9340  10417  10418  10497
                   10619  10648  10913  10941
BIT13  = 020000 G    1738#   1813  10447
BIT14  = 040000 G    1737#   1812  10648
BIT15  = 100000 G    1736#   1806  10447
BIT2   = 000004 G    1760#   1834   1856
BIT3   = 000010 G    1759#   1833   1855
BIT4   = 000020 G    1758#   1830   1851   7011   7140   7238   7296   7371   7433   7530   7623   7929   8030
                    8336   8437   8743   8844  11718  12506
BIT5   = 000040 G    1757#   1827   1850  12109  12506
BIT6   = 000100 G    1756#   1825   1849
BIT7   = 000200 G    1755#   1821   1848  10873
BIT8   = 000400 G    1754#   1819   7624   7725   8031   8132   8438   8539   8845   8946   9337  11843
BIT9   = 001000 G    1753#   1818  12234
BOE    = 000400 G    1793#
CDAL0  = 000001 G    1838#   2532   2542   3632   6127   6334   6347  10217  10233  11051  11061  12646  12656
CDAL1  = 000002 G    1836#
CDAL10= 002000 G     1817#
CDAL11= 004000 G     1816#
CDAL12= 010000 G     1814#
CDAL13= 020000 G     1813#
CDAL14= 040000 G     1812#
CDAL15= 100000 G     1806#   2511   2973
CDAL2  = 000004 G    1834#   4444   4551   4658   4768   4877   4929   5017   5068   5194   5246   5334   5385
                    5510   5562   5650   5701   5826   5880   5971   6024   6805
CDAL3  = 000010 G    1833#  11574  11619  11814  11965  12010  12205  12359  12405  12602  12727
CDAL4  = 000020 G    1830#  11733  12124  12521
CDAL5  = 000040 G    1827#   6486   6598
CDAL6  = 000100 G    1825#   2851   2861
CDAL7  = 000200 G    1821#   9448   9803  10157  10782  10845  10962  11766  12157  12554
CDAL8  = 000400 G    1819#
```

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CDAL9 = 001000 G    1818#  2973
C$AU  = 000052      1500#  3077
C$AUTO= 000061      1500#  3007
C$BRK = 000022      1500#
C$BSEG= 000004      1500#  2468  2510  2530  2557  2660  2708  2757  2850  3126  3143  3174  3192
                    3226   3257  3274  3306  3324  3358  3400  3466  3535  3553  3592  4253  4329
                    4406   4513  4620  4730  4837  4923  4981  5061  5154  5240  5298  5378  5470
                    5556   5614  5694  5786  5874  5934  6017  6102  6249  6480  6916  6984  7058
                    7179   7258  7317  7393  7458  7552  7646  7748  7849  7951  8053  8155  8256
                    8358   8460  8562  8663  8765  8867  9037  9083  9151  9214  9258  9284  9379
                    9442   9734  9797  10080 10148 10329 10531 10742 11044 11535 11926 12319 12720
                   13088
C$BSUB= 000002      1500#  3718  3738  3786  3806  3[illegible]  3874  3923  3943  3991  4011  4059  4079
                    4127   4147  4195  4215  4834  4919  5057  5151  5236  5374  5467  5552  5690
                    5783   5870  6013  6678  6692  6706  6720  6734  7172  7249  7308  7384  8979
                    9026   9072
C$CEFG= 000045      1500#
C$CLCK= 000062      1500#
C$CLEA= 000012      1500#  3032
C$CLOS= 000035      1500#
C$CLP1= 000006      1500#  2491  2541  2577  2675  2772  2795  2860  3414  3432  3480  3499  3628
                    3641   3655  3668  4272  4294  4342  4421  4453  4528  4560  4635  4667  4745
                    4777   4852  4886  4938  4958  4995  5026  5077  5096  5169  5203  5255  5275
                    5312   5343  5394  5413  5485  5519  5571  5591  5628  5659  5710  5729  5801
                    5835   5889  5909  5948  5980  6033  6052  6120  6136  6149  6164  6195  6263
                    6279   6292  6306  6329  6343  6356  6370  6391  6412  6428  6495  6513  6527
                    6542   6568  6593  6607  6749  6768  6794  6814  6833  6851  6869  6942  7074
                    7098   7121  7195  7213  7270  7330  7352  7405  7475  7512  7569  7606  7663
                    7687   7708  7765  7789  7810  7866  7890  7911  7968  7992  8013  8070  8094
                    8115   8172  8196  8217  8273  8297  8318  8375  8399  8420  8477  8501  8522
                    8579   8603  8624  8680  8704  8725  8782  8806  8827  8884  8908  8929  8995
                    9047   9093  9167  9188  9235  9305  9396  9417  9457  9471  9489  9508  9547
                    9571   9612  9640  9654  9751  9772  9812  9826  9844  9863  9902  9926  9967
                    9995   10009 10103 10125 10166 10180 10198 10211 10226 10242 10260 10298 10345
                   1037[illegible]  10385 10399 10427 10441 10457 10472 10486 10547 10572 10587 10601 10628
                   1064[illegible]  10658 10673 10687 10757 10771 10791 10834 10854 10866 10883 10897 10922
                   10936  10950 10971 11013 11060 11070 11084 11098 11127 11150 11167 11183 11199
                   11225  11241 11255 11269 11285 11313 11330 11344 11358 11374 11403 11421 11435
                   11449  11465 11493 11549 11564 11583 11597 11614 11628 11671 11680 11696 11711
                   11728  11742 11761 11775 11808 11823 11837 11853 11868 11889 11940 11955 11974
                   11988  12005 12019 12062 12071 12087 12102 12119 12133 12152 12166 12199 12214
                   12228  12244 12259 12280 12333 12349 12368 12382 12399 12414 12458 12467 12483
                   12498  12516 12530 12549 12563 12596 12611 12626 12642 12655 12665 12736 12759
                   12781  12797 12814 12833 12848 12863 12891 12908 12927 12941 12957 12972 12990
                   13010  13025 13040 13055 13102 13115 13157 13169
C$CVEC= 000036      1500#  2502  2588  13[illegible]4  13147
C$DCLN= 000044      1500#
C$DODU= 000051      1500#
C$DRPT= 000024      1500#
C$DU  = 000053      1500#  3054
C$EDIT= 000003      1500#  1562
C$ERDF= 000055      1500#  2486  2496  2516  2536  254[illegible]  2572  2582  2670  2689  2712  2767  2790
                    2812   2820  2828  2834  2855  28[illegible]  3134  3151  3183  3201  3230  3265  3282
                    3315   3333  3362  3409  342[illegible]  3[illegible]41  3475  3494  3509  3544  3561  3600  3611
                    3623   3636  3650  3663  3676  4267  4289  4306  4337  4355  4416  4448  4463
                    4523   4555  4570  4630  4662  4677  4740  4772  4789  4847  4881  4895  4933
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                      4953     4968     4990     5021     5055     5072     5091     5107     5164     5198     5212     5250     5270
                      5285     5307     5338     5352     5389     5408     5424     5480     5514     5528     5566     5586     5601
                      5623     5654     5668     5705     5724     5740     5796     5830     5846     5884     5904     5921     5943
                      5975     5991     6028     6047     6065     6115     6131     6144     6159     6190     6258     6274     6287
                      6301     6324     6338     6351     6365     6386     6407     6423     6444     6490     6508     6522     6537
                      6563     6588     6602     6629     6744     6763     6789     6809     6828     6846     6864     6883     6937
                      6954     7002     7069     7093     7116     7131     7190     7208     7229     7265     7287     7325     7347
                      7362     7400     7424     7470     7507     7521     7564     7601     7615     7658     7682     7703     7717
                      7760     7784     7805     7819     7861     7885     7906     7920     7963     7987     8008     8022     8065
                      8089     8110     8124     8167     8191     8212     8226     8268     8292     8313     8327     8370     8394
                      8415     8429     8472     8496     8517     8531     8574     8598     8619     8633     8675     8699     8720
                      8734     8777     8801     8822     8836     8879     8903     8924     8938     8990     9042     9056     9088
                      9103     9162     9183     9196     9230     9246     9266     9300     9318     9391     9412     9431     9452
                      9466     9484     9503     9542     9566     9607     9635     9649     9686     9746     9767     9786     9807
                      9821     9839     9858     9897     9921     9962     9990    10004    10041    10098    10120    10139    10161
                     10175    10193    10206    10221    10237    10255    10293    10340    10365    10380    10394    10422    10436
                     10452    10467    10481    10501    10542    10567    10582    10596    10623    10637    10653    10668    10682
                     10701    10752    10766    10786    10829    10849    10861    10878    10892    10917    10931    10945    10966
                     11008    11055    11065    11079    11093    11122    11145    11162    11178    11194    11220    11236    11250
                     11264    11280    11308    11325    11339    11353    11369    11398    11416    11430    11444    11460    11488
                     11506    11544    11559    11578    11592    11609    11623    11666    11675    11691    11706    11723    11737
                     11756    11770    11803    11818    11832    11848    11863    11884    11898    11935    11950    11969    11983
                     12000    12014    12057    12066    12082    12097    12114    12128    12147    12161    12194    12209    12223
                     12239    12254    12275    12289    12328    12344    12363    12377    12394    12409    12453    12462    12478
                     12493    12511    12525    12544    12558    12591    12606    12621    12637    12650    12660    12674    12731
                     12754    12776    12792    12809    12828    12843    12858    12873    12886    12903    12922    12936    12952
                     12967    12985    13005    13020    13035    13050    13065    13097    13110    13152    13164    13174
C$FRHR= 000056        1500#
C$ERRO= 000060        1500#
C$ERSF= 000054        1500#
C$ERSO= 000057        1500#
C$ESCA= 000010        1500#
C$ESEG= 000005        1500#    2505     2522     2552     2592     2595     2718     2840     2871     3140     3157     3189     3207
                      3236     3271     3288     3321     3339     3368     3447     3515     3550     3567     3682     4312     4361
                      4469     4576     4683     4795     4901     4975     5041     5113     5218     5292     5358     5430     5534
                      5608     5674     5746     5852     5928     5997     6071     6200     6450     6635     6960     7008     7137
                      7235     7293     7368     7430     7527     7621     7723     7825     7926     8028     8130     8232     8333
                      8435     8537     8639     8740     8842     8944     9062     9109     9202     9252     9272     9324     9437
                      9692     9792    10047    10145    10304    10507    10707    11018    11512    11904    12295    12681    13071
                     13180
C$ESUB= 000003        1500#    3733     3748     3801     3816     3869     3884     3938     3953     4006     4021     4074     4089
                      4142     4157     4210     4225     4907     5047     5119     5224     5364     5436     5540     5680     5752
                      5858     6003     6077     6688     6702     6716     6730     6889     7242     7300     7375     7437     9022
                      9068     9115
C$ETST= 000001        1500#    3111     3160     3210     3242     3291     3342     3374     3450     3518     3574     3685     3752
                      3820     3888     3957     4025     4093     4161     4229     4373     4481     4588     4695     4806     5122
                      5439     5755     6080     6203     6453     6639     6892     6964     7015     7145     7440     7534     7628
                      7730     7831     7933     8035     8137     8238     8340     8442     8544     8645     8747     8849     8951
                      9118     9354     9709    10064    10308    10510    10710    11022    11515    11907    12298    12684    13074
                     13183
C$EXIT= 000032        1500#    2982     3024    12717
C$GETB= 000026        1500#
C$GETW= 000027        1500#
C$GMAN= 000043        1500#
C$GPHR= 000042        1500#    2958
C$GPLO= 000030        1500#
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C$GPRI= 000040           1500#
C$INIT= 000011           1500#   2990
C$INLP= 000020           1500#
C$MANI= 000050           1500#
C$MEM = 000031           1500#
C$MSG = 000023           1500#   2200    2223    2232    2241    2250    2259    2275    2292    2303    2315
C$OPEN= 000034           1500#
C$PNTB= 000014           1500#   2270    2299    2311    2323
C$PNTF= 000017           1500#
C$PNTS= 000016           1500#
C$PNTX= 000015           1500#   2210    2219    2287    2349    2357    2367    2375    2385    2396    2407    2415
C$QIO = 000377           1500#
C$RDBU= 000007           1500#
C$REFG= 000047           1500#   2929    2934    2939    2946    2952
C$RESE= 000033           1500#   2943   13121
C$REVI= 000003           1500#   1561
C$RFLA= 000021           1500#
C$RPT = 000025           1500#   2899
C$SEFG= 000046           1500#
C$SPRI= 000041           1500#   2978
C$SVEC= 000037           1500#   2474    2563   13127
C$TPRI= 000013           1500#
DFPTBL  002330 G         1691#
DIAGMC= 000000           1500
EF.COM= 000036 G         1769#   2951
EF.NEW= 000035 G         1770#   2945
EF.PWR= 000034 G         1771#   2938
EF.RES= 000037 G         1768#   2933
EF.STA= 000040 G         1767#   2928
EMSGR0  003702 G         2092#   2191    2205
EMSGR2  003732 G         2096#   2228
EMSGR4  003762 G         2100#   2237
EMSGR6  004012 G         2104#   2246    2255    2264    2280
ERORR0  004620 G         2203#   2519
ERRBLK  002346 G         1895#
ERRMSG  002344 G         1894#
ERRNBR  002342 G         1893#
ERRTYP  002340 G         1892#
EVL   = 000004 G         1787#
EVNTCL  003254 G         2027#   9688   10043
EVNTCT  003213 G         2021#   9544    9609    9899    9964   10831   11010   11805   12196   12593
EVNTER  005024 G         2278#   9545    9610    9689    9900    9965   10044   10296   10832   11011   11806   12197   12594
EVNTRL  003321 G         2034#  10295
EXTPER  003450 G         2051#  12794   12845   12888   12938   12969   13022   13067
EXTPRB  002366 G         1909#   2975*  12714
E$END = 002100           1500#
E$LOAD= 000035           1500#   1585
FRMTEC  004360 G         2147#   2284
FRMTR0  004217 G         2129#   2354    2372    2412
FRMTR4  004253 G         2135#   2393
FRMTOR  004145 G         2121#   2216
FUSL30  003365 G         2041#  10454   10483   10655   10684
FUSL7   003601 G         2072#  10424   10503   10625   10703   10880   10919   10947
F$AU  = 000015           1500#   3065    3076
F$AUTO= 000020           1500#   3002    3006
F$BGN = 000040           1500#   1507    1720    1725    2189    2203    2226    2235    2244    2253    2262    2278    2294
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                    8978   9021   9023   9025   9063   9067   9069   9071   9110   9114   9116   9117   9119
                    9139   9203   9253   9273   9325   9353   9355   9375   9438   9693   9708   9710   9730
                    9793  10048  10063  10065  10082  10146  10305  10307  10309  10325  10508  10509  10511
                   10527  10708  10709  10711  10738  11019  11021  11023  11040  11513  11514  11516  11532
                   11905  11906  11908  11923  12296  12297  12299  12315  12682  12683  12685  12712  12717
                   13072  13073  13075  13085  13181  13182  13184  13185  13190  13233  13272  13285  13290
                   13291  13298  13300
F$HARD= 000004      1500#  13201  13231
F$HW  = 000013      1500#   1689   1699
F$INIT= 000006      1500#   2926   2989
F$JMP = 000050      1500#   2891   2982   3024   3046   3069  12717
F$MOD = 000000      1500#   1507   1720   1725   2875   2880   3080   3086  13185  13190  13285
F$MSG = 000011      1500#   2189   2199   2203   2222   2226   2231   2235   2240   2244   2249   2253   2258
                    2262   2274   2278   2291   2294   2302   2306   2314
F$PROT= 000021      1500#   2909   2916
F$PWR = 000017      1500#
F$RPT = 000012      1500#   2887   2898
F$SEG = 000003      1500#   2468   2504   2510   2521   2530   2551   2557   2591   2660   2694   2708   2717
                    2757   2839   2850   2870   3126   3139   3143   3156   3174   3188   3192   3206   3226
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                    3466   3514   3535   3549   3553   3566   3592   3681   4253   4311   4329   4360   4406
                    4468   4513   4575   4620   4682   4730   4794   4837   4900   4923   4974   4981   5040
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                    5607   5614   5673   5694   5745   5786   5851   5874   5927   5934   5996   6017   6070
                    6102   6199   6249   6449   6480   6634   6916   6959   6984   7007   7058   7136   7179
                    7234   7258   7292   7317   7367   7393   7429   7458   7526   7552   7620   7646   7722
                    7748   7824   7849   7925   7951   8027   8053   8129   8155   8231   8256   8332   8358
                    8434   8460   8536   8562   8638   8663   8739   8765   8841   8867   8943   9037   9061
                    9083   9108   9151   9201   9214   9251   9258   9271   9284   9323   9379   9436   9442
                    9691   9734   9791   9797  10046  10086  10144  10148  10303  10329  10506  10531  10706
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F$SOFT= 000005      1500#  13263  13270
F$SRV = 000010      1500#
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                    4141   4147   4156   4195   4209   4215   4224   4834   4906   4919   5046   5057   5118
                    5151   5223   5236   5363   5374   5435   5467   5539   5552   5679   5690   5751   5783
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                    9067   9072   9114
F$SW  = 000014      1500#   1711   1717
F$TEST= 000001      1500#   3104   3110   3123   3159   3171   3209   3221   3241   3254   3290   3303   3341
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                    3819   3850   3887   3919   3956   3987   4024   4055   4092   4123   4160   4191   4228
                    4245   4372   4401   4480   4508   4587   4615   4694   4725   4805   4825   5121   5142
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                    6913   6963   6975   7014   7053   7144   7168   7439   7453   7533   7547   7627   7641
                    7729   7743   7830   7844   7932   7946   8034   8048   8136   8150   8237   8251   8339
                    8353   8441   8455   8543   8557   8644   8658   8746   8760   8848   8862   8950   8973
                    9117   9140   9353   9376   9708   9731  10063  10083  10307  10326  10509  10528  10709
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G$DELM= 000372      1500#
G$DISP= 000003      1500#
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G$OFSI= 000376          1500#  13213   13218   13224
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G$PRMD= 000002          1500#  13218
G$PRML= 000000          1500#  13224
G$RADA= 000140          1500#
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G$RADO= 000020          1500#  13213   13218
G$XFER= 000004          1500#
G$YES = 000010          1500#  13213   13218   13224
HELP  = 000000          1498#   1500    1515    1603    1679    1697    1715    1720#   1723    1731    1889    1945    2087
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                        3082#   3100    3101    3106    3107   13186#  13228   13250   13266   13274   13278   13288
HOE   = 100000 G        1800#
IBE   = 010000 G        1797#
IDDEV   002360 G        1906#   2479    2531    2971*   2972*   3018   13130
IDTYPE  002364 G        1908#   2512    2973*
IDU   = 000040 G        1790#
IER   = 020000 G        1798#
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                        5142    5458    5774    6099    6246    6477    6674    6913    6975    7053    7168    7453    7547
                        7641    7743    7844    7946    8048    8150    8251    8353    8455    8557    8658    8760    8862
                        8973    9140    9376    9731   10083   10326   10528   10739   11041   11533   11924   12316   12713
                       13086
ISR   = 000100 G        1791#
IXE   = 004000 G        1796#
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I$AUTO= 000041          1500#   3002#   3008#
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I$DU  = 000041          1500#   3042#   3055#
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                  11620 11734 11767  11815 11932 11966 12011 12125 12158 12206 12325 12360 12406
                  12522 12555 12603  12647 12657 12728 13094 13149
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                  12450 12475 12618  12751 12773 12806 12825 12855 12870 12900 12919 12949 12982
                  13002 13032 13047  13107
LDRDR4  006202 G   2621#  7113  7128   7226  7359 10377 10579 10875 11191 11277 11366 11457 11720
                  12111 12508
LDRDR6  006250 G   2632#  2686  3424   3438  3491  3506  3558  3620  6298  6534  6934  6951  6999
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                  12094 12490
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LDRD4R  006210 G   2619  2622#
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LOT   = 000010 G   1788#
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LSCO    002032 G   1546#
LSDEPO  002011 G   1528#
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L10034  010152            3573#
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L10124  017545          6963#
L10125  017654          7014#
L10126  020024          7144#
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L10127  020624            7439#
L10130  020210            7241#
L10131  020326            7299#
L10132  020476            7374#
L10133  020622            7436#
L10134  020776            7533#
L10135  021152            7627#
L10136  021346            7729#
L10137  021534            7830#
L10140  021726            7932#
L10141  022122            8034#
L10142  022316            8136#
L10143  022504             137#
L10144  022676            8339#
L10145  023072            3441#
L10146  023266            8543#
L10147  023454            8644#
L10150  023646            8746#
L10151  024042            8848#
L10152  024236            8950#
L10153  024544            9117#
L10154  024334            9021#
L10155  024432            9067#
L10156  024542            9114#
L10157  025320            9353#
L10160  026240            9708#
L10161  027160           10063#
L10162  027664           10307#
L10163  030272           10509#
L10164  030664           10709#
L10165  031450           11021#
L10166  032706           11514#
L10167  034026           11905#
L10170  035146           12297#
L10171  036240           12683#
L10172  037324           12718   13073#
L10173  037574           13182#
L10174  037630           13201   13232#
L10175  037716           13263   13271#
L10176  037746           13293#
L10200  037754           13292   13298#
MSGTM0  004453 G          2157#   2296    2308
MSGTM2  004527 G          2165#
MSGTRM  004112 G          2116#   2267
MSG1    037630           13214   13238#
MSG2    037644           13219   13240#
MSG3    037662           13225   13243#
ONEFIL= 000001              1#    1498#   1501    1720#   1722    2876#   2878    3081    3082#   3084    13185   13186#  13188
ONFILE= ****** U          2876
ORADER  003161 G          2016#    6939    6956    7004    7095    7210    7267    7327    7402    10367   10569   10863   11180
                         11266   11355   11446   11708   12099   12495
ORDATA  003512 G          2062#    7118    7133    7231    7289    7349    7364    7426    10382   10584   11196   11282   11371
                         11462   11725   12116   12513
O$APTS= 000000            1500#   1544
O$AU    000000            1500#   1576
O$BGNR= 000000            1500#   1570
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O$BGNS= 000000          1500#   1536
O$DU  = 000000          1500#   1578
O$ERRT= 000000          1500#   1586
O$GNSW= 000000          1500#   1540
O$POIN= 000001          1500#   1514#   1602
O$SETU= 000001          1500#   1514#   1530   13281
PDAL0 = 000001 G        1858#   1865    1867    1869    1871    1873    1875    1877    1879
PDAL1 = 000002 G        1857#   1866    1867    1870    1871    1874    1875    1878    1879
PDAL2 = 000004 G        1856#   1868    1869    1870    1871    1876    1877    1878    1879
PDAL3 = 000010 G        1855#   1872    1873    1874    1875    1876    1877    1878    1879
PDAL4 = 000020 G        1851#  12948   12981   13001   13031   13046
PDAL5 = 000040 G        1850#  10390   10432   10463   10592   10633   10664   10888   10927   11084   11158   11216   11246
                       11304   11335   11394   11426   11484
PDAL6 = 000100 G        1849#   6111    6270    6283    6419    6504    6518    6759
PDAL7 = 000200 G        1848#   9462    9631    9645    9817    9986   10000   10189   10202
PNT   = 001000 G        1794#
PRI   = 002000 G        1795#
PRI00 = 000000 G        1783#
PRI01 = 000040 G        1782#
PRI02 = 000100 G        1781#
PRI03 = 000140 G        1780#
PRI04 = 000200 G        1779#
PRI05 = 000240 G        1778#
PRI06 = 000300 G        1777#
PRI07 = 000340 G        1555    1776#   2470    2559    2977   13123
PRNTAL  005150 G        2238    2256    2289    2330#
PRNTBS  005130 G        2190    2204    2227    2236    2245    2254    2263    2279    2319#
PRNTR0  005210 G        2192    2330    2338    2345#
PRNTR2  005262 G        2229    2331    2339    2363#
PRNTR4  005334 G        2332    2381#
PRNTR6  005422 G        2333    2340    2403#
PR026R  005172 G        2247    2272    2350
PTER0 = 000000 G        1864#   6111    6270    6504    7491    9034    9081    9145    9408    9499    9562    9631    9763
                        9854    9917    9986   10116   10251   11075   11089   11216   11304   11394   11484   11660   12051
                       12447
PTER1   000001 G        1865#   4248    4324    4949    5087    6819    7585
PTER10  000012 G        1874#   8492   12250   12761   12854   13031
PTER11= 000013 G        1875#   8594   11870
PTER12= 000014 G        1876#   8695   12261
PTER13= 000015 G        1877#   8797    9493    9848   10184   10774   11567   11958   12352
PTER14= 000016 G        1878#   8899
PTER15- 000017 G        1879#   6925    6990    7080    7200    9064    9111    9522    9585    9669    9877    9940   10024
                       10274   10351   10492   10553   10693   10804   10984   11158   11246   11335   11426   11683   12074
                       12470
PTER2 = 000002 G        1866#   5266    5404    6838    7678
PTER3 = 000003 G        1867#   5582    5720    6856    7780
PTER4 = 000004 G        1868#   5900    6043    6874    7881   10432   10633   11588   11828   11880   11979   12219   12271
                       12373   12617   12772   12824   12869   12918   13001   13046
PTER5 = 000005 G        1869#   2809    3730    3745    3798    3813    4247    4432    4866    5004    6685    7482    7576
                        7670    7772    7983    9001    9144    9174    9221    9291    9403    9758   10110   11639   12030
                       12426
PTER6 = 000006 G        1870#   2817    3866    3881    3935    3950    4539    5183    5321    6699    7873    7975    8077
                        8085    8179    9007   11644   12035   12431
PTER7 = 000007 G        1871#   2825    4003    4018    4071    4086    4646    5499    5637    6713    8187    8280    8382
                        8484    8586    9013   11649   12040   12436
PTER8 = 000010 G        1872#   2804    4139    4154    4207    4222    4756    5815    5958    6727    8288    8687    8789
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                        8891    9019    9335   11654   12045   12441
PTER9 = 000011 G        1873#   8390    9480    9835   10171   10762   11555   11859   11946   12340   12750   12805   12899
                       12981
READR0  006116 G        2601#  13161
READR2  006142 G        2609#  13171
READR4  006216 G        2623#   7284    7344    7421    9100    9243    9315   10419   10498   10620   10698   10914   10942
                       11753   12144   12541
READR6  006256 G        2633#   3647    3673    6156    6187    6321    6362    6383    6404    6441    6560    6585    6626
                        6786    6825    6843    6861    6880   10449   10478   10650   10679   10826   11005   11119   11142
                       11233   11322   11413   11503   11606   11800   11845   11895   11997   12191   12236   12286   12391
                       12588   12634   12671   12789   12840   12883   12933   12964   13017   13062
REG0    002350 G        1901#   2481*   2482    2600*   2601    2962    3018*  13129
REG0EQ  004042 G        2108#   2207    2346
REG2    002352 G        1902#   2566*   2567    2608*   2609    3020*
REG2EQ  004054 G        2110#   2364
REG4    002354 G        1903#   2622*   2623
REG4EQ  004066 G        2112#   2382
REG6    002356 G        1904#   2632*   2633    2780*   2803    4280*   4301    4350    4437*   4457    4544*   4564    4651*
                        4671    4761*   4781    4871*   4891    4964    5010*   5031    5103    5188*   5208    5281    5327*
                        5348    5420    5504*   5524    5597    5643*   5664    5736    5820*   5840    5915    5964*   5985
                        6060    9491*   9537    9602    9681    9846*   9892    9957   10036   10181*  10288   10772*  11565*
                       11869*  11956*  12260*  12350*  12760*  12815*  12864*  12909*  12991*  13041*
REG6EQ  004100 G        2114#   2404
ROEROR  004604 G        2189#   2489    2539    2858    2868    3137    3154    3186    3204    3233    3603    3639    3666
                        4419    4451    4526    4558    4633    4665    4743    4775    4850    4884    4936    4993    5024
                        5075    5167    5201    5253    5310    5341    5392    5483    5517    5569    5626    5657    5708
                        5799    5833    5887    5946    5978    6031    6134    6147    6261    6341    6354    6493    6605
                        6747    6812    7072    7193    7473    7567    7661    7763    7864    7966    8068    8170    8271
                        8373    8475    8577    8678    8780    8882    8993    9165    9394    9455    9749    9810   10101
                       10164   10224   10240   10343   10545   10755   10789   10852   10969   11058   11068   11547   11581
                       11626   11740   11773   11821   11938   11972   12017   12131   12164   12212   12331   12366   12412
                       12528   12561   12609   12653   12663   12734   13100   13155   13167
ROGOOD  002372 G        1912#   2213    2480*   2483    2512*   2599*   2602   13160*
ROLOAD  002370 G        1911#   2215    2353    2479*   2480    2481    2511*   2531*   2532*   2542*   2549    2599    2600
                        2851*   2861*   3130*   3147*   3179*   3197*   3223*   3238*   3596*   3632*   3659*   4412*   4444*
                        4519*   4551*   4626*   4658*   4736*   4768*   4843*   4877*   4929*   4986*   5017*   5068*   5160*
                        5194*   5246*   5303*   5334*   5385*   5476*   5510*   5562*   5619*   5650*   5701*   5792*   5826*
                        5880*   5939*   5971*   6024*   6127*   6140*   6254*   6334*   6347*   6486*   6598*   6710*   6805*
                        7065*   7186*   7466*   7560*   7654*   7756*   7857*   7959*   8061*   8163*   8264*   8366*   8468*
                        8570*   8671*   8773*   8875*   8986*   9158*   9387*   9448*   9742*   9803*  10094*  10157*  10217*
                       10233*  10336*  10538*  10748*  10782*  10845*  10962*  11051*  11061*  11540*  11574*  11619*  11733*
                       11766*  11814*  11931*  11965*  12010*  12124*  12157*  12205*  12324*  12359*  12405*  12521*  12554*
                       12602*  12646*  12656*  12727*  13093*  13148*
ROREAD  002374 G        1913#   2214    2352    2482*   2483    2601*   2602
ROTM    005064 G        2294#   2499
RO26ER  004734 G        2244#   2692    2815    2823    2831    2837    3430    3444    3497    3512    3564    3626    3653
                        3679    4309    4358    6162    6193    6304    6327    6368    6389    6410    6447    6540    6566
                        6591    6632    6792    6940    6957    7005    7096    7211    7268    7328    7403   10368   10570
                       10864   11125   11148   11181   11239   11267   11328   11356   11419   11447   11509   11612   11709
                       11851   11901   12003   12100   12242   12292   12397   12496   12640   12677   12795   12846   12889
                       12939   12970   13023   13068
R2EROR  004704 G        2226#   2575    2673    2715    2770    2793    3268    3285    3318    3336    3365    3412    3478
                        3547    3614    4270    4292    4340    4956    5094    5273    5411    5589    5727    5907    6050
                        6118    6277    6290    6426    6511    6525    6766    7685    7787    7888    7990    8092    8194
                        8295    8397    8499    8601    8702    8804    8906    9045    9091    9186    9233    9303    9415
                        9469    9487    9506    9569    9638    9652    9770    9824    9842    9861    9924    9993   10007
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                    10123   10178   10196   10209   10258   10397   10439   10470   10599   10640   10671   10769   10895
                    10934   11082   11096   11165   11223   11253   11311   11342   11401   11433   11491   11562   11595
                    11669   11694   11835   11866   11887   11953   11986   12060   12085   12226   12257   12278   12347
                    12380   12456   12481   12624   12757   12779   12812   12831   12861   12876   12906   12925   12955
                    12988   13008   13038   13053   13113   13177
R2LOAD  002376 G     1915#   2371    2565*   2566    2569    2608    2611    2666*   2706*   2763*   2786*   3261*   3278*
                     3311*   3329*   3355*   3370*   3405*   3471*   3540*   3607*   4263*   4285*   4333*   4949*   5087*
                     5266*   5404*   5582*   5720*   5900*   6043*   6111*   6270*   6283*   6419*   6504*   6518*   6759*
                     7678*   7780*   7881*   7983*   8085*   8187*   8288*   8390*   8492*   8594*   8695*   8797*   8899*
                     9034*   9052    9063*   9064    9081*   9097    9110*   9111    9179*   9226*   9296*   9408*   9462*
                     9480*   9492*   9493    9499*   9562*   9631*   9645*   9763*   9817*   9835*   9847*   9848    9854*
                     9917*   9986*   10000*  10116*  10171*  10183*  10184   10189*  10202*  10251*  10390*  10432*  10463*
                    10592*  10633*  10664*  10762*  10773*  10774   10888*  10927*  11075*  11089*  11158*  11216*  11246*
                    11304*  11335*  11394*  11426*  11484*  11555*  11566*  11567   11588*  11660*  11682*  11683   11828*
                    11859*  11870   11872*  11880*  11946*  11957*  11958   11979*  12051*  12073*  12074   12219*  12250*
                    12261   12263*  12271*  12340*  12351*  12352   12373*  12447*  12469*  12470   12617*  12750*  12761*
                    12772*  12805*  12817*  12824*  12854*  12869*  12899*  12911*  12918*  12948*  12981*  12994*  13001*
                    13031*  13046*  13106*  13170*
R2READ  002400 G     1916#   2370    2567*   2568*   2569    2609*   2610*   2611
R2TM    005106 G     2306#   2585
R4BAD   002412 G     1922#   2388    2624*   2625*   2626
R4EROR  004720 G     2235#   7119    7134    7232    7290    7350    7365    7427    7510    7524    7604    7618    7706
                     7720    7808    7822    7909    7923    8011    8025    8113    8127    8215    8229    8316    8330
                     8418    8432    8520    8534    8622    8636    8723    8737    8825    8839    8927    8941    9059
                     9106    9199    9249    9269    9321    9434    9789   10142   10383   10425   10504   10585   10626
                    10704   10881   10920   10948   11197   11283   11372   11463   11678   11726   11759   12069   12117
                    12150   12465   12514   12547
R4GOOD  002404 G     1919#   2389    2617*   2618*   2621*   2626    7283*   7343*   7420*   9098*   9099*   9241*   9242*
                     9313*   9314*  10418*  10497*  10913*  10941*  11751*  12142*  12539*
R4LOAD  002402 G     1918#   2392    2617    2621    2622    7111*   7127*   7225*   7282*   7342*   7357*   7358*   7419*
                     7503*   7517*   7597*   7611*   7699*   7713*   7801*   7815*   7902*   7916*   8004*   8018*   8106*
                     8120*   8208*   8222*   8309*   8323*   8411*   8425*   8513*   8527*   8615*   8629*   8716*   8730*
                     8818*   8832*   8920*   8934*   9052*   9097*   9098    9192*   9240*   9241    9254*   9255*   9310*
                     9311*   9312*   9313    9426*   9781*  10134*  10375*  10577*  10873*  11189*  11275*  11364*  11455*
                    11661*  11681*  11718*  12052*  12072*  12109*  12448*  12468*  12506*
R4MASK  002406 G     1920#   2390    2625    7112*   7176*   7455*   7549*   7643*   7745*   7846*   7948*   8050*   8152*
                     8253*   8355*   8457*   8559*   8660*   8762*   8864*   8975*   9142*   9427*   9782*  10135*  10376*
                    10417*  10578*  10619*  10874*  11190*  11276*  11365*  11456*  11662*  11719*  11752*  12053*  12110*
                    12143*  12449*  12507*  12540*
R4READ  002410 G     1921#   2391    2623*   2624
R6BAD   002422 G     1927#   2634*
R6LOAD  002414 G     1924#   2411    2632    2636    2684*   2780    2807    3422*   3437*   3489*   3505*   3531*   3569*
                     3570    3618*   3646*   3728*   3743*   3796*   3811*   3864*   3879*   3933*   3948*   4001*   4016*
                     4069*   4084*   4137*   4152*   4205*   4220*   4279*   4303    4349*   4352    4430*   4458    4537*
                     4565    4644*   4672    4754*   4783*   4784    4864*   4892    4963*   4965    5001*   5002*   5032
                     5101*   5102*   5104    5181*   5209    5280*   5282    5318*   5319*   5349    5418*   5419*   5421
                     5497*   5525    5596*   5598    5634*   5635*   5665    5734*   5735*   5737    5813*   5842*   5843
                     5914*   5916*   5918    5954*   5955*   5956*   5987*   5988    6057*   6058*   6059*   6062    6154*
                     6185*   6186*   6196    6296*   6320*   6361*   6440*   6532*   6559*   6625*   6683*   6697*   6711*
                     6725*   6785*   6823*   6842*   6860*   6878*   6932*   6950*   6977*   7010*   7011    7054*   7139*
                     7140    7174*   7219    7224    7237*   7238    7255*   7276    7281    7295*   7296    7314*   7336
                     7341    7370*   7371    7390*   7411    7416    7432*   7433    7454*   7529*   7530    7548*   7623*
                     7624    7642*   7725*   7726    7744*   7827*   7845*   7928*   7929    7947*   8030*   8031    8049*
                     8132*   8133    8151*   8234*   8252*   8335*   8336    8354*   8437*   8438    8456*   8539*   8540
                     8558*   8641*   8659*   8742*   8743    8761*   8844*   8845    8863*   8946*   8947    8974*   9148*
                     9204*   9211*   9274*   9281*   9326*   9333*   9401*   9531*   9534*   9539    9595*   9596*   9604
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                    9679*  9683   9756*  9886*  9889*  9894   9950*  9953*  9959   10034* 10038  10108* 10283*
                   10286* 10290  10360* 10447* 10477* 10562* 10648* 10678* 10822* 11000* 11004* 11117* 11140*
                   11173* 11231* 11259* 11320* 11348* 11411* 11439* 11501* 11604* 11633* 11701* 11798* 11843*
                   11894* 11995* 12024* 12092* 12189* 12234* 12285* 12389* 12420* 12488* 12586* 12632* 12670*
                   12787* 12882* 12963* 13061*
R6MASK  002416 G    1925#  2589*  2635   2685*  3423*  3490*  3532*  3619*  4250*  4302   4319*  4326*  4351
                    4367*  6155*  6297*  6533*  6824*  6879*  6933*  6976*  7055*  7175*  10361* 10448* 10563*
                   10649* 10825* 11001* 11118* 11141* 11174* 11232* 11260* 11321* 11349* 11412* 11440* 11502*
                   11605* 11634* 11702* 11799* 11844* 11996* 12025* 12093* 12190* 12235* 12390* 12421* 12489*
                   12587* 12633* 12788*
R6READ  002420 G    1926#  2410   2633* 2634   2635*  2636   2803*  2806*  2807   4301*  4302*  4303   4350*
                    4351*  4352   4457* 4458   4564*  4565   4671*  4672   4781*  4782*  4784   4891*  4892
                    4964*  4965   5031* 5032   5103*  5104   5208*  5209   5281*  5282   5348*  5349   5420*
                    5421   5524*  5525  5597*  5598   5664*  5665   5736*  5737   5840*  5841*  5843   5915*
                    5917*  5918   5985* 5986*  5988   6060*  6061*  6062   9537*  9538*  9539   9602*  9603*
                    9604   9681*  9682* 9683   9892*  9893*  9894   9957*  9958*  9959   10036* 10037* 10038
                   10288* 10289* 10290
SBLERR  003416 G    2046#  11611  11850  11900  12002  12241  12291  12396  12639  12676
SFPTBL  002340 G    1713#
SVCGBL= 000000      1500#  1517   1518   1526   1527   1528   1529   1530   1531   1532   1533   1534   1535
                    1536   1537   1538   1539   1540   1541   1542   1543   1544   1545   1546   1547   1548
                    1549   1550   1551   1552   1553   1554   1555   1556   1557   1558   1559   1560   1561
                    1563   1564   1566   1567   1568   1569   1570   1571   1572   1573   1574   1575   1576
                    1577   1578   1579   1580   1581   1582   1583   1584   1585   1586   1587   1588   1589
                    1590   1591   1592   1593   1594   1595   1596   1597   1598   1599   1600   1601   1612
                    1613   1690   1691   1692   1712   1713   1714   1891   1892   1940   1941   1949   1950
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                    3624#  3637#  3651#  3664#  3677#  4268#  4290#  4307#  4338#  4356#  4417#  4449#  4464#
                    4524#  4556#  4571#  4631#  4663#  4678#  4741#  4773#  4790#  4848#  4882#  4896#  4934#
                    4954#  4969#  4991#  5022#  5036#  5073#  5092#  5108#  5165#  5199#  5213#  5251#  5271#
                    5286#  5308#  5339#  5353#  5390#  5409#  5425#  5481#  5515#  5529#  5567#  5587#  5602#
                    5624#  5655#  5669#  5706#  5725#  5741#  5797#  5831#  5847#  5885#  5904#  5922#  5944#
                    5976#  5992#  6029#  6048#  6066#  6116#  6132#  6145#  6160#  6191#  6259#  6275#  6288#
                    6302#  6325#  6339#  6352#  6366#  6387#  6408#  6424#  6445#  6491#  6509#  6523#  6538#
                    6564#  6589#  6603#  6630#  6745#  6764#  6790#  6810#  6829#  6847#  6865#  6884#  6938#
                    6955#  7003#  7070#  7094#  7117#  7132#  7191#  7209#  7230#  7266#  7288#  7326#  7348#
                    7363#  7401#  7425#  7471#  7508#  7522#  7565#  7602#  7616#  7659#  7683#  7704#  7718#
                    7761#  7785#  7806#  7820#  7862#  7886#  7907#  7921#  7964#  7988#  8009#  8023#  8066#
                    8090#  8111#  8125#  8168#  8192#  8213#  8227#  8269#  8293#  8314#  8328#  8371#  8395#
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                    8735#  8778#  8802#  8823#  8837#  8880#  8904#  8925#  8939#  8991#  9043#  9057#  9089#
                    9104#  9163#  9184#  9197#  9231#  9247#  9267#  9301#  9319#  9392#  9413#  9432#  9453#
                    9467#  9485#  9504#  9543#  9567#  9608#  9636#  9650#  9687#  9747#  9768#  9787#  9808#
                    9822#  9840#  9859#  9898#  9922#  9963#  9991#  10005#  10042#  10099#  10121#  10140#  10162#
                   10176#  10194#  10207#  10222#  10238#  10256#  10294#  10341#  10366#  10381#  10395#  10423#  10437#
```

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                    10453#  10468#  10482#  10502#  10543#  10568#  10583#  10597#  10624#  10638#  10654#  10669#  10683#
                    10702#  10753#  10767#  10787#  10830#  10850#  10862#  10879#  10893#  10918#  10932#  10946#  10967#
                    11009#  11056#  11066#  11080#  11094#  11123#  11146#  11163#  11179#  11195#  11221#  11237#  11251#
                    11265#  11281#  11309#  11326#  11340#  11354#  11370#  11399#  11417#  11431#  11445#  11461#  11489#
                    11507#  11545#  11560#  11579#  11593#  11610#  11624#  11667#  11676#  11692#  11707#  11724#  11738#
                    11757#  11771#  11804#  11819#  11833#  11849#  11864#  11885#  11899#  11936#  11951#  11970#  11984#
                    12001#  12015#  12058#  12067#  12083#  12098#  12115#  12129#  12148#  12162#  12195#  12210#  12224#
                    12240#  12255#  12276#  12290#  12329#  12345#  12364#  12378#  12395#  12410#  12454#  12463#  12479#
                    12494#  12512#  12526#  12545#  12559#  12592#  12607#  12622#  12638#  12651#  12661#  12675#  12732#
                    12755#  12777#  12793#  12810#  12829#  12844#  12859#  12874#  12887#  12904#  12923#  12937#  12953#
                    12968#  12986#  13006#  13021#  13036#  13051#  13066#  13098#  13111#  13153#  13165#  13175#
T$EXCP= 000000      13213#  13217   13218#  13223
T$FLAG= 000040       2891#   2893    2982#   3024#   3046#   3048    3069#   3071   12717#
T$FREE= 037754      13281   13300#
T$GMAN= 000000       1500#
T$HILI= 000017      13213#  13216   13218#  13222
T$LAST= 000001       1500#  13281#  13290
T$LOLI= 000000      13213#  13215   13218#  13221
T$LSYM= 010000       1500#   1700    1718    2200    2223    2232    2241    2250    2259    2275    2292    2303    2315
                     2899    2990    3007    3032    3054    3077    3111    3160    3210    3242    3291    3342    3374
                     3450    3518    3574    3685    3733    3748    3752    3801    3816    3820    3869    3884    3888
                     3938    3953    3957    4006    4021    4025    4074    4089    4093    4142    4157    4161    4210
                     4225    4229    4373    4481    4588    4695    4806    4907    5047    5119    5122    5224    5364
                     5436    5439    5540    5680    5752    5755    5858    6003    6077    6080    6203    6415    6639
                     6688    6702    6716    6730    6889    6892    6964    7015    7145    7242    7300    7375    7437
                     7440    7534    7628    7730    7831    7933    8035    8137    8238    8340    8442    8544    8645
                     8747    8849    8951    9022    9068    9115    9118    9354    9709   10064   10308   10510   10710
                    11022   11515   11907   12298   12684   13074   13183   13233   13272
T$LTNO= 000101      13284#
T$NEST= 177777       1500#   1507#   1689#   1699#   1711#   1717#   1720#   1725#   2189#   2199#   2203#   2222#   2226#
                     2231#   2235#   2240#   2244#   2249#   2253#   2258#   2262#   2274#   2278#   2291#   2294#   2302#
                     2306#   2314#   2468#   2504#   2510#   2521#   2530#   2551#   2557#   2591#   2660#   2694#   2708#
                     2717#   2757#   2839#   2850#   2870#   2875#   2880#   2887#   2898#   2909#   2916#   2926#   2989#
                     3002#   3006#   3017#   3031#   3042#   3053#   3065#   3076#   3080#   3086#   3104#   3110#   3123#
                     3126#   3139#   3143#   3156#   3159#   3171#   3174#   3188#   3192#   3206#   3209#   3221#   3226#
                     3235#   3241#   3254#   3257#   3270#   3274#   3287#   3290#   3303#   3306#   3320#   3324#   3338#
                     3341#   3354#   3358#   3367#   3373#   3397#   3400#   3446#   3449#   3463#   3466#   3514#   3517#
                     3530#   3535#   3549#   3553#   3566#   3573#   3590#   3592#   3681#   3684#   3714#   3718#   3732#
                     3738#   3747#   3751#   3782#   3786#   3800#   3806#   3815#   3819#   3850#   3854#   3868#   3874#
                     3883#   3887#   3919#   3923#   3937#   3943#   3952#   3956#   3987#   3991#   4005#   4011#   4020#
                     4024#   4055#   4059#   4073#   4079#   4088#   4092#   4123#   41[illegible]#   4141#   4147#   4156#   4160#
                     4191#   4195#   4209#   4215#   4224#   4228#   4245#   4253#   4311#   4329#   4360#   4372#   4401#
                     4406#   4468#   4480#   4508#   4513#   4575#   4587#   4615#   4620#   4682#   4694#   4725#   4730#
                     4794#   4805#   4825#   4834#   4837#   4900#   4906#   4919#   4923#   4974#   4981#   5040#   5046#
                     5057#   5061#   5112#   5118#   5121#   5142#   5151#   5154#   5217#   5223#   5236#   5240#   5291#
                     5298#   5357#   5363#   5374#   5378#   5429#   5435#   5438#   5458#   5467#   5470#   5533#   5539#
                     5552#   5556#   5607#   5614#   5673#   5679#   5690#   5694#   5745#   5751#   5754#   5774#   5783#
                     5786#   5851#   5857#   5870#   5874#   5927#   5934#   5996#   6002#   6013#   6017#   6070#   6076#
                     6079#   6098#   6102#   6199#   6202#   6246#   6249#   6449#   6452#   6476#   6480#   6634#   6638#
                     6674#   6678#   6687#   6692#   6701#   6706#   6715#   6720#   6729#   6734#   6888#   6891#   6913#
                     6916#   6959#   6963#   6975#   6984#   7007#   7014#   7053#   7058#   7136#   7144#   7168#   7172#
                     7179#   7234#   7241#   7249#   7258#   7292#   7299#   7308#   7317#   7367#   7374#   7384#   7393#
                     7429#   7436#   7439#   7453#   7458#   7526#   7533#   7547#   7552#   7620#   7627#   7641#   7646#
                     7722#   7729#   7743#   7748#   7824#   7830#   7844#   7849#   7925#   7932#   7946#   7951#   8027#
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                     8353#   8358#   8434#   8441#   8455#   8460#   8536#   8543#   8557#   8562#   8638#   8644#   8658#
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                    8663#  8739#  8746#  8760#  8765#  8841#  8848#  8862#  8867#  8943#  8950#  8973#  8979#
                    9021#  9026#  9037#  9061#  9067#  9072#  9083#  9108#  9114#  9117#  9140#  9151#  9201#
                    9214#  9251#  9258#  9271#  9284#  9323#  9353#  9376#  9379#  9436#  9442#  9691#  9708#
                    9731#  9734#  9791#  9797#  10046#  10063#  10083#  10086#  10144#  10148#  10303#  10307#  10326#
                   10329#  10506#  10509#  10528#  10531#  10706#  10709#  10739#  10742#  11017#  11021#  11041#  11044#
                   11511#  11514#  11533#  11535#  11903#  11906#  11924#  11926#  12294#  12297#  12316#  12319#  12680#
                   12683#  12713#  12720#  13070#  13073#  13086#  13088#  13179#  13182#  13185#  13190#  13201#  13231#
                   13263#  13270#  13285#
T$NS0 = 000000      1507#  1720    1725#  2875    2880#  3080    3086#  13185   13190#  13285
T$NS1 = 000005      1689#  1699    1711#  1717    2189#  2199    2203#  2222    2226#  2231    2235#  2240    2244#
                    2249   2253#   2258   2262#   2274   2278#   2291   2294#   2302   2306#   2314   2468#   2504
                    2510#  2521    2530#  2551    2557#  2591    2660#  2694    2708#  2717    2757#  2839    2850#
                    2870   2887#   2898   2909#   2916   2926#   2989   3002#   3006   3017#   3031   3042#   3053
                    3065#  3076    3104#  3110    3123#  3159    3171#  3209    3221#  3241    3254#  3290    3303#
                    3341   3354#   3373   3397#   3449   3463#   3517   3530#   3573   3590#   3684   3714#   3751
                    3782#  3819    3850#  3887    3919#  3956    3987#  4024    4055#  4092    4123#  4160    4191#
                    4228   4245#   4372   4401#   4480   4508#   4587   4615#   4694   4725#   4805   4825#   5121
                    5142#  5438    5458#  5754    5774#  6079    6098#  6202    6246#  6452    6476#  6638    6674#
                    6891   6913#   6963   6975#   7014   7053#   7144   7168#   7439   7453#   7533   7547#   7627
                    7641#  7729    7743#  7830    784    7932    7946#  8034    8048#  8136    8150#  8237    8251#
                    8339   8353#   8441   8455#   85     8557#   8644   8658#   8746   8760#   8848   8862#   8950
                    8973#  9117    9140#  9353    93 6#  9708    9731#  10063   10083#  10307   10326#  10509   10520#
                   10709   10739#  11021  11041#  11514  11533#  11906  11924#  12297   12316#  12683   12713#  13073
                   13086#  13182   13201#  13231   13263#  13270
T$NS2 = 000003      3126#  3139    3143#  3156    3174#  3188    3192#  3206    3226#  3235    3257#  3270    3274#
                    3287   3306#   3320   3324#   3338   3358#   3367   3400#   3446   3466#   3514   3535#   3549
                    3553#  3566    3592#  3681    3718#  3732    3738#  3747    3786#  3800    3806#  3815    3854#
                    3868   3874#   3883   3923#   3937   3943#   3952   3991#   4005   4011#   4020   4059#   4073
                    4079#  4088    4127#  4141    4147#  4156    4195#  4209    4215#  4224    4253#  4311    4329#
                    4360   4406#   4468   4513#   4575   4620#   4682   4730#   4794   4834#   4906   4919#   5046
                    5057#  5118    5151#  5223    5236#  5363    5374#  5435    5467#  5539    5552#  5679    5690#
                    5751   5783#   5857   5870#   6002   6013#   6076   6102#   6199   6249#   6449   6480#   6634
                    6678#  6687    6692#  6701    6706#  6715    6720#  6729    6734#  6888    6916#  6959    6984#
                    7007   7058#   7136   7172#   7241   7249#   7299   7308#   7374   7384#   7436   7458#   7526
                    7552#  7620    7646#  7722    7748#  7824    7849#  7925    7951#  8027    8053#  8129    8155#
                    8231   8256#   8332   8358#   8434   8460#   8536   8562#   8638   8663#   8739   8765#   8841
                    8867#  8943    8979#  9021    9026#  9067    9072#  9114    9151#  9201    9214#  9251    9258#
                    9271   9284#   9323   9379#   9436   9442#   9691   9734#   9791   9797#   10046  10086#  10144
                   10148#  10303   10329#  10506   10531#  10706   10742#  11017   11044#  11511   11535#  11903   11926#
                   12294   12319#  12680   12720#  13070   13088#  13179
T$NS3 = 000003      4837#  4900    4923#  4974    4981#  5040    5061#  5112    5154#  5217    5240#  5291    5298#
                    5357   5378#   5429   5470#   5533   5556#   5607   5614#   5673   5694#   5745   5786#   5851
                    5874#  5927    5934#  5996    6017#  6070    7179#  7234    7258#  7292    7317#  7367    7393#
                    7429   9037#   9061   9083#   9108
T$PCNT= 000000     13290#  13291#
T$PTAB= 010177     13291#  13294
T$PTHV= 000001      1531   13300#
T$PTNU= 000001      1500#  13294#  13300
T$SAVL= 177777      1500#
T$SEGL= 177777      1500#  2468#  2504#  2506    2510#  2521#  2523    2530#  2551#  2553    2557#  2591#  2593
                    2660#  2694#  2696   2708#   2717#  2719   2757#  2839#  2841   2850#  2870#  2872   3126#
                    3139#  3141   3143#  3156#   3158   3174#  3188#  3190   3192#  3206#  3208   3226#  3235#
                    3237   3257#  3270#  3272    3274#  3287#  3289   3306#  3320#  3322   3324#  3338#  3340
                    3358#  3367#  3369   3400#   3446#  3448   3466#  3514#  3516   3535#  3549#  3551   3553#
                    3566#  3568   3592#  3681#   3683   4253#  4311#  4313   4329#  4350#  4362   4406#  4468#
                    4470   4513#  4575#  4577    4620#  4682#  4684   4730#  4794#  4796   4837#  4900#  4902
```

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                    4923#  4974#  4976   4981#  5040#  5042   5061#  5112#  5114   5154#  5217#  5219   5240#
                    5291#  5293   5298#  5357#  5359   5378#  5429#  5431   5470#  5533#  5535   5556#  5607#
                    5609   5614#  5673#  5675   5694#  5745#  5747   5786#  5851#  5853   5874#  5927#  5929
                    5934#  5996#  5998   6017#  6070#  6072   6102#  6199#  6201   6249#  6449#  6451   6480#
                    6634#  6636   6916#  6959#  6961   6984#  7007#  7009   7058#  7136#  7138   7179#  7234#
                    7236   7258#  7292#  7294   7317#  7367#  7369   7393#  7429#  7431   7458#  7526#  7528
                    7552#  7620#  7622   7646#  7722#  7724   7748#  7824#  7826   7849#  7925#  7927   7951#
                    8027#  8029   8053#  8129#  8131   8155#  8231#  8233   8256#  8332#  8334   8358#  8434#
                    8436   8460#  8536#  8538   8562#  8638#  8640   8663#  8739#  8741   8765#  8841#  8843
                    8867#  8943#  8945   9037#  9061#  9063   9083#  9108#  9110   9151#  9201#  9203   9214#
                    9251#  9253   9258#  9271#  9273   9284#  9323#  9325   9379#  9436#  9438   9442#  9691#
                    9693   9734#  9791#  9793   9797#  10046#  10048  10086#  10144#  10146  10148#  10303#  10305
                    10329#  10506#  10508  10531#  10706#  10708  10742#  11017#  11019  11044#  11511#  11513  11535#
                    11903#  11905  11926#  12294#  12296  12319#  12680#  12682  12720#  13070#  13072  13088#  13179#
                    13181
T$SEK0= 010000      2468#  2504   2510#  2521   2530#  2551   2557#  2591   2660#  2694   2708#  2717   2757#
                    2839   2850#  2870   3126#  3139   3143#  3156   3174#  3188   3192#  3206   3226#  3235
                    3257#  3270   3274#  3287   3306#  3320   3324#  3338   3358#  3367   3400#  3446   3466#
                    3514   3535#  3549   3553#  3566   3592#  3681   4253#  4311   4329#  4360   4406#  4468
                    4513#  4575   4620#  4682   4730#  4794   4837#  4900   4923#  4974   4981#  5040   5061#
                    5112   5154#  5217   5240#  5291   5298#  5357   5378#  5429   5470#  5533   5556#  5607
                    5614#  5673   5694#  5745   5786#  5851   5874#  5927   5934#  5996   6017#  6070   6102#
                    6199   6249#  6449   6480#  6634   6916#  6959   6984#  7007   7058#  7136   7179#  7234
                    7258#  7292   7317#  7367   7393#  7429   7458#  7526   7552#  7620   7646#  7722   7748#
                    7824   7849#  7925   7951#  8027   8053#  8129   8155#  8231   8256#  8332   8358#  8434
                    8460#  8536   8562#  8638   8663#  8739   8765#  8841   8867#  8943   9037#  9061   9083#
                    9108   9151#  9201   9214#  9251   9258#  9271   9284#  9323   9379#  9436   9442#  9691
                    9734#  9791   9797#  10046  10086#  10144  10148#  10303  10329#  10506  10531#  10706  10742#
                    11017  11044#  11511  11535#  11903  11926#  12294  12319#  12680  12720#  13070  13088#  13179
T$SIZE= 000005      13282  13300#
T$SUBN= 000000      1500#  3103#  3122#  3170#  3220#  3253#  3302#  3353#  3396#  3462#  3529#  3589#  3713#
                    3717#  3737#  3781#  3785#  3805#  3849#  3853#  3873#  3918#  3922#  3942#  3986#  3990#
                    4010#  4054#  4058#  4078#  4122#  4126#  4146#  4190#  4194#  4214#  4244#  4400#  4507#
                    4614#  4724#  4824#  4833#  4918#  5056#  514'#  5150#  5235#  5373#  5457#  5466#  5551#
                    5689#  5773#  5782#  5869#  6012#  6097#  624'#  6475#  6673#  6677#  6691#  6705#  6719#
                    6733#  6912#  6974#  7052#  7167#  7171#  7248#  7307#  7383#  7452#  7546#  7640#  7742#
                    7843#  7945#  8047#  8149#  8250#  8352#  8454#  8556#  8657#  8759#  8861#  8972#  8978#
                    9025#  9071#  9139#  9375#  9730#  10082#  10325#  10527#  10738#  11040#  11532#  11923#  12315#
                    12712#  13085#
T$TAGL= 177777      1500#
T$TAGN= 010201      1500#  1689#  1711#  2189#  2203#  2226#  2235#  2244#  2253#  2262#  2278#  2294#  2306#
                    2887#  2909#  2926#  3002#  3017#  3042#  3065#  3104#  3123#  3171#  3221#  3254#  3303#
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                    2468   2474   2486   2491   2496   2502   2505   2510   2516   2522   2530   2536   2541
                    2546   2552   2557   2563   2572   2577   2582   2588   2592   2660   2670   2675   2689
                    2695   2708   2712   2718   2757   2767   2772   2790   2795   2812   2820   2828   2834
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                    3663   3668   3676   3682   3685   3718   3733   3738   3748   3752   3786   3801   3806
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6279	6287	6292	6301	6306	6324	6329	6338	6343	6351	6356	6365	6370
6386	6391	6407	6412	6423	6428	6444	6450	6453	6480	6490	6495	6508
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8782	8801	8806	8822	8827	8836	8842	8849	8867	8879	8884	8903	8908
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11691	11696	11706	11711	11723	11728	11737	11742	11756	11761	11770	11775	11803
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T$$AUT= 010017    3002#  3006
T$$CLE= 010020    3017#  3024  3031
T$$DAT= 010200   13292#  13298
T$$DU = 010021    3042#  3046  3053
T$$HAR= 010174   13201#  13232
T$$HW = 010000    1689#  1699
T$$INI= 010016    2926#  2982  2989
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T$$PRO= 010015    2909#
T$$PTA= 010177   13290#  13293  13294#
T$$RPT= 010014    2887#  2891  2898
T$$SEG= 010000    2468#  2504#  2510#  2521#  2530#  2551#  2557#  2591#  2660#  2694#  2708#  2717#  2757#
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                  9072#  9114
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T1      007160 G  1615  3103#
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T11	010154	G	1623	3589#
T12	010402	G	1624	3713#
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T12.2	010426		3737#	
T13	010446	G	1625	3781#
T13.1	010452		3785#	
T13.2	010472		3805#	
T14	010514	G	1626	3849#
T14.1	010520		3853#	
T14.2	010540		3873#	
T15	010560	G	1627	3918#
T15.1	010564		3922#	
T15.2	010604		3942#	
T16	010626	G	1628	3986#
T16.1	010632		3990#	
T16.2	010652		4010#	
T17	010672	G	1629	4054#
T17.1	010676		4058#	
T17.2	010716		4078#	
T18	010740	G	1630	4122#
T18.1	010744		4126#	
T18.2	010764		4146#	
T19	011004	G	1631	4190#
T19.1	011010		4194#	
T19.2	011030		4214#	
T2	007166	G	1614	3122#
T20	011052	G	1632	4244#
T21	011406	G	1633	4400#
T22	011602	G	1634	4507#
T23	011776	G	1635	4614#
T24	012172	G	1636	4724#
T25	012410	G	1637	4824#
T25.1	012414		4833#	
T25.2	012572		4918#	
T25.3	013070		5056#	
T26	013242	G	1638	5141#
T26.1	013246		5150#	
T26.2	013424		5235#	
T26.3	013722		5373#	
T27	014074	G	1639	5457#
T27.1	014100		5466#	
T27.2	014256		5551#	
T27.3	014554		5689#	
T28	014726	G	1640	5773#
T28.1	014732		5782#	
T28.2	015124		5869#	
T28.3	015460		6012#	
T29	015646	G	1641	6097#
T3	007252	G	1615	3170#
T30	016056	G	1642	6245#
T31	016500	G	1643	6475#
T32	017000	G	1644	6673#
T32.1	017004		6677#	
T32.2	017024		6691#	
T32.3	017044		6705#	

```
T32.4   017064          6719#
T32.5   017104          6733#
T33     017450 G        1645    6912#
T34     017550 G        1646    6974#
T35     017634 G        1647    7052#
T36     020026 G        1648    7167#
T36.1   020032          7171#
T36.2   020212          7248#
T36.3   020330          7307#
T36.4   020500          7383#
T37     020626 G        1649    7452#
T38     021000 G        1650    7546#
T39     021154 G        1651    7640#
T4      007340 G        1616    3220#
T40     021350 G        1652    7742#
T41     021536 G        1653    7843#
T42     021730 G        1654    7945#
T43     022124 G        1655    8047#
T44     022320 G        1656    8149#
T45     022506 G        1657    8250#
T46     022700 G        1658    8352#
T47     023074 G        1659    8454#
T48     023270 G        1660    8556#
T49     023456 G        1661    8657#
T5      007402 G        1617    3253#
T50     023650 G        1662    8759#
T51     024044 G        1663    8861#
T52     024240 G        1664    8972#
T52.1   024256          8978#
T52.2   024336          9025#
T52.3   024434          9071#
T53     024546 G        1665    9139#
T54     025322 G        1666    9375#
T55     026242 G        1667    9730#
T56     027162 G        1668   10082#
T57     027666 G        1669   10325#
T58     030274 G        1670   10527#
T59     030666 G        1671   10738#
T6      007466 G        1618    3302#
T60     031452 G        1672   11040#
T61     032710 G        1673   11532#
T62     034030 G        1674   11923#
T63     035150 G        1675   12315#
T64     036242 G        1676   12712#
T65     037326 G        1677   13085#
T7      007554 G        1619    3353#
T8      007616 G        1620    3396#
T9      007732 G        1621    3462#
UAM   = 000200 G        1792#
UNITNB  002362 G        1907#   2949*   2955*   2957
X$ALWA= 000000          1500#
X$FALS= 000040          1500#
X$OFFS= 000400          1500#
X$TRUE= 000020          1500#
$PATCH  037716 G       13275#
.     = 037754         1504#   1943#   1954#   2085#   2175#   2892    2983    3025    3047    3070    12718   13248#  13276#
```

D 8

13292 13300

. ABS. 037754 000

ERRORS DETECTED: 0

CVCDBA.BIC,CVCDBA/CRF:SYM/SOL/NL:TOC=SVC/ML,CVCDBA.P11
RUN-TIME: 74 85 6 SECONDS
RUN-TIME RATIO: 1069/166=6.4
CORE USED: 21K (42 PAGES)